Homework #1

Notice:

✓ Solve the problems **1 ~ 9**. The problem must be solved by hand. (Use note or blank paper)

✓ Scan and upload your result to KLAS assignment before due date. No late submission is allowed.

✓ You should solve the problems yourself. All answers should be written in Korean except any terminologies. No English sentence is allowed.

✓ Deadline – 23:59 on March 23rd, 2023 Thursday (UTC+9, Korean Standard Time)

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1. How many different truth tables exist for Boolean functions of N variables? You should explain why.

2. Convert the following decimal numbers to 8-bit two's complement numbers or indicate that the number would overflow the range.

   A. 38_{10}

   B. -24_{10}

   C. -67_{10}

   D. 137_{10}

   E. 127_{10}

3. Convert the following decimal numbers to 6-bit two's complement binary numbers and subtract them. Indicate whether the difference overflows a 6-bit result.
   (Note that you should perform subtraction in two's complement binary form, not in decimal form!)
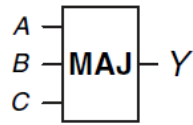
   A. $31_{10} - 17_{10}$

   B. $7_{10} - 9_{10}$

   C. $-32_{10} - 24_{10}$

   D. $12_{10} - 21_{10}$

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4. A majority gate produces a TRUE output if and only if more than half of its inputs are TRUE.


Complete a truth table and Boolean equation for the three-input majority gate of figure above.

Then, draw a schematic of majority gate using CMOS transistor logic. Use minimum number of transistors. Also, you should explain why your circuit works as majority gate.

A	B	C	Y

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5. Is it possible to assign logic levels so that a device with the transfer characteristics shown in figure below would serve as an inverter? If so, what are the input and output low and high levels (V_{IL}, V_{OL}, V_{IH}, and V_{OH}) and noise margins (NM_L and NM_H)? If not, explain why not.
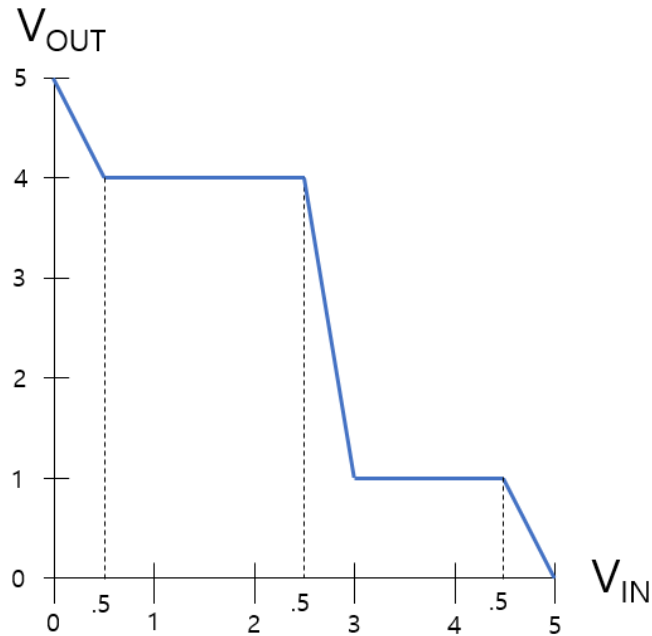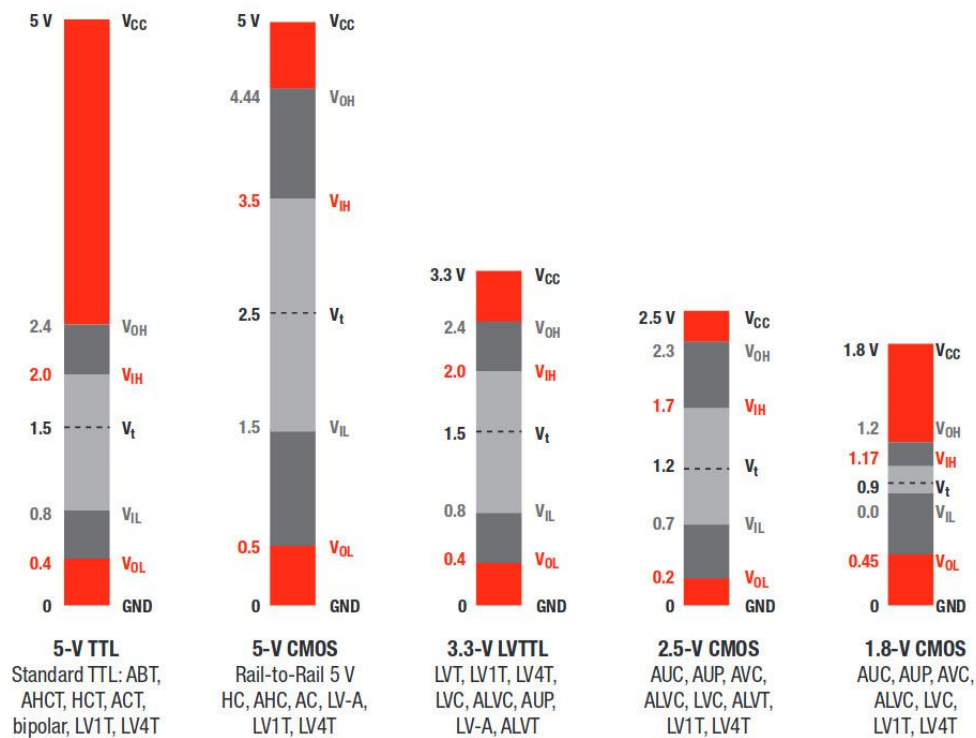
6. Write a truth table for the function performed by the gate in figure below. What is the name of this function?
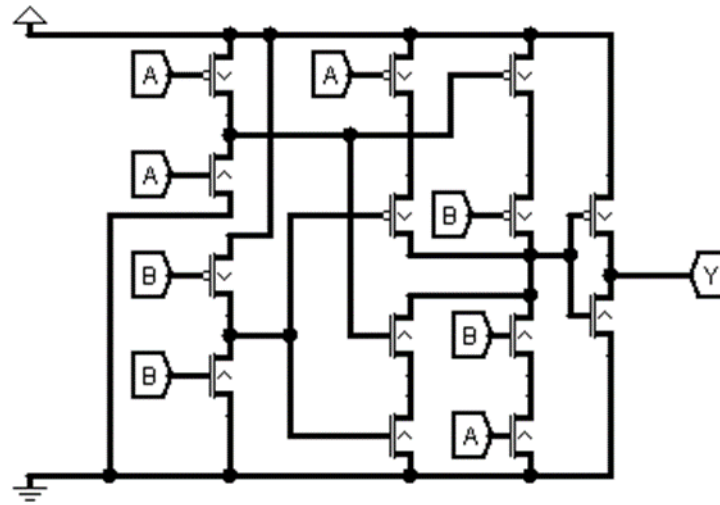
A	B	Y

7. There are various kinds of logic levels. Figure below is examples of logic levels.
   (Figure from Texas instruments, Logic Guide 2017)

A. Is it possible to connect 3.3-V LVTTL to 5-V CMOS as input? Explain it.
   (Assume all logics are 5V tolerant, which means you can connect up to 5V to all chips)

B. Is it possible to connect 5-V TTL to 2.5-V CMOS as input? Explain it.
   (Assume all logics are 5V tolerant, which means you can connect up to 5V to all chips)

C. Is it possible to connect 3.3-V LVTTL to 5-V TTL as input? Explain it.
   (Assume all logics are 5V tolerant, which means you can connect up to 5V to all chips)

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8. Complete a truth table and draw a CMOS schematic of Boolean equations given below.

$$Y = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$$

A	B	C	Y

9. How many different equations exist for Boolean functions of N variables? Explain why.