Homework #3

Notice:

- ✓ Solve the problems **1 ~ 8**. The problem must be solved by hand. (Use note or blank paper.)
- ✓ Scan and upload your result to KLAS assignment before due date. No late submission is allowed.
- ✓ You should solve the problems yourself. All answers should be written in Korean except any terminologies. No English sentence is allowed.
- ✓ All answers **must have enough solutions** to solve the problem.
- ✓ Deadline – 23:59 on May 25th, 2023, Thursday (UTC+9, Korean Standard Time)

1. Simplify the following Boolean equations using Boolean algebra.

   A. AC+A'B'C

   B. A'B'+A'BC'+(A+C')'

   C. ABCD' + A(BCD)' + (A+B+C+D)'

Hint: X + (X'Y) = X + Y (Redundancy law)

2. Multiplier is a circuit that multiplies two binary number. For example, if we multiply 1001_2 (9_{10}) and 1000_2 (4_{10}), output should be 0010 0100_2 (36_{10}). Design a 2-bit multiplier as shown in Figure 1.

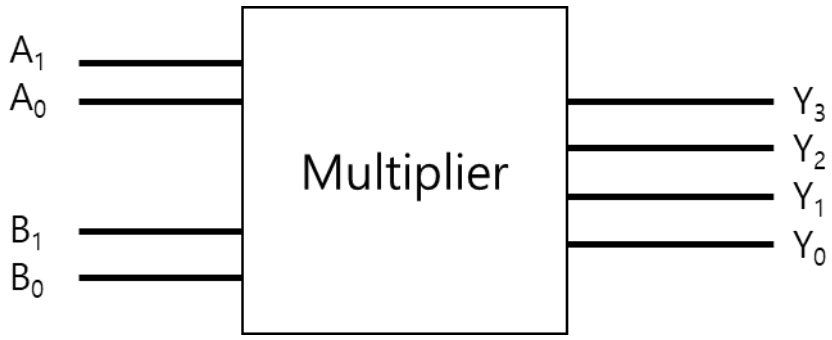

Figure 1 2-bit multiplier

A. Complete a truth table of 2-bit multiplier.

A_1	A_0	B_1	B_0	Y_3	Y_2	Y_1	Y_0

B. Boolean equation of Y

C. Schematic of 2-bit multiplier

D. In your schematic, which path is critical path? You should explain why.

E. Suppose your multiplier is between two flip-flops. You want to increase the clock frequency of your circuit; can you modify your circuit to be pipelined? (Assume you can add only one register) If so, where is the best place to have the register inserted?

3. Find a minimal Boolean equation for the function in table below using K-map and Quine-McCluskey method. Then compare the results of K-map and Quine-McCluskey method. Is it same or not? If not, describe why.

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	X
0	0	1	0	1
0	0	1	1	0
0	1	0	0	X
0	1	0	1	0
0	1	1	0	X
0	1	1	1	X
1	0	0	0	X
1	0	0	1	1
1	0	1	0	X
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	X

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4. Design a sequence detector whose output changes from 0 to 1 when the sequence 101 of an input in is detected. For example, if the sequence of 10101 is given as input, the sequence of output (except initial state) should be 00101 because there are two 101 sequences.

   A. Draw the state transition diagram and find the minimum number of flip-flops in each FSM.

   i. In Moore machine (Hint: need 4 states)

   ii. In Mealy machine
   (Hint: need 3 states, Hint 2: You can convert from Moore machine to Mealy machine.)

B. Draw an encoded state transition table and derive the equation(s) of the flipflop input(s)

i. In Moore machine

B. Draw an encoded state transition table and derive the equation(s) of the flipflop input(s) (cont'd)

ii. In Mealy machine

C. Draw an output table and derive the equation of output signal Y

i. In Moore machine

ii. In Mealy machine

D. Draw a schematic of the sequence detector.

i. In Moore machine

D. Draw a schematic of the sequence detector (cont'd)

ii. In Mealy machine

5. Ring counter, also known as one-hot counter, is a special kind of counter which has one-hot output. Unlike N-bit binary counter, which can count 2^N numbers, N-bit ring counter can count N numbers. For example, outputs of 3-bit ring counter are 100, 010, 001 for 0, 1, 2, respectively. Design a 7-bit ring counter with no input, which starts from 1000000 and ends with 0000001. On each clock edge, the output should advance to next one-hot. After reaching 0000001, it goes back to 1000000.

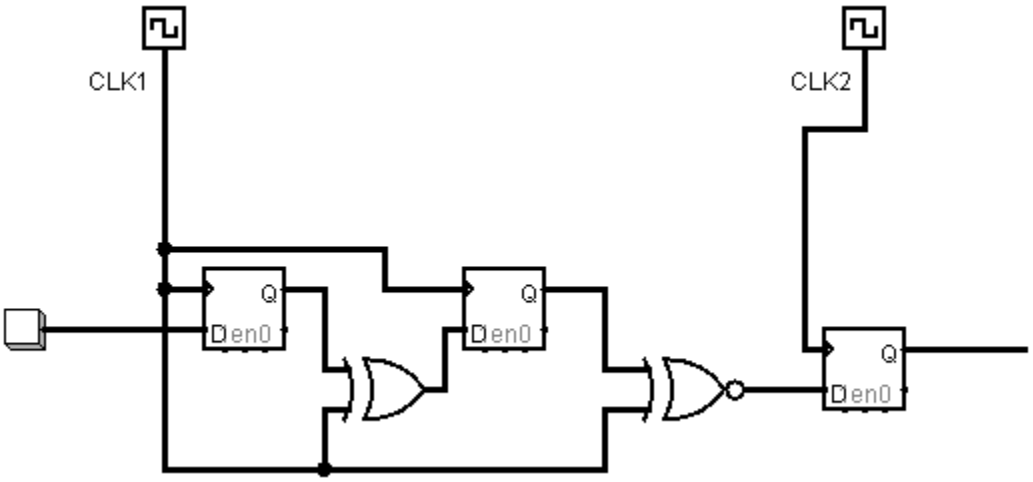
Number	One-hot						
0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0
2	0	0	1	0	0	0	0
3	0	0	0	1	0	0	0
4	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0
6	0	0	0	0	0	0	1

A. Finite state machine with output in each state transition diagram of ring counter with a minimum number of states.

B. Design a ring counter in finite state machine using states you defined above. You should provide state encoding table, state transition table, output table and Boolean equation of output. Also, you should use **minimum number of flip-flops** and simplify your equation as you can. (No schematic is required)

C. Is there any other easy way to design a 7-bit ring counter?

6. What is the problem of circuit below? Is there any possible way to solve the problem?

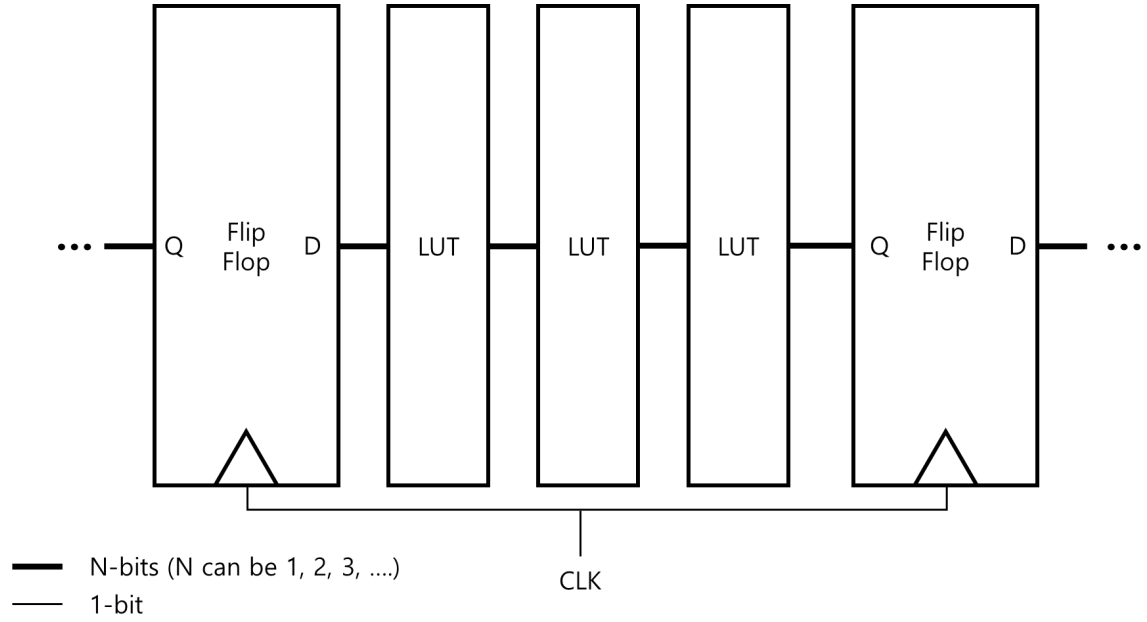


7. A field programmable gate array (FPGA) uses look-up tables (LUTs) rather than logic gates to implement combinational logic. The ESAL NoGwaje 3 FPGA has propagation and contamination delays of 0.49 and 0.24 ns, respectively, for each LUT. It also contains flip-flops with propagation and contamination delays of 0.71 and 0.31 ns, and setup and hold times of 0.51 and 0 ns, respectively.

   A. If you are building a logic circuit that needs to run at 110 MHz, how many consecutive LUTs can you use between two flip-flops? Assume there is no clock skew and no delay through wires between LUTs.

   B. Suppose that all paths between flip-flops pass through at least one LUT. How much clock skew can the FPGA have without violating the hold time?

C. Assume a circuit which has three LUTs between two flip-flops. What is the maximum operating **frequency** of FPGA?



8. Compute the MTBF of a two-flipflop synchronizer and a three-flipflop synchronizer.

$t_{setup} = t_{hold} = t_{dCQ} = t$ =200ps t_{ck} = 2ns must sample a f_{input} = 1MHz asynchronous signal τ=100ps & G = 3