

1.

$$\begin{aligned} (A) \quad AC + A'B'C &= C(A + A'B') \\ &= C(A + B') \quad (\because \text{Redundancy law}) \end{aligned}$$

$$\begin{aligned} (B) \quad A'B' + A'BC' + (A+C)' &= A'B' + A'BC' + A'C \\ &= A'(B' + BC' + C) \\ &= A'(B' + C' + C) \quad (\because \text{Redundancy law}) \\ &= A'(B' + 1) \\ &= A' \end{aligned}$$

$$\begin{aligned} (C) \quad ABCD' + A(BCD)' + (A+B+C+D)' &= ABCD' + A(B'+C'+D') + A'B'C'D' \\ &= ABCD' + AB' + AC' + AD' + A'B'C'D' \\ &= AD'(BC + 1) + AB' + AC' + A'B'C'D' \\ &= AB' + AC' + AD' + A'B'C'D' \\ &= AB' + AC' + D'(A + A'B'C') \\ &= AB' + AC' + D'(A + B'C') \quad (\because \text{Redundancy law}) \end{aligned}$$

2.

(A)

A <sub>1</sub>	A <sub>0</sub>	B <sub>1</sub>	B <sub>0</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

(B)

A <sub>1</sub> A <sub>0</sub>	00	01	10	11
B <sub>1</sub> B <sub>0</sub>				
00	0	0	0	0
01	0	0	0	0
11	0	0	0	1
10	0	0	0	0

$$Y_3 = A_1 A_0 B_1 B_0$$

A <sub>1</sub> A <sub>0</sub>	00	01	11	10
B <sub>1</sub> B <sub>0</sub>				
00	0	0	0	0
01	0	0	0	0
11	0	0	0	1
10	0	0	1	1

$$Y_2 = A_1 B_1 \bar{B}_0 + A_1 \bar{A}_0 B_1$$

$$= A_1 B_1 (\bar{A}_0 + \bar{B}_0)$$

$A_1 A_0$ $B_1 B_0$	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	1	0	1
10	0	1	1	0

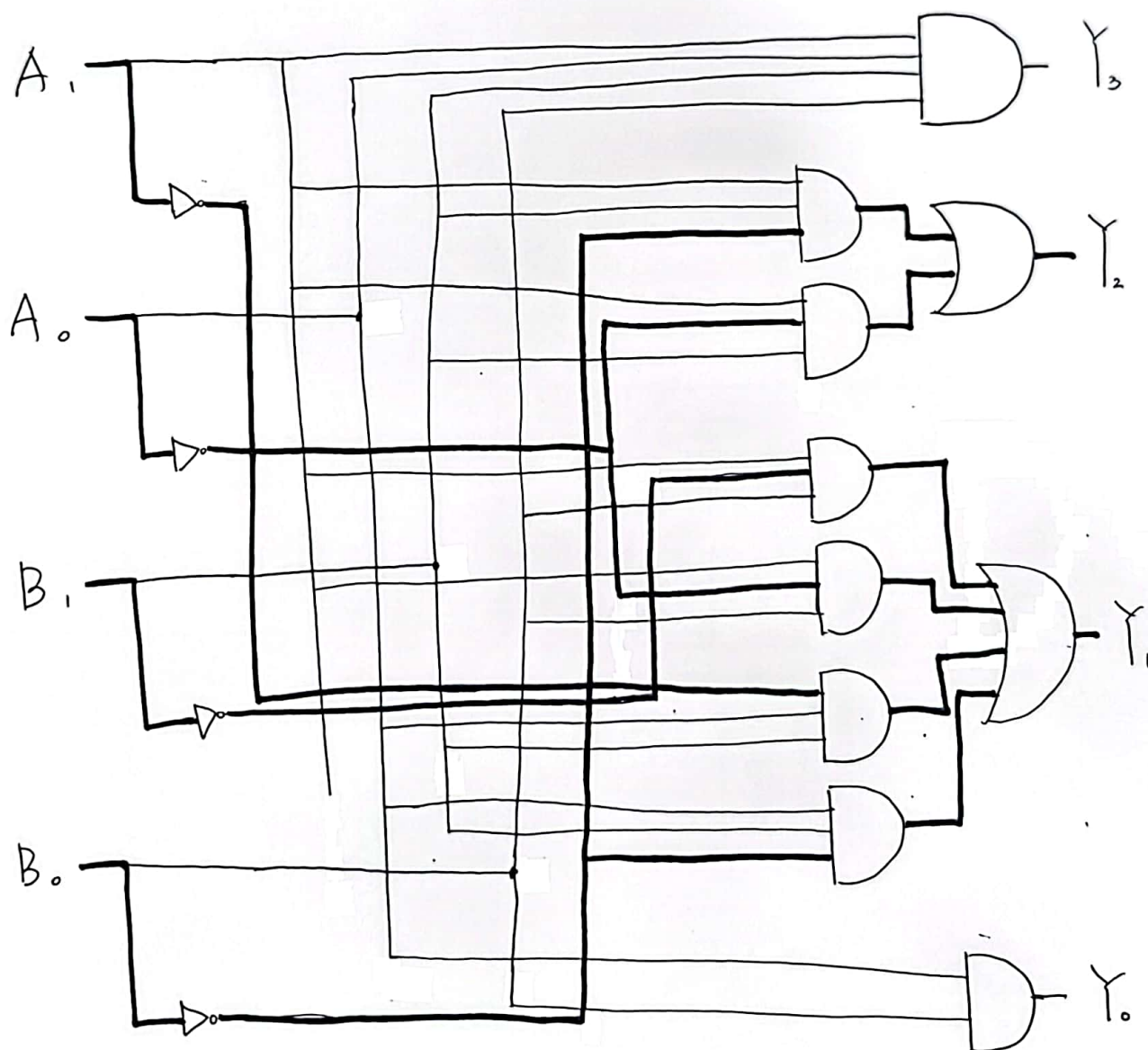
$A_1 A_0$ $B_1 B_0$	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	0	1	1	0
10	0	0	0	0

$$Y_1 = A_1 \bar{B}_1 B_0 + A_1 \bar{A}_0 B_0 + \bar{A}_1 A_0 B_1 + A_0 B_1 \bar{B}_0$$

$$Y_0 = A_0 B_0$$

$$= A_1 B_0 (\bar{A}_0 + \bar{B}_1) + A_0 B_1 (\bar{A}_1 + \bar{B}_0)$$

(C)



(D) (C)에서 굵게 그은 선들이 critical path 다. 거쳐가는 게이트가 NOT, AND, OR 세 개이므로

$$t_{pd} = t_{pd-NOT} + t_{pd-AND} + t_{pd-OR} \text{ 다.}$$

다른 path 들은 1개 혹은 2개의 게이트만을 지나므로 굵게 그은 선들이 critical path 다.

(E) 전파 지연 시간의 민감도가 최소가 되도록 레지스터를 삽입하면 클럭 주기가 최소화 됩니다.

AND Gate 이전 부분에 레지스터를 삽입합니다.

3.

K-map

AB \ CD	00	01	11	10
00	0	X	0	X
01	X	0	1	1
11	0	X	X	0
10	1	X	1	X

$$Y = A\bar{C}D + C\bar{D}$$

Quine-McCluskey

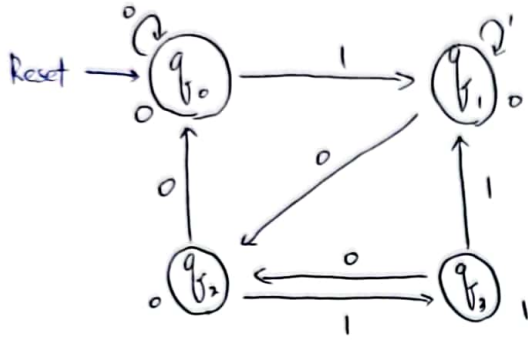
	Column I	Column II	Column III
1	0 0 0 1 ✓	- 0 0 1 *	- - 1 0 *
2	0 0 1 0 ✓	0 - 1 0 ✓	<del>0 0 1 0</del>
4	0 1 0 0 ✓	- 0 1 0 ✓	- 1 1 - *
8	1 0 0 0 ✓	0 1 - 0 *	<del>1 1 - 0</del>
6	0 1 1 0 ✓	1 0 0 - *	
9	1 0 0 1 ✓	1 0 - 0 *	
10	1 0 1 0 ✓	0 1 1 - ✓	
7	0 1 1 1 ✓	- 1 1 0 ✓	
13	1 1 0 1 ✓	1 - 0 1 *	
14	1 1 1 0 ✓	1 - 1 0 ✓	
15	1 1 1 1 ✓	- 1 1 1 ✓	
		1 1 - 1 *	
		1 1 1 - ✓	

prime implicant	00	10	100	110	111
- 0 0 1			↓		
0 1 - 0			↓		
1 0 0 -			↓		
1 0 - 0			↓		
1 - 0 1			↓	↓	
1 1 - 1				↓	
- - 1 0	↓				↓
- 1 1 -					↓

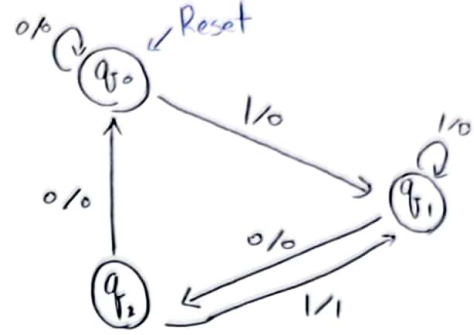
$$Y = A\bar{C}D + C\bar{D}$$

4.

(A) i) Moore machine



ii) Mealy Machine

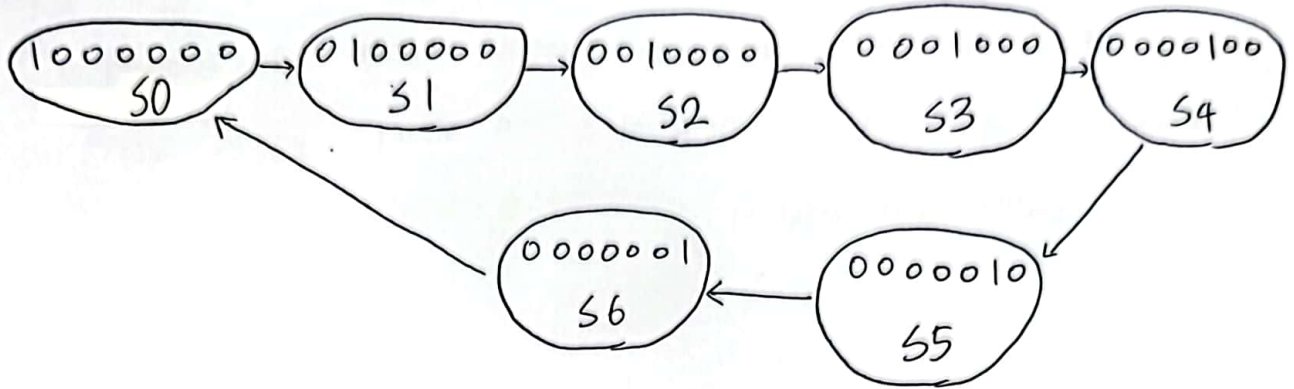


(B)



5.

(A)



(B)

state transition table

Current state							Next state						
$S_6$	$S_5$	$S_4$	$S_3$	$S_2$	$S_1$	$S_0$	$S_6'$	$S_5'$	$S_4'$	$S_3'$	$S_2'$	$S_1'$	$S_0'$
1	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	0	1	0
0	0	0	0	0	1	0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0

state encoding table

State	Encoding
S0	1000000
S1	0100000
S2	0010000
S3	0001000
S4	0000100
S5	0000010
S6	0000001

output table

Current state							Output						
$S_6$	$S_5$	$S_4$	$S_3$	$S_2$	$S_1$	$S_0$	$Y_6$	$Y_5$	$Y_4$	$Y_3$	$Y_2$	$Y_1$	$Y_0$
1	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	0
0	0	0	1	0	0	0	0	0	0	1	0	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0

$$Y_n = S_n (n=0,1,2,3,4,5,6),$$

$$S_6' = S_0, S_5' = S_6, S_4' = S_5$$

$$S_3' = S_4, S_2' = S_3, S_1' = S_2, S_0' = S_1$$

6. 플립플롭을 왼쪽에서부터  $f1$ ,  $f2$ ,  $f3$  라고 하자.

$CLK1$  과  $CLK2$  가 비동기일 가능성이 존재하므로  $f2$  에서  $f3$  로 신호 전달되는  
와중에  $CLK2$  가 rising edge를 클럭한다면 metastable한 스테이트가  $f3$ 로부터 클럭된다,  
metastable한 state의 빈도수가 최소가 되도록 하기 위해서 플립플롭을 추가하여  
MTBF를 증가시키면 문제가 해결됩니다.



7.

(A)

$$T_c = \frac{1}{110} \text{ ns}$$

$$T_c \geq t_{pcq} + N t_{pd-cvb} + t_{setup}$$

$$\frac{10^3}{110} \text{ ns} \geq (0.71 + 0.49N + 0.51) \text{ ns}$$

$$N \leq 16.06$$

$$\therefore \boxed{\text{maximum: } 16}$$

$$(B) \quad t_{skew} < t_{ccq} + t_{cd-cvb} - t_{hold}$$

$$t_{skew} < 0.31 \text{ ns} + 0.24 \text{ ns} - 0 \text{ ns}$$

$$t_{skew} < 0.55 \text{ ns} = 550 \text{ ps}$$

$$\boxed{t_{skew} < 550 \text{ ps}}$$

$$(C) \quad T_c \geq t_{pcq} + 3 t_{pd-cvb} + t_{setup}$$

$$T_c \geq (0.71 + 3 \times 0.49 + 0.51) \text{ ns}$$

$$T_c \geq 2.69 \text{ ns}$$

$$f_c = \frac{1}{T_c} \leq \frac{1}{2.69} \text{ GHz} = 0.37 \text{ GHz}$$

$$\therefore \boxed{\text{maximum: } 0.37 \text{ GHz}}$$

8.

i) two-flipflop synchronizer

$$P_E = \frac{400p}{2n} = 0.2$$

$$P_V = \frac{1}{3} e^{-\frac{1.6}{0.1}} = \frac{1}{3} e^{-16} = 0.4 \times 10^{-7}$$

$$(t_w = t_{cl} - t_{setup} - t_{dca} = 2ns - 0.4ns = 1.6ns)$$

$$P_F = P_E P_V = 0.8 \times 10^{-8}$$

$$R_F = f_{input} \cdot P_F = 0.8 \times 10^{-2}$$

$$MTBF \sim 125 \text{ seconds}$$

↳ 1 failure every 125 seconds ~ every 2 minutes.

ii) three flipflop synchronizer

$$P_E = 0.2$$

$$P_V = \frac{1}{3} e^{-\frac{3.2}{0.1}} = \frac{1}{3} e^{-32} = 4.2 \times 10^{-15}$$

$$(t_w' = t_w \times 2FF = 3.2ns)$$

$$P_F = P_E P_V = 8.4 \times 10^{-16}$$

$$R_F = f_{input} \cdot P_F = 8.4 \times 10^{-10}$$

$$MTBF \sim 1.2 \times 10^9 \text{ seconds} \sim \text{more than } 38 \text{ years.}$$