40-Bit Ripple Carry Adder in Verilog

A ripple carry adder (RCA) is a logic circuit that adds two binary numbers using multiple full adders that ripples carry bits from the previous bit position to the next one.

[Homework 4] Implement a 40-bit RCA in Verilog. The module header is given as follows for the verification with OUR testbenches. [IMPORTANT] If your design does not execute OUR testbenches due to the mismatches in the module header, the verification grade will be zero.

```
module rca_40b (S, A, B, Cout, Cin);

   input [39:0]  A, B;
   input         Cin;
   output [39:0] S;
   output        Cout;

{your code for RCA}

endmodule
```

```
module tb_rca_40b;

{your testbench code for RCA}

endmodule
```

The filename for your source code is given below (Note that automated script will grade your code, so check your filename before submission. Wrong filename will decrease 30% of your Verilog code score)

- Your RCA implementation: rca40.v
- Your RCA testbench: tb_rca40.v
- Name of additional files: Decide as you want

What you need to submit:

1. Report
   - Problem statement (5%)
   - Descriptions for inputs and outputs (5%)
   - Gate-level design and schematic of a full adder (5%)
     - The process of design (e.g., K-map) should be given.
   - Block diagram of your RCA (5%)
   - Descriptions of the operation of your RCA with few examples (15%)
     - Why do you need Cin?
     - What is the value of Cin?
   - Code analysis (line-by-line code description is needed) (15%)
   - RTL view and flow summary from Intel Quartus Prime (5%)
   - Testbench waveform (5%)
     - Any simulator or waveform viewer can be used, but it is recommended to use ModelSim or QuestaSim
   - **Verification strategy & corresponding examples with explanation (40%)**
     - Why your testbench can verify your RCA implementation?
     - Why this testbench?
   - You should submit your report in **PDF format**!!!!! (-10% if you submit non-PDF report)
2. Verilog code **with sufficient comments**
   - Verilog code for RCA (rca40.v)
   - Verilog code for testbenches (tb_rca40.v)
     i. Testbenches that you used to verify your RCA (The quantity as well as the quality of testbenches are very important)
   - Additional Verilog code files required (optional)
   - IMPORTANT: TWO Verilog files (RCA code and testbench) must be present separately so that OUR testbench can be used with your RCA code.
   - You don't have to submit entire Quartus project. What you need to submit is files described above.

3. **How to submit**

   - Compress your report and program into single zip file and upload it to KLAS assignment menu. The filename of your zip file should be "학번_RCA.zip". (e.g., 2022123456_RCA.zip)

4. **Deadline – 23:59 PM on June 11th, 2023**

   - On-line submission: Report and Verilog codes
   - No late submission allowed!!

Grade will be given based on the following criteria

1. Reports 40%
2. Verilog codes 20%
3. Verification with **our** examples 40%
   - Total 80 testbenches will be given, which means you will get 0.5 points per testbench.