EE115C – Digital Electronic Circuits
Project Submission

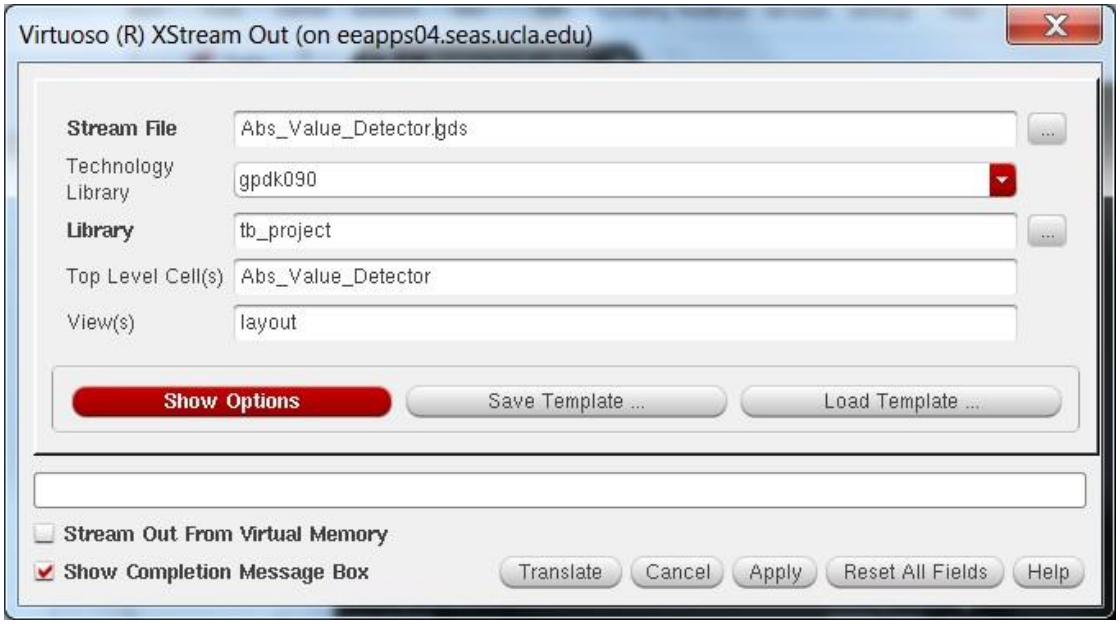
Due Friday, March 10, 10am
(e-mail submission: ee115c.w17@gmail.com)

Following components need to submitted for your project:

1. Presentation Slides:
   - **a.** Use the template provided online *(Do not add additional slides)*.
   - **b.** Also bring a copy to presentation in a USB Flash drive in case there is any error. *(PowerPoint or PDF)*.
   - **c.** Please name the file as: "**present_team_<no>**" *(replace <no> with your team number)*.
2. One-Page Report (optional)
   - **a.** You may write a **1-page report in text** to elaborate your ideas shown in slides.
   - **b.** Please name the file as: "**report_team_<no>**" *(replace <no> with your team number)*.
3. Project Files (3 files, compressed into one folder):
   - **a.** Layout:

     You need to export a **gds** file for your layout to include all the layout information. From the `CDS.log` window (the main window of cadence), choose `File > Export > Stream`…

     The following window will pop up:



Click on `Browser` of the `Library` field and find your `Abs_Value_Detector` layout. Set the remainder of the parameters as shown above and click `Apply`.

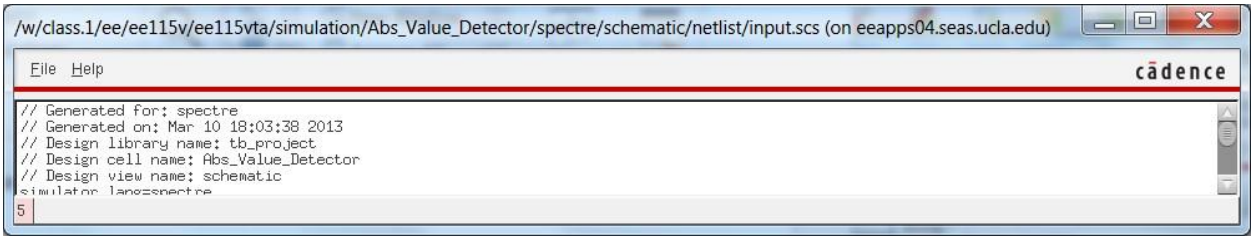
A **gds** file is streamed. A pop window will let you know about any errors in the stream out process. The **gds** file would be present under your working directory.

Rename the file to "**design_team_<no>.gds"** *(replace <no> with your team number)* before submission.

b. Schematic:

Open your `Abs_Value_Detector` schematic and go to `Launch > ADE L` and then, `Simulation > Netlist > Create`

A log file should be opened with a netlist for your design like this.



The netlist is created in your simulation directory. To get the path, you can just replace "input.scs" in the title of the above figure (yours obviously) with "netlist". Make a copy of this file and rename it "**test_circuit_team_<no>"** *(replace <no> with your team number)*.

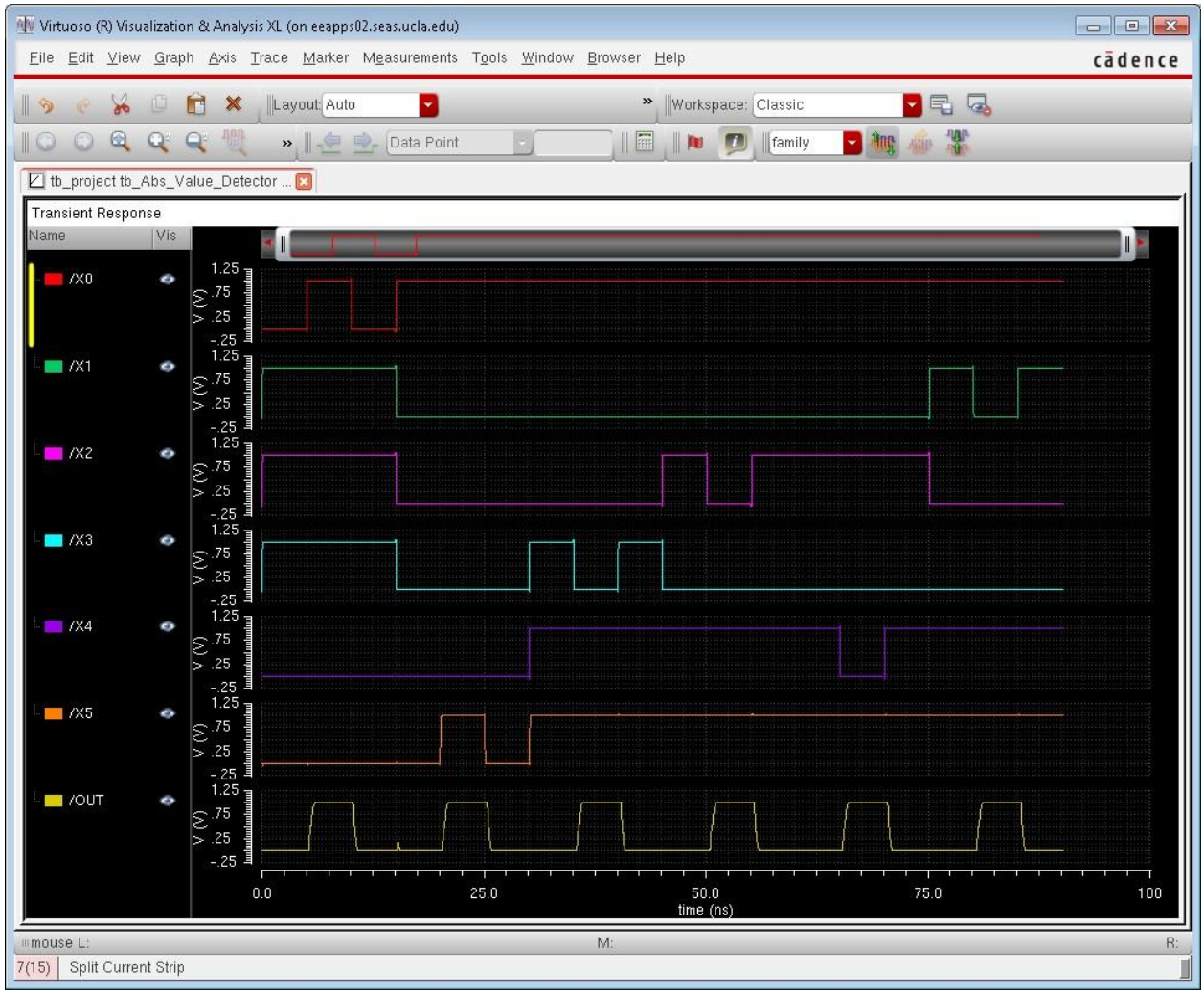
c. Simulation Results:

Attach screenshots of your design performance in testbench, like the figures below.

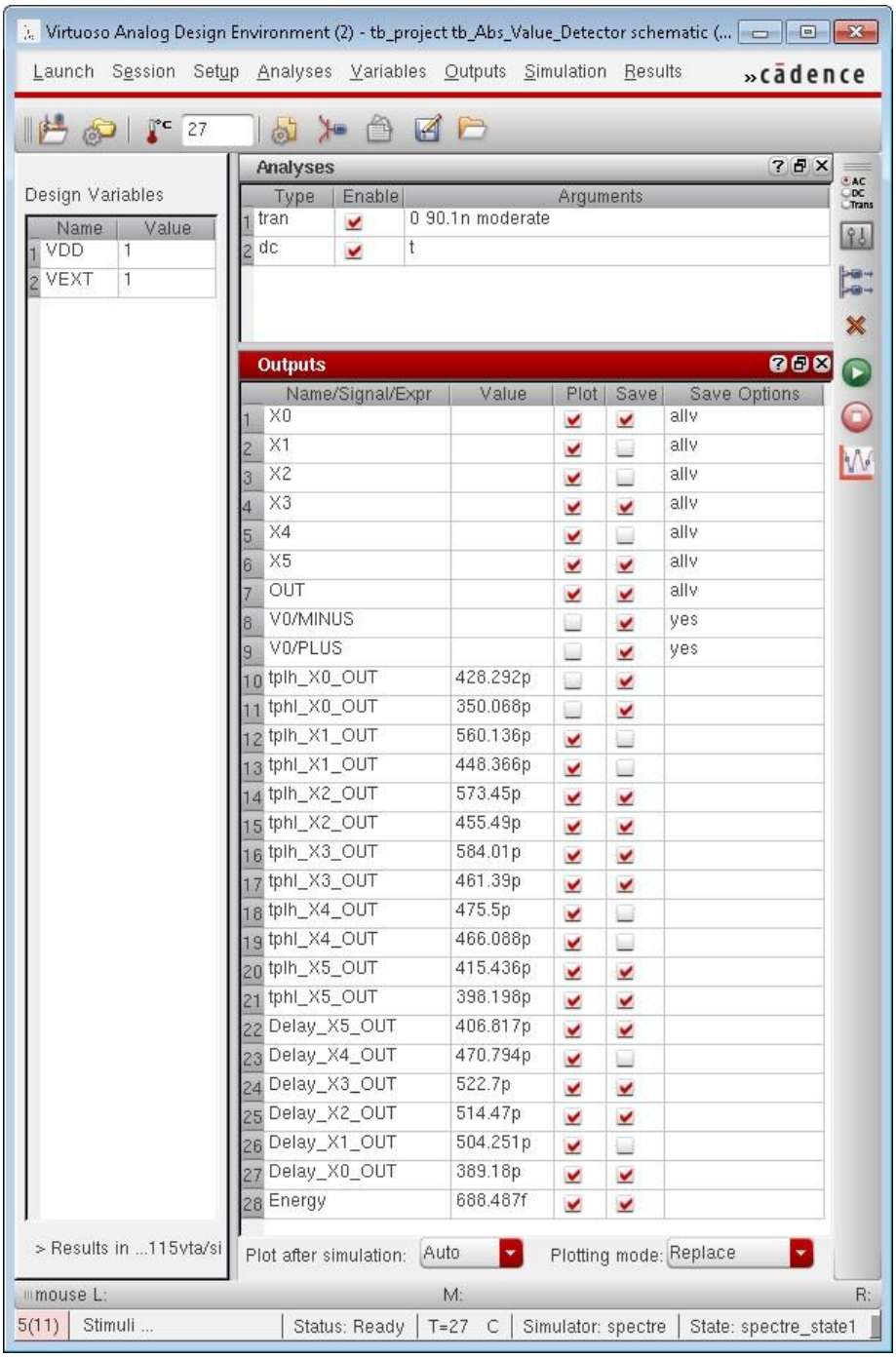
(Attach screenshots for scaled – lowered – voltage value, both schematic and postlayout results)

(Also make sure VDD and VEXT Match and worst delay, t_{pLH}, or t_{pHL} is less than equal to 1ns)

Transient **waveforms**:



Delay and **Energy** numbers: (You may need two figures to capture all the numbers):



You should also include screenshots for your layout verification (**DRC** and **LVS**) in this file, as well as a brief explanation on **work distribution of team members**.

For all the screenshots in this section, paste them in a Microsoft Word file and name it "**result_team_<no>.docx"** *(replace <no> with your team number)*. Alternatively, you can submit a pdf, if you prefer.

Please pack all your project files ("design_team_<no>.gds", "test_circuit_team_<no>", and "result_team_<no>.docx") in a folder, compress it and name it **"prj_team_<no>.rar"** *(replace <no> with your team number)*.

IN SUMMARY:

You need to submit the following by Fri, March 10, 10am to ee115c.w17@gmail.com:

1. Presentation slides (`present_team_<no>.pptx` or `ppt` or `pdf`)
2. OPTIONAL: 1-page report (`report_team_<no>.txt`)
3. Project files (`prj_team_<no>.rar`), which should include:
    a. Layout: (`design_team_<no>.gds`)
    b. Schematic: (`test_circuit_team_<no>`)
    c. Simulation Results: (`result_team_<no>.docx` or `doc` or `pdf`)