EE115C – Digital Electronic Circuits
Project Testbench

This provides a method for you to test your design in Cadence. “□” denotes a blank space explicitly.

1. Copy the test file **`tb_project.tar`** to your working directory (default:

`~/ee115c`)

```
>cp□/w/class.1/ee/ee115v/ee115vta/ee115c_w17/tb_project.tar
□~/ee115c
```

2. From your `~/ee115c` directory, extract the archive with the following command:

```
>tar□–xvf□tb_project.tar
```

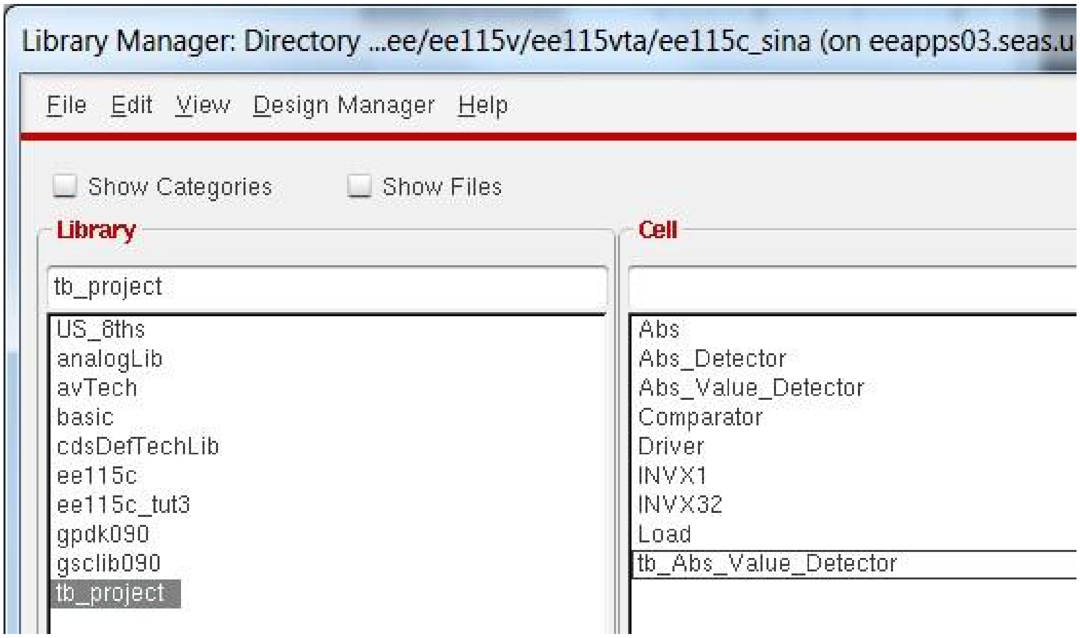
This would create a directory “**`tb_project`**” under your working directory.

3. Edit **`cds.lib`** file in your working directory to add the following line at the end.

```
DEFINE□tb_project□~/ee115c/tb_project
```

This tells Cadence to consider the directory we just copied as a Cadence library.

4. Now launch Cadence as usual. You should now see a new library test_project.



Library Manager: Directory ...ee/ee115v/ee115vta/ee115c_sina (on eeapps03.seas.u

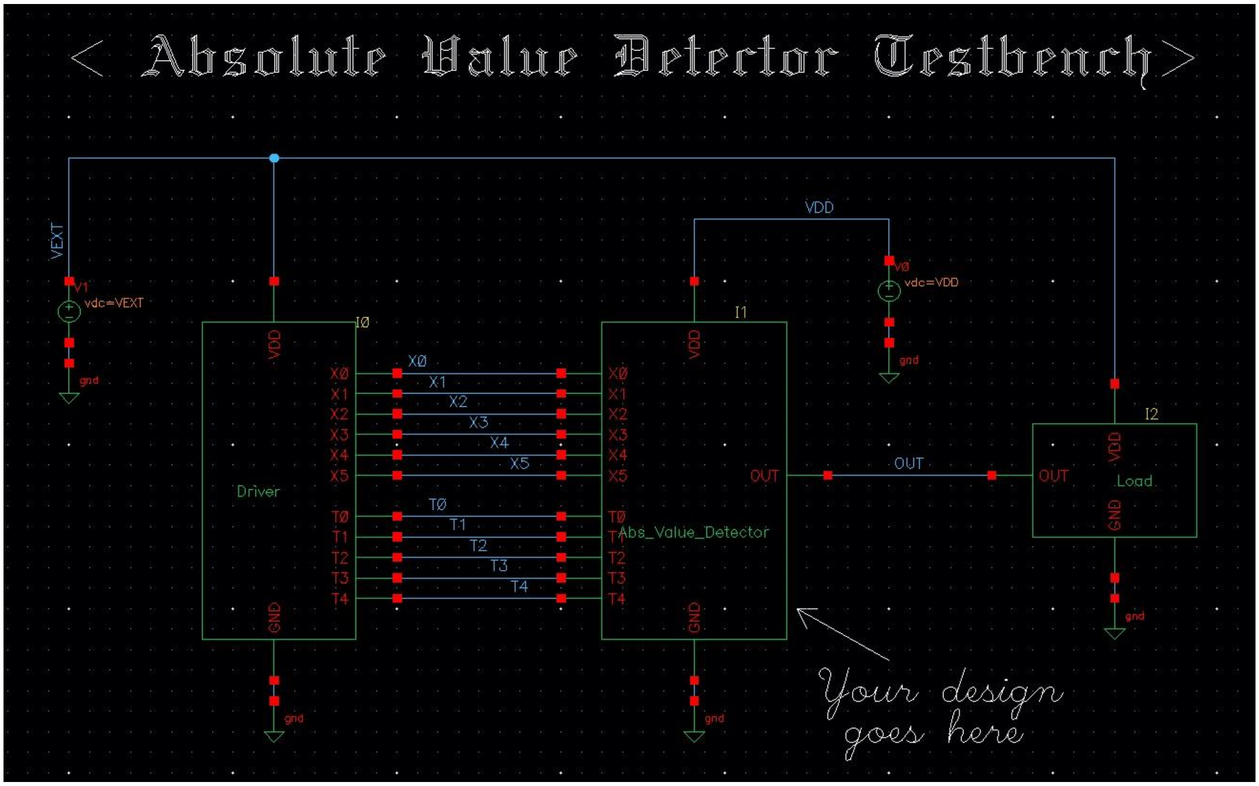
Library: tb_project

US_8ths
analogLib
avTech
basic
cdsDefTechLib
ee115c
ee115c_tut3
gpdk090
gsclib090
tb_project

Cell:

Abs
Abs_Detector
Abs_Value_Detector
Comparator
Driver
INVX1
INVX32
Load
tb_Abs_Value_Detector

Open the schematic “**`tb_Abs_Value_Detector`**”.



Replace the **“`Abs_Value_Detector`”** (this is an example design) in the library “`tb_project`” **with your own absolute value detector** design. <u>Please make sure that your design is named</u> **“`Abs_Value_Detector`”**. Also make sure that you have the following pins on your design:

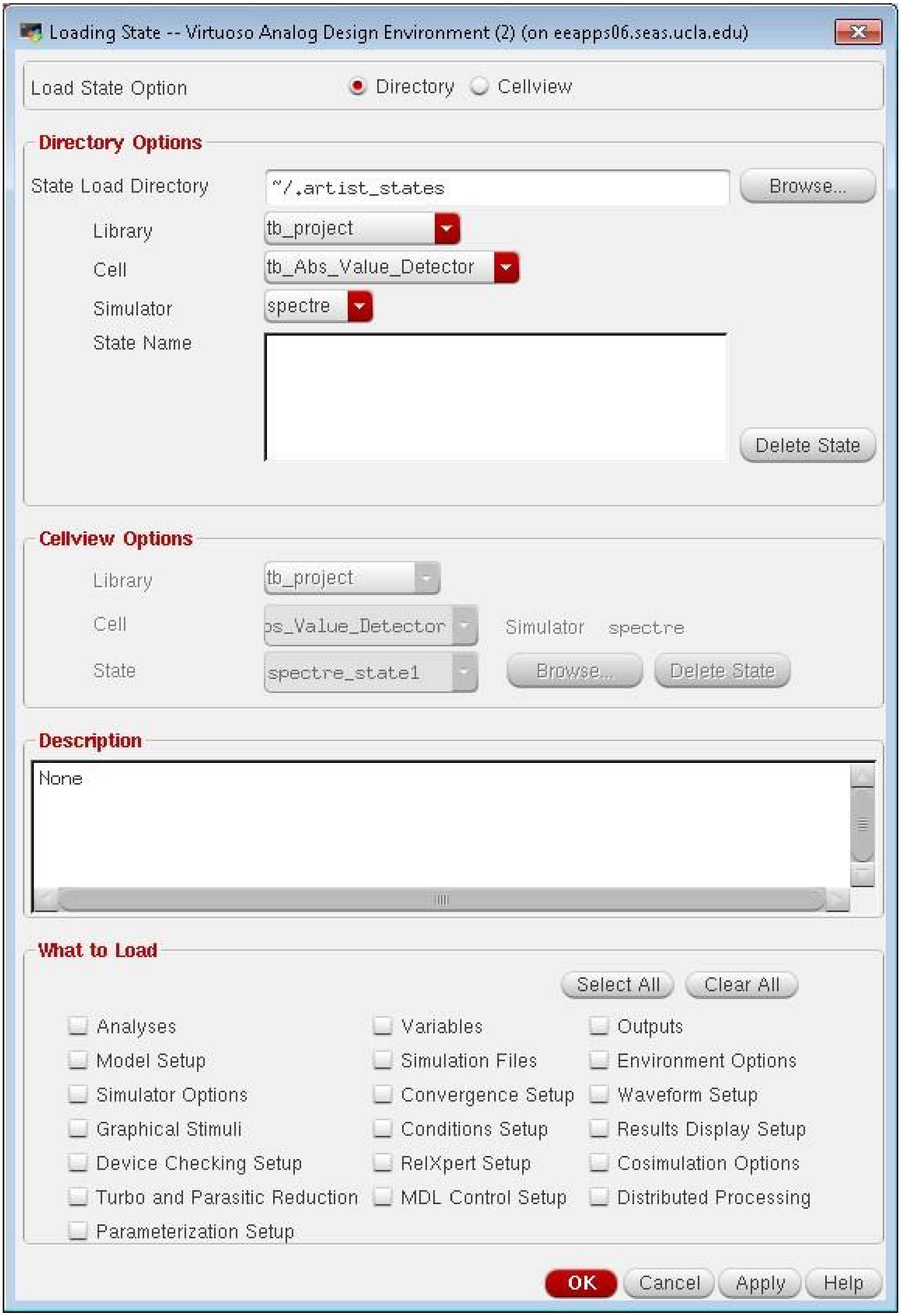
> **`X0, X1, X2, X3, X4, X5, T0, T1, T2, T3, T4, VDD, GND,`** and **`OUT.`**

The above pins are case sensitive. It is important to maintain this consistency in your design name and pin names of the design, for the verification steps to be posted later. Please check the port names in the sample design provided with this testbench to verify that your design and port names are correct.

Note: Once you make sure that the pins names and design name is consistent, you can copy the schematic view of your `Absolute Value Detector` design to the “`tb_project`” library. **You can still retain the symbol view** that you have been provided, to allow very easy replacement of the adder in the testbench schematic.

Save the schematic for “`tb_Abs_Value_Detector`” after your design has been replaced.

Now in the schematic window of `tb_Abs_Value_Detector` click “`Launch → ADE L`”. When Analog Design Environment opens, go to: “`Session → Load State…`”. The following window shows up.



Loading State -- Virtuoso Analog Design Environment (2) (on eeapps06.seas.ucla.edu)

Load State Option ● Directory ○ Cellview

Directory Options

State Load Directory: ~/.artist_states

Library: tb_project

Cell: tb_Abs_Value_Detector

Simulator: spectre

State Name:

Cellview Options

Library: tb_project

Cell: ps_Value_Detector

Simulator: spectre

State: spectre_state1

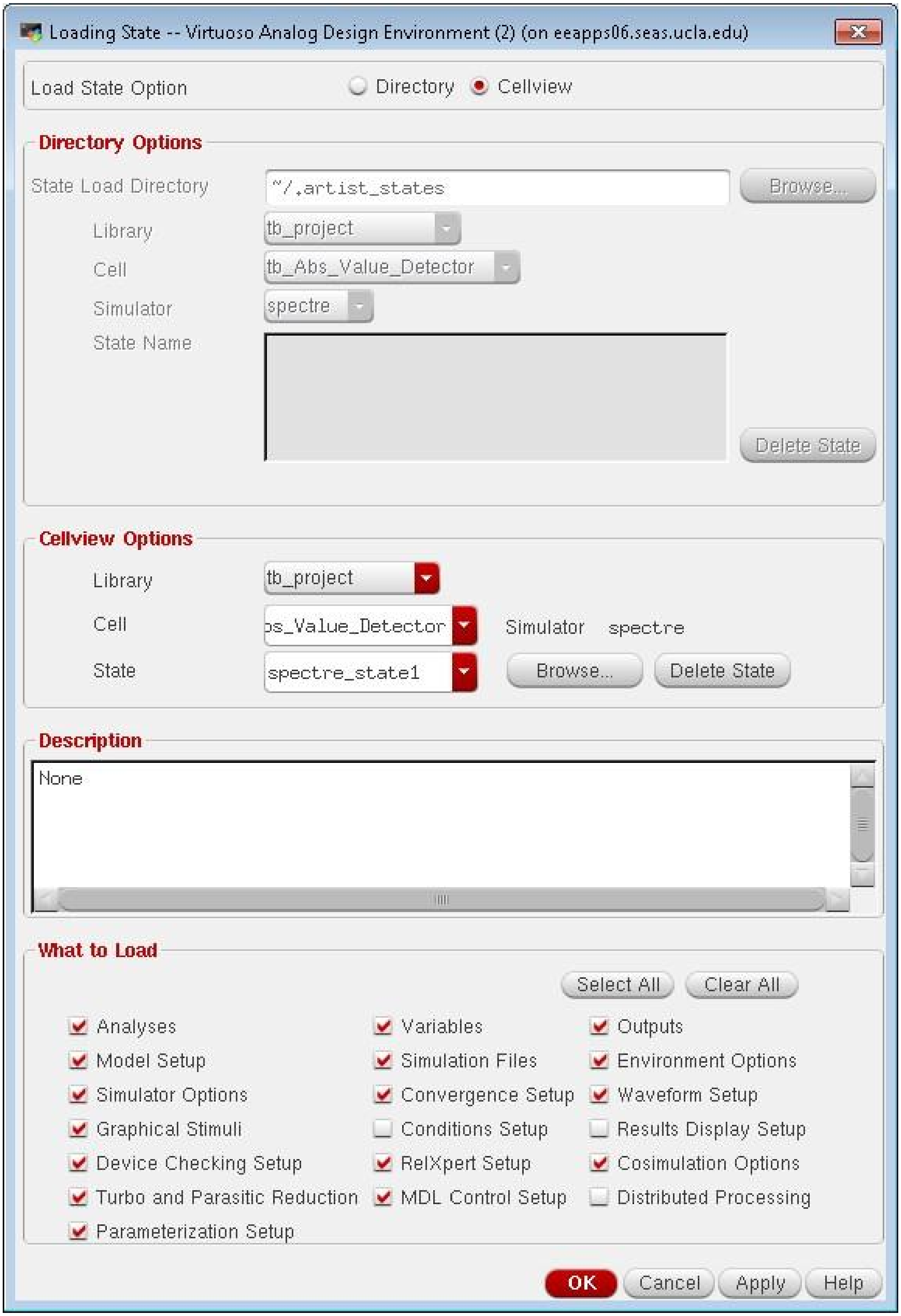
Description

None

What to Load

- □ Analyses
- □ Model Setup
- □ Simulator Options
- □ Graphical Stimuli
- □ Device Checking Setup
- □ Turbo and Parasitic Reduction
- □ Parameterization Setup
- □ Variables
- □ Simulation Files
- □ Convergence Setup
- □ Conditions Setup
- □ RelXpert Setup
- □ MDL Control Setup
- □ Outputs
- □ Environment Options
- □ Waveform Setup
- □ Results Display Setup
- □ Cosimulation Options
- □ Distributed Processing

Choose “`Cellview`” in “`Load State Option`”, the window becomes:



Loading State -- Virtuoso Analog Design Environment (2) (on eeapps06.seas.ucla.edu)

Load State Option ○ Directory ● Cellview

Directory Options

State Load Directory: ~/.artist_states

Library: tb_project

Cell: tb_Abs_Value_Detector

Simulator: spectre

State Name:

Cellview Options

Library: tb_project

Cell: bs_Value_Detector

Simulator: spectre

State: spectre_state1

Description

None

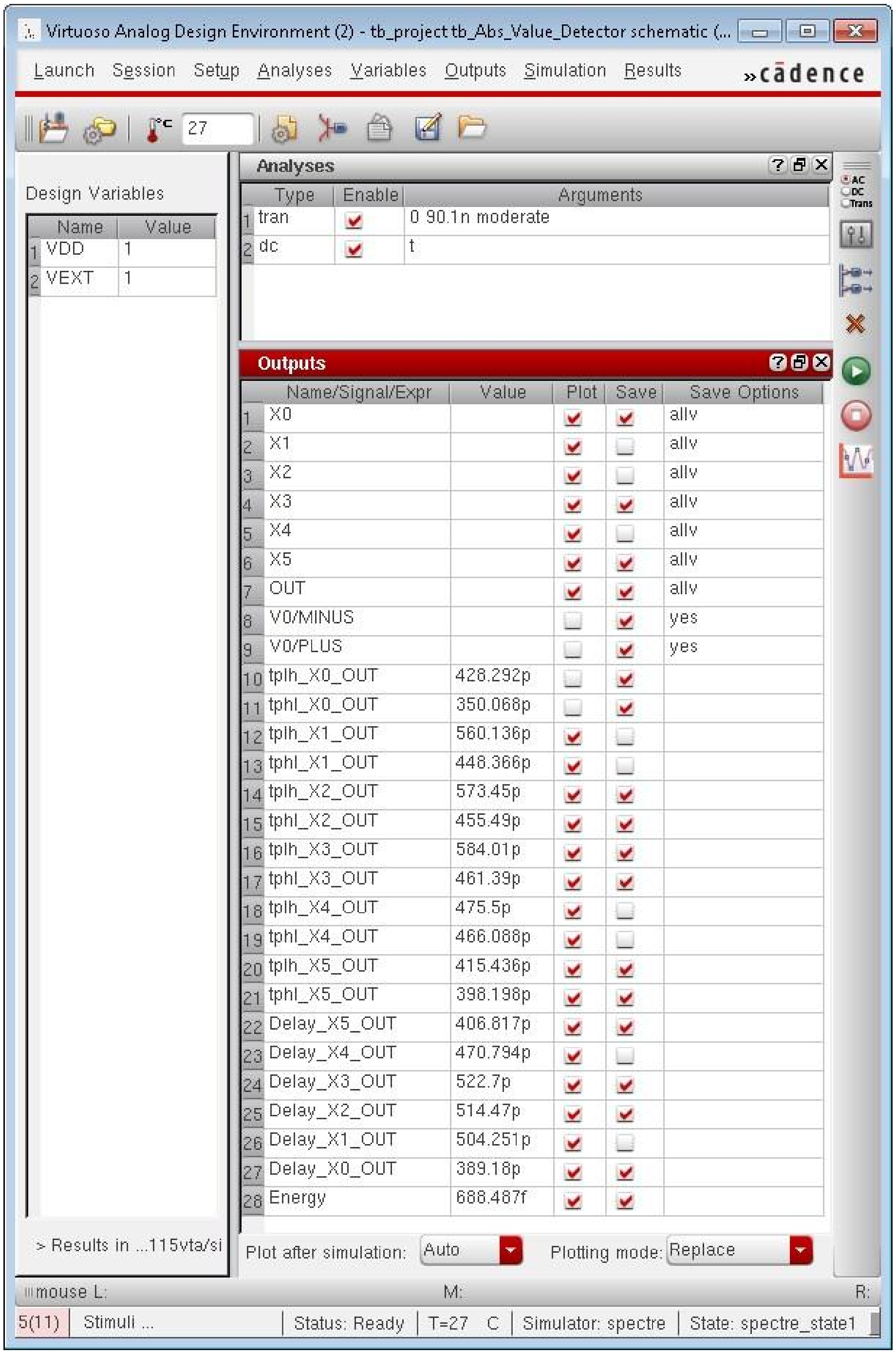
What to Load

- ☑ Analyses
- ☑ Model Setup
- ☑ Simulator Options
- ☑ Graphical Stimuli
- ☑ Device Checking Setup
- ☑ Turbo and Parasitic Reduction
- ☑ Parameterization Setup
- ☑ Variables
- ☑ Simulation Files
- ☑ Convergence Setup
- □ Conditions Setup
- ☑ RelXpert Setup
- ☑ MDL Control Setup
- ☑ Outputs
- ☑ Environment Options
- ☑ Waveform Setup
- □ Results Display Setup
- ☑ Cosimulation Options
- □ Distributed Processing

The state “`spectre_state1`” is just the simulation settings we need, click “`OK`”.
This will set the variables needed for the testbench, the outputs to be evaluated and the analysis to be performed.

The inputs include 16 transitions with input pattern changes due to the probability distribution given earlier in the project description. Another pattern due to the same probability distribution would be used to check your final submission later.

Now you can run the simulation. For the sample design given to you, operating at 1V, you will see an output as follows: (`VDD` and `VEXT` have to always match).



Virtuoso Analog Design Environment (2) - tb_project tb_Abs_Value_Detector schematic (...

Launch Session Setup Analyses Variables Outputs Simulation Results
cādence
27

Design Variables

	Name	Value
1	VDD	1
2	VEXT	1

Analyses

	Type	Enable	Arguments
1	tran	☑	0 90.1n moderate
2	dc	☑	t

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	X0		☑	☑	allv
2	X1		☑	□	allv
3	X2		☑	□	allv
4	X3		☑	☑	allv
5	X4		☑	□	allv
6	X5		☑	☑	allv
7	OUT		☑	☑	allv
8	V0/MINUS		□	☑	yes
9	V0/PLUS		□	☑	yes
10	tplh_X0_OUT	428.292p	□	☑	
11	tphl_X0_OUT	350.068p	□	☑	
12	tplh_X1_OUT	560.136p	☑	□	
13	tphl_X1_OUT	448.366p	☑	□	
14	tplh_X2_OUT	573.45p	☑	☑	
15	tphl_X2_OUT	455.49p	☑	☑	
16	tplh_X3_OUT	584.01p	☑	☑	
17	tphl_X3_OUT	461.39p	☑	☑	
18	tplh_X4_OUT	475.5p	☑	□	
19	tphl_X4_OUT	466.088p	☑	□	
20	tplh_X5_OUT	415.436p	☑	☑	
21	tphl_X5_OUT	398.198p	☑	☑	
22	Delay_X5_OUT	406.817p	☑	☑	
23	Delay_X4_OUT	470.794p	☑	□	
24	Delay_X3_OUT	522.7p	☑	☑	
25	Delay_X2_OUT	514.47p	☑	☑	
26	Delay_X1_OUT	504.251p	☑	□	
27	Delay_X0_OUT	389.18p	☑	☑	
28	Energy	688.487f	☑	☑	

> Results in ...115vta/si

Plot after simulation: Auto   Plotting mode: Replace

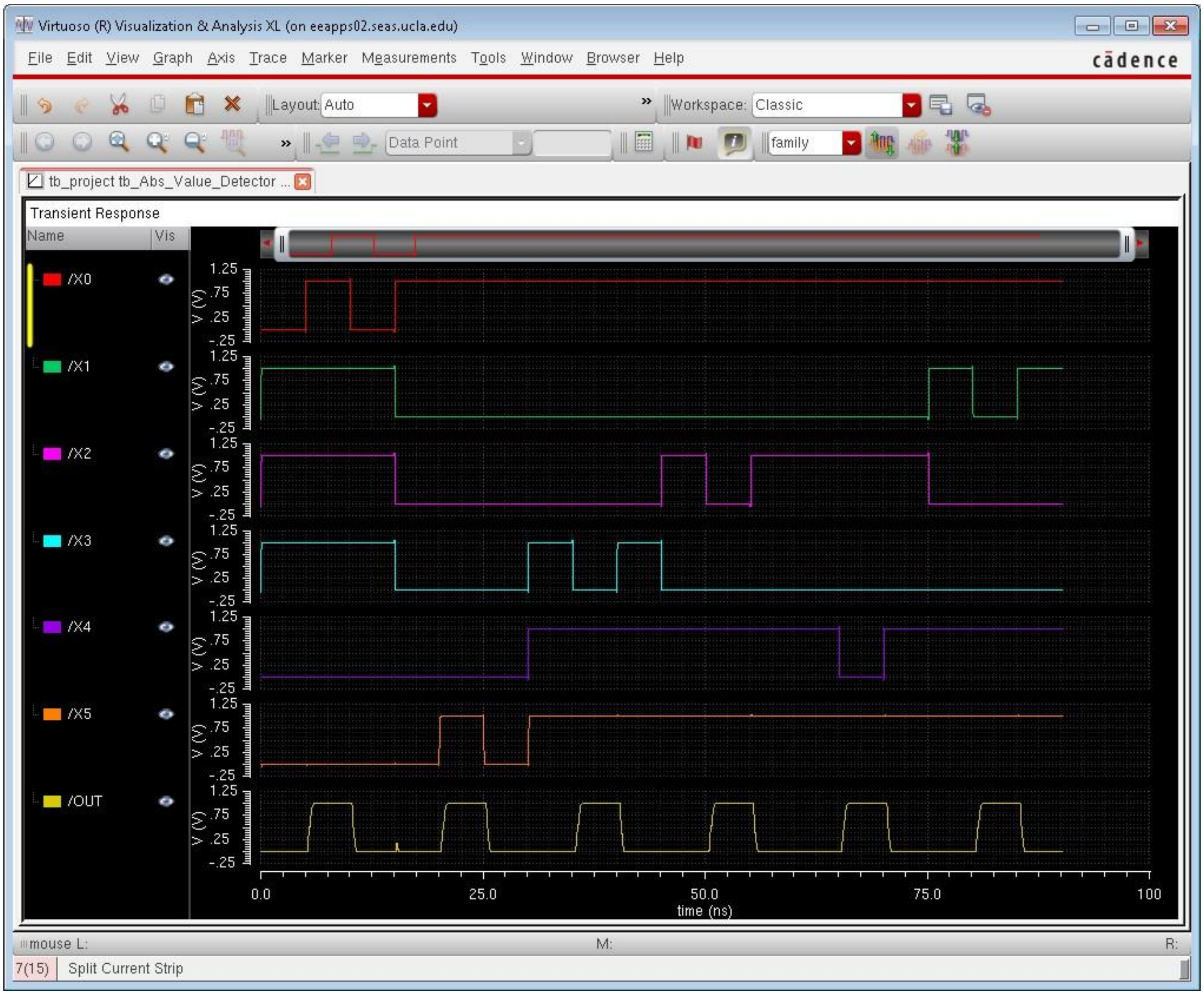
mouse L: M: R:

5(11) | Stimuli ... | Status: Ready | T=27 C | Simulator: spectre | State: spectre_state1

This shows the delay of this design from X_0, X_1, X_2, X_3, X_4 and X_5 to OUT. Energy Consumption in this example is 688.487fJ.

Delay is the average of t_{pLH} and t_{pLH} in each case (Maximum delay and maximum t_{pLH} or t_{pLH}, should all be less than 1ns). In the example shown above Delay_X3_OUT is the critical path.

Transient waveforms of X_0, X_1, X_2, X_3, X_4, X_5 and OUT are shown below:



While only a few input combinations are plotted here, you have to make sure that your design functions for all combinations (even the ones that are not tested in this testbench).

GOOD LUCK!