[Lab 6] Pipelined CPU

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Overview

In this assignment, we are going to implement a pipelined CPU and compare its performance to our previous CPU design, a multi-cycle CPU. In the pipelined design, each pipeline stage executes different instructions at a time. Hence, the output of each stage should be stored in its pipeline latch so that the next pipeline stage can use the output at the next clock cycle.

Goal

- Understand why pipelined CPUs show better performance than single- and multi-cycle CPUs.
- Understand what are the control/data hazards and how to resolve them.
- Design and implement a pipelined CPU.

Assignment Description

Implement a pipelined CPU. Your CPU must pass all provided test cases (see "cpu_tb.v"). Also, include the comparison to a multi-cycle CPU with respect to # of clock cycles. You are not allowed to add or delete ports declared in the skeleton code (see "cpu.v"), as always.

Grading

Functionality

We will grade your CPU module based on the pass/fail result of the provided testbench (see "cpu_tb.v"). The testbench contains most of the pass/fail tests that we will check, but we may add a few other pass/fail tests in grading.

Code review

- Your code should be easy to read. Otherwise, you may lose some points.
- Your code should include comments about your module's specifications.
  (i.e., what function does your module do? what is the purpose of an input/output?)
- Your code should avoid meaningless variable/parameter/file name.
  (e.g., "reg a", "wire wire1", "HelloWorld.v")
- Your code should stick to a consistent coding style.

Report

Basically, please refer to "How_to_write_your_report.pdf".

We'll follow the previous guideline for this week

Submission

Due: 05/08 (Mon.) 19:00 PM

- Late submission
  - 10% penalty per day until 05/13 (Sat.) 19:00 PM
  - NO points after 05/13 (Sat.) 19:00 PM

Upload a single zip file named Lab06_groupXX_20XX-XXXXX including your (1) project folder, (2) report on the eTL board.

- For example, if your student number is 2023-12345, and your group number is 67, submit Lab06_group67_2023-12345.zip
- Check "copy sources into project" option in "add or create design sources".
- **Make sure your Vivado project contains your source code.**
    - Check the Verilog files inside "[vivado_project_name].srcs/sources_1/new/" before submission.
- Do not delete files in the project folder if unnecessary. (e.g., .xpr file)