UCSC Extension – Digital Design with FPGA

Homework #7

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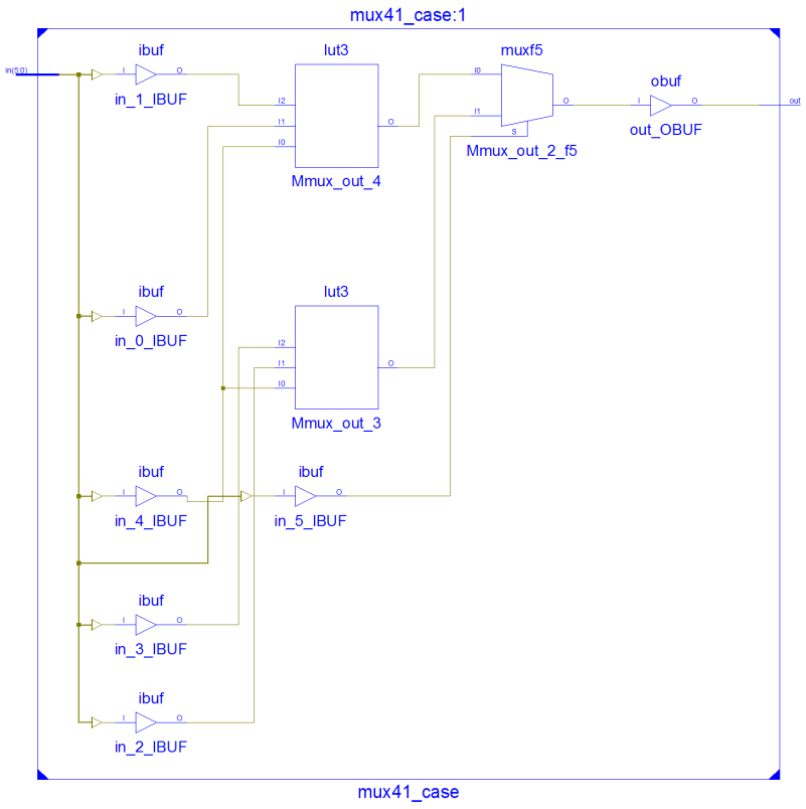
Problem 5.13.8 Implement 4:1 mux

a) Implement using only ‘case’ statement

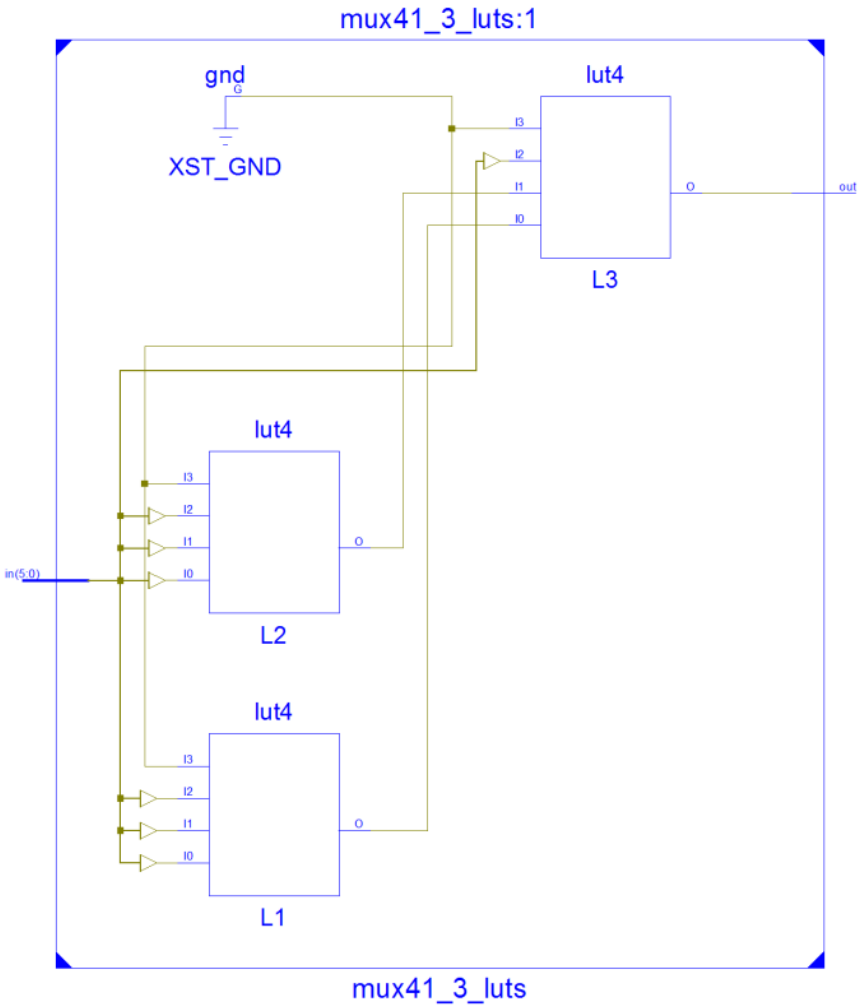
```
module mux41_case(in, out);
        parameter S = 2;                        //
        parameter N = 1 << S;           // # of cases
        input [N+S-1:0] in;
        output out;
        reg out;
        wire [S-1:0] sel;

        assign sel[1:0] = in[5:4];

        always @(*) begin
                case (sel)
                        2'b00: out = in[0];
                        2'b01: out = in[1];
                        2'b10: out = in[2];
                        2'b11: out = in[3];
                        default: out = 1'b0;
                endcase
        end
endmodule
```



```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : mux41_case.ngr
Top Level Output File Name         : mux41_case
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 7

Cell Usage :
# BELS                             : 3
#      LUT3                        : 2
#      MUXF5                       : 1
# IO Buffers                       : 7
#      IBUF                        : 6
#      OBUF                        : 1
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100ecp132-5

 Number of Slices:                        1  out of    960     0%
 Number of 4 input LUTs:                  2  out of   1920     0%
 Number of IOs:                           7
 Number of bonded IOBs:                   7  out of     83     8%

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 7 / 1
-------------------------------------------------------------------------
Delay:               6.054ns (Levels of Logic = 4)
  Source:            sel<0> (PAD)
  Destination:       out (PAD)

  Data Path: sel<0> to out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   1.106   0.532  sel_0_IBUF (sel_0_IBUF)
     LUT3:I0->O            1   0.612   0.000  Mmux_out_3 (Mmux_out_3)
     MUXF5:I1->O           1   0.278   0.357  Mmux_out_2_f5 (out_OBUF)
     OBUF:I->O                 3.169          out_OBUF (out)
    ----------------------------------------
    Total                      6.054ns (5.165ns logic, 0.889ns route)
                                       (85.3% logic, 14.7% route)

=========================================================================
```

b) Implement using only 3 LUTs (No MUXF5)

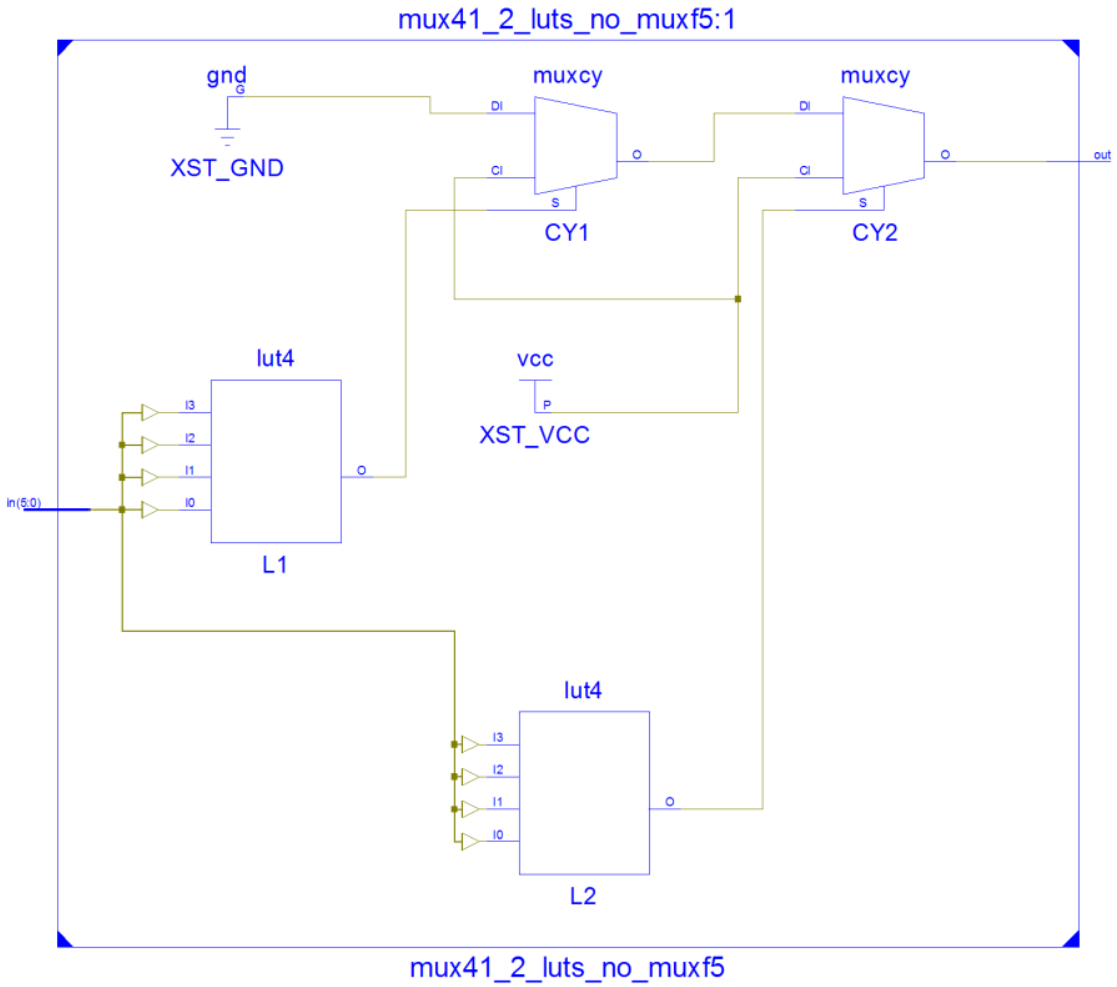
```
module mux41_3_luts(in, out);
        parameter S = 2;                        //
        parameter N = 1 << S;           // # of cases
        input [N+S-1:0] in;
        output out;
        wire [S-1:0] sel;
        wire l1, l2;

        assign sel[1:0] = in[5:4];

        LUT4 #(16'h00ca) L1(l1, in[0], in[1], sel[0], 1'b0);
        LUT4 #(16'h00ca) L2(l2, in[2], in[3], sel[0], 1'b0);
        LUT4 #(16'h00ca) L3(out, l1, l2, sel[1], 1'b0);

endmodule
```



```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : mux41_3_luts.ngr
Top Level Output File Name         : mux41_3_luts
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 7

Cell Usage :
# BELS                             : 4
#      GND                         : 1
#      LUT4                        : 3
# IO Buffers                       : 7
#      IBUF                        : 6
#      OBUF                        : 1
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100ecp132-5

 Number of Slices:                        2  out of    960     0%
 Number of 4 input LUTs:                  3  out of   1920     0%
 Number of IOs:                           7
 Number of bonded IOBs:                   7  out of     83     8%

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 7 / 1
-------------------------------------------------------------------------
Delay:               6.874ns (Levels of Logic = 4)
  Source:            in<0> (PAD)
  Destination:       out (PAD)

  Data Path: in<0> to out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.106   0.509  in_0_IBUF (in_0_IBUF)
     LUT4:I0->O            1   0.612   0.509  L1 (l1)
     LUT4:I0->O            1   0.612   0.357  L3 (out_OBUF)
     OBUF:I->O                 3.169          out_OBUF (out)
    ----------------------------------------
    Total                      6.874ns (5.499ns logic, 1.375ns route)
                                       (80.0% logic, 20.0% route)
```

c) Implement using only 2 LUTs (No MUXF5)

```
module mux41_2_luts_no_muxf5(in, out);
        parameter S = 2;                        //
        parameter N = 1 << S;           // # of cases
        input [N+S-1:0] in;
        output out;
        wire [S-1:0] sel;
        wire l1, l2, o1;

        assign sel[1:0] = in[5:4];

        LUT4 #(16'h00ca) L1(l1, in[0], in[1], sel[0], sel[1]);
        LUT4 #(16'hca00) L2(l2, in[2], in[3], sel[0], sel[1]);

        MUXCY CY1(o1, 1'b1, 1'b0, l1);
        MUXCY CY2(out, 1'b1, o1, l2);
endmodule
```

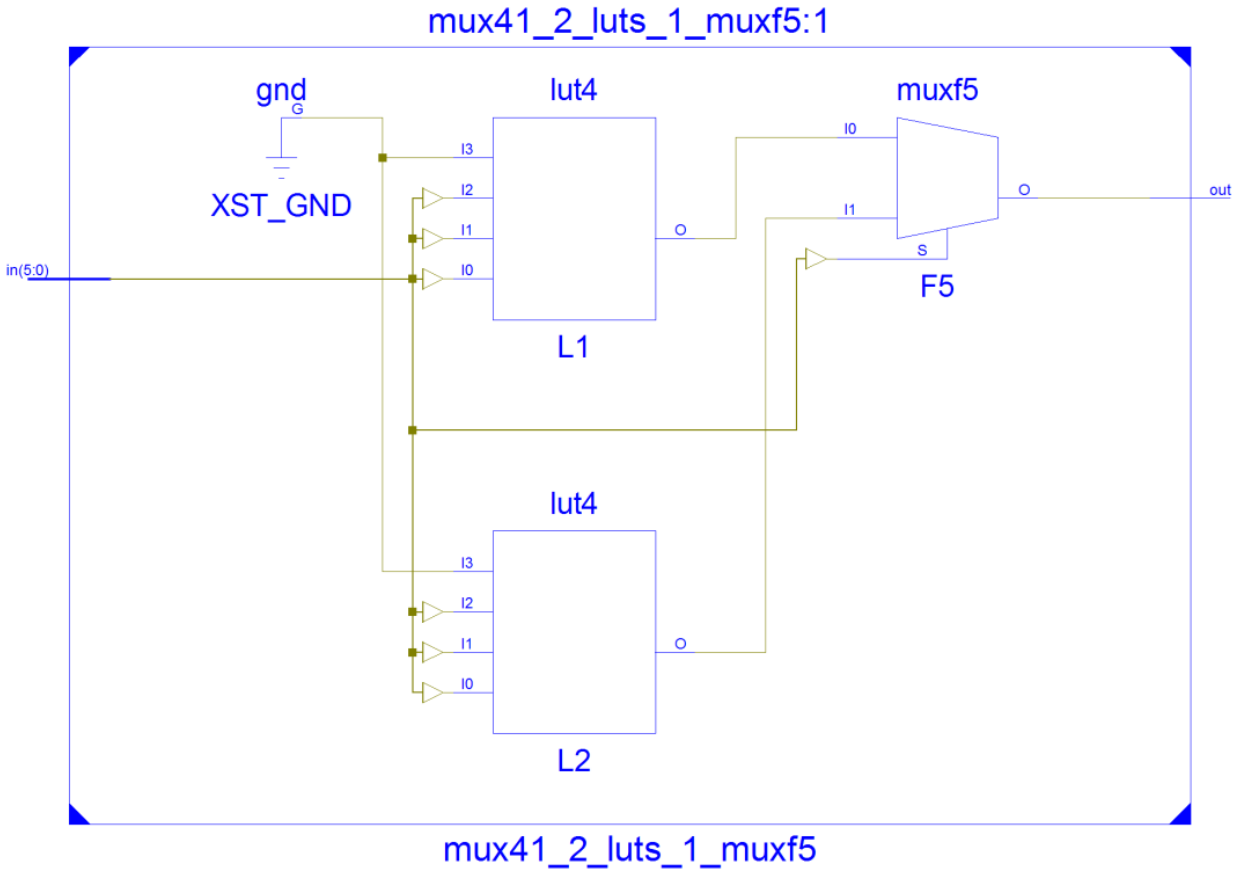


```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : mux41_2_luts_no_muxf5.ngr
Top Level Output File Name         : mux41_2_luts_no_muxf5
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 7

Cell Usage :
# BELS                             : 6
#      GND                         : 1
#      LUT4                        : 2
#      MUXCY                       : 2
#      VCC                         : 1
# IO Buffers                       : 7
#      IBUF                        : 6
#      OBUF                        : 1
=========================================================================

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 8 / 1
-------------------------------------------------------------------------
Delay:               7.626ns (Levels of Logic = 5)
  Source:            in<0> (PAD)
  Destination:       out (PAD)

  Data Path: in<0> to out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.106   0.509  in_0_IBUF (in_0_IBUF)
     LUT4:I0->O            1   0.612   0.000  L1 (l1)
     MUXCY:S->O            0   0.752   0.000  CY1 (o1)
     MUXCY:DI->O           1   1.121   0.357  CY2 (out_OBUF)
     OBUF:I->O                 3.169          out_OBUF (out)
    ----------------------------------------
    Total                      7.626ns (6.760ns logic, 0.866ns route)
                                       (88.6% logic, 11.4% route)
```

d) Implement using only 2 LUTs and one MUXF5

f = s1’s0’d0 + s1’s0d1 + s1s0’d2 + s1s0d3			
S1 == 0		S1 == 1	
S0’d0 + s0d1		S0’d2 + s0d3	
S0 == 0	S0 == 1	S0 == 0	S0 == 1
D0	D1	D2	D3

```
module mux41_2_luts_1_muxf5(in, out);
        parameter S = 2;                        //
        parameter N = 1 << S;           // # of cases
        input [N+S-1:0] in;
        output out;
        wire [S-1:0] sel;
        wire l1, l2;

        assign sel[1:0] = in[5:4];

        LUT4 #(16'h00ca) L1(l1, in[0], in[1], sel[0], 1'b0);
        LUT4 #(16'h00ca) L2(l2, in[2], in[3], sel[0], 1'b0);

        MUXF5 F5(out, l1, l2, sel[1]);
endmodule
```



```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : mux41_2_luts_1_muxf5.ngr
Top Level Output File Name         : mux41_2_luts_1_muxf5
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 7

Cell Usage :
# BELS                             : 4
#      GND                         : 1
#      LUT4                        : 2
#      MUXF5                       : 1
# IO Buffers                       : 7
#      IBUF                        : 6
#      OBUF                        : 1
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100ecp132-5

 Number of Slices:                        1  out of    960     0%
 Number of 4 input LUTs:                  2  out of   1920     0%
 Number of IOs:                           7
 Number of bonded IOBs:                   7  out of     83     8%

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 7 / 1
-------------------------------------------------------------------------
Delay:               6.031ns (Levels of Logic = 4)
  Source:            in<0> (PAD)
  Destination:       out (PAD)

  Data Path: in<0> to out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.106   0.509  in_0_IBUF (in_0_IBUF)
     LUT4:I0->O            1   0.612   0.000  L1 (l1)
     MUXF5:I0->O           1   0.278   0.357  F5 (out_OBUF)
     OBUF:I->O                 3.169          out_OBUF (out)
    ----------------------------------------
    Total                      6.031ns (5.165ns logic, 0.866ns route)
                                       (85.6% logic, 14.4% route)
```

TOP Module

```
module mux_top(CLK1, arst, seg, an, Led);
	parameter N = 7;
	parameter W = 4;
	parameter S = 8;
	parameter H = 14;		// binary size ..9999
	parameter MS = 2;		// mux sel
	parameter MN = 1 << MS;		// mux 4:1

	input CLK1, arst;
	output [0:N-1] seg;
	output [W-1:0] an;
	output [S-1:0] Led;

	wire [15:0] text, disp_text;
	wire one_sec;
	wire [S-1:0] num_sel;
	wire selected;
	wire selected1, selected2, selected3, selected4;

	assign Led = num_sel;
	assign selected = (selected1 == selected2 == selected3 == selected4);
	assign disp_text[3:0] = {3'b0, selected};
	assign disp_text[7:4] = 4'b0;
	assign disp_text[11:8] = text[3:0];
	assign disp_text[15:12] = text[7:4];

	one_second ONE (.CLK1(CLK1), .arst(arst), .one_sec_clock(one_sec));
	counter #(N-1) CNT (.clk(CLK1), .arst(arst), .en(one_sec), .q(num_sel));
	mux41_case #(.S(MS)) MUX4_1 (.in(num_sel), .out(selected1));
	mux41_3_luts #(.S(MS)) MUX4_2 (.in(num_sel), .out(selected2));
	mux41_2_luts_no_muxf5 #(.S(MS)) MUX4_3 (.in(num_sel), .out(selected3));
	mux41_2_luts_1_muxf5 #(.S(MS)) MUX4_4 (.in(num_sel), .out(selected4));
	bin2bcd #(H, W) BCD (.in(num_sel), .out(text));
	display T (.text(disp_text), .clk(CLK1), .arst(arst), .seg(seg), .an(an));

endmodule
```

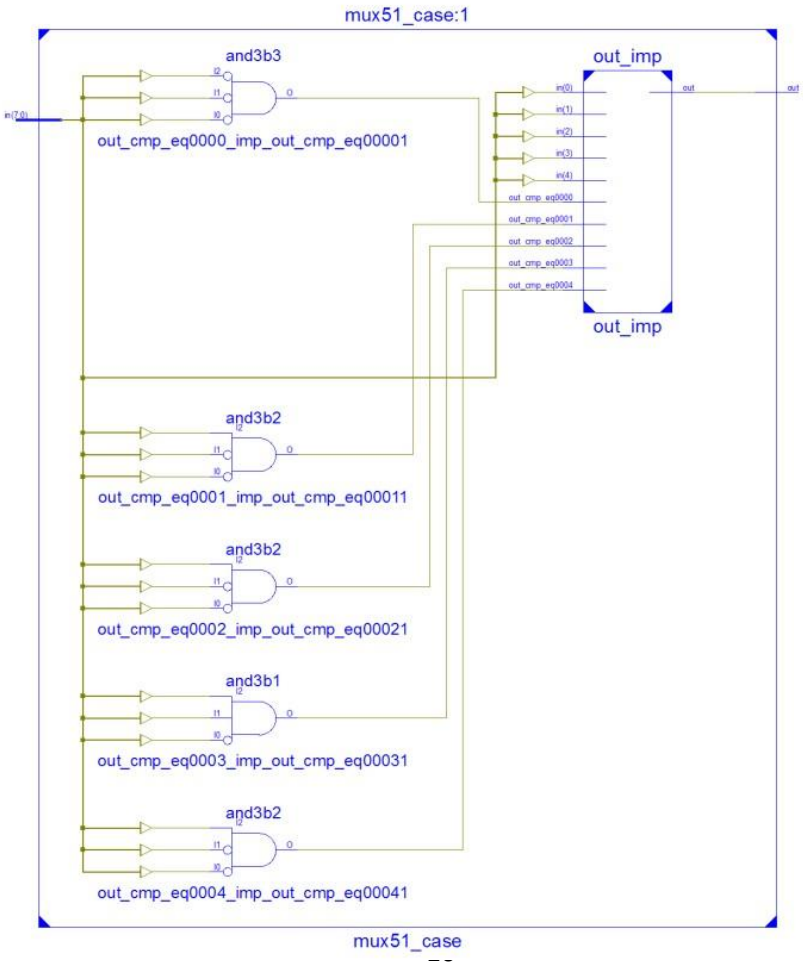
4:1 MUX Design Comparison Table

Design	# SLICEs	# LUTs	# MUXF5	# MUXCY	# LEVELs	DELAY
CASE	1	2	1	0	4	6.054 ns
3 LUT4	2	3	0	0	4	6.874 ns
2 LUT4, NO MUXF5	1	2	0	2	5	7.626 ns
2 LUT4, 1 MUXF5	1	2	1	0	4	6.031 ns

Problem 5.13.9 Implement 5:1 MUX

a) Implement using “case” statement

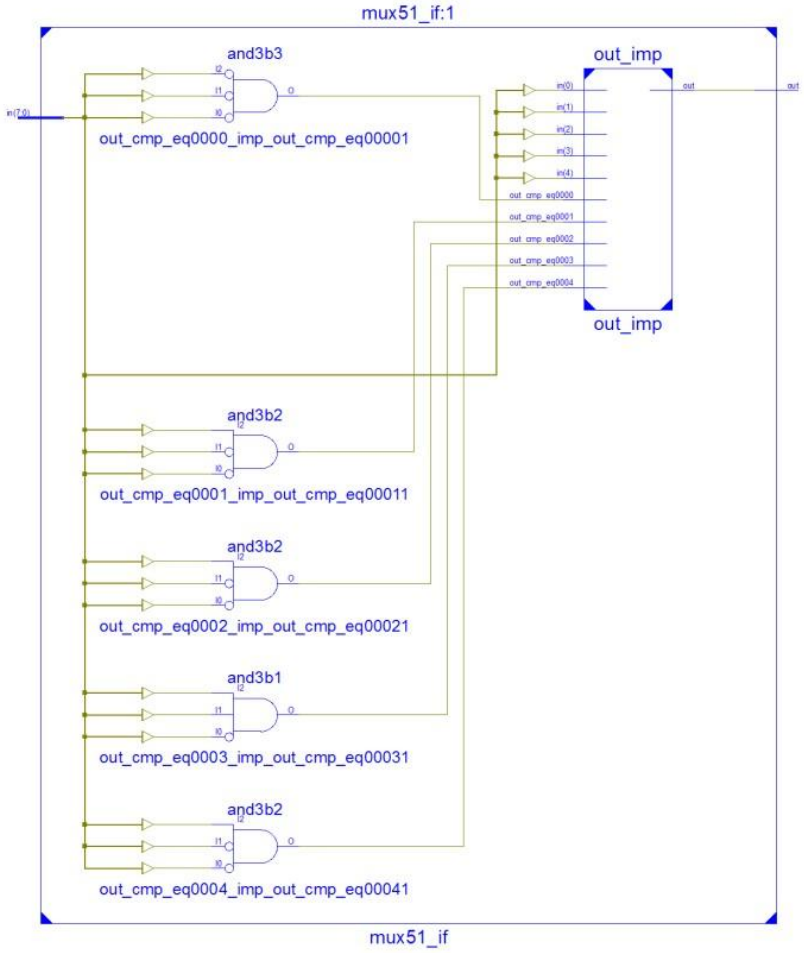
```
module mux51_case(in, out);
        parameter S = 3;                        //
        parameter N = 1 << S;          // # of cases
        input [N-1:0] in;
        output out;
        reg out;

        wire [S-1:0] sel;

        assign sel[2:0] = in[7:5];

        always @(*) begin
                case (sel)
                        3'b000: out = in[0];
                        3'b001: out = in[1];
                        3'b010: out = in[2];
                        3'b011: out = in[3];
                        3'b100: out = in[4];
                        default: out = 1'b0;
                endcase
        end
endmodule
```



```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : mux51_case.ngr
Top Level Output File Name         : mux51_case
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 9

Cell Usage :
# BELS                             : 4
#      LUT4                        : 4
# IO Buffers                       : 9
#      IBUF                        : 8
#      OBUF                        : 1
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100ecp132-5

 Number of Slices:                        2  out of    960     0%
 Number of 4 input LUTs:                  4  out of   1920     0%
 Number of IOs:                           9
 Number of bonded IOBs:                   9  out of     83    10%


=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 13 / 1
-------------------------------------------------------------------------
Delay:               6.968ns (Levels of Logic = 4)
  Source:            in<6> (PAD)
  Destination:       out (PAD)

  Data Path: in<6> to out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   1.106   0.603  in_6_IBUF (in_6_IBUF)
     LUT4:I0->O            1   0.612   0.509  out27 (out27)
     LUT4:I0->O            1   0.612   0.357  out69 (out_OBUF)
     OBUF:I->O                 3.169          out_OBUF (out)
    ----------------------------------------
    Total                      6.968ns (5.499ns logic, 1.469ns route)
                                       (78.9% logic, 21.1% route)
```

b) Implement using “if” statement

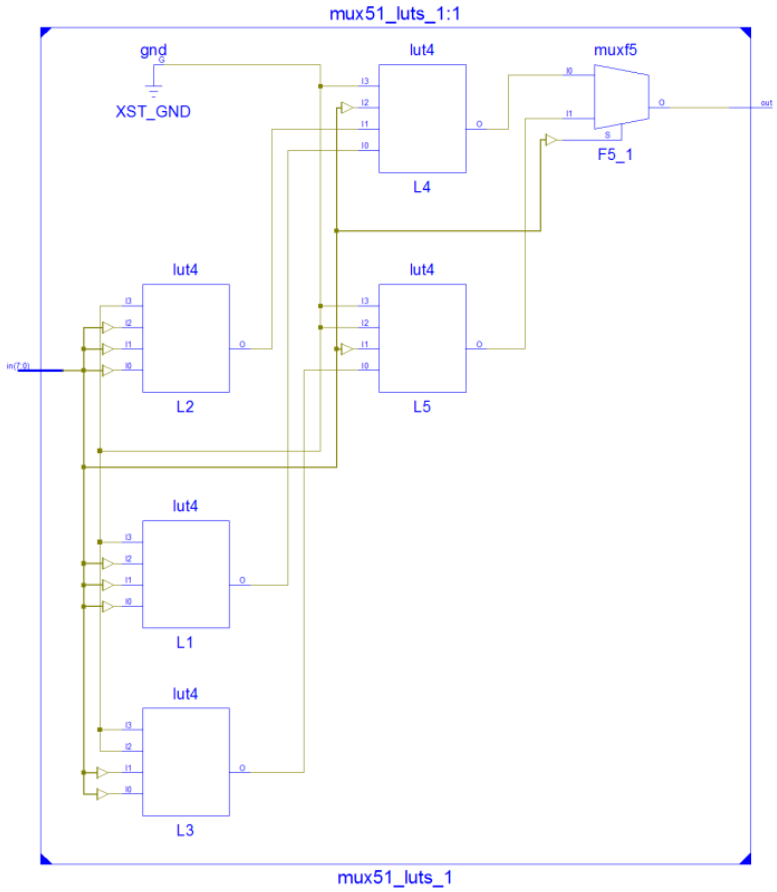
```
module mux51_if(in, out);
        parameter S = 3;                        //
        parameter N = 1 << S;           // # of cases
        input [N-1:0] in;
        output out;
        reg out;

        wire [S-1:0] sel;

        assign sel[2:0] = in[7:5];

        always @(*) begin
                out = (sel == 3'b000) ? in[0] :
                                        (sel == 3'b001) ? in[1] :
                                        (sel == 3'b010) ? in[2] :
                                        (sel == 3'b011) ? in[3] :
                                        (sel == 3'b100) ? in[4] : 1'b0;
        end
endmodule
```



```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : mux51_if.ngr
Top Level Output File Name         : mux51_if
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 9

Cell Usage :
# BELS                             : 4
#      LUT4                        : 4
# IO Buffers                       : 9
#      IBUF                        : 8
#      OBUF                        : 1
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100ecp132-5

 Number of Slices:                        2  out of    960     0%
 Number of 4 input LUTs:                  4  out of   1920     0%
 Number of IOs:                           9
 Number of bonded IOBs:                   9  out of     83    10%


=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 13 / 1
-------------------------------------------------------------------------
Delay:               6.968ns (Levels of Logic = 4)
  Source:            in<6> (PAD)
  Destination:       out (PAD)

  Data Path: in<6> to out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   1.106   0.603  in_6_IBUF (in_6_IBUF)
     LUT4:I0->O            1   0.612   0.509  out27 (out27)
     LUT4:I0->O            1   0.612   0.357  out69 (out_OBUF)
     OBUF:I->O                 3.169          out_OBUF (out)
    ----------------------------------------
    Total                      6.968ns (5.499ns logic, 1.469ns route)
                                       (78.9% logic, 21.1% route)
```

c) Implement using only Spartan3E primitives that requires 2 levels of logic

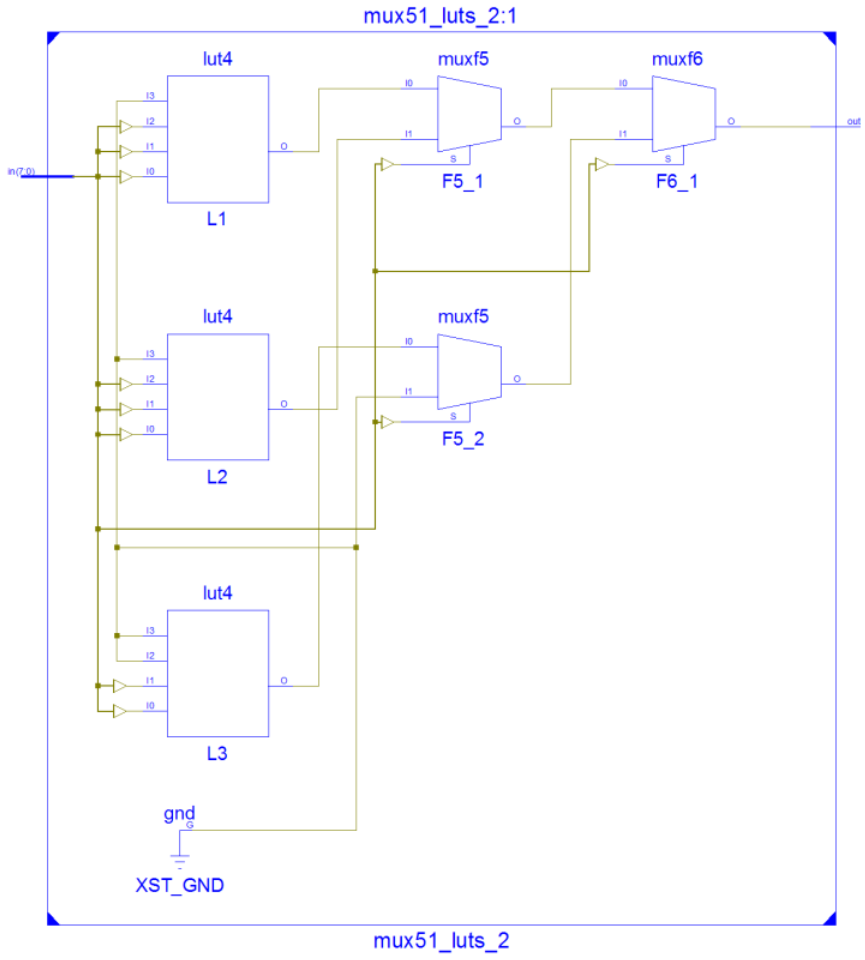
```
// 2 levels of logic
module mux51_luts_1(in, out);
        parameter S = 3;                        //
        parameter N = 1 << S;           // # of cases
        input [N-1:0] in;
        output out;

        wire [S-1:0] sel;
        wire l1, l2, l3, l4, l5;

        assign sel[2:0] = in[7:5];

        LUT4 #(16'h00ca) L1(l1, in[0], in[1], sel[0], 1'b0);
        LUT4 #(16'h00ca) L2(l2, in[2], in[3], sel[0], 1'b0);
        LUT4 #(16'h0002) L3(l3, in[4], sel[0], 1'b0, 1'b0);
        LUT4 #(16'h00ca) L4(l4, l1, l2, sel[1], 1'b0);
        LUT4 #(16'h0002) L5(l5, l3, sel[1], 1'b0, 1'b0);

        MUXF5 F5_1(out, l4, l5, sel[2]);

endmodule
```



```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : mux51_luts_1.ngr
Top Level Output File Name         : mux51_luts_1
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 12

Cell Usage :
# BELS                             : 7
#      GND                         : 1
#      LUT4                        : 5
#      MUXF5                       : 1
# IO Buffers                       : 9
#      IBUF                        : 8
#      OBUF                        : 1
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100ecp132-5

 Number of Slices:                        3  out of    960     0%
 Number of 4 input LUTs:                  5  out of   1920     0%
 Number of IOs:                           9
 Number of bonded IOBs:                   9  out of     83    10%



=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 11 / 1
-------------------------------------------------------------------------
Delay:               7.163ns (Levels of Logic = 5)
  Source:            sel<0> (PAD)
  Destination:       out (PAD)

  Data Path: sel<0> to out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   1.106   0.520  sel_0_IBUF (sel_0_IBUF)
     LUT4:I1->O            1   0.612   0.509  L3 (l3)
     LUT4:I0->O            1   0.612   0.000  L5 (l5)
     MUXF5:I1->O           1   0.278   0.357  F5_1 (out_OBUF)
     OBUF:I->O                 3.169          out_OBUF (out)
    ----------------------------------------
    Total                      7.163ns (5.777ns logic, 1.386ns route)
                                       (80.6% logic, 19.4% route)
```

d) Implement using only Spartan3E primitives that requires 1 level of logic

```
// 1 level of logic
module mux51_luts_2(in, out);
        parameter S = 3;                        //
        parameter N = 1 << S;           // # of cases
        input [N-1:0] in;
        output out;

        wire [S-1:0] sel;
        wire l1, l2, l3, l4, l5;

        assign sel[2:0] = in[7:5];

        LUT4 #(16'h00ca) L1(l1, in[0], in[1], sel[0], 1'b0);
        LUT4 #(16'h00ca) L2(l2, in[2], in[3], sel[0], 1'b0);
        LUT4 #(16'h0002) L3(l3, in[4], sel[0], 1'b0, 1'b0);
        MUXF5 F5_1(l4, l1, l2, sel[1]);
        MUXF5 F5_2(l5, l3, 1'b0, sel[1]);
        MUXF6 F6_1(out, l4, l5, sel[2]);

endmodule
```



```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : mux51_luts_2.ngr
Top Level Output File Name         : mux51_luts_2
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 12

Cell Usage :
# BELS                             : 7
#      GND                         : 1
#      LUT4                        : 3
#      MUXF5                       : 2
#      MUXF6                       : 1
# IO Buffers                       : 9
#      IBUF                        : 8
#      OBUF                        : 1
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100ecp132-5

 Number of Slices:                        2  out of    960     0%
 Number of 4 input LUTs:                  3  out of   1920     0%
 Number of IOs:                           9
 Number of bonded IOBs:                   9  out of     83    10%

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 11 / 1
-------------------------------------------------------------------------
Delay:               6.493ns (Levels of Logic = 5)
  Source:            sel<0> (PAD)
  Destination:       out (PAD)

  Data Path: sel<0> to out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   1.106   0.520  sel_0_IBUF (sel_0_IBUF)
     LUT4:I1->O            1   0.612   0.000  L3 (l3)
     MUXF5:I0->O           1   0.278   0.000  F5_2 (l5)
     MUXF6:I1->O           1   0.451   0.357  F6_1 (out_OBUF)
     OBUF:I->O                 3.169          out_OBUF (out)
    ----------------------------------------
    Total                      6.493ns (5.616ns logic, 0.877ns route)
                                       (86.5% logic, 13.5% route)
```

Top Module

```
module mux_top(CLK1, arst, seg, an, Led);
	parameter N = 7;
	parameter W = 4;
	parameter S = 8;
	parameter H = 14;		// binary size ..9999
	parameter MS = 3;		// mux sel
	parameter MN = 1 << MS;			// mux 5:1

	input CLK1, arst;
	output [0:N-1] seg;
	output [W-1:0] an;
	output [S-1:0] Led;

	wire [15:0] text, disp_text;
	wire one_sec;
	wire [S-1:0] num_sel;
	wire selected;
	wire selected1, selected2, selected3, selected4;

	assign Led = num_sel;
	assign selected = (selected1 == selected2 == selected3 == selected4);
	assign disp_text[3:0] = {3'b0, selected};
	assign disp_text[7:4] = text[3:0];
	assign disp_text[11:8] = text[7:4];
	assign disp_text[15:12] = text[11:8];

	one_second ONE (.CLK1(CLK1), .arst(arst), .one_sec_clock(one_sec));
	counter #(MN+MS) CNT (.clk(CLK1), .arst(arst), .en(one_sec), .q(num_sel));
	mux51_case #(.S(MS)) MUX5_1 (.in(num_sel), .out(selected1));
	mux51_if #(.S(MS)) MUX5_2 (.in(num_sel), .out(selected2));
	mux51_luts_1 #(.S(MS)) MUX5_3 (.in(num_sel), .out(selected3));
	mux51_luts_2 #(.S(MS)) MUX5_4 (.in(num_sel), .out(selected4));
	bin2bcd #(H, W) BCD (.in(num_sel), .out(text));
	display T (.text(disp_text), .clk(CLK1), .arst(arst), .seg(seg), .an(an));

endmodule
```

5:1 MUX Design Comparison Table

Design	# SLICEs	# LUTs	# MUXF5	# MUXF6	# LEVELs	DELAY
CASE	2	4	0	0	4	6.968 ns
IF	2	4	0	0	4	6.968 ns
2 Levels of Logic	3	5	1	0	5	7.163 ns
1 Levels of Logic	2	3	2	1	5	6.493 ns

Other modules

```
`timescale 1ns / 1ps
module mod_counter(clk, arst, q, done);
	parameter N = 7;
	parameter MAX = 127;

	input clk, arst;
	output [N-1:0] q;
	output done;
	reg [N-1:0] q;
	reg done;

	always @(posedge clk or posedge arst) begin
		if (arst == 1'b1) begin
			q <= 0;
			done <= 0;
		end
		else if (q == MAX) begin
			q <= 0;
			done <= 1;
		end
		else begin
			q <= q + 1;
			done <= 0;
		end
	end
endmodule

module one_second(CLK1, arst, one_sec_clock);
	parameter C = 26;   // counter,
	parameter CRYSTAL = 50;       // 50MHz
	parameter NUM_SEC = 1;
	parameter [C-1:0] STOPAT = ((CRYSTAL * 1_000_000 * NUM_SEC) - 1) >> 1;      // 0.5 sec

	input CLK1, arst;
	output one_sec_clock;
	wire [C-1:0] clock;

	mod_counter #(C, STOPAT) ONE_MC (.clk(CLK1), .arst(arst), .q(clock), .done(one_sec_clock));
endmodule

`timescale 1ns / 1ps

module bin2bcd(in, out);
	parameter N = 14;               // input size, decimal 9999 is hex 270f (14 bits)
	parameter C = 4;                // chunk size
	input [N-1:0] in;
	output [15:0] out;   // bcd output

	reg [N-1:0] bin;
	reg [N+3:0] bcd;
	reg [N+3:0] result;

	assign out = bcd[15:0];

	always @(*) begin
```

```
                bin = in;
                result = 0;

                repeat (N - 1) begin
                        result[0] = bin[N-1];
                        if (result[3:0] > 4)
                                result[3:0] = result[3:0] + 4'd3;
                        if (result[7:4] > 4)
                                result[7:4] = result[7:4] + 4'd3;
                        if (result[11:8] > 4)
                                result[11:8] = result[11:8] + 4'd3;
                        if (result[15:12] > 4)
                                result[15:12] = result[15:12] + 4'd3;

                        result = result << 1;
                        bin = bin << 1;
                end

                result[0] = bin[N-1];
                bcd <= result;
        end
endmodule

`timescale 1ns / 1ps

module counter(clk, arst, en, q);
        parameter N = 7;

        input clk, arst, en;
        output [N-1:0] q;
        reg [N-1:0] q;

        always @(posedge clk or posedge arst)
                if (arst == 1'b1)
                        q <= 0;
                else if (en)
                        q <= q + 1;
endmodule

module hex2_7seg_lut(in, out);
        input [3:0] in;
        output [6:0] out;

        LUT4 #(16'h2812) CA (out[6], in[0], in[1], in[2], in[3]);       // a
        LUT4 #(16'hd860) CB (out[5], in[0], in[1], in[2], in[3]);       // b
        LUT4 #(16'hd004) CC (out[4], in[0], in[1], in[2], in[3]);       // c
        LUT4 #(16'h8492) CD (out[3], in[0], in[1], in[2], in[3]);       // d
        LUT4 #(16'h02ba) CE (out[2], in[0], in[1], in[2], in[3]);       // e
        LUT4 #(16'h208e) CF (out[1], in[0], in[1], in[2], in[3]);       // f
        LUT4 #(16'h1083) CG (out[0], in[0], in[1], in[2], in[3]);       // g

endmodule

// for MUX4:1
module decoder(text, s, y, val) ;
        input [15:0] text;
        input [1:0] s ;
```

```
        output reg [3:0] y ;
        output reg [3:0] val ;

        always @(*) begin
                case (s)
                        0: begin
                                y <= 4'b1110 ;
                                val <= text[3:0] ;
                        end
                        1:begin
                                y <= 4'b1111;
                                val <= text[7:4] ;
                        end
                        2:begin
                                y <= 4'b1011 ;
                                val <= text[11:8] ;
                        end
                        3: begin
                                y <= 4'b0111 ;
                                val <= text[15:12] ;
                        end
                        default:begin
                                y <= 4'bx ;
                                val <= 4'bx ;
                        end
                endcase
        end
endmodule

// for MUX5:1
module decoder(text, s, y, val) ;
        input [15:0] text;
        input [1:0] s ;
        output reg [3:0] y ;
        output reg [3:0] val ;

        always @(*) begin
                case (s)
                        0: begin
                                y <= 4'b1110 ;
                                val <= text[3:0] ;
                        end
                        1:begin
                                y <= 4'b1101;
                                val <= text[7:4] ;
                        end
                        2:begin
                                y <= 4'b1011 ;
                                val <= text[11:8] ;
                        end
                        3: begin
                                y <= 4'b0111 ;
                                val <= text[15:12] ;
                        end
                        default:begin
                                y <= 4'bx ;
                                val <= 4'bx ;
```

```
                        end
                endcase
        end
endmodule

module display(text, clk, arst, seg, an);
        parameter C = 26;   // counter,
        parameter N = 7;    // seven segment
        parameter W = 4;
        parameter S = 2;
        parameter ANODE_FREQ = 19;

        input [15:0] text;
        input clk, arst;
        output [0:N-1] seg;
        output [W-1:0] an;

        wire [C-1:0] q;
        wire [S-1:0] sel;
        wire [W-1:0] zero_to_f_counter;

        assign sel[1] = q[ANODE_FREQ];
        assign sel[0] = q[ANODE_FREQ - 1];

        counter #C DISP_C (.clk(clk), .arst(arst), .en(1), .q(q));
        decoder DISP_D (.text(text), .s(sel), .y(an), .val(zero_to_f_counter));
        hex2_7seg_lut DISP_H (.in(zero_to_f_counter), .out(seg));

endmodule
```