**HW#3**

UCEC Extension – Digital Design using FPGA

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**Problem 3.7.4**

Implement and test the circuit shown in the 3.14

**Testing Switches and LEDs**

When SW7 is ON, LED7 must be ON. All other LEDs are OFF.

When SW7 is OFF and SW6 is ON, LED6 must be ON. All other LEDs are OFF.

When SW7, SW6 is OFF and SW5 is ON, LED5 must be ON. All other LEDs are OFF.

When SW7…SW1 is OFF and SW0 is ON, LED0 must be ON. All other LEDs are OFF.

1. What is the name of the circuit that you are designing?

**Priority Selector**

SW7 has the highest priority and SW0 has the lowest priority.

When higher priority SW is ON, lower priority SW is ignored.

1. See below design
2. 8 LUTs are required, but MUX and BUFFER are used in the design.
3. Design – below, 10 LUTs are required in the structural LUT design.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **SW (1 = ON, 0 = OFF, X = Don’t care)** | | | | | | | | **LED (1 = ON, 0 = OFF)** | | | | | | | |  |
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |  |
| 1 | X | X | X | X | X | X | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| 0 | 1 | X | X | X | X | X | X | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| 0 | 0 | 1 | X | X | X | X | X | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |  |
| 0 | 0 | 0 | 1 | X | X | X | X | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |  |
| 0 | 0 | 0 | 0 | 1 | X | X | X | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |  |
| 0 | 0 | 0 | 0 | 0 | 1 | X | X | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

LED7 = SW7

LED6 = SW7’ SW6

LED5 = SW7’ SW6’ SW5

LED4 = SW7’ SW6’ SW5’ SW4

LED3 = SW7’ SW6’ SW5’ SW4’ SW3

LED2 = SW7’ SW6’ SW5’ SW4’ SW3’ SW2

LED1 = SW7’ SW6’ SW5’ SW4’ SW3’ SW2’ SW1

LED0 = SW7’ SW6’ SW5’ SW4’ SW3’ SW2’ SW1’ SW0

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company: UCSC Extension-Digital Design using FPGA

// Engineer: Jae-Yang Park

//

// Create Date: 18:10:41 02/02/2014

// Design Name:

// Module Name: test\_sw

// Project Name:

// Target Devices:

// Tool versions:

// Description:

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//////////////////////////////////////////////////////////////////////////////////

module test\_sw(in, out);

input [7:0] in;

output [7:0] out;

reg [7:0] out;

always @(\*) begin

casex(in)

8'b1xxx\_xxxx: out = 8'b10000000;

8'b01xx\_xxxx: out = 8'b01000000;

8'b001x\_xxxx: out = 8'b00100000;

8'b0001\_xxxx: out = 8'b00010000;

8'b0000\_1xxx: out = 8'b00001000;

8'b0000\_01xx: out = 8'b00000100;

8'b0000\_001x: out = 8'b00000010;

8'b0000\_0001: out = 8'b00000001;

default: out = 8'b00000000;

endcase

end

endmodule

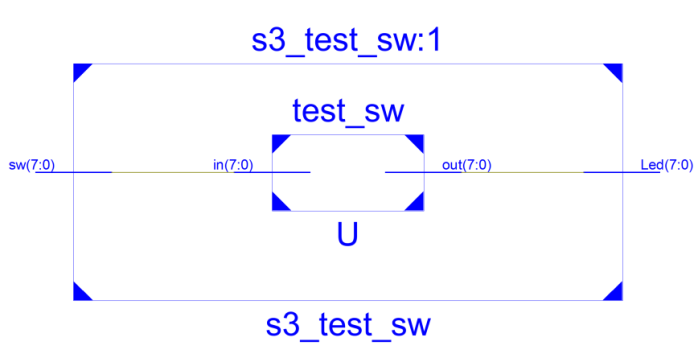
module s3\_test\_sw(sw, Led);

input [7:0] sw;

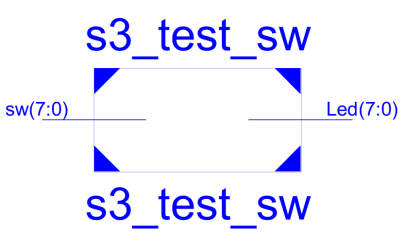
output [7:0] Led;

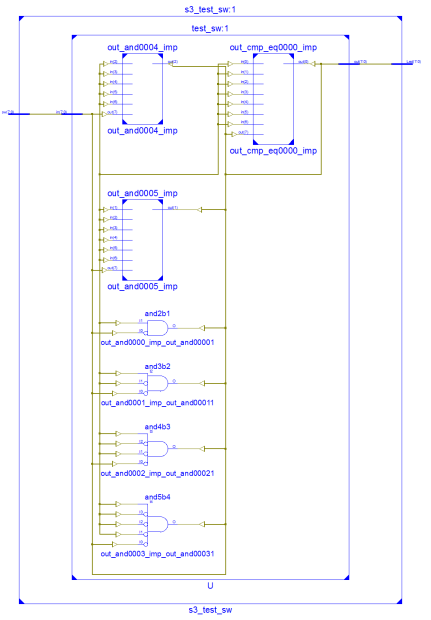
test\_sw U (.in(sw), .out(Led));

endmodule

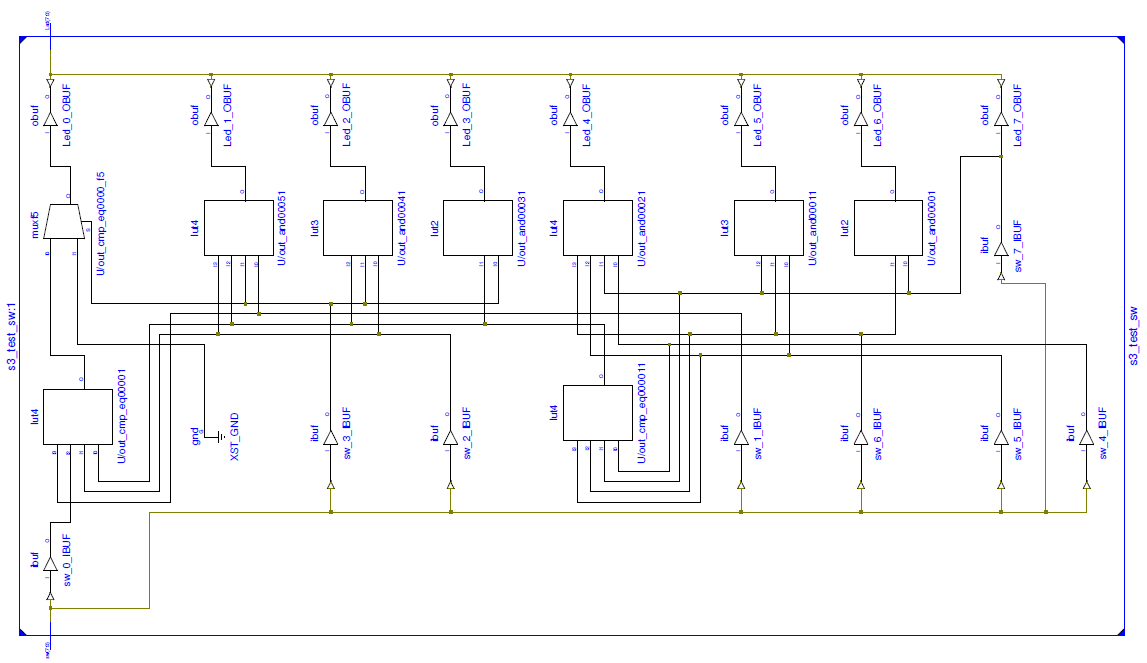
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**RTL Schematics**



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**Technology Schematics**

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**4. Structural Design using LUT**

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company: UCSC Extension-Digital Design using FPGA

// Engineer: Jae-Yang Park

//

// Create Date: 18:10:41 02/02/2014

// Design Name:

// Module Name: test\_sw

// Project Name:

// Target Devices:

// Tool versions:

// Description:

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//////////////////////////////////////////////////////////////////////////////////

module test\_sw\_lut(in, out);

input [7:0] in;

output [7:0] out;

wire out7654, out321;

LUT4 #(16'hFF00) U7 (out[7], in[4], in[5], in[6], in[7]);

LUT4 #(16'h00F0) U6 (out[6], in[4], in[5], in[6], in[7]);

LUT4 #(16'h000C) U5 (out[5], in[4], in[5], in[6], in[7]);

LUT4 #(16'h0002) U4 (out[4], in[4], in[5], in[6], in[7]);

LUT4 #(16'h0001) UG0 (out7654, in[4], in[5], in[6], in[7]);

LUT4 #(16'hF000) U3 (out[3], in[1], in[2], in[3], out7654);

LUT4 #(16'h0C00) U2 (out[2], in[1], in[2], in[3], out7654);

LUT4 #(16'h0200) U1 (out[1], in[1], in[2], in[3], out7654);

LUT4 #(16'h0001) UG1 (out321, in[1], in[2], in[3], 1'b0);

LUT4 #(16'h4000) U0 (out[0], 1'b0, in[0], out321, out7654);

Endmodule

module s3\_test\_sw\_lut(sw, Led);

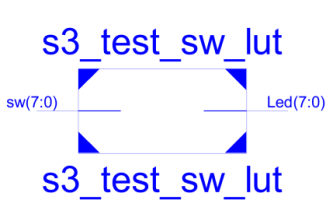
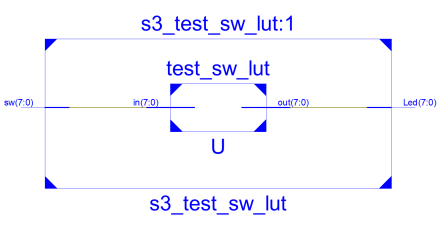
input [7:0] sw;

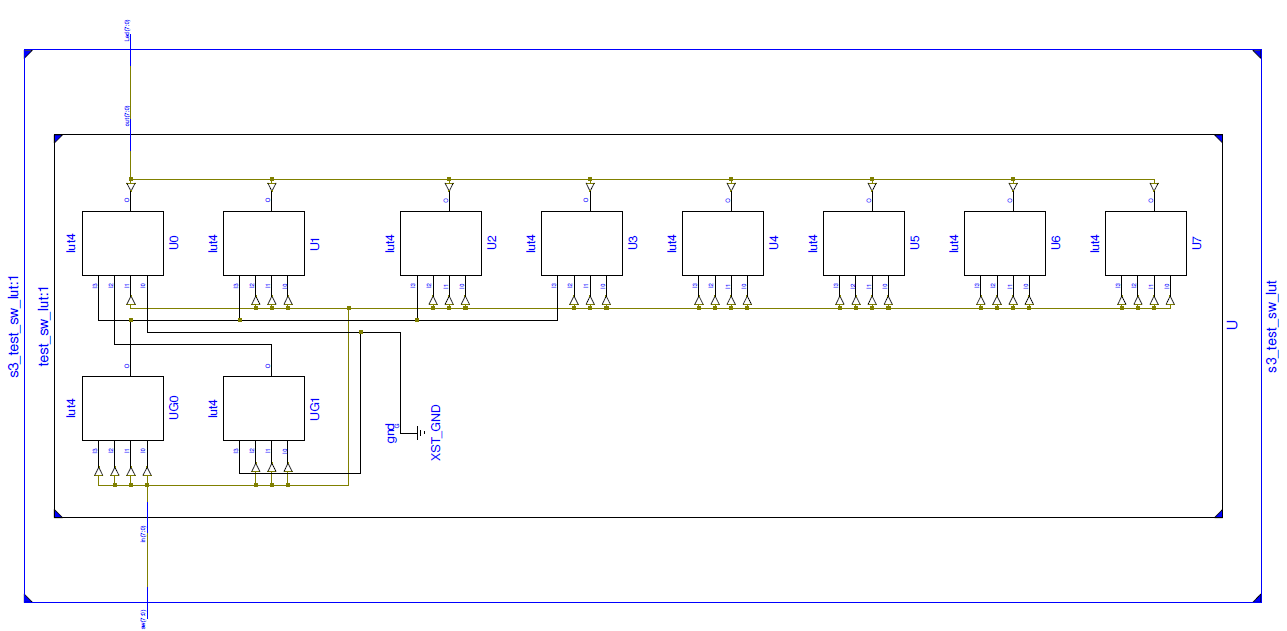
output [7:0] Led;

test\_sw\_lut U (.in(sw), .out(Led));

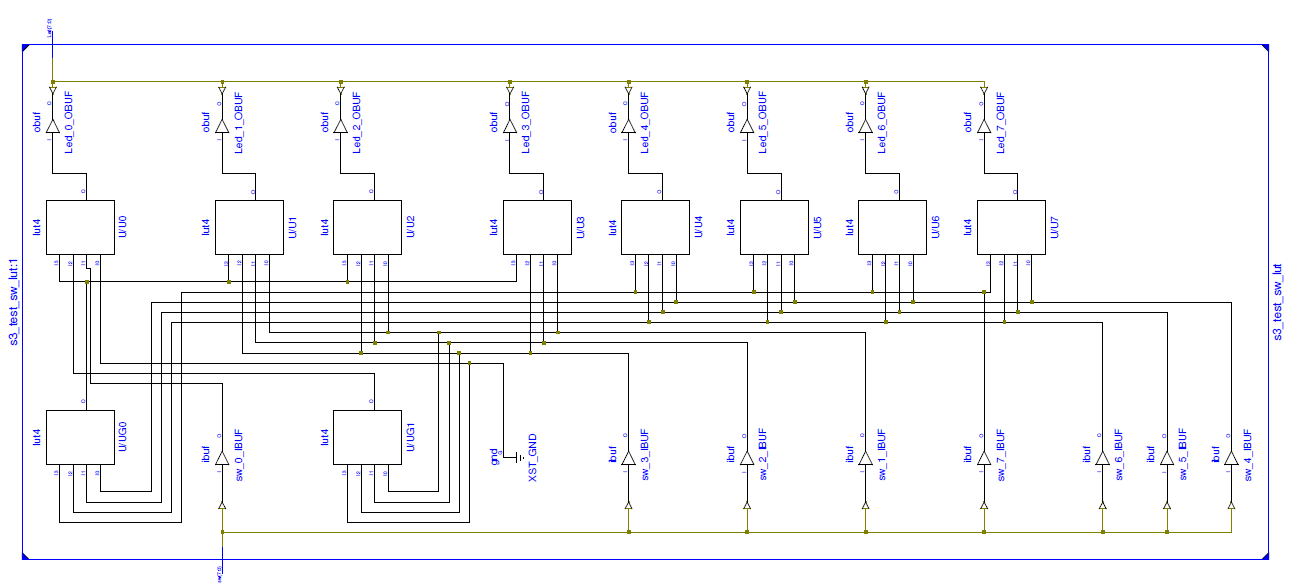
endmodule

RTL Schematics





**Technology Schematics**

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|  |  |
| --- | --- |
| **All Switchs are OFF** | **20140204_213718.jpg** |
| **SW7 is ON, LED7 is ON** | **20140204_213733.jpg** |
| **SW7 OFF, SW6 ON, LED6 ON** | **20140204_213741.jpg** |
| **SW7 OFF, SW6 OFF, SW5 ON**  **LED5 ON** | **20140204_213800.jpg** |
| **SW7..SW1 OFF, SW0 ON**  **LED0 ON** | **20140204_213816.jpg** |
| **SW7 ON, SW6 ON**  **LED7 ON**   * **SW7 has higher priority than SW6** | **20140204_213831.jpg** |
| **SW6 ON, SW5 ON**  **LED6 ON**   * **SW6 has higher priority than SW6** | **20140204_213844.jpg** |
| **SW5..SW0 ON**  **LED5 ON**   * **SW5 has the highest priority** | **20140204_213904.jpg** |

**Problem 3.7.5**

Implement the module hex2\_7seg.v using structural Verilog. You should use only LUTs in your Verilog file. Use the module s3\_hex2\_7seg as is.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| SW (0 = OFF, 1 = ON) | | | | 7 SEGMENT (0 = ON, 1 = OFF) | | | | | | |  |
| SW3 | SW2 | SW1 | SW0 | a | b | c | d | e | f | g | Display |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 3 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 5 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 6 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 9 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | A |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | B |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | C |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | d |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | E |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | F |
| LUTMASK | | | | **2812** | **D860** | **D004** | **8492** | **02BA** | **208E** | **1083** |  |

Code:

`timescale 1ns / 1ps

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// Company: UCSC Extension - Digital Design using FPGA

// Engineer: Jae-Yang Park

//

// Create Date: 18:53:04 02/03/2014

// Design Name:

// Module Name: hex2\_7seg\_lut

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

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module hex2\_7seg\_lut(in, out);

input [3:0] in;

output [6:0] out;

LUT4 #(16'h2812) CA (out[6], in[0], in[1], in[2], in[3]); // a

LUT4 #(16'hd860) CB (out[5], in[0], in[1], in[2], in[3]); // b

LUT4 #(16'hd004) CC (out[4], in[0], in[1], in[2], in[3]); // c

LUT4 #(16'h8492) CD (out[3], in[0], in[1], in[2], in[3]); // d

LUT4 #(16'h02ba) CE (out[2], in[0], in[1], in[2], in[3]); // e

LUT4 #(16'h208e) CF (out[1], in[0], in[1], in[2], in[3]); // f

LUT4 #(16'h1083) CG (out[0], in[0], in[1], in[2], in[3]); // g

endmodule

module s3\_hex2\_7seg(sw, seg, an);

input [3:0] sw;

output [0:6] seg;

output [3:0] an;

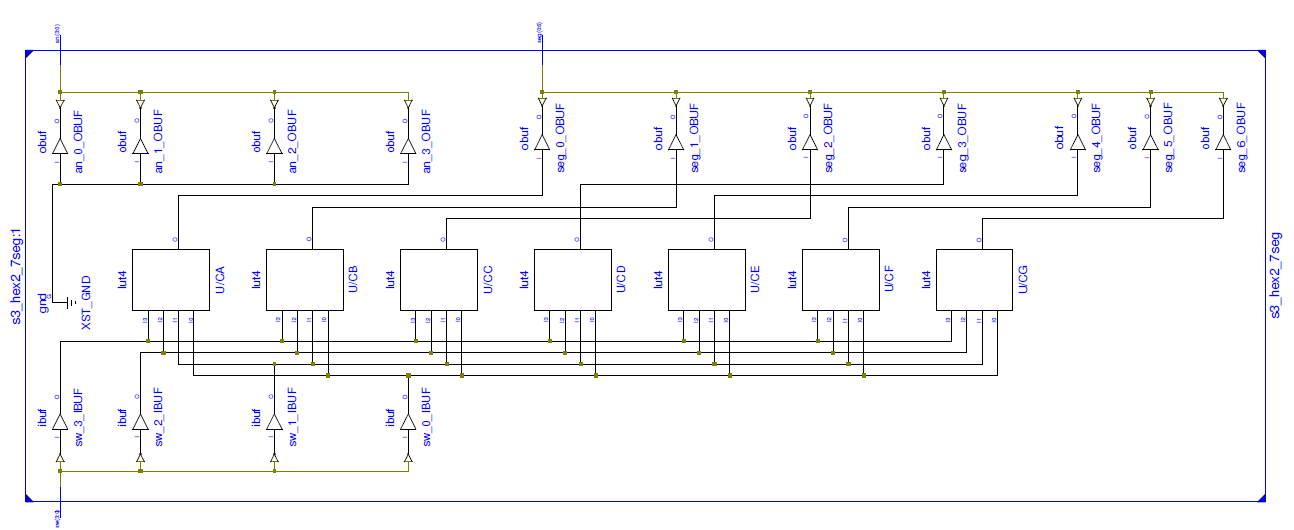
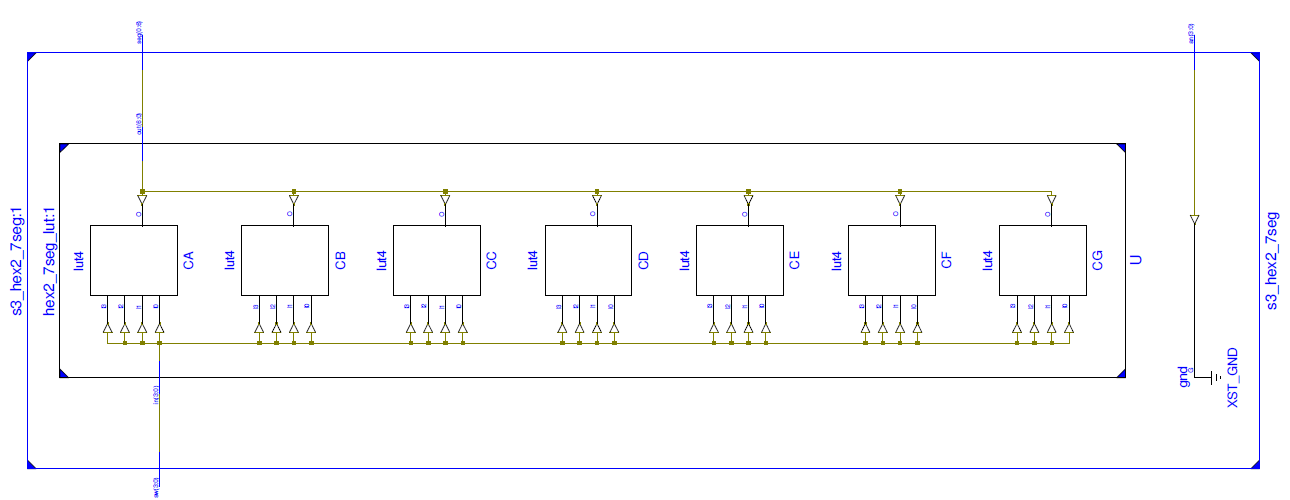
assign an = 4'b0000;

hex2\_7seg\_lut U(.in(sw), .out(seg));

endmodule

|  |  |  |
| --- | --- | --- |
|  |  |  |

**RTL Schematics**



Technology Schematics

ON = 1, OFF = 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| SW3 | SW2 | SW1 | SW0 | DISPLAY |
| 0 | 0 | 0 | 0 | 20140203_221610.jpg |
| 0 | 0 | 0 | 1 | 20140203_221634.jpg |
| 0 | 0 | 1 | 0 | 20140203_221644.jpg |
| 0 | 0 | 1 | 1 | 20140203_221750.jpg |
| 0 | 1 | 0 | 0 | 20140203_221758.jpg |
| 0 | 1 | 0 | 1 | 20140203_221805.jpg |
| 0 | 1 | 1 | 0 | 20140203_221813.jpg |
| 0 | 1 | 1 | 1 | 20140203_221819.jpg |
| 1 | 0 | 0 | 0 | 20140203_221827.jpg |
| 1 | 0 | 0 | 1 | 20140203_221832.jpg |
| 1 | 0 | 1 | 0 | 20140203_221838.jpg |
| 1 | 0 | 1 | 1 | 20140203_221847.jpg |
| 1 | 1 | 0 | 0 | 20140203_221901.jpg |
| 1 | 1 | 0 | 1 | 20140203_221906.jpg |
| 1 | 1 | 1 | 0 | 20140203_221912.jpg |
| 1 | 1 | 1 | 1 | 20140203_221921.jpg |