Digital Signal Processing Concepts

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Abstract

Within the last few years, digital techniques have been extensively applied to the solution of signal processing problems. This paper briefly examines the relative merits of analog and digital signal processing techniques and then considers the conceptual issues involved in formulating the solution to a signal processing problem as a digital signal processor. Issues considered are the representation of a digital processor by a difference equation, formal solution of the difference equation, the system function corresponding to the processor, as well as the frequency response of the system.

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Introduction

Over the last few years we have seen considerable growth in the application of digital techniques to signal processing problems. The obvious question is why? What are the advantages of using digital techniques to process signals? Let us enumerate some of these advantages by considering several examples of digital signal processors. Two years ago, Jackson, Kaiser, and McDonald [1] described techniques for implementing digital filters with a small set of simple, modular digital circuits well suited for LSI implementation. These digital circuits are easily configured to realize different filter forms, parameter accuracies, and arithmetic error levels. Also, filters constructed from these building blocks can be effectively multiplexed in time to process multiple input data sequences with one filter or to process a single data sequence with multiple filters, thus achieving a high level of component utilization.

The staff of the Bell Telephone Laboratories used these techniques to realize an experimental, digital version of the touch-tone receiver. The receiver is a straightforward digital implementation of the analog system [2] and incorporates a total of twenty-one filters (three third-order high-pass filters, two sixth-order band-rejection filters, eight second-order bandpass filters, and eight first-order low-pass filters) in addition to the logic circuitry needed to provide multiplexing control. Implementation of these filters required approximately 400 bits of shift-register-storage and 40 serial adders—less than, say, twenty LSI packages in terms of today's technology. The digital touch-tone receiver occupies about 6 in of rack space including the control circuitry and the power supply (which could power several receivers). The analog receiver occupies a considerably larger section of rack space.

Freeney [3] has used these same digital techniques to realize the filters required for an all digital frequency division multiplex terminal. These digital filters occupy two printed circuit boards with the entire digital receiver, including power supply and multiplexing logic, occupying less than 2 ft of rack space compared to 24 ft of rack space for the equivalent analog terminal.

In addition to occupying less space, present-day economics are such that digital systems such as these cost approximately the same as their analog equivalents. And, the current economic trends are for analog components and systems to increase in cost while digital components and systems decrease.

Another somewhat different example of digital signal processing is reported by Alter [4]. In his development of a system for graded bioelectric control of an elbow prosthesis, Alter used a digital processor to process electromyographic signals obtained from surface electrodes on the biceps and triceps of an amputee's arm. The signal processor's output was used to control a small electric motor which flexed the "elbow" of the prosthesis. Alter chose a digital processor instead of an equivalent analog processor because the digital processor provided greater

flexibility in changing the processing algorithms as well as changing the parameters which define the process and permitted a more exact specification of nonlinear functions as well as their evaluation.

These two examples illustrate several of the advantages of using digital signal processors. But what of the analog processor? Will analog processors become as obsolete as the vacuum tube? Perhaps, but not in the near future. In order for a digital processor to have an economic advantage, its processing capabilities must be fully utilized. This implies that the processor must be above a minimum critical size. Thus, analog systems can be expected to continue to have an economic advantage when the overall system is below this critical size. The critical size depends primarily upon the complexity of the processing algorithm, which in the digital system, involves both the number of poles and zeros in the system as well as the number of samples to be processed each second and the number of bits contained in each sample. Other areas where analog systems will continue to play important roles are in systems which interface transducers with signal processors and in high frequency (say, above 25 MHz) applications.

In the following sections of this paper, the basic concepts of digital signal processing are presented. First, what are the elements of a digital signal processor and how are these elements interconnected to form processors?

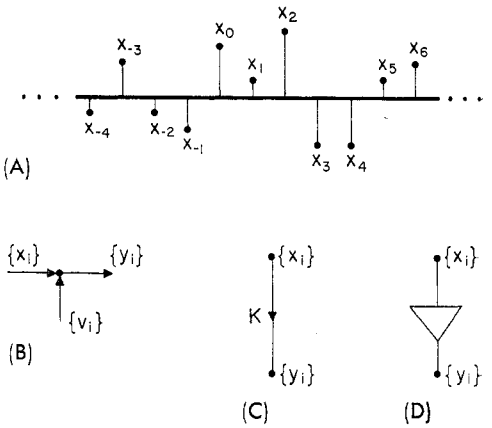
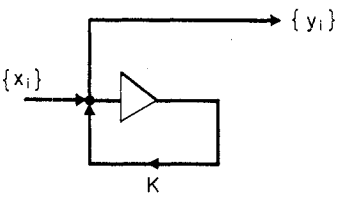


Fig. 1. Example of a sequence and the three basic elements. (A) Sequence $\{x_i\} - \infty < i < \infty$. (B) Adder $y_i = x_i + v_i$. (C) Multiplier $y_i = Kx_i$. (D) Unit-delay $y_i = x_{i-1}$.

Fig. 2. Simple recursive processor.



Elements and Simple Interconnections

Digital signal processors are formed by the interconnection of three basic types of elements: the adder, the multiplier, and the unit-delay. The input to and the output from each of these elements is a sequence of numbers

$$\{x_i\} \qquad -\infty < i < \infty$$

where the subscript i enumerates the various members of the sequence. Fig. 1 pictures a typical sequence and these three basic elements. Assuming that

$$\{x_i\} \qquad -\infty < i < \infty$$

and

$$\{v_i\} \qquad -\infty < i < \infty$$

are the input sequences to the adder, then the adder's output sequence

$$\{y_i\} \qquad -\infty < i < \infty$$

will have members given by

$$y_i = x_i + v_i \qquad -\infty < i < \infty. \tag{1}$$

In the case of the multiplier, if

$$\{x_i\} \qquad -\infty < i < \infty$$

is the input sequence and

$$\{y_i\} \qquad -\infty < i < \infty$$

is the output sequence, the input–output characteristic is

$$y_i = Kx_i \qquad -\infty < i < \infty \tag{2}$$

where K is the constant associated with the multiplier element. For the unit-delay element, if

$$\{x_i\} \qquad -\infty < i < \infty$$

is the input sequence and

$$\{y_i\} \qquad -\infty < i < \infty$$

is the output sequence, the input–output characteristic is

$$y_i = x_{i-1} \qquad -\infty < i < \infty. \tag{3}$$

Having defined each of the elements, let us now connect them into a simple processor. The processor shown in Fig. 2 contains one adder, one multiplier, and one unit-delay element and is the simplest member of the class of digital processors known as recursive (or feedback) processors. From the figure, we see that the present output of the processor is delayed one unit of time by the unit-delay element, multiplied by a constant, and added to the next input in order to generate the next output. Thus, the input–output characteristic of this processor is specified by the equation

$$y_i = x_i + Ky_{i-1} \qquad -\infty < i < \infty \tag{4}$$

or

$$y_i - Ky_{i-1} = x_i \qquad -\infty < i < \infty. \tag{5}$$

Equation (5) is known as a first-order linear constant-coefficient difference equation.

Before proceeding to a more complex processor or to general techniques for solving equations such as (5) let us attempt to gain insight into digital signal processors by considering a numerical example. Consider the processor shown in Fig. 2 and let the input sequence $\{x_i\}$ be defined as

$$x_i = {}_0u_i \qquad -\infty < i < \infty. \tag{6}$$

The sequence

$$\{{}_0u_i\} \qquad -\infty < i < \infty$$

is a special sequence defined by the relation

$${}_0u_i = \begin{cases} 1 & i = 0 \\ 0 & i \neq 0 \end{cases} \qquad -\infty < i < \infty \tag{7}$$

and known as the unit-sample sequence. Let us assume that the processor is at rest (that is, that the signals at each of the connection points within the processor are zero) when the input sequence is applied. Then, from (4), (6), and (7) we see that

$$y_i = 0 \qquad -\infty < i < 0$$

and that

$$\begin{aligned} y_0 &= x_0 + Ky_{-1} = 1 \\ y_1 &= x_1 + Ky_0 = K \\ y_2 &= x_2 + Ky_1 = K^2 \\ y_3 &= x_3 + Ky_2 = K^3 \\ &\vdots \end{aligned}$$

or

$$y_i = K^i \qquad i \geq 0. \tag{8}$$

In Fig. 3 the input and output sequences are shown for $K=0.8$. The response which we have seen here has a parallel in analog processors in the current response of a series *RL* circuit to an impulse of voltage.

Now, let us consider a more complex processor. Fig. 4 pictures a digital signal processor with two feedback and two feedforward paths. Referring to the figure, we see that y_i can be written in parametric form as

$$y_i = b_0\lambda_i + b_1\lambda_{i-1} \qquad -\infty < i < \infty. \tag{9}$$

But,

$$\lambda_i = x_i - a_1\lambda_{i-1} - a_2\lambda_{i-2} \qquad -\infty < i < \infty. \tag{10}$$

Substituting (10) into (9) and rearranging the terms, we have

$$\begin{aligned} y_i = {} & b_0x_i + b_1x_{i-1} - a_1[b_0\lambda_{i-1} + b_1\lambda_{i-2}] \\ & -a_2[b_0\lambda_{i-2} + b_1\lambda_{i-3}] \qquad -\infty < i < \infty. \end{aligned} \tag{11}$$

The terms within the brackets are identified, by referring to (9), as y_{i-1} and y_{i-2} respectively. Therefore (11) becomes

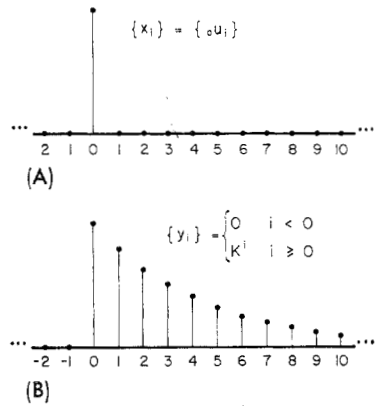
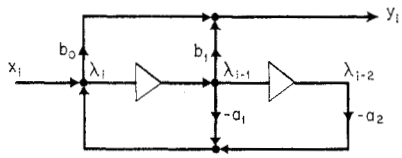


Fig. 3. Graphical representation of the input and output sequences for the processor of Fig. 2. (A) Input sequence. (B) Output sequence, $K=0.8$.

Fig. 4. Processor with both feedback and feedforward paths.



$$y_i = b_0x_i + b_1x_{i-1} - a_1y_{i-1} - a_2y_{i-2}$$

or, as it is usually written,

$$y_i + a_1y_{i-1} + a_2y_{i-2} = b_0x_i + b_1x_{i-1} \qquad -\infty < i < \infty. \tag{12}$$

This equation is known as a second-order linear constant-coefficient difference equation.

Before we develop a procedure for solving equations such as (12) let us take a brief detour to consider a special class of input signals.

Eigenfunctions and Eigenvalues

The key to the description of linear digital processors and their signals is to recognize that if

$$\{{}_k\xi_i\} \qquad -\infty < i < \infty; \quad k = 0, 1, \cdots, N-1$$

is a set of N input sequences yielding known response sequences

$$\{{}_k\eta_i\} = F[\{{}_k\xi_i\}] \qquad k = 0, 1, \cdots, N-1 \tag{13}$$

then any input sequence $\{x_i\}$ that can be represented as a weighted sum of the sequences $\{{}_k\xi_i\}$; that is,

$$\{x_i\} = \sum_{k=0}^{N-1} \alpha_k\{{}_k\xi_i\}; \tag{14}$$

will produce the response sequence

$$\{y_i\} = F[\{x_i\}] = \sum_{k=0}^{N-1} \alpha_k \{{}_k\eta_i\}. \quad (15)$$

(In (13) and (15), $F[\ ]$ indicates the operation performed on the input sequence by the processor to yield the output sequence.) Thus, the principal problem in describing linear digital processors is to choose the set of sequences $\{{}_k\xi_i\}$ in order that the number of sequences $\{x_i\}$ which can be represented by (14) is as large as possible and in order for the description of the sets $\{{}_k\xi_i\}$ and $\{{}_k\eta_i\}$ to be as simple as possible.

There are many possible choices for the set of sequences $\{{}_k\xi_i\}$. One of the more obvious is the set of delayed unit-sample sequences,

$${}_0u_{k-i} = \begin{cases} 1 & k = i \\ 0 & k \neq i. \end{cases} \quad (16)$$

However, there is a special set of functions for every linear (not necessarily time-invariant) digital processor called eigenfunctions which greatly simplify our analysis. Eigenfunctions have the property that if $\{{}_k\xi_i\}$ is an eigenfunction of $F[\ ]$ then

$$\{{}_k\eta_i\} = F[\{{}_k\xi_i\}] = \mu_k\{{}_k\xi_i\} \quad (17)$$

where the μ_k are constants called eigenvalues. Thus, for these special input sequences, the output sequence is identically the same sequence as the input except for a multiplying constant. In general, the set of sequences $\{{}_k\xi_i\}$ which satisfy (17) depends upon the detailed properties of the processor $F[\ ]$. However, if the system is time-invariant as well as linear, then the eigenfunctions are almost totally independent of the specific nature of the system—the eigenfunctions of every linear time-invariant digital processor are functions of the form

$$z_p{}^i \qquad -\infty < i < \infty$$

where z_p is a complex number having the attributes of frequency. Different values of z_p yield different eigenfunctions.

Now, let us prove our assertion that functions of the form $z_p{}^i$ are eigenfunctions of linear time-invariant digital systems. The argument which we present is parallel to Wiener's argument [5] for continuous systems (in which he shows that e^{st} is an eigenfunction of these systems):

1) Let the processor's input be the sequence

$$\{x_i\} = \{z_p{}^i\} \qquad -\infty < i < \infty. \quad (18)$$

We seek to show that the processor's output sequence

$$\{y_i\} = F[\{x_i\}]$$

has the form

$$\{y_i\} = \mu\{z_p{}^i\} \quad (19)$$

(where μ is a constant, possibly complex) provided $F[\ ]$ is a linear time-invariant digital system.

2) Since the processor is time-invariant we may write for any n

$$F[\{x_{i+n}\}] = F[\{z_p{}^{i+n}\}] = \{y_{i+n}\}. \quad (20)$$

3) On the other hand, since the processor is linear, this same excitation can be interpreted in another way.

$$F[\{x_{i+n}\}] = F[\{z_p{}^{i+n}\}] = F[z_p{}^n\{z_p{}^i\}] = z_p{}^nF[\{z_p{}^i\}] = z_p{}^n\{y_i\}. \quad (21)$$

4) Since the response to any one excitation sequence is unique we must have from (20) and (21)

$$\{y_{i+n}\} = z_p{}^n\{y_i\} \quad (22)$$

or, setting $i=0$,

$$y_n = y_0z_p{}^n \quad (23)$$

for all n. That is,

$$\{y_i\} = F[\{z_p{}^i\}] = y_0\{z_p{}^i\}$$

has the form of a constant times $\{z_p{}^i\}$ which is what we wanted to show.

Thus, if the input to a linear time-invariant digital processor is of the form $z_p{}^i$, an eigenfunction of the processor, then the processor's output sequence is identical to the input sequence except for a constant multiplier.

Processor Response to Suddenly Applied Excitations

Let us return now to the processor pictured in Fig. 4. For this processor we developed the equation

$$y_i + a_1y_{i-1} + a_2y_{i-2} = b_0x_i + b_1x_{i-1} \qquad -\infty < i < \infty \quad (24)$$

as the relation between the input and output sequences. We assume that the system is initially at rest and that it is excited by the sequence $\{x_i\}$ having elements

$$x_i = [Xz_p{}^i]_{-1}u_i \quad (25)$$

where X is a constant. In (25) ${}_{-1}u_i$ is the unit step sequence which is defined as

$${}_{-1}u_i = \begin{cases} 1 & i \geq 0 \\ 0 & i < 0. \end{cases} \quad (26)$$

Now, let us solve (24) for the output sequence $\{y_i\}$ for all i.

From (25) and (26) we see that a discontinuity occurs in the input sequence at $i=0$. Therefore, let us divide the problem of solving for $\{y_i\}$ into two regions corresponding to $i<0$ and $i>0$ and obtain the solution to the difference equation separately in each region. Our general approach will be to find solutions to the difference equation in each of the regions and then to select from these the solutions that satisfy certain boundary conditions at $i=0$. Thus, we will need to examine the solution of the equation as we pass through $i=0$. Taken together, the solutions for $i<0$, $i=0$, and $i>0$ form the complete solution to the difference equation for all i.

First, consider the solution for $i<0$. From (25) and (26) we see that the excitation is identically zero throughout this region. Therefore, since the system was at rest prior to the application of the excitation, the output sequence is also zero prior to $i=0$. That is,

$$y_i = 0 \qquad i < 0. \tag{27}$$

Now, we are ready for the region $i>0$. We note from (25) that the excitation for this region is

$$x_i = X z_p{}^i \qquad i > 0. \tag{28}$$

$z_p{}^i$ is an eigenfunction of the processor and therefore the processor's output sequence must be of the form

$$y_i = Y z_p{}^i \qquad i > 0 \tag{29}$$

where Y is a constant yet to be evaluated. Substitution of (28) and (29) into (24) yields

$$Y z_p{}^i + a_1 Y z_p{}^{i-1} + a_2 Y z_p{}^{i-2} = b_0 X z_p{}^i + b_1 X z_p{}^{i-1}$$

from which we obtain

$$Y = z_p \frac{b_0 z_p + b_1}{z_p{}^2 + a_1 z_p + a_2} X. \tag{30}$$

Further substitution of (30) into (29) yields

$$y_i = z_p \frac{b_0 z_p + b_1}{z_p{}^2 + a_1 z_p + a_2} X z_p{}^i \qquad i > 0. \tag{31}$$

This solution is known as the particular solution of the difference equation.

The particular solution is not the most general solution of the difference equation. A more general solution can be obtained by adding to the particular solution a solution of the difference equation with the excitation set to zero; that is, a solution of the equation.

$$y_i + a_1 y_{i-1} + a_2 y_{i-2} = 0. \tag{32}$$

This equation is known as the homogeneous equation and its solution is the homogeneous solution. In order to demonstrate that the sum of the particular solution (denoted by ${}_p y_i$) and the homogeneous solution (denoted by ${}_h y_i$) is a solution of (24), let us begin by writing the equations

$${}_p y_i + (a_1)\,{}_p y_{i-1} + (a_2)\,{}_p y_{i-2} = b_0 X z_p{}^i + b_1 X z_p{}^{i-1}$$

and

$${}_h y_i + (a_1)\,{}_h y_{i-1} + (a_2)\,{}_h y_{i-2} = 0.$$

Upon adding both sides of these two equations and collecting terms we have

$$({}_p y_i + {}_h y_i) + a_1({}_p y_{i-1} + {}_h y_{i-1}) + a_2({}_p y_{i-2} + {}_h y_{i-2}) = b_0 X z_p{}^i + b_1 X z_p{}^{i-1}. \tag{33}$$

Thus,

$$y_i = {}_p y_i + {}_h y_i \tag{34}$$

is a solution of the original difference equation.

In order to determine the homogeneous solution, we select the trial solution

$${}_h y_i = C z^i \tag{35}$$

where C and z are constants. This trial solution is substituted into the homogeneous equation (32) resulting in the equation

$$C z^i + a_1 C z^{i-1} + a_2 C z^{i-2} = 0$$

or

$$(z^2 + a_1 z + a_2) C z^{i-2} = 0.$$

This equation, which is satisfied if

$$z^2 + a_1 z + a_2 = 0 \tag{36}$$

independent of the value C, is known as the characteristic equation. The values of z which satisfy it are

$$z = \frac{-a_1 \pm \sqrt{a_1{}^2 - 4a_2}}{2} \tag{37}$$

which we will denote by z_1 and z_2. Thus, the most general homogeneous solution for the specific processor at hand is

$${}_h y_i = C_1 z_1{}^i + C_2 z_2{}^i \qquad i > 0. \tag{38}$$

The general solution for the processor's output for $i>0$ is then

$$y_i = z_p \frac{b_0 z_p + b_1}{z_p{}^2 + a_1 z_p + a_2} X z_p{}^i + C_1 z_1{}^i + C_2 z_2{}^i \tag{39}$$

where C_1 and C_2 are arbitrary constants.

We now have solutions for y_i in each of the two regions $i<0$ and $i>0$. The next task is to match the solutions at $i=0$. From the original equation (24), upon substitution of (25) and (27), we see that

$$y_0 = b_0 X \tag{40}$$

and

$$y_1 = b_0 X z_p + b_1 X - a_1 b_0 X. \tag{41}$$

However, evaluating (39) for $i=0$, 1 we have

$$y_0 = z_p \frac{b_0 z_p + b_1}{z_p{}^2 + a_1 z_p + a_2} X + C_1 + C_2 \tag{42}$$

and

$$y_1 = z_p \frac{b_0 z_p + b_1}{z_p{}^2 + a_1 z_p + a_2} X z_p + C_1 z_1 + C_2 z_2. \tag{43}$$

Now, the solutions for $i<0$ and $i>0$ can be matched at $i=0$ by first equating the y_0 given by (40) with the y_0 from (42) and by equating the y_1 from (41) with the y_1 from (43) which yield the equations

$$C_1 + C_2 = b_0 X - z_p \frac{b_0 z_p + b_1}{z_p{}^2 + a_1 z_p + a_2} X$$

and

$$C_1 z_1 + C_2 z_2 = b_0 X z_p + b_1 X - a_1 b_0 X - z_p \frac{b_0 z_p + b_1}{z_p^2 + a_1 z_p + a_2} X z_p \quad (44)$$

and then solving these equations for the arbitrary constants C_1 and C_2. The final solution is then

$$y_i = \begin{cases} 0 & i < 0 \\ z_p \dfrac{b_0 z_p + b_1}{z_p^2 + a_1 z_p + a_2} X z_p{}^i + C_1 z_1{}^i + C_2 z_2{}^i & i \geq 0 \end{cases}$$

where C_1 and C_2 are given by the solutions of (44). Since y_i is finite at $i=0$, the step sequence can be used to express this equation in a more compact form

$$y_i = \left[z_p \frac{b_0 z_p + b_1}{z_p^2 + a_2 z_p + a_1} X z_p{}^i + C_1 z_1{}^i + C_2 z_2{}^i \right]_{-1} u_i \quad -\infty < i < \infty. \quad (45)$$

Although we have only considered a specific example involving a second-order digital processor these techniques are easily extended to the analysis of more complex problems.

System Functions, Poles and Zeros, and the Frequency Response

In the previous section we demonstrated that the digital processor's output sequence, in general, is composed of two components: the particular solution and the homogeneous solution. Here we want to focus our attention on the particular solution in order to gain insight into the relations between the form of the particular solution and the properties of the processor response. Our interest in the particular solution stems from the fact that in many instances the particular solution forms the major portion of the total solution.

For the processor of Fig. 4 we found the particular solution to be

$${}_p y_i = z_p \frac{b_0 z_p + b_1}{z_p^2 + a_1 z_p + a_2} X z_p{}^i$$

for an excitation $X z_p{}^i$. For the more complex processor of Fig. 5 (see [1] for a discussion of the various forms that digital processors can have), the particular solution is found to be

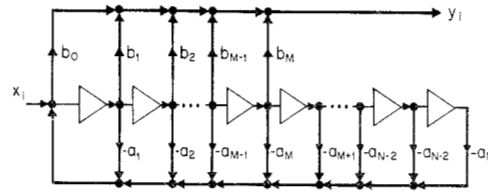


Fig. 5. Digital processor with N feedback paths and (M−1) feedforward paths.

$${}_p y_i = z_p{}^{N-M} \frac{b_0 z_p{}^M + b_1 z_p{}^{M-1} + \cdots + b_{M-1} z_p + b_M}{z_p{}^N + a_1 z_p{}^{N-1} + \cdots + a_{N-1} z_p + a_N} X z_p{}^i. \quad (46)$$

Or, if we let

$$B(z_p) = b_0 z_p{}^M + b_1 z_p{}^{M-1} + \cdots + b_{M-1} z_p + b_M \quad (47)$$

and

$$A(z_p) = z_p{}^N + a_1 z_p{}^{N-1} + \cdots + a_{N-1} z_p + a_N \quad (48)$$

then the particular solution becomes

$${}_p y_i = z_p{}^{N-M} \frac{B(z_p)}{A(z_p)} X z_p{}^k. \quad (49)$$

Thus, the complex amplitude of the particular solution is

$$z_p{}^{N-M} \frac{B(z_p)}{A(z_p)} X$$

that is, it can be obtained by multiplying the complex amplitude of the excitation X by

$$z_p{}^{N-M} \frac{B(z_p)}{A(z_p)}.$$

This rational function plays a significant role in the theory of linear digital processors. It is generally called the system function and denoted by

$$H(z_p) = z_p{}^{N-M} \frac{B(z_p)}{A(z_p)}. \quad (50)$$

When and if steady-state conditions are reached in the processor, the particular solution forms the total response, and the system function relates the complex amplitude of the total response to the complex amplitude of the excitation.

In general, the system function is a function of the complex quantity z_p associated with the excitation sequence. For a given z_p, the system function $H(z_p)$ is simply a complex number; it can be specified by its real and imaginary parts or by its magnitude and angle.

In continuous systems we often summarize the response of a system to a sinusoidal excitation with different values of frequency by displaying the system function in graphical form for a range of frequency values. Since the system function is complex it is represented by two curves—the magnitude as a function of frequency and the angle as a function of frequency. In a similar manner we summarize the response of a linear time-invariant digital processor to samples of a sinusoid; that is, to

$$x_i = z_p{}^i = (e^{jwT})^i \quad (51)$$

by plotting the magnitude and angle of $H(z_p)$ as w is

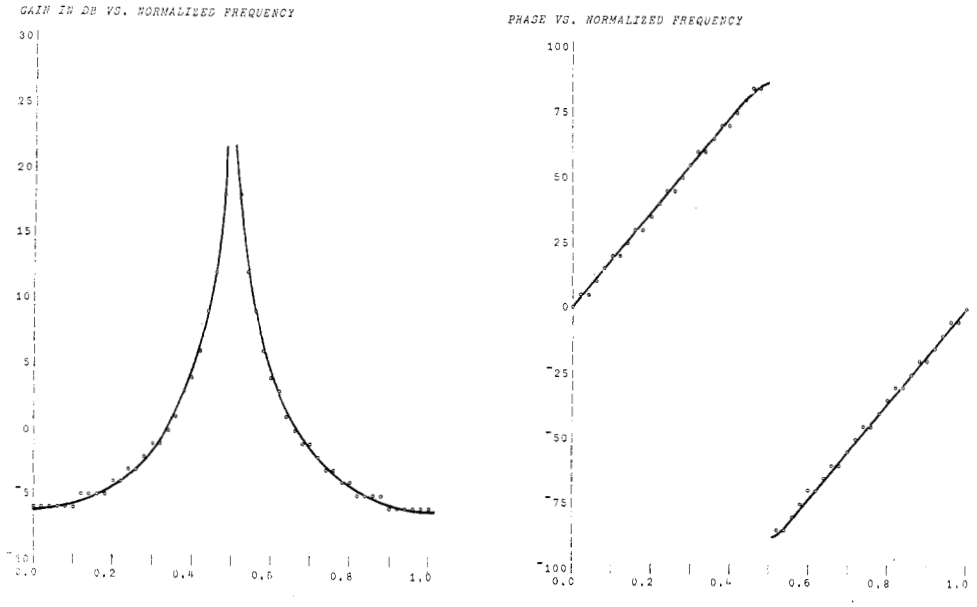


Fig. 6. Frequency response of the system of Fig. 2 with $K=-1$.

varied. In (51), w is the radian frequency of the complex sinusoid,

$$w = 2\pi f$$

where f is the cyclic frequency and T is the time between samples and equals $1/f_s$ where f_s is the sampling frequency. Thus,

$$x_i = (e^{j2\pi f/f_s})^i. \tag{52}$$

As an example, consider the simple processor of Fig. 2. The system function for this processor is

$$H(z_p) = \frac{z_p}{z_p - K}. \tag{53}$$

For $z_p = e^{j2\pi f/f_s}$, this becomes

$$H(z_p) = \frac{e^{j2\pi f/f_s}}{e^{j2\pi f/f_s} - K} \tag{54}$$

from which we obtain

$$\left| H(e^{j2\pi f/f_s}) \right| = \frac{1}{\sqrt{1 + K^2 - 2K\cos 2\pi f/f_s}} \tag{55}$$

and

$$\angle H(e^{j2\pi f/f_s}) = 2\pi f/f_s - \tan^{-1}\frac{\sin 2\pi f/f_s}{\cos 2\pi f/f_s - K}. \tag{56}$$

For this simple example, we see that the $|H|$ is periodic in f/f_s (period of unity) and even and that $\angle H$ is periodic in f/f_s (period unity) when the angle is taken modulo 2π and odd. (For system functions $H(z_p)$ with coefficients a_i, $i=1, 2, \cdots, N$ and b_k, $k=0, 1, 2, \cdots, M$ which are real, it can be shown that $|H|$ will always be even and that $\angle H$ will always be odd.) Equations (55) and (56) are plotted in Fig. 6 for $K=-1$.

Previously, we defined the system function by the equation

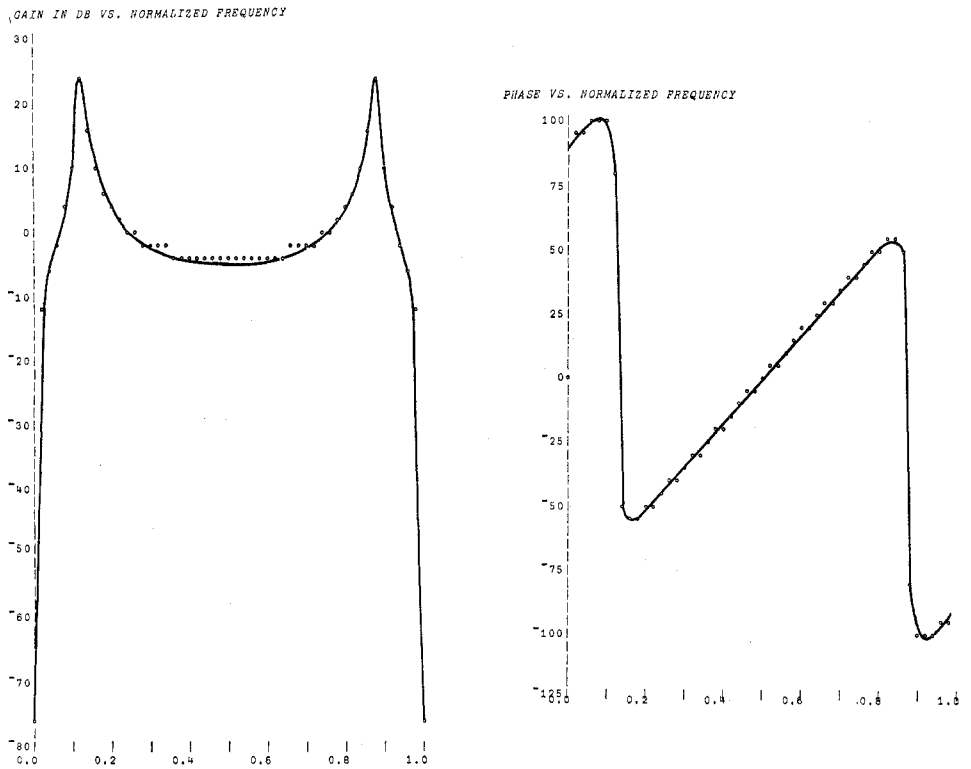
$$H(z_p) = z_p{}^{N-M}\frac{b_0 z_p{}^M + b_1 z_p{}^{M-1} + \cdots + b_{M-1}z_p + b_M}{z_p{}^N + a_1 z_p{}^{N-1} + \cdots + a_{N-1}z_p + a_N} = z_p{}^{N-M}\frac{B(z_p)}{A(z_p)}. \tag{57}$$

Basically, this function consists of three parts: a numerator polynomial $B(z_p)$, a denominator polynomial $A(z_p)$, and a multiplying factor $z_p{}^{N-M}$. Using a basic theorem of algebra which states that, if $f(x)$ is a polynomial of degree M, the equation $f(x)=0$ has M roots, $x_1, x_2, \cdots, x_M$ and therefore that $f(x)$ can be written as $(x-x_1)(x-x_2)\cdots(x-x_M)$, we can write (57) as

$$H(z_p) = z_p{}^{N-M} b_0 \frac{(z_p - {}_1z)(z_p - {}_2z)\cdots(z_p - {}_Mz)}{(z_p - z_1)(z_p - z_2)\cdots(z_p - z_N)}. \tag{58}$$

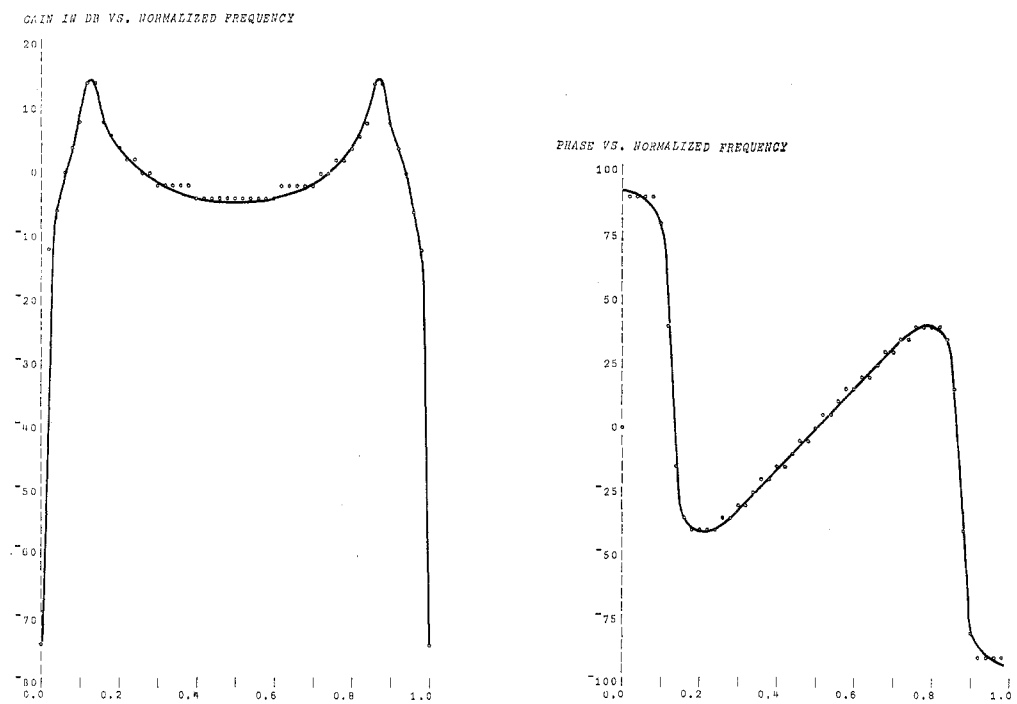
The M complex constants ${}_1z, {}_2z, \cdots, {}_Mz$ are called the zeros of the system function and are roots of $B(z_p)=0$. The N complex constants $z_1, z_2, \cdots, z_N$ are called poles of $H(z_p)$ and are roots of $A(z_p)=0$. The multiplier $z_p{}^{N-M}$ specifies additional zeros (poles) of the system function if $N>M$ (if $N<M$). These zeros (poles) are located at the origin of the z-plane. [In (58) the number of poles identically equals the number of zeros in the system due to the presence of the term $z_p{}^{N-M}$. If as is often the case, the system output is not y_i but y_{i-k}, then the number of poles will not equal the number of zeros and the multiplier will be $z_p{}^{N-M+k}$.] When z_p coincides with a zero of the system function, the system function is zero; when it coincides with a pole of the system function, the system function is infinite.

Each pole or zero is a complex number and can be represented by a point in the z-plane. The usual conven-



g. 7. Frequency response of the system of Fig. 4 with $b_0 = -1$, $b_1 = -1$, and the poles at $z = 0.98e^{\pm j\pi/4}$.

Fig. 8. Frequency response of the system of Fig. 4 with $b_0 = 1$, $b_1 = -1$, and the poles at $z = 0.9e^{\pm j\pi/4}$.



tion is to plot the poles as x's and the zeros as 0's in the z-plane. In Figs. 7–10 we show the frequency response curves for the processor of Fig. 4 with $b_0 = 1$ and $b_1 = -1$, and with a_1 and a_2 taking on various values to illustrate the types of responses which can be obtained with the processor.

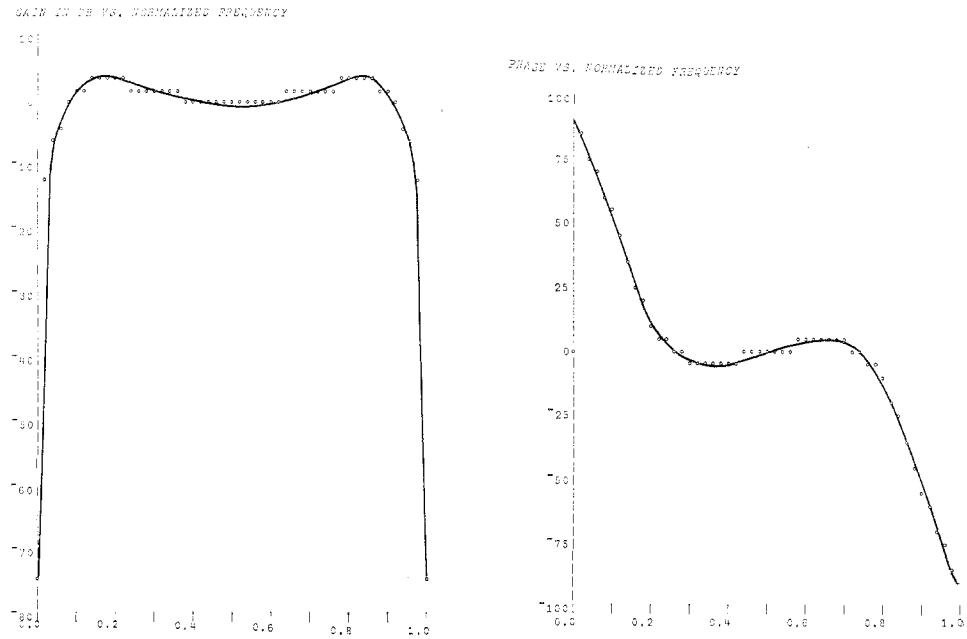
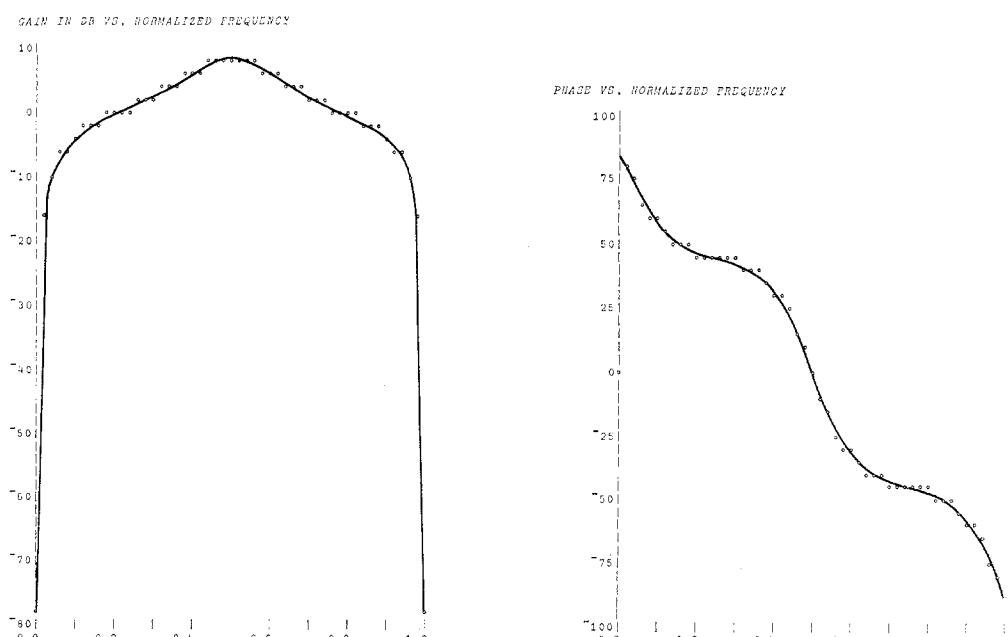


Fig. 9. Frequency response of the system of Fig. 4 with $b_0 = 1$, $b_1 = -1$, and the poles at $z = 0.5e^{\pm j\pi/4}$.

Fig. 10. Frequency response of the system of Fig. 4 with $b_0 = 1$, $b_1 = -1$, and the poles at $z = \pm 0.5$.



Conclusion

In this paper we have illustrated some of the basic concepts in the analysis of digital processors. We have not treated the problems associated with processor design (synthesis) and realization. Extensive bibliographies, which point the interested reader to materials on these subjects, may be found in [6]–[8].

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