Design and Implementation of Power Efficient Logic BIST With High Fault Coverage Using Verilog

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***Abstract*— Due to ever increasing number of transistors on chip and decrease in feature size have posed challenges in manufacturing and have risen defects due to them. Thus, testing have become vital for any Very Large Scale Integrated (VLSI) design. The design engineers concentrate more on design development and test techniques used to test those designs are neglected due to design cycle time. Any design will not be passed unless it is 100% fault free and Design For Testability (DFT) technique facilitates to detect the faults. Multiple standards are developed to test different part of Integrated circuits. In this paper power efficient & high fault coverage Built In Self-Test (BIST) is designed and implemented to test combinational logic. The developed technique is tested on standard combinational circuits and has given promising results. The conventional Linear Feedback Shift Register (LFSR) is modified to generate all the states, hence improving fault coverage. Compared to conventional method, 100% fault coverage & 12.25% reduction in power is achieved by the proposed design. The design is coded in Verilog, verified for functionality using Xilinx ISIM simulator, synthesized by targeting the design to *slow_vdd1v0 1.0* library for 45nm technology using Cadence genus tool and validated on FPGA Spartan 6 boards.**

Keywords—Logic Built In Self-Test (LBIST), Design For Testability (DFT), faults, Design Under Test (DUT), Linear Feedback Shift Register (LFSR)

I. Introduction

The ever-increasing number of transistor and decrease in the size of chip has given rise to defects in the VLSI Circuits. The defect could be in the manufacturing process, fabrication or design. Design errors are attended by verification process while manufacturing errors are detected through testing methods. The advancement in the sub-micron technology has given rise to various Integrated Circuits (IC) complexities. The decrease in the size have led to various complexities in fabrication process also. This has given rise to a demand for fault tolerance which not only depends on reliability but also the ability to detect faults [1].

The branch of VLSI which deals with testing and designing suitable methodology for testing is regarded as DFT. VLSI testing mainly focuses on test generation and DFT. Test generation majorly concentrates on what kind of and how many test patterns to be applied to the design so that with minimum test patterns maximum fault coverage is achieved. DFT concentrates on how to modify the design so as to make it easier and efficient for Testing. BIST is a methodology in DFT. BIST is an art of designing the circuit to test themselves. BIST used for testing logic is regarded as Logic BIST (LBIST).

Power is one of the major concerns that is involved in testing. Studies show that power consumption will be more during testing, because of the increased switching activity. Test power affects the quality of test and test cost, especially in low power circuits. If the test power is left unattended then it could cause circuit malfunction due to excessive heating. Xiaoqing Wen [2], mentions the two goals of test generation and DFT namely, high test quality and low-test cost. And quoting from [2], "*No matter how attractive a low power circuit design is, it cannot be realized without low power testing*". Usha Mehta et al [3], mentions various power reduction techniques for all aspects of testing. Some of the low power testing techniques mentioned are reducing transitions, generating useful vectors only, filtering unnecessary vectors, portioning the circuit, using separate strategy for testing memory.

With the aim to achieve power optimized LBIST design and good fault coverage, a methodology is proposed. The rest of the paper is organized as follows, section II describes Implementation of LBIST, results and discussion are provided in section III, Design Summary is given in section IV and conclusion is presented in section V.

II. Implementation Of Lbist

The architecture of LBIST considered is as shown in Figure. 1. *Test Pattern Generator (TPG):* TPG helps to generate input patterns for LBIST in testing mode. TPG that is considered is an LFSR of size 8 bit. Conventional LFSR generates only (2^n-1) states in pseudo random manner where n is the number of bits, in order to improve the fault coverage a Modified LFSR [4] is considered which generates all (2^n) states in pseudo random manner.

Output Analyser is a compression technique used to obtain a signature from the outputs of the DUT. *Multiple Input Signature Register (MISR)* is chosen for Output Analyser and the size of which is 8 bits.

BIST controller is designed to activate respective blocks based on whether the BIST is operated in normal mode or testing mode.

Multiplexer (MUX) is used to select between the primary inputs and test pattern, therefore 2X1 MUX is utilized. The size of the input to MUX is 8-bit since the LFSR is of 8-bit in size. The input data for MUX is a vector therefore the output data is also a vector. The select signal of MUX is controlled by BIST Controller.

The design that is considered for testing, *DUT* is *Vedic multiplier*, reason being multipliers are widely used in DSP applications and Vedic multipliers are one of the fastest multipliers as per the studies [5], [6]. The size of Vedic multiplier is 4X4, so it requires two inputs of 4-bit size. Since the output of MUX is 8-bit, higher nibble is fed as one input and lower nibble is fed as another input. The output of

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multiplier is 8 bit and they are directly fed to the output analyser.

Comparator is used to generate the status of testing as Good or faulty. In this method, a reference signature obtained for Good DUT called Golden signature is hard coded in the comparator for comparing with the actual signature obtained from DUT.

A. Working of LBIST

The functioning and structure of LBIST is gathered based on the work in [7], [8] and [9]. The LBIST works in two modes namely, test and normal. When in ***testing mode***, test pattern generator, output analyser is activated and the mux feeds test pattern as input to DUT from the test pattern generator, the output of DUT is compressed by MISR and the comparison is made for validating the design. When in ***normal mode***, the DUT works based on the primary inputs and since output analyser is disabled, the primary outputs are tapped out. The testing methodology that is considered is ***Exhaustive***.

B. Faults

Four categories of faults are considered namely: ***stuck at 0, stuck at 1, bridging and multiple faults***. Multiple fault is a combination of stuck at 0, stuck at 1 and bridging fault, that is all these faults will be present in the design. The faults are introduced in the design in the Verilog code and they are introduced at controllable and observable points.

C. Design of fault counter

An attempt to count the number of faults with help of a module included within the LBIST is performed. This modified LBIST is considered for the purpose of counting the number of faults to calculate fault coverage. Therefore, synthesis results of this method are not concentrated in this paper.

The fault counter is designed to count the number of faulty outputs and also gives the list of faulty output and corresponding test pattern. The total number of faults listed at the end of testing helps to calculate fault coverage [10].

Performing exhaustive and pseudo random test every time is not efficient. As the number of bits increases, time consumed by exhaustive testing will increase because of increase in the number of test patterns. With the list of patterns obtained for corresponding faulty output, the search can be narrowed down and with limited number of patterns, the fault can be found out.

The state diagram of the fault counter is as shown in Figure. 2. Initially when the LBIST is in normal or reset mode, all the signals involved in fault counter block is initialised to 0. When the LBIST enters testing mode, comparison is made between stored good output in the Read Only Memory (ROM) and primary outputs obtained from DUT. If they are not equal, the fault count will be incremented else it is not. The block diagram of LBIST with fault counter included is as shown in Figure. 3.

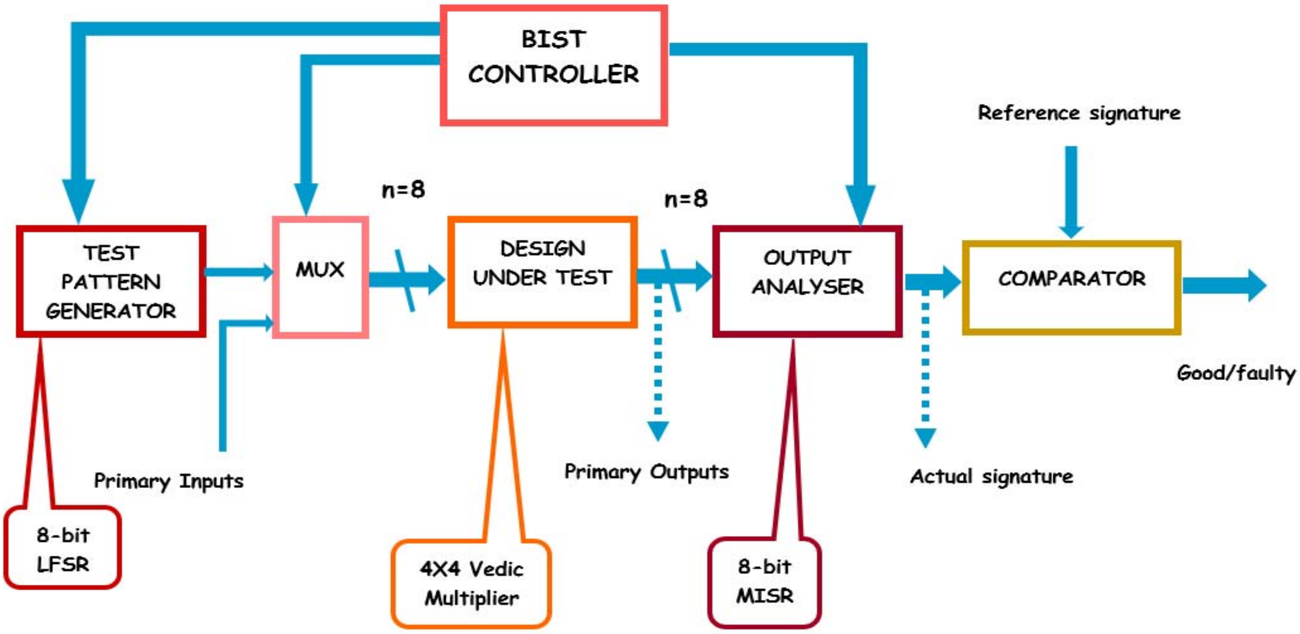

Figure.1: Block diagram of Proposed LBIST

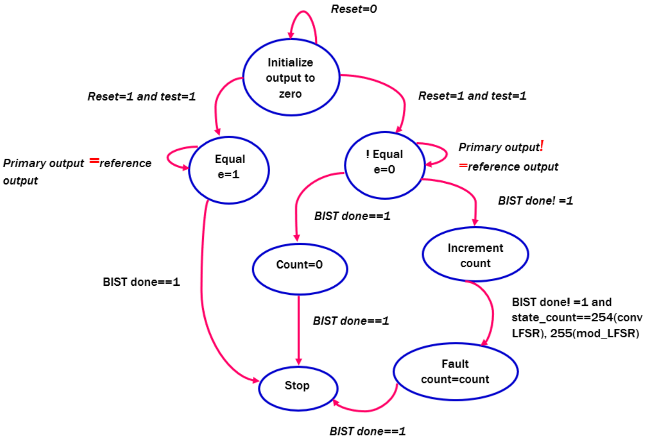

Figure. 2: State diagram of fault counter

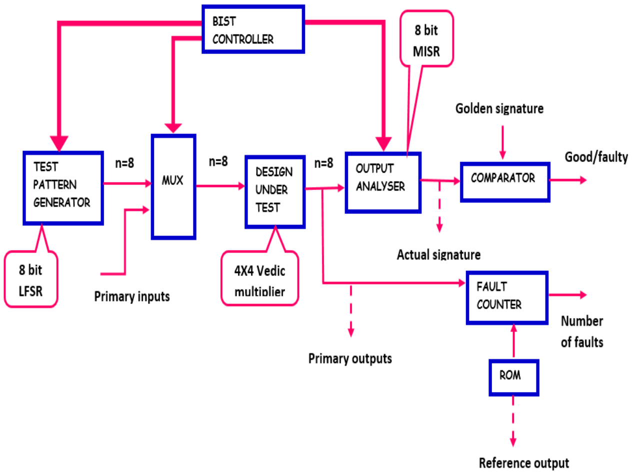

Figure. 3: Block diagram of LBIST with fault counter

III. RESULTS AND DISCUSSION

The proposed LBIST architecture is coded in *Verilog*, simulated using *Xilinx 14.7*, synthesized using *Cadence genus 45nm technology* targeting to *slow_vdd1v0 1.0* standard cell library to produce gate-level netlist and validated on *Spartan 6 FPGA board*. The RTL schematics were generated using *Xilinx 14.7 ISIM simulator*. The LBIST is verified for functionality in normal mode and in testing mode for good and faulty DUT. Also a simulation result for LBIST involving Fault counter is obtained.

A. Simulation Results of LBIST in normal mode

The normal mode of operation of LBIST is indicated in Figure. 4 and the validation of the same on FPGA is depicted in Figure. 5.

When reset is 0 as indicated by marker 1 in Figure. 4, the LBIST enters reset mode and the signals are set to respective initial values.

When reset is 1 and test is 0 as indicated by marker 2 in Figure. 4, the LBIST enters normal mode and works with primary input. The same is depicted in Figure. 5.

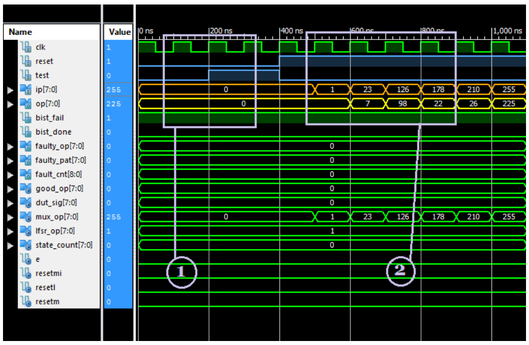

Figure. 4: LBIST in normal mode

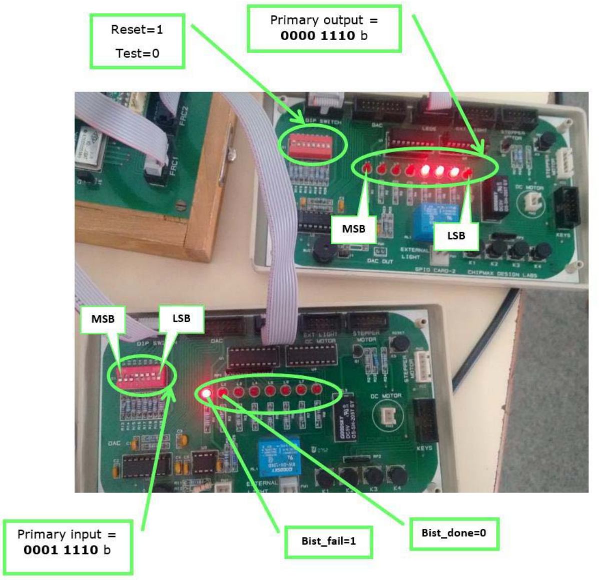

Figure. 5: LBIST in normal mode validated on FPGA

B. Simulation results of LBIST in testing mode

The testing mode of operation is indicated in Figure. 6. Marker 1 indicates when reset and test are 1, the BIST enters testing mode and the enable signals for test pattern generator, response analyser are provided and mux is enabled to choose test patterns as indicated by Marker 2 in Figure. 6.

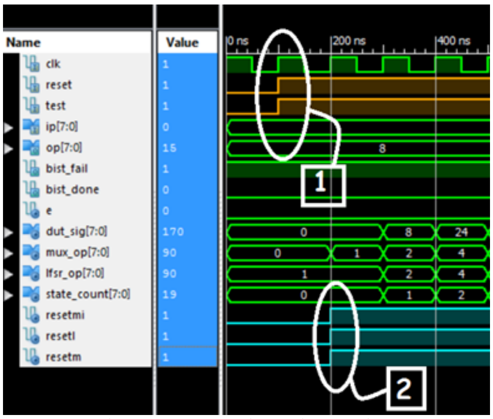

Figure. 6: LBIST in testing mode

C. Simulation result of LBIST testing GOOD DUT

The result of LBIST after testing is given in Figure. 7 and the validation of the same on FPGA is depicted in Figure. 8. Marker 1 in Figure. 7 indicates when testing is complete (*bist_done*=1), *bist_ fail* signal has become 0 indicating the DUT is ***GOOD***. The same is validated on FPGA and depicted in Figure. 8.

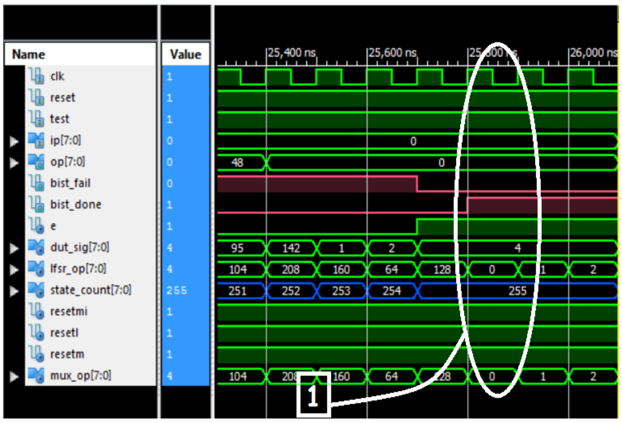

Figure. 7: LBIST in testing mode of GOOD DUT

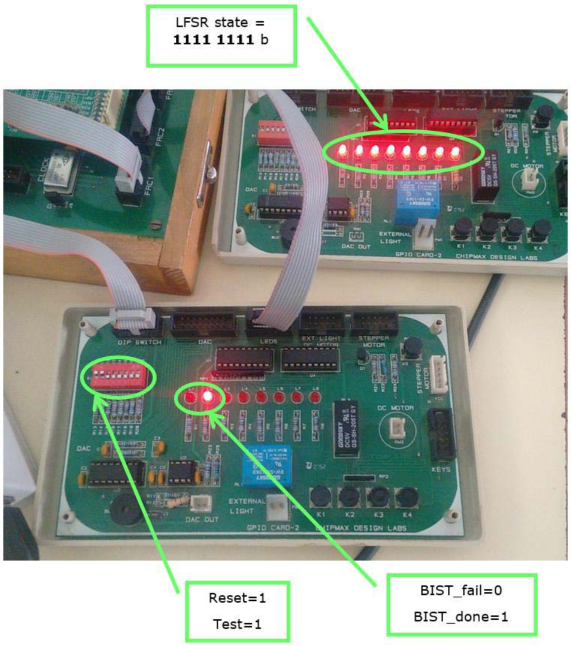

Figure. 8: LBIST in testing mode of GOOD DUT on FPGA

D. Simulation result of LBIST testing FAULTY DUT

The result of LBIST after testing is given in Figure. 9, marker 1 indicates when testing is complete (*bist_done*=1), *bist_ fail* signal has become 1 indicating the DUT is ***faulty***. For this simulation the DUT is injected with only **stuck at 0** faults at controllable and observable points. The similar observation is made when implemented on FPGA and is depicted in Figure. 10

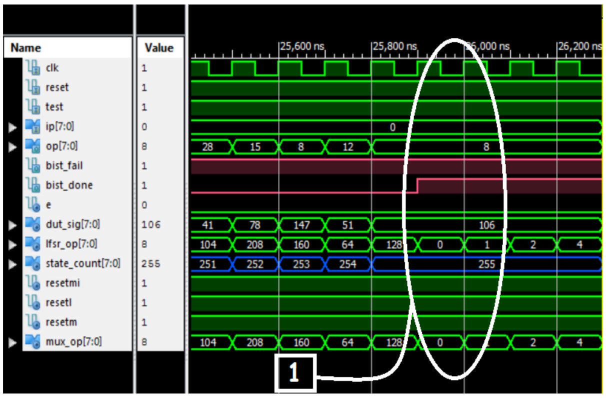

Figure. 9: LBIST in testing mode of FAULTY DUT

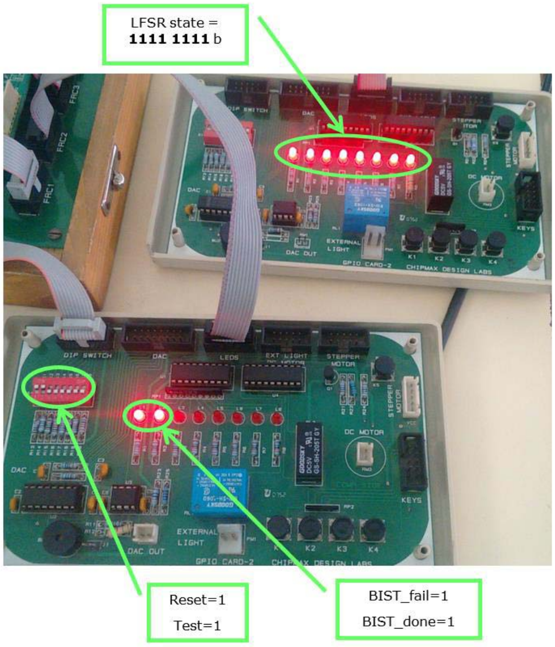

Figure. 10: LBIST in testing mode of FAULTY DUT on FPGA

E. Simulation result of LBIST with Fault counter testing faulty DUT

The result of testing DUT using LBIST with fault counter is given in Figure. 11. In this case **multiple faults** are injected at controllable and observable points of the design. Marker 1 indicates when testing is complete (*bist_done=1*), *bist_ fail* signal has become 1 indicating the DUT is ***faulty***. The LBIST is associated with fault counter also, therefore the **number of faults detected is 236** as indicated in Figure 11.

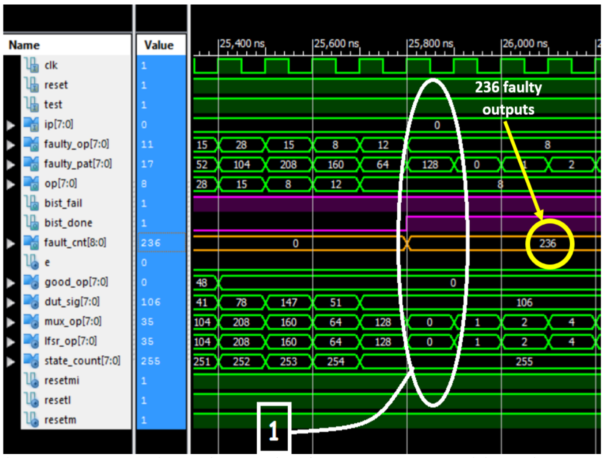

Figure. 11: LBIST in testing mode of FAULTY DUT with Fault counter

F. *Fault Coverage*

The fault coverage obtained for various DUT and for LBIST with conventional LFSR and Modified LFSR as TPG is depicted in Table I. The fault coverage is analyzed to be ratio of Number of faults detected to Number of faults present or injected [10]. The faults induced in each of the DUT are of type multiple faults and they were inserted at controllable and observable points.

It can be observed that because of the introduction of an extra state, fault coverage is improved in the case of LBIST with modified LFSR as TPG. The analysis in the form of a graph is depicted in Figure. 12.

TABLE I
ANALYSIS OF FAULT COVERAGE

Design Under Test (DUT)	**Number of faults present**	**Fault coverage (in %)**	
		Conventional Fibonacci LFSR	***Modified Fibonacci LFSR***
Vedic Multiplier	236	99.57	100
Binary to Gray code converter	224	99.55	100
8 to 3 Priority Encoder	244	99.59	100

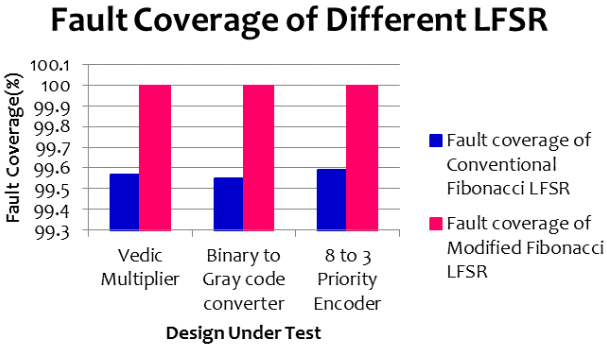

Figure.12: Graph of fault coverage

IV. Design Summary

The proposed LBIST design (Figure. 1) was compared with conventional LBIST which uses conventional LFSR and clocked comparator [8]. The power analysis is presented in Table II. It can be observed that LBIST with modified Fibonacci LFSR (LBIST_mf) gives 12.25% power reduction and improved fault coverage.

The reason for reduction in power is due to consumption of a smaller number of cells by proposed design when compared to conventional LBIST and also the dynamic power consumed has reduced significantly because the comparator utilized in proposed design does not use clock signal as opposed to conventional LBIST. The analysis of the total power trend is presented in Figure. 13 as a graph.

TABLE II
POWER ANALYSIS OF LBIST

Design	**cells**	**Leakage power (nW)**	**Dynamic power (nW)**	**Total power (nW)**	**%power reduction of total power**
conventional LBIST	91	6.818	13501.776	13508.594	--
LBIST_mg	84	6.845	11941.926	11948.771	11.55 ↓
LBIST_mf	86	6.917	11846.385	11853.302	12.25 ↓

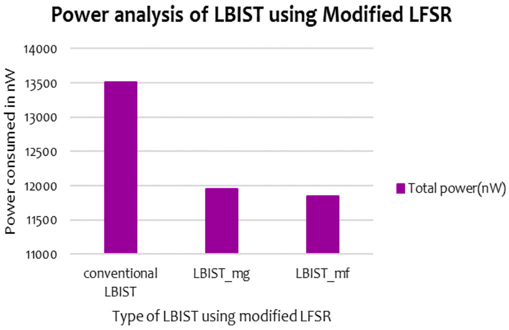

Figure. 13: Graph of power analysis of LBIST

V. Conclusion

To meet ever demanding costumer needs the designs are becoming complex. The complexity involved in chip design makes fabrication process complicated and may lead to defective chips. To improve yield of the chip, fault free design is the need of the day. Design for Test techniques required to detect the faults and some cases correction are also incorporated for improvement in the yield process. The power consumption during testing mode must also be accounted since it affects test quality and test cost.

The proposed LBIST design used to test combinational circuit achieves 12.25% power reduction and 100% fault coverage. The power reduction is due to logic re-structuring optimization. The proposed design is also validated on FPGA spartan 6 development board.

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