BUSIREDDY JAGADEESHWAR REDDY

VLSI ENGINEER

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CAREER SUMMARY

A highly motivated and skilled Electronics and Communication Engineer eager to work in the VLSI front-end domain roles (RTL Design, Design Verification). Passionate about contributing valuable work to innovative projects and learning from industry leaders, I am confident in my ability to make a meaningful impact while growing as a professional.

PROFESSIONAL TRAINING/CERTIFICATION

- **ADVANCE VLSI DESIGN AND VERIFICATION** Feb 2025 – to date
  Maven-Silicon VLSI Design and Training Center | Bangalore, India
- **FUNDAMENTALS OF DIGITAL ELECTRONICS FOR VLSI** Nov 2nd, 2024
  Coursera- an online course authorized by L&T EduTech.
- **PROGRAMMING FOR EVERYBODY (GETTING STARTED WITH PYTHON)** **Oct** 21st, 2023
  Coursera - an online course authorized by the University of Michigan.

EDUCATION

DEGREE	INSTITUTION	DURATION	AGGREGATE
B-TECH (ECE)	GITAM UNIVERSITY (BANGALORE)	2021-2025	8.0 CGPA
INTERMEDIATE (M.P.C)	NARAYANA JUNIOR COLLEGE	2019-2021	916/1000
SSC	NARAYANA SCHOOL	2018-2019	9.8

TECHNICAL SKILLS

- VLSI Design
- Verilog
- Basic Programming Languages (Python and C)
- Xilinx Vivado
- Modelsim
- Cadence Virtuoso

PROJECTS

1. ROUTER 1x3: May 2025 – present

Maven-Silicon VLSI Design and Training Center | Bangalore, India

Designed and implemented a 1x3 Router functionality for forwarding data packets between computer networks and developed a Verilog HDL-based design for an OSI layer 3 routing device.

- **Tools & technologies** – VLSI Design, Verilog, Digital Electronics, Modelsim, Quartus Prime
- Developed the comprehensive block-level architecture for the router, integrating key components such as FSM, dedicated FIFOs for each output and robust error detection logic.

2. BIST DESIGN FOR FAULT DETECTION IN CIRCUITS: Dec 2024 – Mar 2025

B-tech | GITAM, Bangalore

Design a BIST architecture and inject it into modules to find the faults in circuits

- **Tools & technologies –** BIST, VLSI Design, Verilog, Modelsim, Quartus Prime
- TPG (test pattern generator) is used for pattern generator as input for DUT.

- MISR is used as a signal analyzer and to generate a Golden signature.
- With the help of a Golden signature Faults are detected.

3. PROTECTING USER PASSWORD KEYS AT REST: May 2024 – Jul 2024

Intel Unnati | Bangalore, India

Developed a security system using Python and cryptographic algorithms for real-time file management and protection

- **Tools & technologies -** Python, Tkinter, AES Encryption, Argon2.
- I designed a secure and user-friendly encryption tool utilising AES-256 with a graphical user interface (GUI) for easy file and folder encryption and decryption.
- Developed an innovative approach to integrating FPGA boards into functional tests, leading to systematic assessments that ensured compliance with industry standards while maintaining accuracy within a margin of error below one per cent.

INTERNSHIPS

- Self-Development and VLSI Design Intern May 2024 – Jul 2024
- Intel® Unnati Industrial Training for File Protection May 2024 – Jul 2024

ACHIEVEMENTS

- Certificate of Completion - Intel® Unnati Industrial Training – 2024

HOBBIES

- Doing workouts in Gym
- Watching movies

DECLARATION

I hereby declare that all the details mentioned above are true and factual to the best of my knowledge, and I take responsibility for the accuracy of these particulars.

PLACE : BANGALORE **NAME :**

Busireddy Jagadeeshwar Reddy