

0.1 Design Specifications

The Design of a Bootstrapped Sampling Circuit. The specifications for the sample-and-hold circuit are listed in Table 1.

Parameter	Value
Number of bits (N)	10
Supply Voltage (VDD)	1.2V
Input Voltage Swing (VFS)	0.6 - 1.0V
Temperature (T)	300K
ENOB (Nyquist Bandwidth)	> 8 bits
THD (Nyquist Bandwidth)	> 55 dB
Sampling Frequency (Fs)	1.0 GHz
Clock Rise, Fall times (Tr, Tf)	10 ps

Table 1: Design Specifications

0.1.1 Basic Boot-Strap

I Simulated the schematic shown in fig 1 in Cadence for a sine input (near frequency $F_s/5$ and $F_s/2$) using vsin from analoglib and I verified the output by performing the Transient Analysis with given Test Bench. The output is shown in fig2. I provided the required calculations to get the desired output. Our primary concern is On resistance of the Switch should be independent of V_{in} and the Inversion charge is independent of V_{in} in order to reduce to distortion occur at the output. Assumption is Thermal Noise is less than Quantization Noise. So,

$$\frac{KT}{C} < \frac{\Delta^2}{12}$$

Now, $\Delta = \frac{V_{FS}}{2^N}$ where $V_{FS} = (1 - 0.6) = 0.4$ and $N = 10$

$$C > \frac{12KT}{(V_{FS})^2} \times 2^{2N}$$

$$C > 325fF$$

So capacitor value is chosen here as $C=325f\text{ F}$. But $C_L = 250fF$ therefore

$$C_1 = C - C_L = 75fF$$

Transistor Width selection for M1: Settling Error should be less than 1 LSB

$$\text{Settling Error} = V_{in} - V_{out} = V_{in}e^{-\frac{t}{\tau}}$$

$$V_{in} = V_{FS} \quad \text{and} \quad t = \frac{T_{clk}}{2}$$

So,

$$V_{FS}e^{\frac{-t}{\tau}} < \Delta$$

$$\tau = \frac{T_{clk}}{N \times 2 \ln 2} \quad \text{where } \frac{V_{FS}}{\Delta} = 2^N$$

$$R_{SW} < \frac{0.72}{NCf_{sample}}$$

$$R_{SW} < 220 \Omega$$

In order to get the required Ron, I simulated the schematic1 by performing dc analysis by changing the width of Transistor by seeing the Ron in Results(Operating Point Report). Finally, after some iterations to get the Desired $Ron = 200\Omega$ and the width of M1 is 3.25um. I checked the region of Transistor as well , it is perfectly switching between linear and cutoff regions.

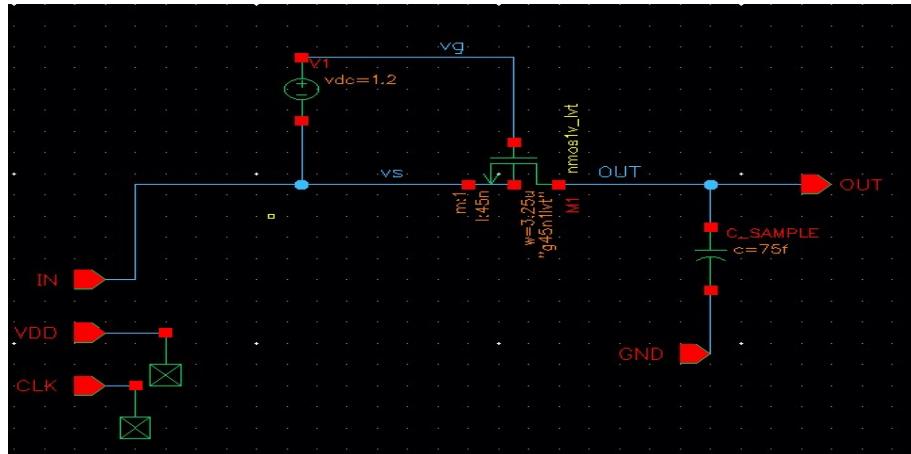


fig1: Basic Boot-Strap

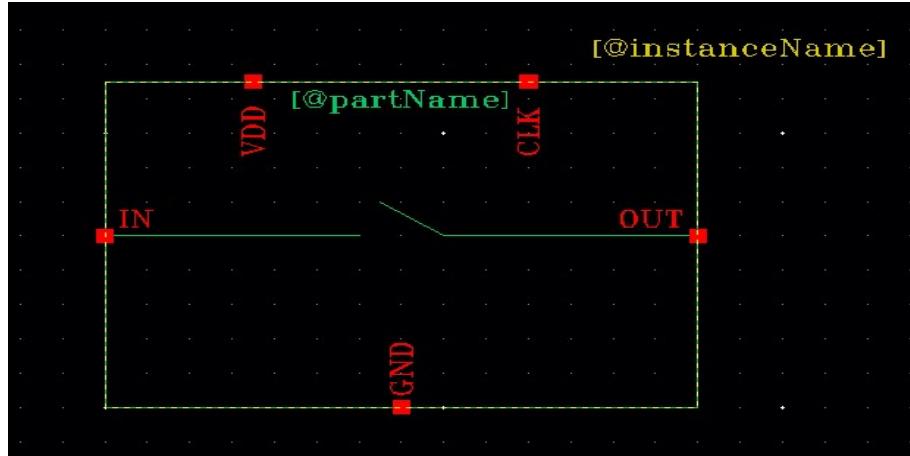


fig2: Symbol

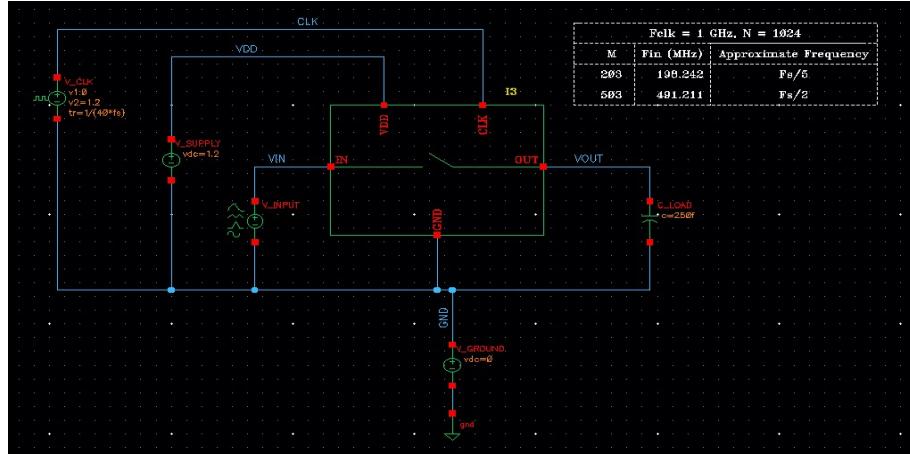


fig3: General Test Bench

Parameter	M1	C1
Width(um)	3.25	75f F
Length(nm)	45	

Table 2: Parameter Values

0.1.2 Introducing Sampling

I Simulated the schematic shown in fig 3 in Cadence for a sine input (near frequency $F_s/5$ and $F_s/2$) using vsin from analoglib and I verified the output by performing the Transient Analysis with given Test Bench. The output is shown in fig4.Based on the condition of on Resistance $R_{on1} = 200\Omega$, I chosen the Width of M2 and M4 as 4um. I checked the region of Transistor as well , it is perfectly switching between linear and cutoff regions. I done

the Spectral analysis to see the ENOB and THD, they meet the required specification.

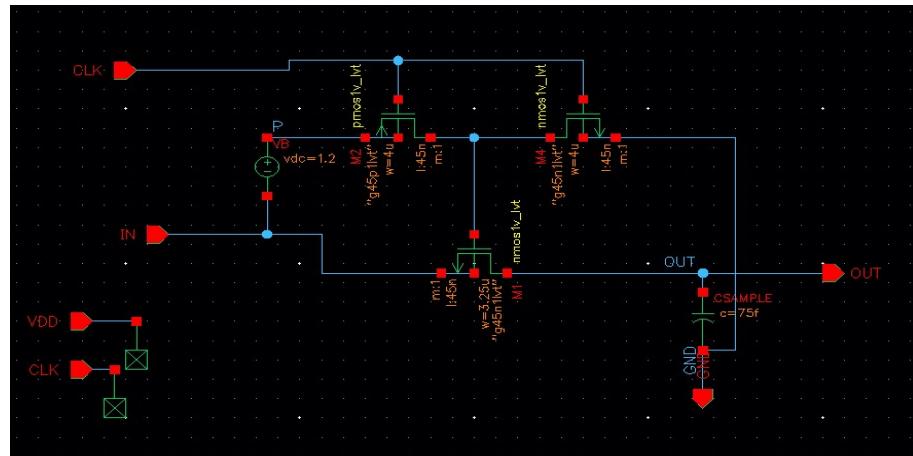


fig4: Introducing Sampling

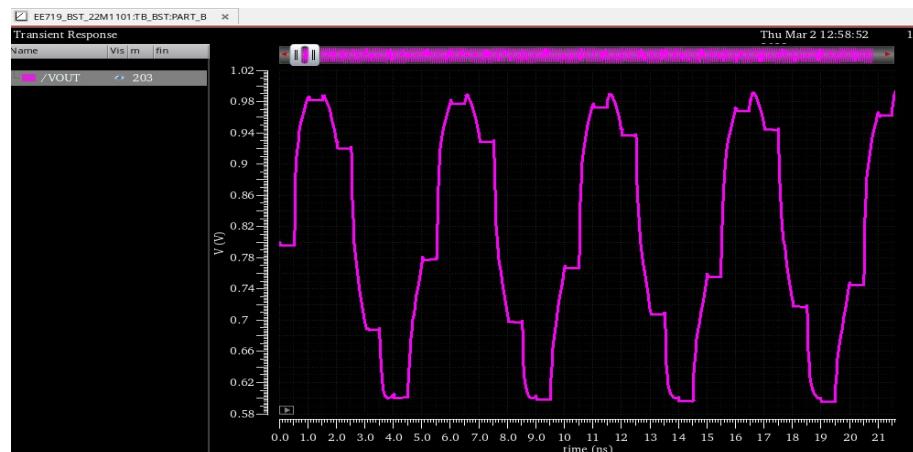


fig5: Output at fin=FS/5

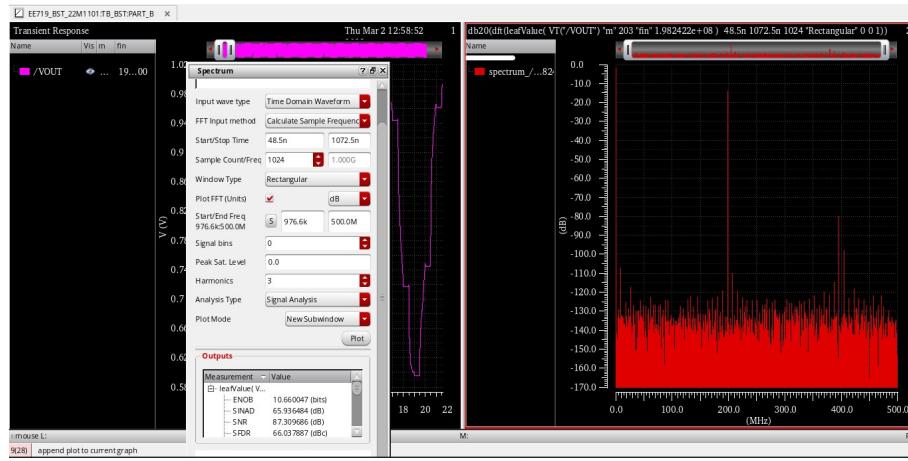


fig6: ENOB

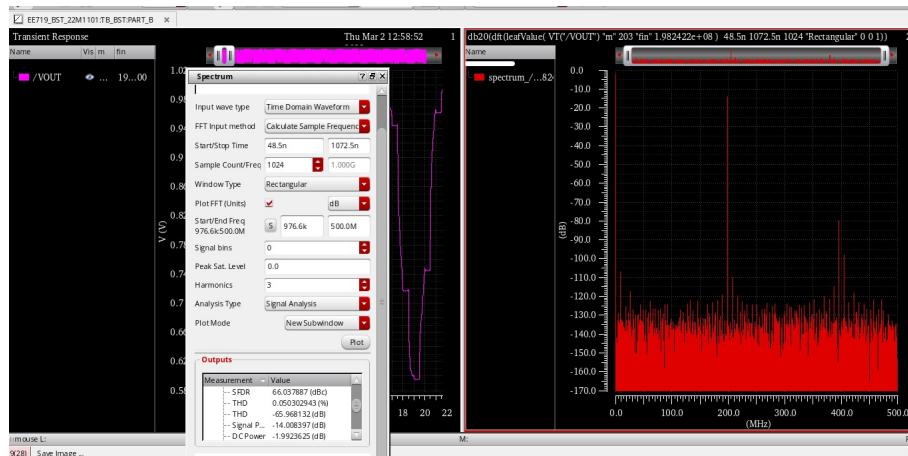


fig7 : THD

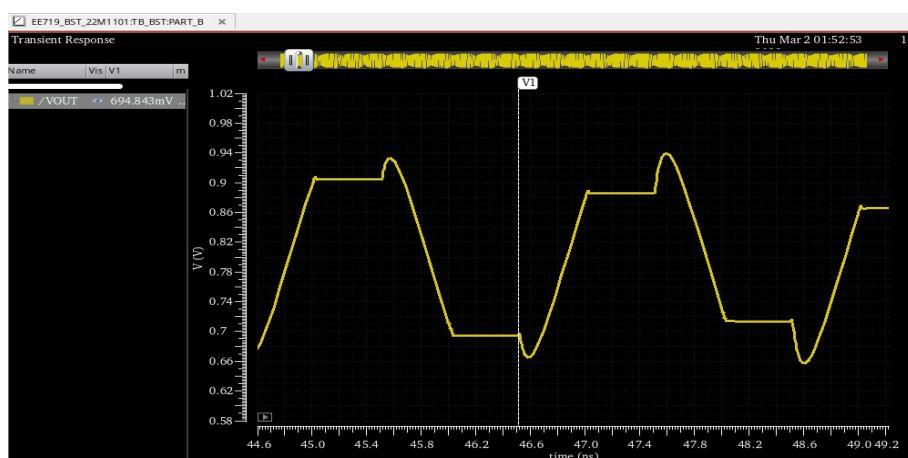


fig8: Output at fin=Fs/2

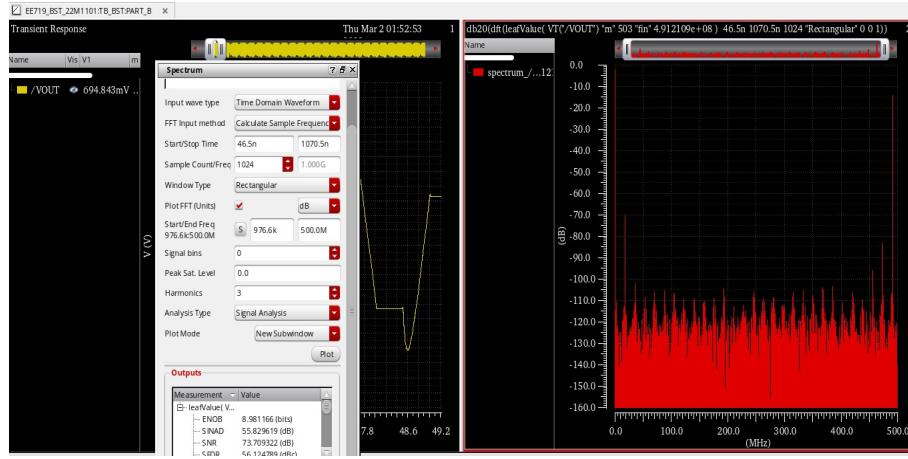


fig9: ENOB

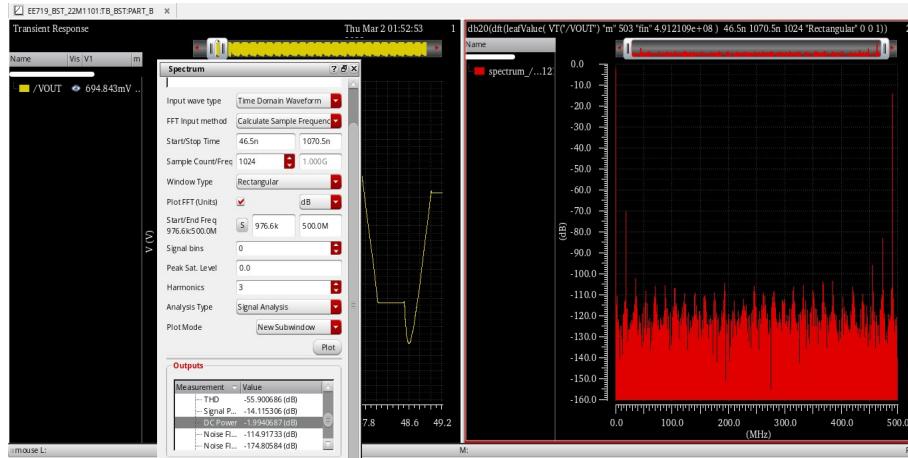


fig10 : THD

Parameter	M2	M4
Width(um)	4	4
Length(nm)	45	45

Table 3: Parameter Values

0.1.3 Disabling Bootstrapping

I Simulated the schematic shown in fig 6 in Cadence for a sine input (near frequency $F_s/5$ and $F_s/2$) using vsin from analoglib and I verified the output by performing the Transient Analysis with given Test Bench. The output is shown in fig7. Here, I chosen width of M3 & M6 as 1um in order to maintain same order of Transistors. I randomly chosen the value 1um and I checked the region of Transistor as well , it is perfectly switching between linear and

cutoff regions. I did the spectral Analysis, I got the required ENOB and THD.

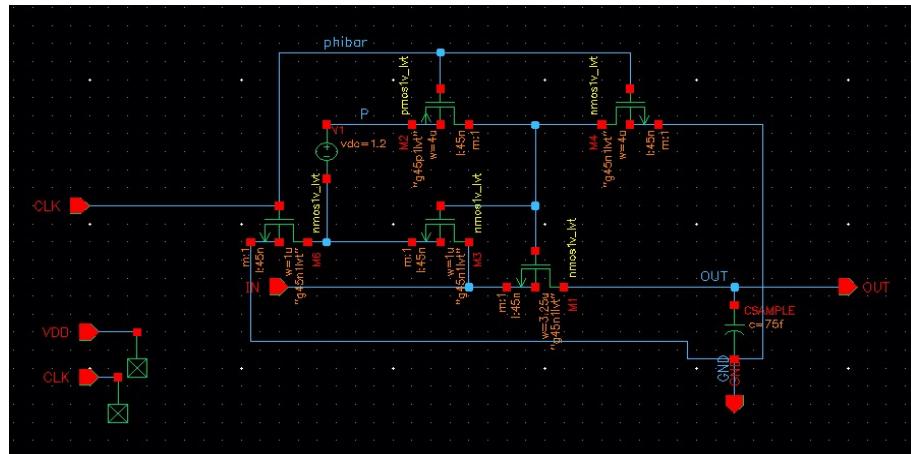


fig11: Introducing Sampling

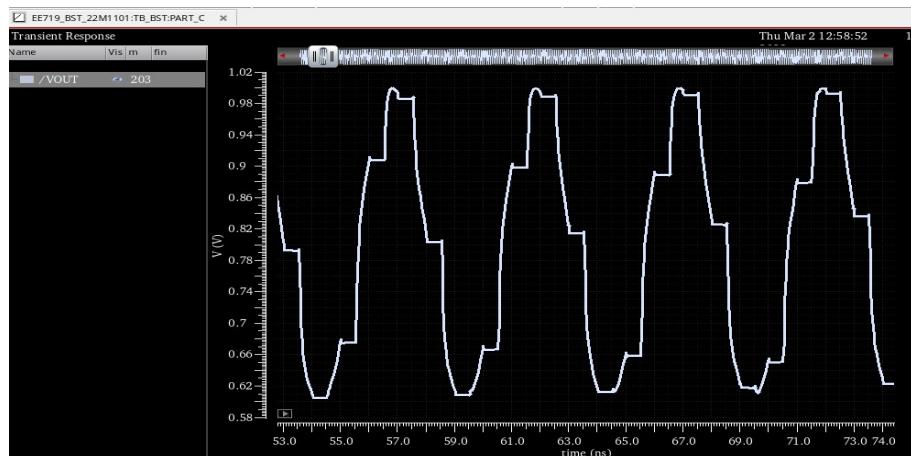
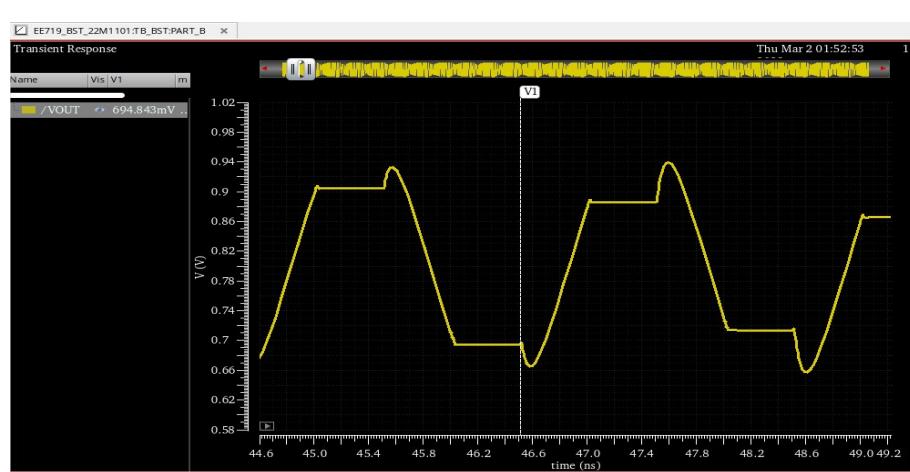
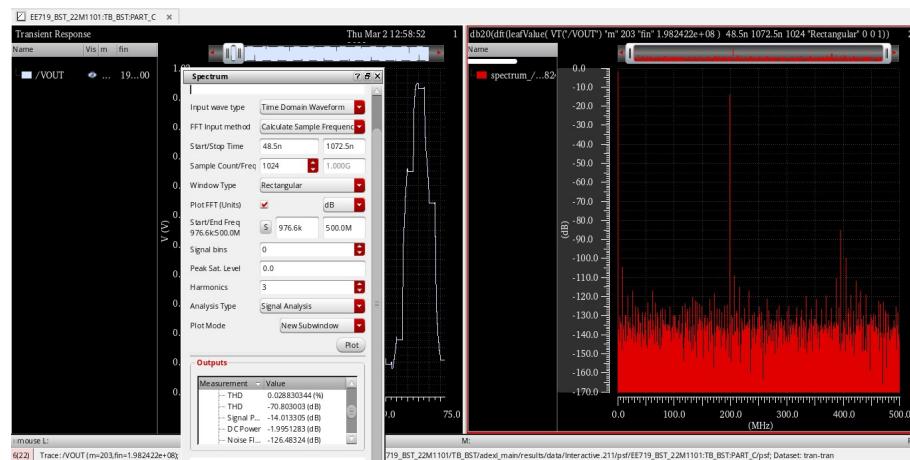
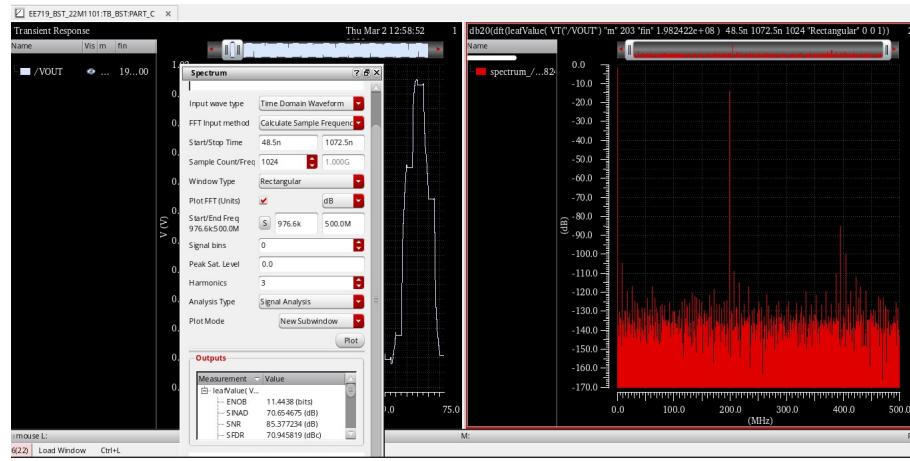


fig12: Output at fin=FS/5



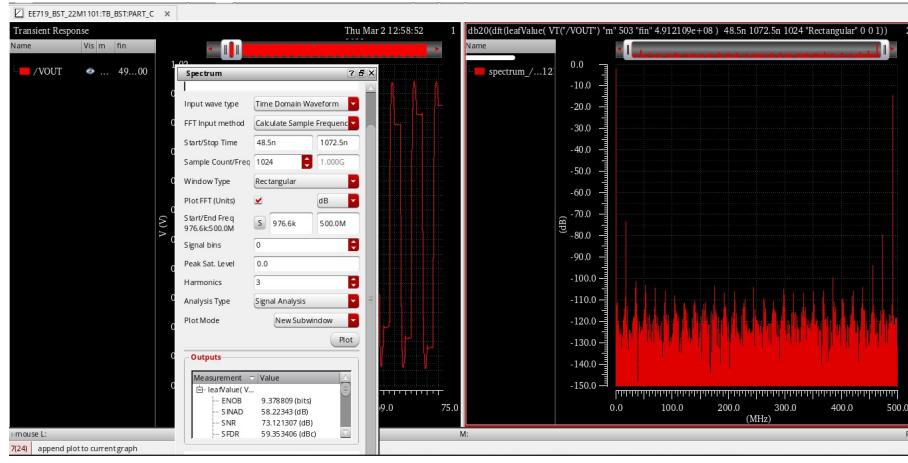


fig16: ENOB

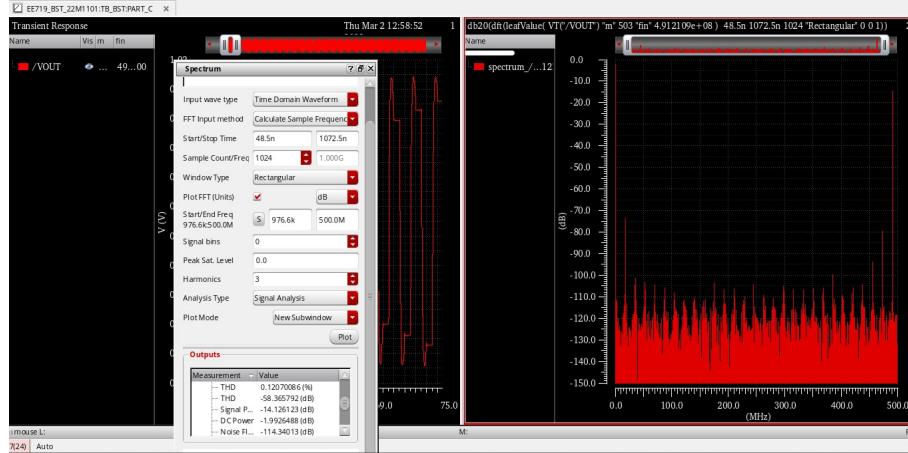


fig17 : THD

Parameter	M6	M3
Width(um)	1	1
Length(nm)	45	45

Table 4: Parameter Values

0.1.4 Introducing the Bootstrap Capacitor

I Simulated the schematic shown in fig 9 in Cadence for a sine input (near frequency $F_s/5$ and $F_s/2$) using vsin from analoglib and I verified the output by performing the Transient Analysis with given Test Bench. The output is shown in fig10. The width of M5 chosen as 1um since for 1um ,M5 is entering into saturation. I have checked for multiple values it is working fine

and for maintain the order of Transistors I selected M5 width as 1um. As per the reference paper,

$$(Ron1 + Ron2)CB < \frac{T_{Clk}}{2}$$

Now, $Ron1 = 200\Omega$, $Ron2 = 180\Omega$, $T_{Clk} = 1000ps$, therefore $CB < 1.31pF$, Here I chosen CB=0.5p F.

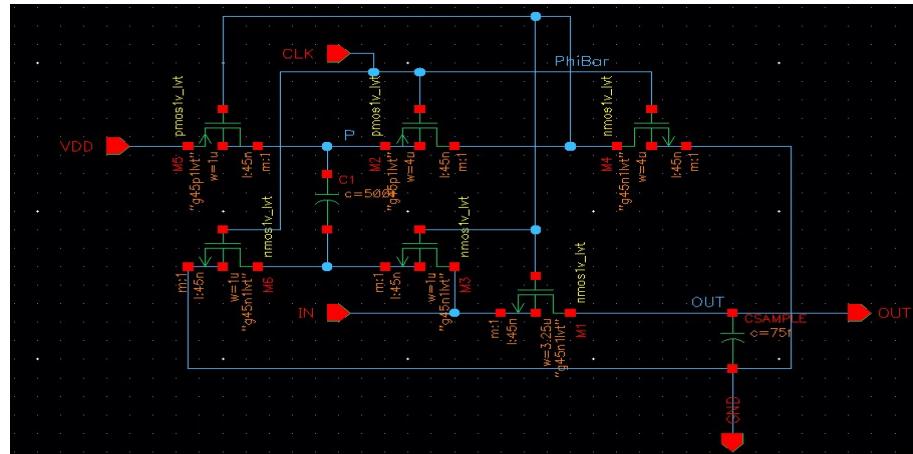


fig18: Introducing Sampling

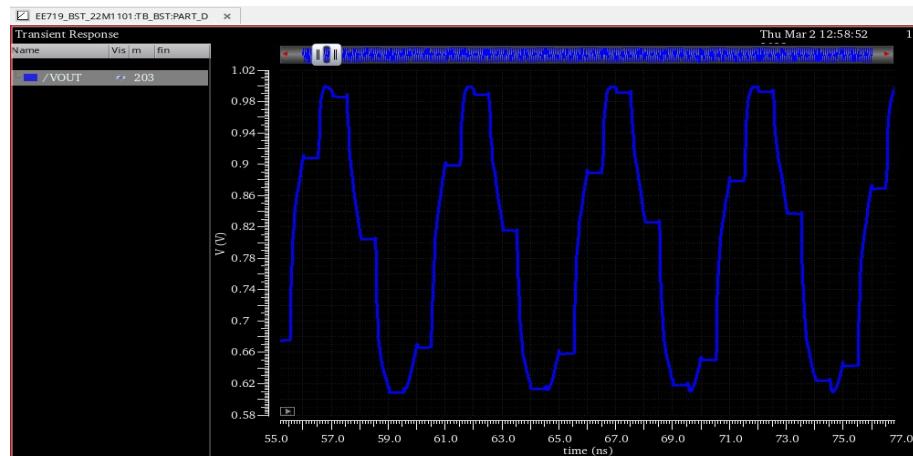


fig19: Output at fin=FS/5

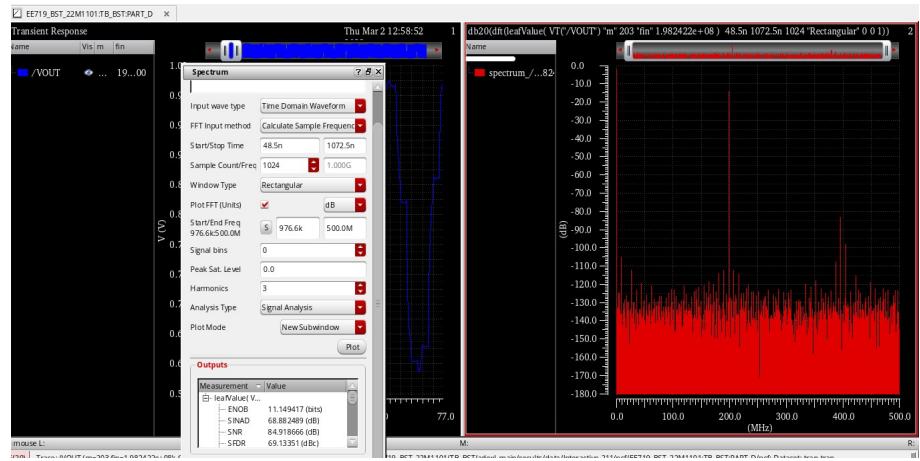


fig20: ENOB

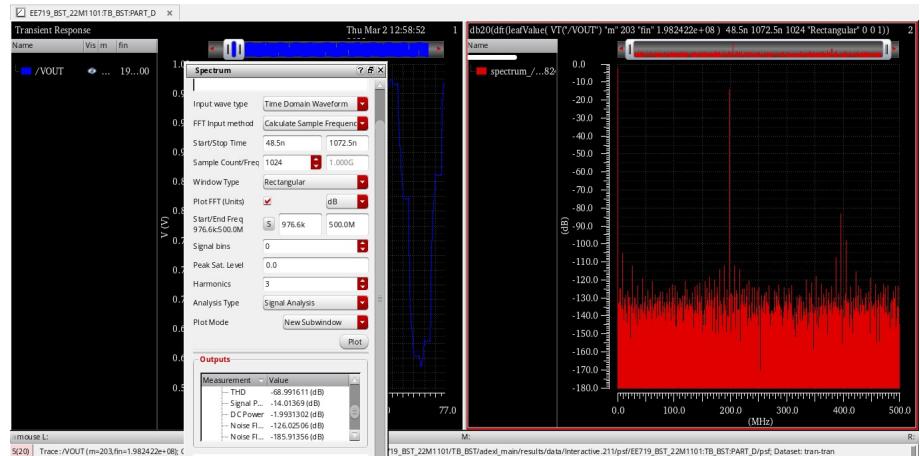


fig21 : THD

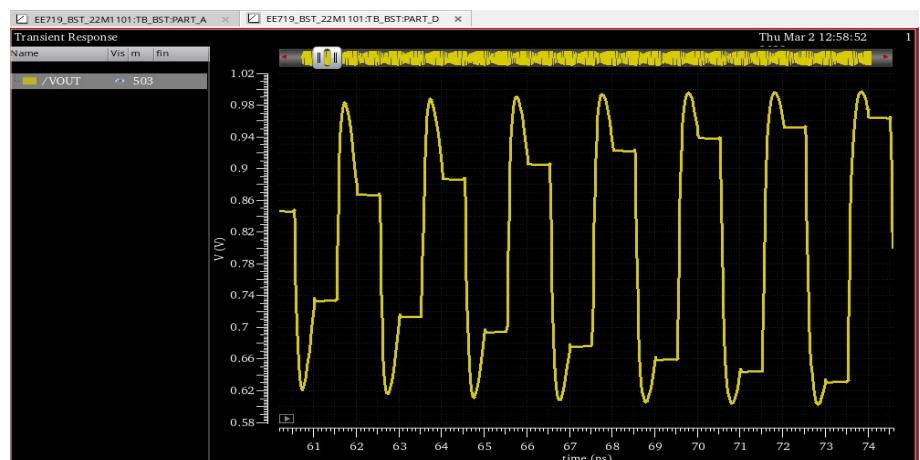


fig22: Output at fin=Fs/2

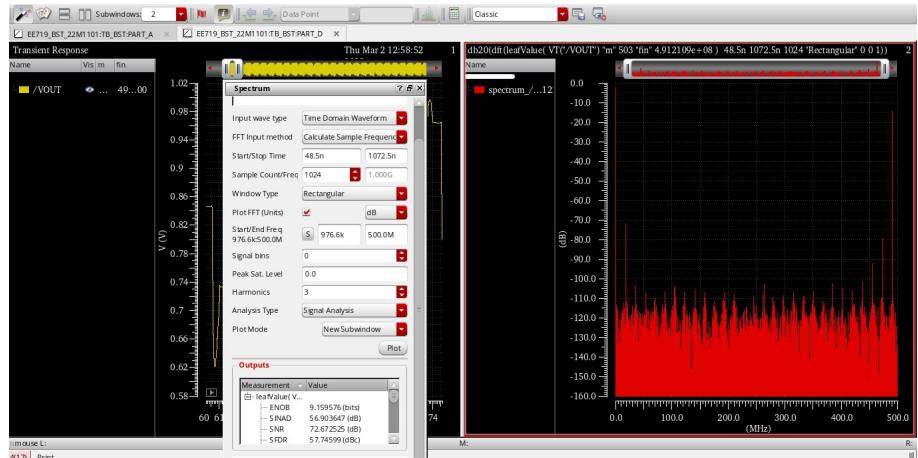


fig23: ENOB

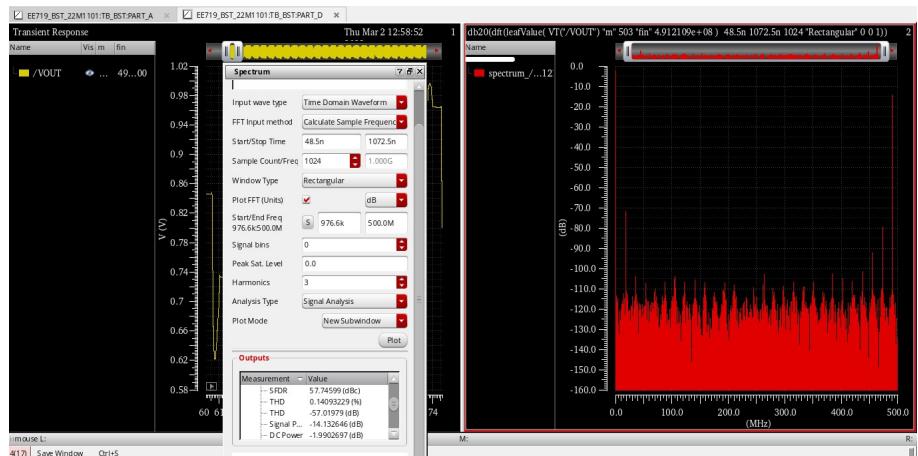


fig24 : THD

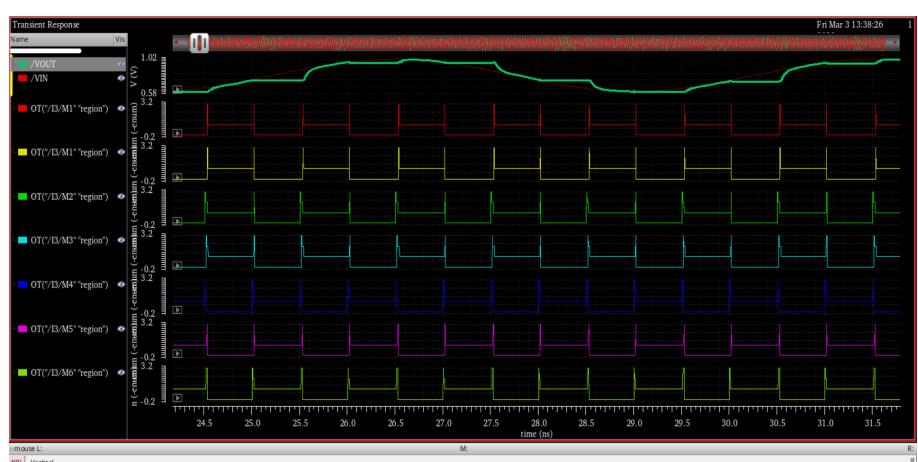


fig25 : Regions of Transistors

Parameter	M5	CB
Width	1 um	500f F
Length	45 nm	

Table 5: Parameter Values

0.1.5 Measurement of ENOB & THD

I performed the Spectral Analysis for schematics shown in fig3,fig6,fig9 for given Test Bench i.e for frequency near FS/2 and FS/5. I tabulated ENOB and THD for three figures for given two frequencies.

Sub-Part	ENOB(FS/5)(Bits)	THD(FS/5)(dB)	ENOB(FS/2)(Bits)	THD(FS/2)(dB)
0.1.2	10.66	65.96	8.98	55.90
0.1.3	11.44	70.8	9.37	58.36
0.1.4	11.14	68.99	9.16	57.02

Table 6: Parameter Values

0.1.6 Tabulation of Final Parameters

Parameter	M1	M2	M3	M4	M5	M6	C1	CB
Width(um)	3.25	4	1	4	1	1	75f F	500f F
Length(nm)	45	45	45	45	45	45		

Table 7: Final Parameters

0.1 Design Specifications

The Design of a Comparator using Storm Arm Latch. The specifications for the comparator design are listed in Table 1.

Parameter	Value
Number of bits (N)	6
Supply Voltage (VDD)	1.2V
Input Voltage Swing (VFS)	0.6 - 1.0V
Temperature (T)	300K
Sampling Frequency (Fs)	1.0 GHz
Clock Rise, Fall times (Tr, Tf)	10 ps
$3\sigma_{offset}$	2.5 mV
Power Consumption	300 uW

Table 1: Design Specifications

0.1.1 Design Procedure of Comparator

I Simulated the Test Bench which is shown in fig 4 in Cadence for a Ramp input using vpwl from analoglib. This Test Bench consists Strong Arm Latch(Core of Comparator), RS Buffer, Output Buffer which are shown in fig 1,2,3 respectively. I verified the output by performing the Transient Analysis with given Test Bench with default values of Widths (120 nm) & Lengths (45 nm). I got the maximum offset of 30mv. So, I started calculating the widths of differential pair transistors by taking reference2. In which Change in threshold voltage is given by

$$\Delta_{Vth} = \frac{A_{Vth}}{\sqrt{WL}}$$

Since $\Delta_{Vth} = \frac{\Delta}{2}$, $\Delta = \frac{V_{FS}}{2^N}$ where $V_{FS} = (1 - 0.6) = 0.4$ and $N = 6$
Given, $A_{Vth} = 4.6mv - um$ and $\frac{\Delta}{2} = 3.125mV$. On Solving, we get

$$WL = 2.1667um^2$$

By taking $L = 65nm$, I get

$$W = 33.35um$$

The tail transistor M_7 in Figure 1 must draw sufficient current for the given values $V_{GS7} = V_{DD}$ and $V_{DS7} = V_{inCM} - V_{GS1,2}$ where V_{inCM} denotes the input common-mode (CM) level. With $V_{inCM} = 0.8V$ and $V_{GS1,2} = 0.35V$ and we have $V_{DS7} = 0.15V$. Hence device operates in the deep triode region.

The circuit provides gain before M3 and M4 turn on, we expect that the offset of this pair is reduced when referred to the main input. Thus, I_{D1} and

I_{D2} entirely flow through M_3 and M_4 , respectively, as if these transistors were absent. The offset contributed by this pair is therefore negligible unless the circuit's capacitances are taken into account. As discussed later in this section, the threshold mismatch between M_3 and M_4 is divided by a factor of 3–5 in typical designs.(This paragraph is taken from reference 2)

Now I select $W_{3,4} = 10\mu m$ for now,I again simulated the circuit but I'm unable to get the required offset value. So, as per the paper I changed the widths of M_3, M_4, M_5, M_6 to 4 um & then I simulated the circuit , This time there is small decrement in power but still offset is larger than required value. Then, I changed the values of widths of transistors which are acts as switches to 700nm but still I'm unable to get the required offset value.

Iteration	Parameter	Expected	Experimented	Changes in Circuit
1	σ_{Offset}	2.5 mV	15 mV	No change
2	σ_{Offset}	2.5 mV	5 mV	Diff pair widths to 30 um
3	σ_{Offset}	2.5 mV	3.54 mV	Tail T_x width to 2um
4	σ_{Offset}	2.5 mV	3.67 mV	Latch T_x widths to 4 um
5	σ_{Offset}	2.5 mV	3.26 mV	Switch (T_x widths to 0.3 um)
6	σ_{Offset}	2.5 mV	2.68 mV	Diff pair widths to 90 um
7	σ_{Offset}	2.5 mV	2.54 mV	Switch T_x widths to 0.7 um
8	σ_{Offset}	2.5 mV	2.44 mV	Tail T_x Width to 4 um

Table 2: Results with Changes in Core

I added only some iterations in the above table , but approximately I taken 10-15 iterations to get the final result (offset in required in range). Below I added the schematics of comparator core, RS buffer, Output Buffer, Test Bench.

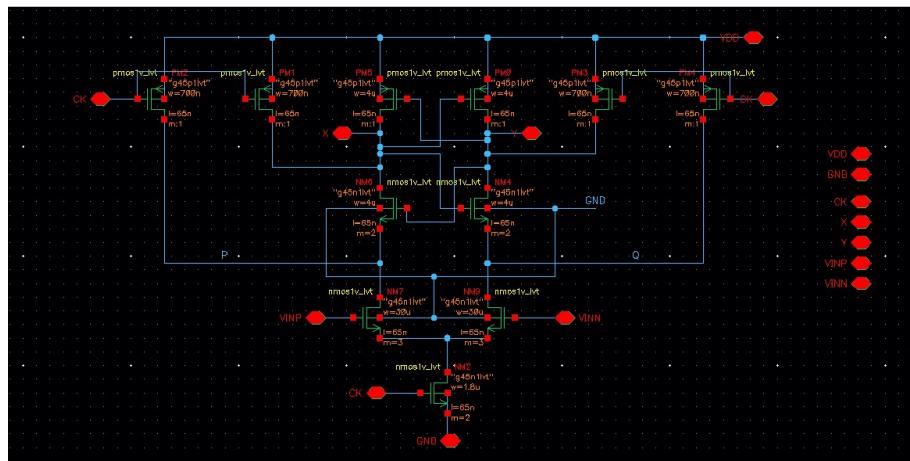


fig1: Strong Arm Latch

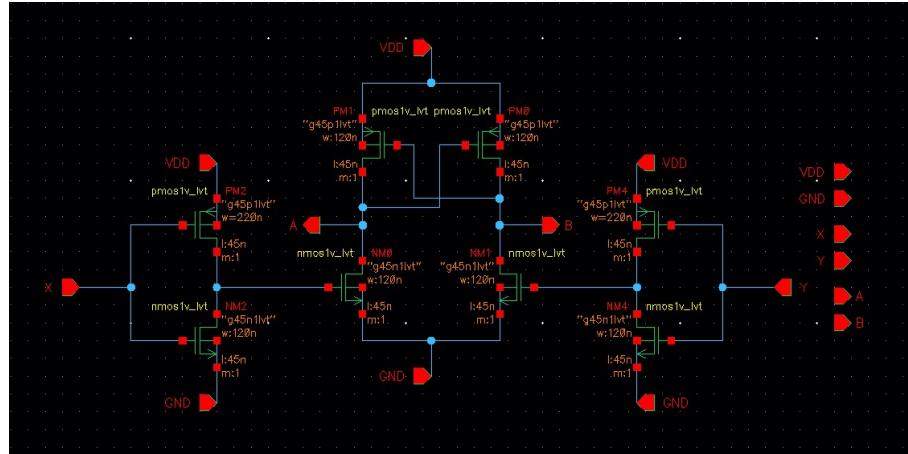


fig2: RS Latch

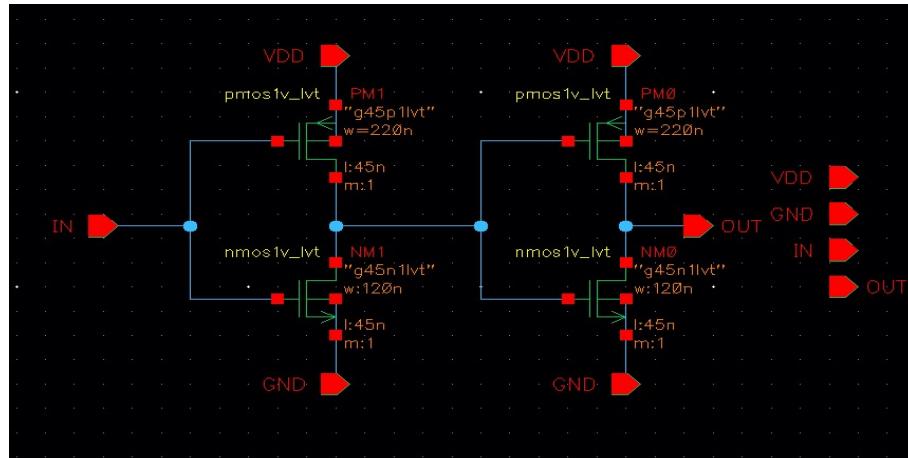


fig3: Output Buffer

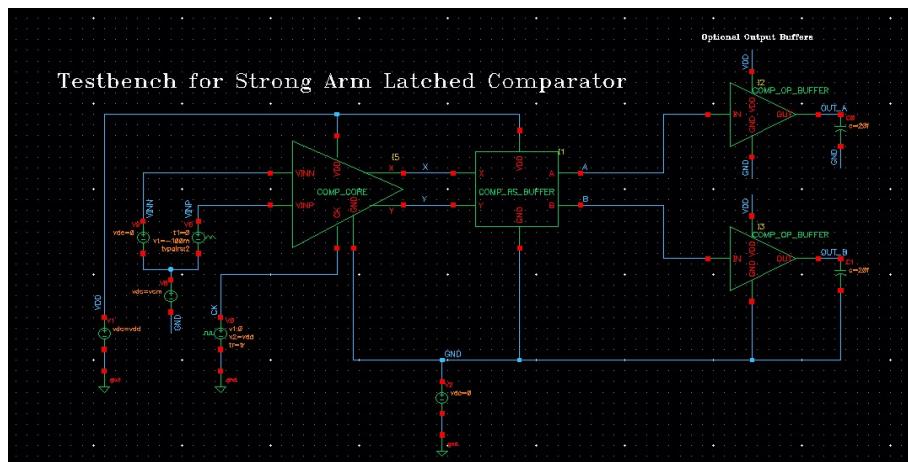


fig4: Test Bench

Now In the below tables , I added Comparator Transistor sizes and RS Latch Transistor sizes.

Parameter	M1	M2	M3	M4	M5	M6	M7	S1	S2	S3	S4
Length(nm)	65	65	65	65	65	65	65	65	65	65	65
Finger Width(um)	1	1	4	4	4	4	1.8	0.7	0.7	0.7	0.7
Number of Fingers	30	30	1	1	1	1	1	1	1	1	1
Number of Multipilers	3	3	2	2	1	1	2	1	1	1	1
TotalWidth(um)	90	90	8	8	4	4	3.6	0.7	0.7	0.7	0.7

Table 3: Comparator Transistor Sizes

Parameter	M11	M12	M13	M14	Wp	Wn
Width(um)	0.12	0.12	0.12	0.12	0.22	0.12
Length(nm)	45	45	45	45	45	45

Table 4: RS Latch Transistor Sizes

0.1.2 Transient Outputs

Using the testbench provided for the comparator, I added necessary intermediate outputs as required by Keeping one of the inputs constant at the common-mode voltage, and providing a ramp at the other input with a ramp-rate of 1 mV per cycle, simulated for a few clock cycles. Those intermediate outputs are listed below which are coming after sevaral iterations as shown below.

In figure 5 , if you observe Waveforms, When clock is low P,Q,X,Y are precharged to VDD and when Clock is high, X slowly decreases to some value and then charged to VDD but y fully decreases to Zero, As a result $Out_A = 1, Out_B = 0$.

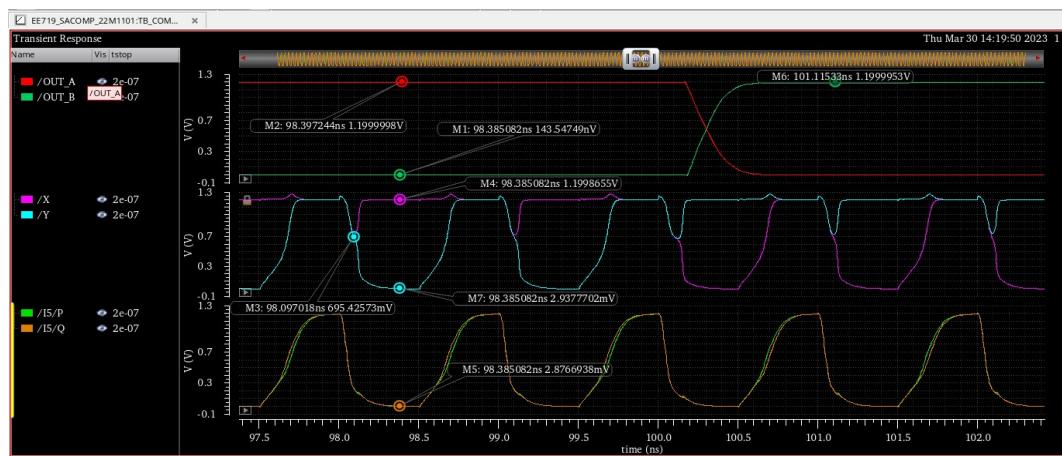


fig5: Decision is zero in Output B

In figure 6 , if you observe Waveforms, When clock is low P,Q,X,Y are precharged to VDD and when Clock is high, X switche from 1 to 0 where as Y switches from 1 to 0 ,As a result Out_A , Out_B will switches from 1 to 0 and 0 to 1 respectively.

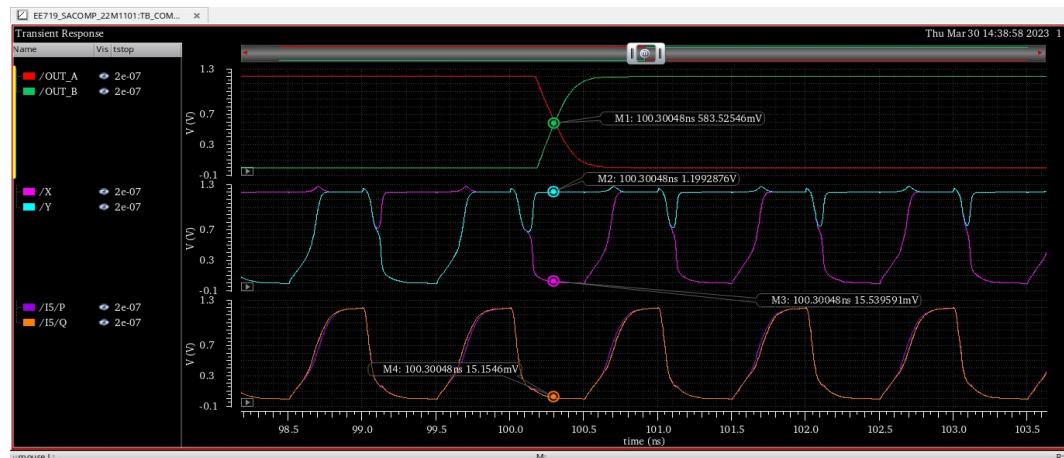


fig6: Transition from zero to one occurs in Output B

In figure 7 , if you observe Waveforms, When clock is low P,Q,X,Y are precharged to VDD and when Clock is high y slowly decreases to some value and then charged to VDD but X fully decreases to Zero, As a result $Out_A = 0$, $Out_B = 1$.

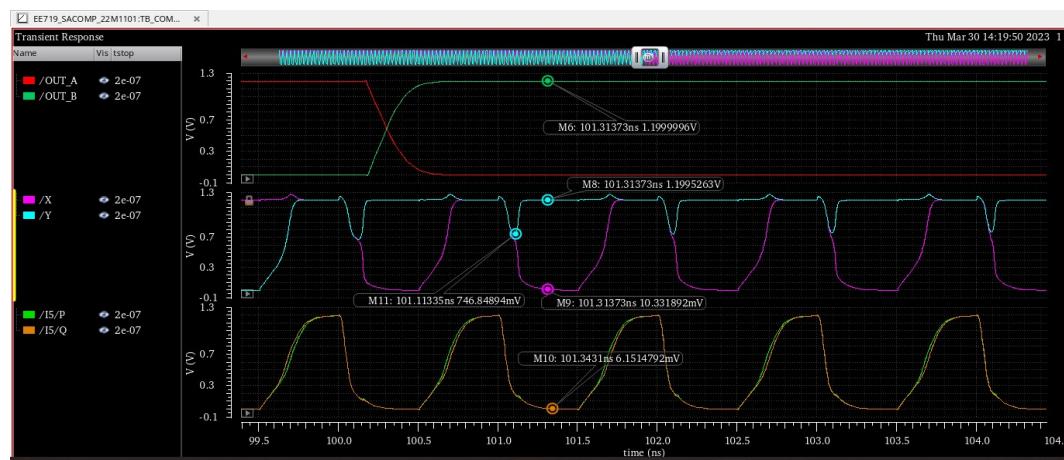


fig7: Decision is One in Output B

Figure 8 gives the histogram of power , in which the range of the power is 238 to 274 uw which is also desirable.

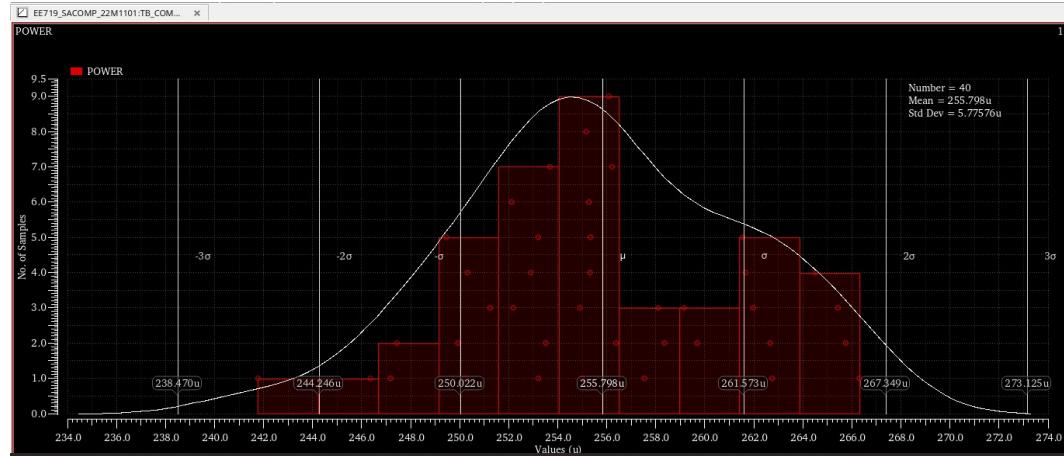


fig8: Histogram of Power

Figure 9 tells about the Histogram(Bar graph) of offset. By waveform $\sigma_{Offset} = 814.712\text{uv}$ and $3\sigma_{Offset} = 2.44\text{mv}$ which is desirable.

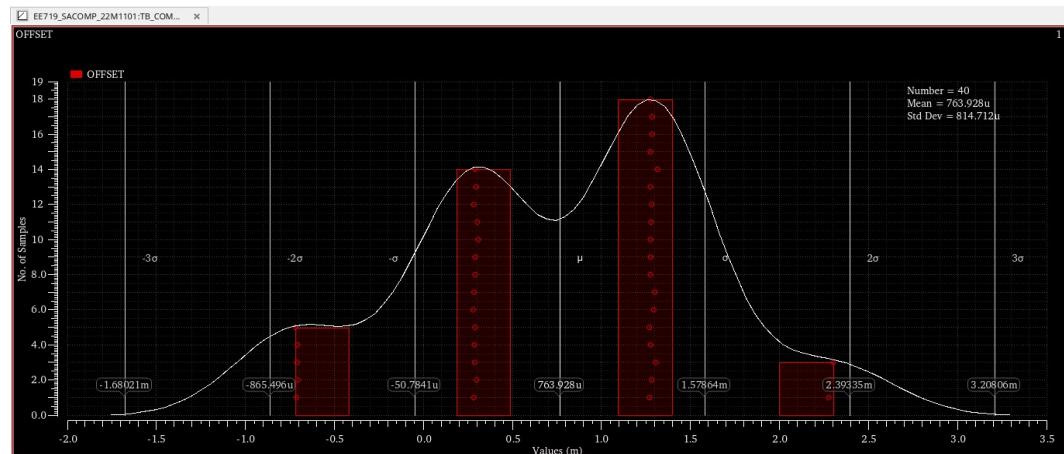


fig9: Histogram of Offset

0.1.3 Conclusion

Finally I designed a Comparator with given design specifications and I met all the required specifications.

0.1 Design Specifications

I already designed a sample-and-hold circuit and a comparator. I will use a resistor ladder to create the references and interface my switch and comparator blocks with an encoder and ideal DAC, hence completing the flash-ADC design. This part of the project involves testing of my switch and comparator designs in the full ADC setup. So, I added my BST & Comparator in the given Flash ADC Schematic it was shown in fig 1. The following specifications are to be met:

Parameter	Value
Number of bits (N)	6
Supply Voltage (VDD)	1.2V
Input Voltage Swing (VFS)	0.6 - 1.0V
Temperature (T)	300K
Sampling Frequency (Fs)	1.0 GHz
Clock Rise, Fall times (Tr, Tf)	10 ps
ENOB	> 5.2Bits
SFDR	> 42dB
INL _{max}	< 1LSB
DNL _{max}	< 0.6LSB

Table 1: Design Specifications

0.2 Simulation of ENOB & SFDR

I Simulated the Test Bench which is shown in fig 2 in Cadence for a sinusoidal input of frequency $\frac{F_S}{2}$ using vsource from analoglib. This Test Bench consists ADC and DAC . I verified the output by performing the Transient Analysis with given Test Bench without changing any values of Comparator and Boot-strapped switch. After that I done the spectral analysis but I didn't get the required values. So, I changed the Hold capacitance of the Switch from 75f F to 325f F. Then again I did the Transient analysis and spectral analysis , This time I get the required values of ENOB and SFDR and those graphs are shown below. Then I repeated the same procedure for $f_{in} = \frac{F_S}{5}$ and I added the respective graphs below. I Marked the fundamental and the subsequent harmonic frequency peaks in the both spectrum's.



fig1: Flash ADC Schematic

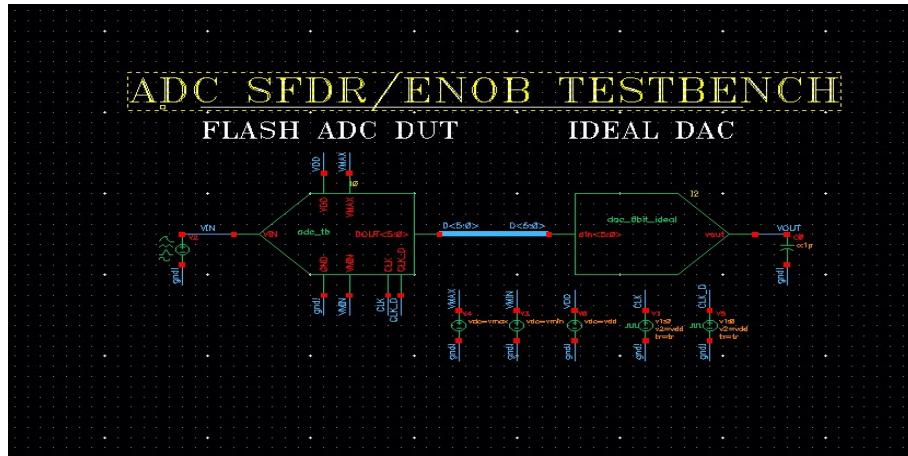


fig2: Test Bench For ADC SFDR & ENOB

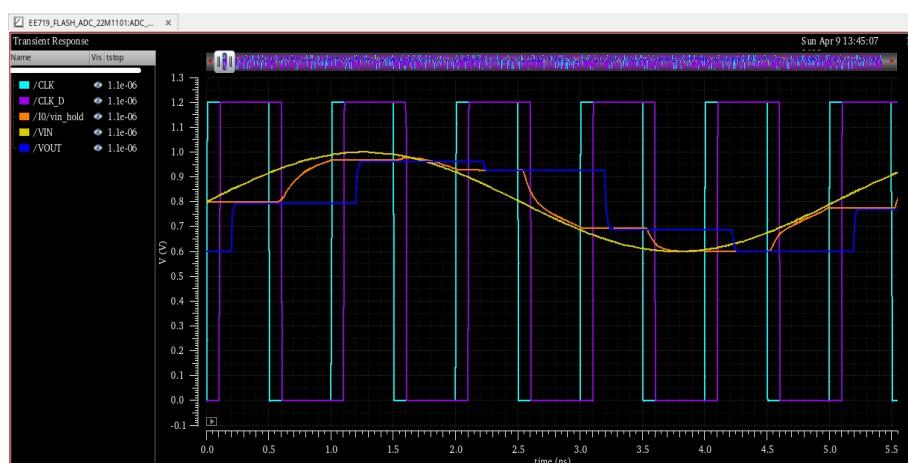


fig3: Output of ADC for $f_{in} = \frac{F_S}{5}$

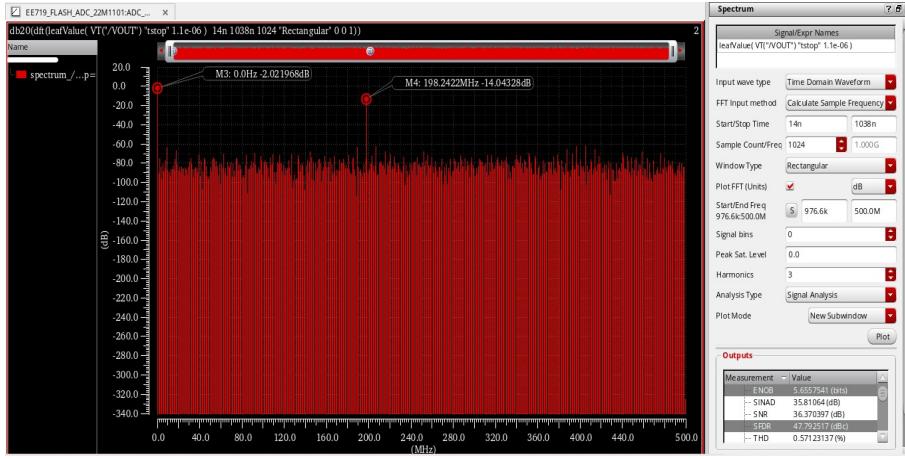


fig4: Spectrum(1024 point) of ADC for $f_{in} = \frac{F_s}{5}$

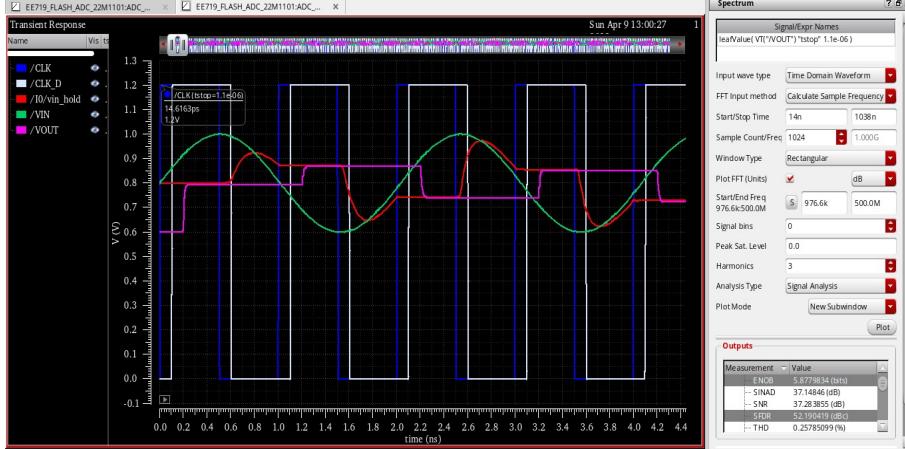


fig5: Output of ADC for $f_{in} = \frac{F_s}{5}$

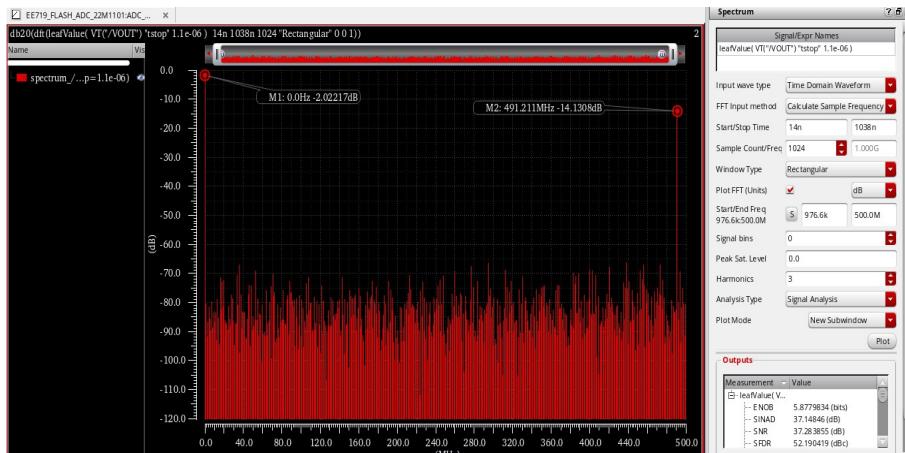


fig6: Spectrum(1024 point) of ADC for $f_{in} = \frac{F_s}{2}$

Parameter	$f_{in} = \frac{F_S}{2}$	$f_{in} = \frac{F_S}{5}$
ENOB(Bits)	5.656	5.877
SFDR(dB)	47.795	52.19

Table 2: ENOB & SFDR

0.3 Simulation of INL & DNL

Using the testbench provided for the calculation of INL and DNL, I performed Transient Analysis for the given ramp binary input. I verified Output that is the superimposition of ramp input & ADC stair case output which was shown below. Then, I calculated the the offset, full scale error, gain error and those values are tabulated below.

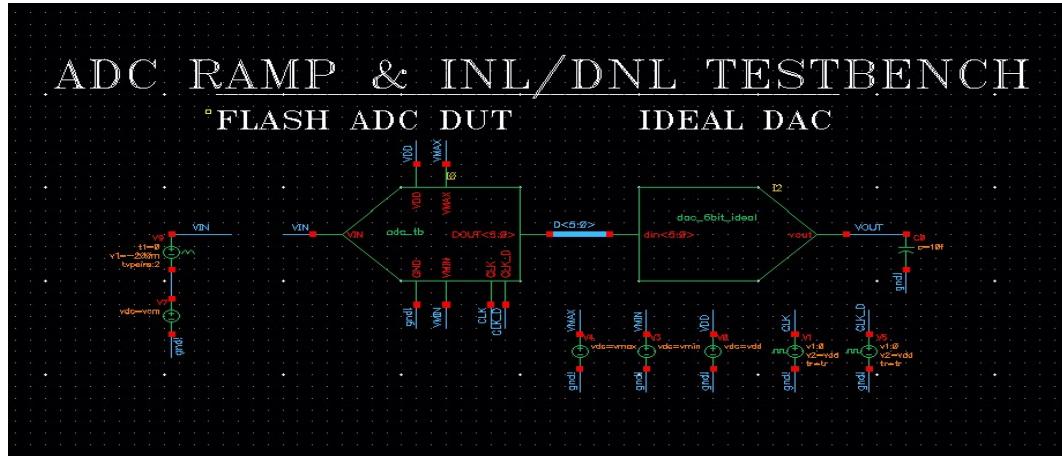


fig7: ADC INL & DNL Test Bench

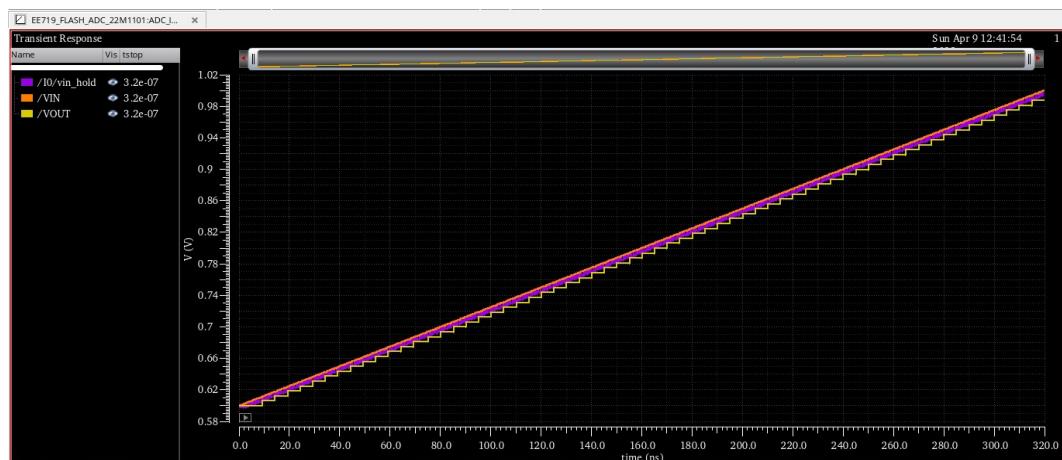


fig8: Superimposition of Ramp Input and ADC output

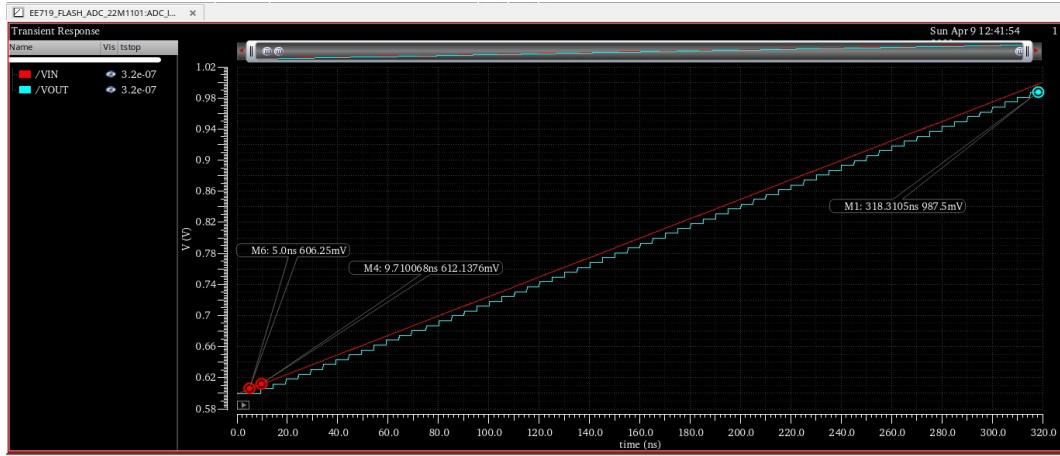


fig9: Calculation of Offset & FS Error

Next , From above above we can see that first transition occurs at 0.612mv but in ideal case it should occur at 0.0625mv because $V_{LSB} = \frac{V_{FS}=0.4}{64} = 6.25mv$, so

$$Offset_{Error} = 0.612 - 0.0625 = 0.575mv$$

Now, Full scale Transition should be at $636.25m + 0.6 = 0.99375V$ but my full scale value at 0.987V , so

$$FullScale_{Error} = 0.99375 - 0.987 = 6.25mv$$

Hence ,

$$Gain_{error} = FS_{Error} - Offset_{Error} = 0.5mv$$

Parameter	Value
Offset	0.92 LSB = 5.75 mV
FS Error	1 LSB = 6.25 mV
Gain Error	0.08 LSB = 0.5 mV

Table 3: Offset, FS Error, Gain Error

I have added a table for INL & DNL for first 10 transitions but originally there are 63 transitions. Since it takes so much time I added only few values which are required for INL & DNL Calculations. If you observe in these 10 transitions

$$INL_{Max} = 0.39LSB$$

and

$$DNL_{Max} = -0.22LSB$$

Input Code	Output(mV)	Output(LSB)	O/p w/o off	DNL(LSB)	INL(LSB)
0	612	97.93	92.18		0
1	618.25	98.95	93.20	0.2	0.2
2	624.53	99.82	94.07	-0.13	0.07
3	630.78	100.92	95.17	0.1	0.17
4	637.21	101.95	96.20	0.03	0.2
5	643.25	102.87	97.12	-0.08	0.12
6	649.52	103.92	98.17	0.05	0.17
7	655.75	104.98	99.23	0.06	0.23
8	662.12	105.99	100.39	0.16	0.39
9	668.28	106.92	101.17	-0.22	0.17

Table 4: INL & DNL Calculation for single Run

Next , I did the Monte Carlo Sampling of 10 iterations for INL & DNL test bench and then exported the .CSV file into Matlab and run the given Matlab code for generating the INL and the DNL plots and those plots are shown below and Maximum INL & DNL are Marked on the plots.

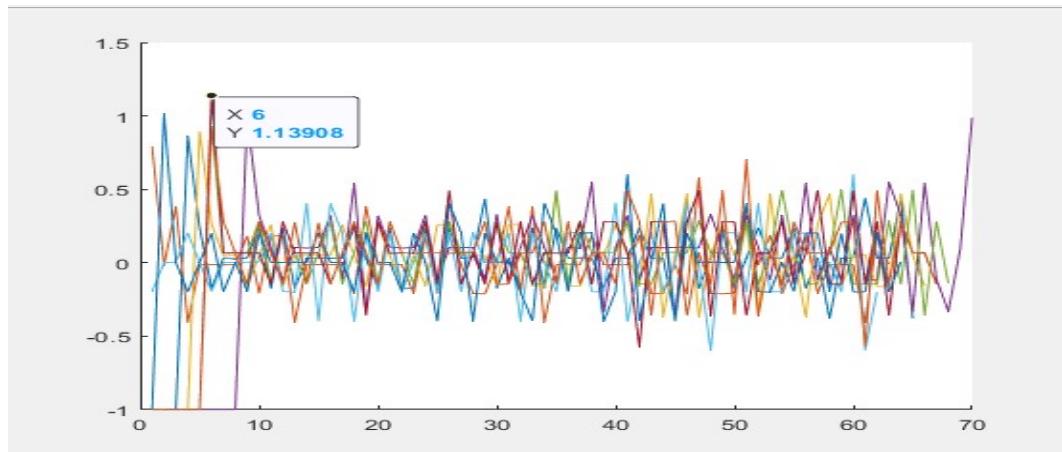


fig10: DNL Plot

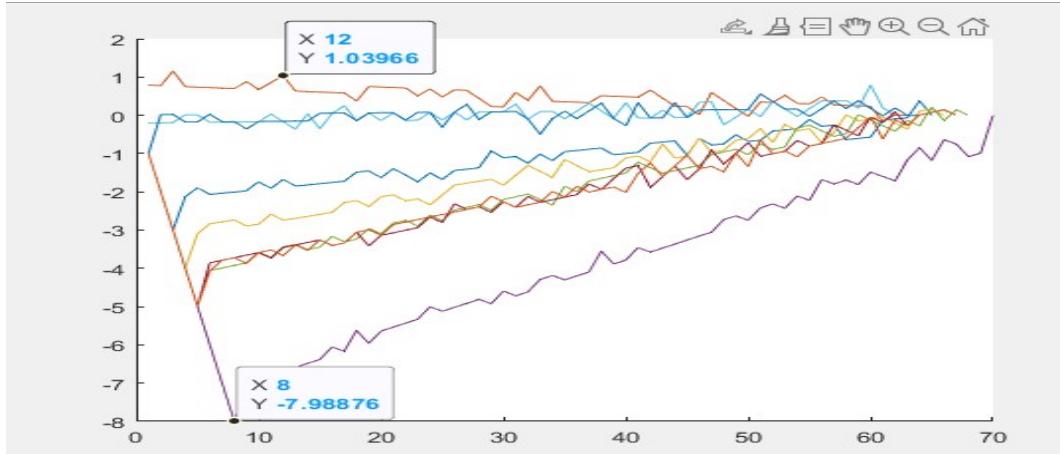


fig11: INL Plot

0.4 Layout Of Strong Arm Latch

Using the testbench provided for the calculation of INL and DNL, I performed Transient Analysis for the given ramp binary input. I verified Output that is the superimposition of ramp input & ADC stair case output which was shown below. Then, I calculated the the offset, full scale error, gain error and those values are tabulated below.

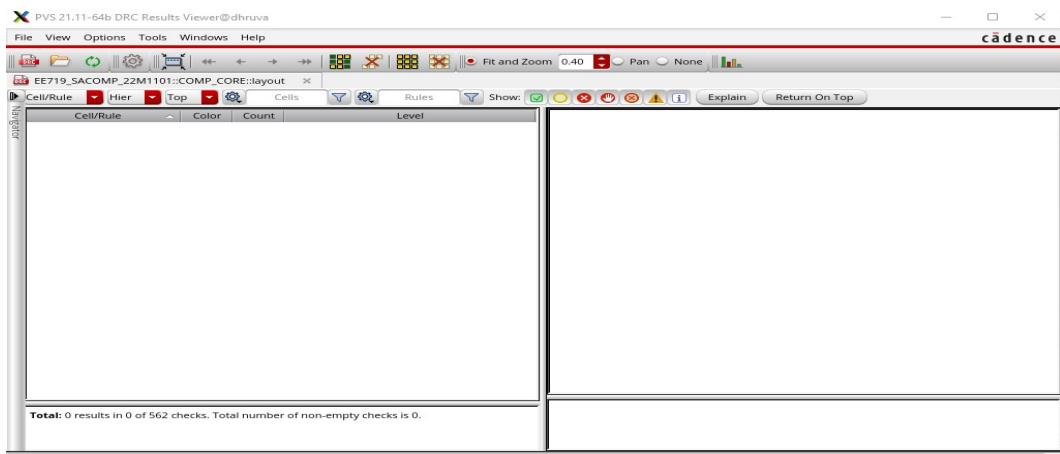


fig12: DRC Check



fig13: LVS Check

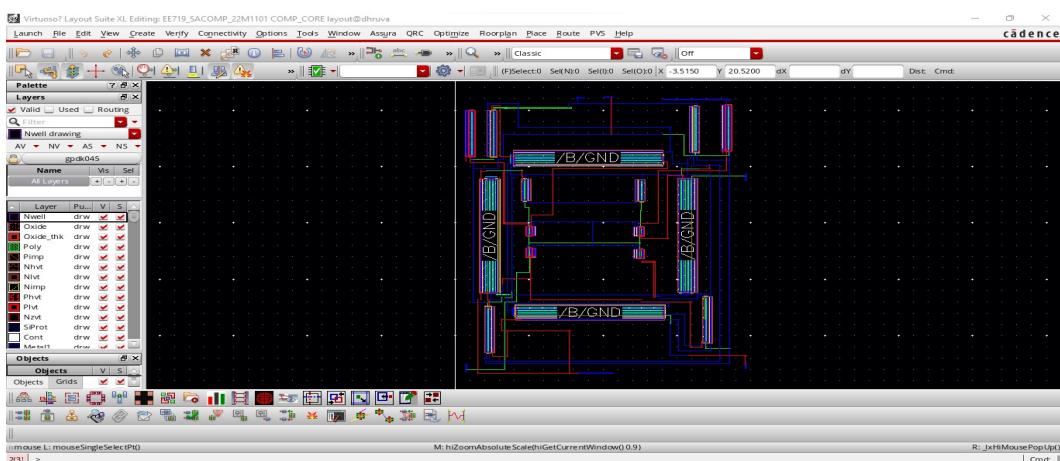


fig14: Layout Image of Comparator



fig15: Successful av extraction

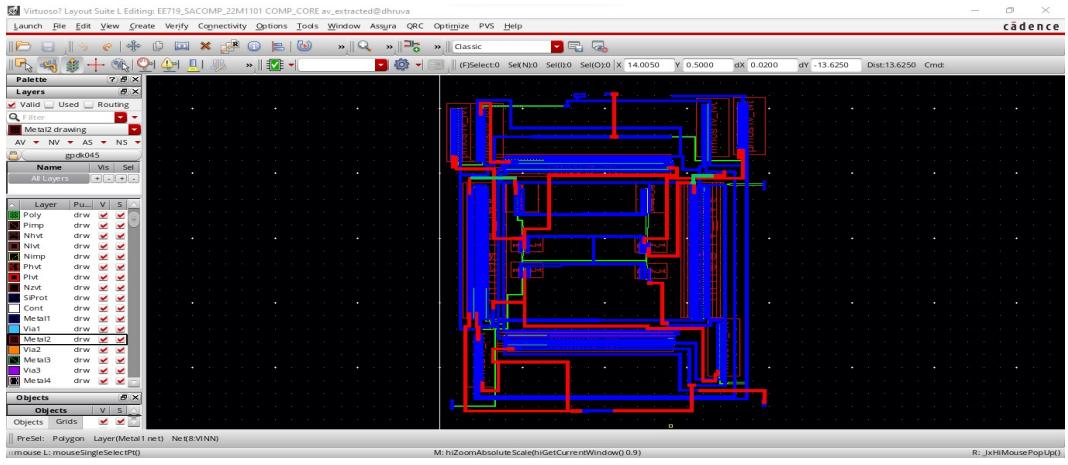


fig16: High Resolution Image of Layout of Comparator

0.4.1 Post Layout Simulation

In this Part I did the post-layout extractions (RC) by Using the av extracted view of the strong-arm latch and then I Performed the transient analysis with a sinusoidal input of frequency $F_s/2$ (ensure coherent sampling) and plotted 1024 point FFT Spectrum. I Marked the fundamental and the subsequent harmonic frequency peaks in the spectrum and I added a zoomed image of the transient simulation showing the input signal, switch output, the output of the DAC along with the clocks and I Tabulated the simulated dynamic performance characteristics (SNDR, SFDR, ENOB) before extraction (as done in 1(b)) and after extraction.

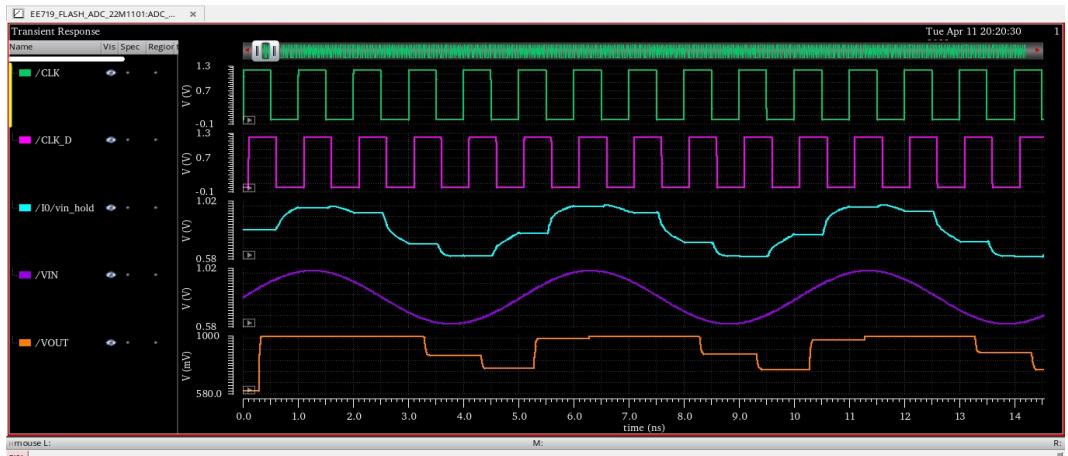


fig17: Output after av Extraction

From the Spectrum ,I measured ENOB & SFDR but those values doesn't meet the required specifications. I'm adding a table those are memory based

values which came in my first run because I don't have slots to recheck the Layout & Schematic and Rerun the Simulations to get the required ENOB & SFDR. I forgot to take screen shot of this spectrum & my history was deleted & there is no slot for rerun the simulation.

Parameter	$f_{in} = \frac{F_S}{2}$
ENOB(Bits)	3.78
SFDR(dB)	29

Table 5: ENOB & SFDR after Post Layout