

Introduction:

Operational Transconductance Amplifiers (OTA) are the major building blocks of many electronic circuits. ADCs, sensor signal processing and other applications use OTAs. Super Class AB Recycling Folded Cascode OTA combines many techniques to improve the performance of basic folded cascode (FC) OTA by current recycling (Recycling Folded Cascode, RFC) and by combining power efficient super class AB OTA to get super class AB RFC OTA. The class AB RFC OTA provide better slew rate and bandwidth while consuming low quiescent power. In this project we design a super class AB RFC OTA for given specifications.

Design Specifications:

The objective is to design a super class AB RFC OTA as per following specifications given in Table 1.

| Parameter | Specification |
|----------------------------|---|
| Load Capacitance | 70 pF |
| Slew Rate | $\geq 0.2 \text{ V}/\mu\text{s}$ |
| Settling Time | $\leq 200 \text{ ns}$ |
| DC voltage gain | $\geq 60 \text{ dB}$ |
| Phase Margin | $\geq 60 \text{ Degree}$ |
| Unity Gain Frequency (UGF) | $\geq 6 \text{ MHz}$ |
| CMRR | $\geq 90 \text{ dB}$ |
| PSRR | $\geq 70 \text{ dB}$ |
| Input noise spec. | $\leq 50 \text{ nV/V Hz density@1 MHz}$ |
| Static Power Consumption | $\leq 150 \mu\text{W}$ |

Table 1: Target Design Specifications

1.a Design Flow: Fully Differential OTA

To get started with initial values of widths we first perform pen and paper calculations. The design flow and the design equations used, taking target specifications as constraints, are listed below along with calculations.

The design for the given circuit has been carried out based on the following assumptions

1. LCMFB resistor $R \ll r_{02b}$
2. Current mirroring ratio $K = 3$

The short circuit transconductance of single ended output OTA is given by

$$G_{mAB} = 2g_{m1a}[1 + g_{m3a}(R||r_{02b})]$$

Since in fully differential version, the currents in transistors M_{1D} and M_{2D} are copied to the output branches, the modified short circuit transconductance is given by

$$G_{mAB} = 2g_{m1a}[2 + g_{m3a}(R||r_{02b})]$$

The output resistance of OTA is given by

$$R_{O,RFC} = R_{OAB} \approx g_{m6}r_{06}(r_{02A}||r_{04A})||g_{m8}r_{08}r_{02A}$$

The gain bandwidth product(UGF) of OTA is given by

$$G.BW = \frac{2g_{m1a}}{2\pi C_L}[2 + g_{m3a}(R||r_{02b})]$$

$$\text{Power Consumption} = I_{drawn} * V_{DD} \leq 150\mu W$$

$$I_{drawn} = 5I_B \leq 84\mu A$$

$$\text{Let } I_{drawn} = 70 \mu A$$

$$\text{So we select } I_B = 14\mu A$$

$$\text{Thus, } \frac{I_B}{2} = 7\mu A$$

Assumption :- All driver transistors should be in saturation i.e. $M_{1A}, M_{1B}, M_{2A}, M_{2B}$ in saturation

$$I_D = \frac{I_B}{2} = 7\mu A$$

Let overdrive $V_{GST} = 150mV$

$$g_{m1a} = \frac{2I_D}{V_{GST}} = 0.0934 mA/V$$

$$DC \text{ Gain} \geq 60dB$$

$$DC \text{ Gain} \geq 1000$$

$$R = 10k ohm$$

Since, $R \ll r_{02b}$ thus $R||r_{02b} \approx R$

$$G_{mAB} = 2g_{m1a}[2 + g_{m3a}R]$$

$$G.BW = 0.1868[1 + g_{m3a}R]$$

$$6MHz = 0.1868[1 + g_{m3a}R]$$

$$R = 10k\ ohm$$

$$g_{m3a} = 1.3122\ mA/V$$

Hence , overdrive voltage of M_{3A} is given by

$$V_{GST} = 38.9mV \approx 39mV$$

Following are the threshold voltages , channel length modulation parameters and K values of PMOS 4T-25 and NMOS 4T-25 respectively.

$$|V_{tp}| = 0.58V , V_{tn} = 0.46V$$

$$\lambda_p = 0.036V^{-1} , \lambda_n = 0.1428V^{-1}$$

$$\mu_p C_{ox} = 21.68 \frac{\mu A}{V^2} \quad \mu_n C_{ox} = 160 \mu A/V^2$$

M1A :

$$I_D = 7\mu A = 21.68 X \frac{W}{2L} (0.163)^2$$

From the above $\frac{W}{L} = 28.7$ and $W= 17.22\mu m$ and $L = 0.6\mu m$

M3C1 :

$$\text{Let , } V_{gs} > V_{TH} + V_{gst(OV)} \quad V_{gs} \approx 0.55V \quad V_{gst} \approx 80mV \quad I_D = 7\mu A$$

$$\text{Taking these values, } \frac{W}{L} = 13.671 \quad \text{thus} \quad W_{3C1} = 8.2 \approx 8 \mu m$$

M3A :

Since current mirroring ratio is K=3

$$W_{3A} = 3 \times W_{3C1} = 24\mu m$$

M1C and Current source transistor :

$$I_D = 7\mu A , \text{ let the overdrive voltage is } V_{gst} \approx 150mV$$

to keep the transistor in saturation

$$\text{Taking these values, } \frac{W}{L} = 28.7 \quad \text{thus} \quad W_{1C} = 17.22 \mu m$$

M1D:

$$I_D = 21\mu A \quad V_S \approx 1.8V$$

Since it is the source of all other current , It should draw maximum current with minimum W/L . So, let

$$V_{gst} \approx 200mV$$

So using these values $W/L = 48.4317$ $W_{1D} = 29\mu m$

M9, M10, M7, M8 :

Since current through M1D and M2D is 1.5 times the current flowing through above transistors,

$$W = \frac{2}{3} \times 29\mu m \approx 19\mu m$$

In the design, the transistors which do not contribute to the transconductance of OTA are kept in cut-off region to reduce power consumption.

The common mode voltage is selected to be $V_{CM} = 0.65V$ and similarly $V_{CN} = V_{CP} = 0.65V$

Using above values the simulations are performed by creating the schematic

Simulation 1:

| Parameter | Obtained Value |
|--------------|----------------|
| DC gain | 61 dB |
| UGF | 16.7MHz |
| Phase margin | 53 degrees |

1.b Iterations:

Simulation 2:

To increase phase margin, LCMFB resistor R value is modified to 20Kilo ohms and obtained values are as follows. The plot for above AC analysis is as follows

| Parameter | Obtained Value |
|--------------|----------------|
| DC gain | 54 dB |
| UGF | 9.6MHz |
| Phase margin | 56 degrees |

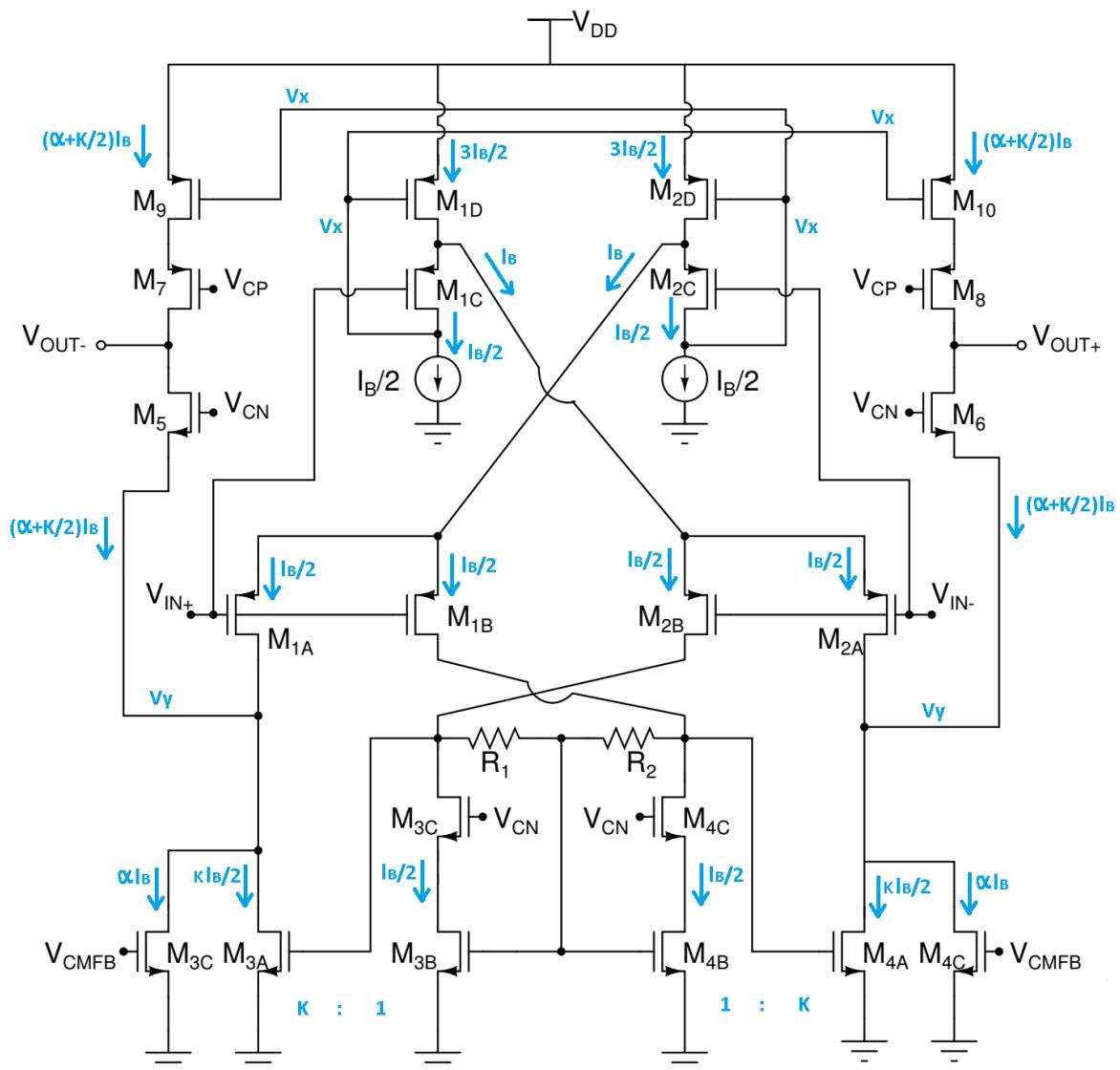
Simulation 3:

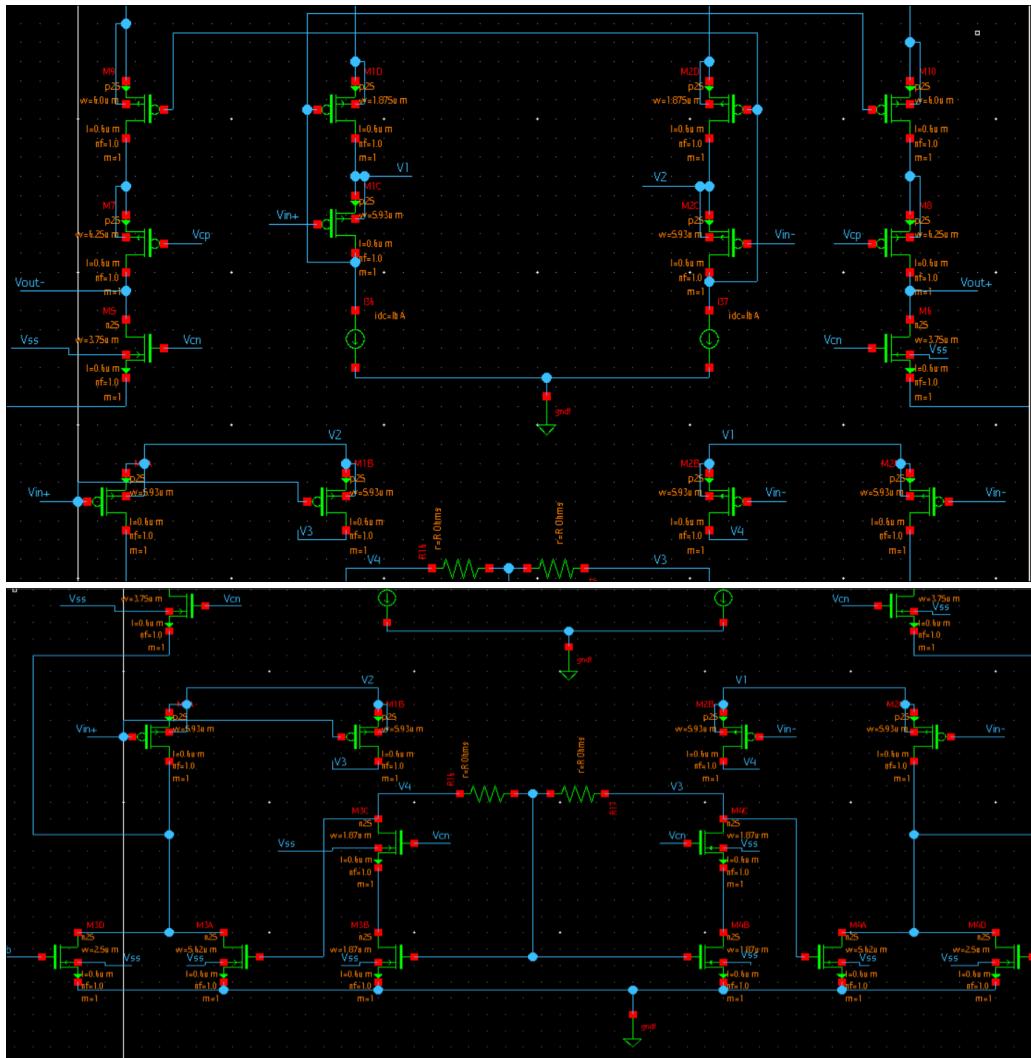
We have done a lot of iterations to get the required specifications but we reported only first 2 iteration and the last iteration. Now to improve DC gain again, keeping R value fixed at 20K,

the driver transistor widths are changed to 15um by fixing the lengths of transistor and the simulations are carried out. It resulted in the following values.

| Parameter | Obtained Value |
|--------------|----------------|
| DC gain | 67.2dB |
| UGF | 6.23MHz |
| Phase margin | 66.4degrees |

1.c Schematics of Super Class AB FD OTA





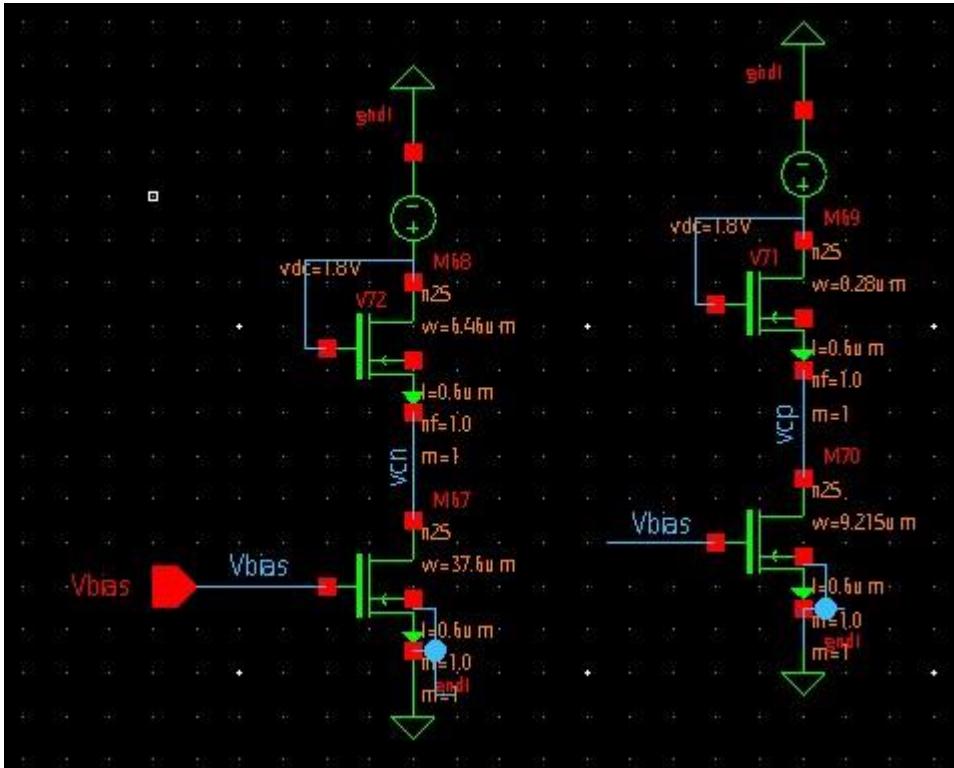
1.d Widths of Transistors:

Below table shows the aspects ratios of all the transistors for the last iteration.

| Name of the Transistor | W/L (um) |
|------------------------|----------|
| M1A, M2A | 15/0.6 |
| M1B, M2B | 15/0.6 |
| M1C, M2C | 15/0.6 |
| M1D, M2D | 8/0.6 |
| M3A, M4A | 40/0.6 |
| M3B, M4B | 8/0.6 |
| M3C, M4C | 8/0.6 |
| M3C1, M4C1 | 8/0.6 |
| M5, M6 | 28/0.6 |
| M7, M8 | 16/0.6 |
| M9, M10 | 16/0.6 |

2.a Biasing Circuit Design

To generate the bias voltages required for OTA biasing, current mirrors with $I_{ref} = 50\mu A$ were used. The V_{bias} from testbench was used. The circuit for biasing voltage generation is shown in below Figure and widths are tabulated below.



2.b Widths of Transistors

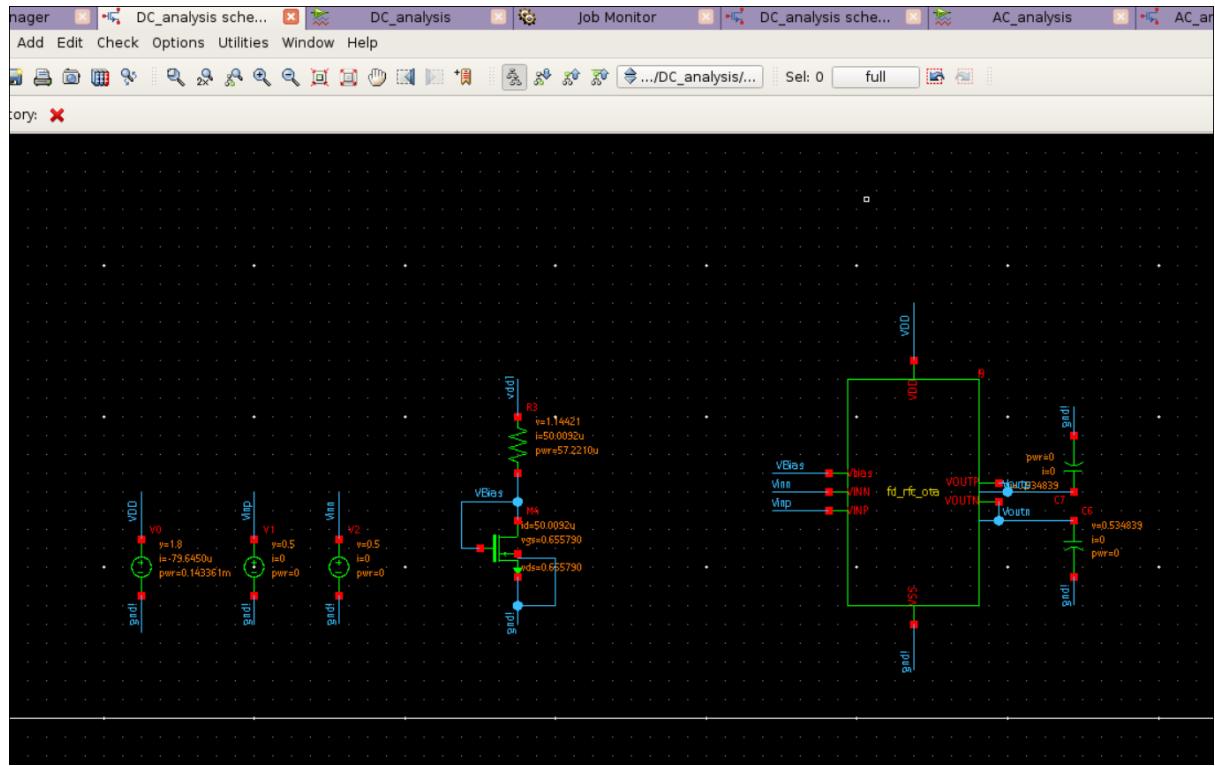
Below table shows the aspects ratios of biasing transistors.

| Name of Transistor | W/L (um) |
|--------------------|-----------|
| M67 | 37.6/0.6 |
| M68 | 6.46/0.6 |
| M69 | 0.28/0.6 |
| M70 | 9.215/0.6 |

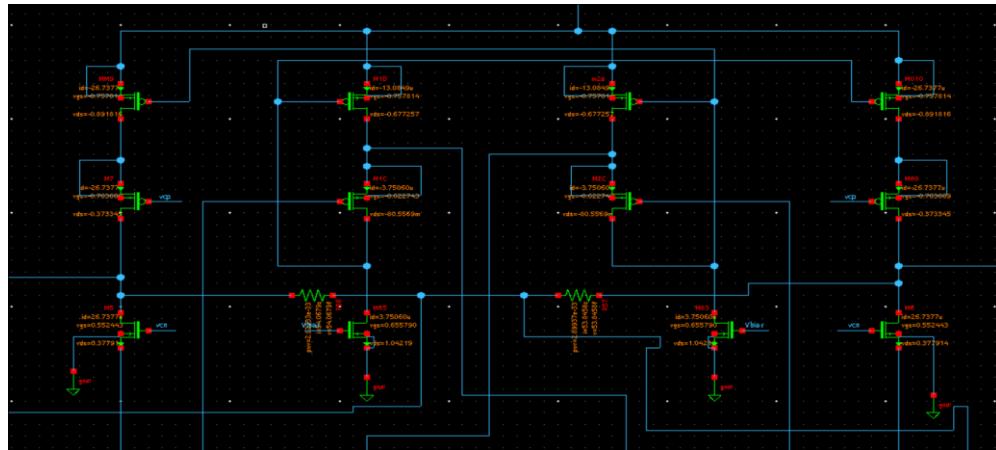
3.a DC Operating Point Analysis

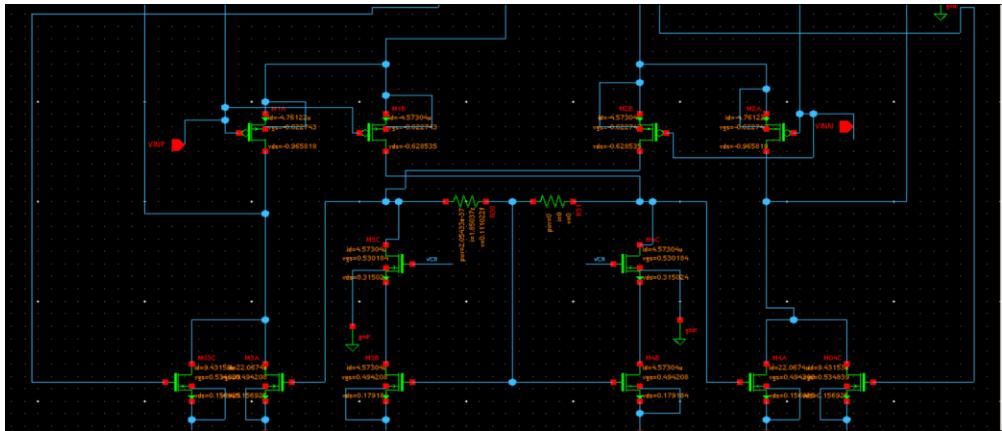
The DC operating point was obtained by simulating the circuit with DC simulation test bench provided and the same is compared against the calculated values in above table. The operating point obtained by simulation is annotated in the schematic shown in

below Figure .



3.c Annotations Operating Points





Operating Regions of All Transistors:

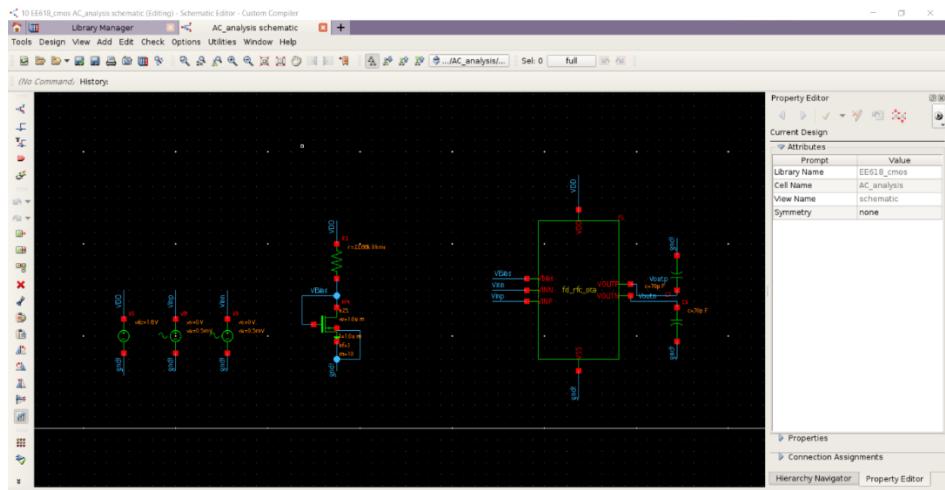
Below screenshots shows that all Tx's are in saturation.

| | name | gm | gmb | ibd | ibs | id | region | vbs | vds | vdsat | vgs | vod | vth |
|----|---------|-----------|-----------|-----|-----|-----------|--------|-----------|-----------|-----------|-----------|-----------|-----------|
| 1 | I9/MB5 | 67.6525u | 4.72862u | 0 | 0 | 52.2768u | 2 | 0.797732 | 1.59546 | 0.665753 | 1.59546 | 1.33579 | 0.259675 |
| 2 | I9/MB1 | 30.7293u | 6.60143u | 0 | 0 | 3.75083u | 2 | 0 | 1.04272 | 0.192090 | 0.655790 | 0.231284 | 0.424506 |
| 3 | I9/MB2 | 30.7293u | 6.60143u | 0 | 0 | 3.75083u | 2 | 0 | 1.04272 | 0.192090 | 0.655790 | 0.231284 | 0.424506 |
| 4 | I9/MB3 | 0.849947m | 97.8032u | 0 | 0 | 0.250528m | 2 | 0.450991 | 0.901982 | 0.350423 | 0.901982 | 0.535835 | 0.366147 |
| 5 | I9/M3C | 90.9653u | 17.8618u | 0 | 0 | 4.58394u | 2 | -0.333026 | 0.158056 | 72.5220m | 0.564992 | 27.6797m | 0.537312 |
| 6 | I9/M4C | 90.9653u | 17.8618u | 0 | 0 | 4.58394u | 2 | -0.333026 | 0.158056 | 72.5220m | 0.564992 | 27.6797m | 0.537312 |
| 7 | I9/M3B | 90.1206u | 20.3649u | 0 | 0 | 4.58394u | 2 | 0 | 0.333026 | 69.4422m | 0.491081 | 30.5781m | 0.460503 |
| 8 | I9/M4B | 90.1206u | 20.3649u | 0 | 0 | 4.58394u | 2 | 0 | 0.333026 | 69.4422m | 0.491081 | 30.5781m | 0.460503 |
| 9 | I9/M4C1 | 0.154848m | 34.5626u | 0 | 0 | 8.90982u | 2 | 0 | 0.311468 | 86.6335m | 0.527285 | 66.6043m | 0.460681 |
| 10 | I9/M3C1 | 0.154848m | 34.5626u | 0 | 0 | 8.90982u | 2 | 0 | 0.311468 | 86.6335m | 0.527285 | 66.6043m | 0.460681 |
| 11 | I9/MB6 | 0.479540m | 0.104743m | 0 | 0 | 52.2768u | 2 | 0 | 0.204537 | 0.167236 | 0.655790 | 0.194010 | 0.461779 |
| 12 | I9/M1D | 0.120336m | 39.0671u | 0 | 0 | -13.0201u | 2 | 0 | -0.677133 | -0.174429 | -0.757278 | -0.170090 | -0.587188 |
| 13 | I9/M2D | 0.120336m | 39.0671u | 0 | 0 | -13.0201u | 2 | 0 | -0.677133 | -0.174429 | -0.757278 | -0.170090 | -0.587188 |
| 14 | M4 | 0.413691m | 88.1347u | 0 | 0 | 50.0092u | 2 | 0 | 0.655790 | 0.196771 | 0.655790 | 0.232122 | 0.423667 |
| 15 | I9/M1A | 74.5321u | 24.6058u | 0 | 0 | -4.68531u | 2 | 0 | -0.811399 | -89.2144m | -0.622867 | -35.3129m | -0.587554 |
| 16 | I9/M2A | 74.5321u | 24.6058u | 0 | 0 | -4.68531u | 2 | 0 | -0.811399 | -89.2144m | -0.622867 | -35.3129m | -0.587554 |
| 17 | I9/M1B | 73.1705u | 24.1461u | 0 | 0 | -4.58394u | 2 | 0 | -0.631785 | -89.2071m | -0.622867 | -35.2985m | -0.587568 |
| 18 | I9/M2B | 73.1705u | 24.1461u | 0 | 0 | -4.58394u | 2 | 0 | -0.631785 | -89.2071m | -0.622867 | -35.2985m | -0.587568 |

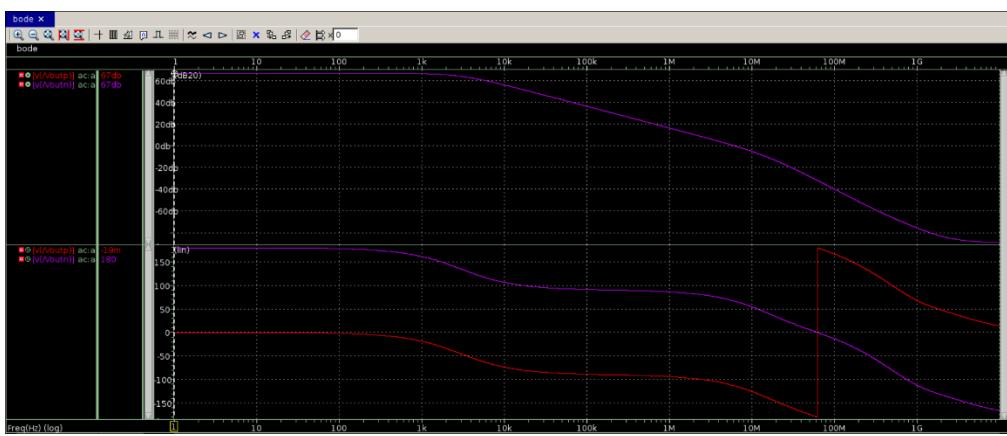
| | | | | | | | | | | | | | | |
|----|--------|-----------|-----------|---|---|-----------|---|---|-----------|-----------|-----------|-----------|-----------|----------|
| 18 | I9/M2B | 73.1705u | 24.1461u | 0 | 0 | -4.58394u | 2 | 0 | -0.631785 | -89.2071m | -0.622867 | -35.2985m | -0.587568 | |
| 19 | I9/M2C | 54.9878u | 18.2439u | 0 | 0 | -3.75083u | 2 | 0 | -80.1442m | -89.1846m | -0.622867 | -35.2542m | -0.587612 | |
| 20 | I9/M1C | 54.9878u | 18.2439u | 0 | 0 | -3.75083u | 2 | 0 | -80.1442m | -89.1846m | -0.622867 | -35.2542m | -0.587612 | |
| 21 | I9/M1D | 0.244400m | 80.5380u | 0 | 0 | -26.4757u | 2 | 0 | -0.833890 | -0.176158 | -0.757278 | -0.169699 | -0.587579 | |
| 22 | I9/M9 | 0.244400m | 80.5380u | 0 | 0 | -26.4757u | 2 | 0 | -0.833890 | -0.176158 | -0.757278 | -0.169699 | -0.587579 | |
| 23 | I9/M7 | 0.240977m | 79.3739u | 0 | 0 | -26.4757u | 2 | 0 | -0.438826 | -0.179269 | -0.761574 | -0.173963 | -0.587611 | |
| 24 | I9/M8 | 0.240977m | 79.3739u | 0 | 0 | -26.4757u | 2 | 0 | -0.438826 | -0.179269 | -0.761574 | -0.173963 | -0.587611 | |
| 25 | I9/M6 | 0.481855m | 95.0985u | 0 | 0 | 26.4757u | 2 | 0 | -0.311468 | 0.215817 | 84.4615m | 0.586550 | 52.8365m | 0.533714 |
| 26 | I9/M5 | 0.481855m | 95.0985u | 0 | 0 | 26.4757u | 2 | 0 | -0.311468 | 0.215817 | 84.4615m | 0.586550 | 52.8365m | 0.533714 |
| 27 | I9/M84 | 2.35433m | 0.513901m | 0 | 0 | 0.250528m | 2 | 0 | 0.898018 | 0.170324 | 0.655790 | 0.198624 | 0.457166 | |
| 28 | I9/M4A | 0.439325m | 99.6064u | 0 | 0 | 22.2512u | 2 | 0 | 0.311468 | 68.8102m | 0.491081 | 29.0725m | 0.462009 | |
| 29 | I9/M3A | 0.439325m | 99.6064u | 0 | 0 | 22.2512u | 2 | 0 | 0.311468 | 68.8102m | 0.491081 | 29.0725m | 0.462009 | |

4.a AC Analysis:

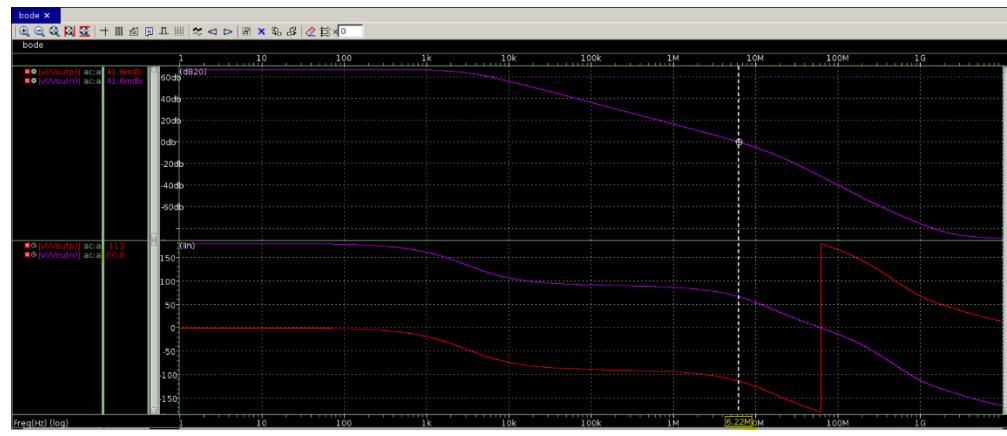
This is the schematic of Ac Analysis.



4.b Bode Plot:



4.c UGF, Phase Margin:



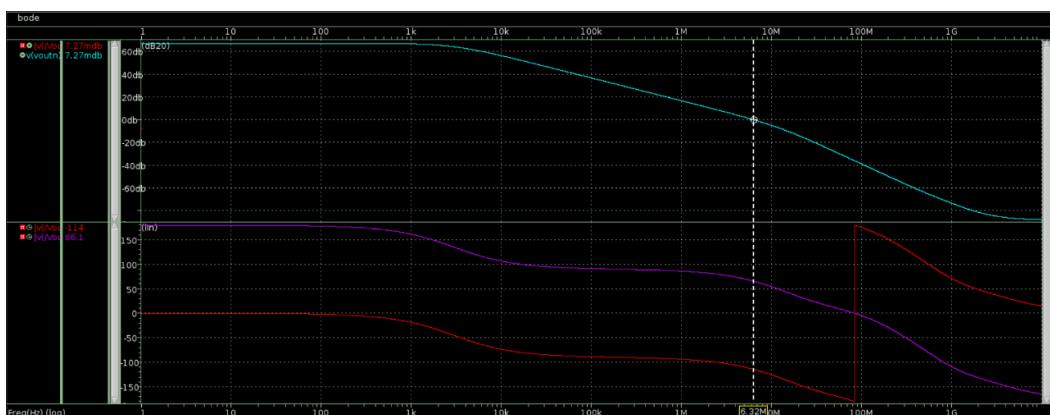
4.d PM ,UGF, Open loop Gain:

| parametre | Value |
|----------------|--------------|
| PM | 66.8 degrees |
| UGF | ~6.22MHz |
| Open Loop gain | 67dB |

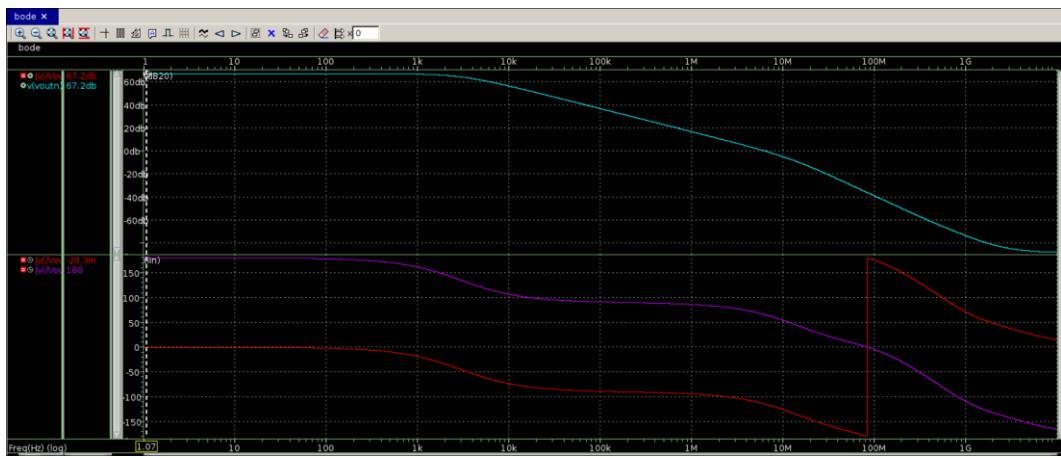
4.e Frequency response for FF,FS,SF,SS:

FF Corner:

UGF and PM :

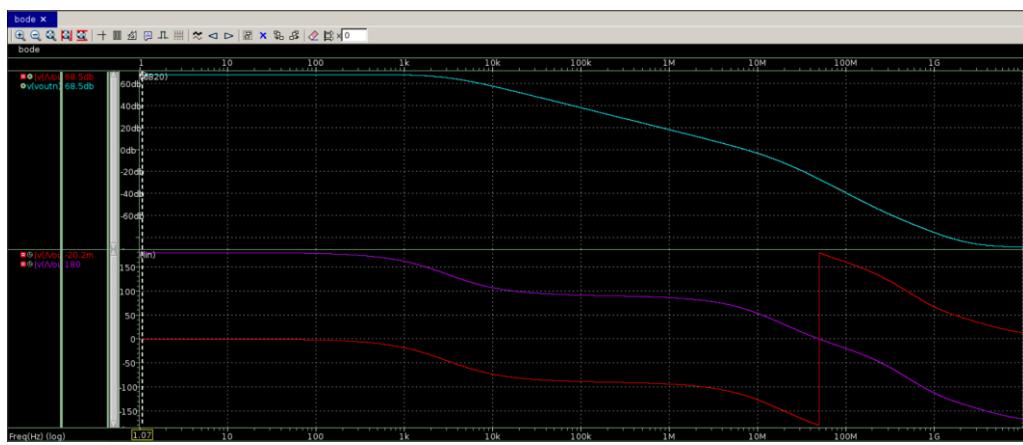


Gain :

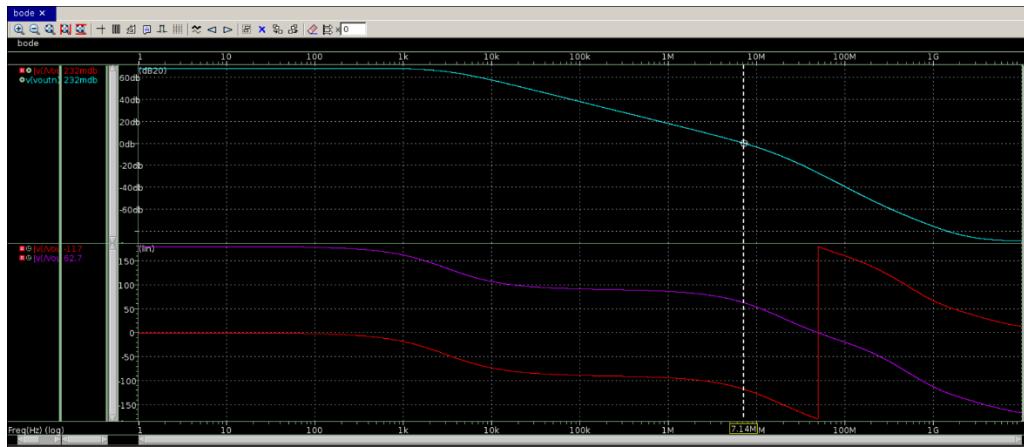


FS Corner:

Gain :

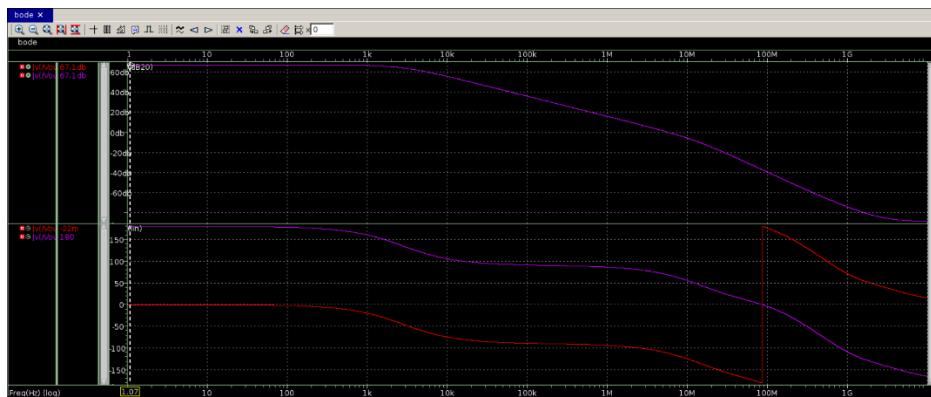


UGF and PM:

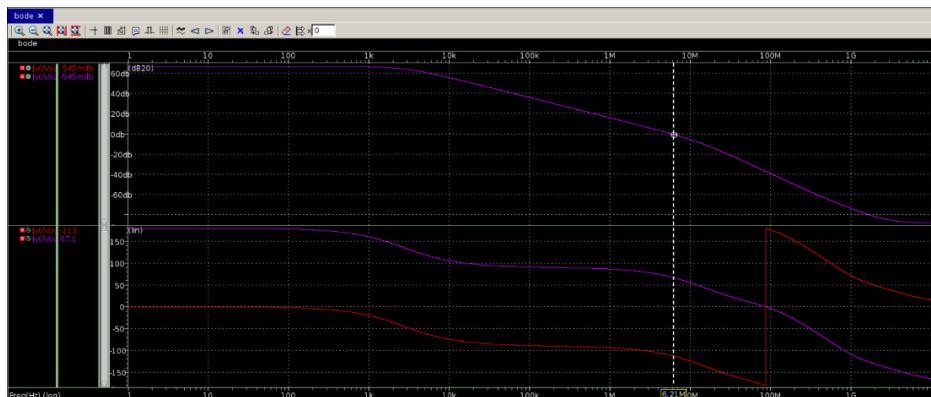


SF Corner:

Gain:

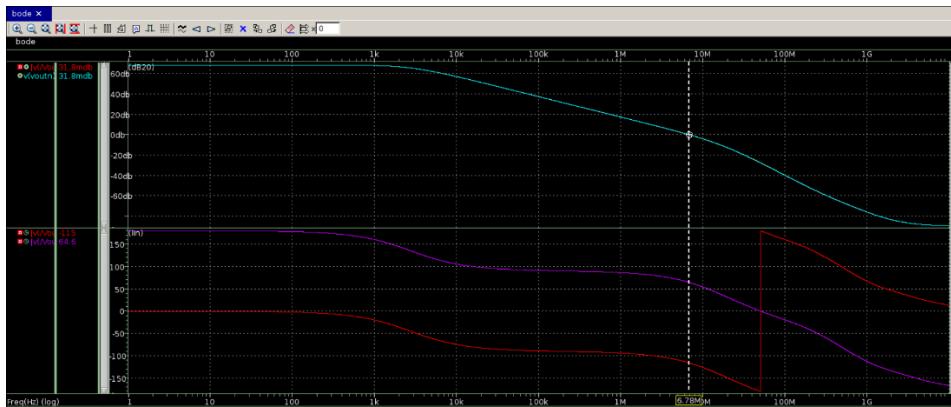


UGF and PM:

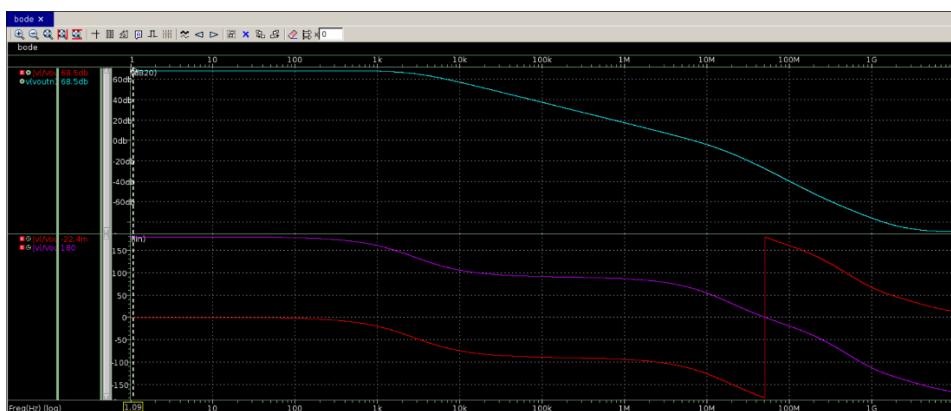


SS Corner:

UGF and PM :



Gain :

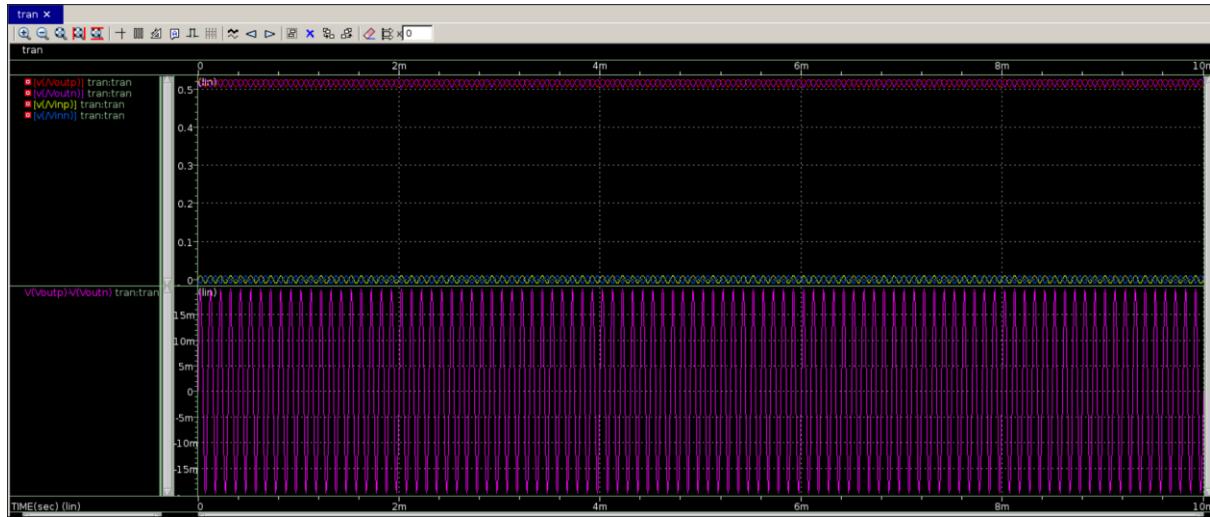


4.f Table for Different Corners

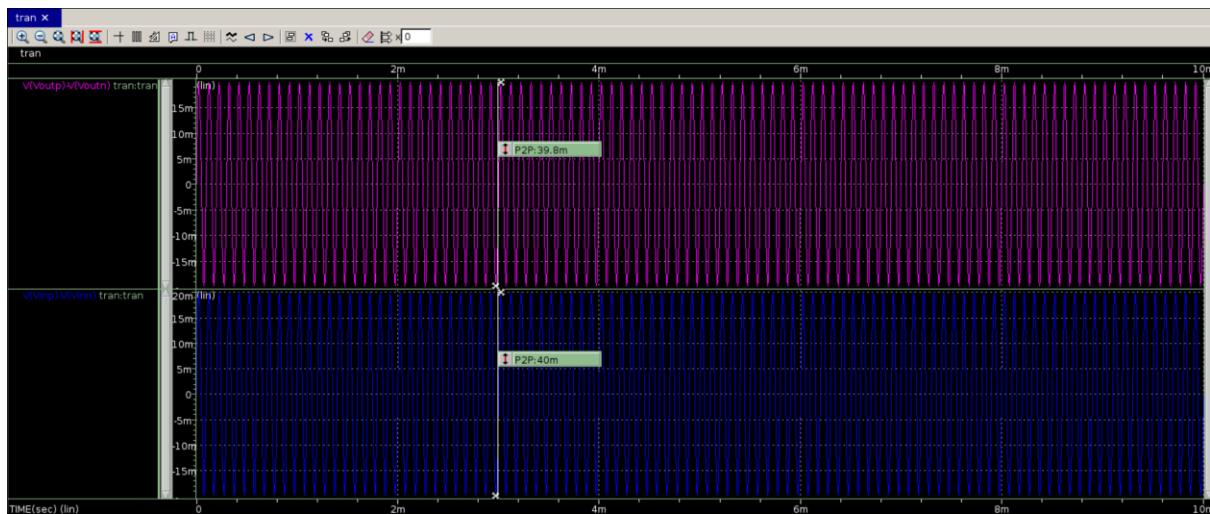
| Process Corner | TT | FF | FS | SF | SS |
|----------------------|-------|------|------|------|------|
| Gain(dB) | 67 | 67.2 | 68.5 | 67.1 | 68.5 |
| UGF(MHz) | ~6.22 | 6.32 | 7.14 | 6.21 | 6.78 |
| Phase Margin(Degree) | 66.8 | 66.1 | 62.7 | 67.1 | 64.6 |
| Gain Margin | 28.9 | 24.3 | 32 | 33 | 24 |

5.a Transient Analysis:

5.b Plot for VOUT +, VOUT -, VIN+ – VIN- and VOUT + – VOUT -



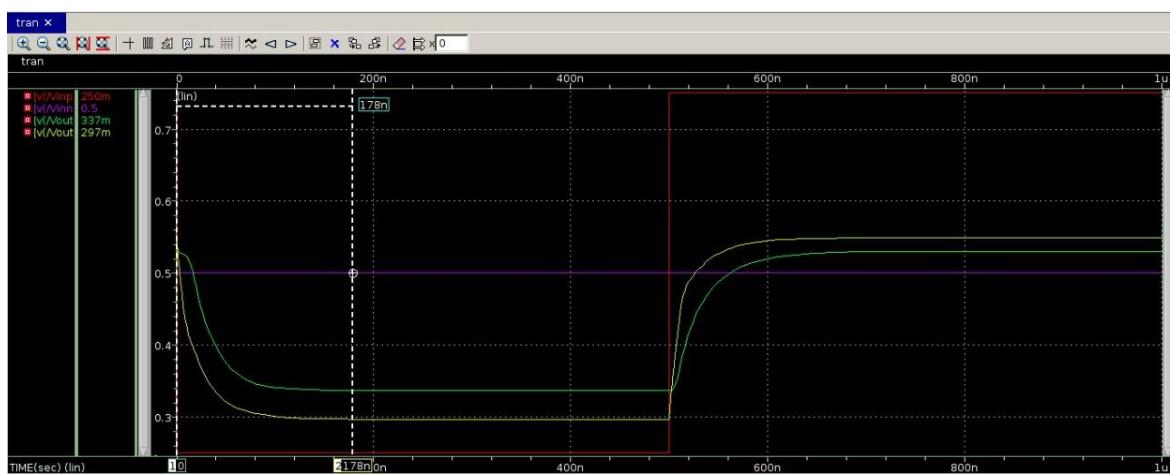
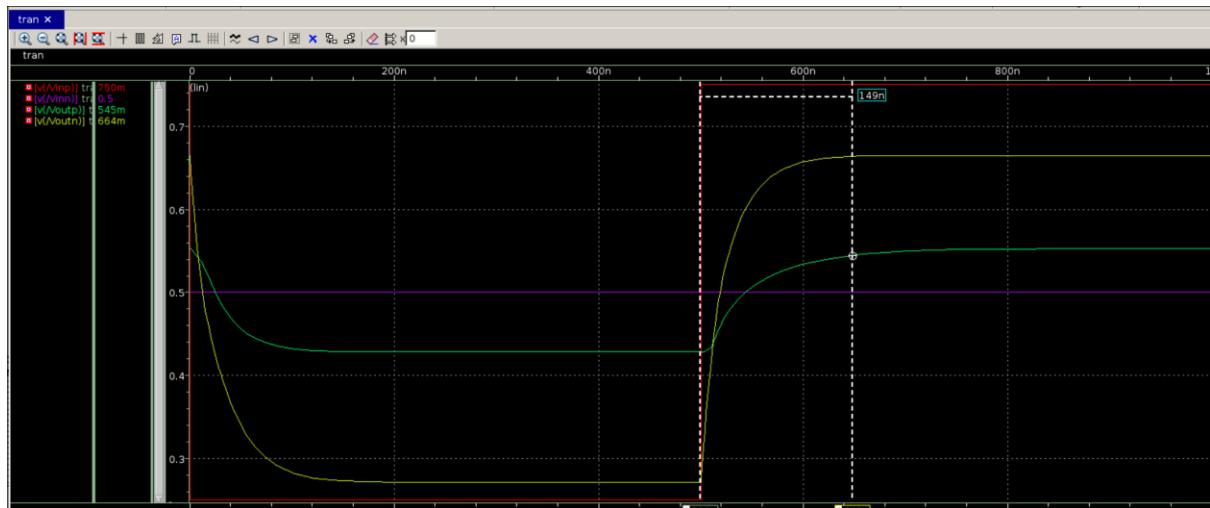
Annotation of peak to peak of (VIN+ – VIN-) and (VOUT + – VOUT -)



5.e Positive and Negative Settling Times for All Corners:

1. TT

Positive :



3. FF

Positive :



Negative

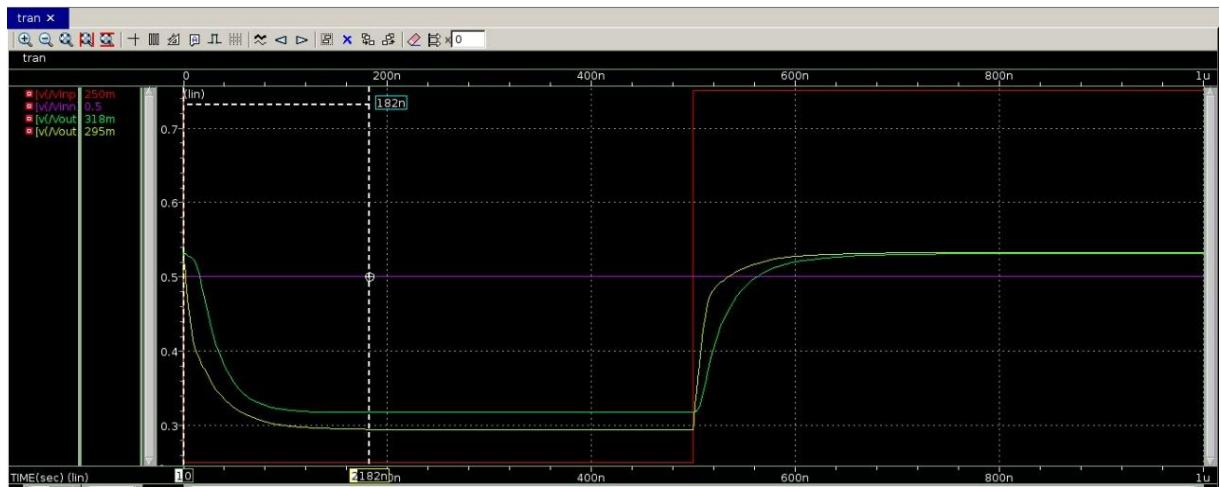


4. FS

Positive :

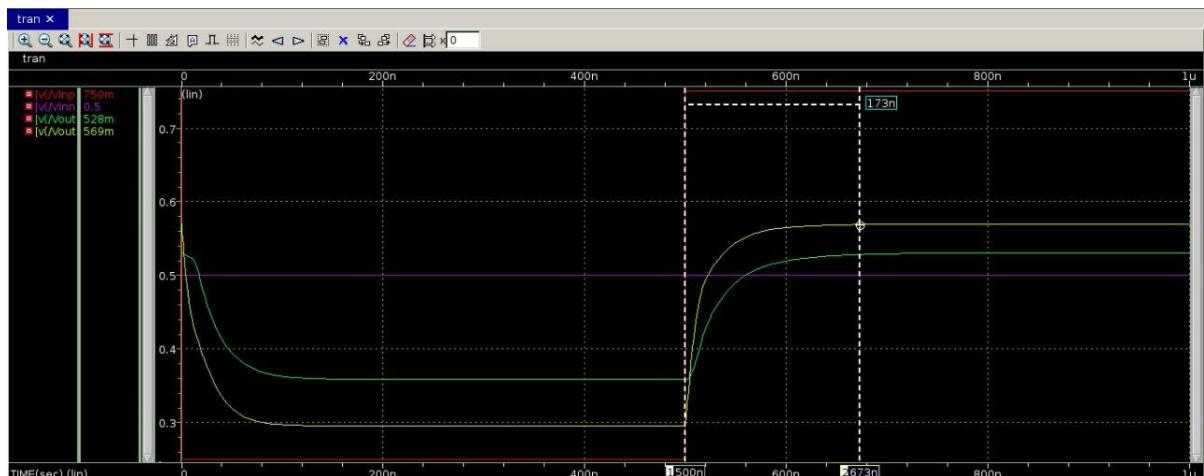


Negative

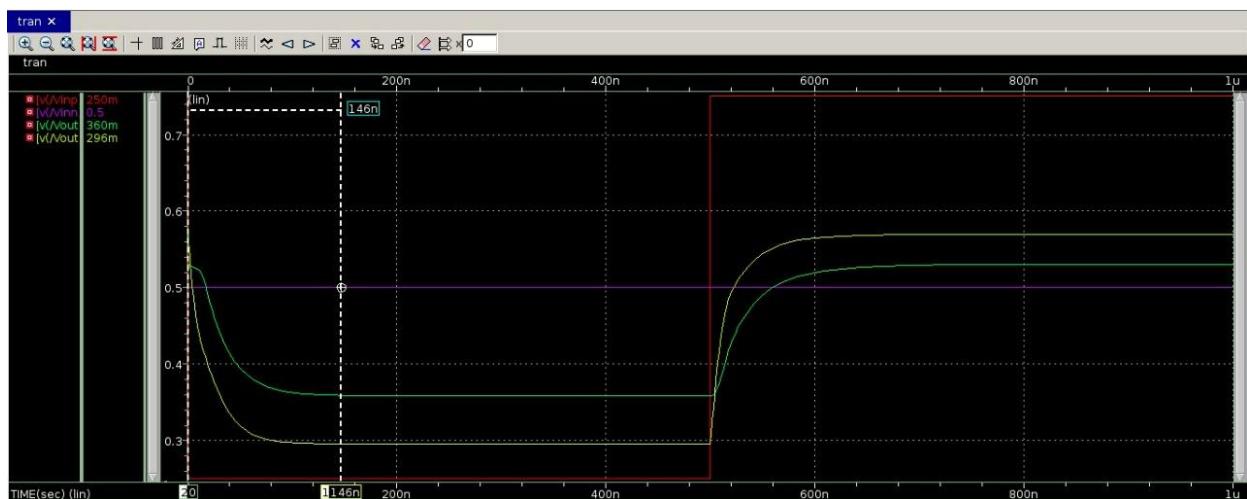


5. SF

Positive :



Negative

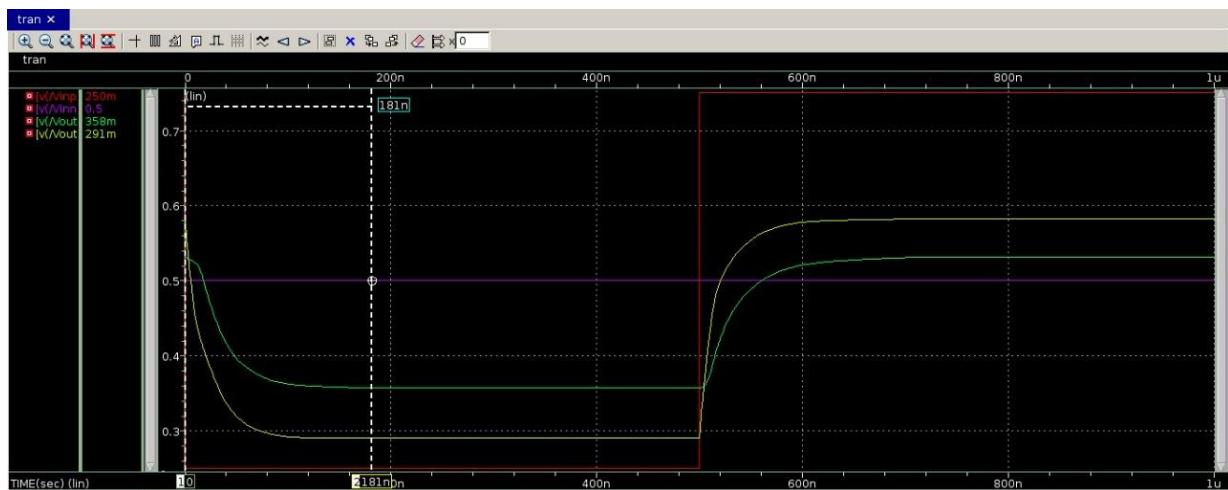


6. SS

Positive :



Negative



5.f Table

| Process Corner | TT | FF | FS | SF | SS |
|----------------------------|-----|-----|-----|-----|-----|
| Positive Settling Time(ns) | 149 | 171 | 171 | 173 | 196 |
| Negative Settling Time(ns) | 178 | 168 | 182 | 146 | 181 |

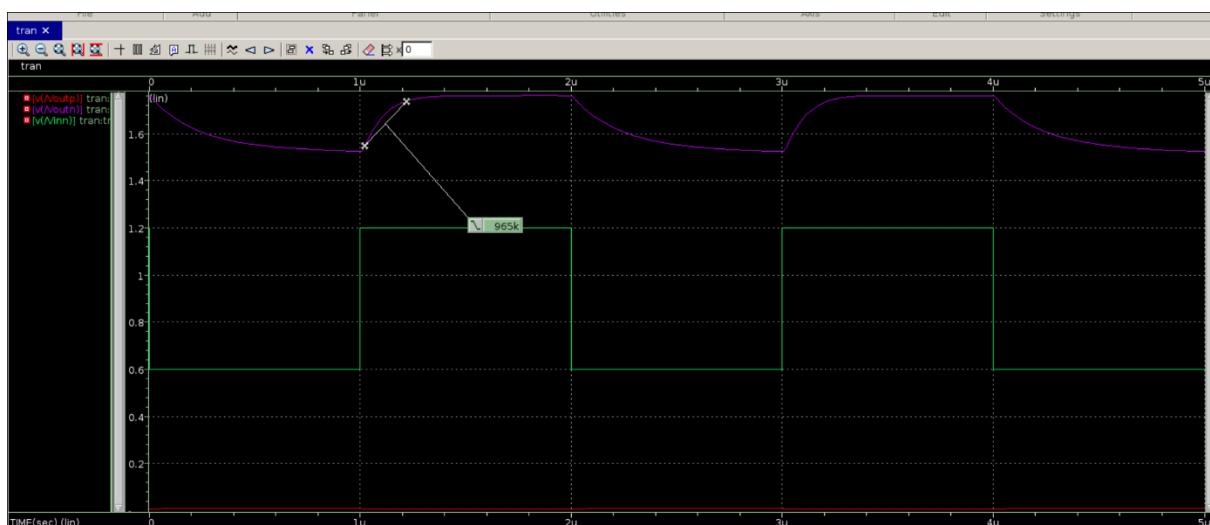
6.a SlewRate:

6.b

1. Negative Slewrate



2. Positive Slewrate

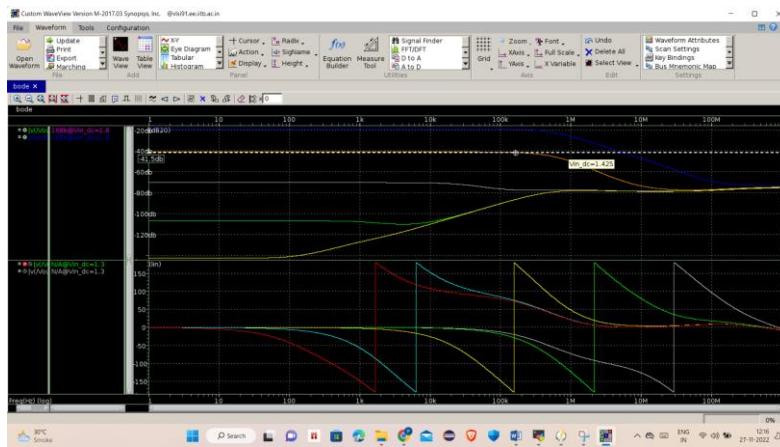


6.c Table

| | Desired Value | Simulation Result |
|--------------------|---------------|-------------------|
| Negative SR (v/us) | -0.2 | -0.335 |
| Positive SR (v/us) | 0.2 | 0.965 |
| Average SR (v/us) | 0 | 0.315 |

7.a Common Mode Simulations:

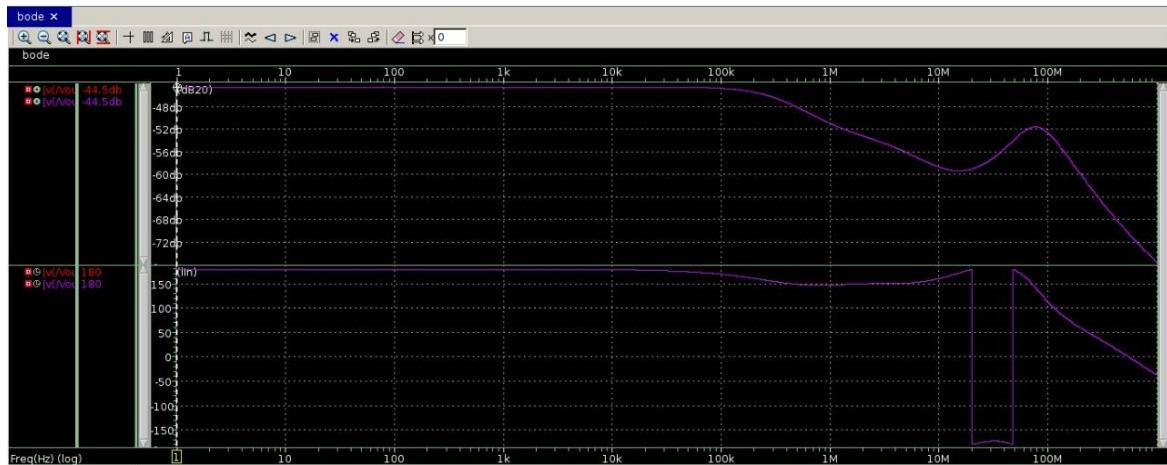
7.b ICMR :



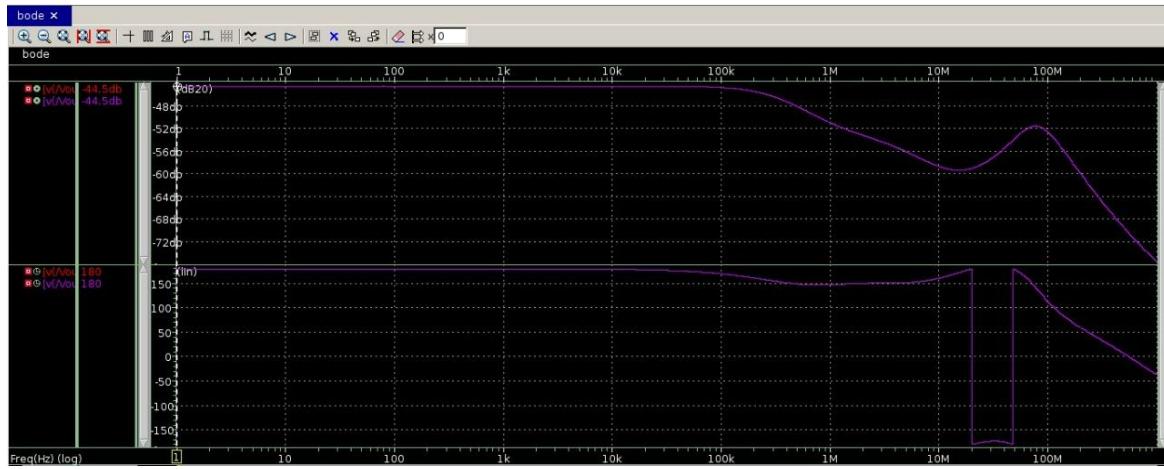
$$V_{cm(min)} = 1.37V$$

$$V_{cm(max)} = 1.86V$$

7.c AC simulations:

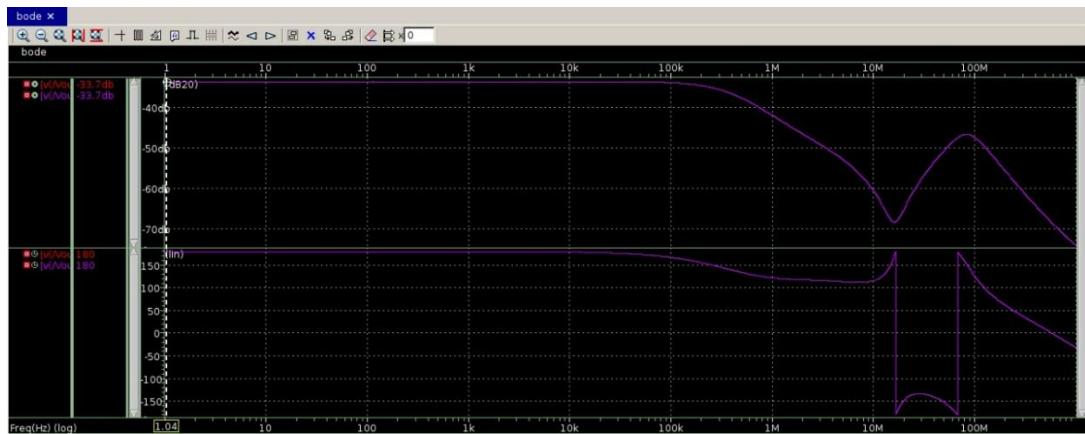


7.d

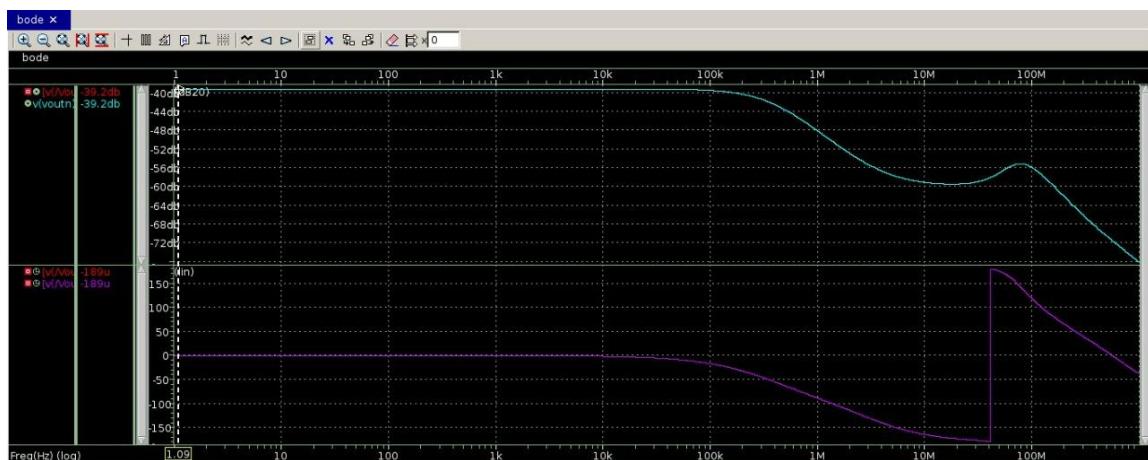


7.e Corners:

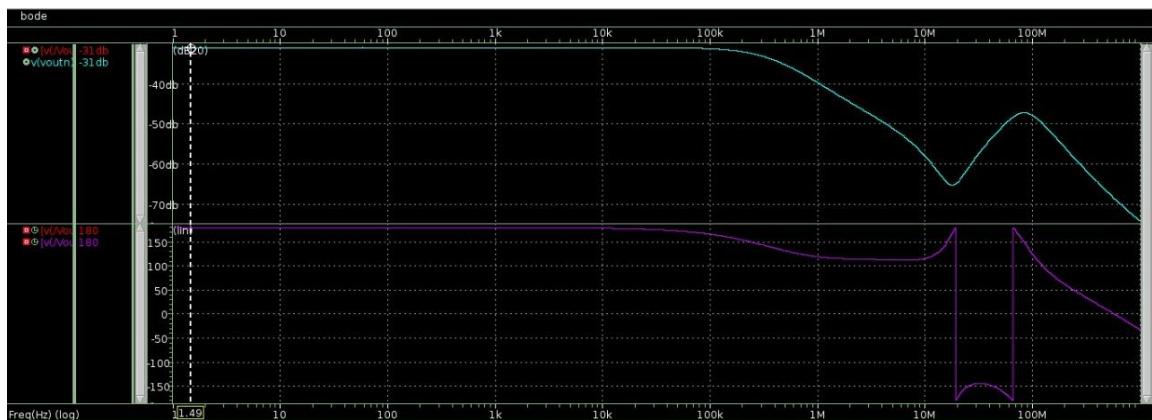
1. FF:



2.FS:



3.SF



4.SS

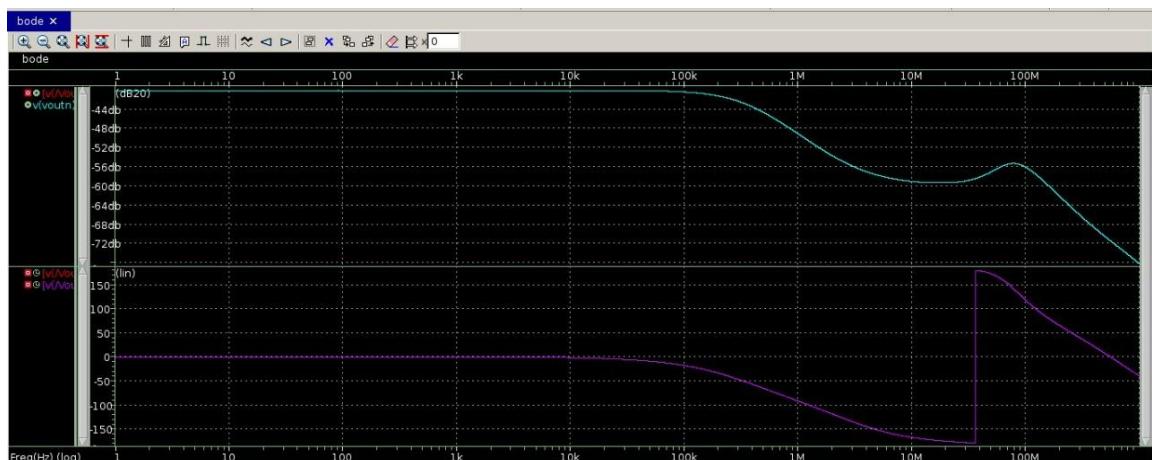


Table:

| Process Corner | TT | FF | FS | SF | SS |
|----------------|-------|-------|-------|------|-------|
| DC Gain(dB) | 67 | 67.2 | 68.5 | 67.1 | 68.5 |
| ACM-DM(dB) | -44.5 | -33.7 | -39.2 | -31 | -42 |
| CMRR(dB) | 111.5 | 100.9 | 107.7 | 98.1 | 110.5 |

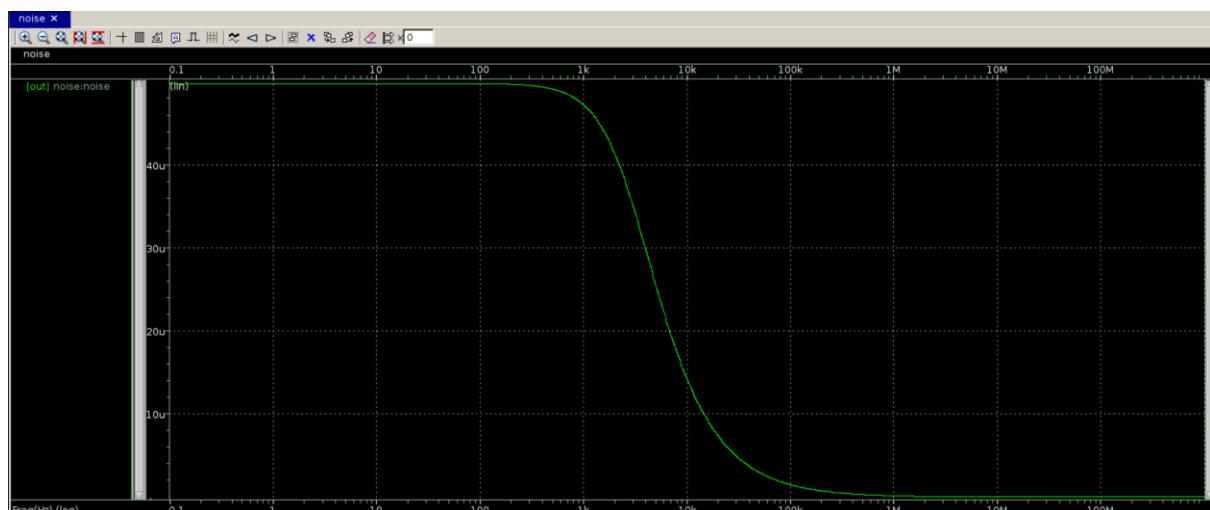
8.a Noise Simulations

8.b Noise Simulation for TT corner:

1. Input Noise



2. Output Noise



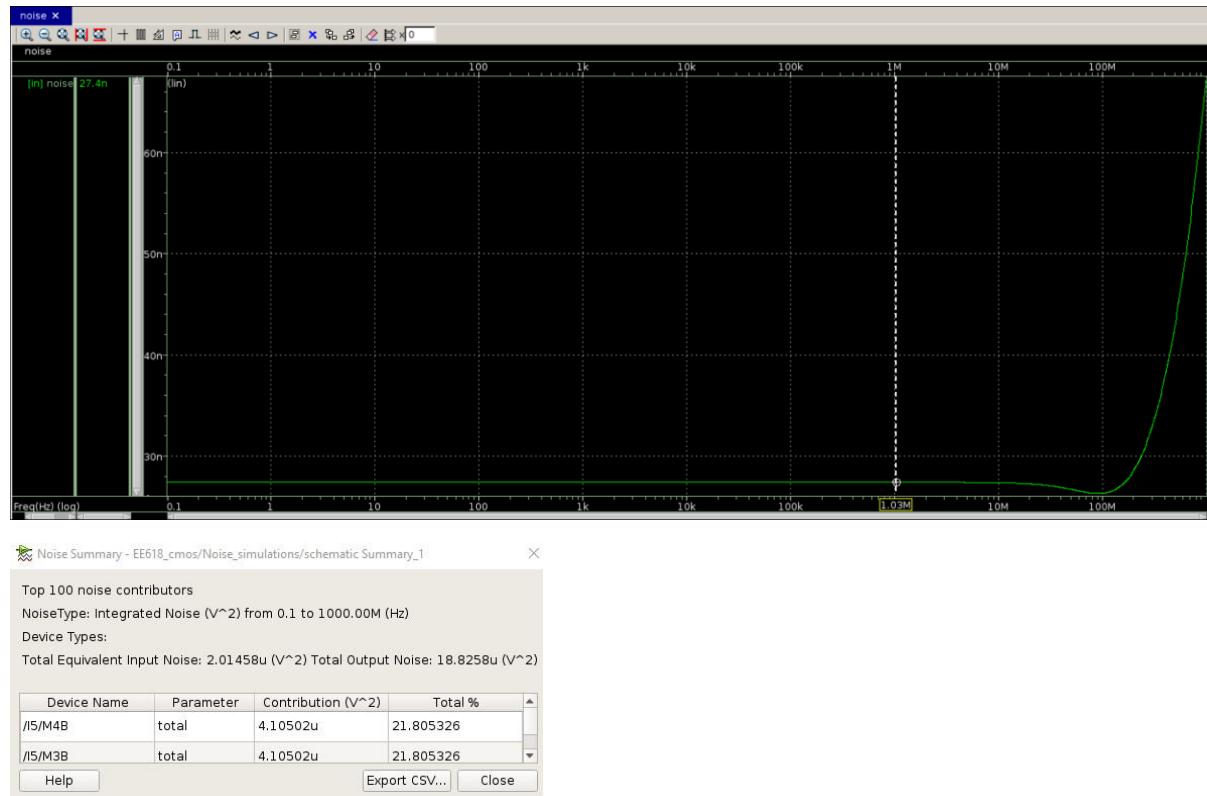
8.c Integrated Total Input Noise Summary:

| Top 100 noise contributors | | | |
|---|-----------|--------------------|-----------|
| NoiseType: Integrated Noise (V^2) from 0.1 to 1000.00M (Hz) | | | |
| Device Types: | | | |
| Total Equivalent Input Noise: 2.52773u (V^2) Total Output Noise: 11.7269u (V^2) | | | |
| Device Name | Parameter | Contribution (V^2) | Total % |
| /I5/M3B | total | 1.83834u | 15.676228 |
| /I5/M4B | total | 1.83834u | 15.676228 |
| /I5/M2B | total | 1.52322u | 12.989043 |
| /I5/M1B | total | 1.52322u | 12.989043 |
| /I5/M1C | total | 1.47089u | 12.542879 |
| /I5/M2C | total | 1.47089u | 12.542879 |
| /I5/M85 | total | 0.563632u | 4.806303 |
| /I5/M83 | total | 0.563632u | 4.806303 |
| /I5/R30 | total | 0.4299878u | 3.665736 |
| /I5/R31 | total | 0.4299878u | 3.665736 |
| /I5/M3A | total | 14.9549n | 0.127526 |
| /I5/M4A | total | 14.9549n | 0.127526 |
| /I5/MM9 | total | 9.56376n | 0.081554 |
| /I5/M010 | total | 9.56376n | 0.081554 |
| /I5/m2d | total | 6.33199n | 0.053995 |
| /I5/M1D | total | 6.33199n | 0.053995 |
| /I5/M03C | total | 5.51289n | 0.047011 |
| /I5/M04C | total | 5.51289n | 0.047011 |
| /I5/M3C | total | 0.966023n | 0.008238 |
| /I5/M4C | total | 0.966023n | 0.008238 |

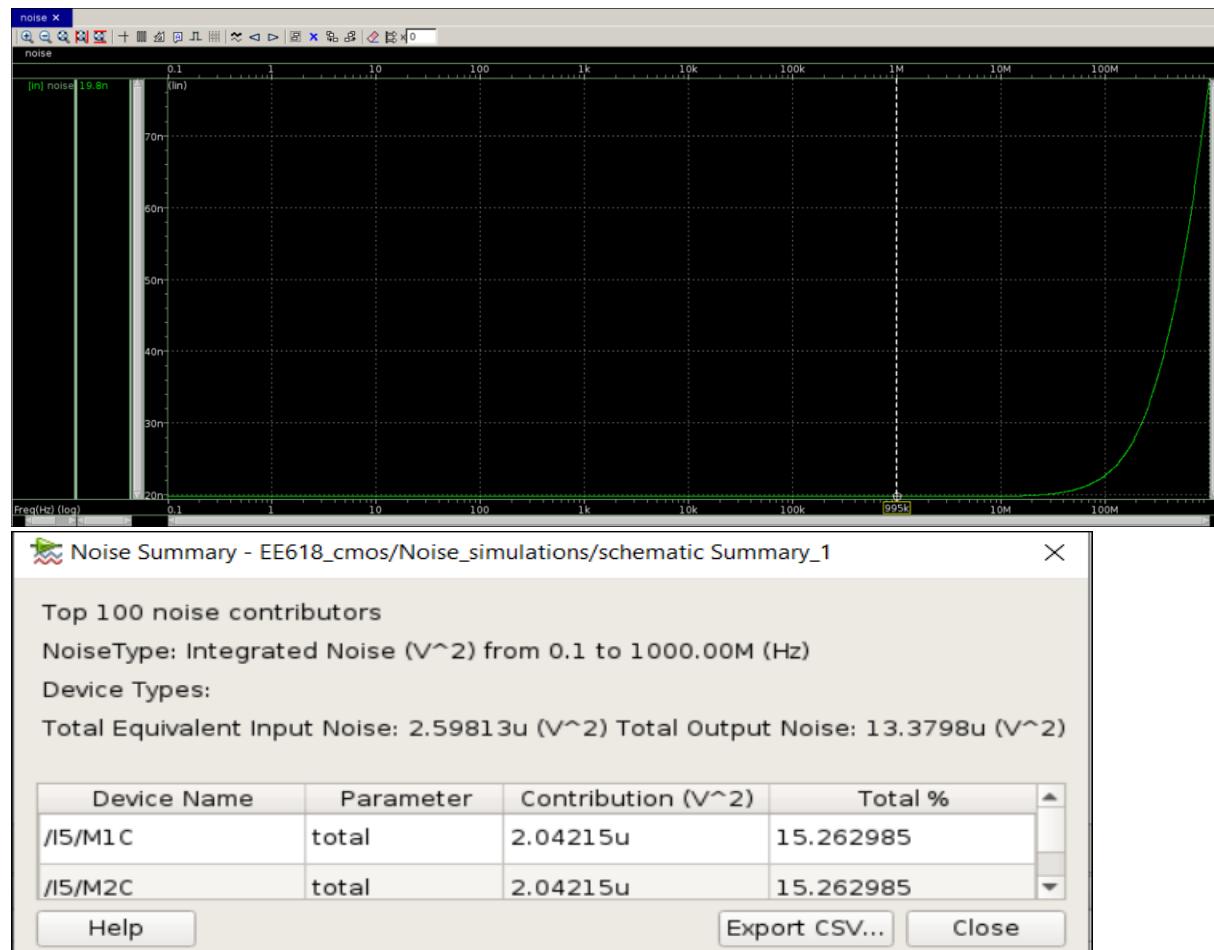
| Noise Summary - EE618_cmos/Noise_simulations/schematic Summary_3 | | | |
|--|-----------|-----------------------|-----------|
| Top 100 noise contributors | | | |
| Device Name | Parameter | Contribution (V^2/Hz) | Total % |
| /I5/M3B | total | 0.388850n | 15.676244 |
| /I5/M4B | total | 0.388850n | 15.676244 |
| /I5/M2B | total | 0.322194n | 12.989057 |
| /I5/M1B | total | 0.322194n | 12.989057 |
| /I5/M1C | total | 0.311127n | 12.542887 |
| /I5/M2C | total | 0.311127n | 12.542887 |
| /I5/M85 | total | 0.119221n | 4.806307 |
| /I5/M83 | total | 0.119221n | 4.806307 |
| /I5/R30 | total | 90.9288p | 3.665739 |
| /I5/R31 | total | 90.9288p | 3.665739 |
| /I5/M3A | total | 3.16280p | 0.127507 |
| /I5/M4A | total | 3.16280p | 0.127507 |
| /I5/MM9 | total | 2.02263p | 0.081541 |
| /I5/M010 | total | 2.02263p | 0.081541 |
| /I5/m2d | total | 1.33934p | 0.053995 |
| /I5/M1D | total | 1.33934p | 0.053995 |
| /I5/M03C | total | 1.16592p | 0.047003 |
| /I5/M04C | total | 1.16592p | 0.047003 |
| /I5/M4C | total | 0.204295p | 0.008236 |
| /I5/M2C | total | 0.204295p | 0.008236 |

8.d Noise Parametre for all Corners:

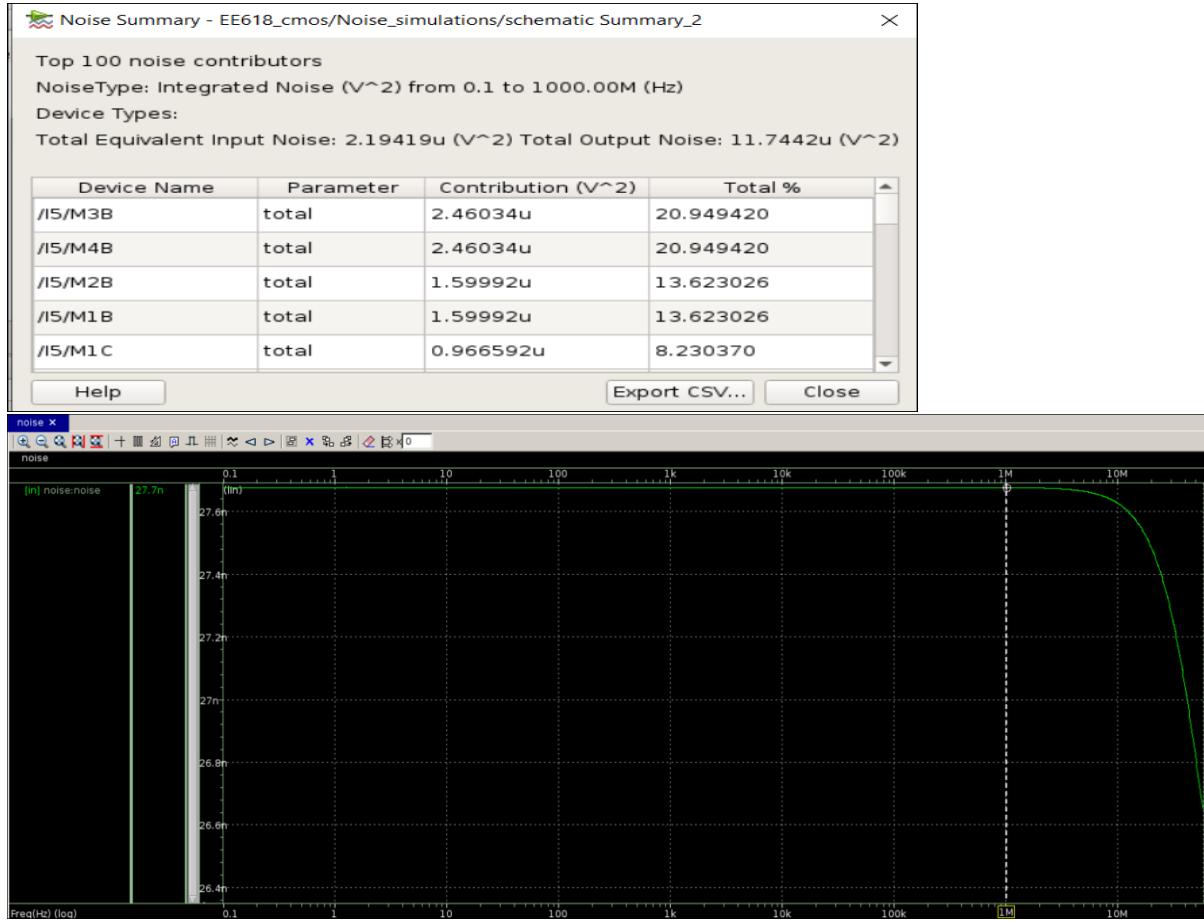
1.FF:



2.FS:



3.SF:



4. SS:

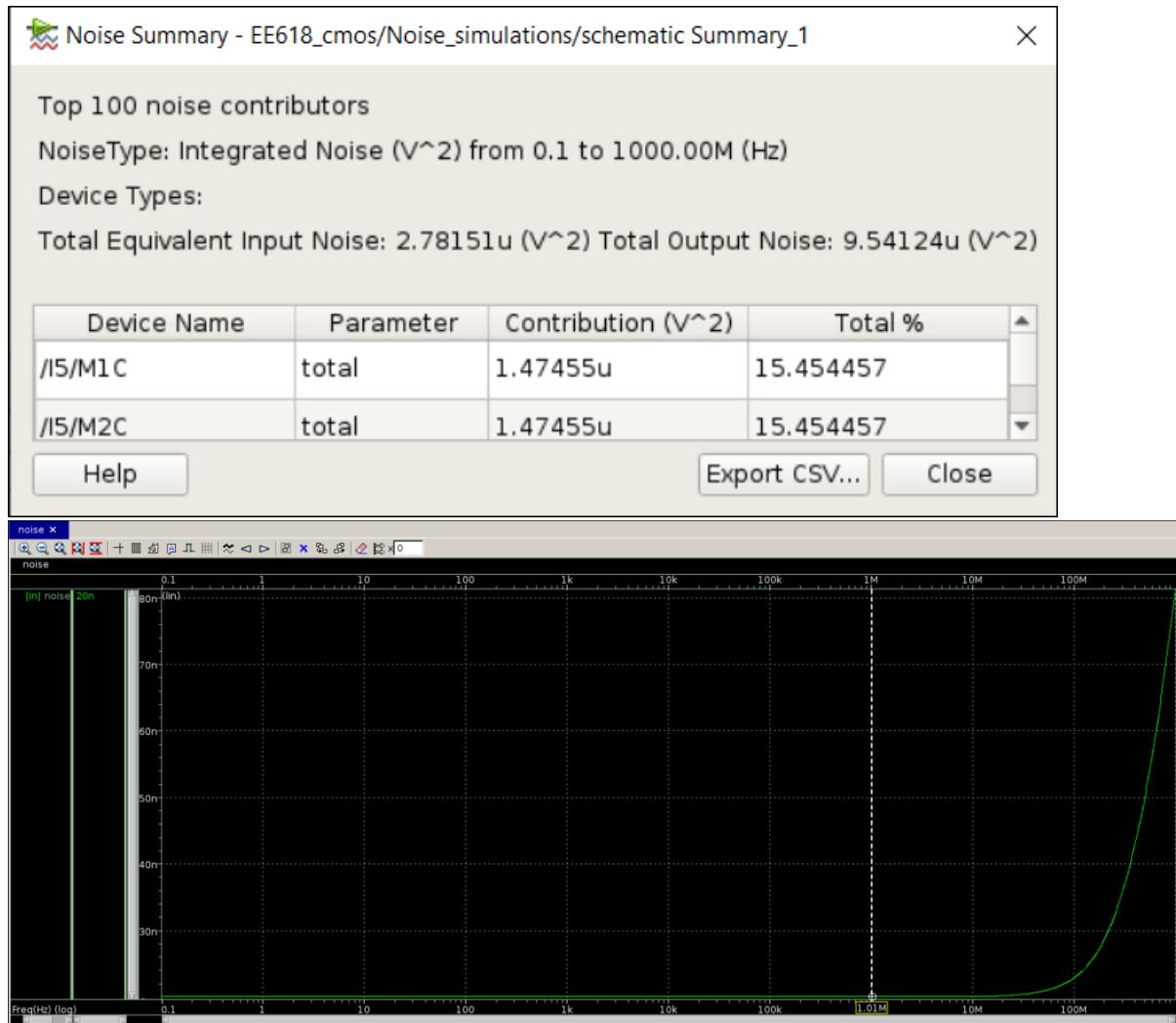


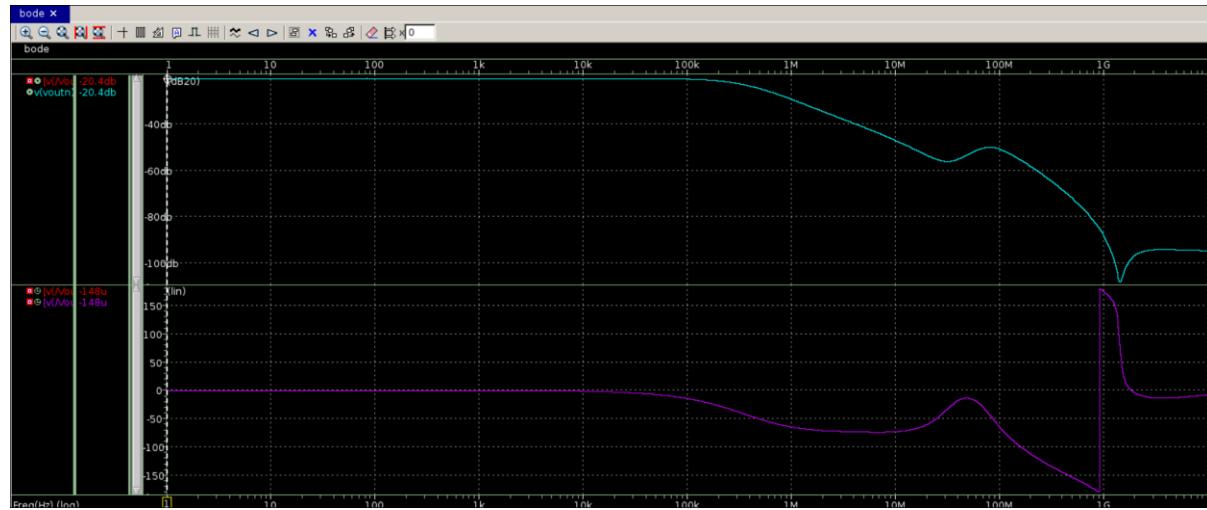
Table:

| Process Corner | TT | FF | FS | SF | SS |
|---|---------|--------|--------|--------|--------|
| Equivalent Input Noise at f = 1MHz in nV/root(Hz) | 22.3 | 27.4 | 19.8 | 27.7 | 20 |
| Total integrated Input Noise(μV^2) | 2.52773 | 2.0145 | 2.5981 | 2.0903 | 2.7815 |

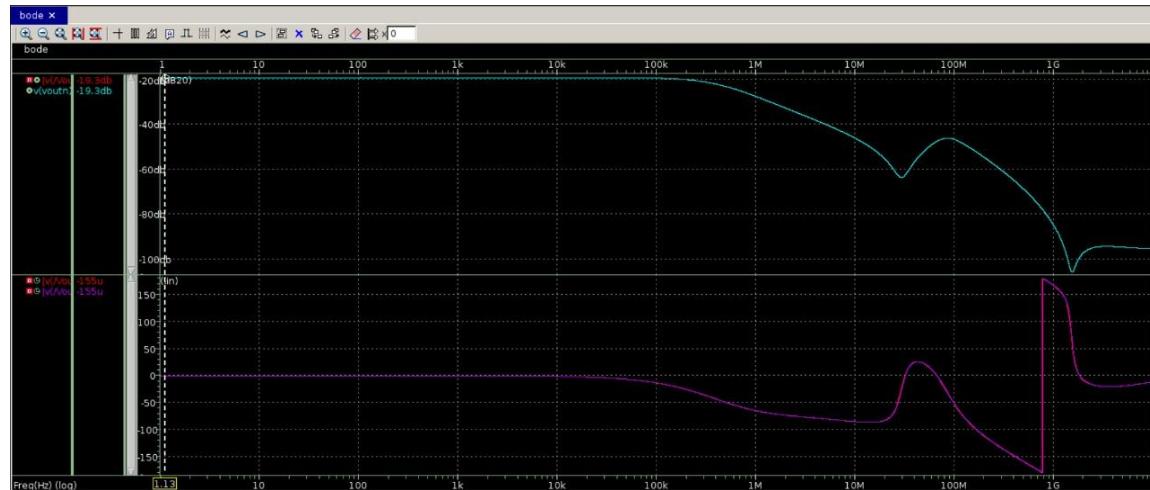
9.a PSRR Simulations:

9.b Ac simulation of PSRR:

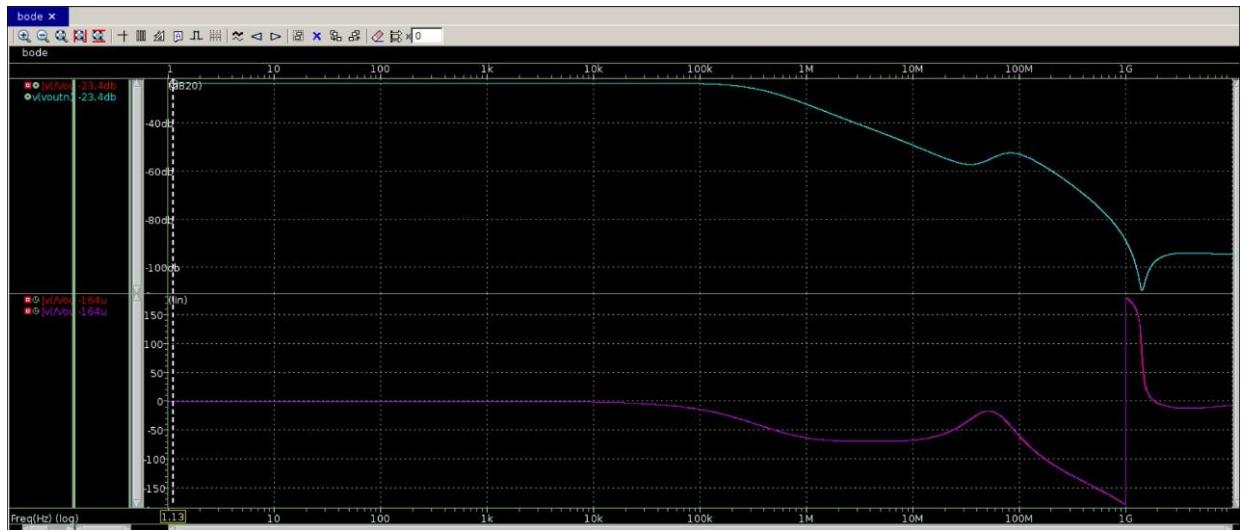
1. TT



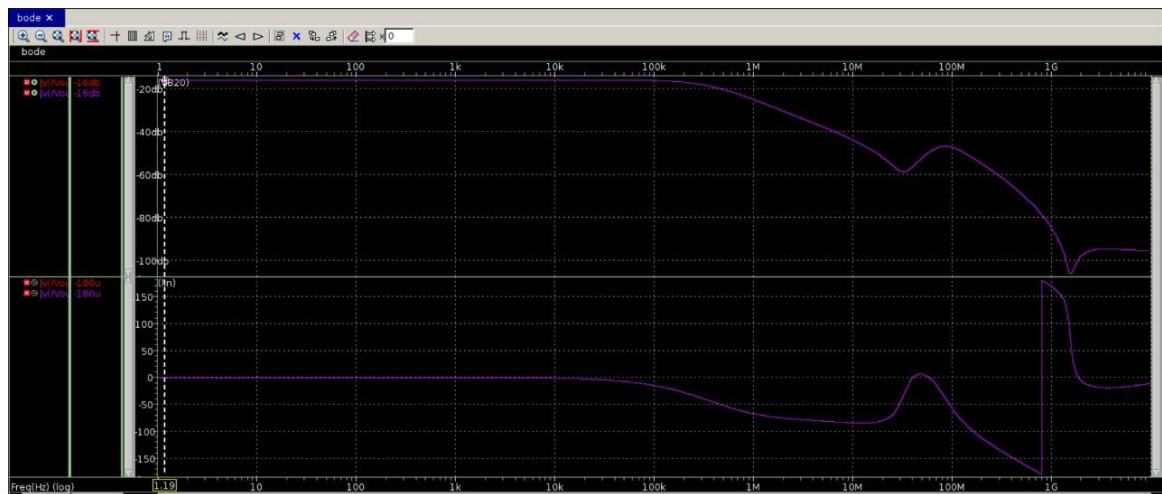
2. FF:



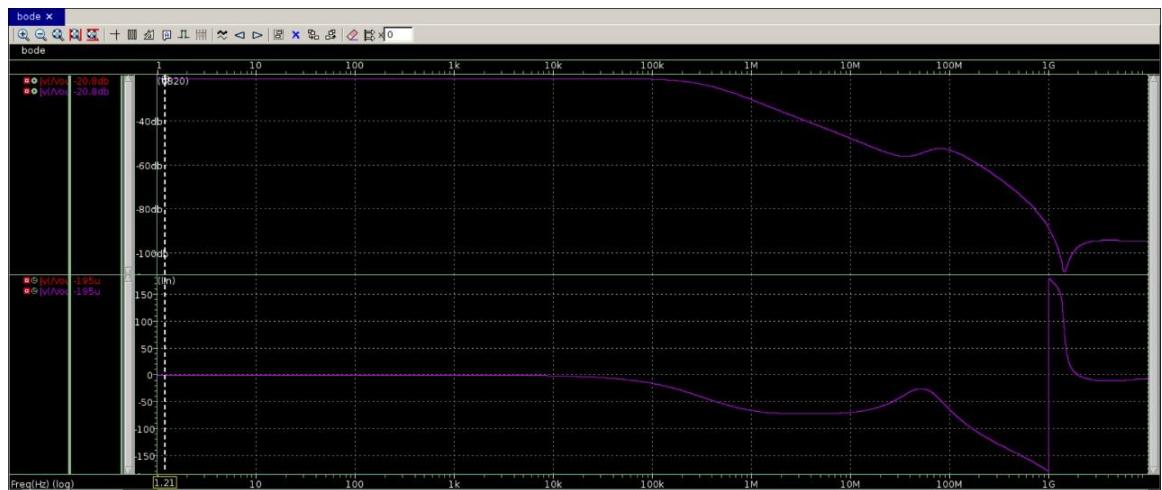
3.FS:



4. SF:



5. SS:



9.c Table for PSRR for all Corners:

| Process Corner | TT | FF | FS | SF | SS |
|------------------------------|-------|-------|-------|------|-------|
| DC Gain(dB) | 67 | 67.2 | 68.5 | 67.1 | 68.5 |
| Gain due to Power Supply(dB) | -20.4 | -19.3 | -23.4 | -16 | -20.8 |
| PSRR(dB) | 87.4 | 86.5 | 91.9 | 83.1 | 89.3 |

10. Work Contribution:

| Question | Golok | Tarak |
|----------|-------|-------|
| 1 | yes | yes |
| 2 | yes | yes |
| 3 | yes | yes |
| 4 | yes | yes |
| 5 | yes | yes |
| 6 | yes | yes |
| 7 | yes | yes |
| 8 | yes | yes |
| 9 | yes | yes |

Conclusion:

Finally we concluded that Super class FD OTA has been designed for all the required specifications with aspect ratios of Table 1 values. Sincerely thanks to **Maryam Shajoei Bhagini** and all the TA's who helped in completing this course and the project.