1) Design a combinational circuit that converts 8421 BCD code to Excess-3 code.

Binary code decimal => 0 to 9 → 10 to 15 is taken as don't care

Decimal	BCD				Excess-3 Code			
	8	4	2	1				
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0
10	1	0	1	0	X	X	X	X
11	1	0	1	1	X	X	X	X
12	1	1	0	0	X	X	X	X
13	1	1	0	1	X	X	X	X
14	1	1	1	0	X	X	X	X
15	1	1	1	1	X	X	X	X

For W

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	1	1	1
11	X	X	X	X
10	1	1	X	X

$W = A + BC + BD$

For X

AB \ CD	00	01	11	10
00		1	1	1
01	1			
11	X	X	X	X
10		1	X	X

$X = \bar{B}D + \bar{B}C + B\bar{C}\bar{D}$

AB \ CD	00	01	11	10
00	1		1	
01	1		1	
11	X	X	X	X
10	1		X	X

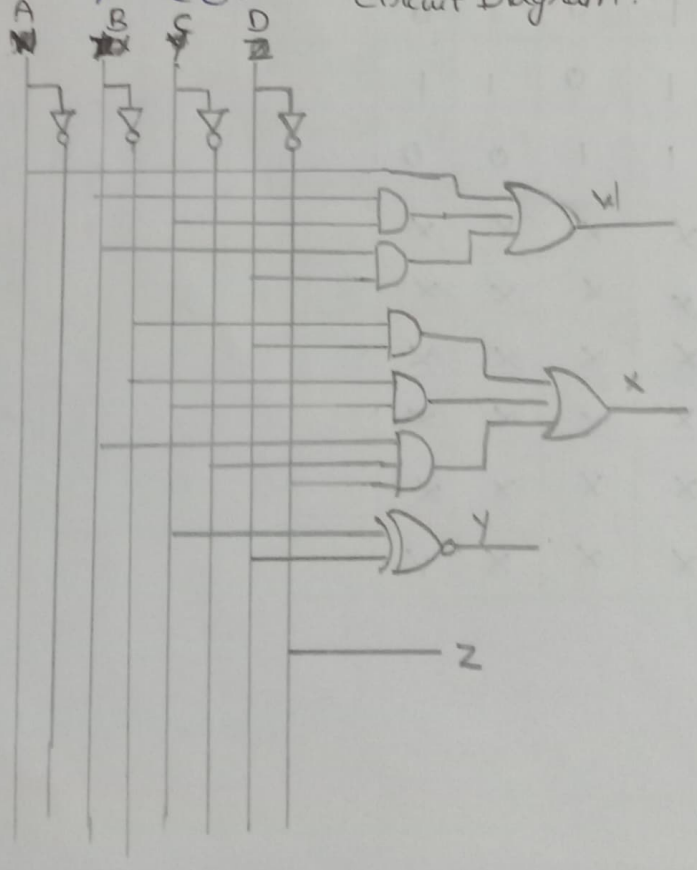
$Y = \bar{C}D + C\bar{D}$

$Y = C \odot D$

AB \ CD	00	01	11	10
00	1			1
01	1			1
11	X	X	X	X
10	1		X	X

$Z = \bar{D}$

Circuit Diagram.



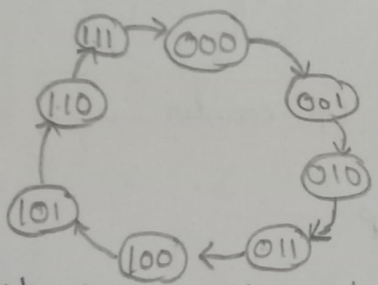
2) Design a Synchronous Counter which counts the Sequence 001, 001, 010, 2) 011, 100, 101, 110, 111, 000 using T flip-flop.

Step 1: n = 3 bits, Flip flop = T Flip flop

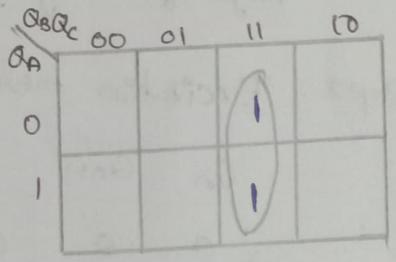
Step 2: Excitation table for T flip flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

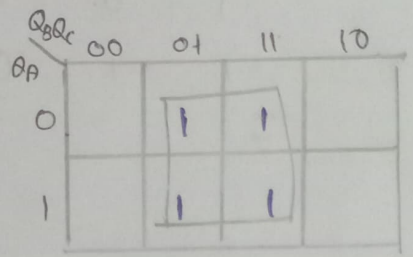
Step 3: State diagram & State Table



Present State			Next State					
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1



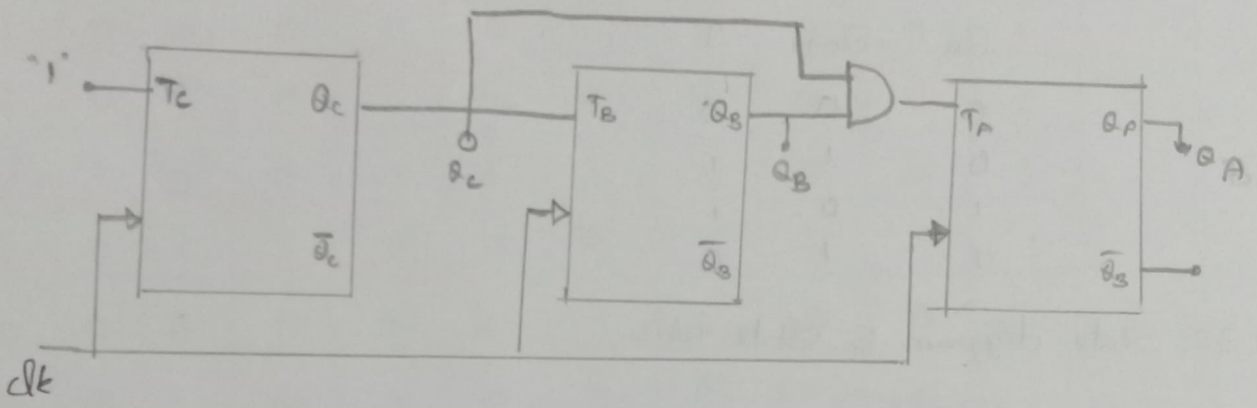
$T_A = Q_B Q_C$



$T_B = Q_C$

Q_A \ $Q_B Q_C$	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$T_C = 1$



3) Design a modulo -10 Synchronous binary UP-counter.

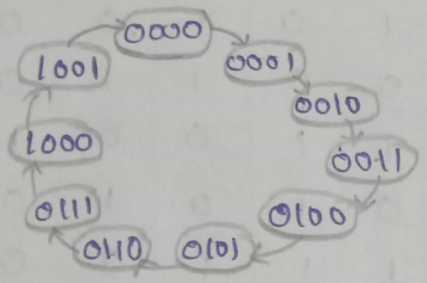
Step 1: n = 4, Flip-flop = T Flip-flop

range of counting = 0 to n-1 = 0 to 9.

Step 2: Excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 3: State diagram



Q_A	Q_B	Q_C	Q_D	Q_{A+1}	Q_{B+1}	Q_{C+1}	Q_{D+1}	T_A	T_B	T_C	T_D
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1
1	0	1	0	x	x	x	x	x	x	x	x
1	0	1	1	x	x	x	x	x	x	x	x
1	1	0	0	x	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x	x

T_A

Q_AQ_B \ Q_CQ_D	00	01	11	10
00				
01			1	
11	x	x	x	x
10		1	x	x

$T_A = Q_AQ_D + Q_BQ_CQ_D$

T_B

Q_AQ_B \ Q_CQ_D	00	01	11	10
00			1	
01			1	
11	x	x	x	x
10			x	x

$T_B = Q_CQ_D$

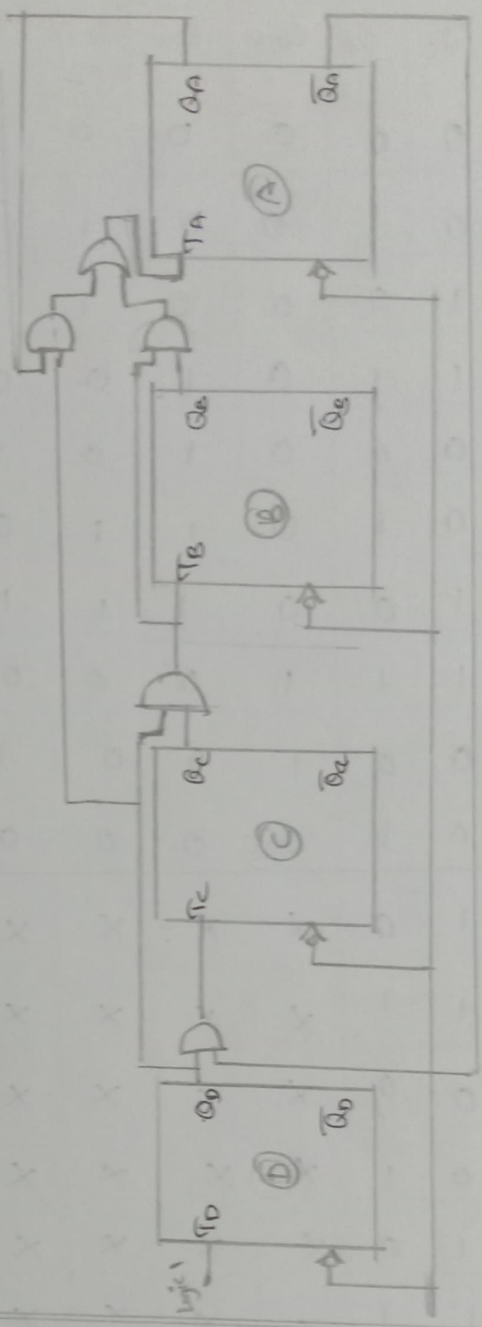
T_C

Q_AQ_B \ Q_CQ_D	00	01	11	10
00		1	1	
01		1	1	
11	x	x	x	x
10			x	x

$T_C = \overline{Q_A}Q_D$

$Q_A Q_B$ / $Q_C Q_D$	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	x	x	x	x
10	1	1	x	x

$T_D = 1$



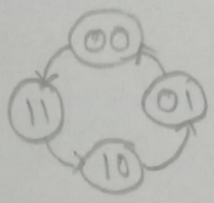
4) Design a 2-bit Synchronous using down-counter

$N = 2^n = 4.$

Excitation table for T flip flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

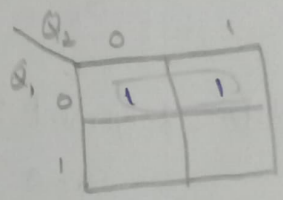
State diagram



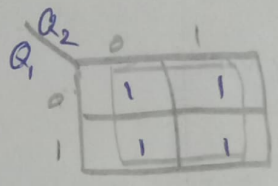
State table

Q_2	Q_1	Q_2^+	Q_1^+	T_2	T_1
0	0	1	1	1	1
0	1	0	0	0	1
1	0	0	1	1	1
1	1	1	0	0	1

Flip Flop

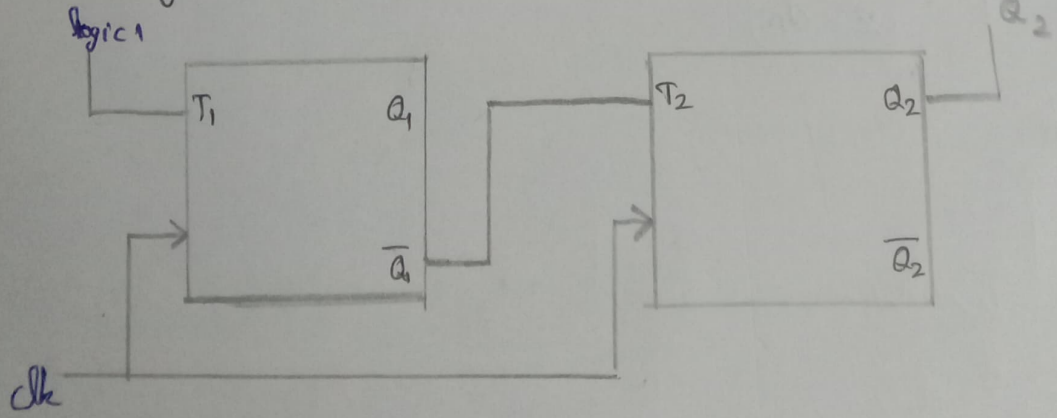


$T_2 = \overline{Q_1}$

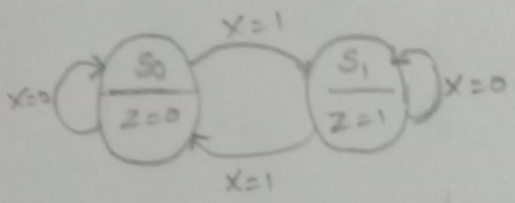


$T_1 = 1$

Circuit diagram:



6) Draw the state table for the following state diagram.



I State table:

Present state	Next state x=0	Next state x=1	O/P Z
S_0	S_0	S_1	0
S_1	S_1	S_0	1

II State assignment:

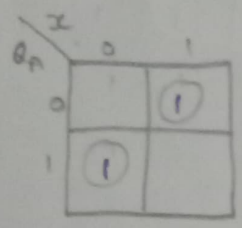
$S_0 = 0$

$S_1 = 1$

State table:

Present State Q_A	Next state x=0	Next state x=1	O/P
0	0	1	0
1	1	0	1

III K-map



$Q_{A+1} = Q_A\bar{x} + \bar{Q}_A x$

$D_A = Q_A \oplus x$

$Z = Q_A$

Logic diagram