Proceedings of the International Conference on Intelligent Computing and Communication for Smart World (I2C2SW-2018)
14-15 December 2018

An Ultra Low Power VLSI Architecture for Viterbi Decoder using Subthreshold Adiabatic Logic

M. Ruban Gladwin
Department of ECE
Jayaraj Annapackiam CSI College of Engineering
Nazareth, India
rubangladwin@gmail.com

N. Kasthuri
Department of ECE
Kongu Engineering College
Perundurai, India
kasthuri@kongu.ac.in

***Abstract*—In modern digital world, the major features expected are portability and reliability. There is a tremendous development in the field of wireless communication systems. Viterbi decoder, the heart of the wireless communication receivers, facilitates the correction of transmission errors occurred in the transmission channels. To realize a portable system, ultra low power digital integrated circuit design is vital. In this paper, we reduced the power consumption of Viterbi decoder and thereby reduced the heat dissipation of the integrated circuits. We propose a novel technique, Viterbi decoder based on sub-threshold adiabatic logic, to achieve power reduction. This approach is used where power consumption is the major concern instead of performance. It is observed that the power consumption of the circuits is more desirable compared with conventional static CMOS implementation.**

Keywords—Viterbi Decoder, Subthreshold Adiabatic Logic, Power Consumption

I. INTRODUCTION

In this digital generation majority of applications utilize wireless communication system, particularly mobile devices, digital TV, supercomputers and applications. For any kind of wireless communication standards (GSM, UMTS, CDMA, CDMA2000, WiMAX, Wi-Fi, DAB, etc) concerned, the problems associated are error correction of received codes through the noisy channel. So far, many sophisticated applications were developed in wireless communication systems. Still, power consumption and heat dissipation are the major challenges for researchers. Since wireless communication digital system is needed to process huge amount of data for such sophisticated applications, several low power design techniques are developed in the literature [7] – [12]. When huge amount of data is processed in the integrated systems, the amount of heat generated increases significantly. The increasing demand for low power design in integrated circuits has caused the growth of various low power design techniques. Viterbi algorithm was developed by Andrew J. Viterbi [1],the founder of Qualcomm Corporation. He addressed the problem of decoding of convolutional codes. Viterbi Algorithm is a maximum-likelihood decoding technique used to decode convolution codes with better BER performance. Viterbi Decoder (VD) performs forward error correction technique which is mostly suitable for the channel corrupted by Additive White Gaussian Noise (AWGN). Viterbi decoder implements Viterbi Algorithm (VA). This algorithm provides optimal solutions as shown by Omura [2], and Forney [3], [4].In 1968, Viterbi & Jacobs developed decoder chips for satellite communications and modems at LINKABIT Corporation. In 1971, Codex 9600 Modem was designed by G. D. Forney. In 1977, VA was used on Voyager Saturn/Jupiter flights communications by NASA. In 1985, Viterbi & Jacobs co-founded Qualcomm. In 1990, VA was used in PRML magnetic hard disk drives by IBM. In 1993, CDMA standard IS-95Awasreleased by Qualcomm. In 1997, a single-chip Viterbi + trellis decoder was released by Qualcomm [6]. Many schemes were proposed to reduce power consumption of the Viterbi decoder. Without degrading the performance of VD, power consumption is reduced with a pre-computation architecture utilizing T- algorithm [7]. Critical path timing error in ACS unit is rectified using Algorithmic noise-tolerance (ANT) technique and power reduction is achieved by voltage over scaling[8]. Implementing low-power Viterbi decoder using Scarce State Transition (SST) method reduces the overall memory accessing power. Uneven-partitioned memory architecture is used in trace-back Survivor Memory Unit (SMU) [9]. A low power State Sequential Viterbi Decoder with a large constraint length was developed for CDMA based personal communication services applications [10]. High speed, low latency TFU based Segmented Register Exchange (SRE) method for SMU in Viterbi decoder is designed to achieve significant power reduction [11]. SRAM based Viterbi decoder is proposed for wireless communication applications [12]. A novel scheme was proposed with a multi-stage pipelined Add Compare and Select (ACS) and cost-effective high-level soft decision Viterbi decoder for IEEE802.11ac systems [13].

In this paper, we propose a novel technique: VLSI hardware-based architecture of Viterbi decoder is designed using sub-threshold adiabatic logic technique and the power consumption of the device is discussed further. Section II discusses design background of convolutional encoder which is used in the transmitter side of communication system. Section III proposes methodology to achieve power reduction of Viterbi Decoder. Section IV covers the proposed design of ultra low power VLSI architecture for Viterbi decoder for wireless communication applications. Section IV compares the results of proposed work with existing systems. Finally, section V draws a conclusion.

II. DESIGN BACKGROUND

Convolutional encoding schemes are widely used in wireless communication systems mainly as forward error correction schemes. Convolutional codes are the most powerful modern error correcting codes used in various systems like LTE, 4G network standards. Figure 1 shows

the design of Convolutional encoder, a basic building block of the transmitter section in wireless communication system. The design is realized by Finite State machine (FSM) in which the output of the encoder depends on the input and present state of the registers. The *(1/2)* rate convolution encoder is used here; it produces 2 output bits for each and every single bit input. Figure 1 shows the design of basic ½ rate*(k/n)* convolutional encoder that has *k=1*bitinputand *n=2*bit code symbol outputs with constraint length *K=3*. The generator polynomials are *G1(1, 0, 1)* and *G2(1, 1, 1)*. Therefore the 2 bits code symbol outputs are calculated as follows.

$$output\ \ 1 = m1 + m3 \quad (1)$$

$$output\ \ 2 = m1 + m2 + m3 \quad (2)$$

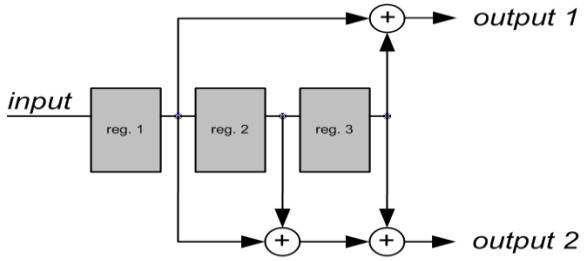

Fig. 1. Design of ½ rate Convolutional encoder

The rate of convolutional encoder is generally specified as (*k/n*) where *k* represents the number of input bits and n represents the number of output bits. *k/n* is also termed as the code rate. The code rate can be varied based on the needs of applications. The constraint length of encoder *K* represents the number of shift register used. As K value increases, the design complexity also increases. For example, if *K=5*, then$2^{5-1}=16$ number of states are needed for the design; and if *K=9*, then the number of states needed increases to *256*, which is very challenging. Convolutional encoder is realized in terms of state diagram and trellis diagram.

III. Design Methodology

Low power design is very important in realizing a digital system suitable for wireless applications. In view of that, devices are made to operate in sub-threshold region. When systems are designed with conventional static CMOS standard cell libraries, there is a tradeoff between power dissipation and performance. Therefore, we need to design our own library insisting sub-threshold operation. Some specific applications utilize the sub-threshold adiabatic logic whereperformance is not a primary concern. In sub-threshold adiabatic logic, transistors operate with power supply voltage V_{dd} near to thethreshold voltage $V_{th.}$ Here, sub-threshold leakage current is used as operating current. The dynamic power dissipation of the CMOS circuits arecalculated as, $P_{dyn} = C_L V_{dd}^2 f_{clk}$ Where P_{dyn}depends on the parameters like load capacitance C_L, Supply voltage V_{dd} and system clock frequency f_{clk}. The major problems associated with digitalsystems that were designed using static CMOS circuit's results in switching, short circuit and leakage power dissipation. When we operate transistor in sub-threshold region, need to scale down the supply voltage which improves the leakage and active power consumption but reduces speed of operation of the digital circuits.

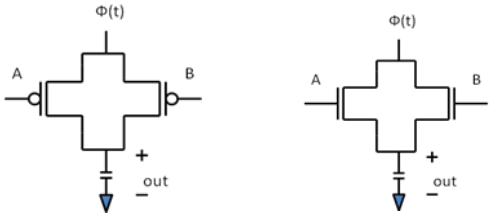

Fig. 2. SAL based NAND and NOR logic gates

A. *Sub-threshold Adiabatic Logic*

Sub-threshold Adiabatic Logic (SAL) is developed from the application of adiabatic logic which is operated in weak inversion region. In order to design digital systems with SAL, the conceptof power dissipation, process variation parameters, temperature, threshold voltage variations, leakage current and operating frequency should be fully understood. Fig. 2. shows the basic sub-threshold adiabatic logic based on NAND and NOR gates. These structures utilize either pull up or pull down network of conventional static CMOS logic. The main difference is that ramp signal type power supply voltage and devices are made to operate in sub-threshold region.

B. *Transistor(MOSFET) under Ramp Signal as Supply Voltage*

In adiabatic technique to reduce charge carrier movement, ramp supply voltage is used instead of dc power supply which reduces significant power consumption. A ramp type signal is defined as$\Phi\ (t) = t$ for $0 < t < T$ and $\Phi\ (t) = -t$ for $T < t < 2T$whichis periodic with time period 2T and frequency $f = (1/2T)$. The ramp type power supply voltage signal $\Phi\ (t)$swings between charging phase and discharging phase i.e.) 0V to V_{dd} for time duration T and V_{dd} to 0V for remaining time duration T.

IV. Proposed Ultra Low Power Viterbi Decoder

In this section we designedultra low power VLSI architecture of Viterbi decoder using sub-threshold adiabatic logic. In the proposed system design, the first step is to build a basic SAL based logic gates. After completing the verification of its functionality and timing constraints,standard cell library is built for those gates. These standard cell primitives are used to build architecture of Viterbi decoder in bottom up approach fashion. Further, analysis of SAL based Viterbi decoder is performed to demonstrate the energy consumption against supply voltage variations of proposed system in depth.

Fig. 3 shows the block diagram of Viterbi decoder. The convolutional encoder is used to convert actual information into code symbols and it is used in the transmitter side. When the transmitted signal is transmitted through the channel the transmitted information is corrupted when noise

gets added with the actual information. At the receiver, the major task is to estimate the actual information from the noisy coded symbol. Viterbi decoder that implements Viterbi algorithm ultimately estimates the actual code symbol from the received noisy sequence. Viterbi algorithm is the most common decoding technique used by many wireless communication application standards and is implemented using VLSI digital hardware.The performance of the decoder is measured in terms of Bit Error Rate (BER). Theoreticallyuncoded BER given by

$$P_{uncoded} \approx Q\left(\sqrt{\frac{E_b}{N_0/2}}\right) \quad (3)$$

Where, E_b is the energy per information bit. For the uncoded channel, $E_s/N_0 = E_b/N_0$, since there is one channel symbol per bit. For the coded channel with rate m/n, $nE_s=kE_b$ and thus $E_s= E_bk/n$. The loss in the signal to noise ratio is thus $-10log_{10}k/ndB$. For rate ½ codes we thus loose*3 dB* in SNR at the receiver.

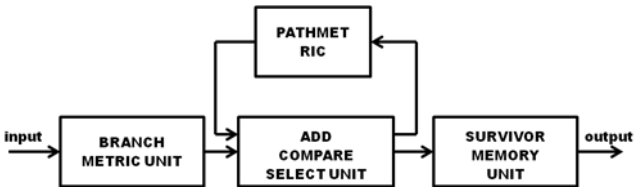

Fig. 3. Block Diagram of Viterbi Decoder

A hardware processor to realize the Viterbi Algorithm is achieved by implementing a Viterbi decoder. Three major blocks are concentrated in this design as we can see in Fig. 3. They are: Branch Metrics calculation Unit (BMU), the Add-Compare-Select unit (ACS), and the Survivor path Memory Unit (SMU).

A. *Branch Metric Unit*

When the coded sequence is transmitted through the noisy channel, due to inter symbol inference there is a possibility of occurrence of error in the coded sequence. As we can see on the receiver side, when we are receiving the data it contains some error bits due to the noisy channel. Viterbi decoder is used for forward Error correction codes which decode the error sequence. Branch Metric Unit is the fundamental block of Viterbi decoder. It computes the values ofBranch Metric (BM) between the received code sequence and expected sequence that is BMU which calculates the hamming distance between the two code sequences. Let us consider the received sequence r_k, and the expected code sequence t_k, and then the branch metric can be calculated as

$$BM_k = \text{Hamming distance } (r_k, t_k) \quad (4)$$

B. *Add Compare and Select Unit*

Viterbi decoder is designed based on the principle of Viterbi algorithm. This decoding operation depends on the state diagram, trellis structure of respective convolutional encoder. After computation of branch metric value, the next step is to compute the state metric and to select the survivor path. Fig. 4 shows the general block diagram of add compare select unit. It consists of adder, comparator and multiplexer.

The function of the adder unit is to add the branch metric and the State Metric value of each trellis stage. The comparator unit then compares the path metric values of the two adders and updates the new state metric value. Finally, the selector unit updates the path metric value of the Survivor Memory Unit.

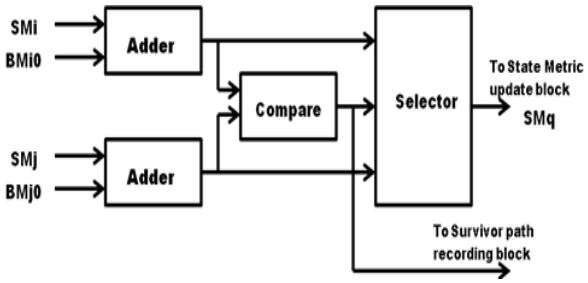

Fig. 4. Block Diagram of Add Compare Select Unit

$$SM1_i = Min\left(SM1_{i-1} + BM1, SM2_{n-1} + BM3\right) \quad (5)$$

The State Metric $SM1_{i-1}$, the Branch Metric *BM1* are added by adder1 and the State Metric$SM2_{i-1}$, the Branch Metric*BM3* are added by adder2. Both the adders compute the new state metric values. The lowest value is selected as new state metric or path metric and that should be treated as survivor path to the next trellis stage. Comparator unit is used to compare both the adder outputs. Selector unit selects the minimum state metric as a new state metric i.e.) $SM1_i$. The survivor path or shortest path which is stored in the survivor memory unit must be traced back to get the decoded data sequence.

V. Results And Discussions

In design environment, basic SAL based logic gates was designed in the schematic editor. A simulation was performed to meet the requirements like functional verification, timing verification, temperature variations, process variations and process parameters of SAL logic gates. Standard cell libraries were developed using the above designed gate primitives. With these standard cell libraries,all the internal blocks of Viterbi decoder were designed with the help of respective logic structures.

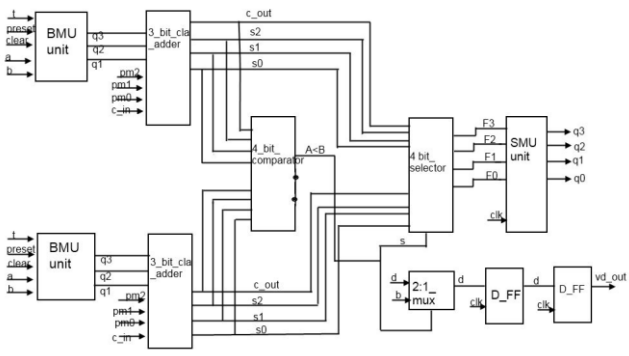

Fig. 5. Proposed Viterbi Decoder

Fig. 5. shows the design of the proposed Viterbi decoder. Each and every block of Viterbi decoder was designed using Sub-threshold Adiabatic Logic in schematic editor. Functionality of the proposed design is validated for 180nm technology with 2.5V supply voltage and 25MHz operating frequency. The simulation results of the proposed design shows significant improvements in terms of power consumption as tabulated below in Table I.

TABLE I. COMPARISON RESULTS

(Area vs. Power)

S.NO.	Logic Style	Power Consumption (mW)	Transistor Count
1	Static CMOS Logic VD	59.56	1682
2	Sub-threshold Adiabatic Logic VD	35.76	928

VI. CONCLUSIONS

From the above discussion, it is clear that the SAL based Viterbi decoder presented in this paper for the initiative in the literature is an eye-opener inultra low power research. We have investigated power consumption in terms of supply voltage variations, temperature variations and process parameters. Thisdesign saves considerable energy compared with the conventional static CMOS logic based Viterbi decoder at the expense of operating frequency. This proposed SAL scheme can be used infuture biomedical implants for devices deeply embedded within the body forenergy efficient embedded circuits where power consumption is the major issue.

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