Proceedings of the International Conference on Intelligent Computing and Communication for Smart World (I2C2SW-2018)
14-15 December 2018

2D Lifting Based Discrete Wavelet Transform Architecture Using Modified Reduced Hardware Algorithm

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***Abstract*—Lifting Based Discrete Wavelet Transform (LDWT) is the proficient mode to generate biorthogonal wavelet transforms and as well to work out classical wavelet transforms. This Modified Reduced Hardware Algorithm (MRHA) is based on a flipping technique in order to reduce arithmetic components with a straightforward control path. To achieve one multiplier delay of critical path and 100 percent hardware utilization efficiency the lifting data flow is performed using parallel computations. The proposed MRH algorithm is varied in accordance with the mathematical modifications.**

MRH algorithm uses associative principle which is applied to the mathematical modifications of the original lifting steps to reduce the number of arithmetic components required to perform compression. This architecture follows the basic lifting steps like splitting, predicting and updating but merges the predictor with the updater. By performing parallel operation using the two-input, two-output architecture the high pass and low pass values can be calculated. DWT provides high coding efficiency and better quality of image restoration when assimilate with the conventional Discrete Cosine Transform.

As a result, it is a speed competent, least hardware regular design with minimum memory requirement. Because of these competences it can be useful to several real-time visual setups viz. JPEG2000, MPEG-4 still texture object decoding, etc. The MRHA based architecture is verified in Lab VIEW tool that shows that the architecture splits the image into four sub-bands namely LL, LH, HL and HH. The architecture implemented on Xilinx ISE 8.2 tool indicates that, it is high speed architecture to compress an image and increases the speed by 20% when compared to existing architecture.

Keywords—LDWT, MRH Algorithm, JPEG 2000

I. INTRODUCTION

Discrete Wavelet Transform (DWT) is a relatively new computing-intensive transform which has been explored and several architectures have been proposed to achieve a performance level that is difficult to reach with traditional DSP devices. Wavelet transform is a relatively new methodology to analyze and represent a signal. Wavelet transform offers very unique features like Adaptive time-frequency windows and Lower aliasing distortion for signal processing as compared to Fourier Transform or Cosine Transform.

Memory is a key limitation in several image compression schemes. Present DCT-based compression algorithms demarcated under the JPEG standard practice memory precisely. They can drive on discrete image blocks as per the requirement and hence very low memory is sufficient. Wavelet-based coders are compression efficient than DCT-based coders but not their implementations.

Before emerging of wavelet based techniques reduction in memory plays major issue. This is also a wide zone of research doings associated through JPEG2000 standard. In JPEG2000 (5, 3), (9, 7), C (13, 7), S (13, 7), (2, 6), (2, 10) and (6, 10). Memory efficacy is indeed one of the supreme key issues in the area of extensive research activity related to JPEG2000 standard. To be yielding with JPEG2000, the codec has to acquire a (5, 3) filter in lossless approach and a (9, 7) filter in lossy method. In the hardware implementations of the DWT it is feasible to address the requirements of specific applications such as the speed, power or size of the circuit.

Because of the special features like progressive image transmission, simplicity in compressed image manipulation and region of interest coding DWT is most preferable for image compression. It has enormous applications in the field of science, engineering, and mathematics and computer science. Above all, it is used for signal coding in order to illustrate a discrete signal with an additional redundant form. Realistic applications can also be created in the field of signal processing of accelerations for gait analysis, in digital communications, etc. Special application includes the compression of images with high tolerable degradation. In large scale storage and data transmission, minimizations of bytes of a graphics file can be reduced by image compression. Hence the reduction in file size permits more images to be kept in a precised quantity of disk or memory space. Time minimization can be achieved for image transmission and reception over the Internet. There are number of research works in this field[1] – [16].

Yeong-Kang Lai [7] presented parallel scanning based pipelined memory efficient architecture for 2-D lifting-based DWT in JPEG 2000 applications. Pramod Kumar Meher[9]offered a multilevel Lifting 2-D DWT modular VLSI architecture with memory efficiency. Wei Zhang [15]proposed a speed efficient area minimized 2-D Discrete Wavelet Transform (2-D DWT) architecture. Chengjun Zhang [16] designed pipelined speed efficient VLSI architecture for 2-D Discrete Wavelet Transform (DWT).

Basant K. Mohanty[2] presented a pipelined parallel 1-D DWT using 2-D systolic array directly from the dependence graph (DG. Chih-Hsien Hsia [5]offered a memory efficient speed efficient algorithms and hardware architectures for 2-D dual-mode lifting based discrete wavelet transform (LDWT). Anand Darjietal.[1] developed a parallel flipping architecture using dual-scan technique for a lifting-based 2-D discrete wavelet transform. For this proposed work for comparison

purpose, this Flipped architecture in Parallel nature using Dual-scan Technique (FPDT) is considered as the best architecture and is modeled and compared with the proposed MRHA based architecture.

The rest of the paper is structured as follows. In Section I, Lifting based Discrete Wavelet Transform is elucidated. In Section II, We described about the lifting based 2D DWT Dual-Scan Parallel Flipping Architecture. The proposed 2D-DWT architecture using MRH algorithm is explained in Section III. In Section IV, results and performance comparison of FPDT and MRH based 2D DWT architectures are included. Finally, a short conclusion and future scope is specified in Section V.

II. LIFTING BASED DISCRETE WAVELET TRANSFORM

The lifting scheme is the modest and proficient algorithm used for the creation of bi- orthogonal wavelets. In lifting scheme all equations are derived in the spatial domain and there is no need of difficult mathematical calculations as per the traditional procedures. There is no dependency on Fourier transforms. Lifting scheme is applied to generate second-generation wavelets. These are not essentially a translation and dilation of an exact function.

This method provides some improved specific properties for a given discrete wavelet transforms. Lifting step can be changed to operate on integers without modifying the property of reversibility. Lifting scheme is composed of three steps in constructing wavelets. Initially in the first step the data is split into two sets of odd and even. Hence the name for this step is split. Then, odd set is predicted from the even set and is named as predict step. This step ensures polynomial cancellation in high pass. Finally it updates even set by means of wavelet coefficient to estimate scaling function. This step is the update step which ensures preservation of moments in low pass.

There are many advantages in lifting scheme when it is used for the image compression applications. They are in-place computation, allows reversible integer wavelet transforms and easy to implement.

The rule in lifting scheme is to split up the polyphase matrix of the wavelet filters into alternating upper and lower triangular matrices and a diagonal normalization matrix. As per the rule of lifting scheme, the polyphase matrix of a 9 / 7 lifting filter is given in equation (1).

$$P(z)=\begin{bmatrix}1 & \alpha(1+z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \beta(1+z) & 1\end{bmatrix}*\begin{bmatrix}1 & \gamma(1+z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \partial(1+z) & 1\end{bmatrix}\begin{bmatrix}k & 0\\ 0 & 1/k\end{bmatrix} \quad (1)$$

Here the predict polynomials are represented as α (1+ z−1) and as well γ (1+ z−1), update polynomials are specified with the symbolic representation of β (1+ z) and as well δ (1+ z) and the scale normalization factor is represented as k. The filter coefficients are α = −1.586134342, β=− 0.052980118, γ=0.8829110762, δ=0.4435068522 and k = 1.149604398(k is the scaling coefficient) for the 9/7 filter.

III. PARALLEL FLIPPING ARCHITECTURE USING DUAL SCAN TECHNIQUE

The lifting steps considered in [1] are described from equation (2) to equation (5) as follows:

$$\frac{d_i^1}{\alpha}=\frac{d_i^1}{\alpha}+(s_i^0+s_{i+1}^0) \quad (2)$$

$$\frac{s_i^1}{\alpha\beta}=\frac{s_i^0}{\alpha\beta}+(\frac{d_{i-1}^1}{\alpha}+\frac{d_i^1}{\alpha}) \quad (3)$$

$$\frac{d_i^2}{\alpha\beta\Upsilon}=\frac{d_i^1}{\alpha\beta\Upsilon}+(\frac{s_i^1}{\alpha\beta}+\frac{s_{i+1}^1}{\alpha\beta}) \quad (4)$$

$$\frac{s_i^2}{\alpha\beta\Upsilon\delta}=\frac{s_i^1}{\alpha\beta\Upsilon\delta}+(\frac{d_{i-1}^2}{\alpha\beta\Upsilon}+\frac{d_i^2}{\alpha\beta\Upsilon}) \quad (5)$$

In this computation the intermediary information are from unrelated routes, it can be computed in parallel fashion with the present system and well ahead it is exploited in the succeeding procedure. For illustration, in the procedure in (2), in the course of the working out phase of is synchronously calculated with the addition assignment between $s_i0$and s_i+10. In the same way equation (3) is computed. Through the second phase of lifting scheme in equation (4) and equation (5), signalsd_i^1 and $s_i^1$are scaled by the scaling coefficients in the order of 1/βγ and 1/γδ. Since outputs $\frac{d_i^1}{\alpha}$and $\frac{s_i^1}{\alpha\beta}$ are computed from the principal lifting process are applied to calculate the subsequent lifting phase, instead of 1/αβγ and 1/αβγδ the signals are scaled by 1/βγ and 1/γδ. The absolute outputs are scaled as specified by equation (6) and (7).

$$d_i=\frac{d_i^2}{k}\alpha\beta \quad (6)$$

$$s_i=s_i^2\times k\alpha\beta\delta \quad (7)$$

The data flow graph of existing method is given in fig. 1.

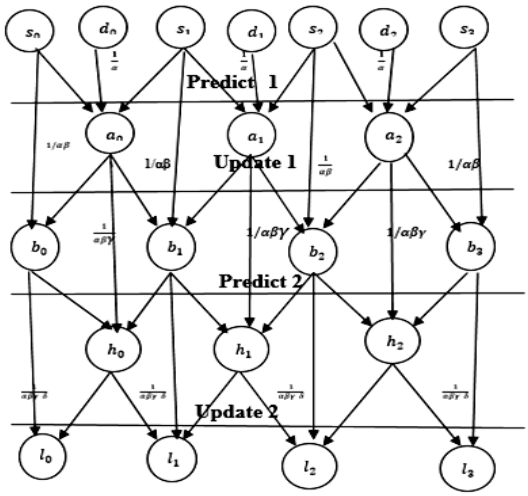

Fig. 1.DFG of Existing Method

The information route of the lifting phases can be modified with folded nature in order to minimize the area requirement but through the overhead of extra computation cycles. The recommended 2-D DWT design with MRH algorithm essentially includes three units, as given in Fig. 2.

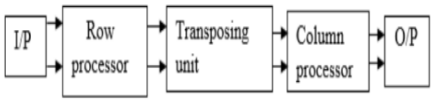

Fig. 2. Block Diagram of 2D DWT

The parallel flipping architecture (FPDT) using dual-scan technique is derived from the DFG of the proposed MRH method. Here the odd and even responses are processed in a Z-scan mode where the pixels are supplied on the occurrence of every clock in the course of its rising edge. The whole image is partitioned into a section of 2 × 2 pixels. A 1-D DWT is illustrious by alternative row processing followed at once by the column processing unit.

Z-scanning technique permits concurrent row and column processing procedure, follow-on in an insignificant constant latency and minimum transposing buffer requisite specifically self-determining of N. It consists of a row processor, column processor and a transposing unit. Row processor consists of adder and multiplier lines. Adder line computes contemporaneous and aforementioned even pixels though the multiplier path process the odd pixel and is multiplied by the pre calculated constant coefficients. Transposing unit converts the one dimensional data into two dimensional. Similarly Column processor is same as that of the row processor in operation but it also has a line buffer and two output lines.

With the aim to accomplish the scheming of 2- D DWT a Transposition Unit (TU) is sandwiched between the row processing unit and a column processing unit to compute 1-D phase. To develop a TU, five registers and a 4 × 2 multiplexer are used. The 1-D row processor produces two outputs namely the high pass (H) output coefficients and the low-pass (L) output coefficients which are transposed and are provided for to the 1-D column processing unit.

IV. MRH ALGORITHM

In the proposed MRHA based architecture mathematical modification is done, so that number of arithmetic components required to implement the architecture is reduced which also leads to the reduction of critical path.

$$d_i^1 = d_i^0 + \alpha(s_i^0 + s_{i+1}^0) \quad (8)$$

$$\frac{s_i^1}{\beta} = \frac{s_i^0}{\beta} + (d_{i-1}^1 + d_i^1) \quad (9)$$

Substitute equation (8) in (9) and use the associative law to reorder the expression gives the following equation (10)

$$\frac{s_i^1}{\beta} = s_i^0\left(\frac{\alpha}{\beta} + 1\right) + s_{i-1}^1 + \alpha s_{i-2}^0 + d_i^0 + \alpha(s_i^0 + s_{i+1}^0) \quad (10)$$

$$d_i^2 = d_i^1 + \gamma(s_i^1 + s_{i+1}^1) \quad (11)$$

$$\frac{s_i^2}{\delta} = \frac{s_i^1}{\delta} + d_{i-2}^2 + d_i^2) \quad (12)$$

Substitute equation (11) in (12) and again use the associative law to reorder the expression that results the following equation (13)

$$\frac{s_i^2}{\delta} = s_i^1\left(\frac{\gamma}{\delta} + 1\right) + s_{i-1}^2 + \gamma s_{i-2}^1 + d_i^1 + \gamma(s_i^1 + s_{i+1}^1) \quad (13)$$

Equation (8) is kept unchanged and Equation (9) is flipped by a factor β and merging the predict1 and update1 stages by associative principle Equation (11) is kept same as previous predict stage and Equation (12) is flipped by a factor δ in update stage and merging the predict2 and update2 stages using associative principle. By solving these equations number of arithmetic components gets reduced.

Fig. 3 shows that for the predict stage 1, current pixel and the next pixel is multiplied by the factor α and for the update stage 1, 1/β is multiplied with the predict factor. In predict stage 2, input is multiplied with γ. For the final update stage 2, coefficients are multiplied with 1/δ.

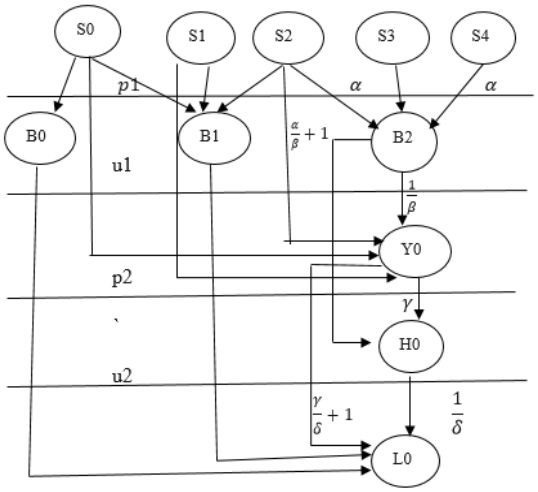

Fig. 3. DFG of MRHA Method

2D DWT architecture using 9/7 filter based on FPDT and MRHA are designed in Verilog Hardware Description Language. These designs are verified using Lab VIEW tool. The architecture is implemented on Xilinx ISE 8.2 tool and the performance comparison is done in terms of area, delay and hardware requirement.

V. RESULT AND DISCUSSIONS

Comparison of 2D DWT 9/7 Filter architecture based on the FPDT with the MRHA is listed in the Table 1.

TABLE I. COMPARISON OF 2D DWT 9/7 FILTER ARCHITECTURE BASED ON FPDT AND MRHA

Name of the Architecture	Area (μm^2)	Delay (nSec)	No. of Adders	No. of Multipliers
FPDT	8634	22.99	8	8
MRHA	5632	15.32	8	6

In the 2D DWT architecture based on MRHA, the area required is reduced by 34.77%, delay is reduced by 33.36 % and the speed increases by 20% when compared to the FPDT architecture shown in Table 1. Graphical representation of area comparison, delay comparison and hardware requirement comparison for the two 2D DWT architecture

using 9/7 filter with FPDT and MRHA is revealed in Figure 4, Fig. 4 and Fig. 5 respectively.

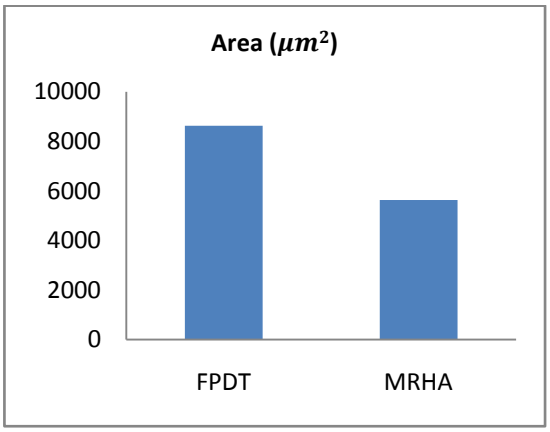

Fig. 4. Area comparison between FPDT and MRHA

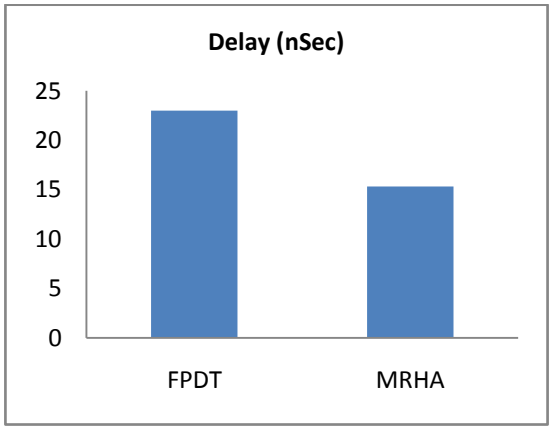

Fig. 5.Delay comparison between FPDT and MRHA

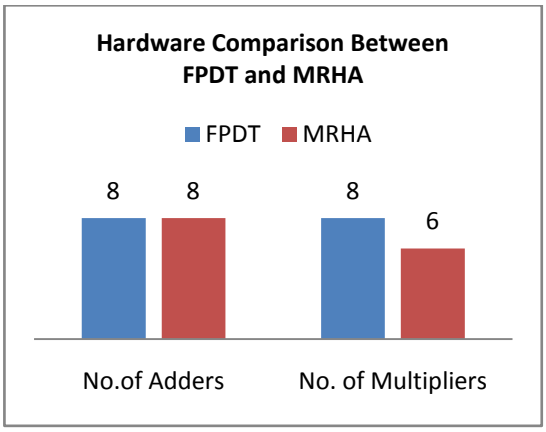

Fig. 6. Hardware comparison between FPDT and MRHA

VI. Conclusion And Future Scope

A high speed modified lifting based MRHA based architecture for 2D DWT by means of 9/7 filter is proposed and implemented on Xilinx ISE 8.2 tool indicates that, it increases the speed by 20% when compared to FPDT architecture. The results obtained from lab view verifies that the architecture splits the given image to four sub bands explicitly LL, LH, HL, HH. It has good hardware efficiency, lower memory size by way of a lesser density. It also shows a good reduction in memory constraint. From the analysis of the ASIC synthesis report, it is concluded that the MRH area reduced architecture is an appropriate choice with the existent uses similar to JPEG 2000, motion- JPEG and MPEG-4. In future, the MRHA architecture may be extended for compression of images in 3D Discrete Wavelet Transform.

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