Area and Power Efficient Approximate Wallace Tree Multiplier using 4:2 Compressors

S.Thava Bala
Department of ECE
Kongu Engineering College
Perundurai- 638 060
thavabala.s@gmail.com

D.Shangavi
Department of ECE
Kongu Engineering College
Perundurai- 638 060
shangaviraji @gmail.com

P.Sangeetha
Department of ECE
Kongu Engineering College
Perundurai-638 060
sangeetha2013@kongu.ac.in

***Abstract*– Over the years, the complexity of VLSI design circuits has increased dramatically. With this improvement, there comes the need for low area and low power VLSI circuits. The common known fact is that multiplier circuit plays an important role in the digital processor design. Nowadays, low power and low area multiplier designs are in high demand. Compared to other multipliers, Wallace tree multipliers are considered to be fast rather than other multipliers. For performing the process of multiplication, there will be many stages in-between and those stages are also having to be realized or implemented using additional gate circuits. This usage of additional circuits will finally result in increased area which in turn increases the power consumption also. To overcome these disadvantages, Approximate Wallace Tree Multiplier is implemented using incomplete adder cell (ICAC) and Accurate Compressor with Cin and Cout ignored (ACCI2) circuits. It is found out that it reduces the area compared to normal Wallace Tree Multiplier Design. Here, another method for Approximate Wallace multiplier using 4:2 compressors is proposed to keep the area overhead minimal. This method uses four to two compressors for addition and this circuit is used in the Approximate Wallace Tree Multiplier. The above designs are synthesized using Synopsys e and the power consumed and area occupied by both the methods is compared. By comparing, the multiplier with compressor minimizes the area by 98.39% when compared to Approximate Multiplier which also reduces the power consumption by 98.13%.**

***Keywords*– Approximate Multiplier, ACCI2, 4:2 Compressors**

I. INTRODUCTION

The functions like addition, multiplication play an imperative role for the processor design and application-specific integrated circuit design. Due to advances in VLSI design technologies, the circuits with large number of gates can also be practicable. ALU performs arithmetic operations like addition, subtraction, multiplication or logical operations like AND and OR, etc. With the use of addition, subtraction and shifts, it is possible to build the operations of multiply and divide. Addition and subtraction are important fundamental functions in arithmetic operations. They take part in many applications especially Digital Signal Processing. They also increase the speed of the circuit as most of the DSP and DIP has multiplication part. Eventually, the fact is that the designer always requires low power, low area and high speed digital VLSI circuit.

Approximate Multiplier is considered to be the efficient technique for reducing the area and power of VLSI circuit design. The advantage of using approximate multiplier is that it provides considerable speed, low area and reduces power consumption. The only disadvantage of approximation is that it reduces accuracy. The approximate multipliers design can be used in applications like Multimedia, Digital Image processing, recognition and mining operations. Compared to array multipliers, Wallace tree multiplier provides higher speed as it overcomes carry propagation delay and also approximate multipliers provide high speed than conventional multipliers. During multiplication of two numbers, Partial products have to be generated , reduced and then they have to be added by Carry Propagation Adder(CPA).

This paper explores the idea of using 4:2 compressors instead of using ACCI2 circuit which reduces area and power consumption. The organization of the paper is as follows. Section II explains the existing Approximate Wallace tree multipliers using ACCI2 circuit. Section III explains the proposed AWT multiplier using four to two compressors. Section IV discusses the simulation and synthesis results obtained for both circuits. Section V discusses the conclusion & future scope.

II. EXISTING APPROXIMATE WALLACE TREE MULTIPLIER

A. Incomplete Adder Cell

In this section, the existing technique of approximate Wallace tree multiplier using ACCI2 multiplier is discussed. The main objective of existing method is to reduce the rows to half by incorporating InComplete Adder Cell (ICAC) which is nothing but an approximate half adder.

A general schematic of exact and inexact Adder cell is depicted in Fig.1.

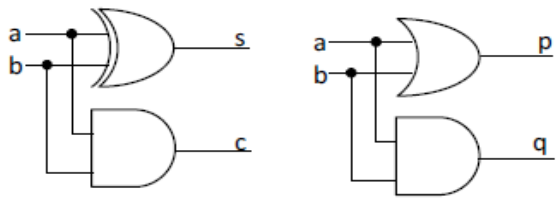

Fig. 1. Exact Half adder and Inexact Half Adder

In accurate half adder, the EX-OR gate and AND gates are used. The equation of sum is A + B and carry is AB. In approximate multiplication, the sum is an approximate value. So, for all the inputs, the sum and carry are equal, except the input 11. The accurate half adder has an output of sum as 0 and carry as 1.For the incomplete adder cell, the sum is 1 and the carry is 1. The sum is different for both, but

it is not considered as a major problem. The Table 1 shows the possible combinations of accurate and inexact adder.

TABLE 1. TRUTH TABLE OF HALF ADDERS (EXACT AND INEXACT HALF ADDER)

Inputs		Outputs			
a	b	Exact Half adder		Inexact Half Adder	
		Sum s	Carry c	Sum p	Carry q
0	0	0	0	0	0
0	1	1	0	1	0
1	0	1	0	1	0
1	1	0	1	1	1

B. Approximate Wallace Tree Multiplier

Fig 2 shows the simplified block diagram for the structure of Approximate Wallace tree multiplier using ACCI2.

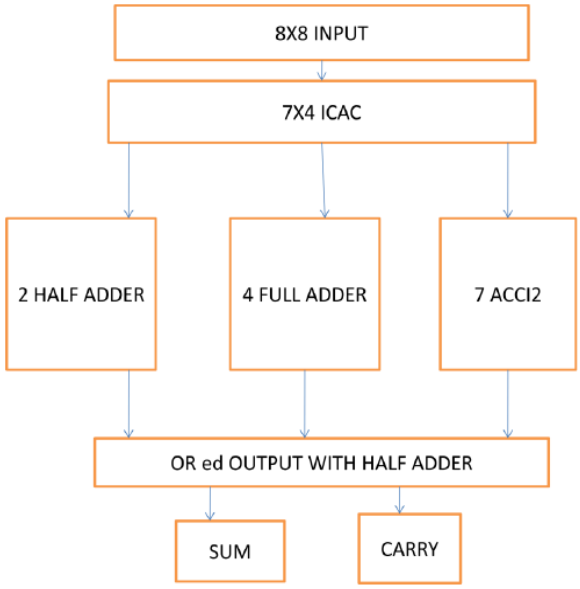

Fig. 2. Simplified Block diagram of AWT using ACCI2

This method consists of 8x8 inputs which feed into four rows and seven columns, two input ICAC is used. According to the inputs which are generated from the sum and carry of the ICACs output, the inputs will undergo an implementation of half adder, full adder and ACCI2 correspondingly. Finally the outputs from these half adders, full adders and ACCI2 are the required sum and carry will be obtained by using half adder.

Assume a Wallace tree multiplier (n*n bit). During multiplication, n number of partial products is obtained. By using ICAC circuit, each pair is replaced by one sum and one carry as p and q respectively. By using Incomplete Adder Cell, n partial products are reduced by n/2. The sum is reduced to n/2 c's and carry is reduced to n/2 e's respectively. The carry of rows e1, e2, e3, e4 is reduced into a single row d by using OR gate operation. By using this technique, n rows are reduced to n/2 rows (ie) half of the rows are reduced.

Fig 3 shows the overall structure of Approximate Wallace Tree Multiplier (8*8).In each row, every black encircle notates one Partial Product. This 8*8 (64) partial product tree is divided into 4 rows of p's and rows of q's using ICAC circuit. Each group of partial product consists of seven ICAC. The construction of seven ICACs of four rectangle boxes generate 4 approximate outputs (sums and carry) and are represented as c1, c2, c3 and c4 for sum and e1,e2,e3 and e4.Each encirclements in Stage 1 with rectangular boxes shows the usage of iCAC circuit which has a total of seven iCACs. Each row of partial product has one bit which is left by the ICAC.

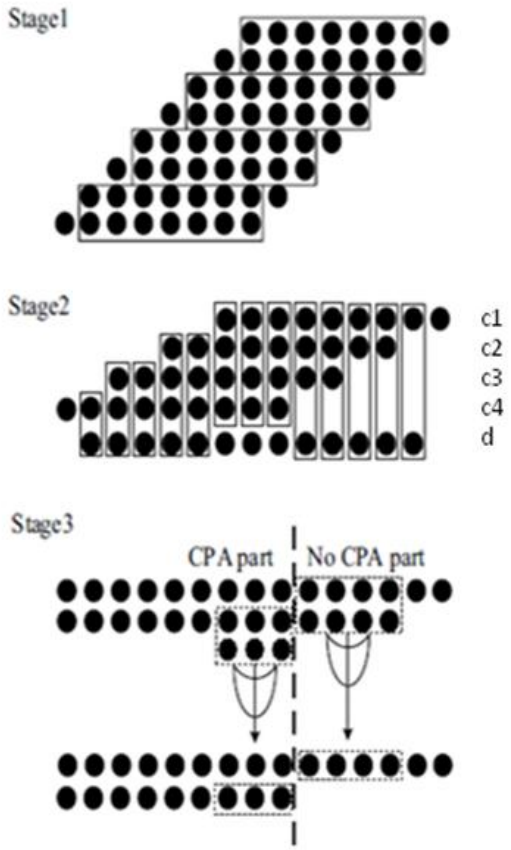

Fig. 3. Structure of Approximate Wallace Tree Multiplier for 8 bit multiplier

In stage 1, the structure compresses 8 rows to 4. Here, eight partial products are reduced to four partial products.

In stage 2, seven ACCI2s are used to compresses the rows. Here, 4 normal full adders and 2 normal half adders are used in addition to ACCI2s. In the next stage, the single bit column will be carried to the next step. The columns which consists of two bits will be executed using half adder and the three bit columns will be executed using full adders and the four bit columns will perform ACCI2 technique and for the five bit columns the first four bits will be taken and it will be performed using ACCI2 technique and the remaining single bit will be carried to the next stage.

The Fig.4 shows the circuit diagram for ACCI2 circuit. This circuit consists of sub circuit called AO222 which means AND-OR 2 2 2 gate which consists of three AND gates & its outputs are given into OR gate. And this ACCI2

also consists of AOI gate i.e. One AND-OR gate. This totally consists of 9 gates including two EXOR gates and one or gate. In this circuit, the 4 bit column is given in order to get carry and sum.

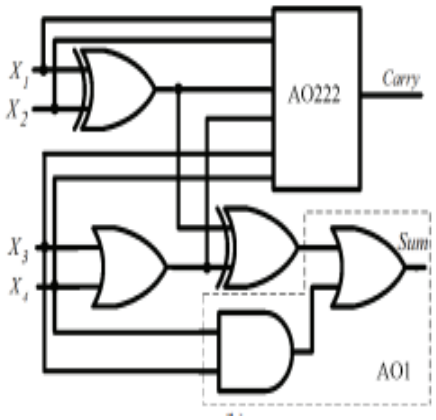

Fig. 4. Circuit diagram of ACCI2

In Stage 3, the sum of the past stage will be given in the first row and the carry will be diagonally given in the second row correspondingly. And the bits which are uncovered will be reduced to single carry row by performing OR operation with the corresponding carries. The no carry propagation part (no CPA) will be reduced to single row by using or operation and kept constant. Then the carry propagation part CPA) will be reduced using the half adder and the sum will be joined with the no carry part in order to give the output.

III. Proposed Approximate Wallace Tree Multiplier Method

This section presents 4:2 compressors based approximate Wallace tree multiplier. The 4-2 compressor consists of 4 gates i.e. 2 AND gates and 2 OR gates accordingly. This 4:2 compressor will correspondingly reduces the use of complexity of gates which accordingly reduces the gates, area and power consumed. This 4:2 compressor will be the good replacement for ACCI2.

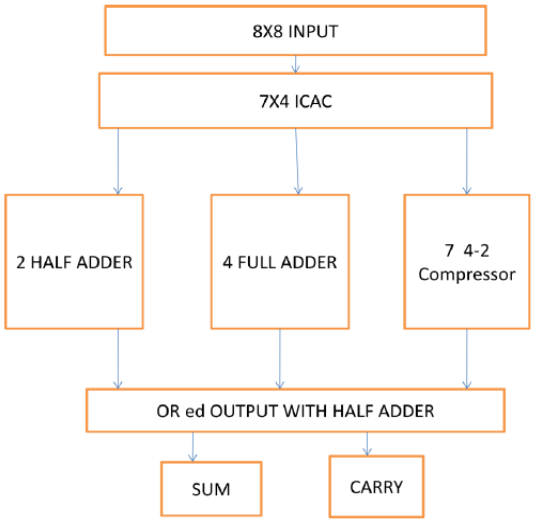

Fig.5. Simplified Block diagram of AWT using compressor

Fig 5 shows the simplified block diagram for the structure of Approximate Wallace tree multiplier using 4-2 Compressor. Here, instead of using ACCI2 in existing method, Compressors are used to reduce the area.

Fig 6 shows the schematic diagram of 4:2 compressors

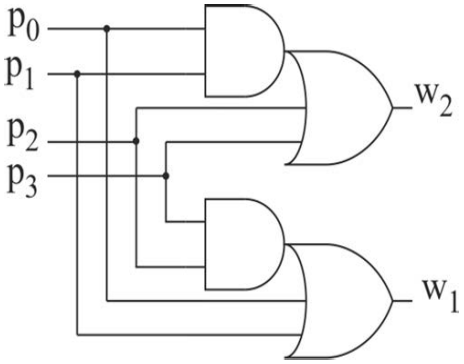

Fig. 6. 4 to 2 compressor circuit

At stage 2, the four inputs are processed by using 4:2 compressors.

In stage 3, the lower column with less than 3 bits is considered as No Carry Propagation Part (CPP). A One OR gate is used by the No CPA part to reduce the number of columns. Then, the remaining two groups of columns in CPA Part are reduced by using half adders, which generates sum and carry.

IV. Experimental Results

In this section, the simulation and synthesis result of Approximate Wallace tree Multiplier using ACCI2 technique and 4:2 Compressors is discussed. The simulation is carried out by using Modelsim 6.6 and synthesized using Synopsys.

A. Simulation Results

Fig.7 shows the simulation output of existing Wallace Tree Multiplier using ACCI2 Technique.

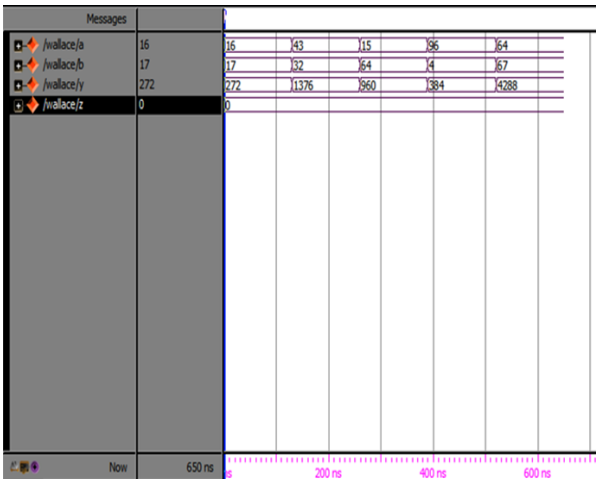

Fig.7.Simulation output of AWT multiplier using ACCI2

For example, a= $(10000)_2$ =16 and b= $(100001)_2$ =17 are given as input and it produces intermediate sum as y =$(100010000)_2$ =272 and carry as 0.

Fig.8 shows the simulation output of Proposed Approximate Wallace tree multiplier using 4-2 Compressor.

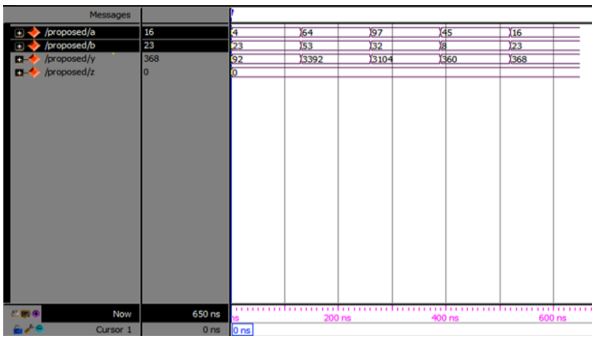

Fig.7.Simulation output of AWT multiplier using 4:2 compressors

Here, for example, a= $(10000)_2$ =16 and b= $(00010111)_2$= 23 are given as input and it produces intermediate sum as $(0000000101110000)_2$ =368 and carry as 0.

B. Power analysis

Table II gives the power consumption of both AWT with ACCI2 technique and Compressors.

TABLE II. POWER ANALYSIS OF TWO APPROXIMATE WALLACE TREE MULTIPLIERS DESIGNS

Power consumption (milli watt)	**Using ACCI2**	**Using 4:2 compressor**
Total power	5.2432mW	0.0982mW

C. Area analysis

Table III shows the Area occupied by both Approximate Wallace tree Multiplier using ACCI2 technique and 4:2 Compressors.

TABLE III. AREA ANALYSIS OF TWO APPROXIMATE WALLACE TREE MULTIPLIERS DESIGNS

Approximate Wallace Tree Multiplier	**Area (in $\mu m^{2)}$**
Using ACCI2	2143.565637
Using 4:2 Compressor	34.420660

From Table III, the area occupied by different designs is analyzed. AWT multiplier using 4:2 compressor designs consumes nearly less area than the AWT multiplier using ACCI2 design.

V. CONCLUSION&FUTURE SCOPE

The Approximate Wallace Tree multiplier based on 4:2 compressors has been presented in this paper. Exhaustive synthesis results show that the above technique improves the performance of the design with respect to the existing Approximate Wallace Tree Multiplier using ACCI2 technique.

Thus, the area and power consumed by AWT multiplier using 4:2 compressors design is less compared to the AWT multiplier using ACCI2 design.

In future, the above AWT multiplier using 4:2 compressors method may be implemented in applications where the inaccurate results are tolerable, image processing, filters like FIR filters, Signal processing applications, etc.

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