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A Novel Ternary Half Adder & One Bit MultiplierCircuits based on Emerging sub-32nm FET Technology

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***Abstract*—In this paper, we present a novel low-power and high-performance new ternarylogicarithmetic circuit that is implemented by double gate (DG) FinFET and graphenenanoribbon (GNR) field effect transistor (GNRFET). Multiple-valued logic (MVL) such as penternary, quaternary and ternary is a promising alternative to the binary logic design, because of less complexity, less computational step and reducedchiparea.The basic ternary gates and its operationarealready described in my previous paper [20]. Ternary logic gate based arithmetic combinational circuits such as ternary half adder and one-bitternarymultiplier are designed.The proposed ternary combinational circuits are simulated using HSPICE via standard 32nm DG-FinFET and GNRFET technology. Extensive simulation results demonstrate that the Graphene field effect transistor based ternary logic arithmetic circuits are more improved than the DG FinFET technology in terms of power consumption, delay and Power delay product (PDP).**

Keywords—Double gate field effect transistor,FET,Graphene field effect transistor, MVL, Ternary Half Adder, Ternary Multiplier.

I. INTRODUCTION

In the past several decades, complementary metal oxide semiconductor (CMOS) technology has created many sophisticated devices and systems such as cameras, cell phones, computers, and many other electronics.Constantlyscaling down the size of CMOS transistors and integrating more and more devices on a single-chip, CMOS technology is encountering tremendous challengesas the size reaches nanometer scale. One of the challenges is that the chips get very hot. Another physical limit is the indivisibility of atoms.Due to the limitation for miniaturization of CMOS transistors possess issues for researcher and directs the research towards the alternative semiconductorthan silicon. The alternative of silicon in near future isdouble gate (DG) FinFET, graphenenanoribbon (GNR) field effect transistor (GNRFET) and Carbon nanotube field effect transistor (CNFET). Since extensive research report already presented based on CNFET devices. So, we selected our choice of interest devices as graphene field effect transistor and double gate field transistor.

In the present electronic era, all the computers are operated based on Booleanbinary number system (radix-2). Due to the carry generation and high propagation delay such computers are not suitable for parallel arithmetic computing. Many techniques have been proposed in the literature to alternate and or solve this problem suchas, negative radix representation [1], reduced number system (RNS) [2], radix-2 modified signed digit(MSD) [2,3], modified trinarynumber(MTN) [4,5], etc. All of these proposals are based on radix-2 number system. In general, as radix of the number system increases, smaller number of digits necessary to express a given quantity. Multi-valued system is the best alternative for generation to come for increasing the data carrying capacities, large information storage and high-speed arithmetic operations [6]. Ternary logic(radix=3) system has a great contribution in this regard. In general, the decimal equivalent of an n-bit ternary number(an-1…a1a0)3 can be written as

$$D = \sum_{i=0}^{n-1} a_i 3^i \tag{1}$$

The paper is organized as follows. In Section II presents a brief review of Ternary Logicfunction.SectionIIIexplore the proposed Ternary arithmetic circuit designs andessential circuitries. The simulation results are illustrated insectionIV, which also include transient analysis and comparison analysisof Power Delay Product [PDP] of two different technologies. Section VI concludes the paperwith the discussion.

II. TERNARY LOGIC FUNCTION

Ternary logic has three logical values that show the third value compared to binary logic (0, 1). Ternary logic uses 0, 1, 2 respectively for false, undefined and true representation.

$$V(x) = \begin{cases} 0; \text{ if } x \text{ is false} \\ 1; \text{ if } x \text{ is perhaps true, perhaps false} \\ 2; \text{ if } x \text{ is true} \end{cases} \tag{2}$$

The main advantage of the ternary logic is that, it reduces the number of required computation steps. Since each signal can have three distinct values, the number of digits required in a ternary family is [log32] times less than required in binary logic. So, if we consider an N-bit binary adder, then the corresponding ternary adder has [log32*N] digits, where [x] represents the integer nearest to x and greater than x (i.e. the ceiling function) [6 -10]. Table I. below shows voltage level assignment to Ternary Logic Values.

There are three logic values for signals in these circuits. So, when analyzing ternary circuits, we should consider the response to six transitions of input signals between three voltage levels as well as the response of circuits to three values of input signals.

TABLE I. LOGIC SYMBOLS FOR CORRESPONDING VOLTAGE LEVEL

Voltage Level	Logic Value
0	0
1/2Vdd	1
Vdd	2

III. PROPOSED TERNARY ARITHMETIC CIRCUIT

The ternary gates presented in the GowriSankar et.al can be used for designing ternary arithmetic circuits such as ternary half adder and multiplier.In the proposed design, the diameters of GNRFETs are 1.47, 1.09, and 0.79 nm, and the chirality ofthe CNTs would be (18, 0), (16, 0), and (10, 0), respectively. Thus, by changing the chiralityvector, the threshold voltage values are also change 0.293, 0.398, and0.557 V, respectively.

A. Proposed Ternary Half-Adder.

A ternary half adder (HA) is is a combinational circuit that adds two ternary inputs and represents ternary Sum and Carry in output. The truth table of the ternary half adder is shown in Table II. A modified ternary HA architecture is proposed in this paper, and is shown inFig.1, which consists of transmission gates and GNRFET transistors to provide Sum and Carry.

TABLE II. TRUTH TABLE OF HALF ADDER

A	B	SUM	CARRY
0	**0**	**0**	**0**
0	**1**	**1**	**0**
0	**2**	**2**	**0**
1	**1**	**2**	**0**
1	**2**	**0**	**1**
2	**2**	**1**	**1**

In designing the Carry circuit (Fig. 1b), the diameters of T1 and T2 transistors are both 0.783 nm and their threshold voltages are both 0.557 V; therefore, p-type transistor (PCNTFET) is turned on with 0 and n-type transistor (NCNTFET) is turned on with 2. In both cases, 0 is transmitted to the output.

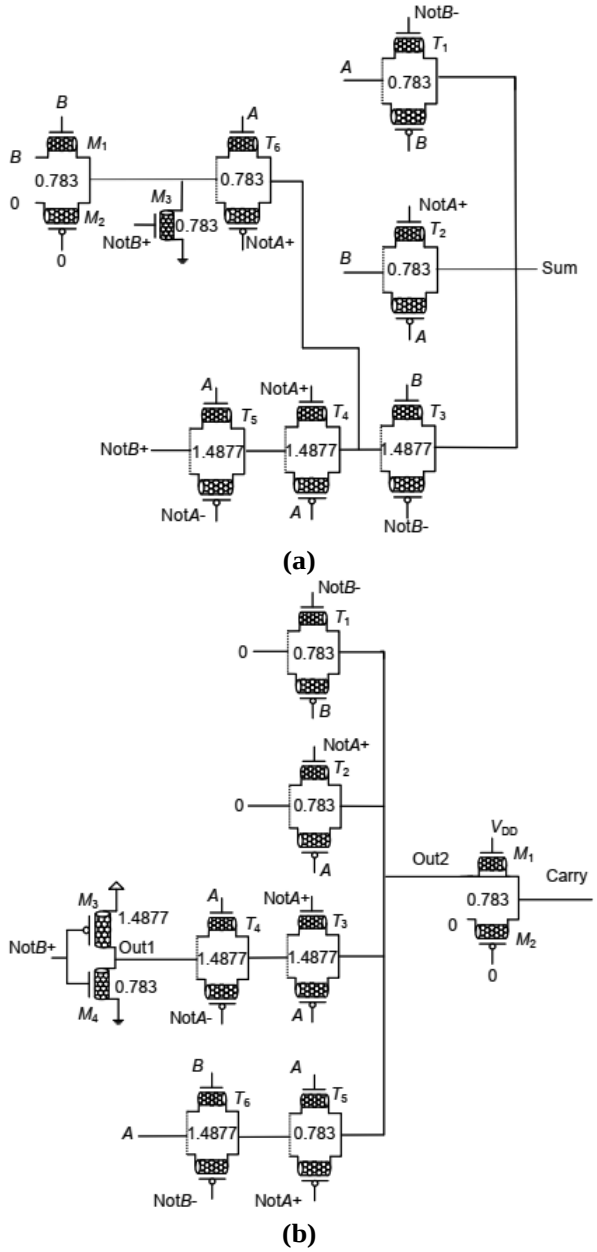


Fig. 1. Schematic diagram of Proposed GNRFET based ternary half adder: (a) Sum; (b) Carry

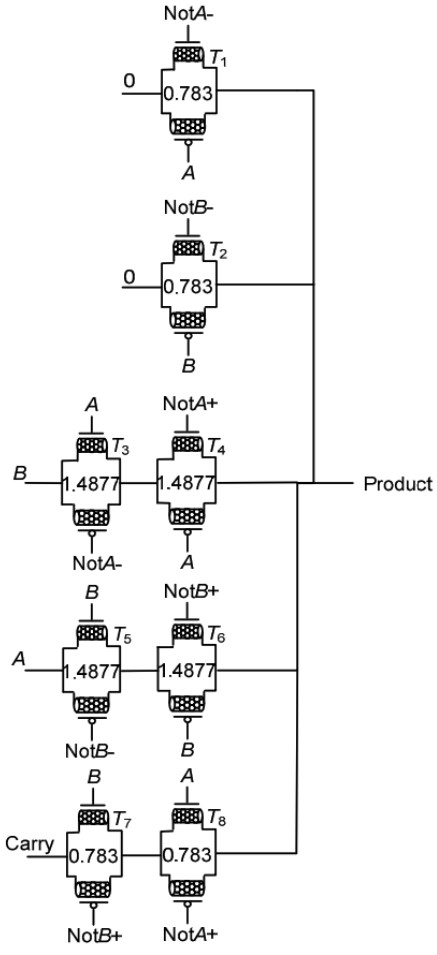
Similarly, if A=0, in T2 both transistors are ON; therefore, the output voltage will be equal to 0. The threshold voltages of T3 and T4 are both 0.293 V; when the input voltage of A is 0 or 1, T3 is ON, and if A is 1 or 2, T4 is ON. While A=1, T3 and T4 are ON simultaneously. In this case, if B=0 or 1, Out2 will be 0; otherwise, it will be 2. If A=2 and B=1 or 2, then T5 and T6 are ON respectively and Out2 will belogic 2 since Out2 is connected to one resistive divider between M1 and M2; consequently, when Out2 is equal to 2, Carry is 1.In the Sum circuit design(Fig. 1a), when either of the inputs A and B is the logic 0, Sum will be equal to the other input by T1 or T2. When B input is 1 or 2, if A=1, the output will be equal to positive not B (NotB+) through T3, T4, and T5. If A=2, T6 is ON; if B=1 or 0, M3 is ON. Therefore, the output reaches GND (logic 0). In this case, if B=2, M1 and M2 are ON and M3 is OFF. Thus, with a resistive divider between M1 and M2, the output logic is equal to 1.

B. Proposed Ternary One Bit Multiplier.

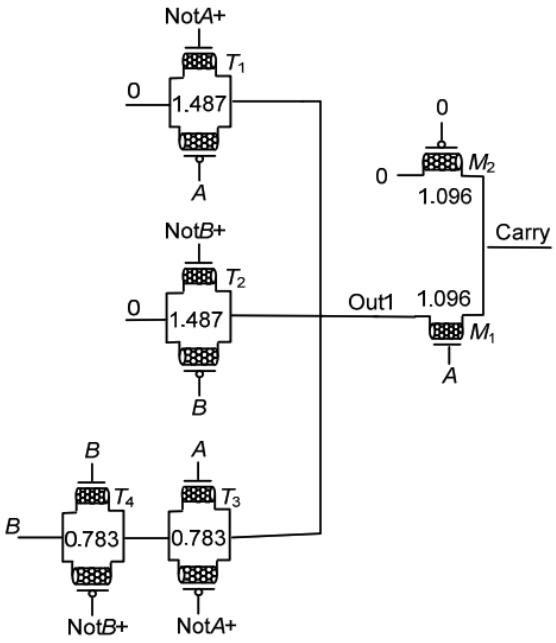
Multipliers are known as the main key element of arithmetic systems. The truth table of the ternary multiplier is shown in Table III. Fig. 2 shows the proposed ternary multiplier, which consistsoftransmission gates and CNT transistors to provide Product and Carry.

TABLE III. TRUTH TABLE OF ONE-BIT MULTIPLIER

A	B	Product	Carry
0	0	0	0
0	1	0	0
0	2	0	0
1	0	0	0
1	1	1	0
1	2	2	0
2	0	0	0
2	1	2	0
2	2	1	1



(a)



(b)

Fig. 2. Schematic diagram of Proposed GNRFET based ternary ternary multiplier: (a) Product; (b) Carry

In the Product circuit design (Fig. 2a), due to the truth table, if one of the inputs is 0, the output will be equal to 0 by T1 or T2. When either of the inputs is logic 1, the Product will be equal to the other input; for example, when A=1, T3 and T4 are ON, and B is transmitted to the output. If both A and B are equal to 2, T7 and T8 will be ON and the Carry will be used to calculate the Product.

In designing Carry (Fig. 2b), when one of the inputs is less than logic 2, Carry will be zero. The diameters of all the transistors of transmission gates (T1, T2, T3, and T4) are 1.4877 nm and their threshold voltages are 0.293 V. When A=0 or 1, T1 is ON and transfers 0; when B=0 or 1, T2 is ON and passes 0. T3 and T4 will be ON only if A=2 and B=2, and Out1 is pulled up to 2. In the output of the design, M1 and M2 are always ON. When Out1=0, Carry is equal to 0; when Out1=2,Carry will be at logic 1.

IV. SIMULATION RESULTS ANALYSIS AND COMPARISON

A. Experimental Setup

The proposed ternary logic arithmetic circuits are extensively evaluated in various test condition. All the circuits are simulated using HSPICEsimulator tool with standard SPICE model for 32nm FinFET and GNRFET technology. FinFET transistor aspect ratio is sized for minimizing the Power-Delay Product (PDP) using the prior published values. More information about the DG FinFET device model can be found in [11-15]. The technological parameters of the FinFET model with brief descriptions are shown in Table IV. Like that, the GNRFET standard model has been designed for unipolar, MOSFET-like GNRFET device [16-19], in which each transistor may have one or more graphenenanoribbons. The technological parameters of the GNRFET model with brief descriptions, are shown in Table V.

TABLE IV. DG-FINFET DEVICE AND ITS PARAMETER VALUES

Device Parameter	Description	Value
Vth	Threshold voltage of the devices	0.29 V
Lg	Channel Length	32nm
Tsi	Fin thickness	8.6 nm
Tfin	Thickness of the FinFET devices	8.6 nm
Tox	oxide-layer thickness	1.4 nm
Nch	Channel doping concentration	2 x 10^{16} cm-3
Hfin	Height of the FinFET devices	13 nm
Lg	Channel length	32 nm
Doping profile	Channel impurity doping type	Uniform
Gate material	Type of gate material	Metal

TABLE V. GNRFET DEVICE AND ITS PARAMETER VALUES

Device Parameter	Description	Value
T_{ox}	The thickness of top gate dielectric material (planer gate).	0.95nm
L	Physical channel length	32 nm
nRib	The number of GNRs in the device.	6
Dop	Source and Drain reservoirs doping fraction	0.001
T_{ox2}	Oxide Thickness between channel and substrate/bottom gate	20nm
2*sp	The spacing between the edges of two adjacent GNRs within the same device.	2.0nm
N	The number of dimer lines in the GNR lattice	12
P	The edge roughness percentage of the device	0
gates_tied	Whether Gate or Sub hold the same voltage	0

B. Test Bench for the Proposed Circuit

The Proposed circuit is characterizedin-terms of the speed and power consumption with respect to low supply voltagesfrom 0.6V, 0.8V and 1V supply voltage. The test bench for the proposed circuit is shown in Fig. 3. Input signals to the ternary logic circuits are driven by inverters that are driven by ideal voltage sources. In order to consider, the transition time degradation from the fan-out, the data inputs signal is also loaded with CL.

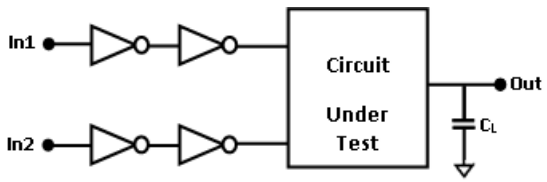


Fig. 3. Test bench of under circuit test

Simulations are carried out in various supply voltage and loads condition at room temperature. The proposed ternary arithmetic circuit performance can be evaluated by calculating the delay, power consumption and power-delay product (PDP). PDP is the multiplication of the average power consumption and the maximum delay. Thus, PDP could be an important parameter for evaluating and comparing the performance of the FinFET and GNRFET-based ternary combinational circuits.

C. Performance Evaluation of Proposed ternary arithmetic Circuits.

The robustness and performance of the proposed ternary logic arithmetic circuits are examined extensively by conducting experiment at various supply voltage and load capacitance values. The circuits are simulated at 0.6V, 0.8V and 1V supply voltages at 250 MHz operating frequency with various output load capacitors, ranged from 0.7fF up to 3.5fF. The detailed results of this simulation are listed in Table VI respectively. The power-delay-product (PDP) comparisonresults are plotted in two dimensional charts, which are shown in Fig. 06to Fig. 09respectively. The results of these charts could be useful for better analyzing the driving capability of the proposed design. The proposed GNRFET-based ternary logic half adder and one bit multiplier transient response performance characteristics are shown in Fig. 4&5 respectively.

Thus, the proposed ternary logicarithmetic circuit performance characteristics are studied using state-of-the-art 32nmDGFinFET and 32nmGNRFET technology in term of speed, power consumption and PDP. Results of the comprehensive simulations demonstrate that GNRFET-based ternary circuit have a considerable improvement in terms of delay, Power consumption and PDP in comparison with the other conventional state-of-the-art 32-nm DG-FinFET technology, in various situations.

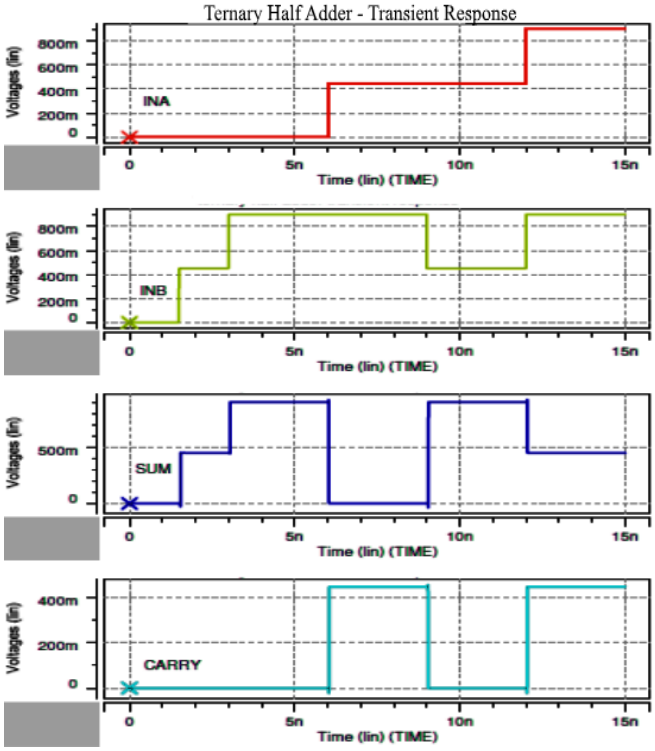


Fig. 4. Transient responseof GNRFET based ternary half adder

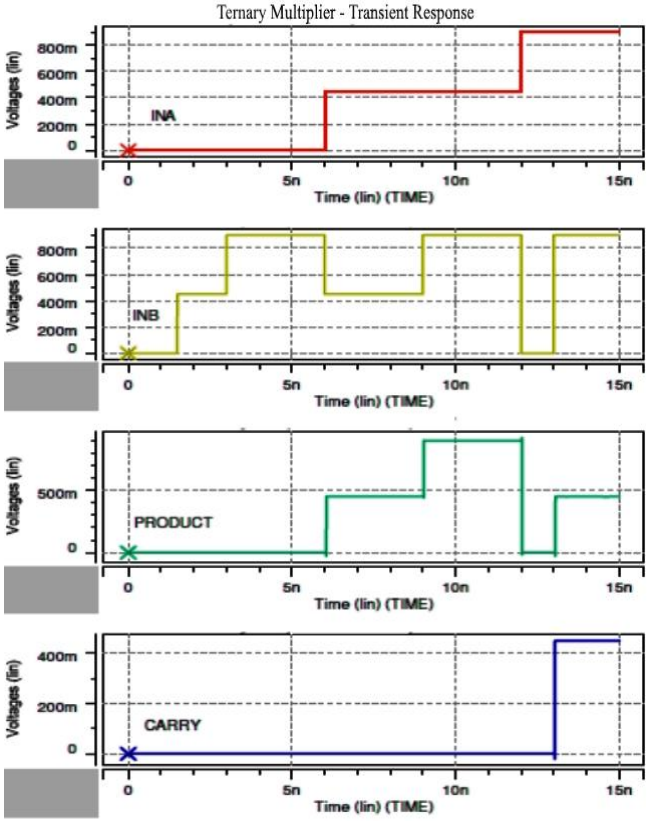


Fig. 5. Transient response of GNRFET based one-bit ternary multiplier

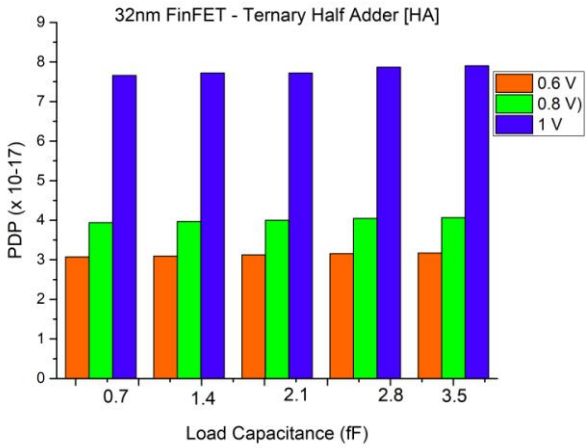


Fig. 6. Comparison Result of Power Delay Product (PDP) of Proposed 32nm FinFET based Ternary Half Adder

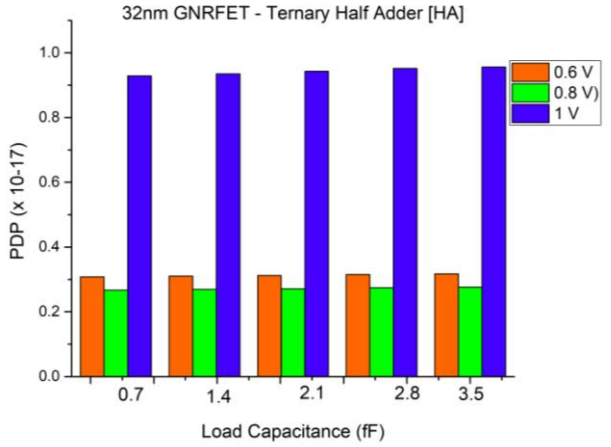


Fig. 7. Comparison Result of Power Delay Product (PDP) of Proposed 32nm GNRFET based Ternary Half Adder

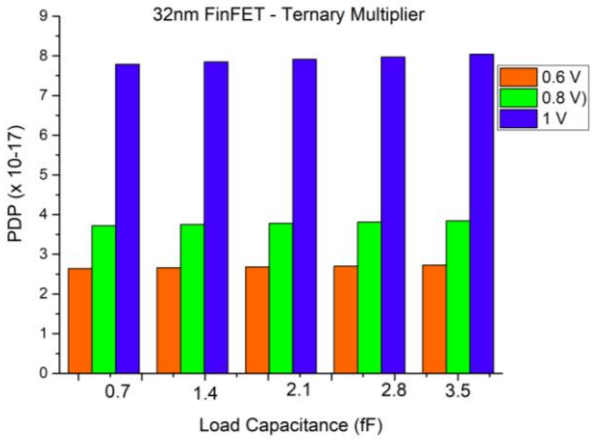


Fig. 8. Comparison Result of Power Delay Product (PDP) of Proposed FinFET based Ternary One-Bit Multiplier

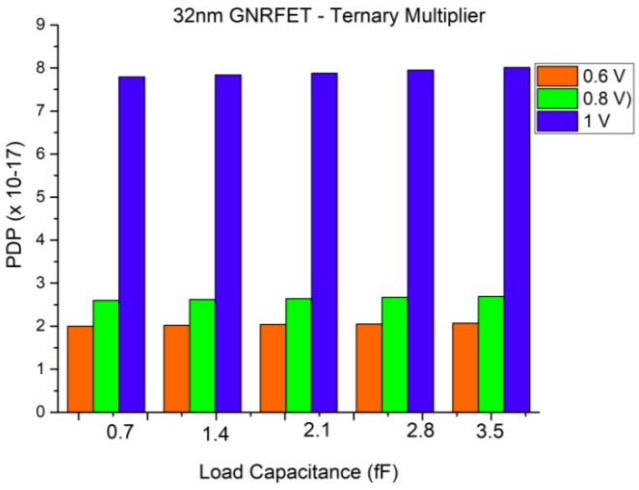


Fig. 9. Comparison Result of Power Delay Product (PDP) of Proposed GNRET based Ternary One-Bit Multiplier

TABLE VI. SIMULATION RESULTS OF THE TERNARY HALF ADDER & MULTIPLIER (@ 250MHZ OPERATING FREQUENCY)

Technology	Load Capacitor (fF)/	Delay (x 10-12 s)					Power (x 10-7 W)					PDP (x 10-17 J)				
		0.7	1.4	2.1	2.8	3.5	0.7	1.4	2.1	2.8	3.5	0.7	1.4	2.1	2.8	3.5

	VDD (V)															
Proposed Ternary Half Adder																
32nm FinFET	**0.6**	92.68	93.14	93.61	94.08	94.54	3.315	3.324	3.335	3.354	3.354	3.072	3.096	3.122	3.156	3.171
	0.8	60.71	61.01	61.32	61.62	61.93	6.488	6.507	6.526	6.566	6.566	3.939	3.97	4.002	4.046	4.066
	1	46.22	46.45	46.68	46.92	47.15	16.57	16.62	16.67	16.77	16.77	7.658	7.719	7.719	7.867	7.906
32nm GNRFET	**0.6**	77.03	77.45	77.88	78.31	78.74	0.399	0.399	0.4	0.402	0.402	0.308	0.31	0.312	0.315	0.317
	0.8	44.4	44.61	44.83	45.04	45.25	0.601	0.603	0.604	0.608	0.608	0.267	0.269	0.271	0.274	0.276
	1	58.7	58.98	59.26	59.54	59.82	1.581	1.585	1.59	1.598	1.598	0.929	0.935	0.943	0.952	0.956
Proposed Ternary Multiplier																
32nm FinFET	**0.6**	81.61	82.02	82.43	82.84	83.25	3.234	3.245	3.255	3.264	3.274	2.64	2.662	2.683	2.704	2.726
	0.8	56.5	56.78	57.07	57.35	57.63	6.585	6.604	6.624	6.644	6.664	3.72	3.75	3.78	3.81	3.841
	1	45.35	45.58	45.81	46.04	46.26	17.17	17.22	17.28	17.33	17.38	7.787	7.85	7.914	7.97	8.04
32nm GNRFET	**0.6**	68.87	69.25	69.62	70	70.38	2.9	2.91	2.92	2.92	2.93	2	2.02	2.04	2.05	2.07
	0.8	44.83	45.09	45.35	45.61	45.87	5.79	5.81	5.82	5.84	5.86	2.6	2.62	2.64	2.67	2.69
	1	47.61	47.82	48.03	48.23	48.44	1.635	1.639	1.64	1.647	1.652	7.79	7.84	7.88	7.95	8.01

V. CONCLUSION

This paper extensively studied the robustness and performance of ternary logic arithmetic circuits based on 32nm DG FinFET and 32-nm GNRFET devices. The performance characteristics of the ternary logic based arithmetic circuits are investigated by using HSPICE simulations. According to the simulation results, the worst-case delay parameter situation occurs when low power supply voltages as well as high load capacitors are used. On the other hand, circuits consume much more power when the values of both power supply voltage and load capacitors increase. The driving capability of circuits is evaluated more precisely by simultaneous variations of both load capacitors and power supply voltage. It can be inferred from the simulation results the proposed ternary arithmetic circuit works with high performance at low voltages even with large load capacitors. The proposed ternary arithmetic combinational circuit have the lowest Power-Delay-Product (PDP) design in various situations.Results for deep submicron technologies (32 nm) show that, they are suitable for the design with future multiple-valued processes also.

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