2D Lifting Based Discrete Wavelet Transform Architecture based on Sub Expression Reduction Technique

V.Anbumani
Department of ECE
Kongu Engineering College
Erode,India
anbumanivenkat@gmail.com

V Geetha
Department of ECE
Kongu Engineering College
Erode,India
geethavelliyangiri@gmail.com

G Murugesan
Department of ECE
Kongu Engineering College
Erode,India
gmece@gmail.com

***Abstract*— There are several methods to implement DWT. But lifting scheme is preferred because it reduces the computational complexity and is easy to implement. 9/7 filter coefficient are used in lifting scheme since they are originally implemented in JPEG codec 2000. Much architecture were developed using lifting scheme. But the number of computations is more leading to less efficient architecture. As an existing work, CSD algorithm based parallel flipped lifting 2D DWT using dual-scan technique (CSDPF) is designed with the modified flipping scheme using Canonical Signed Digit(CSD) algorithm.**

In order to reduce the computations Flipping Structure for a Lifting based Discrete Wavelet Transform using Sub Expression Sharing (SES) is developed for image compression. To improve the computational efficiency, area and power requirements sub expression sharing technique is used. In the case where several multipliers are present in a network of operators, the savings is achieved by identifying common subexpressions and sharing the two most common subexpressions that is expected to save the number of additions. It reduces the arithmetic resources like shifter and adder in its implementation. Using SES method the number of computations is reduced to half of the total computations. Hence a computationally efficient architecture with area and power reduction by 32% and 5% respectively is designed. The various applications include fax transmission, satellite remote sensing, high definition television, storage and transmission of CT and MRI scans etc.

Keywords—DWT, Flipping Structure, SES

I. INTRODUCTION

Image compression technique is necessary to reduce the size of the image file for an efficient storage and transmission of the data. It removes redundant or irrelevant information, and encodes what remains. Image compression is implemented to obtain shot to shot time latency, video-clip transmission, streaming-real time video conference etc., JPEG 2000, based upon Discrete Wavelet Transform (DWT) is the image compression standard employed in this technique since it is a single approach to lossy and lossless compression. It has superior compression performance, error resilience, multiple resolution representation, supports domain-specific metadata in file format. The DWT has better acceptance in signal processing and image compression. Because DWT produces a few significant coefficients for the signals with discontinuities. Thus, better results are obtained for DWT nonlinear approximation rather than other transformations.

In recent years, DWT has been extensively used in various application fields due to its proficiency of decomposing a signal at many resolution levels. By selecting proper shifting and scaling factors, DWT can do decomposition of a signal into components in dissimilar octaves or frequency ranges. The small scaling factor relates to fine details of the signal whereas the large scaling factor to coarse details. The shifting factor relates to the time or space localization of the signal. In Fourier transform and cosine transform the signals are characterized only in frequency domain. But in the case of DWT, signals are characterized by both frequency domain and time domain which offers proficient decomposition of the signal.

DWT is attractive for analysis and more suitable for non-stationary signals since in DWT, the signal which is transformed will not be unable to find the time information. Due to the availability of time domain information without any loss DWT has been taking on to be a component in several image compression standards, for instance JPEG2000. Hence DWT is composed of multirate filters and can achieve high compression ratio by the decomposition of the signals into sub-bands of time and frequency information. As exhaustive calculation is to be performed in several day to day practical applications efficient and cheap hardware is a must. In the up-to-date development, a lot of2-D DWT VLSI architectures for have been recommended to meet the requirements of real time processing. Initially the DWT designs are constructed on convolutions and the second-generation DWTs are built on lifting algorithms.

There are quite a lot of research works in the area of 2D DWT VLSI designs [1]-[15]. Anand Darji et al. [1] have proposed folded dual-scan parallel flipping architecture for a lifting-based 2-D Discrete Wavelet Transform to reduce the data path to only six multipliers and eight adders and as well keeping the same critical path.C.T.Haung et al. [4] have proposed flipping structure with memory efficient lifting-based DWT VLSI architecture to minimize the critical path.Y K Lai et al. [7] have proposed a 2-D DWT VLSI architecture with better enactment in speed and memory utilization with parallel scanning method. W. Zhang et al. [15] have proposed a high speed lifting scheme based DWT architecture. In this, single lifting step can perform computation using three pipelining stages, smaller number registers and Tm critical path delay.

In this paper, multipliers are substituted with optimized shift-and-add operation in 2D lifting. The rest of the paper is ordered as follows. In Section II, CSD algorithm based parallel flipped lifting 2D DWT using dual-scan technique is explained. The proposed 2D-DWT architecture using SES technique is explained in Section III. In Section IV, simulation results and performance comparison of CSD and SES based 2D DWT architectures are included. Finally, a brief conclusion and future scope is given in Section V.

II. CSD ALGORITHM BASED PARALLEL FLIPPED LIFTING 2D DWT USING DUAL-SCAN TECHNIQUE(CSDPF)

Unlike the conventional algorithm, in CSDPF, the computation of the intermediate data is performed on different paths and the calculation is in parallel manner in the present computation and applied in the subsequent operation [1].The mathematical formulation for the CSDPF is depicted in (1)-(4). For accessing inputs in Z-scan approach the odd and even inputs are retrieved. Basic lifting equations can be rearranged as the following equations (1) to (4).

$$\frac{d_i^1}{\alpha} = \frac{d_i^0}{\alpha} + (s_i^0 + s_{i+1}^0) \quad (1)$$

$$\frac{s_i^1}{\alpha\beta} = \frac{s_i^0}{\alpha\beta} + (\frac{d_{i-1}^1}{\alpha} + \frac{d_i^1}{\alpha}) \quad (2)$$

$$\frac{d_i^2}{\alpha\beta\gamma} = \frac{d_i^1}{\alpha\beta\gamma} + (\frac{s_i^1}{\alpha\beta} + \frac{s_{i+1}^1}{\alpha\beta}) \quad (3)$$

$$\frac{s_i^2}{\alpha\beta\gamma\delta} = \frac{s_i^1}{\alpha\beta\gamma\delta} + (\frac{d_{i-2}^2}{\alpha\beta\gamma} + \frac{d_i^2}{\alpha\beta\gamma}) \quad (4)$$

For example, in the operation in equation (1), during the computation cycle of $\frac{d_i^1}{\alpha}$, $\frac{d_i^0}{\alpha}$ is computed at the same time with the addition procedure between s0i and s0 i+1. Similarly equation (2) is computed. Since outputs $\frac{d_i^1}{\alpha}$ and $\frac{s_i^1}{\alpha\beta}$ considered from the first lifting operation are applied in the second lifting step, during the second lifting step in equations (3) and (4), as a replacement for the actual scaling parameters $1/\alpha\beta\gamma$ and $1/\alpha\beta\gamma\delta$,signals d_i^1 and s_i^1 are scaled by $1/\beta\gamma$ and $1/\gamma\delta$. Thus, the critical path2Tm is minimized to Tm. As given by the equations (5) and (6) the overall outputs are scaled down as follows:

$$d_i = \frac{d_i^2 \alpha\beta\gamma}{k} \quad (5)$$

$$s_i = s_i^2 * k\alpha\beta\gamma\delta \quad (6)$$

To create DWT architecture with minimum area and power consumption, the constant coefficients can be prearranged via Canonic Signed Digit (CSD) illustration with smallest number of non-zero bits. The CSD representation of a number comprises the least possible number of non-zero bits, thus the tag canonic. In CSD methodology, no two succeeding bits in a CSD number are non-zero. CSD quantities cover the range (- 4/3, 4/3), out of which the standard range [-1, 1] are the chief concern. Amongst the W-bit CSD statistics in the range [-1, 1], the typical number of non-zero bits is W/3 + 1/9 + O$\left(2^{-W}\right)$. Hence, typically CSD numbers encloses approximately 33% less substantial quantity of non-zero bits than two's complement statistics. The CSDPF architecture is designed with CSD and is compared with Sub Expression Sharing technique.

A. CSD Multiplication

In constant multiplier, the multiplication function can be approved by either addition or subtraction process of partial product expressions analogous to the non-zero bit positions. A CSD-encoded multiplier comprises the least amount of non-zero bits and, henceforth, entails the minimum number of addition or subtraction tasks. In CSD encoding, initially two's complement is taken for the constant coefficients, then signed bit is introduced if there is a presence of consecutive non-zero bits. Here, the first bit is made as the signed bit and the consecutive non-zero bits are made zero till the next zero bit arrives from right to left. Then the immediate zero bit after the consecutive non-zero bits, is made as a non-zero bit. Hence, it reduces the amount of multipliers by decreasing the number of non-zero bits.

CSD based four stages of multiplication alpha, beta, gamma and delta is modeled. Design of CSD based Alpha stage is described as follows:

B. Alpha Stage

The value of α co-efficient is,

$$\alpha = -1.5861$$

Its flipping value is,

$$\frac{1}{\alpha} = -0.63$$

Its binary representation is,

Binary = 0000.101000010100

Its 2's complement value is,

2's complement = 1111.010111101100

Its Canonical Signed Digit representation is,

CSD code = $0000.\bar{1}0\bar{1}000\bar{1}0\bar{1}00$

Hence 22 shifts are required for the computation of alpha stage.

Representation of CSD for α co-efficient in equation form is given below in (7)

$$2^{-1}x - 2^{-3}x - 2^{-8}x - 2^{-10}x \quad (7)$$

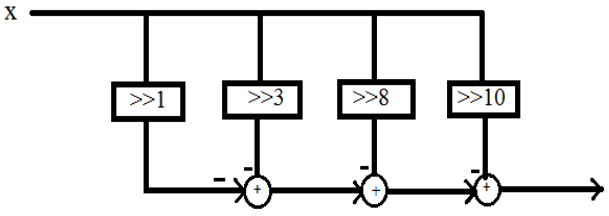

Fig. 1.Block Diagram of Alpha Stage Using CSD

The above Fig 1 illustrates the alpha stage of the CSD representation. Similar procedure is followed for the design and verification of the remaining three stages of multiplication namely beta, gamma and delta.

III. 2D DWT ARCHITECTURE USING SUB EXPRESSION SHARING(SES)TECHNIQUE

In this proposed method, to diminish the total utilized quantity of arithmetic resources like multipliers and adders, Sub Expression Sharing (SES) technique is introduced. First of all, to implement the SES method, the constant coefficients are converted into canonical signed digit (CSD). The CSD representation itself reduces few bits, resulting to the decline of the quantity of multipliers. But to reduce their number further, SES technique is adopted. And then the arithmetic resources, area and power of the existing architecture and the proposed method is compared and the results are verified. Hence, an efficient architecture is designed with very few computations.

A. Sub Expression Sharing Technique

Generally, the possibility for subexpression sharing in a single multiplier is inadequate. Conversely in the instance of digital filters everywhere several multipliers are required to do multiplication operation of the related values. Hence there is more chances to be protracted from sharing subexpressions. Identification of common subexpressions can contribute essential hardware declines.

Example of common sub expression sharing

$$y = 0.10\bar{1}00010\bar{1} * x$$

This may be implemented as given in equation (8)

$$y = (x >> 1) - (x >> 3) + (x >> 7) - (x >> 9) \quad (8)$$

Alternatively, this multiplication can be implemented as

$$x2 = x - x >> 2$$

$$y = (x2 >> 1) + (x >> 7) \quad (9)$$

Equation (9) shows the reduction in addition operation. So the quantity of adders that will be eradicated by a common subexpression taking place N-times is N - 1. The only pretend in creating the precise count is to pay attention that overlapping subexpressions are not calculated double the times. Hence, the system of subexpression sharing has the prospective of realizing significant savings in the quantities of additions used. As said before,SES can lessen the quantity of adders by approximately 50%.SES based four stages of multiplication alpha, beta, gamma and delta is modeled. Design of SES based Alpha stage is described as follows:

B. Alpha Stage

The value of α co-efficient is,

$$\alpha = -1.5861$$

Its flipping value is,

$$\frac{1}{\alpha} = -0.63$$

Its binary representation is,

Binary = 0000.101000010100

Its 2's complement value is,

2's complement = 1111.010111101100

Its Canonical Signed Digit representation is,

CSD code = $0000.\bar{1}01000\bar{1}0\bar{1}00$

Representation of SES for α co-efficient in equation form is given below in (10)

$$= -2^{-1}x - 2^{-3}x - 2^{-8}x - 2^{-10}x$$

$$= -2^{-1}\left(x + 2^{-2}x\right) - 2^{-8}\left(x + 2^{-2}x\right)$$

$$= -2^{-1}\left(\left(x + 2^{-2}x\right) + 2^{-7}\left(x + 2^{-2}x\right)\right) \quad (10)$$

Hence 22 shifts are required in CSD method of implementation and 10 shifts are required in SES method of implementation. The block diagram of the Alpha stage using SES representation is given in Fig 2.

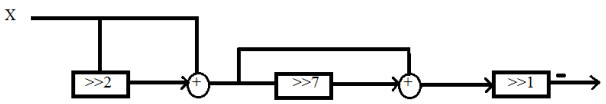

Fig. 2.Block Diagram of Alpha stage using SES

C. Beta Stage

The value of α and β co-efficient are,

α= -1.5861and β = -0.0529

Its flipping value is,

$$\frac{1}{\alpha\beta} = 12$$

Its binary representation is,

Binary = 1100.000000000000

Its Canonical Signed Digit representation is,

CSD code = $10\bar{1}00.000000000000$

Representation of SES for β co-efficient in equation form is given below in (11)

$$= 2^4 x - 2^2 x$$

$$= 2^2\left(2^2 x - x\right) \quad (11)$$

Hence 6 shifts are required in CSD method of implementation and 4 shifts are required in SES method of implementation. The block diagram of the Beta stage using SES representation is given in Fig 3.

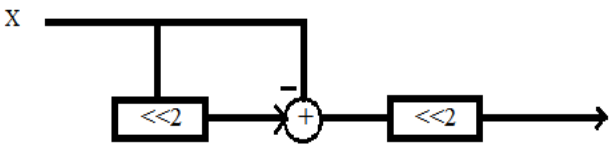

Fig . 3. Block Diagram of Betastage using SES

D. Gamma Stage

The value of β and γ co-efficient are,

B = -0.0529 and γ = 0.8829

Its flipping value is,

$$\frac{1}{\beta\gamma} = -21.41$$

Its binary representation is,

Binary = 10101.011010001111

Its 2's complement value is,

2's complement = 1010.100101110001

Its Canonical Signed Digit representation is,

CSD code = $1010.101010\bar{0}010\bar{0}0001$

Representation of SES for γco-efficient in equation form is given below in (12)

$$= 2^3x + 2^1x + 2^{-1}x + 2^{-3}x - 2^{-5}x - 2^{-8}x + 2^{-12}x$$

$$= 2^3x + 2^1x + 2^{-1}x + 2^{-3}x - 2^{-5}\left(x + 2^{-3}x - 2^{-7}x\right)$$

$$= 2^3x + 2^1x + 2^{-1}x + 2^{-3}\left(x - 2^{-2}\left(x + 2^{-3}\left(x - 2^{-4}x\right)\right)\right)$$

$$= 2^3x + 2^1x + 2^{-1}\left(x + 2^{-2}\left(x - 2^{-2}\left(x + 2^{-3}\left(x - 2^{-4}x\right)\right)\right)\right)$$

$$= 2^1\left(x + 2^2x\right) + 2^{-1}\left(x + 2^{-2}\left(x - 2^{-2}\left(x + 2^{-3}\left(x - 2^{-4}x\right)\right)\right)\right) \quad (12)$$

Hence 33 shifts are required in CSD method of implementation and 15 shifts are required in SES method of implementation. The block diagram of the Gamma stage using SES representation is given in Fig 4.

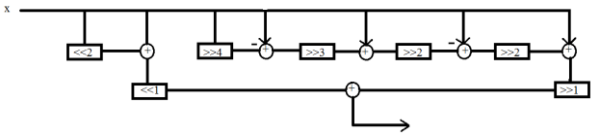

Fig. 4. Block Diagram of Gamma stage using SES

E. Delta Stage

The value of γ andδ co-efficient are,

γ = 0.8829 and δ = 0.4435

Its flipping value is,

$$\frac{1}{\gamma\delta} = 2.55$$

Its binary representation is,

Binary = 0010.100011001100

Its Canonical Signed Digit representation is,

CSD code = $0010.100\bar{1}010\bar{1}00$

Representation of SES for δco-efficient in equation form is given below in (13)

$$= 2^1x + 2^{-1}x + 2^{-4}x - 2^{-6}x + 2^{-8}x - 2^{-10}x$$

$$= 2^1x + 2^{-1}x + 2^{-4}\left(x - 2^{-2}x\right) + 2^{-8}\left(x - 2^{-2}x\right)$$

$$= 2^1x + 2^{-1}x + 2^{-4}\left(\left(x - 2^{-2}x\right) + 2^{-4}\left(x - 2^{-2}x\right)\right)$$

$$= 2^1x + 2^{-1}\left(x + 2^{-3}\left(\left(x - 2^{-2}x\right) + 2^{-4}\left(x - 2^{-2}x\right)\right)\right) \quad (13)$$

Hence 30 shifts are required in CSD method of implementation and 11 shifts are required in SES method of implementation. The block diagram of the Delta stage usingSES representation is given in Fig 5.

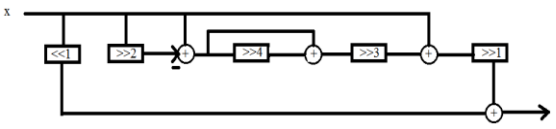

Fig. 5.Block Diagram of Delta stage using SES

IV. RESULT AND DISCUSSION

The Canonical Signed Digit (CSD) based design and Sub Expression Sharing Technique based design are described in Verilog language and synthesized in Synopsys tool. By using Synopsys 90nm technology, the enactments in terms of lessening of area and power consumption are examined.

The Table I shows the comparison of adder and shifter requirement for the 2D DWT architectures based on the CSD algorithm and SES technique. Comparison shows that for the four stages of multiplication namely alpha, beta, gamma and delta, there are reductions of 65 shifters and 2 adders in the SES technique when compared with the CSD algorithm.

Table I. Hardware Requirement for the 2D DWT Architectures Based on the CSD Algorithm and SES Technique

Name of the stage	CSD		SES	
	Adder	**Shifter**	**Adder**	**Shifter**
Alpha	3	22	2	10
Beta	1	6	1	4
Gamma	6	33	6	15
Delta	5	30	4	11

The Table II shows the comparison of Power and Area comparison between the CSD and SES based 2D DWT architectures.

Table II.Power and Area Comparison between the CSD and SES Based 2D DWT Architectures

Name of the architecture	**Power(μW)**	**Area(μm^2)**
CSD	19.45	79848.44
SES	18.62	53599.61

Hence Power and Area is reduced by about 5% and 32% respectively in SES technique based 2D DWT architecture when compared with CSD algorithm based 2D DWT architecture.

V. CONCLUSION AND FUTURE SCOPE

The Discrete Wavelet Transform provides a multi-resolution of images. The 2-D DWT has been designed for less computational flipping architecture using Sub Expression Sharing algorithm. The code for these structures was written in Verilog and synthesized using Synopsys tool and the performance results were obtained. In 2-D DWT using SES, the quantity of calculations is reduced to half of the entire computations in the CSD based flipping2D DWT architecture. The area and power is diminished by 32% and 5% respectively. It is concluded that the architecture designed with SES technique is computationally efficient and has a lower memory storage requirement. The future scope is to model 3-D DWT structure using the SES technique and implement.

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