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Design of Novel SRAM cell using Hybrid VLSI Techniques for Low Power and High Speed in Embedded Memories

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***Abstract*— Static or leakage power is the dominating component of total power dissipation in deep nanometer technologies below 90nm, which has resulted in increase from 18% at 130nm to 54% at 65nm technology due to continued device and voltage scaling. Static Random-Access memory (SRAM) is a type of RAM in which data is not written permanently and it does not need to be refreshed periodically. Different techniques have been applied to SRAM cell to reduce leakage power without affecting its performance. A novel 10T SRAM architecture is proposed in this paper which operates in three modes (active, park, standby or hold). The main objective of the proposed architecture is to provide better stability and reduced delay in active mode, reduced leakage current in standby mode and retaining the logic state in park mode. Design metrics such as static and dynamic power, delay, power delay product, energy, energy delay product, rise and fall time, slew rate and static noise margin are taken into account. All the circuits were designed using SYNOPSYS EDA tool and simulated in 30nm technology. Simulation results shows that the proposed SRAM is much better than conventional and other SRAM cells designed using hybrid techniques.**

Keywords*— *CMOS, SRAM cell, Low power, High Speed, Subthreshold current

I. INTRODUCTION

The increasing demand of battery-operated high speed portable digital system and implantable devices causes increase in need of supply voltage scaling and device scaling [2]. Supply voltage scaling causes the difference between supply voltage and transistor threshold voltage to be a very low value in modern SoC design [1]. This makes stability to reach a problematic zone and making it to be considered as an important factor during designing. Device scaling causes reduction in channel length, oxide thickness and threshold voltage (Vt) which leads to increase in drain induced barrier lowering (DIBL), Gate induced drain leakage (GIDL), and subthreshold current. When a CMOS circuit is in idle state there is still some leakage or static power dissipation due to the leakage current flowing through nominally OFF transistors [23]. CMOS logic gates have both NMOS and PMOS transistors, both of which dissipate finite reverse leakage and sub threshold currents [26]. There are millions of transistors in a silicon chip and overall power dissipation due to leakage current is comparable to dynamic power dissipation. The main leakage current component in NMOS is the reverse-biased diode [21]. With increase in temperature, leakage current increases. In a chip, millions of transistors are fabricated and every transistor in the chip, constitutes the leakage current. In this case, the sum of all leakage currents then becomes significant. So, it is necessary to reduce leakage power dissipation in VLSI circuits [7].

The static power dissipation of CMOS circuits primarily depends on key parameters such as input vectors, device characteristics (threshold voltage, gate oxide thickness, channel length) and operating conditions (VDD and temperature) [14]. Here assumption is that the gate leakage current which is determined by the operational state of the transistors, does not vary with parameters other than input signal values. As leakage power is consumed in OFF state the effect of making input pattern that maximizes the number of "OFF" transistors in PMOS and NMOS stacks would reduce the gate leakage by a significant amount [18 and 25].

As device and voltage scaling does not provide good results in achieving low power, circuit and system level techniques are needed [8-10]. Portable devices require primary memory that respond faster. SRAM is mainly used in this case, though expensive it is faster and does not to refreshed periodically. The dominant leakage in SRAM cell are subthreshold current and gate leakage [19].

In this paper the proposed SRAM cell operates with less delay and high stability in active mode and with reduced leakage current in standby mode. The rest of paper is organized as follows. Section 2 presents the design of SRAM cell using conventional techniques. Section 3 presents design of SRAM cell using hybrid techniques. Section 4 presents design of proposed SRAM cell. Section 5 presents simulation results and graphical analysis. Section 6 concludes the paper.

II. DESIGN OF SRAM CELL USING CONVENTIONAL TECHNIQUES

In this section, we review some SRAM cell designed using conventional techniques to reduce static or leakage power.

A. 6T SRAM Cell

The schematic diagram of conventional 6TSRAM cell is shown in Fig.1. The 6T SRAM cell consist of six transistors,

two pull up transistor (P0,P1), two pull down transistor (N0,N1) and two pass transistor (N2,N3).The gate of pass transistors is controlled by the word line inputs (wl). Whenever the word line is made high, the bl and blb are connected to the cell hence the cell can be read out or write in from the bit lines. The power measured in this state due to switching activity of the output is called dynamic power dissipation. When the word line is made low, there is no reading or writing operation performed by the cell, hence the cell will be in the hold state. The power measured in this state is called static or leakage power dissipation. For successful writing to be done in the cell there must be a write driver which monitor the presence of data and allows the data to be written into the cell [3]. This write driver is simple a AND gate whose inputs are write enable and data.

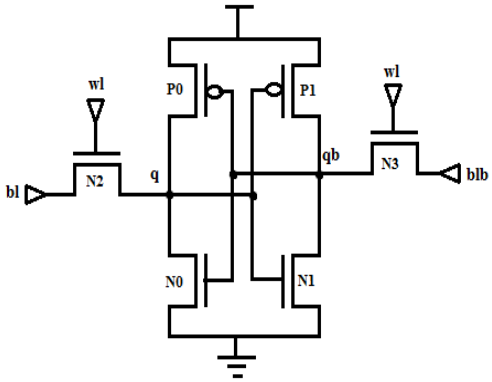

Fig. 1. Schematic diagram of 6T SRAM cell

When reading is to be done the write enable of the write driver is switched off. It is very important that before reading is to begin the bl and blb are to be precharged to the certain level of voltage so that both the bitlines would have same voltage. This precharge is done by the precharge circuit [4]. After precharging, depending on the value stored at the output (q,qb) of the SRAM cell, the capacitor at one end discharges due to voltage difference between nodes of access transistor. Sense amplifier is a differential amplifier which senses the difference between the voltages in bl and blb and amplifies it. During reading bl and blb acts as output lines.

B. SRAM Cell using GALEOR Technique

GALEOR technique uses two extra transistors inserted in series between pull up network and pull-down network in a way that extra NMOS transistor is inserted between pull up network and the output terminal, extra PMOS transistor is inserted between pull down network and output terminal [17]. The extra transistors are connected in such a manner that transistors are always near the cutoff region. This causes increase in path resistance (according to Ohms law) from supply to ground, leading to significant reduction in power. However, GALEOR faces signal quality problems because one of the extra inserted transistors is always near the cutoff voltage. GALEOR falls under the self-controlled leakage technique because added extra transistors are biased internally. The schematic diagram of SRAM cell using GALEOR technique is shown in Fig.2.

The transistors (N4,N5,P2,P3) are connected in such a manner that transistors are always near the cutoff region. In active mode, word line "wlg" is made high, allowing SRAM cell to perform write and read operation and power measured in this mode is dynamic power. In standby mode, word line "wlg" is made low, no read or write operation can be performed in the cell. The increase in resistance (due to more OFF transistors) causes reduction in the leakage current in this state. The power measured in this mode is static power. The inputs are "blg" and "blbg" and outputs are "qg" and "qbg".

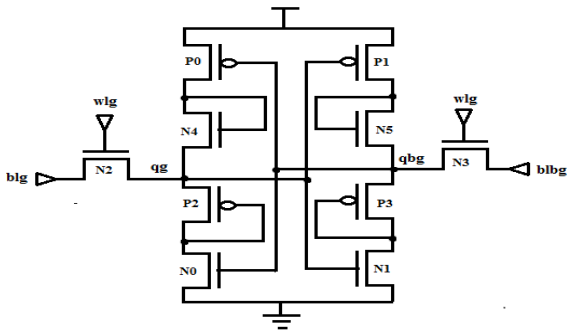

Fig. 2. Schematic diagram of SRAM cell using GALEOR technique

C. SRAM Cell using LECTOR Technique

LECTOR technique uses two additional extra transistors that are inserted in series between pull up network and pull-down network in a way that extra PMOS transistor is inserted between pull up network and the output terminal, extra NMOS transistor is inserted between pull down network and output terminal [17]. The extra transistors (one PMOS and one NMOS transistor) are connected in such a manner that transistors are always near the cutoff region. This causes increase in path resistance from supply to ground, leading to significant leakage reduction. However, LECTOR faces signal quality problems due to lack of good rise and fall time values. LECTOR falls under the self-controlled leakage technique because extra transistors are internally biased, not externally. The schematic diagram of SRAM cell using LECTOR technique is shown in Fig.3.

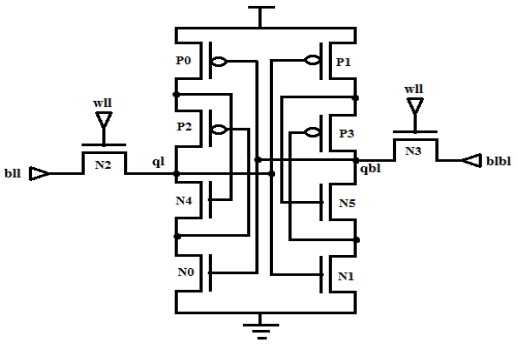

Fig. 3. Schematic diagram of SRAM cell using LECTOR technique

The extra transistors (P2,P3,N4,N5) are connected in such a manner that they are always near the cutoff region. In active mode, the word line "wll" is made high allowing SRAM cell to perform write and read operation, the power measured in this mode is dynamic power. In standby mode, word line "wll" is made low, all transistors are in OFF state providing more resistance thereby reducing the leakage current. The power measured in this mode is static power.

The inputs are "bll" and "blbl" and outputs are "ql" and "qbl".

D. SRAM Cell using MTCMOS Technique

Multi-threshold CMOS (MTCMOS) technique uses two high Vt sleep transistors, in which one PMOS high Vt transistor is inserted in series between supply voltage and pull up network and other NMOS high Vt transistor is inserted in series between pull down network and ground terminal. The remaining circuit is designed using standard Vt transistors. The circuit operates in two modes. In active mode, the two high Vt sleep transistors are turned ON so supply voltage and ground terminal is connected to the circuit to perform its operations. In standby mode, the two high Vt sleep transistors are turned OFF thereby cutting OFF the power supply from supply voltage (Vdd) to ground thereby reducing leakage power dissipation. The drawback of this technique is the circuit will lose data [6] when sleep transistors are in OFF state. The schematic diagram of SRAM cell using MTCMOS technique is shown in Fig.4.

The sleep transistors (P2,N4) are controlled by the inputs "sm" and "sbm". In active mode, word line ("wlm") and "sbm" is made high, "sm" is made low. The sleep transistors (P2,N4) conduct allowing SRAM cell to perform write and read operation as power supply voltage and ground terminal is connected to SRAM cell. The power measured in this mode is dynamic power. In standby mode, word line ("wlm") and "sbm" is made low, "sm" is made high making the sleep transistors (P2,N4) OFF, thereby cutting of the power supply from Vdd to ground reducing the leakage power. The cell in this case is in hold state and power measured in this state is static power. The inputs are "blm" and "blbm" and outputs are "qm" and "qbm".

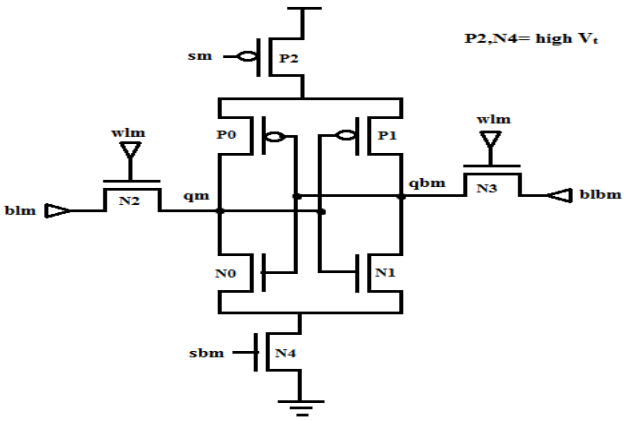

Fig. 4. Schematic diagram of SRAM cell using MTCMOS technique

E. SRAM Cell using Drain Gating Technique

Drain gating uses two sleep transistors connected between pull up and pull-down network in a way PMOS sleep transistor is connected between pull up network and the output, NMOS sleep transistor is connected between pull down network and the output, both of which are controlled externally [20]. The circuit operates in two modes. In active mode, the sleep transistors are ON so circuit operates as per its logic. In standby mode [6] this technique reduces leakage current by turning OFF sleep transistors and causing stack effect. The schematic diagram of SRAM cell using drain gating technique is shown in Fig.5.

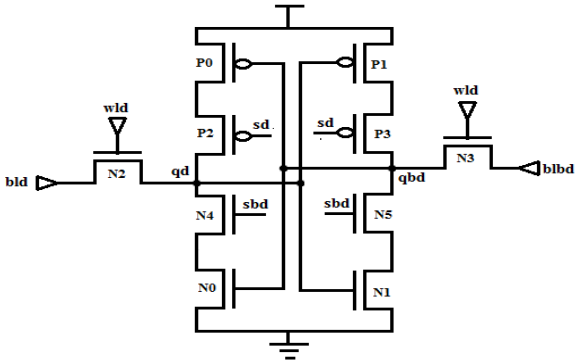

Fig. 5. Schematic diagram of SRAM cell using drain gating technique

The sleep transistors (P2,P3) are controlled by the input "sd" and (N4,N5) are controlled by the input "sbd". In active mode, word line ("wld") and "sbd" is made high, "sd" is made low, the sleep transistors (P2,P3,N4,N5) conduct allowing SRAM cell to perform write and read operation and power measured in this mode is dynamic power. In standby mode [6], word line ("wld") and "sbd" is made low, "sd" is made high, the sleep transistors (P2,P3,N4,N5) are in OFF state. This causes stack effect in the circuit that is source voltage of the upper transistor will be a little higher than the source voltage of the lower transistors in the stack. Hence Vgs and Vbs of the upper transistor is negative resulting in increase in threshold voltage thereby reducing the leakage current. The cell in this case is in hold state and power measured in this state is static power. The inputs are "bld" and "blbd" and outputs are "qd" and "qbd".

F. SRAM Cell using Sleepy Keeper Approach

This approach uses two sleep transistors and two helper transistors (one PMOS and one NMOS) in both cases. The helper transistors is connected in parallel with sleep transistors. The sleep transistors are controlled externally by control signals and helper transistors are driven by output directly [15]. The circuit operates in two modes. In active mode sleep transistors are turned ON providing supply voltage and ground terminal to the circuit to perform its operation. In standby mode sleep transistors are turned OFF thereby cutting OFF the power supply from supply voltage (Vdd) to ground thereby reducing the leakage power dissipation. The schematic diagram of SRAM cell using sleepy keeper approach is shown in Fig.6.

The sleep transistors (P2,N5) are controlled by the inputs "sk" and "sbk". In active mode, word line ("wlk") and "sbk" is made high, "sk" is made low, the sleep transistors (N5,P2) conducts allowing SRAM cell to perform write and read operation by connecting power supply and ground terminal to it. The power measured in this mode is dynamic power. In standby mode, word line ("wlk") and "sbk" is made low, "sk" is made high, the sleep transistors (N5,P2) are turned OFF and hence reduces the leakage current by cutting off the power supply from supply voltage (Vdd) to ground thereby reducing the leakage power dissipation. In this mode one of the helper transistor (N4 or P3) keeps connection with appropriate power rail, thus retaining the previous logic state. The cell in the above case is in hold state and power measured in this state is static power. The inputs are "blk" and "blbk" and outputs are "qk" and "qbk".

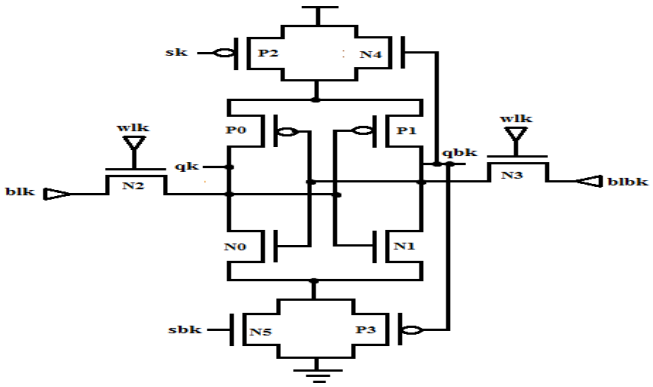

Fig. 6. Schematic diagram of SRAM cell using Sleepy Keeper Approach

G. SRAM Cell using LCNT Technique

Leakage control NMOS transistor (LCNT) approach uses two extra NMOS transistors named LCT transistors connected between pull down network and output terminal. The gate terminal of the extra LCT transistors are connected to the output [17]. When LCT transistors are ON they provide good conducting path. When LCT transistors are OFF, they provide high resistance hence reduces the leakage current that flows in the circuit. The schematic diagram of SRAM cell using LCNT technique is shown in Fig.7.

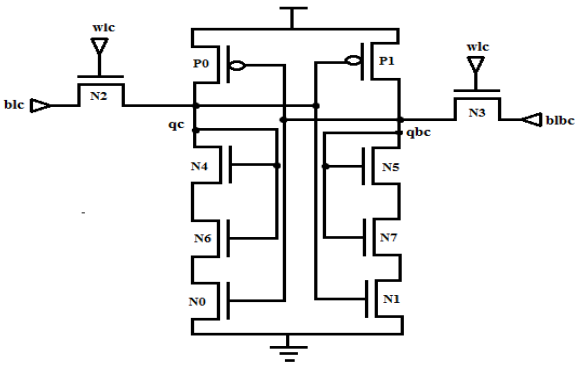

Fig. 7. Schematic diagram of SRAM cell using LCNT technique

The SRAM cell operates in two modes. In active mode, the word line "wlc" is made high, allowing SRAM cell to perform write and read operation and power measured in this case is dynamic power. In standby mode, the word line "wlc" is made low, the SRAM cell is in hold state so all transistors including LCT transistors are OFF, providing high resistance path from pull up network to pull down network thereby reducing the leakage current and thus reducing the leakage power. The power measured in this state is static power. The inputs are "blc" and "blbc" and outputs are "qc" and "qbc".

H. SRAM Cell using DTMOS Technique

A dynamic threshold MOS (DTMOS) technique allows body and gate terminals tied together so body voltage varies with the gate voltage. The main advantage of DTMOS is that it can dynamically tune the threshold voltage of the transistors [20]. In active mode high ON current is provided by lowering the threshold voltage caused by forward biasing the transistor. In standby mode low OFF current is provided by making the threshold voltage higher caused by reverse biasing the transistor. The schematic diagram of SRAM cell using DTMOS technique is shown in Fig.8.

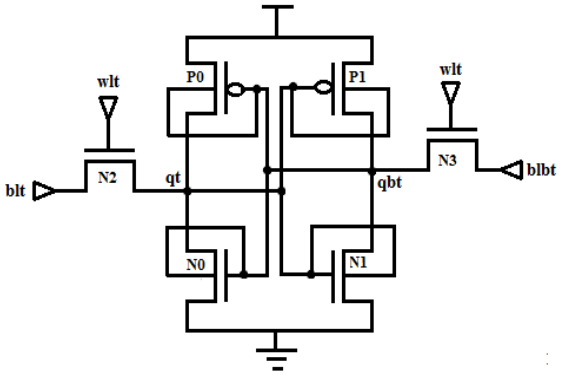

Fig. 8. Schematic diagram of SRAM cell using DTMOS technique

In active mode, the word line "wlt" is made high, inputs are provided causing decrease in depletion width thereby providing high ON current by reducing the threshold voltage necessary to form inversion layer in the transistor. The power measured in this mode is dynamic power. In standby mode, the word line "wlt" is made low, inputs are not provided to the transistors making it reverse biased causing increase in depletion width which in turn increases the threshold voltage necessary to form the inversion layer thereby providing low OFF current (leakage current). The cell in the above case is in hold state and power measured in this state is static power. The inputs are "blt" and "blbt" and outputs are "qt" and "qbt".

I. SRAM Cell using Trimode MTCMOS Ground Gated Technique

Trimode MTCMOS as name specifies performs operation in three modes, standby or hold mode, park mode and active mode. Trimode MTCMOS ground gated uses two extra high Vt sleep transistors one PMOS (parker), one NMOS (footer) both of which are connected in parallel between pull down network and ground terminal which are controlled externally [12]. The remaining circuit is implemented using low Vt transistors. In standby mode the sleep transistors are cut off to place the circuit with low-leakage. In park mode, parker transistor is activated and virtual ground line voltage will be the threshold voltage of parker transistor. In active mode footer is turned on to discharge the virtual ground line to zero voltage. The schematic diagram of SRAM cell using TRIMODE MTCMOS ground gated technique is shown in Fig.9.

The sleep transistors are controlled by the input's "stg" and "stg1". In standby mode word line ("wltg") and "stg" is made low, "stg1" is made high. The footer (N4) and parker (P2) transistors are in OFF state, cutting off the ground terminal to the SRAM cell. The cell in this mode is in hold state and power measured in this state is static power. In park mode word line "wltg" is made high, "stg1" and "stg" is made low. The footer (N4) is in OFF state and parker (P2) transistor is in ON state, the virtual ground line voltage is equal to the threshold voltage of parker transistor (Vss+ Vt) allowing SRAM cell to perform its operations. In active mode, word line ("wltg"), "stg" and "stg1" is made high so footer transistor (N4) conduct. In this mode the virtual ground line is discharged to zero volts and full supply voltage is provided, allowing SRAM cell to perform write and read operation efficiently than in park mode. The power

measured in this mode is dynamic power. The inputs were "bltg" and "blbtg" and outputs were "qtg" and "qbtg".

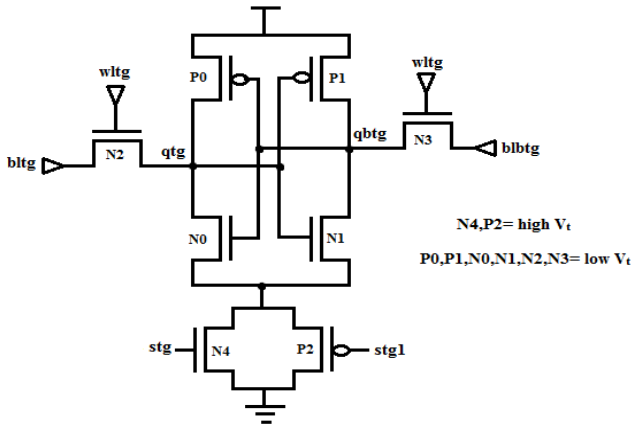

Fig. 9. Schematic diagram of SRAM cell using TRIMODE MTCMOS ground gated technique

J. SRAM Cell using VCLEARIT Technique

VLSI CMOS Leakage reduction technique (VCLEARIT) uses three extra transistors (two PMOS and one NMOS) which are controlled externally. In two PMOS one is connected in parallel to pull up network, other in series between pull up and pull down network and NMOS is connected in parallel to pull down network [16]. The technique operates in two modes, in active mode the transistor (PMOS) connected between pull up and pull down network is turned ON and transistors (PMOS and NMOS) connected in parallel to pull up and pull down network are turned OFF so actual operation is performed by the circuit. In standby mode PMOS transistor connected between pull up and pull down network is turned OFF and transistors (PMOS and NMOS) connected in parallel to pull up and pull down network are turned ON so pull up and pull down network have same potential in both terminals, reducing leakage current. The schematic diagram of SRAM cell using VCLEARIT technique is shown in Fig.10.

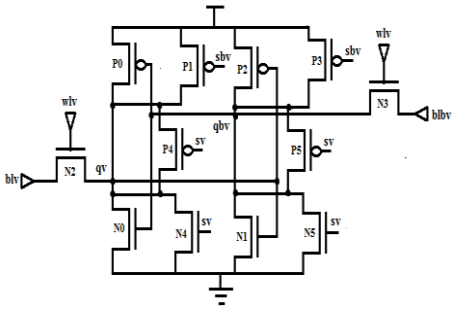

Fig. 10. Schematic diagram of SRAM using VCLEARIT technique

The sleep transistors are controlled by the inputs "sv", "sbv". In active mode the word line "wlv" and "sbv" is made high, "sv" is made low. This condition causes the transistors (P1,P3,N4,N5) to be OFF and transistors (P4,P5) to be ON thereby allowing SRAM cell to perform read and write operations. The power measured in this mode is dynamic power. In standby mode "wlv" and "sbv" is made low, "sv" is made high. This condition causes the transistors (P1,P3,N4,N5) to be ON and transistors (P4,P5) to be OFF. In this case the pull up network is connected between two points having potential Vdd and pull down network is connected between two terminal having same ground potential thereby reducing leakage current flowing in the circuit. The power measured in this state is static power. The cell in this case is in hold state and power measured in this case is static power. The inputs were "blv" and "blbv" and outputs were "qv" and "qbv".

K. SRAM Cell using Trimode MTCMOS Power Gated Technique

Trimode MTCMOS as name indicates performs operation in three modes, standby or hold mode, park mode and active mode. Trimode MTCMOS power gated uses two extra high Vt sleep transistors one PMOS (header), one NMOS (parker) connected in parallel between pull up network and supply voltage and controlled externally [12]. The remaining circuit is implemented using low Vt transistors. In standby mode the sleep transistors are cut off to place the circuit with low-leakage. The virtual power line is maintained at zero potential. In park mode, park transistor is activated and virtual power line is charged to voltage Vdd- Vt where Vt is threshold voltage of parker transistor. In active mode header is turned on to charge the virtual power line to supply voltage level. The schematic diagram of SRAM cell using TRIMODE MTCMOS power gated technique is shown in Fig.11.

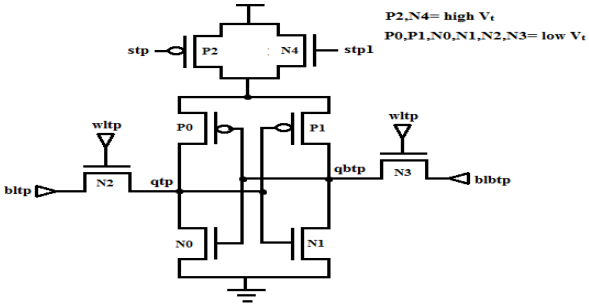

Fig. 11. Schematic diagram of SRAM cell using TRIMODE MTCMOS power gated technique

The sleep transistors are controlled by the inputs "stp" and "stp1". In standby mode word line ("wltp") and "stp1" is made low, "stp" is made high. The header (P2) and parker (N4) transistors are in OFF state, cutting off the power supply to the SRAM cell. The cell in this mode is in hold state and power measured in this state is static power. In park mode word line "wltg", "stg1" and "stg" is made high. The header (P2) is in OFF state and parker (N4) transistors is in ON state, the virtual power line will be at the potential Vdd-Vt allowing SRAM cell to perform its operations. In active mode, word line "wltg" is made high, "stp" and "stp1" is made low so header transistor (P2) conduct. In this mode the virtual power line is charged to supply voltage value, allowing SRAM cell to perform write and read operation efficiently than in park mode. The power measured in this mode is dynamic power. The inputs were "bltg" and "blbtg" and outputs were "qtg" and "qbtg".

III. Design of SRAM cell using Hybrid Techniques

The conventional techniques described in previous section have disadvantages such signal quality problem and

no suitable decrease in power dissipation. To overcome those disadvantages hybrid techniques were designed.

A. A. SRAM Cell using Sleepy Keeper and Drain Gating Techniques

On analysis of different low techniques to reduce static power, sleepy keeper and drain gating provides better result. Combining these two techniques uses extra eight transistors in addition to the six transistors of SRAM cell. The six extra transistors were controlled externally by control signals and two helper transistors were driven by output to avoid data retention problem [15]. The schematic diagram of SRAM cell using sleepy keeper and drain gating techniques is shown in Fig.12

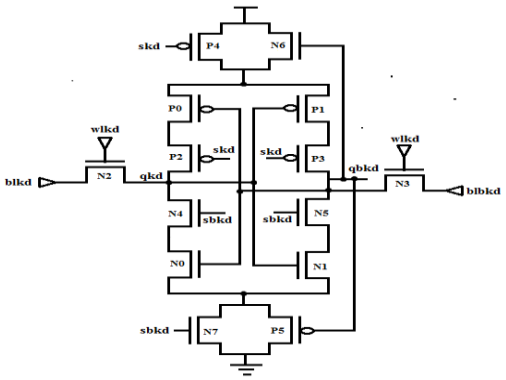

Fig. 12. Schematic diagram of SRAM cell using sleepy keeper and drain gating techniques

The sleep transistors are controlled by the inputs "skd" and "sbkd". The designed SRAM cell operates in two modes. In active mode the word line ("wlkd") and "sbkd" is made high, "skd" is made low. The transistors connected between pull up network and pull down network (P2,P3,N4,N5), transistor connected between pull up network and supply voltage (P4), transistor connected between pull down network and ground terminal (N7) are turned to ON state. This condition causes the SRAM cell to perform write and read operation efficiently. In standby mode the word line ("wlkd") and "sbkd" is made low, "skd" is made high. The transistors connected between pull up network and pull down network (P2,P3,N4,N5) is turned OFF causing stack effect inside the SRAM cell, transistor connected between pull up network and supply voltage (P4), transistor connected between pull down network and ground terminal (N7) are turned OFF cutting off supply voltage and ground terminal to SRAM cell. These conditions cause reduction in the leakage current flowing in the circuit and thus reduces static power dissipation. In this mode one of the helper transistor (N6 or P5) keeps connection with appropriate power rail, thus retaining the previous logic state. The inputs are "blkd" and "blbkd" and outputs are "qkd" and "qbkd". The main drawback of this technique is much increase in area.

B. SRAM Cell using Drain Gating Technique and Helper Transistors

This technique uses extra eight transistors in addition to the six transistors of SRAM cell all of which were controlled externally by control signals. Out of eight, four sleepy transistors are connected between pull up and pull down network. Four helper transistors (2 PMOS, 2 NMOS) in which NMOS transistors are connected in parallel to pull up network and PMOS transistors are connected in parallel to pull down network [20]. This type of connection has the advantage that the effective potential difference between the two power rails is reduced. The schematic diagram of SRAM cell using drain gating technique and helper transistors is shown in Fig.13.

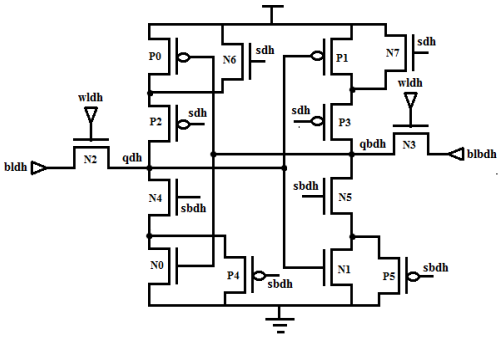

Fig. 13. Schematic diagram of SRAM cell using drain gating technique and helper transistors

The sleep transistors and helper transistors are controlled by "sdh" and "sbdh". The SRAM cell operates in two modes. In active mode, word line ("wdh") and "sbdh" are made high, "sdh" is made low. This condition causes helper transistors (N6,N7,P4,P5) to be turned OFF and sleepy transistors (P2,P3,N4,N5) to be turned ON allowing the SRAM cell to perform read and write operation. In standby mode, word line ("wdh") and "sbdh" are made low, "sdh" is made high. This condition causes helper transistors (N6,N7,P4,P5) to be turned ON and sleepy transistors (P2,P3,N4,N5) to be turned OFF. As the sleep transistors are turned OFF it causes stack effect inside SRAM cell thereby reducing the leakage current inside the cell. At the same case, the helper transistors are turned ON. Due to this condition, pull up network is now connected between Vdd and Vdd- Vth similarly pull down network gets connected between ground and virtual ground Vss+Vth hence, almost no leakage current will flow in pull up and pull down network [16]. The inputs are "bldh" and "blbdh" and outputs are "qdh" and "qbdh". The main drawback of this technique is much increase in area.

C. SRAM Cell using USVL and Trimode MTCMOS Ground Gated Techniques

In case of one conventional technique, SRAM cell designed with TRIMODE MTCMOS ground gated has a disadvantage, full supply voltage is applied to the circuit in all modes of operation. So to overcome it the upper self controllable voltage level (USVL) technique is inserted between pull up network and supply voltage to reduce gate leakage current [13] in pull up network along with trimode MTCMOS ground gated inserted between pull down network and ground terminal. The circuit designed operates in three modes in which park mode is not taken into account. The schematic diagram of SRAM cell using USVL and TRIMODE MTCMOS ground gated is shown in Fig.14.

The SRAM cell operates in two modes. In active mode word line ("wlug"), "stg" and "stg1" is made high, "su" and "sbu" is made low. This causes transistors (P3,N4) to be ON

and transistors (P2,N5) to be OFF. USVL allows full supply voltage applied to the SRAM cell and in trimode MTCMOS ground gated, the footer NMOS transistor (N4) is turned ON and parker PMOS transistor (P2) is turned OFF, this causes virtual ground line to be discharged to zero volts and thereby allowing SRAM cell to perform read and write operation efficiently. The power measured in this mode is dynamic power. In standby mode ("wlug") and "stg" is made low, "su" ,"stg1" and "sbu" is made high. This causes transistors (P3,N4,P2) to be OFF and transistor (N5) to be ON. USVL allows voltage of Vd (Vdd-Vt) to be applied to SRAM cell causing decrease in drain voltage of transistors in SRAM cell, reducing gate leakage current and thereby reducing static power dissipation in pull up network [22]. In pull down network the footer NMOS (N4) as well parker PMOS (P2) of trimode MTCMOS ground gated are turned OFF causing ground connection to be cut off from SRAM cell thereby reducing the leakage power. The power measured in this mode is static power. The inputs are "blug" and "blbug" and outputs are "qug" and "qbug".

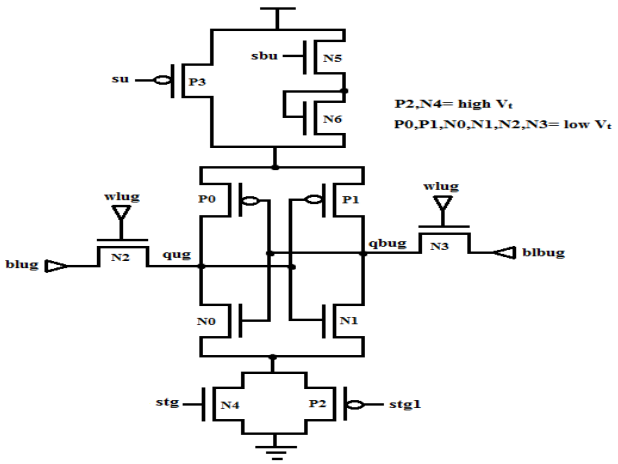

Fig. 14. Schematic diagram of SRAM cell using USVL and Trimode MTCMOS ground gate

D. SRAM Cell using LSVL and Trimode MTCMOS Power Gated

In case of one conventional technique, SRAM cell designed with TRIMODE MTCMOS power gated has a disadvantage, ground terminal is always connected to the circuit in all modes of operation. So, to overcome it the lower self controllable voltage level (LSVL) technique is inserted between pull down network and ground terminal to reduce gate leakage current [13] in pull down network along with trimode MTCMOS power gated inserted between pulup network and supply voltage. The SRAM designed operates in three modes in which park mode is not taken into account. The schematic diagram of SRAM cell using LSVL and TRIMODE MTCMOS power gated is shown in Fig.15.

The SRAM cell operates in two modes. In active mode word line ("wllp"), "sl" and "slb" is made high,"stp" and "stp1" is made low. This causes transistors (P2,N5) to be ON and transistors (P4,N4) to be OFF. LSVL allows ground terminal to be connected to the SRAM cell and in trimode MTCMOS power gated, the header PMOS transistor (P2) is turned ON and parker NMOS transistor (N4) is turned OFF, this causes virtual power line to be voltage to be equal to Vdd and thereby allowing SRAM cell to perform read and write operation efficiently. The power measured in this mode is dynamic power. In standby mode ("wlug"), "slb", "stp1" and "sl" is made low, "stp" is made high. This causes transistors (N5,P2,N4) to be OFF and transistor (P4) to be ON. LSVL causes increase in virtual ground voltage, results in decrease in gate source and gate drain voltages of transistors which is in OFF state and gate drain voltage of transistors which is in ON state in SRAM cell [22], reducing gate leakage current and thereby reducing static power dissipation in pull down network. In pull up network the header PMOS (P2) as well parker NMOS (N4) of trimode MTCMOS power gated are turned OFF cutting off the power connection to SRAM cell thereby reducing the leakage power. The power measured in this mode is static power. The inputs are "bllp" and "blblp" and outputs are "qlp" and "qblp".

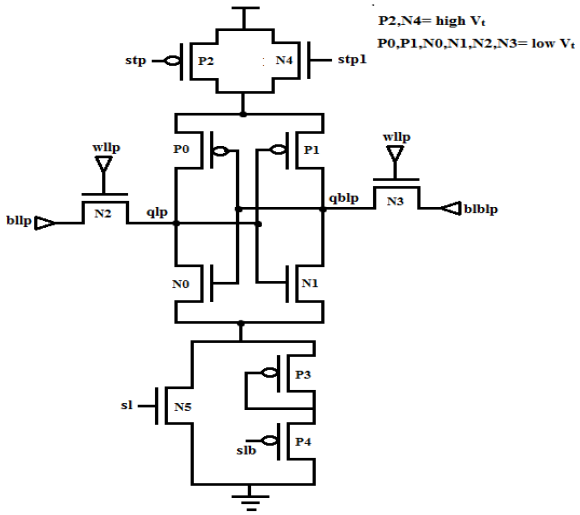

Fig. 15. Schematic diagram of SRAM cell using LSVL and trimode MTCMOS power gated

IV. DESIGN OF PROPOSED SRAM CELL

Proposed SRAM cell was designed by combining TRIMODE MTCMOS power and ground gated techniques. The proposed SRAM cell consist of ten transistors in which four are high Vt transistors and six are low Vt transistors. High Vt transistors are slow, but have a low subthreshold leakage current and low Vt transistors are fast, but have a high subthreshold leakage current. The SRAM cell is implemented using low Vt transistors to perform fast operation and sleepy transistors were implemented using high Vt transistors to have low subthreshold leakage current. The proposed SRAM cell operates in three modes, active, park and standby mode. The schematic diagram of proposed SRAM cell using TRIMODE MTCMOS power and ground gated is shown in Fig.16.

The sleepy transistors are controlled externally by "spg", "spg1", "spg2" and "spg3". The proposed SRAM cell operates in three modes. In active mode the word line ("wlpg"), "spg2" and "spg3" are made high, "spg" and "spg1" are made low. This causes header (P2) and footer (N5) transistors to be turned ON and parker transistors (P3,N4) are turned OFF allowing virtual power line voltage

to be equal to supply voltage and virtual ground line voltage to be at zero volts. In this case SRAM cell performs its operations efficiently. The power measured in this mode is dynamic power.

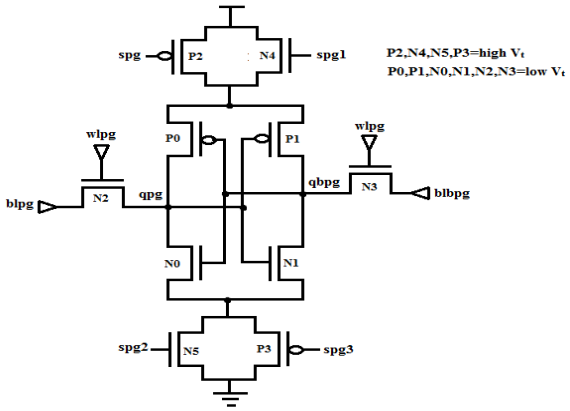

Fig. 16. Schematic diagram of proposed SRAM cell

In standby mode, the word line ("wlpg"), "spg1" and "spg2" are made low, "spg" and "spg3" are made high. This causes header (P2), footer (N5) and parker transistors (N4,P3) to be turned OFF, cutting off power supply and ground terminal from SRAM cell thereby reducing the leakage power. The power measured in this mode is static power. In park mode, the word line ("wlpg"), "spg" and "spg1" are made high, "spg2" and "spg3" are made low. This causes header (P2) and footer (N5) transistors are turned OFF and parker transistors (N4,P3) are turned ON, virtual power line will be at voltage Vdd-Vt and virtual ground line will be at voltage Vss+Vt, so it helps in retaining the previous data stored in active mode and avoids data retention problem. The inputs are "blpg" and" blbpg" and outputs are "qpg" and "qbpg". The proposed design provides less static power and delay with less increase in area.

V. Simulation Results and Graphical Analysis

A. Simulation result

The SRAM cells are designed using SYNOPSYS (Custom designer) tool in 30nm technology. The parameters measured are static and dynamic power, delay, rise and fall time, slew rate. The parameters power delay product, energy, energy delay product were calculated from measured values. Static noise margin [24] is calculated from the butterfly curves which are obtained by voltage transfer characteristics of any one inverter in the SRAM cell. The length of side of largest square that can fit into lobes of butterfly curves gives the SNM value. The area in each design is calculated by having no of transistors count.

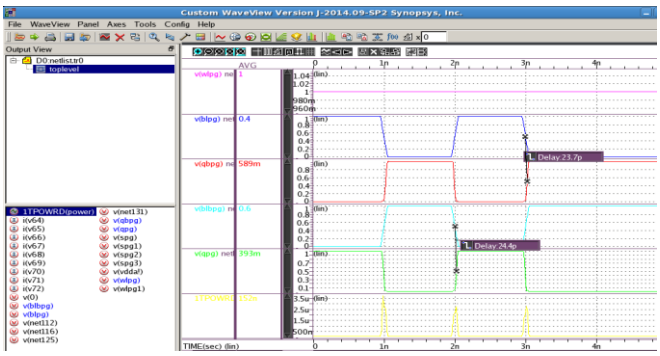

Fig. 17. Simulation result of proposed SRAM cell

Fig.17. shows the simulation result of proposed SRAM cell. The waveforms in the figure indicate that word line (wlpg) is asserted to one to perform read and write operation. The inputs are "blpg" and "blbpg" and outputs are "qpg" and "qbpg".

B. Layout

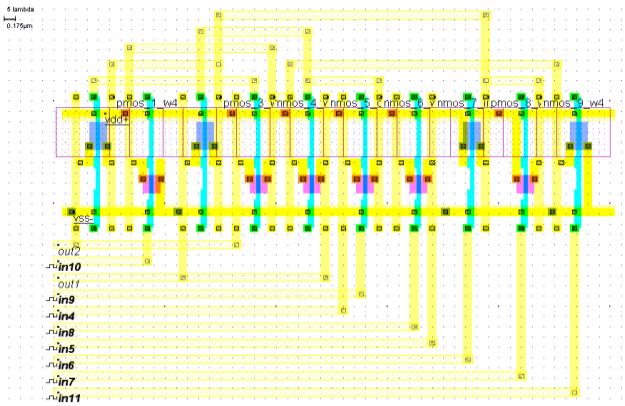

Fig. 18. Layout of proposed SRAM cell

The layout of proposed SRAM cell is shown in Fig.18. The layout of proposed SRAM cell is generated [27]. Although it causes some extra area overhead due to use of sleepy transistors, but it is least concern in nanometer regime.

C. Graphical representation of different parameters for SRAM cell using hybrid techniques

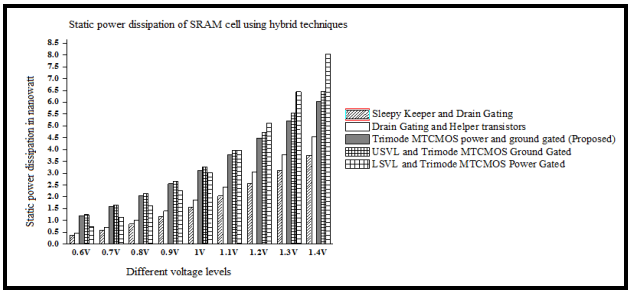

Fig. 19. Static power dissipation of SRAM cell using hybrid techniques

TABLE I. DESIGN METRICS COMPARISON OF SRAM CELL USING DIFFERENT TECHNIQUES FOR INPUT VOLTAGE 0.6V

Various parameters	**Different techniques (Input voltage = 0.6V)**										
	Conventional	MTCMOS	LECTOR	GALEOR	Sleepy Keeper	Drain Gating	LCNT	VCLEARIT	DTMOS	TRMTPG	TRMTGT
Static power dissipation (W)	11.3n	1.2n	6.84n	5.12n	404p	458p	7.75n	60.7n	29.5n	1.24n	1.26n
Delay (ps)	62.7	70.5	98.8	99.7	74.9	110	60.1	83.1	73.2	68	49.7
Dynamic power dissipation (W)	29n	29.8n	30.8n	23.6n	35.9n	49.4n	35.4n	61.2n	1.4u	30.3n	29.3n
Slew rate (Hz)	15.2G	6.11G	2.4G	259M	7.9G	5.3G	6.9G	6.1G	8.1G	6.05G	16.8G
Energy dissipation (J)	22.6n	2.4n	12.9n	10.2n	808p	916p	15.5n	121.4n	59n	2.48n	2.52n
Fall time (ps)	173	64.4	-	-	980	163	886	215	985	56.8	64
Rise time (ps)	35.8	83.7	-	-	70.7	100	54	84.6	72.7	85.7	29.7
Power delay product (J)	708.5 $x10^{-21}$	84.6 $x10^{-21}$	676.4 $x10^{-21}$	588.8 $x10^{-21}$	3025.9 $x10^{-24}$	5633.1 $x10^{-24}$	465.7 $x10^{-21}$	5044.1 $x10^{-21}$	2159.4 $x10^{-21}$	84.32 $x10^{-21}$	62.62 $x10^{-21}$
Energy delay product (Js)	1417.2 $x10^{-21}$	169.2 $x10^{-21}$	1280.4 $x10^{-21}$	1126.4$x10^{-21}$	6051.9 $x10^{-24}$	1126.8 $x10^{-24}$	931.5 $x10^{-21}$	1008.8 $x10^{-21}$	4318 $.x10^{-21}$	168.64 $x10^{-21}$	125.2 $x10^{-21}$

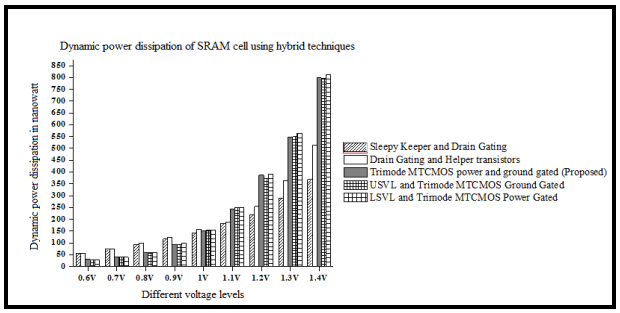

Fig. 20. Dynamic power dissipation of SRAM cell using hybrid techniques

Fig.19 and Fig.20 shows static and dynamic power dissipation of SRAM cell designed using hybrid techniques. Fig.18 shows that static power dissipation of SRAM cell designed using sleepy keeper and drain gating techniques is lower than other hybrid techniques.

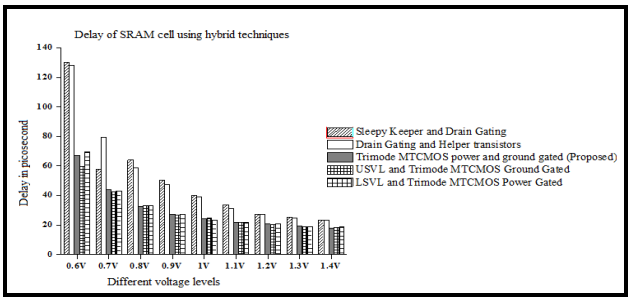

Fig. 21 Delay analysis of SRAM cell using hybrid techniques

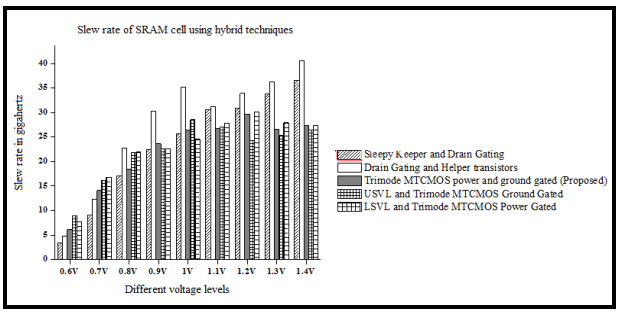

Fig. 22. Slew rate of SRAM cell using hybrid techniques

Fig.21 and Fig.22 shows delay and slew rate analysis of SRAM cell designed using hybrid techniques. Fig.20 shows that incase of different hybrid techniques, SRAM cell designed using sleepy keeper and drain gating approaches has greater delay.

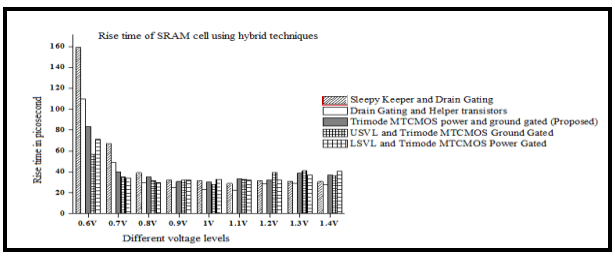

Fig. 23. Rise time of SRAM cell using hybrid techniques

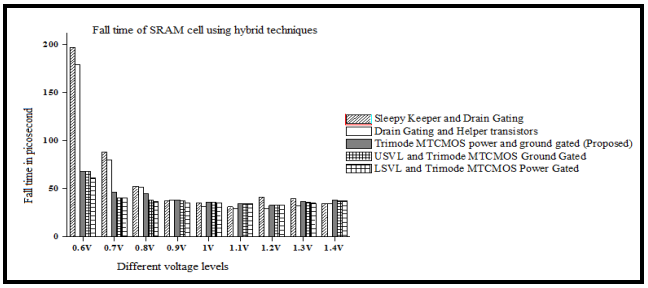

Fig. 24. Fall time of SRAM cell using hybrid techniques

Fig.23 and Fig.24 shows fall time and rise time analysis of SRAM cell using hybrid techniques. These figures indicate that hybrid techniques maintain correct logic levels at different supply voltages.

TABLE II. SNM ANALYSIS AND NO OF TRANSISTOR COUNT OF SRAM CELL USING DIFFERENT TECHNIQUES

Different Techniques	SNM value in volts	No of transistors
Conventional	1.5	6
MTCMOS	0.8	8
LECTOR	1.4	10
GALEOR	1.2	10
Sleepy Keeper	0.9	10
Drain Gating	1.2	10
LCNT	1.1	10
VCLEARIT	1	12
DTMOS	0.2	6
TRMTPG	1.1	8
TRMTGT	1	8
Sleepy Keeper and Drain Gating	1.1	14
Drain Gating and Helper transistors	1.3	14
Trimode MTCMOS (Power and Ground Gated)	**1.4**	**10**
USVL and Trimode MTCMOS Ground Gated	1.1	11
LSVL and Trimode MTCMOS Power Gated	1	11

Fig.25, Fig.26, Fig.27 shows power delay product, energy dissipation and energy delay product of SRAM cell using hybrid techniques. These figures indicate using hybrid techniques the parameter values which are considered get decreased compared to conventional technique.

In case of lower supply voltage value, LECTOR, GALEOR techniques [17] does not have good rise and fall time (one of the extra inserted transistors are always in cutoff state). Techniques such as sleepy keeper [15] and drain gating dissipates less static power due to stack effect in first case and due to cutting of power rails in second case. Techniques such as TRIMODE MTCMOS power and ground gated [12] provides very less delay due to use of different threshold voltage transistors. Techniques such as DTMOS, VCLEARIT [16] dissipates large amount of dynamic power which is due to control of substrate voltage by gate terminal in first case and due more transistors ON (more switching activity) in second case. Table 1 shows the various techniques with parameters.

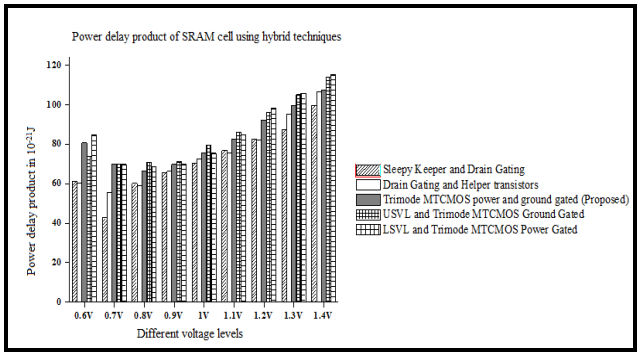

Fig. 25. Power delay product of SRAM cell using hybrid techniques

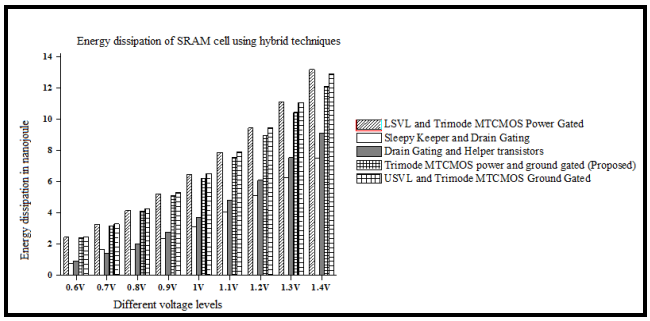

Fig. 26. Energy dissipation of SRAM cell using hybrid techniques

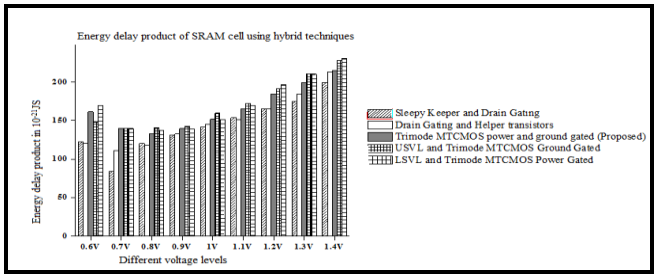

Fig. 27. Energy delay product of SRAM cell using hybrid techniques

Table 2 specifies static noise margin analysis [24] and no of transistors count of SRAM cell using different techniques. The results in table indicates the followings,

SRAM designed using DTMOS technique does not have better stability due to variation of substrate voltage with the gate terminal. SRAM designed using TRIMODE MTCMOS power and ground gated techniques have better stability due to three modes of operations which reduces noise margin values. The SRAM cell designed using VCLEARIT consumes large area due to use of more transistors.

VI. CONCLUSION

The SRAM cells designed using hybrid techniques provides better reduction in most of the parameters which are taken into account compared to conventional techniques. In all the techniques power and delay has been reduced considerably. But the area is increased because of use of extra sleep transistors. Although power has been reduced in all techniques compared to conventional, combining TRIMODE MTCMOS power and ground gated shows best result in terms of power, delay and area. The proposed SRAM cell was designed using SYNOPSYS tool in 30nm technology. Combining TRIMODE MTCMOS power and ground gated technique when applied to SRAM cell reduces the dynamic power dissipation, delay, static power, power delay product, energy, energy delay product by 22%, 12%, 91%, 86%, 90% and 85% compared to conventional technique. In modern day processor power dissipation plays a major role because of the miniaturization of chip design. So, this hybrid technique of combining power and ground gated TRIMODE MTCMOS technique can be used in future where considerable reduction of parameters such as power dissipation, delay and area are needed. In case of RAM, cost and size of DRAM cells are less compared to SRAM cells and power is only disadvantage of DRAM so these powers optimized cell can be used to replace DRAM cell. The proposed SRAM cell can be used to design array structure which replaces in the area of suitable low power applications.

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