VLSI AND NANO TECHNOLOGY

Low Latency Scheduling of Point Multiplication Featuring High Speed GF (2^m) Multiplier Suitable for FPGA Implementation

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ABSTRACT

Point Multiplication (PM) is the most tedious and time consuming operation in Elliptic Curve Cryptography (ECC). Performing PM using a standalone hardware platform – the Field Programmable Gate Array (FPGA) is much necessary for high speed, secured communication. In this paper, we employ Lopez-Dahab (LD) Montgomery PM algorithm to perform PM faster, resisting the side channel attacks. We propose a careful scheduling of LD algorithm to reduce the number of clock cycles; thus reducing latency. Speed of PM fully depends on the speed of finite field multiplier. We implemented the finite field Montgomery modular multiplier in several FPGAs and found that Virtex6 FPGA achieves the highest speed (14.81 ns).

Keywords: Point Multiplication (PM), Elliptic Curve Cryptography (ECC), Field Programmable Gate Array (FPGA), Lopez-Dahab (LD) Montgomery PM Algorithm

An Ultra Low Power VLSI Architecture for Viterbi Decoder Using Subthreshold Adiabatic Logic

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ABSTRACT

In modern digital world, the major features expected are portability and reliability. There is a tremendous development in the field of wireless communication systems. Viterbi decoder, the heart of the wireless communication receivers, facilitates the correction of transmission errors occurred in the transmission channels. To realize a portable system, ultra low power digital integrated circuit design is vital. In this paper, we reduced the power consumption of Viterbi decoder and thereby reduced the heat dissipation of the integrated circuits. We propose a novel technique, Viterbi decoder based on sub-threshold adiabatic logic, to achieve power reduction. This approach is used where power consumption is the major concern instead of performance. It is observed that the power consumption of the circuits is more desirable compared with conventional static CMOS implementation.

Keywords: Viterbi Decoder, Subthreshold Adiabatic Logic, Power Consumption

Design of Novel SRAM cell using Hybrid VLSI Techniques for Low Power and High Speed in Embedded Memories

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ABSTRACT

Static or leakage power is the dominating component of total power dissipation in deep nanometer technologies below 90nm, which has resulted in increase from 18% at 130nm to 54% at 65nm technology due to continued device and voltage scaling. Static Random Access memory (SRAM) is a type of RAM in which data is not written permanently and it does not need to be refreshed periodically. Different techniques have been applied to SRAM cell to reduce leakage power without affecting its performance. A novel 10T SRAM architecture is proposed in this paper which operates in three modes (active, park, standby or hold). The main objective of the proposed architecture is to provide better stability and reduced delay in active mode, reduced leakage current in standby mode and retaining the logic state in park mode. Design metrics such as static and dynamic power, delay, power delay product, energy, energy delay product, rise and fall time, slew rate and static noise margin are taken into account. All the circuits were designed using SYNOPSYS EDA tool and simulated in 30nm technology. Simulation results shows that the proposed SRAM is much better than conventional and other SRAM cells designed using hybrid techniques.

Keywords: CMOS, SRAM cell, Low power, High Speed, Subthreshold current.

In Depth Survey on SMS4 Architecture

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ABSTRACT

In the present world, securing data is very necessary in every industry especially in defense sector and banking sector. Many encryption algorithms are proposed to prevent the data theft. In this paper various architectures of SMS4 algorithm is discussed. SMS4 is a Chinese standard cipher developed for securing information in Wireless Local Area Network (WLAN). This survey is done to propose a new modified SMS4 architecture, which can perform secure encryption and decryption better than the existing SMS4 architectures. Finally discussed about the possible ways of changes can be done for improvement.

Keywords: DPA, LUT,SMS4, Twisted BDD, ESMS4

Survey on Adaptive Filter Applications

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ABSTRACT

Yet without a doubt comprehended and extensively used, adaptable isolating applications are not viably fathomed, and their models are not successfully streamlined. At the present time, flexible filtering application is associated in such unique fields as radar, biomedical application. In spite of the way that these diverse applications are through and through various in the nature, fundamental segment can be seen: a information vector and needed response are used to enroll a estimation bungle, which is used, in this manner, to minimize the estimations of a game plan of adaptable channel coefficients. Adaptable coefficients may show up as tap weights, reflection coefficients, or rotate parameters, dependent upon channel structure used. Notwithstanding varying assortment and capriciousness, a direct request of flexible isolating does rise and sensible applications can be outlined. Application. note begin by delineating four essential classes of adaptable isolating applications and takes after with zones that detail distinctive nuts and bolts, strategies, and counts of a couple of picked flexible applications.

Keywords: Adaptive Filter, VLSI

Area Efficient Implementation of Adaptive Filters using High Level Transformation

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ABSTRACT

Signals carry important information about the behaviour of system under study. Generally, background noises present in the environment corrupt the signal. Raw signals comprises of signal of interest with extraneous noises present in them. Thus it is very important to remove the noises and retrieve the signal of interest. Adaptive filters play an important role in manipulation of the information present in the signal. This paper presents an effort to implement the associativity technique in the adaptive filter design . The proposed architecture is used to reduce the area of the structure. The designed architecture with RLS, Affine Projection (AP) and Kalman filters depict improvement in SNR and VLSI implementation promises to be effective design in terms of area reduction.

Keywords: Adaptive filter, RLS, Affine, Associativity, SNR.

2D Lifting Based Discrete Wavelet Transform Architecture based on Sub Expression Reduction Technique

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ABSTRACT

There are several methods to implement DWT. But lifting scheme is preferred because it reduces the computational complexity and is easy to implement. 9/7 filter coefficient are used in lifting scheme since they are originally implemented in JPEG codec 2000. Much architecture were developed using lifting scheme. But the number of computations is more leading to less efficient architecture. As an existing work, CSD algorithm based parallel flipped lifting 2D DWT using dual-scan technique (CSDPF) is designed with the modified flipping scheme using Canonical Signed Digit (CSD) algorithm.

In order to reduce the computations Flipping Structure for a Lifting based Discrete Wavelet Transform using Sub Expression Sharing (SES) is developed for image compression. To improve the computational efficiency, area and power requirements sub expression sharing technique is used. In the case where several multipliers are present in a network of operators, the savings is achieved by identifying common subexpressions and sharing the two most common subexpressions that is expected to save the number of additions. It reduces the arithmetic resources like shifter and adder in its implementation. Using SES method the number of computations is reduced to half of the total computations. Hence a computationally efficient architecture with area and power reduction by 32% and 5% respectively is designed. The various applications include fax transmission, satellite remote sensing, high definition television, storage and transmission of CT and MRI scans etc.

Keywords: DWT, Flipping Structure, SES

2D Lifting Based Discrete Wavelet Transform Architecture using Modified Reduced Hardware Algorithm

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ABSTRACT

Lifting Based Discrete Wavelet Transform (LDWT) is the proficient mode to generate biorthogonal wavelet transforms and as well to work out classical wavelet transforms. This Modified Reduced Hardware Algorithm (MRHA) is based on a flipping technique in order to reduce arithmetic components with a straightforward control path. To achieve one multiplier delay of critical path and 100 percent hardware utilization efficiency the lifting data flow is

performed using parallel computations. The proposed MRH algorithm is varied in accordance with the mathematical modifications.

MRH algorithm uses associative principle which is applied to the mathematical modifications of the original lifting steps to reduce the number of arithmetic components required to perform compression. This architecture follows the basic lifting steps like splitting, predicting and updating but merges the predictor with the updater. By performing parallel operation using the two-input, two-output architecture the high pass and low pass values can be calculated. DWT provides high coding efficiency and better quality of image restoration when assimilate with the conventional Discrete Cosine Transform.

As a result, it is a speed competent, least hardware regular design with minimum memory requirement. Because of these competences it can be useful to several real-time visual setups viz. JPEG2000, MPEG-4 still texture object decoding, etc. The MRHA based architecture is verified in Lab VIEW tool that shows that the architecture splits the image into four sub-bands namely LL, LH, HL and HH. The architecture implemented on Xilinx ISE 8.2 tool indicates that, it is high speed architecture to compress an image and increases the speed by 20% when compared to existing architecture.

Keywords: LDWT, MRH Algorithm, JPEG 2000

A Novel Ternary Half Adder & One Bit Multiplier Circuits based on Emerging sub-32nm FET Technology

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ABSTRACT

In this paper, we present a novel low-power and high-performance new ternary logic arithmetic circuit that is implemented by double gate (DG) FinFET and graphene nanoribbon (GNR) field effect transistor (GNRFET). Multiple-valued logic (MVL) such as penternary, quaternary and ternary is a promising alternative to the binary logic design, because of less complexity, less computational step and reduced chip area. The basic ternary gates and its operation are already described in my previous paper [20]. Ternary logic gate based arithmetic combinational circuits such as ternary half adder and one-bit ternary multiplier are designed. The proposed ternary combinational circuits are simulated using HSPICE via standard 32nm DG-FinFET and GNRFET technology. Extensive simulation results demonstrate that the Graphene field effect transistor based ternary logic arithmetic circuits

are more improved than the DG FinFET technology in terms of power consumption, delay and Power delay product (PDP).

Keywords: Double gate field effect transistor, FET, Graphene field effect transistor, MVL, Tenrary Half Adder, Ternary Multiplier.

Effects of Microwave Annealing of Graphene and its Impact on Structural, Electrochemical Performance for Energy Storage

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ABSTRACT

In this paper, graphene was prepared via modified hummers' method and then with the help of microwave treatment of as prepared graphene, microwave graphene (MG) was prepared. From the electro chemical experiments, graphene and MG exhibited improved electro chemical performance. Electro chemical performance of graphene and MG electrodes were measured by cyclic voltammetry (CV), galvanostatic charge and discharge measurement (GCD) and electrochemical impedance spectroscopy (EIS). The specific capacitance value of 275 Fg^{-1} And 316 Fg^{-1} for graphene and MG, respectively. Equivalent series resistance of MG was 1.78 Ω and charge transfer resistance was 1.33 Ω, smaller than that of graphene. The fabricated electrodes of supercapacitor show the improved equivalent series resistance and capacitance value. The improved performance of MG electrode was ascribed to the porous nature of graphene after microwave annealing. This work gives the great interest towards the material for high performance high energy and power density application.

Keywords: annealing, electrode grapheme, microwave, super capacitor

Automatic Solar Powdered Grass Cutter Incorporated with Alphabet Printing and Pesticide Sprayer

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ABSTRACT

Lawn maintenance provides aesthetic pleasure to people. The maintenance of lawn can be done with the help of lawn mower. The operation of the lawn mower is very difficult. The automatic grass cutter provides less human intervention. It operates with the help of solar power. Because of this, no pollution is caused. The grass cutter is incorporated with alphabetic printing and pesticide sprayer. The sound produced by the cutter is very low so, it can be used in silence zone areas such as hospitals, educational institutions.

The grass cutter is incorporated with alphabet printing mechanism in grass. Alphabet printing is cutting of grass in the shape of alphabets. The pesticide sprayer is also attached with the grass cutter. All these machines are available as separate machines which require more space and the cost for buying separate machines will be more. The main advantage of our project is to reduce the space, cost and man power required.

Area and Power Efficient Approximate Wallace Tree Multiplier using 4:2 Compressors

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ABSTRACT

Over the years, the complexity of VLSI design circuits has increased dramatically. With this improvement, there comes the need for low area and low power VLSI circuits. The common known fact is that multiplier circuit plays an important role in the digital processor design. Nowadays, low power and low area multiplier designs are in high demand. Compared to other multipliers, Wallace tree multipliers are considered to be fast rather than other multipliers. For performing the process of multiplication, there will be many stages inbetween and those stages are also have to be realized or implemented using additional gate circuits. This usage of additional circuits will finally results in increased area which inturn increases the power consumption also. To overcome these disadvantages, Approximate Wallace Tree Multiplier is implemented using incomplete adder cell (ICAC) and Accurate Compressor with Cin and Cout ignored (ACCI2) circuits. It is found out that it reduces the area compared to normal Wallace Tree Multiplier Design. Here, another method for Approximate Wallace multiplier using 4:2 compressors is proposed to keep the area overhead minimal. This method uses four to two compressors for addition and this circuit is used in the Approximate Wallace Tree Multiplier. The above designs are synthesized using Synopsys e and the power consumed and area occupied by both the methods is compared. By comparing, the multiplier with compressor minimizes the area by 98.39% when compared to Approximate Multiplier which also reduces the power consumption by 98.13%.

Keywords: Approximate Multiplier, ACCI2, 4:2 Compressors

An Improved Transformerless Inverter Topology for Grid Connected Photovoltaic System

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ABSTRACT

Transformerless inverters are gaining importance in grid integration of PV power due to high efficiency, compact size and low cost. Leakage current is the major issue in these inverters which needs to be eliminated. The leakage current depends on common mode voltage (CMV), PV module parasitic capacitances and stray switches junction capacitances. In this paper, an improved common mode voltage clamped transformerless inverter topology has been proposed. Unlike H5 and HERIC topologies, the proposed topology generates constant CMV during both power transfer and freewheeling periods. As a result, leakage current is eliminated. Moreover, the proposed topology is compared with classic full bridge and H5 topologies. The analysis of the proposed topology is carried out in Matlab Simulink. A 2.7 kW grid connected inverter prototype was developed in Matlab Simulink environment.

Keywords: Transformerless, photovoltaic, leakage current, CMV