Dual 4-Channel Analog Data Selector

The MC14529B analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various one-of-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

- Data Paths Are Bidirectional
- 3-State Outputs
- Linear "On" Resistance
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load over the Rated Temperature Range.

MAXIMUM RATINGS* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
Syllibol	i arameter	Value	Oiii
V_{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V _{DD} + 0.5	V
l _{in} , l _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

^{*} Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating:

Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

TRUTH TABLE (X = Don't Care)

I	RUIH	ABLE	(X = Do	n't Care	?)	
SΤχ	STY	В	Α	Z	W	
1	1	0	0	X0	Y0	h
1	1	0	1	X1	Y1	Dual 4-Channel Mode
1	1	1	0	X2	Y2	2 Outputs
1	1	1	1	Х3	Y3	J
1	0	0	0	Х	0	\cap
1	0	0	1	х	1	
1	0	1	0	х	2	
1	0	1	1	Х	.3	Single 8–Channel Mode > 1 Output
0	1	0	0	Y	0	(Z and W tied together)
0	1	0	1	Y	1	
0	1	1	0	ΙΥ	2	
0	1	1	1	Y	3	Į)
0	0	Χ	Χ	Hi	gh	
				Imped	dance	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

MC14529B



L SUFFIX CERAMIC CASE 620



P SUFFIX PLASTIC CASE 648

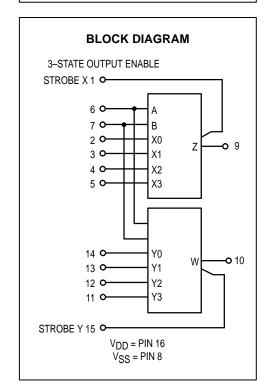


D SUFFIX SOIC CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic MC14XXXBCL Ceramic MC14XXXBD SOIC

 $T_A = -55^{\circ}$ to 125°C for all packages.





ELECTRICAL CHARACTERISTICS

				– 55°C			25°C		125°C		
Characteristic	Symbol	v_{DD}	Test Conditions	Min	Max	Min	Тур#	Max	Min	Max	Unit
SUPPLY REQUIREMENTS	(Voltages Re	eference	ed to VEE)				•				•
Power Supply Voltage Range	V _{DD}	_	V _{DD} - 3.0 ≥ V _{SS} ≥ V _{EE}	3.0	18	3.0	_	18	3.0	18	V
Quiescent Current Per Package	I _{DD}	5.0 10 15	Control Inputs: $V_{in} = V_{SS}$ or V_{DD} , Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$, and $\Delta V_{switch} \le 500$ mV**	_ _ _	1.0 1.0 2.0	_ _ _	0.005 0.010 0.015	1.0 1.0 2.0	 	60 60 120	μА
Total Supply Current (Dynamic Plus Quiescent, Per Package	I _{D(AV)}	5.0 10 15	T _A = 25°C only (The channel component, (V _{in} – V _{out})/R _{on} , is not included.)		Т	ypical	(0.07 μA/kł (0.20 μA/kł (0.36 μA/kł	-lz) f + lc	DD		μА
CONTROL INPUTS — INHII	BIT, A, B (Vo	oltages	Referenced to V _{SS})								
Low-Level Input Voltage	VIL	5.0 10 15	R _{on} = per spec, I _{off} = per spec	— - -	1.5 3.0 4.0	_ _ _	2.25 4.50 6.75	1.5 3.0 4.0	_ _ _	1.5 3.0 4.0	٧
High-Level Input Voltage	VIH	5.0 10 15	R _{on} = per spec, I _{off} = per spec	3.5 7.0 11	_ _ _	3.5 7.0 11	2.75 5.50 8.25	_ _ _	3.5 7.0 11	_ _ _	٧
Input Leakage Current	l _{in}	15	V _{in} = 0 or V _{DD}	_	± 0.1	_	±0.00001	±0.1	_	±1.0	μΑ
Input Capacitance	C _{in}	_		_	_	_	5.0	7.5	_	_	pF
SWITCHES IN/OUT AND CO	OMMONS O	UT/IN -	- W, Z (Voltages Referen	ced to \	√EE)	•		•	•		•
Recommended Peak-to- Peak Voltage Into or Out of the Switch	V _{I/O}	_	Channel On or Off	0	V _{DD}	0	_	V _{DD}	0	V _{DD}	V _{p-p}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 5)	∆V _{switch}	_	Channel On	0	600	0	_	600	0	300	m∨
Output Offset Voltage	Voo	_	V _{in} = 0 V, No Load	_	_	_	10	_	_	_	μV
ON Resistance	R _{on}	10 15	$\begin{array}{l} \Delta V_{Switch} \leq 500 \text{ mV**}, \\ V_{in} = V_{IL} \text{ or } V_{IH} \\ \text{(Control), and } V_{in} = \\ 0 \text{ to } V_{DD} \text{ (Switch)} \end{array}$	_	400 240	_	120 80	480 270	_	560 350	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	10 15		_	_	_	15 10	_	_	_ _	Ω
Off-Channel Leakage Current (Figure 10)	l _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel		± 100	_	± 0.05	± 100	_	±1000	nA
Capacitance, Switch I/O	C _{I/O}	_	Inhibit = V _{DD}				8.0			_	pF
Capacitance, Common O/I	C _{O/I}	_	Inhibit = V_{DD}	_	_	_	20	_	_	_	pF
Capacitance, Feedthrough (Channel Off)	C _{I/O}	_	Pins Not Adjacent Pins Adjacent	_ _	_ _	 _	0.15 0.47				pF

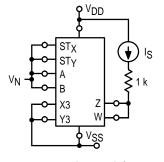
[#]Data labelled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

^{**} For voltage drops across the switch (ΔV_{Switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

SWTCHING CHARACTERISTICS $(T_A = 25^{\circ}C)$

Characteristic	Figure	Symbol	VSS	V_{DD}	Min	Тур #	Max	Unit
V_{in} to V_{out} Propagation Delay Time (C _L = 50 pF, R _L = 1.0 kΩ)	7	^t PLH ^{, t} PHL	0.0	5.0 10 15	_ _ _	20 10 8.0	40 20 15	ns
Propagation Delay Time, Control to Output, $V_{in} = V_{DD}$ or V_{SS} ($C_L = 50$ pF, $R_L = 1.0$ k Ω)	8	t _{PLZ} , t _{PZL} , t _{PHZ} , t _{PZH}	0.0	5.0 10 15	_ _ _	140 70 50	400 160 120	ns
Crosstalk, Control to Output $(C_L = 50 \text{ pF}, R_L = 1.0 \text{ k}\Omega)$ $R_{Out} = 10 \text{ k}\Omega)$	9	_	0.0	5.0 10 15	_ _ _	5.0 5.0 5.0	_ _	mV
Control Input Pulse Frequency (C _L = 50 pF, R _L = 1.0 k Ω)	10	fin	0.0	5.0 10 15	_ _	5.0 10 12	2.5 6.2 8.3	MHz
Noise Voltage (f = 100 Hz)	11, 12	_	0.0	5.0 10 15	_ _ _	24 25 30	_ _ _	nV/ √cycle
				5.0 10 15	_ _ _	12 12 15	_ _ _	
Sine Wave Distortion $ (V_{in} = 1.77 \text{ Vdc RMS} \\ \text{Centered } @ 0.0 \text{ Vdc}, \\ \text{R}_L = 10 \text{ k}\Omega, \text{ f} = 1.0 \text{ kHz}) $	_	_	- 5.0	5.0	_	0.36	_	%
$ \begin{aligned} & \text{Off-Channel Leakage Current} \\ & (V_{in} = + 5.0 \text{ Vdc}, V_{out} = -5.0 \text{ Vdc}) \\ & (V_{in} = -5.0 \text{ Vdc}, V_{out} = +5.0 \text{ Vdc}) \\ & (V_{in} = +7.5 \text{ Vdc}, V_{out} = -7.5 \text{ Vdc}) \\ & (V_{in} = -7.5 \text{ Vdc}, V_{out} = +7.5 \text{ Vdc}) \end{aligned} $	-	l _{off}	- 5.0 - 5.0 - 7.5 - 7.5	5.0 5.0 7.5 7.5	 - - -	± 0.001 ± 0.001 ± 0.0015 ± 0.0015	± 125 ± 125 ± 250 ± 250	nA
$\label{eq:loss_loss} \begin{split} &\text{Insertion Loss} \\ &(V_{in} = 1.77 \text{ Vdc} \\ &\text{RMS centered } @ \ 0.0 \text{ Vdc,} \\ &\text{f} = 1.0 \text{ MHz)} \\ &\text{Iloss} = 20 \text{ Log}_{10} \ (V_{out}/V_{in}) \\ & (R_L = 1.0 \text{ k}\Omega) \\ & (R_L = 100 \text{ k}\Omega) \\ & (R_L = 1.0 \text{ M}\Omega) \end{split}$	13	_	- 5.0	5.0		2.0 0.8 0.25 0.01		dB
$\label{eq:bandwidth} \begin{split} \text{Bandwidth } (-3 \text{ dB}) \\ (\text{V}_{in} = 1.77 \text{ Vdc} \\ \text{RMS centered } @ 0.0 \text{ Vdc}) \\ (\text{R}_{L} = 1.0 \text{ k}\Omega) \\ (\text{R}_{L} = 10 \text{ k}\Omega) \\ (\text{R}_{L} = 100 \text{ k}\Omega) \\ (\text{R}_{L} = 1.0 \text{ M}\Omega) \end{split}$	_	BW	- 5.0	5.0	_ _ _ _	35 28 27 26	_ _ _ _	MHz
$\label{eq:feedthrough} \begin{aligned} \text{Feedthrough and Crosstalk} \\ 20 \ \text{Log}_{10} \ (\text{V}_{out}/\text{V}_{in}) = & -50 \ \text{dB} \\ (\text{R}_{L} = 1.0 \ \text{k}\Omega) \\ (\text{R}_{L} = 10 \ \text{k}\Omega) \\ (\text{R}_{L} = 100 \ \text{k}\Omega) \\ (\text{R}_{L} = 1.0 \ \text{M}\Omega) \end{aligned}$	_	_	- 5.0	5.0	_ _ _ _	850 100 12 1.5		MHz

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Pins 2, 3, 4, 12, 13 and 14 are left open.

$$\begin{split} \text{V}_{IL} \colon \text{V}_{C} \text{ is raised from V}_{SS} \text{ until V}_{C} &= \text{V}_{IL}. \\ \text{at V}_{C} &= \text{V}_{IL} \colon \text{I}_{S} = \pm \ 10 \ \mu\text{A with V}_{in} = \text{V}_{SS}, \ \text{V}_{out} = \text{V}_{DD} \\ \text{V}_{in} &= \text{V}_{DD}, \ \text{V}_{out} = \text{V}_{SS}. \end{split}$$

 V_{IH} : When $V_C = V_{IH}$ to V_{DD} , the switch is ON and the R_{ON} specifications are met.

Figure 2. Noise Immunity
Test Circuit

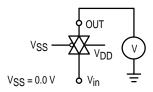


Figure 1. Output Voltage Test Circuit

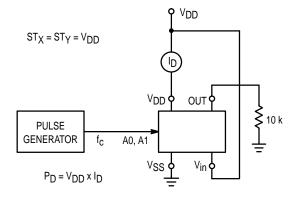


Figure 3. Quiescent Power Dissipation Test Circuit

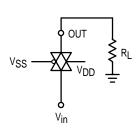


Figure 4. R_{ON} Characteristics Test Circuit

TYPICAL RON versus INPUT VOLTAGE

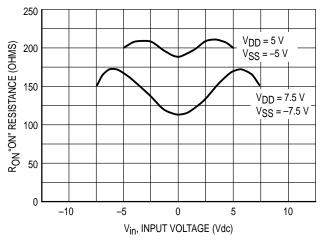


Figure 5.

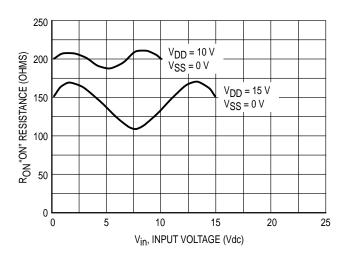


Figure 6.

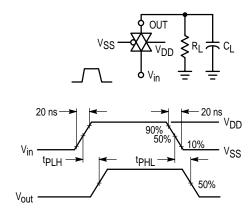


Figure 7. Propagation Delay Test Circuit and Waveforms

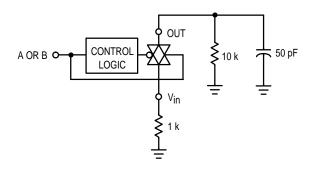


Figure 9. Crosstalk Test Circuit

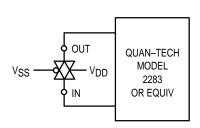


Figure 11. Noise Voltage Test Circuit

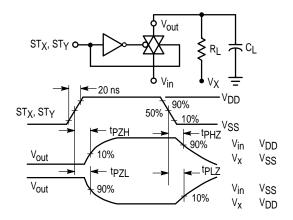


Figure 8. Turn-On Delay Time Test Circuit and Waveforms

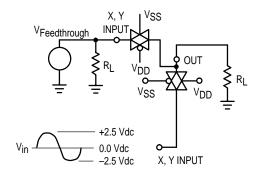


Figure 10. Frequency Response Test Circuit

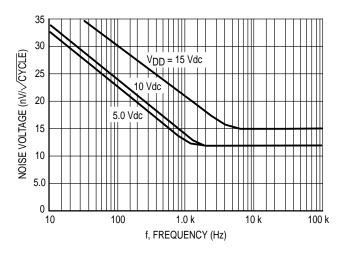


Figure 12. Typical Noise Characteristics

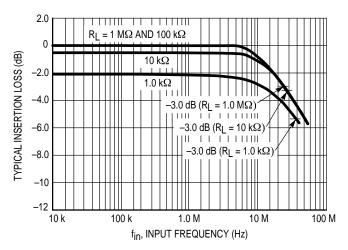
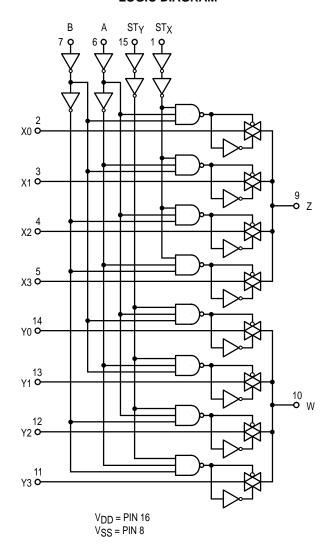


Figure 13. Typical Insertion Loss/Bandwidth Characteristics

PIN ASSIGNMENT ST_X 1 ● 16 V_{DD} X0 [2 15 STY X1 [14 🛮 Y0 X2 🛮 13 TY1 хз Ц 5 12 Y2 11 | Y3 ΑД 6 10 🛭 W в V_{SS} [8 9 🛮 Z

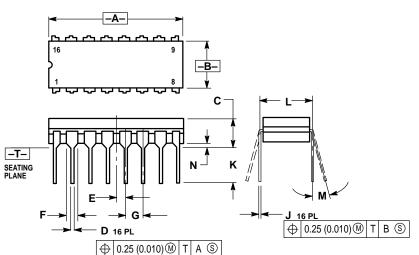
LOGIC DIAGRAM



OUTLINE DIMENSIONS

L SUFFIX

CERAMIC DIP PACKAGE CASE 620-10 ISSUE V



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: INCH.

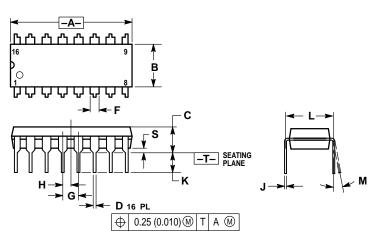
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC RODY.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MIN MAX		MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
C		0.200		5.08	
D	0.015	0.020	0.39	0.50	
Е	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	BSC	2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300	BSC	7.62	BSC	
M	0 °	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	

P SUFFIX

PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: INCH.

 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS		
DIM	MIN	MAX	MIN	MAX		
Α	0.740	0.770	18.80	19.55		
В	0.250	0.270	6.35	6.85		
С	0.145	0.175	3.69	4.44		
D	0.015	0.021	0.39	0.53		
F	0.040	0.70	1.02	1.77		
G	0.100	BSC	2.54	2.54 BSC		
Н	0.050	BSC	1.27 BSC			
J	0.008	0.015	0.21	0.38		
K	0.110	0.130	2.80	3.30		
L	0.295	0.305	7.50	7.74		
M	0°	10°	0°	10 °		
S	0.020	0.040	0.51	1.01		

OUTLINE DIMENSIONS



- DIMENSIONING AND TOLERANCING PER ANSI
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	METERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
C	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
М	0°	7°	0°	7°	
Р	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

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JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



