# IL2239 - Course Project Design of a SAR ADC

J. Altayó B. Sunedahl

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### Outline

Comparator Project Description Digital-to-Analog Converter Roles and Responsibilities Layout Design Flow Comparator System-level Design Digital-to-Analog Converter Problem Statement Simulations **Proposed Solution** Sinusoidal Stimulus Behavioral Modeling Ramp Stimulus Comparator Spectrum Digital-to-Analog Converter Figures of Merit Successive Approximation Register Conclusions Transistor-level Design References

# **Project Description**

Design of a single-ended SAR ADC with the following specifications.

- Comparator clock frequency: 100 MHz
- ► SNDR > 28 dB and SFDR > 37 dB
- ► Technology: 150 nm CMOS
- Supply voltage: 1.8 V
- ▶ Input amplitude  $(V_{in})$ :  $0.5 V_{pp}$
- ▶ Input common-mode voltage:  $0 \le V_{\rm in,cm} \le 1.8 \text{ V}$
- ▶ Voltage reference:  $V_{\rm ref} \le 1.8 \ {
  m V}$
- ightharpoonup Switching energy below 30 pJ for  $V_{\rm in}=300\,{\rm mV}$

# Roles and Responsibilities

### Jordi:

- Comparator
- Successive Approximation Register
- Comparator Layout

# Björn:

- Digital-to-Analog Converter
- ► Sample & Hold
- DAC Layout

# Design Flow

We used a top-down design approach:

- 1. System-level design
- 2. Behavioral modeling using Verilog-AMS
- 3. Transistor level modeling
- 4. Layout

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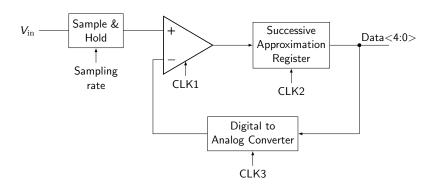
Co-simulations where also used to test individual blocks functionality

# Outline

System-level Design Problem Statement **Proposed Solution** Behavioral Modeling Comparator Digital-to-Analog Converter Successive Approximation Register

**Problem Statement** 

### The basic block diagram of a SAR ADC looks as follows



**Proposed Solution** 

The following topology was used:

- ► Comparator: Strong ARM Latch
  - Reduced power consumption
  - Fast operation
  - Small area

### **Proposed Solution**

### The following topology was used:

- ► Comparator: Strong ARM Latch
  - Reduced power consumption
  - Fast operation
  - Small area
- ► DAC: Charge redistribution weighted capacitors
  - Suitable for CMOS technology
  - Integrates the Sample & Hold

### **Proposed Solution**

### The following topology was used:

- Comparator: Strong ARM Latch
  - Reduced power consumption
  - Fast operation
  - Small area
- ► DAC: Charge redistribution weighted capacitors
  - Suitable for CMOS technology
  - Integrates the Sample & Hold
- SAR: Successive Approximation Register
  - Integrates controls for Sample & Hold
  - Implemented as 7 state FSM
  - Verilog model

### Behavioral Modeling I

### Comparator modeling:

```
always @(posedge CLK) begin
1
        #5
2
        outn = 0; outp = 0;
3
    end
    always @(negedge CLK) begin
5
      if(V(inp) > V(inn)) begin
6
        #50
        outp = 1; outn = 0;
8
      end else begin
9
        #50
10
        outp = 0; outn = 1;
11
12
      end
13
    end
```

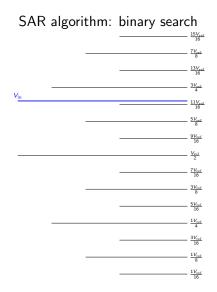
Some delay was added to the behavioral model.

Behavioral Modeling II

### Digital-to-Analog Converter modeling:

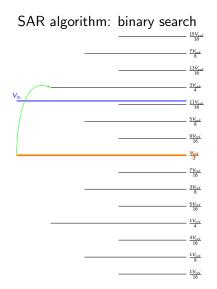
```
analog begin
always @(posedge CLK) begin
for(i=0, i < 5, i++) begin
result += input[5-i] * Vref/(1<<i);
end
V(out) <+ transition(result, 1ns, 0.1ns, 0.1ns)
end
end
end</pre>
```

### Behavioral Modeling III



Assume  $V_{\mathrm{in}} = 0.7\,\mathrm{V},~V_{\mathrm{ref}} = 1\,\mathrm{V}$  and 4 bits

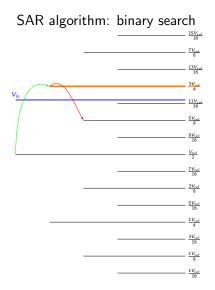
### Behavioral Modeling III



Assume  $V_{
m in} =$  0.7 V,  $V_{
m ref} =$  1 V and 4 bits

1. 
$$V_{\rm in} \stackrel{?}{\geq} \frac{V_{\rm ref}}{2}$$
  $\checkmark$ 

### Behavioral Modeling III

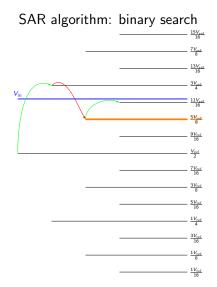


Assume  $V_{
m in}=$  0.7 V,  $V_{
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1. 
$$V_{\rm in} \stackrel{?}{\geq} \frac{V_{\rm ref}}{2} \checkmark$$

2. 
$$V_{\rm in} \stackrel{?}{\geq} \frac{3V_{\rm ref}}{4} X$$

### Behavioral Modeling III



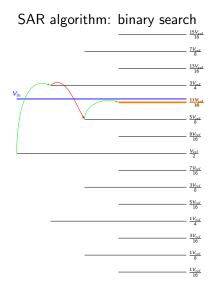
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3. 
$$V_{\rm in} \stackrel{?}{\geq} \frac{5V_{\rm ref}}{8} \checkmark$$

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4. 
$$V_{\rm in} \stackrel{?}{\geq} \frac{11V_{\rm ref}}{16}$$
  $\checkmark$ 

### Behavioral Modeling III

# SAR algorithm: binary search

Assume  $V_{
m in}=$  0.7 V,  $V_{
m ref}=$  1 V and 4 bits

1. 
$$V_{\rm in} \stackrel{?}{\geq} \frac{V_{\rm ref}}{2}$$
  $\checkmark$ 

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$$V_{\rm in} \stackrel{?}{\geq} \frac{11V_{\rm ref}}{16} \checkmark$$

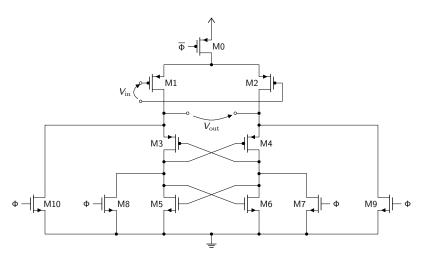
Out = 0b1011 
$$(\frac{11V_{\mathrm{ref}}}{16})$$

# Outline

| Project Description  | Comparator  |
|--|---|
| Roles and Responsibilities   | Digital-to-Analog Converter   |
| Design Flow  | Layout<br>Comparator  |
| System-level Design Problem Statement Proposed Solution Behavioral Modeling Comparator Digital-to-Analog Converter Successive Approximation Register | Digital-to-Analog Converter Simulations Sinusoidal Stimulus Ramp Stimulus Spectrum Figures of Merit Conclusions |
| Transistor-level Design  | References  |

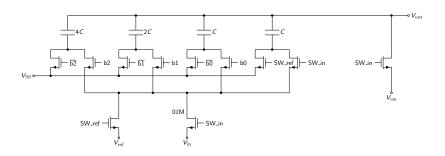
### Comparator

# Strong ARM Latch topology



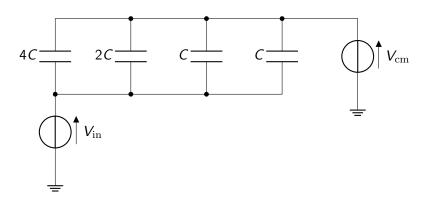
Digital-to-Analog Converter I

# Example with 3 bit



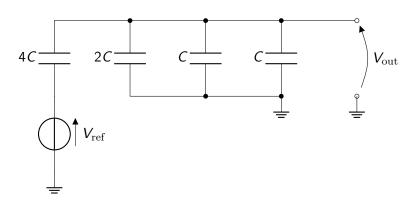
Digital-to-Analog Converter II

# Sample phase:



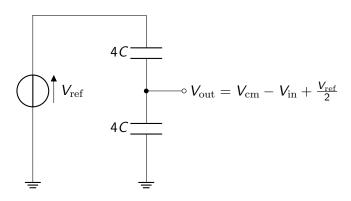
Digital-to-Analog Converter II

Cycling phase:



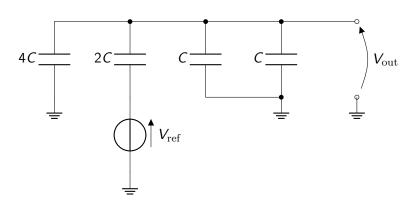
Digital-to-Analog Converter II

# Equivalent circuit:



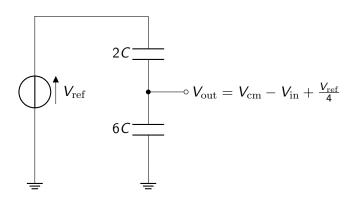
Digital-to-Analog Converter II

Cycling phase:



Digital-to-Analog Converter II

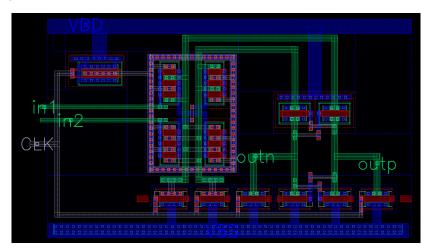
# Equivalent circuit:



# Outline

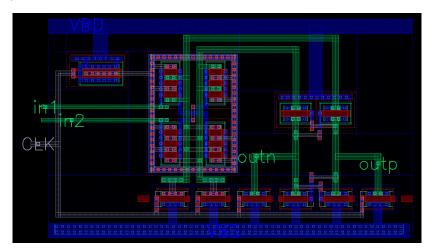
Layout Comparator Digital-to-Analog Converter

### Comparator



 Common centroid for the differential input pair

### Comparator



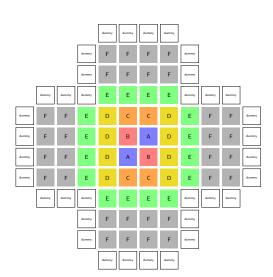
 Common centroid for the differential input pair

 Guard ring around sensitive high impedance nodes

### Digital-to-Analog Converter I

To ensure good matching we used:

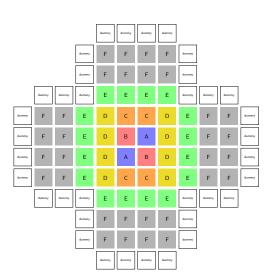
Common centroid technique



### Digital-to-Analog Converter I

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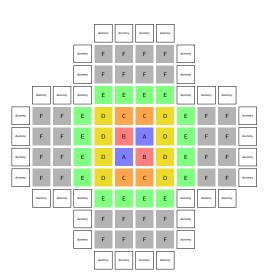
- Common centroid technique
- ► Base unit of half the minmum capacitance



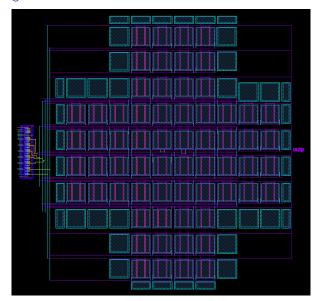
### Digital-to-Analog Converter I

To ensure good matching we used:

- Common centroid technique
- Base unit of half the minmum capacitance
- Dummy capacitors at the edges



Digital-to-Analog Converter II

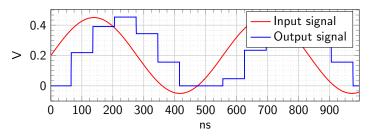


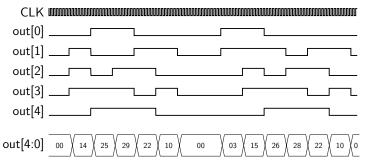
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| Problem Statement  | Digital-to-Analog Converter Simulations       |
| Proposed Solution  | Sinusoidal Stimulus                           |
| Behavioral Modeling  | Ramp Stimulus                                 |
| Comparator<br>Digital-to-Analog Converter                  | Spectrum                                      |
| Successive Approximation                                   | Figures of Merit                              |
| Register   | Conclusions                                   |
| Transistor-level Design                                    | References                                    |

### Simulations I

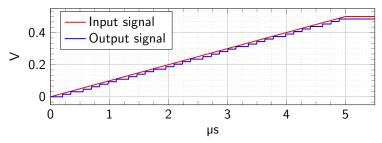
### Sinusoidal Stimulus

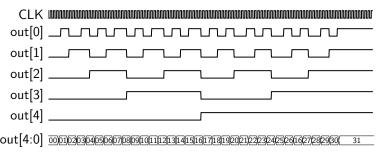




# Simulations II

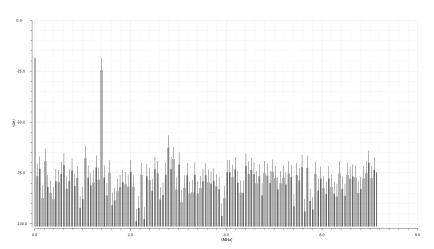
### Ramp Stimulus





# Simulations III

### Spectrum



Input frequency:  $1.3\,\mathrm{MHz}$ 

# Figures of Merit

| Sample rate      | 14.29 MHz          |
|------------------|--------------------|
| Resolution       | 5 bits             |
| Full scale       | 500 mV             |
| $V_{ m ref}$     | 500 mV             |
| $V_{ m cm}$      | 250 mV             |
| $V_{ m LSB}$     | $15.63\mathrm{mV}$ |
| ENOB             | 4.78               |
| SNDR             | 30.55 dB           |
| SFDR             | 38.16 dB           |
| THD              | 1.44%              |
| INL              | $10.22\mathrm{mV}$ |
| DNL              | $8.32\mathrm{mV}$  |
| Energy per cycle | 4.02 pJ            |

We were able to:

► Work on a state-of-the-art ADC topology

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- ► Hands-on experience with charge redistribution circuits

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- Work on a state-of-the-art ADC topology
- Learn behavioral modeling techniques
- Hands-on experience with charge redistribution circuits
- ► Gained knowledge about mixed-signal design and simulations

### References

- A. Rusu, IL2238 & IL2239 Lecture Slides, KTH 2018.
- N. Ivanisevic, P. Chaourani, M. Waqar and D. I. Albertsson, *Course Tutorials*, KTH 2018.
- T.C. Carusone, D. Johns and K. Martin, Analog Integrated Circuit Design, Wiley 2011.
- C. Saint and J. Saing, IC Mask Design: Essential Layout Techniques, McGraw-Hill Professional Engineering 2002.