

# IL2239 - Course Project

## Design of a SAR ADC

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# Outline

Project Description

Roles and Responsibilities

Design Flow

System-level Design

- Problem Statement

- Proposed Solution

- Behavioral Modeling

  - Comparator

  - Digital-to-Analog Converter

  - Successive Approximation

  - Register

Transistor-level Design

Comparator

Digital-to-Analog Converter

Layout

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Digital-to-Analog Converter

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Sinusoidal Stimulus

Ramp Stimulus

Spectrum

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Conclusions

References

# Project Description

Design of a single-ended SAR ADC with the following specifications.

- ▶ Comparator clock frequency: 100 MHz
- ▶ SNDR  $> 28$  dB and SFDR  $> 37$  dB
- ▶ Technology: 150 nm CMOS
- ▶ Supply voltage: 1.8 V
- ▶ Input amplitude ( $V_{in}$ ):  $0.5 V_{pp}$
- ▶ Input common-mode voltage:  $0 \leq V_{in,cm} \leq 1.8$  V
- ▶ Voltage reference:  $V_{ref} \leq 1.8$  V
- ▶ Switching energy below 30 pJ for  $V_{in} = 300$  mV

# Roles and Responsibilities

Jordi:

- ▶ Comparator
- ▶ Successive Approximation Register
- ▶ Comparator Layout

Björn:

- ▶ Digital-to-Analog Converter
- ▶ Sample & Hold
- ▶ DAC Layout

# Design Flow

We used a top-down design approach:

1. System-level design
2. Behavioral modeling using Verilog-AMS
3. Transistor level modeling
4. Layout

# Design Flow

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Co-simulations where also used to test individual blocks functionality

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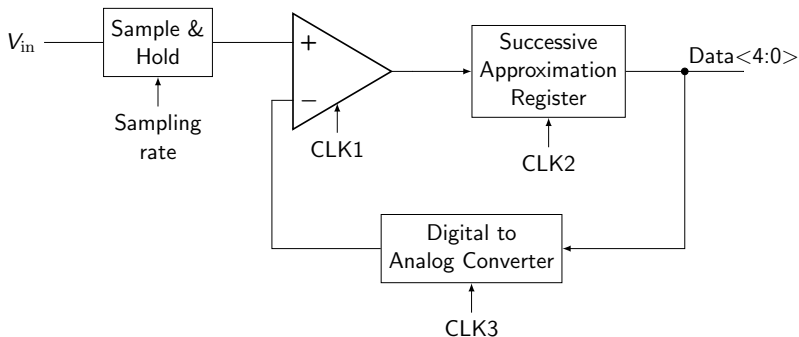
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# System-level Design I

## Problem Statement

The basic block diagram of a SAR ADC looks as follows





# System-level Design II

## Proposed Solution

The following topology was used:

- ▶ Comparator: **Strong ARM Latch**
  - Reduced power consumption
  - Fast operation
  - Small area

# System-level Design II

## Proposed Solution

The following topology was used:

- ▶ Comparator: **Strong ARM Latch**
  - Reduced power consumption
  - Fast operation
  - Small area
- ▶ DAC: **Charge redistribution weighted capacitors**
  - Suitable for CMOS technology
  - Integrates the Sample & Hold

# System-level Design II

## Proposed Solution

The following topology was used:

- ▶ Comparator: **Strong ARM Latch**
  - Reduced power consumption
  - Fast operation
  - Small area
- ▶ DAC: **Charge redistribution weighted capacitors**
  - Suitable for CMOS technology
  - Integrates the Sample & Hold
- ▶ SAR: **Successive Approximation Register**
  - Integrates controls for Sample & Hold
  - Implemented as 7 state FSM
  - Verilog model

# System-level Design III

## Behavioral Modeling I

### Comparator modeling:

---

```
1  always @(posedge CLK) begin
2      #5
3      outn = 0; outp = 0;
4  end
5  always @(negedge CLK) begin
6      if(V(inp) > V(inn)) begin
7          #50
8          outp = 1; outn = 0;
9      end else begin
10         #50
11         outp = 0; outn = 1;
12     end
13 end
```

---

Some delay was added to the behavioral model.

# System-level Design III

## Behavioral Modeling II

### Digital-to-Analog Converter modeling:

---

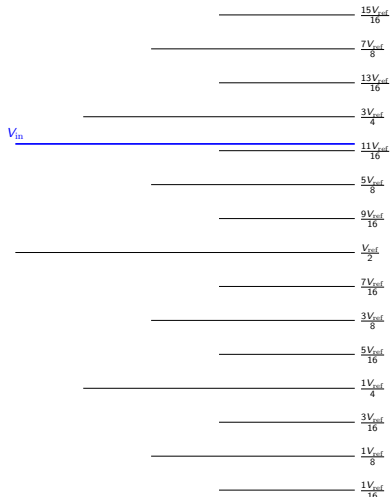
```
1 analog begin
2     always @(posedge CLK) begin
3         for(i=0, i < 5, i++) begin
4             result += input[5-i] * Vref/(1<<i);
5         end
6         V(out) <+ transition(result, 1ns, 0.1ns, 0.1ns)
7     end
8 end
```

---

# System-level Design III

## Behavioral Modeling III

SAR algorithm: binary search

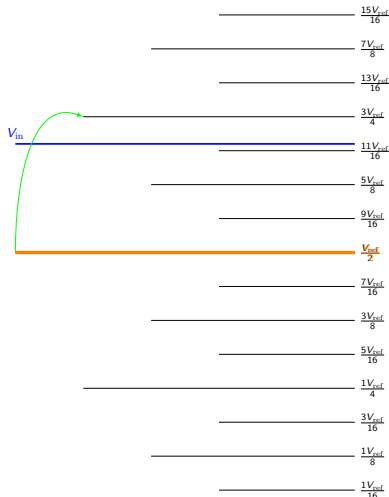


Assume  $V_{in} = 0.7V$ ,  $V_{ref} = 1V$   
and 4 bits

# System-level Design III

## Behavioral Modeling III

SAR algorithm: binary search



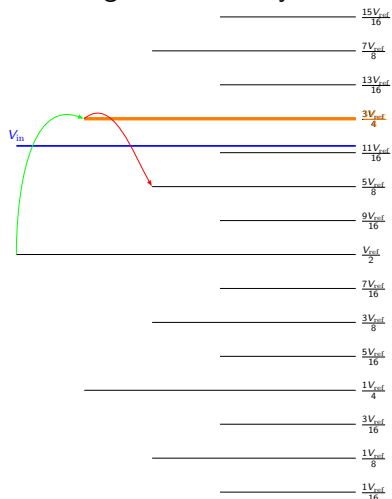
Assume  $V_{in} = 0.7V$ ,  $V_{ref} = 1V$   
and 4 bits

1.  $V_{in} \stackrel{?}{\geq} \frac{V_{ref}}{2}$  ✓

# System-level Design III

## Behavioral Modeling III

SAR algorithm: binary search



Assume  $V_{in} = 0.7V$ ,  $V_{ref} = 1V$   
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1.  $V_{in} \stackrel{?}{\geq} \frac{V_{ref}}{2}$  ✓

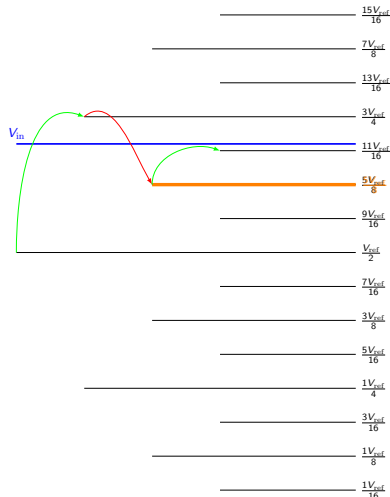
2.  $V_{in} \stackrel{?}{\geq} \frac{3V_{ref}}{4}$  ✗



# System-level Design III

## Behavioral Modeling III

SAR algorithm: binary search



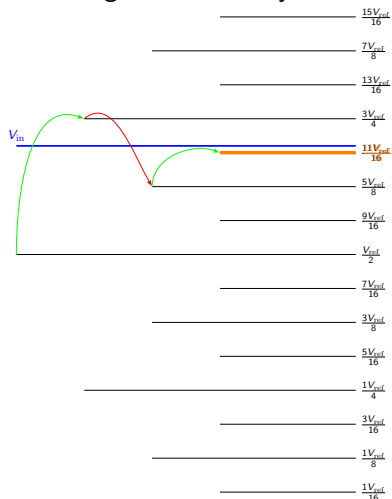
Assume  $V_{in} = 0.7V$ ,  $V_{ref} = 1V$   
and 4 bits

1.  $V_{in} \stackrel{?}{\geq} \frac{V_{ref}}{2}$  ✓
2.  $V_{in} \stackrel{?}{\geq} \frac{3V_{ref}}{4}$  ✗
3.  $V_{in} \stackrel{?}{\geq} \frac{5V_{ref}}{8}$  ✓

# System-level Design III

## Behavioral Modeling III

SAR algorithm: binary search



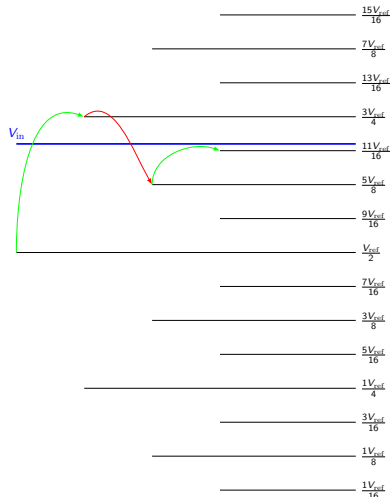
Assume  $V_{in} = 0.7V$ ,  $V_{ref} = 1V$   
and 4 bits

1.  $V_{in} \geq \frac{V_{ref}}{2}$  ✓
2.  $V_{in} \geq \frac{3V_{ref}}{4}$  ✗
3.  $V_{in} \geq \frac{5V_{ref}}{8}$  ✓
4.  $V_{in} \geq \frac{11V_{ref}}{16}$  ✓

# System-level Design III

## Behavioral Modeling III

SAR algorithm: binary search



Assume  $V_{in} = 0.7V$ ,  $V_{ref} = 1V$   
and 4 bits

1.  $V_{in} \geq \frac{V_{ref}}{2}$  ✓
2.  $V_{in} \geq \frac{3V_{ref}}{4}$  ✗
3.  $V_{in} \geq \frac{5V_{ref}}{8}$  ✓
4.  $V_{in} \geq \frac{11V_{ref}}{16}$  ✓

Out = 0b1011 ( $\frac{11V_{ref}}{16}$ )

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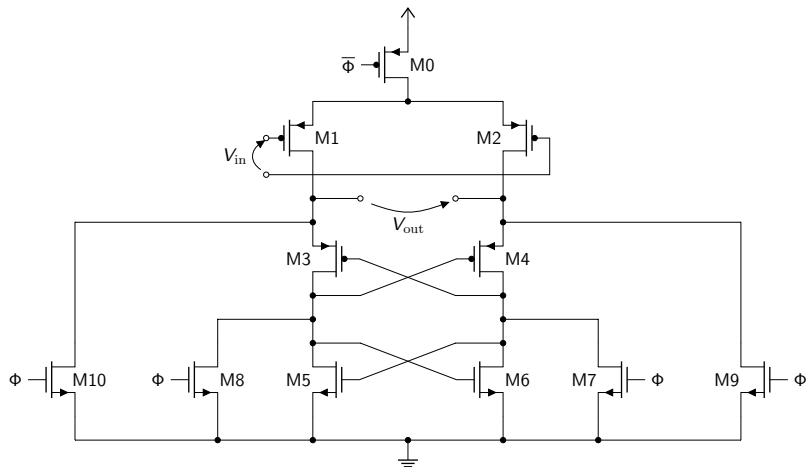
Conclusions

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# Transistor-level Design I

## Comparator

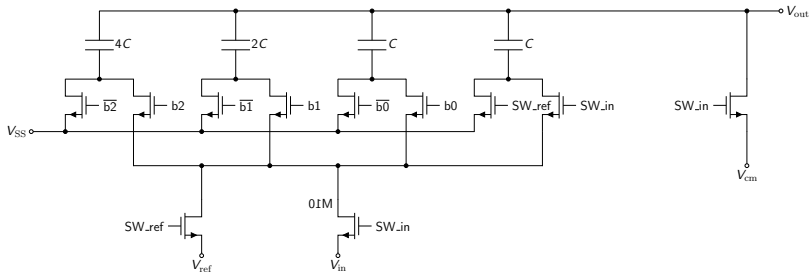
### Strong ARM Latch topology



# Transistor-level Design II

## Digital-to-Analog Converter I

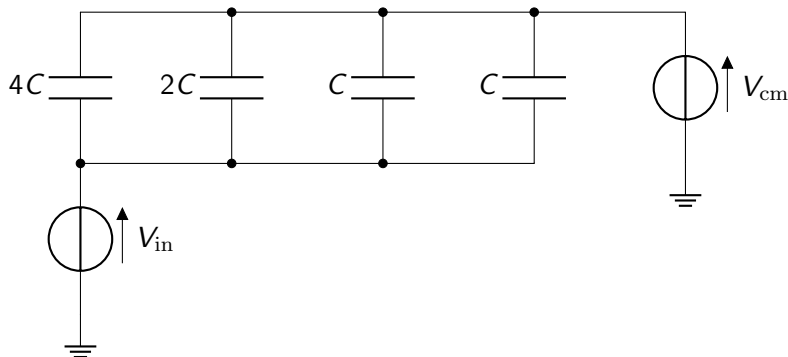
Example with 3 bit



# Transistor-level Design II

## Digital-to-Analog Converter II

Sample phase:

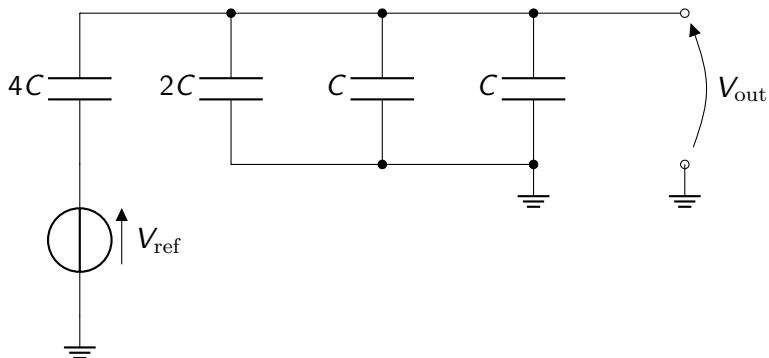


# Transistor-level Design II

## Digital-to-Analog Converter II

Cycling phase:

Input word: 0b100



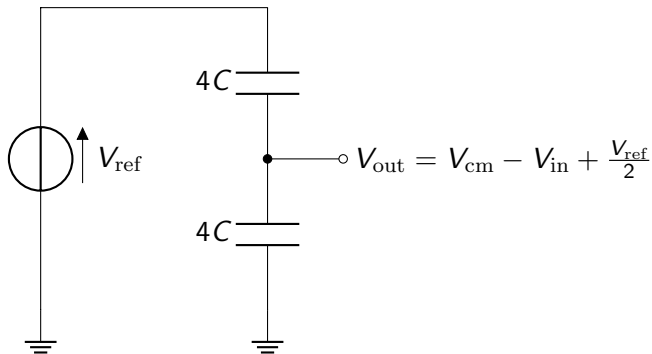


# Transistor-level Design II

## Digital-to-Analog Converter II

Equivalent circuit:

Input word: 0b100

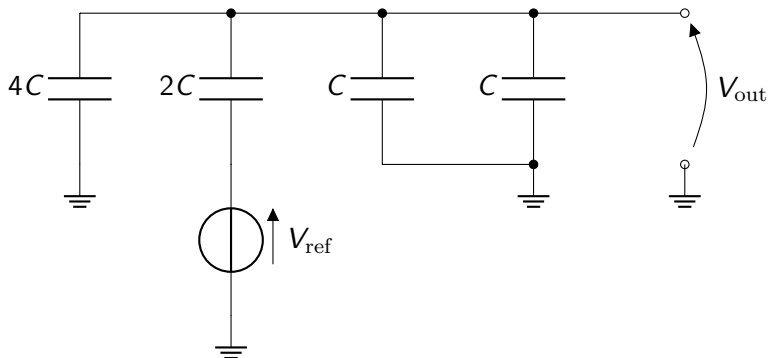


# Transistor-level Design II

## Digital-to-Analog Converter II

Cycling phase:

Input word: 0b010

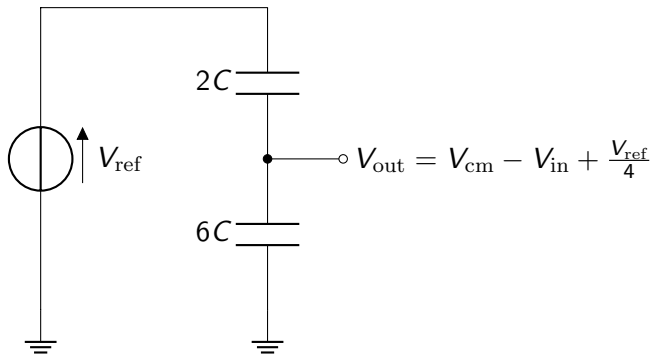


# Transistor-level Design II

## Digital-to-Analog Converter II

Equivalent circuit:

Input word: 0b010



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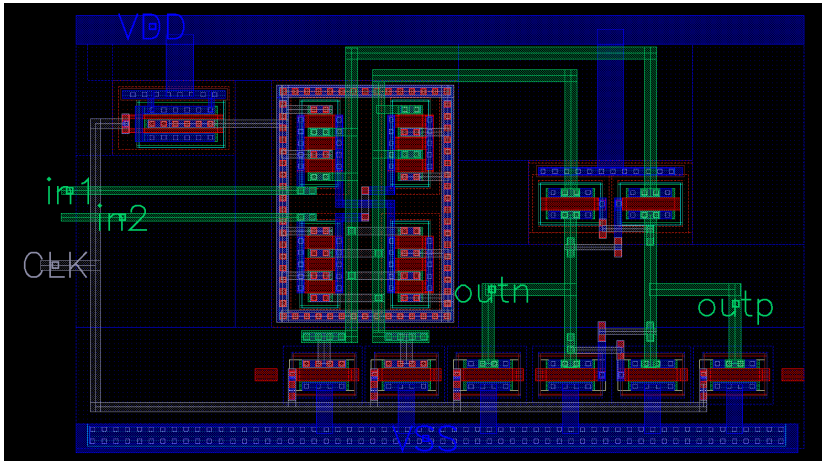
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# Layout I

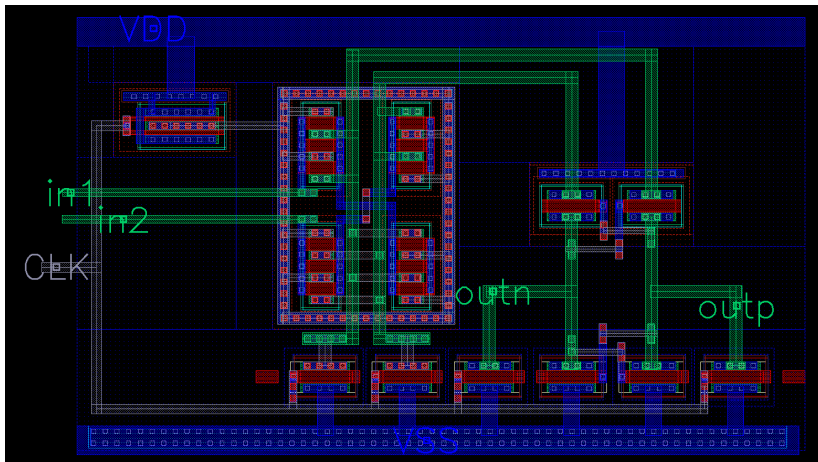
## Comparator



- ▶ Common centroid for the differential input pair

# Layout I

## Comparator



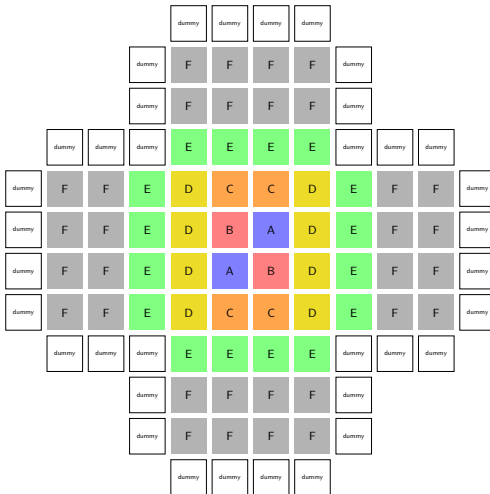
- ▶ Common centroid for the differential input pair
- ▶ Guard ring around sensitive high impedance nodes

# Layout II

## Digital-to-Analog Converter I

To ensure good matching we used:

- ▶ Common centroid technique

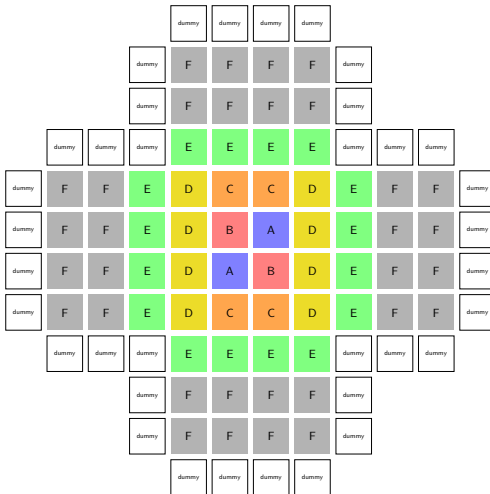


# Layout II

## Digital-to-Analog Converter I

To ensure good matching we used:

- ▶ Common centroid technique
- ▶ Base unit of half the minimum capacitance



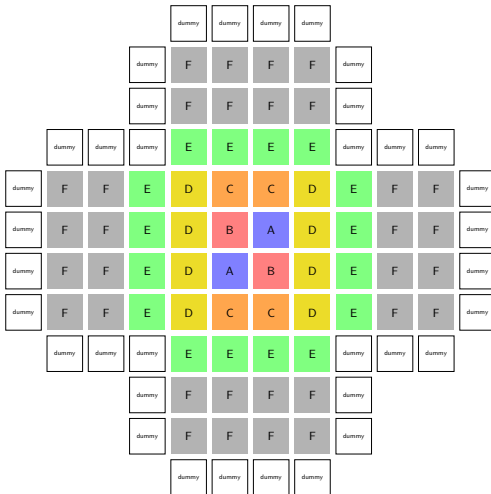


# Layout II

## Digital-to-Analog Converter I

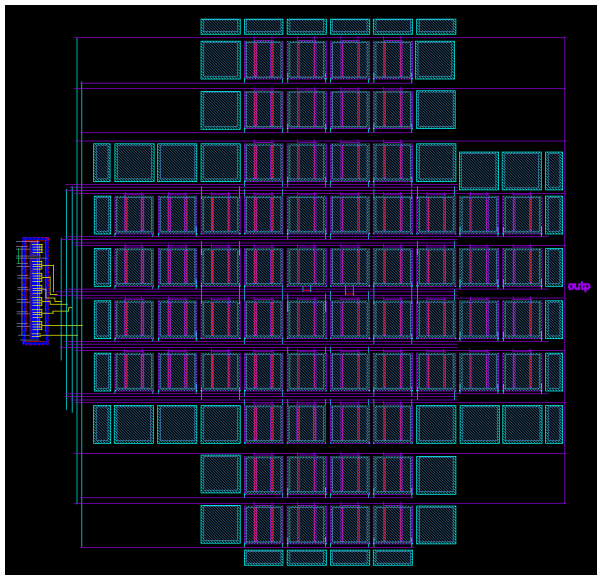
To ensure good matching we used:

- ▶ Common centroid technique
- ▶ Base unit of half the minimum capacitance
- ▶ Dummy capacitors at the edges



# Layout II

## Digital-to-Analog Converter II



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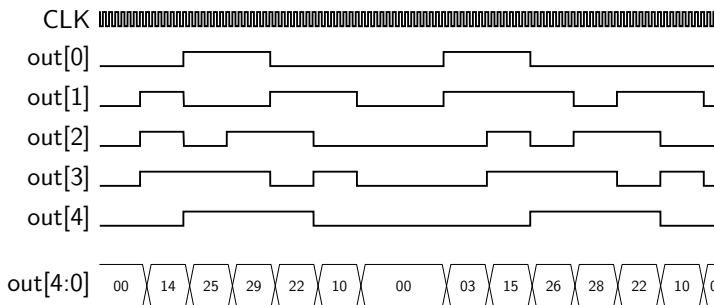
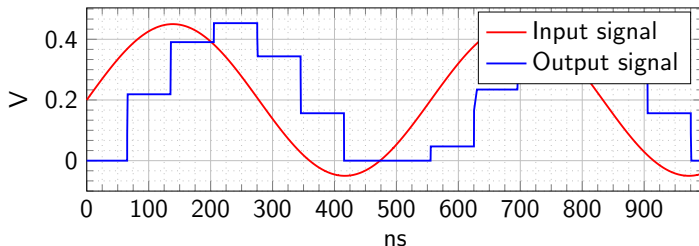
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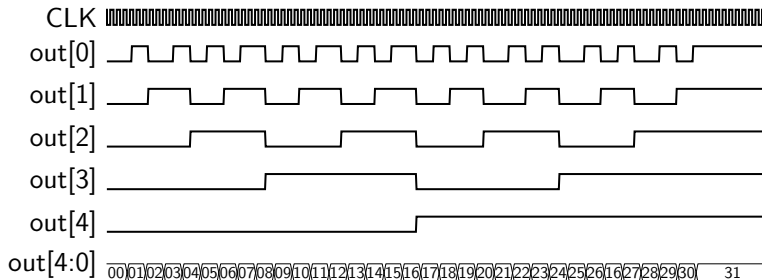
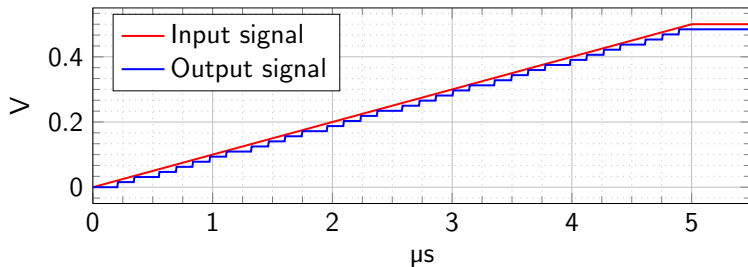
# Simulations I

## Sinusoidal Stimulus



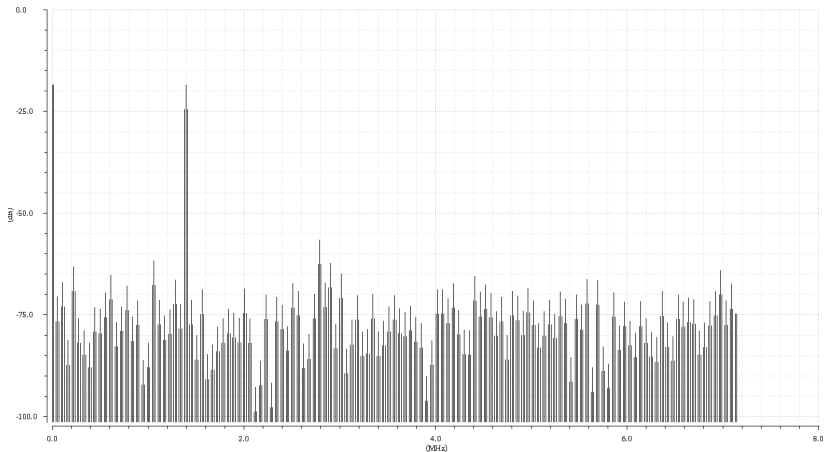
# Simulations II

## Ramp Stimulus



# Simulations III

## Spectrum



Input frequency: 1.3 MHz

# Figures of Merit

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Sample rate	14.29 MHz
ENOB	4.78
SNDR	30.55 dB
SFDR	38.16 dB
THD	1.44 %
Energy per cycle	4.02 pJ

---

# Conclusions

We were able to

- ▶ Work on a state-of-the-art ADC topology



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- ▶ Hands-on experience with charge redistribution circuits

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We were able to

- ▶ Work on a state-of-the-art ADC topology
- ▶ Learn behavioral modeling techniques
- ▶ Hands-on experience with charge redistribution circuits
- ▶ Gained knowledge about mixed-signal design and simulations

