IL2239 - Course Project

Design of a SAR ADC

J. Altayó B. Sunedahl

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Outline

Project Description

Design of a single-ended SAR ADC with the following specifications.

- Comparator clock frequency: 100 MHz
- SNDR $>$ 28 dB and SFDR $>$ 37 dB
- Technology: 150 nm CMOS
- Supply voltage: 1.8 V
- Input amplitude (V_{in}): 0.5 V_{pp}
- Input common-mode voltage: $0 \geq V_{\mathrm{in,cm}} \geq 1.8$ V
- Voltage reference: $V_{\mathrm{ref}} \leq 1.8$ V
- Switghing enegy below 30 pJ for $V_{\mathrm{in}} = 300$ mV

Roles and Responsibilities

Jordi:

- Comparator
- Successive Approximation Register
- Comparator Layout

Björn:

- Digital-to-Analog Converter
- Sample & Hold
- DAC Layout

Design Flow

We used a top-down design approach:

1. System-level design
2. Behavioral moddeling using Verilog-AMS
3. Transistor level mddeling
4. Layout

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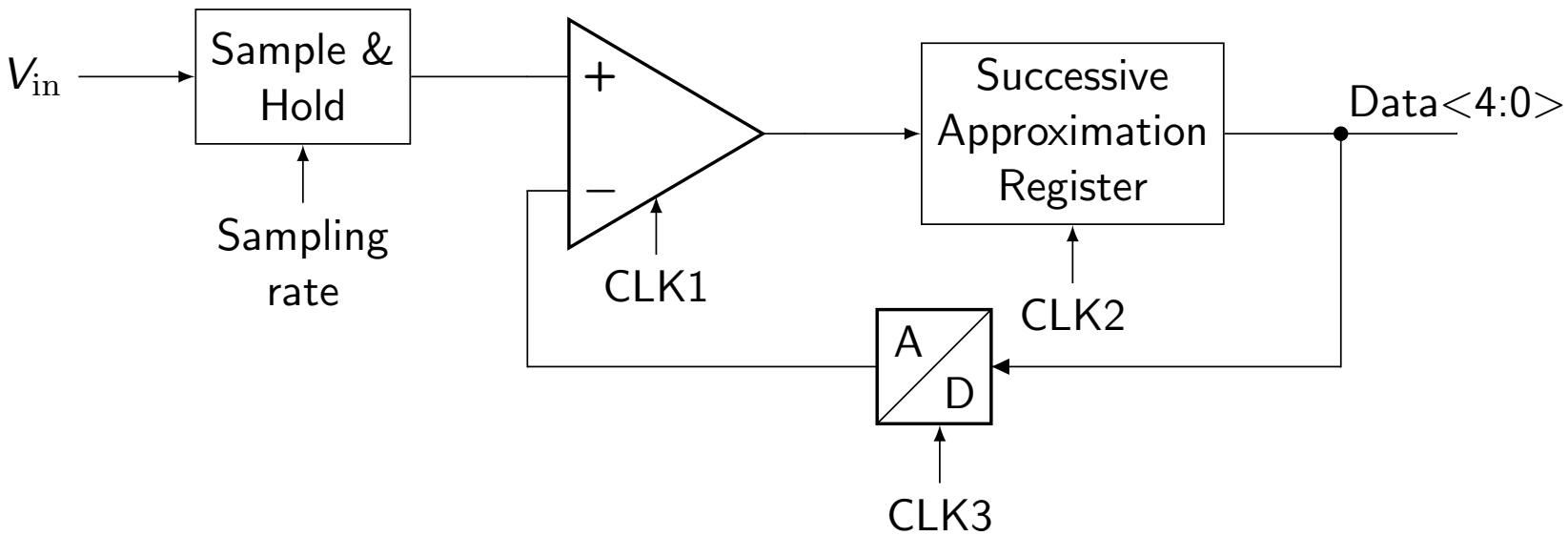
Co-simulations where also used to test individual blocks functionality

System-level Design I

Problem Statement

The basic block diagram of a SAR ADC looks as follows



System-level Design II

Proposed Solution

We choosed to use the following topology:

- Comparator: Strong ARM Latch
  - Reduced power consumption
  - Fast operation
  - Small area

System-level Design II

Proposed Solution

We choosed to use the following topology:

- Comparator: Strong ARM Latch
  - Reduced power consumption
  - Fast operation
  - Small area
- DAC: Charge redistribution weighted capacitors
  - Suitable for CMOS technology
  - Integrates the Sample & Hold

System-level Design III

Verilog-AMS moddeling

Comparator moddeling:

```
1  always @(posedge CLK) begin
2      #5
3      outn = 0; outp = 0;
4  end
5  always @(negedge CLK) begin
6    if(V(inp) > V(inn)) begin
7      #50
8      outp = 1; outn = 0;
9    end else begin
10     #50
11     outp = 0; outn = 1;
12   end
13 end
```

Some delay was added to the behavioral moddel.

System-level Design III

Verilog-AMS moddeling

Digital-to-Analog Converter moddeling:

```
1  analog begin
2    always @(posedge CLK) begin
3      for(i=0, i < 5, i++) begin
4        result += input[5-i] * Vref/5;
5      end
6      V(out) <+ transition(result, 1ns, 0.1ns, 0.1ns)
7    end
8  end
```

System-level Design III

Verilog-AMS moddeling

Layout I

Comparator

- Use `itemizzze` a lot.
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- Use `itemizzze` a lot.
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Layout II

Digital-to-Analog Converter I

To ensure good matching we used:

- Common centroid technique

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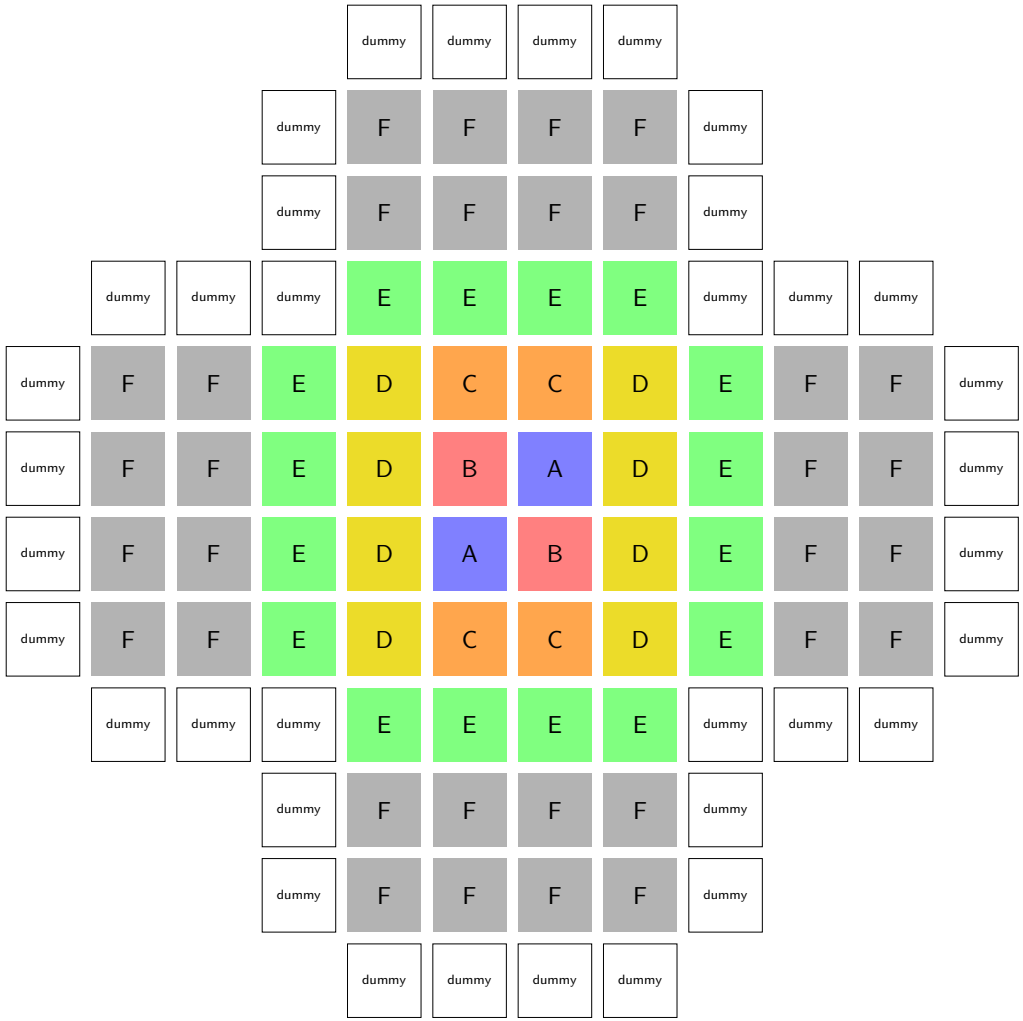
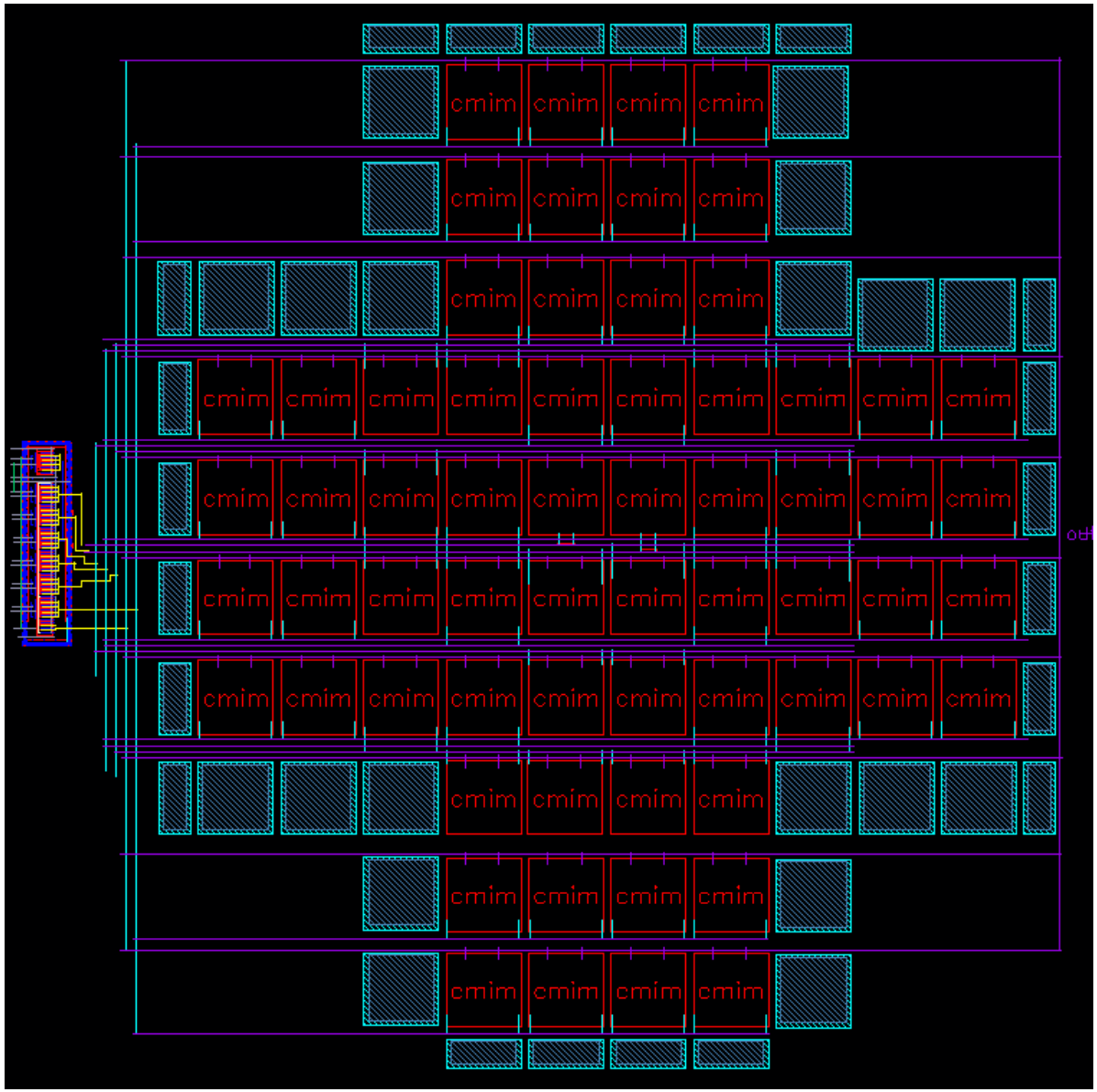


Layout II

Digital-to-Analog Converter II



Figures of Merit

References

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