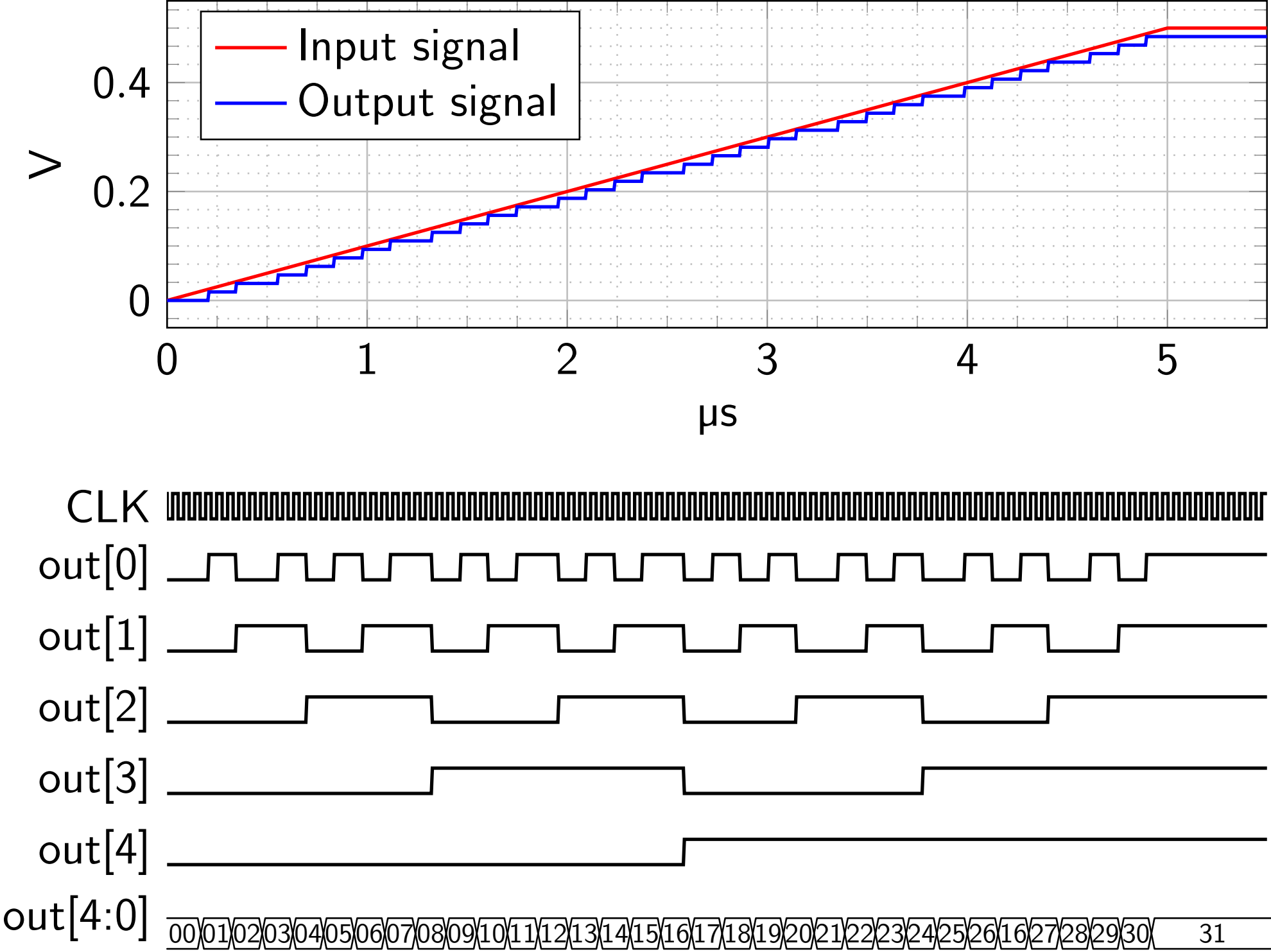
Input signal
Output signal
V
0.4
0.2
0
0
1
2
3
4
5
µs
CLK
out[0]
out[1]
out[2]
out[3]
out[4]
out[4:0]
00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 16 27 28 29 30 31