



Jordi Altayó González

Electrical Engineer

I am a 22-year-old Electrical Engineering student passionate about technology. My career goal is to gain experience in all facets of Engineering and move towards Microelectronic Design. I am also a musician with interests in Art and Philosophy.

Education

- 2012–2014 **High School**, *Sagrada Família*, Sabadell.
Technological modality. See [diploma](#).
- 2014–2018 **Electrical Engineering B.Sc**, *UPC-ETSETB*, Barcelona.
Electronics track. 240 ECTS.
- 2018–2020 **Embedded Systems M.Sc**, *KTH*, Stockholm.
Embedded Electronics track. 120 ECTS
- 2002–2016 **Musical Education**, *Professional Conservatory*, Sabadell.
 - *Main instrument*: viola.
 - *Secondary instruments*: piano and trombone.
 - *Others*: composer and arranger.

Experience

- 2014–2018 **Private teacher**.
Maths, Physics and Electronics teacher for high-school-level students.
- 2015–2018 **Musician**, *Simfònica de Cobla i Corda de Catalunya*, Girona.
Titular violist. Participated in various award-winning CD recordings such as *Tossudament Llach*, *Cançó d'Amor i de Guerra* and *The Very Best*.
- 2015–2018 **Musician**, *Eiron Quintet*, Sabadell.
Founder and member of the group.
- Feb–Jul 2018 **R&D Intern**, *eSilicon*, Barcelona.
Development of a metric analysis tool for ASIC HLBs under PrimeTime and ICC2 environments as part of an internship and the Bachelor's Degree Thesis. This tool will allow designers to have a quick overview on all aspects of the block during the design process without the need to deepen into the design and potentially lose time by analyzing useless or redundant data. It will also provide reports with design changes proposals (ECO) to either facilitate timing closure or reduce power consumption.

Courses, awards and recognitions

- October 2015 **Composition Contest**, *Professional Conservatory*, Sabadell.
Jury award for the piece "Quartet de Tardor". See [diploma](#).
- October 2016 **Innovate or Die[†]**, *LEINN*, Barcelona.
Second place at the challenge of Pyrum®. See [diploma](#).
- October 2016 **Composition Contest**, *Professional Conservatory*, Sabadell.
Jury and public award for the piece "Petit Príncipe". See [diploma](#).

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- November 2016 **EBEC[†]**, *B.E.S.T.*, Barcelona.
Winner of the Regional edition. See [diploma](#).
- April 2017 **EBEC[†]**, *B.E.S.T.*, Valladolid.
Finalist of the National edition. See [diploma](#).
- [†]EBEC stands for European B.E.S.T. (Board of European Students of Technology) Engineering Competition. It is a contest where participants are given 48 hours to solve a challenge by designing and building a functional prototype with the resources provided by the organizers.
- Sept–Dec 2017 **CBI Course**, *UPC & CERN*, Barcelona & Geneva.
Operational methods for radiation inspection project. See [diploma](#).
- March 2018 **Hackathon Mobility**, *SEAT & CARNET*, Barcelona.
First place at SEAT challenge: *AI for Mobility & Driving Experience*. See [prize](#) and [video](#).

Languages

Spanish	Native	
Catalan	Native	
English	C1 (IELTS)	See certificate
French	B2 (DELF)	See certificate

Personal Skills

Programming Languages

- Python
- MATLAB
- C/C++
- Tcl/Tk
- Bash

Hardware Languages

- Verilog
- VHDL
- SystemVerilog
- Verilog A/AMS

Software

- Altium Designer
- PrimeTime
- IC Compiler II
- Design Compiler
- LabVIEW ([CLAD](#))
- L^AT_EX

Soft Skills

- Multidisciplinary team-work capabilities
- Ability to adapt to changes in undergoing projects
- Excellent communication skills
- Ability to analyze and solve complex problems

Others

- Driving license
- Own car

Projects

- December 2015 **Ultrasound distance meter**, *UPC*, Barcelona.
Project developed in a group of 4 engineers. Report can be downloaded [here](#).
- December 2016 **Class D audio amplifier**, *UPC*, Barcelona.
Project developed in a group of 4 engineers. Report can be downloaded [here](#).
- June 2017 **Autonomous weather-related measurement adquisition system**, *UPC*, Barcelona.
Project developed in a group of 2 engineers. Report can be downloaded [here](#).
- December 2017 **CBI Course**, *UPC & CERN*, Barcelona & Geneva.
Project developed in a student team of 2 engineers, 2 designers and 2 MBAs.
Final dossier can be downloaded [here](#).
- June 2018 **Bachelor's Thesis**, *eSilicon & UPC*, Barcelona.
Improving ASIC HLBs Quality of Results Using Design Metrics. See *Experience* for Project details.
- 2018–2020 **KTH Formula Student**, *Stockholm*.
Member of the low-voltage electronics group. See website [here](#).