CMOS VLSI Design

ECE318

Unit6: Dynamic and BiCMOS Logic Circuits

Dynamic Logic Circuit

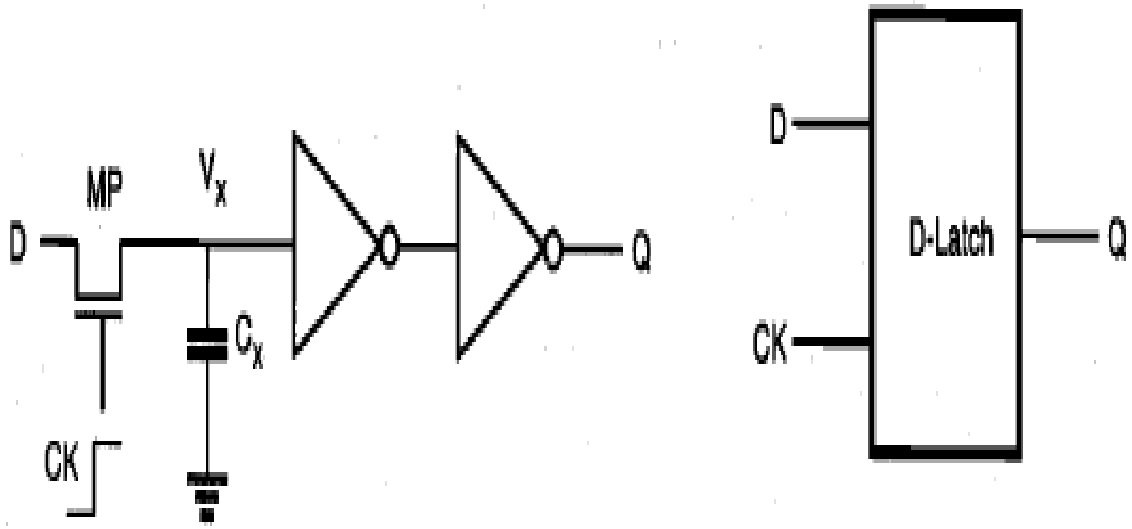
- In high-density, high-performance digital implementations where reduction of circuit delay and silicon area is a major objective, *dynamic logic circuits* offer several significant advantages over static logic circuits.
- The operation of all dynamic logic gates depends on temporary (transient) storage of charge in parasitic node capacitances, instead of relying on steady-state circuit behavior.
- This operational property necessitates periodic updating of internal node voltage levels, since stored charge in a capacitor cannot be retained indefinitely.
- Consequently, dynamic logic circuits require periodic clock signals in order to control charge refreshing.
- The capability of temporarily storing a state, i.e., a voltage level, at a capacitive node allows us to implement very simple
- Sequential circuits with memory functions. Also, the use of common clock signals throughout the system enables us to *synchronize* the operations of various circuit blocks.

Dynamic Logic Circuit

- Finally, the dynamic logic implementation of complex functions generally requires a smaller silicon area than does the static logic implementation.
- As for the power consumption which increases with the parasitic capacitances, the dynamic circuit implementation in a smaller area will, in many cases, consume less power than the static counterpart, despite its use of clock signals.

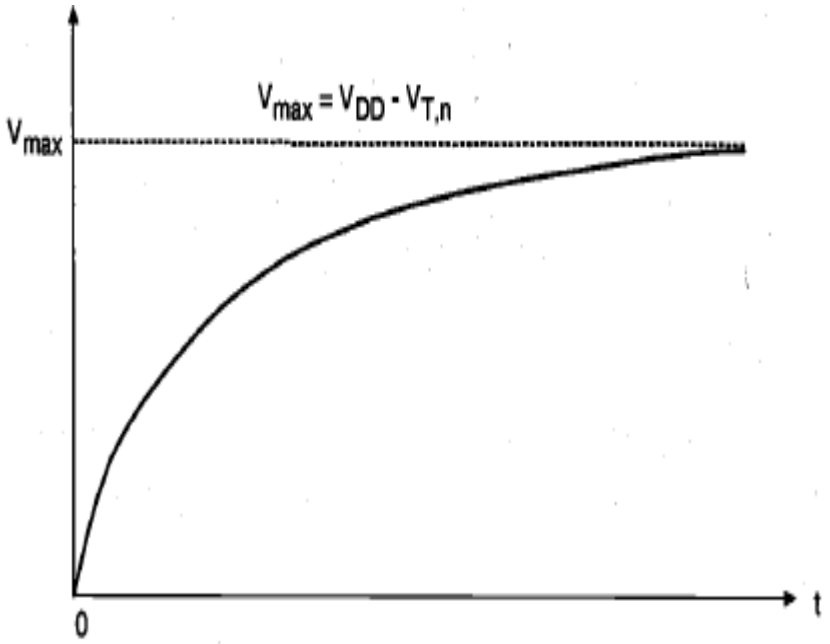
Dynamic D-latch circuit

- Consider the dynamic D-latch circuit shown below. The circuit consists of two cascaded inverters and one nMOS pass transistor driving the input of the primary inverter stage.
- When the clock is high (Clk = 1), the pass transistor turns on. The capacitor *C,* is either charged up, or charged down through the pass transistor MP, depending on the input (D) voltage level. The output (Q) assumes the same logic level as the input.
- When the clock is low (Clk = 0), the pass transistor MP turns off, and the capacitor C is isolated from the input D. Since there is no current path from the intermediate node x to either V_{DD} or ground, the amount of charge stored in C during the previous cycle determines the output voltage level Q

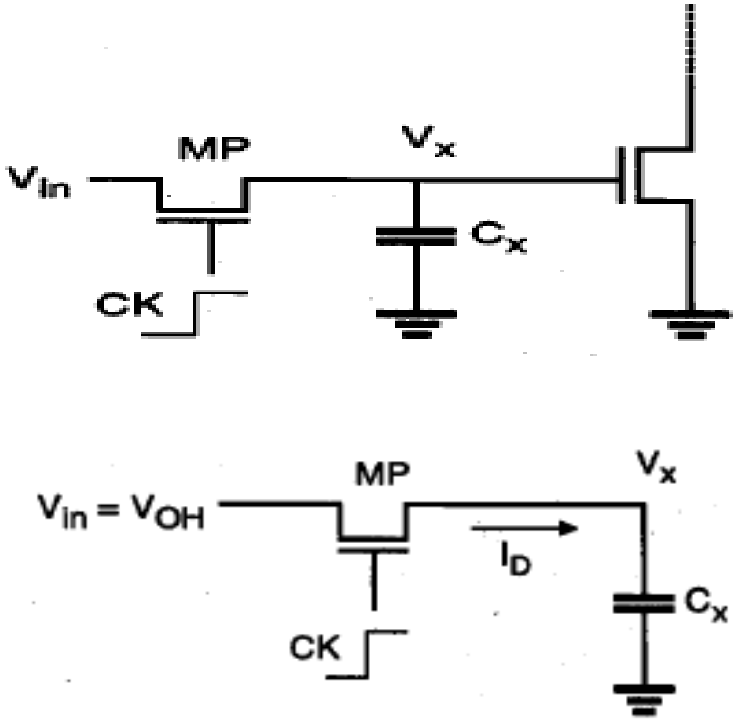


Basic Principles of Pass Transistor Circuits

- ***Logic "1" Transfer***



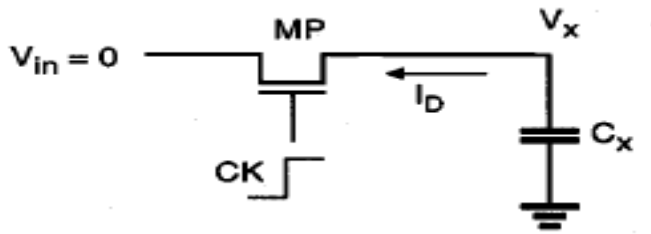
Variation of V as a function of time during logic "I" transfer



Equivalent circuit for the logic " 1 " transfer event

Logic “0" Transfer

- logic “0" level is applied to the input terminal, which corresponds to V_{in} = 0 V. Now, the clock signal at the gate of the pass transistor goes from 0 to *VDD* at t = 0.
- The pass transistor MP starts to conduct as soon as the clock signal becomes active, and the direction of drain current flow through MP will be opposite to that during the charge-up (logic “1 “ transfer) event
- With $V_{GS} = V_{DD}$ and $V_{DS} = V_{max}$, it can be seen that the pass transistor operates in the linear region throughout this cycle, since $V_{DS} < V_{GS} - V_{Tn}$.



Equivalent circuit for the logic "0" transfer event.

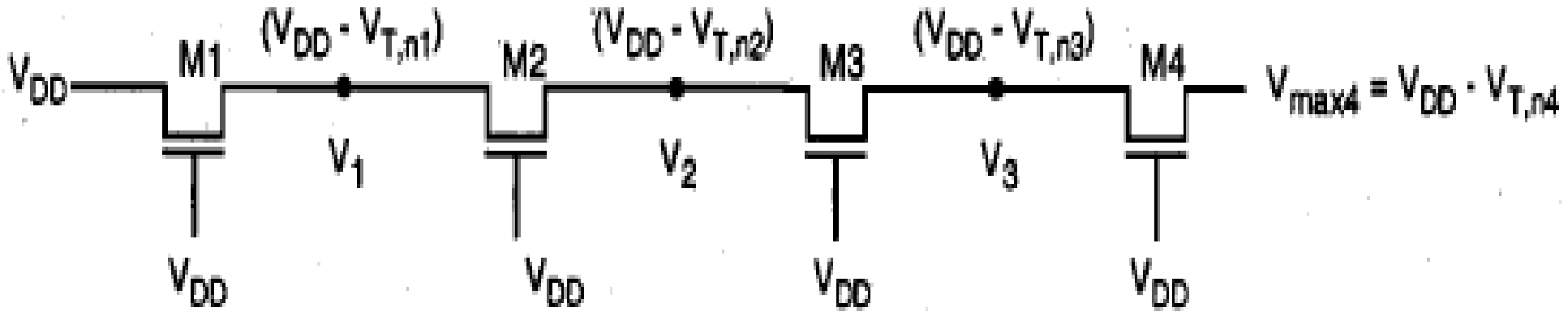
MCQ

- The major drawback of pass transistor logic is

a) Higher delay
b) Higher IC area
c) Imperfect logic level
d) All of the above

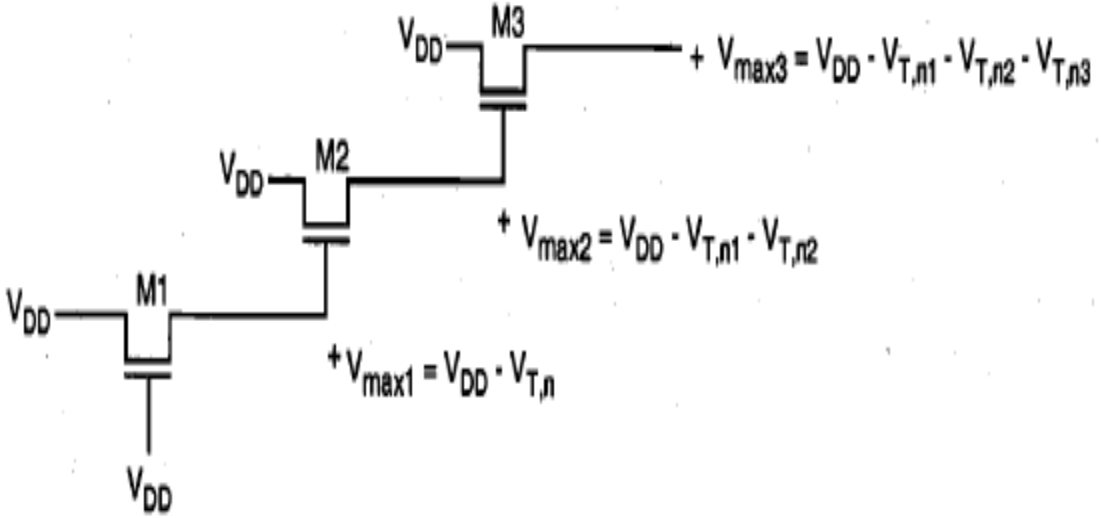
Pass Transistor in cascade : Node voltages in a pass-transistor

- Node voltages in a pass-transistor chain during the logic " 1 " transfer.
- For simple analysis, we assume that initially all internal node voltages,V1, through *V4,* are zero. The first pass transistor Ml operates in saturation with $V_{DS1} > V_{GSI} - V_{Tn1}$.
- Therefore, the voltage at node 1 cannot limit value Vmax1 = $\boldsymbol{(V_{DD} - V_{Tn1})}$
- Now, assuming that the pass transistors in this circuit are identical, the second pass transistor M2 operates at the *saturation boundary.*
- As a result, the voltage at node 2 will be equal to $Vmax2 = (V_{DD} - \boldsymbol{V_{Tn2}})$**.** It can easily be seen that with $V_{Tn1} = V_{Tn2} = V_{Tn3} \ldots$,
- Node voltage at the end of the pass transistor will become one threshold voltage lower than *VDD,* regardless of the number of pass transistors in the chain.
- It can be observed that the steady-state internal node voltages in this circuit are always one threshold voltage below *VDD,* regardless of the initial voltages.



Pass transistor is driving another pass transistor

- This voltage drives the gate of the second pass transistor, which also operates in the saturation region. Its gate-to-source voltage cannot exceed *VTf,2,* hence, the upper
- limit for V_2 is found as $V_{max2} = VDD - V_{Tn1} - V_{Tn2}$.
- It can be seen that in this case, each stage causes a significant loss of voltage level.
- The amount of voltage drop at each stage can be approximated more realistically by taking into account the corresponding substrate bias effect, which is different in all stages.



$$V_{T,n1} = V_{T0,n} - \gamma\left(\sqrt{|2\phi_F| + V_{max1}} - \sqrt{|2\phi_F|}\right)$$

$$V_{T,n2} = V_{T0,n} - \gamma\left(\sqrt{|2\phi_F| + V_{max2}} - \sqrt{|2\phi_F|}\right)$$

Charge Storage and Charge Leakage

- Preservation of a correct logic level at the soft node during the inactive clock phase depends on preserving sufficient amount of charge in C_x , despite the leakage currents.
- We will assume that a logic-high voltage level has been transferred to the soft node during the active clock phase and that now both the input voltage Vin and the **clock** are equal to 0 V.
- The charge stored in ***Cx*** will gradually leak away, primarily due to the leakage currents associated with the pass transistor.
- The gate current of the inverter driver transistor is negligible for all practical purposes.
- $I_{leakage} = I_{subthreshold(MP)} + I_{reverse(MP)}$

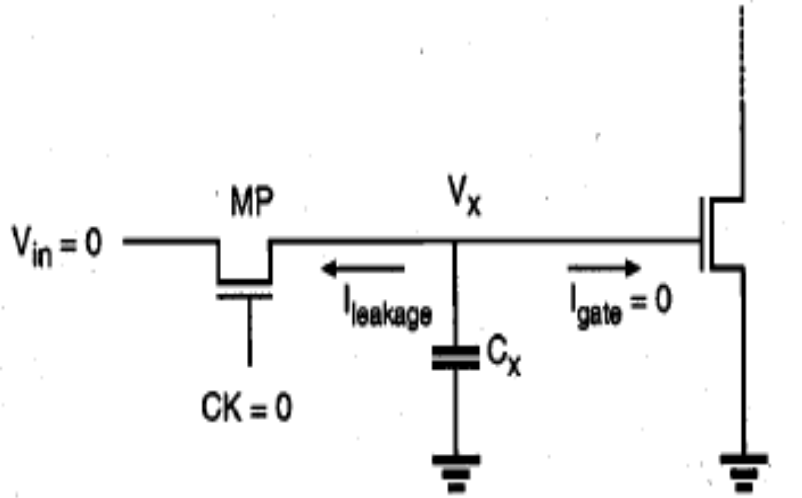


Fig: Charge leakage from the soft node

Synchronous Dynamic Circuit Techniques

- Synchronous dynamic circuits implemented using depletion-load nMOS, enhancement-load nMOS, and CMOS building blocks are need to be discussed.
- **Multi-stage pass transistor logic driven by two nonoverlapping clocks**:
- All inputs of each combinational logic block are driven by a single clock signal.
- Individual input capacitances are not shown in this figure for simplicity, but the operation of the circuit obviously depends on temporary charge storage in the parasitic input capacitances
- To drive the pass transistors in this system, two nonoverlapping clock signals, $\phi 1$ and $\phi 2$, are used.
- The nonoverlapping property of the two clock signals guarantees that at any given time point, only one of the two clock signals can be active,

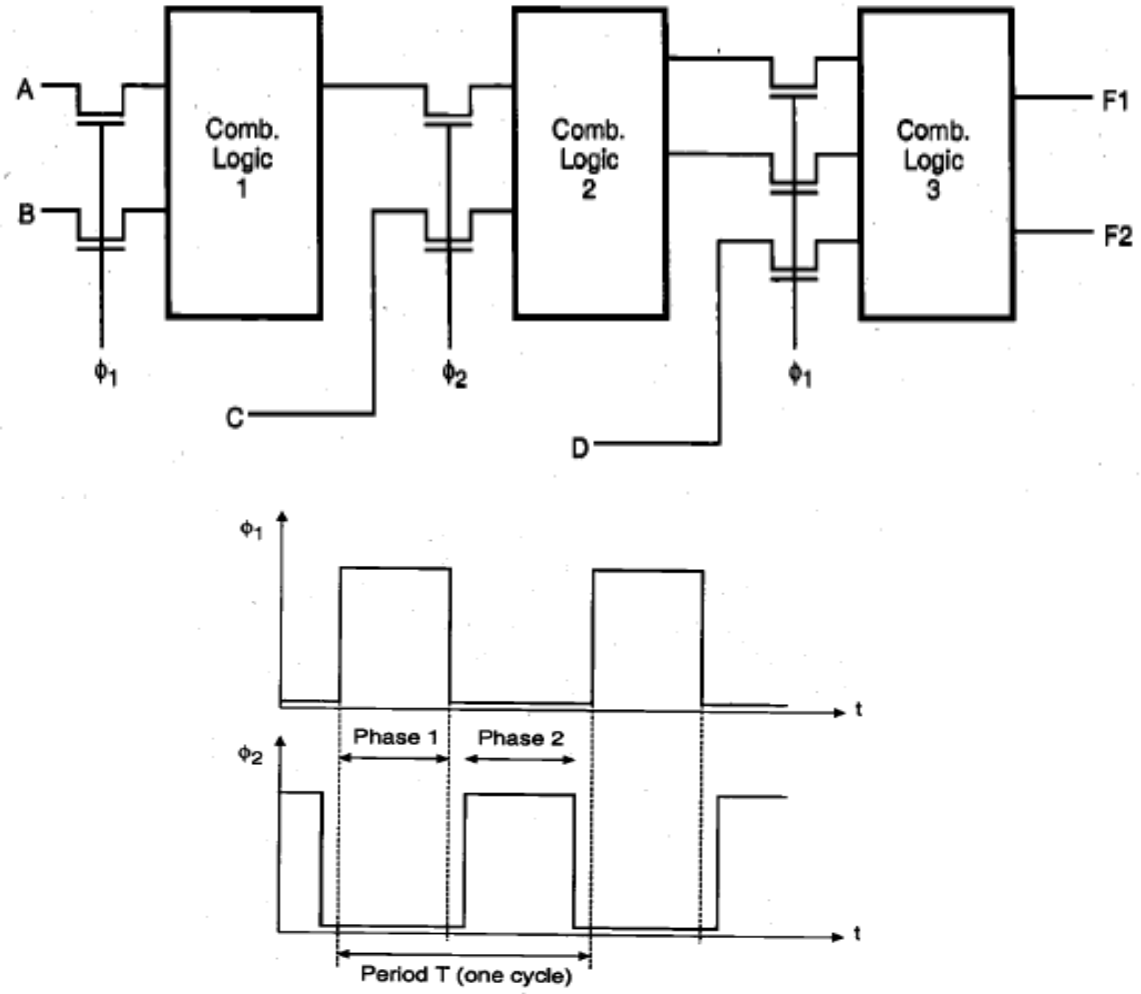


Fig: Nonoverlapping clock signals used for two-phase synchronous operation.

Contd.

- When clock $\phi 1$, is active, the input levels of Stage 1 (and also of Stage 3) are applied through the pass transistors, while the input capacitances of Stage 2 retain their previously set logic levels.
- During the next phase, when clock $\phi 2$ is active, the input levels of Stage 2 will be applied through the pass transistors, while the input capacitances of Stage 1 and Stage 3 retain their logic levels.
- This allows us to incorporate the simple dynamic memory function at each stage input, and at the same time, to facilitate synchronous operation by controlling the signal flow in the circuit using the two periodic clock signals.
- This signal timing scheme is also called *two-phase clocking* and is one of the most widely used timing strategies.
- By introducing the two-phase clocking scheme, no specific assumptions have been made about the internal structure of the combinational logic stages.
- It will be seen that depletion-load nMOS, enhancement-load nMOS, or CMOS logic circuits can be used for implementing the combinational logic.

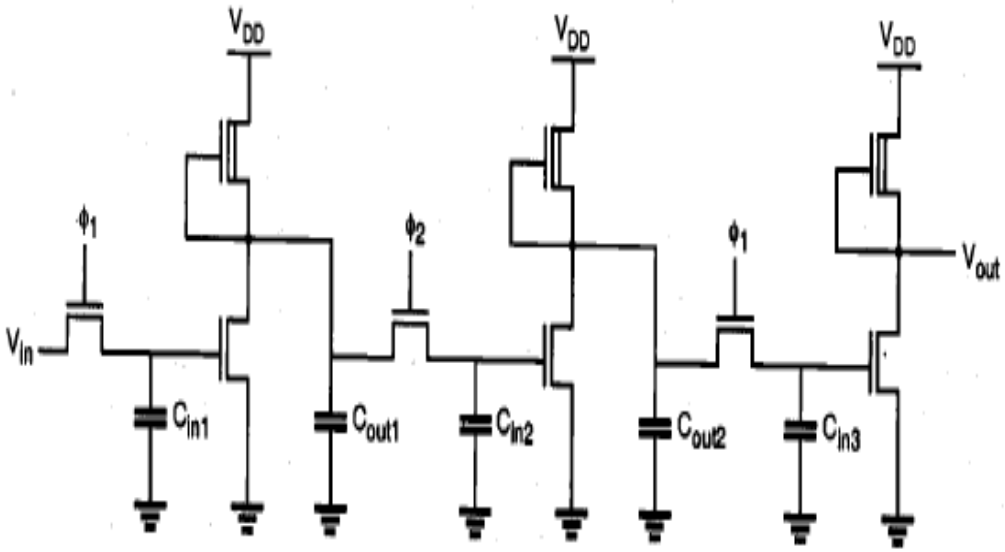
MCQ

- Non overlapping clock $\phi 1$ & $\phi 2$ are

a) 90 degree out of phase
b) 180 degree out of phase
c) 360 degree out of phase
d) None of the above

Example of synchronous dynamic circuit

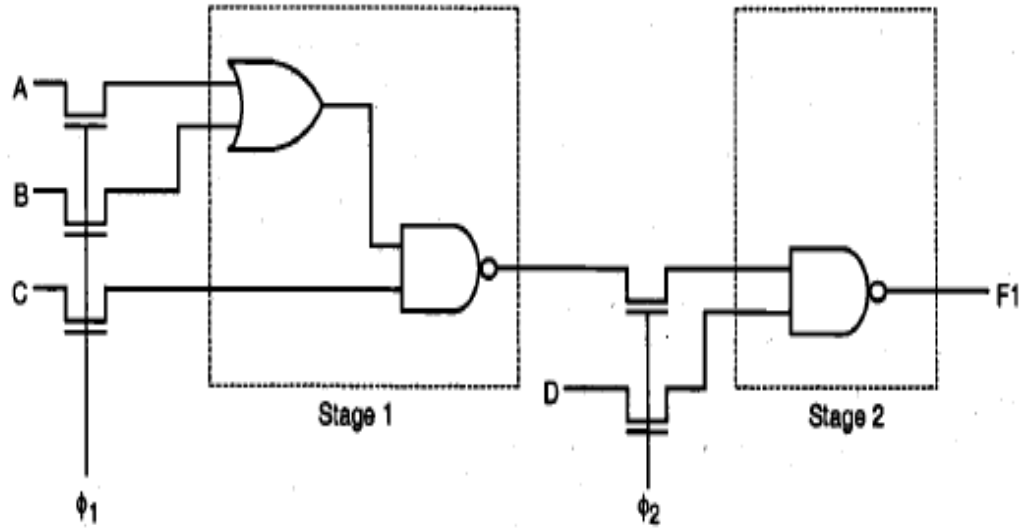
- Three stages of a depletion-load nMOS dynamic shift register circuit driven with two-phase clocking.
- During the active phase of ϕ1 the input voltage level Vin is transferred into the input capacitance Cin1.
- Thus, the valid output voltage level of the first stage is determined as the inverse of the current input during this cycle.
- When ϕ2 becomes active during the next phase, the output voltage level of the first stage is transferred into the second stage input capacitance *Cin2,* and the valid output voltage level of the second stage is determined.
- During the active ϕ2 phase, the first-stage input capacitance continues to retain its previous level via charge storage.
- When ϕ1 becomes active again, the original data bit *written* into the register during the previous cycle is transferred into the third stage, and the first stage can now accept the next data bit.



dynamic shift register

Example of synchronous dynamic circuit

- **A two-stage synchronous complex logic circuit example**
- The same operation principle used in the simple shift register circuit can easily be extended to synchronous complex logic



CMOS Transmission Gate Logic: Dynamic circuit

- The basic two-phase synchronous logic circuit principle, in which individual logic blocks are cascaded via clock-controlled switches, can easily be adopted to CMOS structures as well.
- As a result, two-phase clocking in CMOS transmission gate logic requires that a total of four clock signals are generated and routed throughout the circuit.
- As in the nMOS-based dynamic circuit structures, the operation of CMOS dynamic logic relies on charge storage in the parasitic input capacitances during the inactive clock cycles.
- Dynamic CMOS transmission gate shift register is shown in Fig. b

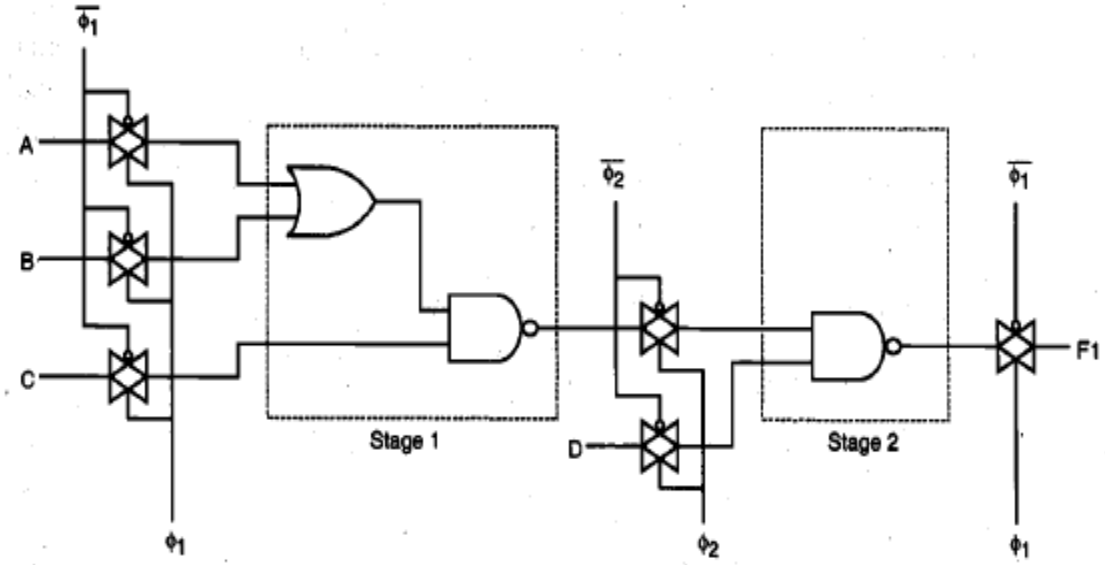


Fig.a: Typical example of dynamic CMOS transmission gate logic

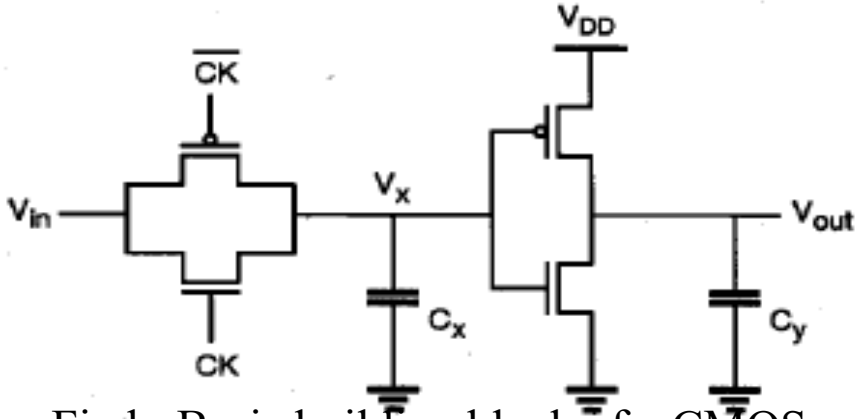
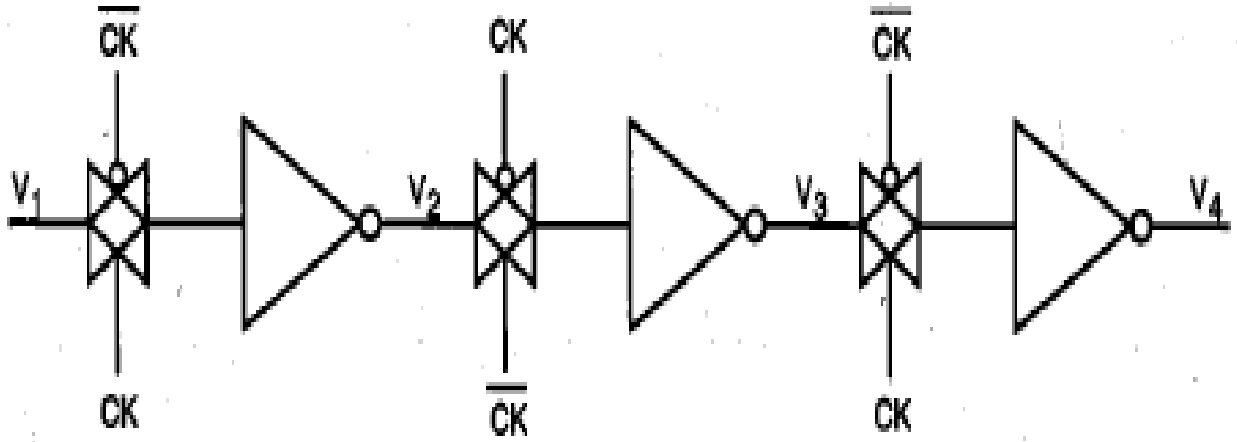


Fig.b: Basic building block of a CMOS transmission gate dynamic shift register

Single-phase CMOS transmission gate dynamic shift register.

- A single-phase CMOS shift register, which is built by cascading identical units as in Fig. 9.24 and by driving each stage alternately with the clock signal and its complement.



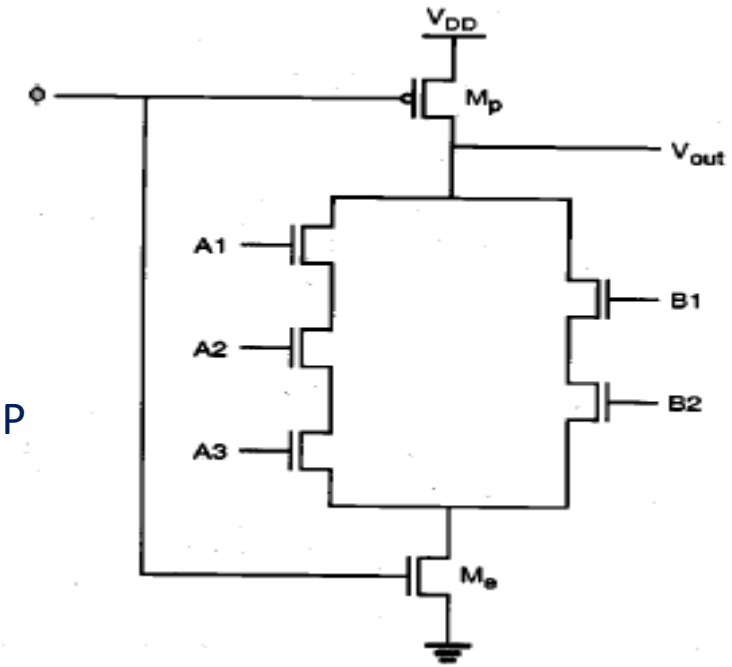
Dynamic CMOS Logic (Precharge-Evaluate Logic)

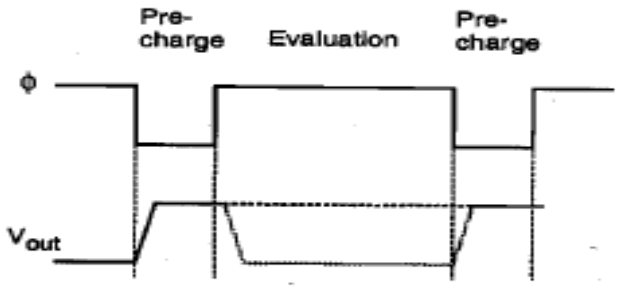
- A dynamic CMOS circuit technique which allows us to significantly reduce the number of transistors used to implement any logic function.
- The circuit operation is based on first *precharging* the output node capacitance and subsequently, *evaluating* the output level according to the applied inputs.
- Both of these operations are scheduled by a single clock signal, which drives one nMOS and one pMOS transistor in each dynamic stage.

Fig.: Dynamic CMOS logic gate implementing a complex Boolean function

F=(A1A2A3+B1B2)'

- When the clock signal is low (precharge phase), the pMOS precharge transistor MP is conducting, while the complementary nMOS transistor Me is off





Q. Design the given function using a) Dynamic CMOS Logic, b) CMOS logic, c) Pseudo NMOS logic d) Pass transistor logic e) CMOS Transmission Gate logic **F=ABC+A'D**

MCQ

Q. In precharge mode of dynamic circuit, the output node charges upto

A) Vdd

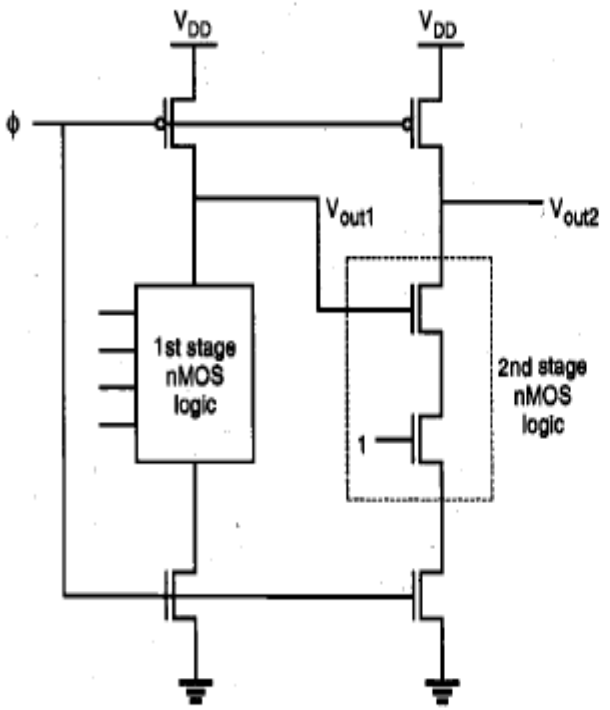
B) Vdd/2

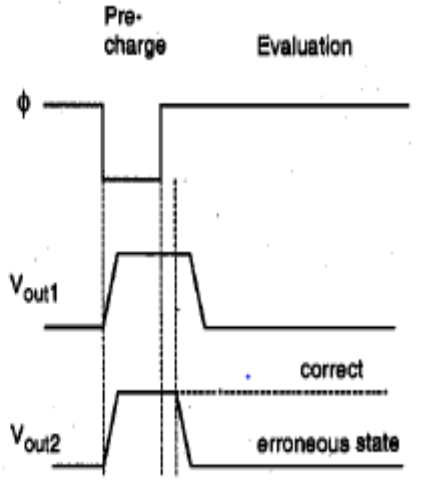
c) Vdd-Vtn

d) 0

Illustration of the cascading problem in dynamic CMOS logic

- The operation of the single-stage dynamic CMOS logic gate is quite straightforward.
- For practical multi-stage applications, however, the dynamic CMOS gate presents a significant problem.
- During the precharge phase, both output voltages Vou and *Vout2* are pulled up by the respective pMOS precharge devices.
- Also, the external inputs are applied during this phase.
- The input variables of the first stage are assumed to be such that the output Vout1 will drop to logic "0" during the evaluation phase.
- On the other hand, the external input of the second-stage NAND2 gate is assumed to be a logic "1"

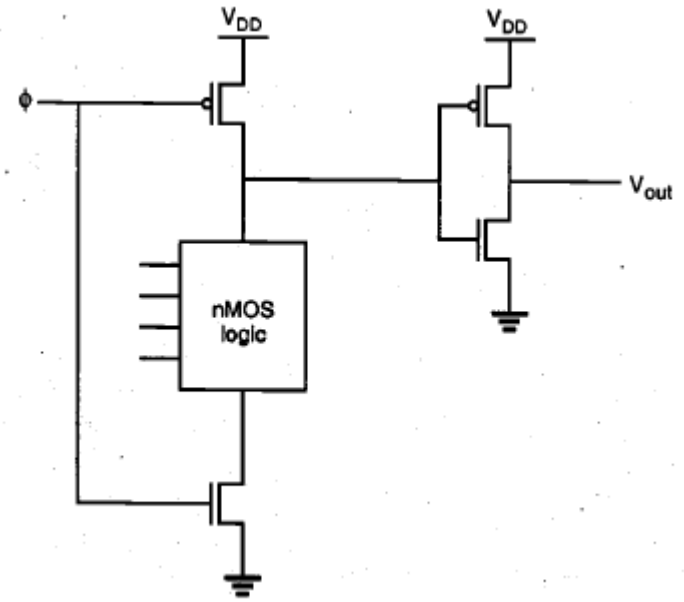




- When the evaluation phase begins, both output voltages Vout1 and Vout2 are logic-high.
- The output of the first stage (Vout1) eventually drops to its correct logic level after a certain time delay.
- However, since the evaluation in the second stage is done concurrently, starting with the high value of Vout1 at the beginning of the evaluation phase, the output voltage *Vout2* at the end of the evaluation phase will be *erroneously* low.

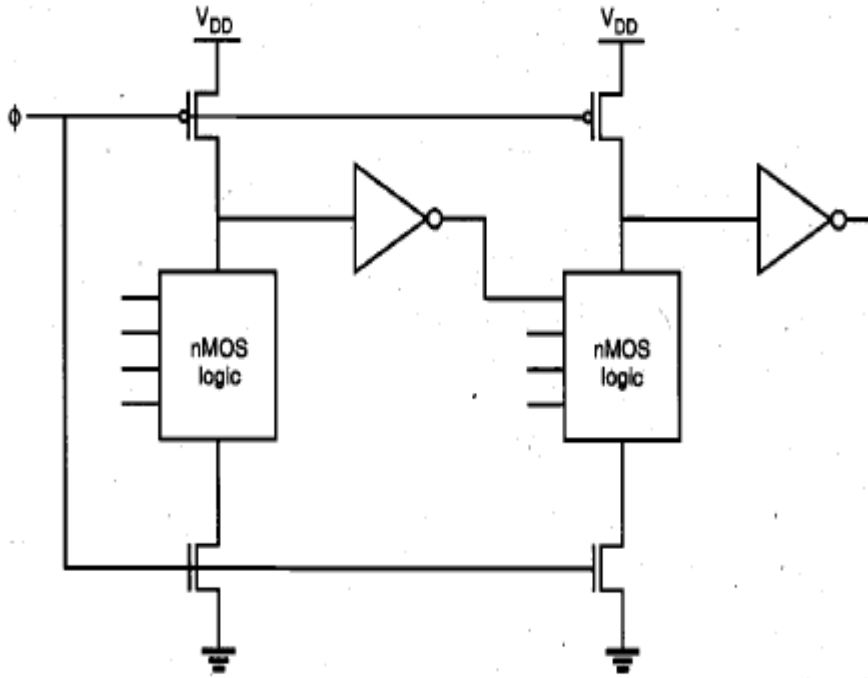
High Performance dynamic circuit

- We will see that they are designed to take full advantage of the obvious benefits of dynamic operation and at the same time, to allow unrestricted cascading of multiple stages.
- The ultimate goal is to achieve reliable, high-speed, compact circuits using the least complicated clocking scheme possible.
- ***Domino CMOS Logic***



Cascaded domino CMOS logic gates.

- Remember that the problem in cascading conventional dynamic CMOS stages occurs when one or more inputs of a stage make a 1 to 0 transition *during* the evaluation phase.
- On the other hand, if we build a system by cascading domino CMOS logic gates as shown in Fig., all input transistors in subsequent logic blocks will be turned off during the precharge phase, since all buffer outputs are equal to 0.
- During the evaluation phase, each buffer output can make at most one transition (from 0 to 1), and thus each input of all subsequent logic stages can also make at most one (0 to 1) transition.
- In a cascade structure consisting of several such stages, the evaluation of each stage ripples the next stage evaluation, similar to a chain of dominos falling one after the other.
- The structure is hence called *domino CMOS logic.*

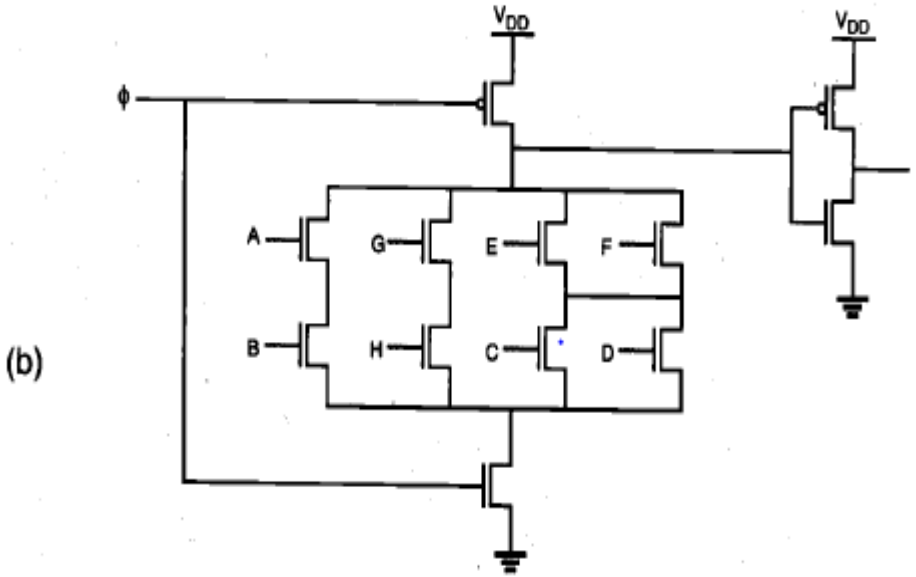


Cascaded domino CMOS logic gates.

Example Domino logic circuit

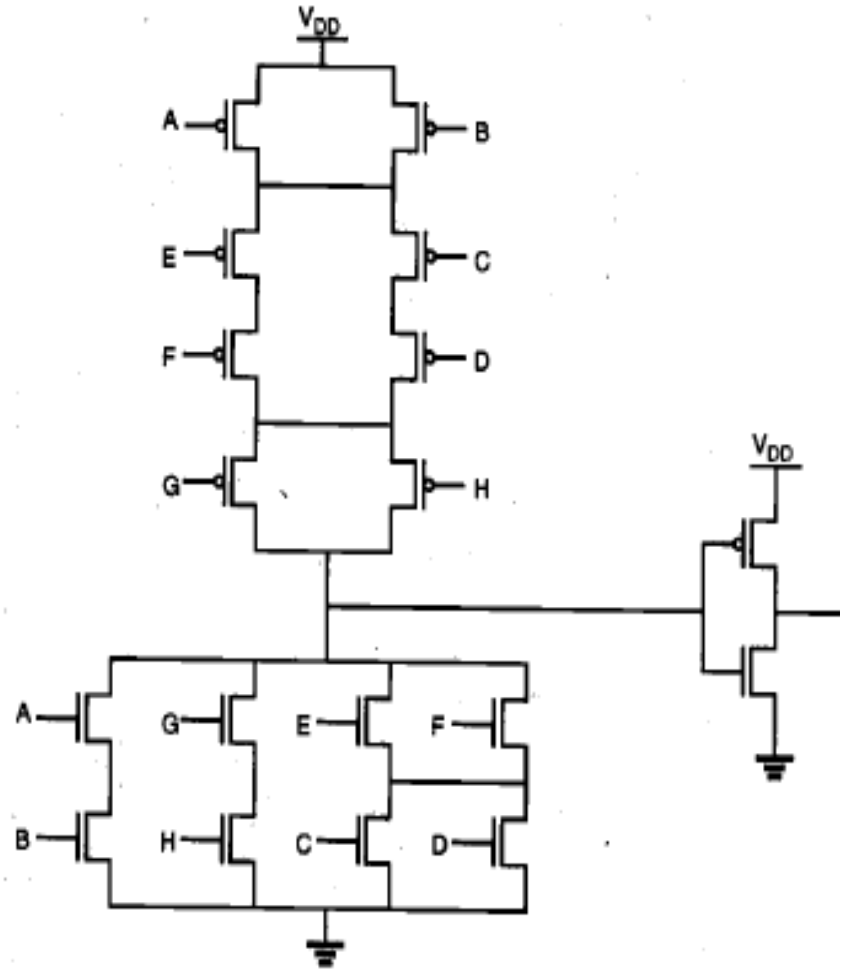
(a) An 8-input complex logic gate, realized using conventional CMOS logic and (b) domino CMOS logic.

$Z = AB + (C+D)(E+F) + GH,$



(b)

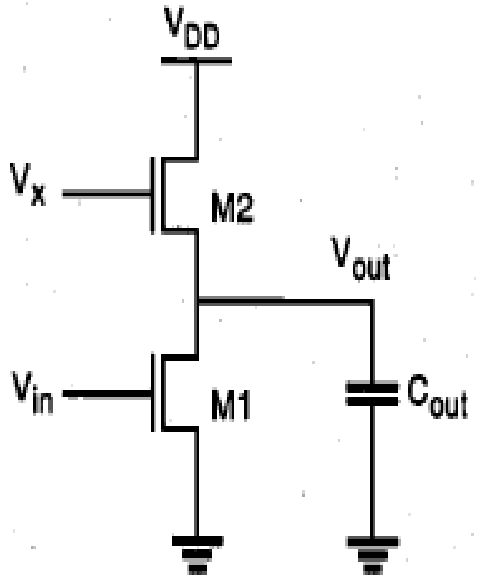
(a)



*Voltage Bootstrapping

- A very useful dynamic circuit technique for overcoming threshold voltage drops in digital circuits, which is called *voltage bootstrapping*.
- We have already seen that output voltage levels may suffer from threshold voltage drops in several circuit structures, such as pass transistor gates or enhancement load inverters and logic gates.
- Dynamic voltage bootstrapping techniques offer a simple yet effective way to overcome threshold voltage drops which occur in most situations.
- the voltage Vx is equal to or smaller than the power supply voltage, Vx *< VDD.* Consequently, the enhancement-type nMOS transistor M2 will operate in saturation.

$$V_{out}(max) = V_x - V_{T2}(V_{out})$$



Enhancement-type circuit in which the output node is weakly driven

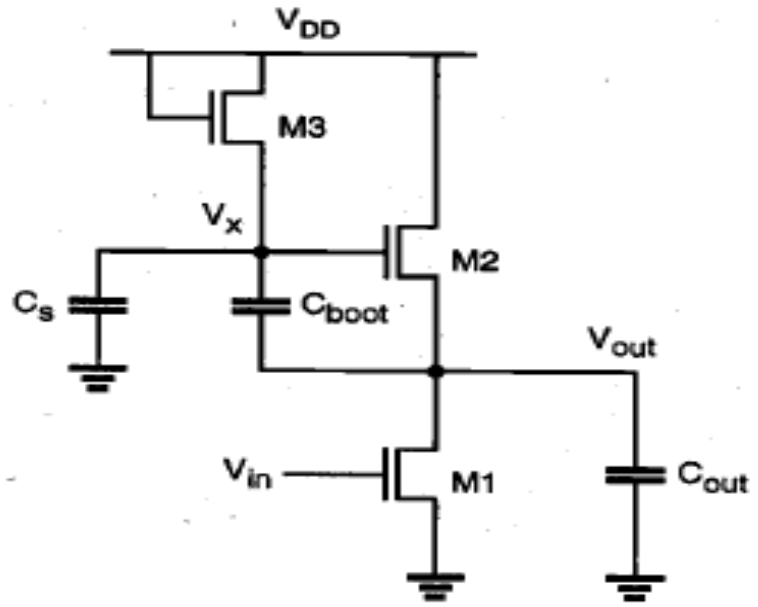
*Dynamic bootstrapping arrangement

- Dynamic bootstrapping arrangement to boost V_x during switching.
- The two capacitors *Cs* and *Cboot,* seen in the circuit diagram represent the capacitances which dynamically couple the voltage Vx to the ground and to the output, respectively.
- This circuit can produce a high Vx during switching, so that the threshold voltage drop can be overcome at the output node.
- At this point, MI is in the linear, region and M2 is in saturation. Since D3 = 0, the initial condition for the voltage Vx can be found as

$$V_x = V_{DD} - V_{T3}(V_x)$$

- Assume that the input switches from its logic-high level to 0 V at t = 0. As a result, the driver transistor Ml will turn off and the output voltage **V,** will start to rise.
- Let i_{Cboot} represent the transient current flowing through the capacitor
- C_{boot} during this charge-up event, and I_{cs} *is* be the current through *Cs.* Assuming that the two current components are approximately equal, we obtain

$$V_x \geq V_{DD} + V_{T2}(V_{out})$$



$$i_{Cs} \approx i_{Cboot} \Leftrightarrow C_S \frac{dV_x}{dt} \approx C_{boot} \frac{d(V_{out} - V_x)}{dt}$$

Contd.

- Reorganizing eqn

$$(C_S + C_{boot})\frac{dV_x}{dt} = C_{boot}\frac{dV_{out}}{dt}$$

$$\frac{dV_x}{dt} = \frac{C_{boot}}{(C_S + C_{boot})} \cdot \frac{dV_{out}}{dt}$$

The increase in the output voltage $V_{out,}$ during this switching event will generate a proportional increase in the voltage level Vx .
Integrating both sides of (2), we obtain

$$\int_{V_{DD}-V_{T3}}^{V_x} dV_x = \frac{C_{boot}}{(C_S + C_{boot})} \cdot \int_{V_{OL}}^{V_{DD}} dV_{out}$$

$$V_x = (V_{DD} - V_{T3}) + \frac{C_{boot}}{(C_S + C_{boot})}(V_{DD} - V_{OL})$$

$$V_x(max) = 2V_{DD} - V_{T3} - V_{OL}$$

which proves that voltagebootstrapping can significantly boost the voltage level V

Contd.

Now remember that in order to overcome the threshold voltage drop at the output, the minimum required voltage level V is

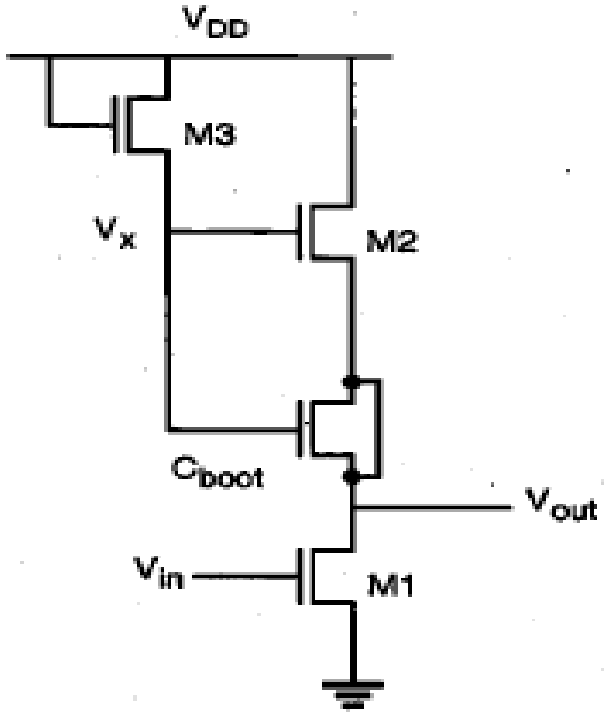
$$V_x(min) = V_{DD} + V_{T2}\big|_{V_{out}=V_{DD}}$$

$$= (V_{DD} - V_{T3}(V_x)) + \frac{C_{boot}}{(C_S + C_{boot})}(V_{DD} - V_{OL})$$

This can rearranged to give the required capacitance ratio, as follows

$$\frac{C_{boot}}{(C_S + C_{boot})} = \frac{V_{T2}\big|_{V_{out}=V_{DD}} + V_{T3}\big|_{V_x}}{(V_{DD} - V_{OL})}$$

$$\frac{C_{boot}}{C_S} = \frac{V_{T2}\big|_{V_{out}=V_{DD}} + V_{T3}\big|_{V_x}}{V_{DD} - V_{OL} - V_{T2}\big|_{V_{out}=V_{DD}} - V_{T3}\big|_{V_x}}$$



Realization of the bootstrapping capacitor with a dummy MOS device.

Note: Cs is essentially the sum of the parasitic source-to-substrate capacitance of M3 and the gate-to-substrate capacitance of M2. To obtain a sufficiently large bootstrap capacitance *Cboot* in comparison to *CS* an extra "dummy" transistor is typically added to the circuit,

BiCMOS

- The signal propagation delay due to large interconnect capacitances is a major factor which limits the performance of CMOS digital integrated circuits.
- The system speed is ultimately restricted by the current-driving capability of CMOS gates that drive large capacitive loads, such as the word lines in memory arrays, or data bus lines between large logic blocks.
- Buffer configurations require a significant amount of silicon area for improvement in the signal propagation delay.
- In comparison, bipolar junction transistors (BJTs) have more current driving
- capability, and hence, can overcome such speed bottlenecks using less silicon area.
- However, the power dissipation of bipolar logic gates is typically one or two orders of
- magnitude larger than that of comparable CMOS gates
- In general, the BiCMOS combination has significant advantages to offer, such as improved switching speed and less sensitivity with respect to the load capacitance.
- In general, BiCMOS logic circuits are not bipolar-intensive, i.e. most logic operations are performed by conventional CMOS subcircuits, while the bipolar transistors are used only when high on-chip or off-chip drive capability is required.

BiCMOS

- An alternative solution to the problem of driving large capacitive loads can be provided by merging CMOS and bipolar devices (BiCMOS) on chip.
- Taking advantage of the low static power consumption of CMOS and the high current driving capability of the bipolar transistor during transients, the BiCMOS configuration can combine the "best of both worlds"

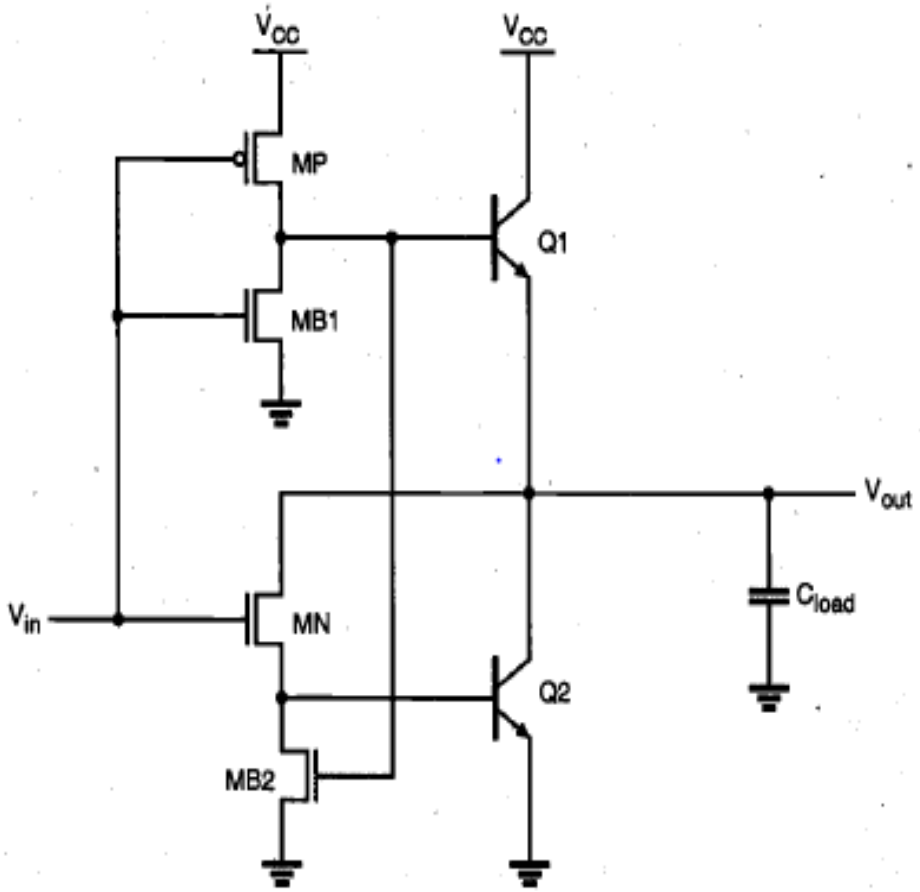
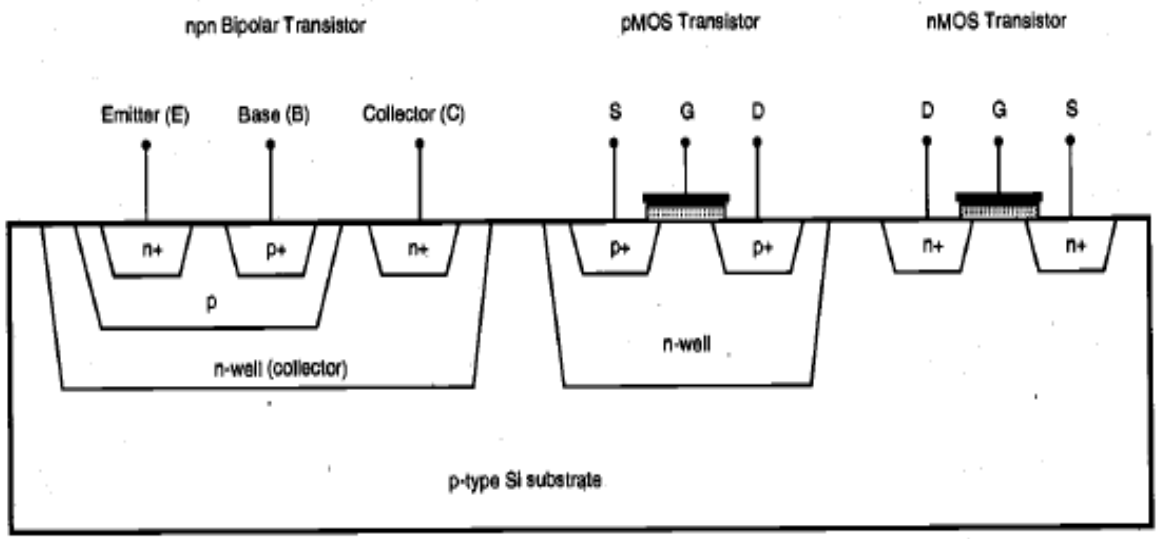


Fig.: Typical BiCMOS inverter circuit, with four MOSFETs and two BJTs

Fabrication of BiCMOS

- The BiCMOS fabrication process typically requires only 3-4 masks in addition to the well-established CMOS process.
- Simplified cross-section showing an npn bipolar transistor, an n-channel MOS transistor, and a p-channel MOS transistor fabricated on the same p-type silicon substrate.
- Notice that many standard CMOS process steps can be used to create bipolar and MOS transistors side-by- side on the chip.



HDD(Hard Disk Drive) Vs SSD(Solid State Drive)

- An HDD is a data storage device that lives inside the computer. It has spinning disks inside where data is stored magnetically. The HDD has an arm with several "heads" (transducers) that read and write data on the disk
- In an SSD, all data is stored in integrated circuits. This difference from HDDs has a lot of implications, especially in size and performance. Without the need for a spinning disk, SSDs can reduce to the shape and size or even as small as a postage stamp
- SSDs dramatically reduce access time since users don’t have to wait for platter rotation to start up.

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