Schmitt Trigger

Figure 1 shows an inverting comparator with positive feedback. This ciruit converts an irregular-shaped waveform to a square wave or pulse. The circuit is known as the Schmitt trigger or squaring circuit. The input voltage v_{in} triggers the output v_o every time it exceeds certain voltage levels called the upper threshold voltage V_{ut} and lower threshold voltage V_{lt}, as shown in Figure 2.

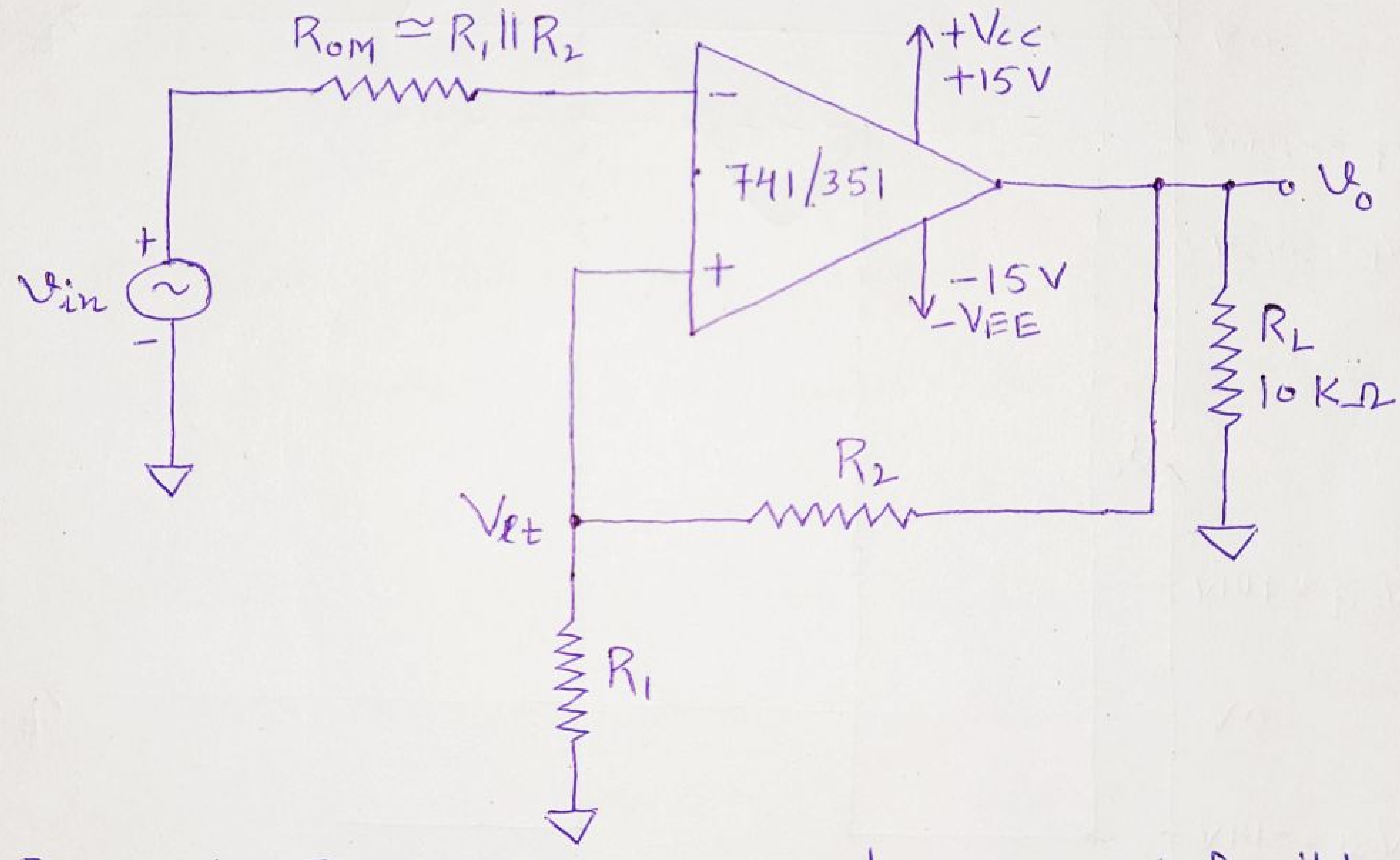

Figure 1. Inverting comparator as schmitt trigger.

In Figure 1, these threshold values of voltages are obtained by using the voltages divider $R_1 - R_2$, where the voltage across R_1 is fed back to the (+) input. The voltage across R_1 is a variable reference threshold voltage that depends on the value and polarity of the output voltage v_o. When $v_o = +V_{sat}$, the voltage across R_1 is called the upper threshold voltage, V_{ut}. The input voltage v_{in} must be slightly more positive than V_{ut} in order to cause the output v_o to switch from $+V_{sat}$ to $-V_{sat}$. As long as $v_{in} < V_{ut}$, v_o is at $+V_{sat}$. Using the voltage divider rule,

$$V_{ut} = \frac{R_1}{R_1 + R_2}(+V_{sat}) \quad \text{——} \quad (1)$$

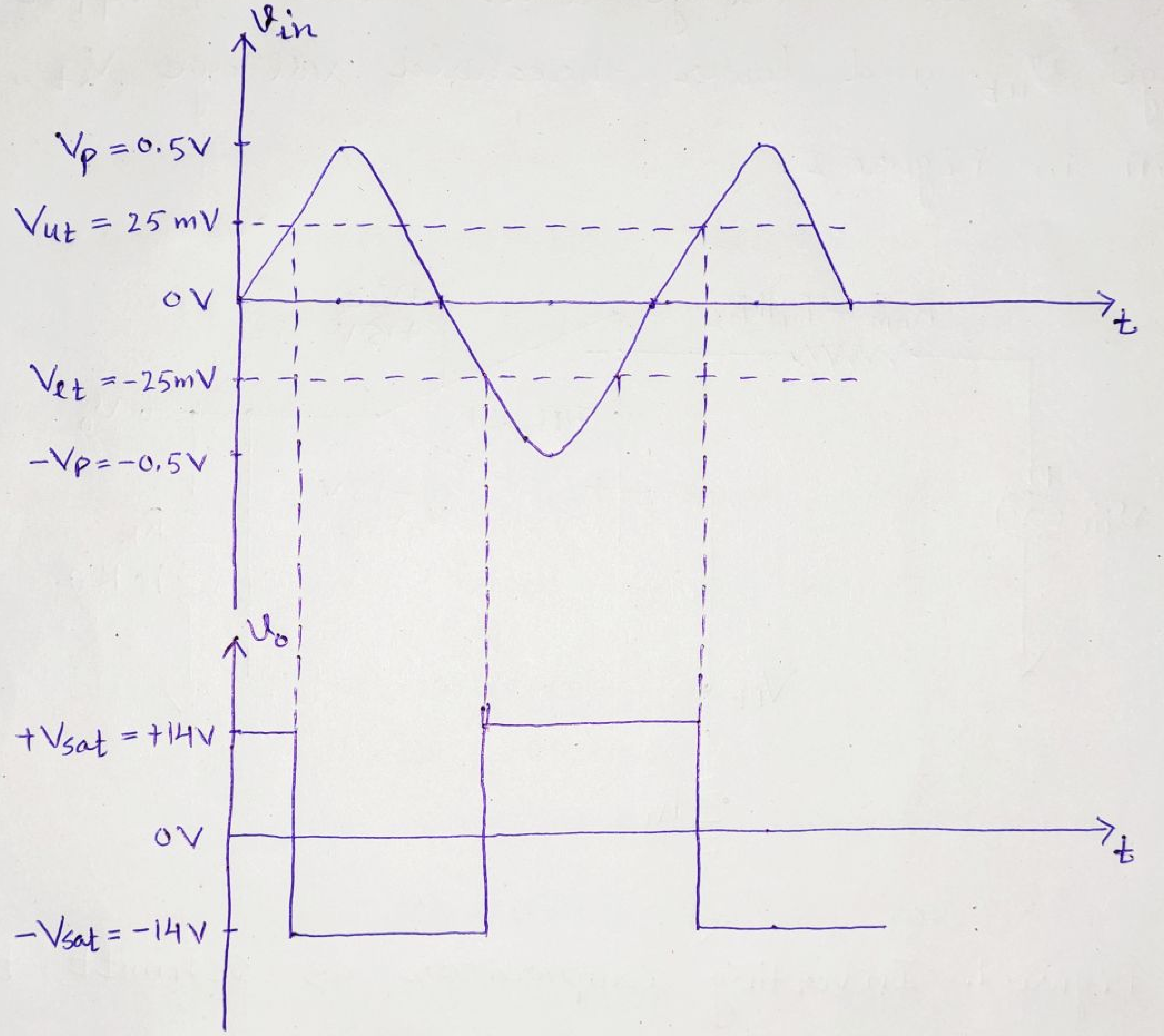

Figure 2. Input and output waveforms of Schmitt trigger.

On the other hand, when $v_o = -V_{sat}$, the voltage across R_1 is referred to as lower threshold voltage, V_{lt}. v_{in} must be slightly more negative than V_{lt} in order to cause v_o to switch from $-V_{sat}$ to $+V_{sat}$.

In other words, for v_{in} values greater than V_{lt}, v_o is at $-V_{sat}$. V_{lt} is given by the following equation:

$$V_{lt} = \frac{R_1}{R_1 + R_2}(-V_{sat}) \quad \text{—— (2)}$$

Thus, if the threshold voltages V_{ut} and V_{lt} are made larger than the input noise voltages, the positive feedback will eliminate the false output transitions. Also the positive feedback, because of its regenerative action, will make v_o switch faster between $+V_{sat}$ and $-V_{sat}$.

In Figure 1, resistance $R_{OM} \cong R_1 \| R_2$ is used to minimize the offset problems.

Figure 2 shows that the output of the Schmitt trigger is a square wave when the input is a sine wave.

The comparator with positive feedback is said to exhibit hysteresis, a dead-band condition. That is, when the input of the comparator exceeds V_{ut}, its output switches from $+V_{sat}$ to $-V_{sat}$ and reverts back to its original state, $+V_{sat}$, when the input goes below V_{lt}.

The hysteresis voltage is, of course, equal to the difference between V_{ut} and V_{lt}. Therefore,

$$V_{hy} = V_{ut} - V_{lt}$$

$$V_{hy} = \frac{R_1}{R_1 + R_2}\left[+V_{sat} - (-V_{sat})\right] \quad \text{—— (3)}$$

The v_o versus v_{in} plot of the hysteresis voltage is shown in Figure 3.

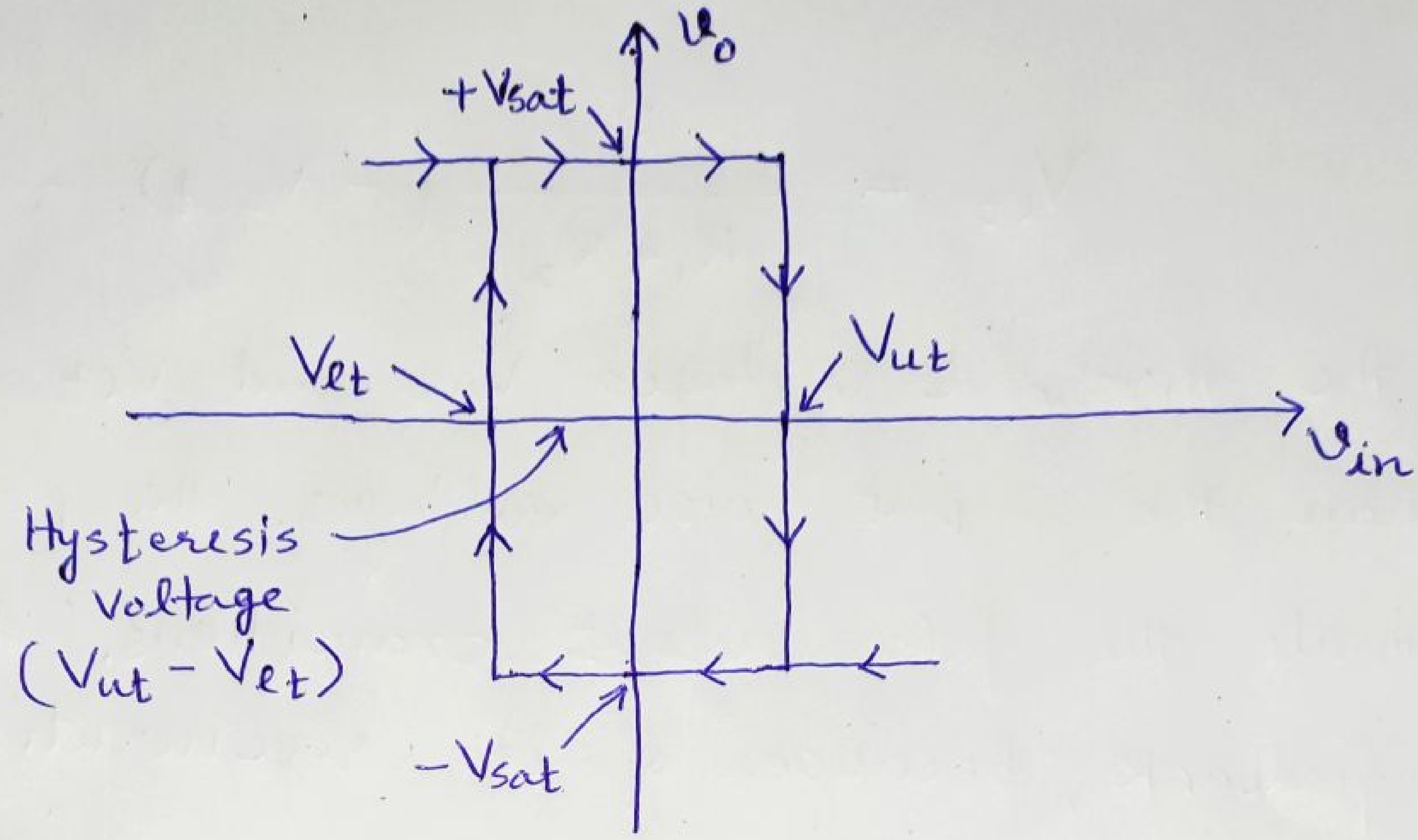

Figure 3. v_o versus v_{in} plot of the hysteresis voltage.

Q1. In the circuit of Figure 1, $R_1 = 100\ \Omega$, $R_2 = 56\ K\Omega$, $v_{in} = 1\ V_{pp}$ sine wave, and the op-amp is type 741 with supply voltages $= \pm 15$ V. Determine the threshold voltages V_{ut} and V_{lt} and draw the output waveform.

Solution: For 741, the maximum output voltage swing is ± 14 V, that is, $+V_{sat} = 14$ V and $-V_{sat} = -14$ V.

From equations (1) and (2),

$$V_{ut} = \frac{100}{56000 + 100}(14) = 25\ mV$$

$$V_{lt} = \frac{100}{56000 + 100}(-14) = -25\ mV$$

The output v_o waveform is shown in Figure 2.

From equation (3), the hysteresis voltage is,

$$V_{hy} = V_{ut} - V_{lt} = 50\ mV$$

Comparator Characteristics

The important characteristics of a comparator are

1. Speed of operation
2. Accuracy
3. Compatibility of output

The output of the comparator must switch rapidly between saturation levels and also respond instantly to any change of conditions at its inputs. This implies that the bandwidth of the op-amp comparator must be rather wide; in fact; the wider the band width, the higher is the speed of operation. The speed of operation of the comparator is improved with positive feedback (hysteresis).

The accuracy of the comparator depends on its voltage gain, common-mode rejection ratio, input offsets, and termal drifts. High voltage gain requires a smaller difference voltage (hysteresis voltage) to cause the comparator's output voltage to switch between saturation levels. On the other hand, a high CMRR helps to reject the common-mode input voltages, such as noise, at the input terminals. Finally, to minimize the offset problems, the input offset current and input offset voltage must be negligible; also, the changes in these offsets due to temperature variations should be very slight.

Since the comparator is a form of analog-to-digital converter, its output must swing between two logic levels suitable for a certain logic family such as transistor-transistor logic (TTL).

Limitations of op-amp as Comparators

The output of an op-amp comparator is generally not compatible with a particular logic family such as the TTL, which requires input voltages of either approximately +5 V or 0V. Therefore, to keep the output voltage swing within specific limits, op-amps are used with externally wired components such as zeners or diodes. The resulting circuits, in which the outputs are limited to predetermined values, are called limiters.

Voltage Limiters

In Figure 4, the zener diodes D_1 and D_2 are connected in the feedback path. This arrangement limits the positive and negative values of the output voltage V_o. When the input voltage V_{in} crosses 0 V and increases in the positive direction, the output voltage V_o increases in the negative direction until diode D_1 is forward biased and D_2 goes into avalanche conduction. Therefore, the maximum negative value of V_o is equal to $(V_Z + V_{D1})$, where V_Z is the zener voltage and V_{D1} is the voltage drop across the forward biased zener D_1 (= 0.7 V typically).

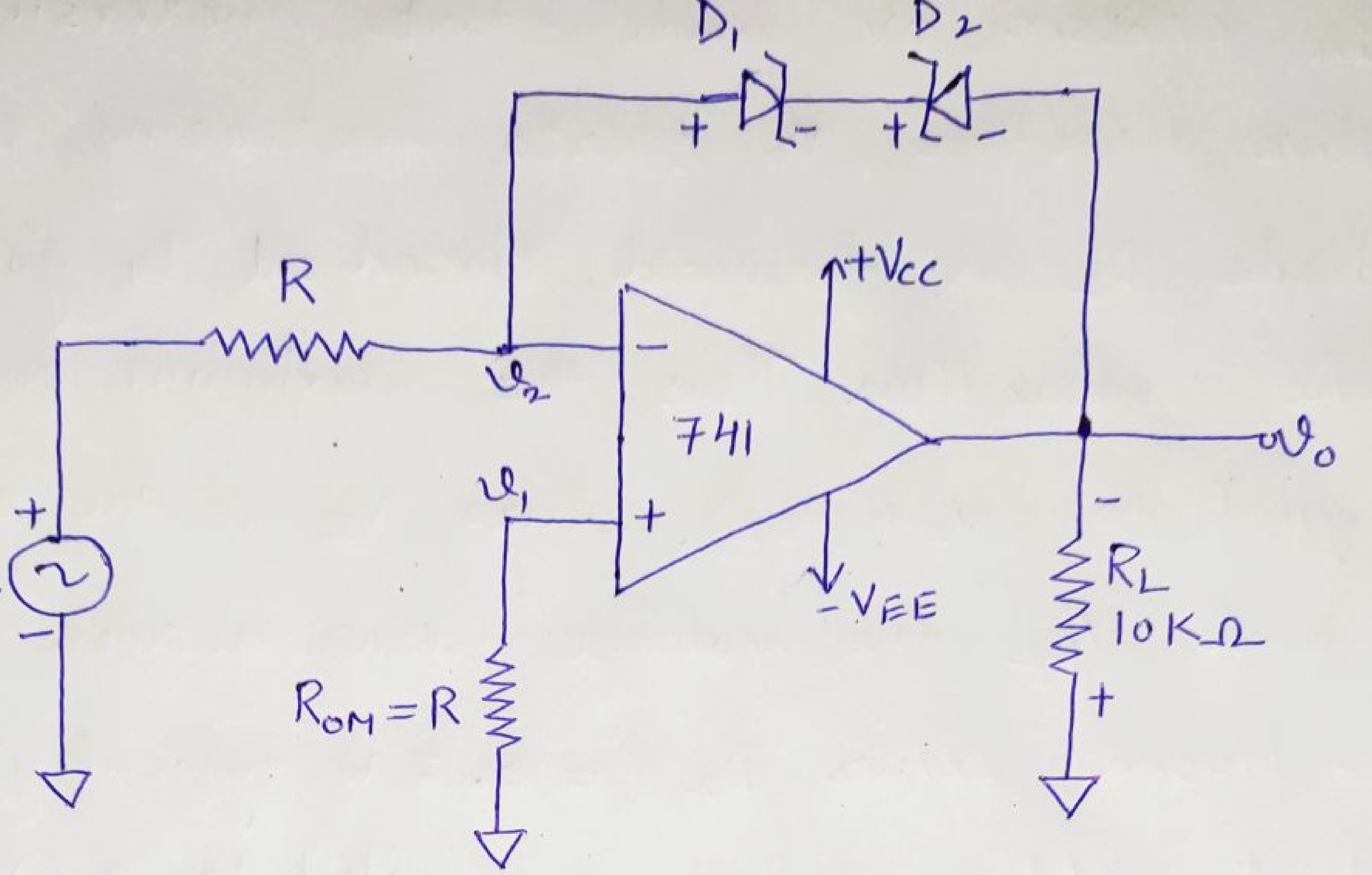

Figure 4. Basic op-amp comparator with positive and negative output voltage limiting.

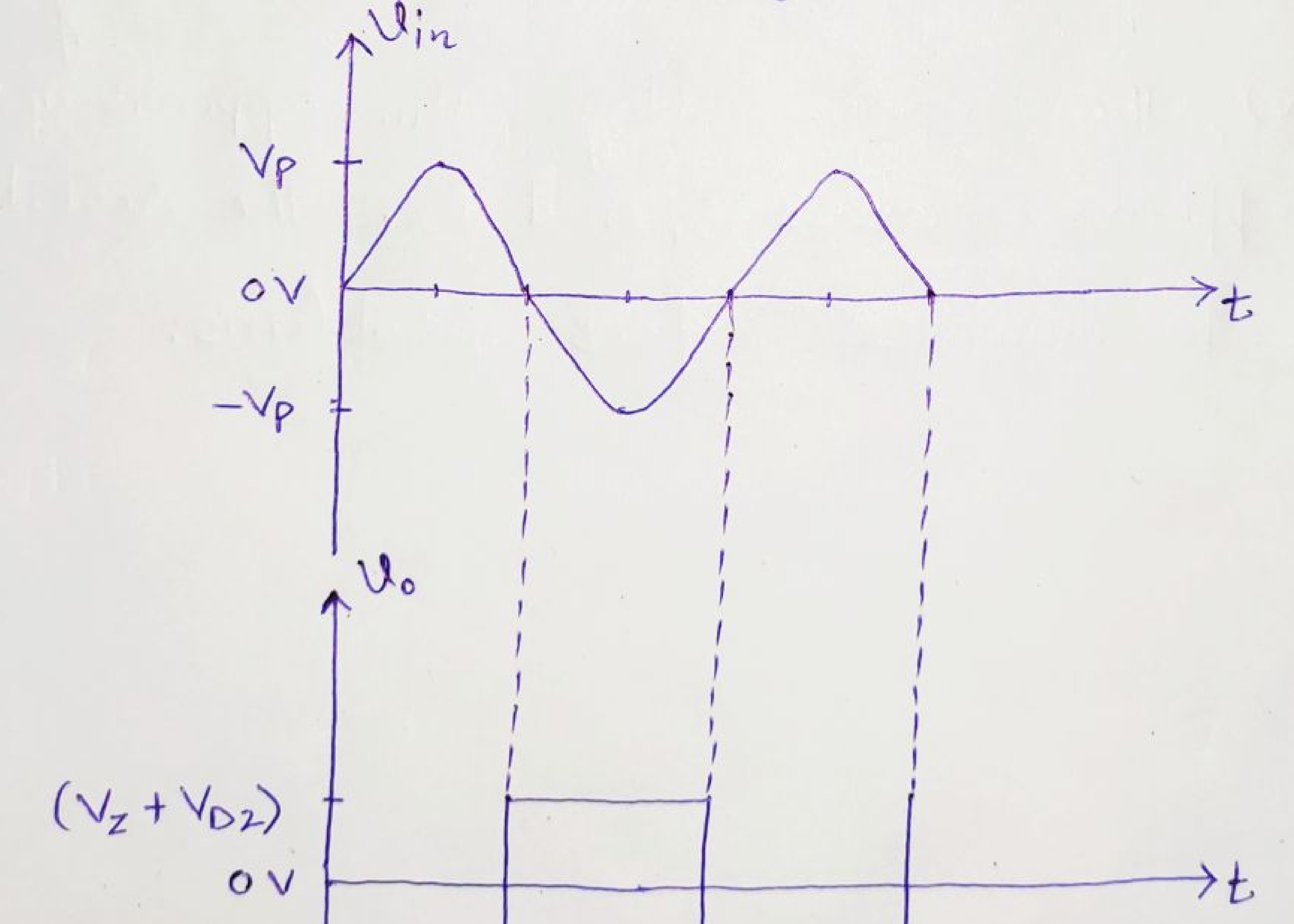

Figure 5. Input and output waveforms.

Figure 5 shows the input and output waveforms for the circuit of Figure 4.

When v_{in} crosses 0V and starts increasing in the negative direction, v_o starts increasing positively until diode D_2 is forward biased and D_1 goes into avalanche conduction. Thus the maximum positive v_o is equal to $(V_Z + V_{D2})$, where V_Z is the zener voltage and V_{D2} the voltage drop across the forward-biased zener D_2 (= 0.7 V typically). Thus, the output voltage swing is limited to $+(V_Z + 0.7)$ and $-(V_Z + 0.7)$, as shown in Figure 5.

Note that, in the circuit of Figure 4, since the input terminals of the op-amp are at virtual ground ($v_1 = v_2 \cong 0V$), the input voltage v_{in} appears across R, and v_o appears across D_1 and D_2. The resistance R_{OM} is used to minimize offset problems.