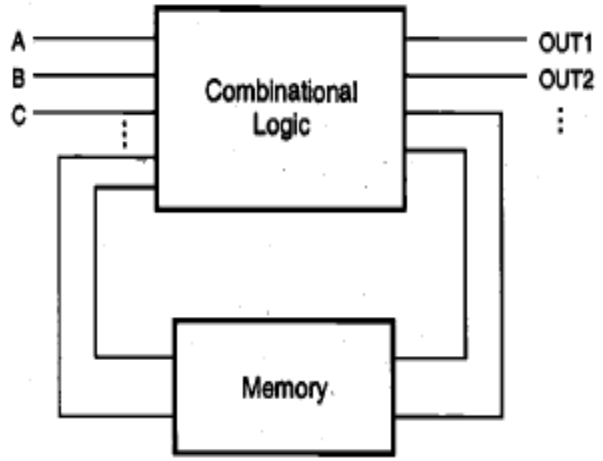
CMOS VLSI Design

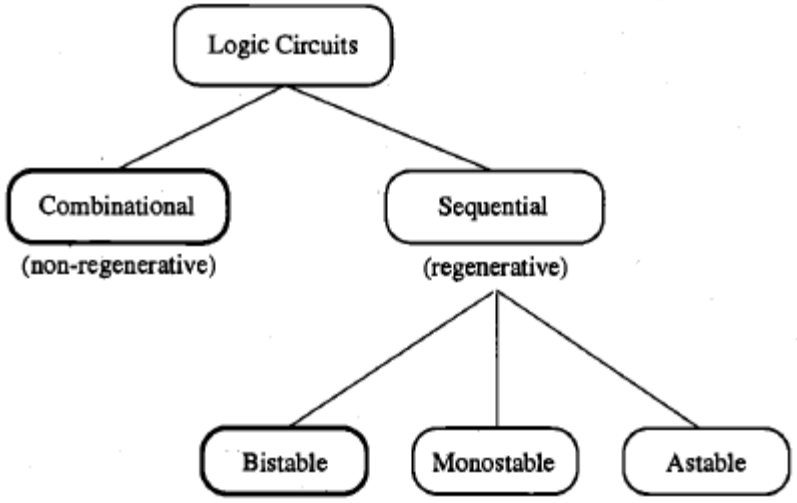
ECE318

Unit5: Sequential Circuit

Sequential Circuit

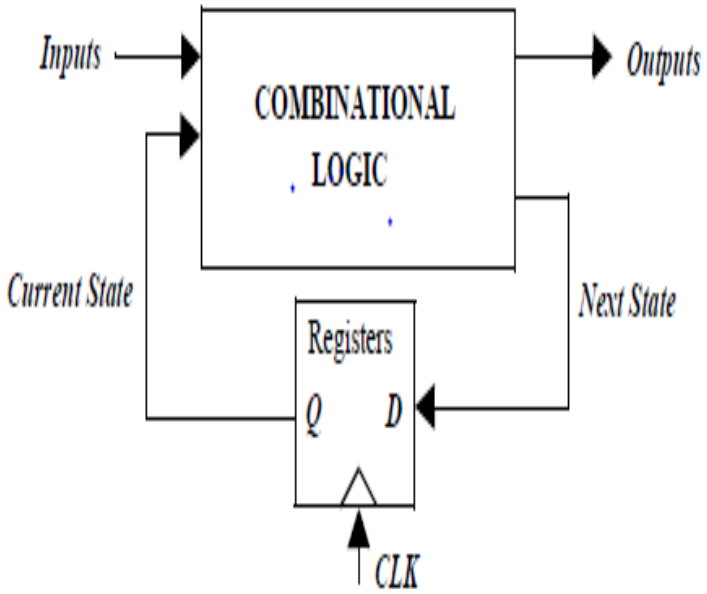
- Logic circuits is called sequential circuits, in which the output is determined by the current inputs as well as the previously applied input variables.
- Classification of logic circuits based on their temporal behavior





Sequential Circuit

- *In sequential logic* circuits, the output not only depends upon the *current* values of the inputs, but also upon *preceding* input values. In other words, a sequential circuit remembers some of the past history of the system—it has memory
- A block diagram of a generic *finite state machine* (FSM) that consists of combinational logic and registers, which hold the system state. The system depicted here belongs to the class of *synchronous* sequential systems, in which all registers are under control of a single global clock.
- The outputs of the FSM are a function of the current *Inputs* and the *Current State*. The *Next State* is determined based on the *Current State* and the current *Inputs* and is fed to the inputs of registers.

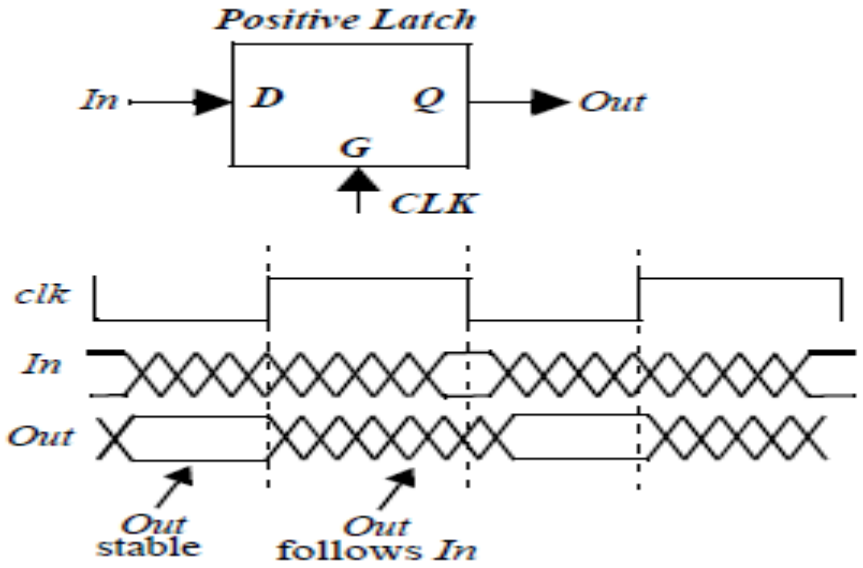


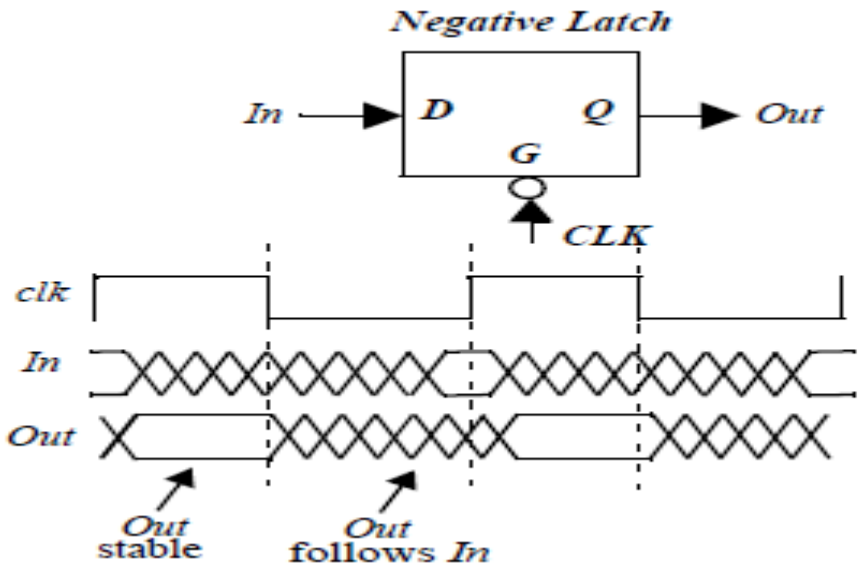
Storage Elements

- A storage element in a digital circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit), until directed by an input signal to switch states.
- *Storage elements that operate with signal levels (rather than signal transitions) are referred to as latches*
- *those controlled by a clock transition are flip-flops .*

Latches versus Registers

- A latch is an essential component in the construction of an *edge-triggered* register. It is *level-sensitive* circuit that passes the *D* input to the *Q* output when the clock signal is high.
- This latch is said to be in *transparent* mode.
- A *negative latch* passes the *D* input to the *Q* output when the clock signal is low.
- Contrary to *level-sensitive* latches, *edge-triggered* registers only sample the input on a clock transition — 0-to-1 for a *positive edge-triggered* register, and 1-to-0 for a *negative edge-triggered* register.





The Bistability Principle

- Bistable circuits have, as their name implies, two stable states or operation modes, each of which can be attained under certain input and output conditions.
- Monostable circuits, on the other hand, have only one stable operating point (state).
- Static memories use positive feedback to create a *bistable circuit* — a circuit having two stable states that represent 0 and 1
- The cross-coupling of two inverters results in a *bistable* circuit, that is, a circuit with two stable states, each corresponding to a logic state. The circuit serves as a memory, storing either a 1 or a 0.
- A bistable circuit has two stable states. In absence of any triggering, the circuit remains in a single state (assuming that the power supply remains applied to the circuit), and hence remembers a value.
- A trigger pulse must be applied to change the state of the circuit.
- Another common name for a bistable circuit is *flip-flop* (unfortunately, an *edge-triggered* register is also referred to as a *flip-flop*).

Bistable Behavior

- Here, the output voltage of inverter (1) is equal to the input voltage of inverter (2), i.e., *Vo1* = *Vi2,* and the output voltage of inverter (2) is equal to the input voltage of inverter (1), i.e., *V02* = *Vi.*
- In order to investigate the static input-output behavior of both inverters, we start by plotting the voltage transfer characteristic of inverter (1) with respect to the *Vo1* – *Vi1*, axis pair

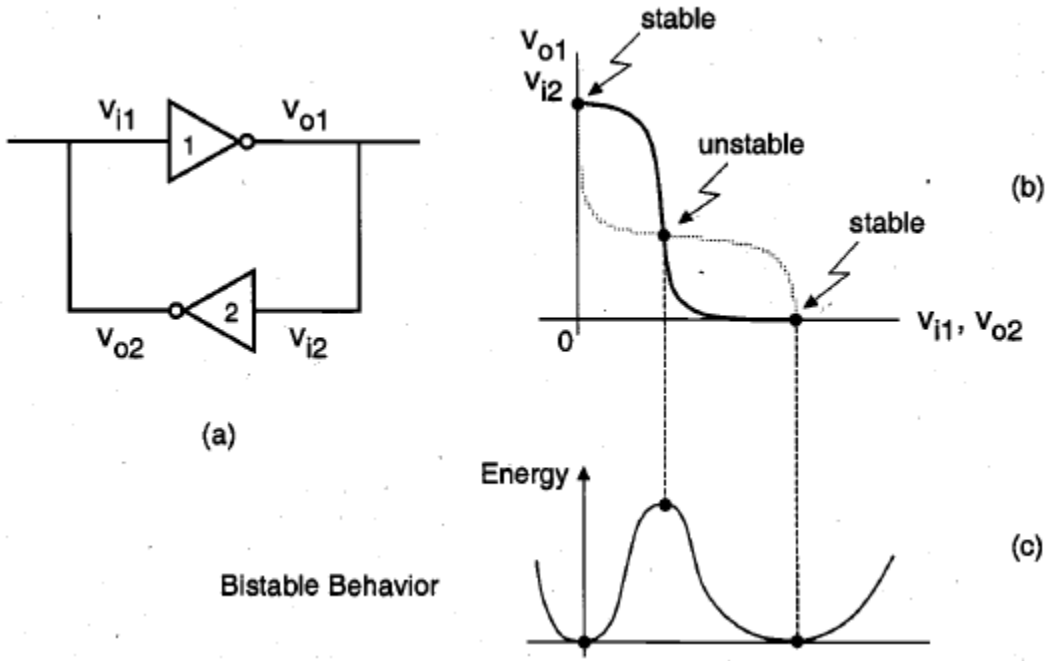
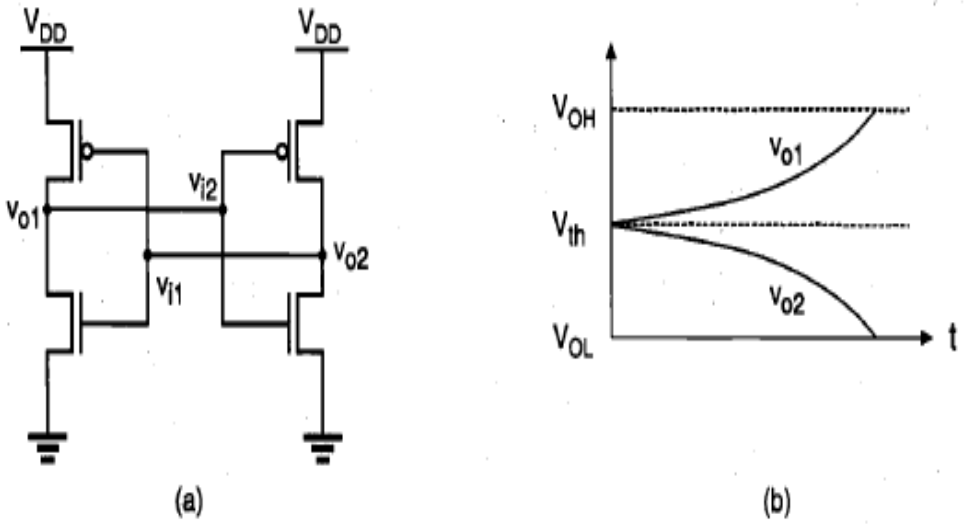
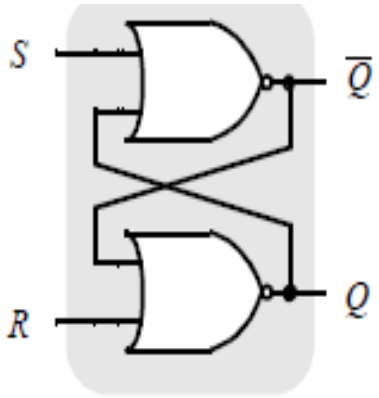


Fig (a) Circuit diagram of a CMOS bistable element. (b) One possibility for the expected time-domain behavior of the output voltages, if the circuit is initially set at its unstable operating point.

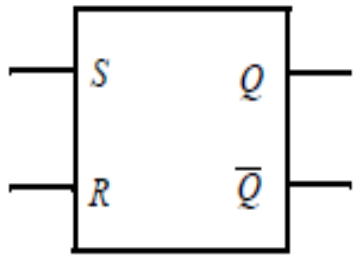


SR Latch

- NOR-based *SR* Latch



(a) Schematic diagram



(b) Logic symbol

S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

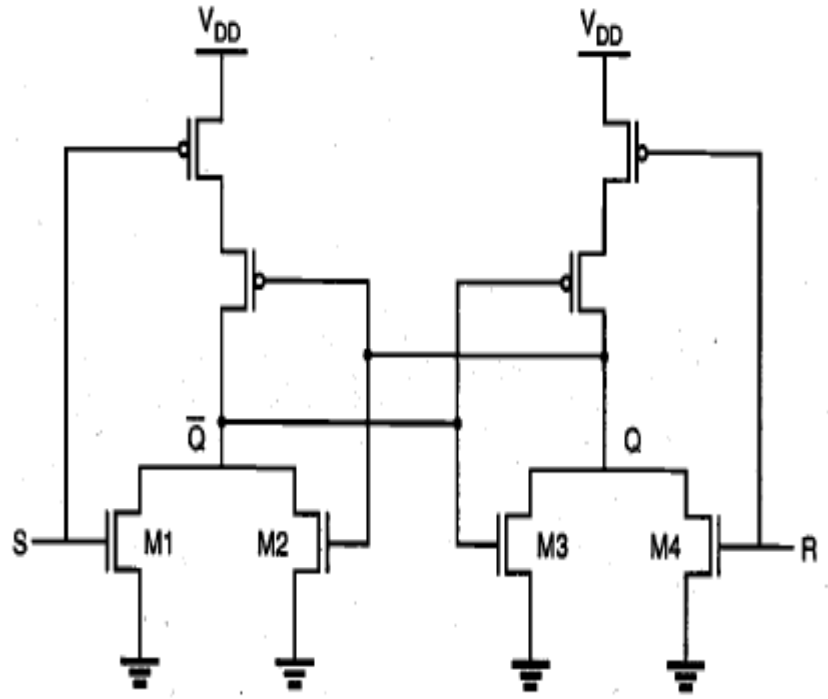
Forbidden State

(c) Characteristic table

The SR Latch Circuit with NOR2

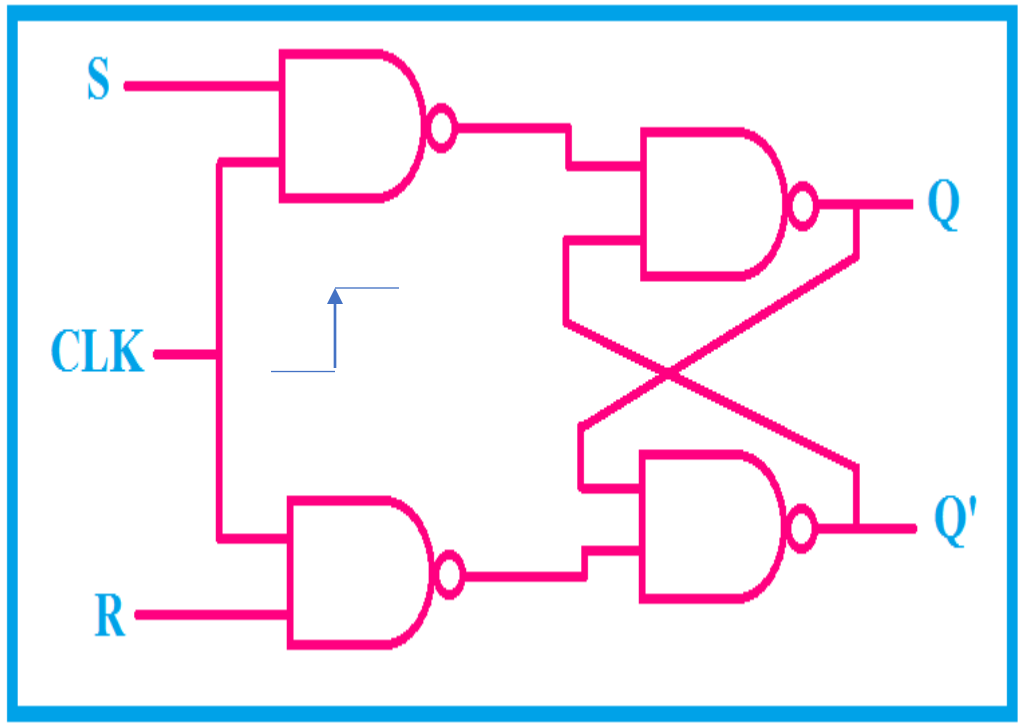
- The circuit preserves its state (either one of the two possible modes) as long as the power supply voltage is provided; hence, the circuit can perform a simple memory function of *holding* its state.
- However, the simple two-inverter circuit examined above has no provision for allowing its state to be changed externally from one stable operating mode to the other.
- To allow such a change of state, we must add simple switches to the bistable element, which can be used to force or trigger the circuit from one operating point to the other.

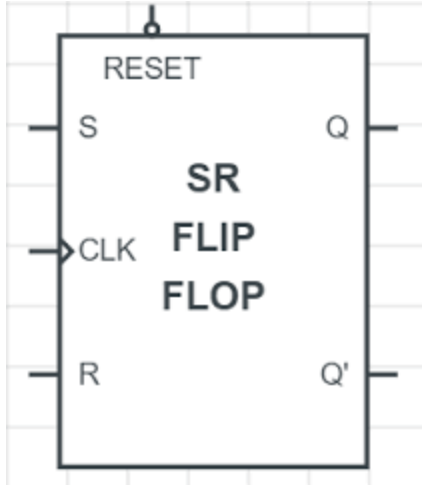
S	R	Q_{n+1}	$\overline{Q}_{n+1}$	Operation
V_{OH}	V_{OL}	V_{OH}	V_{OL}	M1 and M2 on, M3 and M4 off
V_{OL}	V_{OH}	V_{OL}	V_{OH}	M1 and M2 off, M3 and M4 on
V_{OL}	V_{OL}	V_{OH}	V_{OL}	*M*1 and M4 off, M2 on, or
V_{OL}	V_{OL}	V_{OL}	V_{OH}	M1 and M4 off, M3 on



CMOS SR latch circuit based on NOR2 gates

SR Flip flop



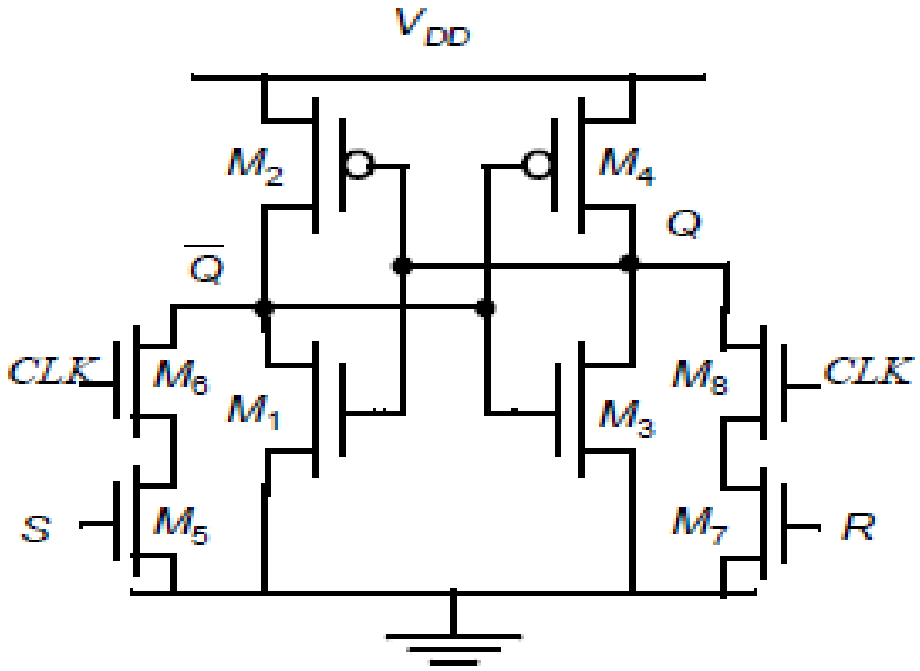


CLK	S	R	Q	Q’
↓	x	x	NC	NC
↑	0	0	NC	NC
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	invalid	invalid

$$Q(t+1)=S+R'Q(t)$$

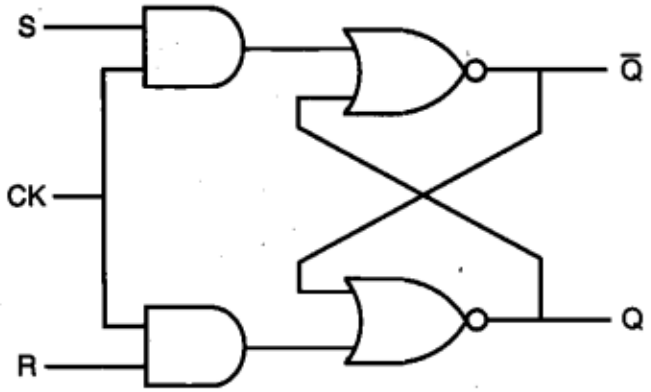
Synchronous SR FF with Clock

- Most systems operate in a synchronous fashion with transition events referenced to a clock.
- The presented flip-flop does not consume any static power.
- In steady-state, one inverter resides in the high state, while the other one is low.
- No static paths between *VDD* and *GND* can exist except during switching.



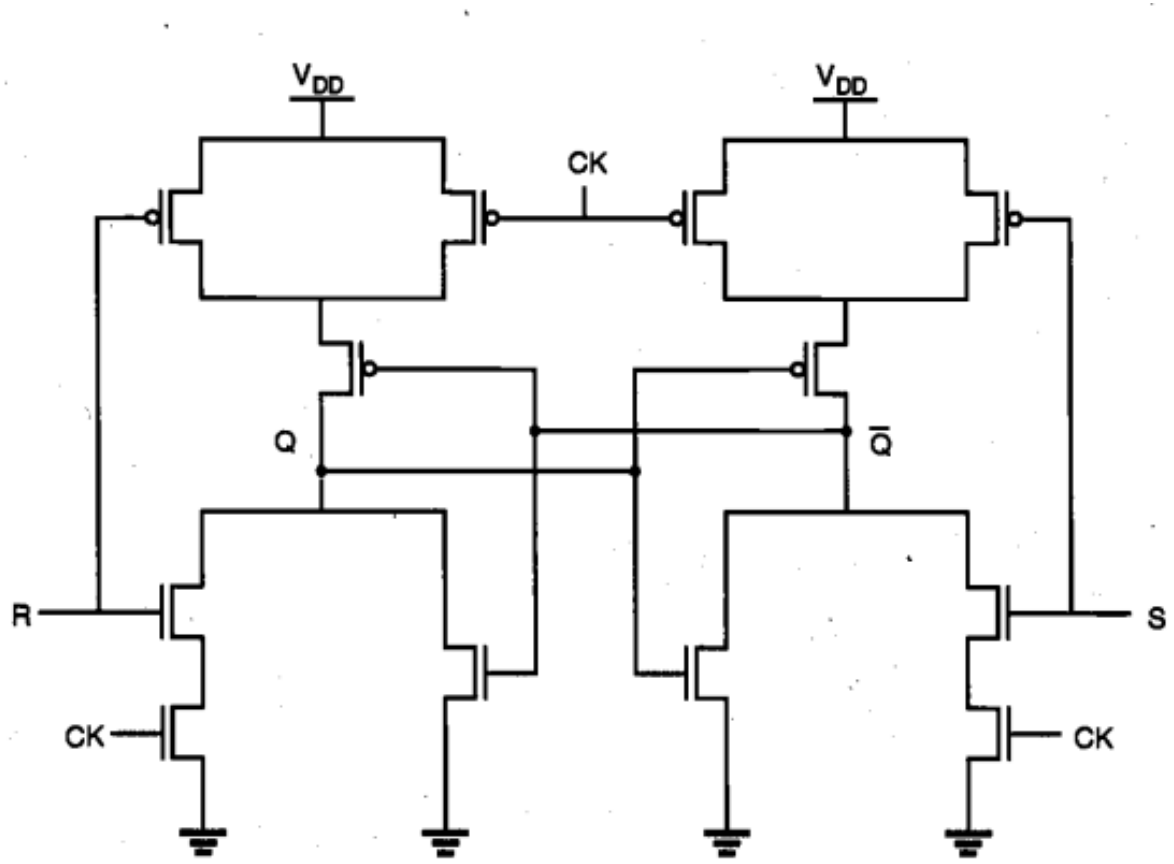
CMOS clocked *SR* flip-flop.

Gate-level schematic of the clocked NOR-based SR latch



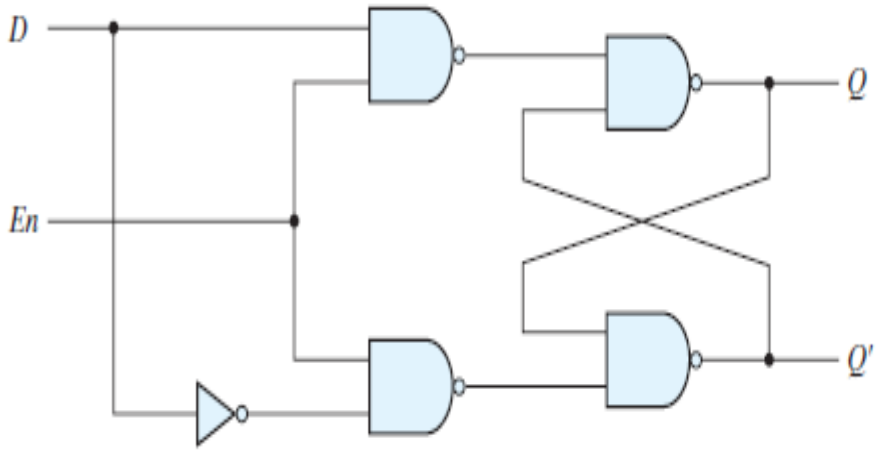
Synchronous SR FF with Clock

AOI-based implementation of the clocked NOR-based SR latch circuit



D Latch

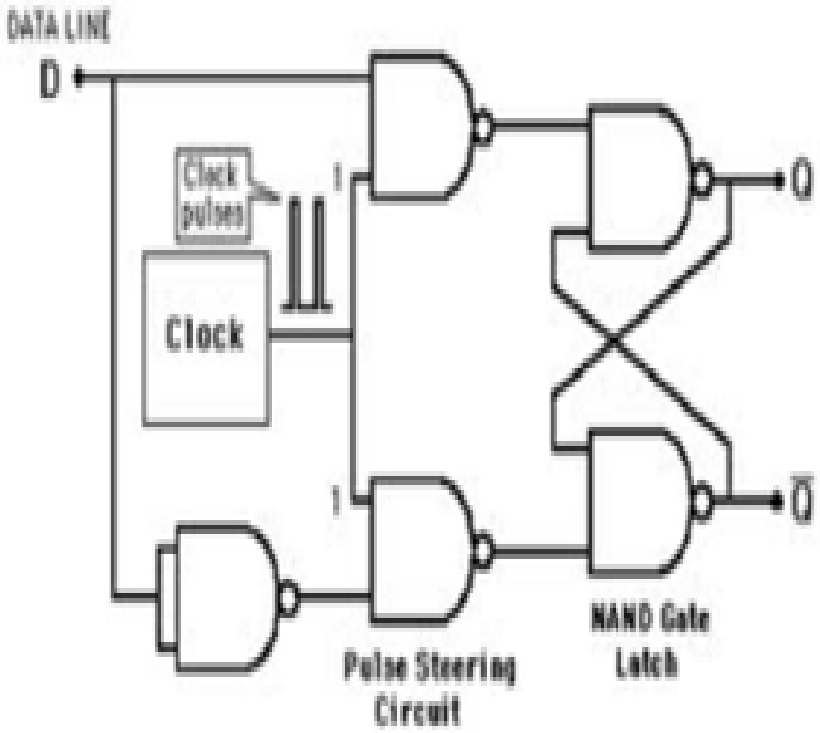
- With NAND gate
- Drawbacks of clocked R-S flip-flop are overcome in D (delay) flip-flop.
- The transfer of data from the input to the output is delayed, the flip-flop is named delay (D) flip-flop.

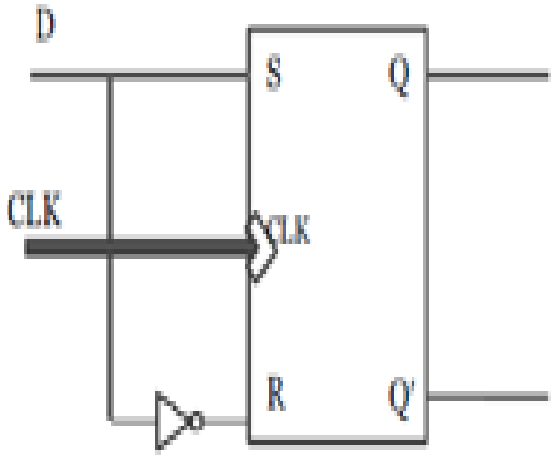


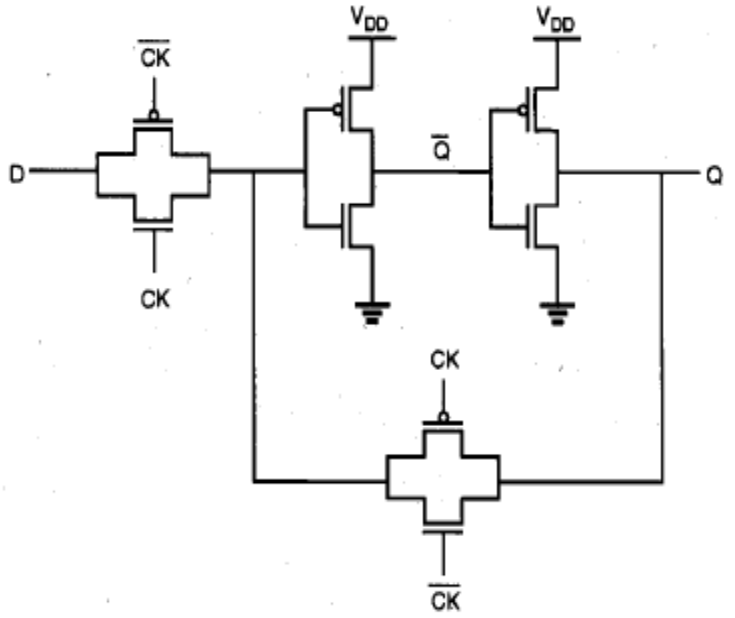
En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

D- flip flop

CLK	D	Q	Q’
↓	x	NC	NC
↑	0	0	1
↑	1	1	0



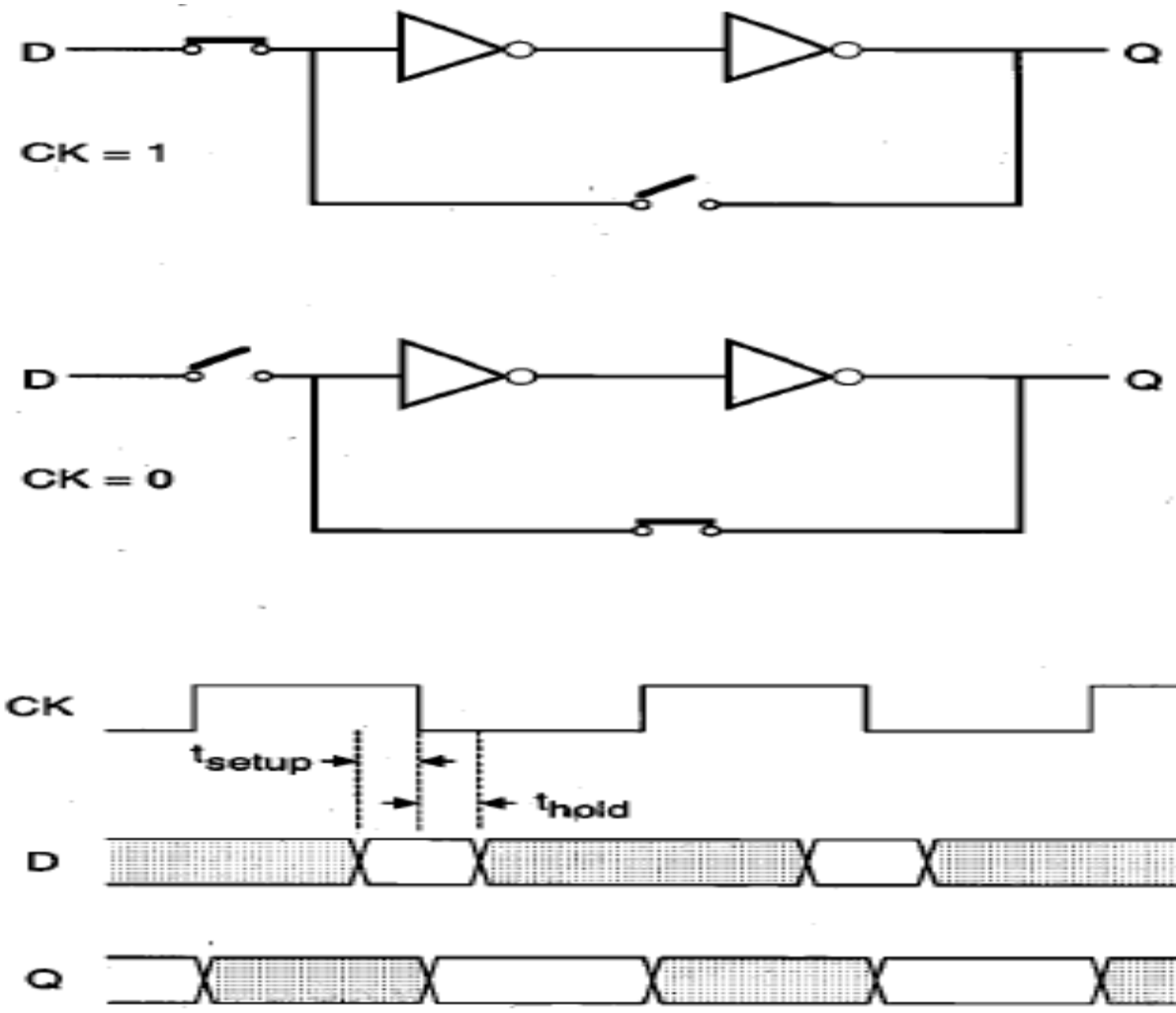




CMOS implementation of the D-latch

Timing Diagram

- Simplified schematic view and the corresponding timing diagram of the CMOS Dlatch circuit, showing the setup time and the hold time.



Keyword

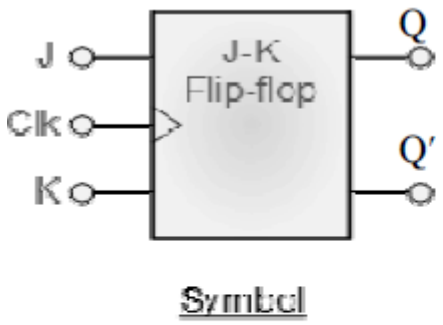
- Latches and Flipflop
- Synchronous and asynchronous sequential circuit
- Combinational and Sequential circuit

Q.1 A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
a) AND or OR gates
b) XOR or XNOR gates
c) NOR or NAND gates
d) AND or NOR gates

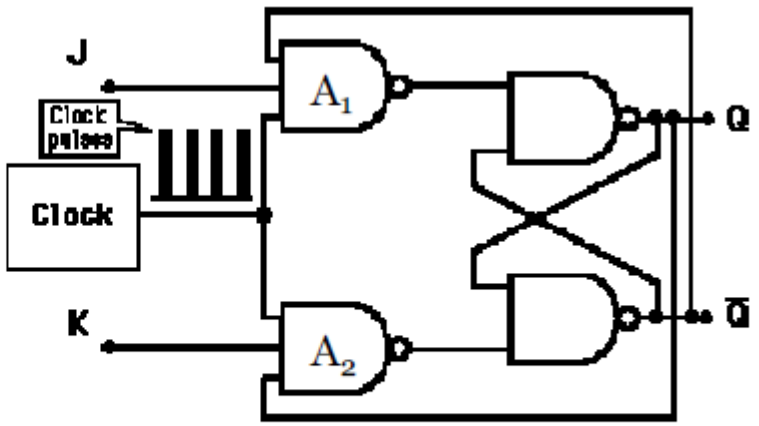
J-K flip flop

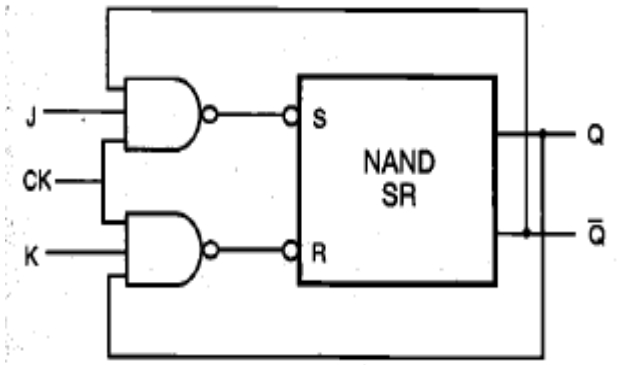
- The functioning of J-K flop-flop is identical to that of the R-S flip-flop in RESET, SET, and no change conditions of operation.
- The difference is that the J-K flip-flop has no invalid state as does the R-S flip-flop.
- J-K flip-flop is a very versatile device
- It has wide application in digital devices such as counters, registers, arithmetic logic units, and other digital systems.

J-K flip-flop



Symbol



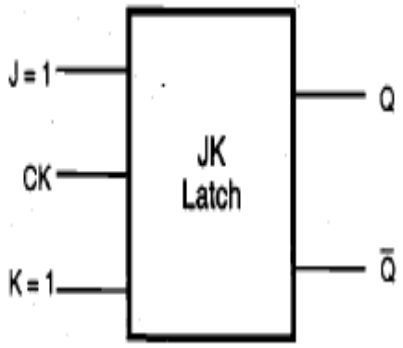


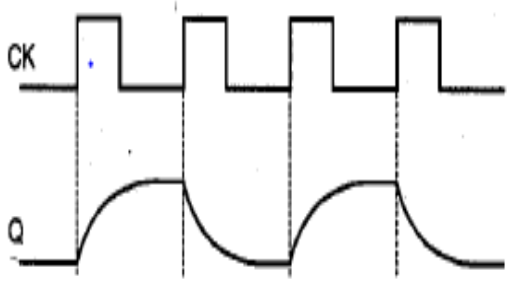
CLK	J	K	Qn+1	Action
↓	x	x	Qn	NC
↑	0	0	Qn	NC
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	Qn’	Toggle

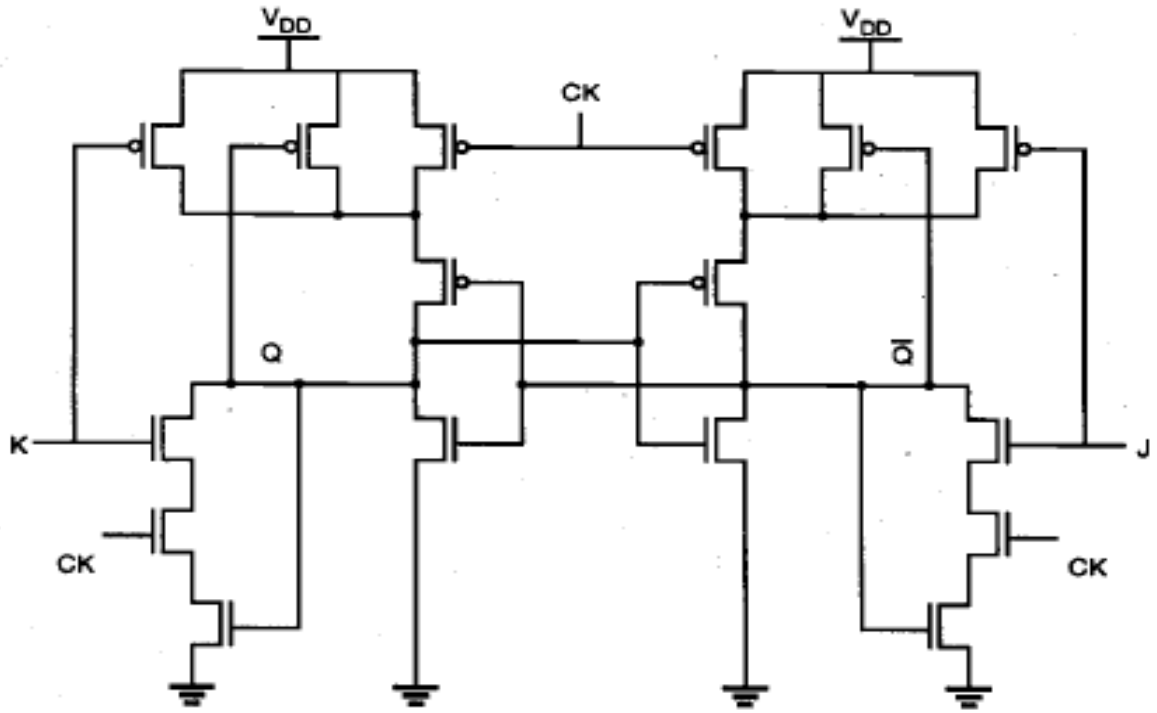
CLK	J	K	Q_n	Q_{n+1}	Q_{n+1}
0	X	X	0/1	0/1	Q_n
↑	0 0	0 0	0 1	0 1	Q_n
↑	0 0	1 1	0 1	0 0	0
↑	1 1	0 0	0 1	1 1	1
↑	1 1	1 1	0 1	1 0	Q_n'

CMOS based J-K FF

- J-K FF







CMOS AOI realization of the JK latch

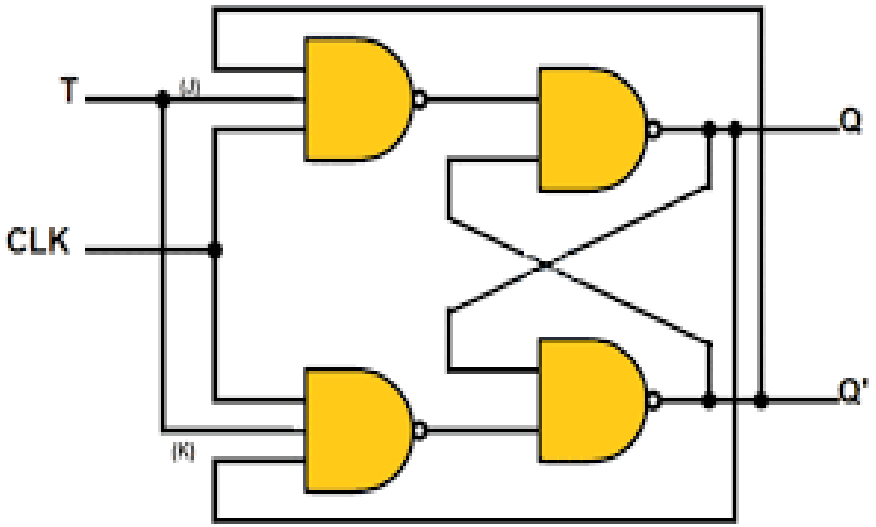
Interview Questions

- Race around condition
- Truth table, Characteristic Table and Excitation table
- Characteristic equation

Quiz

On a J-K flip-flop, when is the flip-flop in a hold condition?
a) J = 0, K = 0
b) J = 1, K = 0
c) J = 0, K = 1
d) J = 1, K = 1

T – Flip-Flop



- This flip-flop is basically a J-K flip-flop. This is also called *Trigger or Toggle flip-flop.*
- This has only a single data input(T), a clock input and two outputs Q and Q'.

$$Q(t+1)= TQ'(t)+T'Q(t)$$

TRUTH TABLE		EXCITATION TABLE			CHARACTERISTIC TABLE		
INPUT	OUTPUT	INPUT		OUTPUT	INPUT	OUTPUT	
T	Q(t+1)	Q(t)	Q(t+1)	T	T	Q(t)	Q(t+1)
0	Q(t) NO CHANGE	0	0	0	0	0	0
		0	1	1	0	1	1
1	Q(t) COMPLEMENT	1	0	1	1	0	1
		1	1	0	1	1	0

TRUTH TABLE, EXCITATION TABLE AND CHARACTERISTIC TABLE OF T FLIP-FLOP

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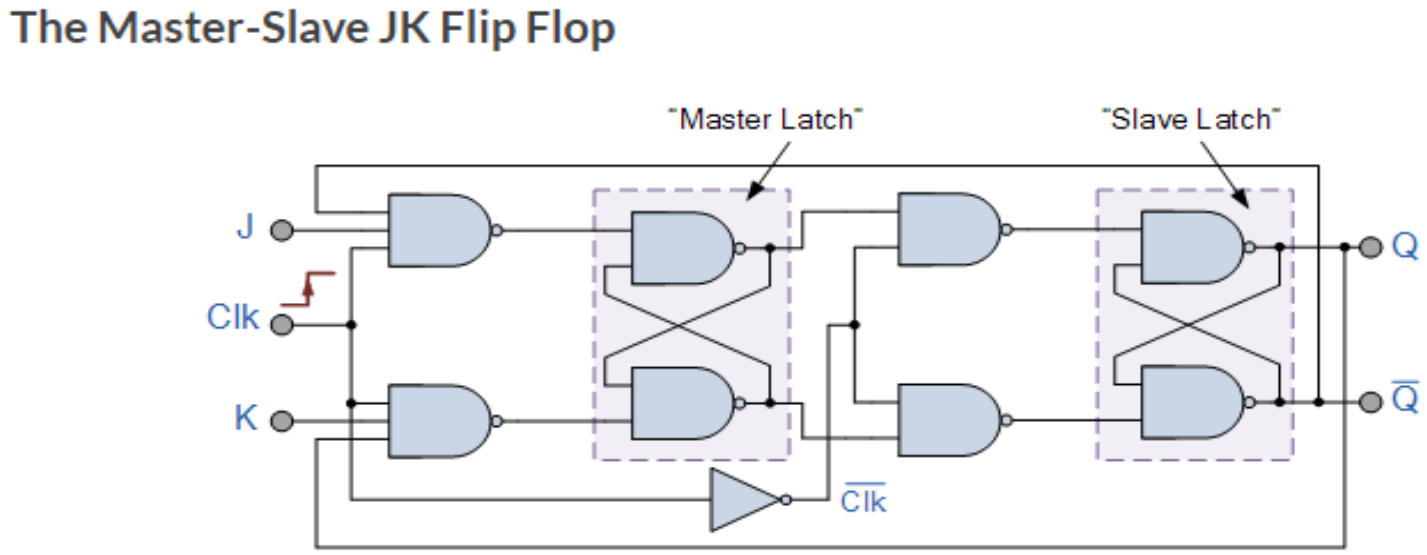
Toggle

Race around condition in J-K flip Flop

Race around condition in J-K flip flop:

- In j—k flip flop, when both j and k inputs are high and when clock pulse width is greater than the prorogation delay of flip flop. In this situation flip ideally toggled only once but toggles more than once. This condition is called race around condition. To prevent this either prorogation delay time should greater than pulse width or use master slave flip flop.
- uncertainty in determining output state of flip flop due toggling of when J=K=1 and clock high for too long period> Propagation delay
- Master -slave flip flop stops continuous toggling by slave filp-flop with clock=0 that shows the state of no change.

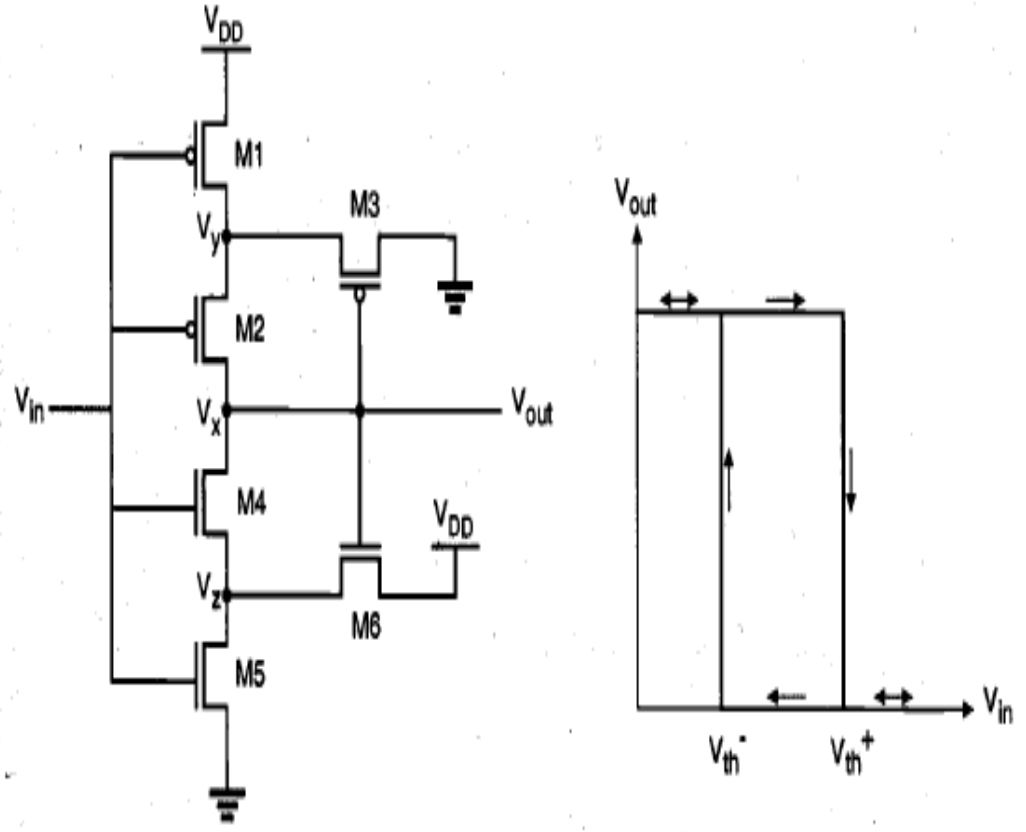
Master-slave J-K flip-flop



- The master-slave flip-flop eliminates all the timing problems by using two SR flip-flops connected together in a series configuration.
- One flip-flop acts as the “Master” circuit, which triggers on the leading edge of the clock pulse while the other acts as the “Slave” circuit, which triggers on the falling edge of the clock pulse.
- This results in the two sections, the master section and the slave section being enabled during opposite half-cycles of the clock signal.

Schmitt Trigger Circuit (Non-biastable sequential circuit)

- Other regenerative circuits can be catalogued as *astable* and *monostable*. The former act as oscillators and for instance, can be used for on-chip clock generation.
- A Schmitt trigger is a device with two important properties:
- It responds to a slowly changing input waveform with a *fast transition time at the output*.
- The voltage-transfer characteristic of the device displays *different switching thresholds for positive- and negative-going input signals*.
- The Schmitt trigger has an inverter-like voltage transfer characteristic, but with two different logic threshold voltages for increasing and for decreasing input signals.
- With this unique property, the circuit can be utilized for the detection of low-to-high and high-to-low switching events in noisy environments.



Working

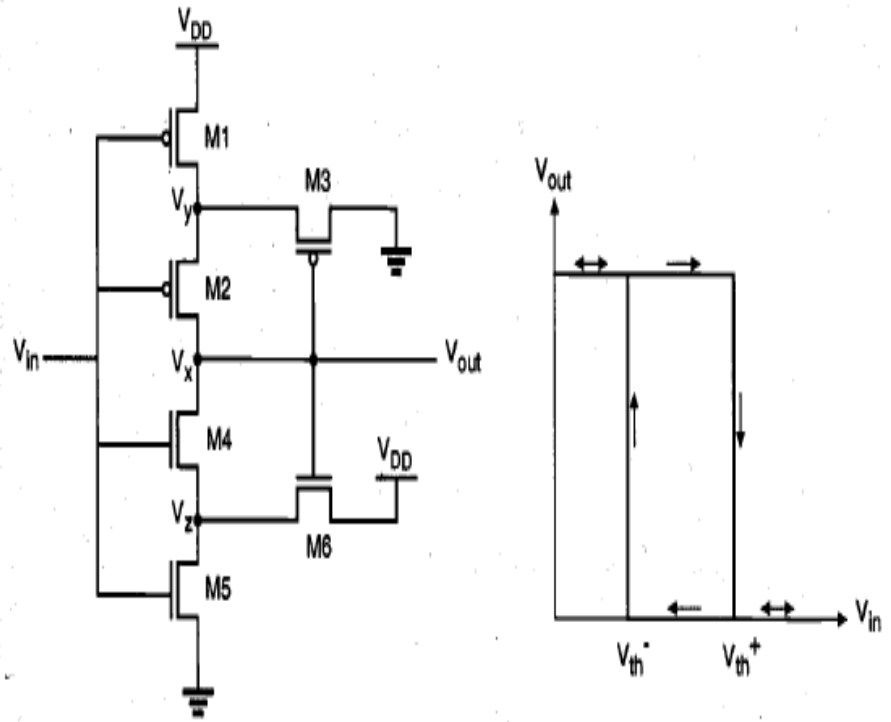
We start our step-by-step analysis by considering a positive input sweep, i.e., assuming that the input voltage is increasing from 0 to VDD.

i) At V_{in}= 0V: M1 and M2 are turned on, then $V_X = V_Y = V_{DD}$=5V At the same time, M4 and M5 are turned off. M3 is off; M6 is on and operates in the saturation region. Calculating the threshold voltage of M6 with $2\Phi_F$ =-0.6 V, $V_z=V_{DD-}V_{T6}$=3.5 V

ii) At $V_{in} = V_{t0}$ = 1.0 V: M5 starts to turn on, M4 is still off. V_x = 5 V

iii) At V_{in} = 2.0 V: Assume M4 is off, while both M5 and M6 operate in the saturation region.

iv) At V_{in}= 3.5V: V_z Continues to decrease. Assuming M5 in linear region and M6 in saturation



Working

Next, we consider a negative input sweep, i.e., assume that the input voltage is decreasing from VDD to 0.

i) At Vin =5.0 V: M4 and M5 are on, so that the output voltage is V, = 0 V. The pMOS transistors MI and M2 are off, and M3 is in saturation, thus

ii) At Vi, = 4.0 V: M1 is at the edge of turning on, M2 is off, and M3 is in saturation. The output voltage is still unchanged

iii) At Vi, = 3 0 V: M1 is on and in saturation region. M3 is also in saturation

It can be shown that at this point, the pMOS transistor M2 is already turned on. Consequently, the output voltage is being pulled up to VDD. We conclude that the lower logic threshold voltage V_{th} is approximately equal to 1.5 V