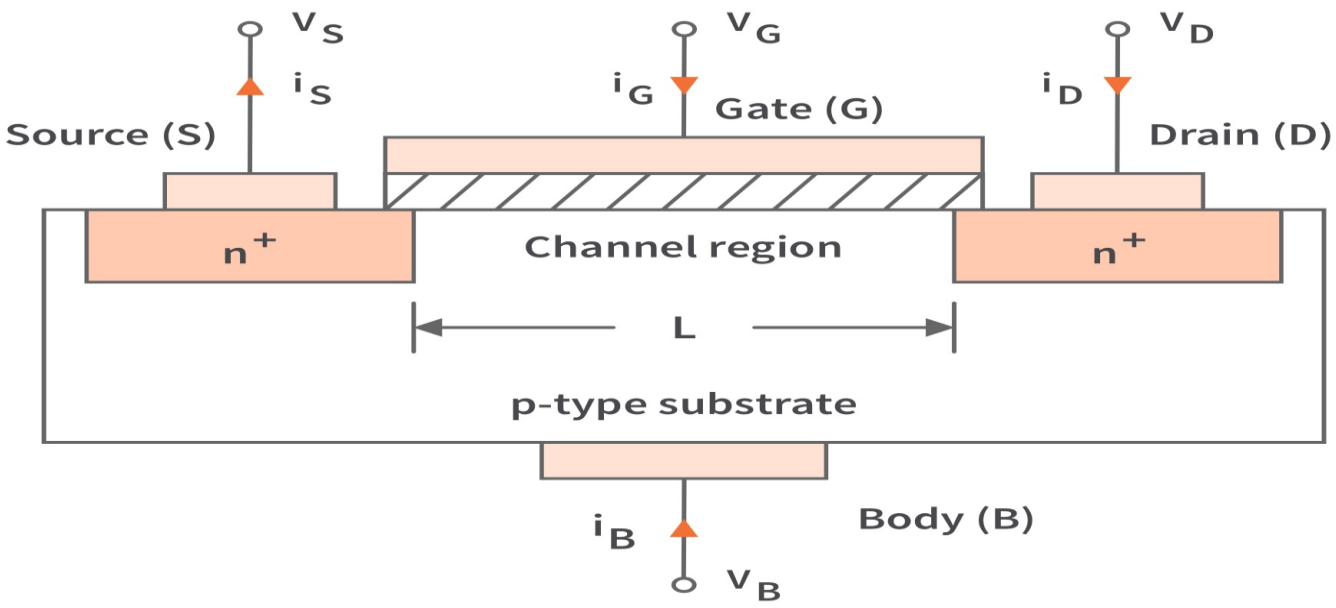
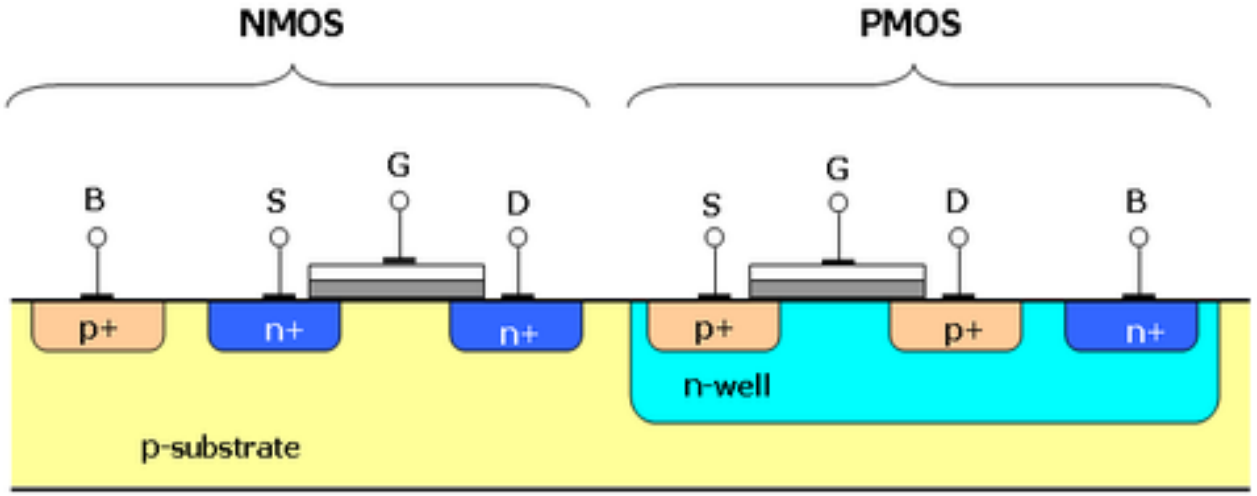
ECE318:CMOS VLSI Design

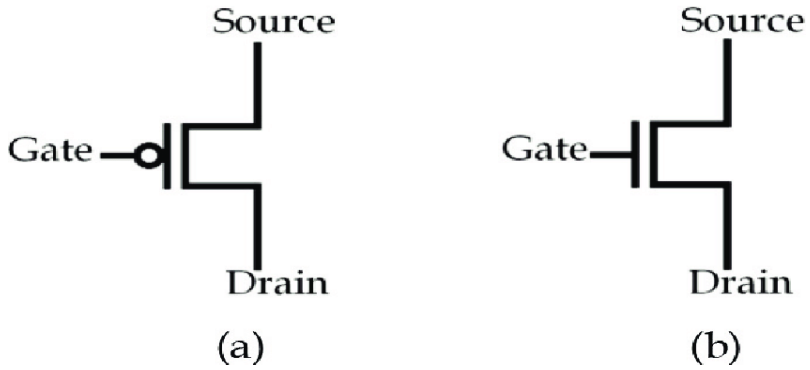
Unit 1

MOS Transistor

MOSFET Structure

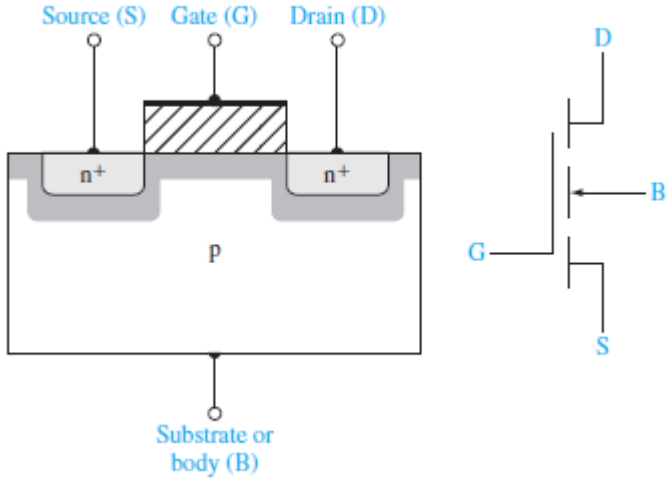




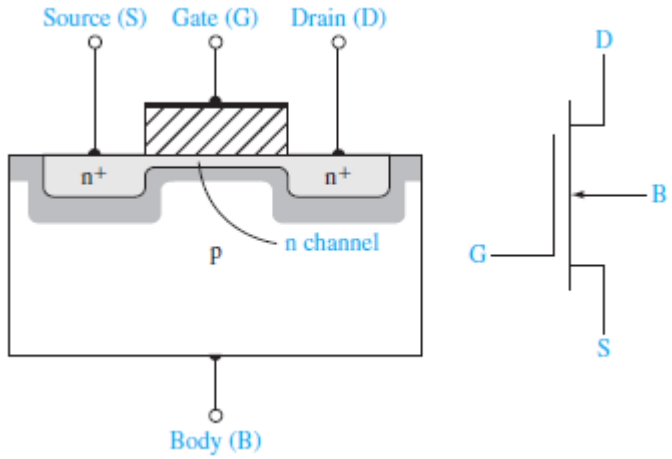


N-channel MOSFET

- nMOSFET



a) Cross section and circuit symbol for an n-channel enhancement mode MOSFET



b) Cross section and circuit symbol for an n-channel depletion mode MOSFET.

BJT Vs MOSFET

- BJT provide more drive current and therefore high speed IC
- MOSFET provide less drive current compared to BJT
- MOSFET offer very high input impedance at gate so it takes very low input current (Ig=0)
- Power consumption is less in MOSFET
- BJT is bipolar device and MOSFET unipolar
- BJT is current controlled and MOSFET is voltage controlled device
- BJT is less stable for temperature compared to MOSFET

MOSFET Operation

- When VDs increases to the point where the potential drop across the oxide at the drain terminal is equal to VT, the induced inversion charge density is zero at the drain terminal. This effect is schematically shown in Fig.
- At this point, the incremental conductance at the drain is zero, which means that the slope of the Id versus Vds curve is zero. Vds(sat)=Vgs-VT

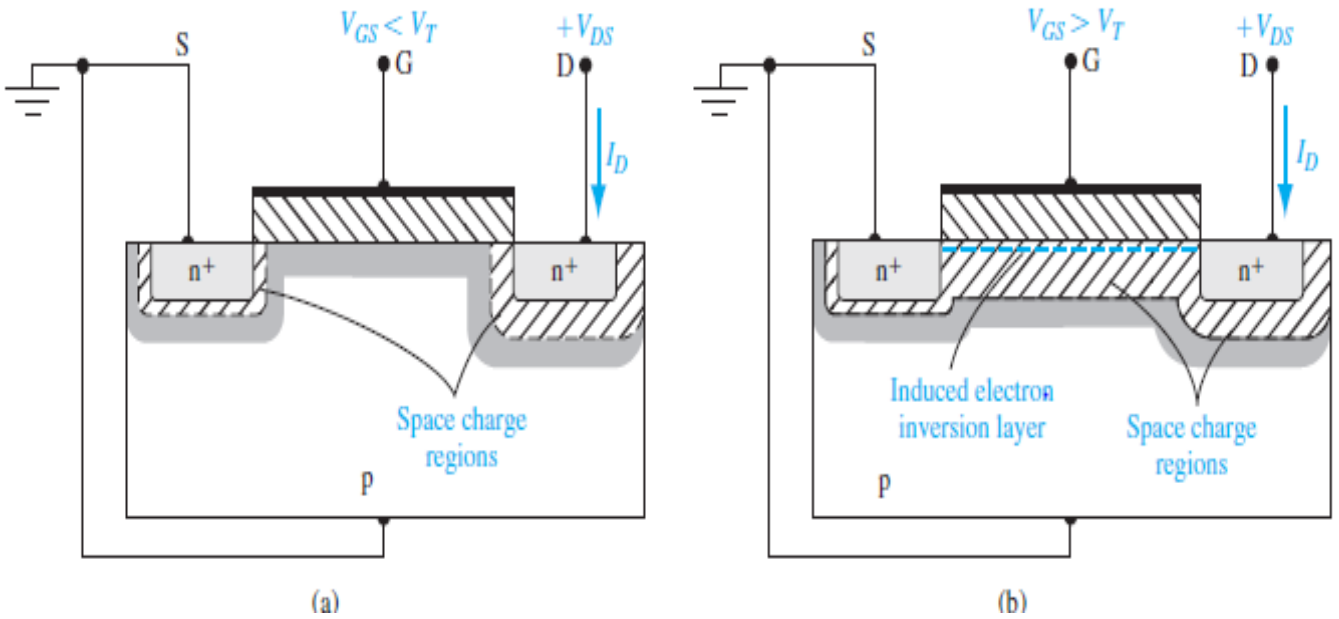


Fig: n-channel enhancement mode MOSFET (a) with an applied gate voltage *VGS* <*VT* and (b) with an applied gate voltage *VGS* >*VT*.

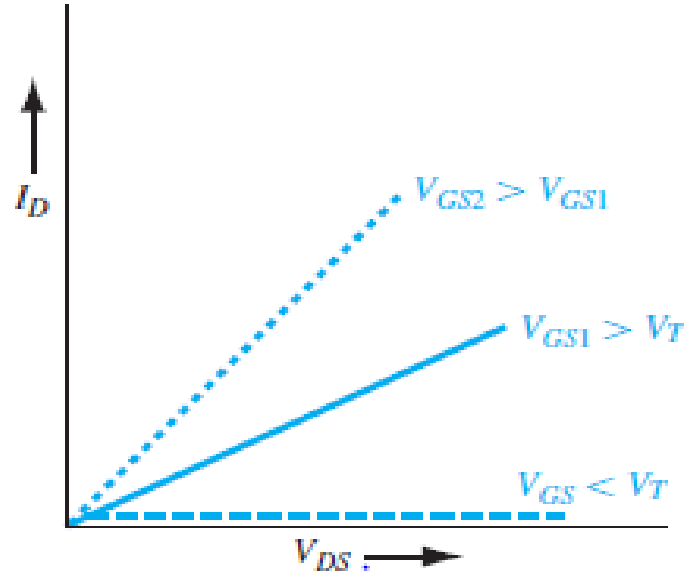


Fig. ID versus *VDS* characteristics for small values of *VDS* at three *VGS* voltages.

MOSFET Operations

$$V_{GS} - V_{DS}(\text{sat}) = V_T$$

$$V_{DS}(\text{sat}) = V_{GS} - V_T$$

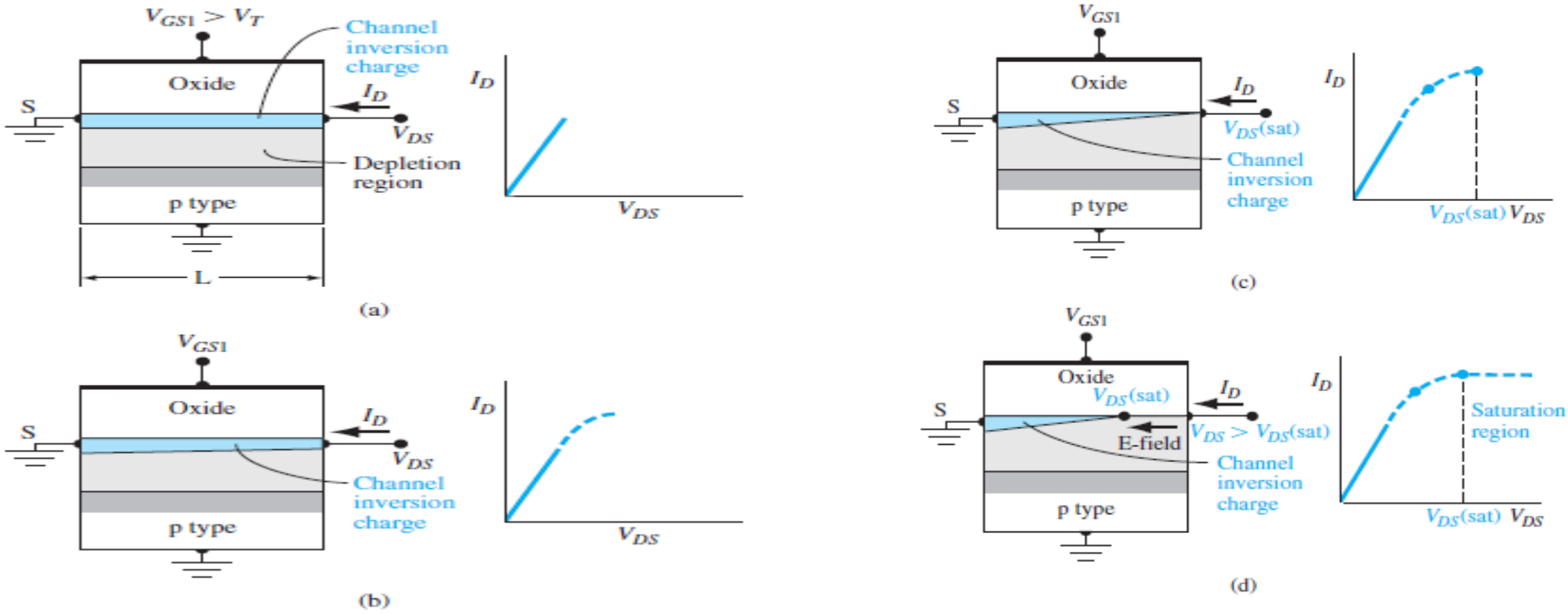


Fig. Cross section and Id versus Vds curve when Vgs> VT for (a) a small V_{DS} value, (b) a larger *Vds* value, (c) a value of *Vds*=*Vds*(sat), and (d) a value of Vds>Vds(sat).

MCQ

Q1. The basic advantage of the CMOS technology is that
a) It is easily available
b) It has small size
c) It has lower power consumption
d) It has better switching capabilities

Q2.The N-channel MOSFET is considered better than the P-channel MOSFET due to its
a) low noise levels
b) TTL compatibility
c) lower input impedance
d) faster operation

Q3. Consider an ideal MOSFET. If Vgs = 0V, then Id = ?
a) Zero
b) Maximum
c) Id(on)
d) Idd

MCQ

Q3. In saturation region, MOSFET act as

a) closed switch

b) open switch

c) amplifier

d) oscillator

Q4. In linear region, drain current is proportional to

a) (Vgs-Vt)

b) Vds

c) Vgs

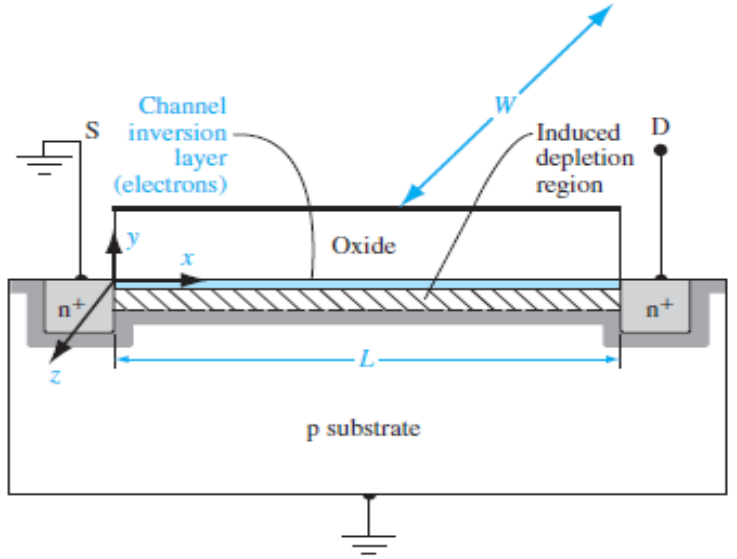
d) Vt

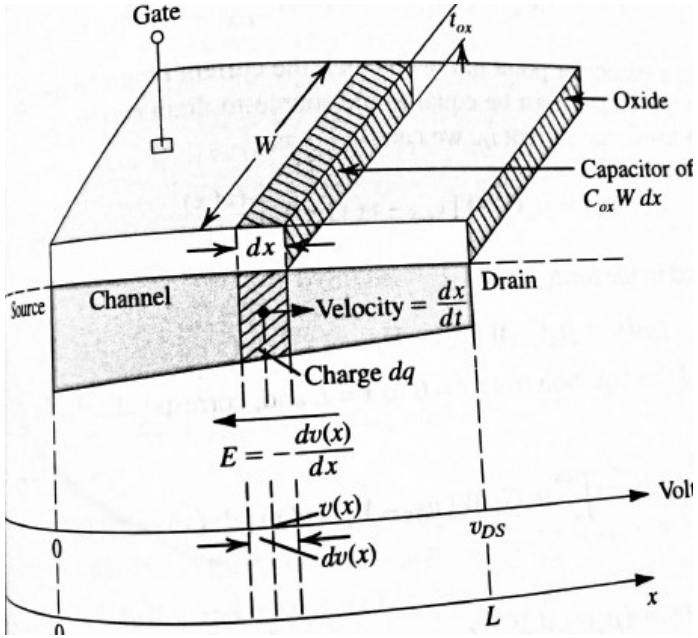
Q5.Channel depletion in p-type substrate occurs at

a) 0<Vgs<Vt b) Vgs>Vt c) Vgs<0 d) None of the above

Derivation of I_d vs V_{ds}

- Consider a small strip of thickness dx in x-direction. V_x is drift velocity and Cox is oxide capacitance per unit area and Vt threshold voltage.
- Consider $C_{ox}=\frac{\in_{ox}}{t_{ox}}$
- Where $\in_{ox}$(=3.45x10^{-11}F/m) permittivity of SiO_2 and t_{ox} oxide thickness
- $v_x = \frac{dx}{dt}$ drift velocity in x-direction





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Electron charge dq in infinitesimal thickness dx

$dq = -C_{ox}\mathrm{W}\mathrm{dx}[(\mathrm{V_{gs}}\text{-}\mathrm{V_x}) - \mathrm{Vt}]$

Since Electric Field in x-direction $E_x = -\frac{dV_x}{dx}$

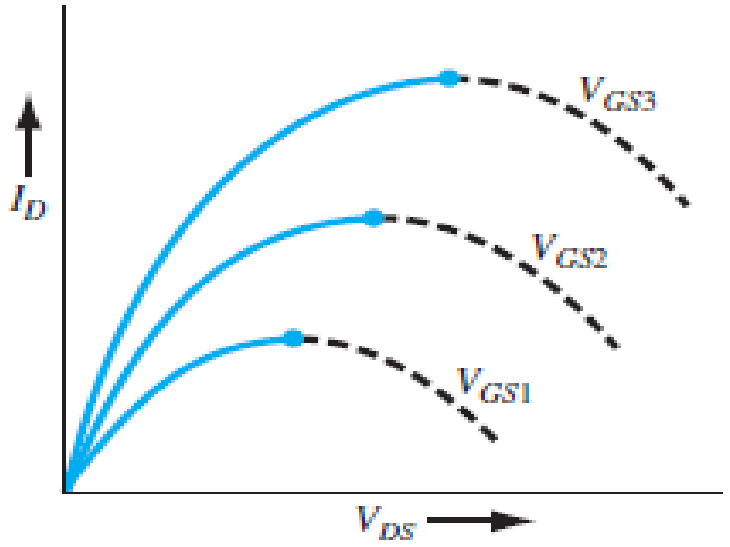
$\frac{dx}{dt}=v_x=-\mu_n E_x=\mu_n \frac{dV_x}{dx}$

$i_x=\frac{dq}{dt}=\frac{dq}{dx}\frac{dx}{dt}$

$i_d=-i_x=C_{ox}\mathrm{W}[(\mathrm{V_{gs}}\text{-}\mathrm{V_x}) - \mathrm{Vt}]\,\mu_n \frac{dV_x}{dx}$

$\int_0^L i_d dx = \mu_n C_{ox}\mathrm{W}\int_0^{V_{ds}}[(\mathrm{V_{gs}}-\mathrm{Vt}) - \mathrm{V_x}]\mathrm{d}V_x$

$\boldsymbol{i_d=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{gs}-V_t)V_{ds}\text{-}V_{ds}^{\,2}]}$



contd.

- Drain Current in saturation region, can be expressed as:

$$i_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[V_{gs} - V_t]^2$$

Id Versus Vds Curve

- When the V_{DS} value increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases.

- The incremental conductance of the channel at the drain decreases, which then means that the slope of the I_D versus V_{DS} curve will decrease. This effect is shown in the I_D versus V_{DS} curve in the fi gure.

$$V_{GS} - V_{DS}(\text{sat}) = V_T$$

$$\boxed{V_{DS}(\text{sat}) = V_{GS} - V_T}$$

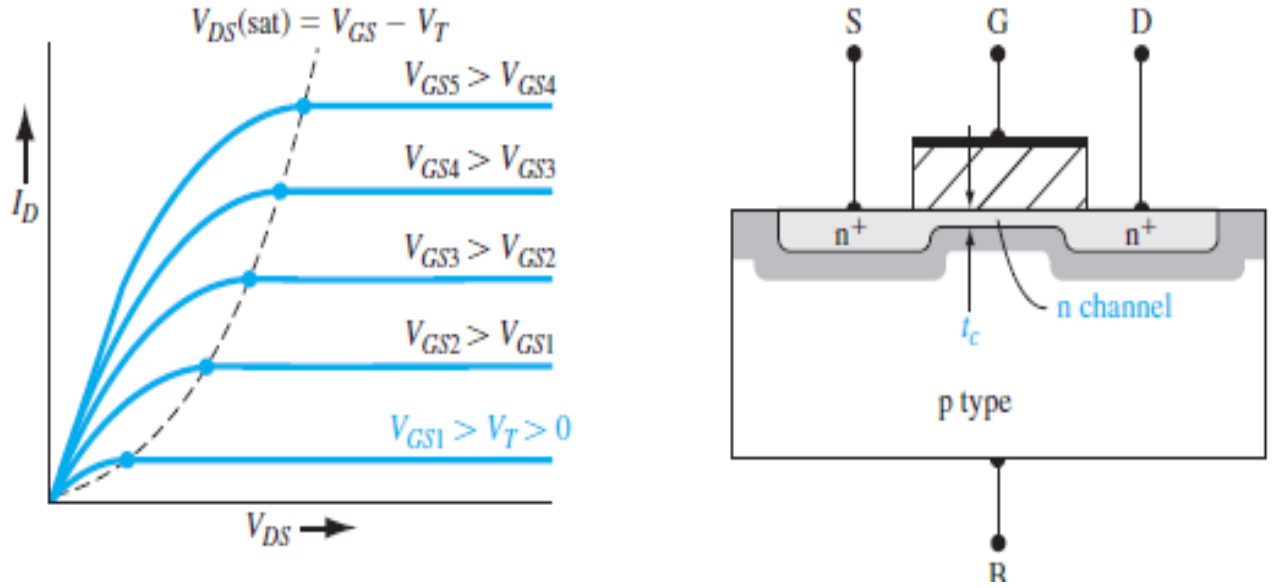


Fig. a) Id vs Vds b) n-channel MOSFET

Id vs Vds

- When V_{GS} changes, the I_D versus V_{DS} curve will change. We saw that, if V_{GS} increases, the initial slope of I_D versus V_{DS} increases.
- For MOSFET in linear:

$$I_D = \frac{W\mu_n C_{ox}}{2L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]$$

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot \left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]$$

$$I_D = K_n\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]$$

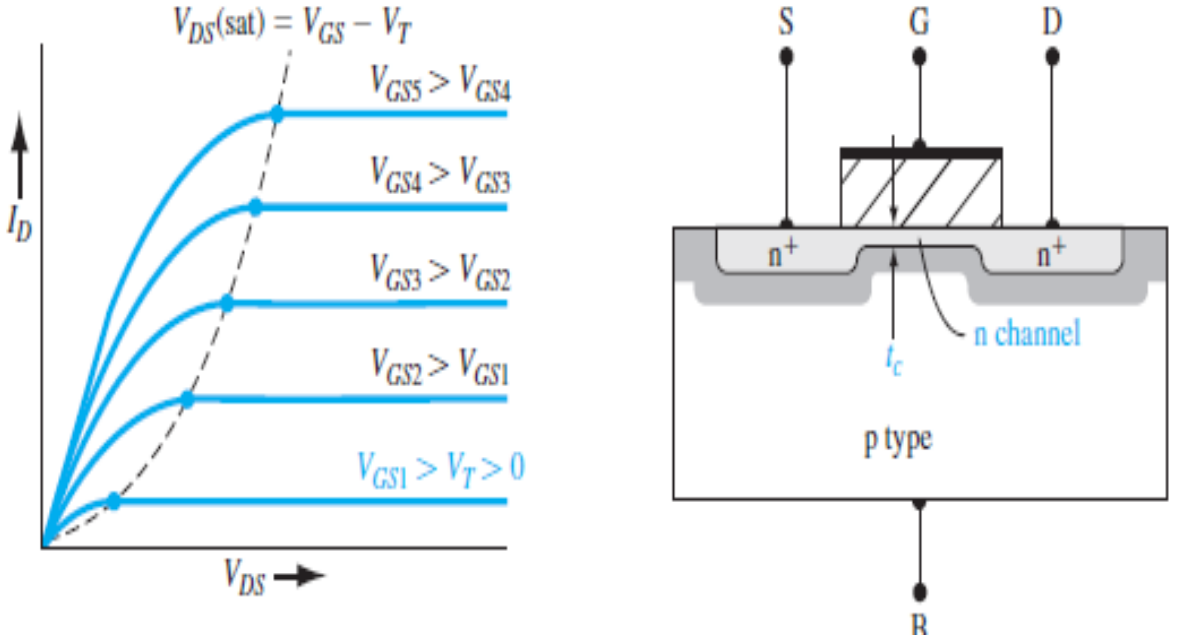


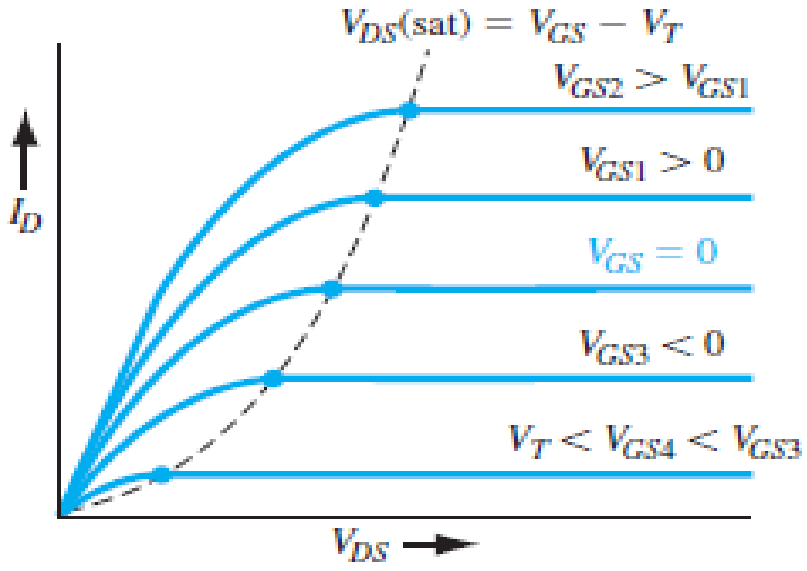
Fig. Family of I_D versus V_{DS} curves for an n-channel depletion mode MOSFET.

MOSFET in Saturation

$$I_D = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2$$

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

$$I_D = K_n(V_{GS} - V_T)^2$$



Transconductance

- Transconductance
- $g_m = \frac{\partial I_D}{\partial V_{gs}}$
- $g_m = \frac{W \boldsymbol{\mu}_n C_{ox}}{L} V_{ds}$

Flat Band voltage

- *Flat band voltage* is defined as the applied voltage such that there is no band bending in the semiconductor and as a result zero net space charge in this region.

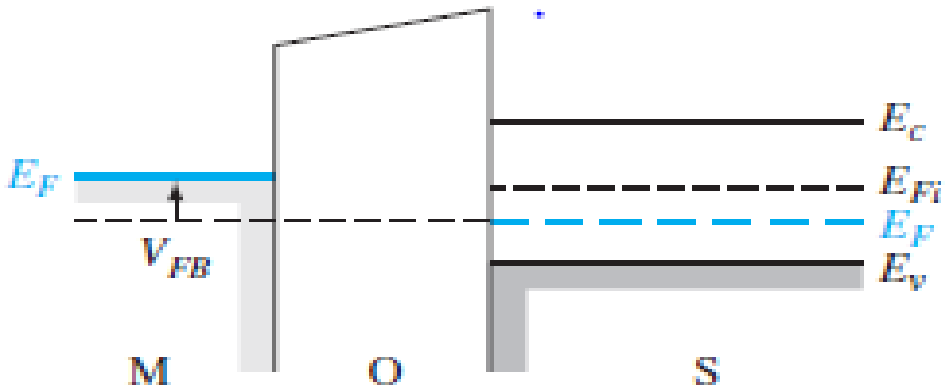
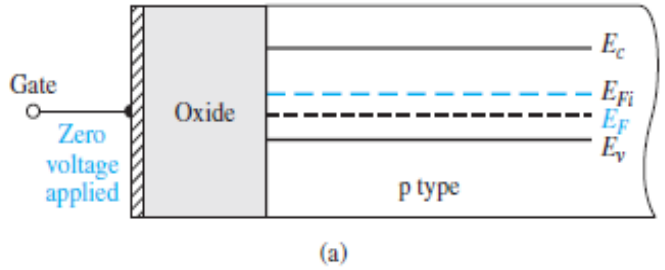


Fig. Energy-band diagram of a MOS capacitor at flat band.

Energy Band Diagram

N-channel MOSFET with P-type substrate



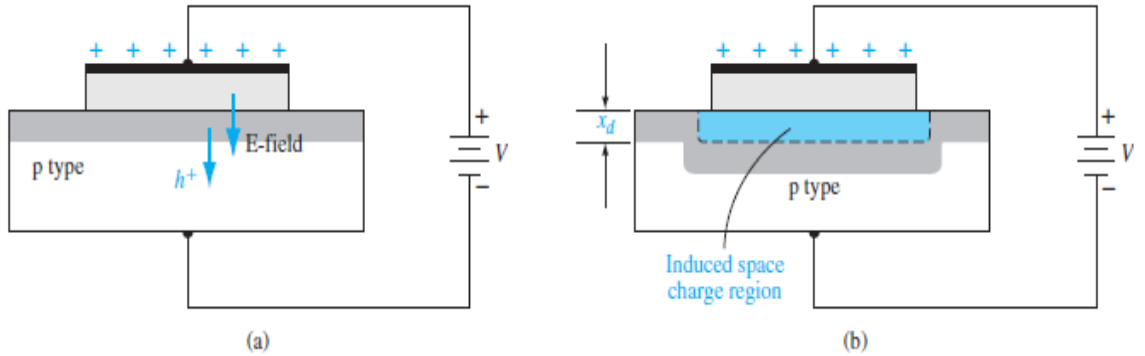


Fig. MOS capacitor with a moderate positive gate bias, showing (a) the electric fi eld and charge flow and (b) the induced space charge region.

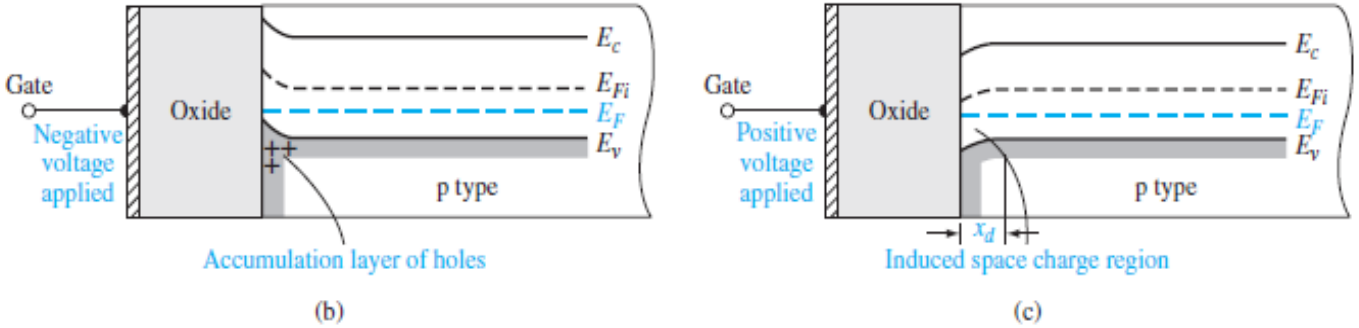


Fig. Energy-band diagram of a MOS capacitor with a p-type substrate for (a) a zero applied gate bias showing the *ideal* case, (b) a negative gate bias, and (c) a moderate positive gate bias

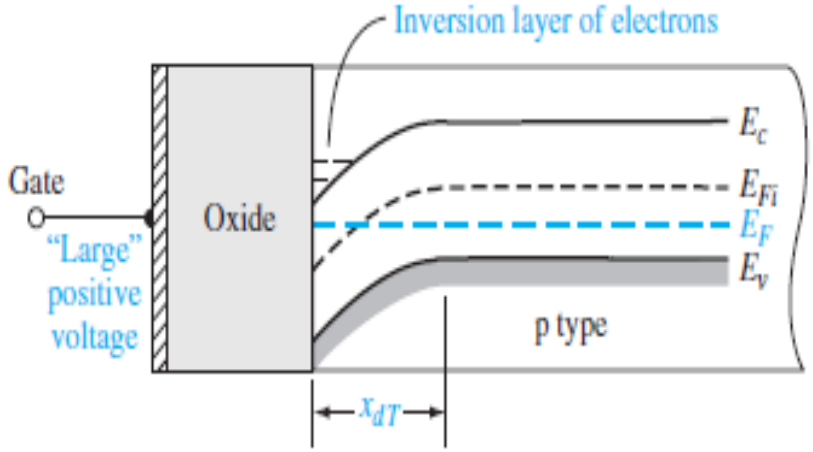


Fig. Energy-band diagram of the MOS capacitor with a p-type substrate for a "large" positive gate bias.

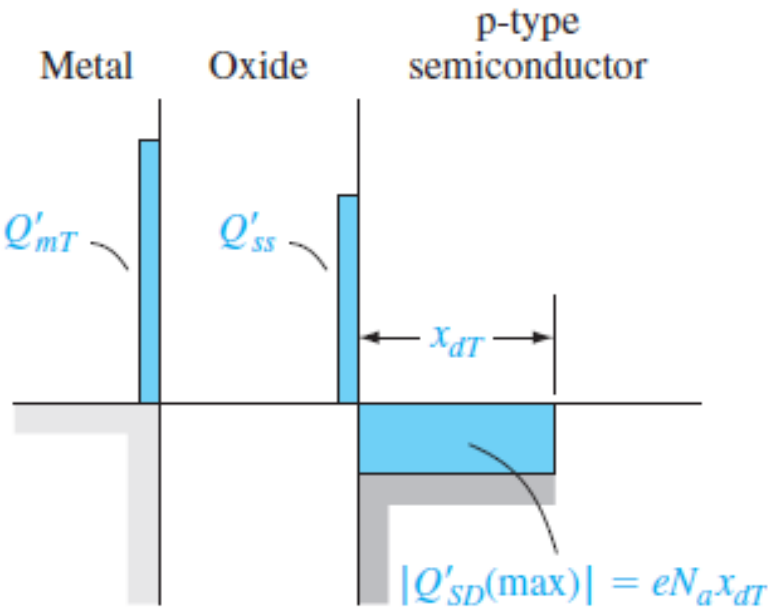
Threshold Voltage

- The threshold voltage is defined as the applied gate voltage required to achieve the threshold inversion point.
- The threshold inversion point, in turn, is defined as the condition when the surface potential is $\phi s = 2\phi fp$ for
- Here Q'ss equivalent oxide charge and Q'mt positive charge on metal gate at threshold.

$$|Q'_{SD}(\max)| = eN_a x_{dT}$$

$$V_{TN} = \frac{|Q'_{SD}(\max)|}{C_{ox}} + V_{FB} + 2\phi_{fp}$$

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$



Charge distribution in a MOS capacitor with a p-type substrate at the threshold inversion point.

Substrate Bias Effects

- In MOSFET circuits the source and body may not be at the same potential.
- Considering the charge neutrality condition through the MOS structure, the positive charge on the top metal gate must increase to compensate for the increased negative space charge in order to reach the threshold inversion point. So when *Vsb* > 0, the threshold voltage of the n-channel MOSFET increases.

$$\Delta V_T = -\frac{\Delta Q'_{SD}}{C_{ox}} = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}}\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

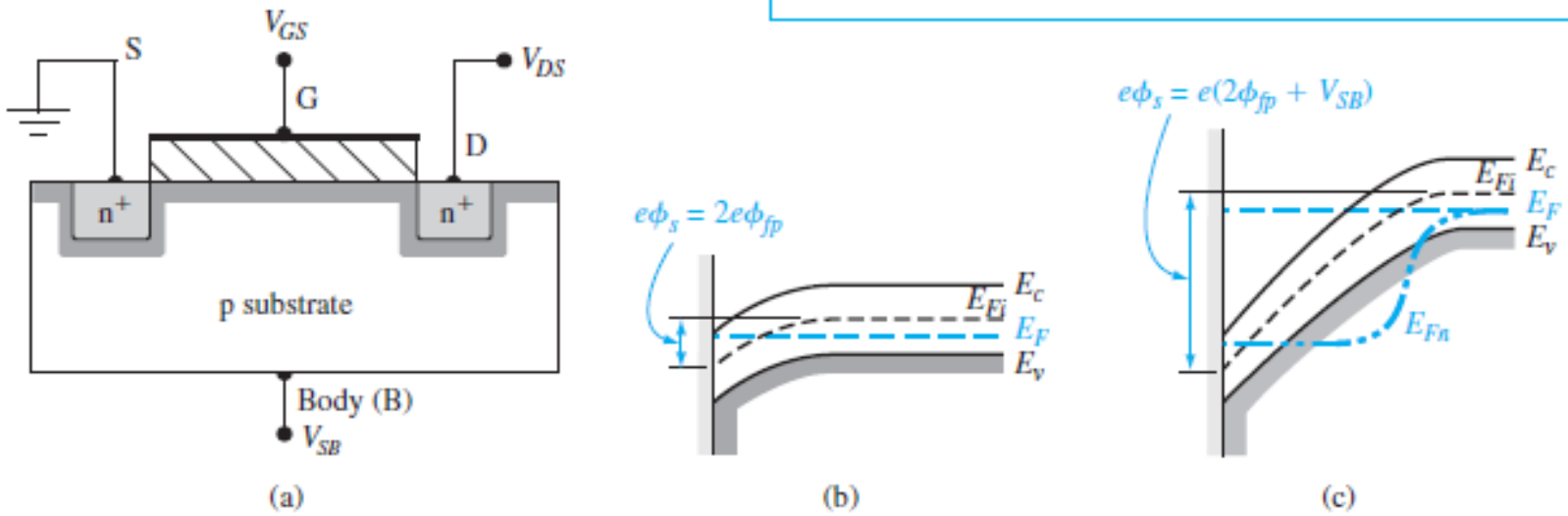


Fig. (a) Applied voltages on an n-channel MOSFET. (b) Energy-band diagram at inversion point when V_{SB}=0. (c) Energy-band diagram at inversion point when V_{SB}>0 is applied.

Frequency Limitations and Equivalent circuit

- small-signal equivalent circuit for the MOSFET is needed in order to mathematically analyze electronic circuit.
- Model is based on the inherent capacitances and resistances
- The equivalent circuit contains capacitances and resistances introduce frequency effects.

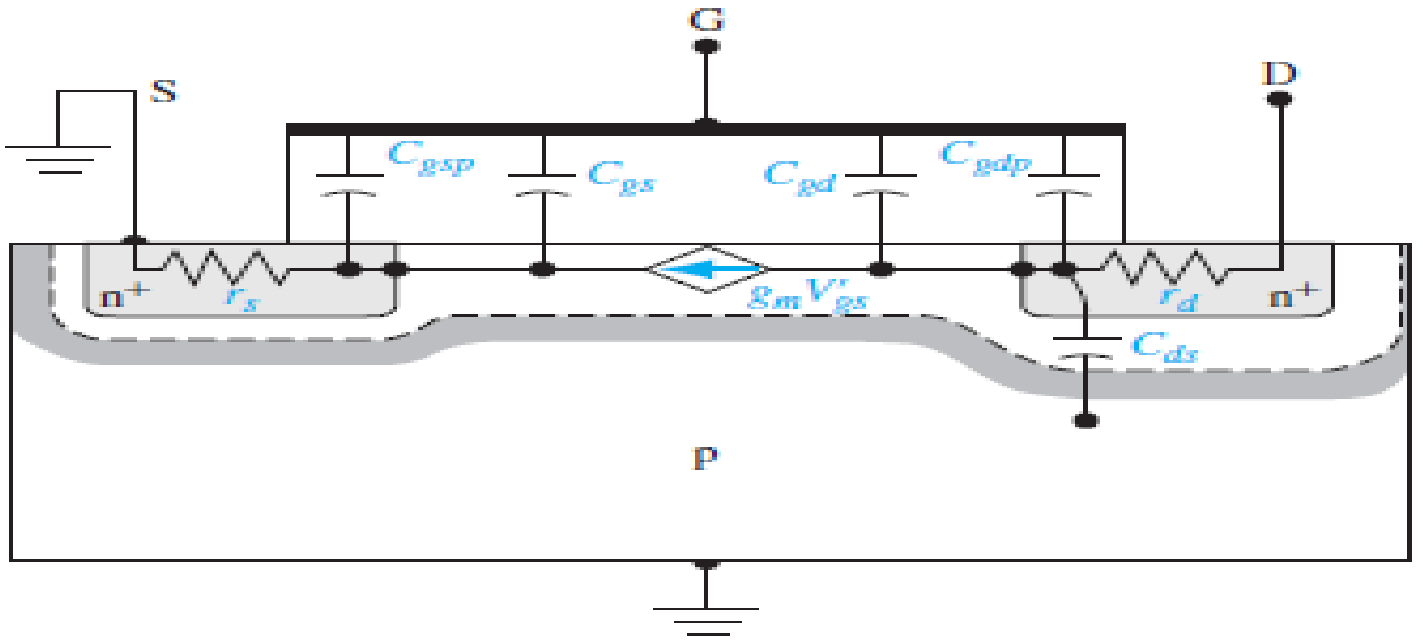


Fig. Inherent resistances and capacitances in the n-channel MOSFET structure.

Equivalent circuit

- The voltage V'_{gs} is the internal gate-to-source voltage that controls the channel current. The parameters C_{gsT} and C_{gdT} are the total gate-to source and total gate-to-drain capacitances.
- This resistance is associated with the slope I_D versus V_{DS}. In the ideal MOSFET biased in the saturation region, I_D is independent of V_{DS} so that r_{ds} would be infinite.
- In short-channel-length devices, in particular, r_{ds} is finite because of channel length modulation

$$I_d = g_m V'_{gs}$$

$$V_{gs} = V'_{gs} + (g_m V'_{gs}) r_s = (1 + g_m r_s) V'_{gs}$$

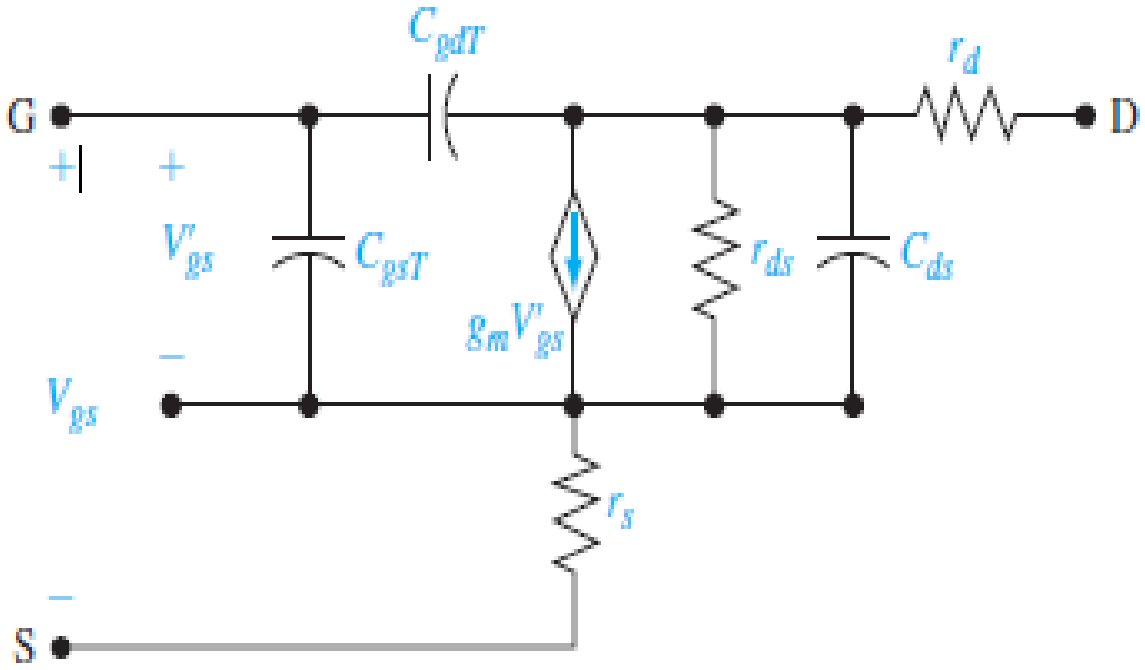


Fig. Small-signal equivalent circuit of a common source n-channel MOSFET.

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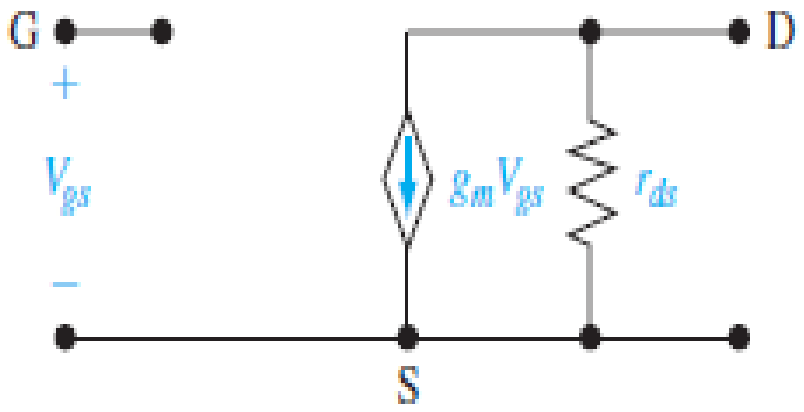
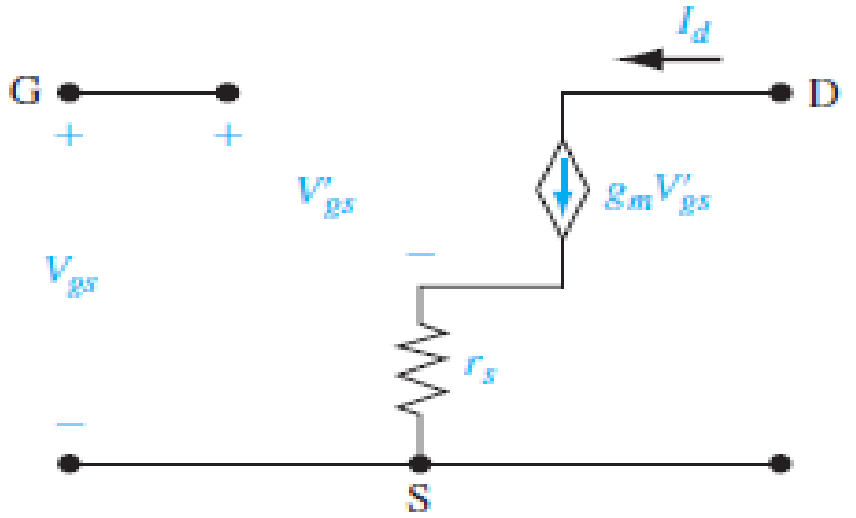
- Fig. Simplified, low-frequency small-signal equivalent circuit of a common-source n-channel MOSFET.



a) Simplified, low frequency small-signal equivalent circuit of common-source n-channel MOSFET including source resistance *rs*.



b) Simplified, low frequency small-signal equivalent circuit of common-source n-channel MOSFET including source resistance r_s.

MCQ

Short channel effects have substantial adverse effect in transistor of

a) 180nm technology node

b) 90nm technology node

c) greater than 45nm technology node

d) less than 45nm technology node

Most commonly used insulating material in MOSFET

a) Al_2O_3

b) SiO_2

c) As_2O_5

d) GeO_2

MCQ

Flat band potential can be expressed as

a) φ_{ms}

b) $\varphi_{ms}-Q_{ss}/C_{ox}$

c) $\varphi_{ms}+Q_{ss}/C_{ox}$

d) None of the above

Review Questions

Q1. What is flat band potential?
Q2. Define MOSFET threshold voltage?
Q3. What is short channel effect?
Q4. Draw the symbol of n-channel and p-channel MOSFET.
Q5. Give current voltage relationship of MOSFET in saturation region.
Q6. Give current voltage relationship of MOSFET in linear region.
Q7. Describe channel inversion in n-channel MOSFET.
Q8. Describe channel depletion in n-channel MOSFET.
Q9. Why polysilicon is preferred in place of metal gate.
Q10. Why high-K dielectric constant insulating material is preferred in place of oxide.

Q6. MOSFET can be used as

a) Current controlled capacitor

b) Voltage controlled capacitor

c) Current controlled inductor

d) Voltage controlled inductor

Why Polysilicon?

- The threshold voltage (and consequently the drain to source on-current) is determined by the work function difference between the gate material and channel material.
- When metal was used as gate material, gate voltages were large (in the order of 3V to 5V), the threshold voltage (resulting from the work function difference between a metal gate and silicon channel) could still be overcome by the applied gate voltage (i.e. $|Vg - Vt| > 0$).
- As transistor sizes were scaled down, the applied signal voltages were also brought down (to avoid gate oxide breakdown, hot-electron reduction, power consumption reduction, etc).
- A transistor with a high threshold voltage would become non-operational under these new conditions. Thus, poly-crystalline silicon (polysilicon) became the modern gate material because it is the same chemical composition as the silicon channel beneath the gate oxide.
- In inversion, the work-function difference is close to zero, making the threshold voltage lower and ensuring the transistor can be turned on.
- Polysilicon is also more stable for temperature variations.
- In place of polysilicon we can also use high work function metals like Ni, Co, Ti and Pt etc.

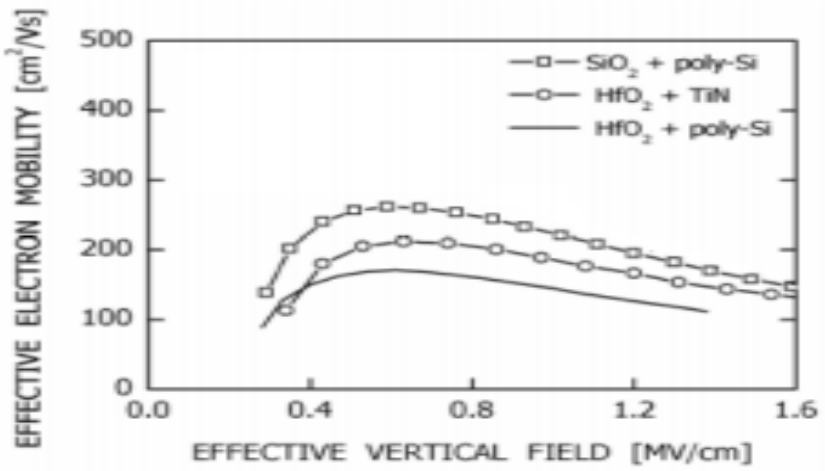
Why high-K dielectric insulating material in place of SiO_2?

The requirements of a new oxide to replace SiO2 are as follows:

- The metal oxide must have a permittivity higher than Si, industry targets values nearly between 15 to 20.
- Aiming towards less leakage of current, the material should allow less leakage current.
- Density of defects must be less
- The oxide is in constant contact with Si and hence must be thermodynamically stable with it.
- High breakdown field and low loss factor .

Drawback: High-K degrade mobility due high threshold voltage.

High-K Material	*K-value*	*Gap (eV)*
Si	3.9	1.1
SiO2	3.9	9
Si3N4	7	5.3
Al2O3	9	8.8
Ta2O5	22	4.4
TiO2	80	3.5
ZrO2	25	5.8
HfO2	25	5.8



Energy band and energy bond

- **Energy Band diagram:** It gives information about valence band, conduction band and band gap which important to categorise semiconductor and their performances.
- Bond Energy: Bond energy is **directly related to the melting temperature of solids**.
- For different types of bonds, the melting temperature scales with the bond energy. Both ionic (e.g. NaCl, MgO) and covalent bonds (e.g. Si, C) have high bond energies and consequently high melting temperature.

Query??

School of Electronics and Electrical Engineering, Lovely Professional University is going to organize a Hackathon on 16 and 17 Feb 2024. This Hackathon will be a great opportunity for students, developers, designers, and entrepreneurs to explore the potential and create innovative applications and products.
Important points1.

There will be two categories (Software group and Hardware group)2. There will be a registration fee of Rs. 2000/- for each team .
Prizes
The winning team of the Hackathon will receive cash prizes as well as certificate.

For more information and registration pls visit:
https://www.lpu.in/events/hack-iot/index.php