ECE318:CMOS VLSI Design

Unit 3

MOS Inverters

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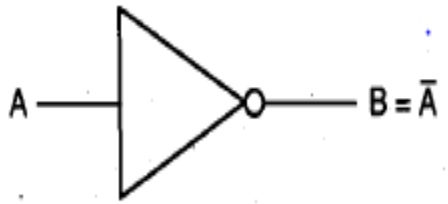
Inverter

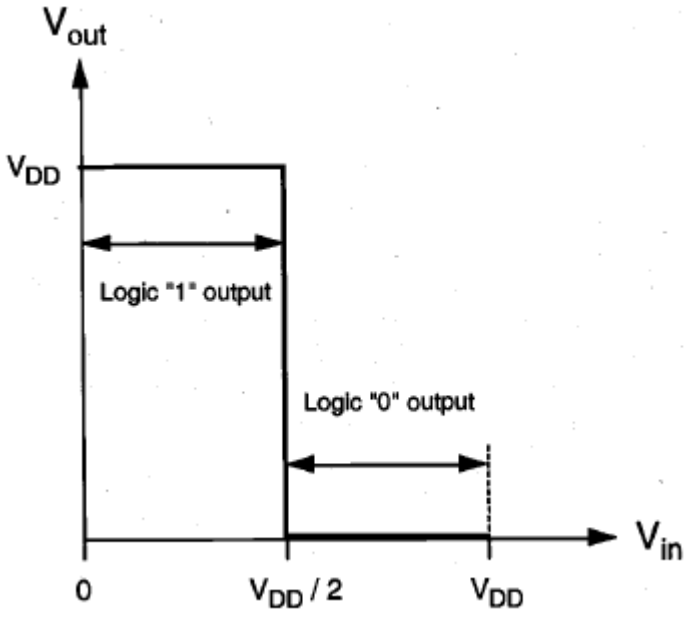
- *I*nverter is the most fundamental logic gate that performs a Boolean operation on a single input variable.
- Ideal Inverter: The voltage *Vth* is called the *inverter threshold voltage.*
- *F*or any input voltage between 0 and $V_{th} = V_{DD}/2$, the output voltage is equal to V_{DD} (logic" 1 *). The output switches to* 0 when the input is equal to V_{th}
- Voltage transfer characteristic (VTC) of the ideal inverter is shown in Fig



Symbol

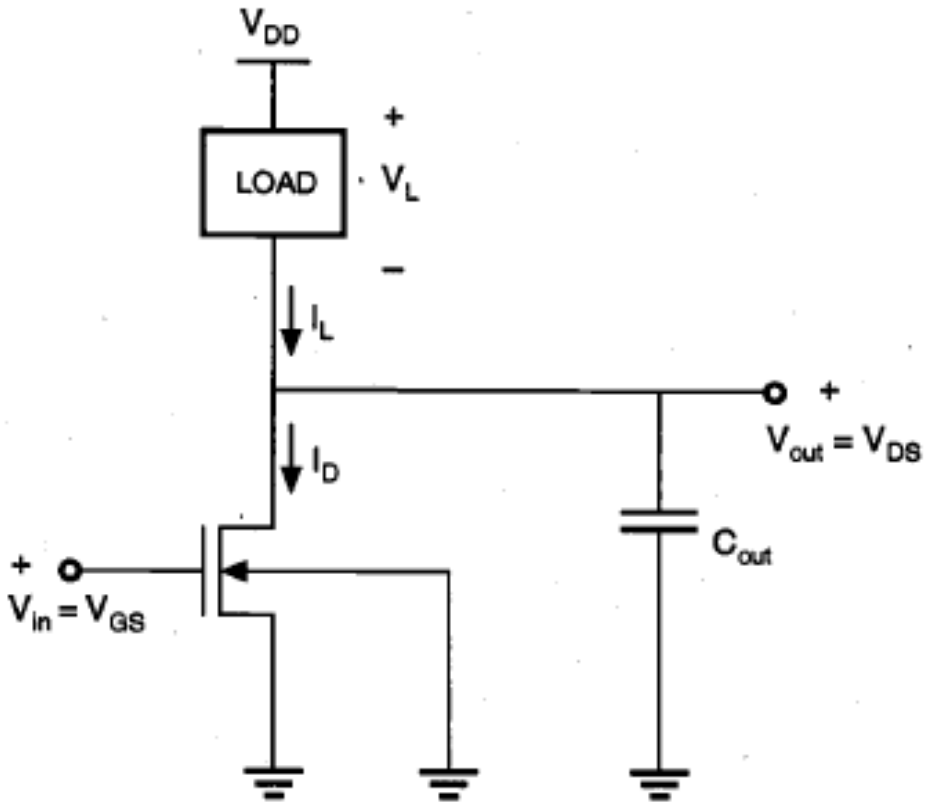
A	B
0	1
1	0

Truth Table



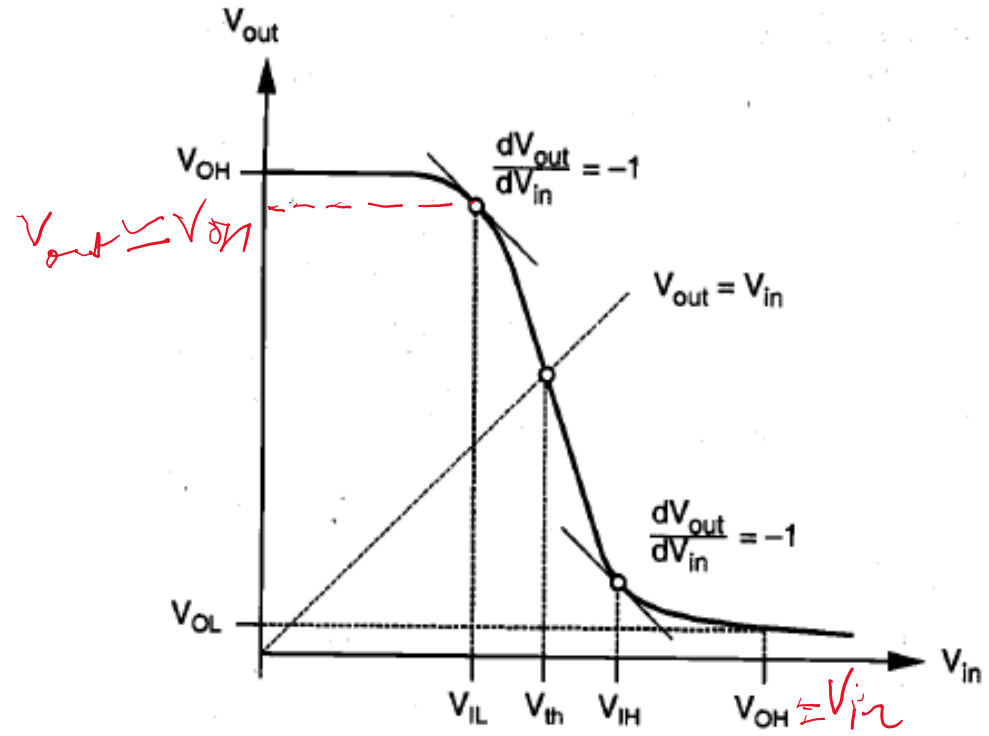
NMOS Inverter

- NMOS inverter
- C_{out} is load capacitance
- DC gate current of an MOS transistor is negligible for all practical purposes, there will be no current flow into or out of the input and output terminals of the inverter in DC steady state.



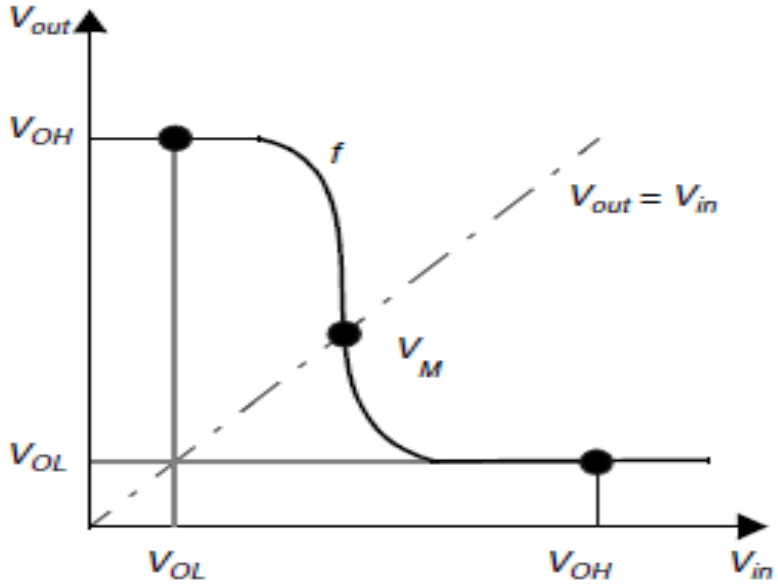
Voltage Transfer Characteristic **(VTC)**

- VTC of realistic inverter
- ***V_{OH}:*** Maximum output voltage when the output level is logic " 1"
- ***V_{OL}:*** Minimum output voltage when the output level is logic "0"
- ***V_{IL}:*** Maximum input voltage which can be *interpreted* as logic "0"
- ***V_{IH}:*** Minimum input voltage which can be *interpreted* as logic " 1“
- *Inverter threshold voltage Vt.,* which is considered as the transition voltage, is defined as the point where $V_{in} = V_{out}$, on the VTC



Voltage-Transfer Characteristic

- The electrical function of a gate is best expressed by its *voltage-transfer characteristic* (VTC) (sometimes called the *DC transfer characteristic*), which plots the output voltage as a function of the input voltage
- The gate threshold voltage presents the midpoint of the switching characteristics, which is obtained when the output of a gate is short-circuited to the input.



VIL VIH

Noise Margin

Noise Margins

- For a gate to be robust and insensitive to noise disturbances, it is essential that the "0" and "1" intervals be as large as possible.
- A measure of the sensitivity of a gate to noise is given by the noise margins *NML* (*noise margin low*) and *NMH* (*noise margin high*), which quantize the size of the logic "0" and "1", respectively.
- The maximum threshold on the noise value:

$$\mathbf{NML=V_{IL}-V_{OL}}$$

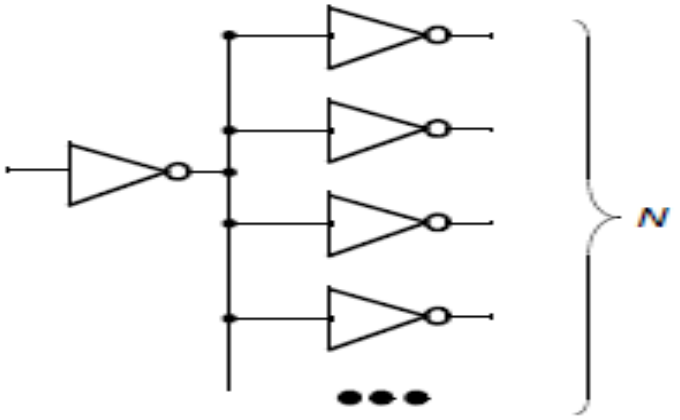
$$\mathbf{NMH=V_{OH}-V_{IH}}$$

The noise margins represent the levels of noise that can be sustained when gates are cascaded.

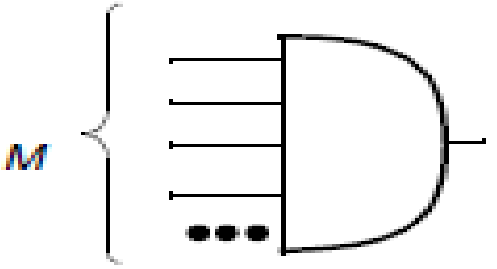
Noise immunity, on the other hand, expresses the ability of the system to process and transmit information correctly in the presence of noise

Fan-In and Fan-Out

- The *fan-out* denotes *the number of load gates N that are connected to the output of the driving gate (Fig.a).*
- Increasing the fan-out of a gate can affect its logic output levels.
- From the world of analog amplifiers, this effect is minimized by making the input resistance of the load gates as large as possible (minimizing the input currents) and by keeping the output resistance of the driving gate small (reducing the effects of load currents on the output voltage).
- When the fan-out is large, the added load can deteriorate the dynamic performance of the driving gate.
- The *fan-in* of a gate is defined as the *number of inputs* to the gate (Fig.b). Gates with large fan-in tend to be more complex, which often results in inferior static and dynamic properties.



(a) Fan-out *N*



(b) Fan-in *M*

Performance

Clock period (*clock cycle time)*, or its rate (*clock frequency*):

The minimum value of the clock period for a given technology and design is set by a number of factors such as:

- time it takes for the signals to propagate through the logic
- time it takes to get the data in and out of the registers,
- uncertainty of the clock arrival times.

Propagation delay tp of a gate defines how quickly it responds to a change at its input(s).

It expresses *the delay experienced by a signal when passing through a gate*. It is measured between the 50% transition points of the input and output waveforms

t_{pLH}= response time of gate from low to high transition

t_{pHL}= response time of gate from high to low transition

Hence, the propagation delay $t_p = \frac{t_{pLH}+t_{pHL}}{2}$

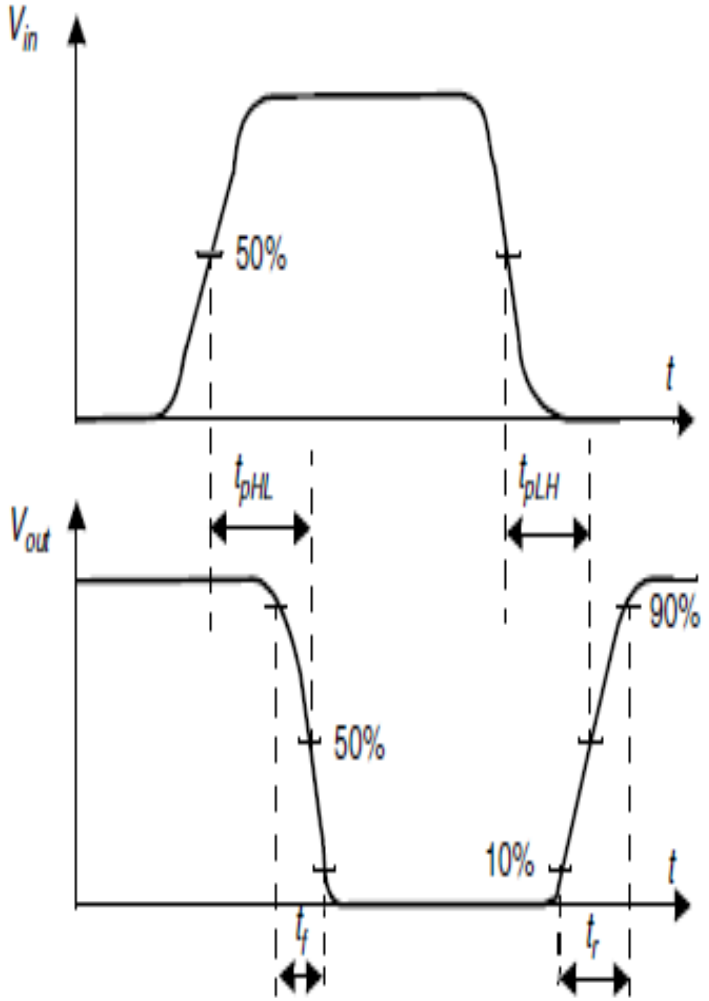


Fig. Propagationdelays and rise and fall times

MCQ

Q. Select the overall delay of a ring oscillator having N inverters with propagation delay tp of each inverter:

a) tpN
b) 2tpN
c) tpN/2
d) None

Power and Energy Consumption

- Power dissipation is an important property of a design that affects feasibility, cost, and reliability
- Two components: static power and dynamic power
- Dynamic power occurs during switching of gate. Therefore, it depends on switching frequency.
- *Higher the number of switching events, higher the dynamic power consumption.*
- $P_{peak} = I_{peak}V_{Peak} = \max[p(t)]$
- $P_{av} = \frac{1}{T}\int_0^T p(t)dt$
- **Total Power Consumption**: $P_{total} = P_{static} + P_{dynamic} + P_{short\ circuit}$

$$P_{total} = V_{dd}I_{static} + \alpha {V_{dd}}^2 C_L f_{clk} + t_{sc}V_{dd}I_{peak}f_{clk}$$

Here, α=activity factor; C_L=load capacitance; f_{clk}=clock frequency; t_{sc}=switching time

MCQ

Q3. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance?

a. Static dissipation
b. Dynamic dissipation
c. Both a and b
d. None of the above

Q4. In high noise margin (NM_H), the difference in magnitude between the maximum HIGH output voltage of driving gate and the maximum HIGH voltage is recognized by the _____gate.

a. Driven
b. Receiving
c. Both a and b
d. None of the above

Power and Area Considerations

- Issues that play significant roles in inverter design: *power* consumption and the *chip area* occupied by the inverter circuit.
- About one million logic gates can be accommodated on a very large scale integrated (VLSI) chip using 0.5 um MOS technology.
- Circuit density is expected to increase even further in future-generation chips.
- Since each gate on the chip dissipates power and thus generates heat, the removal of this thermal energy, i.e., cooling of the chip, becomes an essential and usually very expensive task.
- Junction temperature is given as
- $T_j = T_a + \theta P$
- where ***Ta*** is the ambient temperature, θ is the thermal resistance, and P is the amount of power dissipated.

Power-Delay Product

- The power-delay product (PDP) is a fundamental parameter which is often used for measuring the quality and the performance of a CMOS process and gate design.
- Product of power consumption and propagation delay is generally a constant. This product is called the ***power-delay product*** **(or PDP)** and can be considered as a quality measure for a switching device.

$$PDP = 2 P_{avg}^{*} \tau_P$$

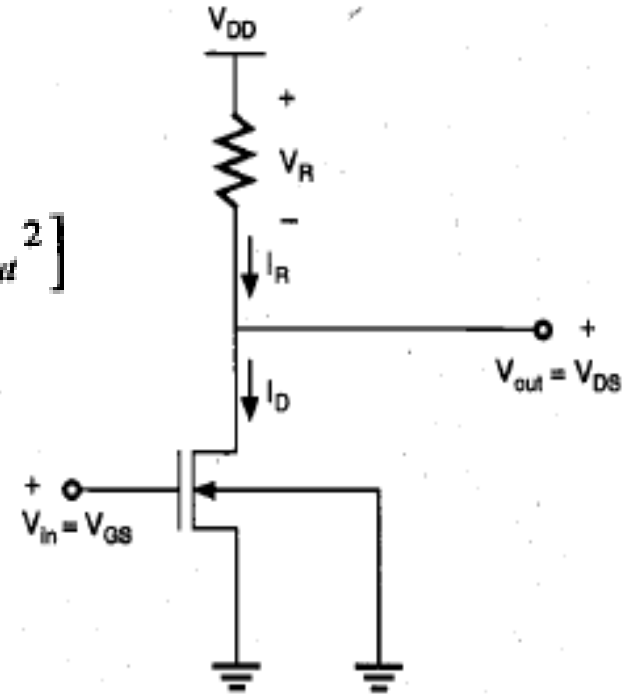
Resistive Load Inverter

- An enhancement-type nMOS transistor acts as the driver device. The load consists of a simple linear resistor, R_L.
- power supply voltage of this circuit is *VDD.*

$$I_R = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2$$

$$I_R = \frac{k_n}{2} \cdot \left[2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2\right]$$

- Driver MOSFET is initially in saturation, since its drain-tosource voltage. *(Vds = Vout)* is larger than $(V_{in} - V_{T0})$.
- At larger input voltages, the transistor remains in linear mode, as the output voltage continues to decrease.



Input Voltage Range	Operating Mode
$V_{in} < V_{T0}$	cut-off
$V_{T0} \leq V_{in} < V_{out} + V_{T0}$	saturation
$V_{in} \geq V_{out} + V_{T0}$	linear

MCQ

Q. In resistive load inverter logic 1 and logic zero of output are maintained by

a) NMOS, Resistance
b) PMOS, Resistance
c) Resistance, NMOS
d) Resistance, PMOS

VTC of a resistive-load inverter circuit

Calculation of V_{OH}

The output voltage Vt is given by

$V_{out}=V_{dd}-I_L R_L$

Since $I_R=I_L=0$

$V_{OH}=V_{dd}$

Calculation of VOL (linear)

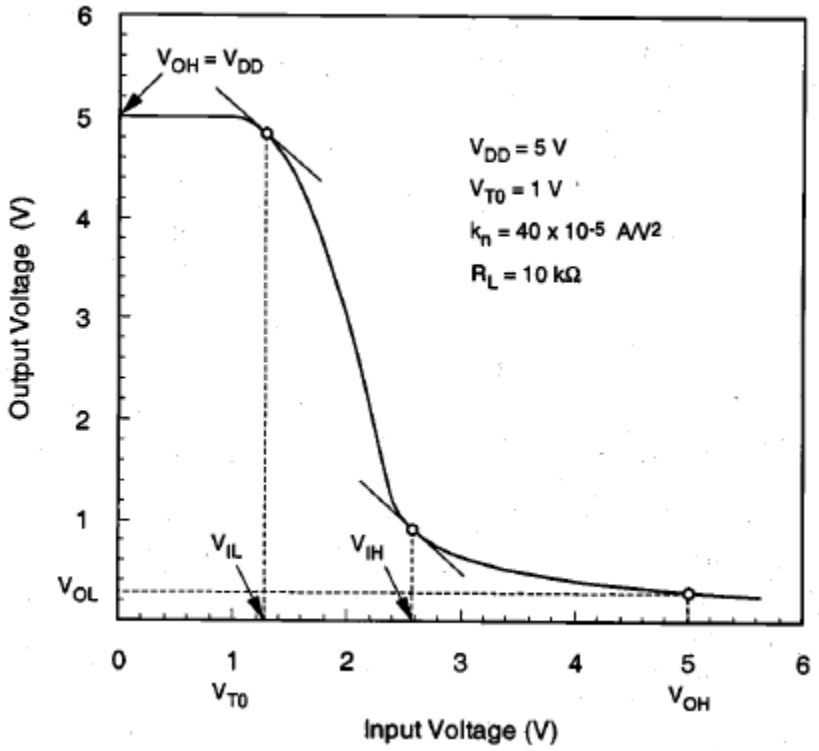
Assume $Vin = V_{OH} = V_{DD}$.

$$I_R = \frac{V_{DD} - V_{out}}{R_L}$$

Kn=µn.Cox.W/L

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n}{2} \cdot \left[2 \cdot (V_{DD} - V_{T0}) \cdot V_{OL} - V_{OL}^2\right]$$

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L}\right)^2 - \frac{2 V_{DD}}{k_n R_L}}$$



Find Roots of $ax^2 + bx + c=0$
$x = (-b \pm \sqrt{(b^2 - 4ac)})/2a$

VTC of resistive inverter(contd.)

Calculation of V_{IL}

- By definition, V_{IL} is the smaller of the two input voltage values at which the slope of the VTC becomes equal to (-1)
- $dV_{out}/dV_{in} = -1$
- $V_{out} > V_{1n} - V.,$ and the driver transistor operates in saturation. (1)

KCL for the output node.

- driver transistor operates in saturation. We start our analysis by writing the KCL for the output node.

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2$$

- To satisfy the derivative condition, we differentiate both sides of eqn with respect to Vin, which results in the following equation:

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = k_n \cdot (V_{in} - V_{T0})$$

Since the derivative of the output voltage with respect to the input voltage is equal to (-1) at *VIL,* we can substitute *dV0ut / dVin* = - 1

$$-\frac{1}{R_L}\cdot(-1)=k_n\cdot\left(V_{IL}-V_{T0}\right)$$

for V_{IL}, we obtain

$$V_{IL}=V_{T0}+\frac{1}{k_n R_L} \qquad (2)$$

The value of the output voltage when the input is equal to *VIL* can also be found by substituting (2) into (1), as follows:

$$V_{out}\left(V_{in}=V_{IL}\right) = V_{DD}-\frac{k_n R_L}{2}\cdot\left(V_{T0}+\frac{1}{k_n R_L}-V_{T0}\right)^2$$

$$=V_{DD}-\frac{1}{2k_n R_L}$$

Calculation of V_{IH}

- V_{IH} is the larger of the two voltage points on VTC at which the slope is equal to (-1).
- It can be seen from Fig. that when the input voltage is equal to V_{IH},
- the output voltage V_{out}, is only slightly larger than the output low voltage V_{OL}.
- Hence, $V_{out} < V_{in} - V_{T0}$
- the driver transistor operates in the linear region.
- The KCL equation for the output node is given below.

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot \left[2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - {V_{out}}^2\right]$$

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = \frac{k_n}{2} \cdot \left[2 \cdot (V_{in} - V_{T0}) \cdot \frac{dV_{out}}{dV_{in}} + 2\,V_{out} - 2\,V_{out} \cdot \frac{dV_{out}}{dV_{in}}\right]$$

we can substitute dV_{out}/dV_{in} **= - 1** into (5.25), since the slope of the VTC is equal to (-1) also at Vin = V_{IH}

$$-\frac{1}{R_L}\cdot(-1)=k_n\cdot\left[(V_{IH}-V_{T0})\cdot(-1)+2\,V_{out}\right]$$

6) for V_{IH} yields the following expression.

$$V_{IH}=V_{T0}+2\,V_{out}-\frac{1}{k_n\,R_L}$$

$$\frac{V_{DD}-V_{out}}{R_L}=\frac{k_n}{2}\cdot\left[2\cdot\left(V_{T0}+2\,V_{out}-\frac{1}{k_n\,R_L}-V_{T0}\right)\cdot V_{out}-{V_{out}}^2\right]$$

The positive solution of this second-order equation gives the output voltage V_{out} input is equal to V_{IH}.

$$V_{out}\left(V_{in}=V_{IH}\right)=\sqrt{\frac{2}{3}\cdot\frac{V_{DD}}{k_n\,R_L}}$$

Finally, V_{IH} can be found by $$V_{IH}=V_{T0}+\sqrt{\frac{8}{3}\cdot\frac{V_{DD}}{k_n\,R_L}}-\frac{1}{k_n\,R_L}$$

Summary

Expression of Critical Values for resistive inverter are V_{OH}, V_{OL}, V_{IL}, V_{IH}

$$V_{OH}=V_{DD}$$

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L}\right)^2 - \frac{2 V_{DD}}{k_n R_L}}$$

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}$$

for V_{IL}, we obtain

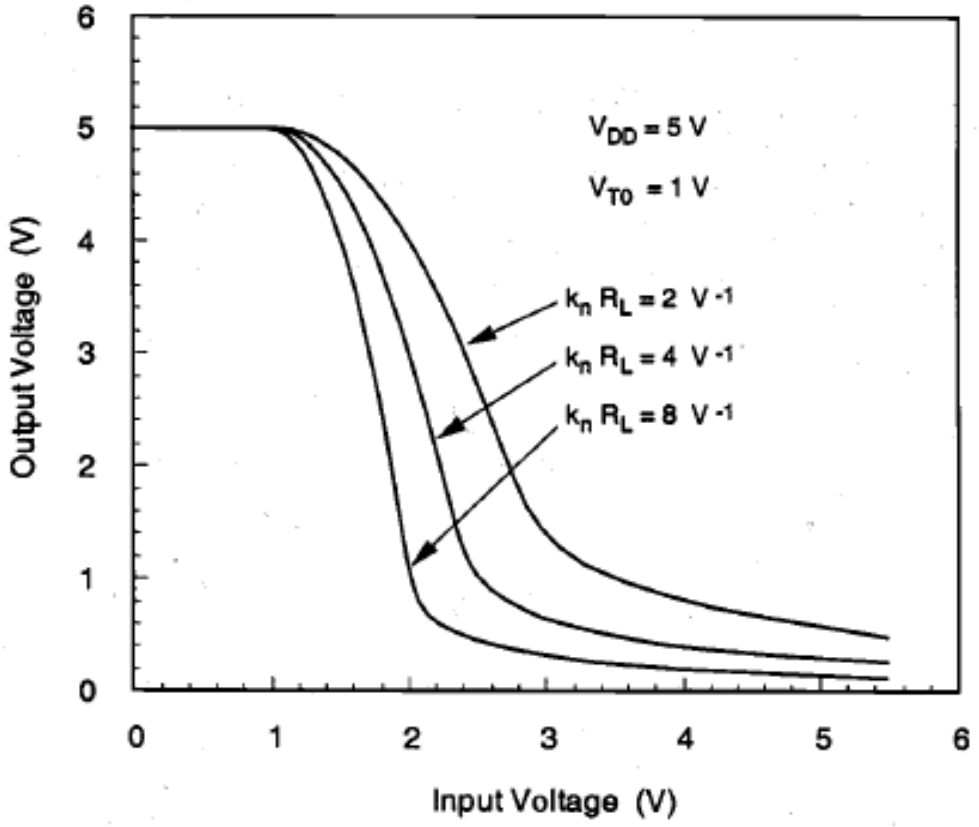
$$V_{IL} = V_{T0} + \frac{1}{k_n R_L}$$

Critical Values for resistive inverter

- The four critical voltage points $V_{OL,}$ $\boldsymbol{V_{OH}}$, V_{IL}, V_{IH} can now be used to determine the noise margins, *NML* and *NMH,* of the resistive-load inverter circuit.
- In addition to these voltage points, which characterize the static input-output behavior, the inverter threshold voltage V_{th} may also be calculated in a straightforward manner.
- Note that the driver transistor operates in saturation mode at this point. Thus, the inverter threshold voltage can be found
- simply by substituting $V_{in} = V_{out} = \boldsymbol{V_{th}}$ into (1), and by solving the resulting quadratic for V_{th}.

Voltage transfer characteristics of the resistive-load inverter, with different (Kn,R_L)

- The output high voltage V_{OH} is determined primarily by the power supply voltage, V_{DD}.
- Among the other three critical voltage points, the adjustment of V_{OL} receives primary attention, while $\boldsymbol{V_{IL}}$ and $\boldsymbol{V_{IH}}$ are usually treated as secondary design variables.
- Figure shows the VTC of a resistive-load inverter for different values of $(kn\ \boldsymbol{R_L})$.
- Note that for larger $\boldsymbol{(kn, R_L)}$ values, the output low voltage V_{OL} becomes smaller
- shape of the VTC approaches that of the ideal inverter, with very large transition slope.



MCQ

Q. For larger values of Kn, VTC of resistive load inverter approaches

a) 0
b) 1
c) Near to ideal value
d) Deviate from ideal value

Power consumption and chip area

- Average DC power consumption of the resistive-load inverter circuit is found by considering two cases, *Vin* = V_{OL} *(low)* and *Vin* = V_{OH} *(high).*
- When the input voltage is equal to $\boldsymbol{V_{OL}}$, the driver transistor is in cut-off. Consequently, there is no steady-state current flow in the circuit *(ID = IR =* 0), and the DC power dissipation is equal to zero.
- When the input voltage is equal to $\boldsymbol{V_{iH}}$ on the other hand, both the driver MOSFET and the load resistor conduct a nonzero current.

Layout of resistive load Inverter

- An alternative approach to save silicon area is to fabricate the load resistor using undoped polysilicon.
- In conventional poly-gate MOS technology, the polysilicon structures forming the gates of transistors and the interconnect lines are heavily doped in order to reduce resistivity.
- Resitive load inverter not a suitable candidate for most digital VLSI system applications, primarily because of the large area occupied by the load resistor.

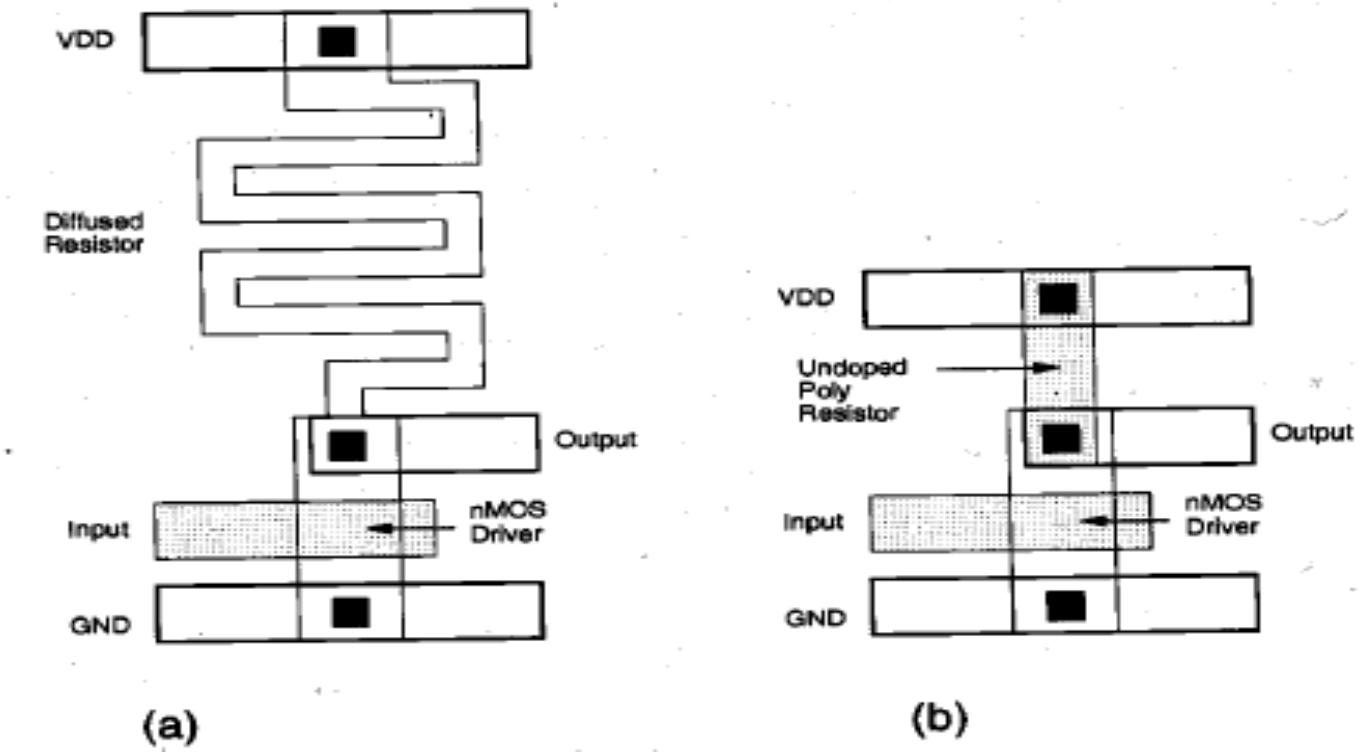


Fig. Sample layout of resistive-load inverter circuits with (a) diffused resistor and (b) undoped polysilicon resistor.

Problem

Q.1 Consider a resistive-load inverter circuit with *VDD*= 5 V, kn '= 20 μA/V^2, $\mathbf{V_{T0}}$**=** 0.8 V, R_L = 200 kW, and *W/L*= 2. Calculate the critical voltages *(V_{OL},V_{OH} V_{IL}, V_{IH})* on the VTC and find the noise margins of the circuit.

Solution: When the input voltage is low, i.e., when the driver nMOS transistor is cut-off, the output high voltage can be found as MOS Inverters:

$VOH = VDD$

- Resistive-load inverter example, the transconductance of the driver transistor is $k = kn'(W/L) = 40\ \mu A/V^2$ and, hence, $(knR_L) = 8\ V^{-1}$.
- The output low voltage *VOL* is calculated by using

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L}\right)^2 - \frac{2V_{DD}}{k_n R_L}}$$

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3}\cdot\frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}$$

The critical voltage V_{IL}

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L}$$

Answers

$V_{OH} = V_{DD} = 5$ V

V_{OL}==0. 147 V

V_{IL}=0.925 V

V_{IH}=1.97V

$$NM_L = V_{IL} - V_{OL} = 0.93 - 0.15 = 0.78 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 5.0 - 1.97 = 3.03 \text{ V}$$

For better noise immunity, the noise margin for "low" signals should be at least about 25% of the power supply voltage V_{DD},

Inverters with n-Type MOSFET Load

- The main advantage of using a MOSFET as the load device is that the silicon area occupied by the transistor is usually smaller than that occupied by a comparable resistive load.
- Inverter circuits with active loads can be designed to have better overall performance compared to that of passive-load inverters.
- Active load nMOS inverter can be implemented in two ways:

- *Enhancement-Load nMOS Inverter*
- *Depletion-Load nMOS Inverter*

Enhancement-Load nMOS Inverter

- Fig. suffer from relatively high stand-by (DC) power dissipation; hence, enhancement-load nMOS inverters are not used in any large-scale digital applications.
- Fig. (a) requires a single voltage supply and a relatively simple fabrication process, yet the V_{OH} level is limited to V_{DD} -V_{Tload}'
- The load device of the inverter circuit shown in Fig. (b), on the other hand, is always biased in the linear region.
- Thus, the $\boldsymbol{V_{OH}}$ level is equal to V_{DD}, resulting in higher noise margins compared to saturated enhancement-load inverter.

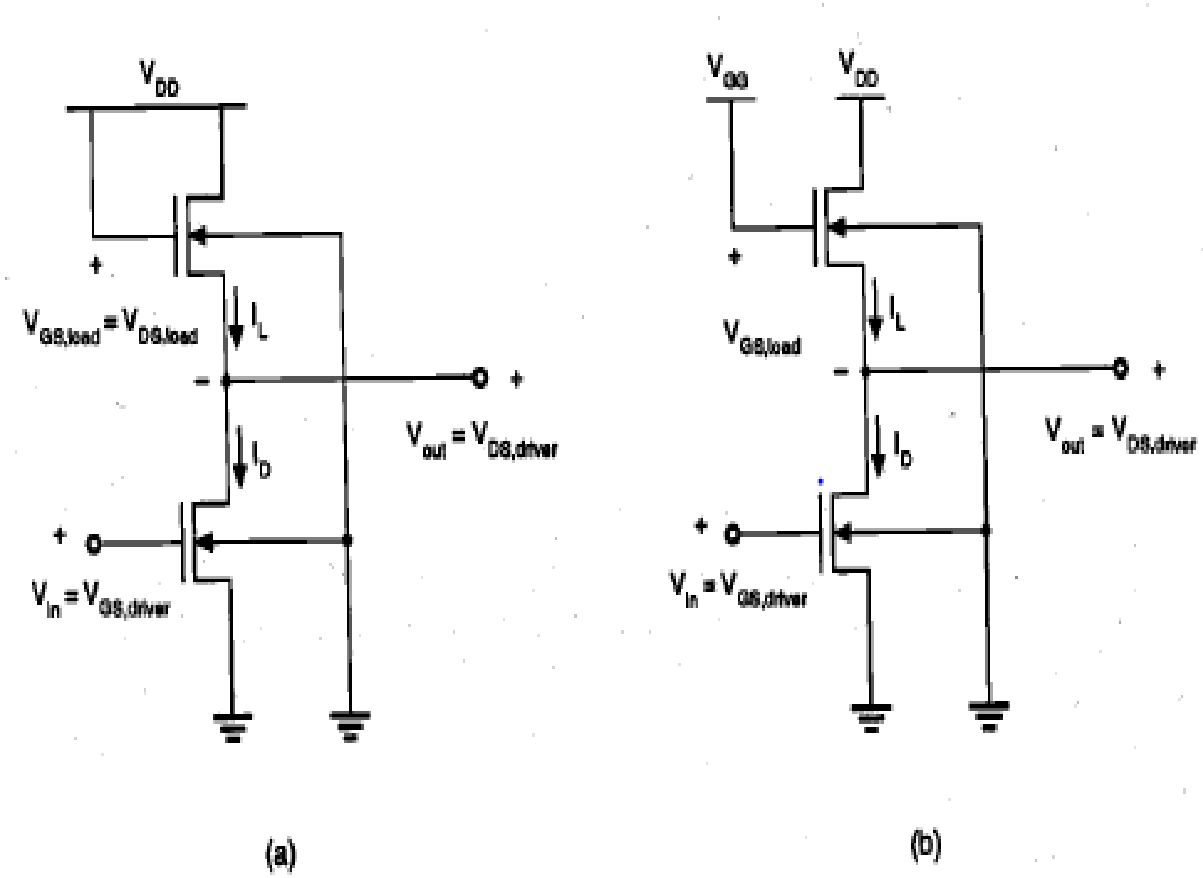
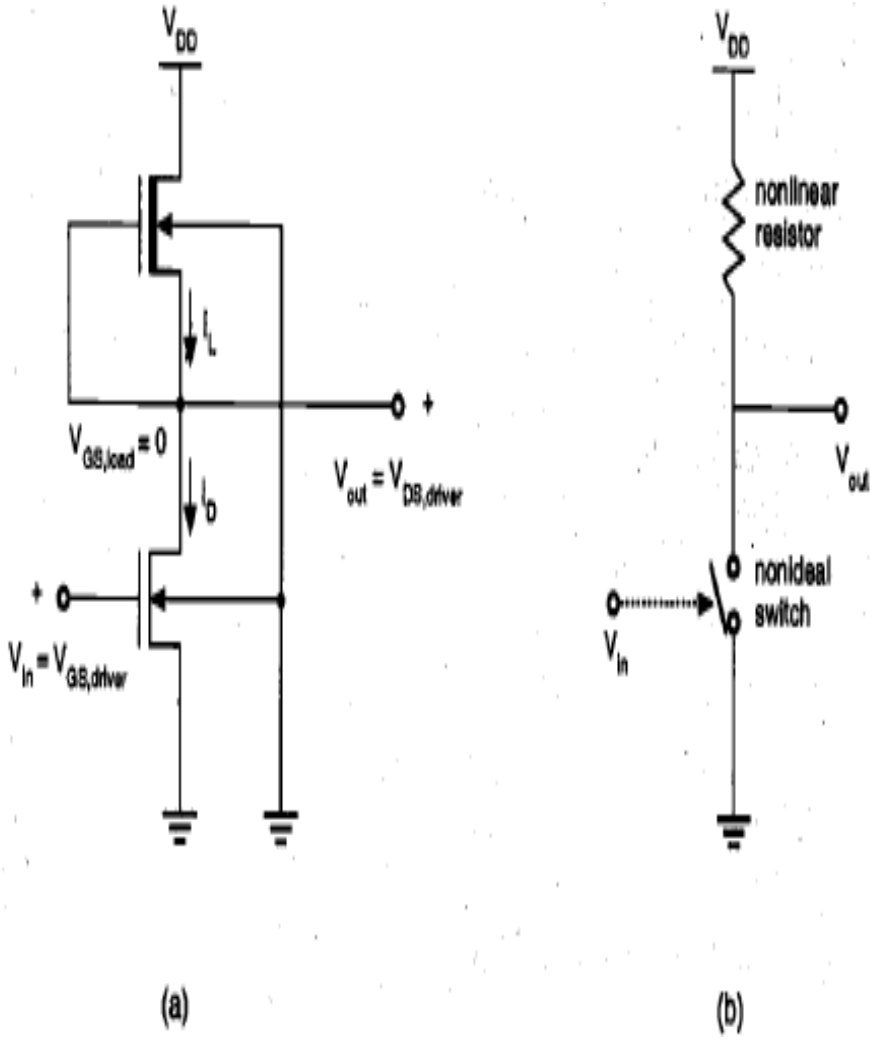


Fig. (a) Inverter circuit with saturated enhancement-type nMOS load. (b) Inverter with linear enhancement-type load.

Inverter circuit with depletion-type nMOS load

- The circuit diagram of the depletion-load inverter circuit is shown in Fig.(a), and a simplified view of the circuit consisting of a nonlinear load resistor and a nonideal switch (driver) in shown in Fig.(b).
- The driver device is an enhancement-type nMOS transistor, with $\boldsymbol{V_{T\,driver}} > 0$, whereas the load is a depletion-type nMOS transistor, with $V_{T0\,load} < 0$.
- The current-voltage equations to be used for the depletion-type load transistor are identical to those of the enhancement-type device, with the exception of the negative threshold voltage.
- The gate and the source nodes of the load transistor are connected, hence, $\boldsymbol{V_{GSload}} = 0$ always.
- Since the threshold voltage of the depletion type load is negative, the condition $\boldsymbol{V_{GSload}} > V_{T\,load}$ *is* satisfied
- Consequently, the load device is subject to the substrate-bias effect, so that its threshold voltage is a function of its source-to-substrate voltage, $V_{SBload} = V_{out}$.



Active NMOS load Inverter

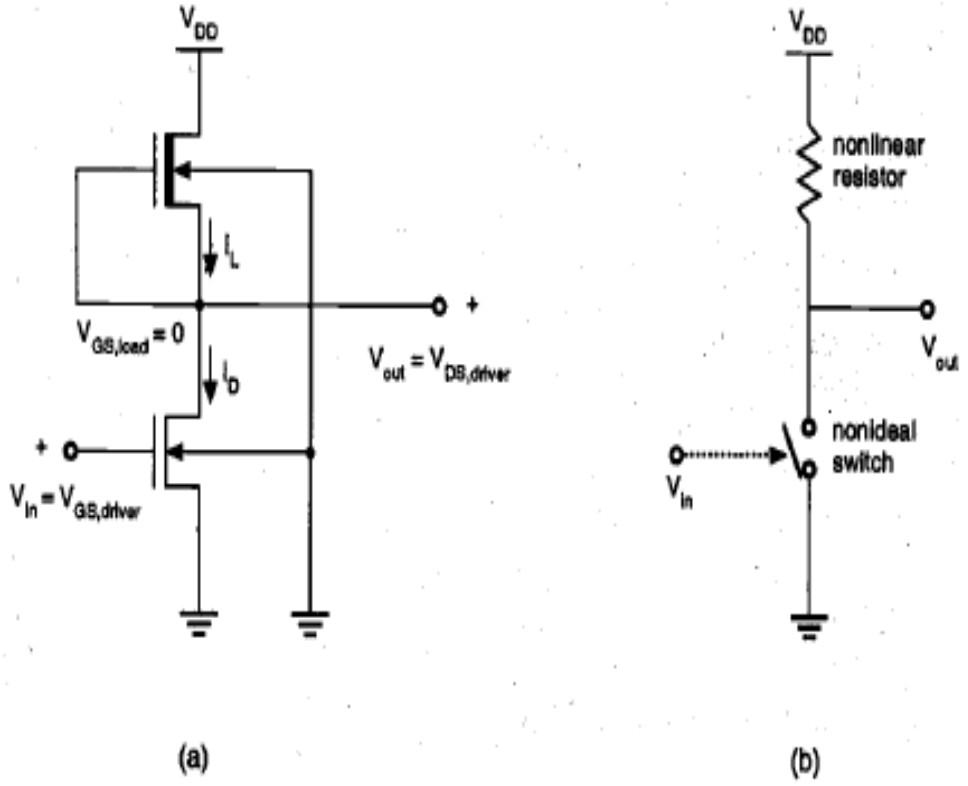
- **Depletion-type nMOS** load is slightly more complicated and requires additional processing steps, especially for the channel implant to adjust the threshold voltage of the load device.
- The immediate advantages of implementing this circuit configuration are:

(i) sharp VTC transition and better noise margins,

(ii) single power supply,

(iii) smaller overall layout area.

- The driver device is an enhancement-type nMOS transistor, with $V_{T\,driver} > 0$, whereas the load is a depletion-type nMOS transistor, with $V_{Tload} < 0$.



(a) Inverter circuit with depletion-type nMOS load. (b) Simplified equivalent circuit consisting of a nonlinear load resistor and a nonideal switch controlled by the input.

- the load device is subject to the substrate-bias effect, so that its threshold voltage is a function of its source-to substrate voltage, $V_{SB\ load} = V_{T0}$.

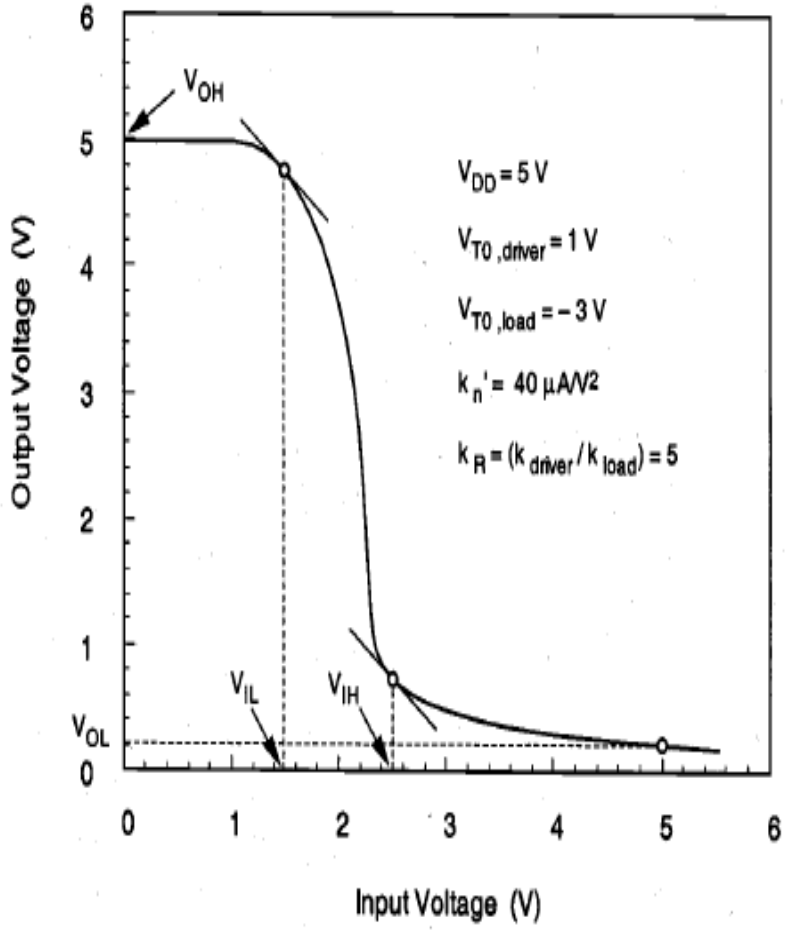
$$V_{T,load} = V_{T0,load} + \gamma\left(\sqrt{|2\phi_F| + V_{out}} - \sqrt{|2\phi_F|}\right)$$

when Vout < $V_{DD} + V_{Tload}$, the load transistor is in saturation. Note that this condition corresponds to $V_{DS\ load} > {}_{VGS\ load} - V_{Tload}$. Then, the load current is given by the following equation.

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot \left[-V_{T,load}(V_{out})\right]^2 = \frac{k_{n,load}}{2} \cdot \left|V_{T,load}(V_{out})\right|^2$$

The voltage transfer characteristic (VTC) of this inverter can be constructed by setting $V_{D,driver} = I_{Dload}$' $V_{GSdriver} = V_{in}$, *and* $V_{DS\ driver} = V_D$, and by solving the corresponding current equations for $\boldsymbol{V_0 = f(Vin)}$.

Fig. shows the VTC of a typical depletion-load inverter, with *kdriver' = knload '*



Depletion load inverter: Region of Operation

- we will consider the critical voltage points V_{OH}, V_{OL}, V_{IL} and V_{IH} for this inverter 163 circuit. The operating regions and the voltage levels of the driver and the load transistors at these critical points are listed below.

V_{in}	V_{out}	Driver operating region	Load operating region
V_{OL}	V_{OH}	cut-off	linear
V_{IL}	$\approx V_{OH}$	saturation	linear
V_{IH}	small	linear	*saturation*
V_{OH}	V_{OL}	linear	saturation

Calculation of V_{OH}

- When the input voltage Vin is smaller than the driver threshold voltage V_T, the driver transistor is turned off and does not conduct any drain current. Consequently, the load device, which operates in the linear region, also has zero drain current. Substituting V_{OH} for V_{out} in fig. and letting the load current $I_{d,load} = 0$,

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot \left[2\left|V_{T,load}\left(V_{OH}\right)\right| \cdot \left(V_{DD} - V_{OH}\right) - \left(V_{DD} - V_{OH}\right)^2 \right] = 0$$

The only valid solution in the linear region is $V_{OH} = V_{DD}$.

Calculation of V_{OL}

- To calculate the output low voltage V_{OL}' we assume that the input voltage V of the inverter is equal to $V_{OH} = V_{DD}$. Note that in this case, the driver transistor operates in the linear region while the depletion-type load is in saturation.
- V_{gs}load=0 (depletion load)

$$\frac{k_{driver}}{2}\cdot\left[2\cdot\left(V_{OH}-V_{T0}\right)\cdot V_{OL}-V_{OL}^2\right]=\frac{k_{load}}{2}\cdot\left[-V_{T,load}\left(V_{OL}\right)\right]^2$$

This second-order equation in V_{OL} can be solved by temporarily neglecting the dependence of $V_{T\,load}$ on V_{OL}, as follows.

$$V_{OL}=V_{OH}-V_{T0}-\sqrt{\left(V_{OH}-V_{T0}\right)^2-\left(\frac{k_{load}}{k_{driver}}\right)\cdot\left|V_{T,load}\left(V_{OL}\right)\right|^2}$$

Calculation of V_{IL}

- By definition, the slope of the VTC is equal to (-1), i.e., $dV_{out}/dV_{in} = -1$ when the input voltage is *Vin = VIL.* Note that in this case, the driver transistor operates in saturation while the load transistor operates in the linear region. Applying KCL for the output node, we obtain the following current equation:

$$\frac{k_{driver}}{2}\cdot\left(V_{in}-V_{T0}\right)^2=\frac{k_{load}}{2}\cdot\left[2\left|V_{T,load}\left(V_{out}\right)\right|\cdot\left(V_{DD}-V_{out}\right)-\left(V_{DD}-V_{out}\right)^2\right]$$

To satisfy the derivative condition at *VIL* we differentiate both sides of (5 .39) with respect to *Vi'.*

$$k_{driver}\cdot\left(V_{in}-V_{T0}\right)=\frac{k_{load}}{2}\cdot\left[2\left|V_{T,load}\left(V_{out}\right)\right|\left(-\frac{dV_{out}}{dV_{in}}\right)+2\left(V_{DD}-V_{out}\right)\left(-\frac{dV_{T,load}}{dV_{in}}\right)-2\left(V_{DD}-V_{out}\right)\left(-\frac{dV_{out}}{dV_{in}}\right)\right]$$

$$V_{IL}=V_{T0}+\left(\frac{k_{load}}{k_{driver}}\right)\cdot\left[V_{out}-V_{DD}+\left|V_{T,load}\left(V_{out}\right)\right|\right]$$

Calculation of V_{IH}

V_{IH} is the larger of the two voltage points on the VTC at which the slope is equal to (-1). Since the output voltage corresponding to this operating point is relatively small, the driver transistor is in the linear region and the load transistor is in saturation.

$$\frac{k_{driver}}{2}\cdot\left[2\cdot\left(V_{in}-V_{TO}\right)\cdot V_{out}-V_{out}^2\right]=\frac{k_{load}}{2}\cdot\left[-V_{T,load}\left(V_{out}\right)\right]^2$$

Differentiating both sides of *(5.42)* with respect to *Vin,* we obtain:

$$k_{driver}\cdot\left[V_{out}+\left(V_{in}-V_{TO}\right)\left(\frac{dV_{out}}{dV_{in}}\right)-V_{out}\left(\frac{dV_{out}}{dV_{in}}\right)\right]$$
$$=k_{load}\cdot\left[-V_{T,load}\left(V_{out}\right)\right]\cdot\left(\frac{dV_{T,load}}{dV_{out}}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)$$

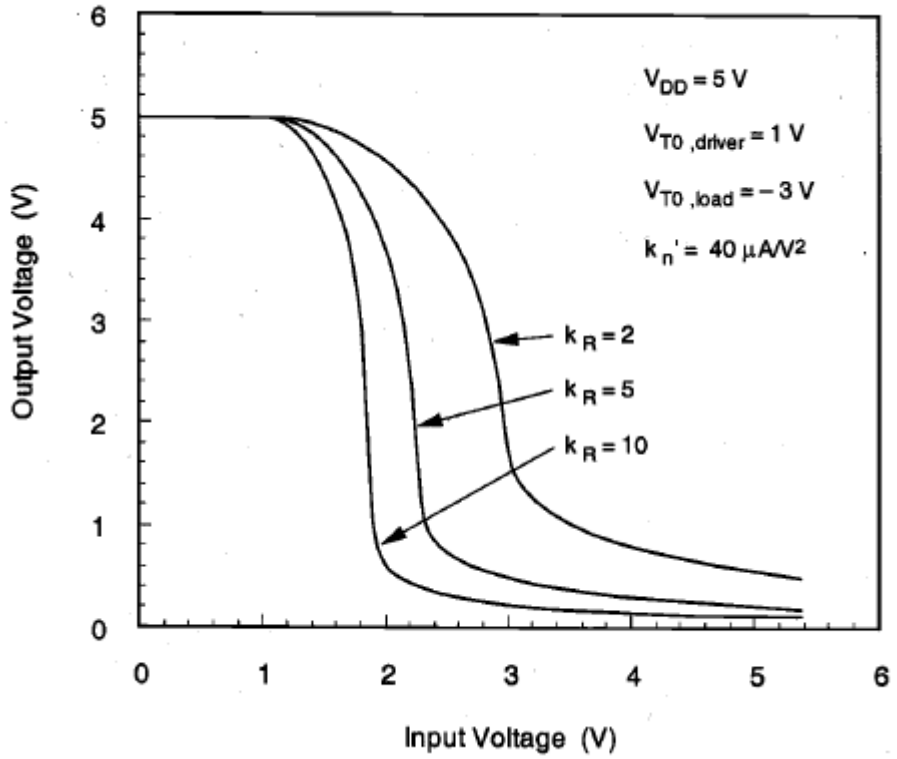
The derivative of the load threshold voltage with respect to the output voltage cannot be neglected in this case.

$$V_{IH}=V_{TO}+2V_{out}+\left(\frac{k_{load}}{k_{driver}}\right)\cdot\left[-V_{T,load}\left(V_{out}\right)\right]\cdot\left(\frac{dV_{T,load}}{dV_{out}}\right)$$

$$\frac{dV_{T,load}}{dV_{out}}=\frac{\gamma}{2\sqrt{\left|2\phi_F\right|+V_{out}}}$$

Design of Depletion-Load Inverters

- Based on the VTC analysis given in the previous section, we can now consider the ***design*** of depletion-load inverters to satisfy certain DC performance criteria.
- Fig. Voltage transfer characteristics of depletion-load inverters, with different driver to-load ratios.



Design Parameters

- The designable parameters in an inverter circuit are: (i) the power supply voltage V_{DD}, (ii) the threshold voltages of the driver and the load transistors, and (iii) the *(WIL)* ratios of the driver and the load transistors.
- In most practical cases, power supply voltage and the device threshold voltages(V_{th}) are dictated by other external constraints and by the fabrication process; thus, they cannot be adjusted for every individual inverter circuit to satisfy performance requirements.
- *(WIL)* ratio of the transistors and more specifically, the driver-to-load ratio k_R, as the primary design parameter.
- power supply voltage V_{DD} of the inverter circuit also determines the level of the output high voltage V_{OH}, since $V_{OH} = V_{DD}$. Of the remaining three critical voltages on the VTC, the output low voltage V_{OL} is usually the most significant design constraint.
- Designing the inverter to achieve a certain V_{OL} value will automatically set the other two critical voltages, V_{IL} and V_{IH}, as well.

Design Parameters (Contd.)

- Calculate the driver-to-load ratio that achieves a target *VOL*

$$k_R = \frac{k_{driver}}{k_{load}} = \frac{\left|V_{T,load}(V_{OL})\right|^2}{2(V_{OH} - V_{T0})V_{OL} - V_{OL}^2}$$

the driver-to-load ratio is given by

$$k_R = \frac{k'_{n,driver} \cdot \left(\frac{W}{L}\right)_{driver}}{k'_{n,load} \cdot \left(\frac{W}{L}\right)_{load}} \qquad k_R = \frac{\left(\frac{W}{L}\right)_{driver}}{\left(\frac{W}{L}\right)_{load}}$$

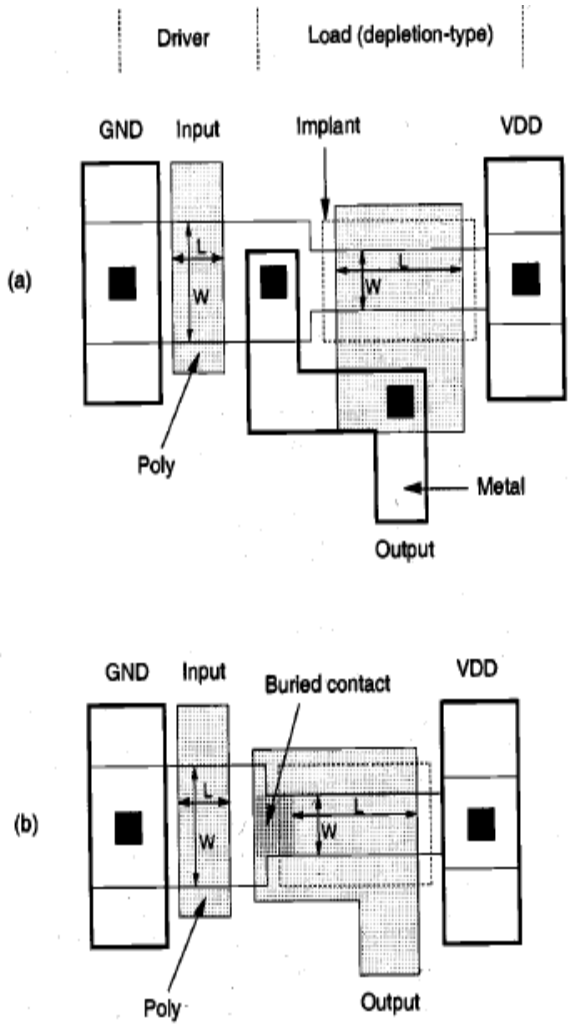
Power Area Consideration

$$I_{DC}(V_{in}=V_{DD}) = \frac{k_{load}}{2}\cdot\left[-V_{T,load}(V_{OL})\right]^2$$

$$= \frac{k_{driver}}{2}\cdot\left[2\cdot(V_{OH}-V_{T0})\cdot V_{OL}-V_{OL}^2\right]$$

- Assuming that the input voltage level is low during 50% of the operation time and high during the other 50%, the overall average DC power consumption of this circuit can be estimated as follows

$$P_{DC} = \frac{V_{DD}}{2}\cdot\frac{k_{load}}{2}\cdot\left[-V_{T,load}(V_{OL})\right]^2$$



Example

Q. Calculate the critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) and find the noise margins of the following depletion-load inverter circuit:

$$V_{OL} = V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{T0})^2 - \left(\frac{k_{load}}{k_{driver}}\right) \cdot \left|V_{T,load}(V_{OL})\right|^2}$$

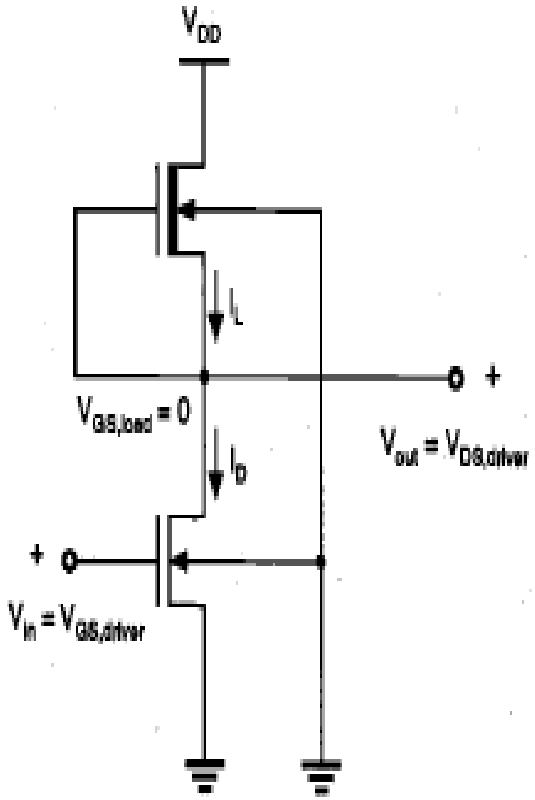
$$V_{T,load} = V_{T0,load} + \gamma\left(\sqrt{|2\phi_F| + V_{OL}} - \sqrt{|2\phi_F|}\right)$$

$$V_{IL}(V_{out}) = V_{T0} + \frac{k_{load}}{k_{driver}} \cdot \left[V_{out} - V_{DD} + \left|V_{T,load}(V_{out})\right|\right]$$

$$V_{IL}(V_{out}) = V_{T0} + \frac{k_{load}}{k_{driver}} \cdot \left[V_{out} - V_{DD} + \left|V_{T,load}(V_{out})\right|\right]$$

$$= 1 + \left(\frac{1}{6}\right)(V_{out} - 5 + 2.36) = 0.167\,V_{out} + 0.56$$

$$V_{out} = 6\,V_{IL} - 3.35$$



$V_{DD} = 5$ V

$V_{T0,driver} = 1.0$ V

$V_{T0,load} = -3.0$ V

$(W/L)_{driver} = 2$, $(W/L)_{load} = 1/3$

$k_{n,driver}' = k_{n,load}' = 25\ \mu A/V^2$

$\gamma = 0.4\ V^{1/2}$

$\phi_F = -0.3$ V

$$\frac{k_{driver}}{2} \cdot (V_{IL} - V_{T0})^2 = \frac{k_{load}}{2} \cdot \left[2\left|V_{T,load}(V_{out})\right| \cdot (V_{DD} - 6\,V_{IL} + 3.35) - (V_{DD} - 6\,V_{IL} + 3.35)^2\right]$$

$$V_{IL} = \begin{cases} 0.98\ \text{V} \\ \underline{\underline{1.36\ \text{V}}} \end{cases}$$

$$V_{out} = 6 \cdot 1.36 - 3.35 = 4.81\ \text{V}$$

$$\frac{dV_{T,load}}{dV_{out}} = \frac{\gamma}{2\sqrt{|2\phi_F| + V_{out}}} = \frac{0.4}{2\sqrt{0.6+0.2}} = 0.22$$

$$V_{IH}(V_{out}) = V_{T0} + 2V_{out} + \frac{k_{load}}{k_{driver}} \cdot \left[-V_{T,load}(V_{out})\right] \cdot \left(\frac{dV_{T,load}}{dV_{out}}\right)$$

$$= 1 + 2V_{out} + \left(\frac{1}{6}\right) \cdot 2.95 \cdot 0.22 = 2V_{out} + 1.1$$

$$V_{out} = 0.5V_{IH} - 0.55$$

$$2 \cdot \left[2 \cdot (V_{IH} - 1) \cdot (0.5V_{IH} - 0.55) - (0.5V_{IH} - 0.55)^2\right] = \frac{1}{3} \cdot (2.95)^2$$

The solution of this simple quadratic equation yields two values for V_{IH}.

$$V_{IH} = \begin{cases} -0.35\ \text{V} \\ \underline{2.43\ \text{V}} \end{cases}$$

$$V_{out} = 0.5 \cdot 2.43 - 0.55 = 0.67\ \text{V}$$

$$\frac{dV_{T,load}}{dV_{out}} = 0.18$$

$$NM_H = V_{OH} - V_{IH} = 2.57\ \text{V}$$

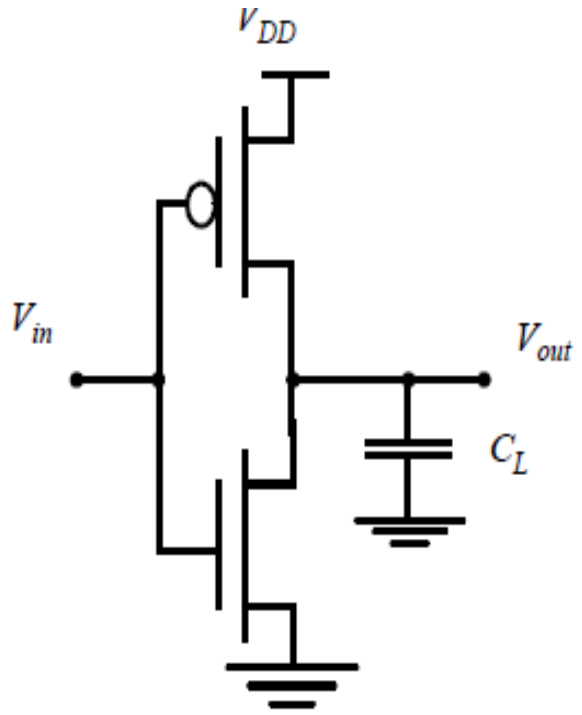
$$NM_L = V_{IL} - V_{OL} = 1.17\ \text{V}$$

CMOS Inverter

Static CMOS inverter. V_{DD} stands for the supply voltage.

Design metrics:

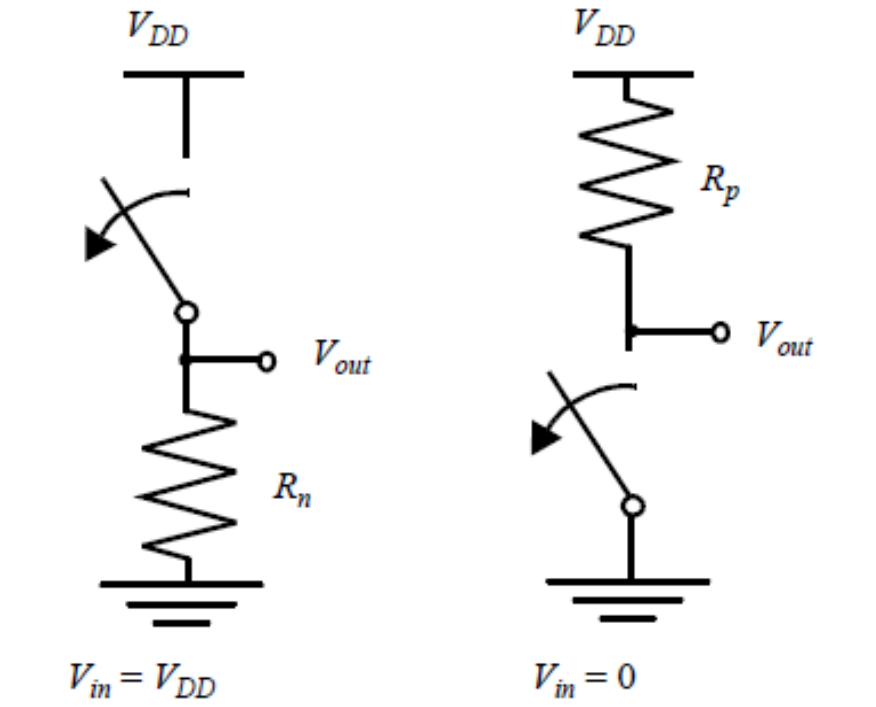
- *cost,* expressed by the complexity and area
- *integrity and robustness*, expressed by the static (or steady-state) behavior
- *performance*, determined by the dynamic (or transient) response
- *energy efficiency,* set by the energy and power consumption



CMOS as switch

A number of other important properties of static CMOS can be derived from this switchlevel
view:

- The high and low output levels equal *VDD* and *GND*, respectively; in other words, the voltage swing is equal to the supply voltage. This results in high noise margins.
- The logic levels are not dependent upon the relative device sizes, so that the transistors can be minimum size.
- In steady state, there always exists a path with finite resistance between the output and either *VDD* or *GND*.
- A well-designed CMOS inverter, therefore, has a *low output impedance*, which makes it less sensitive to noise and disturbances. Typical values of the output resistance are in kΩ range.
- The *input resistance* of the CMOS inverter is extremely high, as the gate of an MOS transistor is a virtually perfect insulator and draws no dc input current

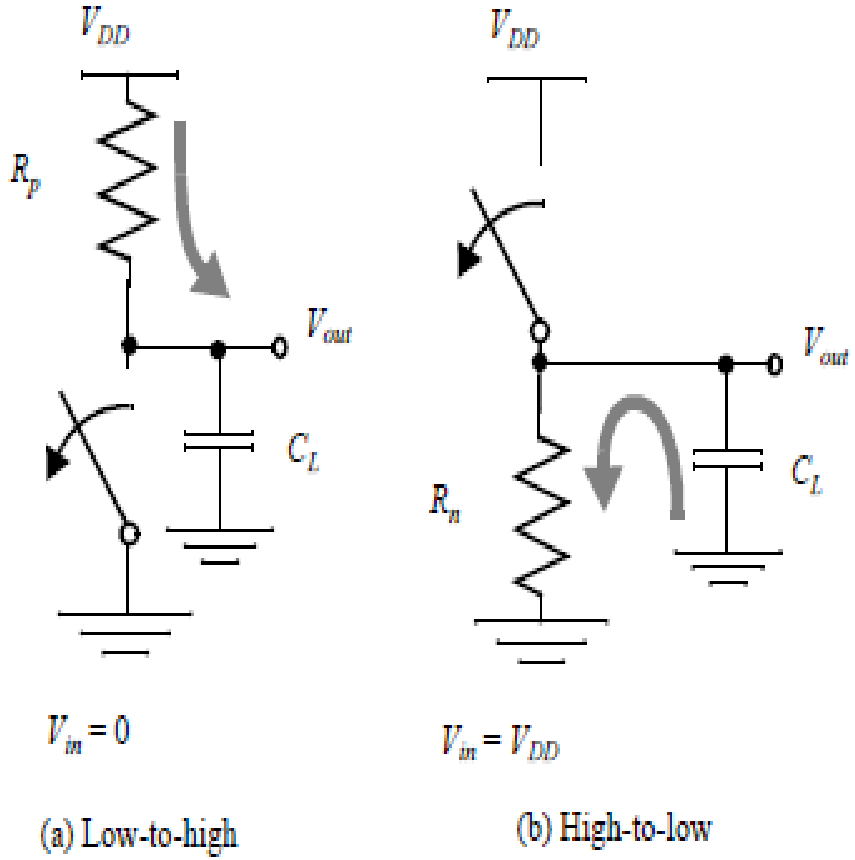


(a) Model for high input (b) Model for low input

- Switch models of CMOS inverter.

Switch model of dynamic behavior of static CMOS Inverter.

- High gain during the switching transient, when both NMOS and PMOS are simultaneously on, and in saturation.
- The gate response time is simply determined by the time it takes to charge the capacitor *CL* through the resistor R_p.
- Propagation delay of such a network is proportional to the its time constant R_pC_L.
- **Hence, a fast gate is built either by keeping the output capacitance small or by decreasing the on-resistance of the transistor.**
- The latter is achieved by increasing the *W*/*L* ratio of the device.



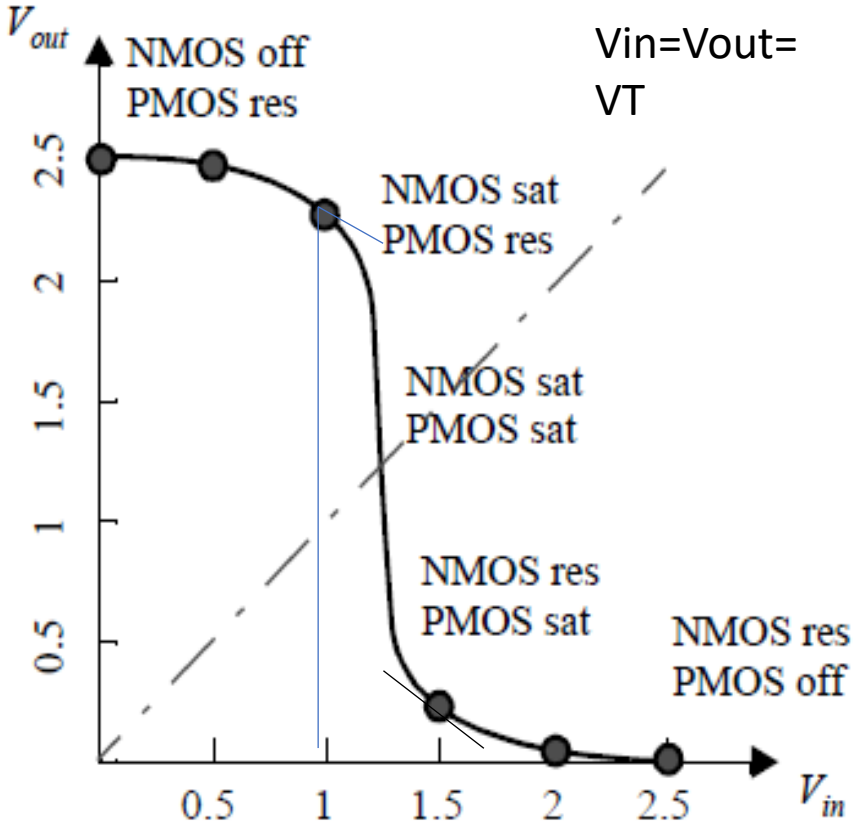
VTC of CMOS Inverter

- VTC of static CMOS inverter
- From voltage-transfer characteristic of the static CMOS inverter, the values of *VOH* and *VOL* are *VDD* and *GND*, respectively.
- Aim is to determine the precise values of switching threshold *VM, VIH,* and *VIL* as well as the noise margins.

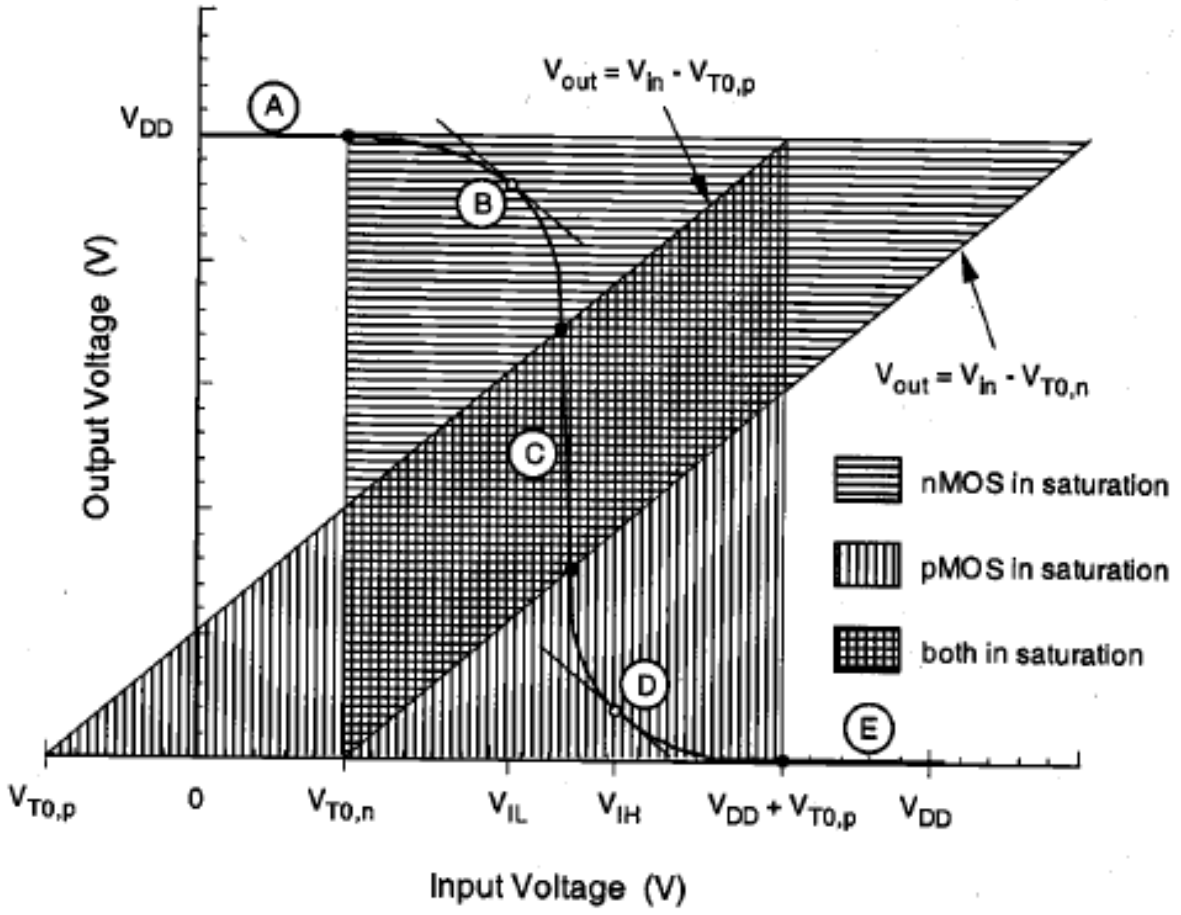
$$i_d=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{gs}-V_T)V_{ds}-V_{ds}^{\ 2}]$$

$$i_d=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}[V_{gs}-V_T]^2$$

Vds=Vgs-VT



Region of operation: VTC



Region	V_{in}	V_{out}	nMOS	pMOS
A	$< V_{T0,n}$	V_{OH}	cut-off	linear
B	V_{IL}	high $\approx V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$>\left(V_{DD} + V_{T0,p}\right)$	V_{OL}	linear	cut-off

Q. In CMOS inverter, what are the region of operation for PMOS and NMOS when Vout=Vin

a) Lin, Sat
b) Lin, Lin
c) Sat, Lin
d) Sat, Sat

Evaluating the Robustness of the CMOS Inverter: The Static Behavior

Switching Threshold

- Switching threshold, V_T, is defined as the point where $V_{in} = V_{out}$. Its value can be obtained graphically from the intersection of the VTC with the line given by $V_{in} = V_{out}$
- *VOH=VDD since IDn=IDp=0*

Here:

$$V_{GS,n} = V_{in}$$
$$V_{DS,n} = V_{out}$$

$$V_{GS,p} = -(V_{DD} - V_{in})$$
$$V_{DS,p} = -(V_{DD} - V_{out})$$

The pMOS transistor operates in *saturation* if $V_{in} < (V_{DD} + V_{T0,p})$, *and* if :

$$V_{DS,p} \leq V_{GS,p} - V_{T0,p} \quad \Leftrightarrow \quad V_{out} \geq V_{in} - V_{T0,p}$$

Inverter Delays

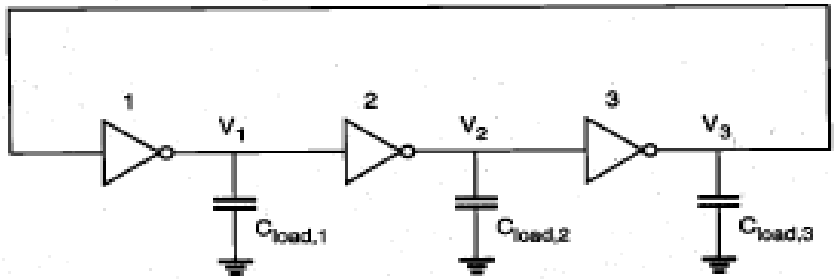
- Cascade connected inverters
- *T = TPHLI + TPLHI + TPHL2 + TPLH2 + TPHL3 +TPLH3*

=2τp +2 τ p +2 τ p

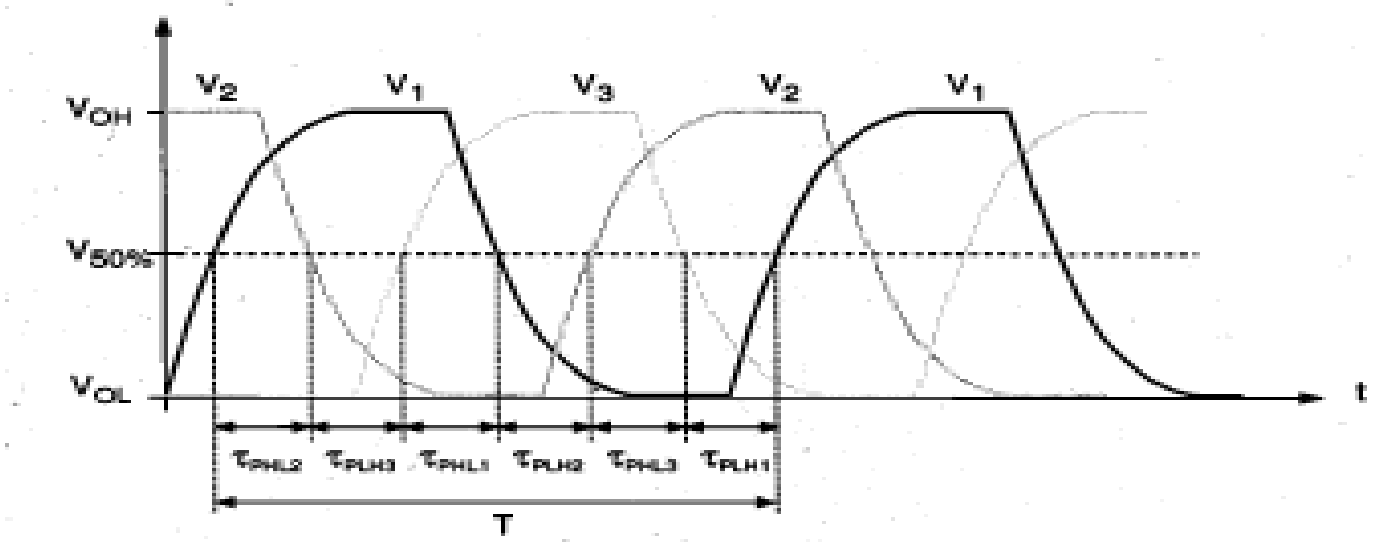
=6 τp

$$f = \frac{1}{2n\tau_p}$$

$$\tau_p = \frac{1}{2nf}$$



CMOS Ring Oscillator Circuit



Typical voltage waveforms of the three inverter

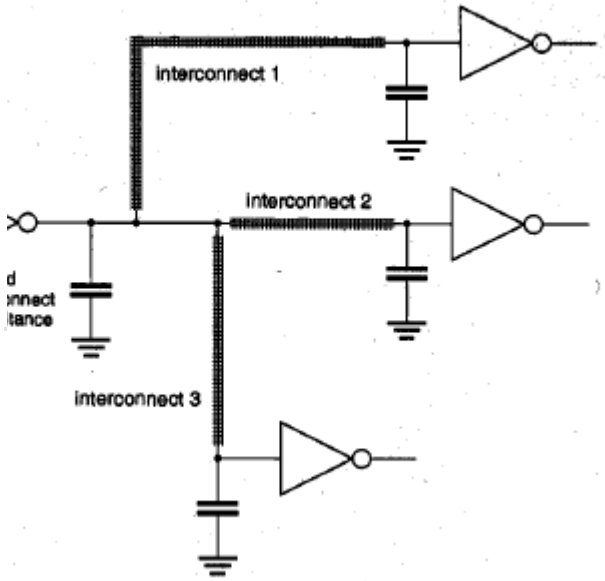
Estimation of Interconnect Parasitic

Interconnects

$$\tau_{rise}\left(\tau_{fall}\right) < 2.5 \times \left(\frac{l}{v}\right) \Rightarrow \{\text{transmission} - \text{line modeling}\}$$

$$2.5 \times \left(\frac{l}{v}\right) < \tau_{rise}\left(\tau_{fall}\right) < 5 \times \left(\frac{l}{v}\right) \Rightarrow \begin{Bmatrix}\text{either transmission} - \text{line} \\ \text{or lumped modeling}\end{Bmatrix}$$

$$\tau_{rise}\left(\tau_{fall}\right) > 5 \times \left(\frac{l}{v}\right) \Rightarrow \{\text{lumped modeling}\}$$



Here, *l* is the interconnect line length, and *v* is the propagation speed. Note that transmission line analysis always gives the correct result irrespective of the rise/fall time and the interconnect length;

Fig: An inverter driving three other inverters over interconnection lines.

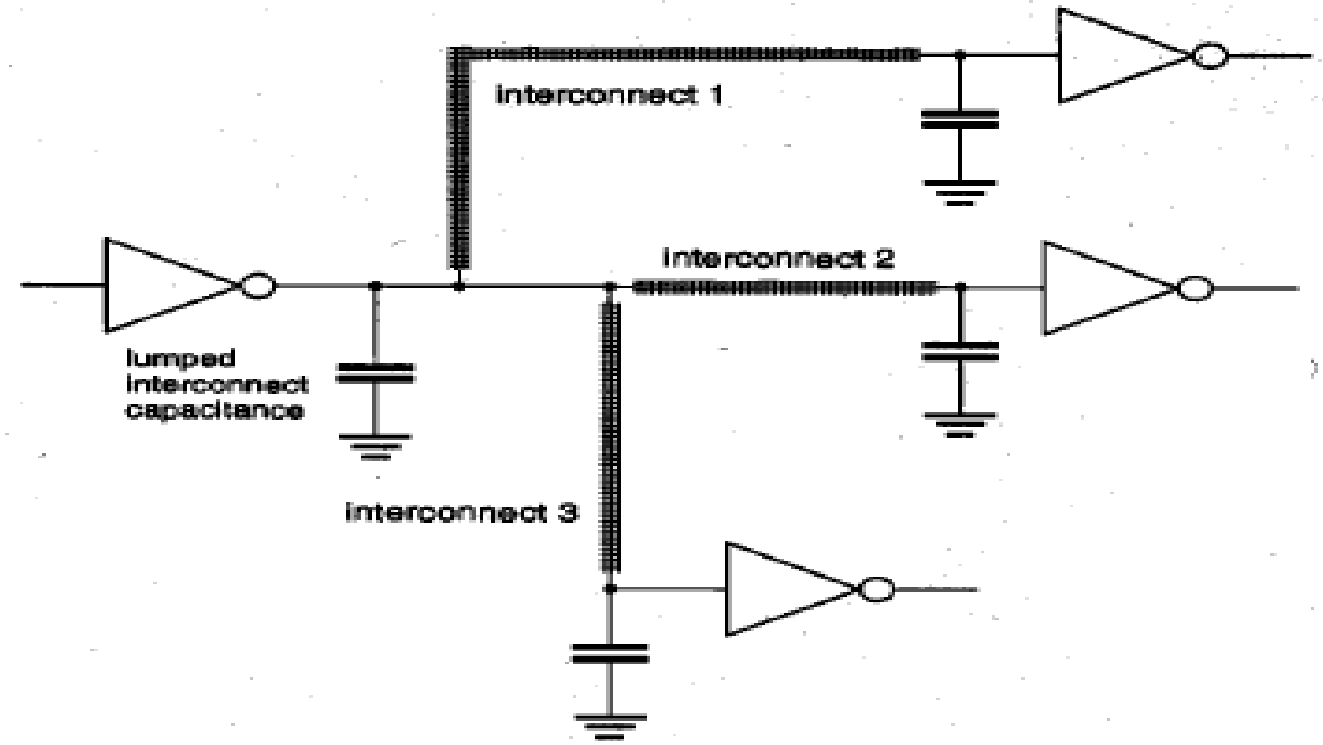
Estimation of Interconnect Parasitic

The conventional delay estimation approaches seek to classify three main components of the output load, all of which are assumed to be purely capacitive, as:

(i) internal parasitic capacitances of the transistors,

(ii) interconnect (line) capacitances, and

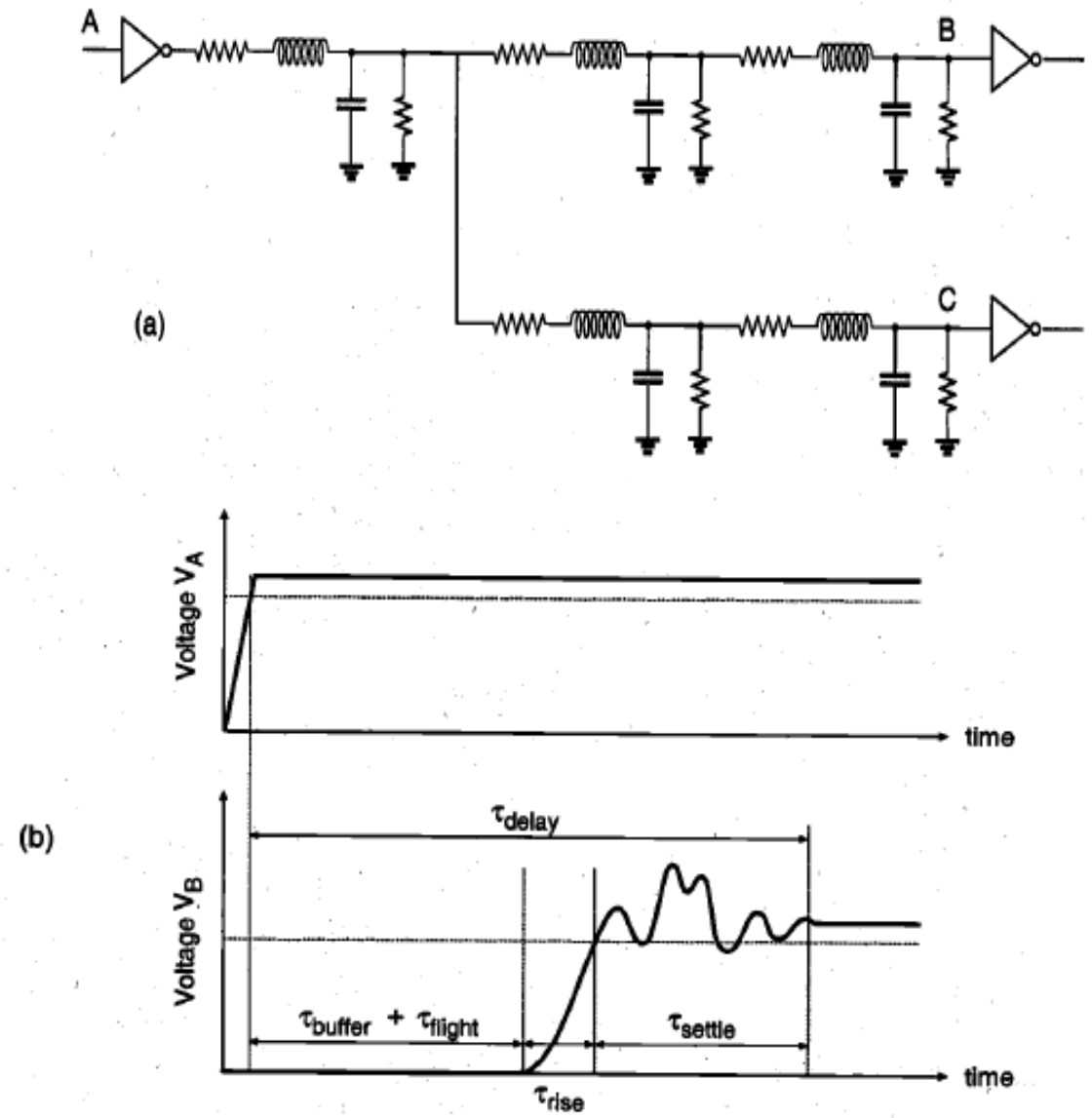
(iii) input capacitances of the fan-out gates.



Calculation of Interconnect Delay

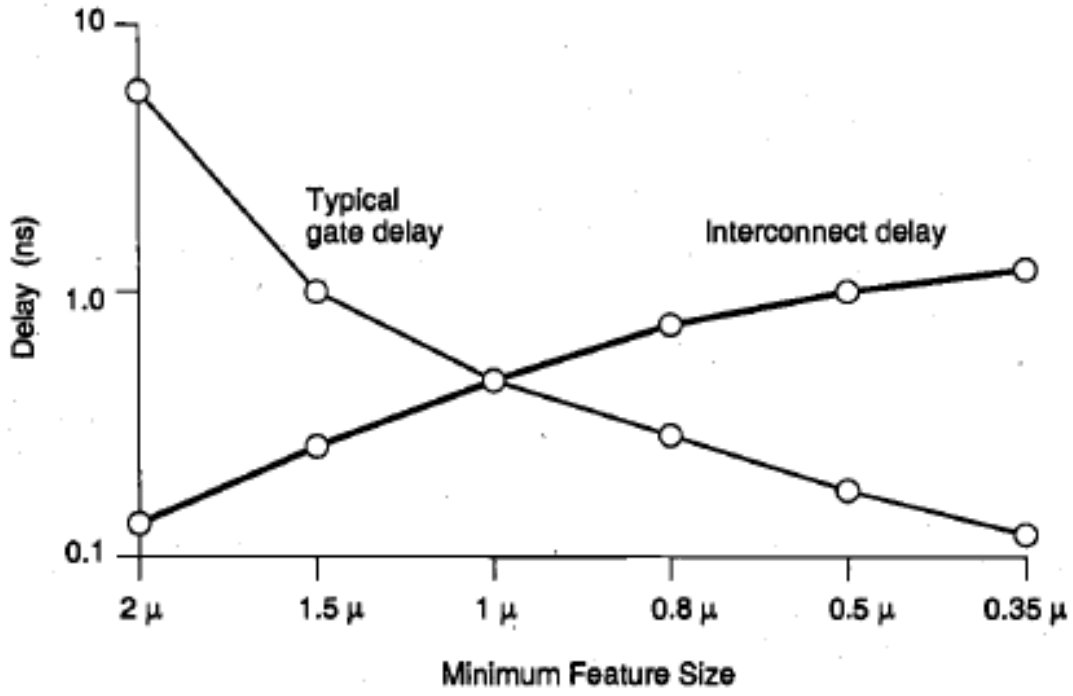
RC Delay Models

- Fig: (a) An RLCG interconnection tree. (b) Typical signal waveforms at the nodes and B, showing the signal delay and the various delay components.
- Signal integrity can be significantly degraded especially when the output impedance of the driver is significantly lower than the characteristic impedance of the transmission line.



Interconnect Delay

- Interconnect delay dominates gate delay ir submicron CMOS technologies.



Interconnect Capacitance Estimation

- In a large-scale integrated circuit, the parasitic interconnect capacitances are among the most difficult parameters to estimate accurately.
- Each interconnection line (wire) is a three-dimensional structure in metal and/or polysilicon with significant variations of shape, thickness, and vertical distance from the ground plane (substrate).
- Also, each interconnect line is typically surrounded by a number of other lines, either on the same level or on different levels.

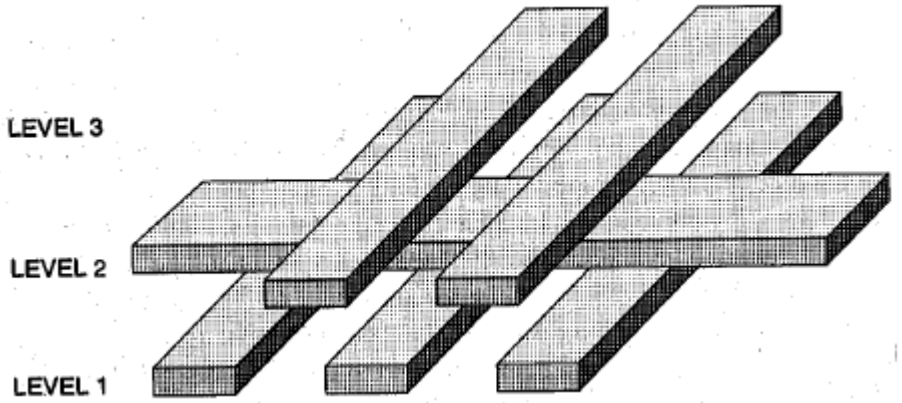


Fig: An example of six interconnect lines running on three different levels

RC Delay Model

- Assuming that the capacitance is discharged initially, and assuming that the input signal is a rising step pulse at time t = 0, the output voltage waveform of this simple RC circuit is found as
- The rising output voltage reaches the 50%-point at $t = \tau_{pHL}$, thus, we have

$$V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{RC}}\right)$$

$$V_{50\%} = V_{DD}\left(1 - e^{-\frac{\tau_{PLH}}{RC}}\right)$$

- $\tau_{pHL} = 0.69RC$

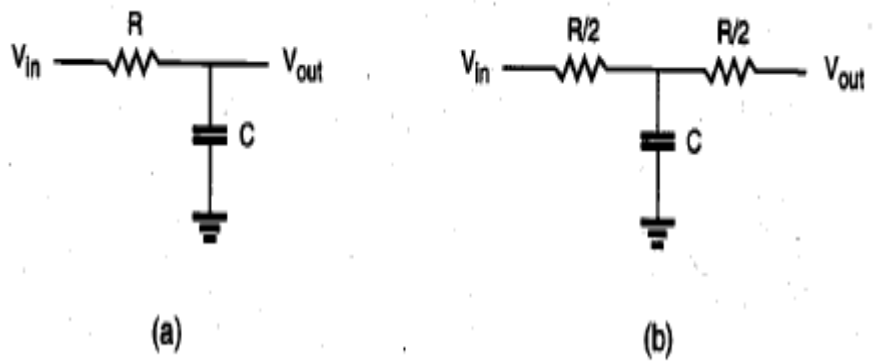


Fig: (a) Simple lumped RC model of an interconnect line, where R and C represent the total line resistance and capacitance, respectively. (b) The T-model of the same line.

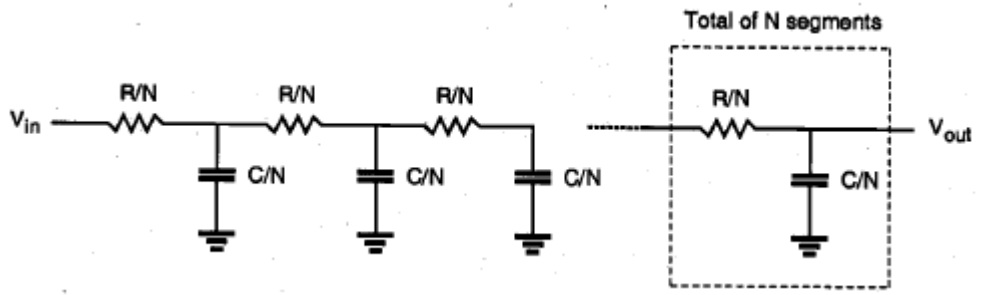


Fig: Distributed RC ladder network model consisting-of N equal segments

The Elmore Delay

- Assuming that the input signal is a step pulse at time $t = 0$, the Elmore delay at node i of this RC tree is given by the following expression.

$$\tau_{Di} = \sum_{j=1}^{N} C_j \sum_{\substack{for\ all \\ k \in P_{ij}}} R_k$$

- Calculation of the Elmore delay is equivalent to deriving the first-order time constant (first moment of the impulse response) of this circuit.
- This delay is still an *approximation* for the actual signal propagation delay from the input node to node i, it provides a fairly simple and accurate means of predicting the behavior of the RC line.

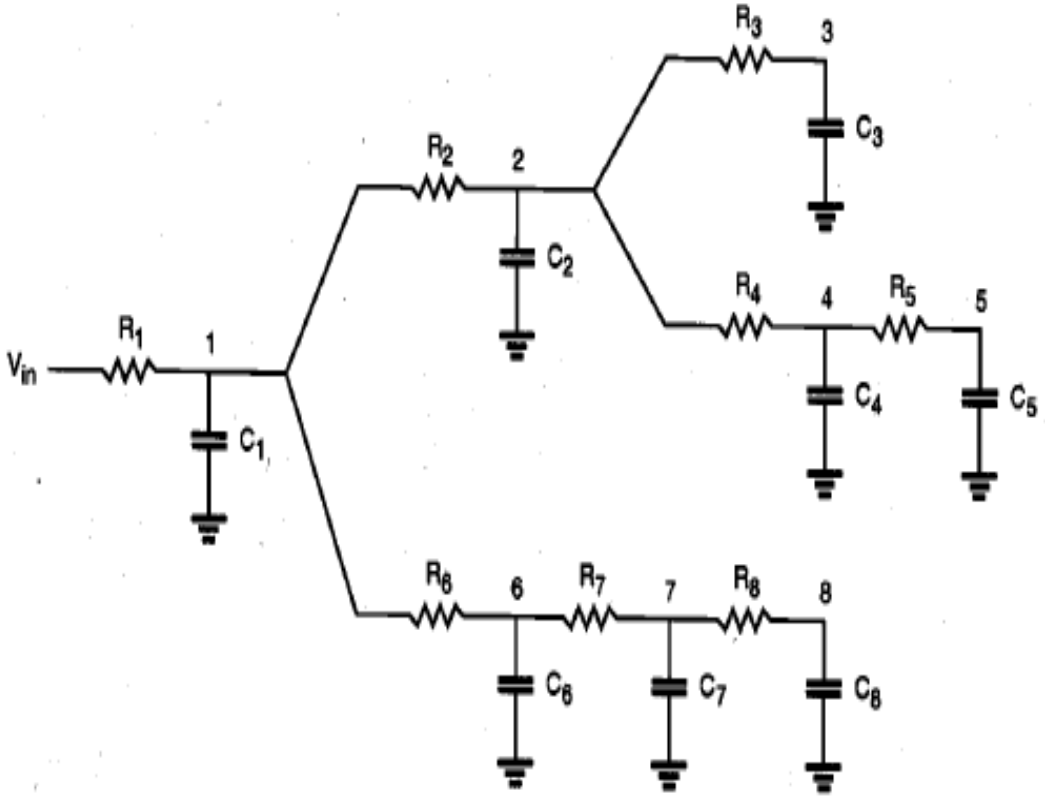


Fig: A general RC tree network consisting of several branches

The Elmore Delay

$$\tau_{D7} = R\,C + R\,C_2 + R_1\,C_3 + R_1 C_4 + R_1\,C_5 + (R_1 + R_6)\,C_6 + (R_1 + \mathbf{R_6} + R_7)C_7 + (R_1 + \mathbf{R_6} + R_7)C_8$$

- If we further assume a *uniform* RC ladder network, consisting of identical elements (R/N) and (C/N) as shown in Fig. 6.24, then the Elmore delay from the input to the output node becomes

$$\tau_{DN} = \sum_{j=1}^{N}\left(\frac{C}{N}\right)\sum_{k=1}^{j}\left(\frac{R}{N}\right)$$

$$= \left(\frac{C}{N}\right)\left(\frac{R}{N}\right)\left(\frac{N(N+1)}{2}\right) = RC\left(\frac{N+1}{2N}\right)$$

For very large N (distributed RC line behavior), this delay expression reduces to

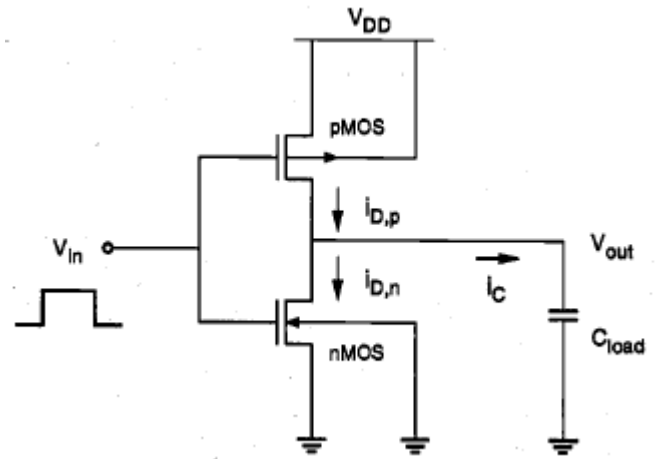
$$\tau_{DN} = \frac{RC}{2} \qquad for\ N \to \infty$$

Switching Power Dissipation of CMOS Inverters

- CMOS inverter used in the dynamic power-dissipation analysis.
- Assuming periodic input and output waveforms, the average power dissipated by any device over one period can be found as follows:

$$P_{avg} = \frac{1}{T}\int_0^T v(t)\cdot i(t)\,dt$$

$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} V_{out}\left(-C_{load}\frac{dV_{out}}{dt}\right)dt + \int_{T/2}^{T}(V_{DD}-V_{out})\left(C_{load}\frac{dV_{out}}{dt}\right)dt\right]$$



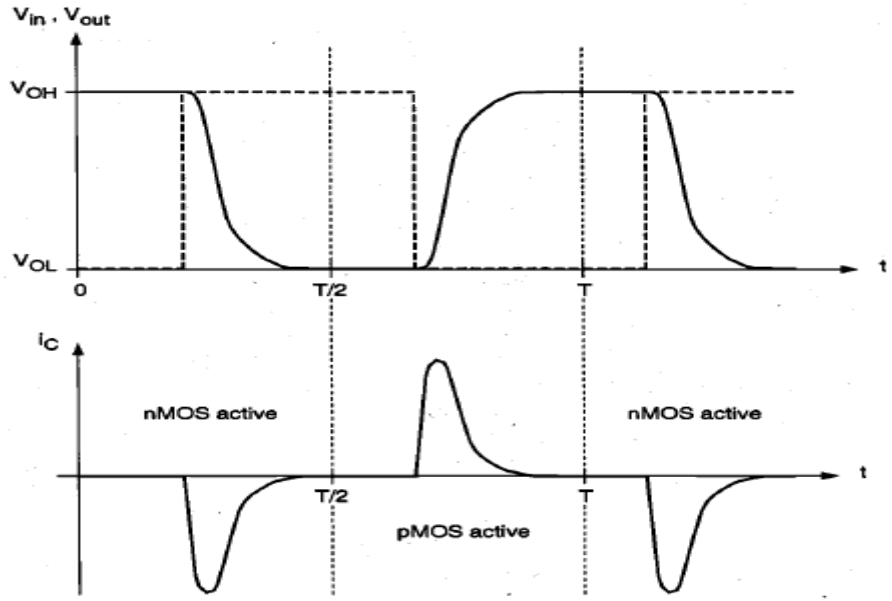


Fig.b:Typical input and output voltage waveforms and the capacitor current waveform during switching of the CMOS inverter.

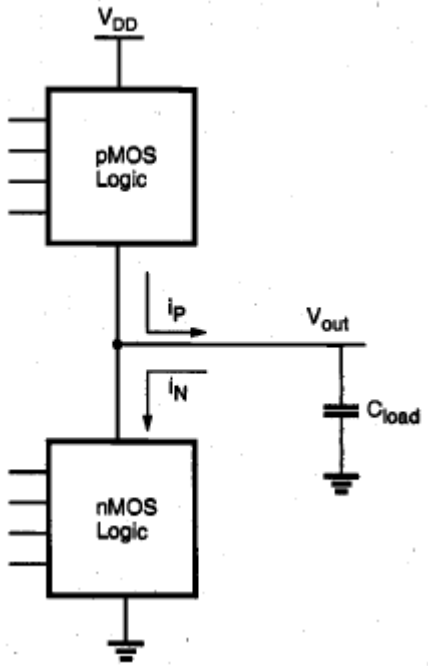
Contd.

$$P_{avg} = \frac{1}{T}\left[\left(-C_{load}\frac{{V_{out}}^2}{2}\right)\Big|_0^{T/2} + \left(V_{DD}\cdot V_{out}\cdot C_{load} - \frac{1}{2}C_{load}{V_{out}}^2\right)\Big|_{T/2}^{T}\right]$$

$$P_{avg} = \frac{1}{T}C_{load}{V_{DD}}^2$$

- Noting that f= 1T, this expression can also be written as:

$$P_{avg} = C_{load}\cdot {V_{DD}}^2 \cdot f$$



- It is clear that the average power dissipation of the CMOS inverter is proportional to the switching frequency *if* Therefore, the low-power advantage of CMOS circuits becomes less prominent in high-speed operation, where the switching frequency is high.
- Also note that the average power dissipation is independent of all transistor characteristics and transistor sizes. Consequently, the switching delay times have no relevance to the amount of power consumption during the switching events.
- The reason for this is that the switching power is solely dissipated for charging and discharging the output capacitance from *VOL* to *VOH,* and vice versa

Power-Delay Product

- The power-delay product (PDP) is a fundamental parameter which is often used for measuring the quality and the performance of a CMOS process and gate design.
- As a physical quantity, the power-delay product can be interpreted as the average *energy* required for a gate to switch its output voltage from low to high and from high to low.

$$PDP = C_{load} V_{DD}^2$$

$$PDP = 2 P_{avg}^{*} \tau_P$$

Query??