ECE164:RECONFIGURABLE ARCHITECTURE FOR VLSI

L:3 T:0 P:0 Credits:3

Course Outcomes: Through this course students should be able to

CO1 :: Discuss VLSI Design flow and Reconfigurable Architectures basics

CO2 :: Recall the Verilog HDL fundamentals and tool exposure

CO3 :: Develop combinational & sequential circuit designs

CO4 :: Simulate the combinational & sequential circuit designed in Verilog HDL using Vivado

CO5 :: Demonstrate the usage of FPGA seven segment in design implementation

CO6 :: Analyze the interfacing of FPGA for various applications

Unit I

Introduction : VLSI Design Flow, ASIC Vs FPGA, PAL,PLA,CPLD, Transistor as a switch, FPGA building Blocks: I/O, CLB, Interconnect

Unit II

Verilog Fundamentals & Vivado Design Suite : Modelling styles in Verilog, Hierarchical concepts, Coding organization and test-bench building, operators, VIVADO design suite: installation, creating a new project, constraint file generation, simulating the project, synthesis and implementation of project, bit stream generation

Unit III

Combinational Circuits: Design, Synthesis, Implementation : Arithmetic circuits : Adders, Subtractors, Multiplexer & Demultiplexer, Encoder & Decoder, Code Converters

Unit IV

Sequential Circuits: Design, Synthesis & Implementation -I : Flip Flops, counters, LFSR, Behavioral modelling Branching statement, Loops, Block Statement

Unit V

Sequential Circuits: Design, Synthesis & Implementation -II : Finite state machines (FSM), Mealy circuit design, Moore circuit design, Frequency division using counters, FPGA seven segment display driver

Unit VI

Digital Interfacing and Advanced Applications : Universal asynchronous receiver/transmitter (UART), Transmitter module, Receiver module, Digital Clock, SPI in Verilog, Calculator

Text Books:

1. DIGITAL SYSTEM DESIGN WITH FPGA - IMPLEMENTATION USING VERILOG AND VHDL by CEM UNSALAN AND BORA TAR, Mc Graw Hill Education

References:

1. FPGA-BASED SYSTEM DESIGN by WAYNE WOLF, PEARSON

2. VERILOG HDL BY SAMIR PALNITKAR, PEARSON by SAMIR PALNITKAR, PEARSON