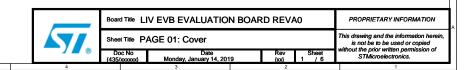
## **LIV EValuation Board**

**Schematics** 

## SHEET NAME

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Designed in OrCAD Capture 16.6 **Bloc diagram** +5V (USB) VCC VCC VCC 10 GND RF Reset 9 1Ω LNA 11 RF IN VCC 3.3V Ω0 +5V (USB) GND RF LDO VCC\_IO VCC 100Ω 13 ANT OFF VBATT TP 받 Vin -VCC Teseo-LIV3F VIO 14 VCC RF WAKE UP 5 TPS22943 10kΩ 10kΩ En ¬ΛΛΛ¬ 0Ω  $\sim$ B3/PPS 4 **B**1  $\text{Ik}\Omega^{\bullet}$  $\text{Im}_{1k\Omega}^{\text{res}}$ VCC Ω0  $\Omega$ 0 16 SDA UART RX (3 +5V (USB) VCC Ω0 10kΩ 17 SCL B0/UART TX (2) 10kΩ 0Ω FT232RQ -VV  $= 1k\Omega$ 18 B2 GND **(1)**  $\text{Ik}\Omega^{\text{l}}\Omega$ Board Title LIV EVB EVALUATION BOARD REVAO PROPRIETARY INFORMATION This drawing and the information hereir Sheet Title PAGE 02: bloc diagram

