

# Elec 2210 Test 1 Spring 2016

Sunday, September 14, 2014 2:07 PM

(OS) 85  
MA 82.11 1.1 kΩ  
1.1 kΩ  
(01)

Name:

Please spread out and leave empty seats between you and your neighbor.

1. Find the current flowing through the circuit above when saturation is just reached.

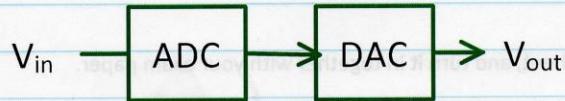
Write your name and student ID number on the back of this page and turn it in together with your exam paper.

## Digital Data (20)

Wednesday, June 13, 2012 11:58 AM

In the system below,  $n=4$ ,  $V_{FS}=16V$ .

determine the interval of  $V_{in}$  that gives the same  $V_{out}$  as  $V_{in}=8.6V$ , but satisfies  $V_{out} < V_{in}$ .  
(10)



$$V_{LSB} = \frac{16V}{2^n} = \frac{16V}{2^4} = 1$$

$$\text{signal} \approx \frac{V_{out}}{V_{in}} \Rightarrow 8.6 \approx 1000, 10 \dots \Rightarrow V_{out} = 7, 8, 9, 10 \dots$$

$$V_{in} = \text{signal} \times V_{LSB} \approx 8.6, \quad V_{LSB} = 0.5V \Rightarrow 8.5V < V_{in} < 9.5V \Rightarrow V_{out} = 9.0V$$

$$9.0V < V_{in} < 9.5V$$

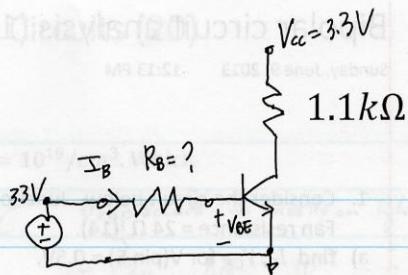
Find out the number of binary Giga Byte (GB) data that can be downloaded in 10 seconds using a 1 GBPS (giga bits per second) connection. (10)

$$\frac{1 \text{ giga bit}}{5} \cdot \frac{1 \text{ byte}}{8 \text{ bits}} \cdot \frac{10 \text{ s}}{1} \cdot \frac{1 \text{ GB}}{(1024)^3 \text{ Bytes}} \cdot \frac{(1000)^3 \text{ Bytes}}{1 \text{ GB}}$$

$$= 1.164 \text{ Binary GB}$$

## Bipolar circuit design (10)

Sunday, June 9, 2013 12:25 PM



- Find the maximum collector current for the circuit above when saturation is just reached.
- Find the  $R_B$  required to put transistor in saturation.

$\beta_F = 100$ .  $V_{BE,ON} = 1V$ ,  $V_{CE,SAT} = 0.2V$ .

$$1) \quad V_{CE,SAT} = 0.2V \Rightarrow V_{1.1k\Omega} = 3.3 - 0.2V = 3.1V$$

$$I_C = \frac{V_{ce} - V_{CE,SAT}}{R_C} = \frac{3.1V}{1.1k\Omega} = 2.82 \text{ mA}$$

$$2) \quad I_C = \beta_F I_B \Rightarrow I_B = \frac{I_C}{\beta_F} = \frac{2.82 \text{ mA}}{100} = 0.0282 \text{ mA}$$

$$R_B = \frac{V_B - V_{BE}}{I_B} = \frac{3.3V - 1V}{0.0282 \text{ mA}}$$

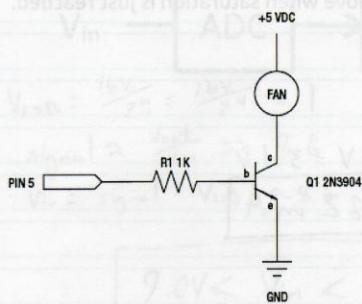
$$R_B = 81.56 \text{ k}\Omega$$

## Bipolar circuit analysis (14)

Sunday, June 9, 2013 12:13 PM

1. Consider the circuit below. Junction turn-on voltage is 1V.  $V_{CE,sat} \approx 0.2V$ .  $\beta_F = 100$ .  
 Fan resistance =  $24\Omega$ . (14).

- a) find  $I_C, V_{CE}$  for  $V(\text{pin } 5) = 0.5V$ .  
 b) find  $I_C, V_{CE}$  for  $V(\text{pin } 5) = 5V$ .



a)  $V_{BE,ON} > V(\text{pin } 5) \Rightarrow \text{off mode}$

$$\boxed{I_C = 0A}$$

$$\boxed{V_{CE} = 5V}$$

b) Assuming forward mode because  $V(\text{pin } 5) < V_{BE}$

$$I_B = \frac{V(\text{PIN } 5) - V_{BE,ON}}{R_{FAN}} = \frac{(5 - 1)V}{24\Omega} = 4mA$$

$$I_C = \beta_F I_B = (100)(4mA) = 400mA$$

$$V_{FAN} = (I_C)(R_{FAN}) = (400mA)(24\Omega) = 9.6V \Rightarrow \text{greater than } V_{DC}$$

$\Rightarrow$  Assume saturation mode

$$I_C = \frac{V_{DC} - V_{CE,sat}}{R_{FAN}} = \boxed{200mA}$$

$$\boxed{V_{CE} = V_{CE,sat} = 0.2V}$$

## PN Junction/Drift-Diffusion/Diode Circuits (20)

Sunday, June 8, 2014 5:38 PM

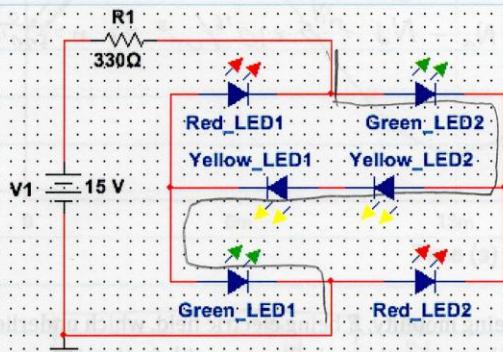
Consider a PN junction with  $N_d = 10^{17}/cm^3$  and  $N_a = 10^{19}/cm^3$ . Which of the following are true? (4)

1) Potential drop occurs mostly on the n-side. False

*Drop occurs mostly on lightly doped side*

2)  $x_p/x_n = 100$ . False

$$x_p/x_n = \frac{N_d}{N_a} = \frac{10^{17}}{10^{19}} = 0.01$$



- a) Which LEDs light up? (5)
- b) Turn on voltage is 2V. Which LEDs if any are seeing reverse voltage? (3) What are the values of the reverse voltages seen? (3)
- c) Redesign R1's value to set LED current to 3.5mA (5).

a) Green\_LED2, Yellow\_LED2, Yellow\_LED1, Green\_LED1

b) Red\_LED1 and Red\_LED2

both have  $V_{reverse} = 6V$

c)  $V_{LED\ total} = 4V_{on} = 8V$

$$V_R = 15V - 8V = 7V$$

$$R = \frac{V_R}{I} = \frac{7V}{3.5\text{mA}} = [2k\Omega]$$

## Solid-State (20)

Sunday, June 9, 2013 11:08 AM

a) What are the n and p in a Si sample with  $6 \times 10^{16}/\text{cm}^3$  phosphorous and  $5 \times 10^{16}/\text{cm}^3$  boron?

b) With additional  $6 \times 10^{16}/\text{cm}^3$  boron?  $n_i = \frac{10^{10}}{\text{cm}^3}$

$$a) N_d = 6 \times 10^{16}/\text{cm}^3, N_a = 5 \times 10^{16}/\text{cm}^3, p + N_d = n + N_a \Rightarrow N_d > N_a$$

$$N_d - N_a \gg n_i \Rightarrow n \approx N_d - N_a = 1 \times 10^{16}/\text{cm}^3 \Rightarrow p = \frac{10^{20}}{10^{16}}$$

$$n = 10^{16}/\text{cm}^3$$

$$p = 10^4/\text{cm}^3$$

$$b) N_d = 6 \times 10^{16}/\text{cm}^3, N_a = 11 \times 10^{16}/\text{cm}^3 \Rightarrow N_a > N_d$$

$$N_a - N_d \gg n_i \Rightarrow p \approx N_a - N_d = 5 \times 10^{16}/\text{cm}^3 \Rightarrow n = \frac{10^{20}}{5 \times 10^{16}}$$

$$p = 5 \times 10^{16}/\text{cm}^3$$

$$n = 2 \times 10^3/\text{cm}^3$$

Electron drift velocity  $v = \mu E$ , with  $\mu$  being mobility,  $E$  being electric field, which underlies Ohm's law,  $I = \frac{V}{R}$ . However, once  $v$  reaches saturation velocity  $v_{sat}$ , with further increase of electric field,  $v = v_{sat}$ , Ohm's law no longer holds.

1) Consider a 20nm long resistor made using state of the art 20nm technology,

$\mu = 200 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ .  $v_{sat} = 10^7 \text{ cm/s}$ . Find out the highest voltage we can apply without breaking Ohm's law.

2) Continuing, if one needs to design a resistor with Ohmic I-V for a maximum voltage of 1V, find the minimum resistor length.

$$1) E_{max} = \frac{V_{sat}}{\mu} = \frac{10^7}{200} \frac{\text{cm}}{\text{s}} \cdot \frac{\text{Vs}}{\text{cm}^2} = 50000 \frac{\text{V}}{\text{cm}}$$

$$V_{max} = E \cdot l = 50000 \frac{\text{V}}{\text{cm}} \cdot 20 \text{ nm} \cdot \frac{1 \text{ m}}{10^9 \text{ nm}} \cdot \frac{10^2 \text{ cm}}{1 \text{ m}} = \boxed{V = 0.1 \text{ V}}$$

$$2) V_{max} = E \cdot l \Rightarrow l = \frac{V_{max}}{E_{max}} = \frac{1 \text{ V}}{50000 \frac{\text{V}}{\text{cm}}} = 2 \times 10^{-5} \text{ cm} \times \frac{10^2 \text{ nm}}{\text{cm}} = 2 \times 10^2 \text{ nm}$$

$$l = \boxed{200 \text{ nm}}$$

## Rectifiers (16)

Wednesday, June 13, 2012

11:46 AM

$$\theta_c = \sqrt{\frac{2V_r}{V_p}}, \Delta T = \frac{\theta_c}{\omega}, \omega = 2\pi f$$

Design a 5V, 1A full wave bridge rectifier with a  $V_r$  no more than 100 mV.  $V_{on} = 1V$ . Frequency of ac source is 60Hz.  $V_{in} = V_p \sin(\omega t)$ ,  $\omega = 2\pi f$ .

a) Draw schematic with all diodes labeled as D1-D4. (4)

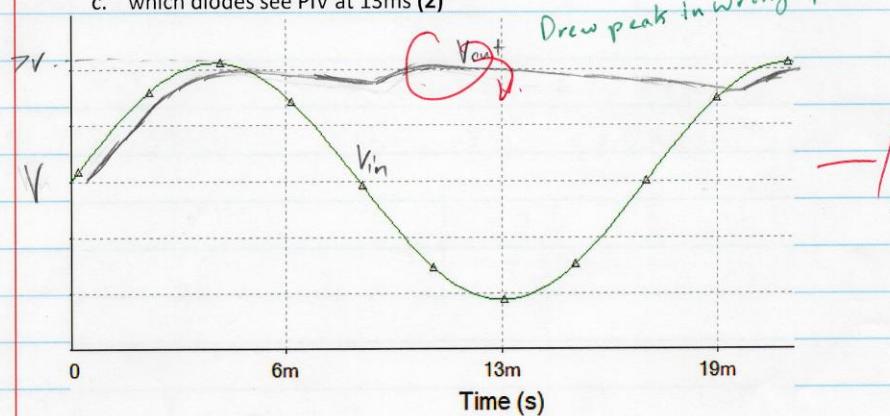
b) Find conduction angle in degree (4)

c) For the  $V_{in}$  below,

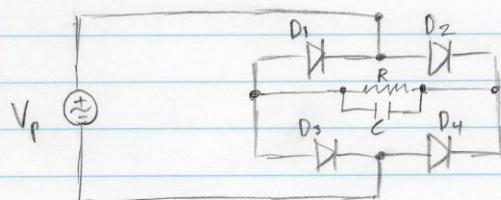
a. sketch  $V_{out}$  (4)

b. which diodes are turned on at 13ms? (2)

c. which diodes see PIV at 13ms (2)



a)



$$R = 5/1 = 552$$

b)

$$V_p = V_{DC} + 2V_{on} = 5V + 2 \cdot 1V = 7V$$

$$\theta_c = \sqrt{\frac{2V_r}{V_p}} = 0.169 \text{ rad} = \dots \text{ degree.} - 2.$$

forgot to convert  
to degrees from radians

c)

b)  $D_1$  and  $D_4$  are on

c)  $D_2$  and  $D_3$  see PIV at 13ms

98+5

## Elec 2210 Test 2

Monday, October 12, 2015 8:18 AM

Name:

Please spread  
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sample prob

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me your equation sheet  
chematics, waveforms,

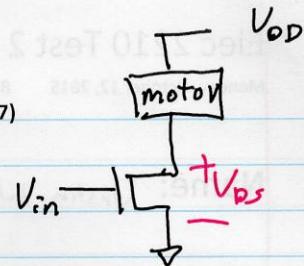
## MOSFET and complex MOSFET (25)

25

Friday, June 27, 2014 3:22 PM

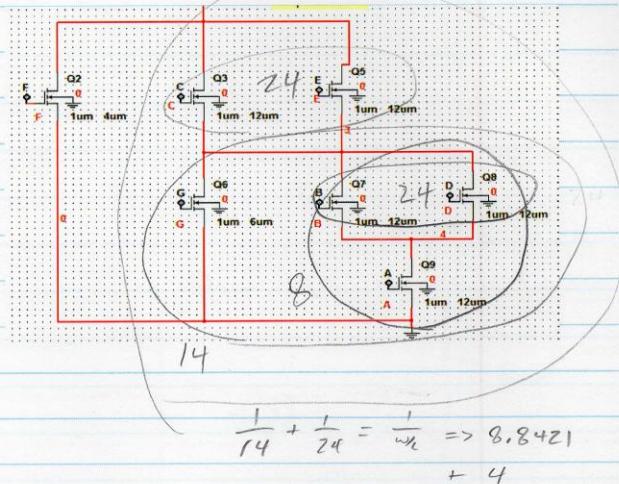
To turn on a motor with a NMOS, which biasing condition is desired? (7)

- 1) A  $V_{in}$  below threshold voltage
- 2) A  $V_{in}$  just above threshold voltage
- 3) A large  $V_{in}$  much higher than threshold voltage

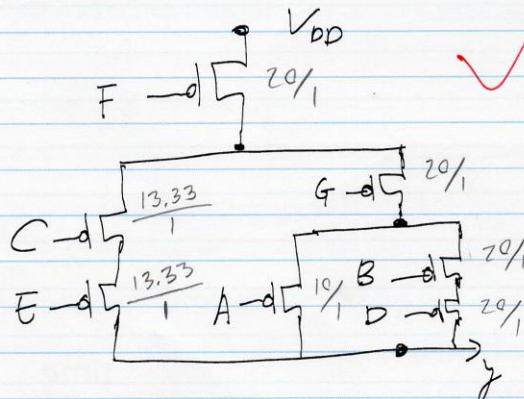


Find the equivalent W/L when all inputs switch together for the NMOS network, L=1um for all, the other number is W. (8)

$$\left(\frac{W}{L}\right)_{EQU} = \frac{12.8421 \mu m}{1 \mu m}$$



Size all PMOS for a worst case effective  $W/L = 5/1$  (10).



## Dc Inverter performance (10 points)

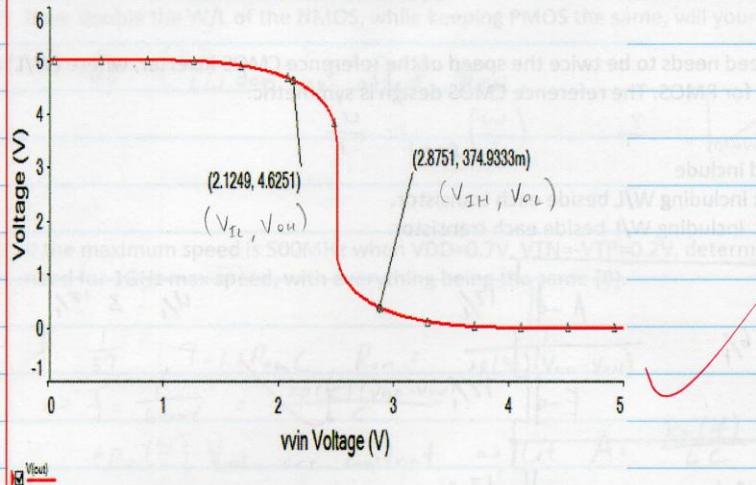
Monday, March 19, 2012

5:20 PM

10

An inverter is designed and simulated with Multisim. The "-1" slope points were obtained using cursor functions as follows:

DC Transfer Characteristic



1. 2.9V is:
- a. A valid input low
  - b. A valid input high**
  - c. An invalid input

$$2.9 > 2.8751$$

## Complex Logic Gate Design (20 points)

Monday, March 19, 2012 5:20 PM

(20)

Design a CMOS complex logic gate for the following function

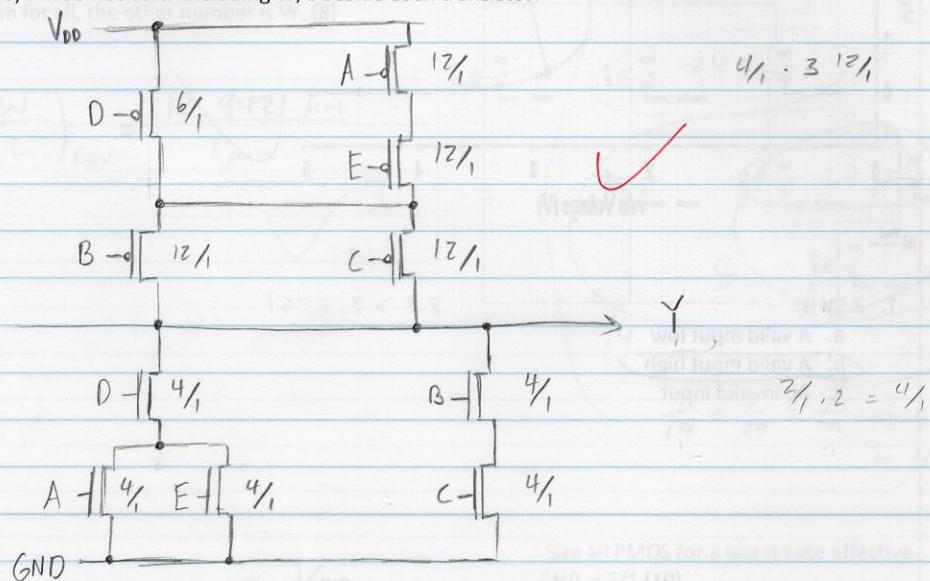
$$y = \overline{(A + E)}D + BC$$

The worst case speed needs to be twice the speed of the reference CMOS inverter, where (W/L) is 1/1 for NMOS and 2/1 for PMOS. The reference CMOS design is symmetric.

$$\left(\frac{W}{L}\right)_{NMOS} = \frac{2}{1} \quad \left(\frac{W}{L}\right)_{PMOS} = \frac{4}{1}$$

Your design should include

- (a) NMOS network including W/L beside each transistor.
- (b) PMOS network including W/L beside each transistor.



## CMOS Inverter Properties (15 points)

Monday, March 19, 2012 5:20 PM

(15)

Consider a symmetric CMOS inverter,  $V_{dd}=1V$ .

1. Assuming  $V_{TN}=-V_{TP}=0.3V$ ,
- 1) Find the  $V_{in}$  range over which  $V_{out} = 1V$  (5).  $0V < V_{in} < 0.3V$
- 2) If we double the  $W/L$  of the NMOS, while keeping PMOS the same, will your answer to 1) change? (2).

No.  $\left(\frac{W}{L}\right)_N$  does not affect  $V_{TN}$ .



1. if the maximum speed is 500MHz when  $V_{DD}=0.7V$ ,  $V_{TN}=-V_{TP}=0.2V$ , determine the  $V_{DD}$  you would need for 1GHz max speed, with everything being the same (8).

$$f = \frac{1}{5T}, T = 1.2R_{on}C, R_{on} = \frac{1}{k_P(\frac{W}{L})(V_{DD} - V_{TN})}$$

$$\Rightarrow f = \frac{1}{6R_{on}C} = \frac{k_P(\frac{W}{L})}{6C}(V_{DD} - V_{TN})$$

$k_P, (\frac{W}{L}), V_{TN}$  are constant  $\Rightarrow$  Let  $A = \frac{k_P(\frac{W}{L})}{6C}$

$$f_{old} = A(V_{DD, old} - V_{TN})$$

$$f_{new} = A(V_{DD, new} - V_{TN})$$

$\downarrow$

$$\frac{f_{old}}{V_{DD, old} - V_{TN}} = \frac{f_{new}}{V_{DD, new} - V_{TN}} \Rightarrow \frac{500 \text{ MHz}}{0.5V} = \frac{1000 \text{ MHz}}{V_{DD, new} - 0.2V}$$

$$V_{DD, new} - 0.2V = 1V \Rightarrow V_{DD, new} = 1.2V$$



$$\boxed{V_{DD} = 1.2V}$$

## digital system dynamics (10 points)

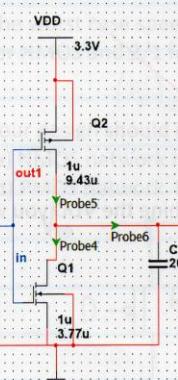
(10)

Monday, March 19, 2012 5:20 PM

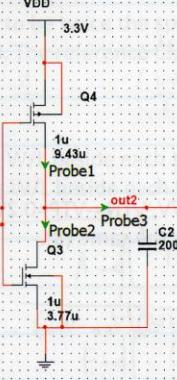
Below are voltage waveforms of input and outputs, and a few selected current waveforms of a chain of 5 inverters.

- 1) Mark the two points you need to find  $\tau_{PHL}$  of the 3rd inverter (5).
- 2) Mark the time interval during which Probe 7 flows a current with a box on the waveforms (5).

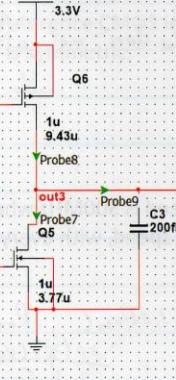
No. 1



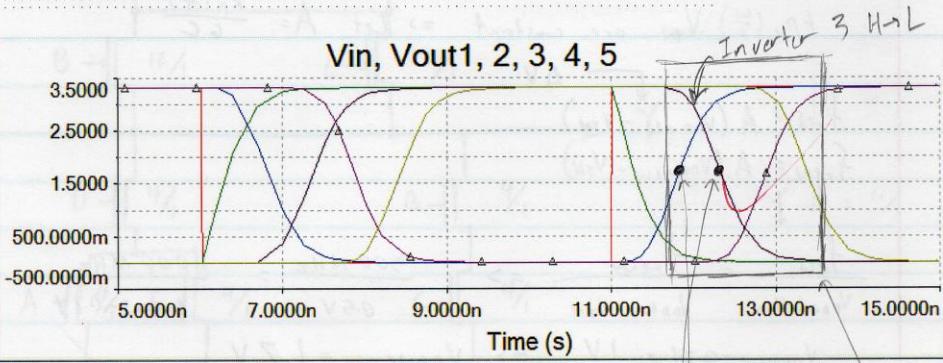
No. 2



No. 3



... no. 4 and 5  
(not shown)



f or part 1

f or part 2

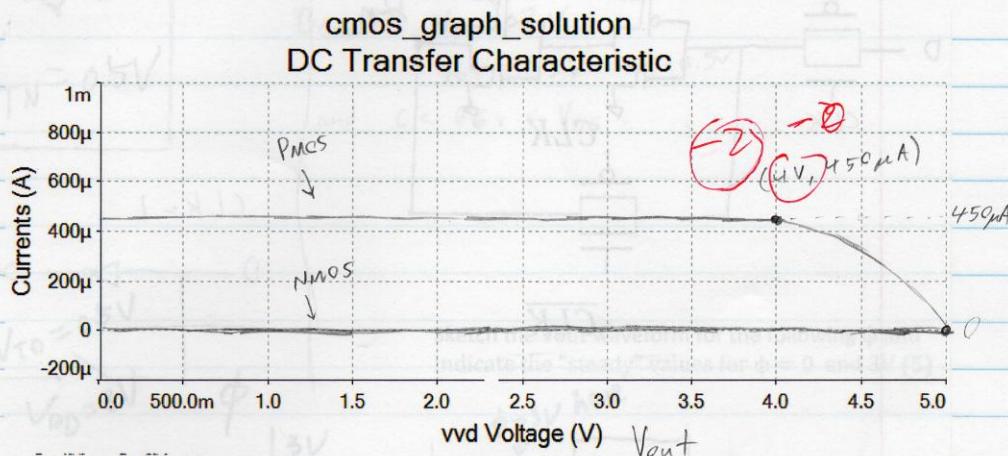
## CMOS I-V/VTC/Sizing (10)

Thursday, July 05, 2012 2:47 PM

Scored 8/10  
Sequel to Circuits (10 points)  
MR 05.2 5.25 5.5 5.75 6.0 6.25 6.5 6.75 7.0 7.25 7.5 7.75 8.0 8.25 8.5 8.75 9.0 9.25 9.5 9.75 10.0

Consider a CMOS inverter with  $K_P = 40 \mu A/V^2$  for PMOS,  $100 \mu A/V^2$  for NMOS.  $V_{TN} = -V_{TP} = 1V$ .  $W/L = 1/1$  for NMOS,  $2.5/1$  for PMOS.  $V_{DD} = 5V$ .

Sketch IDS of NMOS and ISD of PMOS as a function of  $V_d$  as  $V_d$  increases from 0 to  $V_{DD}$  at an input voltage of 1V. The transistor saturation point's current and voltage must be explicitly calculated and labeled for both NMOS and PMOS,  $V_{out}$  must be labeled as well.



Hints: Draw schematic, find VGS of NMOS and PMOS first.

$$\text{NMOS: } V_{in} \Rightarrow V_{GS} = 1V \Rightarrow V_{GT} = 1V - 1V = 0V \Rightarrow \text{off} \quad \checkmark$$

$$\text{PMOS: } V_{GS} = -4V \Rightarrow V_{GT} = -3V$$

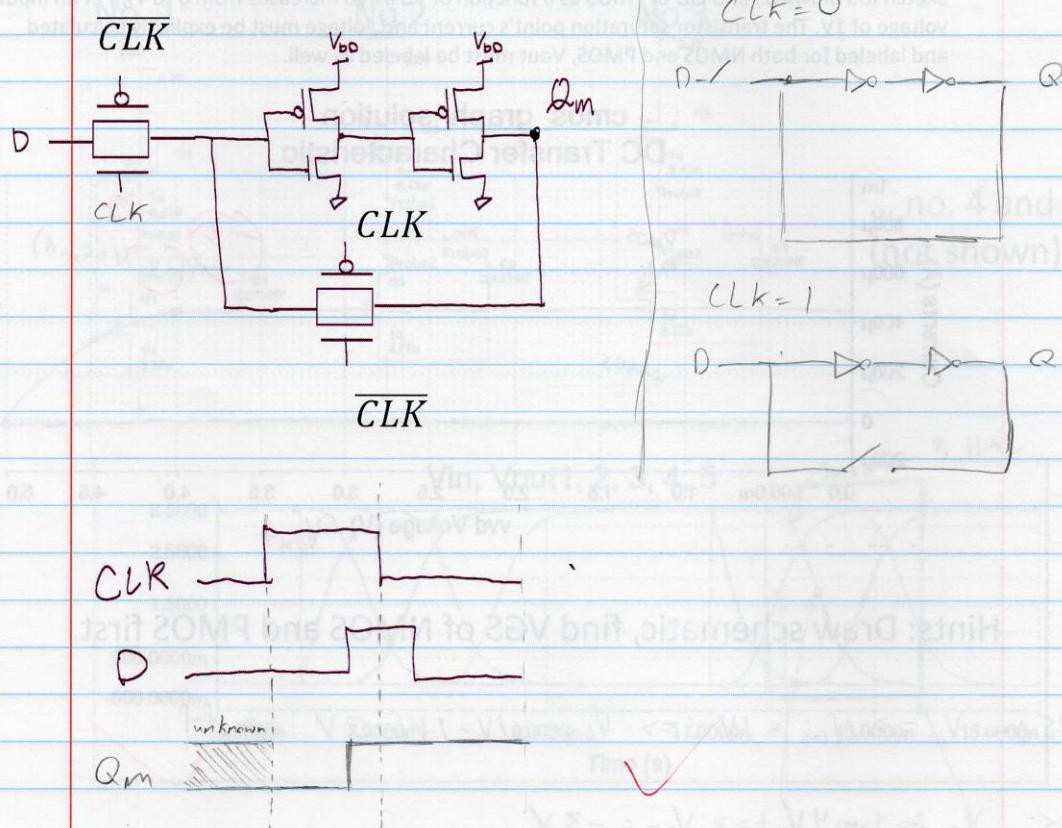
$$I_{DS, \text{sat}} = \frac{1}{2} k_P \left( \frac{W}{L} \right) V_{GT}^2 = \frac{1}{2} (40 \mu A/V^2) (2.5/1) 3^2 = 450 \mu A$$

### Sequential circuits (10 points)

Monday, March 19, 2012 5:20 PM

(10)

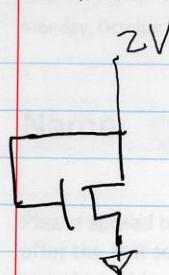
Draw waveform of  $Q_m$ . For unknown state, just label it as "unknown".



## Bonuses (10 points)

Tuesday, March 22, 2016 9:08 AM

(5)



Is the transistor on the left working in saturation or linear region? Why? (5)

saturation region

Because  $V_{DS} = 2V$

$$V_{OT} = 1.5V = 2V - 0.5V$$

$$\text{and } 0 < V_{OT} < V_{DS}$$

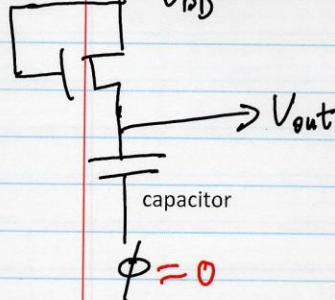
✓

$$V_{TN} = 0.5V$$

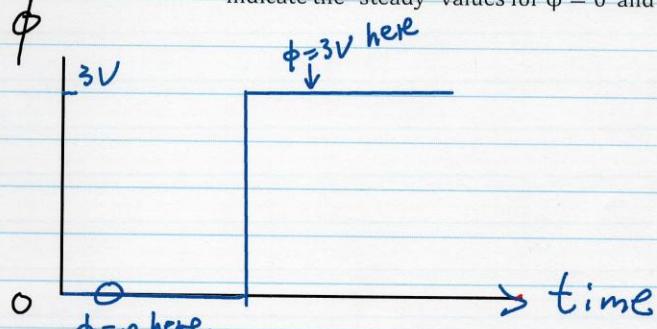
$$V_{TO} = 0.5V$$

$$V_{OD} = 3V$$

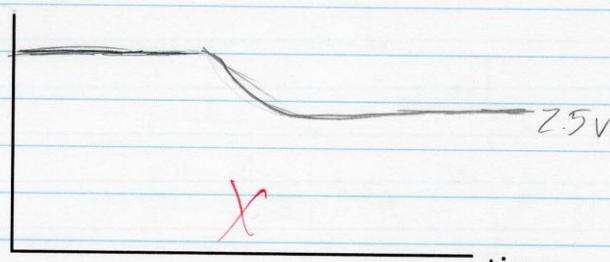
$\phi$



Sketch the  $V_{out}$  waveform for the following  $\phi$  and indicate the "steady" values for  $\phi = 0$  and  $3V$  (5)



$V_{out}$



## Elec 2210 Test 3

Monday, November 16, 2015 8:16 AM

5/10

85+5

(10)

Name:

1. One  
only  
etc)  
is nc
2. Leave \_\_\_\_\_

equation sheet with equations  
gs no text, no sample problems  
tor memory, phone, watch use  
on the schematic below. Show all resistances

minimum between you and  
your neighbor

## 7.28 Buffer (10)

10

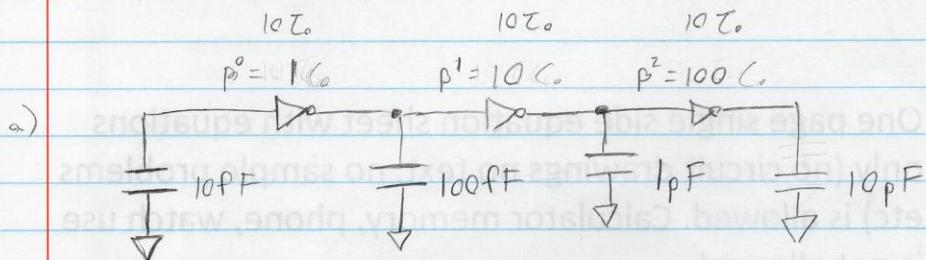
Wednesday, April 20, 2016 11:21 AM

Elec 5330 Test 3

MA333 - 2016 - 2017 Academic Year

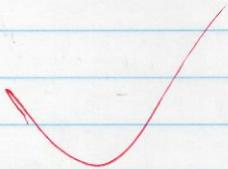
Design a 3 stage buffer with these parameters:  $C_0=10fF$ ,  $C_L=10pF$ .

- Draw schematic, including numerical values of all capacitances and relative sizes of each stage (7)
- Determine the buffer delay in multiples of reference delay  $\tau_0$  (3).



b)

$$\begin{aligned} \text{delay} &= 10\tau_0 + 10\tau_0 + 10\tau_0 \\ &= [30\tau_0] \end{aligned}$$

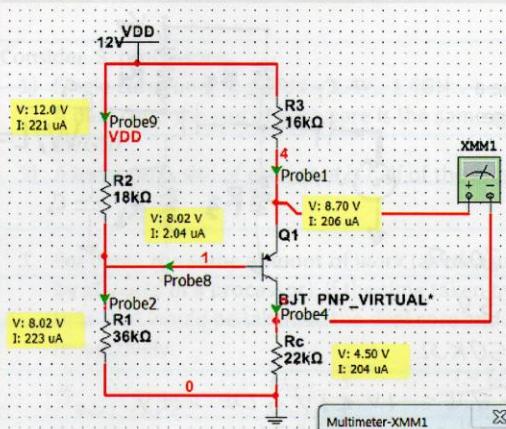


## Bipolar 4R Biasing (10).

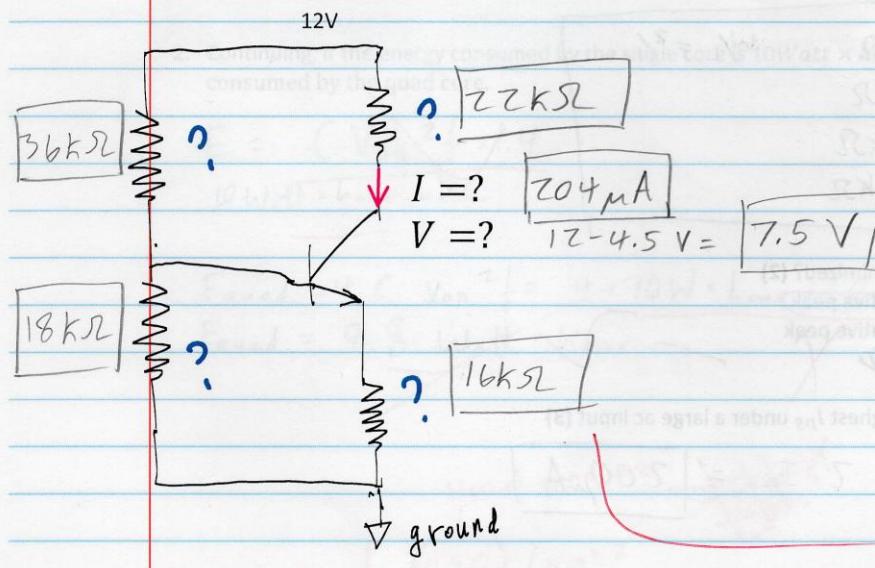
Friday, July 19, 2013 5:04 PM

10

Moat AR (12)



Convert the PNP design above to a NPN design on the schematic below. Show all resistances and the V and I at the probe.

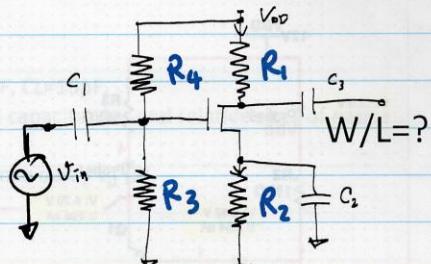


## Mos 4R (15)

13

Friday, April 13, 2012 5:04 PM

- Design  $R_1, R_2, R_3, R_4$  and  $W/L$  to give  $I_{DS}=100\mu A$  with  $V_{DD}=12V$  and  $R_{EQ}=120k\Omega$ ,  $K_P=100\mu A/V^2$ .  $V_{TO}=1V$ .  $V_{GT}$  needs to be 1V. Use a 2V DC feedback and maximize output voltage swing (10).



$$V_S = 2V \Rightarrow R_2 = \frac{V_S}{I_{DS}} = \frac{2V}{100\mu A} = 20k\Omega$$

$$V_{PS} \approx V_{R1} = \frac{V_{DD} - V_S}{2} = \frac{12V - 2V}{2} = 5V$$

$$V_{R1} = 5V \Rightarrow R_1 = \frac{V_{R1}}{I_{PS}} = \frac{5V}{100\mu A} = 50k\Omega$$

$$V_G = V_{GS} + V_S = V_{OT} + V_{TO} + 2V = 1V + 1V + 2V = 4V$$

$$R_4 \cdot V_G = V_{DD} \cdot R_{EQ} \Rightarrow R_4 = \frac{V_{DD}}{V_G} \cdot R_{EQ} = \frac{12V}{4V} \cdot 120k\Omega = 360k\Omega$$

$$\frac{1}{R_3} = \frac{1}{R_{EQ}} - \frac{1}{R_4} = \frac{1}{120k\Omega} - \frac{1}{360k\Omega} \Rightarrow R_3 = 180k\Omega$$

$$I_{DS} = \frac{1}{2} k_P \frac{W}{L} V_{GT}^2 \Rightarrow \frac{W}{L} = \frac{2 \cdot I_{DS}}{k_P V_{GT}^2} = \frac{2 \cdot 100\mu A}{100\mu A/V^2 \cdot 1^2} = 2/1$$

$$R_1 = 50k\Omega \quad \frac{W}{L} = 2/1$$

$$R_2 = 20k\Omega$$

$$R_3 = 180k\Omega$$

$$R_4 = 360k\Omega$$

- When is  $V_{DS}$  minimized? (2)

- a. Input positive peak
- b. Input negative peak
- c. Input at 0V
- d. At DC

- Estimate the highest  $I_{DS}$  under a large ac input (3)

$$I_{DS, max} = 2 \cdot I_{DS} = 200\mu A$$

## Multicore (15)

Friday, July 19, 2013 5:04 PM

Consider 3 processors:

- 1) Single core running at  $V_{dd} = 1.4V$ ,  $1.4GHz$ .
- 2) A dual core, the size of each core is the same as the original core above,  $V_{dd} = 0.7V$ ,  $f = 0.7GHz$ .
- 3) A quad core, size of each core is half of the original core in 1),  $V_{dd} = 0.7V$ ,  $f = 0.7GHz$ .

1. For doing the same amount of work (as measured by the total number of clock cycles run by all cores in a processor), if the time taken by the single core in 1) is 1hour, find out the time that would be taken by the dual core and quad core processors in 2) and 3), respectively.

$$t_{\text{Dual core}} = \frac{N_{\text{core}} \cdot f}{N_{\text{core}} \cdot f} = \frac{1.4GHz}{2 \cdot 0.7GHz} = 1 \Rightarrow 1 \text{ hour}$$

$$t_{\text{quad core}} = \frac{1.4GHz}{4 \cdot 0.7GHz} = 0.5 \Rightarrow 30 \text{ min}$$

2. Continuing, if the energy consumed by the single core is  $10Watt \times hour$ , find the energy consumed by the quad core.

$$E = CV_{dd}^2 f \cdot t$$

$$10 \text{ Watt} \times \text{hour} \Rightarrow C$$

~~$$E_{\text{quad}} = 4C V_{dd}^2 f = 4 \cdot 10W \times \text{hour} \cdot (0.7V)^2 (0.7f)$$~~

~~$$E_{\text{quad}} = 9.8 \text{ Watt} \times \text{hour}$$~~

~~size of quad core~~ ~~4~~ - 4!

$$\frac{10 \text{ Watt} \times \text{hour}}{\cancel{(0.5)} \cancel{(1.4)} \cancel{(1.4)^2}} = \frac{(0.5)}{(0.5)} \cdot (0.5)^2 = 1.25 \text{ Watt} \times \text{hour}$$

## Standby power (10)

Monday, November 16, 2015 8:52 AM

Design R<sub>1</sub>, R<sub>2</sub>, R<sub>3</sub> and W/L to give I<sub>off</sub>100nA with V<sub>DD</sub>=12V and R<sub>DS</sub>=120Ω, K<sub>P</sub>=W=20nm, L=20nm, S=75mV. Find the V<sub>th</sub> required to keep off current below 0.01nA

for use in a DRAM cell.

$$I_{off} = 100\text{nA} * \frac{W}{L} 10^{-\frac{V_{th}}{S}}$$

W=20nm, L=20nm, S=75mV. Find the V<sub>th</sub> required to keep off current below 0.01nA  
for use in a DRAM cell.

$$0.01\text{nA} = 100\text{nA} \cdot \frac{20\text{nm}}{20\text{nm}} \cdot 10^{-\frac{V_{th}}{75\text{mV}}}$$

$$10^{-4} = 10^{-\frac{V_{th}}{75\text{mV}}}$$

↓

$$-4 = -\frac{V_{th}}{75\text{mV}}$$

$$V_{th} = 75\text{mV} \cdot 4$$

$$\boxed{V_{th} = 300\text{mV}}$$

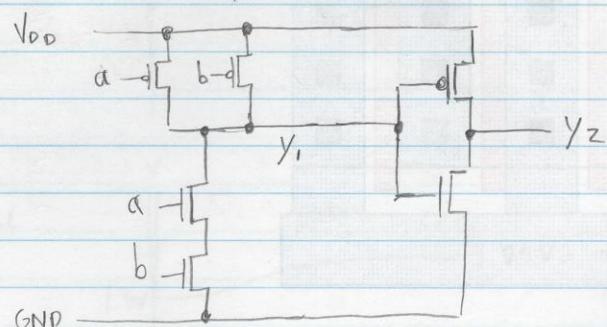
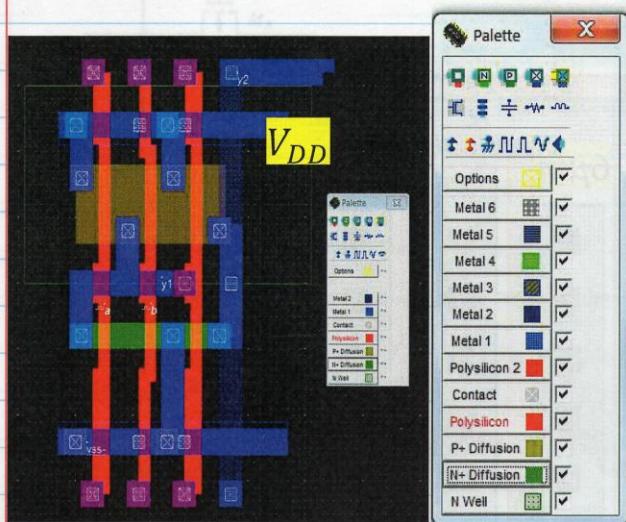
2. Estimate the highest I<sub>ds</sub> under a large ac input (3)

## Layout 1 (10)

Thursday, July 19, 2012 3:34 PM

Wednesday, April 20, 2016 11:55 AM

- draw transistor level schematic, find  $y_1$  and  $y_2$  as functions of  $a$  and  $b$ .



$$y_1 = \overline{ab}$$

$$y_2 = \overline{\overline{ab}} = ab$$

## Layout 2 (10)

Wednesday, April 20, 2016 9:51 PM

10

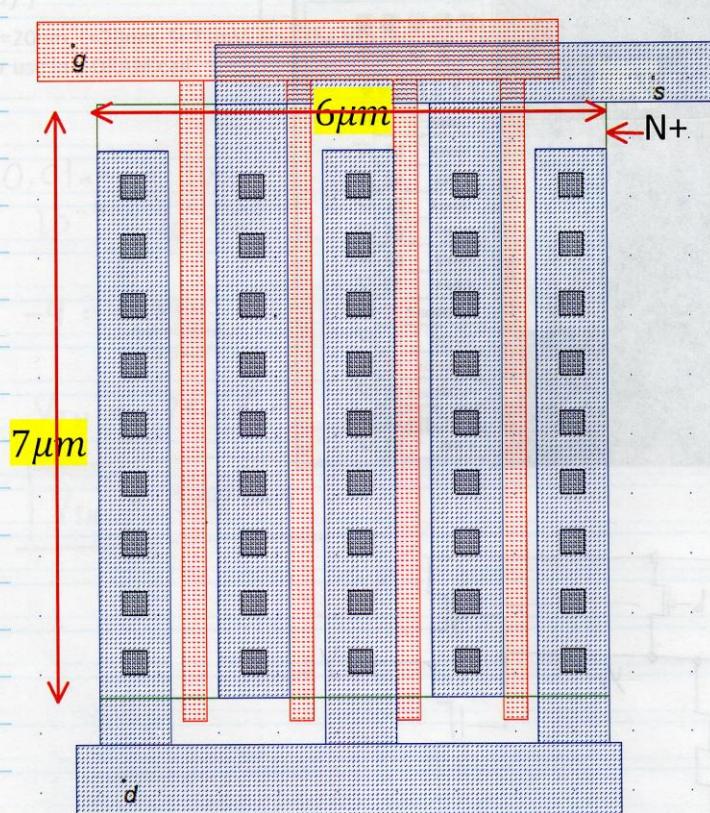
Friday, November 10, 2017 8:53 AM

(01) f Juvyse

MARBLE

SOCIAL SECURITY NUMBER

The green n+ rectangle size is 6um (horizontal) x 7um (vertical), minimum feature size is 0.2um, find the effective W of the multi-finger layout.



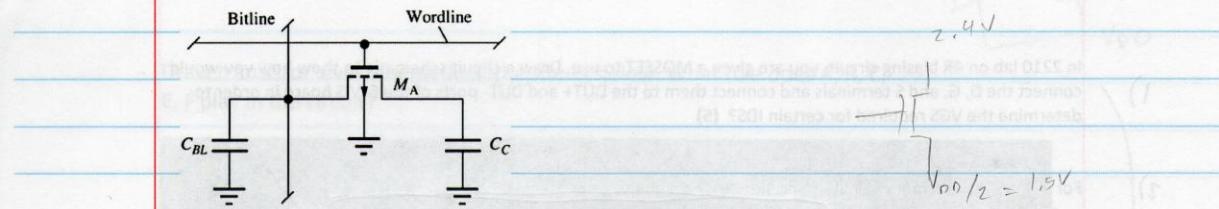
$$\left(\frac{w}{c}\right) = \frac{7 \mu m}{0.2 \mu m} = \frac{35}{1} \text{ or } \frac{7 \mu m}{0.2 \mu m}$$

$$\left(\frac{w}{c}\right)_{\text{EFF}} = 4 \cdot \frac{7 \mu m}{0.2 \mu m} = \frac{28 \mu m}{0.2 \mu m} \text{ or } \frac{140}{1}$$

# DRAM (10)

Wednesday, April 20, 2016

11:55 AM



2.4V

$$V_{DD}/2 = 1.5V$$

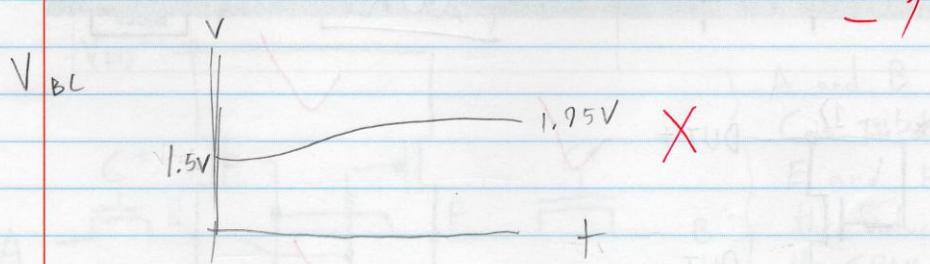
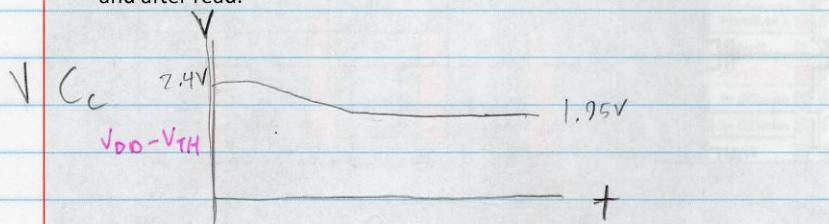
$V_{DD} = 3V$ . Transistor  $V_T = 0.4V$ .  $C_{BL} = 100C_C$ .

- 1) Assuming a cell storing "0" is written with a "1". What will the voltage across  $C_C$  be after writing is complete?

- 2) Next, bitline is precharged to  $V_{DD}/2$  to read the cell, calculate the voltage across  $C_C$  after reading is complete.

$$V_{CC} = \frac{2.4V + 1.5V}{2} = 1.95V$$

Sketch the waveform of cell capacitor voltage and bit line voltage before and after read.



$$V_F = \frac{V_{DD} \cdot C_{BL} + 2.6V \cdot C_C}{C_{BL} + C_C}$$

$$\Delta V = V_{DD} - V_F$$

## Layout 2 (10)

### Misc (10)

Monday, November 16, 2015 9:21 AM

10

1)

In 2210 lab on 4R biasing circuit, you are given a MOSFET to use. Draw a circuit schematic to show how you would connect the D, G, and S terminals and connect them to the DUT+ and DUT- ports of the ELVIS board in order to determine the VGS required for certain IDS? (5)

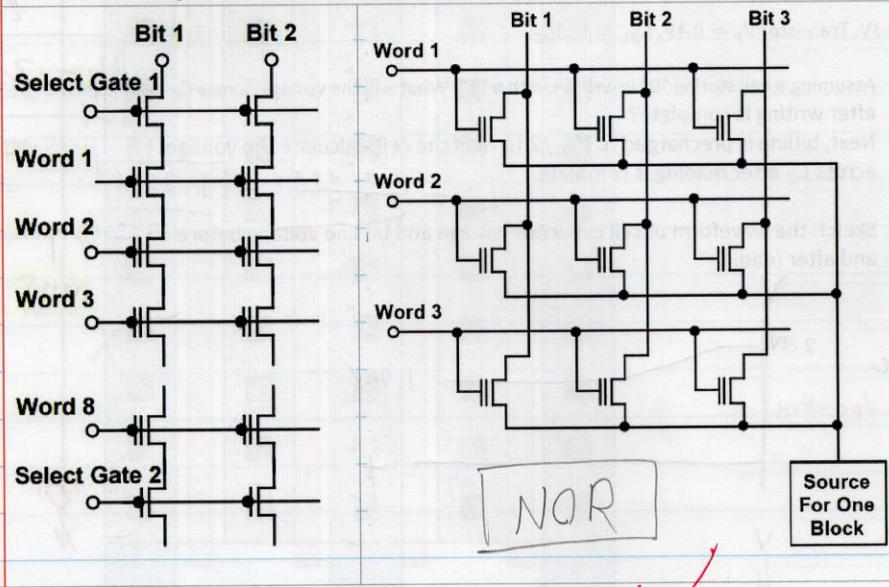
2)

For a 1-bit flash memory cell, how should the read voltage be chosen? (2)

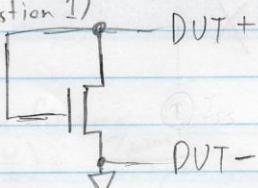
- a) Below  $V_{th}$  of erased cell; b) above  $V_{th}$  of erase cell but below  $V_{th}$  of programmed cell

3)

Which of the following is NOR? (1) Which has a higher density, left or right circuit, and why? (2)



Question 1)



DUT+

DUT-

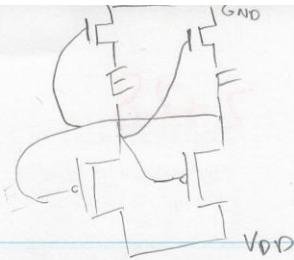
Question 3)

Left circuit has higher Density  
Less Word / Bit line circuitry required

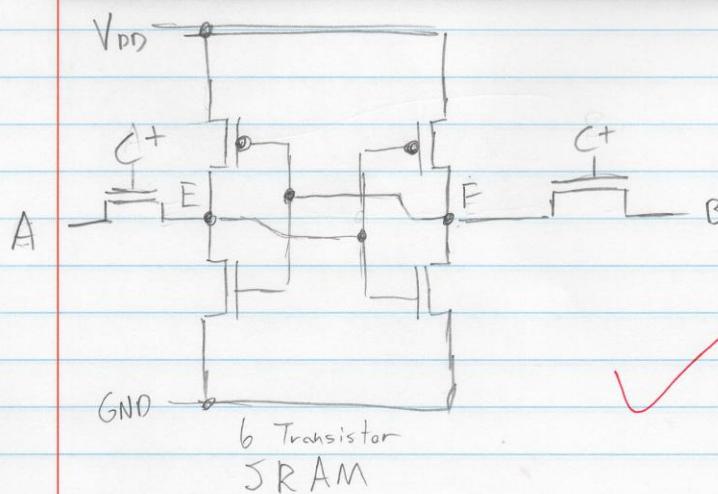
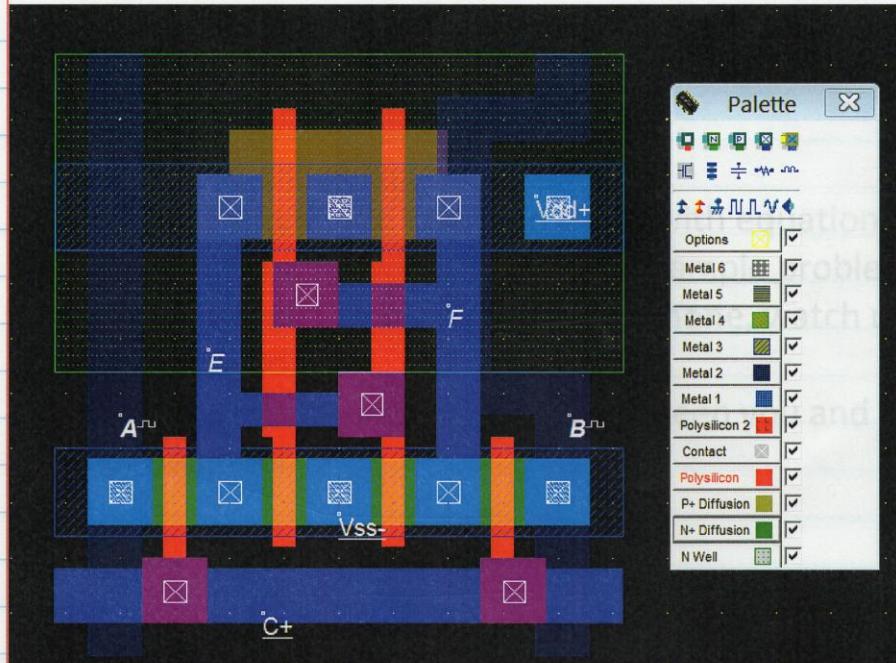
## Bonus (5) Test 3

Wednesday, April 20, 2016 4:41 PM

5



- Draw transistor level schematic of the circuit below. What role does A, B, C, E, F play in the circuit?



A and B are bitlines  
C is word line  
E and F are the value that the SRAM is holding ✓