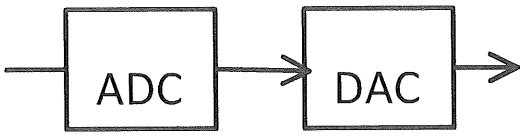
Name: Paul Breck ID: pmb0026

Thursday, September 20, 2018 11:58 AM



Q1. In the system given, n=4, V_{FS}=16V.

- Find V_{out} for $V_{in} = 10.24V$ **(5)**

$V_{out} =$ 10 V

$V_{lsb} = \frac{V_{FS}}{2^n} = \frac{16}{2^4} = 1$

$\frac{10.24}{1} = 10_{10} \Rightarrow 10.1 = 10\ V$

or

ADC 1010 DAC

- Continuing, find the binary code at the input of the DAC **(5)**

$Code =$ 1010

Q2. How many binary EB of memory can a 64 bit processor address? **(5)**

$2^{60} \cdot 2^4$

$Ans =$ 16 *Binary EB*

Q3. Check all cases where the foreign atom is a donor **(4)**

- ☐ B in Si
- ☑ P in Si
- ☑ As in Si
- ☐ Si replacing In when introduced into InP

Q4. A Si sample is doped with $N_d = 2 \times 10^{17} cm^{-3}$, $N_a = 3 \times 10^{17} cm^{-3}$, find n and p. $n_i = 10^{10} cm^{-3}$. **(6)**

$p = \frac{N_a - N_d + \sqrt{(N_a - N_d)^2 + 4n_i^2}}{2}$

$p = 1 \times 10^{17}$

$n =$ 1000 cm^{-3}

$p =$ 1×10^{17} cm^{-3}

$N = \frac{n_i^2}{p}$

$N = 1000$

Q5. Consider an n-type 10nm long Si resistor. Saturation velocity is $10^7 \frac{cm}{s}$. Electron mobility is $100 \frac{cm^2}{V \cdot s}$. Calculate the highest voltage we can apply without breaking Ohm's law **(5)**.

$V = \frac{V_{in}}{L} \mu$

$\frac{10nm}{10^{-5}} \frac{1cm}{1e^{-4}}$

$10^7 = \frac{x}{1e^{-4}} \cdot 100$

$x = 10\ V$

$V_{highest} =$ 10 V

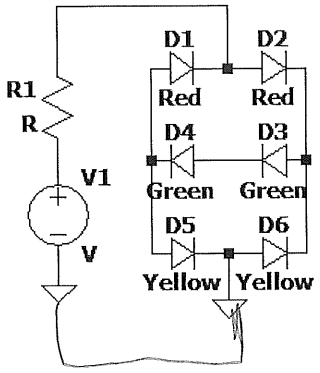
Q6. The left and right contacts of a n-type semiconductor are biased at 0V and 5V, respectively, which of the following statements are true: **(5)**:

- ☑ The left contact acts as source of electrons
- ☐ The right contact acts as source of electrons
- ☐ Electrons flow from left to right
- ☑ Current flows from left to right
- ☐ Current flows from right to left

Q7. Turn on voltage is 2.5V for all LEDs, V1= $-15V$

a) Which diodes (e.g. D1, D2 ...) are lighting up? **(5)**

- ☑ D1
- ☐ D2
- ☑ D3
- ☑ D4
- ☐ D5
- ☑ D6



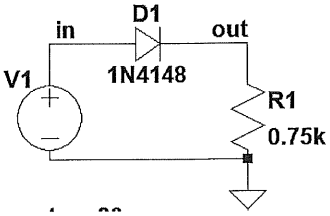
b) Calculate R1 in $k\Omega$ required for 5mA diode current **(5)**.

$4 \times 2.5 = 10$

$V = IR \qquad \frac{5}{.5} = 1k\Omega$

$R_1 =$ 1 $k\Omega$

Q8. Consider switching V1 from 5V to -5V, and the diode has a finite response time. Turn on voltage is 1V.



a) What is V(out) right after the switch? **(3)**

$V(out) =$ −5 V

b) Calculate the diode current in mA right after the switching including sign **(2)**

$V = IR \qquad \frac{-5}{.75} = -6.667\ A$

$I(D_1) =$ −6667 mA

Q9.

β_F=100. $V_{BE,on} = 0.7V$, $V_{ce,sat} = 0.2V$.

a. Find I_C at $V_{in} = 0.3V$. **(5)**

$I_C =$ 0 mA off-mode $V_{IN} < V_{BE,on}$

b. Find $\beta = I_C/I_B$ at V_{in}=5V **(5)**.

$\beta =$ 100

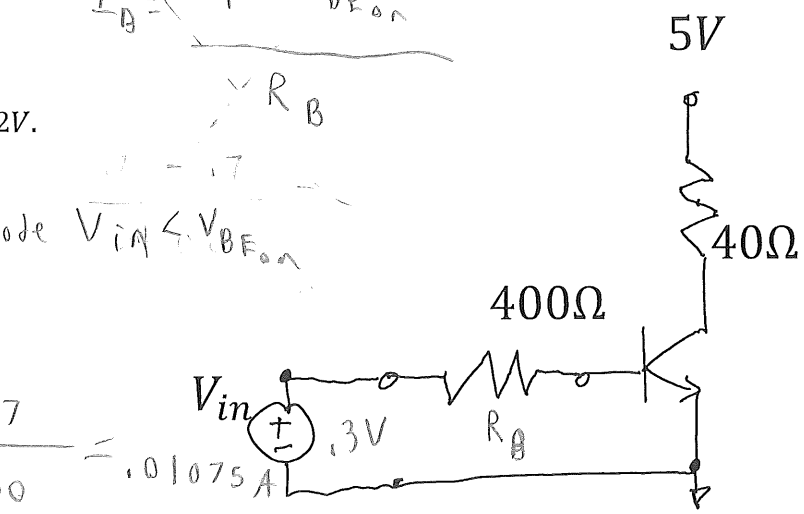
$I_B = \frac{V_1 - V_{BE,on}}{R_B}$

$\frac{5 - .7}{400} = .01075\,A$

$I_C = \beta_F \cdot I_B$

$100 \cdot .01075 = 1.075\,A$

$\beta = \frac{I_C}{I_B} = \frac{1.075}{.01075} = 100$



Q10. For the ltspice simulation shown, determine

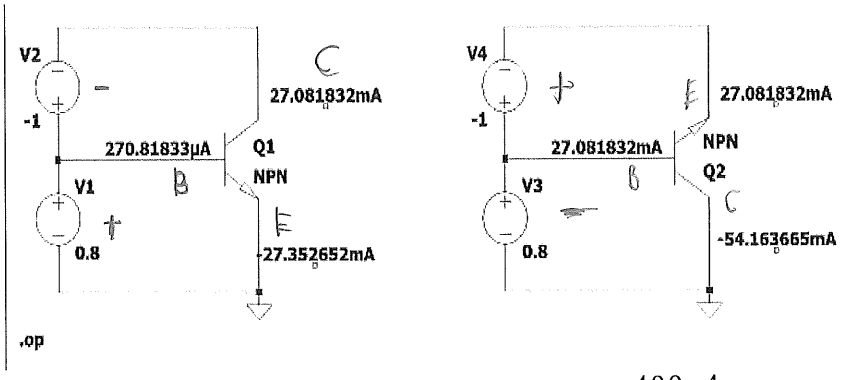
a. β_F **(5)**

$\beta_F =$ ≈100

a. β_R **(5)**

$\beta_R =$ ≈2

$\beta_R = \frac{I_C}{I_B} - 1$



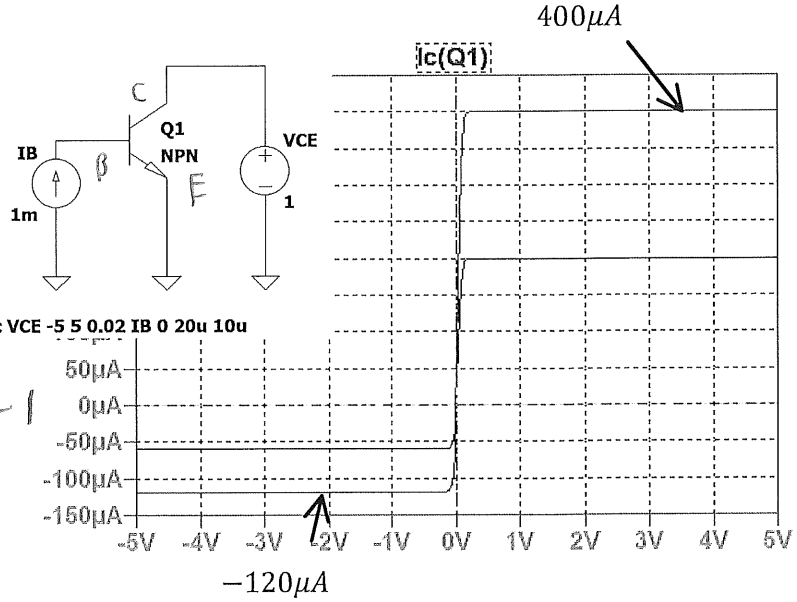
Q11. From the spice simulation shown,

a) Find β_R **(3)**

$\beta_R =$ -.88

$\beta_R = \frac{-I_C}{I_B} - 1$

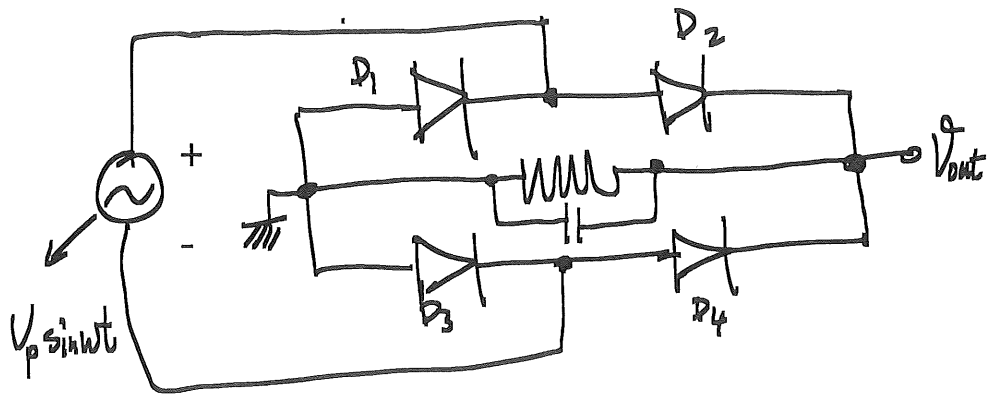
$-\left(\frac{-129\,mA}{1\,mA}\right) - 1$



b) Circle on the graph the saturation operation region **(4)**

c) The arrow on the transistor symbol means: **(3, check all that apply)**

- ☐ It points from P to N
- ☐ It is meaningless
- ☑ It indicates the emitter



Q12. Design a 5V, 5A full wave bridge rectifier with a V_r no more than 10 mV. Von=0.5V. Frequency is 50Hz. $\omega = 2\pi f$.

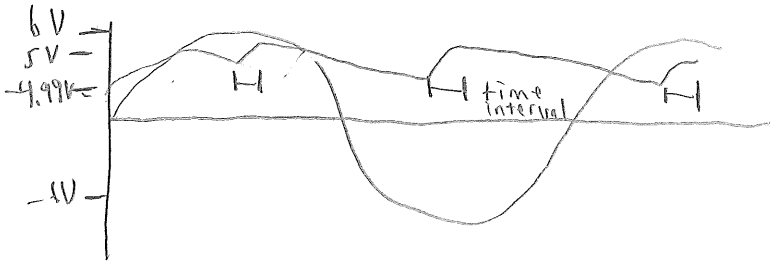
$T = \frac{1}{f} = \frac{1}{50}$

$C = \frac{I_{DC}\, T}{2\, V_r} = \frac{5 \cdot 1/50}{2 \cdot .01} = 5\,F$

a) Find C required **(3)**.

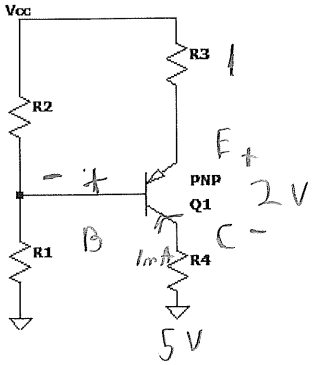
a) Find V_P required **(2)**. $V_P = V_{DC} + 2V_{on} = 5 + 2 \cdot .5 = 6\,V$

b) Sketch Vin=$V_P \sin \omega t$ and V_{out} for the first complete period, from 0 to T, indicate time intervals during which D4 is on **(5).**



Q13.

Design a 4-resistor PNP biasing circuit to achieve: $V_{R_3} = 1V$. $V_{EC} = 2V$. $I_C = 1\,mA$. $\beta_F = 50$. $V_{CC} = 5V$. $\phi_t = 0.0258\,V$. $I_S = 10^{-15}A$. Your design should include $V_{EB}, R_1, R_2, R_3, R_4$. Must use I_S for turn-on voltage calculation. **(10)**



$V_{EB} = \phi_t \ln\left(\frac{I_C}{I_S}\right)$

$.0258 \ln\left(\frac{1 \times 10^{-3}}{10^{-15}}\right) = .712\,V$

$V_{EB} = V_{on} = .712\,V$

$R_2 = \frac{V_{CC} - V_{EB}}{10\, I_B}$ $V_B = V_{CC} - V_{R_E} - V_{EB}$ $V_{R_E} = 1\,V$ $-V_B - V_{CC} + V_{EB} = 0$

$5 - 1 - .712 = 3.288\,V$ $V_B = -4.288$

$R_1 = \frac{V_B}{11 I_B}$ $\frac{I_C}{\beta_f} = I_B$ $I_B = 2 \times 10^{-5}\,A$ $\frac{-4.288}{11 \cdot 2 \times 10^{-5}\,A} \approx 19.5\,k\Omega$

$\frac{5 - .712}{10 \cdot 2 \times 10^{-5}\,A} \approx 21.5\,k\Omega$

Name: Paul Brock ID: 903932140

Q1. To use an NMOS as a closed switch, what are desired **(6, 1.5 pts each)**:

- ☐ $V_{GS} < V_{TH}$
- ☐ $V_{DS} = V_{DD}$
- ☑ $V_{GS} \gg V_{TH}, V_{DS} \approx 0$
- ☐ $\frac{W}{L} \gg 1$

Q2. Given a CMOS inverter, if we increase V_{DD}, what happens **(6, 1.5 pts each)**:

- ☑ V_{IL} *(worst case input low)* increases
- ☑ Noise margin high and low both increase
- ☑ Maximum speed increases
- ☐ τ_p increases

Q3. Consider a symmetric CMOS inverter with 1ns delay, if we double (W/L) of PMOS, while keeping everything else the same, determine **(6, 3 pts each)**:

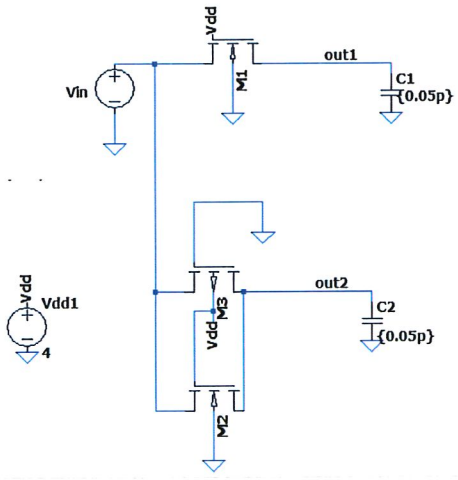
a) High to low delay:

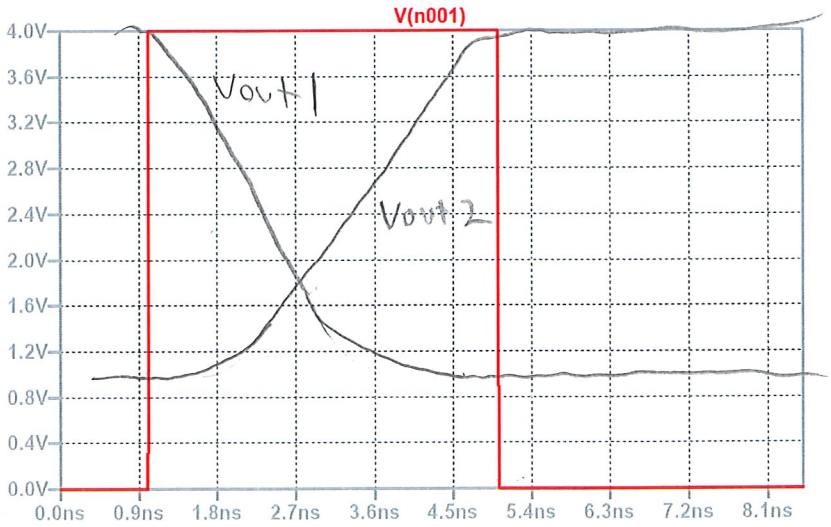
Ans = 1.5 ns

a) Low to high delay:

Ans = 1.5 ns

Q4. For the Vin waveform given, draw waveforms of V(out1) and V(out2). Assume that the pulse high and low times are long enough for charging or discharging to complete. Vdd=4V. VTO=1 and -0.5 V for NMOS and PMOS, respectively **(12)**.

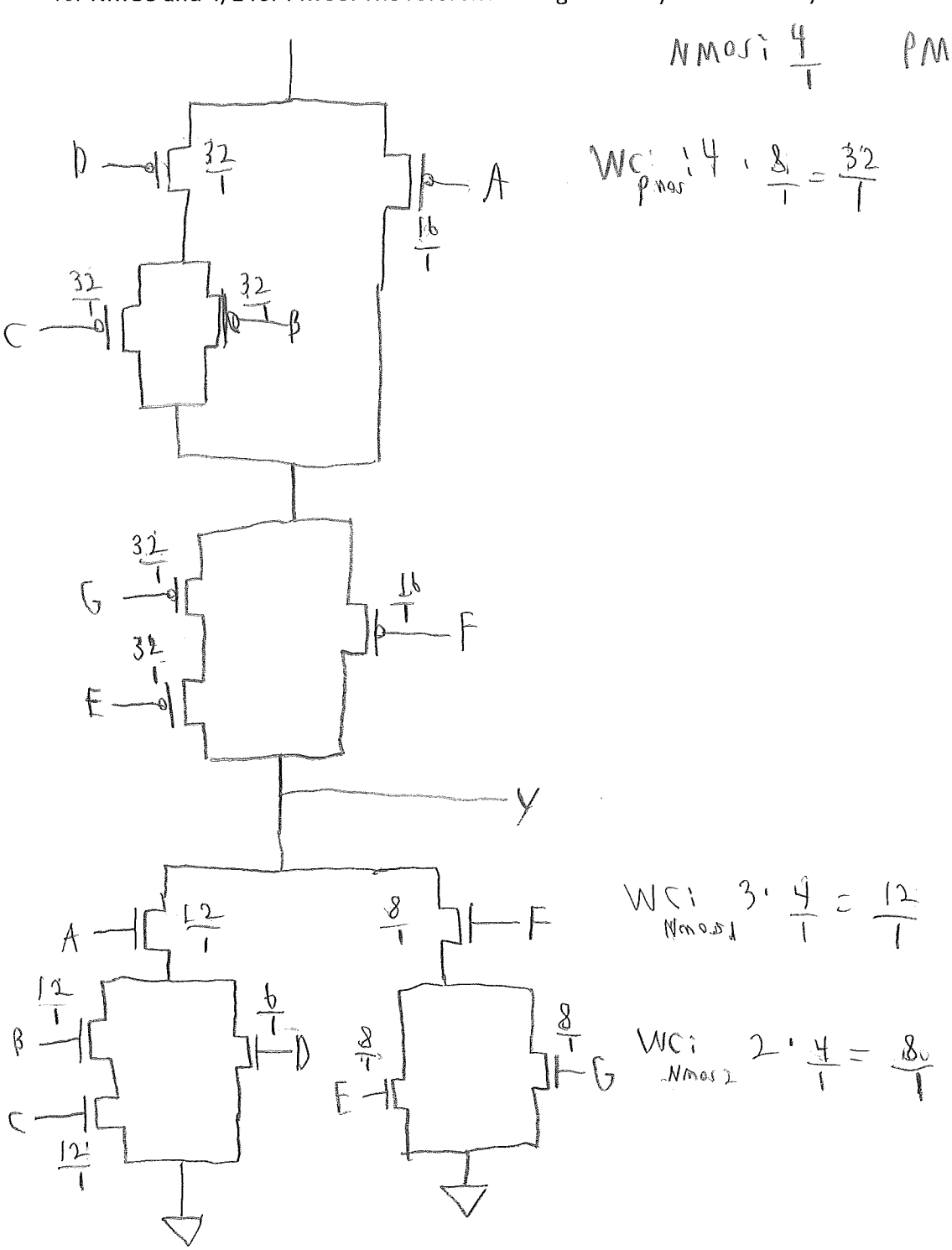




Q5. (20).
Design a CMOS complex logic gate for

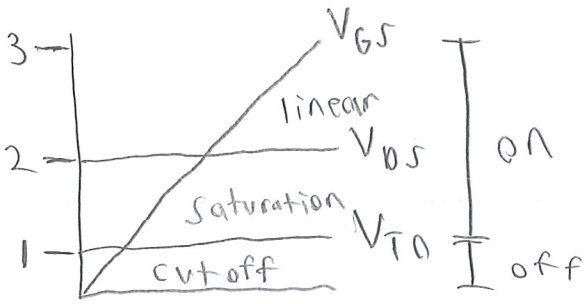
$y = \overline{A(BC + D) + F(G + E)}$

The worst case speed needs to be twice the speed of the reference CMOS inverter, where (W/L) is 2/1 for NMOS and 4/1 for PMOS. The reference design has a symmetric delay of 1ns.

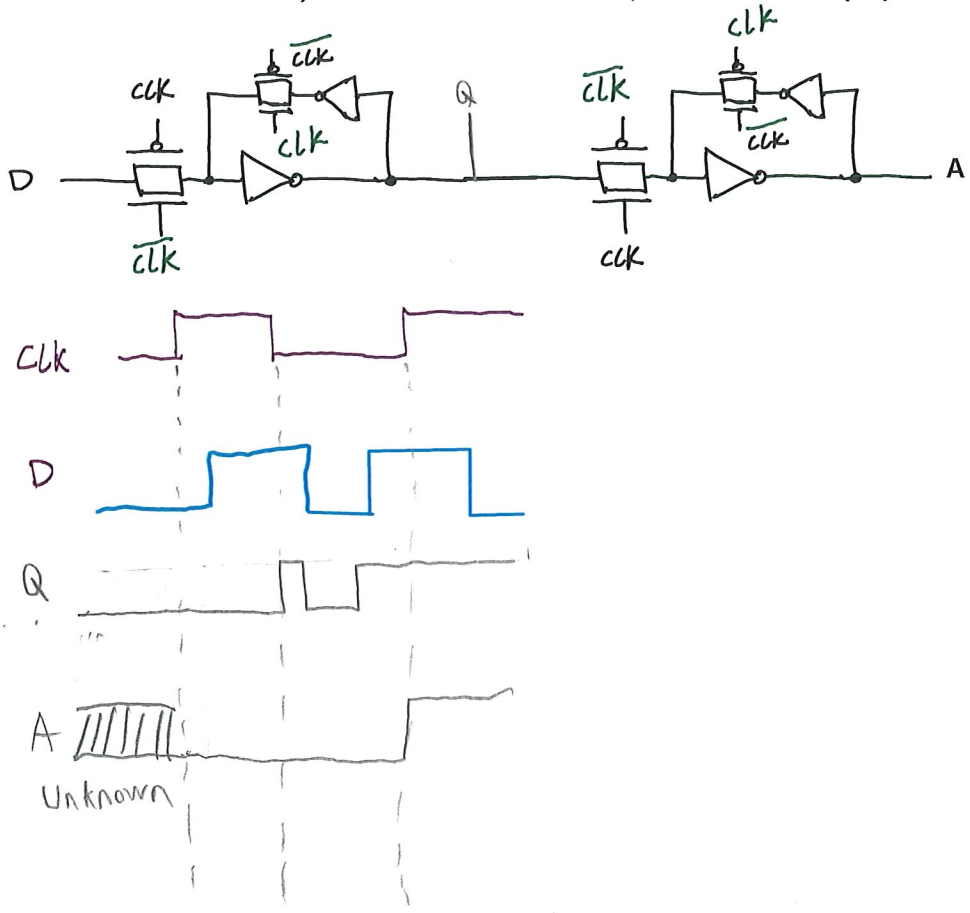


Q6. Sketch qualitatively $I_{DS} - V_{GS}$ at $V_{DS} = 2\ V$ for a NMOS transistor, VTO=1V. V_{GS} range is from 0V to 3V. **(10)**

1. Clearly label ON and OFF regions, for ON region, clearly label linear and saturation regions.
2. Write down the numerical values of V_{GS} at the transition points between regions.

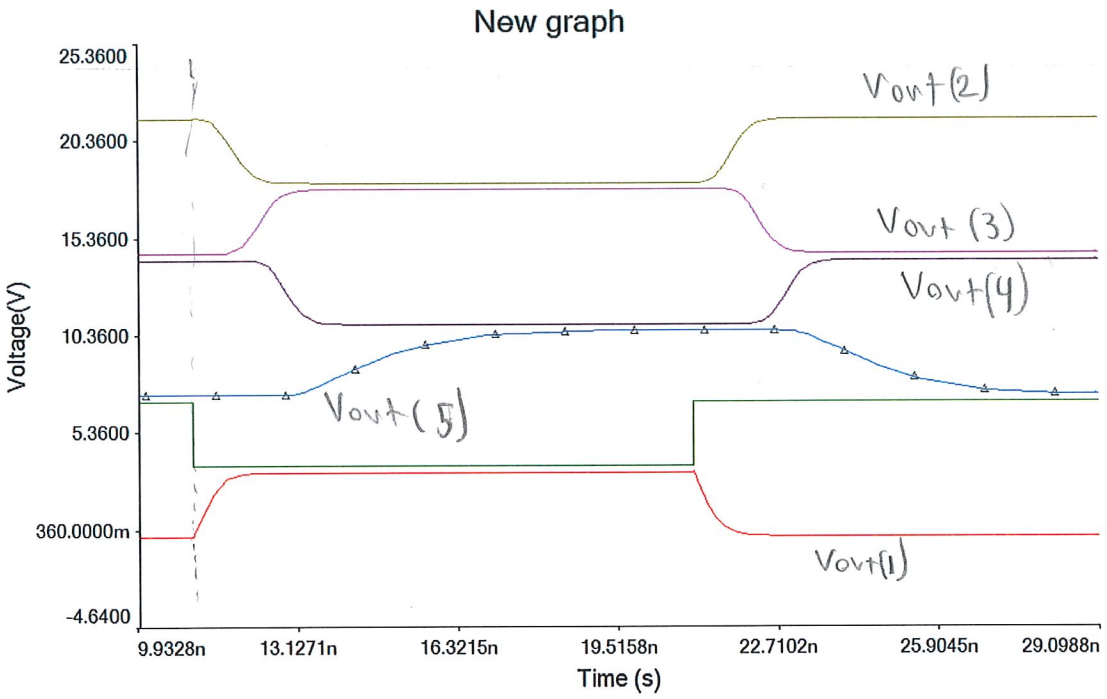


Q7. Draw waveform for **A,** if initial value is unknown, write unknown **(10)**



Q7. Below are waveforms of input and **outputs** of a chain of 5 CMOS inverters, vertically separated. All inverter are identical in transistor size.

1. Label Vout(1), Vout(2), Vout(3), Vout(4), Vout(5) on the curves **(3)**
2. Which inverter (1st, 2nd ...?) has the largest load capacitance? **(2)**



Vout(5) largest
C

Q8. Maximum speed of a CMOS inverter is 1GHz when VDD=1.2V, VTN=-VTP=0.2V, calculate the VDD you would need for 500MHz maximum speed, with everything being the same **(5)**.

$T_{min} = 5\,T_p$

$f_{max} = 1/T_{min}$

$R_{on} = \frac{1}{\frac{W}{L}k(x)}$

$500 = \frac{1}{5x}$ $\quad x = \frac{1}{2.5k}$

$R_{on} = \frac{1}{2}$

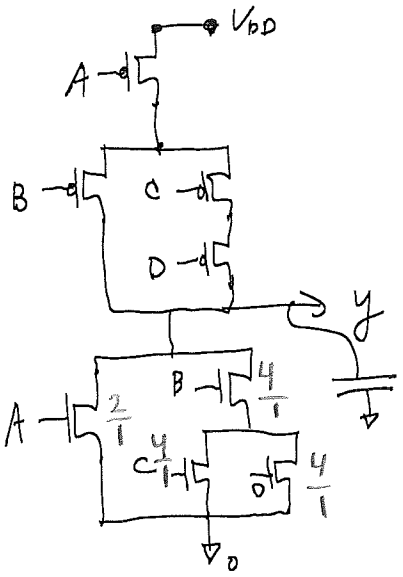
$1000 = \frac{1}{5x}$ $\quad x = \frac{1}{5k}$

$\frac{1}{2} = \frac{1}{x}$ $\quad x = 2$

$x - .2 = 2$

$V_{DD} = 2.2\,V$

Q9. (10) For the complex logic gate shown,



WC: $2 \cdot \frac{2}{1} = \frac{4}{1}$

1) Write y as a function of A, B, C, D.

Ans = $A + B(C+D)$

2) Assume W/L = 2/1 for all NMOS, 5/1 for all PMOS, which input switching combination below leads to shortest low to high delay?
   - ☑ A, B, C, D all switching from high to low, all else at high
   - ☐ A, C, D all switching from high to low, all else at high
   - ☐ A, B switching from high to low, all else at high
   - ☐ B, C switching from low to high, all else at low
3) Find the effective W/L of the NMOS network when all inputs switch together.

Ans= $\frac{4.66}{1}$

Q10 (10). Design a symmetric CMOS inverter that can drive a 0.5pF load with a maximum speed of 200 MHz in a digital system. VTO (NMOS)=0.5V. VTO(PMOS)=-0.5V. KP(NMOS)=200 μA/V². KP(PMOS)=80μA/V². VDD=3.3V. Minimum feature size is 0.35 μm. W, L values for both NMOS and PMOS need to be calculated.

$\tau_p = 2.4 R_{on} C \qquad f_{max} = \frac{1}{T_{min}} \qquad T_{min} = 5\tau_p \qquad f_{max} = \frac{1}{5\tau_p}$

$200\,MHz = \frac{1}{5 \cdot \tau_p} \qquad \tau_p = 1ns$

$1ns = 2.4 R_{on} .5pF \qquad R_{on} = 833.33\Omega$

$R_{on} = \frac{1}{(kp)(\frac{W}{L})(V_{GT})} \qquad V_{GT} = V_{GS} - V_{TH}$

$3.3 - .5 = 2.8 = V_{GT}$

$833.33 = \frac{1}{(200 \cdot 10^{-6})(\frac{W}{L})(2.8)} \qquad \frac{W}{L}_{NMOS} = \frac{2.14}{1} \qquad \frac{2.14}{1} = \frac{x}{.35} \quad x = .749$

$\frac{W}{L_{pmos}} = \frac{kp_{nmos}}{kp_{pmos}} \cdot \frac{W}{L_{nmos}} \qquad \frac{200}{80} \cdot \frac{2.14}{1} = \frac{5.35}{1} = \frac{W}{L_{pmos}} \qquad \frac{5.35}{1} = \frac{x}{.35} \quad x = 1.8725$

$\frac{W}{L_{NMOS}} = \frac{.749\,\mu m}{.35\,\mu m} \qquad \frac{W}{L_{pmos}} = \frac{1.8725\,\mu m}{.35\,\mu m}$