Homework 7

Jacob Howard

Start of code

Freescale HC12-Assembler


```
 Abs. Rel.   Loc    Obj. code   Source line
 ---- ----   ------ ---------   -----------
   1    1              ;*****************************************************************
   2    2              ;* This stationery serves as the framework for a                 *
   3    3              ;* user application (single file, absolute assembly application) *
   4    4              ;* For a more comprehensive program that                         *
   5    5              ;* demonstrates the more advanced functionality of this          *
   6    6              ;* processor, please see the demonstration applications          *
   7    7              ;* located in the examples subdirectory of the                   *
   8    8              ;* Freescale CodeWarrior for the HC12 Program directory          *
   9    9              ;*****************************************************************
  10   10
  11   11                ; export symbols
  12   12                      XDEF Entry, _Startup            ; export 'Entry' symbol
  13   13                      ABSENTRY Entry        ; for absolute assembly: mark this as application entry
point
  14   14
  15   15
  16   16
  17   17                ; Include derivative-specific definitions
  18   18
  19   19        0000 0800   RAMStart    EQU  $0800
```

```
20  20        0000 4000   ROMStart    EQU  $4000  ; absolute address to place my code/constant data
21  21        0000 2000   Stack       EQU  $2000
22  22        0000 0000   PORTA       EQU  $0000
23  23        0000 0002   DDRA        EQU  $0002
24  24
25  25                    ; variable/data section
26  26
27  27                          ORG RAMStart
28  28
29  29  a000800 08         TABLE       DC.B  $08
30  30  a000801 01         DIRECTION   DC.B  1
31  31  a000802 0100        BOUNCE      DC.B  1,0
32  32
33  33  a000804           COUNTER     DS.W  1
34  34  a000806           X_COUNTER   DS.W  1
35  35
36  36
37  37
38  38                          ORG   ROMStart
39  39
40  40                    Entry:
41  41                    _Startup:
42  42
43  43                    inf_loop:
44  44  a004000 CF20 00       lds    #Stack
45  45  a004003 180B 0108     movb   #1, DIRECTION
        004007 01
46  46  a004008 180B 0808     movb   #08, TABLE
        00400C 00
```

```
47  47  a00400D CE00 14       ldx   #$14
48  48  a004010 CD08 02       ldy   #BOUNCE
49  49  a004013 180B FF00     movb  #$FF, DDRA
        004017 02
50  50
51  51                  loop:
52  52  a004018 1640 33       jsr   update_table
53  53
54  54  a00401B 180C 0800     movb  TABLE, PORTA
        00401F 0000
55  55
56  56  a004021 7E08 04       stx   COUNTER
57  57
58  58  a004024 1640 66       jsr   delay
59  59
60  60  a004027 FE08 04       ldx   COUNTER
```

Freescale HC12-Assembler


```
 Abs. Rel.   Loc    Obj. code   Source line
 ---- ----   ------ ---------   -----------
   61   61
   62   62  a00402A 09           dex
   63   63  a00402B 8E00 00       cpx    #0
   64   64  a00402E 2EE8          bgt    loop
   65   65
   66   66  a004030 20CE          bra    inf_loop
   67   67
   68   68  a004032 3D           rts
   69   69
   70   70                  update_table:
   71   71  a004033 F708 00       tst    TABLE
   72   72  a004036 2723          beq    reset
   73   73
   74   74  a004038 F708 01       tst    DIRECTION
   75   75  a00403B 2711          beq    shift_left
   76   76
   77   77  a00403D 7408 00       lsr    TABLE
   78   78  a004040 1F08 0001     brclr  TABLE, #$01, done
          004044 20
   79   79
   80   80  a004045 A670          ldaa   1, y+
   81   81  a004047 271C          beq    done
   82   82
```

```
 83  83  a004049 7908 01       clr    DIRECTION
 84  84  a00404C 2017         bra    done
 85  85
 86  86                  shift_left:
 87  87  a00404E 7808 00       lsl    TABLE
 88  88  a004051 1F08 0080     brclr  TABLE, $80, done
        004055 0F
 89  89
 90  90  a004056 7208 01       inc    DIRECTION
 91  91  a004059 200A         bra    done
 92  92
 93  93                  reset:
 94  94  a00405B 8601         ldaa   #$01
 95  95  a00405D 7A08 00       staa   TABLE
 96  96  a004060 7908 01       clr    DIRECTION
 97  97  a004063 2000         bra    done
 98  98
 99  99                  done:
100  100  a004065 3D          rts
101  101
102  102
103  103                   delay:
104  104  a004066 CE01 00      ldx    #$100
105  105
106  106                   out_loop:
107  107  a004069 7E08 06      stx    X_COUNTER
108  108
109  109  a00406C CE0F FF      ldx    #$0FFF
110  110
```

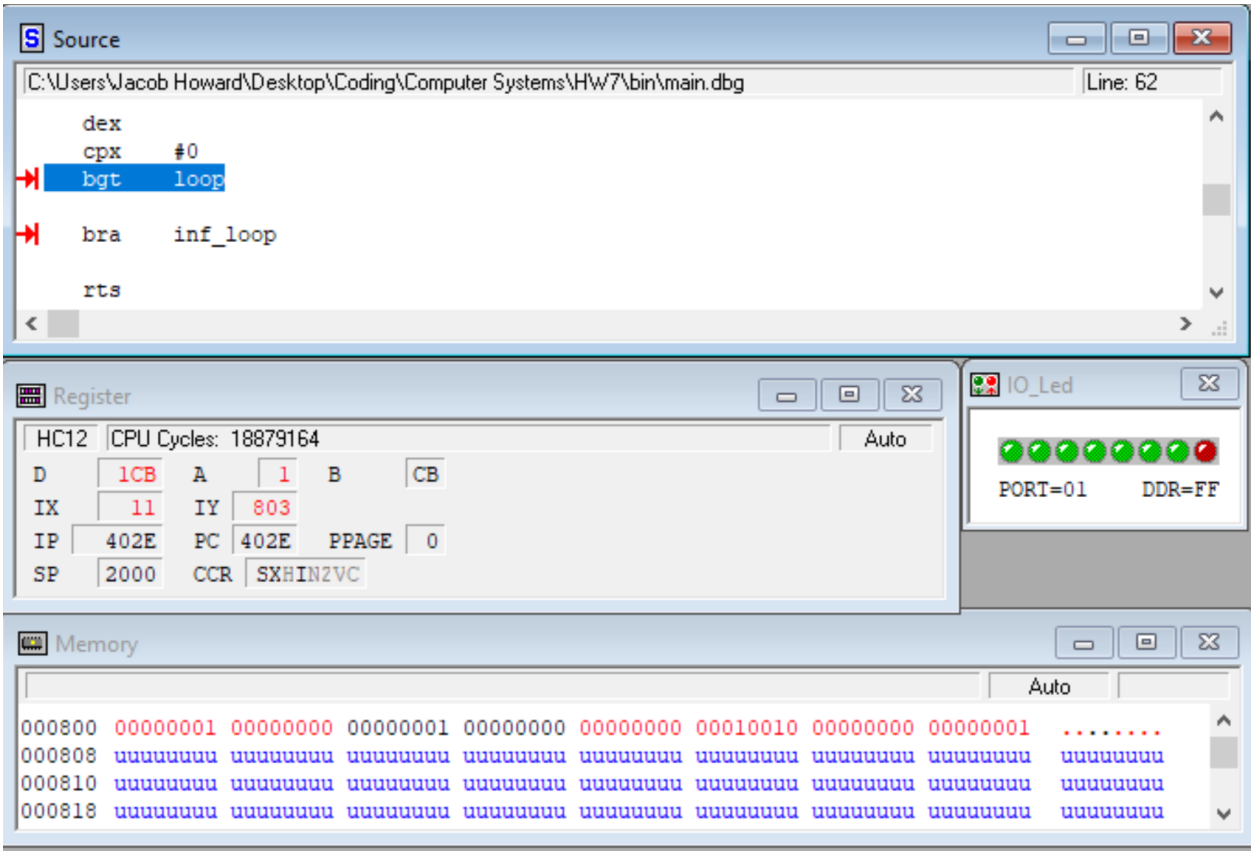
```
111  111                 in_loop:
112  112  a00406F 09          dex
113  113  a004070 8E00 00       cpx    #0
114  114  a004073 2EFA         bgt    in_loop
115  115
116  116  a004075 FE08 06       ldx    X_COUNTER
117  117  a004078 09          dex
118  118  a004079 8E00 00       cpx    #0
119  119  a00407C 2EEB         bgt    out_loop
120  120
121  121  a00407E 3D          rts
122  122
```

Freescale HC12-Assembler

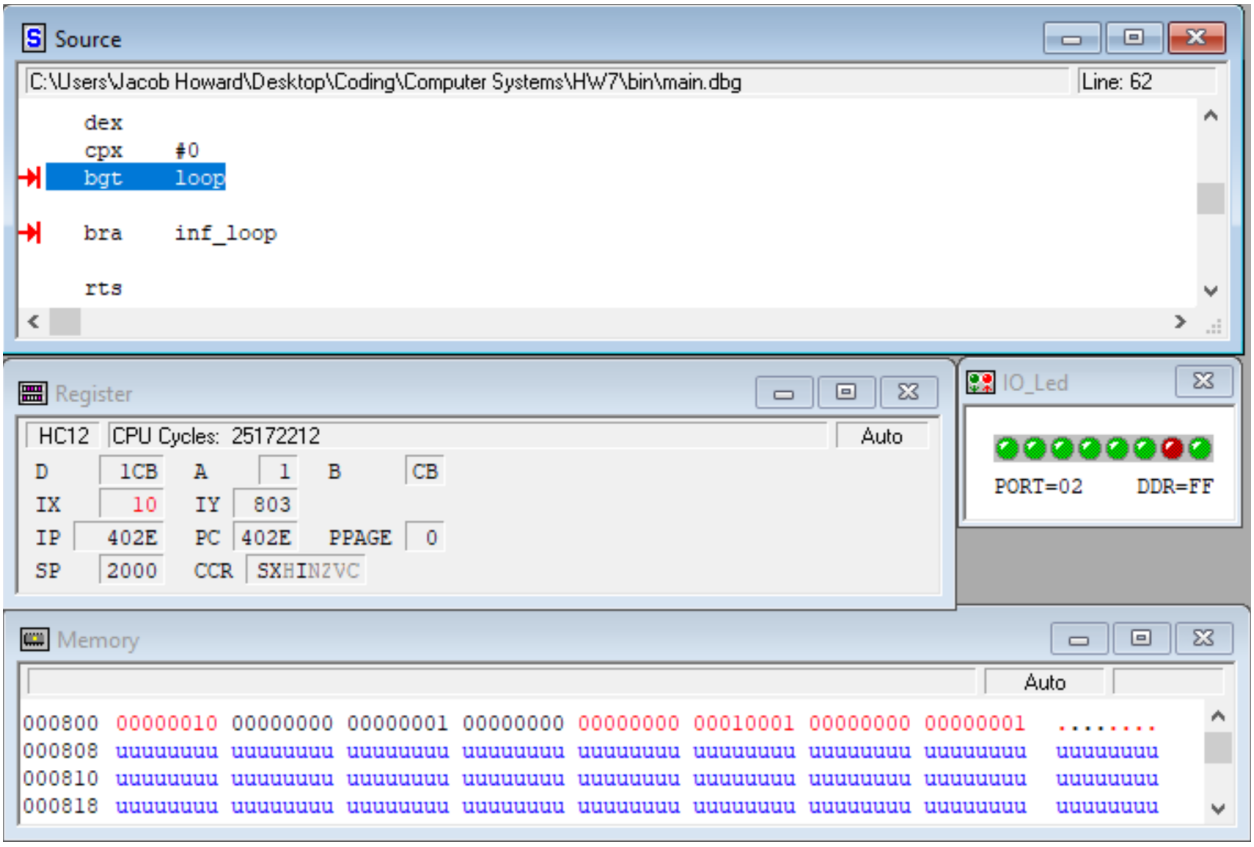

```
 Abs. Rel.   Loc    Obj. code   Source line
 ---- ----   ------ ---------   -----------
  123  123
  124  124
  125  125
  126  126                              ; result in D
  127  127
  128  128                ;*************************************************************
  129  129                ;*             Interrupt Vectors                     *
  130  130                ;*************************************************************
  131  131                          ORG   $FFFE
  132  132  a00FFFE 4000               DC.W  Entry         ; Reset Vector
```

End of code

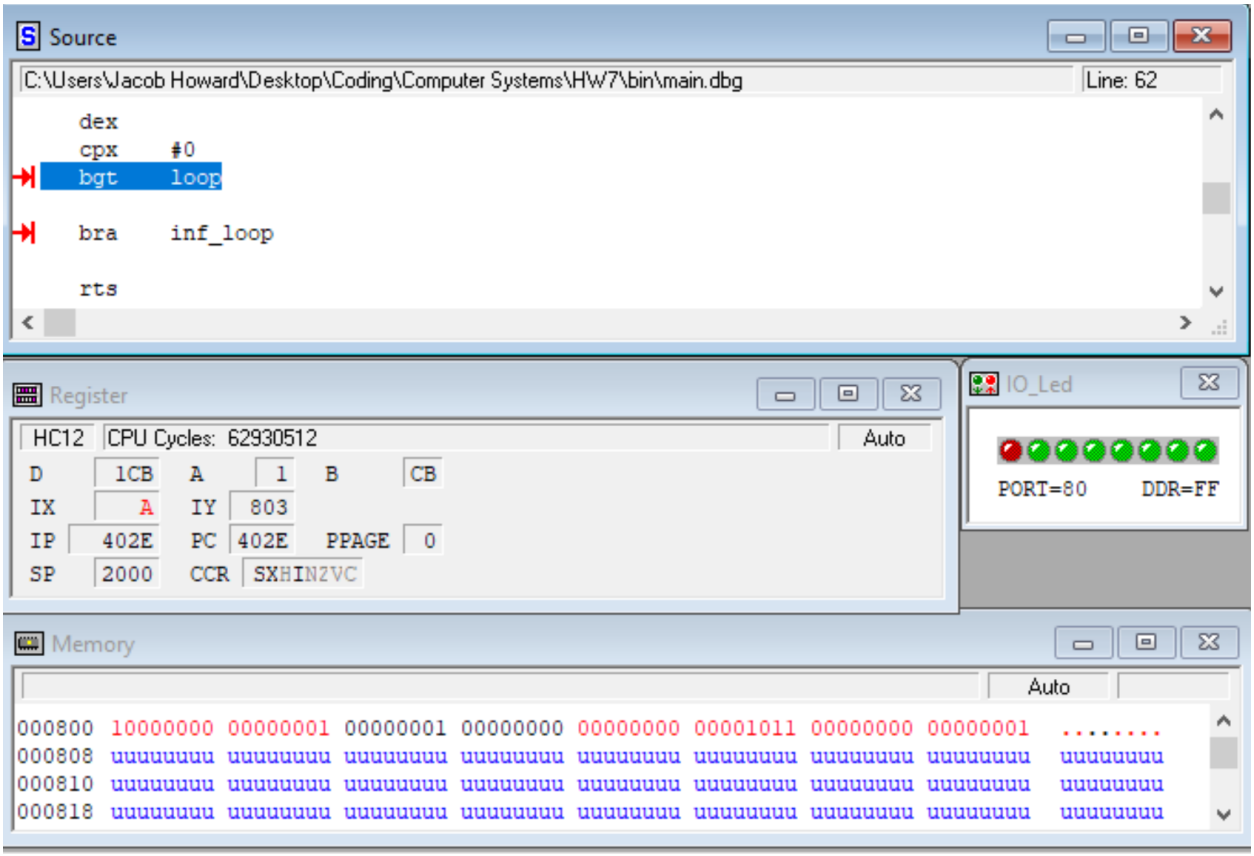
Step 3


Source
C:\Users\Jacob Howard\Desktop\Coding\Computer Systems\HW7\bin\main.dbg
Line: 62
dex
cpx #0
bgt loop
bra inf_loop
rts
Register
HC12
CPU Cycles: 18879164
Auto
D 1CB A 1 B CB
IX 11 IY 803
IP 402E PC 402E PPAGE 0
SP 2000 CCR SXHIN2VC
IO_Led
PORT=01 DDR=FF
Memory
Auto
000800 00000001 00000000 00000001 00000000 00000000 00010010 00000000 00000001 ....
000808 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000810 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000818 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu

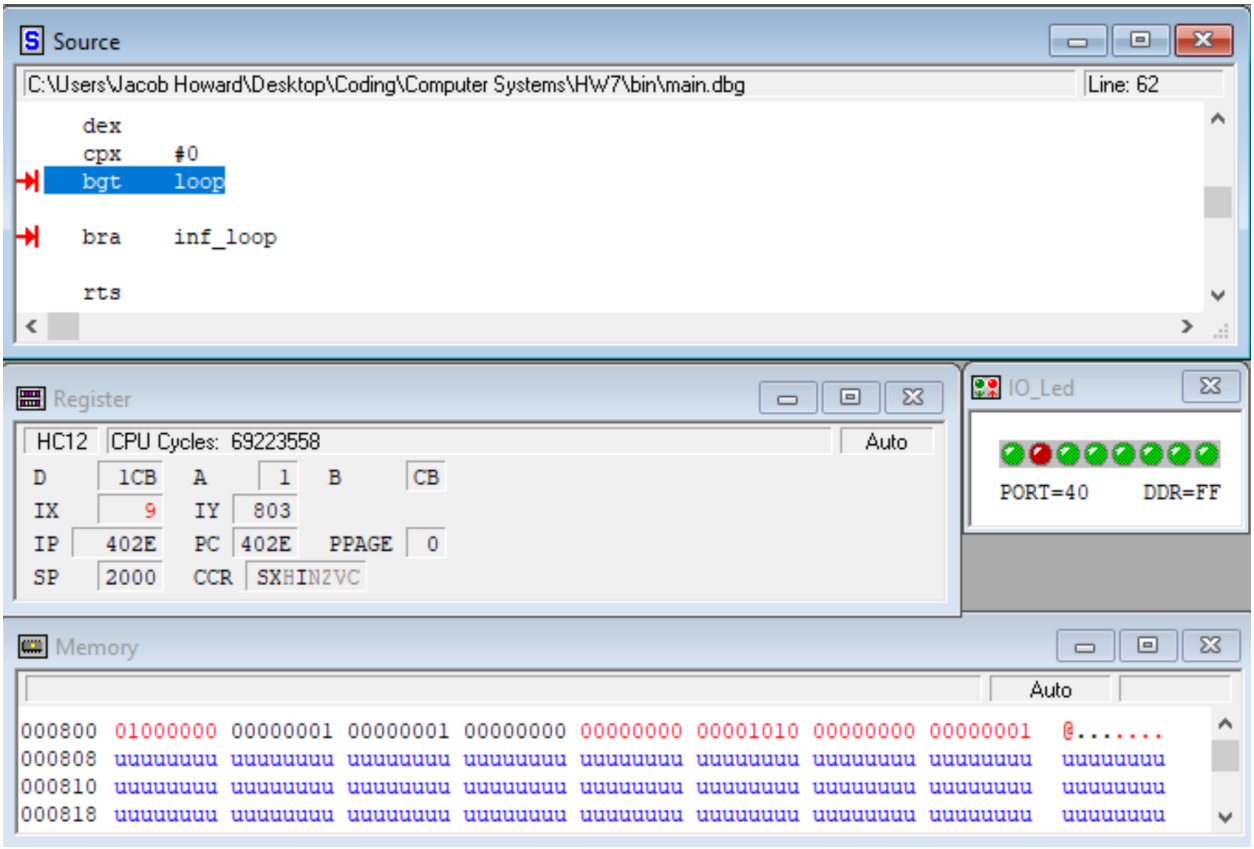
Step 4


Source
C:\Users\Jacob Howard\Desktop\Coding\Computer Systems\HW7\bin\main.dbg
Line: 62
dex
cpx #0
bgt loop
bra inf_loop
rts
Register
HC12
CPU Cycles: 25172212
Auto
D 1CB A 1 B CB
IX 10 IY 803
IP 402E PC 402E PPAGE 0
SP 2000 CCR SXHINZVC
IO_Led
PORT=02 DDR=FF
Memory
Auto
000800 00000010 00000000 00000001 00000000 00000000 00010001 00000000 00000001 ....
000808 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000810 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000818 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu

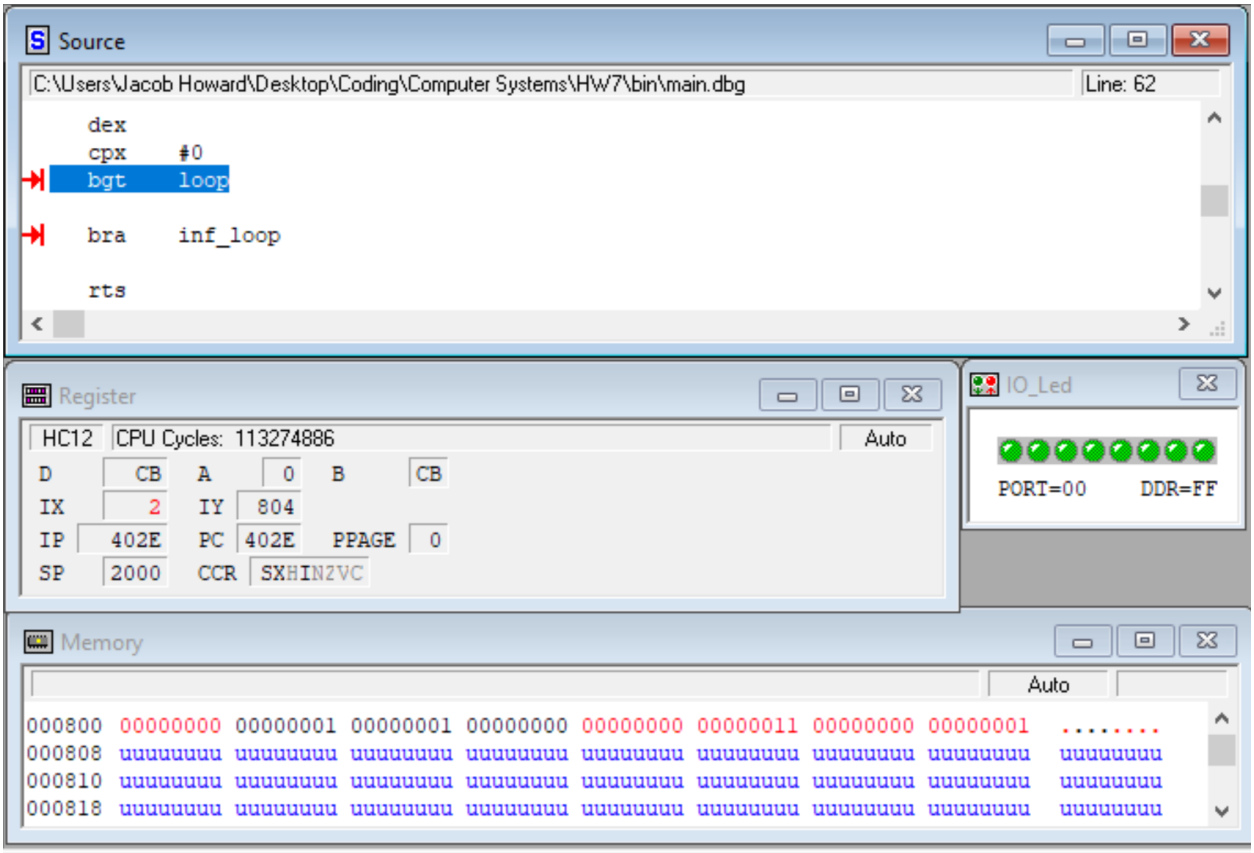
Step 10


Source
C:\Users\Jacob Howard\Desktop\Coding\Computer Systems\HW7\bin\main.dbg
Line: 62
dex
cpx #0
bgt loop
bra inf_loop
rts
Register
HC12
CPU Cycles: 62930512
Auto
D 1CB A 1 B CB
IX A IY 803
IP 402E PC 402E PPAGE 0
SP 2000 CCR SXHINZVC
IO_Led
PORT=80 DDR=FF
Memory
Auto
000800 10000000 00000001 00000001 00000000 00000000 00001011 00000000 00000001 ....
000808 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000810 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000818 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu

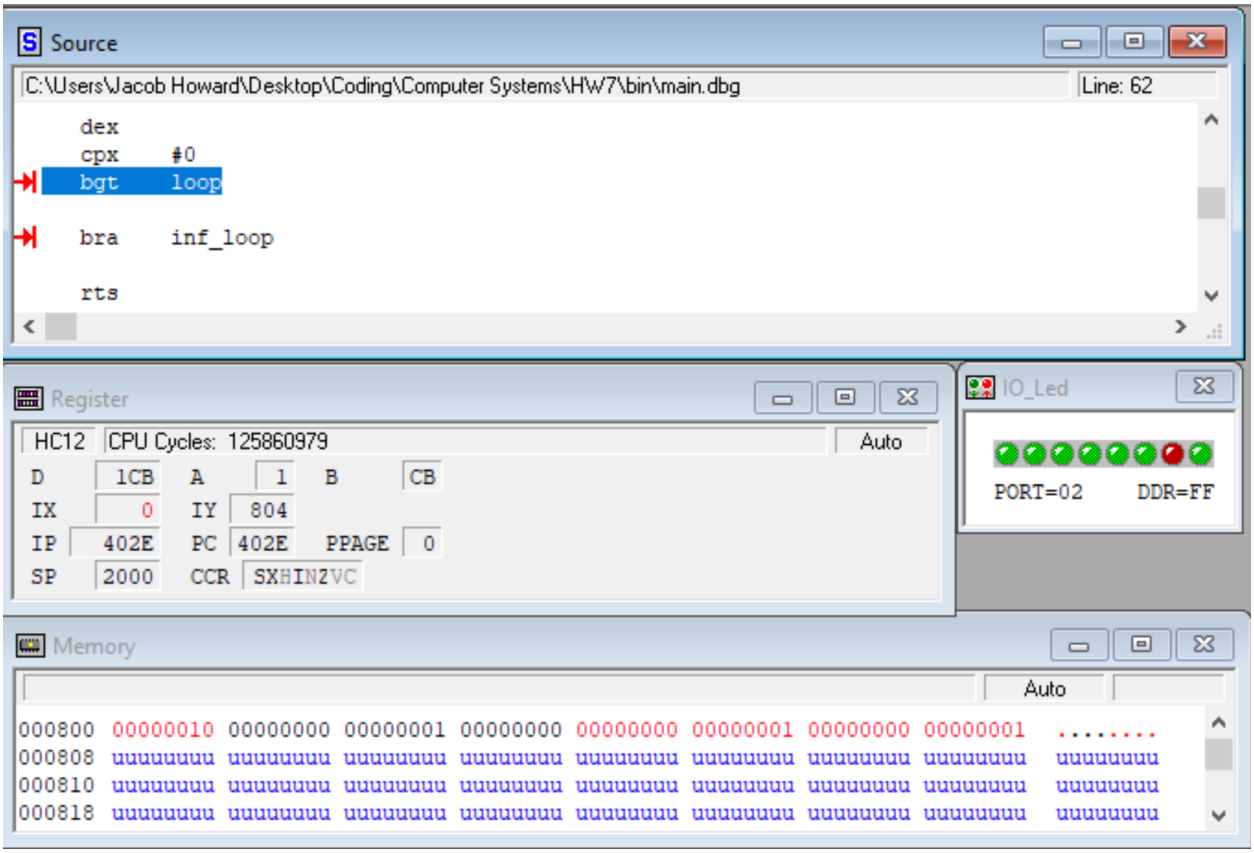
Step 11


Source
C:\Users\Jacob Howard\Desktop\Coding\Computer Systems\HW7\bin\main.dbg
Line: 62
dex
cpx #0
bgt loop
bra inf_loop
rts
Register
HC12
CPU Cycles: 69223558
Auto
D 1CB A 1 B CB
IX 9 IY 803
IP 402E PC 402E PPAGE 0
SP 2000 CCR SXHINZVC
IO_Led
PORT=40 DDR=FF
Memory
Auto
000800 01000000 00000001 00000001 00000000 00000000 00001010 00000000 00000001 @.......
000808 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000810 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000818 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu

Step 18


Source
C:\Users\Jacob Howard\Desktop\Coding\Computer Systems\HW7\bin\main.dbg
Line: 62
dex
cpx #0
bgt loop
bra inf_loop
rts
Register
HC12
CPU Cycles: 113274886
Auto
D CB A 0 B CB
IX 2 IY 804
IP 402E PC 402E PPAGE 0
SP 2000 CCR SXHINZVC
IO_Led
PORT=00 DDR=FF
Memory
Auto
000800 00000000 00000001 00000001 00000000 00000000 00000011 00000000 00000001 ....
000808 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000810 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000818 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu

Step 20


Source
C:\Users\Jacob Howard\Desktop\Coding\Computer Systems\HW7\bin\main.dbg
Line: 62
dex
cpx #0
bgt loop
bra inf_loop
rts
Register
HC12
CPU Cycles: 125860979
Auto
D 1CB A 1 B CB
IX 0 IY 804
IP 402E PC 402E PPAGE 0
SP 2000 CCR SXHINZVC
IO_Led
PORT=02 DDR=FF
Memory
Auto
000800 00000010 00000000 00000001 00000000 00000000 00000001 00000000 00000001 ....
000808 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000810 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu
000818 uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu uuuuuuuu