

Elec 2210 Test 1 Spring 2017

Monday, February 6, 2017 2:07 PM

85

+5

Name: _____

Please spread out, and leave one or more empty seats between you and your neighbor.

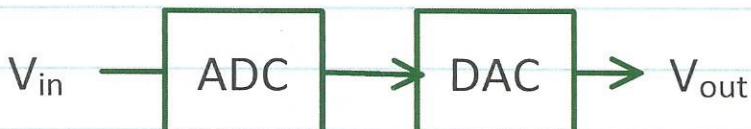
Wullot

Write your name on equation sheet, and turn it in together with your exam paper.

Digital Data (20)

Wednesday, June 13, 2012 11:58 AM

In the system below, $n = 3$, $V_{FS} = 8V$. Determine the interval of V_{in} that gives the same V_{out} as $V_{in} = 5.4V$, but satisfies $V_{in} > V_{out}$. (10)



$$n = 3$$

$$V_{FS} = 8V$$

$$V_{LSB} = \frac{8}{2^3} = 1V$$

$$V_{in} = \text{round}\left(\frac{V_{in}}{V_{LSB}}\right) = 5V \pm \frac{V_{LSB}}{2}$$

$$= 5 \pm 0.5V$$

$$= 4.5 \sim 5.5V$$

$$4.5V < V_{in} < 5.5V$$

(-3)

$$5V \rightarrow 5.5V$$

Find out the number of seconds it takes to download 1 binary Tera Byte (TB) data using a 100 GBPS (giga bits per second) connection. (10)

$$1 \text{ bin TB} \left| \begin{array}{c} 2^{40} \text{ B} \\ \hline 1 \text{ bin TB} \end{array} \right| \begin{array}{c} 8 \text{ bits} \\ \hline 1 \text{ B} \end{array} \left| \begin{array}{c} 1 \text{ Gb} \\ \hline 10^9 \text{ bits} \end{array} \right. = 8796.09 \text{ Gb}$$

$$\frac{8796.09 \text{ Gb}}{100 \text{ Gb ps}} = \boxed{87.961 \text{ s}}$$

PN Junction/Diodes (15 + 5 point bonus)

Sunday, June 8, 2014 5:38 PM

Consider a PN junction with $N_d = 10^{17}/cm^3$ and $N_a = 10^{19}/cm^3$. Which of the following are true? (5)

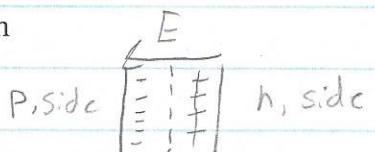
1) Electrons drift from n-side to p-side.

False.

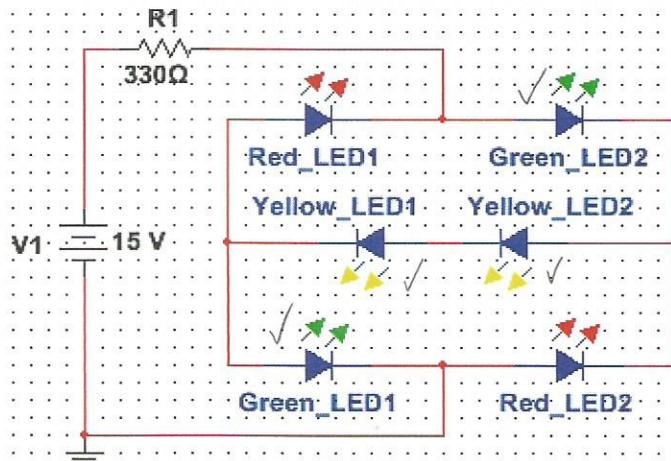
2) $x_p/x_n = 100$.

$$\frac{N_A}{N_D} = \frac{10^{19}}{10^{17}} = 100$$

True.



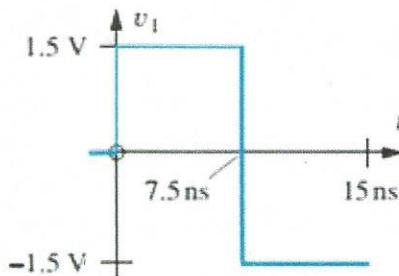
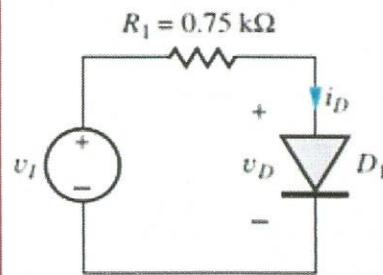
X -2.5



Turn on voltage is 2V. Which LEDs are lighting up and which LEDs are not? (5)

Green_LED2, Green_LED1, Yellow_LED1, Yellow_LED2 lighting up.

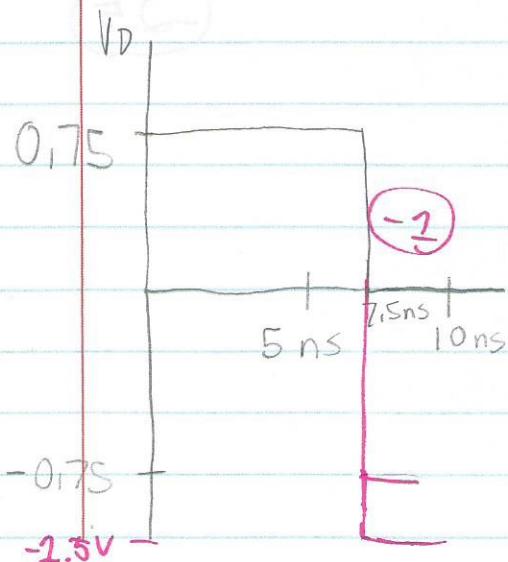
Red_LED1, Red_LED2 not lighting up.



Assuming $V_{on}=0.75V$, sketch v_D for the v_I assuming instantaneous turn-on and turn-off.

Explicitly state the v_D values at $t=5ns$ and $10ns$ (5).

Figure 3.67 Circuit used to explore diode-switching behavior.

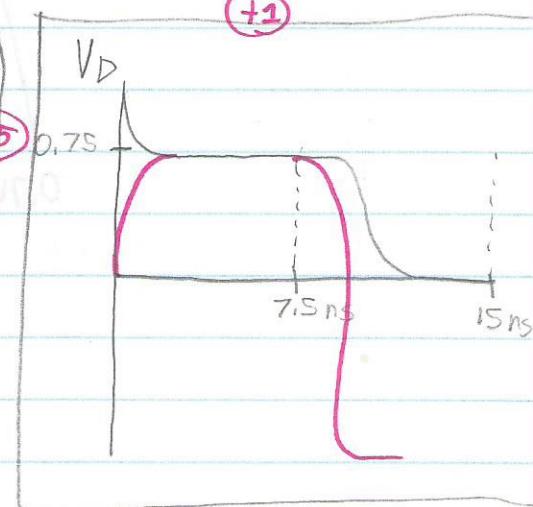


$$V_D(5\text{ns}) = 0.75 \text{ V}$$

$$V_D(10\text{ns}) = 0 \text{ V}$$

X -15

$$I = \frac{0.75}{0.75k} = 1 \text{ mA}$$



Redraw v_D by considering finite turn-on and turn-off (5 bonus)

Bipolar circuit (20)

Sunday, June 9, 2013 12:25 PM

1. $\beta_F = 100$. $V_{BE,ON} = 0.7V$, $V_{ce,sat} = 0.2V$. For the circuit below,
 - What is the transistor's operation mode when $V_{in}=0V$?
 - At what V_{in} will the transistor enter forward operation mode?
 - At what V_{in} will the transistor enter saturation mode?
 - Sketch I_C versus V_{in} as V_{in} increases from 0 to 5V. Label numerical values of I_C , V_{in} at critical points on the curve.

5V

a) $V_{in} < V_{BE,ON}$, CUTOFF Mode

b) $V_{in} \geq 0.7V$

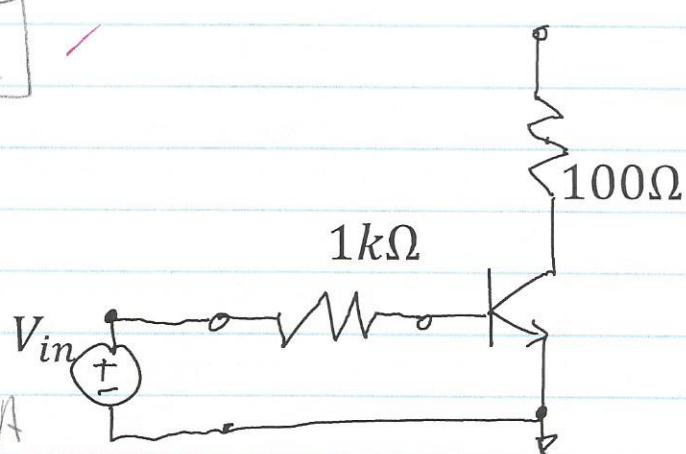
$$c) \frac{5 - 0.2}{100} = 48 \text{ mA} = I_{C, MAX}$$

$$I_C / \beta_F = I_B = \frac{48 \text{ mA}}{100} = 0.48 \text{ mA}$$

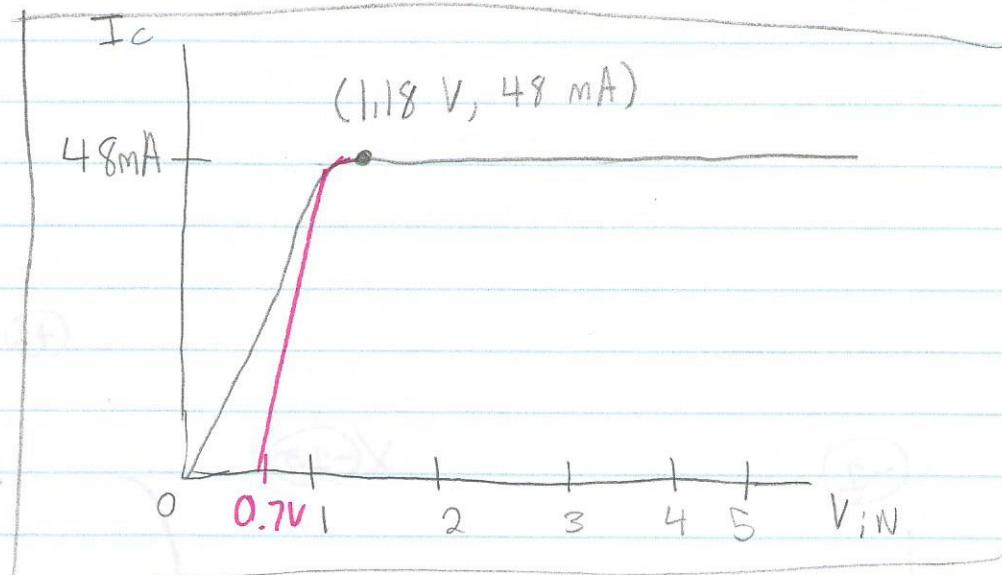
$$V_{in} = I_B R + V_{BE,ON}$$

$$V_{in} = (0.48 \text{ mA})(1 \text{ k}\Omega) + 0.7 = 0.48 \text{ V} + 0.7 \text{ V}$$

$$V_{in} = 1.18 \text{ V}$$



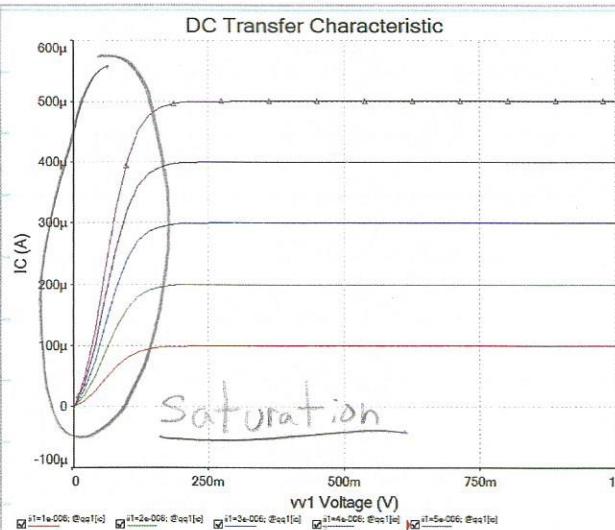
d)



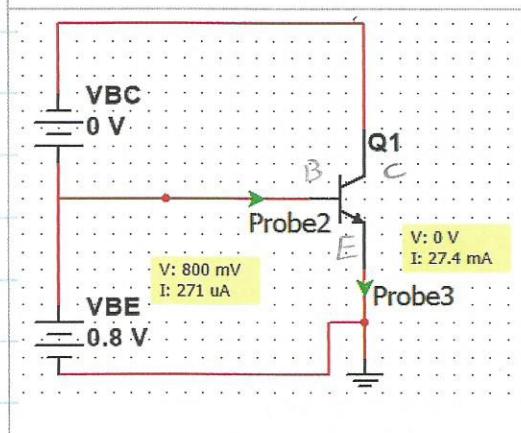
Bipolar transistor I-V (5)

Sunday, June 9, 2013 12:25 PM

1. Complete the problem below.



On the IC-VCE plot, circle portions of the curves where transistor works in saturation region.



Find β_F

$$I_B = 0.271 \text{ mA}$$

$$I_E = 27.4 \text{ mA} = I_B + I_C$$

$$I_C = I_E - I_B = 27.129 \text{ mA}$$

$$\beta_F = I_C / I_B = 27.129 \text{ mA} / 0.271 \text{ mA}$$

$\beta_F \approx 100$

Solid-State (20)

Sunday, June 9, 2013 11:08 AM

N_D N_A
What are the n and p in a Si sample with $5 \times 10^{16}/cm^3$ phosphorous and $1 \times 10^{16}/cm^3$ boron?

With additional $8 \times 10^{16}/cm^3$ boron? $n_i = \frac{10^{10}}{cm^3}$

$N_D > N_A \rightarrow n\text{-type}$

$$n = N_D - N_A = 5 \times 10^{16} - 1 \times 10^{16} = 4 \times 10^{16}/cm^3$$

$$p = n_i^2/n = \frac{10^{20}}{4 \times 10^{16}} = 2500$$

$$n = 4 \times 10^{16}/cm^3$$

$$p = 2500/cm^3$$

$| + 8 \times 10^{16} = 9 \times 10^{16}, N_A > N_D \rightarrow p\text{-type}$

$$p = N_A - N_D = 9 \times 10^{16} - 5 \times 10^{16} = 4 \times 10^{16}/cm^3$$

$$n = \frac{(10^{10})^2}{4 \times 10^{16}} = 2500/cm^3$$

$$p = 4 \times 10^{16}/cm^3$$

$$n = 2500/cm^3$$

Consider a 10nm long resistor, $\mu = 200 \frac{cm^2}{V \cdot s}$. $v_{sat} = 10^7 cm/s$. Find out the highest voltage we can apply without breaking Ohm's law.

$$V_{SAT} = \mu \frac{V}{l}$$

$$V = \frac{V_{SAT} l}{\mu}$$

$$l = 10 \times 10^{-7} cm$$

$$\mu = 200 \frac{cm^2}{V \cdot s}$$

$$V_{SAT} = 10^7 cm/s$$

$$V = \frac{(10^7 cm/s)(10 \times 10^{-7} cm)}{(200 \frac{cm^2}{V \cdot s})} = 0.05 V$$

$$V_{MAX} = 0.05 V$$

Rectifiers (20)

Wednesday, June 13, 2012 11:46 AM

Design a 5V, 1A full wave bridge rectifier with a V_r no more than 50 mV. $V_{on} = 1V$. Frequency of ac source is 60Hz. $V_{in} = V_p \sin(\omega t)$. $\omega = 2\pi f$.

a) For the V_{in} below,

a. Sketch V_{out} (5) -1

b. On your V_{out} drawing, indicate the time intervals during which D_2 is on? (5) -2.5

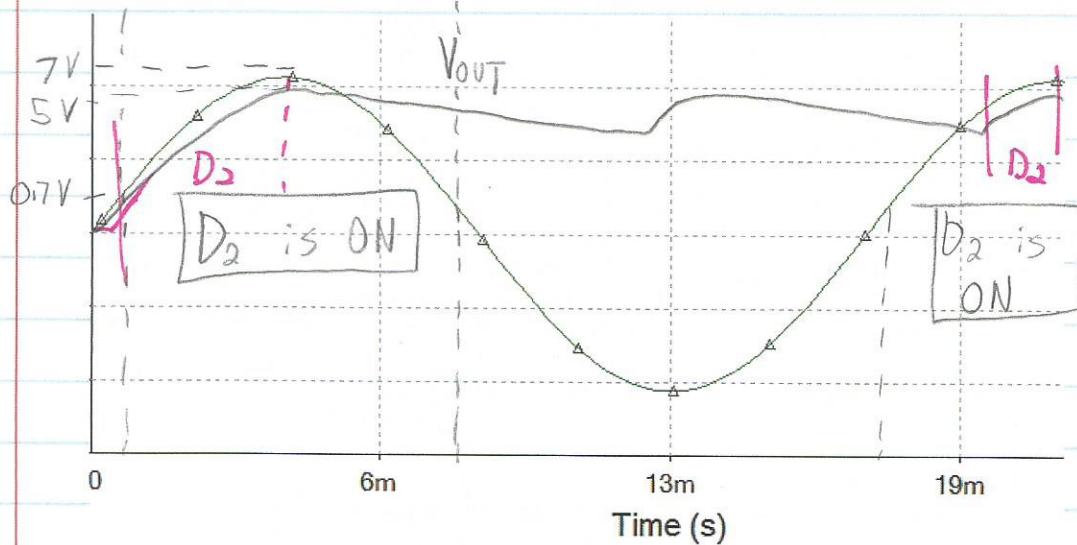
b) At 6ms, which diodes are off? (5)

D_1 and D_4 .

all are off -0.5

c) Find V_p (5).

$$V_p = 7V$$



$$V_{DC} = 5V$$

$$I_{DC} = 1A$$

$$V_r = 0.05V$$

$$V_{on} = 1V$$

$$f = 60 \text{ Hz}$$

$$V_{in} = V_p \sin(\omega t)$$

$$\omega = 2\pi f$$

$$V_p = V_{DC} + 2V_{on} = 5 + 2(1) = \underline{\underline{7V}}$$

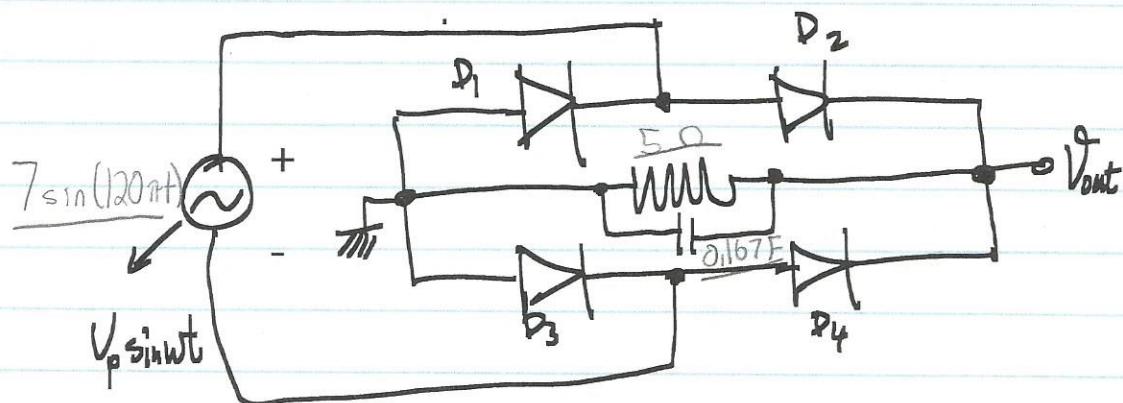
$$R = \frac{V_{DC}}{I_{DC}} = 5 \Omega$$

$$120\pi = \omega$$

$$T = \frac{1}{60}$$

$$V_r = (I_{DC} T / C)^{1/2}$$

$$C = I_{DC} T / 2V_r = 0.167F$$



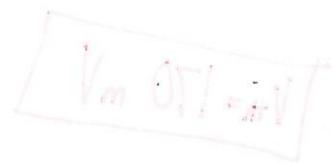
2210 test 2

Saturday, March 11, 2017 9:37 AM

Joshua Causwell

(192)

Leave at least one empty space between you and your
neighbors.

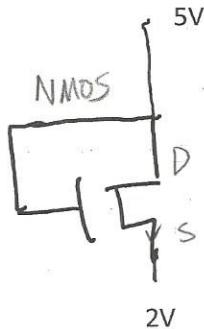
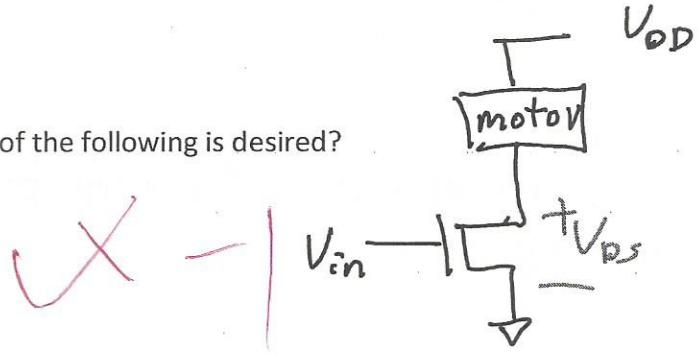


MOSFET+ bonus (20)

Saturday, March 11, 2017 2:22 PM

For the NMOS to work as a closed switch, which of the following is desired?

- both*
- 1) A V_{in} much higher than threshold voltage
 - 2) A large W/L
 - 3) A V_{in} much less than threshold voltage
 - 4) A small W/L



- 1) Find V_{GS} and V_{DS} for the transistor on the left.
- 2) If $V_{th}=0.5V$, is the transistor in saturation operation?

$$V_{DS} = 5 - 2 = 3V$$

$$V_{GS} = 5 - 2 = 3V$$

$$1) \quad V_{DS} = 3V$$

$$V_{GS} = 3V$$

$$2) \quad V_{DS} \geq V_{GT} = 3 - 0.5 = 2.5V$$

Yes, it is saturated.

A transistor with $S = 85mV$ shows I_{off} of $1nA$. To reduce I_{off} to $0.01 nA$,

- 1) Should we increase or decrease V_{th} ? Increase.
- 2) By how much? 34%

$$I_{ds(\text{subthreshold})} = 100\text{nA} * \frac{W}{L} 10^{\frac{V_{gs}-V_{th}}{S}}$$

$$I_{off} = I_{ds}(V_{gs}=0) = 100 \text{nA} \cdot \frac{W}{L} \cdot 10^{-\frac{V_{th}}{S}}$$

$$0.01 \text{nA} = 100 \text{nA} \cdot \left(\frac{W}{L}\right) \cdot 10^{-\frac{V_{th}}{0.085}}$$

$$\log(0.0001) = \left(\frac{W}{L}\right) \cdot 10^{-\frac{V_{th}}{0.085}} \log$$

$$+4 = +\frac{V_{th}}{0.085} \log\left(\frac{W}{L}\right)$$

$$V_{th} = 0.34$$

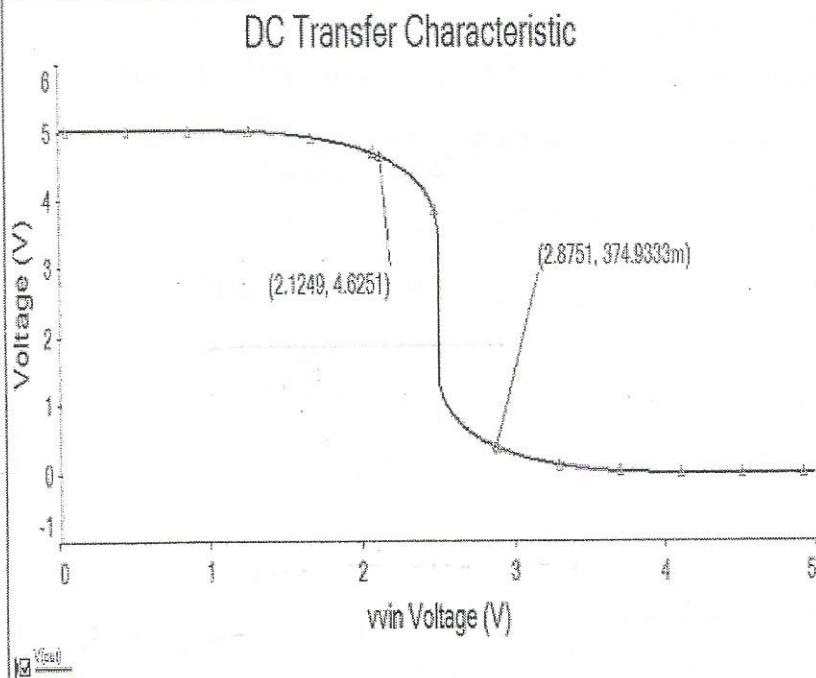
$$\boxed{V_{th} = 170 \text{ mV}}$$

X - 4

Dc Inverter noise margin (10 points)

Saturday, March 11, 2017 4:20 PM

An inverter Vout-Vin is simulated with Multisim. The "-1" slope points were obtained using cursor functions as follows:



1. 2.1V is:
 - a. A valid input low
 - b. A valid input high
 - c. An invalid input

- a. A valid input low
- b. A valid input high
- c. An invalid input

Complex Logic Gate Design (30 points)

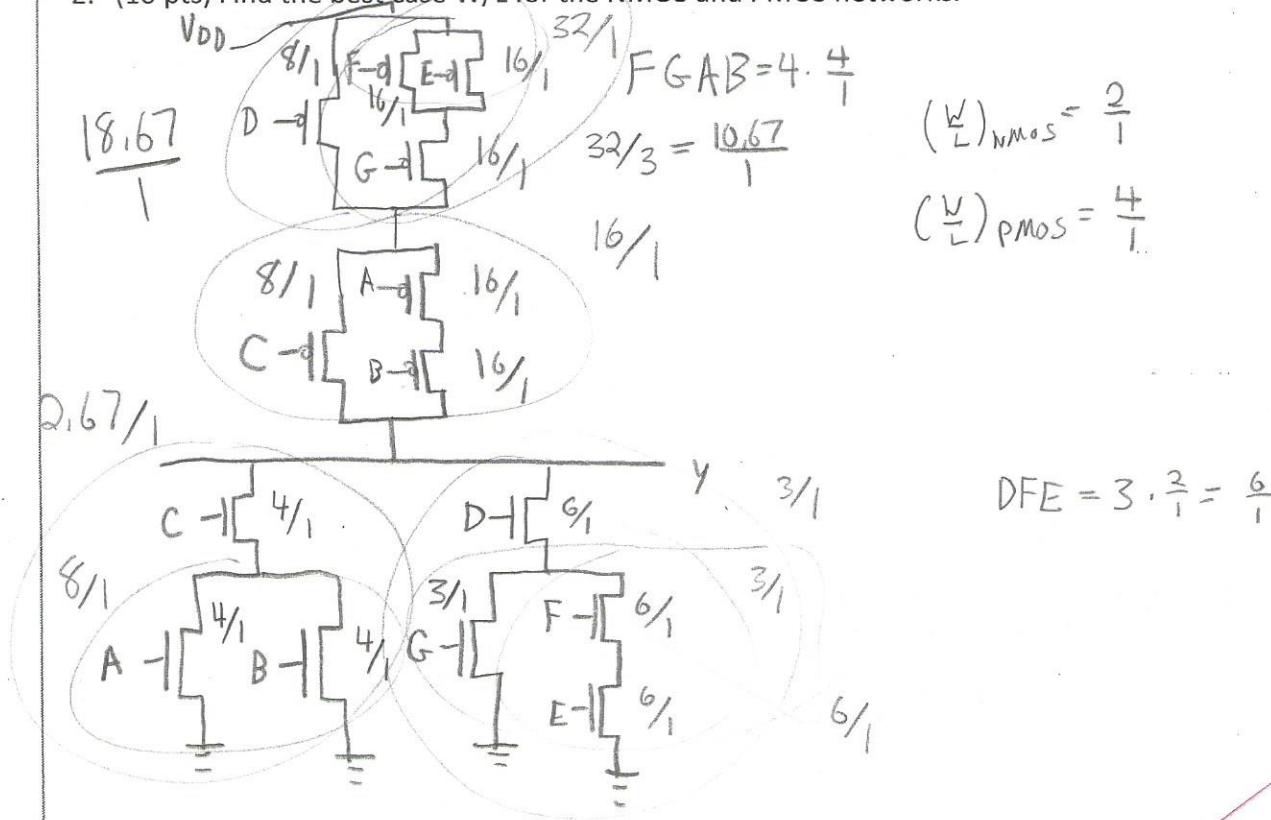
Saturday, March 11, 2017 4:20 PM

- (20 pts) Design a CMOS complex logic gate for

$$y = \overline{(A+B)C + (G+FE)D}$$

Worst case speed needs to be twice the speed of the reference, where (W/L) is 1/1 for NMOS and 2/1 for PMOS.

- (10 pts) Find the best case W/L for the NMOS and PMOS networks.



Best Case

NMOS:	$\frac{5}{1}, \frac{5}{1}$
PMOS:	$\frac{8}{1}, \frac{6}{1}$

$$\frac{1}{\frac{1}{18.67} + \frac{1}{16}} = 8,616$$

Energy, power and throughput (20)

Friday, July 19, 2013 5:04 PM

Consider these processors:

- $V_{dd} = 1.4V$, 1.4GHz single core.
- A quad core, size of each core is half of the original core, $V_{dd} = 0.7V$, $f=0.7\text{GHz}$.

- For the **same total number of clock cycles** run by all cores in a processor, if the energy consumed by the single core processor is $10\text{Watt} \times \text{hour}$, find the energy consumed by the quad core processor.

Hint: use the percentage change of energy required for the same job

$$10\text{ Wh}$$

$$10 \cdot .25 = 2.5$$

$$P_1 = 1 \cdot (1.4)^2 \cdot (1.4 \times 10^9) = 2.744 \times 10^9$$

$$P_2 = \left(\frac{1}{2}\right) \cdot (4) \cdot (0.7)^2 \cdot (0.7 \times 10^9) = 0.686 \times 10^9$$

$$\frac{P_2}{P_1} = 25\%$$

$$2.5 \text{ W} \cdot \text{h}$$

$$1.25 \text{ W} \cdot \text{h}$$

✓ ✓

- Continuing, for the problem above, if the time taken by the single core is 1 hour, find out the time that would be taken by the quad core processor.

Hint: use throughput difference

$$T_{h1} = 1.4$$

$$T_{h2} = 4(0.7) = 2.8$$

$$\frac{T_{h1}}{T_{h2}} = 50\%$$

✓

$$\boxed{\text{time} = 30 \text{ minutes}}$$

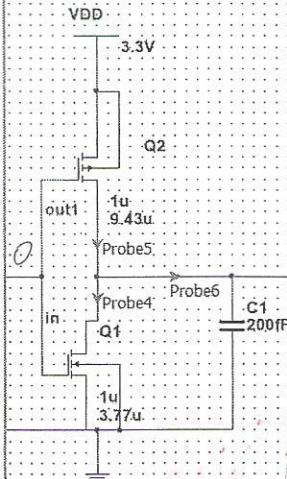
digital system dynamics (10 points)

Saturday, March 11, 2017 4:20 PM

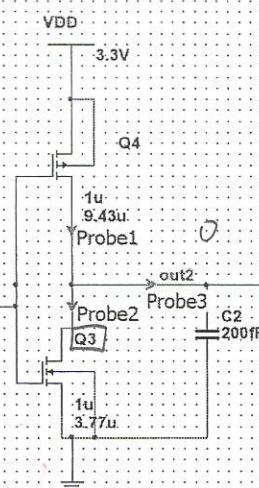
Below are voltage waveforms of input and outputs, and a few selected current waveforms of a chain of 5 inverters.

- 1) Mark the two points you need to find τ_{PLH} of the 2nd inverter (5).
- 2) Mark the time interval during which transistor Q3 is flowing a current with a box on the waveforms (5).

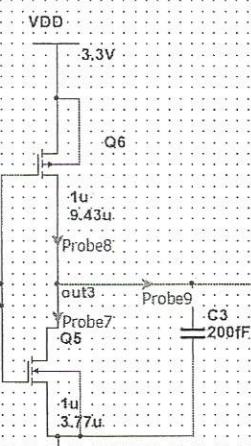
No. 1



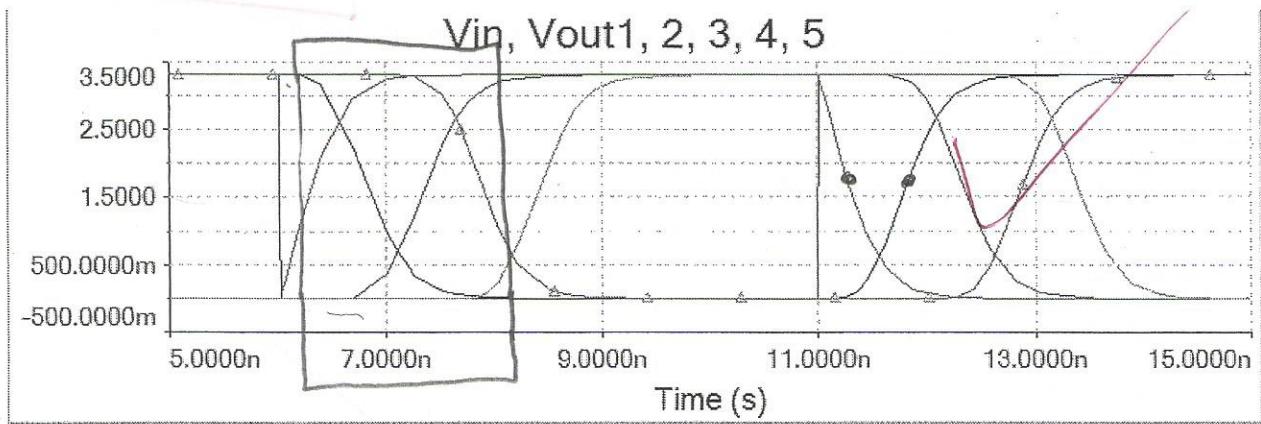
No. 2



No. 3



... no. 4 and 5
(not shown)

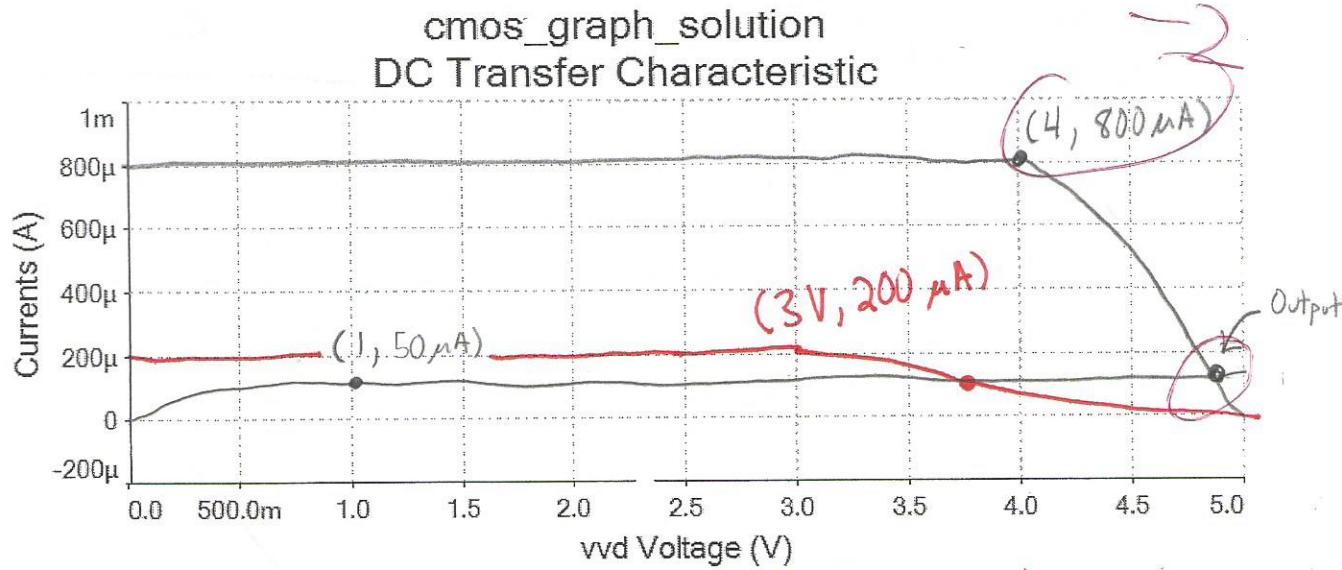


CMOS I-V/VTC/Sizing (10)

Thursday, July 05, 2012 2:47 PM

Consider a CMOS inverter with $K_P = 40 \mu A/V^2$ for PMOS, $100 \mu A/V^2$ for NMOS. $V_{TN} = -V_{TP} = 1V$. $W/L = 1/1$ for NMOS, $2.5/1$ for PMOS. $V_{DD} = 5V$.

Sketch IDS of NMOS and ISD of PMOS as a function of V_d as V_d increases from 0 to V_{DD} at an input voltage of 2V. The transistor saturation point's current and voltage must be explicitly calculated and labeled for both NMOS and PMOS. V_{out} must be labeled as well.



$$I_{DS,SAT} = \frac{1}{2} (100 \times 10^{-6})(1)(2-1)^2 = 50 \mu A$$

$$I_{SD,SAT} = \frac{1}{2} (40 \times 10^{-6})\left(\frac{2.5}{1}\right)(2-5-1)^2 = 800 \mu A$$

$$V_{GT} = -4 V$$

$$V_{Nmos}$$

$$V_{DS} \geq V_{GT} = 1$$

$$V_{DS} \geq 1 V$$

$$V_{PMOS}$$

$$V_{GS} = -3$$

$$V_{TP} = -1$$

$$V_{GT} = -4 V$$

$$V_{DS} \leq -4 V$$

$$V_{OUT} = 1$$

$$V_{DS} \leq 5-1$$

$$V_{DS} \leq 4 V$$

$$3V$$

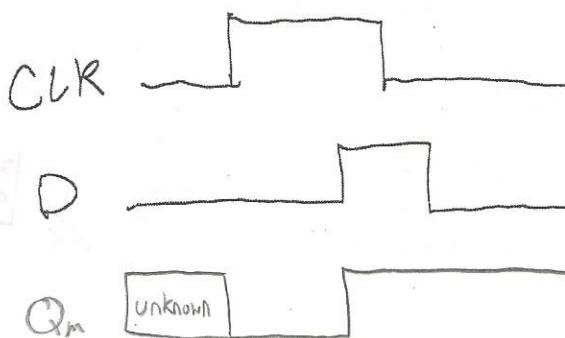
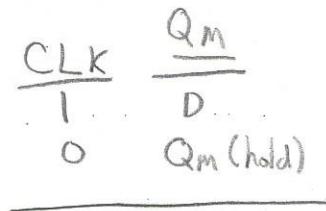
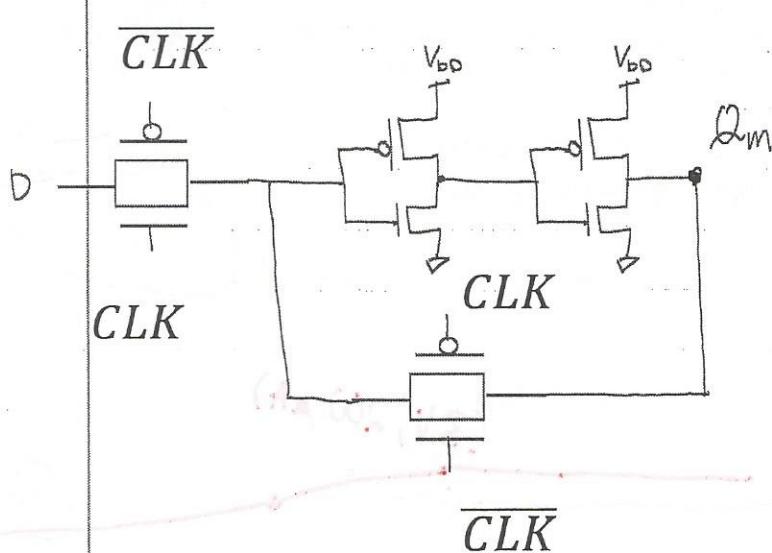
-2

$$V_{OUT} - 5 = -4$$

Sequential circuits (10 points)

Monday, March 19, 2012 5:20 PM

Draw waveform of Q_m . For unknown state, just label it as "unknown".



Elec 2210 Test 3

Sunday, April 23, 2017 10:16 AM

92

Name: Joshua Crouse

1. One page single side equation sheet with equations only
2. One empty seat minimum between you and your neighbor
3. Do not spend too much time on one problem.

Buffer (15)

Wednesday, April 20, 2016 11:21 AM

Design a 3 stage buffer circuit with these parameters: $C_0=10fF$, $CL=10pF$, $W/L=4/1$ for PMOS, and $2/1$ for NMOS in reference.

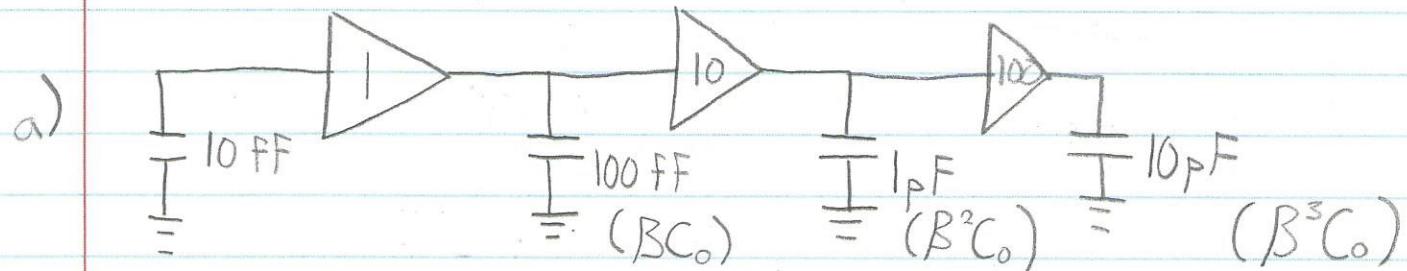
Minimum feature size is 20 nm.

- Draw schematic showing values of all capacitances and relative sizes of all stages
- Determine NMOS and PMOS W and L for all stages using relative sizes obtained.

$N=3$

(15)

$$\beta = \left(\frac{C_L}{C_0}\right)^{1/3} = \left(\frac{10pF}{10fF}\right)^{1/3} = 10$$



$$\frac{W}{L} = \frac{4}{1} = \frac{80 \text{ nm}}{20 \text{ nm}}$$

$$\frac{W}{L} = \frac{2}{1} = \frac{40 \text{ nm}}{20 \text{ nm}}$$

b)

NMOS:	Stage 1	Stage 2	Stage 3
	<u>40 nm</u> 20 nm	<u>400 nm</u> 20 nm	<u>4000 nm</u> 20 nm

PMOS:

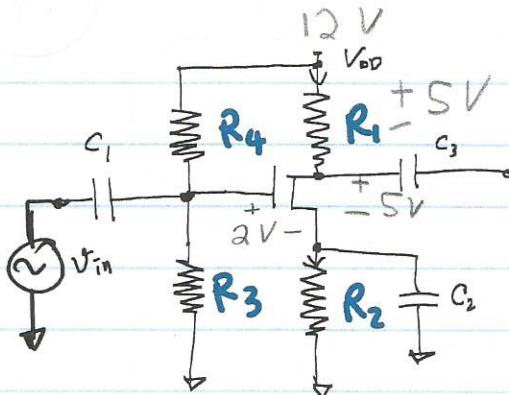
	Stage 1	Stage 2	Stage 3
	<u>80 nm</u> 20 nm	<u>800 nm</u> 20 nm	<u>8000 nm</u> 20 nm

Mos 4R (20)

Friday, April 13, 2012 5:04 PM

- Design R_1, R_2, R_3, R_4 to give $I_{DS} = 100\mu A$ with $V_{DD} = 12V$ and $R_{EQ} = 250k\Omega$, $KP = 100\mu A/V^2$. V_{GS} of 2V has been found to give desired current from ELVIS measurement. Use a 2V DC feedback and design your DC bias point to maximize output voltage swing.

$$V_{DS} = \frac{12-2}{2} = 5 V$$



$$R_1 = \frac{5V}{100\mu A} = 50 k\Omega$$

$$R_2 = \frac{2V}{100\mu A} = 20 k\Omega$$

(20)

$$R_4 V_g = \frac{12 R_3 R_4}{R_4 + R_3}$$

$$R_4 V_g = 12 R_{EQ}$$

$$R_4 = \frac{12(250k)}{4} = 750 k\Omega$$

$$V_g = 2 + 2 = 4 V$$

$$R_{EQ} = \frac{R_3 R_4}{R_3 + R_4}$$

$$R_3 R_{EQ} + R_4 R_{EQ} = R_3 R_4$$

$$R_4 R_{EQ} = R_3 (R_4 - R_{EQ})$$

$$R_3 = \frac{R_4 R_{EQ}}{(R_4 - R_{EQ})} = \frac{(750k)(250k)}{(750 - 250)k} = 375 k\Omega$$

$$R_1 = 50 k\Omega$$

$$R_2 = 20 k\Omega$$

$$R_3 = 375 k\Omega$$

$$R_4 = 750 k\Omega$$

2. Estimate the highest V_{DS} possible under a large ac input

3. Estimate the highest I_{DS} possible under a large ac input

$$2.) V_{DS} = V_{DD} - V_S = 12 - 2 = 10 V$$

$$3.) I_{DS} = \frac{V_{DD} - V_S}{R_1} = \frac{12 - 2}{50k} = 200 \mu A$$

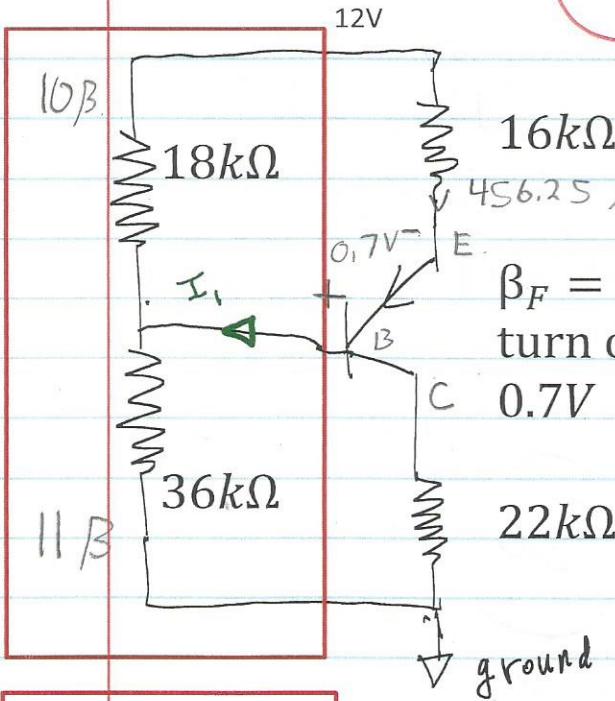
Bipolar 4R (10).

Friday, July 19, 2013 5:04 PM

6.

- Find I_1 only for the PNP 4R circuit.

Hint: use Thevenin equivalence.



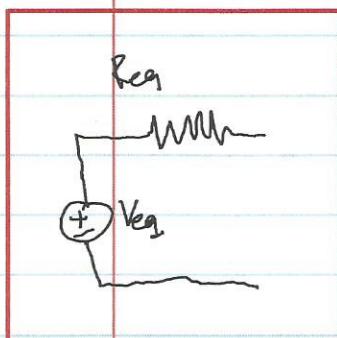
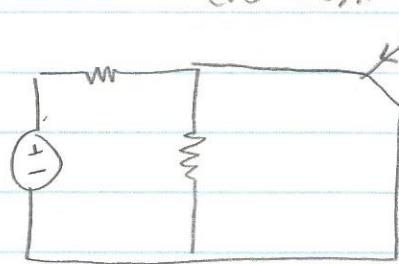
$$V_{EQ} = \frac{12 \cdot 36k}{(18+36)k} = 8V$$

$$\beta_F = 100$$

turn on:

$$0.7V$$

$$R_{EQ} = \frac{18 \cdot 36}{(18+36)k} = 12k\Omega$$



$$I_E = I_B + I_C$$

$$I_E = (101) I_B$$

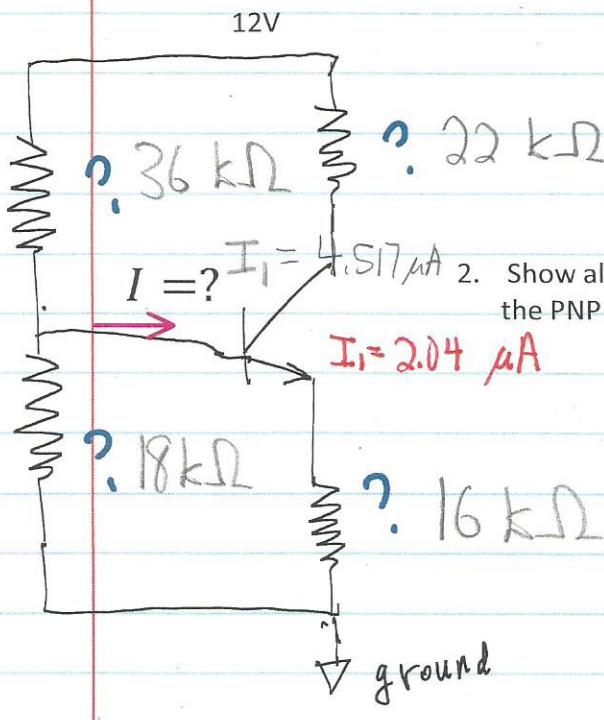
$$I_B = \frac{I_E}{101} = \frac{456.25 \mu A}{101}$$

$$7.3V$$

X

$$I_1 = 4.517 \mu A$$

$$-2 \quad I_1 = 2.04 \mu A$$

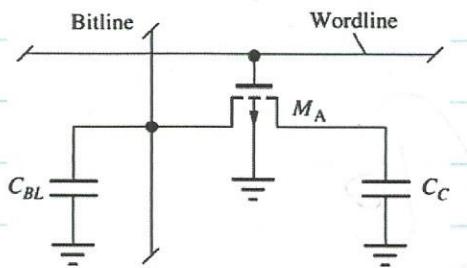


- Show all resistances and the I at the probe on a NPN design symmetric to the PNP design.

-1

DRAM (15)

Wednesday, April 20, 2016 11:55 AM



(11)

$V_{DD} = 1.4V$. Transistor $V_T = 0.4V$. $C_{BL} = 99C_C$.

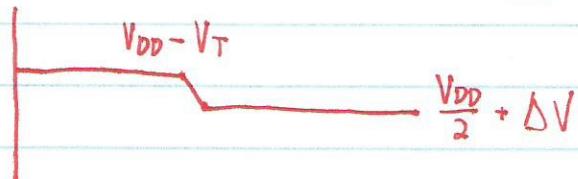
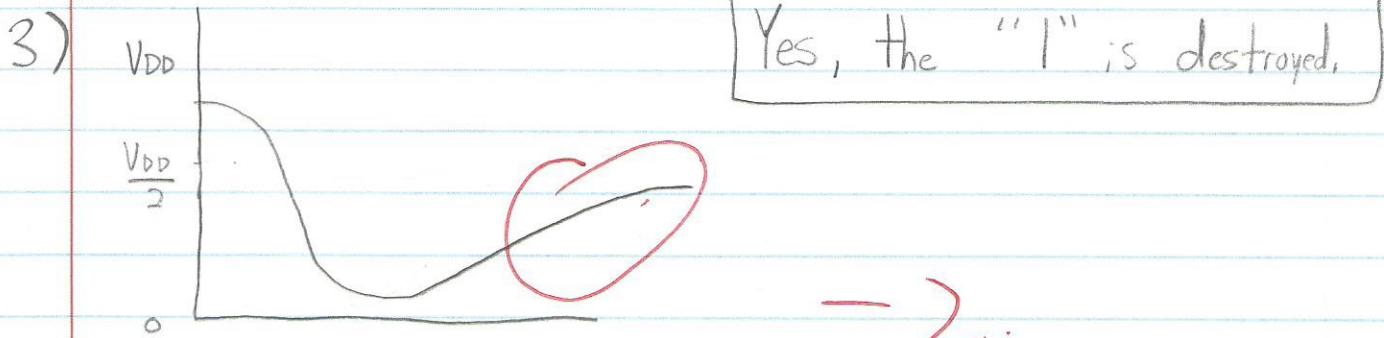
- 1) What is the final cell voltage after writing "1" to a cell storing "0"? (5)
- 2) Next, bitline is precharged to $V_{DD}/2$ to read the cell, calculate cell voltage after reading (5).
- 3) Sketch the waveform of cell voltage to show how it changes by reading, is the stored "1" destroyed or not? (5).

$$1) V_F = \frac{V_{DD} - V_{TH}}{1 + 99} = \frac{1.4 - 0.4}{100} = 1 \text{ V}$$

$V_F = 1 \text{ V}$

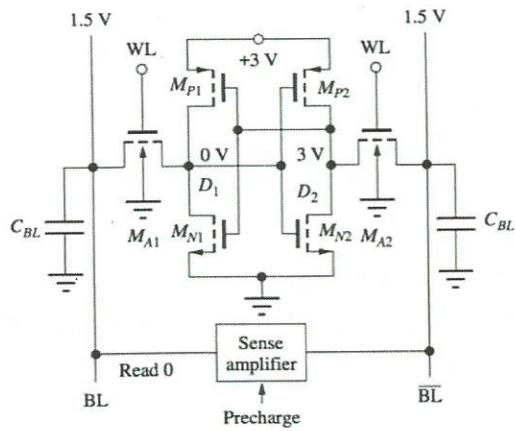
$$2) \Delta V = \left(\frac{V_{DD}}{2} - V_{TH} \right) \frac{C_C}{99C_C + C_C} = (0.7 - 0.4) \left(\frac{1}{100} \right) = 3 \text{ mV}$$

$$V_F = \frac{V_{DD}}{2} - \Delta V = \frac{1.4}{2} - 0.003 \quad \text{---} \\ \boxed{V_F = 0.697 \text{ V}} \quad \text{X} \quad 0.703 \text{ V}$$



SRAM (10)

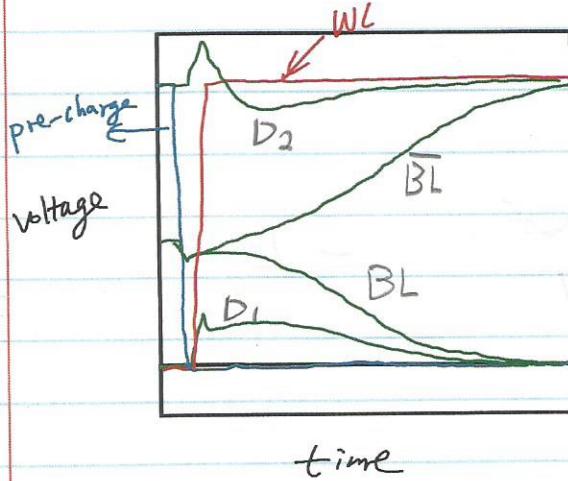
Friday, July 22, 2016 3:16 PM



GO

Figure 8.5 Reading data from a 6-T cell with a 0 stored in the cell.

To read a cell storing "0", BL and \overline{BL} are precharged to $VDD/2$. Wordline is then activated. Identify on the waveforms below D_1 , D_2 , BL, and \overline{BL} .

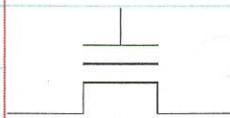


ZERO

Flash (10)

Monday, November 16, 2015 9:21 AM

9.



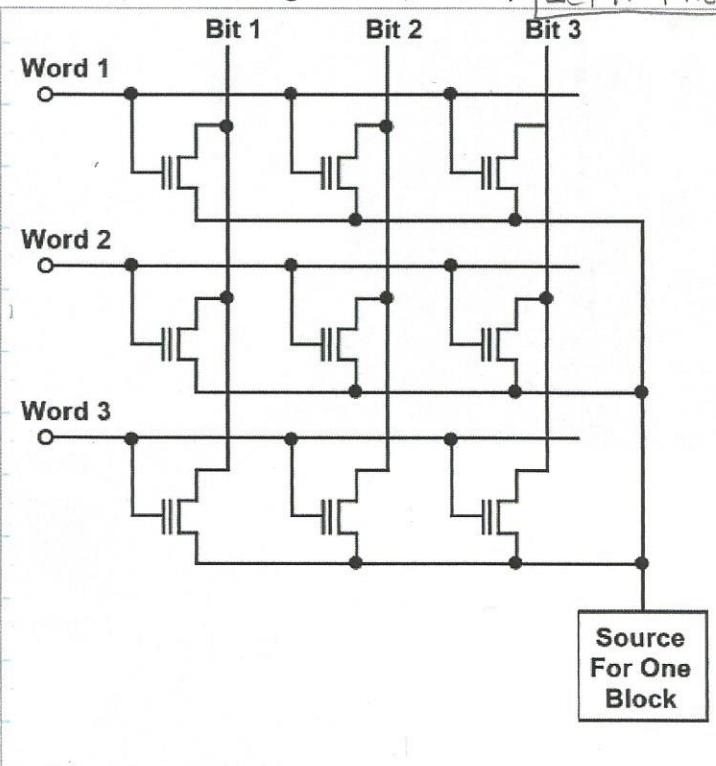
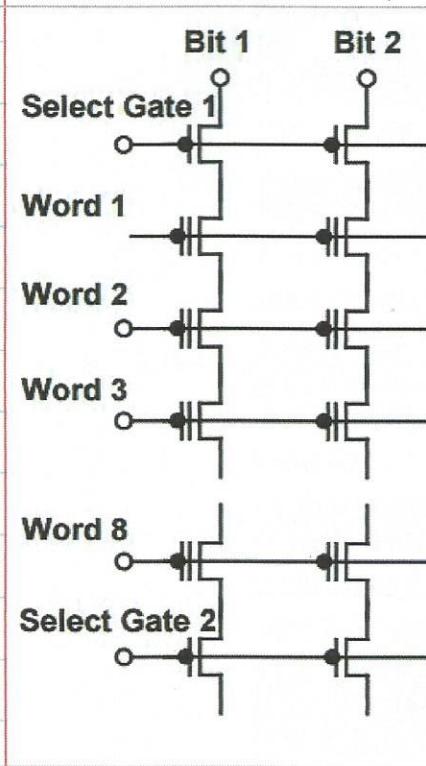
1. Which state has a higher threshold voltage, programmed or erased?
2. Which of the following is NOR? Right.

3. Which has a higher density when fabrication, the left or right circuit, and why?

Programmed.

Left. The shared bit

lines lead
to more
transistor
per area.

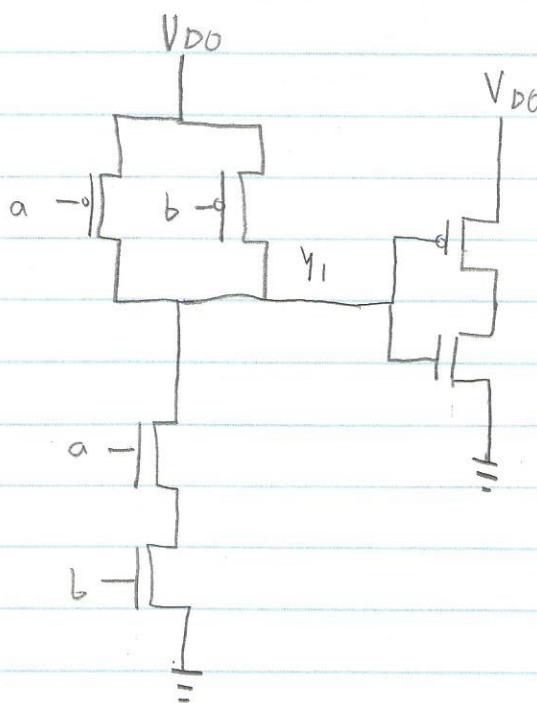
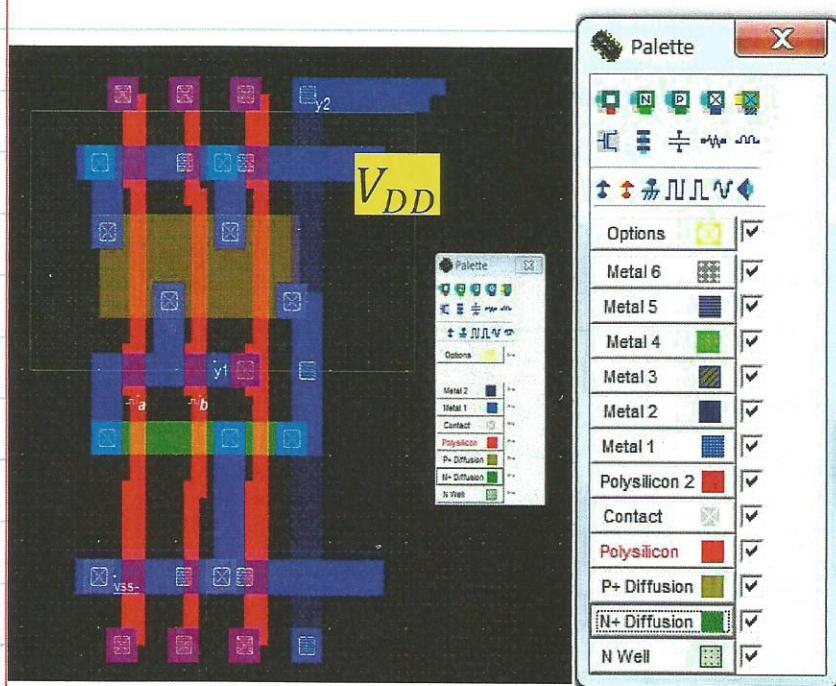


-1
less
connections

Layout 1 (10)

Thursday, July 19, 2012 3:34 PM

- draw transistor level schematic, find y_1 and y_2 as functions of a and b .



a	b	y_1	y_2
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

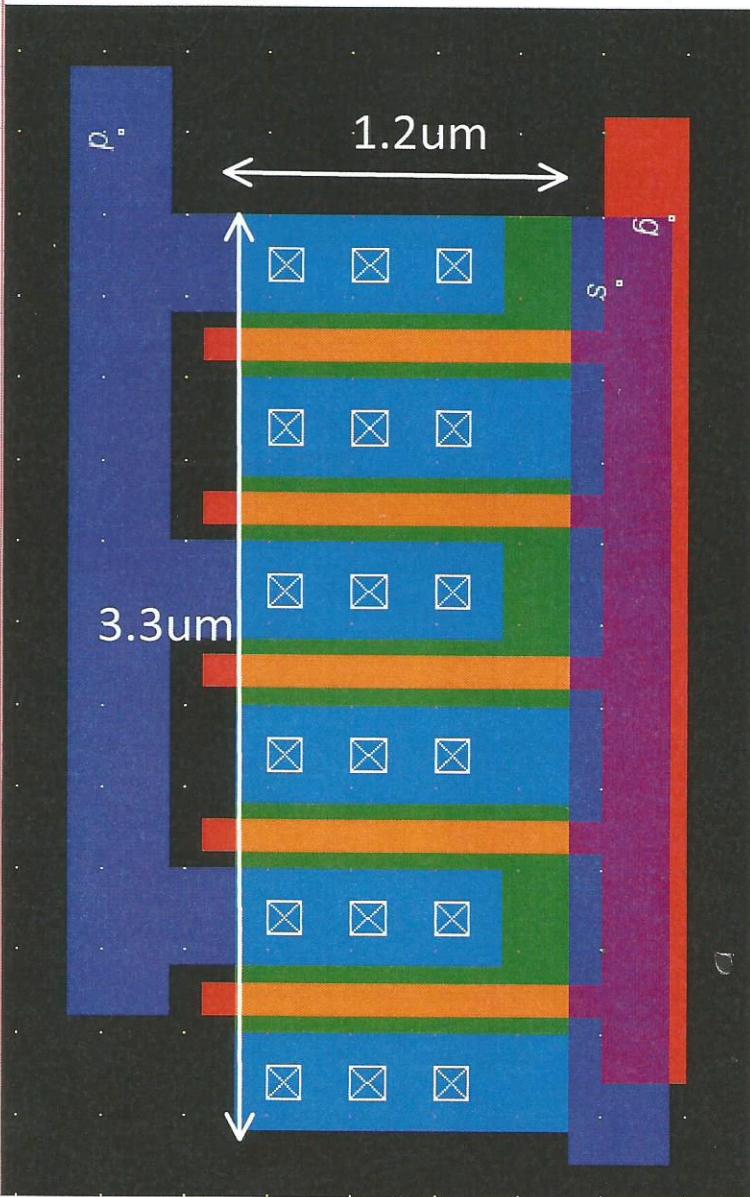
$$Y_1 = \overline{ab} \quad [\text{NAND}]$$

$$Y_2 = ab \quad [\text{AND}]$$

Layout 2 (6)

Monday, May 4, 2015 3:34 PM

The green n+ rectangle size is 1.2um x 3.3um below, gate length is 0.12um, find effective W/L.



$$W_{eff} = 5 \cdot 1.2 \mu m$$

$$W_{eff} = 6 \mu m$$

$$L_{eff} = 0.12 \mu m$$

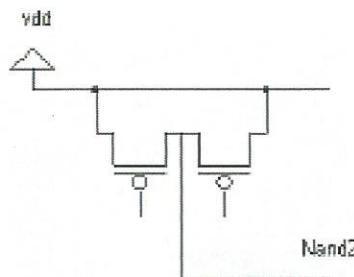
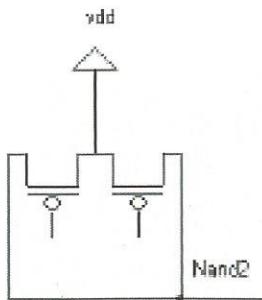
(6)

$$\frac{W}{L} = \frac{6 \mu m}{0.12 \mu m} = \frac{50}{1}$$

Layout 3 (4)

Sunday, April 23, 2017 9:16 AM

For the NAND2 PMOS designs shown, which is better? Why?



(G)

The right design is better. The benefit is the shared P+ region. This leads to less junction capacitance and therefore a faster output.