Grade scope Practice

Full Practice Test 2

1) Which of the following will become better if we decrease the V_{DD} of a CMOS inverter?

- [ ] Speed
- [ ] Delay
- [x] Power
- [ ] Noise Margin
- [ ] V_{IH}

2) Consider a symmetric CMOS inverter with 1 nS delay, if we double $\frac{W}{L}$ of NMOS, while keeping everything else the same, determine low to high delay in nS.

A: low to high is handled by PMOS, high to low is handled by NMOS, so delay of low to high does not change

3) Explain why CMOS logic has zero standby power according to many textbooks. What assumptions are made in drawing such a conclusion? If we consider sub-threshold current, how is the answer affected?

A: One CMOS gate will be off (either NMOS or PMOS), resulting in no current flow, no current means no power consumption. If current is below threshold, there will be finite current flow therefore finite power consumption.

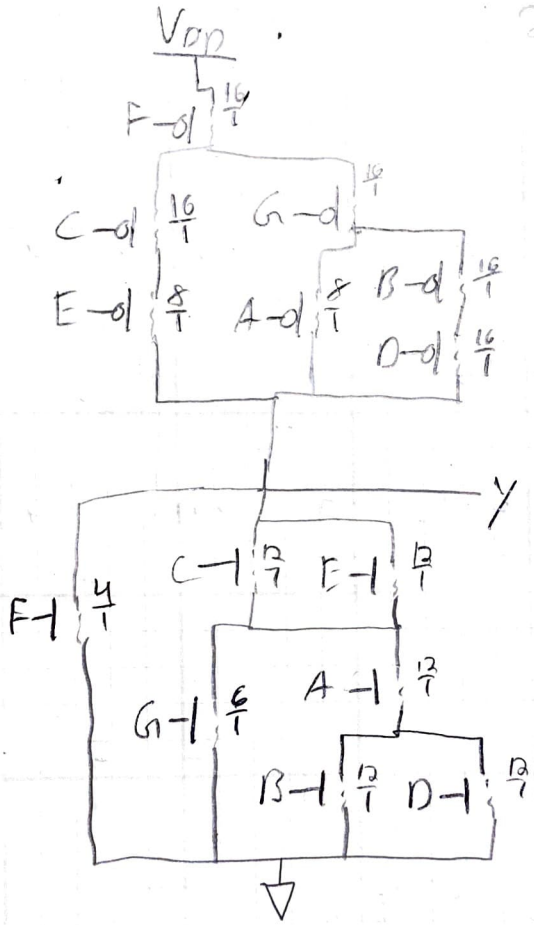
4) Design CMOS complex logic gate for 'y'. The worst case speed needs to be twice the speed of the reference CMOS inverter, in which NMOS W/L is $2/1$ and PMOS is $2/1$.

$$y = \overline{(C+E)(G+(B+D)A)+F}$$

half the delay (twice the speed)

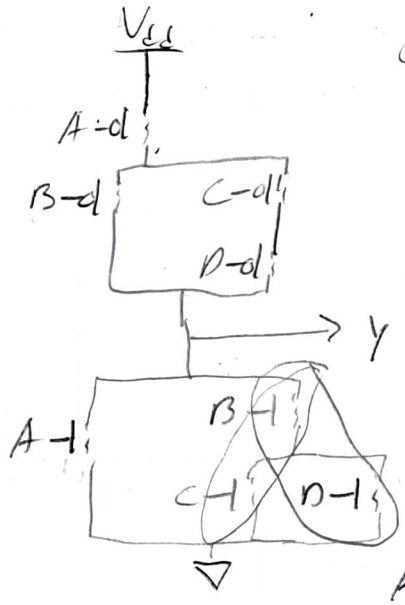
$2 \cdot \frac{2}{1} \rightarrow 2 \cdot \frac{2}{1} = \frac{4}{1}$ for Nand P.

$$\frac{1}{\left(\frac{W}{L}\right)_1} + \frac{1}{\left(\frac{W}{L}\right)_2} = \frac{1}{\left(\frac{W}{L}\right)_{eff}}$$



5) View complex CMOS Logic Circuit below

a)



Q: Assuming that $\frac{W}{L}$ for all NMOS is $\frac{2}{1}$ and all PMOS is $\frac{3}{1}$. Which input switching combinations below lead to the longest high to low delay?

~~A~~ NMOS handles high to low
~~A~~ PMOS handles low to high

A: largest NMOS chain is B, C and B, D equally

b) What is the effective W/L of the PMOS network when all inputs switch together?

~~A~~ To find answer, add all PMOS $\frac{W}{L}$ together, accounting for series and parallel connections, Series = $\frac{1}{\frac{W}{L}} + \frac{1}{\frac{W}{L}}$; Parallel = $\frac{W}{L} + \frac{W}{L}$

All PMOS $\frac{W}{L} = \frac{3}{1}$

$C+D = \frac{1}{\frac{3}{1}} + \frac{1}{\frac{3}{1}} = \frac{3}{2}$ $C+D \| B = \frac{3}{2} + \frac{3}{1} = \frac{9}{2}$ $(C+D\|B) + A = \frac{1}{\frac{9}{2}} + \frac{1}{\frac{3}{1}} = \boxed{\frac{1.8}{1}}$

6) Design a Symmetric CMOS inverter that can drive a capacitive load of 0.5pF with a maximum speed of 500MHz in a digital system. $V_{TO(NMOS)} = 0.2V$ $V_{TO(PMOS)} = -0.2V$

$k_{p(NMOS)} = 1000\mu A$ $k_{p(PMOS)} = 500\mu A$

$V_{DD} = 1.2V$; min size is 28nm

$C = 0.5pF$ (10^{-12})

max speed $= 500MHz \rightarrow \frac{1}{5\tau_p} = 500MHz \rightarrow \tau_p = 0.4nS$

Digital System means $\tau_p = 2.4 R_{on} C \rightarrow R_{on} = \frac{\tau_p}{2.4C} = \frac{0.4nS}{2.4(0.5pF)} = 333\Omega$

$\frac{W}{L}_N = \frac{1}{k_P \cdot R_{on} \cdot (V_{DS} - V_{TO})} = \frac{3}{1} = \boxed{\frac{84nm}{28nm}}$ NMOS

$\frac{W}{L}_P = \frac{k_N}{k_P} \cdot \left(\frac{W}{L}\right)_N = \frac{1000}{500}\left(\frac{3}{1}\right) = \frac{6}{1} = \boxed{\frac{168nm}{28nm}}$ PMOS