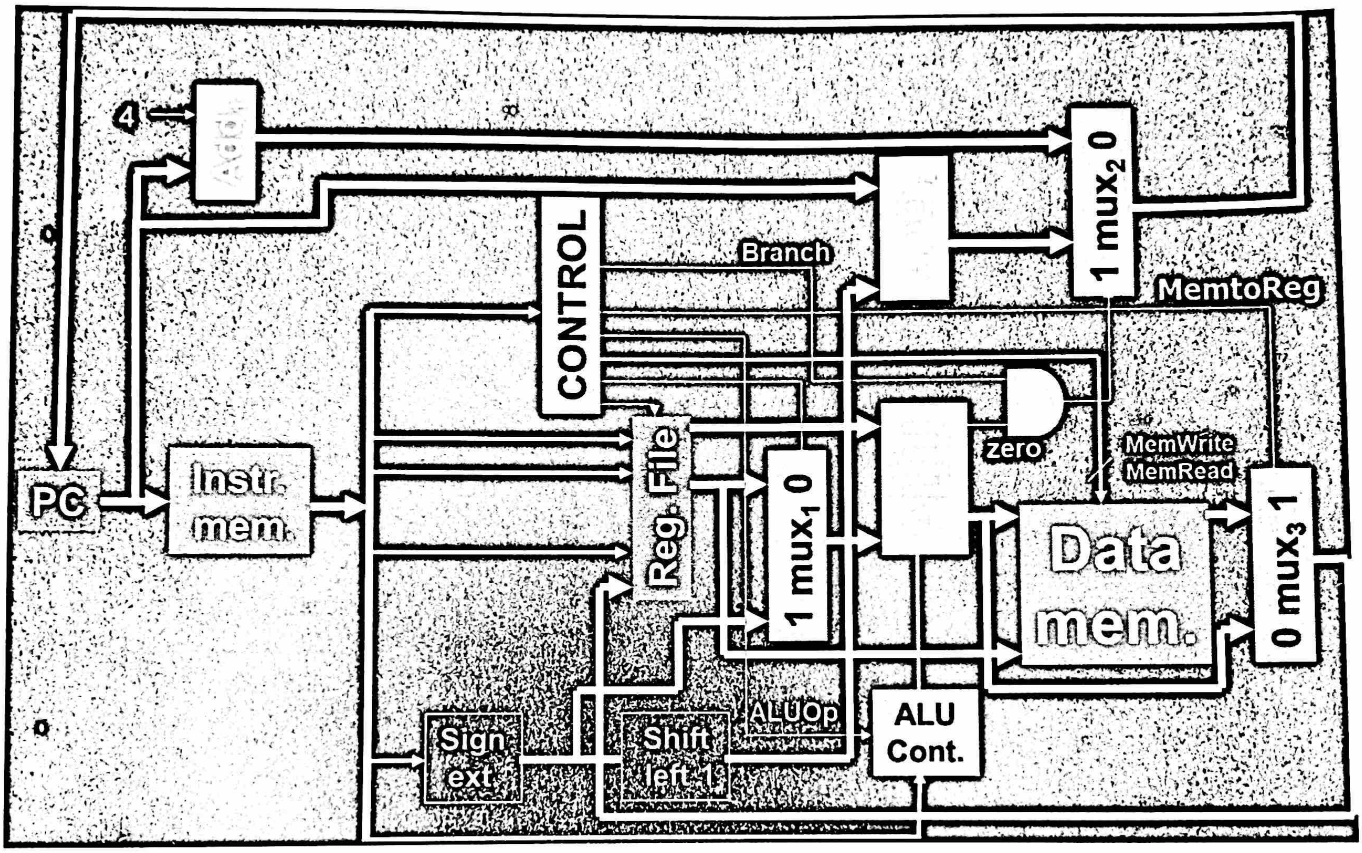
ELEC 5200/6200 (Fall 2021)
Homework 4
Assigned 10/01/21, due 10/11/21

For questions 1-3 refer to the block diagram of the single cycle datapath below (see slides for listing of all signal names):



Question 1: Consider the instruction:

`and rd, rs1, rs2` // Which performs the function: Reg [rd] = Reg[rs1] & Reg[rs2].

(a) What are the values of the control signals required to process this instruction? (4 points)

Branch =0
MemtoReg =0
AluOp = 000
Reg Dst = 1
ALUSrc=0
MemWrite=0
Mem Read=0
Reg Write=1

(b) Which functional units (blocks in the block diagram) perform a useful function in the execution of this instruction? (2 points)

- PC
- Instruction Mem
- Reg file
- ALU
- PC adder
- Mux

(c) Which functional units produce no output when processing this instruction? (2 points)

Data Memory since MemRead = 0

(d) Which functional units produce output which is not used? (2 points)

- Sign extender
- Shift left 1
- Branch adder

Question 2: Consider a program which has the following mix of instructions:

R-type:	24%	I-type (ALU):	28%	Load:	25%
Store:	10%	Branch:	11%	Jump:	2%

(a) What percentage of instructions in the program access data memory? (2 points)

load + Store so, 25% + 10% = 35%

(b) What percentage of instructions in the program access instruction memory? (2 points)

R-type + I-type So, 24% + 28% = 52%

(c) What percentage of instructions in the program require the use of the sign extend unit? (2 points)

All but R-type gives sign extended

28% + 25% + 10% + 11% + 2% = 76%

(d) What does the sign extend unit do during clock cycles when it is not required? (2 points)

Sign extended is only used for 76% of instructions + it is ignored for all other instructions

Question 3: Assume a single cycle datapath has functional units with the following latencies:

Mem access:	250ps	Reg file read:	150ps	Mux:	25ps
ALU:	200ps	Adder:	150ps	AND gate:	5ps
PC read:	30ps	Reg setup time:	20ps	Sign extend:	35ps
Shift Left:	15ps	Control unit:	40ps	ALU Ctrl:	10ps

Note: The PC read time is the time it takes from the beginning of the clock cycle for the new value to show up at the register output. Reg setup time is the minimum amount of time before the active clock edge that a signal must be held stable for it to be clocked into a register without errors.

a) Determine the latency of an R-type instruction: (2 points)

PC read + mem access + reg Setup time + reg file read + mux
+control + Aluctrl + ALU + mus + reg setup time + adder + mux
= 945 ps

b) Determine the latency of a lw instruction. (2 points)

PC read + mem accesst reg Setup time + mux + Sign extended + control
+ Alu Ctrl + ALU + mem access + mux + reg setup time + adder + mux
= 1230 ps

c) Determine the latency of a sw instruction. (2 points)

PC read + memacess + reg setuptime + mux + Sign eatended
+ Control + ALU ctrl + AlU + mem acces + mux + adder + mux

= 1210 ps

d) Determine the latency of the beq instruction. (2 points)

PCread + memaccess + reg Setup time + mux + control + Aluctrl
+ And Gate + mux + Sign extended + Shift left + ALU + adder + mux
= 920ps

e) Determine the latency of I-type (ALU) instruction. (2 points)

PC read + mem access + reg setup time + mux + control + ALU ctrl + ALU
+ mux + reg setup time + sign extended + adder + mux = 980 ps

f) Given the latencies calculated in parts (a) – (e), determine the minimum clock period for this cpu. (2 points)

longest latency = 1230 ps

Clk period must be 1230 ps to account for longest
instuction time