ELEC-4200

Digital System Design

FROM: Jacob Howard

TO: Prof. Ujjwal Guin

DUE DATE: 3/11/21

Lab 8

Introduction

The goal of this lab was to familiarize ourselves with the basics of how Vivado optimizes circuits and how to prevent them to develop circuit structures such as Ring Oscillators. Also, we learned how to design an RO structure and use a hard macro to specify placement on the FPGA. There was only one task in this lab that implemented everything. The TA checked off all work.

Task 1

In Task 1, we were asked to design a 5 stage and a 9 Stage Ring Oscillator. These were to be built into separate files. Once we designed both, we were asked to write test benches for both. You can find the design codes in Code 1 and Code 2 respectively and the test benches in Testbench 1 and Testbench 2. The screenshots of the simulations can be seen in Figure 1 and Figure 2.

Next, we were asked to create hard macros for both designs. The screenshots for the macros can be seen in Figures 3 and 4. Lastly, we were to show the TA the in and out ports of both designs. These can be seen in Figures 5 and 6. This completed the entire lab.

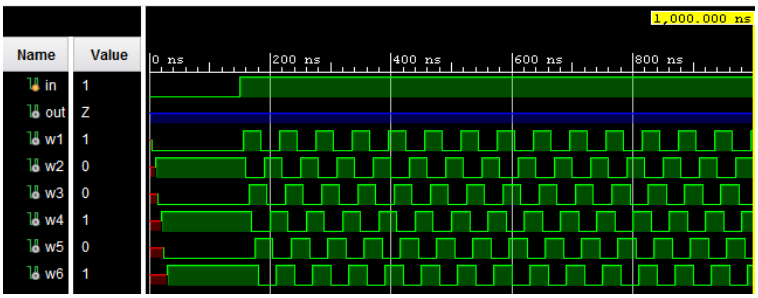

Figure 1

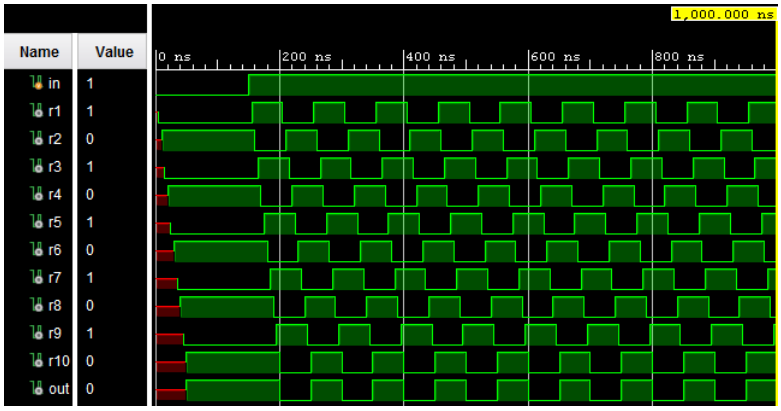

Figure 2

```
(* ALLOW_COMBINATIONAL_LOOPS = "TRUE"
*)
   (* DONT_TOUCH = "TRUE" *)  wire w1, w2, w3,
w4, w5, w6;
   //first RO level 5
   begin
   and #5 (w1, in, w6);
   not #5 (w2, w1);
   not #5 (w3, w2);
   not #5 (w4, w3);
   not #5 (w5, w4);
   not #5 (w6, w5);
   assign w6 = out;
   end

endmodule
```

Code 1

```
(* ALLOW_COMBINATIONAL_LOOPS = "TRUE"
*)
  (* DONT_TOUCH = "TRUE" *)  wire r1, r2, r3, r4,
r5, r6, r7, r8, r9, r10;

  //2nd R0 lvl 6
  begin
     and #5 (r1, in, r10);
     not #5 (r2, r1);
     not #5 (r3, r2);
     not #5 (r4, r3);
     not #5 (r5, r4);
     not #5 (r6, r5);
     not #5 (r7, r6);
     not #5 (r8, r7);
     not #5 (r9, r8);
     not #5 (out, r9);
     assign r10 = out;
  end


endmodule
```

Code 2

```
assign w1 = DUT.w1;
assign w2 = DUT.w2;
assign w3 = DUT.w3;
assign w4 = DUT.w4;
assign w5 = DUT.w5;
assign w6 = DUT.w6;

       initial begin
       #1550 $finish; //runs simulation 100 times
       end

       initial begin
       in = 0;
       #150 in = 1;

       end
endmodule
```

Testbench 1

```
assign r1 = DUT.r1;
    assign r2 = DUT.r2;
    assign r3 = DUT.r3;
    assign r4 = DUT.r4;
    assign r5 = DUT.r5;
    assign r6 = DUT.r6;
    assign r7 = DUT.r7;
    assign r8 = DUT.r8;
    assign r9 = DUT.r9;
    assign r10 = DUT.r10;

    initial begin
    #1550 $finish; //runs simulation 1550 times
    end

    initial begin
    in = 0;
    #150 in = 1;

      end
endmodule
```

Testbench 2

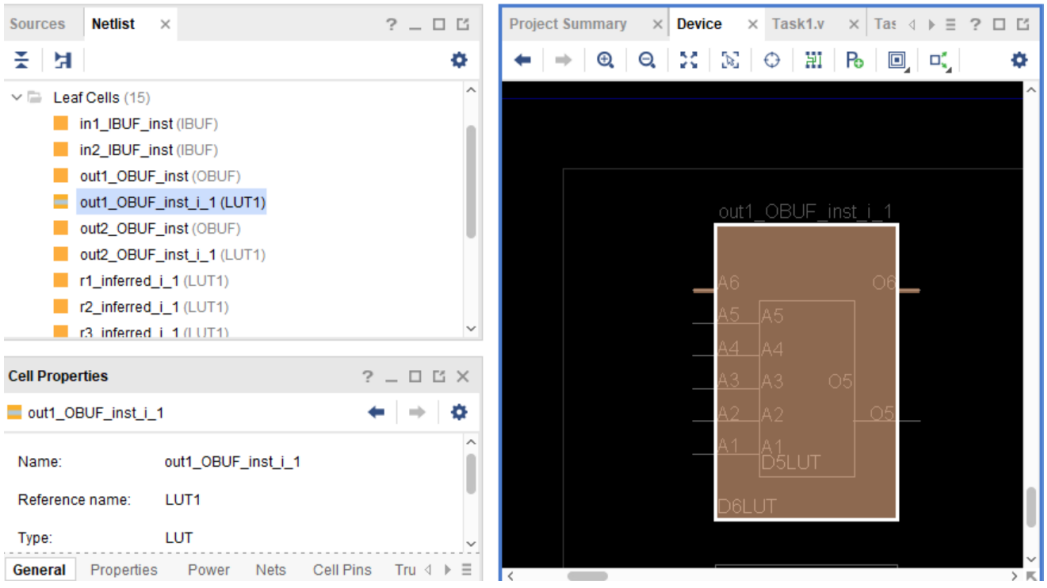

Figure 3

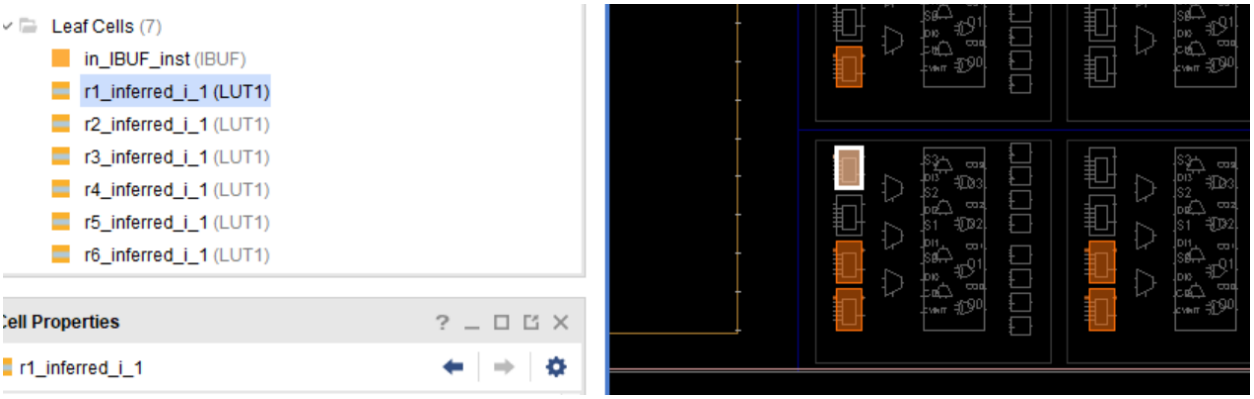

Figure 4

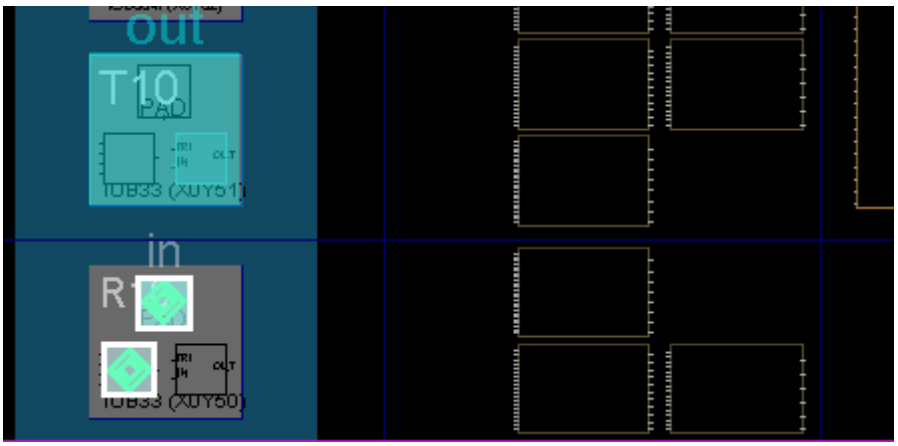

Figure 5

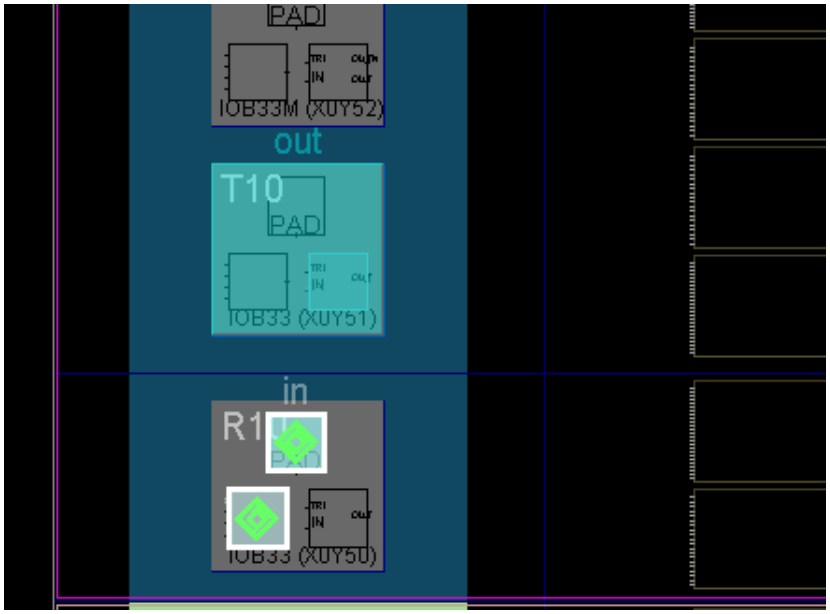

Figure 6

Conclusion

In conclusion, this lab was very simple to do and a nice change of pace from the other labs. This lab took me about 30 minutes the day before to complete, while normally labs will take me a couple of hours to complete the day before. Everything in the lab manual was well written and explained how to implement everything well. I did not have any issues while doing this lab.