ELEC 5200/6200 (Fall 2021)
Homework 1
Assigned 08/25/21, due 09/01/21

Question 1: What are Harvard and von Neumann architectures? (2 points)

Harvard
Stores machine instruction and Data in different memory

Von Neumann
Same memory and Bus are used to store both Data and instructions

Consider the following assembly code written for the IAS computer. Each memory word contains either a 40-bit constant or two 20-bit (left-L and right-R) instructions. Two 30-word integer data arrays, A(I) and B(I), start at memory locations 50 and 100 respectively. Answer the following questions regarding the assembly program.

Memory Address	Instruction / Data value	Comment
0	0	Constant N, initialized to 0
1	1	Constant, set to 1
2	6	Constant, set to 6
3	29	Constant, set to 29
4	50	Constant, set to 50
5L	LOAD M(50)	Transfer A(0) from Memory address 50 to AC
5R	LSH	Multiply AC by 2
6L	LSH	
6R	LSH	
7L	ADD M(2)	Place AC + [value from Memory address 2] in AC
7R	STOR M(100)	Transfer AC to B(0) at Memory address 100
8L	LOAD M(0)	Load N into AC
8R	SUB M(3)	Place N – 29 in AC
9L	JUMP +M(13, 20:39)	Test AC, if N – 29 >= 0 then jump to inst 13R
9R	LOAD M(0)	Load N into AC
10L	ADD M(1)	Increment AC by 1
10R	STOR M(0)	Update N in Memory address 0
11L	ADD M(4)	
11R	STOR M(5, 8:19)	Modify memory address/operand of instruction 5L
12L	ADD M(4)	
12R	STOR M(7, 28:39)	Modify memory address/operand of instruction 7R
13L	JUMP M(5, 0:19)	
13R	HALT	

Question 2: What value should be loaded into the PC register to begin execution of the program?

(1 point) Harvard Von

memory address 0

Question 3: What result does the program produce? (4 points)

N is updated from 0 to 29 and then 29 is subtracted. Program checks N-29 and goes to halt

Question 4: What is the value of memory location 0 when the program terminates? (3 points)

zero

Question 5: Generate the machine code (binary) for memory addresses 3, 5, 7, 9, and 12 of the program. The program is replicated in the table below for your convenience. (9 points)

Memory Address	Instruction / Data value	Machine Code (binary)
0	0	----------
1	1	----------
2	6	----------
3	29	000000000000000000000000000011101
4	50	----------
5L	LOAD M(50)	00000100000011001000010100000000000
5R	LSH	
6L	LSH	----------
6R	LSH	
7L	ADD M(2)	00000101000000000110 00100001 00000110 0100
7R	STOR M(100)	
8L	LOAD M(0)	----------
8R	SUB M(3)	
9L	JUMP +(M13, 20:39)	00010000 000000001101 00000001 00000000000
9R	LOAD M(0)	
10L	ADD M(1)	----------
10R	STOR M(0)	
11L	ADD M(4)	----------
11R	STOR M(5, 8:19)	
12L	ADD M(4)	0000101 000000110010 000100111 000000000111
12R	STOR M(7, 28:39)	
13L	JUMP M(5, 0:19)	----------
13R	HALT	

Question 6: Assume that a processor uses arithmetic instructions with a CPI of 1, load/store instructions with a CPI of 12, and branch instructions with a CPI of 5. Consider running a program on this processor which contains 2.56x109 arithmetic instructions, 1.28x109 load/store instructions, and 0.256x109 branch instructions. Assume the processor runs at 2GHz.

a) Find the total execution time for this program. (2 points)

$$2.56\times10^9 + 12(1.28\times10^9) + \frac{5(0.256\times10^9)}{2\times10^9} = 9.6\ \text{sec}$$

b) If the CPI of the arithmetic instructions was doubled, what would the impact on the execution time of the program (specifically) be? (2 points)

$$\frac{2\times 2.56\times10^9 + 12\times 1.28\times10^9 + 5\times0.256\times10^9}{2\times10^9} = 16.88\ \text{sec}$$

c) What would the CPI of the load/store instructions need to be reduced to in order for the program to complete in 2/3 of the original runtime? (4 points)

$$\frac{9.6}{3} = 3.2\cdot 2 = 6.4$$

$$6.4 = \frac{[2.56\times10^9 + (x\cdot 1.28\times10^9) + (5\cdot 0.256\times10^9)]}{2\times10^9}$$

$$1.28\times10^{10} = 2.56\times10^9 + (x\cdot 1.28\times10^9) + (5\times 0.256\times10^9) = 7.61\times10^9$$

$$x\cdot 1.28\times10^9 = \quad x = 5.95 = 6\ \text{CPI}$$

Question 7: Consider two processors P1 and P2 with the parameters specified in the table below. Each of these processors runs a program compiled with the number of instructions specified. Answer the following...

	Clock Rate	Instructions	Avg CPI
P1	4 GHz	5.0×10^9	0.9
P2	3 GHz	1.0×10^9	0.75

a) (3 points)

Determine analytically if the processor with the fastest clock rate has the best performance.

P_1 $\frac{4 \times 10^9}{0.9} = 4.44 \times 10^9$ instructions per sec

P_2 $\frac{3 \times 10^9}{0.75} = 4 \times 10^9$ instructions per sec

So, P_1 has best performance. The faster clock rate allows for more instructions to be performed over time

b) (4 points)

Determine analytically if the processor running the largest number of instructions requires more or less CPU time than the other processor. Explain your answer.

P_1 requires more CPU time since it has a slower CPI. The instructions will be in the CPU for longer than P2

c) (3 points)

Determine analytically if the processor with the largest MIPS has the best performance (defined here as completing the program the fastest).

Yes. Millions of Instructions Per Second is a relative performance rating. The largest MIPS should have the best performance. (best time doing same instructions)

d) (3 points)

Determine analytically if the processor with the most MFLOPS performs the best. Use the assumption that 40% of the executed instructions are floating point instructions.

Millions of floating point operations per second is another measure of performance. I would say since MFLOPS performance can differ in different systems and only 40% of instructions are floating point, it would be difficult to assume the higher MFLOPS processor is better,