ELEC 5200/ELEC 6200 Computer Architecture and Design
Class Test 2, Solution, Nov. 14, 2018 **Total 45 points**
Broun 235, 11:00-11:50AM

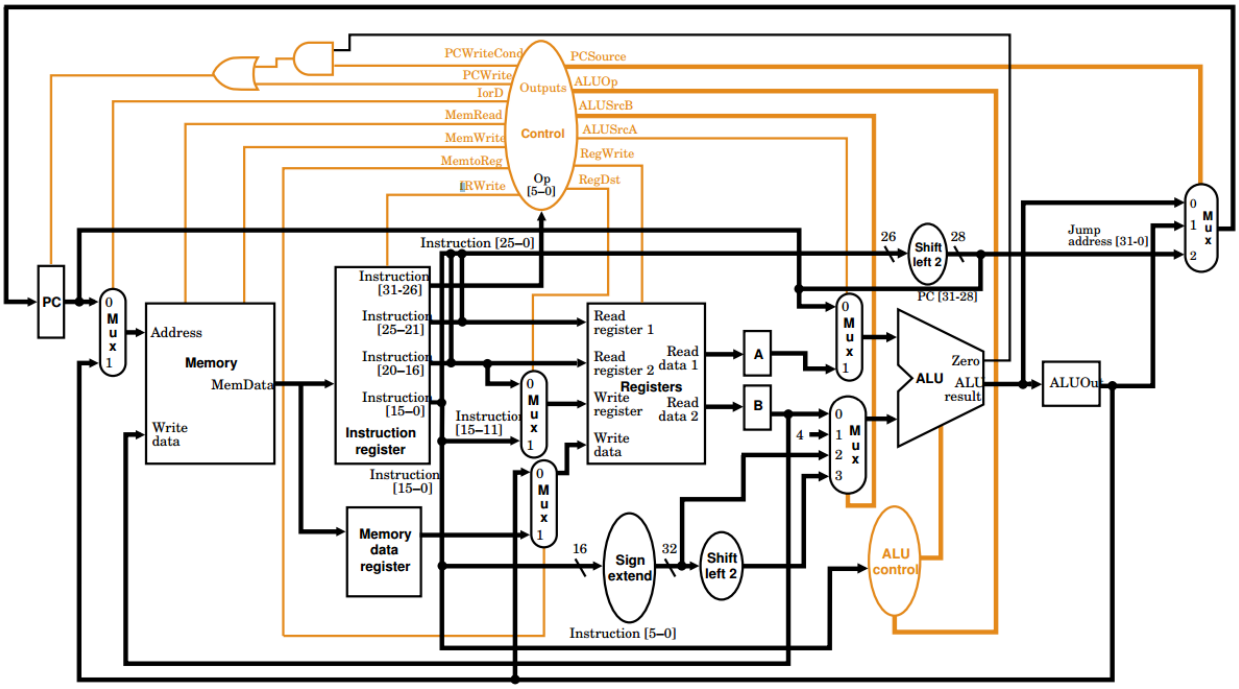
Instructions: Attempt all problems. Write your answers in the provided space. Be sure to review your answers before turning them in. Thank you and good luck!

1. If the ideal CPI of a single cycle processor and a pipelined processor are both 1, why is one design desirable over the other?: (1 point)

Answer:

Both designs complete an instruction in (approximately) one cycle on average, but the cycle time for a pipelined processor is generally shorter. Thus the pipelined design can complete more instructions per second compared to the single cycle design.

For questions 2 and 3 use the multi-cycle datapath diagram provided below:



2. The RTL for Step 1, Instruction Fetch, is:

```
IR = Memory[PC];
PC = PC + 4;
```

Fill in the values that are required for the following control signals: (4 points)

Answer:

ALUSrcA = **0** ALUSrcB = **01**

PCSource = **00** IorD = **0**

3. The RTL for Step 2, Instruction Decode, is:

```
A = Reg[IR[25-21]]
B = Reg[IR[20-16]];
ALUOut = PC + (sign-extend(IR[15-0]) << 2);
```

Fill in the values that are required for the following control signals: (2 points)

Answer:

ALUSrcA = **0** ALUSrcB = **11**

4. Name the three types of pipeline hazards and briefly describe each one. (6 points)

Answer:

A. **Structural hazard - Results from a resource conflict.**

B. **Branch (or control) hazard - The instructions in the pipeline are not the ones that are to be executed due to a change in control flow (i.e. a branch).**

C. **Data hazard - An instruction cannot complete execution because one or more required operands (data) are the result of a previous (incomplete) instruction and not yet available.**

5. Draw a pipeline diagram for the code below, assuming the MIPS pipeline that we used in class. Show stalls and/or forwarding where needed. (5 points)

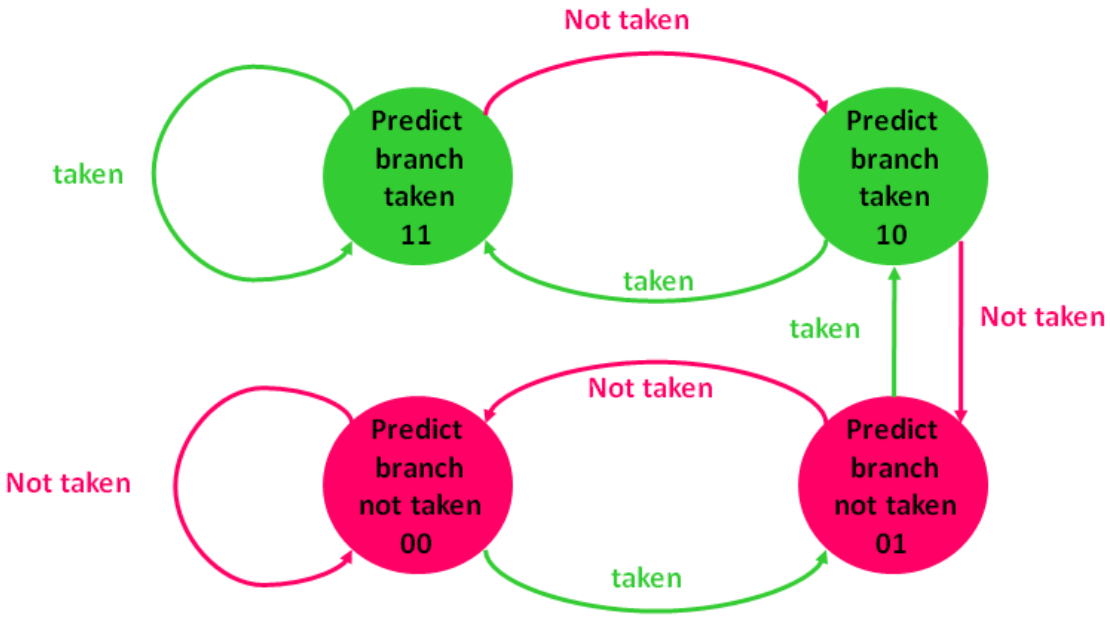
```
add $s1, $s3, $s4
lw $v0, 0($s1)
sub $v0, $v0, $s1
```

Answer:

CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8	CC9	CC10	Instr
FE	DE	EX	MEM	WB						add $s1, $s3, $s4
	FE	DE	EX	MEM	WB					lw $v0, 0($s1)
		BUB	BUB	BUB	BUB	BUB				bubble / stall
			FE	DE	EX	MEM	WB			sub $v0, $v0, $s1

6. Draw the state transition diagram for the two bit branch prediction scheme studied in class. (4 points)

Answer:



7. In what way is the two-bit branch prediction scheme studied in class more robust than the 1-bit branch prediction scheme from class. (1 point)

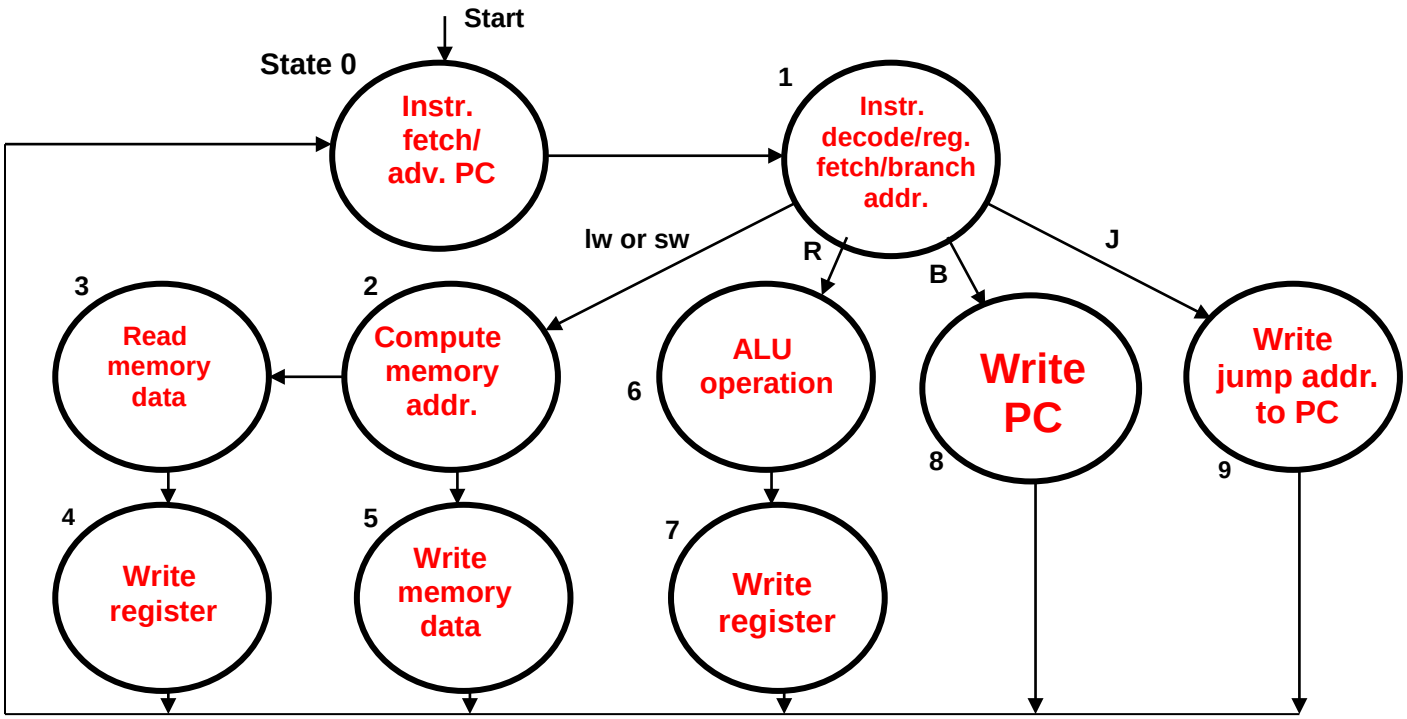
Answer: ***In the two-bit prediction scheme a branch that is repeatedly predicted correctly must be wrong twice before the prediction changes.***

8. What are the primary benefits and/or drawbacks of a pipeline with a large number of stages? (2 points)

Answer: ***A pipeline with more stages generally has a faster clock cycle (ie higher frequency) due to a smaler worst-case delay in the combinational logic. However, a pipeline with many stages tends to have a higher branch penalty.***

9. Complete the state transition diagram for the multicycle datapath discussed in class. (Reg xfers not necessary, just state the task for each state) (10 points)

Answer:



10. For the single cycle processor X assume the following:
    200 ps for memory operations
    100 ps for ALU operations
    50 ps for register file access

    If both a single cycle datapath X and a multi-cycle datapath Y (as shown on test page 1) are running the same benchmark consisting of the following instruction mix:

    20% lw, 10% sw, 11% branch, 3% jump, 56% ALU instr

    Calculate the performance ratio (using ave instruction execution time) for the datapaths. Show your work. (10 points)

Answer:

For the single cycle processor the cycle time is determined by the longest instruction, which is lw.

The cycle time of lw contains the delay of the following units:

lw := IF + REG READ + ALU + MEM + REG WRITE
= 200ps + 50ps + 100ps + 200ps + 50ps
= 600ps

CPI_{SINGLE} for any single cycle processor is 1. Therefore the average instruction execution time for the single cycle processor is:

$T_{EX\text{-}SINGLE}$ = 600ps * 1 = 600ps

For the multicycle datapath the cycle time is determined by the individual cycle with the longest delay. Referring to the state diagram from question 9 we see that cycles where memory is accessed result in the longest delay of 200ps (states 0, 3, and 5). Therefore, the cycle time for the multicycle datapath is 200ps.

The CPI for the multicycle datapath can be calculated using the benchmark instruction mix along with the number of cycles required for each instruction type.
Recall that: lw = 5 cycles, sw & ALU = 4 cycles, jump & branch = 3 cycles

CPI_{MULTI} = 0.20*5 + 0.10*4 + 0.11*3 + 0.03*3 + 0.56*4 = 4.06

The average instruction execution time for the multicycle processor is:

$T_{EX\text{-}MULTI}$ = 200ps * 4.06 = 812ps

The performance ratio of single cycle to multicycle is therefore:

$$\frac{T_{EX\text{-}SINGLE}}{T_{EX\text{-}MULTI}} = \frac{600\text{ ps}}{812\text{ ps}} = 0.7389$$