ELEC 2210 - EXPERIMENT 3
Medium Scale Integrated (MSI) Circuits

The objectives of this experiment: In this lab you will work with some simple MSI (medium scale integration) logic circuits to build and test a digital system. In particular, you will design, build, and test an 8-channel multiplexing/demultiplexing digital communication system. You will also be introduced to some of the circuits used to develop computer components. The objectives of this experiment include:

- Learn to use decoders/demultiplexers /output selectors
- Learn to use multiplexers /data selectors
- Design, implement, and test a multiplexed digital communication system
- Continue to build experience with the ELVIS workstation and digital simulation
- Continue to develop professional communication skills

I. Introduction

Digital telephones and other communication systems often use a single high-speed communication channel and "Time Division Multiplexing" (TDM) to carry data between multiple pairs of lower-speed communicating devices, as illustrated in Figure 1. In a K-channel TDM system, the devices are each allocated one time slot to transmit information, out of every K time slots, as illustrated in Figure 2. For example, a T1 line multiplexes data from 24 digital telephones over a single channel. A digital telephone converts voice signals to 8-bit data samples at a rate of 8K samples/second. Therefore, one 8-bit sample must be transmitted every 1/8KHz = 125msec. Every 125msec, a T1 line transfers 24 of these 8-bit samples, plus some "overhead" bits, for a total of 1.544Mbits/sec. As shown in Figure 1, a multiplexer at the transmitting end performs the TDM by connecting data source Ain to the channel for 8 bit times, with the bits routed to device Aout by a demultiplexer at the receiving end. Then the multiplexer and demultiplexer alternately select Bin-Bout, Cin-Cout, … Kin-Kout, returning to Ain-Aout and so on. The resulting TDM data transmission is illustrated in Figure 2. In this lab session, we will design, construct and test an 8-channel digital communication system, using standard MSI components: Decoder/Demultiplexer, Multiplexer, Binary Counter.

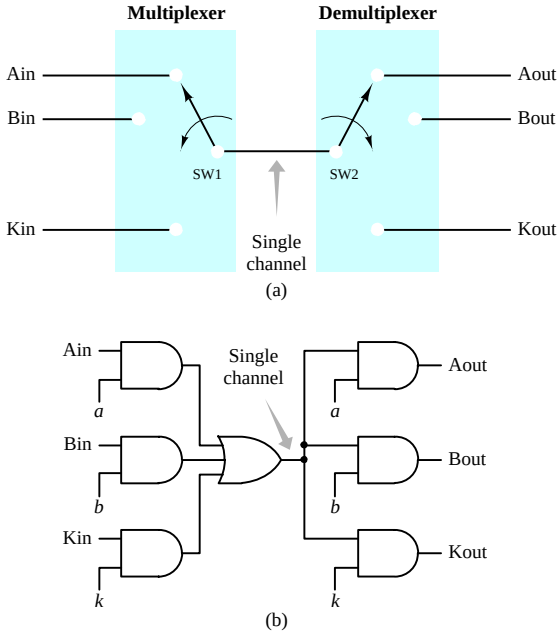


Figure 1. K-channel multiplexing/demultiplexing digital communication system

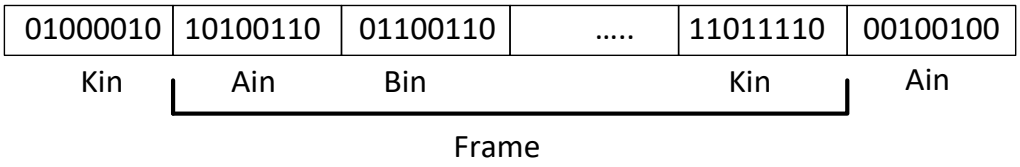


Figure 2. Time multiplexed data frame with K 8-bit time slots

II. Modular Combinational Logic Review

Multiplexers

Digital systems often use a single wire to carry information from several different components to a common destination. For example, the CPU in a computer is connected through a single bundle of wires to its memory chips, CD-ROM, disk drive, etc. In order to control who gets to communicate with the CPU, it is necessary to have a "switchboard" to manage the connections. A *multiplexer* (also called a *data selector*) is used as a switch to connect several inputs lines to a single output line. For example, the 74151 in Figure 3 can be used to switch between 8 inputs, numbered 0-7, that can be connected to the output Y (W is the just the complement of Y). The multiplexer has a group of data select lines (*C*,*B*,*A*) that are used to choose which input line is connected to the output. An additional input line, $\overline{EN}$, is used to enable/disable the chip. When $\overline{EN}$ is active (=0) then the multiplexer connects the output *Y to* the input line indicated by the select lines. When $\overline{EN}$ is inactive (=1), then *Y*=0, regardless of the other input values. The select lines are used as a 3 bit binary number to specify which of the input lines is connected to the output *Y*. *C* is the most significant bit, followed by *B*, and *A* is the least significant select bit. Thus, *CBA*=110 means that input line 6 is connected to the output *Y*. Multiplexers are referred to by size as "*n* to 1" multiplexers, where $n=2^j$ is a power of two. For example, the 74151 above is an 8 to 1 (or simply 8-1) multiplexer. A n-input multiplexer always has $\log_2(n)$ select lines; the 74151 has $\log_2(8) = 3$ select lines. A 4-1 multiplexer has two select lines; a 16-1 multiplexer has 4 select lines, etc.

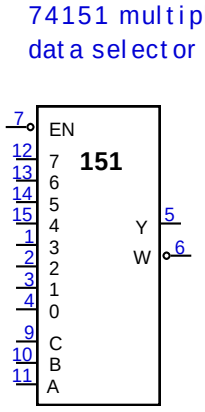


Figure 3. 74151 multiplexer/data selector

Decoders/demultiplexers

Digital systems often have sets of devices, of which at most one should be active. For example, when a computer reads from memory chips, exactly one memory location needs to be chosen and "activated."

A *decoder* is a switch used to "turn on" exactly one item out of a set. A decoder made from four 3-input AND-gates is shown in Figure 4. The input signals are an enable signal *EN* and two select lines, *S0* and *S1*. Since the enable signal is directly wired to all four AND gates, when *EN=0* the outputs are all inactive (0). On the other hand, when *EN=1*, the select lines are connected such that exactly one gate is chosen to be ON based on the value of *S0* and *S1*. For example, look at the AND gate connected to *Y1*. Its top input (like all the other gates) is connected to *EN*. The middle input is connected directly to *S0*, and the bottom input is connected to *S1* through an inverter. Thus, $Y1 = \overline{S1} \bullet S0 \bullet EN$. (The dots indicate logical AND function.). That is, *Y1* is active when (*S1*,*S0*) = (0,1) (binary representation of the number 1) and *EN* is active. The remaining gates are connected in a similar fashion so that they are active when the appropriate number is put on the select lines *S0*, *S1*.

The decoder design shown in Figure 4 is called a 2-to-4 (2:4) decoder because it has two select lines and $2^2 = 4$ output lines. Decoders are usually referred to by size in this fashion (*n* to 2^n decoders).

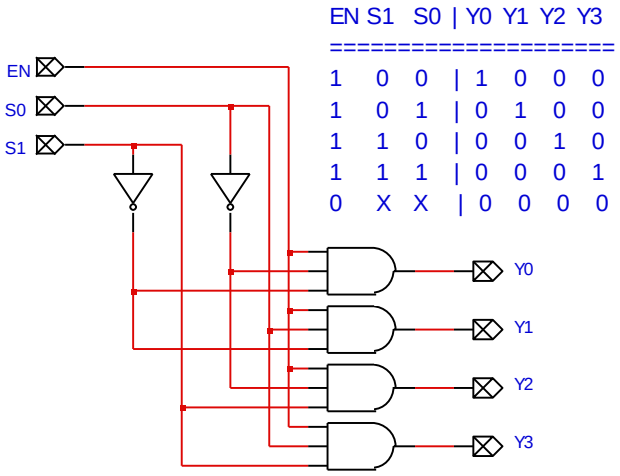


Figure 4. 2-to-4 decoder

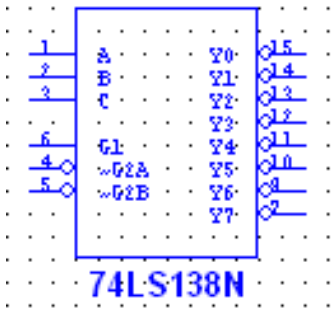


Figure 5. 74LS138 demultiplexer/decoder

Because decoders are used so often in digital systems, TTL manufacturers sell pre-packaged decoders such as the 74LS138 shown in Figure 5. Notice that the 74LS138 is a 3-to-8 decoder. The inputs are *C,B,A* where *C* is the "most significant bit" (i.e., *C*=1 means that one of lines 4,5,...,7 are selected). Notice also that the 74LS138 has three enable lines, *G1*, *~G2A*, *~G2B*. These inputs are connected inside the '138 so that *all three* inputs must be active (*G1* HIGH, *G2A* LOW and *G2B* LOW) for the chip to operate. That is, the chip is only active when *G1* = 1, *G2A* = 0 and *G2B* = 0.

Notice that the outputs of the 74LS138 are *active low*; that is, unlike the 2-4 decoder example in Figure 4, the 74LS138 is built with NAND gates so that its active output is a 0 and all inactive outputs are 1's. (In all digital circuits, it is important to check whether specific outputs or inputs

are active high or active low. Active low I/O will normally be indicated with an open circle, such as pins 4,5,7 and 9-15 on the '138 in Figure 4.)

Using a Decoder as a Demultiplexer

A demultiplexer performs the inverse operation of a multiplexer: it takes a single input line and connects it to exactly one output line, all other output lines being inactive. If you take a look at the 2-4 decoder in Figure 4, you'll see that it also serves as a 1-4 demultiplexer when you use the EN line as the input signal. For example, suppose *S1*=1 and *S0*=0 so that output line *Y2* is selected and all other outputs are inactive. If *EN*=1, then output *Y2* is also 1. Conversely, if *EN*=0, then so is *Y2*. In other words, a demultiplexer and a decoder are exactly the same thing.

Look back at the 74LS138 3-8 active low decoder chip in Figure 5. This chip has three enable lines, not just one enable line. The reason for this is simple: if the chip is used as a demultiplexer, one of the enable inputs is used for the signal input while one of the other two is used as an enable. Since a communication channel value of 0 should produce a 0 on the selected output, and since the 74LS138 outputs are active low, the channel should be connected to one or both of the active-low enable inputs (G2A, G2B). On the other hand, if the chip is used as a decoder, two of the enable inputs can be hard-wired in the enable state, with the third input used as the enable signal.

III. Pre-Lab

1. Obtain and study datasheets for the 74LS151 multiplexer, 74LS138 decoder/demultiplexer, and 74LS161 binary counter from the Internet. Any manufacturer or variety is acceptable, but your data sheets should include the pin-out for the DIP packages (16-pin DIP packages for all three chips). You should keep these datasheets for use in the experiment after your instructor verifies that you have them. You do not have to turn them in with the rest of your Pre-lab. Helpful tip: the datasheets used in this write-up are at:
   74LS151 1-of-8 Line Data Selector/Multiplexer
   74LS138 3-to-8 Line Decoder
   74LS161 Synchronous 4-Bit Binary Counter

2. Use *Multisim* to create a schematic diagram of an 8-channel TDM communication system with the 74LS151 as the multiplexer, the 74LS138 as the demultiplexer, and a 74LS161 binary counter (similar to the counter used in Experiment 2) as the channel selector.
   - Connect counter outputs QC-QB-QA to the C-B-A selection inputs of the multiplexer and demultiplexer, so that the counter "selects" a channel for transmitting/receiving data. As the counter increments, successive channels should be selected. (The fourth counter output, QD, will be left unconnected.)
   - Connect the 8 demultiplexer outputs to probes and/or a Digital Reader to display the data on the 8 "channels". (In the actual experiment, these will be connected to LED0-LED7 on the ELVIS workstation.)
   - To supply the data to be transmitted, insert a Digital Writer into the circuit and connect its first 7 outputs to multiplexer inputs D0-D6. Connect the 8th multiplexer input to logic 0.

- Connect the 8th Digital Writer output to the CLOCK input of the binary counter. Pulses on the CLOCK will increment the counter, thereby selecting channels in sequential order.
- Connect multiplexer output Y to demultiplexer enable signal G2A. This wire is the TDM data signal being transmitted from the multiplexer to the demultiplexer.
- Connect all other multiplexer and demultiplexer enable inputs to constant values corresponding to their active levels (to enable these modules).
- Connect the ENABLE inputs (ENABLE P, ENABLE T) to their active levels (logic 1) to enable counting, and connect the LOAD and CLEAR inputs to their inactive levels (logic 1) to disable the corresponding functions.
- Connect the counter parallel inputs D-C-B-A to logic 0. (These will not be used.)

After you've drawn the schematic diagram, simulate and test the operation of the communication channel. The counter will select one channel on the multiplexer and demultiplexer. With a particular channel N selected, verify that data is transmitted on that channel by using the Digital Writer to toggle the value of multiplexer input N and verifying that those values appear on output N of the demultiplexer (on the attached probe); all other demultiplexer outputs should be in their inactive states. Then pulse the counter CLOCK signal to increment the count, selecting the next channel (a count of 111 will roll over to 000 on the next CLOCK). Again verify that changes to the selected multiplexer input appear at the corresponding demultiplexer output. Repeat for the other 5 channels (note that the data input to channel 7 has been tied to 0, so you will not be able to change that.) Print out your *Multisim* circuit and include it as part of your Pre-lab.

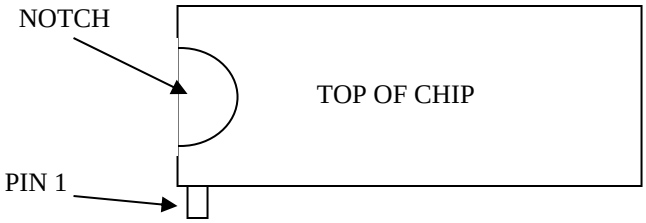
3. The sheet attached to the end of this write-up contains the chip package diagrams of the multiplexer, demultiplexer and counter chips, plus the Digital Writer, 8 LEDs, and the ELVIS +5V and GROUND connections. On this sheet, using your *Multisim* schematic as a guide, create a wiring diagram for your experiment to use as a reference for wiring your circuit on the ELVIS workstation, i.e. draw all wires between component pins and devices. ***Note that* Multisim *does not explicitly show power (VCC) and ground connections on the logic symbols of the chips. You must ensure that you have properly connected each of the chip VCC pins to the +5V power supply terminal on ELVIS, and each of the chip ground pins to the GROUND terminal on ELVIS.***

IV. Lab Exercise

You will use the following equipment and components:

- ELVIS workstation
- A tub of hookup wires.
- If any of these are missing or non-functional, let your lab instructor know.
- The three TTL components listed in the table below.

Qty	Part # or value	Description	Instructions
1	74LS151, 16-pin DIP	8-input multiplexer (MUX), TTL	Identify pin 1 (see drawing)
1	74LS138, 16-pin DIP	3–8 decoder, TTL	Identify pin 1 (see drawing)
1	74LS161, 16-pin DIP	4-bit binary counter, TTL	Identify pin 1 (see drawing)



STEP 1. Connect the 74LS161 4-bit counter and verify correct operation.

Refer to the wiring diagram created in Pre-lab Step 3 and your *Multisim* schematic.

(a) Make the connections listed in Table 2.

(b) To test the counter, outputs QC-QB-QA should be connected to LED2-0 as indicated. You will disconnect the LEDs and connect the counter outputs to the multiplexer and demultiplexer later.

(c) Verify correct operation of the 74LS161 using the Digital Writer to pulse the counter's clock input, verifying the proper counting sequence on the LEDs. Note that the count should roll over from 111 to 000.

Table 2. Connection list for the 74LS161. Active LOW I/O pins are shown with an asterisk (*)

Pin	Label	Function	Connect to	Notes
16	VCC	Power	+5 V	
8	GND	Ground	Ground	
1	CLEAR*	Asynchronous clear	+5V	Disable clear function
2	CLOCK	Clock	Digital I/O DIO7	Use Digital Writer to produce clock pulses
3-6	A-B-C-D	Data inputs	Ground	
7	ENABLE P	Enable	+5V	Enable counting
9	LOAD*	Asynchronous load	+5V	Disable load function
10	ENABLE T	Enable	+5V	Enable counting
11	QD	Count output (bit 3)	Not connected	
12	QC	Count output (bit 2)	LED2	Select channel 0-7
13	QB	Count output (bit 1)	LED1	
14	QA	Count output (bit 0)	LED0	
15	RIPPLE	Ripple carry out	Not connected	

Before proceeding, have your GTA check off Step 1 on your checklist.

STEP 2. Connect the 74LS151 8-input multiplexer and verify correct operation.

Refer to the wiring diagram created in Pre-lab Step 3 and your *Multisim* schematic.

(a) Make the connections listed in Table 3.

(b) To test the multiplexer, output Y should be connected to LED7 as indicated. You will disconnect the LEDs and connect the multiplexer output to the demultiplexer input in Step 3.

(c) Verify the correct operation of the 74LS151 by using the Digital Writer to toggle the value of multiplexer input N, and verify that this value appears on the LED connected to multiplexer output Y, where N is the multiplexer input selected by the counter. Pulse the

counter CLOCK signal and repeat for each of multiplexer channels 0-6. Record your input values and the observed outputs in a table in your report.

Table 3. Connection list for the 74LS151. Active LOW I/O pins are shown with an asterisk (*)

Pin	Label	Function	Connect to	Notes
16	VCC	Power	+5 V	
8	GND	Ground	Ground	
4-1, 15-13	D0-D3, D4-D6	Data inputs 0-6	Digital I/O DIO0-DIO3, DIO4-DIO6	Data to be transmitted from Digital Writer
12	D7	Data input 7	Ground	Constant 0 data
11	A	Data select (LSB)	Counter output QA	These three inputs select the data input to be transmitted.
10	B	Data select	Counter output QB	
9	C	Data select (MSB)	Counter output QC	
7	STROBE*	Enable signal	Ground	
5	Y	Multiplexer output	LED7	Transmitted signal
6	W	Multiplexer output (inverted)	No connection	

Before proceeding, have your GTA check off Step 2 on your checklist.

STEP 3. Connect the 74LS138 decoder/demultiplexer and verify correct operation.

Refer to the wiring diagram created in Pre-lab Step 3 and your *Multisim* schematic.

(a) Disconnect the LEDs from steps (2) and (3) and make the connections listed in Table 4.

(b) Verify the correct operation of the 74LS138 and the digital communication system by using the Digital Writer to toggle the value of multiplexer input N, and verify that this value appears on the LED connected to the corresponding demultiplexer output, where N is the multiplexer input selected by the counter. Then use the Digital Writer to pulse the counter CLOCK, selecting the next channel, and again verify that data changes on the selected multiplexer input appear on the corresponding demultiplexer output. Repeat for the other multiplexer/demultiplexer channels. Record your input values and the observed outputs in a table in your report.

Table 4. Connection list for the 74LS138. Active LOW I/O pins are shown with an asterisk (*)

Pin	Label	Function	Connect to	Notes
16	VCC	Power	+5 V	
8	GND	Ground	Ground	
6	G1	chip is enabled when G1 is high, G2A is low, and G2B is low	+5 V	
4	G2A*		Multiplexer output Y	This will be "data" input.
5	G2B*		Ground	
3	C	Data select (MSB)	Counter output QC	These three inputs select the output to be toggled.
2	B	Data select	Counter output QB	
1	A	Data select (LSB)	Counter output QA	
Pins 15-9, 7	Outputs Y0*-Y6*, Y7*	Outputs	LED0-LED7	All outputs are active low.

Before proceeding, have your GTA check off Step 3 on your checklist.

<u>STEP 4.</u> Cleanup.

DO NOT PUT RESISTORS, CAPACITORS, CHIPS, OR ANY OTHER COMPONENTS IN THE WIRE TUBS.

(a) Turn off the power to the ELVIS base and board.
(b) Disassemble your circuit and place all wires back in the wire tub.
(c) Put all chips and other components back in the proper bins.
(d) Clean up your workstation and discard any trash.

Have your GTA inspect your workstation and check off cleanup on your checklist if acceptable.

PRE-LAB WIRING DIAGRAM