ELEC 5200/6200 (Fall 2021)
Homework 5
Assigned 10/20/21, due 10/29/21
(58 points possible)

Problem 1: Read the article (*Communications of the ACM*, volume 59, number 3, pp. 40-45, March 2016) in which David Patterson (an author of your textbook) interviews John Hennessey (the other author of textbook). Then write an opinion in 3-4 sentences on what you think is the most significant idea that Hennessey expresses about computer architecture. The article is available on the Canvas course website (attached to the homework assignment, look for the file p40-patterson.pdf). (4 points)

One thing to note is he expresses that hardware will be super cheap and software is where money will lie. He talks about machine learning and its future, this is significant because AI has grown so much in so little time and is extremely valuable. He also talks on how hardware is slightly slowing down while software is ramping up!

Problem 2: Consider a chip manufacturer that can construct functional units with the following combinational delays:

Memory read or write	1.2ns
Register file read and write	500ps
ALU	750 ns

You may assume that the delay of other hardware units in a datapath is negligible. A customer would like to run a custom software application with the following with the following instruction mix:

R-type: 45% Branch: 18% Load: 22% Store: 15%

a. Should you recommend that the customer use the single cycle or multicycle datapath design studied in class? Empirically justify your answer. (5 points)

Single Cycle is faster

Multi CPI = $0.45(4) + 0.18(3) + 0.22(5) + 0.15(4) = 4.04$

multi cycle time = 1.2ns

Single CPI = 1

Single time = $0.5 + 0.75 + 1.2 + 0.5 = 2.95$ ns

Ratio = $\frac{1 \times 2.95\text{ns}}{4.04 \times 1.2\text{ns}} = 0.604$

b. Assume your customer increases your development budget. You can either purchase an optimizing compiler which makes much better use of memory, reducing the percentage of loads and stores and thereby providing an instruction mix of:

R-type: 62%	Branch: 18%	Load: 10%	Store: 10%

or you can license a third-party memory design which has a latency of 2/3 your in-house memory design. However, you can only afford to do one. How does this impact your choice of datapath design and which improvement should you go with to get the best performance? Empirically justify your answer. (8 points)

Optomize Compiler

multi CPI = $0.62(4) + 0.18(3) + 0.10(5) + 0.15(4) = 4.12$

Ratio = $\frac{1 \times 2.95ns}{4.12 \times 1.2ns} = 0.597$

3rd party mem

multi CPI = 4.04

multi Time = $\frac{2}{3} \cdot 1.2ns = 0.8ns$

Single Time = $0.5 + 0.75 + 0.8 + 0.5 = 2.85\ ns$

Ratio = $\frac{1 \times 2.55ns}{4.04 \times 0.8ns} = 0.789$

Chose 3rd party Mem since performance is improved still single cycle Datapath

Problem 3: Assume that a pipeline register and the program counter each have a delay of 100ps. Time taken by other major hardware units in a RISC-V processor are:

Memory read or write	800ps
Register file read and write	450ps
ALU	1ns
Add unit	1ns

All other hardware, including the control and multiplexers, have negligible delays. Then,

a. What is the maximum clock frequency for a five-stage RISC-V pipeline datapath? (2 points)

Pipeline should accommodate longest hardware unit

$$\text{max clock freq} = \frac{1}{(\text{ALU+Reg})} = \frac{1}{(1\times10^{-9} + 100\times10^{-12})} = 9.09\times10^{8}\ \text{Hz}$$

b. Neglecting any hazards and resulting stalls, what are the pipeline latency (in units of time) and the cycles per instruction (CPI) for a long instruction sequence? (2 points)

latency is 5 clock cycles

$5 \times 1.1\text{ns} = 5.5\text{ns}$

CPI = 1 assuming no stalls

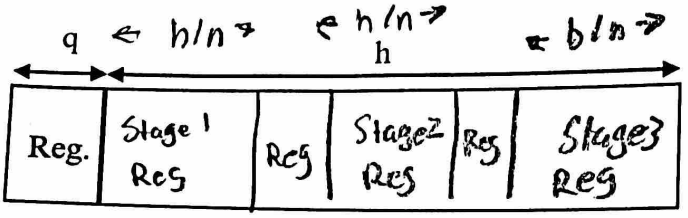
c. Compare this datapath with a single cycle RISC-V datapath using similar hardware: (10 points)

$800\text{ps} + 450\text{ps} + 1\text{ns} + 800\text{ps} + 450\text{ps} + 100\text{ps} = 3.6\text{ ns}$

Datapath	Clock cycle time	Clock frequency	CPI	Time per instruction	Million instructions per second (mips)
Single-cycle	3.6ns	2.78×10^{8} Hz	1	3.6 ns	278
Pipeline	1.1ns	9.09×10^{8} Hz	1	1.1ns	909

Note: Show your work!

Problem 4: Consider a single-cycle datapath as a one-stage pipeline. It consists of combinational and asynchronous circuitry and a single clocked register, the program counter (PC). Its total cycle time consists of an interval q required by the register and an interval h used by the rest of the circuitry:



(a) Assume that the delay h can be partitioned into n equal delay hardware stages separated by clocked registers each having a delay q, the first stage register being the PC. Neglecting the latency and any hazard penalties, compute the average execution time of an instruction by this n-stage pipeline. (2 points)

Total time by combinational and asynchronous circuit is h. Equally among n number of stages.

Each stage requires time q for pipeline register.

Cycletime of n-stage pipeline = $q + h/n$

this is also execution time per instruction

if we ignore latency + hazards

(b) Show that the performance limit for the pipeline when we neglect the latency and hazards is determined by the register delay q. Find the upper bound on the clock frequency for this pipeline datapath. (2 points)

Pipeline will reduce as number of stages increase.

If $n = \infty$ and cycle time of execution time of an instruction is q

Clock freq is $\frac{1}{q}$ Hz

(c) For the n-stage pipeline, suppose the average hazard penalty is $\alpha(n-1)$ cycles per instruction, where $0 < \alpha < 1.0$ and $n \geq 1$. Derive an equation for the optimum number of pipeline stages. (3 points)

$t = (q + \frac{h}{n})(1 + \alpha n - \alpha) = q + q\alpha n - q\alpha + \frac{h}{n} + \alpha h - \frac{\alpha h}{n}$

(d) Assume a circuit design where $h = 4 \times q$ and an ISA where $\alpha \approx 0.1$. What is the optimum number of stages for this pipeline and what is the corresponding speed up over a single-cycle datapath? (3 points)

Optimum Stages $n = \left[\frac{4(1-0.1)}{(0.1)}\right]^{1/2} = 6$

6 stage execution time $= (q + \frac{3q}{6})(1 + 0.1 \times 6 - 0.1) = 2.25q$

Single cycle $= h + q = 4q + q = 5q$

Pipeline to single cycle ratio $= \frac{5q}{2.25q} = 2.22$

(e) For q = 90ps, tabulate clock cycle time, clock rate, average CPI (include hazard penalty, if any) and performance in million instructions per second (mips) for single-cycle datapath and the pipeline datapath with optimum number of stages found in (d). (8 points)

Datapath	Cycle time	Clock frequency	Av. CPI	mips
Single-cycle	450ps	2.2GHz	1	2222
Pipelined	150ps	6.76Hz	1.5	6667

Problem 5: The following RISC-V instruction sequence is executed on a 5-cycle pipeline datapath, implemented with hazard detection and forwarding units.

```
lw    x5, 0(x6)
sub   x19, x5, x18
lw    x29, 4(x19)
add   x19, x29, x18
```

How many bubbles, if any, will be required this instruction sequence? (2 points) Can a compiler improve the performance? (1 point)

there should be 2 bubbles

b/c write afte read hazard on reg x19

Yes, a compiler can improve performance b/c it will eliminate write after read dependency

Problem 6: A program consists of two nested loops, with a branch instruction at the end of each loop and no other branch instruction anywhere. The outer loop is executed 15 times and the inner loop 25 times. Determine the prediction accuracy percentage for the following three prediction strategies:

(a) always predict branch not taken, (2 points)

inner loop ex = 15 x 25 = 375 times

360 times branch is taken, 15 times not taken

outer loop executed 15 times, taken 14 times, 1 not taken

374 wrong predictions $\frac{16 \times 100}{390} = 4.1\%$

(b) always predict branch taken, (2 points)

16 wrong predictions

$$\frac{374 \times 100}{390} = 95.9\%$$

(c) use a 1-bit history buffer initialized to the "taken" state for each branch instruction when executed for the first time. (2 points)

1 wrong prediction outer loop

29 wrong in inner loop

total of 30 wrong predictions

$$Acc = \frac{360 \times 100}{390} = 92.3\%$$