ELEC 2210 LABORATORY REPORT COVER PAGE

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Meeting # 002 Experiment 1: Basic Digital Logic CIrcuits

Title of Lab Experiment

Student Name: Howard Jacob, A

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AU 7-character username

GTA: Jonathan

Name of your GTA

Section you are enrolled in: (Circle One): 1 2 3 4 5 6 7 8

Date experiment performed (dd / mm / yy): *27/10/20*

Date report submitted: (dd / mm / yy): *3/11/20*

If you performed this experiment at a time other than your regularly scheduled section meeting:

Section # of the section you sat in on (Circle One): 1 2 3 4 5 6 7 8 Makeup

Name of the GTA who supervised your work: _____

I hereby certify that the contents of this report are true and complete to the best of my ability. The lab work was performed by me exclusively, and this report was written by me exclusively.

Jacob Howard 20/10/20

Student signature Date signed

ELEC-2210
Digital Electronics

FROM: Jacob Howard

TO: Yili “Jonathan” Wang

LAB DATE: 10/27/20

DUE DATE: 11/3/20

LAB SECTION: 002 (Tuesday, 1:00pm-2:50 pm)

EXPERIMENT 10:
CMOS logic

Introduction

This laboratory experiment had objectives mainly related to CMOS. We gained experience regarding CMOS gates and used more complex circuits to construct CMOS transmission gates.

Step 1

This laboratory had 3 different parts. For Step 1, we connected 3 inverters and tested them. We analyzed the outputs of each of the CMOS inverters .We set up the Function Generator so Vdd= 5 V, DC Offset was half of Vdd and a frequency of 500 Hz. We were required to take multiple screenshots of each inverter in the chain. *Figure 1* though *Figure 5* shows the screenshots and are labeled accordingly.

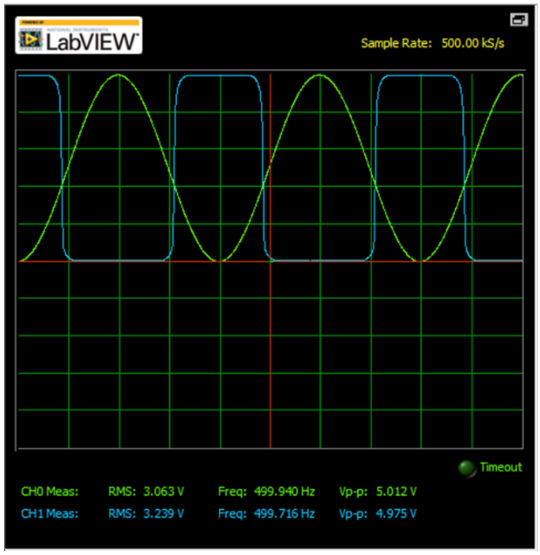

Figure 1 (6-8 input-output)

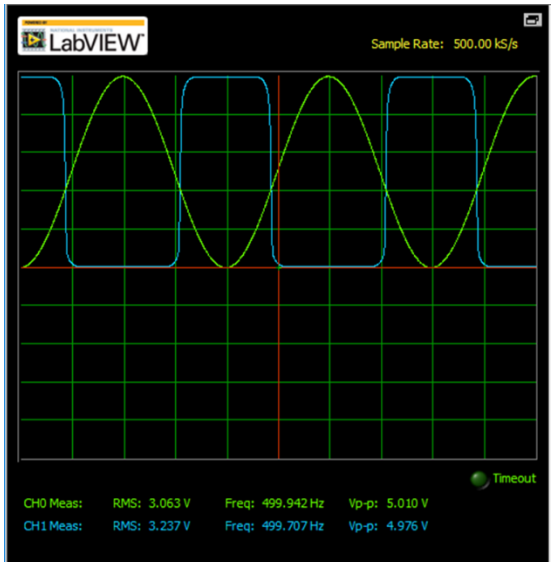

Figure 2 (3-5 input-output)

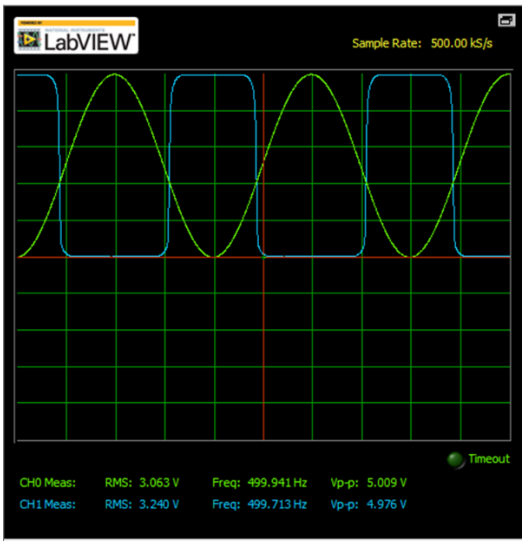

Figure 3 (10-12 input-output)

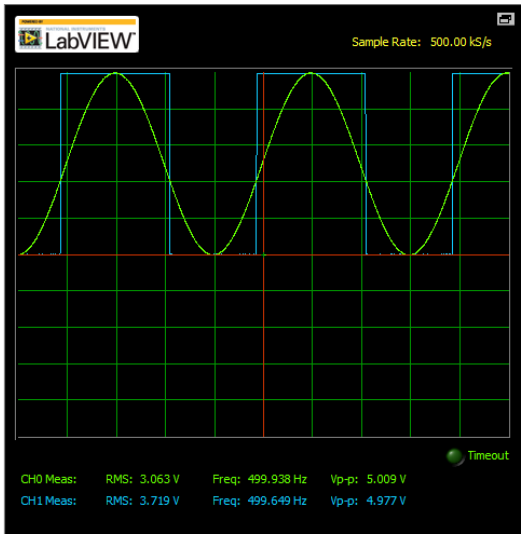

Figure 4 (6-5 input-output)

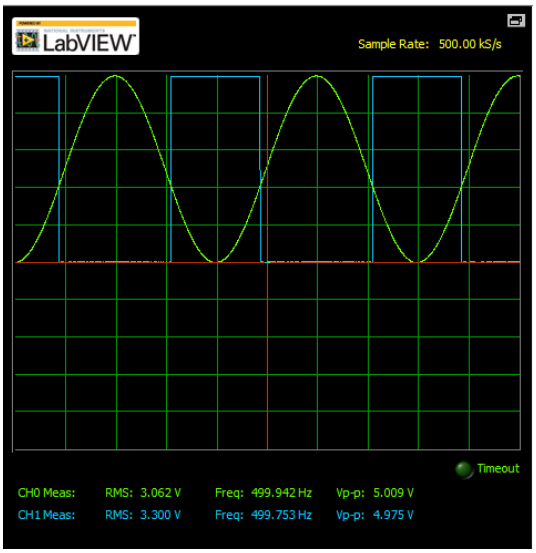

Figure 5 (6-12 input-output)

Step 2

The second part we used a CMOS transmission gate as a multiplexer. In this case we used the oscilloscope to measure the output of the multiplexer when the clock changes from 0 to 1. The screenshots obtained are shown below in *Figure 6* and *Figure 7*.

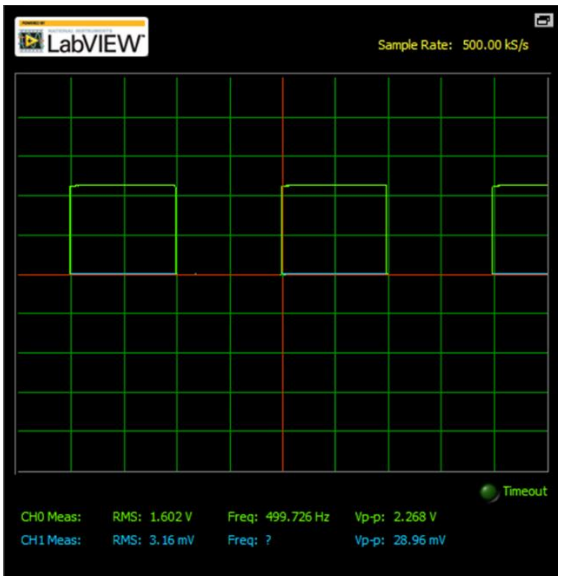

Figure 6

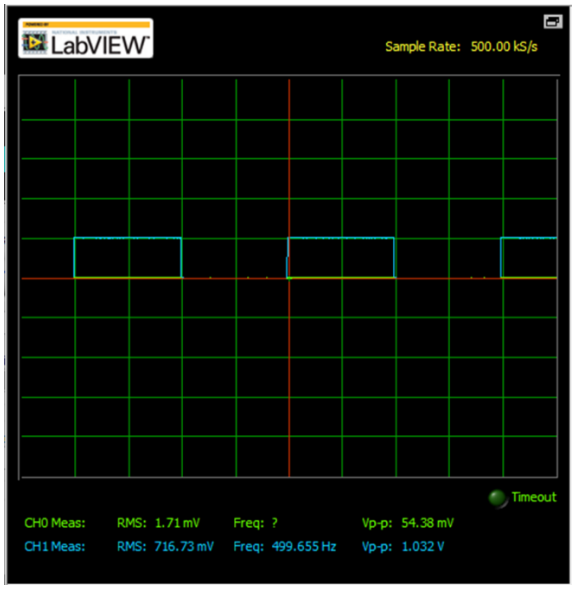

Figure 7

Step 3

Step 3 was related to d-latches. Following the circuit shown in the lab manual it was easy to simulate it in Multisim and obtain the results for when D and CLK varied. When CLK changed from 0 to 1 while D was still 0 nothing happened. Changing D from 0 to 1 without touching CLK would make Q=D. In the case when D=1 and CLK=1 and then D is changed to 0, Q would stay at 1 because Q will only change when the input D is unstable. No screenshots were required for this step. We only had to demonstrate and explain the circuit to the TA.

Conclusion

It is always interesting to apply the material learnt in class into the lab. This lab was very helpful at understanding how the circuits we build work and how they can be constructed in ways to do different things.