

AGENDA

9:30

Session 1: Fundamental Issues with
Concurrency in Embedded Software
Systems from Architectural Point of
View

10:30

10:45

Session 2: Modelling and DSE
Methods for Mixed-Critical Software
Systems using Multicore
Architectures

11:45

12:00

Session 3: Synchronization in
Concurrent Software is an
Architectural Decision

13:00

fortiss

D³SE – Dependency-Driven Design Space Exploration

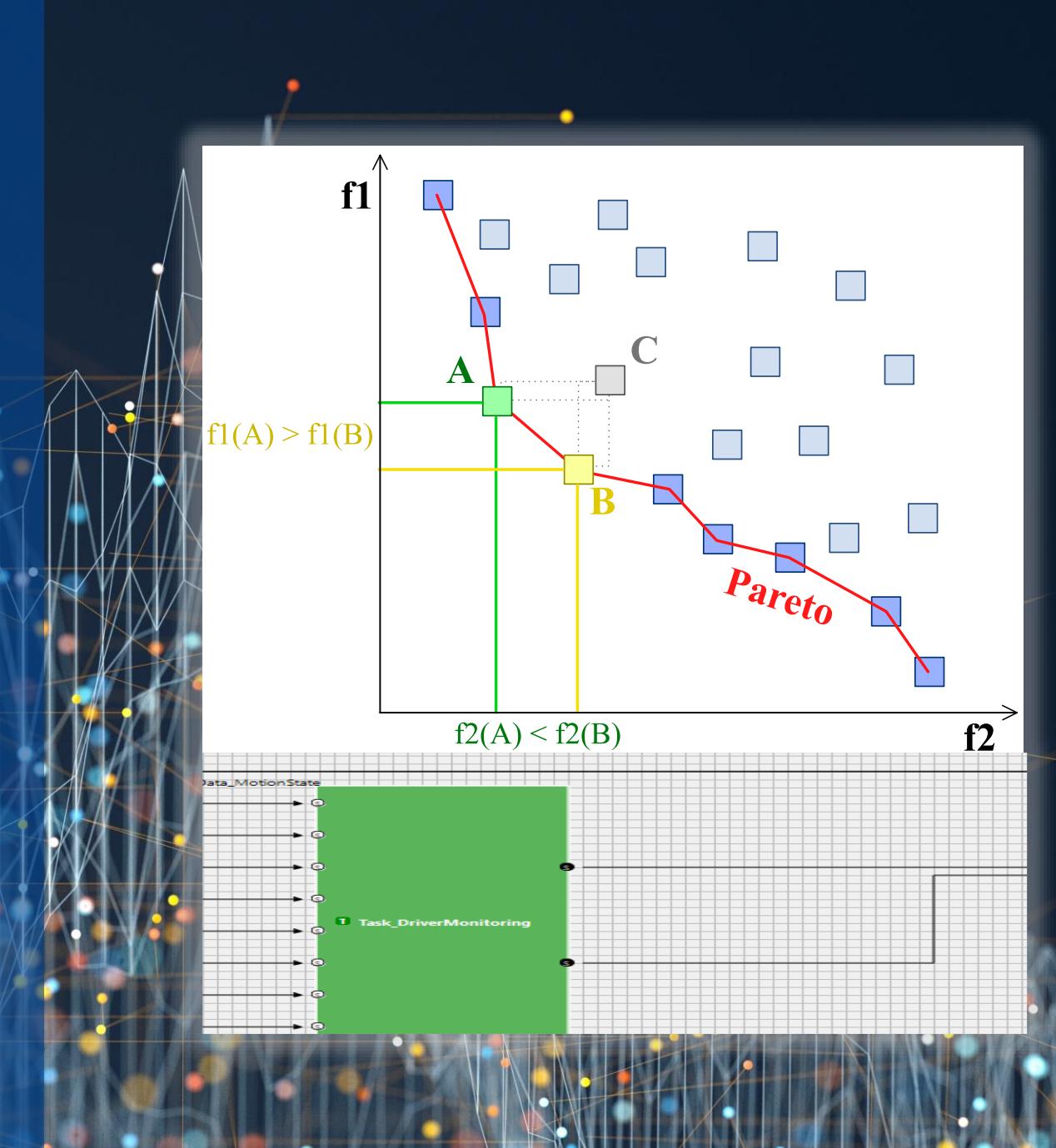
Activity and Artefact-based Optimization
of Distributed Embedded Systems



Alexander Diewald



presented by
Simon Barner



The Systems Engineering Challenge

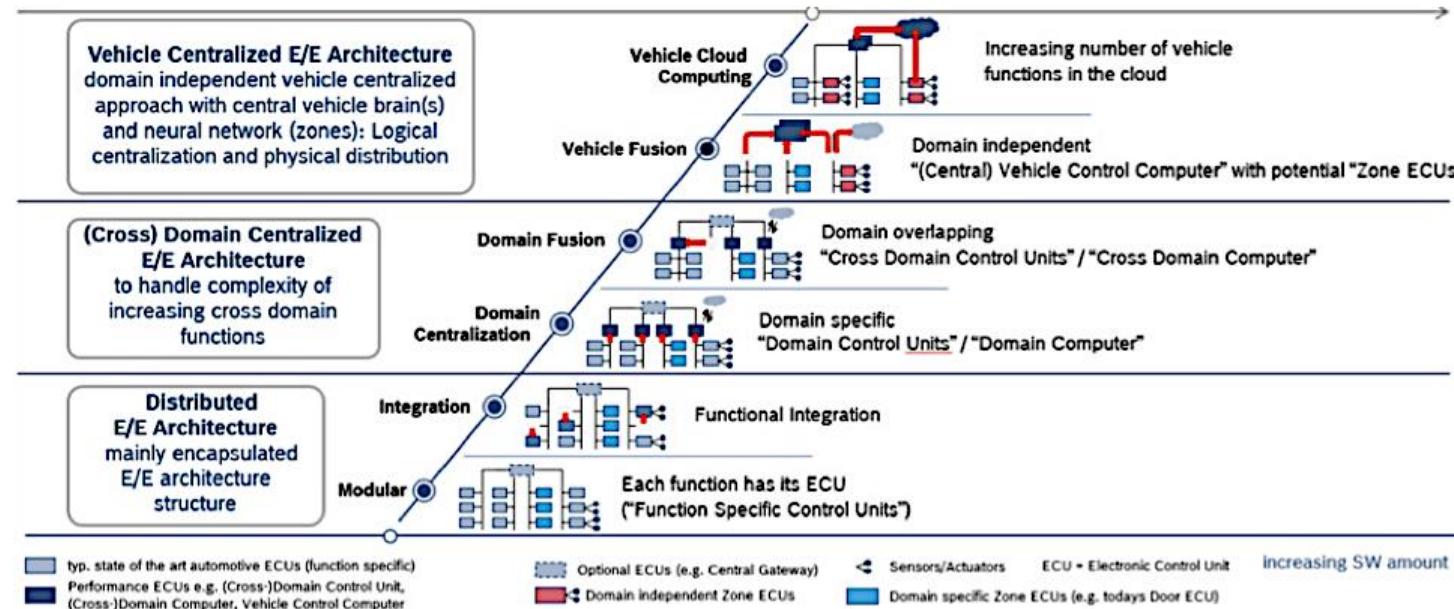
Ever-increasing complexity of software-defined CPS

- ▶ Evolving set of **functionalities**
- ▶ Multitude of **contradicting requirements**
- ▶ Increase in **system variability**
- ▶ **Product-line engineering** and reuse

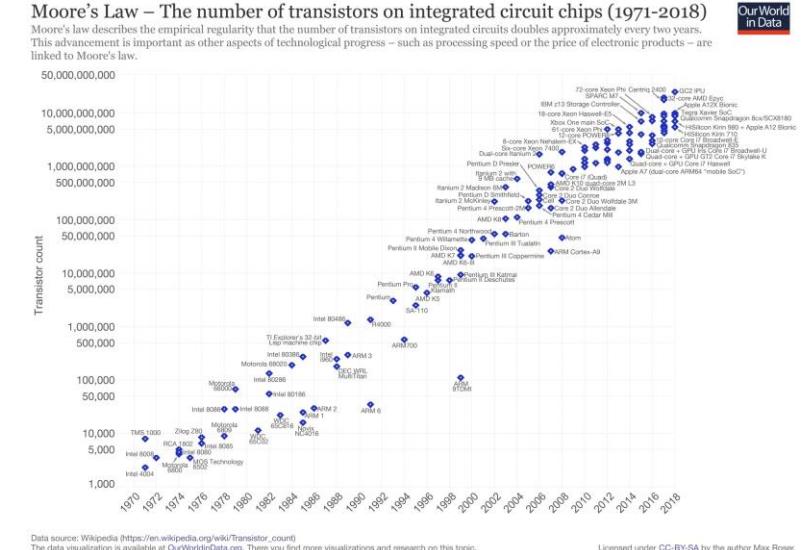


The Systems Engineering Challenge

Complexity of HW/SW platforms



Source: Benckendorff, Tenny, et al. "Comparing current and future E/E Architecture trends of commercial vehicles and passenger cars." 19. Internationales Stuttgarter Symposium. Springer Vieweg, Wiesbaden, 2019.

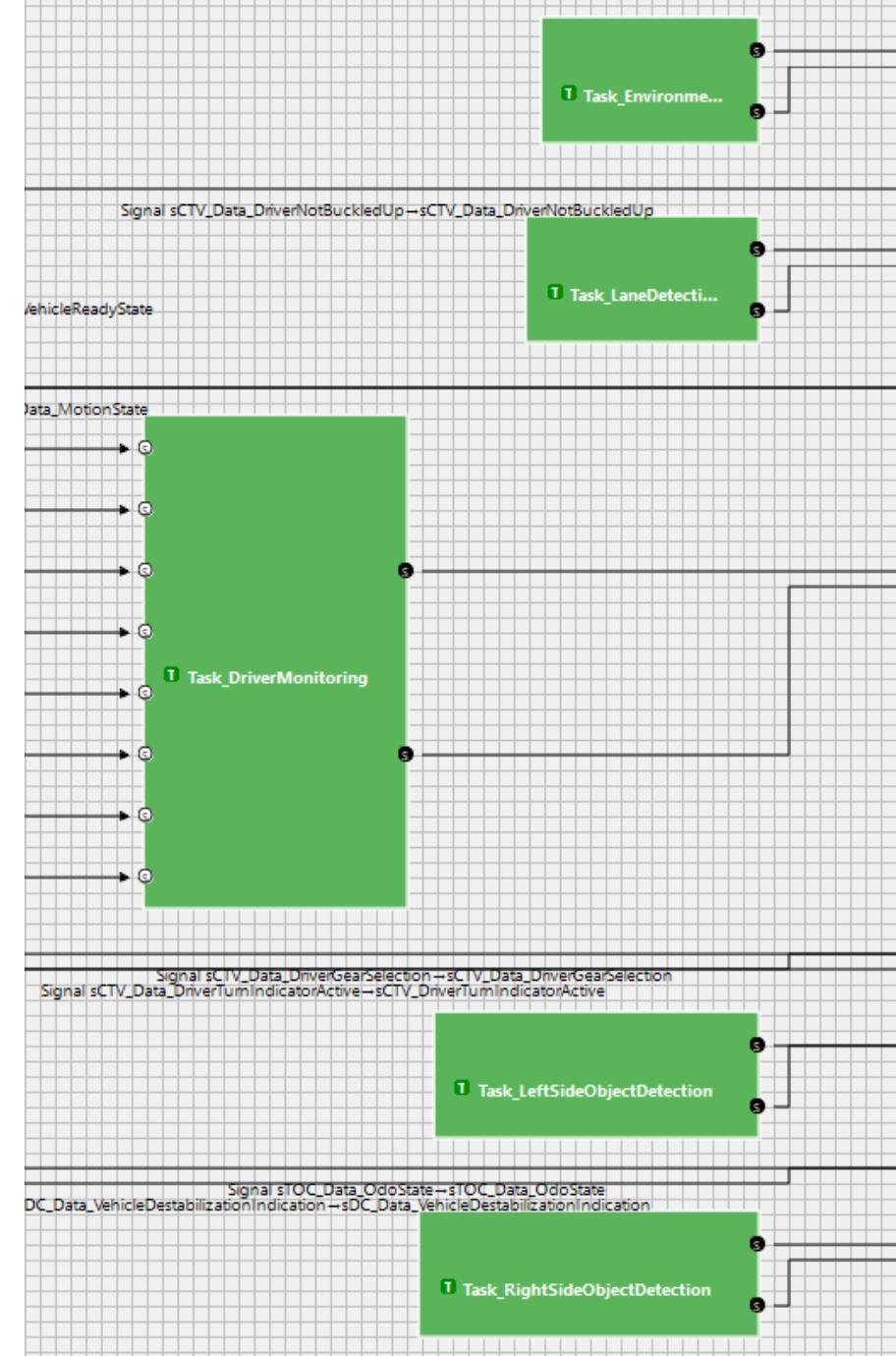


- Increase of software-defined (critical) functions results into massive performance requirements
- Mixed-criticality integration platforms are only a part of the solution & add additional complexity
- **Problem: Now system engineers have to cope with both complexity drivers!**

Example: Real world Traffic Jam Assistant

System level engineering

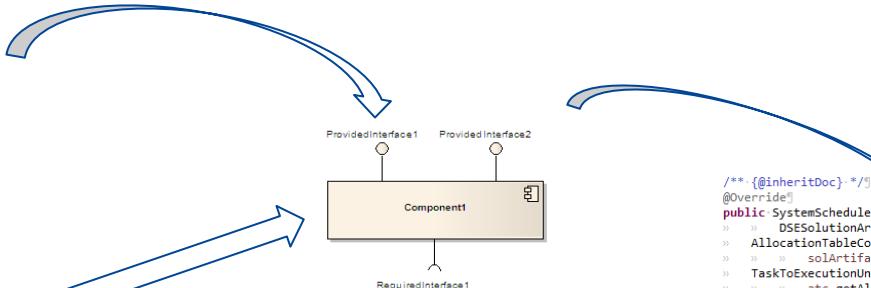
- ▶ # of elements imposes complexity
 - ~30 Tasks
 - ~200 Signals
 - ~10 ECUs
 - ~5 networks
- ▶ Large number of (non-)functional requirements:
 - Separation constraints
 - Temporal constraints (deadlines)
 - ...
- ▶ Source: Waters 2019 Industrial Challenge
(<https://www.ecrts.org/archives/fileadmin/WebsitesArchiv/ecrts2019/waters/waters-industrial-challenge/index.html>)



Can Development Processes beat Complexity?

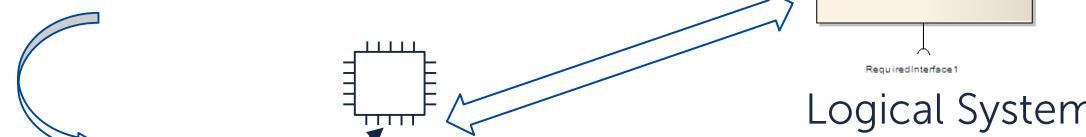
Requirements Allocation Sheet	Functional Flow Diagram Title and No. 2.58.4	Equipment Identification
Function Name	Functional Performance and Guidance	Facility Requirements
2.58.4 Provide Guidance Compartment Cooling	Provide Guidance Compartment Cooling	None
2.58.4.1 Provide Chilled Coolant (Primary)	The temperature in the guidance compartment must be maintained at the initial calibration temperature of +0.3 Deg F. The final calibration temperature of the compartment will be between 46.5 and 48.5 Deg F.	None

Requirements



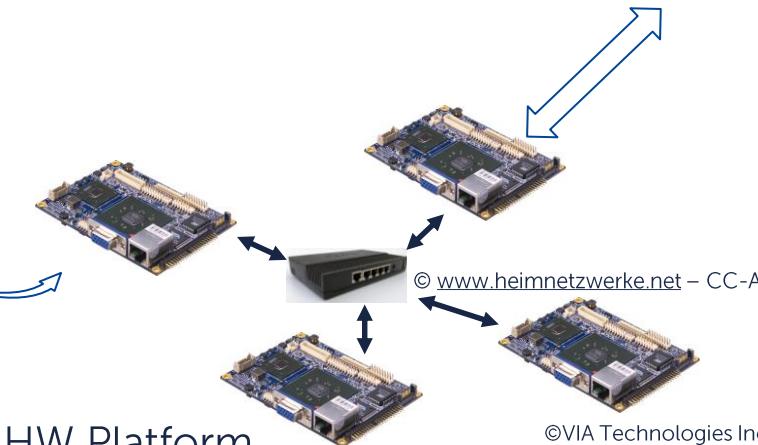
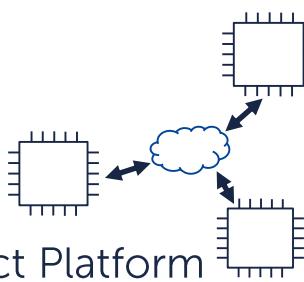
```
/** {@inheritDoc} */
@Override
public SystemSchedule transform(SuperSet<ResourceAllocation> fromSuperSet,
    DSESolutionArtifacts solArtifacts, String basename) {
    AllocationTableCollection atc =
        solArtifacts.getElementOrThrow(AllocationTableCollection.class);
    TaskToExecutionUnitAllocationTable taskToHwTable =
        atc.getAllocationTable(TaskToExecutionUnitAllocationTable.class);
    ...
    SystemSchedule sysSched = createSystemSchedule(basename + " - SystemSchedule");
}
```

Code



Logical System

Abstract Platform

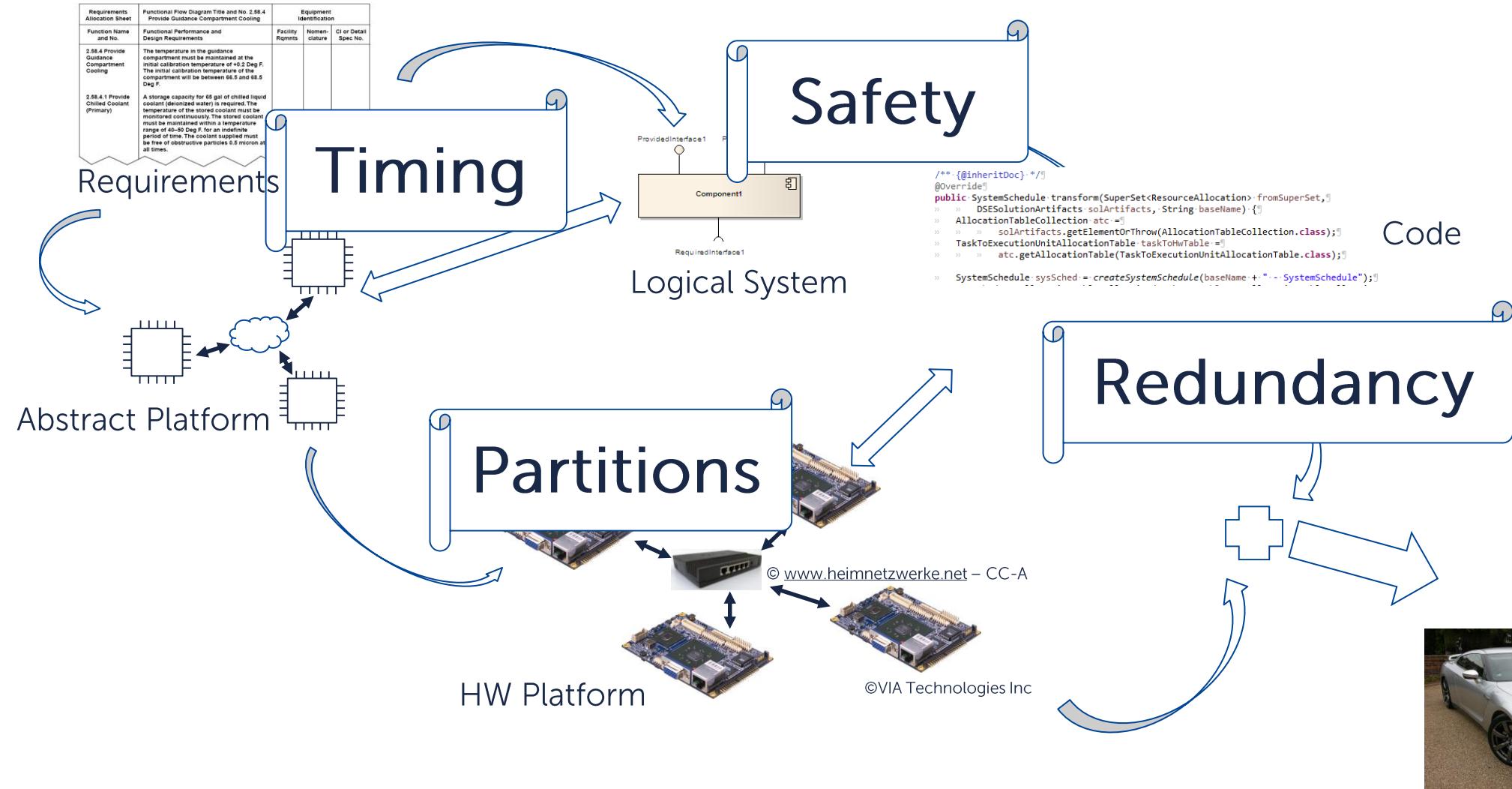


HW Platform

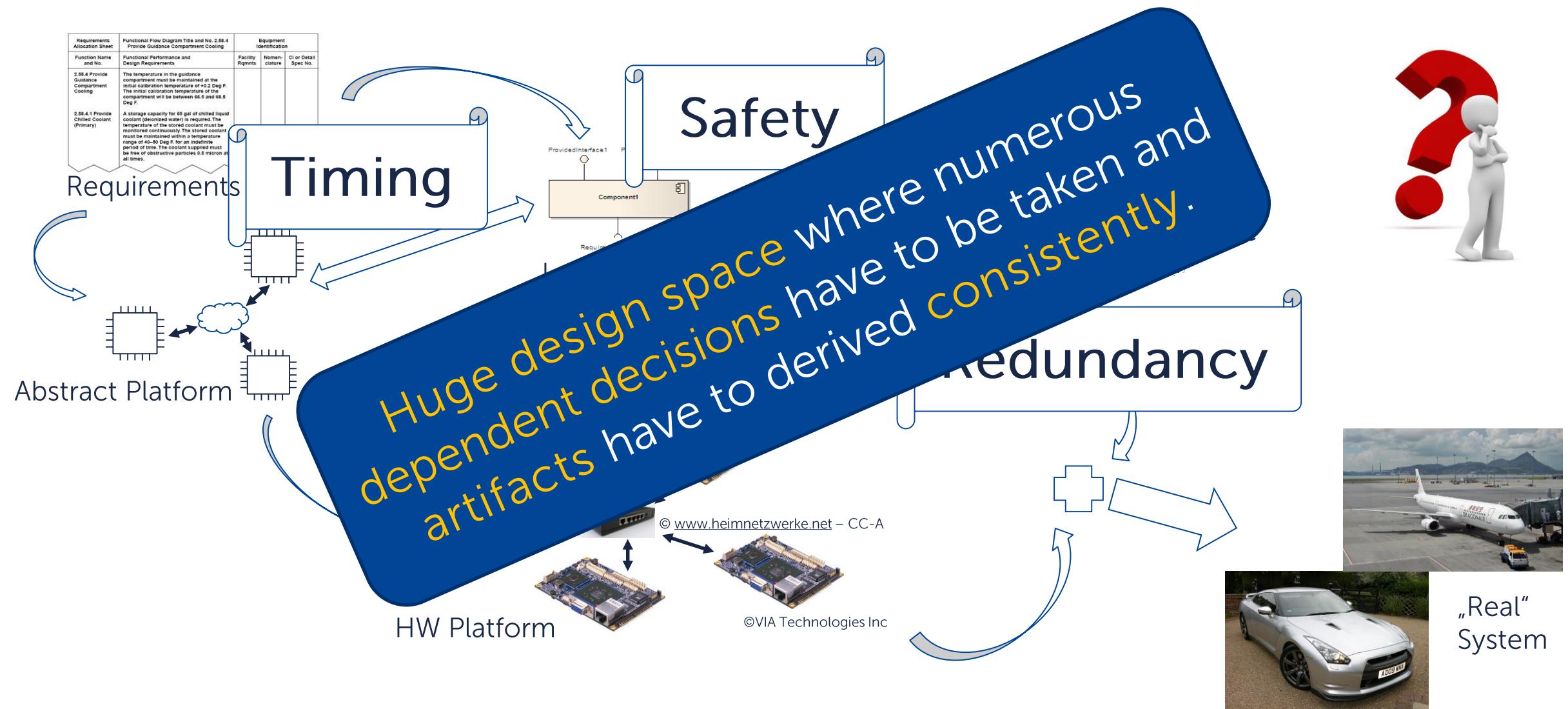


„Real“ System

Can Development Processes beat Complexity?



Can Development Processes beat Complexity?



Can Design-Space Exploration relieve System Engineers?

Needs and suggested approach

- ▶ Compensate complexity of system functionality and platforms
 - Speed-up by means of **design automation**
 - **Frontloading of architectural and design decisions**
 - **What-if analyses**
 - **Decompose decisions** in different layers of the system (SW, HW)
- ▶ **User guidance**
 - Handle dependencies in development processes
 - Meaningful presentation of design-alternatives
 - Take the user into the exploration loop
- ▶ Suggested approach
 - Combination of DSE and Model-based Systems Engineering (MbSE)
 - **Model-based Design-Space-Exploration (MB-DSE)**

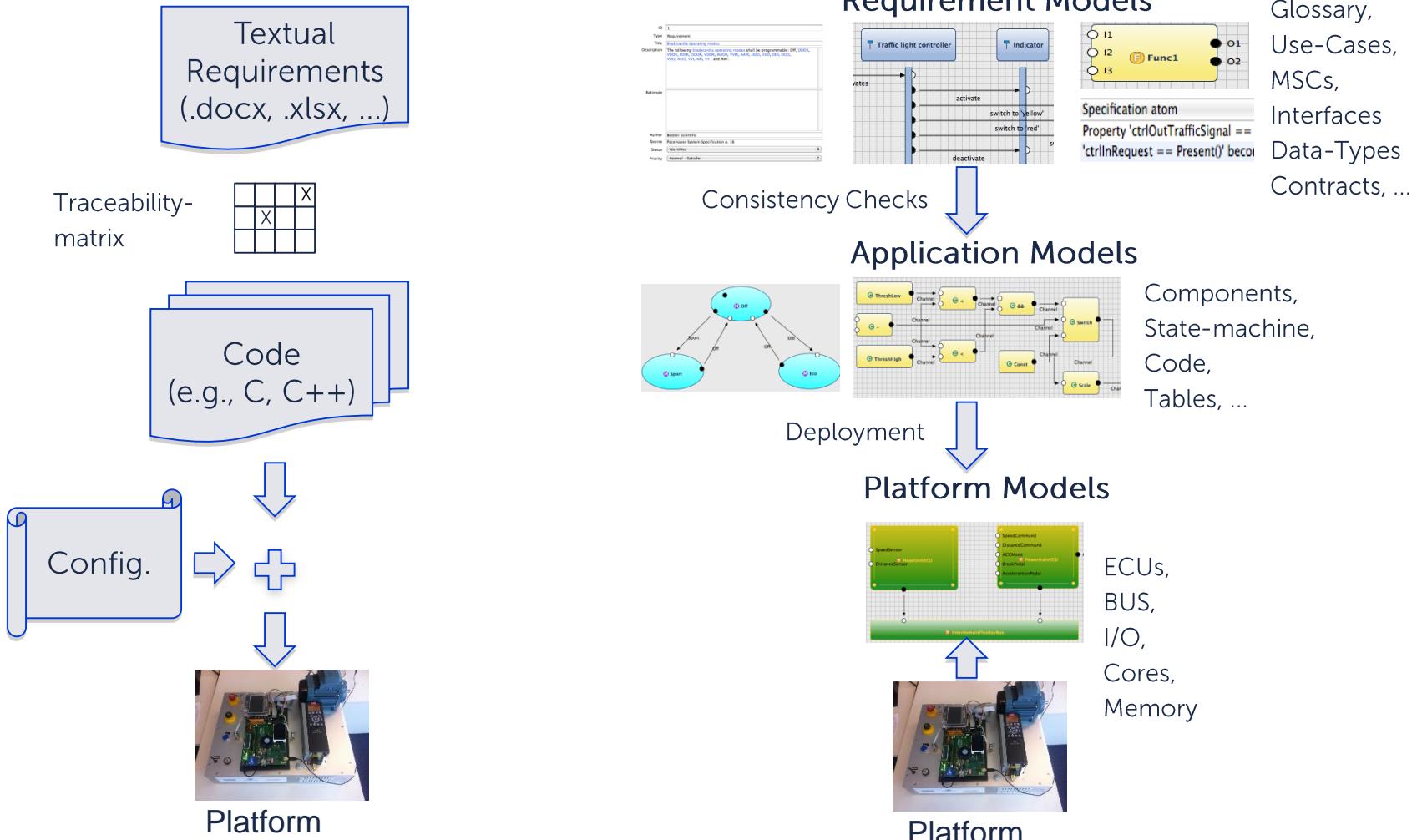


Model-based Design-Space-Exploration

Overview

Why are integrated models needed ?

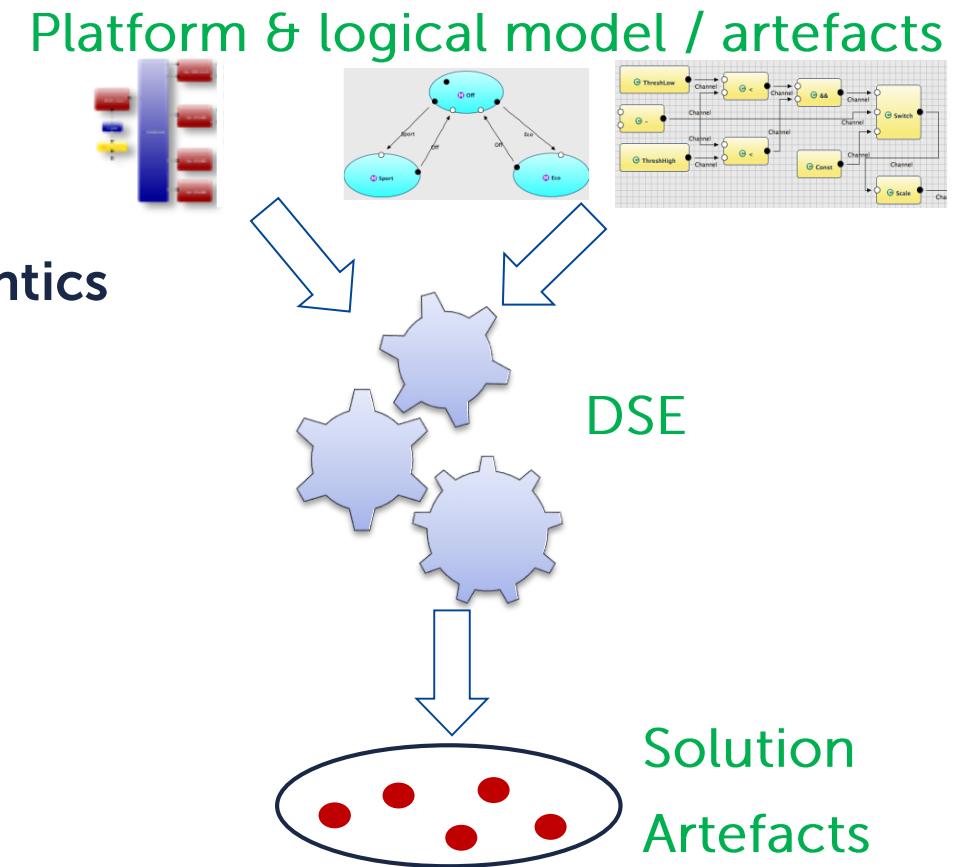
Code-centric vs. Model-Based Development



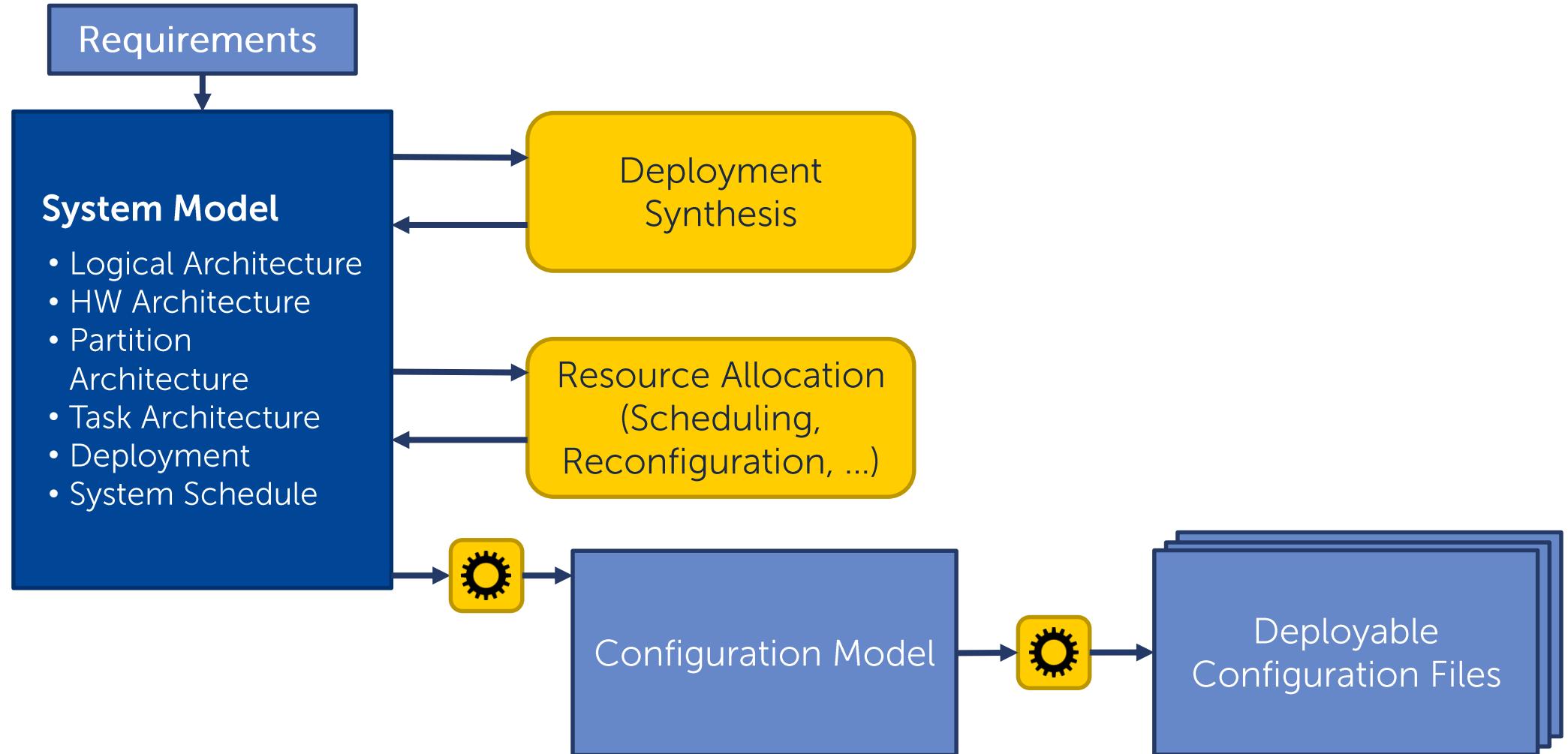
Model-based Design Space Exploration

- ▶ DSE aims at compensating design complexity
 - Automated **exploration of alternatives**
 - Use of **optimization and/or formal methods**

- ▶ MbSE boosts DSE with models that have a strong semantics
 - Validation of user input
 - Evaluation of design alternatives / solution candidates
 - Verification of **constraints**
 - Optimization of **design goals**
 - **Tracking of dependencies** between artefacts
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MB-DSE Engineering Process

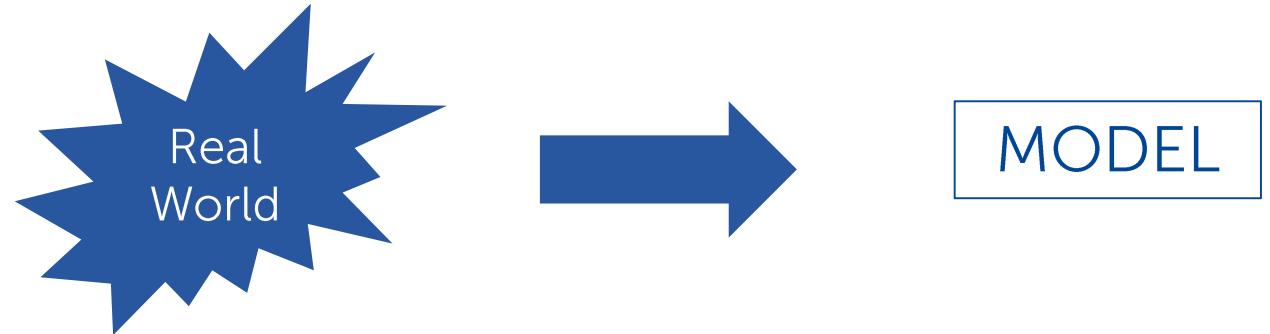


System Model

Modeling Viewpoints and Assumptions

Models and Artifacts

Terminology



„A model is an *appropriate abstraction for a particular purpose*“

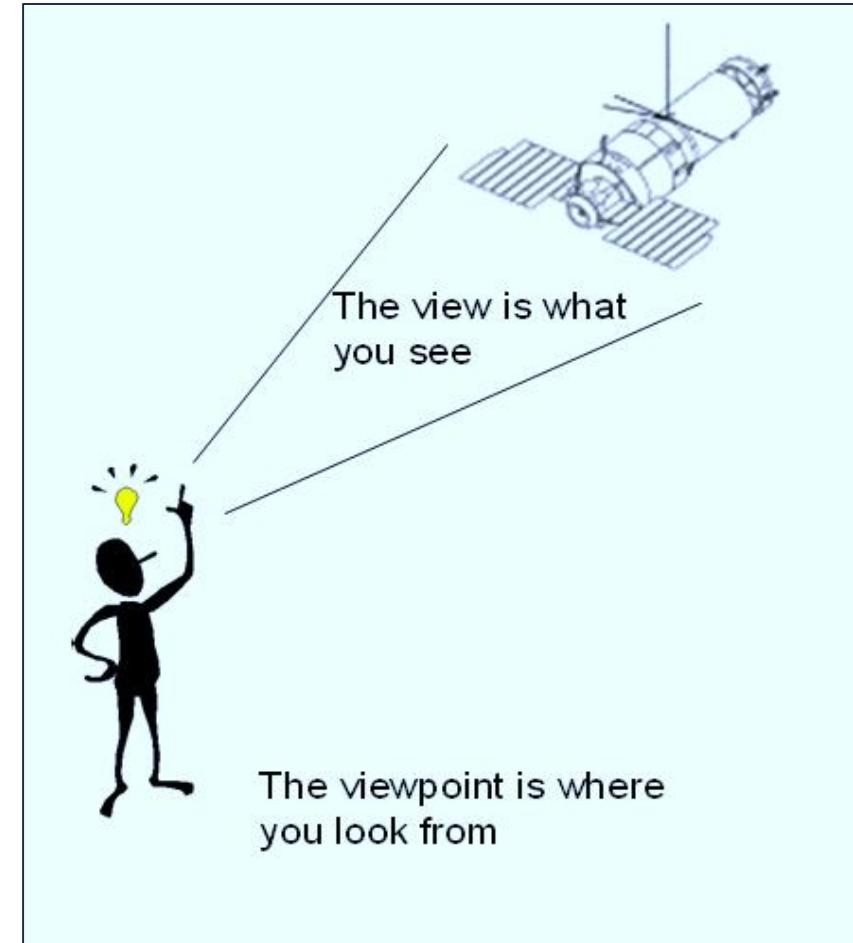
[Broy 2011]

An **artifact** is one of many kinds of tangible (by-)products produced during the development of software.

e.g., use cases, class diagrams, models, requirements and design documents or artifacts concerned with the process of development itself—such as project plans, business cases, and risk assessments.

System Viewpoints and Views

- ▶ A viewpoint reflect the specific interests of dedicated stakeholders and conventions, that enable the generation and analysis of a view
- ▶ These conventions could be languages, notations, model-types, design restrictions or modelling methods, analysis techniques as well as further operations, that can be applied to that view
- ▶ A view is an instance of a certain viewpoint in context to a **specific system**. A view is generated by a set of models that are representing the relevant characteristics.

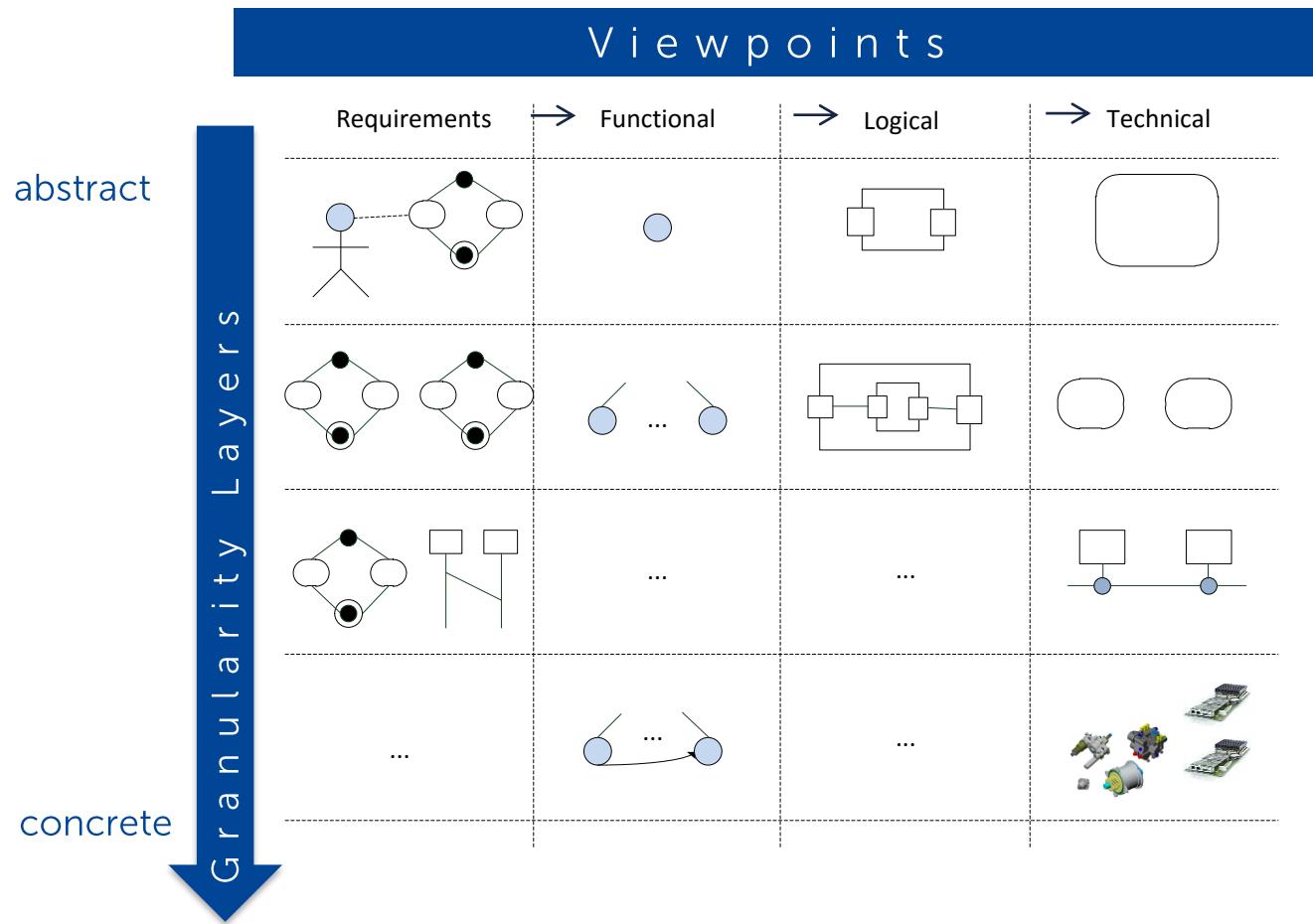


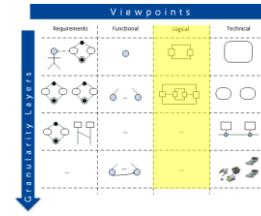
In relation to: IEEE 42010

Systems Engineering Viewpoints

SPES Matrix

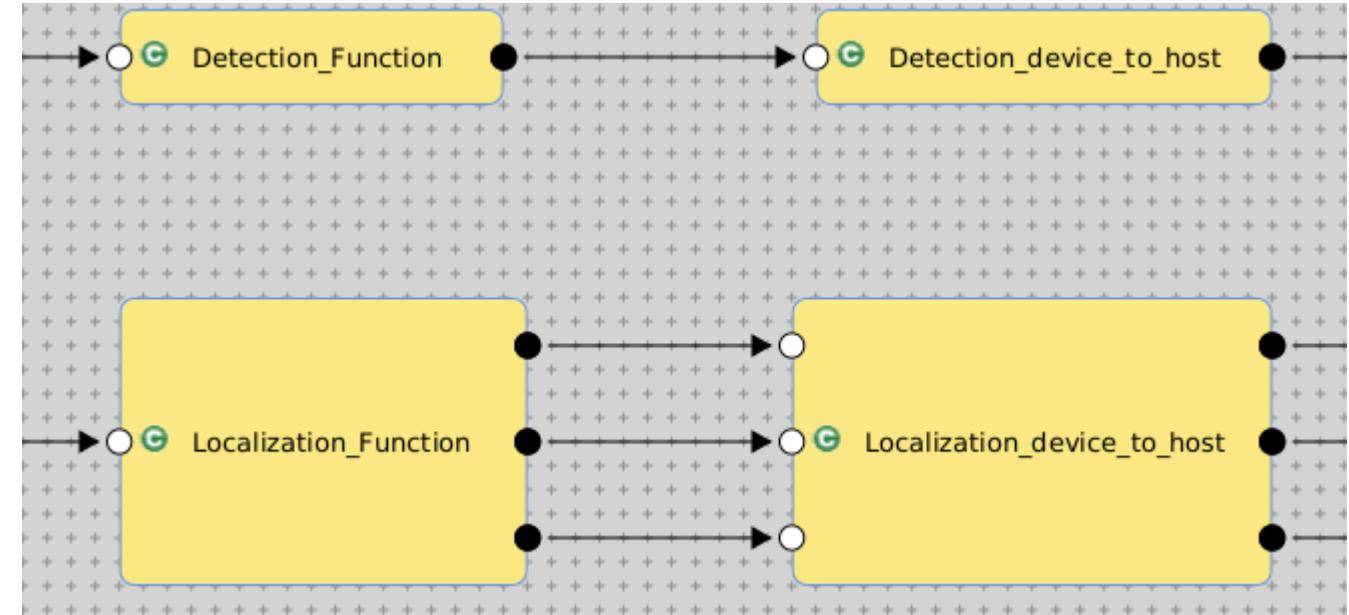
- ▶ Differentiation between **viewpoints** (according to ISO/IEC 42010)
 - ▶ Differentiation by **granularity levels** of a system and its decomposition
 - ▶ **Artefact model** with a well-defined semantic of artifact types and their relation to other artifacts
 - ▶ Overall system properties



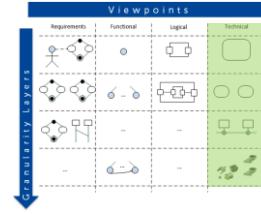


Component Architecture

- ▶ Hierarchical component network
- ▶ Components model behavior (e.g. states)
- ▶ Data transfer by typed ports via channels
- ▶ Components can be distributed on the target platform
- ▶ Agnostic of memory model
 - Shared memory
 - Message passing



Platform Architecture



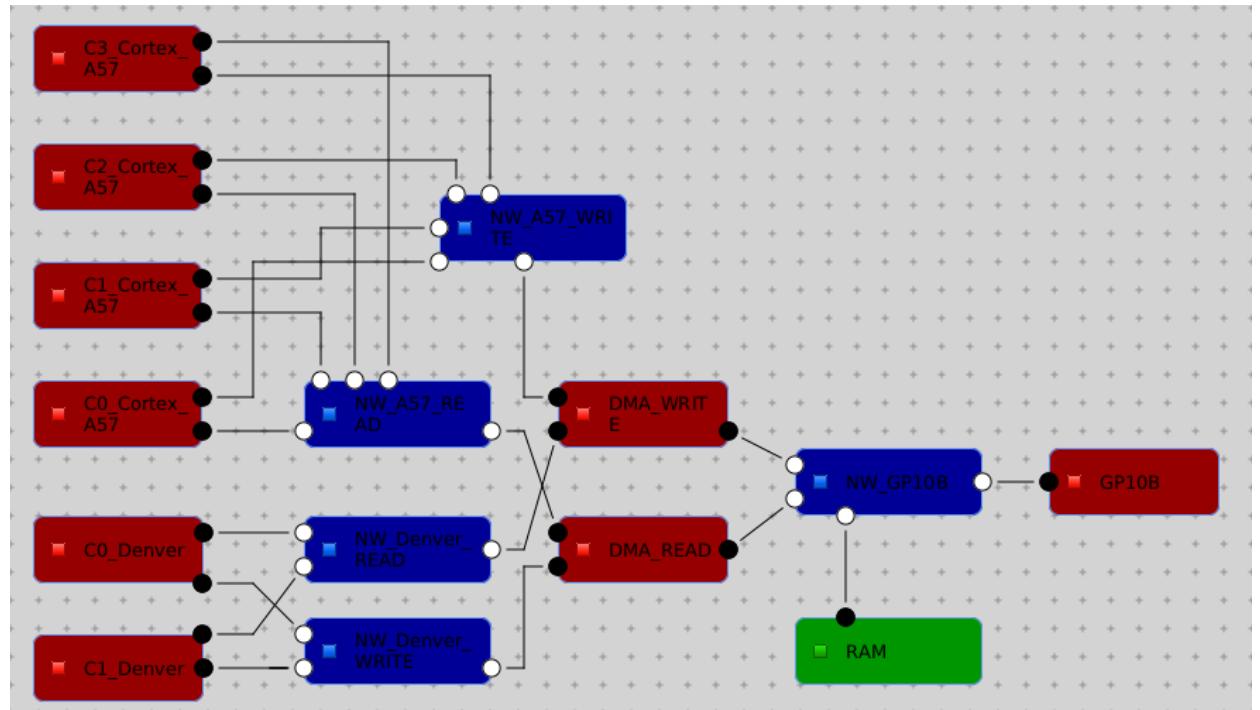
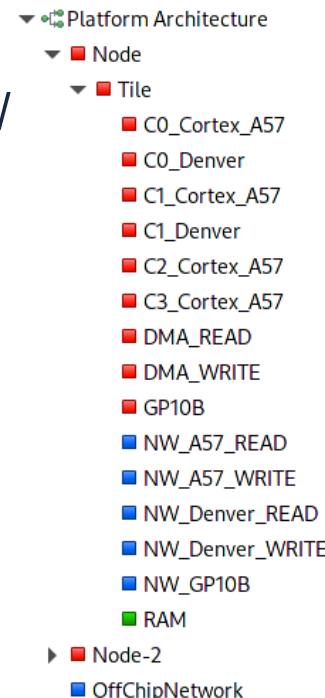
► Hierarchical Platform

► Technical architecture for HW

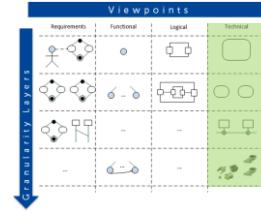
- Distributed systems
- MPSoCs

► Prerequisite to consider non-functional properties

- Safety
- Performance



Task & Partition Architectures



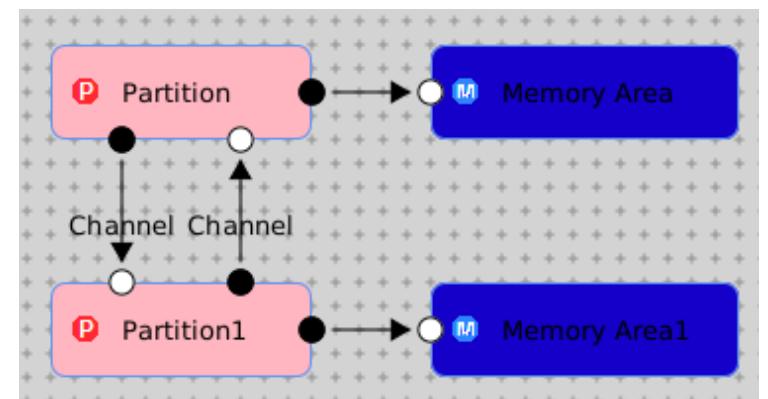
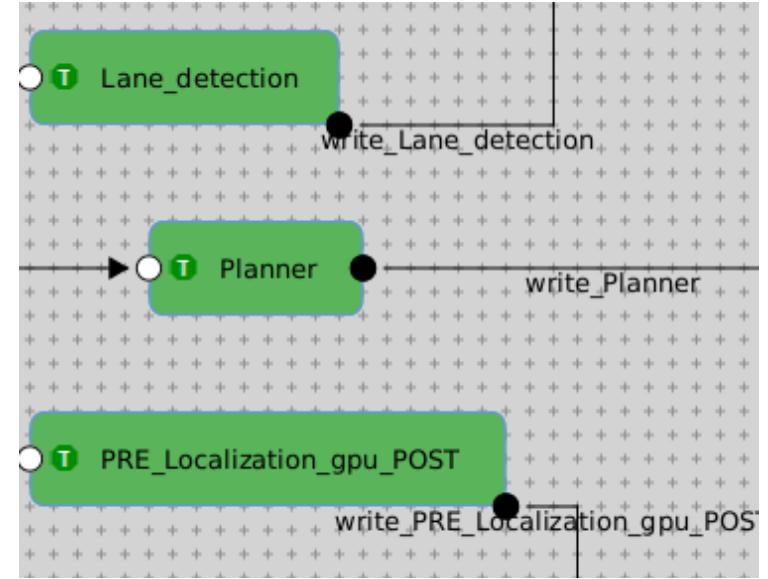
- Flat technical architecture models for system SW

- Task architecture

- Runtime “containers” for (groups of) components
- Defines port semantics (sampling, buffering)

- Partition architecture

- Execution containers for tasks
- Isolation by safety levels



Allocations & Model Element Annotations

- ▶ Allocation Tables model element to element mappings, such as
 - component → task
 - task → execution unit
 - task → memory
 - task → partition → phys. execution unit.
(while multi-layer mapping)

▼ Allocations

- Components → Tasks
- Tasks → Partitions
- Partitions → Hardware

↓ Src. Tgt. →	Head...	PowertrainECU
T Task_&&	☒	
T Task_-	☒	
T Task_<	☒	
T Task_<	☒	
T Task_AccelerationControl	☒	
T Task_Const	☒	
-	-	-

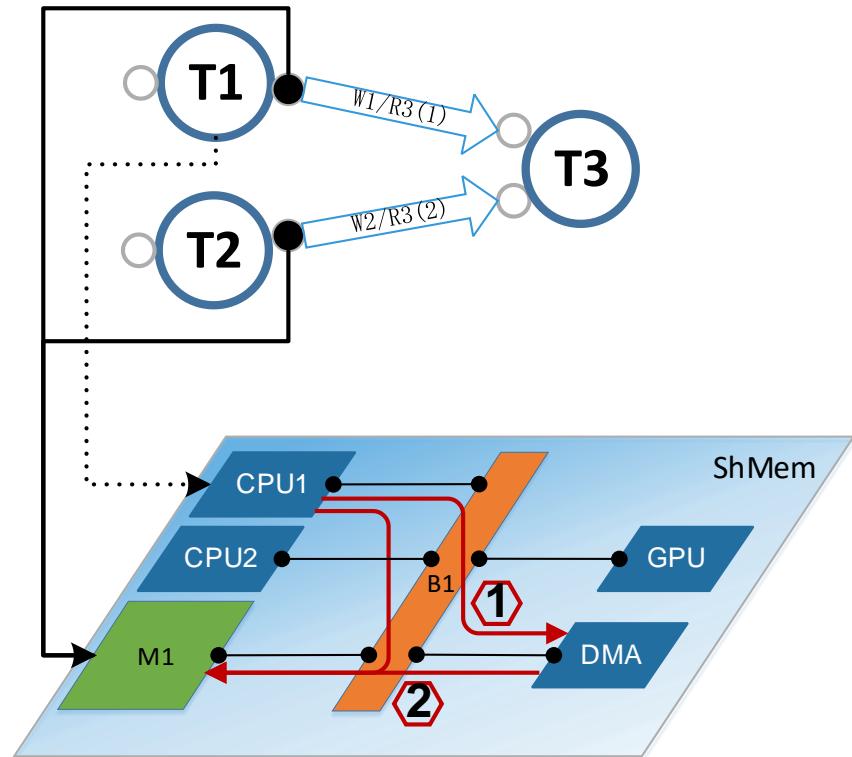
- ▶ Annotations
 - properties attached to model elements,
 - orthogonal and extensible.

Model Element	Architecture Domain	Bandwidth [Mbit/s]	Failure rate [λ]	Flash	Hardware Cost
GP10B	Processor		0.0	300	30
BusMasterPort	Processor		0.0		
NW_A57_READ	Processor	25600.0	0.0		

AER Execution Model

- ▶ Abstraction that enables accurate prediction of temporal behaviour of tasks
 - at design time
 - for shared memory-based systems

- ▶ Separates tasks into *acquire*, *execute*, and *restitution* phases
 - Worst-Case Execution Times (WCETs) of tasks show reduced variance
 - Large variance is caused by interferences at data fetching phases *
 - Enables orchestration of data fetching to avoid interferences at design time



* C. Maia, L. Nogueira, L. M. Pinho and D. G. Pérez, "A closer look into the AER Model," 2016 IEEE 21st International Conference on Emerging Technologies and Factory Automation (ETFA), Berlin, 2016, pp. 1-8, doi: 10.1109/ETFA.2016.7733567.

D³SE – Dependency-Driven Design Space Exploration

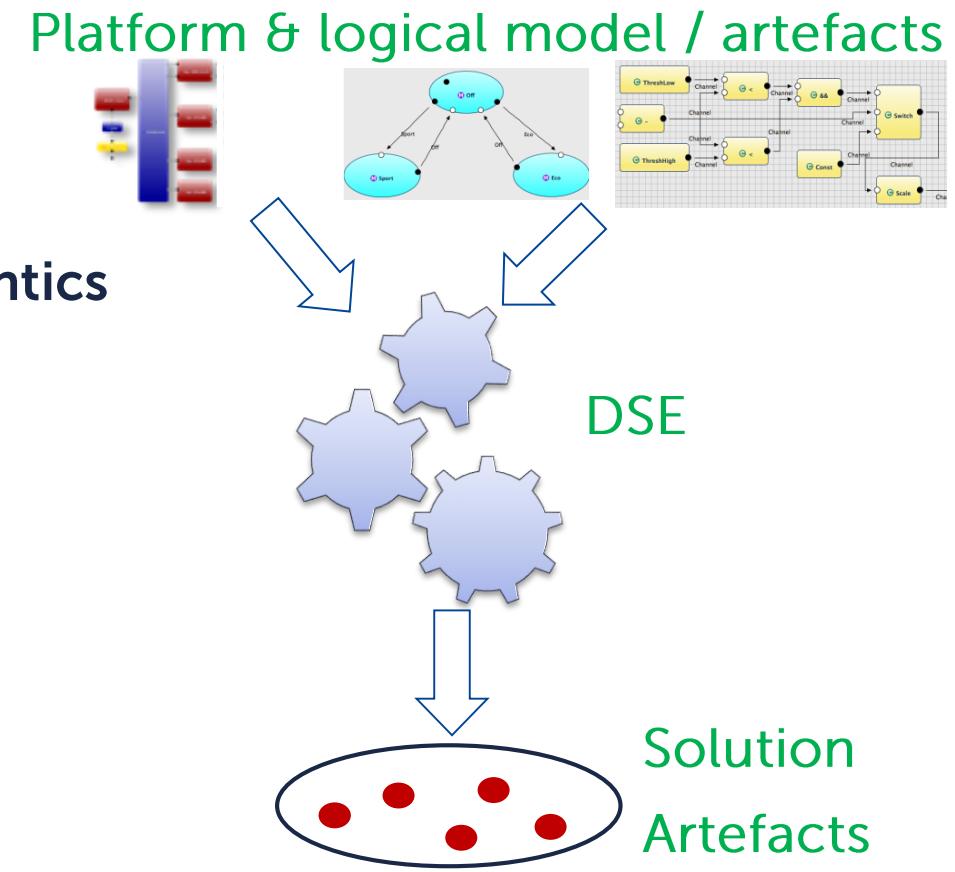
Framework for Activity and Artefact-based Optimization of Distributed Embedded Systems



Reminder: Model-based Design Space Exploration

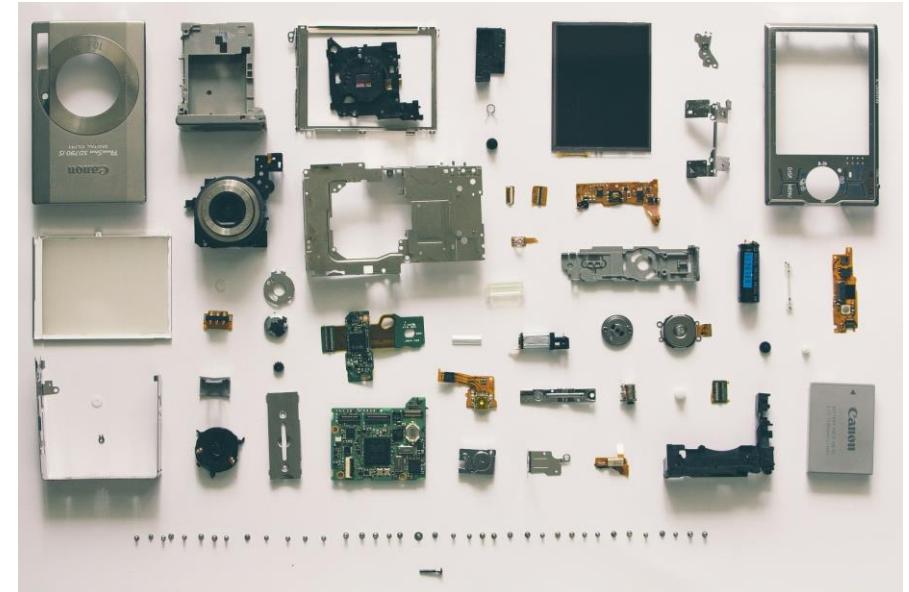
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Decomposition: DSE and Development Processes

1. **Approach:** Decompose development of embedded system into (a set of) activities and artefacts
2. **Artefacts/activities structure the development process:**
 - **Horizontally**, by adding (or synthesizing) additional artefacts from existing ones
 - **Vertically**, by adding details to artefacts
3. An **exploration feature** represents a **development activity**
4. An exploration feature consists of **exploration modules** that **operate on artefacts**



Design Goals for the D³SE Framework

Goals: DSE Expert Productivity, Ease-of-Use, and Performance

► **Supporting system engineers by ease-of-use:**

- Users can tailor DSE executions to their system by enabling/disabling features
- Artefact-based approach allows a deep integration in tools

► **Increasing productivity of DSE experts:**

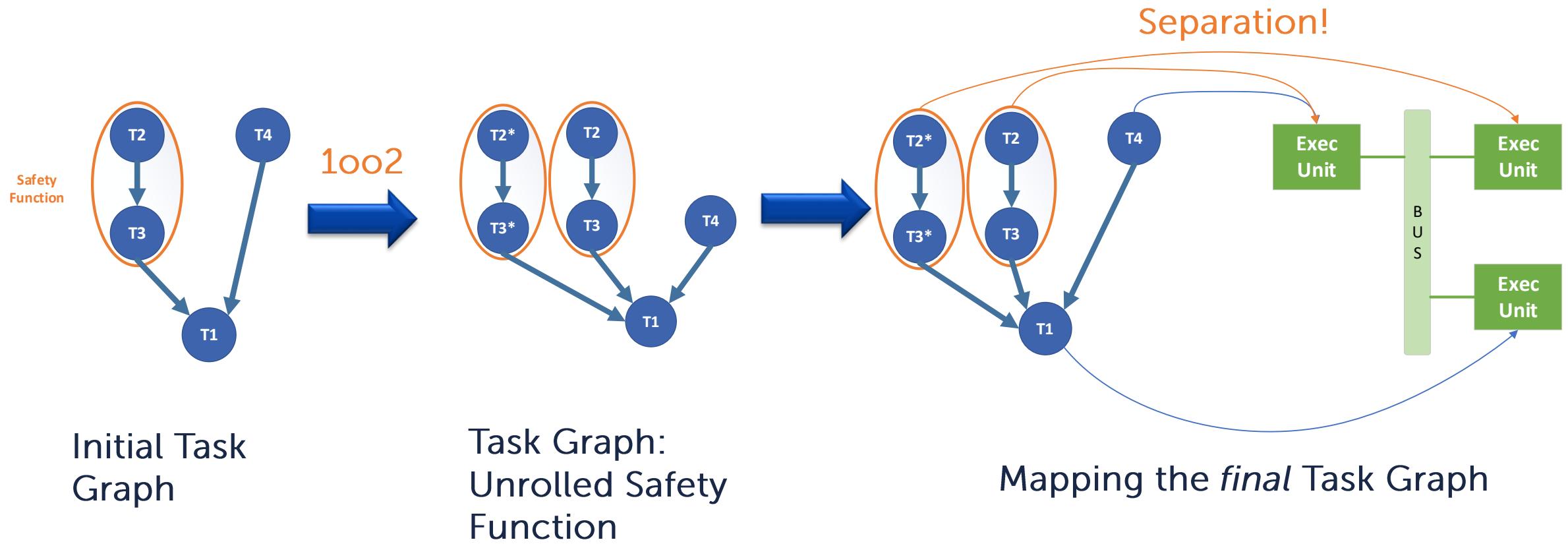
- Interface-driven „orthogonality“ of features eases problem thinking
- White box approach simplifies debugging

► **Performance of iterative approach:**

- Optimizing the elements of a loop pays off
- Avoid infeasible candidates

Dependencies Dominate the DSE

Example: 1oo2 Safety Function → Task Graph → Task Allocation



Dependency-Driven Optimization Decomposition

- State of the art methods require compositionality:

- Convex solution space
- No couplings of subproblems

Master
Problem

SP 1

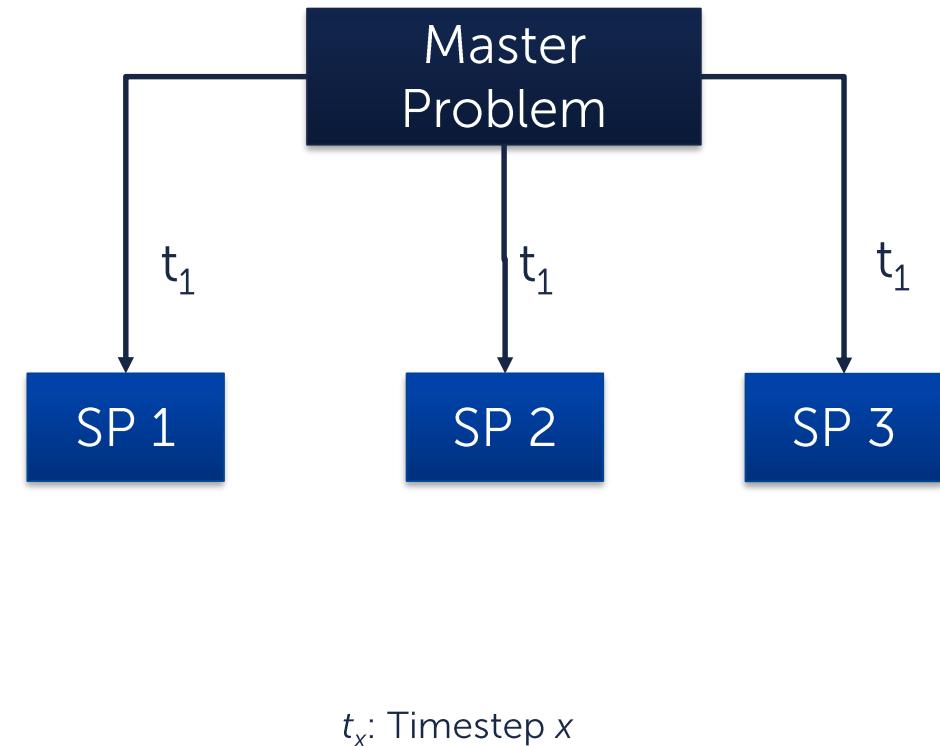
SP 2

SP 3

t_x : Timestep x

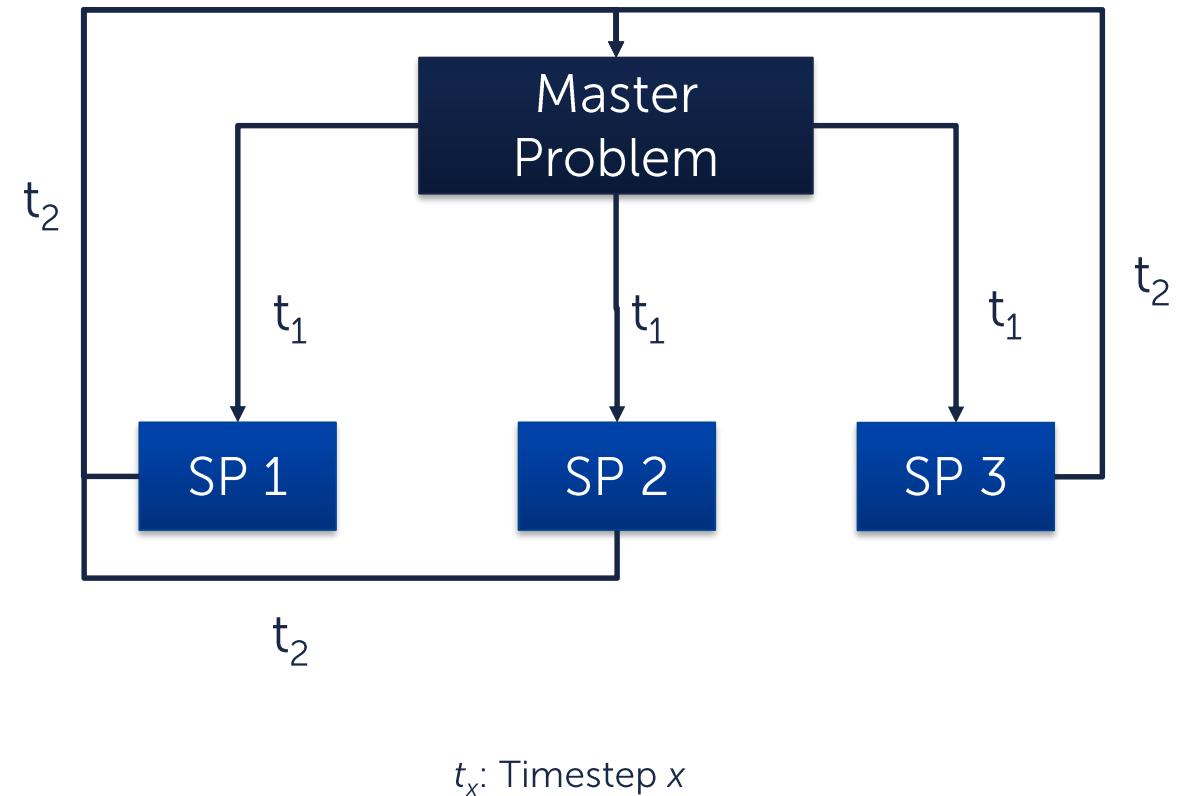
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- **Decomposition by dependencies**

- **Master problem** manages
 - dependencies between subproblems and
 - synchronization between iteration loops.
- **Subproblems**
 - Are solved in order (in parallel where possible)
 - Includes problem-specifics, e.g.
 - SP1: Allocate partitions → execution units
 - SP2: Allocate tasks → partitions
 - SP3: Schedule tasks s.t. SP2

Master
Problem

SP 1

SP 2

SP 3

t_x : Timestep x

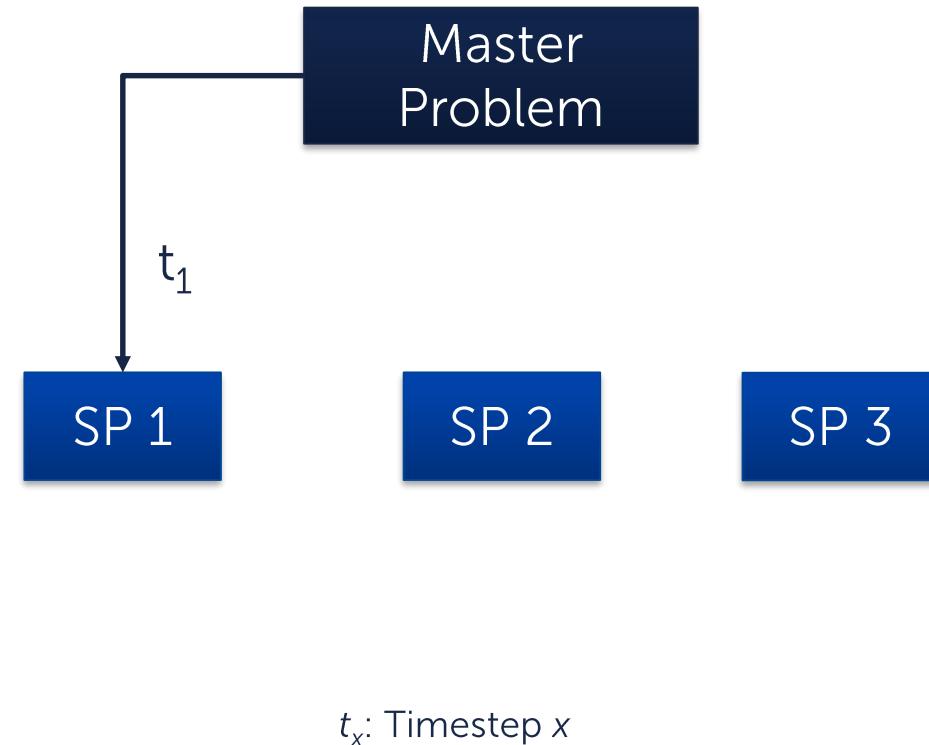
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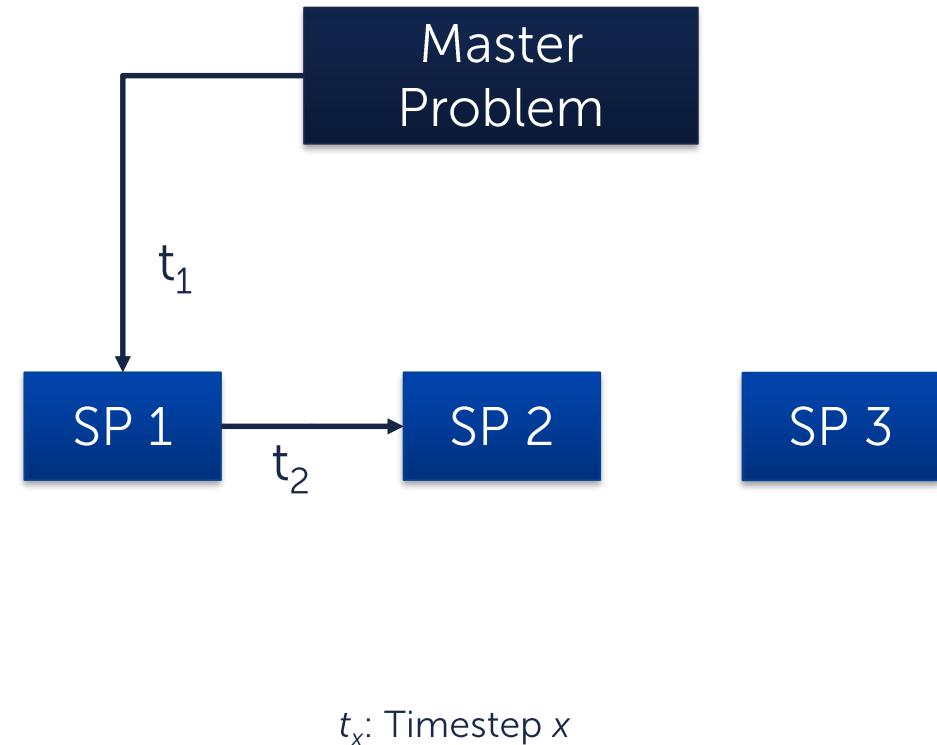
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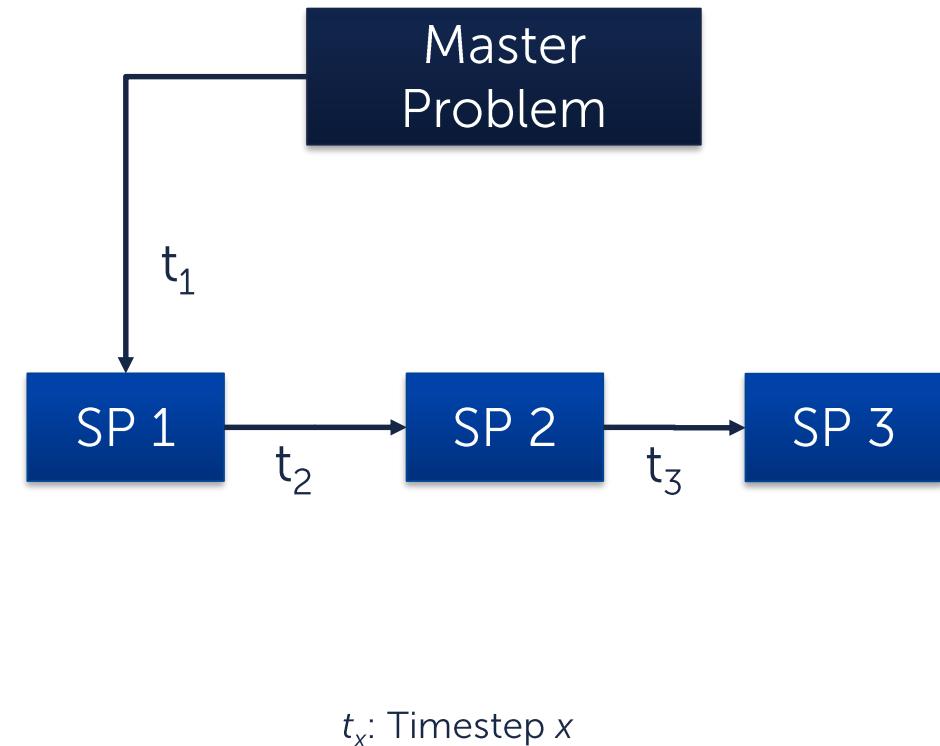
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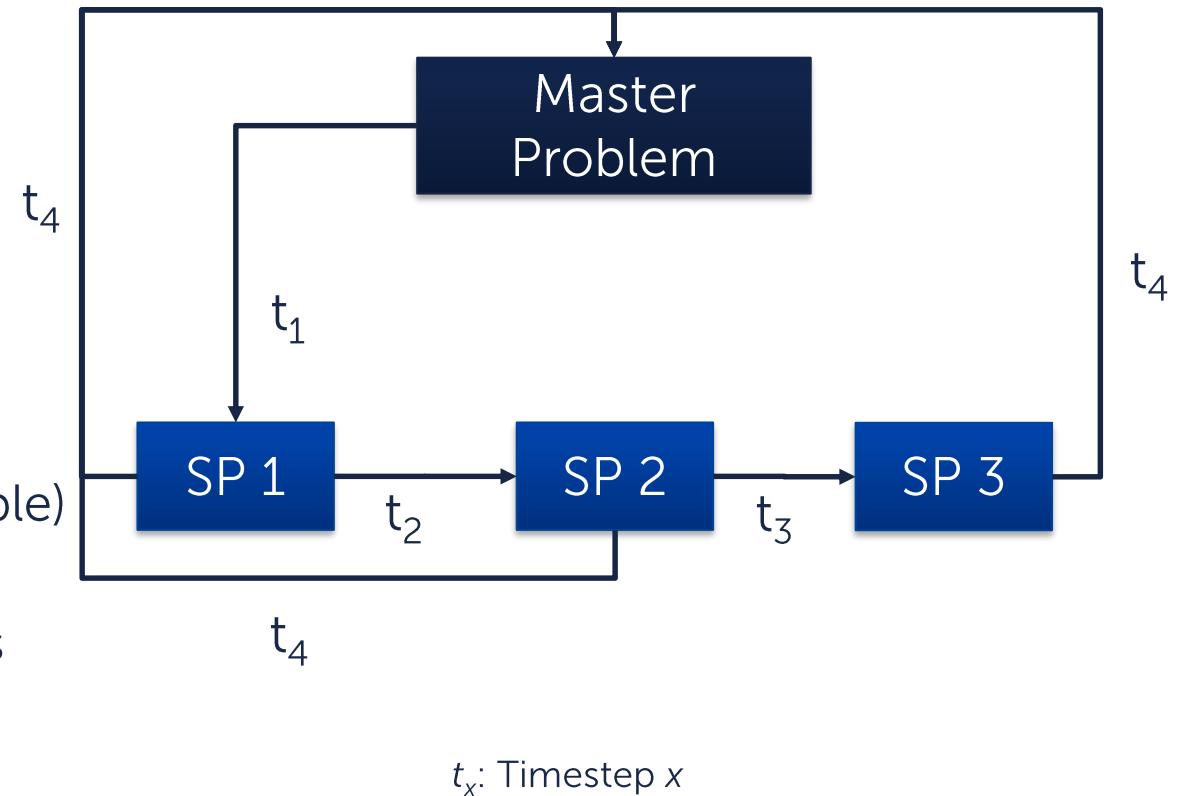
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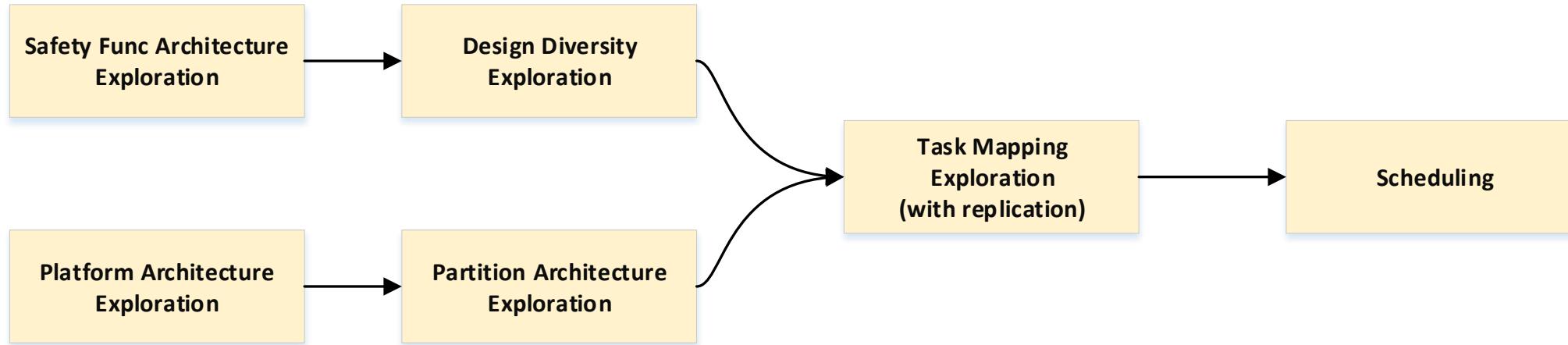
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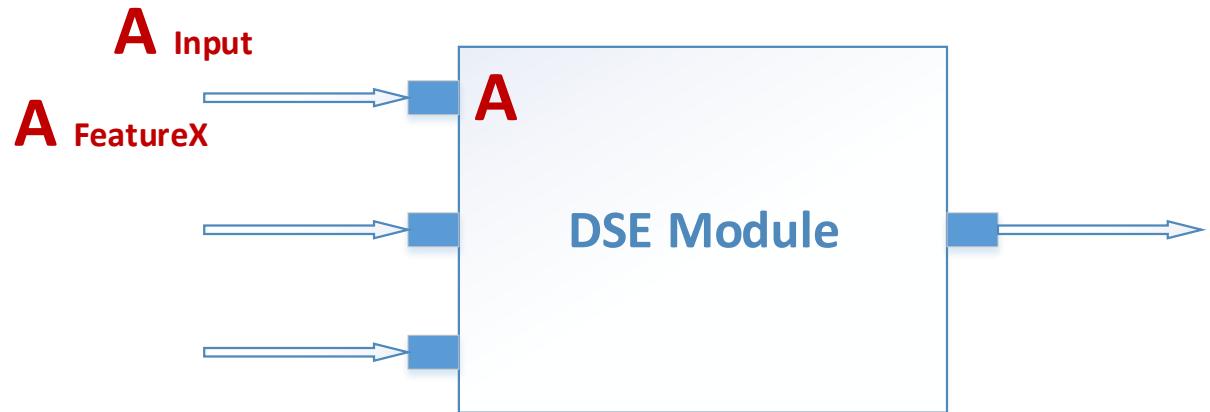
Dependencies - Exploration Feature Graph



- ▶ Represents **dependencies between development activities**
- ▶ Allows switching DSE features on or off according to the system-under-design
- ▶ Avoids hard dependencies between artefacts → **Reusability, flexibility**
- ▶ High-level dependency considerations, low-level problem thinking

Dependencies - Exploration Modules

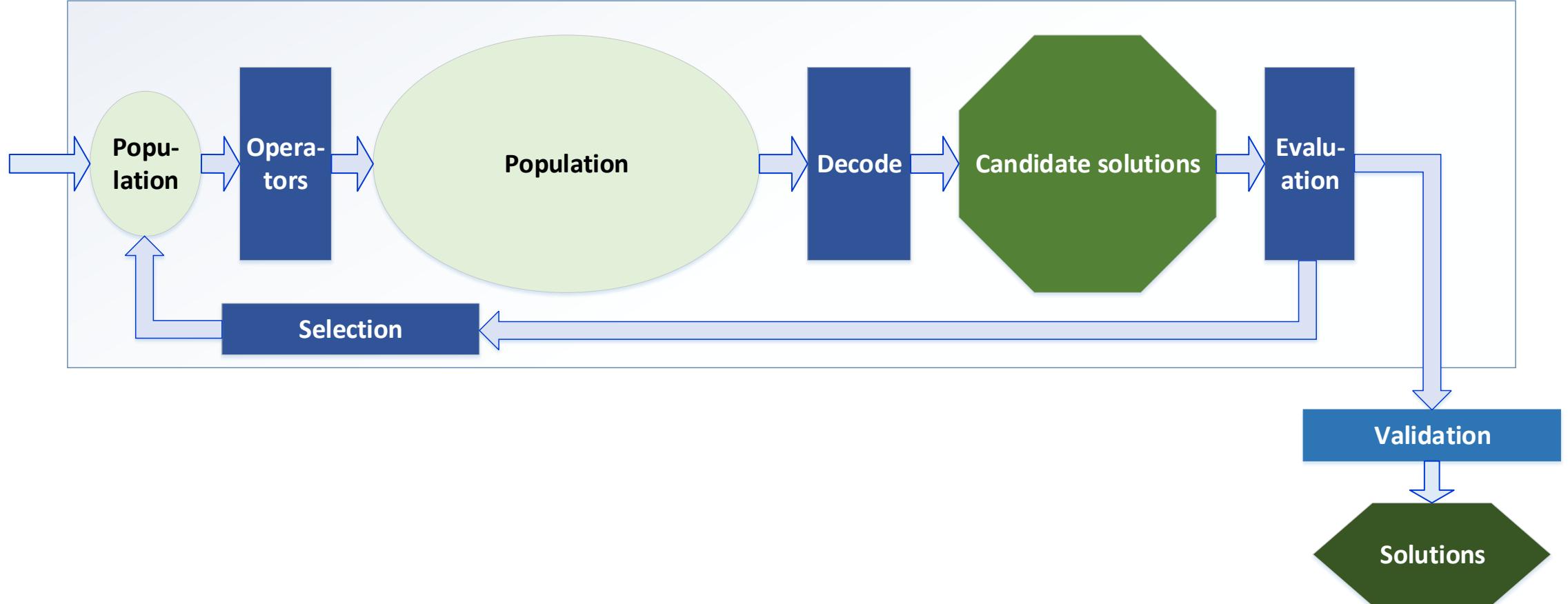
- ▶ Exploration features consist of exploration modules
- ▶ Exploration modules modify / transform artefacts (N:1), e.g.
 - Task graphs (e.g., include task replica)
 - Platform graphs (Exec. Unit Variance)
 - ...
- ▶ DSE Framework implementation
 - Dependency Injection (Guice)
 - I/O artefacts are annotated with their corresponding exploration features
- ▶ DSE Execution
 - Execution order determined by artefact dependencies
 - Identical artefact types ordered by *exploration features*



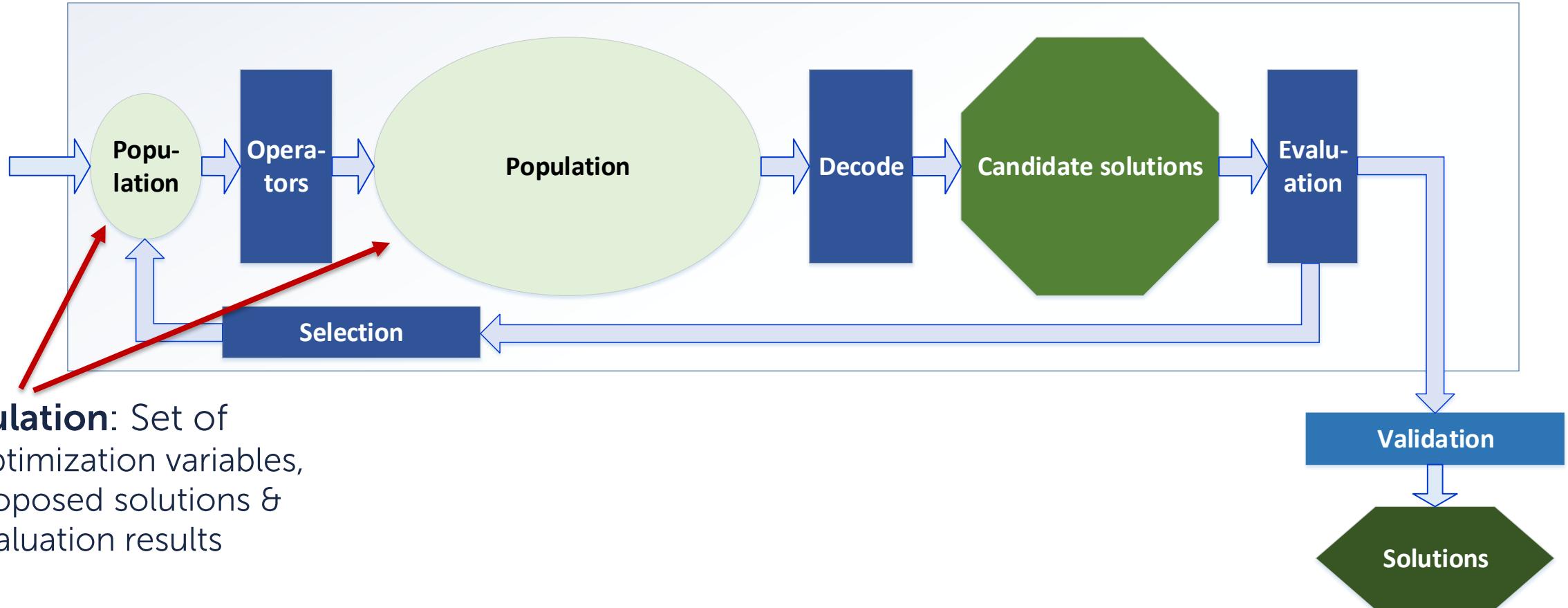
```
47 /**
48 * Takes a {@link PlatformCommunicationGraphEncoding} genotype and provides it as its
49 * {@link Phenotype} representation.
50 */
51 @author diewald
52 */
53 public class PlatformCommunicationGraphExecUnitInstanceDecoder
54   extends DecoderModule<PlatformCommunicationGraphEncoding> {
55
56   /**
57    * See {@link PlatformCommunicationGraphExecUnitInstanceDecoder}.
58   */
59   @Decodes
60   @Provides
61   public PlatformCommunicationGraphEncoding decode(
62     @InputArtifact PlatformCommunicationGraphEncoding pcgEnc,
63     @Genotyped PlatformExecUnitInstanceEncoding peuiEnc,
64     PlatformExecUnitTemplateEncoding execUnitTemplateEnc) {
65     PlatformCommunicationGraphEncoding decodedPCGEnc =
66       new PlatformCommunicationGraphEncoding(pcgEnc);
67     DefaultDirectedGraph<IResourceAdapter<?>, DefaultEdge> pGraph =
68       decodedPCGEnc.getActualGraph();
69     for(IExecutionUnitAdapter<?> execUnitContainer : peuiEnc.getAbstractContainerExecUnits()) {
```

A method signature is sufficient to declare dependencies

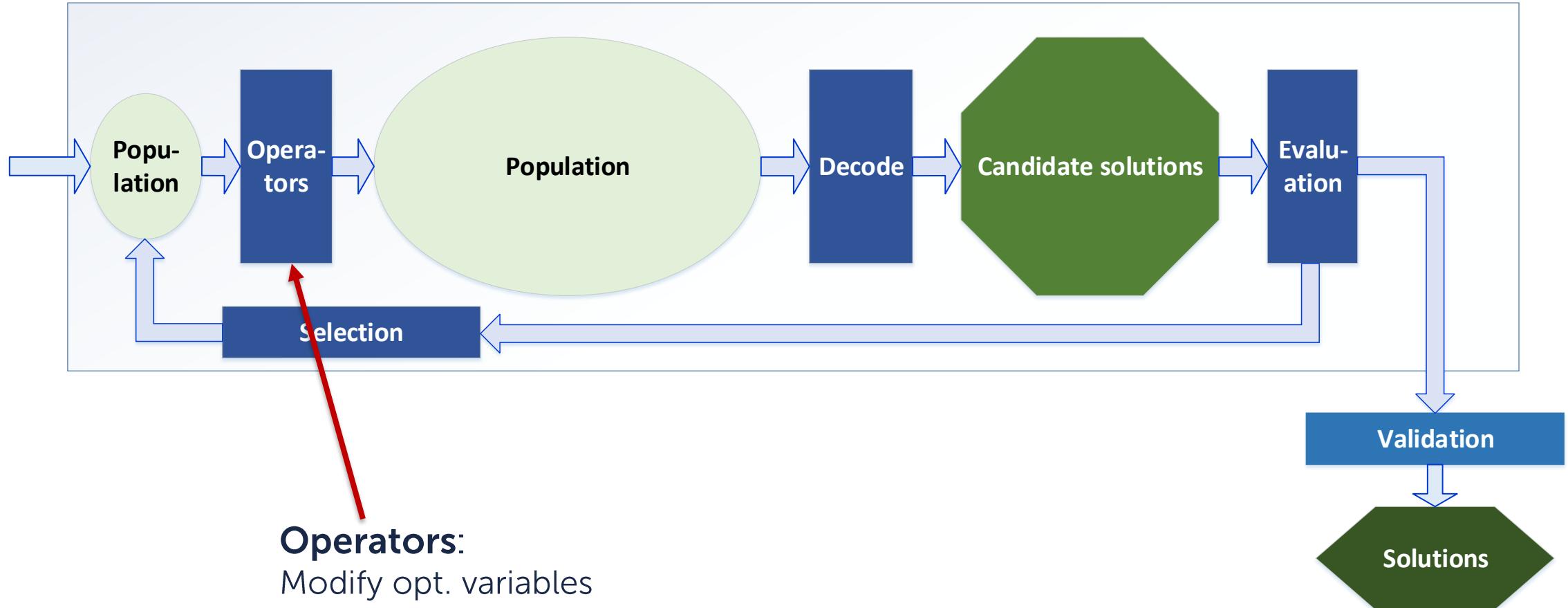
DSE Framework for Architectural Exploration



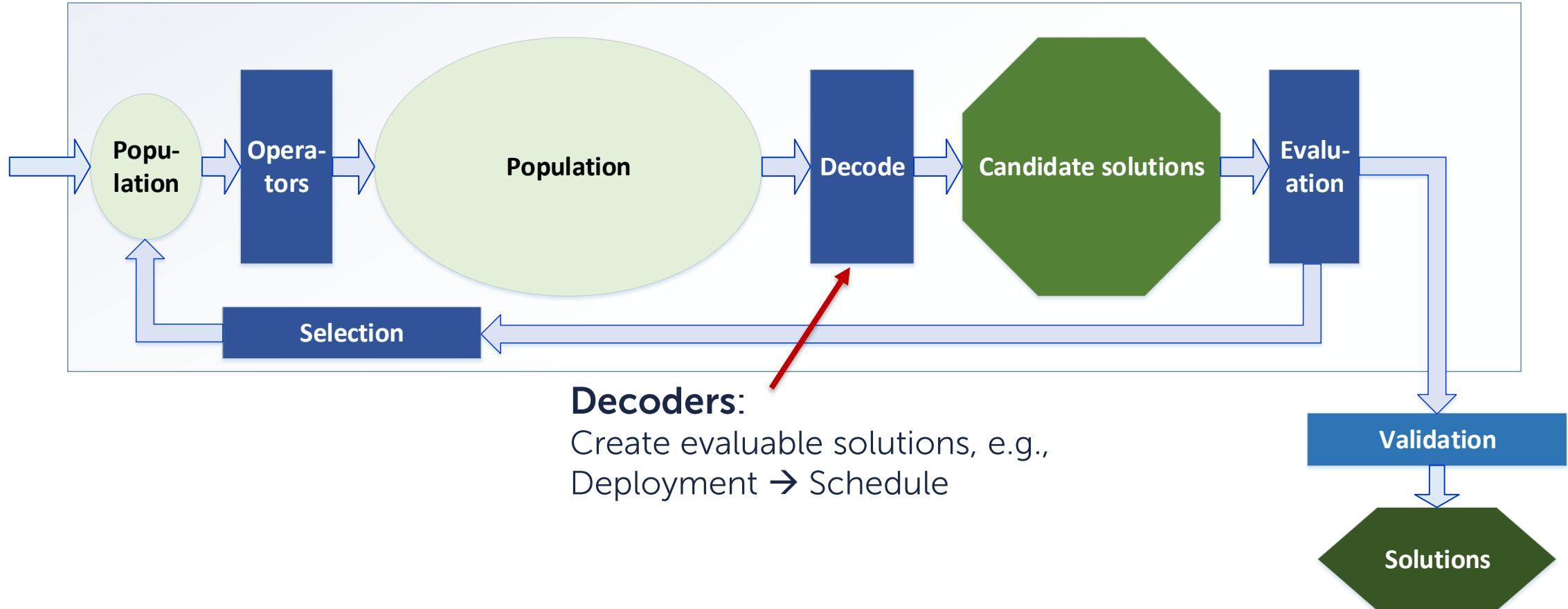
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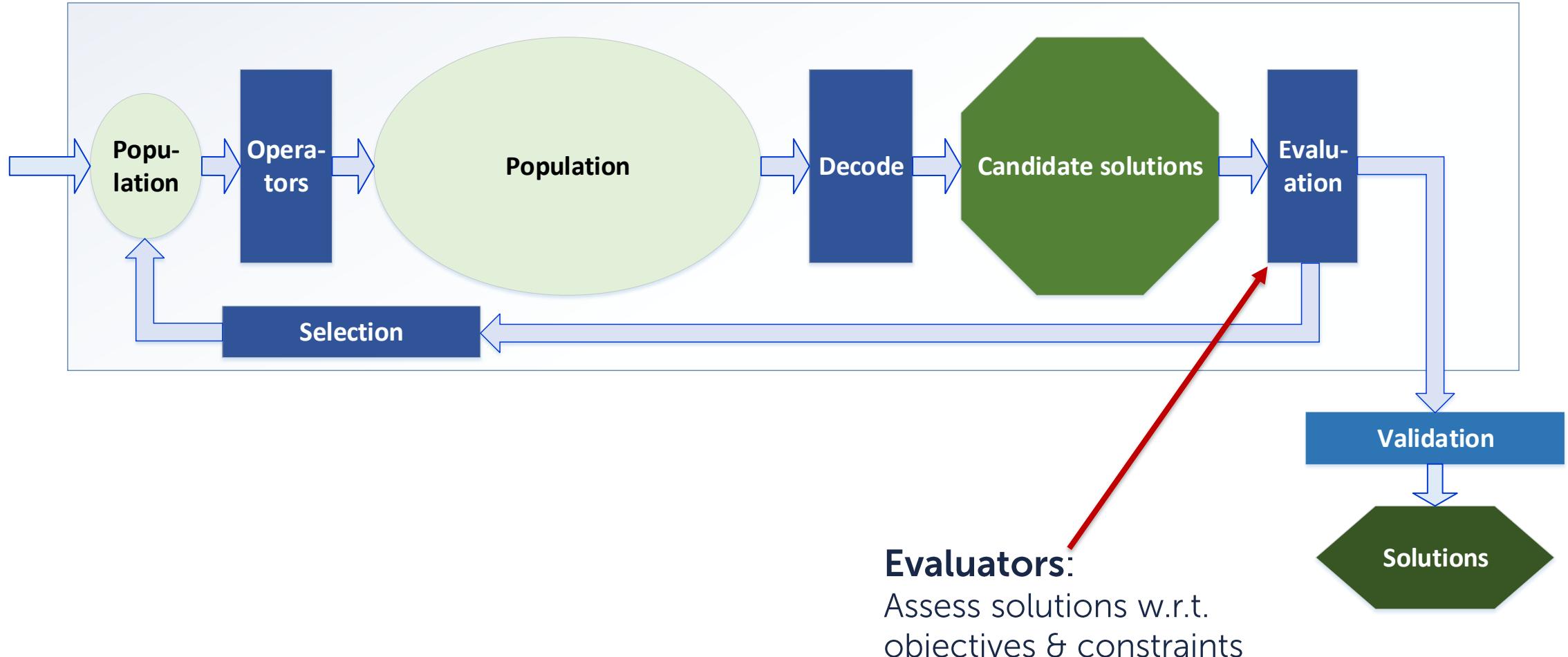
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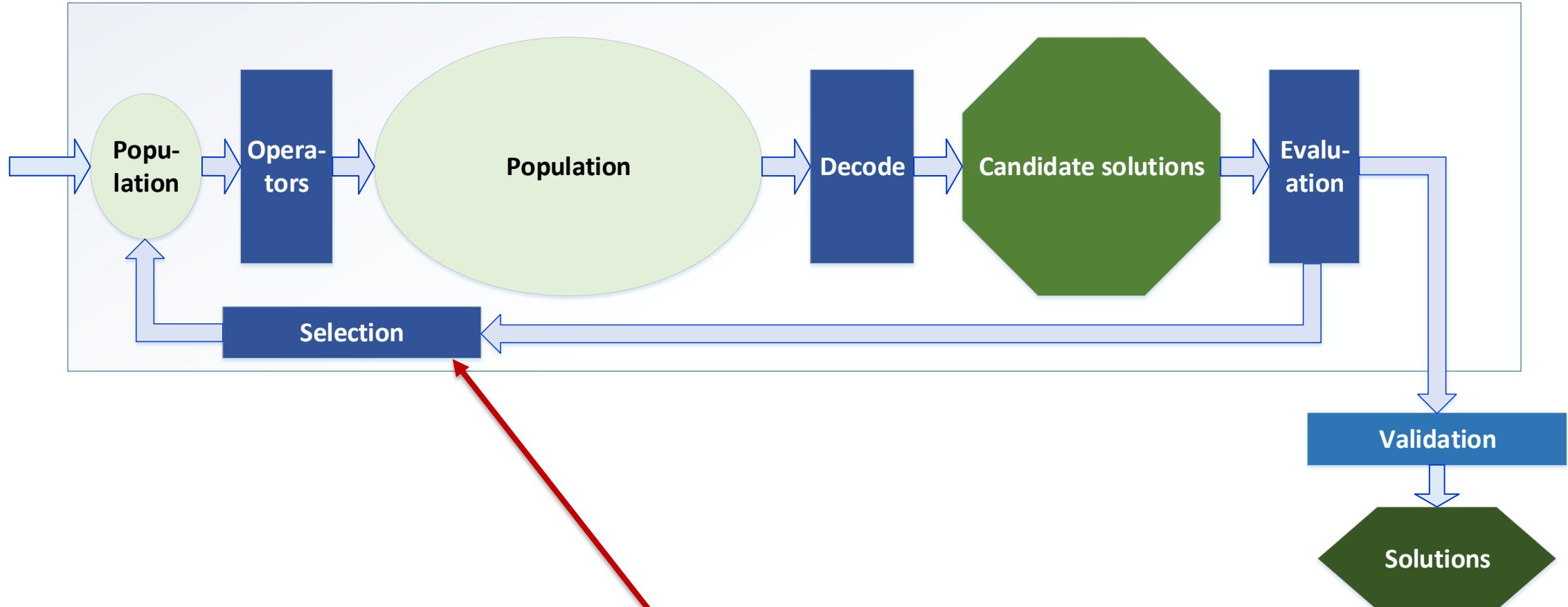
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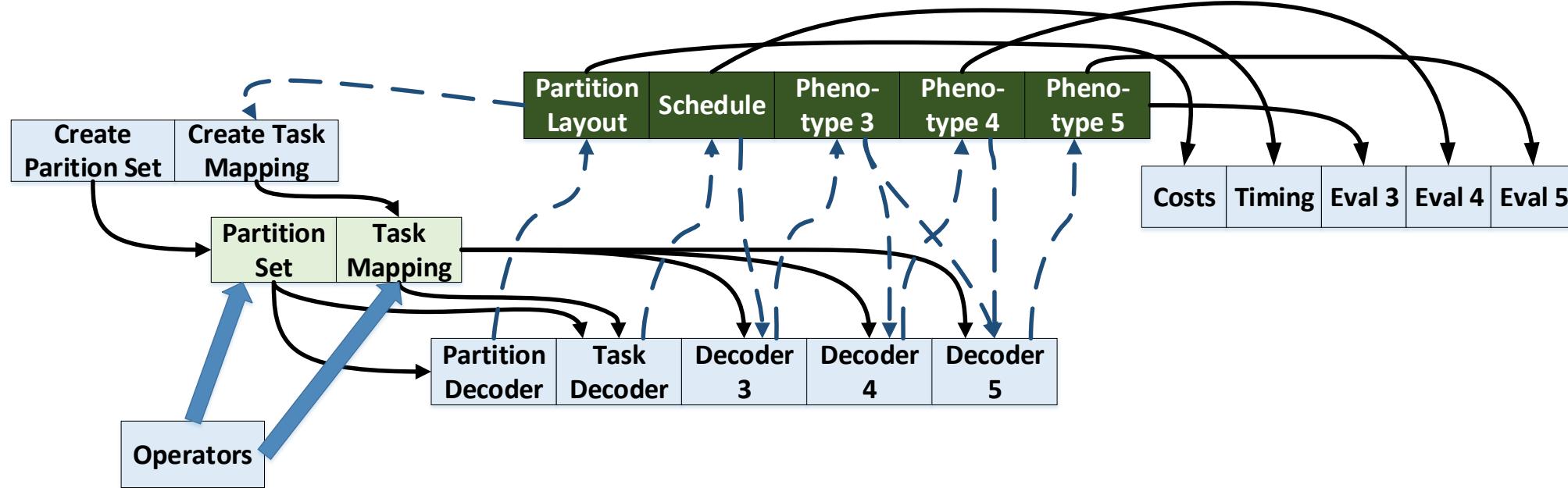


DSE Framework for Architectural Exploration

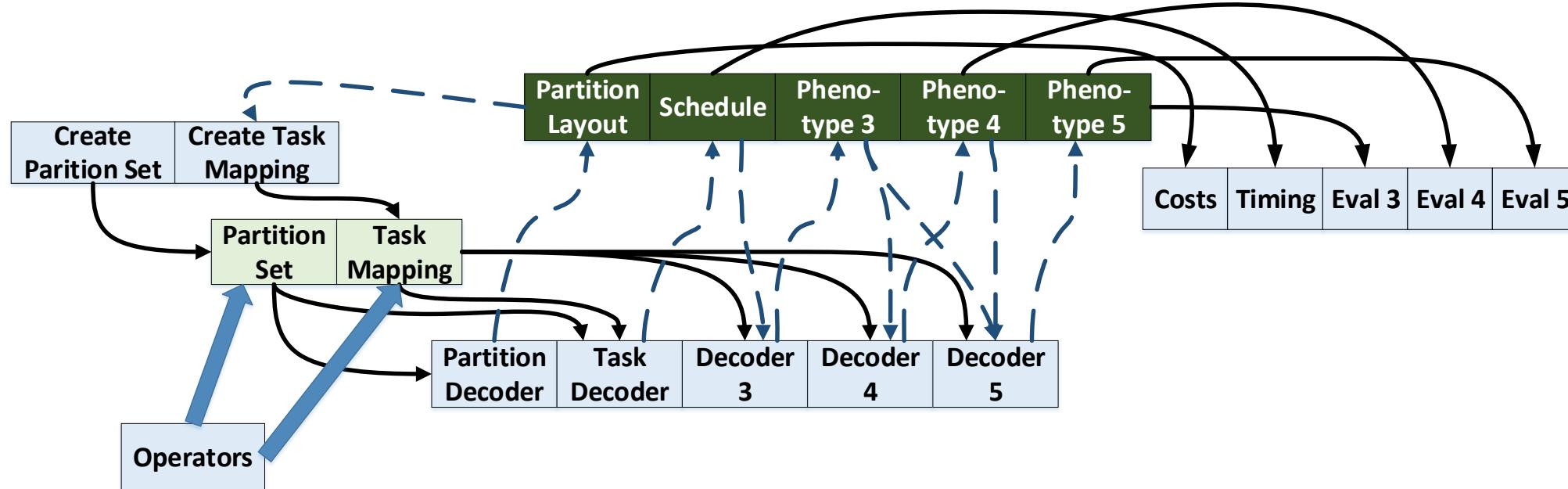


Feedback loop:
Pick promising solutions

DSE Framework for Architectural Exploration



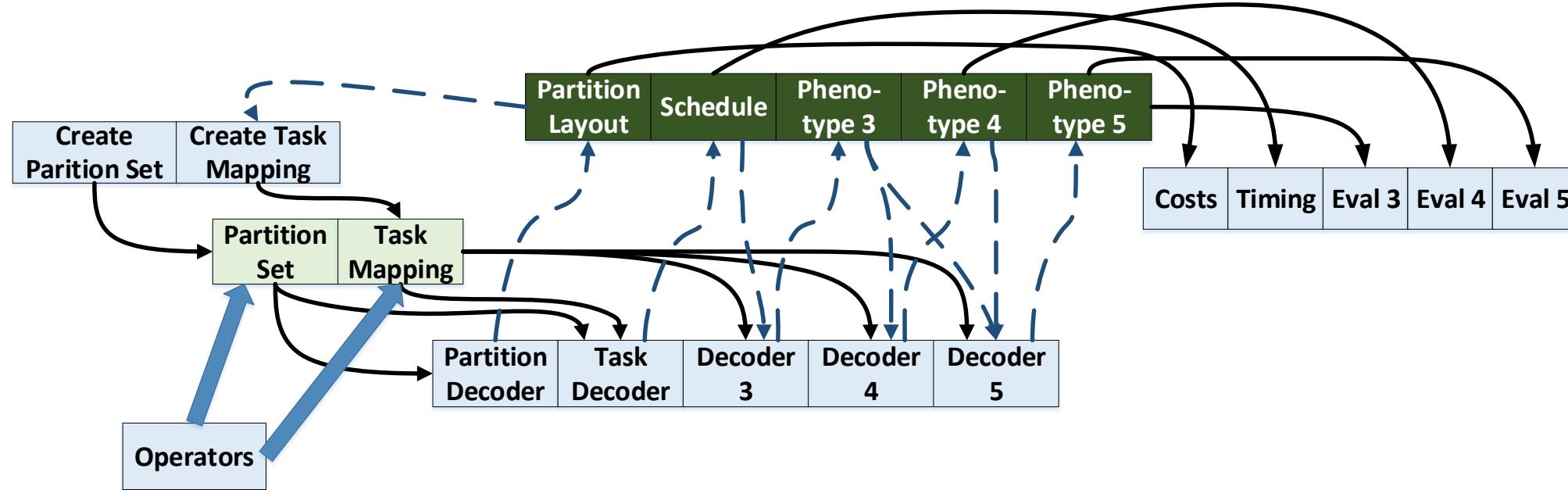
DSE Framework for Architectural Exploration



Exploration Modules

- ▶ Combine sub-problems with matching decoders, etc.
- ▶ Example:
Variable: Safety architecture;
Operators: \pm number of safety function channels

DSE Framework for Architectural Exploration



Exploration Modules

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Process-oriented DSE

- ▶ Optimize multiple design steps in a loop
- ▶ Automatically resolve dependencies, e.g., safety architecture impacts deployment (fault isolation)

Available DSE features (1/2)

► Safety function architecture exploration, e.g., 1oo2D

- Instantiation of isolated safety channels
- Instantiation of diagnosis units
- Operates on a task graph

► Platform exploration:

- Explores an optimal number of execution units
- Adjust the underlying platform graph

► Partition exploration:

- Optimizes the number of partitions
- Optimizes task-partition & partition-exec. unit allocations
- Generates communication channels between partitions

Available DSE features (2/2)

► Design diversity:

Instantiates template tasks (→ task interfaces) with task implementations from a library.

► Bare-metal task mapping exploration

- Optimizes allocations from tasks to execution units
- Allocation mechanism shared with the partition exploration

► Heuristic scheduling

Generation of simple time-triggered system-wide task and communication schedules

Tool Support

Demonstration in AutoFOCUS3

The screenshot displays the AutoFOCUS3 interface with several windows open:

- Model Navigator**: Shows the project structure under the ACC System, including Requirements Analysis, Data Dictionary, and various sub-components like AdaptiveCruiseControl, AccelerationControl, DistanceControl, etc.
- Component Structure**: Shows the internal structure of the AdaptiveCruiseControl component, featuring nodes such as SpeedPlausibilization, DistancePlausibilization, SpeedControl, and DistanceControl, connected by arrows indicating data flow.
- Properties**: A table showing system properties:

Model Element	Comment	Safety Level
ACC System	Overall System with ACC and Sim...	ISO 26262
AdaptiveCruiseControl	The ACC System	QM
AccelerationControl	Component computing the acceler...	QM
DistanceControl	Component computing the mome...	QM
- Marker View FX**: A view showing severity levels (Information, Warning, Error) for different elements.
- Model Elements**: A list of available behavioral specifications and component architectures.
- Task Architecture**: A table mapping components to tasks:

Source	Target	Source Type	Target Type			
ACC System	Task Architecture (generated for: ACC)	Component	Task			
		↓ Src. Tgt. →	Task_& Task_- Task_< Task			
		↓ Src. Tgt. →	Task_& Task_- Task_< Task			
AdaptiveCru...		Acceler...	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		Distanc...	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		Distance...	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
SpeedCo...		&&	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		-	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		<	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
		<	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
		Const	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		Ref...	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		Scale	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		Switch	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		Thr...	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		Thr...	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		SpeedPla...	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

AutoFOCUS3

Fully model-based platform to research future CPS engineering principles

Open Source Tool and Research Platform based on the Eclipse Platform

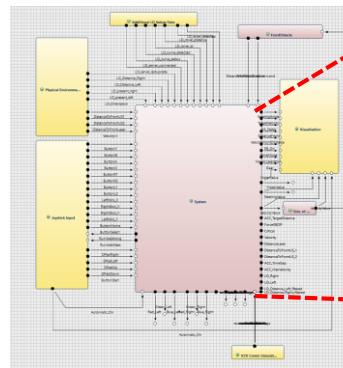
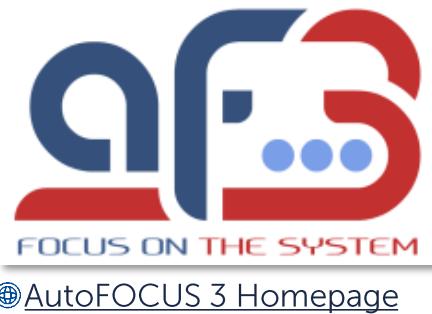
- ▶ Foundation for **applied research** with automotive and avionics OEMs and suppliers
- ▶ High-quality research platform for **efficient prototyping** of novel engineering methods and **collaboration within the team**

Research Areas

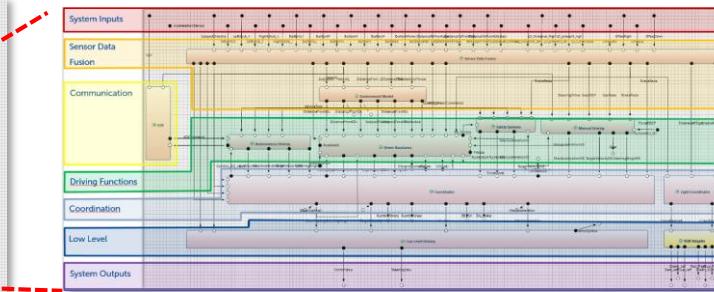
- ▶ **Architecture Analysis and Synthesis:** *"What are the cheapest and most efficient HW/SW architectures satisfying all constraints?"*
- ▶ **Re-Use & Variability:** *"How to incrementally develop product-lines and reusable components in an agile manner?"*
- ▶ **(Co-)simulation:** *"Do my components behave as intended? In particular, does my system when I integrate everything?"*
- ▶ **Safety cases:** *"How to build structured modular safety argumentation, and how to maintain it on model changes?"*

Latest Publications ([@ see here](#) for all 40+)

- ▶ J. Eder, S. Voss, A. Bayha, A. Ipatiov, and M. Khalil, "Hardware architecture exploration: automatic exploration of distributed automotive hardware architectures," *Software and Systems Modeling*, Mar. 2020, doi: 10.1007/s10270-020-00786-6.
- ▶ A. Diewald, S. Barner, and S. Saidi, "Combined Data Transfer Response Time and Mapping Exploration in MPSoCs." in 10th Int. Workshop on Analysis Tools and Methodologies for Embedded and Real-time Systems (WATERS). Jul. 2019.



Logical architecture w/
simulation context



ADAS/AD system of fortissimo rover

Architecture
Analysis & Synthesis

Code Generation
(Co-)Simulation

Safety Cases

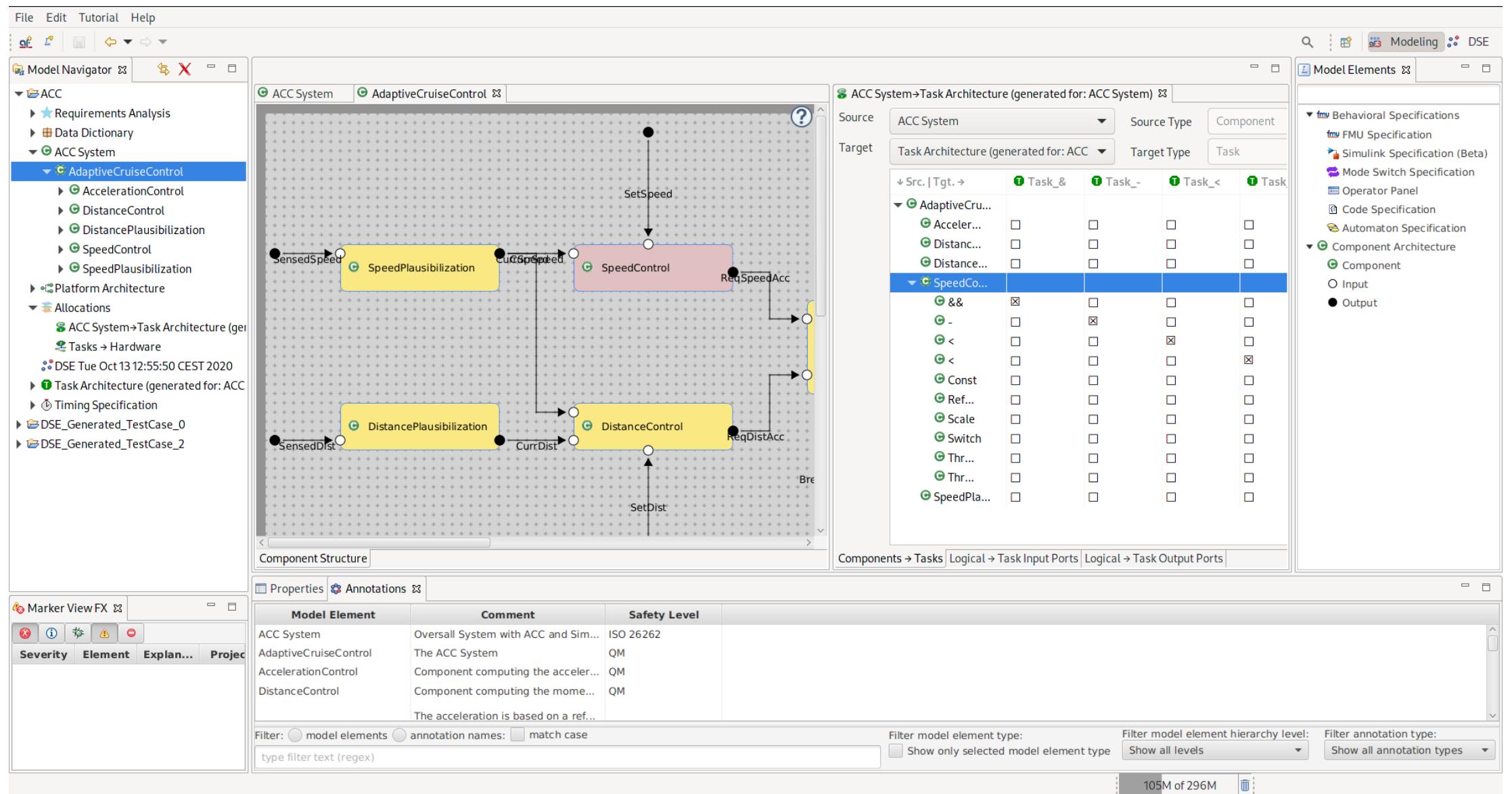


fortissimo
simulator



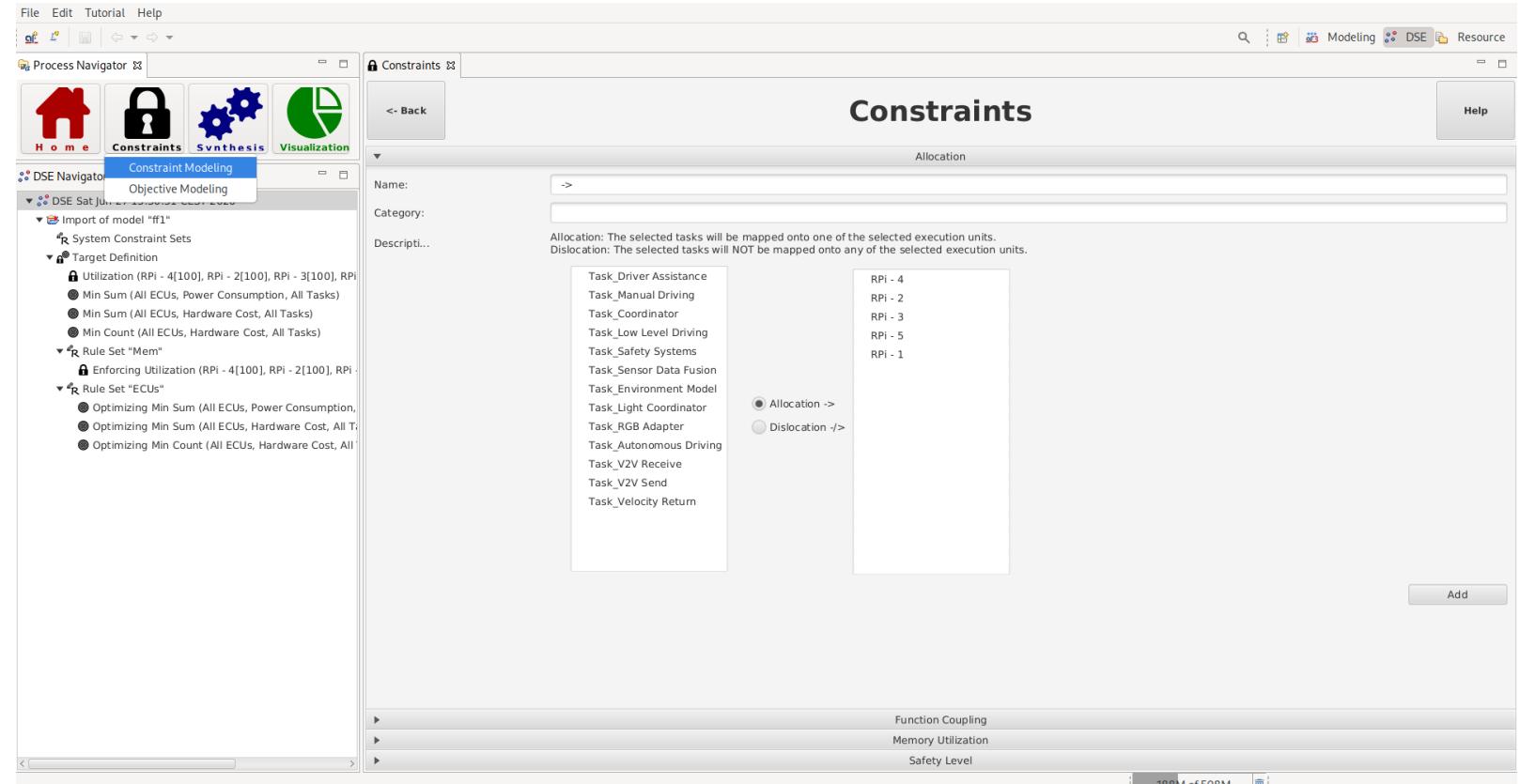
fortissimo
rovers

AutoFOCUS 3 - Modelling



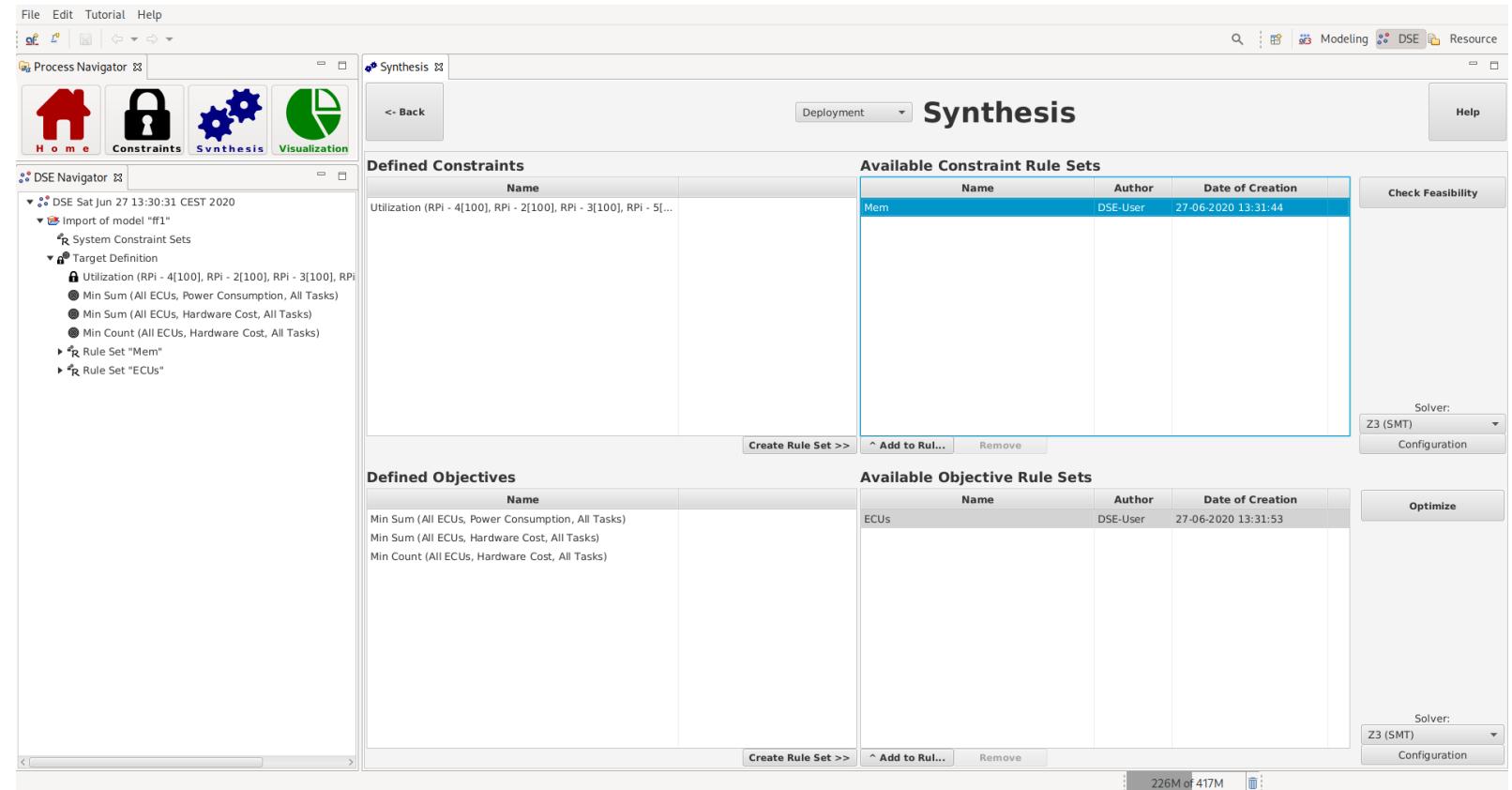
AutoFOCUS 3 – DSE Perspective

- ▶ Modelling of **Constraints & Objectives**
- ▶ Synthesizing artefacts by a DSE algorithm
 - Platform
 - Deployments
 - Schedules
- ▶ Result visualization & model export
 - Spider chart
 - Schedule view



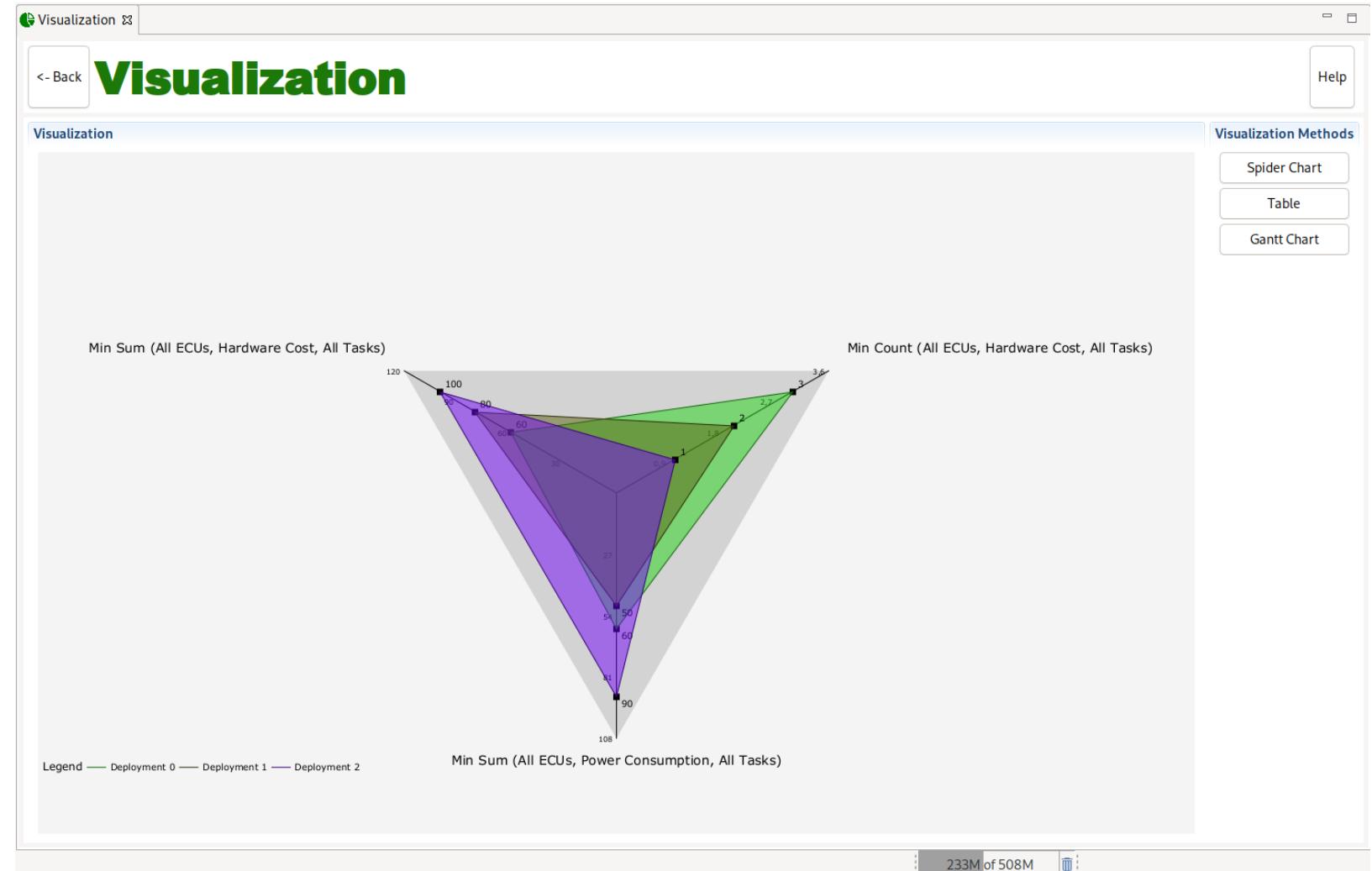
AutoFOCUS 3 – DSE Perspective

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AutoFOCUS 3 – DSE Perspective

- ▶ Modelling of **Constraints & Objectives**
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- ▶ Result visualization & model export
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Take Home and Outlook

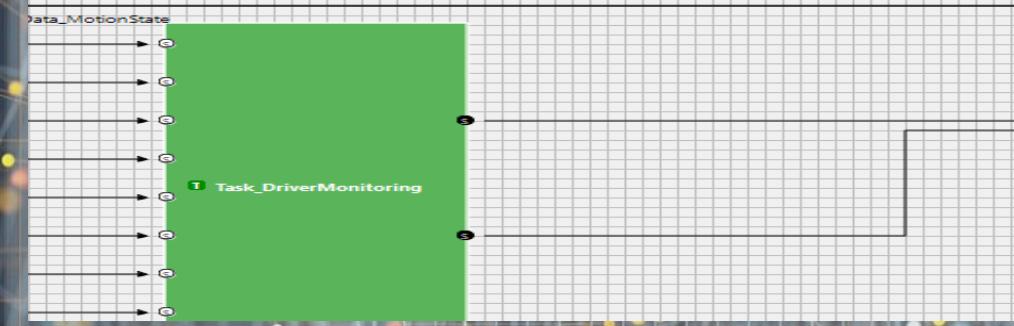
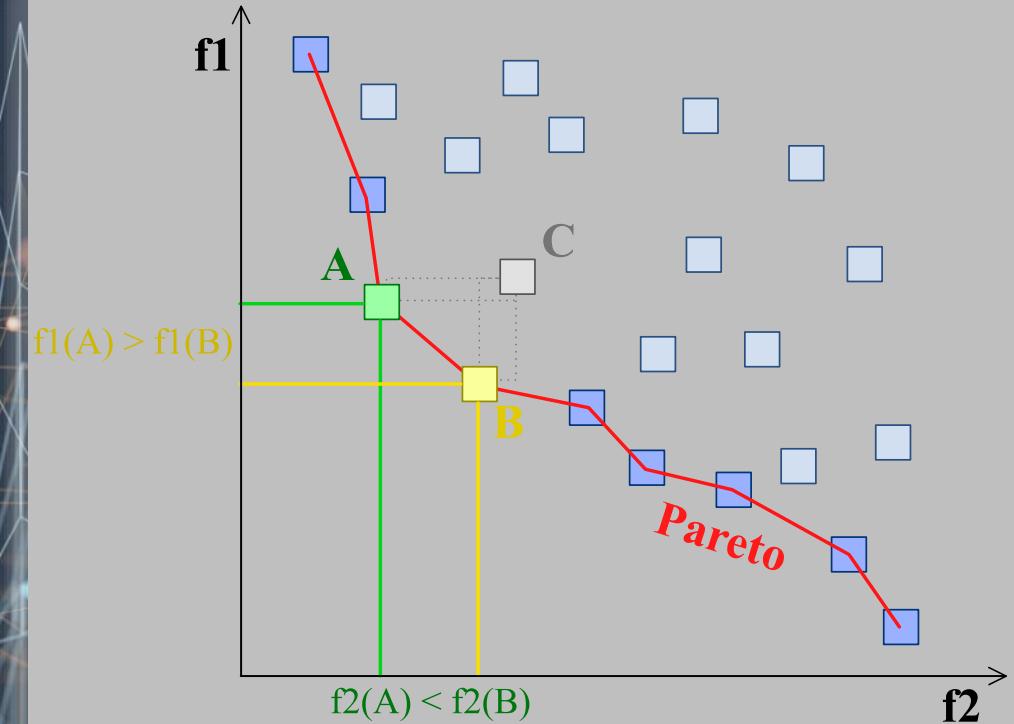
- ▶ **Model-based System Engineering** supports to
 - define and structure the development of complex embedded systems,
 - ease reuse of development artifacts (e.g., to adapt to new platforms), and
 - uncover the underlying design space.
- ▶ **A dependency-driven DSE**
 - Enables reuse and extensibility through **modular exploration features**
 - Can be adapted to different systems under design by means of artifact and I/O thinking,
 - Allows to consider design constraints through dependencies, and to offer design alternatives by multi-objective optimization.
- ▶ **Implementation in AutoFOCUS3**
 - <https://www.fortiss.org/veroeffentlichungen/software/autofocus-3>

Thank you for your attention!

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AGENDA

9:30

Session 1: Fundamental Issues with
Concurrency in Embedded Software
Systems from Architectural Point of
View

10:30

10:45

Session 2: Modelling and DSE
Methods for Mixed-Critical Software
Systems using Multicore
Architectures

11:45

12:00

Session 3: Synchronization in
Concurrent Software is an
Architectural Decision

13:00