STM32WL architecture and peripherals

Architecture & peripherals

Key learning

- STM32WL architecture
- STM32WL new peripherals
- STM32WL low power modes

Architecture

- STM32WL5 embeds dual CPU
  - Cortex-M4
  - Cortex-M0+
- Sub-GHz radio
- Independent real-time CPU execution
- 3 autonomous sub-systems
  - Cortex-M4 (CPU1)
  - Cortex-M0+ (CPU2)
  - Sub-GHz radio sub-system

Application benefits

- Fully Independent autonomous real time operation between the CPU1 and CPU2
- Optimized low power consumption
  - smart clocking
  - stand alone connectivity operation
- Isolation of connectivity Stack

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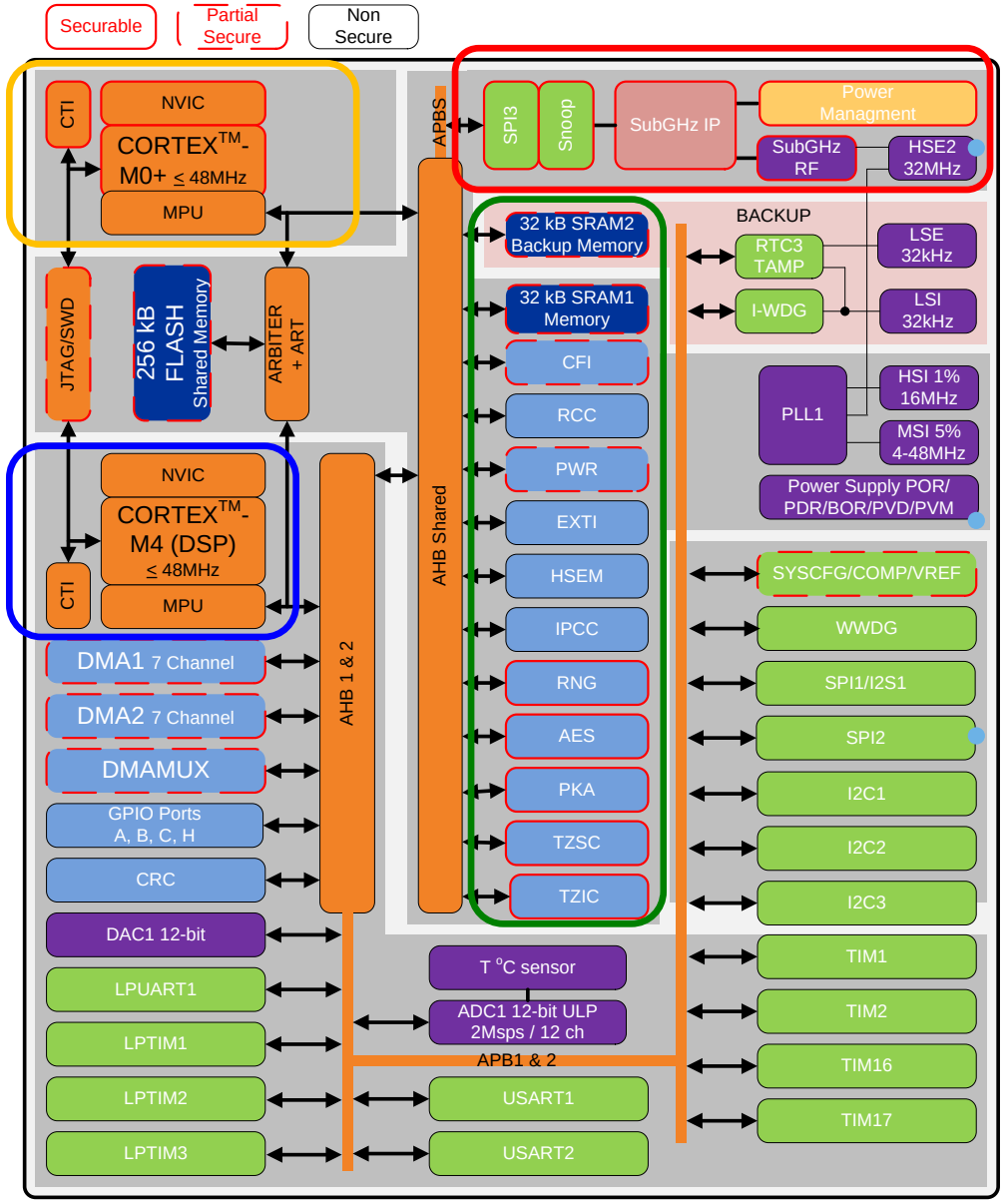
Architecture



3 autonomous sub-systems.

- Cortex-M4 (CPU1)
- Cortex-M0+ (CPU2)
- Radio sub-system

Common domain

- Flash, SRAM1 & 2, RCC, PWR, EXTI

Other peripherals are enabled per CPU

- In the common domain:
  - IPCC, HSEM, AES, PKA, RNG, GTZC, CFI, sub-GHz radio
- In the CPU1 domain
  - DMA, TIM, SPI, USART, I2C, WDG, ADC, DAC, TEMP, RTC, TAMP.

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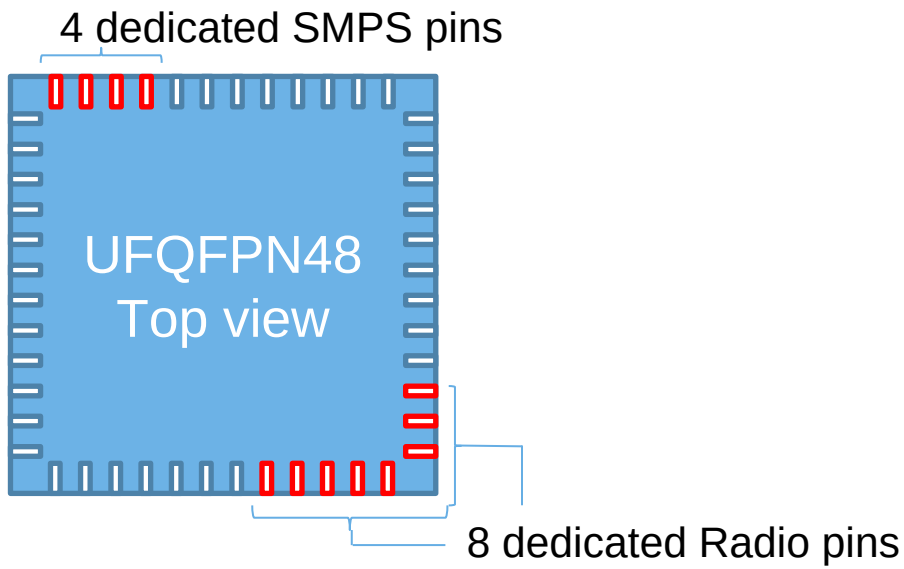
Specific features 1/2

- Autonomous sub-GHz Radio sub-system
- Dual core system
  - CPU1 Cortex-M4 (Boot after Reset)
  - CPU2 Cortex-M0+ (Will only boot once enabled by CPU1).
- Single bank shared Flash and SRAM memories
  - On a separate AHB bus, with it’s own clock divider.
- CPU2 Cortex-M0+ memory and peripheral isolation
- HSE fixed frequency 32 MHz with support for TCXO.

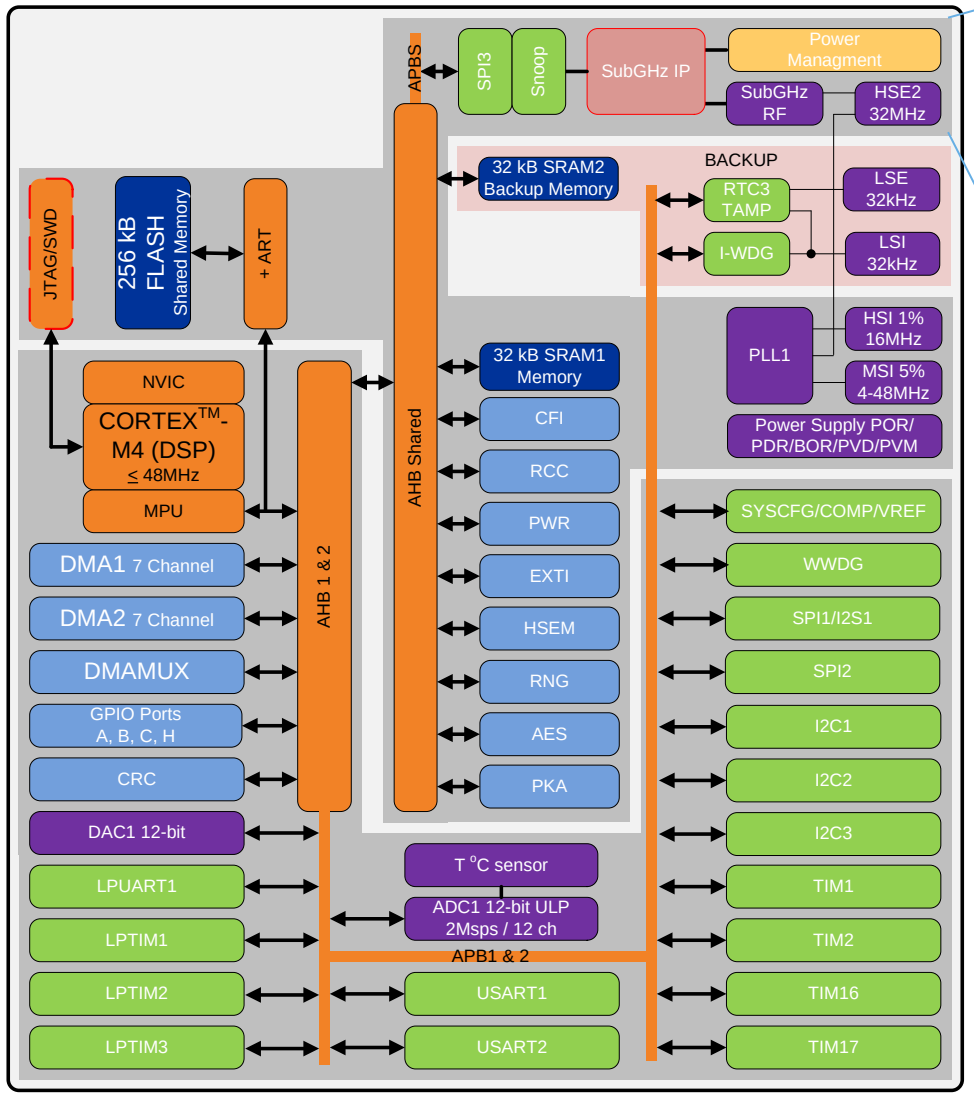
Specific features 2/2

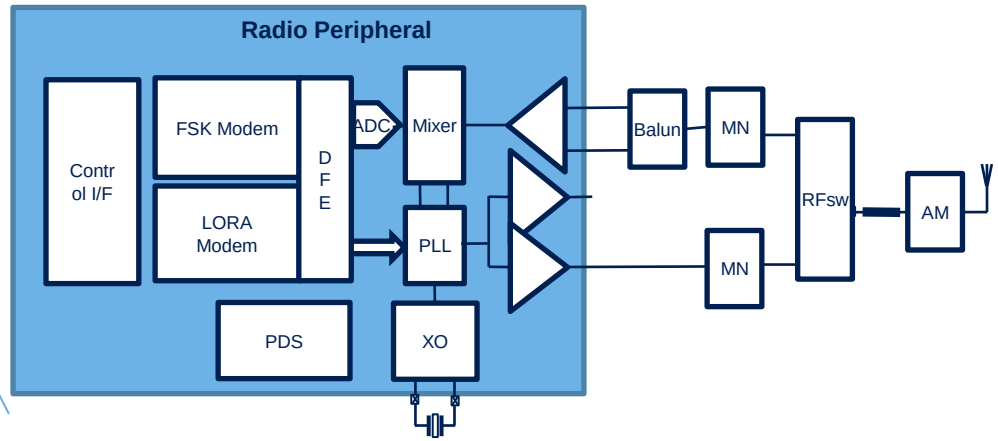
- Debug Cross trigger unit, dual core CPU debug.
- Integrated SMPS to supply Core and sub-GHz radio.
- Dedicated package pins



Other packages show the same dedicated pins.

STM32WL RF transceiver

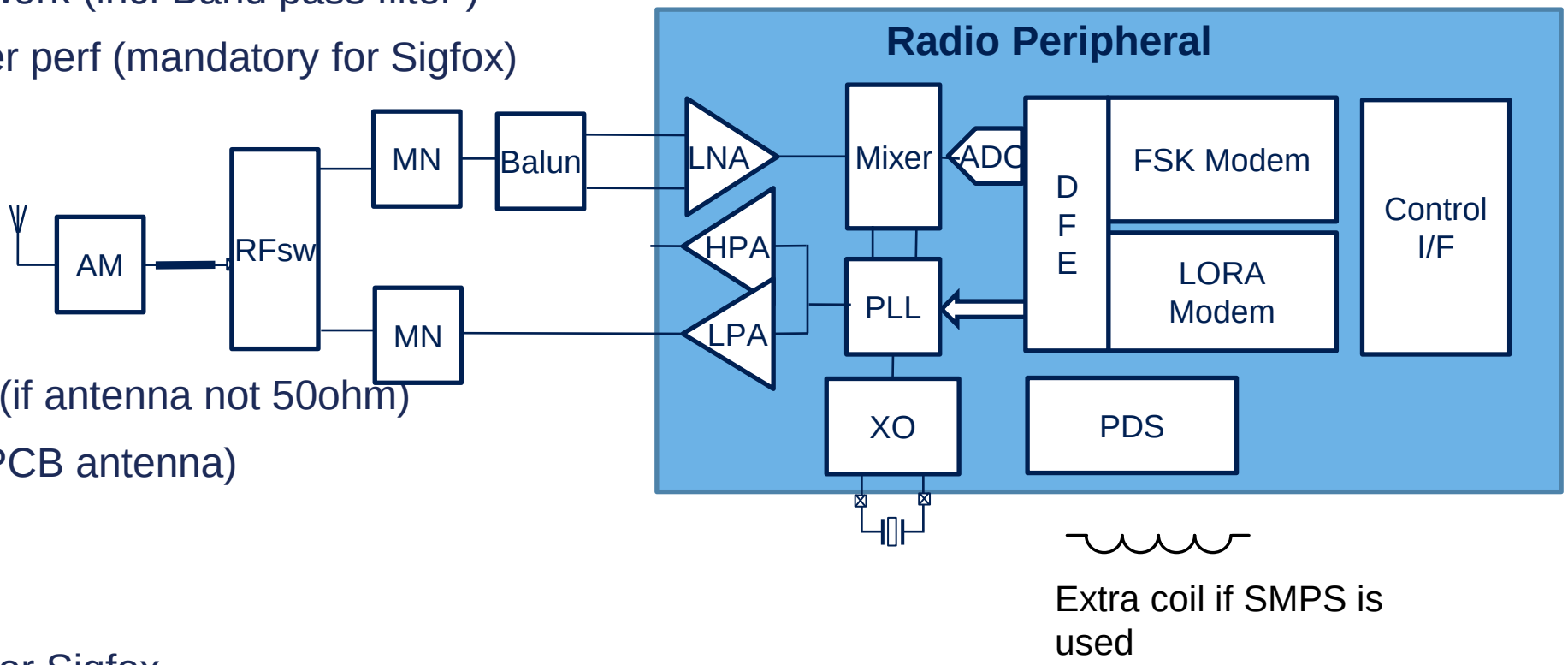




- TRX: ISM band 150 – 960 MHz,
- LoRa™, from 0.013 to 17.4 kbps
- (G)FSK, from 0.6 to 300 kbps
- (G)MSK, from 0.1 to 10 kbps
- Sigfox BPSK, from 100 bps to 600 bps
- Oscillator (HSE&RFPLL source),
- Shared power management, ultra low power,
- SPI securable command base interface
- Radio Interrupt,
- Radio operating mode independent from CPU,
- High output power up to +22 dBm

Typical RF BOM

- RF
  - Balun to convert from unbalanced to balanced in Rx
  - MN: Matching Network (inc. Band pass filter)
  - RF Switch for better perf (mandatory for Sigfox)



  - Antenna matching (if antenna not 50ohm)
  - Antenna (may be PCB antenna)

- Oscillator
  - TCXO mandatory for Sigfox
  - XO option for LoRa

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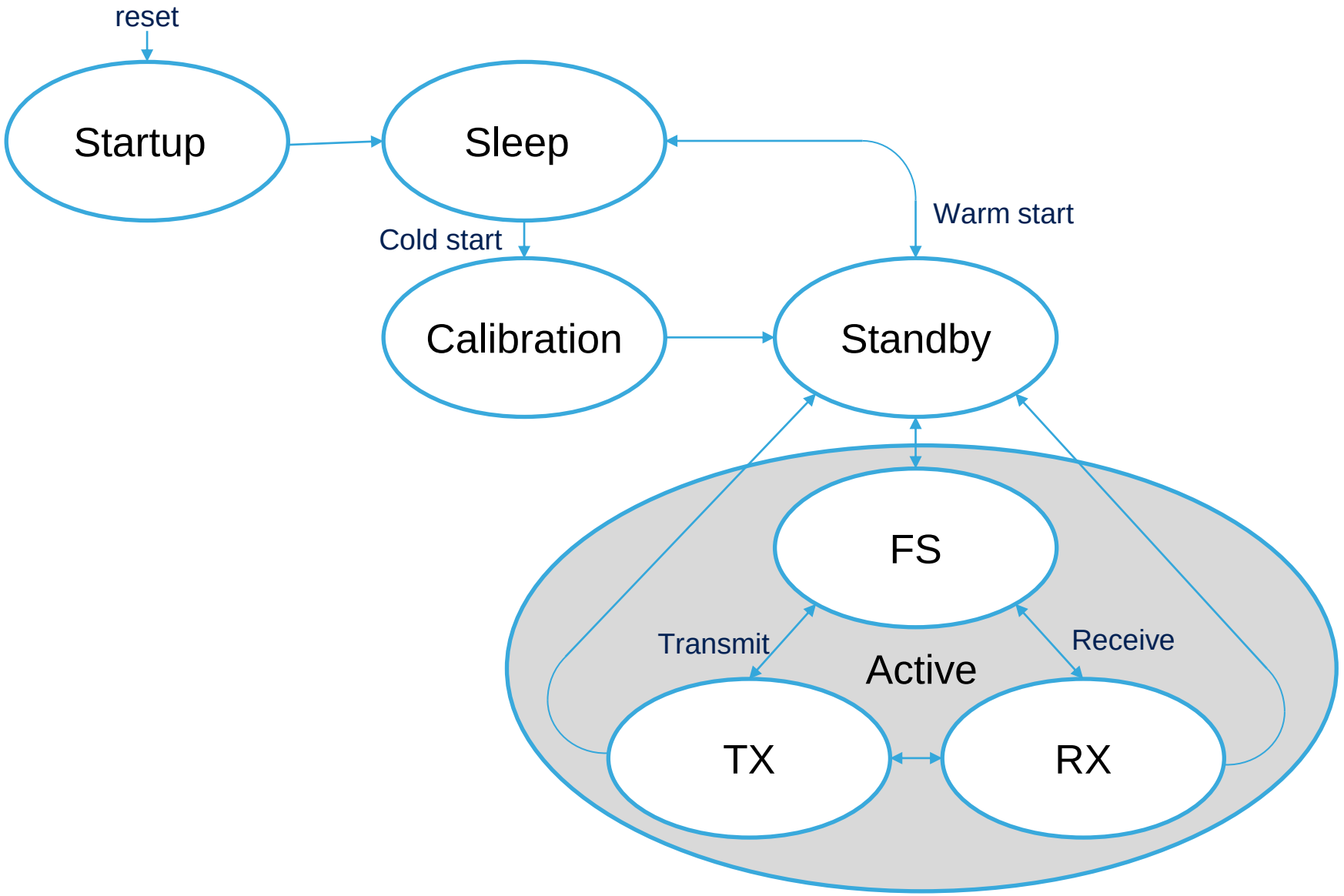
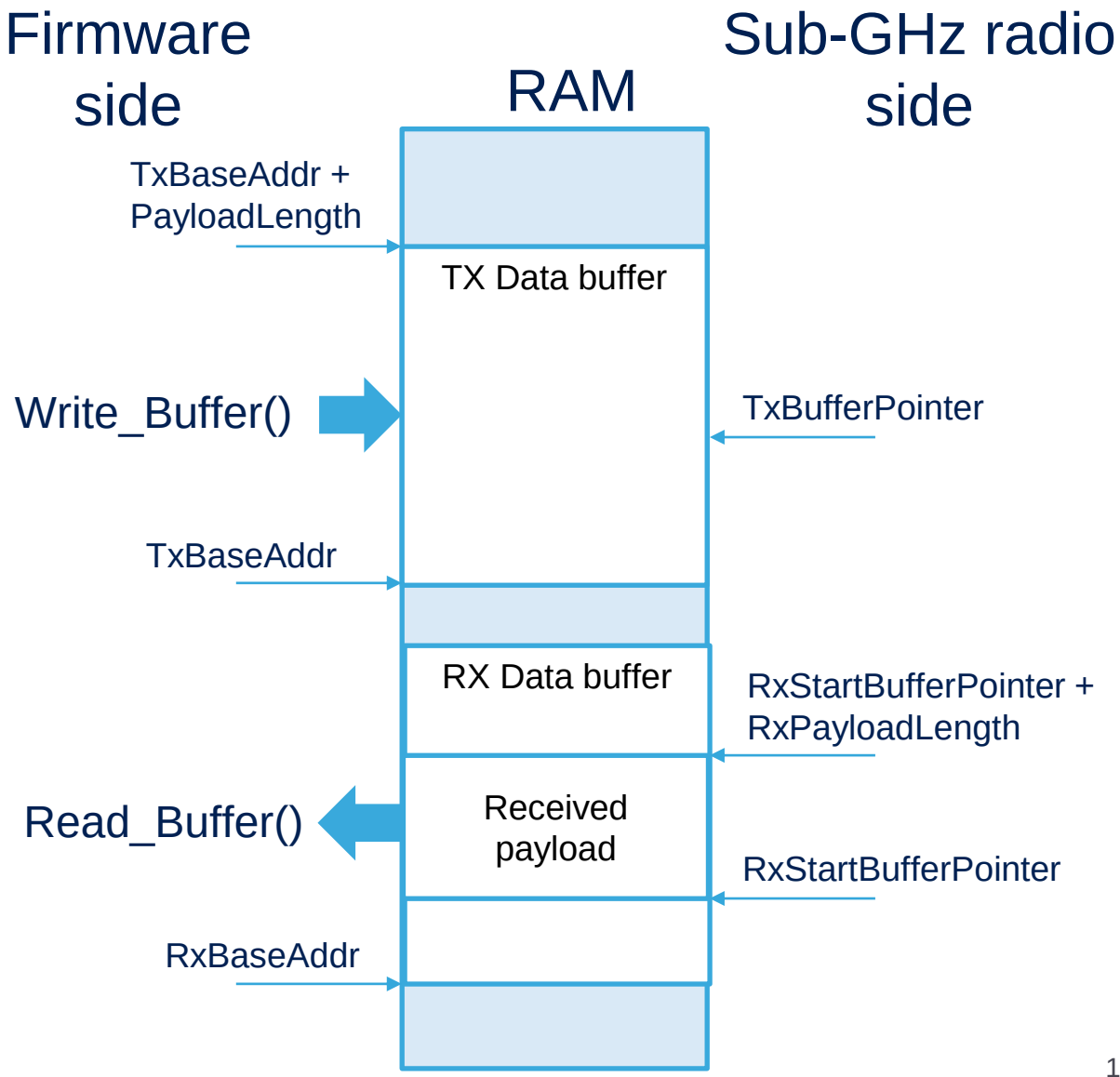
Finite State Machine of STM32WL TRX

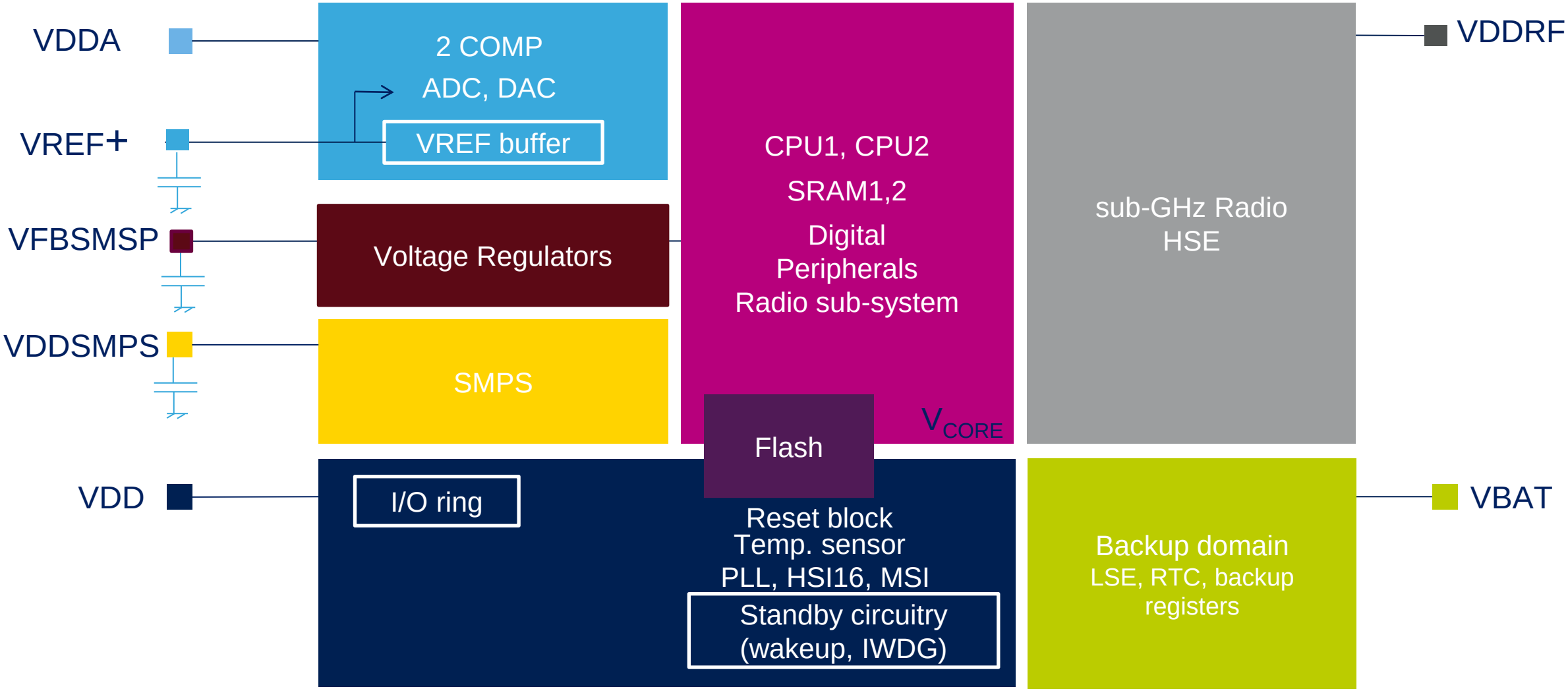


Data buffer

- A 256 bytes RAM
- TX data buffer
  - Written by firmware, read by hardware
  - Parameters:
    - TxBaseAddr,
    - TxBufferPointer
    - PayloadLength
- RX data buffer
  - Written by hardware, read by firmware
  - Parameters:
    - RxBaseAddr,
    - RxStartBufferPointer
    - RxPayloadLength



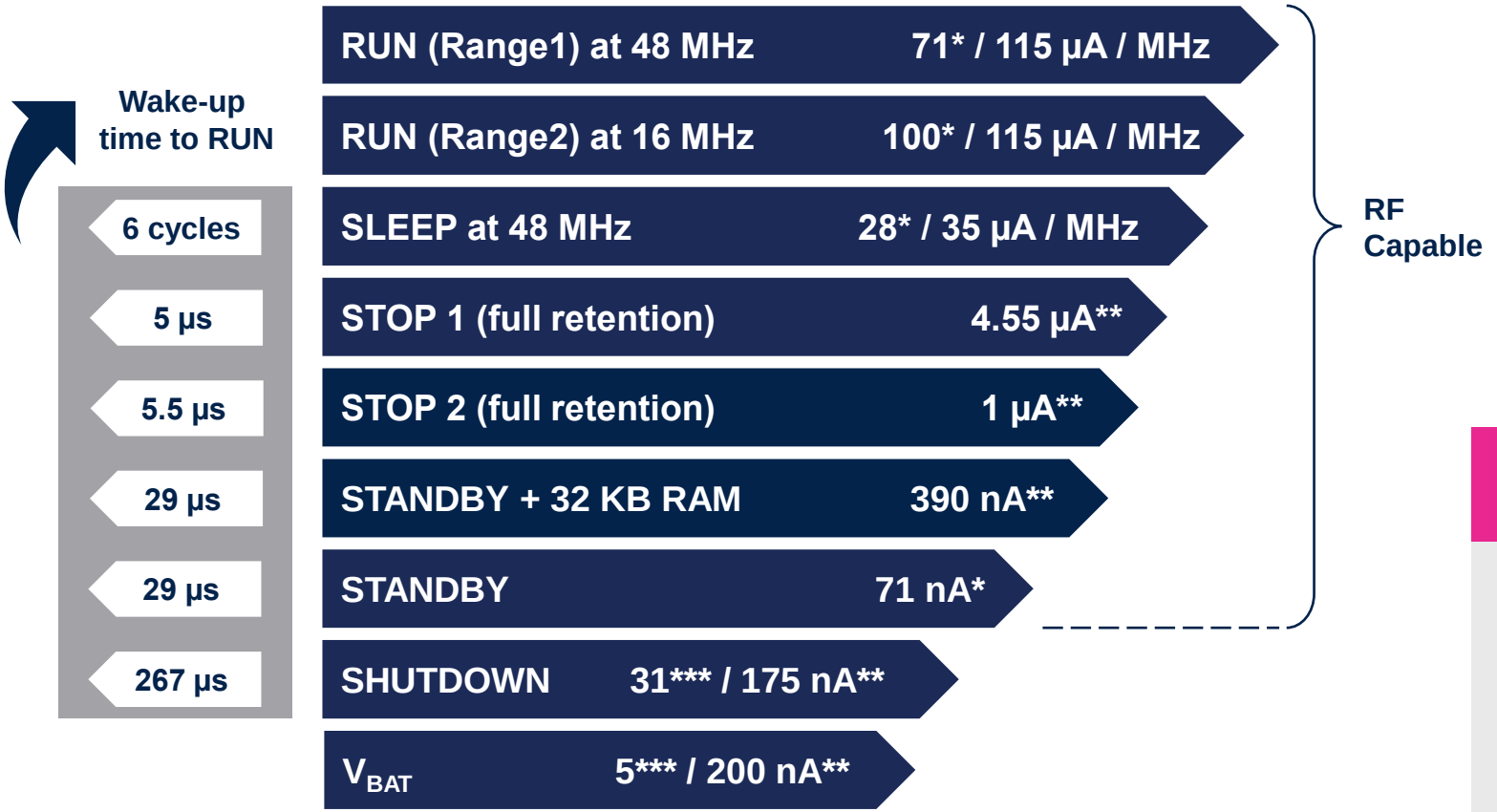
Power schemes



V_{DD} , V_{DDSMPS} , V_{DDRF} : 1V71 ... 3V6 ; 1V95 min, for SUBGHZ RF operation
V_{FBSMPS} regulated 1.5 V
V_{DDA} from 1.62 to 3.6 V
V_{BAT} from 1.55 to 3.6 V including the RTC and backup registers

PWR

Typ with LDO @ V_{DD} = 3 V @ 25 °C



* Typical values with SMPS, **RF OFF**
** with RTC on LSE Bypass
*** All OFF

Benchmark scores

- High Efficiency
  - ➔ CoreMark score = 162
- Ultra Low-Power Platform
  - ➔ ULPBbench score ≈ 204

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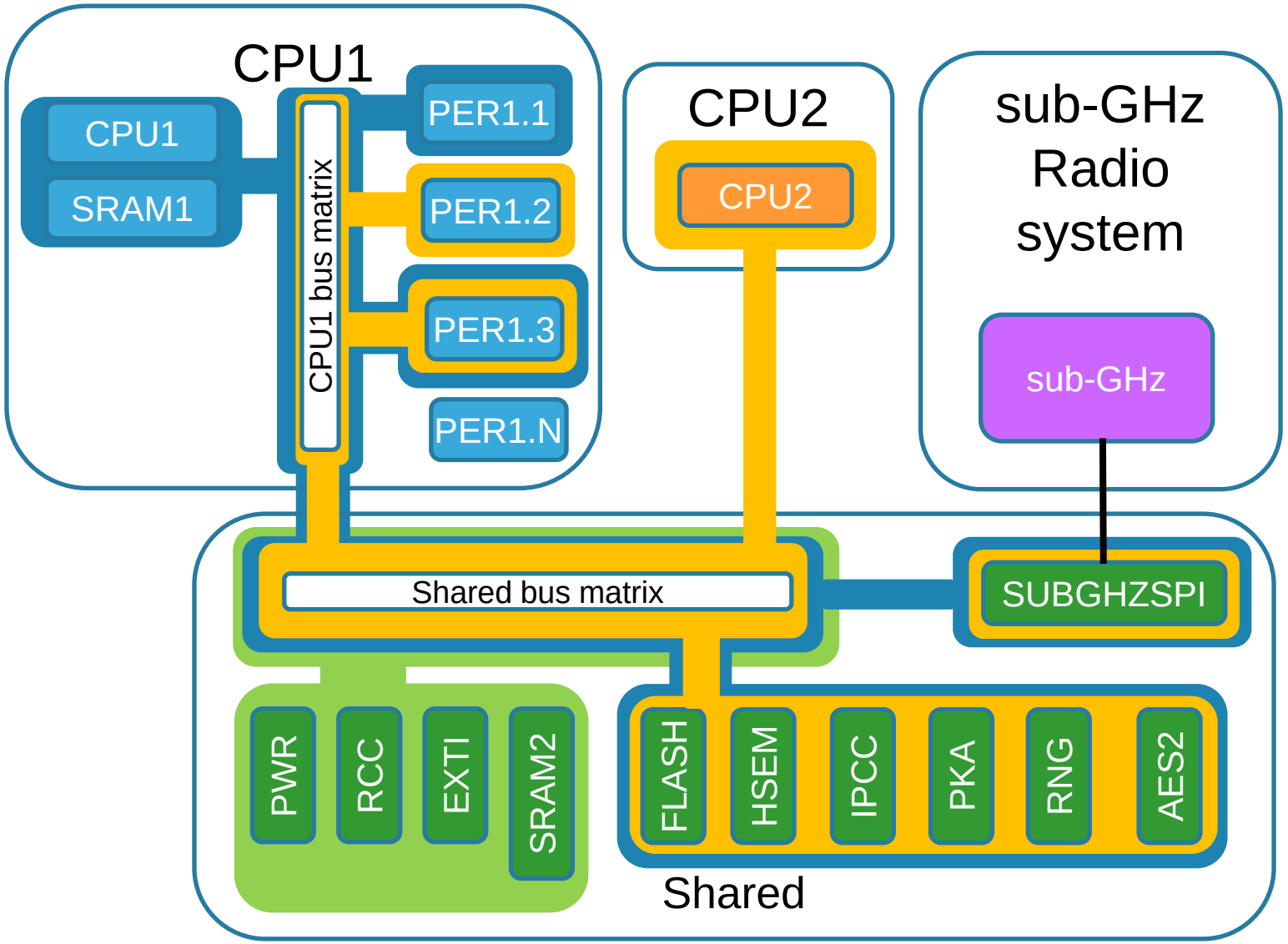
PWR / RCC



- 3 sub-systems
  - CPU1 Corex-M4 (Blue)
  - CPU2 Cortex-M0+ (Orange)
  - Radio system (Violet)
- Always clocked (Green)
- Independent operating modes
  - CRun
  - CSleep
  - CStop
- CPU peripheral allocation by enable bits in RCC

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CPU sharing PWR modes: automatic management

- Each CPU can decide independently which system low-power mode to use (Stop0, Stop1, Stop2, Standby, or Shutdown).
- Each CPU can decide which wakeup source will wake it up.
- When both CPUs enter WFI and/or WFE the HW mechanism executes the compatible request. It selects the highest low-power mode compatible with the two CPU requirements.
- One CPU can wake up without the need to wake up the other one.
  - When the STM32WL5 wakes up from Stop modes, according the wakeup source, only the CPU registered for this wakeup source is restarted, the other one stays in WFI (or WFE) with its clock stopped.
  - When the STM32WL5 wakes up from Standby modes, according with the source, only the CPU registered for this wakeup source is restarted, the other one stays under reset mode.

SUBGHZ / PWR

SUBGHZ automatic PWR mode management

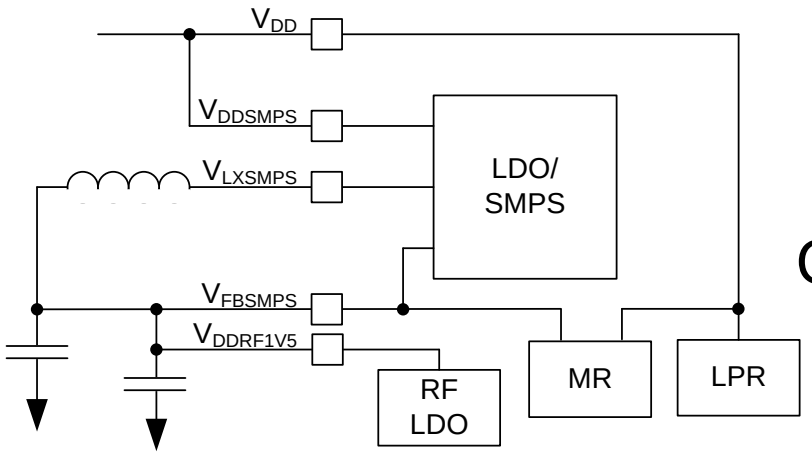
- The sub-GHZ radio can autonomously enter and exit its peripheral low-power modes.
- The sub-GHz radio can be woken-up by the sub-GHz radio low-power timer and by a CPU.
- The sub-GHz radio does not impact the CPUs/system low power modes. The sub-GHz radio may be active even when the system is in Stop or Standby mode.
- The sub-GHz radio can wakeup a CPU and the system from Stop and Standby modes with its wakeup interrupt.

- Performance with SMPS
  - By adding an external coil the SMPS is used to lower power consumption,
  - The SMPS is used to step down the V_{DD} supply and supplies digital core and SUBGHZ (typ. 1V5),

- Low cost using only LDOs
  - By not connecting the coil the SMPS mode can’t be used. The LDOs are directly supplied from V_{DD}. Saving the cost for the coil at the expense of increasing the overall power consumption.

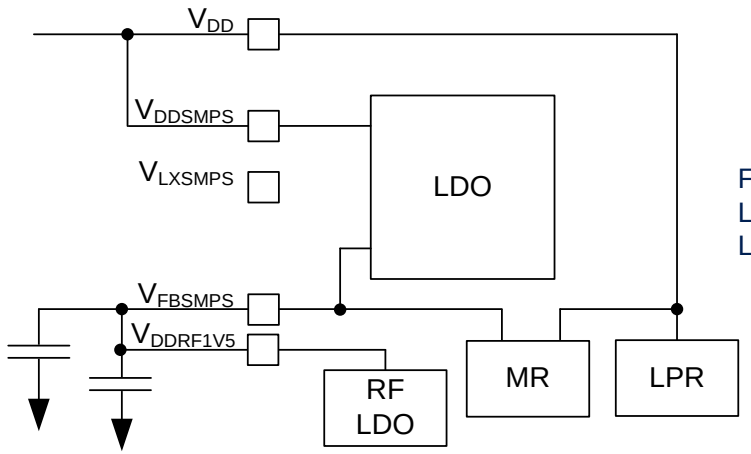
SMPS configuration

Full Vdd range [1.62..3.6V]
High efficiency SMPS



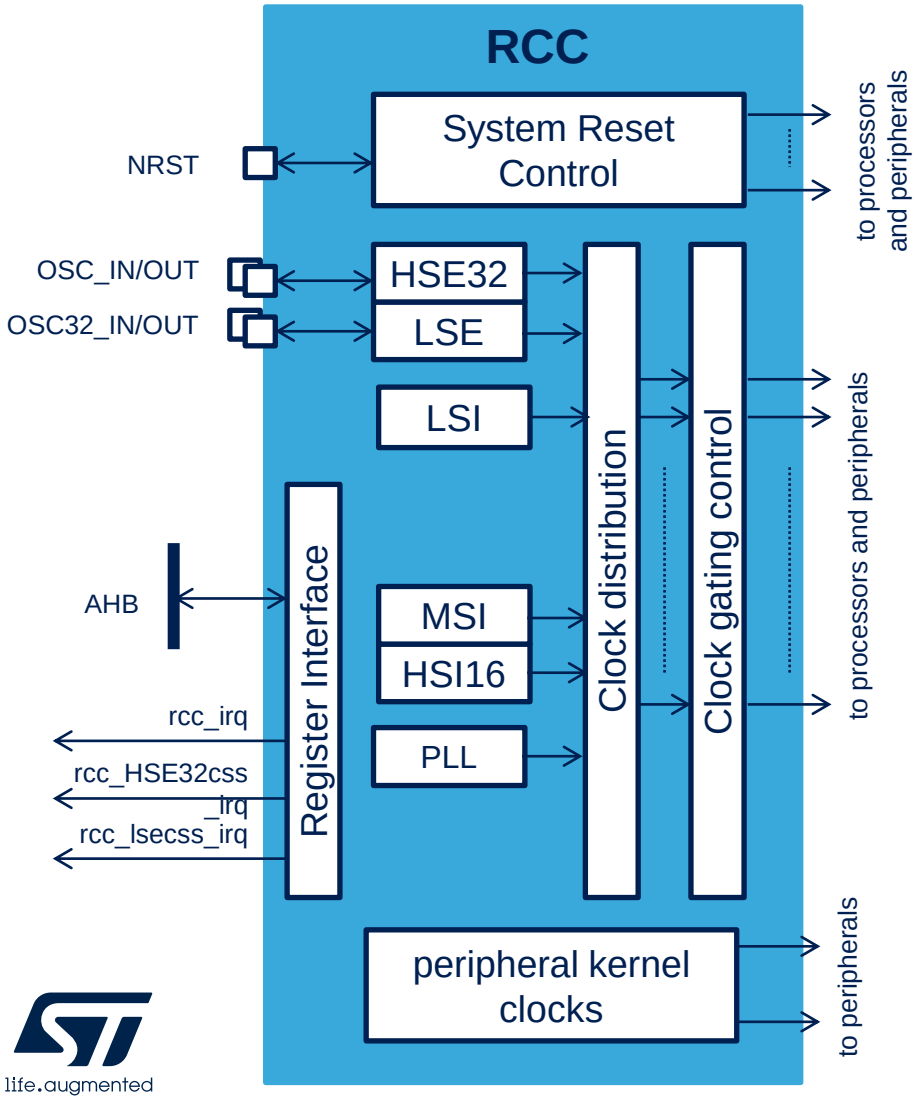
Or

LDO configuration



Full Vdd range [1.62..3.6V]
Low BOM
Low noise

RCC



- The Reset and Clock Controller (RCC) manages:
  - The generation of all the clocks,
    - CPU1, CPU2 and bus matrix
    - Peripheral kernel clocks
    - PLL, RC oscillators, and crystal oscillators…
  - The gating of all the clocks,
  - The control of all the system and peripheral resets.

Application benefits

- High flexibility in choice of clock sources to meet consumption and accuracy requirements.
- Independent clock control for CPU1, CPU2 sub-systems
- Safe and flexible reset management

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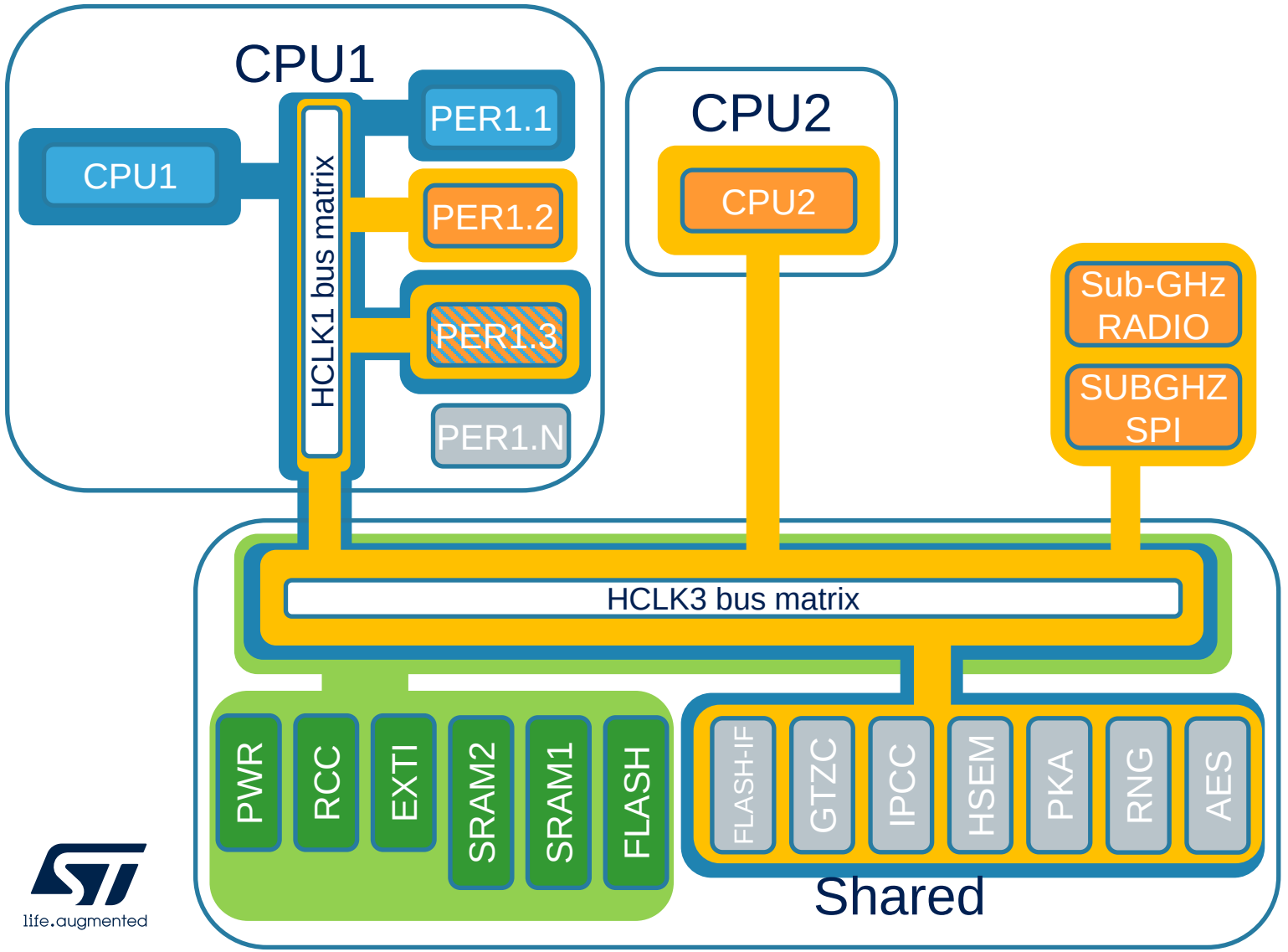
Most peripheral bus and kernel clocks can be **individually enabled per CPU**.The RCC_AHBxENR and RCC_APBxENRy registers enable peripheral clocks for CPU1. RCC_C2_AHBxENR and RCC_C2_APBxENR registers enable peripheral clocks for CPU2.

RCC / PWR



- System peripherals:
  - PWR, RCC, EXTI, FLASH, SRAM1 and SRAM2
  - Active with both CPUs.
- Allocated peripherals: CPU1 CPU2
  - Flash interace, IPCC, PKA, RNG, AES2, SUBGHZSPI, PERn.m
  - Need allocation for CPU1 and CPU2
- De-located peripherals
- Only needed CPU, bus matrix and peripheral clocks will be active.

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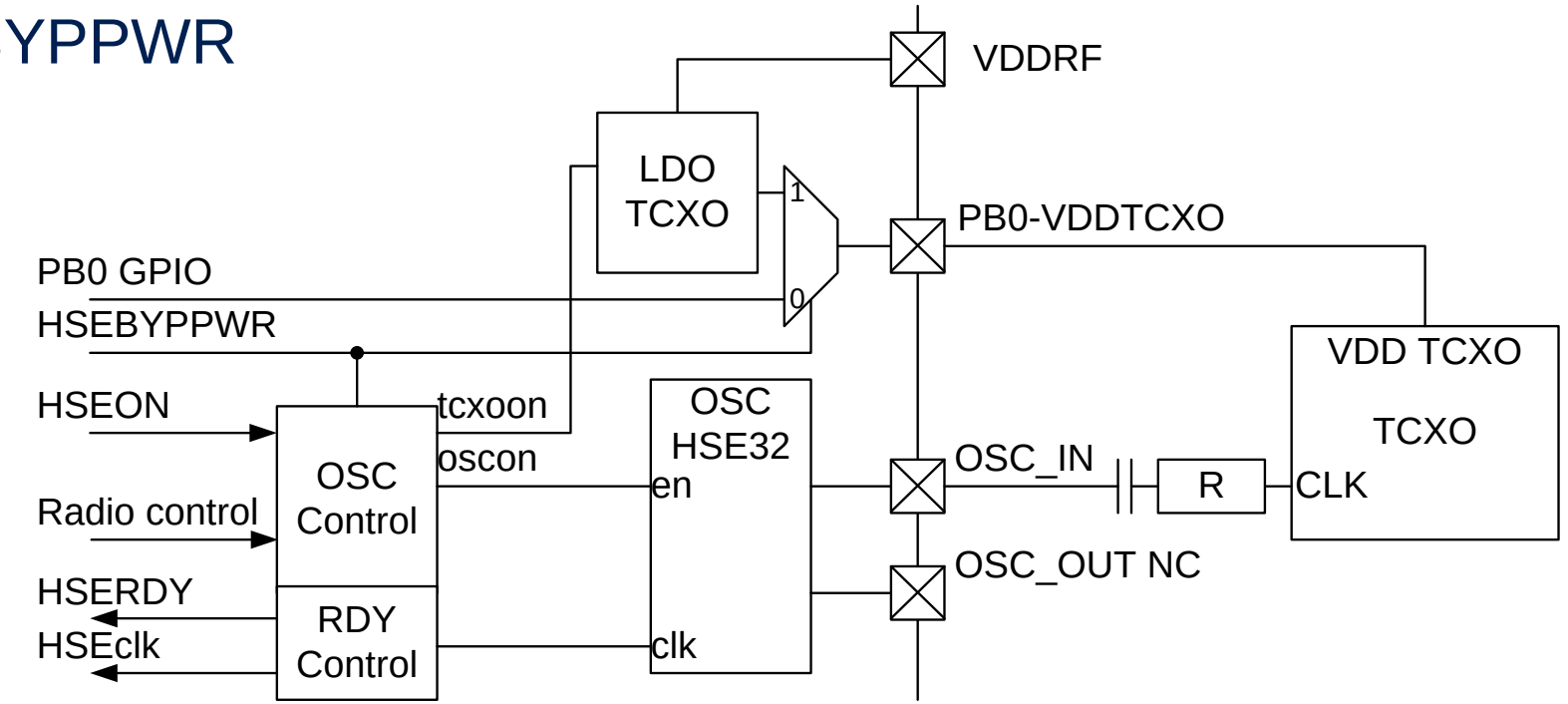
Temperature compensated crystal oscillator

- External TCXO
- Supply provided through PB0-VDDTCXO pin
- Selected by HSEBYPPWR



32kHz LSI with trimming capability

- The ultra-low-power LSI (available in all modes except Shutdown and VBAT)
  - It can be used for RTC, LPTIMs, and IWDG. (Must not be used for the radio system)
  - Application trimming with HSE32 using bits TIM16.

	LSI 32 kHz
Accuracy (typ.)	Initial: ± 1.6 %
	Over-temperature: ± 1.5 %
	Over VDD: +0.1 / -0.2%
Consumption (typ.)	110 nA

Autonomous radio operation

- The Radio system is capable to operate autonomously, without the CPU.
  - Directly manages the HSE32 clock sources.
- Clocks needed for the Radio system are automatically enabled.
  - The radio internal and external system clock

Thank you

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