

COL216 LAB 2B - ALU

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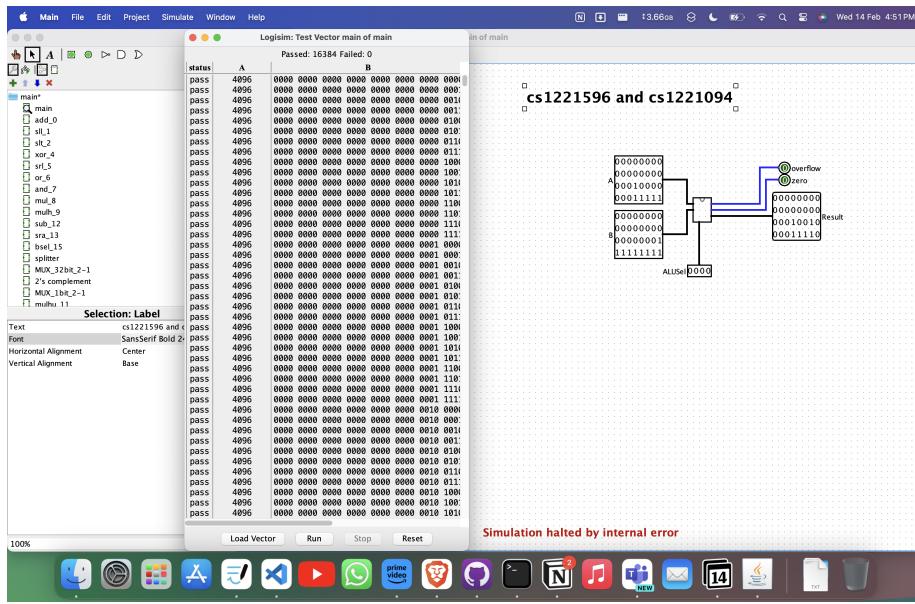
15th February 2024

1 Introduction

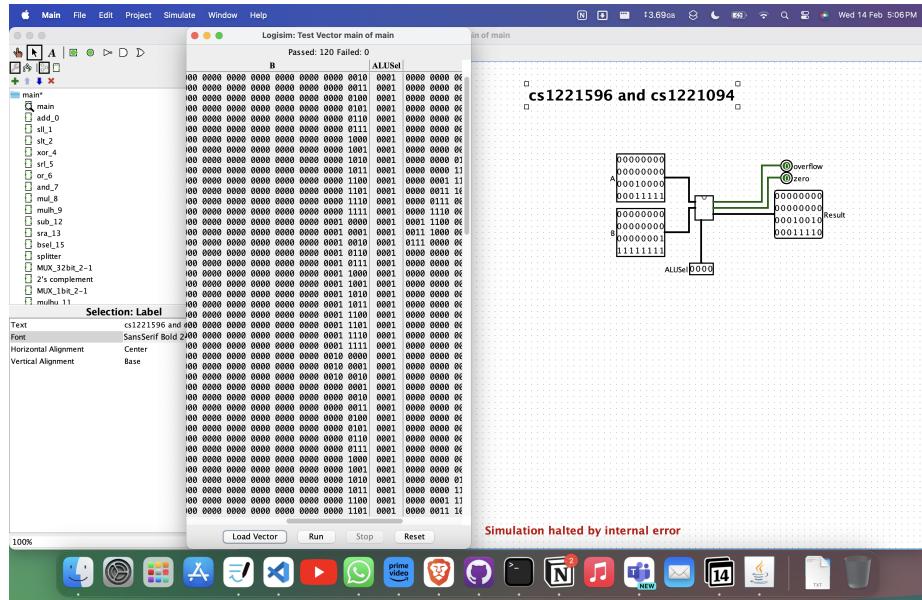
In this task, we made an arithmetic logic unit which supports all operations needed by instructions in ISA. We ignore overflow as RISC-V does with unsigned instructions. The operations as mentioned below have been implemented in the `alu.circ` (`main.circ`) file.

2 Instructions implemented in ALU

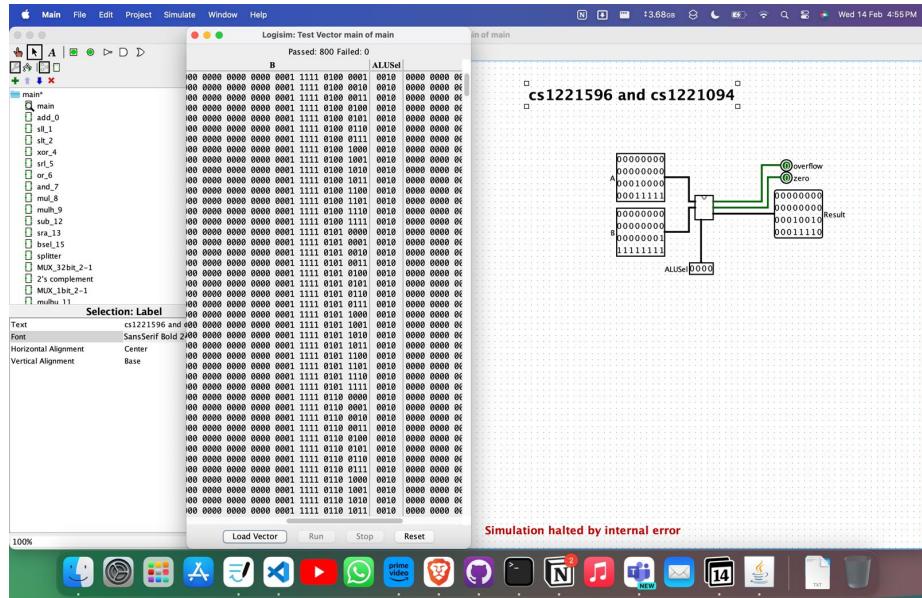
2.1 add



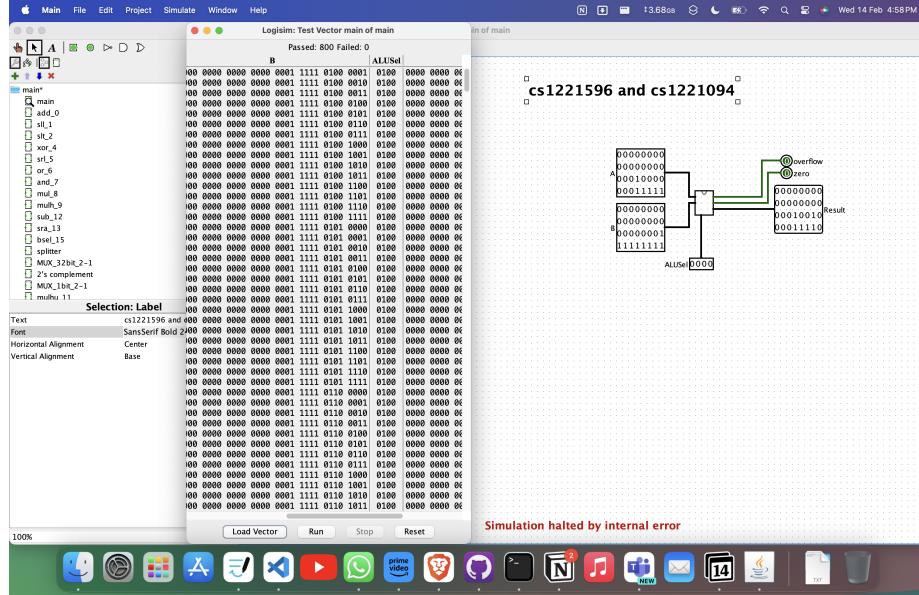
2.2 sll



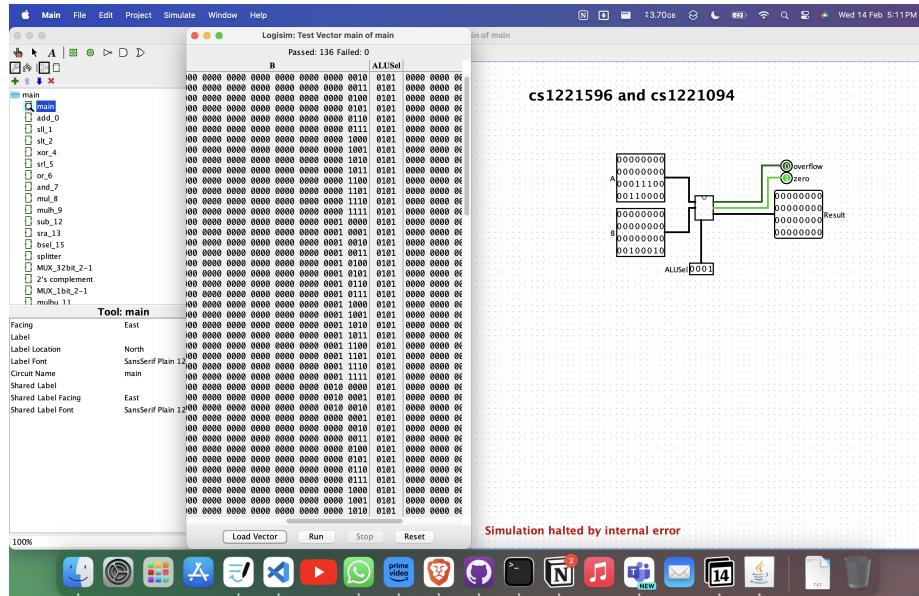
2.3 slt



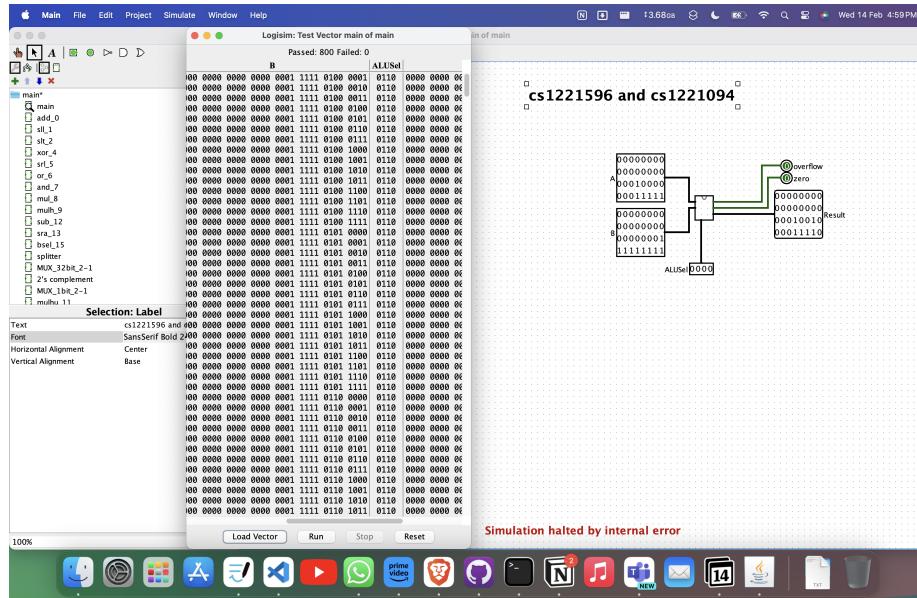
2.4 xor



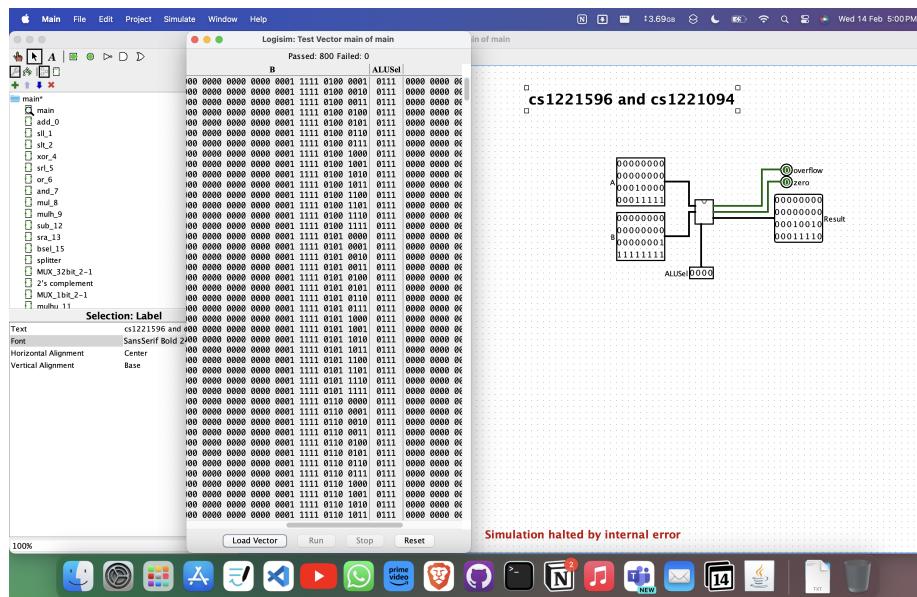
2.5 srl



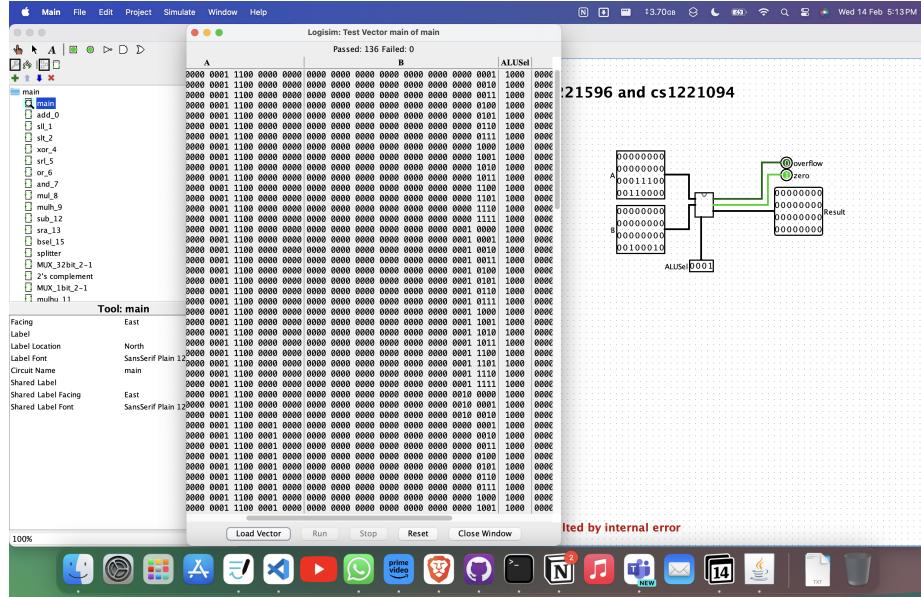
2.6 or



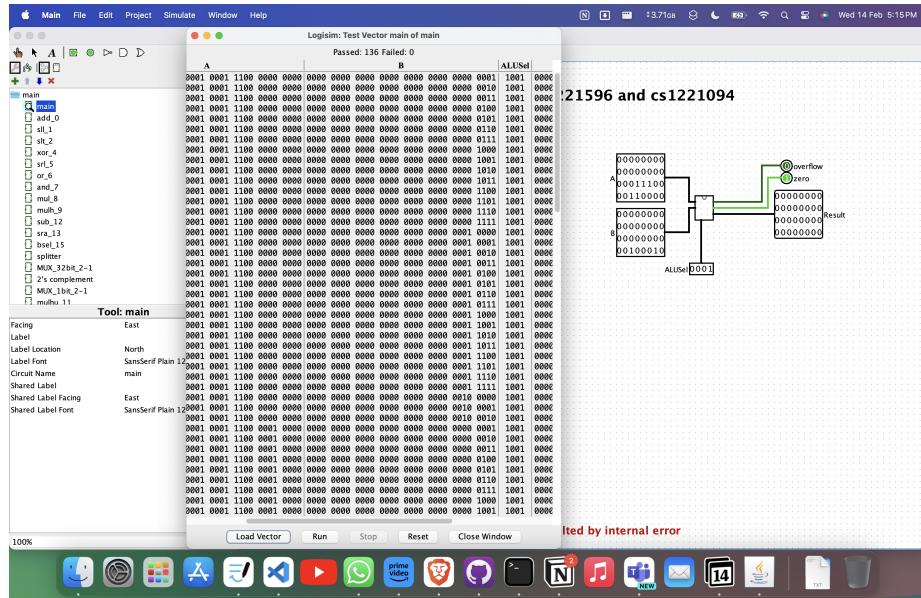
2.7 and



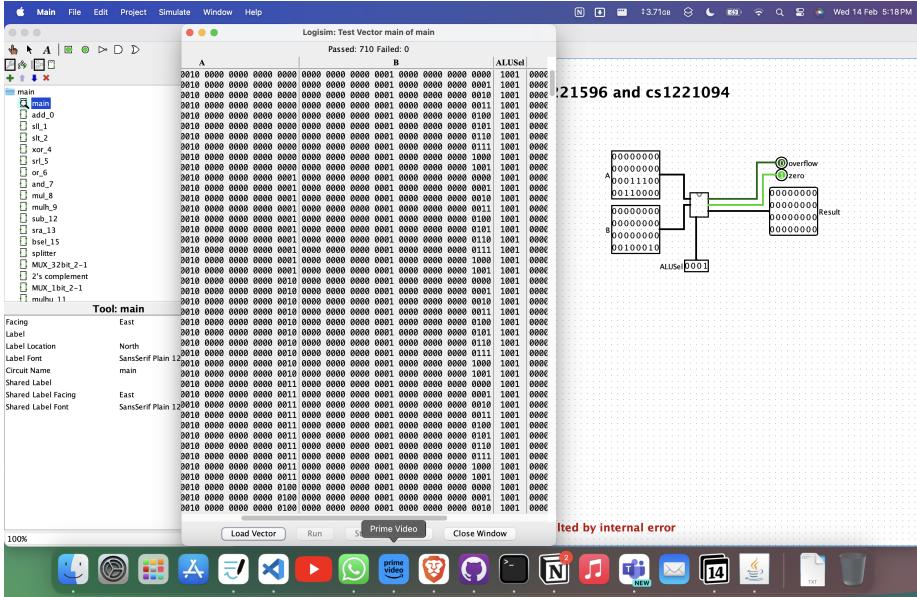
2.8 mul



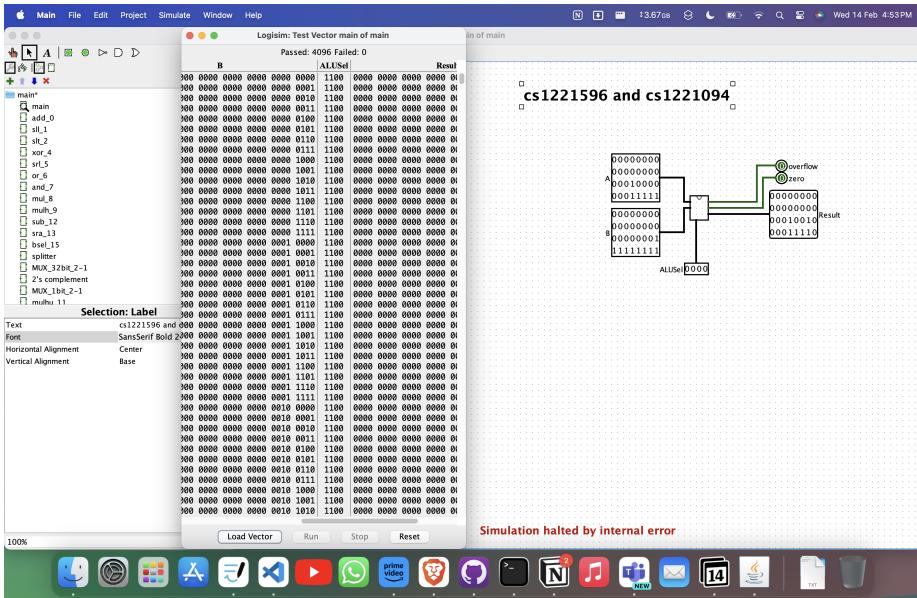
2.9 mulh



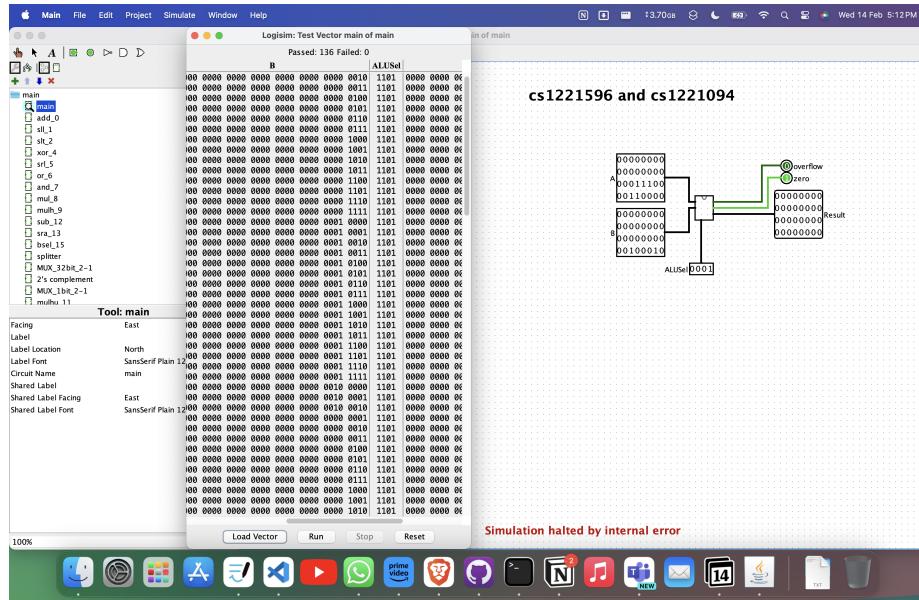
2.10 mulhu



2.11 sub



2.12 sra



2.13 bsel

