COL216 LAB 2C - REGISTER FILE

Jahnabi Roy and Abhinav Rajesh Shripad

22^{nd} February, 2024

1 Register File

In this part, we made a register file circuit and tested it on logisim via the clock ticks enabled feature (simulation). For testing, logging was used to record the *test_vectors* loaded manually and is attached along with the submission. Clock is tick enabled and is thus working for the entire duration of testing.

1.1 Exception Handling

To handle the mentioned exception of zero register, we have set the value of register zero to 0 and adjusted the RegWEn signal accordingly; thus not changing its value. The attached screenshot shows the working of the aforementioned situation.

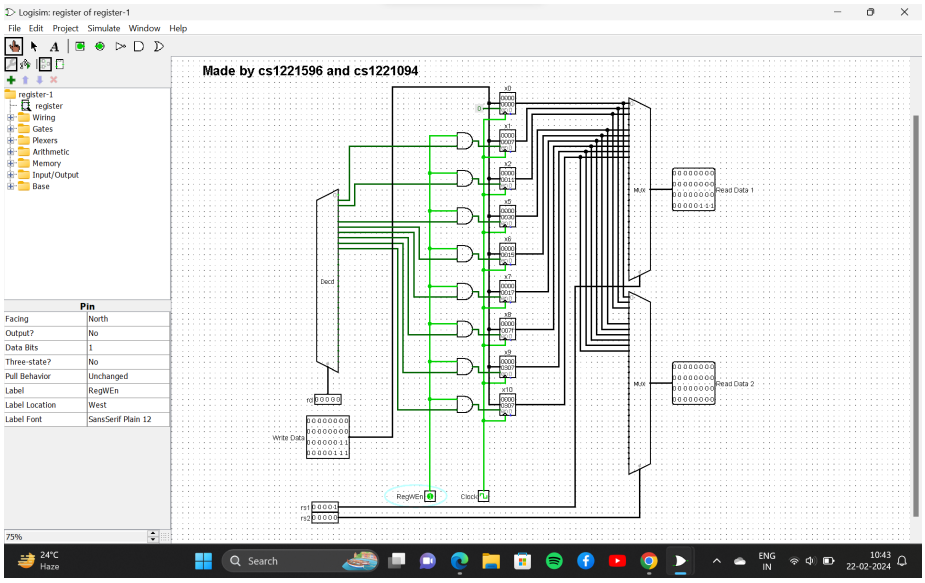


Fig. *Attempting to write into the x0 register.*

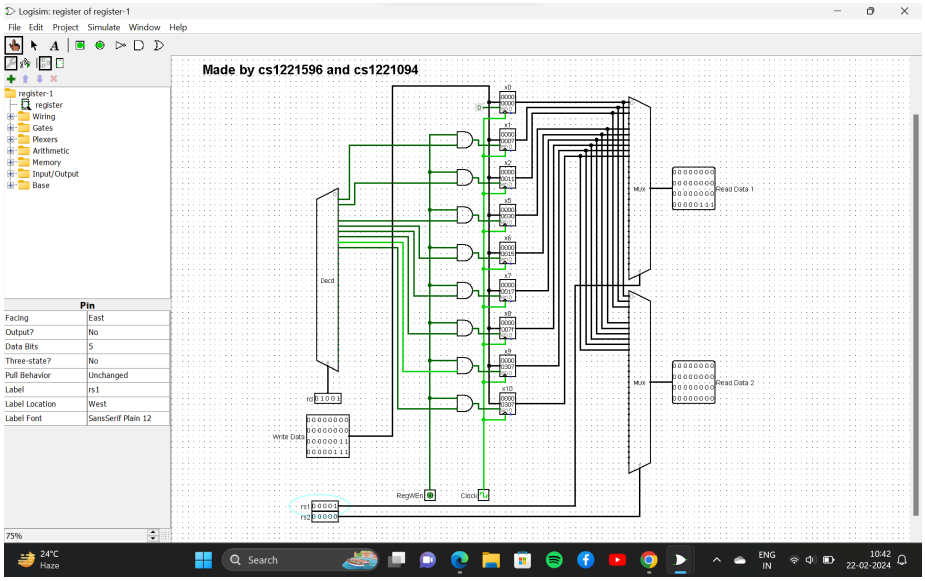
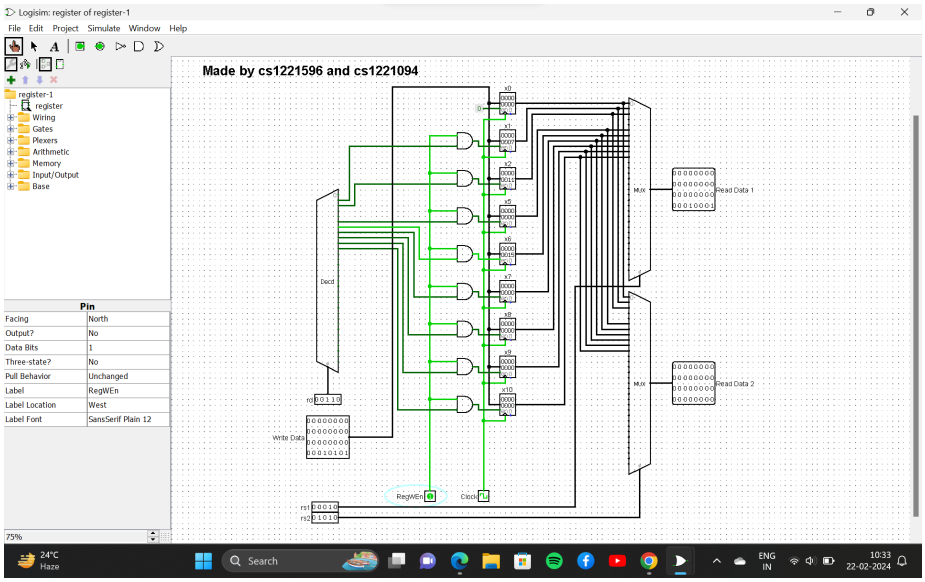
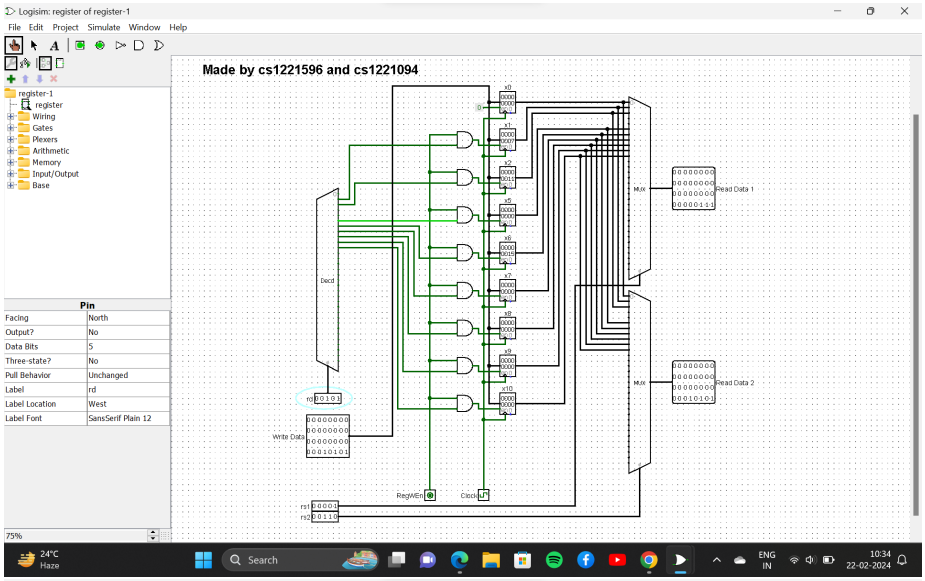


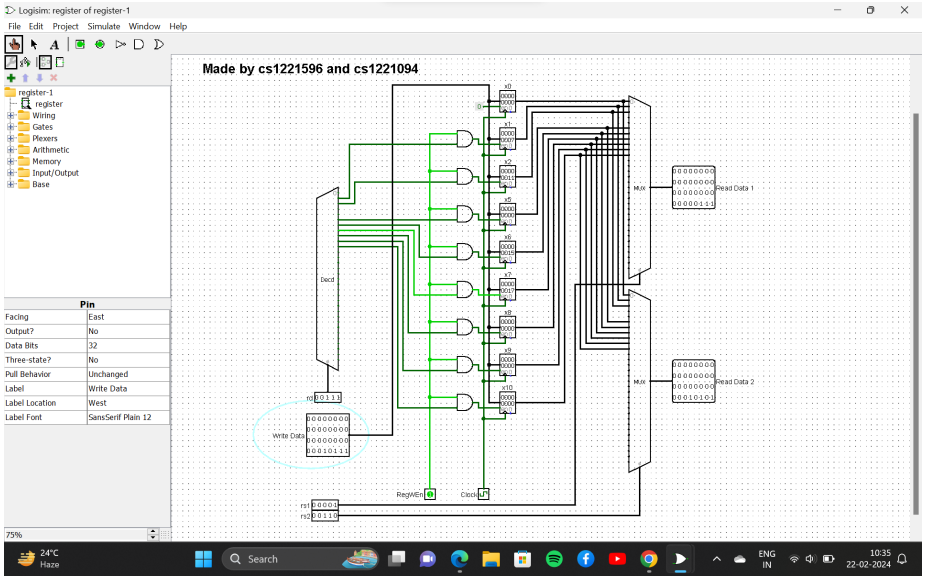
Fig. *The value of x0 shown as read after the above operation.*

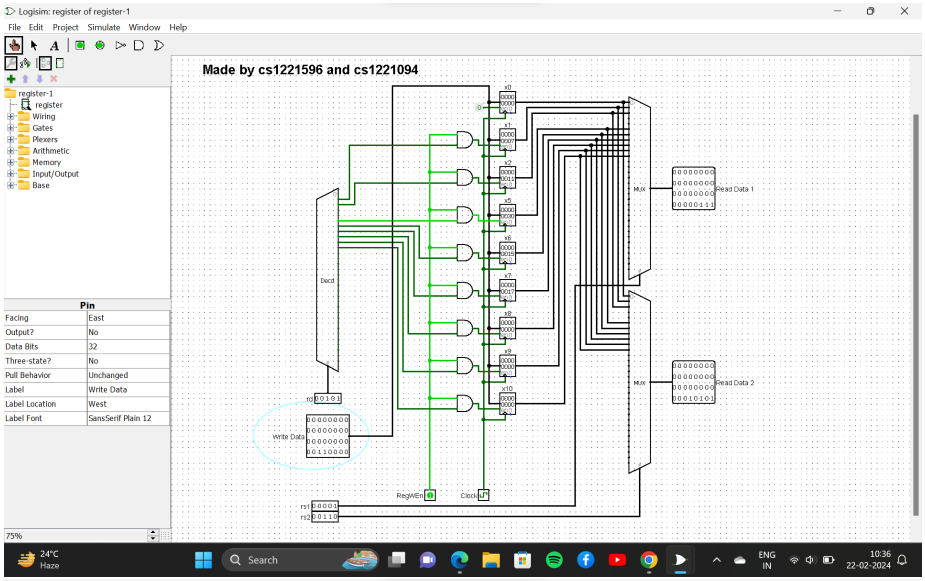
1.2 General cases

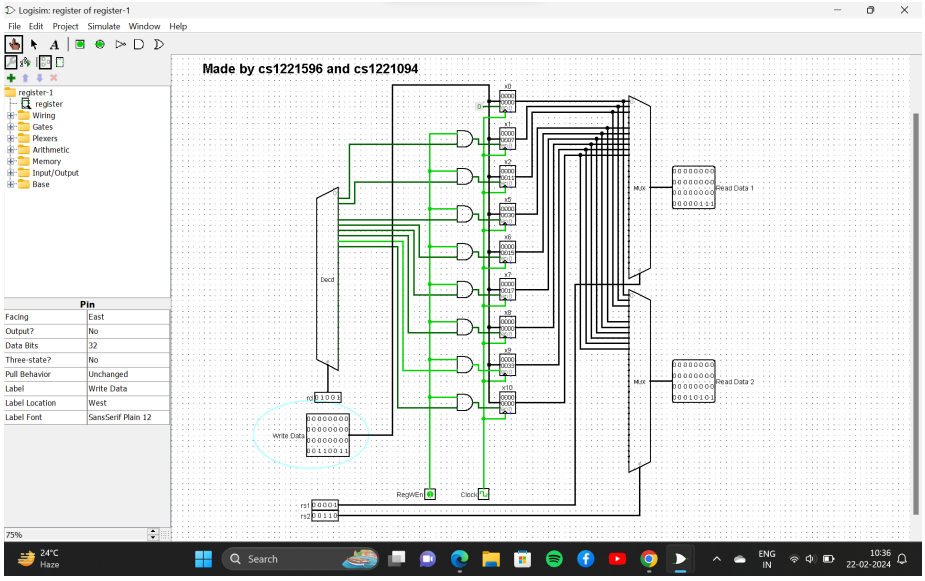
The following screenshots show the general working of the circuit; action triggered at rising edge of the clock and RegWEn signal managing the data written into the respective specified registers.

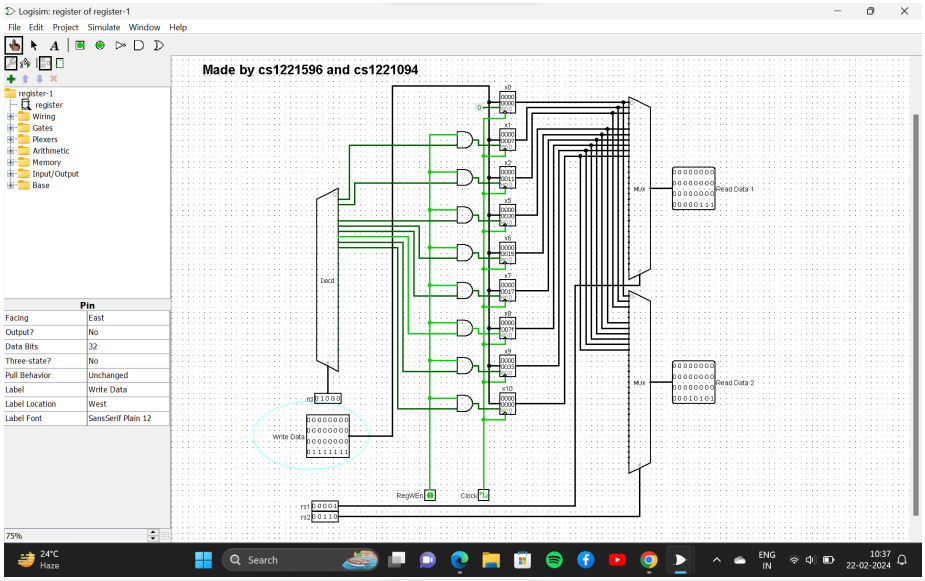


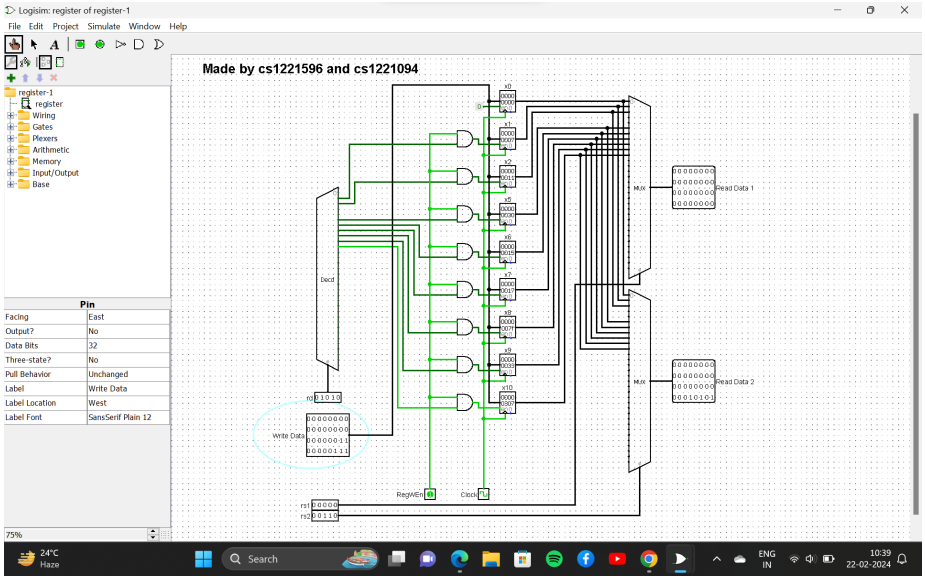

Logisim: register of register-1
File Edit Project Simulate Window Help
Made by cs1221596 and cs1221094
register-1
register
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing North
Output? No
Data Bits 5
Three-state? No
Pull Behavior Unchanged
Label rd
Label Location West
Label Font SansSerif Plain 12
Decd
MUX
Read Data 1
Read Data 2
Write Data
RegWEn
Clock
75%
24°C
Haze
Search
ENG
IN
10:34
22-02-2024

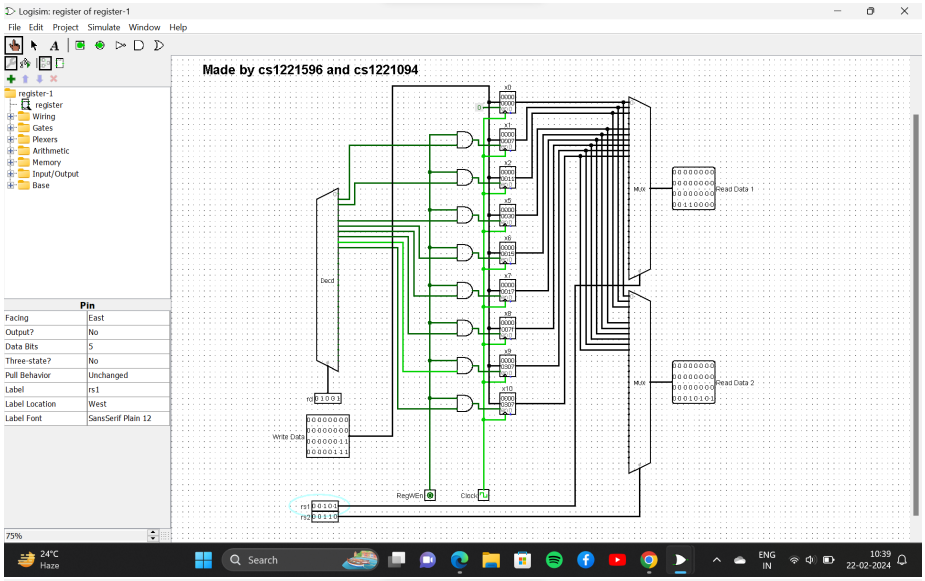

Logisim: register of register-1
File Edit Project Simulate Window Help
Made by cs1221596 and cs1221094
register-1
register
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 32
Three-state? No
Pull Behavior Unchanged
Label Write Data
Label Location West
Label Font SansSerif Plain 12
Decd
MUX
Read Data 1
Read Data 2
Write Data
RegWEn
Clock
75%
24°C
Haze
Search
ENG
IN
10:35
22-02-2024

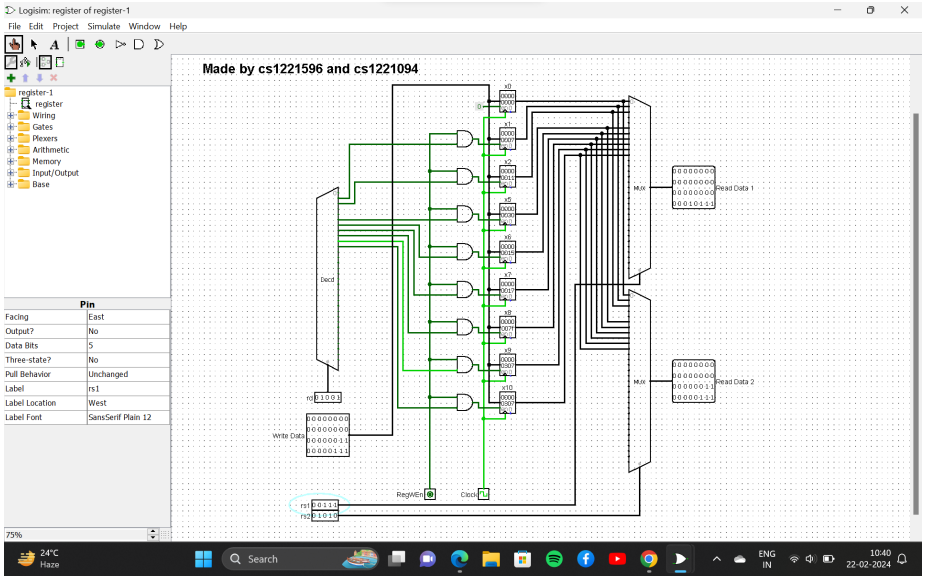

Logisim: register of register-1
File Edit Project Simulate Window Help
Made by cs1221596 and cs1221094
register-1
register
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 32
Three-state? No
Pull Behavior Unchanged
Label Write Data
Label Location West
Label Font SansSerif Plain 12
Decd
MUX
Read Data 1
Read Data 2
Write Data
RegWEn
Clock
rs1
rs2
75%
24°C
Haze
Search
ENG
IN
10:36
22-02-2024


Logisim: register of register-1
File Edit Project Simulate Window Help
Made by cs1221596 and cs1221094
register-1
register
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 32
Three-state? No
Pull Behavior Unchanged
Label Write Data
Label Location West
Label Font SansSerif Plain 12
Decd
MUX
Read Data 1
Read Data 2
Write Data
RegWEn
Clock
rs1
rs2
75%
24°C
Haze
Search
ENG
IN
10:36
22-02-2024


Logisim: register of register-1
File Edit Project Simulate Window Help
Made by cs1221596 and cs1221094
register-1
register
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 32
Three-state? No
Pull Behavior Unchanged
Label Write Data
Label Location West
Label Font SansSerif Plain 12
Decd
MUX
Read Data 1
Read Data 2
Write Data
RegWEn
Clock
75%
24°C
Haze
Search
ENG
IN
10:37
22-02-2024


Logisim: register of register-1
File Edit Project Simulate Window Help
Made by cs1221596 and cs1221094
register-1
register
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 32
Three-state? No
Pull Behavior Unchanged
Label Write Data
Label Location West
Label Font SansSerif Plain 12
Decd
MUX
Read Data 1
Read Data 2
Write Data
RegWEn
Clock
75%
24°C
Haze
Search
ENG
IN
10:39
22-02-2024


Logisim: register of register-1
File Edit Project Simulate Window Help
Made by cs1221596 and cs1221094
register-1
register
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 5
Three-state? No
Pull Behavior Unchanged
Label rs1
Label Location West
Label Font SansSerif Plain 12
75%
Decd
MUX
Read Data 1
Read Data 2
Write Data
RegWEn
Clock
24°C
Haze
Search
ENG
IN
10:39
22-02-2024


Logisim: register of register-1
File Edit Project Simulate Window Help
Made by cs1221596 and cs1221094
register-1
register
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 5
Three-state? No
Pull Behavior Unchanged
Label rs1
Label Location West
Label Font SansSerif Plain 12
75%
Decd
MUX
Read Data 1
Read Data 2
Write Data
RegWEn
Clock
24°C
Haze
Search
ENG
IN
10:40
22-02-2024