ELET2570 – Assignment 2

Due: March 12, 2021 at 11:59 p.m.

Making an ALU – Part II

In this exercise you are required to write VHDL code to implement the Arithmetic-Logic Unit (ALU) that you constructed in Assignment 1.

The specifications for the ALU are as follows:

Input Width:	8 bits
Output Width:	8 bits
ALU Operations:	ADD, OR, EOR, NOT, ADD, SUBTRACT, MULTIPLY, COMPARE

The ALU must also have a status register that stores the following flags:

Negative, **Z**ero, **C**arry and O**V**erflow

Note: Your code should match your schematic from Assignment 1.

Submission:

You are required to submit one (1) file.

1. The finished VHDL code should be put in a PDF document and named as follows:

   FirstName.LastNameALUcode.**pdf**

The file should be uploaded to OURVLE by the time on the due date specified above.