Varun Haldiya

3rd Year Undergraduate B.E. (Hons.) Electrical Engineering (2013-2017)
Birla Institute of Technology and Science, Pilani 333031

Degree/Examination	Year	University/School	Grade/marks
(B.E. Hons.) Electrical and Electronics Engineering	2013-present	Birla Institute of Technology and Science, India	**9.44/10 (Current)**
All India Senior School Certificate Examination (Class XII)	2013	B.V.B Vidyashram, Jaipur, Rajasthan, India	**97%**
All India Secondary School Examination (Class X)	2011	B.V.B Vidyashram, Jaipur, Rajasthan, India	**10(CGPA)**

Courses completed / To be completed before Summer

Electrical Sciences, Electronic Devices, Digital Design, Microprocessors and Interfacing, Control Systems, Microelectronic Circuits, Signals and Systems, Analog and Digital VLSI Design, Digital Signal Processing, Computer Architecture, Operating Systems, Optimization, Communication Systems, Object Oriented Programming, Data Communication and Networks, Analog Electronics, Power Systems, Power Electronics, Electrical Machines, Electromagnetic Theory.

Internships/Assistantships

Teaching Assistant, Microprocessor and Interfacing (EEE F241), BITS Pilani. January 2016 –Present

Summer Intern, National Center for Antarctic and Ocean Research, Goa, India May 2015 - July 2015
Project Titled "Pixel based Spectral study of supraglacial lakes using Unsupervised and Supervised Clustering methods". Used Machine Learning Algorithms such as ISODATA, K-Means, Support Vector Machines, Min. Distance to Mean, Logistic Regression, Maximum Likelihood and applied them using MATLAB for detection of lakes from worldview-2 satellite imagery and then checked that the shape is preserved using control points and calculated the area and cross referenced it with the actual ground area.

Academic Projects

Detection of the needs of a Patient by Analyzing the P300 Wave from the EEG Signals generated by the brain using an FPGA. (In Progress)
Recording EEG waves from various subjects who are made to think about a need for example drinking water. Extraction of the P300 from the EEG. Analysis of the P300 and its classification based on a Machine Learning Algorithm. Testing the Algorithms on Test Set. Hardware Realization of the System Using a FPGA for portability and Faster Results.

Fast response system for medical emergencies in automobile accidents using vibration sensors and communication modules to alert ambulances and hospitals. (In Progress)
Sensing the vibration in the car and if above a certain threshold then sending a signal using a communication module to the medical response team along with the location of the accident
If the driver is safe he/she can press a button that would tell the medical team that their help is not needed now.

Smart Energy Meter with Instant Billing and Payment along with electricity theft detection. (In progress)
Measure the electricity bill of homes. Give the bill to the owner (via SMS) and the electricity corporation (via Internet).
Detect thefts in electricity and if found give its details to the electricity Board.
Make a system where the bill could directly be cut from salary or Users account.

Analyzing an ECG signal and stating whether a person is healthy or not by extracting the PQRS portion of the ECG signal.
Literature Review for various properties on an ECG Signal and how they can be used.
Extraction of QRS Width from the signal using Modified Pan-Tompkins Algorithm.
Extraction of R-peak and S-peak from the signal.
Comparing all the extracted values to predetermined values from literature to determine whether a person is healthy or not.

Material selection for Germanium/ III-V semiconductor CMOS Devices.
Determining as to why we need alternate materials for semiconductor devices. Reading literature to build a background of the domain. Applying TOPSIS approach for the selection of high-K gate oxides using various material properties such as Interface Trap Density States, Band Gap, Conduction Band Offset and Dielectric Constant. I've also written a paper on this under a professor which may get published soon.

Design of Digital Gates and Operational Amplifiers of the given specifications in Cadence Virtuoso.
Designing a 3 input XOR gate with a loading capacitance of 500fF and then testing using various tests such as DRC, LVS and PEX. Also designed a Folded cascode operational amplifier to meet a gain of 80dB, unity gain bandwidth of 100MHz and phase margin of 60 degrees.

Skills

Programming Languages – JAVA, Basics of C programming, Verilog
Software – MATLAB, Simulink, Cadence Virtuoso, LT Spice, Xilinx ISE, Proteus, MS-Office
Other skills- Public Speaking, Leadership, Team worker

Academic Achievements and Awards

97% marks in AISSCE 2013 with 100% in chemistry and Informatics Practices.
Recipient of Merit Scholarship at BITS Pilani.
Merit in International English Olympiad, National Cyber Olympiad, National Science Olympiad in 2012.
Recipient of Kulapati K.M Munshi Award in Mathematics in 2011 from Shikshan Bharti.
Distinction in University of New South Wale's Educational assessment in mathematics.
Pranlal Devkaran Nanjee award from Bhartiya Vidya Bhavan, shikshan bharti in 2011 for excellence in harmonious behavior.
Title of Amul Vidya Shree for outstanding performance in AISCE 2011.

Positions of Responsibility

Treasurer, Marudhara Cultural Association, BITS Pilani
School Football Team Captain

Extra-Curricular Activities and Achievements

Member of Mime Club, BITS Pilani
Open state pool player
Award for Excellence in Football from School

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