The University of Alabama in Huntsville
ECE Department
CPE 431 01, CPE 531 01/01R
Fall 2022
Virtual Memory

Due November 15, 2022
1.0.1(10), 1.0.2(10), 2.0.1(10), 2.0.2(10)

1.0 **<5.7>** As described in Section 5.4, virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. This exercise shows how this table must be updated as addresses are accessed. The following data constitutes a stream of virtual addresses as seen on a system. Assume 8 KiB pages, a 4-entry fully associative TLB, and true LRU replacement. If pages must be brought in from disk, increment the next largest page number. 4669, 2227, 13916, 34587, 48870, 12608, 49225

TLB

Valid	Tag	Physical Page Number
1	11	12
1	7	4
1	3	6
0	4	9

Page table

VPN	Valid	Physical page or in disk
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12

1.0.1 Given the address stream, and the shown initial state of the TLB and page table, show the final state of the system. Also list for each reference if it is a hit in the page table, or a page fault. These are byte addresses. What would be some of the advantages of having a larger page size than 8192 bytes? What are some of the disadvantages?

VPN 4699 = 4669/8192 = 0 map to set 0 for 2-way (LSB of virtual page number) or direct mapped (least two bits of virtual page number)
2227/8192 = 0 map to set 0 for 2-way or direct mapped
13916/8192 = 1 map to set 1 for 2-way or direct mapped

1.0.2 Show the final contents of the TLB if it is 2-way set-associative. Also show the contents of the TLB if it is direct mapped. Discuss the importance of having a TLB to high performance. How would virtual memory accesses be handled if there were no TLB?

Tag for 2-way, Index for 2-way, the VPN is Tag and Index
Tag 5, index 1 = VPN 1011

Initial TLB 2-Way

Index	Valid	Tag	PPN	Valid	Tag	PPN
0	1	2	9	0	5	3
1	1	5	12	1	3	4

Initial TLB Direct Mapped

Index	Valid	Tag	PPN
0	1	0	5
1	1	1	11
2	1	2	3
3	0	2	12

2.0 **<5.7>** In this exercise, we will examine space/time optimizations for page tables. The following list provides parameters of a virtual memory system.

Virtual Address (bits)	Physical DRAM Installed	Page Size	PTE Size (byte)
48	32 GiB	4 KiB	8

2.0.1 For a single-level page table, how many page table entries (PTEs) are needed? How much physical memory is needed for storing the page table?

2.0.2 Using a multilevel page table can reduce the physical memory consumption of page tables, by only keeping active PTEs in physical memory. How many levels of page tables will be needed in this case? And how many memory references are needed for address translation if miss in TLB?