The University of Alabama in Huntsville
ECE Department
CPE 431 01, CPE 531 01/01R
Processor Basics
Fall 2022

Due September 17, 2022
1.0 (30)

1.0 **<4.1>** When processor designers consider a possible improvement to the processor datapath, the decision usually depends on the cost/performance trade-off. In the following three problems, assume that we are starting with the datapath shown, where I Mem, Add, Mux, ALU, Regs, D Mem, and Control blocks have latencies of 320 ps, 150 ps, 20 ps, 180 ps, 90 ps, 350 ps, and 120 ps, respectively, and costs of 900, 80, 10, 195, 250, 1000, and 180, respectively.

Consider the addition of a multiplier to the ALU. This addition will add 250 ps to the latency of the ALU and will add a cost of 450 to the ALU. The result will be 10 % fewer instructions executed since we wil no longer need to emulate the MUL instruction.

1.0.1 **<4.1> (15)** What is the clock cycle time with and without this improvement?

1.0.2 **<4.1> (10)** What is the speedup achieved by adding this improvement?

1.0.3 **<4.1> (5)** Compare the cost/performance ratio with and without this improvement.