Electric Circuits & Electronics Design Lab

EE 316-01

Lab 9&10: Operating Characteristics of JFETs

By: Jaiden Gann

Lab Section 316-01

Lab Date: 7/13/22

Lab Due: 7/19/22

Introduction:

The purpose of this lab is to understand the configuration and characteristics of a JFET, which will later help in understanding MOSFETs. This report will have 5 main sections. First is the theoretical analysis which is done as the pre-lab and includes Multisim simulations. This time there is no handwritten solutions for the circuit. Then we have the physical circuits which are constructed on breadboards in lab. Afterwards, we compare the results from those 3 sections and conclude with an analysis of the results.

Theoretical Analysis:

To start, we look at how a JFET is constructed and works. It has 4 parts: a gate, body, drain, and source region. The body is the channel if voltage in the gate is field affected. There are two types of JFETs: N channel, where the body is a P-type material and P channel, where the body is N-type. Ideally the material used to make the gate has no effect and since the gate has no junctions it can be modeled as a capacitor. Current flows through the body region if its in linear operating mode, which is achieved by biasing the gate appropriately. The gate bias allows the current flow through a channel in the body. The threshold voltage is the voltage needed to put the JFET in linear operating mode. A JFET can act as a current controlled device, thus the current can be maintained regardless of the drain to source voltage.

There are three operating states: saturation, linear, and pinch off. The pinch off voltage is the voltage where the source current is constant. It is when the gate to source voltage is zero. Figures 1 and 2 give the general output characteristics of a JFET. In this lab, we looked at both the drain and transfer characteristics and noted where the pinch off voltage and threshold voltage is. We also looked at its behavior with small signal amplification.
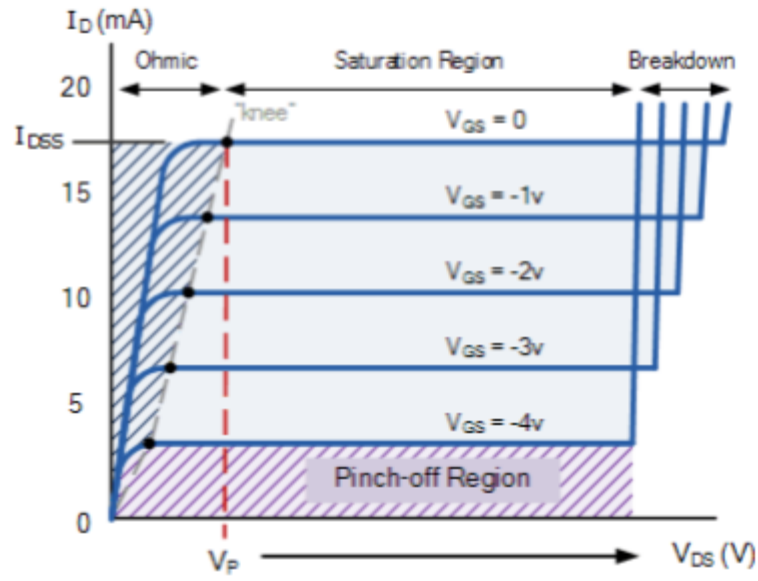
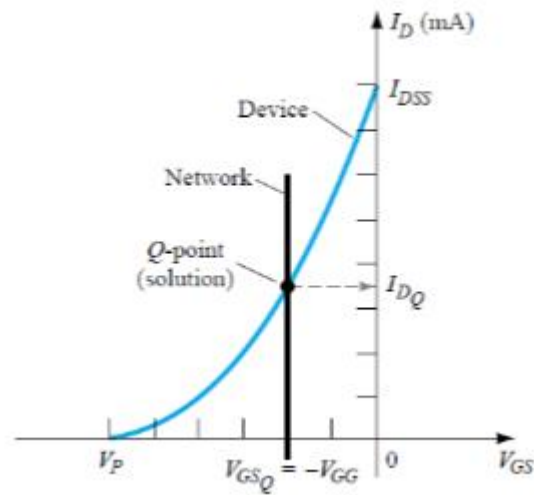**Figure 1**. Drain Characteristics of JFET

Figure 2. Transfer Characteristics of JFET

Simulations:

For the next phase of the lab, we built the circuits shown in Figures 3 and 4 in Multisim. For Multisim, we used the 2N3824 JFET. For Figure 3, we were looking at the drain current given certain drain to source and gate to source voltages. Then we plotted the data to get out transfer and drain characteristics. For Figure 4, we were observing the amplification of the JFET and what the output and gain is at a range of frequencies. We then plotted the gain versus frequency and observed the waveforms and bandwidth frequency.

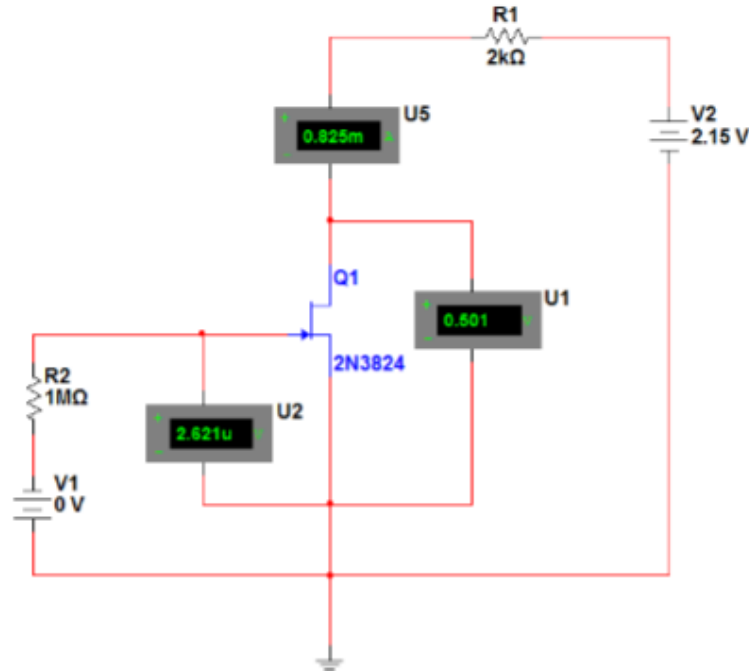Tables 1 – 3 is the data gathered from MultiSim and Figures 5 – 7 are plots generated from the data.
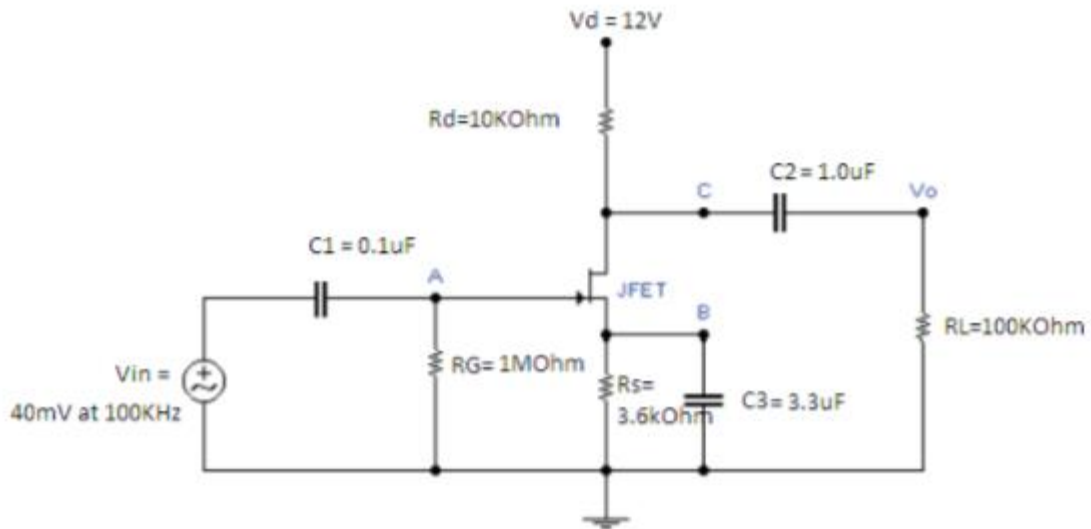
Figure 3: JFET circuit

**Figure 4.** Signal Amplification with JFET

Table 1. Output Characteristics

	$V_{GS} = 0$	$V_{GS} = -0.5$	$V_{GS} = -1$
V_{DS}	Id (mA)	Id (mA)	Id (mA)
0	0.04	0.037	0.033
0.5	0.891	0.595	0.395
1	1.538	0.979	0.567
2	2.175	1.119	0.572
4	2.213	1.131	0.578
8	2.26	1.155	0.59
12	2.306	1.178	0.602
16	2.352	1.204	0.615
20	2.398	1.226	0.629

Table 2. Transfer Characteristics

	$V_{DS} = 6$
V_{GS}	Id (mA)
0	2.236
-0.5	1.142
-1	0.584
-1.5	0.159
-2	0

Table 3. Output and Gain

F(HZ)	V$_{OUT}$	Gain(db)
30	0.443	11.86651
45	0.553	13.79293
60	0.627	14.88378
100	0.723	16.1212
200	0.781	16.79145
500	0.8	17.00023
1k	0.804	17.04355
10k	0.804	17.04355
100k	0.805	17.05435
500k	0.804	17.04355
1M	0.802	17.02192
1.5M	0.798	16.97849
2M	0.792	16.91293
3M	0.774	16.71325
4M	0.754	16.48586
5M	0.732	16.22865
7M	0.68	15.58861
10M	0.596	14.44336
11M	0.57	14.05593
12M	0.545	13.66636
15M	0.481	12.58133
16M	0.461	12.21245
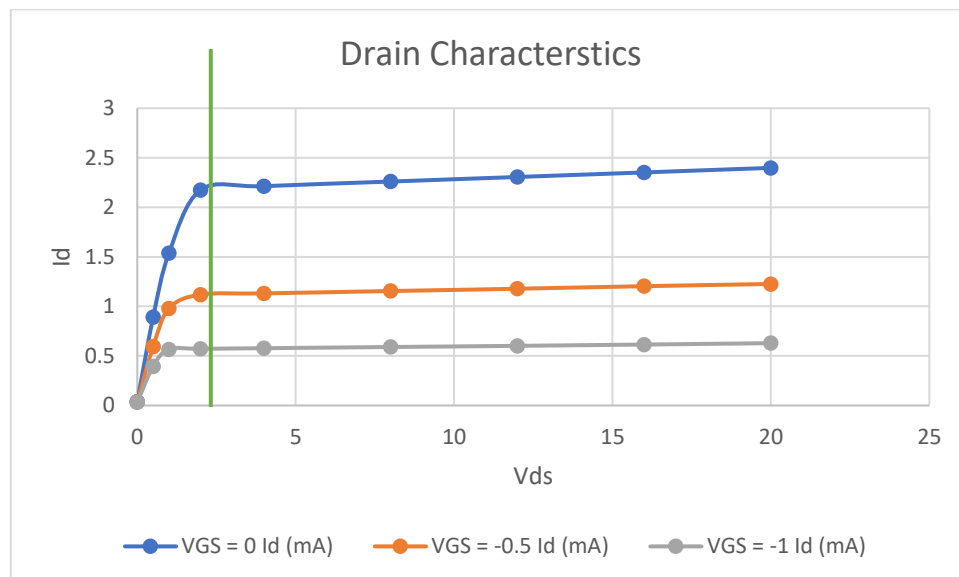
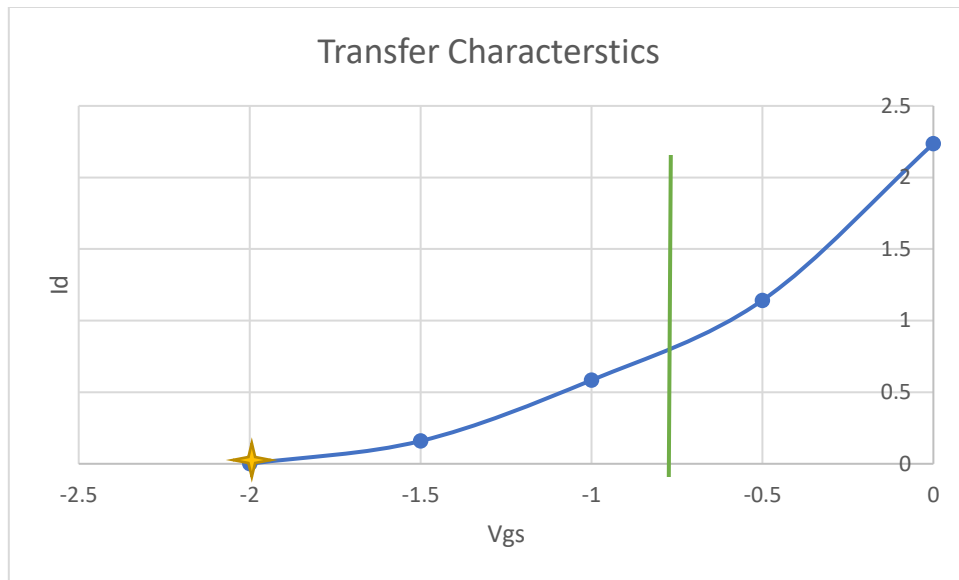

Figure 5. Drain Characteristics

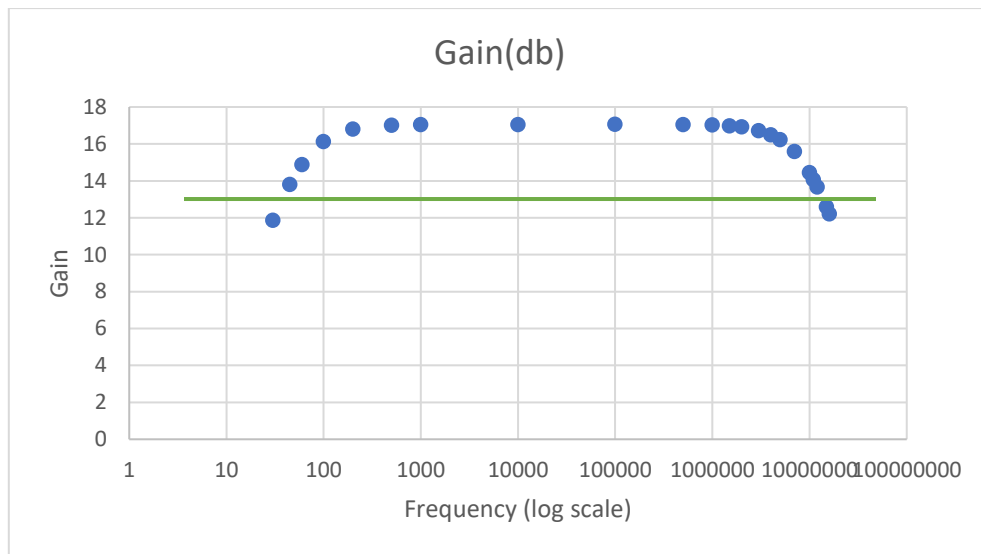**Figure 6.** Transfer Characteristics

Figure 7. Gain vs Frequency

Experimental:

For the last portion of the lab, we did the same things as prior but on a physical board to further validate the output results we obtained. For the first part, we looked at the drain characteristics output for a JFET. Excel was used for any calculations and plots. Table 4 and 5 gives the values collected and Figures 7 and 8 are the characteristic plot. As a note, for the gate to source voltage at 0, the drain to source voltage did not go above 13 volts in the lab. An extra row was also added to Table 5 so that the last value was actually 0. The pinch of voltage is around 1.5 volts and the threshold voltage is about -2.5 volts.

For the second circuit, Table 6 contains the output voltage and gain observed for each frequency. Figure 10 is the plot of gain versus frequency. The lowest frequency that could be done in lab with results was 30 Hz and the highest frequency was 3M Hz, so the table for this portion looks a little different than the one for the previous section. The bandwidth is shown by the green line.

Table 4. Output Characteristics

	$V_{GS} = 0$	$V_{GS} = -0.5$	$V_{GS} = -1$
V_{DS}	Id (mA)	Id (mA)	Id (mA)
0	0.08	0.06	0.02
0.5	2.8	2.16	1.51
1	4.87	3.6	2.38
2	7.23	5	3
4	8.27	5.55	3.25
8	8.5	5.75	3.3
12	8.5	5.8	3.44
16	8.5	5.81	3.48
20	8.5	5.81	3.5

Table 5. Transfer Characteristics

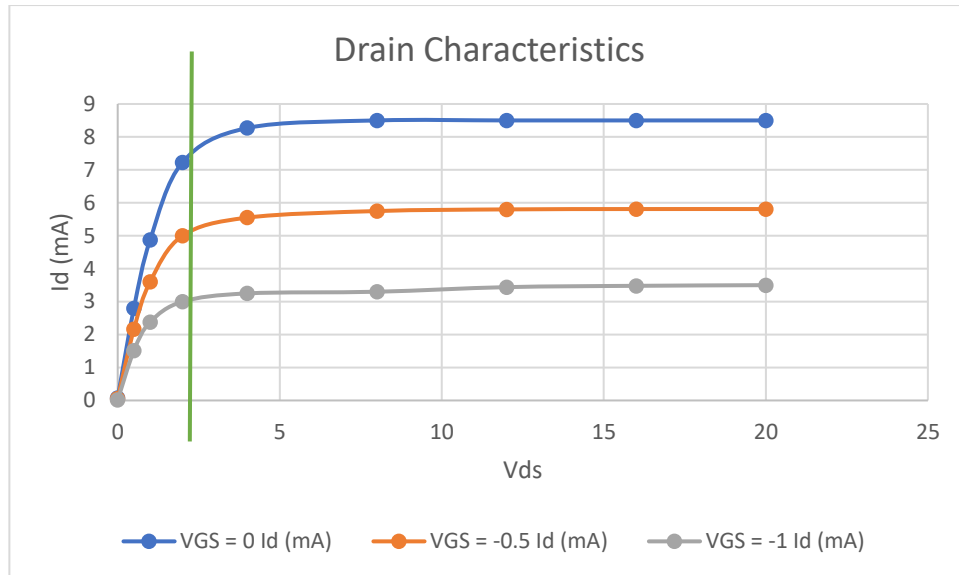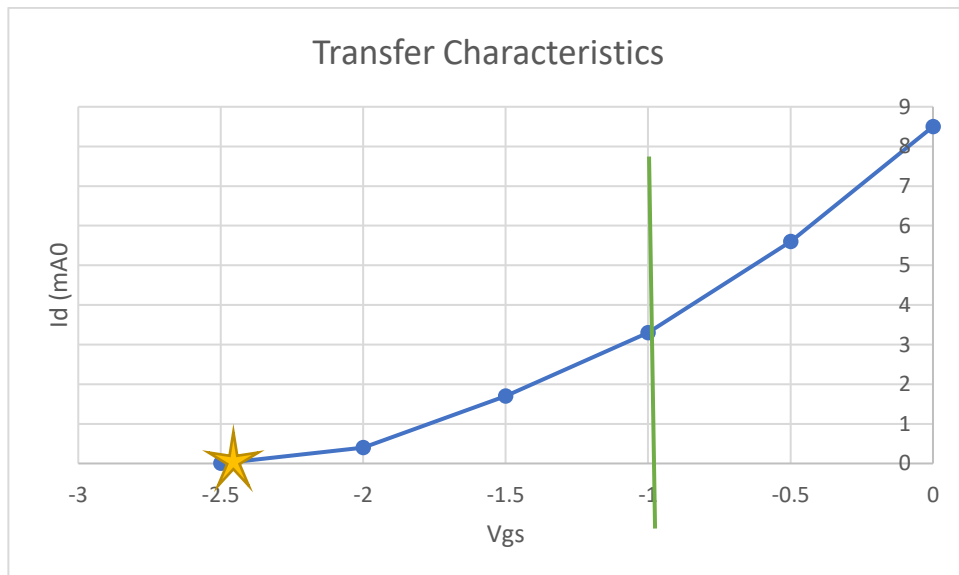|	$V_{DS} = 6$
V_{GS}	Id (mA)
0	8.5
-0.5	5.6
-1	3.3
-1.5	1.7
-2	0.4
-2.5	0

Figure 8. Drain Characteristics

Figure 9. Transfer Characteristics

Table 6. Amplification observations

F(HZ)	V_OUT (mV)	Gain(db)
30	620	13.90963
45	780	15.90369
60	900	17.14665
80	1.07 v	18.64948
100	1.17 v	19.42552
150	1.35 v	20.66848
200	1.45 v	21.28916
300	1.53 v	21.75563
400	1.57 v	21.97979
500	1.58 v	22.03494
1k	1.61 v	21.92472
1.5k	1.63 v	22.03196
10k	1.63 v	22.03196
50k	1.55 v	21.59484
100k	1.33 v	20.26524
300k	700	14.69017
500k	460	11.04336
1M	300	7.330631
1.5M	200	3.808806
2M	200	3.808806
3M	200	3.543567
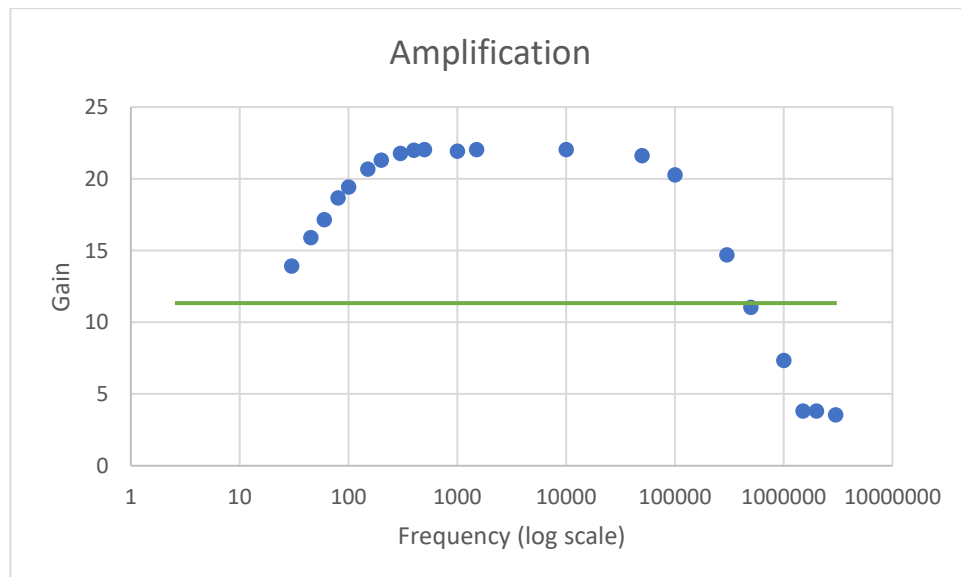
Figure 10. Gain vs Frequency

Results and Discussion:

The results of this lab were pretty in line with what we expected as far as the characteristic plots. The drain currents gathered for the experimental part were higher than the simulation but that could be due to a difference in the JFET used. The pinch off voltages for both simulation and experimental were the same however the threshold voltage was estimated to be a little different. The network line and thus Q point on the transfer characteristics plot was a little different but expected since the values gathered for the experiment were slightly higher than the simulation. The simulation didn't seem to follow the exact decrease you see in the drain currents for each of the gate to source voltages.

The amplification plot is very different from the one done during simulation. This could be due to the fact that the frequency in lab could not go higher than 3M Hz and no good values came from anything below 30 Hz, in fact below 30 it was showing as clipped. The bandwidth for the experimental part is between about 20 and 5k HZ since the amplifier needed to maintain a gain above or equal to 11. There is a bit of a gap due to the values of frequency looked at.

Conclusion

Overall, the results of lab where in line with what we expected from the information gathered from the theoretical sections. Our results matched the characteristic trends in the data for the simulation and experimental portions, even though the actual data itself was slightly different. It showed us what we should see as far as output, gain, waveforms, and current flow in a JFET which will be useful when we do MOSFETS. All together the lab gave us a better understanding of JFETs.

Appendix 1:

N/A

Appendix 2:

Signed lab results

J_{DS}	$V_{GS}=0$	$V_{GS}=-0.5$	$V_{GS}=-1$		V_{GS}	$V_{DS}=6$
0	0.08	0.06	0.02		0	8.5
0.5	2.8	2.16	1.31		-0.5	5.6
1	4.87	3.4	1.38		-1	3.3
2	7.23	5	3		-1.5	1.7
4	8.27	5.55	3.25		-2	0.4
8	8.5	5.75	3.3		-2.5	0
12	8.5	5.8	3.44			
16		5.81	3.48			
20		5.81	3.5			

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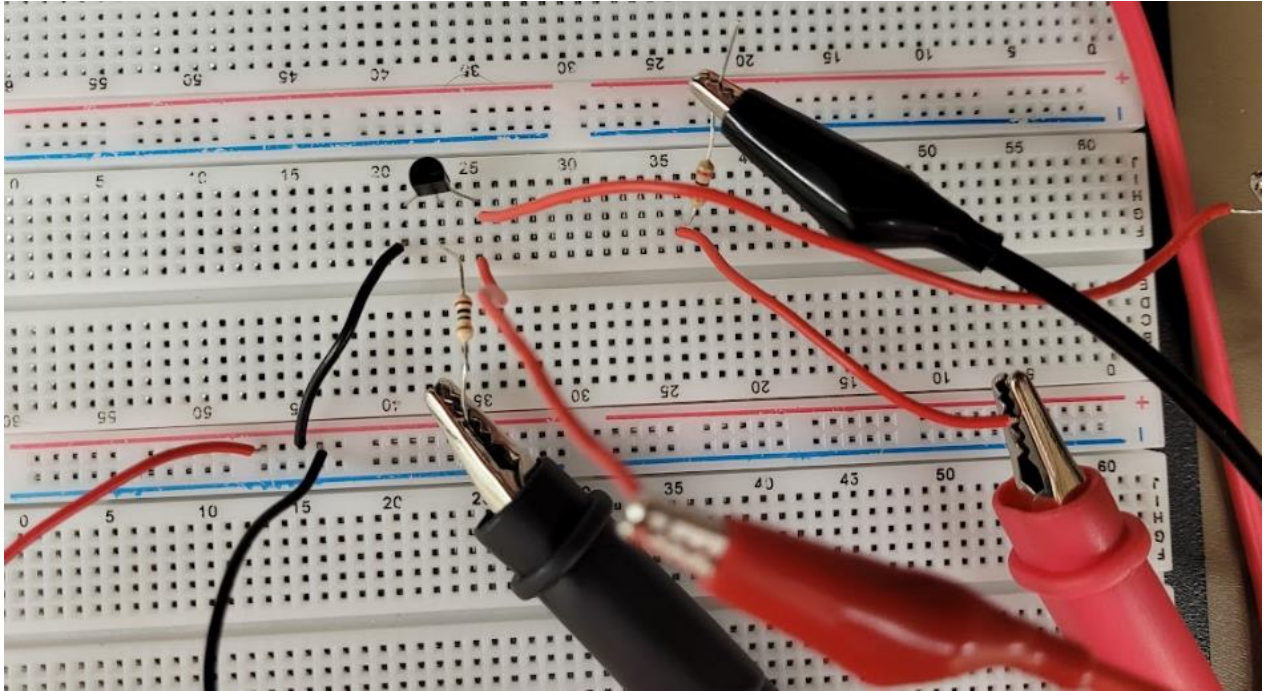|	Vout	Gain	Vin			
30	620	13.91	12.5	15M		
45	780	15.9		16M		
66	900	17.1		80	1.07	18.65
100	1.17	19.42		160	1.35	20.67
200	1.45	21.29		300	1.53	21.78
500	1.57	22.03		405	1.57	21.98
800	1.61	21.9	129	1.5	1.63	22.03
5k	1.63	22.03		300k	700	14.69
50k	1.33	20.26		50k	1.55	21.59
500k	460	11.04				
1M	300	7.33				
5M	200	3.81				
1	200	3.81				
1	200	3.54	133			

Pictures of Circuits

Figure 1. Characteristic Circuit (ref Figure 3)

*Forgot to take picture of second circuit