Electric Circuits & Electronics Design Lab EE 316-01

Lab 4: Digital to Analog Convertor Using Opamp

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Lab Section 316-01

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Introduction:

The purpose of this lab is to examine a binary resistive ladder network that is used to construct a digital to analog converter with an op-amp. We look at how step size, maximum output range, resolution, and accuracy can be found. This report will have 5 main sections. First is the theoretical analysis which is done as the pre-lab and includes Multisim simulations and handwritten solutions to the circuit. Then we have the physical circuits which are constructed on breadboards in lab. Afterwards, we compare the results from those 3 sections and conclude with an analysis of the results.

Theoretical Analysis:

To begin, we considered the main ladder circuit along with the op-amp shown in Figure 1. A digital to analog convertor takes information in the form of discrete bits into the equivalent analog information. A resistor has been added to the positive input in order to null stray currents.

In order to find the output, a Thevenin equivalent approach is used for each section of the ladder. Figure 2 is an example of the section of the ladder we look at. The equation used to find the output for a section of the ladder is $V_{TH} = \frac{V_D}{2R+2R} 2R = \frac{V_D}{2}$. In this case, this equation would be used for the first section of the ladder and as you go further down the equation gets multiplied by 1/2. The total output is the sum of the outputs coming from each section of the ladder. For this lab we had 4 levels of the ladder, so our output equation looked like this: $V_0 = -(\frac{V_A}{2} + \frac{V_B}{4} + \frac{V_C}{8} + \frac{V_D}{16})$.

The step size can be found by using the equation $\frac{V_{IN}}{2^n}$ where the voltage in is from the least significant bit, bottom level of ladder. Maximum output is the number of steps found by $2^N - 1$ * step size and the resolution is the step size divided by 2. To find the accuracy, the usual percent error equation is used, $\frac{V_{O_expected} - V_{O_measured}}{V_{O_expected}} * 100$.

As mentioned previously, we used a ladder system with 4 levels and added switches in order to control which input was high or low, a 1 or 0. Figure 3 shows the circuit we used to compare theoretical, simulation, and experimental output. The hand calculated outputs can be seen in Appendix 1, with the equation and results in their respective columns.

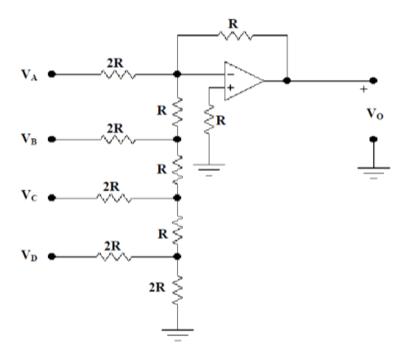


Figure 1. Ladder Circuit with Op-amp

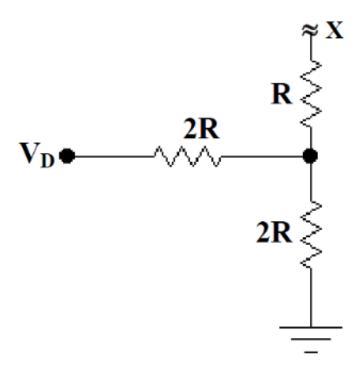


Figure 2. One level of Ladder Resistors for Thevenin analysis

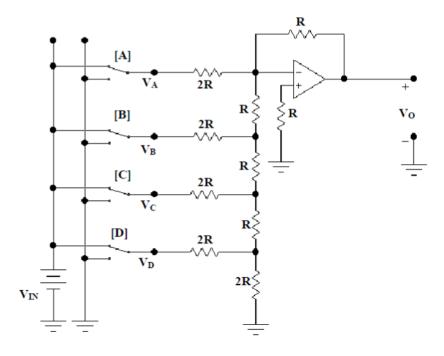


Figure 3. Circuit used for Lab analysis

Simulations:

For the next phase of the lab, we built the circuit from Figure 3 in Multisim which is shown in Figure 4. We simulated each type of input state you could have which is shown in Table 1 under the results section. Overall, the output values did not vary greatly from the theoretical ones that we observed previously.

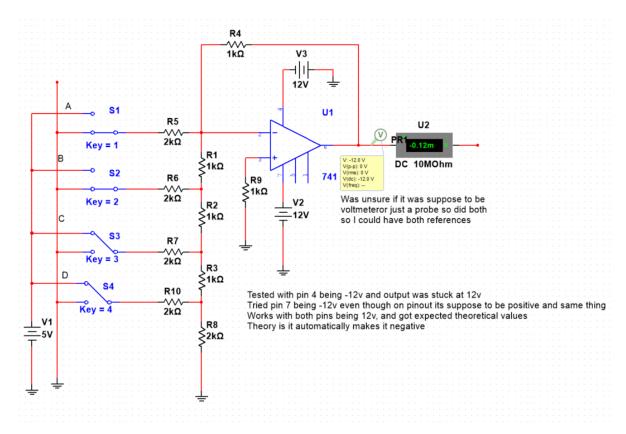


Figure 4: Digital to Analog Converter

Experimental:

For the last portion of the lab, we did the same things as prior but on a physical board to further validate the output results we obtained. Instead of switches though, we used a wire going to the resistor and simply put it in the power or ground row on the breadboard depending on the input we wanted. A multimeter was used at the output of the op-amp to obtain the output voltage. The constructed circuit can be seen in Appendix 2.

Table 1. Results for theoretical, simulation, and experimental sections

Input Table				Theoretical	Simulation	Experimental	
	V _A	V_{B}	V _C	V_D	V _O (V)	V _O (V)	V _O (V)
0	0	0	0	0	0	0	0
1	0	0	0	1	-0.3125	-0.31	-0.307
2	0	0	1	0	-0.625	-0.623	-0.620
3	0	0	1	1	-0.9375	-0.935	-0.927
4	0	1	0	0	-1.25	-1.25	-1.24
5	0	1	0	1	-1.5625	-1.56	-1.55
6	0	1	1	0	-1.875	-1.87	-1.86

7	0	1	1	1	-2.1875	-2.19	-2.17
8	1	0	0	0	-2.5	-2.50	-2.49
9	1	0	0	1	-2.8125	-2.81	-2.81
10	1	0	1	0	-3.125	-3.12	-3.12
11	1	0	1	1	34375	-3.44	-3.42
12	1	1	0	0	-3.75	-3.75	-3.74
13	1	1	0	1	-4.0625	-4.06	-4.05
14	1	1	1	0	-4.375	-4.37	-4.36
15	1	1	1	1	-4.6875	-4.69	-4.66

Results and Discussion:

The outputs for all 3 types of observation were very similar. They only differed in rounding due the way each output voltage was obtained. No significant problems were encountered while performing the simulation and experimental parts of the lab. However, to note during the experimental part, the ladder resistor system was not affecting the output of the opamp and the op-amp was only outputting half of the voltage that you provided to the ladder system. After it sat running for a few seconds, the output suddenly started being the expected value and it is unclear what caused the sudden change.

As discussed earlier, you could find the maximum output, resolution, step size, and accuracy. Num of steps = $2^4 - 1 = 15$ step size = $\frac{5}{2^4} = 0.3125$ Max output = 15 * 0.3125 = 4.6875 Resolution = $\frac{0.3125}{2} = 0.15625$ Error(Input state 12) = $\frac{-3.75 - (-3.74)}{-3.75} * 100 = 0.26\%$

Conclusion

Overall, the results of the lab only differed in small discrepancies due to rounding by how the outputs were obtained. It gave a simple example of how a digital to analog converter could be created. Since this is something used a lot in everyday technology and is typically seen as a box, this lab helps give a good simple visual of what the circuit could look like. All together the lab help furthered our exposure to circuits of commonly used concepts and technology.

Appendix 1:

The equation column contains only the addition of inputs that weren't zero

Vin = S	3/6 = 0.312 5/8 = 0.62	$\frac{5}{4} = 1$		
- x -	- (VA + VB + VC + VD)	(Experiment)	Simulation (Experiment)	
Input State		Output	Output	Experiment
0	. 0	Ö	0.002	0
T.	1/4	- 0.3125	-0.31	-0,307
2	5/8	- 0.625	-0.623	-6.620
3	5/8 5/9 + 9/16	- 0.9375	- 0.935	-0.927
4	5/4	-1.25	1.25	-1.24
5	9/4 + 3/16	- 1.5625	- 1.56	-1.55
6	3/4 + 5/8	- 1.875	- 1.87	- 1.86
7	3/4+ 9/8+ 3/16	- 2.1875	- 2.19	- Z.17
8	5/2	- 2.5	- 2.50	- 2,49
9	5/2 + 5/16	- 2.8175	- 2.81	- 2,81
10	5/2 + 3/8	- 3.125	- 3.12	- 3.12
11	9/2+ 3/8+ 3/6	- 3.4375	- 3.44	- 3.42
12	3/2+3/4	- 3.75	-3.75	- 3.74
13	5/2+ 5/4 + 5/16	-4.0625	-4.06	- 4.05
14	9/2 + 5/4 + 5/8	-4.375	-4.37	- 4,36
15	9/2 + 5/4 + 5/8+5/		-4.69	1-4.66
			Sidding	1
		1	1406	
			-80	12
			Supple	1.00
			198 V	,
			(0)	

Appendix 2:

Signed lab results

	- (VA + VB + VC + VD)	(Experiment)	Simulation (Experiment)	
Input State	Equation	Output	Output	Experiment
0	0	Ö	0.002	0
1	1/16	- 0.3125	-0.31	-0,307
2	5/8 5/4 + 3/16	- 0.625	-0.623	-6.620
3	5/9 + 9/16	- 0.9375	- 0.935	-0.927
4	5/4	-1.25	1.25	-1.24
5	5/4 + 5/16	- 1.5625	- 1.56	-1.55
6	3/4 + 5/8	- 1.875	- 1.87	- 1.86
7	3/4+ 3/8+ 3/6	- 2.1875	- 2.19	- Z.17
8	5/2	- 2.5	- 2.50	- 2,49
9	5/2 + 5/16	- 2.8175	- 2,81	- 2,81
10	5/2 + 5/8	- 3.125	- 3.12	- 3.12
U	9/2+ 9/8+ 9/6	- 3.4375	- 3.44	- 3.42
12	3/2+ 5/4	- 3.75	-3.75	- 3.74
13	5/2+5/4+5/16	-4.0625	-4.06	- 4.05
14	9/2 + 5/4 + 5/8	-4,375	-4.37	- 4,36
15	9/2 + 5/4 + 5/8+5/	16 - 4, 6875	-4.69	-4.66
			Sidding	
			/ v	11
		1	1400	/_
			000	Vav

Pictures of Circuits

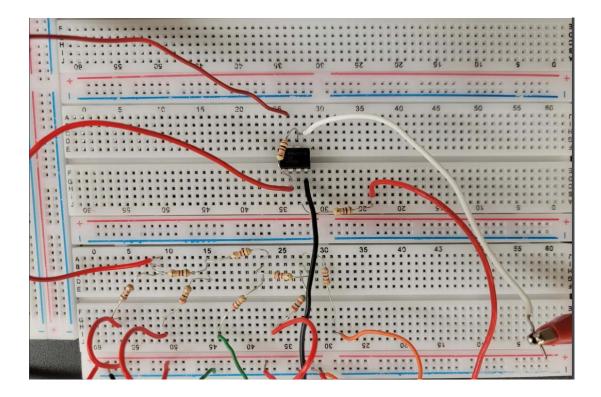


Figure 1. Digital to Analog Convertor



Figure 2. Output from Multimeter