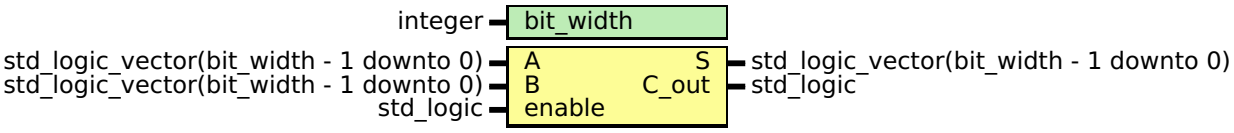
Carry Look-ahead Adder

Diagram



Description

A N-bit adder using carry look-ahead.
This is combinational circuit.
If enable != '1' then the output is set to high impedence.

Generics and ports

Table 1.1 Generics

Generic name	Type	Value	Description
bit_width	integer	4	The bit wifth of input integers.

Table 1.2 Ports

Port name	Direction	Type	Description
A	in	std_logic_vector(bit_width - 1 downto 0)	Input integer A.
B	in	std_logic_vector(bit_width - 1 downto 0)	Input integer B.
S	out	std_logic_vector(bit_width - 1 downto 0)	Output Sum=A+B.
C_out	out	std_logic	Output Carry.
enable	in	std_logic	If not = '1', output is high impedence.

Signals, constants and types

Signals

Name	Type	Description
G	std_logic_vector(bit_width - 1 downto 0)	Generate signals
P	std_logic_vector(bit_width - 1 downto 0)	Propagate signals
C	std_logic_vector(bit_width downto 0)	Carry buffer