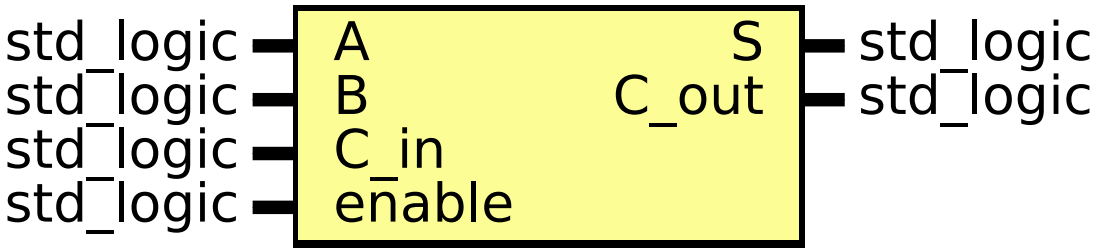
Full Adder

Diagram



Description

This is full adder combinational circuit.
If enable != '1' then the output is set to high impedence.

Generics and ports

Table 1.1 Generics

Table 1.2 Ports

Port name	Direction	Type	Description
A	in	std_logic	Input bit A.
B	in	std_logic	Input bit B.
C_in	in	std_logic	Input bit Carry.
S	out	std_logic	Output bit Sum.
C_out	out	std_logic	Output bit Carry.
enable	in	std_logic	If not = '1', output is high impedence and internal state is frozen.

Signals, constants and types

Signals

Name	Type	Description
I	std_logic	Common signal A xor B.