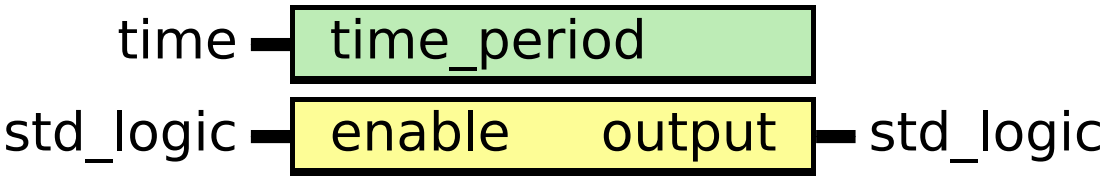
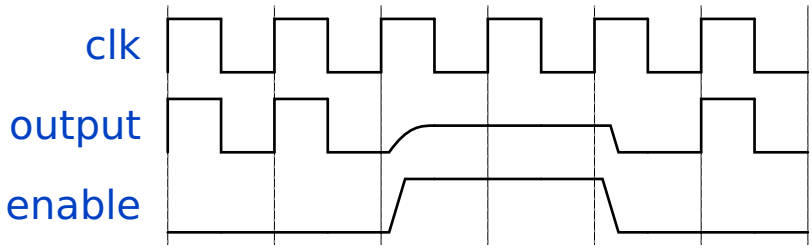
Clock

Diagram



Description

This clock simply switches between '1' and '0' with the given time period.
Internally, it uses the transport delay feature of VHDL.
The default time period is set to 10 ns.
If enable != '1' then the output is set to high impedence.
Note: Even when enable != '1' the clock continues to tick.



Generics and ports

Table 1.1 Generics

Generic name	Type	Value	Description
time_period	time	10 ns	Time period of the clock.

Table 1.2 Ports

Port name	Direction	Type	Description
enable	in	std_logic	If set to anything other than '1', then O/P is high impedence.
output	out	std_logic	Either '1' or '0' depending on the clock signal.

Signals, constants and types

Signals

Name	Type	Description
internal_clock	std_logic	

Processes

- **clock_tick**: ***(enable, internal_clock)***