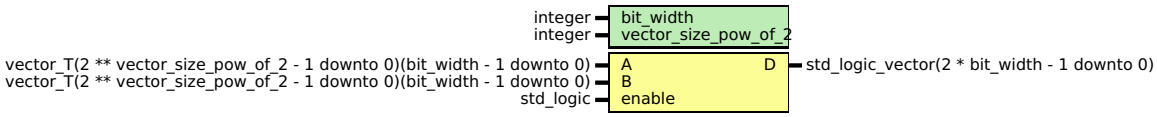
Vector Dot Product Unit

Diagram



Description

A N-bit 2^T length vector multiplier (dot product) using array multipliers and carry lookahead adders.
It requires 2^T as it uses logrithmic parallel addition by dividing the addition into T stages of carry look-ahead adders.
Note: The output has double the bit width of the input.
This ignores (discards carry) any integer overflows during accumulation of the dot product.
NOTE: To compile this file please set modelsim to use VHDL 2008 for all files. See:
https://forums.xilinx.com/t5/Synthesis/Array-of-Unconstrained-Array/td-p/681253
This is combinational circuit.
If enable != '1' then the output is set to high impedence.

Generics and ports

Table 1.1 Generics

Generic name	Type	Value	Description
bit_width	integer	8	Bit width for input integers.
vector_size_pow_of_2	integer	2	The length 2^T of input vectors.

Table 1.2 Ports

Port name	Direction	Type	Description
A	in	vector_T(2 ** vector_size_pow_of_2 - 1 downto 0)(bit_width - 1 downto 0)	Input vector A.
B	in	vector_T(2 ** vector_size_pow_of_2 - 1 downto 0)(bit_width - 1 downto 0)	Input vector B.
D	out	std_logic_vector(2 * bit_width - 1 downto 0)	Output number A.B (dot product). Has integrs with 2*bit_width bits.
enable	in	std_logic	If not = '1', output is high impedence and internal state is frozen.

Signals, constants and types

Signals

Name	Type	Description
AddBuffer	Array_T(vector_size_pow_of_2 downto 0, 2 ** vector_size_pow_of_2 - 1 downto 0)(2 * bit_width - 1 downto 0)	Stores addition stages

Types

Name	Type	Description

Array_T		Type for 2D array of std_logic.