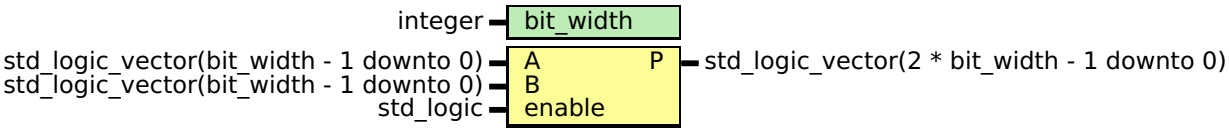
Array Multiplier

Diagram



Description

A N-bit multiplier using add-shift.
Note: The output has double the bit width of the input.
This is combinational circuit.
If enable != '1' then the output is set to high impedence.
Reference: https://faculty.weber.edu/fonbrown/ee3610/arraymult.txt

Generics and ports

Table 1.1 Generics

Generic name	Type	Value	Description
bit_width	integer	8	The bit wifth of input integers.

Table 1.2 Ports

Port name	Direction	Type	Description
A	in	std_logic_vector(bit_width - 1 downto 0)	Input integer A.
B	in	std_logic_vector(bit_width - 1 downto 0)	Input integer B.
P	out	std_logic_vector(2 * bit_width - 1 downto 0)	Output result A*B.
enable	in	std_logic	If not = '1', output is high impedence.

Signals, constants and types

Signals

Name	Type	Description
M	Array_T(bit_width downto 0, bit_width - 1 downto 0)	Used to store bit multiplications A(i) and B(i).
S	Array_T(bit_width - 1 downto 0, bit_width - 1 downto 0)	Used to store intermediate sums.
C	Array_T(bit_width - 1 downto 0, bit_width - 2 downto 0)	Used to store intermediate carry.

Types

Name	Type	Description
Array_T		Type for 2D array of std_logic.