EE-309: Microprocessor

Project 1: IITB-RISC

Multi-Cycle Implementation

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R Type Instruction format

Opcode (4 bit)	Register A (RA) (3 bit)	Register B (RB) (3-bit)	Register B (RB) (3-bit)	Unused (1 bit)	Condition (CZ) (2 bit)

I Type Instruction format

Opcode (4 bit)	Register A (RA) (3 bit)	Register C (RC) (3-bit)	Immediate (6 bits signed)

J Type Instruction format

Opcode (4 bit)	Register A (RA) (3 bit)	Immediate (9 bits signed)

Instructions Encoding:

ADD:	00_01	RA	RB	RC	0	00
ADC:	00_01	RA	RB	RC	0	10
ADZ:	00_01	RA	RB	RC	0	01
ADL:	00_01	RA	RB	RC	0	11
ADI:	00_00	RA	RB	6 bit Immediate		
NDU:	00_10	RA	RB	RC	0	00
NDC:	00_10	RA	RB	RC	0	10
NDZ:	00_10	RA	RB	RC	0	01
LHI:	00_00	RA	9 bit Immediate			
LW:	01_11	RA	RB	6 bit Immediate		
SW:	01_01	RA	RB	6 bit Immediate		
LM:	11_00	RA	0 + 8 bits corresponding to Reg R0 to R7 (right to left)			
SM:	11_01	RA	0 + 8 bits corresponding to Reg R0 to R7 (right to left)			
BEQ:	10_00	RA	RB	6 bit Immediate		
JAL:	10_01	RA	9 bit Immediate offset			
JLR:	10_10	RA	RB	000_000		
JRI	10_11	RA	9 bit Immediate offset			

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Project Aim:-

Designing multi-cycle processor, IITB-RISC-22 with its instruction set architecture given. It is a 16-bit very simple computer developed for teaching based on Computer Architecture. It is implemented using 8-register, 16-bit system using VHDL as hardware description language that uses point to point communication infrastructure.

ALU :

→ takes 2 vectors of size 16-bit and performs addition & Nand operations according to another input and gives output vector of performed operation and C & Z flags.

immediate_6bit and 9bit:-

These components extend sign of input vectors of size 6, 9 bits to vector size_16.

Memory Unit:-

This component outputs the data in given address if read input is '1' & writes given data if mwrite is '1' and there's a rise in edge of clock (CLK).

Register file :-

This consists of 8 registers which we use according to the state where we are currently in.

RISU unit :-

This is important unit of machine. It integrates various sub components we already implemented. This is a ~~mealy~~ mealy machine as output depends on input. (FSM).

This takes opcode & values of C, Z registers as input to give output.

→ There are 3 machine code instruction formats R, I, J and total of 15 instructions.

States :-

(S1)

PC → mem-A

mem-D → IR

PC → ALU-A

+2 → ALU-B

ALU-C → T4

(S2)

IR{8-0} → LE-16

LE-16 → T1

(S3)

T1 → RF-D3

IR{11-9} → RF-A3

T4 → PC

S4

IR {11-9} → RF-A1

IR {8-6} → RF-A2

RF-D1 → T1

RF-D2 → T2

S5

T1 → ALU-A

T2 → ALU-B

ALU-C → T1

ALU-Z → Z

ALU-CA → C

Subtraction.

S6

T1 → RF-D3

IR {5-3} → RF-A3

T4 → PC

S7

IR-{11-9} → RF-A1

RF-D1 → T1

IR {5-0} → SE-16

SE-16 → T2

S8

IR-{8-6} → RE-A2

RF-D2 → T2

IR {5-0} → SE-16

SE-16 → T1

S9

IR {4-9} → RE-A1

READ → T1

'000' → T2

S10

T1 + mem-A

MemD → T3

S11

T3 → RF-D3

T2 {2-0} → RF-A3

T2 → ALU-A

T1 → ALU-B

ALU-C → T2

S12

T1 → ALU-A

T2 → ALU-B

ALU-C → T4

T4 → PC

S13

T2 → ALU-A

+1 → ALU-B

ALU-C → T2

S14

IR {8-6} → RE-A1

RE-A1

RE-DA → PC

S15

T2 → ALU-A

+1 → ALU-B

ALU-C → T2

S16

T2-{2-0} → RE-A2

RE-D2 → T3

T1 → Mem-A

T2 → MemD

S18

PC → ALU-A

IR {5-0} - SE-16

SE-16 → ALU-B

ALU-C → PC

S19

T1 → mem-A

mem-D → RF-D3

IR {11-9} → RF-A3

T4 - PC

S20

IR{11-9} → RF-A1

RF_D1 → T2

T1 → mem_A

T2 → mem_D

S21

T1 → RF_D3

IR{8-6} → RF_A3

T4 → PC

S22

PC → RF_D3

IR{11-9} → RF_A3

S23

IR{11-9} → RF_A2

RF_D2 → T1

T1 → ALU_A

Imm9 → ALUB

ALU_out → PC

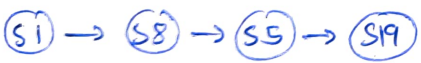
ADD, ADC, ADZ, ADZ

ADI

NDU, NDC, NDZ

LHI

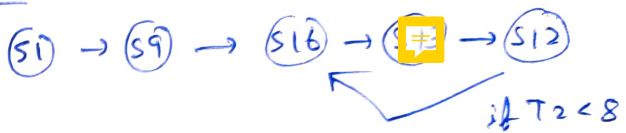
LW



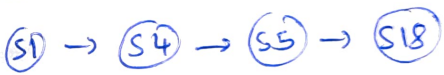
SW

LM

SM



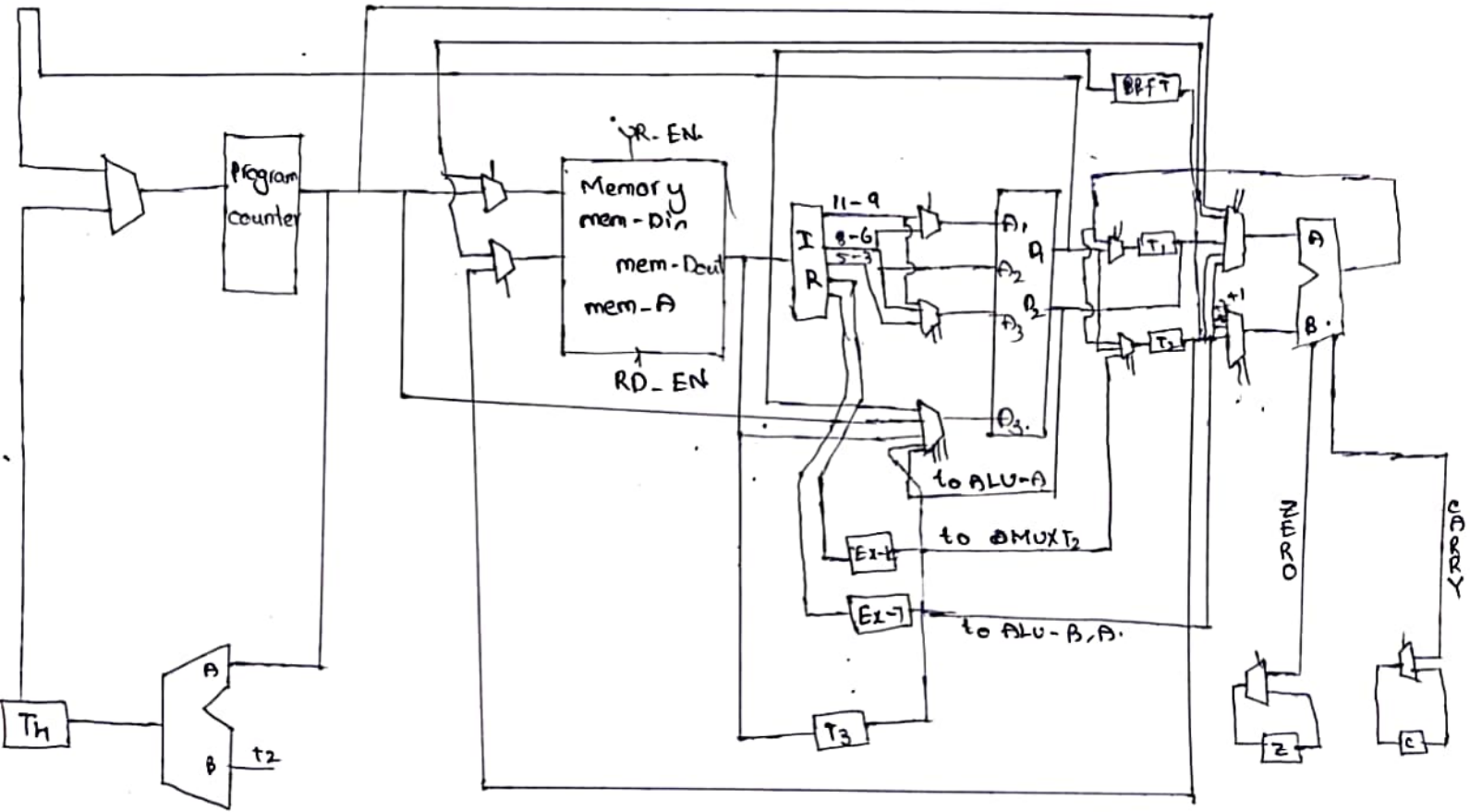
BEQ



JAL

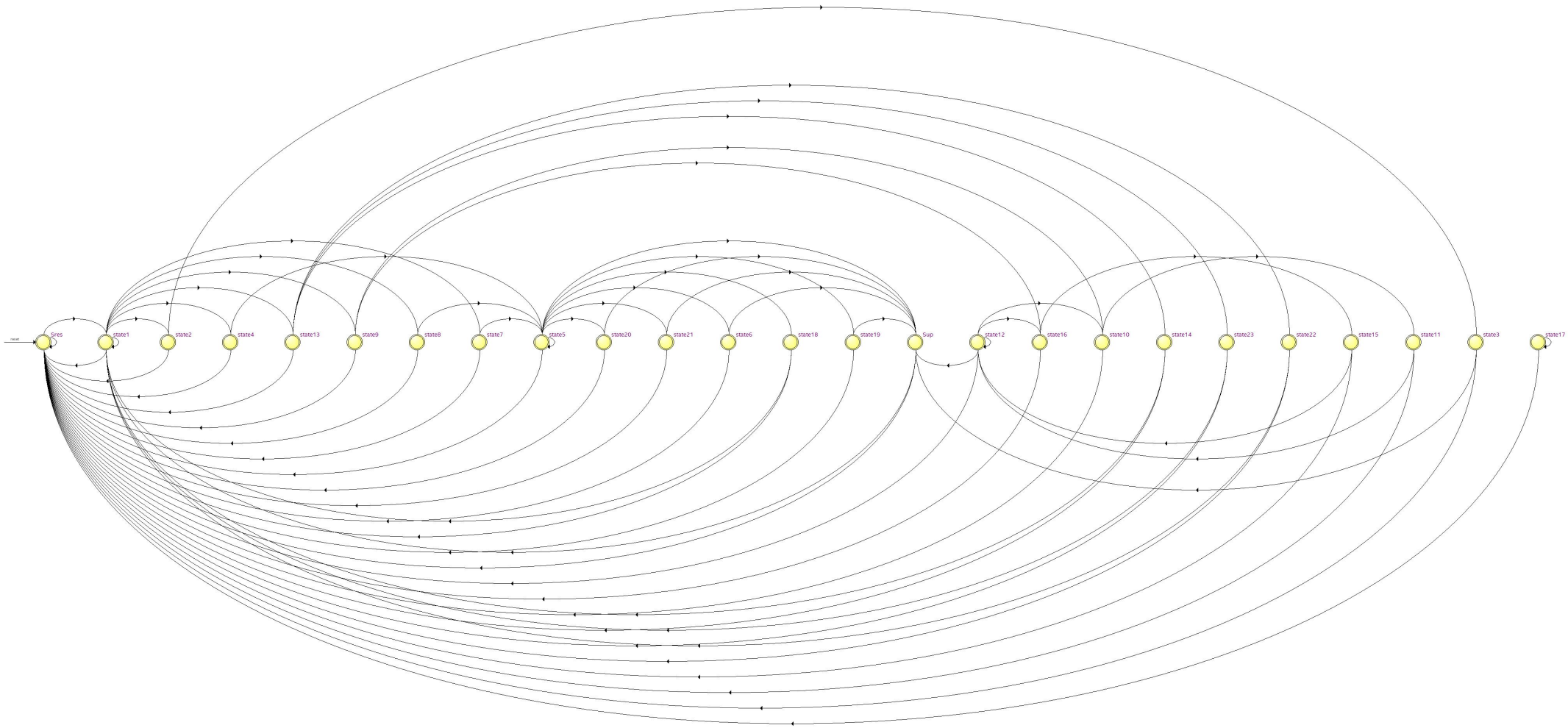
JLR

JRI

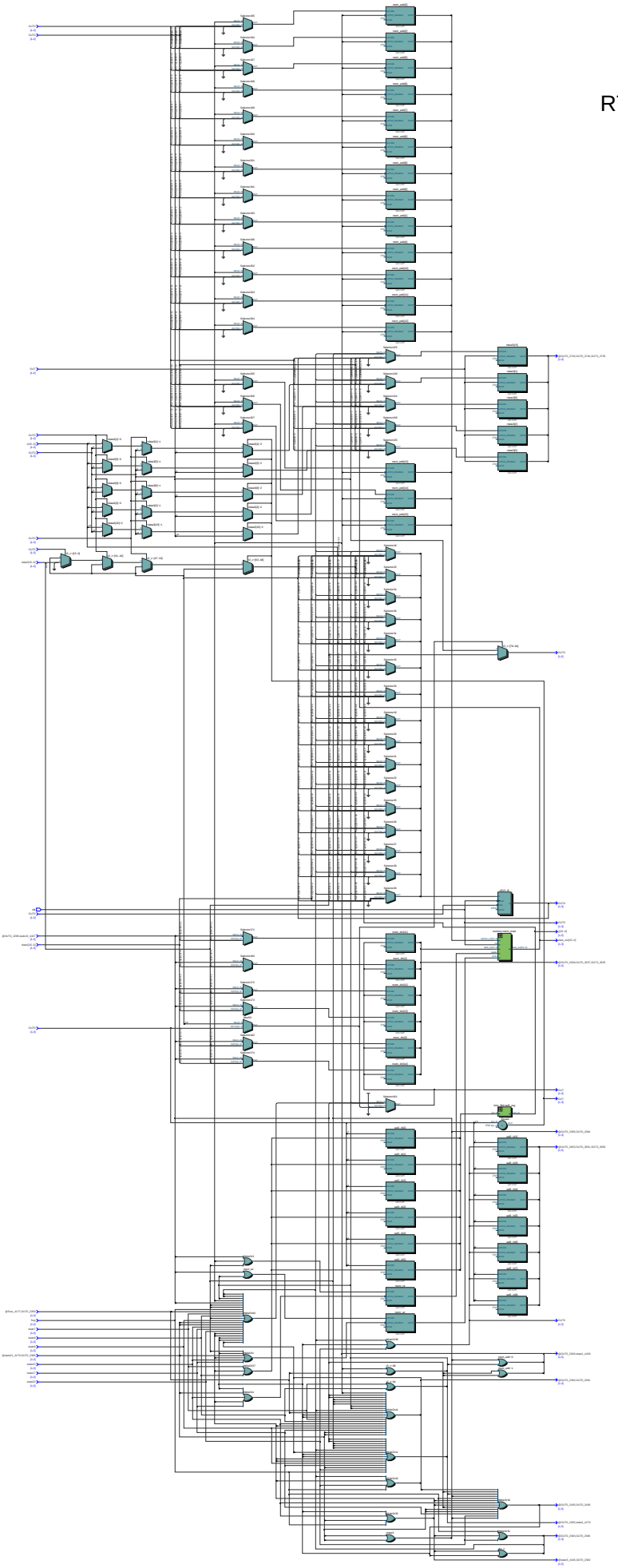


General Data Flow

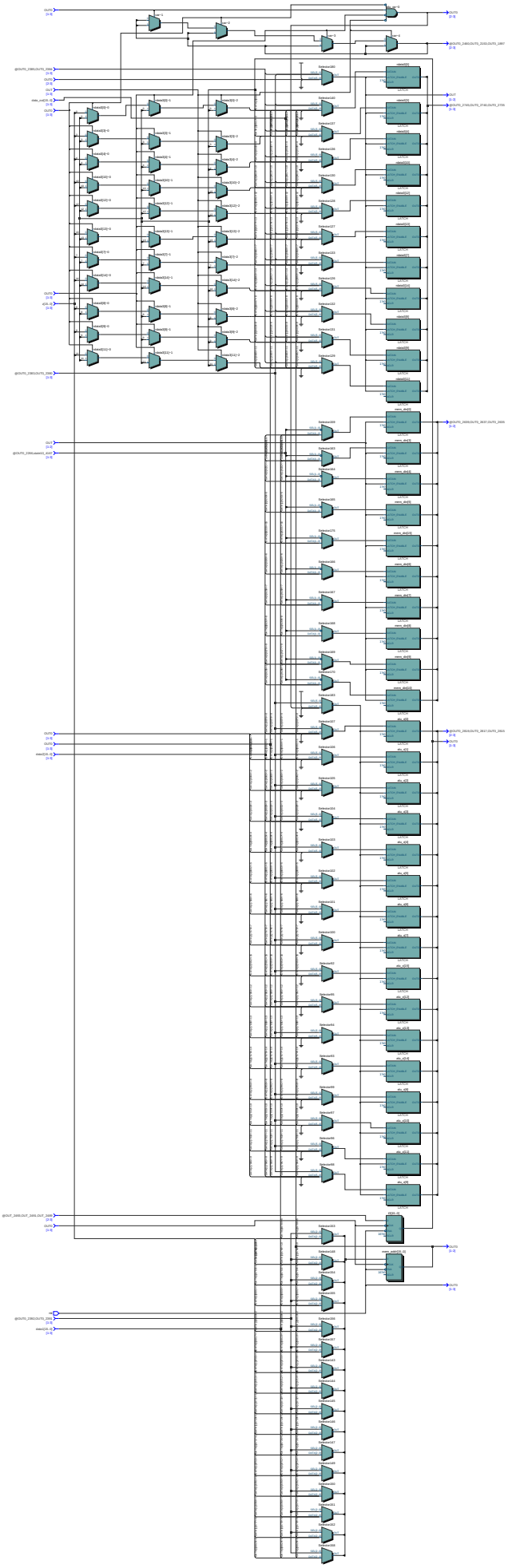
State Machine View



RTL View 1



RTL View 2



RTL View 3