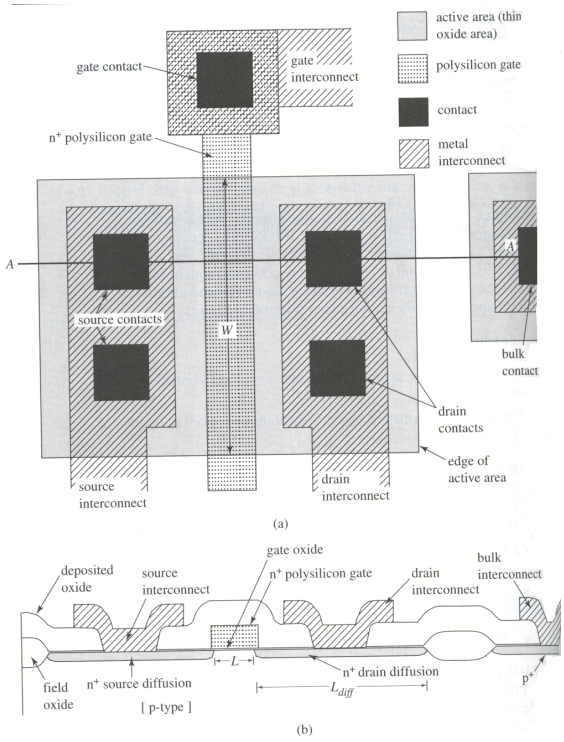
4. SPICE LEVEL 1 MOSFET MODEL

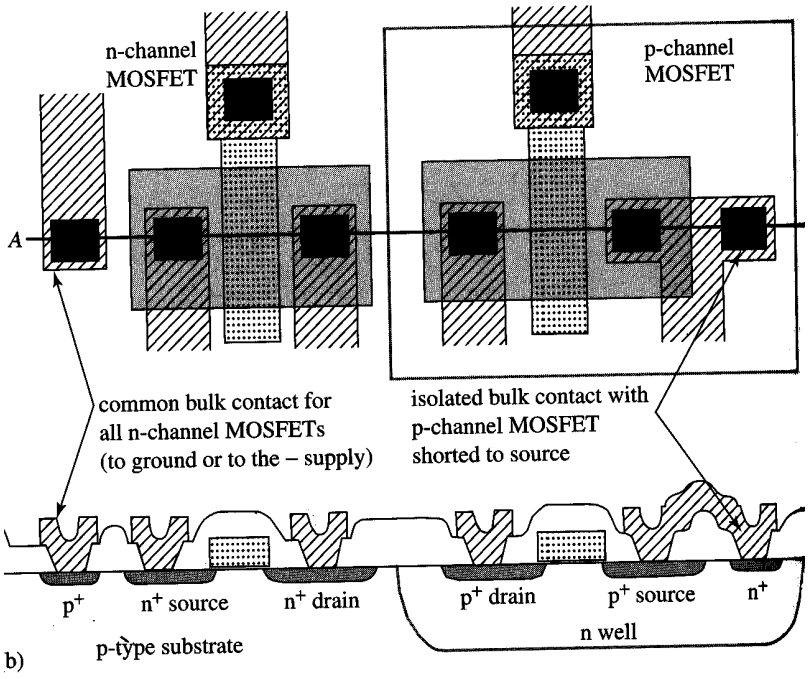
MES Institute of Microelectronic Systems

Four mask layout and cross section of a N channel MOS Transistor.



MES Institute of Microelectronic Systems

Layout and cross section of a n-well CMOS technology.



Equations for the different operation regions

$$I_{DS} = 0 \qquad (V_{GS} \le V_{TH})$$

$$I_{DS} = \frac{KP}{2}(W/L_{eff})V_{DS}\left[2(V_{GS} - V_{TH}) - V_{DS}\right](1 + LAMBDA \cdot V_{DS}) \qquad (0 \le V_{DS} \le V_{GS} - V_{TH})$$

$$I_{DS} = \frac{KP}{2}(W/L_{eff})(V_{GS} - V_{TH})^2(1 + LAMBDA \cdot V_{DS}) \qquad (0 \le V_{GS} - V_{TH} \le V_{DS})$$

Where the threshold voltage is given by:

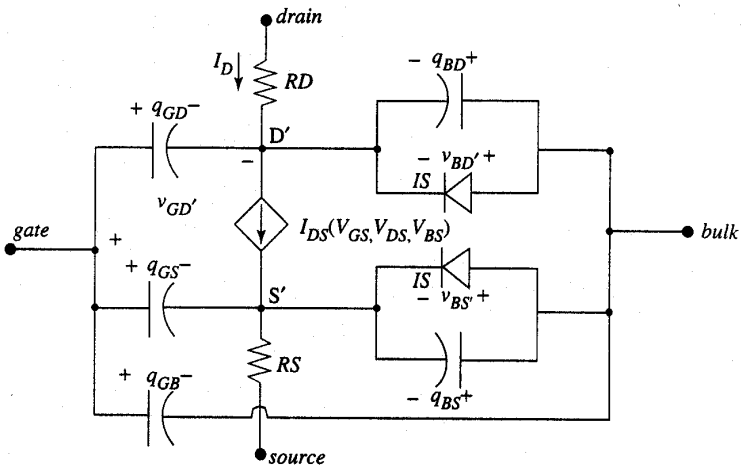
$$V_{TH} = V_{T0} + GAMMA\left(\sqrt{2 \cdot PHI - V_{BS}} - \sqrt{2 \cdot PHI}\right)$$

and the channel length:

$$L_{eff} = L - 2 \cdot LD$$

Where *L* is the length of the polysilicon gate and *LD* is the gate overlap of the source and drain.

The elements in the large signal MOSFET model are shown in the following figure.

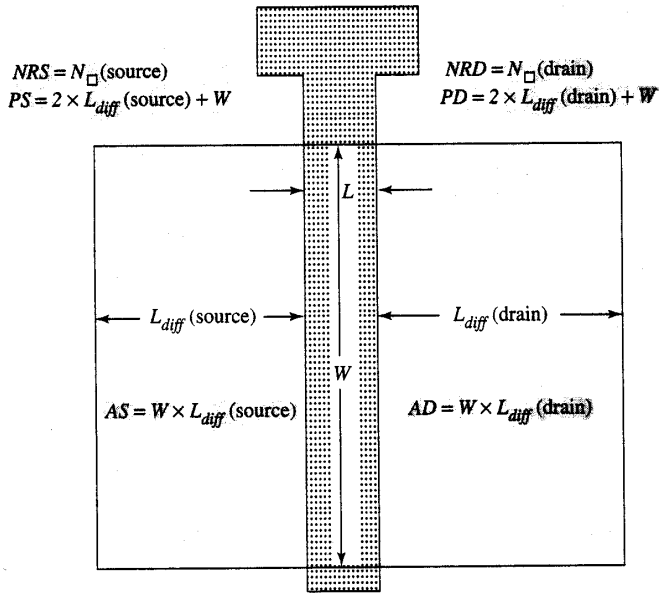


MOSFET SPICE PARAMETERS.

Parameter Name	SPICE Symbol	Analytical Symbol	Units
Channel length	L_{eff}	L	M
Poly gate length	L	L_{gate}	M
Lateral diffusion/ Gate-source overlap	LD	L_D	M
Transconductance parameter	KP	$\mu_n C_{OX}$	A/V^2
Threshold voltage/ Zero-bias threshold	VTO	V_{TO}	V
Channel-length modulation parameter	LAMBDA	λ_n	V^{-1}
Bulk threshold/ Backgate effect parameter	GAMMA	γ_n	$V^{1/2}$
Surface potential/ Depletion drop in inversion	PHI	$-\phi_P$	V

Specifying MOSFET Geometry in SPICE.

M*name* D G S B MOD*name* **L**= **W**= **AD**= **AS**= **PD**= **PS**= **NRD**= **NRS**=



LEVEL 1 MOSFET MODEL PARAMETERS.

.MODEL MOD*name* **NMOS/PMOS VTO**= **KP**= **GAMMA**= **PHI**= **LAMBDA**= **RD**= **RS**= **RSH**= **CBD**= **CBS**= **CJ**= **MJ**= **CJSW**= **MJSW**= **PB**= **IS**= **CGDO**= **CGSO**= **CGBO**= **TOX**= **LD**=

where:

NMOS/PMOS- MOSFET type.

VTO- Threshold voltage (V)

KP- Transconductance parameter (A/V^2)

GAMMA- Bulk threshold parameter ($V^{1/2}$)

PHI- Surface potential (V)

LAMBDA- Channel length modulation parameter (V^{-1})

RD- Drain resistance (Ω)

LEVEL 1 MOSFET MODEL PARAMETERS.

RS- Source resistance (Ω)

RSH- Sheet resistance of the drain/source diffusions (Ω/□)

CBD- Zero bias drain-bulk junction capacitance (F)

CBS- Zero bias source-bulk junction capacitance (F)

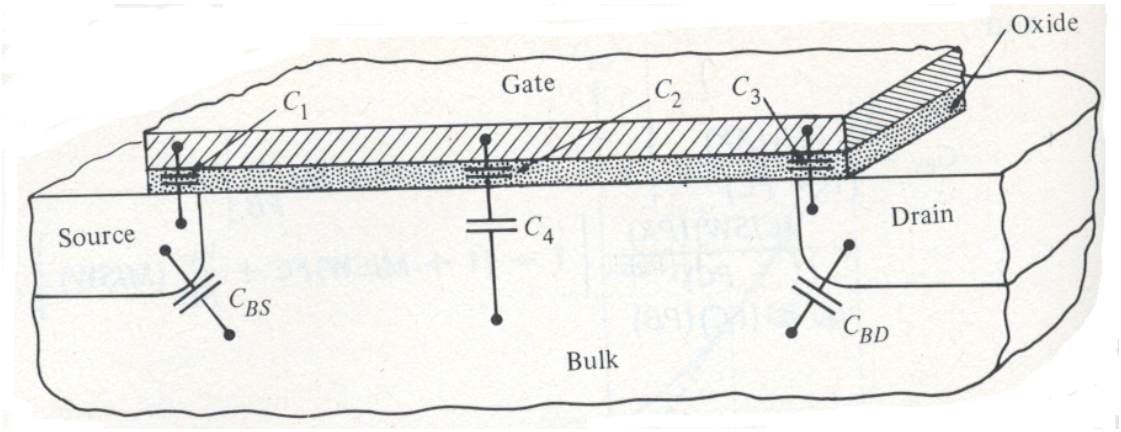
MJ- Bulk junction grading coefficient (dimensionless)

PB- Built-in potential for the bulk junction (V)

- With CBD, CBS, MJ and PB, SPICE computes the voltage dependences of the drain-bulk and source-bulk capacitances:

$$C_{BD}(V_{BD}) = \frac{CBD}{(1 - V_{BD}/PB)^{MJ}} \qquad C_{BS}(V_{BS}) = \frac{CBS}{(1 - V_{BS}/PB)^{MJ}}$$

Large-signal, charge-storage capacitors of the MOS device.



LEVEL 1 MOSFET MODEL PARAMETERS.

CJ- Zero bias planar bulk junction capacitance (F/m^2)

CJSW- Zero bias sidewall bulk junction capacitance (F/m)

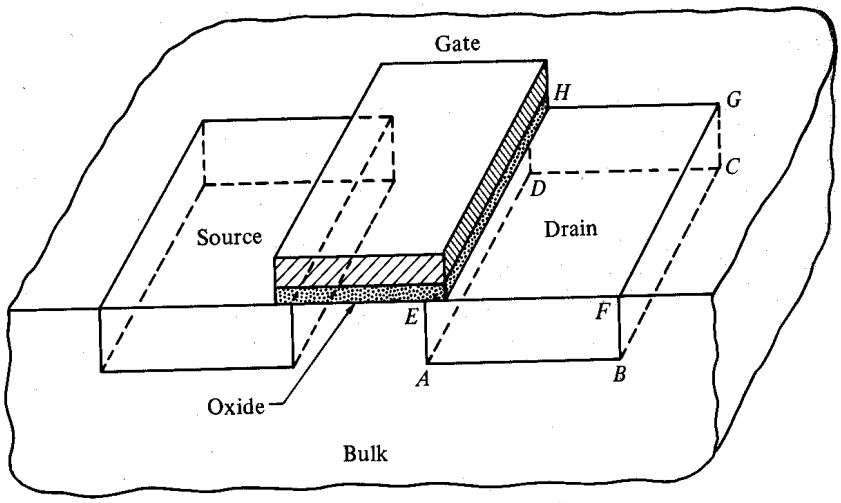
MJSW- Sidewall junction grading coefficient (dimensionless)

- If CJ, CJSW, and MJSW are given, a more accurated simulation of these capacitances is performed using the following equations:

$$C_{BD}(V_{BD}) = \frac{CJ \cdot AD}{(1 - V_{BD}/PB)^{MJ}} + \frac{CJSW \cdot PD}{(1 - V_{BD}/PB)^{MJSW}}$$

$$C_{BS}(V_{BS}) = \frac{CJ \cdot AS}{(1 - V_{BS}/PB)^{MJ}} + \frac{CJSW \cdot PS}{(1 - V_{BS}/PB)^{MJSW}}$$

Bottom and Sidewall components of the bulk junction capacitors.



Bottom=*ABCD*

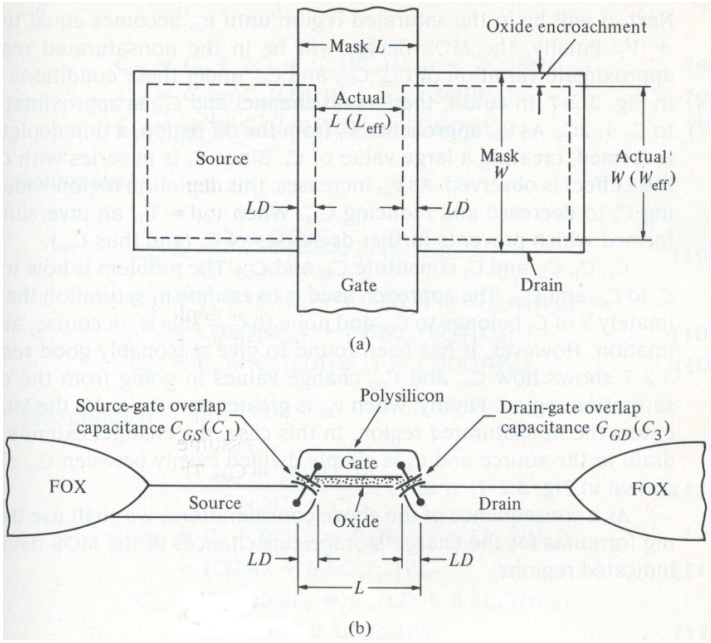
Sidewall=*ABEF+BCFG+DCGH+ADEH*

LEVEL 1 MOSFET MODEL PARAMETERS.

IS- Saturation current of the junction diode (A)
CGDO- Overlap capacitance of the gate with drain (F)
CGSO- Overlap capacitance of the gate with source (F)
CGBO- Overlap capacitance of the gate with bulk (F)
TOX- Gate oxide thickness (m)
LD- Lateral diffusion (m)

Overlap Capacitances of an MOS transistor.

(a) Top view showing the overlap between the source or drain and the gate. (b) Side view.



Example of MOSFET model parameters values.

Parameter Name	N Channel MOSFET	P Channel MOSFET	Units
Gate oxide thickness TOX	150	150	Angstroms
Transconductance parameter KP	50×10^{-6}	25×10^{-6}	A/V^2
Threshold voltage	1.0	-1.0	V
Channel-length modulation parameter LAMBDA	0.1/L (L in µm)	0.1/L (L in µm)	V^{-1}
Bulk threshold parameter GAMMA	0.6	0.6	$V^{1/2}$
Surface potential PHI	0.8	0.8	V
Gate-Drain overlap capacitance. CGDO	5×10^{-10}	5×10^{-10}	F/m
Gate-Source overlap capacitance. CGSO	5×10^{-10}	5×10^{-10}	F/m
Zero-bias planar bulk depeltion capacitance CJ	10^{-4}	3×10^{-4}	F/m^2
Zero-bias sidewall bulk depletion capacitance CJSW	5×10^{-10}	3.5×10^{-10}	F/m
Bulk junction potential PB	0.95	0.95	V
Planar bulk junction grading coefficient MJ	0.5	0.5	
Sidewall bulk junction grading coefficient MJSW	0.33	0.33	