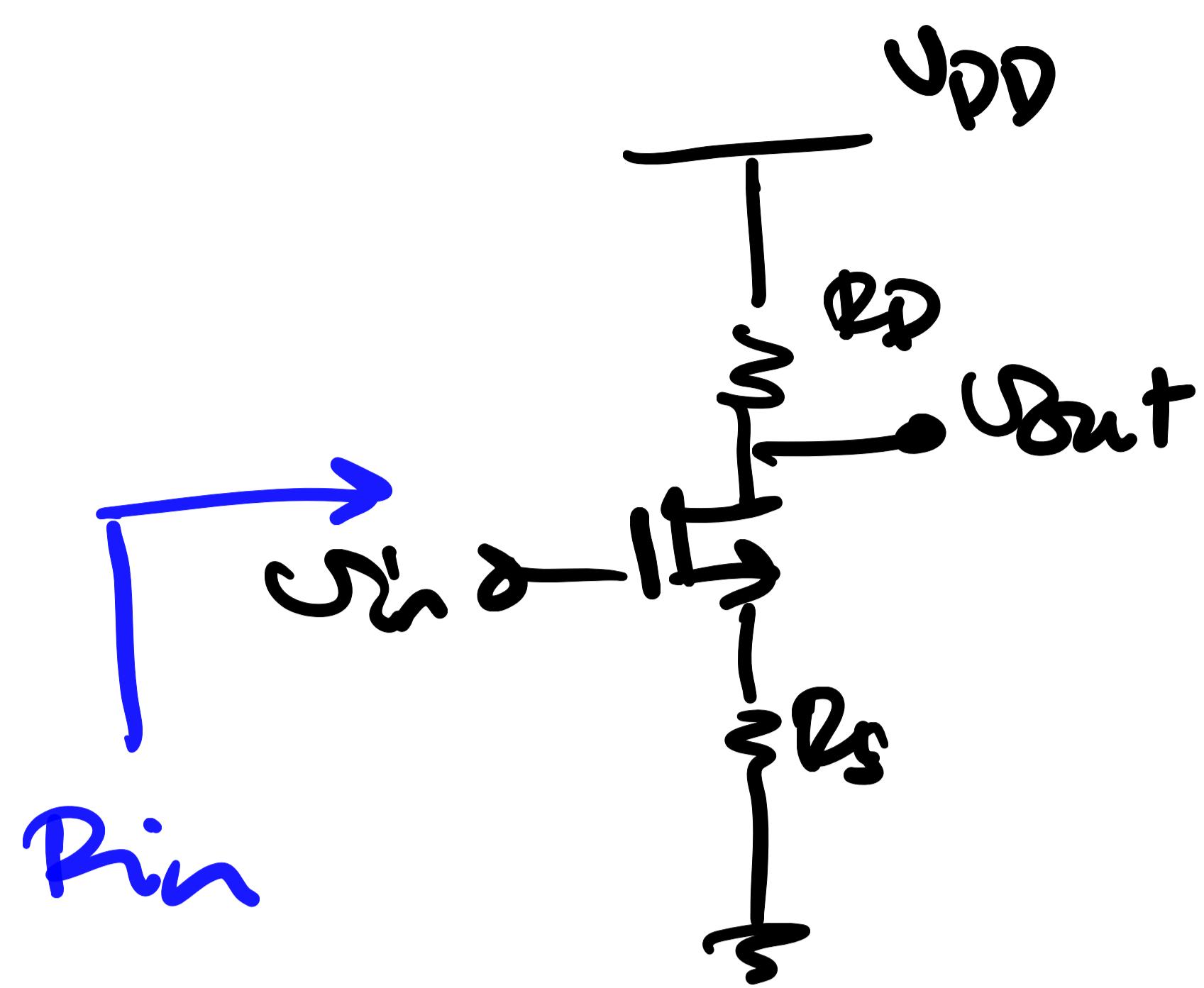


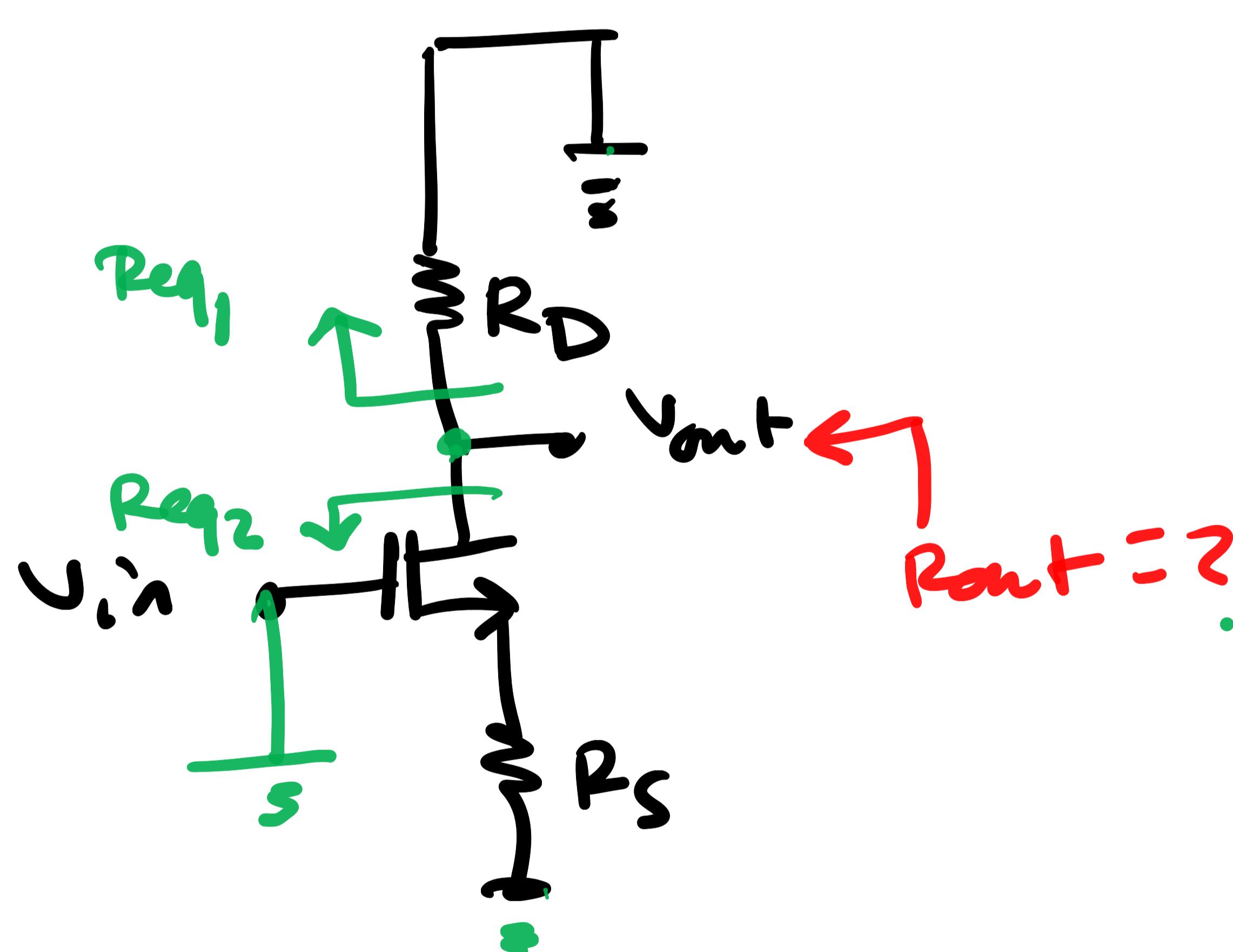
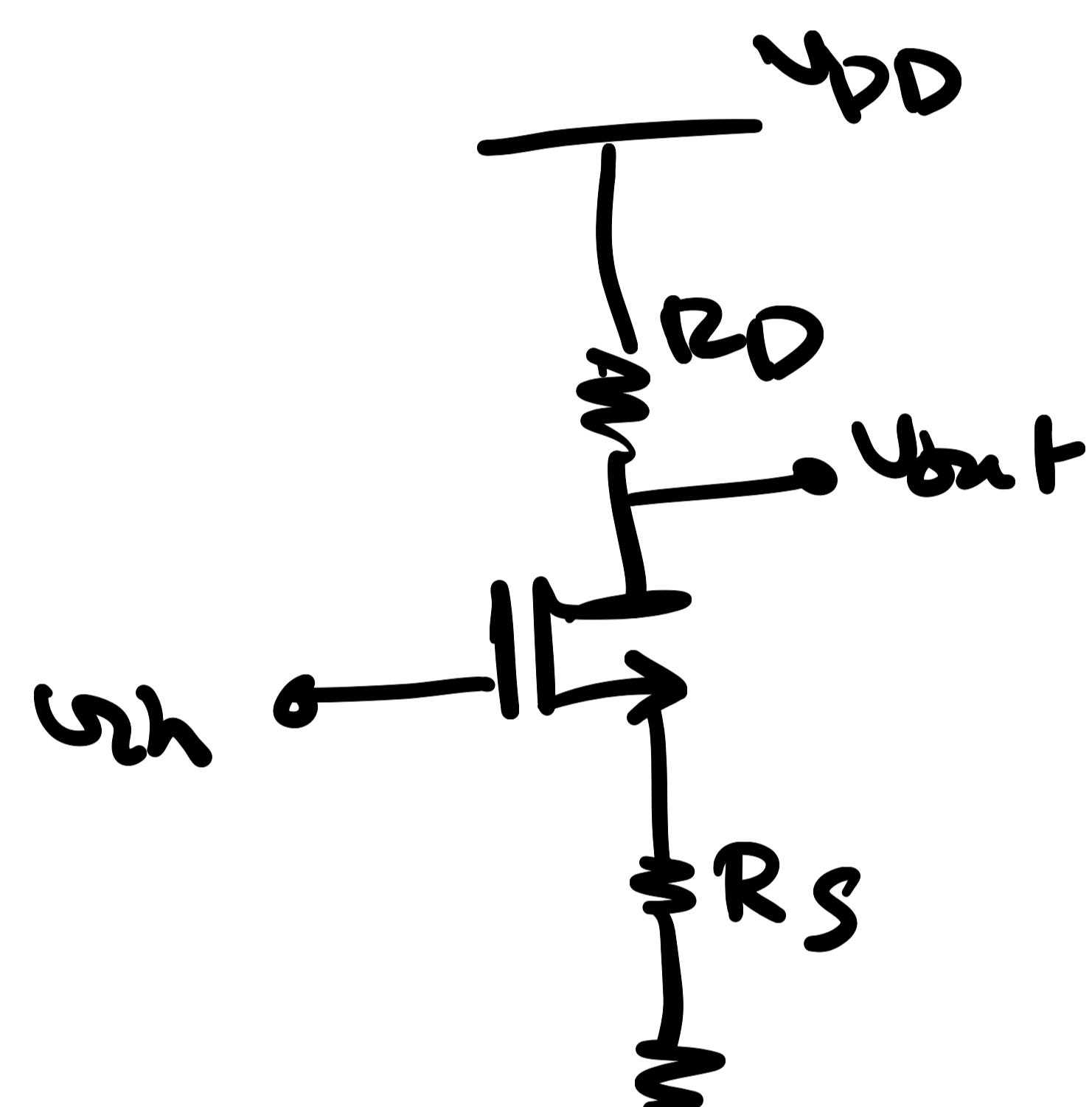
\*  $R_{in}$  for a degenerated stage :-



$$R_{in} = \infty$$

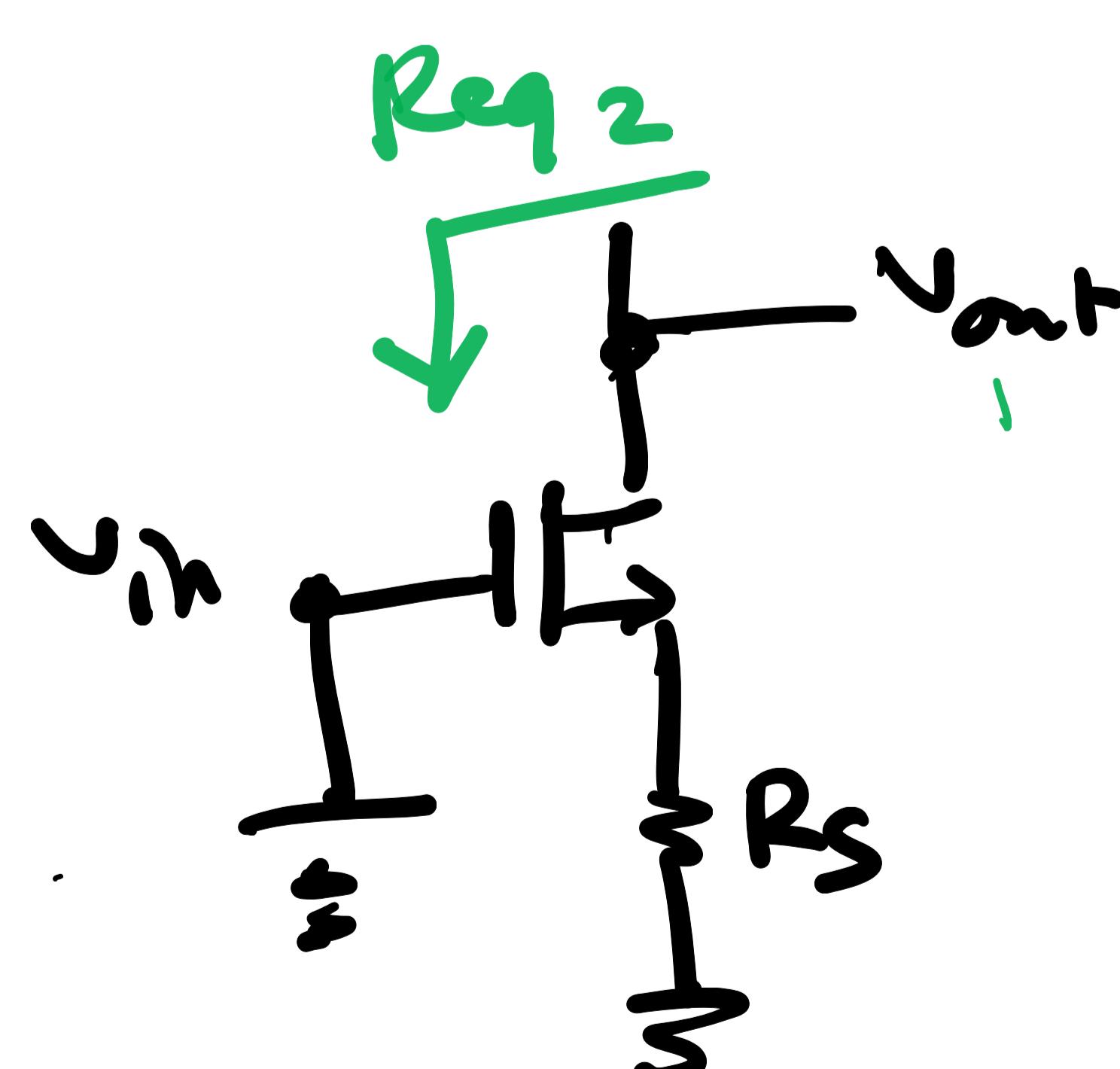
\*  $R_{out}$  for a CS degenerated stage :-

$$\lambda \neq 0$$



$$R_{out} = Req_1 \parallel Req_2$$

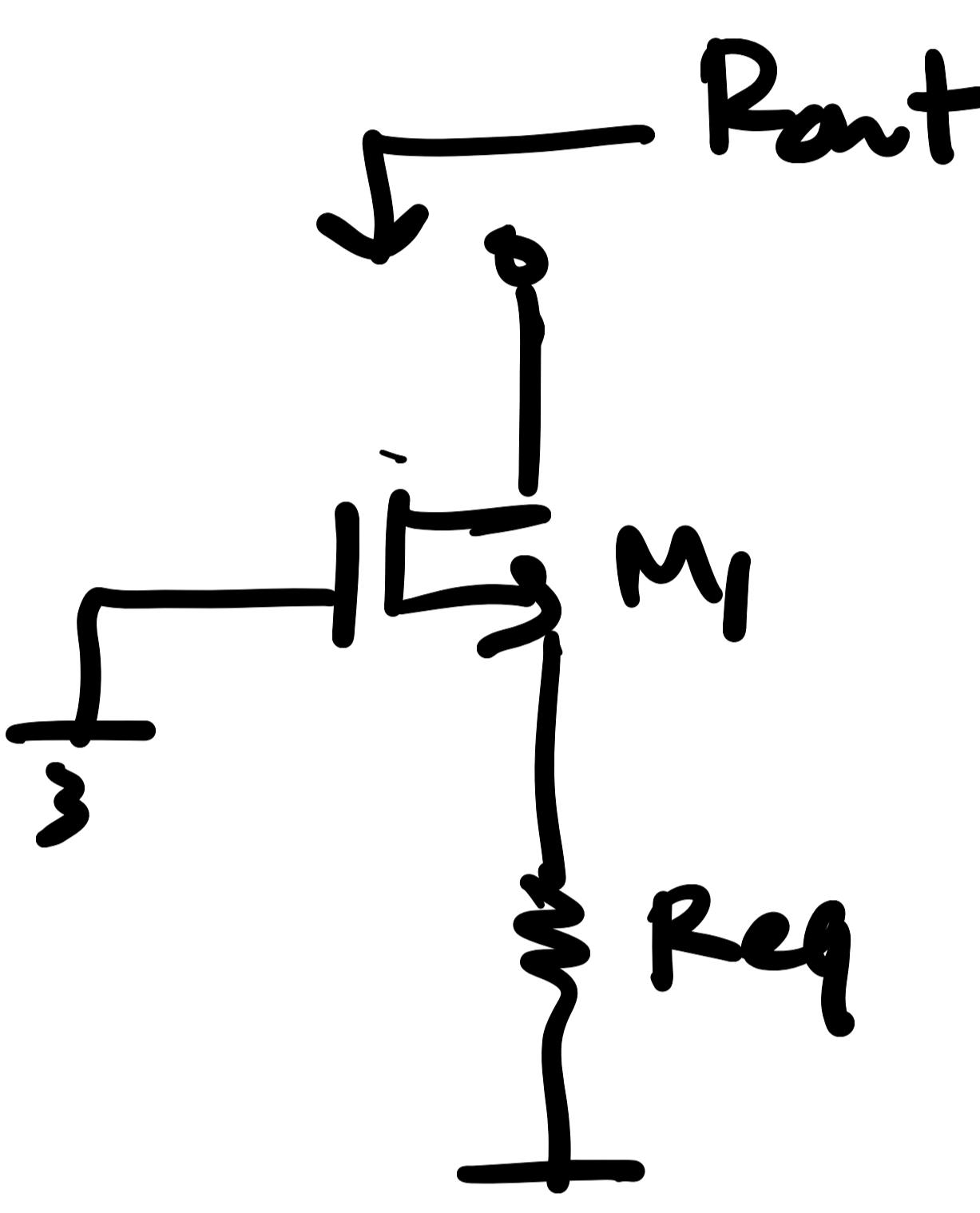
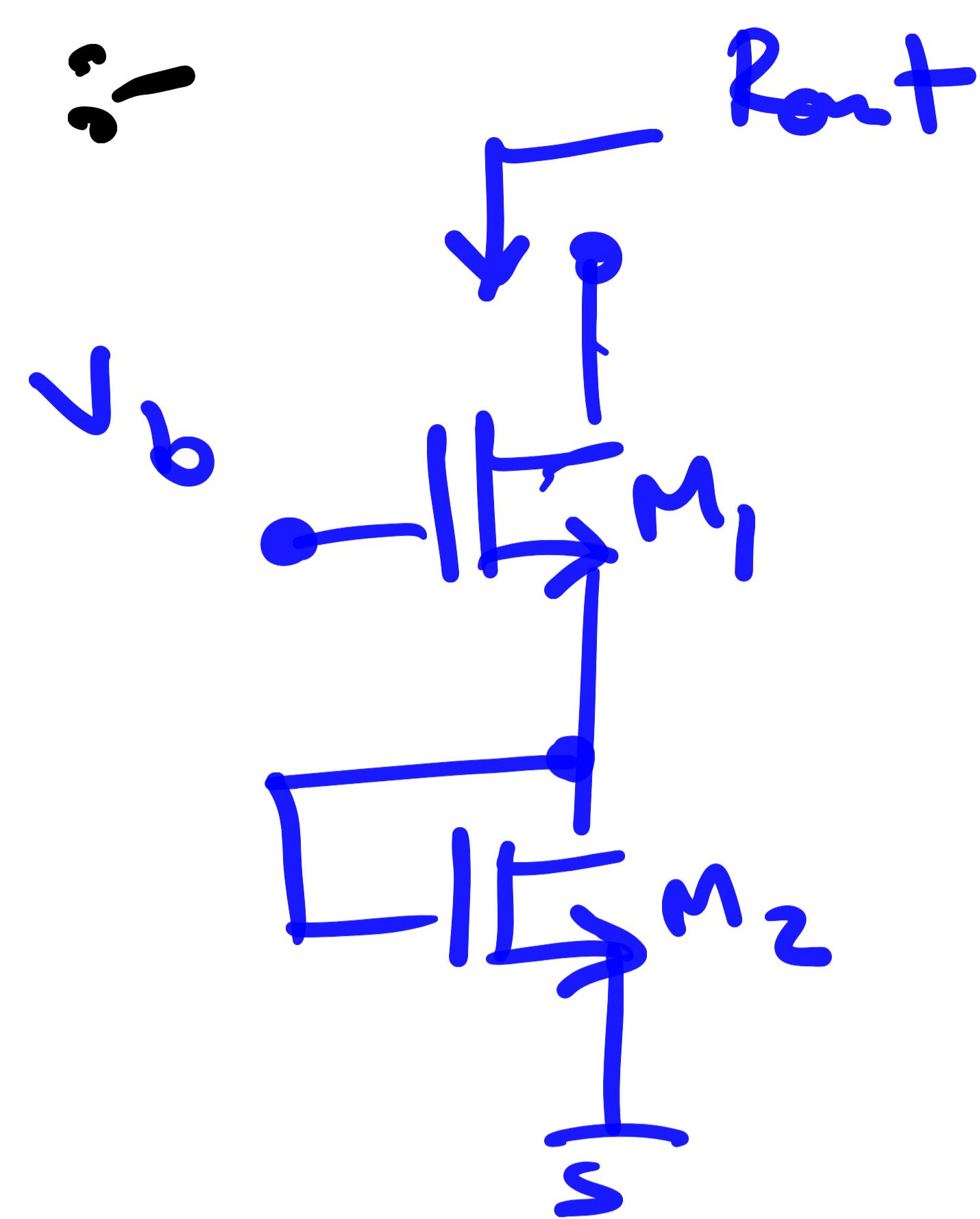
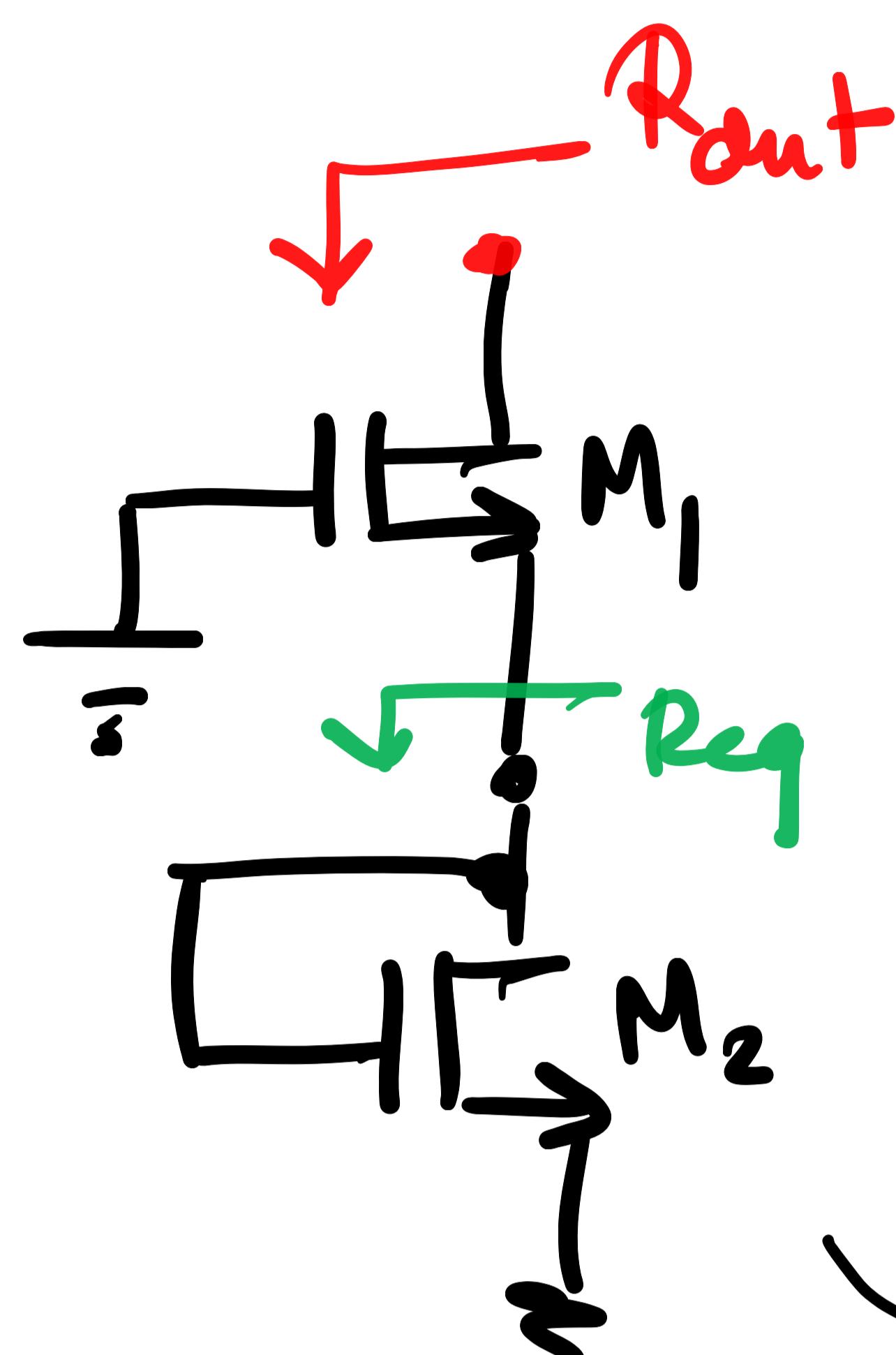
$$Req_1 = R_D$$



$$Req_2 = (1 + g_m R_S) \cdot r_o$$

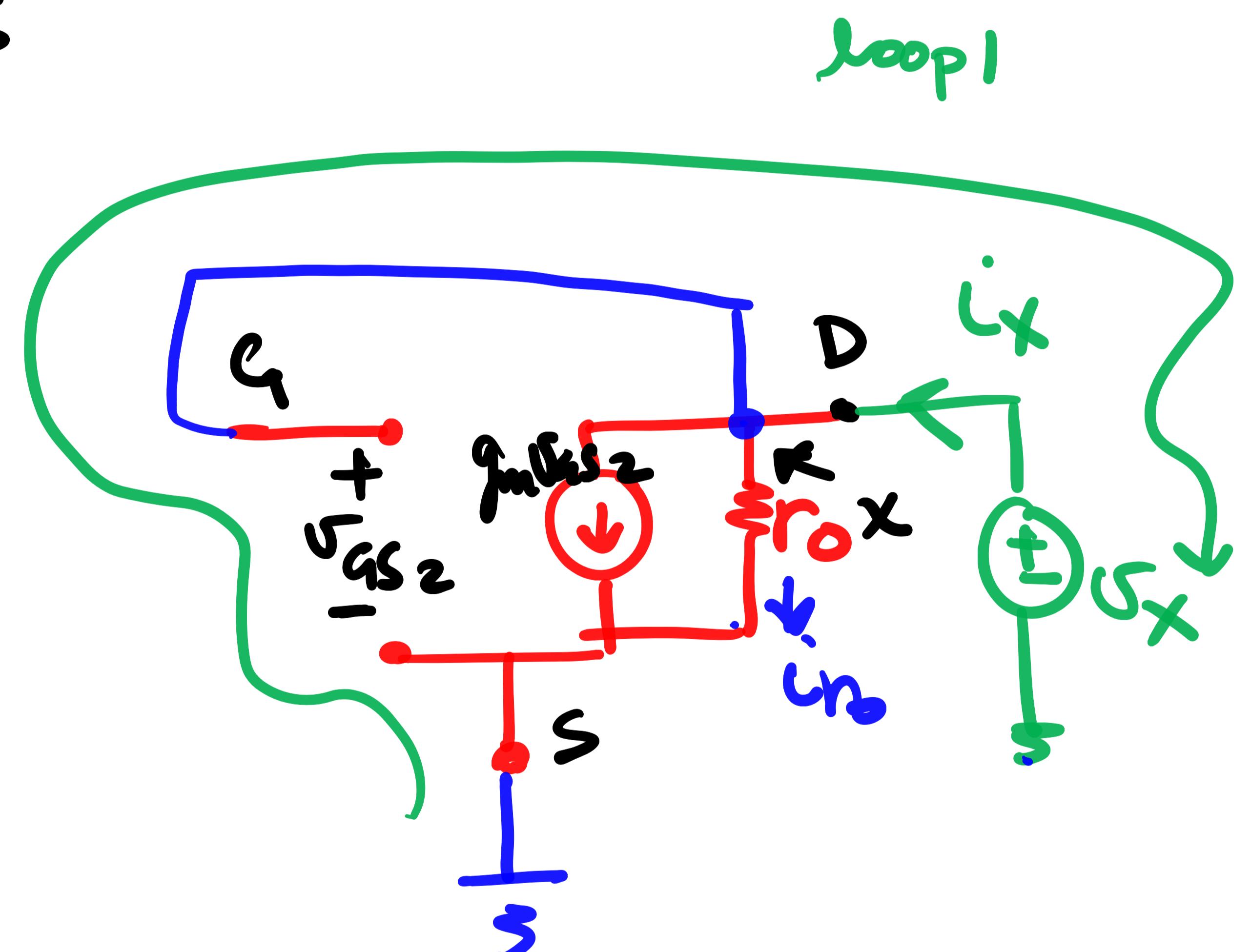
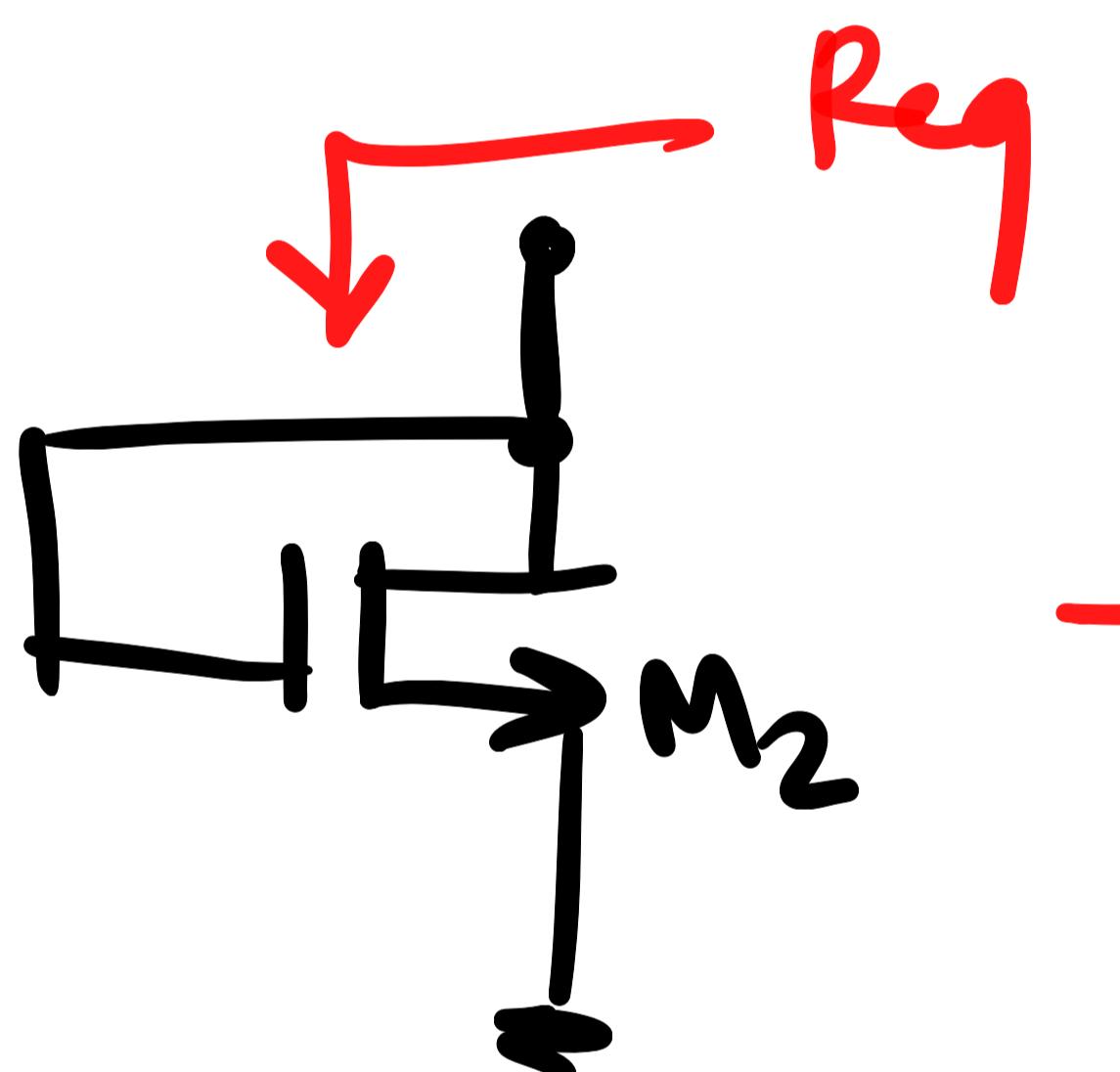
$$R_{out} = R_D \parallel (1 + g_m R_S) \cdot r_o$$

Ex: Find the output Resistance for this circuit assuming that  $M_1$  and  $M_2$  are identical :-



$$R_{out} = (1 + g_{M_1} \cdot Req) \cdot r_{o_1}$$

$$\Rightarrow Req = ?$$



$$Req = \frac{u_x}{i_x} ?$$

applying KCL @ node x :

$$i_x = g_{m_2} u_{AS2} + i_{ro} \Rightarrow u_{ro} = u_x \Rightarrow i_{ro} = \frac{u_x}{r_{o_2}}$$

applying KVL to loop 1

$$-u_{AS2} + u_x = 0 \Rightarrow u_x = u_{AS2}$$

$$\dot{v}_x = g_{m_2} v_x + \frac{v_x}{r_{02}} \Rightarrow \dot{v}_x = \left( g_{m_2} + \frac{1}{r_{02}} \right) \cdot v_x$$

$$\frac{v_x}{\dot{v}_x} = \frac{1}{g_{m_2} + \frac{1}{r_{02}}} \Rightarrow R_{eq} = \frac{1}{\frac{1}{g_{m_2}} + \frac{1}{r_{02}}} = \left( \frac{1}{g_{m_2}} \parallel r_{02} \right)$$

$$R_{ant} = \left[ 1 + g_{m_1} \left( \frac{1}{g_{m_2}} \parallel r_{02} \right) \right] \cdot r_{01} \Rightarrow \frac{1}{g_{m_2}} \ll r_{02}$$

$\downarrow$

$$R_{ant} = \left( 1 + g_{m_1} \cdot \frac{1}{g_{m_2}} \right) \cdot r_{01}$$

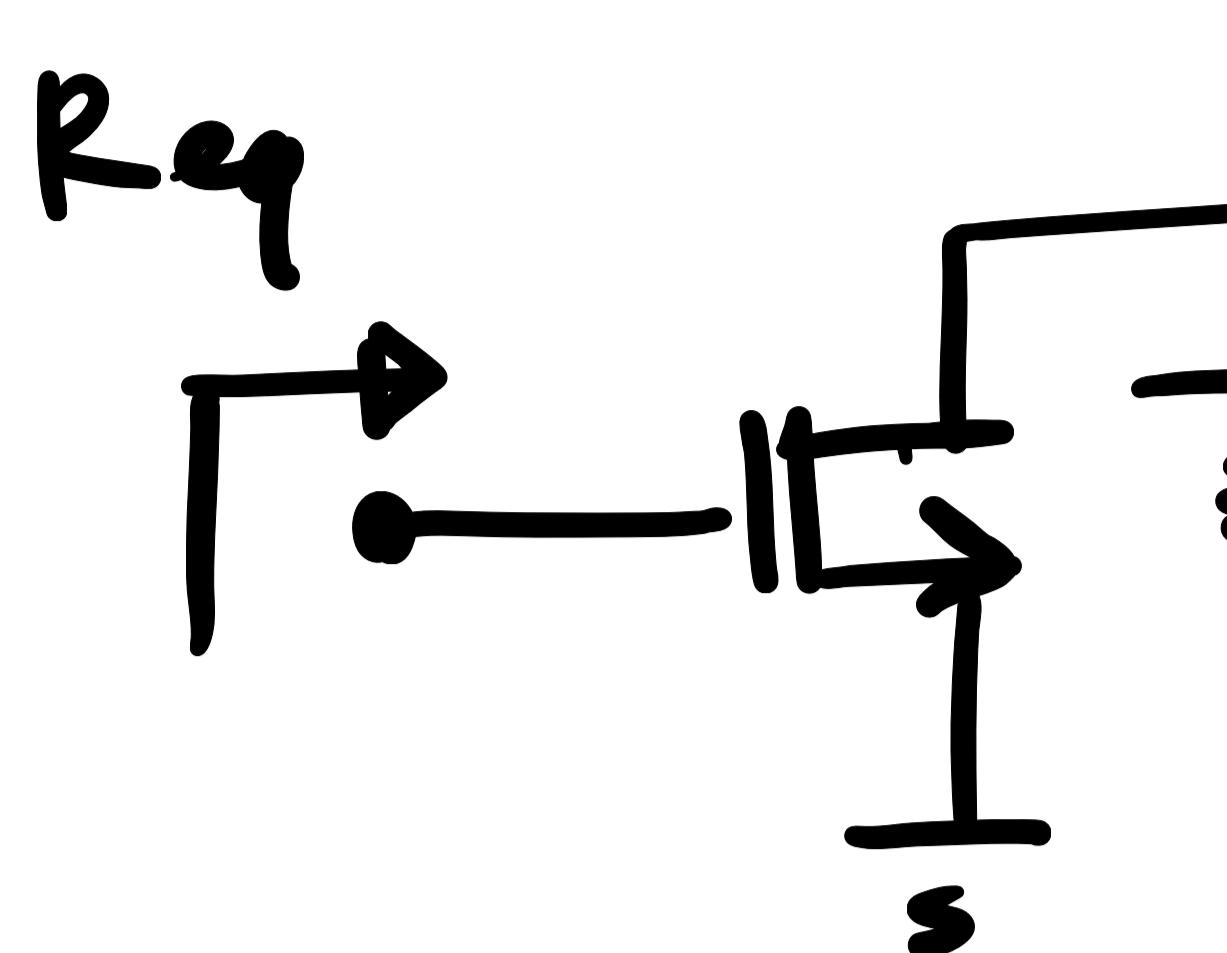
$$\left( \frac{1}{g_{m_2}} \parallel r_{02} \right) \approx \frac{1}{g_{m_2}}$$

Since  $m_1$  and  $m_2$  are identical then

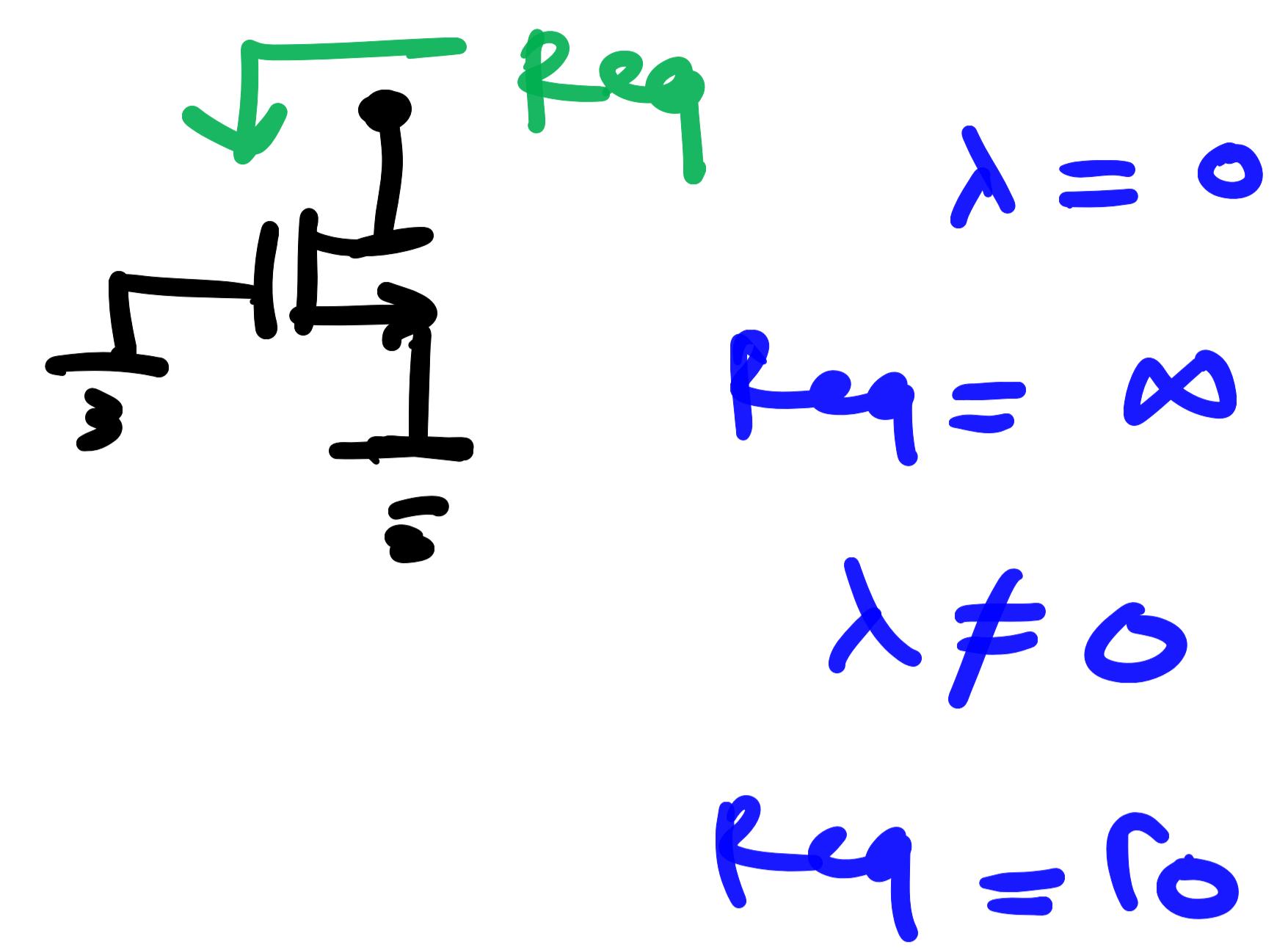
$$g_{m_1} = g_{m_2}, \quad r_{01} = r_{02}$$

$$\Rightarrow R_{ant} \cong \boxed{2 \ r_0}$$

## \* A quick revision for equivalent impedance :-

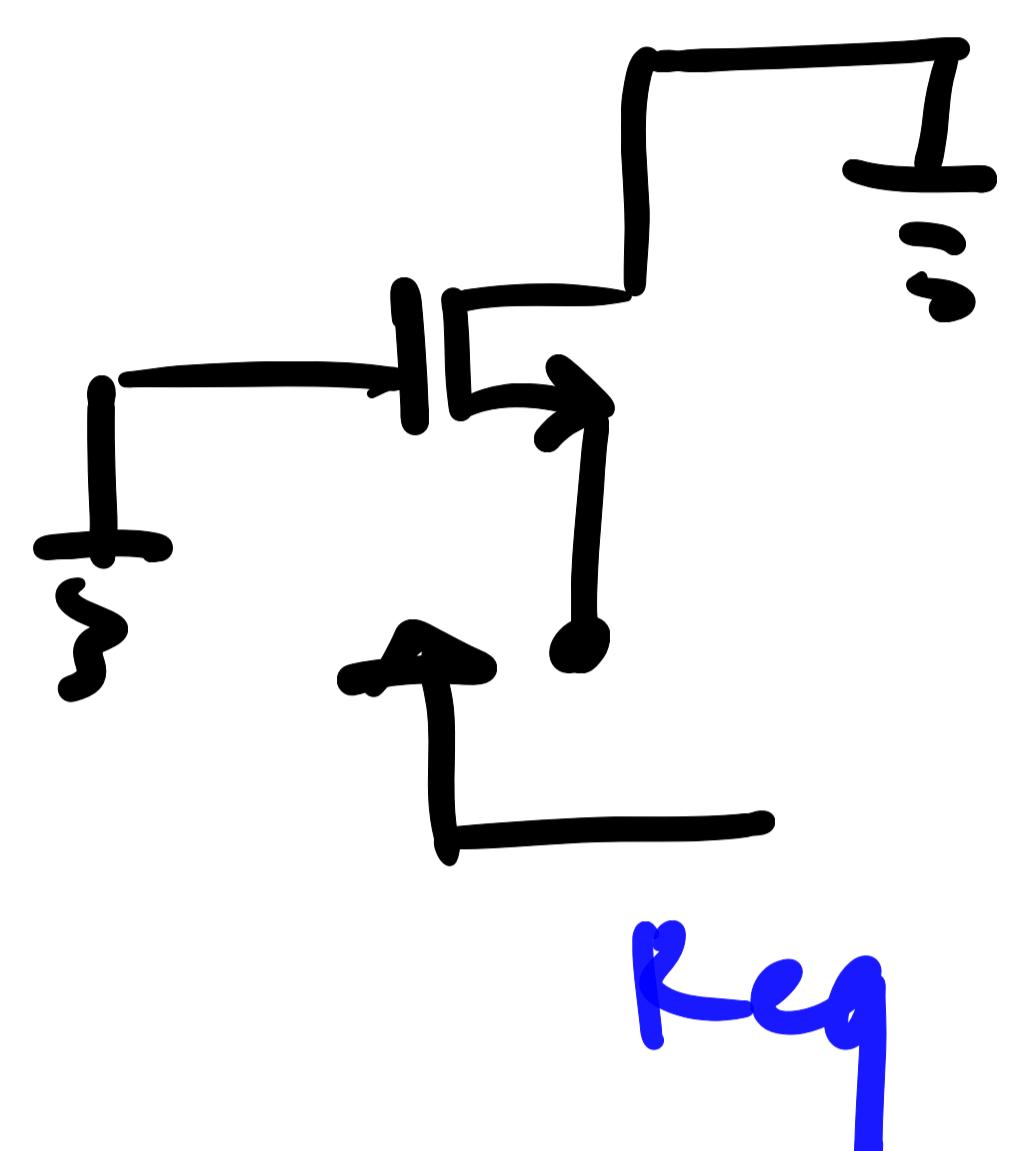


$$\lambda = 0, \lambda \neq 0 \Rightarrow R_{eq} = \infty$$



$$\lambda = 0 \quad R_{eq} = \infty$$

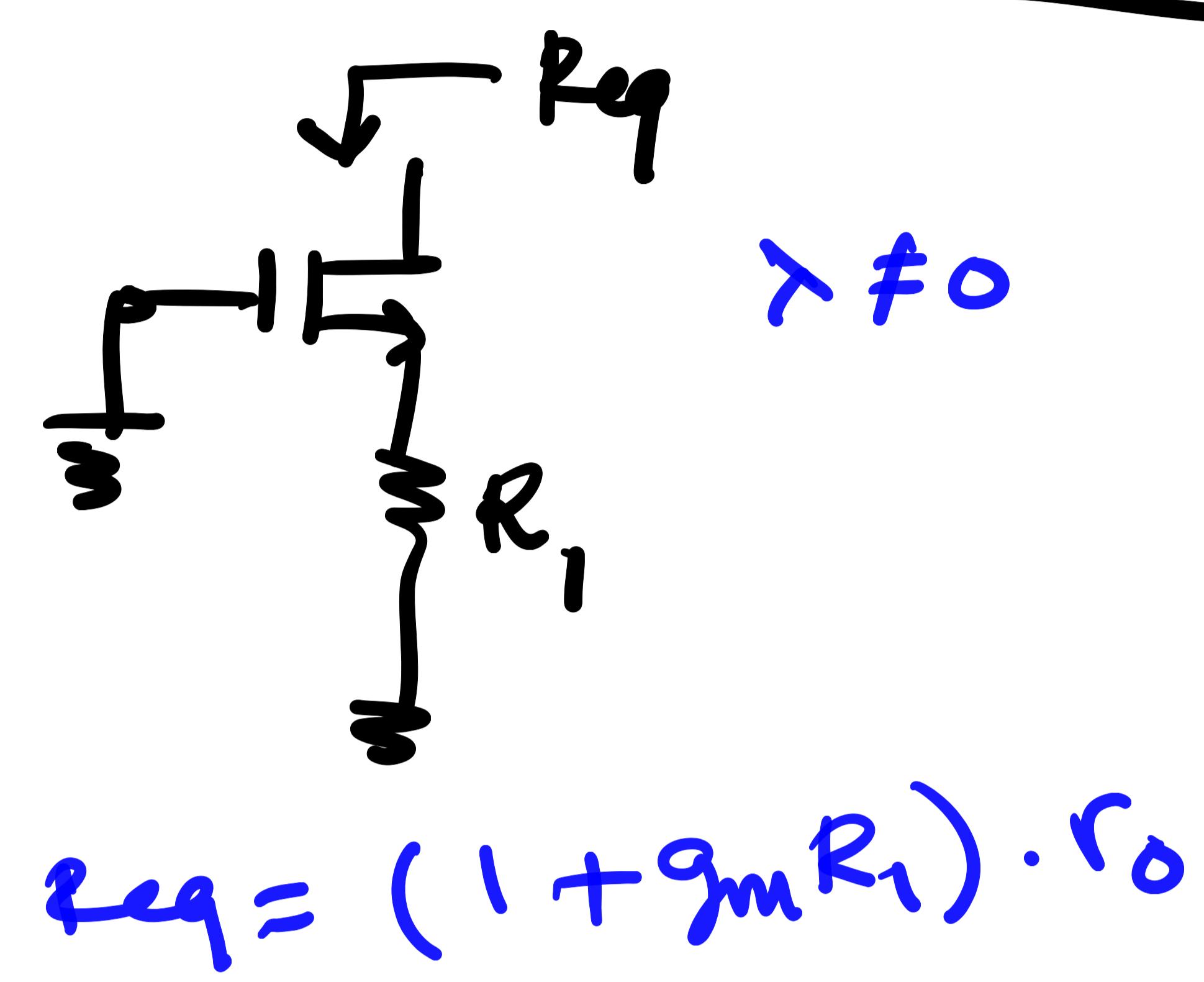
$$\lambda \neq 0 \quad R_{eq} = r_o$$



$$\lambda = 0 \quad R_{eq} = \frac{1}{g_m}$$

$$\lambda \neq 0$$

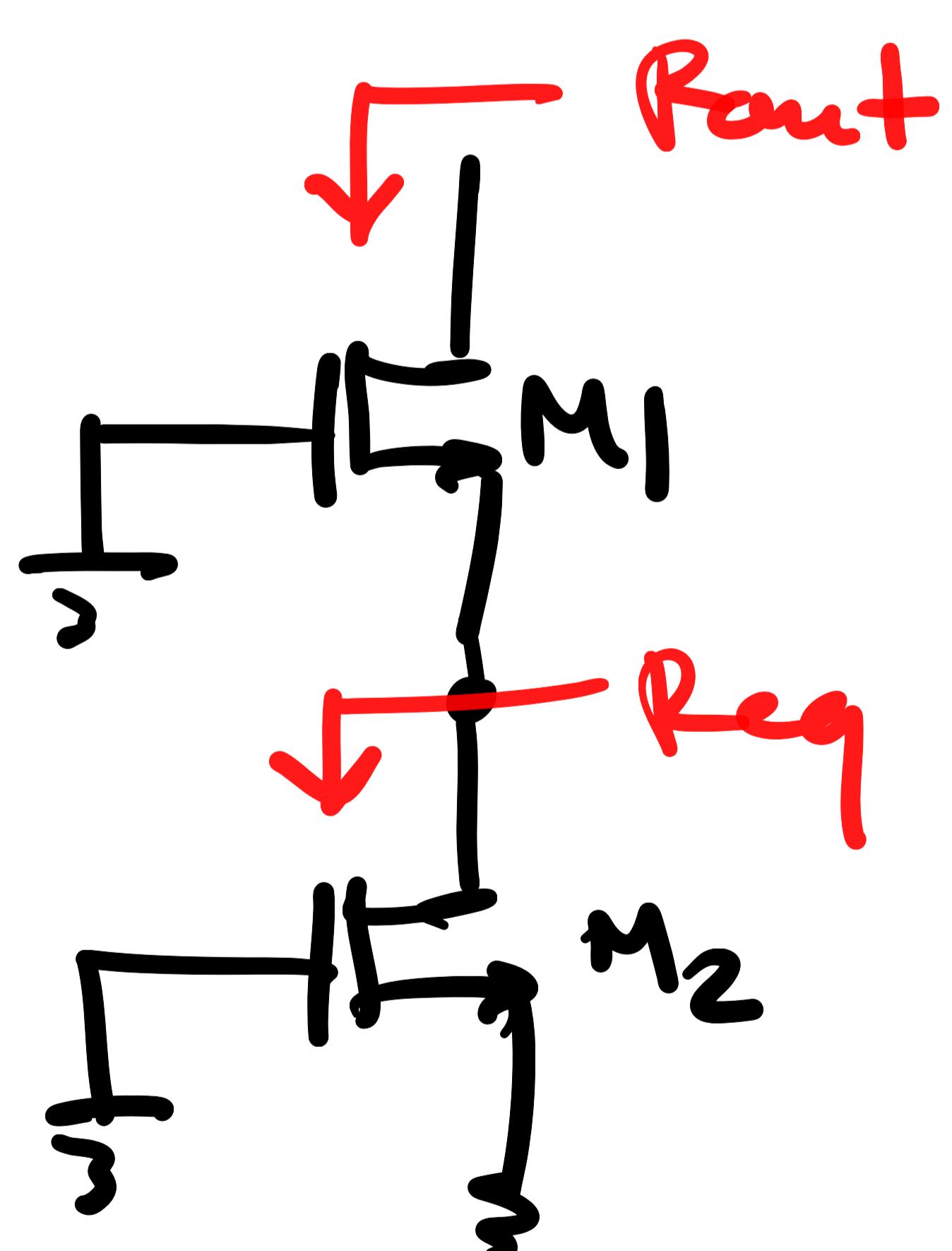
$$Y_{gm} \parallel r_o \approx \frac{1}{g_m}$$



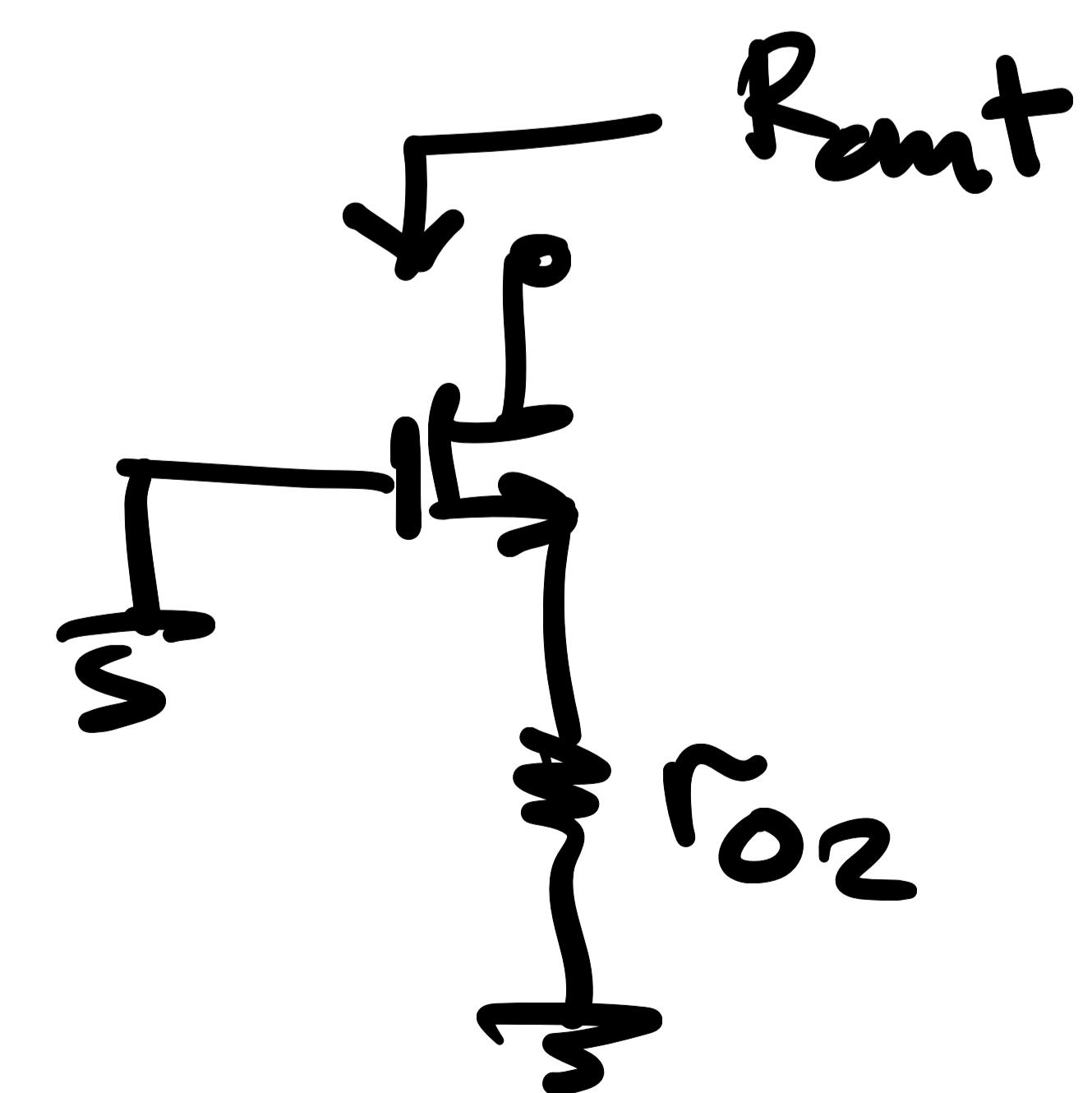
$$\lambda = 0$$

$$R_{eq} = \infty$$

Ex: Find  $R_{out}$  for this cct :-  $\lambda \neq 0$

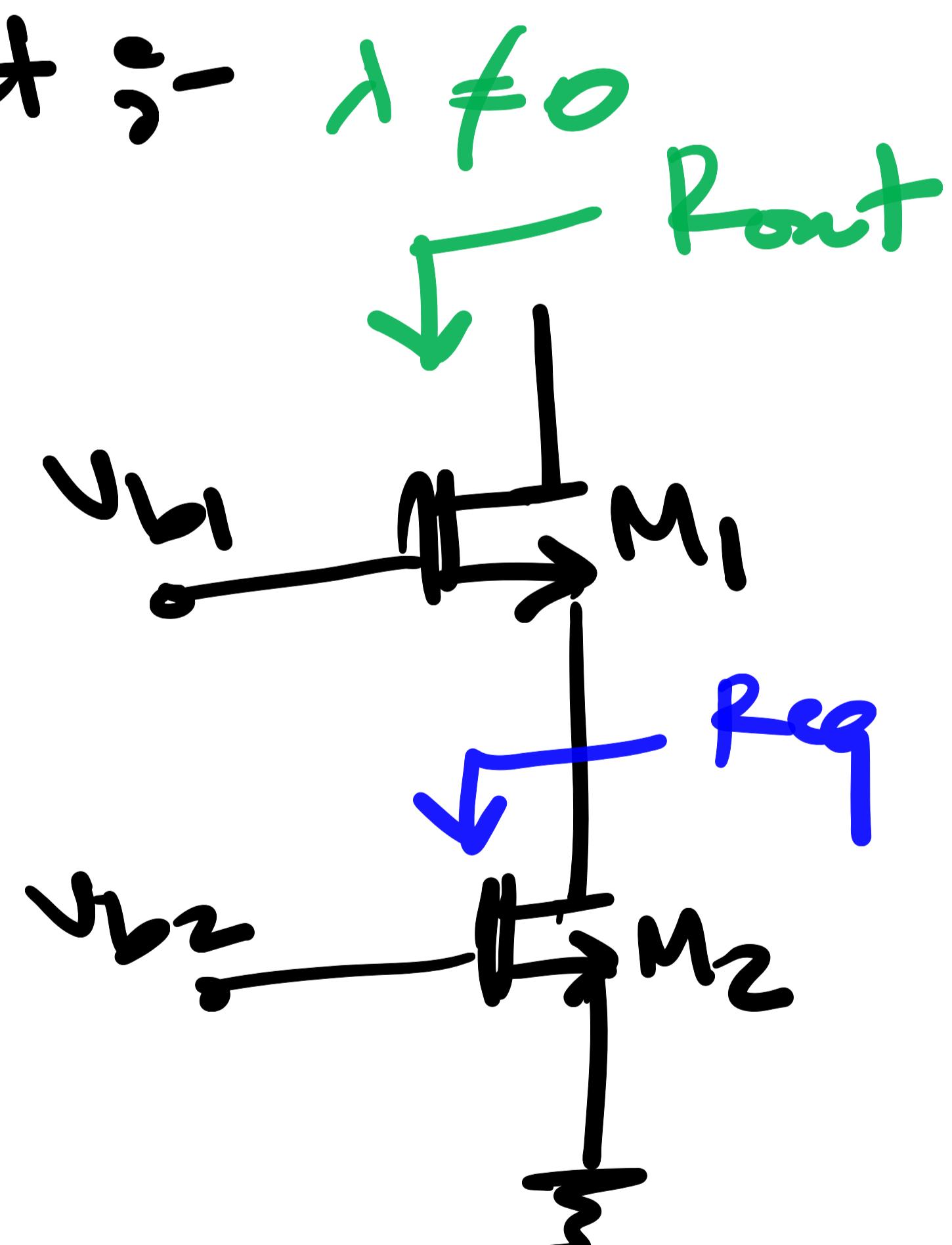


$$R_{eq} = r_{o2} \rightarrow$$

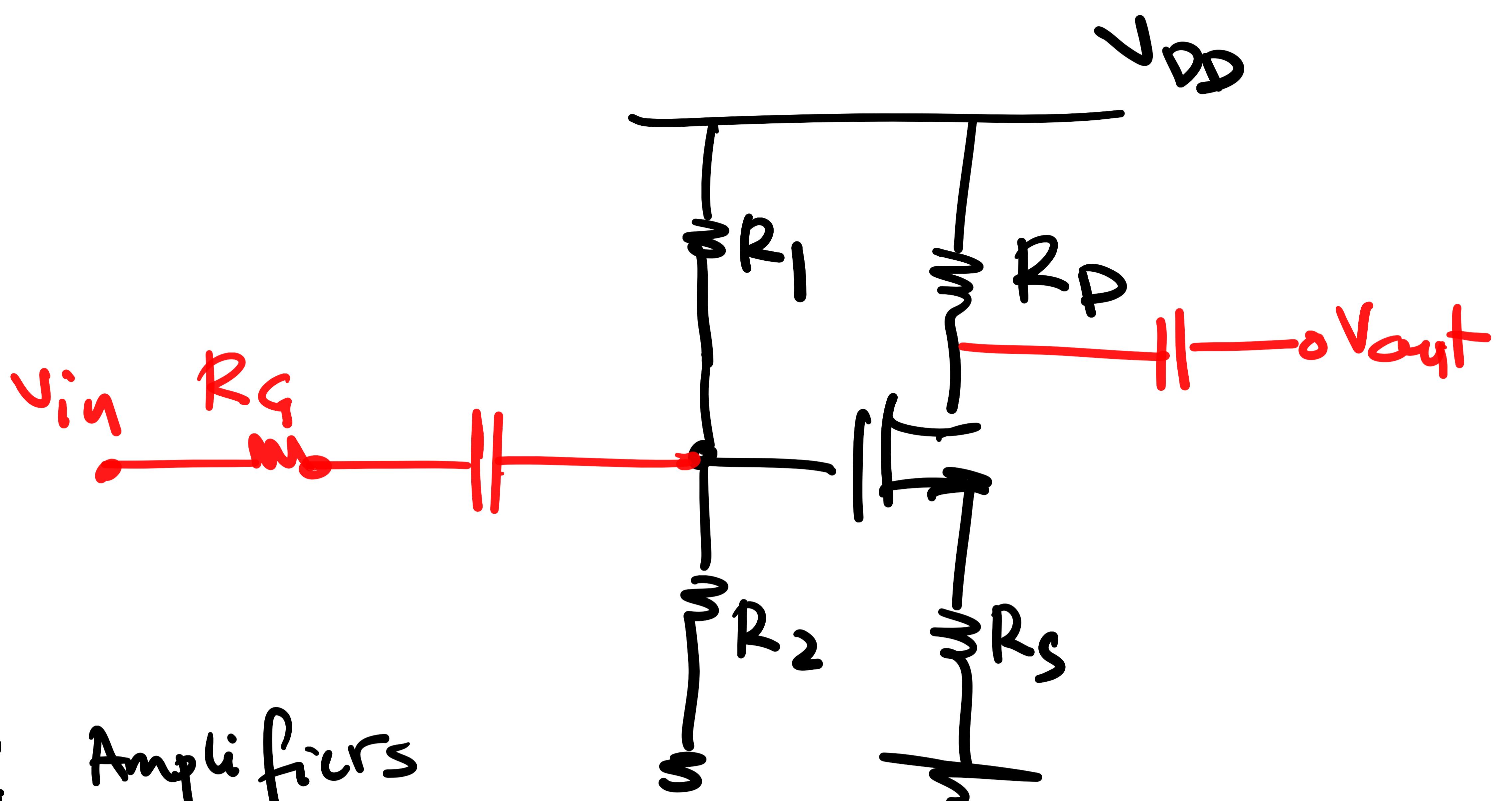


$$\Rightarrow R_{out} = (1 + g_{m1} r_{o2}) \cdot r_{o1}$$

$$R_{out} \approx g_{m1} r_{o1} r_{o2}$$



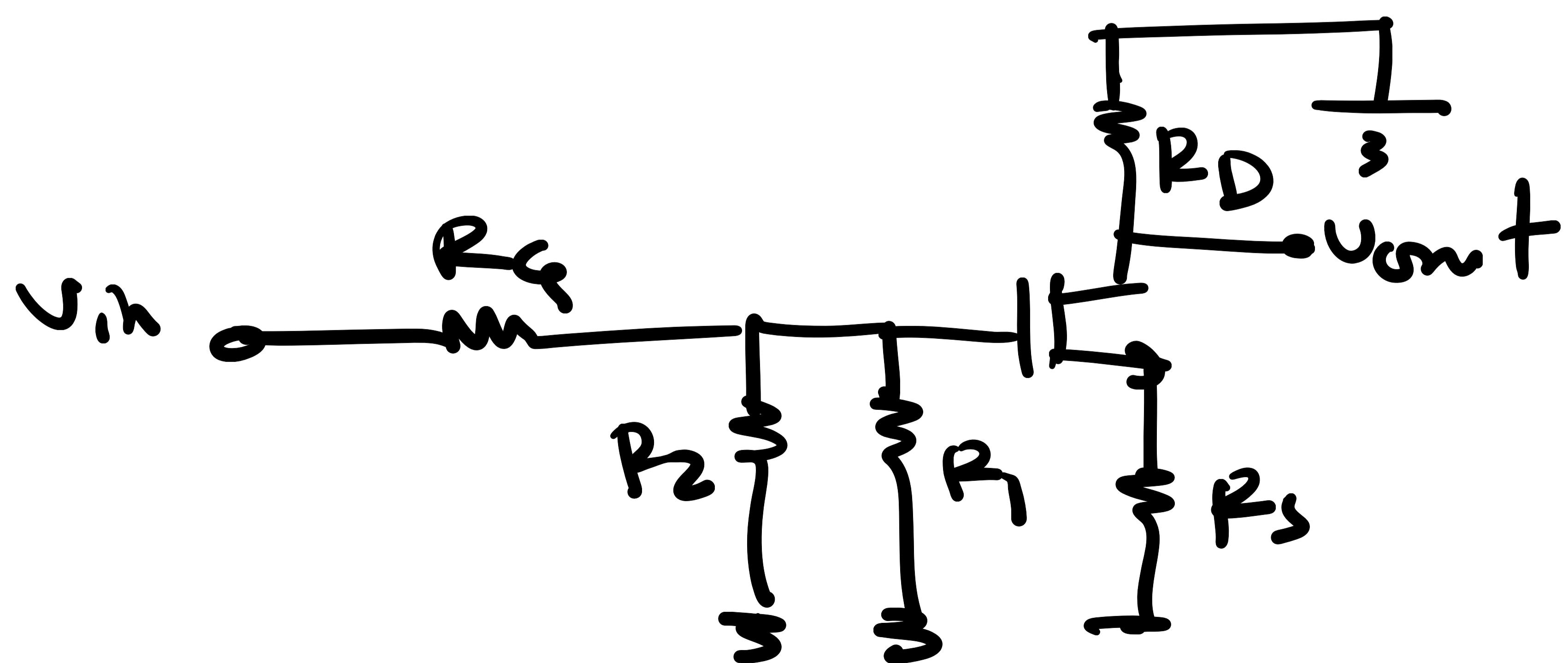
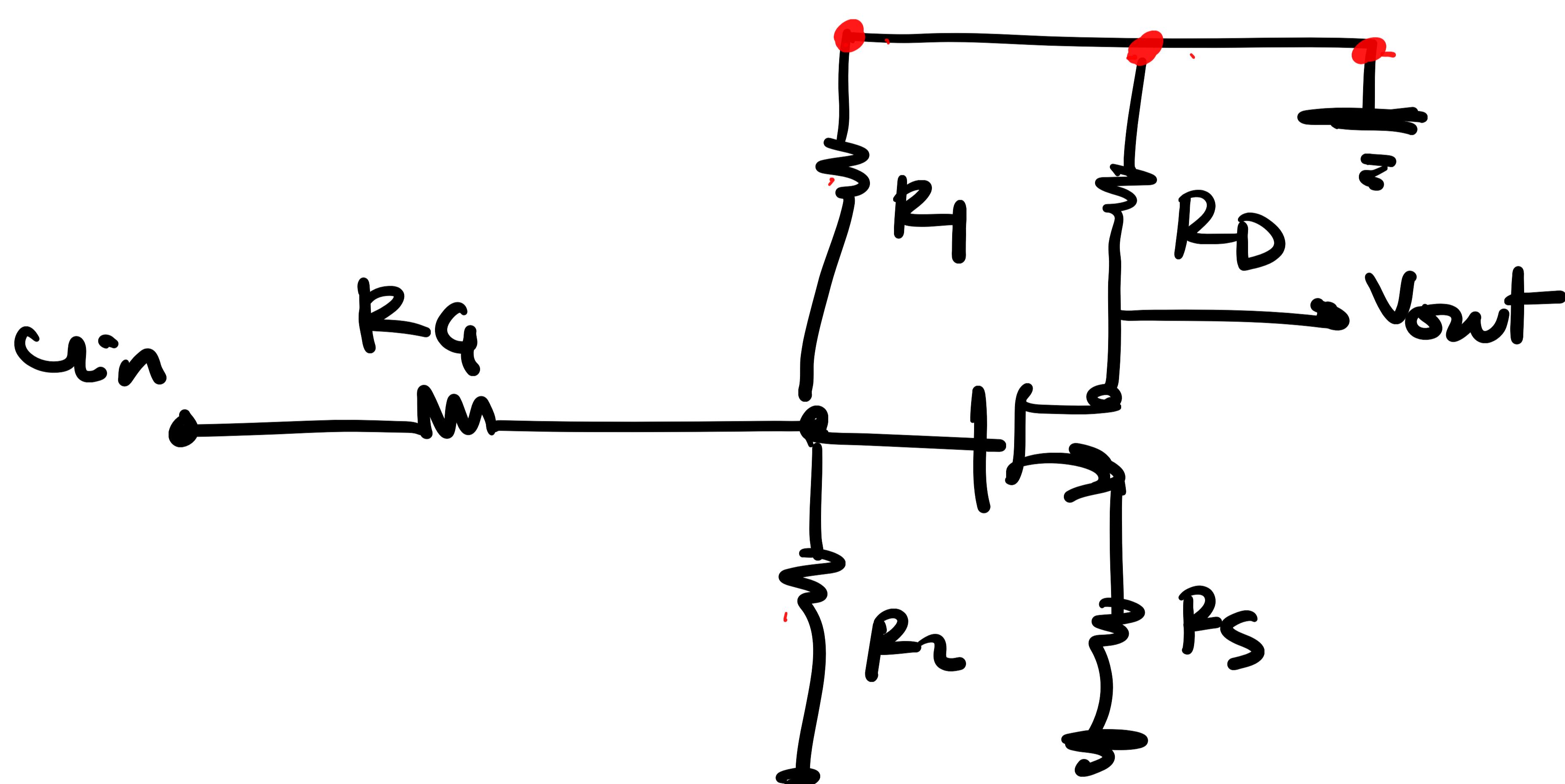
\* CS Core with Biasing :-

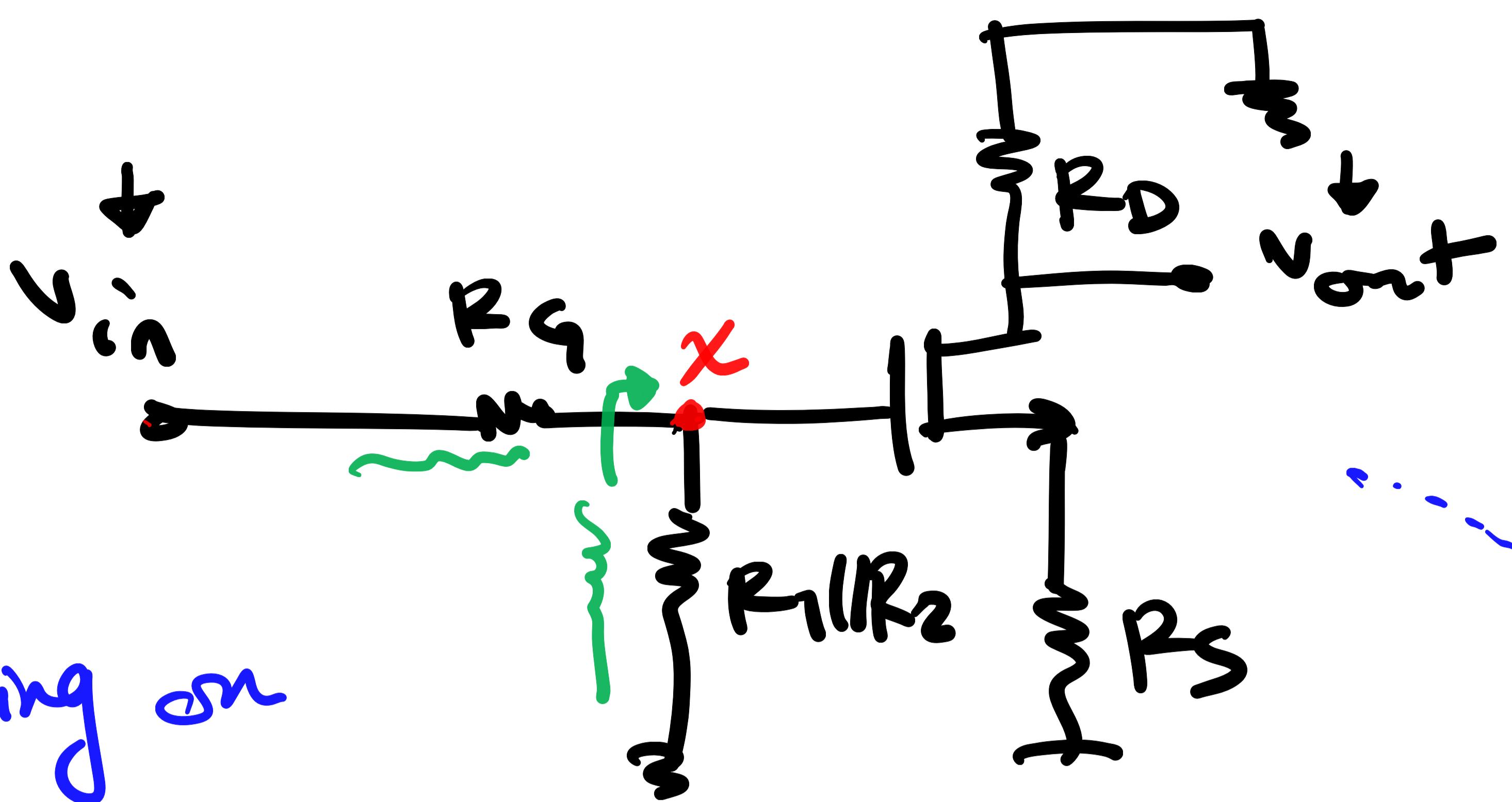


\* Analysing Amplifiers

with biasing :-

- ① deactivate DC voltage source
- ② short the capacitors





\* Effect of Biasing on  
small signal parameters:

fig (a)

$$* Av = \frac{V_{out}}{V_{in}} \rightarrow$$

$$\Rightarrow \frac{V_{out}}{V_X} = \frac{-R_D}{g_m + R_S}$$

$$\text{but } V_X = \frac{R_1 || R_2}{R_1 || R_2 + R_Q} \cdot V_{in}$$

$$\Rightarrow \frac{V_X}{V_{in}} = \frac{R_1 || R_2}{R_1 || R_2 + R_Q}$$

$$Av = \frac{V_{out}}{V_X} \cdot \frac{V_X}{V_{in}} = \frac{R_1 || R_2}{R_1 || R_2 + R_Q} \cdot \frac{-R_D}{g_m + R_S}$$

\* Effects on input Impedance :-

\* without  $R_1$  and  $R_2$  in fig (b)

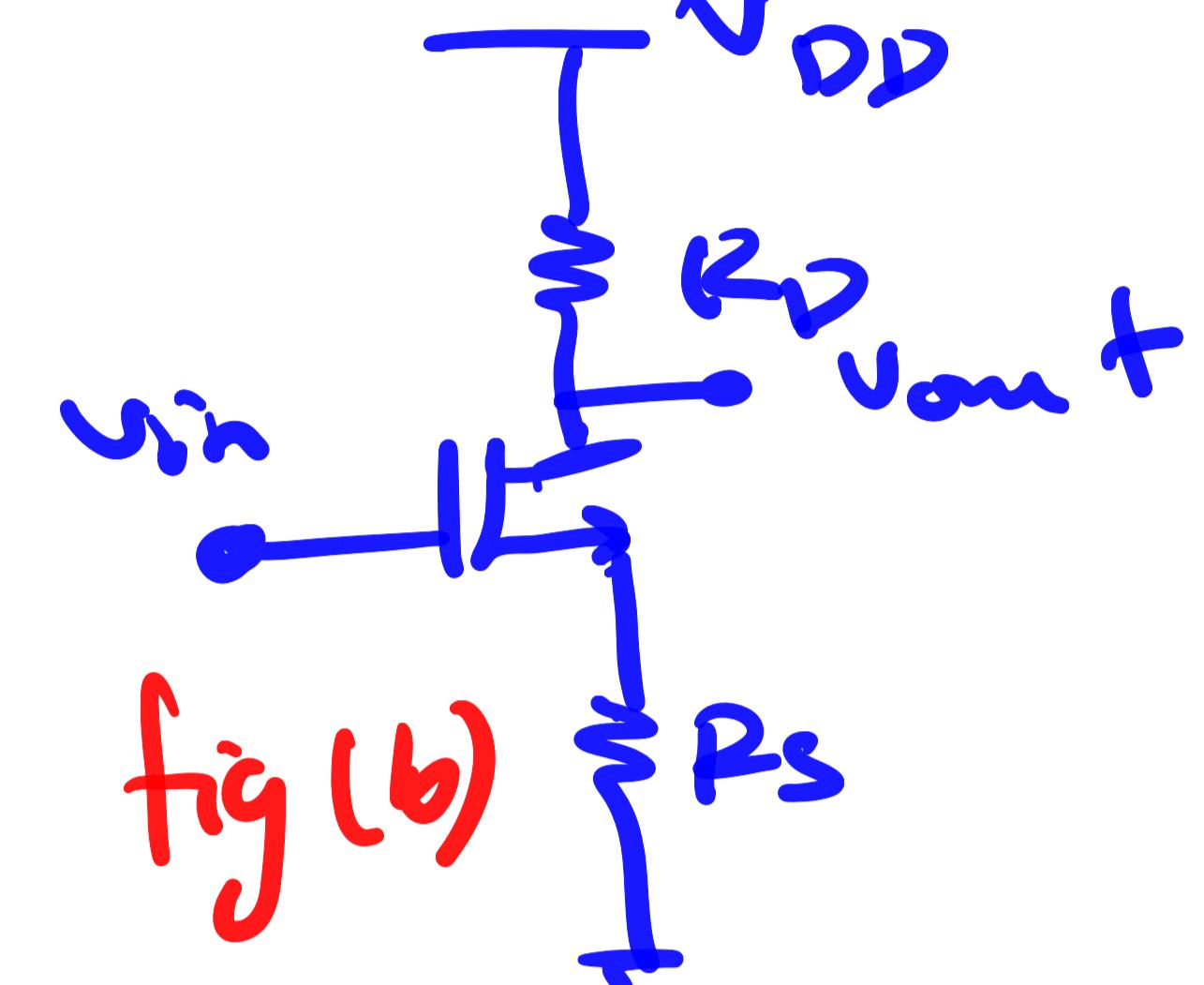
$$R_{in} = \infty$$

\* when biasing using  $R_1$  and  $R_2$  as shown in fig (a)

$$R_{in} = R_1 || R_2 \text{ looking through node } X$$

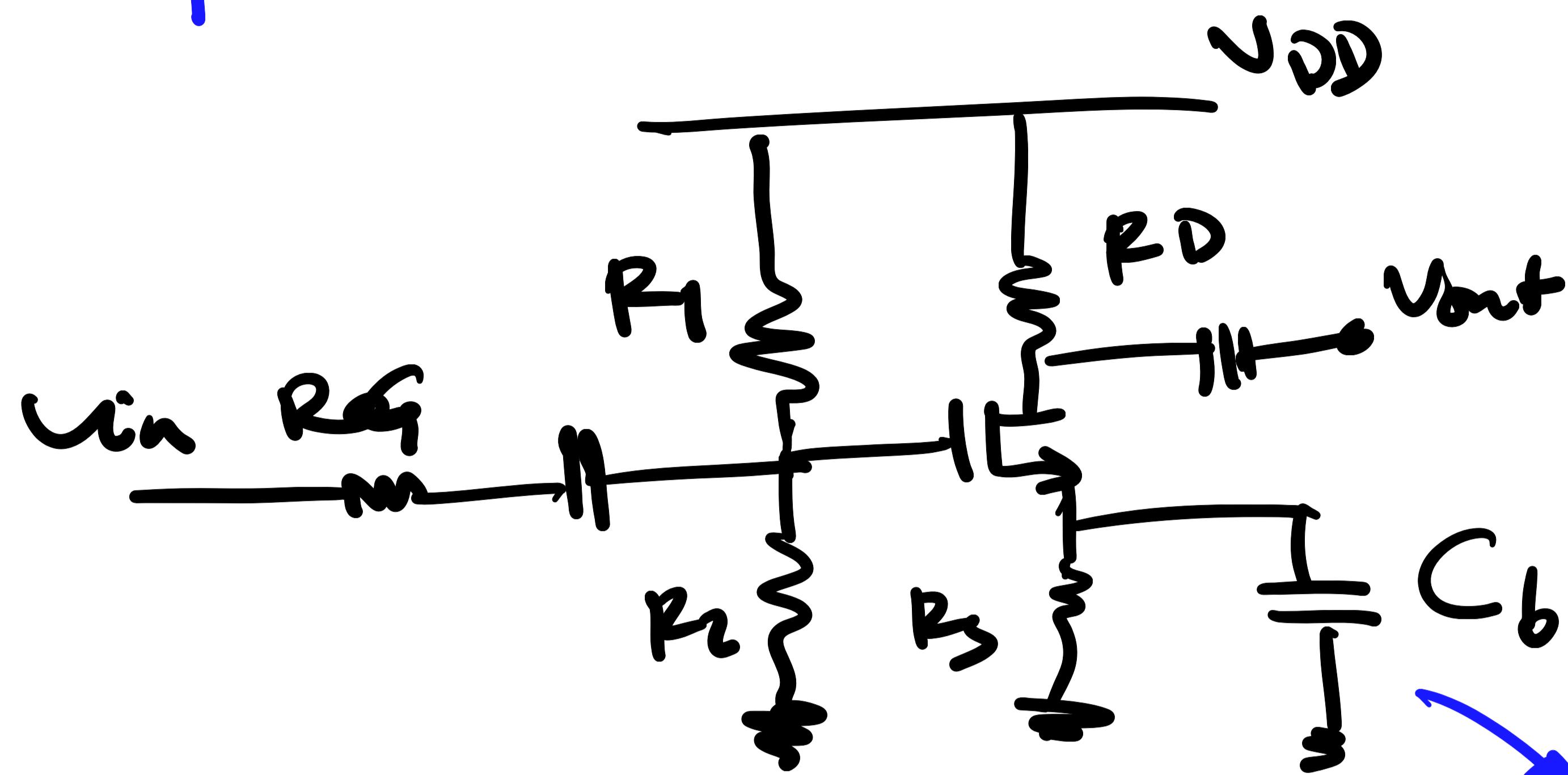
without Biasing

concerns



$$Av = \frac{-R_D}{g_m + R_S}$$

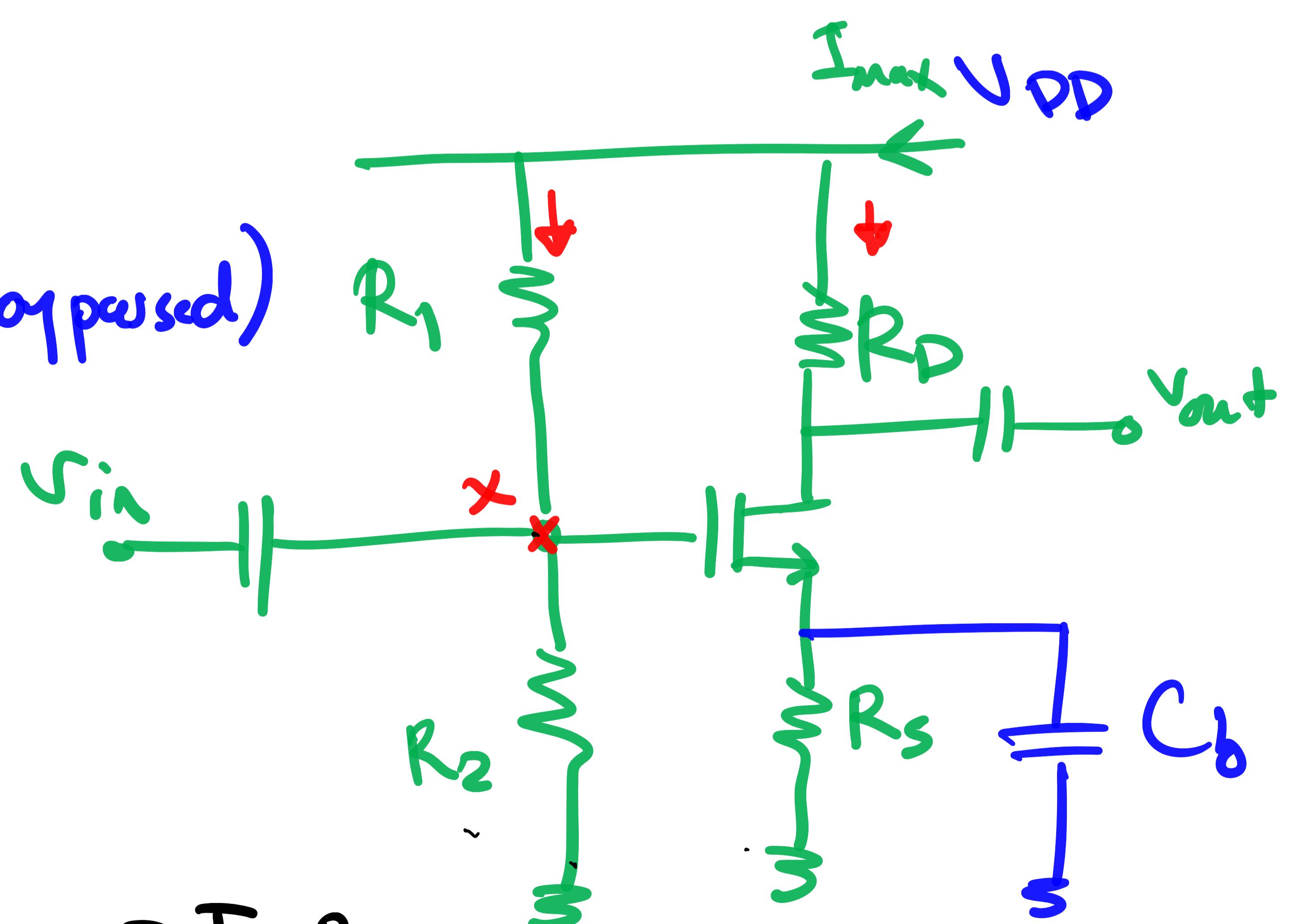
- \* To boost the gain and keep  $R_S$  we connect a bypass capacitor parallel to  $R_S$



- \* Considering small signal analysis
- $\Rightarrow A_v = \frac{R_1 \| R_2}{R_1 \| R_2 + R_S} \cdot -g_m R_D$
- this will act as a short.

Ex:- Design a CS stage with voltage divider biasing and degeneration so that  $|A_v| = 5$ ,  
 $\mu_n l_{ox} = 100 \mu A/V^2$ ,  $\lambda = 0$ , a power budget of 5mW and  $V_{DD} = 1.8V$ ,  $V_{TH} = 500mV$ ,  
an input impedance of 50 kΩ. Assume  $R_S$  is bypassed.

Sol:  $|A_v| = g_m R_D$  ( $R_S$  is bypassed)



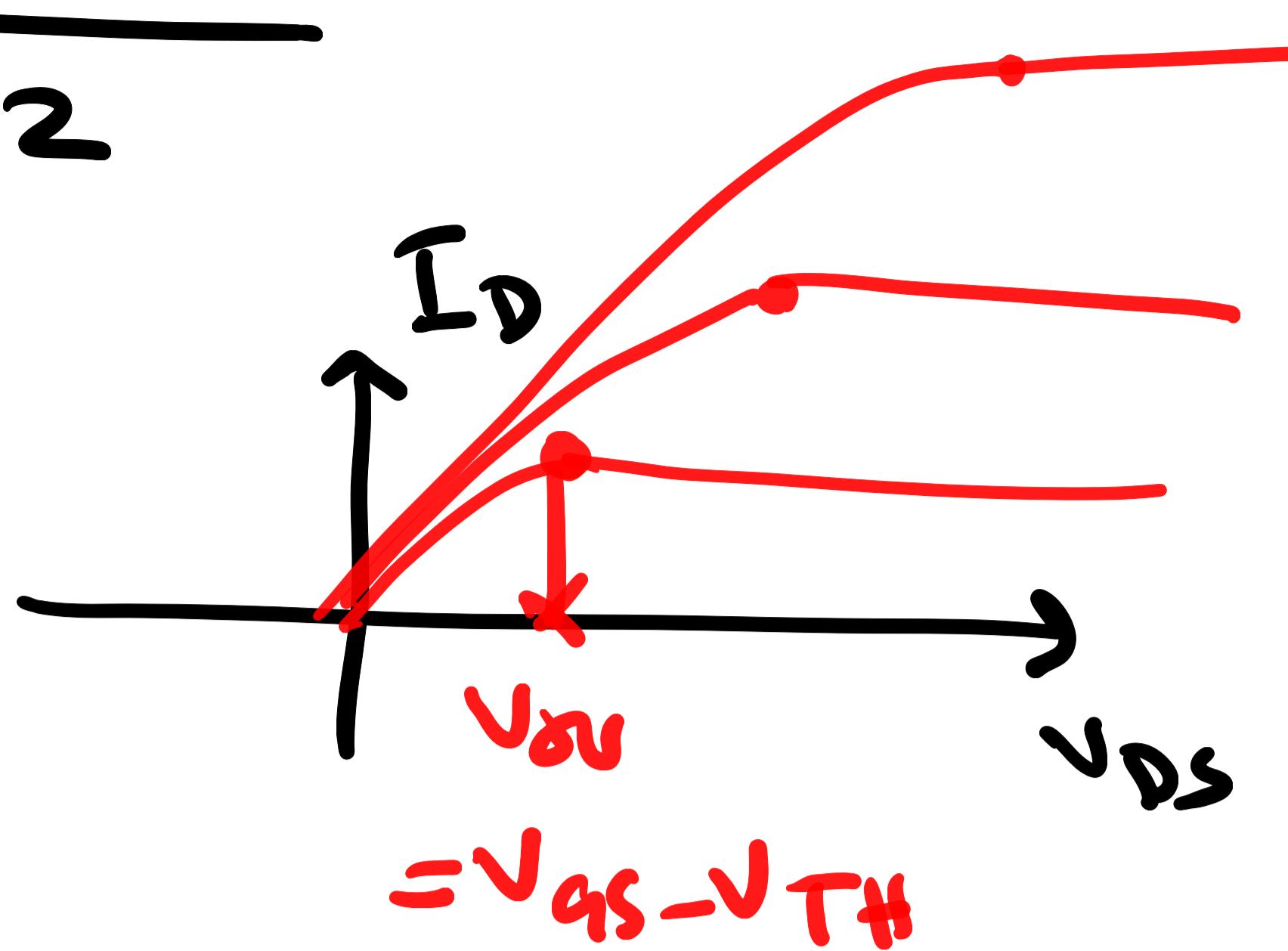
$$\Rightarrow 5 = g_m \cdot R_D$$

$$\Rightarrow g_m = \frac{2 I_D}{V_{ov}} \Rightarrow 5 = \frac{2 I_D \cdot R_D}{V_{ov}}$$

$$S = \frac{2V_{RD}}{V_{OV}} \Rightarrow V_{RD} = \frac{S \cdot V_{OV}}{2}$$

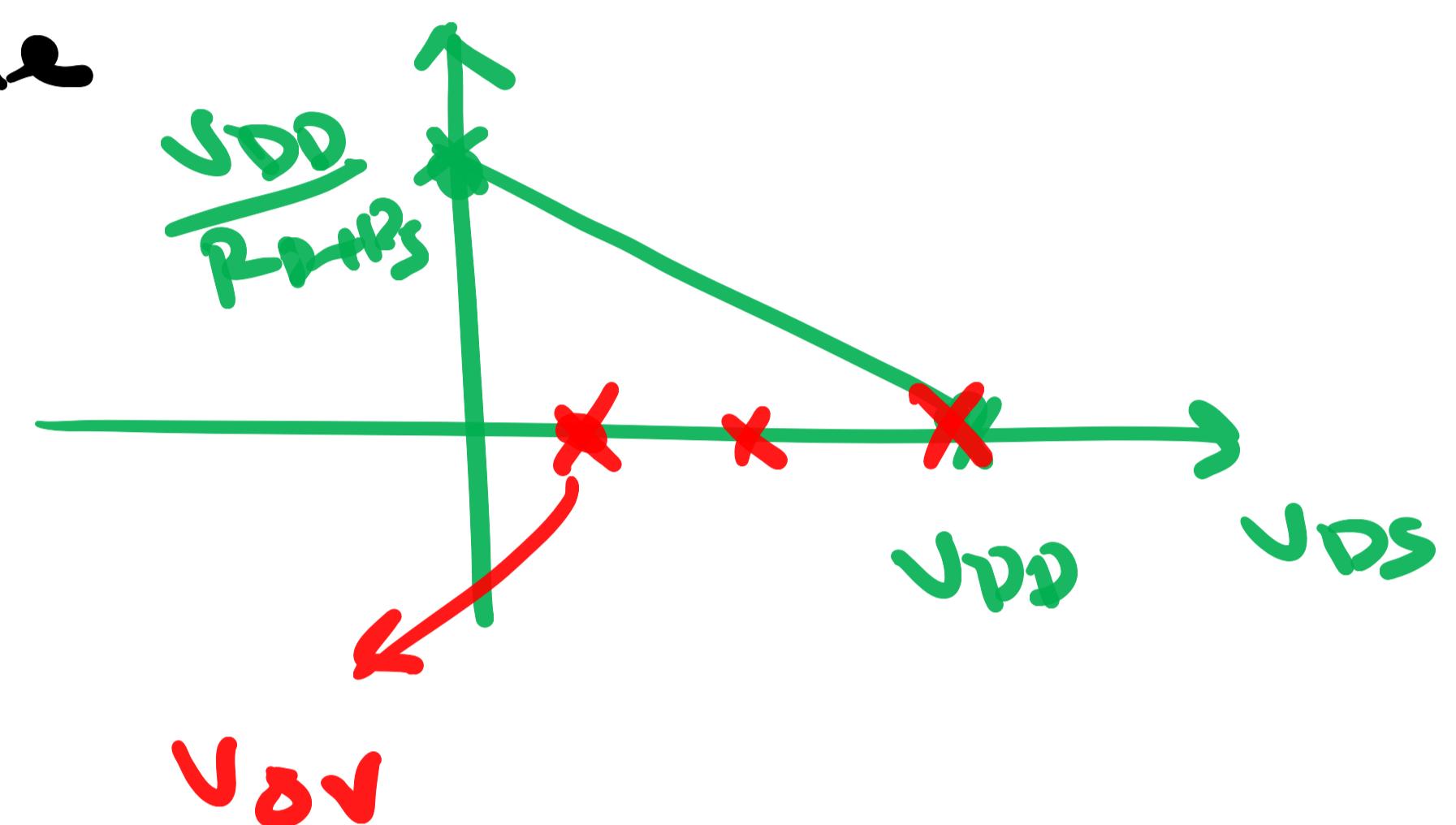
\* choose a  $V_{OV} = 100\text{mV}$

$$\Rightarrow V_{RD} = 250\text{mV}$$



→ choose  $V_{DS}$  using a DC load line

$$V_{DS} = \frac{V_{DD} + V_{OV}}{2} = 950\text{mV}$$



$$\rightarrow V_{RS} = V_{DD} - (V_{RD} + V_{DS}) = 600\text{mV}$$

⇒ Using the power budget  $P_{max} = 5\text{mW}$

$$P_{max} = V_{DD} \cdot I_{max}$$

$$I_{max} = \frac{P_{max}}{V_{DD}} = 2.78\text{mA}$$

$$I_{max} = I_D + I_{R_1}, \quad I_{R_1} = I_{R_2} \text{ since } \Sigma G = 0$$

\* Referring to node X :-

$$V_X = V_{GS} + V_{RS}, \quad V_{GS} = V_{OV} + V_{TH} \\ = 0.1 + 0.5$$

$$V_X = 0.6 + 0.6 = 1.2\text{V}$$

$$V_{RS} = 0.8\text{V}$$

\* We are required to have a  $R_{in}$  of  $50\text{ k}\Omega$

$$R_{in} = R_1 \parallel R_2 = \frac{R_2 R_1}{R_1 + R_2} = 50\text{ k}\Omega$$

$$\Rightarrow R_1 \cdot R_2 \cdot (50\text{ k})^{-1} = R_1 + R_2 \quad \dots \dots \textcircled{1}$$

$\Rightarrow$  define  $V_x$  using voltage division

$$V_x = \frac{R_2}{R_1 + R_2} \cdot V_{DD} \rightarrow \text{replacing } R_1 + R_2 \text{ with its def in eq \# \textcircled{2}}$$

$$V_x = \frac{R_2}{R_1 R_2 (50\text{ k})^{-1}} \cdot V_{DD} \Rightarrow R_1 = 75\text{ k}\Omega$$

$$\Rightarrow \text{but } \frac{R_1 R_2}{R_1 + R_2} = 50\text{ k} \Rightarrow \frac{75\text{ k} \cdot R_2}{75\text{ k} + R_2} = 50\text{ k}$$

$$R_2 \approx 143\text{ k}\Omega$$

$$\Rightarrow I_{R2} = \frac{V_x}{R_2} = 8.3\text{ }\mu\text{A}$$

$$\Rightarrow I_D = I_{max} - I_{R2} = 2.78\text{ mA}$$

$$\Rightarrow R_D = \frac{V_{RD}}{I_D} \approx 90 \Omega$$

$$\Rightarrow R_S = \frac{V_{RS}}{I_D} \approx 126 \Omega$$

$$\Rightarrow \frac{w}{l} = \frac{2 I_D}{\mu_n C_ox V_{ov}^2} = 5542$$

Ex: This stage must satisfy the following :- ( $\lambda=0$ )

①  $|Av| = 4$  ②  $P_{max} = 2mW$  ③  $V_{ov} = 300mV$

④  $R_{out} = 1k\Omega$  ⑤ make sure that the

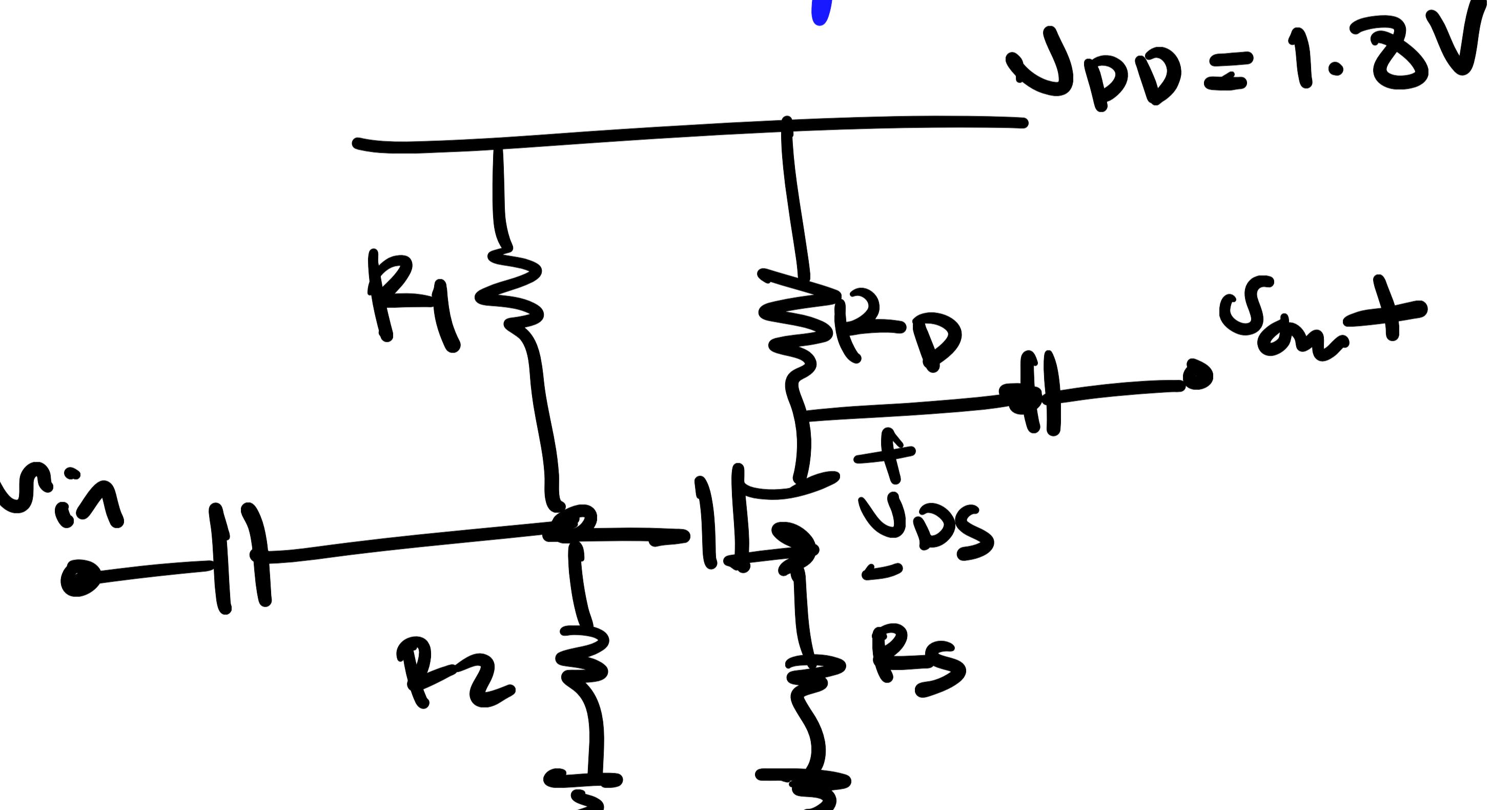
⑥  $V_{TH} = 0.4V$

Sol: ⑦  $R_1$  and  $R_2$  must not consume more than 10% of  $I_{max}$  from the triode region.

$$|Av| = \frac{R_D}{g_m + R_S} = 4$$

$$P_{max} = V_{max} \cdot I_{max}$$

$$\Rightarrow I_{max} = \frac{P_{max}}{V_{DD}} \approx 1.11mA$$



$$\Rightarrow R_{out} = 1k\Omega = R_D \quad (\lambda=0)$$

$$\Rightarrow V_{GS} = V_{ov} + V_{TH} = 0.7V$$

$$\Rightarrow I_{R_1} = 10\% \cdot I_{max} \approx 0.11mA$$

$$\Rightarrow I_D = I_{max} - I_{R_1} \approx 1mA$$

$$\Rightarrow |AV| = \frac{R_D}{g_m + R_S} \Rightarrow g_m = \frac{2I_D}{V_{ov}} = \frac{1}{150\Omega}$$

$$\Rightarrow 4 = \frac{1000}{\frac{1}{150} + R_S} \Rightarrow R_S = 50\Omega ?$$

$$\Rightarrow V_{DS} = V_{DD} - (V_{RD} + V_{RS}) \\ = V_{DD} - I_D (R_D + R_S) = 0.75V$$

we satisfied the requirement for being at least 100mV from V<sub>ov</sub>

$\Rightarrow$  to find  $R_1$  and  $R_2$  let us define  $V_x$

$$V_x = V_{GS} + V_{RS} = 0.7 + I_D R_S = 0.75V$$

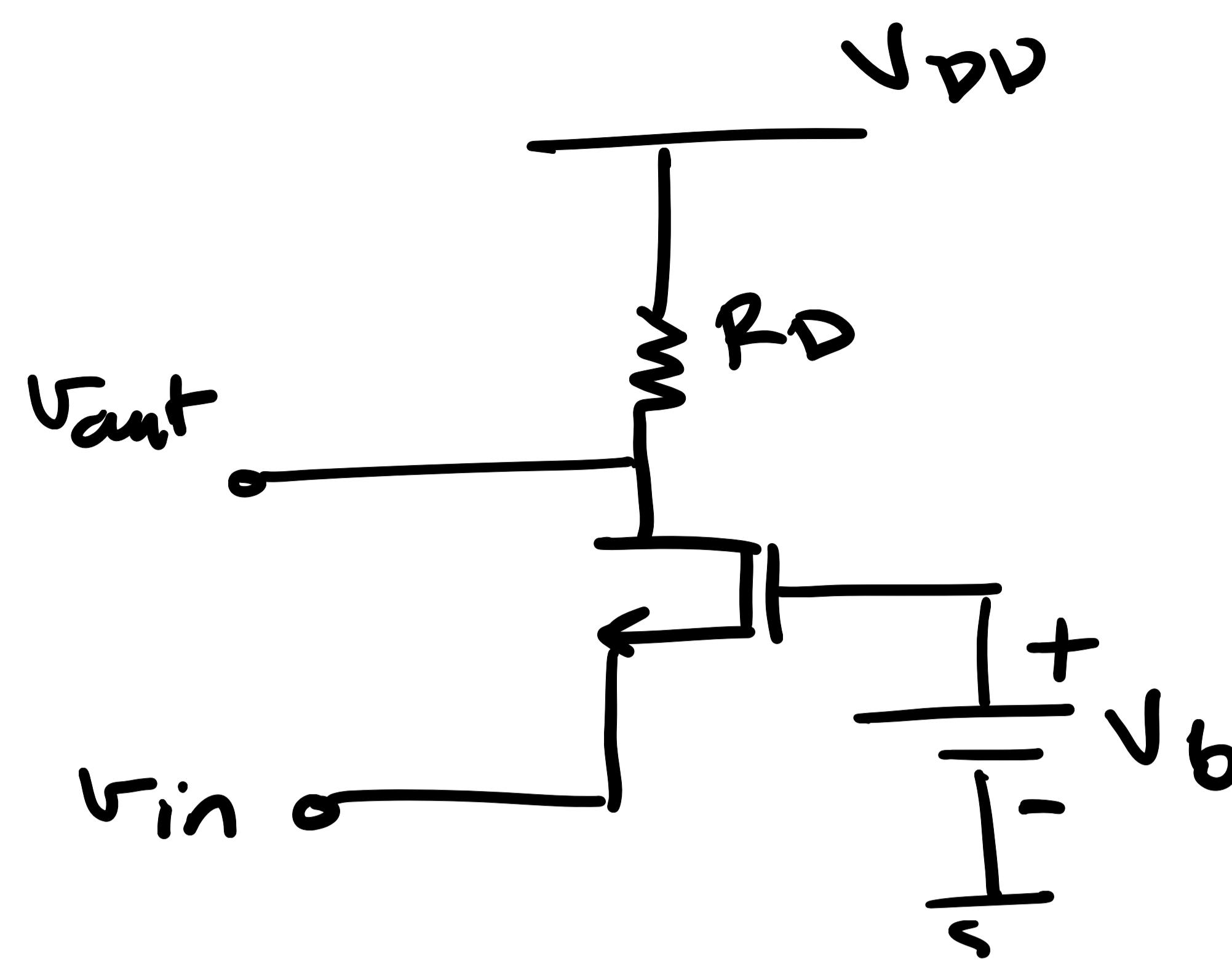
$$\Rightarrow R_2 = \frac{V_x}{I_{R_1}} = 6.75k\Omega$$

$$R_1 = \frac{V_{PD} - V_x}{I_{R_1}} = 9.45k\Omega$$

$$\Rightarrow \frac{w}{l} = \frac{2I_D}{\mu n C_o x V_{ov}^2} \approx \frac{2000}{9}$$

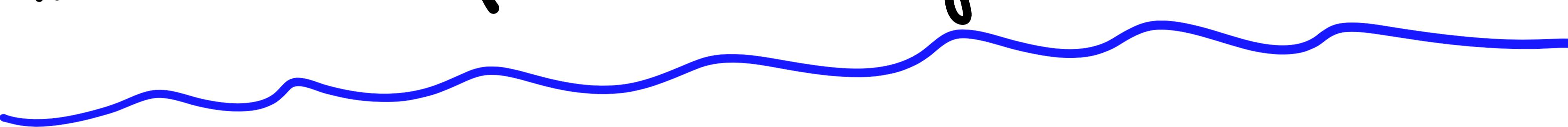
## \* Common Gate stage :- ( CG stage )

\* This topology is favored when working with RF applications due to its low input impedance.



\* a positive voltage gain.

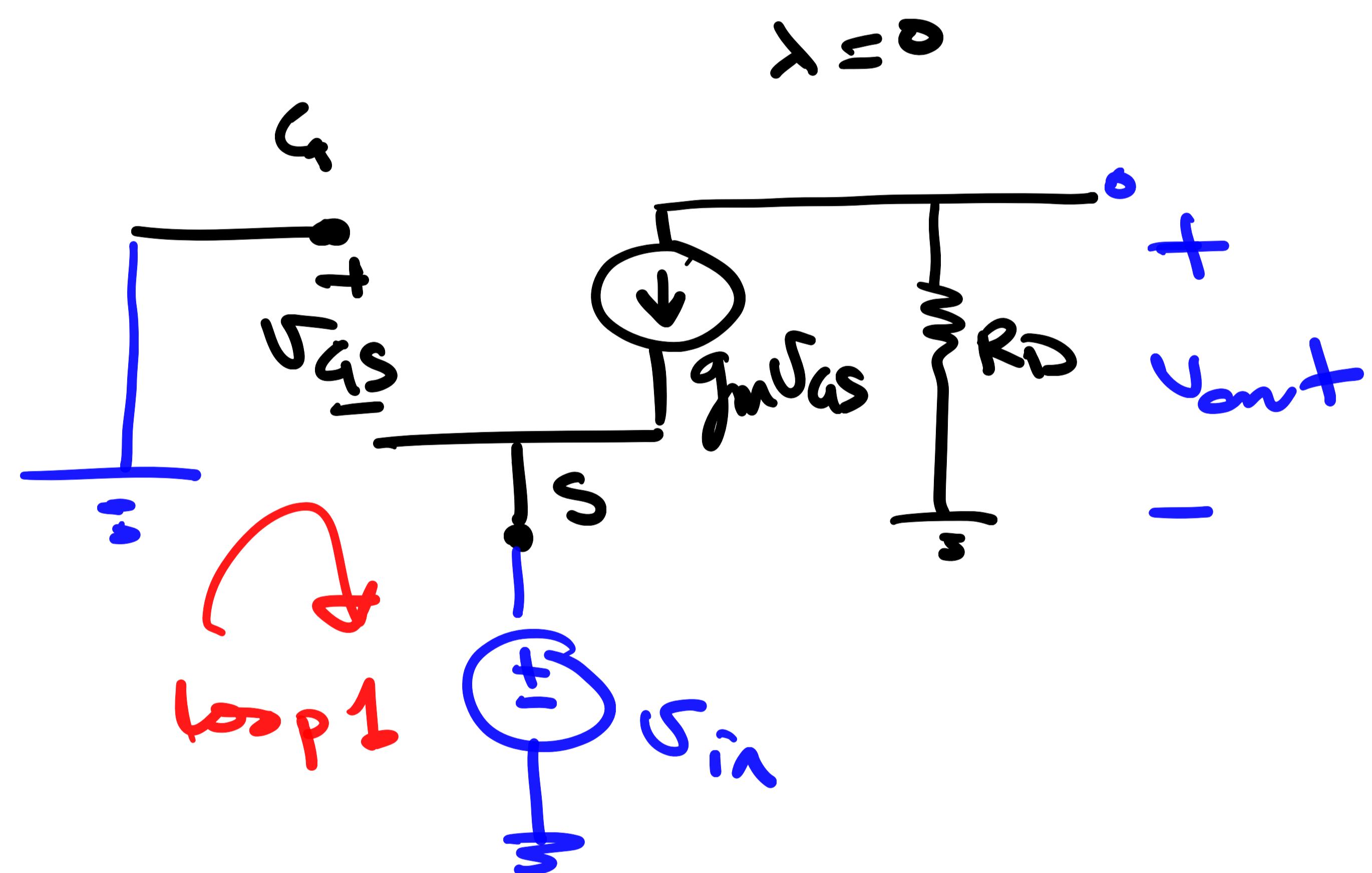
\* a unity current gain.



\* AV analysis:

$$AV = \frac{V_{out}}{V_{in}}$$

$$V_{out} = -g_m V_{GS} \cdot R_D$$



applying KVL @ Loop 1 :-

$$+V_{AS} + V_{IN} = 0 \Rightarrow V_{IN} = -V_{AS}$$

$$V_{AS} = -V_{IN}$$

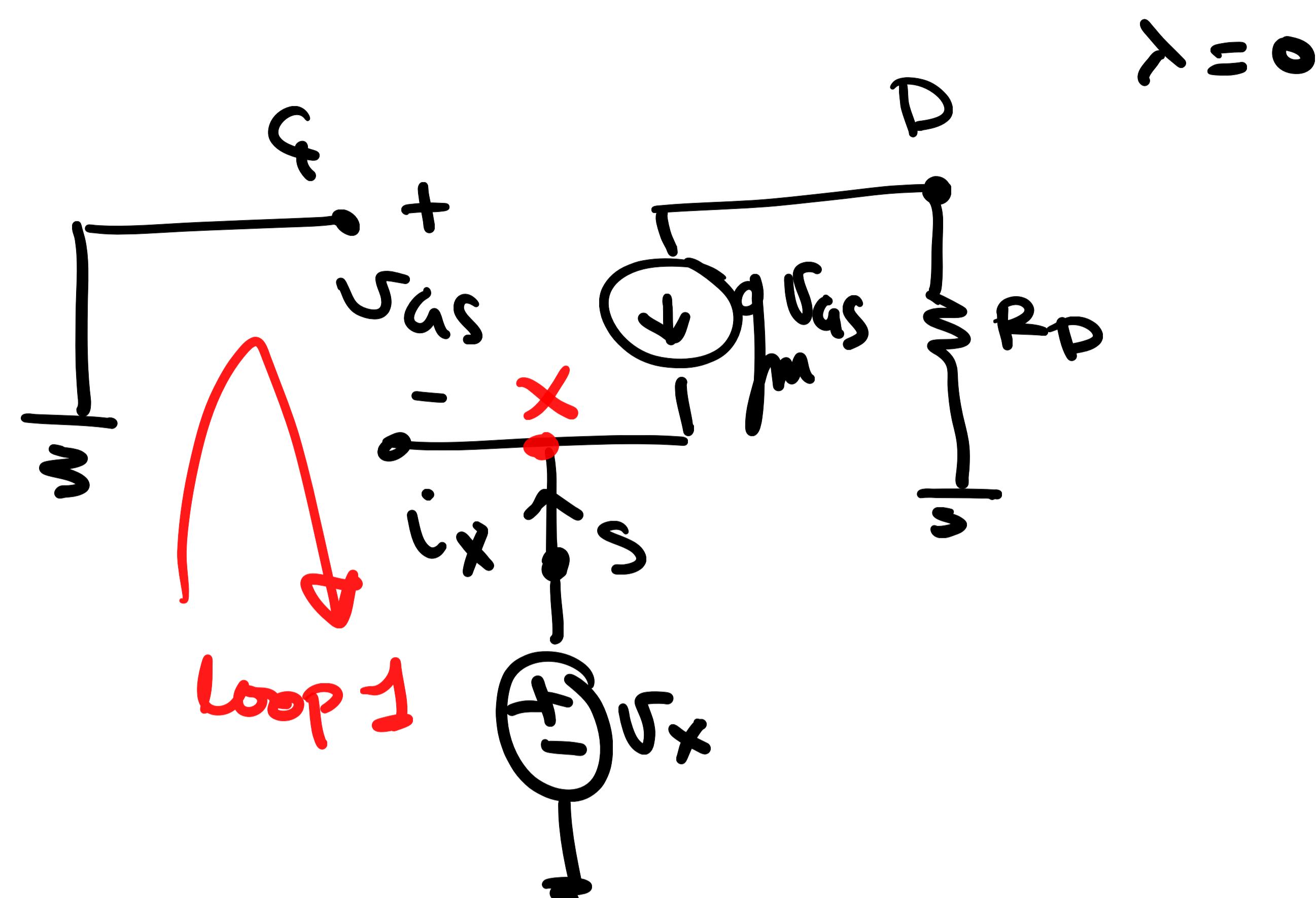
$$V_{out} = g_m \cdot V_{IN} \cdot R_D \Rightarrow \frac{V_{out}}{V_{IN}} = \boxed{AV = g_m R_D}$$

\* Input Impedance Analysis :-

$$R_{in} = \frac{V_x}{i_x}$$

applying KCL @ node X

$$i_x = -g_m V_{GS}$$



applying KVL @ loop 1

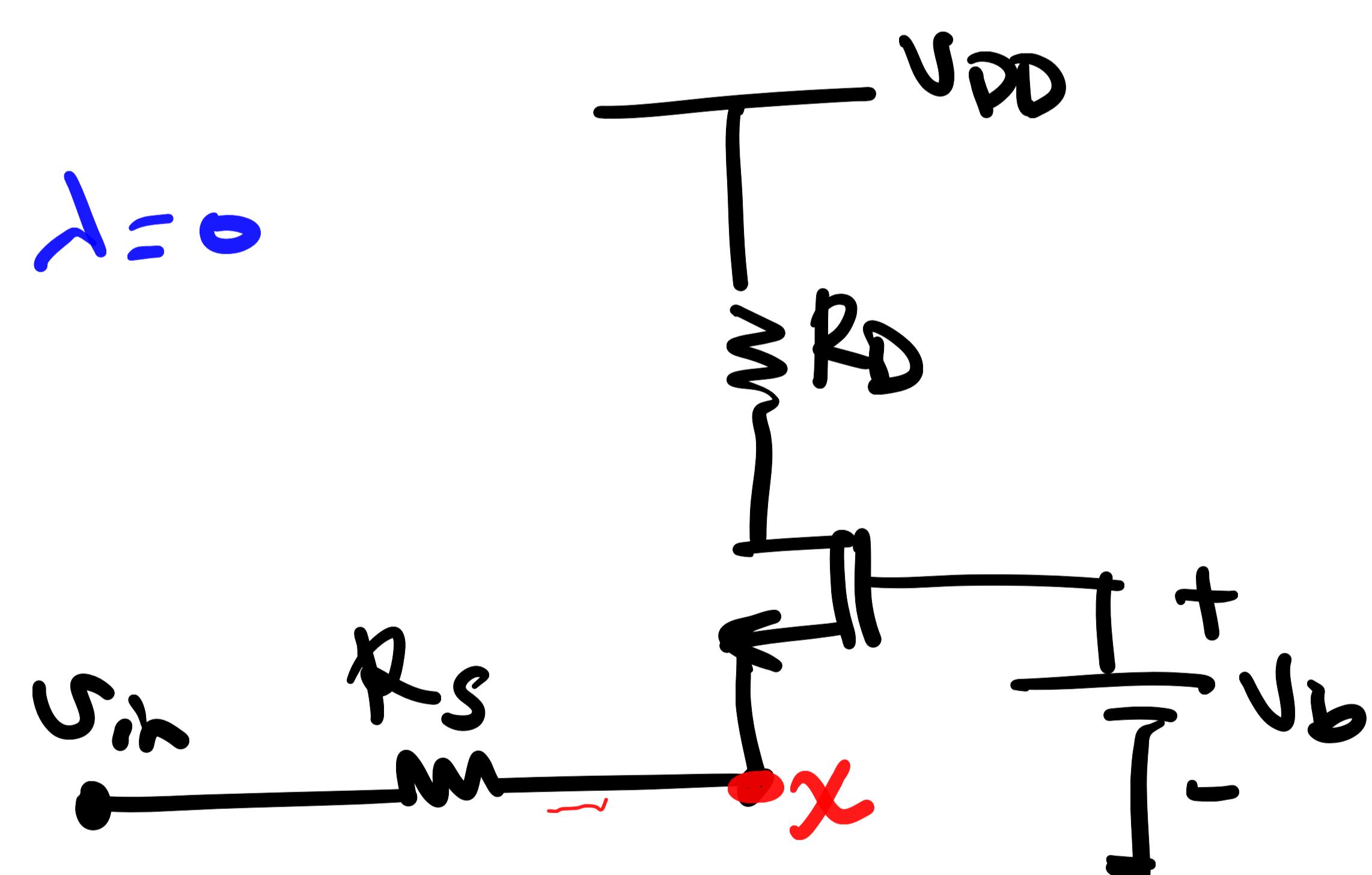
$$V_{GS} = -V_x \Rightarrow i_x = g_m V_x \Rightarrow \frac{V_x}{i_x} = Y_{gm}$$

$R_{in} = Y_{gm}$

\* Analyzing the effect of source resistance on CG:

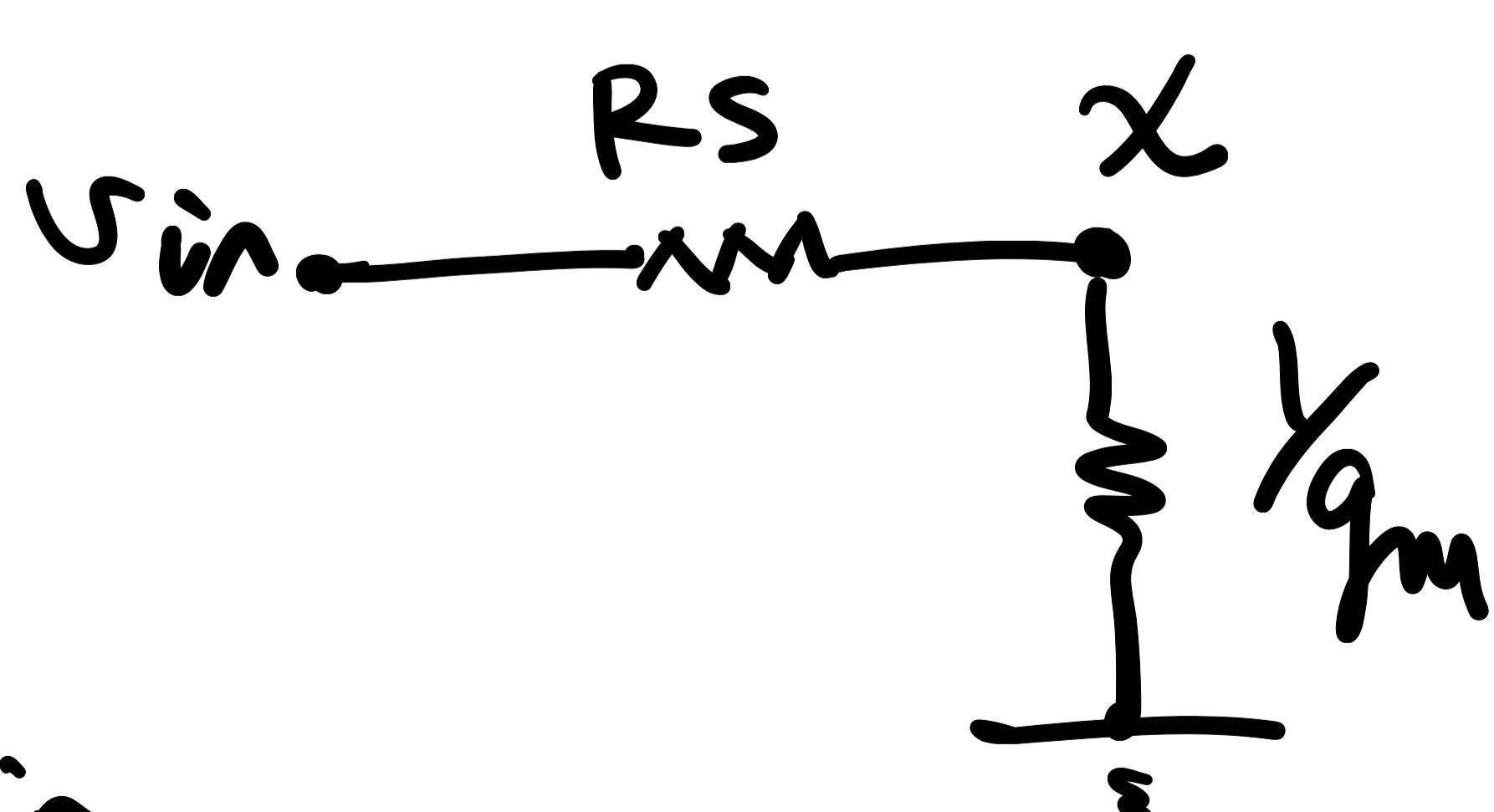
\* Gain Analysis Av :  $\lambda=0$

this cct.



can be simplified

as follows



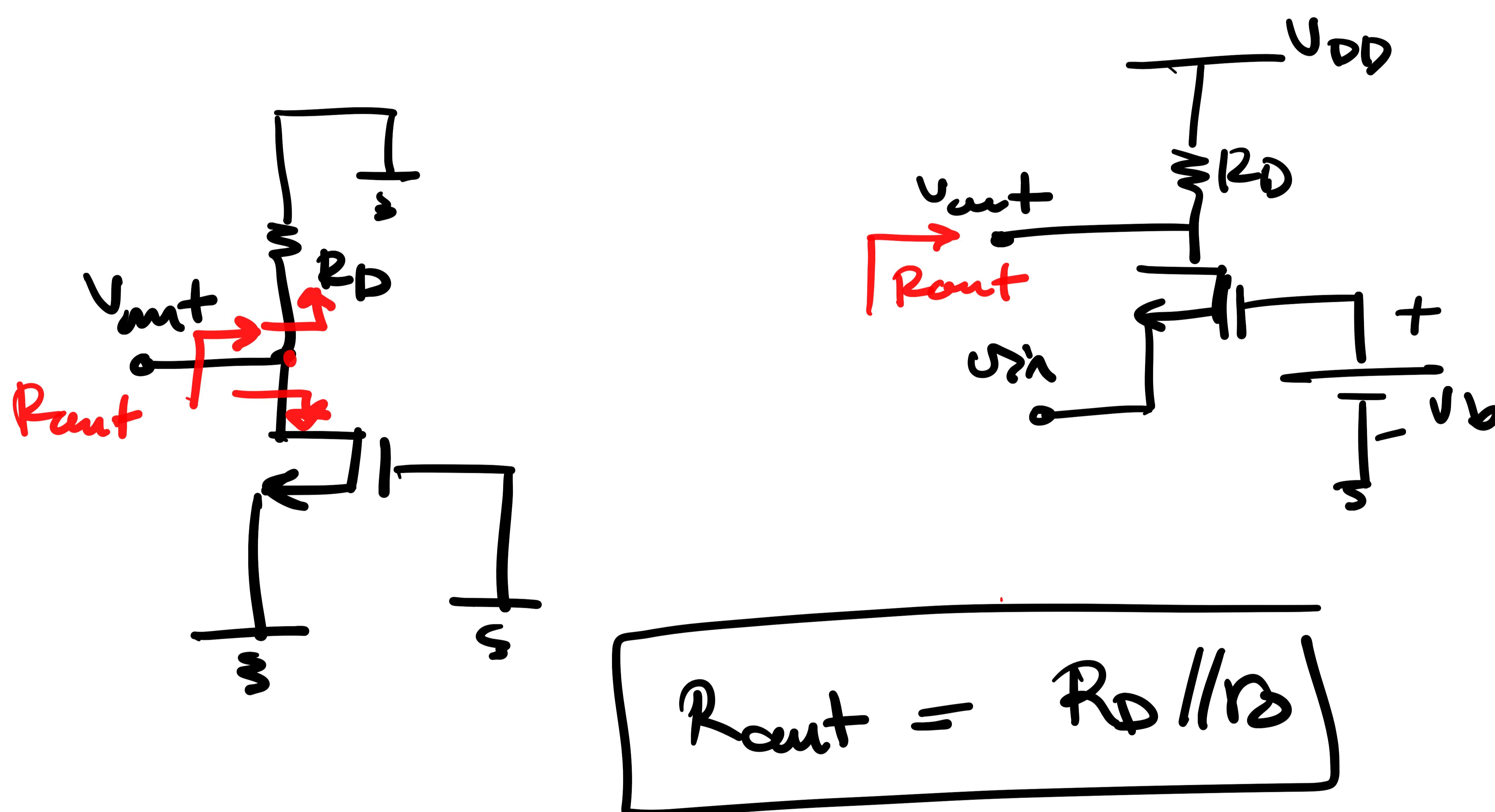
$$V_x = \frac{Y_{gm}}{\frac{1}{Y_{gm}} + R_S} \cdot V_{in}$$

$$\Rightarrow Av = \frac{V_{out}}{V_{in}} = \left( \frac{V_{out}}{V_X} \right) \cdot \frac{V_X}{V_{in}}$$

but  $\frac{V_{out}}{V_X} = g_m R_D \Rightarrow Av = \frac{g_m}{g_m + R_s} \cdot g_m \cdot R_D$

$$Av = \frac{R_D}{g_m + R_s}$$

\* Output Impedance Analysis for CG  $\neq 0$ :



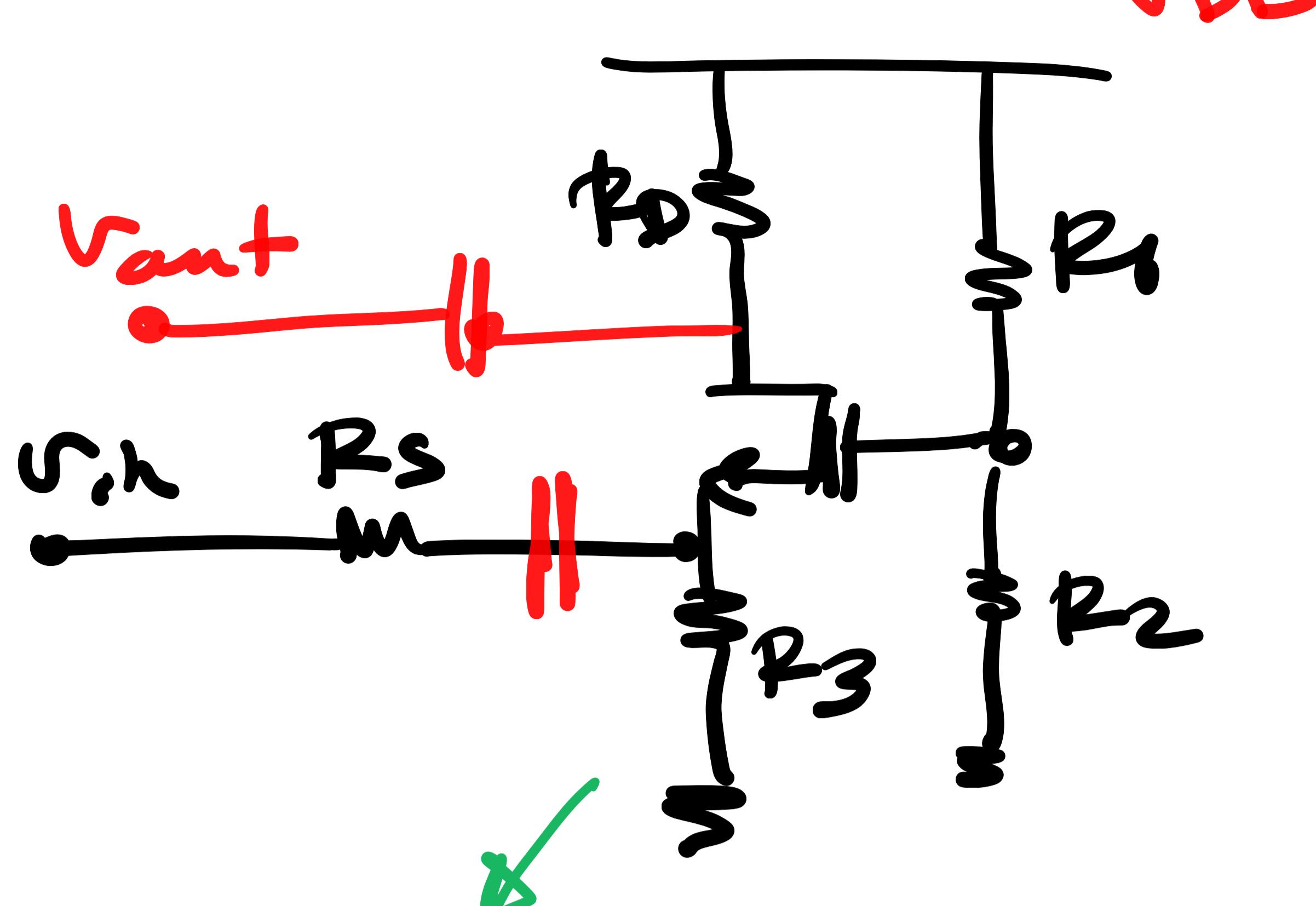
\*  $A_i \Rightarrow$  current gain  $A_i = 1$  because

$$A_i = \frac{i_{out}}{i_{in}} \Rightarrow i_{out} = i_{in}$$

\* CG stage with biasing

\* Gain Analysis

$$AV = \frac{R_3 || \frac{1}{g_m}}{R_3 || \frac{1}{g_m} + R_S} \cdot g_m R_D$$



for small signal analysis:

$R_1 || R_2 = R_G$   
we can neglect  $i_B$  effect  
at low freq.

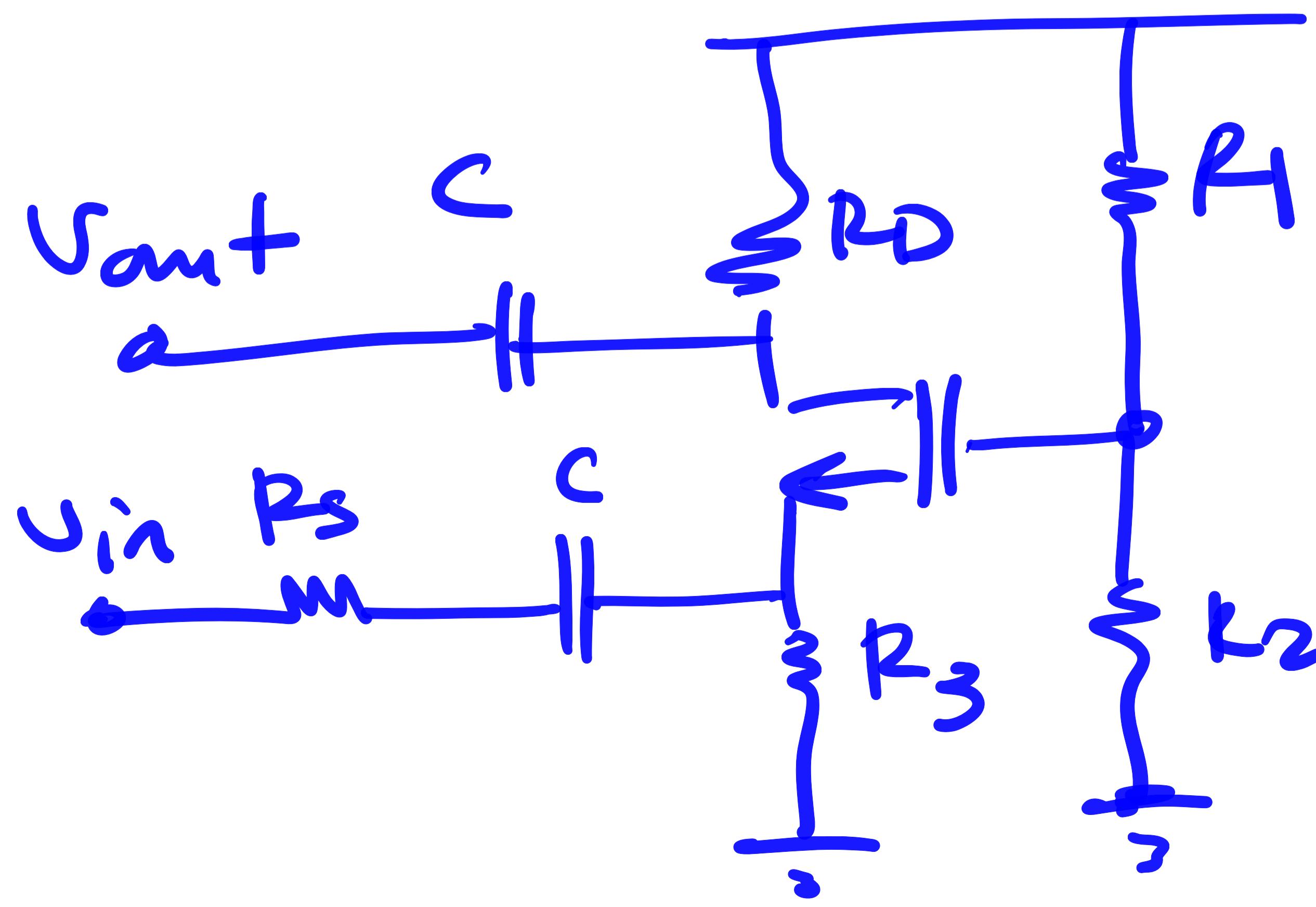
Ex: Design a CG stage with voltage divider biasing to satisfy the following :

1]  $A_v = 5$ ,  $R_S = 0$  3]  $R_{in} = 50\Omega$

4]  $P_{max} = 2mW$ ,  $\mu_n C_{ox} = 100\mu A/V^2$

$V_{TH} = 500mV$ ,  $\lambda = 0$

1.8V



Sol: Given :  $R_{in} = 50 \Omega$

$$\Rightarrow R_{in} \text{ for a CG} = \frac{1}{g_m} = 50 \Omega$$

$$g_m = \frac{1}{50 \Omega}$$

by assuming that  $R_3 > 10 \frac{1}{g_m}$

we grant a path for the small signal through the transistor.

$$\Rightarrow R_3 = 500 \Omega$$

$$\Rightarrow A_v = g_m R_D \Rightarrow R_D = \frac{A_v}{g_m} = 250 \Omega$$

