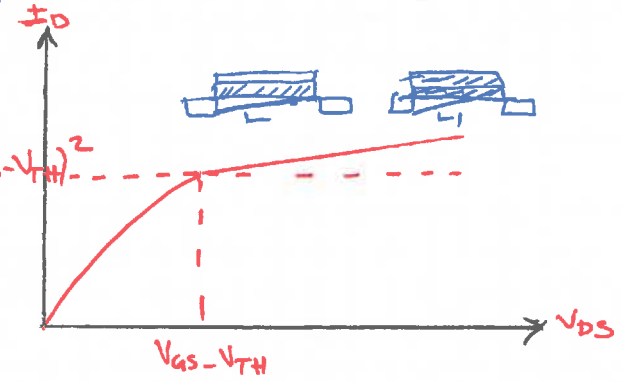
* Channel Length Modulation :-

* We have learned that as V_{DS} increases the "channel Pinches off" at shorter lengths.

* This will shorten the Length of the channel from $L \rightarrow L_1$, $L_1 < L$ since $I_D \propto \frac{1}{L}$ → then we expect the current to increase for shorter L's.



* The variation of L_1 due to changes in V_{DS} is called "channel-modulation"

* To account for channel length modulation, we assume L is constant, but incorporate a term $(1+\lambda V_{DS})$

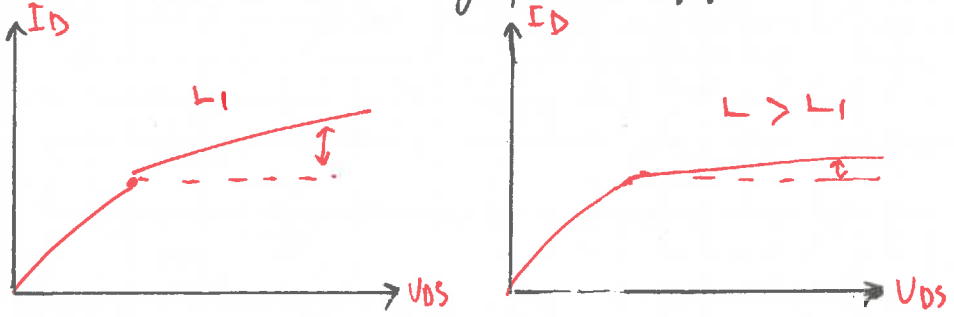
$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

λ: Is the "channel-modulation-coefficient." $\lambda \propto \frac{1}{L}$

* The channel modulation effect can be controlled by the cct. Designer, since the cct. designer can control "L"

* Longer L will reduce the effect of V_{DS} on L

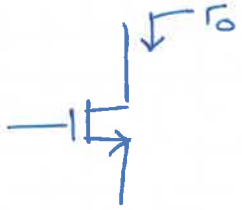
* Shorter L will have a more significant effect.



Ex: A MOSFET carries a Drain current of 1mA with $V_{DS} = 0.5V$. in saturation. Determine the change in I_D if V_{DS} rises to 1V and $\lambda = 0.1V^{-1}$. What is the device output impedance?

Sol: The output resistance of the MOS Device

$$\frac{\Delta V_{DS}}{\Delta I_D} = \frac{v_x}{i_x}$$ ← small signal analysis.



$\rightarrow \quad \Delta I_D = I_{D2} - I_{D1}$

$\rightarrow \quad I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS_1}) =$

$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS_2})$

$$\frac{I_{D2}}{I_{D1}} = \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS2}} \rightarrow I_{D2} = I_{D1}\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS_1}} = 1.048mA$$

$\rightarrow \quad \Delta V_{DS} = V_{DS2} - V_{DS1}$, $\Delta I_D = I_{D2} - I_{D1}$, $\boxed{r_o = 10.42\,k\Omega}$

* Ideally, if the channel modulation is not included (no effect) the a ΔV_{DS} should result in $\Delta I_D = 0$ (independency from V_{DS} changes)

$$r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \infty \rightarrow \text{the}$$

* MOS Transconductance :- 'gm'

* The g_m is Defined at the saturation region where the MOS device acts as a voltage-controlled current source :-

$$g_m = \frac{\partial I_D}{\partial V_{GS}} .$$

In the "sat" region $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$ ---- (1)

$$\rightarrow \boxed{g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})} \quad \text{----- (2)}$$

* higher "g_m" corresponds to a greater change in the Drain current for small changes in V_{GS}.

substituting $(V_{GS}-V_{TH})$ with $\sqrt{\frac{2I_D}{\mu_n C_{ox}}\frac{L}{W}}$

$$\rightarrow \boxed{g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}} \quad \text{---- (3)}$$

* Dividing 2 ÷ 1 $\rightarrow$ $\boxed{g_m = \frac{2I_D}{V_{GS}-V_{TH}}}$ --- (4)

$g_m \propto I_D$ for a given $(V_{GS}-V_{TH})$

$g_m \propto \frac{1}{V_{GS}-V_{TH}}$ for a given I_D

* eq. 3 is more commonly used, since I_D can be specified by the power dissipation requirements.

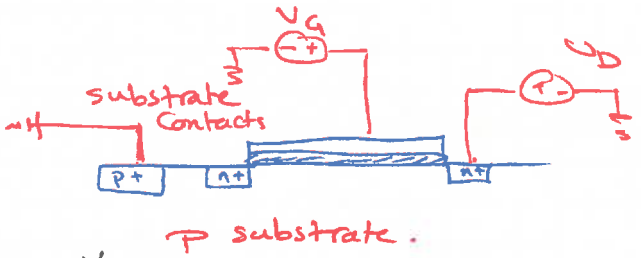
* The g_m for MOS can be controlled by $\frac{W}{L}$ which is something a designer has control over unlike BJTs $g_m = \frac{I_C}{V_T}$

* Second Order Effects :-

1] Body Effects

2] Subthreshold Conduction.

* ① Body Effects :-



* When the sours voltage V_s rises above the substrate (body) voltage

* The voltage difference between the source and the substrate (bulk) = V_{SB} → Source_bulk.

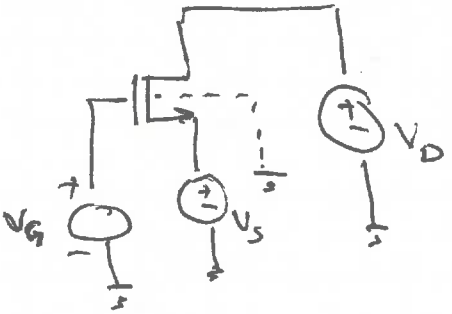
* When $V_{SB} > 0$ then $V_{TH} \uparrow$

$$V_{TH} = V_{THO} + \gamma \left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right)$$

* V_{THO} → V_{TH} when $V_{SB} = 0$

* γ 0.4 $\sqrt{V}$
  ϕ_F 0.4 V
  } technology dependent.

Ex :- In this ccf. $V_S = 0.5V$, $V_G = V_D = 1.4V$, $\mu_n C_{ox} = 100 \mu A/V^2$, $\frac{W}{L} = 50$, $V_{THO} = 0.6V$. Determine the Drain current if $\lambda = 0$.



Sol° Since $V_{SB} = 0.5$

then $V_{TH} = 0.698V$

assuming typical values for γ, ϕ_F

→ If $V_{DS} > V_{GS} - V_{TH}$

→ $V_{GS} = 1.4 - 0.5 = 0.9V$ → $V_{TH} = 0.698V$

* $V_{DS} = V_D - V_S = 0.9V$

→ $V_{DS} > 0.9 - 0.698$ ✓ then the device is in the saturation region.

→ $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 = \boxed{102\,\mu A}$

[2] Subthreshold conduction :-

Ideally, we have assumed that the MOS turns on when V_{GS} reaches V_{TH}. → $V_{GS} \geq V_{TH}$, $I_D > 0$

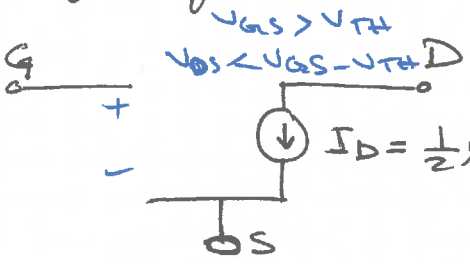
In reality if $V_{GS} < V_{TH}$, $I_D \neq 0$

there is a small current called the "Subthreshold Conduction" current.

* MOS Device Models :-

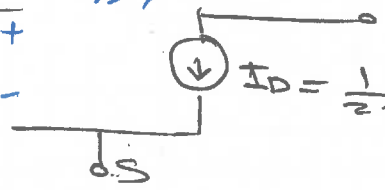
1] large signal Model :

a] $V_{GS} > V_{TH}$, $V_{DS} < V_{GS} - V_{TH}$ — Triode Region



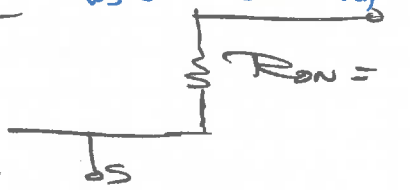
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{GS}-V_{TH})V_{DS} + V_{DS}^2\right]$$

b] $V_{GS} > V_{TH}$, $V_{DS} > V_{GS} - V_{TH}$ — saturation region



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

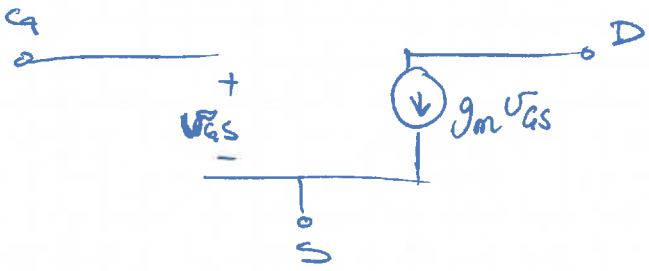
c] $V_{GS} > V_{TH}$, $V_{DS} << 2(V_{GS}-V_{TH})$ — Deep triode region



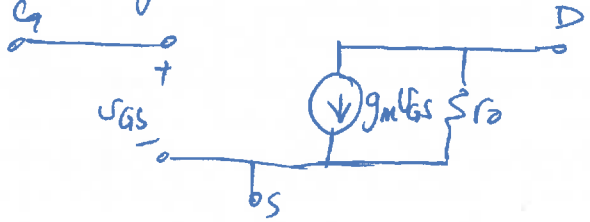
$$R_{ON} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}$$

2] Small Signal Model :-

* $i_D = g_m v_{GS}$



* Including the Output resistance effects



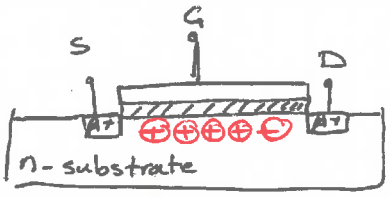
, $r_o \approx \frac{1}{\lambda I_D}$

Ex: A MOSFET Biased at a drain current = 0.5 mA. If $\mu_n C_{ox} = 100\ \mu A/V^2$, $\frac{W}{L} = 10$ and $\lambda = 0.1\ V^{-1}$ find the small signall parameters.

Sol: $r_o = \frac{1}{\lambda I_D} = 20\ k\Omega$.

$$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D} = \frac{1}{1\ k\Omega}$$

PMOS Transistor :-



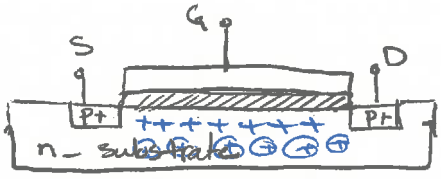
* The channel is formed through the accumulation of positive charge under the bottom of the oxide material.

* To atract the positive charge we need to apply a negative potential at the gate ("G"). Initially this will repel the electrons in the substrate towards the bottom exposing positive ions.

after V_{GS} (negative) ~~exceeds~~ becomes more negative than V_{TH}

$V_{GS} < V_{TH}$, positive charge will start accumulating at the bottom of the oxide surface bottom.

$\therefore V_{TH}$ is a negative value



* V_{GS} is a negative value → V_{SG} a positive value.

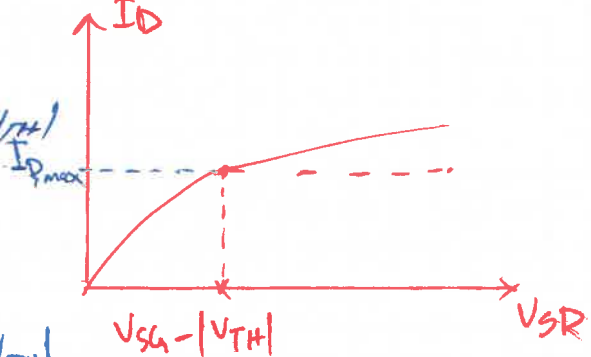
~~* Deep triode region~~ is

$V_{SD} << 2(V_{SG} - |V_{TH}|)$, $V_{SG} > |V_{TH}|$

~~$V_{SD} = V_{GS} - |V_{TH}|$ edge~~

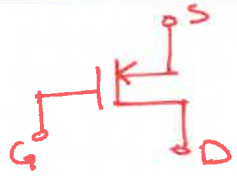
→ Triode region

$V_{SG} > |V_{TH}|$ and $V_{SD} < V_{SG} - |V_{TH}|$



* Saturation is reached when

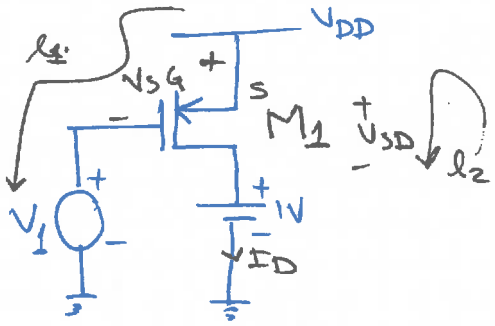
$$V_{SD} > V_{SG} - |V_{TH}|$$



* $I_{D,triode} = \frac{1}{2}\mu_h C_{ox}\frac{W}{L}\left(2(V_{SG}-|V_{TH}|).V_{SD} - V_{SD}^2\right)$

* $I_{D,sat} = \frac{1}{2}\mu_h C_{ox}\frac{W}{L}\left(V_{SG}-|V_{TH}|\right)^2$

Ex: In this cct. determine the region of operation of M_1 as V_1 ~~goes~~ changes from V_{DD} to zero, assume $V_{DD} = 2.5\,V$ and $|V_{TH}| = 0.5\,V$.



Sol:- When $V_1 = V_{DD}$

→ applying KVL at loop 1 :-

$-V_{DD} + V_{SG} + V_1 = 0$

→ $V_{SG} = 0$, since $V_1 = V_{DD}$

if $V_{SG} = 0 \overset{X}{>} |V_{TH}|$ then the device is not "ON"

→ If $V_1 = 0$ → then $V_{SG} = 2.5\,V > |V_{TH}|$ → M_1 is ON

→ V_{SD} ⇒ apply KVL at loop 2 → $-V_{DD} + V_{SD} + 1 = 0$

→ $V_{SD} = V_{DD} - 1 = 1.5\,V$ → $V_{SD} \overset{?}{<>} V_{SG} - |V_{TH}|$

$1.5\,V \overset{?}{<>} 2.5 - 0.5$

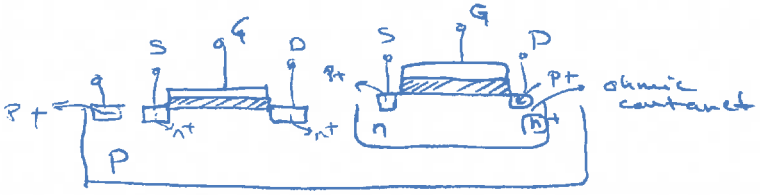
→ $V_{SD} < V_{SG} - |V_{TH}|$

then we are in triode region.

* The small signal Model for PMOS is similar to the NMOS, exactly like BJTs PNP and NPN analogy.

* CMOS technology :- "Complementary MOS" "CMOS"

* It is a technology that builds both NMOS and PMOS on the same wafer:



* The advantages of CMOS technology have dominated led to the CMOS domination on the market when compared to NMOS and PMOS technology. (Used in microprocessors, RAMS, sensors). could also be used for amplification purposes.