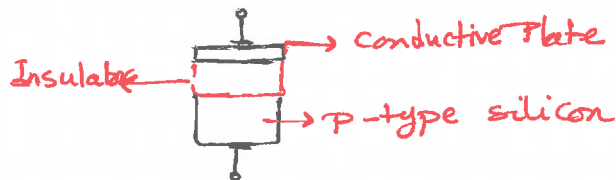


* Physics of MOS Transistors :- Metal Oxide Semiconductor

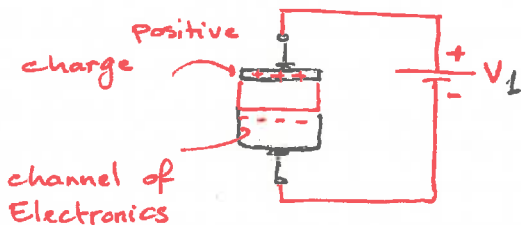
* The micro-electronics field is dominated by a type of device called the Metal Oxide Semiconductor.

* The MOS devices offer unique properties that led to the revolution of the semiconductor industry.

+ Structure of MOSFET :-



* Since the p-type is somewhat conductive. This structure acts as a capacitor.



* The positive charge on the metal plate will attract the minority carriers in the p-material (electrons) type silicon.

* This creates a channel of free electrons at the interface between the insulator and the piece of silicon.

* If the electron density is sufficiently high this will serve as a good conductive path.

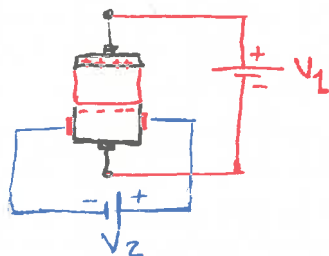
* Since this structure models a capacitor, then the density of electrons will be controlled by V_1 .

$Q = CV_1$, Q is the charge density, C the capacitance

* V_1 controls the conductivity of the channel (also the resistivity) which controls the current flow. "Voltage Controlled Current Source"

* To ~~maximize~~ ^{strongly} the control of Q by V , C must be maximized.

$$Q = CV \rightarrow \frac{dQ}{dV} = C \leftarrow \text{maximizing } C$$

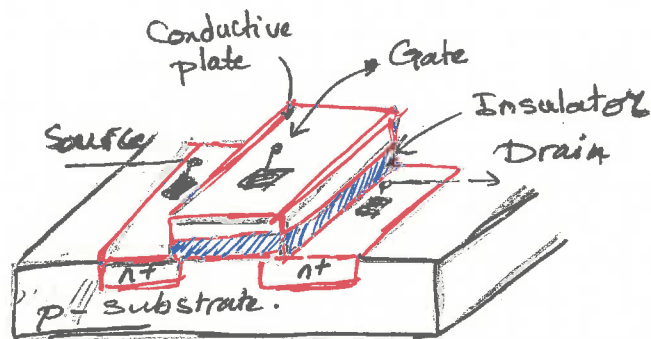


* "Current flow control."

* The capacitance can be increased by reducing the distance between the two plates.

* Current technologies can produce a 20 \AA .

* Note: $1 \text{ \AA} = 0.1 \text{ nmeter} = 10^{-10} \text{ meter}$



* Gate is deposited on top of an insulator material.

* The insulator material is deposited on the ~~top~~ underlying p-type silicon substrate.

* To allow current flow through the silicon material, two contacts are attached to the substrate through two heavily-doped n-type regions.

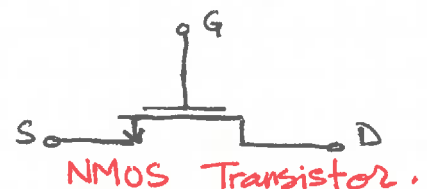
* Direct contact of metal to the substrate would not produce a good "Ohmic" contact.

* "Ohmic" contact is used to distinguish contacts that allow a bidirectional flow of current instead of uni-directional flow such as Diodes.

* **"MOS Transistor Symbol"**

* Since the current flow is generated by electrons flow

the above structure is called "NMOS".

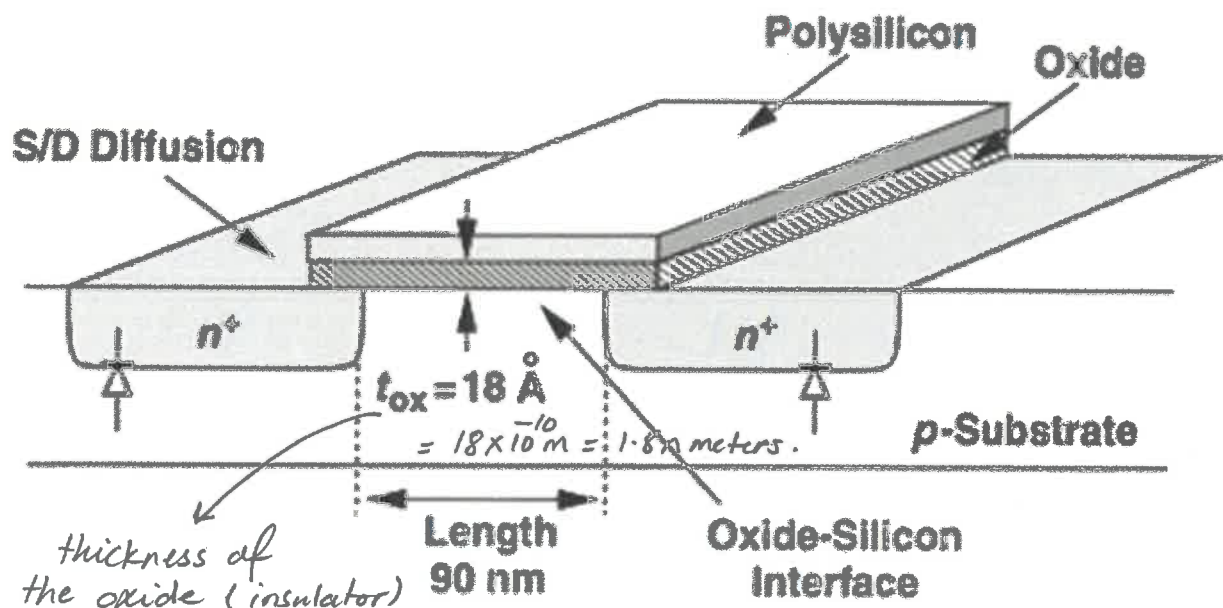


* **Types of material used in the device:-**

① The Gate Material: The material should be chosen as a good conductor. Initially, aluminum was chosen, then, noncrystalline silicon with heavy doping exhibits better fabrication and physical properties - (poly silicon gates)

② The Dielectric material: Silicon dioxide.

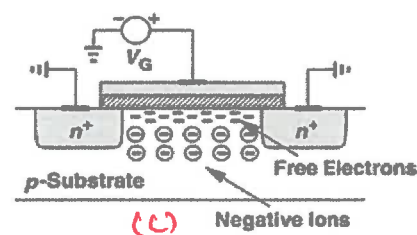
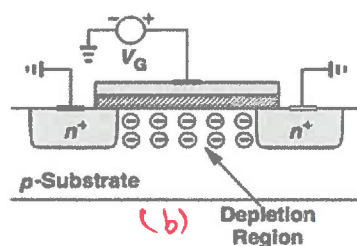
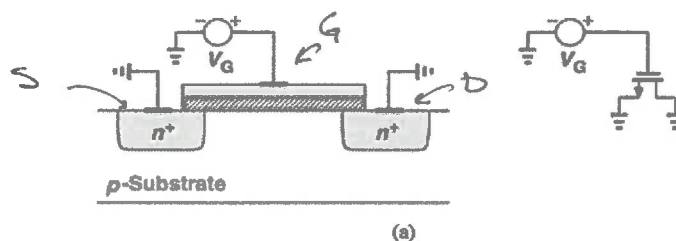
③ The Gate/Drain material: n^+ (heavily doped silicon)
the n^+ region is called the "diffusive region"



thickness of the oxide (insulator)

- * The diffusion regions form diodes with the p-substrate.
- * for proper operation of the transistors, the pn junctions need to remain reverse-biased.
- * Only the depletion region capacitance associated with the two diodes will be taken into consideration.

* OPERATION OF MOSFET:-



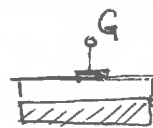
* Referring to the previous figure, the following can be observed :-

- 1] connecting both the source and the drain to ground and the gate to a positive voltage source V_G (see fig. (a))
- 2] Increasing V_G will accumulate positive charge on the gate. (G), this will repel the holes. When the holes are repelled to the bottom of the p-substrate, their hosting atoms will become more negatively charged, and will become negative ions (Ions are immobile). (see fig. b).
- 3] The -ve ions in the bottom of the insulator material will form a depletion region.
- 4] Due to the absence of free charge between the S and D, the MOSFET is OFF.
- 5] Increasing V_G further will attract the minority carriers in the p-substrate to the bottom of the insulator material and will rise above the negative ions. The V_G that causes the minority carriers to rise above the ions is called the "Threshold voltage" (V_{TH}). V_{TH} ranges from 300mV - 500mV

Note: The pn junctions between the n^+ and the p substrate are maintained in a reverse-biased mode. This is insured by connecting the p-substrate to the most negative ~~point~~ point in the cct.

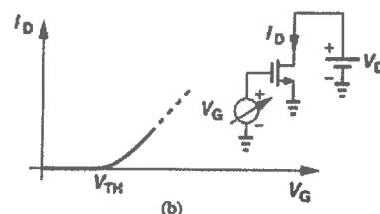
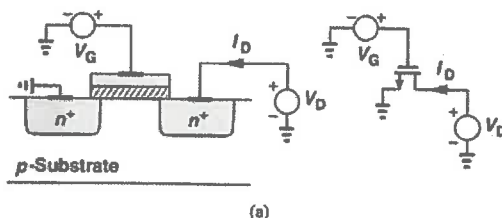
* MOSFET as a Variable Resistor :-

* Since V_G controls the density of electrons in the channel, the S and D path can be viewed as a variable resistor.

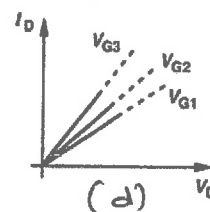
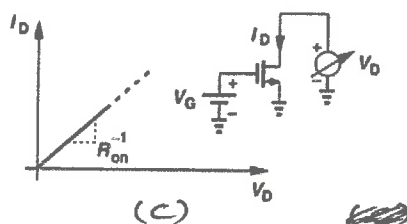


* MOSFET OPERATION :-

- ① * If the S and D are connected to ground and only V_G is applied there will be no current flow.



- ② If $V_D > 0$ and $V_G < V_{TH}$ then the transistor will be OFF and the drain current $I_D (= \text{Source current}) = 0$



- ③ As soon as $V_G > V_{TH}$ and $V_D > 0$ the Device will start conducting and $I_D > 0$.

* The source S and D path will act as a simple resistor

* I-V MOSFET Characteristics :-

- ① I_D vs. V_G → when $V_G > V_{TH} \rightarrow I_D > 0$

- ② I_D vs. V_D → For a fixed $V_G > V_{TH}$, $V_D \uparrow \rightarrow I_D \uparrow$

* the slope of the line in figure (c) = $1/R_{on}$

* R_{on} is the "on-resistance" : The resistance value of the S-D path at a fixed $V_G > V_{TH}$

* The I_D vs. V_D Lines slope is controlled by V_G
Increasing $V_G \uparrow \rightarrow R_{on} \downarrow \rightarrow I_D \uparrow$ for a fixed V_D

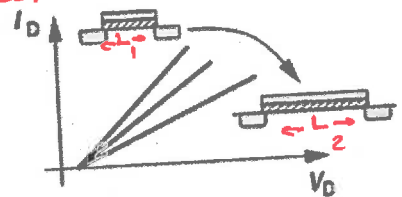
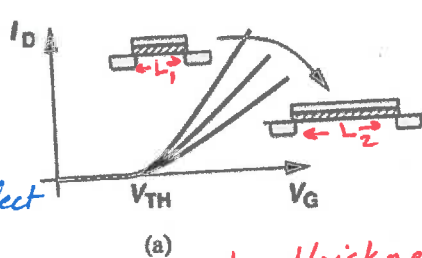
* The Type of current that flows in a MOSFET (I_D) :-

Since both the Source-Substrate and Drain-Substrate are reversed biased pn junctions, and the Drain voltage source is creating an electric-field along the channel, then the I_D current is a "Drift" current.

* The Effect of the MOSFET Physical dimensions on the I-V characteristics :-

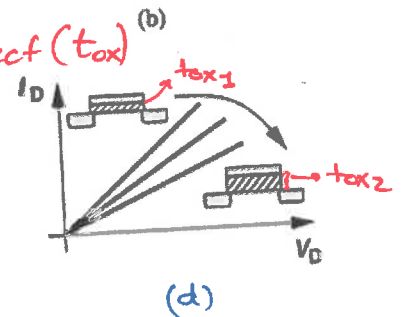
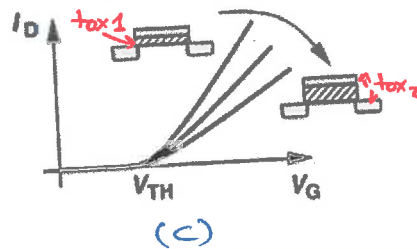
① The channel width Effect (L)

* channel width effect (L)



② The oxide thickness effect (t_{ox})

* oxide thickness effect (t_{ox})



③ The width of the transistor W .

* ① The channel Length Effect (L) :-

* The S-D path is called the channel and is treated as a simple Resistor.

* Recall from physics that the Resistance $R = \rho \frac{L}{A}$, ρ is the resistivity of the material, therefore increasing (L) will increase R_{on} .

* The effect of increasing L can be observed by noticing that the slope of the I_D - V_G lines drop as $L \uparrow$. (see fig(a))

* Similar observations can be noticed on the I_D - V_D characteristics.

* Therefore, it is desirable to minimize the channel length. to achieve larger drain currents.

* Note: The V_{TH} changes with the Length $\boxed{L \downarrow, V_{TH} \downarrow}$ that is at short lengths.

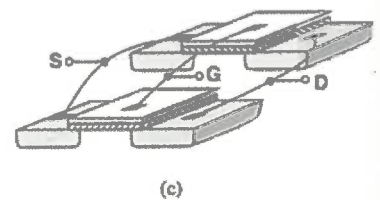
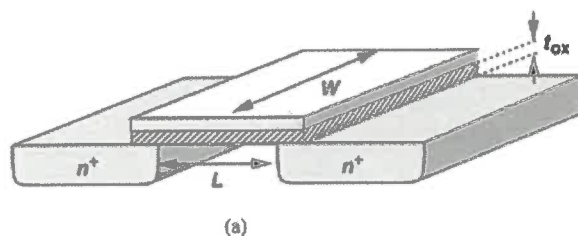
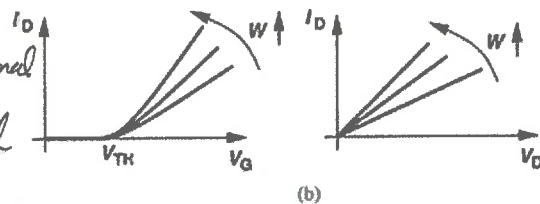
② The ~~Area~~ Oxide thickness (t_{ox}) Effects :-

- * t_{ox} affects the capacitance value, as $t_{ox} \uparrow$, $C \downarrow$ and hence $Q \downarrow$, lowering the number of electrons in the channel this will increase $R_{on} \uparrow$.
- * Therefore, it is desirable to lower the oxide thickness.
- * It can be noticed in figures "c" and "d" that an increase in t_{ox} lowers the slope of the lines in the $I_D - V_{GS}$ and $I_D - V_D$ characteristics.

③ The width of the transistor W :-

* Increasing the Width $W \uparrow$ should reduce R_{on} of the channel since

R is inversely proportional to the cross sectional area.



Hence $W \uparrow \rightarrow R_{on} \downarrow \rightarrow I_D \uparrow$

- * A wider Device can be created by two similar devices connected in parallel. Increasing $W \uparrow$ will also increase the capacitance which will negatively affect the switching speed.

Note :-

- * W and L can be controlled by the cct. designer
- * t_{ox} can't be controlled by the cct. designer it is only specified by the fabrication process

* The Channel Pinch-OFF :-

* The MOS Device is not only a variable resistor but it is also a current source.

* Referring to fig(1)(a) it can be noticed that the Voltage difference between the Gate (G) and the Oxide surface $> V_{TH}$ for the channel to exist.

* When $V_D > 0$ this change the voltage drop profile across the channel or at the oxide material bottom surface.

* At $x=0$ in fig(1)(a)

the voltage drop @ the bottom of the oxide material $\rightarrow 0$, this increases as $x > 0$ and reaches a max at $x=L$,

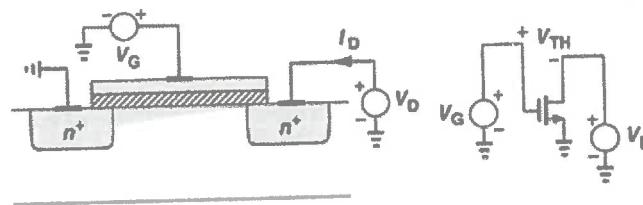
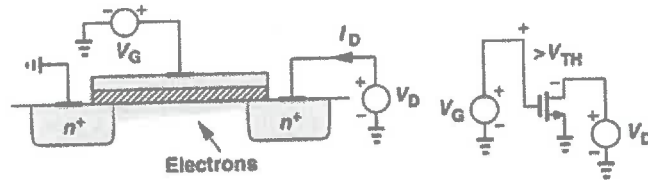
* The voltage drop increases as we reach the drain.

* The Voltage difference as we move from S-D is shown in fig(1)(b).

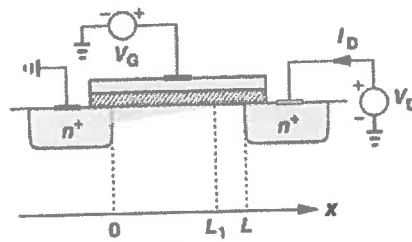
* At $x=0$ $\Delta V = V_G$

* At $x=L$ $\Delta V = V_D - V_G$

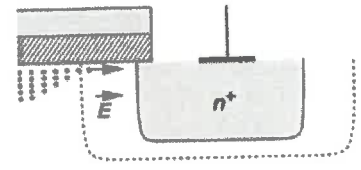
Fig (2)



(a)

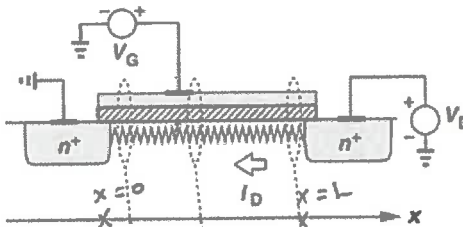


(b)

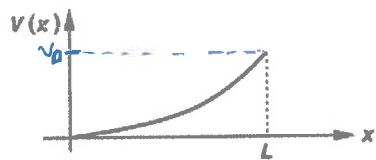


(c)

Fig (1)

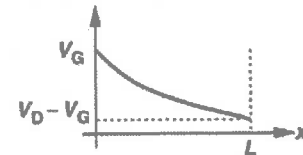


Potential Difference $= V_G < V_G = V_G - V_D$



(a)

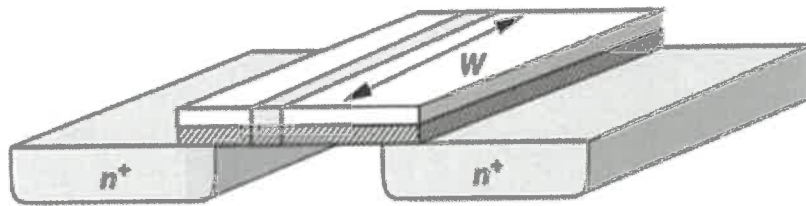
Gate-Substrate Potential Difference



(b)

- * Referring to fig(2) (a), if $V_G - V_D > V_{TH}$ at $x=L$, the channel will be wide at $x=0$ and narrows as we get close to $x=L$.
- * If $V_G - V_D = V_{TH}$ then the channel will become narrower at $x=L$.
- * If $V_G - V_D < V_{TH}$ the channel will only exist up to $x = L_1 < L$.
- * The above two conditions are called "pinch-off".
- * The Electrical field at "D" is sufficient to sweep electrons from $x = L_1$ to the Drain.
- * At this stage, the further increase of V_D does not affect the current significantly making the MOS an independent current source from the Drain control. and becomes a constant current source.

* Derivation of I-V Characteristics :-



fig(1)

* To derive the D current I_D which depends on V_G and V_D , we assume the following :-

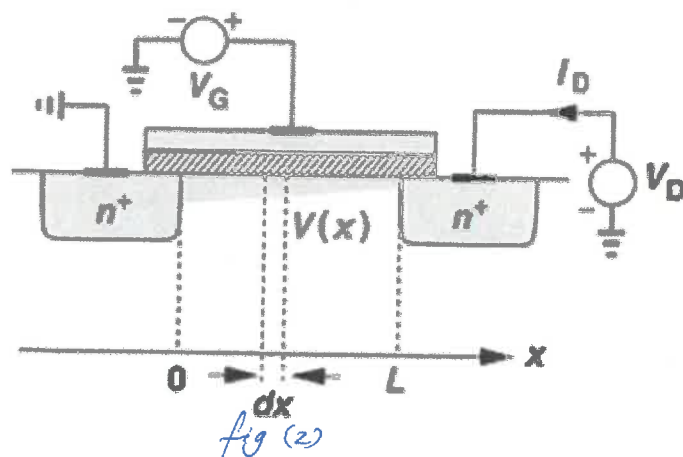
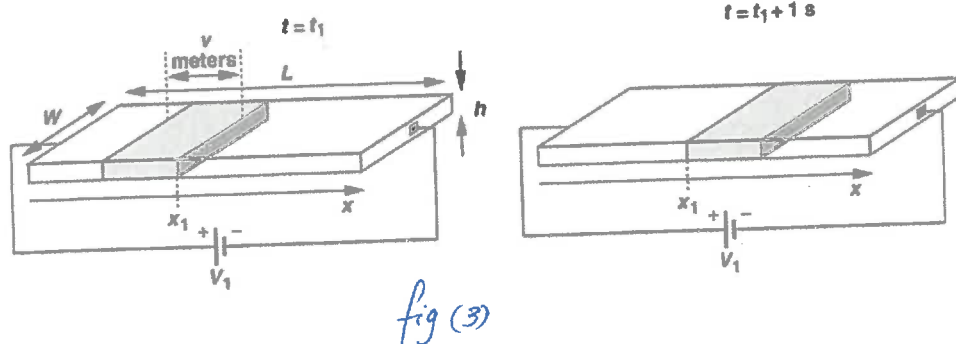


fig (2)

* We realized that I_D results if $V_G > V_{TH}$ and $V_D > 0$.

* we also observed the effect of increasing $V_D(x)$ from 0 - V_D along the S_1D path.



- * We concluded that the current I_D is a drift current.
- * Assuming a Q charge density enclosed in the cube defined by W (width) an v (meters) Length and h (height) and observing the movement of this charge with a velocity of v (meters)/sec ~~at~~ from x_1 at $t = t_1$ to $x_1 + v$ (meters) at $t = t_1 + 1 \text{ sec}$, the current I_D can be defined as follows :-

$$I_D = Q \cdot v, \text{ where } v \text{ is the } \begin{matrix} \text{Drift} \\ \text{velocity in m/sec.} \end{matrix}$$

Q is the charge $\begin{matrix} \text{density} \\ \text{in C/meter} \end{matrix}$

- * The Drift velocity $v = -\mu_n E$, where μ_n is the electrons mobility.
- * Recall that the electrical field applied across a distance dx from $a-b$ is related to the voltage as $V = -\int_a^b E \cdot dx$

$$\rightarrow \rightarrow E = -\frac{dV}{dx} \rightarrow v = +\mu_n \frac{dV}{dx}$$

hence

$$I_D = Q \cdot \mu_n \frac{dV}{dx}.$$

- * Q is expressed as $Q = CV$, to invoke the transistor dimensions $C = C_{ox} \cdot W$, C_{ox} (fF/ μm^2 or F/m^2)
 - * V has two cases if V_{DS} (DS voltage, the source will be used as a ref)
- $V_{DS} = 0$ then the charge Density Q is controlled by $(V = V_{GS} - V_{TH})$

* If $V_{DS} > 0$ then the charge density reduces (due to pinch-off effects) across the S,D path.

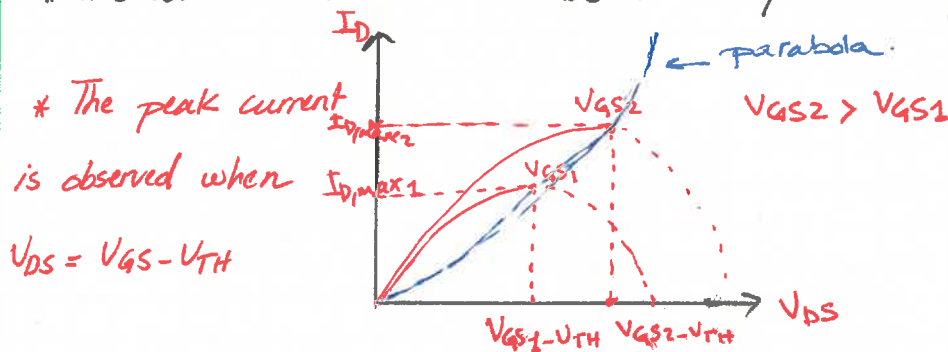
In this case $V = (V_{GS} - V(x) - V_{TH})$

$$I_D = W C_{ox} [V_{GS} - V(x) - V_{TH}] \cdot \mu_n \frac{dV}{dx} \quad (\text{see fig (2)})$$

$$\int_{x=0}^{x=L} I_D \cdot dx = \int_{V(x)=0}^{V(x)=V_{DS}} W \cdot C_{ox} [V_{GS} - V(x) - V_{TH}] \cdot \mu_n \cdot dV$$

Hence $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]$

* The above indicates that I_D varies parabolically with V_{DS} . (for fixed V_{GS})



$$I_{Dmax} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_{TH}]^2$$

$V_{DS} = V_{GS} - V_{TH}$

* Note: It is Desirable to keep $\frac{W}{L}$ as a ratio to express these quantities.

* MOSFET resistive behavior :-

+ by referring to the I_D formula it can be observed that the relationship between I_D and V_{DS} is not linear, therefore the transistor can't be modeled as a resistor.

* To achieve a resistive behavior $V_{DS} \ll 2(V_{GS} - V_{TH})$

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \cdot V_{DS}$$



* In this case $R_{ON} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$

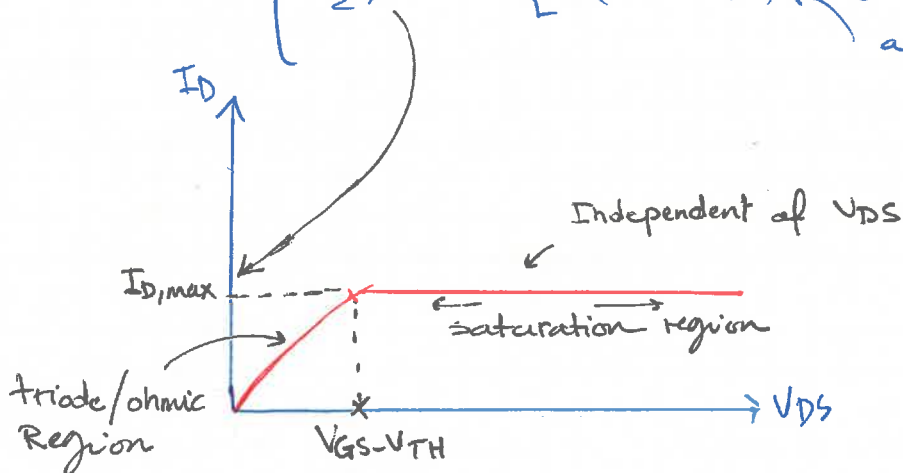
* MOSFET OPERATION REGIONS :-

* $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH}) - V_{DS}]^2$

* The above equation indicates that if $V_{DS} > V_{GS} - V_{TH}$ then $I_D \downarrow$ decreases. Practically, this does not happen, instead the current I_D reaches a constant value.

$$I_D = \begin{cases} \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH}) - V_{DS}]^2, & V_{DS} < V_{GS} - V_{TH} \\ \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2, & V_{DS} > V_{GS} - V_{TH} \end{cases}$$

a constant value $= I_{D,max}$



* 1 Triode Region :- I_D depends on V_{DS} .

* If we want the MOSFET to work as a resistor $V_{DS} \ll 2(V_{GS} - V_{TH})$

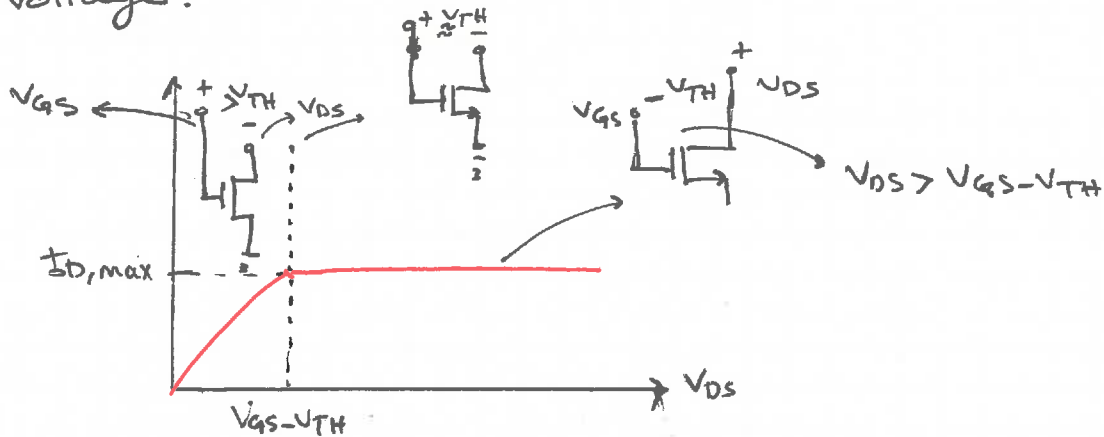
2 Saturation Region :- I_D is max and is independent from V_{DS} .

This region is Desirable when we design amplifiers.

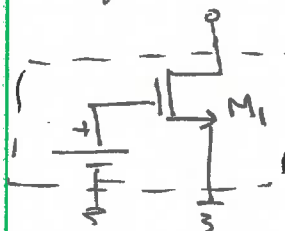
* Attention : The Saturation Region for MOSFET is ~~not~~ equivalent to the active region in BJT.

Note: The quantity $(V_{GS} - V_{TH})$ is called the "over-drive" voltage.

* MOSFETs are called Square law device to emphasize the relationship between I_D and the over-drive voltage.



* when $V_{DS} > V_{GS} - V_{TH}$ and the MOS is in the saturation region then the MOS can be regarded as a current source.



$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

voltage controlled Current source.

Ex: Calculate the bias current of M_1 . Assume $\mu_n C_{ox} = 100 \mu A/V^2$ and $V_{TH} = 0.4 V$. If the gate voltage increase by $10 mV$, what is the change in the drain voltage?

