

Lab 4 Report

Acknowledgements:

- Figures 3.1, 3.2, 3.3 and Figure 0 (expressions for prelab) were taken from Dr. Alhloul's Lab#4.

Prelab: Diode Calculations

Values:

- For prelab, certain pertinent diode parameters were given in order to calculate various other diode parameters (Equations for which are shown in Figure 1). They are as follows:
 - $N_A = 10^{15} \text{ atoms/cm}^3$
 - $N_D = 10^{17} \text{ atoms/cm}^3$,
 - $A = 0.025 \text{ cm}^2$,
 - $T = 300\text{k}$,
 - $D_n = 34 \text{ cm}^2/\text{s}$,
 - $D_p = 12 \text{ cm}^2/\text{s}$,
 - $L_n = 20\mu\text{m}$,
 - $L_p = 30\mu\text{m}$,
 - $E_{\text{critical}} = 3 \times 10^5 \text{ V/cm}$,
- Certain constant values were also known:
 - $n_i(T = 300\text{K}) = 1.08 \times 10^{10} \text{ electrons/cm}^3$,
 - $\epsilon_{\text{si}} = 11.7 \times 8.85 \times 10^{-14} \text{ F/cm}$,
 - $q = 1.6 \times 10^{-19} \text{ C}$,
 - $V_T \approx 26 \text{ mV}$,

Calculations:

This is left blank intentionally

Part 1: LTspice Simulation of Diode (Default)

Description (0volts):

In the beginning of the lab experiment, an LTspice netlist file was created, called “Lab4_Sergey_Brandon_Diode.net.” In the blank netlist, a single diode, D1, was ‘placed’ in parallel (Forward Biased) with a 0v source, V1, and was then given a model name of “NoClue.” Further, the netlist command “.model NoClue D1” was utilized in order to convey to LTspice that the model for the diode “NoClue” was to be defined, however, no parameters were set for this model. A DC operating point analysis was also simulated by adding a command of “.op” to the netlist. (See Figure 1.1 for netlist) Notice how the students referenced a figure in their discussion

Analysis (0volts):

The DC operating point analysis simulation of the netlist is as shown in Figure 1.2, where all noted values are equal to zero (due to the 0v input). After this simulation, the LTspice error log was opened, as shown in Figure 1.3, and in viewing the diode designator it was noted that these values were the default parameters given by LTspice for a diode. It was also noted that the capacitance value defaulted by LTspice’s diode model (and considered as the initial capacitance in the diode) was listed as 0 F.

Description (0.7volts):

The netlist circuit from above was recreated, only this time with a 0.7v source (See Figure 1.4).

Analysis (0.7volts):

The DC operating point analysis simulation of the netlist is as shown in Figure 1.5. After this simulation, the LTspice error log was opened, as shown in Figure 1.6. In viewing the diode designator, the current through the diode was noted as 5.67mA.

Now, in using the given formula: Notice the technical reasoning, where the students used the formulas learned in the class into justifying the observed experiment results

$$I_D = I_s [\exp(V_D / V_T) - 1],$$

we can calculate that LTspice’s default diode model value for Reverse Saturation Current, I_s , is as follows:

$$I_D = I_s [\exp(V_D / V_T) - 1]; \text{ Where } I_D = 5.67\text{mA}, V_D = 0.7\text{v}, \text{ and } V_T = 26\text{mv}$$

$$\rightarrow 5.67\text{mA} = I_s [\exp(700\text{mv}/26\text{mv}) - 1] \rightarrow I_s = 5.67\text{mA} / [\exp(700\text{mv}/26\text{mv}) - 1]$$

Prelab Figure:

Figure 0 - Expressions for Prelab

Expressions to solve lab4 prelab

$$I_S = A q n_i^2 \left(\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D} \right) \rightarrow \text{Reverse Saturation Current}$$

$$V_o = V_T \ln \frac{N_A N_D}{n_i^2} \quad - \text{Built-in potential}$$

$$V_{BV} = \frac{\epsilon_{Si} (N_A + N_D)}{2 q N_A N_D} E_{critical}^2 \quad - \text{Breakdown Voltage}$$

$$C_{j0} = \sqrt{\frac{\epsilon_{Si} q N_A N_D}{2 (N_A + N_D) V_o}} \quad - \text{Zero bias Junction Capacitance Per unit area}$$

$$C_j = \frac{C_{j0}}{\sqrt{1 - \frac{V_D}{V_o}}} \quad - \text{Junction Capacitance per unit area}$$

$$I_D = I_S \left[\exp \frac{V_D}{V_T} - 1 \right] \quad - \text{Diode Current}$$

Part One Figures:

Figure 1.1 - Netlist Code (For V1 = 0volts)

```
|Sergey_Brandon_Lab4 01/30/2020  
  
V1 A 0 0; 0V source  
D1 A 0 NoClue; Diode in parallel with voltage source  
  
.op; DC operation  
  
.model NoClue D1; Diode model command
```

Figure 1.2 - DC Operating Point Analysis (For V1 = 0volts)

Sergey_Brandon_Lab4 01/30/2020		
--- Operating Point ---		
V(a) :	0	voltage
I(D1) :	0	device_current
I(V1) :	0	device_current

Figure 1.4 - Netlist Code (For $V_1 = 0.7\text{volts}$)

```
|Sergey_Brandon_Lab4 01/30/2020  
  
V1 A 0 0.7; 0.7V source  
D1 A 0 NoClue; Diode in parallel with voltage source  
  
.op; DC operation  
  
.model NoClue D1; Diode model command
```

Part Two Figures:

Figure 2.1 - Netlist Code (Diode model XYZ, For V1 = 0volts)

```
Sergey_Brandon_Lab4 01/30/2020

V1 A 0 0; 0V source
D A 0 XYZ; Diode in parallel with voltage source

.model XYZ D (IS=7.95p CJO=268p); New diode model with Reverse Saturation current
                                   ; and Total Zero Bias junction capacitance specified.

.op; DC operation
```

Figure 2.2 - DC Operating Point Analysis (Diode model XYZ, For V1 = 0volts)

```
Sergey_Brandon_Lab4 01/30/2020

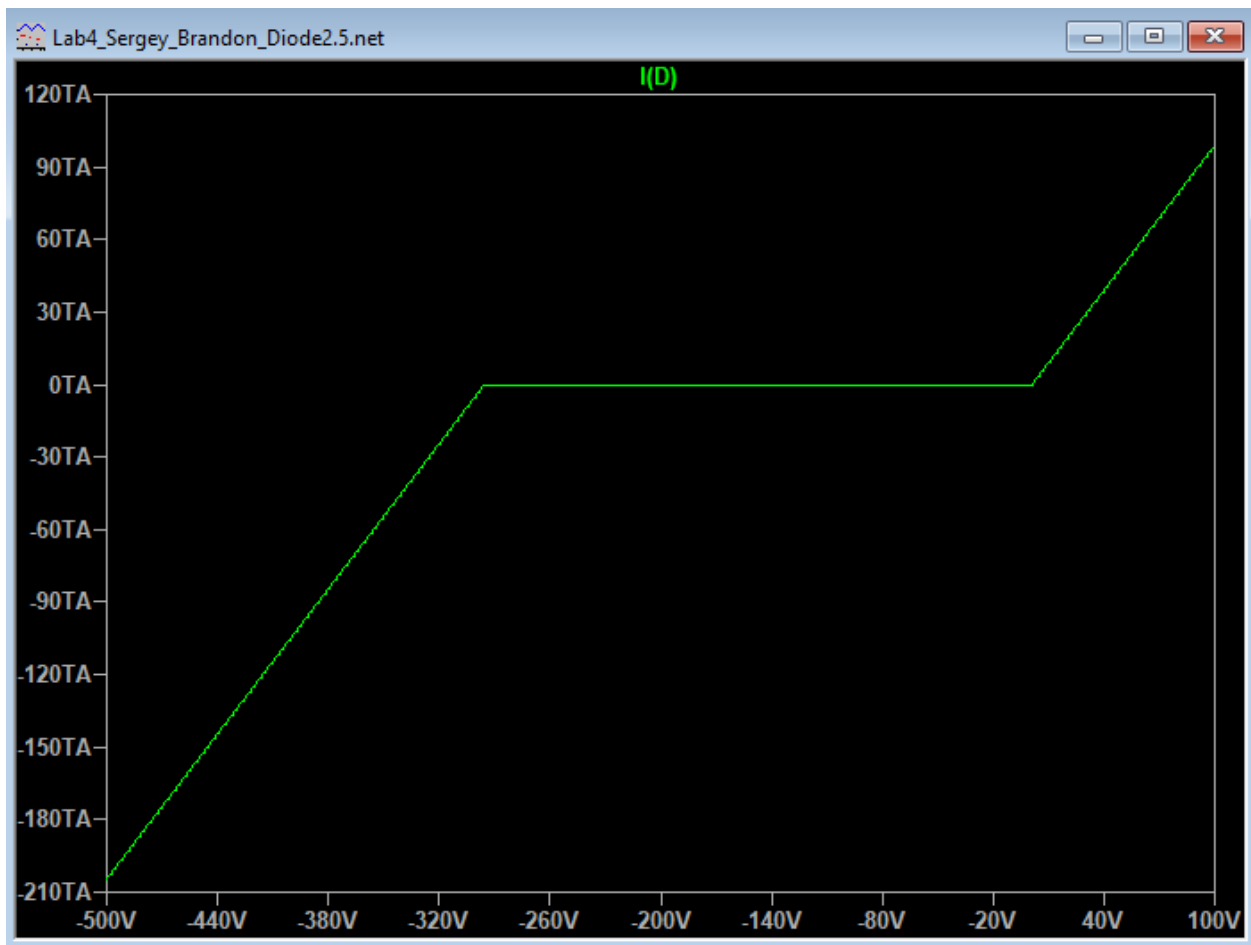
--- Operating Point ---

V(a) :      0      voltage
I(D) :      0      device_current
I(V1) :      0      device_current
```

Figure 2.10 - Netlist (Diode model XYZ with Breakdown Voltage)

```
Sergey_Brandon_Lab4 01/30/2020  
  
V A 0; 0V source  
D A 0 XYZ; Diode in parallel with voltage source  
  
.model XYZ D (IS=7.95p CJ0=268p BV=294)  
  
.op; DC operation  
  
.dc V -500 100 0.01; Voltage source sweep from -500V to 100V in increments of 0.01V.
```

Figure 2.11 - I/V curve (Diode model XYZ with Breakdown Voltage)



Part Three Figures:

Figure 3.1 - Half-wave rectifier with resistor (from lab prompt)

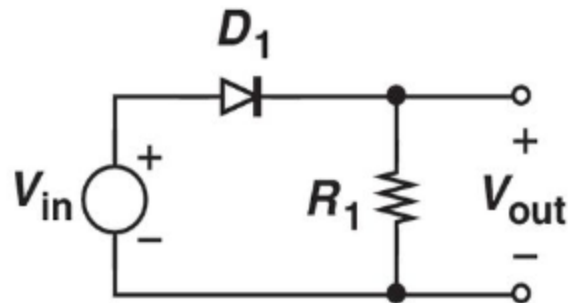


Figure 3.2 - Half-wave rectifier with Capacitor (from lab prompt)

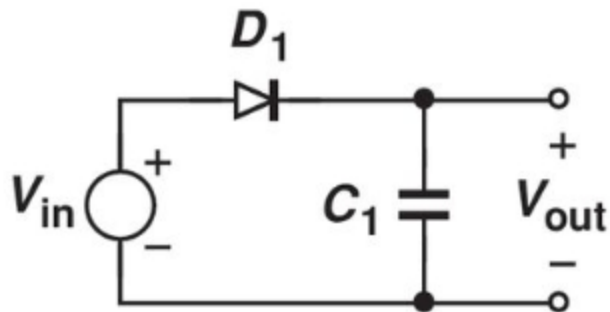


Figure 3.3 - Half-wave rectifier with load resistor (from lab prompt)

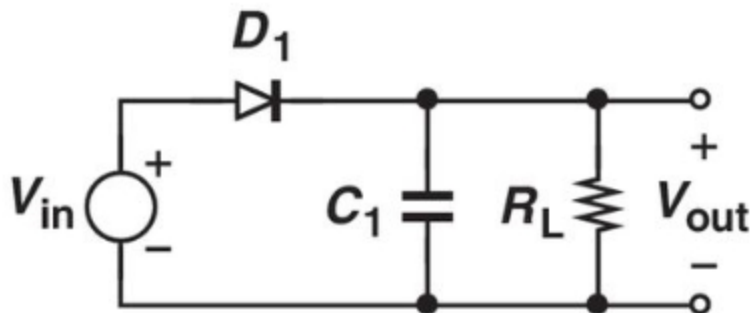


Figure 3.4 - Netlist for Half-wave rectifier with resistor

|Sergey_Brandon_Lab4 01/30/2020

```
Vin A 0 SINE(0 5 1K); Source with peak voltage of 5v and frequency of 1000Hz.  
D3.1 A 1 XYZ; Diode in parallel with voltage source  
R3.1 1 0 1K; Resistor load  
  
.model XYZ D (IS=7.95p CJ0=268p BV=294)  
  
.tran 0 10m; Transient Analysis
```

Figure 3.5 - Input/Output for Half-wave rectifier with resistor
BLUE → Input & GREEN → Output

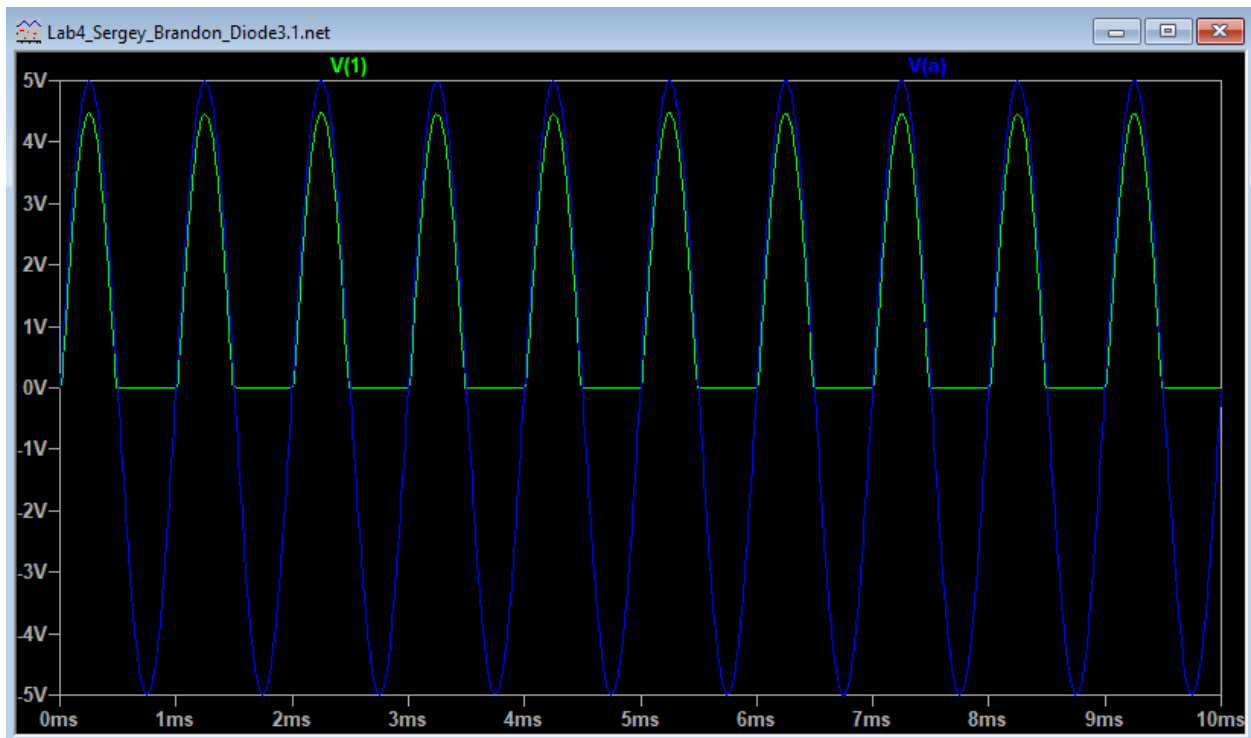


Figure 3.6 - Netlist for Half-wave rectifier with Capacitor

```
Sergey_Brandon_Lab4 01/30/2020  
  
Vin A 0 SINE(0 5 1K); Source with peak voltage of 5v and frequency of 1000Hz.  
D3.2 A 1 XYZ; Diode in parallel with voltage source  
C3.2 1 0 10; 10p capacitor  
  
.model XYZ D (IS=7.95p CJO=268p BV=294)  
  
.tran 0 10m; Transient Analysis
```

Figure 3.7 - Plot for Half-wave rectifier with Capacitor

BLUE → Input & GREEN → Output

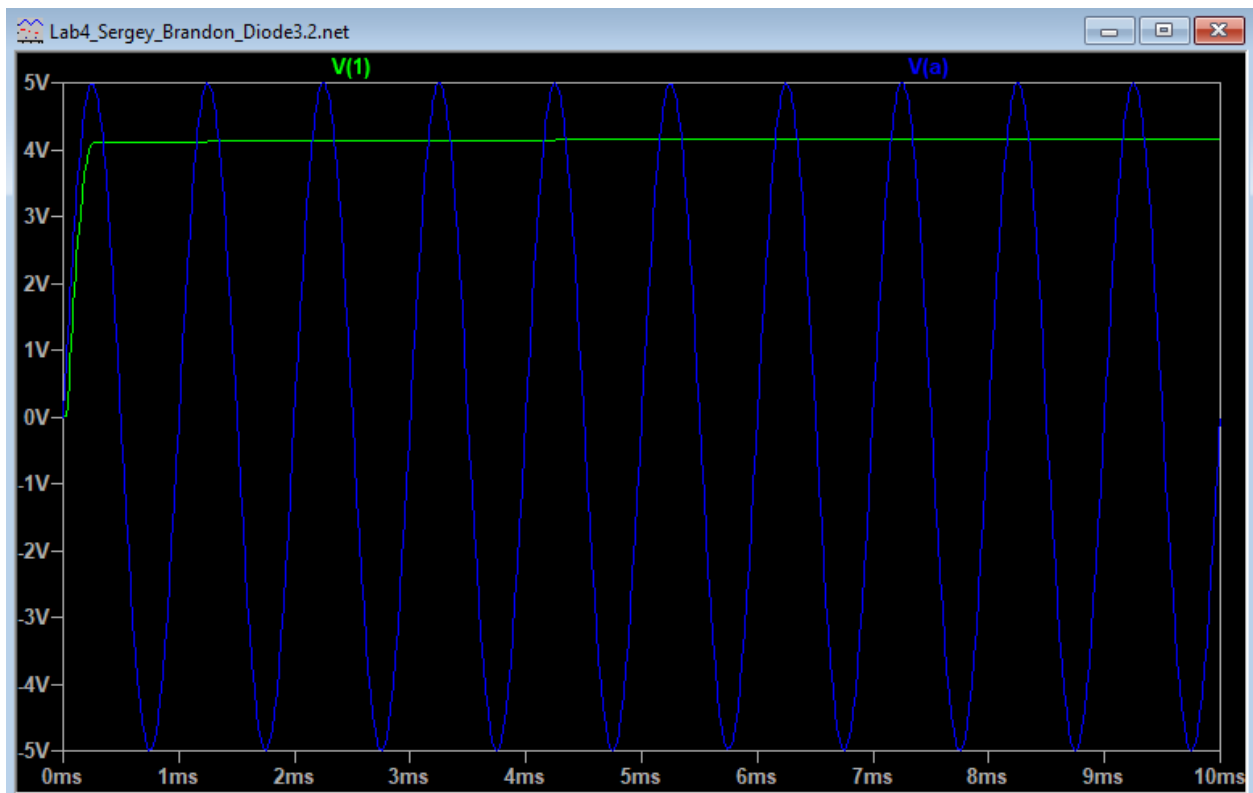


Figure 3.8 - Netlist for Half-wave rectifier with load resistor

```
Sergey_Brandon_Lab4 01/30/2020  
  
Vin A 0 SINE(0 5 1K); Source with peak voltage of 5v and frequency of 1000Hz.  
D3.3 A 1 XYZ; Diode in parallel with voltage source  
C3.3 1 0 1m; Capacitor  
RL3.3 1 0 10; Resistor load  
  
.model XYZ D (IS=7.95p CJO=268p BV=294)  
  
.tran 0 10m; Transient Analysis
```

Figure 3.9 - Plot for Half-wave rectifier with load resistor

BLUE → Input & GREEN → Output

