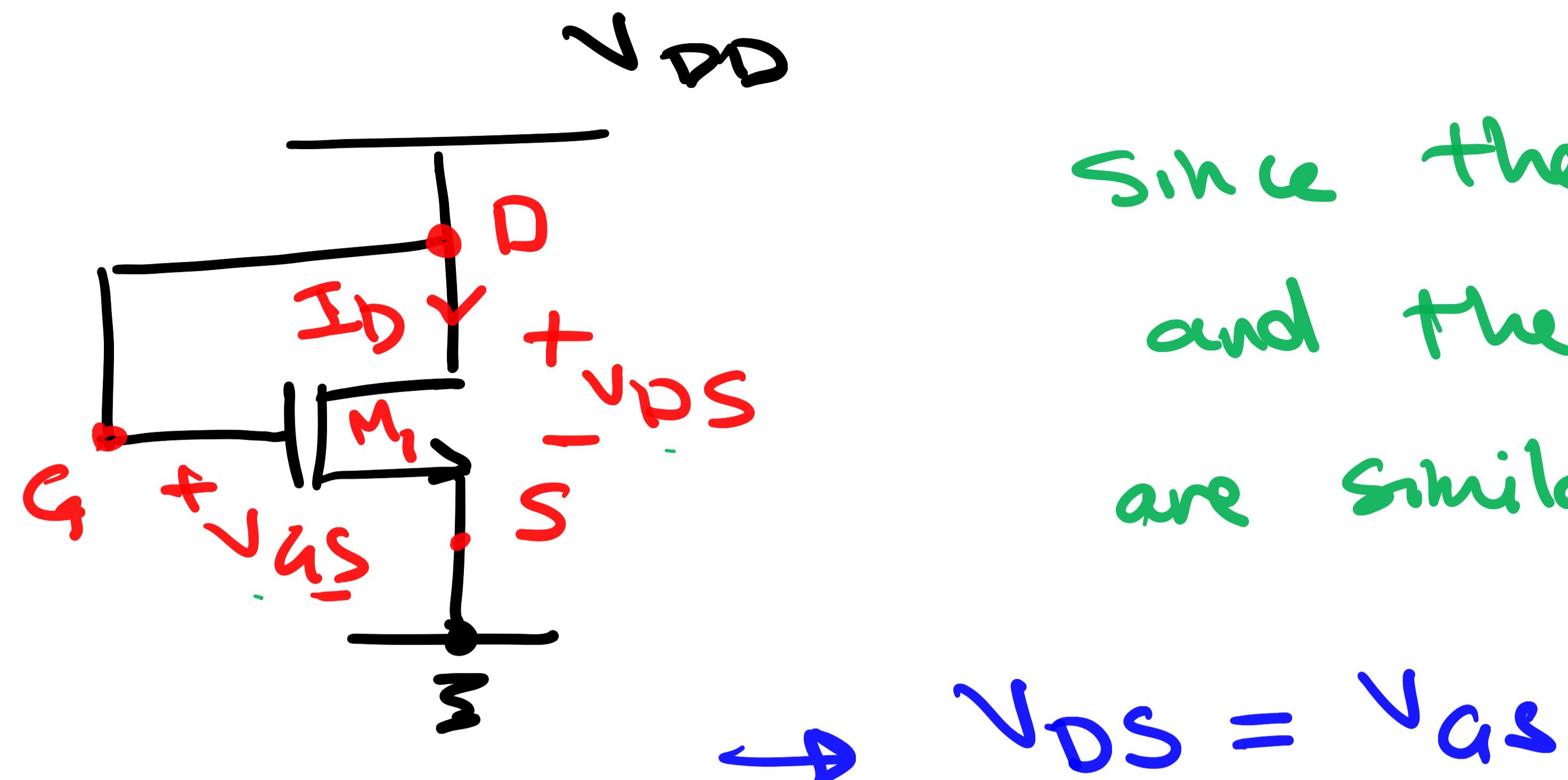


## \* Realization of current sources :-

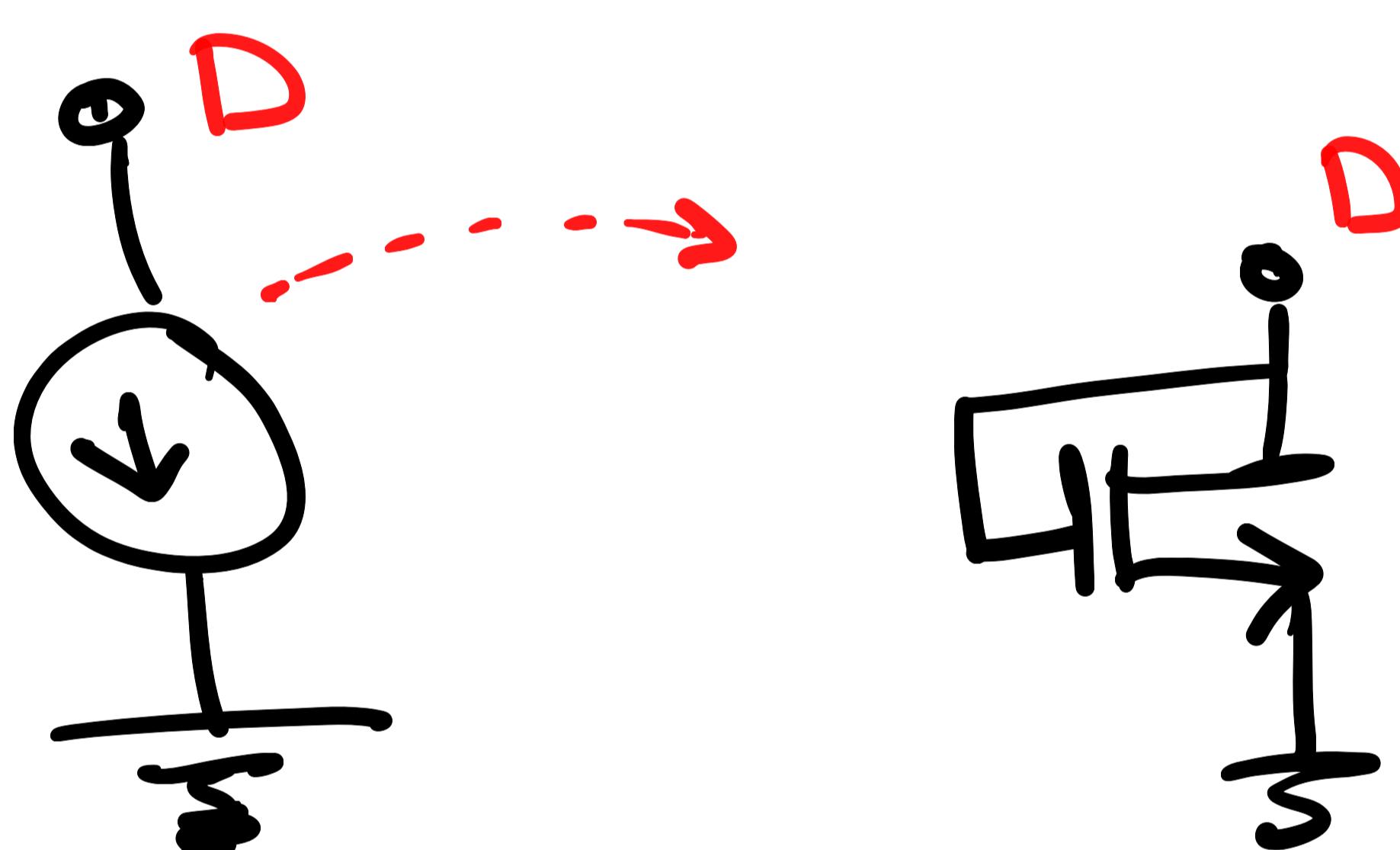
Diode connected devices



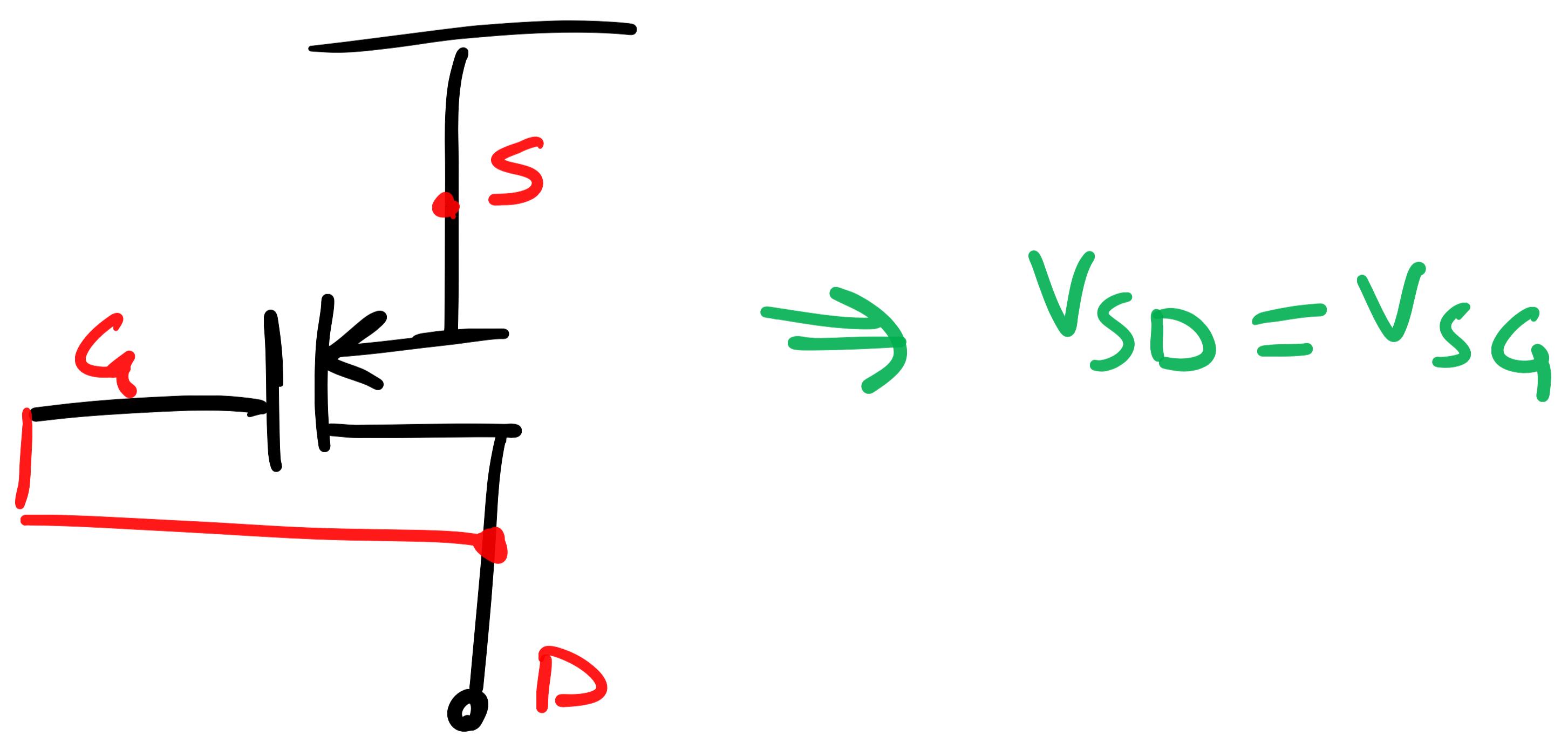
Since the D node and the G node are similar

$\rightarrow$  we conclude that this connection puts  $M_1$  always in the sat. region.

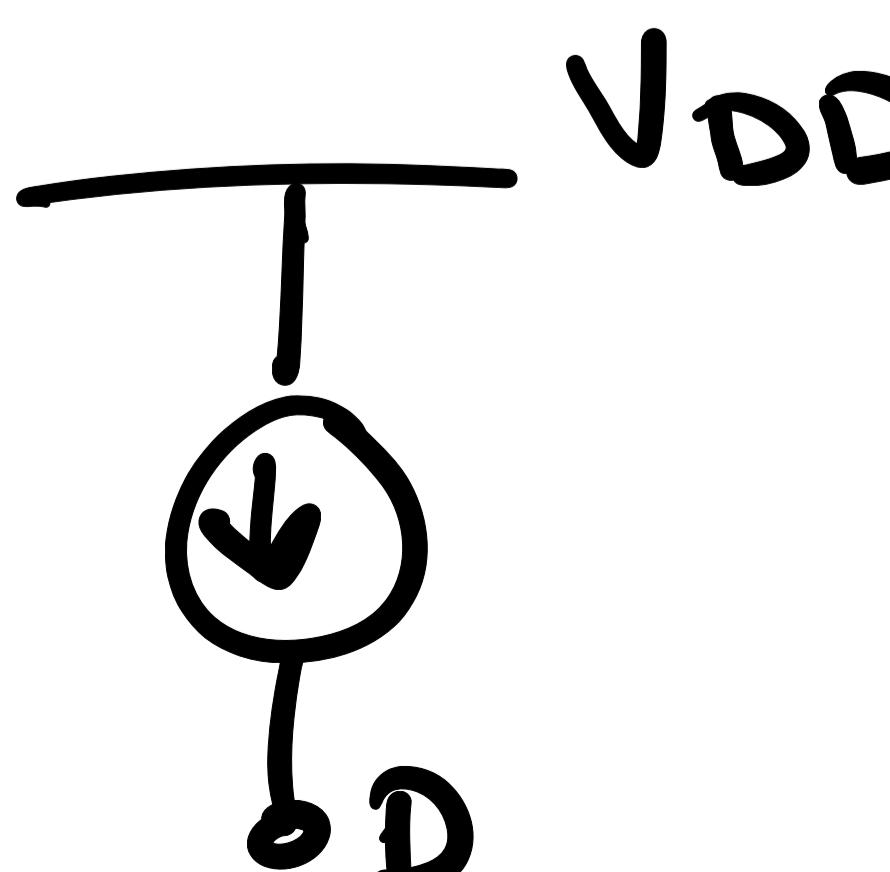
The above cct realizes this current source



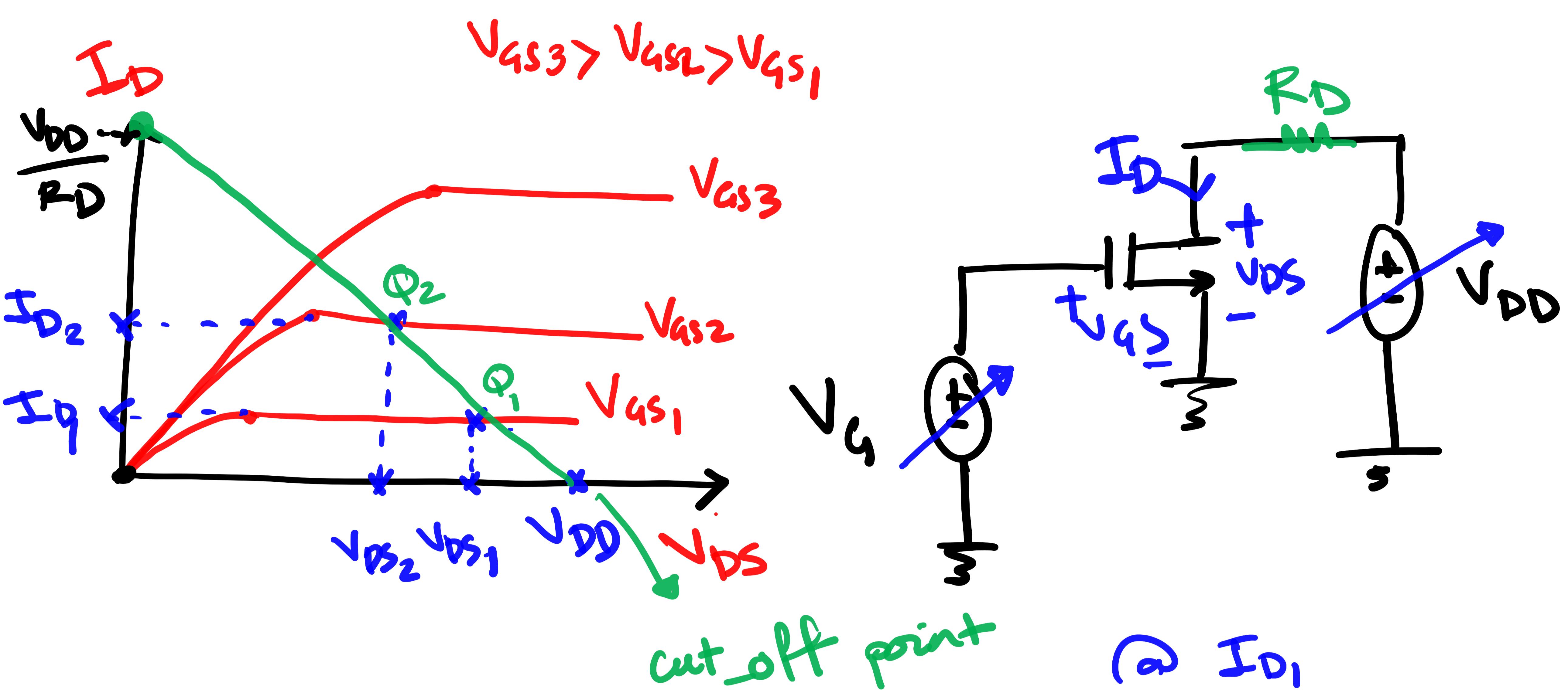
\* The other way to realize a current source



$\hookrightarrow$  this realizes this current source



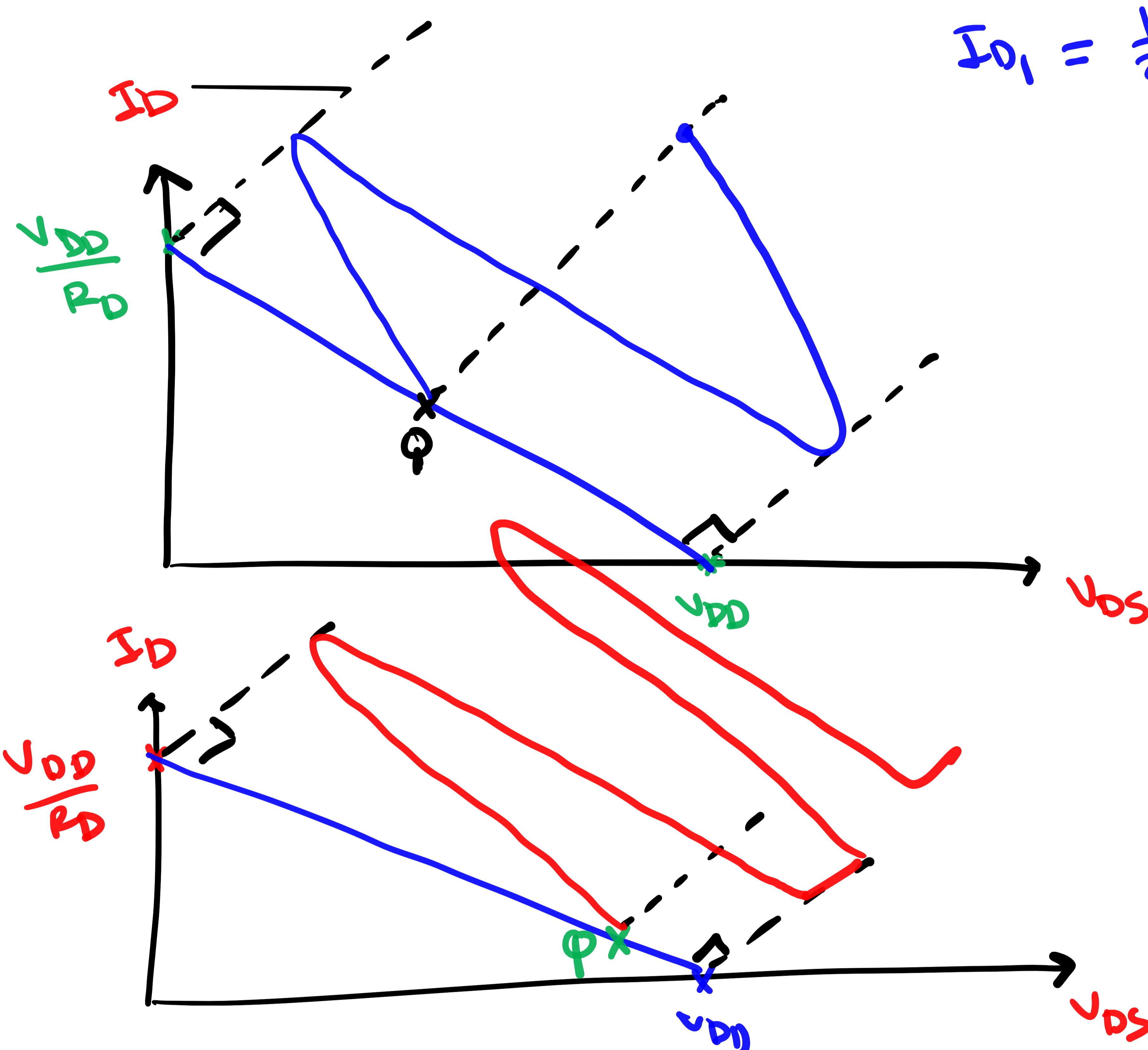
\* The DC Load line :-



@  $I_{D1}$

$$V_{DS_1} = V_{DD} - I_{D1} R_D$$

$$I_{D1} = \frac{1}{2} \mu_{n\text{ox}} \frac{W}{L} V_{GS_1}^2$$



## \* CMOS amplifiers :-

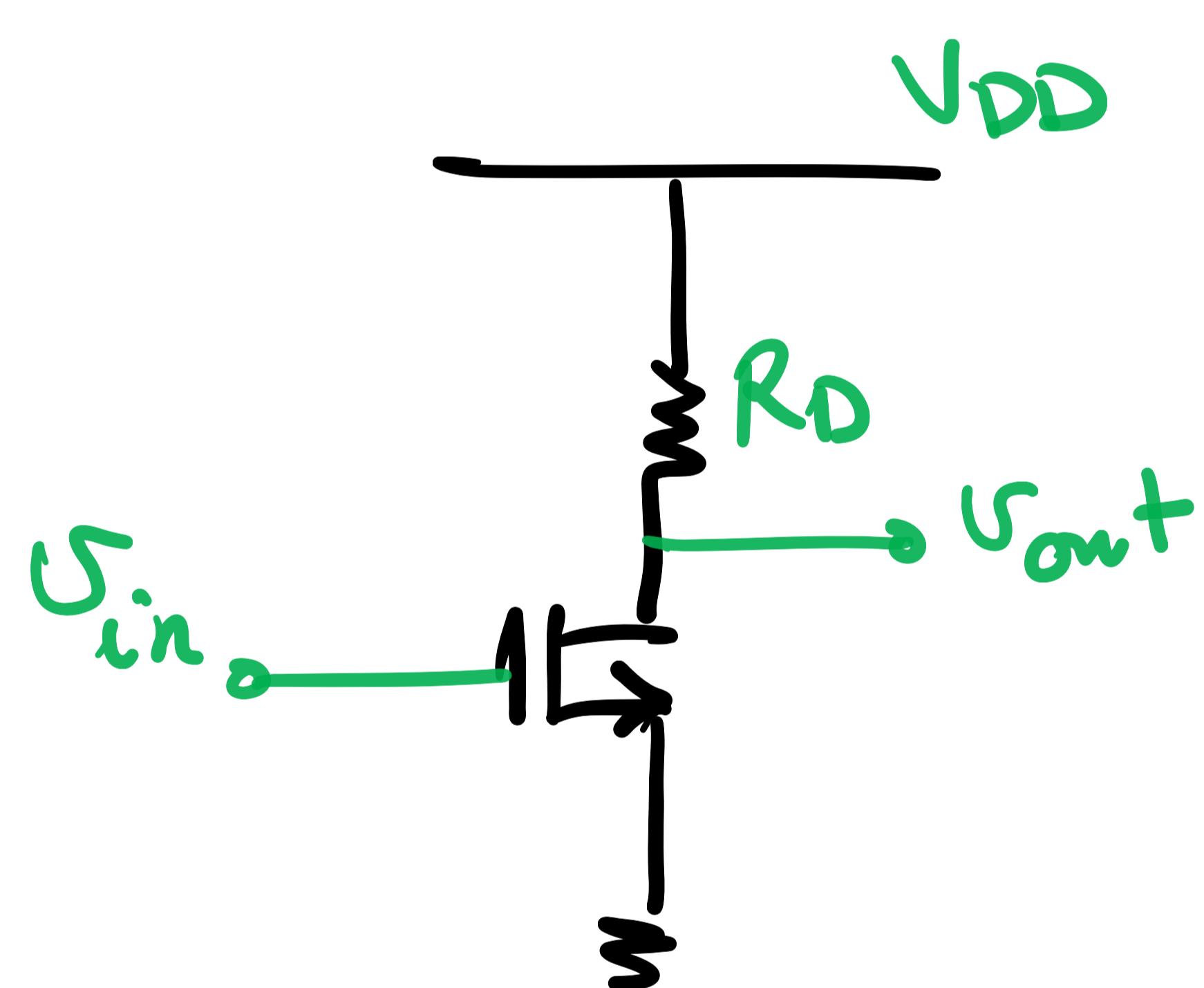
1] Common Source amplifier

2] Common Gate amplifier

3] = Drain = (Source follower)

## \* Common Source Amplifier :-

→ we will study the small signal case



\* We will analyze 3 parameters for each amplifier and those are :-

1] The voltage gain Av

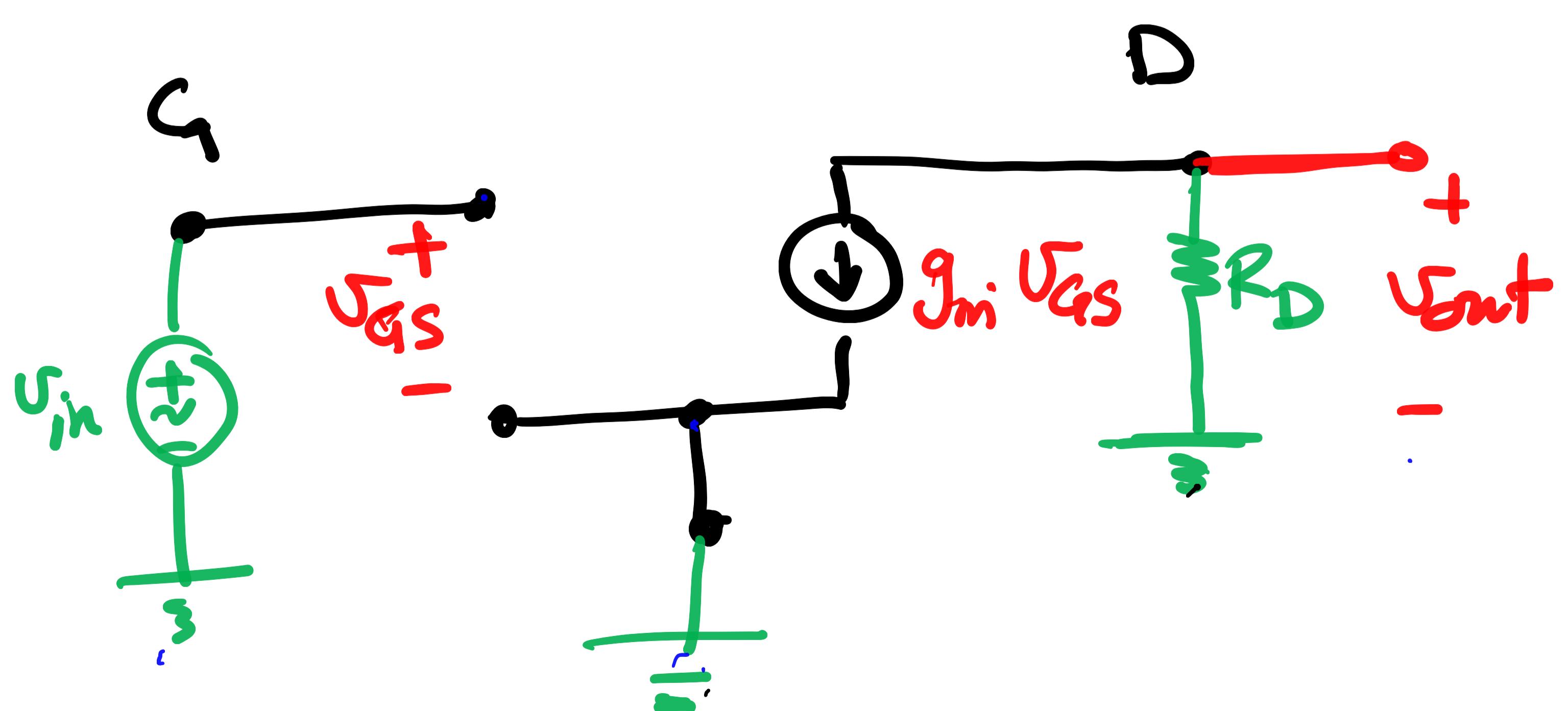
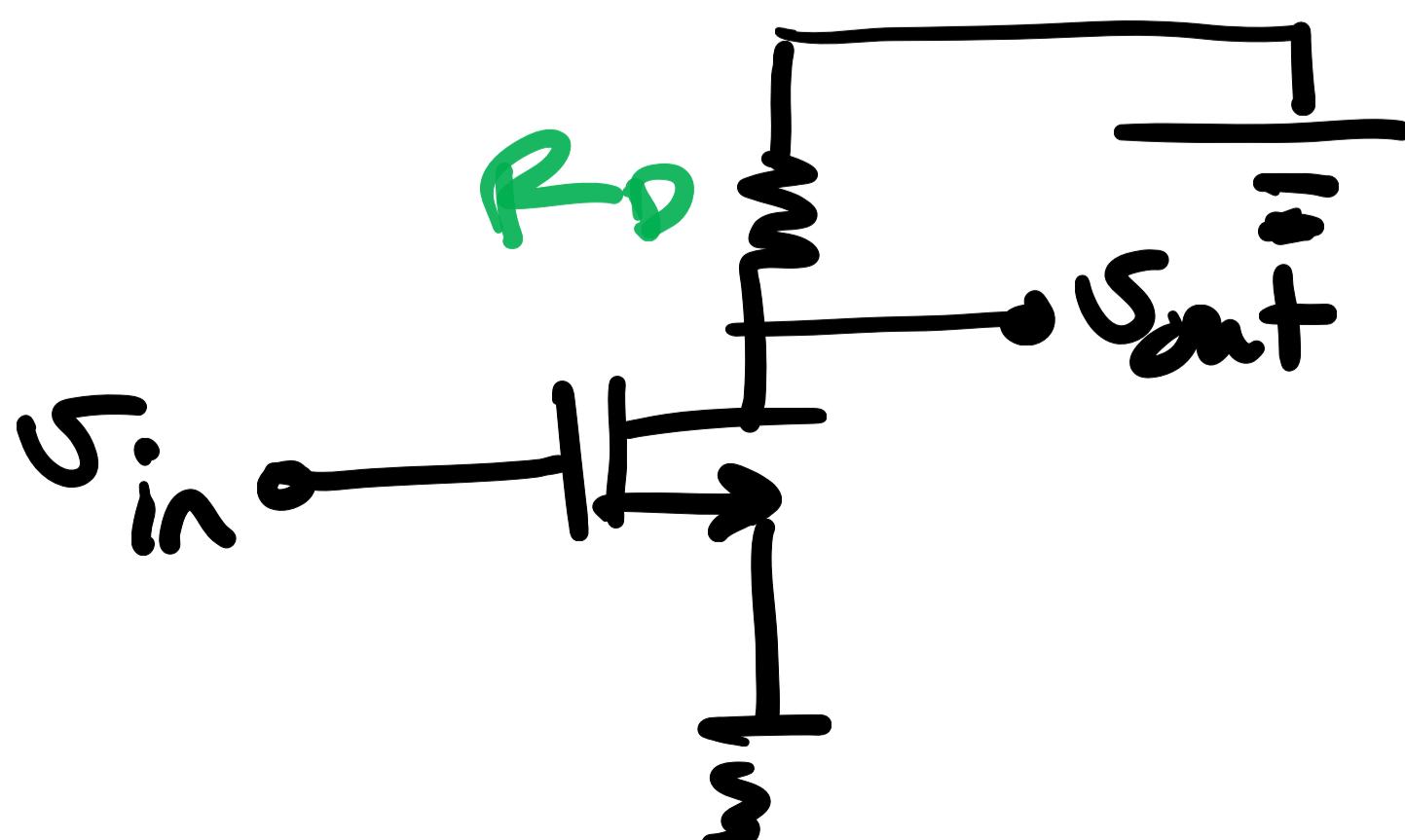
2] The input impedance Rin

3] = output impedance Rout

\* 1] The voltage gain Av

$$Av = \frac{V_{out}}{V_{in}}$$

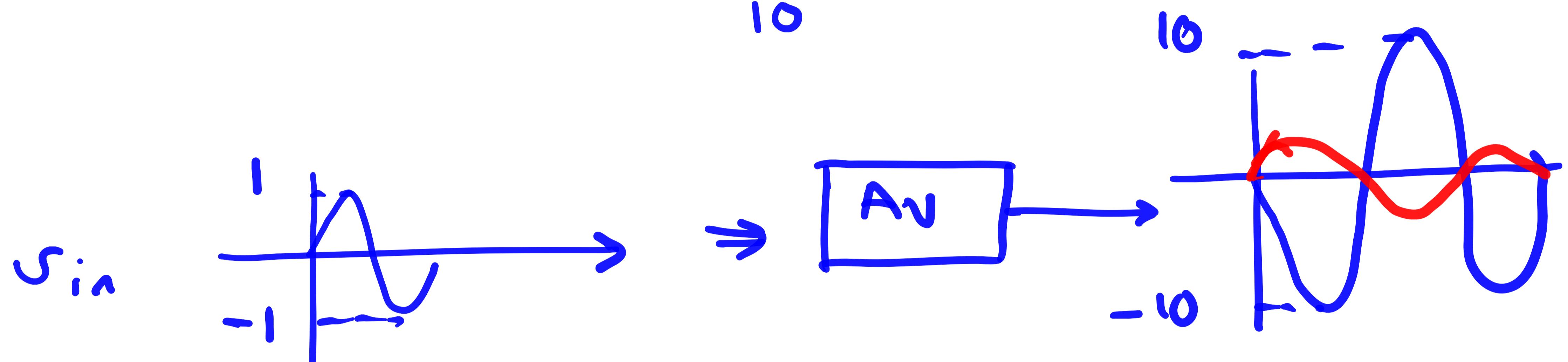
\* Assuming  $\lambda = 0$



$$Av = \frac{V_{out}}{V_{in}} \Rightarrow V_{out} = -g_m \cdot V_{GS} \cdot R_D$$

but  $V_{GS} = V_{in}$   $\Rightarrow \frac{V_{out}}{V_{in}} = -g_m \cdot \frac{V_{in}}{V_{in}} \cdot R_D$

$$Av = \frac{V_{out}}{V_{in}} = \boxed{-(g_m \cdot R_D)}$$



→ gain Analysis

$$Av = -g_m R_D, \quad |Av| = g_m R_D$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{ov}}$$

$$|Av| = 2 \frac{I_D \cdot R_D}{V_{ov}}$$

→ To increase the gain safely (not going to the triode region)

$$V_{DS} > V_{GS} - V_{TH}$$

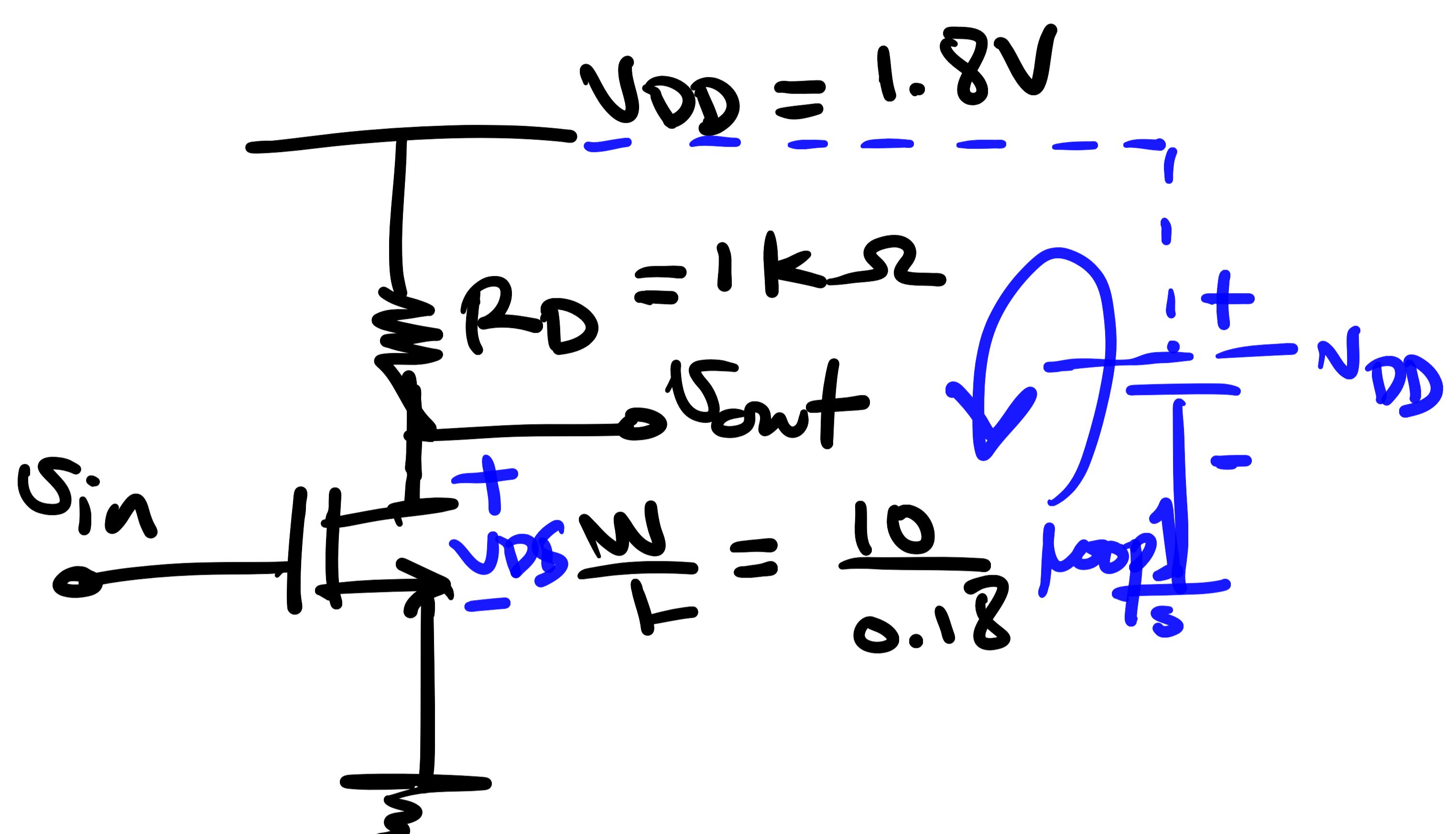
$$V_{DD} - I_D R_D > V_{GS} - V_{TH} \Rightarrow I_D R_D < V_{DD} - V_{ov}$$

Ex: Calculate the small signal gain of the CS stage shown below if  $I_D = 1mA$ ,  $\mu_n C_{ox} = 100 \mu A/V^2$

$V_{TH} = 0.5V$ ,  $\lambda = 0$ , verify that  $M_1$  is in sat?

$$AV = -g_m R_D$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$



$$g_m = \frac{1}{300 \Omega} \Rightarrow AV = g_m \cdot R_D = -3.33$$

$$|AV| = 3.33$$

\* Verify  $M_1$  is in sat?

$$V_{DS} > V_{OV}$$

$$* V_{DS} = V_{DD} - I_D R_D = 0.8V$$

$$* V_{OV} = V_{GS} - V_{TH}, \quad I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

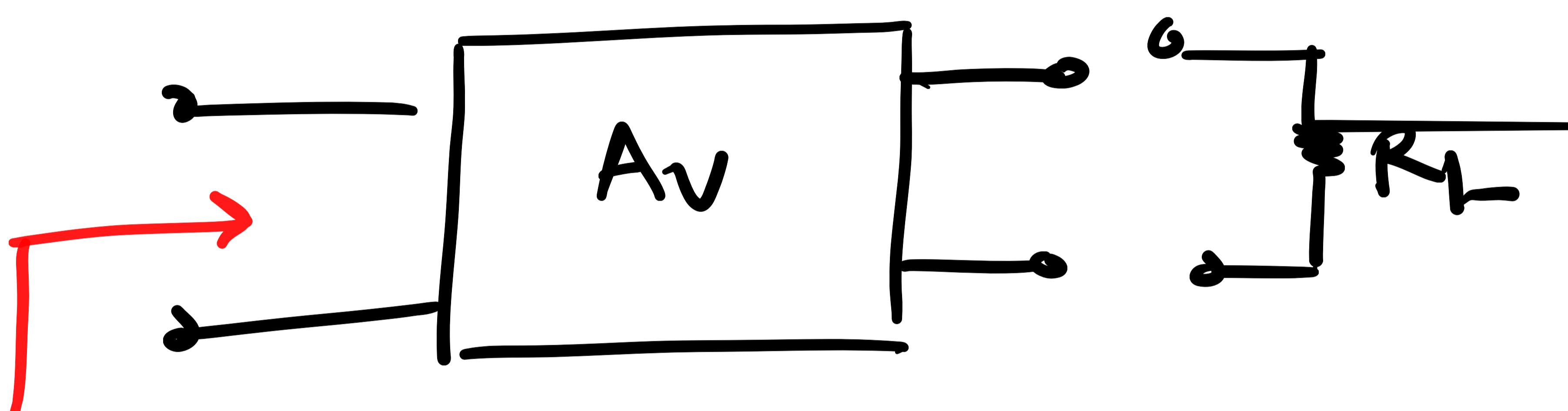
$$\Rightarrow V_{OV} = \frac{2I_D}{g_m} = 0.6V \times g_m = \frac{2I_D}{V_{OV}}$$

$$\Rightarrow V_{OV} = \frac{2I_D}{g_m}$$

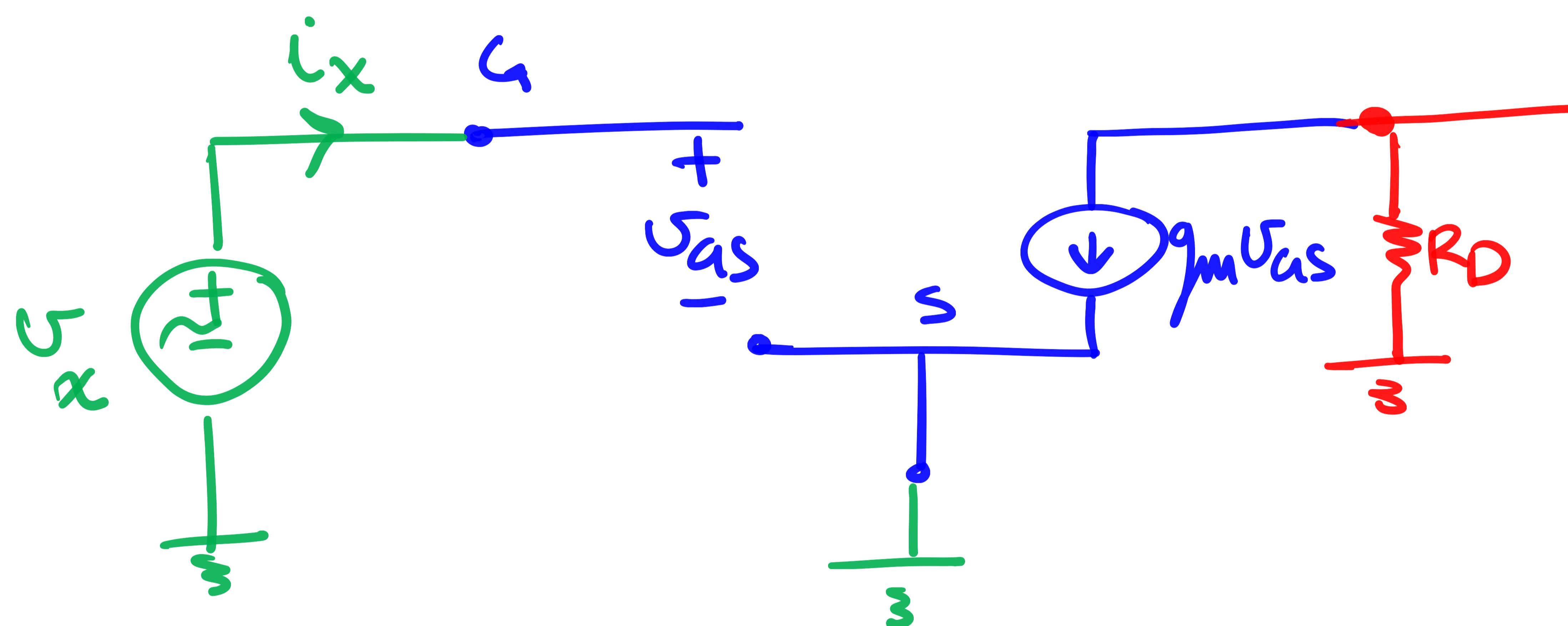
$$V_{DS} > V_{DS} \rightarrow 0.8V > 0.6V \checkmark$$

$M_1$  is in the sat. region.

\* Input Impedance Analysis for a CS stage:  
assume  $\lambda = 0$ .



$R_{in}$  or  $R_{req}$  for  $R_{in} \Rightarrow$  disconnect  $R_L$



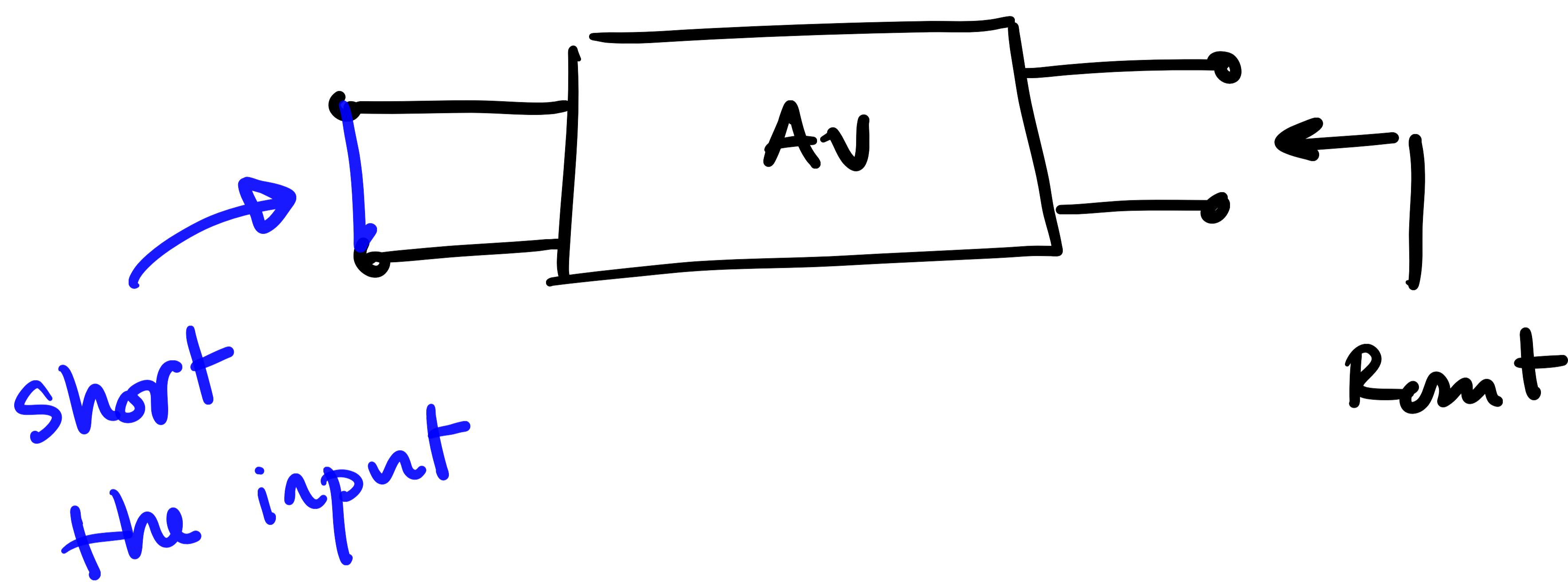
$R_{in} = \frac{U_x}{i_x} \Rightarrow$  due to the open terminals 'g,s'

$$i_x = 0 \Rightarrow R_{in} = \frac{U_x}{0} = \infty$$

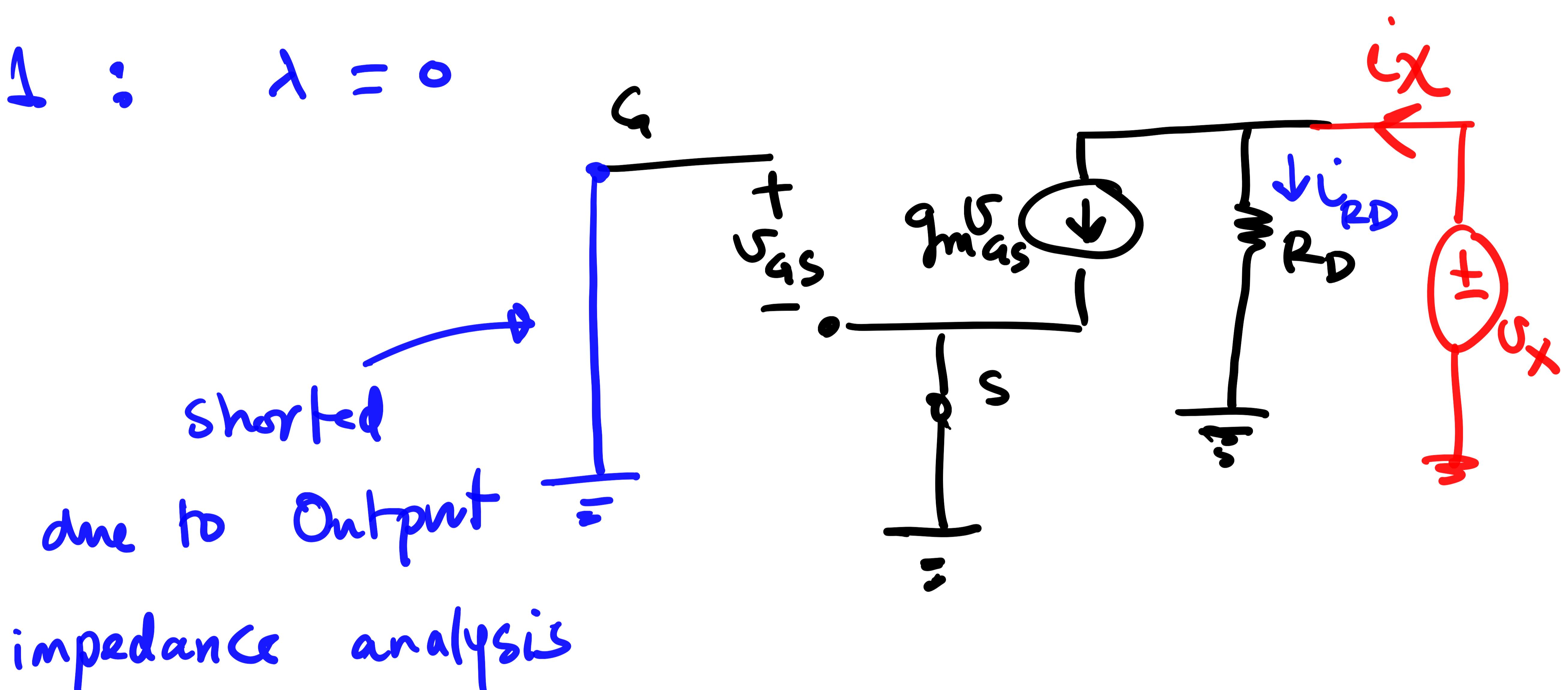
$$R_{in} = \infty$$

for a core CS stage.

## \* Output Impedance :-



case 1 :  $\lambda = 0$



$$R_{out} = \frac{U_x}{i_x} \Rightarrow i_x = i_{RD} + g_m \cdot U_{GS}$$

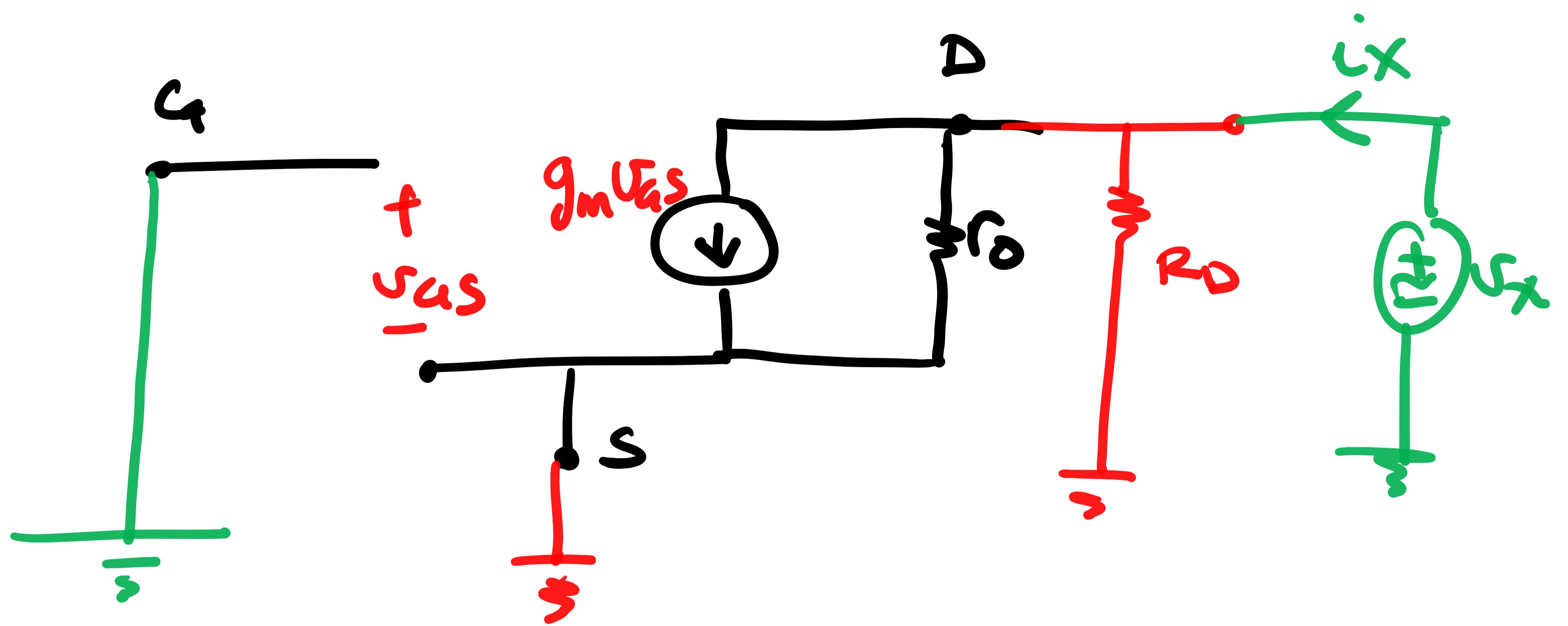
notice that  $U_{GS}$  is trapped between 2 ground nodes hence  $U_{GS} = 0 \rightarrow g_m U_{GS} = 0$

$$i_x = i_{RD} \Rightarrow i_{RD} = \frac{U_x}{R_D}$$

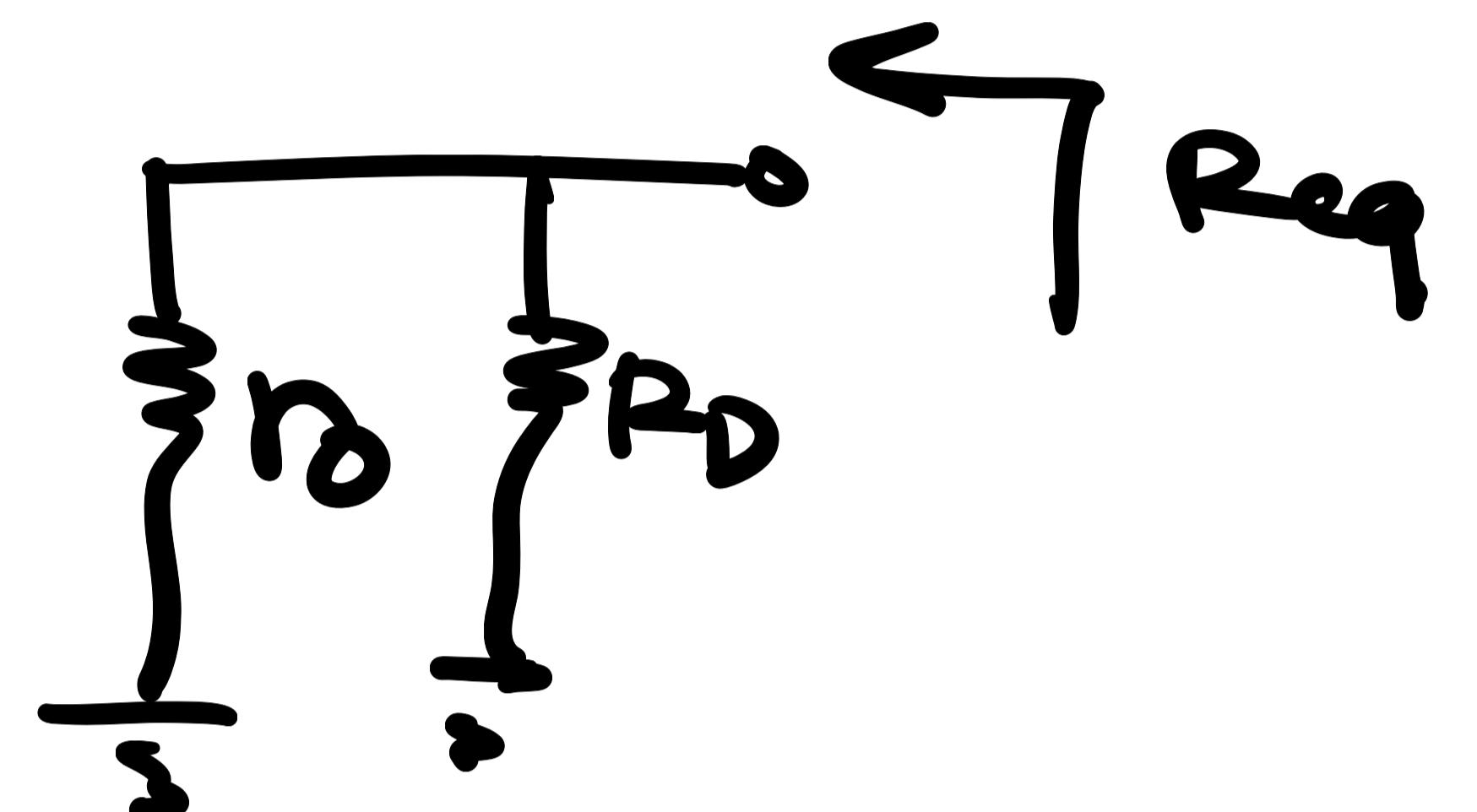
$$\Rightarrow i_x = \frac{U_x}{R_D} \Rightarrow \frac{U_x}{i_x} = R_D$$

$R_{out} = R_D$  if  $\lambda = 0$

\* Case # 2 :  $\lambda \neq 0$

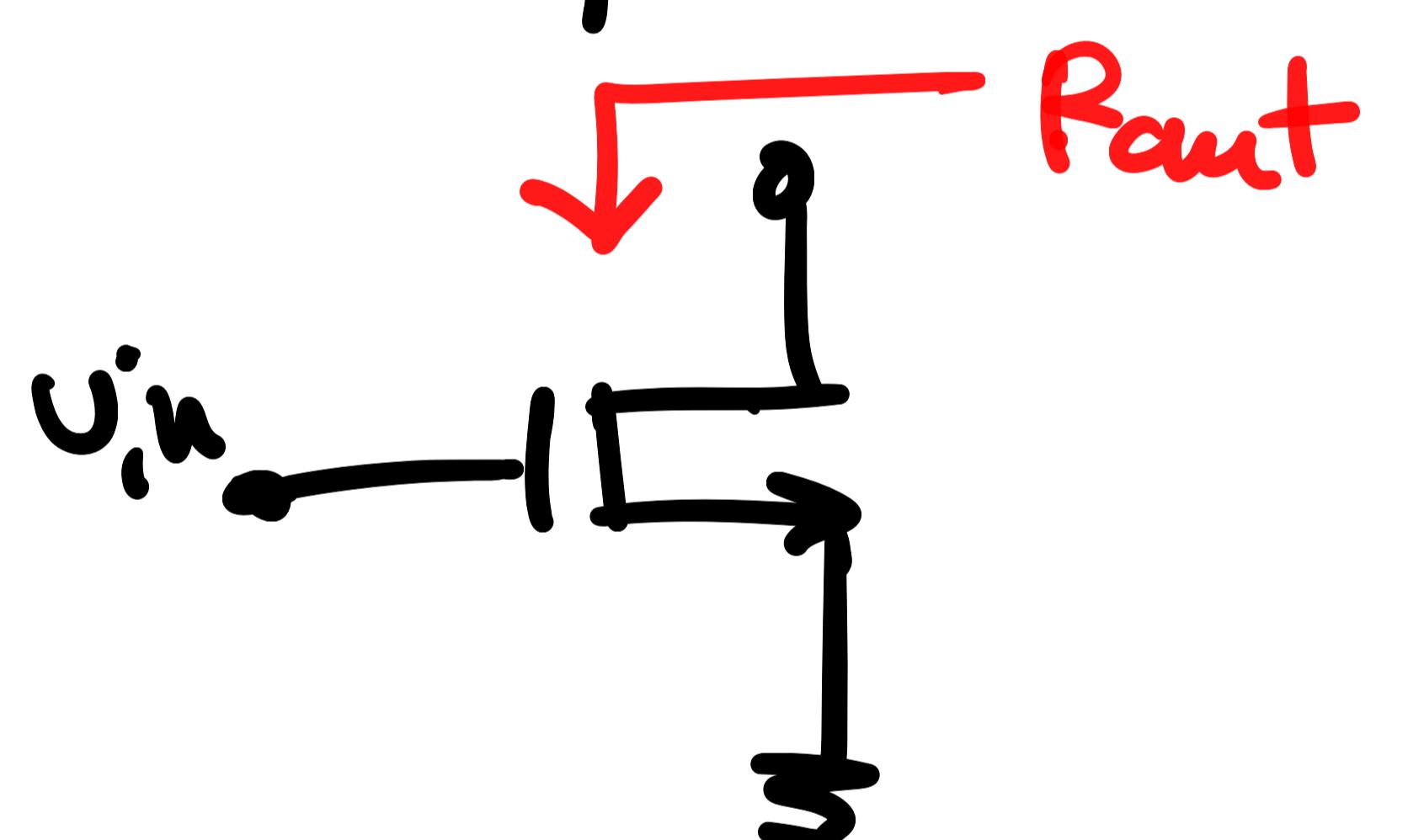


$$\rightarrow V_{GS} = 0 \Rightarrow g_m V_{GS} = 0 \Rightarrow$$



$$R_{out} = R_D \parallel r_o$$

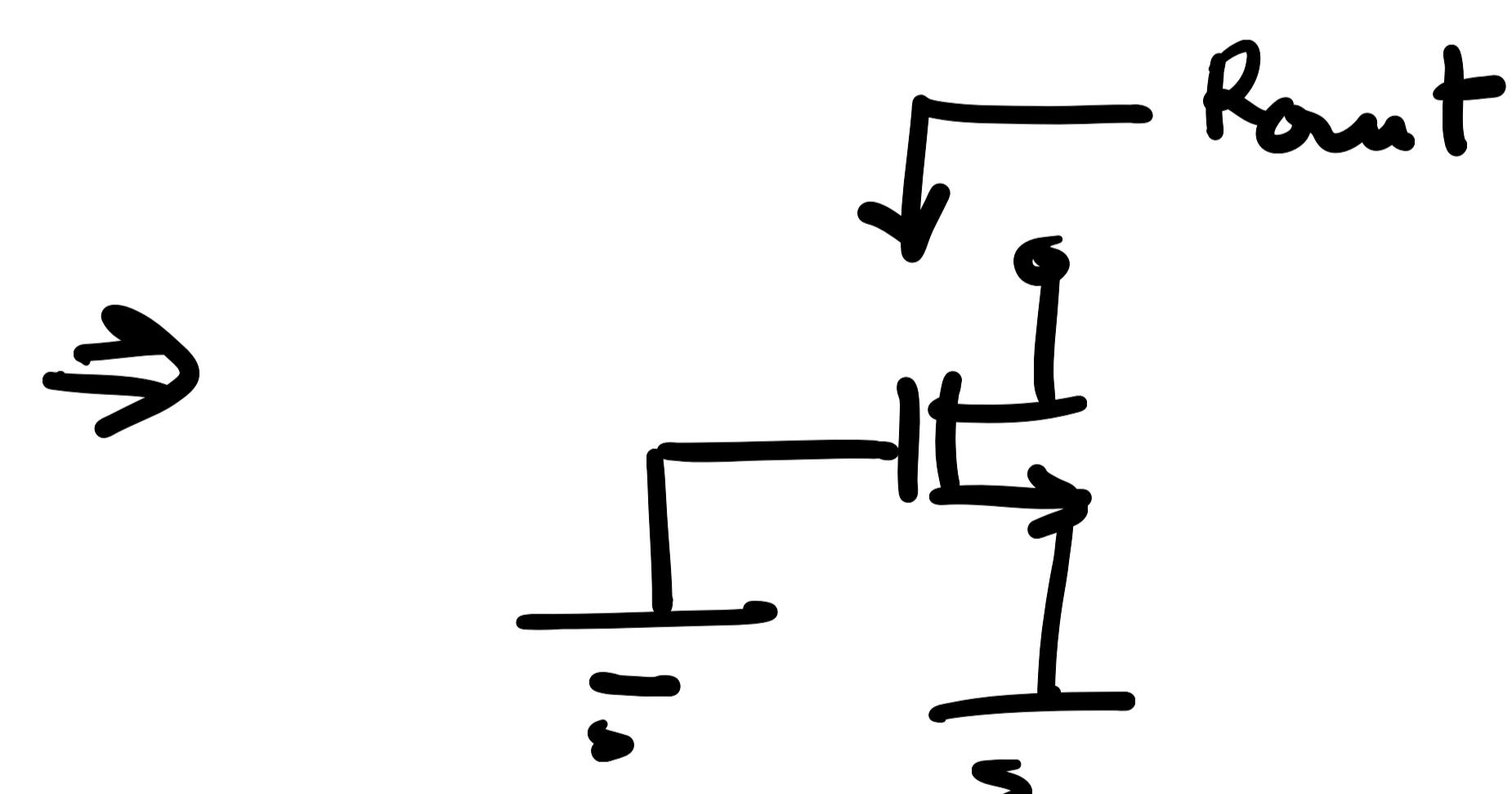
→ find  $R_{out}$  for this device



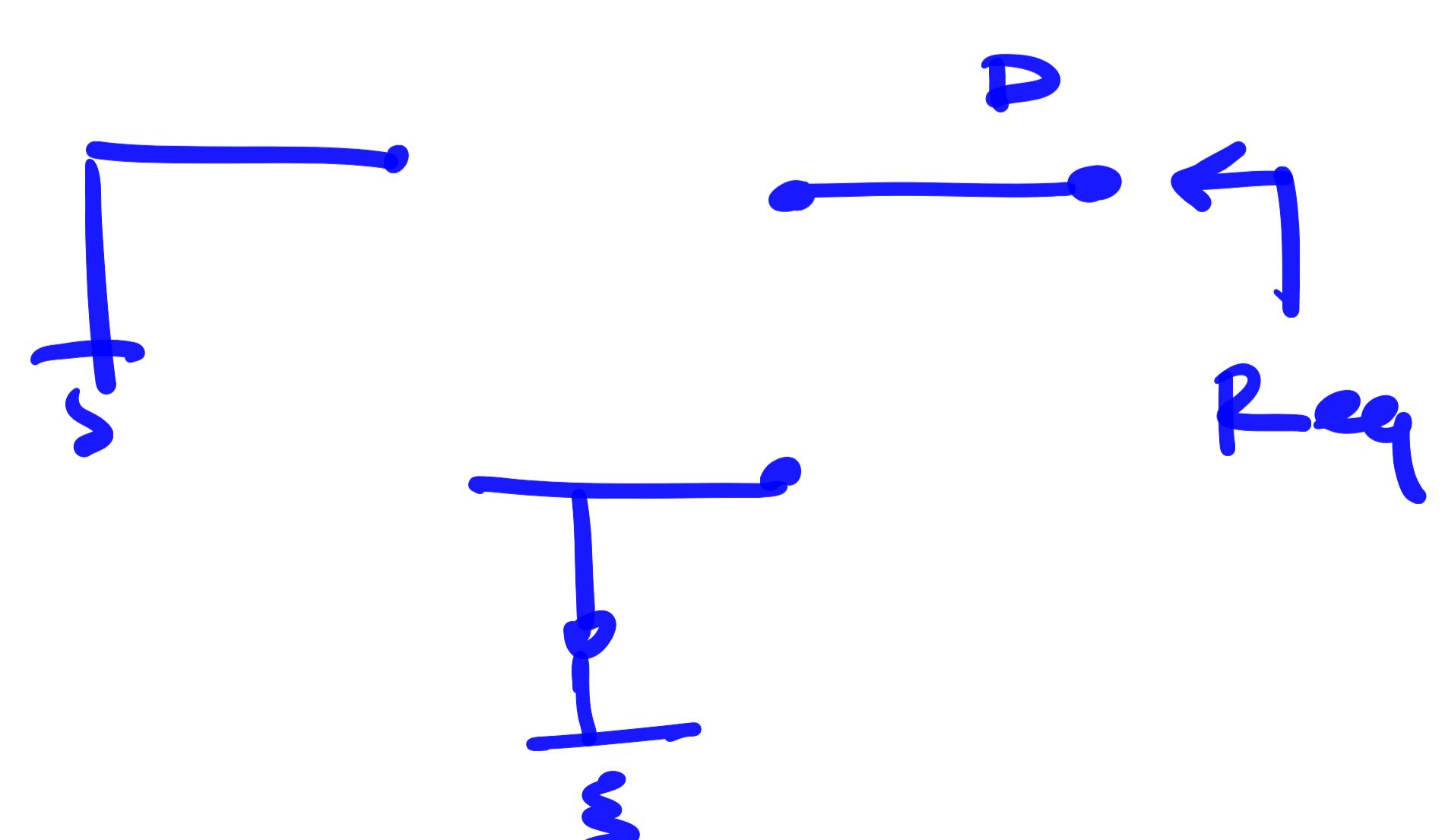
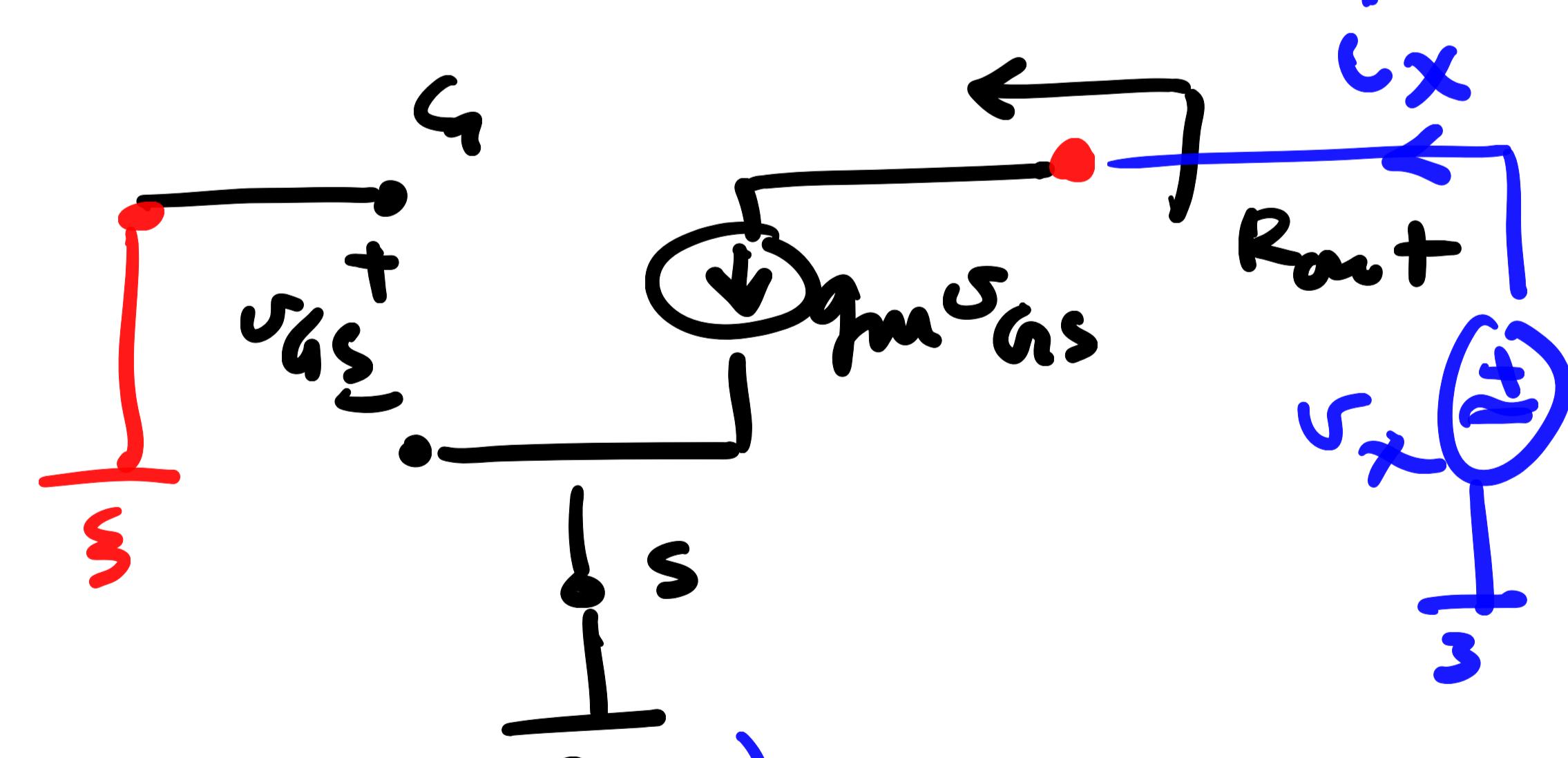
$$\lambda = 0 ?$$

$$\lambda \neq 0 ?$$

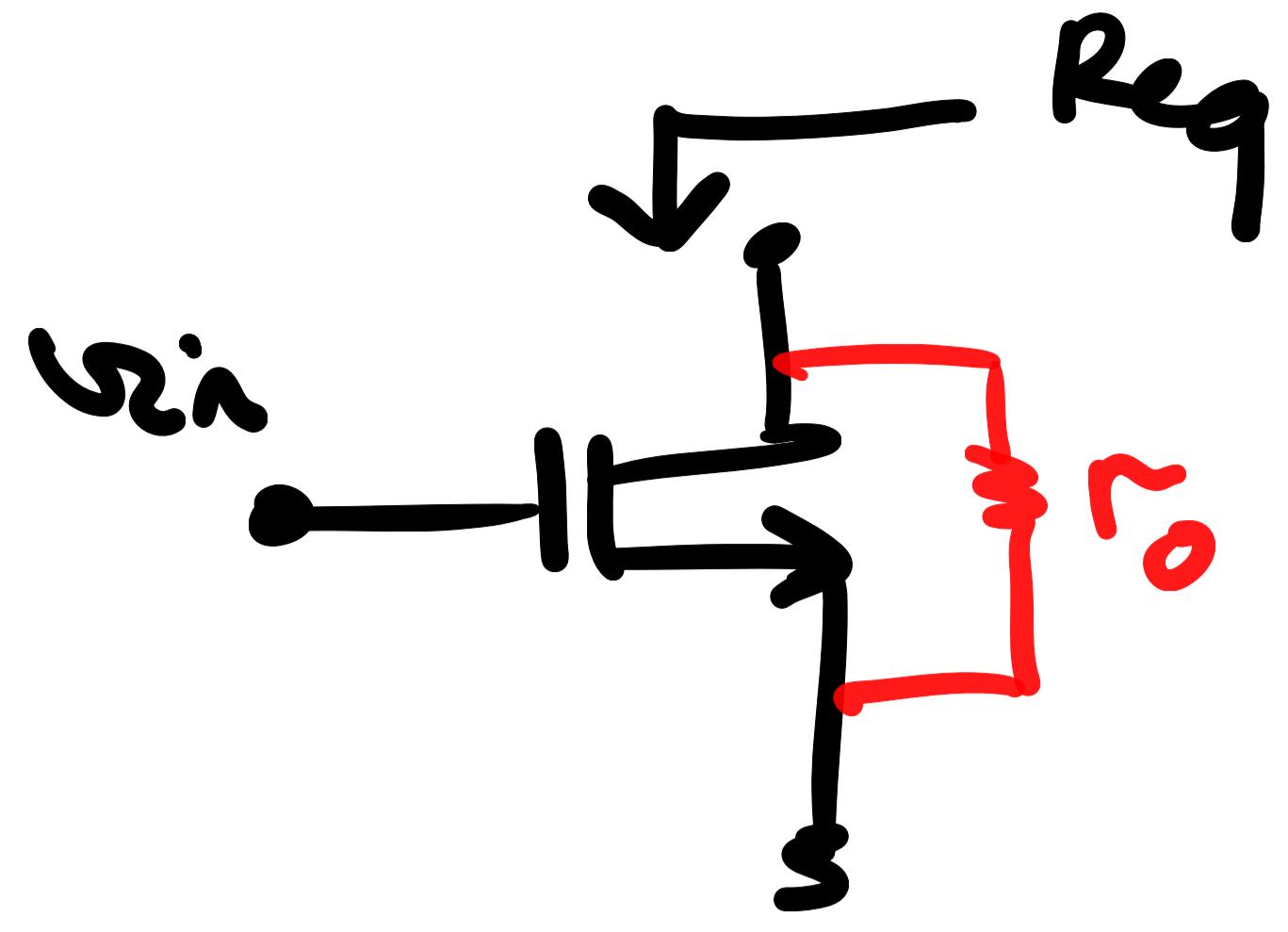
$$\lambda = 0$$



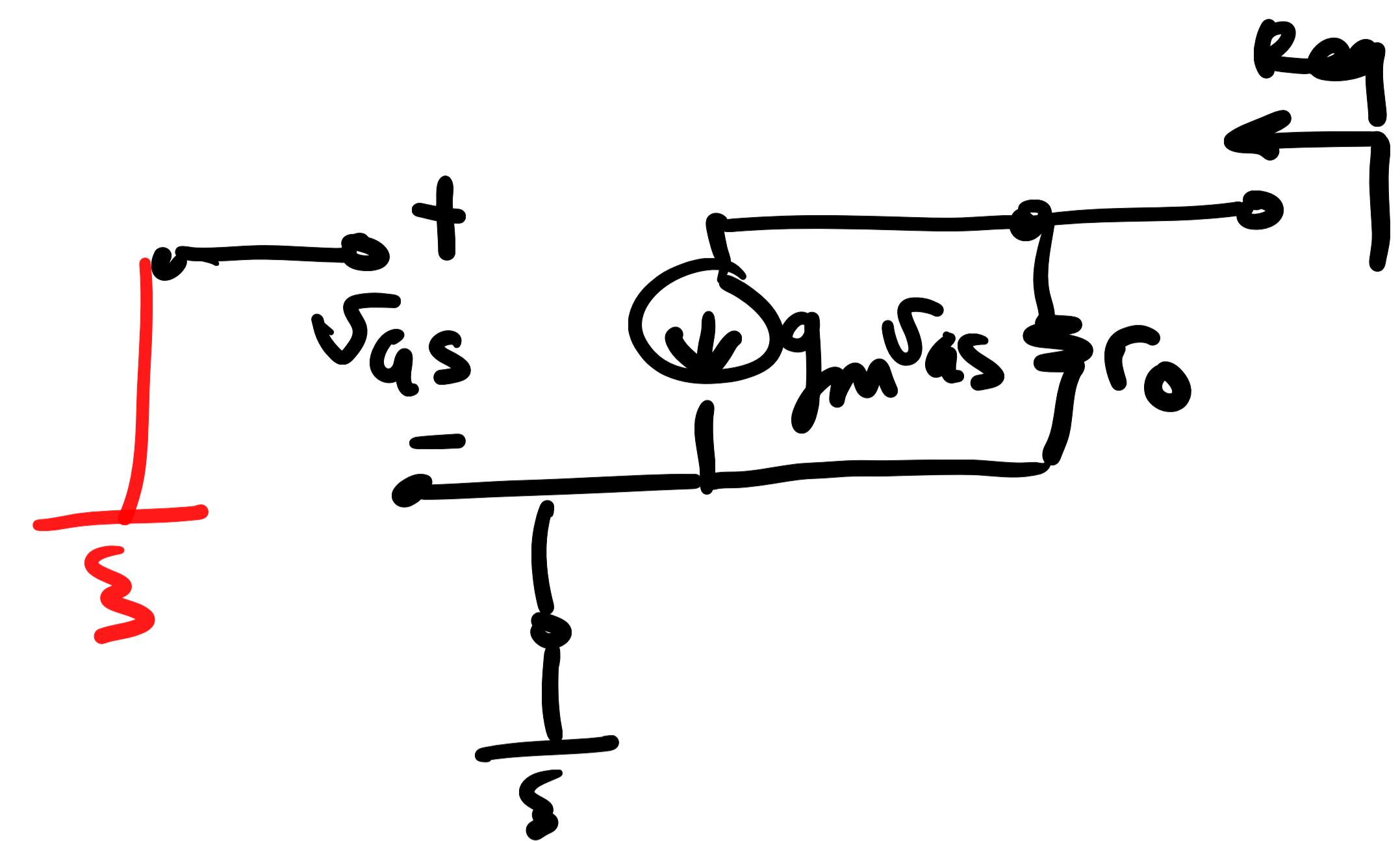
$$R_{req} = \infty$$



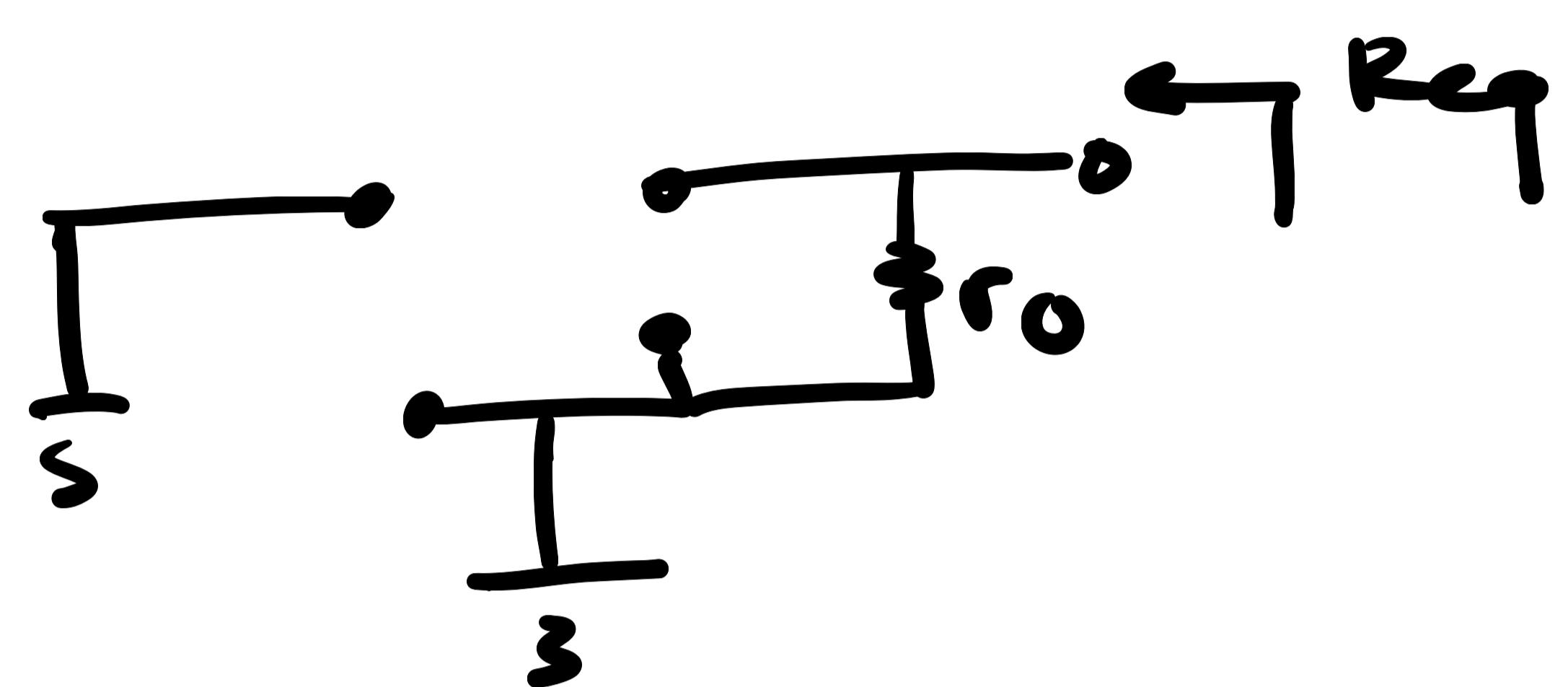
Case 1 & 2  $\lambda \neq 0$



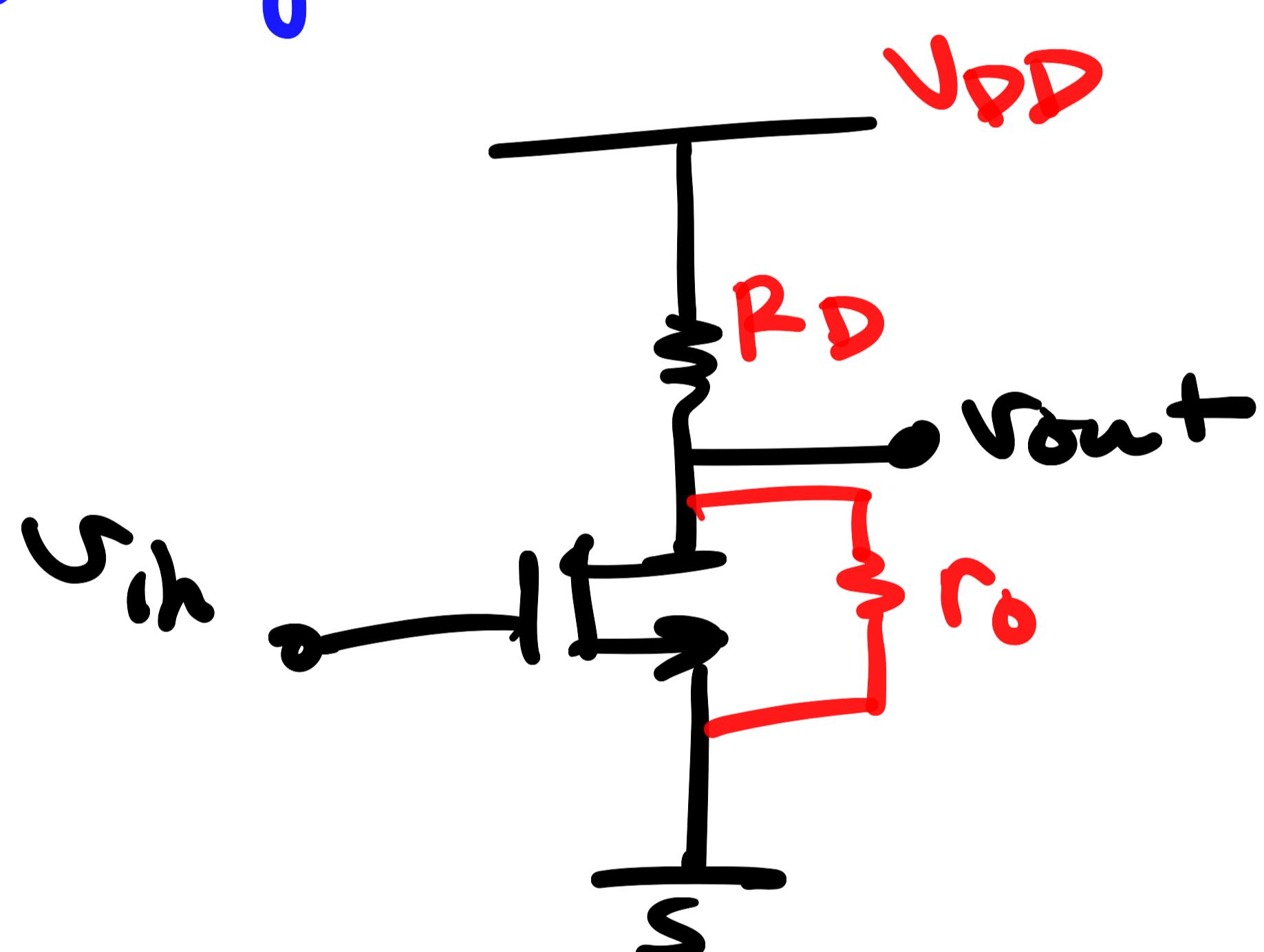
$$Req = \sqrt{r_o}$$



$$v_{GS} \approx 0$$

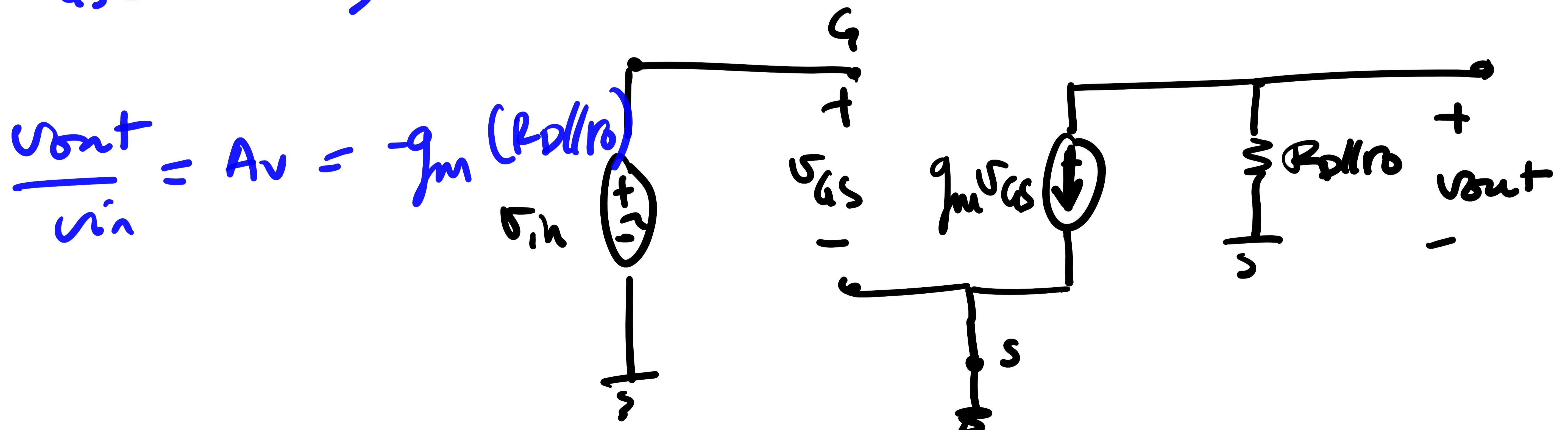


\* CS stage gain analysis if  $\lambda \neq 0$



$$v_{out} = -g_m \cdot v_{AS} (R_D || r_o)$$

$$v_{AS} = v_{in} \Rightarrow$$

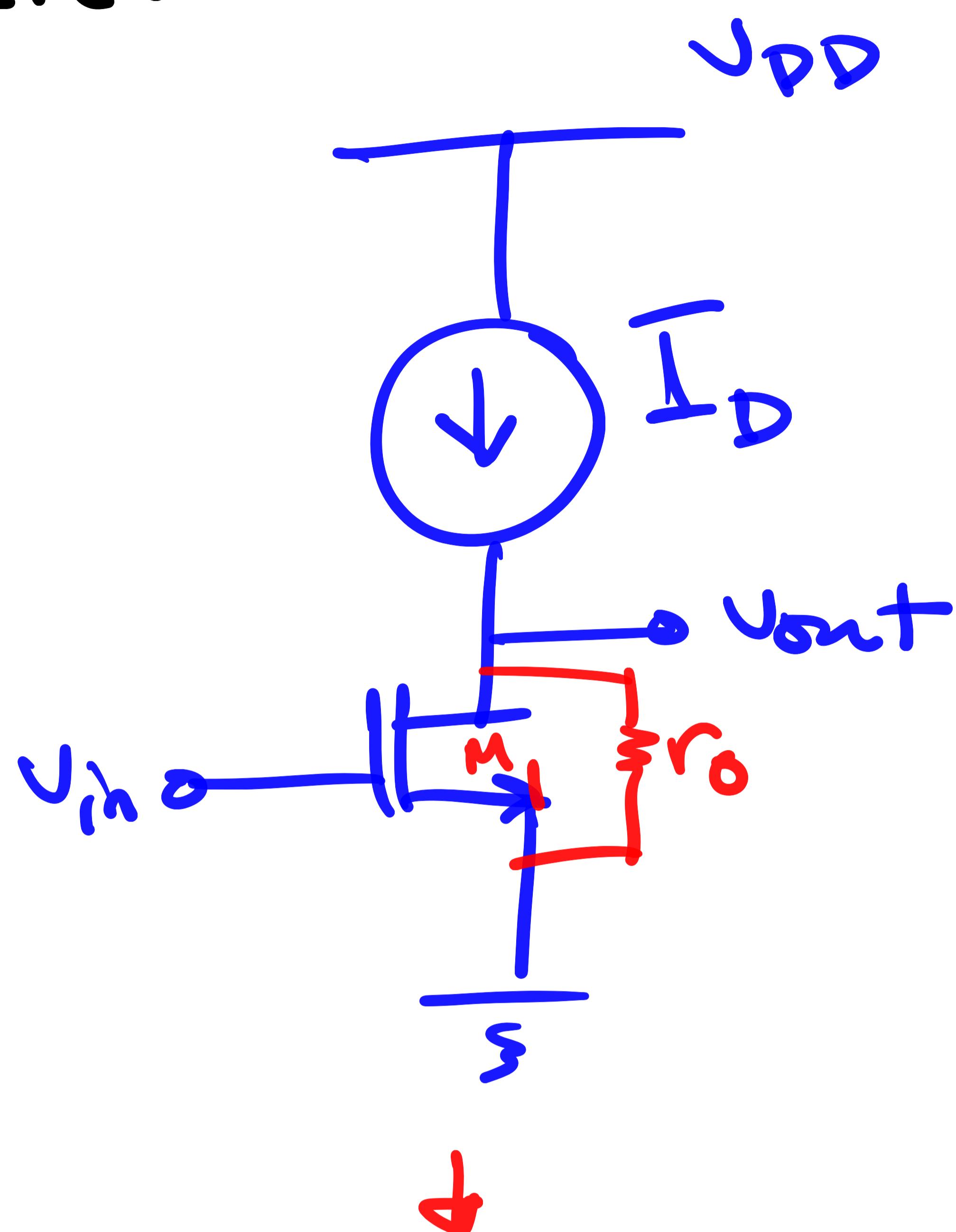


Ex: Assume  $M_1$  operates in the Sat. region, find the voltage gain and study the effect of channel modulation:

→ assuming an  $R_D$

$A_v$  should be

$$-g_m (R_D/r_o)$$

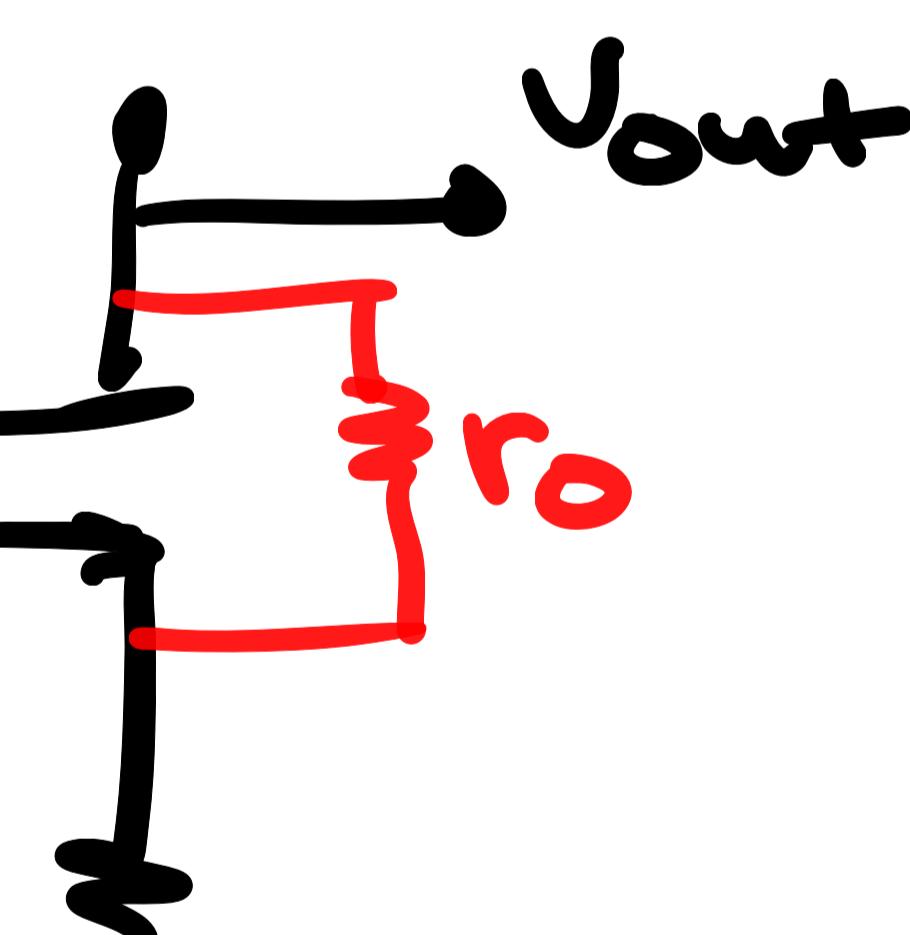


To analyze the gain we apply small-signal analysis

Since current source is open then its treated as an  $R_D = \infty$

$$\frac{1}{s}$$

$$A_v = -g_m (\infty / r_o)$$



$$A_v = -g_m \cdot r_o \rightarrow \text{intrinsic gain.}$$

$$|A_v| = g_m r_o , \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \cdot \frac{1}{\lambda I_D}$$

remember that  $\lambda \propto \frac{1}{L}$

$$|A_v| \propto \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \cdot \frac{1}{\sqrt{\lambda^2 I_D^2}}$$

$$|Av| \propto \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \cdot \frac{1}{\sqrt{\frac{1}{L^2} \cdot I_D^2}}$$

$$|Av| \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}$$

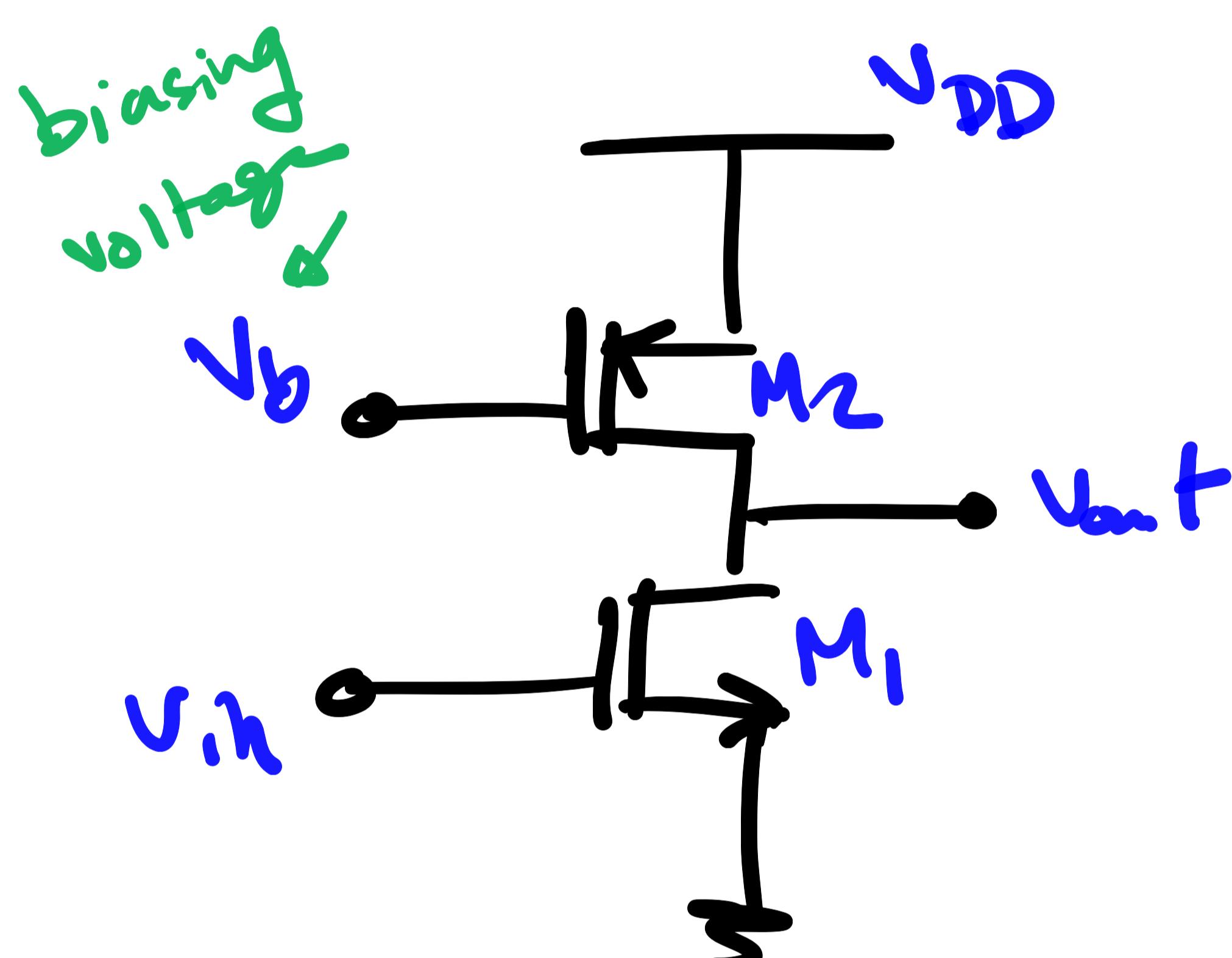
\* CS stage with a current source load (active load):

$$\lambda \neq 0$$

To find the gain

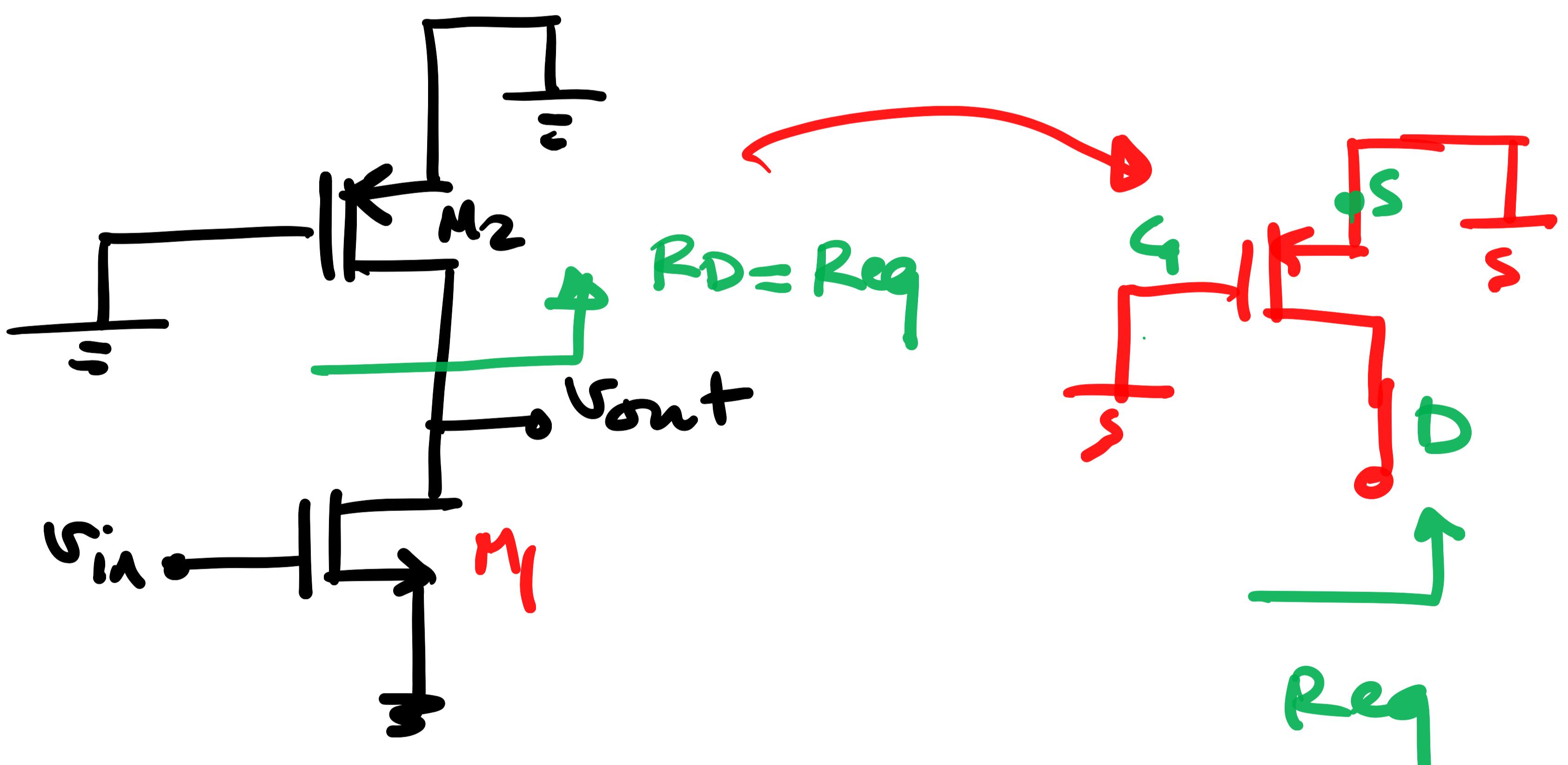
we will perform

small signal analysis.



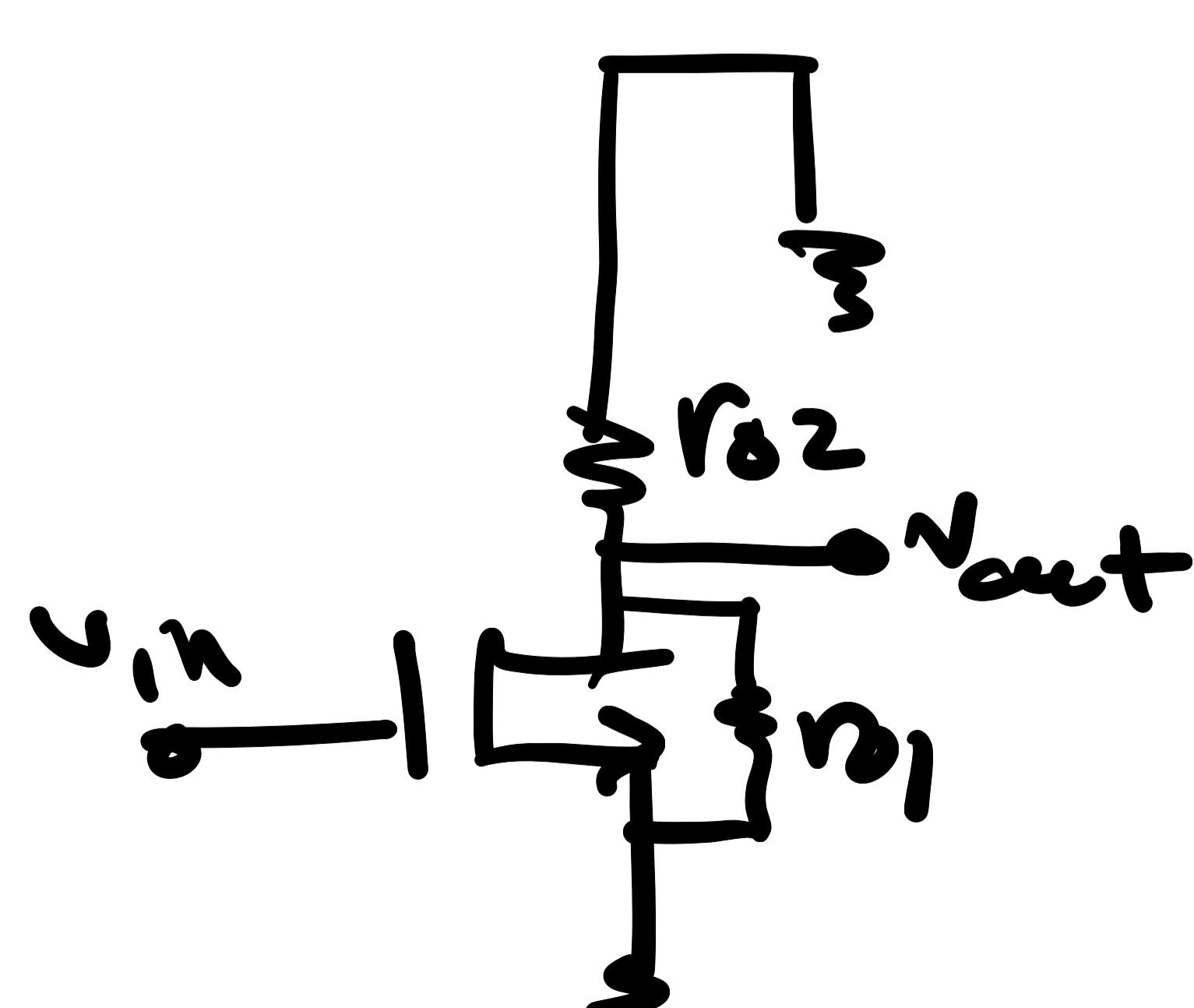
$$\text{Since } \lambda \neq 0$$

$$Av = -g_{m_1} (r_o / R_D)$$



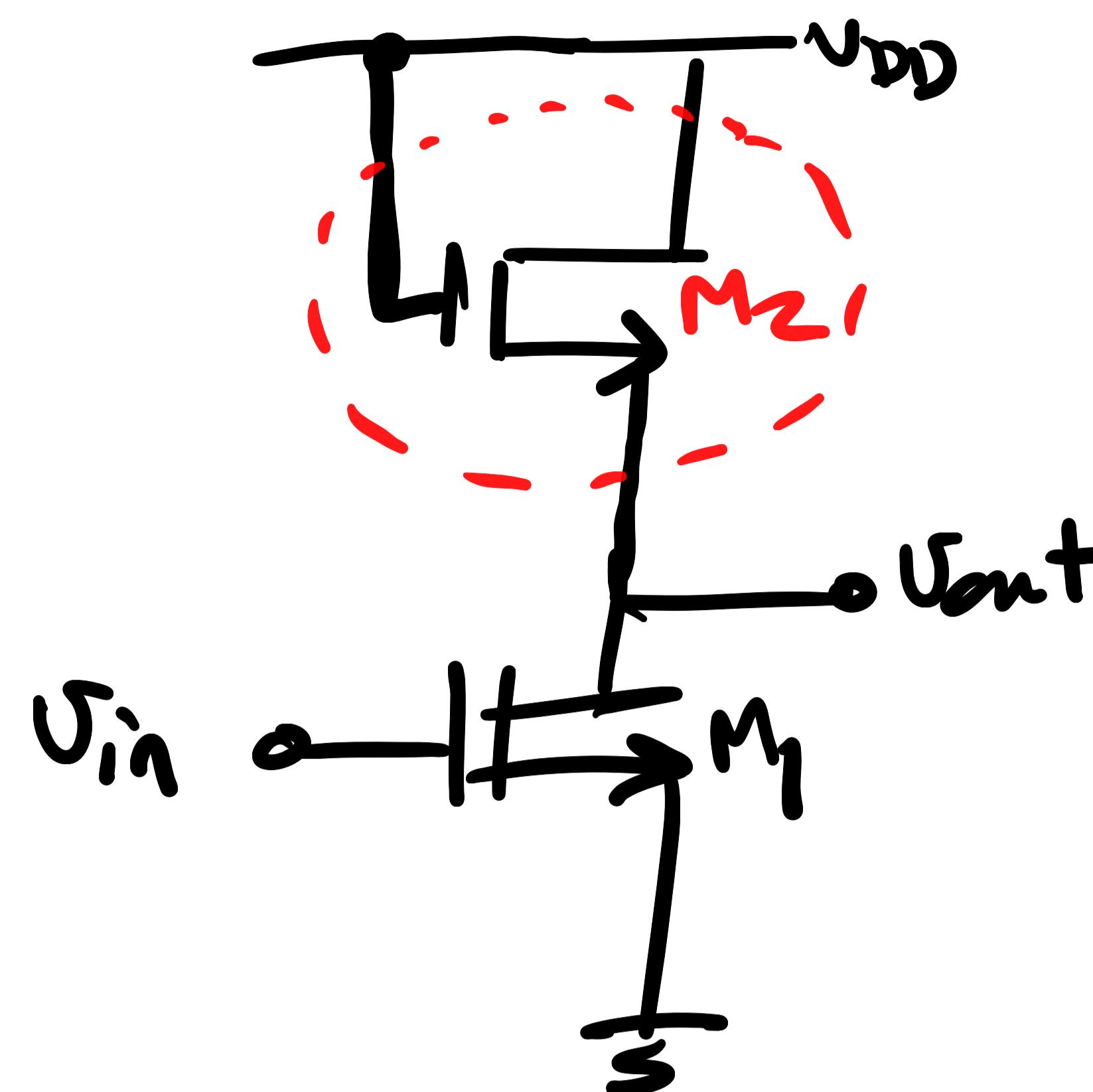
$$Av = -g_{m_1} (r_o / r_{o2})$$

$$Req = r_{o2}$$



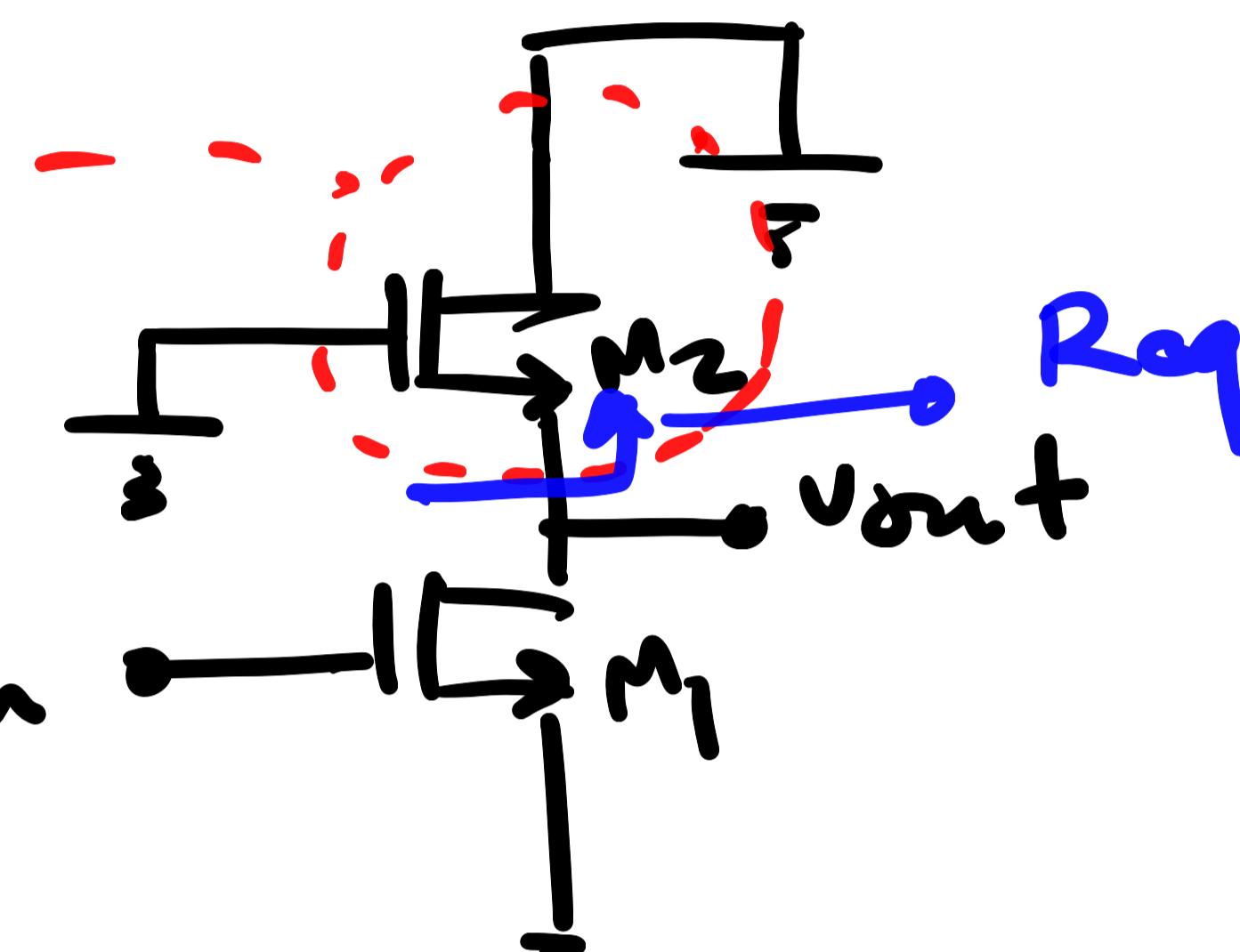
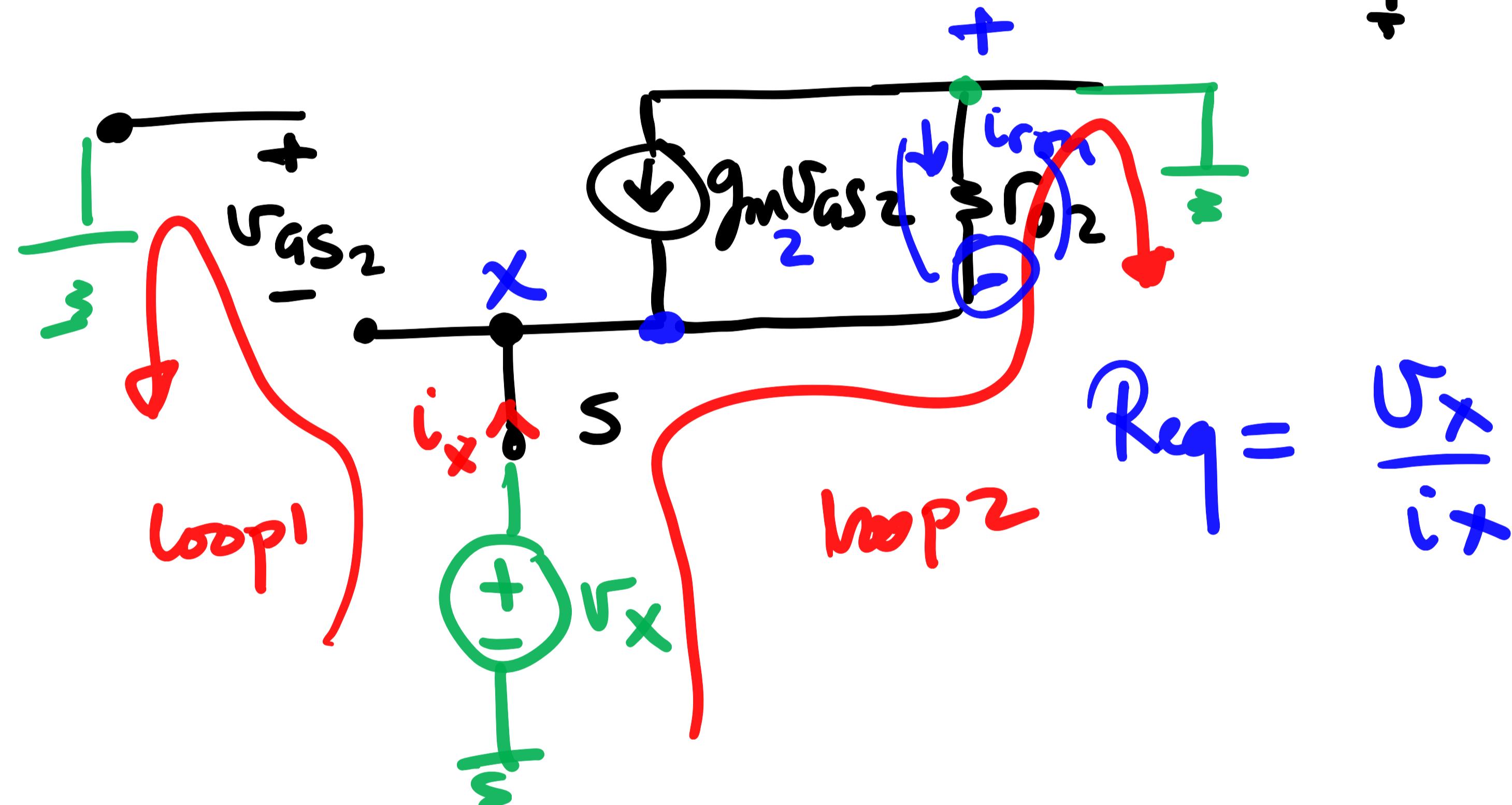
\* CS with diode connected Loads :-

Calculate the gain ?



→ small signal analysis

\* To derive Req :-



$$Req = \frac{V_x}{i_x}$$

applying KCL @ node X :

\* Applying KVL @ loop 1 :

$$i_x + g_{m2}V_{GS2} + i_{rD2} = 0$$

$$-V_x - V_{GS2} = 0$$

$$\boxed{V_{GS2} = -V_x}$$

Applying KVL @ loop 2 :

$$-V_x + (-i_{rD2} \cdot r_{D2}) = 0$$

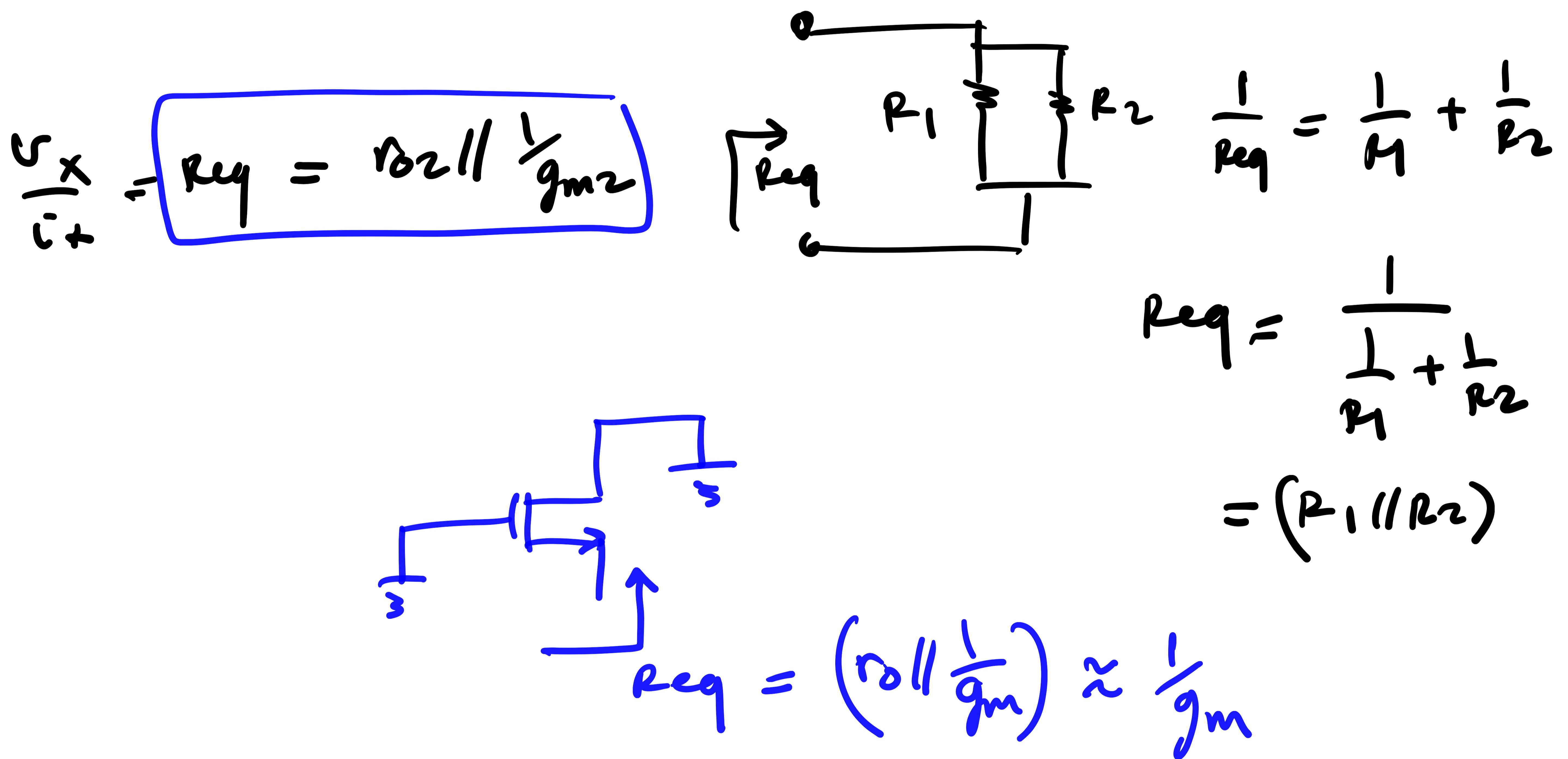
$$\Rightarrow \boxed{i_{rD2} = \frac{-V_x}{r_{D2}}}$$

→ going back to the KCL analysis :

$$i_x + g_{m2}(-v_x) + \left(-\frac{v_x}{r_{o2}}\right) = 0$$

$$i_x = \left(g_{m2} + \frac{1}{r_{o2}}\right) \cdot v_x$$

$$\frac{v_x}{i_x} = \frac{1}{\frac{1}{r_{o2}} + g_{m2}} = \left(\frac{1}{r_{o2}}\right) + \left(\frac{1}{g_{m2}}\right)$$



$\Rightarrow$  going back to the gain analysis :-

$$\Rightarrow A_v = -g_{m1} \left(r_{o1} \parallel \frac{1}{g_{m2}}\right)$$

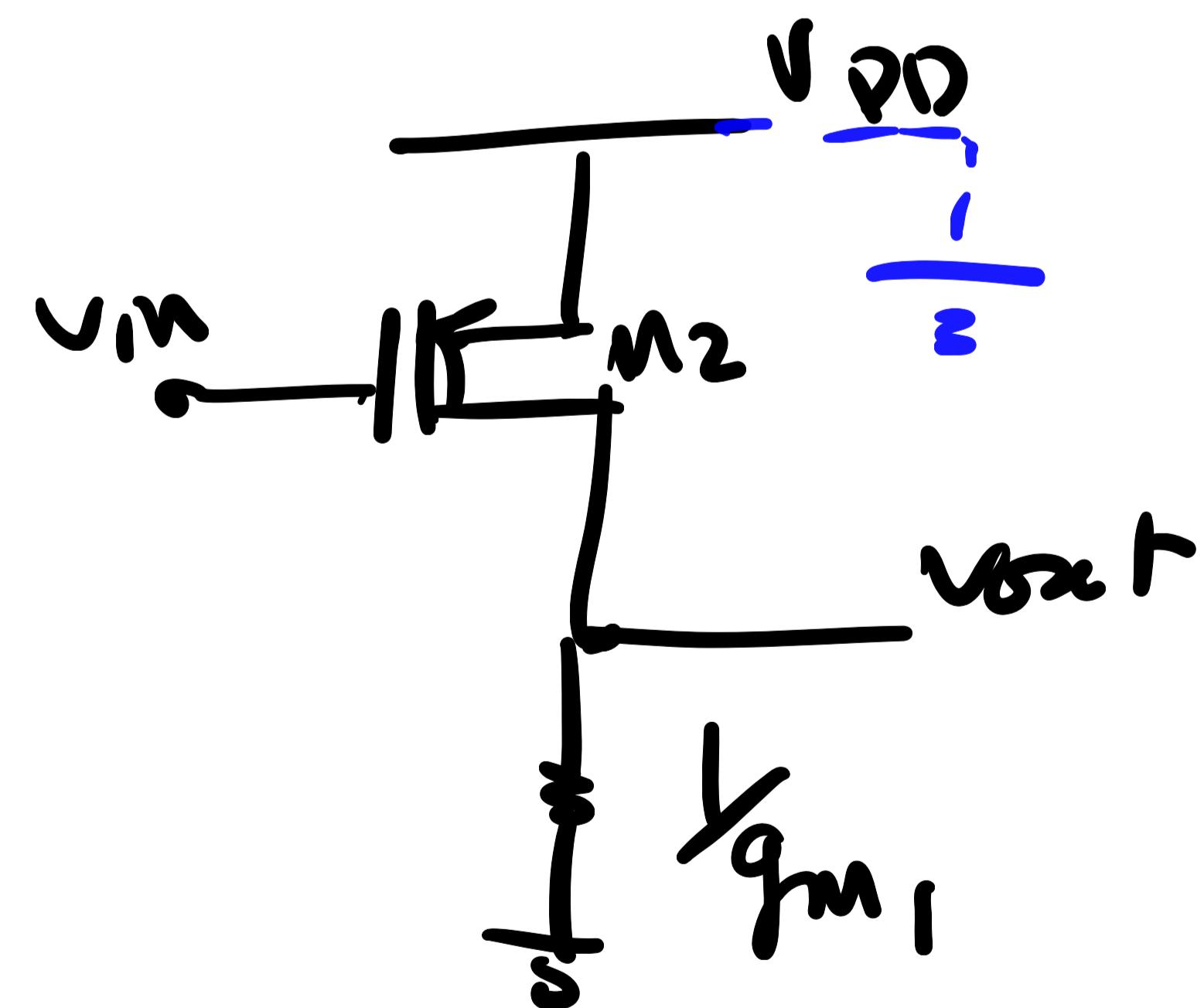
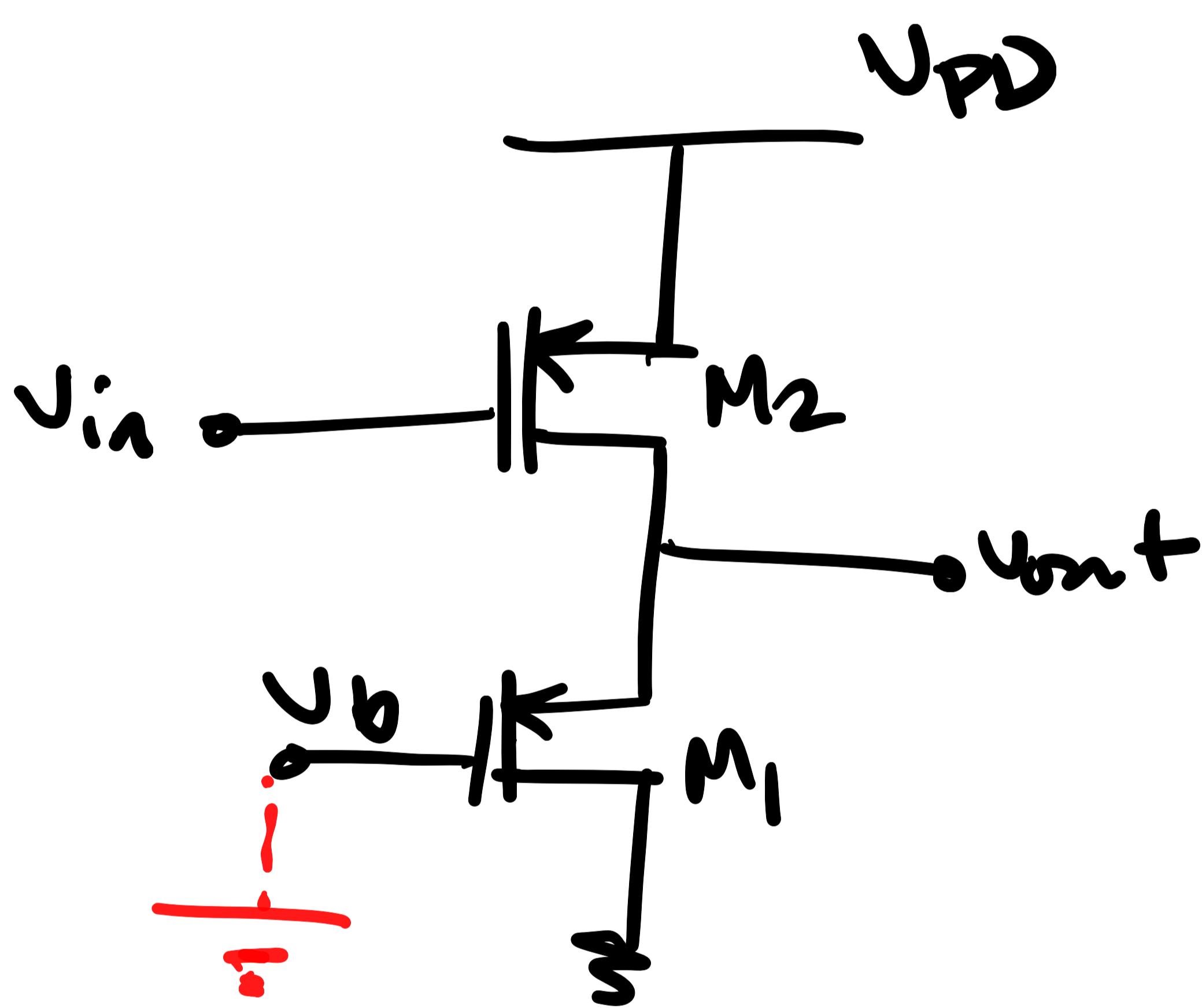
$$A_v \approx -\frac{g_{m1}}{g_{m2}} \Rightarrow |A_v| = \frac{g_{m1}}{g_{m2}} = \frac{\sqrt{2\mu_n C_o X \frac{W_1}{L_1} I_{D1}}}{\sqrt{2\mu_n C_o X \frac{W_2}{L_2} \cdot I_{D2}}}$$

$$|A_V| = \sqrt{\frac{(w/L)_1}{(w/L)_2}} \rightarrow \text{the advantage of such device is the ability to manipulate the gain } A_V \text{ using the physical dimensions of Transistors M}_1 \text{ and M}_2.$$

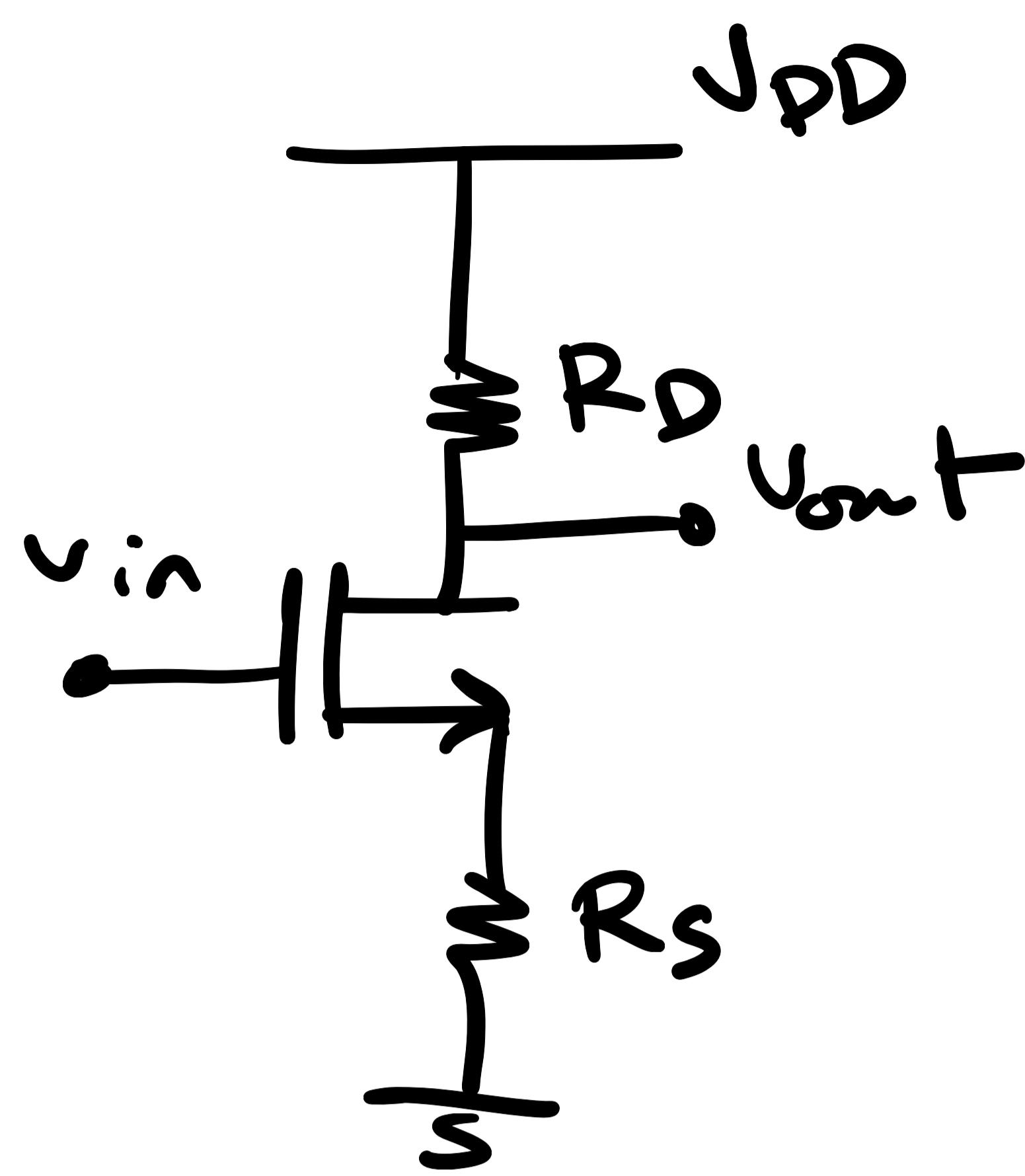
Ex: Determine the voltage gain for this cct.

$$A_V = -g_{m2} (r_{o2} \parallel \frac{1}{g_{m1}})$$

$$A_V \approx -\frac{g_{m2}}{g_{m1}}$$



\* CS stage with degeneration :-



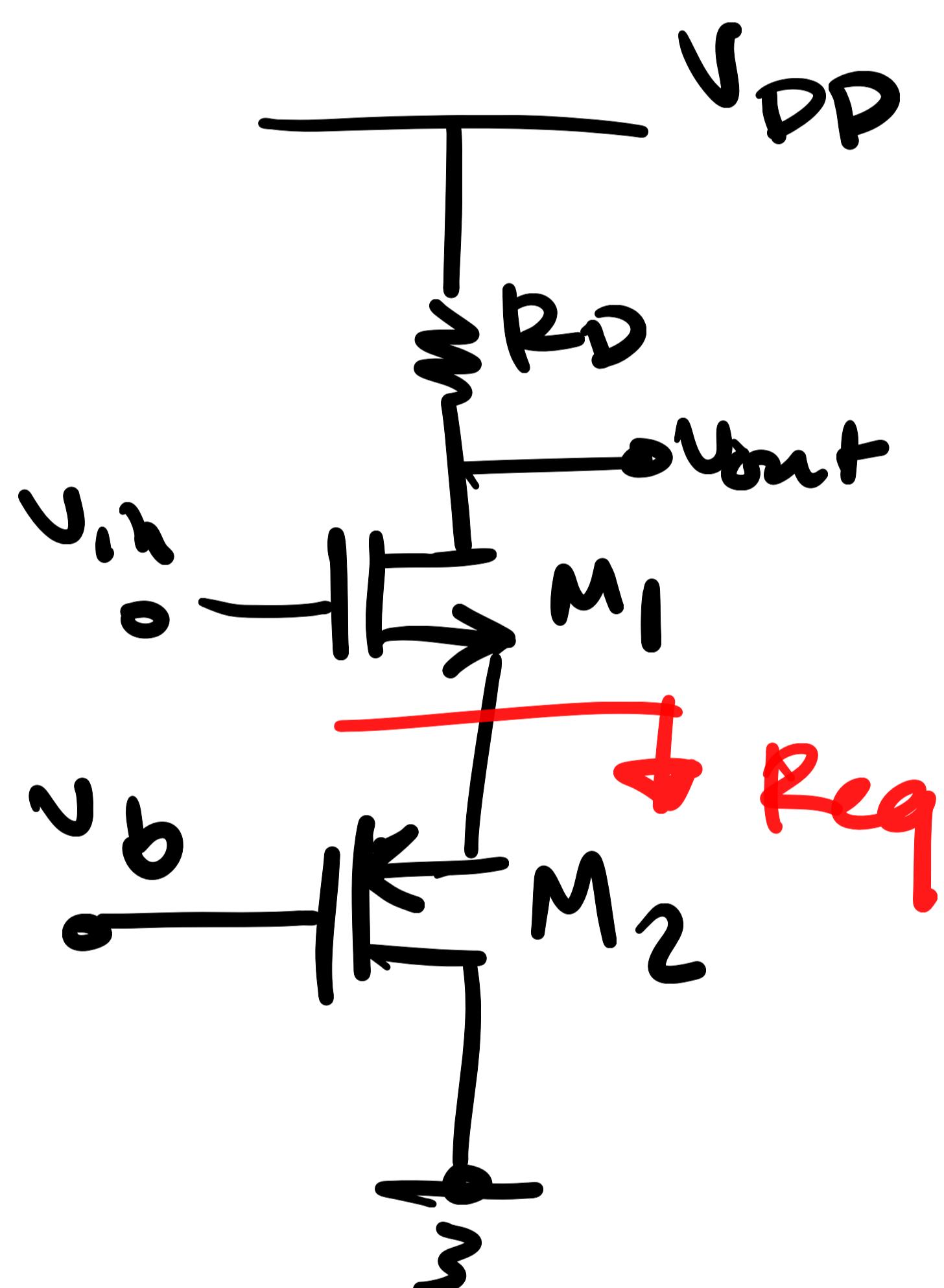
\* AV analysis :-

$$AV = \frac{-R_D}{g_m + R_s}$$

Ex : Compute the voltage gain for this stage,  $\lambda = 0$ :

This is a CS stage with degeneration

$$AV = \frac{-R_D}{g_{m1} + R_{eq}}$$



$$\Rightarrow R_{eq} = g_{mu_2}$$

$$AV = \frac{-R_D}{g_{m1} + g_{m2}}$$