cadence®

Allegro® X User Guide: Working with RF PCB

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1

Getting Started

- Introduction
- The RF PCB Design Flow
- System File Changes
- RF Properties
- The RF PCB User Interface
- RF Board Setup
- RF Global Variable Initialization

Introduction

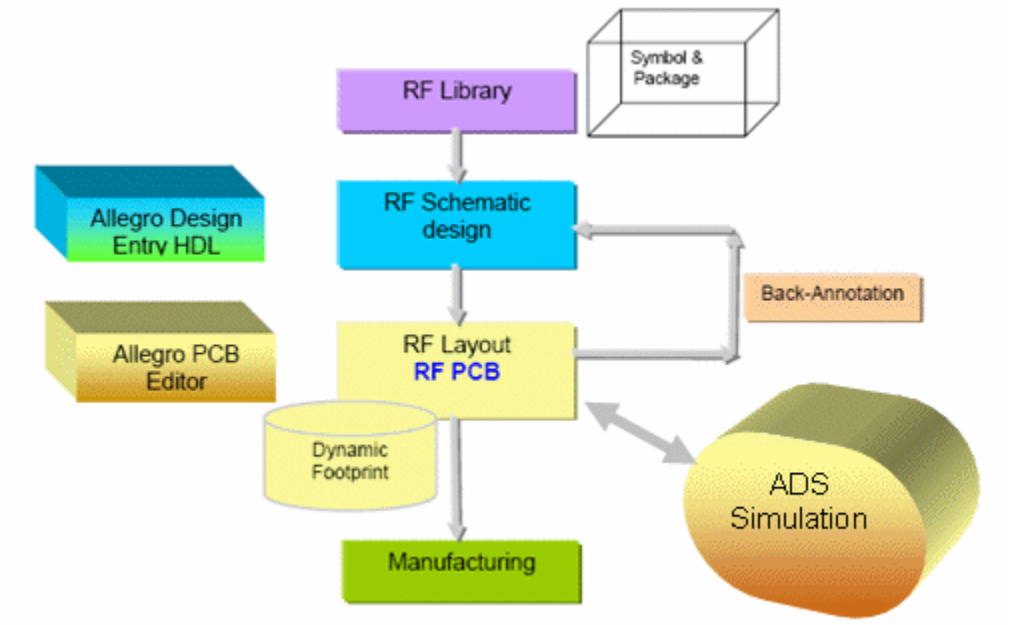
Allegro® RF PCB provides you with a unified design solution for complex mixed-signal projects. From schematic, to layout, to manufacturing, a total front-to-back design flow helps you streamline your entire RF design process. You lay out RF design areas on your board using discrete functions for component creation and placement as well as routing. Once complete, you can export these RF layouts to ADS for simulation and parameter optimization. The results of the ADS simulation are then imported back into Allegro to update the layout, and from there can be back-annotated to the schematic.

RF PCB features its own flexible shape editor (FSE) that works in conjunction with the existing Allegro shape editor to address the specific requirements of RF design. FSE enhances the existing Allegro shape editing functions by providing powerful functions for copper editing, adjustment, and resizing. Also provided are utilities such as transmission line calculators and an extensive library of RF schematic symbols that greatly simplify the process of RF component creation and modification.

The RF PCB Design Flow

The RF PCB design flow is a series of tasks that you perform using Allegro Design Entry HDL, Allegro PCB Editor, as well as ADS. These tasks are grouped into phases as illustrated in Figure 1-1.

Figure 1-1 RF PCB Design Flow



RF PCB provides a library of parameterized components (PCELL) that you use in your RF schematic designs. You can change component parameters and shapes within your RF layout or from within ADS after simulation. The changes you make are synchronized between these two environments and also between the layout and schematic - front to back or back to front.

Design Flow Use Models

There are actually several supported flow use models for Allegro RF / mixed signal design. These use models are described in Table 1-1.

Note: Cadence recommends that you use flow model 1.

Table 1-1 Supported Use Models

Flow Model	Logic design in . . .	Physical design in . . .	RF Simulation in . . .	Combine and adjust in . . .
1	Design Entry HDL (RF and non-RF)	PCB Editor (RF and non-RF)	ADS	N/A
2	Design Entry HDL (non-RF) - or - ADS (RF)	PCB Editor (RF and non-RF)	ADS	N/A
3	3rd Party (non-RF) No RF	PCB Editor	ADS	N/A
4	Design Entry HDL (non-RF) - or - ADS (RF)	ADS	ADS	PCB Editor

RF Library Generation

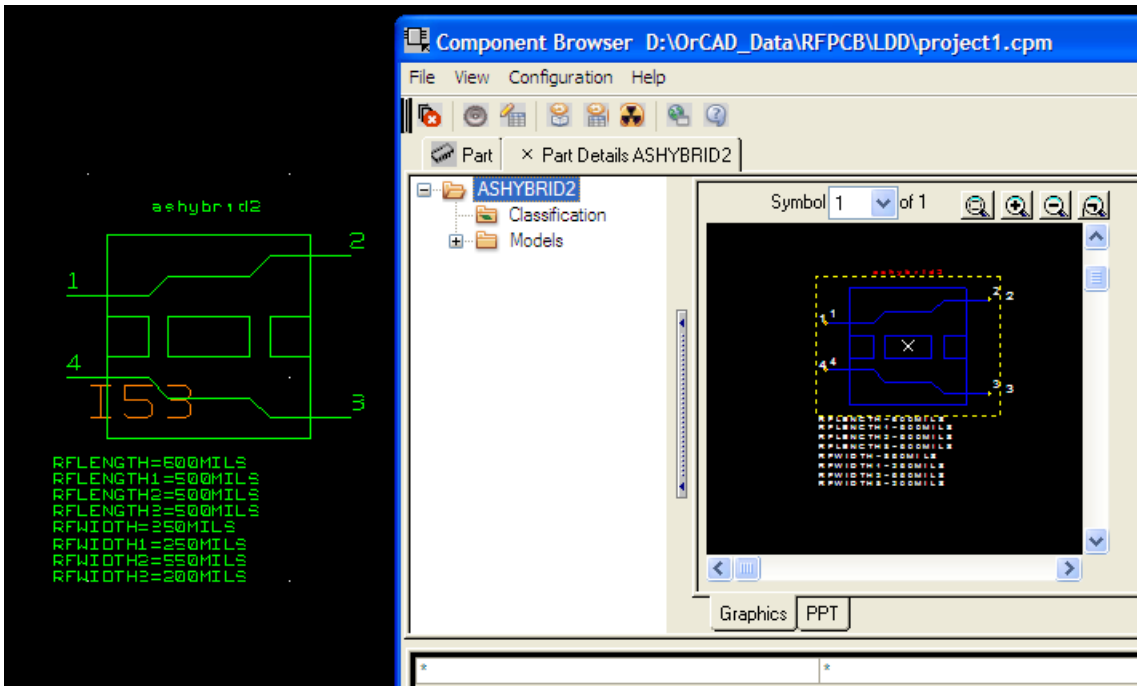
The RF library `rf_comp_lib` is incorporated into your Allegro library database after the RF PCB software is installed. It contains over two hundred schematic symbols that represent most RF component types. Each schematic symbol has a corresponding package symbol that is included in the library for reference.

For example, all MLIN components are represented using one master schematic symbol in the RF library. You use this symbol by loading an instance of it into your schematic within Design Entry HDL, and then change the instance parameters to suit your design requirements. The actual footprint of the component is created dynamically in the RF layout according to the parameter values you set in the schematic. For descriptions of RF components currently supported, refer to the *Allegro RF PCB Library Reference*.

RF Schematic Design

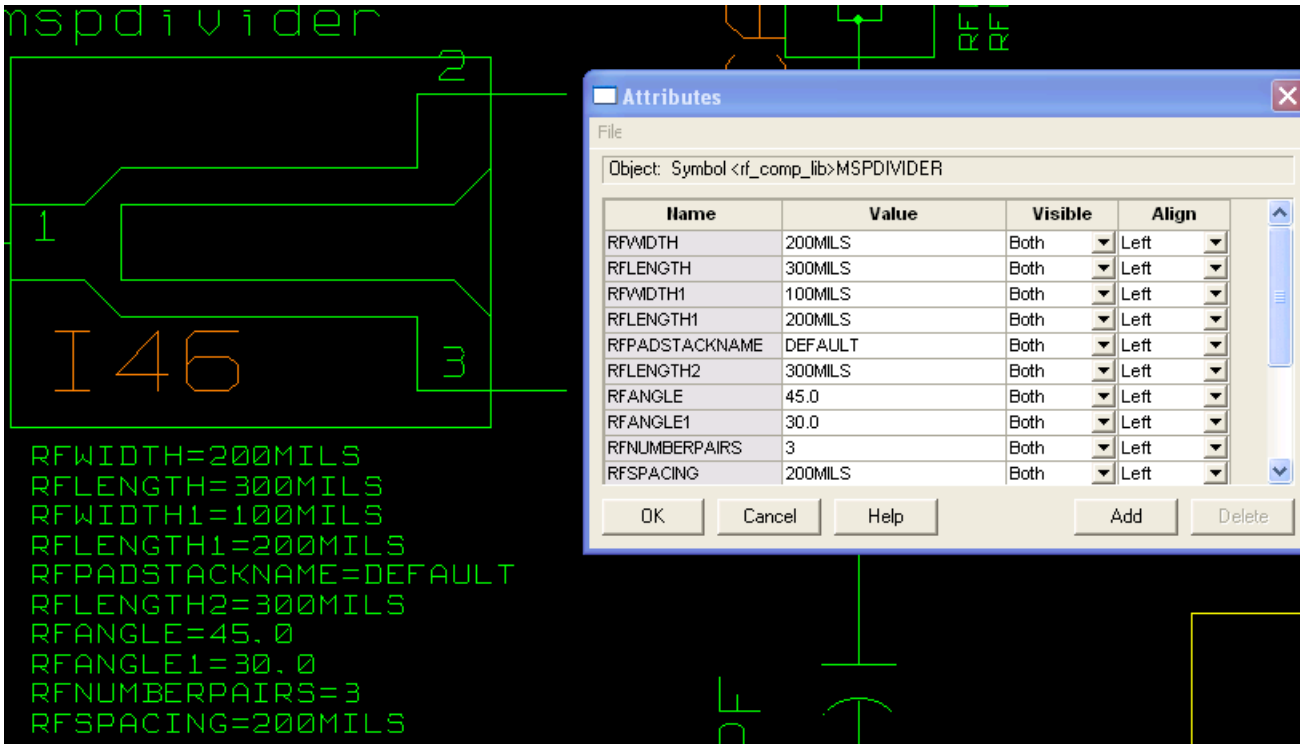
Use Design Entry HDL to create your schematic by placing RF components, entering parameters, connecting RF pins, and adding signal names. The RF components are loaded using the Component Browser shown in Figure 1-2.

Figure 1-2 Loading Components in Design Entry HDL



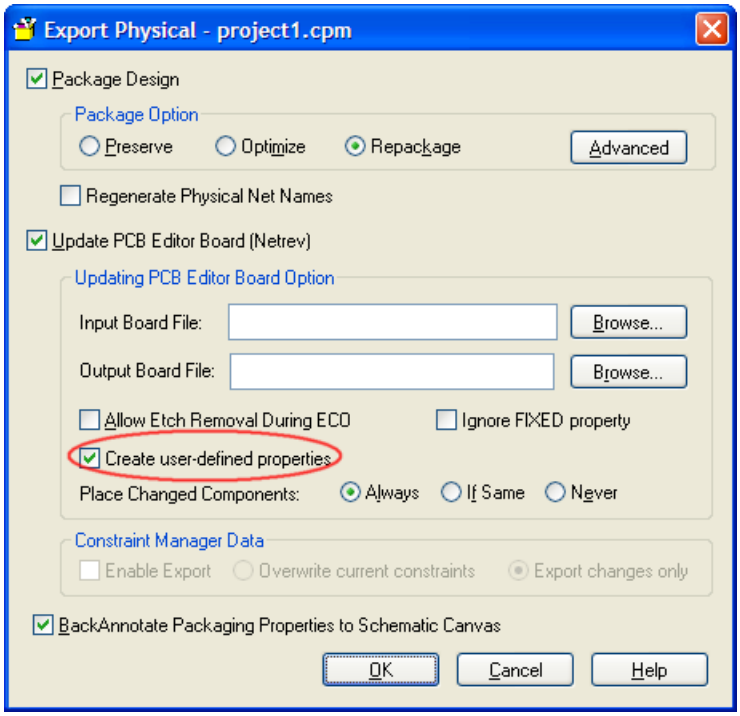
Once components are loaded, use the Attributes dialog box to assign values to component parameters as shown in Figure 1-3. For further details on creating a schematic in Design Entry HDL, see the *Allegro Design Entry HDL User Guide*.

Figure 1-3 Assigning Parameter Values in Design Entry HDL



The conventional front-to-back flow is used to transfer all RF parameters as RF properties to Allegro PCB Editor. Therefore, it is necessary to enable the *Create user-defined properties* option on the PXL form when exporting your schematic to layout as shown in Figure 1-4 on page 14. For further details on exporting schematics to physical layout, see *Packaging Your Design* in the *Allegro Front-to-Back User Guide*.

Figure 1-4 Transferring the Schematic to Layout



RF Autoplace and RF Quickplace

RF Autoplace and RF Quickplace are two methods to create RF component footprints based on parameters set in the schematic. Unlike regular components which use footprints defined in static libraries, the footprints of all RF components are dynamically created using specific RF PCB commands and stored in PCB database. After you transfer your RF schematic to layout, it is necessary to create the footprints for all RF components. Using RF PCB Autoplace command, you can create RF component footprints and automatically place them based on the logical connectivities of the RF components and related discrete components. Using RF PCB Quickplace command, you can create RF component footprints and automatically place them around the board outline similar to Allegro's quickplace command.

Only when a RF component footprint is created and placed can it be modified using other RF PCB commands. If the footprint of a RF component is deleted, either the autoplace or the quickplace command must be used to re-generate the footprint.

After you transfer your RF schematic to layout, it is necessary to specify a location in your design to generate the footprint for the first RF component. The tool then creates the footprint for the next sequential RF component and connects them if the connectivity between them is unique. If all RF components in the schematic connect using point-to-point mode, then the repackaging process automatically creates the remaining RF component footprints and

connects them all together. In cases where the connectivity is not unique, you need to specify a location for a multi-point connected component in the layout.

RF Layout

RF PCB provides a powerful RF physical design environment within Allegro PCB Editor. Key features include:

- RF placement
- RF routing
- RF editing
- RF shape editing
- RF module reuse
- Clearance shapes and assemblies

Once your layout is complete, you can export all or a portion of it to ADS Momentum for EM simulation. For further details, refer to specific chapters in this book.

ADS Simulation

ADS Momentum by Keysight Technologies is popular among engineers who perform EM simulation and parameter optimization on RF designs. Cadence provides a bi-directional IFF interface between PCB Editor and ADS for that purpose.

The recommended use model is to start your RF layout design in PCB Editor (RF or mixed signal design) and then transfer the RF portion to ADS Momentum for EM simulation. You modify and optimize component parameters or shapes in ADS to meet design requirements, then back-annotate the modified RF part to PCB Editor to update the original design. Other use models are supported, see Table 1-1 on page 11 for further details.

Back-Annotation

You can use the conventional back-to-front flow to back-annotate RF component changes from the layout in PCB Editor to the schematic in Design Entry HDL. Changes to parameter values, RefDes, and connectivity are all supported for back-annotation. Design Difference and Design Association also support this kind of back-annotation.

The layout-driven back-annotation is an enhancement to the conventional back-to-front flow in Design Entry HDL. This enhancement lets you back annotate more changes made in the back-end RF portion of the design in a structural process.

Manufacturing

Unlike IC or discrete devices, RF components are not real parts. They are really shapes from a manufacturing point of view. There is no package geometry and manufacturing information needed for RF components. The RefDes and pin number are available in the RF library, but you can remove them from manufacturing output, if required. To avoid RF components occurring in the BOM file, the property BOM_IGNORE exists both in the schematic symbol and in the package symbol.

System File Changes

If you customize the standard Cadence system files at your site, you need to modify the following files to support the RF PCB design flow. See your CAD administrator for further details.

- cds.lib
- propflow.txt
- pxlBA-rfPCB.txt
- cds.cpm
- property.dat

cds.lib

The `cds.lib` file defines the libraries that are available to your design tool. The file maps user library names to physical directory paths. Typically, one `cds.lib` file references other `cds.lib` files using INCLUDE and SOFTINCLUDE statements.

Tip

The INCLUDE statement specifies the generation of an error message when Cadence tools cannot find the library file.The SOFTINCLUDE statement specifies no error message.

File Location

Find this file in the following location:

```
<installation_directory>/share/cdssetup/
```

Changes Required

The RF library file `rf_cds.lib` must be included.

Example

Note: Changes shown in bold text.

```
DEFINE standard ../library/standard
SOFTINCLUDE ../library/vlog_cds.lib
SOFTINCLUDE $CHDL_LIB_INST_DIR/share/library/cds.lib
SOFTINCLUDE ../library/rf_cds.lib
```

propflow.txt

The `propflow.txt` file defines the properties that are transferred between Design Entry HDL and PCB Editor.

File Location

Find this file in the following location:

```
<installation_directory>/share/cdssetup/
```

Changes Required

Add all RF properties to this file. The following properties are excluded.

- RFUIDRFPADTYPE
- FSESHAPEIDX
- FSESHAPEMLSIDX

- FSESEGIDX
- RFELENGTH
- RFPADSTACKNAME
- RFPADSTACKNAME1
- RFPADSTACKNAME2
- USER_DEFINED
- RFUSRSHAPENET
- RFOLDVALUES
- RFUID

Example

Note: Changes in bold text.

```
PROPERTY_NAME!OWNER!CONCEPT!ALLEGRO!TRANSFER!WINNING_VALUE!TYPE!
ALT_SYMBOLS!1!1!1!0!0!0!
AUTO_GENERATED_TERM!1!1!1!0!0!0!
AUTO_RENAME!1!1!1!0!0!0!
. . .
. . .
ISRFELEMENT!1!1!1!1!0!0!
RFELEMENTTYPE!1!1!1!1!0!0!
RFLAYER!1!1!1!1!0!0!
RFLAYER1!1!1!1!1!0!0!
RFLAYER2!1!1!1!1!0!0!
RFLAYER3!1!1!1!1!0!0!
RFLAYER4!1!1!1!1!0!0!
RFLAYER5!1!1!1!1!0!0!
RFLAYER6!1!1!1!1!0!0!
RFLAYER7!1!1!1!1!0!0!
RFLAYER8!1!1!1!1!0!0!
```

```
RFLAYER9!1!1!1!1!0!0!
RFLAYER10!1!1!1!1!0!0!
RFLAYER11!1!1!1!1!0!0!
RFLAYER12!1!1!1!1!0!0!
RFLAYER13!1!1!1!1!0!0!
RFLAYER14!1!1!1!1!0!0!
RFLAYER15!1!1!1!1!0!0!
RFLAYER16!1!1!1!1!0!0!
RFCOUPLINGMODE!1!1!1!1!0!0!
RFFLIPMODE!1!1!1!1!0!0!
RFANGLE!1!1!1!1!0!0!
RFANGLE1!1!1!1!1!0!0!
RFWIDTH!1!1!1!1!0!0!
RFWIDTH1!1!1!1!1!0!0!
RFWIDTH2!1!1!1!1!0!0!
RFWIDTH3!1!1!1!1!0!0!
RFWIDTH4!1!1!1!1!0!0!
RFWIDTH5!1!1!1!1!0!0!
RFWIDTH6!1!1!1!1!0!0!
RFWIDTH7!1!1!1!1!0!0!
RFWIDTH8!1!1!1!1!0!0!
RFWIDTH9!1!1!1!1!0!0!
RFWIDTH10!1!1!1!1!0!0!
RFWIDTH11!1!1!1!1!0!0!
RFWIDTH12!1!1!1!1!0!0!
RFWIDTH13!1!1!1!1!0!0!
RFWIDTH14!1!1!1!1!0!0!
RFWIDTH15!1!1!1!1!0!0!
RFWIDTH16!1!1!1!1!0!0!
RFLENGTH!1!1!1!1!0!0!
RFLENGTH1!1!1!1!1!0!0!
RFLENGTH2!1!1!1!1!0!0!
```

```
RFLENGTH3!1!1!1!1!0!0!
RFLENGTH4!1!1!1!1!0!0!
RFLENGTH5!1!1!1!1!0!0!
RFLENGTH6!1!1!1!1!0!0!
RFLENGTH7!1!1!1!1!0!0!
RFLENGTH8!1!1!1!1!0!0!
RFSPACING!1!1!1!1!0!0!
RFSPACING1!1!1!1!1!0!0!
RFSPACING2!1!1!1!1!0!0!
RFSPACING3!1!1!1!1!0!0!
RFSPACING4!1!1!1!1!0!0!
RFSPACING5!1!1!1!1!0!0!
RFSPACING6!1!1!1!1!0!0!
. . .
. . .
```

pxIBA-rfPCB.txt

The `pxIBA-rfPCB.txt` file is used to extract properties for back annotation using Packager XL.

File Location

Find this file in the following location:

```
<installation_directory>/share/pcb/text/views/
```

Changes Required

Add all RF properties to this file within the component section. The following properties are excluded.

- RFUID
- RFPADTYPE
- FSESHAPEIDX

- FSESHAPEMLSIDX
- FSESEGIDX
- RFELENGTH
- RFPADSTACKNAME
- RFPADSTACKNAME1
- RFPADSTACKNAME2
- USER_DEFINED
- RFUSRSHAPENET
- RFOLDVALUES

Example

Note: Changes shown in bold text.

```
. . .
. . .
#   The following properties are needed to feedback ppt
#   part selections done in Allegro.
#   You may comment them out if you do not use this functionality.
    COMP_PARENT_PPT
    COMP_SYMBOL_EDITED
    COMP_PARENT_PPT_PART
          COMP_ISRFELEMENT
          COMP_RFELEMENTTYPE
          COMP_RFLAYER
          COMP_RFLAYER1
          COMP_RFLAYER2
          COMP_RFLAYER3
          COMP_RFLAYER4
          COMP_RFLAYER5
          COMP_RFLAYER6
          COMP_RFLAYER7
          COMP_RFLAYER8
          COMP_RFLAYER9
          COMP_RFLAYER10
          COMP_RFLAYER11
          COMP_RFLAYER12
          COMP_RFLAYER13
          COMP_RFLAYER14
          COMP_RFLAYER15
          COMP_RFLAYER16
          COMP_RFCOUPLINGMODE
          COMP_RFFLIPMODE
          COMP_RFANGLE
```

COMP_RFANGLE1

COMP_RFWIDTH

COMP_RFWIDTH1

COMP_RFWIDTH2

COMP_RFWIDTH3

COMP_RFWIDTH4

COMP_RFWIDTH5

COMP_RFWIDTH6

COMP_RFWIDTH7

COMP_RFWIDTH8

COMP_RFWIDTH9

COMP_RFWIDTH10

COMP_RFWIDTH11

COMP_RFWIDTH12

COMP_RFWIDTH13

COMP_RFWIDTH14

COMP_RFWIDTH15

COMP_RFWIDTH16

COMP_RFLENGTH

COMP_RFLENGTH1

COMP_RFLENGTH2

COMP_RFLENGTH3

COMP_RFLENGTH4

COMP_RFLENGTH5

COMP_RFLENGTH6

COMP_RFLENGTH7

COMP_RFLENGTH8

COMP_RFSPACING

COMP_RFSPACING1

COMP_RFSPACING2

COMP_RFSPACING3

COMP_RFSPACING4

COMP_RFSPACING5

COMP_RFSPACING6

COMP_RFSPACING7

COMP_RFSPACING8

COMP_RFSPACING9

COMP_RFSPACING10

COMP_RFSPACING11

COMP_RFSPACING12

COMP_RFSPACING13

COMP_RFSPACING14

COMP_RFSPACING15

COMP_RFOFFSETX

COMP_RFOFFSETY

COMP_RFRADIUS

COMP_RFDEPTH

COMP_RFFREQUENCY

COMP_RFMITERFRACTION

COMP_RFBENDMODE

COMP_RFNUMBERLEGS

COMP_RFNUMBERPAIRS

COMP_RFNUMBERTURNS

COMP_RFCAPACITANCE

COMP_RFRESISTANCE

COMP_RFINDUCTANCE

COMP_RFPADSTACKNAME

COMP_RFPADSSMNAME1

COMP_RFPADSSMNAME2

COMP_RFPADBEGINLAYER

COMP_RFPADENDLAYER

COMP_RFPADLINEWIDTH1

COMP_RFPADLINEWIDTH2

COMP_RFPADDIAMETER1

```
          COMP_RFPADDIAMETER2
          COMP_RFPADLENGTH1
          COMP_RFPADLENGTH2
          COMP_RFHOLEDIAMETER
          COMP_RFPADANGLE
          COMP_RFDRANAME
          COMP_RFPADTYPE
END
. . .
. . .
#
# Signal properties view. File: netView.dat
# Include this section only if you wish to extract and ba any net properties.
# In order to backannotate signal properties you must
# include NET_NAME
```

cds.cpm

This file defines default setup information for all design projects.

File Location

Find this file in the following location:

```
<installation_directory>/share/cdssetup/projmgr/
```

Changes Required

Add all RF properties to the end of this file in a separate section. The following properties are excluded.

- FSESHAPEIDX
- FSESHAPEMLSIDX
- FSESEGIDX

Example

Note: Changes shown in bold text.

```
. . .

. . .

EXCLUDE_REF_PPT

INCLUDE_REF_PPT

END_ADW

START_RFPCB

COMP_INST_PROP  'ISRFELEMENT' 'RFELEMENTTYPE' 'RFLAYER' 'RFLAYER1' 'RFLAYER2'
     'RFLAYER3' 'RFLAYER4' 'RFLAYER5' 'RFLAYER6' 'RFLAYER7' 'RFLAYER8' 'RFLAYER9'
     'RFLAYER10' 'RFLAYER11' 'RFLAYER12' 'RFLAYER13' 'RFLAYER14' 'RFLAYER15'
     'RFLAYER16' 'RFCOUPLINGMODE' 'RFFLIPMODE' 'RFANGLE' 'RFANGLE1' 'RFWIDTH'
     'RFWIDTH1' 'RFWIDTH2' 'RFWIDTH3' 'RFWIDTH4' 'RFWIDTH5' 'RFWIDTH6' 'RFWIDTH7'
     'RFWIDTH8' 'RFWIDTH9' 'RFWIDTH10' 'RFWIDTH11' 'RFWIDTH12' 'RFWIDTH13'
     'RFWIDTH14' 'RFWIDTH15' 'RFWIDTH16' 'RFLENGTH' 'RFLENGTH1' 'RFLENGTH2'
     'RFLENGTH3' 'RFLENGTH4' 'RFLENGTH5' 'RFLENGTH6' 'RFLENGTH7' 'RFLENGTH8'
     'RFSPACING' 'RFSPACING1' 'RFSPACING2' 'RFSPACING3' 'RFSPACING4' 'RFSPACING5'
     'RFSPACING6' 'RFSPACING7' 'RFSPACING8' 'RFSPACING9' 'RFSPACING10'
     'RFSPACING11' 'RFSPACING12' 'RFSPACING13' 'RFSPACING14' 'RFSPACING15'
     'RFOFFSETX' 'RFOFFSETY' 'RFRADIUS' 'RFDEPTH' 'RFFREQUENCY' 'RFMITERFRACTION'
     'RFBENDMODE' 'RFNUMBERLEGS' 'RFNUMBERPAIRS' 'RFNUMBERTURNS' 'RFCAPACITANCE'
     'RFRESISTANCE' 'RFINDUCTANCE' 'RFPADSTACKNAME' 'RFPADSSMNAME1'
     'RFPADSSMNAME2' 'RFPADBEGINLAYER' 'RFPADENDLAYER' 'RFPADLINEWIDTH1'
     'RFPADLINEWIDTH2' 'RFPADDIAMETER1' 'RFPADDIAMETER2' 'RFPADLENGTH1'
     'RFPADLENGTH2' 'RFHOLEDIAMETER' 'RFPADANGLE' 'RFDRANAME' 'RFPADTYPE'

END_RFPCB
```

property.dat

This file controls the default properties displayed in various selection lists within Design Entry HDL.

File Location

Find this file in the following location:

```
<installation_directory>/share/cdssetup/
```

Changes Required

Include the following RF properties in the `"ALT_SYMBOLS""COMP"` section.

- ISRFELEMENT
- RFELEMENTTYPE
- RFPADSTACKSSMNAME1
- RFPADSTACKSSMNAME2

Example

Note: Changes shown in bold text.

```
;;   This file controls the default properties displayed
;;   in various selection lists for Concept HDL
. . .
. . .
("ALT_SYMBOLS""COMP")
                    ("ASSIGN_TOPOLOGY""WIRE")
                    ("BLOCK   ""COMP")
                    ("BOM_IGNORE""COMP")
                    ("BUS_NAME""WIRE")
                    ("COMMENT_BODY""COMP")
                    ("DIFFERENTIAL_PAIR""WIRE")
                    ("ECL" "WIRE")
                    ("ELECTRICAL_CONSTRAINT_SET""WIRE")
                    ("EMC_COMP_TYPE""COMP")
                    ("EMC_CRITICAL_IC""COMP")
                    ("EMC_CRITICAL_NET""WIRE")
                    ("GROUP""COMP")
                    ("HDL_PORT""WIRE")
                    ("HDL_POWER""COMP")
                    ("HEIGHT""COMP")
```

```
("IMPEDANCE_RULE""COMP")
("JEDEC_TYPE""COMP")
("LOCATION""COMP")
("LINK" "COMP")
("LINK" "WIRE")
("MAX_VIA_COUNT""WIRE")
("MAX_XTALK""WIRE")
("MIN_LINE_WIDTH""WIRE")
("NC_PINS""COMP")
("NET_PHYSICAL_TYPE""WIRE")
("NET_SCHEDULE""WIRE")
("NET_SPACING_TYPE""WIRE")
("NO_SWAP_GATE""COMP")
("NO_SWAP_GATE_EXT""COMP")
("NO_SWAP_PIN""COMP")
("PACK_IGNORE""COMP")
("PACK_SHORT""COMP")
("PACK_TYPE""COMP")
("PART_NUMBER""COMP")
("PATH""COMP")
("PINUSE""WIRE")
("PIN_TYPE""WIRE")
("PLUMBING_BODY""COMP")
("POWER_GROUP""COMP")
("POWER_PINS""COMP")
("PROPAGATION_DELAY""WIRE")
("RATSNEST_SCHEDULE""WIRE")
("RELATIVE_PROPAGATION_DELAY""WIRE")
("REMOVE""COMP")
("REUSE_INSTANCE" "COMP")
("REUSE_MODULE" "COMP")
("ROOM""COMP")
```

```
            ("ROUTE_PRIORITY""WIRE")
            ("SIG_NAME""WIRE")
            ("SIM_MAP_VIEW""WIRE")
            ("SPLIT_INST""COMP")
            ("SPLIT_INST_NAME""COMP")
            ("STUB_LENGTH""WIRE")
            ("SUBNET_NAME""WIRE")
            ("SWAP_GROUP""COMP")
            ("TERMINATOR_PACK""COMP")
            ("VALUE""COMP")
            ("VERILOG_MODEL""COMP")
            ("VHDL_INIT""WIRE")
            ("VHDL_MODEL""COMP")
            ("VIA_LIST""WIRE")
            ("VLOG_MODEL""COMP")
            ("VOLTAGE""COMP")
            ("WEIGHT""COMP")
            ("ISRFELEMENT""COMP""unlocked"    "hidden")
            ("RFELEMENTTYPE""COMP""unlocked"    "hidden")
            ("RFPADSTACKSSMNAME1"   "COMP""unlocked""hidden")
            ("RFPADSTACKSSMNAME2""COMP""unlocked""hidden")
      )
)
(
      (
            GC_CHANGE_FROM_VALUE
      GC_CHANGE_TO_VALUE
      GC_DELETE_VALUE
      )
      (


      )
```

)

)

RF Properties

The properties used by RF PCB in Design Entry HDL and PCB Editor are shown in Table 1-2.

Table 1-2 RF Properties

Property	Design Entry HDL	PCB Editor	Transferred Between
ISRFELEMENT	x	x	x
RFELEMENTTYPE	x	x	x
RFLAYER	x	x	x
RFLAYER1	x	x	x
RFLAYER2	x	x	x
RFLAYER3	x	x	x
RFLAYER4	x	x	x
RFLAYER5	x	x	x
RFLAYER6	x	x	x
RFLAYER7	x	x	x
RFLAYER8	x	x	x
RFLAYER9	x	x	x
RFLAYER10	x	x	x
RFLAYER11	x	x	x
RFLAYER12	x	x	x
RFLAYER13	x	x	x
RFLAYER14	x	x	x
RFLAYER15	x	x	x
RFLAYER16	x	x	x
RFCOUPLINGMODE	x	x	x

Table 1-2 RF Properties

Property	Design Entry HDL	PCB Editor	Transferred Between
RFFLIPMODE	x	x	x
RFANGLE	x	x	x
RFANGLE1	x	x	x
RFWIDTH	x	x	x
RFWIDTH1	x	x	x
RFWIDTH2	x	x	x
RFWIDTH3	x	x	x
RFWIDTH4	x	x	x
RFWIDTH5	x	x	x
RFWIDTH6	x	x	x
RFWIDTH7	x	x	x
RFWIDTH8	x	x	x
RFWIDTH9	x	x	x
RFWIDTH10	x	x	x
RFWIDTH11	x	x	x
RFWIDTH12	x	x	x
RFWIDTH13	x	x	x
RFWIDTH14	x	x	x
RFWIDTH15	x	x	x
RFWIDTH16	x	x	x
RFLENGTH	x	x	x
RFLENGTH1	x	x	x
RFLENGTH2	x	x	x
RFLENGTH3	x	x	x
RFLENGTH4	x	x	x
RFLENGTH5	x	x	x

Table 1-2 RF Properties

Property	Design Entry HDL	PCB Editor	Transferred Between
RFLENGTH6	x	x	x
RFLENGTH7	x	x	x
RFLENGTH8	x	x	x
RFSPACING	x	x	x
RFSPACING1	x	x	x
RFSPACING2	x	x	x
RFSPACING3	x	x	x
RFSPACING4	x	x	x
RFSPACING5	x	x	x
RFSPACING6	x	x	x
RFSPACING7	x	x	x
RFSPACING8	x	x	x
RFSPACING9	x	x	x
RFSPACING10	x	x	x
RFSPACING11	x	x	x
RFSPACING12	x	x	x
RFSPACING13	x	x	x
RFSPACING14	x	x	x
RFSPACING15	x	x	x
RFOFFSETX	x	x	x
RFOFFSETY	x	x	x
RFRADIUS	x	x	x
RFDEPTH	x	x	x
RFMITERFRACTION	x	x	x
RFBENDMODE	x	x	x
RFNUMBERLEGS	x	x	x

Table 1-2 RF Properties

Property	Design Entry HDL	PCB Editor	Transferred Between
RFNUMBERPAIRS	x	x	x
RFNUMBERTURNS	x	x	x
RFELENGTH		x	
RFFREQUENCY	x	x	x
RFCAPACITY	x	x	x
RFRESISTANCE	x	x	x
RFINDUCTANCE	x	x	x
RFPADSTACKNAME		x	
RFPADSSMNAME1		x	
RFPADSSMNAME2		x	
RFPADBEGINLAYER	x	x	x
RFPADENDLAYER	x	x	x
RFPADLINEWIDTH1	x	x	x
RFPADLINEWIDTH2	x	x	x
RFPADDIAMETER1	x	x	x
RFPADDIAMETER2	x	x	x
RFPADLENGTH1	x	x	x
RFPADLENGTH2	x	x	x
RFHOLEDIAMETER	x	x	x
RFPADANGLE	x	x	x
USER_DEFINED		x	
RFDRANAME	x	x	x
RFUSRSHAPENET		x	
RFOLDVALUES		x	
RFUID		x	
RFPADTYPE		x	

Table 1-2 RF Properties

Property	Design Entry HDL	PCB Editor	Transferred Between
FSESHAPEIDX		x	
FSESHAPEMLSIDX		x	
FSESEGIDX		x	
RF_PCB_SYMBOL	x	x	x

RF Properties in Design Entry HDL

The following RF properties are invisible in the Attribute dialog box of Design Entry HDL.

- ISRFELEMENT
- RFELEMENTTYPE
- RFPADSSMNAME1
- RFPADSSMNAME2
- RFGROUP
- RFSPLIT

RF Properties in PCB Editor

The following properties are incorporated into Allegro database but are invisible to users.

- ISRFELEMENT
- RFELEMENTTYPE

All other RF properties are of the user-defined type. Be sure to enable *Create user-defined properties* on the Export Physical dialog box when transferring a schematic to layout.

The RF PCB User Interface

You can enter RF PCB commands within the PCB Editor environment using a drop-down menu from the toolbar or by typing directly in the console window. Clicking the *RF-PCB* toolbar item allows access to the complete set of RF PCB menus shown in Table 1-3.

RF-PCB Toolbar Item and Main Menu

The RF-PCB command can be accessed from the RF-PCB main menu in the Allegro toolbar. The following table lists all the RF-PCB menus and sub-menus.

Table 1-3 RF-PCB Menus and submenus

Menu	Sub menu	Corresponding command
Setup		`rf_setup`
Quickplace		`rf_quickplace`
Autoplace		`rf_autoplace`
Load Module		`rf_load_module`
Add Component		`rf_add_component`
Add Connect		`rf_add_connect`
Single segment Connect		`rf_single_segment_connect`
Any Angle Bend Connect		`rf_any_angle_bend`

Menu	Sub menu	Corresponding command
Edit		
	Change	rf_change
	Break	rf_break
	Snap	rf_snap
	Delete	rf_delete
	Scaled Copy	rf_scaled_copy
	Modify Connectivity	rf_modify_net
	Copy	rf_group_copy
	Flip	rf_flip
	Push	rf_push
	VAR Edit	rf_varedit
Convert		
	Tapered Pin Connect	rf_tapered_connect
	Chamfer	rf_chamfer
	Shape to Component	rf_shape2component
	Component to Shape	rf_component2shape
	CLine to TLine Conversion	rf_cline_convert
Clearance		
	Settings	rf_ac_setup
	Initialize	rf_ac_init
	Assemble	rf_ac_assemble
	Disassemble	rf_ac_disassemble
	Delete	rf_ac_delete
Display		
	Information	rf_display_info
	Measurement	rf_measure
	New Component	rf_display_newcomp

Menu	Sub menu	Corresponding command
IFF Interface		
	Import	rf_iff_import
	Export	rf_iff_export
	SMT Library Translator	rf_libxlator
Flexible Shape Editor		
	Edge Move	fse_edge_move
	Edge Stretch	fse_edge_stretch
	Edge Spread	fse_edge_spread
	Tangent Segment	fse_seg_tangent
	Arc Tangent	fse_arc_tangent
	Line End Connect	fse_end_connect
	Break and Delete	fse_break_delete
	Vertex Insert	fse_vertex_insert
	Vertex Move	fse_vertex_move
	Vertex Convert	fse_vertex_convert
	Shape Operations	fse_shape_logicop
	Shape Corner Chamfer	fse_shape_chamfer
	Shape Scale	fse_shape_scale
	Multi-Layer Shape ZCopy	fse_shape_zcopy
	Multi-Layer Shape ZDelete	fse_shape_zdelete

Right Mouse Button

Use the right mouse button to make command entries more efficient. While in any command, you can click the right mouse button to access the command options as you desire. Table 1-4 outlines some of the common options in a right mouse button menu.

Table 1-4 Common Right Mouse Button Commands

Command	Function
Done	End the current command.
Oops	Undo the last action.
Cancel	Undo all actions up to the last Done.
Next	Commit all changes and continue.

In addition, there are right mouse button options specific to RF PCB commands.

If you are in the Rfedit_Appm mode, you can use the right-mouse button to access a number of context sensitive RF commands. In this mode, if you right-click on a selected RF element or group of RF elements, the context menu displays RF commands specific to the types of objects selected. In addition, the menu also displays some generic RF commands (not specific to the object or objects selected) under a Quick Utilities sub-menu of the RMB.

The following table describes the list of RF commands available on the right-mouse button in the Rfedit_Appm mode:

RF Command	Supported Object Types	Single / Multiple Object selection support*
rf_change	■ Component (*RF component only*) ■ Symbol (*RF symbol only*)	Single
rf_break	■ Component (*RF component only*) ■ Symbol (*RF symbol only*)	Single
rf_snap	■ Pin (*non-mechanical*)	Single
rf_modify_net	■ Pin (*non-mechanical*)	Single
rf_delete	■ Component (*RF component only*)	Single or Multiple
rf_scaled_copy	■ Component (*RF component only*) ■ Symbol (*RF symbol only*)	Single or Multiple

RF Command	Supported Object Types	Single / Multiple Object selection support*
rf_group_copy	■ Component ■ Symbol ■ Cline ■ Line ■ Cline segment ■ Line segment ■ Shape ■ Filled rectangle ■ Rectangle ■ Via ■ Group	Single or Multiple
rf_flip	■ Component ■ Symbol ■ Cline ■ Line ■ Cline segment ■ Line segment ■ Shape ■ Filled rectangle ■ Rectangle ■ Via ■ Group	Single or Multiple

RF Command	Supported Object Types	Single / Multiple Object selection support*
rf_push	■ Component ■ Symbol ■ Cline ■ Line ■ Cline segment ■ Line segment ■ Shape ■ Filled rectangle ■ Rectangle ■ Group	Single or Multiple
rf_display_info	■ Component (RF component only) ■ Symbol (RF symbol only)	Single or Multiple
rf_tapered_connect	■ Pin (non RF and non mechanical pin only)	Single or Multiple
rf_chamfer	■ Component (*RF component only*) ■ Symbol (*RF symbol only*)	Single or Multiple
rf_shape2component	■ Shape / Filled rectangle (non dynamic etch only)	Single or Multiple
rf_component2shape	■ Component (*RF component only*) ■ Symbol (*RF symbol only*)	Single or Multiple
rf_cline_convert	■ Cline	Single or Multiple
rf_ac_init	■ Component (*RF component only*) ■ Symbol (*RF symbol only*)	Single or Multiple

RF Command	Supported Object Types	Single / Multiple Object selection support*
rf_ac_assemble	■ Component ■ Symbol ■ Cline – non symbol child ■ Shape (etch or AC shape only) – non symbol child ■ Filled rectangle (etch or AC shape only) – non symbol child ■ Via – non symbol child ■ Group	Single or Multiple
rf_ac_disassemble	■ Group (AC assembly only)	Single or Multiple
rf_ac_delete	■ Group (AC assembly only)	Single or Multiple

* This implies that the corresponding RF command is available on the right-click menu in a single object or multiple object selection.

In addition to the context sensitive RF commands available in the Rfedit_Appm mode, the right-click menu also displays the following commands in the Quick Utilities sub-menu:

- rf_setup
- rf_autoplace
- rf_quickplace
- rf_add_component
- rf_add_component
- rf_iff_import
- rf_iff_export

RF Board Setup

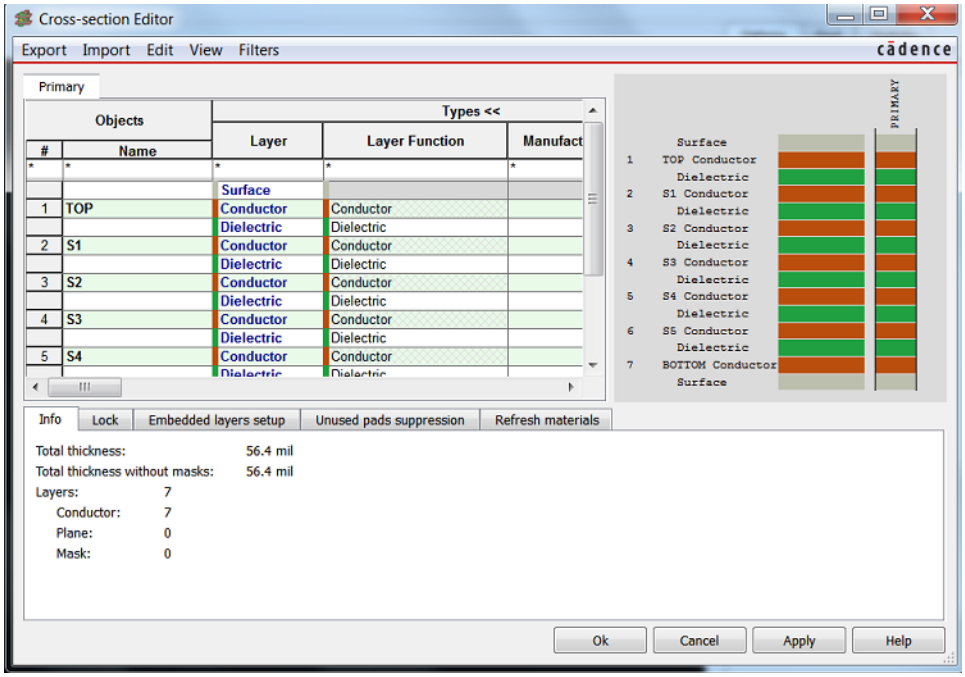
Setting up Layers

RF PCB performs various calculations that use the stackup. Therefore, you need to specify the layer cross section prior to starting your design layout.

➤ Choose *Setup – Cross Section* to access the Cross Section Editor dialog box shown in Figure 1-5, then specify a proper layer structure for your design.

For further details, see the `xsection` command in the *Allegro PCB and Package Physical Layout Command Reference*.

Figure 1-5 Cross Section Editor Dialog Box



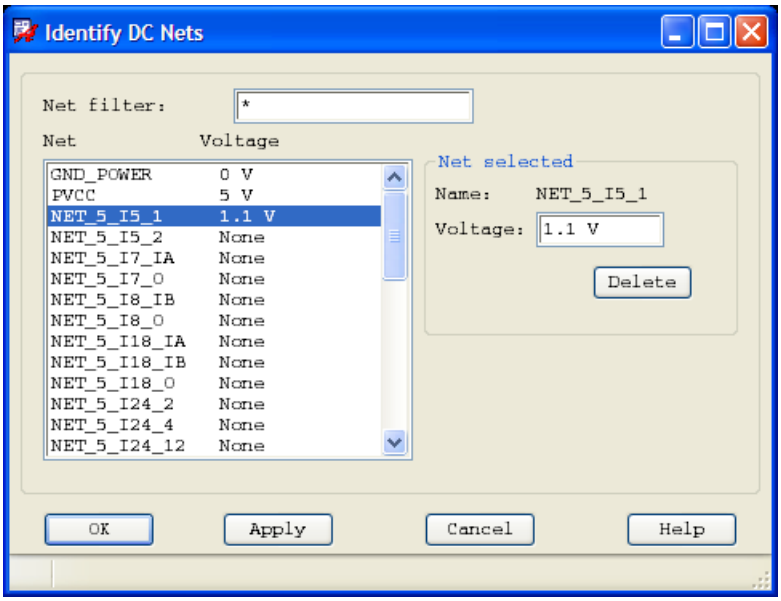
Identifying DC Nets

Some RF components may involve shapes (such as shield line and CPW). Before placing those components, you need to identify the voltage for planes and shapes. Otherwise, the console window displays an error message as you generate them.

➤ Choose *Logic – Identify DC Nets* to access the Identify DC Nets dialog box as shown in Figure 1-6, then select the appropriate nets and assign each a voltage of zero.

For further details, see the identify nets command in the *Allegro PCB and Package Physical Layout Command Reference*.

Figure 1-6 The Identify DC Nets Dialog Box



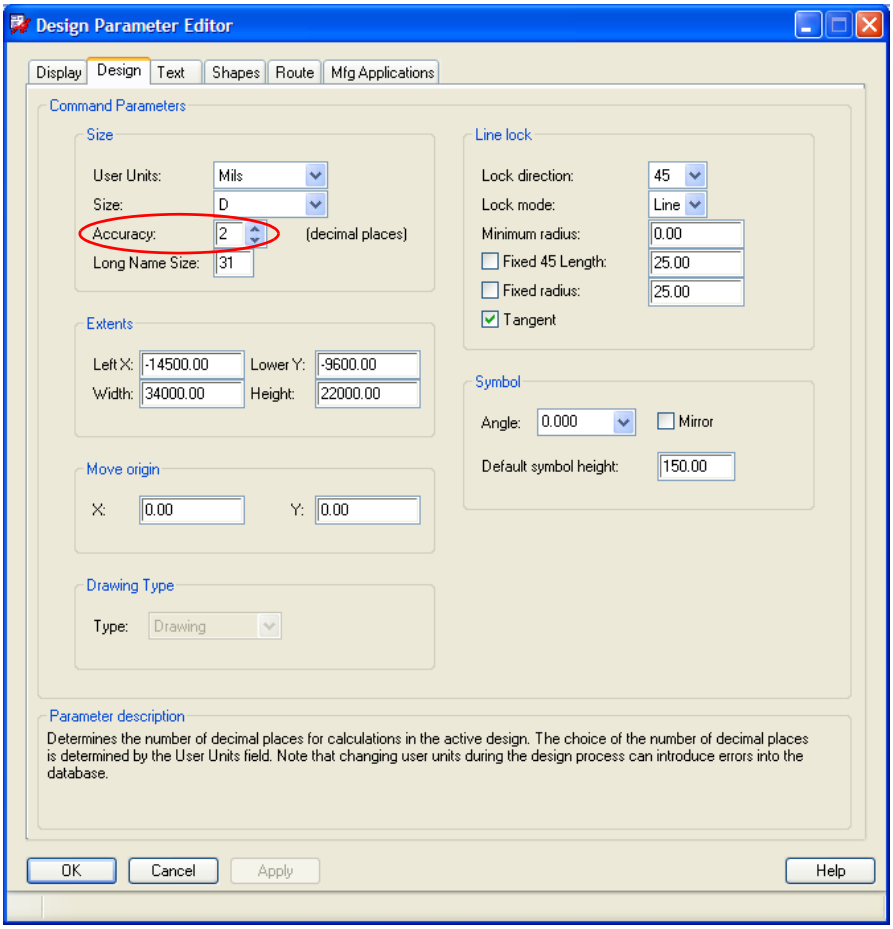
Other Setup Tasks

Given the special structure of RF components, Cadence recommends that you perform these additional setup tasks for your RF design.

➡ Choose *Setup – Design Parameters – Design* to access the Design Parameter Editor dialog shown in Figure 1-7, then set *Accuracy* to more than 1 decimal place.

For further details, see the prmed command in the *Allegro PCB and Package Physical Layout Command Reference*.

Figure 1-7 Design Parameter Editor Dialog Box



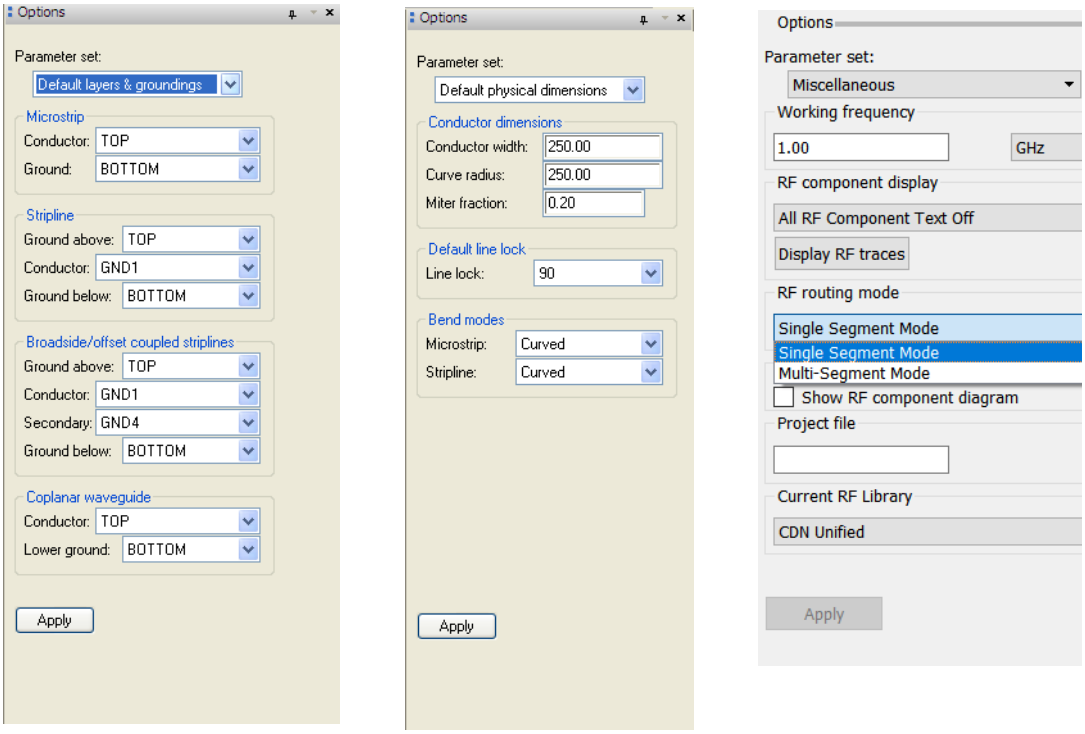
RF Global Variable Initialization

Before using RF PCB, you need to perform RF global variable initialization. This will specify default parameters for the following:

- Structure of microstrip and stripline
- Physical dimensions for routing RF traces
- Line lock mode and bend mode for RF routing
- Working frequency

To perform the initialization, choose *RF PCB — Setup* to access the RF PCB Settings shown in Figure 1-8.

Figure 1-8 RF-PCB Setup options



For further details on the settings themselves, see the `rf setup` command in the Allegro PCB and Package Physical Layout Command Reference.

2

RF Placement

- RF Component Autoplace
- RF Quickplace
- RF Add Component Command
- RF Components

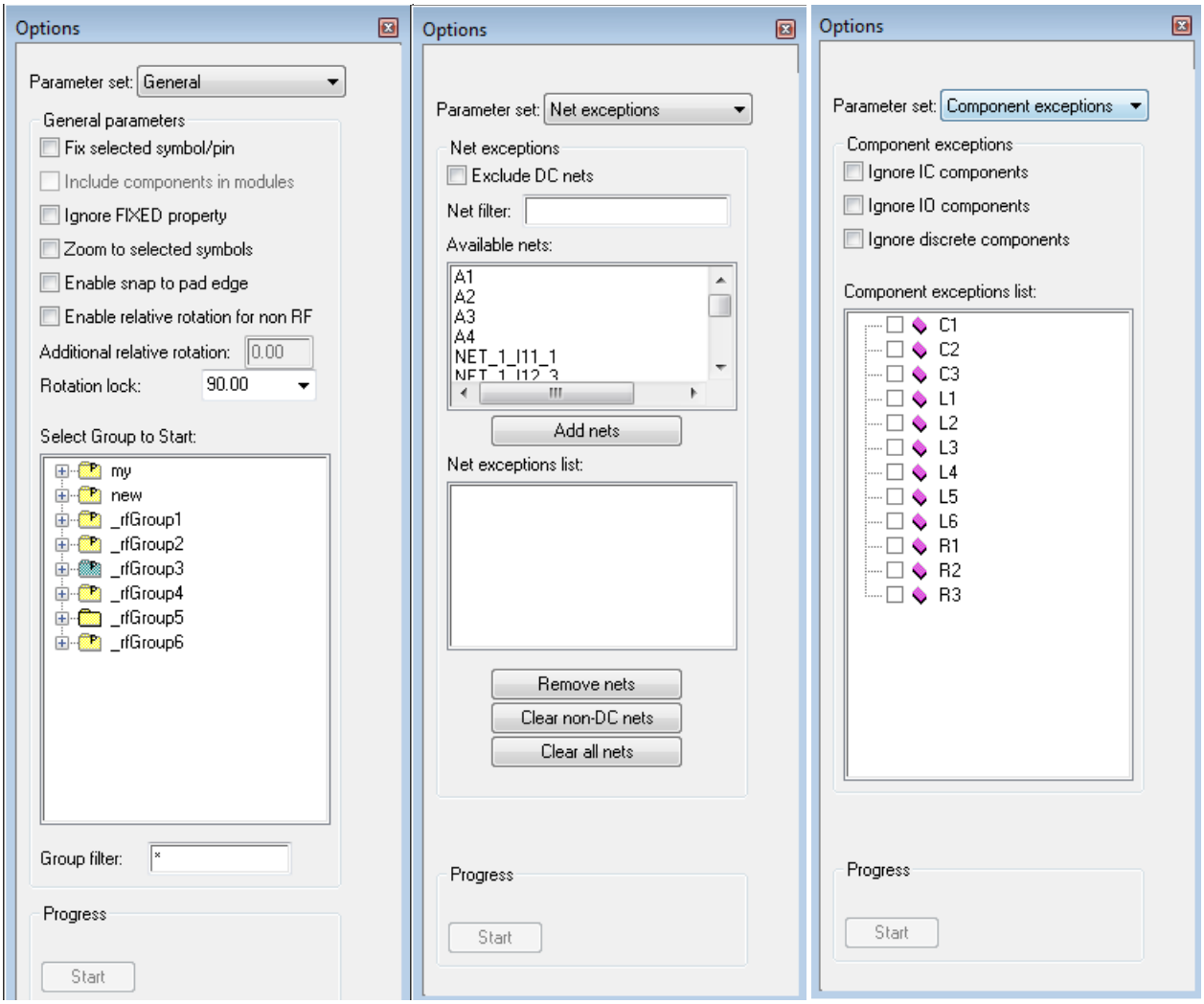
RF Component Autoplace

Component autoplacing is the process of repackaging (generating or re-generating) the physical footprints for the RF components in the design according to the parameter values assigned in the schematic and then placing (or re-placing) them in the layout. You need to perform component repackaging when you:

- Transfer a schematic to the board for the initial design.
- Make changes to the schematic and then transfer the logic information back to the board.
- Delete the RF package symbols on the board and then decide to place those RF components again in the design.
- Change the units or accuracy of the design in the Drawing Parameters dialog box.

To perform component repackaging within Allegro PCB Editor, choose *RF-PCB — Autoplace.*

Figure 2-1 Autoplace Options pane

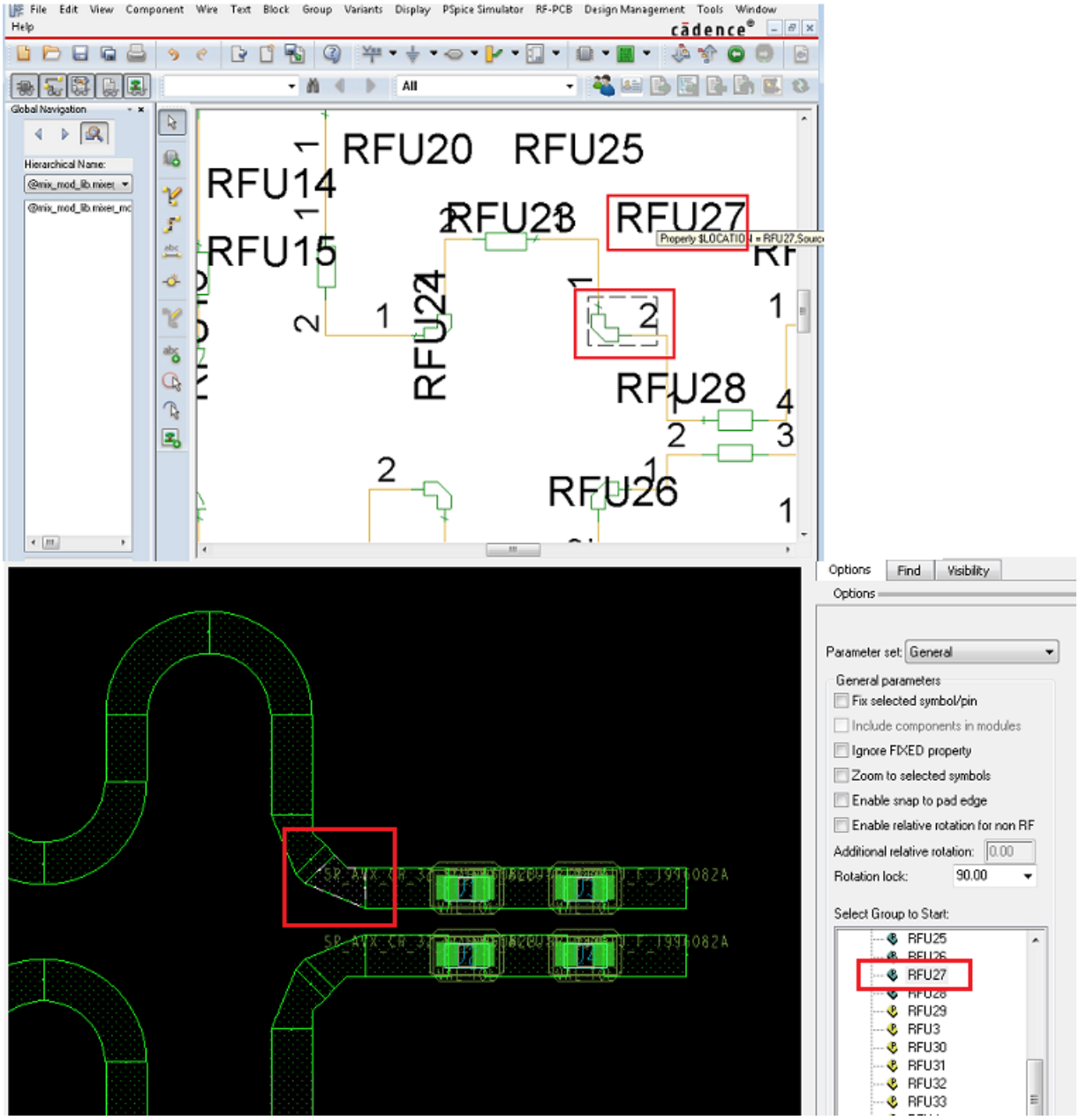


The command first checks to see if it is necessary to repackage a component before creating the dynamic footprint. If its package symbol already exists and no parameter changes are required, the component is skipped (not repackaged).

Distinct features of RF Component Autoplace

- You can select the symbol in the schematic for autoplacement. When the symbol in the schematic is selected, the corresponding symbol in PCB Editor will also be selected in the design canvas. If `rf_autoplace` command is active in *Options* pane the group in

which the symbol is present is expanded and the corresponding tree view item is also selected.



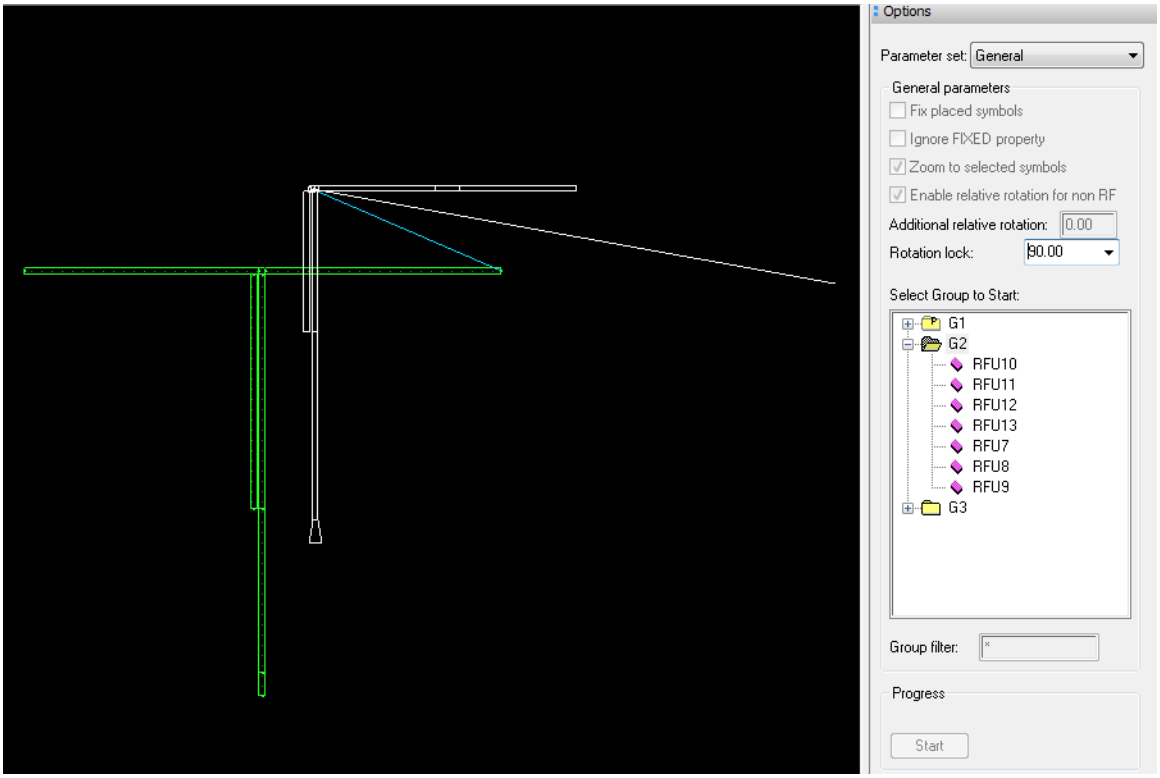
You can also select a pin in the schematic and it will be selected in the PCB editor canvas if the Find filter is set to *Pins*.

- You can search for any group or component by using *Group filter*. This filter is very useful in large designs that contain many groups and components. The *Group filter* narrows down the list of groups and only displays the groups that are searched. For

example, if group G1 is searched, only the group G1 is displayed. The wildcard * is supported.

If you input a Reference Designator to the group filter, only the group that contains the component with the Reference Designator is displayed.

The autoplace command lets you choose a group of components and place it where you want it. All the components in a group are placed automatically. These groups are based on the logic connectivity of components. When you select a group for placement, the ratsnest are displayed and a dynamic path is attached to the group. For example, in the following figure, group G2 is being placed. The dynamic path and ratsnests connecting this group to components outside the group are displayed.



Tip

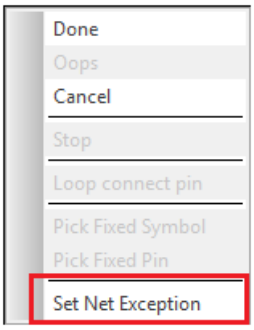
To include fixed components into the group for auto placement, enable the option *Ignore Fixed Property.*

- You can use *Loop connect pin* command from right-click menu to select the specific pin to connect.

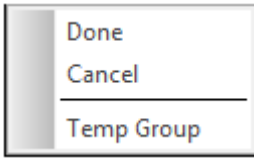
  When you have selected *Enable relative rotation for non-RF* the right-click menu option *Loop connect pin* is enabled for groups or components with multiple connect

pins. Connect pins are pins that are used to connect to other logical pins outside the group. Use the *Loop connect pin* option to change to other connect pins.

- For placement of all non-RF components during the repackaging process you can specify a default angle.
- To exclude specific nets (such as DC nets) in the autoplace process by selecting and adding the nets to the Net Exceptions List in the Options tab. You can also choose nets from the design canvas using right-click menu *Set Net Exception* and enable the Find Filter for Nets, Pins, Vias and Clines.



In the interactive selection process, the right-click menu changes as follows to help easy selection of objects.



Once objects are selected, the net names of those objects are retrieved and added in the Net Exception list.

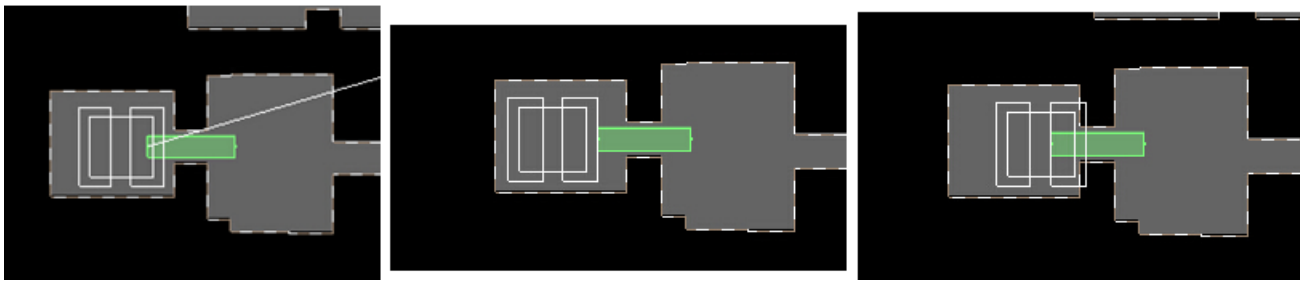
- You can also exclude specific components in the autoplace process by selecting them in the Components exception list.

Interactive Repackaging or Autoplacement with Snap to Pad Edge

The interactive repackage process is enabled by turning off the options *Fix selected symbol/pin* and *Enable relative rotation for non RF* and turning on *Enable snap to pad edge* for making connections between components.

Connecting a non-RF component to RF component

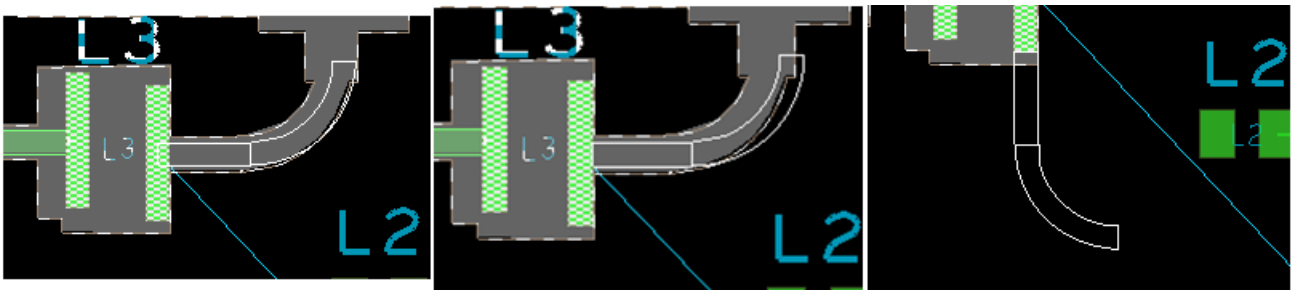
To connect a non-RF component to a RF component first specify the angle of rotation for a non-RF component. The autoplace command automatically searches for valid pad edges of the connecting pin of the non-RF component that are parallel to the edge of the connecting pin of the RF component. The list of pad edges also includes center point of the connecting pin of the non-RF component. Use mouse to snap pad edge of a non-RF component pin to the RF component. The following image shows the snapping of a non-RF component to the pad edge of a RF component.



Connecting RF component to a non-RF component

You can snap the RF component to one of the pad edges of the connecting pin of a non-RF component or the center point of the connecting pin of the non-RF component.

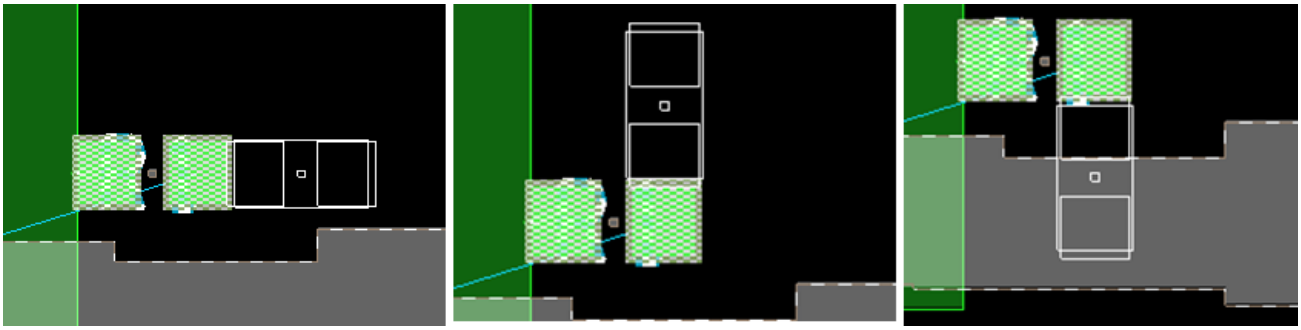
The following image show the snapping of a RF component to the pad edge/connection point of a non-RF component.



Connecting a non-RF component to a non-RF component

You can snap the pad edge of the source non-RF component to one of the pad edges of the destination non-RF component. The snapping is controlled by the movements of the mouse.

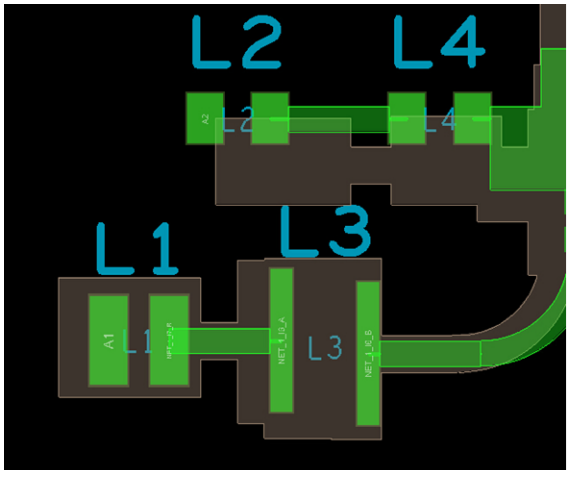
The following image show the snapping of a non-RF component to the pad edge/connection point of a non-RF component



Pin to pin connections for Pad Edge Snapping

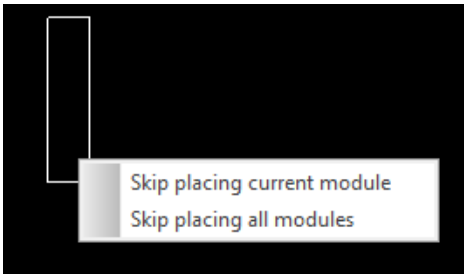
When components are connected using pad edge snapping, pin-pin connection is not realized and there will be ratsnest between the two pins. The autoplace command automatically adds cline segments to ensure pin to pin connections.

The following image shows the cline segments added by the interactive repackage process without ratsnests. You can see that there is no cline segment between RF component that is connected to the pin of L1 as the RF component is connected to the pin location rather than one of the pin pad edges.

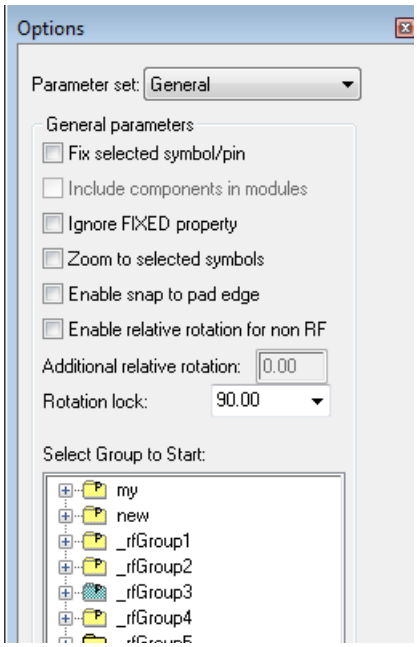


Module Placement Support for Autoplace

If there is any unplaced module in the design the autoplace command allows you to place them first. You can skip the placement of module using right-click menu options. You can choose to skip placement of one or all the modules.



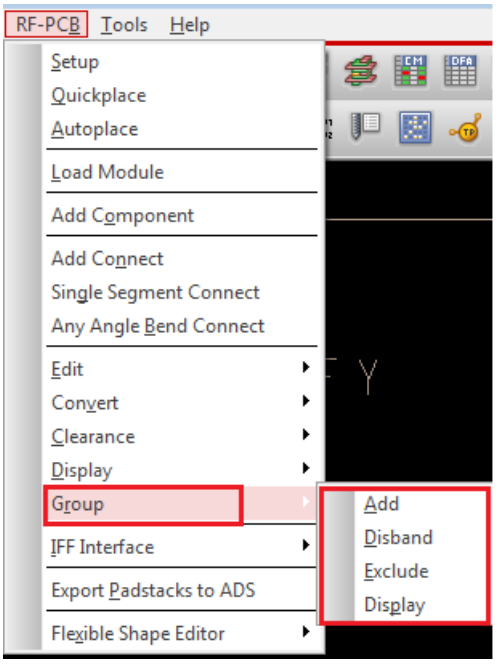
After the module instanced are all placed or skipped, the autoplacement options are displayed and the *Include components in modules* becomes enable.



If you choose *Include components in modules,* all module instances are listed in separate groups under the module instance name. You can select the group or individual component for autoplacement.

Grouping functionality for Autoplace

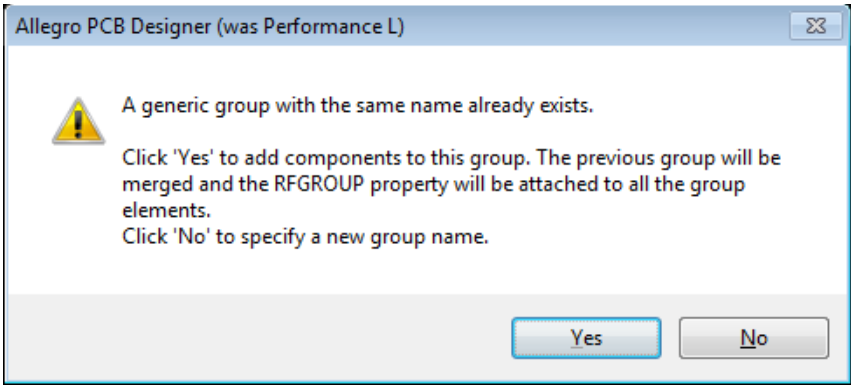
You can define and manage RF groups for autoplacement of components in the layout by using RF group commands.



The RFGROUP property is added to all the members of a group with the value is equal to the name of the RF group. All the components with same RFGROUP property are placed together during autoplacement.

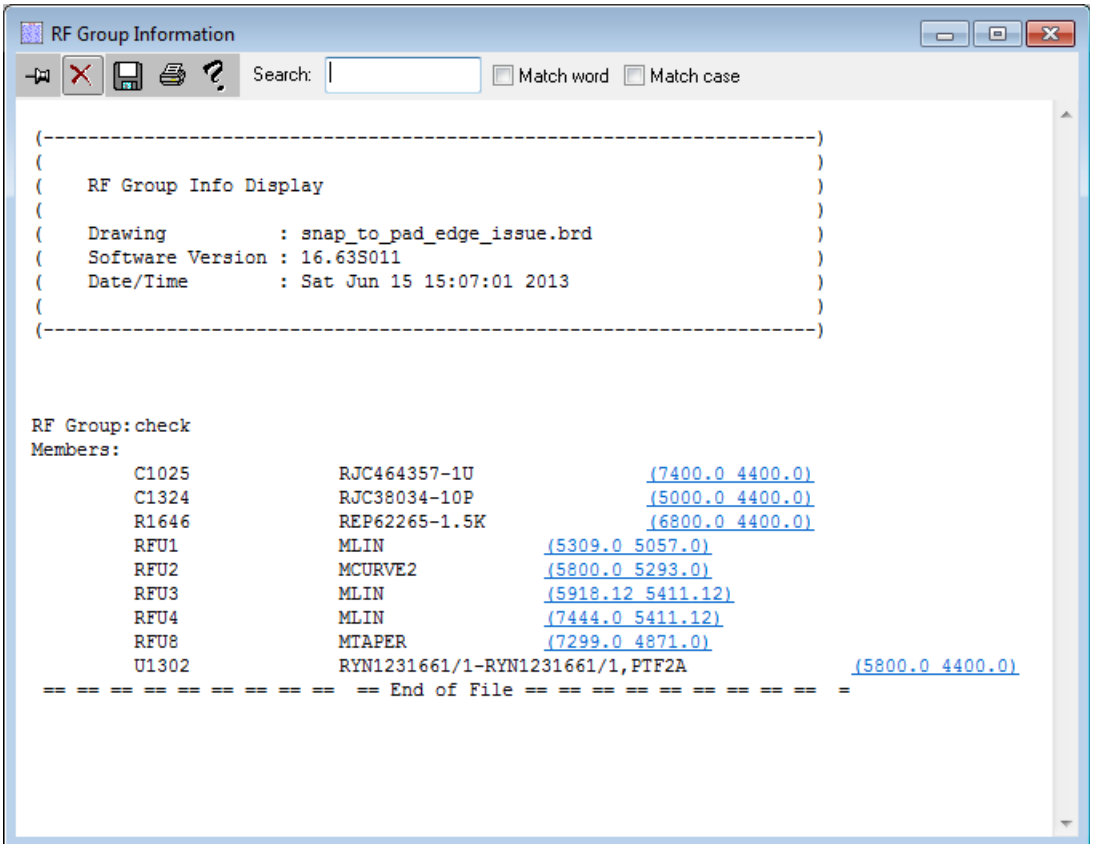
The `rf_group_add` command also generates a generic group and lets you add the selected components to the group.

If a generic group with the same name already exists, a warning message is displayed.

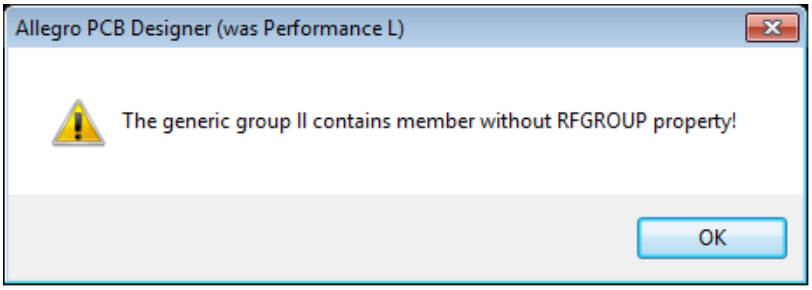


The grouping functionality lets you exclude components from any group, and disband any or all the groups by removing RFGROUP property from each component of the group. In such case, the components are removed from the generic group as well.

You can also see the information of any or all the RF groups using RF Display group command. A dialog box appears which has detailed information of all the group members as shown in following figure.



If any component is added to the generic group, a warning message is displayed.



Marking components and groups

Clicking on a placed component or group highlights it on the board.

Table 2-1 shows the icons for different groups and components. Placed components and groups are indicated with a “P” mark on the icons. The icon is displayed in blue color for the components and groups that have inconsistent parameters and are out-of-sync with their placed symbols. Autoplaced groups and components are indicated with a “A” mark on the icons.

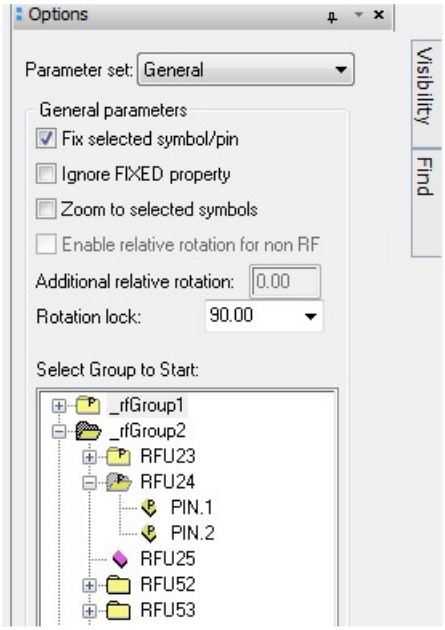
The list of groups in the tree view is also updated when a group is placed. The unplaced groups are sorted first. Rest of the groups are sorted in an alphabetic order.

Table 2-1 Icons for groups and components

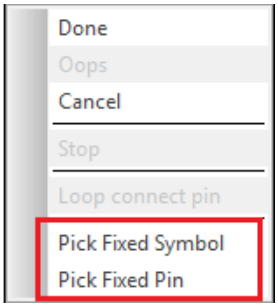
	Unplaced and closed group
	Unplaced and open group
	Unplaced component
	Placed and closed group
	Placed and open group
	Placed component
	Autoplaced and closed group (in green)
	Autoplaced and open group (in green)
	Autoplaced component (in green)
	Out-of-sync group/component (in blue)

Autoplace with Fix Selected Symbol/Pin

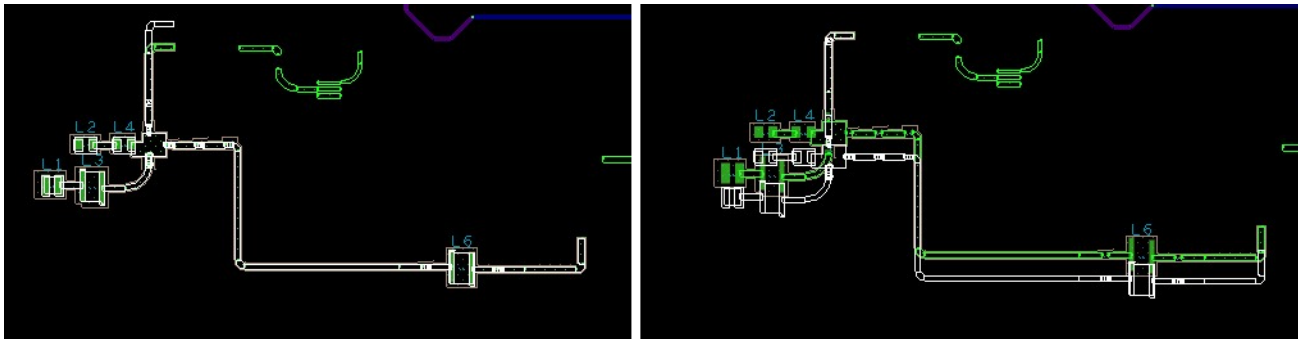
The placed components in the component group list are displayed with their pin numbers.



You can select a component or component pin from the GUI or from the right-click pop-up menu.



The cursor dynamics are updated with the selected component or component pin fixed at their placed position and other parts are shifted.



Autoplace with Clearance Assembly

Placed RF components are related to clearance assemblies. When you autoplace an RF component, the related clearance assembly is taken into account. There are two cases:

- If the *Fix selected symbol/pin* option is enabled.

The symbol of the selected RF component is either deleted or regenerated. However, the RF symbol is still associated with the same clearance assembly. You should run *Clearance - Initialize* command to update the clearance.

- If the *Fix selected symbol/pin* option is disabled.

The symbol of the selected RF component is either deleted or regenerated at another location. However, the RF symbol is still associated with the same clearance assembly. If all the RF symbols related to the same clearance assembly are part of the group for autoplacement, then all the members of the assembly are transformed to the new location Otherwise, all the members of the Clarence assembly stay at the same location.

Retaining Autoplacement Settings

The autoplacement command retains following important settings:

- Fix selected symbol/pin
- Include components in modules
- Ignore FIXED property
- Zoom to selected symbols

- Enable relative rotation for non RF
- Additional relative rotation
- Rotation lock
- Exclude DC nets
- Net exceptions list
- Ignore IC components
- Ignore IO components
- Ignore discrete components

When the command is finished, save the design to store the above settings as a design attachment. When you relaunch the `rf_autoplace` command the settings are restored.

Handling NET_SHORT property

Once the autoplacement is finished, the command checks the NET_SHORT property on all discrete pins in the design and update it as follows:

- If a discrete pin connects to the nets defined by NET_SHORT property, the NET_SHORT property remains unchanged.
- If a discrete pin connects to either one or zero net, the NET_SHORT property is removed.
- If a discrete pin connects to more than one nets, the NET_SHORT property is updated with the current connected nets.

For further details, see the `rf_autoplace` command in the *Allegro PCB and Package Physical Layout Command Reference*.

RF Quickplace

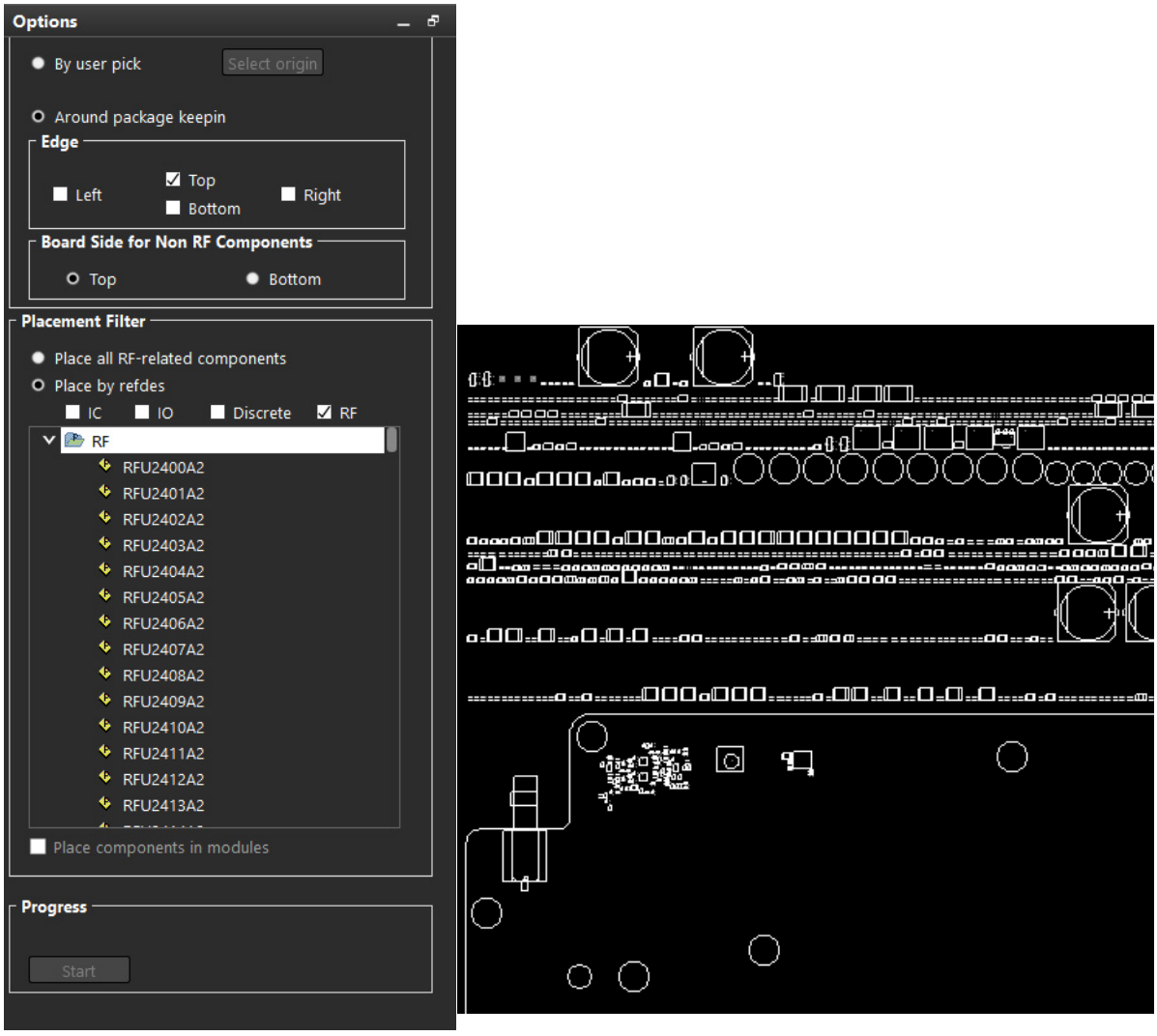
The RF Quickplace feature lets you easily add unplaced RF components to the board design. You place logic bearing RF symbols at a specified point or outside the board outline. The placed components create a palette of symbols that you can view, filter, and move into the design.

You can also quickly place the components contained in the modules by enabling the *Place components in modules* checkbox.

Choose *RF-PCB – Quickplace* (`rf_quickplace` command) to filter components to place at a specified point or on the outside edges of the board outline.

Note: You need to define the board geometry outline before using RF Quickplace.

Figure 2-2 RF Quickplace

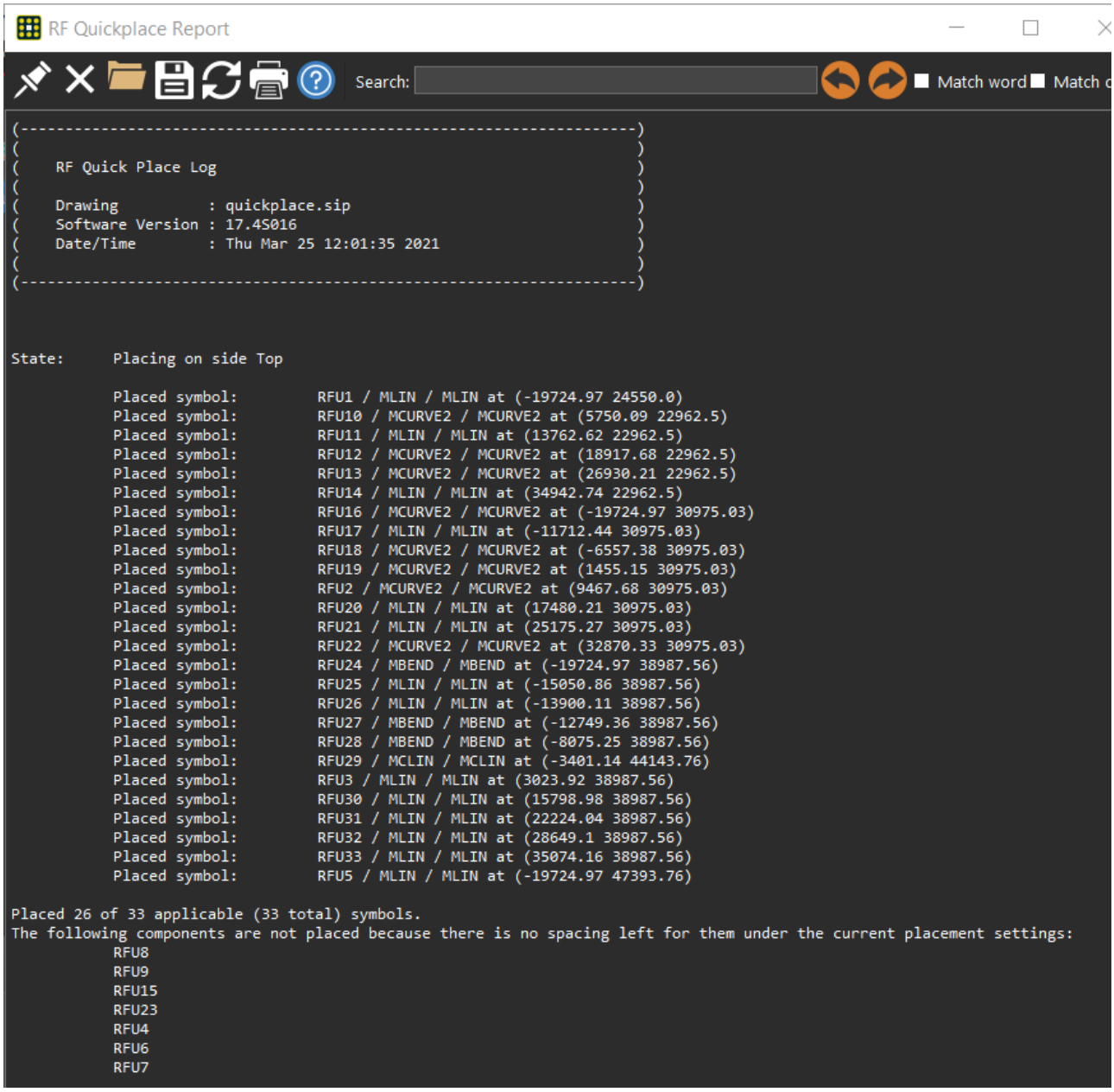


The layout editor places components in a non-rotated state along the edge of the board geometry boundary or at a point specified by you. If quickplace does not detect a board or substrate outline, the command changes to *By user pick* mode to continue with quickplace operation. If the boundary is not rectangular, Quickplace creates a minimum outside rectangle (not a design element) whose minimum and maximum extents are the outer edges of the boundary geometry.

As shown in Figure 2-2 the selected components are placed around the Top and Right edges of the package keepin. For easier understanding, the quickplaced components are highlighted in red, using the RF-PCB Display option (*RF-PCB — Display — New Components*).

When the process is complete, a RF Quickplace report displays. A sample is shown in Figure 2-3. If there is not enough space to place all the components, a message is displayed in the log file.

Figure 2-3 RF Quickplace report



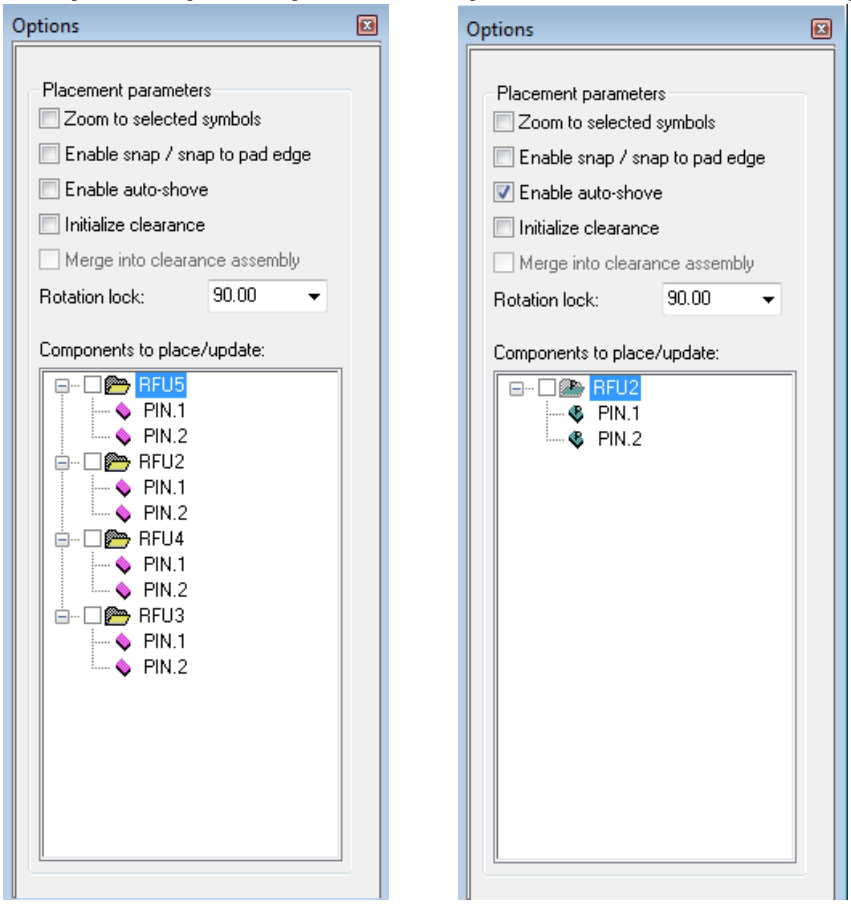
RF Manualplace

The RF Manualplace command lets you interactively place revised or unplaced RF components to the board design. Revised components are placed components with some parameters changes but not updated in the design.

Placed components are indicated with “P” mark on the icons.

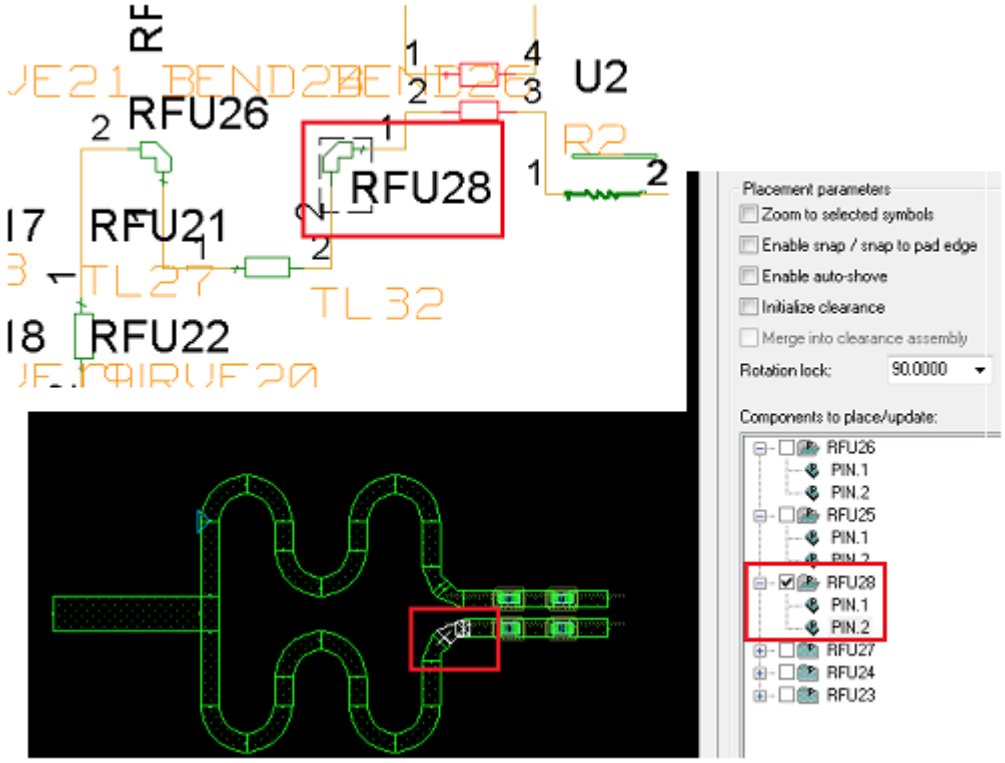
Choose *RF-PCB – Manualplace* (`rf manualplace` command) to manually place components.

Figure 2-4 Manualplace Options pane for Unplaced and Revised Components



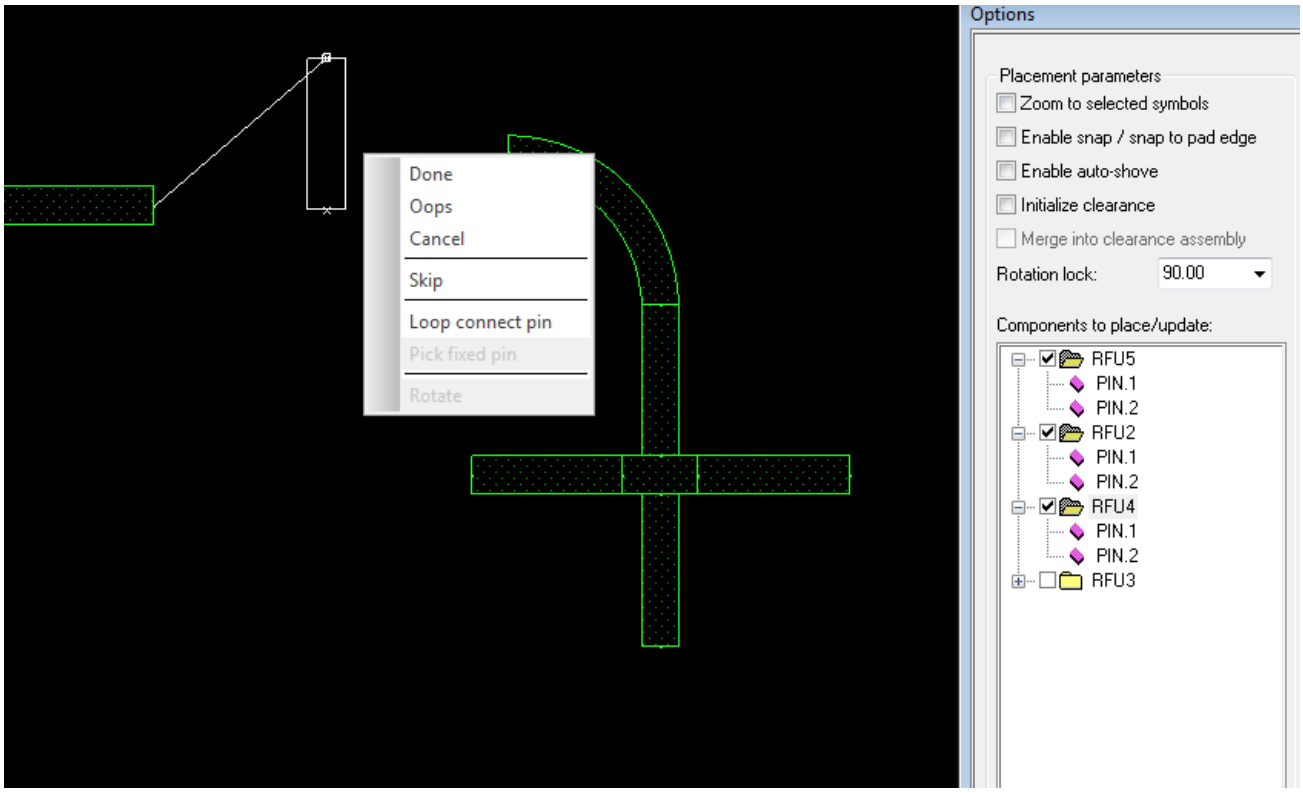
To start manual placement, you can select any of the pins of a revised or unplaced component. By default, pin1 is selected. To select a different pin you can either use right-click pop-up menu or the *Options* pane. You can select multiple components to update or place from the list and update/place them sequentially.

The cross-probing feature between schematic and layout editors lets you pick the component directly from the schematic.



Once you select a component, the component is attached to the cursor, the cursor dynamics changes and displays the outline of the attached component.

Figure 2-5 Placing Unplaced Component



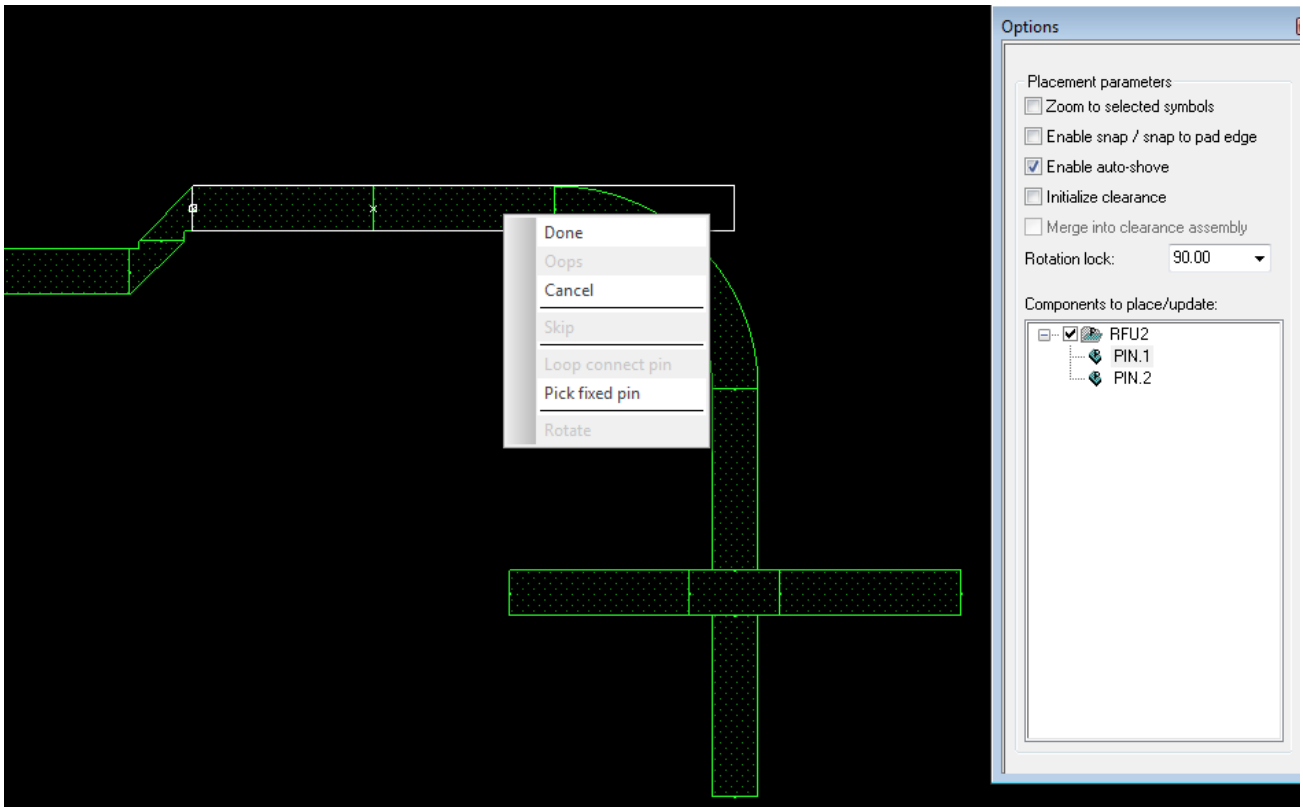
Before placing the component you can perform following actions:

- rotate the unplaced component before picking the destination
- skip the current component and select the next, if multiple components are selected
- select the start pin

If you select other component from the list, the placement for the current component is cancelled.

To update an existing component, select it from the list, the cursor dynamics displays the outline of the component. You can also change the fixed pin from right-click menu.

Figure 2-6 Updating Revised Component



Clicking on the design confirm the update process.

Snapping during Manual Placement

The snapping features work in the following two ways:

- When placing components – allows close connection between the components and the etch objects
- When shoving etch objects after components are placed or updated – allows interactive shoving of etch objects

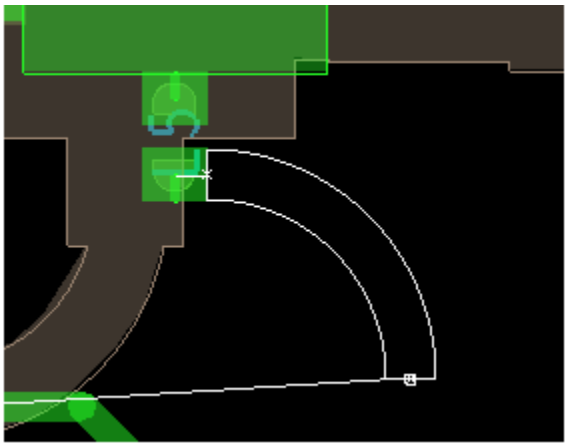
Snapping before Component Placement

The following etch objects support snapping before component placement:

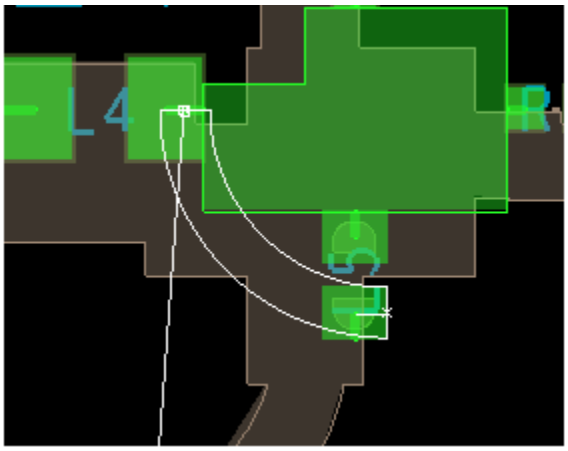
- symbols – snapping to pad edge of the nearest pin of a non-RF symbol.
- pins – snapping to pad edge of the selected pin of a non-RF component.

- vias – snapping to the via location
- clines – snapping to the nearest end point of the selected segment of the cline
- shapes – snapping to the nearest edge point of the shape

The following illustrations shows an example of snapping to pad edge in outward and inward directions.



Outward



Inward

Snapping after Component Placement

Snapping is performed after component placement/update only if *Enable auto-shove* option is checked. You can snap only those etch objects that are not physically connected to the placed/updated component.

Auto-shoving during Manual Placement

You can use auto-shoving in following two ways:

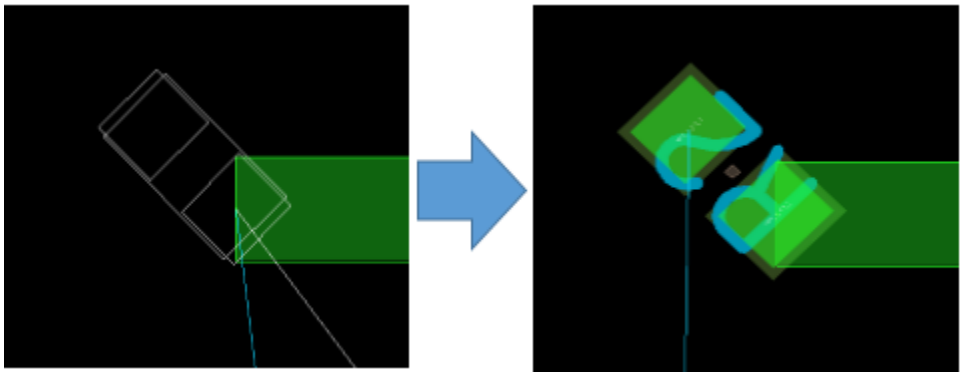
Auto-shoving of Connected Etch Objects

Auto-shoving moves/rotate the etch objects that are already connected to each pin of an updated component and maintains the physical connection.

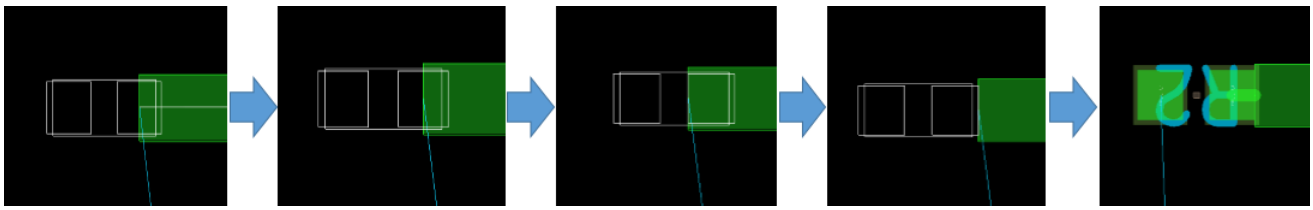
Auto-shoving of Non- Connected Etch Objects

Non-connected etch objects have logical relations with the placed or revised component but are not physically connected to it.

If *Enabled snap/snap to pad edge* is not checked, auto-shoving is performed without snapping on the non-RF component. You can auto-shove by specifying the rotation angle of a non-RF component. The following image illustrates the steps for auto-shoving when snap is disabled.



If *Enabled snap/snap to pad edge* is checked, auto-shoving is performed with snapping to pad edge of the pin of a non-RF component. You can auto-shove by specifying the rotation angle of a non-RF component and then snap to pad edge of the pin of the non-RF component. A small cline segment is automatically added to connect the pins of RF and non-RF components. The following image illustrates the steps for auto-shoving when snapping is enabled.

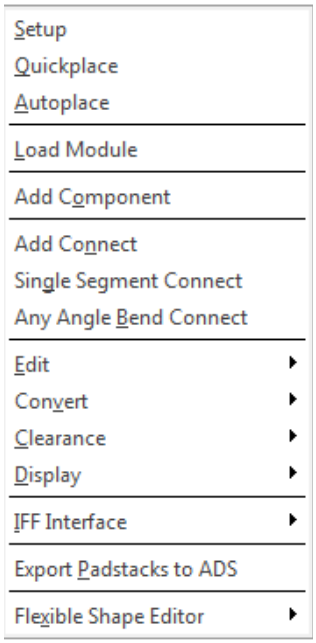


The snapping point is calculated from the connection point of the RF component and does not dependent on grid settings.

RF Add Component Command

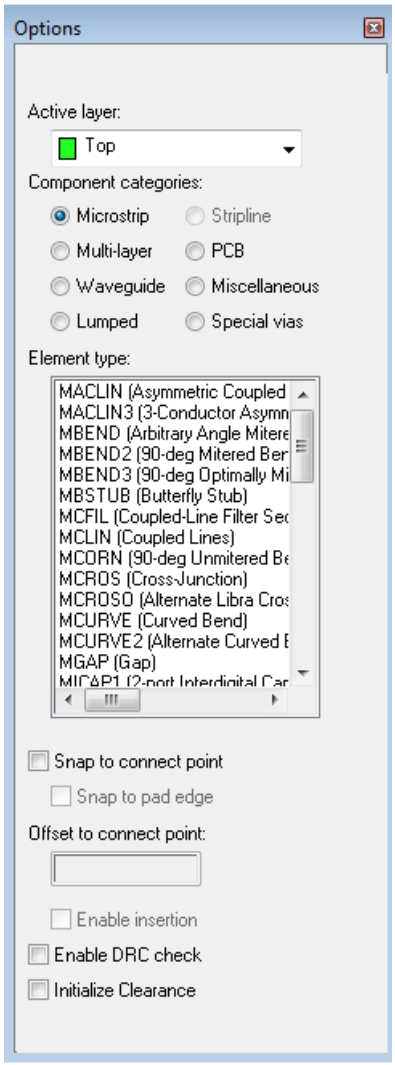
Create an RF component in your design using the RF Add Component command. Choose *RF-PCB — Add Component* to access the command option shown in Figure 2-7.

Figure 2-7 RF Add Component Menu



When you start the *Add Component* command, the Options pane in Figure 2-8 displays.

Figure 2-8 RF Add component Options pane



RF Components

Component Classification

RF PCB provides the following component categories:

- Microstrip
- Stripline
- Multi-layer
- Printed Circuit Board (PCB)
- Waveguide
- Miscellaneous
- Lumped
- Special Vias

Microstrip, Multi-layer, Waveguide, PCB, Lumped, Special via and Miscellaneous components can be placed on outer (top or bottom) layers of the board. Stripline, Multi-Layer, Special via, PCB and Miscellaneous components can be placed on inner layers.

Important

Only create PCB components in designs with eight or less layers. If you design exceeds eight layers, then PCB components are unavailable.

If you use fixed component footprints selected from other libraries instead of `rf_comp_lib`, no RF properties are attached. Therefore, RF PCB considers them to be non-RF components.

Creating an RF Component

Create an RF component using the Add Component options as shown in Figure 2-8. You first choose the layer you wish to place the component on followed by a component category. You then select a component type from the Element type list. When you select the type, an instance of the component is attached to your cursor.

When ready to place the component, drag the instance to its destination and click to anchor it. At that point you can rotate it about its anchor (origin) point.

You can enable *Snap to connection poin*t and then specify a *Offset to connect point* to help you in placing the component. You can enable DRC checking and if placing the component results in a violation the component is not placed. You can create default clearance shapes for the RF component and add them to an existing clearance assembly. You can also insert the selected RF component between two connected RF components on your canvas by choosing the Enable insertion option.

Tip

To view a Component-specific dialog box to enable you to change the default parameters and assign nets to component pins, right-click on the component and choose *Show/Hide GUI Form*.

Click again to fix its final orientation. Figure 2-9 depicts the component creation process.

The right mouse button menu provides options for enhanced placement and editing of RF components:

- Loop Pin Forward
- Loop Pin Backward
- Pick Connect Pin
- Flip Symbol
- Snap to

The *Loop Pin Forward* and *Loop Pin Backward* options available from the right mouse button menu of each enhanced RF command let you more precisely determine the physical positioning of the symbol. Connect pin logic inherits from the connected object and fixes at the first pin of the component. When the connect point is not the first pin, you can use *Loop Pin Forward* and *Loop Pin Backward* to change the pin to the connect point. The net logic and symbol rotation also change.

Each time you use these options, the pin at the connect point shifts to the next one of the RF component. When you reach the last pin, the function swaps to the first one and begins another loop session. *Loop Pin Forward* and *Loop Pin Backward* actions change the net of the pin at the connect point and update the net. The net of the pin does not change if there are no objects connected at the connect point.

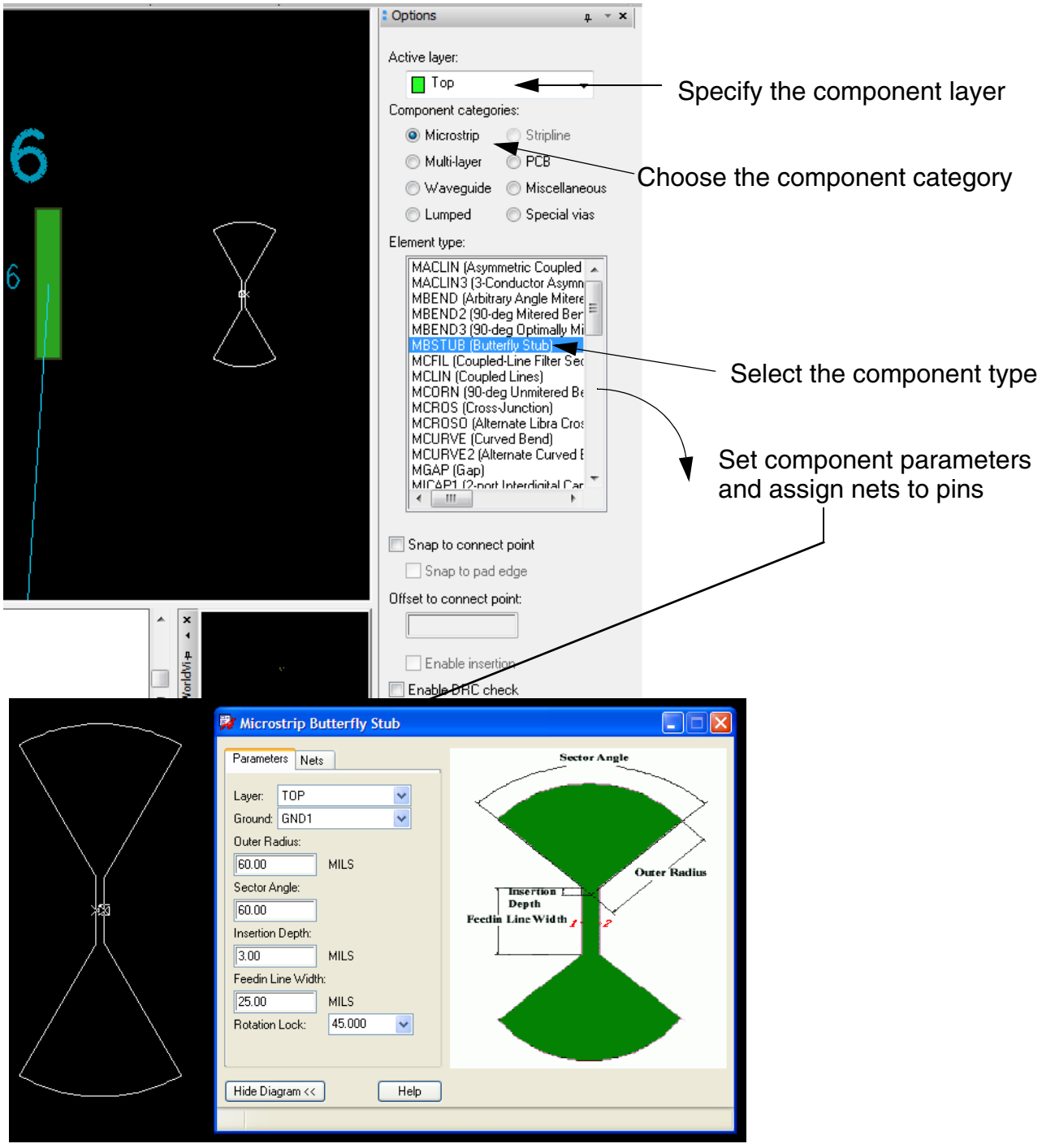
You can see the effect caused by pin looping in the updated cursor dynamics of the component. The connection point at `pin 1` is marked with a cross in a square. Other connection points are marked with only a cross.

Pick Connect Pin option allows you to directly pick the desired connect pin of a multi-pin RF component.

The *Flip Symbol* option lets you change the flip mode as long as the pin to connect point is fixed.

For snapping information see the *Allegro User Guide: Getting Started with Physical Design*.

Figure 2-9 Creating an RF Component



For further details on how to change component parameters, assign nets to pins, and place components in your design, see the procedures for the `rf_add_component` and

`rf change` commands in the *Allegro PCB and Package Physical Layout Command Reference*.

3

RF Routing

- Overview
- Setting Up for Routing
  - Choosing a Route Mode
  - Routing Setup
- Setting Up for Routing
  - Extended Route Options
  - Starting from a New Point
  - Starting from a Component Pin, Via, Cline, or an Etch Shape
- Routing an RF Trace or Meander with Components

Overview

You can route RF traces with different bend types directly within Allegro PCB Editor. Each trace and bend is considered an RF component. As you route a trace, you can conveniently insert other RF components in-line, such as transmission line components.

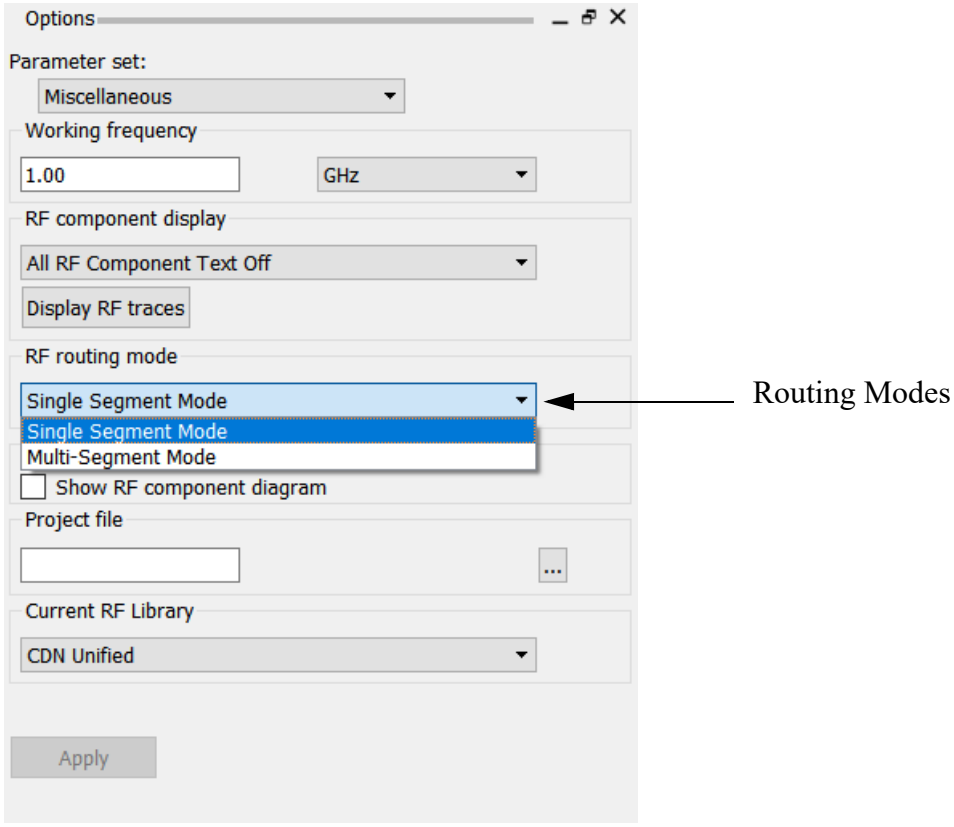
Setting Up for Routing

Choosing a Route Mode

There are two RF route modes; single segment and multi-segment. If you choose *Single Segment Mode*, the routing operation only allows you to route one trace segment at a time, alternating between straight segments and bends. If you select *Multi-segment Mode*, you can conduct an RF routing operation that includes several trace segments and bends in a heads-up display as you route.

You set the route mode by choosing *RF-PCB – Setup*. The RF Setup dialog appears as shown in Figure 3-1. Select the *Miscellaneous* tab, then click on the *RF Routing Mode* down-arrow to choose the desired mode.

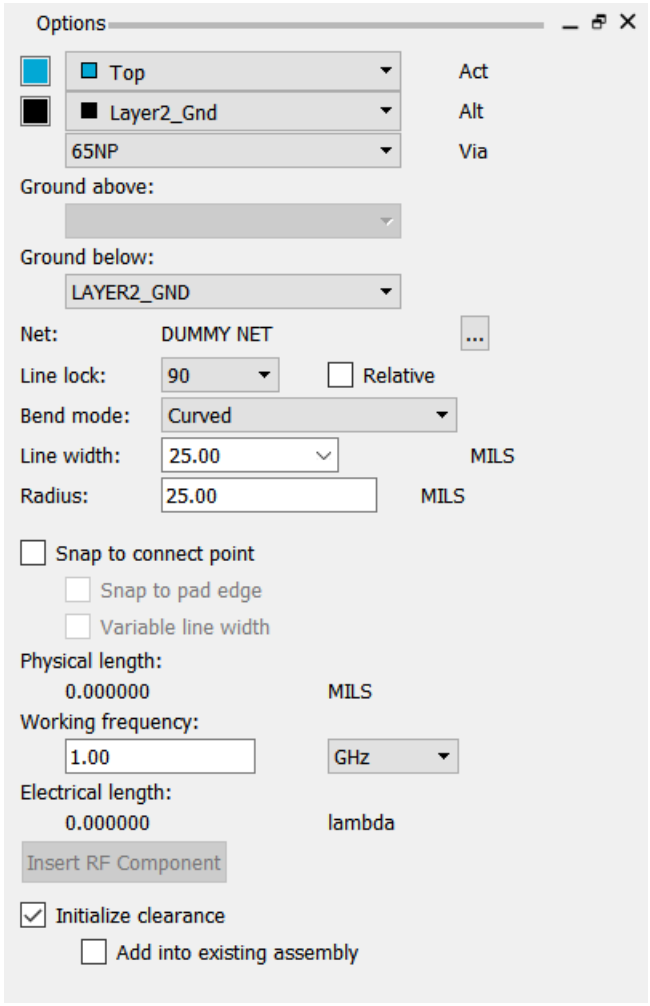
Figure 3-1 Route Mode Setting



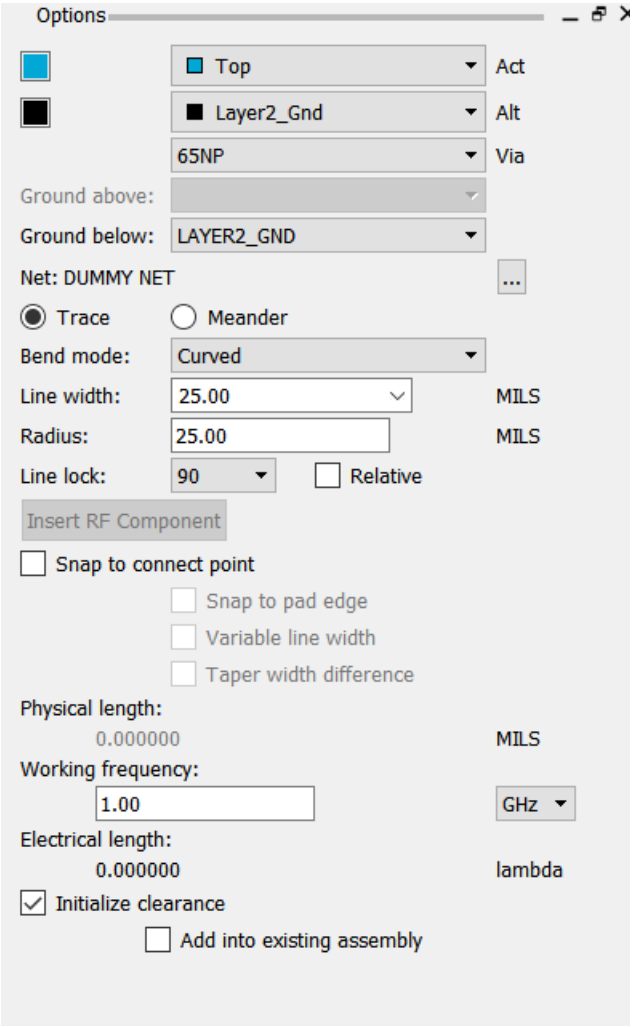
Routing Setup

Before you route RF traces, you need to perform some initial setup. Choose *RF-PCB — Add Connect* to access the options shown in Figure 3-2. Enter appropriate values for all routing parameters, then begin routing your trace. For further details on the routing parameters, see the Options pane description for the `rf add connect` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Figure 3-2 RF Add Connect Options pane (single line and multi-segment modes)



Single segment mode options



Multi segment mode options

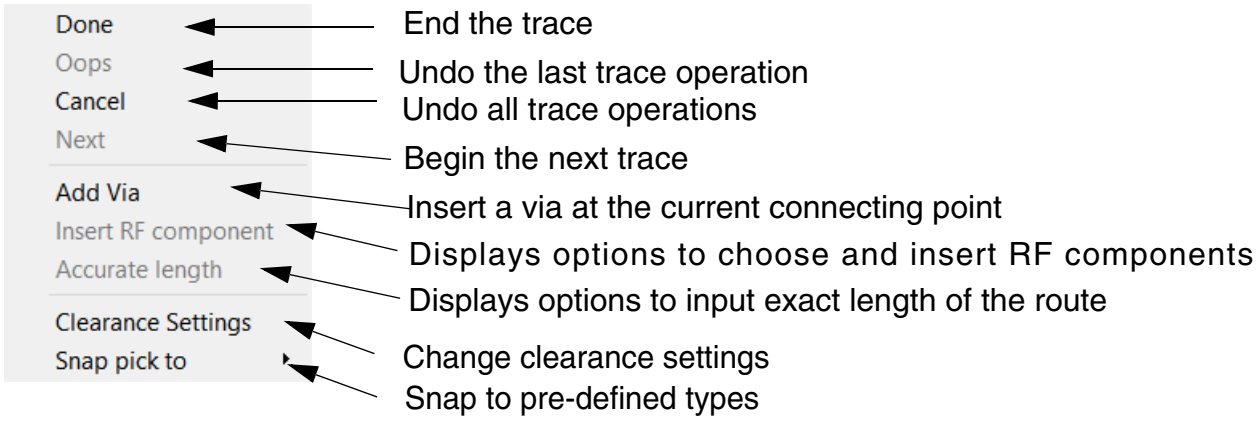
Routing an RF Trace or Meander

Once values have been entered for parameters in the Add Connect options pane, start routing your trace by locating your cursor and clicking the left mouse button. For specific details on how to route a trace, see to the procedures for the `rf_add_connect` command in the *Allegro PCB and Package Physical Layout Command Reference*.

Extended Route Options

As you route the trace, you can press the right mouse button to access the extended command options shown in Figure 3-3.

Figure 3-3 Route right mouse button menu



Starting from a New Point

If you start routing a trace from a new point (as opposed to an existing pin), a net name is assigned to the starting pin. You can change it manually. As you route, the physical length of the trace displays in the options pane. If you specify a working frequency for the trace before routing, the electrical length displays as well.

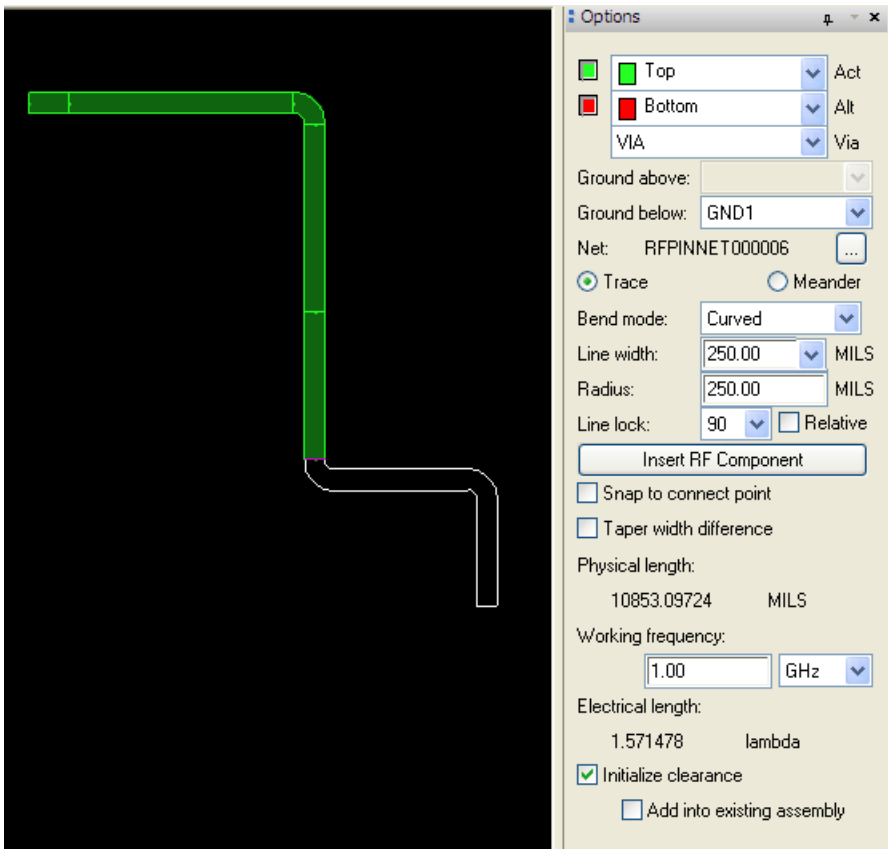
Note:

- Only *consecutive* RF traces and bends are used in length calculations. Other (non-RF) components are ignored when detected and cause length accumulation for a following trace to begin at zero.

- You cannot change the working frequency while routing a trace. However, you can change it just prior to routing the next trace (after selecting *Next* from the right mouse button option menu).

Figure 3-4 shows an example of an RF trace routing from a new point.

Figure 3-4 Routing from a New Point



Changing line width while routing

You can change the line width value while routing a trace. When RF routing command starts, the tool loads the stored line-width values from the design into the line width drop-down list. Each of the new values for line-widths are saved in the drop-down list for quick reference.

When the routing is completed, all the line-width values are stored to the global RF setting attachment for further usage.

Starting from a Component Pin, Via, Cline, or an Etch Shape

You can click on an existing object to begin routing your trace. In this case, only component pins are used for the start and end points of the trace. When you select the first component, the pin position nearest your cursor is used as the starting point. The location and direction attributes of the pin are used and its net name is also assigned to the first pin of the trace component.

The starting point on a cline is the vertex closest to the mouse pick.

The starting point on an etch shape is the nearest point on the boundary edge of the shape. You cannot start routing from an arc segment on a shape. The routing direction is perpendicular to the outside of the shape.

Note: If the component selected happens to be an RF trace, the physical and electrical lengths of that trace are included in the total length calculations for the entire trace.

Figure 3-5 Routing from a cline

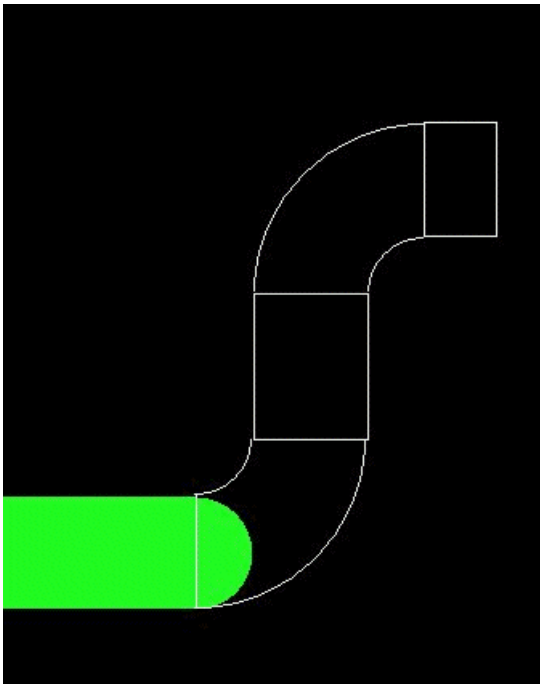
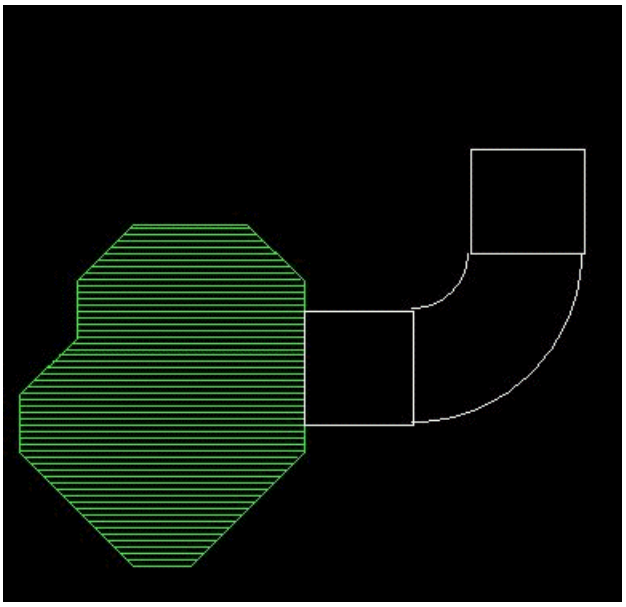


Figure 3-6 Routing from an etch shape

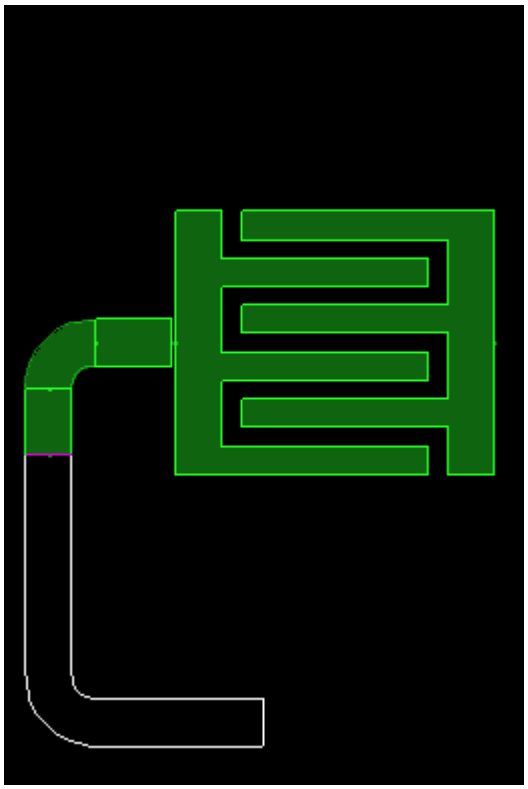


Changing the Trace Width

After you have routed a trace segment, you can change the width of the trace by choosing *RF-PCB — Edit — Change.*

Figure 3-7 shows an example of an RF trace routing from a component pin.

Figure 3-7 Routing from a Component Pin



Snapping to a connect point

For ease in connecting two existing RF components with an RF trace or to resolve a ratsnest, you can check *Snap to connect point* when setting routing parameters in the Options pane. The tool then automatically calculates a path to the next available destination point. If the destination point is a connect pin, the trace snaps the trace to the correct entry orientation. The following examples illustrate the snapping mode in range and out of range.

Figure 3-8 Snapping to a connect pin within range

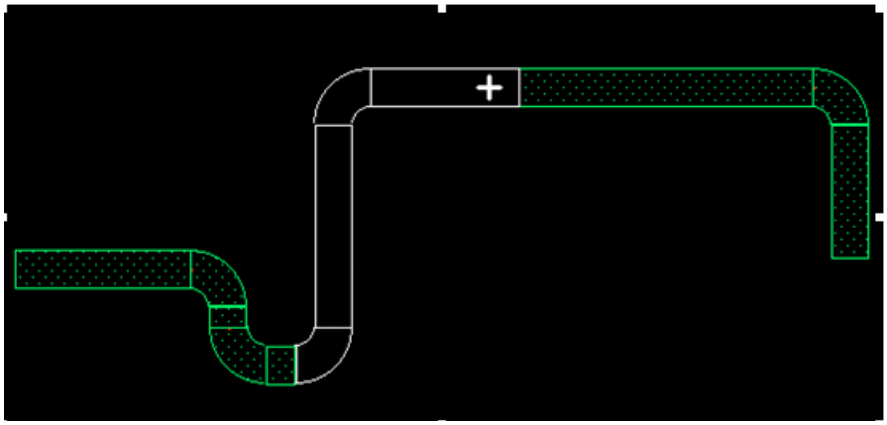
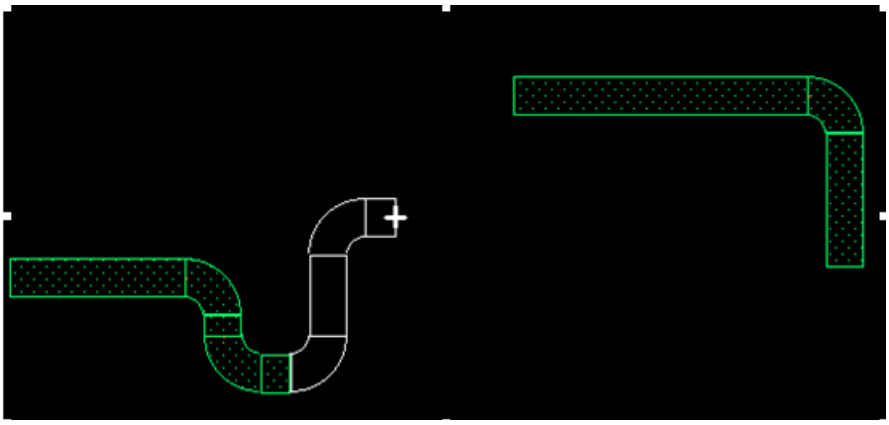


Figure 3-9 Snapping when no connect pin exists in range



When no connect pin exists in range, the tool uses the current mouse location for the destination of the trace and displays a possible route for you to use to create an extra trace to complete the connection.

Figure 3-10 Snapping when no dynamic path is possible at the mouse location

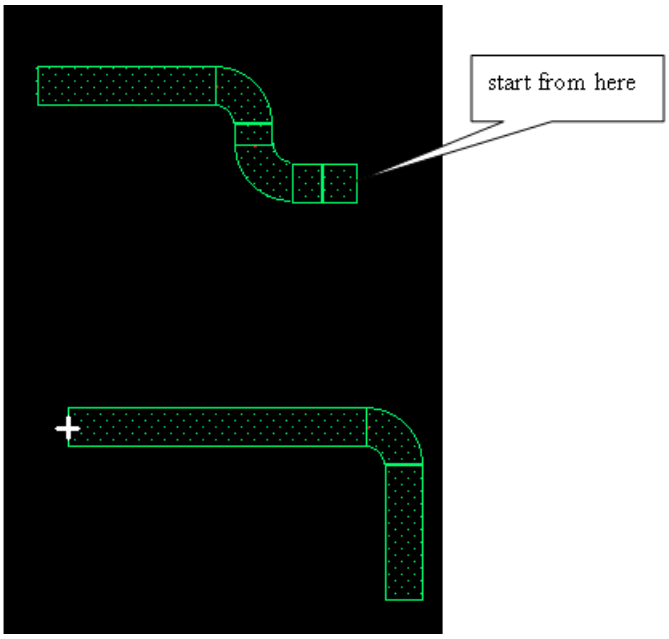
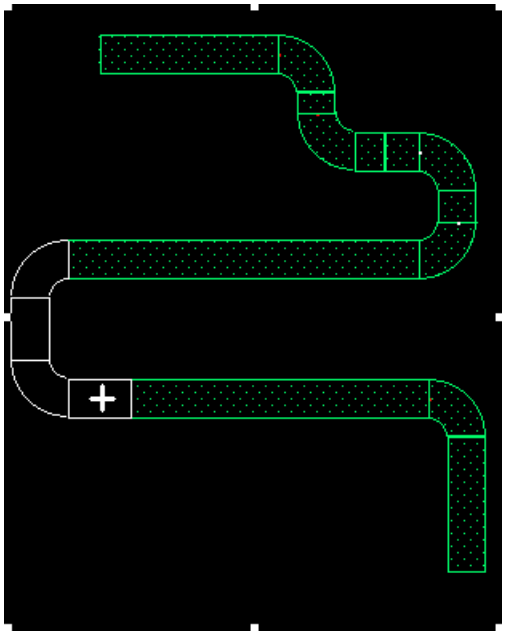


Figure 3-11 After routing an extra trace, you can complete the connection



Routing with an interface pin of module

You can now route from an interface pin of a module instance. The interface pin is the pin which serves as an interface to connect to objects outside the module instance.

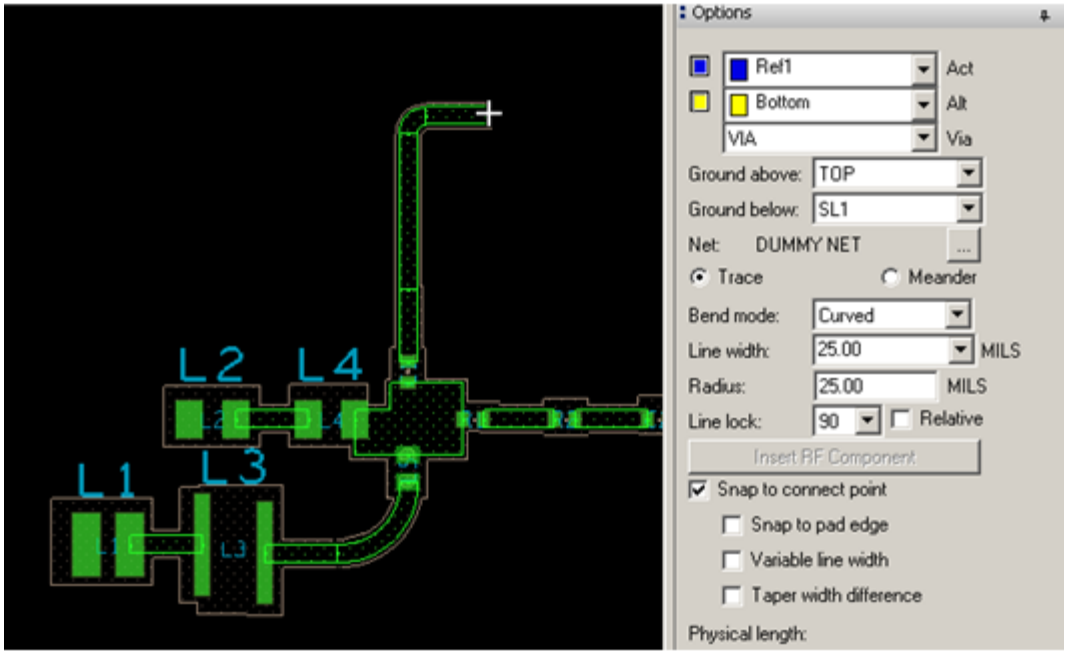
Automatic layer selection

While routing with *Snap to connect point*, the tool automatically selects a proper routing layer. Supported objects for snapping are:

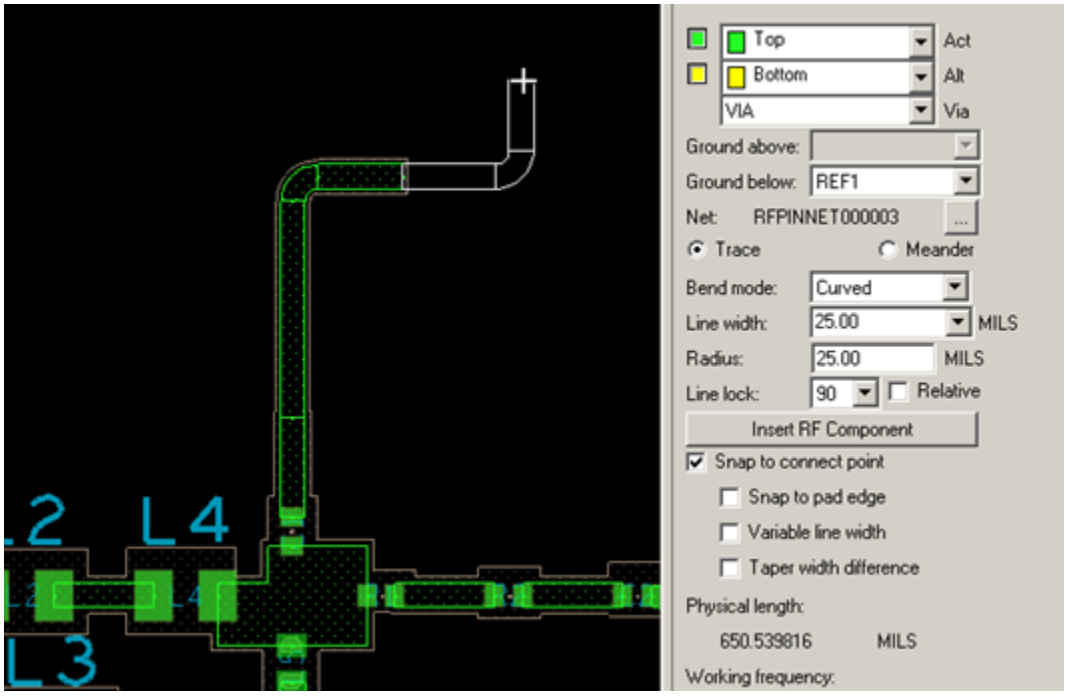
- Symbol
- Pin
- Etch path
- Etch shape
- Via

If the selected routing layer does not match with the current active subclass, the tool automatically updates the active subclass, alternative layers, ground layers and some of the other global RF parameters.

In the following figure, the active subclass is REF1 and no object is selected.



After selecting symbol Rfu15, the routing starts from the RF pin on TOP layer and the other options are also changed.



Layer Selection Criteria

When you start a routing and choose object for snapping, a set of nearby objects are selected and stored in following order:

Symbols, pins, etch paths, etch shapes, vias

The automatic layer selection is based on above priority order. Following table shows list of layers selected for different objects:

Object	Supporting Object	Candidate layer
Symbol	symbol	use nearest pin to the pick point
RF pin	pin	use pin layer
Non-RF pin	path/shape	use path/shape layer
	RF pin	use pin layer
	non-RF SMD pin	use pin layer

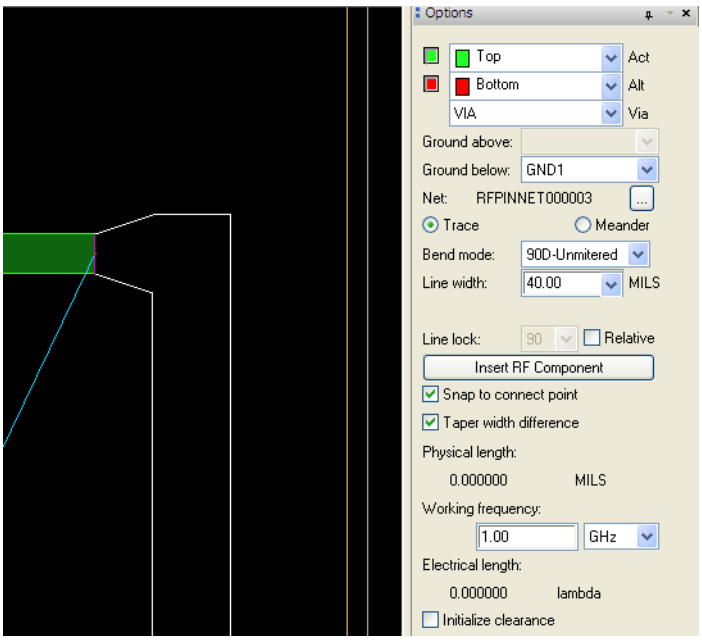
Object	Supporting Object	Candidate layer
	non-RF through pin	use topmost layer of cline/shape, if pin is connected to any cline/shape
		use topmost pin layer, if pin is not connected to any cline/shape
	blind-buried via	use topmost layer of cline/shape, if pin is connected to any cline/shape
		use topmost pin layer, if pin is not connected to any cline/shape
	via	use topmost layer of cline/shape, if via is connected to any cline/shape
		use topmost via layer, if via is not connected to any cline/shape
Etch path	path	use path layer
Etch shape	shape	use shape layer
Via	path/shape	use path/shape layer
	RF pin	use pin layer
	non-RF SMD pin	use pin layer
	non-RF through pin	use topmost layer of cline/shape, if pin is connected to any cline/shape
		use topmost pin layer, if pin is not connected to any cline/shape
	blind-buried via	use topmost layer of cline/shape, if pin is connected to any cline/shape
		use topmost pin layer, if pin is not connected to any cline/shape

Object	Supporting Object	Candidate layer
	via	use topmost layer of cline/shape, if via is connected to any cline/shape use topmost via layer, if via is not connected to any cline/shape

Using Taper width difference

For connecting two existing RF components with different widths you can enable *Taper width difference option* along with the *Snap to connect point* when setting routing parameters in the Add Connect Options pane. The tool then automatically calculates and adds a taper to the connection.

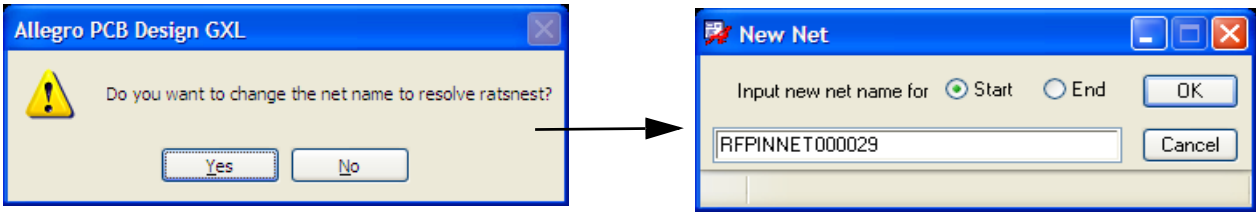
Figure 3-12 Using Taper width difference



Resolving ratsnest

If during the rf_add_connect the nets at the start and end of an RF trace are the same, the tool prompts if you want to resolve the ratsnest and change the net name. Choose Yes and then enter a new name for the net and click OK.

Figure 3-13 Resolve ratsnest



Routing an RF Trace or Meander with Components

You have the option of inserting components in-line as you route an RF trace. The component can be a transmission line component (RF component), or a lumped component.

When you insert a component during trace routing, the following actions occur:

- The component generation options display.
- RF PCB assigns the net name of the trace to the end pin of the component.
- RF PCB matches the active layer of the component to the trace layer.
- RF PCB matches the connection direction of the component to the trace being drawn.

Important

If you insert a component after you've routed a trace, by default, pin 1 of the component is used as the connecting pin.

If you insert an RF trace or bend, its length is added to the total length of the trace.

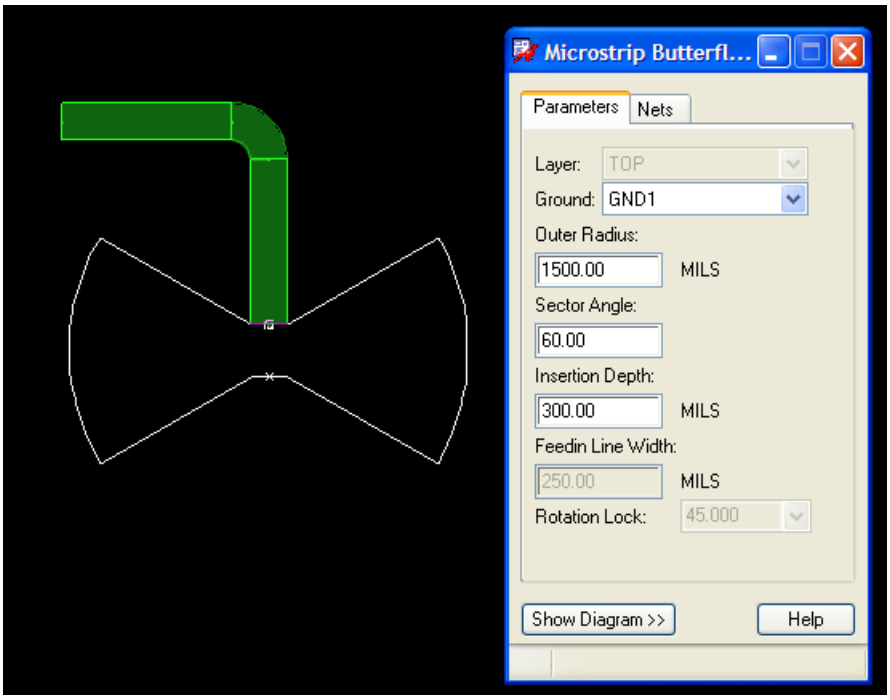
Inserting a Component

To insert a component while routing a trace, click the *Insert RF Component* button in the Add Connect options pane.

Note: If the active layer is top or bottom, you can create any of microstrip, multi-layer, waveguide or miscellaneous components. Otherwise, only PCB and special via components are available.

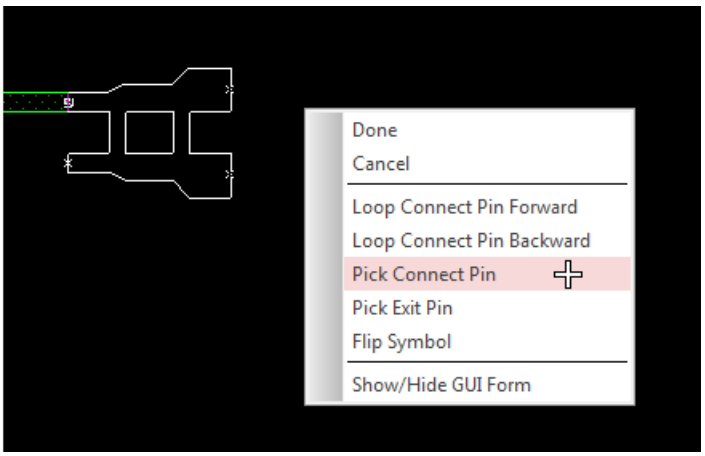
If you've enabled *Show GUI Form* option from the from pop-up menu then after you select a component from the list, a dialog box appears for component generation as shown in Figure 3-14.

Figure 3-14 Inserting a Microstrip Butterfly Component



Change the component parameters in the dialog box as desired and place the component. To change the connect pin, right- click and choose Loop Connect Pin Forward and Loop Connect Pin Backward. The cursor dynamics changes to reflect the selection.

You can also pick the connect pin directly using Pick Connect Pin option, as shown in figure below.



Once the connect pin is selected, choose the pin to continue the route using Pick Exit Pin option.

Note: When routing in Single Segment Mode the next trace segment is added automatically and the trace attributes are carried forward.

Direct Connecting Two Points

You can directly connect two points with a trace by choosing *RF-PCB — Add Connect*. The connect options display in the options pane. You choose parameters for the connecting trace and then click on the two points to connect.

You can directly connect any two points by:

- a straight line
- a meander line
- a specified electrical length

For details on how to direct connect points, see the procedures for the `rf_add_connect` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Connection Criteria

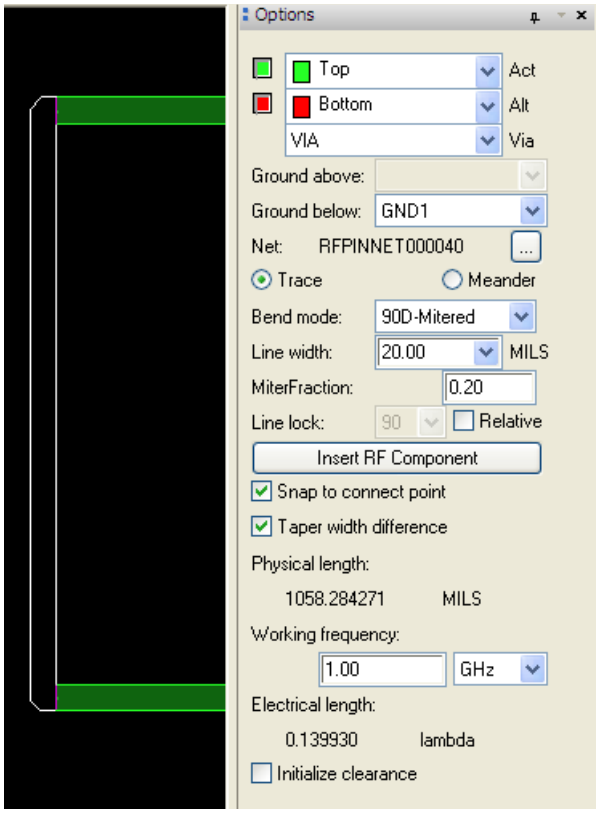
If the active class is not etch, etch / top is used as the default layer for the connecting trace. If you want to use a different layer, you need to change the active class and subclass first. The miter fraction or curve radius are calculated automatically.

If you specify two arbitrary points to connect, a trace is drawn between them without further checking. However, to connect two pins, the net name of the pins must be different and the working frequency and connecting widths of the two components must match before being directly connected together.You can also connect one pin to a shape (a solid shape is recommended).

Interconnecting by a Straight Line

You can connect two points using a straight line plus two bends. Figure 3-15 shows the Interconnection options with *Trace* connection mode specified. If you choose two arbitrary points to connect, a straight trace is generated between them using the line width and bend mode specified. If you choose two pins to connect (same net name, frequency, and connecting width), they are connected together using their existing parameters.

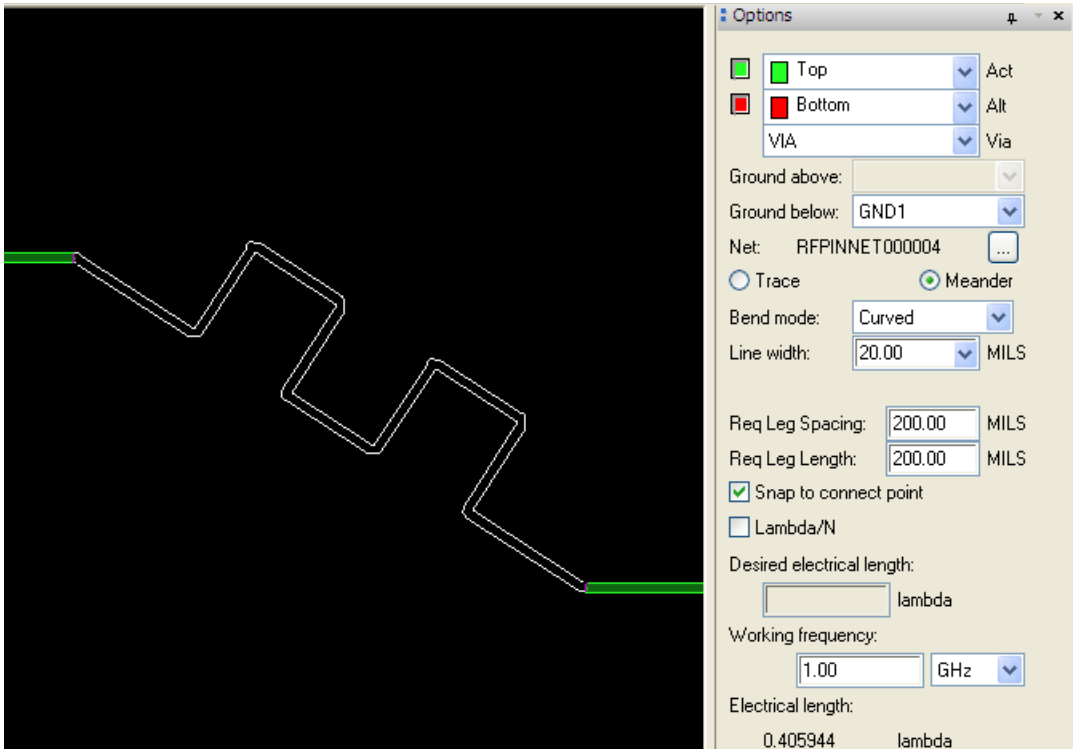
Figure 3-15 Interconnecting two points using a straight line



Interconnecting by a Meander Line

You can connect two points using a meander line plus two bends. Figure 3-16 shows the options pane with *Meander* connection mode specified. If you enter two arbitrary points to connect, a meander trace is generated between them using the line width and bend mode specified. If you enter two pins to connect (same net name, frequency, and connecting width), they are connected together using their existing parameters.

Figure 3-16 Interconnecting two points using a meander line



Interconnecting by a Specified Electrical Length

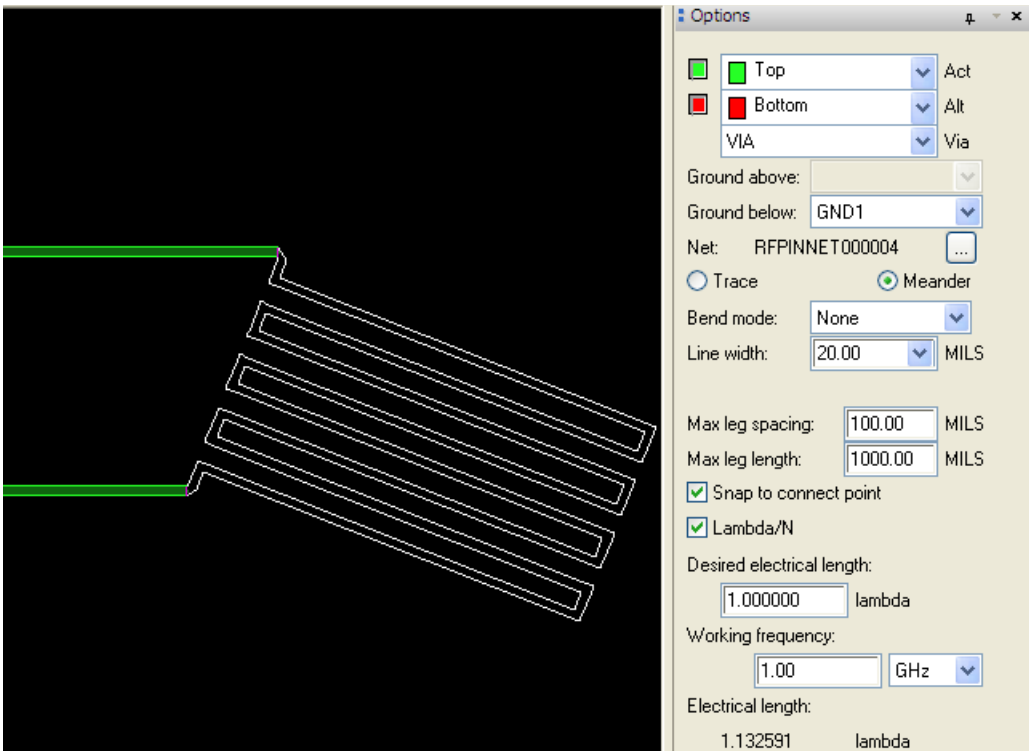
You can connect two points using a specified electrical length with a suitable meander line plus two bends. Figure 3-17 shows the Interconnection options with an electrical length specified.

If you select two pins to connect, and conditions are satisfactory, they are connected together using their existing parameters by a meander and two bends to meet the electrical length. Otherwise, the console window displays warning information. Adjust the connection parameters and try again.

Note: If *Frequency* is set to 0, you cannot specify an electrical length.

In cases where you want to use a meander trace with a specified electrical length to connect two points, the distance between the two points you select is checked. If the *Direct Line Electrical Length* between the two points is greater than the *Desired Electrical Length*, an error message appears and you cannot complete the direct connection. The *Direct Line Electrical Length* field serves as a reference during direct connection.

Figure 3-17 Interconnecting two points using a specified electrical length



4

RF Editing

- Overview
- Changing Component Parameters
- Breaking RF Components
- Snap Connecting an Element
- Deleting RF Components
- Copying an RF Component with a Scale Factor
- Modifying Connectivity of RF Components
- Editing Groups of Objects
- Editing variables imported from an IFF Schematic File

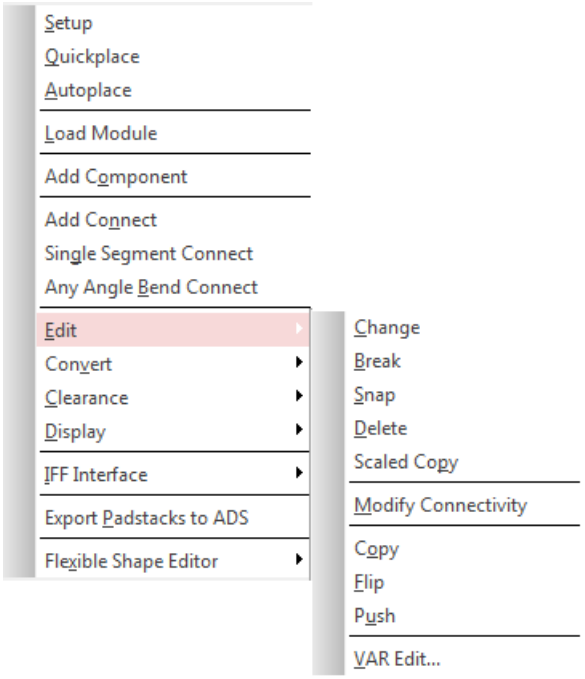
Overview

After you place an RF component or route an RF trace, you can use RF editing commands to:

- change component parameters
- break RF components
- snap RF components
- delete RF components
- copy an RF component with a scale factor
- modify connectivity of components
- copy multiple objects simultaneously
- flip a group of objects
- push groups of RF components up or down layers
- edit variables in an IFF schematic file

Choose *RF-PCB – Edit* to access the command options shown in Figure 4-1.

Figure 4-1 RF-PCB Edit Menu

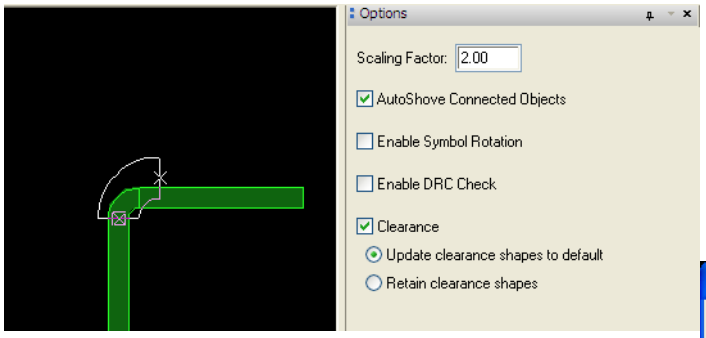


You can also use Allegro PCB Editor commands to move and rotate RF components. For further details, see the `move` and `spin` commands in the *Allegro PCB and Package Physical Layout Command Reference*.

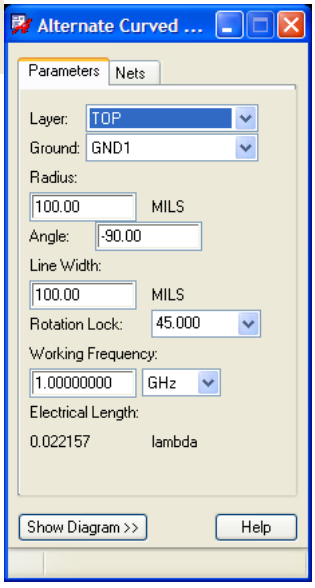
Changing Component Parameters

You can change RF component parameters by choosing *RF-PCB – Edit – Change*. The editing options appear in the Options pane (Figure 4-2). Parameter changes may break existing connections of RF components, so use the *AutoShove Connected Objects* option to keep the components connected after you make the changes.

Figure 4-2 RF Edit Options pane



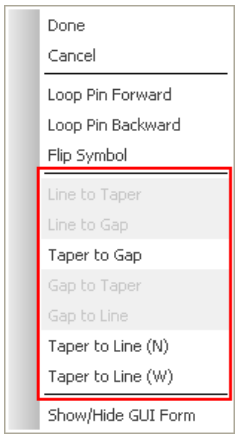
By checking the AutoShove Connected Objects box, the curved line will remain connected when you make parameter changes. Right-click and choose Show GUI Form to edit the parameters.



Click on the RF component in the design that you want to change. Right-click and choose *Show GUI Form*. A component generation dialog box specific to that component appears enabling you to change its parameters. Once parameters have been modified, click on the component again to apply the changes.

You can also change the component type for certain types of RF symbols. In the `rf_change` mode, the right-click menu displays the change type options available for the selected RF component. Notice that the available conversion options will depend on the type of object selected.

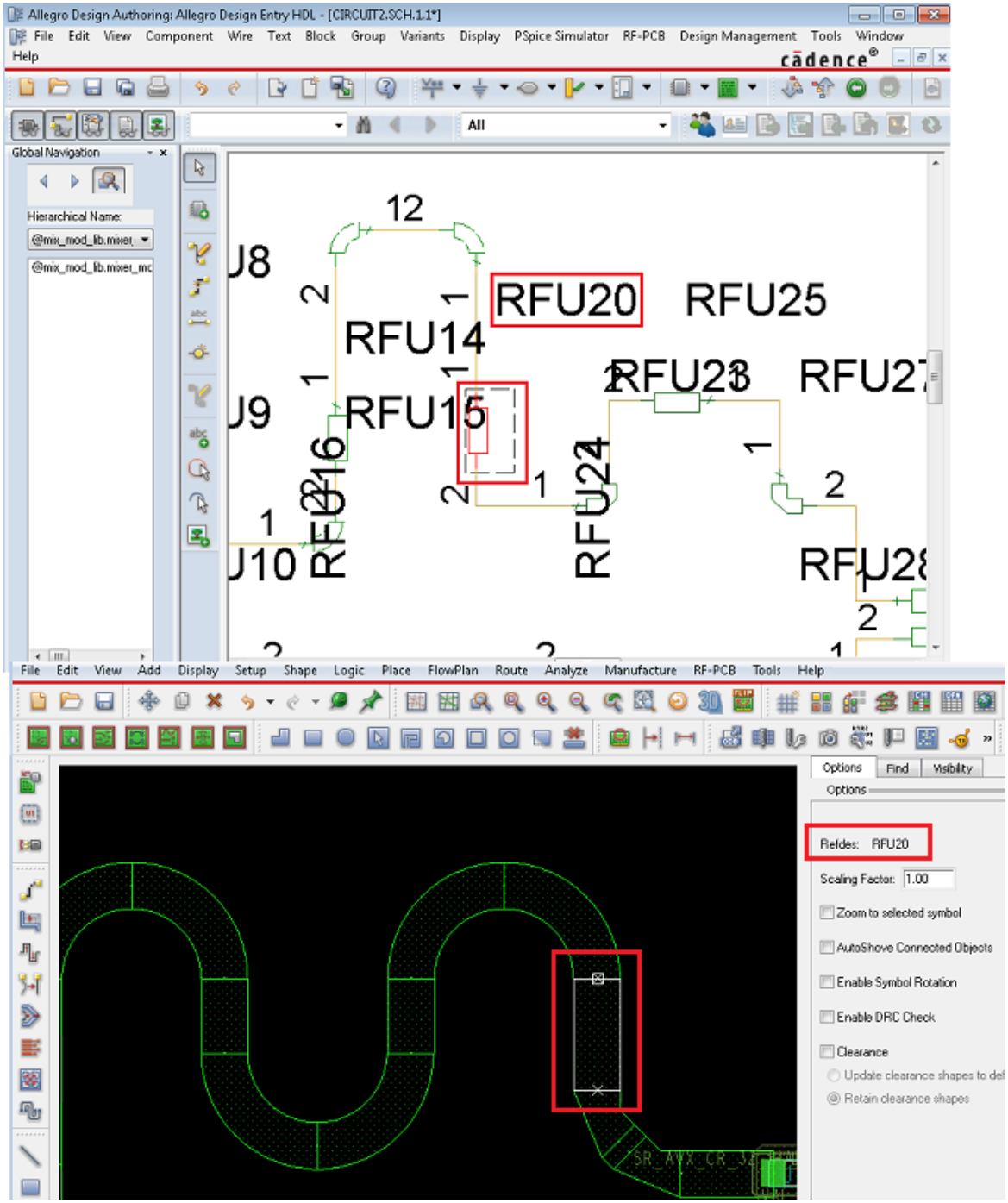
Figure 4-3 RF Type Conversion options



Note: You cannot use this command to change non-RF components.

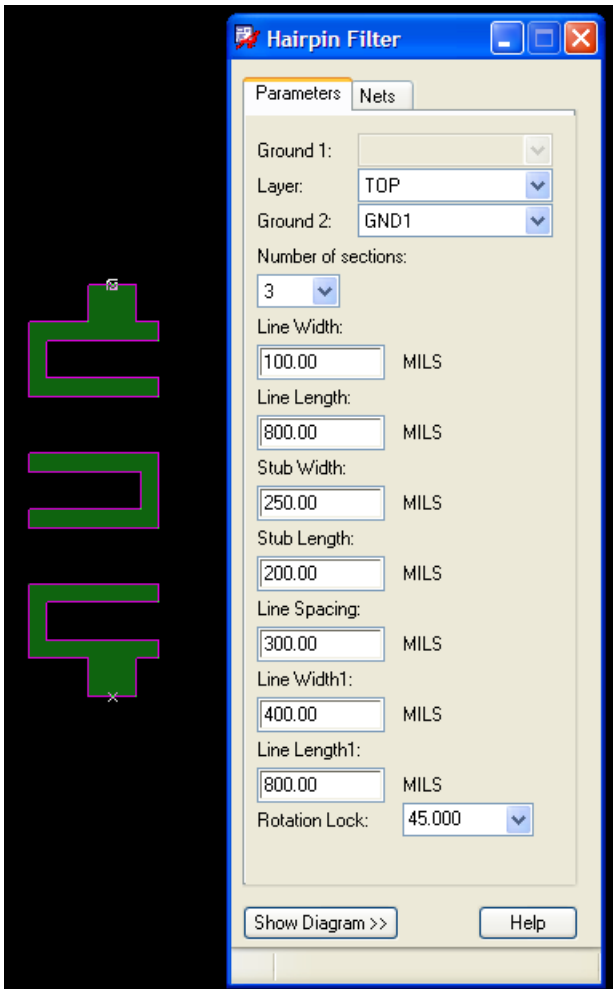
Crossprobe Selection From Schematic

The cross-probing feature between schematic and layout editor lets you pick the component directly from schematic.



For further details, see the `rf change` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Figure 4-4 Changing RF Component Parameters



Breaking RF Components

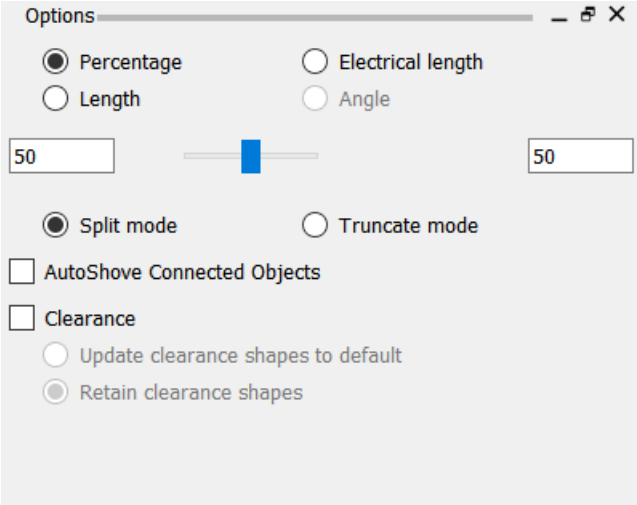
You break an RF component parameters by choosing *RF-PCB – Edit – Break*. The breaking options appear in the Options pane (Figure 4-5). Since parameter changes may break existing RF component connections, use the *AutoShove Connected Objects* option to keep the components connected after you make the changes.

When you break an RF component, you can choose to either split or truncate the component. You can break an RF component by the angle of the curvature (in the case of curved components) or the length (in the case of non-curved components). Also, the option to break

a component by its electrical length is available only for RF components that support this property.

You can break a component by percentage (applicable for all valid types of components), by length (applicable for LINE type components), by angle (applicable for CURVE type components), or by electrical length (applicable for MLIN, MCURVE, MCURVE2).

Figure 4-5 RF Break Options pane



Breakable RF components

The following table describes the RF components types and their effective breaking parameters.

	Percentage	Length	Angle	Electrical Length
MACLIN	✓	✓	✗	✗
MACLIN3	✓	✓	✗	✗
MCLIN	✓	✓	✗	✗
MCURVE	✓	✗	✓	✓
MCURVE2	✓	✗	✓	✓

MLIN	✓	✓	✗	✓
MTAPER	✓	✓	✗	✗
SBCLIN	✓	✓	✗	✗
SCLIN	✓	✓	✗	✗
SCURVE	✓	✗	✓	✗
SLIN	✓	✓	✗	✗
SOCLIN	✓	✓	✗	✗
PCCURVE	✓	✗	✓	✗
PCLIN1	✓	✓	✗	✗
PCLINn	✓	✓	✗	✗
PCTAPER	✓	✓	✗	✗
PCTRACE	✓	✓	✗	✗

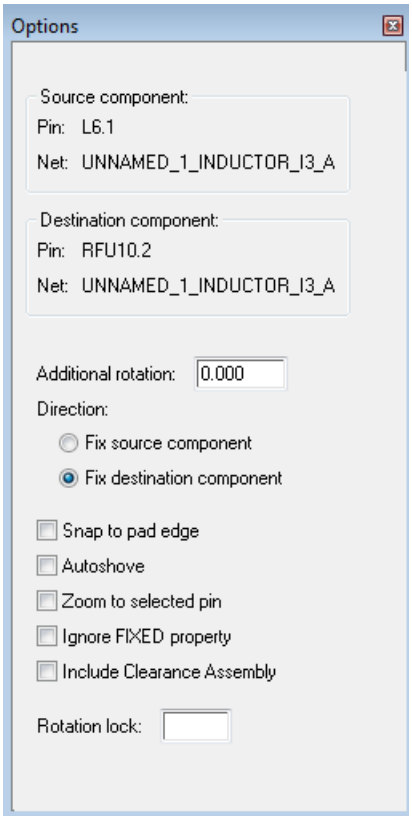
Note: You cannot use this command to break non-RF components.

For further details, see the `rf_break` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Snap Connecting an Element

In certain cases, you may need to connect all elements of a trace according to a netlist. It can be difficult sometimes to ensure the accuracy of manual connections with respect to position, direction, and so on. You can quickly snap (move and connect) elements and reorder their connections by choosing *RF-PCB – Edit – Snap*. Once the RF Snap options appear, you select a target pin on one component, then a destination pin on another component with the same net name. The first component then snaps to connect to the second component.

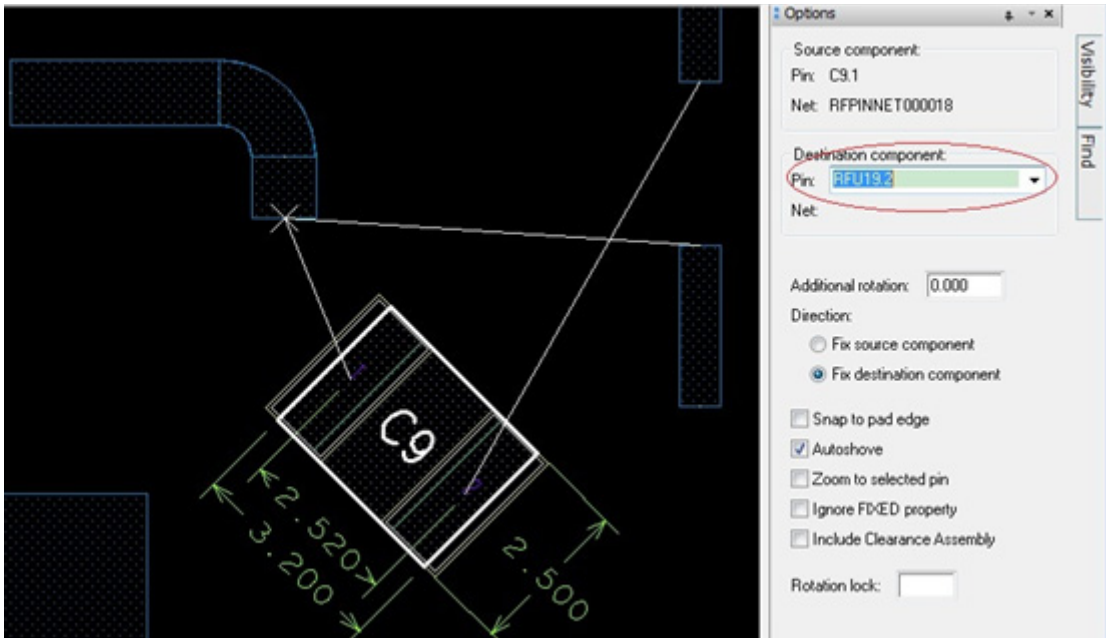
Figure 4-6 Pin Snapping Between RF Components

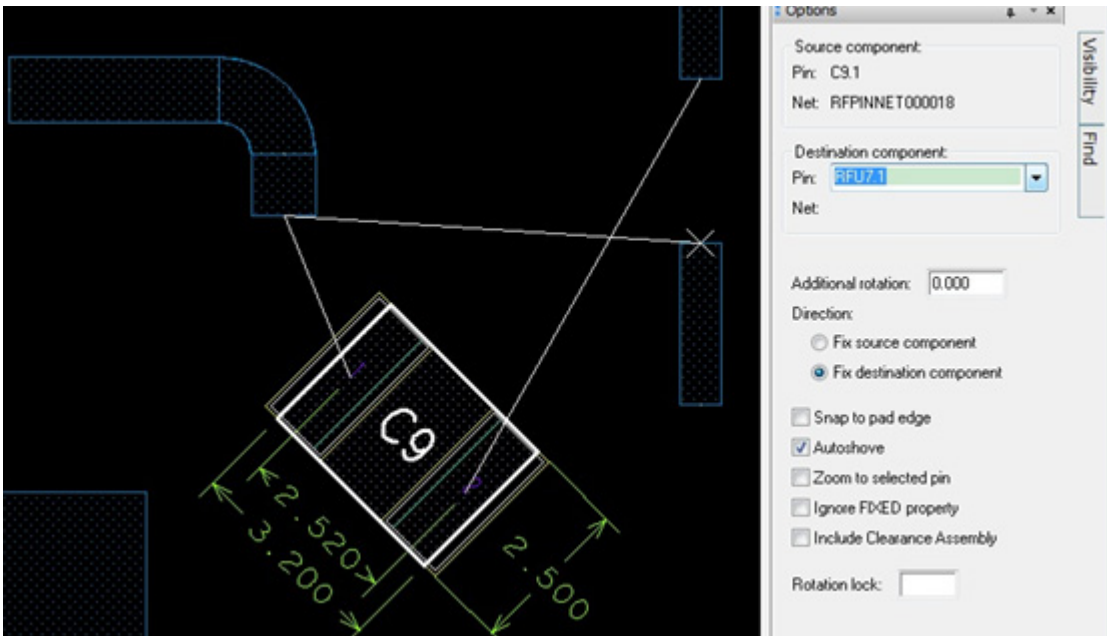


The snap options provide a drop-down list for the destination pins (RF pins are displayed on the top of the list) if multiple pins are connected. In such case, you can choose a destination pin directly on the canvas as shown in the following example.

The component C9.1 is connected to RFU19.2 and RFU7.1. When C9.1 is selected as a source pin, RFU19.2 and RFU7.1 are listed in the drop-down list for the destination pin. A cross mark is displayed at the corresponding destination pin location when the different pin is

selected. You can select and click the destination pin at the canvas to confirm the snap operation.





For further details, see the `rf snap` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Deleting RF Components

You use the rf_delete command to permanently remove RF components from the design. Choose *RF-PCB – Edit – Delete*, then click on the components in the design.
You can also delete multiple RF components simultaneously by drawing a bounding box around them. This command purges all component information (physical as well as logical) from the design database.

Note:

- If you just want to delete the component symbol, you can use the Allegro PCB Editor delete command by choosing *Edit – Delete*. However, you must repackage the RF component before you can use it again in the design. See the rf_autoplace command for further details.
- You cannot use this command to delete non-RF components.

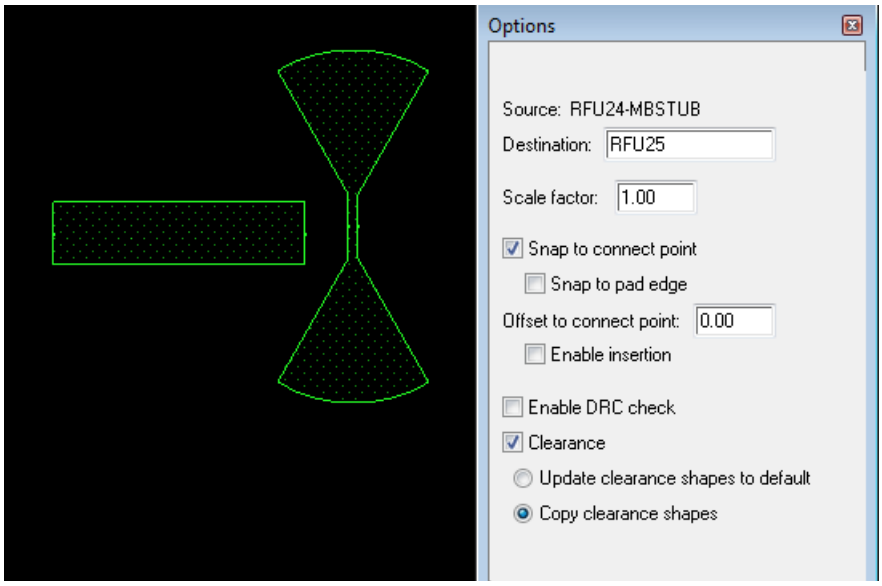
Copying an RF Component with a Scale Factor

Use the rf_scaled_copy command to copy an RF component at a specified scale. Choose *RF-PCB– Edit – Scaled Copy*, then choose the component to copy. Enter a scale factor in the Options pane, then move the copy to its destination. The scale factor may be any number greater than 0. A scale factor between 0 and 1 decreases the size of the component.

Note:

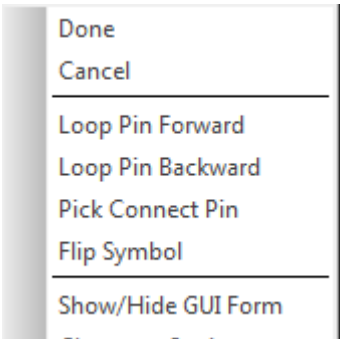
- When you scale copy RF components, angle values are unaffected.
- You cannot use this command to copy non-RF components.
- You can use the Enable insertion option to insert the scale copy between to connected RF components.

Figure 4-7 Copying a Microstrip Butterfly Stub Component



To change the connect pin, right- click and choose Loop Connect Pin Forward and Loop Connect Pin Backward. The cursor dynamics changes to reflect the selection.

You can also pick the connect pin directly using Pick Connect Pin option, as shown in figure below.



f you want to control physical positioning and logic information, check *Snap to connect point,* and the start point and rotation of the copied component will be calculated by any object it touches. You can use the `rf_modify_net` command to change the connectivity.

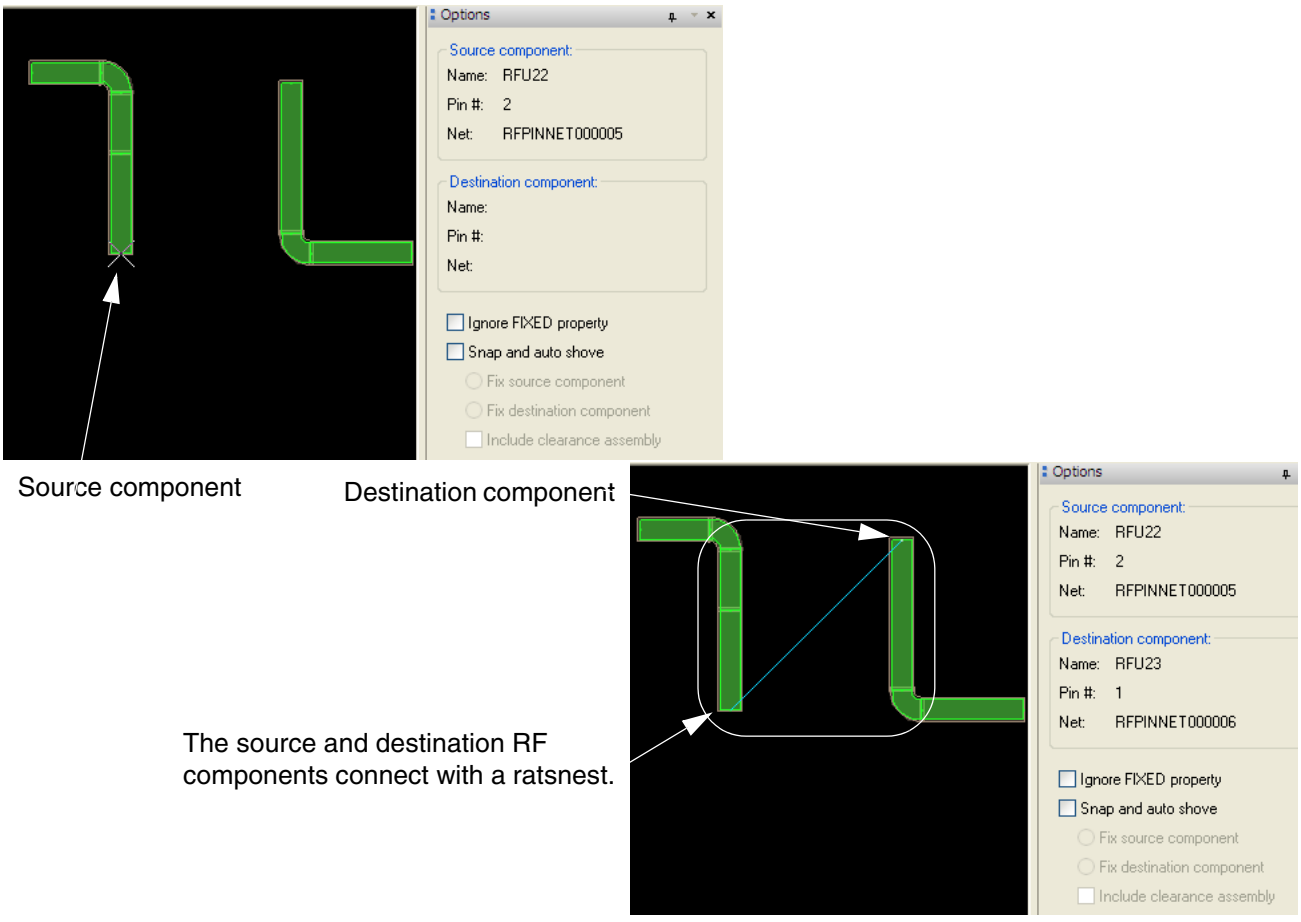
Modifying Connectivity of RF Components

Use the `rf_modify_net` command to quickly and interactively change the pin logic connectivity of RF components. Choose *RF-PCB – Edit – Modify Connectivity*, and then

choose a source and destination RFcomponent. The tool immediately assigns the source pin to the net of the destination pin, as long as, you do not click *Snap and Auto Shove*.

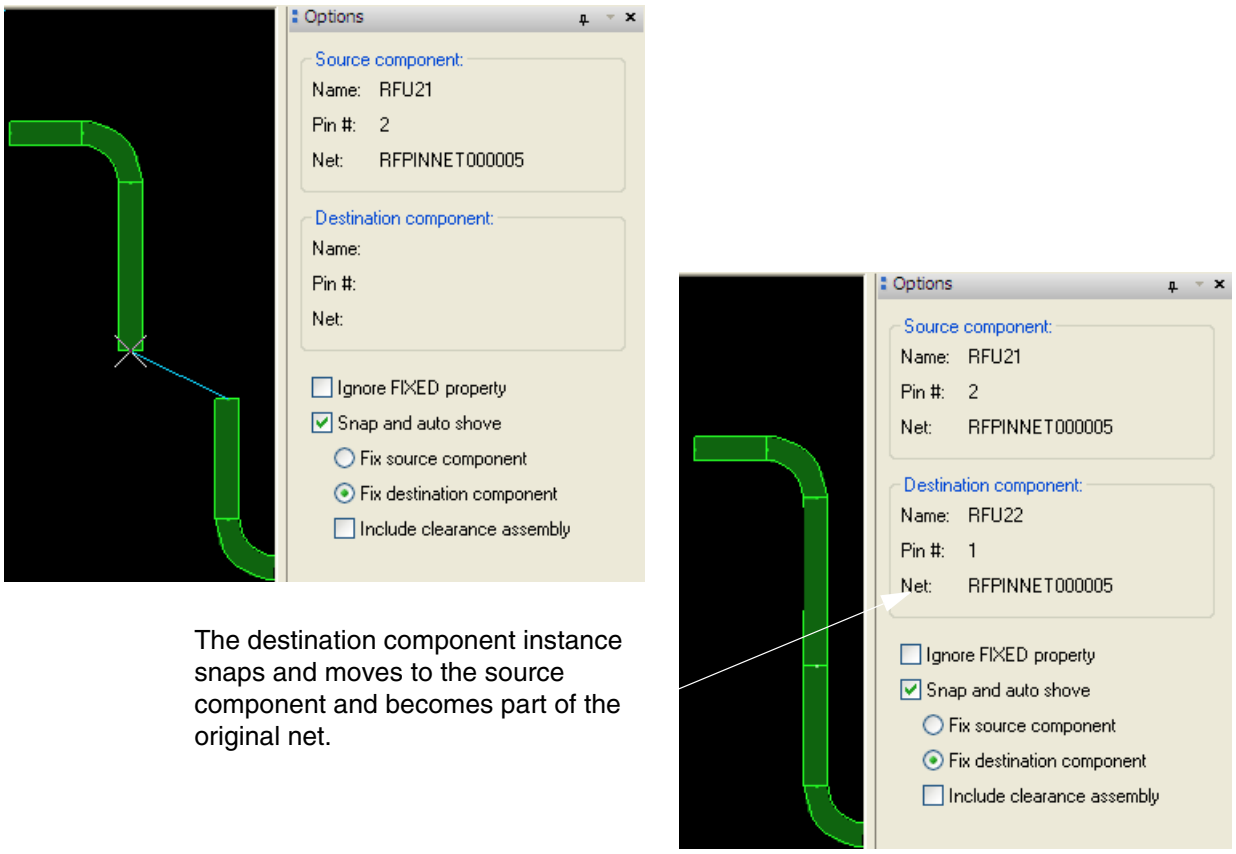
In the following example `RFU22.2` is the source pin and `RFU23.1` is the destination. When you pick the destination pin, the net of the source pin immediately changes to that of the destination pin. In this case, the net `RFU22.2` will change to `RFU23.1`.

Figure 4-8 Modifying Connectivity without Snap and Auto Shove



When *Snap and Auto Shove* is checked, the tool moves the component to attach to `RFU22` or `RFU23` depending on whether *Fix Source* or *Fix Destination* is checked.

Figure 4-9 Snap and Auto Shove



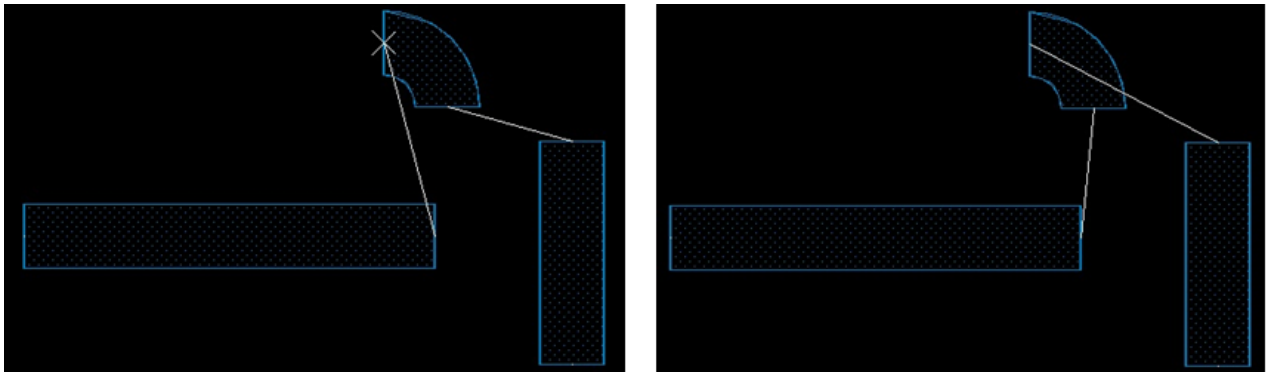
The destination component instance snaps and moves to the source component and becomes part of the original net.

Swapping nets on pins

The *Swap pin nets* option in the `rf modify net` command lets you swap nets on the pins of RF components. This functionality is only available when *Swap pin nets* option is checked.

To swap nets choose source and destination pins on RF components, as shown in the following example. The tool displays the name of pins and the nets are swapped by the command.

Figure 4-10 Swapping nets on pins

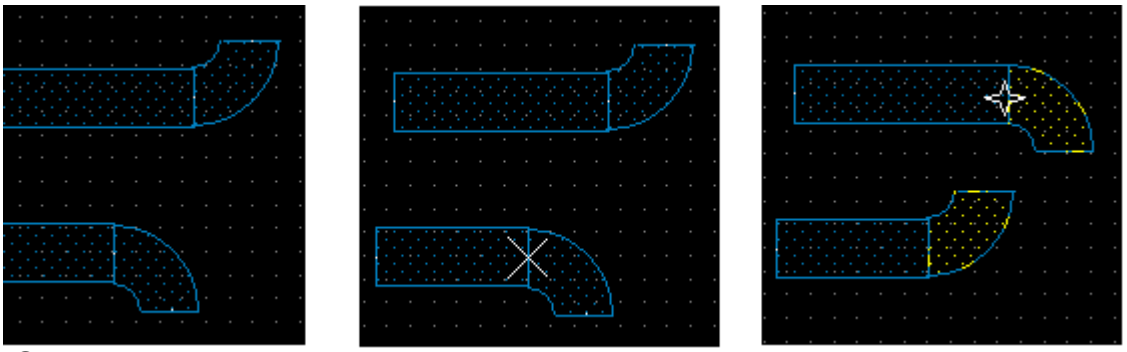


Swapping nets on pins with autoshove

To autoshove when swapping nets on the pins, enable both *Snap and auto shove* and *Swap pin nets* options.

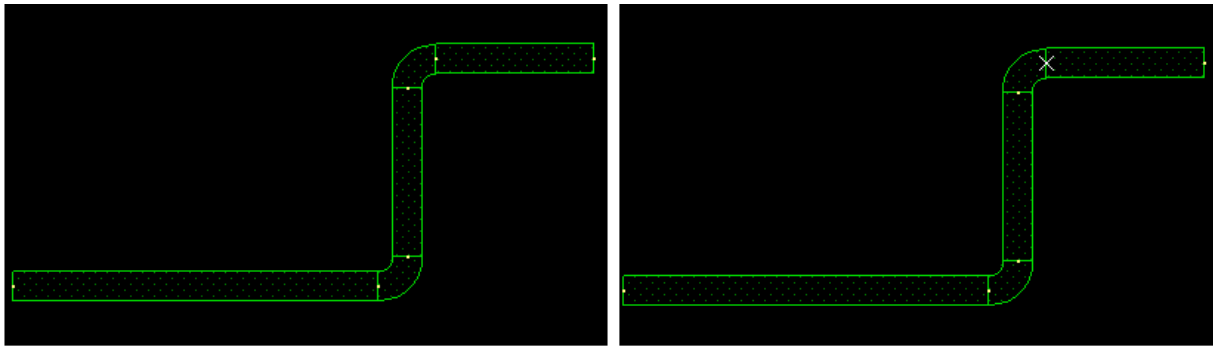
The following examples shows the results of autoshove with swapping nets on pins functionality on different and same components.

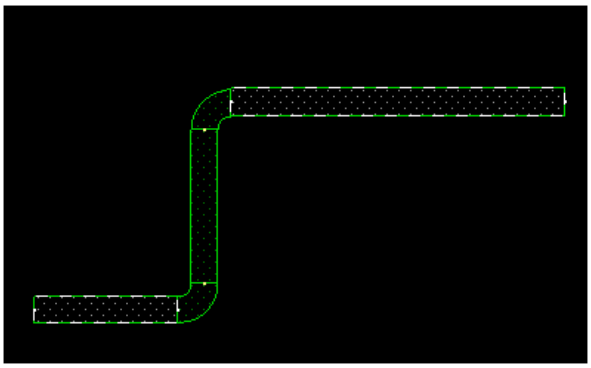
Figure 4-11 Operation on different components



Original RF components | Pick Source Pin | Pick Destination Pin

Figure 4-12 Operation on same component





Note: The swap operation works only for pins of RF components. If either of the pin belongs to a non-RF component, the tool displays following error:

```
E- (SPRFPC-201): U1302 or C1324 is not a recognized RF component.
```

Editing Groups of Objects

The `rf_group_copy`, `rf_flip`, and `rf_push` are group editing commands. They share the following similarities by supporting:

- group selection of objects
- on-demand snapping
- both RF components and non-RF components

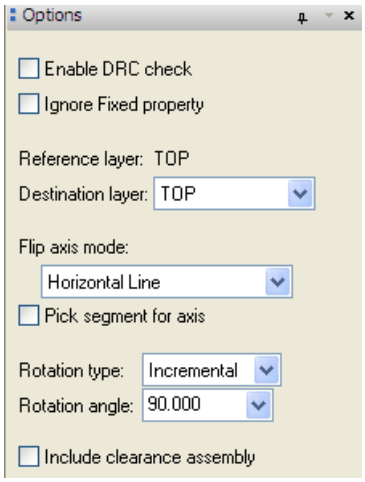
The `rf_push` command differs from `rf_copy` and `rf_flip`. in the objects that it supports. It does not operate on non-RF components.

Copying a Group of Objects

Use the `rf_group_copy` command to copy groups of objects simultaneously. Choose *RF-PCB – Edit – Copy*, and then draw a bounding box around the components. The `rf_group_copy` command lets you rotate and flip using the right mouse button for more accurate positioning and flexible geometric structures. You can also include clearance assemblies attached to the RF components. You can perform these actions before and after copying a group of objects.

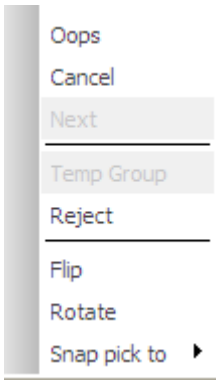
You use the Copy Operation Options pane(Figure 4-13) to set up the group copy, flip, and rotate options.

Figure 4-13 Copy Operation Operations pane



The right mouse button menu provides access to *Flip*, *Rotate,* and *Snap pick to,* enabling you to perform these operations after you have copied the objects. For more information on snapping, see *Snapping Mode* in the *Allegro User Guide: Getting Started with Physical Design*.

Figure 4-14 Right Mouse Button Menu



The following table lists all supported object types for the copy command.

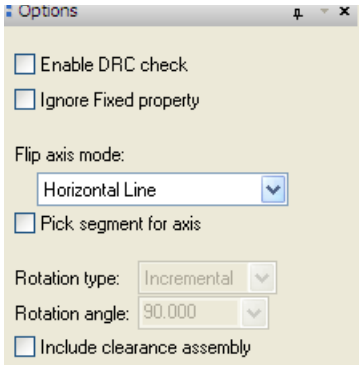
Type	Notes
Shape	ETCH shape only, both static and dynamic
Line/Line Segment	
Cline/Cline Segment	
Group	A group is supported only if all members are supported
RF Component	Microstrip/Stripline limitation applied.
Non-RF Components	Non-RF components copy using the device type and package name from the source. The symbol mirror state also copies from source. This means the copy may lead to connectivity issues. When flipping unsupported, non-RF components such as multi-pin symbols, they move and rotate to the proper positions.
Via	A via copies using the padstack of the source. You need to manually edit the padstack if the copy operation leads to connectivity loss due to layer changes.

Flipping a Group of Objects

You use the `rf flip` command to flip a group of objects with pre-defined flip axis selection in your design. Choose *RF-PCB – Edit – Flip*, and the Flip Operation options appear in the Options pane, which you predefine the flip modes you want to use to flip a group of objects. You can flip both RF and certain non-RF objects at the same time with optional rotation

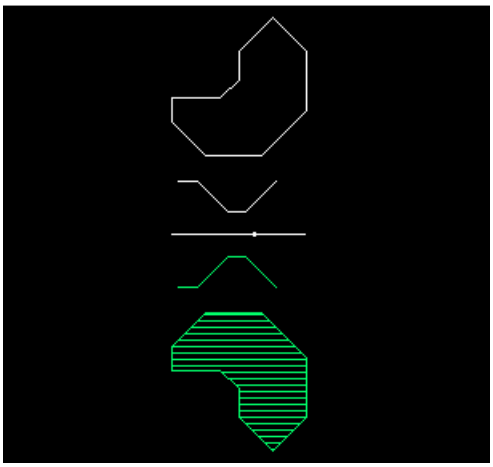
actions. You can also flip clearance assemblies attached with the RF objects. The flip command is a subset of the copy command and performs similarly.

Figure 4-15 Flip Operation Options pane



The following flip axis modes are supported:

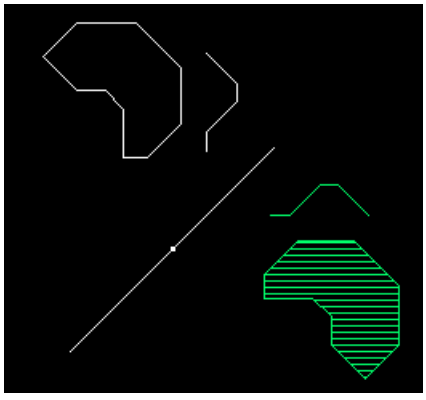
- Horizontal Line — Specified by a point you pick.The horizontal coordinate is used to form a horizontal line. The length is not important as the flip command specifies it internally.



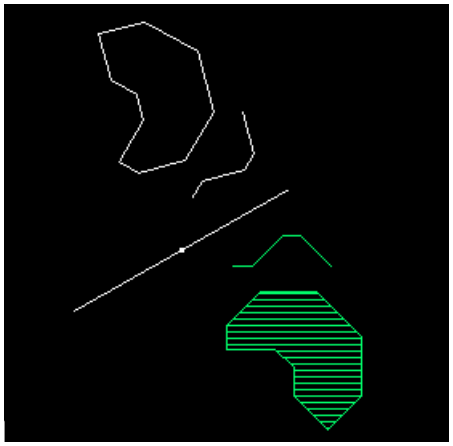
- Vertical Line — Specified by a point you pick. The vertical coordinate is used to form a vertical line.

- Diagonal Line — Specified by two points that you pick. The direction of the diagonal line is determined by the relative position of the two points. The first pick point is used as the origin of the diagonal line and the second is used to determine its direction as described in the following table.

Relative Positioning	Direction
second point is within the upper-right region of the first point	45 degrees
Second point is within the upper-left region of or directly above the first point	135 degrees
Second point is within the lower-left region of or directly under the first point	-135 degrees
Second point is within the lower-right region of the first point	-45 degrees



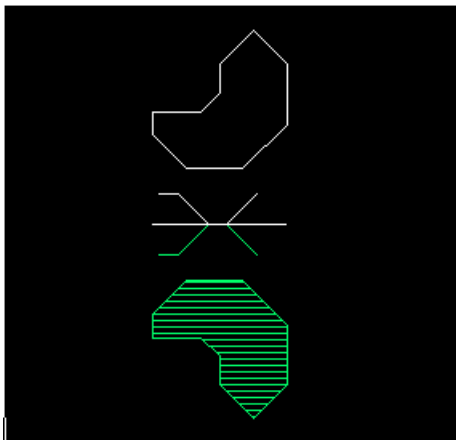
- Odd Line — An arbitrary angle specified by a point you pick as the reference point and the angle specified by the values in the *Rotation Type* and *Rotation Angle* fields.The reference point and the angle value calculate the two points for the odd line. When the rotation type is *Absolute*, the value in the *Rotation Angle* field becomes the angle to create the odd line. If the rotation type is *Incremental*, the value in the *Rotation Angle* field is used as the lock angle, so you can rotate the odd line to fix at a particular position. The locked angle is calculated and used to create the odd line. Setting the rotation angle to zero enables you to rotate without angle locking.



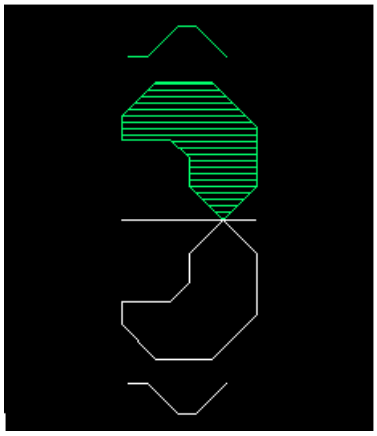
- Left Edge of Object Box — The left edge of the bounding box of the selected objects to flip.

- Right Edge of Object Box — The right edge of the bounding box of the selected objects to flip.

- Top Edge of Object Box — The top edge of the bounding box of the selected objects to flip.



■	Bottom Edge of Object Box	The bottom edge of the bounding box of the selected objects to flip.



Pushing components

You can change the layer specifications of a group of RF components by choosing *RF-PCB – Edit – Push.*

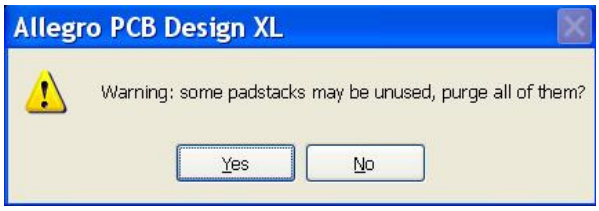
The push command operates on the following database types:

Shape	ETCH shapes only, both static and dynamic
Line/line segment	
Cline segment	Vias are added automatically if no vias or pins connect to the cline. If vias and pins are connected and the destination layer is not included in the padstack, you cannot use the push command.
Group	A group is supported if all members are supported.

Vias	This includes user-defined components containing vias. If you push vias (or user-defined components containing vias), you are prompted with the following warning:

While the push operation on the vias may create new padstacks, some of these newly created padstacks may not be used.

In this case, you choose Done to complete the push operation, you are prompted as follows:



Alternatively, you can also purge all the unused padstacks in the Options pane from Tools - Padstack - Modify Design Padstack.

RF component	Exceptions: ■ microstrip components cannot push to inner layers. ■ stripline components cannot push to surface layers. ■ miscellaneous RF components can push to any layer.

The push operation is interactive and is initialized after you choose the objects to push. When you make the selection, you are automatically in temporary group mode so that you can make multiple, separate selections based on the visible etch layers.

The push operation performs as follows:

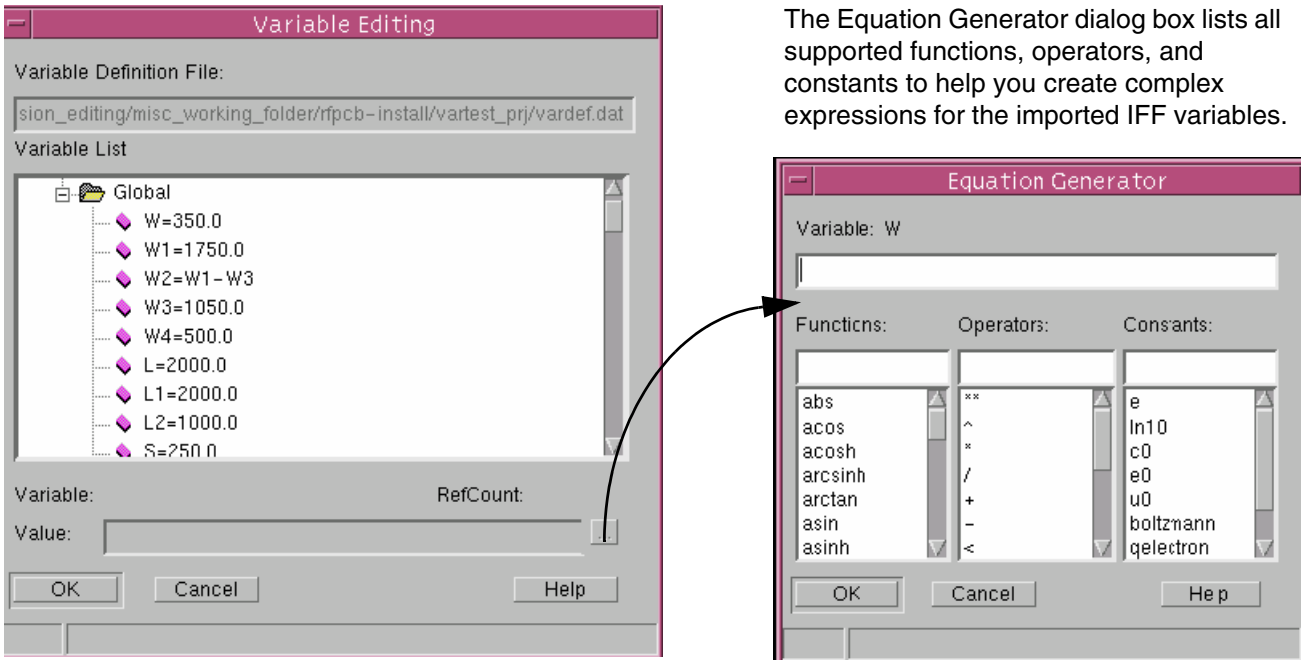
- Generic object types delete and recreate on the desired layer at the same position and with the same geometry.
- RF components change layer parameters and repackage.

Editing variables imported from an IFF Schematic File

To generate synchronized physical packages you need to have variables and expressions that you import in the IFF schematic file. Once you specify a project directory in the RF PCB Settings options and the IFF file contains VAR components, the tool creates a variable definition file (`vardef.dat`) and saves it in the project directory. The tool searches in the directory for the file and displays the variables and expressions in the Variable Editing dialog box for editing.

If the variable definition file is not there, the tool issues a message in the console window prompt indicating there are no VAR components in the project's schematic.

Figure 4-16 Editing Variables in IFF Schematic File



Error Messages for Variable Expressions

If any of the following errors occur, the tool displays an error message:

- `ERROR (RFVAREDIT-646): Undefined variable(s) "…" in expression "…"`
- `ERROR (RFVAREDIT-644): Multiple definitions found in sub-block … for variable: "…" in expressions :…`

- `ERROR (RFVAREDIT-647): Recursively defined variable "…". ". "ERROR (RFVAREDIT-642): Lexical error(s) in expression "…" defined in … in sub-block …`
- `ERROR (RFVAREDIT-648): Error in variable changes.`
- `ERROR (RFVAREDIT-641): Error in variable definition file.`

When you close the dialog box, the tool checks to determine if any variables changed. If there have been changes, you need to repackage your design to refresh the variable definitions.

The tool updates the variable definition file and the parameters for all component instances that use that variable.

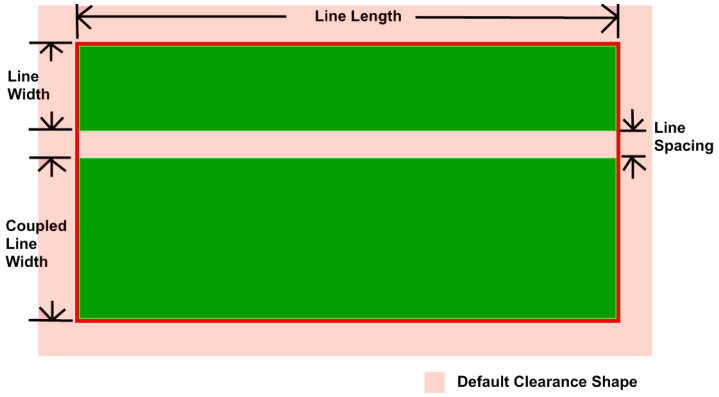
5

Asymmetrical Clearances

- Overview
- Understanding Clearance Shapes and Assemblies
  - Surrounding clearance mode
  - Sidewalk clearance mode
- Working with Clearances
  - Initializing clearance shapes
  - Assembling Clearance Shapes
  - Disassembling Clearance assemblies
  - Deleting Clearance shapes

Overview

The relationship of copper elements to each other is critical for RF circuit design and performance. Especially so is the placement of RF elements and the positioning of copper shapes (also known as copper pouring). Very often these copper shapes are connected, for example, to ground to provide shielding. The clearance values can, in some cases, even be more important than the circuit elements themselves.



Defining these clearance shapes manually can be very time consuming and tedious. This version of RF-PCB provides you with the ability to create and assign clearance shapes to the RF elements of your design.You can control clearance relationships and that provides significant productivity gains and reduce the need to continually take measurements (from the Layout) to verify the performance.

Understanding Clearance Shapes and Assemblies

Clearance shapes are generally route keepout shapes and default clearance shapes of RF components can be defined as an expansion of its etch shape by a defined offset amount. The offset can be defined as the clearance distance or the shape cut-out from the edge of the clearance shape to the edge of the RF symbol.

Every clearance shape can be part of clearance assembly, and the RF component etch shape is related to the clearance assembly. Multiple clearance shapes can be merged and grouped together into a clearance assembly.

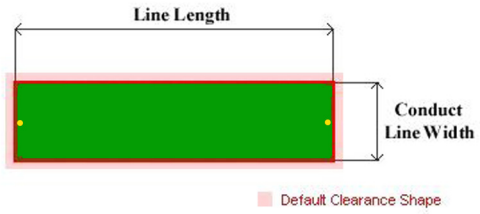
All RF components have a Surrounding clearance shape. Transmission line components also have an additional Sidewalk mode.

Surrounding clearance mode

The surround clearance mode works by creating an expansion of the boundary of the etch shape by the defined offset. The boundary is generated by considering all shapes within an RF component as an integral shape.

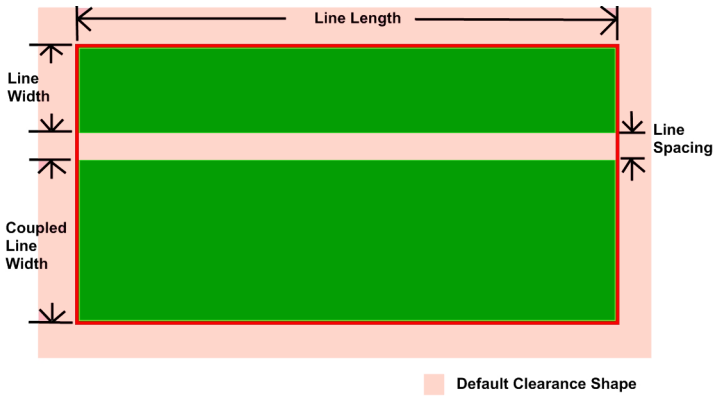
Single etch shape components

For RF components with a single regular etch shape, for example, MLIN, MCURVE, or MSTUB, the clearance shape is defined by expanding the etch shape by an offset amount.



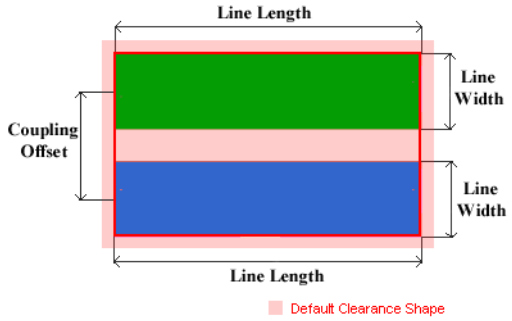
Multiple etch shape components

For RF components with multiple regular etch shapes, for example, MCFIL, MACLIN, or MACLIN3, the clearance shape is defined by expanding the bounding box of the etch shapes by an offset amount. The boundary is drawn in red.



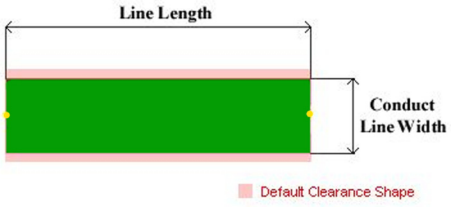
Multi-layer, multiple etch shape components

For RF components with multi-layer, multiple etch shapes, for example, SOCLIN, the clearance shape is defined by expanding the bounding box of the etch shapes by an offset amount. The boundary is drawn in red.



Sidewalk clearance mode

For transmission line components, shapes can also be defined using the sidewalk mode, in addition to the surrounding mode. In the sidewalk mode, the clearance shape is generated by expanding the etch shape only in the peripheral directions. For the directions that lead to pins or connections, clearance shapes are not expanded.



Sidewalk clearance mode ensures that adjacent transmission line components do not have overlapping clearance shapes, make cleaner clearance assemblies.

Working with Clearances

In this section...

- Set up clearance shapes
- Initializing clearance shapes
- Assembling Clearance Shapes

- Disassembling Clearance assemblies
- Deleting Clearance shapes

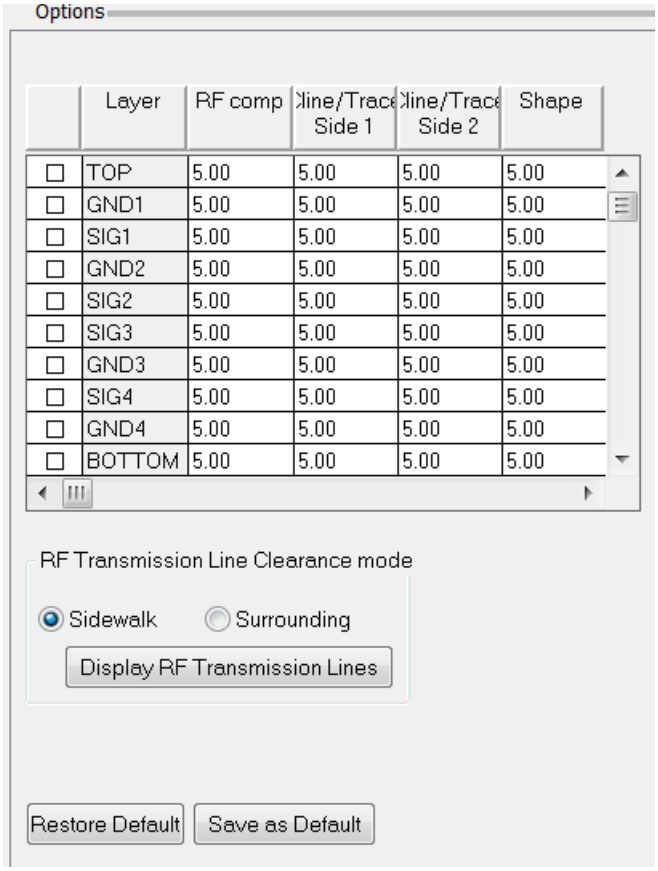
Set up clearance shapes

Before you can create clearance shapes, you need to specify the setup options for Clearance shapes.

The setup options include specifying:

- Layers for which the clearance shapes are created
- Offset values to create the clearance shapes
- Transmission line clearance modes

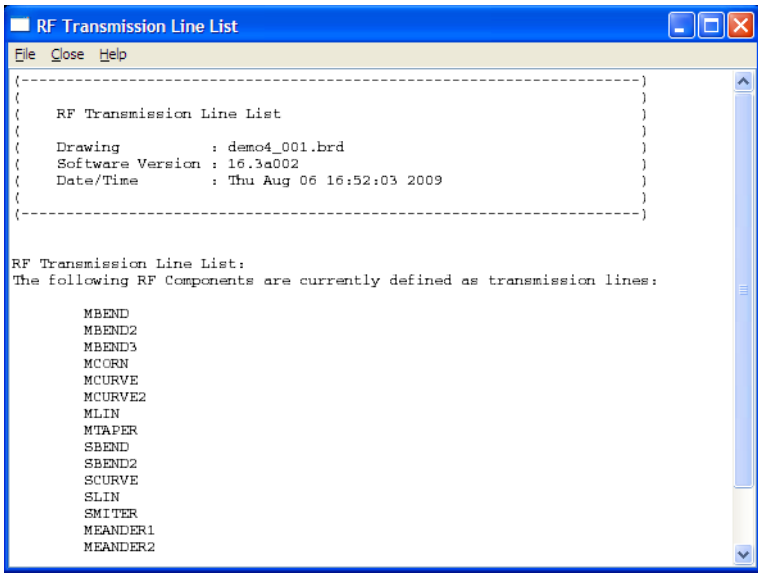
To specify the setup options choose *RF-PCB — Clearance — Settings* or run `rf ac setup` command. The *Clearance Settings* dialog box appears.



Select the *Layers* on which to create the clearance shapes, followed by the offset values of the clearance shapes for different objects like, RF comp, cline, and shapes. Clearance shapes are generated only on the selected layers. You can also create asymmetrical clearance shapes for clines and RF traces by defining different left and right offset values.

Choose *Sidewalk* or *Surrounding* to specify the mode to use while creating clearance shapes for transmission line components. Click *Close* or right-click on the board and choose *Done*.

Click the *Display Transmission Lines* button to view a report that lists all the types of transmission lines that support the Sidewalk mode.



Click *Close* to dismiss the dialog box. The settings you enter in the dialog box are retained in the current session of Allegro. To retain these values in other sessions use *Save as Default* and *Restore Default* options.

For further details, see the `rf_ac_setup` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Initializing clearance shapes

After you have defined the setup options, you can initialize the clearance shapes for the RF components, cline, RF traces, and shapes. Every RF symbol has an initial clearance shape definition. The clearance shapes are initialized using the physical dimension of the RF symbol and the offset values that you have defined in the RF PCB setup dialog box. You can initialize clearance shapes for both existing and new RF components, clines, traces, and generic shapes.

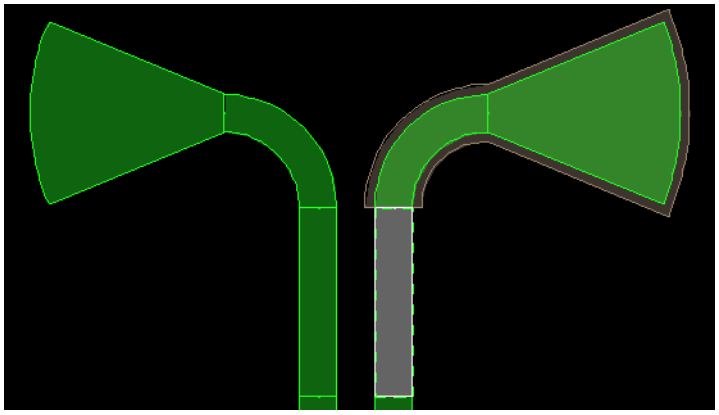
Important

Creating clearance shapes for Vias, Pins, and are not supported.

Initializing clearance shapes for existing RF components

To initialize clearance shapes on existing RF components and transmission lines, choose *RF-PCB — Clearance — Initialize* or run the `rf_ac_init` command. You can also set local clearance settings by enabling *Override global clearance settings* option. This option enables the global Clarence settings for editing. You can use these local settings during the command process. The *Group Asymmetrical Clearances* option displays in the *Options* pane to enable group clearances.

Click on the RF component to select it and click again to create a clearance shape around it. Continue with other RF components. At any time you can right-click to access the context menu and choose Cancel, Done, Next, Change Settings, or use the Temp Group feature.



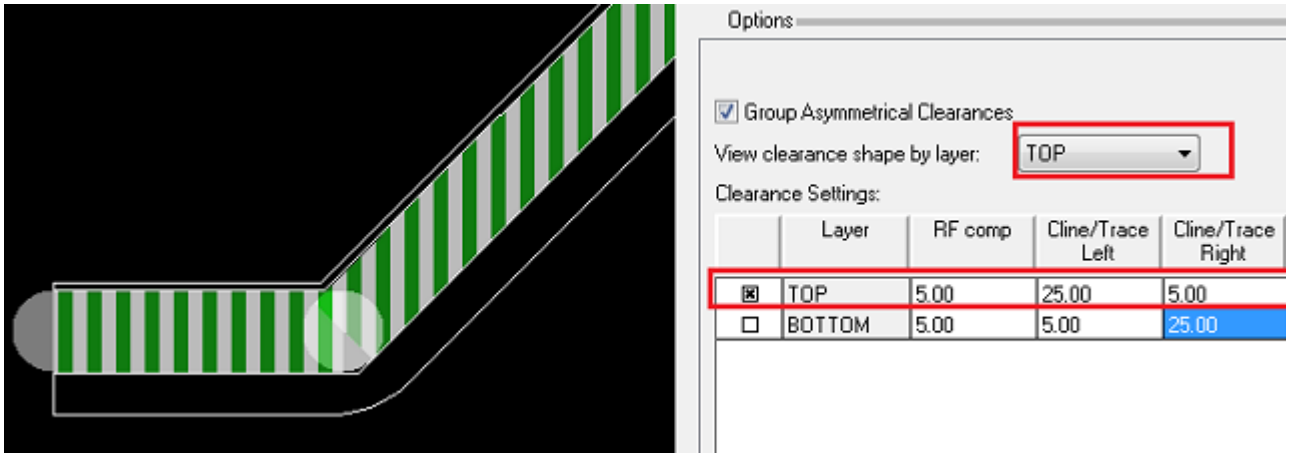
You can also select multiple RF components by creating a temporary group, or draw a bounding box using the mouse, and then initialize a single clearance shape for the group.

Note: If you initialize clearance shapes on multiple objects without creating a temporary group, individual clearance shapes are created for each shape. The clearance shapes may have overlaps. If you use the temporary groups.

You can also create the initial clearance shapes for RF components that are part of a replicated block in the design.

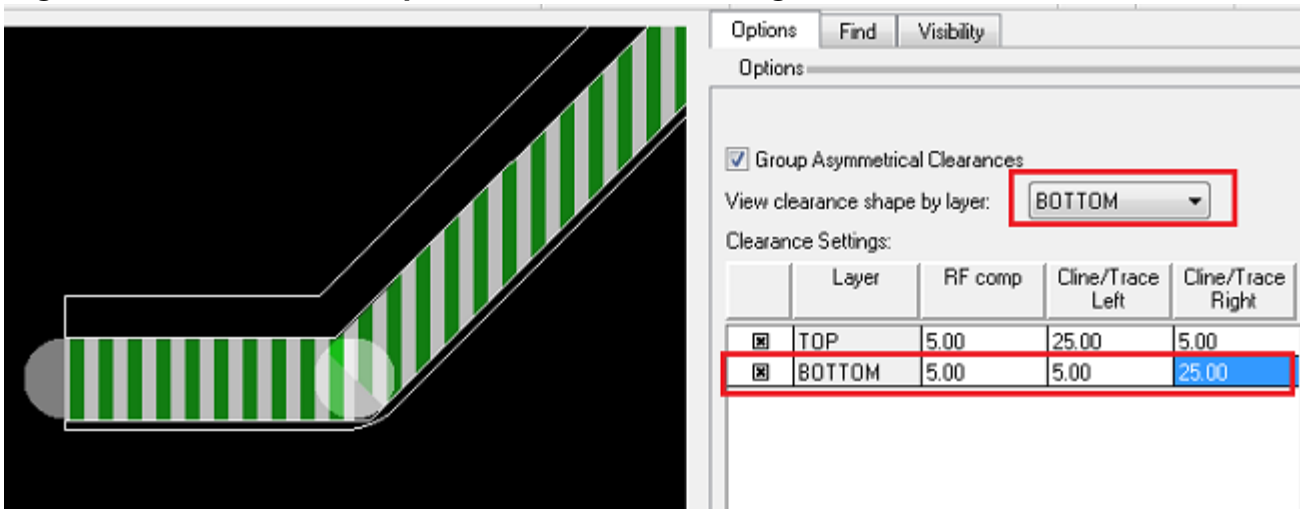
For creating asymmetrical clearance shapes on a cline and trace shapes by specifying different offset values for left and right.

Figure 5-1 Clearance shape initialization on the left side of a cline



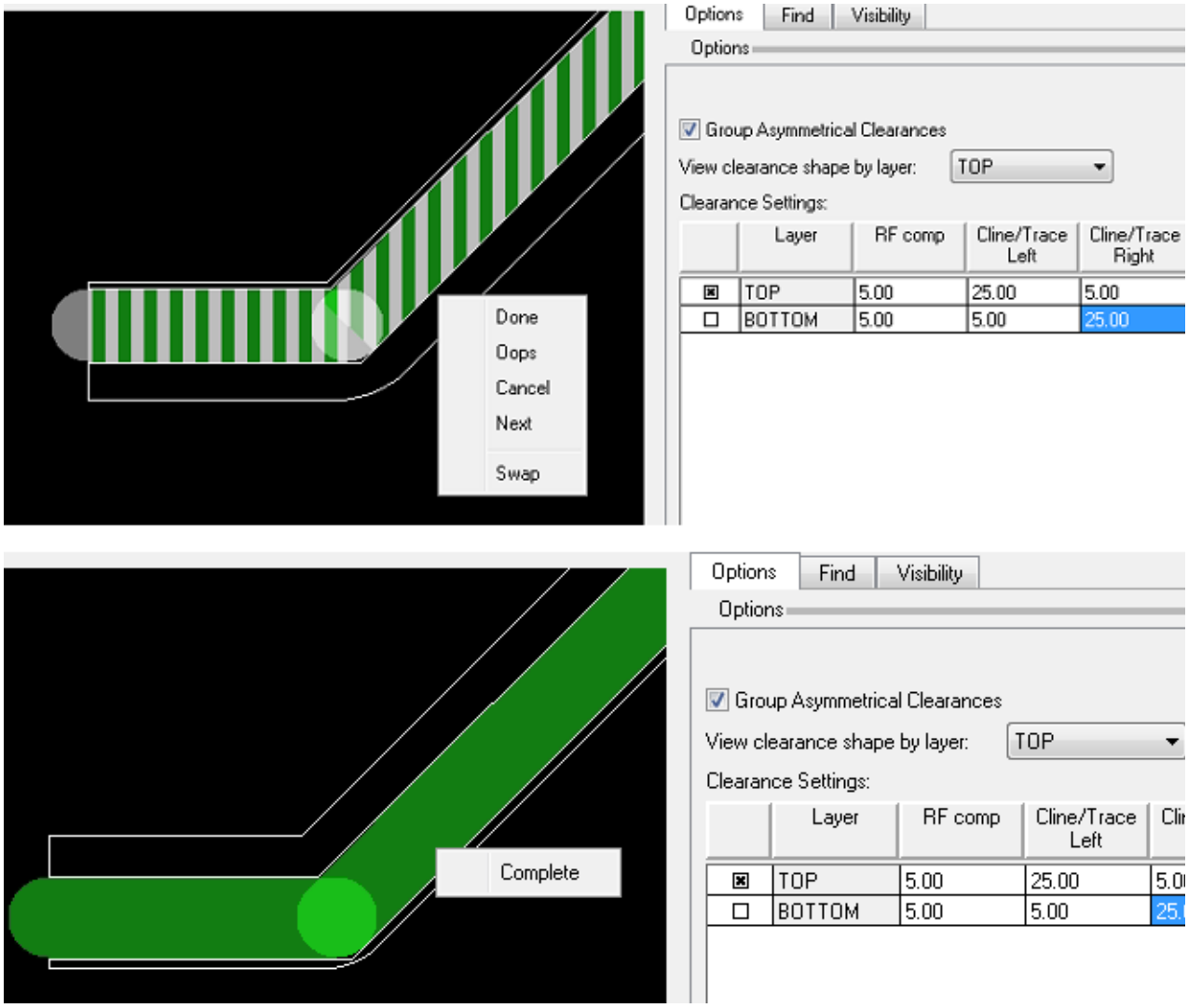
Choose a layer to preview the dynamic path of the clearance shape.

Figure 5-2 Clearance shape initialization on the right side of a cline



The swap functionality provided in the pop-up menu allow you to interchange the left and right offset values. The *Swap* option is available in the po-up menu when the dynamic path is displayed for a selected object.

Figure 5-3 Swapping clearances on the objects



When adding

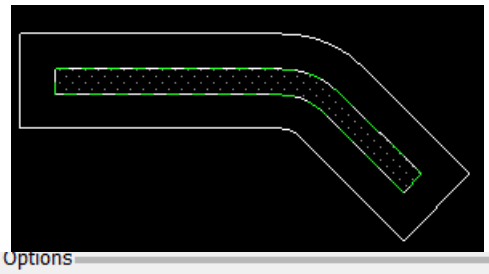
For further details, see the `rf_ac_init` command in the *Allegro PCB and Package Physical Layout Command Reference.*

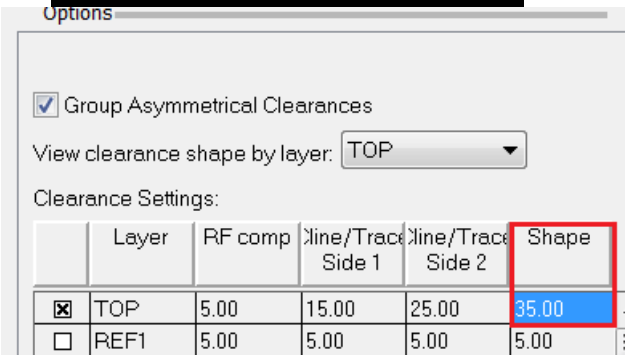
Creating Initial Clearance for Generic Shapes

To create initial clearance for generic shape elements, specify settings for *Shape* in the *Clearance Settings* section of the `rf_ac_init` command. The offset value specified in

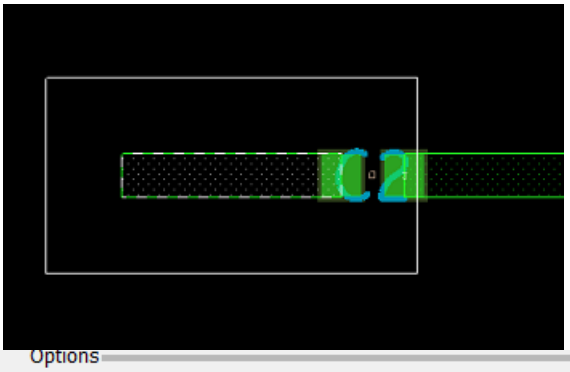
the *Shape* column controls the size of the clearance shape for generic shape elements. The initial clearance for generic shape elements depends on its connectivity with other elements.

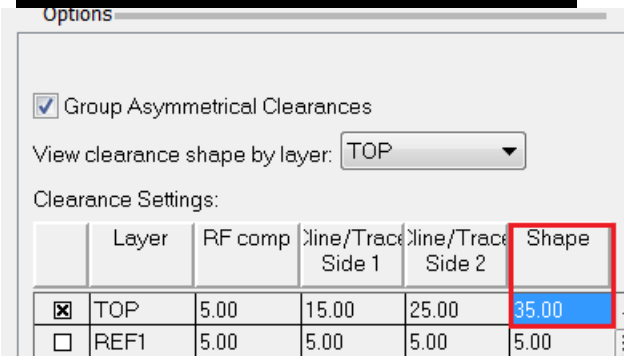
Generic Shape Connected to	Clearance Type	Clearance Setting Used
no pin	Symmetrical	Shape



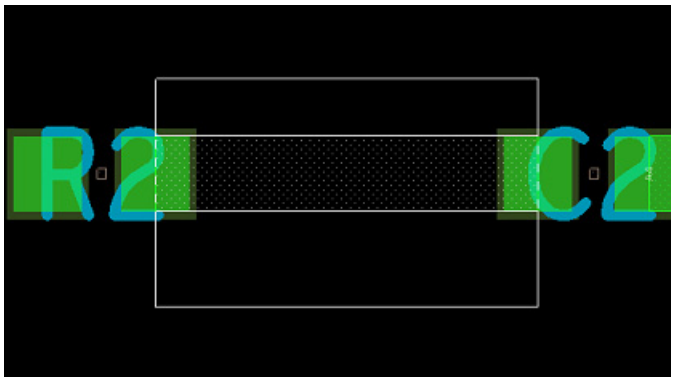


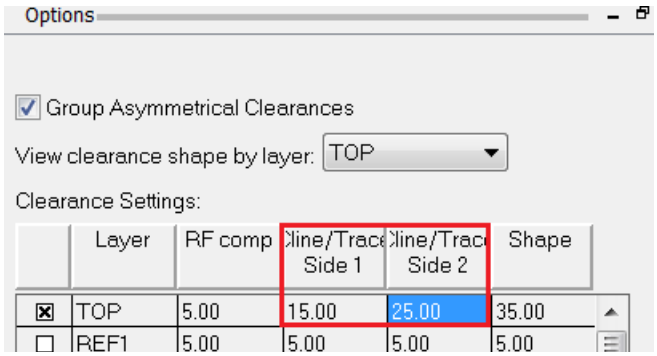
only one pin Symmetrical Shape



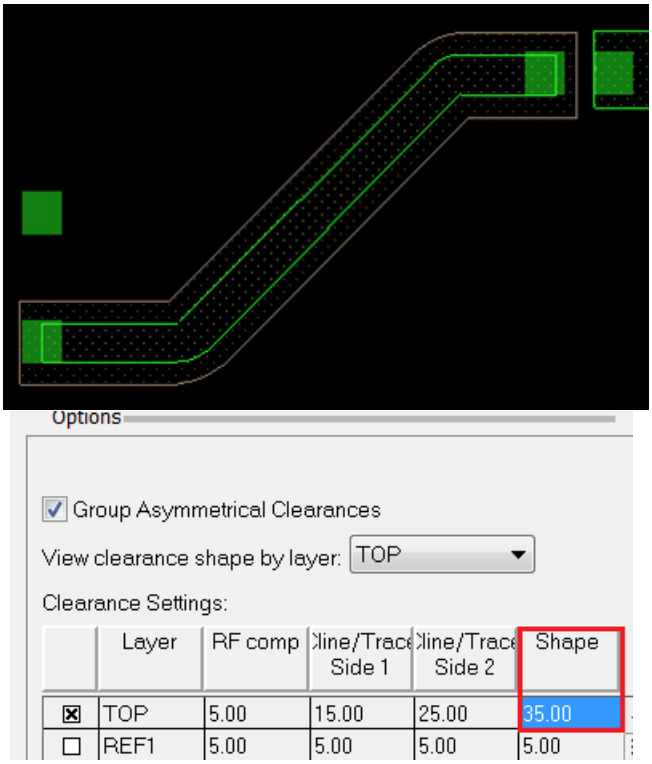


two pins that are close to shape boundary	Asymmetrical	Cline/Trace side 1 and Cline/Trace Side 2

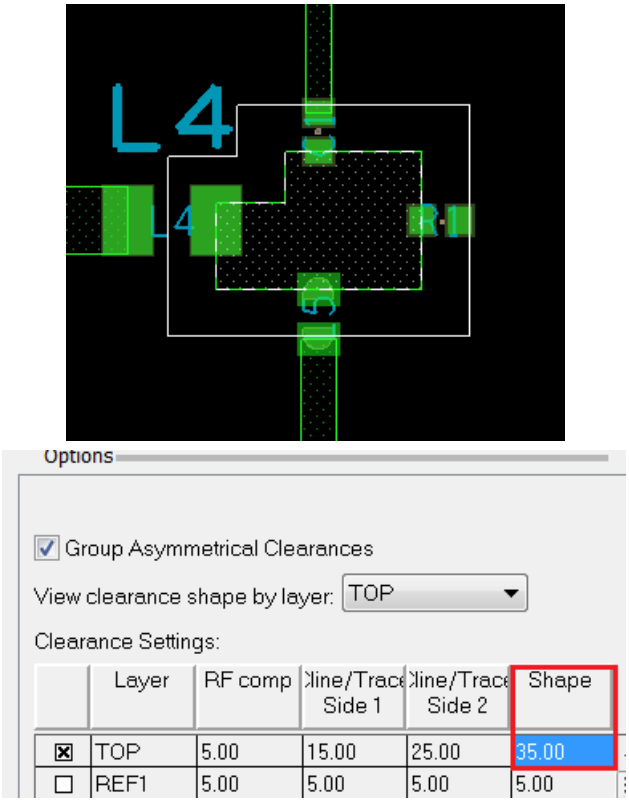




two pins that are not close to shape boundary	Symmetrical	Shape

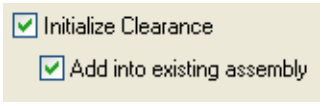


more than two pins Symmetrical Shape



Initialize clearance shapes for new components and connects

You can initialize clearance shapes while you are adding new RF components and RF connects to your design by enabling the *Initialize Clearance* option in the *Add Component* and *Add Connect* options pane.



For further details, see the `rf_add_connect` and `rf_add_component` commands in the *Allegro PCB and Package Physical Layout Command Reference.*

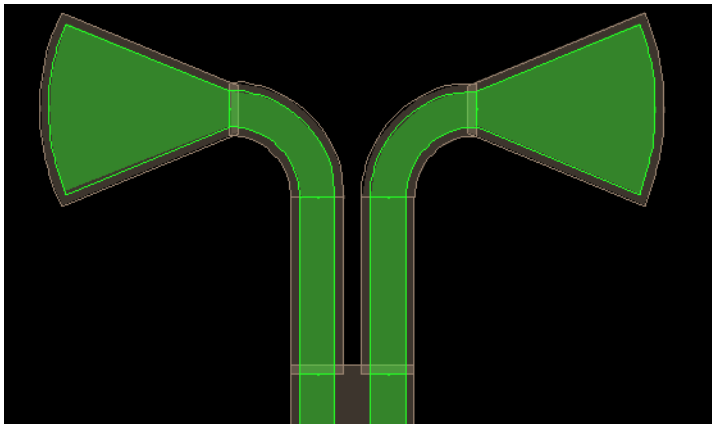
Assembling Clearance Shapes

Clearance shapes can be merged and grouped for better handling. After assembling they behave as a single unit. To assemble various clearance shapes into a clearance assembly, choose *RF-PCB — Clearances — Assemble* or run the `rf_ac_assemble` command.

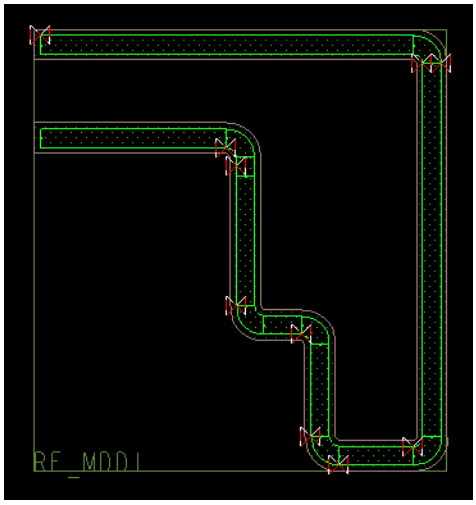
You can also use this command:

- to merge clearance assemblies into a larger one
- to include non-RF objects with clearance shapes to generate a clearance assembly.
- to assemble the clearance shapes for RF components that are part of a replicated block.
- to merge clearance shapes with overlapping or shared boundaries

Figure 5-4 Individual shapes with overlaps

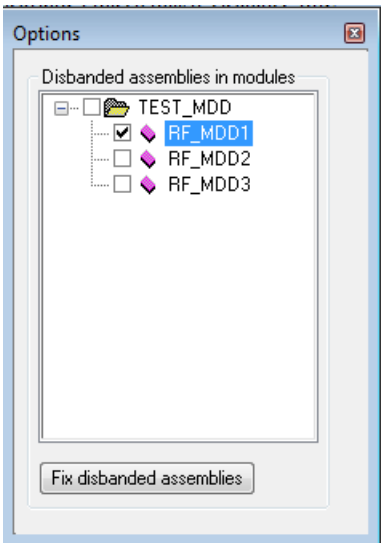


- to resolve DRC errors of shape to route keepout spacing. These DRCs are generated when module instances that have disbanded asymmetrical clearances are instantiated in the design. When a module is placed the route keep out and etch objects are not bound into asymmetrical clearance assemblies.

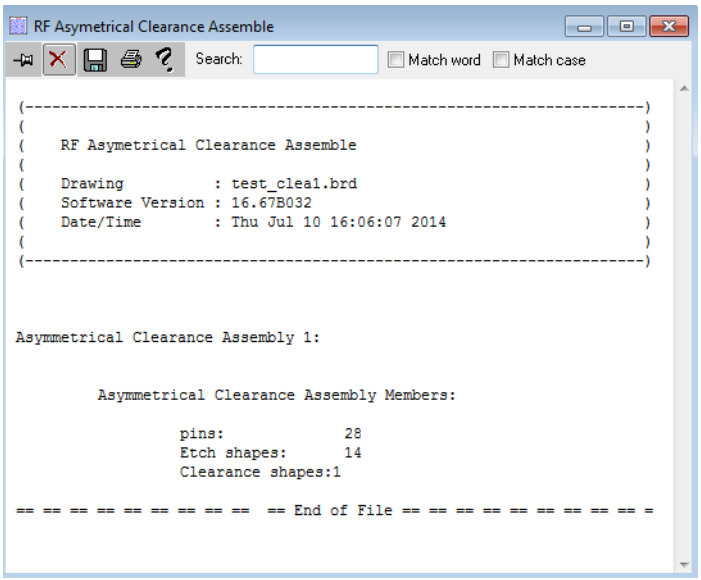


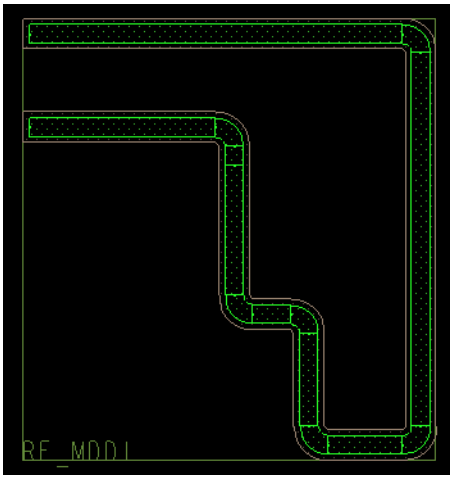
The rf_ac_assemble command includes available route keepout shapes or clearance etch objects (etch shapes, vias, pins and clines) into a clearance assembly. Click on the objects to add the associated clearance shapes into a clearance assembly or choose the module

instances that have disbanded asymmetrical clearances from the *Options* tab. Once the objects are selected click on the canvas or on the *Fix disbanded assemblies* button in the *Options* tab.



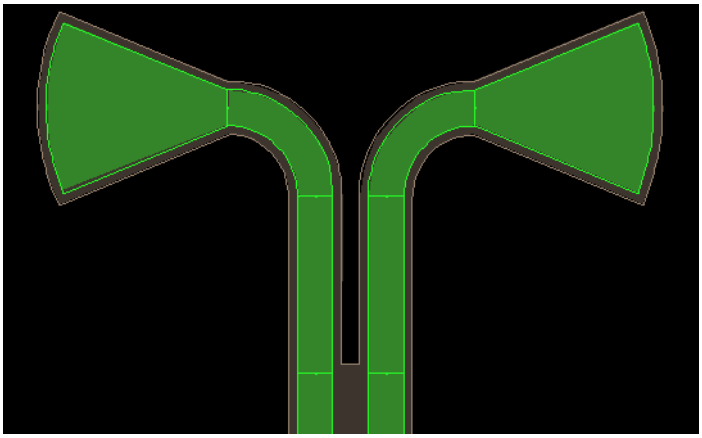
The DRC errors are removed and a report is displayed that contains a summary of the clearance assembly.





Right-click and choose *Done* to create a clearance assembly.

Clearance shapes that have overlapping or shared edges can be merged to create a single clearance shape, by using the *Temp Group* functionality from the right-click menu or by drawing a bounding rectangle to select multiple objects.



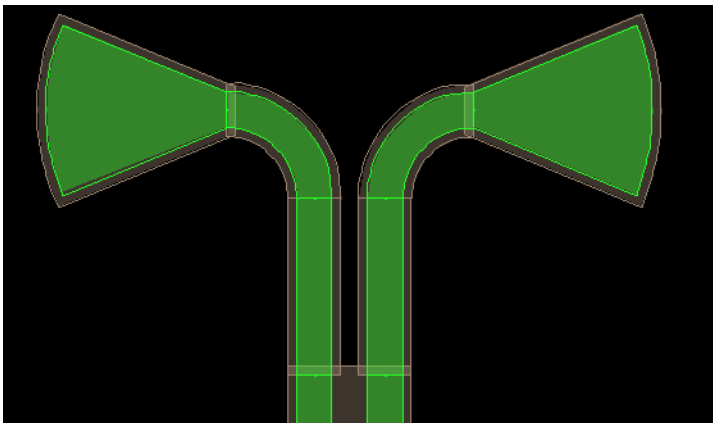
For procedural details, see the `rf_ac_assemble` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Disassembling Clearance assemblies

You can disband all the constituents of a clearance assembly by disassembling the clearance assembly. You can also discard the members of a clearance assembly and re-initialize the clearance shapes for the components.

Choose *RF-PCB — Clearances —Disassemble* or run the `rf_ac_disassemble` command. The options display in the Options pane.

Select an option to either *Retain Clearance Shapes* or *Re-initialize Clearance Shapes* and additionally group them into one clearance assembly. Click on the clearance assembly to discard to highlight. Click again in the design to disassemble the clearance assembly.



If you select *Retain Clearance Shapes*, the clearance assembly is disbanded from the clearance assembly but any modifications done to them are retained. In the *Re-initialize Clearance Shapes* option, the existing clearance assemblies are disbanded and the member clearance shapes are deleted. New clearance shapes are created based on the default settings.

You can also disband the clearance shapes for RF components that are part of a replicated block in the design.

For further details, see the `rf ac disassemble` command in the *Allegro PCB and Package Physical Layout Command Reference.*

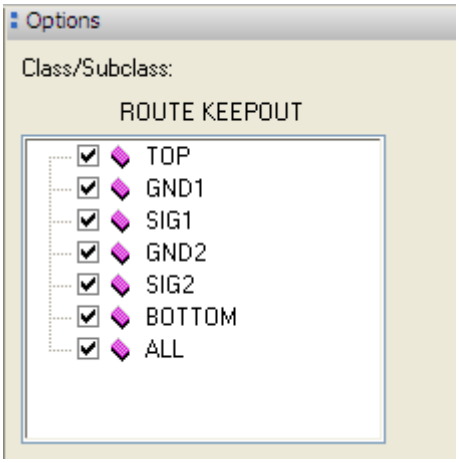
Deleting Clearance shapes

You can delete clearance shapes from a clearance assembly.

Choose *RF-PCB — Clearances —Delete* or run the `rf ac delete` command.

Select the clearance assembly to delete. Use the *Find* filter with *Groups* option to select the clearance assembly. You can select a single clearance shape by clicking on it.

To select multiple clearance assemblies or shapes, use the *Temp Group* option from the right-click menu or draw a bounding box using the mouse.The Options pane displays the layers on which the clearance shapes exist.



Select the layers on which to delete the clearance shapes. Remove the checks from the layers to retain the clearance shapes. Click on the board again to delete the clearance shapes.

You can also delete the clearance shapes for RF components that are part of a replicated block in the design.

Editing clearance shapes

The default clearance shapes can be created using the `rf_ac_init` and the `rf_ac_assemble` commands. These clearance shapes are basic shapes that as a designer you might need to edit.

You can use the Allegro Shape Commands or RF-PCB's *Flexible Shape Editor* to edit the clearance shapes. You can move, spread, and stretch the edges and vertices of the clearance shapes using the Flexible Shape Editor.

Use the Active class and subclass drop-down lists to select the clearance shapes while using the Flexible Shape Editor.

For details on using the Flexible Shape Editor, see Chapter 8, "RF Shape Editing".

6

Display and Measurement

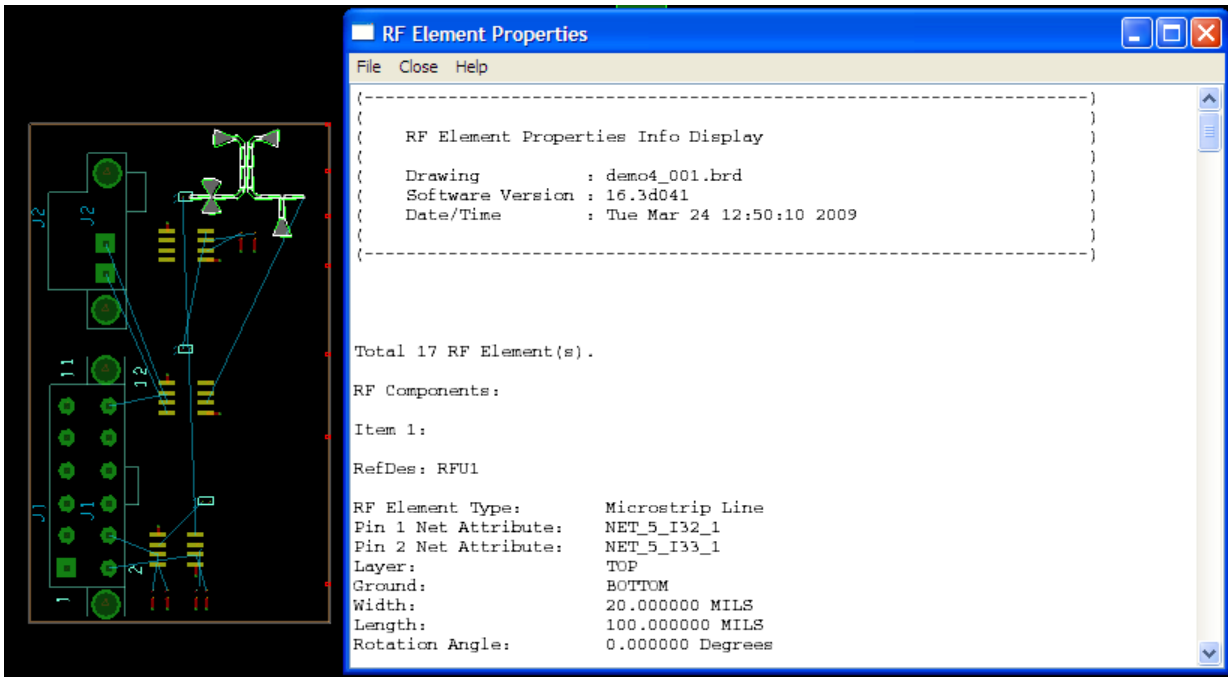
- Displaying RF Component Information
- RF Measuring
  - Measuring a Distance Between Points
  - Measuring a Segment
  - Measuring a Trace
  - Measuring Centered Spacing
- Displaying New RF Components
- Displaying RF Status

Displaying RF Component Information

You can query property information for RF elements by choosing *RF-PCB – Display – Information*. Select the elements by drawing a bounding box around them. All properties for the selected RF elements appear as shown in Figure 6-1. Non RF elements are ignored. When you finish reading the information, close the window, click the right mouse button and select *Done*.

For further details, see the `rf_display_info` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Figure 6-1 Display of RF Element Properties



RF Measuring

The following measurement types are available in RF PCB:

- General
- Segment
- Trace
- Centered

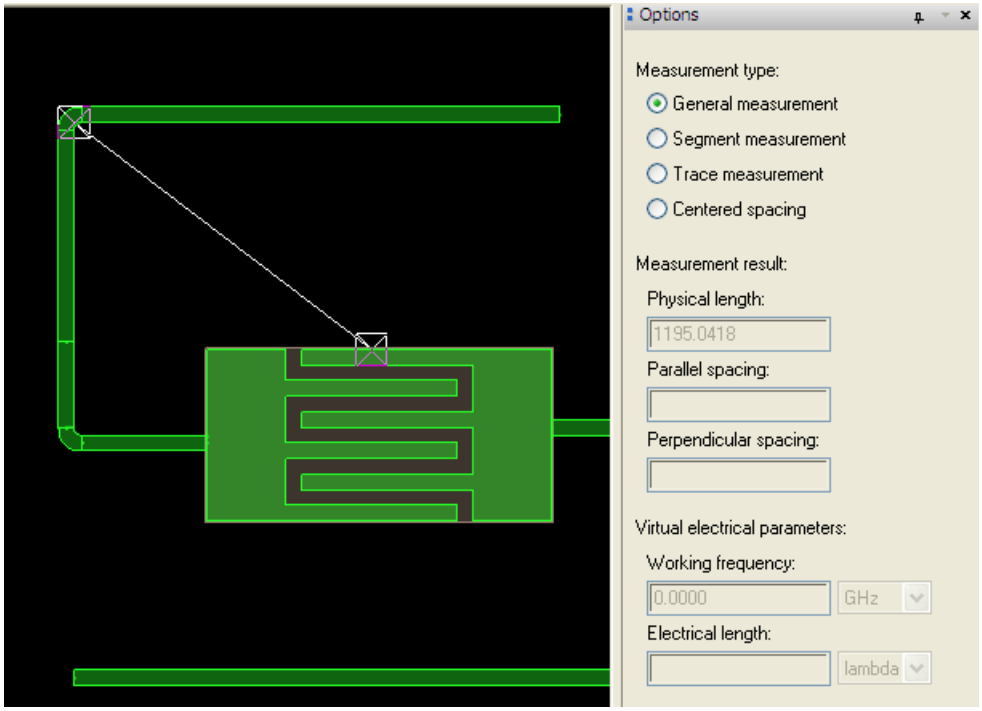
You measure objects by choosing *RF-PCB – Display – Measurement*. Choose a measurement type from the Options pane, then select objects to measure. Once you have read the measurement information in the Options pane, click the right mouse button and select *Done*.

Measuring a Distance Between Points

When you choose *General Measurement* from the Options pane, you can measure the distance between any two points that you click on in the design. The result is displayed in the *Physical Length* field in the Options pane.

Note: The electrical length is not available with a general measurement.

Figure 6-2 Measuring a distance between two points



Measuring a Segment

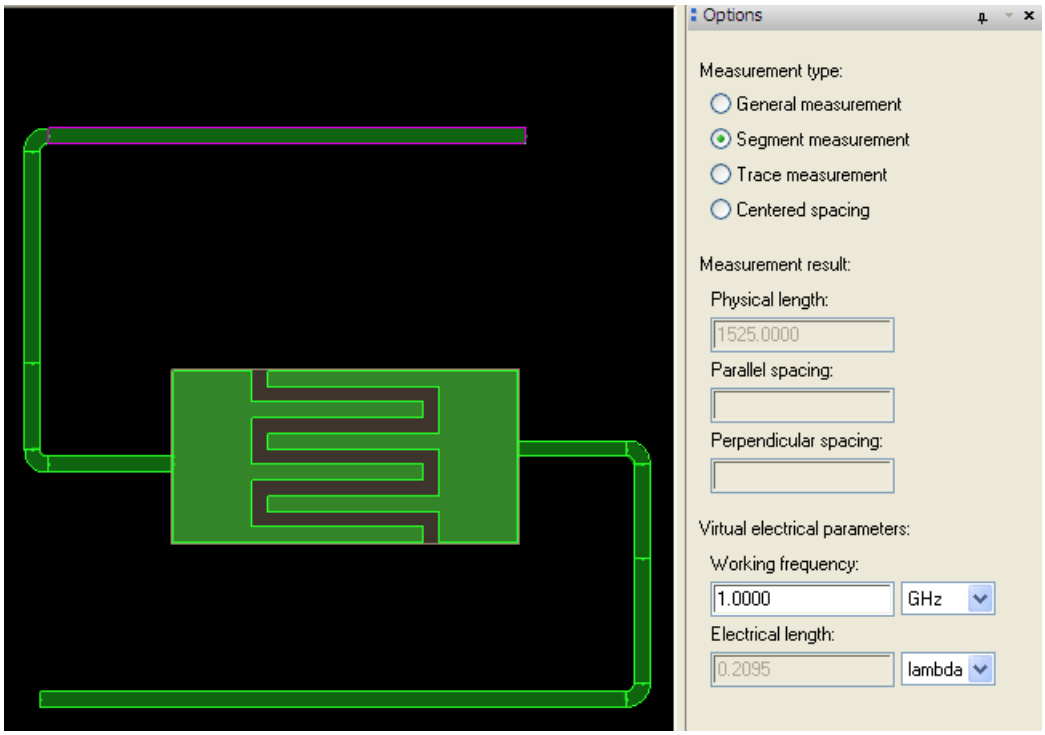
When you choose *Segment Measurement* from the Options pane, you can click on a trace segment to highlight it, and then read its length measurement in the *Physical Length* field.

Note: If you had previously entered a value in the *Virtual Working Frequency* field, you can also read the electrical length of the trace segment in the *Electrical Length* field.

An RF trace segment may be:

- a microstrip line or stripline
- a bend
- a curved line
- a meander line

Figure 6-3 Measuring an RF trace segment

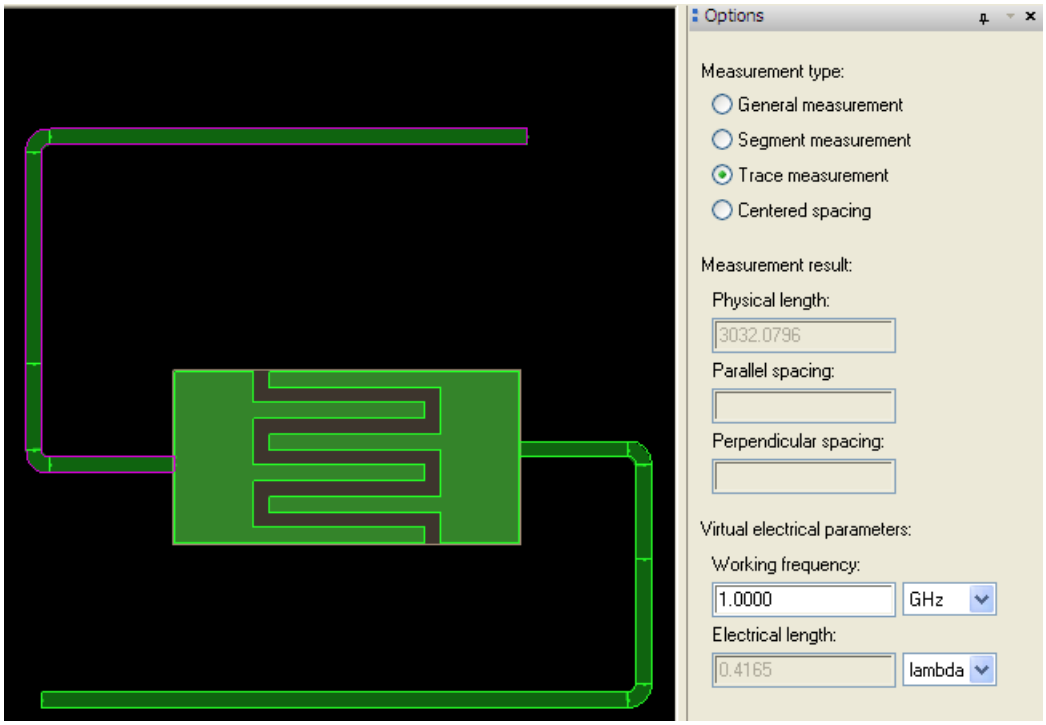


Measuring a Trace

When you choose *Trace Measurement* from the Options pane, you can click a trace to highlight it and read its total length in the *Physical Length* field. If you had previously entered a value in the *Virtual Working Frequency* field, you can also read its electrical length in the *Electrical Length* field.

Note: An RF trace consists of one or more consecutive RF segments. Therefore, a non-RF segment or component between two RF segments is divisive and creates two RF traces.

Figure 6-4 Measuring a whole trace



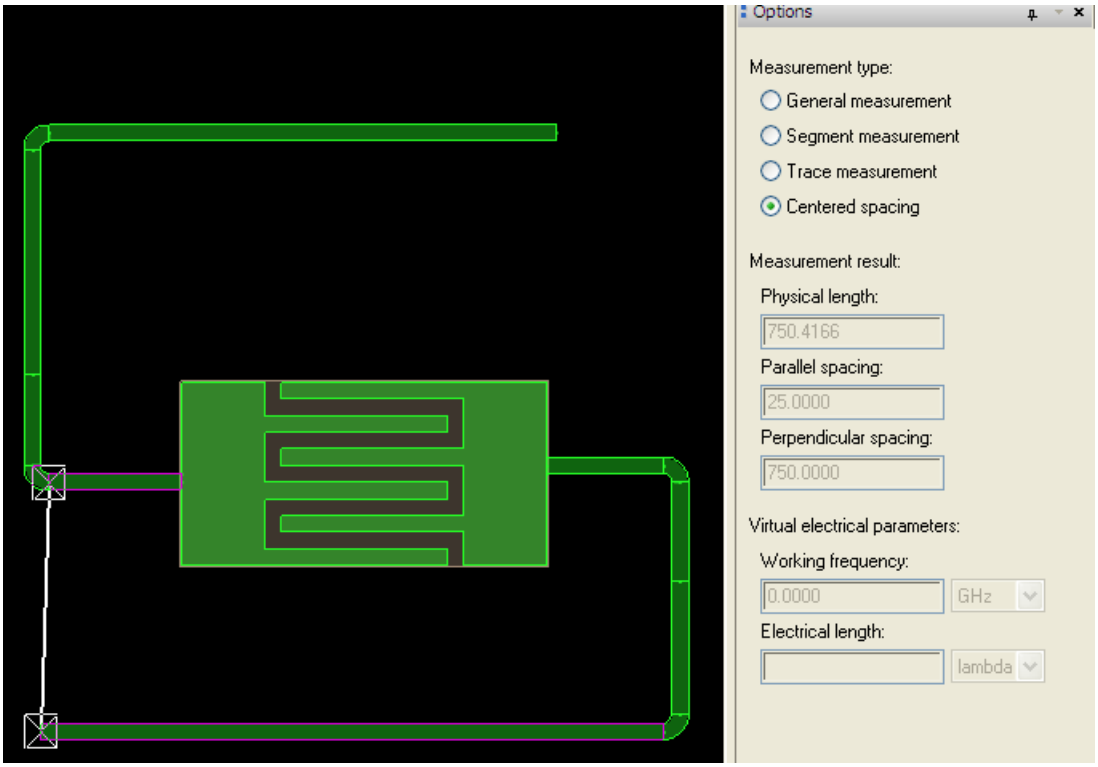
Measuring Centered Spacing

When you choose *Centered Spacing* from the Options pane, you can click on any two RF segments to highlight them and read the shortest distance between them in the *Physical Length* field. You can also read *Parallel Spacing* (Dx) and *Perpendicular Spacing* (Dy) values.

Note: Only select RF segments for centered spacing measurement. An RF segment may be one of the following:

- microstrip line or stripline
- bend
- curved line
- meander line

Figure 6-5 Measuring centered spacing between two RF segments

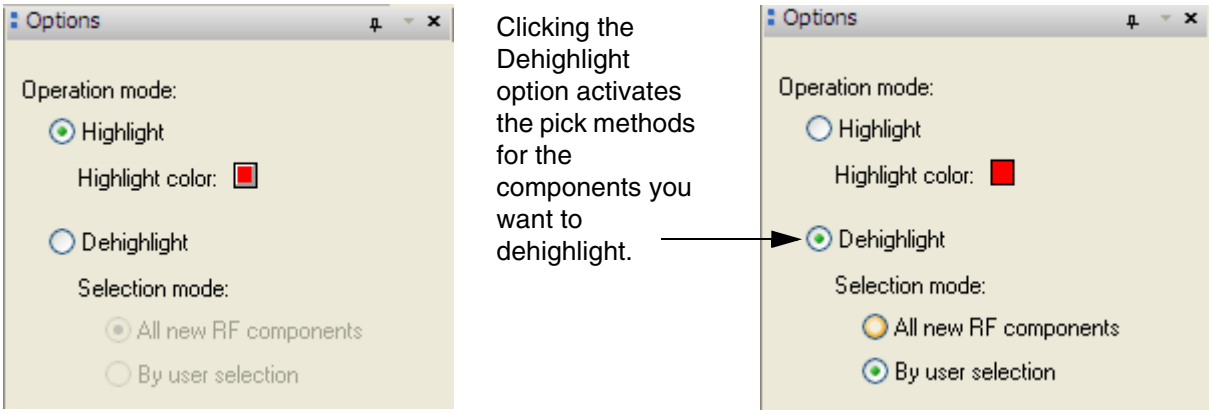


For further details, see the `rf_measure` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Displaying New RF Components

To differentiate newly created RF components from existing components, the tool automatically highlights them in the design using the default color for permanent highlights. You can change the default color in the Assign Color dialog box. Choose *RF-PCB – Display – New Component* to display the highlighted new components and to dehighlight them as necessary.

Figure 6-6 Highlighted new RF components



Note: All newly created RF components have the RFNEWCOMP property attached to them.

There are two methods of selection for dehighlighting components:

- All new RF components
- By user selection

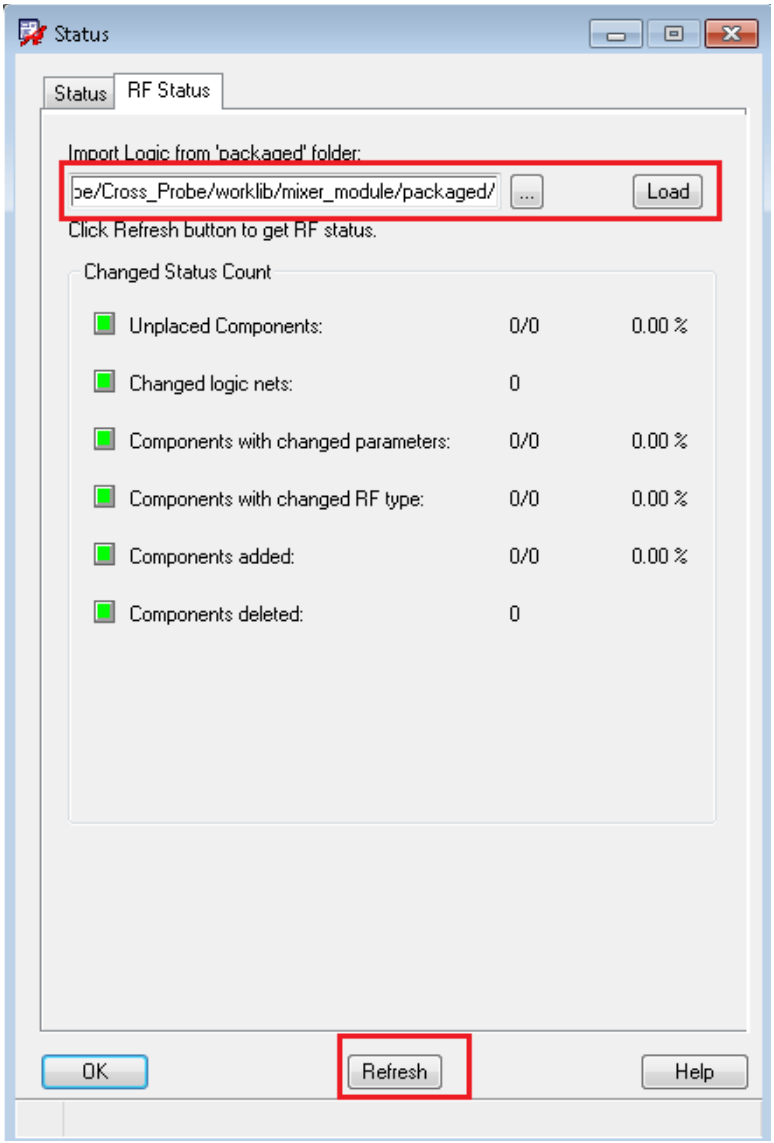
Important

Dehighlighting cannot be undone.

Displaying RF Status

Any change in the design for RF components can be seen in the layout using `status` command.

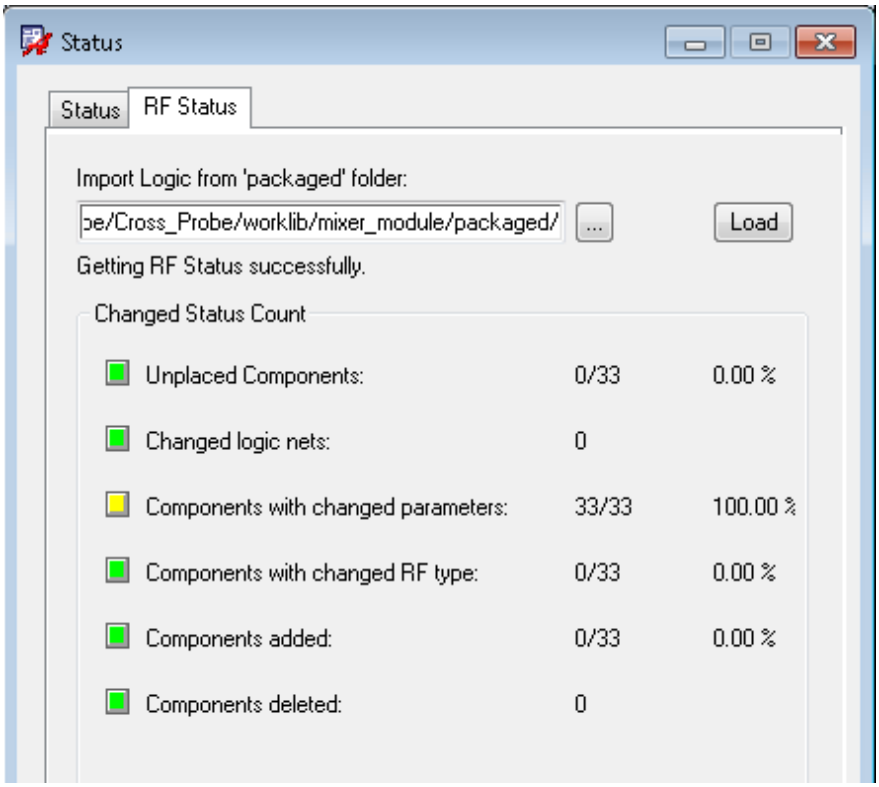
If Analog/RF option is enabled a separate tab RF Status is displayed in the *Status* dialog box. All the changes specific to RF components are listed here.



These changes are displayed when you compare the layout design data with schematic design data. The command compares packaged files (`pstxnet.dat, pstxprt.dat`) and physical design data.

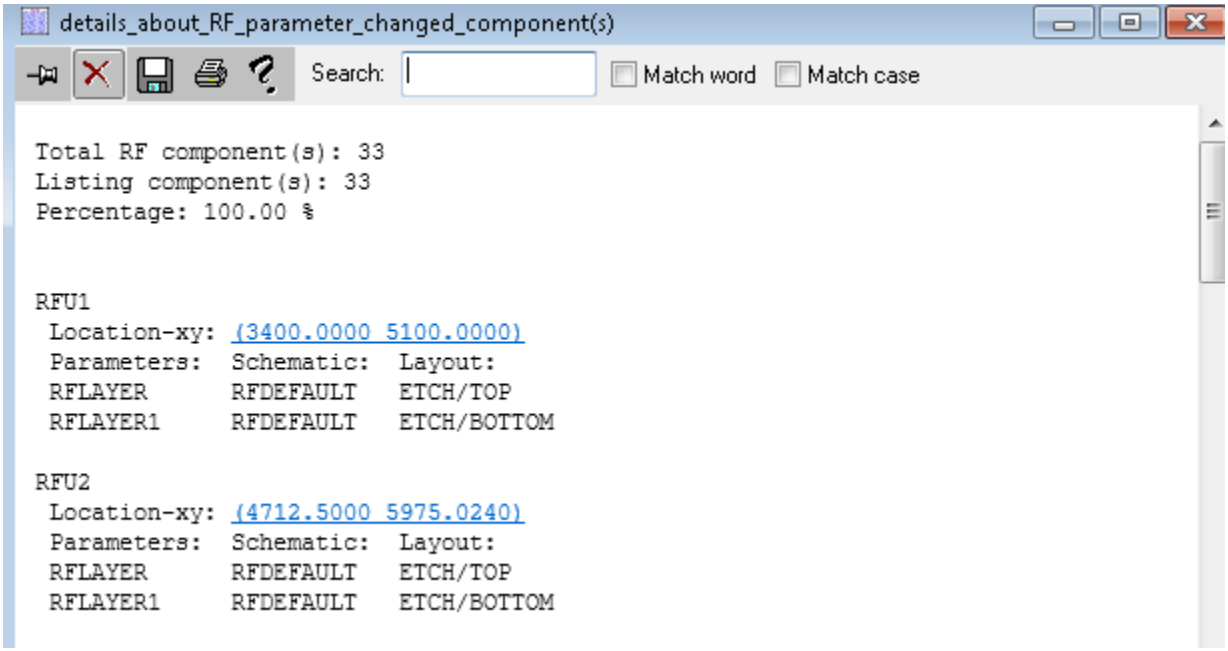
To view the changes you need to load packaged files directory and refresh the dialog box.

The physical design data is compared with schematic design data and produce results for following differences:



The color of the swatch changes from green to yellow if there is any difference between schematic design and physical design.

On clicking the color swatch for a selected change, a detailed report showing all the differences is displayed. For example, details of components with changed parameters are displayed in `details_about_RF_parameter_changed_component(s) r`eport.



7

RF Converting

- Smooth for RF Routing
  - Tapered Pin Connection
  - Chamfer
- Defining a Custom RF Component
- Changing RF Components to Shapes
- Converting Clines to RF Transmission Line Components

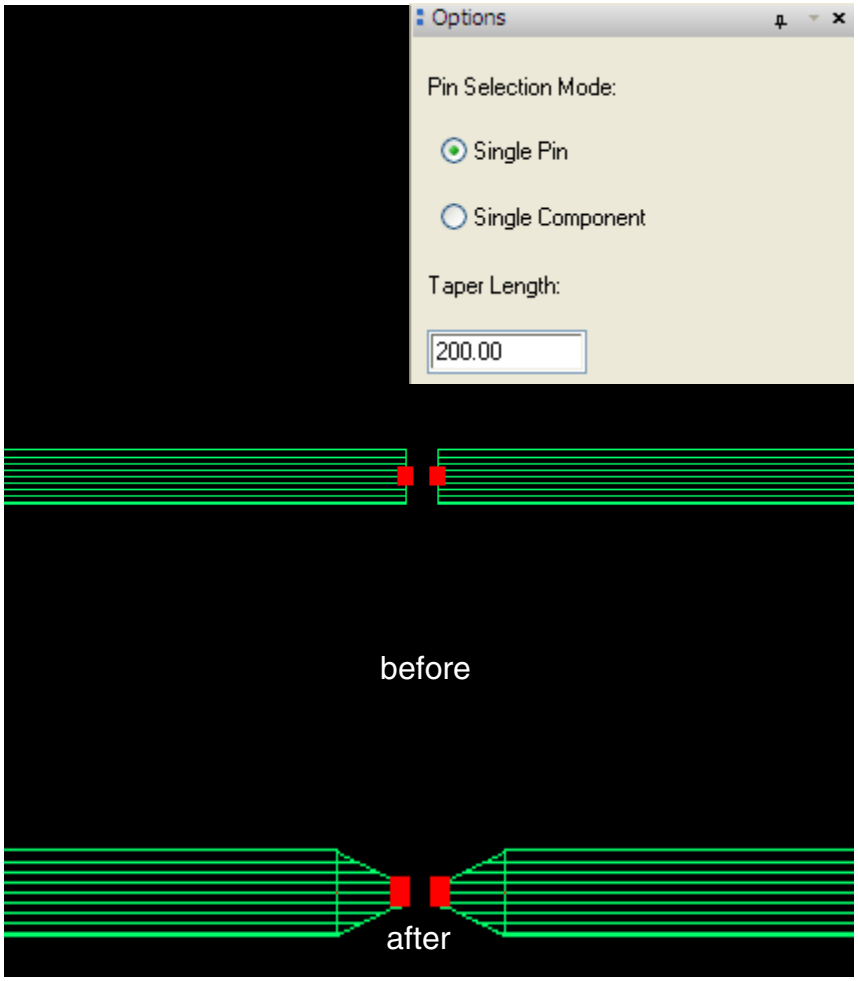
Smooth for RF Routing

Once you complete RF placement and routing, you can perform smooth operations on the interconnect, such as tapered connections and chamfers.

Tapered Pin Connection

To initiate a tapered pin connection, choose *RF-PCB – Convert – Tapered Pin Connect*. In the Options pane, specify the taper length from a pin of the non-RF component (for example, an IC or connector or discrete) to the RF trace, then choose one or all of the component pins for modification. Figure 7-1 shows a tapered pin operation.

Figure 7-1 Tapered pin connection



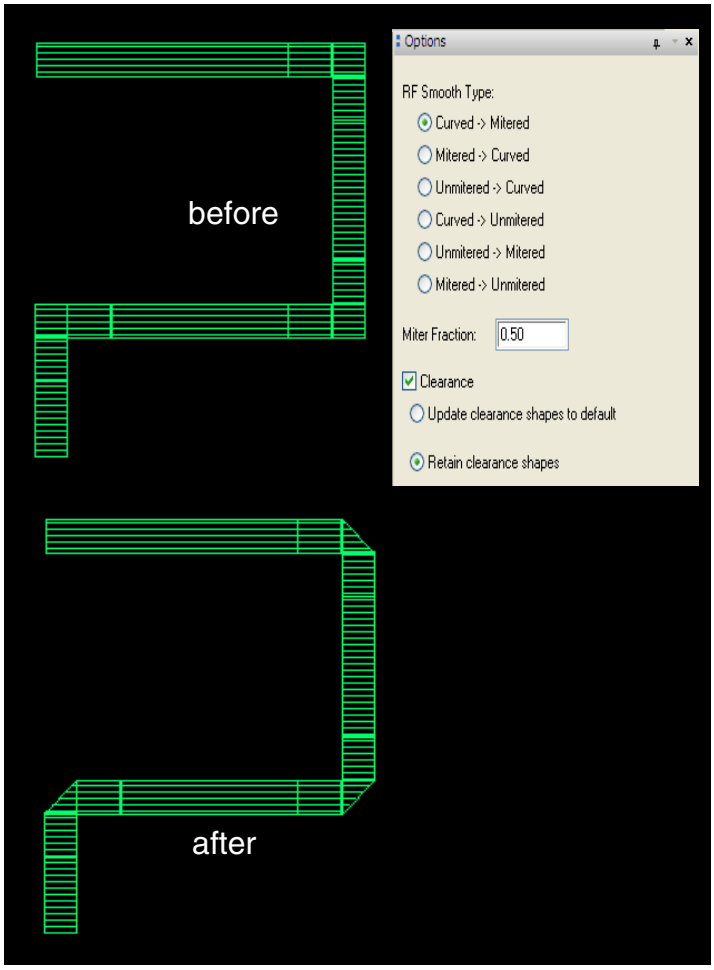
Note: You cannot handle active or lumped components with RF properties using this command. You can, however, insert a width taper to connect to the pin/pad of the component.

For further details, see the `rf_tapered_connect` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Chamfer

To initiate a corner smoothing operation, choose *RF-PCB– Convert – Chamfer*. Select the smoothing type, then click on a trace to be modified. Figure 7-2 shows a chamfering operation.

Figure 7-2 RF trace chamfering



This command handles all bends on a trace line (straight lines, curved lines, and bends) simultaneously. If multiple components exist in the trace, then you need to repeat the operation for each one.

For further details, see the `rf chamfer` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Defining a Custom RF Component

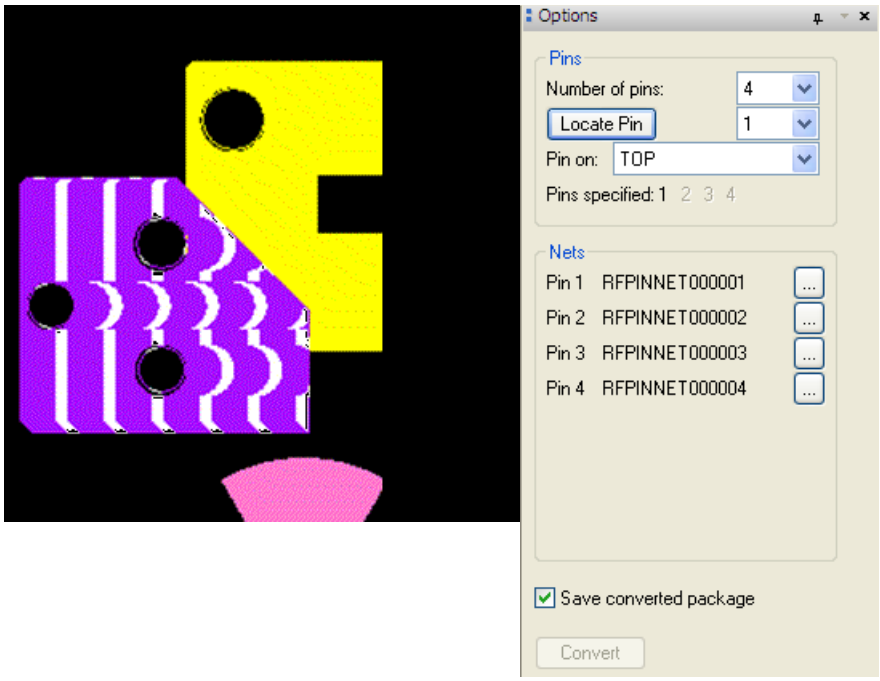
You can convert one or more static shapes or vias to a component and save it for reuse by choosing *RF-PCB – Convert – Shape to Component*. On the *Pins* area in the Options pane, you specify the total number of pins for the component and then choose the location for each one on the shapes selected for conversion. Optionally, you can assign a net to each pin in the *Nets* area. Figure 7-3 shows a shape to component conversion in progress.

For each pin, you must first specify its ID in the Options pane, followed by its location on the shape. You can check the *Save converted package* option to save the component to a file for future use.

Note: Shape to component conversions currently have the following parameters:

- You cannot convert dynamic shapes.
- You can specify no more than 8 pins for a user-defined component.
- You can use multiple static shapes on different layers to define the component.
- You cannot convert a shape already owned by an RF component.
- The shape can include voids, but you cannot locate a pin on an arc edge.
- You can select vias along with the shapes to convert. This will cause the vias to be included in the RF component after conversion.

Figure 7-3 Converting a shape to a component

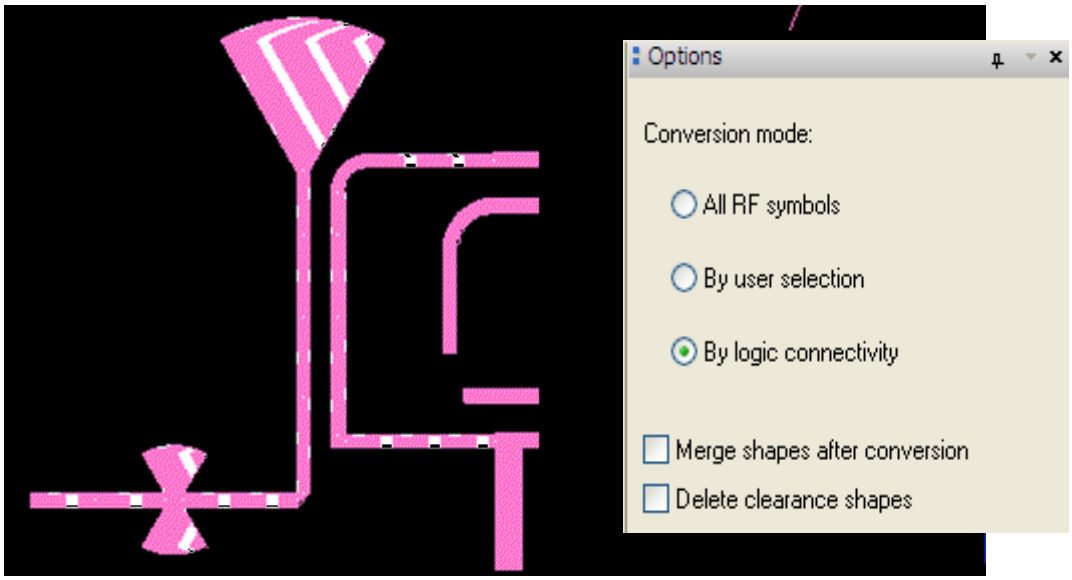


For further details, see the `rf_shape2component` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Changing RF Components to Shapes

You can convert RF components to shapes in your design by choosing *RF-PCB – Convert – Component to Shape.* Choose a conversion mode in the Options pane, then select the components to change. Only shape-type components are selected and highlighted. If you enable (check) the *Merge shapes after conversion* option, once the conversion is complete, all connected shapes will merge together to form a single shape. If you enable (check) *Delete clearance shapes*, any clearance shapes attached to the RF component are deleted. Figure 7-4 shows a component to shape conversion in progress.

Figure 7-4 Changing Components to Shapes



For further details, see the `rf component2shape` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Converting Clines to RF Transmission Line Components

You can use clines to connect RF components and later convert them to compatible RF transmission line components by choosing *RF-PCB – Convert – Cline to Tline Conversion*. All clines in a group have the same net logic, but the converted RF transmission line components will have different net logic names.

Currently, not all combinations of cline topologies convert. You can use the following cline topologies for conversion:

- No Tpoint – uses RF transmission line components of MLIN, SLIN and proper bends and curves during conversion.
- Tpoint with three or four connected segments and a connection angle of 90 degrees – uses RF transmission line components of MLIN, SLIN and proper cross junctions, T junctions, bends, and curves during conversion.

You can use the following RF transmission line component types in the decomposition:

For clines on surface etch layers

- MBEND – map connection of two segments at any angle

- MCROS – map connection of four segments at 90 degrees
- MCURVE – map arc segment
- MLIN – map single segment
- MTEE – map connection of three segments at 90 degrees

For clines on internal etch layers

- SBEND – map connection of two segments at any angle
- SCROS – map connection of four segments at 90 degrees
- SCURVE – map arc segment
- SLIN – map single segment
- STEE – map connection of three segments at 90 degrees

The following cline topologies are not supported:

- T point with more than 4 connected segments – the tool cannot perform the conversion and will issue error messages.
- T point with non-90 connection angle – the tool cannot perform the conversion and will issue error messages.
- Multiple clines connect to single pin – introduces ambiguities in the net logic.
- Cline that contains connected segments with different widths and the connection angle is non-zero – there is no compatible RF bend component.
- Cline that contains connected line and arc segments, and the line is not tangent to the arc at the connection point – there is no compatible RF bend component.

Cline to RF Components Mapping

The following are diagrams for cline to RF components mapping:

Single Cline Segment

If you use a single cline segment to connect:

- Two pins
- One pin and an etch shape

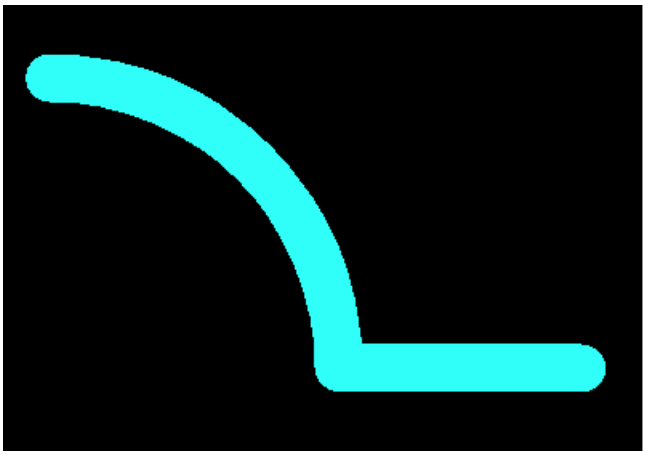
- Two etch shapes

The cline segment converts to an RF line or arc component.

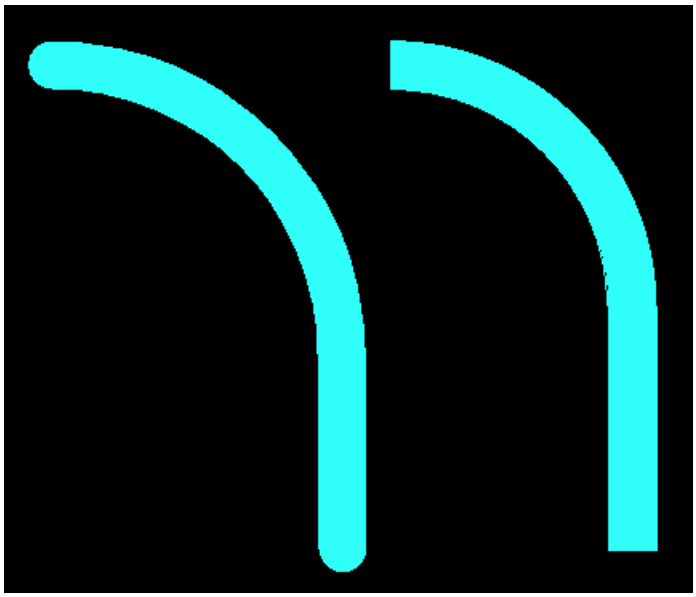
Two Connected Segments

If two cline segments connect together at an angle between 0 and 180 degrees, they convert into two RF line components with a bend.

You cannot convert a structure that contains a line segment connecting to an arc segment when the line segment is not tangent to the arc segment at the connection point:



Note: However, the tool supports conversion of a structure that contains a line segment connecting to an arc segment when the line segment is tangent to the arc segment at the connection point:

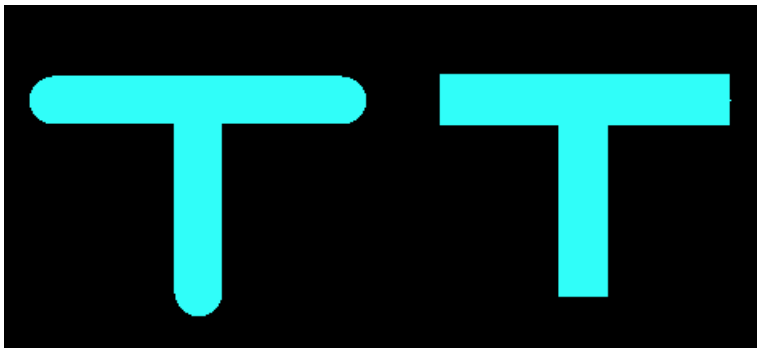


The tool cannot convert two connected segments with different widths when the connection angle is not zero:

If the connection angle is zero, the tool converts them to two connected RF line components:

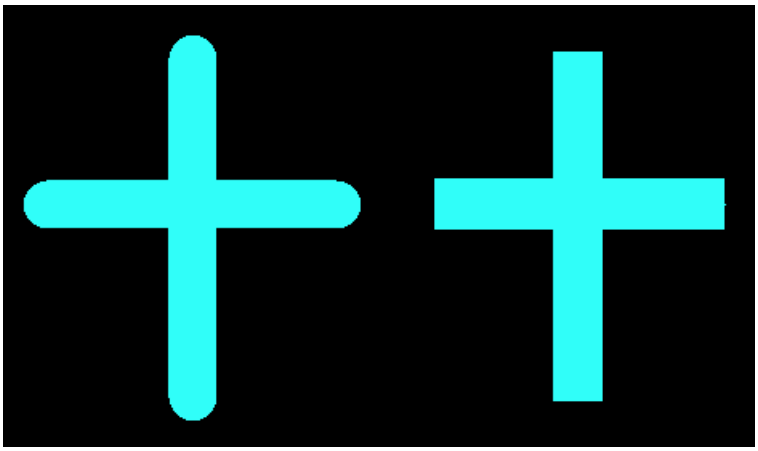
Three Connected Line Segments

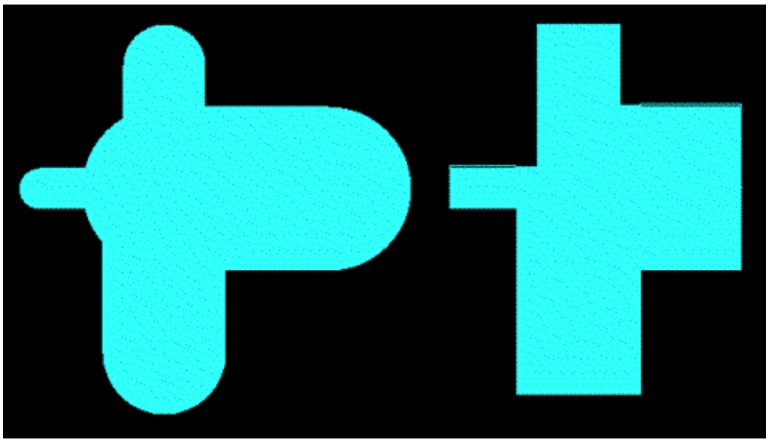
If three line segments connect together at right angles, the tool converts them to RF line components and an RF T component.



Four Connected Line Segments

If four line segments connect together at right angles, then they convert to an RF line component and an RF cross component.





8

RF Shape Editing

- Overview
- Shape Edge Editing
  - Moving an Edge
  - Stretching an Edge
  - Spreading an Edge
- Line Segment Drawing
  - Drawing a Tangent Line
  - Drawing a Tangent Arc
  - Connecting Two End Points with a Line
  - Breaking and Deleting Extra Lines or Segments in a Shape Outline
- Shape Vertex Editing
  - Inserting a Vertex
  - Moving a vertex
  - Converting a Vertex
- Whole Shape Editing
  - Shape Operations
  - Shape Corners Edit
  - Shape Scale / Copy
  - Multi-layer Shape Zcopy

Overview

The Flexible Shape Editor (FSE) enhances the shape editing capability already available in PCB Editor. It provides powerful shape editing functionality that helps meet current RF design requirements. FSE offers four basic types of shape editing operations:

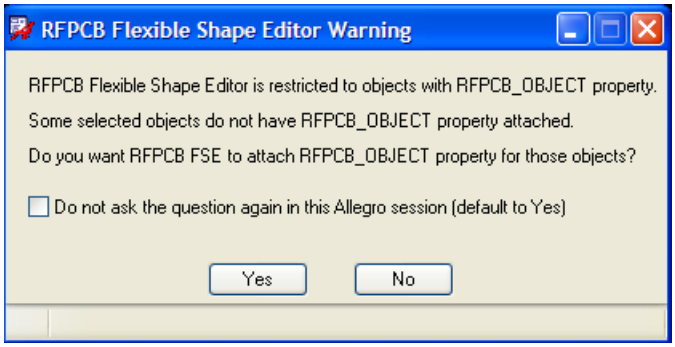
- Shape edge editing
- Line segment drawing
- Shape vertex editing
- Whole shape editing

You access FSE commands by choosing *RF-PCB – Flexible Shape Editor*.

Usage Restriction

Usage of the Flexible Shape Editor in Allegro PCB Editor is currently restricted to objects (shapes and lines) with the RFPCB_OBJECT property. If you invoke an FSE command and then select an object that does not have this property, the warning shown in Figure 8-1 is presented.

Figure 8-1 Flexible Shape Editor Warning



Clicking *Yes*, attaches the RFPCB_OBJECT property to the object and allows you to continue on with the FSE command. If you enable the *Do not ask. . .* option, the warning is turned off for the remainder of the current Allegro session. By turning off the warning, FSE commands automatically attach RFPCB_OBJECT property to selected objects that do not already have this property attached.

Note: RFPCB_OBJECT is a visible Allegro system property that applies to shapes and lines. Its value type is BOOLEAN. You can add or remove this property on shapes or lines to enable

or disable RFPCB FSE operations on them. For further details, see the property edit command in the *Allegro PCB and Package Physical Layout Command Reference*.

Shape Edge Editing

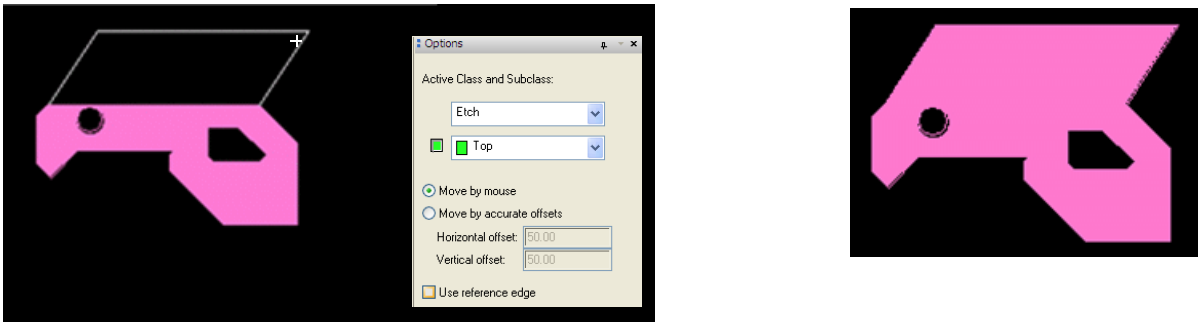
The shape edge editing commands operate on shape boundaries including voids. Shapes selected for editing can be filled or unfilled, dynamic or static, and etch or non-etch.

Moving an Edge

Choose *RF-PCB – Flexible Shape Editor – Edge Move* to offset a shape edge in a free direction while maintaining its original slope. You can choose to specify the offset distance using a mouse pick, by x and y offset values measured from the start point of the edge. You can also decide to use a reference edge and move the edge relative to the reference edge.

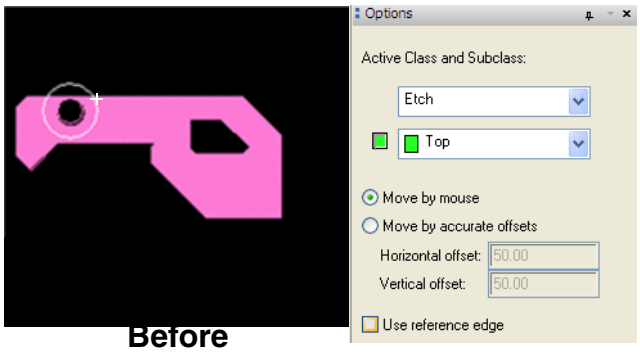
Examples

Figure 8-2 Moving a straight edge



Before **After**

Figure 8-3 Moving a circular edge



Before

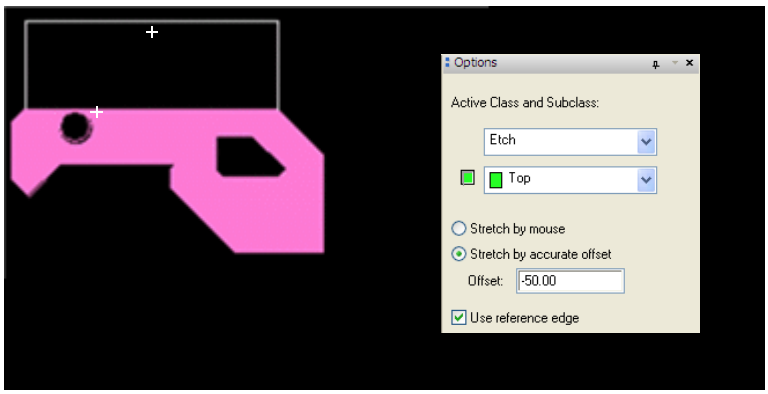
After

For further details, see the `fse edge move` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Stretching an Edge

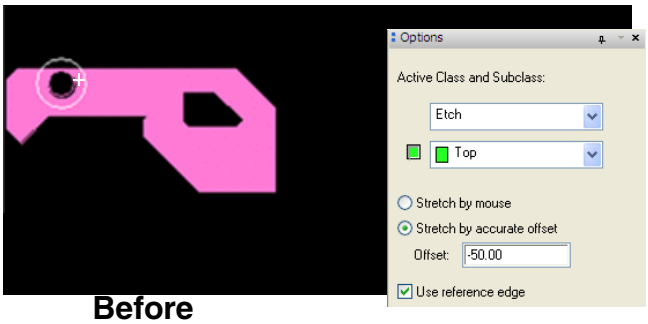
Choose *RF-PCB – Flexible Shape Editor – Edge Stretch* to stretch an edge to a new position in a direction perpendicularly to the edge itself. The offset value represents a distance from the end point of the segment in the two-dimensional Cartesian coordinate system. A positive offset implies that the destination point is horizontally to the right and/or vertically above the referenced point. A negative offset always implies the destination point is horizontally to the left and/or vertically below the referenced point. You can choose to specify the offset distance using a mouse pick or by an input value. You can also use a reference edge and stretch the edge relative to the reference edge.

Figure 8-4 Stretching a straight edge (perpendicular direction)



After

Figure 8-5 Stretching a circular edge (same effect as moving)



Before

After

For further details, see the `fse_edge_stretch` command in the *Allegro PCB and Package Physical Layout Command Reference.*

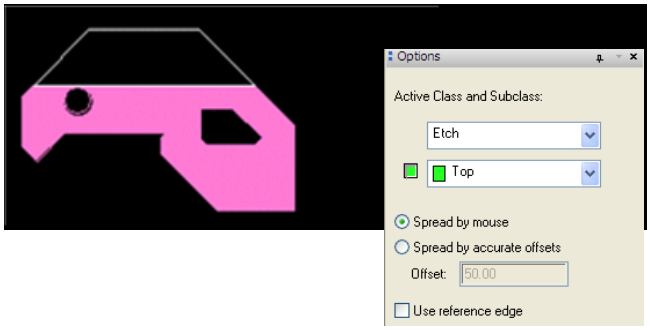
Spreading an Edge

Choose *RF-PCB – Flexible Shape Editor – Edge Spread* to offset an edge to a new position while maintaining the angles of it's two adjacent edges. A positive stretch offset indicates an offset to the outside of the shape and a negative stretch offset indicates an offset to the inside of the shape. You can choose to specify the offset distance using a mouse pick, or by x and y offset values measured from the start point of the edge. You can also use a reference edge and spread the edge relative to the reference edge.

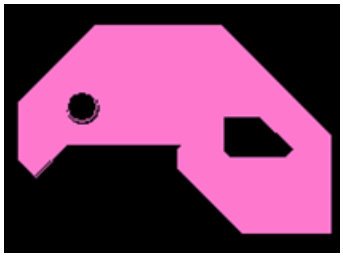
Note: An edge spread is not possible in cases where there is an arc edge between the two adjacent edges.

Examples

Figure 8-6 Spreading a straight edge



Before



After

Note: Spreading a circular or an arc edge has the same effect as stretching a straight edge.

For further details, see the `fse edge spread` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Line Segment Drawing

Line segment drawing commands create tangent line or arc segments. The line segments that are created are not connect line segments (cline segments) nor can you select cline segments to draw from.

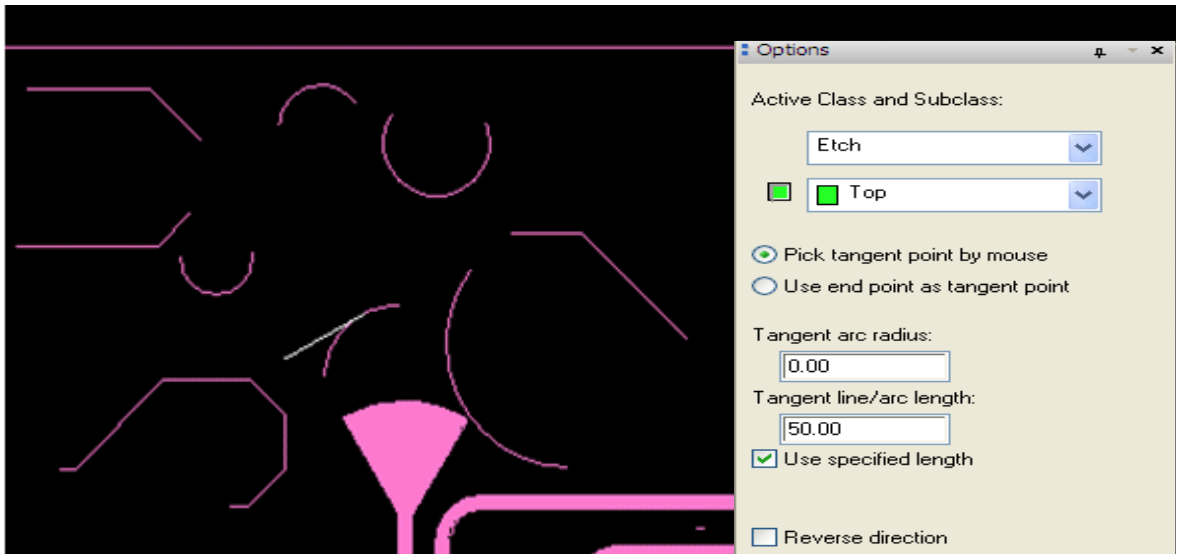
You can draw a tangent line segment from a point on an existing arc. You can also draw an arc segment from a point on an existing line or arc. Indicate the start point using a mouse pick on a selected line or arc. You can also choose to designate the start point as the end point of a selected line or arc.

Drawing a Tangent Line

Choose *RF-PCB – Flexible Shape Editor – Tangent Segment*. Select the *Mouse Pick* option in the Options pane and specify the radius as 0 (indicating a line segment). Click on an arc to indicate the start point for the tangent line. Determine the segment length with an additional mouse pick or by specifying an absolute length in the Options pane.

Example

Figure 8-7 Drawing a tangent line



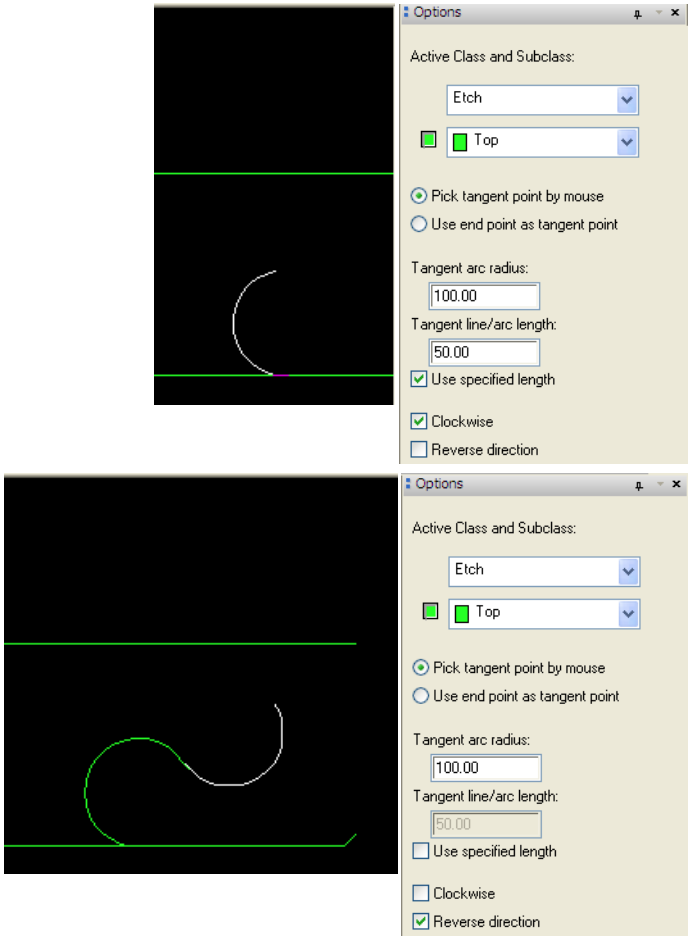
Note: After you draw a tangent line segment, the original arc segment is cut into two arc segments. You can delete the one you don't want by choosing *Edit – Delete* (remember to select *Other Seg* in the filter option list).

Drawing a Tangent Arc

Choose *RF-PCB – Flexible Shape Editor – Tangent Segment*. Select the *Mouse Pick* option and specify a positive (non-zero) value for the arc radius. Click on the line or the arc to indicate the start point for the tangent arc. Determine the arc length with an additional mouse pick or by specifying an absolute length in the Options pane.

Examples

Figure 8-8 Drawing a tangent arc



For further details on drawing tangent line or arc segments, see the `fse seg tangent` command in the *Allegro PCB and Package Physical Layout Command Reference.*

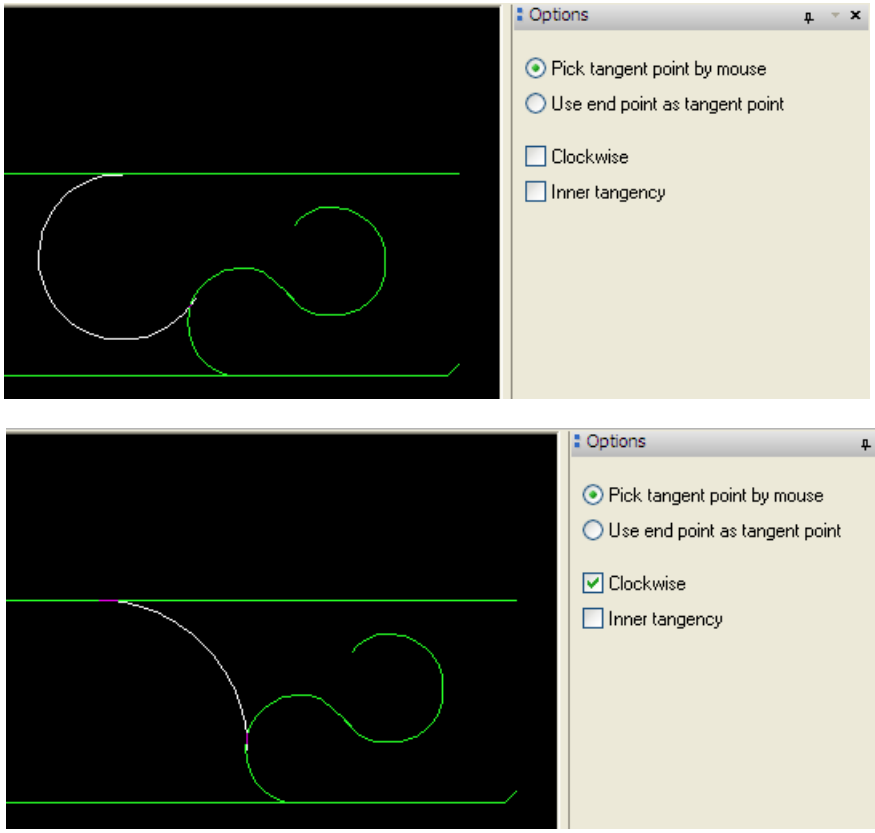
Connecting two points with a tangent arc

You can connect any two points on different line or arc segments with a tangent arc by choosing *RF-PCB – Flexible Shape Editor – Arc Tangent*. Select the *Mouse Pick* option, then click on lines or arcs to indicate the start and end points for the tangent arc. You can also select the *End Point* option and click near the endpoints of lines or arcs to use. After the two points are connected with a tangent arc, you can delete line segments that you don't need by choosing *Edit – Delete*.

For further details, see the `fse_arc_tangent` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Examples

Figure 8-9 Connecting two end points with a tangent arc



Connecting Two End Points with a Line

You can connect two end points of two line or arc segments by choosing *RF-PCB – Flexible Shape Editor – Line End Connect*. Simply click on the two endpoints to connect them with a line segment.

For further details, see the `fse_end_connect` command in the *Allegro PCB and Package Physical Layout Command Reference.*

Breaking and Deleting Extra Lines or Segments in a Shape Outline

You can create a freeform shape by drawing an outline and then converting it to a filled shape. If extra lines exist, you can remove them without breaking the shape by choosing *RF-PCB – Flexible Shape Editor – Break and Delete*. Instead of deleting the whole line, Allegro lets you delete a portion of a line from your mouse-click point to any intersection point with another line or until the end of a line.

As shown in Figure 8-10, the *Break and Delete* command searches in both directions from the mouse-click point on the line until the first intersection point or an end of the line is found.

Examples

Figure 8-10 Lines with at least one intersection point

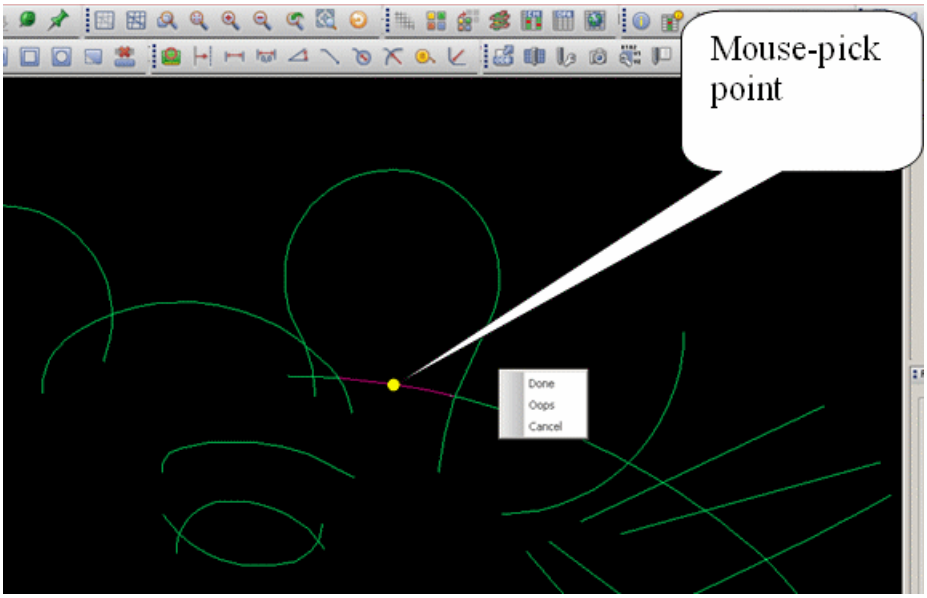


Figure 8-11 shows another example of deleting a line segment between an end point on one side and an intersection point on the other side.

Figure 8-11 Deleting a line segment between an end point and an intersect point

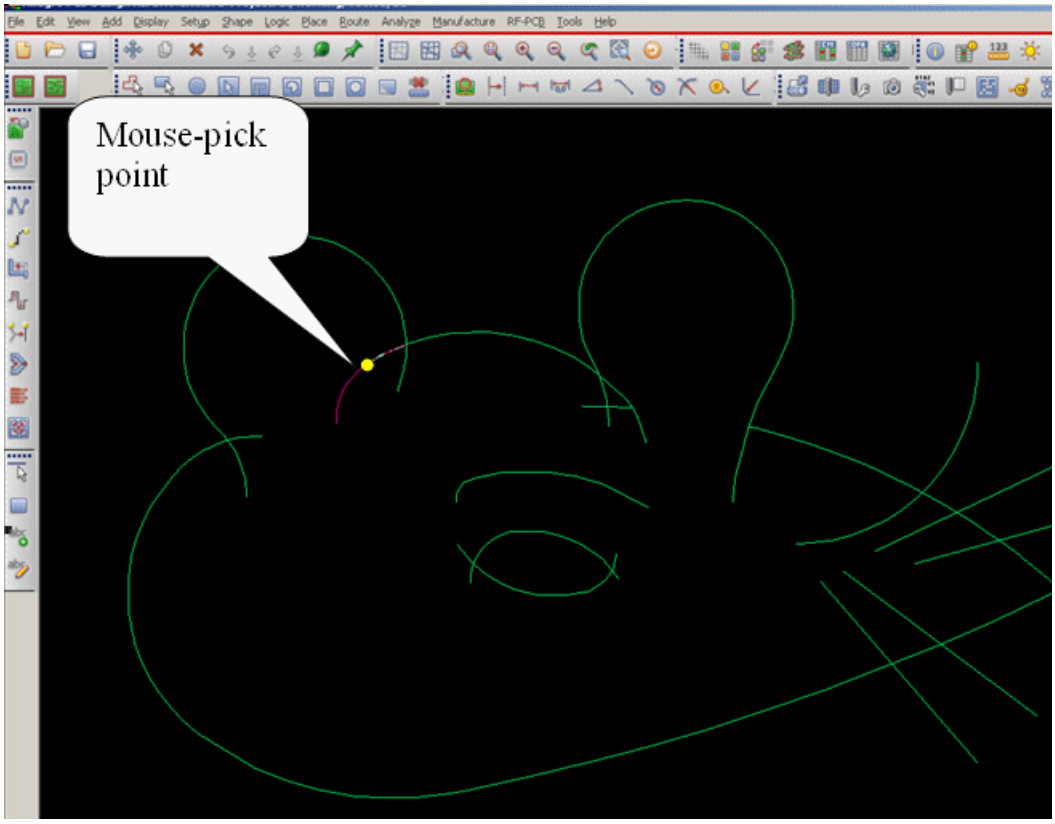
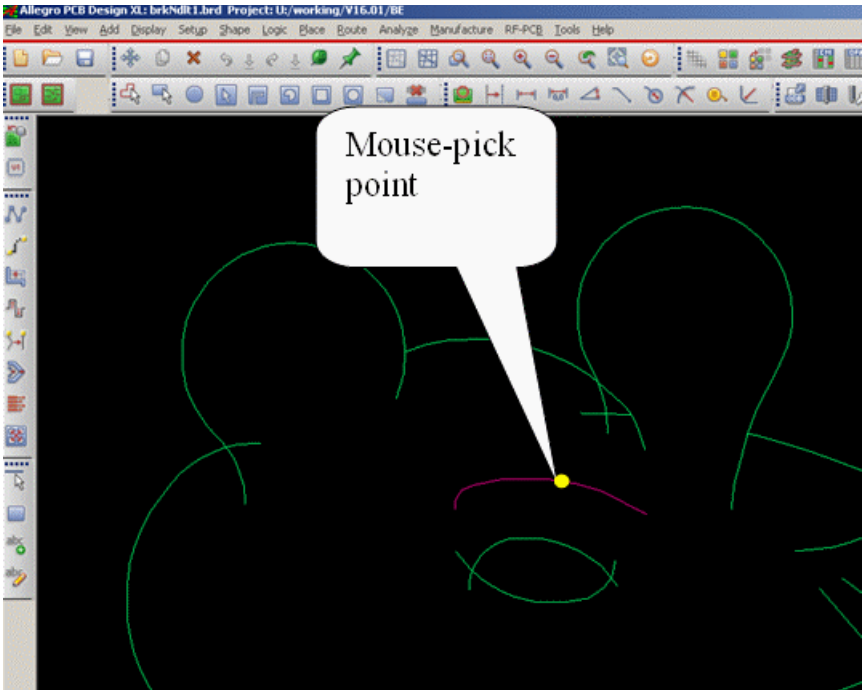


Figure 8-12 shows an example of deleting an isolated line that has no intersection with any other line.

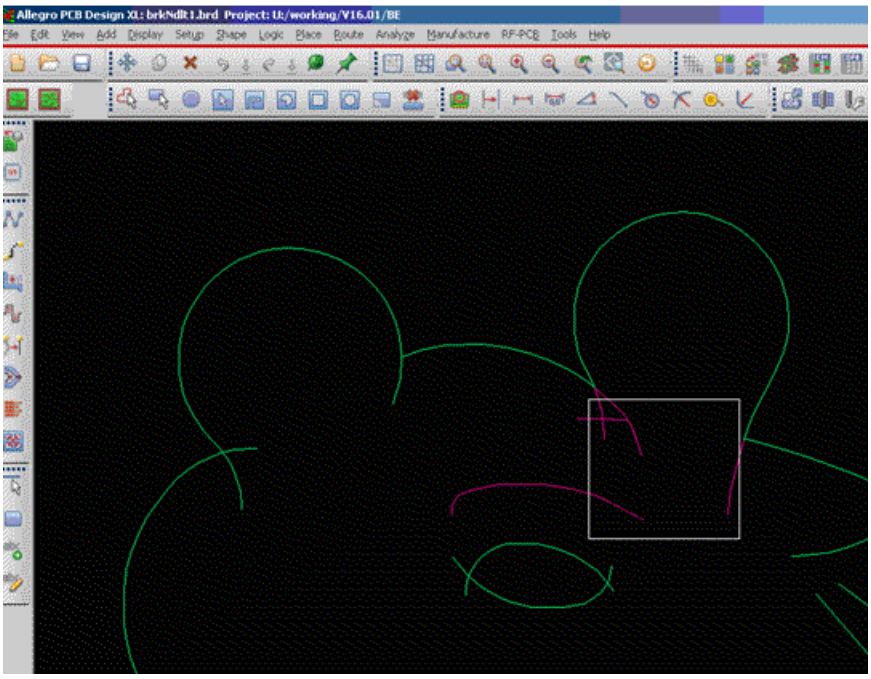
Note: A circle is considered an isolated line.

Figure 8-12 Deleting an isolated line



Shown in Figure 8-13, you can delete a group of lines by drawing a bounding box around the section, letting you break and delete multiple lines at one time.

Figure 8-13 Deleting a group of lines using a bounding box



Once you complete the deletion of all extra lines, you can convert the outline to a filled shape using *Shape – Compose Shape* in Allegro.

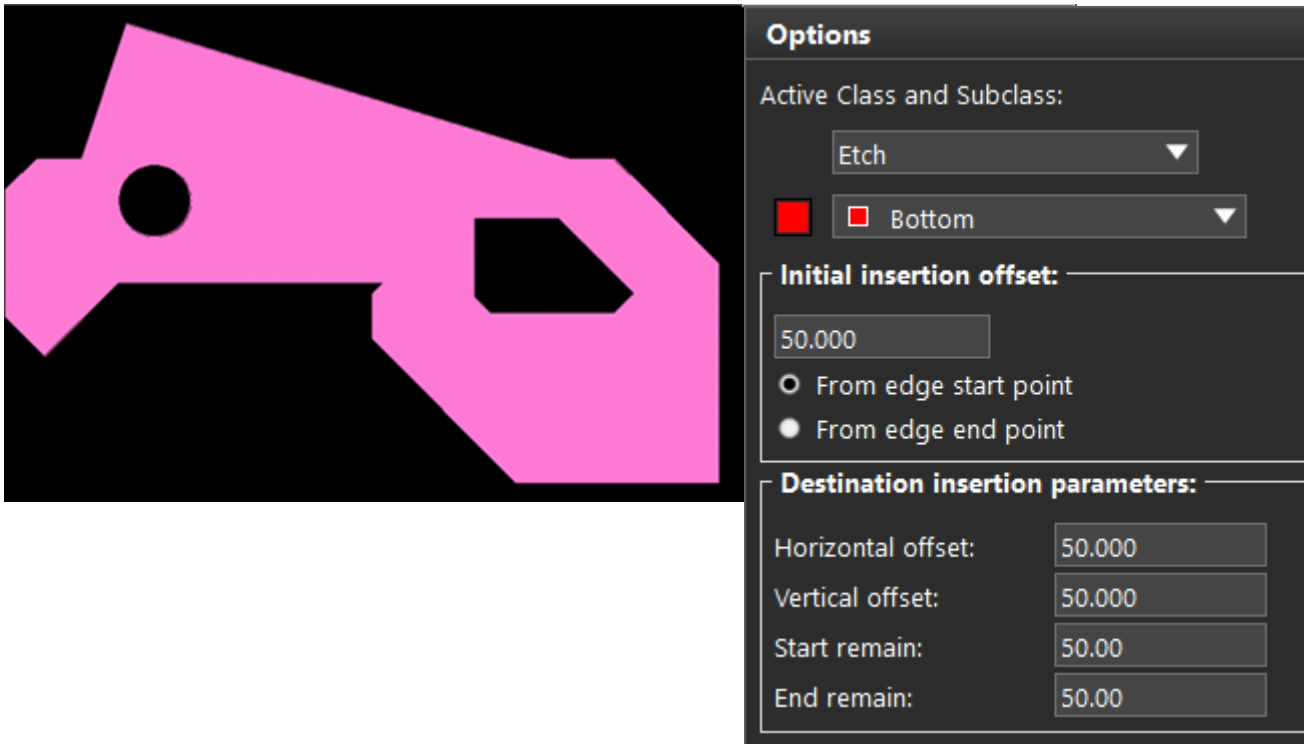
Shape Vertex Editing

Inserting a Vertex

You can insert a new vertex into the edge of a shape to modify its boundary by choosing *RF-PCB – Flexible Shape Editor – Vertex Insert*. Once the initial insertion location and destination offsets are defined, a vertex is inserted and the shape re-configures itself.

Note: Do not insert vertices into circular shapes or voids.

Figure 8-14 Inserting a vertex into an edge



For further details, see to the `fse vertex insert` command in the *Allegro PCB and Package Physical Layout Command Reference*.

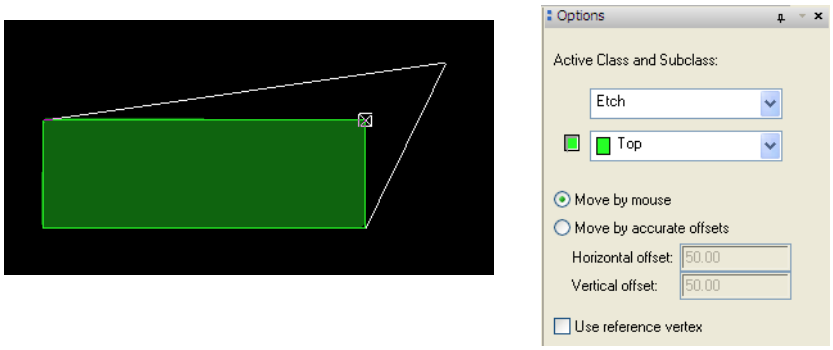
Moving a vertex

You can move a vertex in the shape to modify its boundary by choosing *RF-PCB – Flexible Shape Editor – Vertex Move*. Once destination offsets are defined, a vertex is moved and

the shape re-configures itself. You can specify the destination point of the vertex using the mouse or by entering the Offset values from the original location.

You can also move the vertex relative to a reference vertex either on the same or different Active class and subclass.

Figure 8-15 Moving a vertex



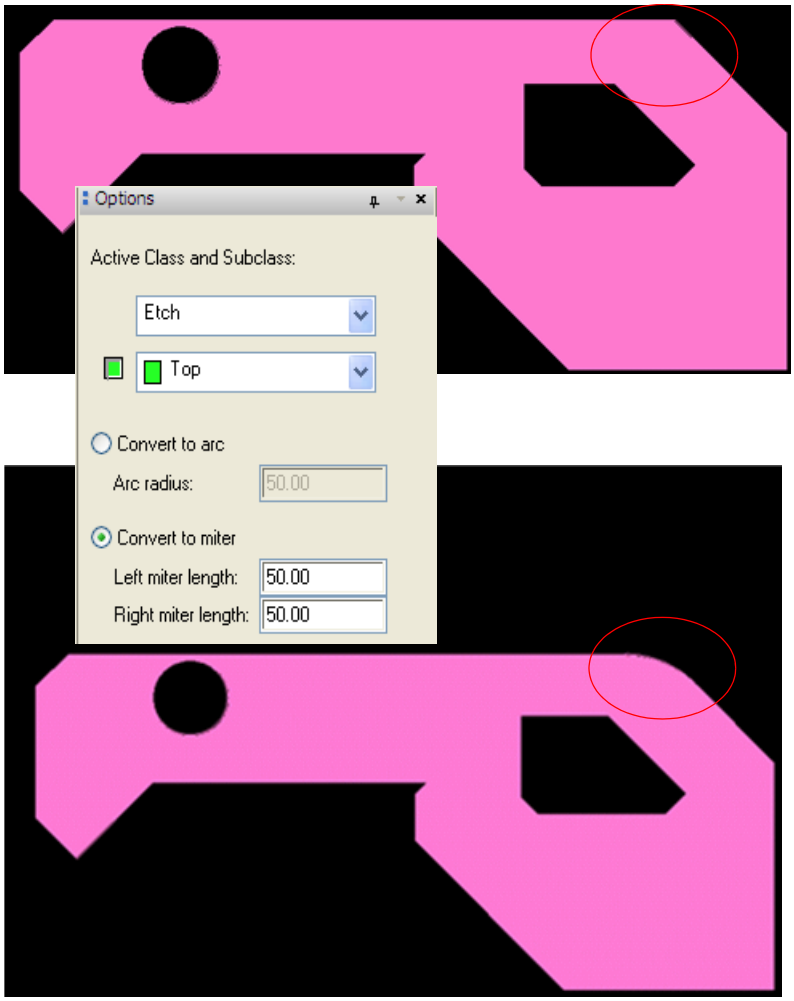
For further details, see to the `fse_vertex_move` command in the *Allegro PCB and Package Physical Layout Command Reference*.

Converting a Vertex

You can convert a vertex to a miter or an arc by choosing *RF-PCB – Flexible Shape Editor – Vertex Convert*. Once the miter lengths or arc radius is specified, you select the vertex and the conversion is applied accordingly.

Note: This command converts one vertex at a time. To convert all the vertices of a shape simultaneously, choose *RF-PCB – Flexible Shape Editor – Shape Corner Chamfer*.

Figure 8-16 Filleting a shape corner



Before

After

For further details, see the `fse vertex convert` command in the *Allegro PCB and Package Physical Layout Command Reference*.

Whole Shape Editing

Whole shape editing enables you to modify multiple features of a shape or group of shapes in a single operation. You choose *RF-PCB – Flexible Shape Editor – Shape Operations*, select a logic operation type from the Options pane, then identify two groups of overlapping shapes to operate on.

Shape Operations

Shape editing uses boolean logic for modifying shapes that have the same net name. These operations require at least two shape groups to be selected after the command is activated. Each shape group can consist of one or more shapes. You define a temporary group of shapes by clicking the right mouse button, choosing *Temp Group*, selecting the shape objects, then clicking the right mouse button and choosing *Complete*. You can also create a bounding box using the left mouse button to select multiple shapes that are in close proximity to each other.

Examples

The three shapes in Figure 8-17 have the same net name and are used in the following examples. In each example, shapes A and B (group 1) are combined with shape C (group 2) to produce a different result.

Figure 8-17 Shape groups

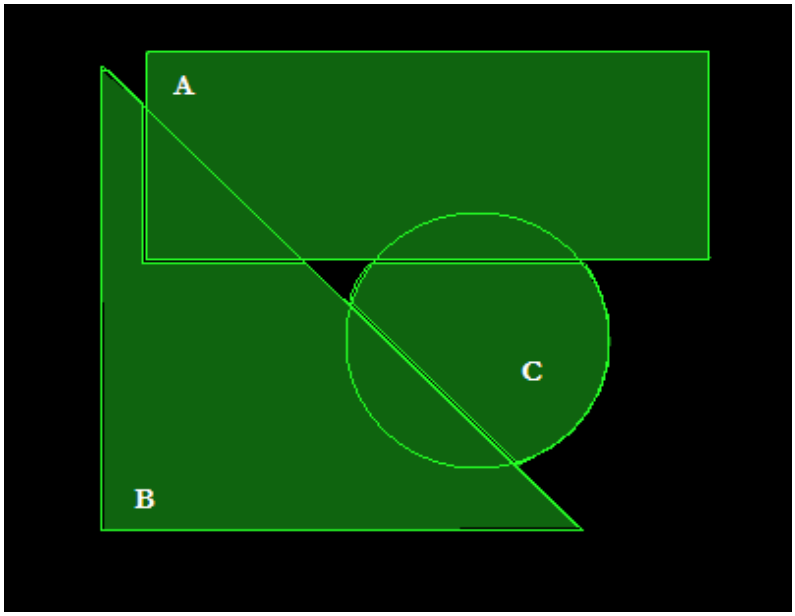


Figure 8-18 Union operation result

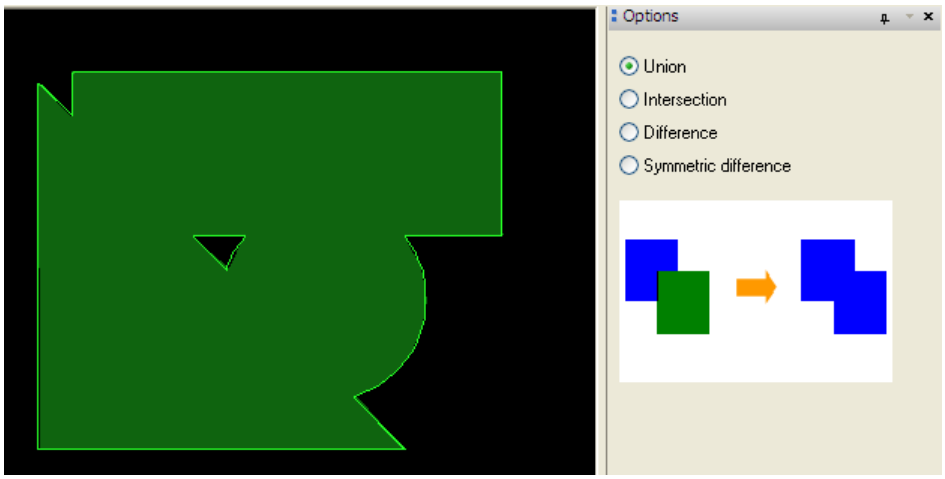


Figure 8-19 Intersection operation result

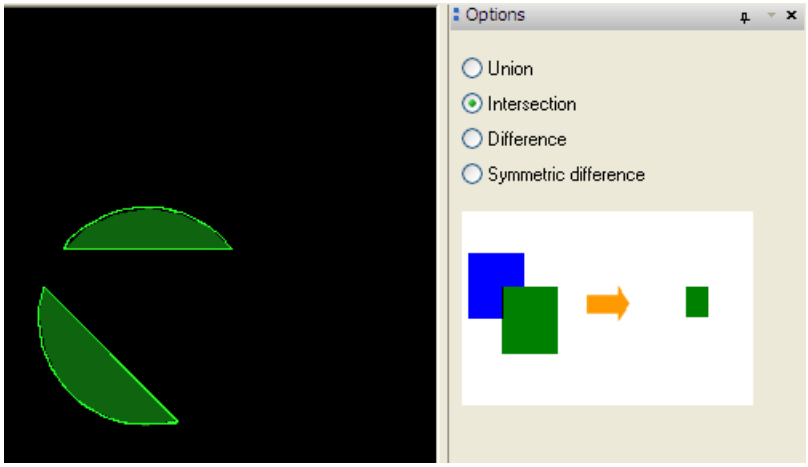


Figure 8-20 Difference operation results

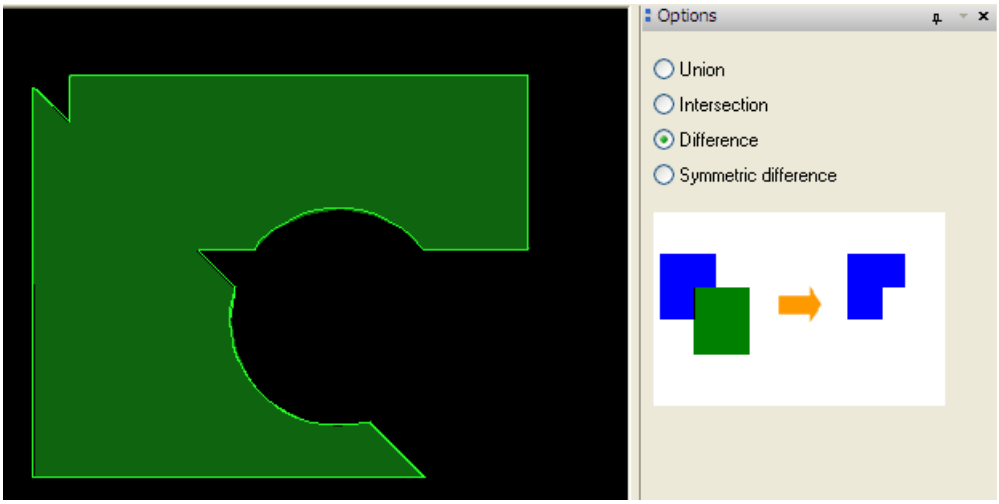
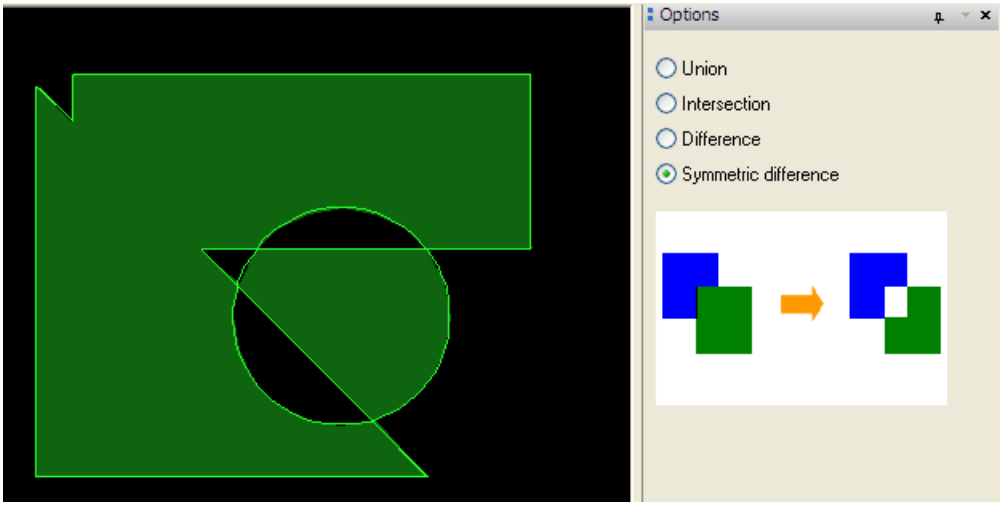


Figure 8-21 Symmetric difference operation results



For further details on how to edit shapes using boolean logic, see to the procedures for `fse shape logicop` command in the *Allegro PCB and Package Physical Layout Command Reference*.

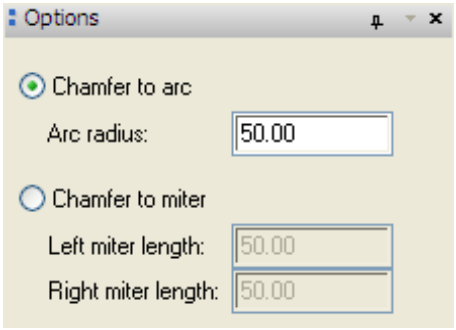
Shape Corners Edit

You can convert all the corners of a shape to miters or fillets by choosing *RF-PCB – Flexible Shape Editor – Shape Corner Chamfer* to access the Options pane shown in Figure 8-22. Once you choose the type of corner to convert to and enter the size, you simply click on a shape to execute the conversion.

Note:

- If you enter a miter or fillet size that is out of range relative to the size of a corner, the conversion is not applied to that corner.
- You cannot convert corners consisting of one or two arcs.

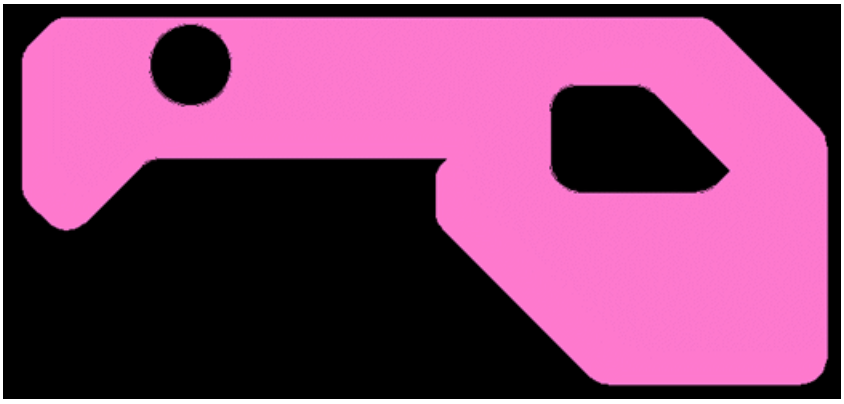
Figure 8-22 Corner Chamfer Options pane



Example

Figure 8-23 Converting all corners to arcs

Before



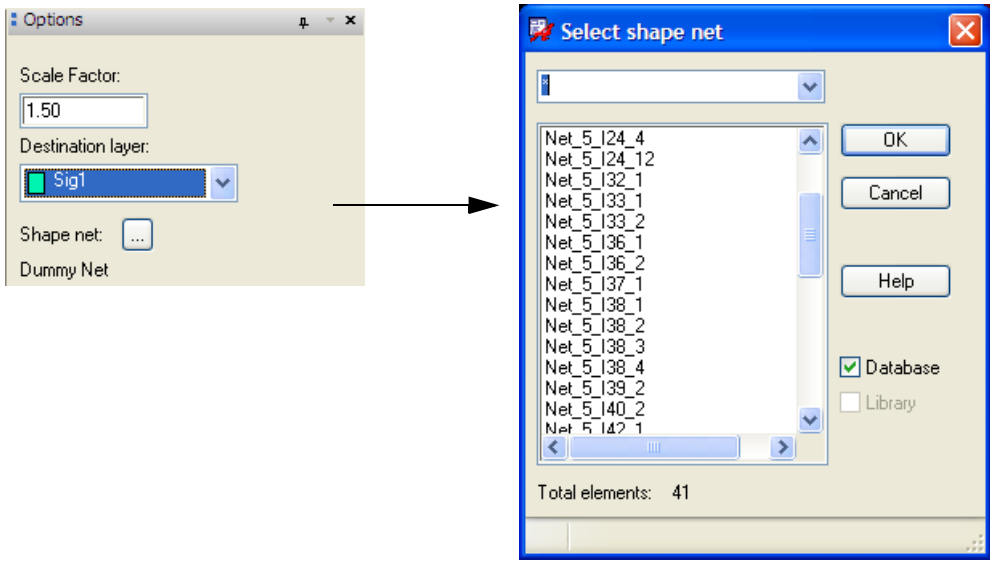
After

Shape Scale / Copy

You can enlarge or reduce the size of a shape using a scale factor by choosing *RF-PCB – Flexible Shape Editor – Shape Scale* to access the Options shown on the left of Figure 8-24. The shape copy can also be sent to a different etch layer in the stackup with the option of

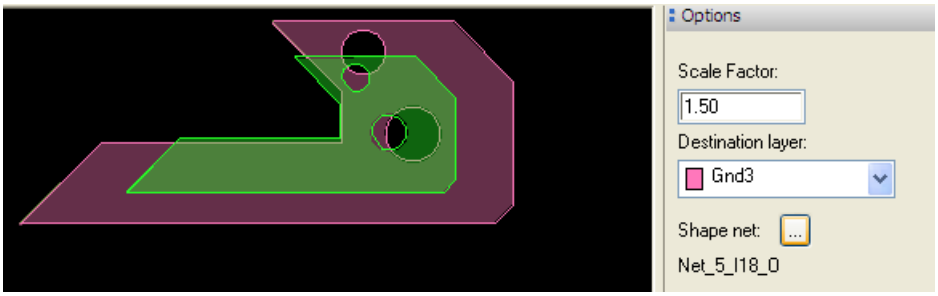
using an alternate net name. For further details on how to scale and copy a shape, see the procedures for `rf_scaled_copy` in the *Allegro PCB and Package Physical Layout Command Reference*.

Figure 8-24 The Shape scale Options pane



Example

Figure 8-25 Creating a scaled copy of a shape



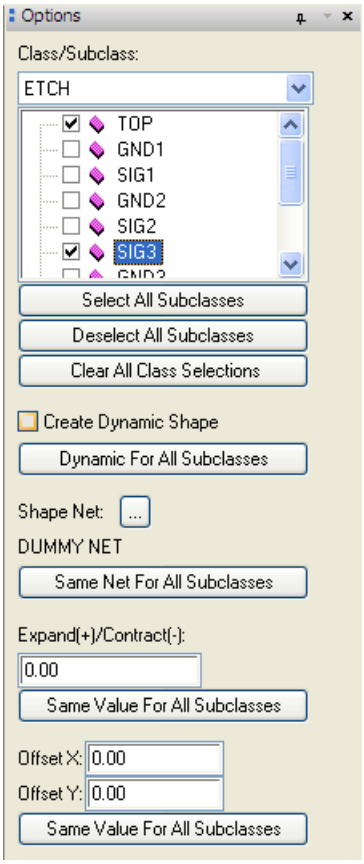
Multi-layer Shape Zcopy

You can copy a shape to several different layers in the stackup simultaneously by choosing *RF-PCB – Flexible Shape Editor – Multi-Layer Shape ZCopy* to access the options shown in Figure 8-26. You can specify net name, scale, and offset for each the copies. For

further details on how to Zcopy a shape to multiple layers, see the procedures for `fse_shape_zcopy` in the *Allegro PCB and Package Physical Layout Command Reference*.

Example

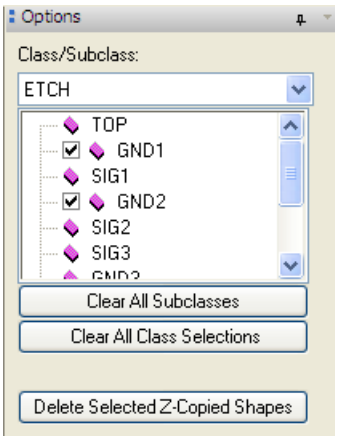
Figure 8-26 Zcopying a Shape to Multiple Layers



Multi-layer Shape ZDelete

You can delete Zcopy shapes by choosing *RF-PCB – Flexible Shape Editor – Multi-layer Shape ZDelete* to access the options shown in Figure 8-27. All layers of the selected class with Zcopied shapes are listed with a checked status.
To keep all the Zcopied shapes on a certain layer, clear the check box for that layer, then click *Delete Selected Z-Copied Shapes* to remove the shapes on the selected layers.

Figure 8-27 The Multi-Layer Shapes ZDelete Options pane



9

Module Reuse

- Saving Components as a Module
- Reusing a Module
  - ECO Workaround

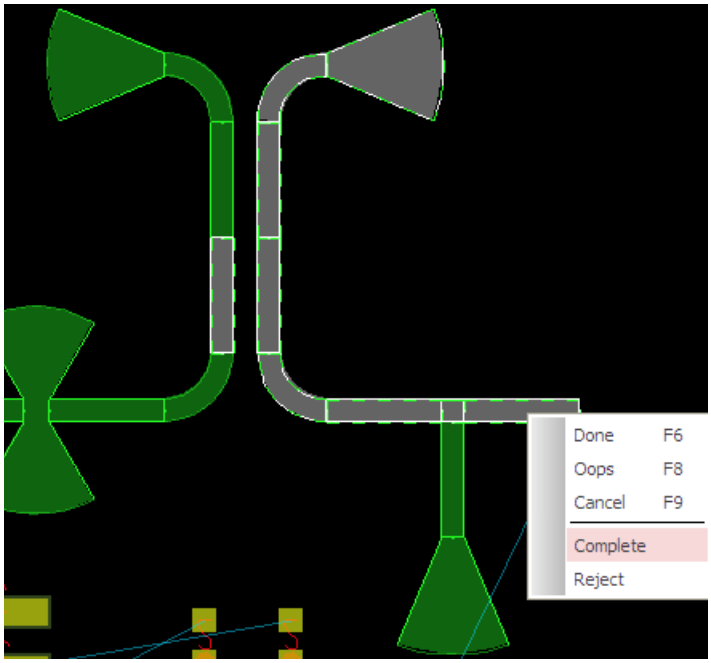
Saving Components as a Module

You can reuse a portion of your RF design by defining a module and saving it as a file. You can save both RF and non-RF components in a module. For details on how to save a module, see to the procedures for the `create_module` command in the *Allegro PCB and Package Physical Layout Command Reference*.

Important

To reuse a module in another design, the stackups must match.

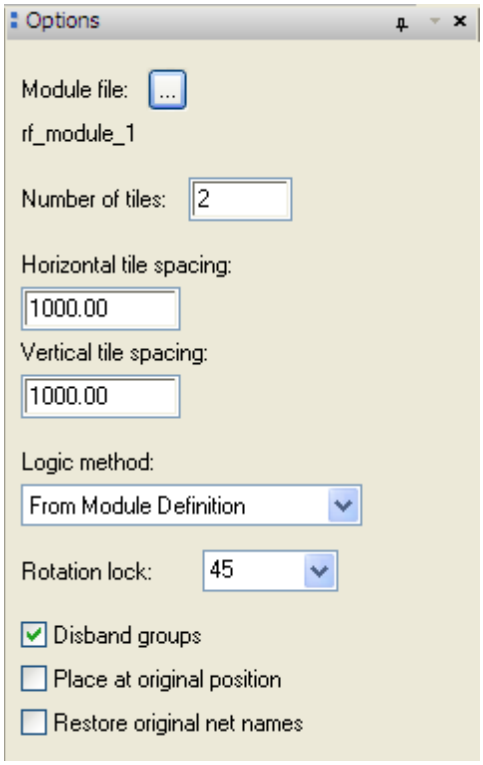
Figure 9-1 Saving part of a design as a module



Reusing a Module

After saving a module, you can reuse it in the same design or in a different design having the same stackup (tech file). Load the module into a design by choosing *RF-PCB – Load Module* to access the options shown in Figure 9-2. Once you select a module (`.mdd`) file to load, specify the number of module iterations as well as other module parameters, you click in your design to fix the location of the module origin. You can then move your cursor about the module to adjust its orientation in the design. To complete the module loading, you click the right mouse button and choose *Done*.

Figure 9-2 Loading a module into a design



If you disable *Disband groups*, then all components of the module are loaded into the design as a group. Otherwise, they are loaded as individual components. If you enable *Restore original net names*, then all nets will keep their original names, otherwise a prefix is added for each net.

For further details on how to load a module, see the procedures for the `rf load module` command in the *Allegro PCB and Package Physical Layout Command Reference*.

ECO Workaround

If you use a third-party tool for your schematic design (for example, the digital portion) and use RF PCB to layout your RF design, you may encounter an ECO problem. You can use module reuse to work around it.

1. Save all your RF traces as a module.
2. Import the logic into Allegro to implement the digital portion ECO.
3. Choose *RF-PCB — Load RF Module* to access the Load RF Module Options pane.
4. Enable *Place at original position* and *Restore original net names*.

5. Load the module back into the design.

   Note: Some elements may overlap when you load the module into the original design.

10

ADS Interface

- Overview
  - Allegro PCB Editor / ADS Flow
- Allegro PCB Editor to ADS (Export IFF)
  - Export IFF Output Files
  - Export IFF Completion Checklist
  - Importing IFF into ADS Layout
- ADS to Allegro PCB Editor (Import IFF)
  - Import IFF Checks
  - Import IFF Completion Checklist
  - Rules for Processing Unit Scale Factor
- **Exporting Allegro Padstack to ADS**

Overview

The ADS interface in RF PCB is based on the industry-standard IFF format originally proposed by Hewlett Packard in 1995. The IFF acronym stands for Intermediate File Format.

This bidirectional interface lets you transfer your physical RF design to Keysight ADS for EM simulation and optimization using Momentum. Once physical modifications are made in the ADS environment, you can back-annotate your changes to Allegro PCB Editor. You can also use this interface to import new designs from ADS to Allegro. The interface supports the following elements for import and export:

- RF components (Microstrip, Stripline, CPW, PCB. etc.)
- Shapes
- Clines and lines
- Vias, pins and pads
- Discrete components

Note: Unsupported RF components transfer to ADS by changing them to shapes or boundary lines. See Figure 10-14 for further details.

Allegro PCB Editor / ADS Flow

Cadence recommends that you adhere to the following flow when using the ADS interface.

1. In Allegro PCB Editor, set up your board stackup.
2. Initialize your RF design using the `rf_setup` command.

   Note: If you have not previously set up for RF PCB, the setup options appear automatically when you run the `rf_iff_export` command.
3. Layout and adjust your RF design.
4. Use Export IFF to translate your RF design and stackup.
5. In ADS, use the *Cadence/PCB* option to import your design into ADS Layout, then use Momentum *Substrate Open* to load it.

   Note: Also load the `.slm` file to import the design stackup (if applicable).
6. Perform EM simulation using Momentum.
7. Analyze the simulation results and modify (optimize) physical parameters accordingly.

8. Use Export IFF or the *Cadence/PCB* option to translate the modified design and Momentum *Substrate Save* to export the stackup.
9. In Allegro PCB Editor, use Import IFF to back-annotate your changes and update your RF design and stackup.
10. Repeat steps 2 through 8 if needed (using same Allegro session).

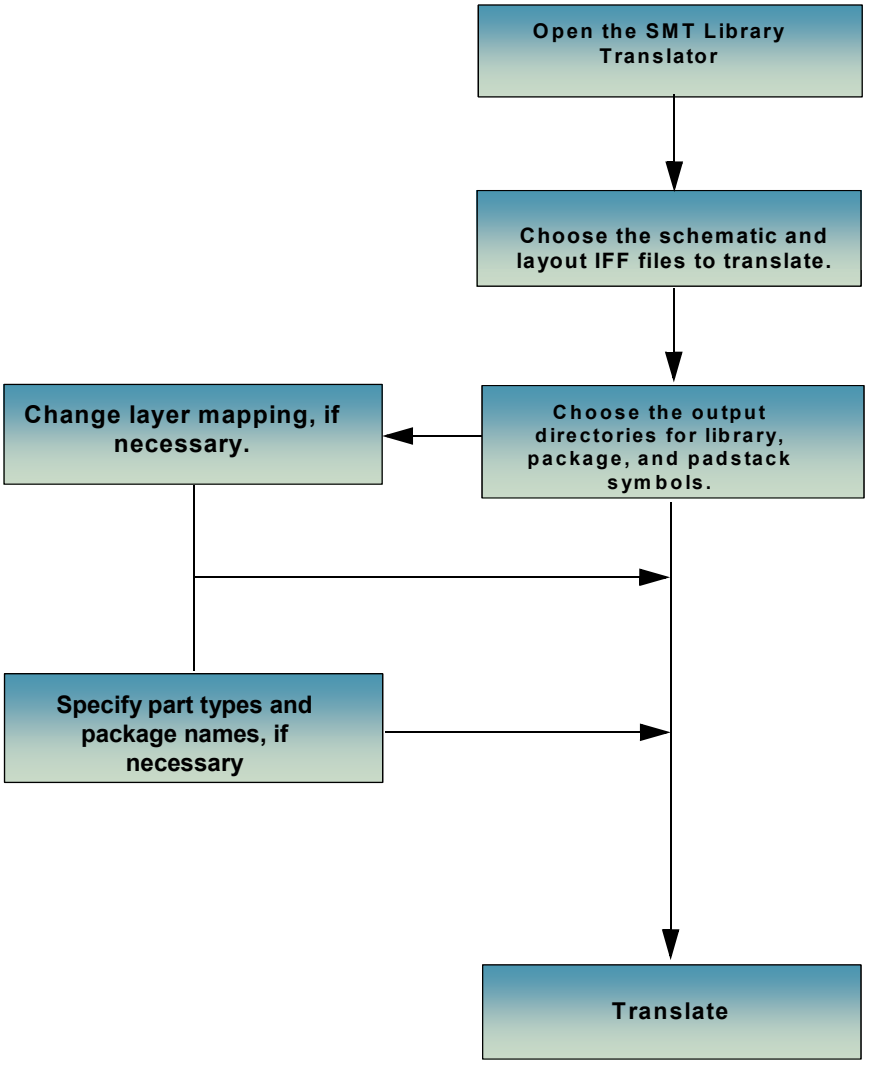
    Note: Repeat *all* steps when running a subsequent session of Allegro PCB Editor.

SMT Library Translator

Transferring a logic design from ADS to Design Entry HDL or Allegro PCB Editor, requires the translation of all packaged parts. Since these packaged parts are pre-defined, you can translate them before transferring the design and save them to a local library for ease of use. When you transfer the design, Design Entry HDL or Allegro PCB Editor retrieves the information on the packaged parts from the local library.

The following diagram (Figure 10-1) illustrates the flow for translating an SMT library.

Figure 10-1 SMT Library Translation Flow

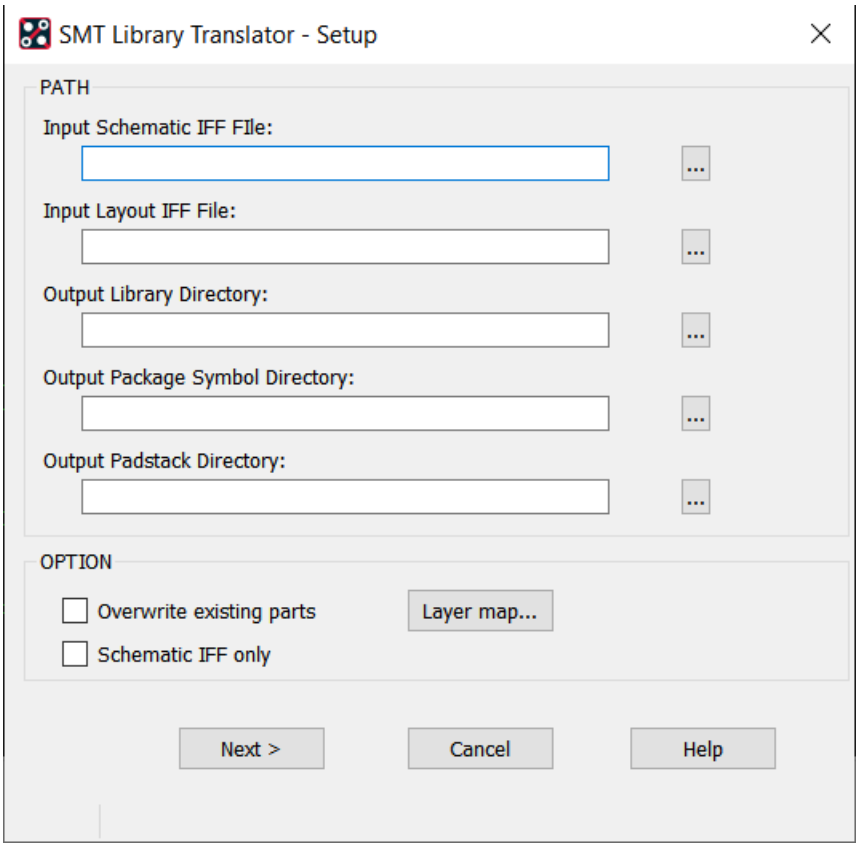


Note: Allegro PCB Editor checks the validity of the part types and package symbols before translating. You can view the results in the SMT Library Translator report.

The SMT Translator provides a series of dialog boxes that let you specify the directory in which you want to save the translated parts, change part types, and change package names. In the Setup dialog box (Figure 10-2), you enter names of the files to import and designate directories in which to store the translated packaged parts. If you choose to *Overwrite existing parts*, the translator overwrites parts in the specified path during the import process and turns off the messages as seen in (Figure 10-7 and Figure 10-6). If you choose *Schematic IFF only*, you cannot enter or browse to a filename in the *Input Layout IFF File* field, and you must specify all footprint symbols in mapping mode.

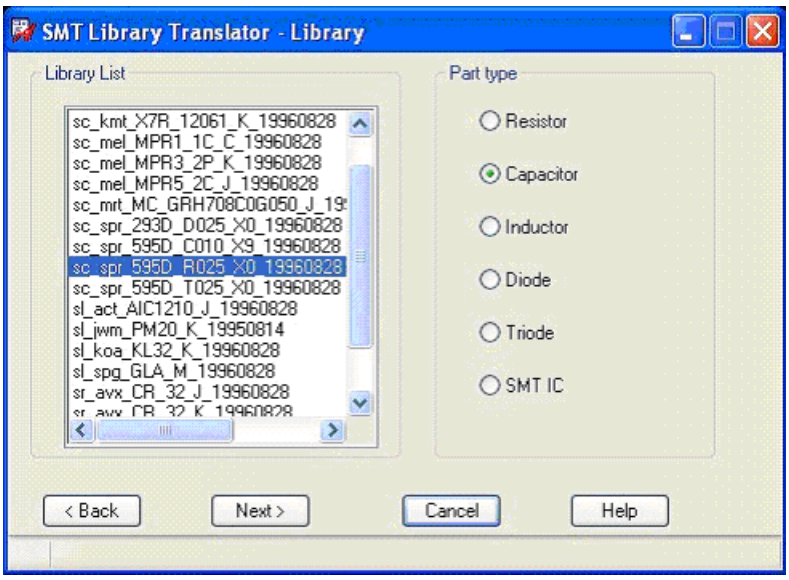
Select *RF-PCB — IFF Interface — SMT Library Translator.* The SMT Library Translator opens.

Figure 10-2 SMT Library Translator – Setup



When you complete setup, the SMT Library Translator - Library dialog box appears (Figure 10-3).

Figure 10-3 SMT Library Translator – Library



The list of libraries originates in the IFF files you are importing. When you choose a component in the component list, the default part type displays. The tool checks the validity of the part type immediately after you change it. For example, if you change the part type of a component with 2 pins from a capacitor to an SMT_IC, a warning message appears as in Figure 10-4.

Figure 10-4 Warning Message

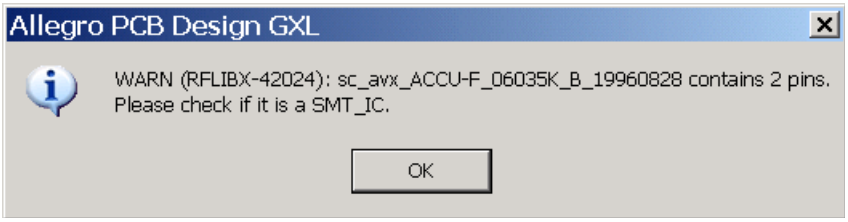
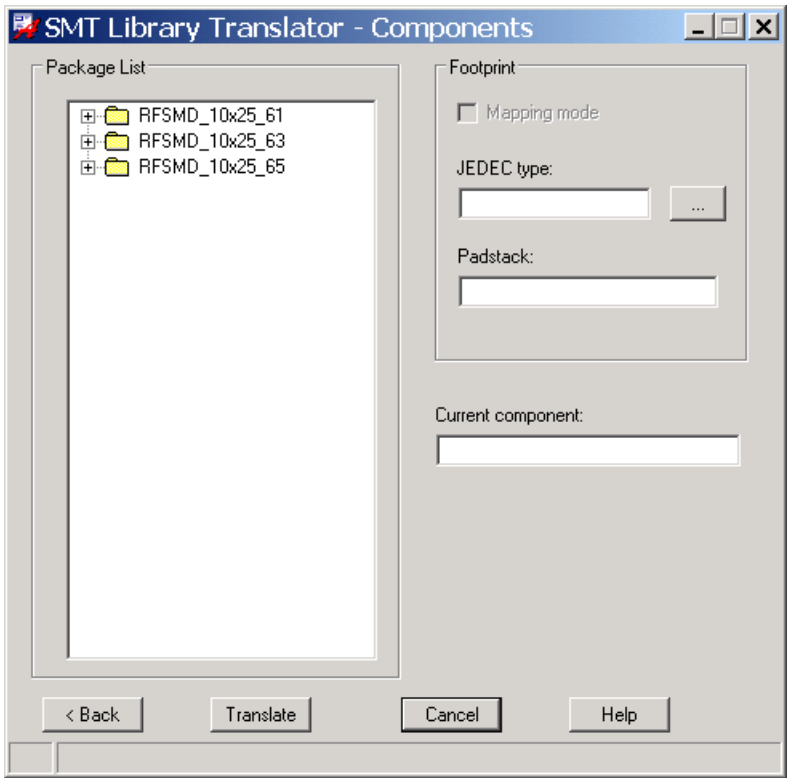


Figure 10-5 SMT Library Translator – Components Dialog Box

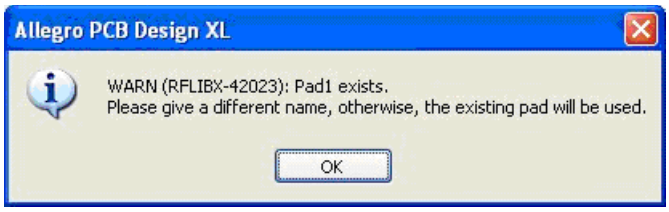


The SMT Library Translator – Components dialog box (Figure 10-5) displays package symbols extracted from the imported IFF file, classified by their package. You can change the package name in the JEDEC *type* field. When you choose a component from the list, the *Package Symbol* field updates and you can edit the package symbol of the component. When you choose a package, the *Package Symbol* field updates and you can edit the package symbol of a group of components.

There are two modes for package symbol generation. When *Mapping mode* is not checked, you cannot edit the JEDEC *type* field, and the tool generates the package symbol according to the specified IFF files.

In *Mapping mode*, you can specify the package symbol within the local file. The *Padstack* field displays the name of the pad used in the component. You can edit this field after you choose a package node. A warning message prompts you to give a different name when the same pad exists in the specified path in the *Output Padstack Directory* field (Figure 10-6). Otherwise, the tool uses the existing padstack.

Figure 10-6 Duplicate Padstack Warning

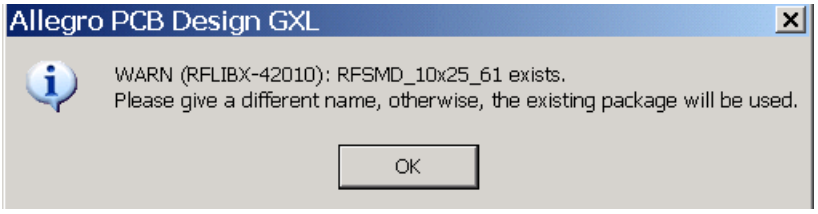


Note: When *Schematic IFF only* is checked, *Mapping mode* is automatically checked and not editable.

The default JEDEC type footprint information comes from the layout IFF file and has a prefix `RFSMD`. When the component includes the DEVICE property, the tool uses it as the default JEDEC type. You can change it using this dialog box. After the change, the icon before the component changes to a diamond shape.

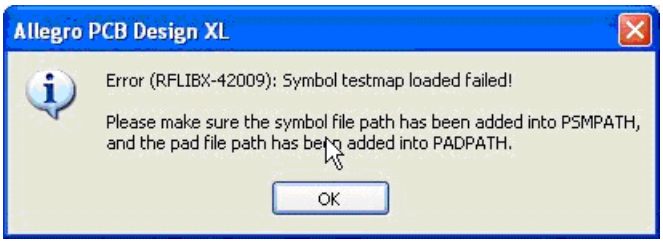
If the JEDEC type already exists in the specified path, a warning message appears (Figure 10-7) reminding you to give it a different name. Otherwise, the component uses the existing package.

Figure 10-7 JEDEC Type Warning



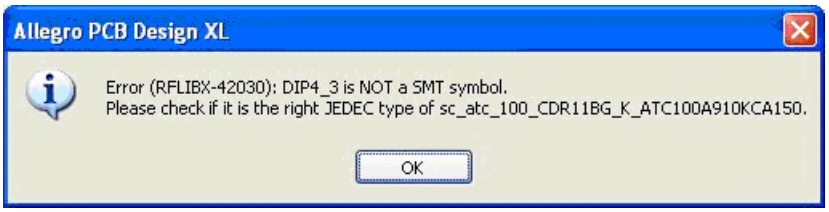
You can map the footprint to an existing one in another path. Browse to a `.psm` file and the tool copies both the `.dra` file with the same name and the `.psm` file to the *Output Package Symbol Directory*. After mapping, the icon before the component changes. Then the tool checks the validity of the `.psm` file. If an error exists, a warning message appears (Figure 10-8).

Figure 10-8 Validity Check Warning



When you specify the package symbol of a capacitor as `DIP4_3`, a warning message also appears.

Figure 10-9 Package Symbol Validity Warning



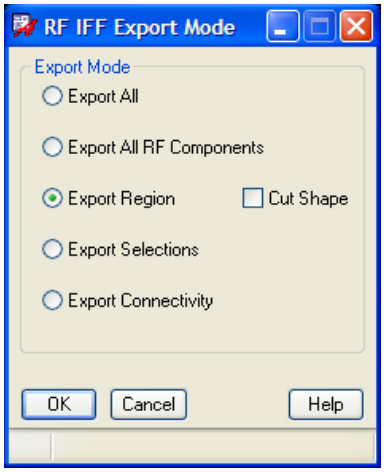
Once you start the translation process, a progress bar appears tracking the translation status. When finished, a pop-up appears giving you the option to view the translation report. If you click Yes, a log file opens containing the following information:

- File header that contains the board name, software version, and generation date of the log file.
- Directory name where the exported library, package symbols, and the padstack directories exist.
- Layer mapping.
- Translation log that includes the translated components and those that did not translate.

Allegro PCB Editor to ADS (Export IFF)

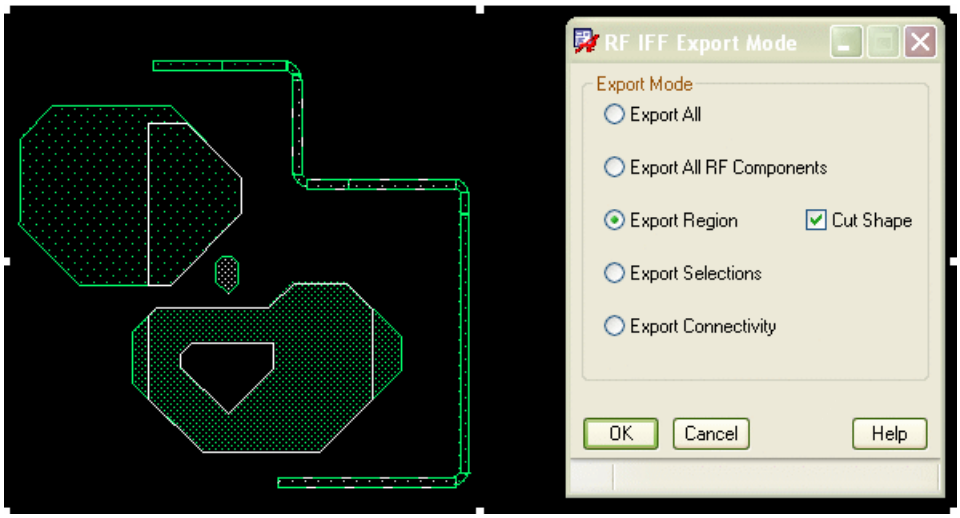
You export your RF design to ADS by choosing *RF-PCB – IFF Interface – Export.* The dialog box shown in Figure 10-10 appears allowing you to select all or a portion of the design to export. For a description of the export modes, see the `rf_iff_export` command in the *Allegro PCB and Package Physical Layout Command Reference*.

Figure 10-10 RF IFF Export Mode Dialog Box



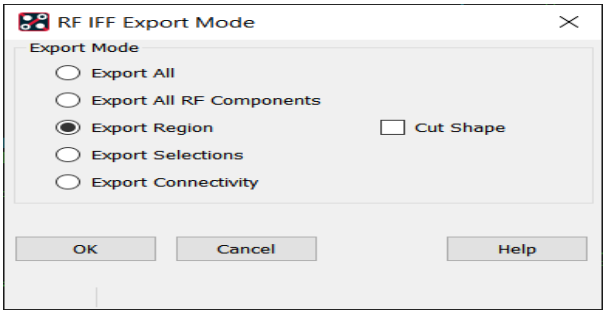
When exporting a region of your design, you can also export a part of a shape that falls within the bounding box of the selected region. This option is useful when you require only a portion of a shape to simulate an RF circuit. If you export a shape that is not completely inside the selected region, a dynamic path displays showing you which part of the shape will export (Figure 10-11).

Figure 10-11 Exporting a Partial Shape



As shown in Figure 10-12, you can export the current stackup information as a `.slm` file and import it into ADS to perform EM simulation. If you don't export the stackup information, you will need to specify the substrate layer mapping manually on the ADS side.

Figure 10-12 RF IFF Export Dialog Box

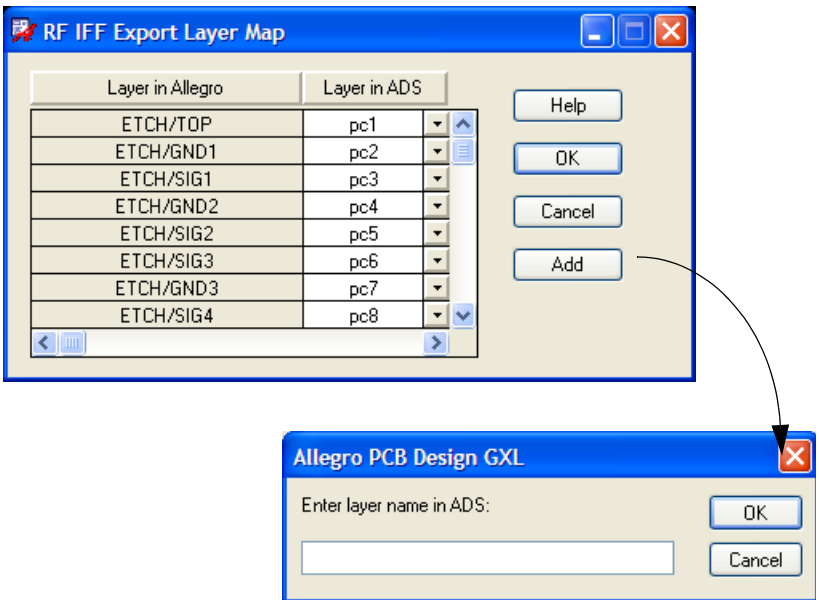


Check *Discrete component name mapping* check box to specify if you want to rename the discrete components after export, to make them consistent with the Allegro Discrete Library Translator. This option is enabled only if discrete components are selected for export.

Note: If the property PART_NUMBER does not exist for the for a discrete component, the discrete component is not renamed.

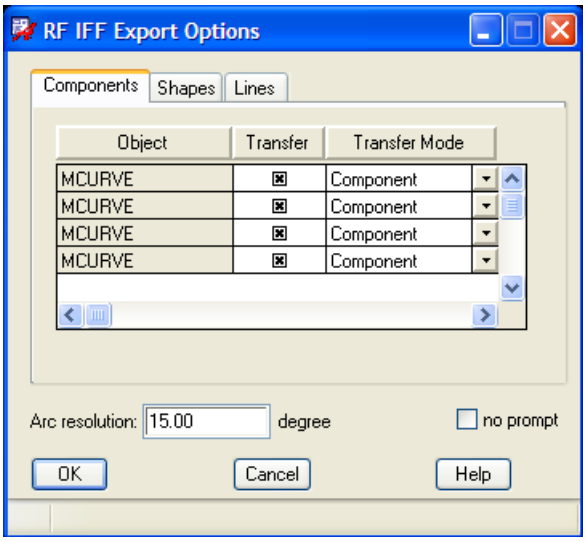
After you select the elements to export, you need to perform layer mapping between Allegro PCB Editor and ADS. By default, every layer in Allegro PCB Editor maps to a layer in ADS automatically. You can change the map layer in ADS and add new layers by clicking the *Add* button shown in Figure 10-13.

Figure 10-13 RF IFF Layer Map Dialog Box



You can transfer unsupported RF elements by clicking the *More options* button shown in Figure 10-12. This displays the dialog box shown in Figure 10-14.

Figure 10-14 RF IFF Export Options Dialog Box



For example, you can transfer unsupported RF components by choosing the *Components* tab, selecting the unsupported objects for transfer, and then specifying a transfer mode for each. When you invoke an IFF export that includes non-supported elements, a warning

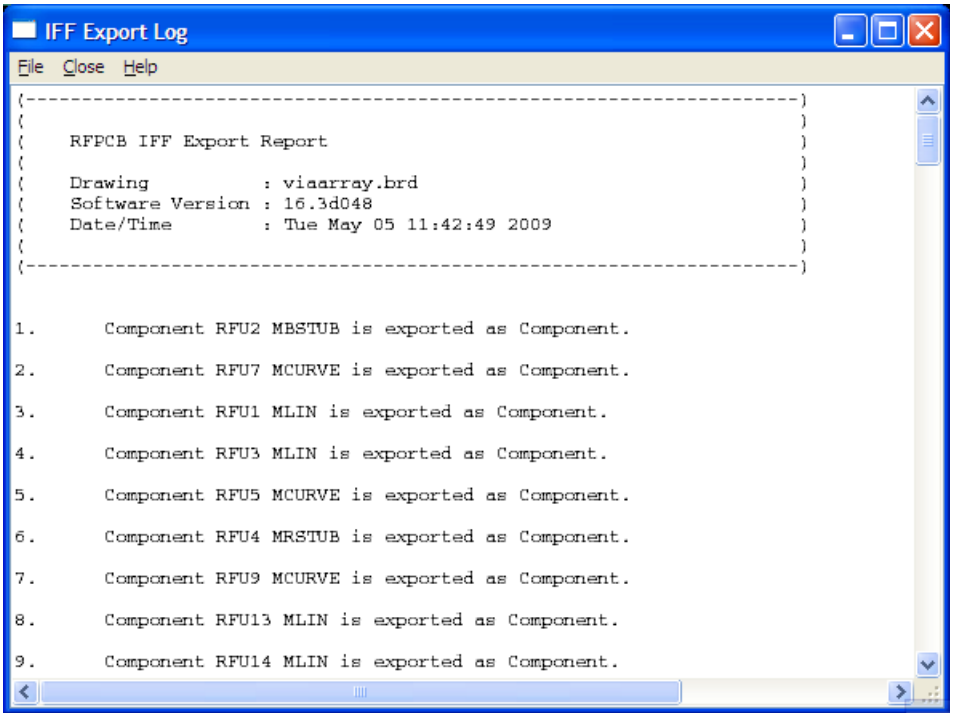
message appears. Upon confirmation, the elements are changed to the new element types specified in the *Transfer Mode* column, and are then exported to ADS.

Unlike unsupported components, a cline or a line segment is exported as a polyline to ADS if its width is constant. If its width is variable, then it is exported as a shape. There is another exception for a constant width line segment. If it contains an arc, this line or cline is exported as a series of smaller segments. However, their element types remain unchanged in the Allegro PCB Editor design database.

Tip

To suppress the warning message when transferring unsupported elements, check *no prompt* in the dialog box shown in Figure 10-14. When this option is enabled, no confirmation is required and unsupported elements transfer directly using the selected transfer mode.

Figure 10-15 Sample IFF Export Log



Export IFF Output Files

RF PCB exports both a `layout.iff` and a `schematic.iff` file in the specified directory. For RF designs with RF components, the `schematic.iff` is necessary when you perform

simulation on the ADS side. However, for RF designs without RF components, use the `layout.iff` file only for simulation in ADS.

Export IFF Completion Checklist

Once you finish the ADS export, you should do the following:

- Check the export report log file to find out which elements were transferred, their transfer mode, and so on.
- If you plan to import IFF later using the update mode in Allegro PCB Editor, save your current design.
- Plan to conduct RF Setup again in Allegro PCB Editor before you import IFF via update mode next time you open the design.

Importing IFF into ADS Layout

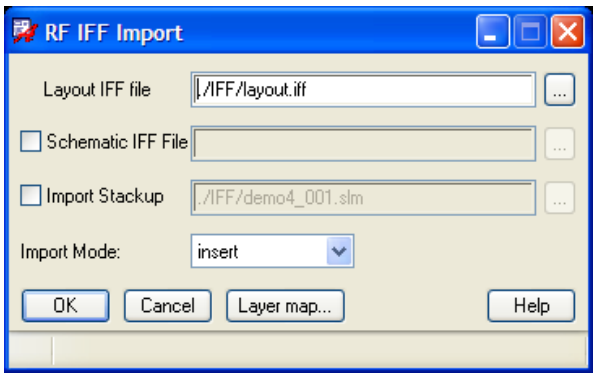
Following are some recommendations for importing IFF files on the ADS side.

- If there are RF components included in the IFF file (especially stripline or CPW components), you need to use the Cadence PCB option to import them into ADS. You can perform the import within the ADS main or ADS Layout environment.
- After you complete the import, all other windows are closed and the schematic window is open. You can then generate the layout from the schematic to perform EM simulation in ADS Layout.
- If no RF components are included in the IFF file, you can use the above method or use the standard IFF option and just select the layout IFF file.

ADS to Allegro PCB Editor (Import IFF)

Once RF simulation and parameter optimization in ADS is complete, you can use Export IFF on the ADS side to translate the modified design and stackup. You can then import the design and stackup into Allegro PCB Editor by choosing *RF-PCB – IFF Interface – Import* to access the dialog box in Figure 10-16.

Figure 10-16 RF IFF Import Dialog Box



In the IFF file fields, you specify the path of the ADS layout and schematic IFF files to import (both are necessary to synchronize your design). If you choose to import the IFF files in *new design* mode, and a `.slm` file is input as the desired stackup for the new design, the tool generates a new design using the stackup information specified in the `.slm` file before importing the IFF files. However, you can switch to the *Copy current stackup* option to use the current stackup information for the new design.

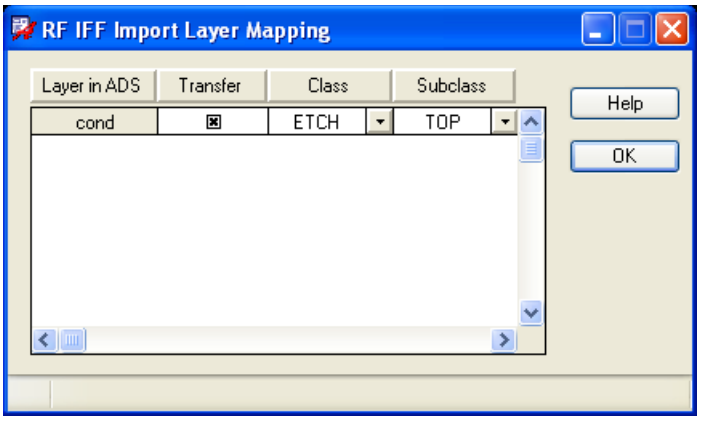
You can also import the stackup information from a `.slm` file that you save from within ADS. When you do this, the stackup in Allegro PCB Editor updates with the stackup information from ADS when you import the IFF layout.

Important

When *Import Stackup* is enabled, the ADS and Allegro PCB Editor stackups are compared and must match each other. Otherwise, the IFF import aborts. Be certain to specify the correct `.slm` file.

If you choose not to import the stackup, you can assign ADS layers to map to Allegro PCB Editor layers by clicking *Layer map* which displays the dialog box shown in Figure 10-17.

Figure 10-17 RF IFF Layer Map Dialog Box



Important

Some lines or clines may not have been exported using the default state (for example, when a cline or line with non-zero width is exported as shape). If you attempt to import them using *update* mode, you are asked to confirm the replacement of the original elements with the new elements. Therefore, only use *update* mode to import elements from the same design. Otherwise, you may end up with elements that are superimposed (overlapping) in your design.

For a description of the import modes shown in Figure 10-16, see the `rf iff import` command in the *Allegro PCB and Package Physical Layout Command Reference*.

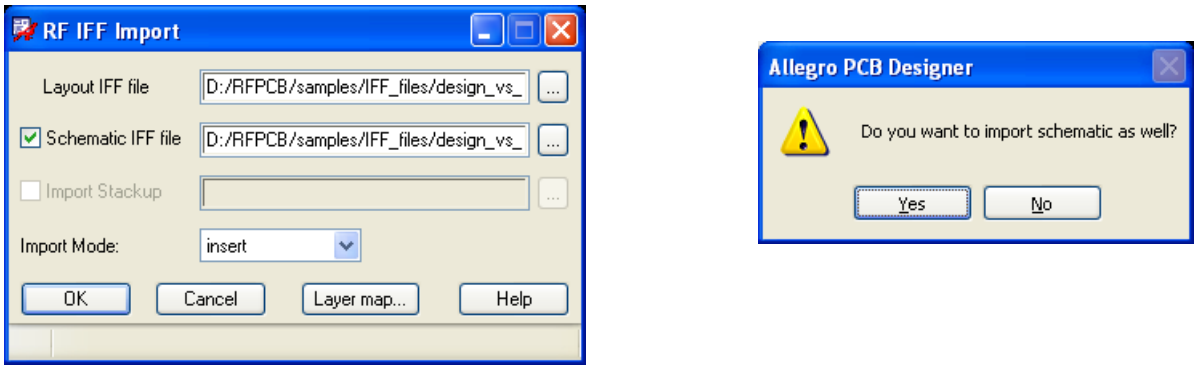
IFF Schematic File Import Model

Sometimes information exists in your IFF files from ADS that requires you to import the IFF layout and schematic files together.

If the IFF file contains variables and expressions, you need to import the layout IFF file together with a schematic IFF file containing the variables and expressions.

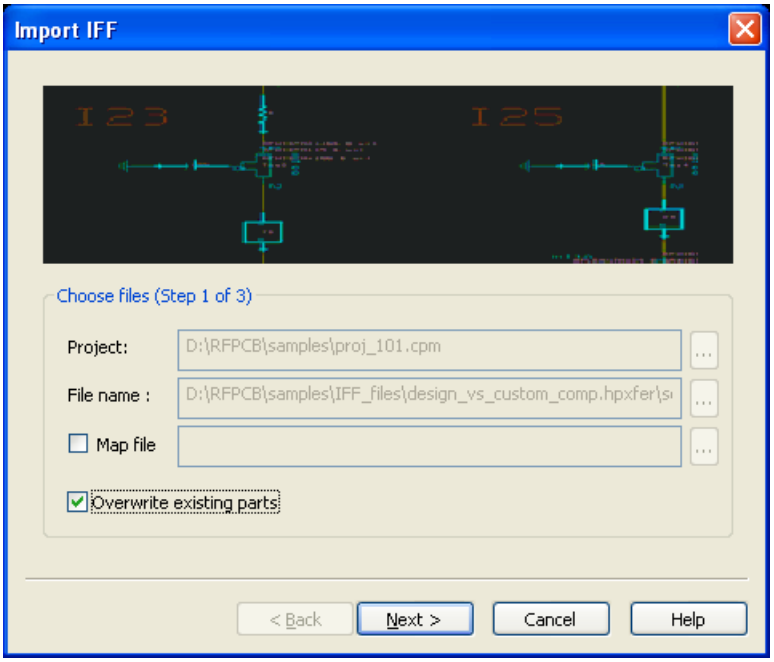
After importing the layout design, a prompt window appears asking you to import the schematic IFF file as well (Figure 10-18).

Figure 10-18 RF-PCB IFF Import Dialog Box



When you choose *Yes* to import the schematic design as well, the tool launches a series of dialog boxes to help you import the schematic file (Figure 10-19).

Figure 10-19 RF-PCB Schematic IFF Import Dialog Box



The layer mapping relationship in the IFF file resides in the project directory, and the tool uses this information to import components and their associated substrates. If non-parameterized components exist in the design, the tool performs symbol mapping (see Figure 10-20) and stores the information in a local library. You can specify footprints for these symbols to replace those defined in the layout IFF file.

Figure 10-20 RF-PCB Schematic IFF Import Dialog Box - Screen 2

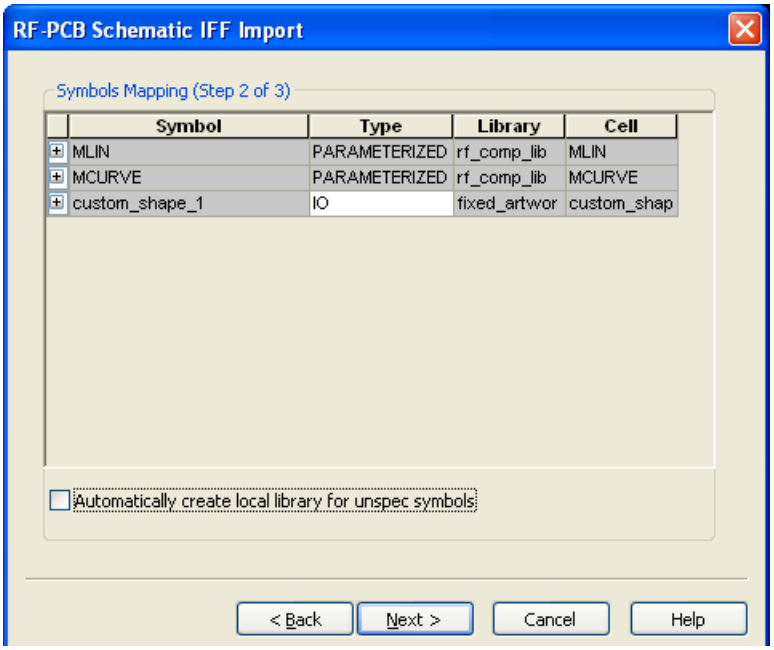
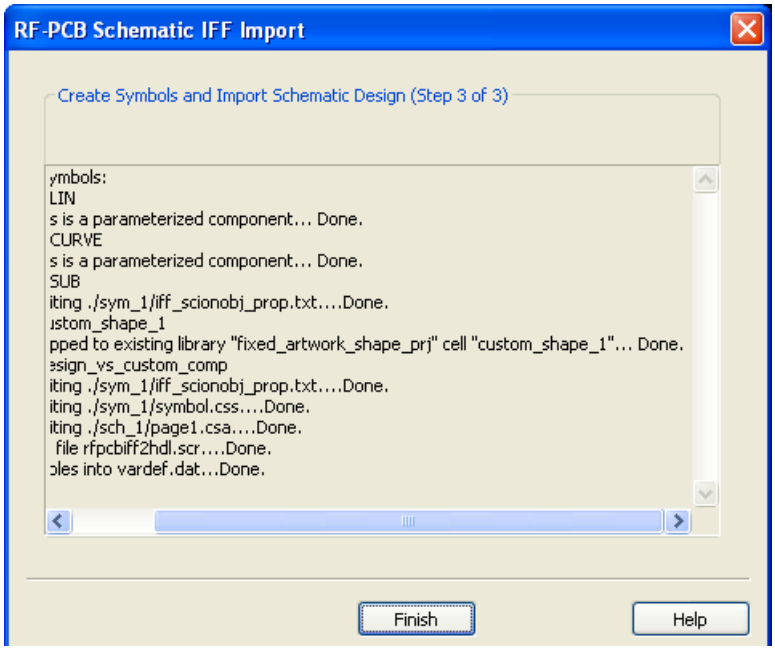


Figure 10-21 RF-PCB Schematic IFF Import Dialog Box - Screen 3



Once the schematic file import is complete, click *Finish* and Design Entry HDL launches (if you have not opened it already), and then Allegro PCB Editor imports the layout file.

Schematic and layout synchronization

As part of the import procedure, RF PCB ensures that the schematic and layout files are synchronized by ensuring that the reference designators are assigned for each component imported into the schematic and layout files.

Hierarchical component import

The RF PCB IFF import procedure interprets elements within a hierarchical layout component in ADS, and generates the corresponding Allegro layout elements.

If the hierarchical components contain other components, the IFF import procedure puts these individual elements into a group with the same name as the hierarchical component from ADS. The group is then assigned the “RFADSHIER” property. In the schematic the hierarchical ADS component is created as a block with a sub-circuit.

However, if the hierarchical component does not contain any other components, except components such as shapes and lines, the import procedure creates a footprint with the same name as the hierarchical component from ADS. If a footprint with the same name already exists, you can choose to overwrite the existing footprint. The footprint is then assigned the, JEDEC_TYPE property. Also, the import procedure will generate a schematic symbol identical to the corresponding symbol in ADS.

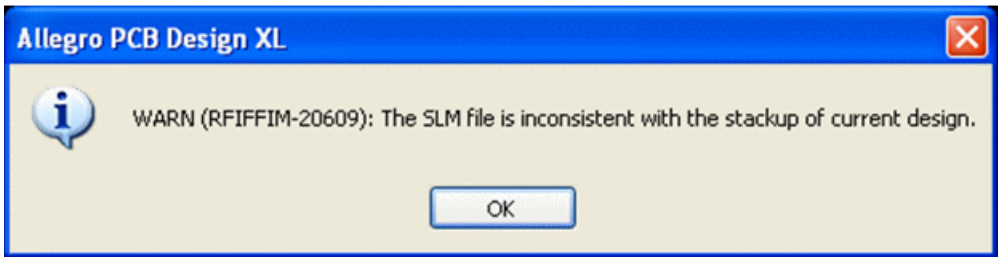
Import IFF Checks

RF PCB conducts several checks on the incoming IFF import file before accepting the data into the current design. If inconsistencies are detected, the import procedure aborts. This gives you an opportunity to make adjustments and retry the import process.

Stackup

If the stackup information described in the incoming `.slm` file is inconsistent with the stackup used in the current design, the warning message shown in Figure 10-22 appears.

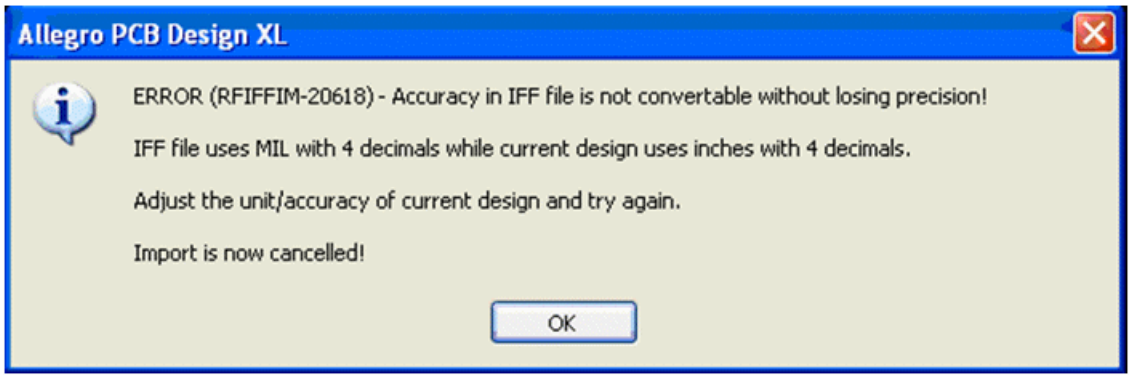
Figure 10-22 Import Stackup Inconsistency Warning



Precision

The unit and accuracy used of the incoming IFF import file is checked. If they are not consistent with those used in the current design, the warning message shown in Figure 10-23 appears.

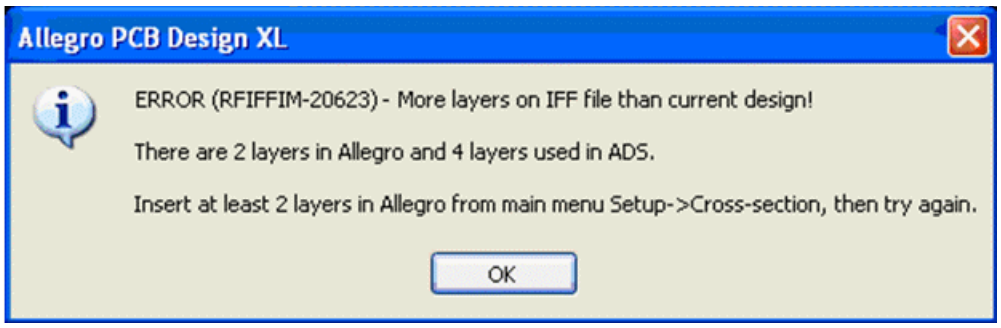
Figure 10-23 Import Precision Warning



Layers

The number of layers defined in the IFF import file is checked. If that number does not match the number of layers used in the current design, it is impossible to have a one-to-one mapping and the warning message shown in Figure 10-24 appears.

Figure 10-24 Import Layer Mismatch Warning

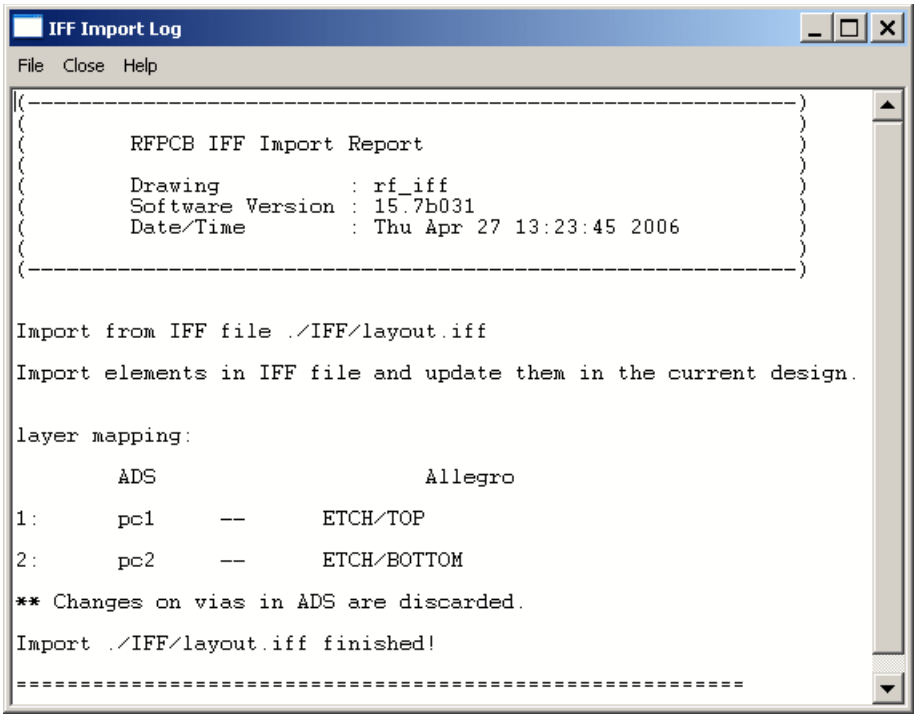


Import IFF Completion Checklist

Once you finish the IFF Import procedure, you should do the following:

- Check the import report log to find out which elements were transferred, their import mode, and so on.

Figure 10-25 Sample RF IFF Import Log



Rules for Processing Unit Scale Factor

IFF files includes unit scale factors that are defined in ADS. The units scale factors are used in property value expressions or in variable definition expressions. The ADS follows a set of rules in using unit scale factors. Import IFF command recognizes and parses the unit scale factors as per these rules.

Rule 1:

If the scale factor exactly matches one of the predefined scale factor words, use the numerical equivalent. The numerical equivalent is defined in the following table:

Scale Factor Words	Meaning	Numerical Equivalent
mil	mils	2.54e-5
mils	mils	2.54e-5
in	inches	2.54e-2
ft	feet	12*2.54e-2
mi	miles	5280*12*2.54e-2
cm	centimeter	1.0e-2
PHz	petaHertz	1.0e15
db	decibles	1.0
nmi	nautical miles	1852

Rule 2:

If the scale factor exactly matches one of the scale factor units except for m, use the numerical equivalent as defined in the following table:

Scale Factor Words	Meaning	Numerical Equivalent
A	Amperes	1.0
F	Farads	1.0
H	Heneris	1.0

Scale Factor Words	Meaning	Numerical Equivalent
Hz	Hertz	1.0
meter/meters/metre/ metres	meters	1.0
ohm/Ohms	Ohms	1.0
S	Siemens	1.0
sec	seconds	1.0
V	Volts	1.0
W	Watts	1.0

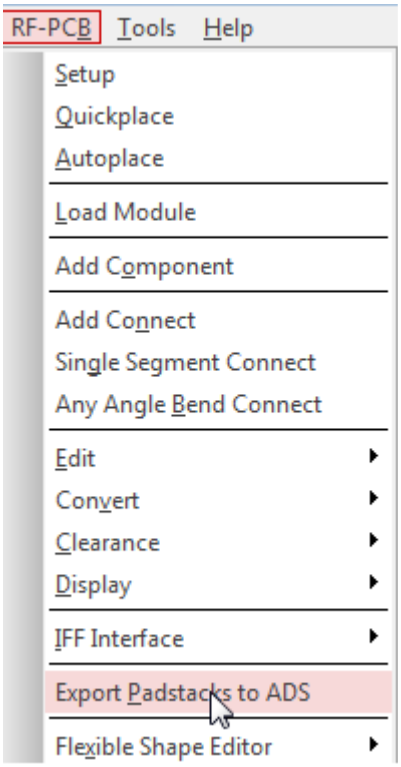
Rule 3:

If the first character of the scale factor is one of the legal scale factor prefixes, use the numerical equivalent as defined in the following table:

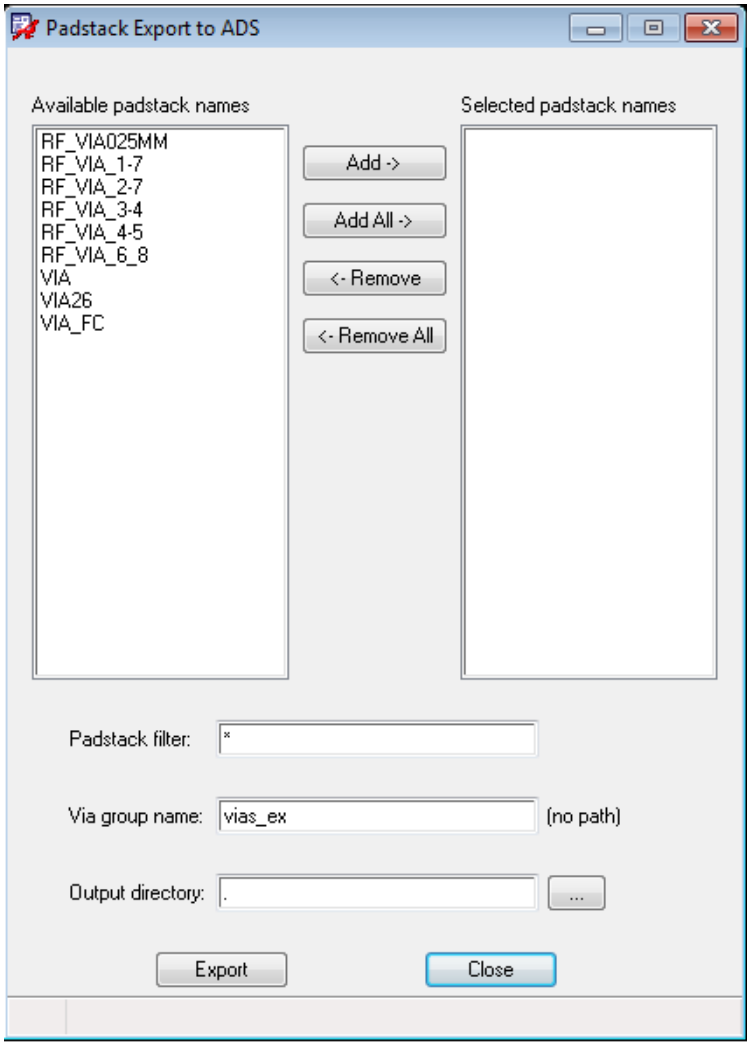
Scale Factor Words	Meaning	Numerical Equivalent
T	tera	1.0e12
G	giga	1.0e9
M	mega	1.0e6
K/k	kilo	1.0e3
_	(no scale)	1.0
m	milli	1.0e-3
u	micro	1.0e-6
n	nano	1.0e-9
p	pico	1.0e-12
f	femto	1.0e-15
a	atto	1.0e-18

Exporting Allegro Padstack to ADS

You can transfer the padstack definitions from Allegro to ADS using *Export Padstacks to ADS* option.



The available padstacks in the current design are exported to ADS into three files (`.ael`, `.dat` and `.xml`).



You can select some or all the available padstacks/vias to export to ADS. The *Via group name* creates the via components in ADS and lets you place a via component in ADS layout from the specific via group.

Note: It is recommended to use a unique group name for each design.