

# **Best Practices: Setting Up a Die Stack**

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# Setting Up a Die Stack

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This document describes the recommended best practice to ensure success in setting up a package cross-section and a die stack.

For complete information on this topic, see the *Allegro X User Guide: Preparing the Layout* and the *Allegro X PCB and Package Physical Layout Command Reference*.

To set up a die stack, perform these steps:

- [Step 1: Define the Package Cross-Section](#) on page 5
- [Step 2: Define the Die Stack](#) on page 6
- [Step 3: Define a Spacer Symbol](#) on page 7
- [Step 4: Define an Interposer Symbol](#) on page 8
- [Step 5: Route to and from the Interposer](#) on page 9

## Step 1: Define the Package Cross-Section

1. Choose *Setup – Cross-section* from the menu in Allegro X Advanced Package Designer to open the Cross-section Editor window.
2. Add the appropriate layers between the surfaces:
  - ☐ Each flip-chip die requires a CONDUCTOR layer and a DIELECTRIC layer above and below it. Generally, you place flip-chip dies on the top package substrate or bottom package substrate, or both.
  - ☐ Each wire bond die requires a DIE layer outside the package substrate with a DIELECTRIC layer above and below it.
  - ☐ Each interposer requires a DIE layer outside the package substrate with a DIELECTRIC layer above and below it.
  - ☐ Each spacer requires a DIELECTRIC layer that is named to allow the placement of geometry on it.

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### Example

The following table shows a stackup example and the layers that you use to create it. Note that the blue layers are die-stack layers. The die-stack editor maintains the ordering and sequencing of these layers. For example, if you add these layers above the substrate in the cross-section, and then want to move them below the substrate, you do not need to change the cross-section. Instead just change the Placement Layer in the die-stack editor.

Cross-section Editor

Export Import Edit View Filters

Primary

Objects		Types				Thickness	Physical		Embedded	Signal Integrity		
#	Name	Layer	Layer Function	Manufacture	Constraint	Value um	Layer ID	Material	Embedded Status	Conductivity mho/cm	Dielectric Constant	SI Ignore
1	WS2	Surface									1	
2	SP1	Die Stack					01					
3	WS1	Die Stack					02					
4	IP1	Die Stack					03					
5	TOP_COND	Conductor	Conductor			30.48	1	Copper	Not embedded	596000	1	
6	VSS	Plane	Plane			30.48	2	Fr-4	Not embedded	596000	4.5	
7	VDD	Plane	Plane			30.48	3	Fr-4	Not embedded	596000	4.5	
8	BOT_COND	Conductor	Conductor			30.48	4	Copper	Not embedded	596000	1	
		Surface									1	

## Step 2: Define the Die Stack

1. Add the required die and BGA to the design.

Use these commands: *Add – Co-Design Die* or *Add – Standard Die*; *Add – Standard Package*.

**Note:** You place flip-chip dies on the top or bottom substrate surfaces, or both; place wire bond dies on DIE layers above or below the substrate surfaces, or both, as necessary.

2. Add the spacers and interposers as required.

Use these commands: *Add – Spacer*, *Add – Interposer*. See [Step 3: Define a Spacer Symbol](#) and [Step 4: Define an Interposer Symbol](#) for definition requirements.

3. Choose *Edit – Die Stack* to open the Die-stack Editor.

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The dies, interposers, and spacers in the selected diestack are listed in the *Die stack members* group.

4. For each die, interposer, or spacer listed specify or reset the parameters as required.

**Note:** Right-click the RefDes to access options.

## Step 3: Define a Spacer Symbol

You can add spacers from pre-defined spacer symbols or create them in real time using the *Add – Spacer* command.

To pre-define a spacer symbol:

1. Build the symbol.
2. Specify the properties.

### Step a: Building the Symbol

When you build the symbol in the Symbol Editor, add the following to the mechanical symbol (*.bsm*):

- A filled rectangle on *PART\_GEOMETRY/PLACE\_BOUND\_TOP*
- A filled rectangle on *CONDUCTOR/TOP* class and subclass
- Ref ID text on *REF\_DES/ASSEMBLY\_TOP*
- A rectangle on the *PART\_GEOMETRY/ASSEMBLY\_TOP* class and subclass (optional)

### Step b: Specifying Properties

When you create a spacer symbol in the Symbol Editor, you can specify properties for a spacer's thickness, material, and part number using the property edit command. Each spacer symbol instance in a package design inherits these properties. You need to enter valid values for Material Name and Thickness before the SiP tool can place the symbol. The property names are:

- *DIELECTRIC\_THICKNESS*, a number, for example, 100.00
- *DIELECTRIC\_MATERIAL*, a material existing in the material file (*mcmmat.dat*), for example, *PHENOLIC*

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You can invoke the Material Browser by clicking the ... button that follows the Material text box in the Add Spacer dialog box.

- *PART\_NUMBER*, an alphanumeric string, for example, 1ZX-256X-CL4

## Step 4: Define an Interposer Symbol

Due to the complexity of interposer symbols, you cannot create them in real time using the Add - Interposer command. You must add them from pre-defined symbols.

To build an interposer symbol:

1. Build the package symbol.
2. Specify the properties.

### Step a: Building the Package Symbol

Before adding an interposer to a die stack, build it as a package symbol (.psm) with the following:

- A filled rectangle on PART\_GEOMETRY/PLACE\_BOUND\_TOP
- Ref ID text on REF\_DES/ASSEMBLY\_TOP
- Clines, vias, and shapes on CONDUCTOR/TOP
- A rectangle on the PART\_GEOMETRY/ASSEMBLY\_TOP class and subclass (optional)
- A corner mark to help view rotations

**Note:** The interconnect that you use for interposer symbols is limited to clines, vias, and shapes (no pins).

### Step b: Specifying Properties

You must add the BOND\_PAD property to every via that will have a wire bond attached to it (This tags the vias as bond fingers). You can add the properties for the thickness, material, and part number for an interposer in the Symbol Editor or add the values directly into the Add Interposer dialog box. The SiP tool assigns these properties to each interposer symbol instance in a package design. If the SiP tool does not find a given property on the pre-defined symbol, you need to enter a value in the dialog box before the SiP tool can place the symbol. The property names are:



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- PART\_NUMBER, an alphanumeric string, for example, 1ZX-256X-CL4 (optional)
- CONDUCTOR\_THICKNESS, a number, for example, 30.48
- CONDUCTOR\_MATERIAL, a material existing in the material file, mcm\_mat.data, for example, COPPER
- DIELECTRIC\_THICKNESS, a number, for example, 100.00
- DIELECTRIC\_MATERIAL, a material existing in the material file, mcm\_mat.dat, for example, CERAMIC

**Note:** You can invoke the Material Browser by clicking the ... button that follows the Name text box in the Add Interposer dialog box.

## Step 5: Route to and from the Interposer

This section describes routing to and from the interposer.

### Routing to the Interposer

1. From the menu, choose *Route – Wire Bond – Add* and select the die pins for wire bonding.

In the Options tab:

- ☐ Add a new Group name.
- ☐ Select the Wire Profile.
- ☐ Set Pattern Style to Direct Connection.

Because the bond fingers already exist on the interposer, the wirebonder ignores the bond finger set in the dialog box and uses the bond finger on the interposer.

2. In the design, right-click and choose Settings to set any necessary wire bond constraints.
3. Guide the wire bonds to make the connections to the bond fingers on the interposer.

### Routing from the Interposer

1. Run `wirebond select`.
2. Set the Find Filter to Vias only to allow selection of the interposer bond fingers.
3. Select the interposer bond fingers for wire bonding.

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**4.** Right-click and choose Add.

In the Options tab:

- ☐ Add a new Group name.
- ☐ Select the Wire Profile.
- ☐ Set the Pattern Style.
- ☐ Set the Pattern Length.
- ☐ Set the terminating bond finger padstack.

**5.** Right-click in the design and choose *Settings* to set any necessary wire bond and bond finger attributes and constraints.

**6.** Guide the wire bonds to the terminating bond finger locations.