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# Allegro® Design Synchronization and Packaging User Guide

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# Contents

# Preface

## About This Guide

The *Design Synchronization and Packaging User Guide* demonstrates the major features of the Design Synchronization solution, which is part of the front-to-back flow for PCB design. The Design Synchronization toolset lets you compare the logical design, that is, the schematic, and the physical design, that is, the board. You can update changes from the board to the schematic or from the schematic to the board. However, you cannot update changes across schematics or boards.

The *Design Synchronization and Packaging User Guide* describes how to:

- Set packaging options and package a design
- Control the property flow between a schematic and a board
- Synchronize the schematic and the board for any design. The guide details the functions of all tools in the Design Synchronization toolset and explains the procedures used in synchronizing the schematic and the board. You can synchronize the following differences:
  - connectivity differences
  - net differences
  - component differences
  - net property differences
  - pin property differences
  - component property differences

You can use the *Design Synchronization and Packaging User Guide* to also understand Visual Design Differences (commonly referred to as Design Differences), Design Association, and Packager Setup. You will also find information about the commands and the associated tasks related with the dialog boxes of the Design Synchronization toolset in the *Design Synchronization and Packaging User Guide*.

# How To Use This Guide

The *Design Synchronization and Packaging User Guide* contains the conceptual and procedural information necessary to use the Design Synchronization toolset. The organization of the user guide is based on how different tools in the Design Synchronization toolset are used to synchronize the schematic and the board. The first chapter explains the design synchronization process. The subsequent chapters explain how to use the different Design Synchronization tools. See details in the Brief Outline of Different Chapters section.

If you are a new user and do not have any prior working experience with the Design Synchronization toolset, begin from the first chapter and continue learning about different tools in the sequence covered in the user guide. If you are using the user guide to find information about a design synchronization tool, you can refer directly to the chapter corresponding to a tool.

This guide assumes that you are familiar with the following tools in the front-to-back flow for PCB design:

- Allegro Project Manager
- Allegro Design Entry HDL
- Allegro PCB Editor

# Brief Outline of Different Chapters

In Chapter 1, “Introduction to the Design Synchronization Process,” you will learn about the reasons for design synchronization. You will know about the functions of different tools in the Design Synchronization toolset. You will also learn about important steps in the design synchronization process.

In Chapter 2, “Setting Up Packager-XL,” you will learn to set Packager-XL properties and directives. Packager-XL is a tool used to translate the schematic into the board and backannotate the changes made in the board to the schematic.

In Chapter 3, “PCB Editor-Design Entry Property Flow,” you will learn to control the flow of properties between PCB Editor and Design Entry HDL. By controlling the property flow, you have greater control in packaging a design. You can decide which properties should be packaged or backannotated.

In Chapter 4, “Packaging Your Design,” you will see the essential requirements to package a design. You will understand the difference between the Forward and Feedback mode for packaging a design. In the Forward mode, you package the schematic into the board. In the Feedback mode, you backannotate the changes from the board to the schematic. In this

chapter, you will also learn to create netlists and synchronize the changes between the board and the schematic.

In Chapter 5, “Resolving Design Differences,” you will use the Visual Design Differences (VDD) tool to view the differences between the schematic and the board. You will also learn to filter specific differences, and update a specific difference or all differences in either the schematic or the board.

In Chapter 6, “Using Design Association,” you will use the Design Association tool to synchronize the connectivity changes between the schematic and the board. You will be able to identify the different types of markers and use them to synchronize the schematic and the board.

# Related Documentation

If you want to learn by working on tasks, see *Design Synchronization Tutorial*. This tutorial includes a design example and step-by-step instructions that are useful to practice synchronizing boards and schematics.

The *Design Synchronization and Packaging User Guide* introduces the basic concepts of packaging a design. For a more detailed description of the packaging process and how you can optimize it, see *Packager-XL Reference*.

# 1

# Introduction to the Design Synchronization Process

## Overview

The development of any design requires synchronization between the schematic and the board. Based on how you prepare a new design, you can synchronize the schematic and the board in one of the following two ways:

1. The conventional or linear flow

   In the conventional flow, you first design the schematic, make changes to it, and get the schematic reviewed and approved. Next, you prepare the board and send it for manufacturing. When you prepare the board, last-minute changes, such as adding termination resistors or removing certain components, can cause property changes and connectivity differences between the schematic and the board. These changes need to be backannotated to the schematic.

2. The parallel flow

   In the parallel flow, schematic designers and board designers work in parallel. First, the schematic designer starts work on the schematic. At a logical point, the board designer imports the schematic and uses it to create the board. Meanwhile, the schematic designer starts work on the next module. At the next logical point, the schematic designer might add some new information to the schematic and the board designer might make changes to the board that require backannotation to the schematic. Therefore, it is important to synchronize the schematic and the board.

Whether you follow the linear flow or the parallel flow, it is important that the schematic and the board are always synchronized. The process of synchronizing the schematic and the board is called design synchronization. You can use the Design Synchronization toolset to synchronize differences between the schematic and the board.

# Need for Synchronization

The primary need for synchronization is caused by changes that occur either in the board or in the schematic after the initial transfer of packaged information to the board.

The following four changes occur in the board after the initial transfer of packaged information from the schematic:

1. Component changes

   You might add new components in the design to handle signal integrity and electromagnetic compatibility problems. These components can include termination resistors, series or shunt buffers, and bypass capacitors.

2. Connectivity changes

   You might make connectivity changes to facilitate routing after the initial placement of components. Connectivity changes might be caused by pin swaps, section swaps, and reference designator (refdes) swaps.

3. Reference designator changes

   You might change the reference designators to debug board problems.

4. Property changes

   You might modify certain components in the board. These modifications will cause property changes.

Besides the changes in the board after the initial transfer of packaged information from the schematic, certain changes, such as Engineering Change Order (ECO), are also made in the schematic. The need for the Design Synchronization toolset arises from the need to synchronize these differences between the schematic and the board.

# Design Synchronization Toolset

The Design Synchronization toolset includes the following tools:

- Packager Setup
- Packager Utilities
- Design Differences
- Design Association
- Netrev

- Genfeedformat

## Packager Setup

The Packager Setup tool is used to view or change the default packaging setup options in the project file. By controlling the default packaging options, you can define the properties that must be packaged or backannotated. You can also control the reports that you want to generate while packaging a design.

Packager utilities and Design Differences follow the Packager Setup options of the project file. You can change the Packager settings in the Packager Setup tool and thereby control how the design is packaged.

**Note:** The word Packager represents Packager-XL. Packager-XL is the interface between the logical design (schematic) and the physical layout (board) in the Cadence Board Design Solution.

## Packager Utilities

There are five Packager utilities:

- Export Physical
- Import Physical
- BOM
- Electrical Rule Check
- Netlist Reports

### Export Physical

Export Physical translates a logical design entered in Design Entry HDL into a physical design ready for layout. For more information about translating a logical design into a physical design, refer to Exporting the Design on page 29.

### Import Physical

Import Physical receives property/swapping changes made in PCB Editor and incorporates them into the logical design. See Importing the Design on page 32 for more information about feeding back the changes made in a board to the schematic.

### BOM

The Bill of Material (BOM) utility creates BOM reports that are useful for manufacturing. You can use the BOM-HDL tool to generate BOM reports in multiple formats such as text, spreadsheet, and HTML. BOM-HDL supports standard templates that display BOM reports in a user-friendly manner. Besides, you can create new templates to customize the report. See Generating the Bill of Materials on page 101 for more information about generating BOM reports.

### Electrical Rule Check

The Electrical Rule Check utility helps you check for compatible outputs, single-node nets, source/driver checks, net loading, and pin directions. The utility generates a summary of electrical rule violations in a report named `erc.rpt`. See Running Electrical Rule Checks on page 102 for more information about performing electrical rule checks.

### Netlist Reports

The Netlist Reports utility prepares different types of netlist reports. See Generating Netlist Reports on page 104 for more information about generating netlist reports.

## Design Differences

The Design Differences tool (also referred to as Visual Design Differences or VDD) compares schematics and boards and generates a list of differences. VDD displays these differences in difference view windows. VDD records the following:

- Differences in instances, nets, and pin connectivity
- Differences in properties on instances, nets, and pins
- Information about function and pin swaps
- Information about renamed reference designators

VDD supports various controls to view, query, and filter the differences between the schematic and the board. You can update either the schematic or the board by accepting or rejecting individual differences. You can even accept or reject all differences simultaneously.

### Design Association

Design Association (DA) is used to update the connectivity changes made in the board to the schematic. To update the connectivity changes, Design Association requires the `dessync.mkr` file produced by the Design Differences tool.

### Netrev

Netrev is a tool that loads the packager output into a database for the physical layout. This database works as the board file, which is operated on by PCB Editor or Allegro SI.

### Genfeedformat

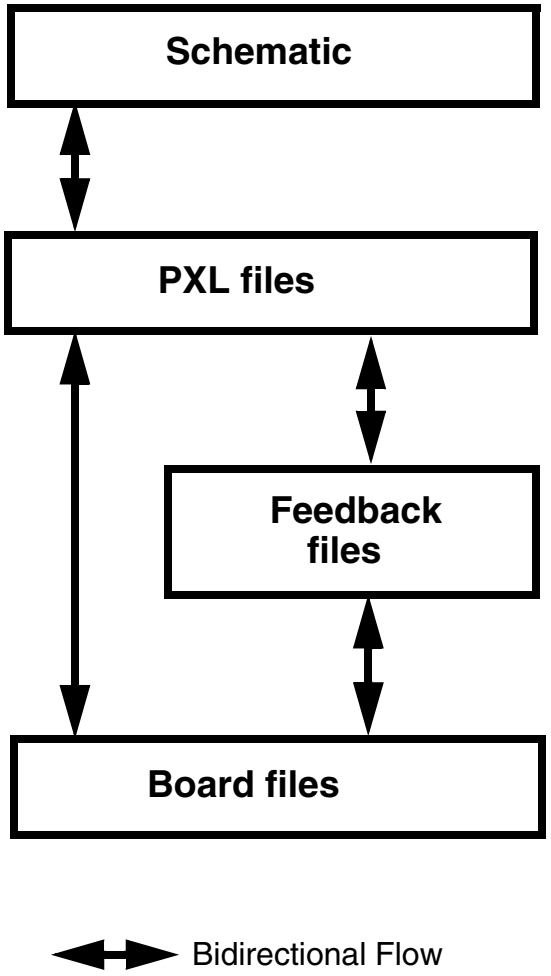
Genfeedformat extracts connectivity and property information from the board into view files that are used by Design Differences and Packager-XL.

## Front-to-back Flow

### Overview

Traditionally, before the release of Design Synchronization tools, the conventional front-to-back flow worked as depicted in Figure 1-1 on page 22.

**Figure 1-1 Conventional front-to-back Flow**




1. Create schematic files by using a schematic editor such as Design Entry HDL.
2. Package the design into Packager-XL files. Three files (`pstchip.dat`, `pstxprt.dat`, and `pstxnet.dat`) are generated.
3. Use netrev to take the Packager-XL files to the board.
4. Feed back the property changes to the schematic by generating the feedback files (`pinview.dat`, `netview.dat`, `funcview.dat`, and `compview.dat`) and use these files to create Packager-XL backannotation files to backannotate the schematic.

While the conventional flow was able to successfully transfer property changes made in the board back to the schematic, it could not highlight connectivity changes to the schematic. The conventional front-to-back flow did not have any tool that could capture the connectivity

changes in the board and feed them back to the schematic. The use of the Design Synchronization toolset helped overcome the problem of synchronizing the connectivity changes between the schematic and the board.

## Front-to-back: Constraint Manager-Enabled Flow

In the Constraint Manager-enabled flow, Constraint Manager is used for managing electrical constraints in Design Entry HDL. If you use Constraint Manager in Design Entry HDL to manage electrical constraints, Constraint Manager saves information about electrical constraints in a new view named constraints under the root design. This view includes a file named <*root_design*>.dcf, which contains a snapshot of electrical constraint information in the design.

*Important*

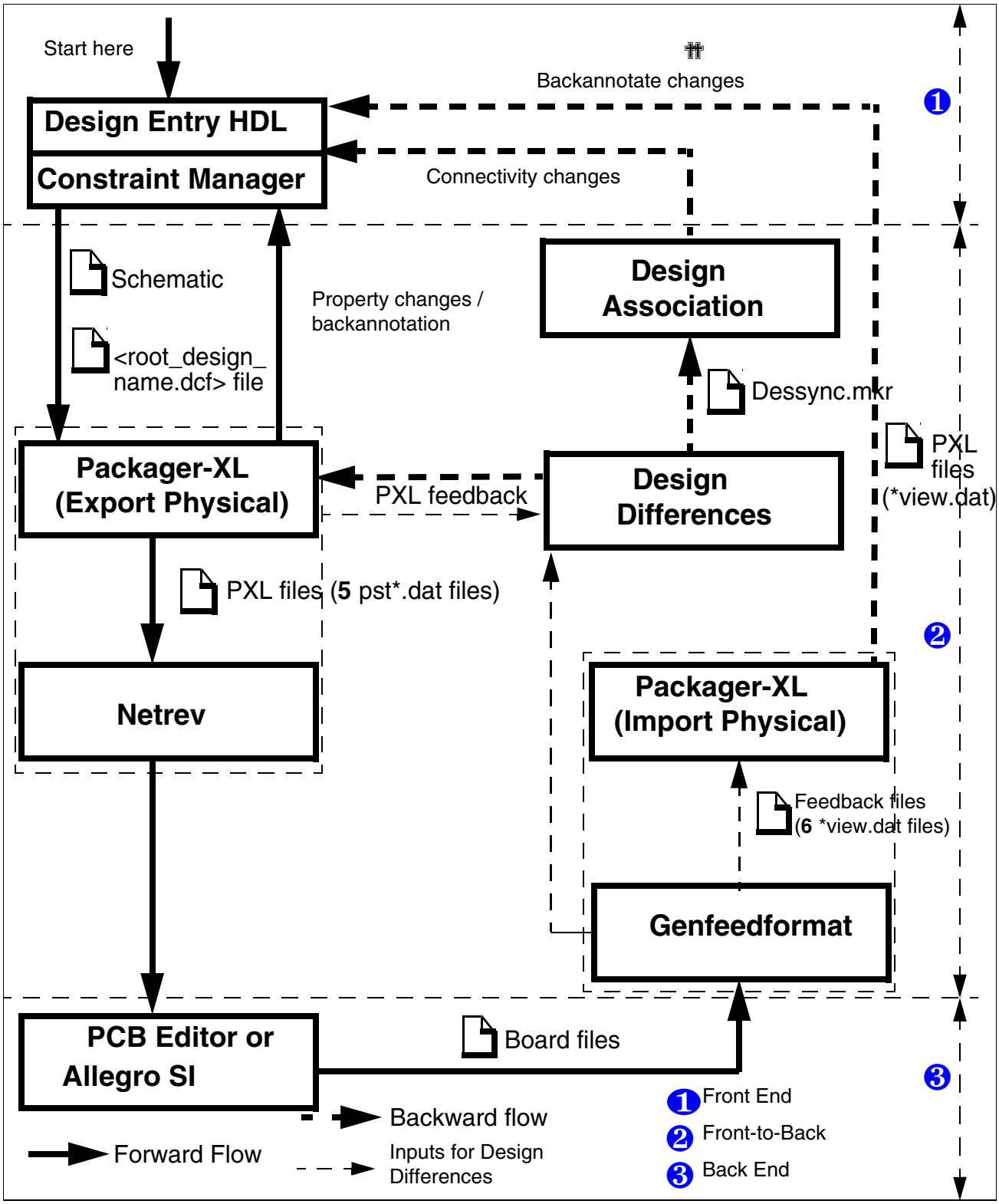
If you are using the Constraint Manager-enabled flow:

- You must not use Design Entry HDL 16.3 with PCB Editor or Allegro SI 16.2 or earlier versions.
- You must not use Design Entry HDL 16.2 or a previous version with PCB Editor or Allegro SI 16.3.

## Overview

The front-to-back flow works as depicted in the following figure:

**Figure 1-2 Front-to-back Flow**



In the Constraint Manager-enabled flow, Packager-XL creates five `pst*.dat` files when you run Export Physical (with *Package Design* and *Update PCB Editor Board (Netrev)* check boxes selected). These include the three files generated in the traditional flow (`pstchip.dat, pstxprt.dat`, and `pstxnet.dat`) and the following two files:

- **pstcmdb.dat**—Contains the definitions of electrical constraints in the schematic as defined and created in the Constraint Manager database. This file is a copy of the <*design_name*>.dcf file in the `constraints` view, where <*design_name*> represents the name of the root cell of the schematic, and the dcf extension signifies that the file is a constraint file.

The four `pst*.dat` files are used by `Netrev` to create or update the board. You can make changes in PCB Editor and then feed back the changes in the board to the schematic by running Import Physical (with the *Generate Feedback Files* and *Package Design* check boxes and the *PCB Editor* option selected). Import Physical allows you to overwrite all current electrical constraints in the schematic with the electrical constraint information in the PCB Editor board file or import only the electrical constraint information that has changed in the PCB Editor board file since the last import. Import Physical detects the presence of the <*root_design_name*>.dcf file and runs in the Constraint Manager-enabled flow.

If the <*root_design_name*>.dcf file is in the `constraints` view of the root design, you are using the Constraint Manager-enabled flow. The *Extract Constraints* check box in the *Import Physical* dialog box will be selected by default. When you run Import Physical, `genfeedformat` creates the following six feedback files—`pinview.dat`, `netview.dat`, `funcview.dat`, `compview.dat`, `cmdbview.dat`, and `cmbcview.dat`. Note that the first four files are the same as those created in the traditional flow. The remaining two files contain electrical information as described below:

- **cmdbview.dat**—Describes the current electrical constraint information for the design.
- **cmbcview.dat**—Specifies the base copy of the electrical constraint information used by the PCB Editor board snapshot.

You can now use the feedback files to synchronize the schematic and the board by doing one of the following:

- Choose *Tools > Back Annotate* in Design Entry HDL to backannotate all the changes in the board to the schematic.

  Select the *Package Backannotation* check box in the *Backannotation* dialog box to backannotate all changes (excluding changes in electrical constraint information) in the board to the schematic. Select the *Constraint Backannotation* check box in the *Backannotation* dialog box to backannotate changes in electrical constraint information in the board to the schematic.

- Use the Design Differences (VDD) and Design Association (DA) tools to resolve individual connectivity and property differences between the schematic and the board.

  Use VDD to update the property differences either to the board or to the schematic. When you run VDD, it displays differences in properties between the schematic and the board in multiple windows. The differences in electrical constraints information in the schematic and the board are displayed in two difference windows—*Constraints Differences-Logical* and *Constraints Differences-Physical*. See Differences View Windows: Traditional Flow on page 117 for more information about these windows.

  Use DA to update the connectivity changes made in the board to the schematic. DA uses a file generated by VDD named `dessync.mkr` (which captures connectivity information) to guide you in updating the schematic.

## Design Synchronization Tasks

The entire Design Synchronization process can involve the following tasks:

1. Package and export the Design Entry HDL schematic design to the PCB Editor or SI layout by running Packager-XL in the Forward mode. Use Export Physical to package the design.
2. Compare the schematic and layout designs by using the Design Differences tool.
3. Package the design for feedback by running Packager-XL in the Feedback mode.
4. Generate the `dessync.mkr` marker file to backannotate the physical connectivity changes to the Design Entry HDL schematic by using the Design Association tool.
5. Backannotate the schematic based on information in the board.
6. Run the Packager utilities to complete any or all of the following steps:
   a. Generating the Bill of Materials
   b. Performing electrical rule checks
   c. Generating netlist reports
7. Run Packager Setup to complete any or all of the following steps:
   a. Viewing the default Packager Setup options
   b. Changing the default Packager Setup options

# Getting Started with Design Synchronization

## Overview

Depending on the task to execute, you can launch one of the following tools:

- Design Differences
- Design Association
- Packager-XL
- Packager utilities (Bill of Materials, Electrical Rules, Netlist Rules, Export Physical, and Import Physical)

You can launch these tools from either the Project Manager user interface or the Design Entry HDL schematic editor.

## Launching Design Differences

You can launch Design Differences in one of the following three ways:

- Click the *Design Sync* icon in Project Manager. A drop-down list appears. Select the *Design Differences* option from the list.
- From Project Manager, choose *Tools – Design Sync – Design Differences*.
- From Design Entry HDL, choose *Tools – Design Differences*.

## Launching Design Association

Before you launch the Design Association tool, ensure the following:

- You have expanded the design in the Design Entry HDL editor. A warning message to expand the design is displayed if you launch the Design Association tool without expanding the Design Entry HDL design.
- You have run the Design Differences tool and generated the `dessync.mkr` marker file. This file is used by Design Association to synchronize connectivity differences.

To launch Design Association:

➤ From the Design Entry HDL menu bar, choose *Tools – Design Association*.

### Launching Packager Setup

You can launch Packager Setup in one of the following two ways:

1. Click *Advanced* in the Export Physical or Export To Packager Files dialog box.
2. Click *Options* in the Import Physical, Design Differences, or Import From Feedback Files dialog box.

### Launching Packager Utilities

You can launch Export Physical and Import Physical utilities from Project Manager in one of the following two ways:

1. Click the *Design Sync* icon.
2. Choose *Tools – Design Sync,* and click on the *Export Physical* or *Import Physical* option in the drop-down menu.

To launch other Packager utilities such as Bill of Materials, Electrical Rules, and Netlist Reports, complete the following step:

➤ Choose *Tools – Packager Utilities,* and click the appropriate option.

## Design Synchronization Process

The following are the key procedures in the Design Synchronization process:

- Define Packager-XL setup options.
- Package the design.
- Run Packager utilities.
- Export the design.
- Compare the schematic and the layout.
- Import the design.

## Defining Packager Setup Options

The Packager Setup tool helps you record the default packaging setup options in the project file. The `Export`, `Import`, `Design Differences`, `Package`, and `Feedback` commands use the default packaging settings in the project file to complete their operations.

You can use Packager Setup to change the information about properties and define how to package them. For example, you can use Packager Setup to change the properties that will be packaged in the Forward and Feedback modes. You can also use the Packager Setup tool to define how Packager-XL formats output reports. See Setting Up Packager-XL on page 35 for more information about the different Packager Setup options and how to change them.

## Packaging the Design

Packaging involves converting a logical design into a physical layout and vice versa. The utility that completes packaging is Packager-XL. Packager-XL works in the following two modes:

- Forward Mode

  Packager-XL translates a logical design entered in Design Entry HDL into a physical design ready for layout on PCB Editor.

- Feedback Mode

  Packager-XL receives the changes made in the physical design in PCB Editor and incorporates these changes into the logical board.

See Packaging Your Design on page 71 for more information about packaging a design.

## Running Packager Utilities

There are three packager utilities: the BOM utility, the Electrical Rules utility, and the Netlist Reports utility. Using these utilities, you can generate the Bill of Material reports, run electrical rule checks on the design, and generate netlist reports.

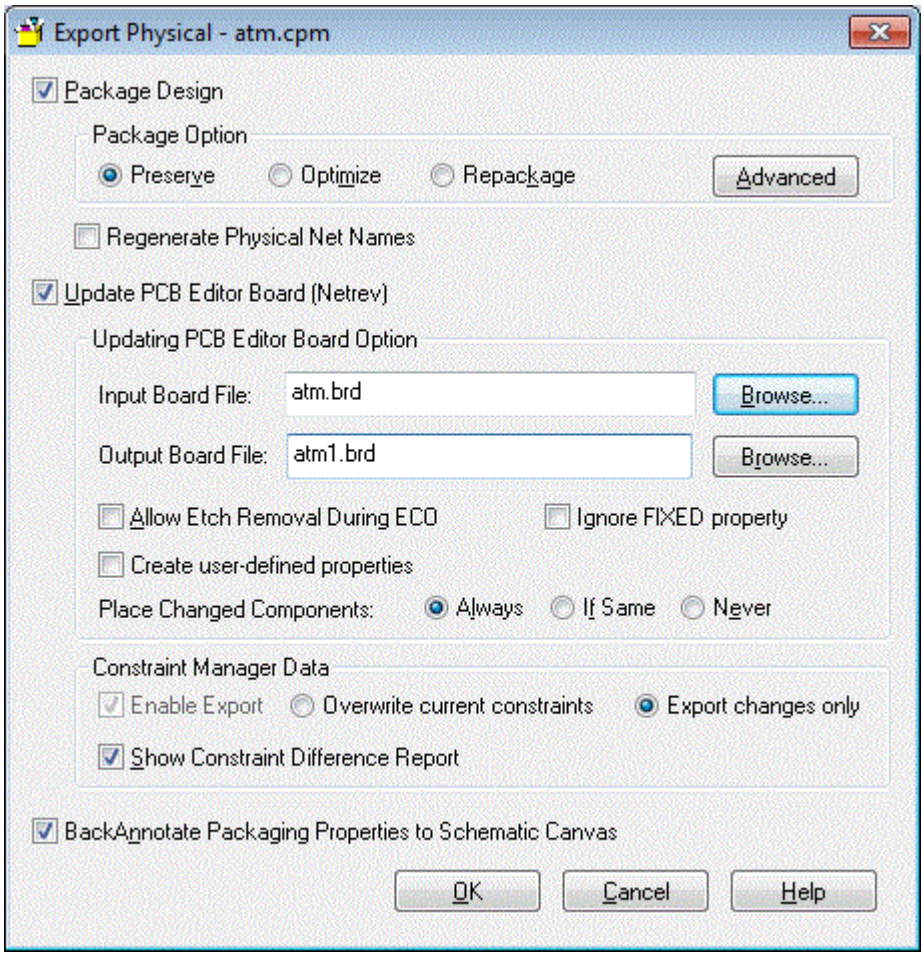
See Packaging Your Design on page 71 for more information about the Packager utilities.

## Exporting the Design

The `Export Physical` command transfers the Design Entry HDL schematic to the physical PCB Editor layout database. To run this command, you use the Export Physical dialog box.

Depending on the presence of the <*root_drawing*>.dcf file in the constraints view, Export Physical runs in the Constraint Manager-enabled flow. See Running Packager-XL in the Forward Mode on page 83 for more information about running Export Physical in different flows.

**Figure 1-3 Export Physical Dialog Box**




➤ Click *OK* in the Export Physical dialog box to run the `Export Physical` command.

The `Export Physical` command performs the following tasks:

- Expands and packages the schematic design by using Packager-XL (if you have selected the *Package Design* option and defined the packaging options)
- Transfers the schematic design to the PCB Editor layout by using the netrev program
- Transfers information about electrical constraints to PCB Editor and updates the physical PCB Editor or SI layout board with the latest logical schematic data

- Backannotates the latest packaged and constraint information to the schematic

See Packaging Your Design on page 71 for more information about exporting a design.

## Comparing the Schematic and the Layout

A design and a board are “in sync” when they represent the same logical circuit, have identical packaging, and share the same set of properties. They get “out of sync” when changes are made to the board or the schematic.

The `Design Differences` command finds differences between the board (physical data in the PCB Editor or SI layout) and the schematic (logical data in the Design Entry HDL schematic) when they are “out of sync”. To run the `Design Differences` command, you use the Design Differences dialog box. Design Differences may run in the Constraint Manager-enabled flow.

- Constraint Manager-enabled flow: In this flow, Design Differences displays constraint differences in two new Constraints Differences windows, one each for the logical and physical domains. Any constraint property differences are filtered from the net-properties difference windows and displayed in the new windows.

  **Note:** See Differences View Windows: Constraint Manager-Enabled Flow on page 118 for more information about Constraints Differences windows.

  The Constraint Manager-enabled flow is selected when the <*root_drawing*>.dcf file is found in the constraints view or the `pstcmdb.dat` or `cmbcview.dat` or `cmdbview.dat` files are present in the packaged view.

**Note:** See Design Differences Functions on page 111 for more information about comparing the schematic and the layout and resolving design differences.

The `Design Differences` command performs the following tasks:

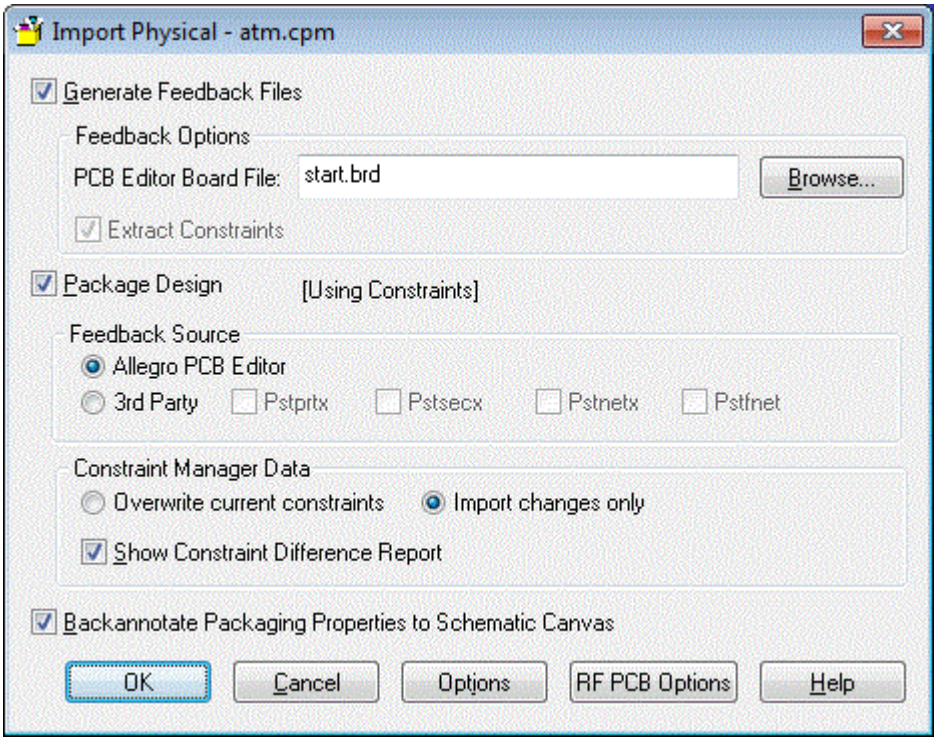
- Calls Export Physical to package the design
- Extracts the design from PCB Editor
- Generates design differences
- Displays the Design Differences user interface

## Importing the Design

The `Import Physical` command transfers the physical design from the PCB Editor or SI layout database to the Design Entry HDL schematic. To run the `Import Physical` command, use the Import Physical dialog box.

Depending on whether Constraint Manager has been used in Design Entry HDL and the selection of the *Extract Constraints* check box, Import Physical runs in the Constraint Manager-enabled flow. See Running Packager-XL in the Feedback Mode on page 90 for more information about running Import Physical in different flows.

**Figure 1-4 Import Physical Dialog Box**




➤ Click *OK* in the Import Physical dialog box to run the `Import Physical` command.

The `Import Physical` command performs the following tasks:

- Runs the PCB Editor extract program and generates feedback files using the Genfeedformat tool
- Processes the electrical constraint feedback files (`cmdbview.dat` and `cmbcview.dat`) generated from PCB Editor and updates the constraints view of the design

- Runs Packager-XL in the Feedback mode and packages the physical design
- Backannotates all the changes (electrical, connectivity, and constraints) made in the board to the schematic

**Note:** In the Constraint Manager-enabled flow, Import Physical, in addition to the above steps, will generate electrical constraint backannotation files. Packager-XL also extracts the constraints differences in the board to a file called `pstcmback.dat`.

If you do not backannotate the changes using Import Physical, you can use one of the following two operations to transfer the physical design changes from the layout database to the Design Entry HDL schematic:

- Choose *Tools - Backannotate* in the Design Entry HDL menu bar to feed back the changes from the layout to the schematic.
- Use the Design Association tool to feed back the connectivity changes from the layout to the schematic.

If you do not have access to PCB Editor or the PCB Editor layout (*.brd file), but have access to the feedback files, you can use them to feed back the physical design from the layout and backannotate the changes made in the layout to the design.

Feeding back involves generating the feedback files from the PCB Editor layout and packaging the design with the feedback files. To feedback to the design:

1. Choose *Design Sync - Import Physical* to launch the Import Physical dialog box.
2. Click *OK* to start the `Feedback` command.

By default, both the *Generate Feedback Files* and the *Package Design (Feedback)* options are selected in the Import Physical dialog box. Therefore, if you click the *OK* button without modifying these options, Packager-XL generates the feedback files and packages the design for feedback.

# 2

# Setting Up Packager-XL

## Overview

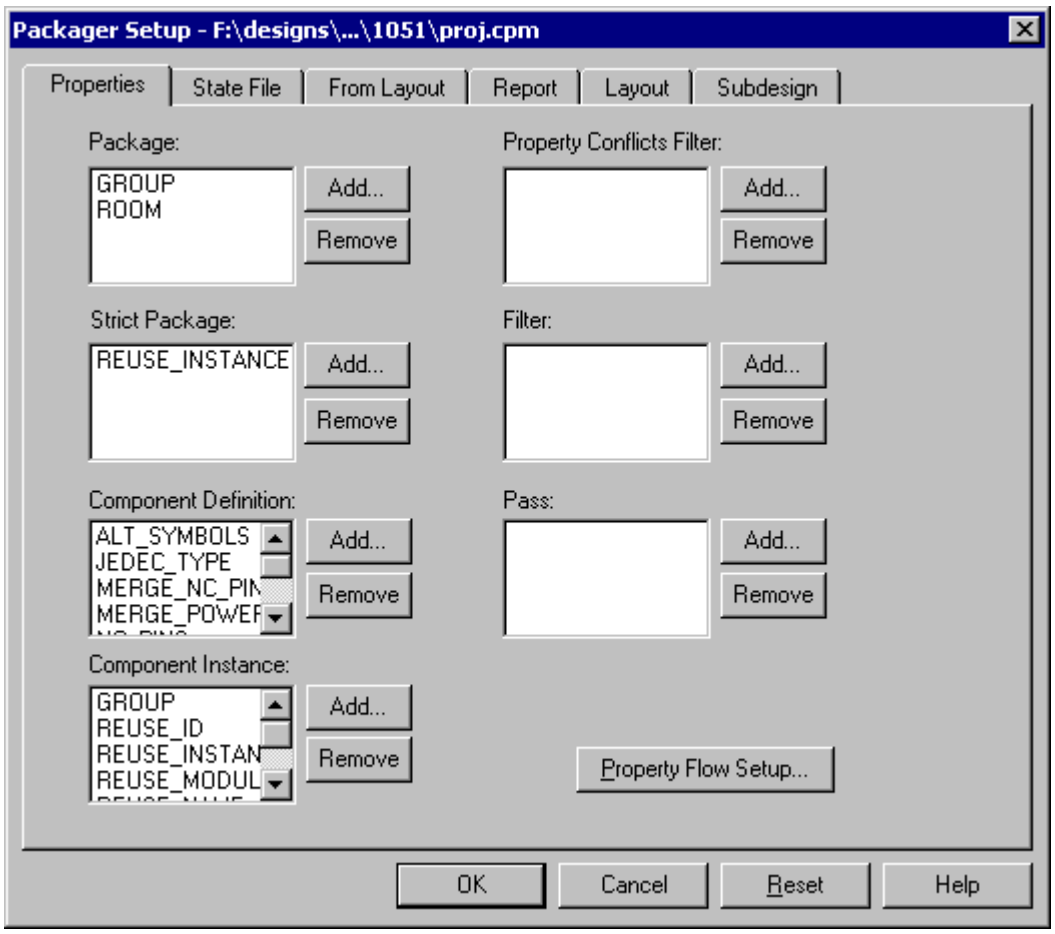
The Packager Setup tool is used to view or change the default packaging options in the project file. Packager utilities and Design Differences obtain their Packager Setup options from the project file. You can use Packager Setup to define how a design will be packaged.

## Packager Setup Dialog Box

To change any Packager Setup option, you use the Packager Setup dialog box. To launch the Packager Setup dialog box, refer to Launching Packager Setup on page 28.

**Note:** Depending on how you launch the Packager Setup dialog box, the available packaging options vary. If you launch Packager Setup from the Project Setup dialog box, the titlebar of the Packager Setup dialog box will display the name Project Setup. This dialog box contains all the options supported by Packager Setup. It also contains some additional options such as `Optimize` and `Repackage`.

**Figure 2-1 Packager Setup Dialog Box**




The Packager Setup dialog box contains six tabs:

- Properties Tab
- State File Tab
- From Layout Tab
- Report Tab
- Layout Tab
- Subdesign Tab

Each tab controls a group of Packager settings. To view or change the default Packager Setup options, you can select any of these tabs.

## Properties Tab

The *Properties* tab is the default tab. You use this page to package schematic instances that share the same properties. You can create component definition properties, that is, the properties for which Packager-XL creates alternate physical parts. You can also create filters that specify the properties that must not be packaged.You can specify the properties that should be listed in the Packager output files. Finally, you can use the *Property Flow Setup* button to launch the Property Flow Setup dialog box, which helps you to set the default properties that flow between Design Entry HDL and PCB Editor.

See Changing the Packager Setup Properties on page 38 for more information.

## State File Tab

You can use the *State File* tab to control the properties in the state file. The state file is used to store a flattened, packaged view of the design. It contains all the packaging properties used in the design, the physical net names, and the properties whose values differ from those in the schematic. Using the *State File* tab, you can define the properties in the state file that replace the corresponding properties in the schematic. You can also define the properties that will replace the properties in the layout file (in case of differing values). Finally, you can use the *State File* tab to remove properties from the state file.

**Note:** When you remove properties from the state file, the properties in the schematic or the layout automatically win.

See Changing Packaging Information in the State File on page 42 for more information.

## From Layout Tab

You can use the *From Layout* tab to control the properties that will be fed back or backannotated from the layout to the schematic. You can specify whether or not a particular property will be backannotated.

See Changing Feedback Properties in the Layout on page 45 for more information.

## Report Tab

You can use the *Report* tab to specify the Packager-XL output. By default, Packager-XL generates a number of report files. You can also select the report files that you need as output. For more information about Packager-XL report files, see Packaging Your Design.

You can also use the *Report* tab to control the display of warnings when Packager-XL packages a design. By default, all warnings are displayed. You can suppress any warning.

See Changing Packager Output Information on page 48 for more information.

### Layout Tab

You can use the *Layout* tab to modify layout netlist parameters and reference designators. You can change reference designator naming schemes. You can also change the default prefix for reference designators. You can increase or decrease the number of characters used to define component or physical net names. Finally, you can define which characters can or cannot be used in defining net names.

See Changing Reference Designators and Netlist Parameters on page 51 for more information.

### Subdesign Tab

You can use the *Subdesign* tab to specify how to package blocks in hierarchical designs. You can generate a specific subdesign state file for the block. After defining a subdesign state file, you can force packaging for each instance of the subdesign in the subdesign state file. You can even customize how packaging in the subdesign state file is used in place of new subdesign instances.

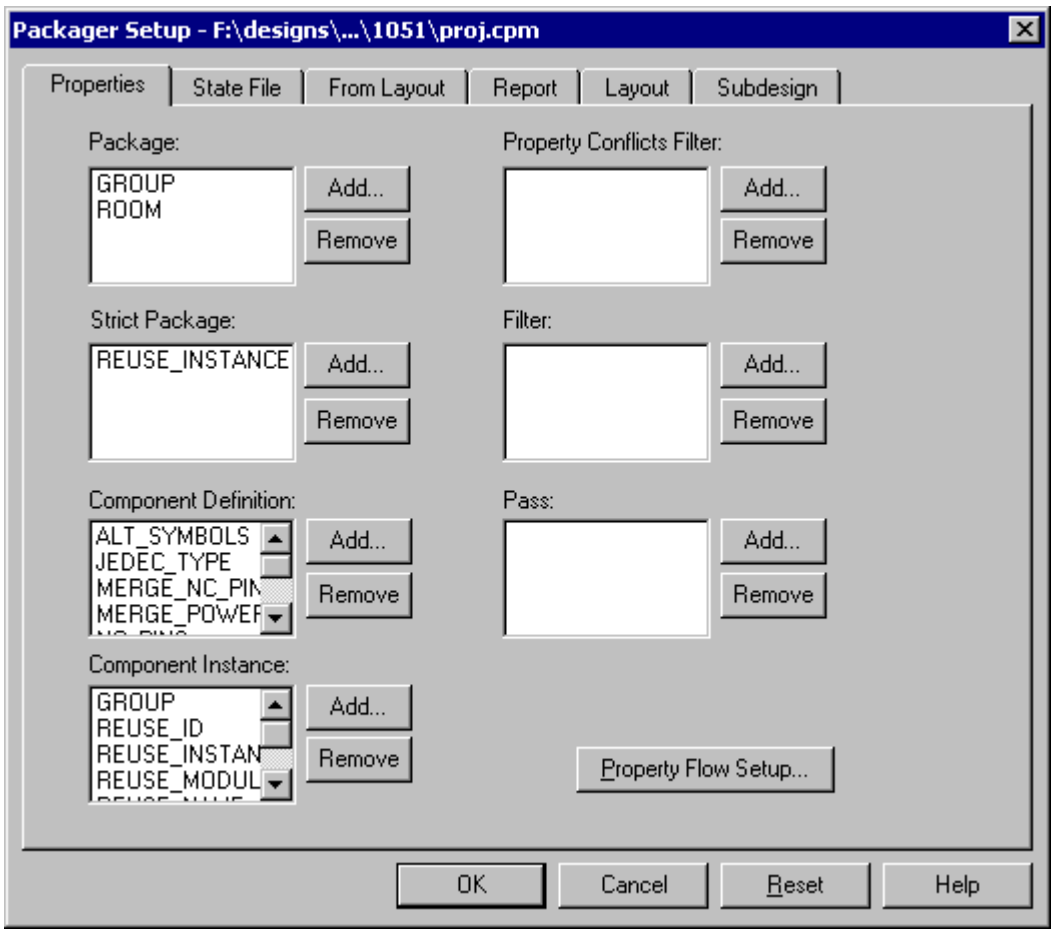
See Changing Setup Options While Packaging Subdesigns on page 54 for more information.


***Unless absolutely required, do not change the default settings.***

## Changing the Packager Setup Properties

To change the default properties that will be used by Packager-XL, use the Packager Setup - Properties Tab.

**Figure 2-2 Packager Setup - Properties Tab**




You can make seven types of property changes by using the *Properties* tab.

1. Make packages.

   A package consists of schematic instances that share properties with the same value. Packager-XL does not package together any instances that have different values for the same property. You can define packages by adding properties in the *Package* list box. For more information about adding or removing properties in the *Package* list box, see Adding and Deleting Properties.

   **Note:** The packaged properties are assigned the `PACKAGE_PROP` directive.

   For more information about the `PACKAGE_PROP` directive, see the Cadence document *Packager-XL Reference*.

2. Create strict packages.

A strict package is used to restrict the packaging of schematic instances. A strict package includes only the instances with the package properties. You cannot package any other properties in a strict package. You can define strict packages by adding properties in the *Strict Package* list box.

**Note:** Strict packages are defined using the `STRICT_PACKAGE_PROP` directive. See the Cadence document *Packager-XL Reference* for more information about the `STRICT_PACKAGE_PROP` directive.

3. Define component definition properties.

   Component definition properties are used by Packager-XL to create alternate physical parts. To define these properties, add them in the *Component Definition* list box.

   **Note:** Component definition properties are defined using the `COMP_DEF_PROP` directive. See the Cadence document *Packager-XL Reference* for more information about the `COMP_DEF_PROP` directive.

4. Define component instance properties.

   You can use the *Properties* tab to define the properties that will be treated as component instance properties. Packager-XL creates alternate physical parts for component instance properties. To define these properties, add them in the *Component Instance* list box.

   **Note:** Component instance properties are defined using the `COMP_INST_PROP` directive. See the Cadence document *Packager-XL Reference* for more information about the `COMP_INST_PROP` directive.

5. Define the properties that be filtered from the `pstprop.dat` file.

   To filter a conflicting property from the `pstprop.dat` file, you can add it to the *Property Conflicts Filter* list box.

6. Filter properties.

   To omit any property from the packager output files, you can add them to the *Filter* list box.

   **Note:** The `FILTER_PROPERTY` directive is used to filter out properties from the packager output files. See the Cadence document *Packager-XL Reference* for more information about the `FILTER_PROPERTY` directive.

7. Pass properties to the packager output files.

   To pass any property to the packager output files, you can add it to the *Pass* list box.

   **Note:** The `PASS_PROPERTY` directive is used to pass properties to the packager output files. See the Cadence document *Packager-XL Reference* for more information about

the PASS_PROPERTY directive.

8. Change the default property flow between Design Entry HDL and PCB Editor.

   Click the *Property Flow Setup* button to launch the Property Flow Setup dialog box. You can use the Property Flow Setup dialog box to add, edit, or remove properties that flow between Design Entry HDL and PCB Editor. You can even change the property flow by importing properties from the `pxlBA.txt` file and packaged files.

After you have added or removed properties, check if you need to change any other setup options in the other five tabs. To change information in another tab, select that tab and make the required changes. Click the *OK* button to accept the changes, or click the *Cancel* button to ignore the changes.

If you have made any property changes in the current session and want to ignore the changes, click the *Reset* button.

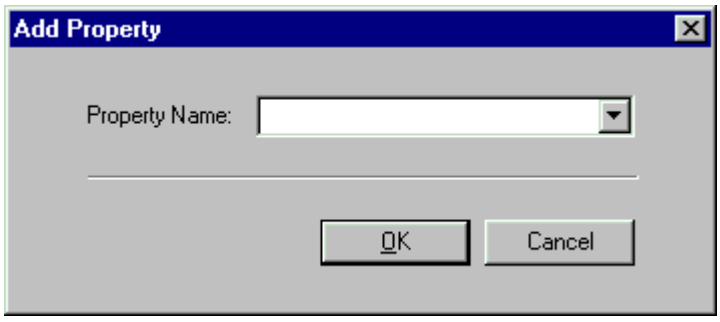
## Adding and Deleting Properties

### Adding a Property

1. To add a property to any list in the Packager Setup dialog box, click the *Add* button corresponding to that list.

   The Add Property dialog box appears.

**Figure 2-3 Add Property Dialog Box**




2. To add the property, type its name in the *Property Name* list. You can also select a name from the *Property Name* list.
3. Click *OK* to add the property.

### Removing a Property

1. Select the property to be removed in the Packager Setup dialog box.
2. Click the *Remove* button.

# Changing Packaging Information in the State File

## Overview of the State File

The state file is used to store a flattened, packaged view of the design. It contains all the packaging properties used in the design, physical net names, and the properties whose values differ from those in the schematic. By default, Packager-XL uses the information in the state file to maintain the existing packaging assignments. If you do not want to use the existing packaging assignments, set the `REPACKAGE` directive to `on`. For more information about the `REPACKAGE` directive, see the Cadence document *Packager-XL Reference.*

The `STATE_WINS_OVER_DESIGN` and `STATE_WINS_OVER_LAYOUT` directives are used to control the precedence of properties in the schematic, layout, and state files. You can set these directives from the *State File* tab in the Packager Setup dialog box.

The `STATE_WINS_OVER_DESIGN` directive specifies whether or not the property values in the state file will replace the schematic values. The default value is `off`. This value specifies that the schematic property values take precedence over the values in the state file. To preserve the changes made during the layout phase, you must complete one of the following tasks:

- Backannotate your schematic after running Packager-XL in the Feedback mode
- Set the `STATE_WINS_OVER_DESIGN` directive to `on`

**Note:** It is recommended that you backannotate your design after packaging in the Feedback mode and let the `STATE_WINS_OVER_DESIGN` directive remain `off`.

If you want the feedback values in the state file to replace any values in the schematic, set the `STATE_WINS_OVER_DESIGN` directive to `on`. This setting preserves the property values fed back from the layout. Consequently, the schematic does not display the values used by Packager-XL and any changes to the packaging properties in the schematic are ignored.

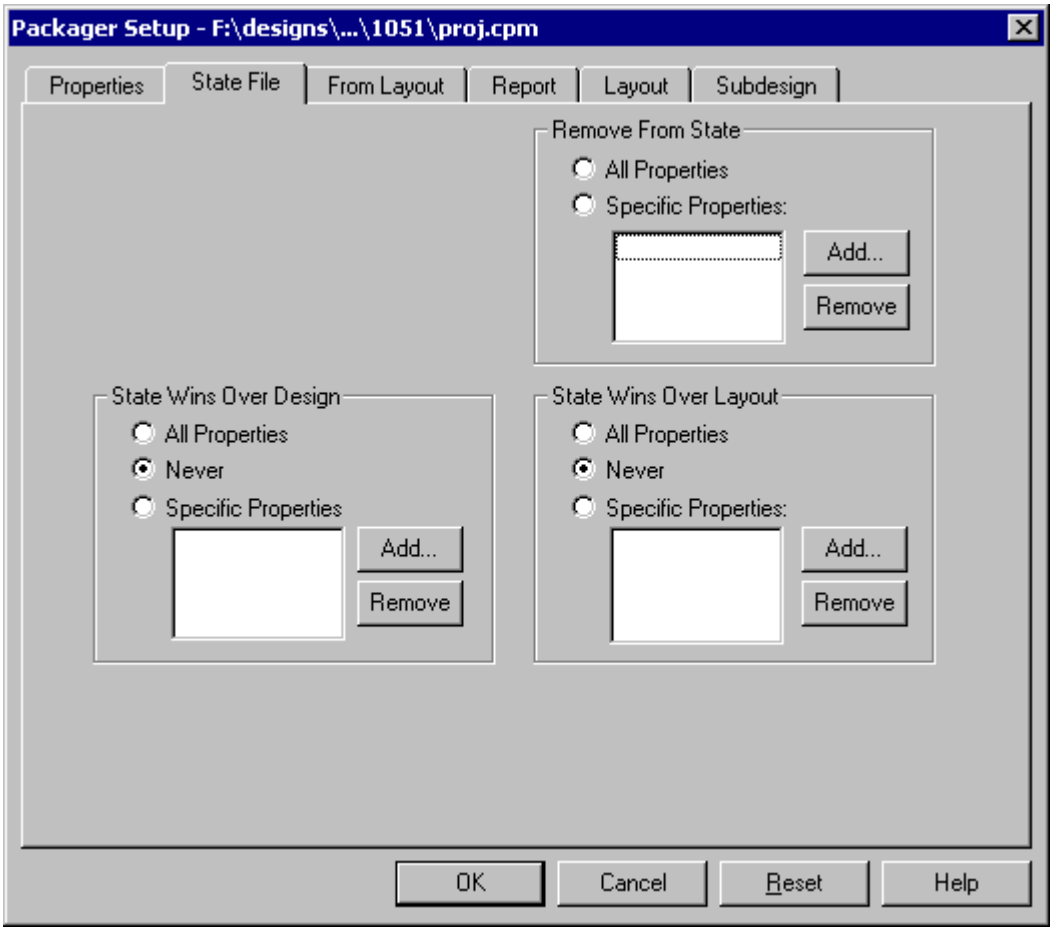
The `STATE_WINS_OVER_LAYOUT` directive specifies whether or not the property values in the state file will replace the feedback values (that is, the changes made in the layout). The default value is `off`. This specifies that the feedback values take precedence over the values in the state file.

**Note:** By setting the `STATE_WINS_OVER_LAYOUT` directive to `on`, you force the packaging changes to originate in the schematic. The property values in the state file will not replace the property values in the schematic. The value `on` for the `STATE_WINS_OVER_LAYOUT` directive might prove too restrictive. It is recommended that you let the `STATE_WINS_OVER_LAYOUT` directive remain `off`.

## Changing the State File

To change the packaging information in the state file, select the *State File* tab.

**Figure 2-4 Packager Setup - State File Tab**




You can use the *State File* tab to make the following changes:

1. Change the properties in the state file.

You can use the *Remove From State* group box to remove properties from the state file. Packager-XL cannot reuse existing packaging information for the properties that are removed from the state file. Therefore, you must be cautious while removing properties from the state file.

If you want to remove all the properties from the state file, click the *All Properties* radio button.

To remove specific properties from the state file, select the *Specific Properties* radio button and remove properties. See Adding and Deleting Properties for more information about adding or removing properties from the *Remove From State* list box.

**Note:** The `REMOVE_FROM_STATE` directive is used to remove properties from the state file. For more information about the `REMOVE_FROM_STATE` directive, see the Cadence document *Packager-XL Reference.*

2. Define the properties in the state file that replace the properties in the design.

   By default, the properties in the schematic always replace the properties in the state file. However, you can define the properties in the state file that will replace similar properties in the schematic. If you want to make all properties in the state file, replace the properties in the schematic, and select the *All Properties* radio button.

   To make specific properties in the state file replace the schematic properties, select the *Specific Properties* radio button and add or remove properties. See Adding and Deleting Properties for more information about adding or removing properties from the *State Wins Over Design* list box in the Packager Setup dialog box.

   To revert to the default selection, where the schematic properties will always replace the state file properties, select the *Never* radio button.

3. Define the properties in the state file that replace the properties in the layout

   By default, the properties in the state file never replace the feedback values in the layout. However, you can define the properties in the state file that replace the properties in the layout. If you want to make all properties in the state file, replace the properties in the layout, and select the *All Properties* radio button. This is the default selection.

   To make a specific property in the layout replace its value in the state file, select the *Specific Properties* radio button and add or remove properties. The properties added in the *State Wins Over Design* list box always replace the feedback values in the layout.

   To revert to the default selection, that is, that the schematic properties will always replace the state file properties, select the *Never* radio button.

After you have added or removed properties, check if you need to change any other setup options in the other five tabs. To change information in another tab, select the tab and make the required changes. Click the *OK* button to accept the changes, or click the *Cancel* button to ignore the changes.

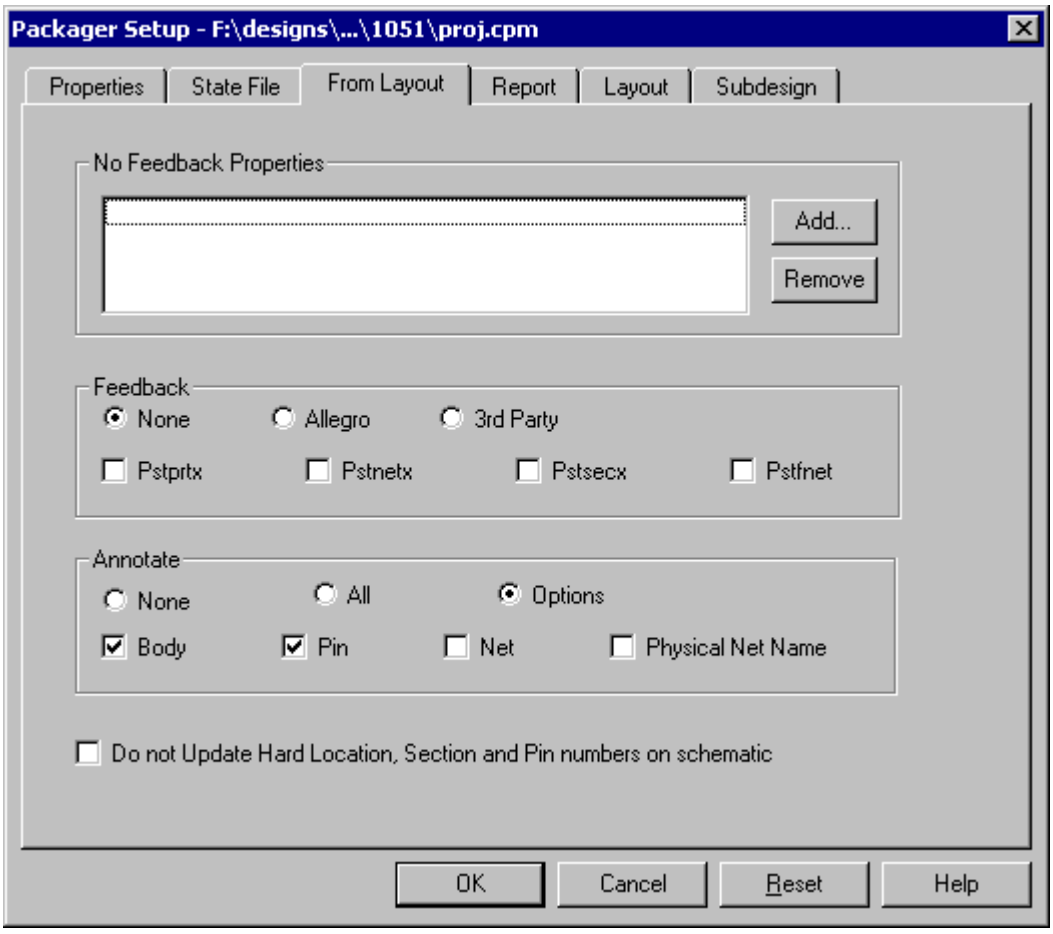
If you have made any property changes in the current session but want to revert to the default properties, click the *Reset* button.

**Note:** For more information about the STATE_WINS_OVER_DESIGN and STATE_WINS_OVER_LAYOUT directives, see the Cadence document *Packager-XL Reference.*

# Changing Feedback Properties in the Layout

To change the feedback properties in Packager Setup, select the *From Layout* tab. For more information, see Packager Setup - From Layout Tab on page 46.

**Figure 2-5 Packager Setup - From Layout Tab**




You can use the *From Layout* tab to make the following changes:

1. Define the feedback properties.

   By default, the feedback properties replace the corresponding properties in the schematic. You can, however, specify that certain feedback properties will not replace the properties in the schematic. To specify that a feedback property will not replace the schematic property, add that property in the *No Feedback Properties* list box. To add or remove properties from the *No Feedback Properties* list box, refer to Adding and Deleting Properties.

   Click *Remove* in the *No Feedback Properties* list box to delete any property from it. A property removed from the *No Feedback Properties* list box is fed back to the schematic.

   **Note:** The `NO_FEEDBACK` directive is used to prevent feeding back properties to the

schematic. For more information about the NO FEEDBACK directive, see the Cadence document *Packager-XL Reference.*

2. Run Packager-XL in the Feedback mode.

   By default, the *None* radio button is selected, signifying that Packager-XL will run only in the Forward mode.

   To run Packager-XL in the Feedback mode, click either the *PCB Editor* radio button or the *3rd Party* radio button to specify the source of the feedback files.

   If you want feedback from a third party feedback file, select the appropriate feedback file by clicking the check box to its left. You can specify one of the four check boxes:

   - *Pstprtx*—Feeds back physical reference designator transformation
   - *Pstnetx*—Feeds back physical net name transformation
   - *Pstsecx*—Feeds back physical reference designator transformation
   - *Pstfnet*—Feeds back connectivity changes for RefDes pin numbers

   **Note:** The FEEDBACK directive is used to run Packager-XL in the Feedback mode. For more information about the FEEDBACK directive, see the Cadence document *Packager-XL Reference.*

3. Annotate properties.

   You can define the objects in the design that must be backannotated. You can select body, pin, net, or physical net name for backannotation. To select any object for backannotation, click the respective check boxes under the *Options* radio button.

   To select all objects, click the *All* radio button.

   If you do not want to specify any object for backannotation, select the *None* radio button. The properties that are not backannotated to the schematic are assigned the ANNOTATE directive. For more information about the ANNOTATE directive, see the Cadence document *Packager-XL Reference.*

4. Manage hard properties.

   You can manage the packaging of hard properties (user-defined properties) by selecting the *Do not Update Hard Location, Section and Pin numbers on schematic* check box.

   By default, Packager-XL updates only soft properties in the Feedback mode. By selecting the *Do not Update Hard Location, Section and Pin numbers on schematic* check box, you can update hard properties.

> **Note:** The HARD_LOC_SEC directive is used to control the backannotation of hard properties. For more information about the HARD_LOC_SEC directive, see the Cadence document *Packager-XL Reference.*

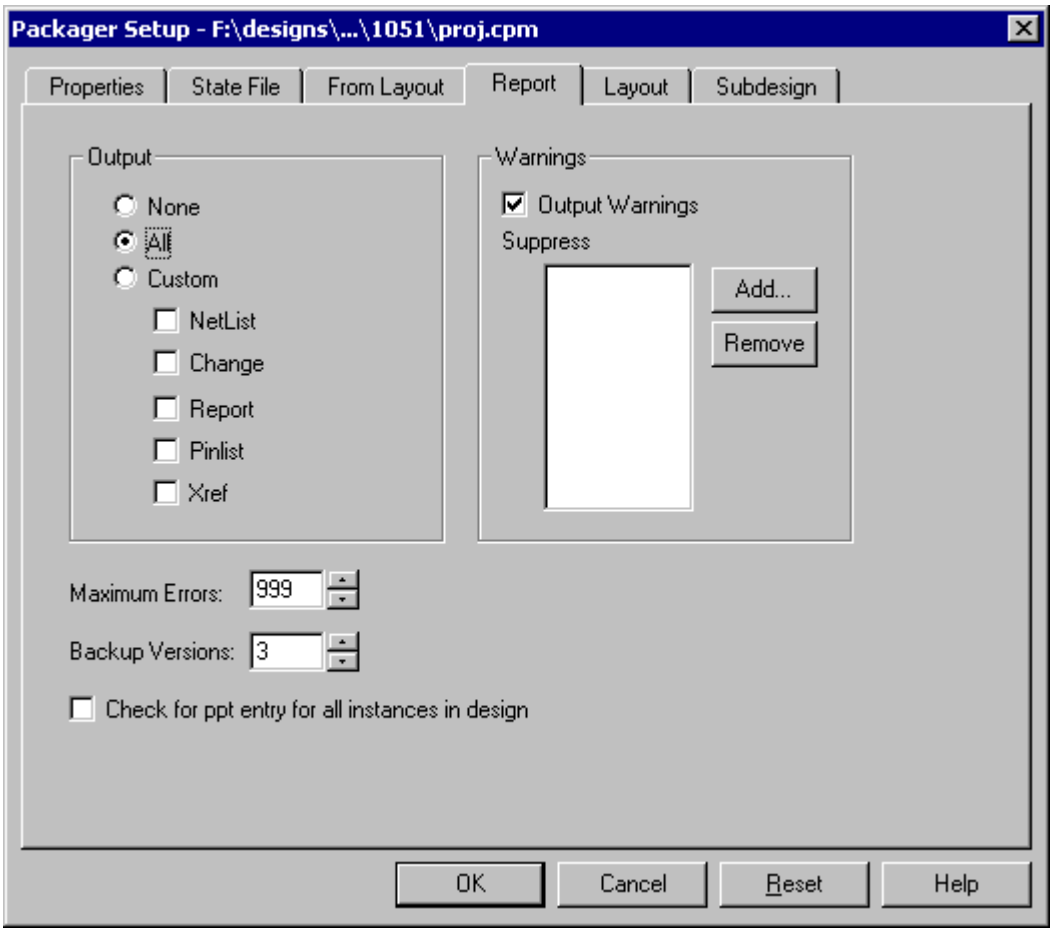
After you have added or removed properties, check if you need to change any other setup options in the other five tabs. To change information in another tab, select the tab and make the required changes. Click the *OK* button to accept the changes, or click the *Cancel* button to ignore the changes.

If you have made any property changes in the current session and want to ignore these changes, click the *Reset* button.

# Changing Packager Output Information

To change the output files that Packager-XL generates or to suppress warning messages, select the *Report* tab (See Figure 2-6 on page 49).

**Figure 2-6 Packager Setup - Report Tab**




You can use the *Report* tab to make the following changes:

1. Define the Packager-XL output files.

   By default, Packager-XL generates the following output files: netlist files (`pstchip.dat`, `pstxnet.dat`, and `pstxprt.dat`), a change file (`pxl.chg`), a report file (`pstrpt.dat`), a pinlist file (`pstpin.dat`), and an Xref file (`pstxref.dat`). For more information about Packager-XL output files, refer to Forward Mode on page 74.

   If you do not want Packager-XL to generate any output file, select the *None* radio button.

   To customize the Packager-XL output files, select the *Custom* radio button and click any of the following check boxes:

   - *NetList* check box—Select this check box to generate the netlist files.

- *Change* check box—Select this check box to generate the `pxl.chg` file, which documents the packaging changes between two packager runs.
- *Report* check box—Select this check box to generate the `pstrpt.dat` file, which provides a component summary and spares list.
- *Pinlist* check box—Select this check box to generate the `pstpin.dat` file, which contains a design-specific pin list.
- *Xref* check box - Select this check box to generate the `pstxref.dat` file, which contains information about cross-references between all logical-to-physical assignments, net names, and components.

**Note:** The `OUTPUT` directive specifies the output files generated by Packager-XL. For more information about the `OUTPUT` directive, see the Cadence document *Packager-XL Reference*.

**2.** Suppress warnings.

By default, Packager-XL generates all output warnings and stores them in the `pxl.log` file. You can suppress warnings. To suppress any warning, add the warning number corresponding to that warning in the *Suppress* list box, which is a part of the Add Suppressed Warnings dialog box.

To display the Add Suppressed Warnings dialog box, select the *Add* button in the Packager Setup dialog box. In the Add Suppressed Warnings dialog box, you can suppress any warning by adding its warning number in the *Warning Number* field and clicking *OK*.

**Note:** The `SUPPRESS` directive is used to suppress specific warning messages. For more information about the `SUPPRESS` directive, see the Cadence document Packager-XL Reference.

**3.** Define the maximum number of errors.

To change the maximum number of permissible errors that Packager-XL records before terminating an operation, change the number in the *Maximum Errors* field. The default value is `999`.

**Note:** The `MAX_ERRORS` directive is used to specify the maximum numbers of errors allowed before Packager-XL terminates an operation. For more information about the `MAX ERRORS` directive, see the Cadence document *Packager-XL Reference*.

**4.** Define the number of backup versions.

You can use the *Backup Versions* field to define the number of backup (pst) files that Packager-XL will maintain. The default value is three.

**Note:** The NUM_OLD_VERSIONS directive is used to define the number of backup (pst) files that Packager-XL will maintain. For more information about the NUM_OLD_VERSIONS directive, see the Cadence document *Packager-XL Reference*.

5. Verify that a logical part is assigned to every instance in the design.

   You can select the *Check for ppt entry for all instances in design* check box to ensure that ppt entries exist for all instances in the design. If an instance does not have a ppt entry or if the corresponding ptf files are not present, a warning is generated. This warning is recorded in the `pxl.log` file.

After you have added or removed properties, check if you need to change any other setup options in the other five tabs. To change information in another tab, select the tab and make the required changes. Click the *OK* button to accept the changes, or click the *Cancel* button to ignore the changes.

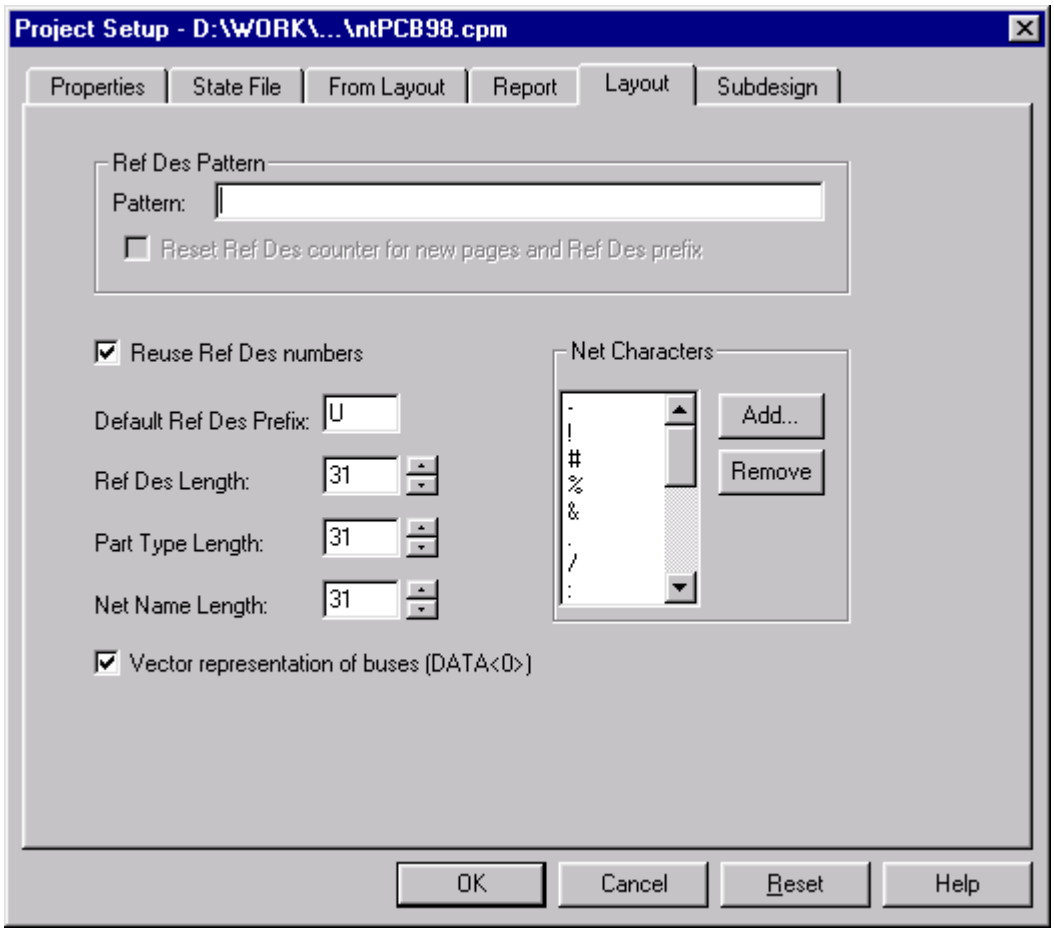
If you have made any property changes in the current session and want to ignore these changes, click the *Reset* button.

# Changing Reference Designators and Netlist Parameters


***Exercise caution when changing the default-naming scheme for reference designators. To apply a new pattern to the existing reference designators, you must repackage the design.***

To change reference designators and netlist parameters, select the *Layout* tab. See Packager Setup - Layout Tab on page 52.

**Figure 2-7 Packager Setup - Layout Tab**




You use the *Layout* tab to make the following changes:

1. Change the reference designator.

   By default, Packager-XL assigns a default reference designator that has two parts, the base name as defined by the `PHYS_DES_PREFIX` property, and a number that is appended by Packager-XL. If you need to specify a reference designator that is different from the default, specify its value in the *Ref Des Pattern* field.

   **Note:** The `REF_DES_PATTERN` directive is used to specify the format of reference designators assigned to the physical parts in the design. See the Cadence document *Packager-XL Reference* for more information about the `REF DES PATTERN` directive.

   If you want to reset the Ref Des counter for new pages and different Ref Des prefixes, select the *Reset Ref Des counter for new pages and Ref Des prefix* check box.

2. Specify that you want to reuse reference designator numbers.

By default, the *Reuse Ref Des numbers* check box is selected signifying that Packager-XL can use the reference designators of changed or deleted components in the schematic or the board for new components. If you do not want to reuse existing reference designators, clear the *Reuse Ref Des numbers* check box.

**Note:** The REUSE_REFDES directive is used to control the reuse of reference designators in a project. For more information about the REUSE_REFDES directive, see the Cadence document *Packager-XL Reference.*

3. Change the default reference designator prefix.

   By default, Packager-XL uses U as the reference designator prefix. If you have a PHYS_DES_PREFIX property that is different from U, type its value in the *Default Ref Des Prefix* field.

4. Change the default reference designator length.

   By default, Packager-XL uses a maximum of 31 characters for defining reference designators. If you want to change the default length, enter a number for the new length in the *Ref Des Length* field.

   **Note:** The REF_DES_LENGTH directive is used to control the maximum length of the physical reference designators generated by Packager-XL. For more information about the REF_DES_LENGTH directive, see the Cadence document *Packager-XL Reference*.

5. Change the default part type length.

   By default, Packager-XL uses a maximum length of 31 characters for defining component names. If you want to change the default length, enter a number for the new default length in the *Part Type Length* field.

   **Note:** The PART_TYPE_LENGTH directive is used to control the maximum length of the synthesized part names generated by Packager-XL. For more information about the PART_TYPE_LENGTH directive, see the Cadence document *Packager-XL Reference*.

6. Change the default net name length.

   By default, Packager-XL uses a maximum length of 31 characters for defining net names. If you want to change the default length, enter a number for the new default length in the *Net Name Length* field.

   **Note:** When you change the default value, the new value does not become effective automatically. You must repackage the design for the new value to become effective.

   **Note:** The NET_NAME_LENGTH directive is used to control the maximum length of the physical net names generated by Packager-XL. For more information about the NET_NAME_LENGTH directive, see the Cadence document *Packager-XL Reference*.

7. Define the list of characters that will be included in net names.

   You can change the list of characters that will be included when defining net names. To add a new character, click the *Add* button. This will display the Add Net Characters dialog box where you can add a character. To remove any character, select it in the *Net Characters* list and click *Remove*.

   **Note:** The NET_NAME_CHARS directive is used to specify special (non-alphanumeric) characters permitted in physical net names. For more information about the NET_NAME_CHARS directive, see the Cadence document *Packager-XL Reference*.

8. Specify whether buses will have vector representation.

   All buses are represented in vector form in the pstxnet file. You can change the representation to non vector (that is, avoid having bits within angular braces) by clearing the *Vector representation of buses (DATA <0>)* check box and later repackaging the design.

   **Note:** The USE_VECTOR_NOTATION directive specifies that individual bits for vector signals will always be saved within angular braces in the pstxnet.dat file. For more information about the USE VECTOR NOTATION directive, see the Cadence document *Packager-XL Reference*.

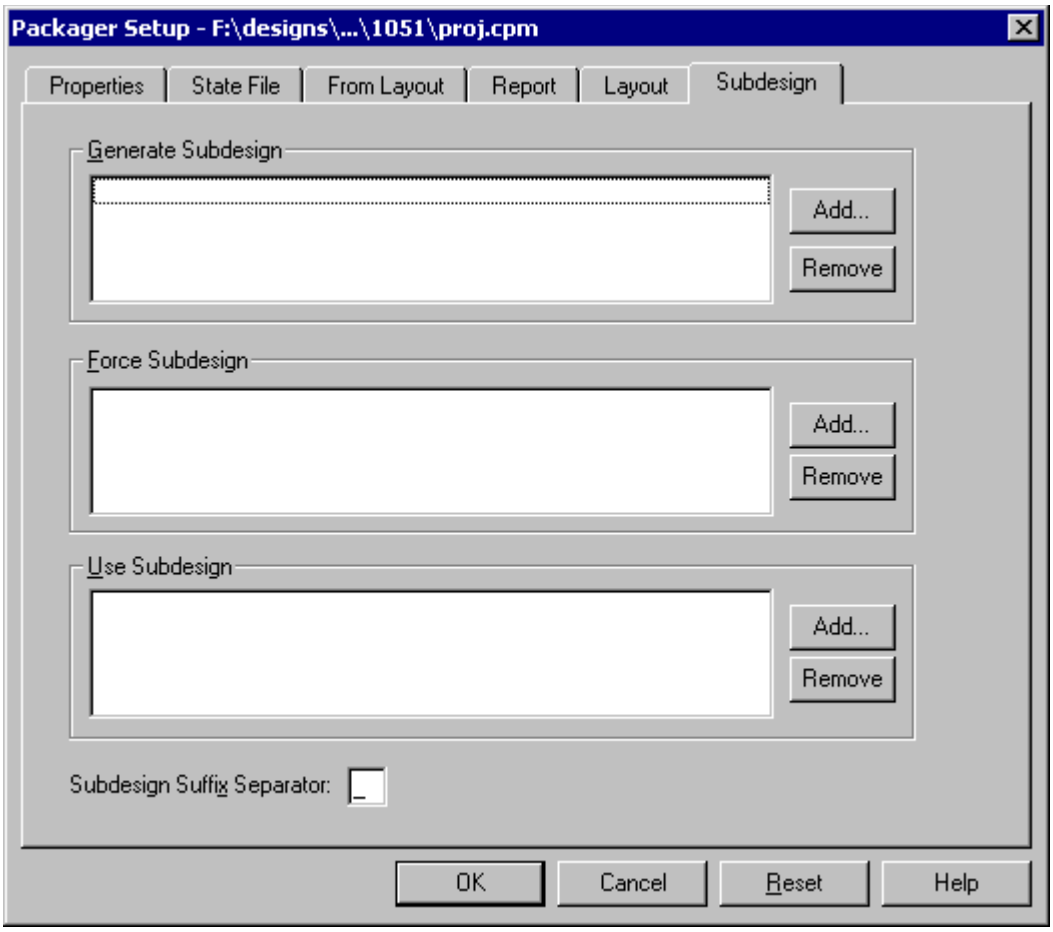
After you have added or removed properties, check if you need to change any other setup options in the other five tabs. To change information in another tab, select the tab and make the required changes. Click the *OK* button to accept the changes, or click the *Cancel* button to ignore the changes.

If you have made any property changes in the current session and want to ignore these changes, click the *Reset* button.

# Changing Setup Options While Packaging Subdesigns

To change the setup options while packaging subdesigns, select the *Subdesign* tab. See Packager Setup - Subdesign Tab on page 55.

**Figure 2-8 Packager Setup - Subdesign Tab**




You use the *Subdesign* tab to make the following changes:

1. Generate a subdesign state file.

   Subdesigns are pre-packaged blocks containing logic that can be reused in the context of larger designs. Using Packager-XL, you can save packaging assignments for a subdesign in a new file called the subdesign state file.

   To generate the subdesign state file, add the name of the design in the *Generate Subdesign* list box by using the *Add* button. When you click the *Add* button, the Add Subdesign dialog box appears. You can enter the name of the design and click the *OK* button to add the name of the design in the *Generate Subdesign* list box. The design names entered in this list box are used to prepare the subdesign state files.

   You can remove a subdesign from the *Generate Subdesign* list box. To remove the subdesign, select the design name and click the *Remove* button.

**Note:** The GEN_SUBDESIGN directive is used to specify the modules for which you want to generate subdesign state files.For more information about the GEN_SUBDESIGN directive, see the Cadence document *Packager-XL Reference*.

2. Force packaging in the subdesign.

   To apply the packaging in the subdesign state file to each instance of the subdesign, add the names of the design to the *Force Subdesign* list box.

   To add or remove design names from the *Force Subdesign* list box, use the *Add* or *Remove* buttons.

   **Note:** The FORCE_SUBDESIGN directive is used to apply the packaging in the subdesign state file to each instance of the subdesign. For more information about the FORCE_SUBDESIGN directive, see the Cadence document *Packager-XL Reference*.

3. Use subdesigns selectively.

   If you want to apply the packaging in the subdesign state file only to the new instances of the subdesign, add the name of the design to the *Use Subdesign* list box. This lets you change the subdesign packaging without affecting existing instances of the subdesign.

   To add or remove design names from the *Use Subdesign* list box, use the *Add* or *Remove* buttons.

   **Note:** The USE_SUBDESIGN directive is used to apply the packaging in the subdesign state file only to the new instances of the subdesign. For more information about the USE_SUBDESIGN directive, see the Cadence document *Packager-XL Reference*.

4. Define a different character for renaming reference designators for reuse modules.

   By default, the underscore (_) letter is used by Packager-XL to define the reference designator for reuse modules. If you want to define a different character for renaming reference designators for reuse modules, type that character in the *Subdesign Suffix Separator* field.

   **Note:** The SD_SUFFIX_SEPARATOR directive is used to define a different character for renaming reference designators for reuse modules. For more information about the SD_SUFFIX_SEPARATOR directive, see the Cadence document *Packager-XL Reference*.

After you have added or removed properties, check if you need to change any other setup options in the other 5 tabs. To change information in another tab, select that tab and make the required changes. Click the *OK* button to accept the changes, or click the *Cancel* button to ignore the changes.

If you have made any property changes in the current session and want to ignore these changes, click the *Reset* button.

# 3

# PCB Editor-Design Entry Property Flow

## Overview

To synchronize the property changes between the schematic prepared in Design Entry HDL and the board generated in PCB Editor, use the Visual Design Differences (VDD) tool. VDD compares the schematic and the board and lists all property differences between them. You can synchronize a schematic and a board by accepting the property differences in the board.

However, resolving the property differences between the schematic and the board might be difficult because VDD displays a large number of property differences. Most of these differences are caused because of the inability of VDD to recognize whether or not the following are true:

1. A property is Design Entry-only. This property belongs only to the schematic and should not be transferred to the board.
2. A property is PCB Editor-only. This property belongs only to the board and should not be backannotated to the schematic.
3. A property originated from Design Entry HDL but was deleted in PCB Editor.

You can use the Property Flow Setup dialog box to define the properties that will flow between PCB Editor and Design Entry HDL.

**Note:** See the Cadence document PCB Systems Properties Reference for more information about different properties.

## PCB Editor-Design Entry Property Flow Use Model

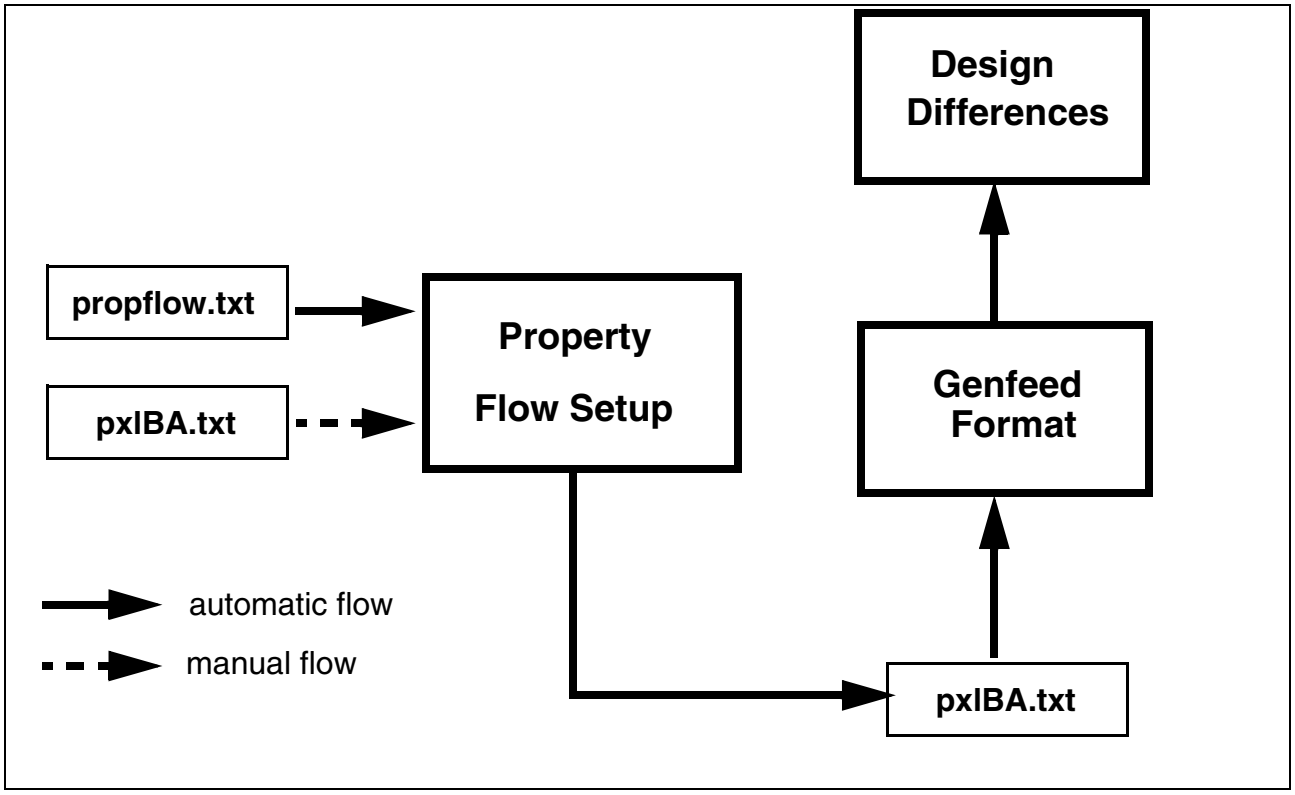
Before you package the design, select all properties that will be transferred between PCB Editor and Design Entry HDL by using the Property Flow Setup dialog box.

The Property Flow Setup dialog box provides an easy way to update the `pxlBA.txt` file. This file contains information about which properties can be transferred from PCB Editor to Design Entry HDL.

# Properties Flow from PCB Editor to Design Entry HDL

The properties flow from PCB Editor to Design Entry HDL is summarized in the following figure:

**Figure 3-1 Property Flow**




The inputs to the Property Flow Setup dialog box are:

1. The Cadence default `propflow.txt` file—This file defines the default properties that flow between PCB Editor and Design Entry HDL.
2. `pxlBA.txt` file—The `pxlBA.txt` file is used to define the properties that are backannotated to Design Entry HDL. This file is located in the physical view of the root design.

   **Note:** Property Flow Setup does not automatically pick all properties from the `pxlBA.txt` file. If you have customized the `pxlBA.txt` file from a previous release, then use the information contained in it to populate the Property Flow Setup dialog box.

The Property Flow Setup dialog box accepts the above inputs and allows you to modify the existing properties and add new properties. When you save the changes in the Property Flow Setup dialog box, the `pxlBA.txt` file is updated. This file is used by VDD and Genfeedformat to determine the default properties that flow between PCB Editor and Design Entry HDL.

# Opening the Property Flow Setup Dialog Box

1. Display the Export Physical dialog box.

   To display the Export Physical dialog box,

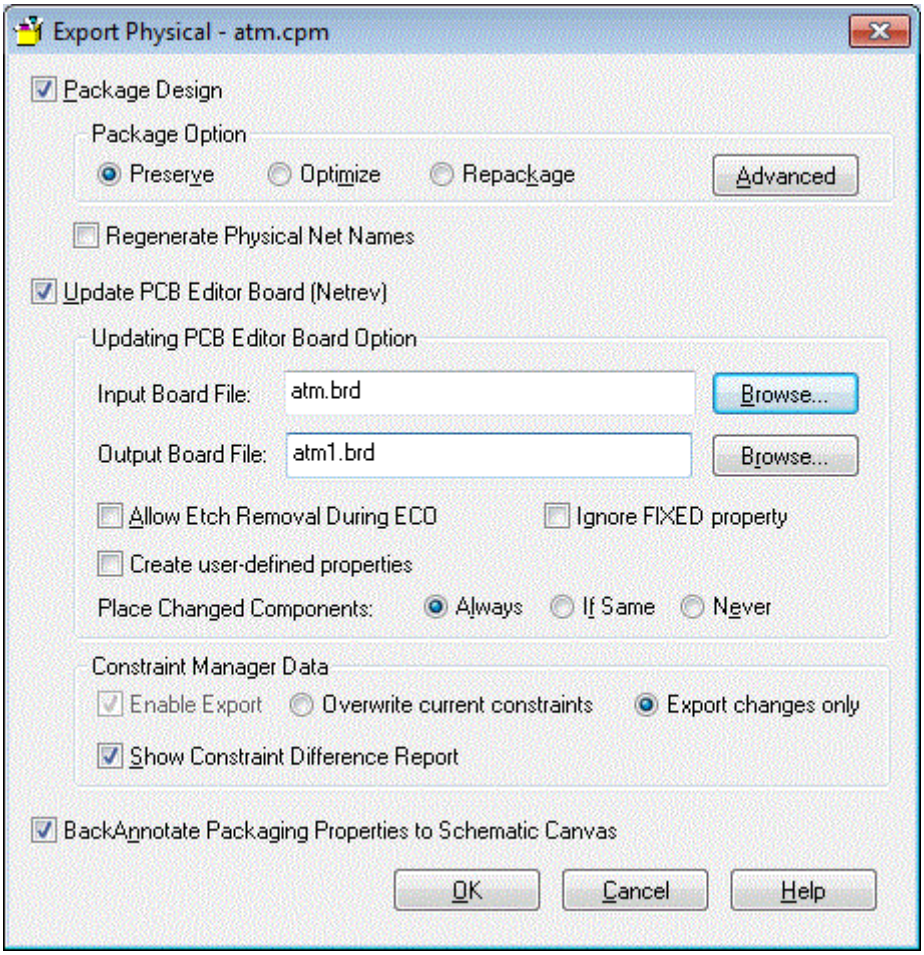
   - Choose *Export Physical* from the *File* menu in Design Entry HDL.

*Tip*

   - Click the *Design Sync* icon in Project Manager, and click the *Export Physical* option.

   The Export Physical dialog box appears.

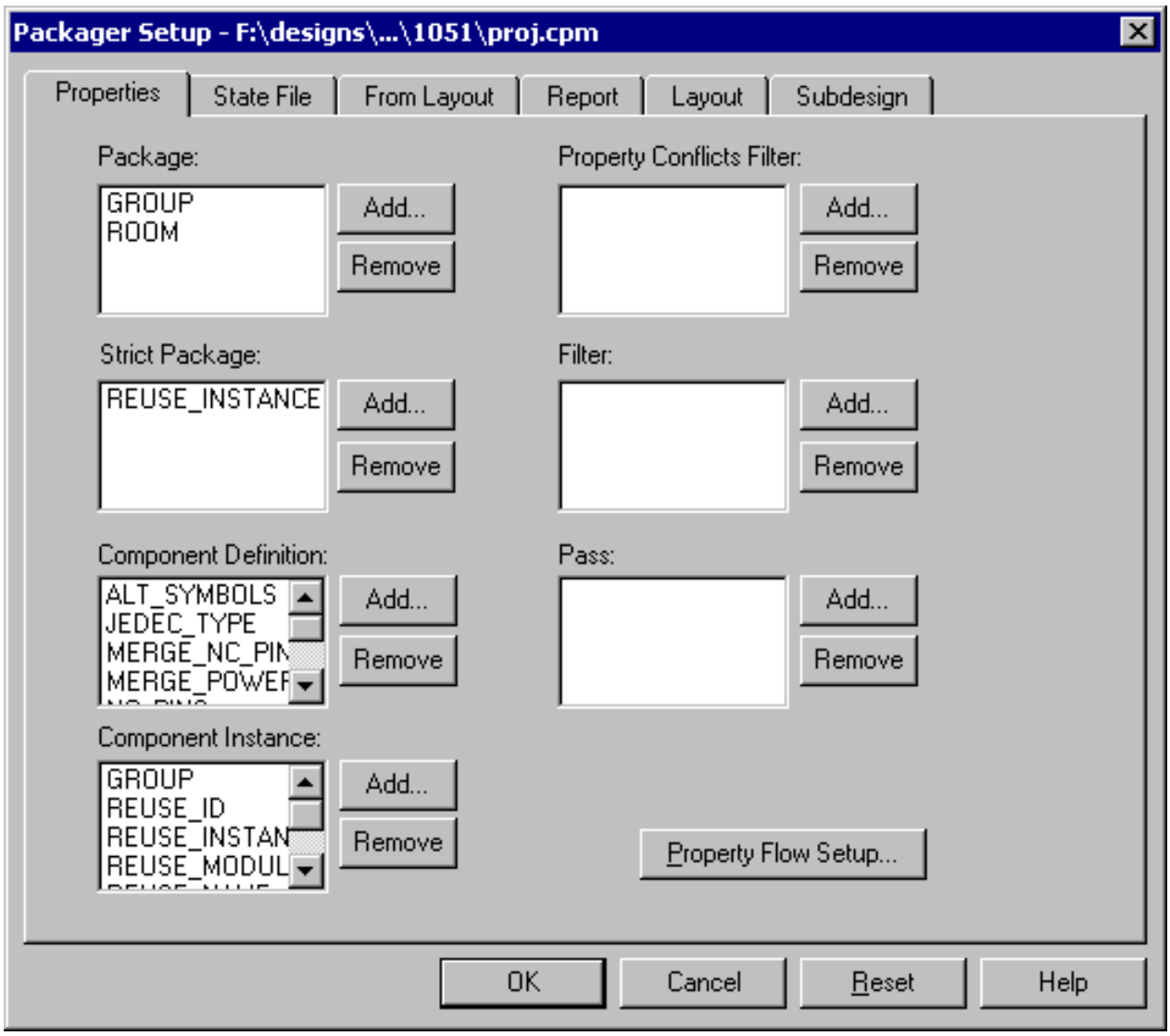
**Figure 3-2 Export Physical Dialog Box**




2. Click the *Advanced* button.

   The Packager Setup dialog box appears.

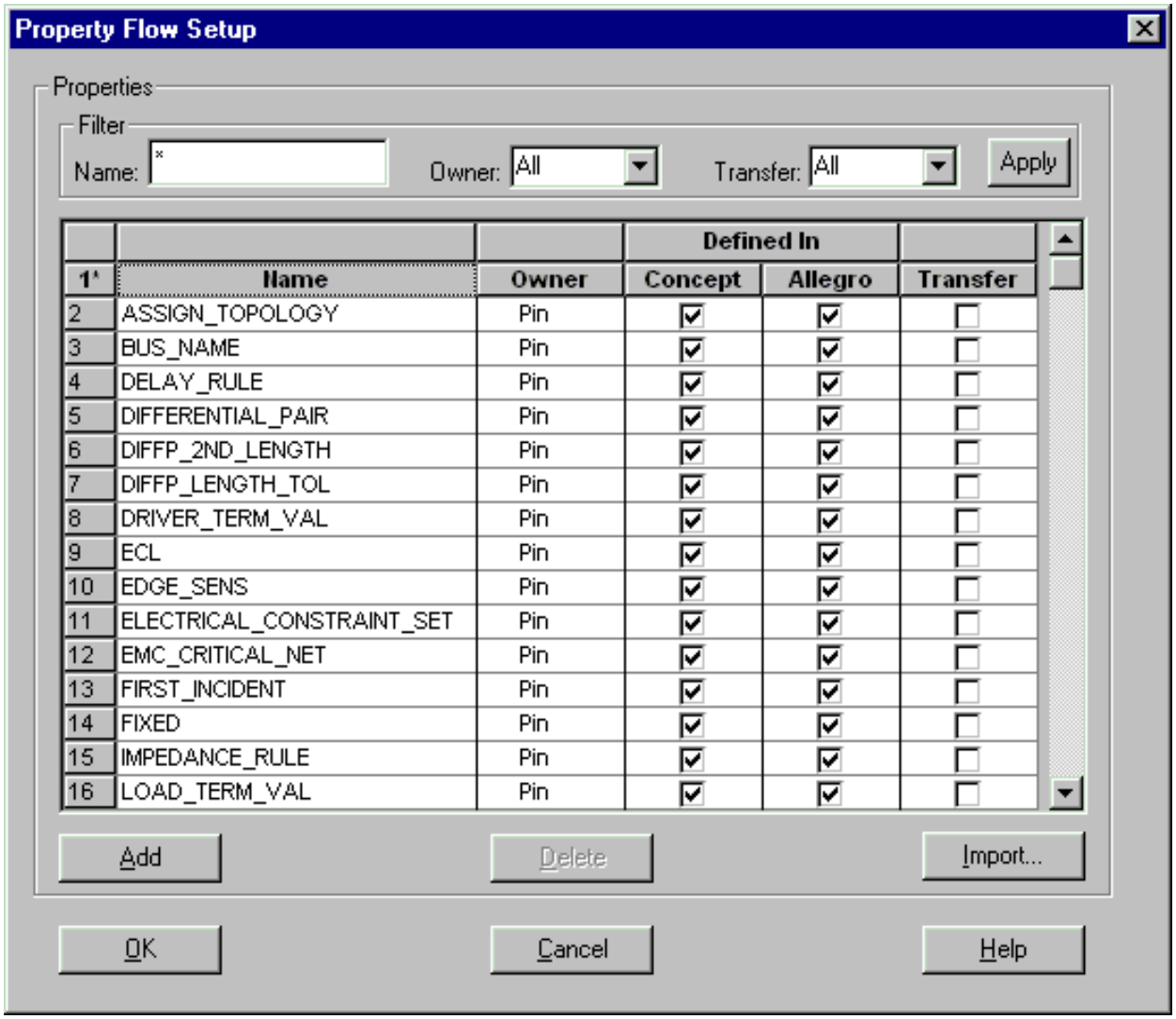
**Figure 3-3 Packager Setup Dialog Box**




3. Click the *Property Flow Setup* button.

   The Property Flow Setup dialog box appears.

**Figure 3-4 Property Flow Setup Dialog Box**




**Note:** You can also launch the Property Flow Setup dialog box from VDD by choosing the *Property Flow Setup* option from the *Difference* menu.

**Note:** The use of the Property Flow Setup dialog box does not change the front-to-back flow. For more information about the front-to-back flow, see Front-to-back Flow on page 21.

# Setting the Property Flow

To set the property flow, you need to include and exclude properties in the Property Flow Setup dialog box. By default, the Property Flow Setup dialog box picks the properties from the `propflow.txt` file (`<your_inst_dir>/share/cdssetup/propflow.txt`).

These properties are displayed in a grid box with five columns representing the property name, the object to which these properties are attached, information about whether properties are defined in PCB Editor or Design Entry HDL, and whether each property will be transferred from PCB Editor to Design Entry HDL along with the netlist.

You can change the default properties in one of the following four ways:

1. Add a new property.
2. Delete an existing property.
3. Edit the values for a property.
4. Import properties from another file (`pxlBA.txt` or `pst*.dat` files).

## Adding New Properties

1. Click at the number to the left of the property name after which the new property is to be created.
2. Click the *Add* button.

   A new property row is created. The *Property* name is blank. The *Owner* field is filled based on the object to which the property is attached. The *Defined In* check boxes are selected for both Design Entry HDL and PCB Editor. The *Transfer* check box is grayed out.

   **Note:** You can define a new name for the property.
3. To change the owner, select the *Owner* field for the new property.
4. A list button appears. Click the list button and click one of the four options: *Comp*, *Pin*, *Function*, and *Net*.

   **Note:** If you need to add a property as a `Comp` property, add the property in the list of properties defined by the `COMP_INST_PROP` directive.
5. If the new property is not defined in Design Entry HDL or PCB Editor, clear the check box corresponding to *Design Entry* or *PCB Editor* in the *Defined In* fields.
6. If the property can be transferred from PCB Editor to Design Entry HDL along with the netlist, select the *Transfer* check box.
7. To accept the property changes and close the Property Flow Setup dialog box, click the *OK* button. To ignore the property changes and close the Property Flow Setup dialog box, click the *Cancel* button.

## Deleting Properties

1. To delete a property, select the property by clicking the number to the left of the property name.
2. Click the *Delete* button.
3. To accept the property changes and close the Property Flow Setup dialog box, click the *OK* button. To ignore the property changes and close the Property Flow Setup dialog box, click the *Cancel* button.

## Editing Properties

1. To edit a property name, select the property name by triple-clicking in the *Property* field and type the new name.

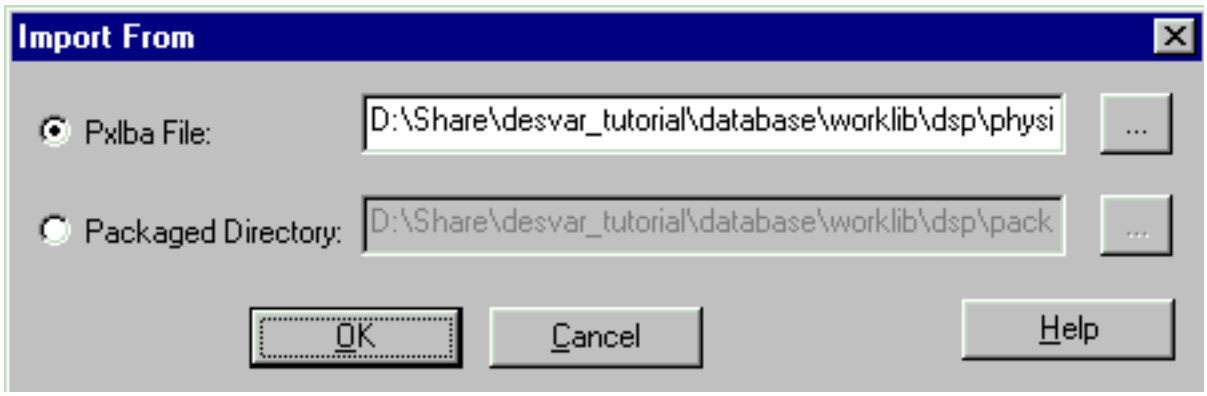
   **Note:** Editing a property name is rarely required. Unless you have made a spelling error while defining the property name, avoid editing the property name.
2. To change the owner of the property, select the new option in the *Owner* field.
3. To set the property as defined in Design Entry HDL or PCB Editor, select or clear the check box corresponding to *Design Entry* or *PCB Editor* in the *Defined In* fields.
4. To define a property as transferable, select the *Defined In Design Entry* and *Defined In PCB Editor* property. Next, select the *Transfer* check box.
5. To accept the property changes and close the Property Flow Setup dialog box, click the *OK* button. To ignore the property changes and close the Property Flow Setup dialog box, click the *Cancel* button.

## Importing Properties

1. To import properties from the `pxlBA.txt` file or the `pst*.dat` files, click the *Import* button.

   The Import From dialog box appears. The *Pxlba File* radio button is selected by default.

**Figure 3-5 Import From Dialog Box**




2. The `pxlBA.txt` file for the project (located in the `physical` view under the root design) appears selected in the *Pxlba File* field. To change the path of the `pxlBA.txt` file, click the browse button and select the new file.

3. To import the properties from the `packaged` directory, select the *Packaged Directory* radio button. The *Packaged Directory* field displays the path to the `packaged` directory of the root design. You can change this path by using the browse button.

4. To accept the property changes and close the Property Flow Setup dialog box, click the *OK* button. To ignore the property changes and close the Property Flow Setup dialog box, click the *Cancel* button.

   If you click *OK,* the Import From dialog box closes and a new set of properties is added to the property list in the Property Flow Setup dialog box.

### How properties from the pxlBA.txt file are seeded in the Property Flow Setup dialog box

Packager-XL reads all properties defined in the `pxlBA.txt` file. For each property definition that does not exist in the Property Flow Setup dialog box, Packager-XL creates a new row with the following attributes:

- The property name is filled in the *Name* field.
- The owner field shows the owner type specified in the `pxlBA.txt` file.
- The *Design Entry* and *PCB Editor* check boxes are selected.
- The *Transfer* check box is selected signifying that the property will be transferred from PCB Editor to Design Entry HDL.

If the property name already appears in the Property Flow Setup dialog box and the owner type is the same as in the `pxlBA.txt` file, the following check boxes for the property are selected:

- *Design Entry*
- *PCB Editor*
- *Transfer*

If the property name already exists in the Property Flow Setup dialog box and the owner type is different from that in the `pxlBA.txt` file, a new row is added to the dialog box with property values same as those for a new property.

### How properties from Packager files are seeded in the Property Flow Setup dialog box

All properties defined in the Packager (`pst*.dat`) files are read by the Property Flow Setup dialog box. A predefined list of properties that are used by Cadence tools is filtered out. To view the list of properties filtered using the Property Flow Setup dialog box, refer to the List of Properties Filtered from Packager Files. For each property definition that does not exist in the Property Flow Setup dialog box, a new row is created with the following attributes:

- The property name is filled in the *Name* field.
- The *Owner* field is filled based on the object to which the property is attached.
  - If the object is attached to a package, the owner defined is a component.
  - If the object is attached to an instance, the owner defined is a function.
  - If the object is attached to a pin, the owner defined is a pin.
  - If the object is attached to a net, the owner defined is a net.
- The *Design Entry* check box is selected.
- The *PCB Editor* check box is not selected.
- The *Transfer* check box is grayed out because the *PCB Editor* check box is not selected.

If the property name already exists in the Property Flow Setup dialog box and the owner type is the same as for the existing property, the *Defined In Design Entry* check box is selected for the row.

If the property name already exists in the Property Flow Setup dialog and the owner type is different in the `pst*.dat` files, the property is considered a new property. A new row is added to the dialog box with the property values being the same as those for the new property.

# 4

# Packaging Your Design

## Overview

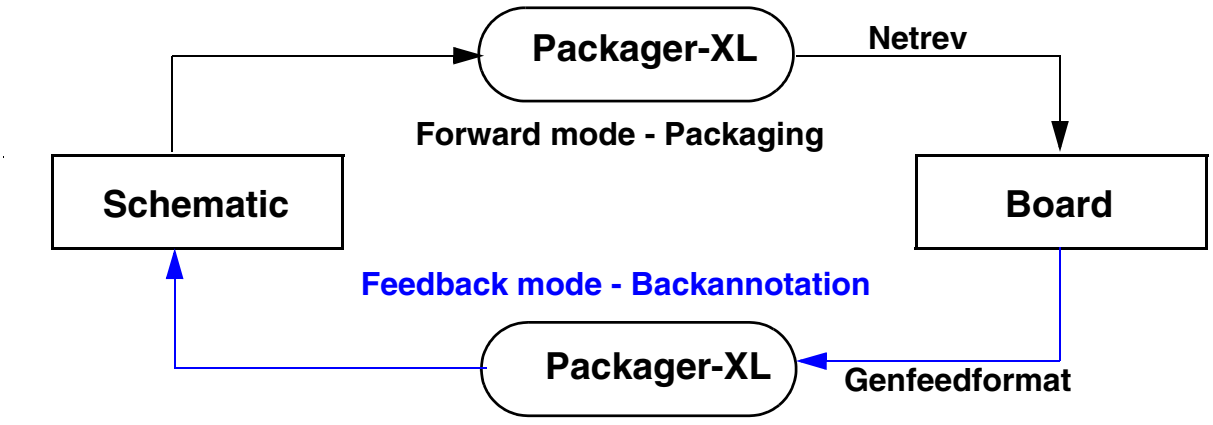
Packager-XL is the interface between the schematic and the board for the Cadence Board Design solution.

You can use this utility to do the following:

- Translate the schematic into a physical design
- Backannotate the changes made in the board to the schematic
- Update the changes made in the schematic after initial packaging to the board

**Note:** While the translation is done only once, backannotation and updating can be done multiple times to bring the schematic and the board in sync, that is, they have identical information.

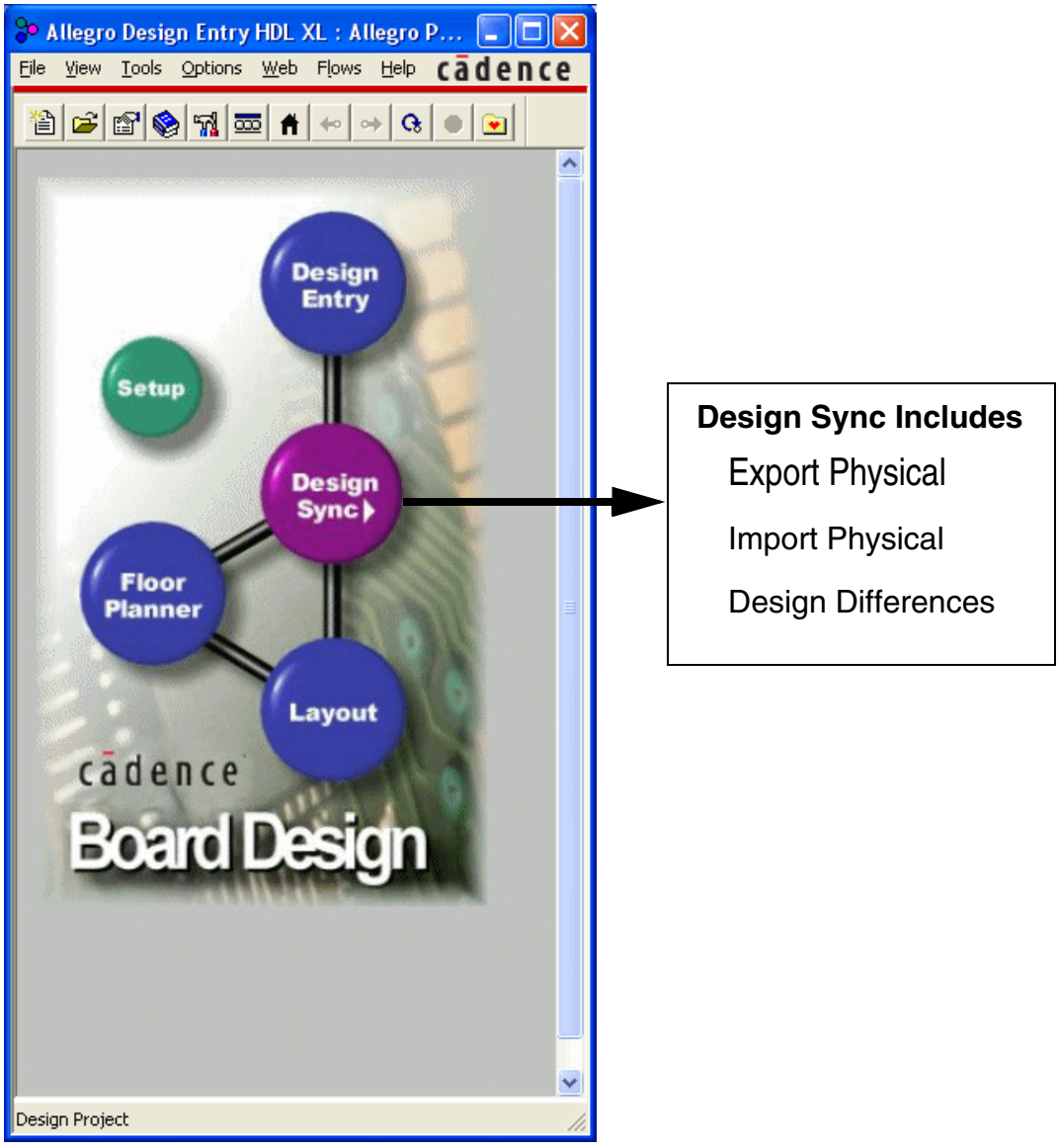
**Figure 4-1 Packager-XL and Synchronizing the Schematic and the Board**



# Where Packager-XL Fits in the PCB Design Process

Packager-XL forms the middle layer of the PCB design process. It acts as a bridge between the design entry phase, which involves preparing the schematic, and the board creation phase, which involves creating the layout.

**Figure 4-2 Project Manager with the Board Design Flow**



# Packager-XL Operation Modes

Packager-XL works in the following two modes:

- Forward Mode

  In the Forward mode, Packager-XL translates a logical design entered in Design Entry HDL into a physical design ready for layout in PCB Editor. To run the Forward mode, you need to run the `Export Physical` command.

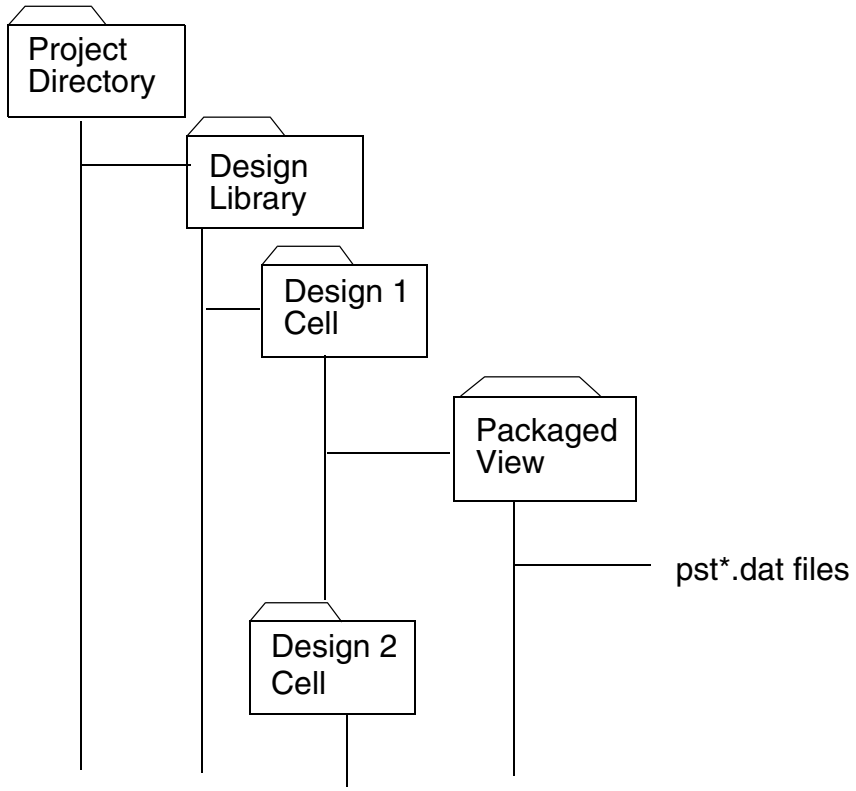
- Feedback Mode

  In the Feedback mode, Packager-XL receives changes made in PCB Editor and incorporates these changes into the logical design. To run the Feedback mode, you need to run the `Import Physical` command.

Packager-XL uses the standard Hardware Description Language (HDL) naming conventions to simplify intertool communication. The library structure used is based on the Library-Cell-View model and is common across all Cadence solutions.

After packaging a design, Packager-XL places HDL-based netlist files in a packaged view within the design cell view as shown in the HDL-Based Directory Structure figure on page 74.

**Figure 4-3 HDL-Based Directory Structure**



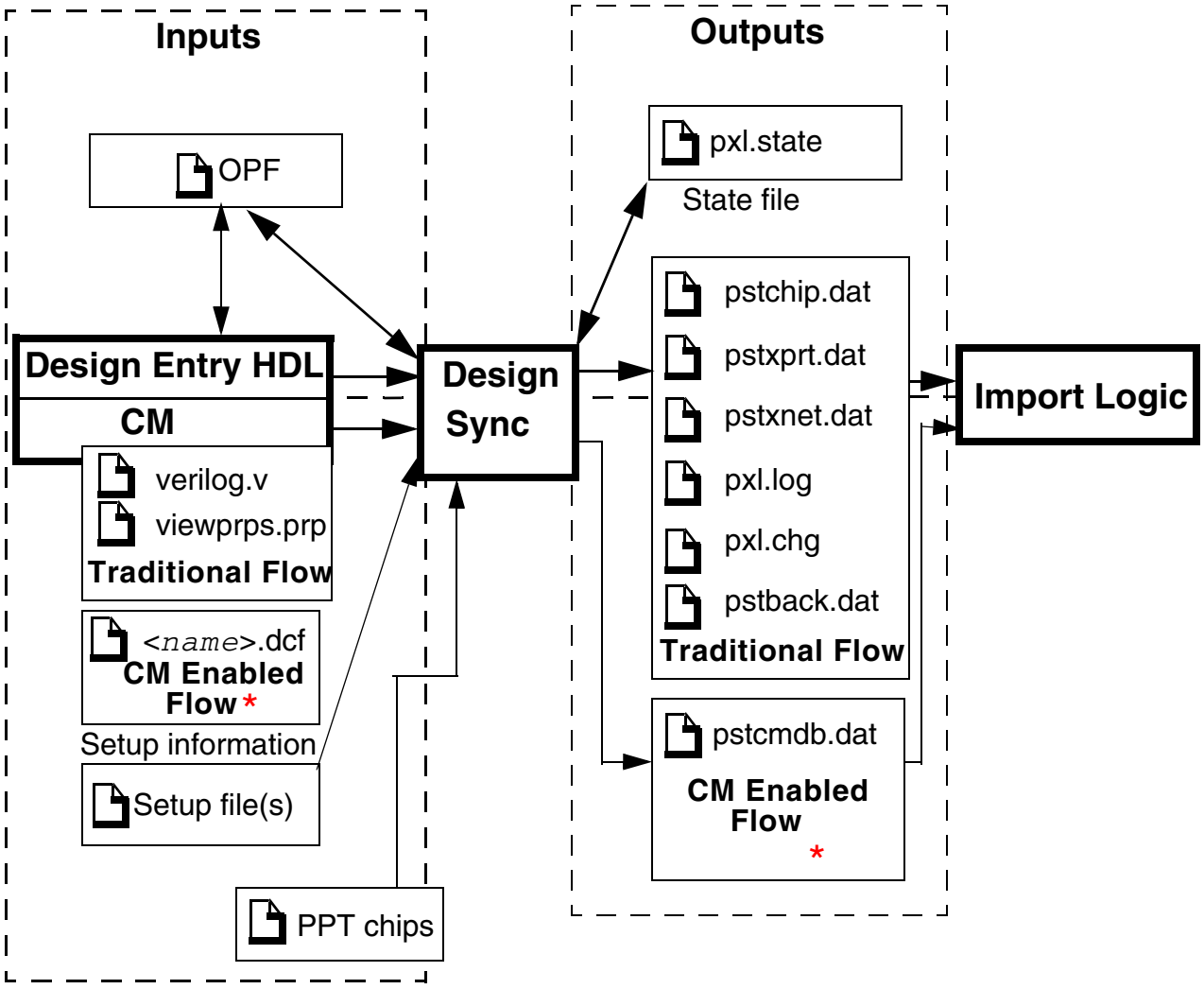

# Forward Mode

In the Forward mode, you enter a design in Design Entry HDL, and then run Packager-XL to translate the logical design into a physical design. This process is also known as packaging the design into physical parts. To incorporate incremental design changes into the existing physical design, you can use subsequent Packager-XL runs. To import the packaged design into the PCB Editor environment, you use the PCB Editor Import Logic program.

In the Constraint Manager-enabled flow, PCB Editor reads 3 or 5 pst*.dat files. In the traditional flow, PCB Editor reads `pstxprt.dat`, `pstxnet.dat`, and `pstchip.dat` netlist (output) files. In the Constraint Manager-enabled flow, PCB Editor reads `pstxprt.dat`, `pstxnet.dat`, `pstchip.dat`, and pstcmdb.dat files. Based on information contained in these files, PCB Editor produces or updates an PCB Editor layout file. See the Forward Mode of Operation figure on page 75 for details.

**Note:** See Front-to-back Flow on page 21 for and Front-to-back Flow on page 21 for more information about the different files used in the two design flows.

**Figure 4-4 Forward Mode of Operation**




* CM enabled flow includes all files in the traditional flow and some additional files as mentioned in the figure.

## Inputs in the Forward Mode

The inputs to Packager-XL during the Forward mode are as described below:

1. Setup information

   Packager-XL obtains its setup information from the project file (.cpm).

2. Design entered in Design Entry HDL

   A design saved in Design Entry HDL generates the `verilog.v`, `viewprps.prp`, and `SIR files.` The the `verilog.v` file contains connectivity information (information about the structure of the design). The `viewprps.prp` file contains information about all properties in the schematic. The SIR file contains information for EDB to create an expanded view of the design.

3. Electrical constraint file

   If you run Constraint Manager from Design Entry HDL, then it creates <*root_design*>.dcf file, which contains a snapshot of electrical constraint information in the design. This file is available in the `constraints` view under the root design. If this file is present, Packager-XL reads electrical constraint information from it will get filtered and Packager-XL will run in the Constraint Manager-enabled flow.

4. Library data

   Packager-XL uses the library chips files and Physical Part Tables (PPTs) to obtain the physical information for the schematic instances used in the design.

5. State file, `pxl.state`

   Packager-XL uses the state file as an input file to maintain the packaged design for subsequent runs of Packager-XL.

## Outputs From the Forward Mode

The outputs produced by Packager-XL in the Forward mode are as described below:

- `pxl.state`

  Packager-XL uses the state file to store the packaging assignments for subsequent runs. The `pxl.state` file stores the mapping information for physical nets, differences between the schematic and the layout, and instance-specific information for reused hierarchical or structured blocks.

- `pxl.log`

  Packager-XL dumps any warnings and errors encountered during the Packager-XL run in the `pxl.log` file. This file also includes the values of directives used and run statistics such as elapsed time.

- `pstchip.dat`, `pstxprt.dat`, and `pstxnet.dat`

  Packager-XL generates three netlist files, `pstchip.dat`, `pstxprt.dat`, and `pstxnet.dat`. These files are imported by PCB Editor to create or update a board.

Packager-XL utilities, such as the Bill of Materials (BOM), also use netlist files to generate BOM reports.

- `pstcmdb.da`

  Packager-XL generates the above file (in addition to all other files mentioned in this section) when it runs in the Constraint Manager-enabled flow. The file contain information about the current electrical constraints for the design. If you are running Packager-XL in the traditional flow then information about the current electrical constraints for the design is stored in the `pstxnet.dat` file.

- `pstback.dat`

  Packager-XL generates the `pstback.dat` file, which backannotates the Design Entry HDL schematic with packaging information, such as reference designator assignments and physical pin numbers. Backannotation is done using the `backannotate` command in Design Entry HDL.

- `pxl.chg`

  Packager-XL dumps the differences in packaging between two consecutive runs of Packager-XL in the `pxl.chg` file. This file contains a list of the binding changes, logical changes, physical changes, and net changes.

- `pstcmback.dat`

  If you are using the Constraint Manager-enabled flow, then the *Tools > Constraints > Update Schematic* and *Tools > Back Annotate > Constraint Backannotation* command*s* create the `pstcmback.dat` file. This file contains information about the electrical constraints that require backannotation to the schematic.

  The `Import Logic` program in PCB Editor uses all Packager-XL output files to import the packaged design.

# Packaging Hierarchical Designs Using Command Line Option

When you run Packager-XL for hierarchical designs, the root (top) level and each reuse block must be packaged with each block defined as the root. Classifying each reuse block as the root and packaging it is done manually.

To simplify this process, you can package hierarchical designs using a command-line option, which allows you to hierarchically package the designs in a batch process. Packaging hierarchical designs in a batch process is like running Packager-XL on a hierarchical design with a bottom-up approach.

To package hierarchical designs in a batch process, use the following command:

```
csnetlister -proj <cpm file name> -packageonly
```

Packager-XL runs on the root-level design and all the reuse blocks that are in the design, starting from the block instantiated at the lowest level in the block hierarchy.

After running the `csnetlister -proj` command, you can check `netlistSummary.log`. This file contains information about the Packager-XL status for each block in the design, such as whether the block was run, and information about any errors or failures during the Packager-XL run.

You can ignore the NETLIST RUN STATUS column in `netlistSummary.log`, since the column is not applicable to the `-packageonly` option.

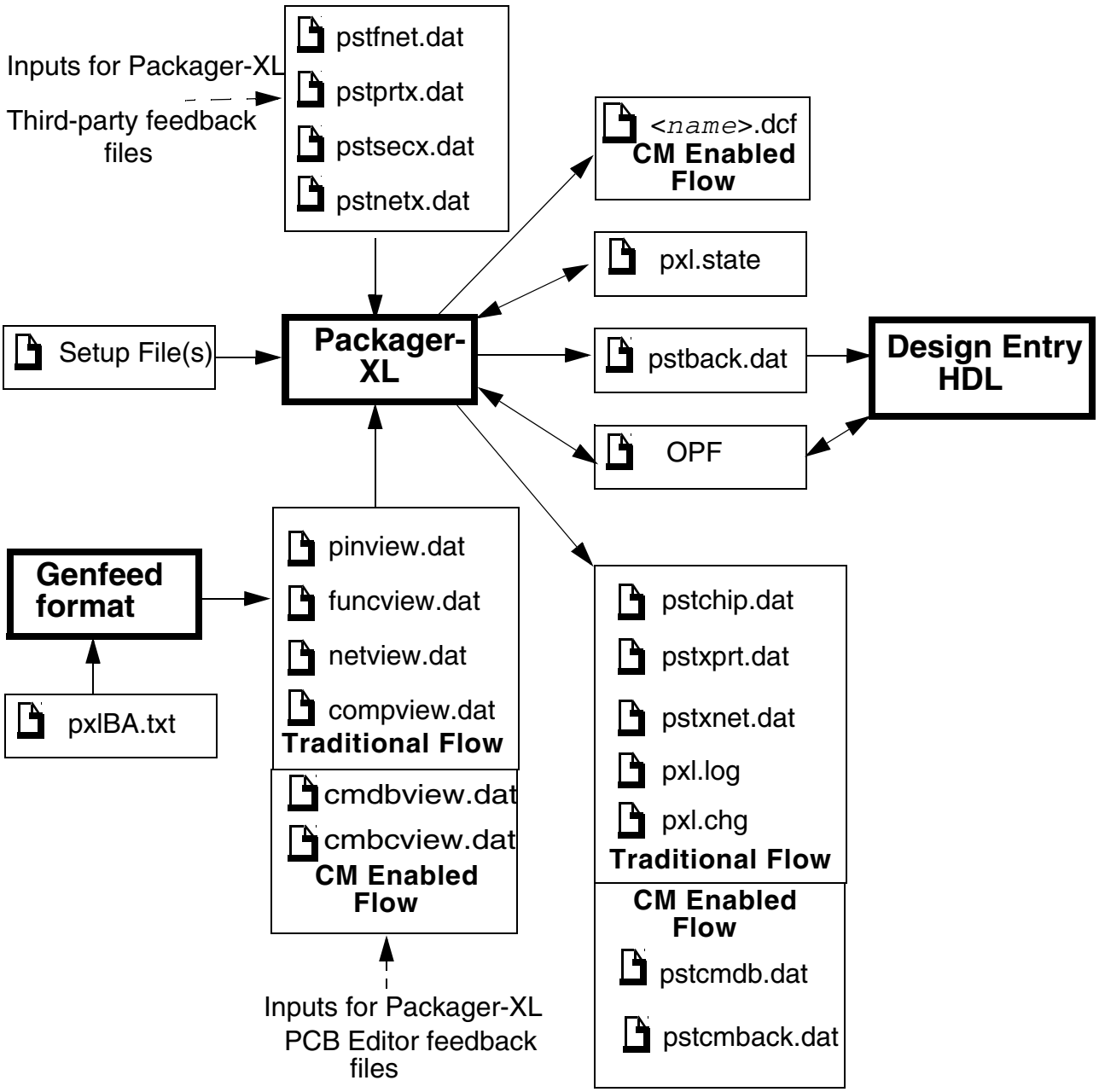
If there are any errors or failures for any blocks, you can check `csnetlister.log`, which logs all the blocks that were packaged.

**Note:** Components in the reuse blocks are not packaged with the components in the root blocks.

# Feedback Mode

After you have packaged the design and prepared the board, you may add new components, or make property, connectivity, or reference designator changes. These changes cause the schematic and the board to go “out of sync”. You can use the Feedback mode to incorporate the logical changes and assignments made in the physical layout back to the design. See the Feedback Mode of Operation figure on page 79 for details.

**Figure 4-5 Feedback Mode of Operation**




## Inputs to the Feedback Mode

The inputs to Packager-XL during the feedback mode are as described below:

1. Export Logic from PCB Editor or Import Physical from Packager-XL

   To extract information from the physical layout and create feedback files for Packager-XL, you use the PCB Editor `Export Logic` program.

2. `pxlBA.txt` (You can use Property Flow Setup UI to generate this file)

   To change backannotation information, you can modify the `pxlBA.txt` file. This file is used by the PCB Editor `Export Logic` program to determine the properties included in the feedback files.

3. PCB Editor feedback files (`pinview.dat`, `funcview.dat`, `netview.dat`, and `compview.dat`)

   PCB Editor feedback files are produced by genfeedformat. These files store the following information:

   - `pinview.dat`—This file stores information about connectivity and pin instance properties.
   - `funcview.dat`—This file stores property information for schematic instances.
   - `netview.dat`—This file stores property information for nets.
   - `compview.dat`—This file stores property information for component instances.

   PCB Editor feedback files provide Packager-XL inputs about all changes that are made in the board.

   In the Constraint Manager-enabled flow, besides the above 4 *view.dat files, Packager-XL also uses the following 2 files, which are generated by genfeedformat when you run Import Physical or Export Logic from PCB Editor:

   - `cmdbview.dat`—This file stores information about the current electrical constraints for the design.
   - `cmbcview.dat`—This file stores the electrical constraint information for the design used by the board during the last time when it was updated.

4. Third-Party Feedback Files

   If you are running a third-party layout tool, you can produce four feedback files (`pstfnet.dat`, `pstprtx.dat`, `pstsecx.dat` and `pstnetx.dat`) and use them as input to Packager-XL during the Feedback mode. These files store the following information:

   - `pstfnet.dat`—This file describes the connectivity for each reference designator pin number in the design. You require this file as an alternate feedback file from third-party layout systems other than PCB Editor.

- `pstprtx.dat`—This file describes the physical reference designator changes.
- `pstsecx.dat`—This file describes section changes. Using this file, you can reassign logical parts within the same physical package or to another physical package.
- `pstnetx.dat`—This file describes the physical net name changes.

You use either PCB Editor feedback files or third-party feedback files but not both.

### Outputs From the Feedback Mode

After receiving inputs, Packager-XL produces output files, which include the `pstback.dat` file used by Design Entry HDL for backannotation.

Packager-XL produces the following files in the Feedback mode:

1. `pstback.dat`—Design Entry HDL uses this file to backannotate to the base schematic.
2. `pxl.state`—Packager-XL updates the pxl.state file to store packaging information about future runs.
3. `OPF`—Packager-XL updates the OPF file with any change in property or connectivity information that might have occurred in the board after the initial transfer of packaging information from the schematic.
4. Output files—Packager-XL generates the following output files: `pstchip.dat`, `pstxprt.dat`, `pstxnet.dat`, `pxl.log`, and `pxl.chg`. These output files are updated so that future runs by PCB Editor get the right packaging information. The output files generated by Packager-XL in the Feedback mode are the same as the output files generated in the Forward mode.

   In the Constraint Manager-enabled flow, Packager-XL generates one more pst file, `pstcmdb.dat`.

# Properties and Directives

You can use Packager-XL properties to control the packaging of the schematic. You can control the flow of properties between Packager-XL and the layout tool using Packager directives.

## Packager Properties

You can assign properties to do the following:

- Define unique physical components or devices by using component definition properties.
- Assign schematic instances to specific reference designators or sections (using the LOCATION property and the SECTION command in Design Entry HDL).
- Swap pins within sections (using the PINSWAP command in Design Entry HDL).
- Group schematic instances (using the GROUP property), or assign schematic instances to specific areas on the board (using the ROOM property).
- Mark schematic instances for special handling during packaging (using the PACK_IGNORE and PACK_SHORT properties).

During the packaging of a design, Packager-XL makes packaging assignments for all schematic instances that do not have user-assigned values. These assignments are saved in the state file for use in future runs of Packager-XL. These assignments are also written to the backannotation file pstback.dat, which is used by Design Entry HDL to backannotate properties to the schematic. Packager-XL assignments are backannotated to the Design Entry HDL schematic as CDS_LOCATION, CDS_SEC, and CDS_PN properties.

Packager-XL backannotates two sets of properties to the Design Entry HDL drawing.

- Packager-XL properties (CDS_LOCATION, CDS_SEC, and so on)
- Display properties ($LOCATION and $PN)

You can replace Packager-XL-assigned properties. For example, you can edit the $LOCATION or $PN properties and make them work like the LOCATION or PN properties. Packager-XL does not replace the value for the edited $LOCATION or $PN properties. To change the SEC property, you must use the SECTION command in Design Entry HDL.

## Packager Directives

Packager directives are specified in the Packager Setup form and are stored in the project file. These directives allow you to control the flow of properties between Packager-XL and the layout tool.

- FILTER_PROPERTY—Use the FILTER_PROPERTY directive to specify the properties to be omitted from the output files. You can list any number of properties to be omitted.
- PASS_PROPERTY—Use the PASS_PROPERTY directive to specify the properties that are to be passed to the packager output files.

- REMOVE_FROM_STATE—Use the REMOVE_FROM_STATE directive to specify the properties to be removed from the state file.
- STATE_WINS_OVER_DESIGN—Use the STATE_WINS_OVER_DESIGN directive to use the property values in the state file to replace the values in the schematic.
- STATE_WINS_OVER_LAYOUT —The STATE_WINS_OVER_LAYOUT directive is used only when feedback is allowed. By default, the feedback properties are retained in the state file. Use the STATE_WINS_OVER_LAYOUT directive to specify that the property values in the state file replace the values in the feedback properties.

# Prerequisites for Running Packager-XL

Before you run Packager-XL, you need to

- Specify your design and include Packager-XL-specific properties in Design Entry HDL.
- Create or modify the setup information for Packager-XL. See Chapter 2, “Setting Up Packager-XL” for more information about Packager Setup.

  **Note:** You can create or modify the setup information for Packager-XL using a text editor or the Setup program. However, it is recommended that you change properties using the Packager Setup dialog box.

# Running Packager-XL in the Forward Mode

## Updating the Board with the Changes in the Schematic

After you have specified the setup information, you can run Packager-XL from Project Manager or from an operating system prompt.

**Note:** It is not recommended that you run Packager-XL from an operating system prompt.

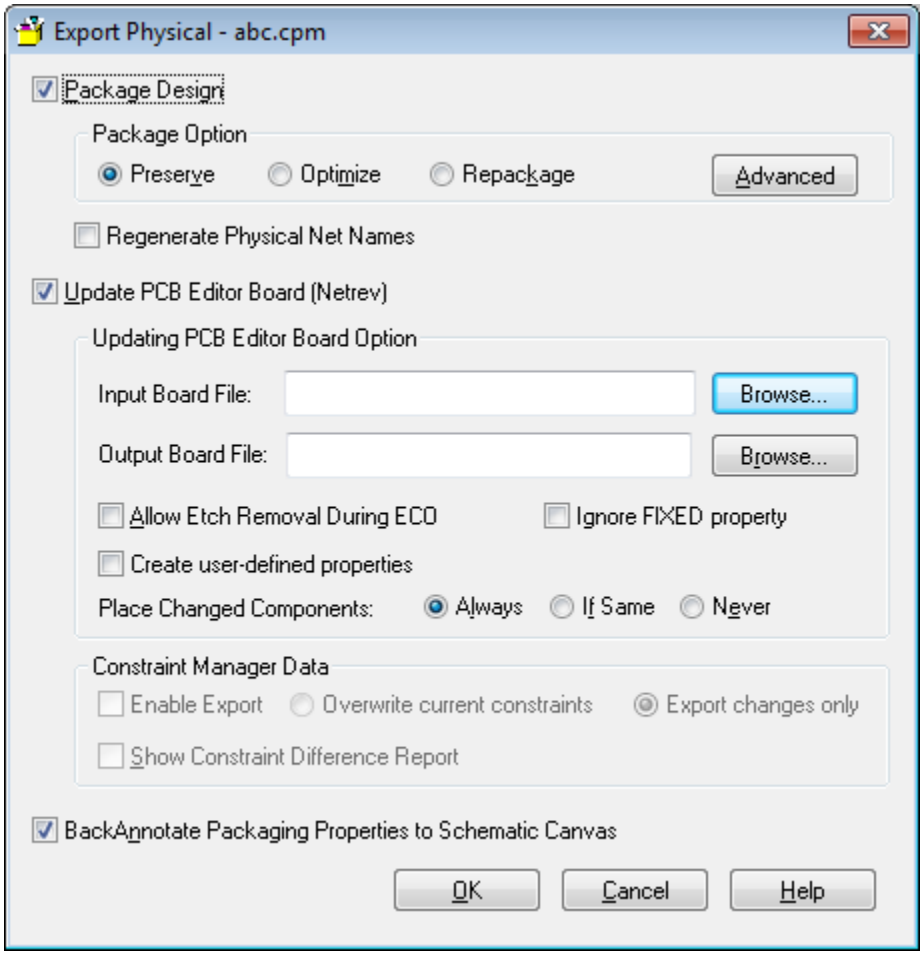
To run Packager-XL from Project Manager and transfer the logic from the Design Entry HDL schematic to the PCB Editor board, do the following steps:

1. Choose the *Design Sync* icon from the Project Manager window and click *Export Physical.*

   **Note:** You can also choose *Tools - Design Sync - Export Physical* to display the Export Physical dialog box.

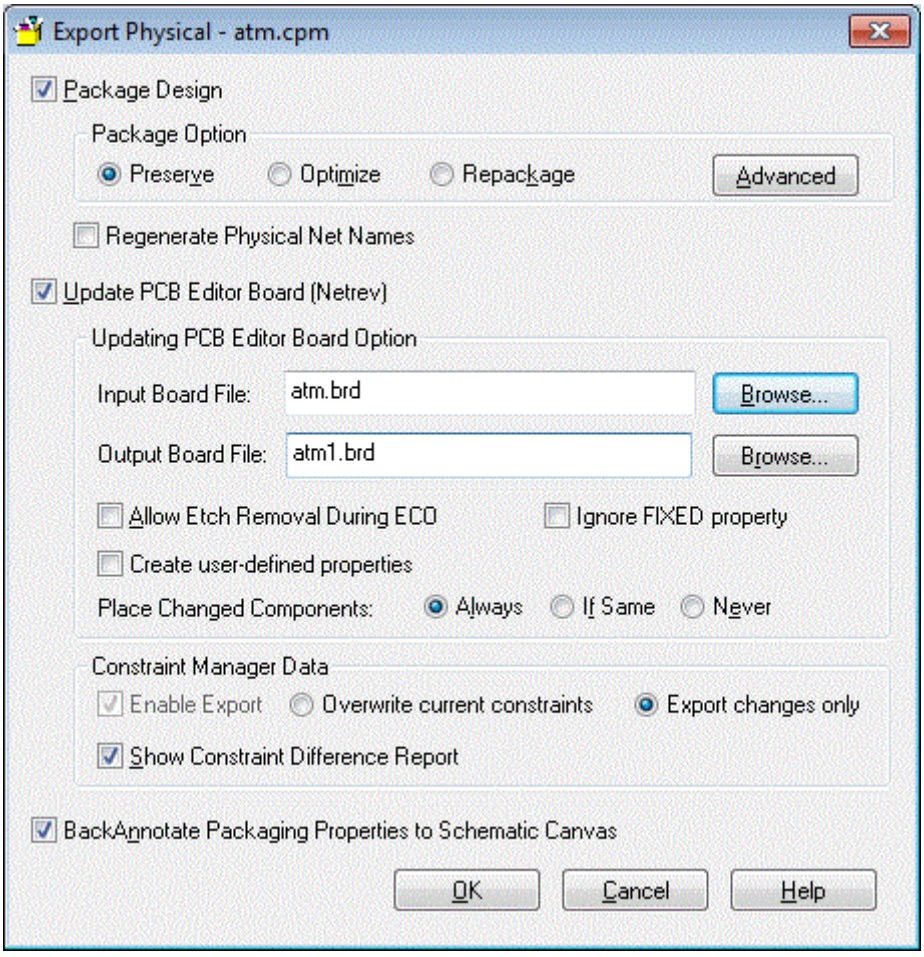
Depending on whether you are using Constraint Manager to edit electrical constraints in Design Entry HDL (which means depending on the presence of the <*root_drawing*>.dcf file in the constraints view), Export Physical runs in two flows, traditional and Constraint Manager enabled. The Export Physical Dialog Box: Traditional Flow figure on page 84 shows the Export Physical dialog box that appears when Constraint Manager is not used to edit electrical constraints in Design Entry HDL.

**Figure 4-6 Export Physical Dialog Box: Traditional Flow**




The Export Physical Dialog Box: Constraint Manager-Enabled Flow figure on page 85 shows the Export Physical dialog box that appears when Constraint Manager is used to edit electrical constraints in Design Entry HDL.

**Figure 4-7 Export Physical Dialog Box: Constraint Manager-Enabled Flow**




2. To package your design before updating the layout data, select the *Package Design* check box. You have the following options in packaging:

   - `Preserve`—Packager-XL uses *Preserve* as the default packaging option. When the *Preserve* option is selected, Packager-XL incrementally packages the design. All previous packaging is preserved and only the changes from the last packaging run are added.
   - `Optimize`—Packager-XL uses *Optimize* to package the schematic data into a compact physical design.
   - `Repackage`—Packager-XL uses *Repackage* to ignore all previous packaging results and repackage the design.

3. If you want to regenerate physical net names, select the *Regenerate Physical Net Names* check box.

**Note:** Selecting the *Regenerate Physical Net Names* check box is useful if you have changed the net length and you have not selected *Repackage* as the packaging option.

**Note:** Be cautious about selecting the *Regenerate Physical Net Names* check box. An accidental selection can remove all assigned physical net names. You can gray out the *Regenerate Physical Net Names* check box by setting the `DISABLE_REGEN_NET_NAME` directive to `YES` in the `DESIGNSYNC` section of the project (.cpm) file.

4. Select a package design setting.
5. If you want to change the Packager-XL setup options, click the *Advanced* button.

   The Packager Setup dialog box appears. See Chapter 2, "Setting Up Packager-XL" for more information about setting Packager-XL setup options.
6. To update the PCB Editor board, select the *Update PCB Editor Board (Netrev)* check box in the Export Physical dialog box.
7. Specify the input and output board files. Enter the name of the existing PCB Editor file that needs to be updated in the *Input Board File* field. Enter the name of the resulting updated file in the *Output Board File* field. To specify the *Input Board File*, click the *Browse*... button. Packager-XL displays the board files (if any) in the `physical` sub-directory under the `design` directory. You can select the board file and click *OK*.

   If you specify the output board file as the same as the input board file, Packager-XL overwrites the existing file. If you specify the output board file as a new file (<*any_name*>.`brd`), a new board file is created.

   **Note:** Before you transfer the logic data from Design Entry HDL, you must create the design database (.`brd`) file in PCB Editor. You can create an empty .`brd` file, or start setting up your design by creating a board outline and defining the layers for the design.
8. To make PCB Editor rip up an etch from a removed pin to the closest connection or pin, select the *Allow Etch Removal During ECO* check box.
9. To indicate that components with FIXED property set as TRUE can also be moved or deleted, select the *Ignore FIXED property* check box.
10. This check box is used for changing symbols. For example, fix three out of four dip14_3 components on a board. Change your `pstchip.dat` file so that `soic14` is used instead of `dip14_3` for the JEDEC_TYPE. Import a design without selecting the *Ignore FIXED property* check box. An error pops up that the object cannot be modified because of a FIXED property. This is because the part is fixed and you cannot change the symbol.
11. You can now either remove the fixed component from the parts, which can take some time, and then import the design, or you can select the *Ignore FIXED Property* check box so that you do not have to remove the fixed property. Either way, the error will no longer be displayed and the `soic14` symbol replaces all the `dip14_3` symbols on the

board. Note that the latter option (ignore fixed property) keeps the fixed property on the components that have it, so a fixed `dip14_3` becomes a fixed `soic14`.

**12.** In summary, when importing a schematic, parts that are fixed are deleted if they are not in the netlist. The ignore fixed property only allows you to change the board symbols without removing the fixed property first.

**13.** To create user-defined properties, select the *Create user-defined properties* check box.

User properties are added automatically into the board when you run the export physical command. When you delete such a property in Design Entry HDL, it is automatically deleted from the PCB Editor board.

**14.** Select the option for placing changed components in layout from those made available by packager-XL. Select one of the following three options:

- Always

This is the default selection. If you load a new design logic into the PCB Editor or SI layout, PCB Editor automatically replaces all components in the layout with the new components from Packager-XL according to their reference designators.

- If same

PCB Editor automatically replaces all components in the layout with the new components from Packager-XL but only if the replacement component matches the package symbol, value, and the tolerance of the component in the layout.

- Never

PCB Editor will never replace any components in the layout with new components. You must make the changes interactively.

**15.** In the traditional flow, the *Electrical Constraints* options are disabled. You cannot make any selection. However, in the Constraint Manager-enabled flow, the *Enable Exports* check box is selected by default. You need to select one of the following two options for exporting constraints from the schematic to the board:

- Overwrite current constraints

Netrev deletes all existing electrical constraint information in the *Output Board File* and replaces it with the electrical constraint information currently available in the schematic.

- Export changes only

Netrev exports only the electrical constraint information that has changed in the schematic since the last export, and updates such constraints in the *Output Board File*.

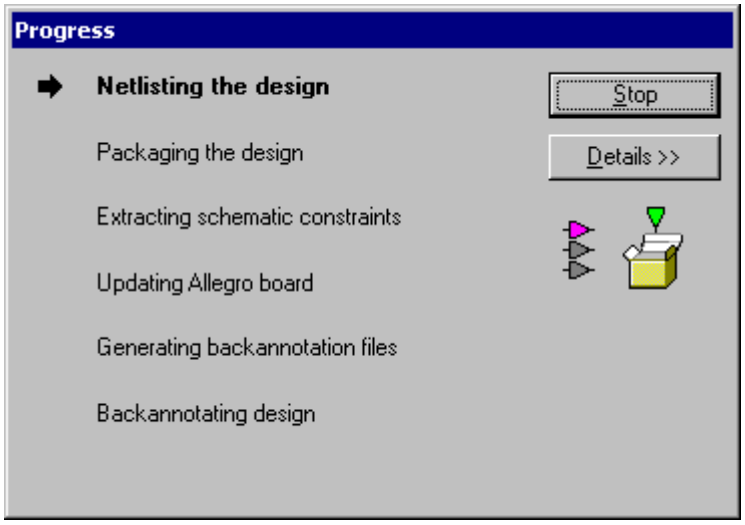
16. Select the *Backannotate Packaging Properties to Schematic Canvas* check box to backannotate packaging data to the schematic when you run Export Physical.

    **Note:** Electrical constraints are automatically backannotated to schematic canvas.

17. In the Export Physical dialog box, click *OK*.

    The Progress window appears. Information in the Progress window will change based on the options you selected.

**Figure 4-8 Progress Window**




In the traditional flow, the following four steps are performed by Packager-XL:

1. Netlisting the design (Select the *Package Design* check box)
2. Packaging the design (Select the *Package Design* check box)
3. Updating the board (Select the *Update PCB Editor Board* check box)
4. Backannotating the design (Select the *Backannotate Packaging Properties to Schematic Canvas* check box)

In the Constraint Manager-enabled flow, the following two steps are performed by Packager-XL in addition to the four steps performed in the traditional flow:

1. Extracting schematic constraints.
2. Backannotating electrical constraints.

When Packager-XL completes packaging the design, it displays a message stating that packaging is completed and whether you want to view the results. If you want to view the results, select the *View Results* button. The View Files dialog box appears. You can select a file and view it in the default text editor.

### Mismatch in View Files Generated Across Different Release/Flows

If you have a Version 14.0 Constraint Manager enabled design and bring it to Version 14.2 by running only genfeedformat, then the `pstxnet.dat` and `pstcmdb.dat` files will not have the same tag that is used to identify the flow. Export Physical in such case will generate the following message:

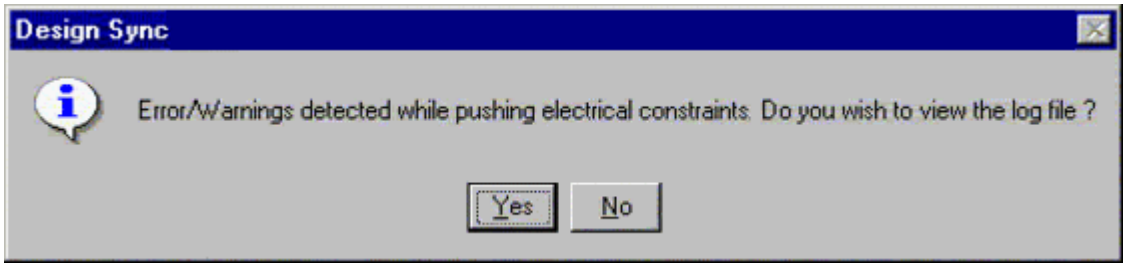
```
Design Flow is Constraint Manager enabled, pstxnet.dat and pstcmdb.dat do not
appear to be from the same feedback step. You will not be able to
package the design.
```

Export Physical will not package the design. However, it will call genfeedformat and generate the `*view.dat` and `pstcmdb.dat` files. You can then again package the design.

### Errors in Electrical Constraints Extraction

If you have defined an electrical constraint with an incorrect syntax, then you will get the following message:

**Figure 4-9 Design Sync Error Message**




If you click *Yes*, the concept2cm.log file opens. It lists the errors. You can fix the error and then run *Tools-Constraints-Update Schematic* command to update the schematic with proper values.

## Using the State File for Successive Packager-XL Runs

After the initial packaging, you can make changes to your design. These changes can include adding and deleting pages, schematic instances, nets, connectivity, and properties. The next time you package the design, Packager-XL does the following:

1. Reads the state file that contains the packaging data from the previous run.
2. Copies the state file information to the relevant parts of your design (parts that have not changed since the previous Packager-XL run). The `STATE_WINS_OVER_DESIGN` and `REMOVE_FROM_STATE` directives control how the state file data is copied to the design. See the Cadence document *Packager-XL Reference* for more information on how you can use the `STATE_WINS_OVER_DESIGN` directive.
3. Packages the entire design - Conflicts occur when the state file packaging assignments are in conflict with the assignments you make. For example, if you have modified your schematic by assigning a section to a part that was previously packaged, the assignment in the state file is ignored.

   In case of a conflict, Packager-XL reassigns the `LOCATION`, `SEC`, and `PN` properties that it copied from the state file. However, the state file packaging information is preserved whenever possible.

# Running Packager-XL in the Feedback Mode

## Overview

The following types of changes are made in PCB Editor:

- Renaming reference designators
- Swapping sections
- Swapping pins
- Updating property values

These changes need to be updated in the schematic. You can run Packager-XL in the Feedback mode to update the changes made in the board back to the schematic.

## Updating the Schematic with the Changes in the Board

You need to integrate the layout changes with the existing logical design by running Packager-XL in the Feedback mode.

You can use the following two steps to run Packager-XL in the Feedback mode:

1. Generate the layout feedback files from PCB Editor or third-party tool.

2. Integrate the layout changes with the existing logical design by running Packager-XL in the Feedback mode.

### Using Export Logic to Extract Feedback Files

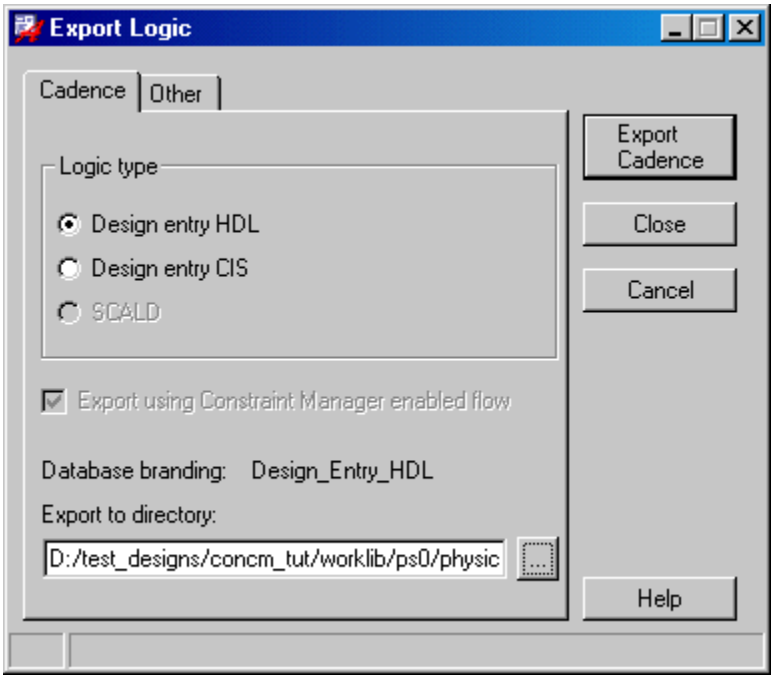
1. From the PCB Editor `Export Logic` function,

   a. Choose *File - Export - Logic* in PCB Editor.

   The Export Logic dialog box appears. Depending on whether you are using Constraint Manager to edit electrical constraints in Design Entry HDL (which means depending on the presence of the <*root_drawing*>.dcf file in the constraints view), Export Logic runs in 2 flows, traditional and Constraint Manager enabled.

   The Export Logic Dialog Box: Constraint Manager-Enabled Flow figure on page 91 appears when Export Logic detects that the design is in the Constraint Manager-enabled flow, that is Constraint Manager has not been used to edit electrical constraints in Design Entry HDL.

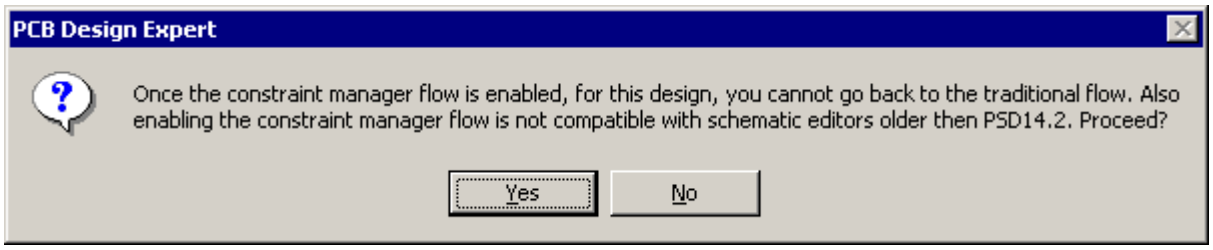
**Figure 4-10 Export Logic Dialog Box: Constraint Manager-Enabled Flow**




   b. To switch to the Constraint Manager-enabled flow from the traditional flow, select the *Export using Constraint Manager enabled flow* check box.

**Note:** If you switch to the Constraint Manager-enabled flow, you cannot return to the traditional flow. A message box appears stating this fact, if you want to change flow to Constraint Manager enabled, click *Yes*.

**Figure 4-11 Export Logic Dialog Box: Traditional Flow**




**c.** Select the logic type as *HDL-Design Entry*.

**d.** Specify the path of the directory where you want to store the exported files.

**e.** Click the *Export Cadence* button.

The five feedback (*view.dat) files are generated.

**Note:** If you run Import Physical and select the *Generate Feedback Files* option, you need not run Export Logic in PCB Editor.

### Moving From Three to Six File Flow: Handling Special Case

If you are in the traditional flow in the Forward mode, 3 pst*.dat file would be generated. Now if in PCB Editor you run *File - Export - Logic* and select the *Export using Constraint Manager enabled flow* check box, PCB Editor switches to six files-based Constraint Manager-enabled flow:

Since the PCB Editor board was branded as working in traditional flow, do an explicit save of the PCB Editor board file. This will ensure that the board file is branded as working in the Constraint Manager-enabled flow.

Next, run Import Physical and select the *Package Design* check box to package the design. This step will ensure that both Design Entry HDL and PCB Editor are running in the Constraint Manager-enabled flow.

**Note:** If you do not run Import Physical and run Export Physical immediately after switching to the Constraint Manager-enabled flow in PCB Editor, then Netrev will generate an error stating that the `pstcmdb.dat` file is not found.

### Using Import Physical to Update the Schematic and the Board

You can use the Import Physical dialog box to update the schematic with the changes in the board. To update the schematic with changes in the board using Import Physical, do the following:

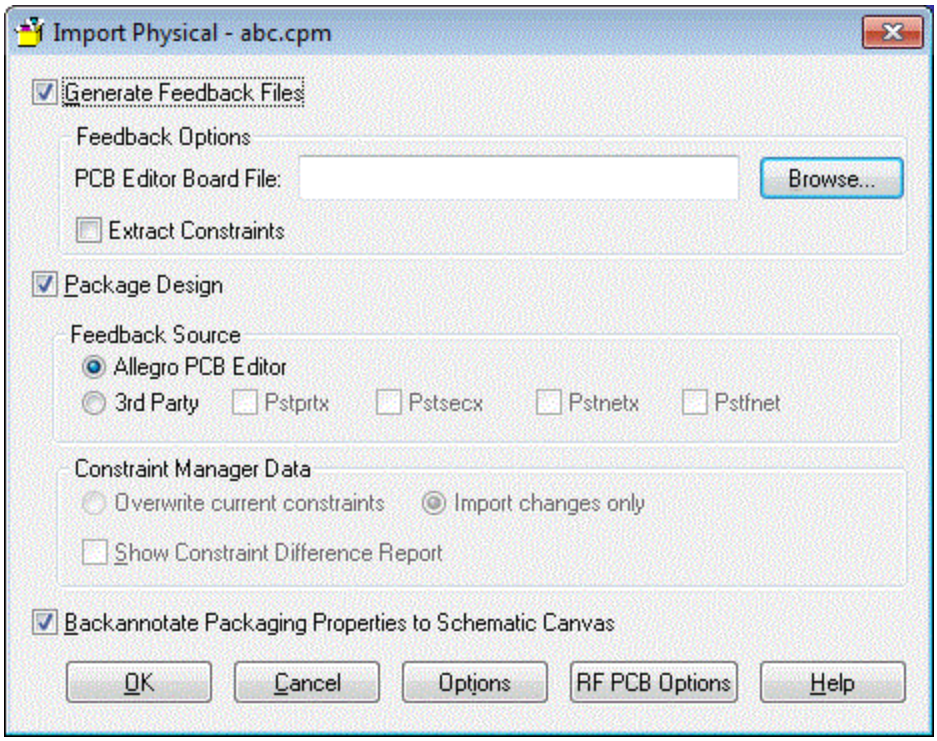
1. Choose *Tools - Design Sync,* and click on the *Import Physical* option in the drop-down menu.

   Import Physical can run in two flows, traditional and Constraint Manager enabled. If Constraint Manager has not been used to edit electrical constraints in Design Entry HDL, Import physical runs in the traditional flow otherwise it runs in the Constraint Manager-enabled flow. You can move from the traditional flow to the Constraint Manager-enabled flow but not vice versa.

   The Import Physical Dialog Box: Traditional Flow figure on page 94 appears when Import Physical detects that the design is in the traditional flow. A design is in the Constraint Manager-enabled flow when:

   - No <*root_drawing*>.dcf file is found in the constraints view.
   - The *Generate Feedback Files* check box is not selected and only 4 pst*.dat files exist in the packaged view.
   - The *Generate Feedback Files* check box is selected but the *Extract Constraints* check box is not selected.

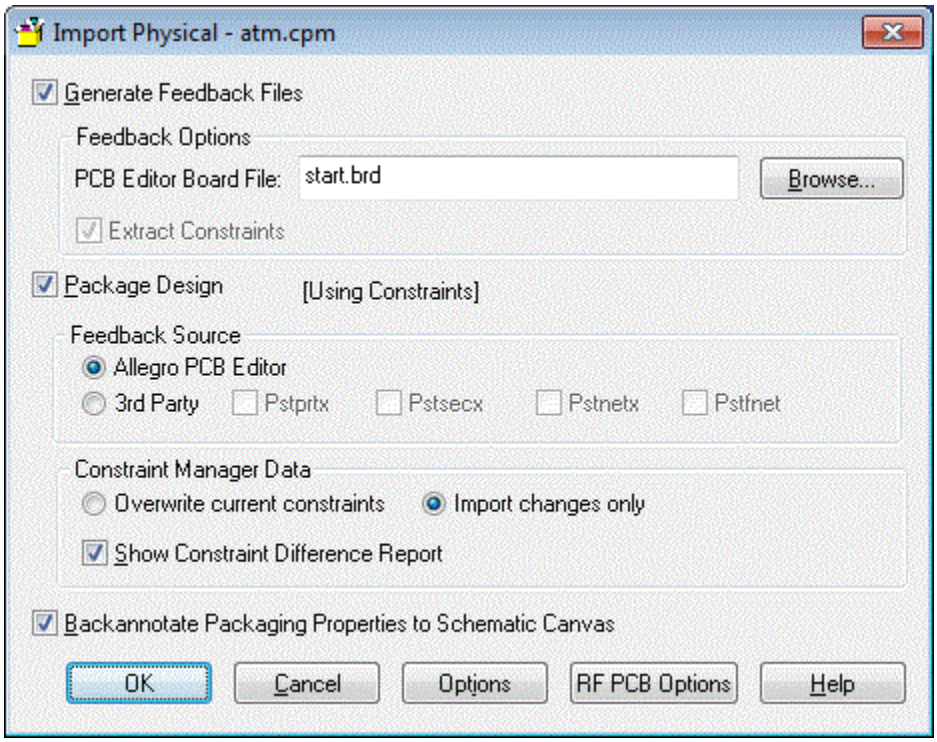
**Figure 4-12 Import Physical Dialog Box: Traditional Flow**




The Import Physical Dialog Box: Constraint Manager-Enabled Flow figure on page 95 appears when Import Physical detects that the design is in the Constraint Manager-enabled flow. A design is in the traditional flow when:

- The <*root_drawing*>.dcf file is found in the `constraints` view.
- 6 `pst*.dat` files exist in the `packaged` view.
- The *Generate Feedback Files* check box is selected and the *Extract Constraints* check box is also selected.

**Figure 4-13 Import Physical Dialog Box: Constraint Manager-Enabled Flow**




2. Select the *Generate Feedback Files* check box.

*Tip*

You can also use *File > Export > Logic* in PCB Editor to generate feedback files.

3. Specify the PCB Editor board name in the *PCB Editor Board File* field.

4. To integrate the layout changes with the existing logical design, run Packager-XL in the Feedback mode by clicking the *Package Design (Feedback)* check box and selecting the feedback source. You can select either PCB Editor or third party files for feedback. If you have 3rd party files for feedback, select the feedback files to be generated by selecting the appropriate check boxes.

5. Select the option for exporting constraints from the schematic to the board. These options are available based on whether you are in the Constraint Manager-enabled flow or the traditional flow.

   - *Extract Constraints* check box

     In the Constraint Manager-enabled flow, the *Extract Constraints* check box is selected and grayed. You cannot change it. In the traditional flow, you can select this

check box. When you are in the traditional flow and you select the *Extract Constraints* check box, Import Physical displays the following message:

**Figure 4-14 Import Physical: Warning Message**


If you select the *Yes* button, then Import Physical will move to the Constraint Manager-enabled flow where electrical constraint information is generated in the `cmdbview.dat` and the `cmbcview.dat` files. You cannot switch back to the traditional flow. Therefore if you want to stick to the traditional flow and maintain electrical constraint information in the `pstxnet.dat` file, click on the *No* button.

- Overwrite current constraints

  Packager-XL overwrites all existing electrical constraint information in the *schematic* with the electrical constraint information currently available in the *PCB Editor Board File*.

- Import changes only

  Packager-XL will import only the electrical constraint information that has changed in the *PCB Editor Board File* since the last import and overwrite such constraints in the schematic.

6. Select the *Backannotate Packaging Properties to Schematic Canvas* check box to backannotate packaging data to the schematic when you run Import or Export Physical. Clear this check box if you do not want the schematic to be backannotated with packaging data when you run Import Physical. You can perform backannotation later by choosing *Tools - Back Annotate* in Design Entry HDL.

*Caution*

***Do not run backannotation if any other user who has write permissions is working on the design. Running backannotation when another user is working on the design results in incomplete backannotation.***

7. Click *OK*.

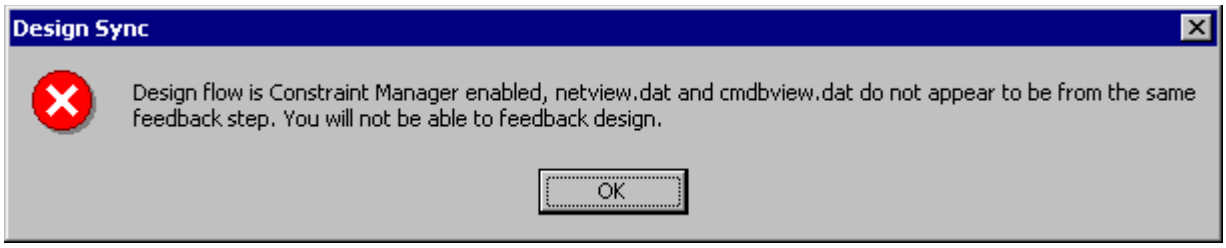
The Progress dialog box appears, displaying the progress of the Import Physical process.The feedback files are created from the PCB Editor or SI board. Packager-XL is run in the feedback mode using the feedback files from PCB Editor. The files used for backannotating the constraint changes in the board to the schematic are created in the `packaged` view of the root design. The constraints in the board are extracted to a file called `pstcmback.dat`. This file is used to backannotate the changes in constraints in the board to the schematic.

The constraints in the schematic are synchronized with the constraints in the board. If you now start Constraint Manager from Design Entry HDL, all the electrical constraints that you captured in PCB Editor, APD or SI will appear in Constraint Manager.

### Mismatch in View Files Generated Across Different Release/Flows

If the `netview.dat` and `cmdbview.dat` files have not been generated at the same time or they have been hand-edited, then Import Physical generates the following message:

**Figure 4-15 Import Physical: Warning Message**




Import Physical will not feedback the design. However, it will call genfeedformat and generate the `netview.dat` and `cmdbview.dat` files. You can then again feedback the design.

## Using the pxlBA.txt File for Controlling the Backannotation of Properties

### Overview

The `pxlBA.txt` file is a file used during backannotation. It lists the properties that you may need to extract from the PCB Editor or SI layout. Before you run the *Import Physical* command or the *Export Logic* program, you can modify the `pxlBA.txt` file to control the properties that you want to extract from the PCB Editor or SI layout. You can extract either standard PCB Editor properties or PCB Editor user-defined properties.

The `pxlBA.txt` file is located at the following path:

`<`*`your_install_dir`*`>/share/pcb/text/views`

You can specify the properties in the `pxlBA.txt` file by using the *Property Flow Setup* button in the Packager Setup - Properties Tab.

### Displaying the pxlBA.txt File

**Note:** You can launch the `pxlBA.txt` file from Project Manager, the Packager Setup dialog box, or the Design Differences tool.

### Displaying the pxlBA.txt file from Project Manager

1. Choose *Tools - Packager Utilities - View Results…* from the Project Manager menu bar.
2. Click the *Physical* option.

   The view files in the `physical` view directory appear in the View Results window.
3. Select the `pxlBA.txt` file from the view files listed.
4. Click *OK*.

The `pxlBA.txt` file appears in a text editor. You can view or edit this file for properties that you want to be backannotated from the layout during feedback.

### Displaying the pxlBA.txt File from the Packager Setup Dialog Box

1. Select the *Property* tab to display the *Packager Setup - Properties* page of the Packager Setup dialog box.
2. Click the *Property Flow Setup* button.

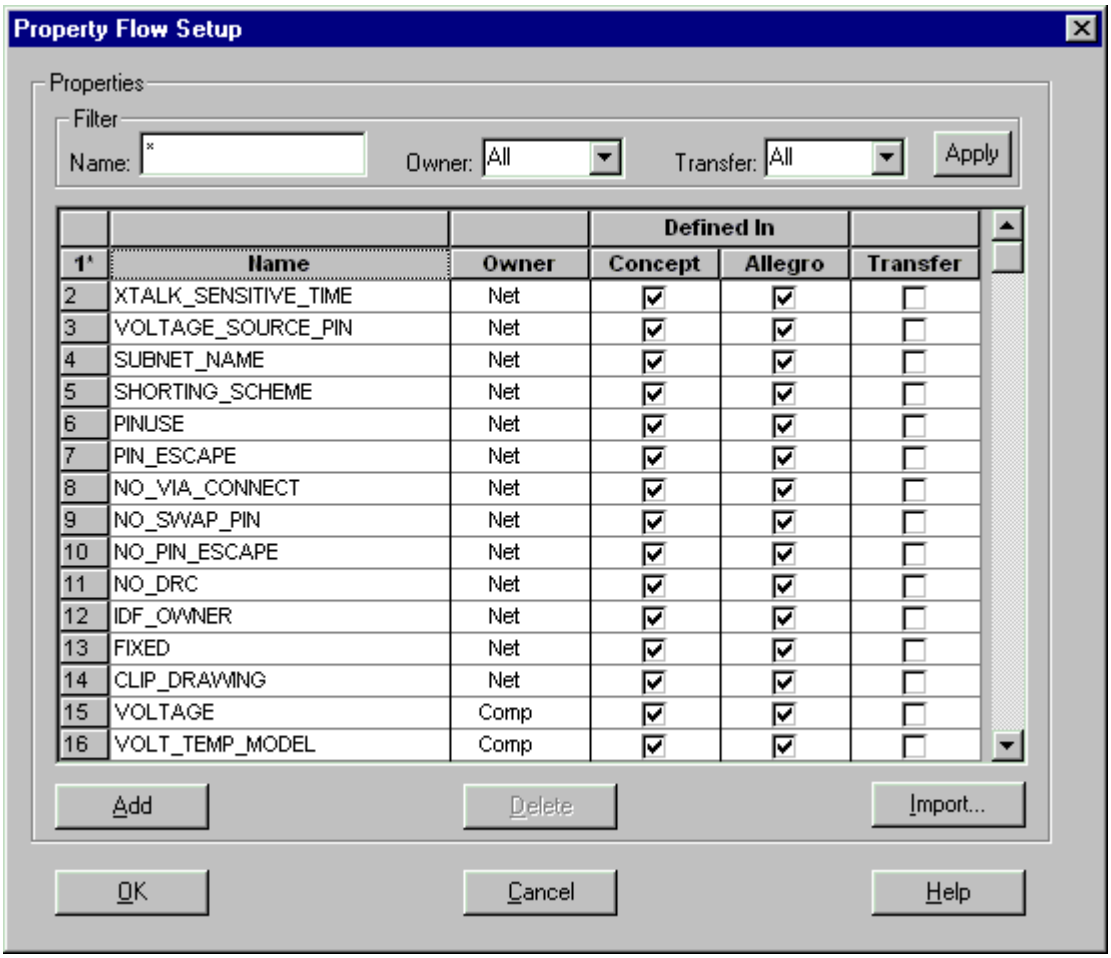
The Property Flow Setup dialog box appears. The dialog box provides a graphical interface for changing the properties in the `pxlBA.txt` file.

### Displaying the pxlBA.txt file from Design Differences

➤ Choose *Difference - Property Flow Setup.*

The Properties Flow Setup dialog box appears with the default `pxlBA.txt` file loaded. See the Property Flow Setup Dialog Box figure on page 99.

**Figure 4-16 Property Flow Setup Dialog Box**




The Property Flow Setup dialog box lists the properties that flow between Design Entry HDL and PCB Editor. Each property name follows with the property owner name (net, pin, component, or function). You can specify whether the property applies to Design Entry HDL or to PCB Editor, or to both Design Entry HDL and PCB Editor. If a property applies to both Design Entry HDL and PCB Editor, you can specify whether or not the property should be transferred between Design Entry HDL and PCB Editor.

For more information about how properties flow between Design Entry HDL and PCB Editor, see PCB Editor-Design Entry Property Flow on page 59.

# Packager-XL Exit Status

After packaging the design, Packager-XL exits displaying one of the following exit status values:

**Exit status 0**

**Message** - Packager-XL execution done.

**Description** - Packager-XL has successfully packaged the design. It did not encounter any errors.

**Exit status 1**

**Message** - ERROR Packager-XL exiting with status 1.

**Description** - Packager-XL has encountered non-fatal errors during the packaging of the design. Packager-XL has generated the netlist files. However, some instances might not have been packaged. You can check the `pxl.log` file to find the details of the errors encountered.

**Exit status 2**

**Message** - FATAL ERROR Packager-XL exiting with status 2.

**Description** - Packager-XL execution failed and no netlist files are generated. You can check the `pxl.log` file to find the details of the errors encountered.

**Exit status 202**

**Message** - Packager-XL execution done. ECO detected. Exiting with status 202.

**Description** - Packager-XL has successfully completed executing. ECO (Engineering Change Order) was detected during the feedback. You should synchronize the schematic and the board.

# Using Packager Utilities

## Overview

Packager utilities are used to

- Generate the Bill of Materials (BOM) reports
- Run electrical rule checks
- Generate netlist reports

To launch any Packager utility perform the following step:

➤ Choose *Tools - Packager Utilities* in the Project Manager window and click the appropriate tool.

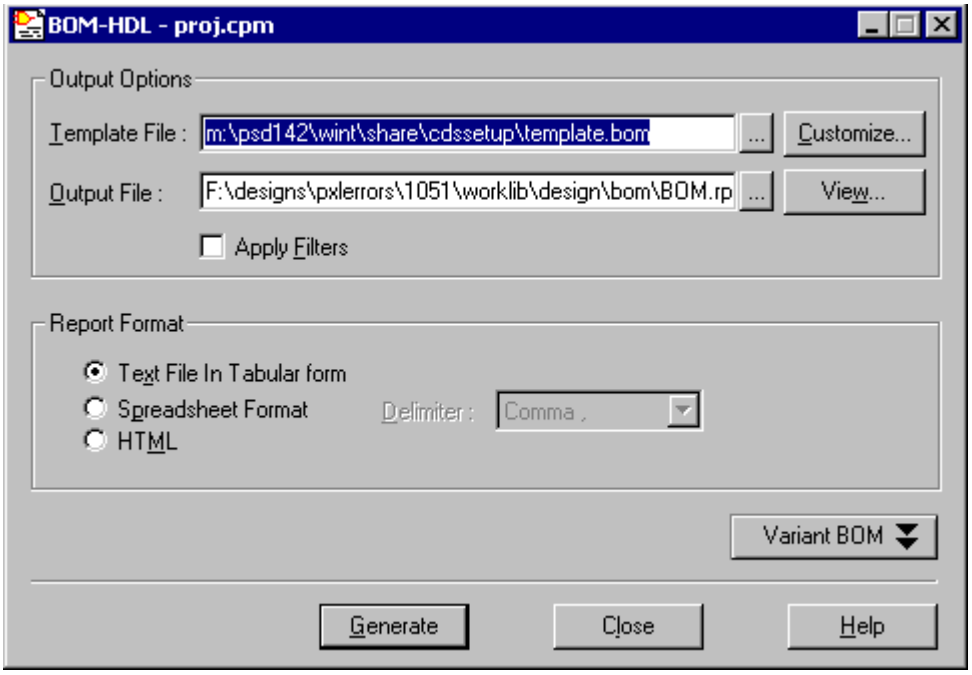
## Generating the Bill of Materials

You can use the BOM-HDL tool to generate BOM reports. To generate BOM reports, do the following:

➤ Choose *Tools - Packager Utilities - Bill of Materials* in Project Manager.

The BOM-HDL dialog box appears.

**Figure 4-17 BOM-HDL Dialog Box**




1. To change the path to the BOM template file, enter the new path of the template file in the *Template File* field. Alternatively, you can browse to the new path.

   You can customize the BOM template by clicking the *Customize* button. See BOM-HDL Help for information on how to customize the BOM template, and use callouts or filters.

2. By default, the BOM report is created in the file named `BOM.rpt`. To change the path to the output file, enter the new path of the output file in the *Output File* field. Alternatively, you can browse to the new path.

3. The default BOM report is created in the text format. To change the report format to spreadsheet or HTML, select the respective radio button. If you select the *Spreadsheet Format* radio button, you can change the delimiter by selecting a new delimiter in the *Delimiter* field. You can change the delimiter to semicolon, colon, space, dot, or hash.
4. If you have created variants for the design using the Variant Editor tool, you can click the *Variant BOM* button and select the variant.

   **Note:** See the *Variant Editor Help* for more information on creating variants and generating BOM reports for those variants.

## Running Electrical Rule Checks

You can use the Electrical Rule Checks dialog box to run electrical rule checks. Using these checks, you can verify whether or not the following conditions are correct:

- All outputs on a net have the same output type.
- All nets have at least two nodes (pins) attached to them.
- Each net has at least one input pin and output pin. If there is a bi-directional net, then it must have two pins.
- Each output pin on the net has sufficient drive for the input loading on the net.
- Each pin in the design is defined as input, output, or bi-directional.

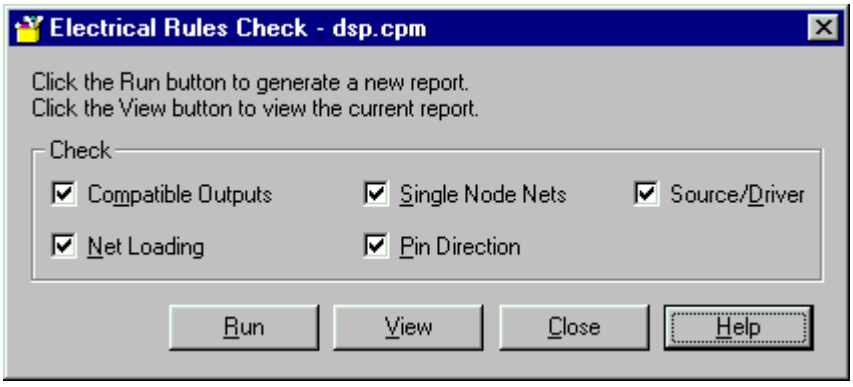
**Note:** Before running Electrical Rule Checks, you must have packaged your design to obtain the required netlist files: `pstchip.dat`, `pstxprt.dat`, and `pstxnet.dat`.

To display the Electrical Rule Check dialog box,

➤ Choose *Tools - Packager Utilities - Electrical Rules* in Project Manager.

The Electrical Rule Checks dialog box appears.

**Figure 4-18 Electrical Rules Check Dialog Box**




To perform electrical rule checks, do the following:

1. To check that all outputs on a net have the same output type, select the *Compatible Outputs* check box.
2. To check that every net has at least two nodes (pins) attached to it, select the *Single Node Nets* check box.
3. To check that each net has at least one input pin and one output pin, select the *Source/Driver* check box.

   **Note:** To override the source/driver check for a pin or a net, attach the `NO_IO_CHECK` property to it. You can also suppress the error by not selecting the *Source/Driver* check box.
4. To check that each output pin on the net has sufficient drive for input loading on the net, select the *Net Loading* check box.

   **Note:** To override the net loading check for a pin or a net, attach the `NO_LOAD_CHECK` or the `UNKNOWN_LOADING` property to it. You can also suppress the error by not selecting the *Net Loading* check box.
5. To check that each pin in the design is defined as input, output, or bi-directional, select the *Pin Direction* check box.

   **Note:** To override the pin direction check for a pin or a net, attach the `NO_DIR_CHECK` property to it. You can also suppress the error by not selecting the *Pin Direction* check box.
6. To perform electrical rule checks, click the *Run* button.

A new report file, `erc.rpt`, containing a summary of violations, severity levels, and directive settings is produced. You can select the *View* button to open the `erc.rpt` file and view it.

## Generating Netlist Reports

You can use the Netlist Reports dialog box to view or generate netlist reports. You can also select the format in which you would like a report to appear.

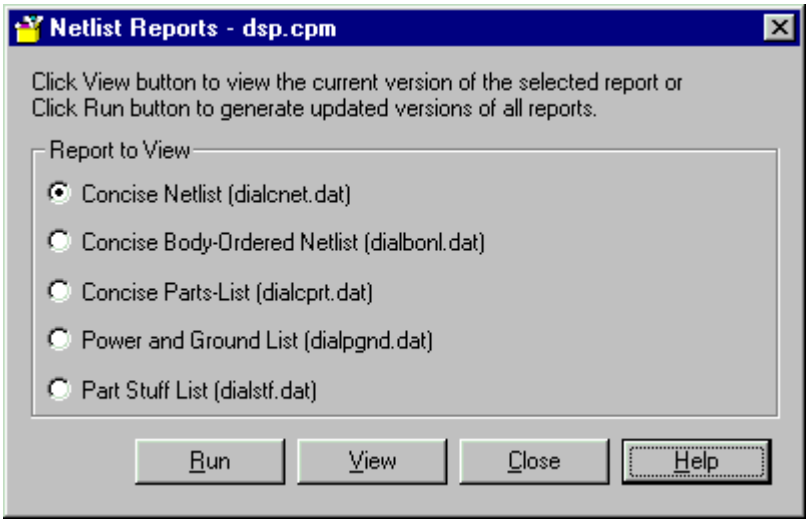
**Note:** Before generating netlist reports, you must have packaged your design to obtain the required netlist files: `pstchip.dat`, `pstxprt.dat`, and `pstxnet.dat`.

To generate a netlist report:

1. Launch the Netlist Reports dialog box by using one of the following methods:
   - Choose *Tools - Packager Utilities - Netlist Reports* in Project Manager.
   - Choose *Tools - Packager Utilities - Netlist Reports* in the Design Entry HDL schematic editor.

   The Netlist Reports dialog box appears. See Netlist Reports Dialog Box on page 104.

**Figure 4-19 Netlist Reports Dialog Box**




2. To list the nets in the design that have a minimum of two nodes, select the *Concise Netlist (dialcnet.dat)* radio button. The `dialcnet.dat` file stores the concise netlist. This file is ordered by nets.
3. To list the nets in the design that have a minimum of two nodes that are ordered by physical part designator (body) information, select the *Concise Body-Ordered Netlist (dialbonl.dat)* check box.
4. To list the part types used in the design and their quantities, select the *Concise Parts List (dialcprt.dat)* check box.

5. To list the physical part designators for each part type used in the design and their power and ground pins, select the *Power and Ground List (dialpgnd.dat)* check box.
6. To list the part types used in the design and their reference designators, select the *Power and Ground List (dialstf.dat)* check box.
7. To generate the selected reports, click the *Run* button.
8. To view the current version of any report file you selected (for example, the Concise netlist `dialcnet.dat` file), click the *View* button.
9. To close the Netlist Reports dialog box, click the *Close* button.

## Viewing Any File

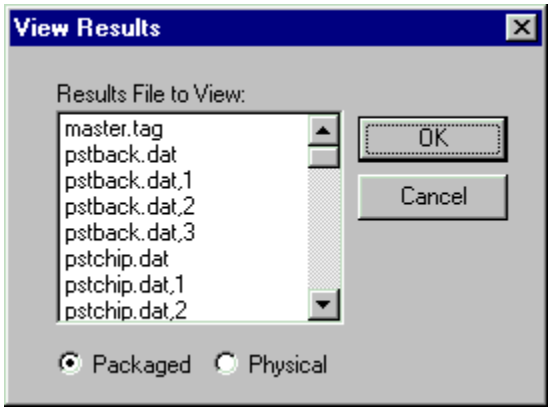
You can view any file in the `packaged` view (created by Packager-XL) or the `physical` view (created by PCB Editor or SI) by using the View Results dialog box.

To view any file,

1. Choose *Tools - Packager Utilities - View Result*.

   The View Results dialog box appears.

**Figure 4-20 View Results Dialog Box**




2. Select the *Packaged* or *Physical* radio button based on whether you want to see the view files from the `packaged` view directory or from the `physical` view directory. The default option is *Packaged*.
3. Highlight the file that you need to view from this list (for example, `*view.dat`, `*.mkr`, `*.log`, and so on from the `packaged` view or `*.log`, `*.brd`, `*.jrl`, and so on from the `physical` view) and click *OK*.

The selected file is displayed in a text editor. You can use the text editor to edit or print the file.

4. To close the View Results dialog box without viewing any file, click the *Cancel* button.

# 5

# Resolving Design Differences

## Overview

The development of any design involves an iterative process of synchronizing the differences between the schematic and the board. Changes especially caused by Engineering Change Orders (ECOs) are made in the schematic and need to be updated in the board. Similarly, changes in the board such as reference designator changes and section and pin swaps require updating the board.

You can use the Design Differences tool (also called Visual Design Differences or VDD) to compare the Logical View (that is the packaged representation of the design) and the Physical View (that is the connectivity representation of the layout design) and list the differences. The differences listed by the Design Differences tool includes the following:

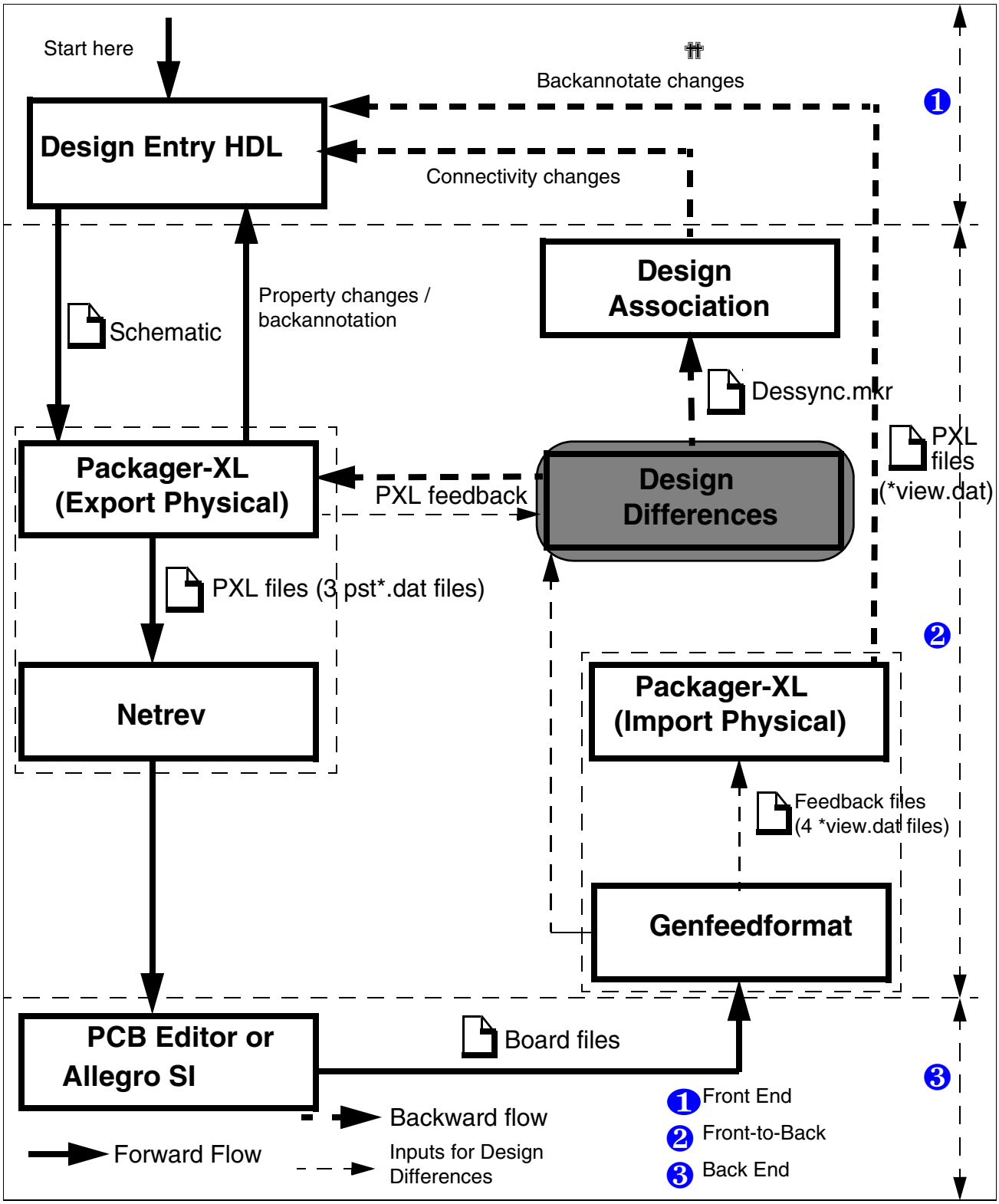
- Net, instance, instance part (reference designator), and pin connectivity differences
- Property differences for instances, nets, or pins
- Swapping differences for functions, pins, or reference designators

You can use the Design Differences tool to synchronize any of the above differences.

## How the Design Differences Tool Fits in the Front-to-Back Flow

The Design Differences tool fits in the middle of the front-to-back flow. It uses the files produced by Packager-XL in the Forward mode (the PXL files) and the feedback files generated by Genfeedformat to obtain the property and connectivity differences between the schematic and the board. Design Differences updates the property changes in the board back to the schematic. Design Differences also generate the `dessync.mkr` file, which lists the connectivity differences between the schematic and the board. This file is used by Design Association to backannotate the connectivity differences to the schematic. For more details, see Design Differences: Traditional Flow on page 108.

**Figure 5-1 Design Differences: Traditional Flow**



You can make changes in PCB Editor and then feed back the property changes to the schematic by generating the feedback files using genfeedformat.

You can then use the VDD tool to update the property changes either to the board or to the schematic. When you run VDD, it displays differences in properties between the schematic and the board in multiple windows.See Differences View Windows: Traditional Flow on page 117 for more information about difference windows.

To update the connectivity changes made in the board to the schematic, use the DA tool. DA uses a file generated by VDD named `dessync.mkr` (which captures connectivity information) to guide you in updating the schematic.

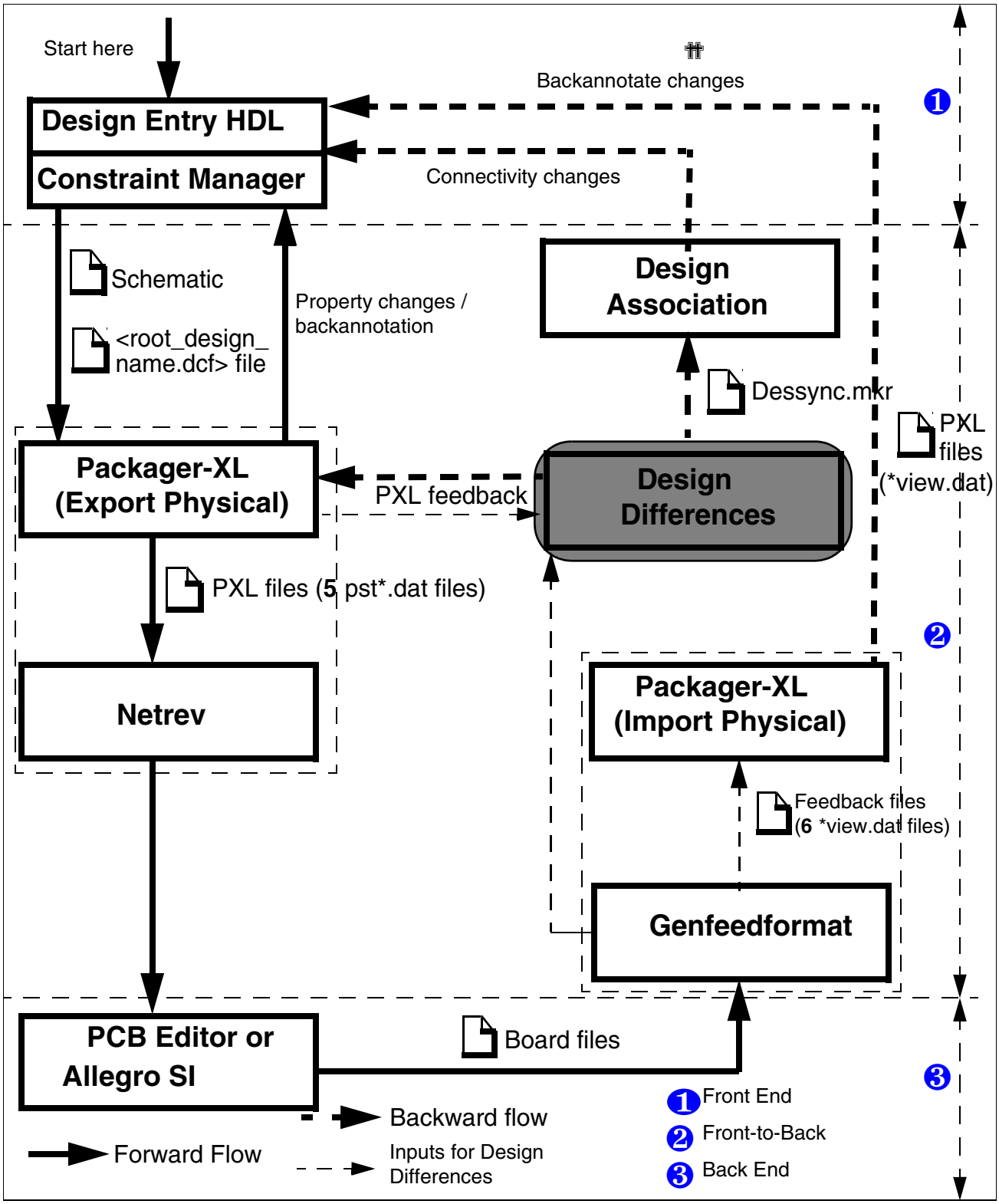
**Note:** While the Design Synchronization toolset helps you synchronize logical-to-physical design differences, it does not allow you to synchronize logical-to-logical or physical-to-physical differences. This implies that you cannot synchronize two schematics or two boards with the Design Synchronization toolset.

You can use the Property Flow Setup dialog box to define the properties that should be transferred between the board and the schematic. The improved property flow allows Design Differences to have a smoother run as it has to capture fewer property mismatches.

## Design Synchronization Flow: Constraint Manager-Enabled Flow

The primary difference between design synchronization flow in the traditional flow and the Constraint Manager-enabled flow is the use of Constraint Manager for managing electrical constraints. If you use Constraint Manager in Design Entry HDL to manage electrical constraints, then Constraint Manager dumps information about electrical constraints in a new view named constraints under the root design. This view includes a file named <*root_design*>.dcf, which contains a snapshot of electrical constraint information in the design.

**Figure 5-2 Design Differences: Constraint Manager-Enabled Flow**



# Design Differences Functions

The Design Differences tool does the following:

- Generates differences between the logical and physical views and lists them
- Filters specific differences so that you can view differences of specific interest
- Displays the objects in the entire logical and physical design as a hierarchical tree composed of components, nets, and parts
- Generates the `dessync.mkr` file, which captures connectivity change information and is used by the Design Association tool to backannotate physical connectivity changes to the Design Entry HDL schematic
- Queries on a design by part name, reference designator, net name, and property name-value pairs
- Cross-probes instances, nets, and pins on a Design Entry HDL schematic design, or an PCB Editor board, or a SI layout design to display the source of the differences
- Synchronizes either the logical design or the physical design based on where you want to accept the individual differences

# Running Design Differences

To run Design Differences, complete the following steps:

1. The first step in opening the Design Differences tool is to load the Design Differences dialog box. You can load the Design Differences dialog box using one of the following three methods:

   **a.** Choose *Project Manager - Tools - Design Sync - Design Difference*.

   **b.** Choose the *Design Sync* icon in Project Manager and select *Design Differences*.

   **c.** Choose *Design Entry - Tools - Design Difference*.

   The `Design Differences` command finds differences between the board (physical data in the PCB Editor or SI layout) and the schematic (logical data in the Design Entry HDL schematic) when they are “out of sync”. To run the `Design Differences` command, you use the Design Differences dialog box. Design Differences may run in two modes, Non-CM and CM.

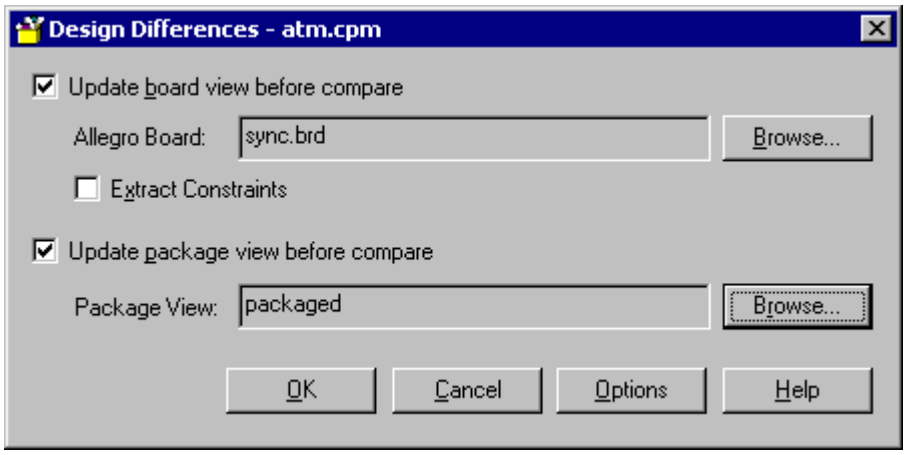
   - **Traditional flow**: This is the default flow. In this flow, Design Differences does not distinguish electrical properties differences from other properties and displays the

differences between the schematic and the board in the net and properties difference windows.

The traditional flow is selected when <*root_drawing*>.dcf file is not found in the constraints view and none of the pstcmdb.dat or cmbcview.dat or cmdbview.dat files are present in the packaged view.

The Figure 5-3 on page 112 displays Design Differences dialog box in the traditional flow.

**Figure 5-3 Design Differences Dialog Box: Traditional Flow**

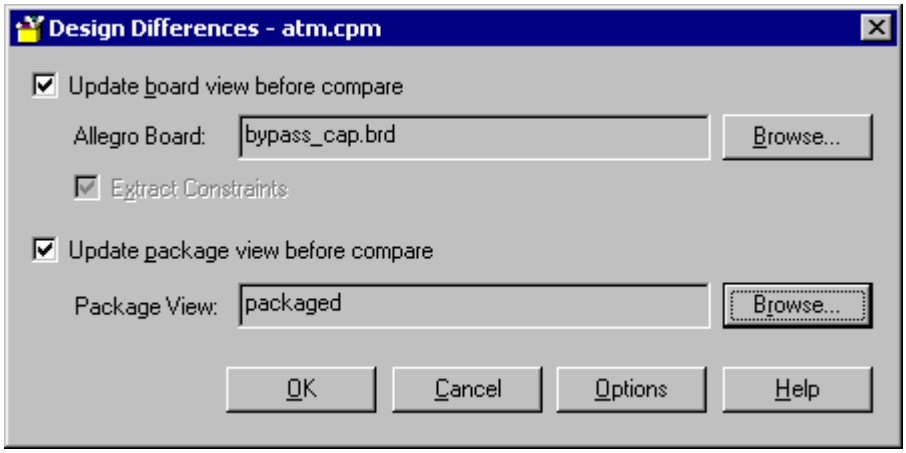



- **Constraint Manager-enabled flow**: In the Constraint Manager-enabled flow, Design Differences displays constraint differences in two new Constraints Differences windows, one each for logical and physical domain. Any constraint property differences are filtered from the net-properties difference windows and displayed in the new windows.

  The Constraint Manager-enabled flow is selected when <*root_drawing*>.dcf file is found in the constraints view or the pstcmdb.dat or cmbcview.dat or cmdbview.dat files are present in the packaged view.

The Figure 5-4 on page 113 displays the Design Differences dialog box in the Constraint Manager-enabled flow.

**Figure 5-4 Design Differences Dialog Box: Constraint Manager-Enabled Flow**




2. The *Update board view before compare* check box is deselected by default. To re-extract the physical view from the layout before generating the design differences, select this check box. If the *Update board view before compare* check box is selected, the default board name appears in the *PCB Editor Board* field.

3. To select a different board than the default, select *Browse* next to the *PCB Editor Board* field and browse to the file.

4. To switch to the Constraint Manager-enabled flow from the traditional flow, select the *Extract Constraints* check box. When you select the *Extract Constraints* check box, Design Differences filters constraint property differences from the net-properties difference windows and displays them in the Constraints Differences windows.

5. The *Update package view before compare* check box is deselected by default. To repackage the logical view from the schematic before generating the design differences, select this check box. If the *Update package view before compare* check box is selected, the default packaged view appears in the *Package View* field.

6. To select a different view than the default, select *Browse* next to the *Package View* field and browse to the file.

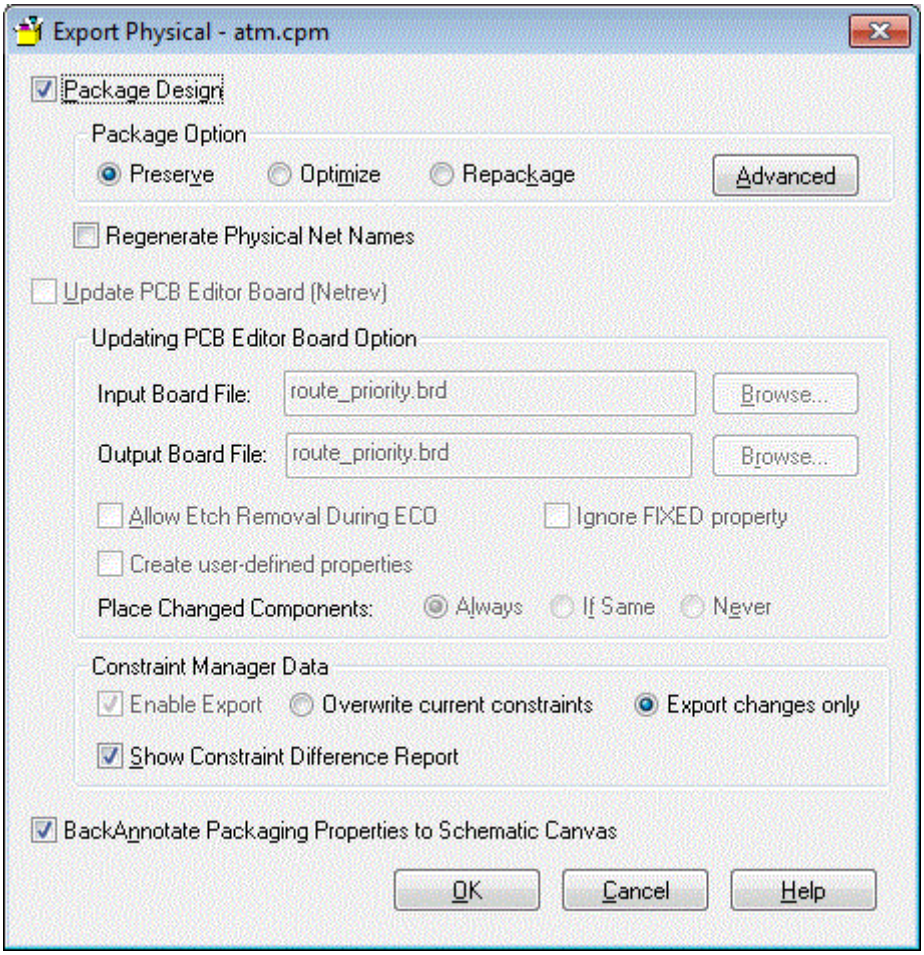
7. To compare the differences, click *OK*.

   The Progress window appears.

   When you run Design Differences with the Update package view before compare check box as selected, Design Differences calls Export Physical in a special mode (see Export Physical: Design Differences Mode figure on page 114) where the Update PCB Editor Board option is grayed. You can then package and/or backannotate the design. Based on your selection, Export Physical will run. When Export Physical has completed its

operation, control is passed back to the Design Differences progress window. Design Differences will complete its progress and display difference windows.

**Figure 5-5 Export Physical: Design Differences Mode**




8. Click *OK*.

   After Export Physical completes its operation, it passes the control back to the Design Differences tool. The *Design Differences* window appears displaying multiple difference view windows based on the property and connectivity differences in the design.

# Design Differences User Interface

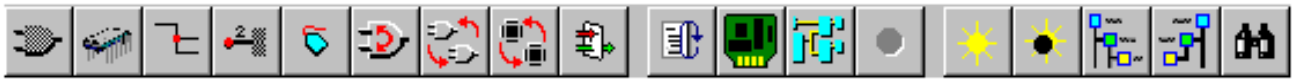
The Design Differences tool supports a simple, intuitive graphical user interface for displaying differences between the schematic and the layout. This user interface consists primarily of a menu bar, a toolbar, and multiple design differences view windows.

## Design Differences Toolbar

The Design Differences window includes a toolbar with 18 tool buttons. These toolbar icons provide quick access to Design Differences functions.

The figure below displays the Design Differences toolbar.

**Figure 5-6 Design Differences Toolbar**




The toolbuttons that are grayed out, such as the toolbutton corresponding to the number 13, are inactive. If you place the pointer over a toolbutton, a descriptive label will appear.

The table below describes the function of each toolbutton.

**Table 5-1 Design Differences Toolbar: Description**

| S No. | Label | Function |
|---|---|---|
| 1 | Instance Difference | Executes the `Difference - Instance` command and displays the Instance Difference window. |
| 2 | Instance Part Difference | Executes the `Difference - Instance Part` command and displays the Instance Part Difference window. |
| 3 | Net Difference | Executes the `Difference - Net` command and displays the Net Difference window. |
| 4 | Pin Connection Difference | Executes the `Difference - Pin Connection` command and displays the Pin-Net Connection Difference window. |

| S No. | Label | Function |
|---|---|---|
| 5 | Property Difference | Executes the `Difference - Instance Property` command and displays the Instance Property Difference window. |
| 6 | Pin Swap | Executes the `Difference - Pin Swap` command and displays the Pin-Swapping Difference window. |
| 7 | Section Swap | Executes the `Difference - Section Swap` command and displays the Section-Swapping Difference window. |
| 8 | RefDes Rename | Executes the `Difference - RefDes Rename` command and displays the RefDes Difference window. |
| 9 | Filter Options | Executes the `Difference - Filter Options` dialog box and displays the Filter Options for Difference dialog box. |
| 10 | Update Differences | Executes the `File - Update Differences` command and displays the updated difference view windows when differences exist between the schematic and the layout. |
| 11 | Update Board | Executes the `Sync - Update Allegro Board` command and displays the Preview ECO on PCB Editor Board dialog box. |
| 12 | Update Schematic | Executes the `Sync - Update Design Entry Schematic` command and displays the Preview ECO on Schematic dialog box. |
| 13 | Stop | Executes the `File - Stop Loading` command and stops reloading the Design Entry HDL schematic design or the PCB Editor or SI board layout. |
| 14 | Highlight | Executes the `Display - Highlight Source` command and highlights the element causing the difference in the schematic and the board. |
| 15 | Dehighlight | Executes the `Display - Dehighlight Source` command and removes the highlight from the element causing the difference in the schematic and the board. |
| 16 | Explore (Logical) Design | Executes the `Explore - Logical Design` command and displays the Logical Design View window. |

| S No. | Label | Function |
|---|---|---|
| 17 | Explore (Physical) Design | Executes the `Explore - Physical Design` command and displays the Physical Design View window. |
| 18 | Query Design | Executes the `Explore - Query Design` command and displays the Query Design window. |

## Design Differences Windows

### Differences View Windows: Traditional Flow

Design Differences displays the difference between the logical database and the physical database in difference view windows. There are ten difference view windows in the traditional flow.

- Instance Difference View window
- Instance Part Difference View window
- Instance Property Difference View window
- Net Difference View window
- Net Property Difference View window
- Pin Property Difference View window
- Pin-Swapping Difference View window
- Pin-Connection Difference View window
- Section-Swapping Difference View window
- RefDes-Swapping Difference View window

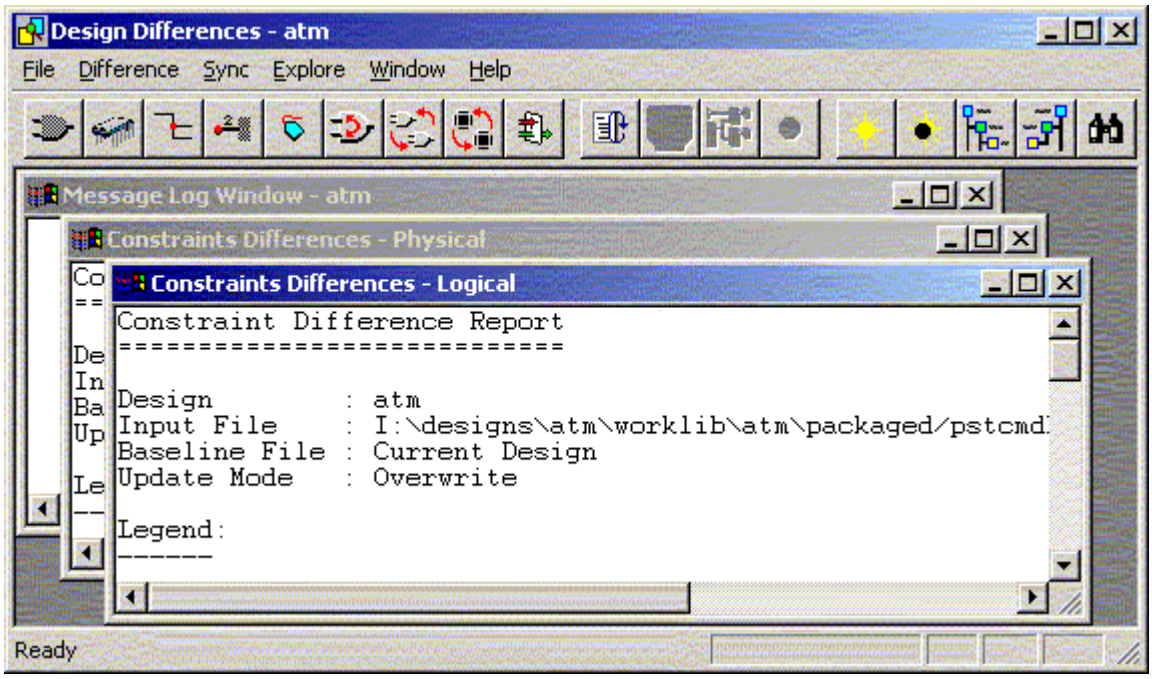
The following generic features apply to all of the above-mentioned difference view windows:

- The titlebar of every difference view window displays the name of the difference view, the design name corresponding to the logical Design Entry HDL schematic, and the layout name of the layout database to which it is being compared.
- Design Differences displays a difference view window only if differences exist between the schematic and the layout. If the logical design in the Design Entry HDL schematic and the physical design in the PCB Editor or SI layout do not have any differences, Design Differences displays this in a message box.

- Each column in a difference view window identifies the information related to the differences between the logical and physical views while each row displays the differences.
- Sometimes, a column in a window might display a partial value. If this happens, place the pointer on the column-header title and drag the column header outline to the right to display the full value.
- Each difference view window lets you arrange all differences in an alphabetical order. For this, you need to click the column header corresponding to the column on which you want to sort properties.
- You can highlight or dehighlight any instance, component, net, or pin in a Design Entry HDL schematic or an PCB Editor or SI layout.

### Differences View Windows: Constraint Manager-Enabled Flow

In the Constraint Manager-enabled flow, besides the above difference view windows, two more difference view windows exist. These are Constraints Differences - Physical Difference View window and Constraints Differences - Logical Difference View window.




- Constraints differences are displayed in the following format:

```
Net: <net_name>
     <constraint name>  (<new value>) (<old value>) (*<original value>*)
```

- Object differences are displayed in the following format:

  ```
  <object> association  (<new association>) (<old association>) (*<original association>*)
  ```

- "Clearing" an object implies that all electrical constraints captured on the object have been deleted.

The `Summary` section displays the summary of constraint and object differences between the schematic and the board.

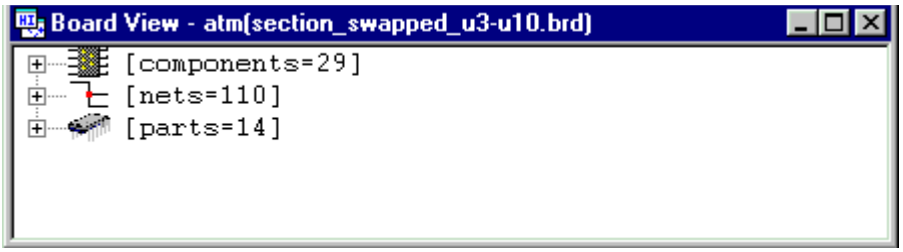
**Note:** For more information about Constraints Differences windows, see *Allegro Design Entry HDL User Guide* in CDSDoc.

### Physical Design View Window

The Physical Design View window displays the objects in the physical view of the design as hierarchical trees. To display the Physical Design View window, choose *Explore - Physical Design*.

There are three hierarchical trees, one each for components, nets and parts. By default, a hierarchical tree is not expanded. The root node of a component, net, or part hierarchical tree displays a number signifying their total number in the design. For example, `components=29` in the root node of the component tree signifies that there are 29 components in the design.

**Figure 5-7 Physical Design View Window: Unexpanded**

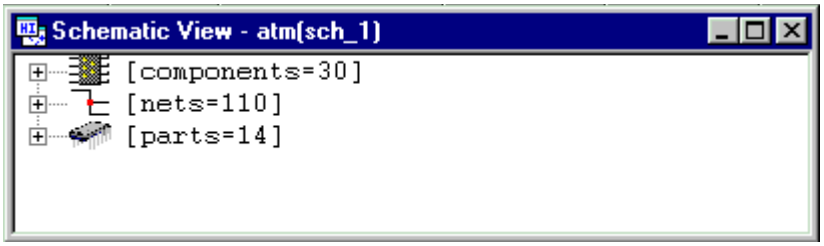



### Logical Design View Window

The Logical Design View window displays the objects in the logical view of the design as hierarchical trees.

There are three hierarchical trees, one each for components, nets, and parts. By default, none of these trees are expanded. The root node of the component, net, or part hierarchical tree displays a number signifying their total number in the design. For example, nets=108 signifies that there are 108 nets in the design.

**Figure 5-8 Logical Design View Window: Unexpanded**




### Rearranging Windows

If there are multiple open windows in Design Differences, you might like to rearrange them for better viewing. You can rearrange a window in any of the following ways:

1. Choose *Window - Cascade*. This command arranges all the active windows as a cascade. The active window appears at the top of the cascade and the title bars of the other windows are visible beneath it like a cascade.
2. Choose *Window - Vertical Tile*. This command arranges all the active windows vertically (that is each window appears as a column in a single row table).
3. Choose *Window - Horizontal Tile*. This command arranges all the active windows horizontally (that is, each window appears as a row in a single column table).
4. Choose *Window - Arrange Icons*. This command arranges all the icons relating to active windows.
5. Choose *Window - Close All*. This command simultaneously closes all open windows.

# Using Design Differences

## Viewing Any Files

Multiple files are generated when you package a design. You can view any packaging file or any other file in the design from Design Differences. To view any file,

1. To display any file, choose *File - View File*. This displays the Select File dialog box.
2. Use the *Browse* button to navigate to the design directory containing the files you want to see.
3. Choose the required view from the list box containing the cell views of the design.

4. Choose the required file format (`*.dat`, `*.log`, `*.txt`, `*.dif`, or `*.mkr`) from the *Files of type* list box.
5. Click *Open* to display all the files corresponding to the file format you selected.

   The list of files under the selected view directory appears. For example, if you selected the `*.mkr` file format, the `dessync.mkr` and `pxl.mkr` files now appear in the list box.
6. Choose any file from the list box by highlighting the file.

   The name of the file you selected appears in the *File Name* box.
7. Click *Open* to view the file.

   or

   Click *Cancel* if you want to close the Select File dialog box without displaying the file.

### Viewing Errors

You can view errors by either using the Message Log window or by viewing the `dessync.log` or `pxl.log` files. To view any file, refer to Viewing Any Files.

## Viewing the Logical Design

You can display the objects in the logical view of the design as hierarchical trees.

➤ To view the logical design, choose *Explore - Logical Design*.

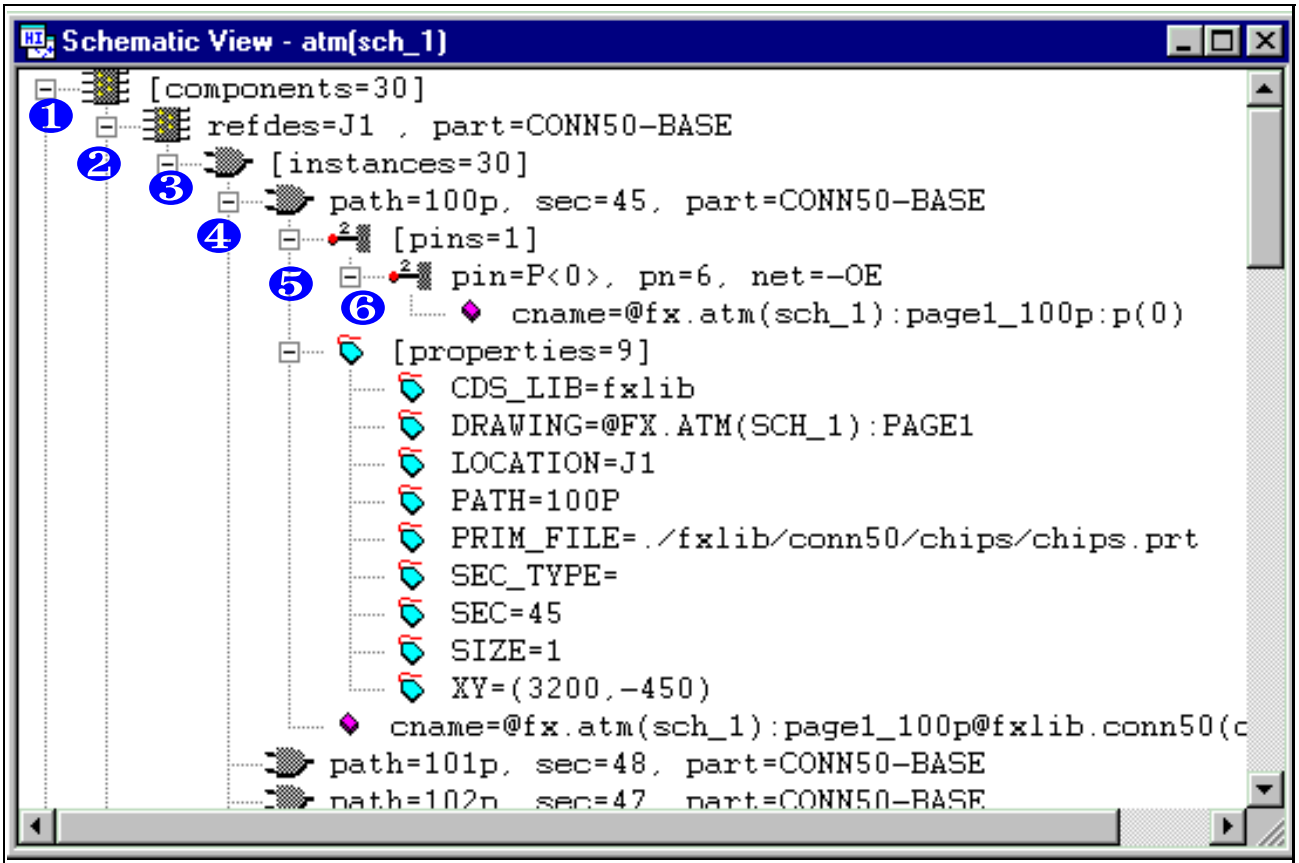
The Logical Design View window displays with the title `<design_name>(<view_name>)`. Logical Design View Window: Unexpanded represents a logical design window. You can expand the hierarchical list to view the details about components, nets, or parts.

A hierarchical tree can run into multiple levels. For example, the components tree in the logical design window is organized into six levels. To expand any level, you can do one of the following two steps:

- Click the + button to the left of the base node of the non-expanded level.
- Double-click the base node of the non-expanded level.

The Logical Design View Window: Expanded Component Tree figure on page 122 displays the expanded components tree. The numbers 1 to 6 represent the actions that you need to complete.

**Figure 5-9 Logical Design View Window: Expanded Component Tree**




1. Click the component tree node to list the reference designator identifying each component and the name of each part together with the `PACK_TYPE` property
2. Click a component tree node to list the number of instances.
3. Click the number of instances node to display the information about the path and section number.
4. Click the tree node corresponding to the path and the section number to display the number of pins and properties attached to the component.
5. Click the tree node corresponding to the total pin number to display the pin name, pin number, and the net name.
6. Click the tree node corresponding to the total properties number to display the instance properties.

See Viewing the Hierarchical List of Components on page 125 for a detailed procedure of expanding components in a hierarchical tree.

## Viewing the Physical Design

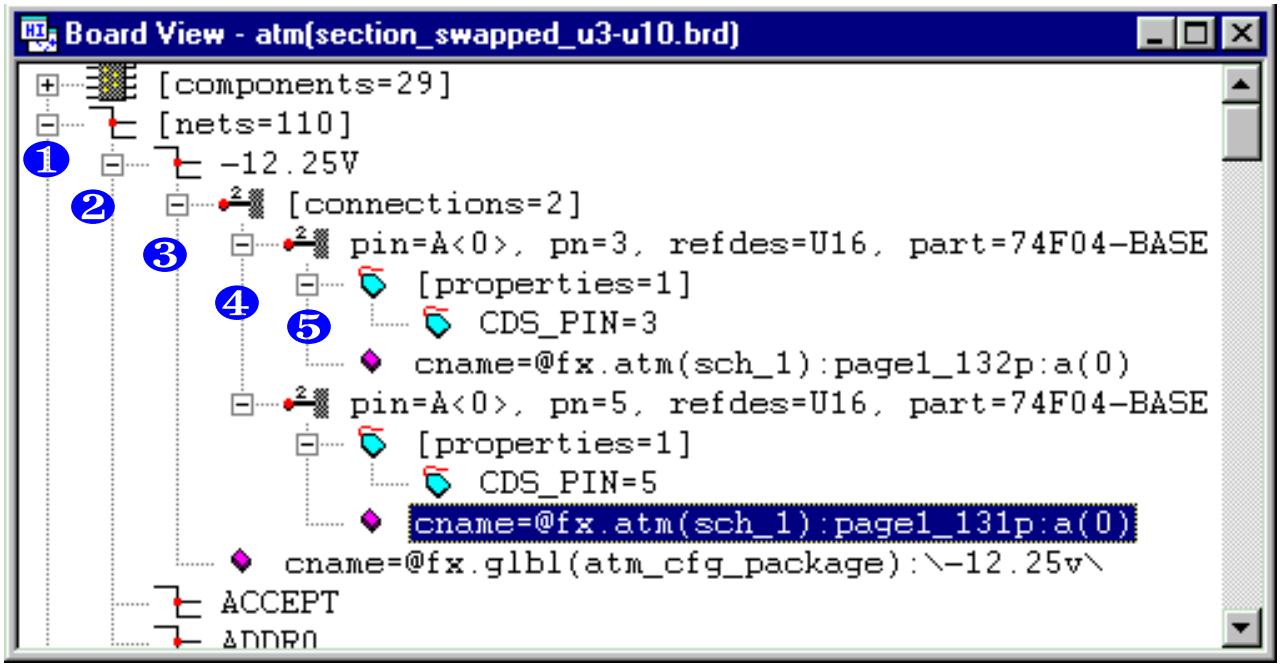
You can display the objects in the physical view of the design as hierarchical trees.

➤ To view the physical design, choose *Explore - Physical Design*.

Physical Design View Window: Unexpanded represents a logical design window displayed by running the above command. The Physical Design View window is displayed in the title `<design_name>(<board_name>`. You can expand the hierarchical list to view the details about components, nets, or parts.

An example of how the hierarchical net tree is expanded in the physical design window appears in Physical Design View Window: Expanded Net Tree on page 124. The numbers one to five represent the actions that you need to complete.

**Figure 5-10 Physical Design View Window: Expanded Net Tree**




1. Click the net tree base node to display the list of all nets.
2. Click the tree node corresponding to a particular net to display the number of net connections and properties and the logical net name.
3. Click the node displaying the number of connections to display the pin name, pin number, reference designator, and the part to which the net is attached.
4. Click the tree node corresponding to a connection to display the hierarchical logical net name.
5. Click the node displaying the number of connections to display the net properties.

See Viewing the Hierarchical List of Nets on page 125 for the detailed procedure of expanding components in a hierarchical tree.

## Viewing the Differences in a Text Editor

You can view the differences in a text editor by sending the differences generated in VDD to a text file.

➤ To view the differences in a text editor, choose *File - Output Differences*.

The differences corresponding to the difference view window that is currently active are displayed in the default text editor. You can either edit or print these differences.

## Viewing Hierarchical Trees

You can view any hierarchical tree by expanding its individual levels.

### Viewing the Hierarchical List of Components

1. Click the components tree node to display the list of reference designators identifying each component and the name of each part together with the `PACK_TYPE` property attached to it.
2. Click the tree node corresponding to a specific component to display the total number of instances related to the component.
3. Click the *<total number of instances>* tree node to display the path and section number related to all instances of the component.
4. Click the tree node corresponding to the path and section number (displayed in the last step) to display the number of pins and properties attached to the component. The hierarchical logical path of the component is also displayed.
5. Click the tree node corresponding to the *[pins = <total number of pins>]* tree node to display the pin name, pin number, and net name.
6. Click the *[properties = <total number of properties>]* tree node attached to the component to display a list of all instance properties attached to the component.

See Logical Design View Window: Expanded Component Tree on page 122 for a detailed diagram that implements the above-mentioned steps.

### Viewing the Hierarchical List of Nets

1. Click the tree node corresponding to *[nets = <total number of nets>]* to display the list of all nets in the alphabetical order.
2. Click the tree node corresponding to a specific net to display the number of net connections, the number of properties, and the hierarchical, logical net name.

3. Click the tree node corresponding to *[connections = <total number of connections>]* to display the pin name, the pin number, the reference designator, and the part to which the net is attached.
4. Click the tree node corresponding to each individual connection in the tree to display the hierarchical logical pin name.
5. Click the tree node corresponding to *[properties = <total number of properties>]* for this net to display the net properties.

See Physical Design View Window: Expanded Net Tree on page 124 for a detailed diagram that depicts the above-mentioned steps.

### Viewing the Hierarchical Listing of Parts

1. Click the tree node corresponding to *[parts = <total number of parts>]* to display the list of all the parts in the design.
2. Click the tree node corresponding to one specific part to display the total number of components of the part, the total number of pins in the part, and the total number of properties attached to the part.
3. Click the tree node corresponding to *[components = <total number of components>]* to display the reference designators identifying the components.
4. Click the tree node corresponding to any reference designator to display the total number of instances and the total number of properties attached to the reference designator.
5. Click the tree node corresponding to *[instances = <total number of instances>]* to display the part, the section number, and the part name for each of the instances of the part.
6. Click the tree node corresponding to any instance to display the total number of pins, the total number of properties, and the canonical path name of the instance.
7. Click the tree node corresponding to any pin attached to the selected instance to display the pin name, the pin number, and the net name corresponding to the instance.
8. Click the tree node corresponding to the properties of the instance to display the instance properties.
9. Expand the tree node at the *[pins = <total number of pins>]* level to display the pin names of the part.

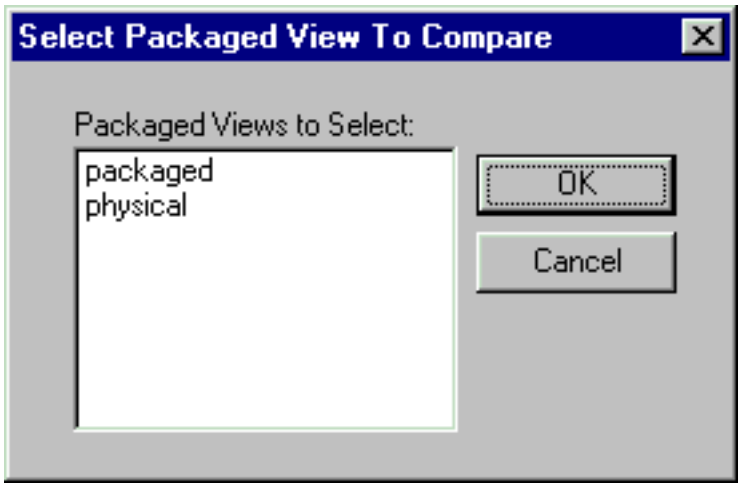
## Loading the Design Views

### Loading the Design Entry HDL Schematic

1. To load the Design Entry HDL schematic, choose *File - Load Design Entry Schematic.*

   The Select Packaged View To Compare dialog box appears listing the `packaged` views that you can choose.

**Figure 5-11 Select Packaged View To Compare Dialog Box**




2. If you click *OK* without highlighting the packaged view that you want to compare, a Design Differences window appears with the Caution symbol. This window displays the warning that you have not selected any packaged view.

   Design Differences repackages the updated schematic design, reloads the logical view from the updated schematic, and displays a window with the message “Reload schematic has successfully completed.”

3. Click *OK*.

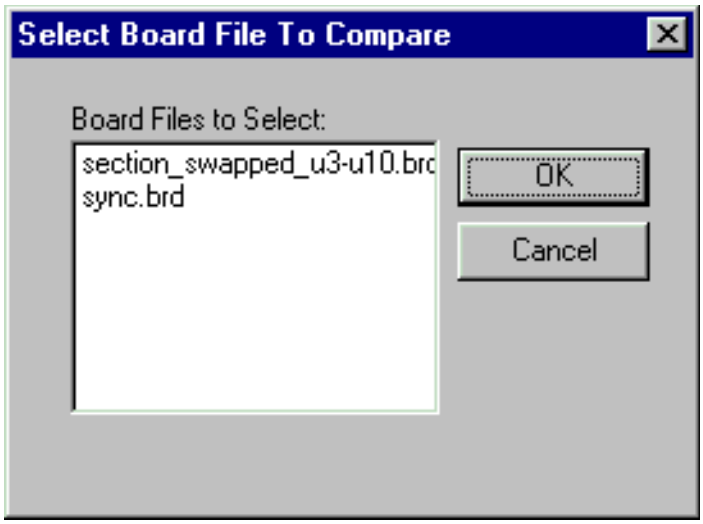
The difference view windows are displayed. These windows list any differences that were found between the regenerated packaged view of the Design Entry HDL schematic and the PCB Editor or SI layout view.

### Loading the PCB Editor Layout

1. To load the PCB Editor layout, choose *File - Load PCB Editor Board*.

The Select Board File To Compare dialog box appears listing the board files that you can choose.

**Figure 5-12 Select Board File To Compare Dialog Box**




2. In the `layout` view, select the board file that you want to compare with the packaged view in the schematic and click OK.

   **Note:** You may click Cancel if you do not want to compare any board file in the layout view with the `packaged` view in the schematic.

Design Differences re-extracts the physical layout design, reloads the `physical` view from the layout, and displays a window with the message “Reload PCB Editor Board has successfully completed.” Clicking *OK* on this window displays the difference view windows. These windows list any differences found between the regenerated PCB Editor layout physical view and the packaged logical view of the Design Entry HDL schematic.

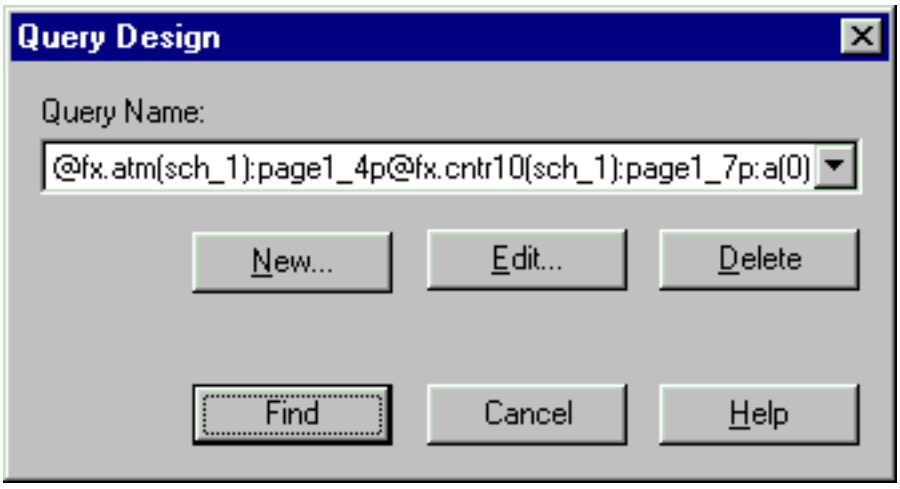
## Querying a Design

### Querying for a new instance, component, net, pin, or property

1. To display the Query Design dialog box, choose *Explore - Query Design*.

   The Query Design Dialog Box figure on page 129 appears.

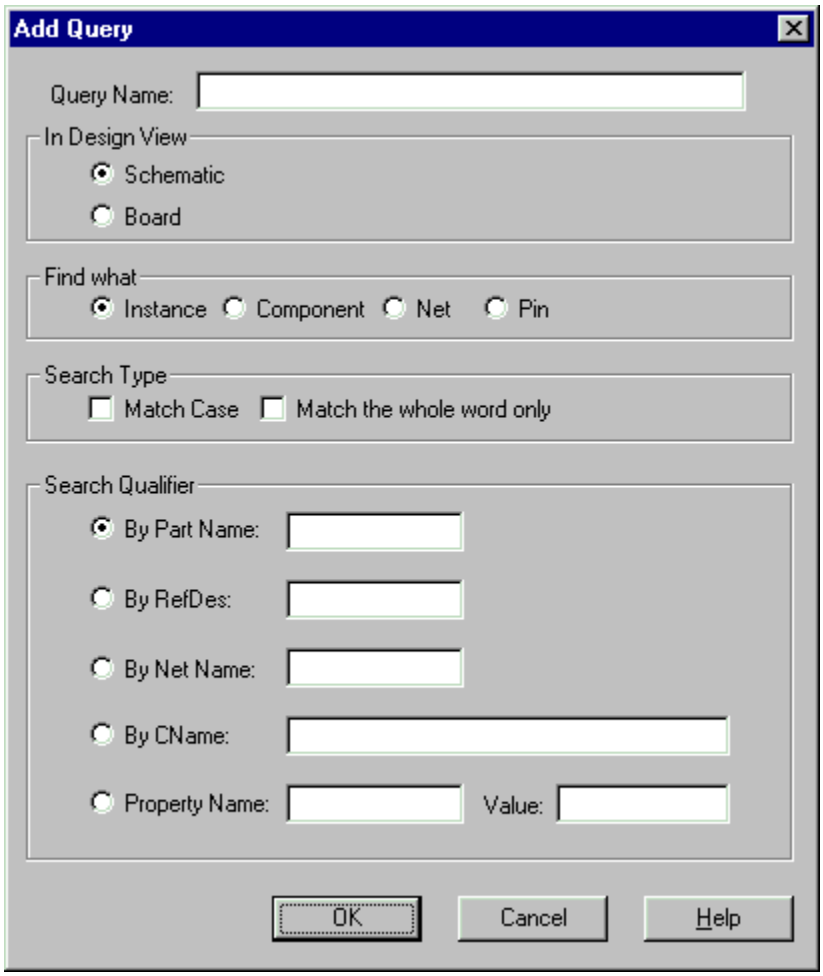
**Figure 5-13 Query Design Dialog Box**




**2.** Click *New*.

The Add Query dialog box appears. You can use this dialog box to search for any instance, component, net, or pin in the schematic or the board.

**Figure 5-14 Add Query Dialog Box**




3. Enter the name of the instance, component, net, pin, or property that you want to search for in the *Query Name* field.
4. Depending on whether you want to select the object in the logical design or in the physical design, click the *Schematic* or *Board* radio button.
5. In the *Find What* group box, specify whether you are searching for instance, component, net, or pin by clicking the respective radio button.
6. In the *Search Type* group box, select either the *Match Case* radio button or the *Match the whole word only* radio button. If the instance name, component name, net name, pin name, or property name you are searching for is case-sensitive, select the *Match Case* radio button. If you want a whole-word search, select the *Match the whole word only* radio button.

7. In the *Search Qualifier* group box, select an option (By Part Name, By Ref Des, By Net Name, by Property Name, or by Cname) and type in the specific part, reference designator, net name, property name and value, or the canonical path you are searching for.
8. Click *OK*.

   The Query Design dialog box reappears with the *Query Name* field showing the name of the instance, component, net, pin, or property you are querying.
9. Click *Find*.

   The *Query Board- <query name> or Query Schematic - <query name>* window appears with a list of all the instances, components, nets, or pins in the logical or physical design that matches the query.
10. To further expand the tree and display the specific location and properties attached to the object, click the tree node corresponding to an object in this list.

### Example

For example, to search for all the parts in the schematic with the `DES` property value of `F6`, display the Add Query dialog box and follow the steps below:

1. Type these selections:

| | |
|---|---|
| **Query Name** | DES |
| **In Design** | Schematic |
| **Find What** | Instance |
| **Search Type** | Match the case |
| **Search Qualifier** | By Part Name<br>By Property: DES Value: F6 |

2. Click *OK* in the Add Query dialog box. The Query Design dialog box appears with `DES` in the *Query Name* field.
3. Click *Find*.

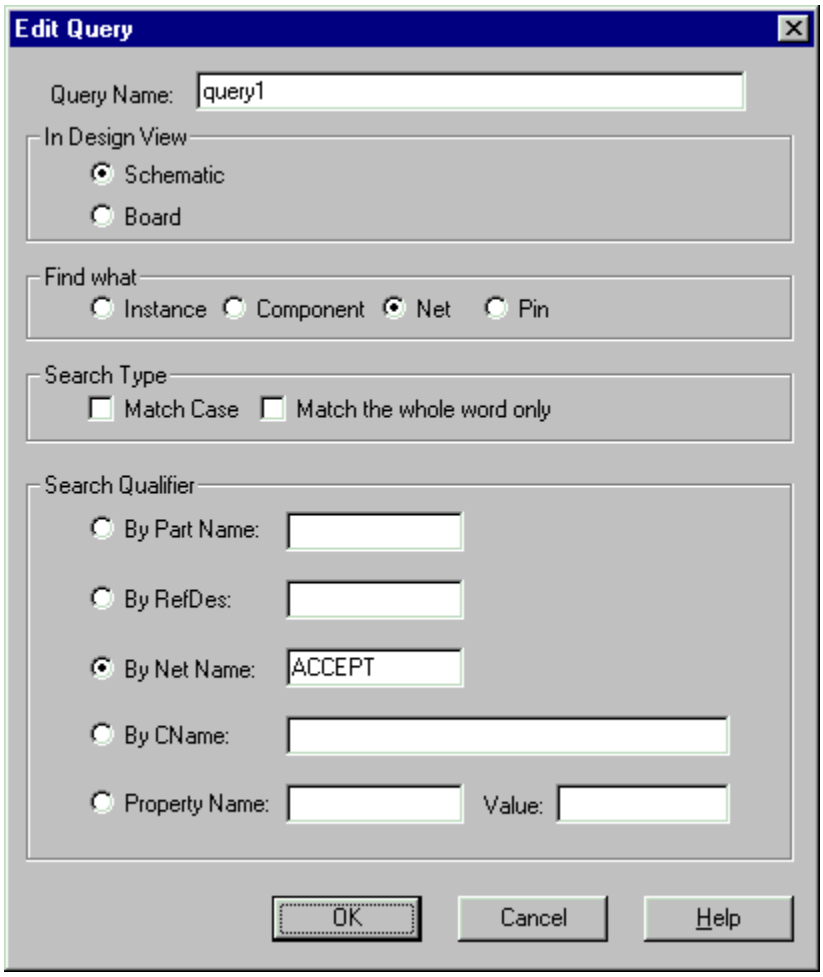
The *Query Logical Design - DES* window appears listing all the parts in the schematic that have the `DES` property value of `F6`.

### Querying for another instance, component, net, pin, or property

1. To display the Edit Query dialog box in which you can edit an existing query, click *Edit* in the Query Design dialog box.

   The Edit Query dialog box appears.

**Figure 5-15 Edit Query Dialog Box**




   The Edit Query dialog box has the same selection options and check boxes as the Add Query dialog box.

2. You can now make any changes in the query. (Steps similar to the steps 3-8 for Querying for a new instance, component, net, pin, or property on page 128).

# Highlighting and Dehighlighting Objects

### Steps to follow before highlighting or dehighlighting objects

Before highlighting an object in a Design Entry HDL schematic and its corresponding graphical element in the PCB Editor or SI layout, you need to select a difference displayed in any of the following windows or dialog boxes:

- Difference view window
- Query Schematic and Query Board windows
- Preview ECO on PCB Editor Board or Preview ECO on Schematic dialog box

**Note:** Neither the menu command nor the alternative steps given below will work unless you have selected a difference in any of the above-mentioned windows.

### Highlighting Objects

To highlight the object source corresponding to the selected difference:

➤ Choose *Display - Highlight Source* from the Design Differences menu bar.

The Design Differences tool automatically opens up the corresponding page in the Design Entry HDL schematic design and highlights its source. If a match for the graphical element corresponding to the object being highlighted exists in the PCB Editor or SI layout, the object is also highlighted.

You can use the following alternative steps to highlight an object:

1. Position the pointer in any of the following windows or dialog boxes:
   - Difference view window
   - Query Schematic and Query Board windows
   - Preview ECO on PCB Editor Board or Preview ECO on Schematic dialog box
2. Choose the instance, component, net, or pin difference whose source you need to highlight.
3. Click the right mouse button on the selected object.

   or

   Double-click the selected object.

A pop-up menu with two commands, *Highlight Source* and *Dehighlight Source,* appears.

4. Choose *Highlight Source*.

The selected object is highlighted in the logical view. Its corresponding graphical element in the physical view is also highlighted if a corresponding match exists.

## Dehighlighting Objects

### *To dehighlight using the menu command*

To dehighlight the object source corresponding to the difference you selected:

➤ Choose *Display - Dehighlight Source* from the Design Differences menu bar.

Design Differences automatically opens up the corresponding page in the Design Entry HDL schematic design and dehighlights its source. Its corresponding graphical element in the PCB Editor or SI layout is also dehighlighted if a corresponding match exists.

### *Alternative steps to dehighlight (without using the menu command)*

1. Position the pointer in any of the three windows listed below:
   - ❑ Difference view window
   - ❑ Query Logical Design or Query Physical Design window
   - ❑ Preview ECO on PCB Editor Board or Preview ECO on Schematic dialog box
2. Choose the instance, component, net, or pin difference whose source you need to highlight.
3. Click the right mouse button on the selected object.

   or

   Double-click the selected object.

   A pop-up menu with the *Highlight Source* and *Dehighlight Source* options appears.
4. Choose *Dehighlight Source*.

The selected object is dehighlighted in the logical view. Its corresponding graphical element in the physical view is also dehighlighted if a corresponding match exists.

### Regenerating Difference Views

➤ To repackage the schematic, update the schematic view (logical view), and regenerate the differences, and choose *File - Load Design Entry Schematic*.

-or-

To re-extract differences from the PCB Editor or SI layout, update the layout view (physical view), regenerate the differences, and choose *File - Load PCB Editor Board*.

**Note:** In case you change the schematic or board while in VDD, you can view the effect by reloading the schematic or board.

### Previewing ECO on PCB Editor Board

The Preview ECO on PCB Editor Board dialog box displays the list of the connectivity changes and property changes that need to be made on the physical view to update the layout and synchronize the layout database with the Design Entry HDL schematic design.

➤ To display the Preview ECO on PCB Editor Board dialog box, choose the *Sync - Update PCB Editor Board* command from the Design Differences menu bar.

### Previewing ECO on Schematic

You can use the Preview ECO on Schematic dialog box to list the properties, instances, or nets that need to be modified in the logical view to update the schematic and to synchronize the Design Entry HDL schematic design with the layout database.

➤ To display the Preview ECO on Schematic dialog box, choose the *Sync - Update Schematic* command from the Design Differences menu bar.

## Synchronizing Difference Views

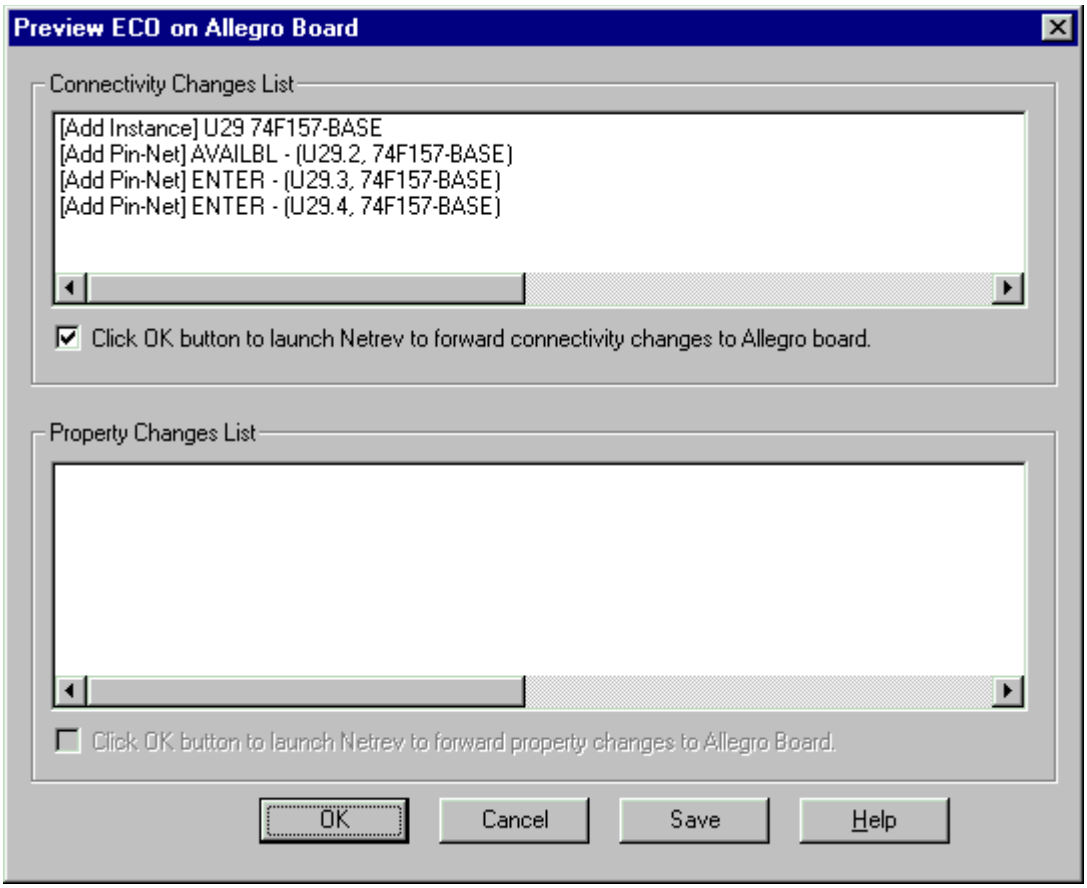
You synchronize the difference views by accepting or rejecting ECO changes in the schematic and the layout. ECO changes are often made in the schematic or the layout after the initial transfer of packaging information from the schematic to the layout. You can preview ECOs and use the information contained in them to bring the schematic and the layout in sync.

### Synchronizing the Board Layout

1. Choose *Sync - Update PCB Editor Board* from the Design Differences menu bar.

The Preview ECO on PCB Editor Board dialog box appears with the list of property and connectivity changes to be made to the layout.

**Figure 5-16 Preview ECO on PCB Editor Board Dialog Box**




2. By default, the connectivity or the property changes, if any, are forwarded to the PCB Editor board layout. If you do not want to forward either the connectivity changes or the property changes to the PCB Editor board layout, clear the *OK* check box under the relevant list.

   **Note:** If connectivity changes or property changes do not exist, the check box corresponding to them is grayed out.

3. Click the *OK* button to update the layout with the listed connectivity and property changes.

   The Message log in the Design Differences window is updated. A message box appears asking if you want to update difference views.

4. Click *Yes*.

A message box appears stating that the PCB Editor board has been successfully reloaded.

5. Click *OK*.

   A message box appears stating that no differences exists between the board and the schematic.

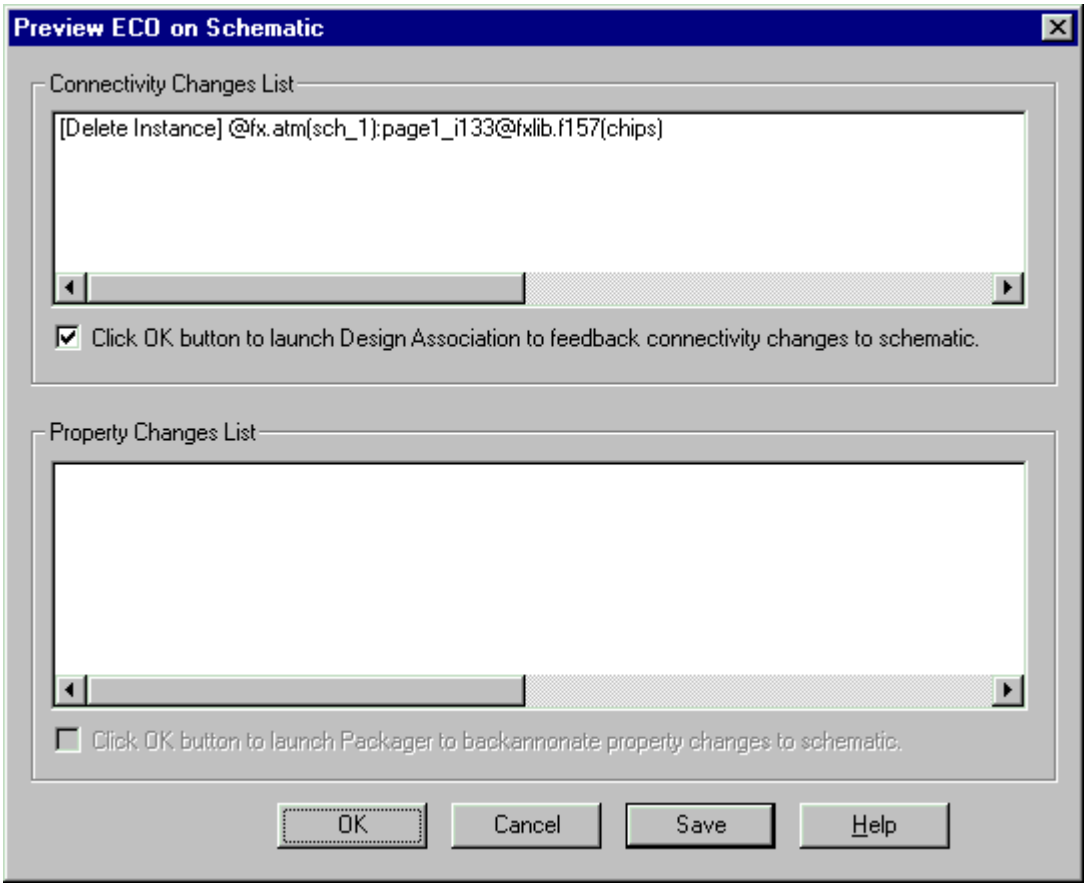
6. Click *OK* to close the message box.

### Synchronizing the Design Entry HDL Schematic

1. Choose *Sync - Update Design Entry Schematic* from the Design Differences menu bar.

   The Preview ECO on Schematic Dialog Box on page 138 appears with two list boxes containing the lists of property and connectivity changes to be made to the Design Entry HDL schematic.

**Figure 5-17 Preview ECO on Schematic Dialog Box**




2. By default, the property and connectivity changes, if any, are fed back to the schematic. If you do not want to backannotate the connectivity changes to the Design Entry HDL schematic, clear the *OK* check box under the *Connectivity Changes* list box. This will not launch Design Association to feed back the property changes to the schematic.

   -or-

   If you do not want to launch Packager-XL to backannotate the property changes to the Design Entry HDL schematic, clear the *OK* check box under the *Property Changes* list box.

   **Note:** By default, the check boxes for property changes and connectivity changes are selected. If there are no connectivity changes or property changes, then the check box corresponding to them are grayed out.

   The Message log in the Design Differences window is updated and the Import Physical dialog box is displayed.

3. Click *OK*.

A Progress Window appears mentioning that design is netlisted and being fed back. Finally a message box appears asking whether you want to see Packager results.

4. Click *No*.

   The Control is passed back to Design Differences, which displays a message that schematic has successfully loaded.

5. Click OK.

   Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Design Entry HDL schematic. A message box appears displaying the message that the schematic and the `section_swapped2.brd` board file are in sync.

6. Click *OK* to close the message box.

## Comparing Differences between Schematics and Boards

For a given object, such as net, instance, or part, you can compare the differences between the logical view and the physical view. These differences are returned in a difference view window. For example, net differences are returned in the Net Difference window.

### Comparing Net Differences

You can compare net objects to verify if they exist in the logical and physical views. To compare net objects:

➤ Choose *Difference - Net* from the Design Differences menu bar.

The Net Difference window displays the differences between the nets in the logical and physical views. These differences are displayed in a tabular format. A difference in net occurs when you have added or deleted a net from the schematic or the layout.

**Note:** If the logical and physical views do not have any differences, a message box appears stating that differences do not exist.

### Comparing Instance Differences

You can compare instances to verify if differences exist in the logical and physical views. To compare instances:

➤ Choose *Difference - Instance* from the Design Differences menu bar.

The Instance Difference window displays the differences between the instances in the logical and physical views. These differences are displayed in a tabular format. A difference in instance occurs when you have added or deleted an instance from the schematic or the layout.

### Comparing Instance Part Differences

You can compare instance parts to verify if differences exist in the logical and physical views. A difference in an instance part occurs when there is:

- A `PACK_TYPE` property change
- A ptf file mapping change

To display the instance part differences,

➤ Choose *Difference - Instance Part* from the Design Differences menu bar.

The Instance Part Difference window appears. This window displays the differences between the instance parts in the logical and physical views. These differences are displayed in a tabular format.

### Comparing Pin-Net Connection Differences

Pin-net differences occur when you rewire nets, add instances or nets, or delete instances or nets in either the schematic or the layout. To view the connectivity differences between the logical and physical views in a tabular format, display the pin-net connection differences in the Pin-Net Connection Difference window.

To display the pin-net connection difference,

➤ Choose *Difference - Pin Connection* from the Design Differences menu bar.

The Pin-Net Connection Difference window appears. The differences between pins and nets are displayed in a tabular format.

### Comparing Instance Property Differences

To display the instance property differences between the logical and physical views:

➤ Choose *Difference - Inst Property* from the Design Differences menu bar.

The Instance Property Difference window displays the instance property differences between the logical and the physical views in a tabular format.

### Comparing Pin Property Differences

You can have pin property differences between the logical and physical views because of the following two reasons,

1. You have added, modified, or deleted a property that is attached to a pin in the schematic or layout.
2. You might not have specified the pin properties that need to be fed back to the `pxlBA.txt` file. A missing pin property in the `pxlBA.txt` file would give a false impression that the pin property is missing on the schematic.

To display the pin property differences between the logical and physical views,

➤ Choose *Difference - Pin Property* from the Design Differences menu bar.

The Pin Property Difference View window appears. This window lists the pin property differences between the logical and physical views.

**Note:** To control the pin properties that are transferred from the schematic to the layout and back from the layout to the schematic, use the Property Flow Setup dialog box.

### Comparing Net Property Differences

You can have net property differences between the logical and physical views because of the following two reasons:

1. You have added, modified, or deleted a property that is attached to a net in the schematic or layout.
2. You might not have specified the net properties that need to be fed back within the `pxlBA.txt` file. A missing net property in the `pxlBA.txt` file incorrectly suggests that the net property might be missing on the schematic.

You can display the net property differences in the Net Property Difference window. To display the net property differences,

➤ Choose *Difference - Net Property* from the Design Differences menu bar.

The Net Property Difference window appears. This window displays the differences in net properties between the logical and physical views in a tabular format.

**Note:** To control the net properties that are transferred from the schematic to the layout and back from the layout to the schematic, use the Property Flow Setup dialog box.

### Comparing Pin-Swapping Differences

To view the pin-swapping differences between the logical and physical views,

➤ Choose *Difference - Pin Swapping* from the Design Differences menu bar.

The Pin-Swapping Difference window displays the pin-swapping differences between the logical and physical views in a tabular format.

### Comparing Section-Swapping Differences

You might have different sections in the schematic and the board. These sections might have been swapped (that is, interchanged with each other). For example, a section with the schematic value 6 might be assigned the value 4 on the board. You can display the section-swapping differences in the Section-Swapping Differences window.

To display the section-swapping differences between the logical and physical views,

➤ Choose *Difference - Section Swapping* from the Design Differences menu bar.

The Section-Swapping Difference window displays the section-swapping differences between the logical and physical views in a tabular format**.**

**Note:** Design Differences uses the physical section transformations file, `pstsecx.dat`, to reassign a logical part from an old physical section to a new physical section. This file contains the list of section numbers that have been changed. The file lists the old and new values of the changed section numbers.

### Comparing Refdes Differences

If you have changed the `LOCATION` or the `CDS_LOCATION` property in the schematic or have renamed a reference designator in the layout, refdes swapping differences will exist between the schematic and the layout.

To display the differences in the reference designators between the logical and the physical views,

➤ Choose *Difference - RefDes Swapping* from the Design Differences menu bar.

The Refdes Difference window displays the section-swapping differences between the logical and physical views in a tabular format.

## Filtering Differences Between Schematics and Boards

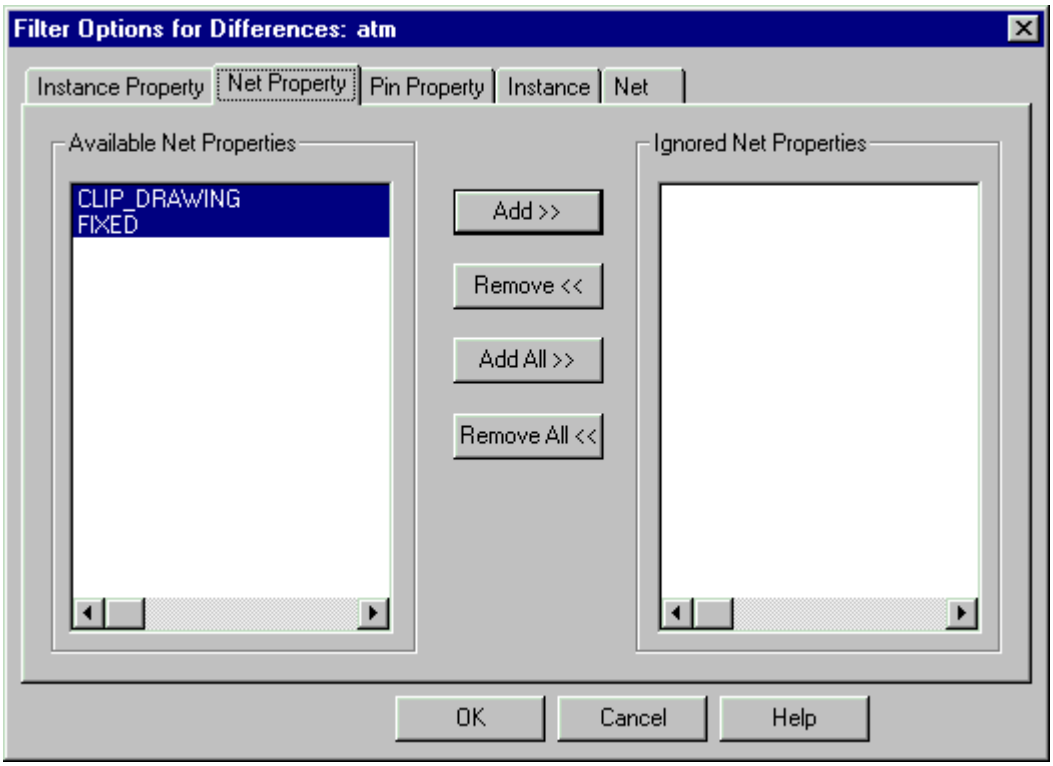
You can filter the nets, instances, or properties that you do not need or do not want to synchronize.

To filter the differences,

➤ Choose *Difference - Filter Options* from the Design Differences menu bar.

The Filter Options for Difference dialog box appears. It has five tabs: Instance Property, Net Property, Pin Property, Instance, and Net. To filter any differences, select the respective tab.

**Figure 5-18 Filter Options for Differences Dialog Box**




**Note:** Filter options let you control the display of differences. You cannot control the backannotation of data using the Filter Options for Difference dialog box.

### Filtering Instance Properties

You can filter instance properties using the following steps:

1. Choose *Difference - Filter Options* from the Design Differences menu bar.

The Filter Options for Difference dialog box appears. The Instance Property tab is selected by default.

2. Choose the net properties you need to filter and move them from the *Available Net Properties* list box to the *Ignored Net Properties* list box or vice versa.
3. Click *OK*.

The instance properties selected in the *Ignored Instance Properties* list box are ignored.

### Filtering Net Properties

You can filter net properties using the following steps:

1. Choose *Difference - Filter Options* from the Design Differences menu bar.

   The Filter Options for Difference dialog box appears.
2. Select the *Net Property* tab.
3. Select the net properties you need to filter and move them from the *Available Net Properties* list box to the *Ignored Net Properties* list box or vice versa.
4. Click *OK*.

The net properties selected in the *Ignored Net Properties* list box are ignored.

### Filtering Pin Properties

You can filter pin properties using the following steps:

1. Choose *Difference - Filter Options* from the Design Differences menu bar.

   The Filter Options for Difference dialog box appears.
2. Select the *Pin Property* tab.
3. Select the pin properties you need to filter and move them from the *Available Pin Properties* list box to the *Ignored Pin Properties* list box or vice versa.
4. Click *OK*.

The pin properties selected in the *Ignored Pin Properties* list box are ignored.

### Filtering Instances

You can filter instances using the following steps:

1. Choose *Difference - Filter Options* from the Design Differences menu bar.

   The Filter Options for Difference dialog box appears.

2. Select the *Instance* tab from this dialog box.
3. Select the instances you need to filter and move them from the *Available Instances* list box to the *Ignored Instances* list box or vice versa.
4. Click *OK*.

The instances selected in the *Ignored Instances* list box are ignored.

### Filtering Nets

You can filter nets using the following steps:

1. Choose *Difference - Filter Options* from the Design Differences menu bar.

   The Filter Options for Difference dialog box appears.

2. Select the *Net* tab in this dialog box.
3. Select the nets you need to filter and move them from the *Available Nets* list box to the *Ignored Nets* list box or vice versa.
4. Click *OK*.

The instances selected in the *Ignored Nets* list box are ignored.

# 6

# Using Design Association

## Overview

The Design Association tool is an important component of the Design Synchronization toolset. It allows you to update the connectivity changes made in the layout to the schematic. Design Association provides an intuitive user interface, which displays markers to all connectivity changes. You can select any marker and use it to update the Design Entry HDL schematic.

The Design Association tool performs the following three tasks:

1. Communicates with the Design Entry HDL schematic through Design Entry HDL SKILL
2. Executes the functions related to the Actions generated for connectivity markers
3. Updates the Design Entry HDL schematic design

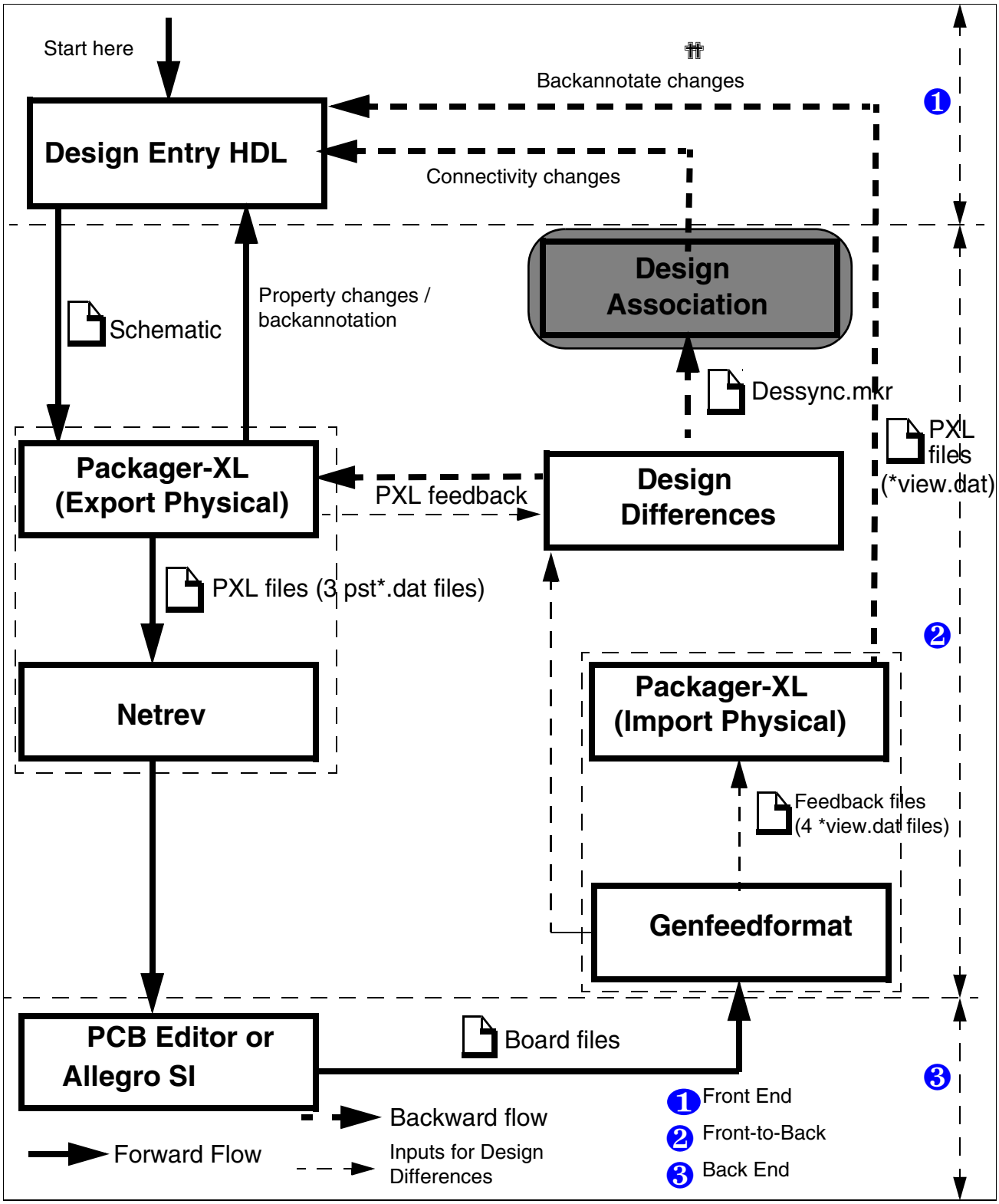
## How Design Association Fits in the Front-to-back Flow

When creating concurrent designs, you can transfer the packaging information from the schematic to the layout and continue to make changes both to the schematic and the layout. You can synchronize these changes using Design Synchronization tools. For details about how Design Association fits in the front-to-back flow, see Design Association Tool in the Front-to-Back Flow on page 148.

Design Association uses a file generated by VDD, `dessync.mkr`, which captures the connectivity change information and guides you in updating the schematic.

The property changes are made to the schematic using the Design Differences tool.

**Figure 6-1 Design Association Tool in the Front-to-Back Flow**



# Design Association Functions

The Design Association tool:

- Helps you to navigate through a Design Entry HDL schematic and run a design editing session where you can update and synchronize the logical Design Entry HDL schematic design with the corresponding physical layout drawing
- Guides you to the individual pages of the schematic and prompts you with the connectivity changes and design changes that need to fed back based on the changes in the layout

# Understanding Markers and Actions

### Markers

Markers record the information about the connectivity changes in the layout. This information is used by Design Association to do an update action on the Design Entry HDL schematic design.

### Dessync Marker File

The Design Differences tool creates the `dessync` marker file. This file contains the list of connectivity changes that you need to make in the Design Entry HDL schematic to synchronize it with the physical layout view. This file resides in the `packaged` view of the design that you have loaded in your Design Entry HDL schematic.

### Actions

To synchronize the Design Entry HDL schematic design with the PCB Editor or SI layout changes, you need to run actions corresponding to the markers in the *Markers* list box. You can use the Design Association tool to start an action.

When you start an action, the Design Association tool

- Transfers the property information (object properties, net names, and so on) stored in the `dessync.mkr` input file to the Design Entry HDL schematic and updates the schematic design
- Reflects the execution status of the action in the check box corresponding to the marker

# Launching and Exiting Design Association

## Overview

You launch Design Association from the Design Entry HDL schematic editor or from Design Differences. Before you start the schematic design, expand Design Entry HDL.

**Note:** If you open Design Association without expanding the design, Design Entry HDL displays a warning message. You are also allowed to expand the design.

## Launching from the Design Entry HDL Schematic

1. Open the Design Entry HDL schematic design.
2. To expand the design, choose *Tools - Expand Design* from the Design Entry HDL menu bar.
3. To display Design Association, choose *Tools - Design Association*.

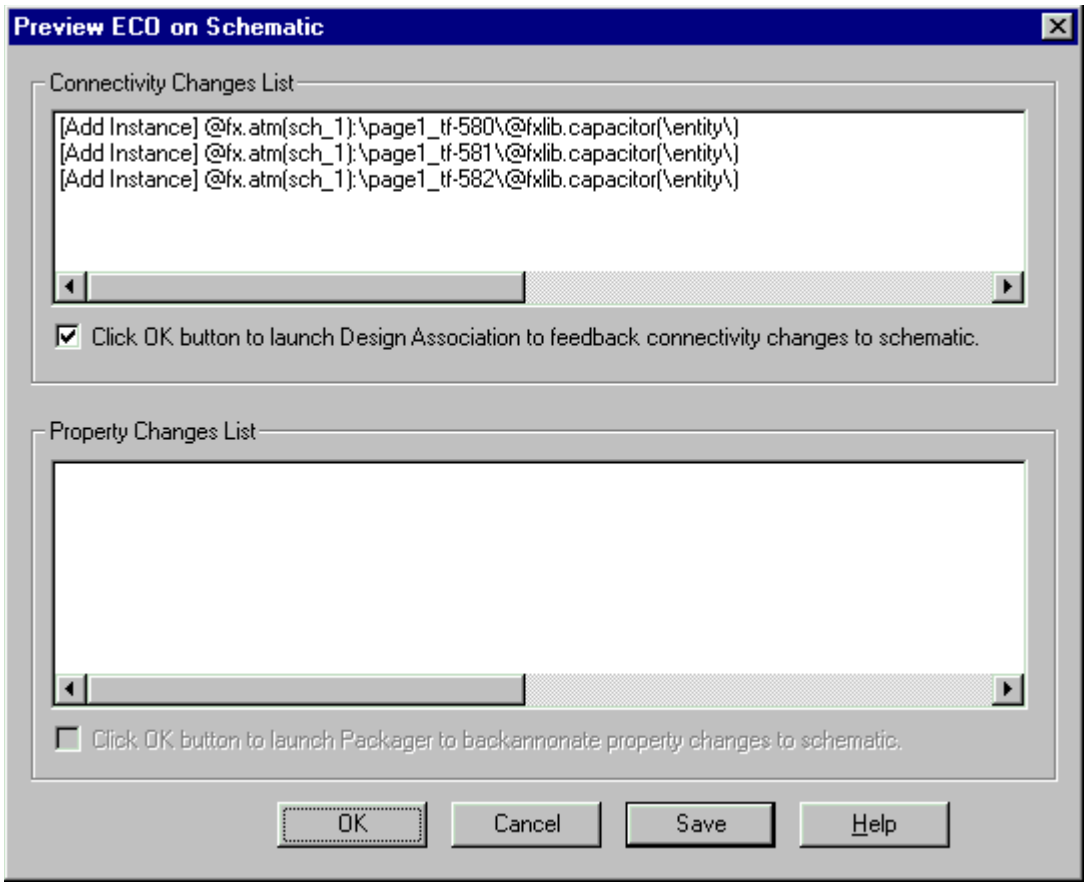
   The Design Association Window figure on page 152 appears.

## Launching from the Design Differences Tool

1. Launch the Design Differences tool.
2. Choose *Sync - Update Allegro Design Entry Schematic* from the Design Differences menu bar.

   The Preview ECO on Schematic Dialog Box figure on page 151 appears.

**Figure 6-2 Preview ECO on Schematic Dialog Box**




3. Select the *Click OK button to launch Design Association to feedback connectivity changes to schematic* check box.
4. Click *OK* on the Preview ECO on Schematic dialog box.

   The Design Association Window figure on page 152 appears.

## Exiting Design Association

➤ To exit from Design Association, choose *File - Exit* from the menu bar.

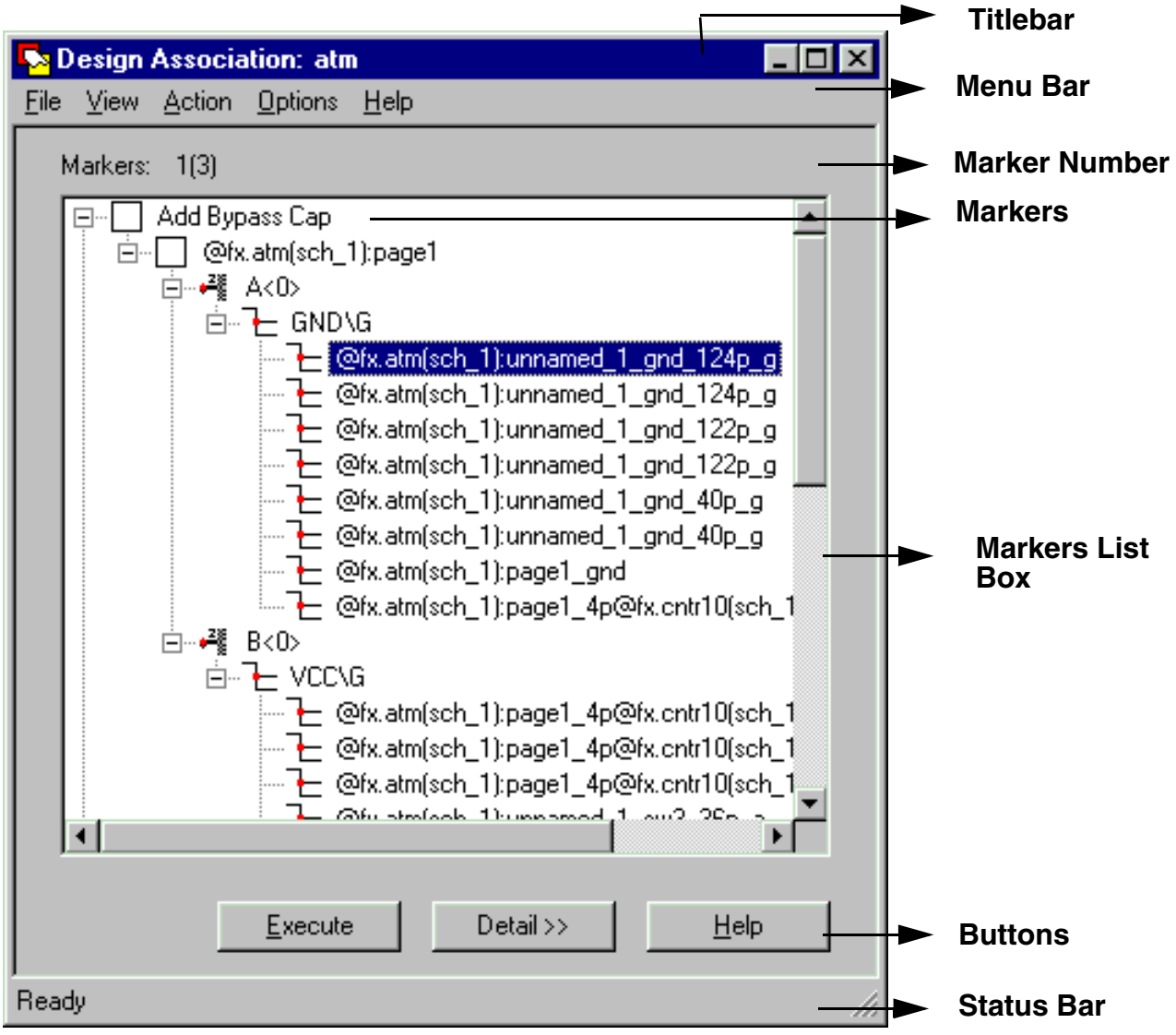
If the marker file has changed, Design Association displays a window that helps you save the Design Entry HDL schematic. If you click *OK*, all the modified pages of the Design Entry HDL schematic are saved. You can also save the marker file by using Design Association and use the file to update the changes to the schematic.

# Design Association User Interface

When you launch Design Association, it displays a window containing the list of markers. By default, the Design Association window does not display details about markers.

## Main Window

**Figure 6-3 Design Association Window**




The Design Association window has a titlebar that displays the name of the project file that you loaded in Design Entry HDL. For example, in the Design Association Window figure on

page 152, the titlebar displays the name of the project file as `atm`. The window also has a menu bar, a *Markers* list box, a status bar, and the following three buttons: *Execute*, *Detail*, and *Help*.

You can use the *Execute* button to run the action associated with the marker. You can expand the Design Association window to display the *Detail* section by clicking the *Detail* button. The *Detail* button acts as a toggle button. If you have expanded the window, you can click the *Detail* button to display the default main window.

The Design Association window helps you:

- Execute any of the Design Association menu commands
- Select any of the actions listed in the *Markers* list box and start the function associated with the action
- Filter the actions through the Filter/Select dialog box
- View the detailed information associated with each marker
- Update the information corresponding to the synonyms of the net for a selected marker, location, or the nets in the *Markers* list box

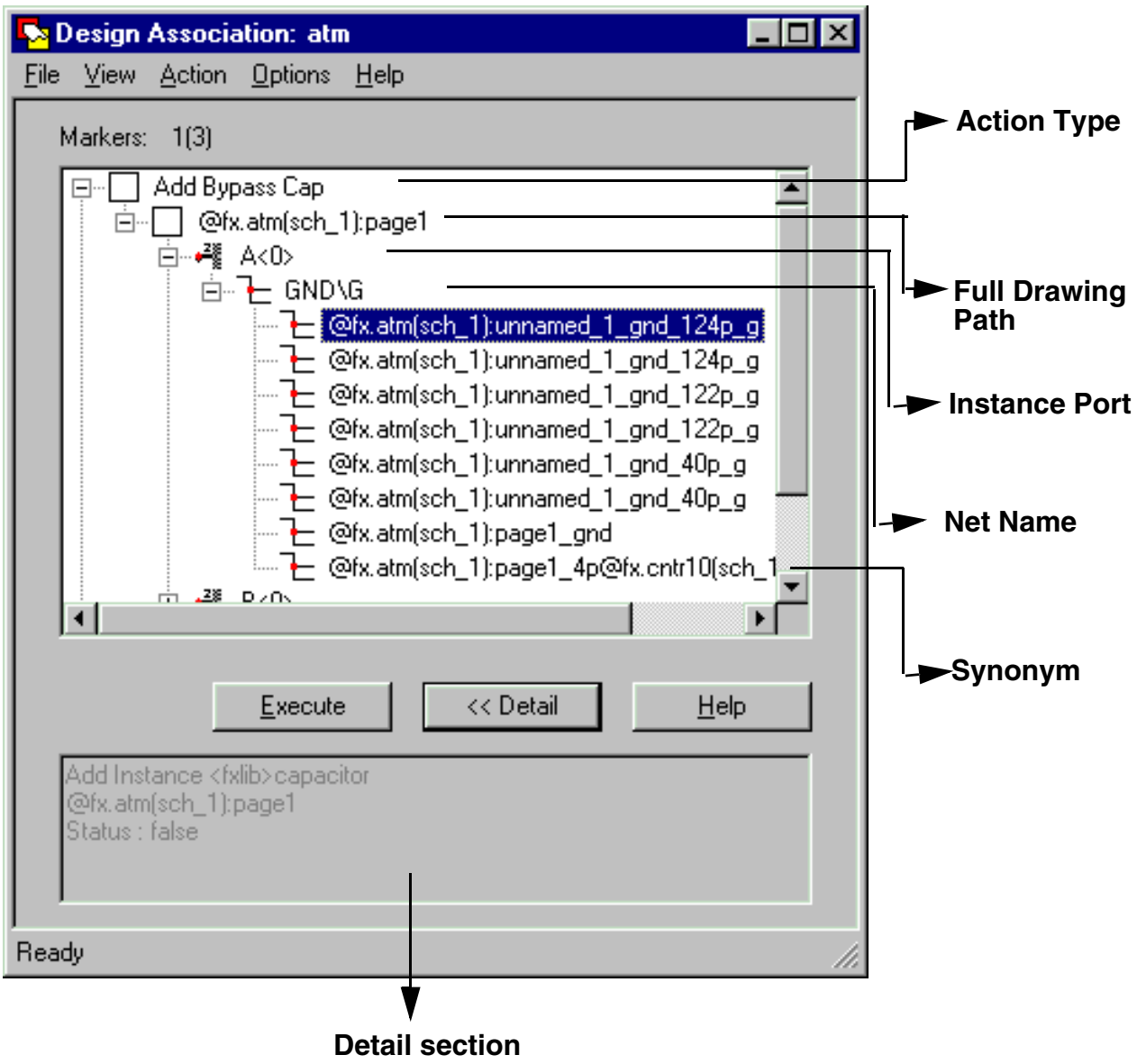
## Detail Window

You can expand the Design Association window to display the *Detail* section. To expand the Design Association window,

➤ Click the *Detail* button.

The Design Association window expands as displayed in the Design Association Window: Expanded figure on page 154.

**Figure 6-4 Design Association Window: Expanded**




The Detail window displays detailed information about the markers listed in the *Markers* list box. You can select any marker from the *Markers* list box. When a marker is selected, the check box associated with the marker is highlighted. The detailed information corresponding to the selected marker appears in the *Detail* window. The *Detail* window also displays the execution status of actions. When an action is executed, the status is updated accordingly. If the action fails, it displays the reason for the failure of the action.

## Markers List Box

The *Markers* list box provides the following:

- A static field to show *<Marker number><(Total number of markers)>*. For example, Design Association Window on page 152 displays the following value: `Markers: 1(3)`. This signifies that the selected marker is the first marker in a list of three markers.
- A list of markers that you can expand as hierarchical trees. Each marker corresponds to an action required for updating the Design Entry HDL schematic. For more information about how to expand a hierarchical tree, see Displaying a Hierarchical Tree on page 160.

## How Markers are Displayed

Markers are displayed in the following order:

- All markers are sorted by nine different Action Types.

  **Note:** Each marker corresponds to an action used by Design Association to update the Design Entry HDL schematic design.
- When a marker is unexpanded, it shows the execution status of the action and the action type to be executed. A check box to the left of each marker displays the execution status of the action.
- When an action associated with a marker has not been executed and you select a marker, Design Association automatically navigates to the corresponding location in the Design Entry HDL schematic. In addition for `Add Net To Pin`, `Delete Net From Pin`, or `Replace Net on Pin` or action types, it highlights the pin-net connection and for the `Add Instance` or `Delete Instance` action types, it highlights the instance.
- By default, the marker list is unexpanded. You can choose the *View - Expand Markers* command from the Design Association menu bar to see a hierarchical tree view of markers. If you again choose the *View - Expand Markers* command, the marker list appears collapsed.
- When you expand any marker, Design Association displays detailed information about the objects in the Design Entry HDL schematic on which it will operate for the selected marker. You can select any tree node in the marker list and update the schematic with the action specified by the marker.
- Navigating to an object results in changing its parent location node in the tree to the checked state. You can expand each marker by clicking its tree node. Each marker, when fully expanded, displays the action type, the full drawing path of the location, the instance port, the net name, and synonyms.

**Note:** You can control the display of markers in the tree control based on the action type, execution status, and the short message string.

## Execution Status of an Action

The check box next to each tree node corresponding to an action changes color based on the execution status of the action. The following figure describes the meaning of each colored check box in Design Association:

**Table 6-1 Execution Status of an Action**

| Color | Description |
|---|---|
| Black | The action was not executed. |
| Gray | The action cannot be executed. This is valid only for the `Add Instance` action type. |
| Red | The action was unsuccessfully executed. |
| Blue | The action was successfully executed. |
| Magenta | Locations added with the *Action - Add Location* command are preceded by magenta check boxes. |

## Action Types

The Design Association tool lists nine action types. Each action types does an action on a particular marker type. For example, the `Action Type - Delete an Instance` deletes an instance from the Design Entry HDL design.

The following section describes the function of each action type.

### Delete Instance Action Type

The `Delete Instance` action type deletes an instance from the Design Entry HDL design.

The `Delete Instance` marker in the *Markers* list box indicates the drawing in your Design Entry HDL design, where the instance to be deleted is located. You need to delete this instance for synchronizing the Design Entry HDL schematic and the PCB Editor or SI layout.

### Add Instance Action Type

The `Add Instance` action type adds an instance that is present in PCB Editor or SI to your Design Entry HDL design. The `Add Instance` action type adds the instance and also does the following tasks:

- Attaches properties to the instance
- Makes net-stub connections
- Attaches pin properties
- Attaches net properties

**Note:** An `Add Instance` marker can have multiple locations. Therefore before you add an instance, you need to select the location where you want the instance to be placed in the Design Entry HDL schematic. If you do not select any location, Design Association will select the first location. You can later recompute the locations or select a page in the Design Entry HDL schematic and define it as the location for adding instances.

### Delete Pin Net Action Type

The `Delete Pin Net` action type deletes a specified net from a pin within your Design Entry HDL design. You need to delete the specified pin-net connection for synchronizing the Design Entry HDL schematic and PCB Editor or SI layout.

### Add Pin Net Action Type

The `Add Pin Net` action type adds a pin-net connection to an instance in your Design Entry HDL design. You need to add this pin-net connection for synchronizing the Design Entry HDL schematic design with the PCB Editor or SI layout design.

### Replace Pin Net Action Type

The `Replace Pin Net` action type replaces a pin-net connection in your Design Entry HDL design.

You use this action type to replace a pin-net connection for synchronizing the Design Entry HDL schematic with the PCB Editor or SI layout design.

### Add Series Terminator Action Type

The `Add Series Terminator` action type, also known as `Add Series Term`, adds a series terminator to the net on the given pin.

Besides adding the series terminator, the `Add Series Terminator` action type does the following tasks:

- Attaches properties to the instance
- Makes net-stub connections
- Attaches pin properties
- Attaches net properties

### Add Shunt Terminator Action Type

The `Add Shunt Terminator` action type, also known as `Add Shunt Term`, adds a shunt terminator to the net on the given pin.

**Note:** You can apply the `Add Shunt Term` action type on Pull Down, Shunt RC, Power Diode, Ground Diode, Dual Diode, and Thevnin shunt terminators. You can add multiple instances of the shunt terminator using the `Add Shunt Term` action type.

In addition to adding the shunt terminator, the `Add Shunt Terminator` action type does the following tasks:

- Attaches properties to the instance
- Makes net-stub connections
- Attaches pin properties
- Attaches net properties

### Replace Instance Action Type

The `Replace Instance` action type replaces an existing instance on your Design Entry HDL design with a new instance.

You need to replace this instance for synchronizing the Design Entry HDL schematic and the PCB Editor or SI layout.

The `Replace Instance` action type does the following tasks:

- Deletes the existing component
- Adds the new instance
- Attaches properties to the instance
- Makes net-stub connections
- Attaches pin properties
- Attaches net properties

You can do the `Replace Instance` action in two modes, Automatic and Interactive. In the Automatic mode, Design Association checks if a new component can physically fit in the same space occupied by the existing instance and routes the pin-net connection. If the new component can fit in the same space as the existing component, Design Association replaces the instance. Otherwise, you are prompted to place the instance in another location and the connection is completed through the `Connect by Name` command.

In the Interactive mode, you can select the place in Design Association for adding instances. If you want to add the instance on a different page, you can select the location in the Design Entry HDL design where you want to add the instance. If you do not select any location, Design Association selects the first location by default.

### Change Part Action Type

The `Change Part` action type changes the property on an existing instance on your Design Entry HDL design so that the physical part of the instance is synchronized with the PCB Editor or SI layout.

# Using Design Association

You can use Design Association to do the following procedures described in this section:

- Displaying a Hierarchical Tree on page 160
- Expanding a Marker on page 160
- Starting an Action on page 161
- Adding Locations, Nets, Instances, and Terminators on page 165
- Backannotating to Design Entry HDL on page 168
- Changing Parts on page 169

- Opening and Saving the Markers File on page 174

## Displaying a Hierarchical Tree

When Design Association appears for the first time, the *Markers* list box shows the unexpanded markers, which display only the names of the corresponding action types. To display a hierarchical tree, you have to expand the marker.

1. To expand a marker, choose *View - Expand Markers* from the Design Association menu bar.

   The Design Association tool expands all the markers. A tree control appears with a tree node (+ sign) next to each marker.

2. Click the tree node next to any marker to expand the marker and display more details on the specific marker. For more details about expanding a marker, see Expanding a Marker on page 160.

Design Association automatically opens the drawing page corresponding to the marker in the Design Entry HDL design. It also highlights a section in which any instance needs to be added, or the section where a pin-net connection needs to be made or replaced, or a section from where an instance or the pin-net connection needs to be removed.

## Expanding a Marker

1. Expand the tree node corresponding to an unexpanded marker.

   The full drawing path of the instance corresponding to the marker appears. You can add the instance in this expanded path.

   **Note:** The first tree node constitutes the best location. If Design Association is not able to find any such location, the bitmap associated with the action turns red to mark the action as unexecutable.

2. Expand the tree node corresponding to the drawing path at that location to see the instance ports. The `Delete Instance` and `Add Instance` action types can have multiple instance ports.

3. Expand the tree node corresponding to the instance ports to see the nets (signals) connected to the instance ports.

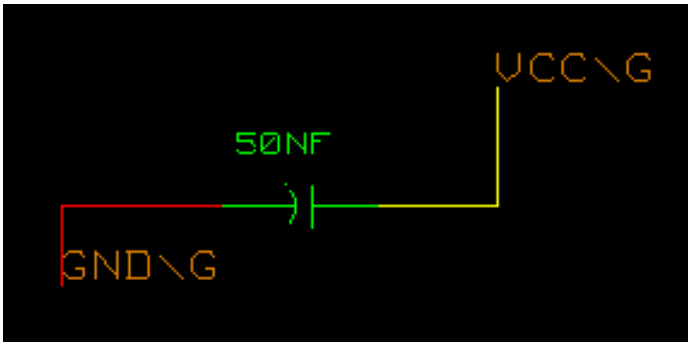
4. Click the net name.

   Design Association finds the synonyms of the net and updates the Design Association window with the synonyms of the net.

5. Select any of the synonyms or aliases.

Design Association opens the corresponding drawing in the Design Entry HDL schematic and highlights the corresponding location. See Design Association Window: Expanded on page 154 to understand how a marker expands. The following diagram shows a sample synonym `GND\G` highlighted in Design Entry HDL.

**Figure 6-5 Synonym Highlighted by DA in Design Entry HDL**




## Starting an Action

To synchronize the Design Entry HDL schematic design with the PCB Editor or SI layout changes, you need to start actions corresponding to the markers in the *Markers* list box.

There are two modes in which you can start actions.

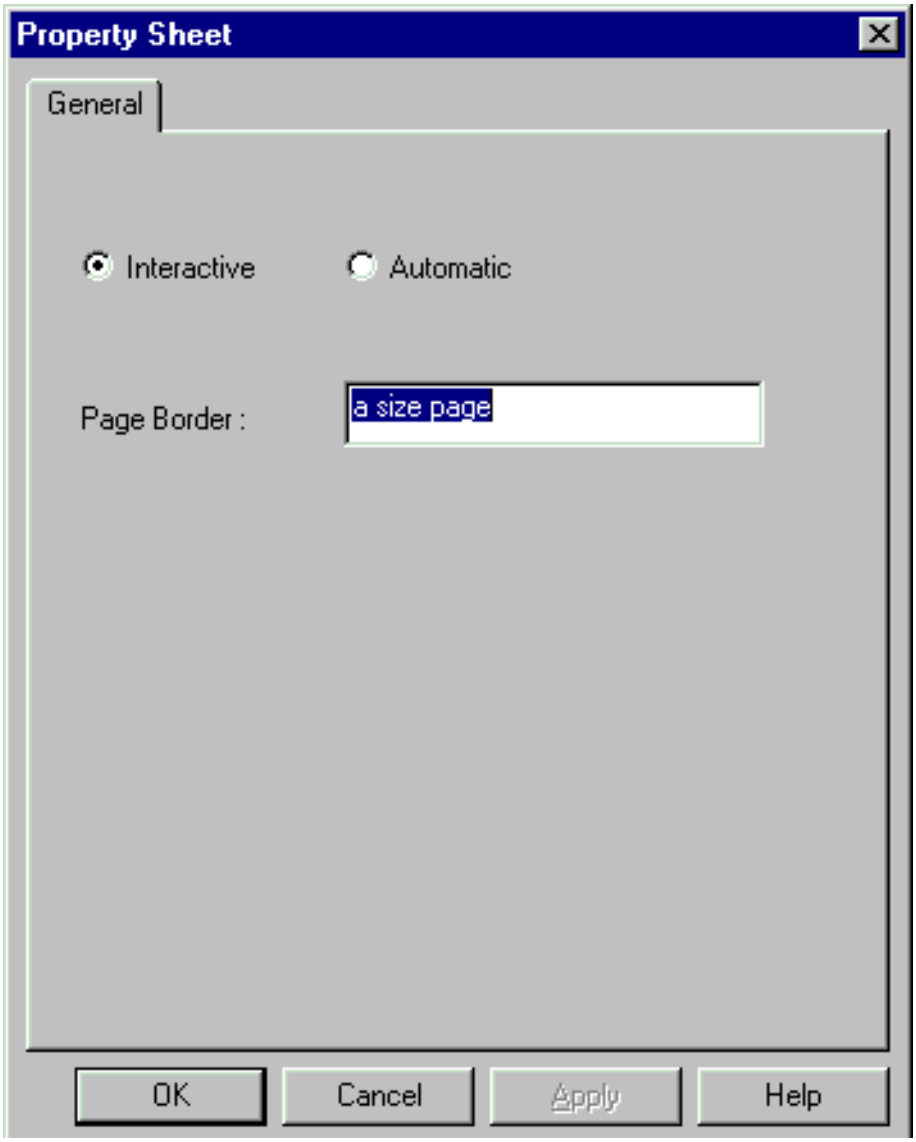
- Interactive mode
- Automatic mode

In the Interactive mode, Design Association lets you chose the location for the new instance in the Design Entry HDL design. In the Automatic mode, Design Association automatically starts all the actions corresponding to the markers in the Markers list box. To start a large number of actions, you can use the Automatic mode. You can select the mode in the Setup window (also called the Property Sheet).

To display the Setup window, choose *Options - Set Up* from the *Design Association* menu.

The *Property Sheet* dialog box appears.

**Figure 6-6 Property Sheet**




To change the Property Sheet settings:

1. To change the mode, select `Automatic`. The default mode is `Interactive`.
2. To change the page border, type the required drawing page size in the *Page Border* field. The default page border for adding new instances is `a size page`.
3. Click *OK*.

If you change the mode to Automatic, all marker changes are automatically executed. If the page corresponding to the location of a marker does not exist, the page will be created with the page border defined in the `Page Border` field.

### Running an Action for a Selected Marker

1. Select the marker whose action you need to start from the *Markers* list box.
2. If you need to display more information about the marker, expand it.

   Design Association automatically opens the corresponding drawing page in the Design Entry HDL schematic design.
3. To start the action, choose *Action - Execute* from the Design Association menu bar.

   or

   Click the *Execute* button.

Depending on the mode you select in the Property Sheet figure on page 162, the action corresponding to the marker is automatically executed or interactively executed. The check box next to the marker also changes to reflect the execution status of the action.

**Note:** It is possible to run multiple actions simultaneously. See Running Multiple Actions Simultaneously on page 163 for more information about executing multiple actions.

### Running the Action Again

If you have done a *Delete* or *Undo* action in the Design Entry HDL schematic and need to run the action again, follow the following steps:

1. Select the marker associated with the action.
2. Clear the marker by choosing *Action-Clear Status*.
3. Once the marker is cleared, follow the steps 1-3 as mentioned in the procedure Running an Action for a Selected Marker on page 163 to run the action again.

### Running Multiple Actions Simultaneously

You can start multiple actions simultaneously by using the `Ctrl` and `Shift` keys. Before you start any action that adds any instance, ensure that you have selected the page border in the Property Sheet on page 162.

1. Select all the markers in the *Markers* list box by using the `Shift` or `Control` key.

**Note:** The `Shift` key is used to select markers in succession. For example if you select the third marker and keeping the `Shift` key pressed, select the 17th marker, all markers beginning from the third to the 17th are selected.

**Note:** The `Control` key is used to select markers randomly. For example, you can select the third marker and keeping the `Control` key pressed select the seventeenth marker. Design Association will highlight the third and the seventeenth marker. You can simultaneously select any number of markers randomly by using the `Control` key.

2. Click the *Execute* button.
   - ❑ The Execute All window appears showing the progress status. The Progress control progresses whenever a new action is executed.
   - ❑ For each selected marker, Design Association displays a message box asking you to place the component in the Design Entry HDL design.
3. Click the *OK* button to place the component in the Design Entry HDL design.
4. The Design Entry HDL window appears. Observe the pointer. It displays the component corresponding to the marker. You can move the pointer to any place in the Design Entry HDL window and click at that point.
   - ❑ The component corresponding to the marker is placed at the selected point.
   - ❑ If there are more components to be placed, Design Association displays a message window asking you to place the next component in the Design Entry HDL design. If you need to place more components, repeat steps 3 and 4.
   - ❑ Finally, the Design Association window appears informing you that multiple actions have been executed. The window also displays a `Yes` or `No` option that you can use to review the details of the actions.
5. If you want to stop Design Association from executing all the selected actions, click *Stop*.
   - ❑ If you click *Stop* while Design Association is executing an action, the current action is executed, but none of the remaining actions are not executed. You cannot undo the executed actions.
   - ❑ The *Stop* button changes to *Cancel* when all the selected actions have been executed.
6. Click *Detail*, which is a toggle button, on the Execute window if you want to view the details while all the actions are being executed.

   The Execute window expands displaying all the details corresponding to each action as it is executed. You can click *Detail* again to switch the Execute window back to the unexpanded state.

7. Save the design by using *File - Save* or *File - Save As* from the Design Entry HDL menu bar.

   The design is saved.

**Note:** For an `Add Instance` action type, a new drawing page is added and all the instances are placed on that page.

**Note:** You can select multiple markers only with the following command menu items *Action - Execute*, *Action - Mark As Completed*, or *Action - Clear Status*.

## Adding Locations, Nets, Instances, and Terminators

### Adding a Location

Each marker is associated with a location, which represents the logical path name in the Design Entry HDL schematic where the marker will be executed. If the location is not attached to a marker or if you want to define a new location, you can add a location to that marker. To add a location to a marker,

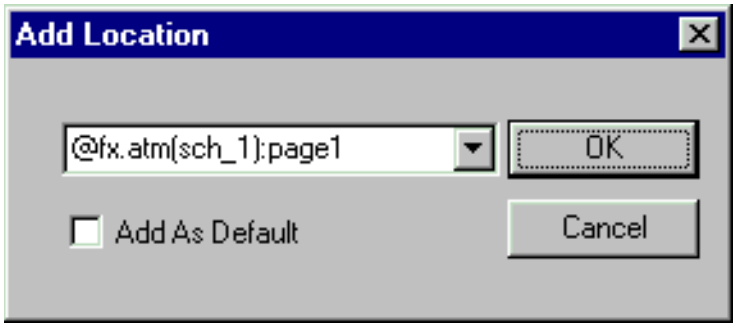
1. Select a marker from the *Markers* list box.

   The *Action - Add Location* menu is enabled.

2. To add the location, choose *Action - Add Location* from the Design Association menu bar.

   The Add Location window appears with a selection box, which presents the location (the logical path name of the drawing) of the active page that you want to edit in the Design Entry HDL design.

**Figure 6-7 Add Location Dialog Box**




3. If the action displays the canonical path, you can edit the selection. Next, click *OK* on the Add Location window to add the specified location.

The Design Association tool

- Adds the logical path name of the drawing in the active page in your Design Entry HDL design. If the location does not exist, the location is added as a new location in the current marker.
- Displays the new location below the parent marker as a magenta check box.

4. Select the marker corresponding to the new location or the default location from the *Markers* list box.
5. Choose *Action - Execute* from the Design Association menu bar.

   A message to place the component in your Design Entry HDL design appears in the status bar of the Design Association tool.
6. Zoom to the corresponding location in your Design Entry HDL design.
7. Place the component. After the action is executed, the magenta check box next to the new location is checked and the *Action - Execute* command is disabled.

**Note:** If you decide to add all the instances simultaneously using the *Action - Execute* command, Design Association adds a new page border. Before running the *Action - Execute* command, you must select *Options - Set Up* and indicate the drawing page size you need.

### Adding a Net to a Pin

1. To add a net to a pin in the Design Entry HDL schematic, select the corresponding `Add Pin Net` marker in the *Markers* list box.

   Design Association opens the corresponding drawing page in your Design Entry HDL design and highlights the specified net.
2. Click *Execute* in the Design Association window or choose *Action - Execute* from the menu bar.

   The drawing page of the instance is edited, and the wire-segment pin is added to the instance port.

**Note:** If the pin-net connection cannot be made, the Design Association window appears with a warning message explaining why the task cannot be executed.

**Note:** The check box next to the tree node corresponding to the specific `Add Pin Net` marker changes based on the execution status of the action.

### Adding an Instance

To add only one instance at a time,

1. To add an instance in the Design Entry HDL schematic, select the marker corresponding to the `Add Instance` action type.

   Design Association automatically opens up the corresponding drawing page in the Design Entry HDL schematic where the instance is to be added. To change the location, add a new location and click that location.

2. Zoom to the section in the Design Entry HDL schematic where you want to add the instance.

3. Click *Execute* in the Design Association window or choose *Action - Execute* from the menu bar.

   The instance to be added is attached to the pointer.

4. Place the instance in the section that you have zoomed into the Design Entry HDL schematic design.

   After you place the instance on the corresponding drawing page location of the Design Entry HDL schematic, Design Association attaches the net stubs to the instance ports.

To add multiple instances simultaneously,

1. Select the markers that you want to add from the *Markers* list box by using the `Shift` or `Control` key.

2. Choose *Options - Set Up* from the menu bar and show the new drawing page size.

3. Choose the *Action - Execute* command. Design Association places the components on the Design Entry HDL schematic.

**Note:** The check box next to the tree node corresponding to the selected `Add Instance` markers changes depending on the execution status of the action.

### Adding a Series Terminator

1. Select the marker corresponding to the `Add Series Term` action type.

   Design Association automatically opens up the corresponding drawing page and highlights the pin where the series terminator is to be added.

2. Click *Execute* in the Design Association window or choose *Action - Execute* from the menu bar.

If you have not selected a point, the series terminator will be added at the same predefined distance from the driver pin in the `Automatic` mode. If you have selected the point where you want to add the series terminator, the series terminator is added there in the `Interactive` mode. To select a mode, use the Setup dialog box.

### Adding a Shunt Terminator

1. Select the marker corresponding to the `Add Shunt Term` action type.

   Design Association automatically opens the corresponding drawing page and highlights the pin where the shunt terminator is to be added.

2. Click *Execute* in the Design Association window or choose *Action - Execute* from the menu bar.

   Depending on the mode selected in the Setup dialog box, the shunt terminator will either be added automatically or will be added at the point selected by you. If you have selected the `Automatic` mode, the Design Association tool selects the pattern of the shunt terminator that fits in the given place and the point where it can be added.

   If you have selected the `Interactive` mode, you can select different patterns of the shunt terminator by pressing the `Control` key and clicking the right mouse button. You can also select the point at which you want to add the given pattern of the shunt terminator.

## Backannotating to Design Entry HDL

### Loading the Feedback Files from the Current Packaged View Directory

1. To backannotate the changes to Design Entry HDL, choose *Action - Backannotate* from the Design Association menu bar.

   The Open dialog box appears showing an explorer view from which you can select the appropriate feedback files.

2. Browse to the `packaged` view directory or any other directory where you have the packaged files.

3. Select the format Data Files (`*.dat`) from the *Files of type* field.

4. Select the appropriate `*.dat` feedback files as described below:

   - Select the `*view.dat` files if you are backannotating from the PCB Editor layout tool.

- Select the `pstrprt.dat`, `pstxnet.dat`, `pstxprt.dat`, and `pstxref.dat` files if you are backannotating from a third-party layout tool.

The File name box is filled with the feedback file names you have selected.

5. Click *Open* in the Open dialog box to load the selected `*.dat` files for backannotation.

## Changing Parts

You may want to change a part for only one instance at a time or for multiple instances simultaneously.

### Changing Parts for a Single Instance

1. To change a part for a single instance, select the marker corresponding to the *Change Part* action type for that instance.

   Design Association automatically opens up the corresponding drawing page where the instance exists.

2. Click *Execute* in the Design Association window or choose *Action - Execute* from the Action menu bar.

The property value of `component_definition_property` is changed or the property is deleted.

### Changing Parts for Multiple Instances Simultaneously

1. To change parts for multiple instances, select the corresponding *Change Part* markers for each instance from the *Markers* list box using the `Shift` or `Control` key.
2. Choose *Action - Execute All*.

The property value of `component_definition_property` corresponding to each selected marker is changed, or the property is deleted.

**Note:** The status of the check box next to the tree node corresponding to the selected `Change Part` markers changes depending on the execution status of the action.

### Deleting a Location

You can delete a selected location using the *Action - Delete Location* command. This command can be applied only to the locations specified by `Add Instance` action types. If

you have any other action type, the *Action - Delete Location* command becomes unavailable for selection.

You cannot start the *Action - Delete Location* command if an `Add Instance` marker has only one location. The Design Association window appears with a warning that you cannot delete an instance that has only one location.

To delete a location,

1. Select the *Add Instance* marker corresponding to the location that you want to delete from the *Markers* list box.

   The *Action - Delete Location* command is enabled.

2. Choose *Action - Delete Location* from the Design Association tool menu bar.

   - The check box and the added location under the *Add Instance* parent marker are deleted.
   - The component corresponding to the marker in Design Entry HDL and its location are deleted from the design.

### Deleting a Net from a Pin

To delete a net from a pin,

1. Select the `Delete Pin-Net` marker corresponding to the net that you want to delete.

   Design Association automatically opens the corresponding drawing page in the Design Entry HDL design highlighting the specific net that needs to be deleted.

2. Choose *Execute* or choose the *Action - Execute* menu command.

   - The drawing page containing the pin-net connection that needs to be deleted is edited.
   - The wire segment is deleted from the pin.

**Note:** If the action cannot be executed, you get a warning indicating that the pin on the instance is not connected to the net or the segment.

**Note:** The status of the check box next to the tree node corresponding to the selected *Delete Pin-Net* marker changes based on the execution status of the action.

### Deleting an Instance

To delete an instance from the Design Entry HDL schematic,

1. Select the `Delete Instance` marker corresponding to the instance that you want to delete.

   Design Association automatically opens and highlights the instance that needs to be deleted from the corresponding drawing page of the Design Entry HDL schematic.

2. Choose *Execute* or click the *Action - Execute* menu command.

**Note:** If the instance cannot be deleted, the Design Association window appears with a warning message explaining why the instance cannot be deleted. Also, the check box next to the tree node corresponding to the specific `Delete Instance` action type changes depending on the execution status of the action.

### Replacing a Net on a Pin

To replace a pin-net connection, you can begin by expanding the marker. This is an optional step. Next, do the following steps:

1. Select the `Replace Pin-Net` option in the *Markers* list box to define the action that you need to start.

   The Design Association tool automatically opens up the corresponding drawing page in the Design Entry HDL schematic design in which the pin-net connection is to be replaced.

2. Choose *Action - Execute* or choose the *Action - Execute* menu command.

   The Design Association tool replaces the pin-net connection and the check box next to the marker changes to reflect the execution status of the action.

**Note:** If the pin-net connection cannot be replaced, the Design Association window appears with a warning message explaining why the action cannot be executed.

**Note:** It is possible to run multiple actions simultaneously.

### Replacing an Instance

Based on your requirements, you can select to replace only once instance or multiple instances simultaneously.

#### *Replacing Only One Instance at a Time*

1. Select the `Replace Instance` marker corresponding to the instance that you want to replace. Design Association automatically opens up the corresponding drawing page where the instance is to be replaced.

2. Select the *Interactive* or *Automatic* option from *Options - SetUp*.

   **Note:** In the *Interactive* mode, you can specify the location where you want to add the instance.

3. Click *Execute* in the Design Association window or choose the *Action - Execute* menu command.

   The instance to be replaced is attached to the pointer.

4. Place the component in the section that you have zoomed into in your Design Entry HDL schematic design.

Design Association attaches the net stubs to the instance ports.

### *Replacing Multiple Instances Simultaneously*

1. Select the `Replace Instance` markers corresponding to the instances that you want to replace by using the `Shift` or `Control` key.
2. Choose the *Action - Execute All* command.

   Design Association replaces the components in the Design Entry HDL design.

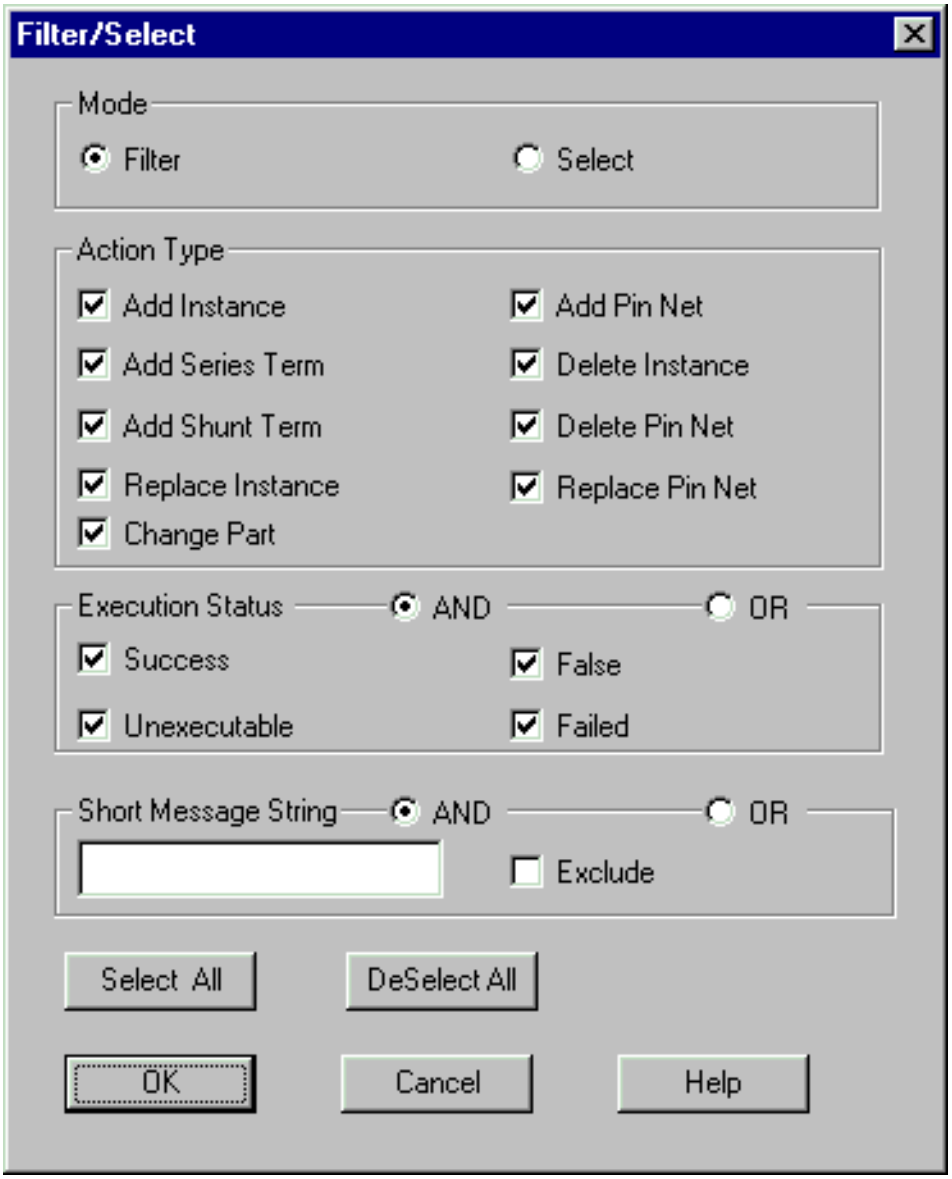
**Note:** The check box next to the tree node corresponding to the selected `Replace Instance` markers changes based on the execution status of the action.

### Filtering Action Types and Message Strings

1. Choose *Options - Filter/Select* from the Design Association window.

   The Filter/Select Dialog Box appears.

**Figure 6-8 Filter/Select Dialog Box**




2. Select the *Filter* radio button or the *Select* radio button in the *Mode* group.
3. Select *Filter* to indicate that you want to filter out all the markers in the *Markers* list box. Choose *Select* to show that you want to specify the markers to be executed.
4. Select the actions you need to start by clicking one or all options in the *Action Type* box.

   The *Markers* list box in the Design Association window lists only those action types that you have chosen.

5. To display the status of the action, select one or all options, Success, False, Failed, or Unexecutable, in the *Execution* group.

   When an action is started, the check box to the left of the marker in the *Markers* list box in the Design Association dialog box changes in color based on the execution status of the action.

6. Enter an expression to filter the markers in the *Short Message String* field.

7. To exclude the specified regular expression that you typed in step 5 in the *Short Message String* field from the filter, click *Exclude*.

   **Note:** If you select the *Exclude* check box, then only those short messages that do not match the specified regular expression are passed through this filter.

8. Click *Select All* or *DeSelect All* to select or clear all the options in the *Action Type* box or the *Execution Status* box.

9. Click *OK* to filter the markers.

   All the markers matching your search criteria are displayed.

10. If you need to close the Filter/Select dialog box without filtering the markers, click *Cancel*.

### Marking an Action as Completed

If you make a change without going through the Design Association tool, you can mark the action using the `Mark as Completed` command.

➤ Choose *Action - Mark as Completed* from the Design Association menu bar.

**Note:** You can select multiple selection of markers only with the following commands: *Action - Execute*, *Action - Mark As Completed*, and *Action - Clear Status*.

## Opening and Saving the Markers File

### Loading the Markers File

The Design Differences tool sends connectivity changes to the `dessync.mkr` file. Design Association uses this file as the input to apply the connectivity changes to the Design Entry HDL schematic and get the logical view in sync with the physical view. By default, Design Association generally starts loaded with the `dessync.mkr` file generated by Design Differences. If this does not happen, you can open and load the marker file using the following steps:

1. Choose *File - Open* from the Design Association menu bar.

   The Open Marker File dialog box appears with a list of marker files (`*.mkr`). Design Association opens the Open Marker File dialog box in the same directory where your project file (`*.cpm`) is located.

2. Use the *Navigate* button in the *Look in* box to navigate to the directory that contains the specific application directory whose marker file you need to load.

3. Double-click the application directory to open it.

4. Select the `*.mkr` file that has been generated by Design Differences from the application directory.

   The *File* field shows the marker filename, `dessync.mkr`.

5. Select the format marker Files (`*.mkr`), in the *Files of type* box.

6. Click *Open* in the Open Marker File dialog box to load the marker file `dessync.mkr`.

### Saving the Marker File

You must save the marker file before exiting Design Association to ensure that the execution status of an action is available for future Design Association sessions.

1. Choose *File - Save* from the Design Association menu bar.

   The current marker file is saved in the directory from where it was read, and a message box appears asking you to save your design in Design Entry HDL.

2. Choose *File - Save Schematic* from the Design Association menu bar to save the schematic design so that the marker file is in sync with your design.

**Note:** You can save the marker file with a different name by using the *File - Save As* command.

### Viewing Marker File Properties

1. Choose *File - Properties* from the Design Association menu bar. The Design Association window appears displaying the following:

   - The full path to the current marker file

     **Note:** The path to the `dessync.mkr` file appears by default.

   - The path to the current project file

2. Click *OK* to close the Properties window.

# A

# Miscellaneous Items

The following list covers miscellaneous terms that have been used in this guide.

### Logical View

The set of files that Packager-XL uses to represent a schematic is called a logical view. The logical view shows information about the instances, nets, properties, and connectivity in a Design Entry HDL schematic database.

The logical view shows the following Packager-XL output files: `pstxnet.dat`, `pstxprt.dat`, and `pstchip.dat`.

### Physical View

The set of files that Packager-XL uses to represent a layout is called a physical view. The physical view shows information about the instances, nets, properties, and connectivity in the PCB Editor layout database.

The physical view shows the following output files extracted by PCB Editor: `pinview.dat`, `funcview.dat`, `netview.dat`, and `compview.dat`.

## Sample propflow.txt File

The `propflow.txt` file is used to define the properties that will be transferred between Design Entry and PCB Editor. A sample `propflow.txt` file is shown below:

```
OWNER
0 - Undefined
1 - Component
2 - Instance
3 - Net
4 - Pin
Concept
```

```
0 - Not defined in concept
1 - Defined in concept
Allegro
0 – Not defined in allegro
1 – Defined in allegro
Transfer
0 - Not transferable between concept and allegro
1 - Transferable
WINNING_VLAUE
0 - None
1 - Allegro
2 - Concept
TYPE
0 - Undefined
1 - String
2 - Integer
```

**PROPERTY_NAME!OWNER!CONCEPT!ALLEGRO!TRANSFER!WINING_VALUE!TYPE!**

```
NET_NAME!3!1!1!1!1!0!
REFDES!3!0!1!0!0!0!
PIN_NUMBER!3!1!0!0!0!0!
COMP_DEVICE_TYPE!3!0!0!0!0!0!
FUNC_LOGICAL_PATH!2!1!1!1!1!0!
COMP_DEVICE_TYPE!2!1!0!0!0!0!
COMP_PARENT_PPT_PART!2!0!1!0!0!0!
COMP_PARENT_PART_TYPE!2!0!0!0!0!0!
COMP_NO_ROUTE!1!1!1!1!1!0!
COMP_MAX_POWER!1!0!1!0!0!0!
COMP_RATED_POWER!1!1!0!0!0!0!
NET_PHYSICAL_TYPE!4!1!1!1!1!0!
NET_DELAY_RULE!4!0!1!0!0!0!
NET_FIXED!4!1!0!0!0!0!
NET_WEIGHT!4!0!0!0!0!0!
```

# List of Properties Filtered from Packager Files

The predefined list of properties that are filtered out while reading packager output files is:

### Pin Properties

NO_LOAD_CHECK

NO_IO_CHECK

ALLOW_CONNECT

PIN_GROUP

## Component Properties

FAMILY

CLASS

PART_NAME

PHYS_DEF_PREFIX

PART_NUMBER

JEDEC_TYPE

DESCRIPTION

ALT_SYMBOLS

PARENT_PART_NAME

PARENT_PPT

PARENT_PPT_PART

BODY_NAME

POWER_PINS

SCH_MODIFIED_PART

TECH

DEFAULT_SIGNAL_MODEL

## Function Properties

XY

PATH

DRAWING

PACK_TYPE

CDS_LIB

PRIM_FILE

PART_NUMBER

# B

# Packager Setup Command Information

## Packager Setup

Procedures Command

Use this dialog box to view or change the default packaging options in the project file. Packager utilities and Design Differences obtain their packager setup options from the project file.

### Available In

The dialog box can be accessed from:

1. Export Physical—Click the *Advanced* button to access Packager Setup.
2. Import Physical and Design Differences—Click *Options* to access Packager Setup.
3. Project Manager—Click *Setup*. Next, select *Tools* tab and click the *Setup* button for *Packager-XL*.

#### Function

The Packager Setup dialog box consists of six tabbed pages. You can change the following setup options in each tab:

1. Packager Setup - Properties—Use this tabbed page to specify the schematic and component definition properties for packaging. You can also create filters to prevent packaging of certain properties.You can specify the properties to be listed in the Packager output files. Finally, you can use *Property Flow Setup* to set the default properties that flow between Design Entry HDL and PCB Editor.
2. Packager Setup - State File—Use this tabbed page to control the properties in the state file. You can define the properties in the state file that replace the corresponding

properties in the schematic. You can also define the properties that will replace the properties in the layout file (in case of differing values). Finally, you can use the *State File* tab to remove properties from the state file.

3. Packager Setup - From Layout—Use this tabbed page to control the properties that will be fed back or backannotated from the layout to the schematic.
4. Packager Setup - Report—Use this tabbed page to specify the Packager-XL output. By controlling settings, you can generate multiple output files and control error and warning displays.
5. Packager Setup - Layout—Use this tabbed page to modify layout netlist parameters and reference designators. You can change reference designator naming schemes. You can also change the default prefix for reference designators. You can increase or decrease the number of characters used to define component or physical net names. Finally, you can define which characters can or cannot be used in defining net names.
6. Packager Setup - Subdesign—Use this tabbed page to specify how to package blocks in hierarchical designs. You can generate a specific subdesign state file for the block. After defining a subdesign state file, you can force packaging to each instance of the subdesign in the subdesign state file. You can even customize how packaging in the subdesign state file is used in place of new subdesign instances.

### Procedures

- Changing the Packager Setup Properties on page 38
- Changing Packaging Information in the State File on page 42
- Changing Feedback Properties in the Layout on page 45
- Changing Packager Output Information on page 48
- Changing Reference Designators and Netlist Parameters on page 51
- Changing Setup Options While Packaging Subdesigns on page 54

### Command

To access Packager Setup from the command prompt or terminal, first call Project Setup and then select *Tools* tab and click the *Setup* button for *Packager-XL*

To access Project Setup from command prompt or terminal, use the command:

```
psetup -proj <file_name>.cpm
```

where:

<*file_name*> is the project file.

# Packager Setup - Properties

Procedures Command/Directives

Use this dialog box to add and remove Packager properties. You can specify the schematic and component definition properties for packaging. You can also create filters to prevent packaging of certain properties.You can specify the properties to be listed in the Packager output files.

**Package**

Specifies a preference to package together the schematic instances that share these properties if their values are the same. However, if spare slots are available, instances without the packager properties can be added.

Use *Add* to add a property to the *Package* list box. When you choose *Add*, the Add Property dialog box displays. You can add properties here.

**Note:** To enable Packager to honor the property assigned to split parts, you need to add the `SPLIT_INST_NAME` property as a packaging property. To do this, click the *Add* button in the Package section, type `SPLIT_INST_NAME` and click *OK*.

Use *Remove* to delete any property from the *Package* list box.

**Strict Package**

Specifies that only the schematic instances that have properties with identical values be packaged together.

Use *Add* to add a property to the *Strict Package* list box.

Use *Remove* to delete any property from the *Strict Package* list box.

| | |
|---|---|
| **Component Definition** | Specifies the names of the properties to be treated as component definition properties, which Packager-XL uses to create alternate physical parts.<br><br>Use *Add* to add a property to the *Component Definition* list box.<br><br>Use *Remove* to delete any property from the *Component Definition* list box. |
| **Component Instance** | Specifies the names of the properties to be treated as component instance properties.<br><br>Use *Add* to add a property to the *Component Instance* list box.<br><br>Use *Remove* to delete any property from the *Component Instance* list box. |
| **Property Conflicts Filter** | Specifies the names of the properties to be filtered from the `pstprop.dat` file.<br><br>Use *Add* to add a property to the *Property Conflicts Filter* list box.<br><br>Use *Remove* to delete any property from the *Property Conflicts Filter* list box. |
| **Filter** | Specifies any properties that you want to omit from the packager output files.<br><br>Use *Add* to add a property to the *Filter* list box.<br><br>Use *Remove* to delete any property from the Filter list box. |
| **Pass** | Specifies the properties that you want to include in the packager output files.<br><br>Use *Add* to add a property to the *Pass* list box.<br><br>Use *Remove* to delete any property from the *Pass* list box. |
| **Property Flow Setup** | Launches the Property Flow Setup dialog box, which can be used to control the properties that flow between Design Entry HDL and PCB Editor. |

| | |
|---|---|
| **OK** | Completes the setup process by:<br>■ Closing the Packager Setup dialog box.<br>■ Taking you back to the dialog box from which you invoked Packager Setup.<br>■ Applying the Packager Setup options, which you specified in the above selection boxes, to the design. |
| **Cancel** | Closes the Packager Setup dialog box without applying any changes to the Packager Setup options in the design. |
| **Reset** | Resets the Packager Setup options to the default values. |

### Command/Directives

To access Packager Setup from command prompt, see Command on page 182.

For more information about the Packager-XL directives modified from the Properties tab, see the following directives in *Packager-XL Reference*.

- PACKAGE_PROP
- FILTER_CONFLICTING_PROP
- COMP_DEF_PROP
- COMP_INST_PROP
- FILTER_CONFLICTING_PROP
- FILTER_PROPERTY
- PASS_PROPERTY

# Packager Setup - State File

| Procedures | Command/Directives |
|---|---|

Use these setup options to control how Packager-XL feeds back or backannotates properties from the layout to the schematic.

**Remove From State**

Specifies the properties to be removed from the State file.

Use *Add* to construct the list of properties to be removed from the State file. When you choose *Add*, the Add Property dialog box displays. You can add properties here.

Use *Remove* to delete any specific property listed under the *Remove From State* list box that you do not want to be removed from the State file.

-or-

Specify *All Properties* if you want all the properties to be removed from the State file.

**State Wins Over Design**

Causes the property values in the State file to override the properties in the schematic when their values differ.

Use *Add* to construct the list of properties to be overridden in the schematic design.

Use *Remove* to delete any specific property listed under the *State Wins Over Design* list box that you do not want to be overridden in the schematic.

-or-

Select *All Properties* so that all the properties in the schematic are overridden.

Select *Never* so that the properties in the schematic are never overridden. The default is *Never*.

| | |
|---|---|
| **State Wins Over Layout** | Causes the property values in the State file to override the properties in the layout feedback files when their values differ.<br><br>Use *Add* to construct the list of properties to override in the physical layout.<br><br>Use *Remove* to delete any specific property listed under the *State Wins Over Layout* list box that you do not want to be overridden in the layout feedback files.<br><br>-or-<br><br>Select *All Properties* to specify that all properties in the physical layout be overridden.<br><br>Select *Never* to specify that the properties in the physical layout should not be overridden. Never is the default option. |
| **OK** | Completes the setup process by:<br><br>■ Closing the Packager Setup dialog box.<br><br>■ Taking you back to the dialog box from which you invoked Packager Setup.<br><br>■ Applying the Packager Setup options, which you specified in the above selection boxes, to the design. |
| **Cancel** | Closes the Packager Setup dialog box without applying any changes to the Packager Setup options in the design. |
| **Reset** | Resets the Packager Setup options to the default values. |

### Command/Directives

To access Packager Setup from command prompt, see Command on page 182.

For more information about the Packager-XL directives modified from the Properties tab, see the following directives in *Packager-XL Reference*.

- REMOVE_FROM_STATE
- STATE_WINS_OVER_DESIGN
- STATE_WINS_OVER_LAYOUT

# Packager Setup - From Layout

Procedures Command/Directives

Use these setup options to control how Packager-XL uses packaging information in the State file.

**No Feedback Properties**

Specifies the feedback properties that you do not want to override in the schematic.

Use *Add* to construct the list of feedback properties that you do NOT want to import from the physical layout. When you choose *Add*, the Add Property dialog box displays. You can add properties here.

Use *Remove* to delete a property from the *No Feedback Properties* list.

**Feedback**

Runs Packager-XL in the feedback mode.

*None*—Runs Packager-XL in the forward mode. The default *Feedback* value is *None*.

*PCB Editor*—Performs feedback using the PCB Editor feedback files from the layout.

*3rd Party*—Performs feedback using these files from the 3rd Party layout tool.

Select the check box to generate the corresponding file:

*Pstprtx.dat*—Describes physical reference designator transformations.

*Pstsecx.dat*—Describes sections transformations.

*Pstnetx.dat*—Describes physical net name transformations.

*Pstfnet.dat*—Describes the connectivity for each refDes pinNumber in the design.

**Note:** This option is available only when you do Setup from Project Manager.

| | |
|---|---|
| **Annotate** | Select *All* to specify that all the properties in the layout be backannotated to the schematic.<br><br>Select *None* to specify that properties in the layout should not be backannotated to the schematic. If this option is selected, the backannotation file `pstback.dat` will not be generated even if the *Backannotate Packaging Properties to Schematic Canvas* option is selected in the Export Physical dialog box.<br><br>Select from the *Options* list if you need to control specific objects (Body, Pin, Net, Physical Net Name, or a combination of these) in the design you need to backannotate to the Design Entry HDL schematic.<br><br>The default is *Options*. |
| **Do not Update Hard Location, Section and Pin numbers on schematic** | Select this check box to prevent the packaging of hard properties.<br><br>The default option is *off*, signifying that Packager-XL will update hard (Location, Section and Pin) properties. |
| **OK** | Completes the setup process by:<br><br>■ Closing the Packager Setup dialog box.<br><br>■ Taking you back to the dialog box from which you invoked Packager Setup.<br><br>■ Applying the Packager Setup options, which you specified in the above selection boxes, to the design. |
| **Cancel** | Closes the Packager Setup dialog box without applying any changes to the Packager Setup options in the design. |
| **Reset** | Resets the Packager Setup options to the default values. |

### Command/Directives

To access Packager Setup from command prompt, see Command on page 182.

For more information about the Packager-XL directives modified from the Properties tab, see the following directives in *Packager-XL Reference*.

- ANNOTATE
- FEEDBACK

- HARD_LOC_SET
- NO_FEEDBACK

# Packager Setup - Report

| Procedures | Command/Directives |
|---|---|

Use these setup options to control the Packager-XL output.

**Output**

Specifies the output that Packager-XL should generate. Choose *None*, *All*, or *Custom*. Packager-XL generates all the output files by default.

If you select *Custom*, choose any of the following options from the *Custom* list to specify the output that you want.

*Netlist*—Generates the following:

`pstchip.dat`—Contains the physical information for each part, including that found in the chips files for each component in the schematic.

`pstxnet.dat`—Lists the physical net names and nodes connected to each net.

`pstxprt.dat` * Correlates the logical components to their physical reference designator and section assignments.

*Change*—Generates

`pxl.chg`— Documents the packaging changes between two packager runs.

*Report*—Generates:

`pstrprt.dat`—Provides the component summary and spares list.

*Pinlist*—Generates:

`pstpin.dat`—Contains the design specific pin list. This list is similar to the pstchip.dat file.

*Xref*—Generates:

`pstxref.dat`—Cross references all logical-to-physical assignments, net names, and components.

| | |
|---|---|
| **Warnings** | Lists the warning numbers that you want to suppress. Packager-XL generates all the *Output Warnings* by default.<br><br>Use *Add* to construct a list of warning numbers to suppress. When you choose *Add*, the Add Property dialog box displays. You can add properties here.<br><br>Use *Remove* to remove any warnings from the Suppress list box. |
| **Maximum Errors** | Specifies the number of allowable errors before Packager-XL stops. |
| **Backup Versions** | Specifies the maximum number of backup packaged file sets that Packager-XL will maintain. |
| **Check for ppt entry for all instances in design** | Select the *Check for ppt entry for all instances in design* check box to verify that the ppt files are present in the cell view for all instances, and a ppt entry is defined for each instance in the ptf file. |
| **OK** | Completes the setup process by:<br>■ Closing the Packager Setup dialog box.<br>■ Taking you back to the dialog box from which you invoked Packager Setup.<br>■ Applying the Packager Setup options, which you specified in the above selection boxes, to the design. |
| **Cancel** | Closes the Packager Setup dialog box without applying any changes to the Packager Setup options in the design. |
| **Reset** | Resets the Packager Setup options to the default values. |

### Command/Directives

To access Packager Setup from command prompt, see Command on page 182.

For more information about the Packager-XL directives modified from the Properties tab, see the following directives in *Packager-XL Reference*.

- OUTPUT
- WARNINGS
- MAX_ERRORS
- NUM_OLD_VERSIONS

- FORCE_PTF_ENTRY

# Packager Setup - Layout

Procedures Command/Directives

Use these setup options to modify layout netlist parameters and reference designators. In most cases, you do not need to modify the default pattern for reference designators.


***Use caution when changing the default-naming scheme for reference designators. To apply a new pattern to the existing reference designators, you must repackage the design.***

**Ref Des Pattern**

Specifies a reference designator that is different from the default.

The default reference designator uses the `PHYS_DES_PREFIX` property as the base name plus a number, which is appended by Packager-XL.

If you require a different naming scheme from the default, you can specify a new naming scheme.

**Reset Ref Des counter for new pages and Ref Des prefix**

Specifies that the counter used to designate reference designators be reset for:

- New pages
- Different Ref Des prefix

**Note:** The *Reset Ref Des counter for new pages and Ref Des prefix* check box is enabled when you enter any character in the *Ref Des Pattern* field.

**Reuse Ref Des numbers**

Specifies that the reference designators for the changed or the deleted components in the schematic or the board should be reused for new components.

By default, the *Reuse Ref Des numbers* check box is selected. If you do not want to reuse existing reference designators, clear the *Reuse Ref Des numbers* check box.

| | |
|---|---|
| **Default Ref Des Prefix** | Specifies a default reference designator to be used if no `PHYS_DES_PREFIX` property can be found. `U` is the default option. |
| **Ref Des Length** | Specifies the maximum number of characters used to define reference designators. |
| **Part Type Length** | Specifies the maximum number of characters used for component names. |
| **Net Name Length** | Specifies the maximum number of characters used for physical net names.The default value is 31.<br><br>If you change the default value, it will become effective only when the design is repackaged. |
| **Net Characters** | Allows or disallows specified characters in net names. Use *Add* to construct a list of characters that you want to include in the net names in the *Net Characters* list box. The Add Net Characters dialog box appears.<br><br>Use *Remove* to delete any character that you do not want to include in the net names from the *Net Characters* list box. |
| **Vector representation of buses (DATA <0>)** | Specifies that the physical net names corresponding to individual bits in buses will be saved in the pstxnet.dat file within angular braces. For example, if you have a bus DATA <7..0>, then the individual bits would be represented as DATA <7>, DATA <6>, , and DATA <0>.<br><br>**Note:** If you do not want to save the individual bits for buses in angular braces, clear the Vector representation of buses (DATA <0>) check box and repackage the design. However, avoid making frequent changes in representation of buses through the use of this directive.<br><br>**Note:** If you have a design already packaged in release 14.2 or earlier and you are packaging it in SPB 15.2 and want vector representation for buses, then select the Vector representation of buses (DATA <0>) check box and repackage the design. |

| | |
|---|---|
| **OK** | Completes the setup process by:<br>■ Closing the Packager Setup dialog box.<br>■ Taking you back to the dialog box from which you invoked Packager Setup.<br>■ Applying the Packager Setup options, which you specified in the above selection boxes, to the design. |
| **Cancel** | Closes the Packager Setup dialog box without applying any changes to the Packager Setup options in the design. |
| **Reset** | Resets the Packager Setup options to the default values. |

### Command/Directives

To access Packager Setup from command prompt, see Command on page 182.

For more information about the Packager-XL directives modified from the Properties tab, see the following directives in *Packager-XL Reference*.

- DEFAULT_PHYS_DES_PREFIX
- NET_NAME_CHARS
- NET_NAME_LENGTH
- PART_TYPE_LENGTH
- REF_DES_LENGTH
- REF_DES_PATTERN
- REF_DES_PATTERN_FIX

# Packager Setup - Subdesign

Procedures Command/Directives

Use these setup options to package blocks in hierarchical designs.

**Generate Subdesign**

Generates a subdesign state file for use in the context of a larger design.

Use *Add* to construct a list of subdesigns that you want to include to the *Generate Subdesign* list box. When you choose *Add*, the Add Subdesign dialog box appears. You can add subdesigns using this dialog box.

Use *Remove* if you want to delete any subdesign from the Generate Subdesign list box.

**Force Subdesign**

Applies the packaging in the subdesign state file to each instance of the subdesign.

Use *Add* to construct a list of subdesigns that you want to include to the *Force Subdesign* list box. The Add Subdesign dialog box appears.

Use *Remove* if you want to delete any subdesign from the Force Subdesign list box.

**Use Subdesign**

Applies the packaging in the subdesign state file only to the new instances of the subdesign. This allows you to change the subdesign packaging without affecting the existing instances of the subdesign.

Use *Add* to construct a list of subdesigns that you want to include to the *Use Subdesign* list box. The Add Subdesign dialog box appears.

Use *Remove* if you want to delete any subdesign from the *Use Subdesign* list box.

**Subdesign Suffix Separator**

Defines a different character for renaming reference designators for reuse modules.

By default, the underscore letter (_) is used to define reference designators for reuse modules.

| | |
|---|---|
| **OK** | Completes the setup process by:<br>■ Closing the Packager Setup dialog box.<br>■ Taking you back to the dialog box from which you invoked Packager Setup.<br>■ Applying the Packager Setup options, which you specified in the above selection boxes, to the design. |
| **Cancel** | Closes the Packager Setup dialog box without applying any changes to the Packager Setup options in the design. |
| **Reset** | Resets the Packager Setup options to the default values. |

### Command/Directives

To access Packager Setup from command prompt, see Command on page 182.

For more information about the Packager-XL directives modified from the Properties tab, see the following directives in *Packager-XL Reference*.

- GEN_SUBDESIGN
- FORCE_SUBDESIGN
- USE_SUBDESIGN
- SD_SUFFIX_SEPARATOR

# Add Net Characters

The Add Net Characters dialog box allows you to add a net character to the list of net characters in the Packager Setup dialog box.

You can add a net character by entering its name in the *Net Character* field. Alternatively, you can select a net character from the *Net Character* list by clicking on the drop-down arrow button located to the right of the *Net Character* field.

After entering or selecting a net character, you can click on *OK* to enter the net character in the Packager Setup dialog box and close the Add Net Characters dialog box.

# Add Subdesign

The Add Subdesign dialog box allows you to add a subdesign to the list of subdesigns in the Packager Setup dialog box.

You can add a subdesign by entering its name in the *Add Subdesign* field. Alternatively, you can select a subdesign from the *Subdesign* list by clicking on the drop-down arrow button located to the right of the *Add Subdesign* field.

After entering or selecting a subdesign, you can click on OK to enter the subdesign in the Packager Setup dialog box and close the Add Subdesign dialog box.

# Add Property

The Add Property dialog box allows you to add a new property to the list of properties in the Packager Setup dialog box.

You can add a new property by entering its name in the *Property Name* field. Alternatively, you can select a property from the *Property Name* list by clicking on the drop-down arrow button located to the right of the *Property Name* field.

After entering or selecting a property, you can click on the *OK* button to enter the property in the Packager Setup dialog box and close the Add Property dialog box.

# Property Flow Setup

Procedures

The Property Flow Setup dialog box allows you to define the properties that will be transferred between Design Entry and PCB Editor. By defining these properties before you package a design, you can ensure that the Design Differences tool returns fewer property mismatches.

The Property Flow Setup dialog box consists of a Filter box that allows you to filter properties by owner and transferability between Design Entry HDL and PCB Editor, a grid box that defines different properties, and six buttons to control the definition of properties.

**Filter**

Controls the list of properties displayed in the dialog box. The group box includes the following options:

*Name*—Enter the name of the property or wild cards to filter properties by name. For example, if you type `ROOM` in this field and click *Apply*, then only the `ROOM` property will be displayed.

You may use wild cards such as `*` or `?` to filter results. For example, `d*` will display all properties whose name starts with the letter `d`. Similarly, `r??m` will display all property names whose first letter is `r` and fourth letter is `m`.

*Owner* —Select the owner name in this list. The default value is `All`. You can, however, select `Comp` (component), `Function`, `Net` or `Pin` in this list.

*Transfer*—Select the transfer status in this list. By default, all properties whether or not they can be transferred between Design Entry HDL and PCB Editor are displayed. You can, however, select either transferable properties or non-transferable properties by selecting the *Transfer* or *Non-Transfer* option.

**Property**

Controls the property characteristics. The *Property* grid box is organized into 5 columns as described below:

*Name*—Enter the name of the property in this field.

*Owner*—This field specifies the object to which the property can be attached. The objects supported are net, pin, component, and function.

**Note:** If a property can exist in multiple objects, then it has multiple row entries in the Property grid box. Each row corresponds to one object as owner.

*Defined In Design Entry*—Select this check box if the property can be defined in Design Entry HDL.

*Defined In PCB Editor*—Select this check box if the property can be defined in PCB Editor.

*Transfer*—Select this check box to specify that the property can be transferred between Design Entry HDL and PCB Editor along with the netlists.

**Note:** You can select the *Transfer* check box only if the property is defined both in Design Entry HDL and PCB Editor. If the property is not defined in either Design Entry HDL or PCB Editor, then the *Transfer* check box is grayed out.

**Add**

Inserts a new row at the current position. The new row has a blank value for the Property field. The *Defined In Design Entry* and *Defined In PCB Editor* check boxes are selected while the *Transfer* field is grayed out.

**Delete**

Deletes the selected row(s). If no row is selected, then the *Delete* button is grayed out.

**Import**

Launches the Import From dialog box. You can use this dialog box to import the properties from the `pxlba` file or Packaged (`pst*.dat`) files.

**OK**

Accepts all changes to the property flow setup and closes the Property Flow Setup dialog box.

**Cancel**

Reject all changes to the property flow setup and closes the Property Flow Setup dialog box.

**Help**

Displays help about setting the property flow.

**Procedures**

- Opening the Property Flow Setup Dialog Box on page 61
- Setting the Property Flow on page 64

# Import From

Procedures

The Import From dialog box is used to import the properties from the `Pxlba` file and the packaged files. To display the Import From dialog box, select the *Import* button in the Property Flow Setup dialog box.

| | |
|---|---|
| **PxIba File** | Specifies that the pxlBA.txt file would be used to import the properties. The *PxIba File* radio button is selected by default.<br><br>Enter the path to the *pxlBA* file or use the browse button to locate the file. |
| **Packaged Files** | Specifies that packaged files would be used to import the properties.<br><br>Specify the path to the folder (packaged) which contains the Packaged files by typing the path to the folder or browsing to the folder. |
| **OK** | Imports the properties from the *PxIba* or Packaged files to the Property Flow Setup dialog box. |
| **Cancel** | Reject the import operation and returns to the Property Flow Setup dialog box. |
| **Help** | Display help about importing properties. |

**Procedures**

- Setting the Property Flow on page 64
- Importing Properties on page 66

# C

# Design Differences Dialog Help

## Design Differences

Procedures

Use the Design Differences dialog box to update the package and physical views.

### Available In

The dialog box can be accessed from:

1. Project Manager—Click *Design Sync* and select the *Design Differences* option. Alternatively, select *Tools - Design Sync - Design Differences*.
2. Design Entry HDL—Select *Tools - Design Differences*. If the design is not expanded, you would be required to expand the design.

#### Function

The Design Differences dialog box runs for two flows:

- **Traditional flow**: This is the default flow. In this flow, Design Differences does not distinguish electrical property differences from other properties and displays the differences between the schematic and the board in the net and properties difference windows.

  The traditional flow is selected when you have not used Constraint Manager to manage electrical constraints in Design Entry HDL. As a result, the <*root drawing*>.dcf file is not found in the constraints view and none of the pstcmdb.dat or cmbcview.dat or cmdbview.dat files are present in the packaged view.

- **Constraint Manager-enabled flow**: In this flow, Design Differences displays constraint differences in 2 new Constraints Differences windows, one each for logical and

physical domains. Any constraint property differences are filtered from the net-properties difference windows and displayed in the new windows.

The Constraint Manager-enabled flow is selected when you have used Constraint Manager to manage electrical constraints in Design Entry HDL. You can also switch from the traditional to the Constraint Manager-enabled flow but not vice versa by selecting the *Electrical Constraints* check box (described below).

**Note:** In the Constraint Manager-enabled flow, the `netview.dat`, `cmdbview.dat`, and `pstcmdb.dat` files contain a similar tag, which is created by either Import Physical or Export Physical running in the Constraint Manager-enabled flow. If there is a difference in the tag in the `netview.dat` and `cmdbview.dat` files or the `pstxnet.dat` and `pstcmdb.dat` files, then Design Differences generates an error. Again, if the `cmdbview.dat` or the `pstcmdb.dat` file is present but the `netview.dat` file does not contain the necessary tag for the Constraint Manager-enabled flow, then Design Differences generates an error.

**Note:** If you have selected the Constraint Manager-enabled flow for one run of Design Differences, you cannot switch back to the traditional flow.

The Design Differences dialog box includes the following options:

**Update board view before compare**

Select this check box if you need to update the board file before comparing the schematic and layout.

**Note:** If you have already updated the board either in the PCB Editor or SI layout or using the Design Synchronization tool, you do not need to update the board file again, unless you have done changes to your board since your last update.

**Note:** Until you select the *Update board view before compare* check box, the PCB Editor Board box and the *Browse...* button remain unavailable for selection.

**PCB Editor Board**

Displays the output board view file (physical view) that is created when the Design Entry HDL schematic data (logical view database) is loaded in to the input board file.

**Note:** You cannot create a board by transferring the design logic to PCB Editor. You should rather update an existing board displayed in PCB Editor.

**Browse...** Select this button to display the Select Board File dialog box, where you can select the board file (for example, *start.brd*, **.brd*). To select a different board file other than the default board file, highlight the board file and click *OK*. Click *Cancel* if you do not want to select a different board file.

**Extract Constraints** Select this check box to switch to the Constraint Manager-enabled flow. When you select the *Extract Constraints* check box, Design Differences filters constraint property differences from the net-properties difference windows and displays them in the Constraints Differences windows.

**Note:** If Design Differences detects the <*root drawing*>.dcf file in the constraints view, then the *Extract Constraints* check box is selected and grayed. You cannot change it.

**Update package view before compare** Select this check box if you need to update the packaged view of the schematic design before comparing the schematic and the layout. This option is always selected by default.

**Note:** When you run Design Differences with the *Update package view before compare* check box as selected, Design Differences calls Export Physical in a special mode where the *Update PCB Editor Board* option is grayed. You can then package and/or backannotate the design. Based on your selection, Export Physical will run. When Export Physical has completed its operation, control is passed back to the Design Differences progress window. Design Differences will complete its progress and display difference windows.

**Note:** If you have already updated the packaged view, you do not need to update it again, unless you have done changes to the schematic since your last update and have not repackaged the schematic.

**Package View** Displays the packaged view directory. Packager-XL places the HDL-based transfer view files (`pstchip.dat`, `pstxnet.dat`, and `pstxprt.dat` files) in the packaged view directory within the <`Library`><`Cell`><`View`> directory structure.

| | |
|---|---|
| **Browse...** | This button displays the Select Packaged View dialog box, where you can select the packaged view (for example, packaged). To choose a different view file other than the default view file, highlight the view file and click OK. Click *Cancel* if you do not want to select a different view file. |
| **Options** | This button displays the Packager Setup dialog box. The Design Difference command gets its setup options from the project file. Use this dialog box if you need to modify the default behavior of the packager or need to choose the properties that are fed back.<br><br>**Note:** Most users do not need to make modifications to the default behavior. Click the *Help* button on this dialog box for help on the various setup options on each tab. |
| **OK** | Click this button to display the Design Differences tool. The Design Synchronization tool expands the design, packages the design, updates the PCB Editor board, and displays the Design Differences tool that allows you to see the differences between the logical (schematic) and physical views (board). |
| **Cancel** | Closes the Design Differences dialog box without comparing the design differences between the schematic and layout. |

**Procedures**


- Running Design Differences on page 111
- Viewing Any Files on page 120
- Viewing the Logical Design on page 121
- Viewing the Physical Design on page 123
- Viewing the Differences in a Text Editor on page 124
- Viewing Hierarchical Trees on page 125
- Loading the Design Views on page 127
- Synchronizing Difference Views on page 135
- Comparing Differences between Schematics and Boards on page 139
- Filtering Differences Between Schematics and Boards on page 143

# Net Difference Window

The Net Difference window displays the net differences between the logical view and the physical view in a tabular form. The table includes the following fields:

| | |
|---|---|
| **Net** | Displays a net difference. |
| **Schematic Net** | Displays the net existing in the schematic that does not exist in the layout. |
| **Board Net** | Displays the net existing in the layout that does not exist in the schematic. |
| **Where in the Design** | Displays the hierarchical logical path name of the net in the schematic. |

# Instance Part Difference Window

The Instance Part Difference Window displays the part differences between the logical view and the physical view in a tabular form. The table includes the following fields:

| | |
|---|---|
| **Part** | Displays an instance part difference. |
| **Schematic Comp Part Name** | Displays the logical part name for the instances found in the schematic that differ from the part names found in the layout. |
| **Board Comp Part Name** | Displays the part names for the instances found in the layout that differ from the part names found in the schematic. |
| **Schematic Comp Device Type** | Displays the physical part name assigned to the instance in the schematic. |
| **Board Comp Device Type** | Displays the physical part name assigned to the instance in the layout. |
| **RefDes** | Displays the reference designator of the instance. |
| **Section Number** | Displays the section number assigned to the schematic instance to identify the physical slot (function) assignment. |
| **Where in the Design** | Provides the hierarchical logical path to the instance. |

# Instance Difference Window

The Instance Difference window displays the instance differences between the logical view and the physical view in a tabular form. The table includes the following fields:

| | |
|---|---|
| **Instance** | Displays an instance difference. |
| **Part Name** | Displays the logical part name for the instance. |
| **Schematic Refdes** | Displays the reference designator for the instance in the schematic. |
| **Board Refdes** | Displays the reference designator for the instance in the layout. |
| **Section Number** | Displays the section number assigned to a schematic instance to identify the physical slot (function) assignment. |
| **Where in the Design** | Provides the hierarchical logical path to the instance. |

# Pin-net Connection Difference

The Pin-net Connection Difference window displays the connectivity differences between the logical view and the physical view in a tabular form. The table includes the following fields:

| | |
|---|---|
| **Pin** | Displays a connectivity difference. |
| **Pin Name** | Displays the logical pin name in the schematic. |
| **Pin Number** | Displays the physical pin number in the schematic. |
| **Schematic Net** | Displays the net if it exists in the schematic. |
| **Board Net** | Displays the net if it exists in the layout. |
| **Section Number** | Displays the section number assigned to the schematic instance to identify the physical slot (function) assignment. |
| **RefDes** | Displays the reference designator of the instance. |
| **Part** | Displays the logical part name for the part. |
| **Where in the Design** | Displays the hierarchical logical path to the instance pin. |

# Instance Property Difference Window

The Instance Property Difference window displays the instance property differences between the logical view and the physical view in a tabular form. The fields in this table are:

| | |
|---|---|
| **Property** | Displays a property difference attached to an instance. |
| **Name** | Displays the name of the instance property. |
| **Schematic Value** | Displays the value of the instance property that exists in the schematic. |
| **Board Value** | Displays the value of the instance property that exists in the layout. |
| **Section Number** | Displays the section number assigned to the schematic instance to identify the physical slot (function) assignment. |
| **RefDes** | Displays the reference designator for the instance. |
| **Part** | Displays the logical part name of the part in the schematic to which the instance property is attached. |
| **Where in the Design** | Displays the hierarchical logical path to the instance. |

# Pin Property Difference Window

The Pin Property Difference window displays the pin property differences between the logical view and the physical view in a tabular form. The table includes the following fields:

| | |
|---|---|
| **Property** | Displays property difference attached to a pin. |
| **Name** | Displays the name of the pin property. |
| **Schematic Value** | Displays the value of the pin property that exists in the schematic. |
| **Board Value** | Displays the value of the pin property that exists in the layout. |
| **Pin** | Displays the pin name. |
| **Pin #** | Displays the pin number. |
| **Section #** | Displays the section number assigned to the schematic instance to identify the physical slot (function) assignment in which the pin is present. |

| | |
|---|---|
| **RefDes** | Displays the reference designator of the instance on which the pin is present. |
| **Part** | Displays the logical part name on which the pin is present. |
| **Where in the Design** | Displays the hierarchical logical path to the pin. |

# Net Property Difference Window

The Net Property Difference window displays the net property differences between the logical view and the physical view in a tabular form. The table includes the following fields:

| | |
|---|---|
| **Property** | Displays property difference attached to a net. |
| **Name** | Displays the name of the net property. |
| **Schematic Value** | Displays the value of the net property that exists in the schematic. |
| **Board Value** | Displays the value of the net property that exists in the layout. |
| **Net** | Displays the name of the net to which the net property is attached. |
| **Where in the Design** | Displays the hierarchical logical path to the net. |

# Section-Swapping Difference Window

The Section-Swapping Difference window displays the section (function) swapping differences between the logical view and the physical view in a tabular form. The table includes the following fields:

| | |
|---|---|
| **Property** | Displays property difference that resulted from section swapping. |
| **Name** | Displays the names of the section properties that exist in the schematic. |
| **Schematic Value** | Displays the section assignment in the schematic. |
| **Board Value** | Displays the slot (function) assignment in the layout. |
| **Section #** | Displays the number assigned to a schematic instance to identify the physical section assignment. |

| | |
|---|---|
| **RefDes** | Displays the Reference Designator. |
| **Part** | Displays the logical part name for the part. |
| **Where in the Design** | Displays the hierarchical logical path to the instance. |

# RefDes Difference Window

The RefDes Difference Window displays the reference designator differences between the logical view and the physical view in a tabular form. The table includes the following fields:

| | |
|---|---|
| **Property** | Displays property difference that resulted RefDes swapping. |
| **Name** | Displays the name of the reference designator property attached to the instance in the schematic. |
| **Schematic Value** | Displays the value of the reference designator for an instance that exists in the schematic. |
| **Board Value** | Displays the value of the reference designator for an instance that exists in the layout. |
| **Section #** | Displays the number assigned to a schematic instance to identify the physical slot (function) assignment. |
| **RefDes** | Displays the reference designator. |
| **Part** | Displays the logical name for the part. |
| **Where in the Design** | Displays the hierarchical logical path to the instance. |

# Filter Options for Difference

Procedures

Use this dialog box to customize your own difference windows and filter out the instances that you do not need or do not want to synchronize.

### Function

The Filter Options for Difference dialog box consists of five tabbed pages. You can change the following setup options in each tab:

1. Filter Options for Difference - Instance Property—Use this tabbed page to customize your own Instance Property Difference window and filter out the instance properties that you do not need or do not want to synchronize.
2. Filter Options for Difference - Net Property—Use this tabbed page to customize your own Net Property Difference window and filter out the net properties that you do not need to see or do not want to synchronize.
3. Filter Options for Difference - Pin Property—Use this tabbed page to customize your own Pin Property Difference window and filter out the pin properties that you do not need to see or do not want to synchronize.
4. —Use this tabbed page to customize your own Instance Difference window and filter out the instances that you do not need or do not want to synchronize.
5. Filter Options for Difference - Net—Use this tabbed page to customize your own Net Difference window and filter out the nets that you do not need or do not want to synchronize.

### Procedures

- Filtering Differences Between Schematics and Boards on page 143
- Filtering Instance Properties on page 143
- Filtering Net Properties on page 144
- Filtering Pin Properties on page 144
- Filtering Instances on page 145
- Filtering Nets on page 145

# Filter Options for Difference - Instance Property

Procedures

Use this dialog box to customize your own Instance Property Difference window and filter out the instance properties that you do not need or do not want to synchronize. This dialog box includes the following fields:

| | |
|---|---|
| **Available Instance Properties** | Displays the list of instance properties that you want to retain for the Design Differences tool to compare between the schematic and layout.<br><br>**Example**:<br><br>Properties such as `GROUP`, `POWER`, `ROOM`, `VALUE`, and so on are some properties you want to retain. |
| **Ignored Instance Properties** | Displays the list of instance properties that are to be ignored for comparison. You retain in this list box all the instance properties that are unique to either the schematic or the layout.<br><br>**Example**:<br><br>Properties such as `PATH` and `XY` are properties unique to only the schematic and are never found in the layout. |
| **Add >>** | Use this button to move any instance properties from the *Available Instance Properties* list box to the *Ignored Instance Properties* list box. |
| **Remove <<** | Use this button to move any instance properties from the *Ignored Instance Properties* list box to the *Available Instance Properties* list box. |
| **Add All >>** | Use this button to move all the instance properties from the *Available Instance Properties* list box to the *Ignored Instance Properties* list box. |
| **Remove All <<** | Use this button to move all the instance properties from the *Ignored Instance Properties* list box to the *Available Instance Properties* list box. |
| **OK** | Click OK to close the dialog box. |
| **Cancel** | Click Cancel to cancel any changes to the filtering options. |

**Procedures**

- Filtering Instance Properties on page 143
- Comparing Instance Property Differences on page 140

# Filter Options for Difference - Net Property

Procedures

Use this dialog box to customize your own Net Property Difference window and filter out the net properties that you do not need to see or do not want to synchronize.

| | |
|---|---|
| **Available Net Properties** | Displays the list of net properties that you want to retain for the Design Differences tool to compare between the schematic and layout.<br><br>**Example**:<br><br>`TRACK_WIDTH` is a net property that you might want to retain for comparison. |
| **Ignored Net Properties** | Displays a list of net properties that are to be ignored for comparison. You retain in this list box all the instance properties that are unique to either the schematic or the layout. |
| **Add >>** | Use this button to move any net properties from the *Available Net Properties* list box to the *Ignored Net Properties* list box. |
| **Remove <<** | Use this button to move any net properties from the *Ignored Net Properties* list box to the *Available Net Properties* list box. |
| **Add All >>** | Use this button to move all the net properties from the *Available Net Properties* list box to the *Ignored Net Properties* list box. |
| **Remove All <<** | Use this button to move all the net properties from the *Ignored Net Properties* list box to the *Available Net Properties* list box. |
| **OK** | Click *OK* to close the dialog box. |
| **Cancel** | Click *Cancel* to cancel any changes to the filtering options. |

**Procedures**

- Filtering Net Properties on page 144
- Comparing Net Property Differences on page 141

# Filter Options for Difference - Pin Property

Procedures

Use this dialog box to customize your own Pin Property Difference window and filter out the pin properties that you do not need to see or do not want to synchronize.

| | |
|---|---|
| **Available Pin Properties** | Displays the list of pin properties that you want to retain for the Design Differences tool to compare between the schematic and layout. |
| **Ignored Pin Properties** | Displays the list of pin properties that are to be ignored for comparison. You retain in this list box all the instance properties that are unique to either the schematic or the layout. |
| **Add >>** | Use this button to move any available pin properties from the *Available Pin Properties* list box to the *Ignored Pin Properties* list box. |
| **Remove <<** | Use this button to move any pin properties from the *Ignored Pin Properties* list box to the *Available Pin Properties* list box. |
| **Add All >>** | Use this button to move all the pin properties from the *Available Pin Properties* list box to the *Ignored Pin Properties* list box. |
| **Remove All <<** | Use this button to move all the pin properties from the *Ignored Pin Properties* list box to the *Available Pin Properties* list box. |
| **OK** | Click *OK* to close the dialog box. |
| **Cancel** | Click *Cancel* to cancel any changes to the filtering options. |

**Procedures**

- Filtering Pin Properties on page 144
- Comparing Pin Property Differences on page 141

# Filter Options for Difference - Instance

Procedures

Use this dialog box to customize your own Instance Difference window and filter out the instances that you do not need or do not want to synchronize.

| | |
|---|---|
| **Available Instances** | Displays the list of instances that you want to retain for the Design Differences tool to compare between the schematic and layout. |
| **Ignored Instances** | Displays the list of instances that are to be ignored during comparison. |
| **Add >>** | Use this button to move any available instances from the *Available Instances* list box to the *Ignored Instances* list box. |
| **Remove <<** | Use this button to move any instances from the *Ignored Instances* list box to the *Available Instances* list box. |
| **Add All >>** | Use this button to move all the instances from the *Available Instances* list box to the *Ignored Instances* list box. |
| **Remove All <<** | Use this button to move all the instances from the *Ignored Instances* list box to the *Available Instances* list box. |
| **OK** | Click *OK* to close the dialog box. |
| **Cancel** | Click *Cancel* to cancel any changes to the filtering options. |

**Procedures**

- Filtering Instances on page 145
- Comparing Instance Differences on page 139

# Filter Options for Difference - Net

Procedures

Use this dialog box to customize your own Net Difference window and filter out the nets that you do not need or do not want to synchronize.

| | |
|---|---|
| **Available Nets** | Displays the list of nets that you want to retain for the Design Differences tool to compare between the schematic and layout. |
| **Ignored Nets** | Displays the list of nets that are to be ignored during comparison. |

| | |
|---|---|
| **Add >>** | Use this button to move any nets from the *Available Nets* list box to the *Ignored Nets* list box. |
| **Remove <<** | Use this button to move any nets from the *Ignored Nets* list box to the *Available Nets* list box. |
| **Add All >>** | Use this button to move all the nets from the *Available Nets* list box to the *Ignored Nets* list box. |
| **Remove All <<** | Use this button to move all the nets from the *Ignored Nets* list box to the *Available Nets* list box. |
| **OK** | Click *OK* to close the dialog box. |
| **Cancel** | Click *Cancel* to cancel any changes to the filtering options. |

**Procedures**

- Filtering Nets on page 145
- Comparing Pin-Net Connection Differences

# Query Design Window

Procedures

The Query Design window is used to search for any instance, component, net, or pin in the logical or physical view. You can narrow down the search by doing a case-sensitive or case-insensitive search, or by specifically querying using the part name, reference designator name, net name, property name-value pairs, or the canonical path name.

| | |
|---|---|
| **New...** | Displays the Add Query to input the new query options and parameters. |
| **Edit...** | Allows you to edit an existing query by bringing up the Edit Query. |
| **Find** | Brings up the *Query Logical Design - <query name> or Query Physical Design - <query name>* window, which lists all possible results of the query. |
| **Delete** | Deletes the list of existing queries. |
| **Cancel** | Cancels the query and quits the Query Design window. |

**Procedures**

- Viewing Hierarchical Trees on page 125
- Querying for a new instance, component, net, pin, or property on page 128
- Querying for another instance, component, net, pin, or property on page 132

# Query Window

Procedures

The Query window can be either:

- An Add Query window which is used to input a query

  (The *New...* button in the Query Design dialog box displays this window.)

- An Edit Query window which allows you to edit an existing query

  (The *Edit...* button in the Query Design dialog box displays this window.)

The following table describes the various selection boxes and check boxes in the Add Query or Edit Query windows:

| | |
|---|---|
| **Query Name** | Enter the name of the instance, component, net, or pin that you are searching. |
| **In Design** | Click *Schematic* or *Board* to limit your search to the logical or physical view. |
| **Find what** | Click *Instance*, *Component*, *Net*, or *Pin* to limit the search to one of these objects. |
| **Search Type** | Select *Match Case* if you want a case-sensitive search.<br>Select *Match the whole word* only if you want a whole-word search. |

| | |
|---|---|
| **Search Qualifier** | By *Part Name*: Limits the search by the complete or partial logical part names.<br><br>By *Ref Des*: Limits the search by the complete reference designators.<br><br>By *Net Name*: Limits the search by the complete net names.<br><br>By *Cname*: Limits the search by the complete canonical path of the drawing where the instance, component, net, or pin is located in the design.<br><br>By *Property Name and Value*: Limits the search by property names and property values attached to the instance, component, net, or pin. |
| **OK** | Click OK to specify the completion of the query input. The Query Design reappears with the word that you are searching filled in the Query Name box. Click Find to start your search. |
| **Cancel** | Click Cancel to cancel the query input. |

# Preview ECO on PCB Editor Board

Procedures

This dialog box lists the connectivity changes and property changes that need to be done to the physical view to update the layout and synchronize it with the logical view.

| | |
|---|---|
| **Connectivity Changes List** | Lists the connectivity changes that need to be made in the layout to synchronize the logical and physical views.<br><br>**Note:** When you double-click any of the entries listed in the *Connectivity Changes* list box or the *Property Changes* list box, the corresponding source object will be highlighted in the schematic or layout. |

| | |
|---|---|
| **Click OK button to launch Netrev to forward connectivity changes to PCB Editor board** | Always selected by default. Deselect this check box only if you do not want to forward the connectivity changes to the PCB Editor board layout. |
| **Property Changes List** | Lists the property changes that need to be made in the layout to synchronize the logical and physical views. |
| **Click OK button to launch Netrev to forward property changes to PCB Editor board** | Always selected by default. Deselect this check box only if you do not want to forward the property changes to the PCB Editor board layout. |
| **OK** | Click *OK* to accept the connectivity or property changes listed in the *Connectivity Changes List* and *Property Changes List* boxes and to update the layout. |
| **Cancel** | Click *Cancel* to close the *Preview ECO on PCB Editor Board* dialog box without making any of the listed connectivity or property changes to the layout. |
| **Save** | Click *Save* to save the layout in the packaged view as a text file called `ECOBrd.txt`. |

**Note:** If there are no connectivity or property changes to be made to the layout, the *Connectivity Changes* list box and the *Property Changes* list box will be empty.

**Procedures**

- Previewing ECO on PCB Editor Board on page 135
- Synchronizing the Board Layout on page 135

# Preview ECO on Schematic

Procedures

Lists the properties, instances, or nets that need to be modified in the logical view to update the schematic and synchronize it with the layout database.

| | |
|---|---|
| Connectivity Changes List | Lists the connectivity changes to be made in the logical view to synchronize the logical and physical views.<br><br>**Note:** When you double-click any of the entries listed in the *Connectivity Changes List* box or *Property Changes List* box, the corresponding source object will be highlighted in the schematic or layout. |
| Click OK button to launch Design Association to feedback connectivity changes to schematic | Always selected by default, this option launches the Design Association tool and generates a Design Association Markers file, `dessync.mkr`, with the connectivity changes listed in the *Connectivity Changes List* box.<br><br>**Note:** Deselect this button only if you do not want to launch Design Association to feed back the connectivity changes to the Design Entry HDL schematic. |
| Property Changes List | Lists the property changes to be made in the logical view to synchronize the logical and physical views. |
| Click OK button to launch Packager to backannotate property changes to schematic | Always selected by default. Deselect this button only if you do not want to launch Packager-XL to backannotate the property changes to the Design Entry HDL schematic. |
| OK | Click *OK* to update the schematic with the property changes (listed in the *Property Changes List* box) and to generate a Design Association Marker file with the connectivity changes (listed in the *Connectivity Changes List* box). |
| Cancel | Click *Cancel* to close the Preview ECO on Schematic dialog box without making any connectivity or property changes to the logical view. |
| Save | Click *Save* to save the layout in the packaged view as a text file called `ECOSch.txt`. |

### Procedures

- Previewing ECO on Schematic on page 135
- Synchronizing the Design Entry HDL Schematic on page 137

# D

# Design Differences Menu Help

## Menu Commands in Design Differences

This appendix describes the functions of menu commands in Design Differences. The commands are organized based on the menus.



## File Menu

### File > Load Design Entry Schematic...

Procedure

Use this command if you have updated the Design Entry HDL schematic design and would like to regenerate the differences.

This command:

- Repackages the logical schematic view.
- Reloads the updated packaged view (`pst*.dat` files) and generates the differences.

- Displays the difference view windows listing the differences, if any, that were found between the regenerated packaged view of the Design Entry HDL schematic and the PCB Editor or SI layout view.

## File > Load PCB Editor Board...

Use this command if you want to update the PCB Editor or SI layout design and would like to regenerate the differences. Also, if the PCB Editor board is changed in the back end, you can load a new board and generate the differences.

This command:

- Re-extracts the physical view from the updated PCB Editor layout.
- Reloads the updated physical design view (`view*.dat` files) and generates the differences.
- Displays the difference view windows listing the differences, if any, that were found between the regenerated PCB Editor or SI layout physical view and the packaged logical view of the Design Entry HDL schematic.

## File > Stop Loading

Stops reloading of either the updated packaged view (`pst*.dat` files) from the Design Entry HDL schematic design, or the updated physical view (`view*.dat` files) from the PCB Editor or SI board layout.

## File > View File...

Displays the *Choose File* browser window for you to view the `pst*.dat` files, `view*.dat` files, the Markers file, the log files, or other files.

## File > Update Differences

Use this command if you need to regenerate the differences between the logical view and the physical view when the other tools have changed the logical view (`pst*.dat`) files or the physical view (`view*.dat`) files. You can also use this command if the design has been repackaged, Genfeedformat has been executed, or filters have got changed.

This command:

- Updates the logical and physical views based on the filtering options.

- Displays a Message Log window with a message about the difference views that were found between the schematic and the layout.
- Displays the corresponding difference view windows.

### File > Output Difference

Procedure

Outputs the differences found between the schematic and the layout corresponding to the difference view window that is currently active. The Design Differences tool outputs these differences in a text editor. You can use the text editor to either save the differences as another file or print the differences that were generated.

### File > Exit

Closes the Design Differences tool window and the tool exits.

## Difference Menu

### Difference > Net

Procedure

Displays the differences in nets between the logical view and the physical view in a tabular form in the Net Difference window.

Net differences may have been caused when you added or deleted a net in the schematic or layout.

### Difference > Instance

Procedure

Displays the differences in instances between the logical view and the physical view in a tabular form in the Instance Difference window.

Instance differences may show up because you may have added, modified or deleted an instance in the schematic or layout.

## Difference > Instance Part

Procedure

Displays the differences in instance parts between the logical view and the physical view in a tabular form in the Instance Part Difference window.

A difference in instance part occurs when there is:

- A PACK_TYPE property change.
- A ptf (Physical Part Table (PPT) file) mapping change.

## Difference > Pin Connection

Procedure

Displays the net-pin connectivity differences between the logical view and physical view in a tabular form in the Pin-net Connection Difference window. Rewiring nets, adding instances or nets, deleting instances or nets in either the schematic or the layout causes pin-net differences.

## Difference > Inst Property

Procedure

Displays the differences in the instance properties between the logical view and the physical view in a tabular form in the Instance Property Difference window.

In the logical view, instance properties are properties attached to a schematic instance. In the physical view, instance properties are properties attached to a function inside a package.

Instance properties are transferred from the schematic to the layout in the `pstxprt.dat` file and are fed back from the layout to the schematic in the `funcView.dat` file.

Instance property differences may show up in the Instance Property Difference window because of two reasons:

- You may have added, modified, or deleted a property that is attached to an instance in the schematic or layout.
- You may have not specified the instance properties that need to be fed back within the `pxlBA.txt` file. This may cause the appearance that the instance property is missing on the schematic.

You can control the instance properties that are transferred from the schematic to the layout using the Packager Setup dialog box within Design Synchronization. However, it is advised to refrain from frequently changing the default Packager Setup options.

You can decide the instance properties that are backannotated from the layout to the schematic by specifying them in the Property Flow Setup dialog box.

## Difference > Pin Property

Procedure

Displays the differences in the pin properties between the logical view and the physical view in a tabular form in the Pin Property Difference window.

Pin properties are transferred from the schematic to the layout in the `pstxnet.dat` file and fed back from the layout to the schematic in the `pinView.dat` file.

Pin property differences may show up in the Pin Property Difference View window because of two reasons:

- You may have added, modified, or deleted a property that is attached to a pin in the schematic or layout.
- You may have not specified the pin properties that need to be fed back within the `pxlBA.txt` file. This may cause the appearance that the pin property is missing on the schematic.

You can control the pin properties that are transferred from the schematic to the layout using the Packager Setup dialog box within Design Synchronization. However, it is advised to refrain from frequently changing the default Packager Setup options.

You can decide the instance properties that are backannotated from the layout to the schematic by specifying them in the Property Flow Setup dialog box. Use the Filter Options for Difference dialog box to filter out the pin properties that you do not want to show up in the difference view windows.

## Difference > Net Property

Procedure

Displays the differences in the net properties between the logical view and the physical view in a tabular form in the Net Property Difference window.

In the logical view, net properties are properties attached to a net on the schematic. In the physical view, net properties are properties attached to a net in the layout. Net properties are transferred from the schematic to the layout in the `pstxnet.dat` file and are fed back from the layout to the schematic in the `netView.dat` file.

Net property differences may show up in the Net Property Difference window because of two reasons:

- You may have added, modified, or deleted a property that is attached to a net in the schematic or layout.
- You may have not specified the net properties that need to be fed back within the `pxlBA.txt` file. This may cause the appearance that the net property is missing on the schematic.

You can control the net properties that are transferred from the schematic to the layout using the Packager Setup dialog box within Design Synchronization. However, it is advised to refrain from frequently changing the default Packager Setup options.

You can decide the instance properties that are backannotated from the layout to the schematic by specifying them in the Property Flow Setup dialog box. Use the Filter Options for Difference dialog box to filter out the net properties that you do not want to show up in the difference view windows.

## Difference > Pin Swapping

Procedure

Displays the differences in pin swapping between the logical view and the physical view in a tabular form in the Pin-Swapping Difference window.

## Difference > Section Swapping

Procedure

Displays the differences in section (function) swapping between the logical view and the physical view in a tabular form in the Section-Swapping Difference window.

The physical section transformations file, `pstsecx.dat`, is used to reassign a logical part from an old physical section to a new physical section. This file contains the list of old-physical-section to new-physical-section pairs.

## Difference > RefDes Swapping

Procedure

Displays the differences in reference designators between the logical view and the physical view in a tabular form in the RefDes Difference window.

**Note:** For more information about difference view windows, see Design Differences Windows on page 117.

## Difference > Filter Options...

Procedure Dialog Box

Displays the Filter Options for Difference dialog box, which you can use for customizing the difference view windows by filtering out properties (instance property, net property, pin property, instance and net) that you do not need or do not want to synchronize. Click *Help* on this dialog box for more information about each Filter Options tab.

**Note:** Filter options is only for viewing the difference and in no way controls the backannotation of data.

## Difference > Property Flow Setup

Procedures Dialog Box

Displays the available properties that you can backannotate from the layout to the Design Entry HDL schematic in the Property Flow Setup dialog box. You can even control the properties that should be transferred from Design Entry HDL schematic to the PCB Editor layout.

**Note:** You can define your own properties that are to be backannotated.

### Procedures

- Opening the Property Flow Setup Dialog Box on page 61
- Setting the Property Flow on page 64

# Explore Menu

## Explore > Logical Design

Procedure

Displays the objects in the logical view of the design in the Logical Design View window. The Logical Design View window displays the objects in the logical design as a hierarchical tree view composed of components, nets, and parts

You can expand the tree by clicking on the tree node corresponding to a specific component, net, or part to get more information about the instances, pins, nets, or properties related to the component, net, or part.

## Explore > Physical Design

Procedure

Displays the objects in the physical view of the design in the Physical Design view window. The Physical Design view window displays the objects in the physical design as a hierarchical tree view composed of components, nets, and parts.

You can expand the tree by clicking on the tree node corresponding to a specific component, net, or part to get more information about the instances, pins, nets or properties attached to the component.

### Explore > Query Design...

Procedure Dialog Box

Brings up a Query Design window to enter a query to search for any instance, component, net, or pin in the logical or physical view. You can narrow down the search by doing a case-sensitive or case-insensitive search, or by specifically indicating the part name, the reference designator name, the net name, or the property name and the property value.

### Explore > Query Unconnected Comp

Brings up a Query Design window to enter a query to search for any unconnected components in the logical or physical views.

## Sync Menu

### Sync > Update PCB Editor Board...

Procedures Dialog Box

Displays the Preview ECO on PCB Editor Board dialog box.

**Note:** This command is unavailable for selection if there are no differences between the logical and physical views.

You can update the layout database by clicking *OK* on this dialog box. When you click *OK*, the Design Differences tool automatically updates all the connectivity changes as listed in the *Connectivity Changes List* box and all the property changes as listed in the *Property Changes List* box in the board layout database.

Once an update is made, the difference views are automatically updated to reflect the changes.

**Note:** Updating the physical design implies you are running the Netrev program to update the layout.

### Procedures

- Previewing ECO on PCB Editor Board on page 135
- Synchronizing the Board Layout on page 135

## Sync > Update Design Entry Schematic...

Procedures Dialog Box

Displays the Preview ECO on Schematic dialog box.

**Note:** This command remains unavailable for selection unless you have updated the Design Entry HDL schematic design (using the *File > Load Design Entry Schematic...* command) or updated the PCB Editor or SI layout view (using the *File > Load PCB Editor Board...* command), and regenerated the design differences.

You can update the Design Entry HDL schematic design by clicking *OK*. The Design Differences tool writes all the connectivity changes listed in the *Connectivity Changes List* box to the Design Association tool marker file (`dessync.mkr`) and makes all the property changes listed in the *Property Changes List* box to the schematic.

Once an update is made, the difference views are automatically updated to reflect the changes.

### Procedures

- Previewing ECO on Schematic on page 135
- Synchronizing the Design Entry HDL Schematic on page 137

# Display Menu

## Display > Highlight Source

Procedure

Highlights any instance, component, net, or pin that you have selected in the difference view window and whose source you need to locate in the Design Entry HDL schematic.

The selected object is highlighted in the Design Entry HDL schematic. Its corresponding graphical element is also highlighted in the PCB Editor or SI layout if the corresponding match exists.

## Display > Dehighlight Source

Procedure

Dehighlights any instance, component, net or pin that you have selected in the difference view window and whose source you have already located in the Design Entry HDL schematic using the *Display > Highlight Source* command.

The selected object is dehighlighted in the Design Entry HDL schematic. Its corresponding graphical element is also dehighlighted in the PCB Editor or SI layout if a corresponding match exists.

# Window Menu

## Window > Cascade

Arranges the windows of the Design Differences tool as a cascade.

## Window > Vertical Tile

Arranges all the active windows of the Design Differences tool vertically.

## Window > Horizontal Tile

Arranges all the active windows of the Design Differences tool horizontally.

## Window > Arrange Icons

Arranges all the icons relating to the active windows.

## Window > Close All

Closes all the active windows of the Design Differences tool.

# E

# Design Synchronization Dialog Help

## Export Physical

Procedures Command

Use this dialog box to transfer the logical schematic design from the Design Entry HDL editor to the physical PCB Editor or SI layout database.

### Available In

The dialog box can be accessed from:

1. Project Manager—Click *Design Sync* and select the *Export Physical* option.
2. Design Entry HDL—Select *File - Export Physical*.

#### Function

The Export Physical dialog box is used to package the design in the forward mode.

**Package Design** Select this check box if you want to package the Design Entry HDL design before exporting it to the PCB Editor or SI layout database.

**Package Option**

Specifies all the options (*Preserve*, *Optimize*, *Repackage*, or *Advanced*) for packaging your Design Entry HDL design before you export the design to the PCB Editor or SI layout database.

**Note:** This option is enabled only after you have selected *Package Design*.

**Note:** Packager-XL does not support the preserve packaging option if the value of `SUBDESIGN_SUFFIX` is changed in a design. If the value is changed, you need to repackage the design keeping the *Optimize* (non-preserve) option selected in Export Physical.

The new suffix is honored only in the non-preserve mode.

**Preserve**

Preserves all the previous packaging you have done before (incremental packaging). The default is *Preserve*.

**Optimize**

Repackages the design into a more compact physical design.

**Note:** If your design includes a design reuse block (that is, a block which has its <*block_name*>.`substate` file) and other components and you package it using the *Optimize* option, then Packager-XL will not optimize packaging between the components in the block and other components in the design. The reference designators in the reuse blocks will be retained and any optimizing will only work for components that are not part of reuse blocks.

**Repackage**

Packager-XL uses *Repackage* to ignore all previous packaging results and repackage the design. The Repackage option re-identifies parts in a design in the event some parts are added, deleted, and/or moved around. It reassigns reference designators such that they are in sequence in the schematic. If a part is moved out of the sequence, deleted, or if a new part is added, the sequence would change depending on where the change takes place. Otherwise, the sequence remains the same as the last time the design was packaged.

**Example:** There are six instances of a part, LS04, in a design, out of which two have Location property value as U12 and four as U10. When you re-run the *Export Physical* command with the *Preserve* option, the existing values of the Location property will be preserved and the part instances will continue to show different values of the Location property. However, if you select the *Repackage* option all instances of the part, LS04, will be assigned the same Location property.

**Advanced**

Displays the Packager Setup dialog box. The Export Physical command gets its packager setup options from the project file.

Use this dialog box if you need to view or modify the default behavior of the packager.

**Note:** It is advised not to make frequent changes to the default behavior. Click *Help* on the Packager Setup dialog box for help on the various Packager Setup options on each tab.

**Regenerate Physical Net Names**

Generates the physical net names for all nets. Select this check box if you have changed the net length and you have not selected repackage as the packaging option.

**Note:** You may accidentally select the *Regenerate Physical Net Names* check box and lose the assigned physical net names. You can gray out the *Regenerate Physical Net Names* check box by setting the `DISABLE_REGEN_NET_NAME` directive to `YES` in the `DESIGNSYNC` section of the project (`.cpm`) file.

**Update PCB Editor Board (Netrev)**

Transfers the Design Entry HDL design and updates the PCB Editor or SI database. If you are running Export Physical for the first time, then by default this option is not selected. As a consequence no information is imported to the board from the schematic. However, if you want to export the changes made in the schematic to the board, select the **Update PCB Editor Board (netrev)** option.

If the **Update PCB Editor Board (netrev)** option is selected and you want to only package the design using the packaging options (given above), but do not want to export it to the layout database, then deselect this option.

**Note:** If you are running Design Differences with the **Update package view before compare** option selected, then it calls Export Physical and the **Update PCB Editor Board (netrev)** option is grayed out, that is not available for selection.

**Updating PCB Editor Board Option**

Specifies all the options for updating the PCB Editor or SI layout database before you export the Design Entry HDL schematic design to the layout.

**Input Board File**

Displays the input board file or previous board file (*.brd, physical view), which is a base (template) file on the top of which the logical schematic data is placed to create the output board file.

**Browse**

Displays the Choose View File window with the Existing View File Names (*.`brd` file). You can choose a different board file (a different base template file or the old board file) from this list and click *OK*, or click *Cancel* to close this window.

**Output Board File**

Displays the output board file (*.`brd`) or the same board file that is created when the Design Entry HDL logic data is loaded onto the input board file.

**Note:** You cannot create a board by transferring the design logic to PCB Editor. You can only update an existing board displayed in PCB Editor.

**Browse**

Displays the Choose View File window with the Existing View File Names (*.brd). You can choose a different board file from this list and click OK, or click Cancel to close this window.

| | |
|---|---|
| **Allow Etch Removal During ECO** | Select this option:<br>■ To specify what to do with the connect lines that connect to the pin if an ECO removes a pin from a net.<br>■ To save time and have PCB Editor rip up this etch from a removed pin to the closest T connection or pin.<br>**Note:** Do not select this option if you want PCB Editor to rip up the etch interactively. |
| **Ignore FIXED property** | Select this option to indicate that components with FIXED property set as TRUE can also be moved or deleted. |
| **Create user-defined properties** | Select this option to create user-defined properties. User properties are added automatically into the board when you run the export physical command. When you delete such a property in Design Entry HDL, it is automatically deleted from the PCB Editor board. |

**Place Changed Components**

Tells you what to do when you load the new design logic into the PCB Editor or SI layout. An ECO (engineering change order) can result in a reference designator being assigned to a different type of device in the schematic than the device used in the PCB Editor layout.

- If the part has not changed, it maintains its location in the PCB Editor layout.
- If the part has changed, you can select one of the following options given below.

**Always**: Specifies that PCB Editor must replace all components in the layout with the new components from Packager-XL according to their reference designators. Always is the default option. The Design Synchronization tool places this new component at the same x y location and rotation as the old part.

**If Same**: Specifies that PCB Editor must replace all components in the layout with the new components from the packager, but only if the replacement component matches the package symbol, value, and tolerance of the component in the layout.

If the package symbol has changed, the old part is removed from the layout, and the changed part is added to the PCB Editor database (unplaced part).

**Never**: Specifies that PCB Editor should not replace the components in the layout with new components from the packager. You must make the changes interactively.

**Constraint Manager Data**

**Enable Export:** Specifies that Export physical will run in the Constraint Manager-enabled flow, where electrical constraints will be generated in the pstcmdb.dat file and stored in the packaged view. If this option is not selected, then electrical constraint information is stored in the pstxnet.dat file.

**Note:** The availability of *Enable Export* check box is based on whether you want to run Export Physical in the Constraint Manager-enabled flow or the traditional flow.

- **Traditional flow**: In this flow, Export Physical reads electrical constraint information, if any, and updates it in the pstxnet.dat file. Export Physical works in the traditional flow when it does not detect any constraint file (<*root drawing*>.`dcf`) in the `constraints` view. Since the constraints view is created when you run Constraint Manager from Design Entry HDL, Export Physical will be in the traditional flow when you have never run Constraint Manager from Design Entry HDL. In the traditional flow, the *Enable Export* option is disabled and grayed.
- **Constraint Manager-enabled flow**: This is the default flow. You select the Constraint Manager-enabled flow by running Constraint Manager from Design Entry HDL using the *Tools > Constraints > Edit* option. Running this option synchronizes electrical constraint information between the schematic and Constraint Manager and backannotates changes in electrical constraints in the board to the schematic. A new `constraints` view is created. When Export Physical detects this view, it works in the Constraint Manager-enabled flow. In this flow, the *Enable Export* check box is selected and grayed. You cannot change it. You can select one of the following two options:

**Overwrite current constraints**: Packager-XL overwrites all existing electrical constraint information in the Output Board file with the electrical constraint information currently available in the schematic. For example, assume that you have:

- `MAX_XTALK=0.5 mV` and `PULSE_PARAM=20 MHz` constraint on a net INT in the schematic
- `MAX_XTALK=0.4 mV` and `MAX_OVERSHOOT=40 mV` constraints on the net `INT` in the board

After you run Export Physical with the *Overwrite current constraints* option, the net `INT` in the board will have the `MAX_XTALK=0.5 mV` and `PULSE_PARAM=20 MHz` constraints on it. Note that the `MAX_OVERSHOOT=40 mV` constraint on the net `INT` in the board has got deleted. This means the following:

- If a constraint exists on a net in the schematic and the board, the constraint in the board is overwritten with the constraint in the schematic.
- If a constraint exists on a net in the schematic but does not exist on the same net in the board, the constraint is added on the net in the board.
- If a constraint does not exist on a net in the schematic but exists on the same net in the board, the constraint in the board is deleted.

**Export changes only**: Packager-XL will export only the electrical constraint information that has changed in the schematic since the last export and overwrite such constraints in the *Output Board File*. For example, assume that after the last time you ran Export Physical, you have:

- `MAX_XTALK=0.4 mV` constraint on a net `INT` in the schematic
- `MAX_XTALK=0.5 mV` on the net `INT` in the board

Now, add the `MAX_OVERSHOOT=40 mV` constraint on the net `INT` in the schematic. After you run Export Physical with the Export changes only option, the net `INT` in the board will have the `MAX_XTALK=0.5 mV` and `MAX_OVERSHOOT=40 mV` constraints on it.

Note that the value of the `MAX_XTALK` constraint on the net INT in the board has not changed. This means that only the constraint changes that you make in the schematic since the last time you ran Export Physical are updated in the board.

Before running Export Physical, if you had changed the value of the `MAX_XTALK` constraint on the net `INT` in the schematic to `0.6 mV`, the net `INT` in the board will have the `MAX_XTALK=0.6 mV` constraint after you run Export Physical.

**Show Constraint Difference Report**: Enables you to compare two constraint databases to view the constraint differences in a report viewer. The report viewer supports a simple, intuitive graphical user interface for displaying constraint differences between the two databases. Amongst other things, the report lists the objects which have changed since the last update.

For more information, see *Generating and Viewing Constraints Differences* in *Allegro Constraint Manager User Guide*.

**Backannotate Packaging Properties to Schematic Canvas**

Backannotates the latest packaging data in the board to the schematic. Select this check box to backannotate packaging data (`pstback.dat`) to the schematic when you run Export Physical.

Use this option to backannotate packaging data to the schematic on the schematic with the latest data in Constraint Manager connected to Design Entry HDL or the board.

In hierarchical designs that have non-replicated blocks, the packaging data at the root level is annotated to the schematic sheets. Therefore, the packaging data which is in-context of the root design is propagated down to the lower level blocks. With packaging data available in the schematic (lower-level) blocks, the packaging data is now available for import by other users.

When you use the backannotation process in flat designs, the packaging data, which is in the property database (.dcf), is added to the schematic sheets. While importing sheets, the packaging data is from the schematic sheets and not from the .dcf file.

**Note:** The *Backannotate Packaging Properties to Schematic Canvas* option does not backannotate board changes to the schematic. It updates the schematic with any new packaging information resulted from making changes only in the schematic. For example, if you add a part in Design Entry HDL, save the design, and then check for design differences with the *Backannotate Packaging Properties to Schematic Canvas* option checked, your added part will have the new reference designator backannotated automatically.

**Note:** Starting SPB 15.7, constraints are automatically backannotated to schematic canvas.

*Tip*

If you want the logic extracted from the board to be backannotated to the schematic, then perform an update schematic after generating the design differences.

| | |
|---|---|
| **OK** | Exports the schematic design to the layout. The following operations are performed when you choose OK:<br>■ Expands and packages the Design Entry HDL schematic design using Packager-XL.<br>■ (Constraint Manager-enabled flow) Updates the electrical constraint information by copying the <constraints/top.dcf> file as <packaged/pstcmdb.dat> file. The pstxnet.dat and pstcmdb.dat files are tagged properly so that netrev can run properly in the Constraint Manager-enabled flow.<br>■ Transfers the schematic design using netrev<br>■ Updates the physical PCB Editor or SI layout board with the latest logical schematic data<br>■ (Constraint Manager-enabled flow) Generates electrical constraint back-annotation files<br>■ Backannotates the latest packaged and constraints information to the schematic<br>■ Displays a Progress Status window with the details of the Export program |
| **Cancel** | Closes the Export Physical dialog box without exporting the schematic design to the layout. |

### Procedures

- Updating the Board with the Changes in the Schematic on page 83
- Using the State File for Successive Packager-XL Runs on page 89

### Command

You can run Export Physical from a system terminal, the Windows command prompt, by using the following command:

```
ds -dlg export -proj <path_to_file>.cpm [-test 1]
```

where,

`-test 1` is optional. It is used to run Export Physical in automode, where you need not press the *OK* button to start packaging.

This command cannot be run the DE-HDL console command window, which is accessed from *View — Console Window*.

# Import Physical

Procedures Command

Use this dialog box to transfer the physical design from the PCB Editor layout database to the Design Entry HDL schematic design.

| | |
|---|---|
| **Generate Feedback Files** | Use this option to generate the feedback files from the PCB Editor or SI layout board. The Design Synchronization generally selects this option by default. |
| **PCB Editor Board File** | Displays the input board file (*.`brd`). |
| **Browse...** | Displays the Select Board File window with a list of board file names (for example, `start.brd` or *.`brd`). From this list of board files, you can choose a different board file (other than the default board file) and click *OK*.<br><br>Click *Cancel* if you do not want to select a different board file. |

**Extract Constraints** Use this selection to decide the packaging flow. You can switch from the traditional flow to the Constraint Manager-enabled flow but not vice versa. If you select the *Extract Constraints* check box, then Import Physical runs in the Constraint Manager-enabled flow. To select this check box, ensure that the *Generate Feedback Files* check box is selected.

If Import Physical detects that you are in the Constraint Manager-enabled flow, then the *Extract Constraints* check box is selected and grayed.

**Note:** The *Extract Constraints* check box and the *Constraint Manager Data option* (detailed below) both help determine whether you are in the Constraint Manager-enabled flow or the traditional flow.

**Package Design (Feedback)** Select this option to run Packager-XL in the feedback mode. The Design Synchronization selects this option by default.

**Feedback Source** Runs Packager-XL in the feedback mode and allows you to use the feedback files from PCB Editor or a 3rd Party layout tool.

**Allegro PCB Editor** Specifies PCB Editor as the layout tool for feedback so that the `Feedback` command uses the following feedback files from PCB Editor: `pinview.dat`, `compview.dat`, `netview.dat`, and `funcview.dat` files. PCB Editor is the default option.

**3rd Party** Specifies any alternative layout tool for feedback so that the Feedback command uses the following feedback files: `pstprtx.dat`, `pstsecx.dat`, `pstnetx.dat`, and `pstfnet.dat`.

**Pstprtx**: Describes physical reference designator changes.

**Pstsecx**: Describes section changes.

**Pstnetx**: Describes physical net name changes.

**Pstfnet**: Describes the connectivity for each refdes pinNumber in the design.

**Options**

Displays the Packager Setup dialog box. The Import Physical... command gets its setup options from the project file.

Use this dialog box if you need to modify the default behavior of the Packager Setup tool or need to choose which property is fed back from the layout (using the `pxlBA.txt` file).

It is advised not to make frequent changes to the default behavior. Click *Help* on the Packager Setup dialog box for help on the various Packager Setup options on each tab.

**RF PCB Options**

Displays the RF Topology Import Settings dialog box. Use this dialog box if you need to enable RF PCB Import and modify the default RF PCB Import settings.

For more information about RF PCB Import settings, see the *RF Topology Import Settings* section in *Allegro® RF Layout-Driven Design User Guide*.

**Note:** The RF PCB Options button is enabled only with Allegro PCB RF Option.

**Constraint Manager Data**

Specifies that Import Physical will run in the Constraint Manager-enabled flow, where electrical constraints will be generated in the `cmdbview.dat` and `cmbcview.dat` files in the `packaged` view. If this option is not selected, then electrical constraint information is updated in the `pstxnet.dat` file.

**Note:** The availability of *Constraint Manager Data* options is based on whether you are in the Constraint Manager-enabled flow or the traditional flow.

**Traditional flow**: This is the default flow. In this flow, Import Physical reads electrical constraint information, if any, and updates it in the pstxnet.dat file. Import Physical works in the traditional flow when it does not detect any constraint file (<*root drawing*>.dcf) in the constraints view. Since the constraints view is created when you run Constraint Manager from Design Entry HDL, Import Physical will be in the traditional flow when you have never run Constraint Manager from Design Entry HDL.

In the traditional flow, the *Extract Constraints* check box is available for selection. If you select the *Extract Constraints* check box, a message box appears stating that you are about to move in to the Constraint Manager-enabled flow and you cannot then move back from the Constraint Manager-enabled flow to the traditional flow. If you select *Yes*, Import Physical will work in the Constraint Manager-enabled flow.

**Constraint Manager-enabled flow**: You select the Constraint Manager-enabled flow by running Constraint Manager from Design Entry HDL using the *Tools > Constraints > Update Schematic* option. Running this option synchronizes electrical constraint information between the schematic and Constraint Manager and backannotates changes in electrical constraints in the board to the schematic. A new constraints view is created. When Import Physical detects this view, it works in the Constraint Manager-enabled flow.

Import Physical will also run in the Constraint Manager-enabled flow when:

- The cmdbview.dat and cmbcview.dat files are detected
- The *Generate Feedback Files* and *Extract Constraints* check boxes are selected

In the Constraint Manager-enabled flow, you can select one of the following two options:

**Overwrite current constraints**: Packager-XL overwrites all existing electrical constraint information in the schematic with the electrical constraint information currently available in the PCB Editor Board File. For example, suppose that you have:

- `MAX_XTALK=0.5 mV` and `PULSE_PARAM=20 MHz` constraint on a net `INT` in the board
- `MAX_XTALK=0.4 mV` and `MAX_OVERSHOOT=40 mV` constraints on the net `INT` in the schematic

After you run Import Physical with the *Overwrite current constraints* option, the net `INT` in the schematic will have the `MAX_XTALK=0.5 mV` and `PULSE_PARAM=20 MHz` constraints on it. Note that the `MAX_OVERSHOOT=40 mV` constraint on the net `INT` in the schematic has got deleted. This means the following:

- If a constraint exists on a net in the board and the schematic, the constraint in the schematic is overwritten with the constraint in the board.
- If a constraint exists on a net in the board but does not exist on the same net in the schematic, the constraint is added on the net in the schematic.
- If a constraint does not exist on a net in the board but exists on the same net in the schematic, the constraint in the schematic is deleted.

**Import changes only**: Packager-XL will import only the electrical constraint information that has changed in the PCB Editor Board File since the last import and overwrite such constraints in the schematic. For example, suppose that after the last time you ran Import Physical, you have:

- `MAX_XTALK=0.4 mV` constraint on a net `INT` in the board
- `MAX_XTALK=0.5 mV` on the net `INT` in the schematic

Now, add the `MAX_OVERSHOOT=40 mV` constraint on the net `INT` in the board. After you run Import Physical with the Import changes only option, the net `INT` in the schematic will have the `MAX_XTALK=0.5 mV` and `MAX_OVERSHOOT=40 mV` constraints on it.

Note that the value of the `MAX_XTALK` constraint on the net `INT` in the schematic has not changed. This means that only the constraint changes that you make in the board since the last time you ran Import Physical are updated in the schematic.

Before running Import Physical, if you had changed the value of the `MAX_XTALK` constraint on the net `INT` in the board to `0.6 mV`, the net `INT` in the schematic will have the `MAX_XTALK=0.6 mV` constraint after you run Import Physical.

**Show Constraint Difference Report**: Enables you to compare two constraint databases to view the constraint differences in a report viewer. The report viewer supports a simple, intuitive graphical user interface for displaying constraint differences between the two databases. Amongst other things, the report lists the objects which have changed since the last update.

For more information, see *Generating and Viewing Constraints Differences* in *Allegro Constraint Manager User Guide*.

**Backannotate Packaging Properties to Schematic Canvas**

Backannotates the latest packaging data in the board to the schematic. Select this check box to backannotate packaging data (`pstback.dat`) to the schematic when you run Import Physical.

Use this option to backannotate packaging data to the schematic on the schematic with the latest data in Constraint Manager connected to Design Entry HDL or the board.

In hierarchical designs that have non-replicated blocks, the packaging data at the root level is annotated to the schematic sheets. Therefore, the packaging data which is in-context of the root design is propagated down to the lower level blocks. With packaging data available in the schematic (lower-level) blocks, the packaging data is now available for import by other users.

When you use the backannotation process in flat designs, the packaging data, which is in the property database (.dcf), is added to the schematic sheets. While importing sheets, the packaging data is from the schematic sheets and not from the .dcf file.

**Note:** The *Backannotate Packaging Properties to Schematic Canvas* option does not backannotate board changes to the schematic. It updates the schematic with any new packaging information that resulted from making changes only in the schematic . For example, if you add a part in Design Entry HDL, save the design, and then check for design differences with the *Backannotate Packaging Properties to Schematic Canvas* option checked, your added part will have the new reference designator backannotated automatically.

**Note:** Starting SPB 15.7, constraints are automatically backannotated to schematic canvas.

**OK**

Selecting *OK* executes the following:

- Runs the PCB Editor extract program to create feedback files from the active board and from the properties specified in the `pxlBA.txt` file.
- Runs Packager-XL in the feedback mode. Packager-XL creates the `*view.dat` feedback files (`pinview.dat`, `compview.dat`, `netview.dat` and `funcview.dat`) and writes the backannotation file, `pstback.dat` (Design Entry HDL uses this file to update the Design Entry HDL schematic).
- (Constraint Manager-enabled flow) Reads the electrical constraint information in the `cmbcview.dat` and `cmdbview.dat` files.
- (Constraint Manager-enabled flow) Generates electrical constraint back-annotation files. Packager-XL also extracts the constraints in the board to a file called `pstcmback.dat`.
- Transfers the physical design data from the PCB Editor layout to the Design Entry HDL schematic. The physical design changes are fed back by four methods:
  - **a.** Selecting the *Backannotate Packaging Properties to Schematic Canvas* check box in Import Physical.
  - **b.** Using the *Tools – Backannotate* command in Design Entry HDL, which feeds back property changes. This command uses the pstback.dat file to update the Design Entry HDL schematic
  - **c.** Using *Tools – Design Association* in the Design Entry HDL schematic (The Design Association tool feeds back connectivity changes.)
- Displays a Progress Status window.

**Note:** *OK* is enabled only when you have supplied a board file name in the *PCB Editor Board File* box.

Cancel

Closes the Import Physical dialog box without transferring the physical design from the PCB Editor layout database to the Design Entry HDL schematic.

### Procedures

- Updating the Schematic with the Changes in the Board on page 90
- Using the pxlBA.txt File for Controlling the Backannotation of Properties on page 97

### Command

You can run Import Physical from the command prompt by using the following command:

```
ds -dlg import -proj <path_to_file>.cpm [-test]
```

where,

-`test` is optional. It is used to run Import Physical in automode, where you need not press the *OK* button to start packaging.

# Bill of Materials

Use this dialog box to generate the Bill of Materials.

| | |
|---|---|
| **Template File** | Specifies the template file for the bill of materials report. The default template file is <*your_install_dir*>/`tools/fet/interface/template.bom`. Copy the default template to your project directory if you wish to customize the report. |
| **Browse** | Opens the Select BOM Template File browser that you can use to locate and specify the template (*.`bom`) file you want to use. |
| **Output File** | Specifies the name of the bill of materials report. The default is `bom.rpt`. |
| **Browse** | Opens the Select BOM Output File browser that you can use to locate and specify that the output file (`bom.rpt`) be saved in a different directory or under another file name. |
| **Part Table File** | Specifies a special part table file (*.`ptf`) that is used to add external property information for use in the BOM report. |
| **Browse** | Opens the Select BOM PPT File browser that you can use to locate and specify the part table file (*.`ptf` file) |
| **Use Spreadsheet Format** | Generates a comma-delimited report file typically used for importing the bill of materials into a spreadsheet program. |

| | |
|---|---|
| **Run** | Runs the Bill of Materials program and generates a new report. |
| **View** | Displays the current Bill of Materials. |
| **Close** | Closes the Bill of Materials dialog box. |

# Electrical Rules Check

Procedure

Use this dialog box to run electrical rule checks.

| | |
|---|---|
| **Check** | Allows you to select any of the following Electrical Rules Check Options: |
| **Compatible Outputs** | Checks that all outputs on a net have the same output type. The power nets are not checked. The `OUTPUT_TYPE` property determines the output type. Outputs without the `OUTPUT_TYPE` property are flagged as a `WIRED-AND` condition. |
| **Single Node Nets** | Checks that every net has at least two nodes (pins) attached to it. When you generate a Concise Net List (dialcnet.dat) report with this option selected, the resulting listing shows all the single node nets of the design.<br><br>**Note:** You can control the checking of single node nets by attaching the `NO_SINGLE_CHECK` property to it. You can also suppress the error by not selecting the *Single Node Nets* check box.<br><br>**Note:** To set the single node nets option to “on”, enter the following lines in the <projectname>.cpm file:<br>`start_gscald`<br>`single_node_nets 'on'`<br>`end_gscald`<br><br>On a Windows system, you modify the `.cpm` file by opening it in Wordpad or Notepad. Double-clicking a `.cpm` file starts Project Manager. |

**Source/Driver** Checks that each net has at least one input and output pin. A violation occurs if:

- There are no output or bidirectional pins
- There are no input or bidirectional pins
- There is only one bidirectional pin

Specify the pin direction by attaching the `INPUT_LOAD`, `OUTPUT_LOAD`, or `BIDIRECTIONAL` properties to pins.

**Note:** You can control the checking of individual pins or nets by attaching the `UNKNOWN_LOADING` or `NO_IO_CHECK` properties to them. You can also suppress the error by not selecting the *Source/Driver* check box.

**Net Loading** Checks that each output pin on the net has sufficient drive for the input loading on the net.

**Note:** You can control the checking of individual pins or nets by attaching the `UNKNOWN_LOADING` or `NO_LOAD_CHECK` properties to them. You can also suppress the error by not selecting the *Net Loading* check box.

**Pin Direction** Checks that each pin in the design is defined as input, output, or bidirectional. A violation occurs if the pin does not have the proper combination of the `INPUT_LOAD`, `OUTPUT_LOAD`, `OUTPUT_TYPE`, or `BIDIRECTIONAL` properties.

**Note:** You can control the checking of individual pins or nets by attaching the `NO_DIR_CHECK` properties to them. You can also suppress the error by not selecting the *Pin Direction* check box.

**Run** Runs the Electrical Rule Checking program and produces a report file, `erc.rpt,` containing a summary of violations, severity levels, and directive settings.

**View** Opens the `erc.rpt` file for you to view the current report.

**Close** Closes the Electrical Rules Check dialog box.

# Netlist Reports

Procedure

Use this dialog box to generate Netlist Reports.

| | |
|---|---|
| **Report To View** | Allows you to generate, select and view any of the following reports: |
| **Concise Net List (dialcnet.dat)** | Lists the nets in the design that have at least two nodes unless you enable the *Single Node Nets* option in the Electrical Rules Check dialog box. |
| **Concise Body-Ordered Net List (dialbonl.dat)** | Contains the same information as `dialcnet.dat`, but is ordered by physical part designators (body) rather than by nets. |
| **Concise Parts List (dialcprt.dat)** | Lists the part types used in the design and their quantities. |
| **Power and Ground List (dialpgnd.dat)** | Lists the physical part designators for each part type used in the design and their power and ground pins. |
| **Part Stuff List (dialstf.dat)** | Lists the part types used in the design and their reference designators. |
| **Run** | Generates updated versions of all reports. |
| **View** | Displays the current version of the selected report file (for example, `dialcnet.dat` file) for viewing. |
| **Close** | Closes the Netlist Reports dialog box. |

# Export To Packager Files

Use this dialog box to run Packager-XL in the forward mode and package your design. (You can also use the Package Design option section of the Export Physical dialog box to perform this task.)

If you do not have access to PCB Editor or the PCB Editor layout (*.brd file), you can still package the design and create the netlist files for the PCB Editor or SI layout using this dialog box.

| | |
|---|---|
| **Packager Files Location** | Displays the path to the packaged view directory where Packager-XL places the HDL-based transfer netlist files (`pstchip.dat`, `pstxnet.dat`, and `pstxprt.dat` files). |
| **Options** | Specifies all the options for packaging your Design Entry HDL design. |
| **Preserve** | Preserves all the previous packaging run results. The default is Preserve. |
| **Optimize** | Repackages the design into a more compact physical design. |
| **Repackage** | Ignores any previous packaging and regenerates new Packager-XL output files. |
| **Advanced** | Displays the Packager Setup dialog box. The `Package` command gets its setup options from the project file.<br><br>Use the Packager Setup dialog box if you need to modify the default behavior of the packager.<br><br>**Note:** It is advised not to make frequent changes to the default behavior. Click *Help* on this dialog box for help on the various packager setup options on each tab. |
| **OK** | Runs Packager-XL in the forward mode, expands and packages the design provided there were no errors. |
| **Cancel** | Closes the Export To Packager Files dialog box without packaging the design. |

**Note:** You can use the Export Physical dialog box, which contains more advanced packaging options, to package the design in the Forward mode.

# Import from Feedback Files

Use this dialog box to package the design for feedback using the feedback files produced from the PCB Editor layout. If you do not have access to the PCB Editor or SI layout, but have access to the feedback files, you can still feedback the physical design from the layout and backannotate it using the feedback files.

| | |
|---|---|
| Feedback Files Location | Displays the path to the packaged view directory that contains the feedback files. |
| Feedback Source | Runs Packager-XL in the feedback mode and specifies whether you want to use the feedback files from PCB Editor or a 3rd Party layout. |
| PCB Editor | Specifies PCB Editor as the layout tool for feedback so that the Feedback command uses the following feedback files from PCB Editor: pinview.dat, compview.dat, netview.dat and funcview.dat files. PCB Editor is the default. |
| 3rd Party | Specifies any alternative layout tool for feedback so that the Feedback command uses the following feedback files:<br><br>**Pstprtx**: Describes physical reference designator changes.<br><br>**Pstsecx**: Describes section changes.<br><br>**Pstnetx**: Describes physical net name changes.<br><br>**Pstfnet**: Describes the connectivity for each refDes pinNumber in the design. |
| Options | Displays the Packager Setup dialog box. The Feedback command gets its setup options from the project file.<br><br>Use the Packager Setup dialog box if you need:<br><br>■ To modify the default behavior of Packager-XL.<br><br>■ To choose which property is fed back from the layout (using the `pxlBA.txt` file).<br><br>**Note:** It is advised not to make frequent changes to the default behavior. Click Help on this dialog box for help on the various Packager-XL setup options on each tab. |

| | |
|---|---|
| OK | Packages the design using the feedback files from the layout (PCB Editor or 3rd Party layout) and feeds back the design to the Design Entry HDL schematic provided there were no errors. |
| Cancel | Closes the Import From Feedback Files dialog box without packaging the design for feedback. |

**Note:** You can use the Import Physical dialog box, which contains more advanced packaging options, to package the design in the Feedback mode.

# Feedback

The `Extract` command generates the following feedback files that are required to run Packager-XL in the feedback mode:

| | |
|---|---|
| **pinview.dat** | Contains the reference designator, pin number, and net name for each device pin in the schematic. |
| **compview.dat** | Contains component instance properties. |
| **netview.dat** | Contains net properties. |
| **funcview.dat** | Contains function properties. |

# Progress Status for Import

The Progress Status window appears while the Import command transfers the updated physical design from the PCB Editor or SI layout to the Design Entry HDL schematic and it contains a Details toggle button, which you can switch to No Details to avoid displaying details.

Finally, an Import From PCB Editor Board File window appears informing that "Import has successfully completed". You can click *OK* to simultaneously close this window and the Progress Status window.

If the feedback fails, an error message appears that the genfeedformat has failed. View the genfeed.log for information about the feedback errors.

**Note:** The Progress Status window for the `Export Design` command contains a *Details* button which you can switch to *No Details* to prevent the tool from displaying details. Finally, an Export To PCB Editor Board File window appears informing that the "Export has

successfully completed" and you click *OK* on this window to close this window and the Progress Status window.

F

# Design Association Dialog Help

This section contains information on the dialog boxes of Design Association:

- Design Association
- Markers List Box
- Detail Window
- Filter/Select
- SetUp

## Design Association

Procedures

Use Design Association to resolve connectivity differences between the schematic and the board.

### Available In

The dialog box can be accessed from:

1. Design Entry HDL—Select *Tools - Design Association*. If the design is not expanded, you would be required to expand the design.
2. Design Differences—First, select *Sync - Update Design Entry Schematic*. Next, select the *Click OK button to launch Design Association to feedback connectivity changes to schematic* check box and click *OK*.

### Function

The Design Association user interface window has a title bar showing the project file that you loaded in Design Entry-HDL, a menu bar, a Markers list box, a status bar, and the following buttons: Execute, Detail and Help. You can expand this user interface window to display the Detail window by clicking on the Detail button.

The Design Association user interface allows you to:

- Execute any of the Design Association menu commands.
- Select any of the actions listed in the Markers list box and execute the function associated with the action.
- Filter the actions through the Filter/Select dialog box.
- View the detailed information associated with each marker.
- Update the information corresponding to the synonyms of the net for a selected marker, location, or net in the Markers list box.

### Procedures

- Launching and Exiting Design Association on page 150
- Using Design Association on page 159

# Markers List Box

The Markers list box of the Design Association window has a list of markers provided by the input Design Synchronization marker file called `dessync.mkr`.

- Each marker corresponds to an action that the Design Association tool needs to perform to update the Design Entry-HDL schematic design.
- The nine different action types that you can execute are used to sort all the Design Association markers.
- When a marker is unexpanded, it shows the execution status of the action and the name of the action type to be executed. Each marker displays a check box to the left of it denoting the execution status of the action.
- You can expand the markers to see a hierarchical tree view of the markers by choosing the *View > Expand Markers* command from the Design Association menu bar. This is a toggle menu, which when chosen, expands all the markers.

When an action associated with a marker has not yet been executed and you click the marker, the Design Association tool automatically navigates you to the corresponding location in the Design Entry-HDL schematic. In addition, it highlights the pin-net connection (in the case of Add Net To Pin, Delete Net From Pin, or Replace Net on Pin action types) or instance (in the case of Add Instance or Delete Instance action types).

Expansion of each marker reveals more detailed information about the objects that it operates on. At any level of expansion, you can select a tree node to generate an edit of the page that the object refers to and update the default action to the one specified by the marker. Navigating to an object results in changing its parent location node in the tree to the checked state. You can expand each marker by clicking on its tree node. Each marker when fully expanded shows:

- Action Type
    - Full drawing path
        - Instance Port
            - Net (signal) name

You can control the display of markers in the tree control based on the action type, execution status, and the short message string.

**Note:** For more information about markers, see How Markers are Displayed on page 155.

# Detail Window

You can expand the Design Association user interface window to display the Detail window.

The Detail window provides detailed information about the markers listed in the Markers list box. You can select a marker in the *Markers* list box. When a marker is selected, the check box associated with the marker is highlighted. The detailed information corresponding to that selected marker appears in the Detail window. The Detail window also displays the execution status of the action. When the action is executed, the status is updated accordingly. If the action fails, it displays the reason for the failure of the action.

# Filter/Select

Procedure

Use this dialog box to specify filter options for the markers displayed in the Design Association window.

**Action Type**

Filters markers by the specified action type associated with the marker location.

The Design Association tool allows the following Action Type options:

**Delete Instance**: Deletes an instance from a design.

**Delete Net on Pin**: Deletes the net connection from a pin and deletes the associated instance from the design or deletes only the pin-net connection.

**Add Instance**: Adds an Instance to the design.

- **Add Net to Pin**: Adds a net connection to a pin.
- **Replace Net on Pin**: Replaces a net connection on a pin.
- **Add Shunt Terminator**: Adds a shunt terminator to the net on the given pin.
- **Add Series Terminato**r: Adds a series terminator to the net on the given pin.
- **Replace Instance**: Replaces an instance on the design.
- **Change Part**: Changes a part on the existing instance.

**Filter**

Select this option to indicate whether you want to filter out all the markers in the Markers list box.

**Select**

Select this option to indicate whether you want to select the markers based on the action type specified by the user.

**Execution Status**

Displays the status of the action after it has been executed. The check box next to each tree node corresponding to an action changes depending on the execution status of the action.

| | |
|---|---|
| **Short Message String** | A selection box used to filter markers based on regular expressions. This selection box accepts regular expressions. If you enter a regular expression in this selection box, the message will get filtered.<br><br>If you select the *Exclude* check box, then only those short messages, which do not match the regular expression, are passed through this filter. |
| **AND, OR** | The *AND* and *OR* radio buttons located in the *Execution Status* and the *Short Message String* selection boxes enable you to logically AND or OR the selection of markers, the execution status options and the short message string options. |
| **Select All** | Selects all the *Filter* options. |
| **DeSelect All** | Deselects all the *Filter* options. |
| **OK** | Filters markers based on your selection. |
| **Cancel** | Cancels your filtering selection and closes the Filter/Select dialog box. |

# SetUp

Procedure

Use the SetUp dialog box to specify the setup options for the page border and the interactive or automatic mode.

| | |
|---|---|
| **Interactive** | Select this option to indicate whether you want the action to be performed in the manual mode. You can specify this for adding an instance, adding a series terminator, adding a shunt terminator, and replacing a component. |
| **Automatic** | Select this option to indicate whether you want the action to be performed in the automatic mode. You can specify this for adding an instance, adding a series terminator, adding a shunt terminator, and replacing a component.<br><br>Click *Apply* to apply the setup options. |
| **Page Border** | Enter the size for the page border. |

| | |
|---|---|
| **OK** | Click *OK* to close the dialog box and save the setup options. |
| **Cancel** | Click *Cancel* to cancel any changes to the setup options. |
| **Apply** | Click *Apply* to apply the setup options. |

# G

# Design Association Menu Help

## File Menu

### File > Open

Displays the Open Marker File window for you to load the marker file corresponding to the current project. The `dessync.mkr` file is the default file, which is loaded from the Design Synchronization application. This marker file is located under the packaged view directory of the root drawing.

If you have switched projects and loaded another design in your Design Entry-HDL schematic, you need to navigate to the corresponding project directory and load the marker file.

**Note:** In multi-session Design Association flows, you can load or save a marker file at any time. The alternate locations that have been selected for actions are promoted and added to the default locations of their marker, and thus saved.

### File > Save

Procedure

Saves the current marker file in the directory from where it was read. When the file is saved, information that an action was executed or not executed is also stored.

**Note:** In multi-session Design Association flows, you can save a marker file at any time. The valid locations that have been selected for actions are promoted and added to the default locations of their marker, and thus saved.

## File > Save As...

Brings up the Save Marker File window. You can use this window to save the marker file either in the current project directory, or under another name, drive or directory.

The information that is saved in the marker file is the same as the information saved by the *File > Save* command.

## File > Save Schematic

Procedure

Saves the Design Entry schematic design so that the Design Entry design is updated with all the changes made by the Design Association tool. All the modified pages of the drawing in Design Entry-HDL are saved.

## File > Properties

Displays the Design Association window with the following:

- The path to the current marker file provided by the Design Synchronization tool in the packaged directory.

  Example:

  Marker File: `C:\cruz\user_group_5x\poa\poa\packaged\dessync.mkr`

- The path to the current project file.

  Example;

  Project Name: `C:\cruz\user_group_5x\ftb.cpm`

## File > Exit

Exits the Design Association tool.

Before exiting, the Design Association tool lets you save the current marker file and the design changes in Design Entry-HDL.

# Options Menu

## Options > Filter/Select

Procedure Dialog Box

Displays the Filter/Select dialog box. You can use this dialog box to filter the markers based on the *Action Type*, the *Execution Status*, or any arbitrary string in the *Short Message String* box. The markers you select are displayed and executed in the *Markers* list box of the Design Association window.

## Options > SetUp

Procedure Dialog Box

Displays the Setup window. You can operation mode as interactive or automatic. You can enter a new drawing page size in the selection box on that window and click *OK*. Or, you can click *Cancel* if you do not want to select a new drawing page.

If you have *Add Instance* action types, then use the *Options > SetUp* command before executing the *Action > Execute* command. When you choose the *Action > Execute* command, the Design Association tool places all the components corresponding to the Add Instance action types in the new drawing page specified by the *Options > SetUp* command.

## View > Detail

Procedure

Expands the Design Association window and displays the Detail window. The Detail window contains detailed information about the selected marker in the Markers list box. You can also display or hide from view the Detail window through the *Detail* toggle button.

## About the Detail Window

You can expand the Design Association user interface window to display the Detail window.

The Detail window provides detailed information about the markers listed in the Markers list box. You can select a marker in the *Markers* list box. When a marker is selected, the check box associated with the marker is highlighted. The detailed information corresponding to that selected marker appears in the Detail window. The Detail window also displays the execution status of the action. When the action is executed, the status is updated accordingly. If the action fails, it displays the reason for the failure of the action.

# Action Menu

## Action > Backannotate...

Procedure

Displays the Open window. You can use this window to choose the feedback for backannotating the design changes from the PCB Editor or 3rd Party layout tool to the Design Entry-HDL schematic design. The feedback files are located in the packaged view under the root drawing.

In a hierarchical schematic, all the changed design information in PCB Editor may not be fed back to it. Added instances and connectivity changes can only be backannotated if they preserve the hierarchy. The following design changes cannot be backannotated:

- A part added to one instance of a multiply-used hierarchical module
- Changes to structured (sized) parts

## Action > Mark As Completed

Procedure

Sets the Execution Status of the selected marker. You use this command to mark an action as completed once the action has been executed or to change the execution status of the action without having executed the action.

## Action > Add Location

Procedure

Adds the location of the active drawing to the current marker. These are locations that the Design Association tool cannot know about or compute without additional user input. Adding a location puts the marker in the manual state, thus re-enabling actions by converting the gray-colored check boxes that are next to the marker to magenta color.

Whenever you execute an action at a location, the location check box and its parent *Add Instance* marker check box switch to a different color indicating the status of execution. Blue color indicates successful execution of action and red color denotes failure in executing the action.

**Note:** If the location cannot be added, a gray-colored check box appears next to the marker.

If the location can be added:

- After adding a location, when you save and restore your marker file, you see your marker and the new location checked.
- The locations added with the Action > Add Location command are preceded by the magenta-colored check boxes to differentiate from other locations.
- If you subsequently save and restore the marker file, the new location you added reappears as a black icon indicating that it has been prompted to a persistent location. If you do not execute the action at the new location, it will still be saved in the marker file (unless you have deleted the location).

## Action > Delete Location

Procedure

Deletes a selected location. The *Action > Delete Location* command can only be applied to the locations in an Add Instance action type. Otherwise, the *Action > Delete Location* menu command becomes unavailable for selection.

**Note:** You cannot execute the *Action > Delete Location* command if a specific Add Instance marker has only one location. The Design Association window appears with a warning that you cannot delete that only location.

## Action > Clear Status

Procedure

If you have done a Delete or Undo action in the Design Entry-HDL schematic and need to execute the Design Association action again, you need to first clear the check box next to the marker that denotes the execution status of that specific action.

When you choose the Action > Clear Status command, the colored check box associated with the marker is cleared and changes to the unmarked status.

## View > Expand Markers

Procedure

The *View > Expand Markers* command is a toggle menu, which when chosen, expands all the markers. It is only after you select the *View > Expand Markers* command that a tree control is displayed with a tree node (+ sign) to the left of the check box next to each marker. Click the tree node next to any marker to expand the marker and see more details about that marker.

## Action > Execute

Procedure

Executes the function associated with the action for a selected marker.

Once the action is executed, the check box next to the selected marker is checked depending on the execution status of the action.

You can uncheck the marker and execute the action again by choosing the *Action > Clear Status* menu command.

You can also do a multi-selection of markers and execute all the actions associated with the selected markers all at once.

If you have selected just one marker (together with its action) to be executed, the *Execute* menu command just executes the selected action. If you have done a multiple selection of markers (together with their respective actions) to be executed, the *Execute* menu command executes all the selected actions.

**Note:** In the case of the Add Instance action type, before choosing *Action > Execute*, you must choose *Options > Set Up* and add a new drawing page. The Design Association tool places all the components to be added on the new drawing page.

# Help Menu

## Help – Documentation

Displays the Design Association Online Help.

## Help – About

Displays the version number and the release date of the Design Association tool.

# Index

## A



## B



## C



## D

# E

# F



# G



# H



# I



# L

# M



# N



# O



# P

# Q



# R



# S



# T

# U



# V



# W