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Best Practices:
Working with Rigid-Flex Designs

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Contents

Best Practices: Working with Rigid-Flex Designs

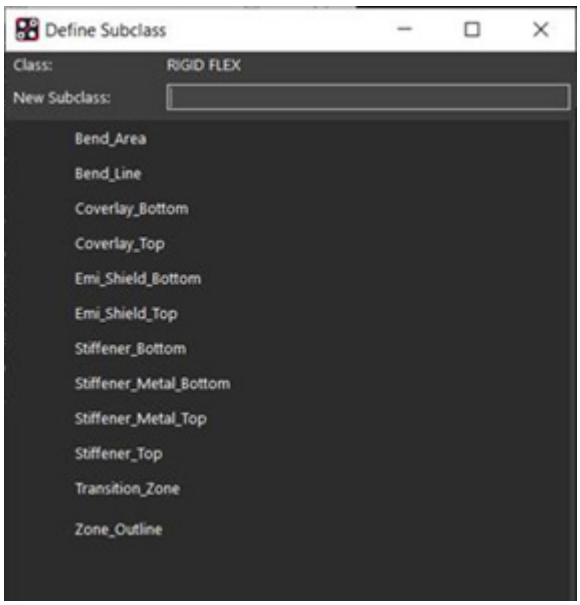
Allegro PCB Editor enables you to create a more accurate representation of a rigid-flex design using capabilities such as multiple stack up zones, bend areas, masks layers, surface finishes, and zone-aware placement to name a few of the features that are available to create the level of design data required for fabrication with minimal workarounds. Using the right functionality during the design process helps create more accurate results and lets you take advantage of the features that work together smoothly. This Best Practices document guides you to leverage these features.

Subclass Definitions

The layer structures of designs are represented by classes and subclasses in PCB Editor. Prior to 17.2, the variety of layers used to define rigid-flex designs were represented by user-defined subclasses created in the BOARD GEOMETRY, MANUFACTURING, or other class. Two new classes, RIGID FLEX and SURFACE FINISHES are introduced in 17.2 specifically for rigid-flex designs, but may also be referenced in rigid, flex, and in-lay designs.

The RIGID FLEX class is intended to be used for the structure of flex and rigid-flex designs – bend area, bend line, zones, stiffeners, and more. The SURFACE FINISHES subclass is added to provide a category for the finished materials used on a design such as tin plating, gold, Organic Solderabilty Preservative (OSP), and so on. Many of the materials used in stackup definition, including finishes can be managed in a new Mask Layer Site File. This file

controls the material names, values, and classes, customized on a company's specific requirements, to be used in the stackup definition..



When you define a rigid-flex, flex, or an inlay style design, placing user-defined subclasses into related classes helps to maintain a better organized design data. For rigid-flex, it is practical to place structural materials into the RIGID FLEX class. It might be more viable to place plating, coatings, or other non-structural materials into the SURFACE FINISHES class.

Creating Physical Outline

Even though the BOARD GEOMETRY/OUTLINE subclass remains, because of the way this layer has been used historically, its initial purpose has been altered making this subclass unreliable for identifying the true outline of the design. Use the new BOARD GEOMETRY/DESIGN_OUTLINE subclass as the main source of identifying the boundary of a design. As PCB Editor continues to be enhanced, more features can leverage this geometry as the proper 2D profile of the design.

When updating a pre-17.2 release design that do not have DESIGN_OUTLINE, the geometry on the OULTINE subclass that can be identified as the board outline and converted into a shape is copied to the DESIGN_OUTLINE subclass. The geometries in the OUTLINE subclass found in the interior of the board boundary are copied to the CUTOUT subclass. The geometries on the OUTLINE subclass determined to be outside the board boundary are ignored.

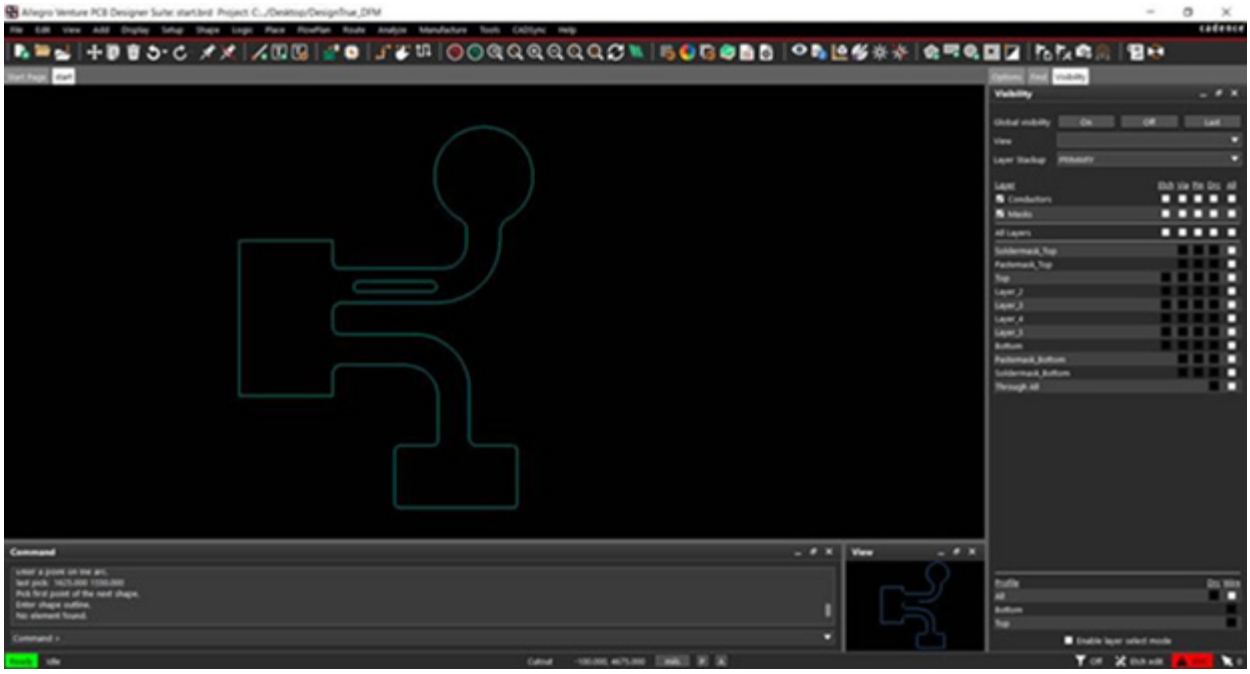
Other import/export tools that use the DESIGN_OUTLINE and CUTOUT subclasses are IDF, IDX, Artwork, and IPC-2581. The artwork command displays a pop-up warning that the

artwork layers contain the OUTLINE subclass and do not include the DESIGN_OUTLINE subclass when the situation arises. If the DESIGN_OUTLINE subclass does not exist, the other interfaces report that in the log files. For these export tools, it is strongly recommended that the DESIGN_OUTLINE subclass be used for outline creation.

Using the DESIGN_OUTLINE subclass for rigid-flex designs enables other objects related to rigid-flex design to behave more effectively, such as stackup zones that trim to the design outline. When multi- stackup zones are added within a design, if required, certain keepouts are generated that are also trimmed to the ZONE and DESIGN_OUTLINE definitions.

The DESIGN_OUTLINE geometry comprises a single unfilled closed polygon or shape. Only one DESIGN_OUTLINE geometry is allowed in a layout drawing. When IDX or IDF ECAD/MCAD exchange formats are imported or exported, only the DESIGN_OUTLINE geometry is used. Voids are not allowed in the DESIGN_OUTLINE geometry. Cutouts in the design are represented by the subclass BOARD_GEOMETRY/CUTOUT. You can add as many CUTOUTs as needed in the design, each being an unfilled shape.

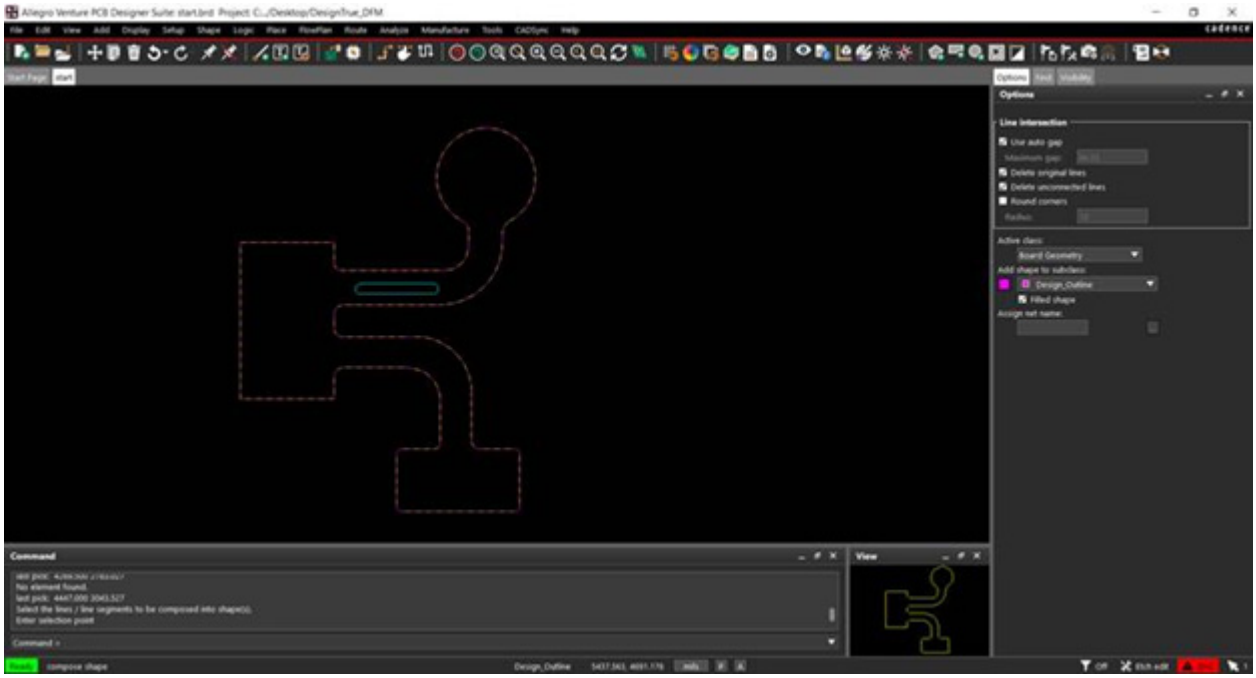
Without importing a mechanical interface (IDX, IDF, and so on) for outline creation, defining the outline using shape editing tools can often become a challenge. Defining a complex DESIGN_OUTLINE geometry can be done by creating the design profile using the BOARD_GEOMETRY or OUTLINE subclasses for the initial profile creation. Using the *Compose Shape* command, the board OUTLINE can be copied to the DESIGN_OUTLINE subclass. In the following example, a board outline with cutouts is created using the OUTLINE subclass:



To define the outline, do the following steps:

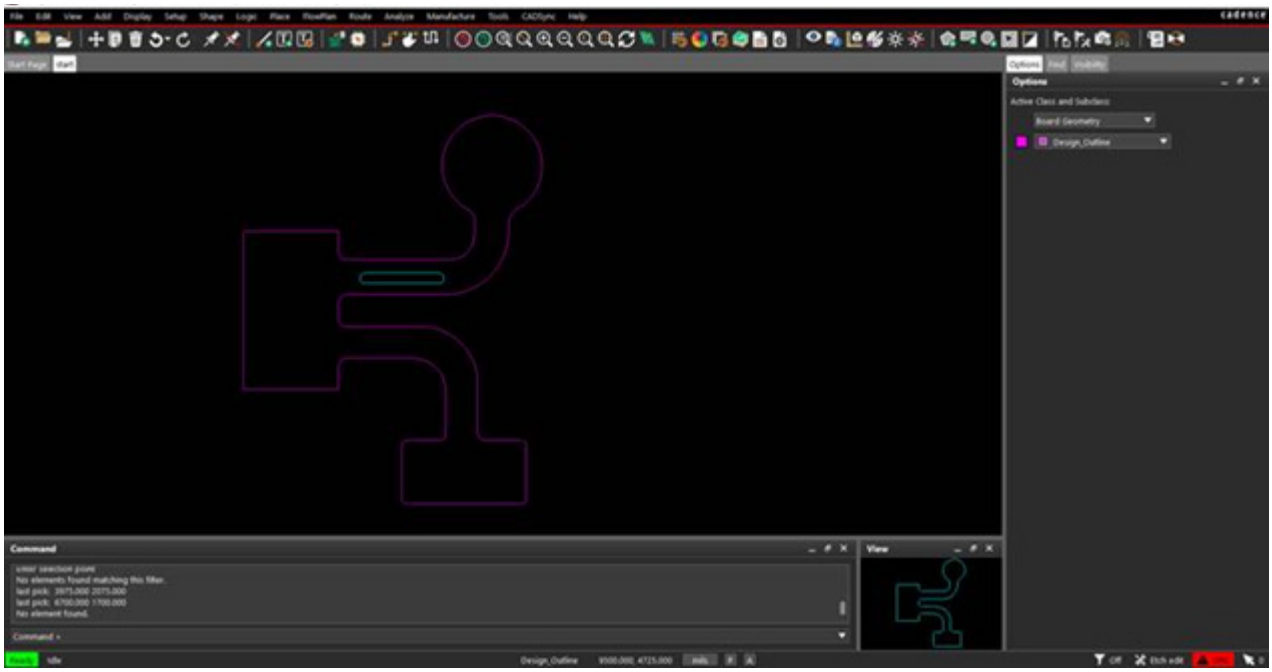
1. Choose *Shape – Compose Shape*.
2. In the Options tab, set the Active class to *BOARD GEOMETRY*.
3. Select *DESIGN_OUTLIN*E in the Add shape to subclass field.

   All the board outline external boundary elements are selected as shown by the highlighted lines and arcs:



4. Right-click the canvas and choose *Done*.

The outline geometry is copied, converted into a shape, and placed onto the DESIGN_OUTLINE subclass.

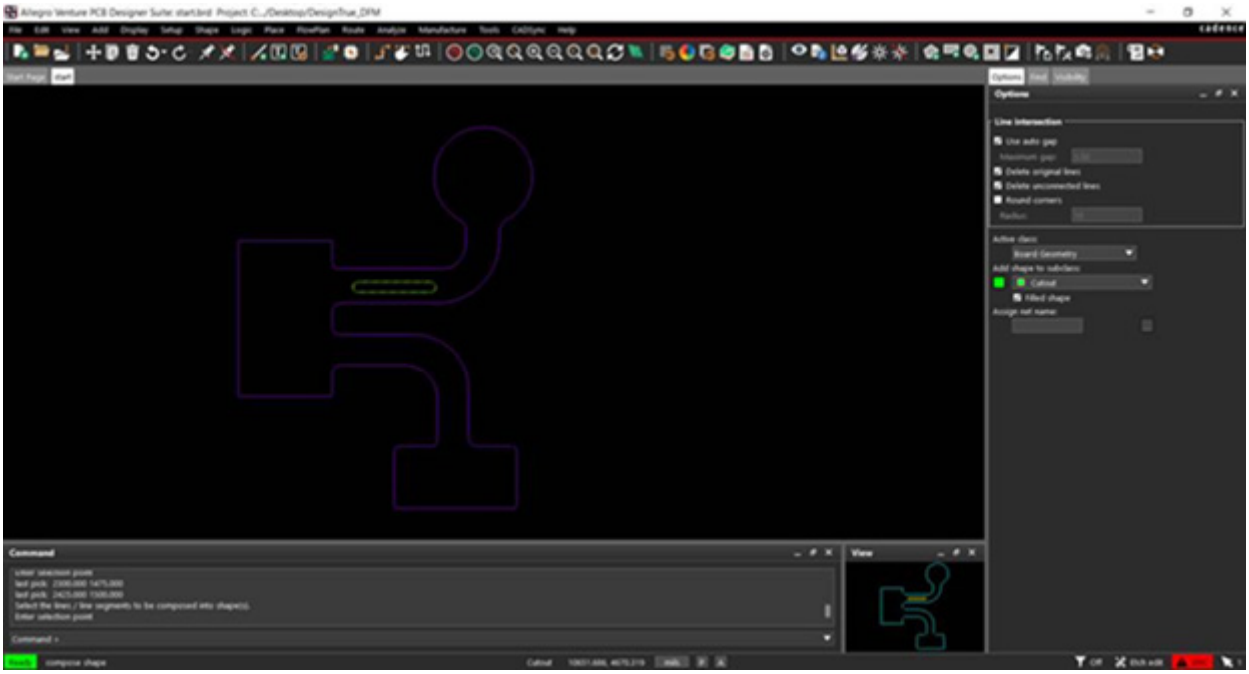


After creating the outline, you can copy the cutouts.

To copy the cutouts, do the following steps:

1. In the Compose Shape Options tab, set the Active class to *BOARD GEOMETRY*, and the subclass to which the shape is added is to *CUTOUT*.

As each item is selected, it is copied to the BOARD GEOMETRY/OUTLINE subclass.



The board outline or a cutout might not be created if a closed shape is not created. Check the geometries for gaps at intersections, or where line/arc segments form an overlapping where a shape boundary will overlap itself.

2. Right-click and choose *Find Break* from the pop-up menu.

   This command zooms into the location for any breaks that prevent the creation of the closed shape.

Creating Rigid-Flex Stackups

You can add mask layers above the TOP conductor layer and below the BOTTOM conductor layer. Soldermask, pastemask, coverlay, and son can be included as part of the stackup definition. The stackup definition for flex and rigid designs commonly includes a single stackup definition where the design has a single uniform layer stackup through the entire cross-section. PCB designs that leverage material inlay or rigid-flex technology, use non-uniform stackups across the design with two or more different layer stackup definitions. Cross Section Editor provides the capability of defining multiple stackup definitions.

The selection of materials used in a design have an impact on the performance, productibility, and function of a design. Careful attention should be given to the selection and use of materials and it should be in accordance with the company's standards. However, the key in getting proper stackup materials is the collaboration with the intended fabricator(s) who will

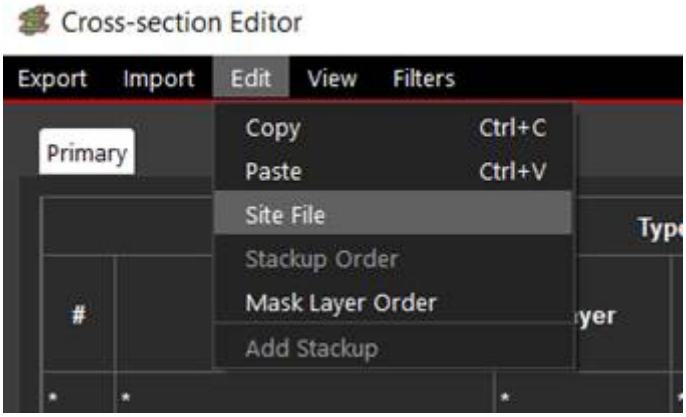
provide proper materials. Proper choices made in the preliminary phases of the design helps eliminate issues later in the design and fabrication process.

Always update the `materials.dat` file with the latest materials. Many of the mask layers and material used should also be maintained in the materials.dat file. Use the *Mask Layer Site File* to specify the stackup definition for assigning different mask type layers. The materials and their definitions in the materials.dat file are referenced from the Mask Layer Site File.

Mask Layer Site File

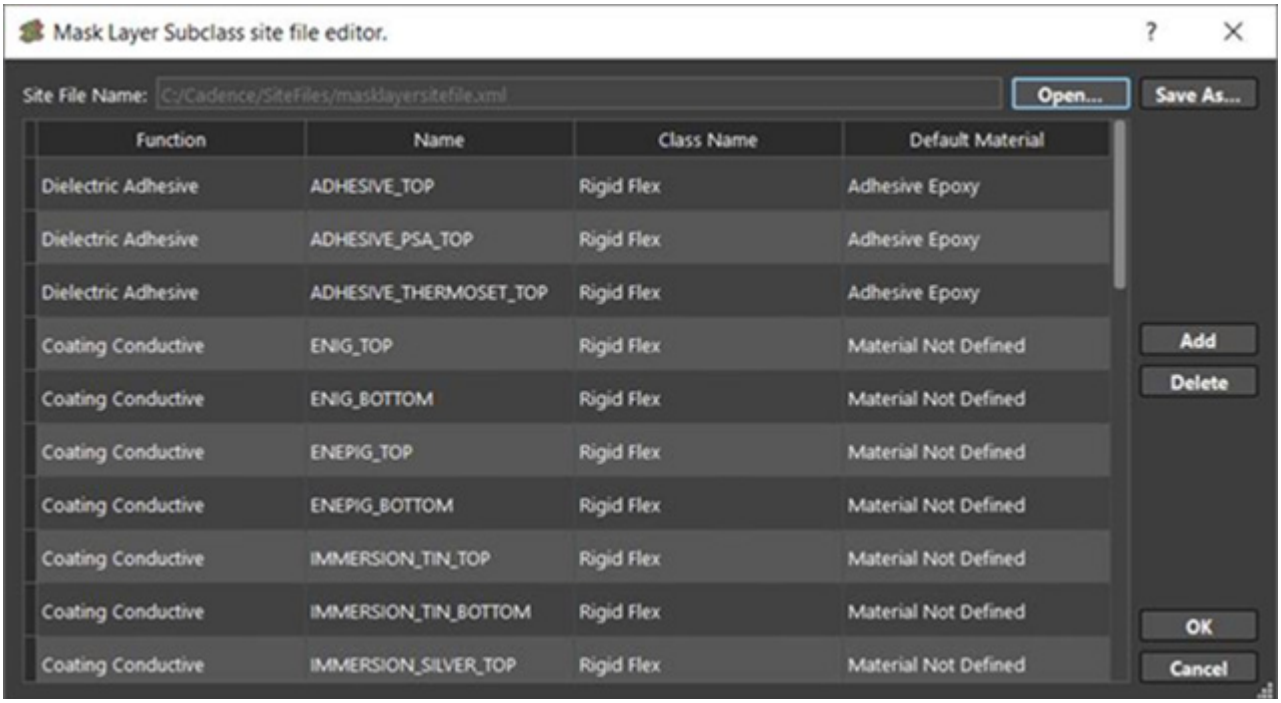
Maintaining consistent layer names, materials, and stackup data is possible by using the Cross Section Technology File to import and export the stackup data. Creating a library of standard stackups for rigid PCBs is a minor task compared to the limitless possibilities that rigid-flex designs offer. Maintaining common layer names for the many mask and dielectric structures used in a rigid-flex design can be better managed using the Mask Layer Site File.

The Mask Layer site file should be accessible to all the users and located within the *MATERIALPATH* env definition in Allegro PCB Editor. Edit the file using the *Edit – Site File* menu command in Cross Section Editor.



The Mask Layer site file editor allows you to add, delete, and modify material entries for use in the stackup definition. The data provided in the Mask Layer site file helps in maintaining consistency between designs. The materials approved by company policies, should be listed

in this file along with the intended function type, based on the IPC-2581 data exchange standards.



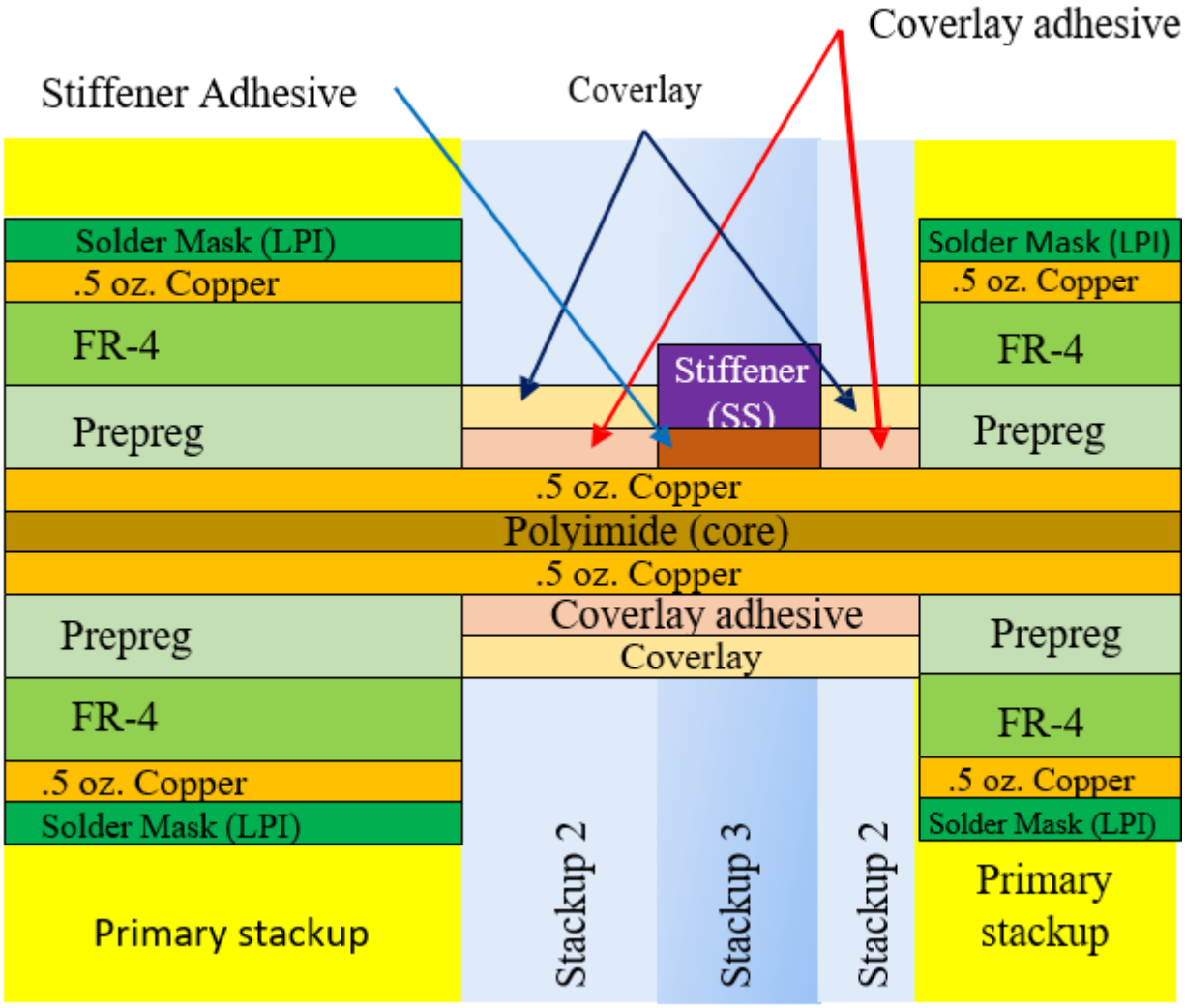
The Mask Layer file provides the following data:

- Function: The assignment of IPC Layer Function Type as defined by IPC-2581. The value set for this field is from a pull down menu of legal values. Choose the type that fits closest to the intended use of the layer.
- Name: This is the name of the subclass used in the design database. The default name is MASK_0. This name may be any legal subclass name.
- Class Name: There are four legal classes to which a layer can be assigned. Surface Finishes, Rigid Flex, Package Geometry, and Board Geometry. The class selected should best fit the intended use of the subclass being created.
- Default Material: A pull down list of available material as defined in the materials.dat file. The value selected becomes the default material value for this layer.

Building and maintaining an accurate Mask Layer Site file will save time when initially setting up a new design and provide accurate data for manufacturing. Working with the fabricator to define the materials will assist in creating a well-defined set of materials.

Rigid Flex Design Structure Example

Rigid flex designs consist of multiple materials and thickness across the entire design. Each of these materials is represented by different layers in the PCB Editor cross section. Various mask types, dielectrics, stiffeners, and copper layers are combined in different ways to build up the various thicknesses determining which zone is flexible and which zone is rigid. The following diagram is an example of a rigid-flex design structure, where the buildup of materials create the various rigid and flex zones.



There are three basic stackup definitions in Cross Section:

- The first group of materials identified in the image as *Primary Stackup* represents the rigid zones of the design.

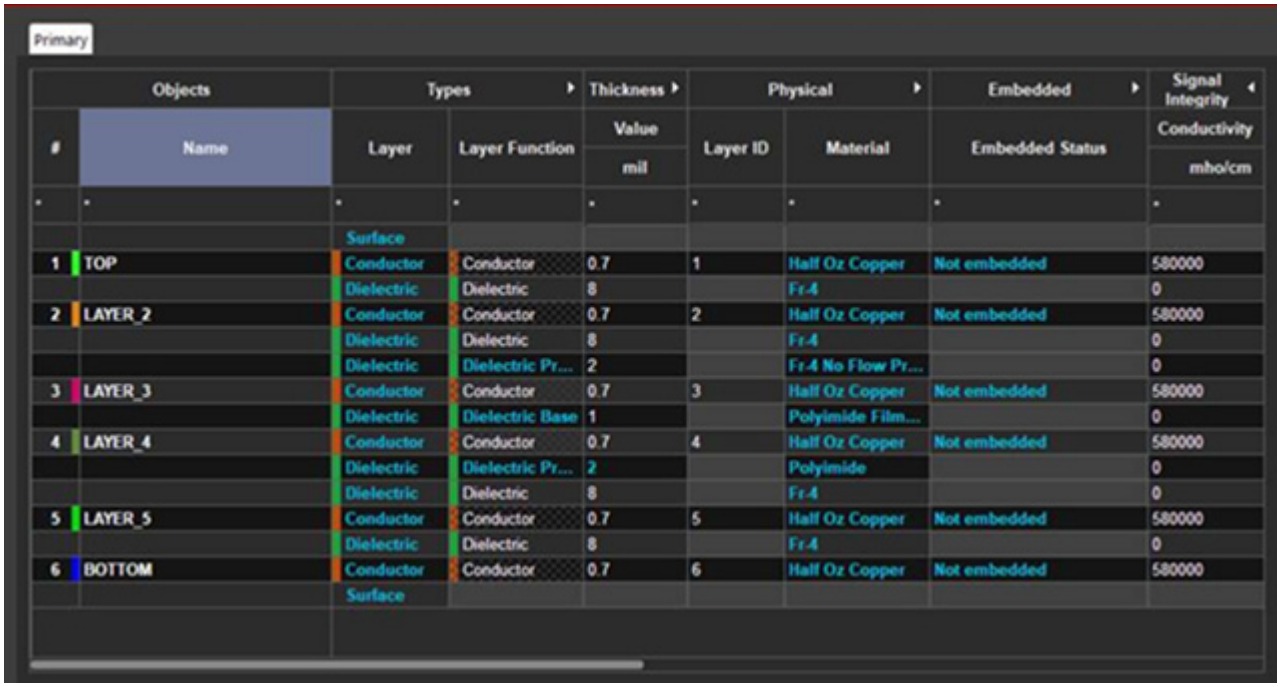
- The second stackup group, identified as *Stackup 2*, represents the flex zones of the design.
- *Stackup 3* represents a flex zone with a stiffener making the zone “inflexible”.

In Cross Section Editor, do the following tasks:

1. Define the Primary stackup definition.

   By default, Cross Section Editor contains a single Dielectric layer and two copper layers. This is the default Primary layer.

2. Add four more copper layers.
3. Add multiple dielectric layers as illustrated in the following figure:

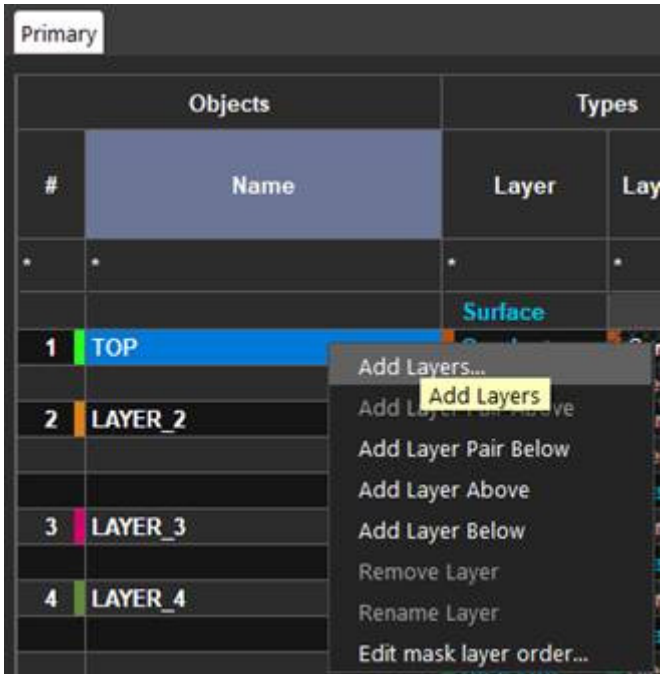


Objects		Types		Thickness	Physical		Embedded	Signal Integrity
#	Name	Layer	Layer Function	Value mil	Layer ID	Material	Embedded Status	Conductivity mho/cm
		Surface						
1	TOP	Conductor	Conductor	0.7	1	Half Oz Copper	Not embedded	580000
		Dielectric	Dielectric	8		Fr-4		0
2	LAYER_2	Conductor	Conductor	0.7	2	Half Oz Copper	Not embedded	580000
		Dielectric	Dielectric	8		Fr-4		0
		Dielectric	Dielectric Pr...	2		Fr-4 No Flow Pr...		0
3	LAYER_3	Conductor	Conductor	0.7	3	Half Oz Copper	Not embedded	580000
		Dielectric	Dielectric Base	1		Polyimide Film...		0
4	LAYER_4	Conductor	Conductor	0.7	4	Half Oz Copper	Not embedded	580000
		Dielectric	Dielectric Pr...	2		Polyimide		0
		Dielectric	Dielectric	8		Fr-4		0
5	LAYER_5	Conductor	Conductor	0.7	5	Half Oz Copper	Not embedded	580000
		Dielectric	Dielectric	8		Fr-4		0
6	BOTTOM	Conductor	Conductor	0.7	6	Half Oz Copper	Not embedded	580000
		Surface						

   The Soldermask top and bottom layers may now be added.

4. Add the top soldermask layer.
5. Place the cursor on the TOP conductor layer.

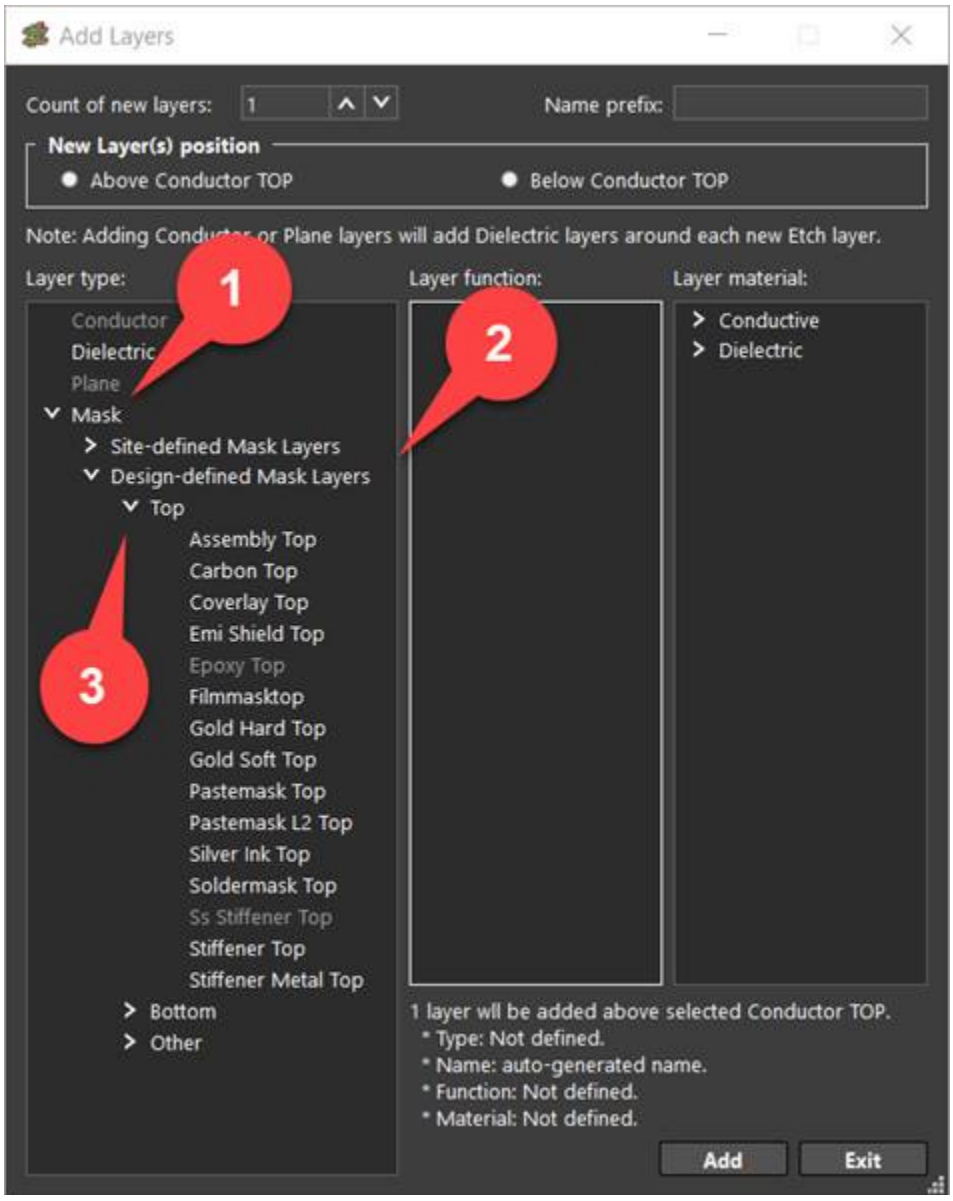
6. Right-click and choose *Add Layers* from the pop-up menu.



This opens the Add Layers form. This form references the existing subclass data that currently exists in the design and also references the Mask Layer Site File and materials.dat file.

SOLDERMASK_TOP is the default subclass as a Design-defined mask layer.

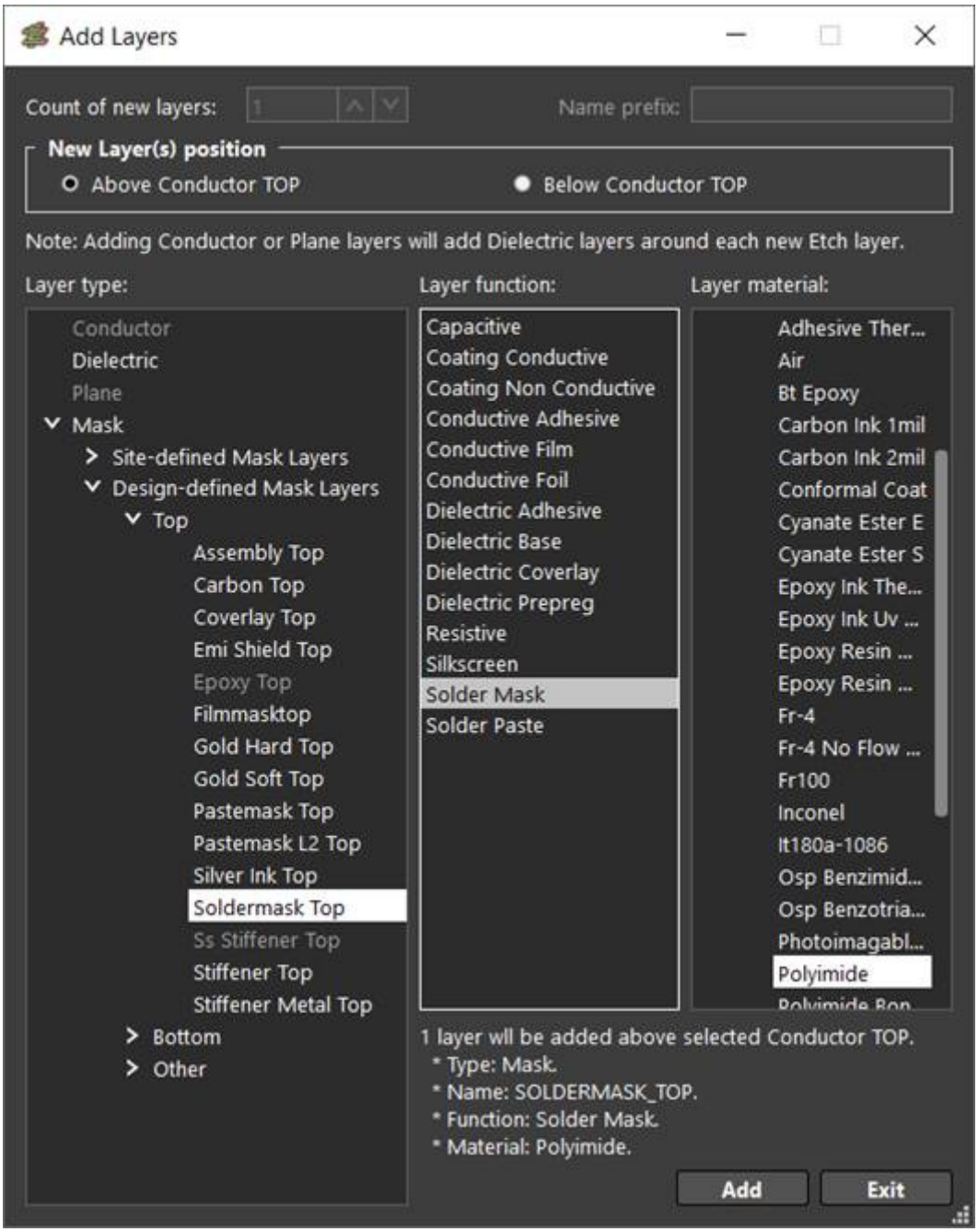
7. In the Layer Type tree of the Add layers form, expand the *Mask – Design-defined Mask Layers – Top Node*.



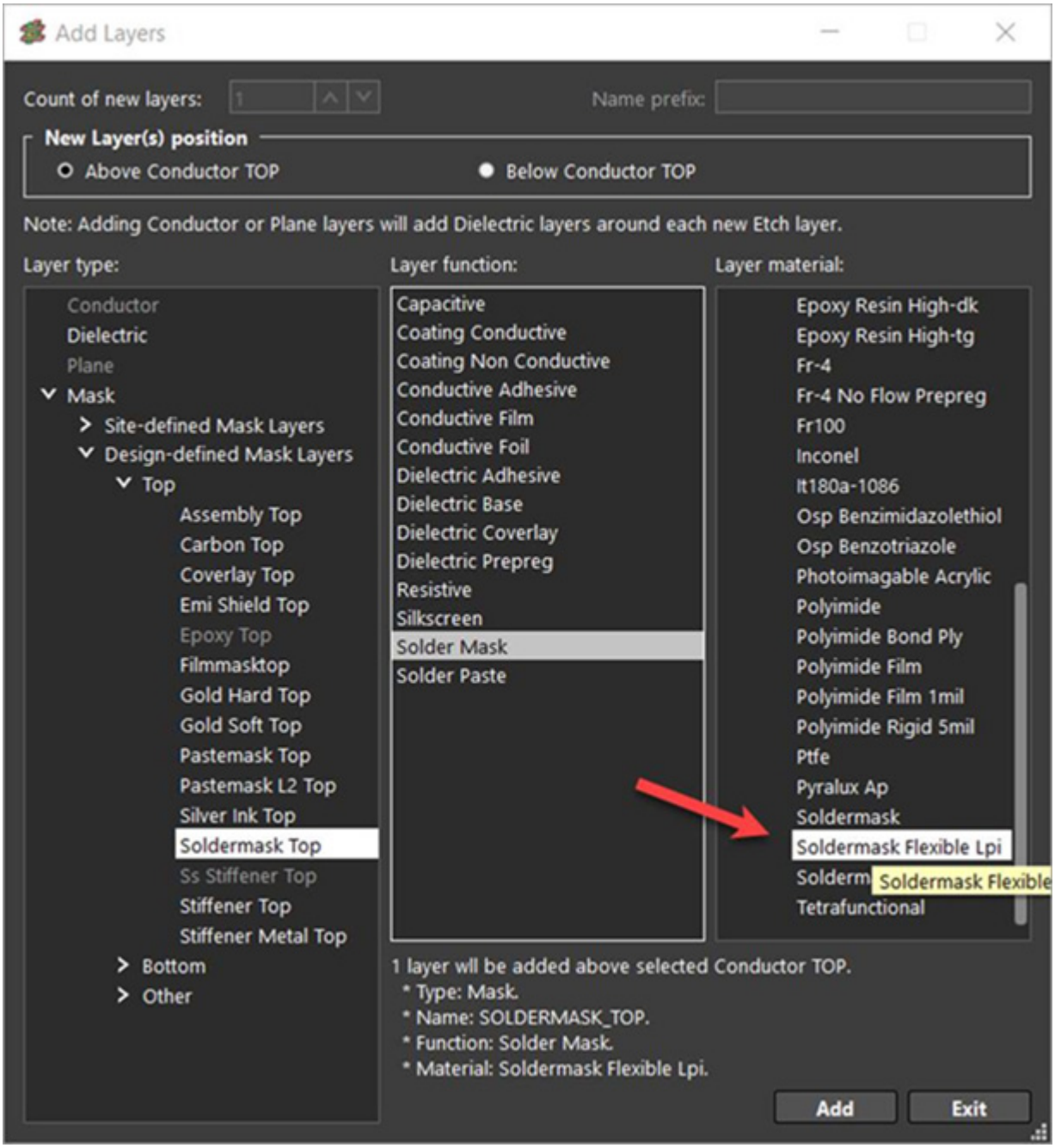
The mask layer subclasses defined in the design are listed under the *Top* category.

8. Select the *Soldermask Top* node.

As the node is selected, the default values for this layer are also highlighted in the Layer Function and Layer Materials columns. If required, override the default by selecting another entry in either the function or the material columns.

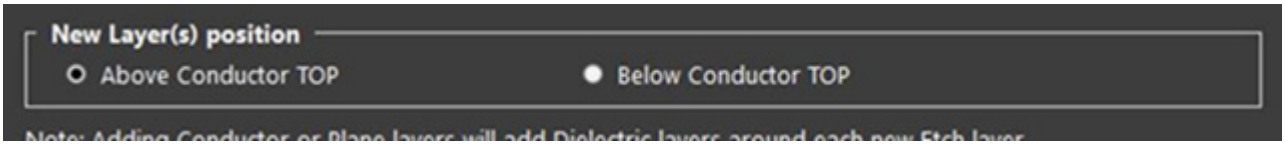


The summary at the bottom of the form displays the selection and the associated function and materials. For this example, the Layer material will be changed to Soldermask Flexible Lpi.



The summary also indicates that the new layer will be added above the TOP conductor layer. The location of the new layer is related to the initial selection made in Cross Section

Editor, in this case TOP, and the option button for the New Layer(s) position area of the Add Layers form.

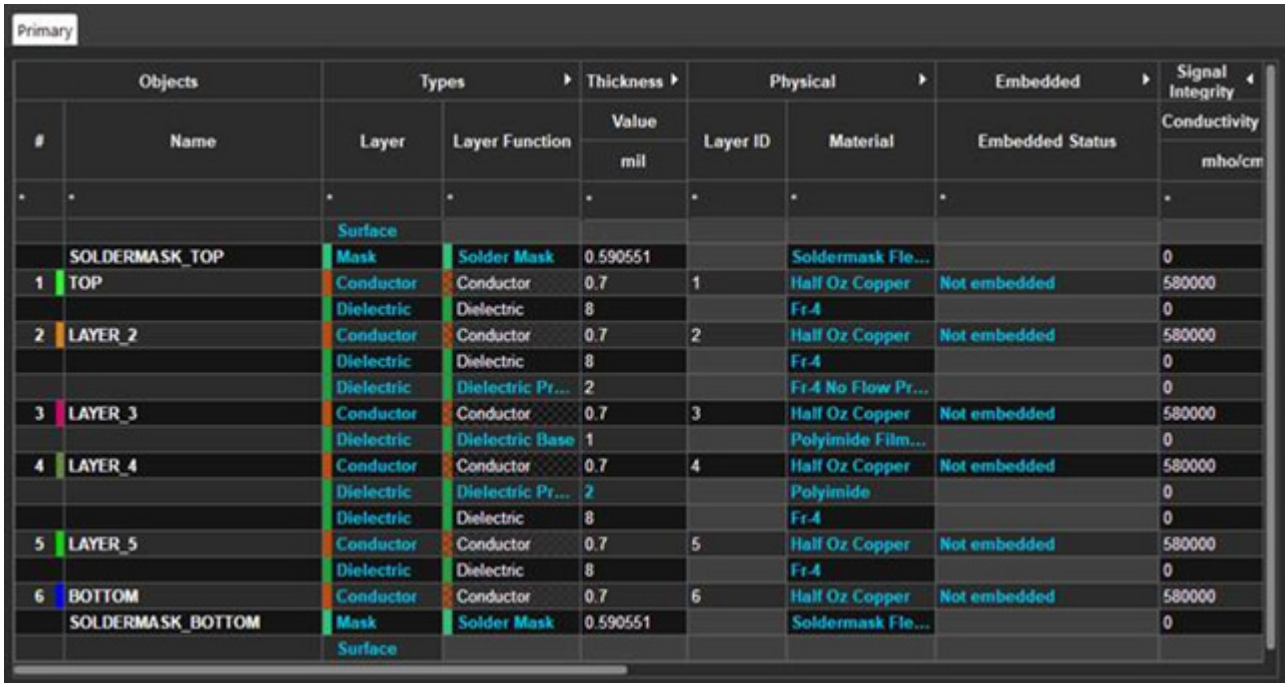


9. To apply the changes, click *Add*.

   The Primary Stackup definition is updated. Using the same methodology, the SOLDERMASK_BOTTOM can be added. This can be done without exiting the Add Layers form

10. Select the BOTTOM conductor subclass in the Primary stackup.
11. Select the *Below Conductor BOTTOM* option in the Add Layers form.
12. Expand the *Mask – Design-defined Mask Layers – Bottom* node.
13. Select *Soldermask Bottom*.
14. Add the new layer.

    The Primary stackup is updated.

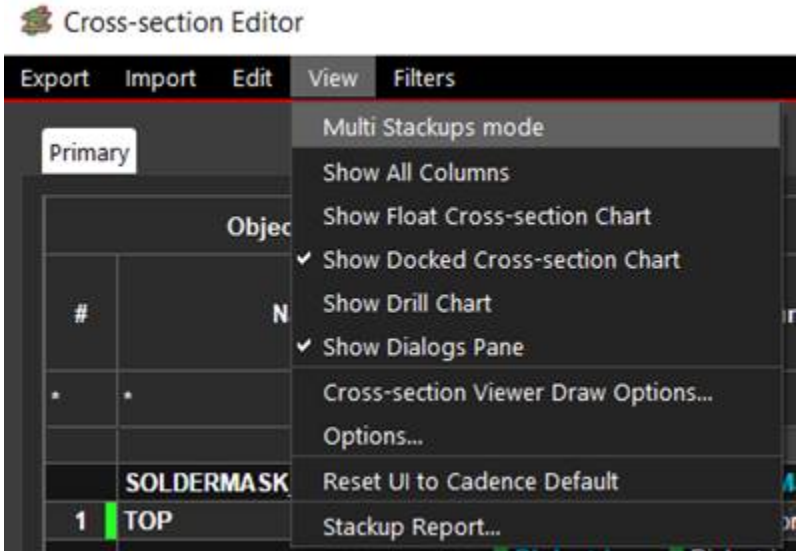

Primary

Objects		Types		Thickness	Physical		Embedded	Signal Integrity
#	Name	Layer	Layer Function	Value mil	Layer ID	Material	Embedded Status	Conductivity mho/cm
		Surface						
	SOLDERMASK_TOP	Mask	Solder Mask	0.590551		Soldermask Fle...		0
1	TOP	Conductor	Conductor	0.7	1	Half Oz Copper	Not embedded	580000
		Dielectric	Dielectric	8		Fr-4		0
2	LAYER_2	Conductor	Conductor	0.7	2	Half Oz Copper	Not embedded	580000
		Dielectric	Dielectric	8		Fr-4		0
		Dielectric	Dielectric Pr...	2		Fr-4 No Flow Pr...		0
3	LAYER_3	Conductor	Conductor	0.7	3	Half Oz Copper	Not embedded	580000
		Dielectric	Dielectric Base	1		Polyimide Film...		0
4	LAYER_4	Conductor	Conductor	0.7	4	Half Oz Copper	Not embedded	580000
		Dielectric	Dielectric Pr...	2		Polyimide		0
		Dielectric	Dielectric	8		Fr-4		0
5	LAYER_5	Conductor	Conductor	0.7	5	Half Oz Copper	Not embedded	580000
		Dielectric	Dielectric	8		Fr-4		0
6	BOTTOM	Conductor	Conductor	0.7	6	Half Oz Copper	Not embedded	580000
	SOLDERMASK_BOTTOM	Mask	Solder Mask	0.590551		Soldermask Fle...		0
		Surface						

   The graphical representation of the stackup located on the left side of Cross-section Editor reflects the current stackup.

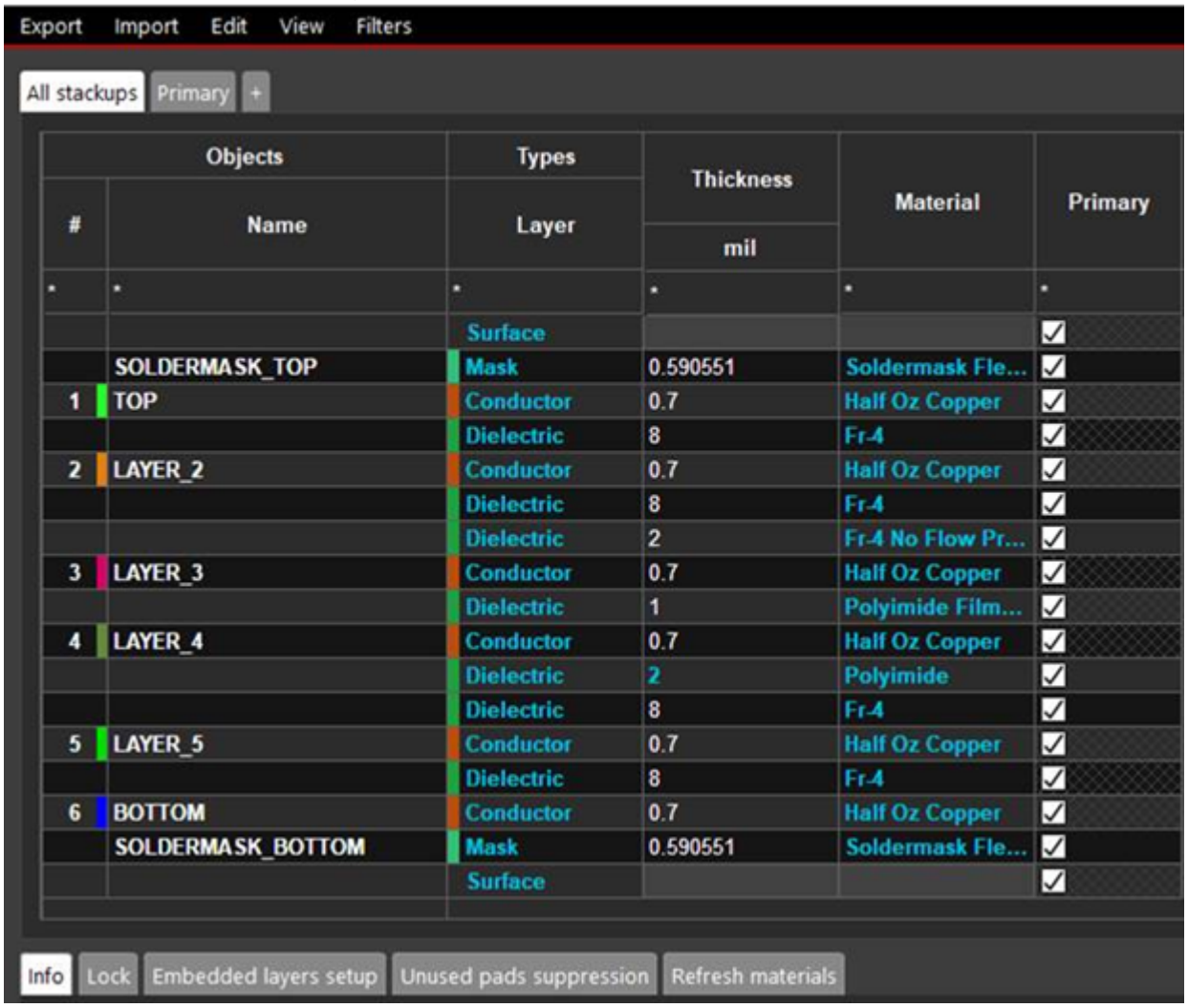
The next step is to define the flexible stackup of the design.

1. In Cross Section Editor, choose the *View – Multiple Stackups mode*.

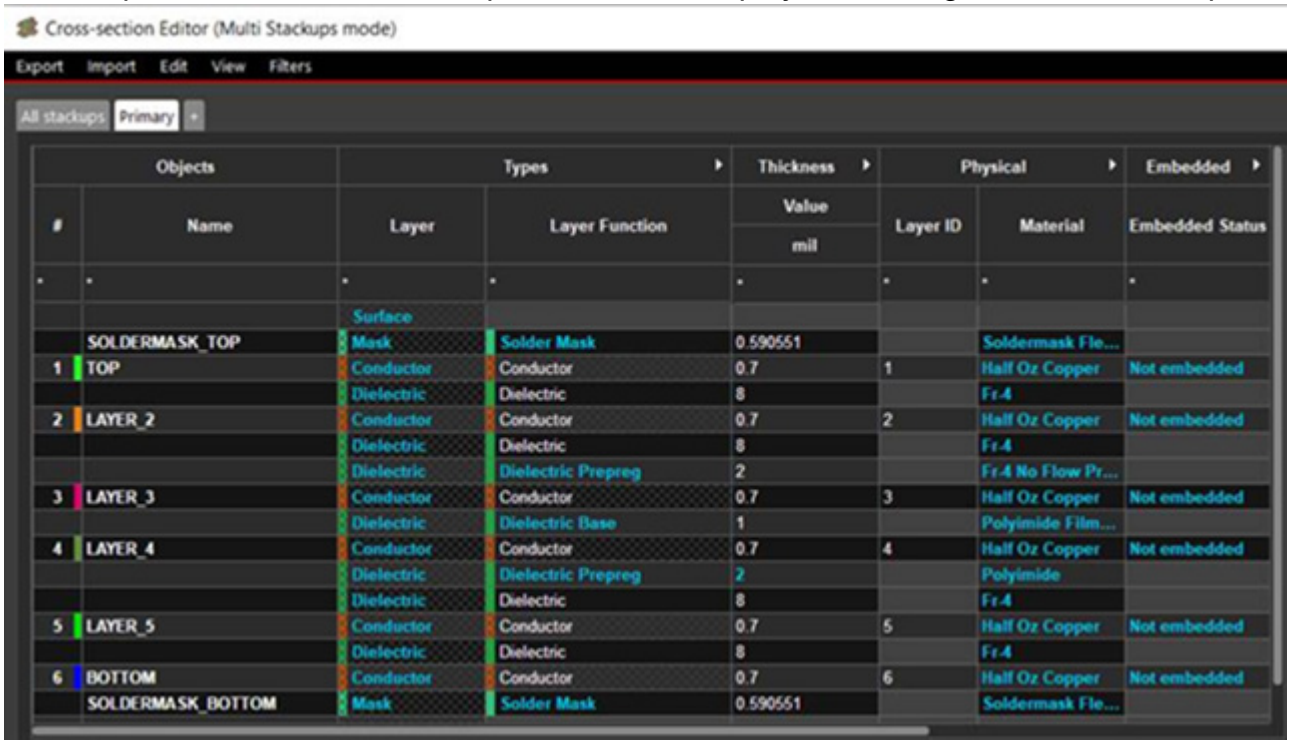


This mode alters the stackup table. The display now contains tabs for All stackups, Primary, and “+”. The All stackups tab displays all the layers defined in the design with a

column for each of the defined stackups. The check boxes in each stackup column indicate the layers assigned to the stackup definition.



When a stackup definition tab is selected Primary for instance, only the layer definitions and parameters for that stackup definition are displayed, and might be edited as required.

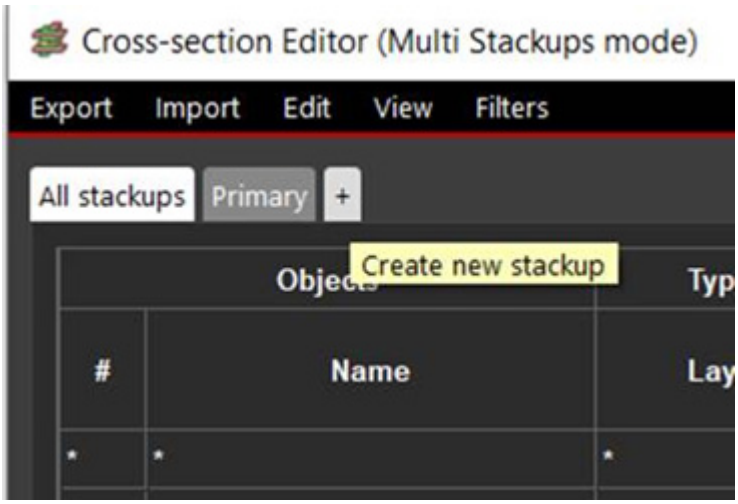


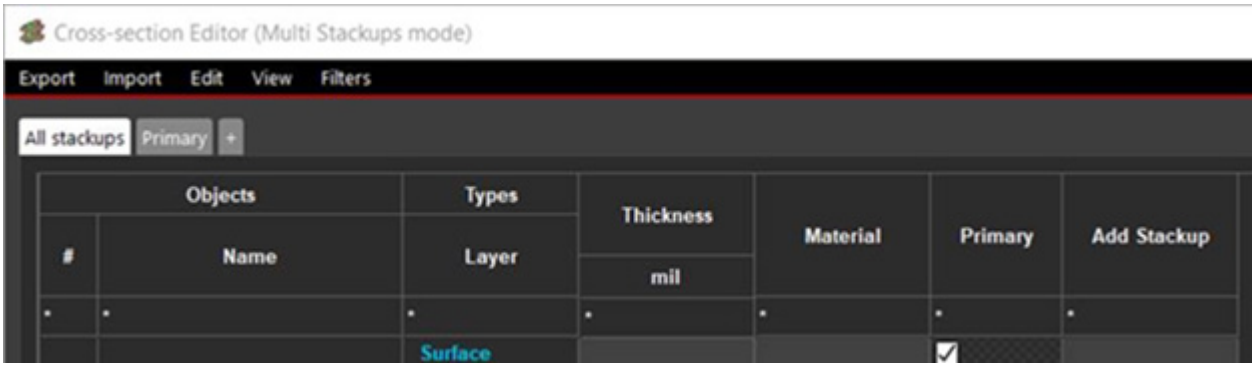
Objects		Types		Thickness	Physical		Embedded
#	Name	Layer	Layer Function	Value mil	Layer ID	Material	Embedded Status
		Surface					
	SOLDERMASK_TOP	Mask	Solder Mask	0.590551		Soldermask Fle...	
1	TOP	Conductor	Conductor	0.7	1	Half Oz Copper	Not embedded
		Dielectric	Dielectric	8		Fr-4	
2	LAYER_2	Conductor	Conductor	0.7	2	Half Oz Copper	Not embedded
		Dielectric	Dielectric	8		Fr-4	
		Dielectric	Dielectric Prepreg	2		Fr-4 No Flow Pr...	
3	LAYER_3	Conductor	Conductor	0.7	3	Half Oz Copper	Not embedded
		Dielectric	Dielectric Base	1		Polyimide Film...	
4	LAYER_4	Conductor	Conductor	0.7	4	Half Oz Copper	Not embedded
		Dielectric	Dielectric Prepreg	2		Polyimide	
		Dielectric	Dielectric	8		Fr-4	
5	LAYER_5	Conductor	Conductor	0.7	5	Half Oz Copper	Not embedded
		Dielectric	Dielectric	8		Fr-4	
6	BOTTOM	Conductor	Conductor	0.7	6	Half Oz Copper	Not embedded
	SOLDERMASK_BOTTOM	Mask	Solder Mask	0.590551		Soldermask Fle...	

To add the flex stackup to the design, perform the following steps:

1. Open the Create Stackup form:
2. Verify that the All stackups tab has been selected and select the *+* tab.

a. Click the Add Stackup Column header or choose the *Edit –Add Stackup*.



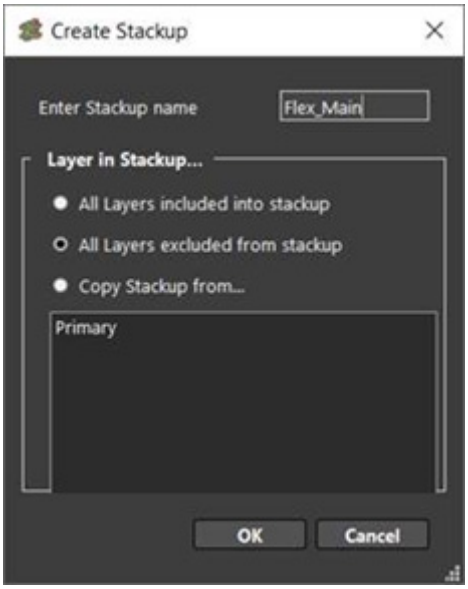


The Create Stackup form is opened.

3. Specify a name for the stackup.

A default name for the stackup is displayed, but this name is not very descriptive. The name should be simple, yet descriptive of the stackup. In this example, “Flex_Main”

indicates that the structure is for the flex portion of the design, and this is the common structure for any flexible areas in the design.

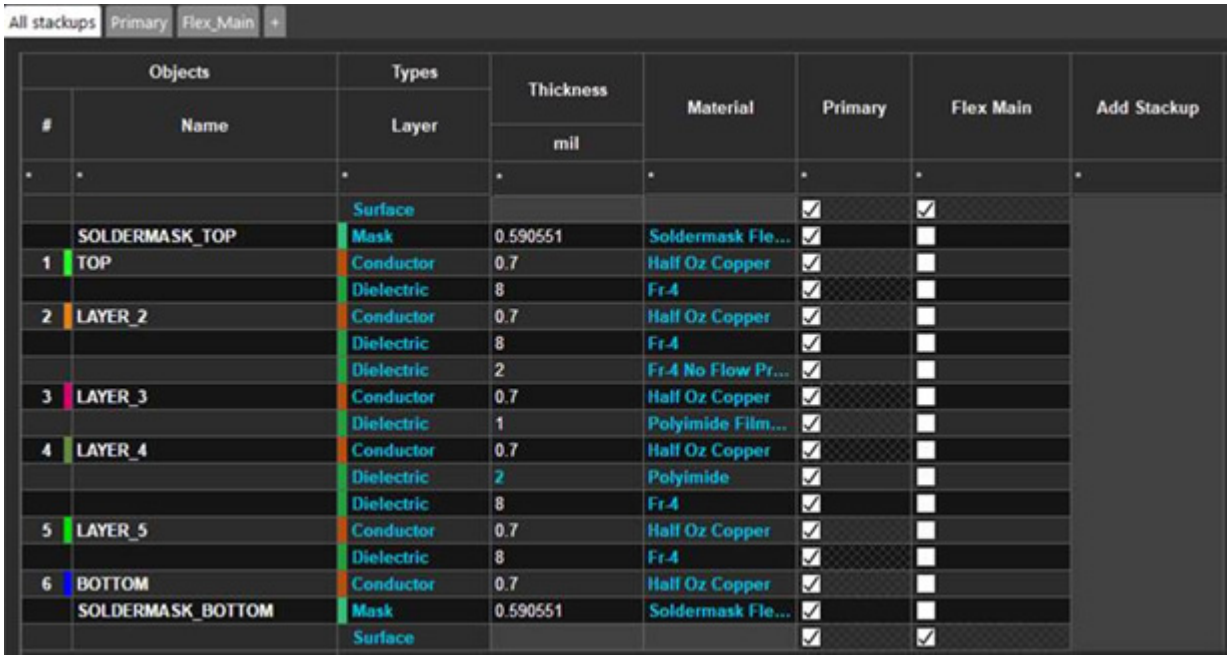


4. Select the layers in the stackup.

   The layers that currently exist in the stackup can be assigned by default, or excluded by default by selecting one of the three options in the Create stackup form. The same structure of another stackup may be copied, and then modified after creation to meet the new definition requirements. For this step, the exclude layers option is selected.

5. Click *OK*.

A new tab and column are added to the All stackups tab with the new stackup name. Only the Surface layer (TOP and BOTTOM) checkboxes are set in the new column.

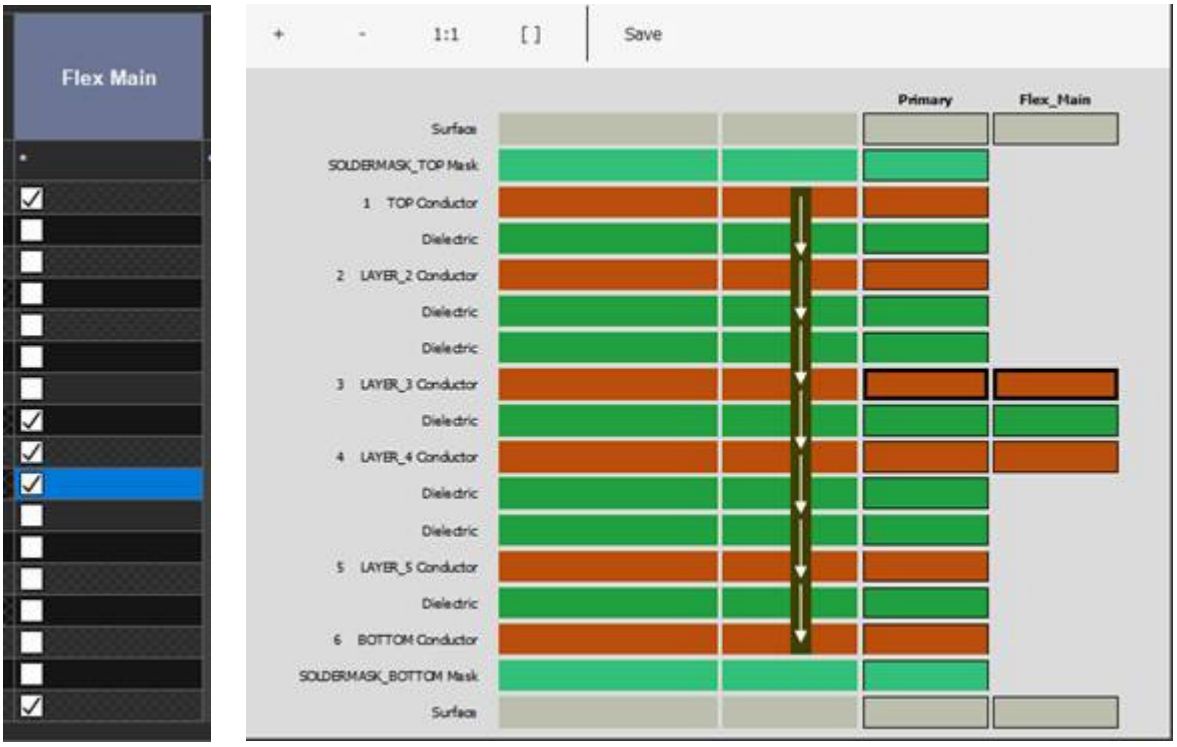


All stackups | Primary | Flex_Main | +

Objects		Types	Thickness	Material	Primary	Flex Main	Add Stackup
#	Name	Layer	mil				
		Surface			☑	☑	
	SOLDERMASK_TOP	Mask	0.590551	Soldermask Fle...	☑	☐	
1	TOP	Conductor	0.7	Half Oz Copper	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
2	LAYER_2	Conductor	0.7	Half Oz Copper	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
		Dielectric	2	Fr-4 No Flow Pr...	☑	☐	
3	LAYER_3	Conductor	0.7	Half Oz Copper	☑	☐	
		Dielectric	1	Polyimide Film...	☑	☐	
4	LAYER_4	Conductor	0.7	Half Oz Copper	☑	☐	
		Dielectric	2	Polyimide	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
5	LAYER_5	Conductor	0.7	Half Oz Copper	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
6	BOTTOM	Conductor	0.7	Half Oz Copper	☑	☐	
	SOLDERMASK_BOTTOM	Mask	0.590551	Soldermask Fle...	☑	☐	
		Surface			☑	☑	

6. To construct the stackup for the flex, set the checkboxes for each of the layers that are part of flex.

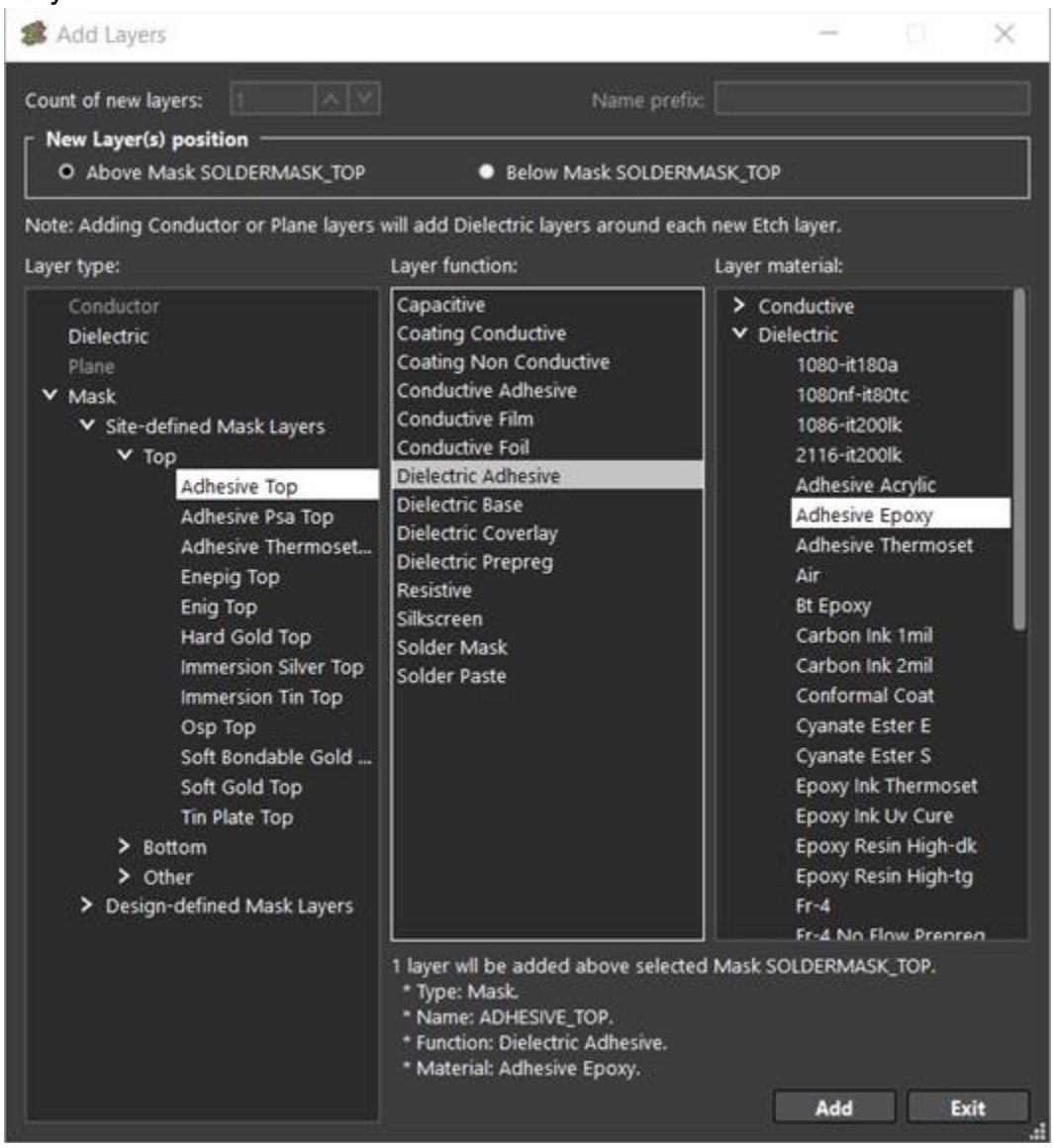
As each layer is selected, the cross section graphics image is updated.



Define the top and bottom Coverlay and Coverlay Adhesive layers in the stackup:

1. In Cross Section Editor, right-click a layer and choose *Add Layers* from the pop-up menu.
2. Add the Coverlay Top and Adhesive Top layers above the Soldermask Top layer.
3. Add Coverlay Bottom and Adhesive Bottom below the Soldermask Bottom layer.

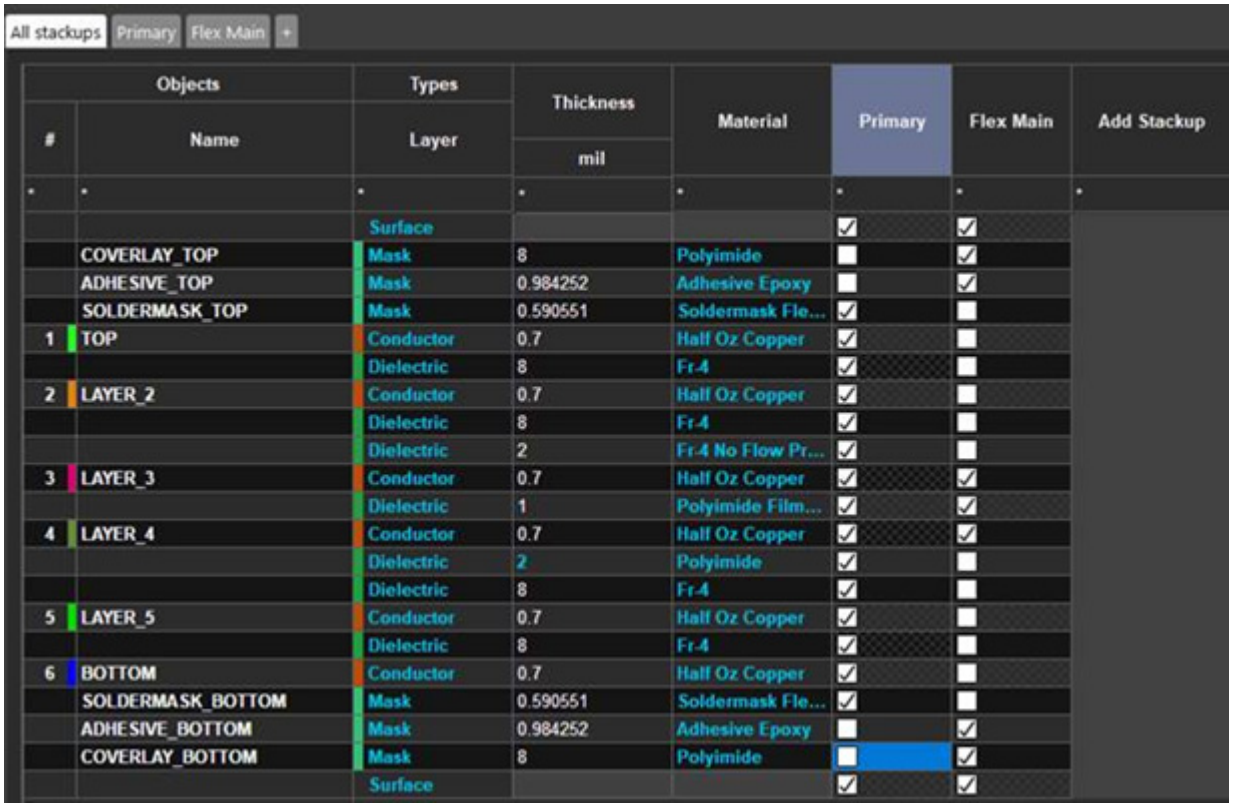
When assigning the adhesive layers, the layer definition was created in the Mask Layer Site File, so this material will also be selected in the Site-defined Mask Layer node in the Add Layers form.



After the layers are added, they are assigned to both the Primary and FLEX_MAIN stackup definitions:

4. For the Primary stackup, deselect the Coverlay and adhesive masks.

As they are deselected, the change is reflected in the cross section graphics image.



Objects		Types	Thickness	Material	Primary	Flex Main	Add Stackup
#	Name	Layer	mil				
		Surface			☑	☑	
	COVERLAY_TOP	Mask	8	Polyimide	☐	☑	
	ADHESIVE_TOP	Mask	0.984252	Adhesive Epoxy	☐	☑	
	SOLDERMASK_TOP	Mask	0.590551	Soldermask Fle...	☑	☐	
1	TOP	Conductor	0.7	Half Oz Copper	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
2	LAYER_2	Conductor	0.7	Half Oz Copper	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
		Dielectric	2	Fr-4 No Flow Pr...	☑	☐	
3	LAYER_3	Conductor	0.7	Half Oz Copper	☑	☑	
		Dielectric	1	Polyimide Film...	☑	☑	
4	LAYER_4	Conductor	0.7	Half Oz Copper	☑	☑	
		Dielectric	2	Polyimide	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
5	LAYER_5	Conductor	0.7	Half Oz Copper	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
6	BOTTOM	Conductor	0.7	Half Oz Copper	☑	☐	
	SOLDERMASK_BOTTOM	Mask	0.590551	Soldermask Fle...	☑	☐	
	ADHESIVE_BOTTOM	Mask	0.984252	Adhesive Epoxy	☐	☑	
	COVERLAY_BOTTOM	Mask	8	Polyimide	☐	☑	
		Surface			☑	☑	

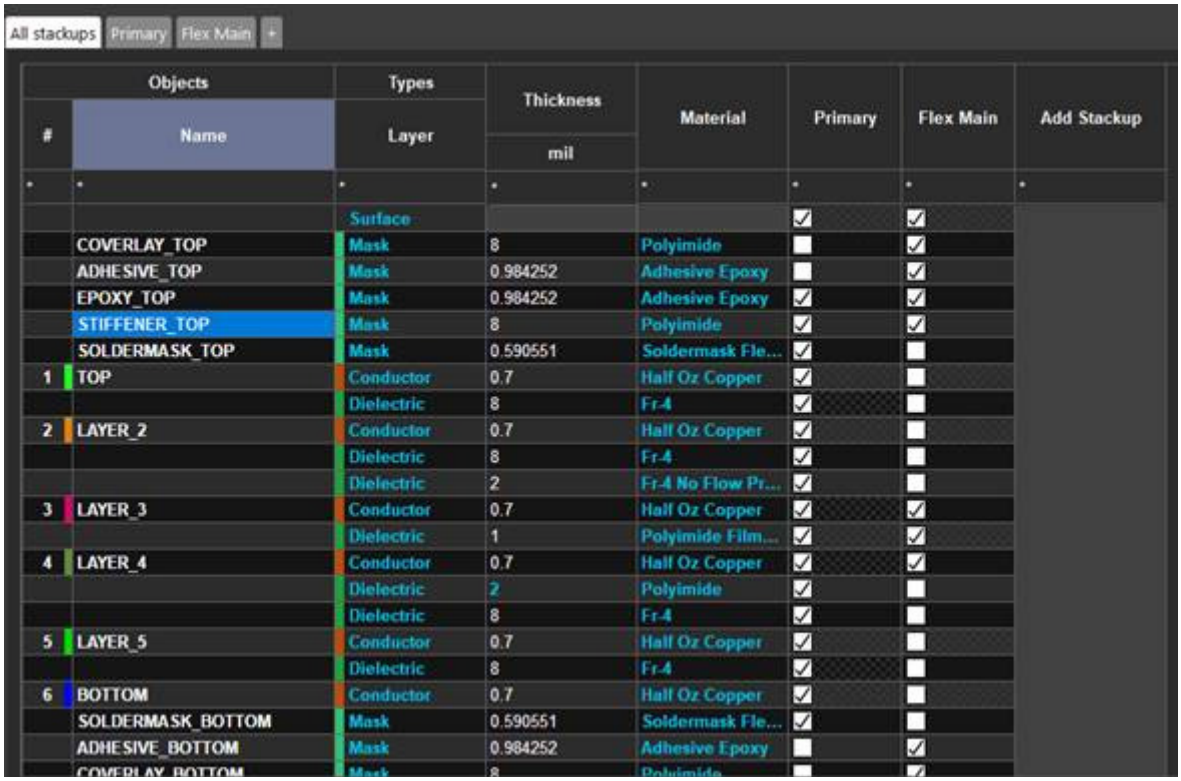
5. Click *Apply* in Cross Section Editor to implement the stackup data into the design.

   The remaining stackup definition is now created. This stackup has a STIFFENER_TOP with an EPOXY_TOP in place of COVERLAY_TOP and ADHESIVE_TOP. The order in which the structure is defined does not require creation of a stackup definition first followed by the addition of the layers.

The layer can be added first if that is more convenient:

1. Create the two new top layers using the Add Layers command above the TOP Conductor.
2. Use the Site-defined Mask layers EPOXY_TOP and STIFFENER_TOP.

3. Remove these selections from the Primary and FLEX_MAIN.



#	Objects: Name	Types: Layer	Thickness: mil	Material	Primary	Flex Main	Add Stackup
		Surface			☑	☑	
	COVERLAY_TOP	Mask	8	Polyimide	☐	☑	
	ADHESIVE_TOP	Mask	0.984252	Adhesive Epoxy	☐	☑	
	EPOXY_TOP	Mask	0.984252	Adhesive Epoxy	☑	☑	
	STIFFENER_TOP	Mask	8	Polyimide	☑	☑	
	SOLDERMASK_TOP	Mask	0.590551	Soldermask Fle...	☑	☐	
1	TOP	Conductor	0.7	Half Oz Copper	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
2	LAYER_2	Conductor	0.7	Half Oz Copper	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
		Dielectric	2	Fr-4 No Flow Pr...	☑	☐	
3	LAYER_3	Conductor	0.7	Half Oz Copper	☑	☑	
		Dielectric	1	Polyimide Film...	☑	☑	
4	LAYER_4	Conductor	0.7	Half Oz Copper	☑	☑	
		Dielectric	2	Polyimide	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
5	LAYER_5	Conductor	0.7	Half Oz Copper	☑	☐	
		Dielectric	8	Fr-4	☑	☐	
6	BOTTOM	Conductor	0.7	Half Oz Copper	☑	☐	
	SOLDERMASK_BOTTOM	Mask	0.590551	Soldermask Fle...	☑	☐	
	ADHESIVE_BOTTOM	Mask	0.984252	Adhesive Epoxy	☐	☑	
	COVERLAY_BOTTOM	Mask	8	Polyimide	☐	☑	

Note: When defining the stackup, correct order of the layers is important. The structure that is being defined in Cross Section Editor is used for documentation sent to the fabricator. The Cross Section chart relies on the information defined in the cross section definition and should be as accurate as possible. Signal integrity (SI) tools also rely on proper structure to provide more realistic analysis based on the materials, and the position of those materials in the stackup.

4. Add a new stackup named FLEX_STIFFENER.

5. Use Copy Stackup and select FLEX_MAIN.

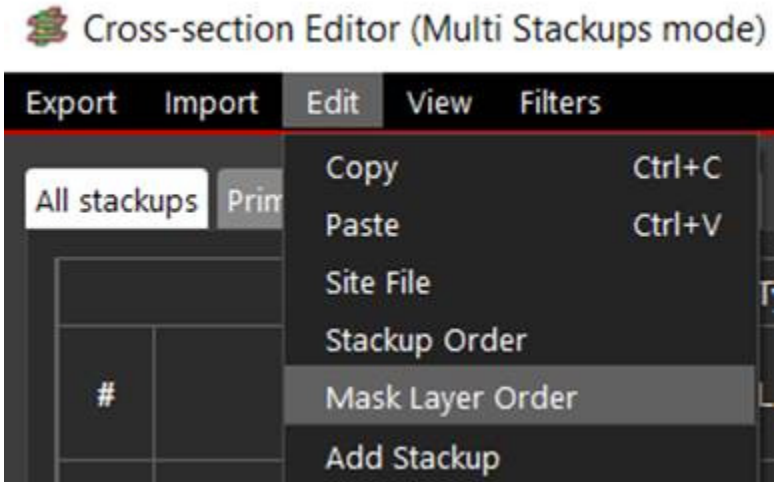
   A copy of this stackup will require less work to build the definition of the stackup.

6. Deselect the checkboxes for COVERLAY_TOP and ADHESIVE_TOP in the Flex Stiffener column.

7. Add the STIFFENER_TOP and EPOXY_TOP to the FLEX_STIFFENER stackup definition, by selecting the check boxes in the Flex Stiffener column.

   On review of the stackup, the EPOXY_TOP and STIFFENER_TOP are not found to be in the correct order. The order of these two stackups needs to be swapped.

8. In Cross Section Editor, choose *Edit – Mask Layer Order*.

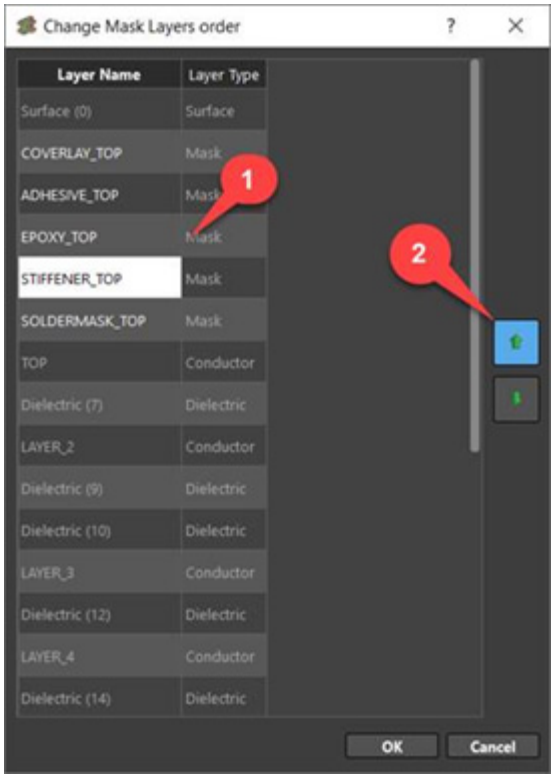


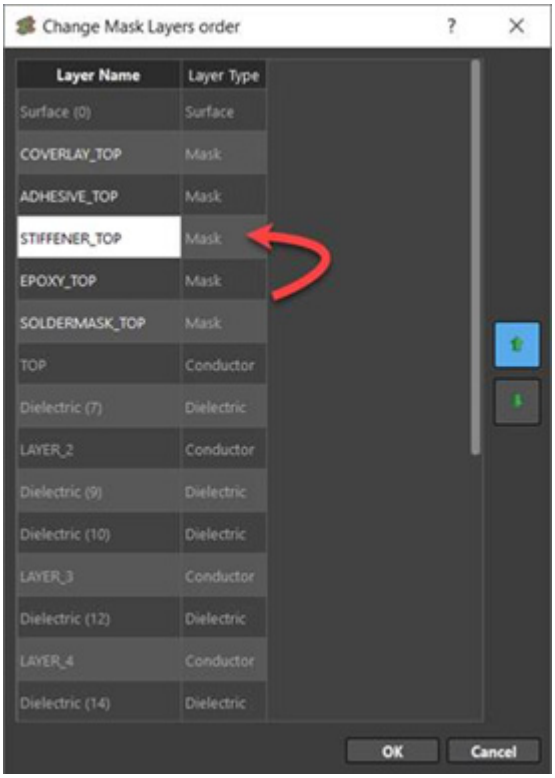
In the resultant dialog, the mask layers can be repositioned in the stackup.

9. Select the STIFFENER_TOP layer.

10. Click the Up arrow and move the STIFFENER_TOP layer above the EPOXY_TOP layer placing the layers in the correct order.

11. Click *OK*.





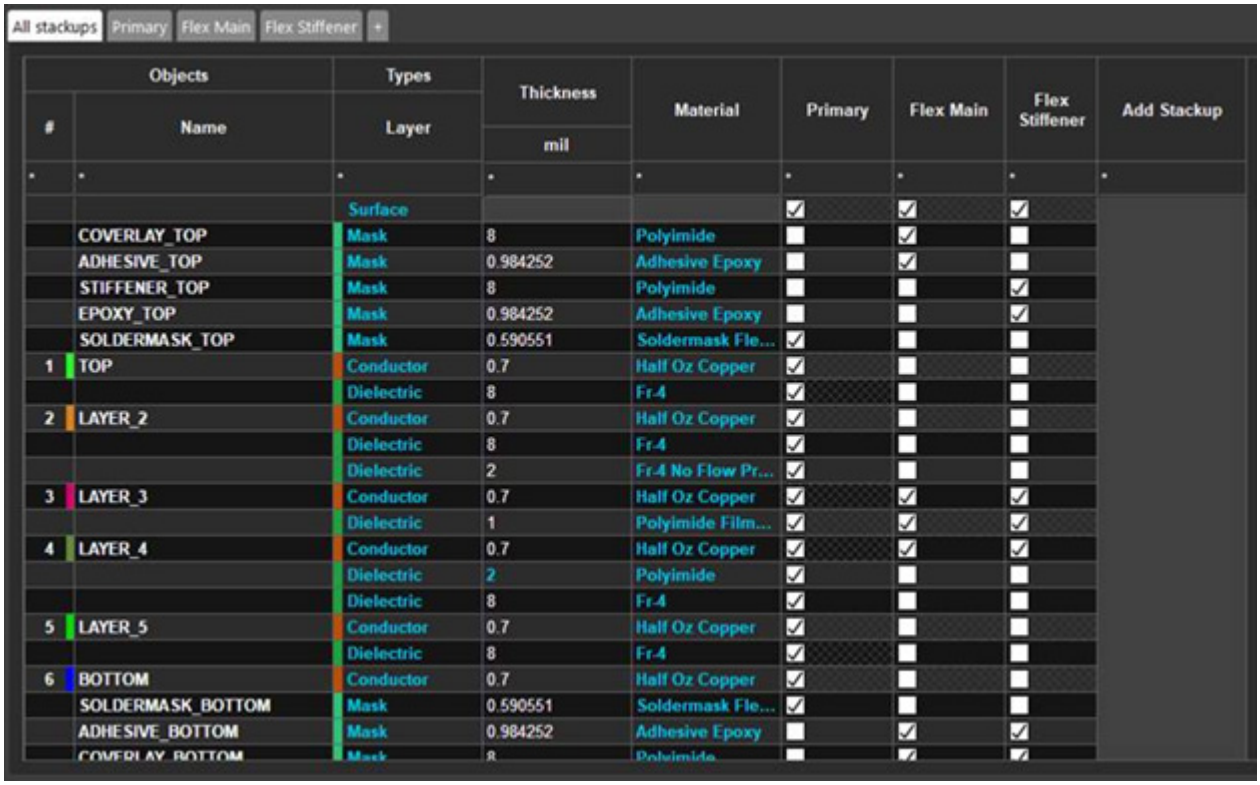
The change in the stackup is displayed in Cross Section Editor. The construction of the multiple stackups is complete.

12. Click *Apply* to implement the cross section definition into the drawing database.

13. Explore each Cross Section tab to verify that each structure is complete.

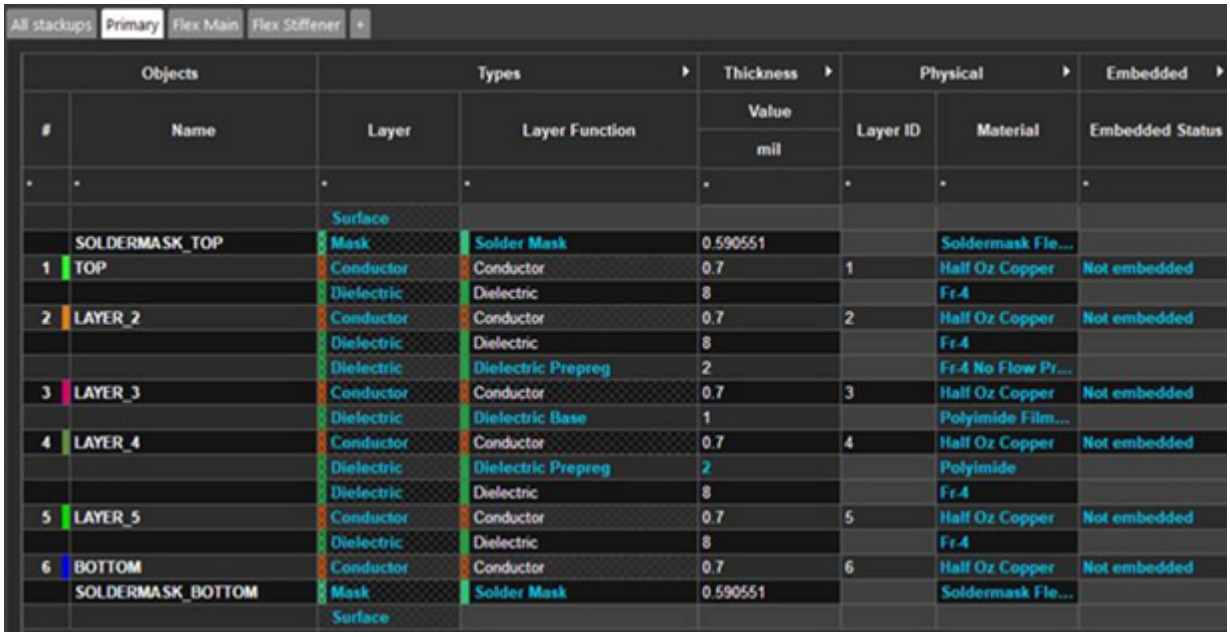
14. Make any changes or updates as required.

All of the Stackups are defined:



Objects		Types	Thickness	Material	Primary	Flex Main	Flex Stiffener	Add Stackup
#	Name	Layer	mil					
		Surface			☑	☑	☑	
	COVERLAY_TOP	Mask	8	Polyimide	☐	☑	☐	
	ADHESIVE_TOP	Mask	0.984252	Adhesive Epoxy	☐	☑	☐	
	STIFFENER_TOP	Mask	8	Polyimide	☐	☐	☑	
	EPOXY_TOP	Mask	0.984252	Adhesive Epoxy	☐	☐	☑	
	SOLDERMASK_TOP	Mask	0.590551	Soldermask Fle...	☑	☐	☐	
1	TOP	Conductor	0.7	Half Oz Copper	☑	☐	☐	
		Dielectric	8	Fr-4	☑	☐	☐	
2	LAYER_2	Conductor	0.7	Half Oz Copper	☑	☐	☐	
		Dielectric	8	Fr-4	☑	☐	☐	
		Dielectric	2	Fr-4 No Flow Pr...	☑	☐	☐	
3	LAYER_3	Conductor	0.7	Half Oz Copper	☑	☑	☑	
		Dielectric	1	Polyimide Film...	☑	☑	☑	
4	LAYER_4	Conductor	0.7	Half Oz Copper	☑	☑	☑	
		Dielectric	2	Polyimide	☑	☐	☐	
		Dielectric	8	Fr-4	☑	☐	☐	
5	LAYER_5	Conductor	0.7	Half Oz Copper	☑	☐	☐	
		Dielectric	8	Fr-4	☑	☐	☐	
6	BOTTOM	Conductor	0.7	Half Oz Copper	☑	☐	☐	
	SOLDERMASK_BOTTOM	Mask	0.590551	Soldermask Fle...	☑	☐	☐	
	ADHESIVE_BOTTOM	Mask	0.984252	Adhesive Epoxy	☐	☑	☑	
	COVERLAY_BOTTOM	Mask	8	Polyimide	☐	☑	☑	

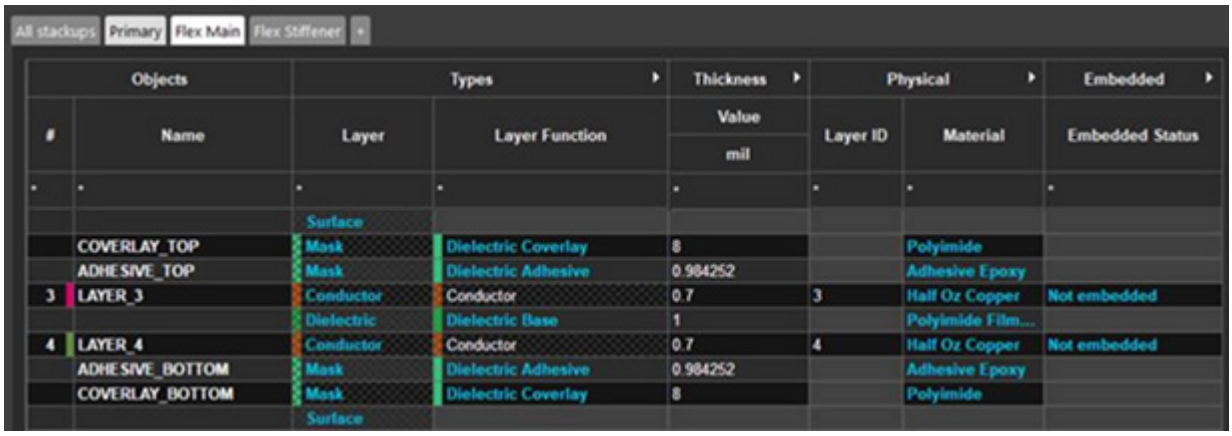
Primary Stackup:



All stackups | Primary | Flex Main | Flex Stiffener | +

Objects		Types		Thickness	Physical		Embedded
#	Name	Layer	Layer Function	Value (mil)	Layer ID	Material	Embedded Status
		Surface					
	SOLDERMASK_TOP	Mask	Solder Mask	0.590551		Soldermask Fle...	
1	TOP	Conductor	Conductor	0.7	1	Half Oz Copper	Not embedded
		Dielectric	Dielectric	8		Fr-4	
2	LAYER_2	Conductor	Conductor	0.7	2	Half Oz Copper	Not embedded
		Dielectric	Dielectric	8		Fr-4	
		Dielectric	Dielectric Prepreg	2		Fr-4 No Flow Pr...	
3	LAYER_3	Conductor	Conductor	0.7	3	Half Oz Copper	Not embedded
		Dielectric	Dielectric Base	1		Polyimide Film...	
4	LAYER_4	Conductor	Conductor	0.7	4	Half Oz Copper	Not embedded
		Dielectric	Dielectric Prepreg	2		Polyimide	
		Dielectric	Dielectric	8		Fr-4	
5	LAYER_5	Conductor	Conductor	0.7	5	Half Oz Copper	Not embedded
		Dielectric	Dielectric	8		Fr-4	
6	BOTTOM	Conductor	Conductor	0.7	6	Half Oz Copper	Not embedded
	SOLDERMASK_BOTTOM	Mask	Solder Mask	0.590551		Soldermask Fle...	
		Surface					

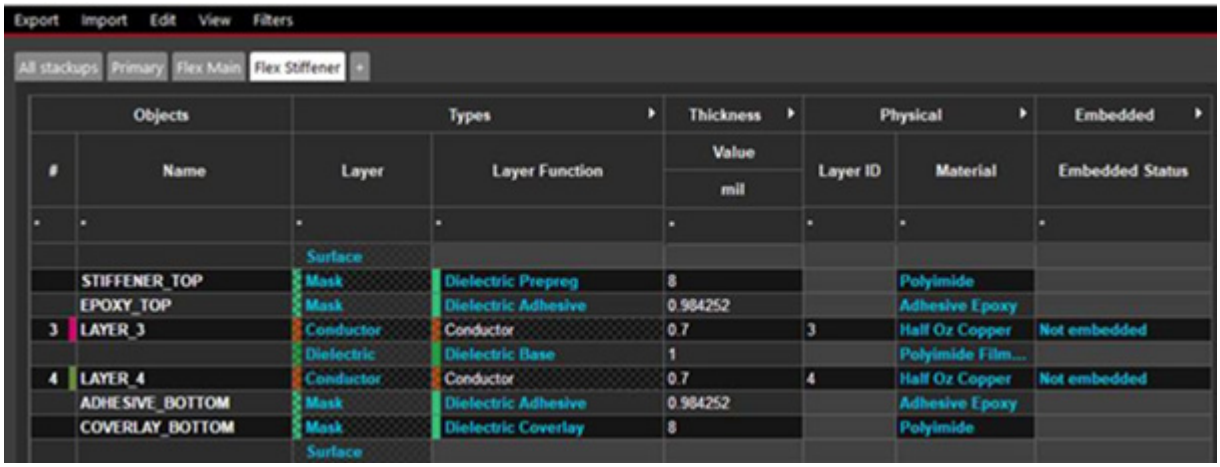
Flex Main Stackup:



All stackups | Primary | Flex Main | Flex Stiffener | +

Objects		Types		Thickness	Physical		Embedded
#	Name	Layer	Layer Function	Value (mil)	Layer ID	Material	Embedded Status
		Surface					
	COVERLAY_TOP	Mask	Dielectric Coverlay	8		Polyimide	
	ADHESIVE_TOP	Mask	Dielectric Adhesive	0.984252		Adhesive Epoxy	
3	LAYER_3	Conductor	Conductor	0.7	3	Half Oz Copper	Not embedded
		Dielectric	Dielectric Base	1		Polyimide Film...	
4	LAYER_4	Conductor	Conductor	0.7	4	Half Oz Copper	Not embedded
	ADHESIVE_BOTTOM	Mask	Dielectric Adhesive	0.984252		Adhesive Epoxy	
	COVERLAY_BOTTOM	Mask	Dielectric Coverlay	8		Polyimide	
		Surface					

Flex Stiffener Stackup:



Objects		Types		Thickness	Physical		Embedded
#	Name	Layer	Layer Function	Value mil	Layer ID	Material	Embedded Status
		Surface					
	STIFFENER_TOP	Mask	Dielectric Prepreg	8		Polyimide	
	EPOXY_TOP	Mask	Dielectric Adhesive	0.984252		Adhesive Epoxy	
3	LAYER_3	Conductor	Conductor	0.7	3	Half Oz Copper	Not embedded
		Dielectric	Dielectric Base	1		Polyimide Film...	
4	LAYER_4	Conductor	Conductor	0.7	4	Half Oz Copper	Not embedded
	ADHESIVE_BOTTOM	Mask	Dielectric Adhesive	0.984252		Adhesive Epoxy	
	COVERLAY_BOTTOM	Mask	Dielectric Coverlay	8		Polyimide	
		Surface					

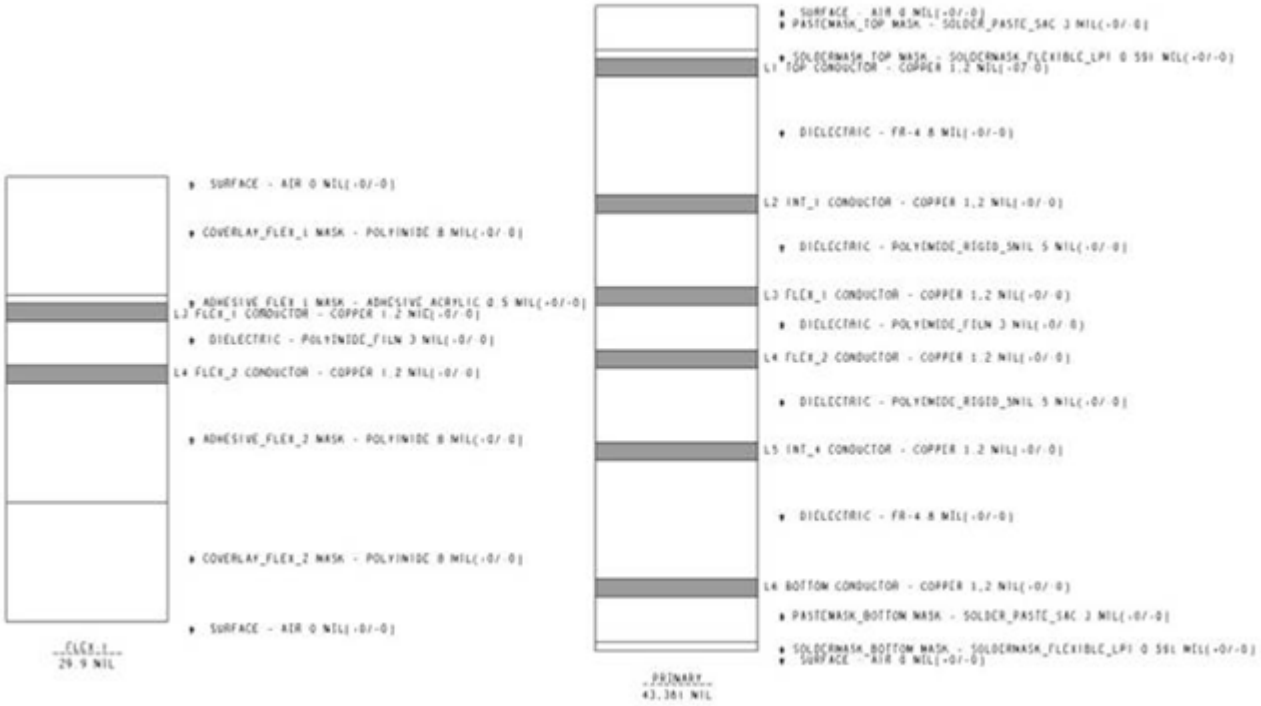
Stackup Details for Documentation

Relaying stackup structure to the manufacturer is an important part of defining the physical aspects of a design. Manufacturers need to know the material required for each of the different zones in the design. As standards such as IPC-2581 that are beginning to output this information, the zone dimensions and linked stackups are exchanged electronically. Until these standards are fully adopted, documentation is the method for relaying the stackup construction.

Document should have a detailed diagram of the various zones with zone identification labels and dimension for the zone profile. This gives the fabricator the information on the tool-related processes to build up a rigid-flex design. Details of the stackup data clearly referencing the zone(s) that they are assigned to should also be a part of the documentation. The Cross Section Chart provides two methodologies for representing the stackup structure and the stackup to zone reference, the Chart and the Table.

The Chart process creates a graphical representation of each of the stackup definitions in the design. Graphical chart is a group of geometries placed into a fabrication drawing. The chart

describes the stackup structure as defined in Cross Section Editor, a note for each graphical image listed may need to be added to identify the zones with which each chart is associated.



The Table process displays a spreadsheet into the drawing database that is a close representation of the Cross Section Editor form. The materials, thicknesses, tolerances, and other attributes are listed. Most importantly, the zones that are associated with the stackup are listed in the table.

MULTIPLE STACKUP TABLE
Unit - mils

#	NAME	TYPE	MATERIAL	TOLERANCE	RIGID_2	FLEX_3	PRIMARY	FLEX-STIFFENER	FLEX_1	FLEX_2
		SURFACE	AIR	-0/-0	0.000	0.000	0.000	0.000	0.000	0.000
	STIFFENER_TOP	MASK	STAINLESS STEEL	-0/-0		0.000		0.000		
	EPOXY_TOP	MASK	ADHESIVE EPOXY	-0/-0		0.984		0.984		
	COVERLAY_FLEX_1	MASK	POLYIMIDE	-0/-0		8.000		8.000	8.000	8.000
	ADHESIVE_FLEX_1	MASK	ADHESIVE ACRYLIC	-0/-0		0.500		0.500	0.500	0.500
	PASTEMASK_FLEX_1	MASK	SOLDER PASTE SAC	-0/-0						3.000
	GOLD_SOFT_FLEX_1	MASK	POLYIMIDE	-0/-0						8.000
	PASTEMASK_TOP	MASK	SOLDER PASTE SAC	-0/-0			3.000			
	SOLDERMASK_TOP	MASK	SOLDERMASK FLEXIBLE LPI	-0/-0			0.591			
	SOLDERMASK_INT1	MASK	SOLDERMASK FLEXIBLE LPI	-0/-0	0.591					
	PASTEMASK_INT1	MASK	SOLDER PASTE SAC	-0/-0	3.000					
1	TOP	CONDUCTOR	COPPER	-0/-0			1.200			
		DIELECTRIC	FR-4	-0/-0			8.000			
2	INT_1	CONDUCTOR	COPPER	-0/-0	1.200		1.200			
		DIELECTRIC	POLYIMIDE RIGID 5MIL	-0/-0	5.000		5.000			
3	FLEX_1	CONDUCTOR	COPPER	-0/-0	1.200	1.200	1.200	1.200	1.200	1.200
		DIELECTRIC	POLYIMIDE FILM	-0/-0	3.000	3.000	3.000	3.000	3.000	3.000
4	FLEX_2	CONDUCTOR	COPPER	-0/-0	1.200	1.200	1.200	1.200	1.200	1.200
		DIELECTRIC	POLYIMIDE RIGID 5MIL	-0/-0	5.000		5.000			
5	INT_4	CONDUCTOR	COPPER	-0/-0	1.200		1.200			
		DIELECTRIC	FR-4	-0/-0			8.000			
6	BOTTOM	CONDUCTOR	COPPER	-0/-0			1.200			
	PASTEMASK_BOTTOM	MASK	SOLDER PASTE SAC	-0/-0			3.000			
	SOLDERMASK_BOTTOM	MASK	SOLDERMASK FLEXIBLE LPI	-0/-0			0.591			
	PASTEMASK_INT4	MASK	ADHESIVE ACRYLIC	-0/-0	0.500					
	SOLDERMASK_INT4	MASK	POLYIMIDE	-0/-0	8.000					
	GOLD_HARD_FLEX_2	MASK	POLYIMIDE	-0/-0		8.000		8.000		
	ADHESIVE_FLEX_2	MASK	POLYIMIDE	-0/-0		8.000		8.000	8.000	8.000
	COVERLAY_FLEX_2	MASK	POLYIMIDE	-0/-0		8.000		8.000	8.000	8.000
		SURFACE	AIR	-0/-0	0.000	0.000	0.000	0.000	0.000	0.000
			TOTAL THICKNESS		29.891	38.884	43.381	38.884	29.900	40.900
			ZONE NAME		RIGID_ZONE_1 RIGID_ZONE_2	FLEX_ZONE_3 CONECTOR_ZONE FLEX_ZONE_5		FLEX_ZONE_6	FLEX_ZONE_1	FLEX_ZONE_2

Creating Multi-Stackup Zones in the Design Drawing

Positioning of different stackups for a rigid-flex design is accomplished by defining Stackup Zones. Create the boundary (a shape) of the Zone, then assign a stackup definition previously created in Cross Section Editor to the zone. Zones are not required for every stackup definition in the design. Any area within the DESIGN_OUTLINE that does not have a zone is defaulted to the Primary Stackup.

When creating stackup zones in the design, each stackup zone requires a unique name and must be assigned a stackup definition. Options for a constraint set and Room name are available. If you select either of these two options, a constraint region or room geometry is created for the optional object. The optional geometries are copies of the zone boundary and are grouped with the zone so that when any boundary changes are made to a zone, the associated constraint region and room are also updated. If the zone is deleted, so are the constraint region and the room.

Important

There are specific rules and processes that must be followed to correctly define zones.

- The DESIGN_OUTLINE is used for the outer extents of the design. Zone trimming will only apply to the DESIGN_OUTLINE or another ZONE boundary.
- Zones cannot be overlapped or nested. If a zone is added and intersects/overlaps with an existing zone, the newer zone will be trimmed to the existing zone boundary.
- When a zone is first defined with pre-existing symbols, traces, vias, or conductor shapes within the boundary, the stackup assignment for that zone may fail. The symbols, traces, vias, conductor shapes must be moved out of the area where the zone will be defined, and the stackup reassigned. After that the moved or deleted objects can be replaced. Traces and shape placement within a zone will fail if the layer they are defined on no longer exists.
- If any symbols, traces, vias, and/or conductor shapes are placed on the design within a zone, and the zone stackup assignment is altered, the modification will fail. The symbols, traces, vias, conductor shapes must be moved out of that zone prior to the new stackup assignment. After the modifications are complete, the objects can be replaced. Traces and shape placement within a zone will fail if the layer they are defined on no longer exists.

Creating a Zone

A zone is created using the Zone Creation tool in the PCB Editor. To create a zone, perform the following steps:

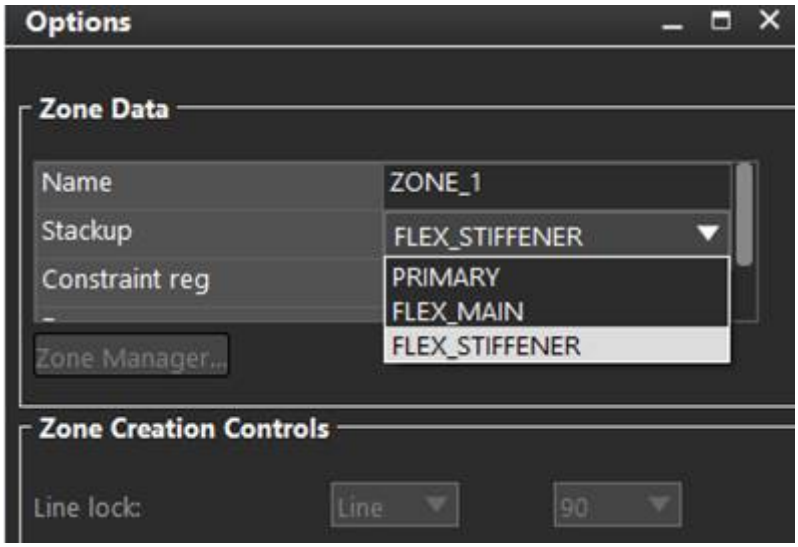
1. In PCB Editor, choose *Setup – Zones – Create*.

   The Options Tab displays the parameters for the Zone definition.

2. Specify the zone name and the stackup definition to be assigned to that zone.

   Default zone name, such as ZONE_1, ZONE_2, and so on appear in the Name field under Zone Data.

3. Assign other attributes such as a constraint set and room.



   The boundary is defined in the PCB Editor canvas.

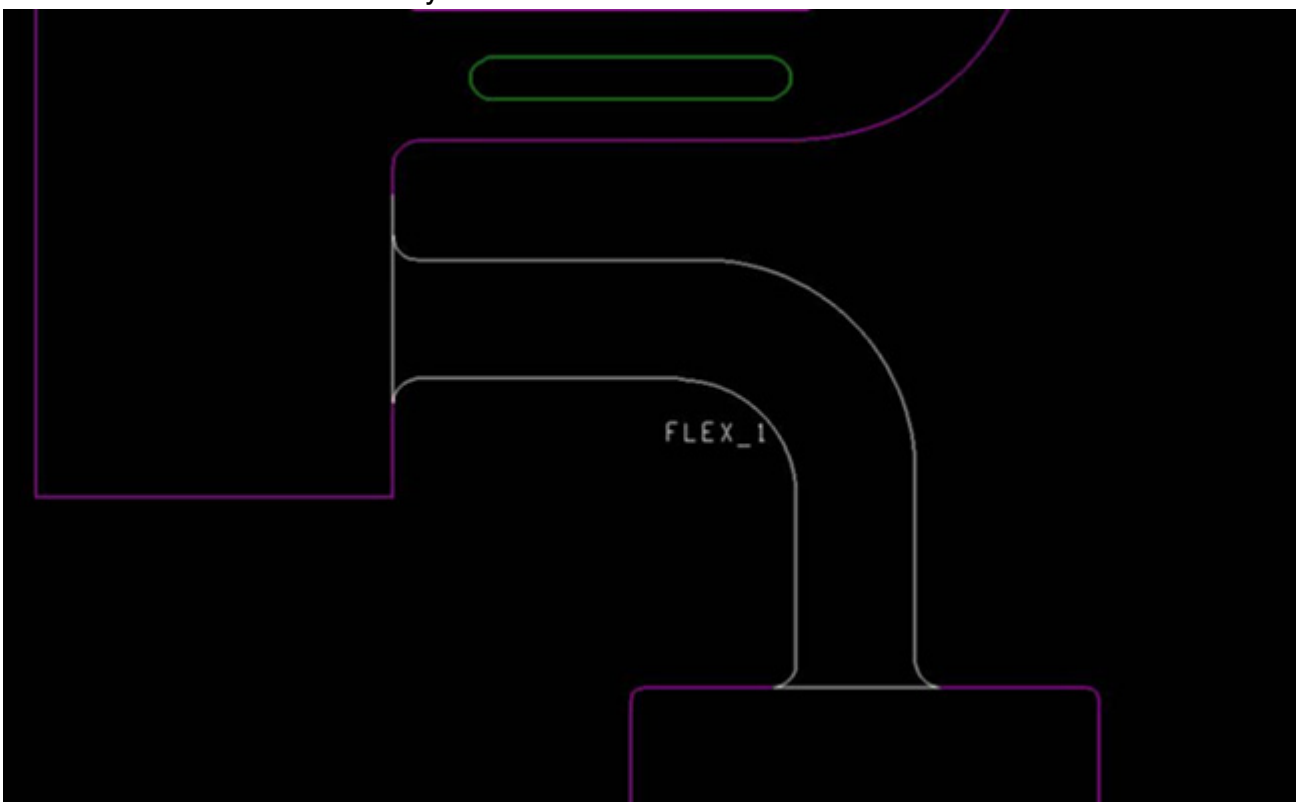
There are two methods to create a zone boundary: by using the Add Rectangle command or using the Add Shape command. The default process is by adding a rectangle.

Adding a Rectangle

1. Right-click the canvas and choose *Add Rectangle*.

2. Use the Snap pick to right mouse button pick to select an edge to align to a segment of the DESIGN_OUTLINE as illustrated in the following figure:

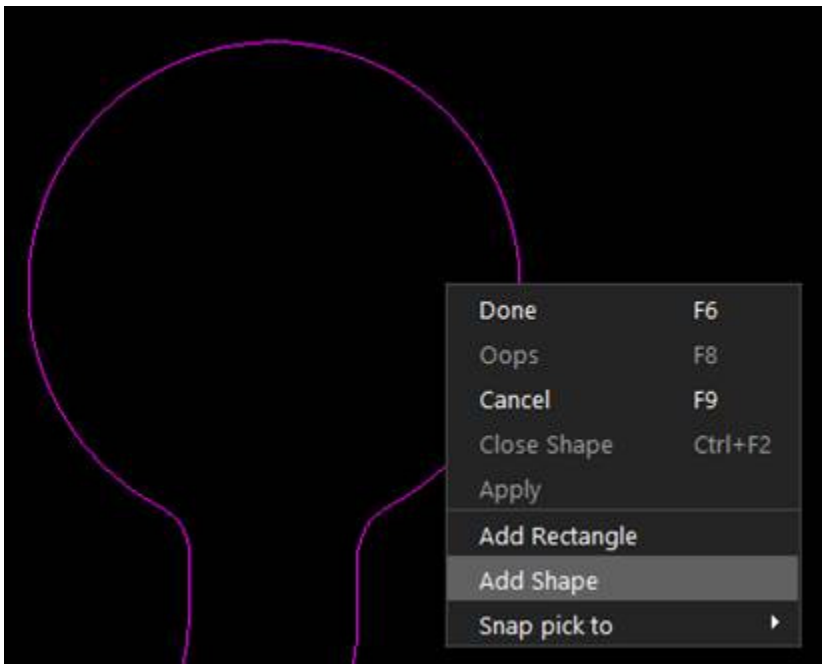
In this example, the second pick extends into a previously-defined zone. After the second pick is completed, the zone boundary is trimmed to DESIGN_OUTLINE and any other intersected zone boundary.



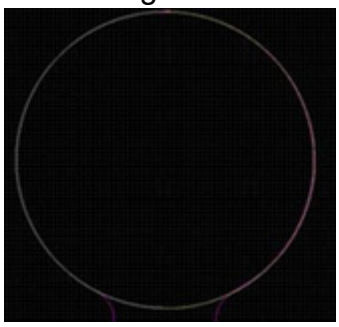
Adding a Shape

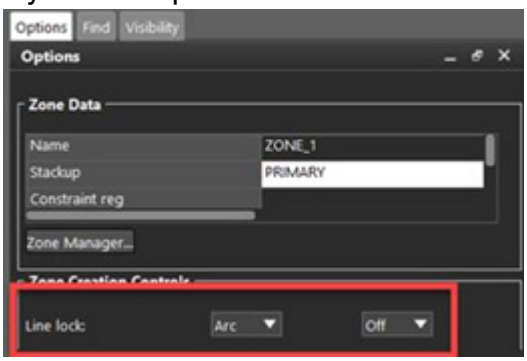
A zone boundary can also be added using the *Add Shape* command. This is best used for complex shape outlines where boundaries must be carefully controlled.

1. Right-click the canvas and choose *Add Shape*.



2. Use the Zone Creation Controls in the Options tab to select Line or Arc mode when adding the zone boundary as a shape.





Editing a Zone

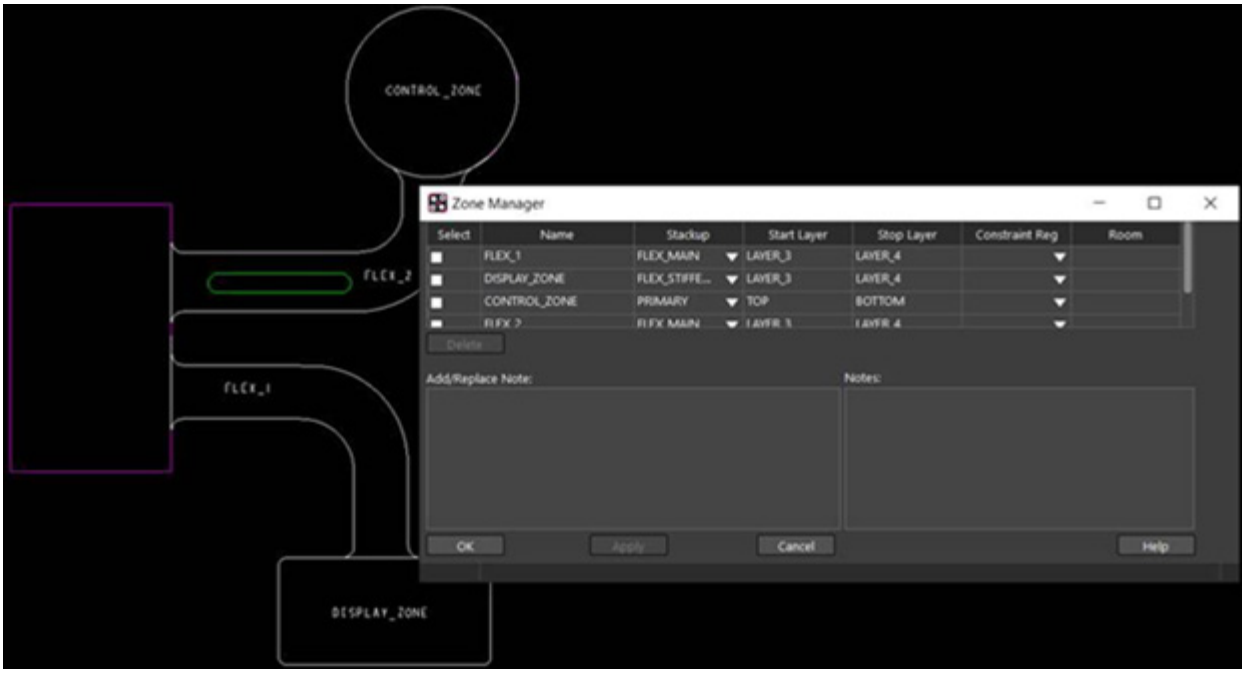
After a zone is created, the parameters can be edited within the Zone Manager form.

To edit a zone:

1. Choose *Setup – Zones – Manage*.

   The Zone Manager form displays the zone names, the current stackup assignment, constraint set name, and room name. Any of these fields may be modified and applied through this form. The Zone Manager also displays the Start Layer, or the topmost conductor layer name and the Stop Layer, or the bottommost conductor layer name

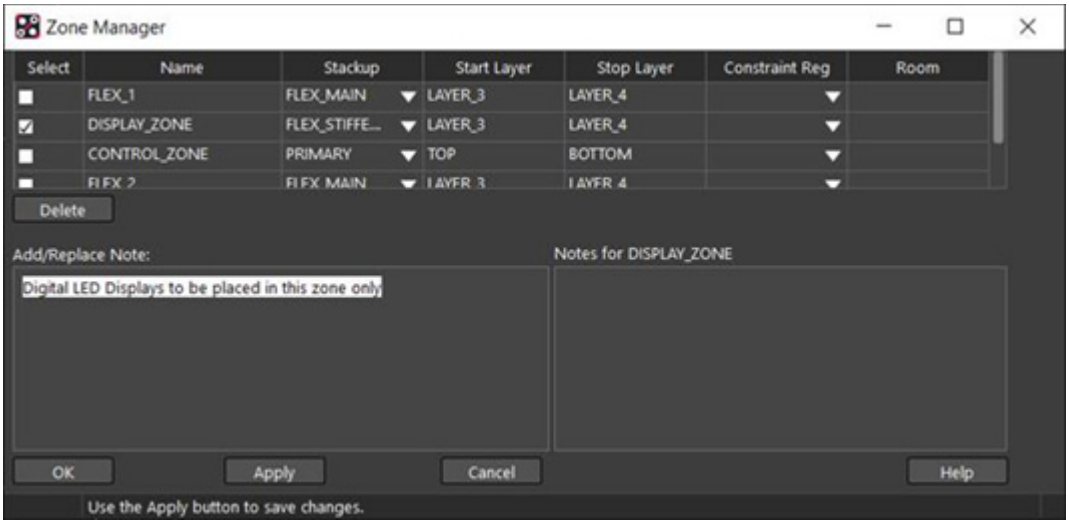
defined in that zone based on the stackup assignment. These layer names are informational and only modified by changing the stackup definition for that zone.

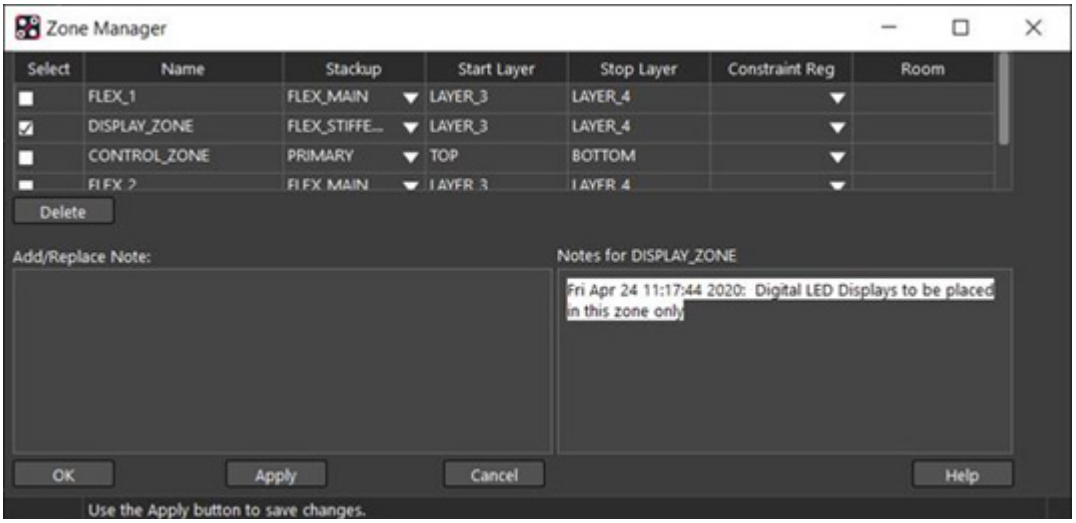


Notes may be added to zones using the *Add/Replace Note* field in the form.

2. Select the check box next to a zone and specify a note to be associated with the zone.

3. Click *Apply* to associate the note with the zone.





Zones may only be deleted through the Zone Manager.

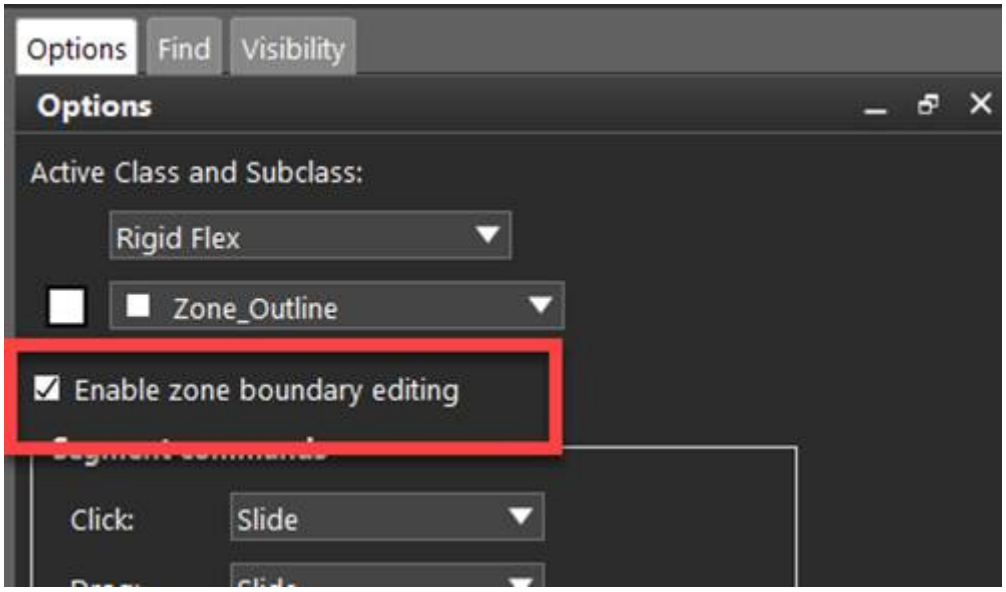
To delete a zone:

1. Select the checkbox next to the Zone name.
2. Click *Delete*.

   The zone is removed from the database.

   If a zone boundary needs to be modified, the Shape Edit application mode is preferred. While in the Shape Edit application mode, the option Enable zone boundary editing in

the Options Tab must also be selected. If this option is not selected, the zone boundaries cannot be modified.

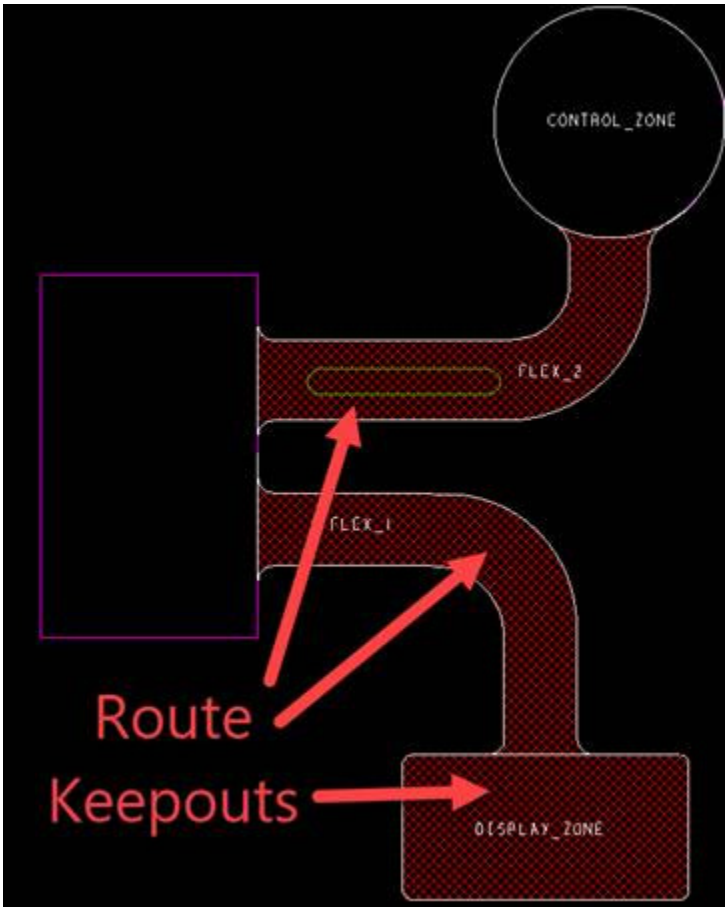


Special Zone Characteristics

Enabling zone boundary editing

Stackup zones provide the boundary and stackup information for a particular region of a design. They also provide the awareness of non-existent layers for those particular regions. As a zone is created in the database, route keepouts are added to prevent traces from being added into a zone where no conductor layer exists. Zones also become placement aware so

that when an SMD Package is placed in a zone, the pads are pushed to the outermost conductor layer.

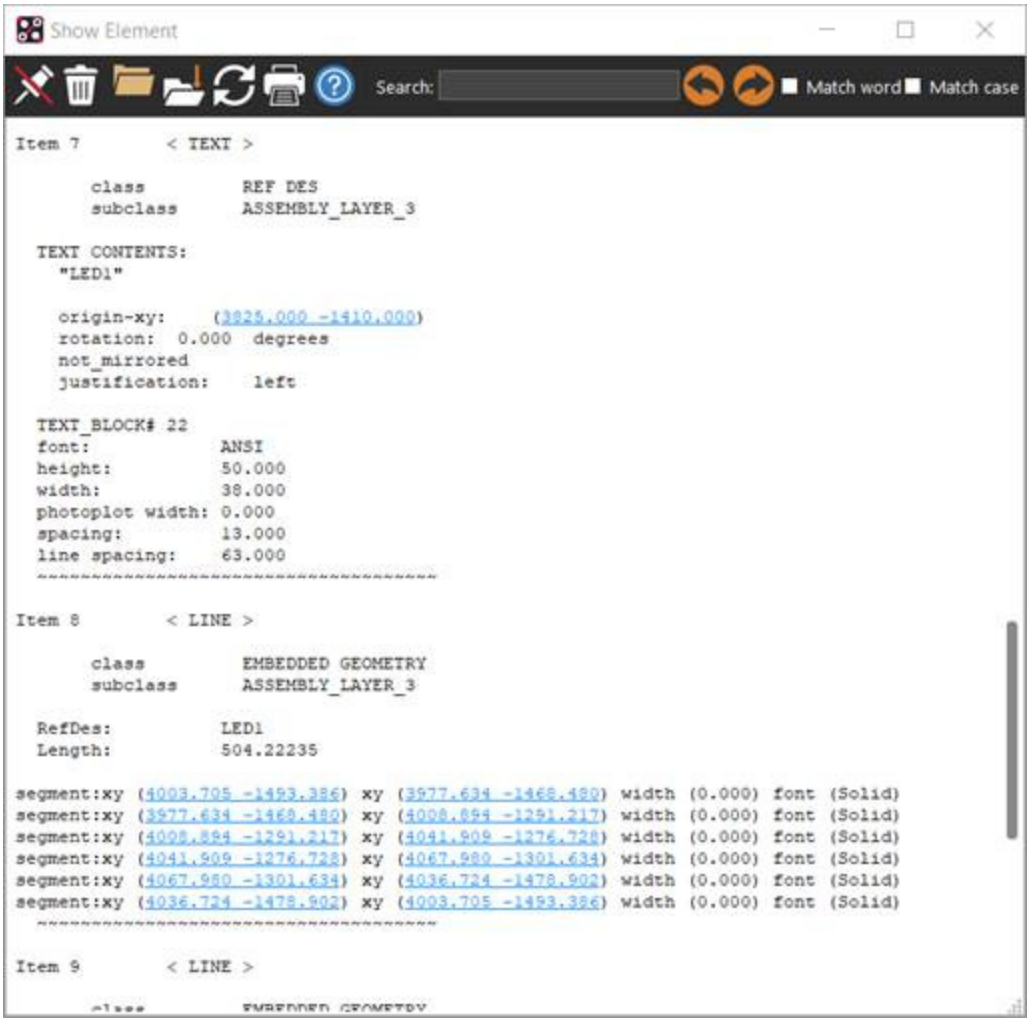


When placing a component into a zone, the component padstack and geometry adjust for that zone. Without requiring the user to set up the design for embedded geometry or creating special alternate footprints, the tool leverages the embedded capability to place packages on legal conductor layers. The pastemask and soldermask layer for the padstack are adjusted as well. The symbol Geometry is also adjusted to accommodate the move from the TOP and BOTTOM layer geometries.

In the following example, an LED Display (LED1)is placed on the top side of a stackup zone where Layer_3 is the top outermost layer. The details in the Show Element window indicate

that the component is placed on layer LAYER_3. The Show Element display also identified the zone the component is placed in.

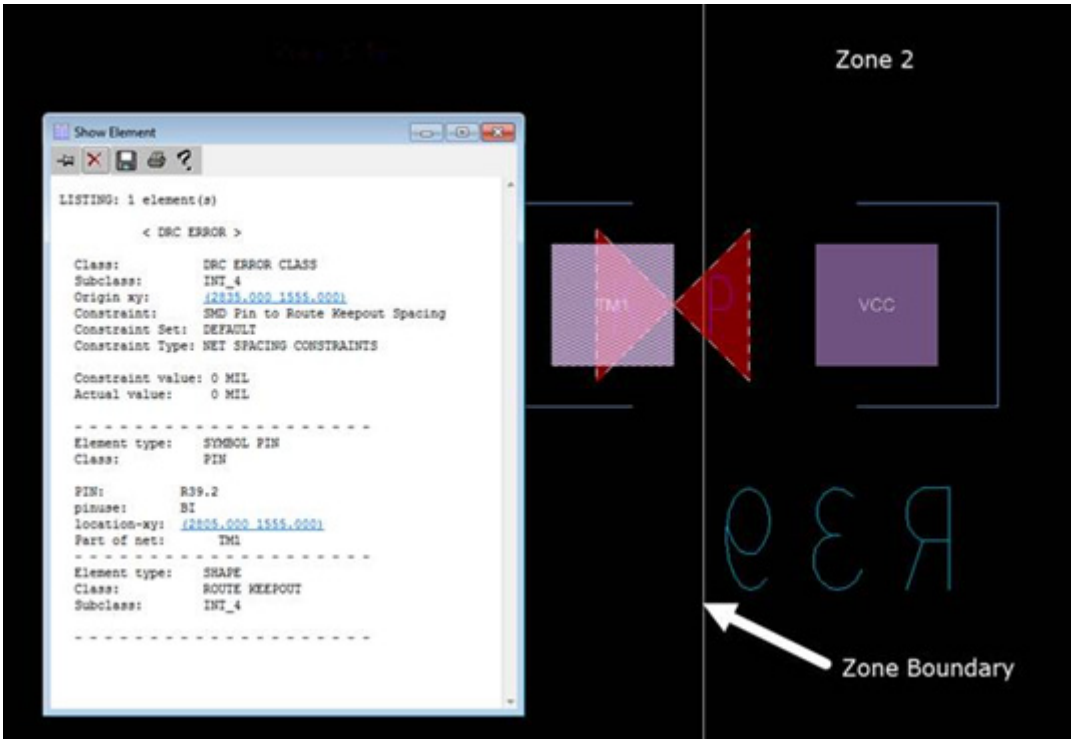
The details also indicate that the new subclass location for the reference designator is now REFDES/Assembly_LAYER_3. The component PACKAGE GEOMETRY/TOP is moved to the EMBEDDED GEOMETRY/ASSEMBLY_LAYER_3 subclass.



As components are moved from one zone to the other, the layers are adjusted to the new outermost layer definitions:

- If a component straddles a zone boundary, the zone where the symbol origin is positioned takes precedence.

- If a component is placed into a zone, and any of the pins cross into an adjacent boundary where the conductor layer does not exist for the pin, a DRC marker will display.



Flex and Rigid-Flex Bend Areas

One of the advantages of using Flex or Rigid-flex is the ability of the circuit to bend or twist to meet a particular form. A bend is defined by the side or direction of the bend, the finish angle, and the radius. Other considerations include allowing or disallowing components to be placed on a bend, or even how far from a bend the component must be to avoid interference between the bending surface and the component. Avoid placing vias within a bend area to prevent weak spots where the via may cause a failure in the bend area.

Defining a Bend Area

To define a bend area, perform the following steps:

1. Choose *Setup – Bend – Create*.

   The Create Bend Area form opens.

2. Add a unique bend area name.

   Duplicate names are not allowed.

3. Add a bend line location and the bend parameters.

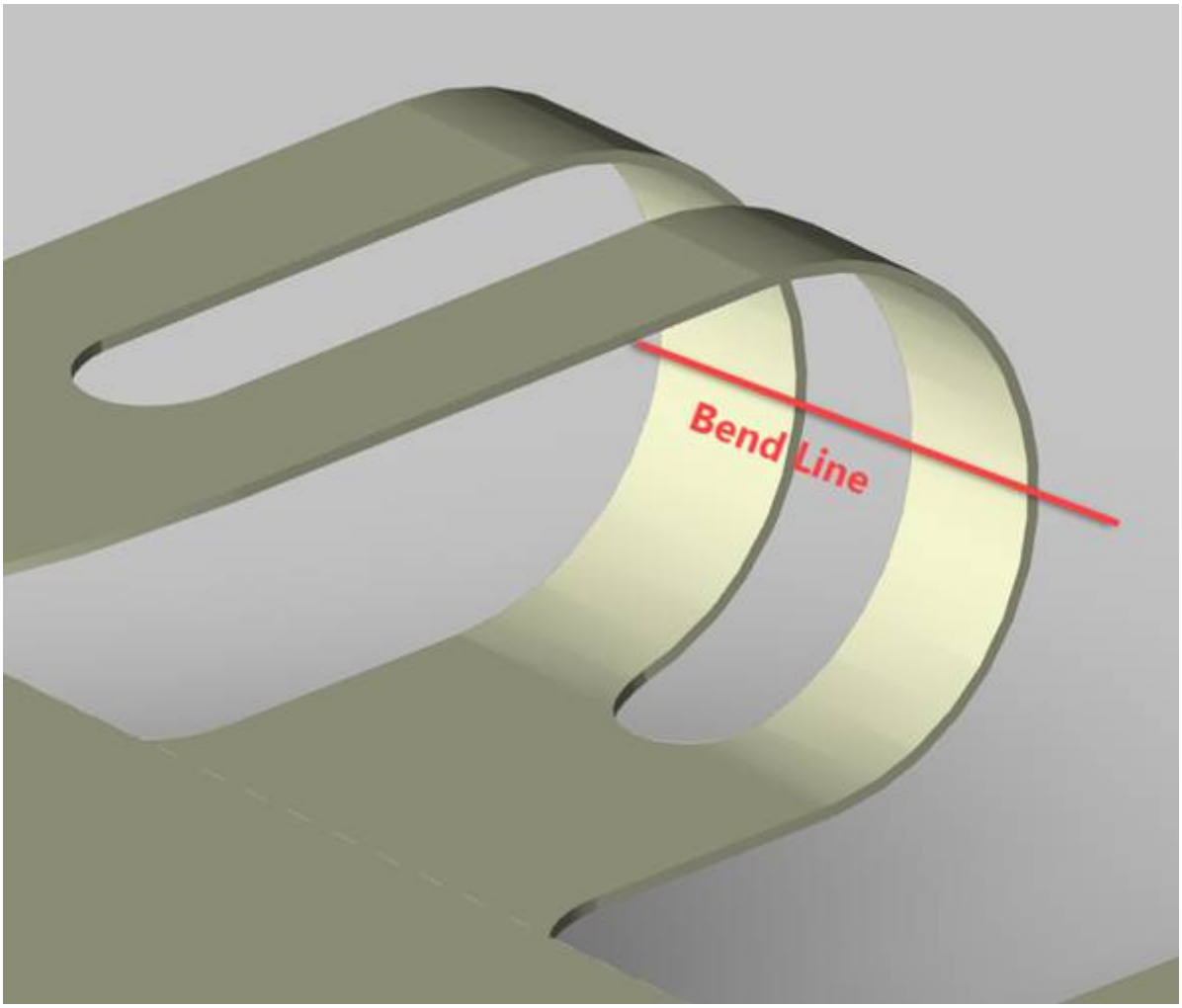
   To add a bend line, specify the start and end coordinates.

   You can also pick the coordinates on the PCB Editor canvas.

4. Optionally, add via and package keepouts with oversizing, if desired.

   Bend Areas cannot overlap. If an attempt to create or modify a bend area results in a situation with an overlap of bend area geometry, the newly added or modified bend area creation will fail, and no bend data or geometry is added to the design database for that instance. The location of the bend line or parameters will need to be modified.

   The bend line is the most critical part of a bend area. The bend line represents the midpoint of the bend and the extents of the bend area along the line's axis. The parameters defined in the Create Bend Area form are attached as a property to the bend line. This information is transferred to MCAD through the EDMD Collaborative data format (IDX).



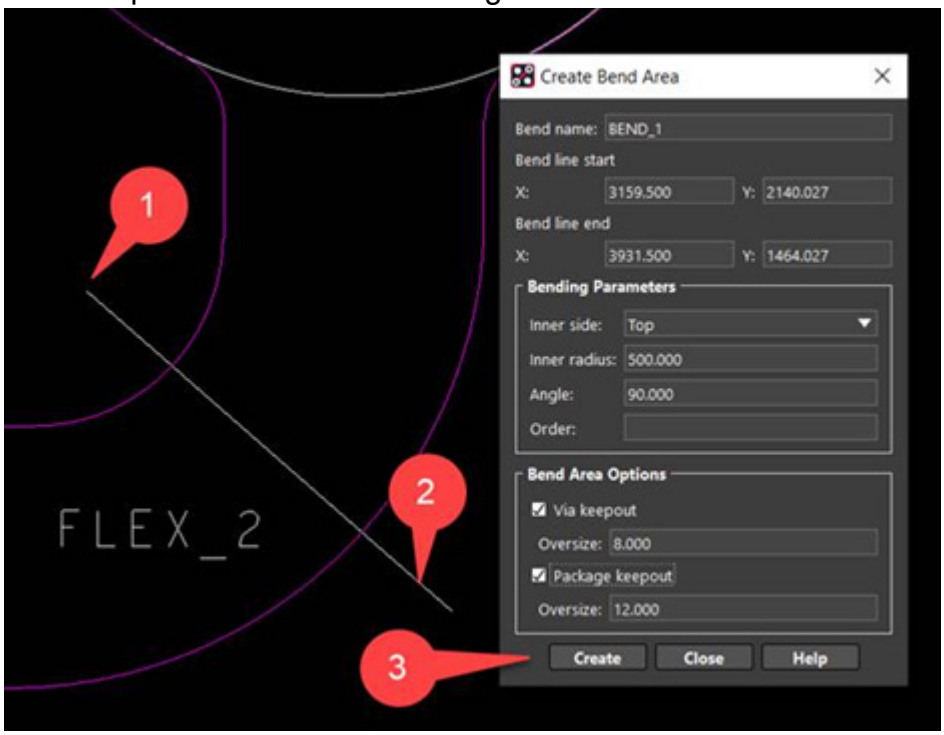
When defining the location of the bend line (added to the RIGID FLEX/BEND_LINE subclass), the end points should be carefully and accurately positioned for best results. Incorrect positioning may result in an incorrect bend area definition such as the axis along the bend line, a diagonal bend.

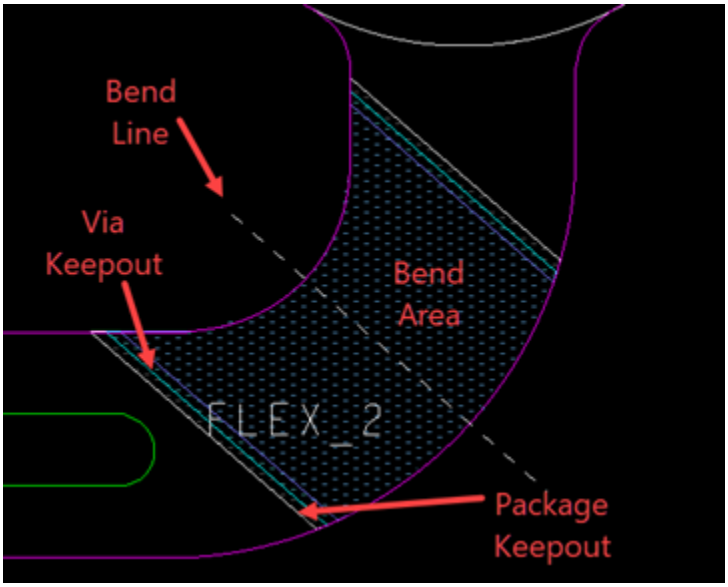
5. After the parameters are defined and the bend line is located, click *Create*.

The Bend Area is created on the RIGID FLEX/BEND_AREA subclass representing the extents of the bending area. The Bend area is a shape where the boundary is determined by:

- ❑ The bend line location and position
- ❑ Bending Parameters
- ❑ Board Geometry/DESIGN_OUTLINE definition.

The Bend area shape is trimmed to the Design outline.

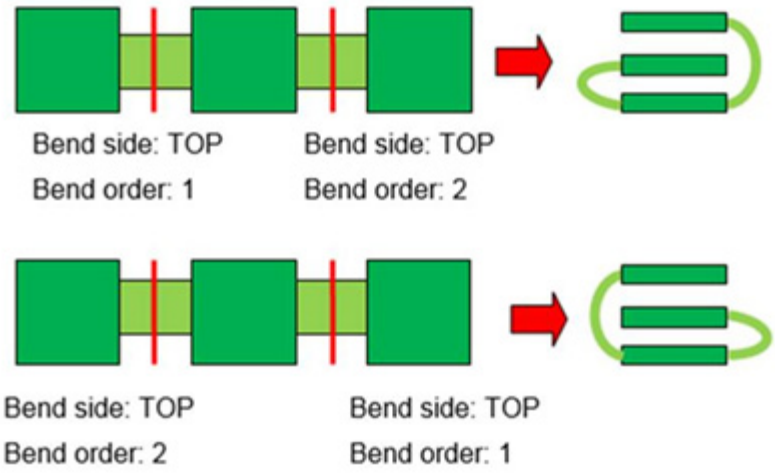




In the example, Via and Package Keepouts were selected with oversize values. When the bend area geometry is created, the keepout areas are generated based on the bend area outline. Expansion, or oversizing will occur if a value greater than 0 is entered. Negative values are not allowed. The expansion occurs along the same plane, or runs parallel to the bend line.

All of the Bend Area objects are also collected together to form a single group. The group name is defined by the Bend Area Name. Single entities in the bend area cannot be modified, the entire bend group must be managed through the Edit Bend Area function.

The Bending Data Order defines the sequence number for bending the final product. In some instances, the sequence of bends is required to obtain the proper assembly position of the design.



Modifying a Bend Area

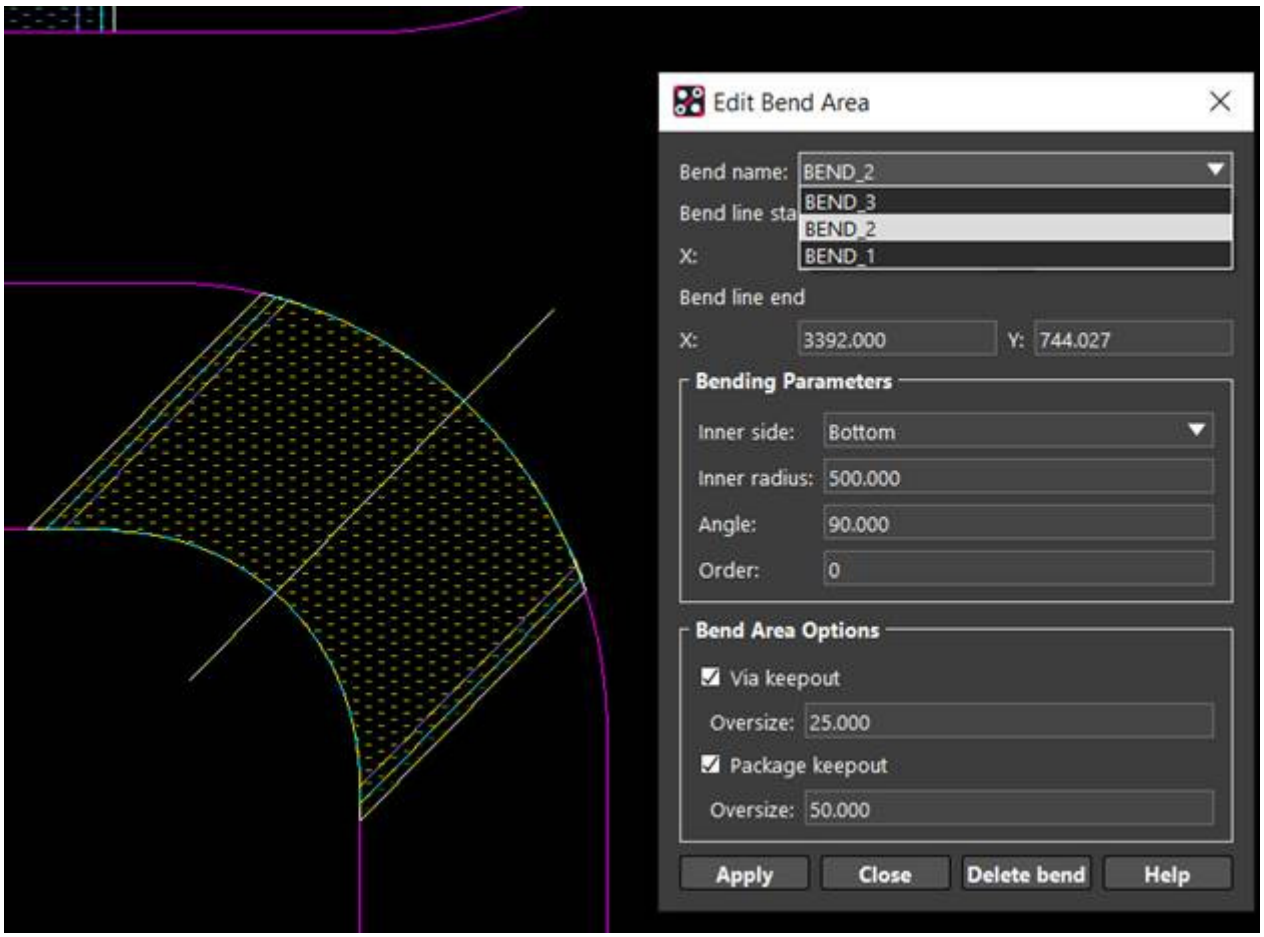
To modify a bend area, perform the following steps:

1. Choose *Setup – Bend – Edit*.

   The Edit Bend Area form opens. Use this form to modify or delete existing bend areas.

2. Select the bend area to be edited from the *Bend Name* pull down.

   When a bend area name is selected, the area is highlighted, and the PCB Editor canvas centers on the selected area.



   Modifying the bending data in the form also impacts the bend area geometry.

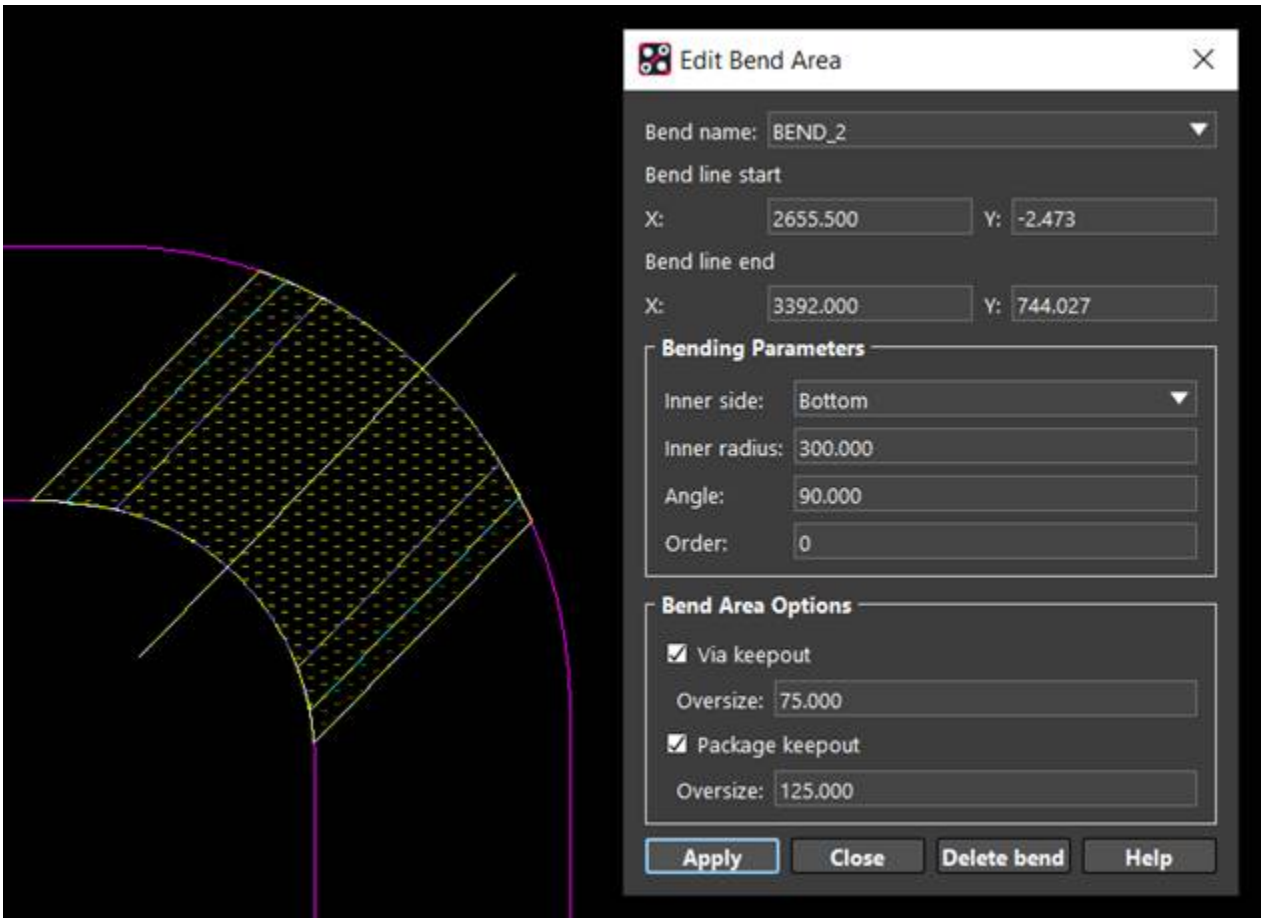
3. With the bend area selected, modify the bend line by making the new start and end point picks in the PCB Editor canvas.

   Alternatively, specify the new values in the start/end XY coordinate fields.

4. Change the other desired parameters in the Edit Bend Area form.

5. Click *Apply*.

   The changes are updated to the bend. The parameters may be altered and applied until the desired result is achieved.



The InterLayer Checks

In typical Rigid Flex designs, the creation of various masks, bend areas, stiffeners, and so on require special clearances or overlaps of materials and spacing. These objects are represented on specific subclasses that require a verification process to ensure that the clearances and overlaps are properly met. Allegro PCB Editor provides the ability to perform a check on geometries that exist on two different Class/Subclasses. The InterLayer Checks that perform this task are defined in Allegro Constraint Manager.

Inter-layer checks can be run as part of the on-line DRC process, set as a batch process, or turned off. This is accomplished by using the Constraint Analysis Modes Design Options for On-line InterLayer Checks.

Using InterLayer Check Rules

The basic interlayer rule definition requires two different Class/subclasses, a choice of four rule types, and how the DRC marker should be displayed. The four checks available in the InterLayer Check definitions are:

- Gap
- Overlap
- 1 Inside 2
- 2 inside 1

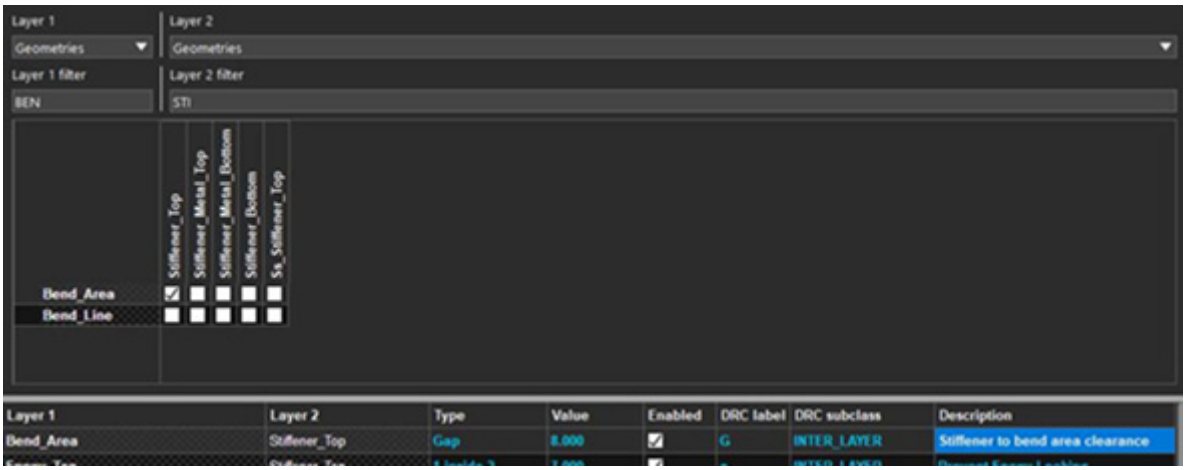
Gap

When two objects on different subclasses need to be a minimum distance apart, the Gap rule is used to perform that check. For example, the edge of any Stiffener in the design must be a minimum of 1.27mm away from a Bend_Area.

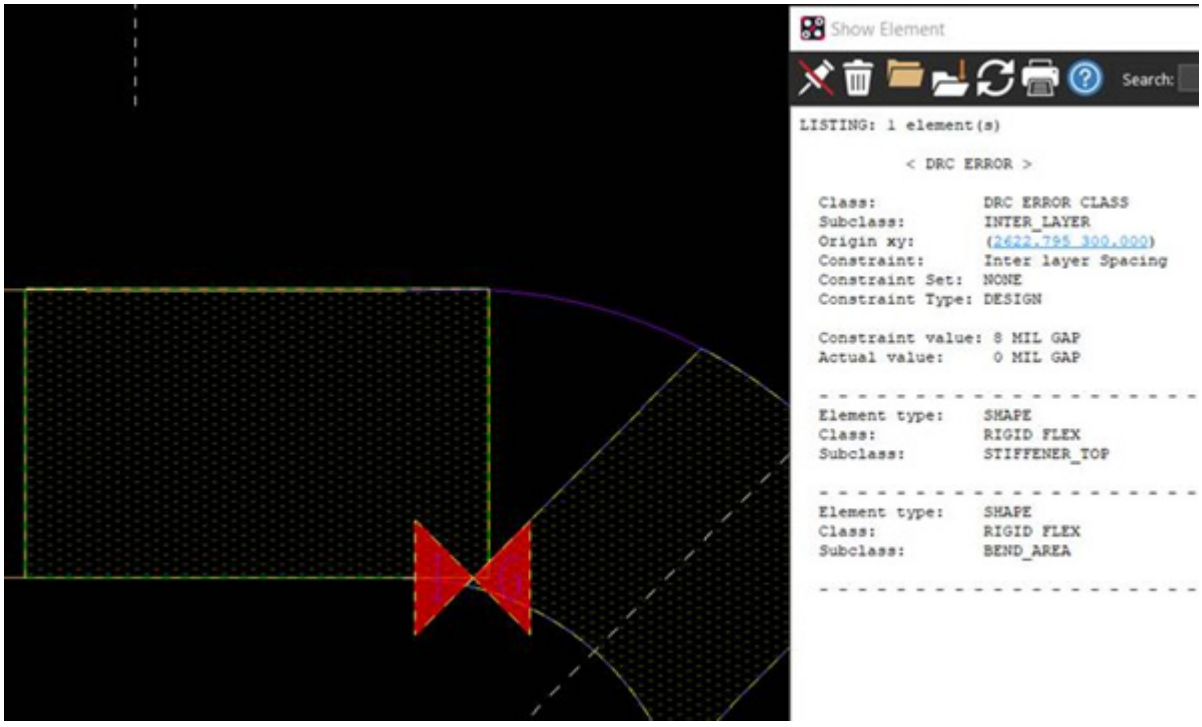
To enable a Gap check:

1. In *Constraint Manager – Spacing – Inter Layer – Spacing*, select the subclasses for BEND_AREA and STIFFENER_BOTTOM.
2. Select the rule type as *Gap*.
3. Define the minimum gap value.
4. Select the checkbox to show a DRC marker if this condition is violated.
5. Specify a character for the DRC marker character. In this case, use *G* to represent Gap.

6. Specify the Display layer. For example, INTER_LAYER. Alternatively, add a note to inform users of the intent of the rule.



With the gap rule in place, any violation is flagged with a DRC marker. In this example, the Shape that represents the stiffener is edited to correct the violation.

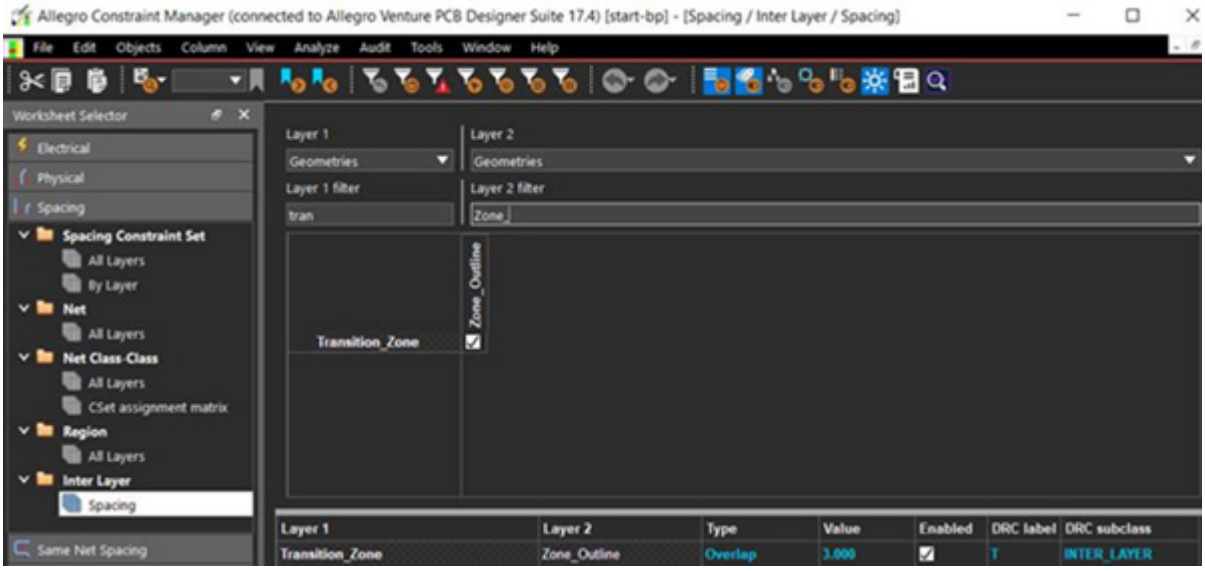


Overlap

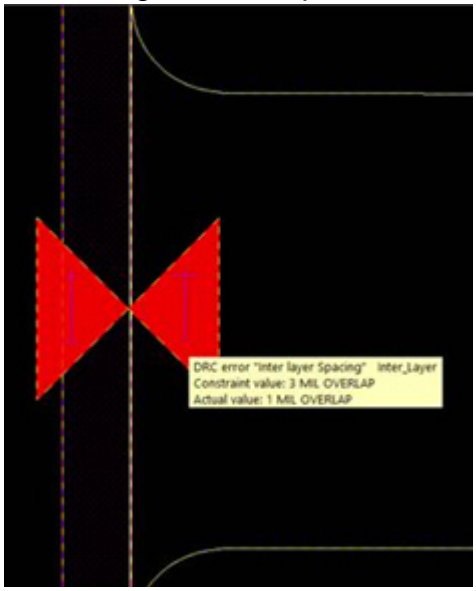
The overlap rule is used to ensure that one item overlaps another by a minimum amount. For example, a transition area must overlap a zone boundary by 3 MILS.

To enable an Overlap rule:

1. Select the TRANSITION_ZONE and ZONE_OUTLINE subclasses.
2. Select the rule type as *Overlap*.
3. Define the overlap value.
4. Assign a DRC label. For example, choose *T* for Transition.
5. Assign the DRC Display Layer.



When the user adds a transition area geometry and violates the overlap rule, a DRC marker is displayed indicating the overlap value has not been met.



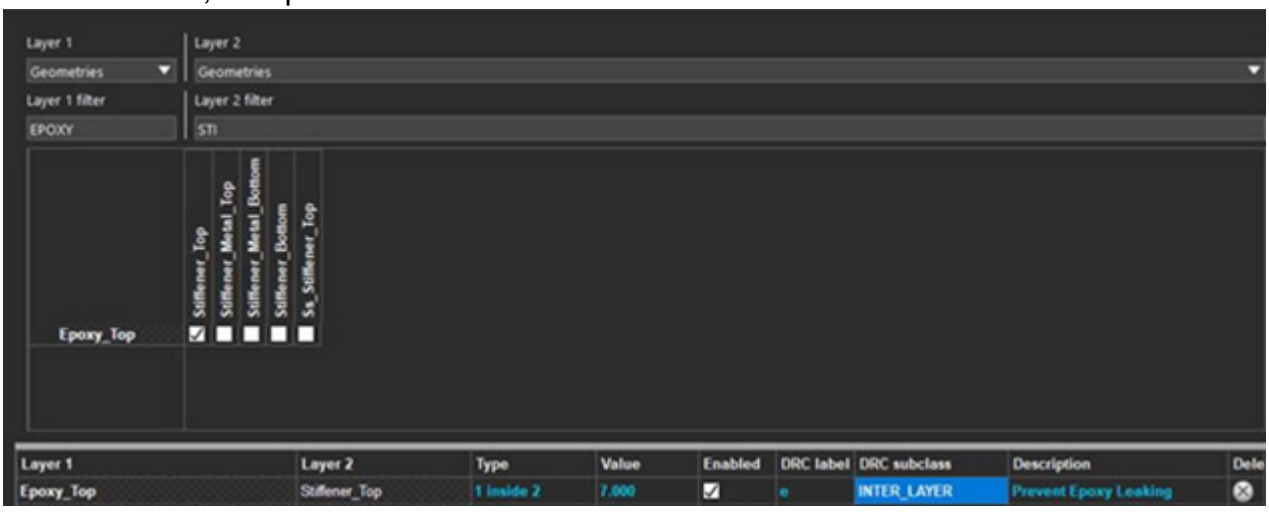
Overlap of geometries is detected in both X and Y axis when the objects intersect. The following examples are based on an Overlap value of 10 mils.

Inside Rules – 1 Inside 2 and 2 Inside 1

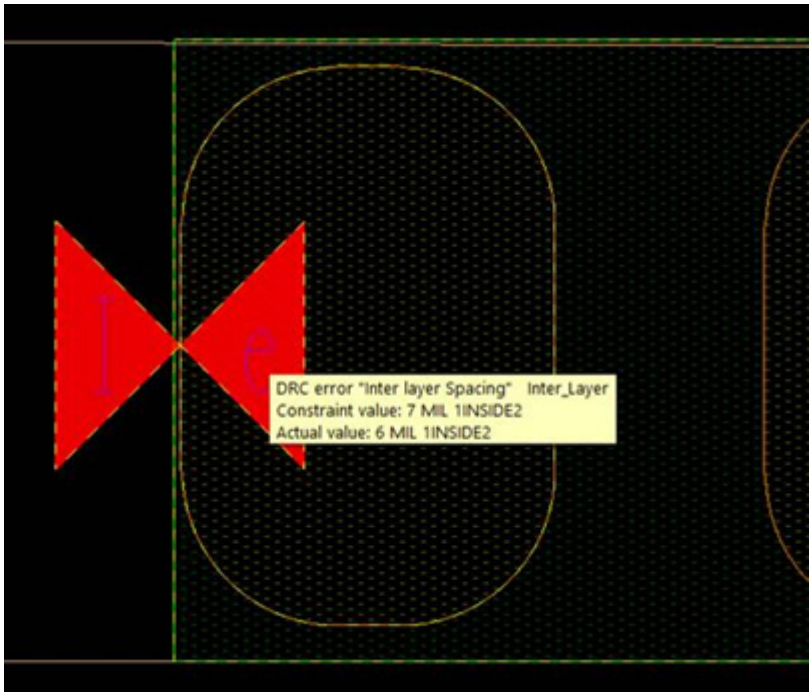
The Inside rules are used to check that a graphical element on one subclass is contained within another geometry defined on another subclass. For example, an epoxy adhesive can be used as a stiffener. The adhesive edge to stiffener edge distance must have a minimum value of 3 mils to prevent the epoxy from leaking out the sides of the stiffener.

1. In Constraint Manager Inter Layer rules, select the two subclasses:
   - ❑ Select the subclass EPOXY_TOP. This will be designated as Layer 1.
   - ❑ Select Layer 2 as the STIFFENER_TOP subclass.

   With the EPOXY_TOP subclass contained within the STIFFENER_TOP, the rule 1 Inside 2 is selected, indicating that Layer 1 is within the bounds of the object on Layer 2.
2. Assign the edge to edge spacing value as 3 mils.
3. Set the DRC label to “e” for epoxy.
4. Assign the DRC Display Layer to INTER_LAYER.
5. Add a note, if required.



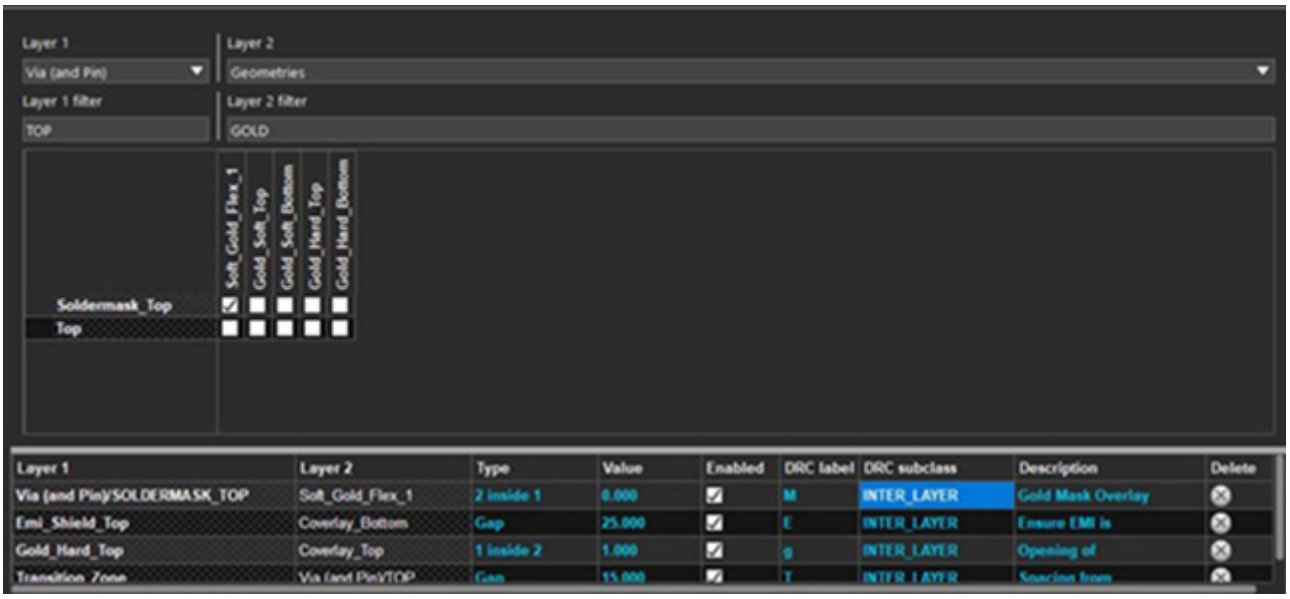
As the user adds the geometry that represents the epoxy adhesive, the DRC checks the distance between the epoxy geometry and the stiffener geometry edges. If in violation, a DRC will display indicating the issue.



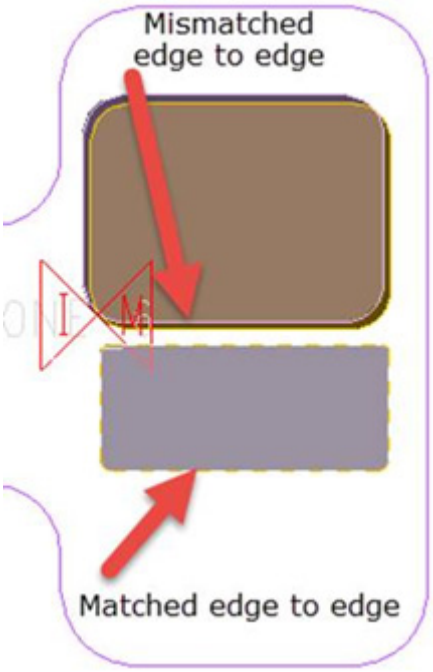
When two objects on different subclasses must have matching outlines, such as a Gold Mask on a Component Pin, the Inside check may also be used. To set the exact outline match, the value for the check is set to “0.00”.

- The rule is defined as category Via (and Pin), and TOP and GOLD_SOFT_TOP subclasses are selected.
- The 2 Inside 1 rule type is set with a value of 0.00.
- The “M” character is used to represent mask.
- The DRC is displayed on the INTER_LAYER subclass.

- A note is also added.



When the two subclasses are checked, the DRC violation is displayed,



Limitations of InterLayer Checks

Inter layer checks do not:

- Permit checking between Etch Layers, such as TOP etch to BOTTOM etch

- Same Layer checks (Coverlay_top to Coverlay_top)
- Distinguish between a Trace (Cline) or copper area (Shape).

Other Classes, Subclasses, and objects that are not included in the Inter Layer checks are:

- Drawing format
- Analysis
- DRC
- Text (on any subclass)
- Board geometry outline
- Silk Screen layers
- Named dielectric layers

The subclasses enabled for InterLayer checking are :

`Conductor Layers (No Text)`	Place Bound (TOP/EMBEDDED/BOTTOM)
`Pin/Via Layers`	Filmmask (TOP/BOTTOM)
`All Mask Layers (stackup defined)`	Soldermask(TOP/BOTTOM)
`Rigid Flex Subclasses`	Pastemask(TOP/EMBEDDED/BOTTOM)
`Surface Finishes Subclasses`	User Defined Subclasses **Note:** User defined subclasses in excluded classes are not enabled.