

# **Topology Workbench Frequently Asked Questions**

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# Frequently Asked Questions for Topology Workbench

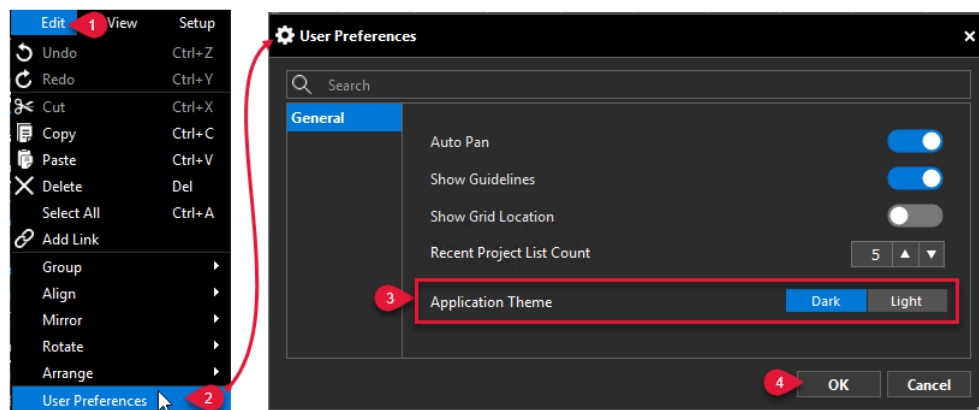
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### Related Document

In addition to this document, you can refer to [Topology Workbench User Guide](#) for detailed procedural information related to the Topology Explorer, SystemPI, Parallel Bus Analysis, Serial Link Analysis, AMI Builder, and Compliance Kits workflows of Topology Workbench.

### Can I change the overall "Dark" theme appearance of the Topology Workbench interface?

The *Dark* theme is the default for the Topology Workbench interface. You can choose between *Light* and *Dark* themes in the *User Preferences* dialog box that is accessible from the *Edit – Preferences* menu as shown below.



### Why are there no TLines in the Constraint Topology tab?

TLine elements between pins were required in SigXplorer, but are not needed in Topology Workbench. This allows for a cleaner view of the topology where the focus is on the connectivity between the pins. T-points can still be inserted into the topology if needed.

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## Frequently Asked Questions for Topology Workbench

### How do I expose a single pin from a multi-pin connection?

Block-based connectivity uses multi-pins where multiple signals are combined into a single connect point. To expose single pin from a multi-pin connection, perform the following steps:

1. Double-click a multi-pin to expose the list of signals in the *Properties* pane.
2. Select one or more signals.
3. Click right and select *Remove Selected Pin(s)* from the menu to break the selected pin(s) into new individual pins.

The figure below illustrates the steps to expose pins 3 (*dq0*) and 6 (*dq3*) from a multi-pin connection:

1 Double-click a multi-pin. The *Properties* panel opens with a list of combined signals.

2 Select the required signals and right-click.

3 Select *Remove Selected Pin(s)*.

The exposed pins (3 and 6 in this example) are removed from the multi-pin connection.

The exposed pins are separated from the multi-pin. Also, notice the change in total number of signals in the multi-pin reduces as shown in this example (11/42 changes to 9/40).

Net	Pin	Cktnode
vddq	1	1
vssq	2	2
dq0	3	3
dq1	4	4
dq2	5	5
dq3	6	6
dq4	7	7
dq5	8	8

Net	Pin	Cktnode
vddq	1	1
vssq	2	2
dq1	4	4
dq2	5	5
dq4	7	7
dq5	8	8
dq6	9	9
dq7	10	10

To reverse the process, select and drag a pin, and then drop it on top of another pin to merge the signals into a single pin.

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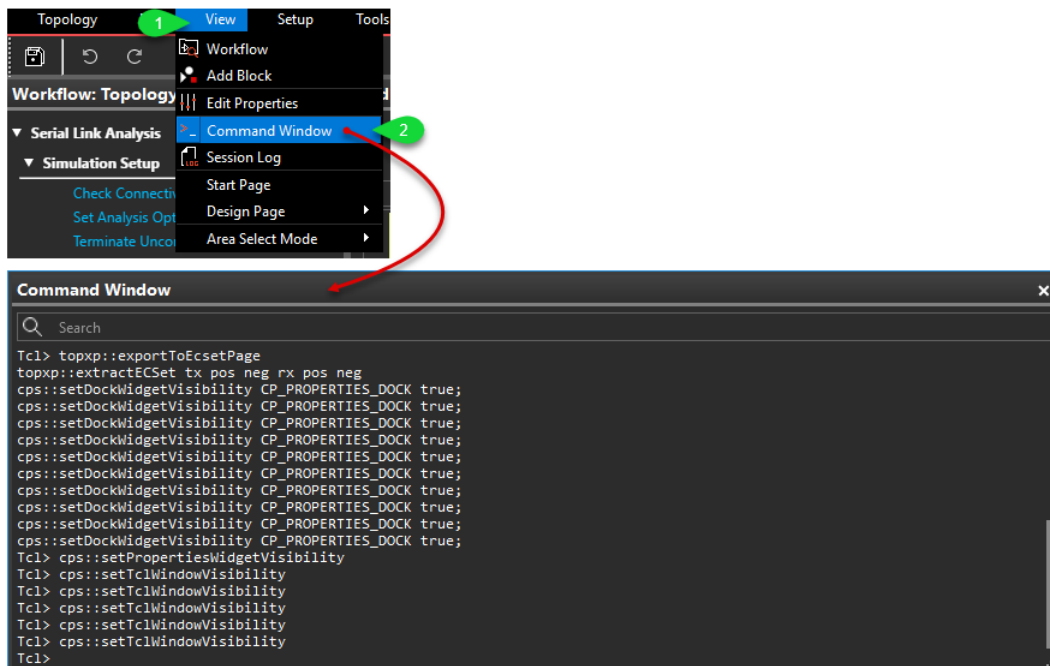
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#### Can I change the grid settings in the canvas?

The grid settings in the canvas cannot be changed.

#### Are there Tcl commands available?

Topology Workbench is completely based on Tcl. The related commands can be exposed using the *View – Command Window* menu as shown below.



**Note:** The *Command Window* panel is a dockable window. To detach the panel from the Topology Workbench window, click its title bar and drag it while keeping the mouse button pressed. To attach it back again, double-click the title bar of the panel.

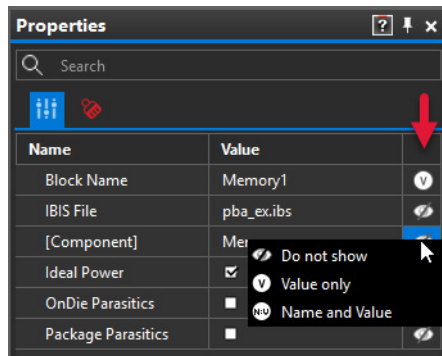
#### How can I extract a topology from Allegro?

Set the `use_topxp_for_sigxp` environment variable in Allegro.

**Note:** This only impacts the *View Topology* button in the *Analyze – Probe* dialog box.

### Can I annotate additional attributes to blocks on the canvas?

Yes. The third column in the *Properties* pane controls the visibility of the attributes.



When you click the visibility control button adjacent to the attribute that needs to be edited, you can select one of the following options:

- *Do not show* to hide the attribute.
- *Value only* to display only the value of the attribute.
- *Name and Value* to display both attribute name and value.

### What are the differences between level 1, 2, and 3 extraction?

Level 1 extraction contains no coupling and assumes an ideal power supply to the IO (transmitter and receiver) models.

Level 2 extraction adds signal coupling (for example, crosstalk effects), while still using ideal power.

Level 3 extraction adds signal coupling and non-ideal power effects, such as, simultaneous switching noise (SSN).

### How can blocks be interconnected?

Blocks can be connected with one big bus-level connection that can contain many node-to-node connections underneath. For example, in a DDR topology, there can be one bus-level connection between a package and PCB block that may contain 64 data signals, a differential strobe, and a ground reference. In addition to block-based connections, simple wire-based connections are also supported, where you can have multiple wires connect between blocks, with each connecting a pair of nodes.



## **Can a combination of block- and wire-based connectivity be used in the same topology?**

Yes, a combination of block- and wire-based connectivity can be used in the same topology.

## **Can I create my own templates?**

Yes, it is possible to create your own templates as a starting point. You can save them into your software installation with the standard templates or save them in another location and browse to them as a starting point for a project.

## **Which circuit simulators are supported with Topology Workbench?**

The SPEED2000 simulator (SPDSIM) is included as part of Topology Workbench. HSPICE and SPECTRE are also directly supported if you have a licensed installation of those simulators in place.

**Note:** SPECTRE is currently available on Linux only.

## **What other types of models are supported?**

The elements that comprise a topology are all associated with a SPICE subcircuit, including S-parameter Touchstone files, IBIS, transistor-level, behavioral Spice IO models, and W-elements.

## **What if my circuit simulation does not converge?**

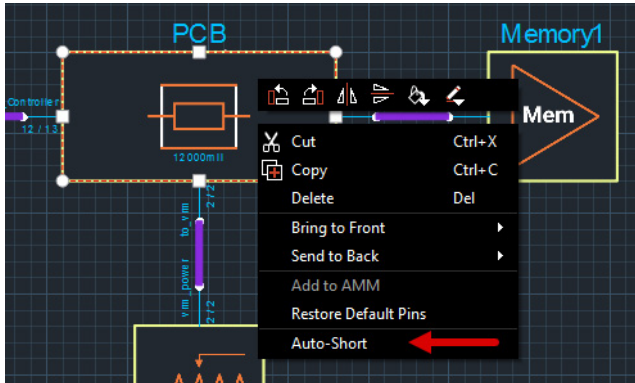
Usually this is due to a poorly-behaved S-parameter model. This can be tracked down by sequentially shorting out blocks using the *Auto-Short* command from the shortcut menu

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displayed when you right-click a block. The offending model can then be replaced, or sometimes repaired for time domain simulation using Broadband SPICE.



### What is a power-aware SI?

This refers to when non-ideal power effects like SSN are modeled in the topology. This becomes increasingly important as data rates go up and margins go down.

### Can I perform mask-based checking for DDR interfaces?

Yes, waveforms are post-processed to determine how to position masks within the associated eye diagrams, enabling margins to those masks to be automatically measured.

### Are AMI models mandatory for channel simulation?

No. AMI models are for transmitters and receivers with algorithmic content, which for SerDes devices is typically adaptive filtering. With adaptive filtering, the device's filter coefficients are optimized on-the-fly based on a particular channel. However for SerDes that use static (non-adaptive) filtering or no equalization, no AMI model is required.

### How many AMI models are supported for each device?

Multiple AMI models can be cascaded together in Topology Workbench. This unique feature can be used to simplify the creation, debug and use of AMI models.

## **Can the tool generate IBIS-AMI models?**

Topology Workbench includes an application called AMI Builder, with which you can create AMI models for both transmitter (Tx) and receiver (Rx). AMI Builder includes an advanced set of AMI models, such as feed-forward equalization (FFE), clock and data recovery (CDR), linear and non-linear decision feedback equalization (DFE), and continuous-time equalization (CTE). Any user with a Topology Workbench license can create and use these AMI models. For testing, Topology Workbench provides a robust environment to test out the channel with and without the AMI models enabled to verify the AMI model's behavior.

## **Which algorithm is used by default for models generated by AMI Builder for automated FFE tap optimization?**

A Least Mean Square (LMS) algorithm is used, which is common in the industry.

## **Can I use channel simulation for parallel buses like DDR4?**

Yes. This enables AMI models to be used, jitter/noise injection to be incorporated, and bit error rate (BER) analysis to be performed using bathtub curves.

## **What stimulus types are available for the transmitter?**

Random patterns, PRBS (up to 100), and user-defined patterns are all supported. The random number generation is based on 128-bit Tiny Encryption Algorithm (TEA). Different encoding schemes, for example 8b/10b and 64b/66b, can also be used.

## **What is the difference between random and PRBS bit patterns?**

Random bit patterns will repeat only after 2<sup>128</sup> bits. Pseudo-random bit sequence (PRBS) patterns are generated based on the linear feedback shift register (LFSR) technique. A PRBS<sub>31</sub> pattern will repeat after 2<sup>31</sup> bits.

## **How large of a bit stream is practical to use as stimulus?**

200,000 bits will be sufficient to enable most design decisions and trade-offs to be made rapidly. For final verification, it is typical for users to simulate up to 10 million bits. However, the real answer should be to the question that *'when does the eye contour stops shrinking significantly?'*

## **What is the difference between random and deterministic jitter and noise?**

Random noise and jitter are external to simulation and are known as unbounded *white* Gaussian noise and jitter. Deterministic noise and jitter are bounded. A dominant source of deterministic noise and jitter is the Phase Locked Loop (PLL), and PLL reference clock power noise. You can use the periodic jitter or noise option to introduce this kind of noise into simulation.

## **How are jitter and noise injections associated with the Tx AMI models incorporated into the analysis?**

Jitter and noise injections associated with Tx are incorporated into the bit stream stimulus applied to the Tx AMI model. Both types of jitters, deterministic and random, can be applied to the stimulus bit stream. Multiple sub-components of deterministic jitter (Dj), such as periodic jitter (Pj) and duty cycle distortion (DCD), can be applied. In addition, random jitter (Rj) can also be applied to the transitions in the bit stream, assuming Gaussian distribution.

## **How are jitter and noise injections associated with the Rx AMI models incorporated into the analysis?**

In contrast with the Tx jitter and noise injection, where the impairments are applied to the stimulus bit stream, jitter and noise injections associated with the Rx AMI models are all post-processed into the eye distribution produced from the channel simulation. Both deterministic and random jitter and noise are considered. A Gaussian distribution (out to 8 sigma) is used to represent Rj and Rn, while Dj and Dn are represented by a simple rectangular window. The effects of all these impairments are incorporated into the statistical analysis used to produce bathtub curves to predict BER.

## **How are random and deterministic jitter and noise values entered?**

The Rj and noise values are specified as RMS values. If the data is available as a peak-to-peak value, you first need to convert it to the associated RMS value, and then enter it into the tool.

For example, 70ps peak-to-peak random jitter for a BER of 1e-12 would yield an RMS value of about 5ps. This is then entered in terms of % UI.

Deterministic jitter and noise values are specified as the peak values. If the data is provided as a peak-to-peak value, it needs to be divided in half.

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For example, 6ps peak-to-peak deterministic jitter is entered as the peak value of 3ps, in terms of % UI.

### How is transition jitter and noise incorporated into the analysis?

It is applied directly to each clock period of the ideal incoming bit stream that gets synthesized as stimulus for the Tx AML model. Therefore, these effects can potentially be amplified by the channel during the time domain channel simulation.

### What is Duty Cycle Distortion (DCD)?

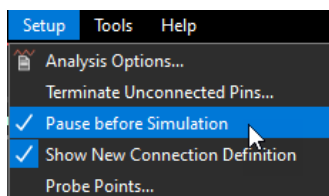
DCD is the deviation in duty cycle from the ideal value of 0%, for the clock associated with the incoming bit stream. Ideally the pulse widths of the positive and negative pulses of the clock period are identical or 0% different.

### How many crosstalk channels are supported?

There is no direct limit to the number of crosstalk channels that can exist in a topology (although check any associated AML models for a maximum limit). A characterization will be run for each transmitter found in the topology.

### Which state are the other transmitters held in during characterization of topologies with crosstalk channels?

By default, the input stimuli to transmitter IOs not exercised are held in a logic state 0 (zero) during characterizations. You can modify this by editing the SPICE deck prior to characterization simulations by using the *Pause before Simulation* option from the *Setup* menu.



### What is meant by Statistical crosstalk mode?

Statistical crosstalk is used to find the *average* crosstalk that might be produced in a system. The crosstalk aggressor probability density functions (PDF) are statistically computed, and a

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statistical *average* of this crosstalk is convolved with the PDF of the through channel to produce the overall result.

### Is Statistical crosstalk computation the worst case?

Some people consider statistical crosstalk to represent the worst case, but it is somewhat subjective. Therefore, multiple options are provided to let the user select their preferred method. Statistical crosstalk is not preferred if the Rx AMI model uses real-time adaptive filtering with the `AMI_GetWave` function. In this case, the time domain channel simulation method is recommended over the statistical approach.

### What results are provided for serial link simulations?

Serial Link Analysis outputs include step and impulse responses, 2D eye contours and bathtubs, 3D eye diagrams and bathtubs, raw waveforms, and a summary report.

### What effects are included in eye contours and eye density plots?

Eye contours are derived directly from the raw time domain waveforms of the channel simulator. The eye density plots include the added effects of the Dj, Dn, Rj, and Rn settings defined in the Jitter & Noise tab associated with the Rx.

### Why does the report show more bits simulated than what I have defined?

The number of bits will be always slightly larger than you've specified, because the simulation is done by blocks, and the block sizes are automatically optimized for simulation performance.

### What is the meaning of normalized jitter and noise (NJN)?

Within one Unit Interval (UI) in an eye diagram, the tool looks at how much open area there is in the middle of the eye vs. the entire area within the eye envelope. Whatever percentage is NOT in that open area is considered jitter and noise. Therefore, NJN is a dimensionless metric that helps you rank the quality of one eye from another.

## **Are there any limitations for using probe points in topologies with AMI models?**

Yes. Any AMI model that uses the impulse response of the channel to ***automatically*** derive its settings will not produce reliable results for probe points. When probe points are placed into the topology, they essentially get their own characterization, or impulse response. If the transmitter (Tx) AMI model automatically derives its settings on-the-fly based on impulse response, then the probe point will essentially get its own custom and optimized EQ settings. This contrasts with what is really desired, which is to see the result at the probe point with the same settings that are used for the main characterization of the receiver (Rx). The way to handle this is to manually set the Tx AMI model parameters (for example, its tap coefficients) as desired, and not let it self-optimize. Then the probe will get the same EQ settings as the main channel.

## **Can I define my own compliance kit content for serial links?**

Yes, using the *Generic Compliance Kit* workflow.

## **Can backchannel training be simulated?**

Yes, backchannel is supported if the Tx and Rx IBIS-AMI models contain the required reserved keywords.

## **Can multi-level signaling like PAM4 be simulated?**

Yes, PAM3 and PAM4 signaling is supported for simulation.