

# **PSpice A/D Simulations in Allegro® X System Capture**

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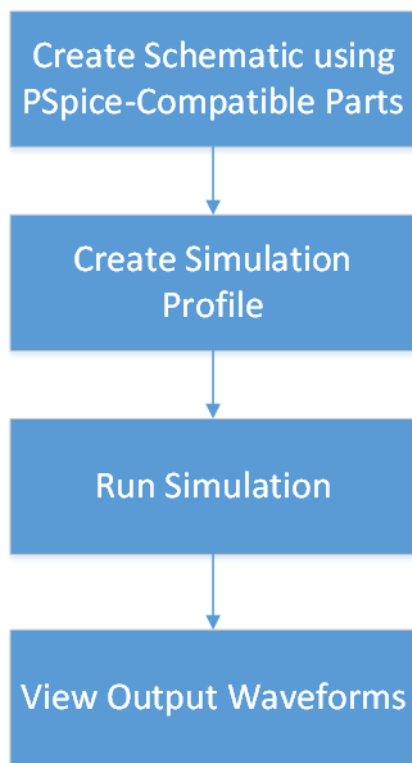
## Simulating System Capture Designs

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With the integrated System Capture – PSpice flow, schematic designs created in System Capture can be easily simulated in PSpice A/D. The integration provides seamless access to PSpice features from within System Capture.

*Important*

System Capture - PSpice flow is available only on Windows.



### System Capture – PSpice Flow

# PSpice A/D Simulations in Allegro X System Capture

## Simulating System Capture Designs

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To simulate a design in PSpice, components must have an associated PSpice model. You can use components from PSpice-compatible Cadence-supplied libraries, or create new components for the available models.

## Setting Up Simulation Environment

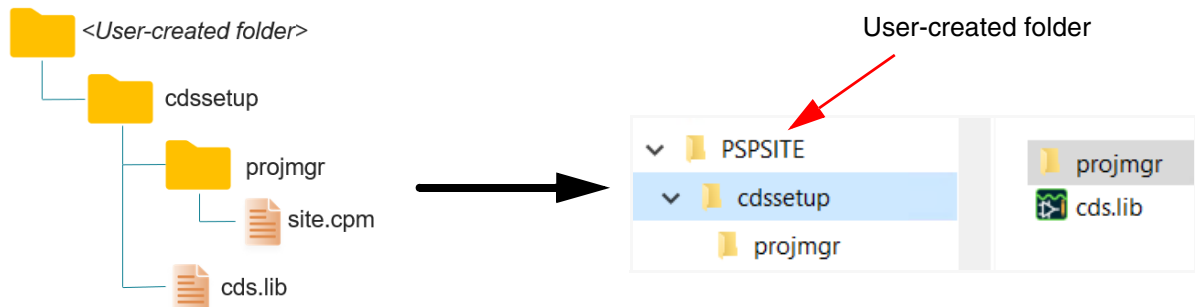
Before you can create a System Capture schematic that can be simulated using PSpice, you need to complete the following tasks:

- Set Up PSpice Libraries
- Enabling PSpice in System Capture

### Set Up PSpice Libraries

Cadence-supplied libraries are shipped as a self-extracting executable in the installation. To make these component libraries available in System Capture, complete the following tasks:

1. Navigate to `<install_dir>/share/canvaslibrary/pspice`, and double-click `pspicecanvaslib.exe` to extract the PSpice libraries.
2. Create a new folder with the following folder structure.

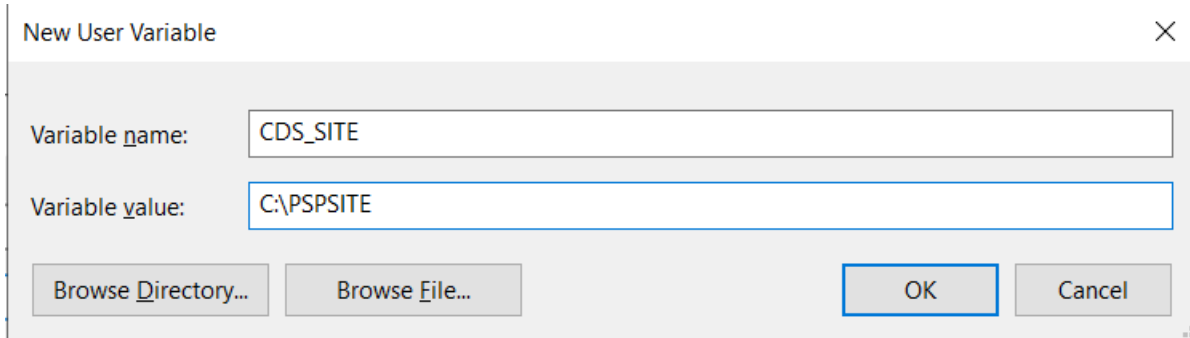


## PSPice A/D Simulations in Allegro X System Capture

### Simulating System Capture Designs


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3. Set the `CDS_SITE` variable to point to the folder created in [step 2](#)



Setting the `CDS_SITE` variable ensures that parts from the Cadence-supplied libraries can be instantiated in System Capture.

4. Modify `cds.lib` to include the Cadence-supplied PSPice libraries, the standard library, and any other libraries that you need to use during the schematic design process.

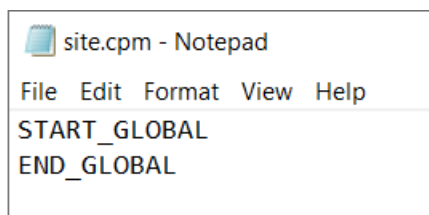
 `cds.lib` - Notepad

File Edit Format View Help

```
DEFINE standard <Installation_hierarchy>/share/library/standard
## standard library is must for System Capture
```

```
INCLUDE <Installation_hierarchy>share/canvaslibrary/pspice/canvaspsp_cds.lib
## Path to the folder containing libraries extracted from pspicecanvaslib.exe
```

5. Under the `projmgr` folder, create a `site.cpm` file with statements `START_GLOBAL` and `END_GLOBAL`.



The `site.cpm` file is required to ensure that the PSPice library components shown under the *Library* tab of Unified Search panel in System Capture.

## Enabling PSPice in System Capture

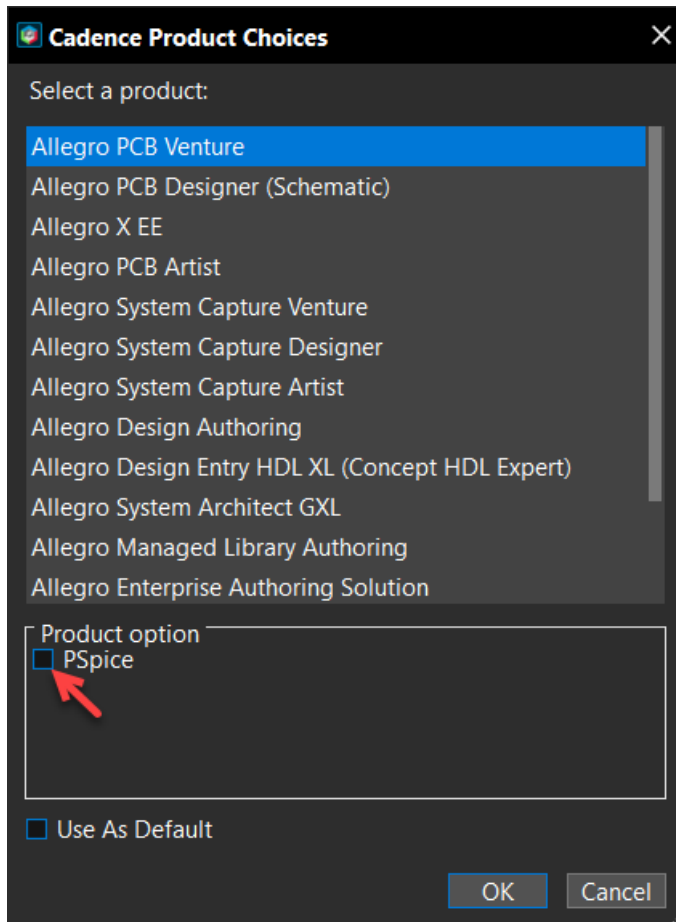
To enable the System Capture - PSPice integration flow, you need an enterprise license, such as *PS2200* or *SDA 200*.

## PSpice A/D Simulations in Allegro X System Capture

### Simulating System Capture Designs

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- ➔ When launching System Capture, select the *PSpice* product option in addition to the System Capture license, in the Cadence Product Choices dialog box.



**Note:** Selecting the option enables PSpice toolbar and menus in System Capture.

System Capture starts and a dialog box listing the available PSpice licenses is displayed.

## Creating New Project

System Capture-PSpice flow is supported only for the designs that are based on Design Entry HDL libraries.

To create a new project using Design Entry HDL libraries, do the following steps:

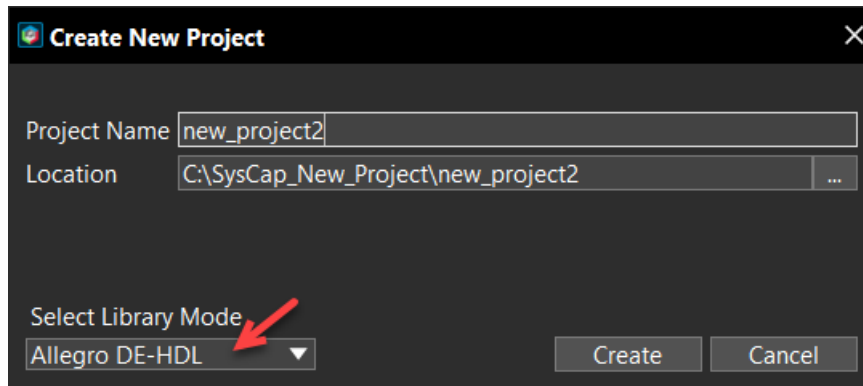
1. Choose *File – New Project*.
2. Specify the project name and location.



## PSpice A/D Simulations in Allegro X System Capture

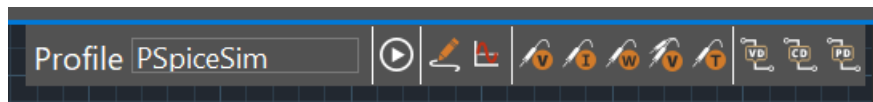
### Simulating System Capture Designs

3. From the *Select Library Mode* list, select *Allegro DE-HDL* and click *Create*.

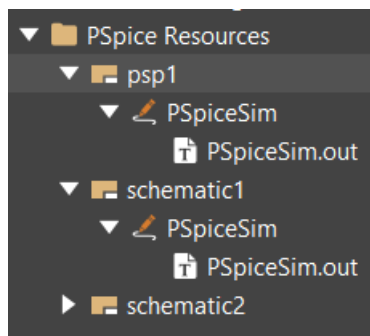


A project is created, and a blank canvas opens in System Capture.

A new menu—*PSpice*—is added to the menu bar. In addition, a new floating toolbar is added on the upper-right corner of the canvas. The toolbar contains icons to run simulations, edit simulation profiles, view simulation results, and add markers.



The Project Explorer panel displays a new entry, *PSpice Resources*. Under this node, PSpice resources for the entire design are listed. If a design has multiple blocks, block-specific resources are listed under each block name.



## Placing Components

Parts from the libraries included in the project are available for placement from the Unified Search panel.

To place a part, do the following:

1. Search for the component in the Unified Search panel.
2. Right-click the component and choose *Place Part*.

Unified Search				
Library (28k+)		My Parts		
CLASSIFICATION		*		
PART NUMBER	CLASSIFICATION	FOOTPRINT	LIBRARY	SUMMARY
\$d_hi	\$d_hi		dataconv	
\$d_lo	\$d_lo		dataconv	
0	0		source	
0402CS-10N	0402CS-10N			
0402CS-11N	0402CS-11N			
0402CS-12N	0402CS-12N			

## Placement Checklist for PSpice-Compatible Designs

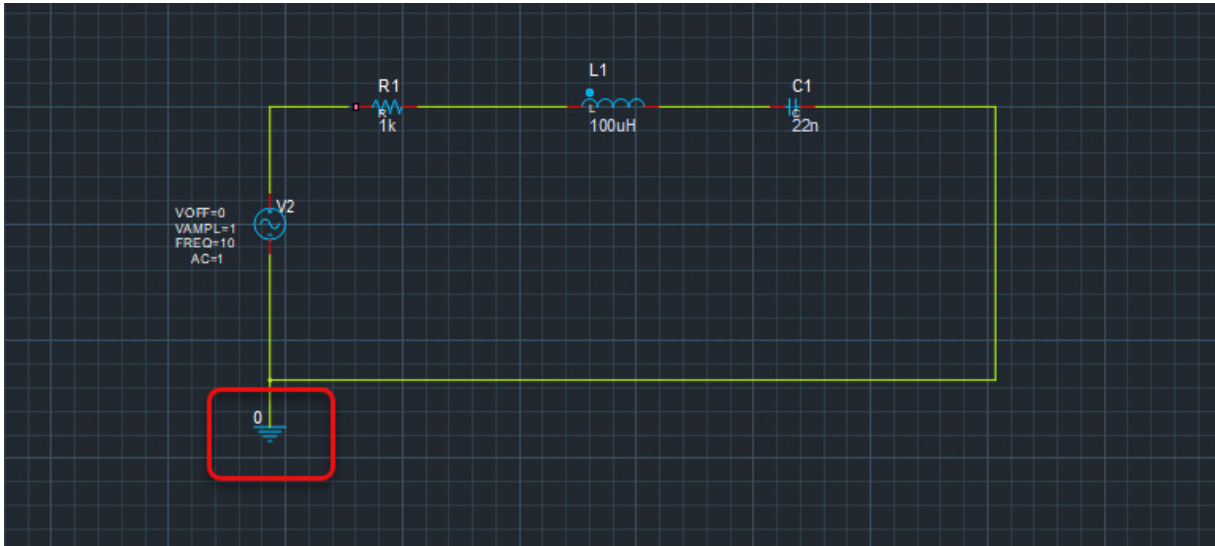
To ensure that schematic designs created in System Capture can be simulated in PSpice, consider the following points:

- To run an analog simulation, the design must have at least one ground symbol.

## PSpice A/D Simulations in Allegro X System Capture

### Simulating System Capture Designs

Use the PSpice ground symbol, '0', instead of GND. In the Unified Search panel, search for 0 and place the ground symbol. By default, this symbol is available in the `source` library.



- To identify unconnected pins in the design, instead of using the *No Connect* symbol, use the PSpice pin property, *FLOAT*. This is required to ensure that the generated PSpice netlist is correct. Valid values for the *FLOAT* property are:

e (Error)	If <i>FLOAT</i> property is set to e or ERROR, the pin is not netlisted. An error message is returned when the PSpice simulation netlist is generated. Use this value when you want to be reminded that this pin is a "no connect" and should be treated in a special way. Error is the default value.
r (RtoGND)	Adds a large virtual resistor to the pin. The second pin of the virtual resistor is grounded by connecting it to 0 symbol in the netlist. The resistor has a value of $1/GMIN$ . With this value, the simulation netlist can be created and PSpice analysis can be run. The virtual resistor is not processed as part of the layout netlist nor listed in the BOM.
n (UniqueNet)	A unique node is attached to the unconnected pin in the generated PSpice simulation netlist. Use this value when you want the pin to remain unconnected but correspond to the Probe data associated with its part.

u (Unmodeled)                      Use of this value is recommended for unmodeled component pins. Unmodeled pins are non-functional for a simulation , and not present in a PSpice template and the model file.

## Creating Parts Based on Model Parameters

If you do not have the required part in an existing library, you can easily create part in System Capture by specifying the values of the electrical parameters from the datasheets to the model definition. Using this approach, you can create parts for the following component models:

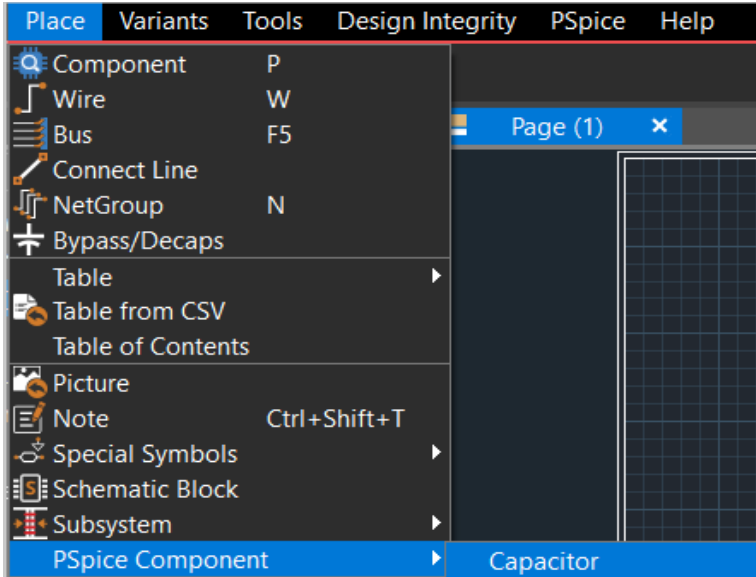
- Capacitor
- Inductor
- Independent Sources
- Power Diode
- Power MOSFET
- Switch
- Transformer
- TVS (Transient-Voltage-Suppression diode)
- VCO (Voltage Controlled Oscillators)
- Zener

## PSpice A/D Simulations in Allegro X System Capture

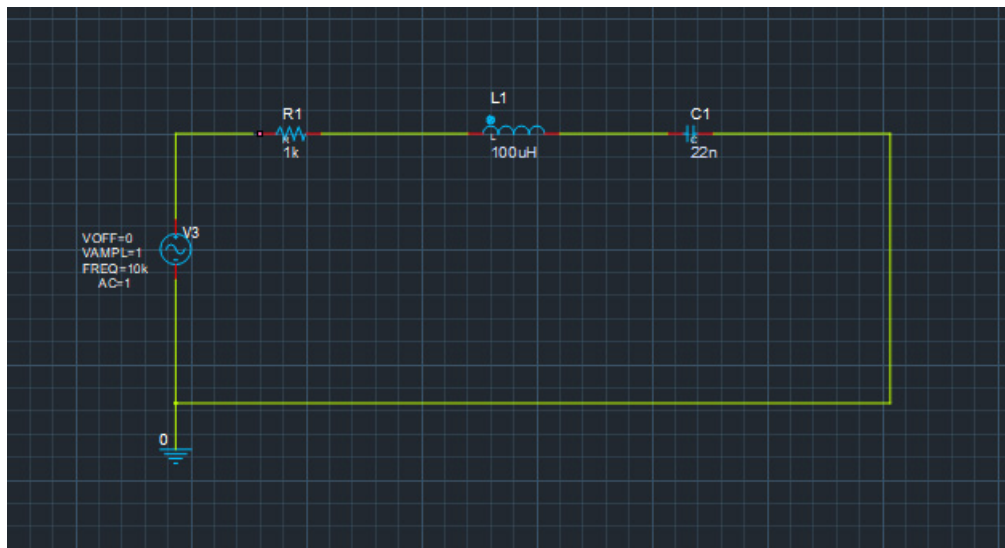
### Simulating System Capture Designs

To model new parts based on electrical parameter values, do the following:

1. Choose *Place – PSpice Component*.



2. From the submenu select the model to create the component.
3. Specify the component parameter values.
4. Place a component instance on the schematic and complete the connectivity.



### Related Topics

- [Connecting Components](#)

## Setting Up Simulation Profiles

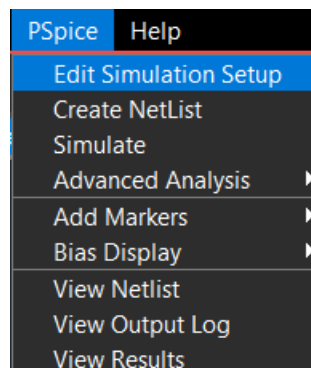
Inputs and instructions to the PSpice simulator are specified using simulation profiles. In a PSpice-enabled project, a default simulation profile is created for the schematic design. You can modify the default profile, or create a new one.

You can create multiple simulation profiles. You can have a different profile for different analysis type. This makes it quick and easy to run different types of analysis on a design.

## Modifying a Simulation Profile

To edit an existing profile, do the following steps:

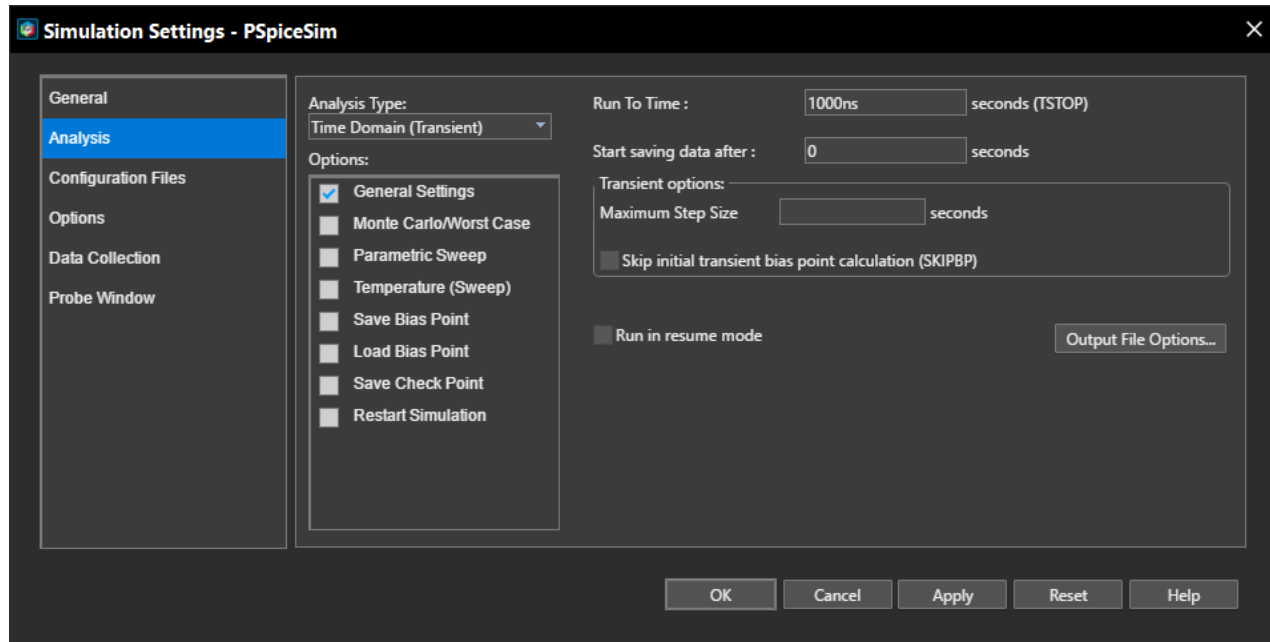
1. Choose *PSpice – Edit Simulation Setup*.



## PSPice A/D Simulations in Allegro X System Capture

### Simulating System Capture Designs

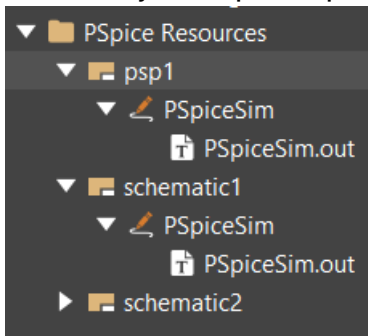
2. In the *Simulation Settings* dialog, modify the simulation parameters as required, and click *OK* to update the profile.



## Creating a New Simulation Profile

To create a new simulation profile, do the following steps:

1. In the Project Explorer panel, open *PSpice Resources*.

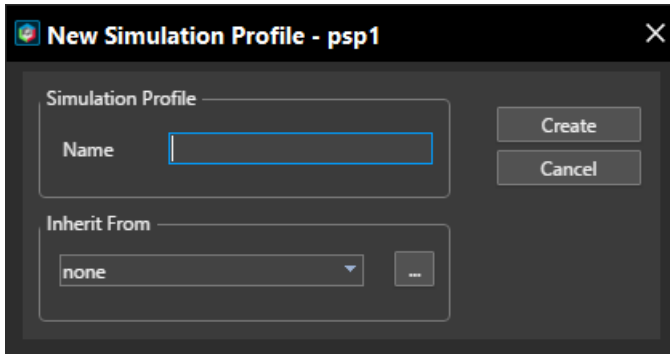


## PSpice A/D Simulations in Allegro X System Capture

### Simulating System Capture Designs

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2. Right-click the project name and choose *New Simulation Profile*.



3. Specify a new profile name and click *Create*.

In the Simulation Settings dialog box is displayed for the new profile.

4. Specify simulation details, such as the analysis type, simulator run time, maximum step size, and so on, and click *OK*.

The new simulation profile is created and set as the current simulation profile.

### ***Related Topics***

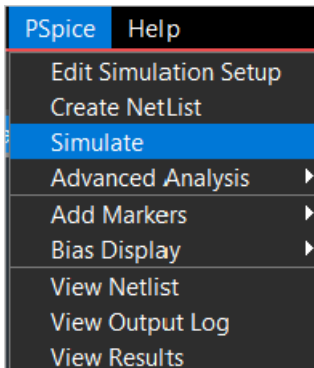
- [Analysis settings for simulation profiles](#)

## Simulating the Design

You can run simulation for the design you created and display the simulation results in the PSpice Simulator Probe window.

To simulate the design, use one of the following methods:

- Choose *PSpice – Simulate*.





## PSpice A/D Simulations in Allegro X System Capture

### Simulating System Capture Designs

- Click *Run Simulation* from the PSpice toolbar.
- Right-click on the simulation profile for the design in the Project Explorer panel and choose *Simulate*.

As the simulation starts, the PSpice Waveform Viewer window is displayed in the background.

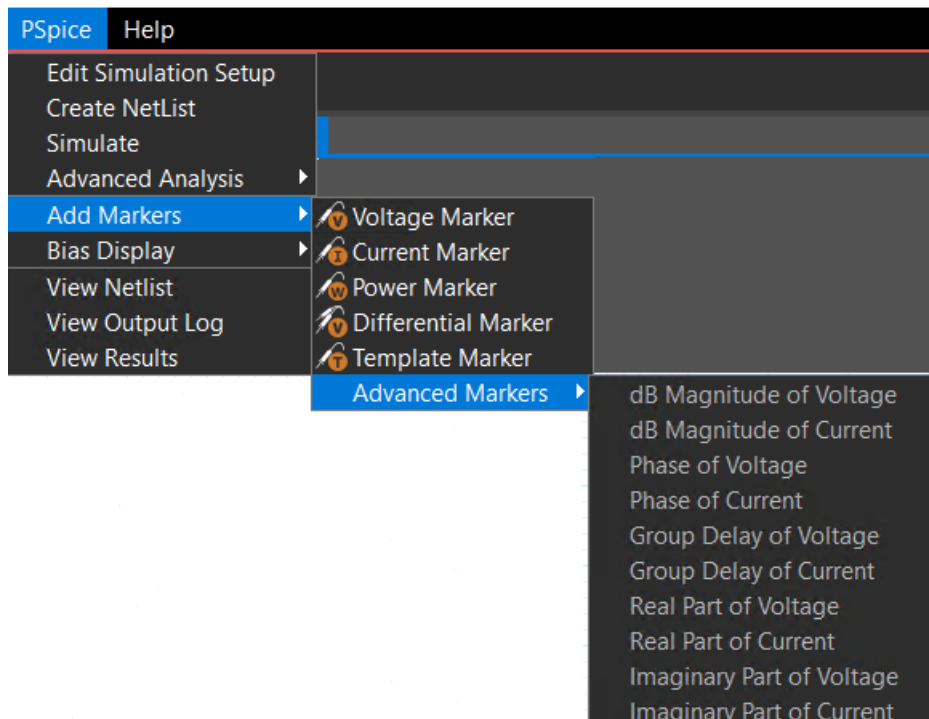
## Viewing Output Waveforms

To display output waveforms in PSpice, you need to place markers in your design to indicate the points where you want to see the output waveforms.

1. From the PSpice toolbar, select the required markers and place them in the design to display traces in the PSpice Waveform Viewer window.



You can also use the *PSpice – Add Markers* menu to add markers.

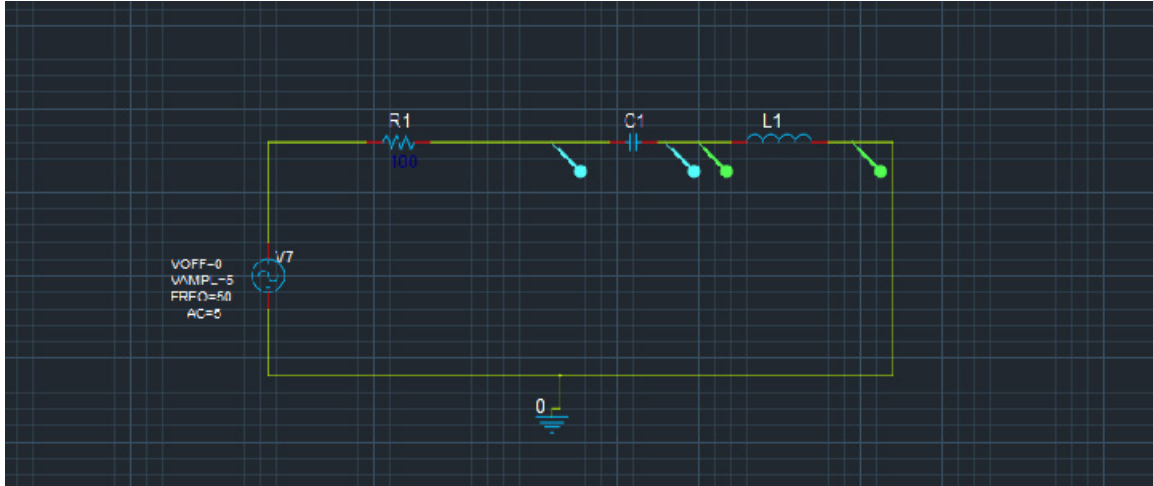


2. Select the marker and place it in the design to display the traces in PSpice Waveform Viewer window.

## PSpice A/D Simulations in Allegro X System Capture

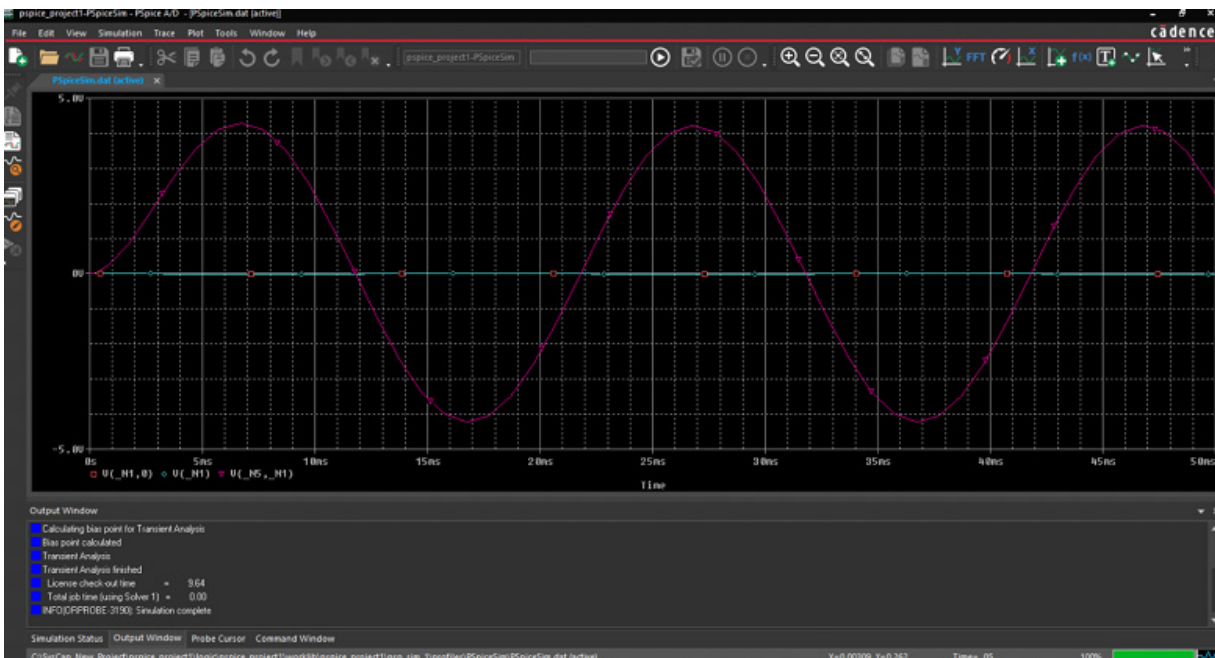
### Simulating System Capture Designs

**Note:** In System Capture, you can place multiple voltage markers on the same net in a same or a different location.



The simulation output is displayed as waveform in the Waveform Viewer window.

3. You can also add Measurements in the Probe window.



### Related Topics

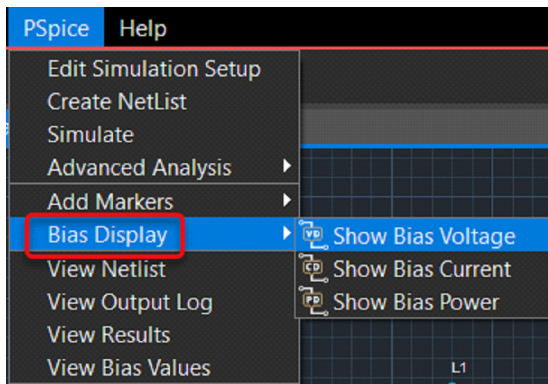
- [Compose Measurements](#)
- [Add Traces](#)

## Enabling Bias Display

After simulating the design, you can display bias point information, such as bias voltage, bias current, and bias power, on your schematic to identify potential problem areas in your design.

To enable bias display in your design, do the following in System Capture:

1. Choose *PSpice – Bias Display*. The available bias display options can be selected from the submenu.

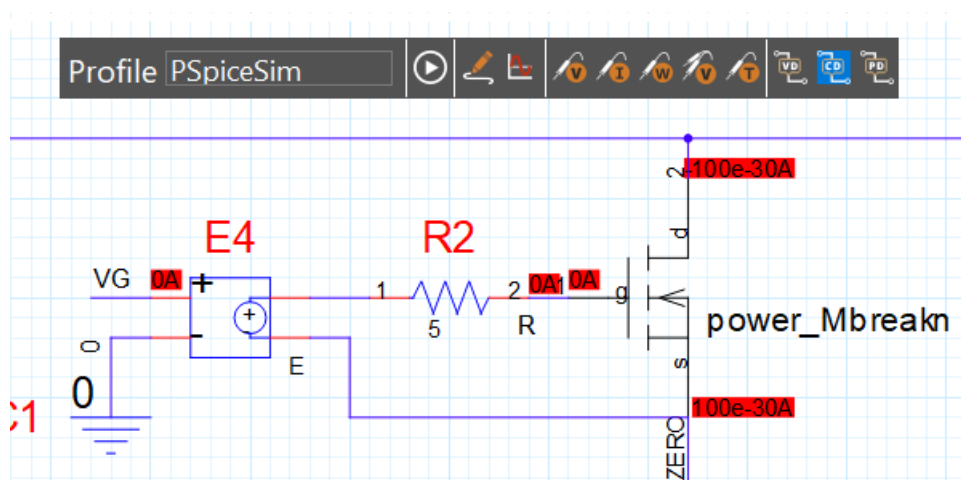


2. Choose the required option to display the corresponding bias point.

Alternatively, use the PSpice toolbar to enable bias point display. Check the Bias displays in the toolbar that are marked as enabled.



Selected bias point data is displayed on the schematic.

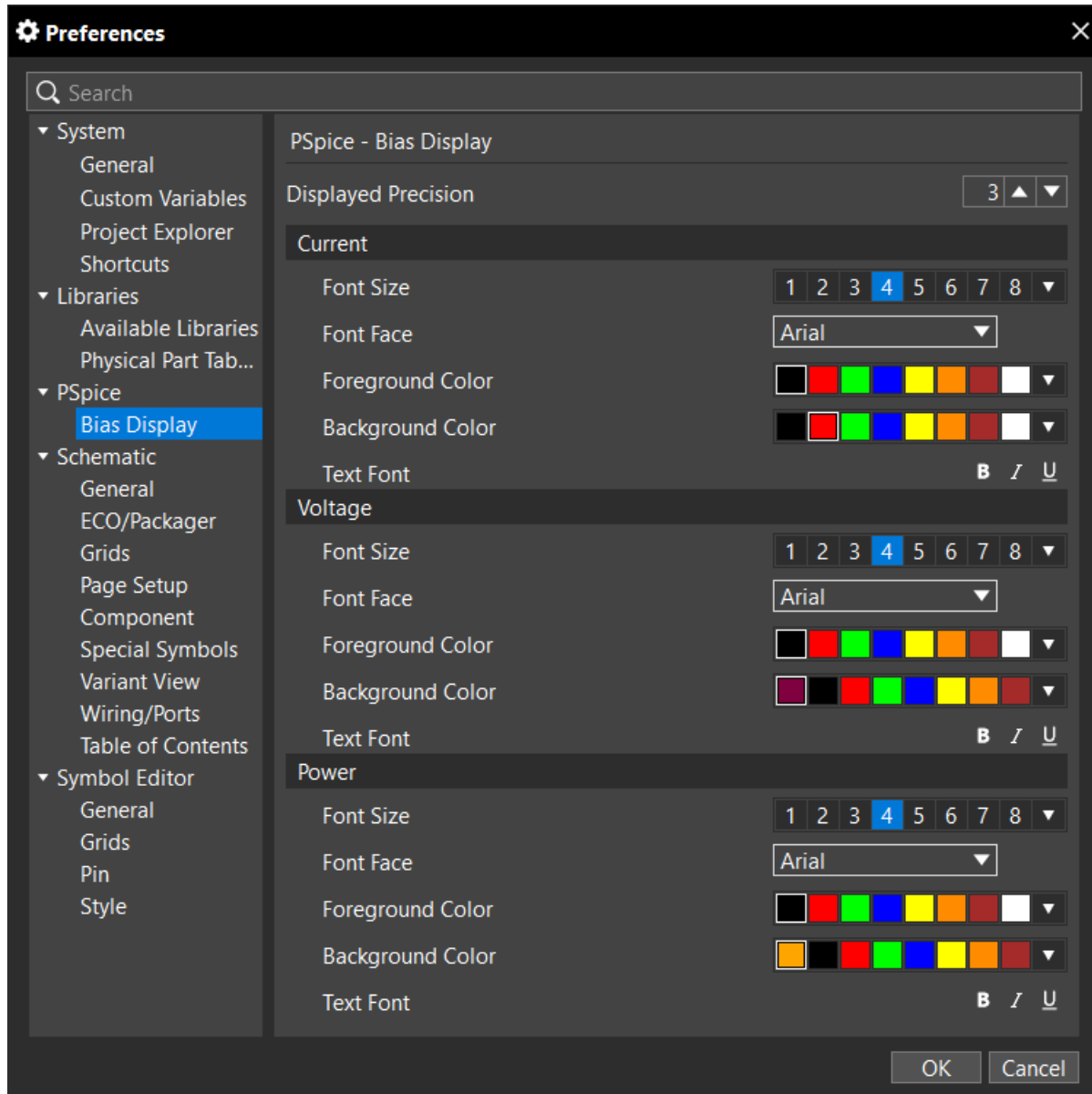


**Note:** Display settings of the bias point data, such as font size and color can be

## PSpice A/D Simulations in Allegro X System Capture

### Simulating System Capture Designs

customized using the Bias Display page of the *Preferences* dialog box.



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## Simulation Models and Stimulus

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To simulate a design in PSpice, the components must have associated electrical models. In addition, inputs to the design, such as power supplies or stimulus for the circuit, also need to be specified.



### *Tip*

When you copy or archive a PSpice-enabled System Capture project, PSpice related information is retained including simulation profiles, marker information, and simulation outputs.

## Associating PSpice Model

If a design component is not a Cadence-supplied PSpice compatible part, it can still be simulated in PSpice after associating a spice model to it.

PSpice supports associating custom or downloaded models to a component symbol on the schematic. To associate a PSpice model to a component instance, do the following steps:

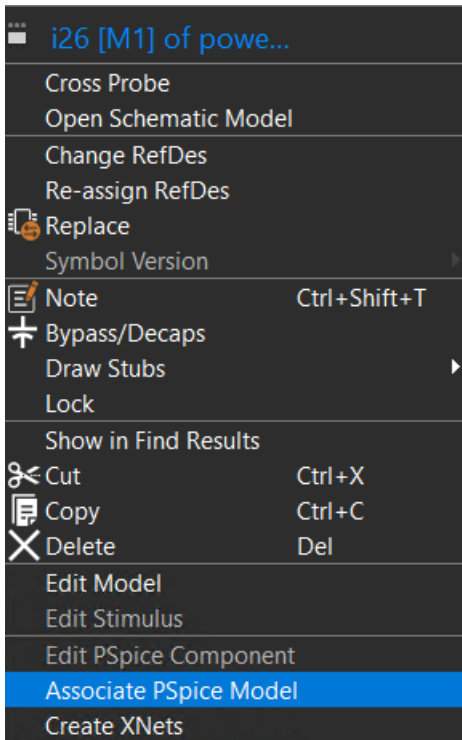
1. Right-click the component.

## PSpice A/D Simulations in Allegro X System Capture

### Simulation Models and Stimulus

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#### 2. Choose *Associate PSpice Model*.



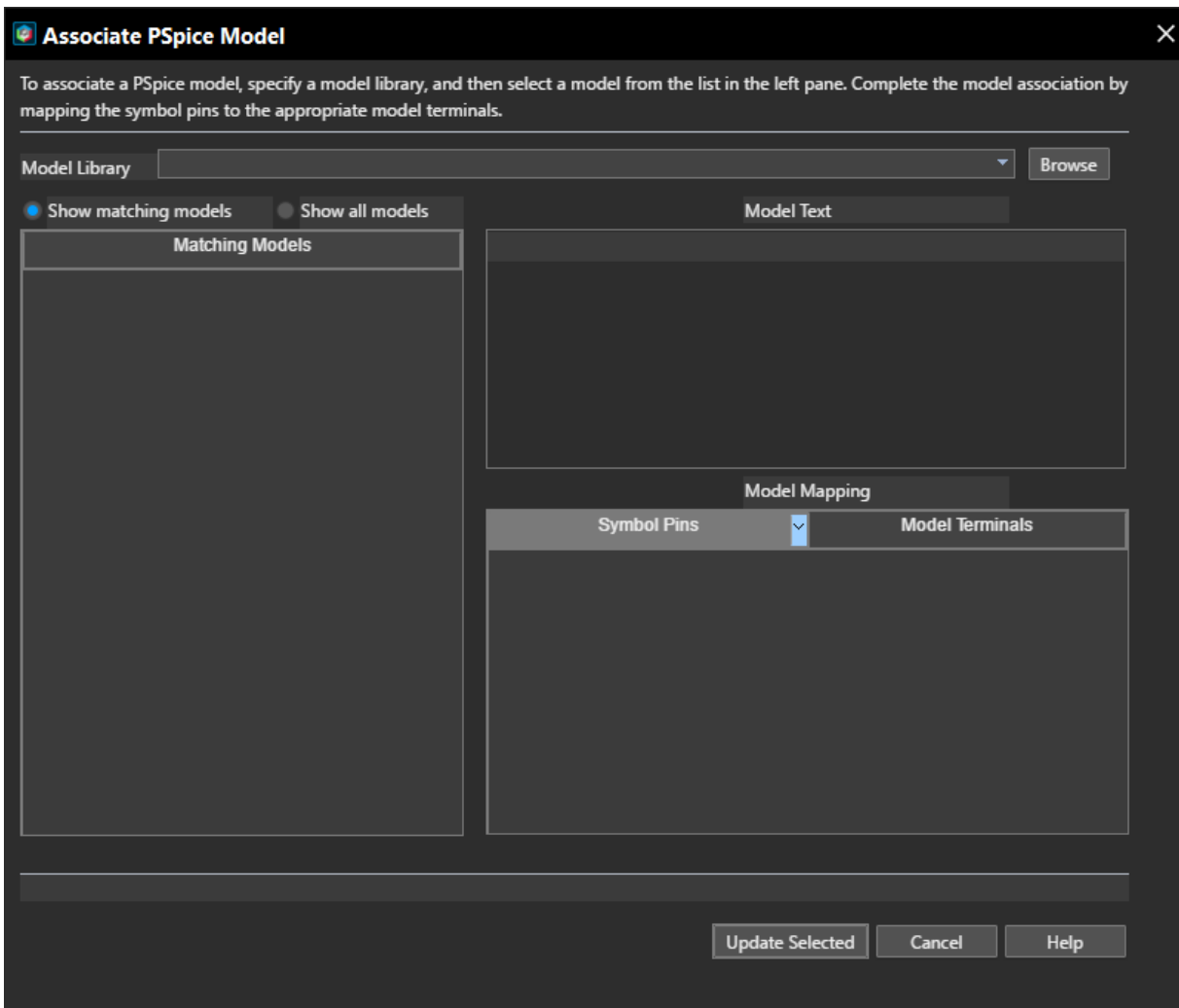
If the selected part already has a PSpice model attached, a message appears to confirm if you want to overwrite this implementation.

#### 3. To proceed, click *Yes*.

## PSPice A/D Simulations in Allegro X System Capture

### Simulation Models and Stimulus

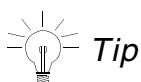
The *Associate PSPice Model* dialog box is displayed.



4. In the Model Library field, specify the location of the library containing the PSPice model to be associated with the component.

The Matching Models section is populated with the list of models that can be associated with the selected component. The Model Text section displays the model definition of the model selected in the list.

5. In the Model Mapping section, map the symbol pins to the correct model terminal. For this, select a port from the *Model Terminal* for each symbol pin.



*Tip*

See the model text to identify the model terminal to be mapped to each symbol pin.

6. Click *Update Selected*.

The instantiated component instance has the PSpice model associated with it.

## Editing Models

You can edit models associated with an instantiated component. To modify the model parameter values of a placed component, do the following steps:

1. Right-click the component and choose *Edit Model*.

Model definition opens in Model Editor.

2. Modify the parameter values or add new parameter, as required.
3. Save the changes.

## Adding Circuit Stimulus

To run analysis on your design, you need to add stimuli defining inputs for the circuit. For this, you can instantiate parts from the Cadence-supplied libraries, *sourcestm* and *source*. Depending on the part used, stimulus information is added either as part property, or attached as a stimulus file, or specified using Stimulus Editor.

For example, if you use parts *STIM1*, *STIM4*, *STIM8*, or *STIM16* from the *source* library, stimulus information is specified as part property.

Parts, such as *VPWL\_F\_RE\_FOREVER*, *IPWL\_F\_RE\_FOREVER*, *VPWL\_F\_N\_TIMES*, and *IPWL\_F\_N\_TIMES*, use file-based stimulus. The stimulus information specified using PSpice netlist syntax is saved in a file attached to the part.

For parts such as *VSTIM* and *ISTIM*, stimulus information is specified using Stimulus Editor.

## Using Stimulus Editor

The *VSTIM* and *ISTIM* parts are used to define time-based input signals. Parts such as *DIGSTIMn* are used to specify digital stimulus to a circuit. When using these components, stimulus information is specified using Stimulus Editor.



### Tip

The value of the *STIMTYPE* property indicates if the stimulus is analog or digital.

To add stimulus to a circuit, do the following steps:

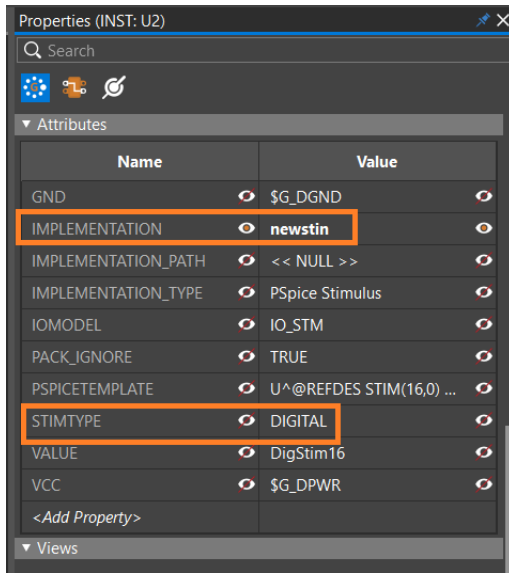


## PSpice A/D Simulations in Allegro X System Capture

### Simulation Models and Stimulus

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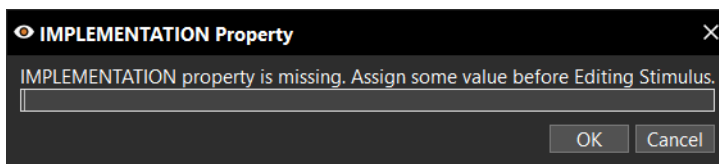
1. Place a stimulus part on the schematic.
2. For the part, specify the value of the *IMPLEMENTATION* property in the *Attributes* section of the *Properties* panel.



This value is used as the stimulus name.

3. Right-click the placed part and choose *Edit Stimulus*.

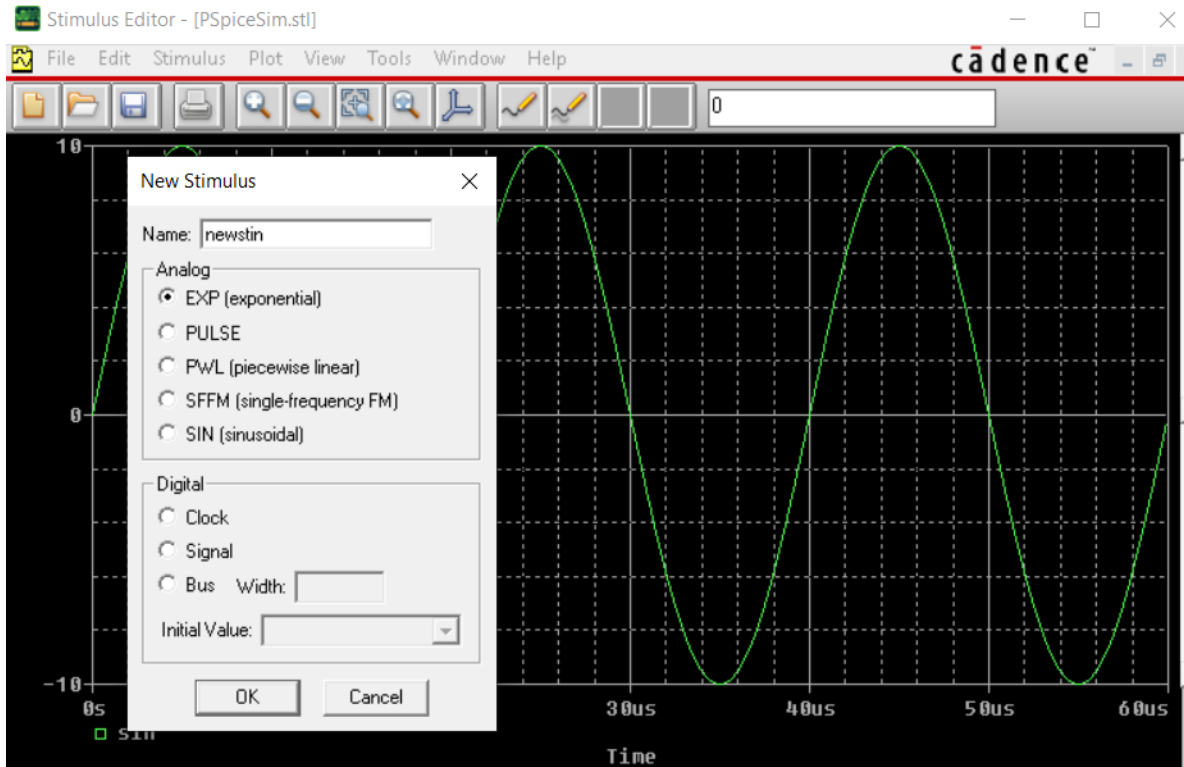
**Note:** If the *IMPLEMENTATION* property is not specified, the following dialog is displayed on selecting *Edit Stimulus*.



## PSpice A/D Simulations in Allegro X System Capture

### Simulation Models and Stimulus

The Stimulus Editor window opens and the *New Stimulus* dialog box is displayed.



4. Select the stimulus type and specify details in the subsequent dialog boxes.

Depending on the stimulus details you specify, a stimulus waveform is displayed in the Stimulus Editor window.

5. Save the waveform.

A message box prompts you to update the schematic.

6. Click Yes, to update the schematic with the stimulus information.

## Creating Custom Digital Power Supplies

Digital power supplies are required if a design contains digital power and ground nodes. To define a custom digital power supply for the schematic, use parts from the *special* library. The following customizable digital power supply parts are available in this library:

- ❑ CD4000\_PWR
- ❑ DIGIFPWR (TTL power supply)

## PSpice A/D Simulations in Allegro X System Capture

### Simulation Models and Stimulus

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- ☐ ECL\_10K\_PWR
- ☐ ECL\_100K\_PWR

To create a custom digital power supply, do the following steps.

1. Place the required power supply part in your design.
2. To specify power and ground voltages, assign values to the PWR and GND component properties, respectively.

Name		Value	
AGND		0	
GND		<Gnd_Node>	
GND_REF		0V	
IMPLEMENTATION		DIGIFPWR	
IMPLEMENTATION_PATH		<< NULL >>	
IMPLEMENTATION_TYPE		PSpice Model	
PACK_IGNORE		TRUE	
PSPICEONLY		TRUE	
PSPICETEMPLATE		X^@REFDES %AGND %P...	
PWR		<Pwr_Node>	
VALUE		DIGIFPWR	

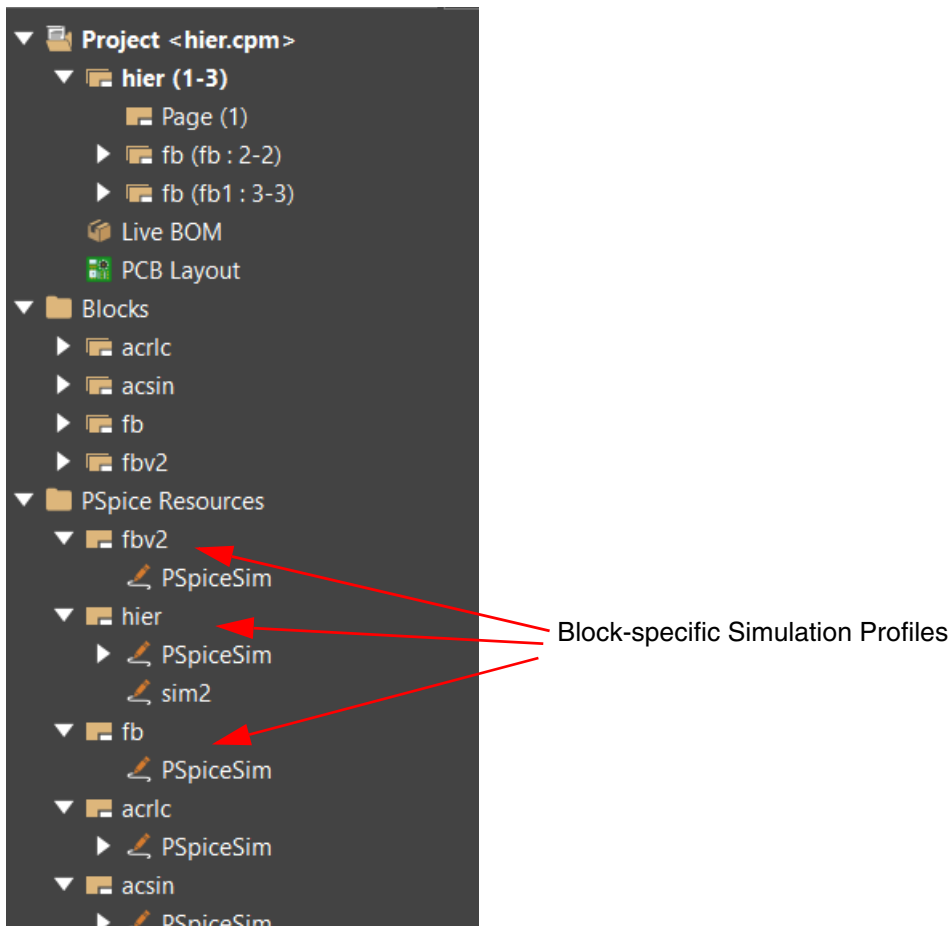
## **PSpice A/D Simulations in Allegro X System Capture**

### **Simulation Models and Stimulus**

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## Simulating Hierarchical Design

The hierarchical designs created in System Capture can be simulated using PSpice. On creating a hierarchical schematic in PSpice-enabled System Capture, a new simulation profile is created for each schematic block. Using the block-specific simulation profile, each block can be simulated independently in PSpice A/D.

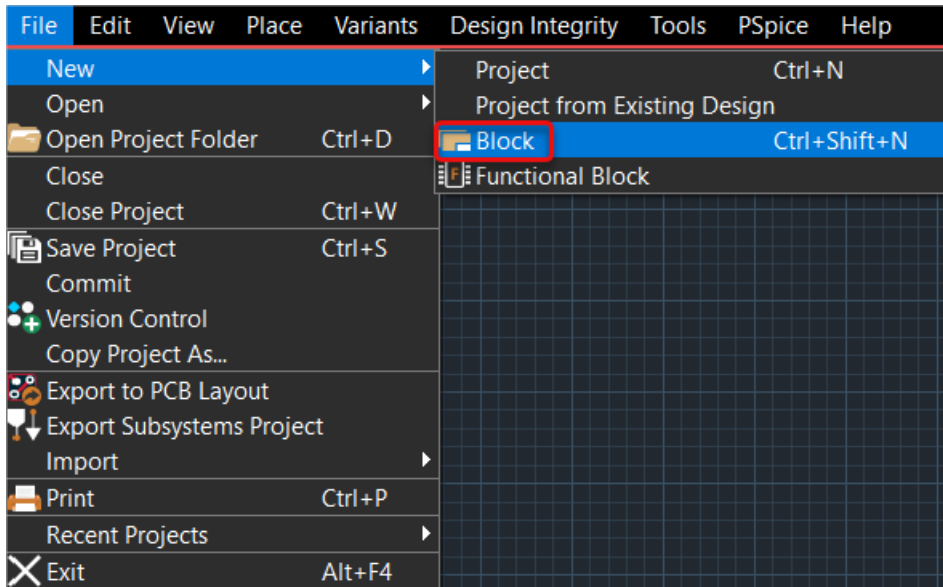


For simulating the complete design, the simulation profile of the root design is used.

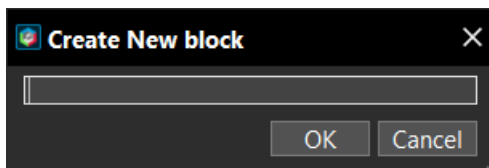
## Simulating a Block Schematic

To create and simulate a block in System Capture, do the following steps:

1. Choose *File – New – Block*.



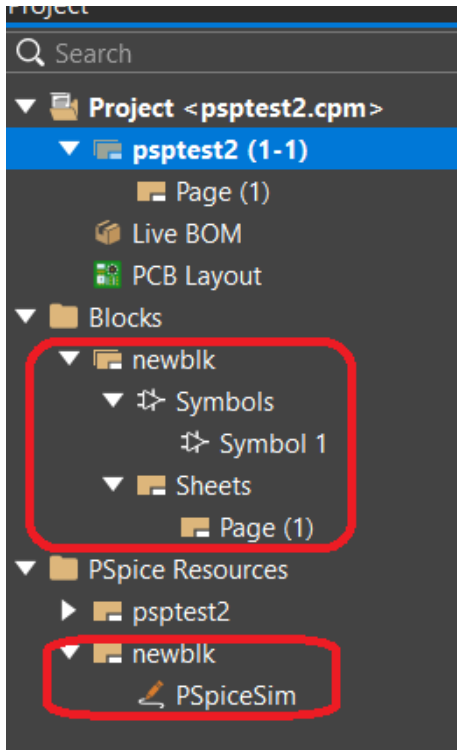
2. In the *Create New block* dialog box, specify the new block name and click *OK*.



## PSPice A/D Simulations in Allegro X System Capture

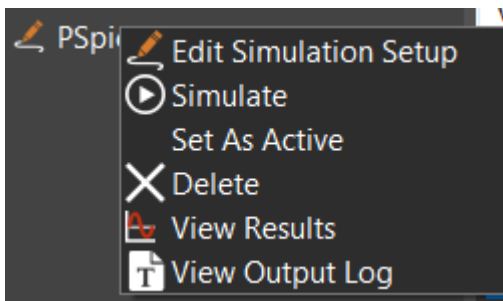
### Simulating Hierarchical Design

A new block is created under the *Blocks* node with a blank schematic page and a zero-pin symbol. A default simulation profile is also created and is visible under the *PSPice Resources* node.



#### Block-specific Simulation

3. Create the block schematic and update the simulation profile as required.
4. To simulate the block, right-click the simulation profile for the block under the PSPice Resources node, and choose *Simulate*.

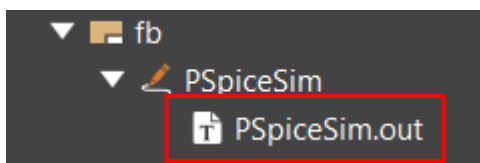




#### Tip

If the shortcut menu commands appear disabled, the block symbol might be open for editing. Close the symbol view to enable the block simulation commands. Alternatively, open the block schematic, and click the *Simulate* icon from the PSpice toolbar on the schematic page.

When the simulation completes, the simulation output file for the block is also listed under the *PSpice Resources* node.

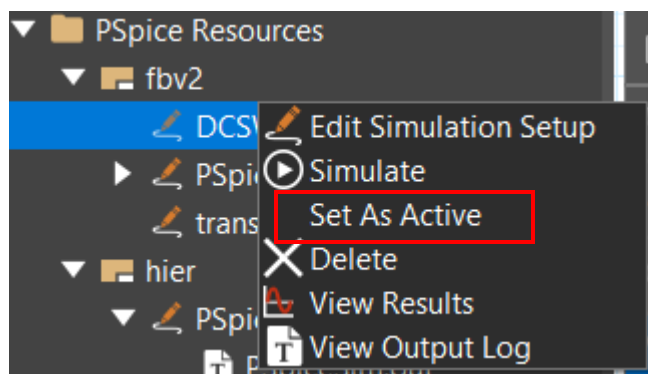


## Using Alternate Simulation Profiles

When you create a block, a new simulation profile, *PSpiceSim*, is created by default for each schematic block. This default profile is displayed under the block name in the *PSpice Resources* node, and the PSpice toolbar. When you simulate the design from the *PSpice – Simulate* menu, or by clicking the *Simulate* icon, the default simulation profile is used.

Alternate simulation profiles created for a block are also listed under the block name in the *PSpice Resources* node. To simulate a block design using an alternate profile, use one of the following methods:

- Right-click the profile name to be used, and choose *Simulate*.
- Modify the default profile, and simulate. For this, do the following:
  - a. Right-click the profile name to be used and choose *Set As Active*.





## PSpice A/D Simulations in Allegro X System Capture

### Simulating Hierarchical Design

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The active simulation profile name is reflected in the PSpice toolbar for the block schematic.



- b.** To simulate the block schematic, click the Simulate button (▶) from the PSpice toolbar.

After a profile is set as the active simulation profile, it becomes the default profile for subsequent simulations of that schematic.



#### *Tip*

Schematic blocks can be used for creating and simulating different versions of a schematic. To do this, open the new page of a block and copy an existing schematic. You can create variations by adding a new component, replacing an existing component, or by modifying component parameters.

## **PSpice A/D Simulations in Allegro X System Capture**

### **Simulating Hierarchical Design**

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## Running Analysis

With PSpice integration you can run Advanced Analysis tools on your System Capture design. PSpice Advanced Analysis includes Sensitivity analysis, Optimizer runs, Monte Carlo analysis, Smoke analysis, and Parametric Plotter.

### Parametric Sweep

Parametric Sweep is a multi-run simulation analysis where circuit behavior is tested by varying the specified parameter values. Parametric Sweep is available with AC Sweep, DC Sweep, and Transient analysis.

To run a Parametric Sweep analysis, do the following tasks:

1. Add the component for which parameter values are to be changed.
  - a. Using the Unified Search panel, place an instance of the *param* component from the *special* library on the schematic.

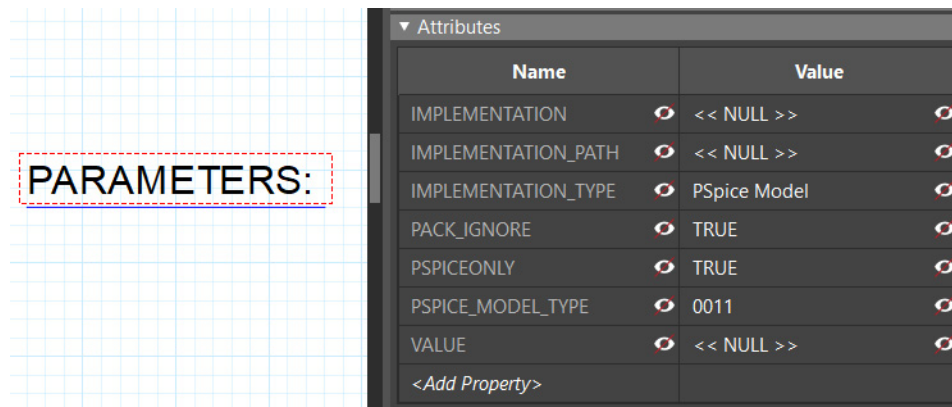
Library (4)    My Parts    SamacSys (18)				
CLASSIFICATION				
param				
PART NUMBER	CLASSIFICATION	SUMMARY	FOOTPRINT	LIBRARY
param	PARAM			special

## PSpice A/D Simulations in Allegro X System Capture

### Running Analysis

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- b. Select the instances and in the Attributes section click *<Add Property>*.



- c. Add the name and the value of the parameter to be modified.

### 2. Specify the simulation settings.

- From the PSpice toolbar, select the *Edit Simulation Setup* icon.
- Select the *Parametric Sweep* check box.
- In the Sweep Variable section, select the *Global Parameter* option.
- In the Parameter name field, specify the parameter name entered in the param component instance ( step c of 1).
- In the Sweep Type section, select the option to indicate how parameter values are to be modified.
- For the selected Sweep type, specify the required field values.
- Click OK to save the changes to the simulation profile.

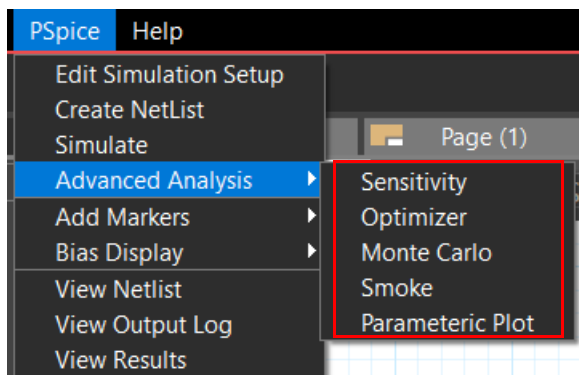
### 3. Run the simulation.

After the simulation run completes, place the required markers on the schematic to view the output waveform.

## Advanced Analysis

Besides the Transient, AC and DC Sweep analysis, you can also run PSpice Advanced Analysis simulations to optimize your designs, improve design reliability and yield, to reduce overall cost. These Advanced Analysis checks examine the circuit performance against specified goals defined through various measurement expressions created for the design.

- ➔ To run Advanced Analysis checks on a System Capture design, choose *PSpice – Advanced Analysis*.



From the submenu, choose the analysis to be run.

### Advance Analysis Options

Option	Function
<u>Sensitivity</u>	Identifies key components that impact the design performance
<u>Optimizer</u>	Calculates optimum component values
<u>Monte Carlo</u>	Predicts production yield
<u>Smoke</u>	Identifies components most likely to fail in the PCB
<u>Parametric Plotter</u>	Records circuit behavior within the tolerance range

### Related Topics

- [Measurement Expressions](#)

## **PSpice A/D Simulations in Allegro X System Capture**

### **Running Analysis**

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