cadence®

OrCAD X Capture with PCB Editor Tutorial

Product Version 23.1
September 2023

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Contents

1

Tutorial Overview

This tutorial enables you to evaluate the power of the OrCAD X tools for the PCB design process. You can run through the steps to perform the basic tasks in the PCB design process in sequence.

You will start with capturing the circuit diagram in Capture, followed by circuit simulation using PSpice, through to the PCB layout stages, and finally, complete the design cycle by generating the manufacturing output.

This document does not cover all the features of a tool. It only highlights the tasks that you need to perform in each OrCAD X tool so that your design works smoothly through the flow.

Audience

This tutorial is useful for:

- Designers who want to use OrCAD X tools for the complete PCB design flow or for analog and digital simulation flow.
- First-time users of OrCAD X Capture, PSpice, and PCB Editor.

Using the tutorial

To run through the complete tutorial, you need the following tools:

- OrCAD X Capture CIS
- PSpice AD
- PCB Editor

All these tools are available with the `OrCAD X Standard` and `OrCAD X Professional` licenses.

Sample Design

The design created by the end of this tutorial is available at the following location:

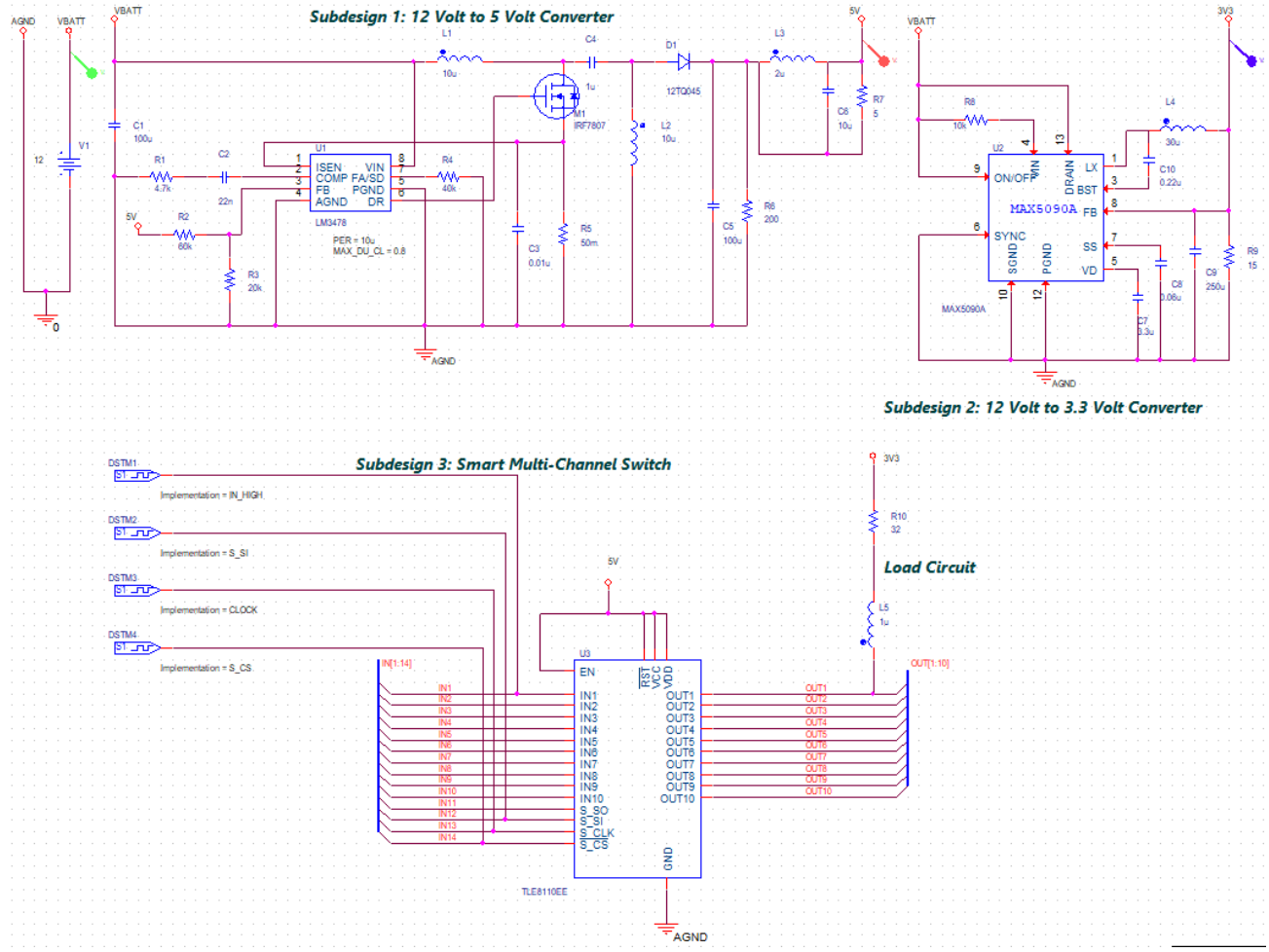
<installation_directory>\share\orcad\tutorial\tutorial.opj

2

Creating a Schematic Design

In this section, you will create a schematic design for a fan-control module with three subdesigns as illustrated in the following figure:

Schematic design for the complete fan-control module



The following table provides a brief description of the function of each subdesign:

Subdesigns in the fan module circuit

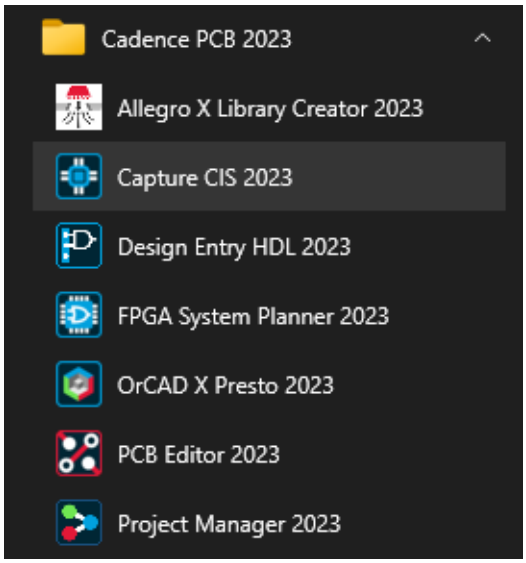
Subdesign	Function
Subdesign 1	A step-down DC-DC converter. It uses `IC LM3478`, a low-side n-channel `MOSFET` controller for switching regulators, which converts `12 volt` to `5 volt`. The output of `5 volts` is the internal power supply for this circuit. It provides supply voltage to `IC TLE8110EE` (in subdesign 3).
Subdesign 2	A step-down DC-DC converter that uses the IC MAX5090A to convert `12 volt` to `3.3 volt`.
Subdesign 3	A smart multi-channel switch, TLE8110EE powered by a `5 volt` supply. This switching of `IC`, `TLE8110EE` can control multiple load types (fan load in this tutorial). It has `10` input channels and a serial peripheral interface (SPI). It has `10` output pins, which can control up to `10` fans.

Creating a New Project

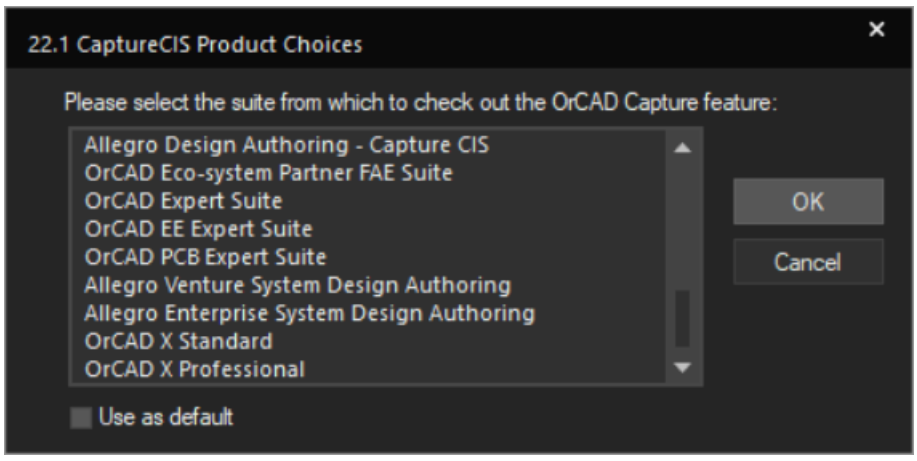
A project file (`.OPJ`) is a container for the design file (`.DSN`). In addition, a project file also includes simulation profile and layout information.

To create a new project, do the following:

1. From the Start menu, select *Capture CIS 2023*.



The *23.1 CaptureCIS Product Choices* dialog box opens.



2. Select `OrCAD X Professional` and click *OK*.

The OrCAD X Capture CIS window opens. When you open Capture with an OrCAD X license, you are prompted to provide your login credentials to access OrCAD X-enabled features.

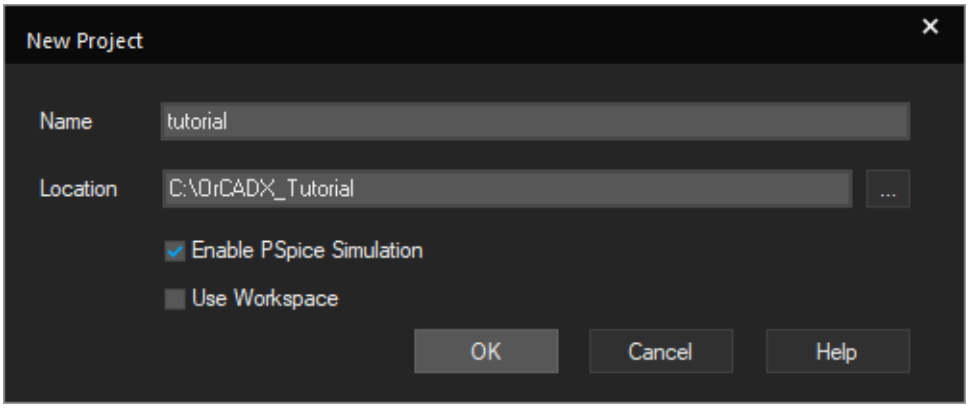
Note: This step is not mandatory for the purpose of this tutorial. You can skip this step by closing the login window and moving to the next step.

To learn about OrCAD X Capture CIS part authoring capability, see OrCAD X Part Authoring Tutorial.

3. Choose *File – New – Project*.
4. In the *New Project* dialog box, specify the project name as `tutorial`.

   At the time of creating a new project, you can decide if you want to store the project in the OrCAD X Cloud workspace. If you select the *Use Workspace* option in the *New Project* dialog box, the Cloud workspace location is pre-seeded and cannot be changed later:

   `%HOME%\cdssetup\workspace\`
5. For the purpose of this tutorial, deselect the *Use Workspace* option.
6. Specify the location as: `C:\OrCADX_Tutorial`.

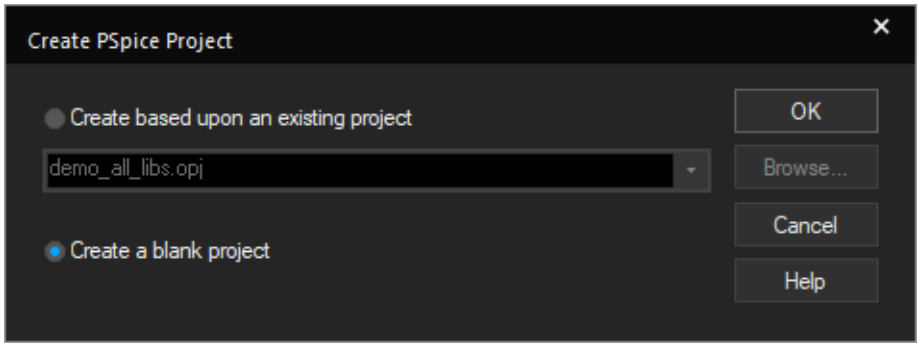


The *Enable PSpice Simulation* option is selected by default.

7. Click *OK*.

   The *Create PSpice Project* dialog box opens.

8. Select *Create a blank project*.

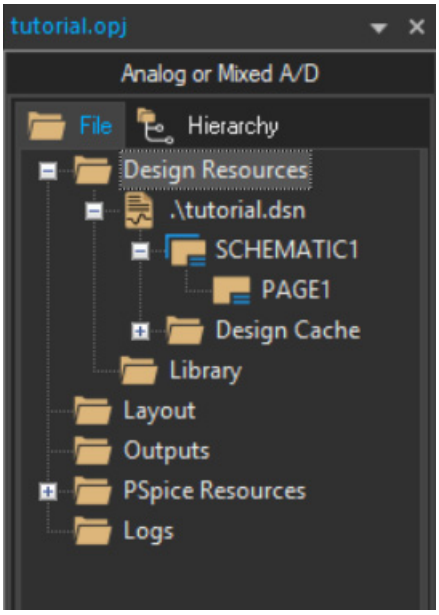


When you create a blank project, the project can be simulated in PSpice, but libraries are not configured by default. When you base your project on an existing project, the new project has the same configured libraries.

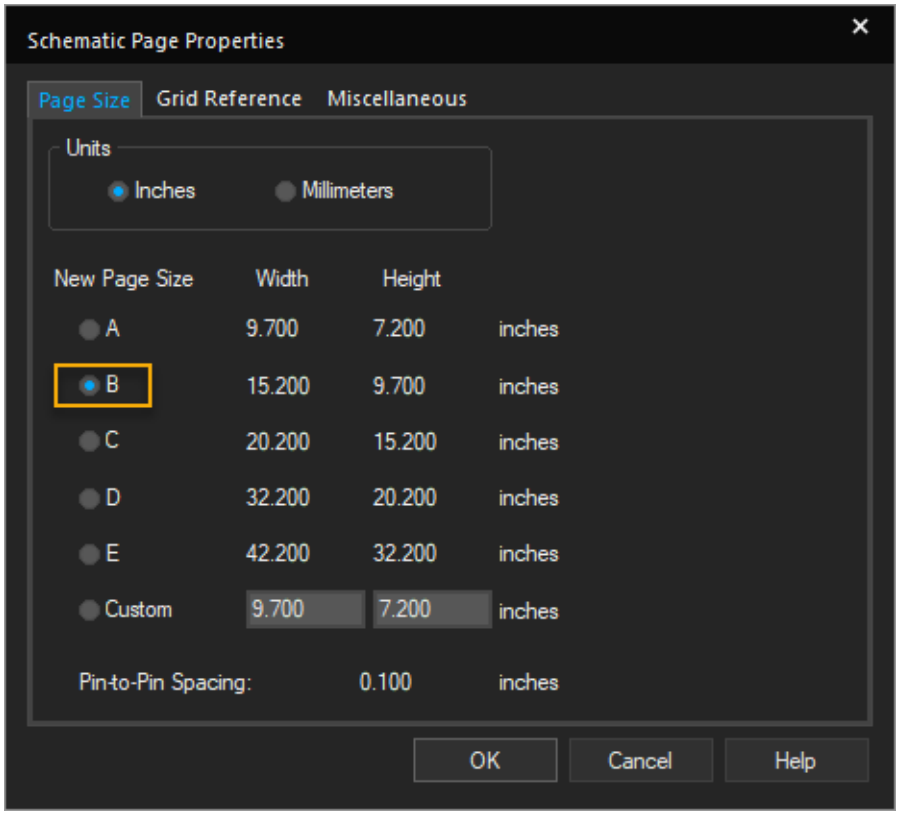
9. Click *OK*.

The `tutorial` project is created. In the project manager window, a design file, `tutorial.dsn`, is created. Under the design file, a schematic folder with the name `SCHEMATIC1` is created. This folder contains a schematic page named `PAGE1`.

Project Manager Window



10. Choose *Options – Schematic Page Properties*, and select the page size as `B`.



11. Click *OK*.

Creating Design in Capture

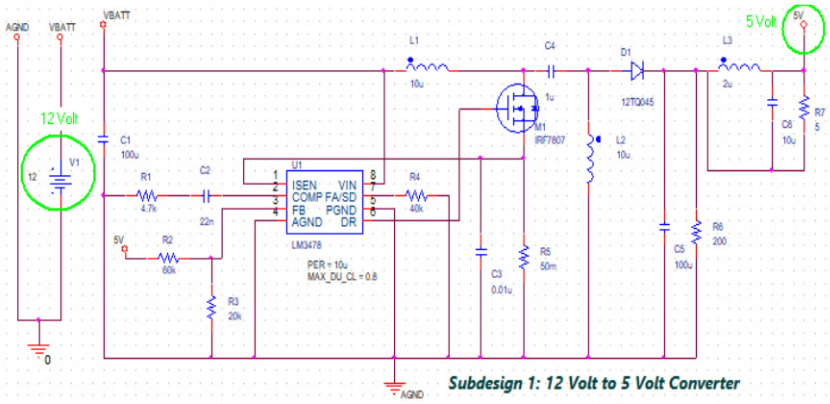
You will now create the three subdesigns of the fan module.

Subdesign No.	Instructions for subdesign creation are in the section...
1	Subdesign 1: 12 Volt to 5 Volt Converter
2	Adding Subdesign 2: 12 Volt to 3.3 Volt Converter
3	Subdesign 3: Smart Multi-Channel Switch Circuit

Subdesign 1: 12 Volt to 5 Volt Converter

Subdesign 1 consists of two parts, a `12 volt` main power supply and a `12 volt` to `5 volt` converter as illustrated in the following image:

Subdesign 1: Main power supply and 12V to 5V converter



Part 1: Creating Subdesign 1A

To create the subdesign for the main power supply, you must place the components listed in the following table:

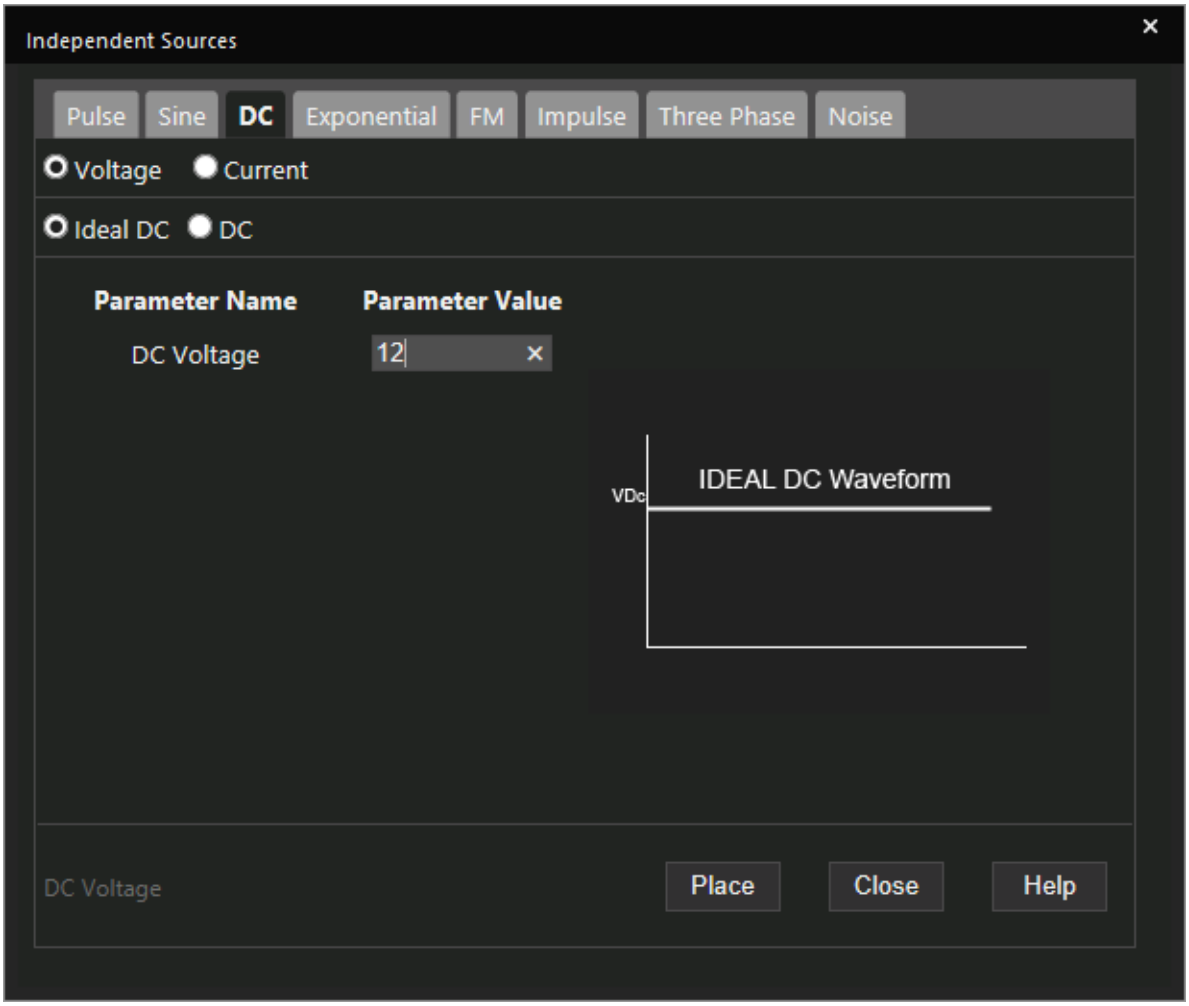
Component	Source
DC voltage source (V1)	Place – PSpice Part – Modeling Application
Ground symbols	Place – PSpice Part – PSpice Ground
Power ports	Place – Power

Placing Components for Subdesign 1A

1. To instantiate an ideal DC voltage source on the schematic page(SCHEMATIC1:PAGE1), choose *Place – PSpice Part – Modeling Application*.
   Alternatively, click the *Modeling Application* icon () on the PSpice toolbar.

   The *Modeling Application* pane opens.
2. Select *Sources – Independent Sources*.
3. Click *DC*.
4. Select *Voltage* and *Ideal DC*.

5. Specify the value of DC Voltage as `12`.



6. Click *Place*.

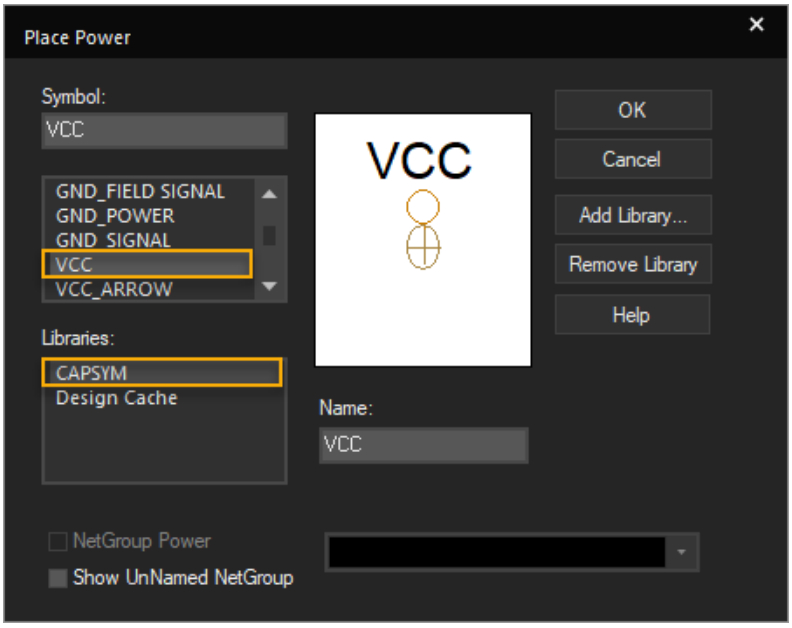
   The PSpice component is attached to the cursor.

7. Click to place the component on the schematic.
8. To place a ground symbol, choose *Place – PSpice Part – PSpice Ground*.
9. Click on the schematic page to place the part.
10. Right-click and select *End Mode* or press *Esc*.

Next, you need to place a power port, `VCC` with its value set to `VBATT`, and another one with its value set to `AGND` from the `CAPSYM` library.

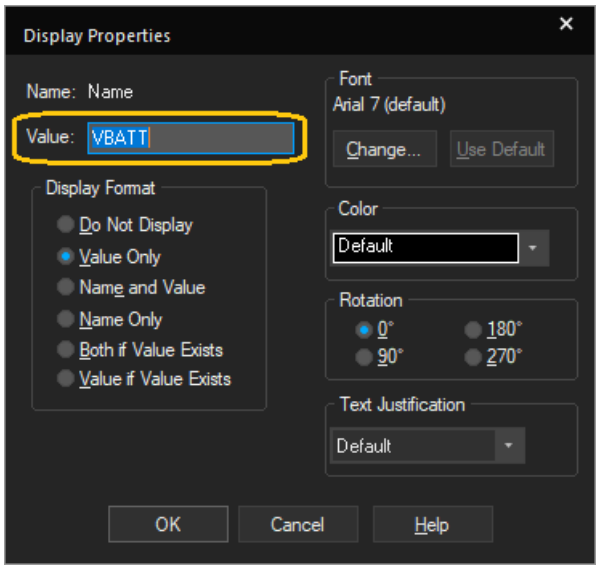
To place power components, do the following:

1. Choose *Place – Power*. Alternatively, press *f* or click the *Place power (F)* icon ( ) on the *Draw Electrical* toolbar.
2. Select `CAPSYM` from the *Libraries* list box.
3. Select `VCC` from the *Symbol* list box.



4. Click *OK*.
5. Click the schematic page to place this power port above the `12 volt` DC source.
6. Press `Esc`.
7. Double-click `VCC` to open the *Display Properties* dialog box.

8. Specify `VBATT` in the *Value* fields and click *OK*.



9. Repeat steps 1 through 7 to add another power port, `VCC`, and set its value to `AGND`.

Connecting the Components

1. Choose *Place – Wire*. Alternatively, press *w* or click the *Place wire* icon () on the *Draw Electrical* toolbar.

   The cursor shape changes from pointer to cross-hair.

2. Draw the wire from the connection points of port `AGND`, `PSpice ground`, `12 volt` DC voltage source, to the `VBATT` port as illustrated in the figure, Subdesigns in the fan module circuit.

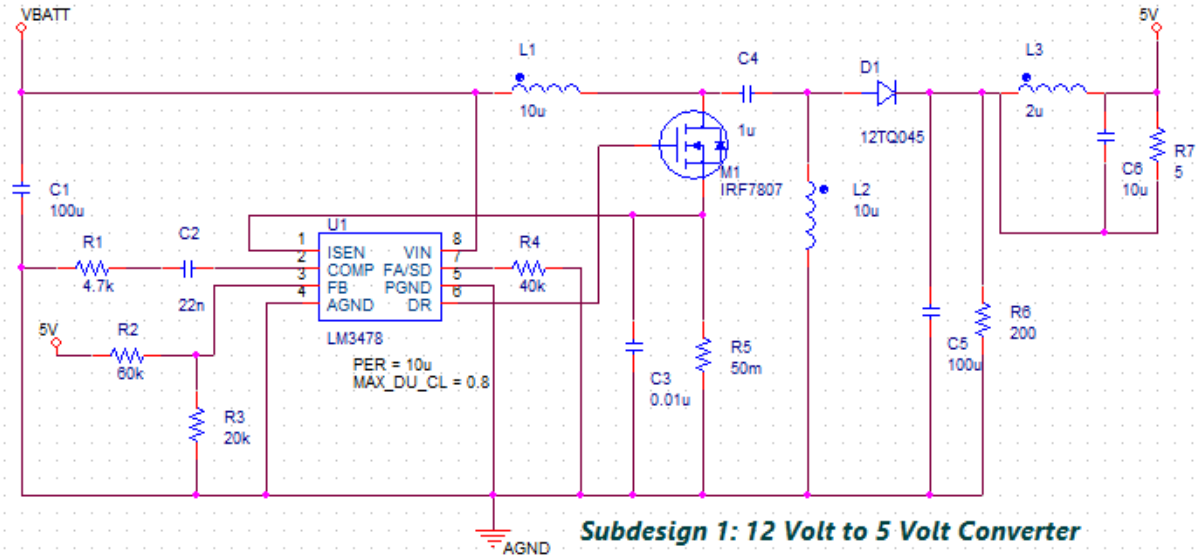
Part 2: Creating Subdesign 1B

To create the subdesign for the main power supply, you must place the components listed in the following table:

Component	Source
`DC-DC converter IC LM3478`	`Place – Component – Component Explorer`

Component	Source
MOSFET IRF7807	Place – Component – Component Explorer
Power ports	Place – Power
Discrete components: Capacitor, Inductor, and Resistor	Place – PSpice Part

Subdesign 1B: 12V to 5V Converter

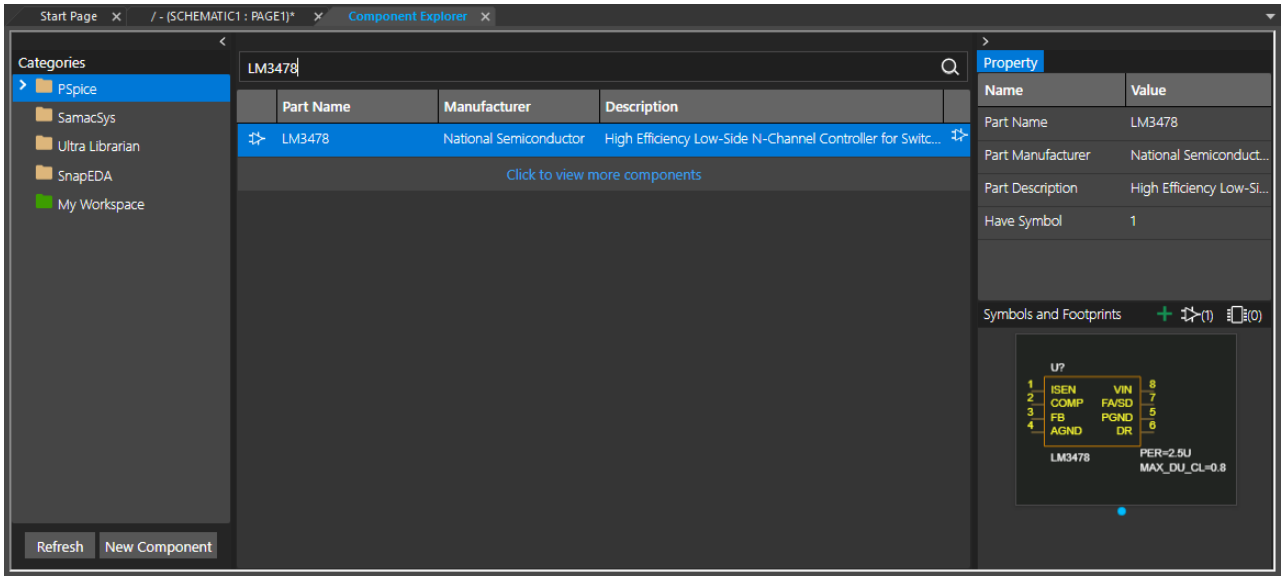


Placing Components for Subdesign 1B

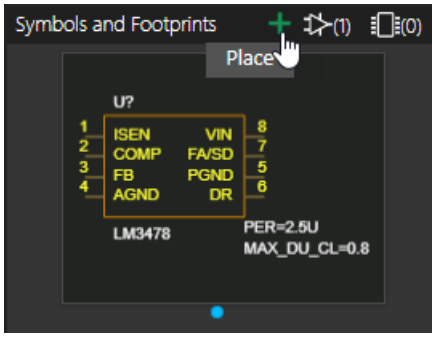
1. To place the DC-DC converter IC `LM3478`, choose *Place – Component.*

   The *Component Explorer* interface opens. By default, the Cadence-supplied library, *PSpice*, is displayed.

2. Specify `LM3478` in the *Search here* text box and press *Enter* or click the magnifying lens icon.



3. Double-click `LM3478` in the search results. Alternatively, right-click `LM3478` in the search results and choose *Place*.
   You can also click the *Place* icon in the *Symbols and Footprints* bar in the right pane.



4. Click the schematic page to place the converter IC.
5. Right-click and select *End Mode* or press `Esc`.
6. Double-click `PER` and set its value to `10u` in the *Display Properties* dialog box.

   This value sets the frequency of the IC. Changing the value to `10u` (`1/10u = 100KHz`) sets the IC frequency to `100 KHz`.
7. Follow steps 2-5 to place the MOSFET, `IRF7807`.
8. Place the `VBATT` and the two `5V` power ports shown in subdesign 1.

Placing Discrete Components

To place the commonly used discrete components, capacitor, inductor, and resistor, do the following:

1. Choose *Place – PSpice Part –*
   - ❑ *Capacitor* to place a capacitor.
   - ❑ *Inductor* to place an inductor.
   - ❑ *Resistor* to place a resistor.
2. Click the schematic page to place each component and press `Esc` when done.
3. To change the value of discrete components:
   a. Double-click their value to open *Display Properties* window.
   b. In the *Value* field, specify the required value of the discrete component.
   c. Click *OK*.

   For reference, see Example - Placing the 100u Capacitor, C1.
4. Similarly, add other discrete components as specified in the following table:

PSpice Part Name	PSpice Part Value
C2	22n
R1	4.7k
R2	60k
R3	20k
R4	40k
L1	10u
C3	0.01u
C4	1u
R5	50m
L2	10u
C5	100u
R6	200

PSpice Part Name	PSpice Part Value
L3	2u
C6	10u
R7	5

5. Search for 12TQ045 diode in the *PSpice* node in Component Explorer and place it on the schematic.
6. Place the AGND port on the schematic.

Example - Placing the 100u Capacitor, C1

1. Choose *Place – PSpice Part – Capacitor*.
2. Click the schematic page to place the capacitor C1 below the VBATT port as shown in the figure, Circuit for smart multi-channel switch, TLE8110EE
3. Right-click and choose *End Mode* or press Esc.
4. Double-click the value, 1n.

   The *Display Properties* dialog box opens.
5. In the *Value* field, specify the value of C1 as 100u.
6. Click *OK*.

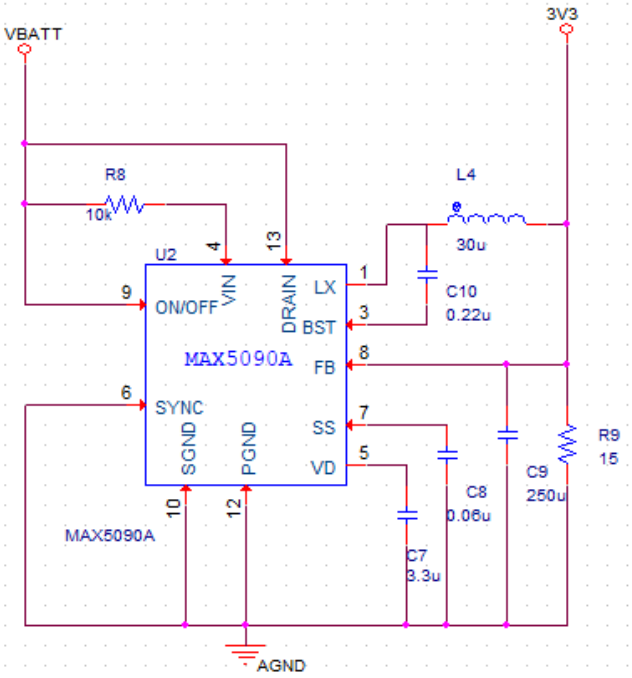
Connecting all the Components in Subdesign 1

1. Draw a wire from pin 1 of LM3478 to the source of MOSFET M1, IRF7807.
2. Draw a wire from pin 6 LM3478 to the gate of MOSFET M1, IRF7807.
3. Draw a wire from 10u inductor, L1 to the drain of MOSFET M1, IRF7807.
4. Similarly, add wires to the subdesign 1 until all the components are connected as shown in the figure, Subdesign 1B: 12V to 5V Converter.

Subdesign 2: 12 Volt to 3.3 Volt Converter

The subdesign 2 of the fan module uses the IC, `MAX5090A`, which is a DC-DC converter that is down converting `12 volt` to `3.3 volt`. The output of `3.3 volt` powers the fan.

Circuit for 12 Volt to 3.3 Volt converter



Subdesign 2: 12 Volt to 3.3 Volt Converter

Creating Subdesign 2

To create subdesign 2, you must place the following components as listed in the following table:

Component	Source
DC-DC converter MAX5090A	Place – Component – Component Explorer
Ground symbols	Place – PSpice Part – PSpice Ground
Power ports	Place – Power

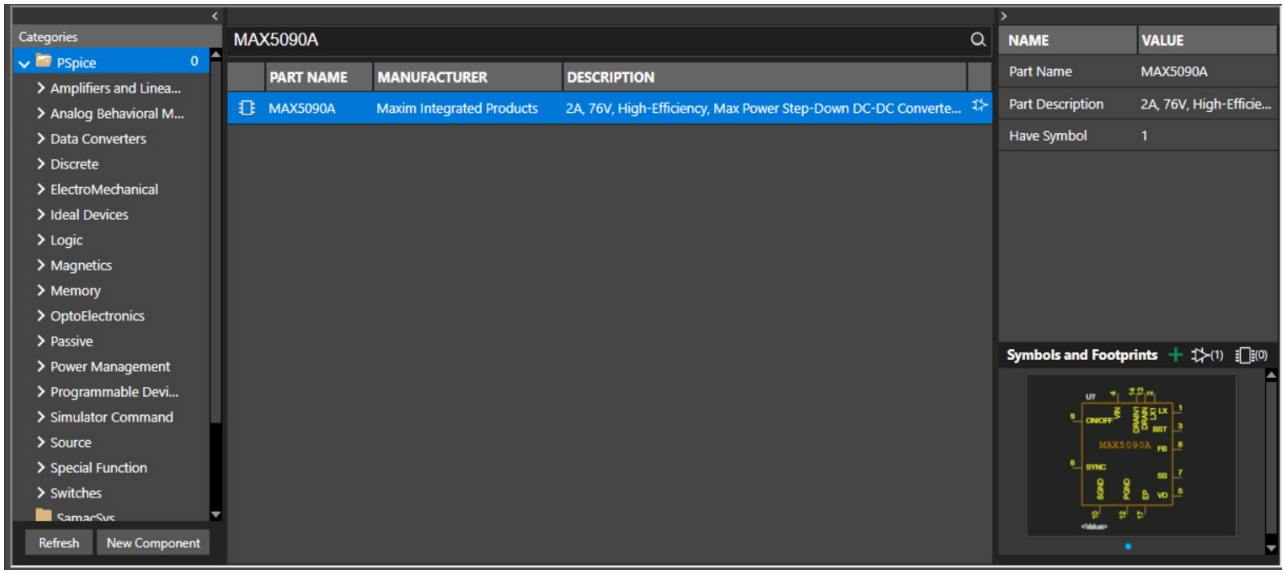
Component Placement for Subdesign 1A

1. To place the DC-DC converter, `MAX5090A`.

   a. Choose *Place – Component.*

   In the *Component Explorer* interface, the *PSpice* node is selected by default in the *Categories* pane.

   b. Specify `MAX5090A` in the *Search here* text box and press `Enter` or click the magnifying lens icon.



   c. Double-click `MAX5090A` in the search results.

   d. Click the schematic page to place the component and press `Esc`.

2. Place the `VBATT`, `AGND`, and `3V3` power ports shown in figure, Circuit for 12 Volt to 3.3 Volt converter.

3. Place the remaining discrete components in figure, Circuit for 12 Volt to 3.3 Volt converter) and specify their values from the following table:

PSpice Part Name	PSpice Part Value
`L4`	`30u`
`C10`	`0.22u`
`R8`	`10k`

PSpice Part Name	PSpice Part Value
C7	3.3u
C8	0.06u
C9	250u
R9	15

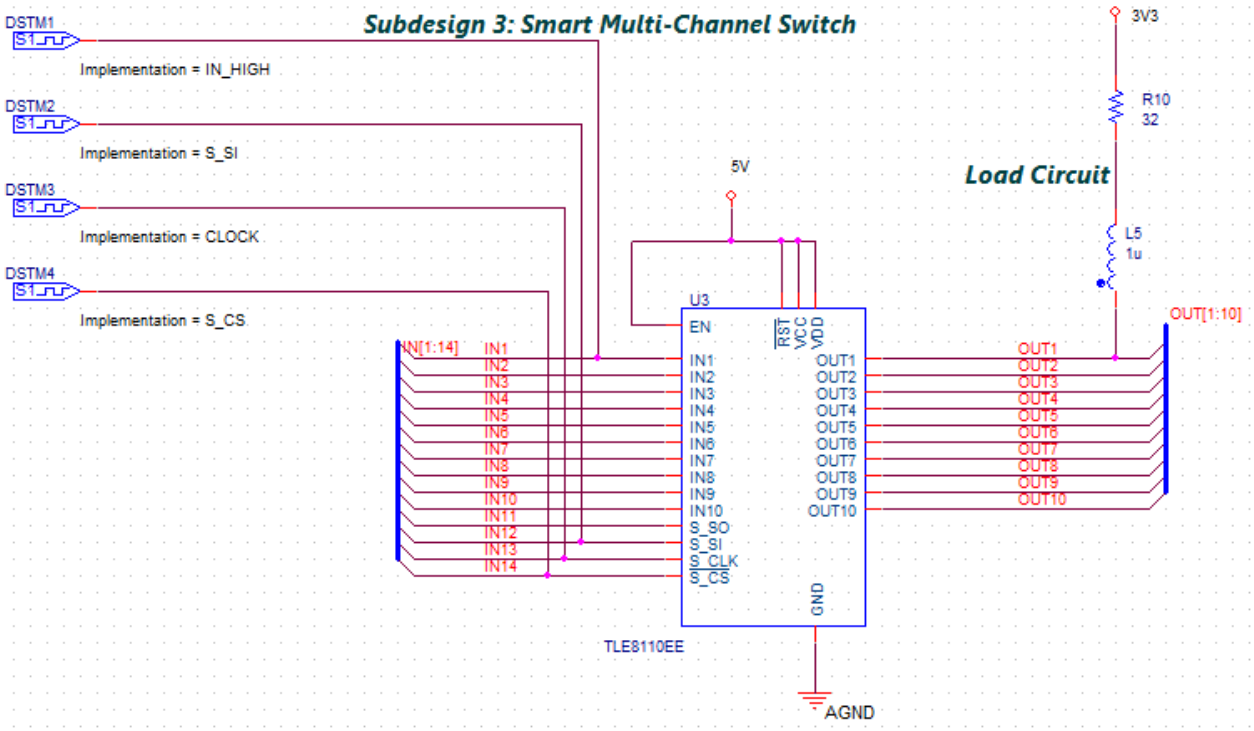
4. Right-click C8 and choose *Edit Properties*.
5. Set the value of *IC* as 0.
6. Add wires to the subdesign 2 until all components are connected as shown in figure, Circuit for 12 Volt to 3.3 Volt converter.

Subdesign 3: Smart Multi-Channel Switch Circuit

In subdesign 3, you will create the circuit for a smart multi-channel switch as shown in figure, Circuit for smart multi-channel switch, TLE8110EE.

In this subdesign an IC, `TLE8110EE` is placed to be interfaced with an off-board micro-controller. The input to the 10 channels of this IC are digital signals generated from a micro-controller. For this tutorial, these digital signals are modeled using digital stimulus sources.

Circuit for smart multi-channel switch, TLE8110EE



Creating Subdesign 3

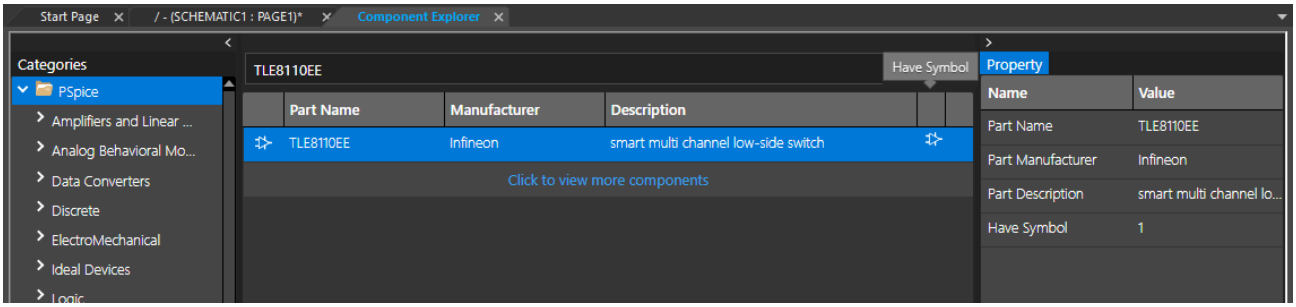
To create the subdesign 3, you must place the following components as listed in the following table:

Component	Source
`IC TLE8110EE`	`Place – Component – Component Explorer`

Component	Source
Ground symbols	Place – PSpice Part – PSpice Ground
Power ports	Place – Power
Discrete components: Inductor and Resistor	Place – PSpice Part
Digital stimulus DIGSTIM1	Place – Component – Component Explorer

Component Placement for Subdesign 3

1. Place the IC, TLE8110EE from the *PSpice* node of the Component Explorer interface.



2. Place the AGND, 5V, and 3V3 power ports shown in figure, Circuit for smart multi-channel switch, TLE8110EE.

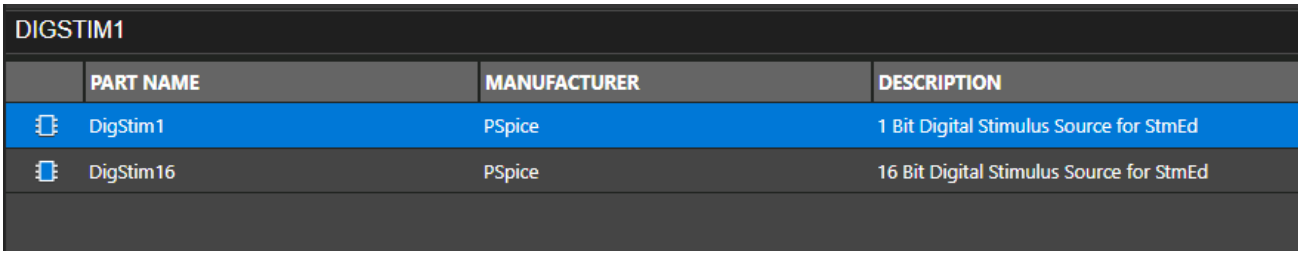
3. Place the discrete components as shown in figure, Circuit for smart multi-channel switch, TLE8110EE and specify their values from the following table:

PSpice Part Name	PSpice Part Value
R10 This resistor forms the RL circuit for the fan type of load.	32
L5 This inductor forms the RL circuit for the fan type of load.	1u

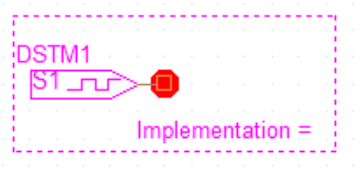
4. Place the digital stimulus sources from the *PSpice* node in the *Component Explorer* interface.

   These are `1-bit` digital stimulus sources.

   To add these, search for `DIGSTIM1` in the *PSpice* node of *Component Explorer* and select `DigStim1` from the results.



5. Double-click the `Implementation` property of a digital stimulus source.



   The *Display Properties* dialog box opens.

6. In the *Value* field, specify the value of this `Implementation` property as shown in the following table:

Digital Stimulus Source Name	Value of Implementation property
DSTM1	IN_HIGH
DSTM2	S_SI
DSTM3	CLOCK
DSTM4	S_CS

   Note: The stimulus data from these sources is read from a `.stl` file.

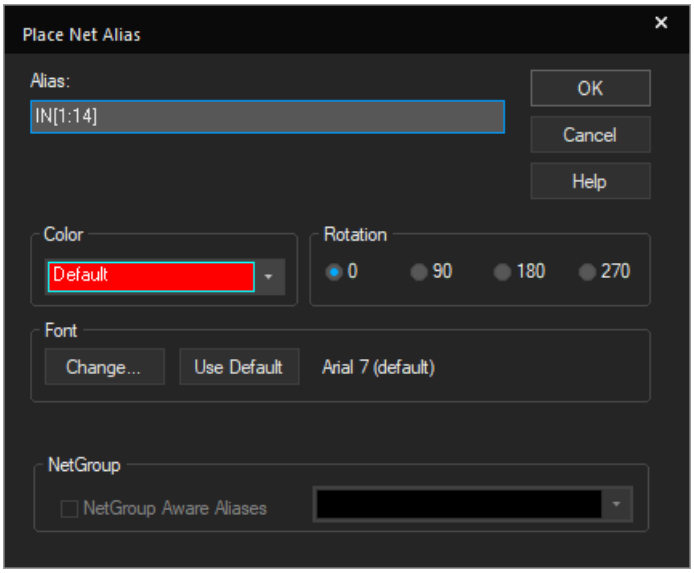
Placing and Connecting Buses

1. Select *Place – Bus* or press `B`. Alternatively, click the *Place bus* icon () on the *Draw Electrica*l toolbar.

The cursor shape changes from pointer to cross-hair.

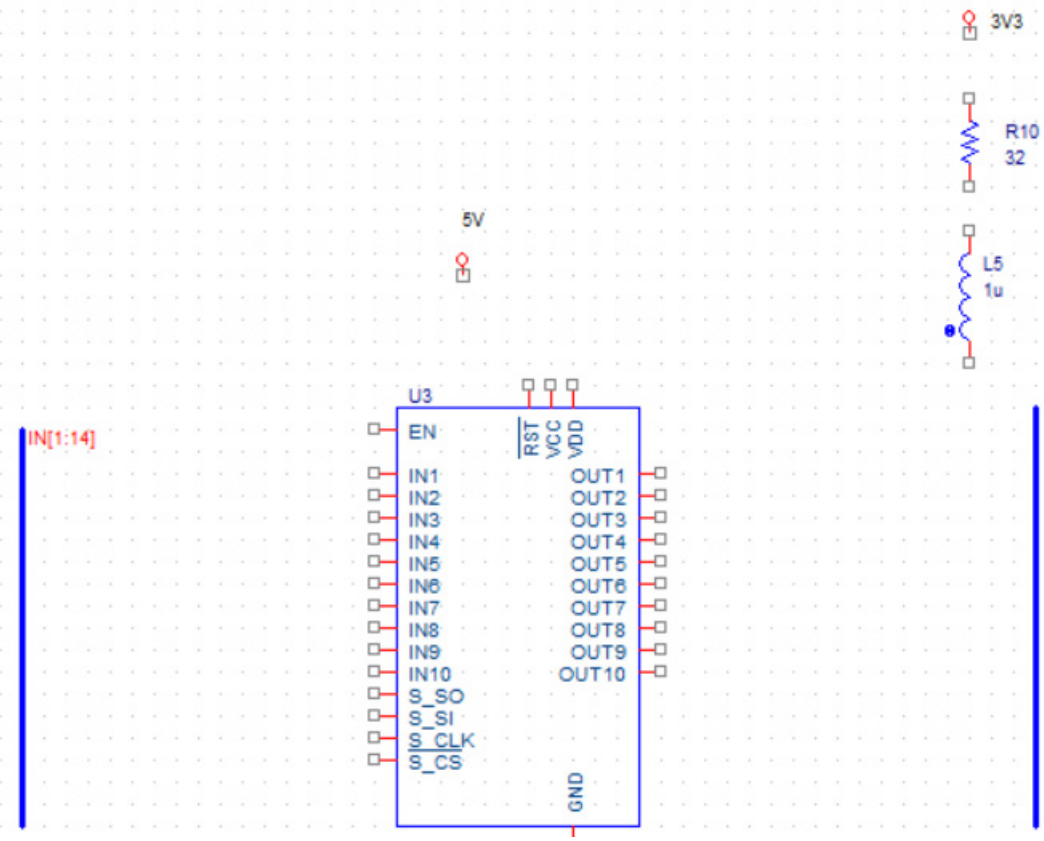
2. Draw the bus before the input pins and after the output pins of `TLE8110EE` as shown in figure, Placing Buses.
3. Select *Place – Net Alias* or press *N*. Alternatively, click the *Place net alias* icon ( ) on the *Draw Electrical* toolbar.

   The *Place Net Alias* dialog box appears.
4. Specify the value in the *Alias* field as `IN[1:14]`.



5. Click *OK*.
6. Move the cursor on the bus and place the net alias name as shown in the following figure:

Placing Buses

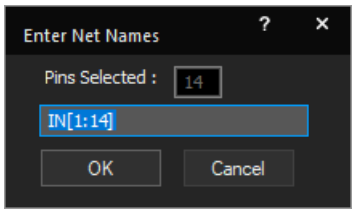


7. Select all the input pins of `TLE8110EE` (except `EN`), right-click the selection, and choose *Connect to Bus*.

   The cursor shape changes from pointer to cross-hair.

8. Click the bus placed before the input pins.

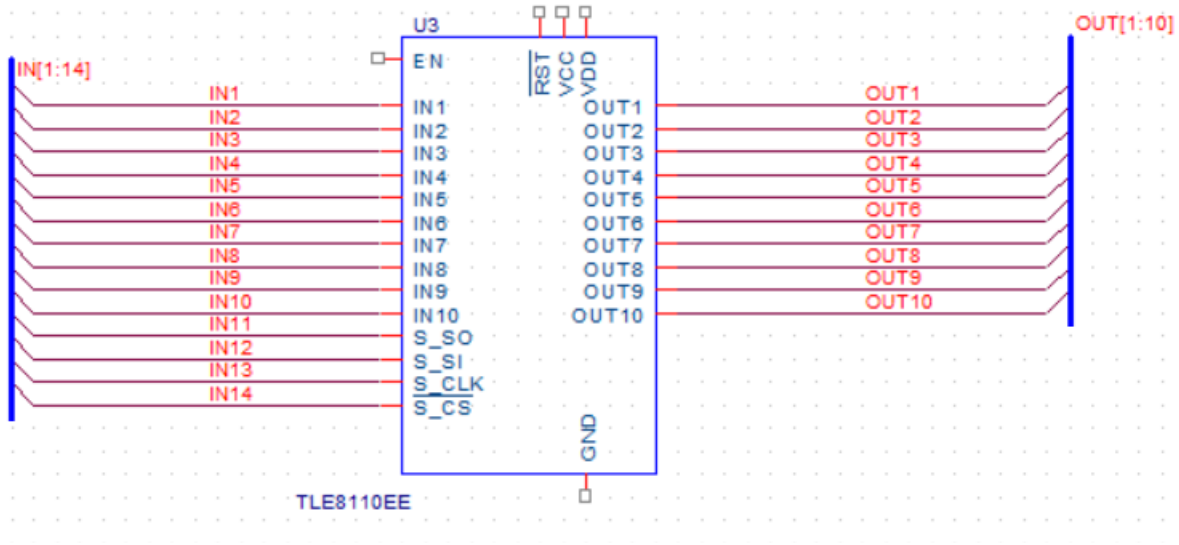
   The *Enter Net Names* dialog box appears.



9. Click *OK*.

   Net names appear on each net from the input pins to the bus.

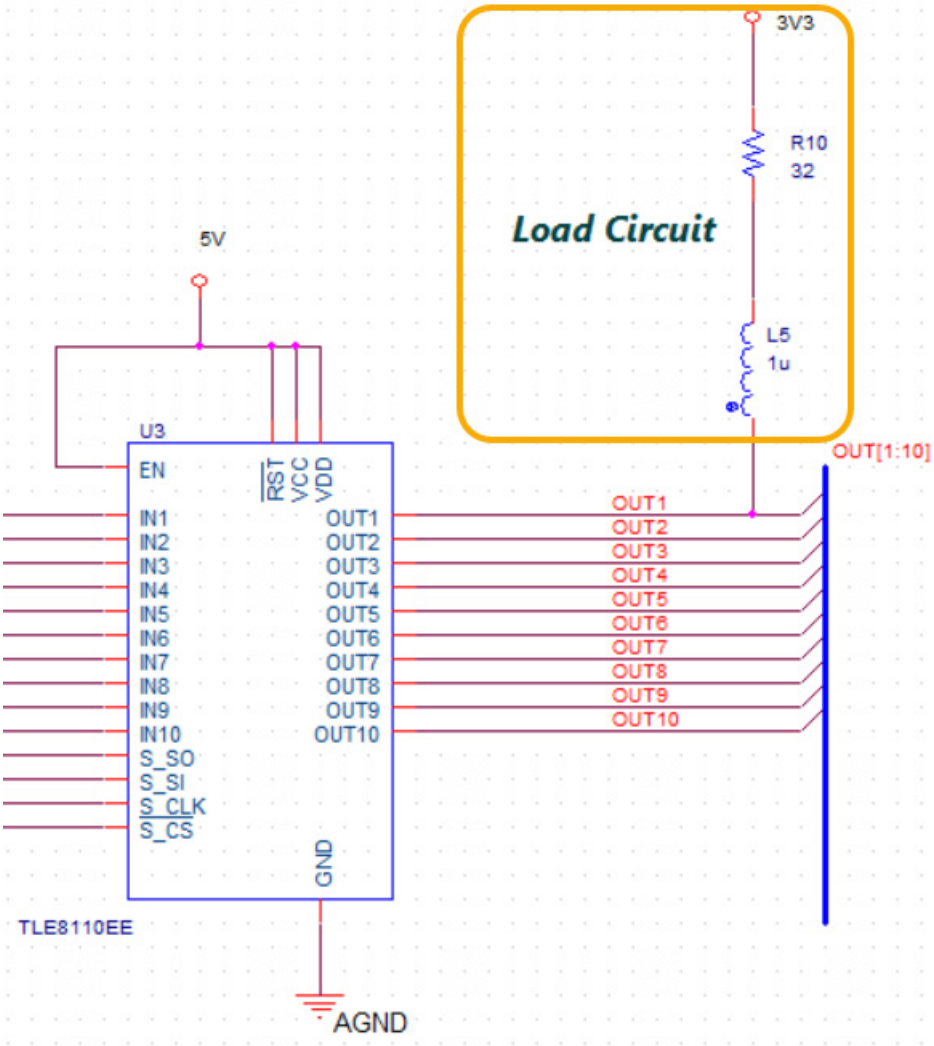
10. Repeat steps 3 to 10 to place the `OUT[1:10]` net alias on the bus placed next to the output pins of `TLE8110EE`, and to connect the output pins of `TLE8110EE` to this bus as shown in the following figure:



Connecting Components of Subdesign 3

1. Draw a wires from the pins, `RST`, `VCC`, and `VDD` to the `5V` power port.
2. Draw a wire from the `5V` power port to the input pin, `EN` of `TLE8110EE`.
3. Draw a wire from the `GND` pin to the power port, `AGND`.
4. Draw a wire from the output pin of:
   - `DSTM1` (with `implementation=IN_HIGH`) to net `IN1`.
   - `DSTM2` (with `implementation=S_SI`) to net `IN12`.
   - `DSTM3` (with `implementation=S_CLK`) to net `IN13`.
   - `DSTM4` (with `implementation=S_CS`) to net `IN14`.

5. Connect the load circuit to the net, `OUT1` as shown in the following figure:



Summary

This section covered the steps to create a schematic design using Capture CIS. In the process, you were introduced to some of the basic design creation tasks, such as creating a project, placing parts, editing property values, and connecting parts.

3

Simulating a Design

In this section, you will use PSpice to simulate the design created in the previous section using Capture CIS. You will also learn about transient analysis that is performed using PSpice.

Getting the Design Ready for Simulation

To simulate a design, the PSpice simulator needs information about circuit topology, analysis type, and stimulus definitions.

The analysis type, stimulus definition, and the information related to the initial digital state of the simulation is provided by a simulation profile (`*.SIM`). In the following section, you will create a simulation profile.

Prerequisite to Simulation Setup

Before creating the simulation profile, you need to specify the stimulus definition to be used for simulating the circuit. For this, you need to create a stimulus file and then specify its location in the *Simulation Setting* dialog box to create the simulation profile. To create the stimulus file, copy the following information in a text editor (`.txt`) file and save it as `stimulus.stl`.

```
.STIMULUS IN_HIGH STIM (1, 1)
+ 0 0
+ +0 1

.STIMULUS S_SI STIM (1, 1)
+0ms 0
+808.400000000u 0
+ +200ns 0
+ +200ns 0
+ +200ns 0
+ +200ns 0
+ +200ns 1
+ +200ns 1
+ +200ns 1
+ +200ns 0
+ +200ns 0
+ +200ns 0
+ +200ns 1
+ +200ns 0

.STIMULUS CLOCK STIM (1, 1)
+ 0 0
+ +0 1
+REPEAT FOREVER
+ +100n 0
+  +100n 1
+ ENDREPEAT

.STIMULUS S_CS STIM (1, 1)
+0u 0
+807.763636u 1
+808.333363636u 0
+811.56335227u 1
+812.13370351u 0
```

Creating a New Simulation Profile

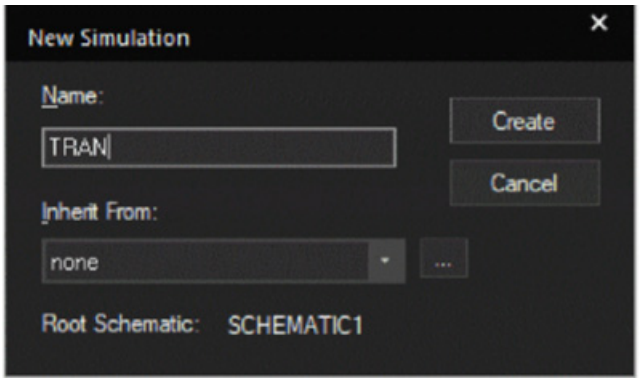
To view the behavior of this circuit over time, transient analysis will be used. To perform this analysis, you will specify this analysis type when creating the simulation profile.

To create a new simulation profile, do the following:

1. Choose *PSpice – New Simulation Profile*, or click the *New Simulation Profile* icon on the PSpice toolbar.

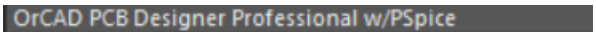
   The *New Simulation* dialog box opens

2. Specify the name of the new simulation profile as `TRAN`.
3. In the *Inherit From* drop-down list, ensure that `none` is selected and click *Create*.



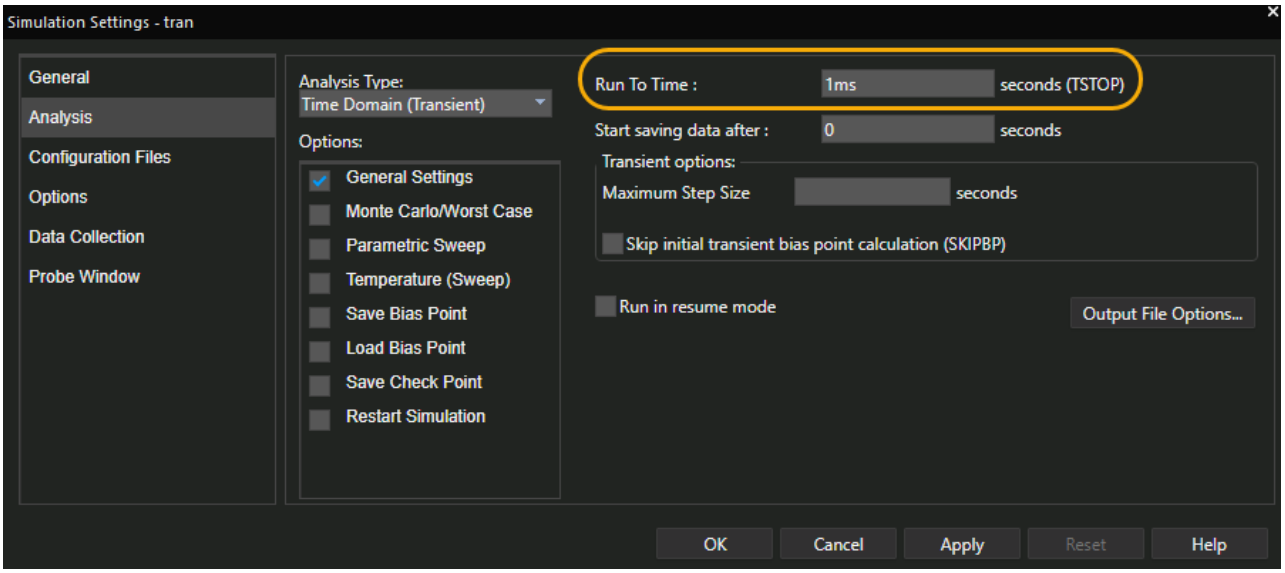
   The *Simulation Manager Product Choices dialog box appears*.

4. Select the OrCAD X PCB Designer Professional w/PSpice suit and click OK.



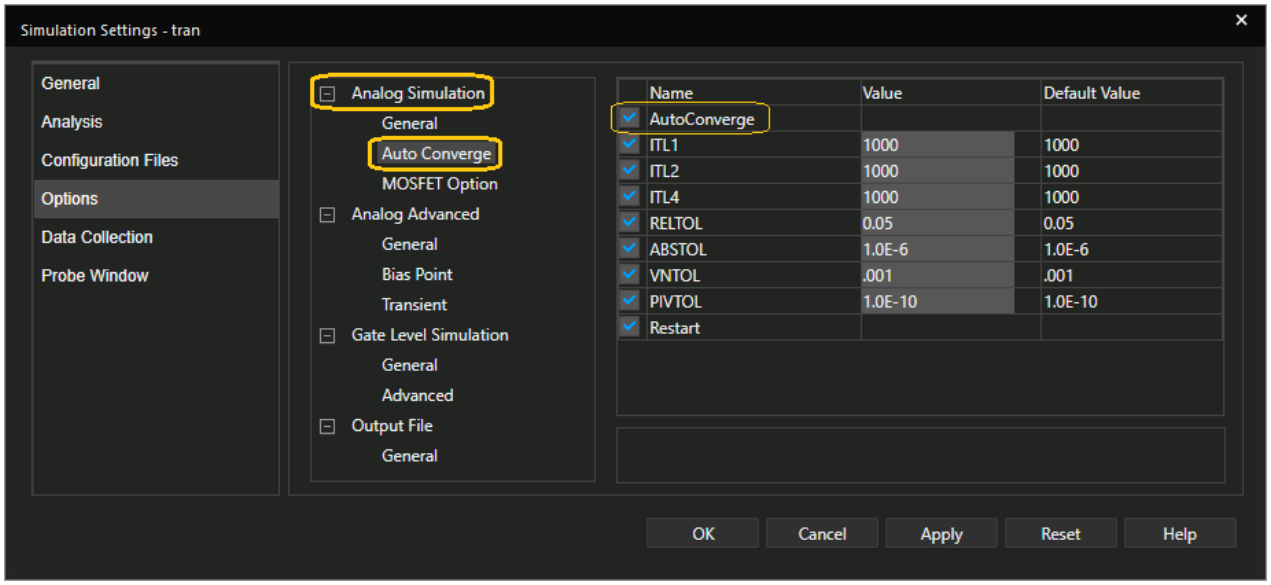
5. The Simulation Setting dialog box appears with the Analysis tab selected.
6. In the *Analysis Type* drop-down list, `Time Domain (Transient)` is selected by default. Retain this default setting.
7. Specify the following options to run a transient analysis.
   - ❑ In the *Run To Time* text box, specify the time as `1ms`.

Simulation Setup - Analysis tab

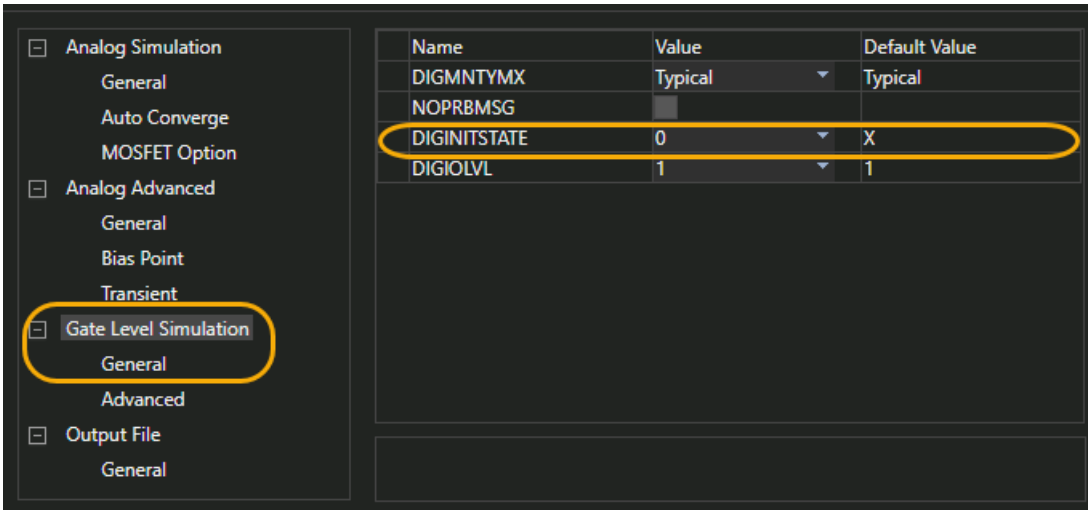


8. To prevent any convergence issues, in the *Options* tab, select the *AutoConverge* check box.

Simulation Setup - Options tab



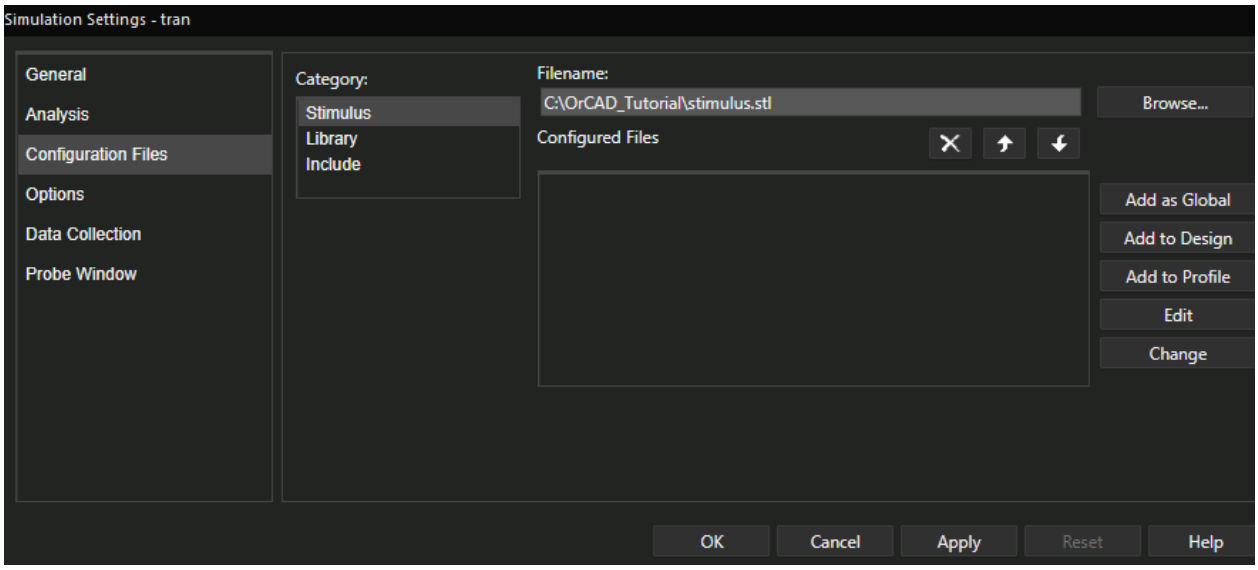
9. To set the initial digital state of the simulation to `0`, make the following modification by setting *DIGINISTATE* as `0` in the *Gate Level Simulation* tab.



10. In the *Configuration Files* tab, select `Stimulus` from *Category* list.

11. Click the *Browse* button to navigate to the `stimulus.stl` file and click *Open*.

Simulation Setup - Configuration Files tab



12. Click the *Add to Design* button.

13. Click *OK* to save your modifications and to close the dialog box.

When the simulation is run from the schematic, the simulator reads the SPICE models connectivity information (netlist) from the design files, and the analysis type and the stimulus details from the simulation profile.

Running the Simulation

➡ To simulate the design, choose *PSpice – Run* or click the *Run PSpice* icon.

The Schematic1-TRAN - PSpice window opens.

Viewing Output Waveforms

To visualize the circuit behavior and determine the validity of your circuit design, you can plot the output waveforms in the Probe window. By analyzing the output waveforms you can evaluate your circuit for performance.

For PSpice to display output waveforms in the Probe window, you need to place markers in your circuit design in Capture to indicate the points where you want to see simulation waveforms displayed in PSpice.

Markers can be placed:

- before simulation to limit results written to the waveform data file, and automatically display those traces in the active Probe window.
- during or after simulation, to automatically display traces in the active Probe window.

➡ To add markers, choose *PSpice – Markers* or use the icons provided on the PSpice toolbar.

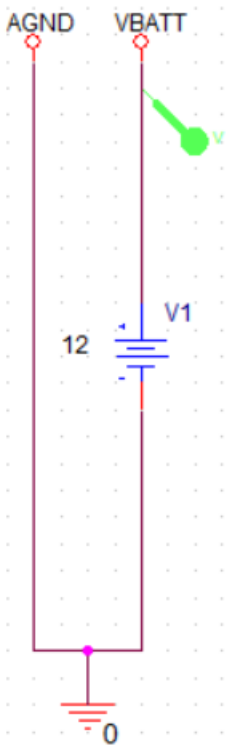
Important

To view the markers in the simulation results, the schematic design must be open.

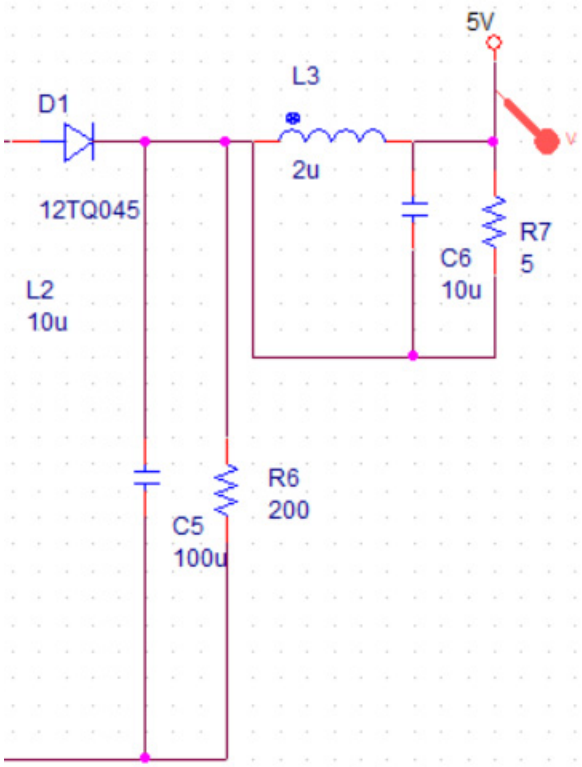
You will now add Voltage markers to view the output waveforms in the Probe window. To do so:

1. Select *PSpice – Markers – Voltage Level*, or click the Voltage/Level Marker icon () on the PSpice toolbar.

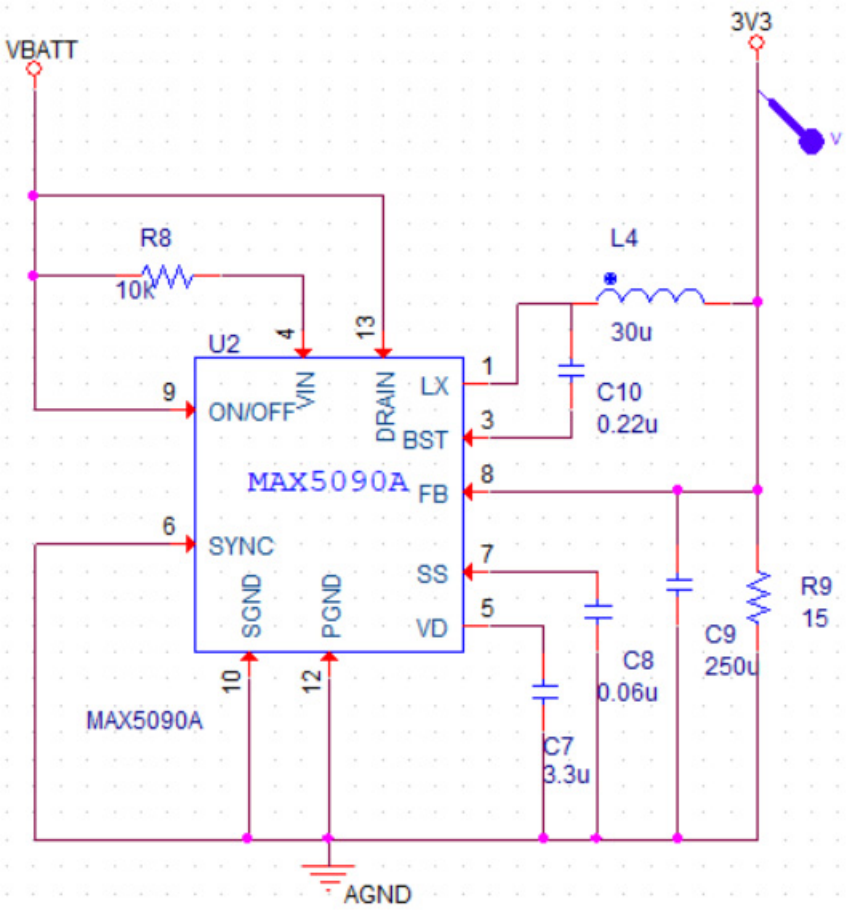
2. Place the marker at the main power supply, that is at the 12 Volt `VBATT` power net.



3. Place the marker at the end of the first subdesign (12V to 5V converter), that is at the `5V` power net, as shown in the following figure.



4. Place another voltage marker at the end of the third subdesign (12V to 3.3V converter), that is at the `3V3` power net, as shown in the following figure.

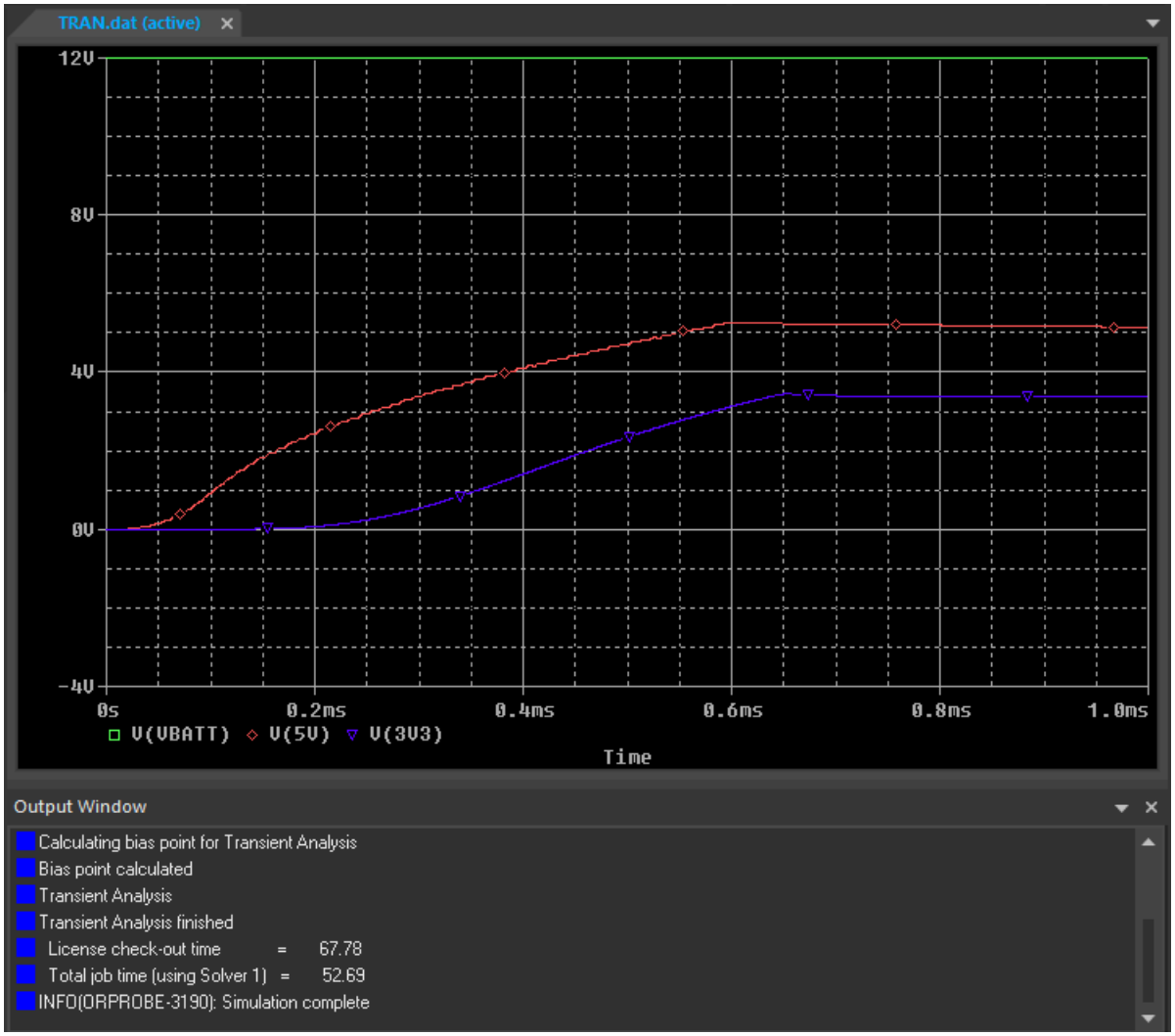


Note: If you add markers before simulating the design, the output waveforms are displayed automatically in the Probe window after the simulation is complete.

5. Switch to the Probe window to view the output waveform.

   The output waveform appears as shown in the following figure.

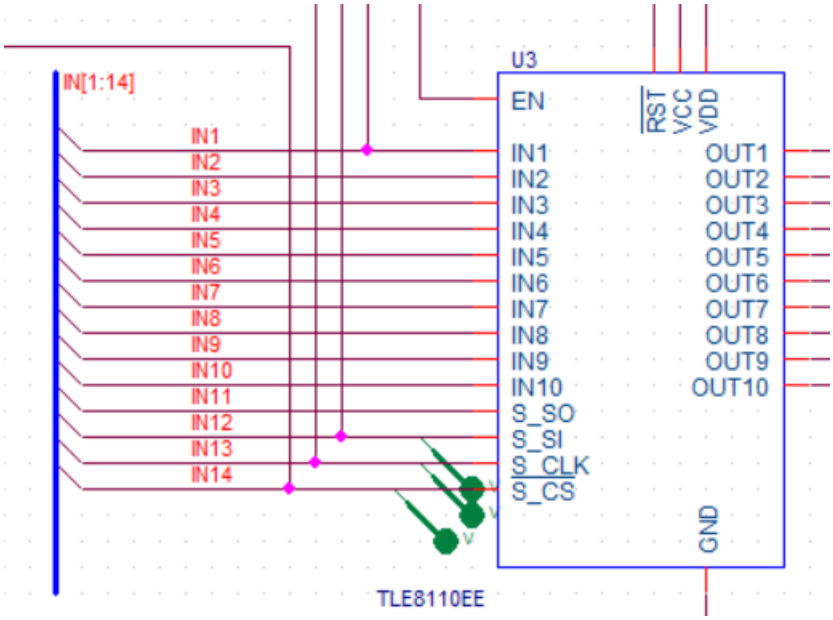
Output Waveform - Probe window



6. To view the waveform of the digital stimulus sources at the input of the switching IC `TLE8110EE`, place voltage markers on the following nets:

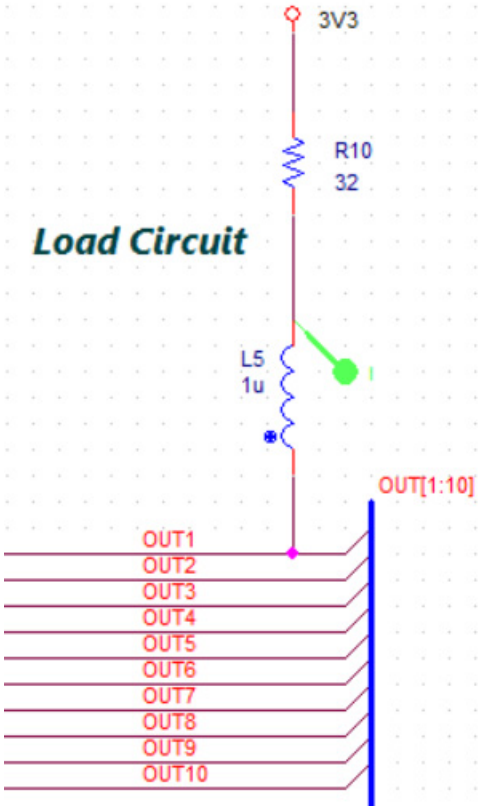
- ❑ `IN12` (connected to pin S_SI)
- ❑ `IN13` (connected to pin S_CLK)

- ❑ `IN14` (connected to pin S_CS)

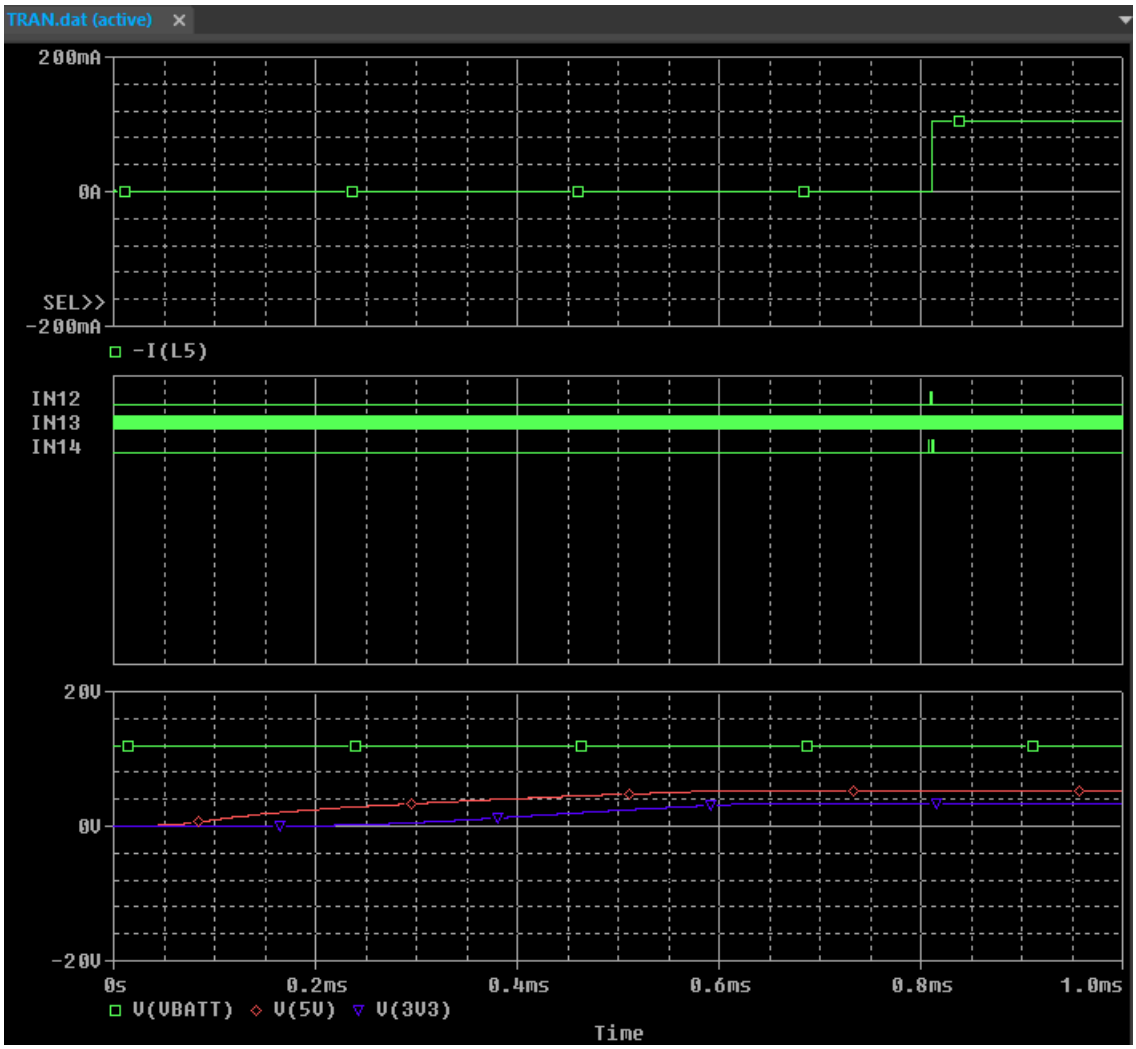


7. In PSpice, select *Plot – Add Plot to Window*.

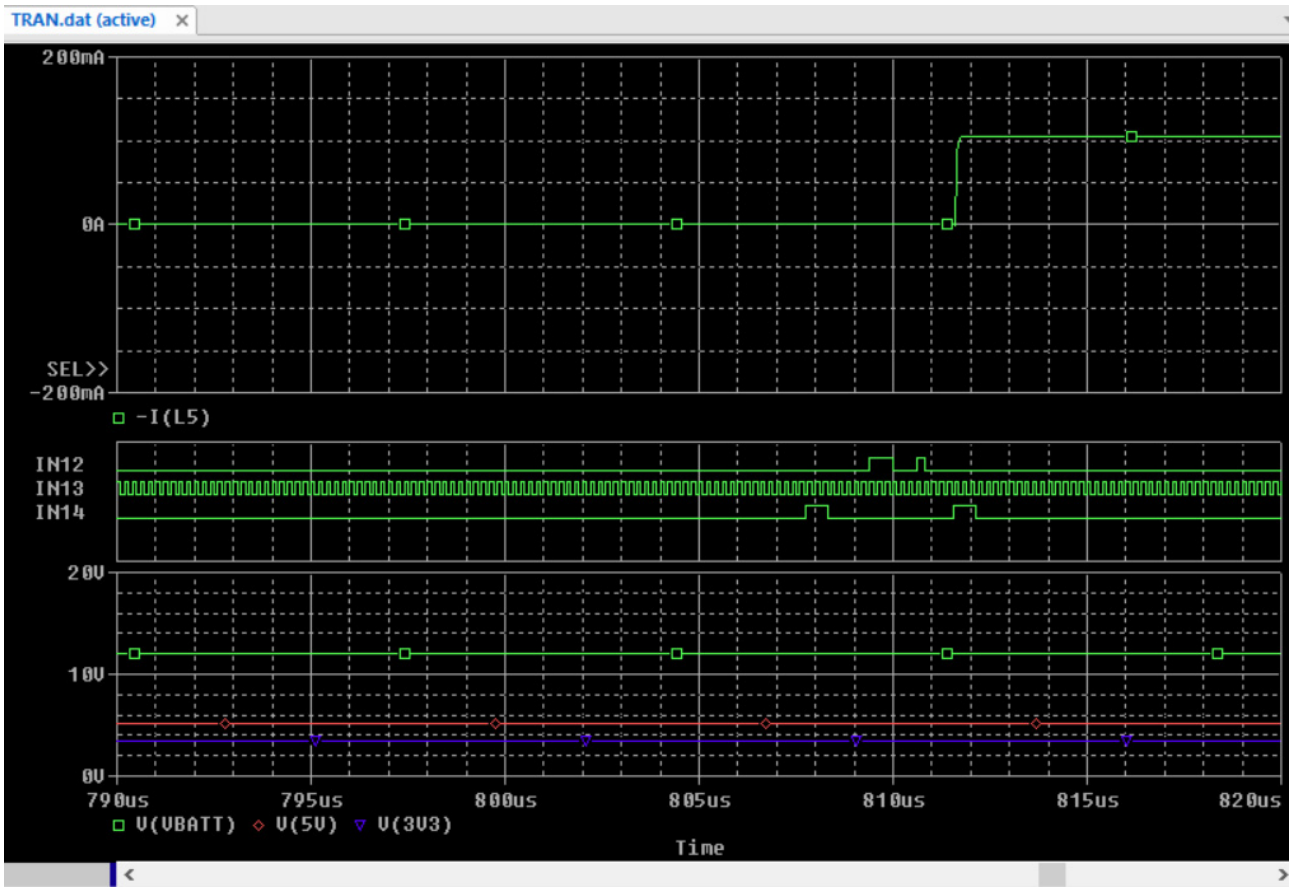
8. In Capture, place a current marker (using the *Current Marker* icon, ) on the pin of the inductor as shown in the following figure.



The changes in the waveform are displayed in the following figure:



The command to turn on the fan is sent to the `S_SI` pin. This command is read and executed at the low to high transition of the `S_CS` signal. The input signal through the `S_SI` pin is sent from the duration `808us` to `811us`, as shown in the following figure:



Summary

This section covered the steps for simulating the fan module design using PSpice. In this section, you were introduced to various tasks involved in the simulation process, such as creating a simulation profile, running simulation, placing markers, and analyzing simulation results.

4

Preparing for PCB Layout Creation

Now that you have verified the performance of your logical circuit through simulations, you can start designing the physical layout of the PCB board for this schematic design.

Before you create the PCB layout for this schematic design, you need to ensure that the design has no open or unconnected signal, footprint information is available for all components, and electrical constraints, if any, are specified.

Adding and Placing Connectors

To connect the fan module with a system, connector components are required to be placed in the schematic design.

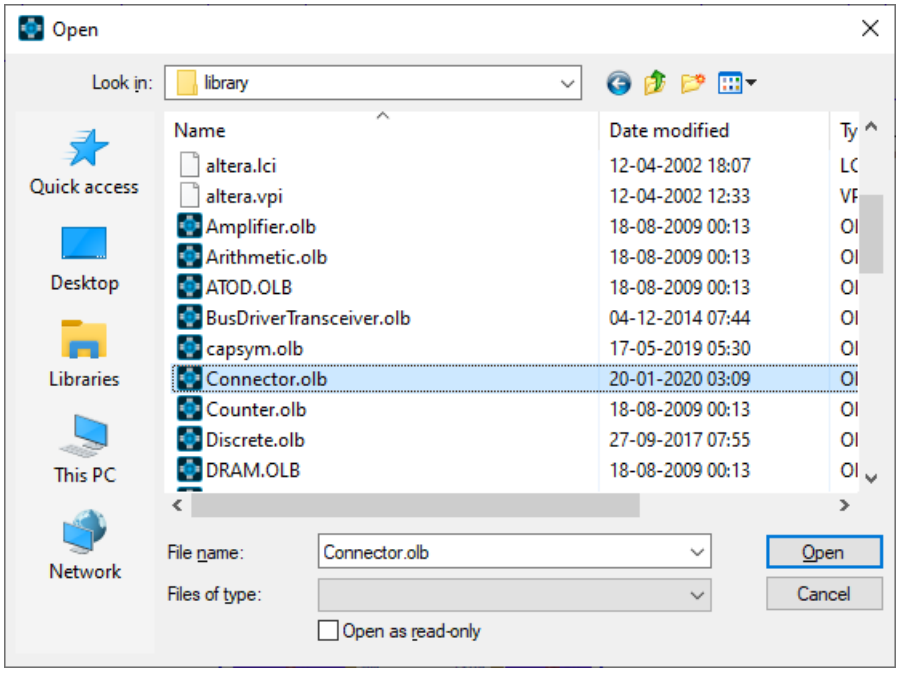
To add and place connectors in this schematic design, do the following:

1. Open your Capture CIS design.
2. Select *Place – Part*, press *P*, or click the Place part icon ().

   The *Place Part* pane opens.
3. To add `Connector.olb` to the project, click the *Add Library* icon ().

   The *Browse File* dialog box opens.

4. Browse to
`<installation_directory>\tools\capture\library\Connector.olb`.



5. Select `Connector.olb` and click *Open*, or double-click `Connector.olb`.

   The `CONNECTOR` library appears in the *Libraries* list box.

6. Search for `CON2_M` from the *Part* list box.

7. Click the *Place Part* icon ( ) or press *Enter*.

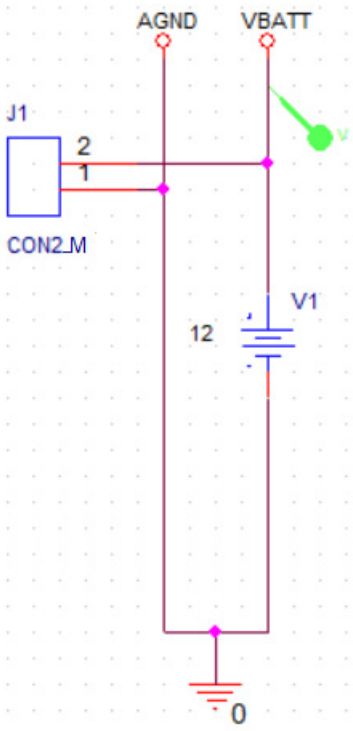
   The part symbol is attached to the cursor.

8. Click the schematic page where you have placed the 12 volt DC source and place the connector `J1`.

9. Right-click and select *End Mode* or press `Esc`.

10. Right-click this connector and select *Rotate* and the connect it as shown in Figure, Connector at the main power supply.

Connector at the main power supply



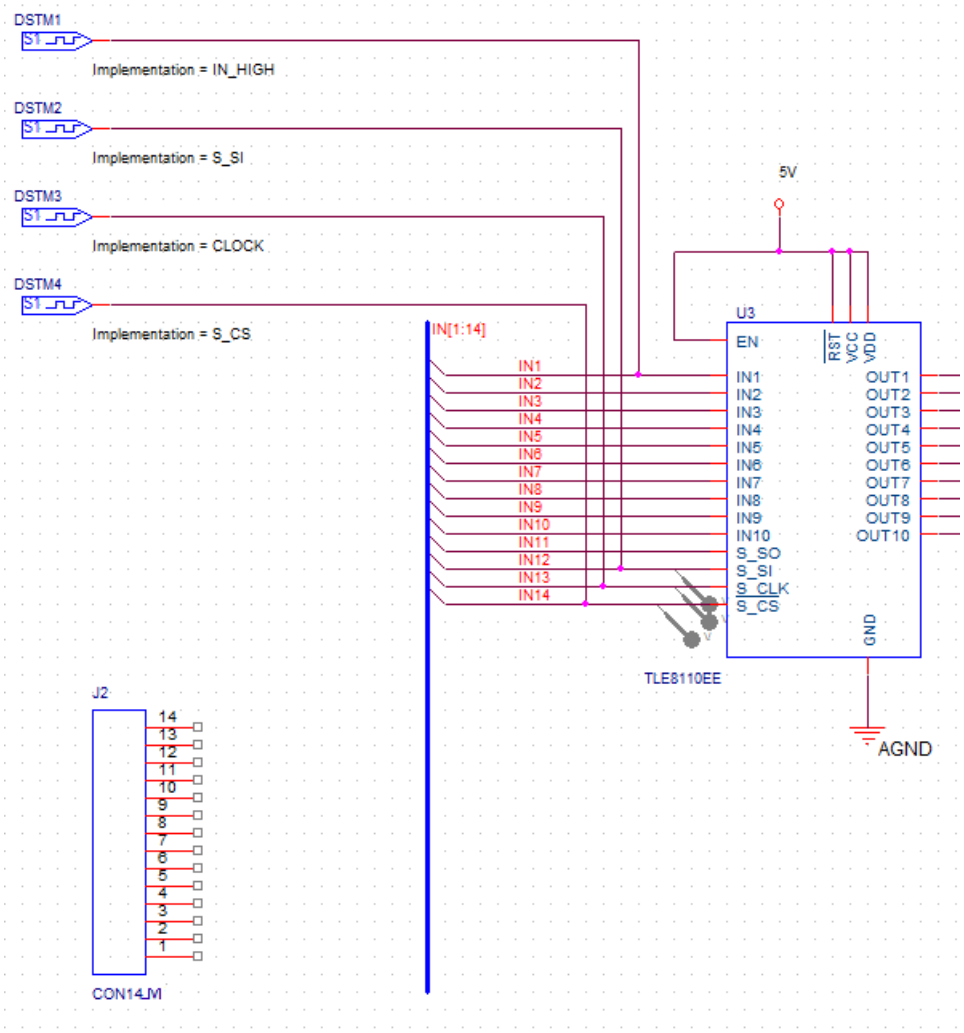
Similarly, add a 14-pin connector (`CON14_M`) to the input and output channels of the smart multi-channel switch IC.

To add the connectors in the smart multi-channel switch circuit, do the following:

1. In the *Place Part* pane, search and select `CON14_M` from the *Part* list box.
2. Click the *Place Part* icon ( ) or press *Enter*.

   The part symbol is attached to a cursor.
3. Click the schematic page before the IC `TLE8110EE` and place the connector `J2` as shown in Figure, Placing connector, J2.
4. Right-click `J2` and select *Rotate*.
5. Extend the bus before the input pins of `TLE8110EE` as shown in Figure, Placing connector, J2.

Placing connector, J2

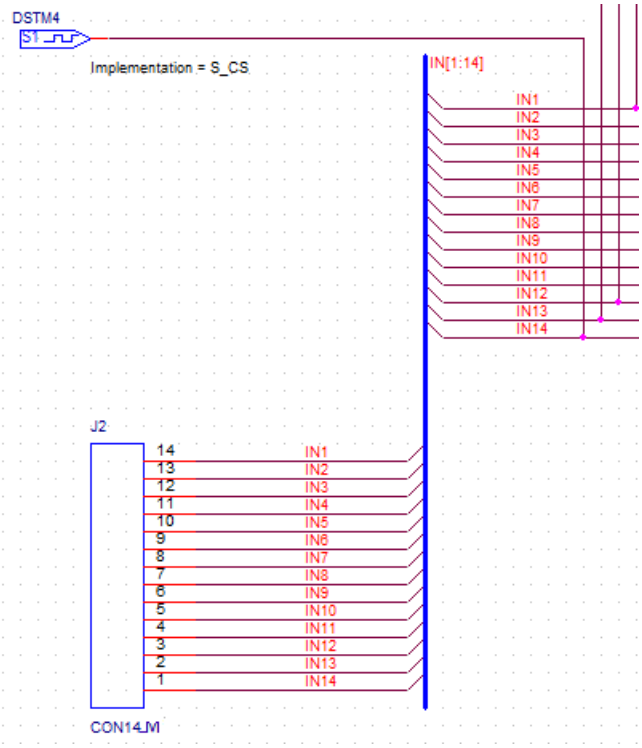


6. Select all the pins of connector `J2`, right-click the selection, and choose *Connect to Bus*.
7. Click the bus that you had extended in step 5.

   The *Enter Net Names* dialog box appears.
8. Click *OK*.

   Net names appear on each net from the connector pins to the bus.

Connecting J2 to bus at the input of TLE8110EE



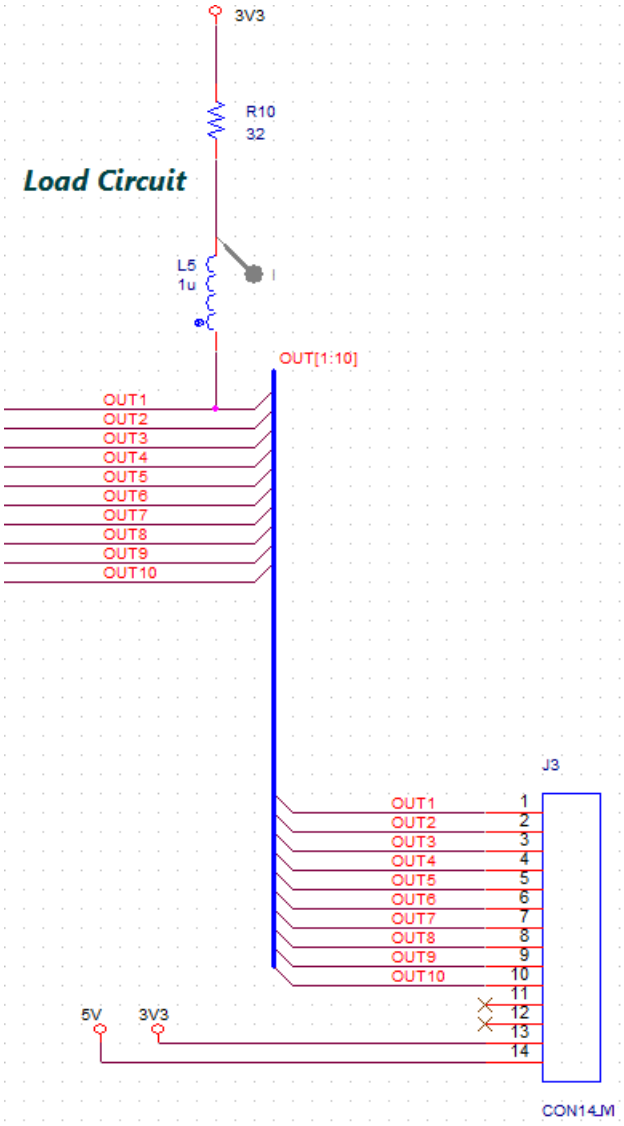
9. Similarly, place another connector `J3` and do the following:

   a. Connect its first 10 pins as shown in Figure, Connecting J3 to bus at the output of TLE8110EE.

   b. Click the No Connect icon ( ) or press *X*, and connect it to pins 11 and 12 of connector `J3`.

   c. Connect `3V3` and `5V` power ports to pins 13 and 14 of connector `J3`.

Connecting J3 to bus at the output of TLE8110EE



Updating Footprints

As the first step to preparing your design for layout creation, update the footprint associated with all the resistors in the design.

Updating Footprints Associated with Resistors

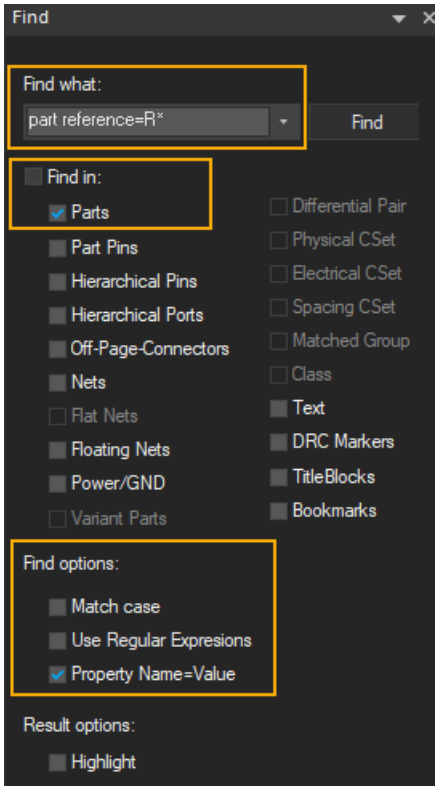
To assign footprints to all the resistors, do the following:

1. Select *Edit* – *Find* or press `CTRL+F`.

   The Find pane appears.

2. Specify `part reference=R*` in the *Find what* field.
3. Select the *Parts* check box under *Find in*.
4. Select the *Property Name=Value* check box under *Find options*.

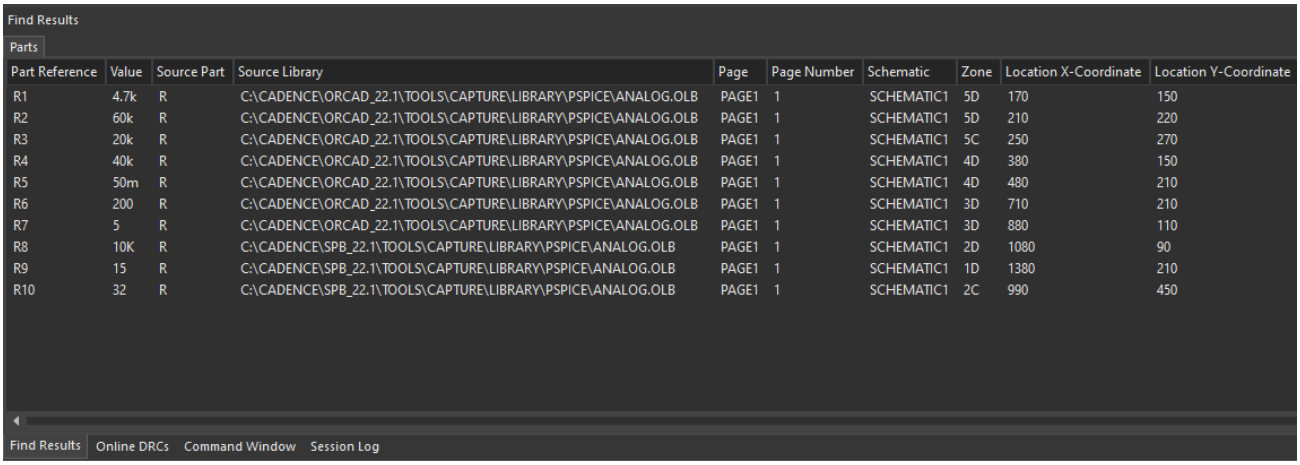
Specifying search criteria in Find pane



5. Click the *Find* button.

The Find Results window appears with all the resistors in the design.

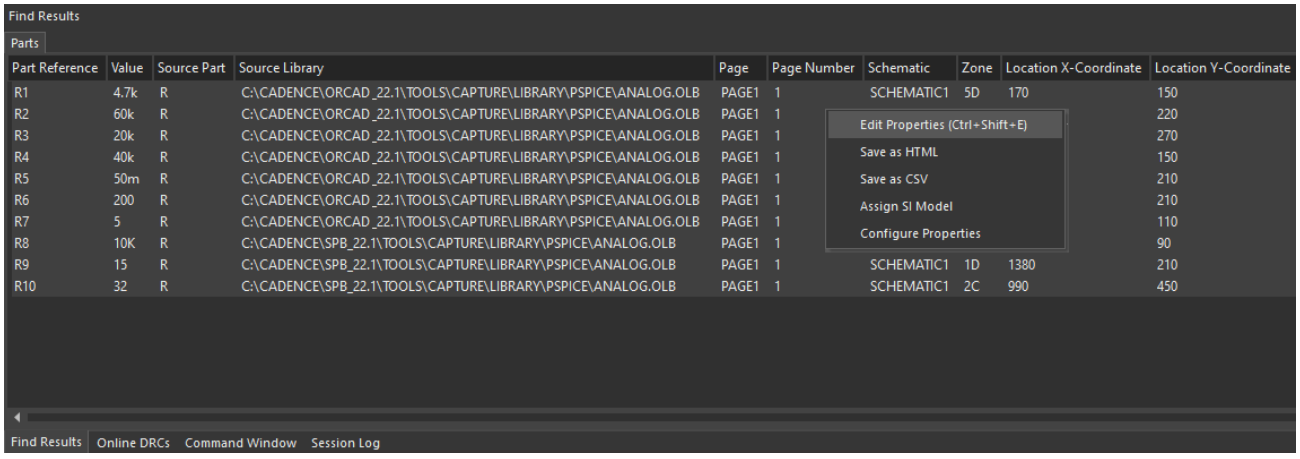
Viewing search results in Find Results window



6. To select all rows in the search result, click the first search results row, press `SHIFT` and then click the last search results row.

7. To modify the properties of the selected search results, right-click the selection and choose *Edit Properties* or press `CTRL+SHIFT+E`.

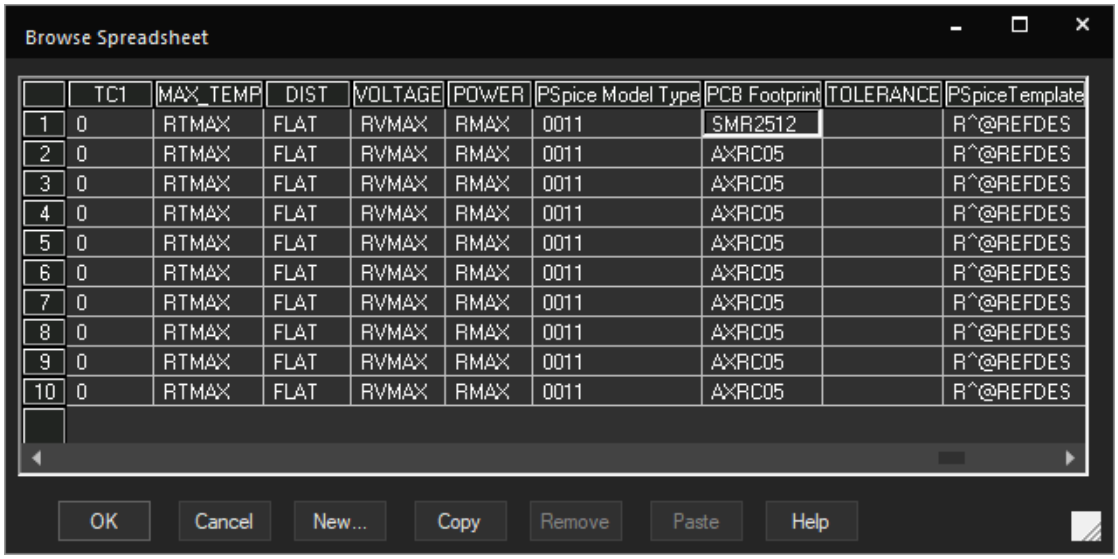
Editing properties of search results

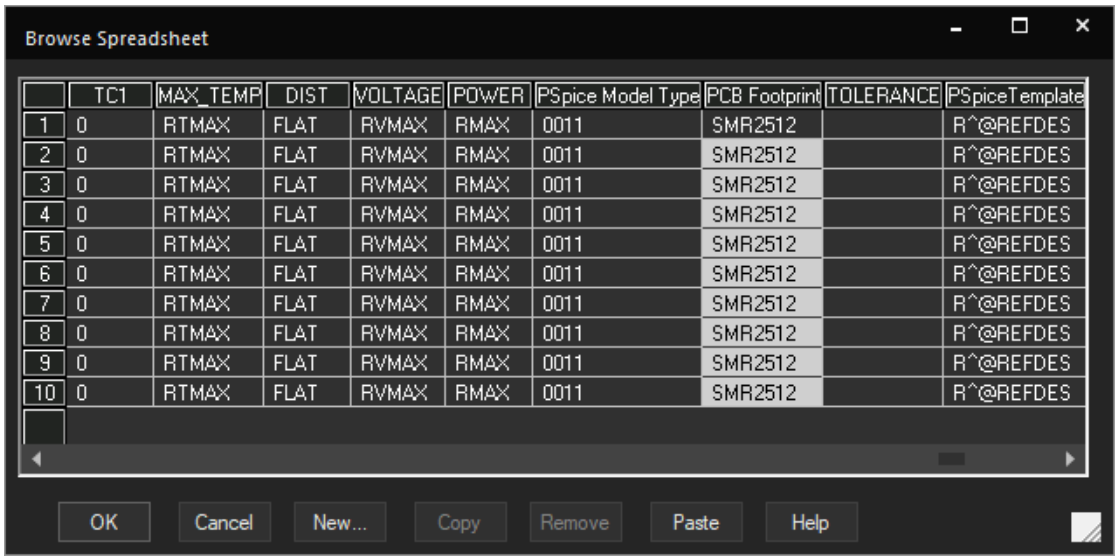


The Browse Spreadsheet window opens.

8. Change the value from `AXRC05` to `SMR2512` for *PCB Footprint* corresponding to each resistor.

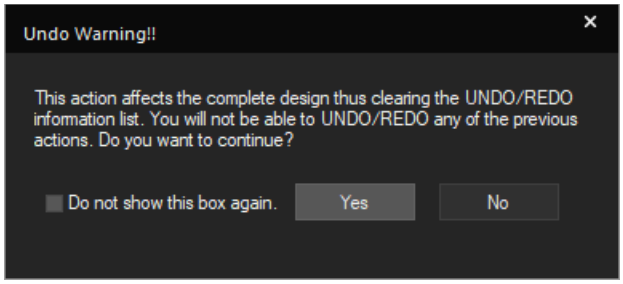
Changing PCB Footprint values in Browse Spreadsheet window





9. Click *OK*.

An undo warning appears to confirm the change.



10. Select the *Do not show this box again* check box and then click *Yes*.

Updating Footprints associated with Capacitors

To update footprints associated with all the capacitors in the design, do the following:

1. Repeat step 2 to step 10 listed in the section, Updating Footprints Associated with Resistors with the following changes:
   - In step 2, specify `part reference=C*` in the *Find what* field.
   - In step 8, change the value from `cap196` to `SMC0603` for *PCB Footprint* corresponding to each capacitor.
2. Save the design.

Updating Footprints associated with Inductors

To update footprints associated with all the inductors in the design, do the following:

1. Repeat step 2 to step 10 listed in the section, Updating Footprints Associated with Resistors with the following changes:
   a. In step 2, specify `part reference=L*` in the *Find what* field.
   b. In step 8, change the value from `DISC350x1`to `SML0805` for *PCB Footprint* corresponding to each inductor.
2. Save the design.

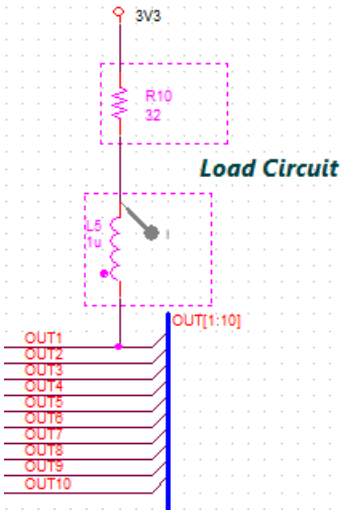
Configuring the PSpiceOnly Property

These components are added only to represent the fan loads and are not required for the physical layout. To ignore them in board design, the `PSpiceOnly` property is specified.

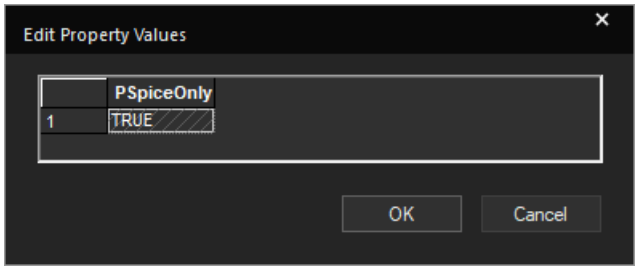
To assign the `PSpiceOnly` property to the inductor and the resistor of the load circuit, do the following:

1. Select the inductor and resistor in the load circuit.

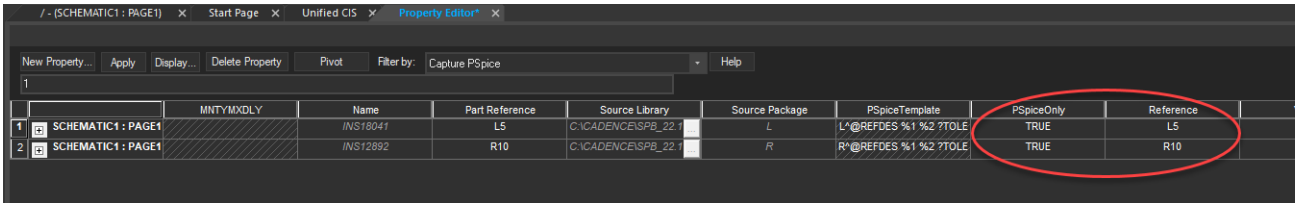
Selecting components of load circuit



2. Right-click and select *Edit Properties*.
3. Click the *Parts* tab in the *Property Editor* window.
4. From the *Filter by* drop-down list, select `Capture PSpice`.
5. Right-click the cell for the `PSpiceOnly` property and choose *Edit*.
6. Specify `TRUE` as the value in the *PSpice Only* cell and click *OK*.



Parts tab in Property Editor window



7. Save the design.

Adding Constraints

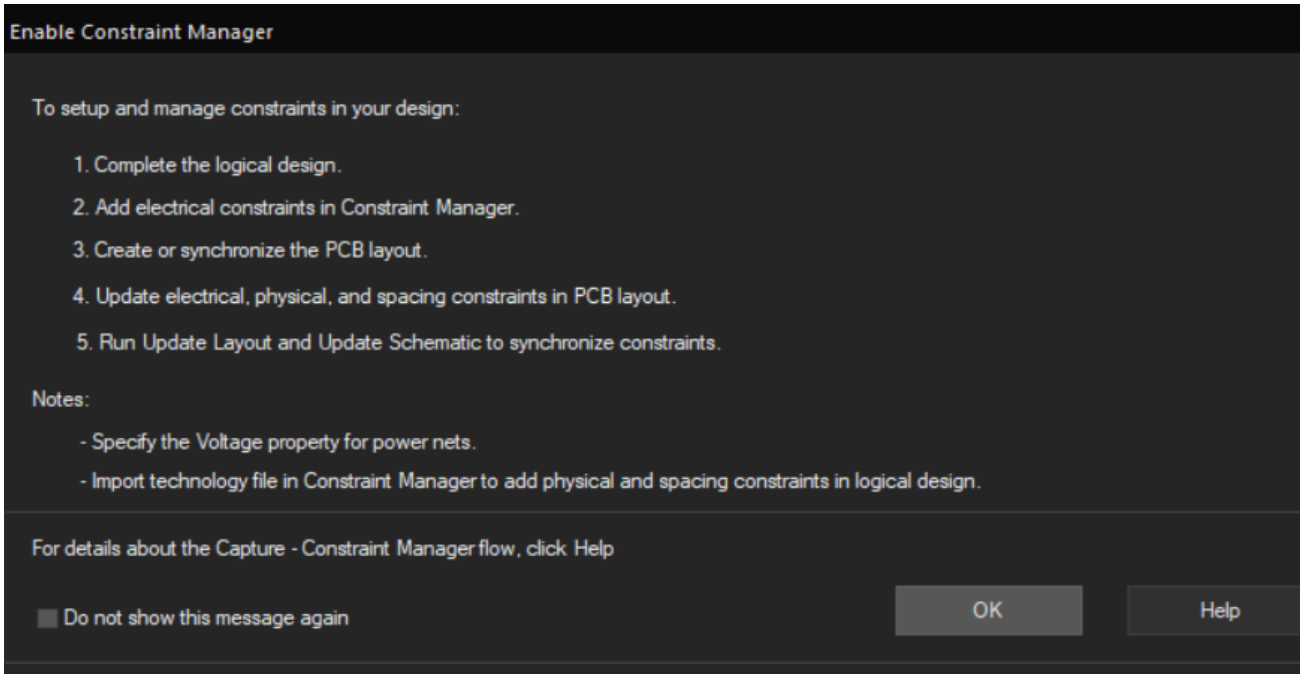
You specify the minimum value of the total etch length of each net in Constraint Manager launched from Capture.

To add this electrical constraint in the schematic design, do the following:

1. Select *PCB – Constraints Manager* or click the CM icon ( ) on the PCB toolbar.

   An information window appears to explain the Capture-Constraint Manager flow.

Enable Constraint Manager window



2. Click *OK*.

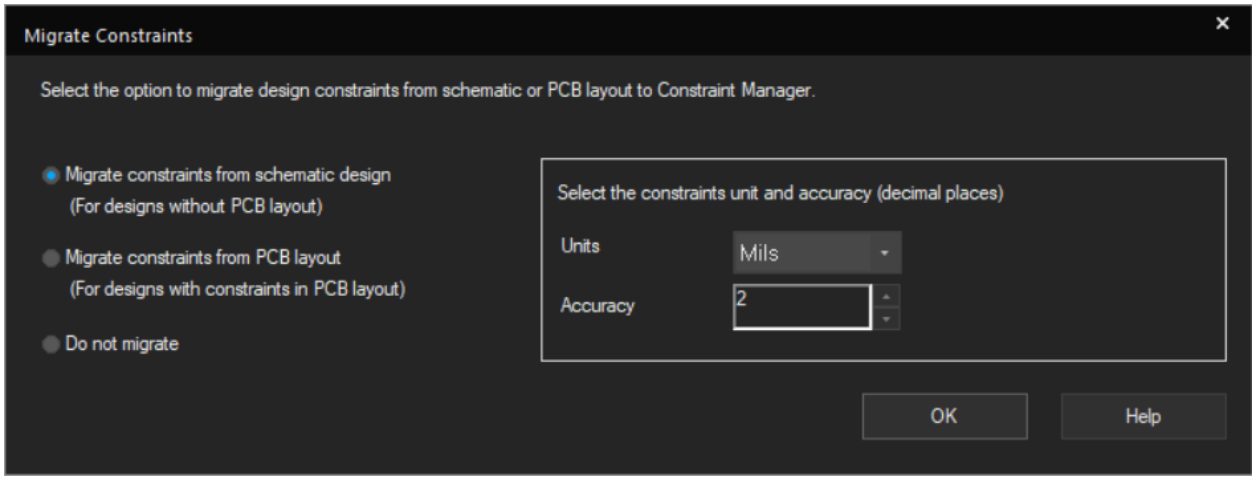
   The *Migrate Constraints* dialog box appears.

3. Select *Migrate constraints from schematic design*.

4. Specify the unit to be used for physical and spacing constraints in the Constraint Manger window.

   PCB Editor uses `Mils` as the default unit. For this tutorial, select `Mils` from the *Units* drop-down list.

Using option to migrate constraints from schematic design



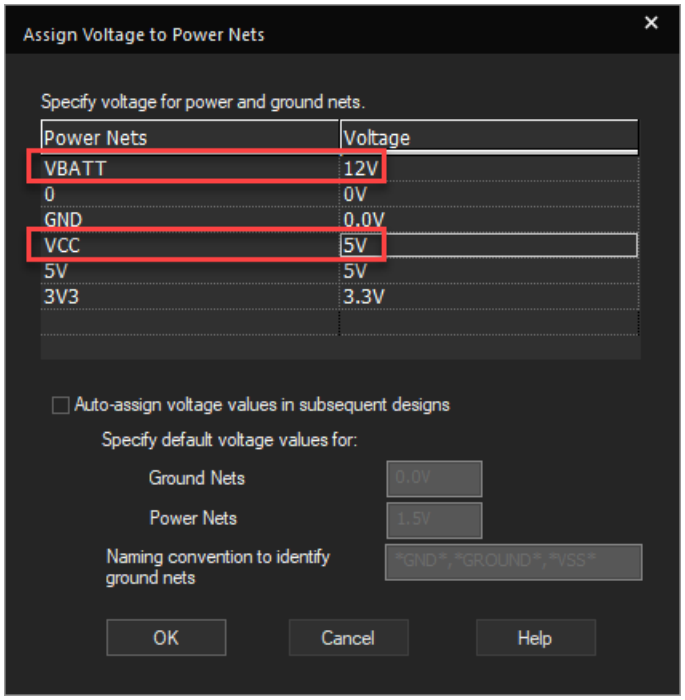
5. Click *OK*.

The Assign Voltage to Power Nets window opens. This has predefined voltage values for all the power nets.

6. Modify these voltage values as follows:

- `VBATT = 12V`
- `VCC=5V`

Modifying predefined voltage values

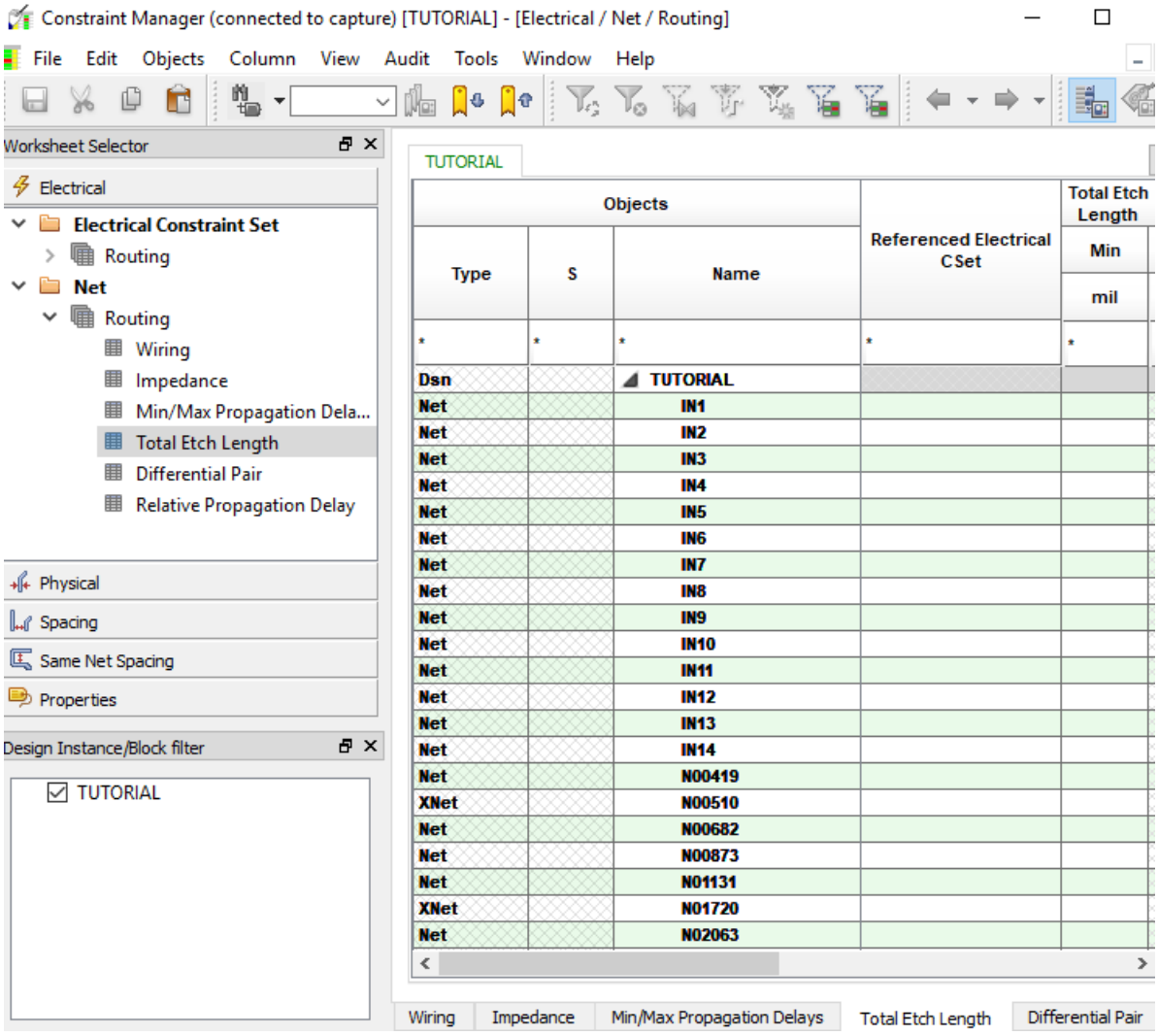


You can also open this dialog box from *SI Analysis – Identify DC Nets*.

7. Click *OK*.

   The Constraints Manager window opens.

Constraint Manager window



8. Specify the minimum total etch length for the `IN1` net as `100` mils as shown in the following figure.

Specifying minimum total etch length value in schematic design

TUTORIAL

Objects			Referenced Electrical CSet	Total Etch Length		
Type	S	Name		Min	Actual	Margin
				mil	mil	mil
*	*	*	*	*	*	*
Dsn		TUTORIAL				
Net		IN1		100.00		
Net		IN2				
Net		IN3				
Net		IN4				
Net		IN5				
Net		IN6				
Net		IN7				
Net		IN8				
Net		IN9				
Net		IN10				
Net		IN11				
Net		IN12				
Net		IN13				
Net		IN14				
Net		N00419				
XNet		N00510				
Net		N00682				

9. To specify the same value for *Total Etch Length* in all the nets, select the next row up till the last net in this window. Release the mouse and specify `100` in the last row.

All the nets and Xnets in the design are assigned the same value.

TUTORIAL

Objects			Referenced Electrical CSet	Total Etch Length		
Type	S	Name		Min	Actual	Margin
				mil	mil	mil
*	*	*	*	*	*	*
Dsn		TUTORIAL				
Net		IN1		100.00		
Net		IN2		100.00		
Net		IN3		100.00		
Net		IN4		100.00		
Net		IN5		100.00		
Net		IN6		100.00		
Net		IN7		100.00		
Net		IN8		100.00		
Net		IN9		100.00		
Net		IN10		100.00		
Net		IN11		100.00		
Net		IN12		100.00		
Net		IN13		100.00		
Net		IN14		100.00		
Net		N00419		100.00		
XNet		N00510		100.00		
Net		N00682		100.00		
Net		N00873		100.00		
Net		N01131		100.00		
XNet		N01720		100.00		
Net		N02063		100.00		
Net		N02685		100.00		
Net		N03504		100.00		
Net		N03592		100.00		
XNet		N04181		100.00		
XNet		OUT1		100.00		
Net		OUT2		100.00		
Net		OUT3		100.00		
Net		OUT4		100.00		
Net		OUT5		100.00		
Net		OUT6		100.00		
Net		OUT7		100.00		
Net		OUT8		100.00		
Net		OUT9		100.00		
Net		OUT10		100.00		

10. Save the design.

Summary

This section covered the steps for preparing the schematic design for designing the physical layout of the PCB board. In the process, you were introduced to tasks, such as placing

connectors, adding footprint information, and adding electrical constraints using Constraint Manager.

5

Creating a Board Design

After the logic design is completed, the next step is to create the layout of the PCB. This section walks you through the basics of the layout creation steps, such as placement, routing, and generating output data to create a layout of the fan-control module design in the PCB Editor.

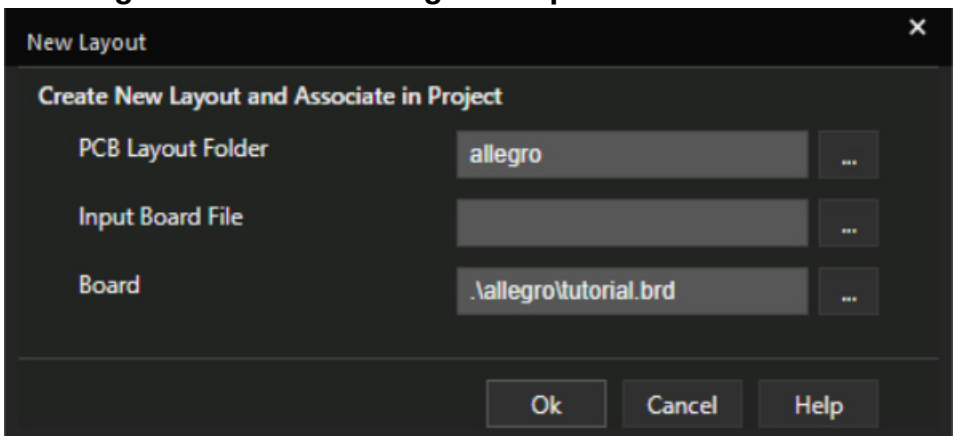
In this section, you will learn how to create a layout design `tutorial.brd` for the logic design you created and simulated in the previous sections.

Creating a Blank Board

The first task is to create a new blank board design. Perform the following steps to create a blank board design:

1. Open `tutorial.opj` in OrCAD X Capture.
2. Choose *PCB – New Layout*.

Creating a blank board design in Capture



The new board design will be created in the default PCB Layout folder `allegro` inside the working project directory.

3. To create a blank board design, leave the *Input Board File* name field blank.

4. Specify the output board file name as `tutorial` and click *OK*.

   The *Cadence Product Choices* dialog box is displayed.

5. Select the *OrCAD PCB Designer Professional* w/*PSpice* option and click *OK*.

   A blank design `tutorial.brd` is opened in PCB Editor. The logic design data is transferred to the layout and is saved in the `allegro` directory.

Creating Design Outline

Design outline specifies the boundary within which components can be placed. It is necessary to create a design outline when transferring design data for ECAD-MCAD evaluation.

1. In PCB Editor, choose *Outline – Design*.

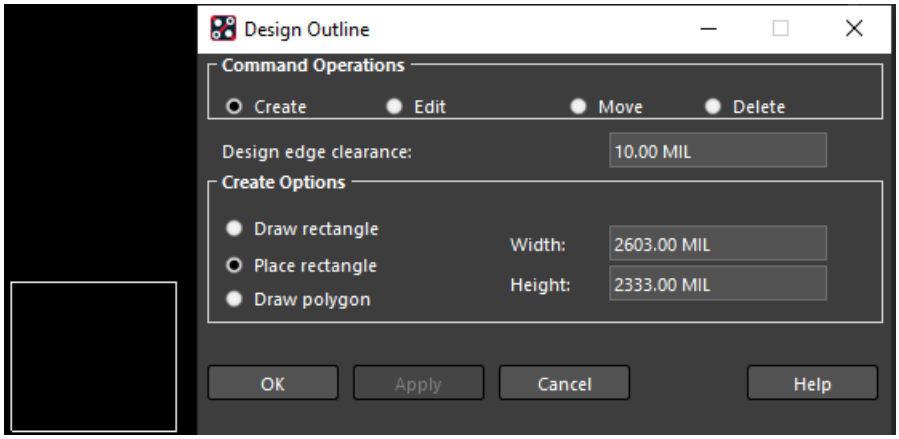
   The *Active Class and Subclass* fields are by default set to *Board_Geometry* and *Design_Outline* in the Options tab.

2. In the Design Outline dialog box, select *Place rectangle* and set *Width* and *Height* values to `2603` and `2333 mils`, respectively.

3. Set *Design edge clearance* value to `10 mils`. This value defines the space between the board outline and package and route keepin boundaries which is required to accommodate manufacturing tolerances, testing, and assembly.

   A rectangular design outline is attached to the cursor.

Setting up design outline parameters



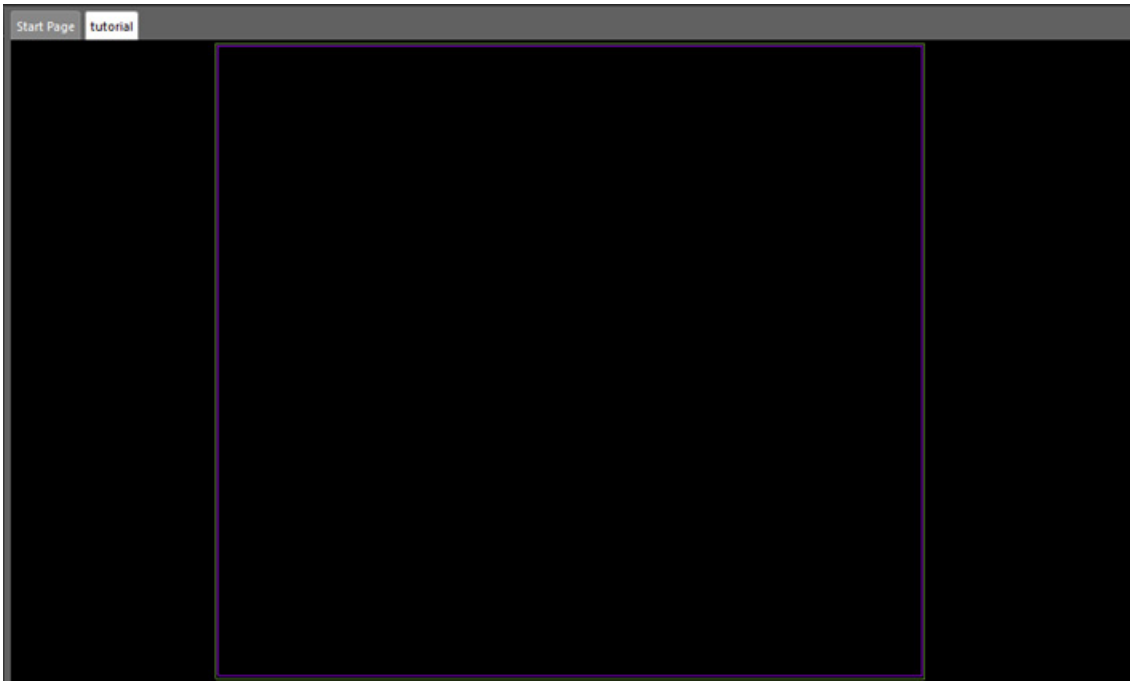
4. Click anywhere in the design canvas to place the outline.

5. Click *OK* to close the *Design Outline* dialog box.

   A rectangular board outline is created with package and route keepin areas.

6. To view the entire board in the design canvas, choose *Display – Zoom – Fit* to center the board outline in the design window.

Design outline with package and route keepin areas



7. Choose *File – Save* to save the design.

Placing Components

After creating the design outline you can start with component placement. All types of component symbols (discrete, ICs, mechanical, and format) can be placed either manually or by using automatic placement in the PCB Editor.

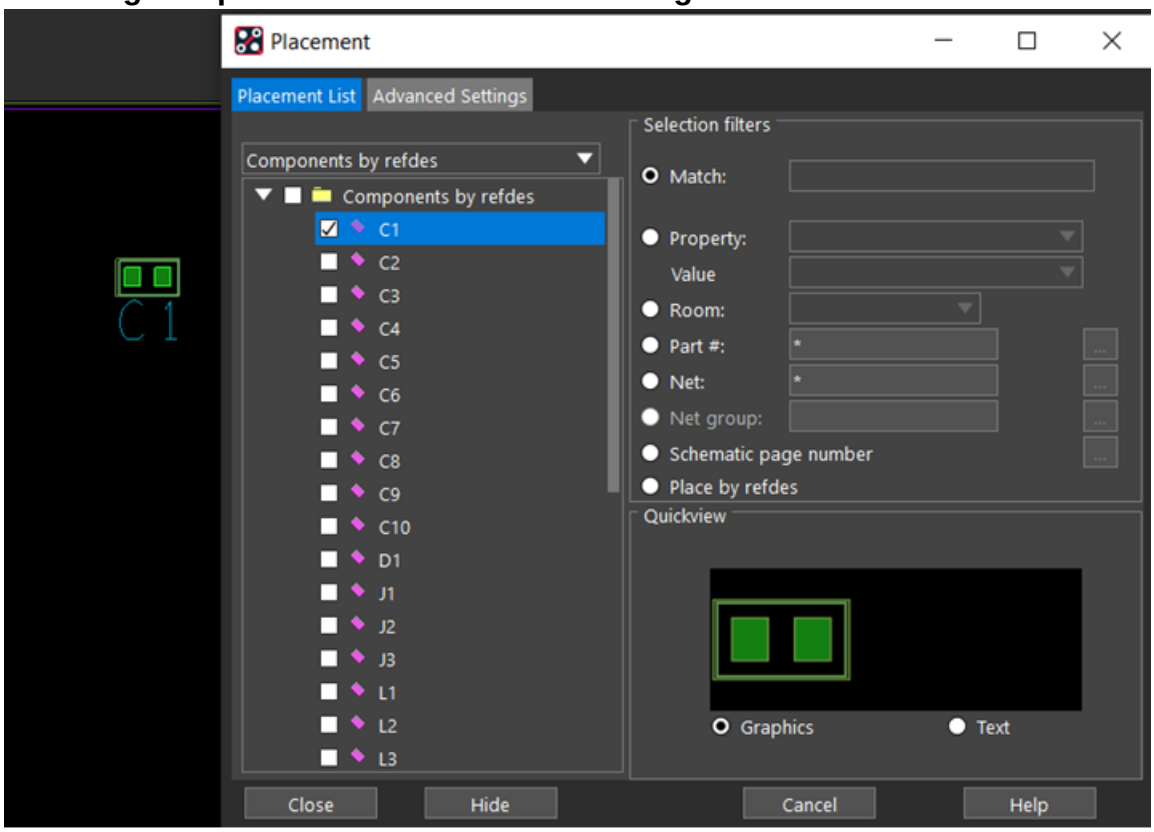
For this tutorial, place components interactively using the `place manual` command either in horizontal or vertical orientation using standard grid size of `25 mil`, which makes them easy to align and assemble on the board.

1. To start the placement, first enable the placement editing environment. Choose *Setup – Application Mode – Placement Edit*.

2. Choose *Place – Components Manually*.

By default, *Placement* dialog box shows all the components listed by their reference designators. You can choose any reference designator and place it in the design canvas.

Selecting components from Placement dialog box

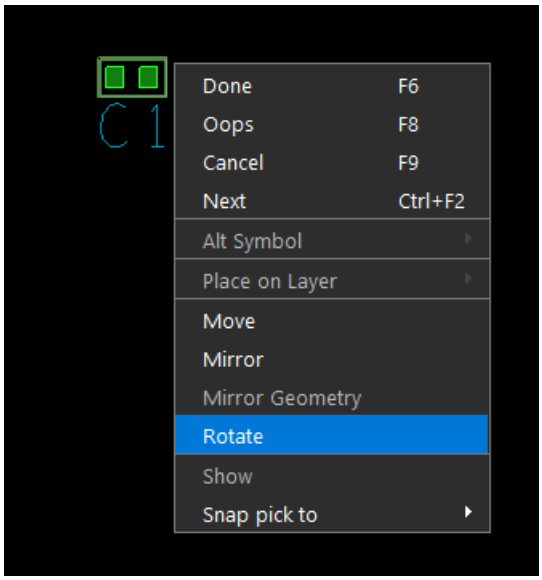


3. Select the capacitor symbol `C1`.

   The symbol gets attached to the cursor and is also visible in the Quickview window.

4. Right-click to choose *Rotate.* Use the handlebar to rotate the symbol by `90` degrees in anti-clockwise direction.

Rotating component before placing



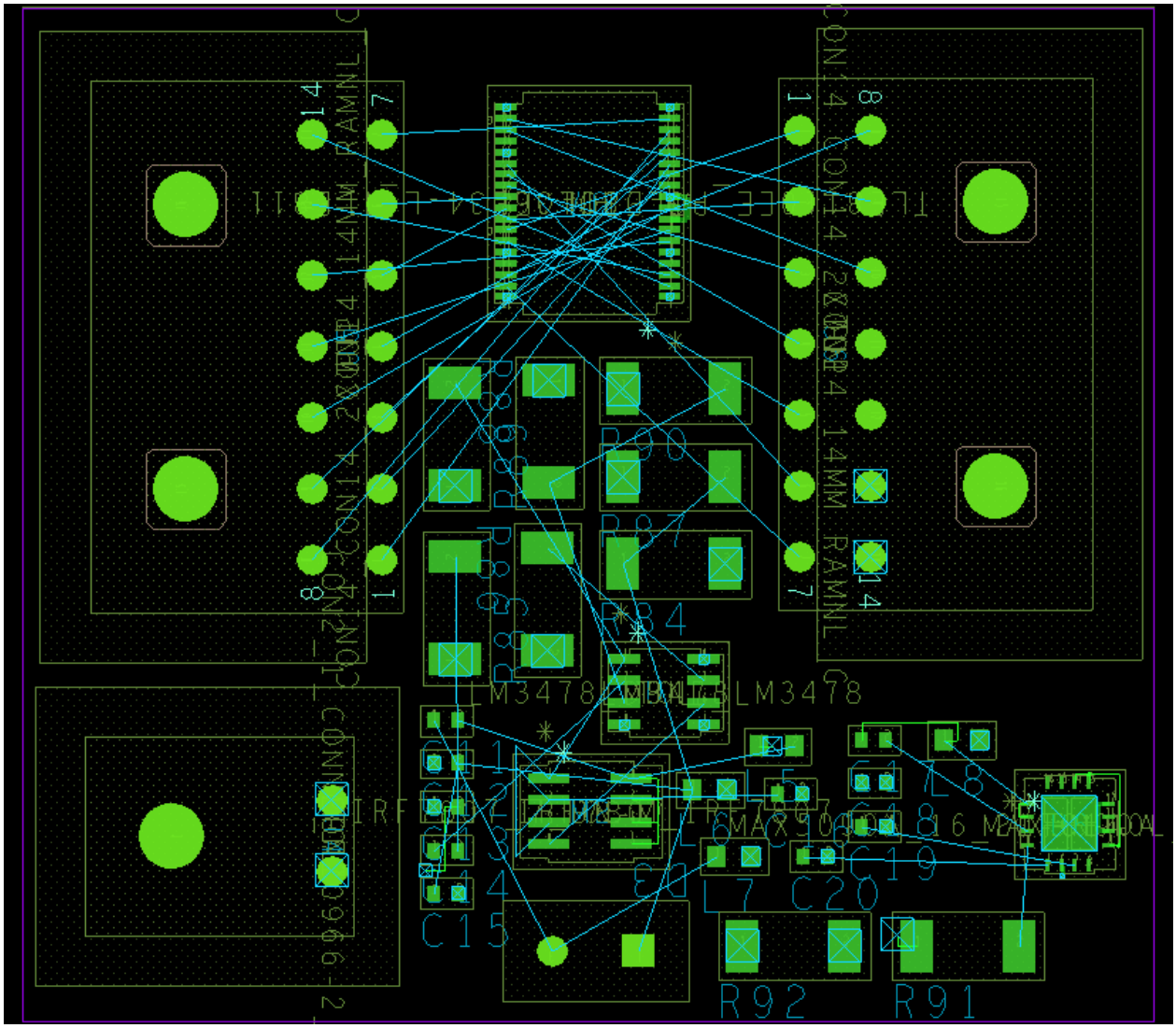
5. Left-click in the design canvas to place the capacitor symbol.
6. Similarly, select each reference designator one by one to place all the component symbols.

Tip

Place the symbols according to their logically connectivity. You can refer to schematic design to know which components are logically connected and must be placed closely.

The following image depicts a sample placement.

Sample placement



7. Choose *File – Save* to save the design.

Note: The placement is the most important step of the PCB design and impact all the subsequent steps of the layout design. If you choose to place components differently, the final routed board will also be different.

Setting Up Constraints

To meet manufacturing requirements you can configure the default constraint values in Constraint Manager either by creating constraint sets or by directly modifying the constraint values.

Before routing the board, specify the design constraints for routing. For this tutorial, specify two constraints for routing power nets: minimum thickness of the cline and maximum length of cline in neck mode.

1. Choose *Setup – Constraints.*
2. In the *Physical* domain, choose *Net – All Layers.*
3. In the *All Layers* worksheet, select the net `5V`.
4. Change the value of *Min Line Width* to `15 mil` and *Max Neck Length* to `100 mil`.
5. Similarly, select the nets `3V3` and `0` and change the values for *Min Line Width* and *Max Neck Length.*

   New values are displayed in blue color for the power nets. When routing, any violation to these values will create a DRC error.

Setting overrides for physical constraints

Objects			Referenced Physical CSet	Line Width		Neck	
Type	S	Name		Min	Max	Min Width	Max Length
				mil	mil	mil	mil
*	*	*	*	*	*	*	*
Net		OUT10	DEFAULT	5.00	0.00	5.00	0.00
Net		VBATT	DEFAULT	5.00	0.00	5.00	0.00
Net		0	DEFAULT	15.00	0.00	5.00	100.00
Net		3V3	DEFAULT	15.00	0.00	5.00	100.00
Net		5V	DEFAULT	15.00	0.00	5.00	100.00

6. Close Constraint Manager.
7. Choose *File – Save* to save the design.

Routing Nets

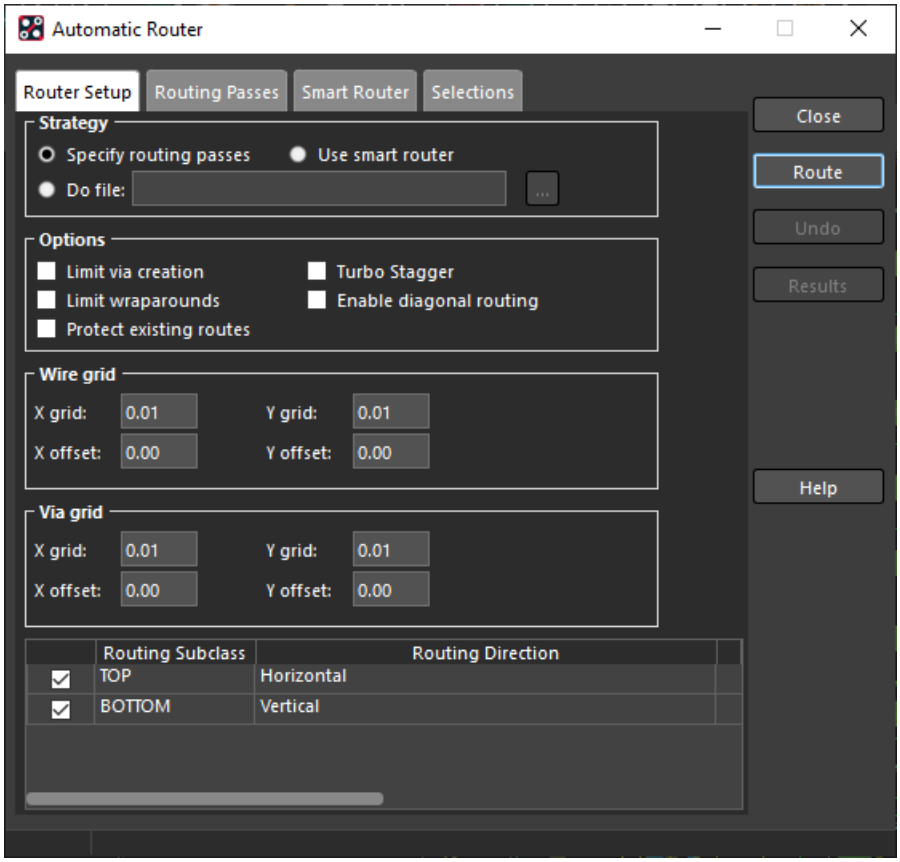
Connecting the components in a layout is called routing. PCB Editor provides both manual and auto routing capabilities.

For this tutorial, use smart router for complete auto-routing.

1. Choose *Route – PCB Router – Route Automatic.*

   The *Automatic Router* dialog box opens and shows options to configure parameters for routing. For this tutorial, use the default values.

Automatic Router setup dialog box

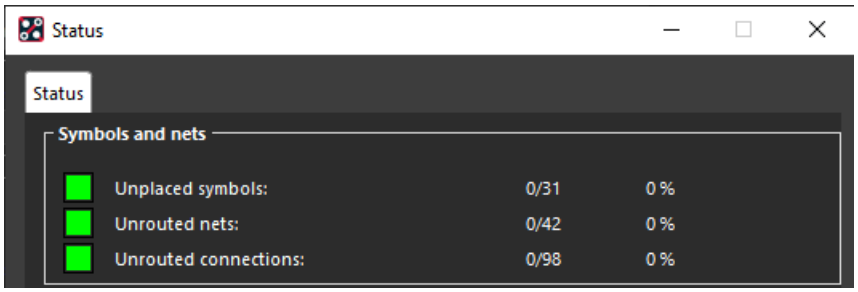


2. To start auto-routing, click the *Route* button.

   The auto-route process starts and takes a few seconds to complete. The auto-router considers the design outline and keepin areas while routing nets.

3. To verify that routing is completed successfully, choose *Check – Design Status*.

Status dialog box

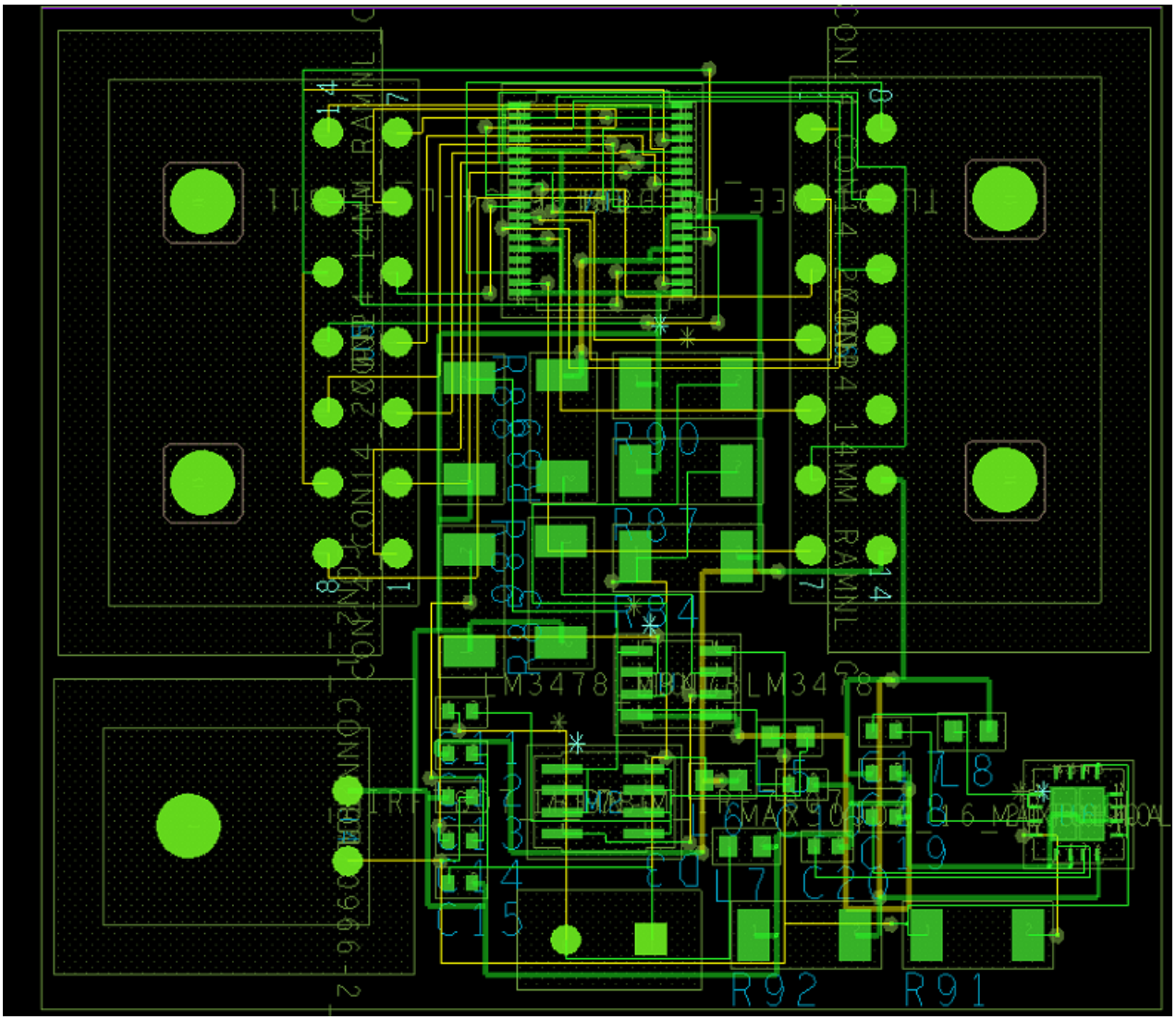


The *Status* dialog box confirms that all the nets are routed.

4. Click *OK* to close the *Status* dialog box.
5. Close the *Automatic Router* dialog box.

   The following image shows a routed board design.

Auto-routed board design sample



6. Choose *File – Save* to save the design.

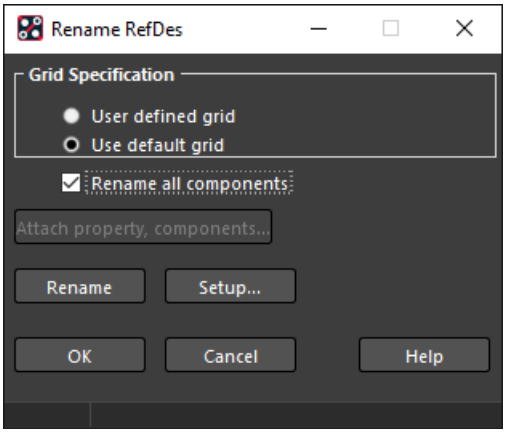
Renaming Components

After you have completed the placement and routing you can reorder the reference designators of components on the board in a specific pattern. This steps makes the testing and assembly process easier.

1. Choose *Manufacture – Auto Rename Refdes – Rename*.

   The *Rename Refdes* dialog box opens showing grid settings and option to select all the components for renaming action.

Rename Reference Designators options



2. Click the *Setup* button to specify more options.

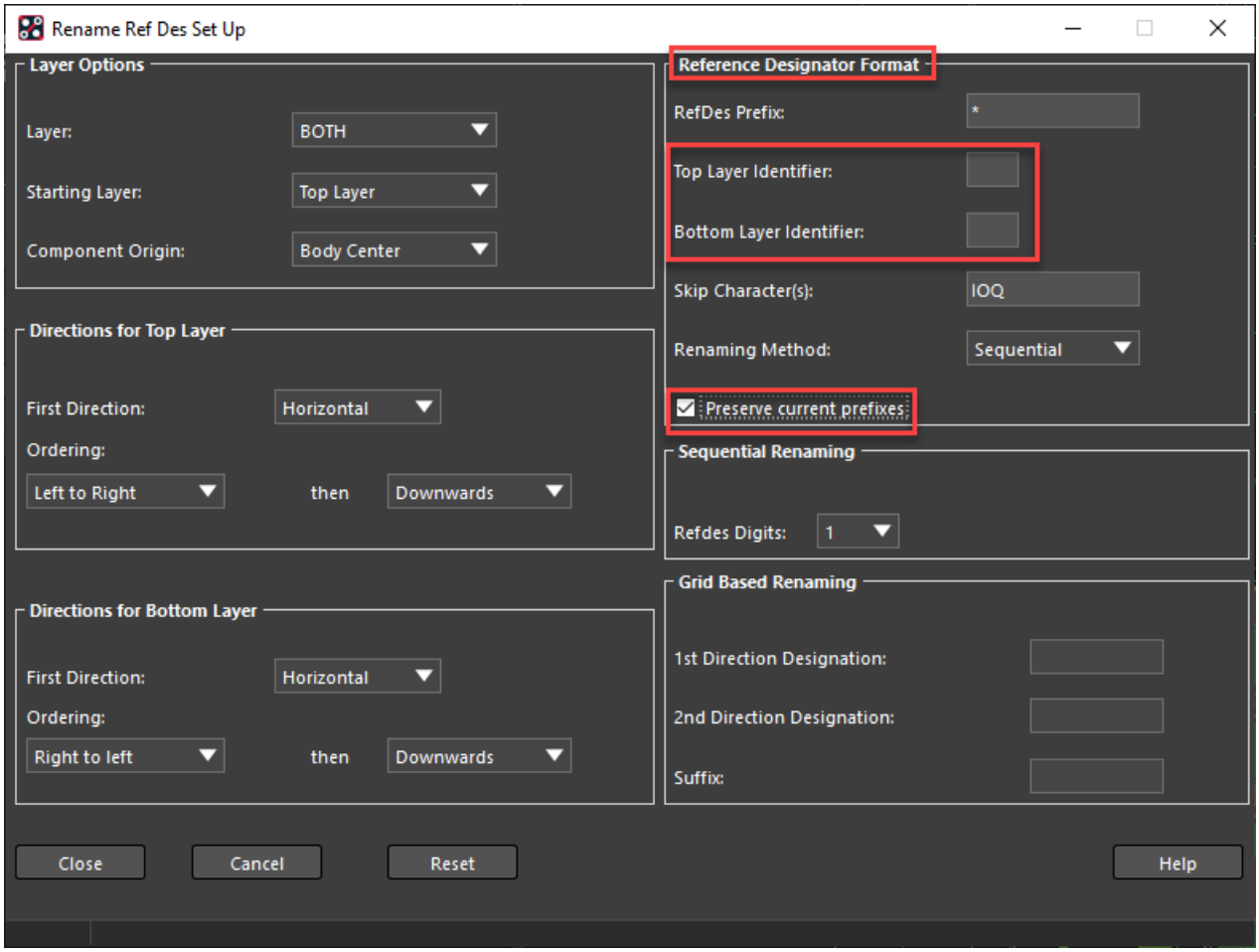
   The *Rename Ref Des Set Up* dialog box opens.

3. In the *Reference Designator Format* section:

   a. Remove layer identifier for `TOP` and `BOTTOM` layers.

   b. Enable the *Preserve Current prefixes* check box.

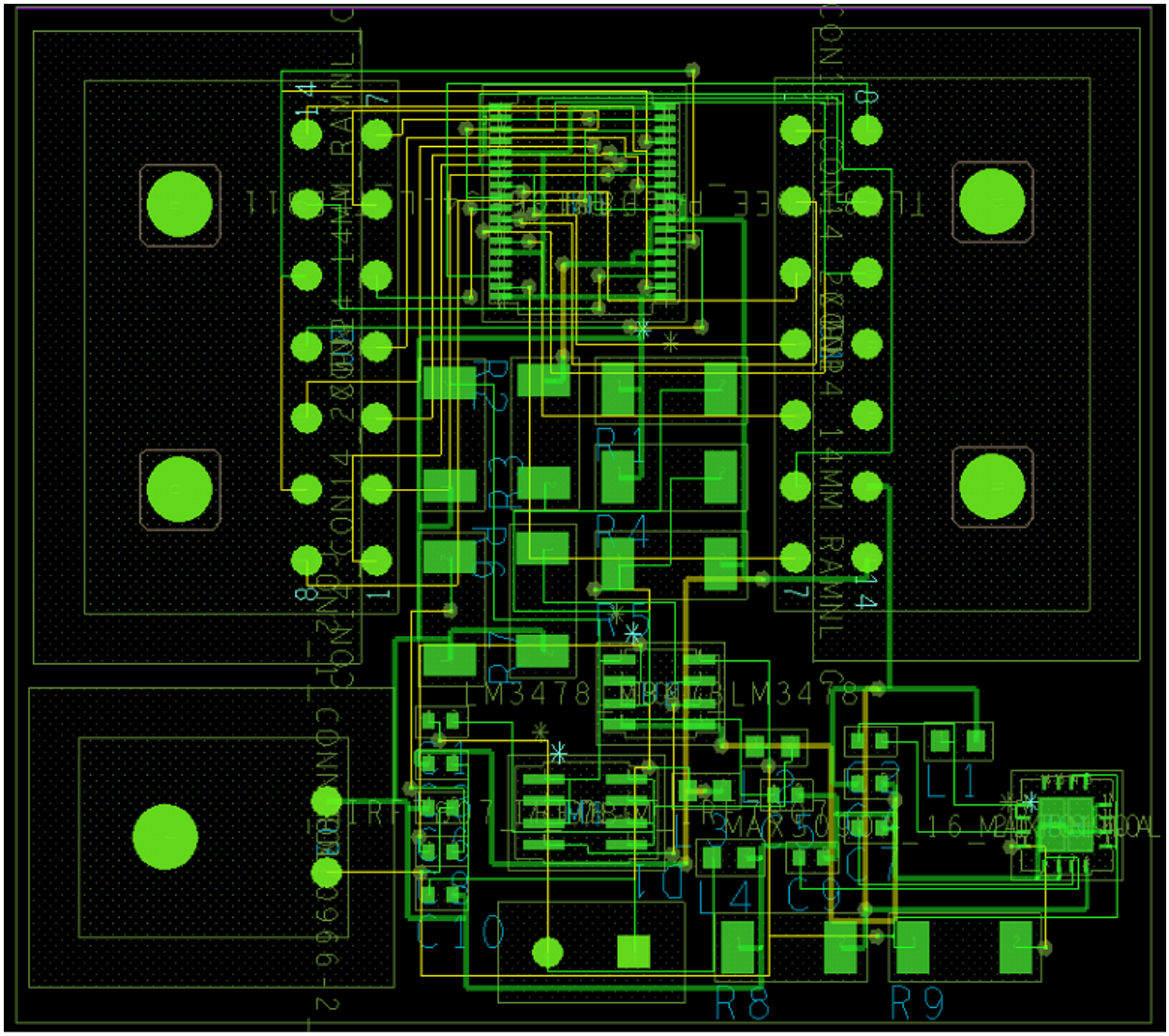
Rename Reference Designator Set Up dialog box



4. Close the *Rename Ref Des Set Up* dialog box.
5. Click the *Rename* button in the *Rename RefDes* dialog box.

   Renaming of reference designators starts from the upper-left corner of the board in the horizontal direction and the numbers are increasing in the downward direction.

Board design with renamed reference designators



6. Click *OK* to close the Rename RefDes dialog box.
7. Choose *File – Save* to save the design.

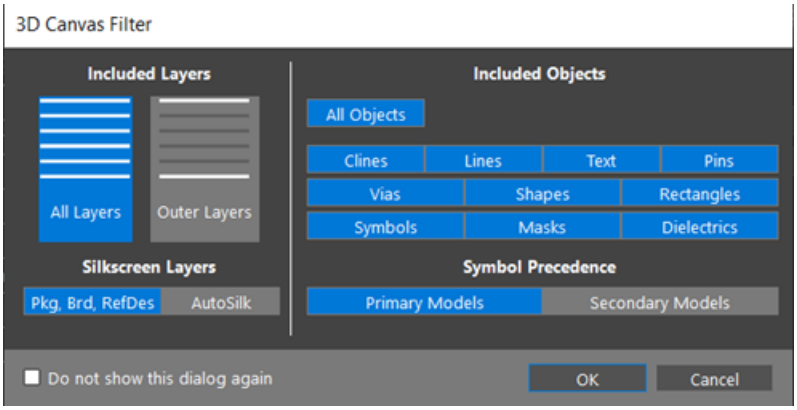
Visualizing Design in 3D

The built-in 3D visualization tool of PCB Editor lets you preview the board design at any time during the design. You can open the design in 3D Canvas and verify the design as a complete assembly.

To analyze the design in the 3D Canvas, 3D models must be assigned to all the symbols. You can map a 3D model either at a symbol level or at the design level. PCB Editor, by default, supports STEP models for 3D visualization. For the components used in this tutorial, 3D models are assigned at the symbol level.

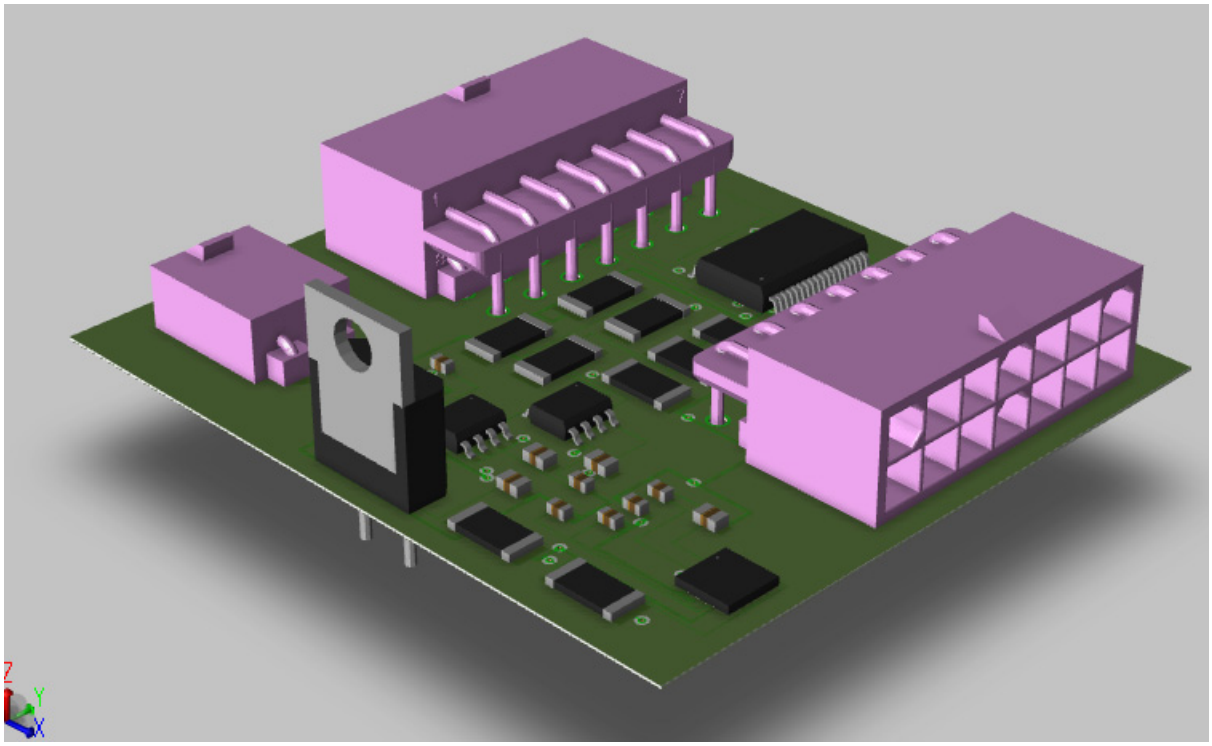
1. Choose *Display – 3D Canvas*.

   A *3D Canvas Filter* dialog box opens. Click *OK* to proceed.



   A progress bar displays while loading the design into 3D Canvas.

3D view of board design



2. Choose *View – Camera* options to view the design in different perspectives.
3. Close 3D Canvas.

Generating Manufacturing Files

The final task is to generate various types of output files of the physical design data. You can create Gerber files, Excellon NC Drill files, DXF files, IPC2581, ODB++, and printer/plotter files.These files are standard files and are required by the fabrication houses to manufacture a PCB.

For this tutorial, create three types of output files:

- Artwork (Gerber)
- NC Drill
- IPC2581

Creating Artwork

To create artwork files, PCB Editor reads film control records to determine the number of artwork files to produce, their names, and list of classes and subclasses to include in each artwork file.

To specify classes and subclasses for an artwork file, use *Color Dialog* to set the visibility of required classes and subclasses.

1. Choose *Setup – Colors.*

   The *Color Dialog* opens.

2. In the *Layers* tab, click the *Off* button for *Global Visibility*.

   The visibility of all the classes and subclass are turned off.

3. Expand the *Stack-Up – Conductor* folder, select `Soldermask_Top` and `Pastemask_Top` layers and enable the check box for *Pin* only.

   The soldermask and pastemask layers of pins becomes visible in the design canvas.

4. Similarly, in the *Geometry* folder, select `Soldermask_Top` and `Pastemask_Top` layers and enable the check box for *All* objects.

   The visibility of soldermask and pastemask layer is set on both board and package geometry.

5. Click *OK* to close the *Color Dialog*.

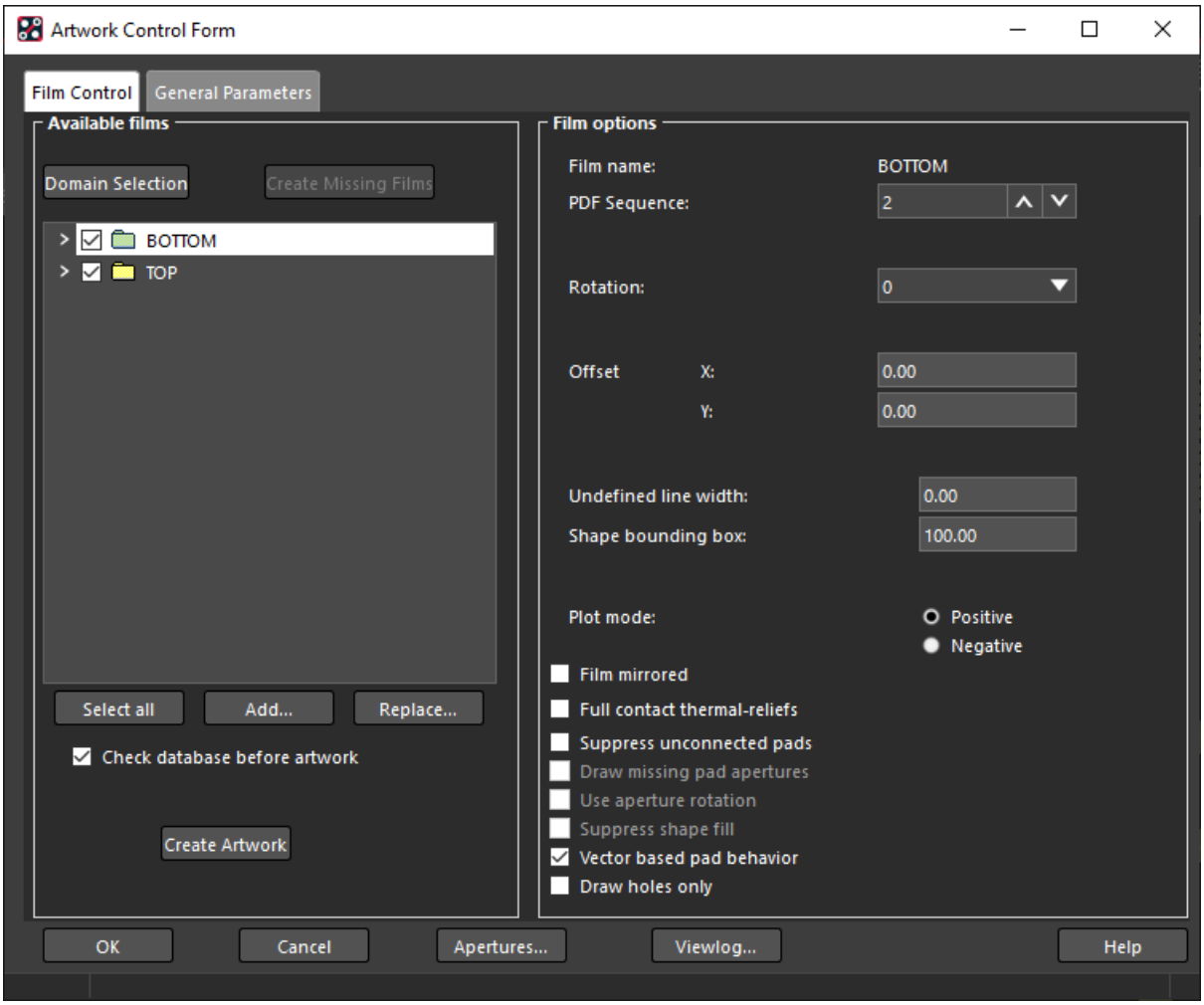
6. Choose *Export – Gerber*.

   The *Artwork Control Form* opens which reads the cross-section and auto-generates one film record for each etch subclass and includes etch, pins, and vias.

7. In *Artwork Control Form*, select both the `TOP` and `BOTTOM` layers.

8. Click *Create Artwork* to generate artwork.

Artwork generation settings



Two artwork files (`TOP.art` and `BOTTOM.art`) are created in the `allegro` directory.

9. Click *Viewlog* to review the log file.
10. Click *OK* to close the *Artwork Control Form*.

Creating NC Drill

NC Drill output files are created for numerically-controlled (NC) drills and router and helps in assessing the cost of PCB manufacturing. The drill output files include drill legend tables and drill files.

Generating Drill Legend

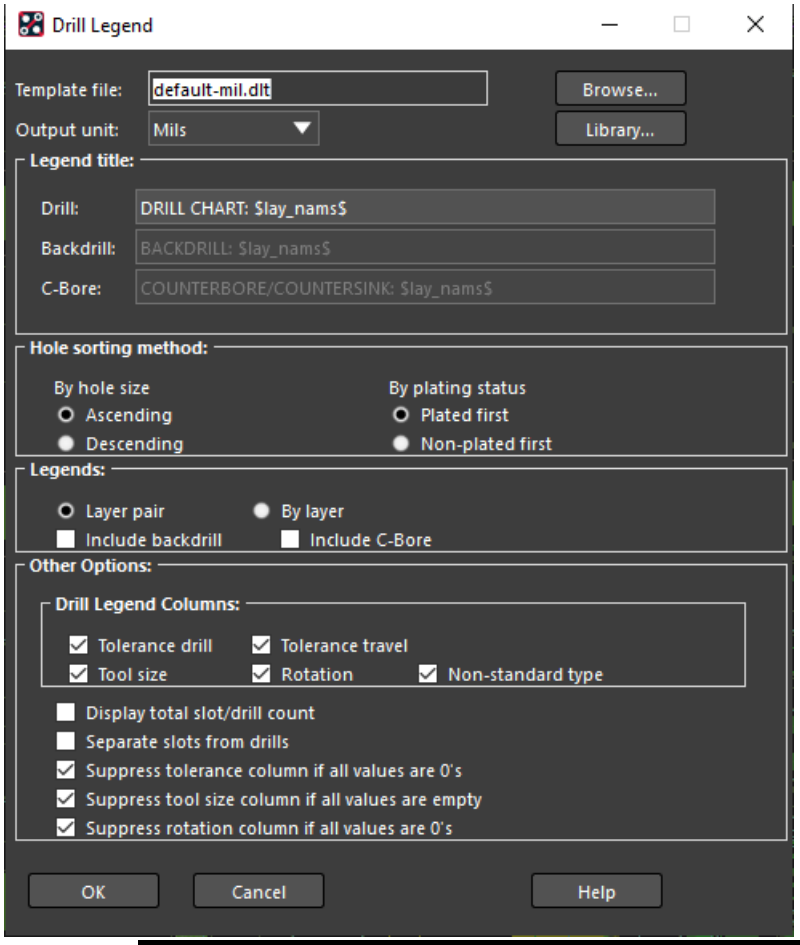
Drill legend tables are used in fabrication drawing and show the number, type, and tolerance of plated and non-plated holes in the design.

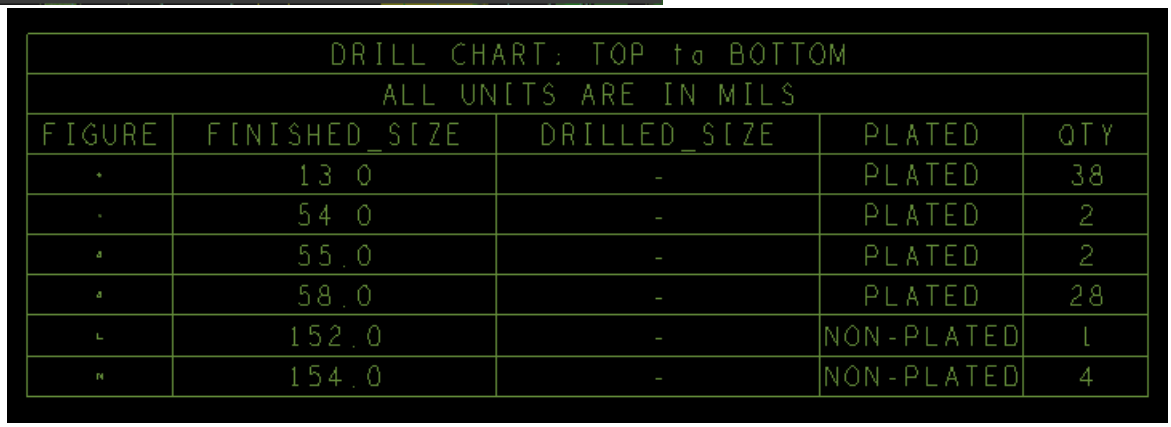
1. Choose *Setup – Colors,* click *On* to enable *Global Visibility* and click *OK* to close the dialog box.
2. Choose *Manufacture – Create Drill Table.*

   The *Drill Legend* dialog box opens.
3. Click *OK* to generate the drill legend symbol.

   The drill legend symbol gets attached to the cursor.
4. Left-click to place the drill legend in the design canvas.

Drill Legend parameters and table





DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	FINISHED_SIZE	DRILLED_SIZE	PLATED	QTY
•	13.0	-	PLATED	38
·	54.0	-	PLATED	2
▲	55.0	-	PLATED	2
▲	58.0	-	PLATED	28
⌞	152.0	-	NON-PLATED	1
⌜	154.0	-	NON-PLATED	4

Generating NC Drill

The NC drill file is created based on the parameters specified for the drill coordinate data format.

1. Choose *Export – NC Drill*.

   The *NC Drill* dialog box opens.

2. Click *Parameters* to open *NC Parameters* dialog box.

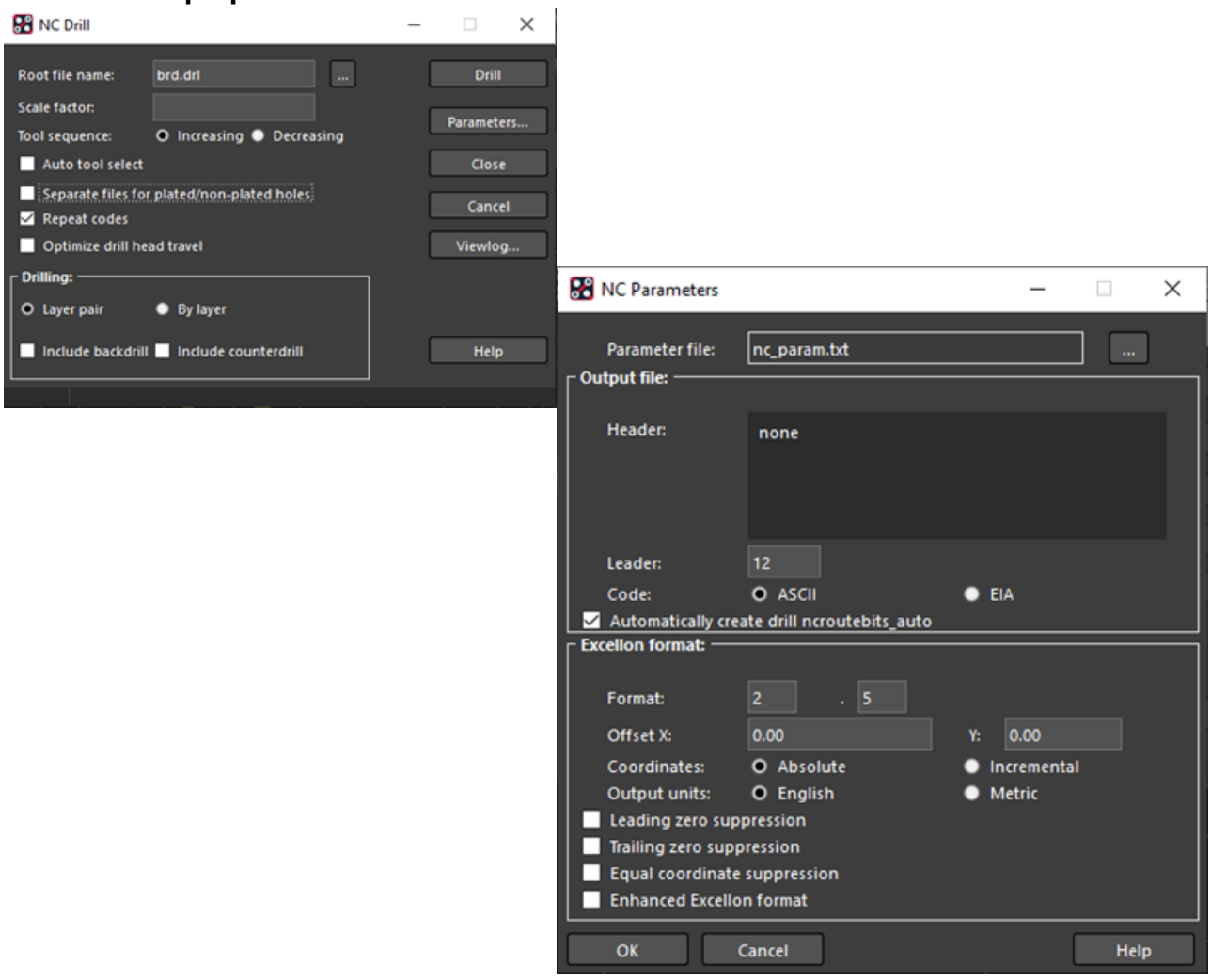
3. Enable the *Enhanced Excellon format* check box.

   A header in the NC Drill and NC Route output files is generated that uses Excellon commands.

4. Click *OK* to save the parameters.

5. Click *Drill* to generate the drill file.

NC Drill setup options



The NC Drill file (`tutorial.drl`) is created in the `allegro` directory.

6. Click *Viewlog* to review the log file.
7. Close the dialog box.

Creating IPC2581 Files

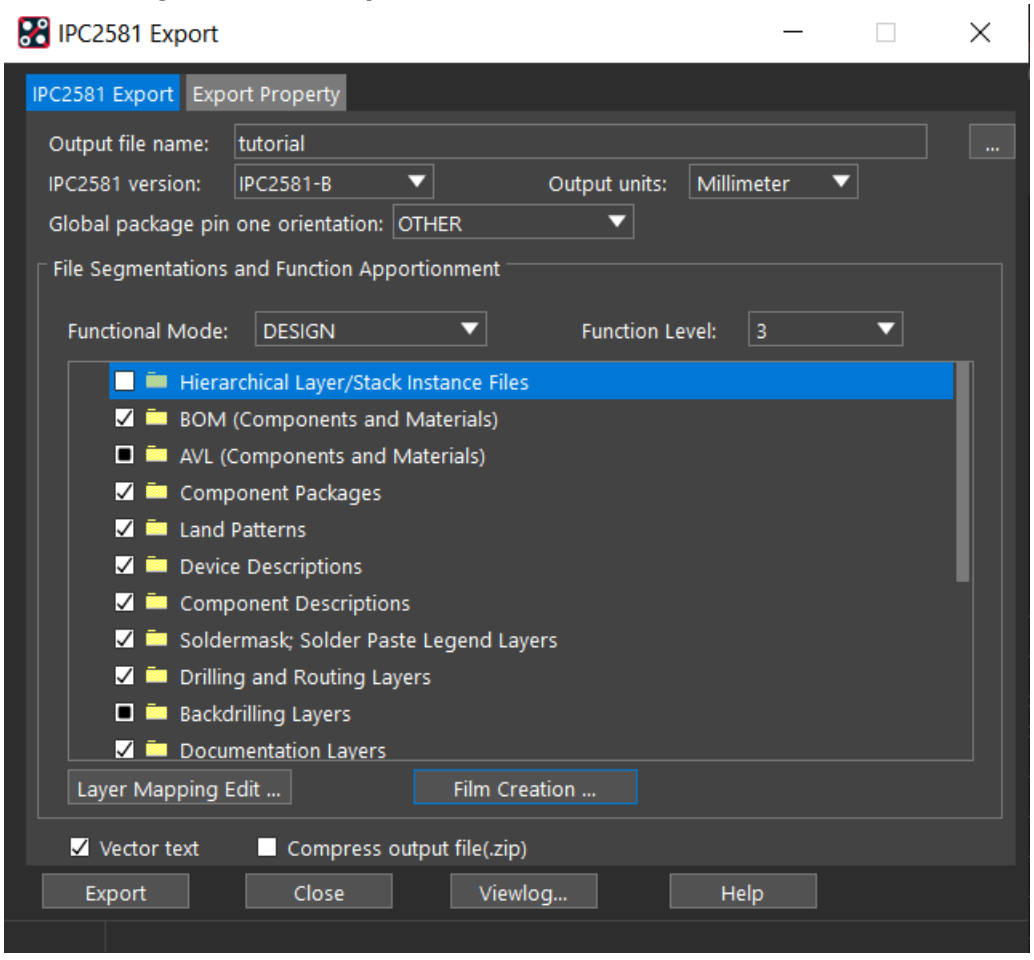
IPC2581 is an XML-based data exchange format used for providing physical design data for fabrication and assembly of PCBs.

For this tutorial, create IPC2581 output using default values.

1. Choose *Export – IPC2581*.

   The *IPC2581 Export* form opens.

Generating IPC2581 output



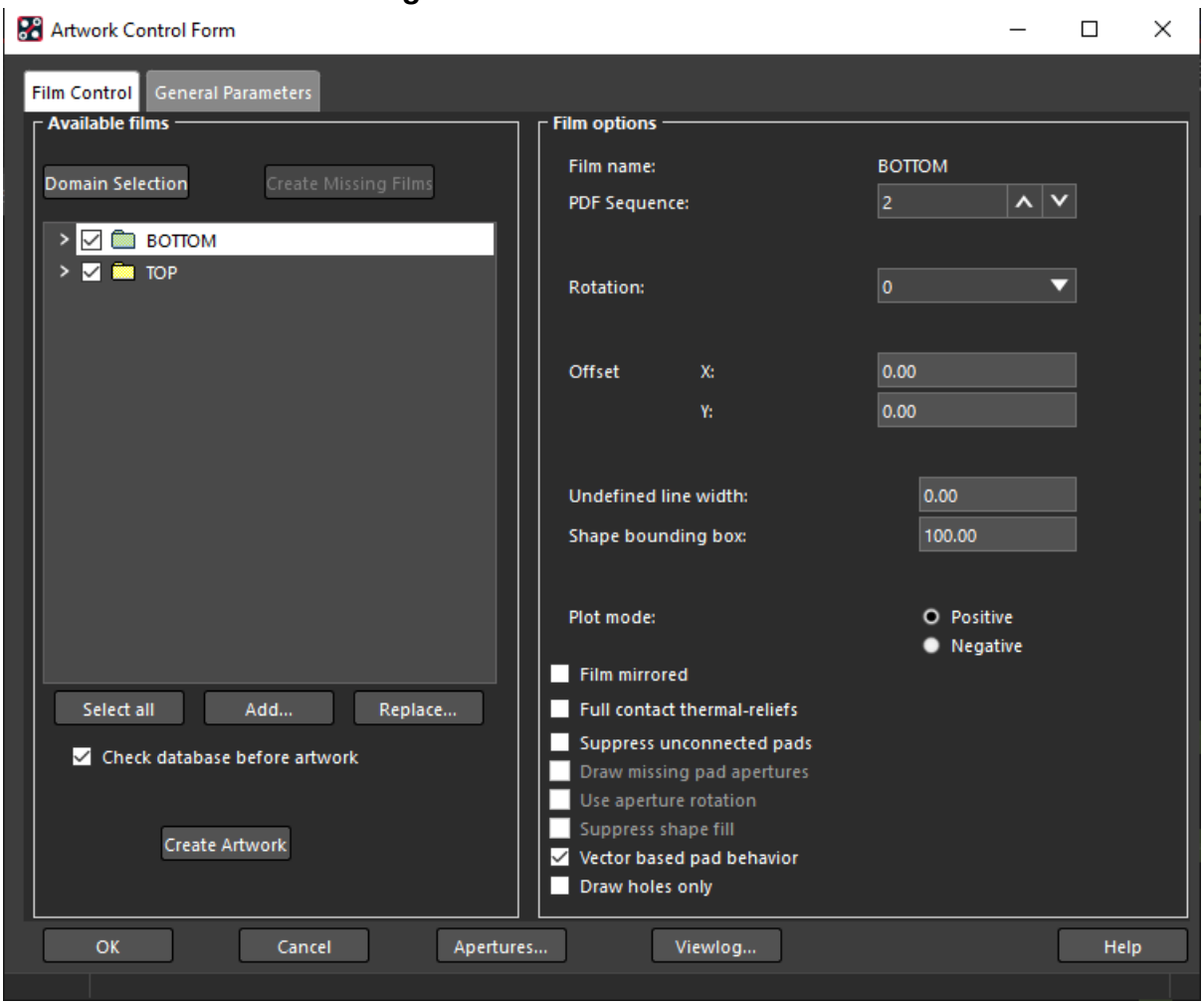
2. Leave the *IPC2581 version* to default, which is set to the latest version *IPC2581-B*.

3. Select *Output units* to `Millimeter`.
4. Set the *Functional Mode* to `DESIGN` and *Level* to `3`.

   Five functional modes are supported and each mode consists of three levels that define the complexity and detail of the output file.
5. Click *Film Creation* to add class and subclass for film records.

   The *Artwork Control Form* opens.
6. Select both the `TOP` and `BOTTOM` layers and click *OK* to close the dialog box.

Film record creation settings

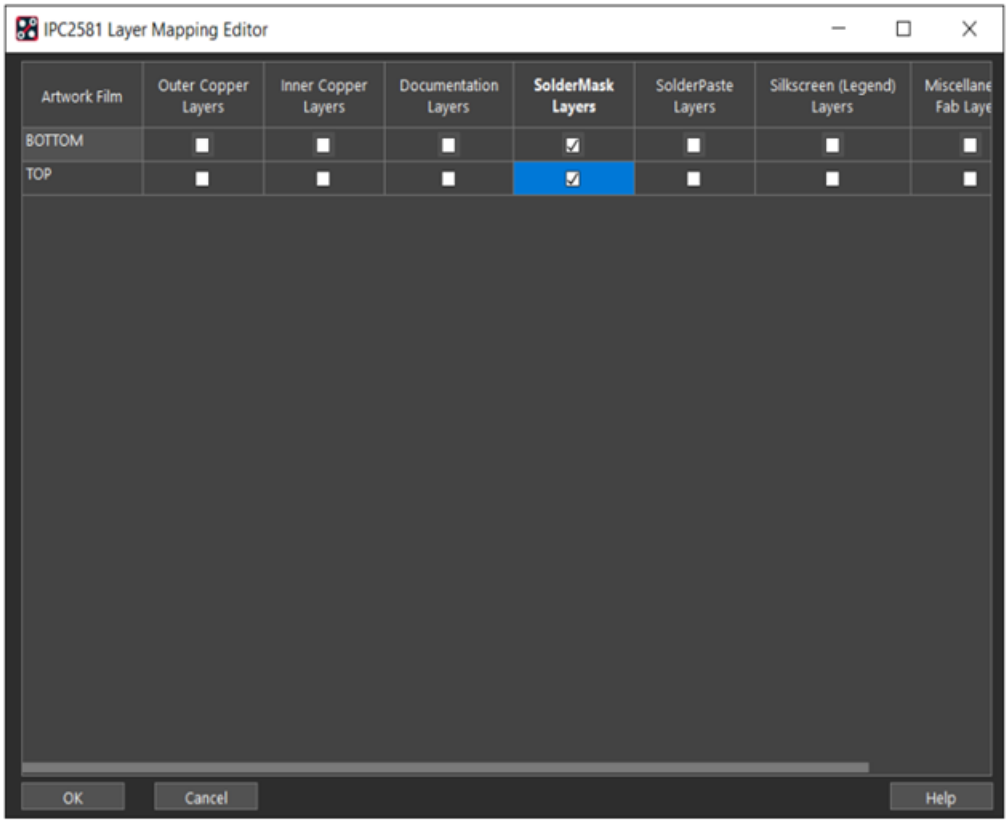


Tip

When exporting IPC2581, it is recommended to enable *Dynamic unused pads suppression* option in Cross-section Editor to suppresses unconnected pads for the selected object types (pin/via) on the selected inner layers.

7. Click *IPC2581 Layer Mapping Editor* to specify layer type for each artwork film.
8. Select the check boxes for *Soldermask Layers* for both the artwork films and click *OK* to close the dialog box.

IPC2581 Layer Mapping Editor



9. To generate IPC2581 file, click *Export*.

   An XML file (`tutorial.xml`) is created in the `allegro` directory.

10. Click *Viewlog* to review the log file.

Summary

This completes the task of creating a board design and generating manufacturing files for the PCB. In this section, you were introduced to the flow of tasks required for creating a board design using PCB Editor. For detail description of layout creation tasks, refer to PCB Editor information set.