cadence®

Allegro® X Layout Editors: What's New in Release 23.1

Product Version 23.1
September 2023

Cadence Design Systems, Inc., 555 River Oaks Parkway, San Jose, CA 95134, USA

Contents

What’s New in 23.1

This document describes the new features and enhancements in Allegro® X PCB Editor and Allegro® X Advanced Package Designer (APD) in release 23.1. If a feature is available in only one of the layout editors or for a specific license, a note is provided.

Migrating Designs and Libraries to Release 23.1

You can open designs and libraries from the following releases without any migration updates and still take advantage of the latest design solutions: 17.2-2016, 17.4-2019, and 22.1.

Note: You must use release 23.1 licenses to run the release 23.1 products. However, 23.1 licenses can be used to run 16.6 or a later release.

If you save a design in release 23.1, it will be saved in the 23.1 database format and will not support compatibility with previous releases. You must run downrev (*File – Export – Downrev Design*) to be able to open the saved design in a previous release.

Library symbols and padstacks saved in release 23.1 are saved to the lowest possible database version to maintain compatibility with early releases with the following exceptions:

- Libraries with padstacks using Secondary Side Countersink or Counterbore or Drilled Hole values can only be used in the 23.1 release.
- Symbols with Hierarchal Route and Via Keepout shapes defined on Outer_Layer, Inner_Signal_Layers and Inner_Plane_Layers layers can only be used in 17.4 or a later release.

By default, you can downrev to the 17.4 database format, but if a design contains Nested Zones, it can only be saved to the 22.1 HotFix 003 (QIR2) database format.

Tip

You can use `dbstat` command to determine the database version of a symbol and padstack used in a library.

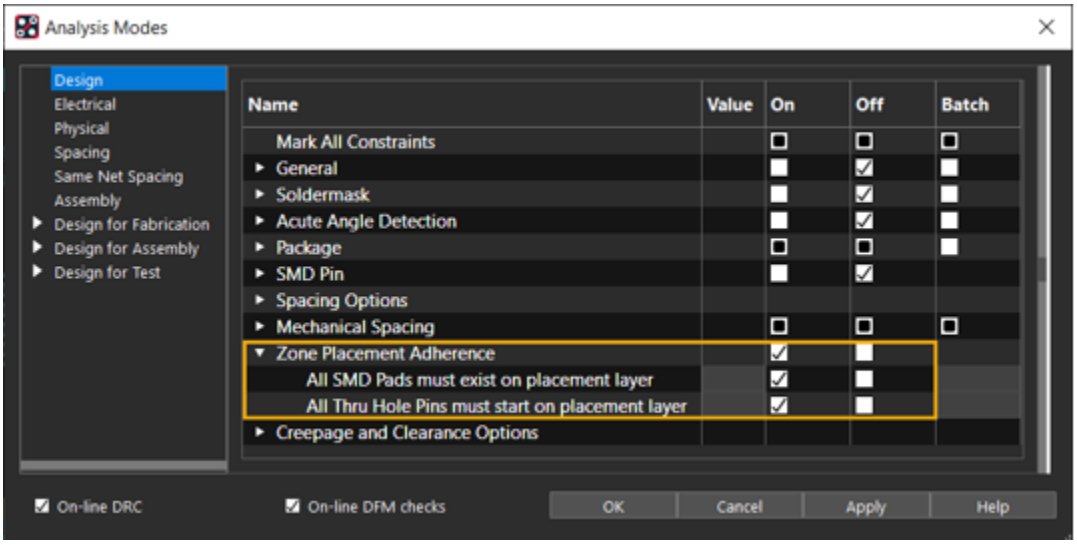
For detailed migration information, see Migration Guide for Allegro X Platform Products.

Rigid-Flex Enhancements

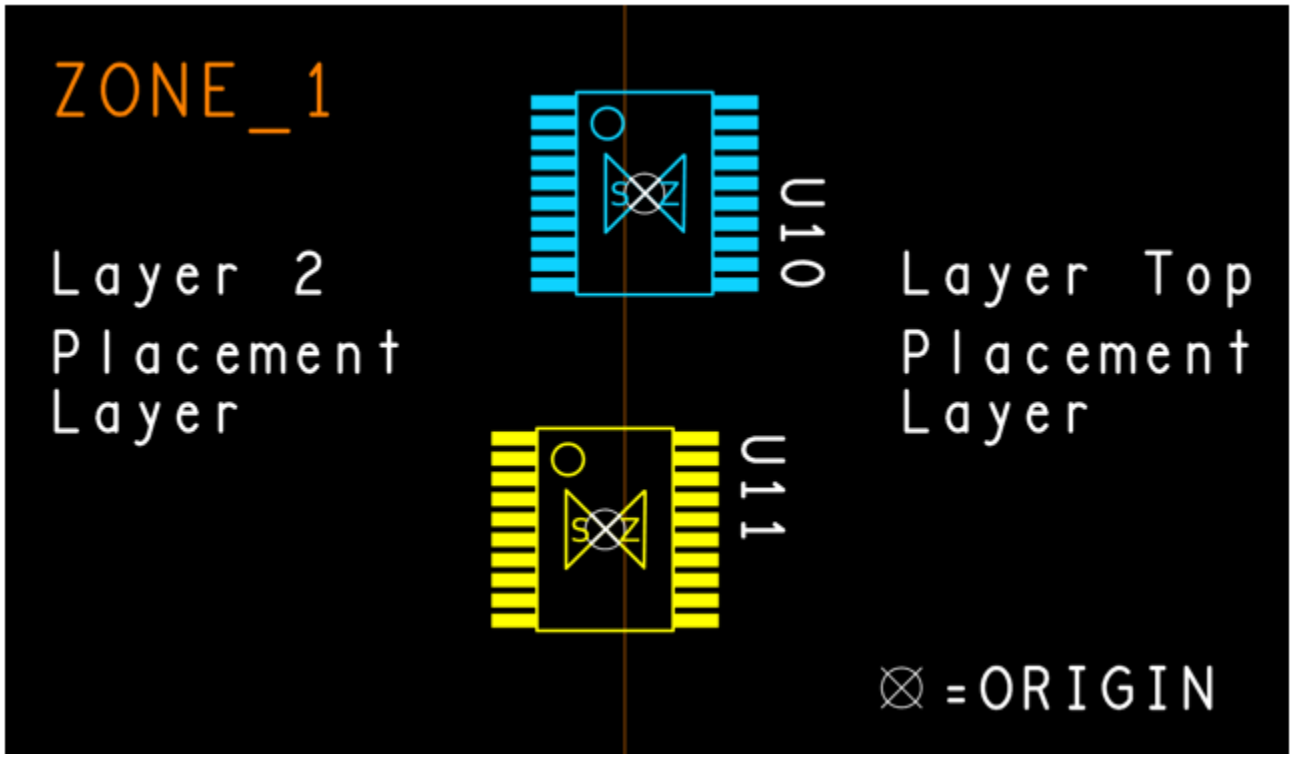
This release has the following Rigid-Flex enhancements:

Zone Adherence for Symbol Pins

There are two new Analysis Mode checks (*Analysis Modes – Design – Zone Placement Adherence*) to verify that all pin pads of a component are on the same placement layer.



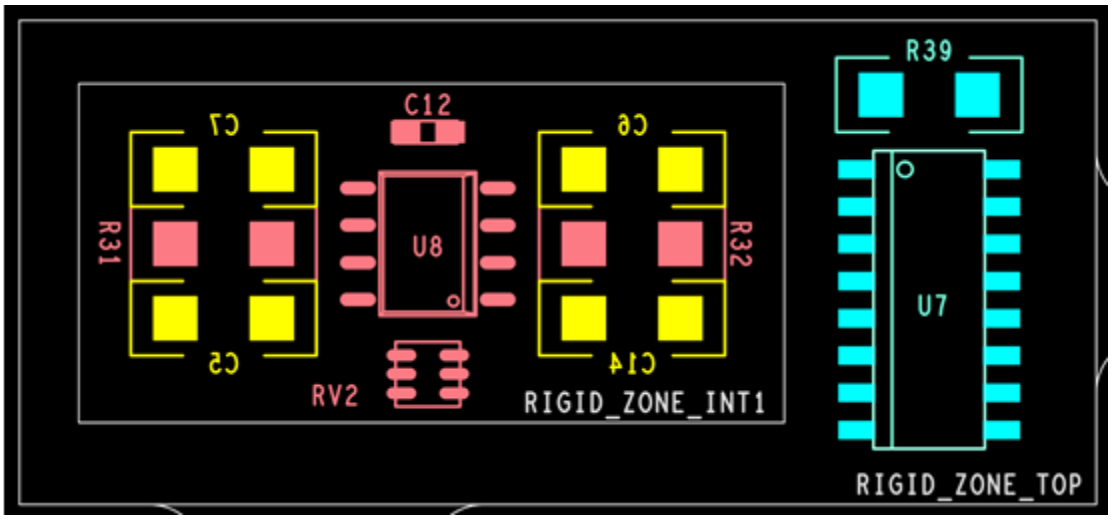
DRC is generated if part of a pad crosses over an area where placement layer does not exist. Components can span different stack-ups areas if placement layer exists in both stack-ups, meaning that placement layer exists in adjacent zones or zone adjacent to primary.



Nested Zones Support

It is sometimes necessary to have an area in a zone with special mask, plating, or stack-up requirements different than the rest of the zone. In these cases, a separate stack-up will be specified to drive the fabrication process to produce correct design result.

Introduced in release 22.1, HotFix 003 (QIR2), you can now have one zone surrounded by another zone, avoiding a shape creation process that is complex and error prone.



ZONE = RIGID_ZONE_TOP	ZONE = RIGID_ZONE_INT1
PASTEMASK_TOP	
SOLDERMASK_TOP	PASTEMASK_INT1
TOP (Surface)	SOLDERMASK_INT1
INT_1	INT_1 (Surface)
FLEX_1	FLEX_1
FLEX_2	FLEX_2
INT_4	INT_4
BOTTOM (Surface)	BOTTOM (Surface)
SOLDERMASK_BOTTOM	SOLDERMASK_BOTTOM
PASTEMASK_BOTTOM	PASTEMASK_BOTTOM

Zone Boundary Updates

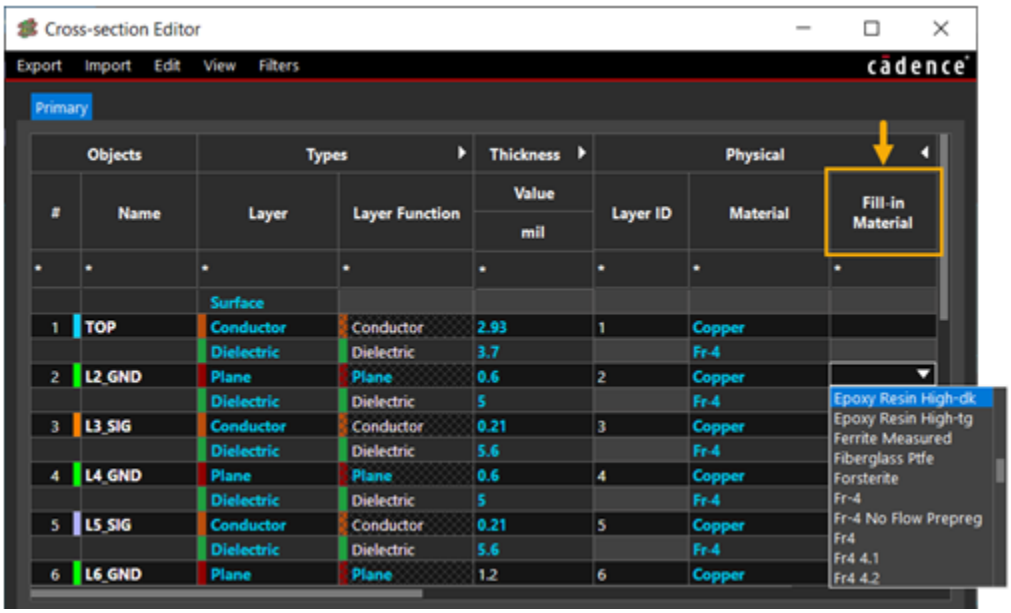
Now, you can use standard shape commands on zones, and edit zone shapes even outside the Shape Edit application mode. In previous releases, zone shape modifications were limited to the Shape Edit application mode by setting the *Enable zone boundary editing* option.

Fill-In Material (Dielectric Layers)

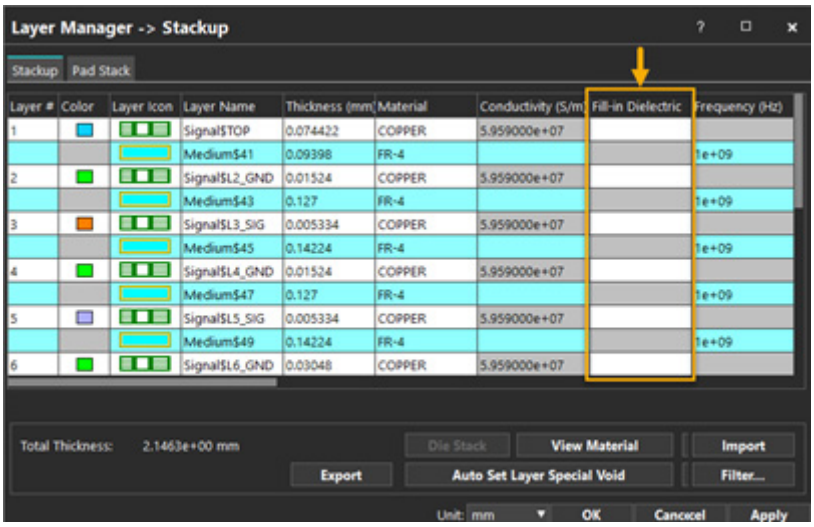
The new column *Fill-In Material* in Cross Section Editor is sourced from the common materials file (`.cmx`). The column is available on Conductor/Plane rows and is read-only for Dielectric or Named Dielectric rows.

The Fill-In Material value is supported with export or import of IPC-2581 and Cross Section files. Material defined in this column is read by Sigrity™ products for a more realistic simulation result.

The following image shows the *Fill In Material* column in Cross-section Editor:



The following image shows the equivalent *Fill in Dielectric* field in Layout Manager of the Sigrity product:

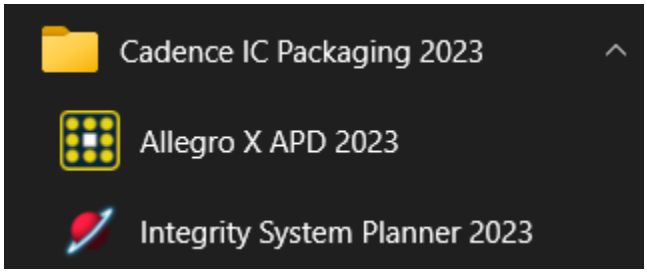


Note: Fill-In Material is deleted on downrev.

Branding Updates: Allegro X Advanced Package Designer

The constraint-driven, correct-by-design package substrate layout editor is now known as Allegro® X Advanced Package Designer.

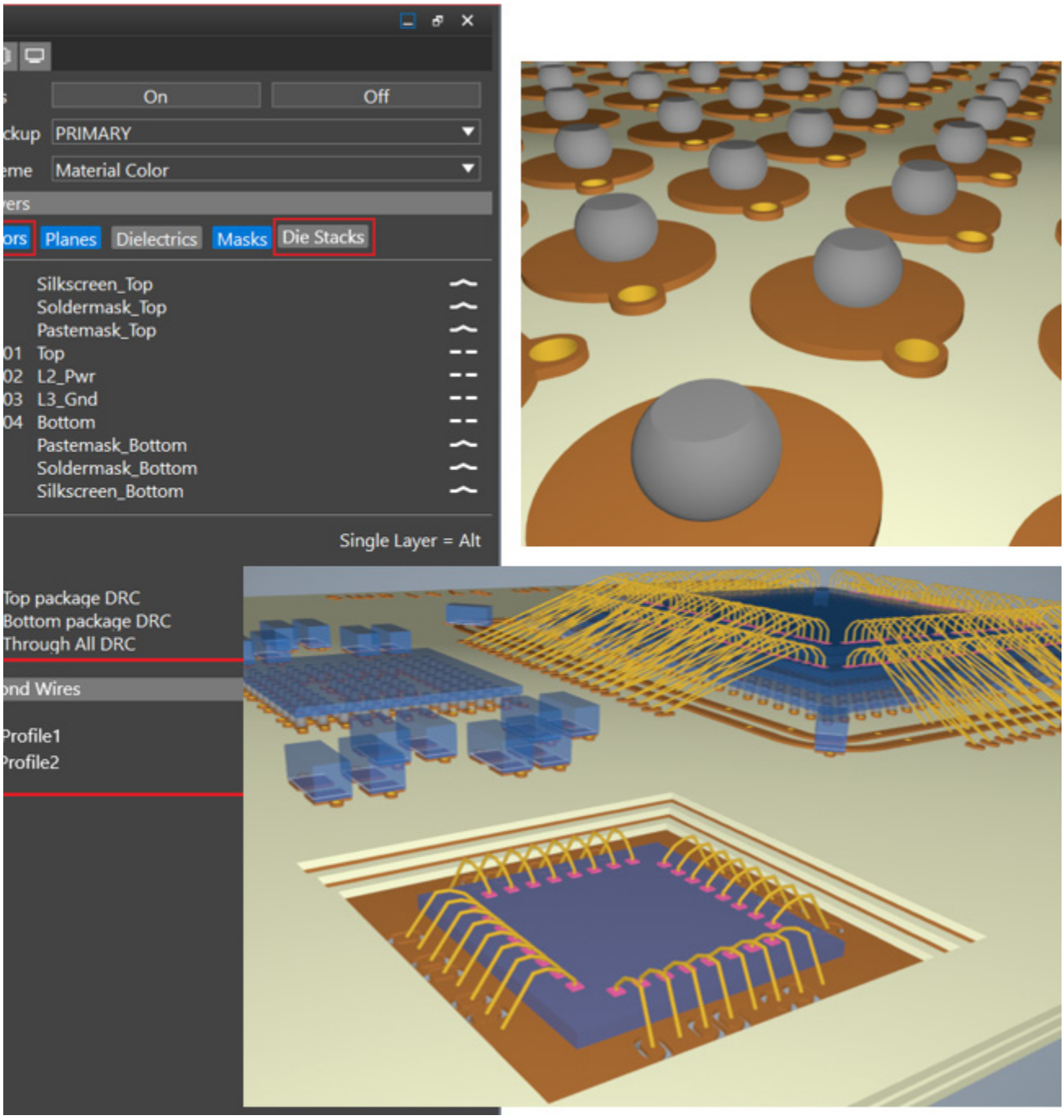
You can access the editor from *Cadence IC Packaging 2023* of the Windows *Start* menu.



Packaging Support in 3DX Canvas

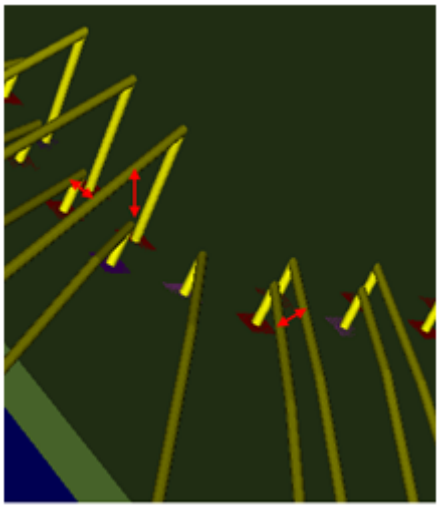
3DX Canvas addresses the scale and complexity in large modern package designs. 3DX Canvas provides highly efficient visualization representation and implementation and the new architecture enables high-performance 3D incremental updates by utilizing GPU for fast rendering.

In addition to real-time 3D incremental updates and providing 3D view in sync with all changes to database, now there is support for 3D visualization for packaging objects such as wire bonds, ball, die bump/pillar geometries, die stacks, etch back, plating bar.



3DX Wire DRCs

Constraint Manager now has 3D DRCs that are computed and checked in 3D providing real 3D checks.



You can view DRC Violations can be viewed in the 2D canvas or the new 3DX Canvas.

The following DRC checks are available:

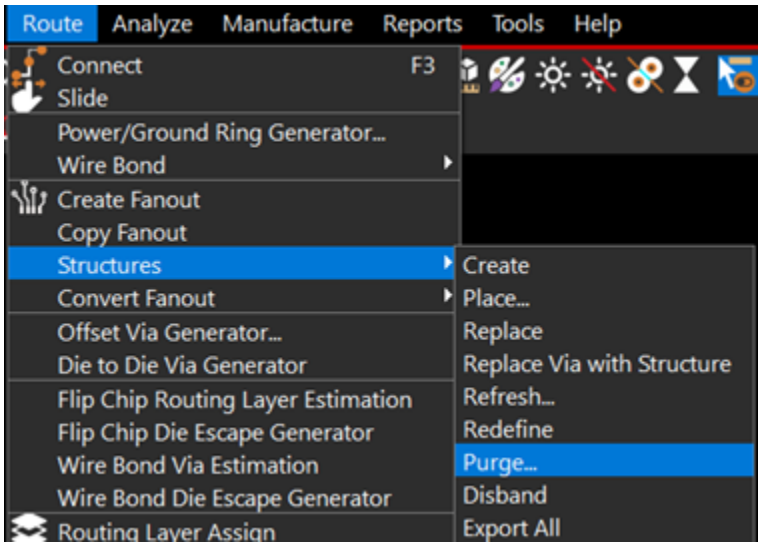
- Wire to Wire
- Wire to Finger
- Wire to Shape
- Wire to Cline
- Wire to Component

Structure Enhancements

Structures have been enhanced with the following changes:

- Purging of Structures

  You can now Purge structures to remove their definitions from the design.

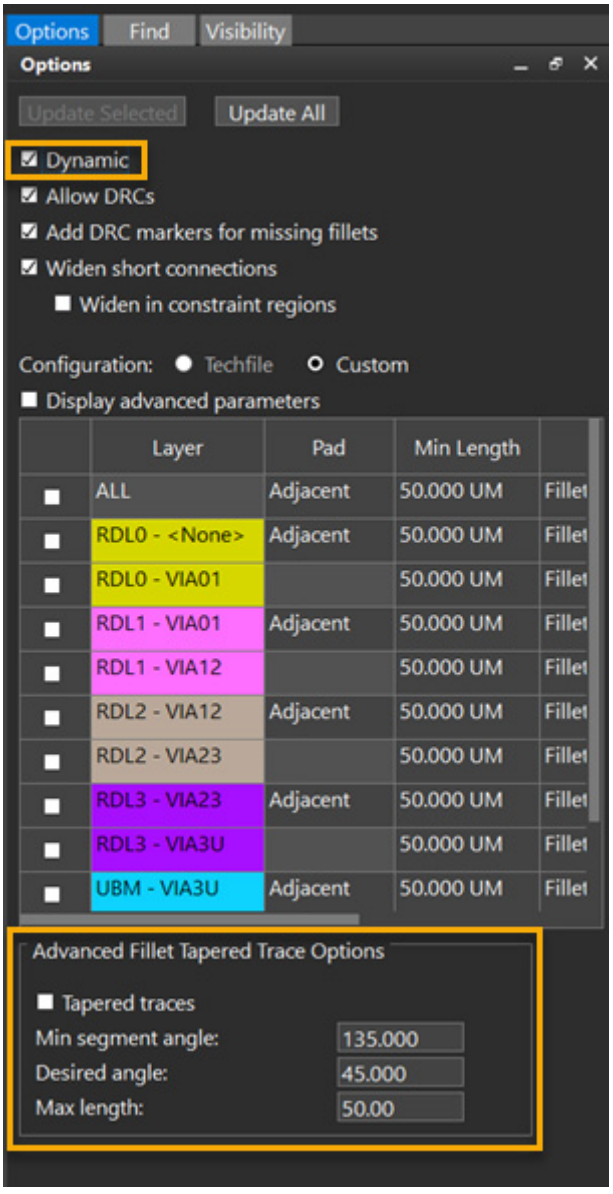


- Via Structures Loaded from Library: If you reference Via structures in subdrawing/clip files and the structures do not exist in the target design, the structures are now loaded from library, similar to other symbols.

Dynamic Advanced Fillets

Note: This enhancement is available in Allegro X Advanced Package Designer with the *Silicon Layout* option.

Now, fillets are dynamically updated while routing to meet silicon fillet rules. You can also dynamically add tapered trace fillets as you route using Advanced Fillets.



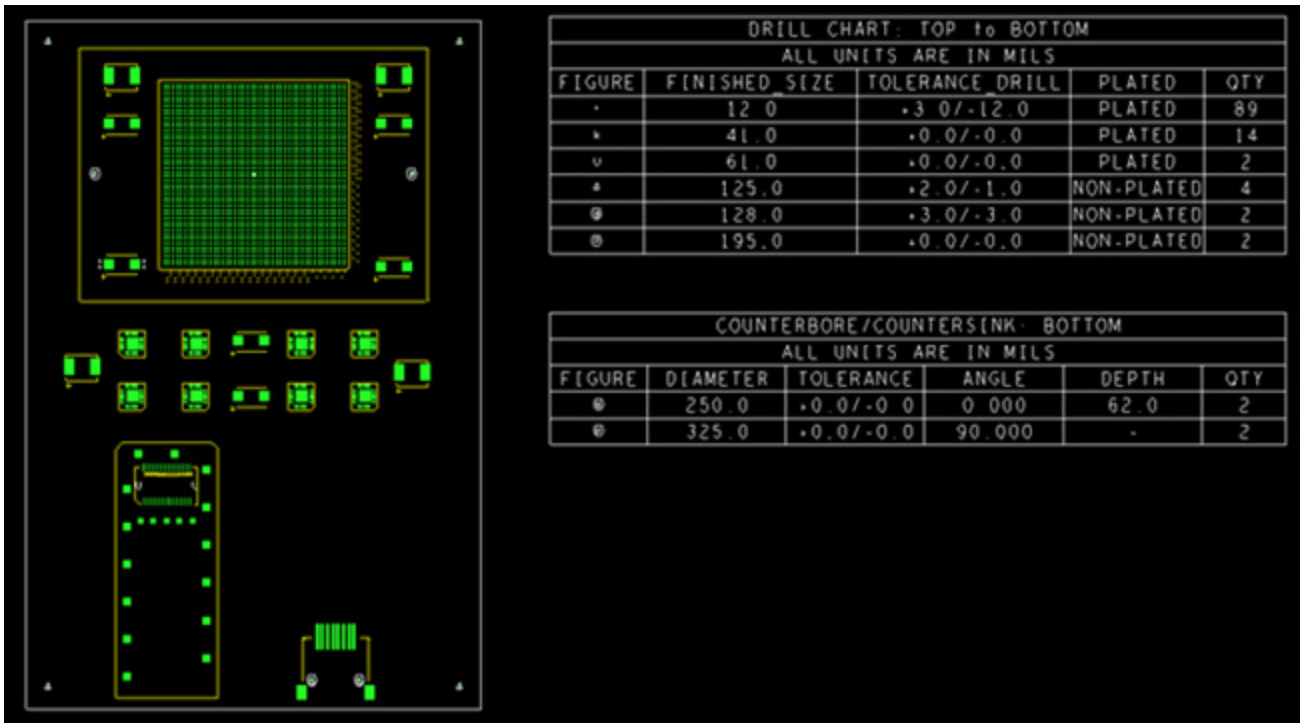
Padstack Editor Enhancements

Following are the enhancements available in Padstack Editor in this release:

Counterbore and Countersink Secondary Side Definition and Reporting

Now, you can define counterbore or countersink from either the primary or the secondary side, and are not bound to the side the component is placed on.

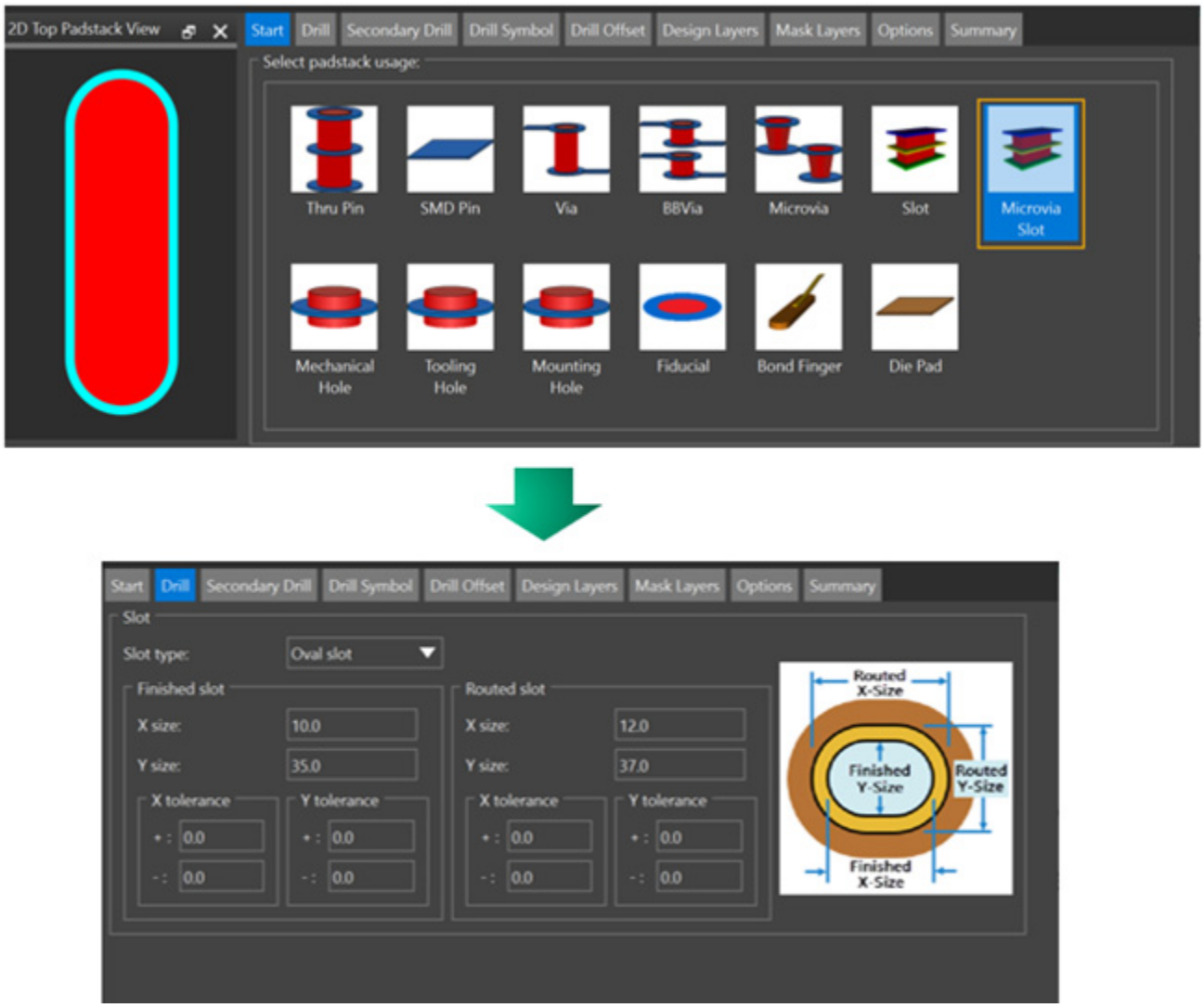
You also do not need to inform the fabricator about secondary drill requirements separately because Drill Legend and NCDrill Export now report when drilling is required from secondary side.



Note: If you need to downrev a release 23.1 design, you must manually remove any counterbore or countersink that exist in the secondary side.

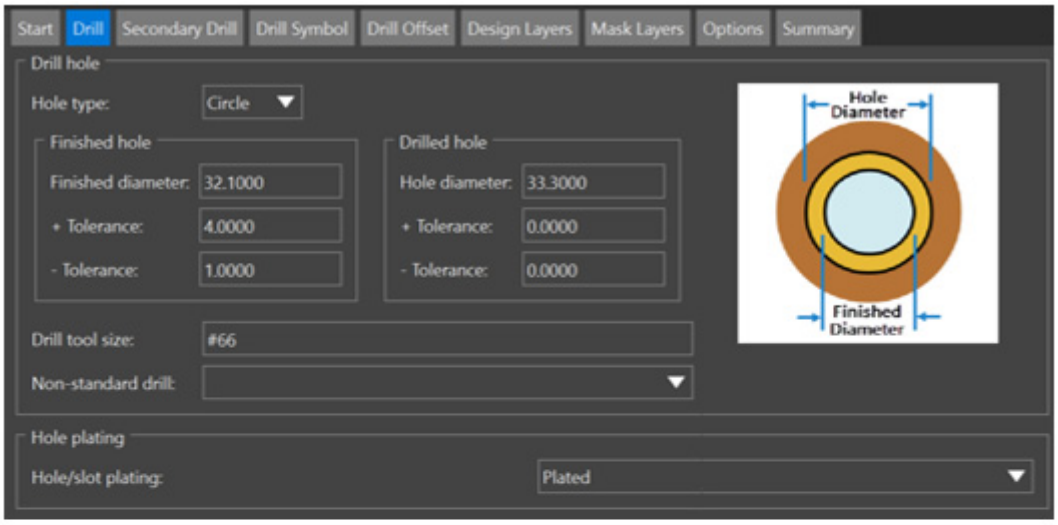
Oval and Rectangular Slots for Microvia Padstacks

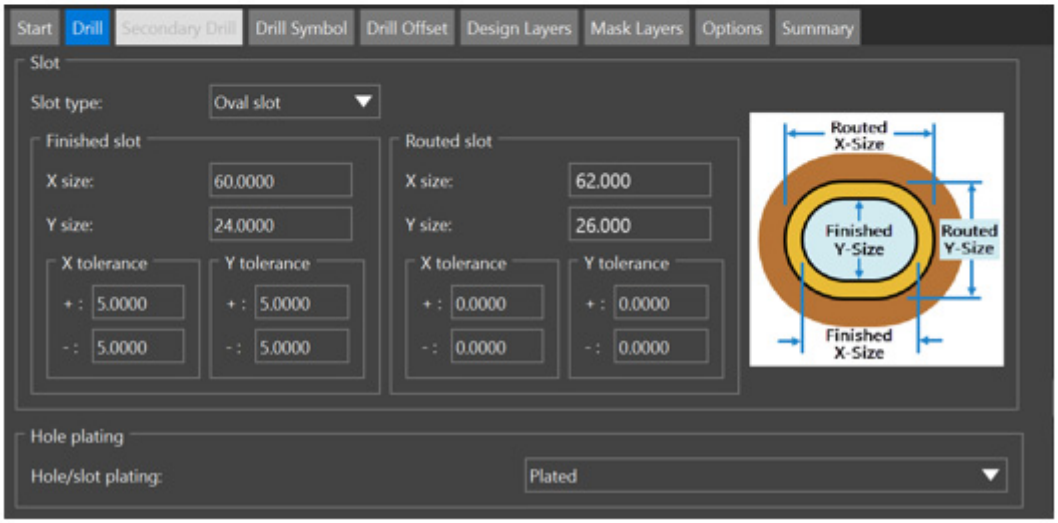
You can now use oval and rectangular slots in microvia padstacks These slots are in addition to the existing circle and square plated holes. The new slot types follow the standard Microvia constraints.



Drilled Holes/Slots Before Plating

You can now specify accurate size for drill holes or routed slots before the holes are plated to ensure the holes or slots are not damaged during assembly, for example, for Press Fit connectors.



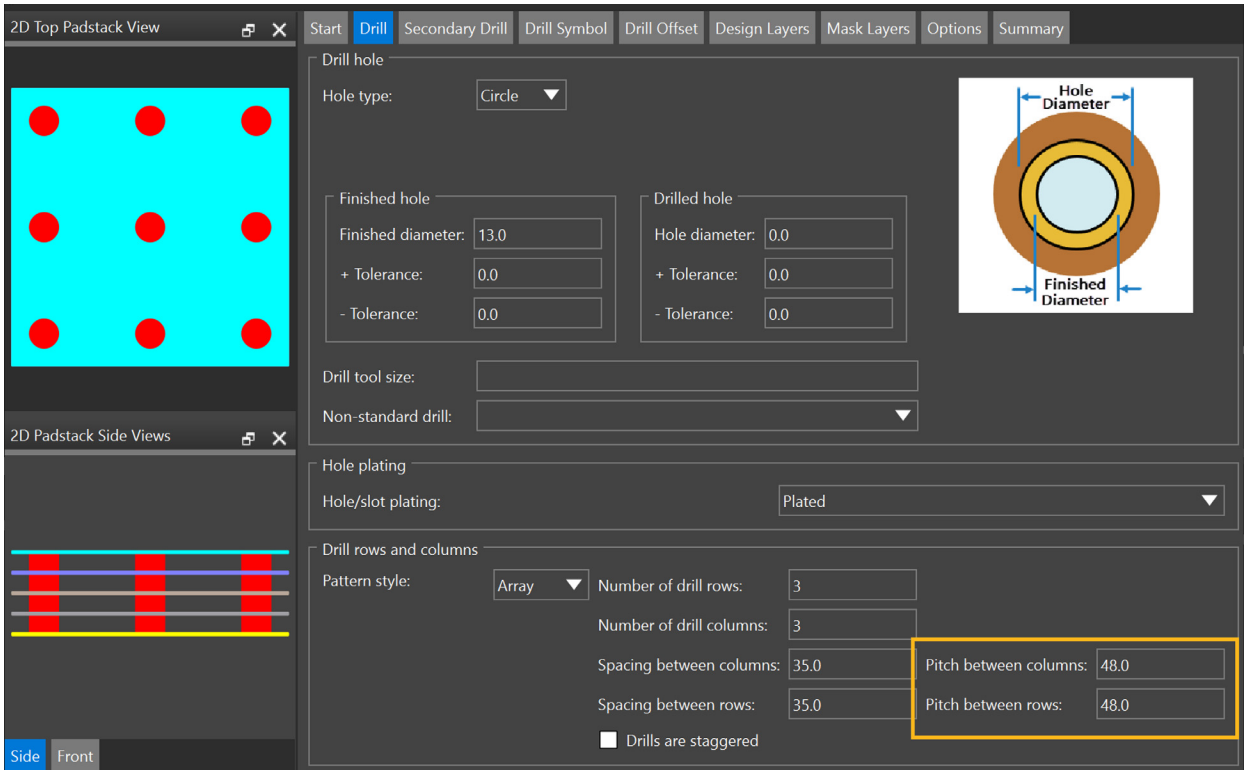


You can specify circle or square holes for Drilled Holes and rectangle or oval slots for Slot Holes. You can also specify a tolerances for the hole or slot size.

Note: During downrev, any drilled holes will be removed from the padstacks of the design.

Calculated Spacing for Multi-Drill

Now, you can specify pitch values for the rows and columns for a multi-drill and the spacing is automatically calculated.

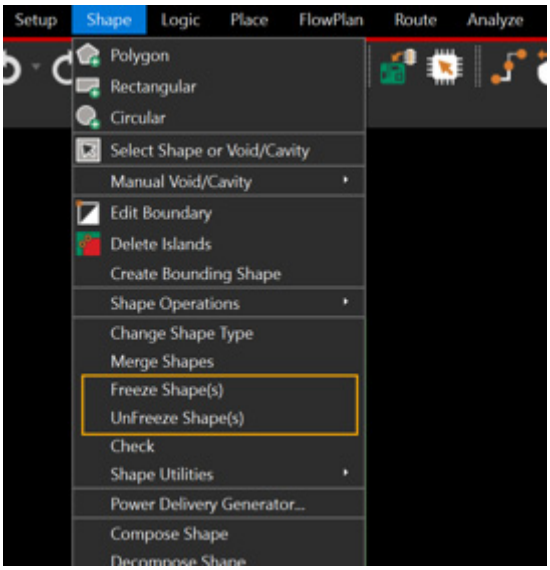


Dynamic Shape Update: Frozen Shapes

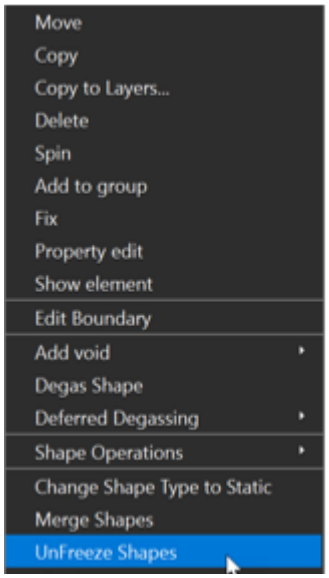
Dynamic shapes are automatically updated when interacting with other objects, but you can now freeze the shapes without changing them to static; for example, to maintain design intent by protecting critical circuitry drawn using shapes.

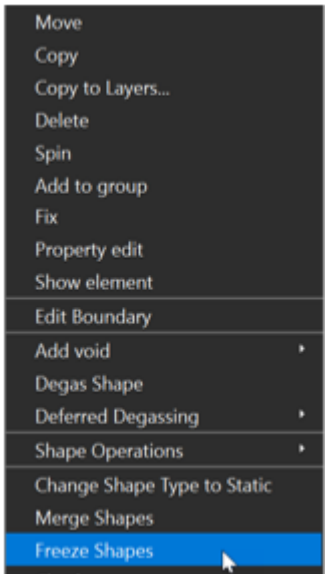
Once a dynamic shape is frozen, new objects entering the dynamic shape area will not void and generate a DRC Error similar to a static shape. You can manually modify shape boundaries on frozen dynamic shapes to maintain current voiding while avoiding new voids.

Choose the *Freeze Shape(s)* or *Unfreeze Shape(s)* command options from the *Shape* menu to freeze or unfreeze a dynamic shape.

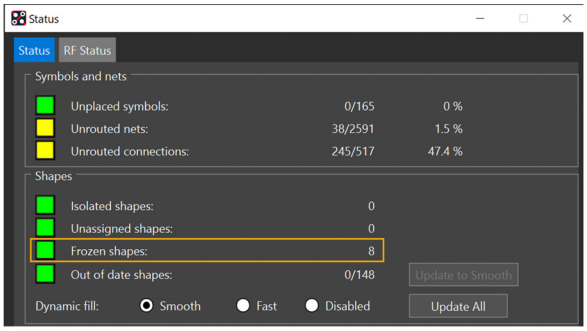


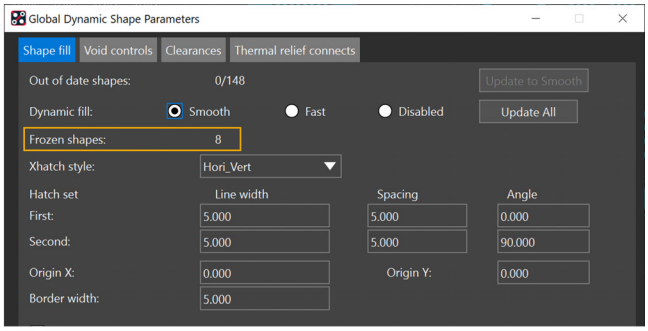
You can also select a shape and then choose command from the context menu.

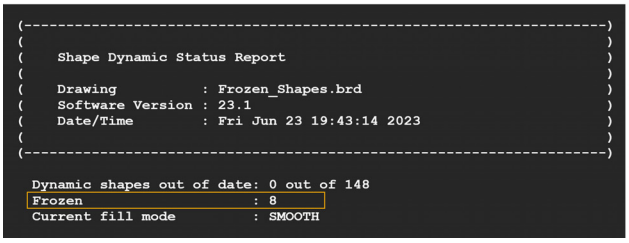


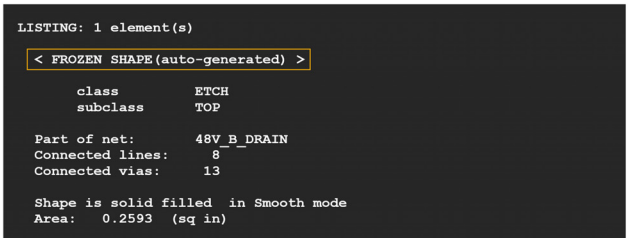


All reports, such as Design Status, Shape Parameters, Shape Reports, Show Element, or Find By Query, that show Dynamic shape status also show frozen shapes.





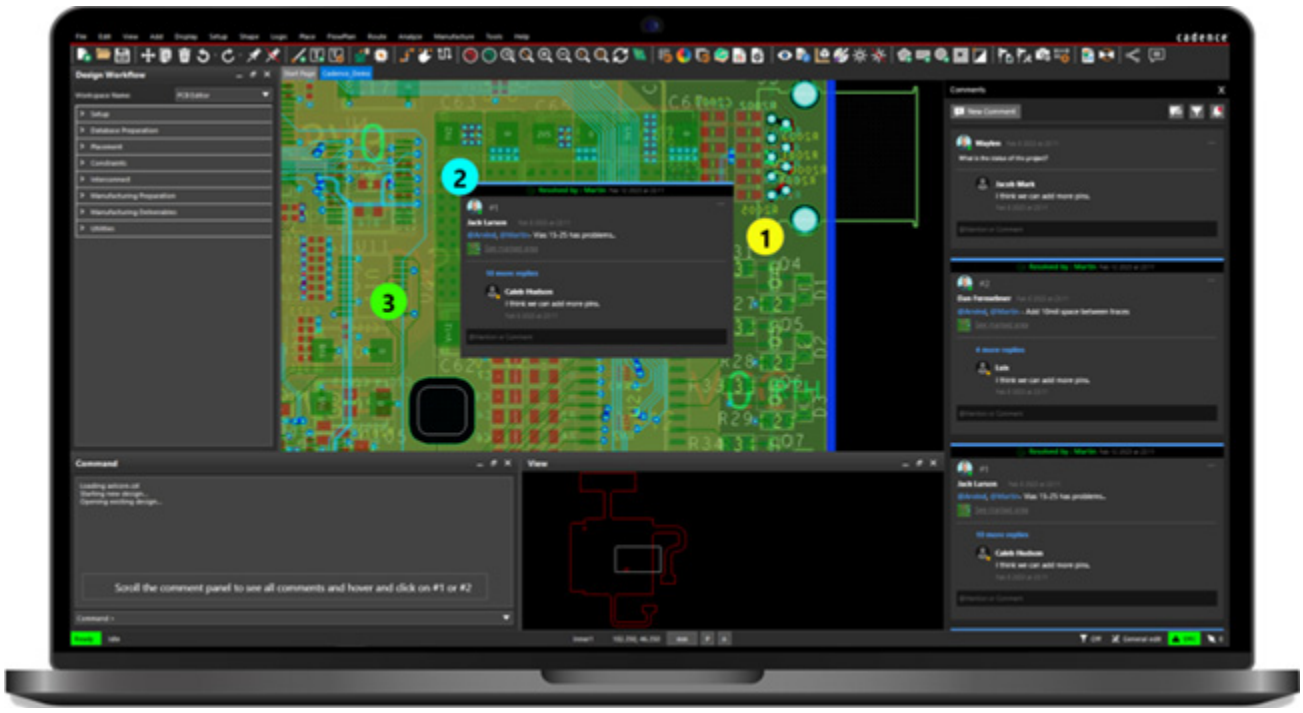




Design Review and Markup

This release has the new Design Review and Markup feature enabling the review and tracking of designs through markups. The markups are stored in the database with tracking comments. You can recall a markup with canvas auto-centering and layer display.

Note: This feature is available in Allegro®, Allegro® X, OrCAD® X licenses and Allegro® X System Capture licenses that can edit layout databases.



Usability Enhancements

This release has the following usability enhancements:

Allegro X - 3D Canvas Update

It is now easier to map 3D Models and output 3D representation.

3D Model Mapper in Symbol Editor

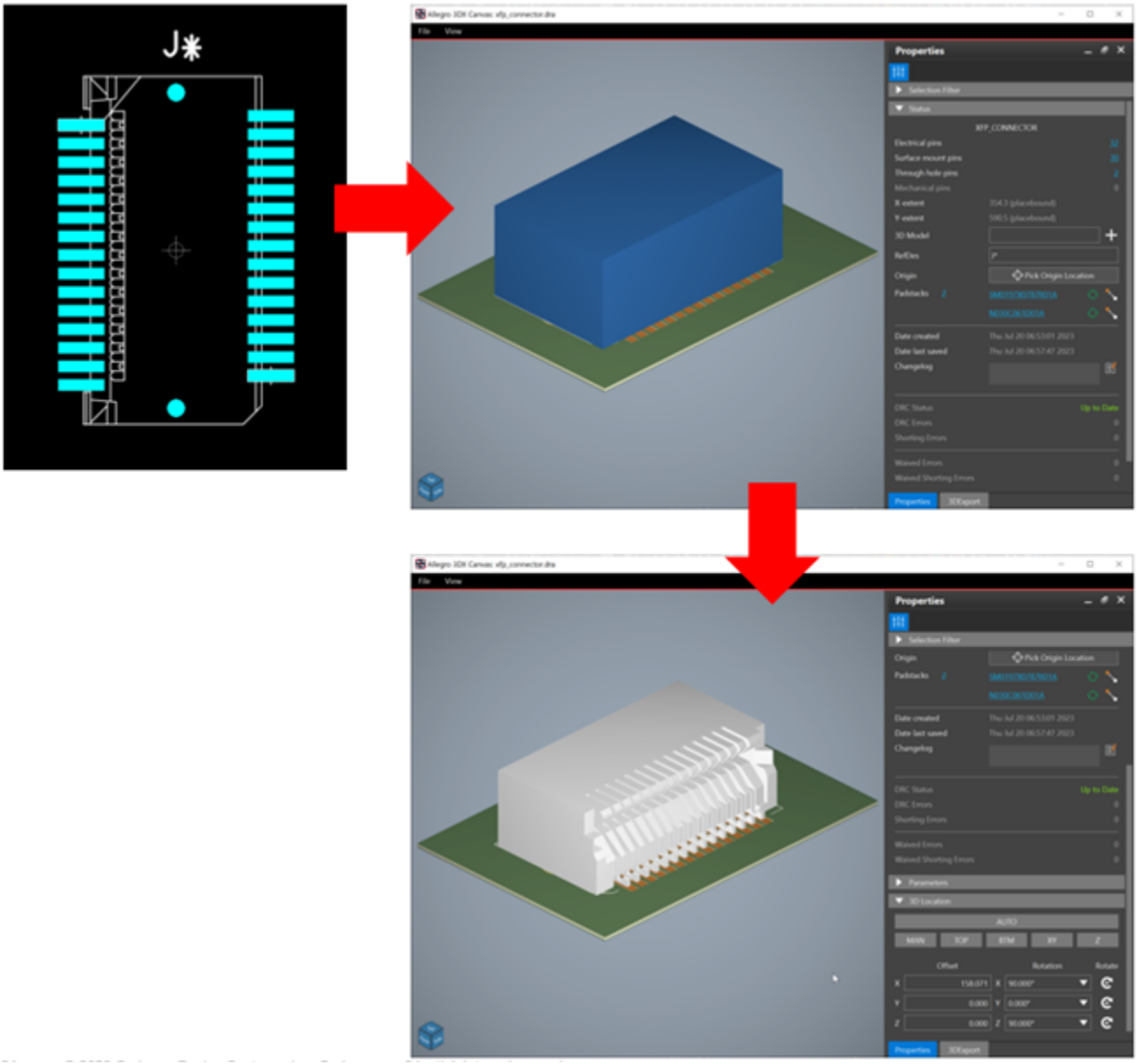
You can now map 3D Models to footprints directly in the library without the need of STEP models on the disk.

To assign a model to a footprint and view in the layout, do the following:

1. In the *Properties* tab, select the STEP model

2. Under *3D Location*, click *AUTO* and then fine tune the X-Y-Z placement.

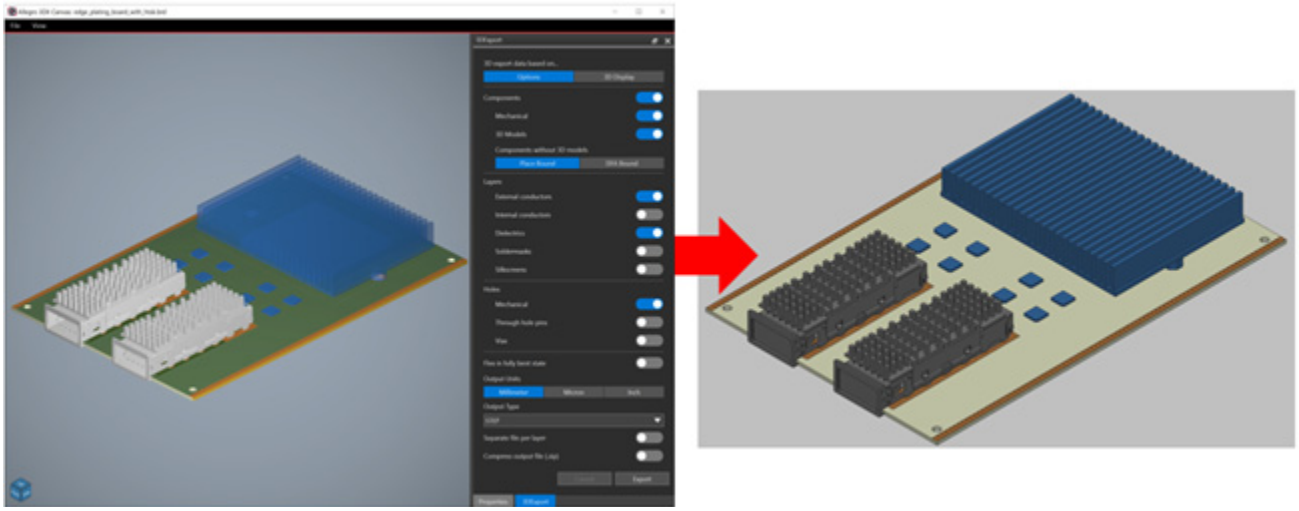
   Footprint Model assignment is visible in the layout.



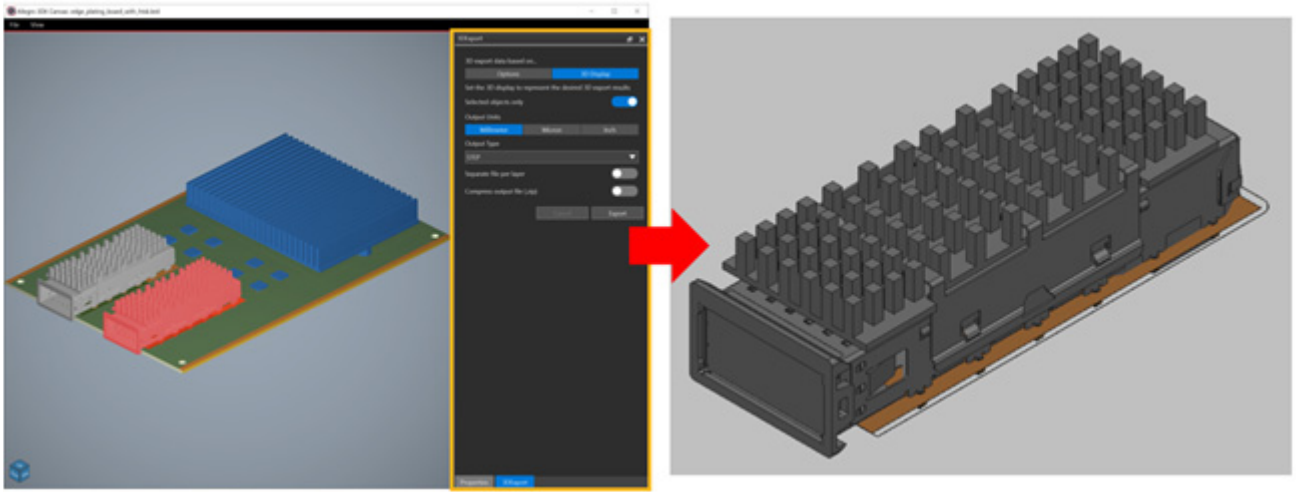
3D Model Export Support

You can now output complete 3D representation of the entire design or 3D representation of based on visibility settings.

To output a complete 3D representation, select the required output from the 3D Export tab and then click *Export*. You can select from any one of STEP, IGES, ACIS, or PDF.

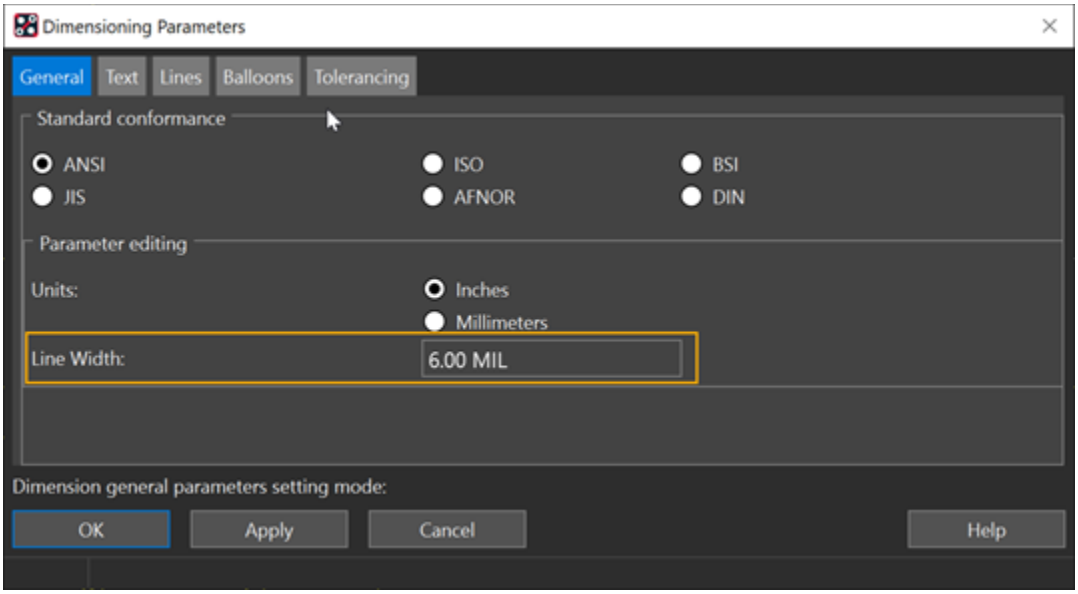


To output 3D representation based on visibility settings, set Selected objects only.



Dimension Environment Update

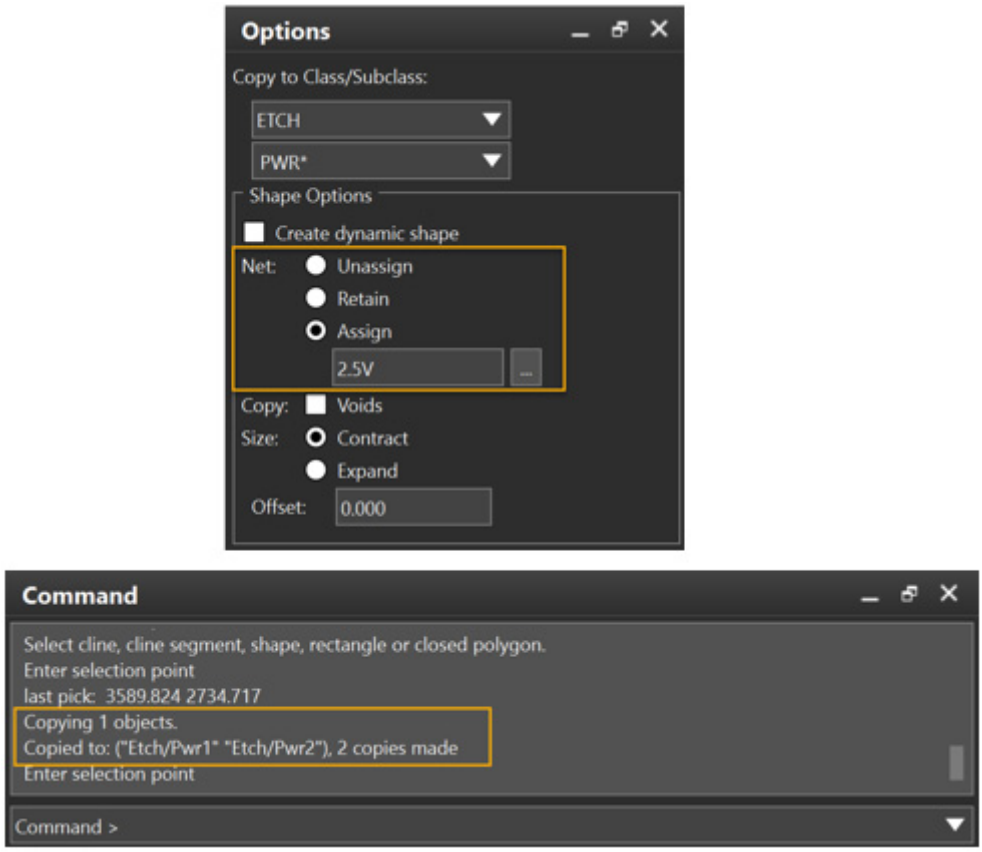
Use the new *Line Width* parameter to apply a line width to dimension lines.



Without the line width, the dimensions were drawn with thin (0-width) lines as shown in the following figure:

Z-Copy Enhancements

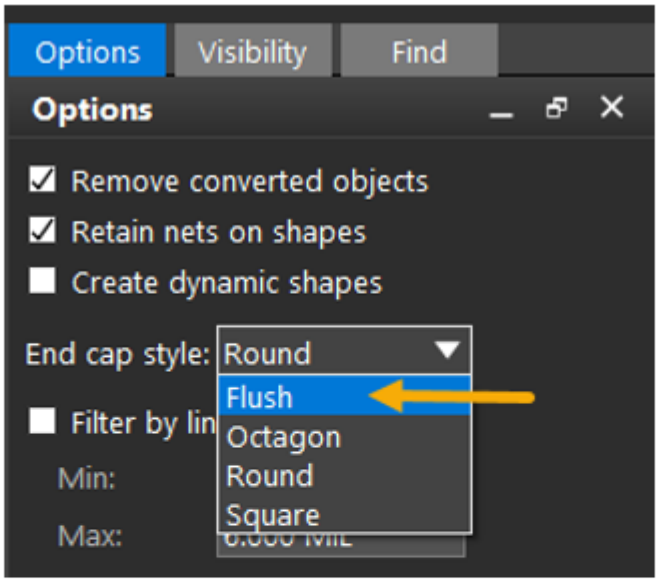
Copying etch shapes to other layers has become easier with Z-Copy using the new *Net* options that save extra steps on canvas to adjust shape Net Name on copies.

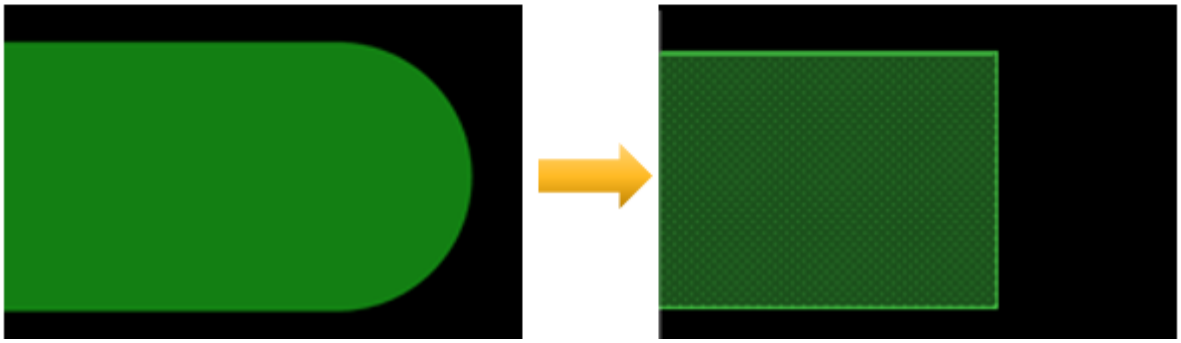


Note: You can use a wildcard in the target layer name to copy a shape to multiple layers.

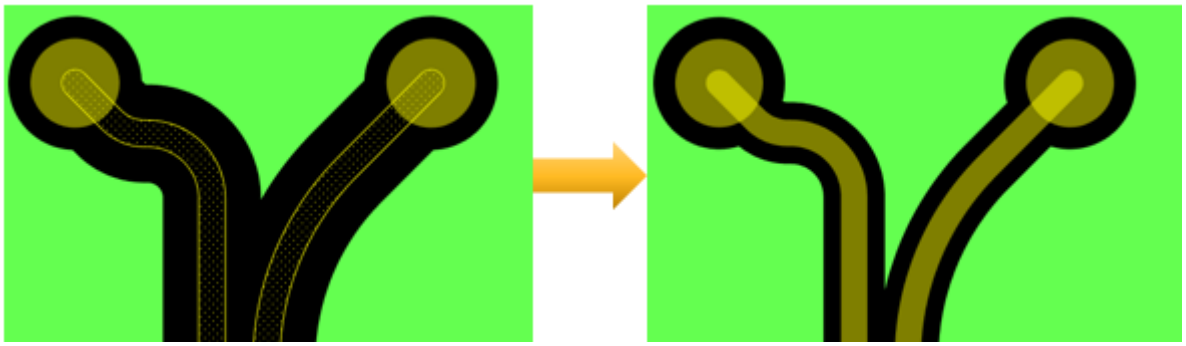
Enhancements to the Convert Cline or Line to Shape Utility

Tools – Convert contains several conversion utilities to convert between object types. The Cline / Line to Shape utility has been enhanced to include an additional *End Cap Style* called *Flush*.





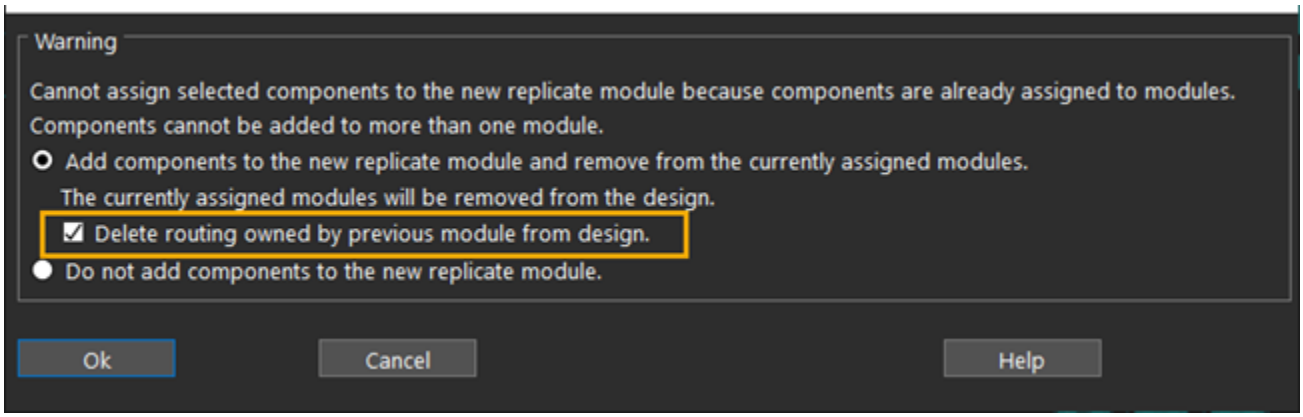
In addition, converting Shapes with arc segments now converts to Clines Arcs.



Place Replicate Apply Enhancements

Components can only be a member of one Place Replicate module at any given time. It is possible to re-apply a component or group of components to a new replicate module, but it leaves behind any connected copper features from the previously applied module. You must manually remove routing that is left behind.

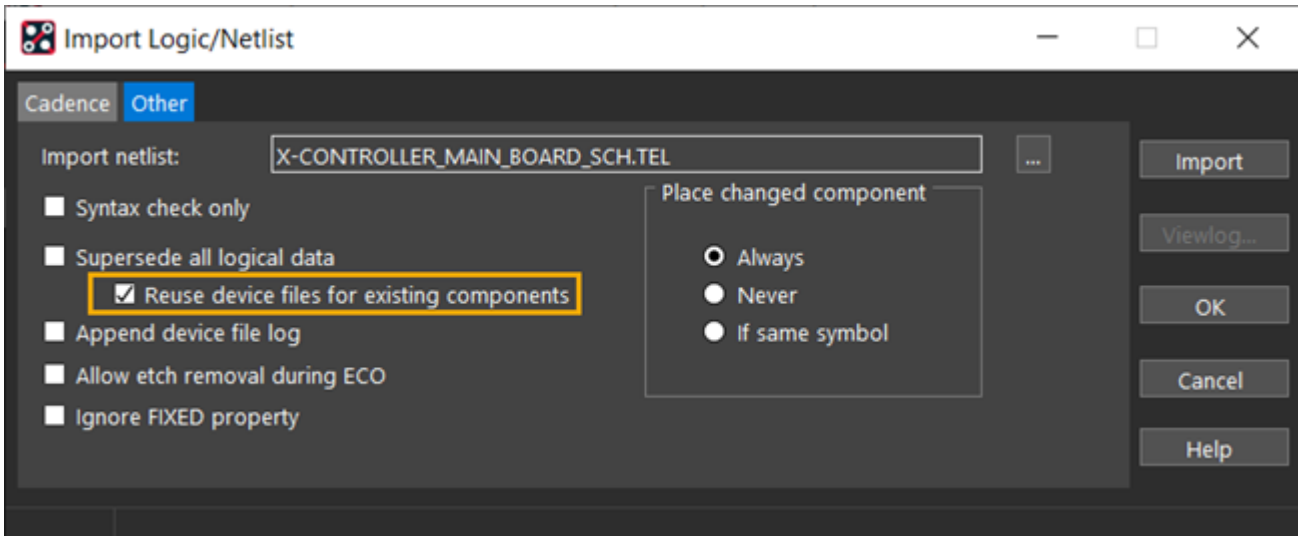
You can use the new option *Delete routing owned by previous module from design* in the Warning dialog box to remove the routing from previously applied modules.



Third-party Netlist Import

You might be receiving a new netlist several times during the design process. Devices files are required to import a netlist successfully.

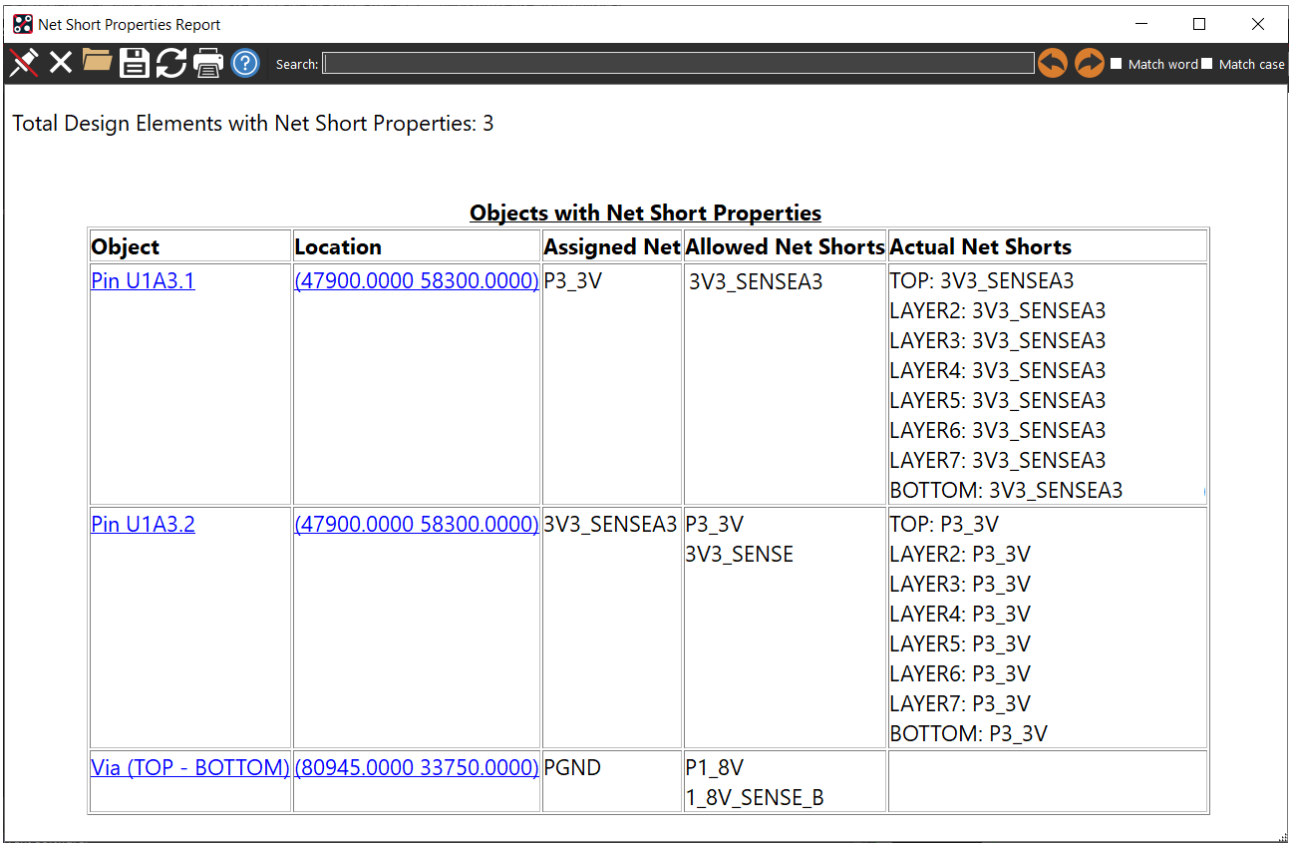
A new option *Reuse device files for existing components* has been added to reuse Devices Files that are currently in a design, eliminating the need of export them out of design every time a netlist import is required.



Net Short Report

You can create a direct short in a design by adding a NET_SHORT property to the objects and then shorting Net Name. You must then verify manually that all the required shorts have been made.

You can now use the new Net Short Properties report to verify shorts. This report lists all objects in the design with NET_SHORT properties along with the layers that the short occurs.

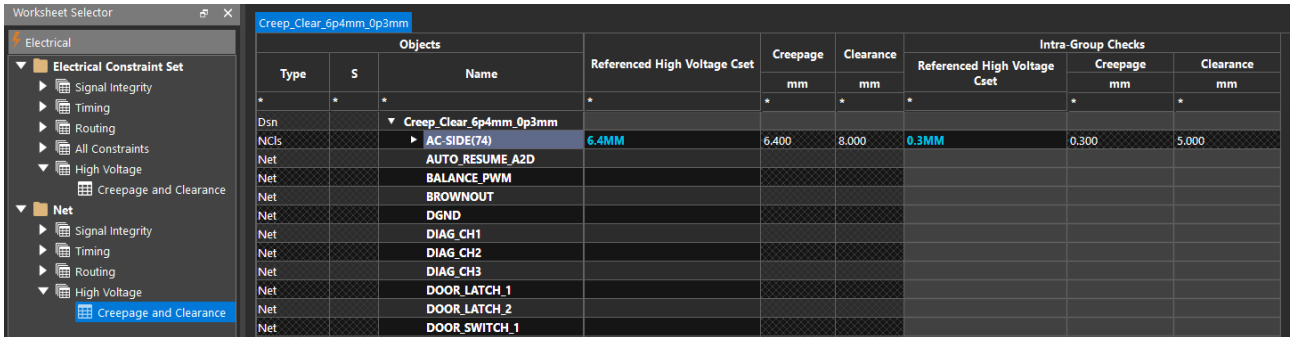


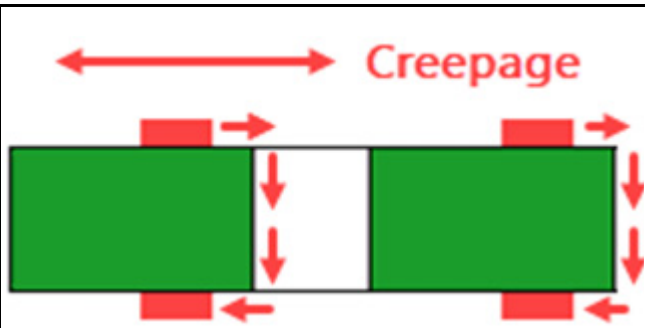
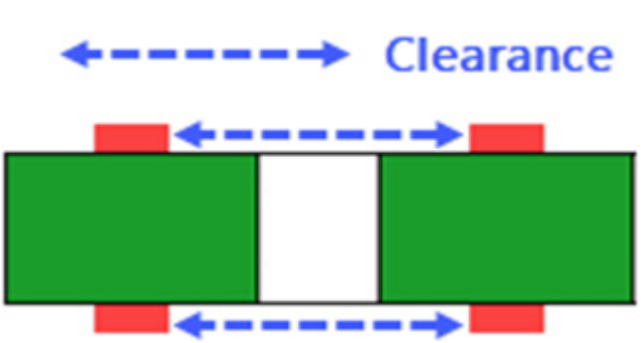
Object	Location	Assigned Net	Allowed Net Shorts	Actual Net Shorts
Pin U1A3.1	(47900.0000 58300.0000)	P3_3V	3V3_SENSEA3	TOP: 3V3_SENSEA3 LAYER2: 3V3_SENSEA3 LAYER3: 3V3_SENSEA3 LAYER4: 3V3_SENSEA3 LAYER5: 3V3_SENSEA3 LAYER6: 3V3_SENSEA3 LAYER7: 3V3_SENSEA3 BOTTOM: 3V3_SENSEA3
Pin U1A3.2	(47900.0000 58300.0000)	3V3_SENSEA3	P3_3V 3V3_SENSE	TOP: P3_3V LAYER2: P3_3V LAYER3: P3_3V LAYER4: P3_3V LAYER5: P3_3V LAYER6: P3_3V LAYER7: P3_3V BOTTOM: P3_3V
Via (TOP - BOTTOM)	(80945.0000 33750.0000)	PGND	P1_8V 1_8V_SENSE_B	

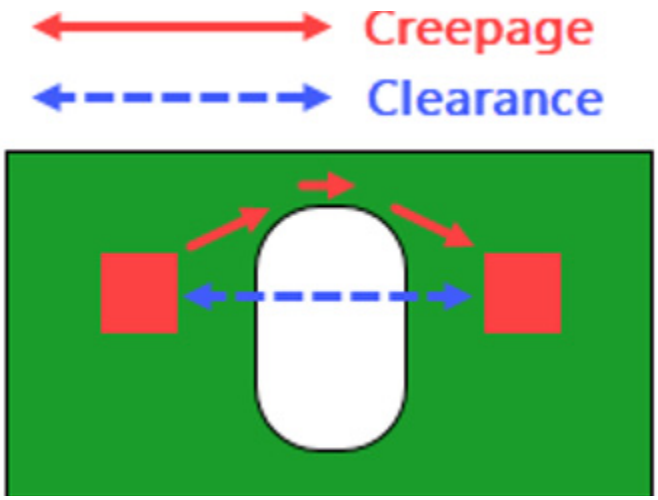
Creepage and Clearance Checking

Note: This feature is available only for the Allegro X Venture and Enterprise licenses.

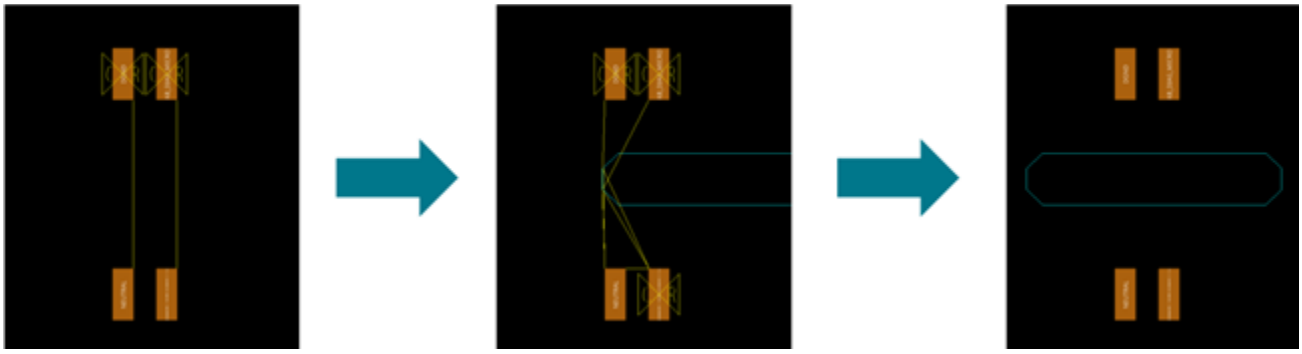
You can use the new High Voltage Constraint checks to verify creepage and clearance rules.



Creepage: Distance measurement along surface of material between high-voltage objects.	
Clearance: Spacing measurement through the air between high-voltage objects.	

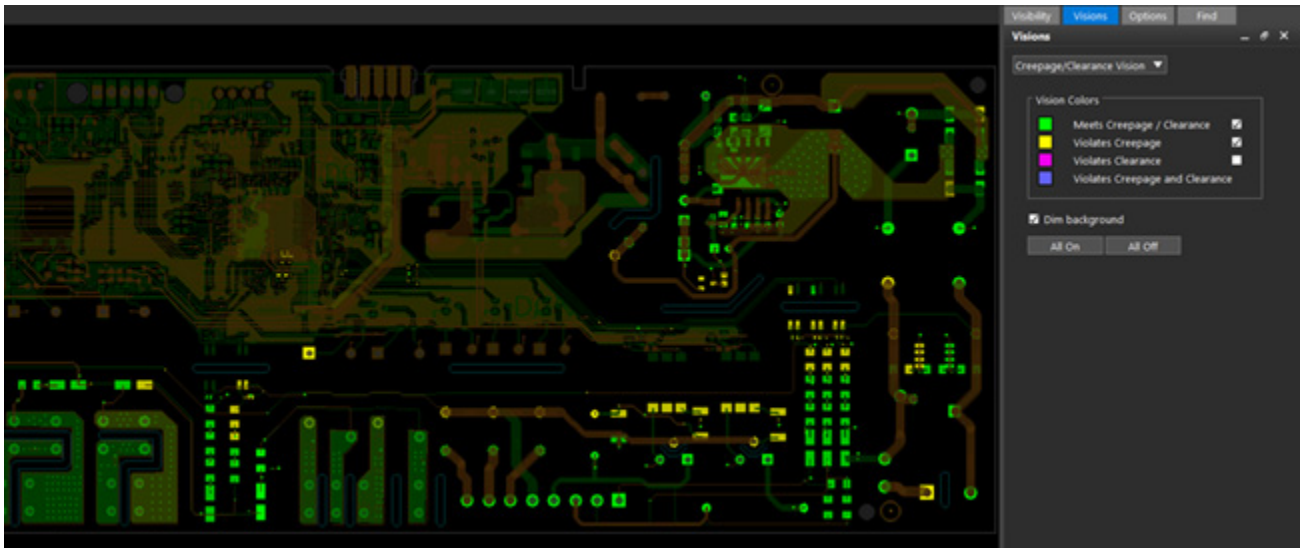


The DRC system recognizes non-plated slots added between two high-voltage objects to increase creepage, and recalculates the creepage around the slot while clearance is measured across the slot opening through the air. Creepage measurement jumps across slot openings when distance is less than Pollution Degree defined in Analysis Modes (*Setup – Constraints – Modes - Design Settings*).



Note: Design Outline notches and Multi-Layer stack-up might not calculate Creepage distances correctly. This will be addressed in a future HotFix.

You can use the Creepage/Clearance Vision to review the DRC errors. The Vision provides graphical feedback with color coding directly on canvas.



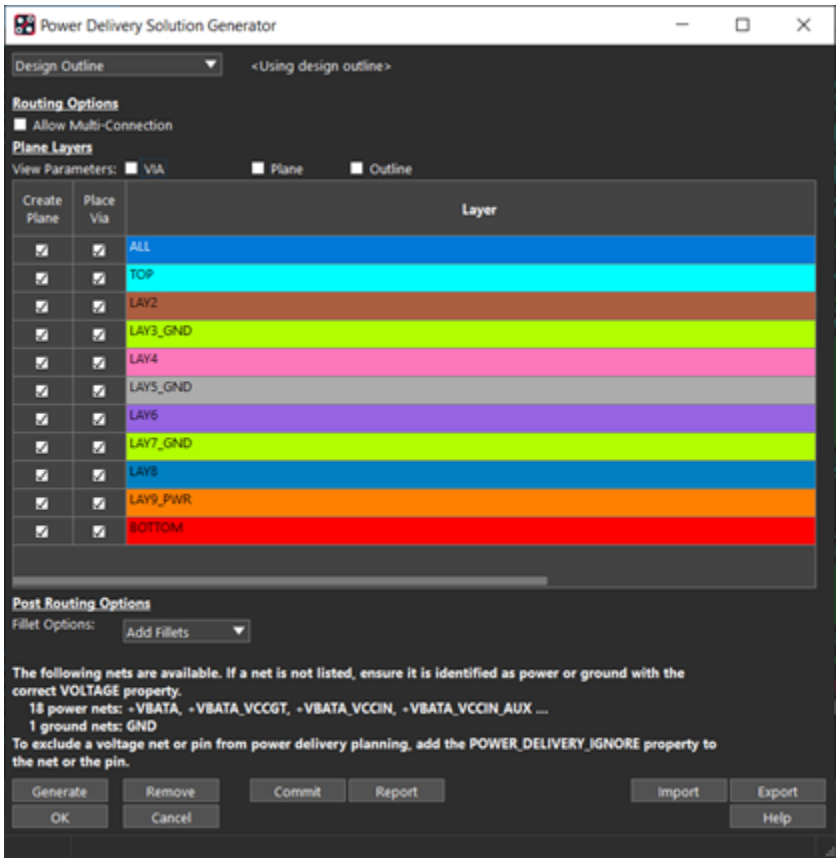
Power Delivery Generator Enhancements

Note: This feature is available in *Allegro X Advanced Package Designer* with *Silicon Layout*, *Allegro Enterprise PCB Designer*, and *Allegro X Venture Layout*.

You can use Power Plane Generator to quickly generate planes for a section of the design or the entire design based on pin placement for voltage nets. You can also review power plane escape and adjust placement or constraints to improve power connections.

Now, you can select different parameters for a basic or an advanced mode.

If you do not select any of the Via, Plane, or Outline parameters, you can generate planes in the basic mode with minimal setup for fast results with little to no learning curve.



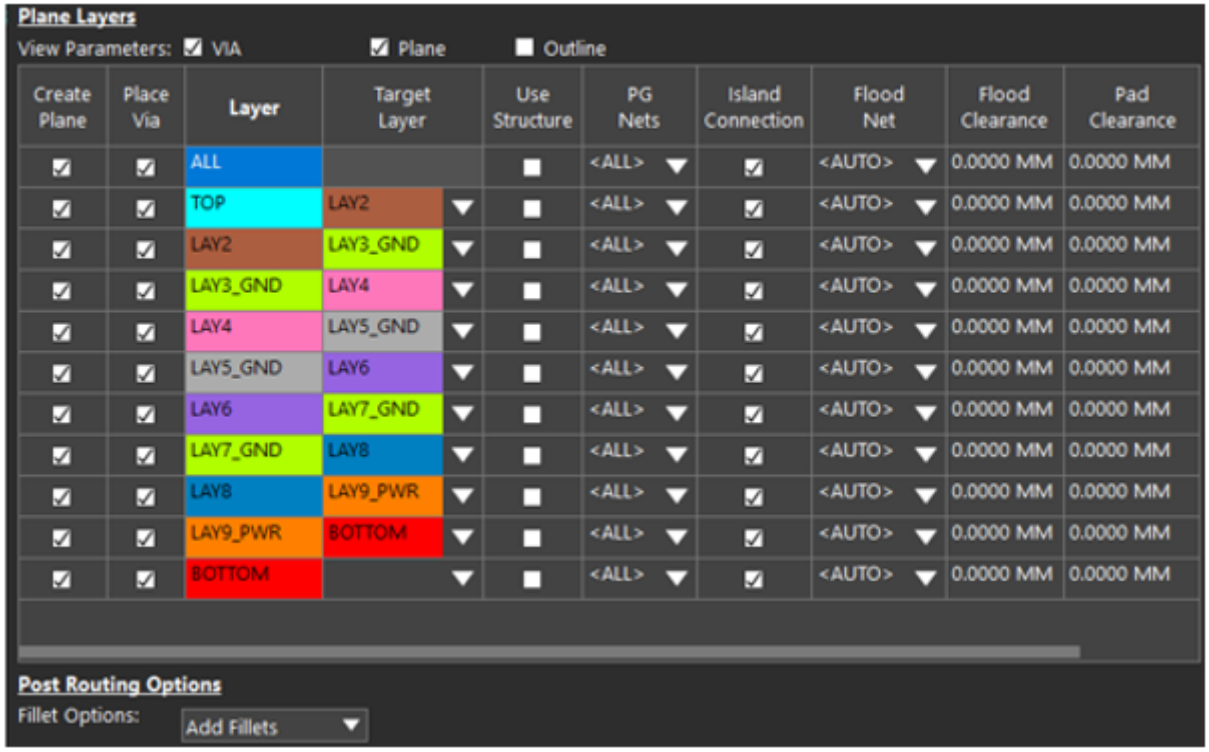
You can select to view parameters for Via, Plane, and Outline to access additional columns for a more detailed settings to control plane generation:

- Select *Via* to be able to stitch Via and Structure controls from current layer to a target layer.

- Select *Plane* to indicate specific details for Plane construction.
- Select Outline to be able to specify the shape outline controls.

Depending on the selection you see the following columns:

Column	Description	Available for Parameters
Use Structure	Select to use via structures for Power/Ground connections.	Via
PG Nets	Specify All, Ground, or Power nets (Nets with VOLTAGE property) on a per layer basis or define specific nets and priority per layer.	Via, Plane
Island Connection	Set to Allow trace connections to isolated vias.	Plane
Flood Net	Specify Flood Net (Voltage Nets) to backfill layer after plane generation.	Plane
Flood Clearance	Specify Flood Net Shapes inset for specific area outline.	Plane
Pad Clearance	Specify pad expansion to determine plane shape edge.	Plane
Plane Corners	Specify shape outline corner to be used (45° or 90°).	Outline
Plane Grid Snap	Set to snap each shape outline vertex to the etch grid.	Outline



Performance Improvements

Performance has improved substantially in features related to modules and in the 3DX Canvas application.

The module flow has up to 60X improvements in the following aspects:

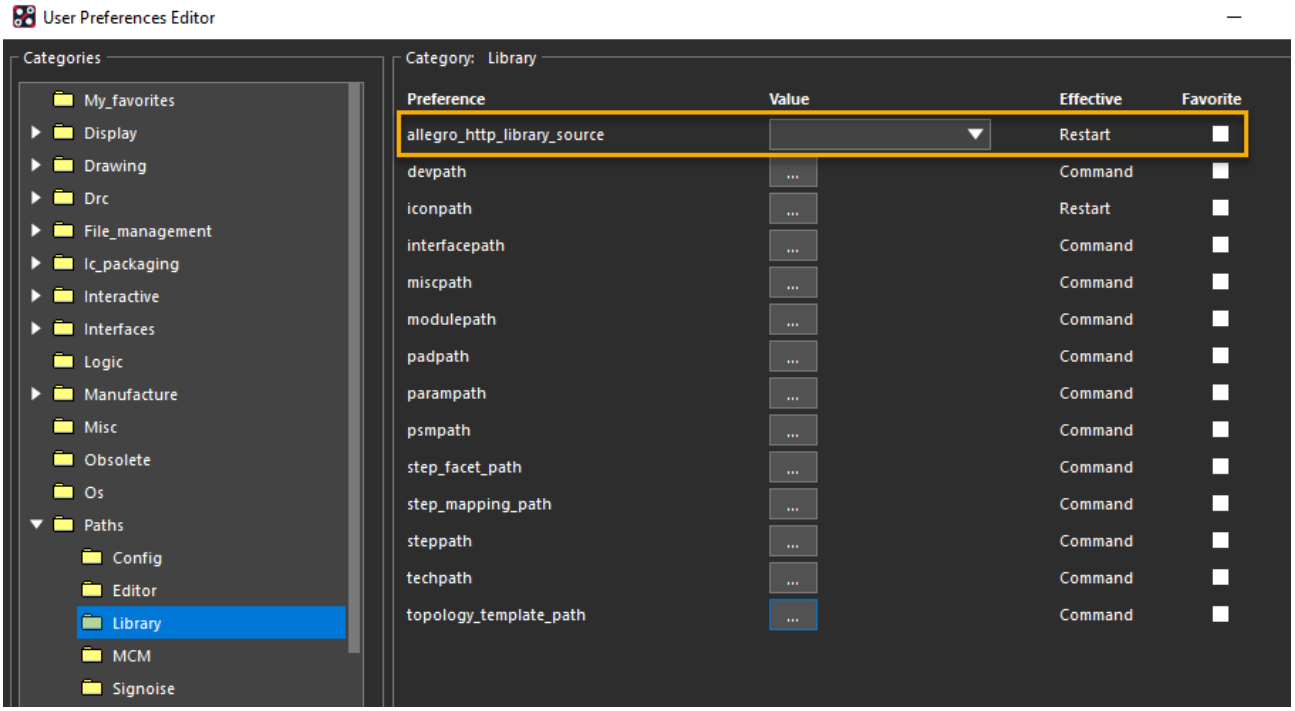
- Creation of modules
- Creation of Place Replicate modules
- Placement of modules
- Refreshing modules
- Replacement module definition
- Disbanding of modules

The 3DX Canvas has demonstrated improvement compared to the legacy 3D applications in speed and memory utilization. The loading of designs is now at least 20 times faster and there is a 10X reduction in memory usage for large designs.

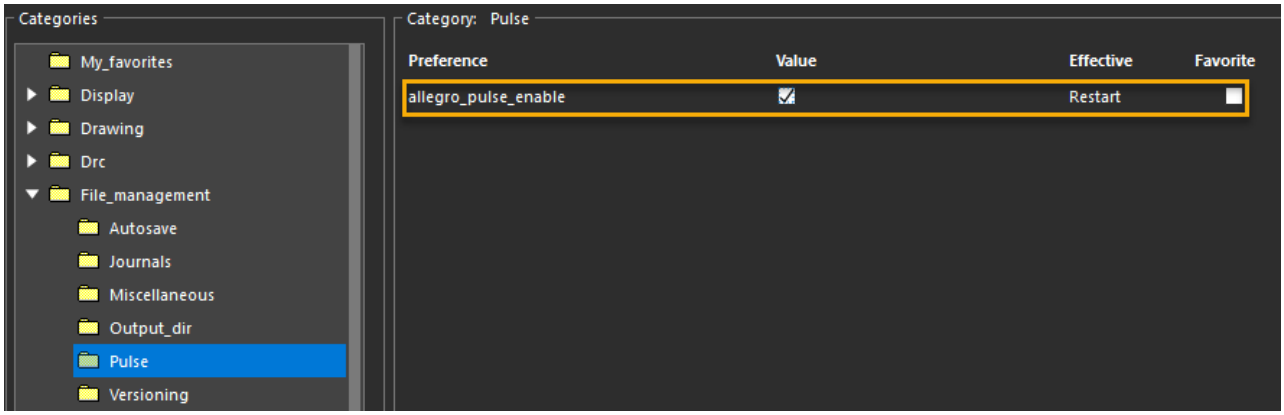
Library and Symbol Updates Using Allegro X Pulse

Note: These enhancements are only available in Allegro X PCB Editor.

You can now search and download library elements, such as padstacks or shapes, using the HTTP protocol instead of only accessing libraries on disks using the PSMPATH and PADMPATH variables. You can set *allegro_http_library_source* under *Paths – Library* to EDM to specify the source as a Pulse server or set the to OrCAD X Cloud to query and download library elements from the Cloud. You must restart the application after setting the variable to see the changes.



You can now use Symbol Revision Manager (*Place – Symbol Revision Manager*) to update Allegro symbols without the Flow Manager if you set *allegro_pulse_enable* under *File_management – Pulse* and restart the application.



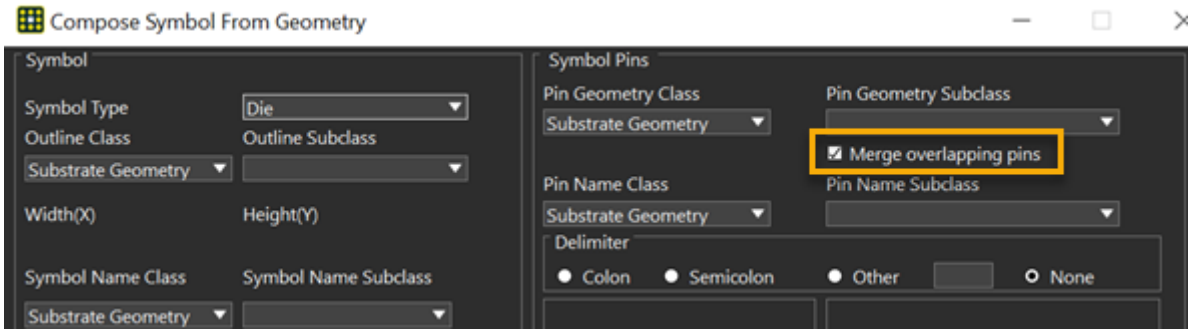
Miscellaneous Enhancements

This release has the following miscellaneous enhancements:

Compose Symbol Merge Option for Overlapping Pins

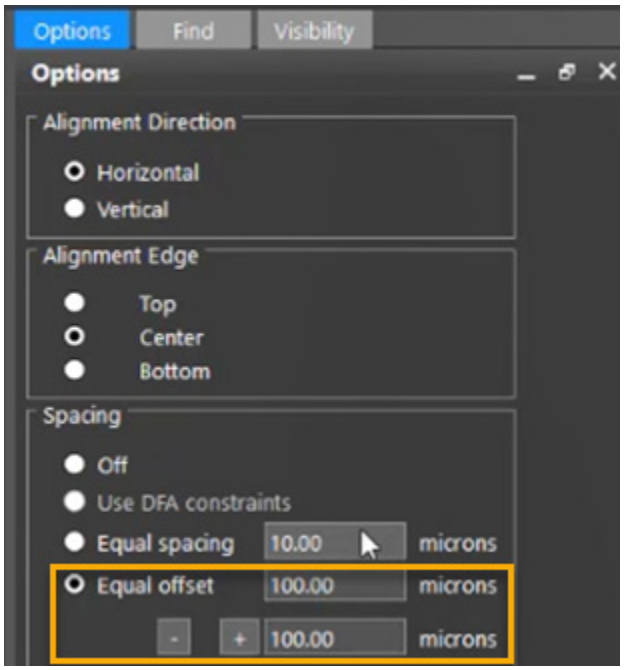
Note: This feature is available only in Allegro X Advanced Package Designer.

You can now select to merge two pins that touch or overlap into a single pin using the *Merge overlapping pins* option in Compose Symbol from Geometry. The option is selected by default.



Aligning Components by Offset

Now you can align components using the new offset mode. Selecting the new mode gives center to center offset with stepping increments.

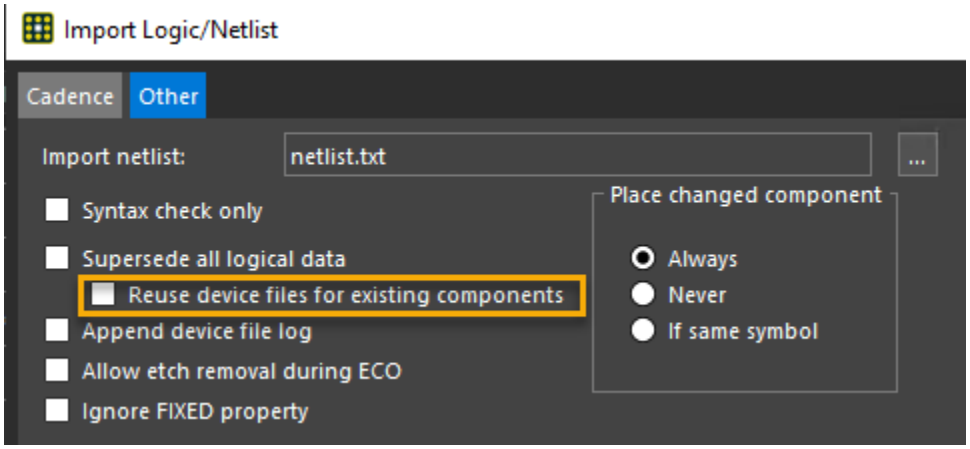


Retaining Original Definition After Optical Die Shrink

You can now save the original definition of a die in the database on applying an optical shrink.

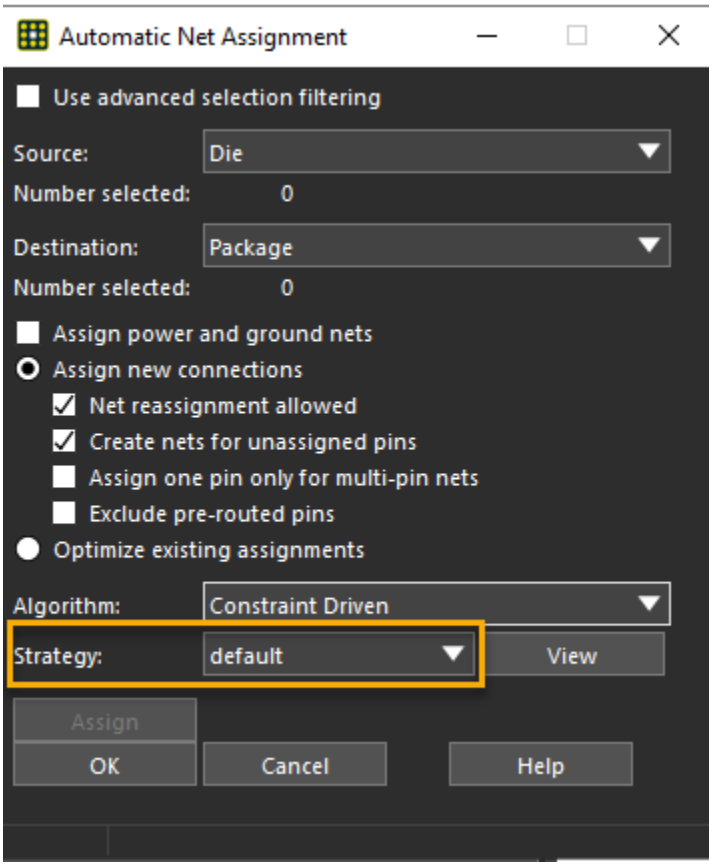
Device File Reuse for Existing Components for Netlist and Logic Import

Now, you can reuse device files for existing components without first adding the components to libraries even for net name changes. The Import Logic/Netlist dialog box (*File – Import – Logic/Netlist*) now has the *Reuse device files for existing components* option. This option is not selected by default.



Easy Access to Strategy Files

Now, you can easily access strategy files while assigning nets automatically in the constrained-driven flow.



You can have different weights for objects depending on the type of nets being assigned.

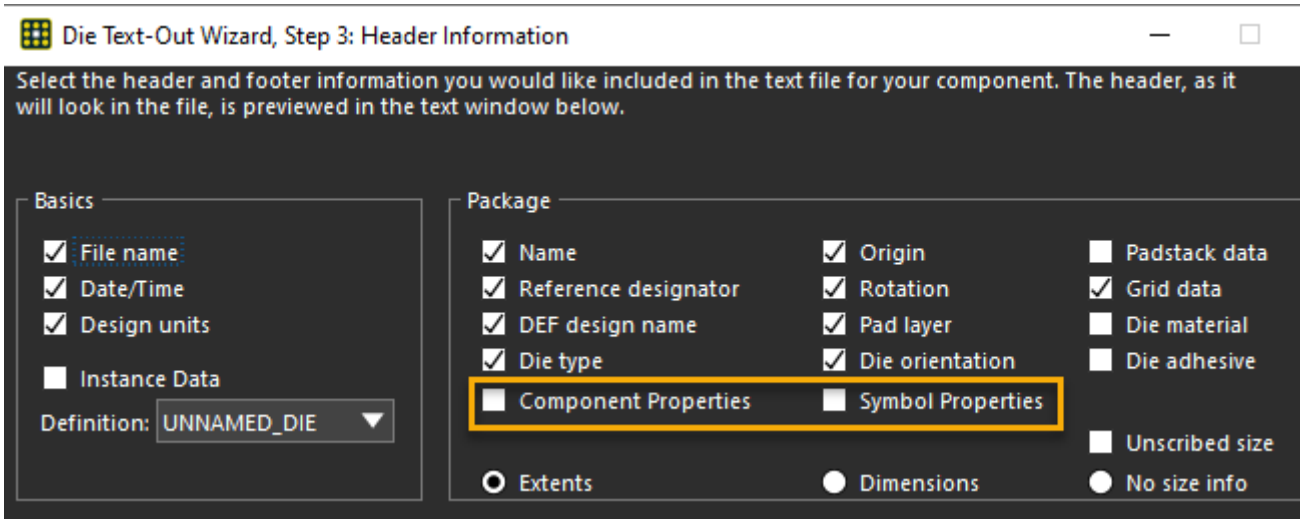
```
#########################################################
# Weighted Rules (0 = unused; 1 = min; 99 = max penalty) #
#########################################################

AssignAllNets                99
PhysicalViolation            95
DiffPair                        90
MinLength                       95
MaxLength                       95
RelativeLength               85
MatchLength                     80
PinCode                         50
SwapCode                        25

#################################
# Assignment Parametric Controls #
#################################

HowHardToTry                 Low                              # Low | Middle | High
DiffPairOrientation          Adjacent                  # Adjacent | Tandem | Diagonal
AssignFirst                         RingToRing                # Middle | Corners | RingToRing
LayerBalance                 EvenDistribution      # FillLayers | EvenDistribution
NetLengthBalance             Average                   # Average | Minimize | Maximize
MultiNetScheduling           Independent               # Independent (pin to pin) | MST
```

Text Wizard Enhancements

Text wizards have been enhanced with the following changes in this release:

- Export and import symbol and component properties.

  Now, you have options to export symbol and component properties.



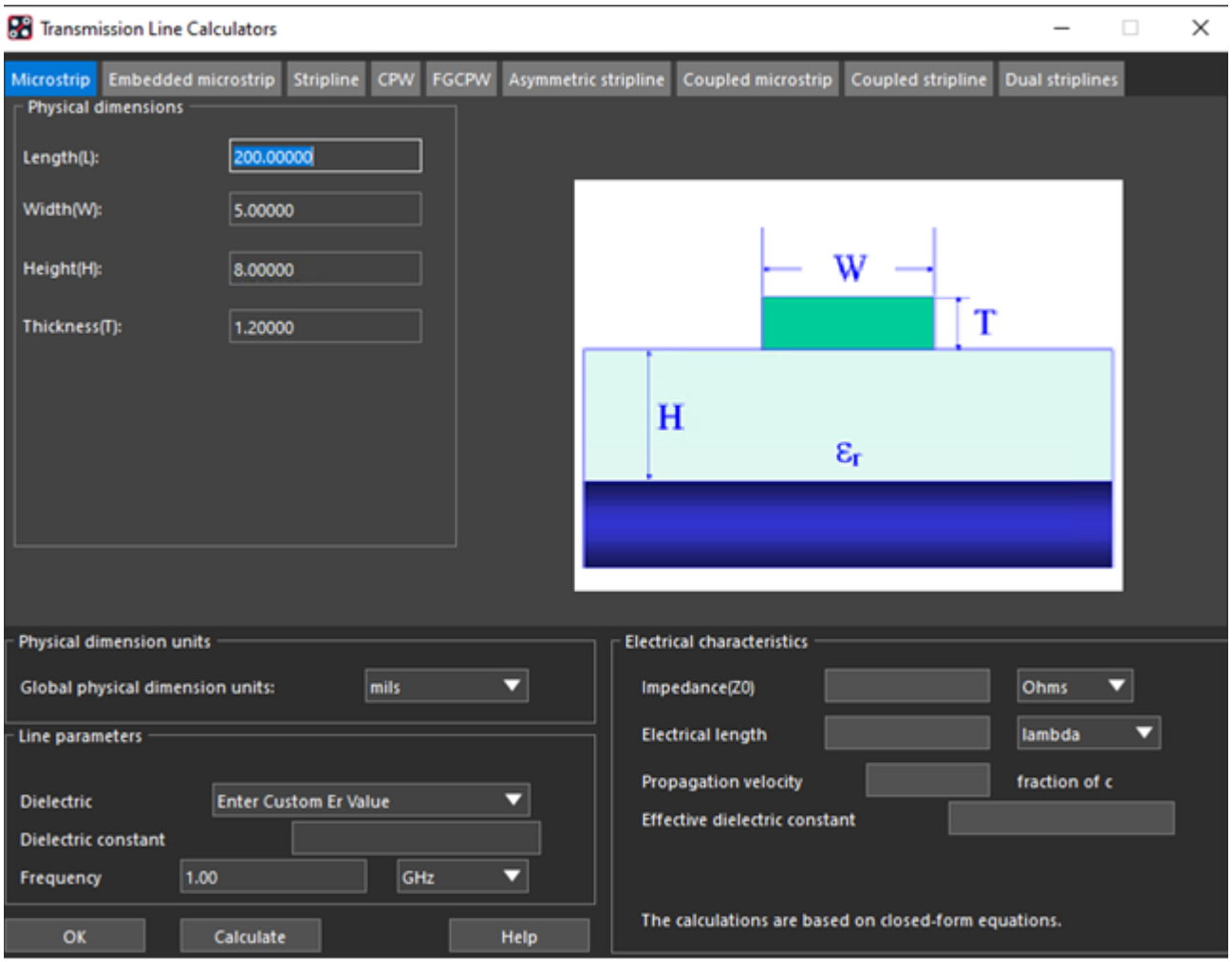
On import, the properties are applied to the listed object types. You can apply the properties to one or all instances of a component in a design.

- Configure the default state of derive assignment option

  To set the default state of derive assignment related options in wizards, configure the *icp_derive_assign_default_value* under *Ic_packaging* in User Preferences Editor.

Transmission Line Calculators in Allegro X Advanced Package Designer

Now, you can access Transmission Line Calculators (*Analyze – Transmission Line Calculator*) from Allegro X Advanced Package Designer.



You can use Transmission Line Calculators to calculate the correct stackup material and width or spacing to meet any requirements that may be later entered in a constraint.

Use the calculators if you need to test a quick spacing or width as per the impedance value. Use simulators for more precise results.

Quick Access to Snap Window

You can now access all *Snap pick to* commands immediately by pressing `Shift` with right-click.

SKILL Support for Expanded Hole Checks

In this release `axlCNSSetSpacing` and `axlCNSSetSameNet` are updated to include constraint symbols to support expanded hole checks: Thru Via, BB Via, Microvia, and Pin Hole.

Creating Mechanical Devices using axlCreateDeviceFileTemplate

You can now create mechanical devices using `axlCreateDeviceFileTemplate`.