

Topology Workbench: Parallel Bus Analysis Tutorial

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Topology Workbench: Parallel Bus Analysis Tutorial

Parallel Bus Analysis Tutorial: An Overview

The Parallel Bus Analysis (PBA) workflow of Topology Workbench is an end-to-end solution that targets analysis of source-synchronous parallel interfaces such as designs with DDRx memory. Pre-layout capabilities enable you to begin with models that are quickly generated and connected. As the design is refined, more detailed models can be swapped in to reflect actual hardware behavior. Concurrent simulation accounts for the effects of dielectric and conductor losses, reflections, inter-symbol interference (ISI), crosstalk, and simultaneous switching noise. These simulations are able to fully account for the effects of non-ideal power-delivery systems. Graphical outputs and post-processing options give insight for rapid system improvements.

For detailed conceptual information, see the [Using Parallel Bus Analysis Workflow](#) chapter of the [Topology Workbench User Guide](#).

Organization of this Document

Each chapter in this tutorial has been written to be a standalone module that covers specific tasks. Review the following chapters for the typical steps you will perform to create, edit, and simulate a parallel bus interface:

<u>Chapter 1, “Parallel Bus Analysis Tutorial: An Overview”</u>	
	This is the current chapter. It covers the basic overview of the PBA tutorial and the additional resources.
<u>Chapter 2, “Getting Started with Parallel Bus Analysis”</u>	
	Covers the information to introduce you to the PBA workflow of Topology Workbench using a default template from the install hierarchy that contains a simple data bus with non-ideal power. Also, provides reference information including details related to an IBIS model file.

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Parallel Bus Analysis Tutorial: An Overview

Chapter 3, “Creating a Blank Topology and Assigning Device Models”

Provides a step-by-step overview of how to create from scratch a new DDR3 design having a Controller, Memory device, PCB and VRM.

Chapter 4, “Extracting and Generating an Interconnect Model”

Details the procedure of assigning to the PCB block a circuit file that describes it. The chapter also walks you through the process of extracting an S-parameter description of a board using Sigriity PowerSI

Chapter 5, “Connecting the Blocks”

Covers information about how to connect all the blocks in the DDR3 design.

Chapter 6, “Running Simulations and Analyzing the Results”

Covers information about the basic simulation settings and how to simulate a bus design. It also shows how to review the simulation results.

Sample Test Case Files

The test case files provided along with this tutorial can be classified into two types: default templates and samples.

- The default template files for Chapter 2 are accessible from the Topology Workbench interface.
- The sample files for Chapter 3 through 6 are in the `<INSTALL_DIR>\share\topxp\Tutorials\PBA_Tutorial` directory.

Note: Instead of updating the files in the sample directory, it is recommended that you copy these files to your working directory and work on them.

This tutorial document does not provide conceptual details or familiarity with different user interface elements. For such information, refer to the documents listed in the Related Documents section.

Related Documents

In addition to this tutorial, you can refer to:

- *Topology Workbench Frequently Asked Questions* to find answers to a few commonly encountered questions.

Topology Workbench: Parallel Bus Analysis Tutorial

Parallel Bus Analysis Tutorial: An Overview

- *Topology Workbench User Guide* for detailed procedural information related to SI Exploration, Parallel Bus Analysis, Serial Link Analysis, AMI Builder, and Compliance Kits workflows of Topology Workbench.
- *Topology Workbench: SI Exploration Tutorial* captures the step-by-step instructions on exploring the Topology Workbench canvas, creating a topology from scratch in the Topology Explorer workflow, doing pre-layout extraction and post-layout routed interconnect extraction, and updating the ECSet using Constraint Manager.

Additional Learning Resources

Cadence offers training courses that enable you to understand the applications better. For specific information about the courses available in your region, visit [Cadence Training](#) or write to training_enroll@cadence.com.

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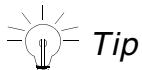
Parallel Bus Analysis Tutorial: An Overview

Getting Started with Parallel Bus Analysis

This chapter explains how to create a new project for *Parallel Bus Analysis* using a default template. It also familiarizes you with the Topology Workbench interface and the properties of the blocks placed in the default template. Finally, the chapter covers how to augment an associated I/O Buffer Information Specification (IBIS) file.

Create a New Template-Based Topology

1. Start Topology Workbench in standalone mode.
 - ❑ In Windows, use one of the following ways:
 - *Start — Run*, and type `TopWb`
 - *Start — Programs — Cadence PCB <release_number> — Sigrity Topology Explorer*
 - ❑ In UNIX, type `TopWb` in a Shell window.
2. Select *Advanced SI* from the *Cadence Product Choices* dialog box and click *OK*. This product choice lets you focus on analyzing advanced source-synchronous parallel buses (for example, DDR).

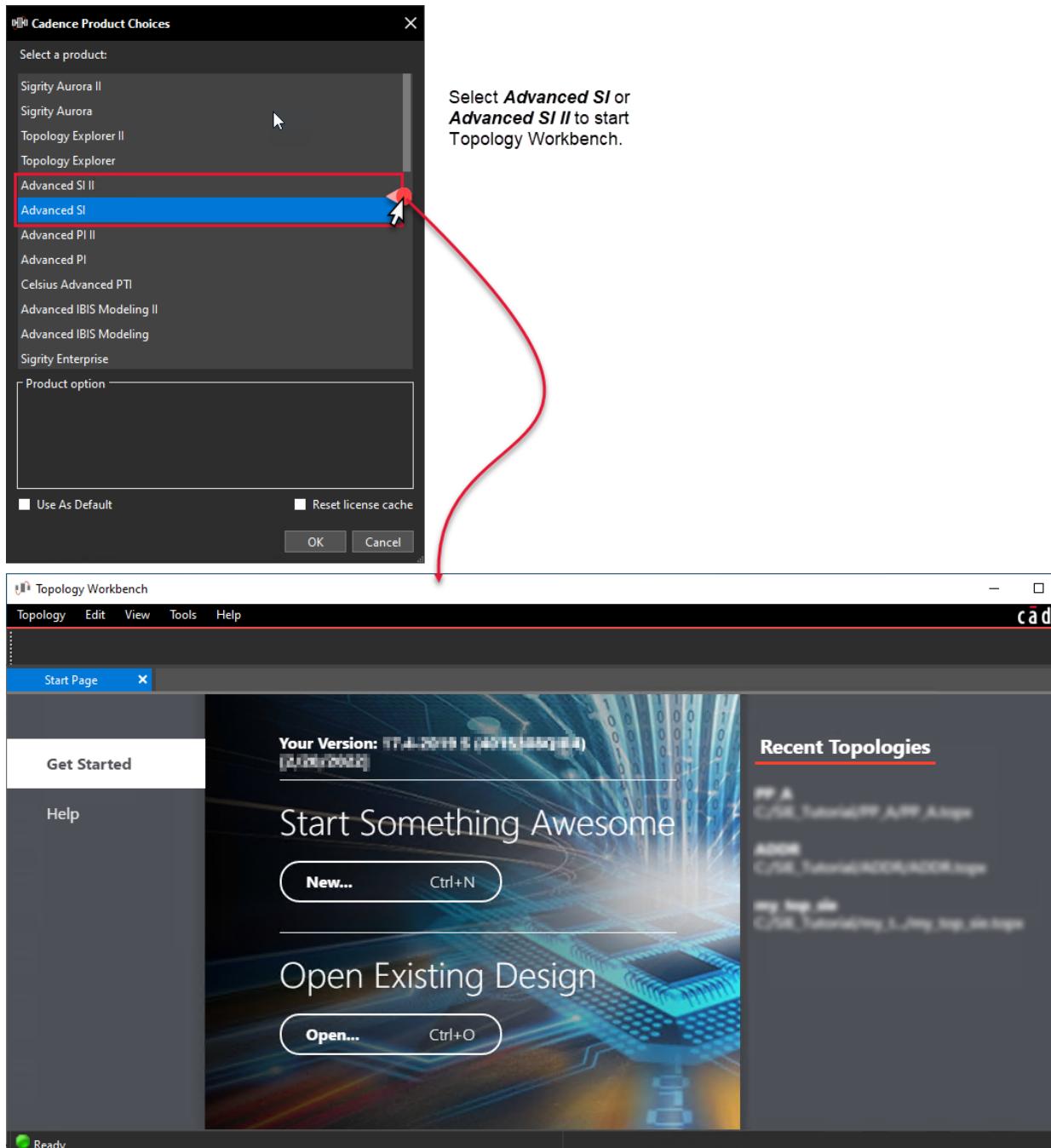


You can alternatively select *Advanced IBIS Modeling* if you want to develop I/O Buffer Information Specification (IBIS) models, including Algorithmic Modeling Interface (AMI) functionality for equalization.

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Getting Started with Parallel Bus Analysis

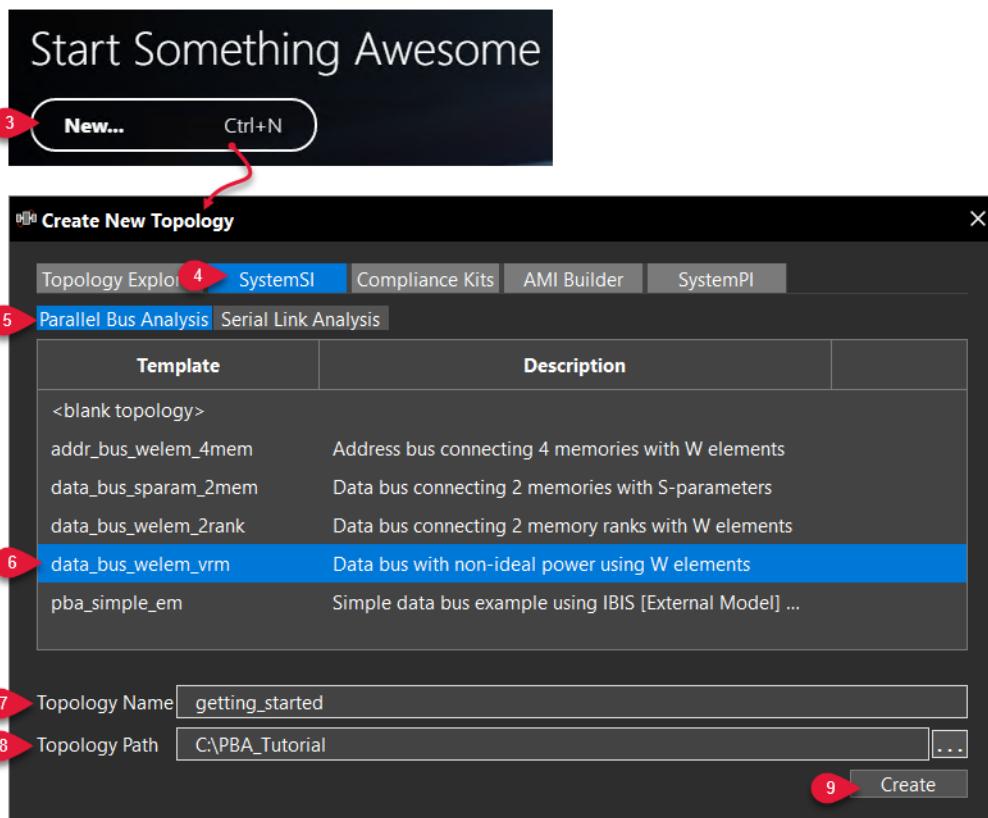
The Topology Workbench window opens with the *Start Page* tab in focus as shown below.



Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

3. Click *New...* from the *Start Something Awesome* section on the *Start Page* tab. The *Create New Topology* dialog box is displayed, as shown below.



4. Click the *SystemSI* tab.
5. Click the *Parallel Bus Analysis* tab. The table in this tab shows a list of default templates associated with the PBA workflow.
6. Select *data_bus_welem_vrm*.
7. Type *getting_started* in the *Topology Name* box.

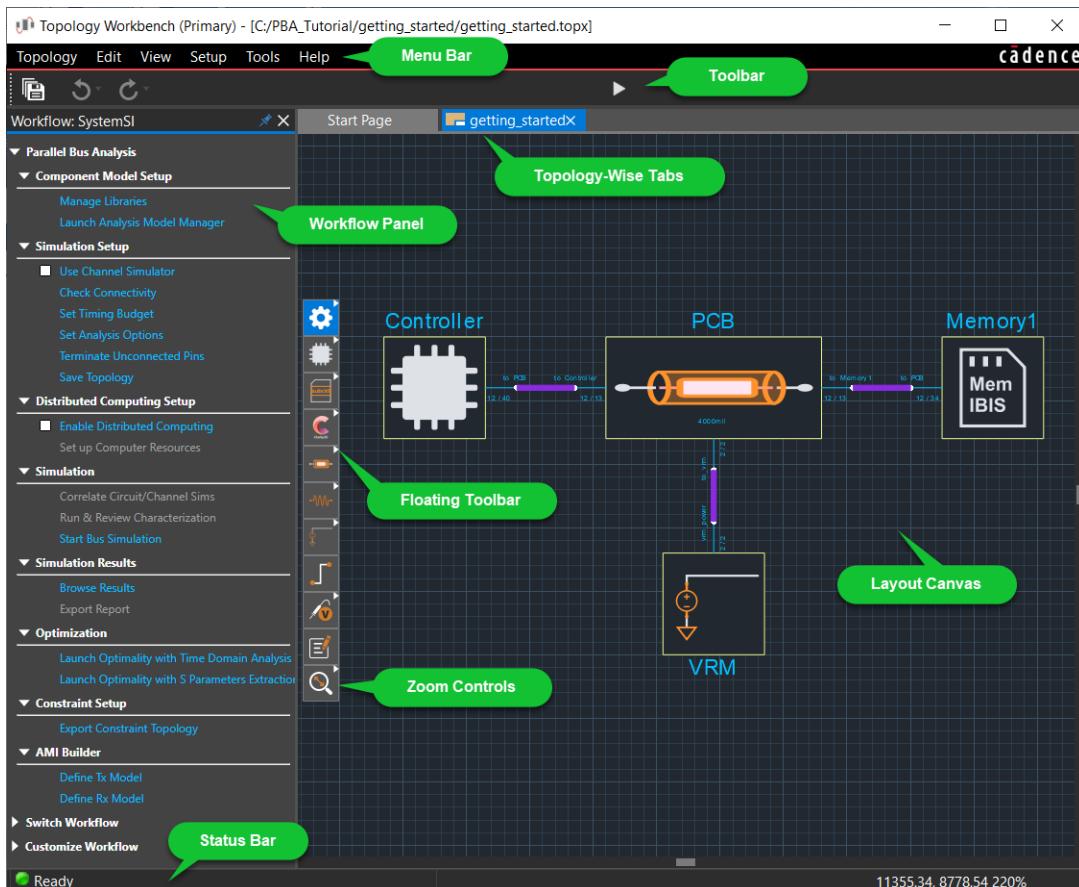
Note: A topology's name can contain only lowercase alphanumeric characters and underscores. If a topology with the same name exists already, a message is displayed to confirm if you want to overwrite it.

8. Browse and set the *Topology Path* to the directory where the new topology and related files should be saved on the hard drive. For example, we have browsed and selected the *PBA_Tutorial* directory, which we had created before starting this tutorial.

Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

9. Click *Create*. The block diagram based on the selected template opens in the layout canvas of the Topology Workbench window.



This block-based topology is a pre-constructed, ready to simulate template, consisting of a controller and a single memory device. The IBIS models are defined, edited, and linked to the devices. The PCB interconnects are coupled transmission line models, consisting of HSPICE W-element components. There is also a Voltage Regulator Module (VRM) block that has power supply explicitly defined. This is required for simulations including non-ideal power (that is no “ideal power” assumption at the IO models). In the sections that follow from here, let us review each block to note its properties and connectivities.

A subdirectory with the given topology name, *getting_started*, is created at the *Topology Path* you browsed to in [step 8](#). This directory contains the project file

Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

(*getting_started.topx*), and subdirectories for the model files associated with the various blocks, history, and simulation results.

Name	Date modified	Type	Size
asi_models	8/21/2023 8:01 PM	File folder	
history	8/21/2023 8:01 PM	File folder	
result	8/21/2023 8:01 PM	File folder	
getting_started.topx	8/21/2023 8:01 PM	TOPX File	60 KB
getting_started.topx.lock	8/21/2023 8:01 PM	LOCK File	1 KB
max_valid_electric_grid.txt	8/21/2023 8:01 PM	TXT File	1 KB
topxp.log	8/21/2023 8:01 PM	Text Document	1 KB

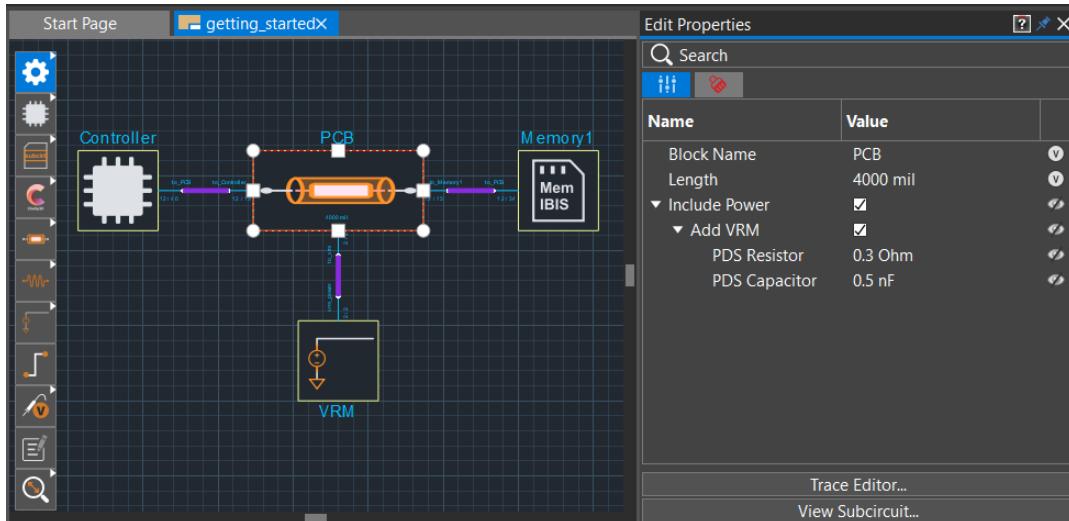
Edit the Components of Template-Based Topology

A double-click on a block or its pins opens the corresponding properties in the *Edit Properties* panel. To familiarize you with the properties of all four blocks in the *data_bus_welem_vrm* template, let us review each one by one.

PCB Block

The PCB block in the chosen template has been created using a Trace block that lets you leverage the advantages of pre-layout transmission line modeling capability.

1. Double-click the *PCB* block. The *Edit Properties* panel opens.

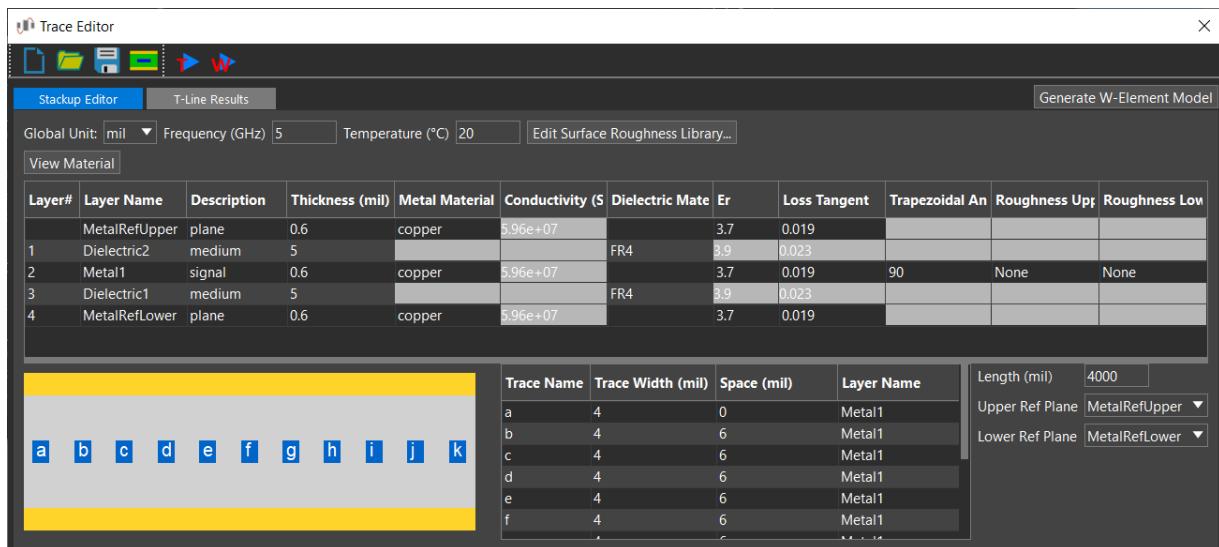


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In this panel, you can update the following properties: *Block Name*, *Length*, and *Include Power*.

2. Deselect the *Include Power* check box. Notice that the VRM block is removed from the canvas and the panel.
3. Select the *Include Power* check box again. On the canvas, a VRM block gets automatically connected to the PCB block and the *Add VRM* check box is displayed as selected in the *Edit Properties* panel. The editable *PDS Resistor* and *PDS Capacitor* boxes are also added with default values.
4. Click *Trace Editor*. The *Trace Editor* dialog box opens to let you define the properties of the transmission line (TLine) associated with the PCB block as illustrated in the image below.



5. Click the *Generate W-Element Model* menu item in the toolbar of the *Trace Editor* dialog box. It populates the model's information in the PCB block.

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Getting Started with Parallel Bus Analysis

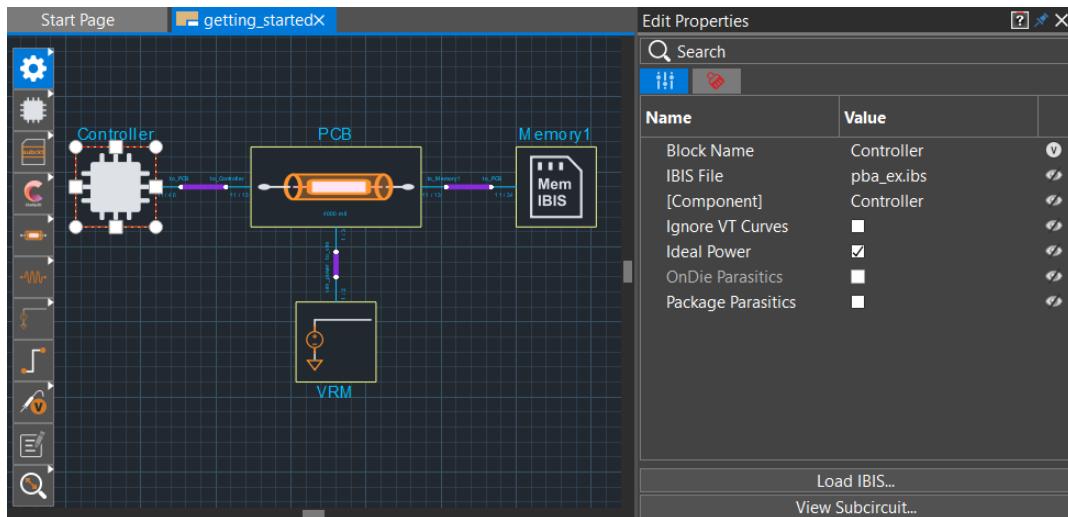
6. Click *View Subcircuit*. The *Subcircuit Editor* opens in read-only mode.



```
43 *|10 |K |L2 |2.54mm |0.1016mm
44
45 *[END]
46
47 ****
48
49 *WELEM FREQMAX = 5e+09 *
50
51 .Model DEFAULT_2DEM_MODEL W MODELTYPE=RLGC N=11
52
53 + L0=
54
55 + 3.39704e-07
56
57 + 2.50234e-08 3.38949e-07
58
59 + 1.97042e-09 2.49640e-08 3.38945e-07
60
61 + 1.55198e-10 1.96575e-09 2.49637e-08 3.38945e-07
62
63 + 1.22241e-11 1.54830e-10 1.96572e-09 2.49637e-08 3.38945e-07
```

Controller and Memory Blocks

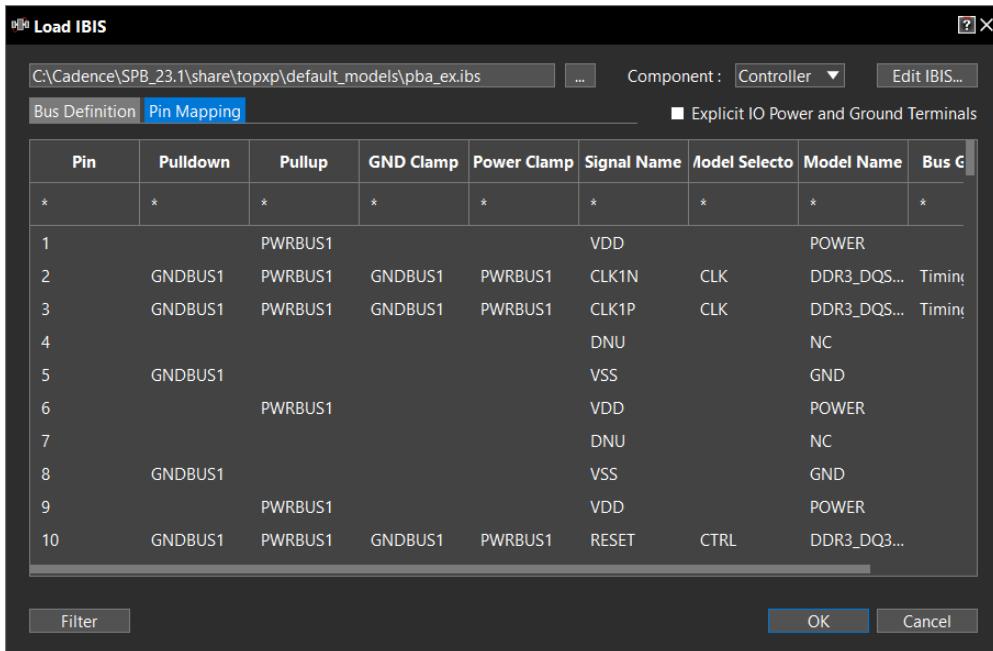
1. Double-click the *Controller* or *Memory* block. The *Edit Properties* panel opens with properties of the selected block on display for editing.



Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

2. Click the *Load IBIS* button and review the IBIS model definition for the selected *Controller* block.



Note: Topology Workbench uses IBIS models and allows both behavioral and transistor-level IO models for the devices used in the topology.

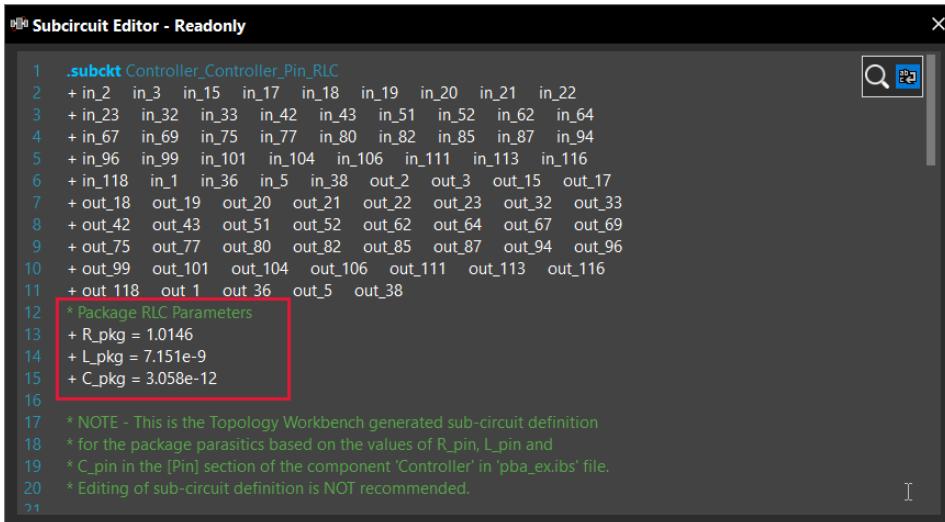
To learn the steps for modifying an IBIS model file, refer to the [Augmenting the IBIS File](#) topic.

3. Click *Cancel* to exit without making changes and return to the *Edit Properties* panel.
4. Ensure that the *Ignore VT Curves* check box is not selected. For Parallel Bus Analysis, this check box is unchecked by default so that the simulator takes into account the non-linear behavior of the drivers by reading the VT data.
5. Select the *Package Parasitics* check box to specify the package's resistor, inductor, and capacitor (RLC) parameters for the *Controller* block. The *Model Type* is set to *Pin RLC* by default.

Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

6. Click *View Package Subcircuit*, which is added to the panel when you select the *Package Parasitics* check box.

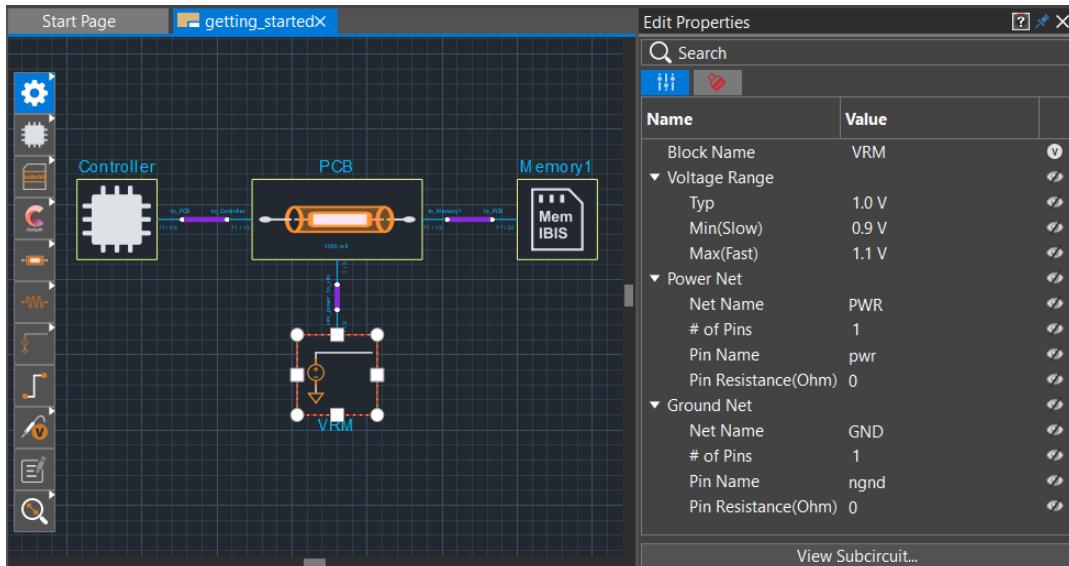


```
.subckt Controller_Controller_Pin_RLC
  + in_2  in_3  in_15  in_17  in_18  in_19  in_20  in_21  in_22
  + in_23  in_32  in_33  in_42  in_43  in_51  in_52  in_62  in_64
  + in_67  in_69  in_75  in_77  in_80  in_82  in_85  in_87  in_94
  + in_96  in_99  in_101  in_104  in_106  in_111  in_113  in_116
  + in_118  in_1  in_36  in_5  in_38  out_2  out_3  out_15  out_17
  + out_18  out_19  out_20  out_21  out_22  out_23  out_32  out_33
  + out_42  out_43  out_51  out_52  out_62  out_64  out_67  out_69
  + out_75  out_77  out_80  out_82  out_85  out_87  out_94  out_96
  + out_99  out_101  out_104  out_106  out_111  out_113  out_116
  + out 118  out 1  out 36  out 5  out 38
* Package RLC Parameters
+ R_pkg = 1.0146
+ L_pkg = 7.151e-9
+ C_pkg = 3.058e-12
* NOTE - This is the Topology Workbench generated sub-circuit definition
* for the package parasitics based on the values of R_pin, L_pin and
* C_pin in the [Pin] section of the component 'Controller' in 'pba_ex.ibs' file.
* Editing of sub-circuit definition is NOT recommended.
```

Note: The *Subcircuit Editor* displays the Topology Workbench generated subcircuit definition for the package parasitics based on the values of *R_pin*, *L_pin*, and *C_pin* in the *[Pin]* section of the IBIS file associated with the Controller block. The editor is opened in read-only mode because editing of the subcircuit definition is not recommended.

VRM Block

- Double-click the VRM block. The *Edit Properties* panel opens.



The VRM block for this template is simply an ideal DC supply of 1.5 Volts. The Parallel Bus Analysis workflow parameterizes the corner voltages here, including the *Typ*, *Min(Slow)*, and *Max(Fast)* VRM voltages, for fast and consistent simulation of the IBIS corner models.

Add New Blocks to the Canvas

To add new blocks to the schematic, select the required block from the floating toolbar, drag the mouse to the place where it needs to be positioned on the layout canvas, and click the canvas to release the block.

In the Parallel Bus Analysis workflow, you can choose from an array of blocks with single-ended, block-based signals.

Connect the Blocks

Until you connect one block to another, their connection ports appear as pink dots and indicate that no electrical model has been assigned to the block. Connecting all blocks on the canvas as per the design requirement helps to develop a circuit schematic and show the actual electrical connections between the blocks.

In the PBA workflow, when the *Block-Based* toggle button is selected in the *Settings* option of the floating toolbar, you can place blocks that have single-ended signals. For connecting signals of these type of blocks, Topology Workbench supports the block-based connectivity scheme. A block-based connection can be converted into a wire-based connection if required later.

To connect two blocks using the pin-to-pin method:

1. Click the connection port of the first block.
2. Move the pointer to the connection port of the second block. As the pointer moves, a line indicating the connectivity path trails.
3. Click the connection port of the second block to connect with the first block.

Configure the Connection Definitions

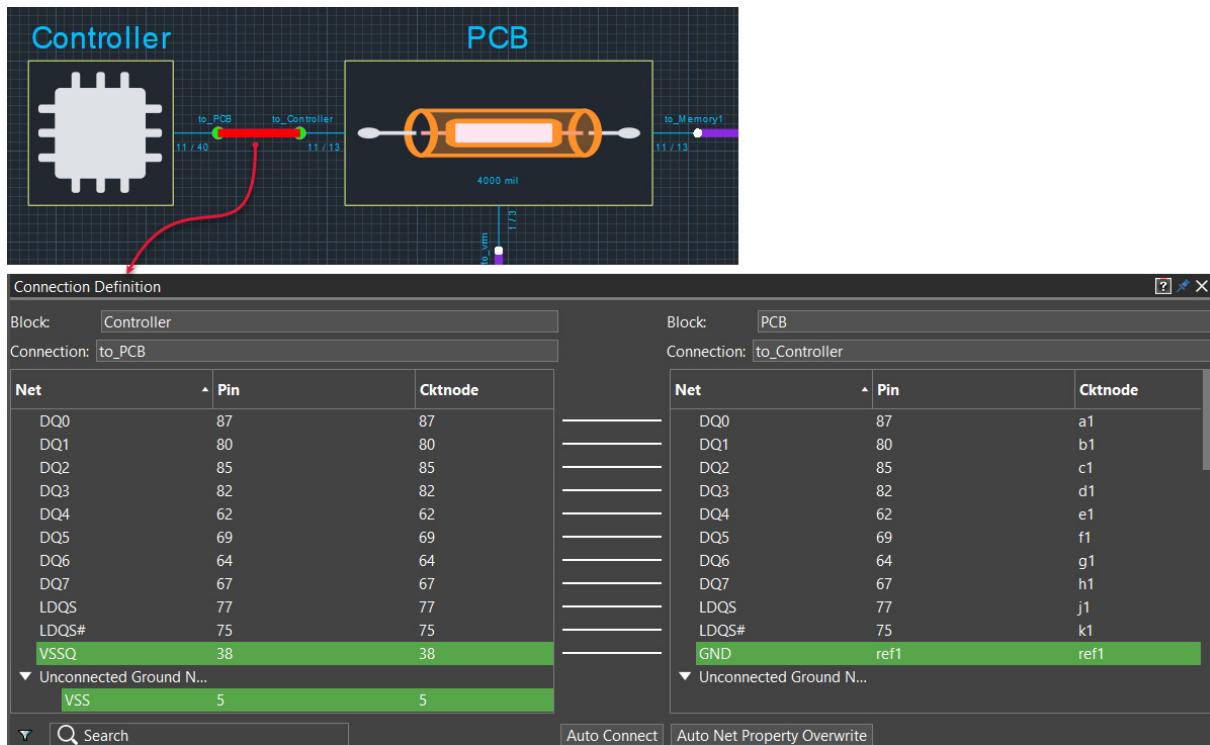
Block-based connectivity uses multi-pins where multiple signals are combined into a single connect point. Therefore, connections of such blocks need to be represented in a multi-pin or block-based connections netlist.

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The default blocks in the *data_bus_welcm_vrm* template already have sample connection definitions. You can configure the connections of the pins attached to two blocks as needed.

- Click the connection joining the *PCB* block to the *Controller* block to review their connection definitions. In the displayed panel, the connectivity between these two components, with specific pin-to-pin mapping, is shown.



Set Up the Analysis Options for Simulation

Before you simulate a design, basic simulation settings such as signals to be simulated, simulator to be used, simulation configuration, and simulation name can be specified in the *Analysis Options* panel. After specifying the simulation settings and running an initial simulation, you can make required changes to the design and simulation settings, and perform various experiments.

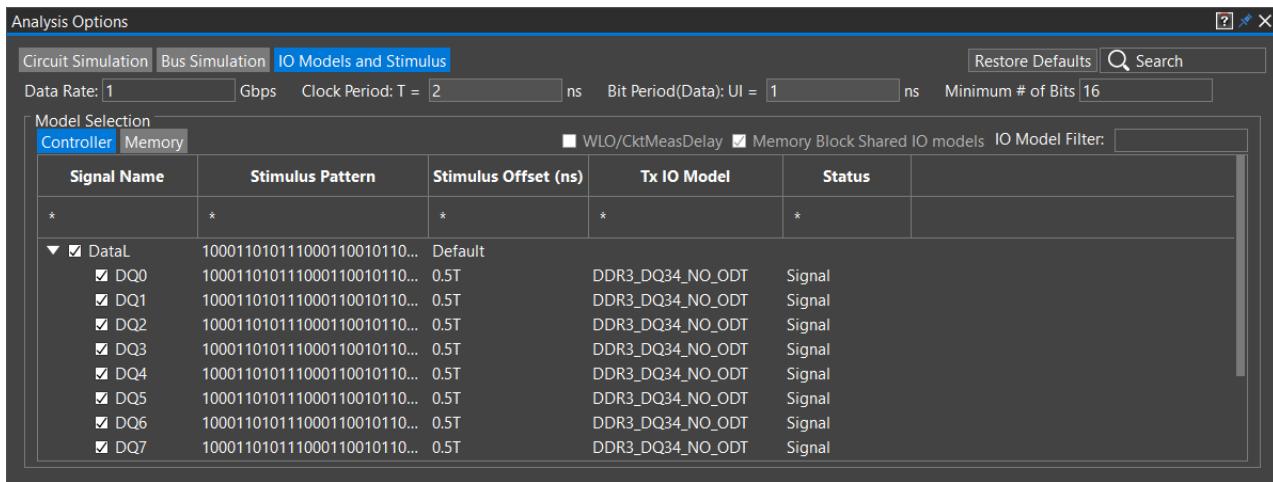
To open the *Analysis Options* panel, use one of the following methods:

- Click *Set Analysis Options* in the *Simulation Setup* schema of the *Workflow* panel.

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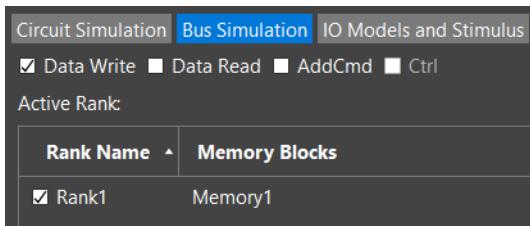
Getting Started with Parallel Bus Analysis

- Choose *Setup – Analysis Options* from the menu bar.



The key aspects for setting up the analysis options for a simulation run are:

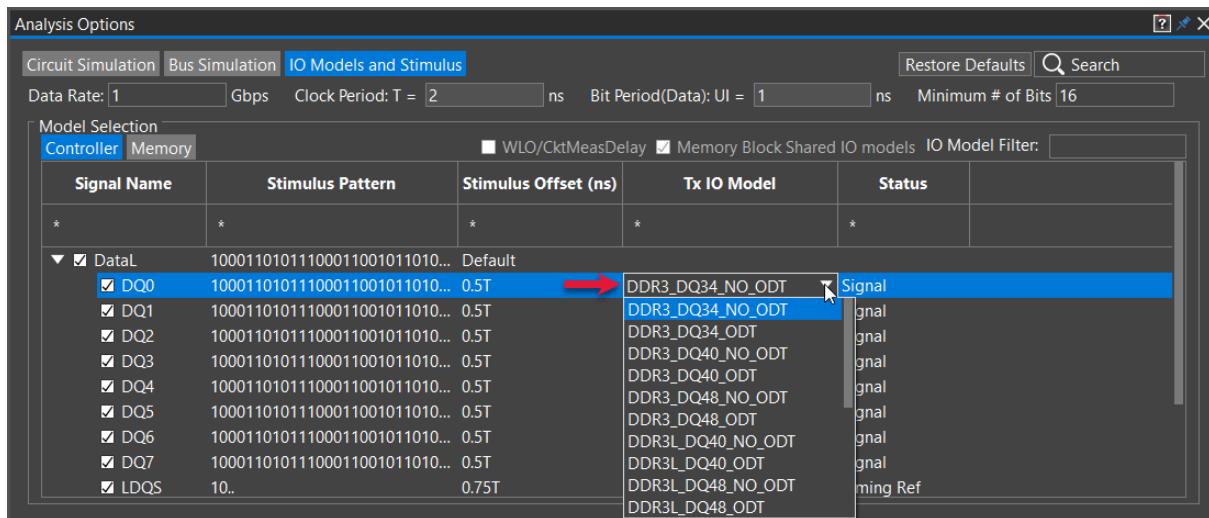
- If the design has more than one type of bus defined, define the bus type to be simulated. For this setting, open the *Bus Simulation* tab in the *Analysis Options* panel. Then select the required check boxes from the following available options to specify the bus type: *Data Write*, *Data Read*, *AddCmd*, and *Ctrl*.



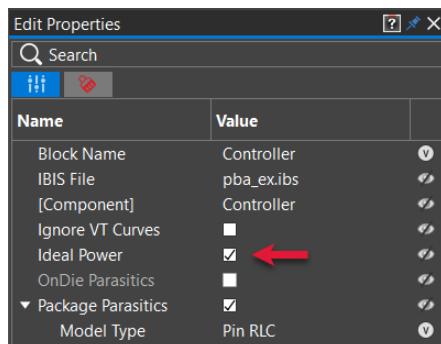
Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

- Select the IO models for Controller and Memory in the *IO Models and Stimulus* tab of the *Analysis Options* panel as shown below.



- Simulation can be run assuming ideal or non-ideal power. This can be set in the *Edit Properties* panel opened for a *Controller* or *Memory* block.



Set Up Probe Points

While performing parallel bus analysis in Topology Workbench, you can define the voltage and current probes. You can define both current and voltage probes using the *Probe Points* panel that can be accessed:

- from the canvas directly
 - or-
- by the *Setup – Probe Points* menu

Topology Workbench: Parallel Bus Analysis Tutorial

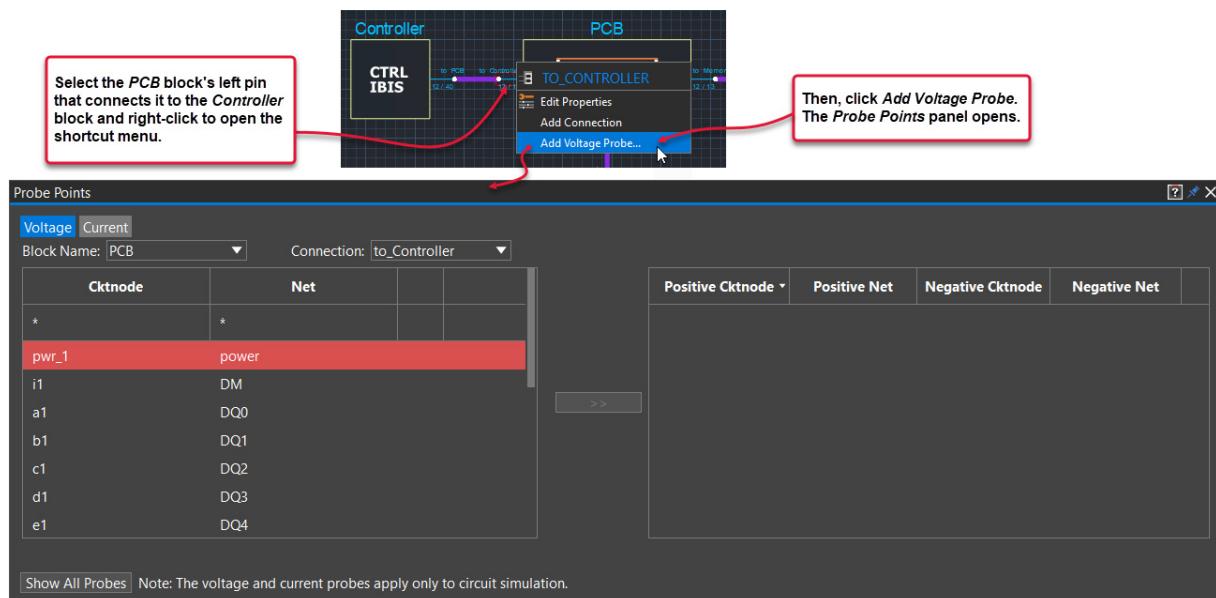
Getting Started with Parallel Bus Analysis

This topic covers information about how to [Add Voltage Probes](#) and [Add Current Probes](#).

Add Voltage Probes

To add three voltage probe points between *DQ0–GND*, *DQ2–GND*, and *DQ3–LDQS* on the pin connecting the *PCB* block to the *Connector* block:

1. Select the left pin of the *PCB* block and right-click to open the shortcut menu.
2. Click *Add Voltage Probe*. The *Probe Points* panel opens with the *Voltage* tab in focus.

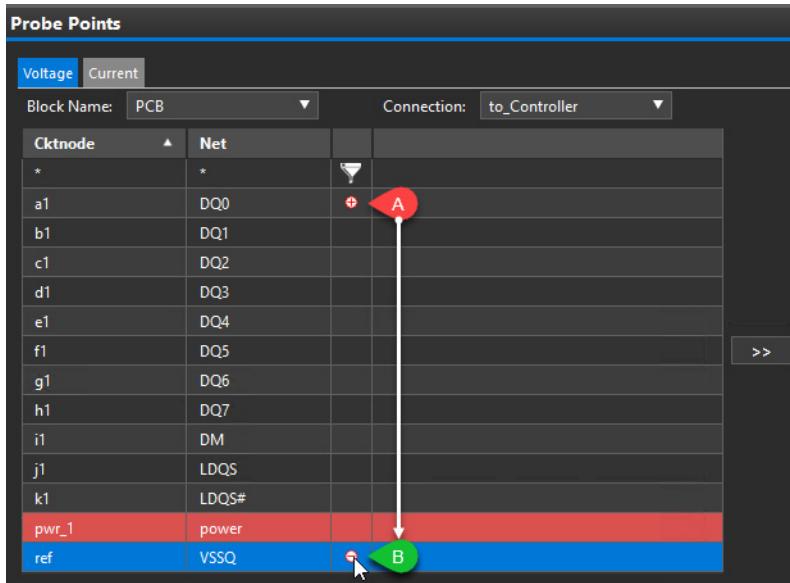


Note: In the PBA workflow, the voltage and current probes apply only to circuit simulation.

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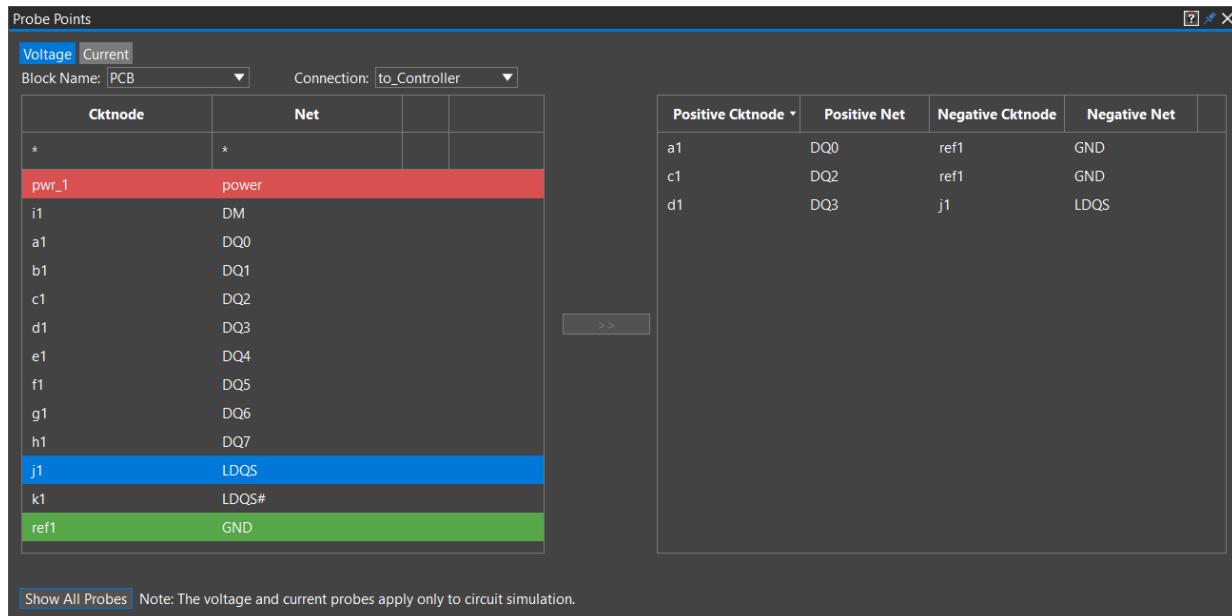
Getting Started with Parallel Bus Analysis

3. Select *DQ0* first and then select *GND*. Notice that the net you select first has a plus displayed adjacent to it (Positive Cktnode/Net) and the other net has a minus (Negative Cktnode/Net).



4. Click the >> button, which is placed between the two panes. The selected positive and negative circuit node – net name combination appears in the right pane.

Similarly, add probes for the remaining two net pairs, that is, *DQ2–GND* and *DQ3–LDQS*.



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5. Click *Show All Probes*. By default, all probe points are enabled.

Probe Points						
Voltage		Current				
Enab	Signal	Block	Connection	Positive Cktnode	Negative Cktnode	Custom Probe Name
<input checked="" type="checkbox"/>	DQ0-GND	PCB	to_Controller a1	ref1		PCB_a1_ref1
<input checked="" type="checkbox"/>	DQ2-GND	PCB	to_Controller c1	ref1		PCB_c1_ref1
<input checked="" type="checkbox"/>	DQ3-LDQS	PCB	to_Controller d1	j1		PCB_d1_j1

Add Probes Note: The voltage and current probes apply only to circuit simulation.

6. Deselect the check box adjacent to the *DQ3-LDQS* signal under the *Enable* column, as is shown below. This ensures that the deselected signal will not be probed during the simulation.

Probe Points						
Voltage		Current				
Enab	Signal	Block	Connection	Positive Cktnode	Negative Cktnode	Custom Probe Name
<input checked="" type="checkbox"/>	DQ0-GND	PCB	to_Controller a1	ref1		PCB_a1_ref1
<input checked="" type="checkbox"/>	DQ2-GND	PCB	to_Controller c1	ref1		PCB_c1_ref1
<input type="checkbox"/>	DQ3-LDQS	PCB	to_Controller d1	j1		PCB_d1_j1

Add Probes Note: The voltage and current probes apply only to circuit simulation.

7. Right-click the *DQ3-LDQS* signal's row to open the shortcut menu and click *Delete*, as is shown below. This removes the selected probe.

Probe Points						
Voltage		Current				
Enab	Signal	Block	Connection	Positive Cktnode	Negative Cktnode	Custom Probe Name
<input checked="" type="checkbox"/>	DQ0-GND	PCB	to_Controller a1	ref1		PCB_a1_ref1
<input checked="" type="checkbox"/>	DQ2-GND	PCB	to_Controller c1	ref1		PCB_c1_ref1
<input type="checkbox"/>	DQ3-LDQS	PCB	to_Controller d1	j1		PCB_d1_j1

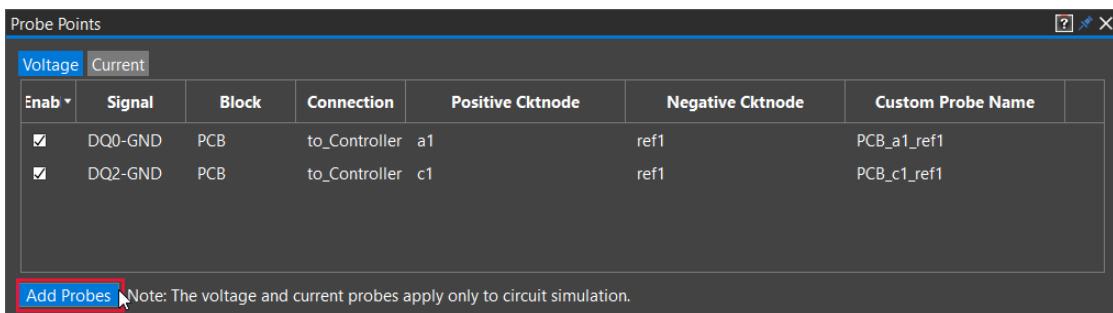
Delete Probe

Add Probes Note: The voltage and current probes apply only to circuit simulation.

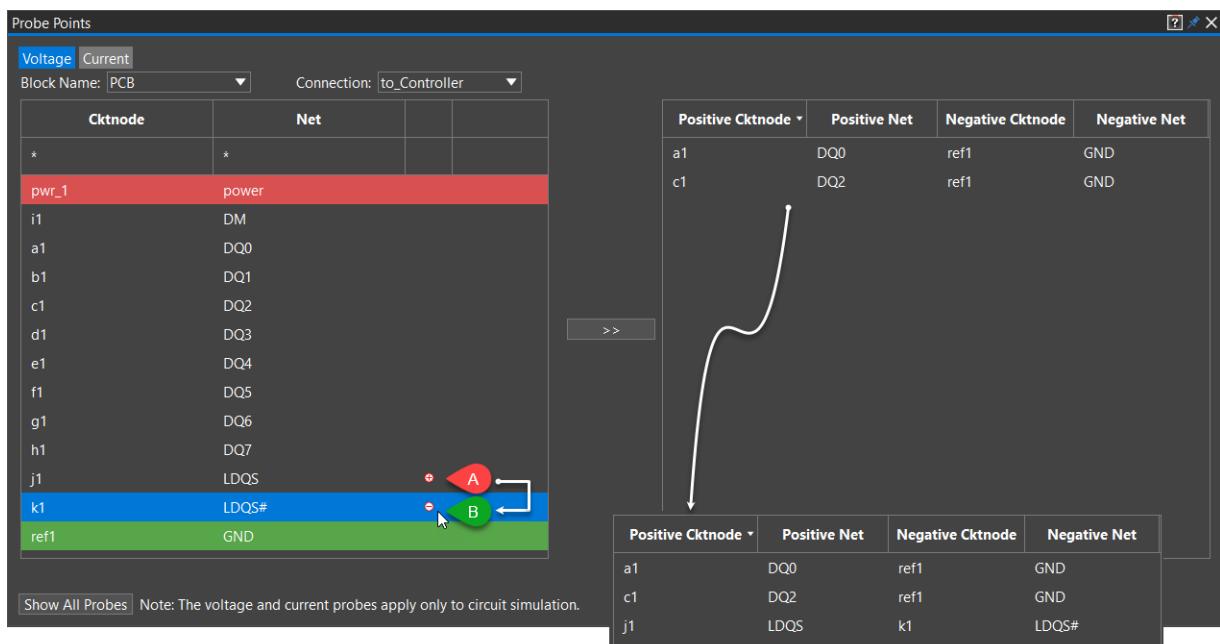
Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

8. Click the *Add Probes* button to add more probes. The contents of the *Voltage* tab are refreshed to display again the list of nets on which you can add probes and the ones on which a probe has already been added.



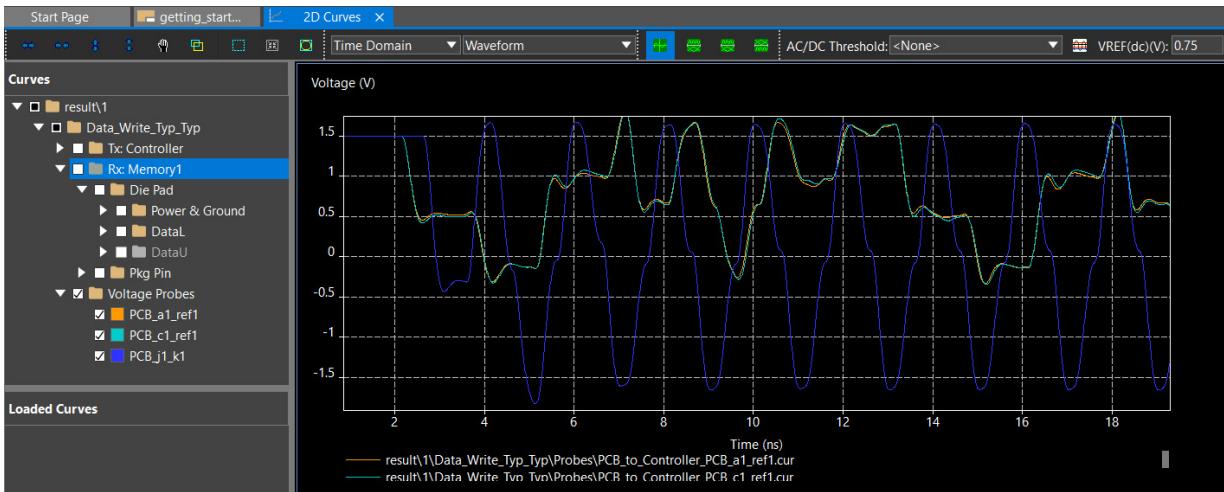
9. Select *LDQS* and then *LDQS#*, and click the *>>* button to add a new probe on this net pair.



Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

After the simulation, the curves of the defined probe points can be viewed in the *2D Curves* tab. For example, the following image shows how the waveforms are plotted if all three voltage probes we added above are simulated:



Add Current Probes

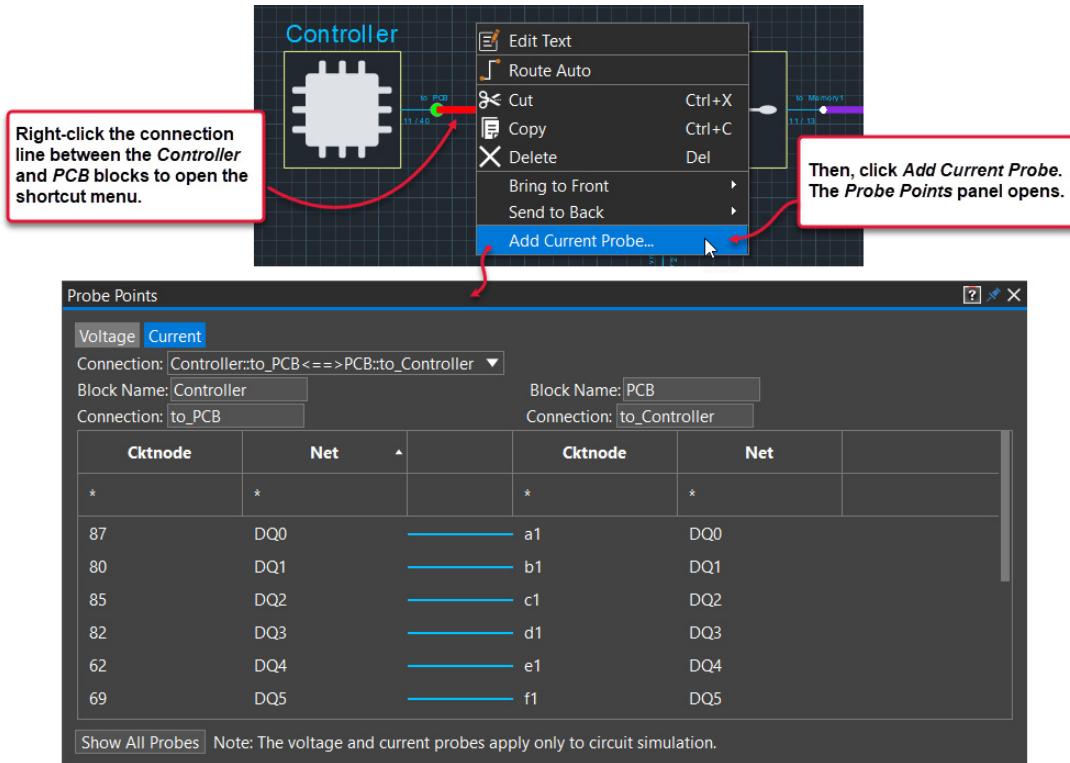
To add current probes on the connection between the *Controller* block and the *PCB* block:

1. Right-click the connection line that connects the two blocks to display the shortcut menu.

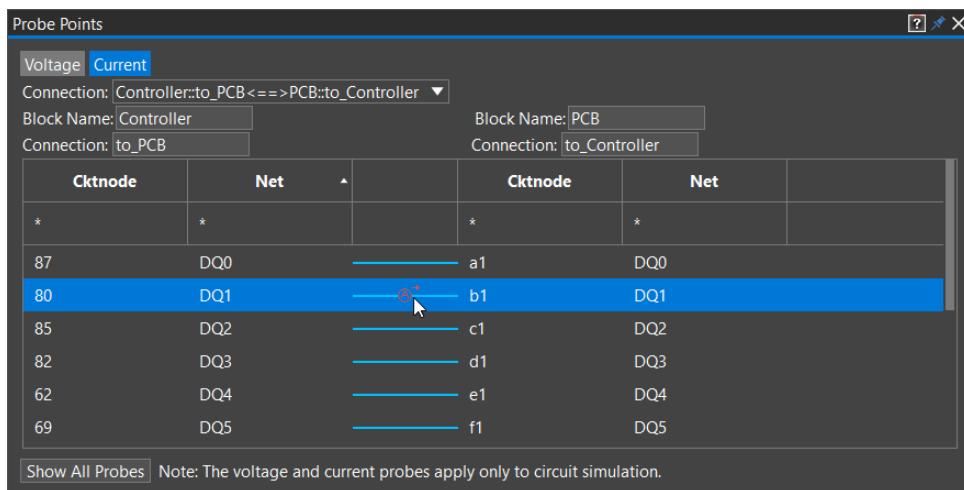
Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

2. Click *Add Current Probe*. The *Probe Points* panel opens with the *Current* tab in focus.



3. Double-click the connecting line between *DQ1* <<--> *DQ1*, which are the two nets that need to be probed. An icon is placed on the connection line indicating that the current probe as shown below.

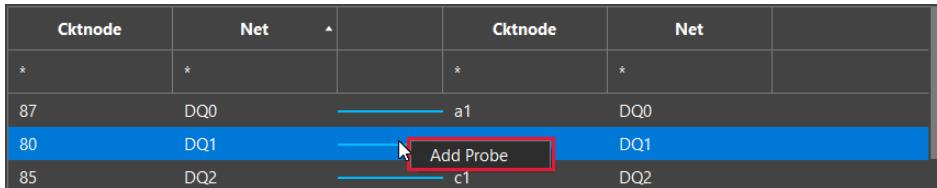


Note: In the PBA workflow, the voltage and current probes apply only to circuit simulation.

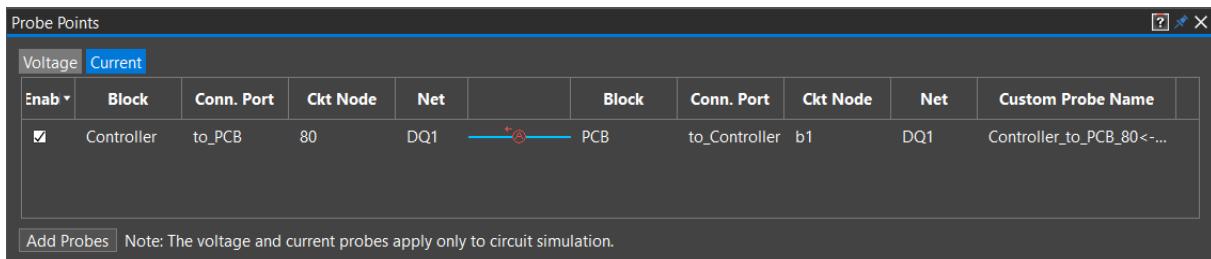
Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

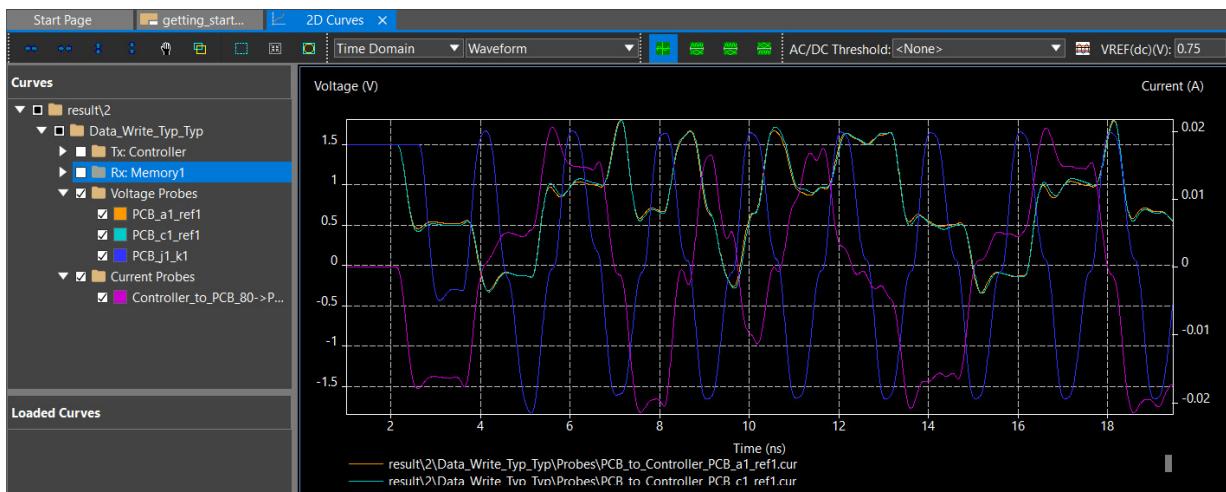
Alternatively, right-click the connecting line and select *Add Probe* from the displayed shortcut menu.



4. Click *Show All Probes* to view only those *Cktnode-Net* connections on which current probes have been set.



If you now simulate the design, the *Voltage Probes* and *Current Probes* nodes are displayed in the *2D Curves* tab.



Run the Simulation

1. Click *Start Bus Simulation* in the *Simulation* schema of the Workflow panel.

A message box is displayed to check if you want to verify the Min Transmit Setup and Min Transmit Hold specifications using the *Timing Budget* tool.

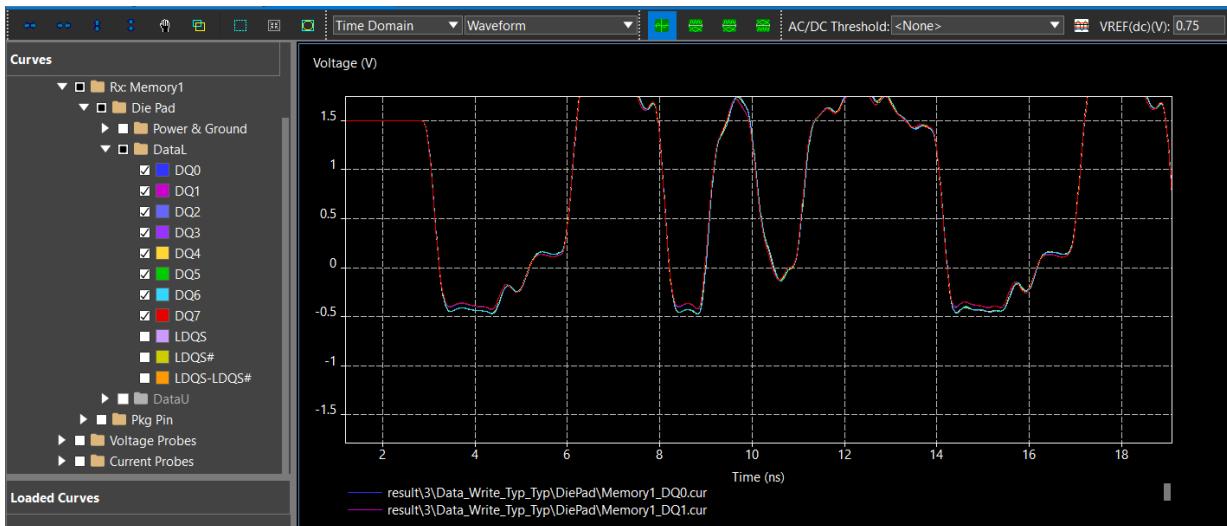
Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

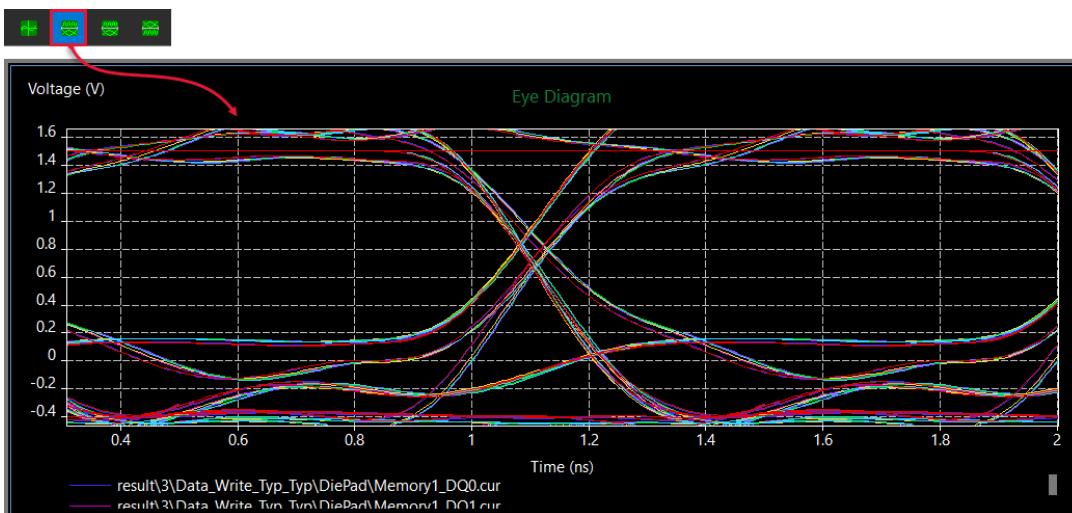
- Click No. The simulation's progress is displayed in the status bar of the Topology Workbench window.

If you click Yes instead, the *Timing Budget* panel opens to let you set up the custom timing specifications associated with the transmitting component.

On completion of the simulation run, waveform results are shown in the *2D Curves* tab.



- Use the toolbar icons to view the *Eye Diagrams* when *Time Domain – Waveforms* are selected.



Augmenting the IBIS File

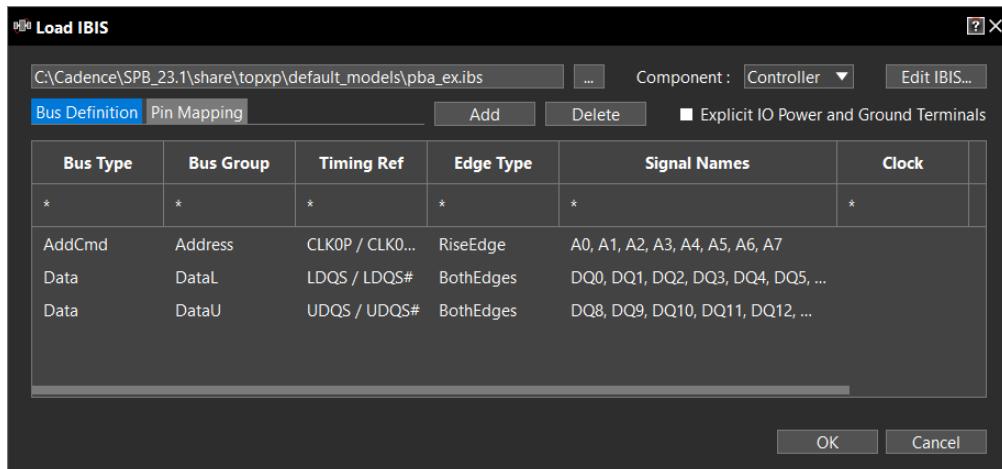
To enable the automation provided by Parallel Bus Analysis, some augmentation of the standard IBIS files is required. Specifically, the definition of bus groups, timing reference signals, and setup/hold specifications are needed. This can all be done through the Topology Workbench window, and the comments are automatically embedded into the IBIS file itself.

Before you start with the steps explained below, copy the following file:

Copy	From	To
topxp_pba_ex.ibs	<INSTALL_DIR>\share\topxp\default_models	<WORK_DIR>\PBA_Tutorial\getting_started\asi_models

Open the IBIS File

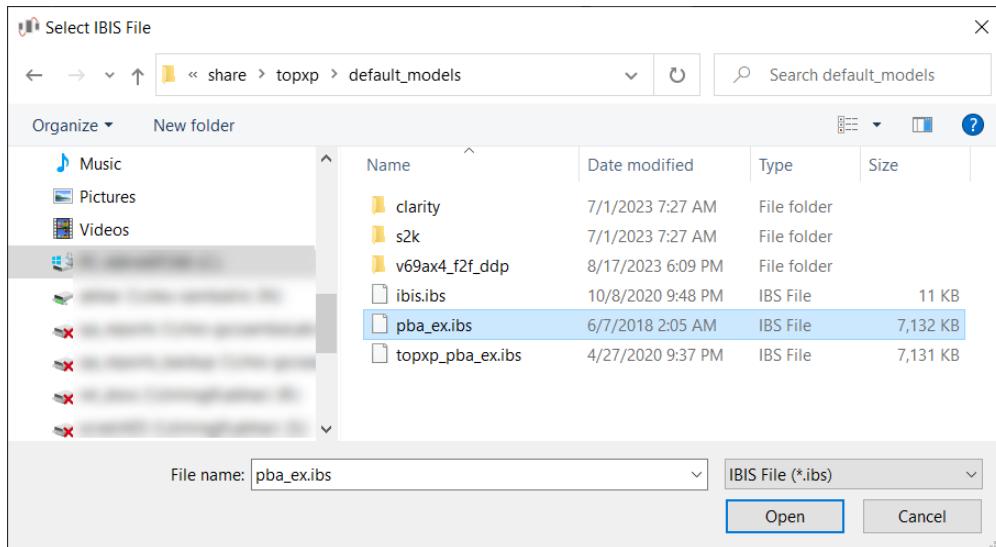
1. Click the *Controller* block to open the *Edit Properties* panel.
2. Click *Load IBIS*. The *Load IBIS* dialog box opens.



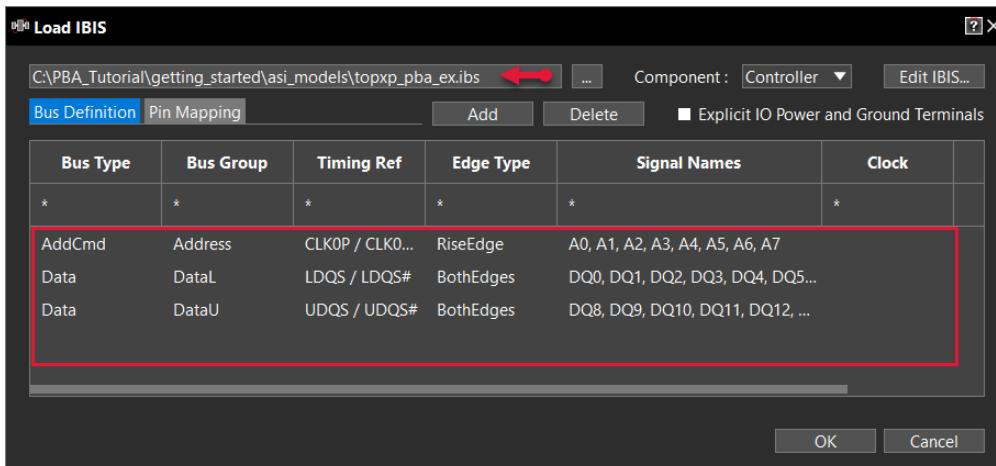
Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

- Click the browse (...) button adjacent to the box that contains the path to the currently selected default IBIS model file. The *Select IBIS File* dialog box opens.



- Browse to `<WORK_DIR>\PBA_Tutorial\getting_started\asi_models` where you had copied the `topxp_pba_ex.ibs` file at the beginning of this topic.
- Select the `topxp_pba_ex.ibs` file.
- Click *Open*. The *Load IBIS* dialog box shows the updated path to the IBIS file you selected. The file's contents are shown in the *Bus Definition* and *Pin Mapping* tabs.



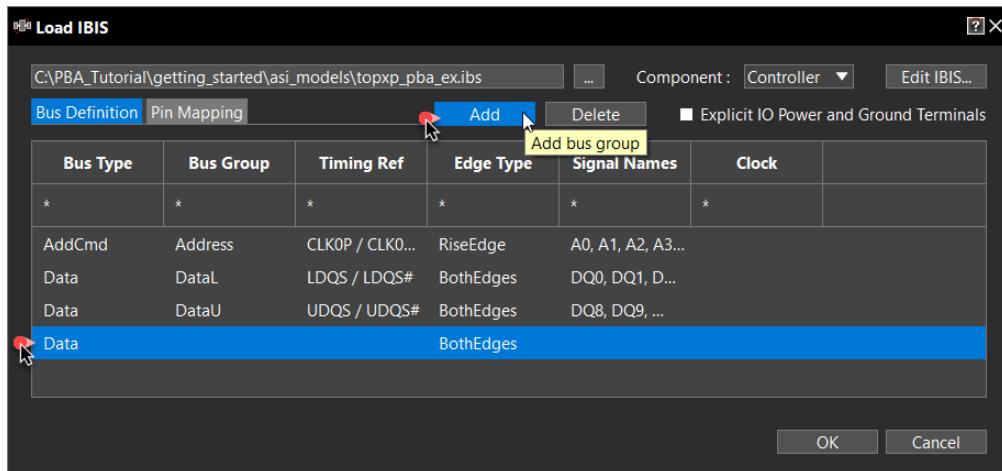
Edit the Bus Definitions in the IBIS File

- Review the buses list on the *Bus Definition* tab.

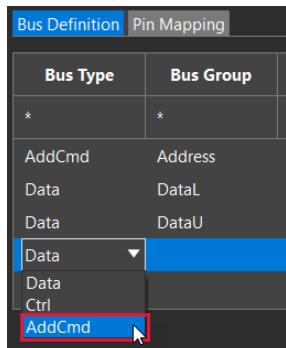
Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

- Click *Add* to add a new bus group. A new row gets added to the table with the *Bus Type* set to *Data* and *Edge Type* set to *BothEdges* by default.



- Click the cell under the *Bus Type* column and select *AddCmd* instead of *Data* from the list.

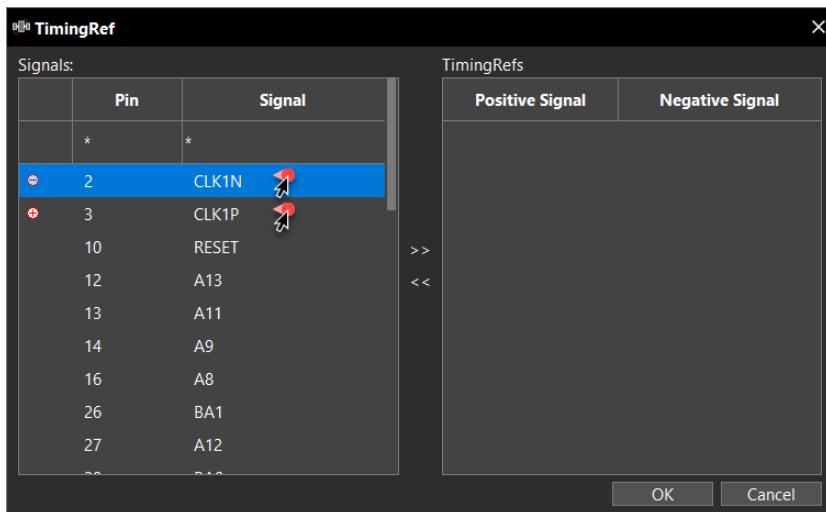


- Enter the *Bus Group* as *Calibration*.
- Click the adjacent cell under the *Timing Ref* column. The *TimingRef* dialog box opens.

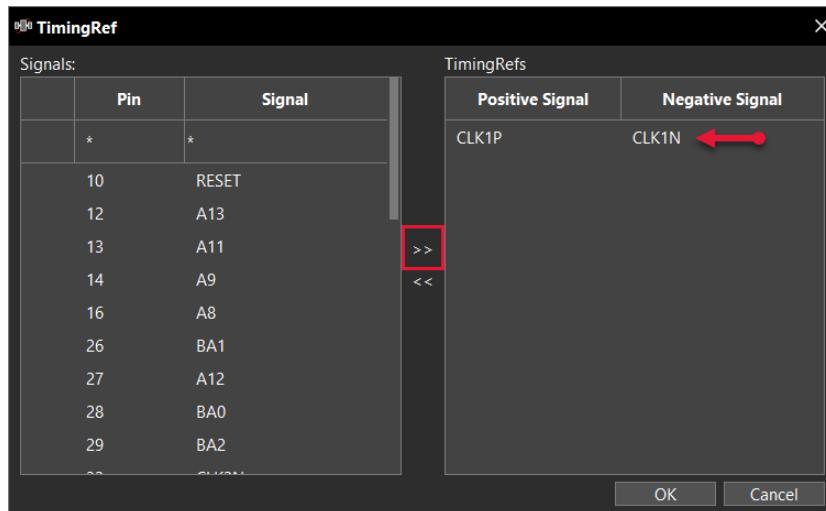
Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

6. Click *CLK1P* first to define the positive signal and then *CLK1N* to define the negative signal. Notice the plus and minus symbols that are added to the selected signals.



7. Click the >> button to move the selected signals to the *TimingRefs* table.



8. Click *OK*. The *TimingRef* dialog box closes and the *Timing Ref* column of the *Load IBIS* dialog box shows the newly added definition.

Topology Workbench: Parallel Bus Analysis Tutorial

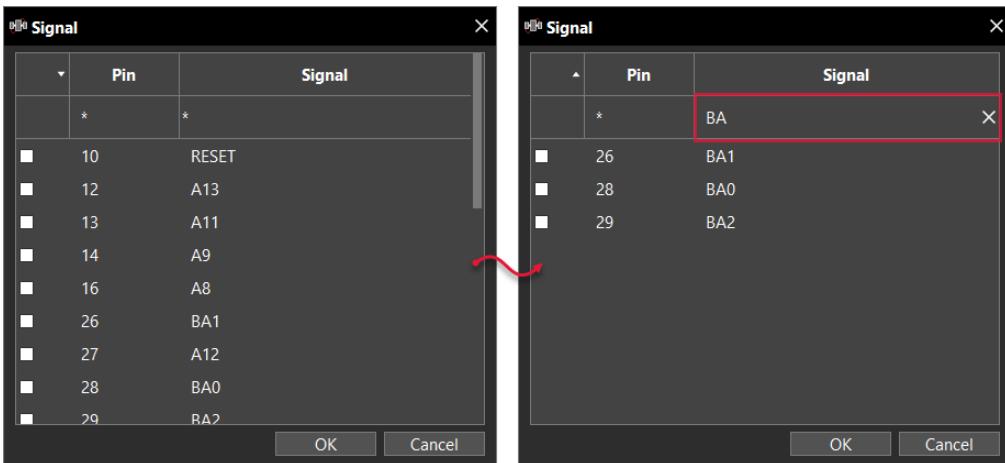
Getting Started with Parallel Bus Analysis

9. Click the cell under the *Edge Type* column and select *RiseEdge* instead of *BothEdges* from the list. This is required in case of this topology because the *Edge Type* of all *AddCmd* bus groups should be the same.

Bus Type	Bus Group	Timing Ref	Edge Type	Signal Names	Clock
*	*	*	*	*	*
AddCmd	Address	CLK0P / CLK0...	RiseEdge	A0, A1, A2, A3, A4, A5, A6, A7	
Data	DataL	LDQS / LDQS#	BothEdges	DQ0, DQ1, DQ2, DQ3, DQ4, ...	
Data	DataU	UDQS / UDQS#	BothEdges	DQ8, DQ9, DQ10, DQ11, DQ1...	
AddCmd	Calibration	CLK1P / CLK1N	RiseEdge		
			BothEdges		
			RiseEdge		
			FallEdge		

Note: For a *AddCmd* bus group, the *Edge Type* should be *RiseEdge* or *FallEdge*.

10. Click the *E* button displayed when you select the cell under the *Signal Names* column. The *Signal* dialog box opens.

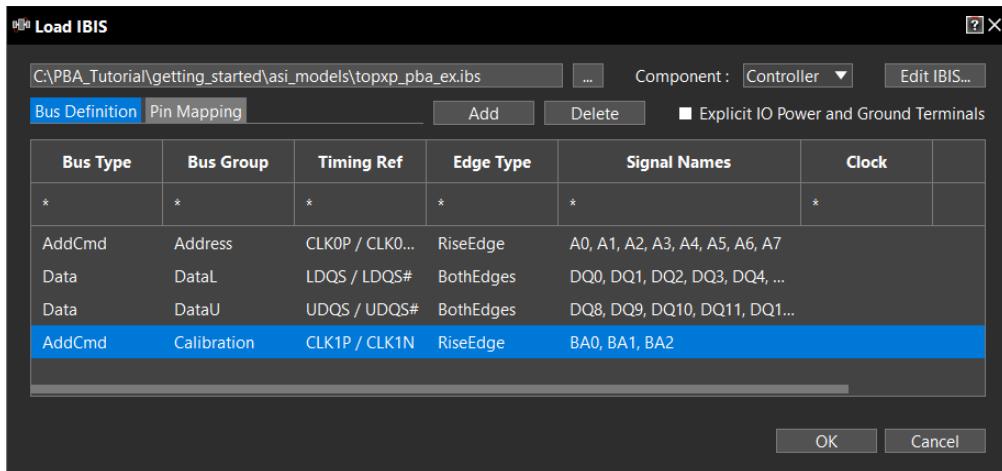


11. Type *BA* in the cell below the *Signal* column. This filters the signals that have name starting with *BA*. For example, sample `topxp_pba_ex.ibs` contains the following three signals: *BA0*, *BA1*, and *BA2*.
12. Select the check box adjacent to *BA0*, *BA1*, and *BA2*.

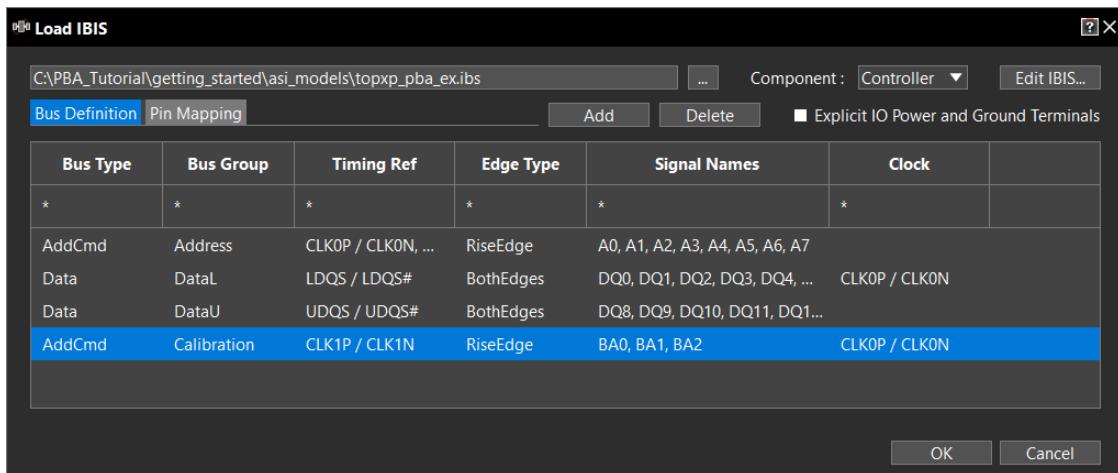
Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

13. Click *OK*. The *Signal* dialog box closes and the *Signal Names* column in the *Load IBIS* dialog box gets updated to show the selected signals.



14. Define *CLK0P / CLK0N* as the clock for the new *Calibration* bus group. The process is the same as you did for *Timing Ref* and *Signal Names*.
15. Define *CLK0P / CLK0N* as the clock for the existing *DataL* bus group too.

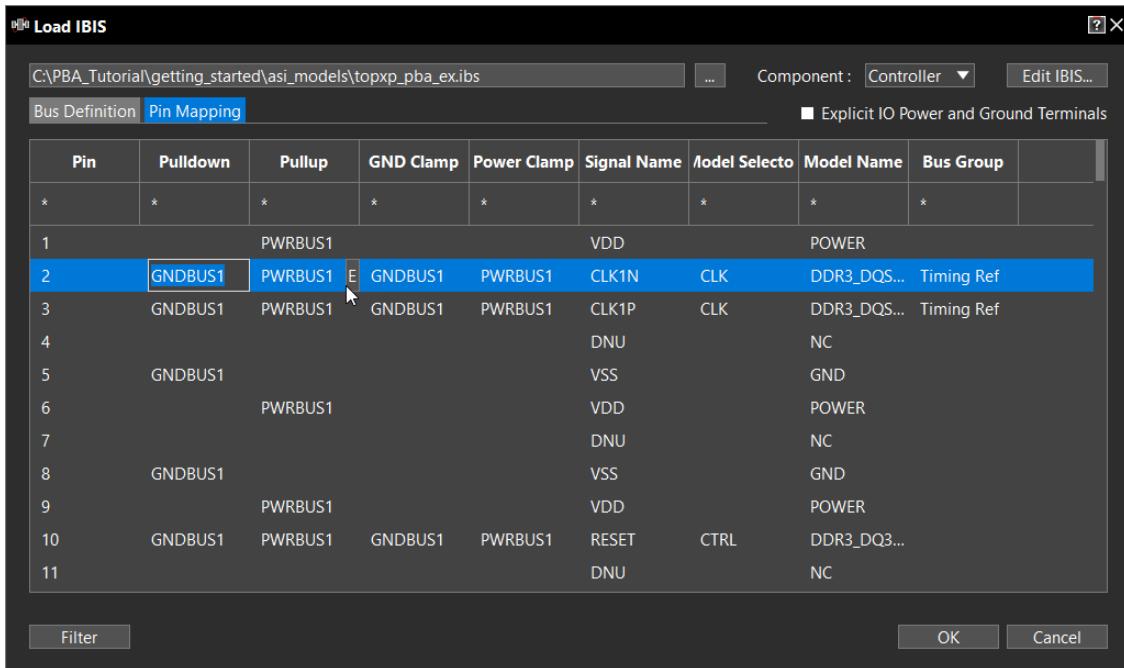


16. Click the *Pin Mapping* tab to review its contents. This tab, which is equivalent to the *[Pin Mapping]* keyword in an IBIS file, lets you edit the pin names defined in the

Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

Pulldown, Pullup, GND Clamp, and Power Clamp columns. For this tutorial, do not make any changes.



17. Click *OK* to accept the changes you incorporated in the *Bus Definition* tab.

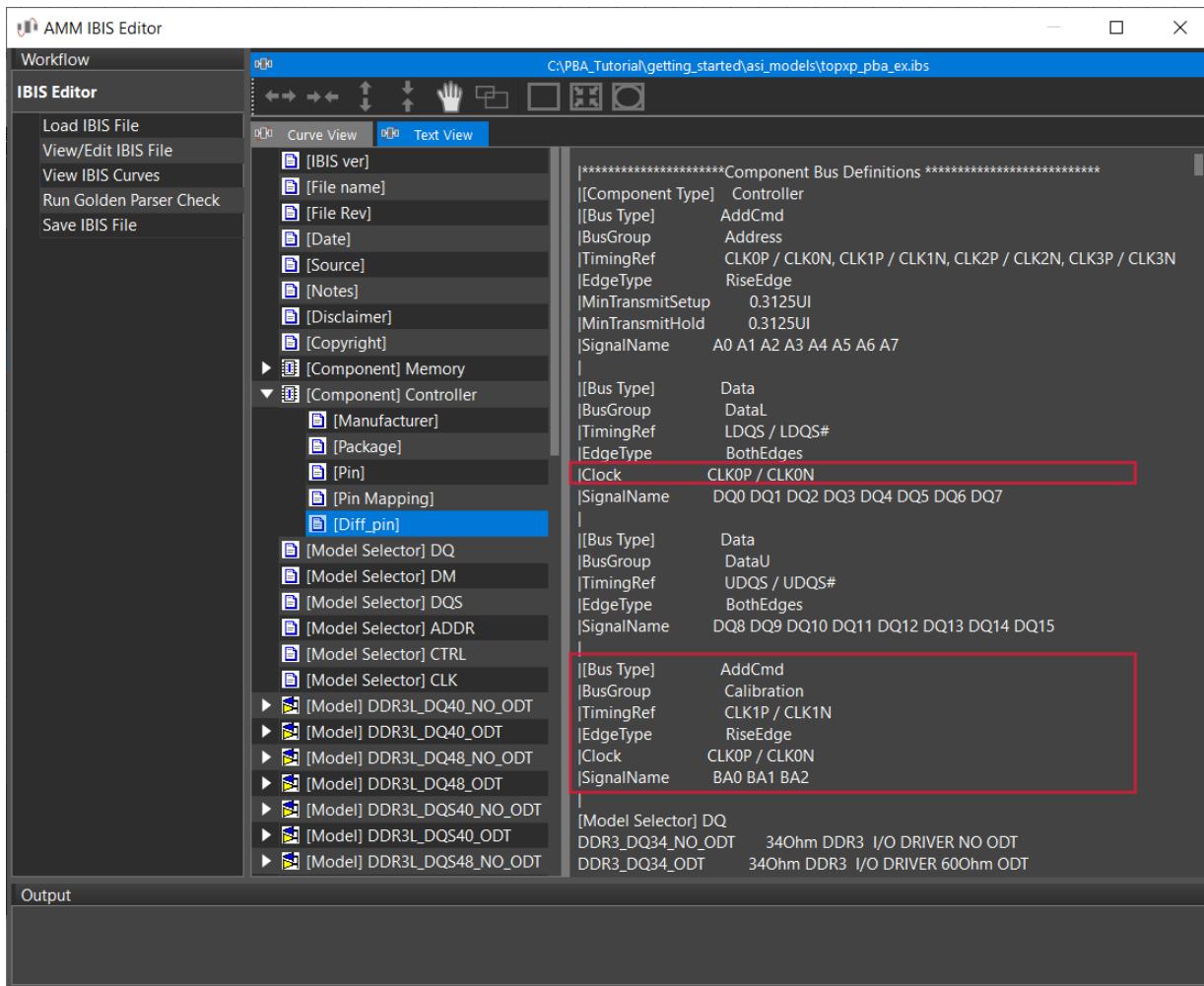
Verify the IBIS File Updates

1. Click *Load IBIS* in the *Edit Properties* panel. The *Load IBIS* dialog box opens.
2. Click *Edit IBIS*. The *AMM IBIS Editor* window opens.

Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

3. Search for the *Component Bus Definition* section related to the *Controller* block. The clock added to the *DataL* bus group and the new bus group, *Calibration*, can be seen as illustrated below.



Note: The IBIS model for the *Memory* block has similar elements. As the IBIS model editing functionality is identical to that for the *Controller* block, details for the *Memory* block are not reviewed in this tutorial. You are encouraged to explore the editing of IBIS model for the *Memory* block using the steps given above for the *Controller* block.

Topology Workbench: Parallel Bus Analysis Tutorial

Getting Started with Parallel Bus Analysis

Creating a Blank Topology and Assigning Device Models

Topology Workbench provides an intuitive block-based approach for capturing system designs as a block diagrams. You can base the designs on pre-defined templates shipped with the tool, or you can create your own designs on a blank topology. The [Getting Started with Parallel Bus Analysis](#) topic covered information about how to create a topology using a template provided in the installation hierarchy. In this chapter, lets create a new design from scratch and then assign device models to the blocks.

Chapters from 3 to 6 go through a sequential bus system design session from block-based setup to simulation and data processing. It focuses on an actual DDR3 design having a Controller, Memory device, PCB and VRM. You can go through each chapter sequentially to get a comprehensive understanding of the Topology Workbench – Parallel Bus Analysis workflow, or you can choose to go through selected chapters as needed.

The design files for each chapter are saved in the `PBA_Tutorial` directory that is available at the following path:

```
<INSTALL_DIR>\share\topxp\Tutorials\PBA_Tutorial
```

You can choose to perform each step explained in the chapter or open the specific files to review the resultant files.

Create a New Blank Topology

1. Start Topology Workbench in standalone mode.

In Windows, use one the following ways:

- Start — Run*, and type `TopWb`
-or-
- Start — Programs — Cadence PCB <release_number> — Sigrity Topology Explorer*
-or-

In UNIX, type `TopWb` in a Shell window.

2. Select *Advanced SI* from the *Cadence Product Choices* dialog box that is displayed. This product choice lets you focus on analyzing advanced source-synchronous parallel buses (for example, DDR).

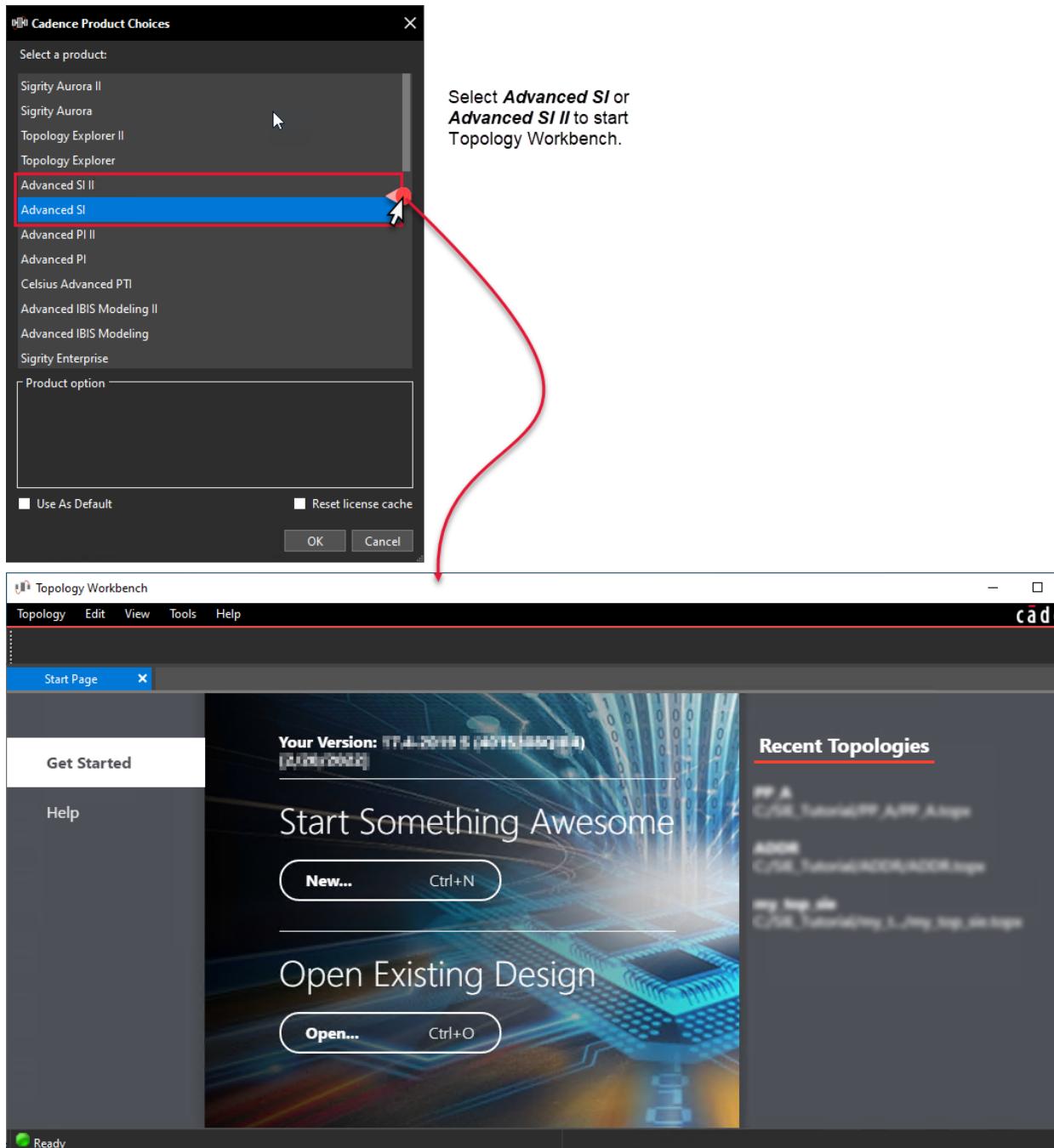


Tip
You can alternatively select *Advanced IBIS Modeling* if you want to develop I/O Buffer Information Specification (IBIS) models, including Algorithmic Modeling Interface (AMI) functionality for equalization.

Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

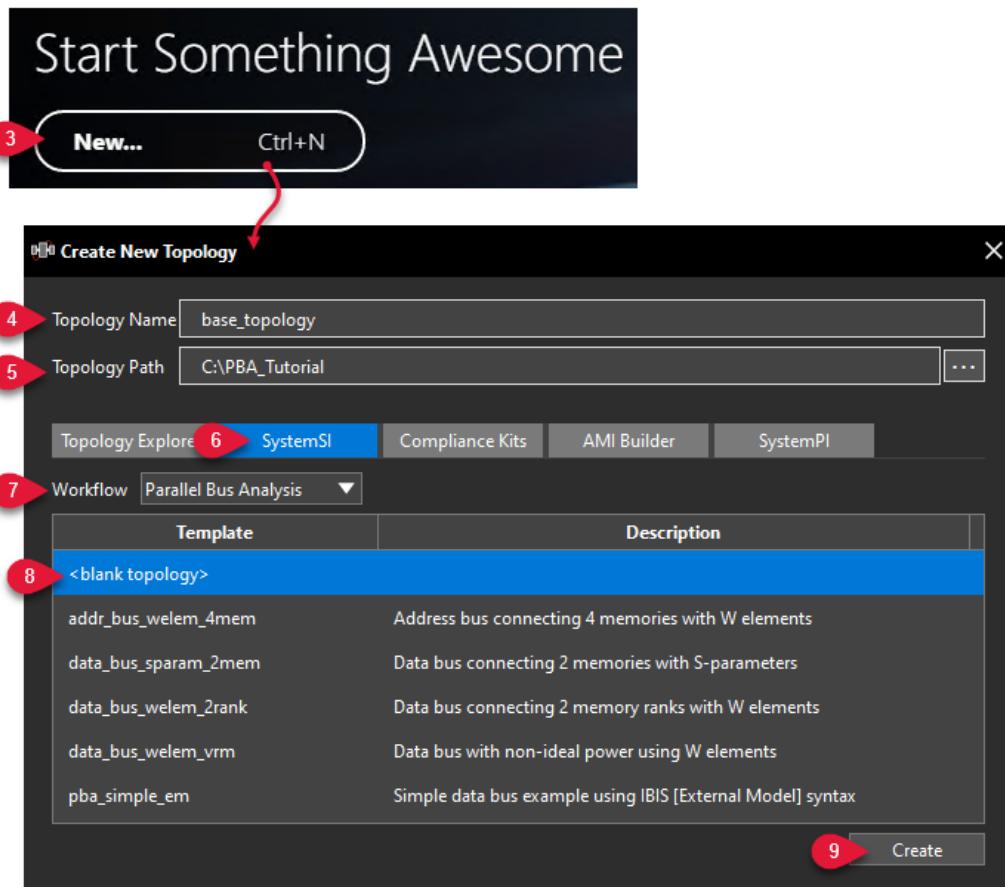
The Topology Workbench window opens with the *Start Page* tab in focus as shown below.



Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

3. Click *New...* from the *Start Something Awesome* section on the *Start Page* tab. The *Create New Topology* dialog box is displayed, as shown below.



4. Click the *SystemSI* module (tab).
5. Click the *Parallel Bus Analysis* from the *Workflow* list box. The table in this tab shows a list of default templates associated with the PBA workflow.
6. Select *<blank topology>*.
7. Type *base_topology* in the *Topology Name* box.

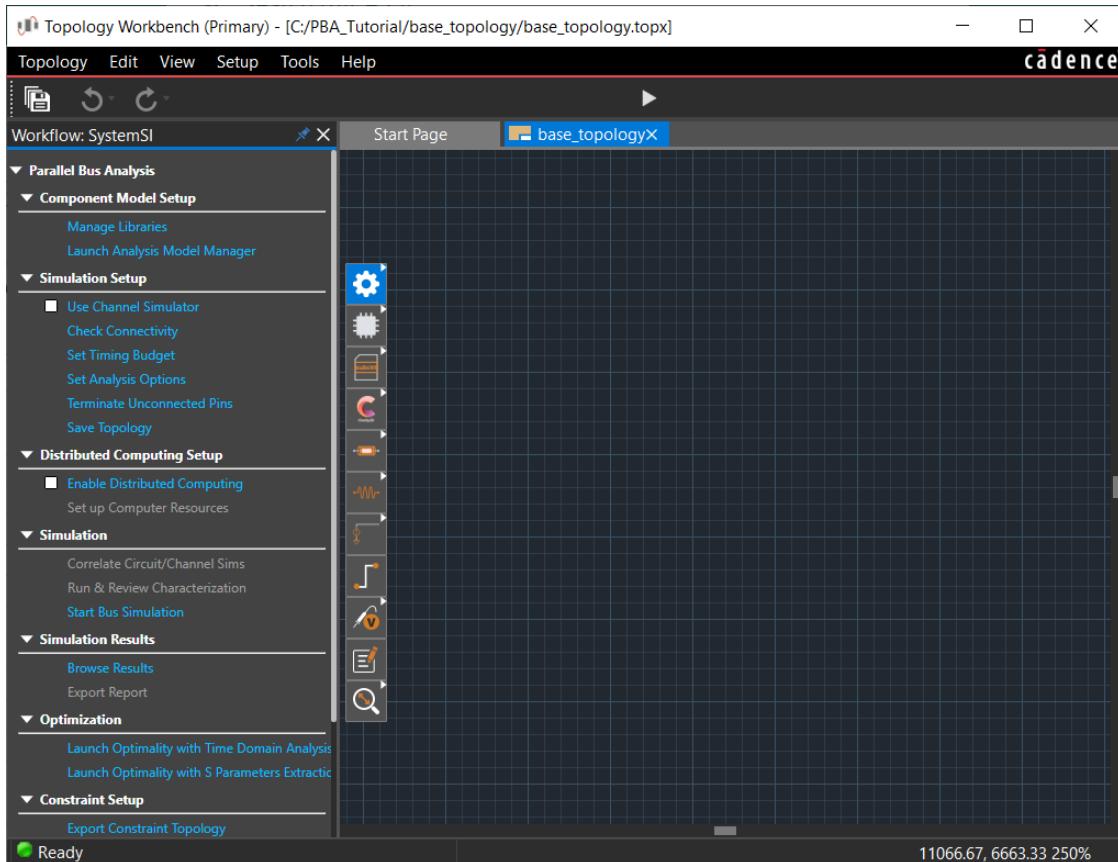
Note: A topology's name can contain only lowercase alphanumeric characters and underscores. If a topology with the same name exists already, a message is displayed to confirm if you want to overwrite it.

8. Browse and set the *Topology Path* to the directory where the new topology and related files should be saved on the hard drive. For example, we have browsed and selected the *PBA_Tutorial* directory, which we had created before starting this tutorial.

Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

9. Click *Create*. A tab named *base_topology* with blank canvas opens in the Topology Workbench window.



A subdirectory with the given topology name, *base_topology*, is created at the *Topology Path* you browsed to in [step 8](#). This directory contains the project file (*base_topology.topx*), all the models associated with the various blocks, and directories to hold the history and simulation results.

This PC > PC-ADHARDESH (C:) > PBA_Tutorial > base_topology >				
Name	Date modified	Type	Size	
asi_models	8/23/2023 11:21 AM	File folder		
history	8/23/2023 11:21 AM	File folder		
result	8/23/2023 11:21 AM	File folder		
base_topology.topx	8/23/2023 11:21 AM	TOPX File	7 KB	
base_topology.topx.lock	8/23/2023 11:21 AM	LOCK File	1 KB	
max_valid_electric_grid.txt	8/23/2023 11:21 AM	TXT File	1 KB	
topxp.log	8/23/2023 11:21 AM	Text Document	1 KB	

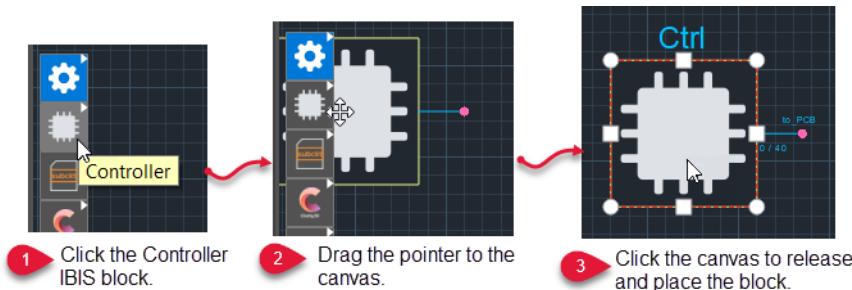
Add Blocks to the Blank Topology

Let us add the following types of blocks to the blank canvas of *base_topology*:

- A *CTRL IBIS* block (Controller)
- A *Mem IBIS* block (Memory)
- A *Layout* block (PCB)
- A *VRM* block (VRM)

To add these block to the canvas:

1. Click the controller block in the floating toolbar. This selects and attaches the block to the pointer.



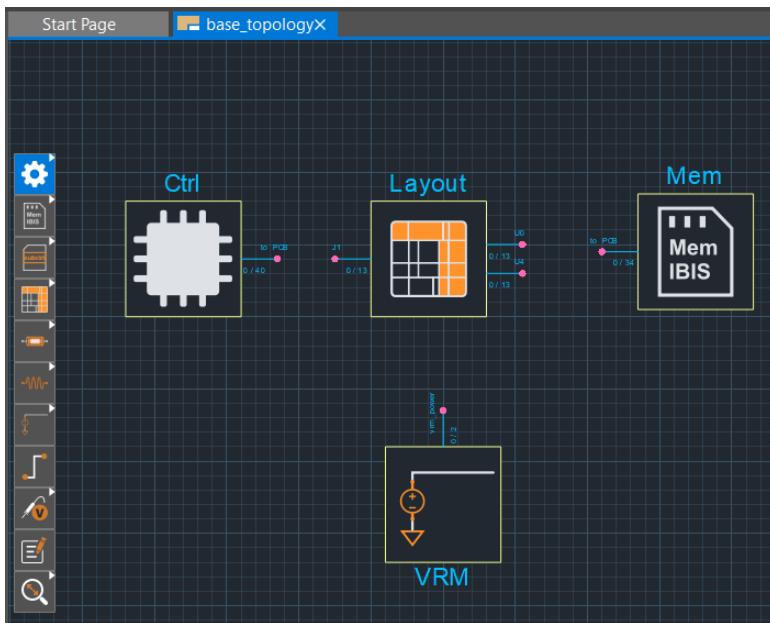
Note: If the controller block is not visible in the floating toolbar, right-click the first block under the *Settings* option to view the other available types of blocks.

2. Drag the pointer to the canvas location where the controller block needs to be placed.
3. Click the canvas to release and place the controller block. The block is assigned default name, *Ctrl*, which you can change in the *Edit Properties* panel.

Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

4. Repeat steps 1 to 3 to place a block each of the following types: *Mem IBIS*, *Layout*, and *VRM* block. The canvas looks as illustrated in the following image:



Assign Device Models

When you place a *CTRL IBIS* or a *Mem IBIS* block on the canvas, Topology Workbench automatically assigns to it a default IBIS model. Similarly, a *CTRL SPICE* or a *Mem SPICE* block is assigned a default SPICE compatible circuit model. However, Topology Workbench also lets you assign your own device model files to both the types of controller and memory blocks.

As we placed a *CTRL IBIS* and a *Mem IBIS* block on the blank canvas of *base_topology*, this section demonstrates the procedure for assigning IBIS models to these blocks.

Before you start with the steps explained below:

Copy	From	To
topxp_pba_ex.ibs	<INSTALL_DIR>\share\topxp\default_models	<WORK_DIR>\PBA_Tutorial\base_topology\asi_models

Assign IBIS Model to the Controller

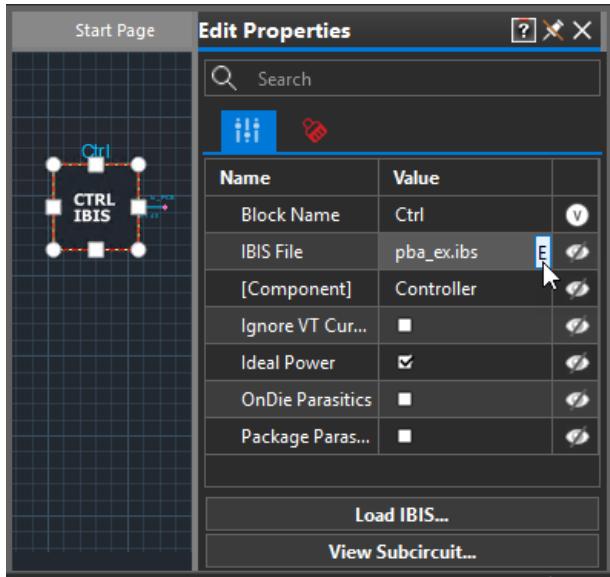
Lets see the steps to be followed for assigning a controller IBIS model file to the *Ctrl* block.

Topology Workbench: Parallel Bus Analysis Tutorial

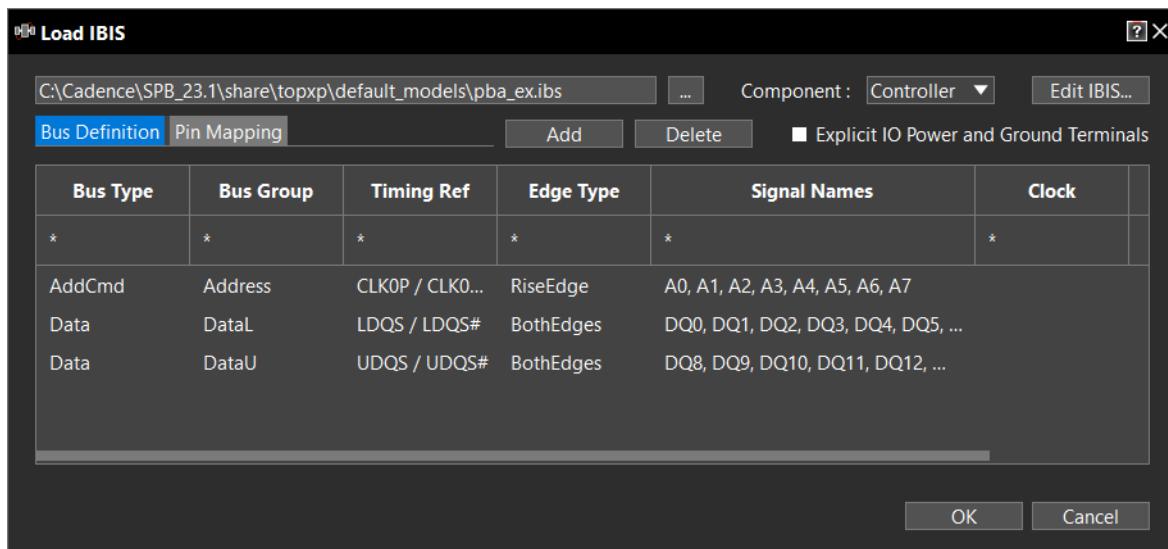
Creating a Blank Topology and Assigning Device Models

Loading IBIS File

1. Double-click the *Ctrl* (controller) block to open the *Edit Properties* panel.
2. Click the *E* button in the cell adjacent to *IBIS File*.



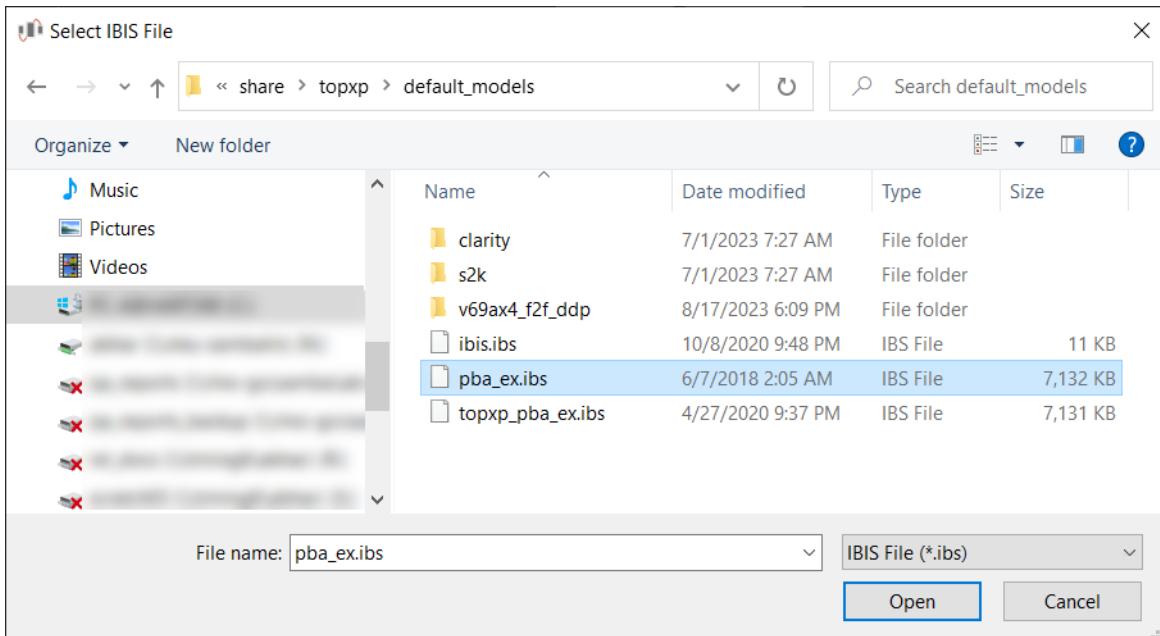
Alternatively, click *Load IBIS*. The *Load IBIS* dialog box opens.



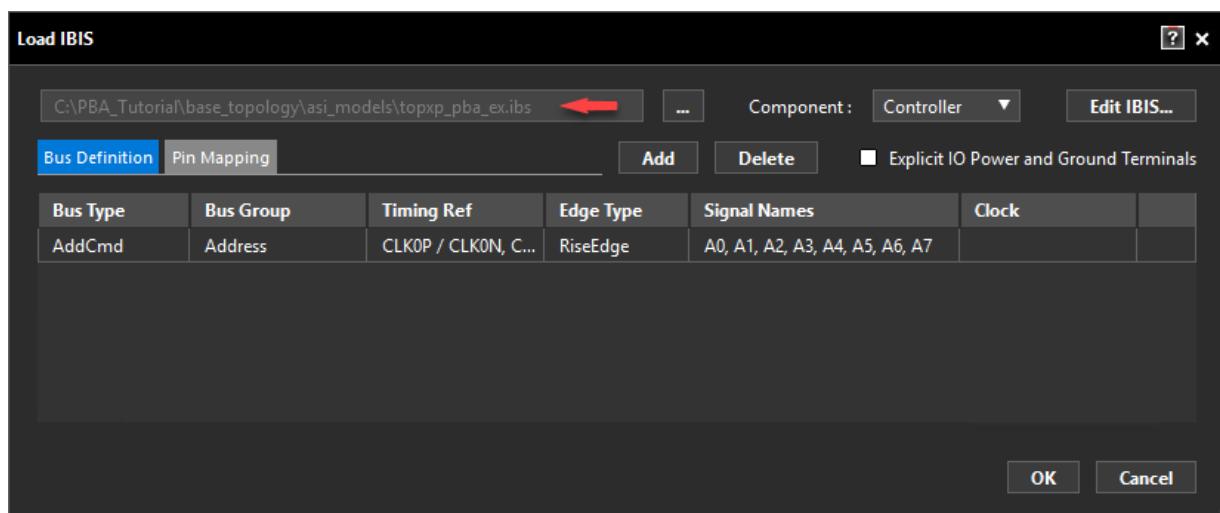
Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

3. Click the browse (...) button adjacent to the box that contains the path to the currently selected default IBIS model file. The *Select IBIS File* dialog box opens.



4. Browse to `<WORK_DIR>\PBA_Tutorial\base_topology\asi_models` and select `topxp_pba_ex.ibs`.
5. Click *Open*. The *Load IBIS* dialog box shows the updated path to the IBIS file you selected above. The content of the *Bus Definition* and *Pin Mapping* tabs are refreshed as per the selected sample IBIS model file.



Topology Workbench: Parallel Bus Analysis Tutorial

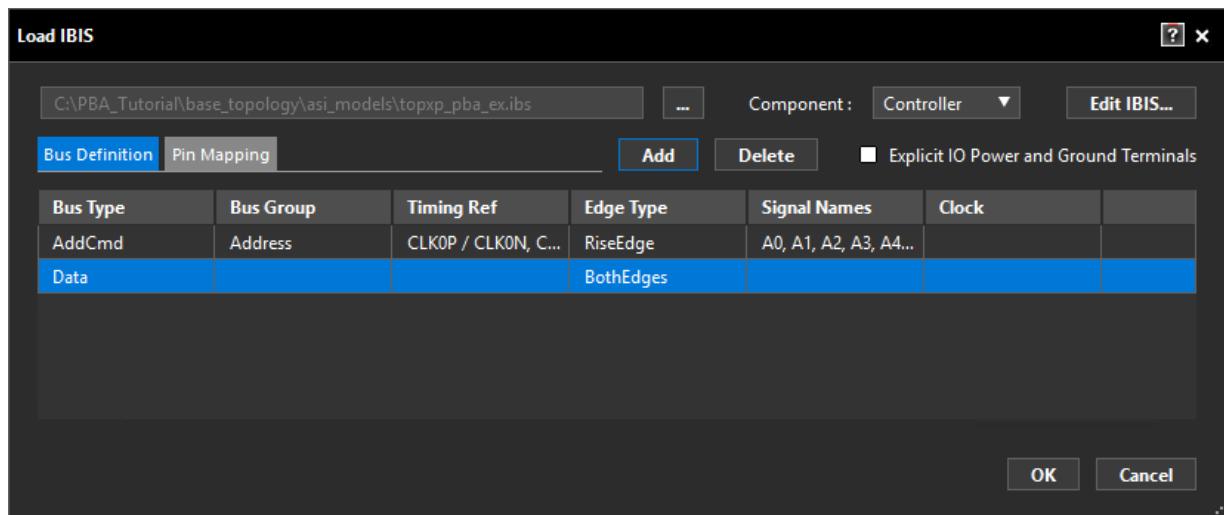
Creating a Blank Topology and Assigning Device Models

For this example, the IBIS model has the *Pin Mapping* from the device manufacturer. However, because the *Bus Definition* is not yet complete, the *Pin Mapping* is not fully defined, with only one bus group is shown.

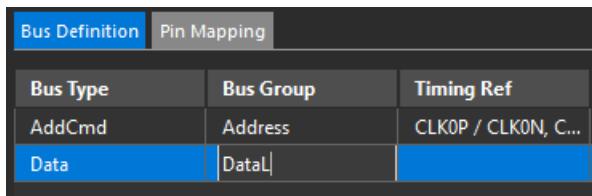
Adding Bus Definition

In this section, for the *Ctrl* block, lets define two data buses, *DataL* and *DataU*, consisting of DQ signals. In the *Bus Definition* tab of the *Load IBIS* dialog box, perform the following steps:

1. Click *Add* to create a new bus group.



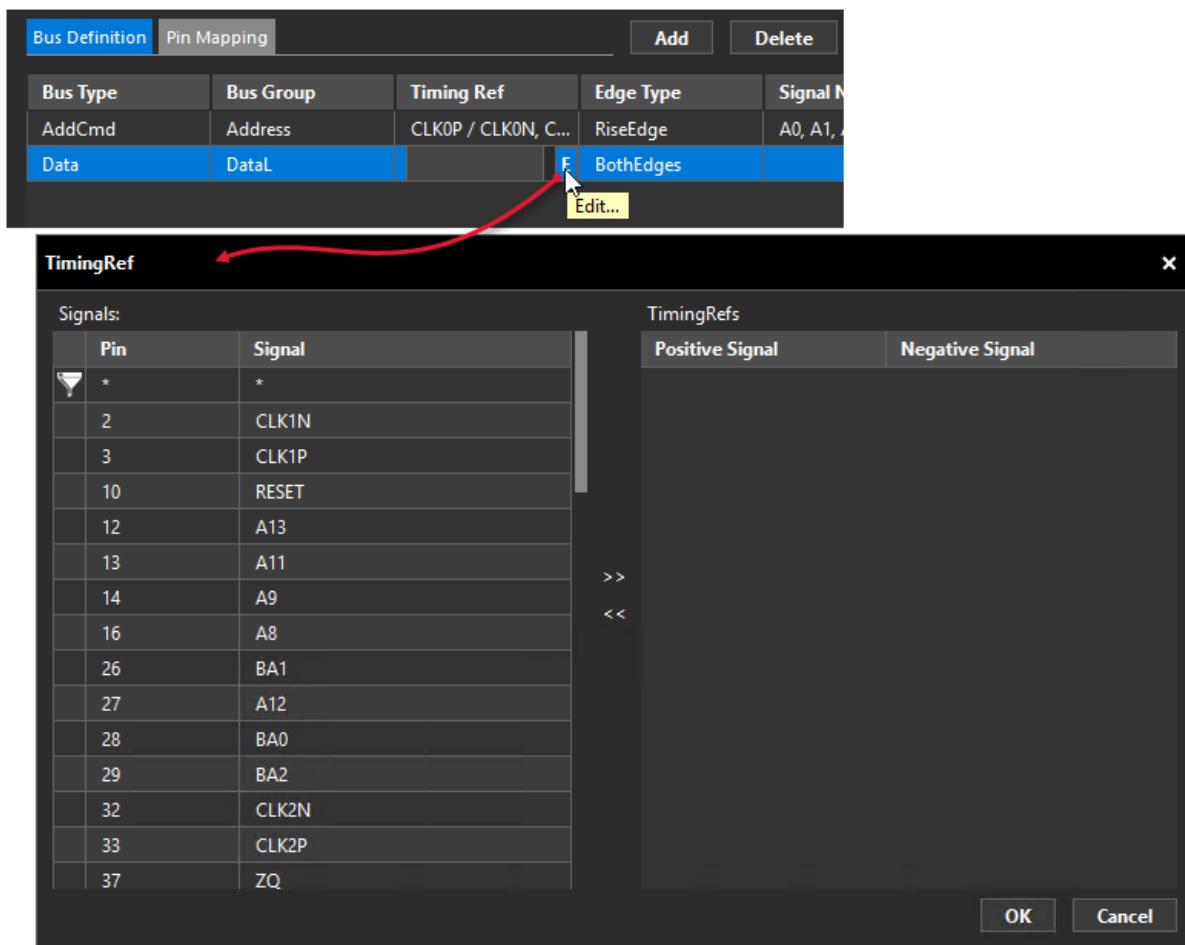
2. Click the *Bus Type* box. From the displayed list, you can select *Data*, *AddCmd*, or *Ctrl*.
3. Select *Data*.
4. Type *DataL* in the *Bus Group*.



Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

5. Click the *E* button in the *Timing Ref* box. The *TimingRef* dialog box is displayed, listing all the signals available in the IBIS file.

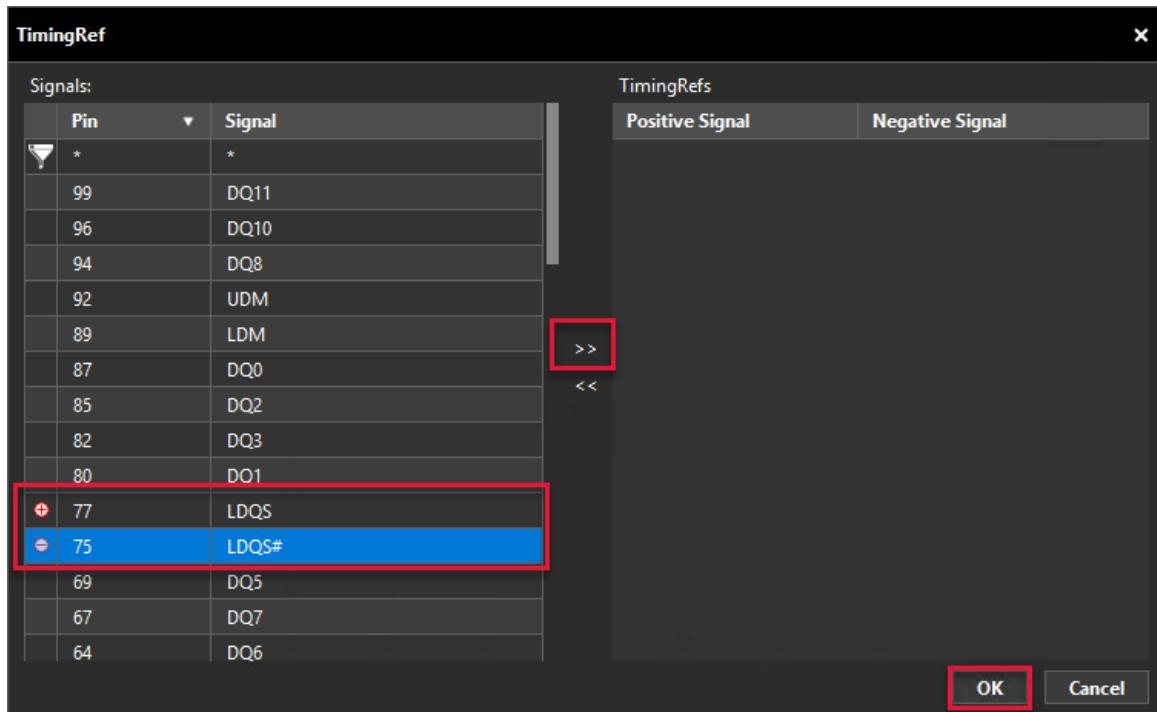


- Click the *Pin* column header to sort the signal names by pin numbers.
- Click pin 77 connected to the *LDSQ* signal.

Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

- c. Click pin 75 connected to the *LDSQ#* signal.

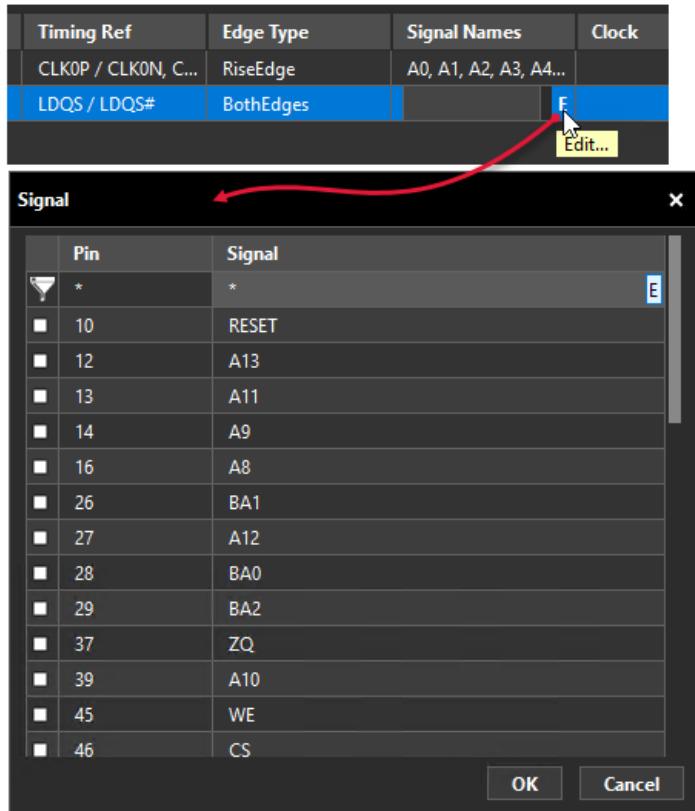


- d. Click the *>>* button to add the timing reference.
- e. Click *OK*.
6. Click the *Edge Type* box. From the displayed list, you can select *BothEdges*, *RiseEdge*, or *FallEdge*.

Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

7. Click the *E* button in the *Signal Names* box to define the signals that make up the bus. The *Signal* dialog box is displayed listing all the signals available in the IBIS file.

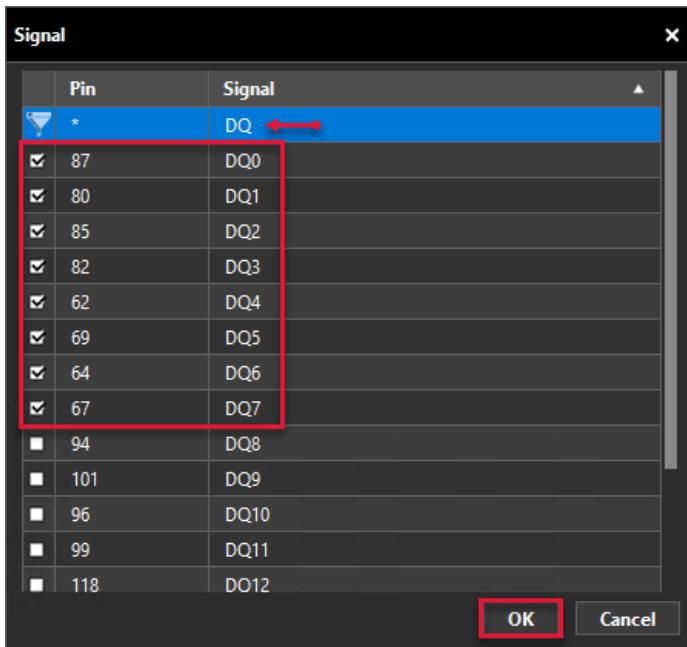


- Click the *Signal* column header to sort the signals in ascending order.
- Type *DQ* in the filter box below the *Signal* column header. This filters out the signals that have a name starting with *DQ*.

Topology Workbench: Parallel Bus Analysis Tutorial

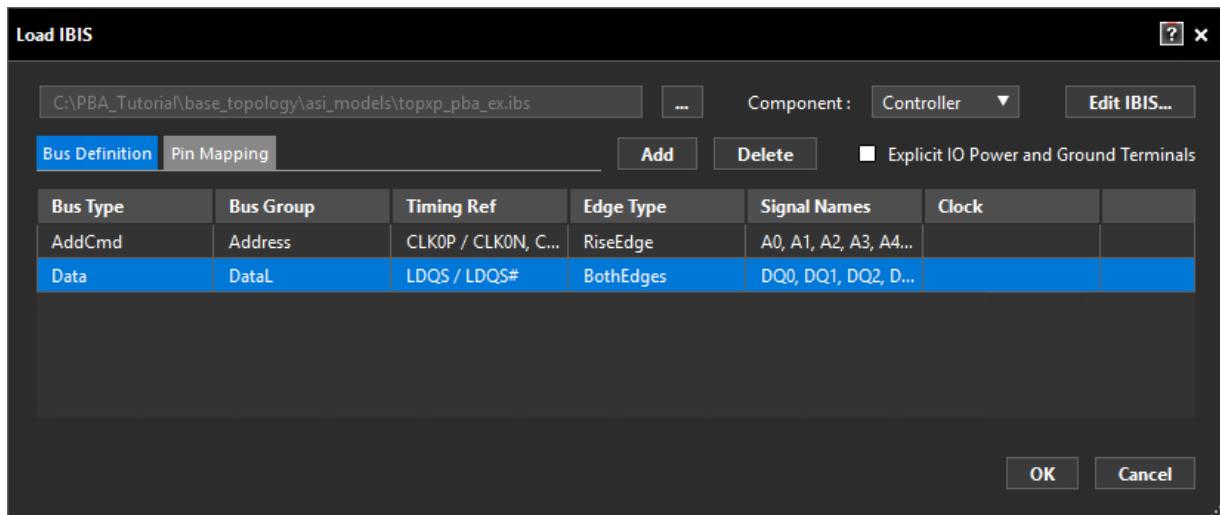
Creating a Blank Topology and Assigning Device Models

- c. Select the check boxes for eight signals starting from *DQ0* to *DQ7*.



- d. Click *OK*.

This completes the setup of the *DataL* bus as shown in the following image.



8. Repeat step 1 through step 6 above to create the second data bus with the following specifications:

- Bus Type: *Data*
- Bus Group: *DataU*

Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

- ❑ Edge Type: *BothEdges*
- ❑ Timing Ref Signals: *UDQS / UDQS#*
- ❑ Signal Names: *DQ8* through *DQ15*

Following figure shows the *Bus Definition* tab after you have successfully created the *DataU* bus group.

Bus Definition		Pin Mapping		Add	Delete	<input type="checkbox"/> Explicit IO Power and Ground Terminals
Bus Type	Bus Group	Timing Ref	Edge Type	Signal Names	Clock	
AddCmd	Address	CLK0P / CLK0N, C...	RiseEdge	A0, A1, A2, A3, A4...		
Data	DataL	LDQS / LDQS#	BothEdges	DQ0, DQ1, DQ2, D...		
Data	DataU	UDQS / UDQS#	BothEdges	DQ8, DQ9, DQ10, ...		



If required, you can specify the *Clock* signal for the data buses.

9. Click *OK* to close the *Load IBIS* dialog box.

The changes incorporated in the *Bus Definition* tab are saved to the IBIS model file. To verify, reopen the *Load IBIS* dialog box and click *Edit IBIS* to open the AMM *IBIS*

Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

Editor. Access the *Component Bus Definition* section and you can find the definitions of *DataL* and *DataU* added, as shown below:

```
77 75 0.350V 0ns NA NA
*****
*[Component Type] Controller
*[Bus Type] AddCmd
*[BusGroup] Address
*[TimingRef] CLK0P / CLK0N, CLK1P / CLK1N, CLK2P / CLK2N, CLK3P / CLK3N
*[EdgeType] RiseEdge
*[MinTransmitSetup] 0.3125UI
*[MinTransmitHold] 0.3125UI
*[SignalName] A0 A1 A2 A3 A4 A5 A6 A7

*[Bus Type] Data
*[BusGroup] DataL
*[TimingRef] LDQS / LDQS#
*[EdgeType] BothEdges
*[SignalName] DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7

*[Bus Type] DataU
*[BusGroup] DataU
*[TimingRef] UDQS / UDQS#
*[EdgeType] BothEdges
*[SignalName] DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15

[Model Selector] DQ
DDR3L_DQ40_NO_... 340Ohm DDR3 I/O DRIVER NO ODT
DDR3_DQ34_ODT 340Ohm DDR3 I/O DRIVER 600hm ODT
DDR3_DQ40_NO_ODT 400hm DDR3 I/O DRIVER NO ODT
```



In the PBA workflow, editing of the IBIS model file directly in the AMM IBIS Editor is not recommended.

Assigning an IBIS Model to Memory Block

The procedure for assigning IBIS models to memory devices is similar to that for the controller. In this exercise, the Memory component IBIS file has already been defined with correct pin mapping. The *Bus Definition* has not been created, and will be defined in this section of the tutorial.

Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

Adding a Bus to Memory IBIS Model

1. Double-click the *Mem* (memory) block to open the *Edit Properties* panel.
2. Click *Load IBIS* in the dialog box that opens.
3. Click the browse (...) button adjacent to the box that contains the path to the currently selected default IBIS model file. The *Select IBIS File* dialog box opens.
4. Browse to <WORK_DIR>\PBA_Tutorial\base_topology\asi_models and select the sample IBIS model file, topxp_pba_ex.ibs.
5. Click *Open*. The *Load IBIS* dialog box shows the updated path to the IBIS file you selected above. The content of the *Bus Definition* and *Pin Mapping* tabs are refreshed as per the selected sample IBIS model file.
6. Review the bus definitions available in the *Bus Definition* tab.

Two buses have been added to match the Controller's data buses that were defined in the previous section. The details of these buses are:

- ❑ First Bus:
 - Bus Group: *DataL*
 - Edge Type: *BothEdge*
 - Timing Ref Signals: *LDQS / LDQS#*
 - Signal Names: *DQ0* through *DQ7*
- ❑ Second Bus:
 - Bus Group: *DataU*
 - Edge Type: *BothEdges*
 - Timing Ref Signals: *UDQS / UDQS#*
 - Signal Names: *DQ8* through *DQ15*

The following image shows the *Bus Definition* tab for the memory block.

The screenshot shows the Topology Workbench interface with the 'Edit Properties' panel open for a 'Memory' component. The 'Bus Definition' tab is selected. The path 'C:\PBA_Tutorial\base_topology\asi_models\topxp_pba_ex.ibs' is shown in the top bar. The table lists three bus definitions:

Bus Type	Bus Group	Timing Ref	Edge Type	Signal Names	Clock	
AddCmd	AddCmd::CK/CK#	CK / CK#	RiseEdge	A0, A1, A2, A3, A4...		
Data	DataL	LDQS / LDQS#	BothEdges	DQ0, DQ1, DQ2, D...		
Data	DataU	UDQS / UDQS#	BothEdges	DQ8, DQ9, DQ10, ...		

Topology Workbench: Parallel Bus Analysis Tutorial

Creating a Blank Topology and Assigning Device Models

7. Click *OK* to save the definition and to close the *Load IBIS* dialog box.

Note: Bus and signal names for Controller and Memory are local to the IBIS file, and do not have to match each other, nor do they have to match the names in other components, including the Controller. Pin names, however, are used to automate connectivity between components that have a physical connection. The signal/pin mapping is addressed in the block connections, which is covered in [Chapter 5, “Connecting the Blocks.”](#)

This completes the task of adding IBIS models to the Controller and Memory blocks. Now, let's move to the next step, that is, [Extracting and Generating an Interconnect Model](#) for the *subckt* block, which we will configure as the PCB block in our design.

Extracting and Generating an Interconnect Model

Interconnect components, including Printed Circuit Boards (PCBs) and packages, are defined in the SPICE netlist definitions. These can be circuit models including lumped elements and distributed transmission lines, W-element models, or S-parameter models in Touchstone or Sigrity BNP format. These models can be created within the Topology Workbench – Parallel Bus Analysis workflow using an integrated layout extraction utility that has the capability to use a variety of extraction engines. Sigrity PowerSI board and package modeling tool is seamlessly integrated with the Parallel Bus Analysis workflow to allow easy extraction of full boards and packages, including non-ideal power and ground nets.

This chapter details the procedure of assigning to the PCB block a circuit file that describes it. It also walks you through the process of extracting an S-parameter description of a board using Sigrity PowerSI, and see how the extracted model file is integrated with Parallel Bus Analysis.

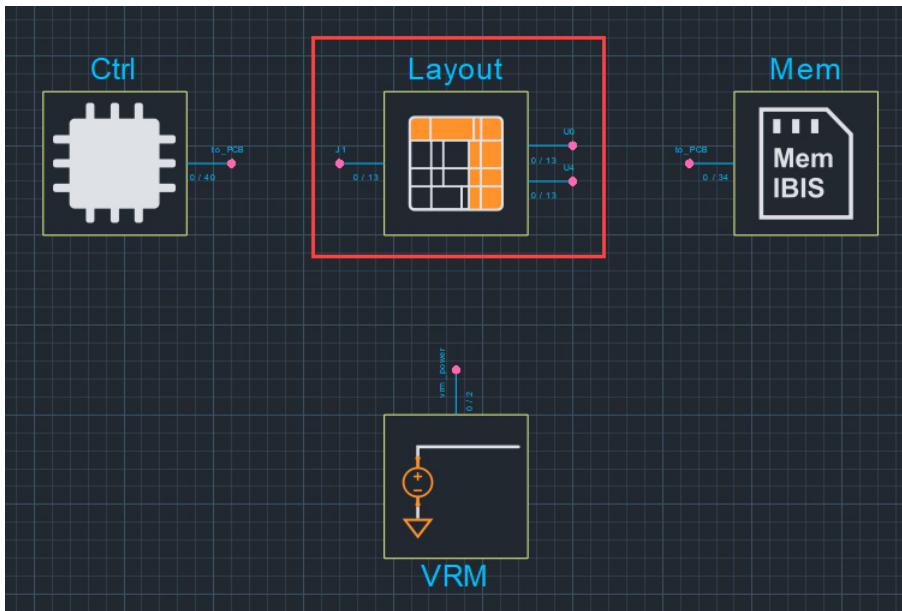
Tutorial Files

The design is the same one that was edited in [Chapter 3, “Creating a Blank Topology and Assigning Device Models.”](#) By now, the block diagram has models defined for the Controller

Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

and Memory blocks. In this chapter, you will extract and assign a model to the PCB block, that is, the *Layout* block.



If you have performed the tasks covered in the previous chapter, you can continue with the same design files. However, before you start with the steps explained in this chapter, copy the following file:

Copy	From	To
tutorial_PCB1.SPD	<INSTALL_DIR>\share\topxp\Tutorials\PBA_Tutorial	<WORK_DIR>\PBA_Tutorial\ba se_topology

If you are starting directly from this chapter, open the `interconnect_model.topx` file located at following path:

```
<INSTALL_DIR>\share\topxp\Tutorials\PBA_Tutorial\interconnect_model
```

This directory also contains the IBIS model file for the Controller and Memory.

For the interconnect model extraction, the `PBA_Tutorial` directory contains PCB file, `tutorial_PCB1.SPD`:

```
<INSTALL_DIR>\share\topxp\Tutorials\PBA_Tutorial
```

Generate a PCB Model

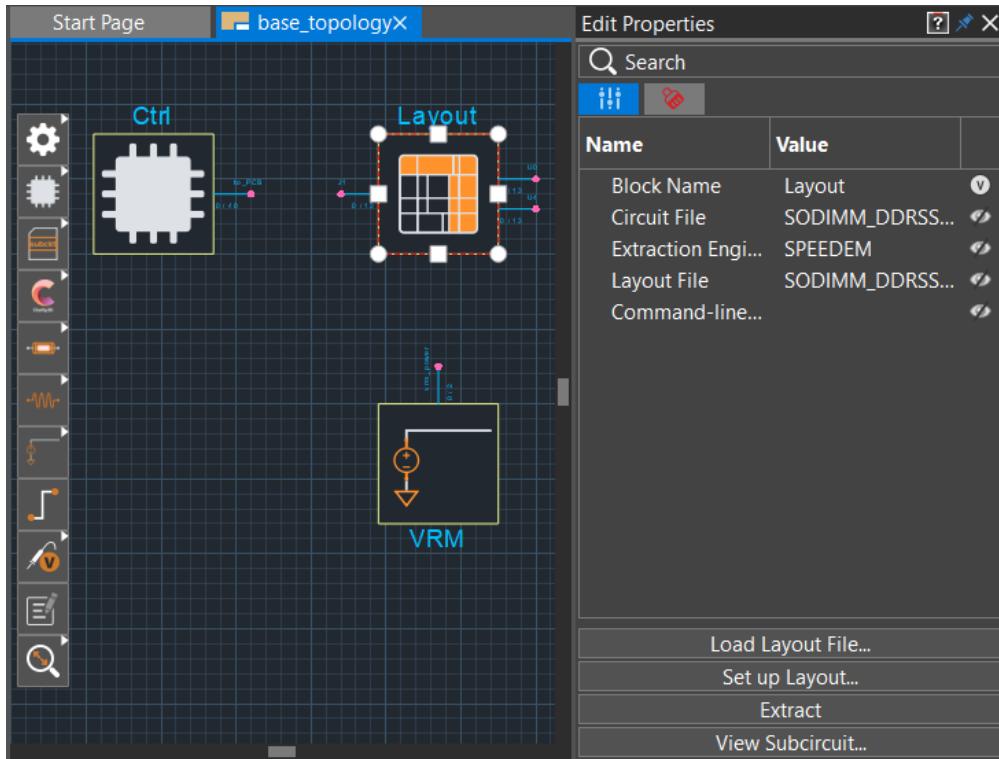
In this section, you will create a model for a DDR3 PCB bus using the Sigrity PowerSI simulator. The result of the PowerSI simulation is an S-parameter model, and a SPICE netlist that has the model connection information embedded. This netlist file is loaded and can be reviewed in the Topology Workbench – Parallel Bus Analysis workflow.

A simple package model, using different types of SPICE interconnects, will be called in the Parallel Bus Analysis workflow, and associated with the *subckt* block, which represents the PCB in our design.

Note: Sigrity PowerSI is a physical board and package simulator that uses Sigrity-patented solution technology to quickly and accurately model high-speed interconnects. Through this simulator, both signal integrity and power integrity effects are accurately modeled on the parallel bus topologies. For more information about Sigrity PowerSI and its working knowledge, refer to the [Cadence Online portal](#).

Edit the PCB Block

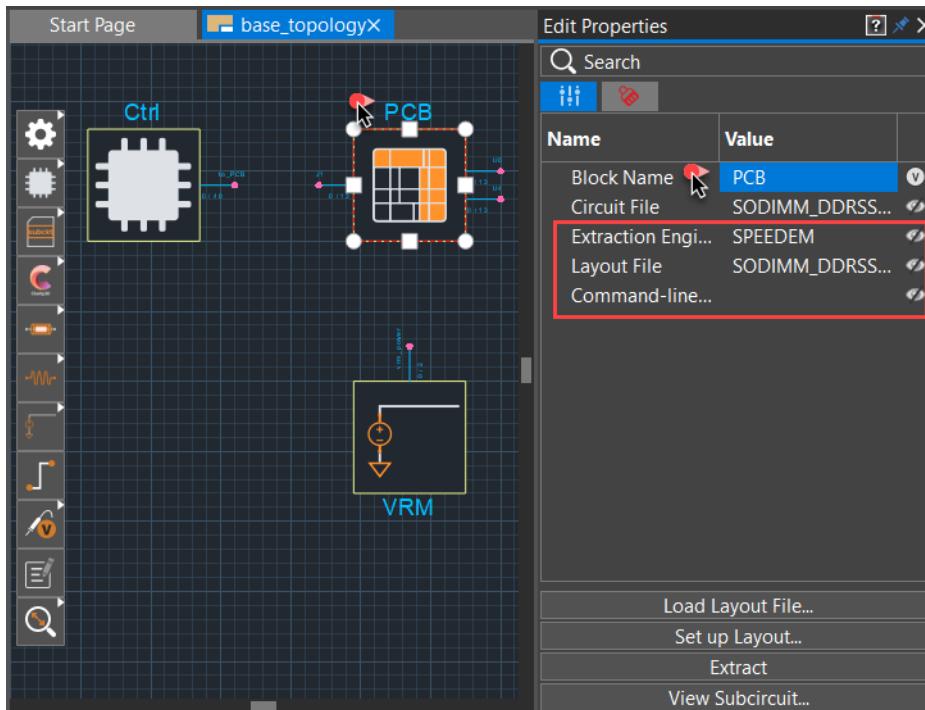
1. Double-click the *Layout* block to view its properties. The *Edit Properties* panel opens.



Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

2. Change the *Block Name* to *PCB*. Notice that the name of the *Layout* block is updated simultaneously from *New* to *PCB* on the canvas.



Now, proceed to setting up the *Extraction Engine*, providing the *Layout File Name*, and specifying the *Command-line Switches* as needed.

3. Select *PowerSI* from the *Extraction Engine* list to ensure that the PCB design will open in the Sigrity PowerSI modeling tool as we proceed further. By default, *SPEEDEM* is selected.

Important

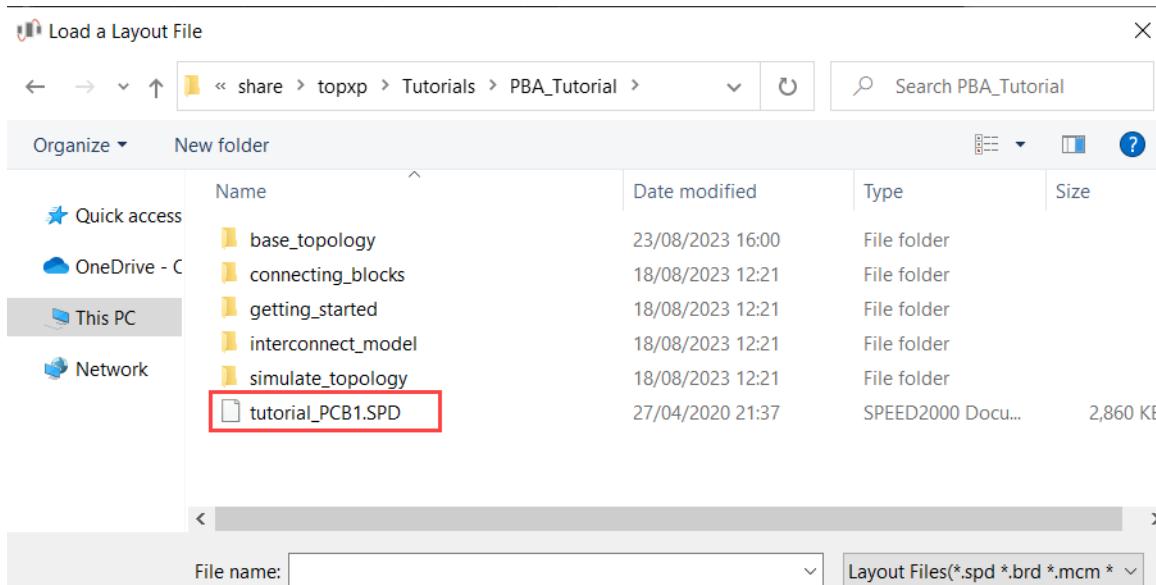
Topology Workbench checks out a PowerSI license for both *Set up Layout* and *Extract* unless you are using a license where both Topology Workbench and PowerSI are included, such as, the *Advanced SI* option from the *Cadence Product Choices* dialog box.

4. Click the browse (...) button next to the *Layout File* name.

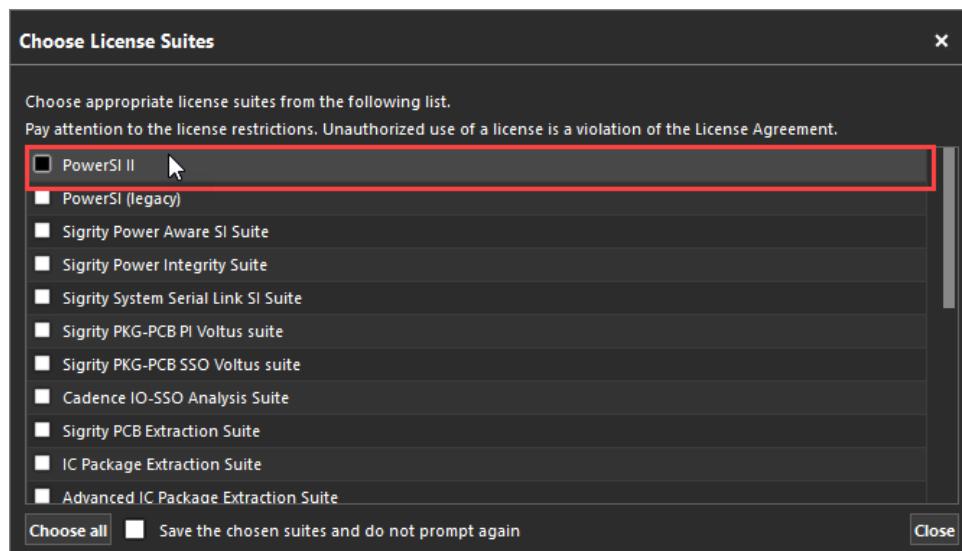
Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

5. Browse and select the `tutorial_PCB1.SPD` file in the displayed dialog box. This is the same file that was referred to at the beginning of the chapter.



6. Click *Set up Layout*. The *Choose License Suites* dialog box opens.

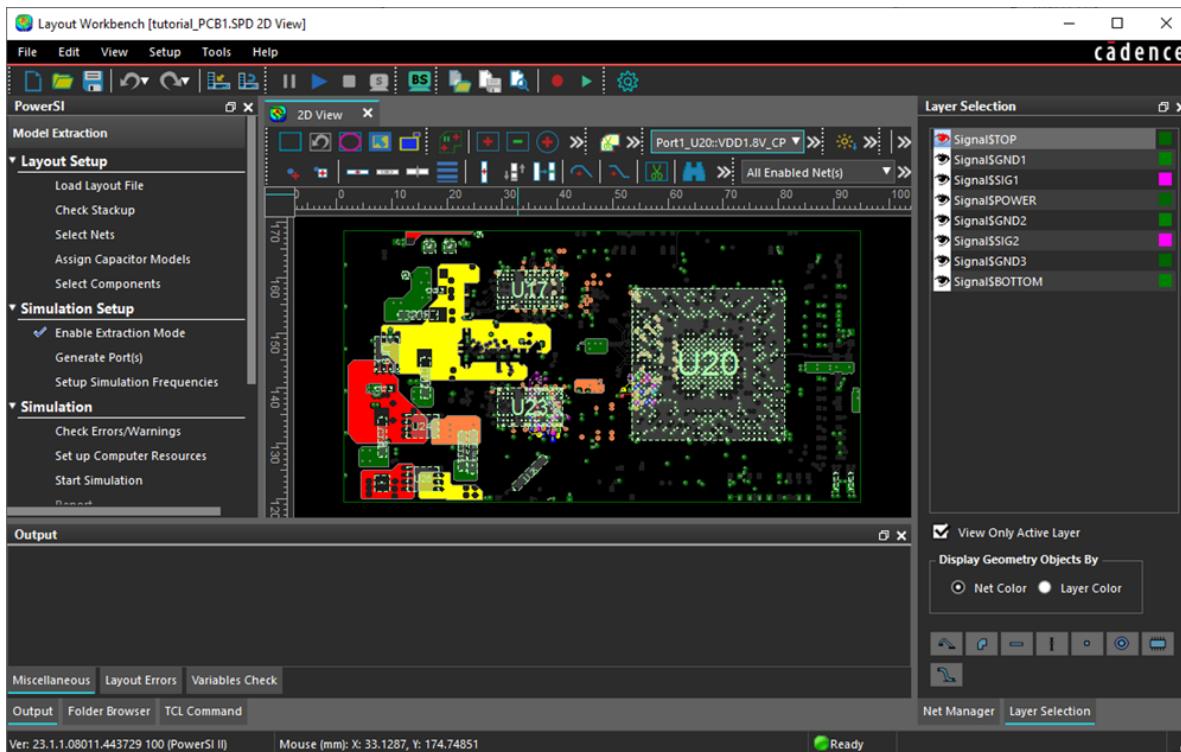


7. Select the *PowerSI II* check box.

Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

- Click *Close*. The *Sigrity Suite* window opens with 2D View of the Topology Workbench design in the PowerSI-based extraction workflow.



Note: Other tools can also be used for interconnect model extraction, but Sigrity PowerSI is the preferred modeling tool. In general, any tool that can create SPICE compatible interconnect models, including S-parameters, can theoretically be used. The critical model connection is automated when using PowerSI.

Extract the PowerSI Model

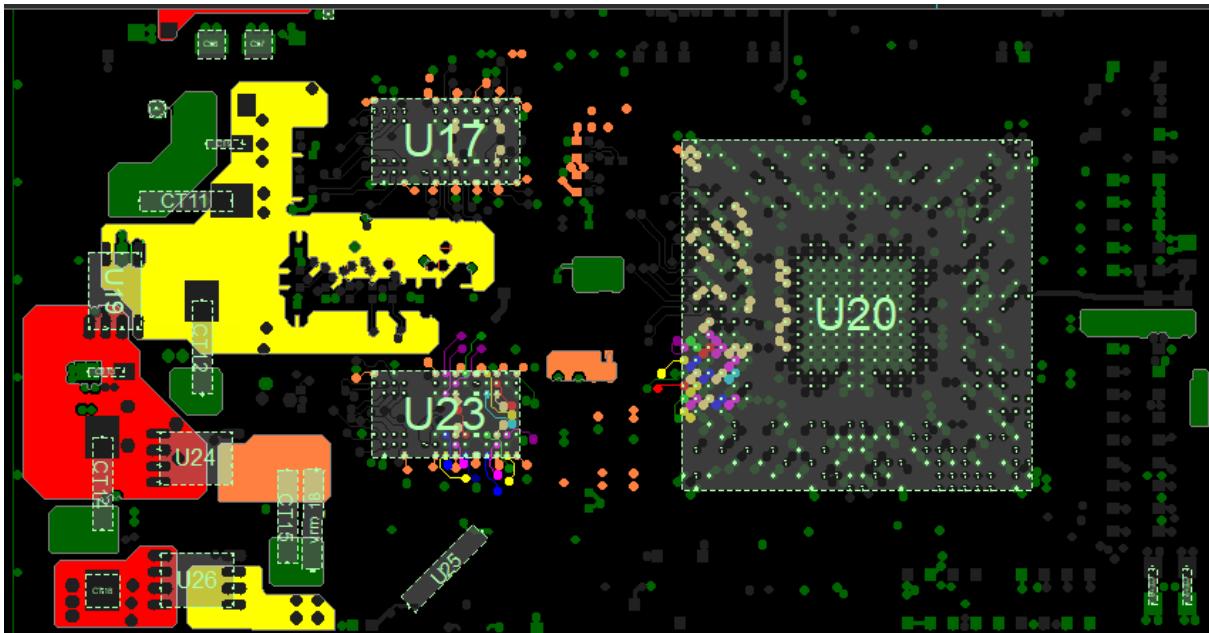
By the time you reach this section of the tutorial, you should have the PCB design file open in Sigrity PowerSI. As a detailed discussion of the PowerSI simulation is beyond the scope of this document, the `tutorial_PCB1.SPD` file has been edited and set up, and preliminary simulations have already been performed for you. This section covers some of the PowerSI setup options, but for detailed information, see the *Setting up the Ports in Extraction Mode* section of the *Preparing for Simulation* chapter in the *PowerSI User Guide*.

- In the PowerSI toolbar, click the *Select Components* () tool button to display the components in the PCB design.

Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

- Click the **Area** button () to zoom in a part of the window. Zoom in the middle part of the PCB, with the largest components, *U23* and *U20*.



The DDR3 bus on this board connects the memory controller, *U20*, with two DDR3 devices, *U17* and *U23*. For this tutorial, you will simulate only the Data Bus connecting *U20* and *U23*.

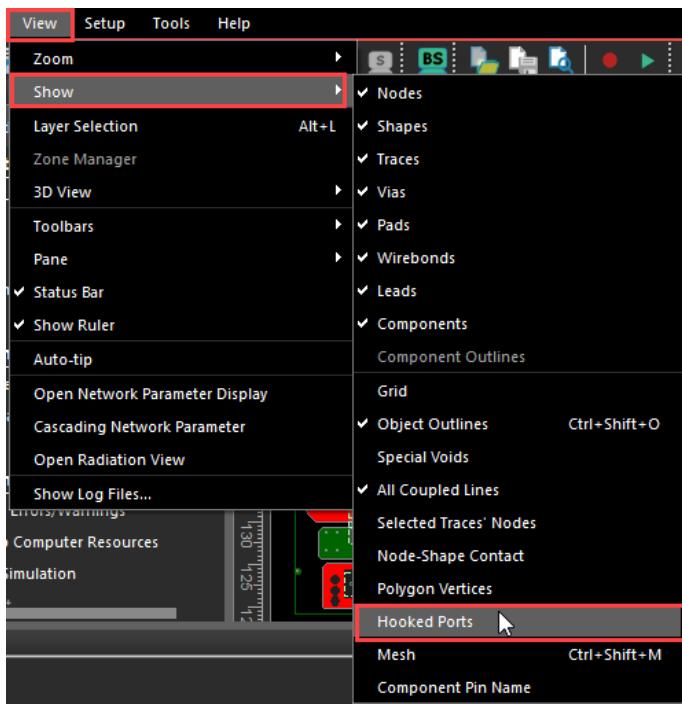
Note: Only circuit connections that are part of the buses to be simulated should be included in the extraction process. Additional circuit connections that are unterminated, at both Controller and Memory block levels, result in unconnected bus signals that cannot be resolved, which in turn results in an error at run time in the Topology Workbench – Parallel Bus Analysis workflow.

PowerSI extracts the S-parameter model of this bus over the specified frequency range.

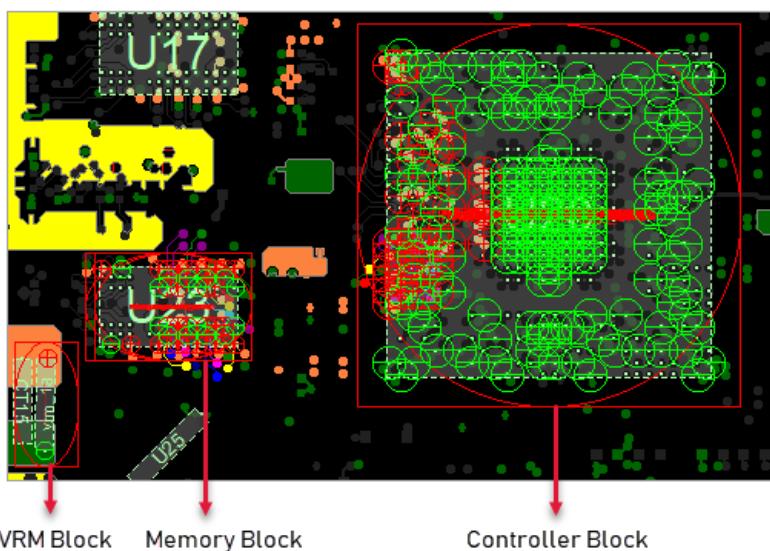
Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

3. Choose *View – Show – Hooked Ports* to see the port locations for the S-parameters. For information about hooked ports, refer to the *Hooking Port Pins to Nodes* section in the *Preparing for Simulation* chapter of the *PowerSI User Guide*.



The ports on each of the data lines including the strobe are shown on the controller (*U20* – right side) and DRAM (*U23* – middle) components. Positive port terminals are displayed as Red “+” symbols, and negative terminals are Green “-” symbols.



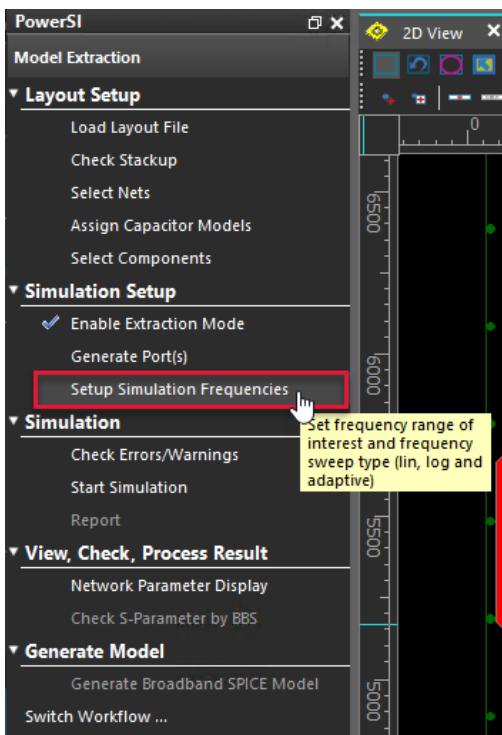
Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

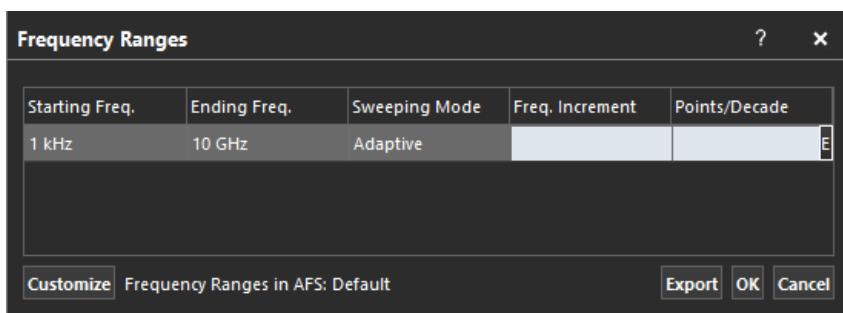
The port in the bottom left is where the 1.8 Volt DDR power supply for the PCB. This voltage regulator module (VRM) port is circled in Red.

There are total 39 ports defined on the PCB.

4. Click *Setup Simulation Frequencies* in the *Simulation Setup* schema of the *Workflow: PSI Extraction* pane. This lets you view the frequency range for the S-parameter simulation.



The simulation frequencies should be set as shown in the following figure, with a starting frequency of *1 KHz*, ending frequency of *10 GHz*, and frequency sweep mode set to *Adaptive*.



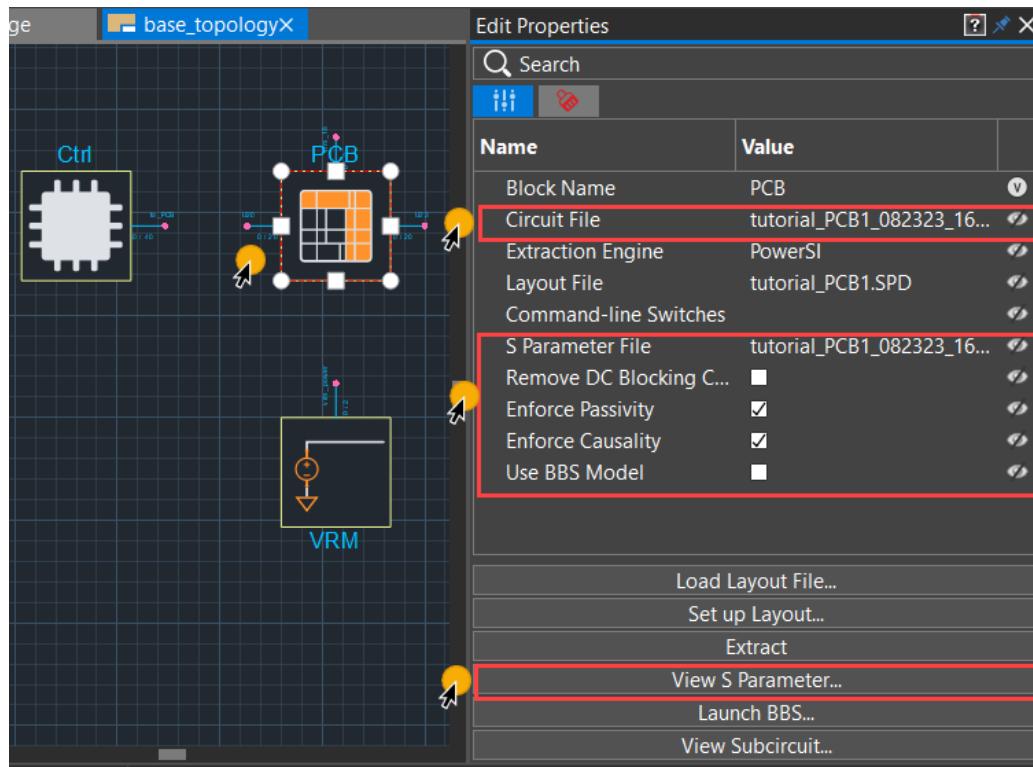
5. Click *OK* to close the *Frequency Ranges* dialog box.

Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

6. Select *File – Exit* to close the PowerSI window now that you have reviewed the components in the PCB design. Click *Yes* if a message prompts you to save. The Topology Workbench window continues to be displayed.
7. Click *Extract* in the *Edit Properties* panel. The model extraction process starts, and the progress can be seen in the status bar. After the completion of the process, the following two files are generated and corresponding information is shown in the *Edit Properties* panel:
 - ❑ A 39-port BNP (.bnp) file that has the S-parameter data in Sigrity compact binary format.
 - ❑ A circuit (.ckt) file with the SPICE netlist that calls this S-parameter data model, and has the connection syntax defined.

Note: These .bnp and .ckt files are generated and saved in the same location where the .spd file resides.



In addition, notice the following two updates:

- ❑ The *Edit Properties* panel shows the *View S Parameter* button that lets you view the simulation results.

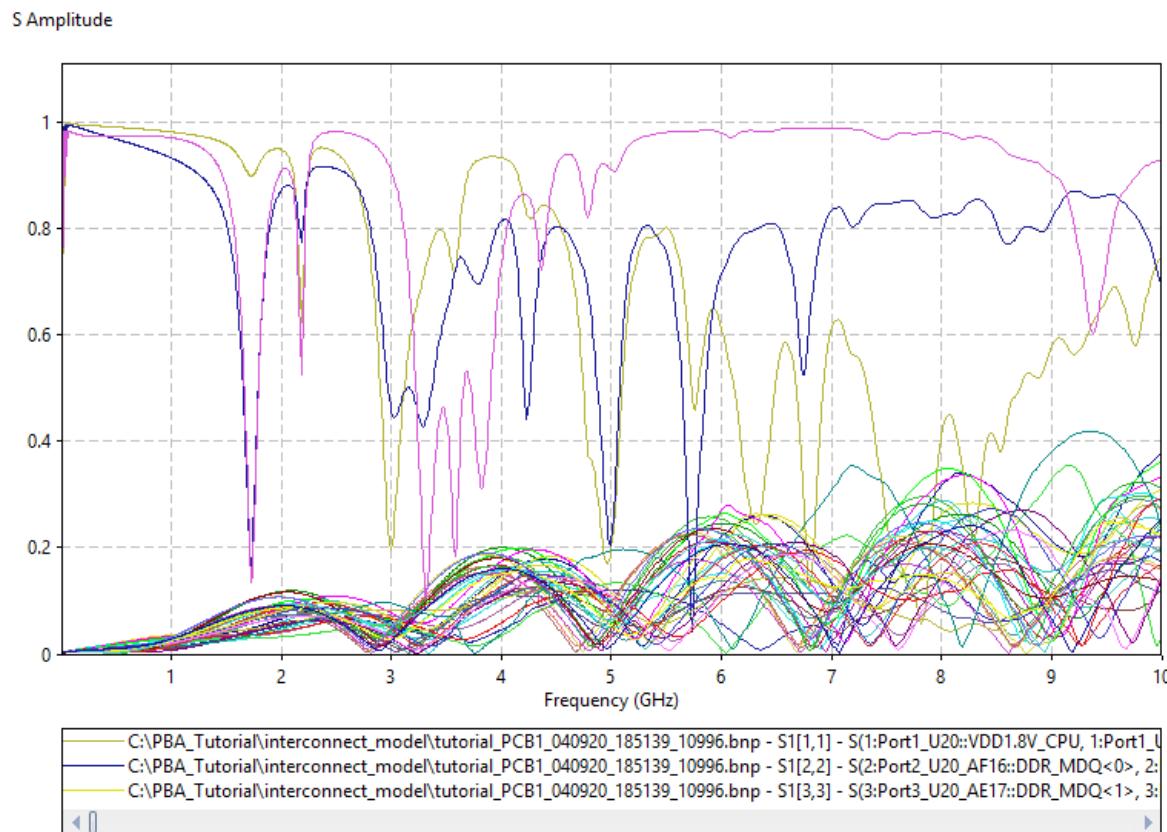
Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

- The PCB block gets updated on the canvas to show the following three connectivity ports instead of two, which were seen initially before the extraction process started: Ctrl to PCB, VRM to PCB, and Memory to PCB.

Note: In case you are not able to see the third pin, right-click on the canvas and select the *Display Unconnected Power Pins* option from the short-cut menu.

- Click *View S Parameter* in the *Edit Properties* panel. The simulation results open in the SSI Viewer window as shown below:

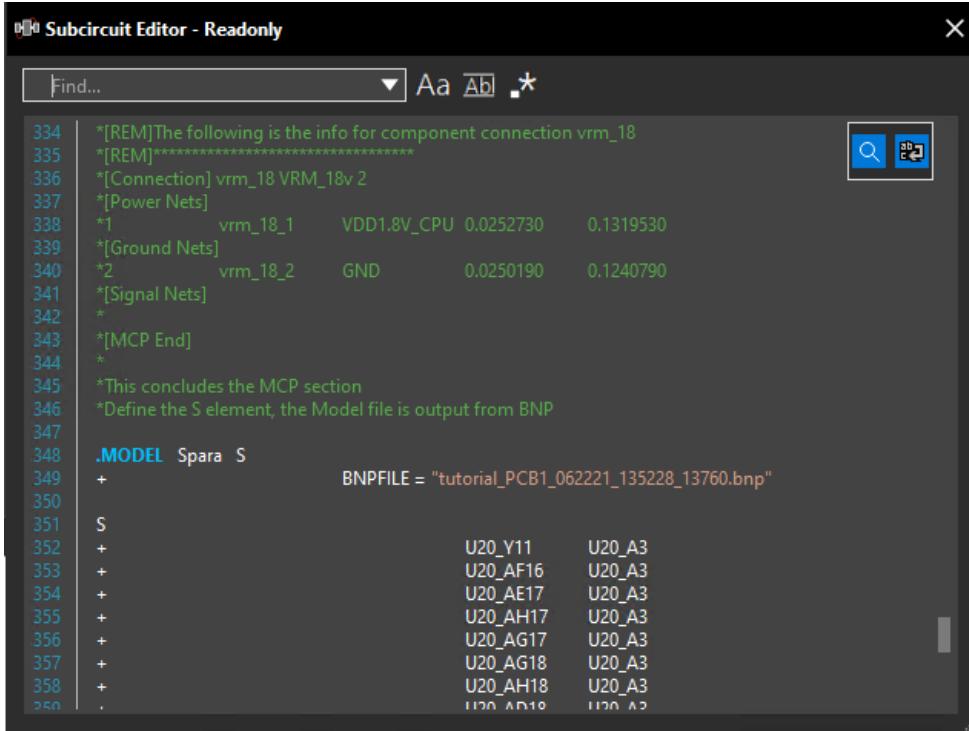


Note: The display of Y-axis in log scale has been disabled in results view shown above by selecting the related option from the shortcut menu accessed with a right-click on the waveform canvas.

Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

9. Click *View Subcircuit* in the *Edit Properties* panel. The *Subcircuit Editor* opens in non-editable mode.



The screenshot shows the 'Subcircuit Editor - Readonly' window. The title bar has a magnifying glass icon and the window title. Below the title bar is a toolbar with a search icon, a font size dropdown, and a refresh/cancel icon. The main area contains a text editor with numbered lines of code. The code includes comments starting with '*' and sections like '[Connection]', '[Power Nets]', '[Ground Nets]', '[Signal Nets]', '[MCP End]', and a MODEL section. The MODEL section specifies a S-parameter model named 'S' with a BNPFILE of 'tutorial_PCB1_062221_135228_13760.bnp'. There are also port definitions for U20_Y11 through U20_A3.

```
334 *[REM]The following is the info for component connection vrm_18
335 *[REM]*****
336 *[Connection] vrm_18 VRM_18v2
337 *[Power Nets]
338 *1 vrm_18_1 VDD1.8V_CPU 0.0252730 0.1319530
339 *[Ground Nets]
340 *2 vrm_18_2 GND 0.0250190 0.1240790
341 *[Signal Nets]
342 *
343 *[MCP End]
344 *
345 *This concludes the MCP section
346 *Define the S element, the Model file is output from BNP
347
348 .MODEL Spara S
349 +
350
351 S
352 +
353 +
354 +
355 +
356 +
357 +
358 +
359 .
360
361 U20_Y11 U20_A3
362 U20_AF16 U20_A3
363 U20_AE17 U20_A3
364 U20_AH17 U20_A3
365 U20_AG17 U20_A3
366 U20_AG18 U20_A3
367 U20_AH18 U20_A3
368 U20_AF19 U20_A3
```

Note: The SPICE file created using the Layout Extraction does not require editing. In particular, you **should not change** the pin-naming and model connection protocol (MCP) sections. The MODEL section includes information about the S-parameter filename, topology, port location, numbering, and naming.

Enable Package Models

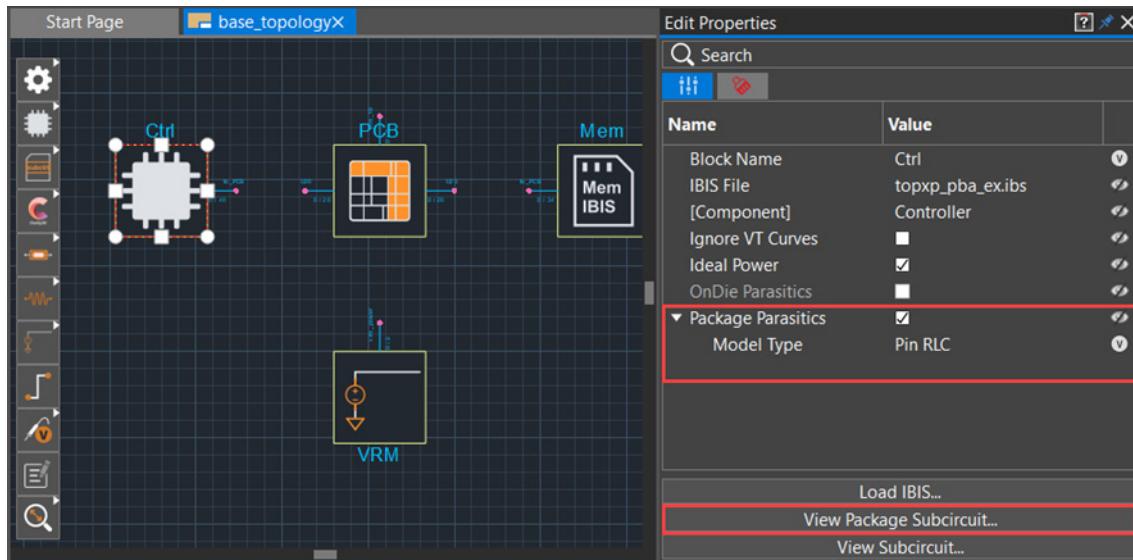
Packages can be modeled in the same way as PCB interconnects, with dedicated extraction using external tools like PowerSI. However, the PBA workflow also has the flexibility to use the package parasitics defined in IBIS files. For this example, you will enable the RLC parasitic models in the Controller and Memory components.

Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

Controller and Memory Package Model

1. Double-click the Controller component in the block diagram to open the corresponding properties in the *Edit Properties* panel.



2. Select the *Package Parasitics* check box. The *Model Type* is preset to *Pin RLC*. The *View Package Subcircuit* button also is added to the *Edit Properties* panel.
3. Click *View Package Subcircuit*. The *Subcircuit Editor* opens in read only mode.

```

1 .subckt Ctrl_Controller_Pin_RLC
2 + in_2 in_3 in_15 in_17 in_18 in_19 in_20 in_21 in_22
3 + in_23 in_32 in_33 in_42 in_43 in_51 in_52 in_62 in_64
4 + in_67 in_69 in_75 in_77 in_80 in_82 in_85 in_87 in_94
5 + in_96 in_99 in_101 in_104 in_106 in_111 in_113 in_116
6 + in_118 in_1 in_36 in_5 in_38 out_2 out_3 out_15 out_17
7 + out_18 out_19 out_20 out_21 out_22 out_23 out_32 out_33
8 + out_42 out_43 out_51 out_52 out_62 out_64 out_67 out_69
9 + out_75 out_77 out_80 out_82 out_85 out_87 out_94 out_96
10 + out_99 out_101 out_104 out_106 out_111 out_113 out_116
11 + out_118 out_1 out_36 out_5 out_38
12 * Package RLC Parameters
13 + R_pkg = 1.0146
14 + L_pkg = 7.151e-9
15 + C_pkg = 3.058e-12
16
17 * NOTE - This is the TopXplorer generated sub-circuit definition
18 * for the package parasitics based on the values of R_pin, L_pin and
19 * C_pin in the [Pin] section of the component 'Controller' in 'topxp_pba_ex.ibs' file.
20 * Editing of sub-circuit definition is NOT recommended.
21
22 ** Signals
23 x_2 in_2 out_2 in_5 onpkg_RLC R.Pin='R_pkg' L.Pin='L_pkg' C.Pin='C_pkg'
24 x_3 in_3 out_3 in_5 onpkg_RLC R.Pin='R_pkg' L.Pin='L_pkg' C.Pin='C_pkg'
25 x_15 in_15 out_15 in_5 onpkg_RLC R.Pin='R_pkg' L.Pin='L_pkg' C.Pin='C_pkg'
26 x_17 in_17 out_17 in_5 onpkg_RLC R.Pin='R_pkg' L.Pin='L_pkg' C.Pin='C_pkg'
27 x_18 in_18 out_18 in_5 onpkg_RLC R.Pin='R_pkg' L.Pin='L_pkg' C.Pin='C_pkg'
28

```

Topology Workbench: Parallel Bus Analysis Tutorial

Extracting and Generating an Interconnect Model

4. Review the definition and close the editor.
5. Repeat step 1 to step 4 for the Memory component.

Connecting the Blocks

In the previous chapters, we configured the properties of the Controller, Memory, and PCB blocks and assigned relevant device models to each. However, these three blocks and the VRM block in our topology are still unconnected.

To proceed, let us start with editing the properties of the VRM block and then establish connections between all four blocks to assign an electrical model to them. Connecting all blocks on the canvas together helps to develop a circuit schematic and show the actual electrical connections between the blocks.

In the Topology Workbench – Parallel Bus Analysis (PBA) workflow, you can use the block-based connectivity to connect the blocks at the net, pin, and node levels. Though the default mode of connectivity in PBA workflow is block-based, you can also use wire-based connectivity if required.

In the PBA workflow, for the Controller and Memory components, the connections netlist is created automatically from the IBIS file.

For the VRM block, the connections netlist is contained in the `.sp` file. This file also includes the model's information that can be edited.

For the PCB and other interconnects, the model's information is saved in a `.CKT` netlist file. Tools such as Sigrity PowerSI are used for generating the `.CKT` files from the network parameter simulation results.

For most system designs, the connections between components will be created automatically based on common pin names. The exception to this rule are connections between the Power and Ground nets that mostly require manual editing.

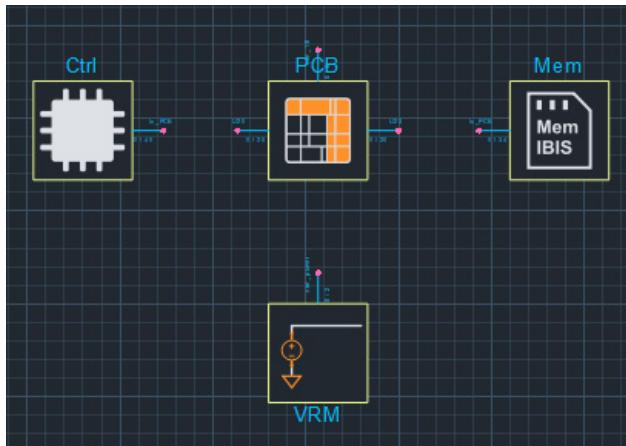
Tutorial Files

The block diagram for this chapter consists of a Controller, a PCB, a Memory and a VRM component after [Extracting and Generating an Interconnect Model](#). These blocks have been

Topology Workbench: Parallel Bus Analysis Tutorial

Connecting the Blocks

defined and linked to models, but have not been connected together, as shown in the following figure.



If you have performed the tasks covered in the previous chapter, you can continue with the same design files.

If you are starting directly from this chapter, open the `connecting_blocks.topx` file from the following directory:

```
<INSTALL_DIR>\share\topxp\Tutorials\PBA_Tutorial\connecting_blocks
```

Configure the VRM and Connect it to the PCB

The Topology Workbench – PBA workflow allows non-ideal power simulation, including all aspects of power distribution network (PDN) modeling. This includes real power and ground planes in the PCB and package interconnects, as well as the I/O and VRM models.

In this section, you will connect the VRM block to the PCB block and define a simple model for it.

When non-ideal power simulations are performed, on-die parasitics should be included in the models of Controller and Memory component to include the effects of any on-die decoupling capacitance. These are defined when the *OnDie Parasitics* check box is selected in the *Edit Properties* panel of a Controller or Memory block.

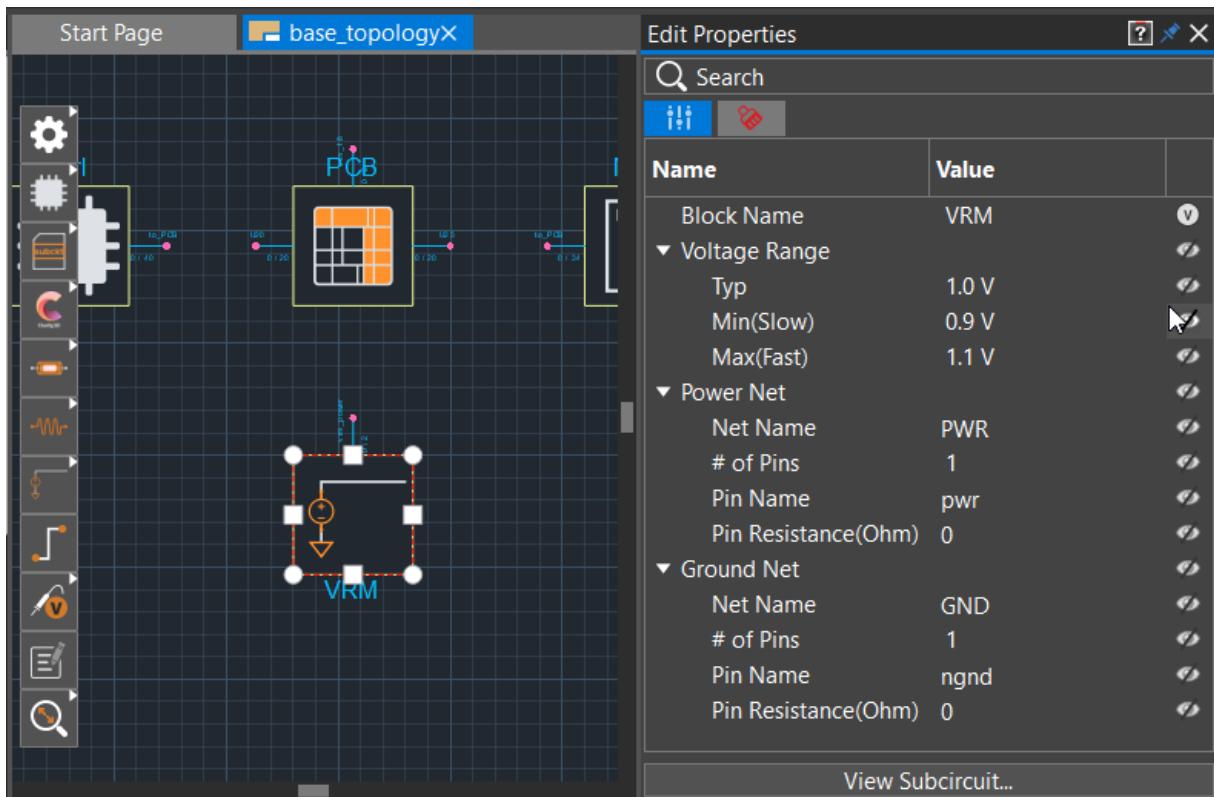
Update the VRM Block Properties

In this section, you will edit the VRM component and define the model.

Topology Workbench: Parallel Bus Analysis Tutorial

Connecting the Blocks

1. Double-click the VRM block to open the *Edit Properties* panel.



This netlist file is created when you add the VRM block to the block diagram. This file uses a model with constant DC voltage having Typical, Minimum, and Maximum corners as shown in the figure.

2. Click *View Subcircuit* to open the circuit definition netlist in read only mode. Review the definition and close the dialog box.

The screenshot shows the 'Subcircuit Editor - Readonly' window. It displays the following netlist code:

```
1 .subckt VRM pwr ngnd
2 * User-specified corner voltage for the first transmit 'Corner' selected in the 'Analysis Option'.
3 + Voltage = 1.0      $ Typ Voltage
4
5 .ends VRM
6
```

3. Change the values in the Voltage Range schema as following to modify the DC Voltage source:

- Typ* = 1.35V

Topology Workbench: Parallel Bus Analysis Tutorial

Connecting the Blocks

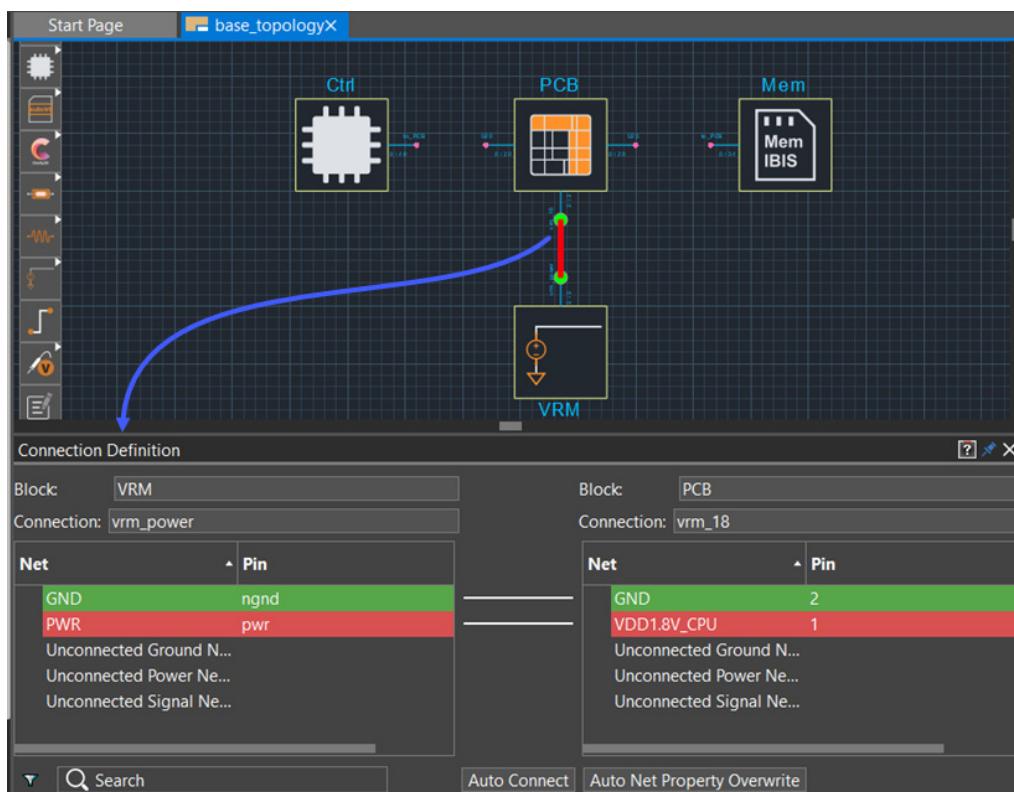
- $\text{Min}(\text{Slow}) = 1.27\text{V}$
- $\text{Max}(\text{Fast}) = 1.42\text{V}$

At this point all of the components in the bus are defined. The last step before simulation is to define the connections between each component.

Connect the PCB Block to the VRM Block

The *PCB* block has two connection ports, out of which the one that needs to be connected to the *VRM* block is labeled as *vrm*.

1. Click the rounded end of the *PCB* block's *vrm* connection port. The port gets highlighted.
2. Move the pointer to the connection port of the *VRM* block. As the pointer moves, a pink line indicating the connectivity path trails. When the pointer is placed on the *VRM* block's connection port, this target port is highlighted too.
3. Click the connection port of the *VRM* block. The color of the two connected ports changes to green and the *Connection Definition* panel opens.



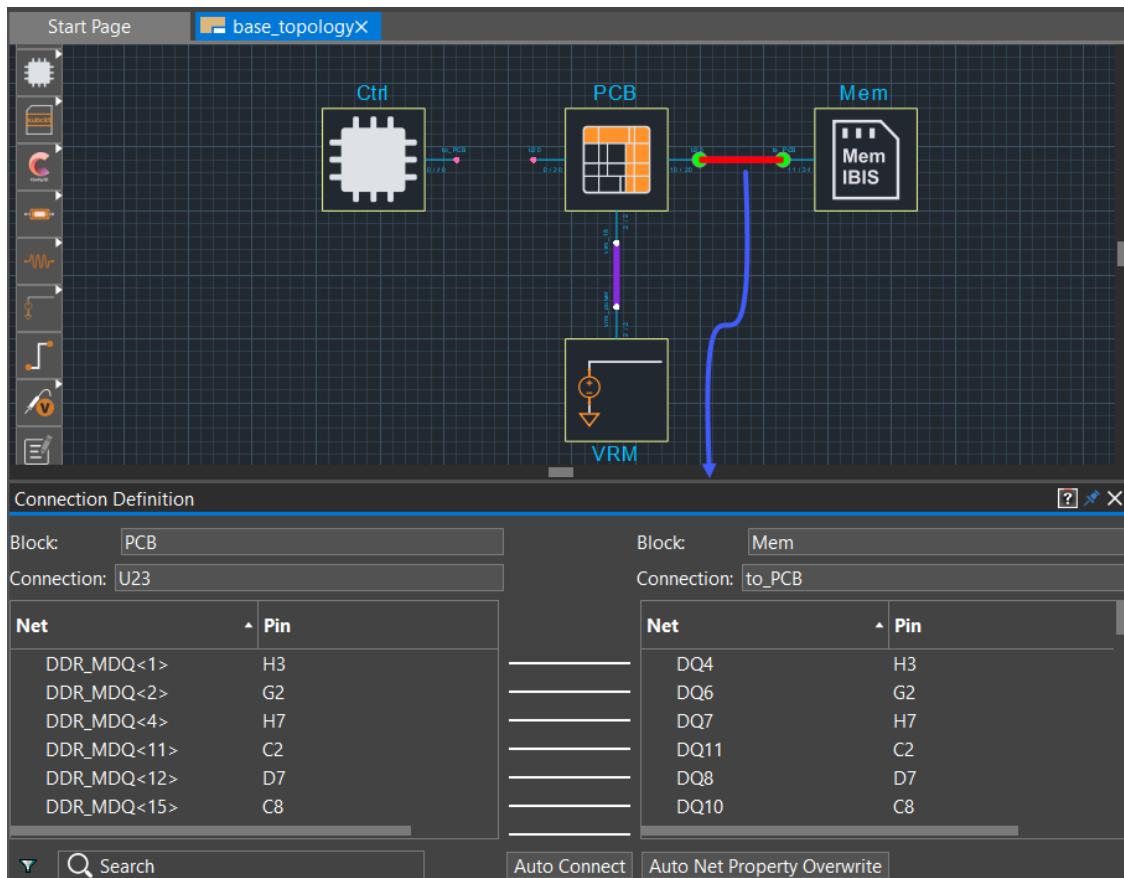
4. Verify the connections that Topology Workbench sets automatically.

Topology Workbench: Parallel Bus Analysis Tutorial

Connecting the Blocks

Connect the PCB Block to the Memory Block

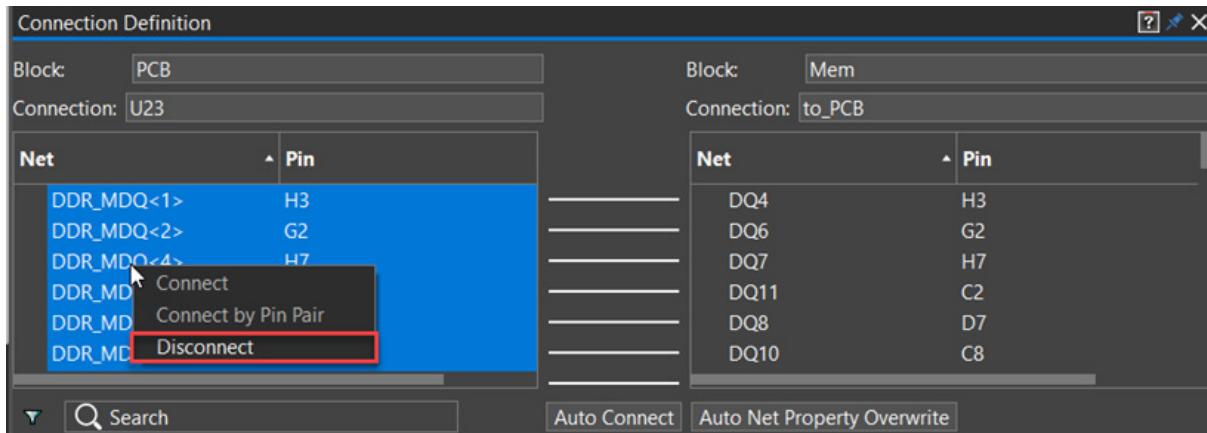
1. Connect the *PCB* block to the *Memory* block. Follow the same process that you did to connect the *VRM* block to the *PCB* block (see [step 1](#) to [step 3](#)). The *Connection Definition* panel opens with a list of Net, Pin, and Cktnode of the two blocks displayed in two panes.



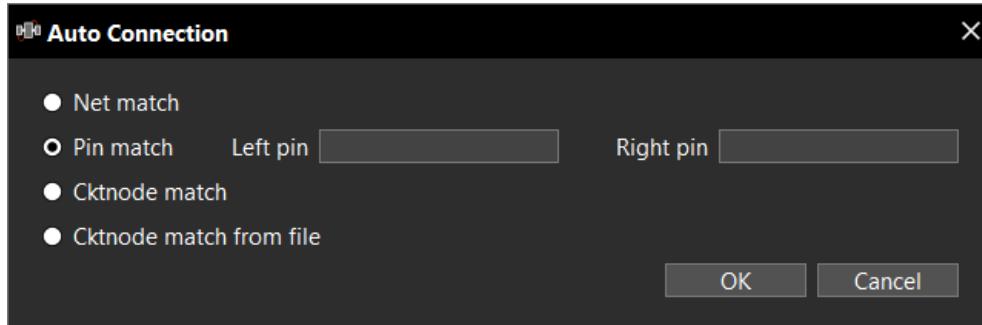
Topology Workbench: Parallel Bus Analysis Tutorial

Connecting the Blocks

2. Remove the default connections. For this, select all connected nets in one of the panes while keeping the **Ctrl** key pressed and right-click to open the shortcut menu from which you select *Disconnect*.



3. Click *Auto Connect*. The *Auto Connection* dialog box opens. Now, lets connect all *DQ* signals of the Memory block to all *DDR_MDQ* signals of the PCB block.
4. Select *Net match*.

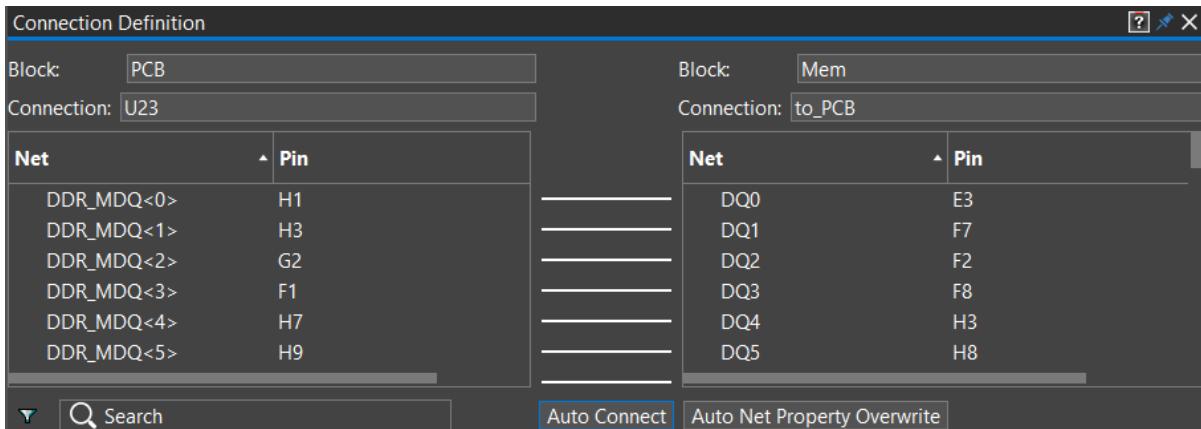


5. Enter *DDR_MDQ<*>* in the *Left net* box.
6. Enter *DQ** in the *Right net* box.

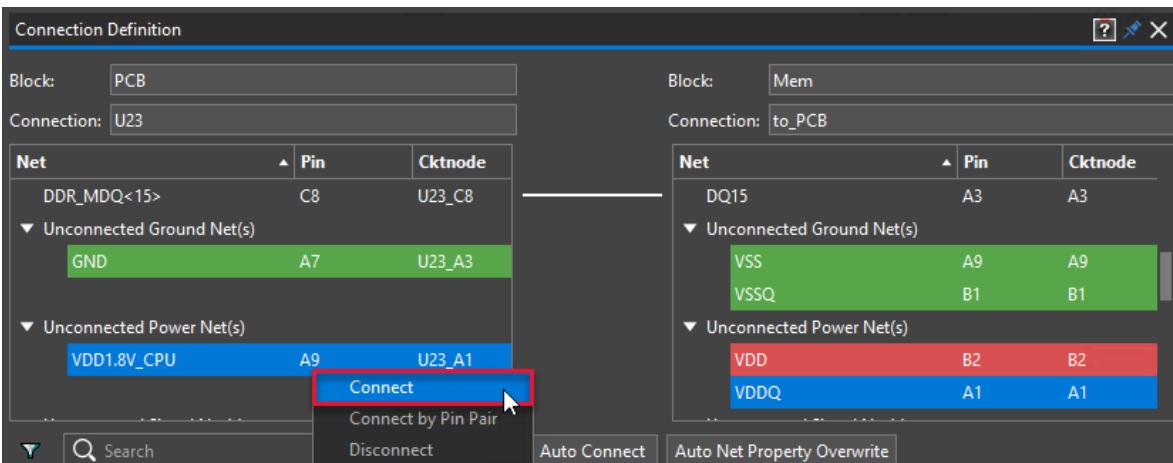
Topology Workbench: Parallel Bus Analysis Tutorial

Connecting the Blocks

7. Click *OK* to create connections. The *Connection Definition* panel shows the established connections.



8. Scroll down the list to display the *Unconnected Power Net(s)*.



9. From the left column, select *VDD1.8V_CPU*.
10. From the right column, select *VDDQ*.
11. Right-click to open the shortcut menu and select *Connect*.
12. Similarly, connect *GND* to *VSSQ*.

Topology Workbench: Parallel Bus Analysis Tutorial

Connecting the Blocks

All PCB signals required for this tutorial are now connected as shown in the following figure:

Connection Definition		
Block:	PCB	Block:
Connection:	U23	Connection:
Net	Pin	Cktnode
DDR_MDDQ<9>	D3	U23_D3
DDR_MDDQ<10>	D1	U23_D1
DDR_MDDQ<11>	C2	U23_C2
DDR_MDDQ<12>	D7	U23_D7
DDR_MDDQ<13>	D9	U23_D9
DDR_MDDQ<14>	B9	U23_B9
DDR_MDDQ<15>	C8	U23_C8
GND	A7	U23_A3
VDD1.8V_CPU	A9	U23_A1
▼ Unconnected Ground Net(s)		
▼ Unconnected Power Net(s)		
Block: Mem		
Connection: to_PCB		
Net	Pin	Cktnode
DQ9	C3	C3
DQ10	C8	C8
DQ11	C2	C2
DQ12	A7	A7
DQ13	A2	A2
DQ14	B8	B8
DQ15	A3	A3
VSSQ	B1	B1
VDDQ	A1	A1
▼ Unconnected Ground Net(s)		
VSS	A9	A9
▼ Unconnected Power Net(s)		
VDD	B2	B2

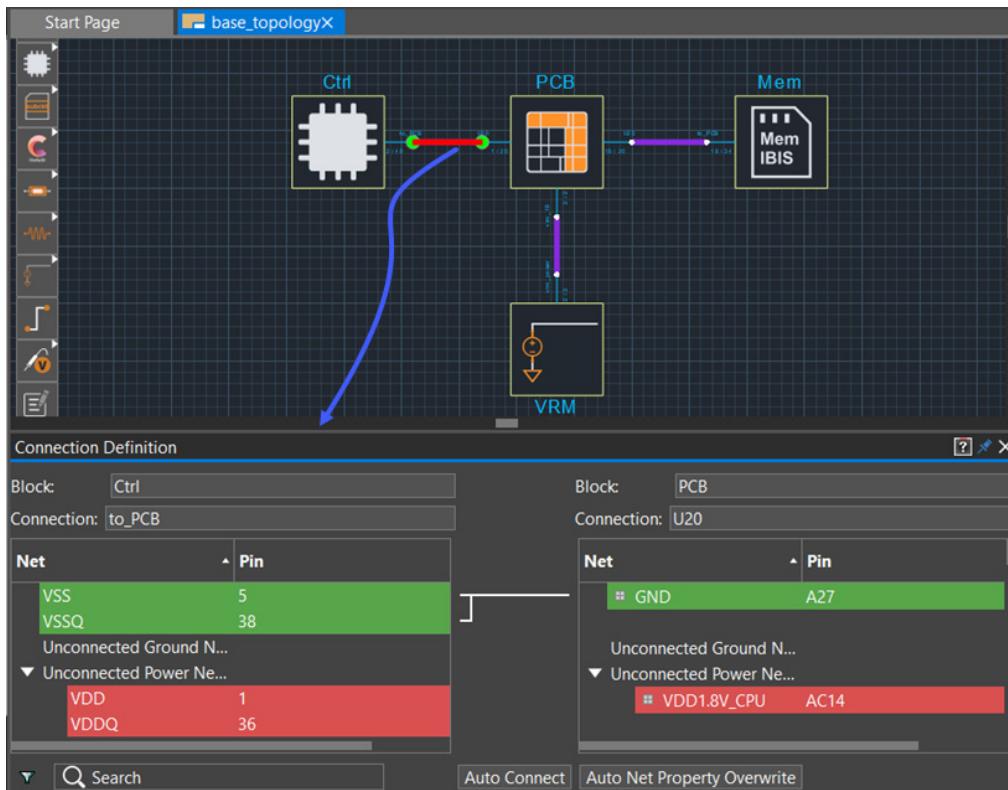
Connect the Controller Block to the PCB Block

1. Connect the *Controller* block to the *PCB* block. Follow the same process that you did to connect the *VRM* block to the *PCB* block (see [step 1](#) to [step 3](#)). The *Connection*

Topology Workbench: Parallel Bus Analysis Tutorial

Connecting the Blocks

Definition panel opens with a list of Net, Pin, and Cktnode of the two blocks displayed in two panes.



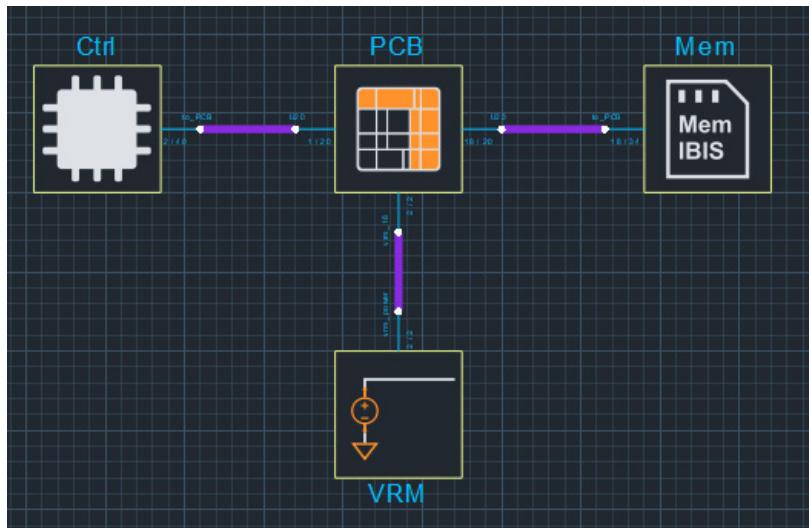
2. Connect signals *DQ** to *DDR_MDQ<*>* using the *Auto Connect* button (see [step 3](#) to [step 7](#) of the [Connect the PCB Block to the Memory Block](#) section.)
3. Connect the following signals.
 - VDDQ* to *VDD1.8V_CPU*
 - VSSQ* to *GND*

Note: If the ground nets and power nets appear with automatic connections, then disconnect

Topology Workbench: Parallel Bus Analysis Tutorial

Connecting the Blocks

The block diagram is updated and now shows a valid connection between the Controller and PCB blocks as well.

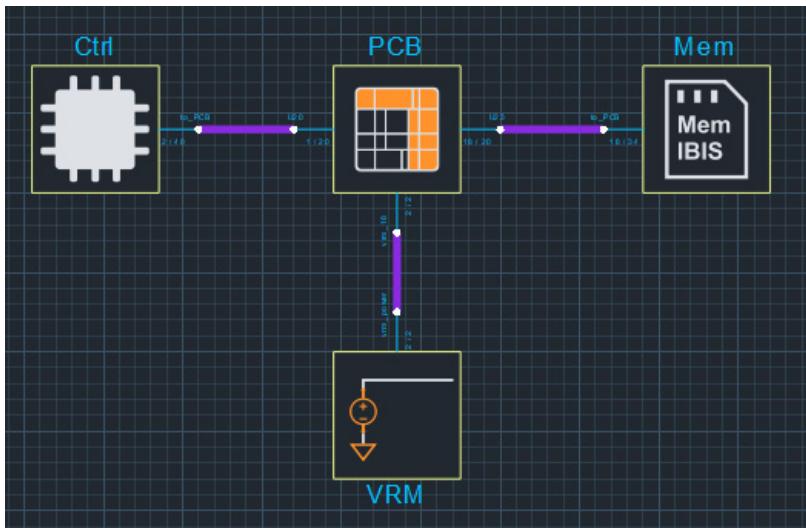


Running Simulations and Analyzing the Results

The basic simulation settings are specified in the *Analysis Options* panel. After you specify the simulation settings and perform an initial simulation, you can make the required changes to the bus design and simulation settings, and experiment with the other Topology Workbench features on the bus.

Tutorial Files

The block diagram for this chapter consists of a *Controller*, *Memory*, *PCB*, and *VRM* component, as created in previous chapters. This design is fully defined with models for each component and a valid connection between each of the components.



If you have performed the tasks covered in the previous chapter, you can continue with the same design files.

Topology Workbench: Parallel Bus Analysis Tutorial

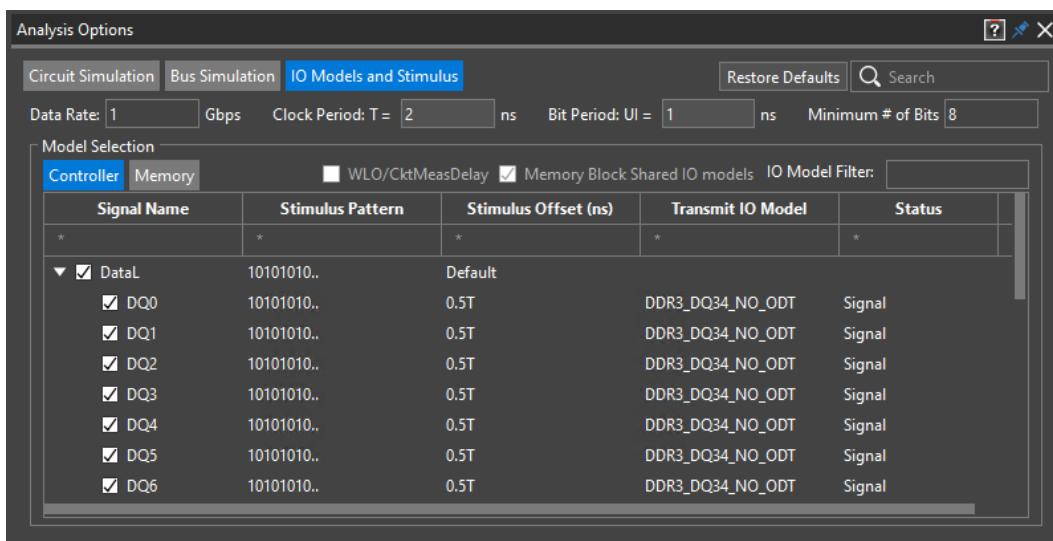
Running Simulations and Analyzing the Results

If you are starting directly from this chapter, open the `simulate_topology.topx` file from the following directory:

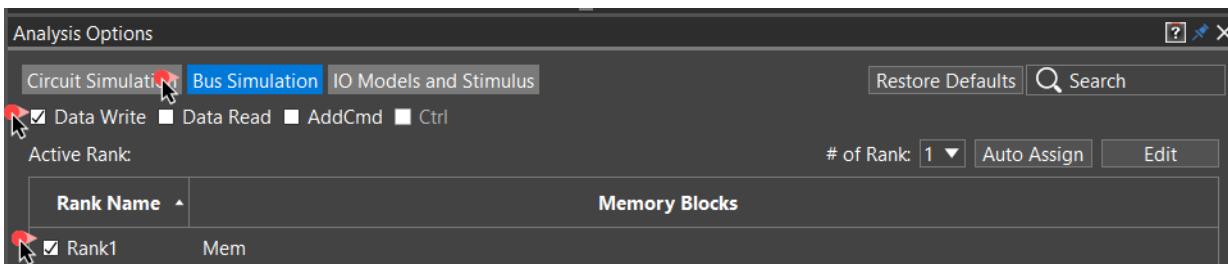
```
<INSTALL_DIR>\share\topxp\Tutorials\simulate_topology
```

Set Analysis Options for the Simulation

1. Click *Set Analysis Options* in the *Workflow* panel. The *Analysis Options* panel opens with the *IO Models and Stimulus* tab selected by default.



2. Click the *Bus Simulation* tab and configure the following settings for the bus simulation run:

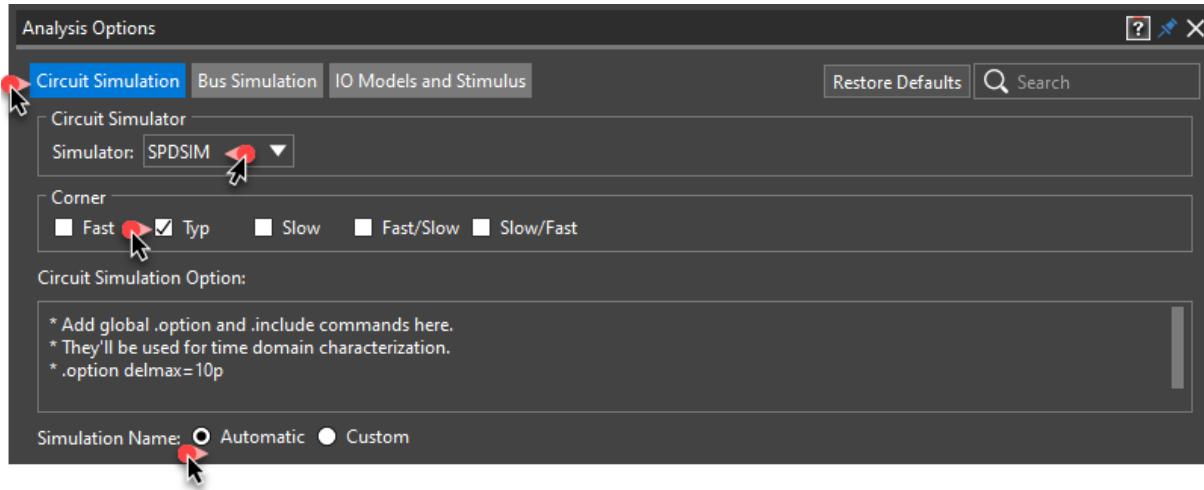


- a. Select the *Data Write* check box to define the bus type and its direction.
- b. Select the *Rank1* check box in the *Active Rank* table. (Only one option is listed for selection because the topology created in this tutorial contains only one memory block.)

Topology Workbench: Parallel Bus Analysis Tutorial

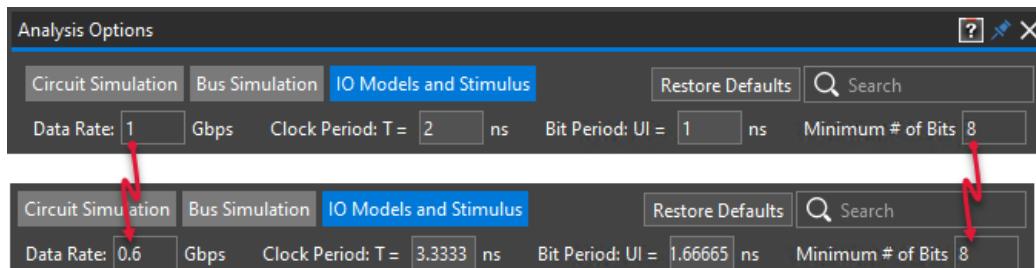
Running Simulations and Analyzing the Results

3. Click the Circuit Simulation tab to specify the circuit simulator of your choice, corner settings, circuit simulations options, and simulation name option. For this tutorial, ensure that the following default settings are not changed:



- a. *Circuit Simulator = SPDSIM*
 - b. *Corner = Typ*
 - c. *Circuit Simulation Option = no options*
 - d. *Simulation Name = Automatic*
4. Click the IO Models and Stimulus tab.
5. Set *Data Rate* to *0.6* in the Stimulus Definition and Model Selection section.

Based on the changed *Data Rate* value, the *Clock Period* (*T* for this data rate) and *Bit Period* (*UI* for this data rate) are recalculated and displayed in the respective read-only boxes.

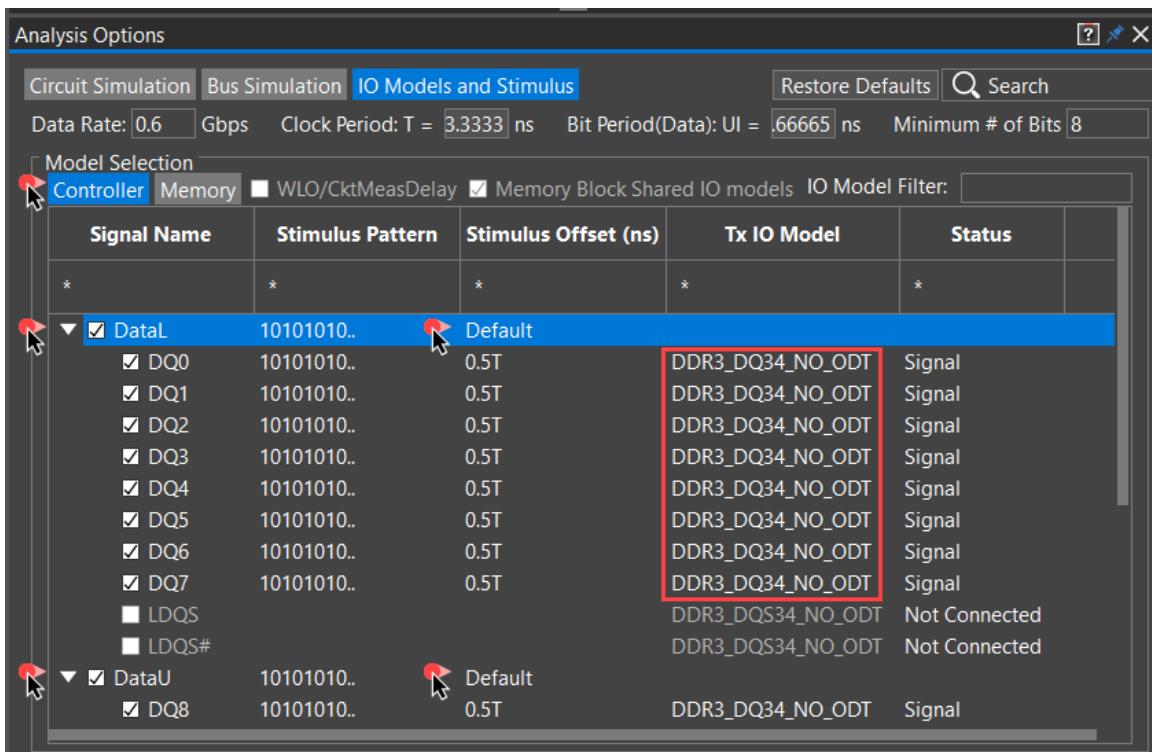


6. Let the *Minimum # of Bits* be set to *8*, that is, its default value.

Topology Workbench: Parallel Bus Analysis Tutorial

Running Simulations and Analyzing the Results

7. Verify that the following are set in the *Controller* tab and do not make any other changes for this tutorial:



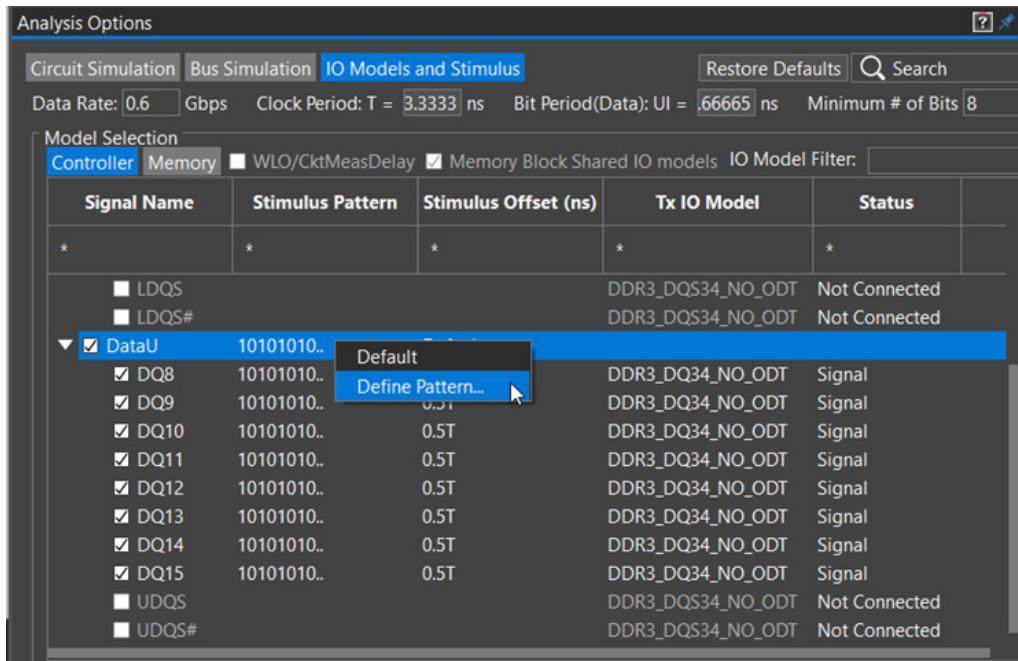
- In the *Signal Name* column, the check boxes for the two data bus groups, *DataL* and *DataU*, are selected. These bus groups connect signals from *DQ0* to *DQ15*.
- In the *Stimulus Offset (ns)* column, select *Default* in the rows for *DataL* and *DataU* bus groups. The relative delay for each data line and strobe is set to *0.5T* for the *DQ** signals.
- In the *Tx IO Model* column, use the *DDR3_DQ34_NO_ODT* model for all the *DQ** signals.

Note: The *WLO/ClkMeasDelay* and *Memory Block Shared IO Model* check boxes are disabled because the tutorial design contains only one memory.

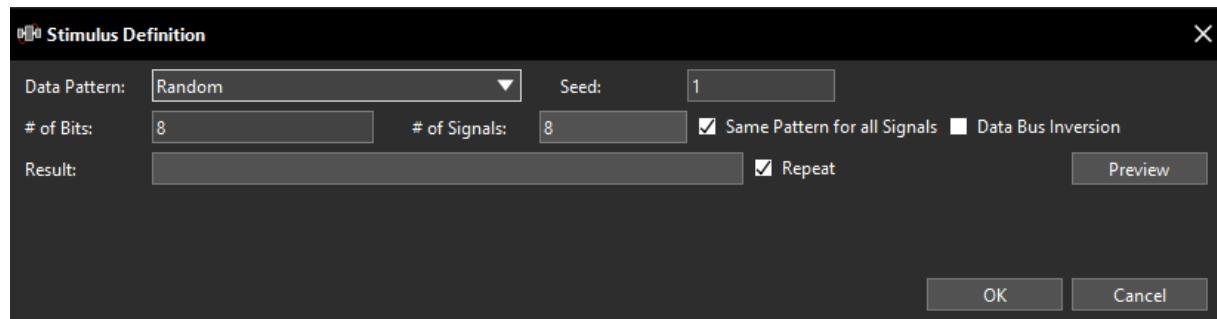
Topology Workbench: Parallel Bus Analysis Tutorial

Running Simulations and Analyzing the Results

8. Select the *DataU* row and right-click the cell under the *Stimulus Pattern* column. By default, a stimulus pattern identical to *10101010..* is defined for each data and strobe line.



9. Select *Define Pattern...* from the displayed shortcut menu. The *Stimulus Definition* dialog box is displayed.



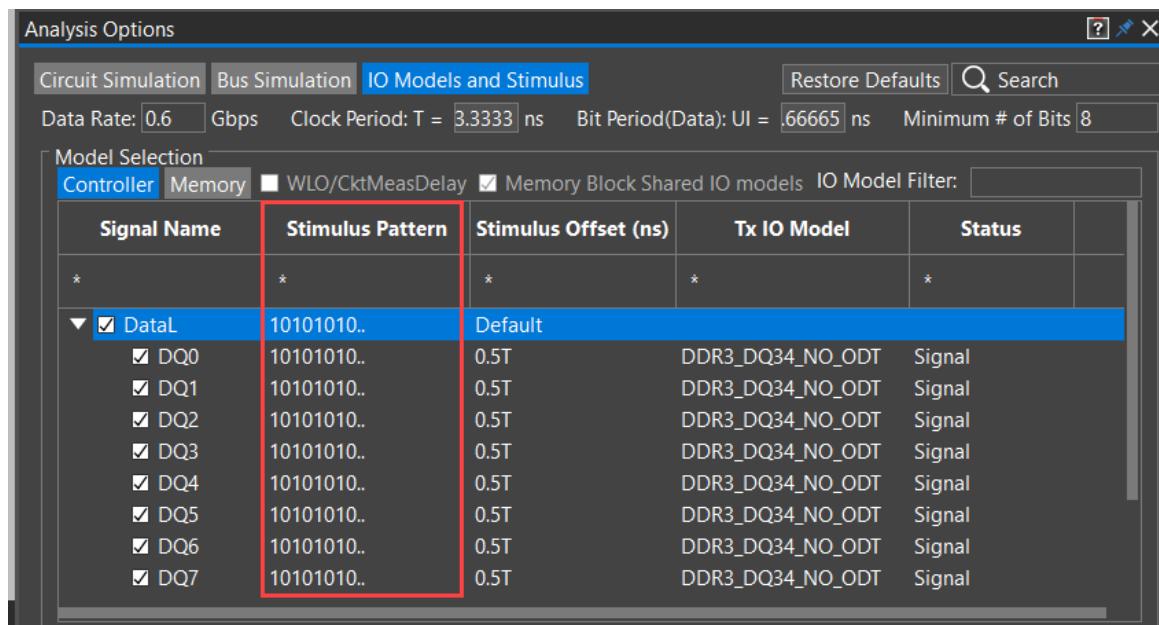
Topology Workbench: Parallel Bus Analysis Tutorial

Running Simulations and Analyzing the Results

10. Select *PRBS* from the *Data Pattern* list.



11. Click *Preview* to view the stimulus pattern in the *Result* box, which is used for verifying the changed data pattern.
12. Click *OK*. The dialog box closes and the values displayed in the *Stimulus Pattern* column change as per the edits incorporated above.

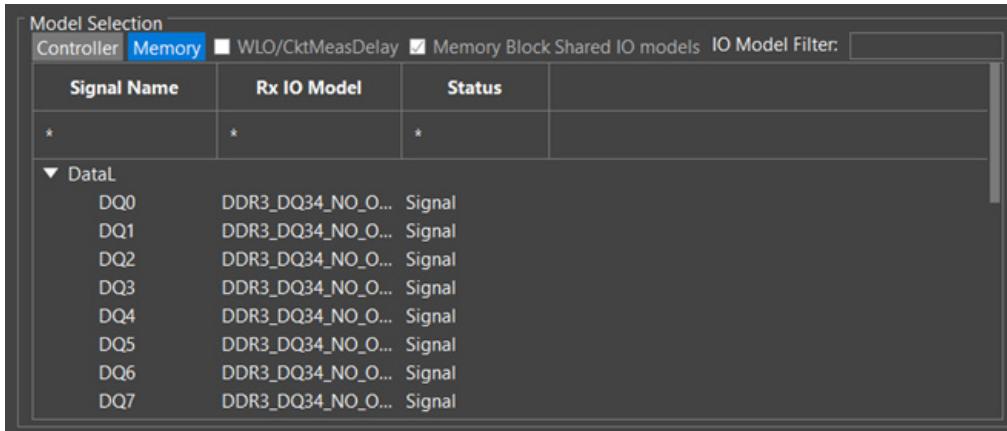


13. Select the *DataU* row and repeat step 8 to step 12.
14. Click the *Memory* tab to review its contents. For a single memory device, this tab only displays the two corresponding bus groups, *DataL* and *DataU*, which connect signals

Topology Workbench: Parallel Bus Analysis Tutorial

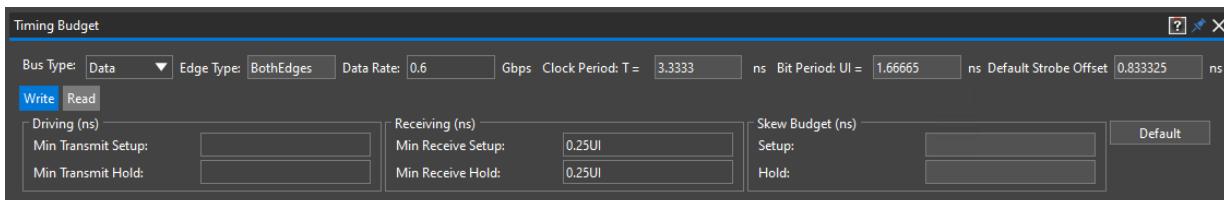
Running Simulations and Analyzing the Results

from *DQ0* to *DQ15*. Ensure that the *Receive IO Model* is set to the *DDR3_DQ34_NO_ODT* model for all the *DQ** signals.



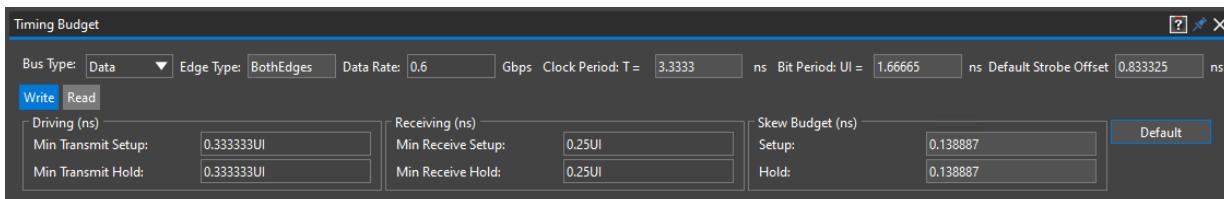
Set Timing Budget for the Simulation

1. Click *Set Timing Budget* in the *Simulation Setup* schema. Alternatively, click *Tools – Timing Budget....* The *Timing Budget* panel opens.



Note: The values set/reset in the *Analysis Options* panel are updated in the *Timing Budget* panel. For example, notice *Bus Type*, *Data Rate*, *Clock Period*, and *Bit Period*.

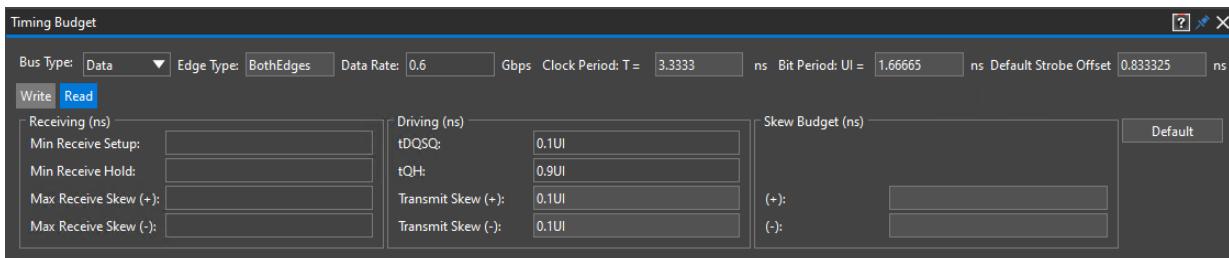
2. Click the *Default* button in the *Write* tab to populate the *Driving*, *Receiving*, and *Skew Budget* text boxes with the respective default values. You can enter desired values as well, but for this tutorial, use the default values.



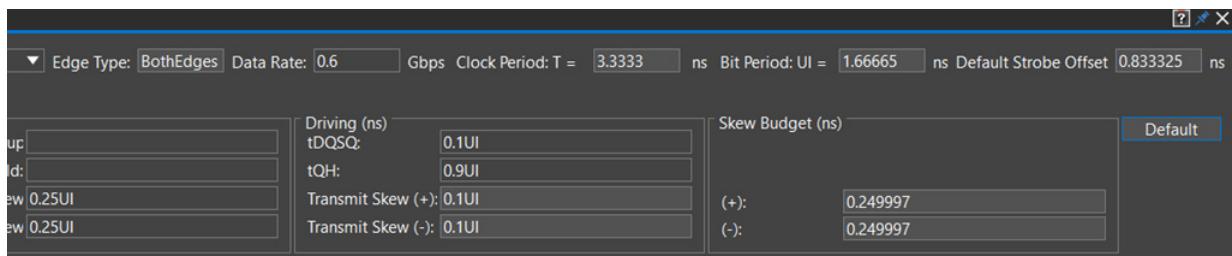
Topology Workbench: Parallel Bus Analysis Tutorial

Running Simulations and Analyzing the Results

- Click the *Read* tab.



- Click the *Default* button in the *Read* tab to populate the *Driving*, *Receiving*, and *Skew Budget* text boxes with the respective default values. You can enter desired values as well, but for this tutorial, use the default values.



Simulate the Topology using Ideal Power

The bus has now been fully defined. Recall that it consists of a Controller (U20), Memory (U23), and a VRM on a PCB.

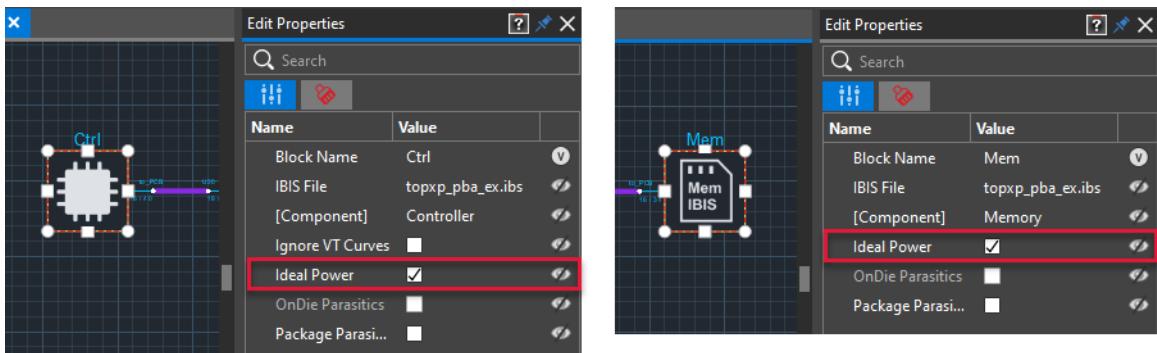
Let us start with simulating the topology using Ideal Power, while ignoring the Power Distribution Network (PDN) and Voltage Regulator Module (VRM) in the topology.

Topology Workbench: Parallel Bus Analysis Tutorial

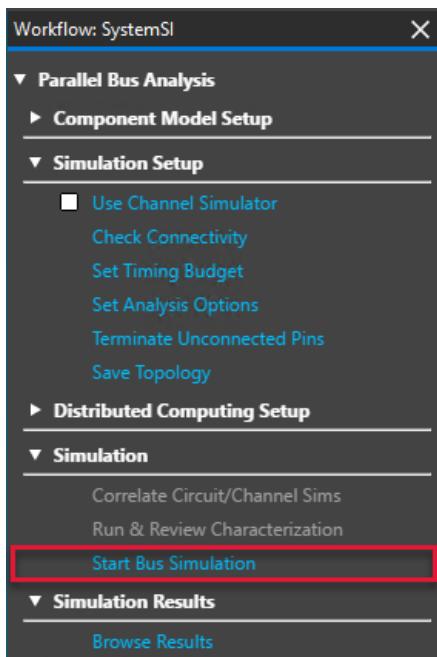
Running Simulations and Analyzing the Results

Start the Simulation

1. Verify that the *Ideal Power* check box is selected for both *Controller* and *Memory* blocks in their respective properties.



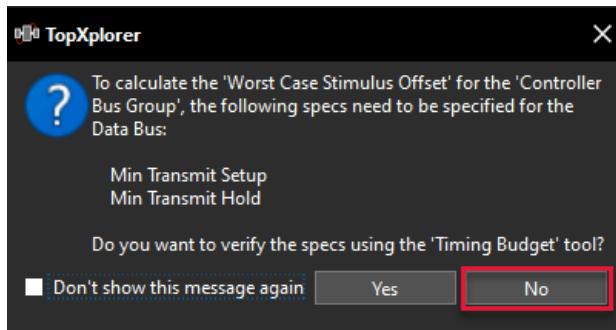
2. Click *Start Bus Simulation* in the *Workflow* panel or click the play (▶) button.



Topology Workbench: Parallel Bus Analysis Tutorial

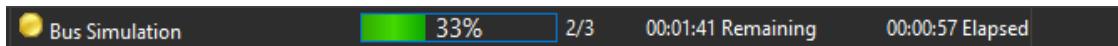
Running Simulations and Analyzing the Results

3. Click **No** in the warning message box that is displayed. This warning can be ignored because you had set the specifications to default in the *Timing Budget* panel. Refer to the [Set Timing Budget for the Simulation](#) section.

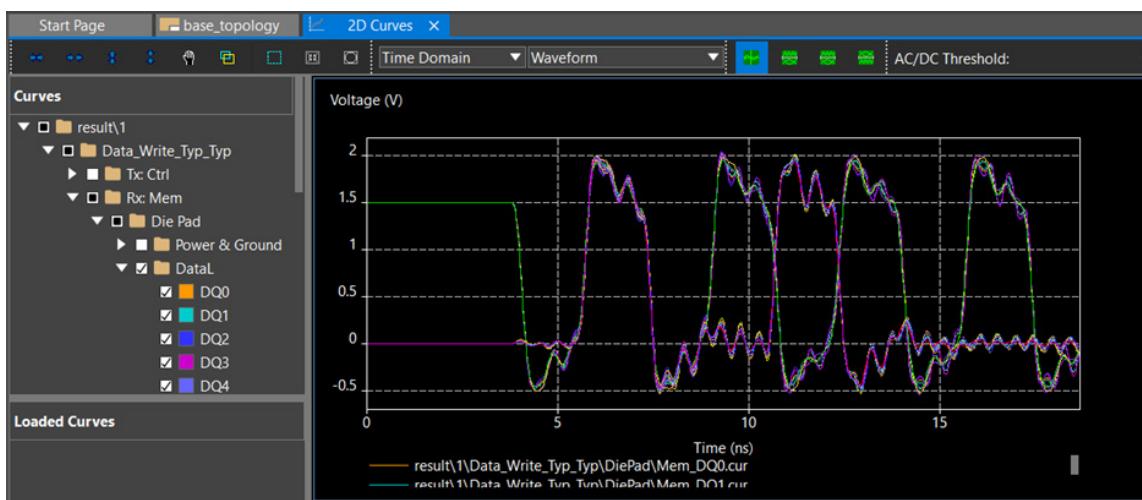


Note: If during a previous simulation run, you selected the *Do not show again* check box, this message box is not displayed.

The simulation starts to run. The status bar gives you a run-time glimpse of the type of processing that Topology Workbench is running on the topology, such as, *Check Connectivity* and *Bus Simulation*. It also shows the time elapsed and remaining.



When the process finishes, the *2D Curves* tab opens with the relevant waveform results that are generated based on the *Corner* options selected in the *Circuit Simulation* tab of the *Analysis Options* panel.



Note: Select the check box adjacent to *Power & Ground* to view the waveforms of the power and ground signals also.

Topology Workbench: Parallel Bus Analysis Tutorial

Running Simulations and Analyzing the Results

In addition, the simulation results are saved to a directory within your current workspace, that is, the directory you specified in the *Topology Path* field of the *Create New Topology* dialog box. For details, refer to [Review the Simulation Results Directory](#).

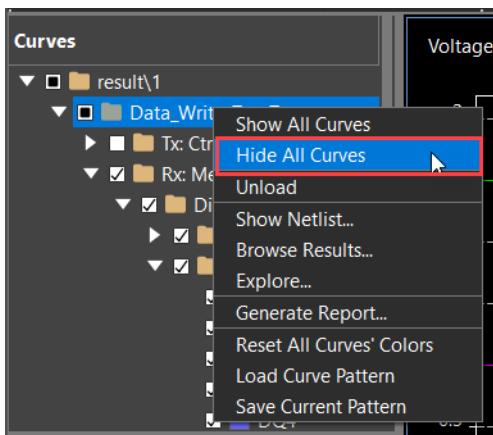
Review the Generated Simulation Results in the 2D Curves Tab

Data for each signal in the bus can be selected and viewed individually as a raw waveform or an eye diagram.

In the *2D Curves* tab, the *Curves* pane lists the simulation results including each signal or power net, such as, the two data buses, *DataL* and *DataU*, used in our tutorial.

Each element in the tree has a check box adjacent to it. You can select or deselect a check box to control viewing of waveform for the corresponding net. For example, to view the curves for only *DQ0* to *DQ7* from the *DataL* bus group along with the *Power & Ground* nets:

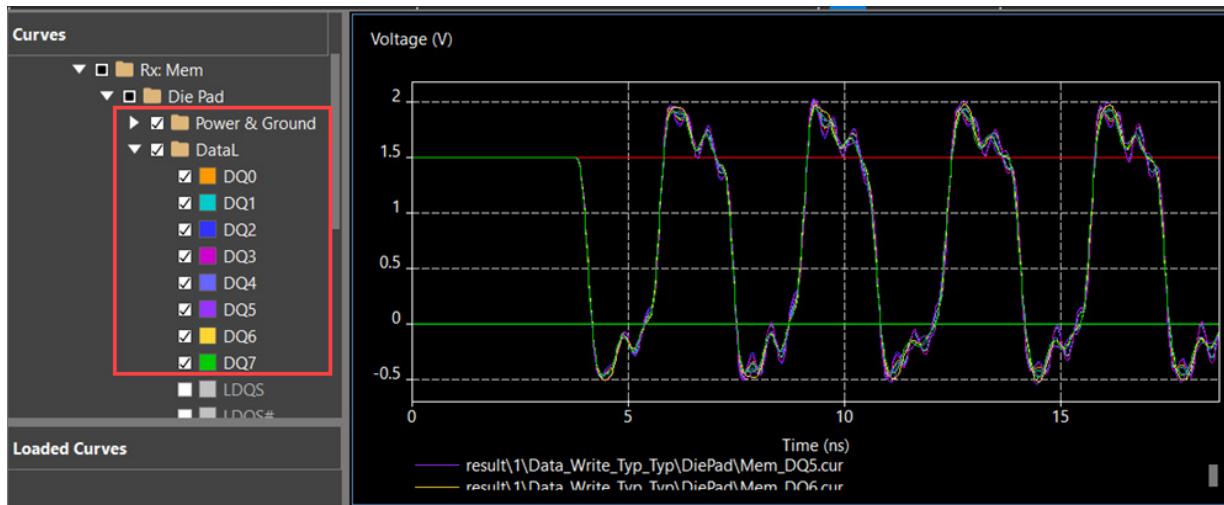
1. Right-click in the *Curves* pane and select *Hide All Curves* from the displayed shortcut menu.



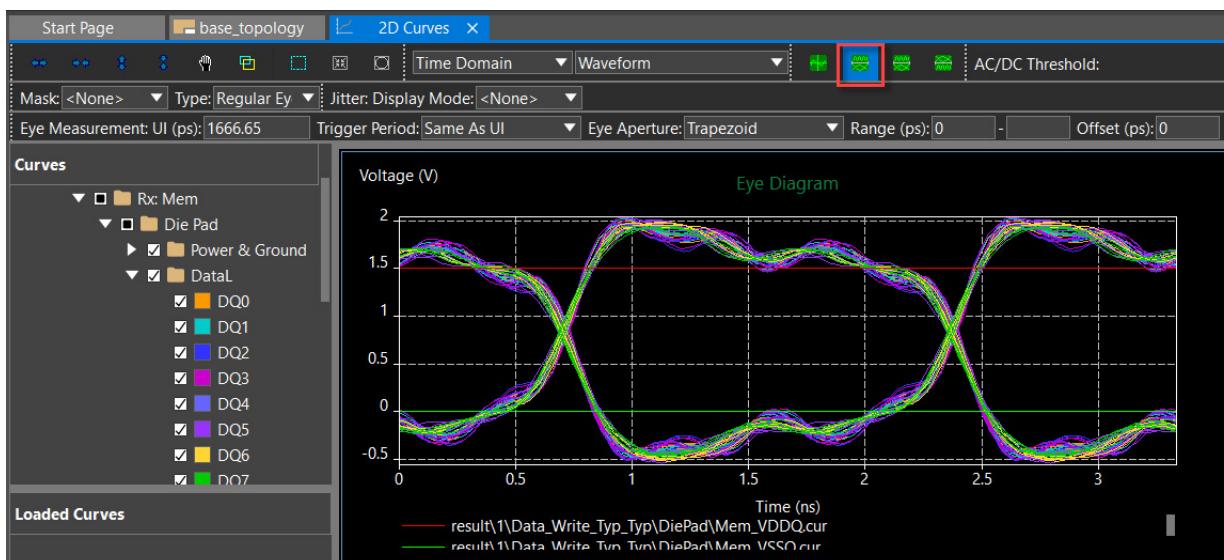
Topology Workbench: Parallel Bus Analysis Tutorial

Running Simulations and Analyzing the Results

2. Select the check boxes adjacent to *Power & Ground* and the *DQ0* to *DQ7* signals from the *Die Pad*. The waveform in the right pane of the *SS/Viewer* window is refreshed to display the plotted data for only these signals as shown below.



3. Select the *Show Eye Diagram* only button from the toolbar, as shown below. The right pane of the *2D Curves* tab is refreshed again to display the plotted waveform data in form of an eye diagram.



With the *Eye Diagram* visible, the toolbar now has additional measurement and data processing functions available. You can specify an *Eye Contour* or *Eye Density* plot, overlay

Topology Workbench: Parallel Bus Analysis Tutorial

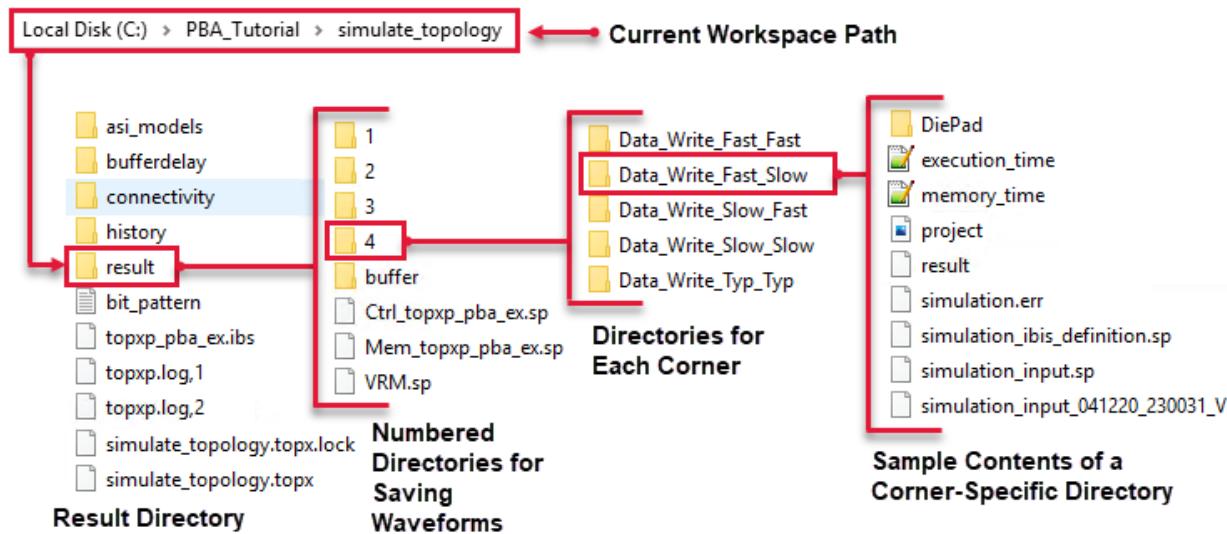
Running Simulations and Analyzing the Results

an *Eye Mask*, or measure the Eye opening including *Trigger Period*, *Eye Aperture*, *Min Tac Width*, *Range*, *Offset* and *# of Period*.

You can also view the Jitter values. Select *Density* from the *Jitter: Display Mode* list to overlay the Jitter estimate on the Eye Diagram.

Review the Simulation Results Directory

Each simulation creates a unique directory (1, 2, 3 ...) where all the related waveform files are saved. The default destination of these numbered directories is <currentWorkspacePath>\result. The image below illustrates the directory structure that gets created after the simulation run:



The directories created for each corner type selected in the *Analysis Options* panel are named in the following format:

<SimulationType>_<CornerType1>_<CornerType2>

For example, in the PBA workflow, the directories are named as:

- Data_Write_Typ_Typ
- Data_Write_Fast_Fast
- Data_Write_Slow_Slow
- Data_Write_Slow_Fast
- Data_Write_Fast_Slow

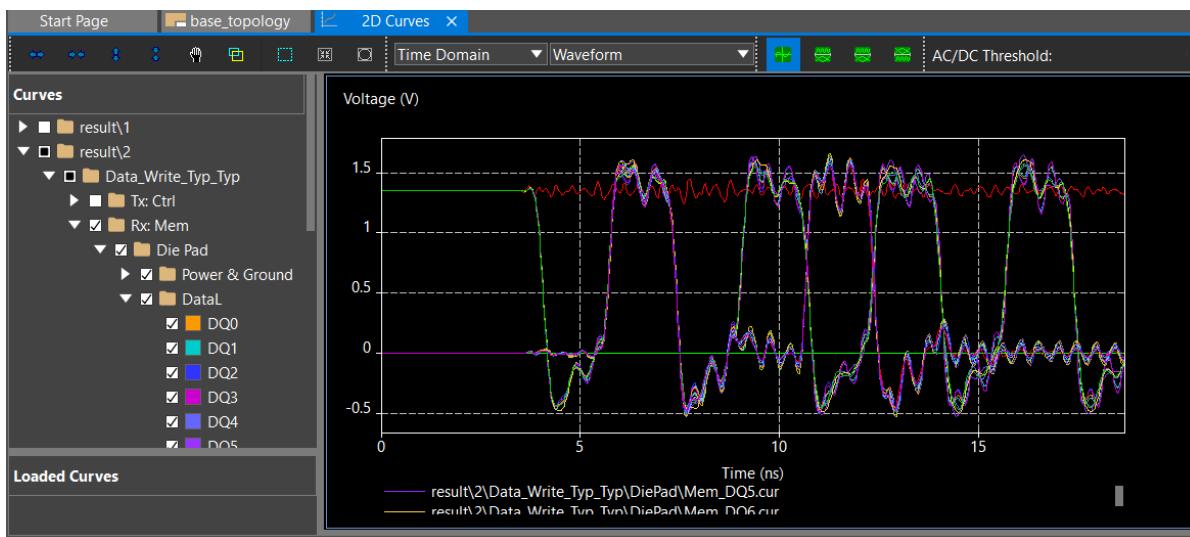
Topology Workbench: Parallel Bus Analysis Tutorial

Running Simulations and Analyzing the Results

By default, the `result` directory is moved to the `history` folder when an existing project is opened. To change this behavior, choose a different option in the *Result* module of the dialog box displayed when you select *Tools – Options* from the menu bar.

Simulate the Topology using Non-Ideal Power

1. Deselect the *Ideal Power* check box for both *Controller* and *Memory* in their respective *Edit Properties* panel. This effectively enables the 1.8V VCC connections on the PCB that were generated in the PowerSI extraction (see [Chapter 4, “Extracting and Generating an Interconnect Model”](#)), as well as the VRM and their references that are impacted in the *Controller* and *Memory*.
2. Click *Start Bus Simulation* in the *Workflow* panel to rerun simulation on the topology. When the process finishes, the *2D Curves* tab opens with the results of this simulation run also.

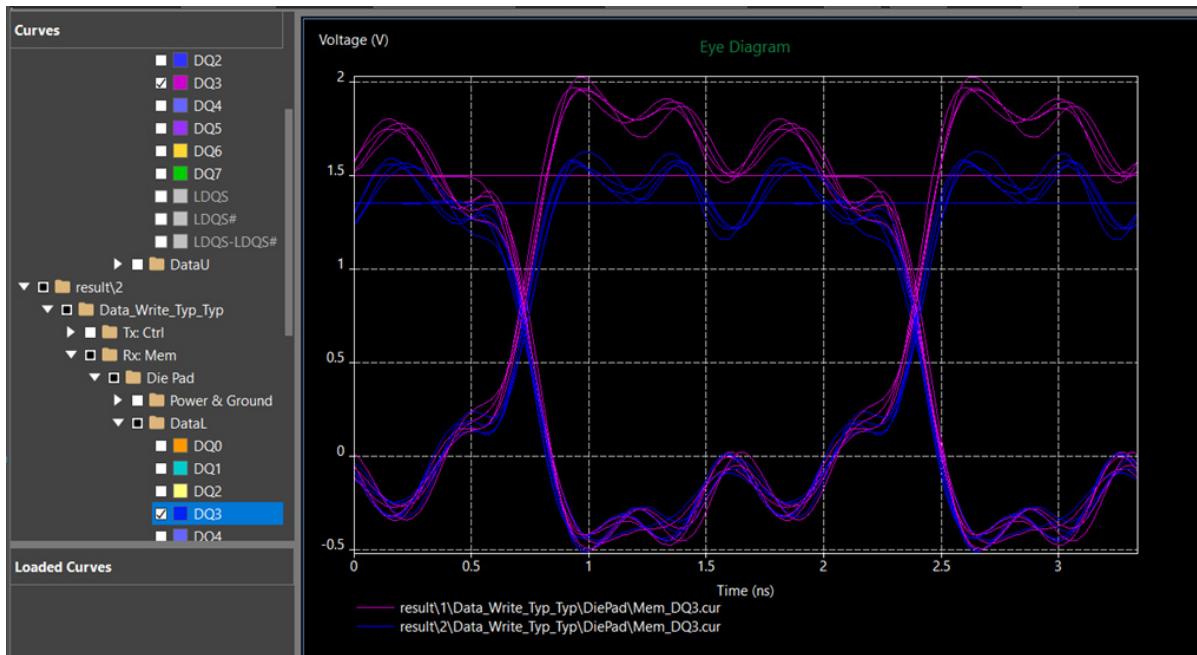


Note: Select the check box adjacent to *Power & Ground* to view the waveforms of the power and ground signals also. As can be seen, the power net has ripples that indicates PDN is considered in the simulation.

Topology Workbench: Parallel Bus Analysis Tutorial

Running Simulations and Analyzing the Results

3. Compare the results of the non-ideal power simulation with that of the ideal power. To simplify the comparison, plot **only** the *DQ3* signal with Ideal Power (Magenta) and Non-ideal Power (Blue) in an Eye Diagram as shown below:



Analyze the Simulation Results

Once the required results are generated, you can correlate the results with standard measurements and specifications from JEDEC standards, such as DDR3 and DDR4. You can also generate a report based on the waveform results. These reports equip you with user-friendly data presentation and parsing, for unprecedented troubleshooting, all combined with the implicit accuracy that comes with unique simulation technology.

Let us now try to generate DDR measurement reports for the non-ideal power simulation that was run in the above section.

Prepare for DDR Measurement Reports

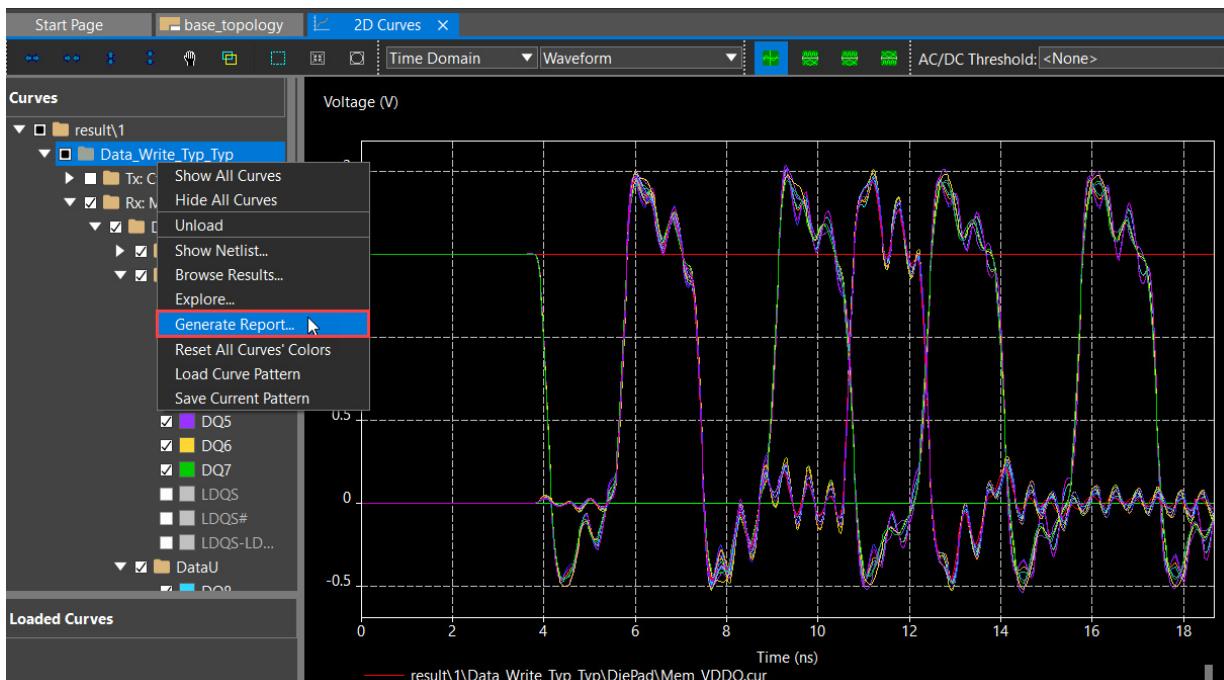
To start with DDR measurement reports,

1. Run the simulation for a topology in Topology Workbench. The *2D Curves* tab opens with the results.
2. Right-click a top-level node in the hierarchy displayed in the *Curves* pane to display the shortcut menu. A top-level node includes:

Topology Workbench: Parallel Bus Analysis Tutorial

Running Simulations and Analyzing the Results

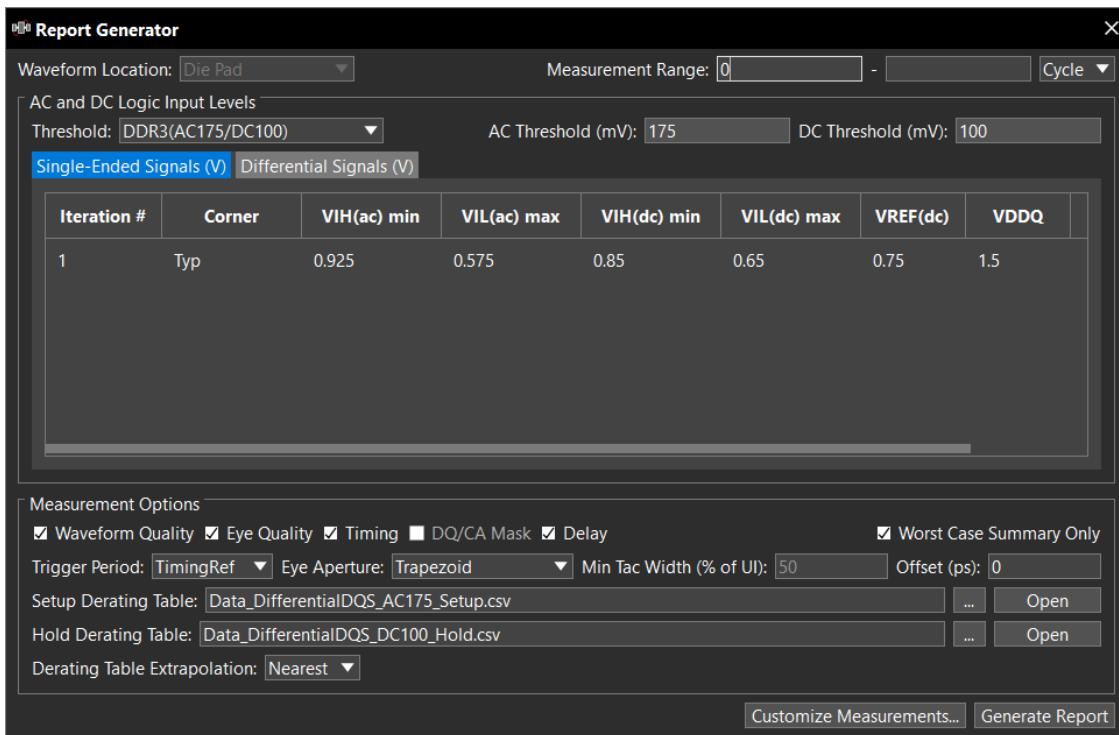
- ❑ The topmost node that shows the path to simulation result directory. Right-click this to view the overall simulation results.
- ❑ The second-level nodes that indicate the type of simulation. Right-click this to view the results for a specific simulation type.
- ❑ The third-level nodes that represent the simulated blocks. Right-click this to view the results for a specific block.



Topology Workbench: Parallel Bus Analysis Tutorial

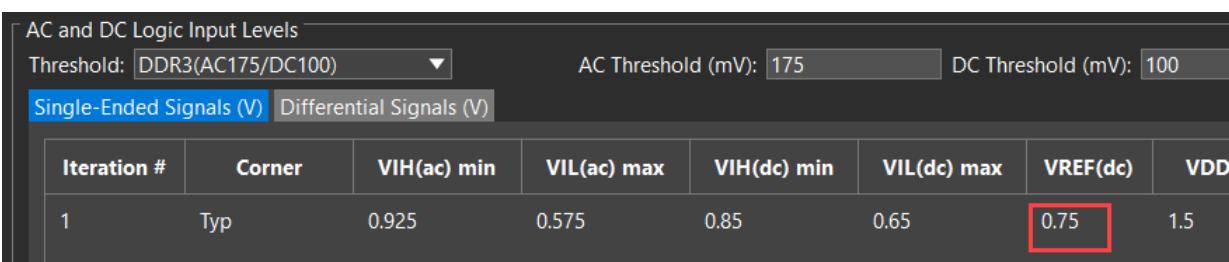
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3. Click *Generate Report* from the shortcut menu. The *Report Generator* dialog box opens.



The *Waveform Location* field displays that the output waveform uses *Die Pad* data.

4. Specify the start and end *Measurement Range* as 0 and 2 cycles.
5. Select *DDR3(AC175/DC100)* from the *Threshold* list box. The *AC Threshold* and *DC Threshold* values are displayed in read-only boxes.
6. On the *Single-Ended Signals (V)* tab, in the row for *Iteration # 1*, change the value under the *VREF(dc)* column from 0.675 to 0.75. This modifies the DC reference voltage value and the other voltage values in the table are recalculated accordingly.



7. Right-click the value for *VREF(dc)* to display the shortcut menu.

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8. Select *Default* from the shortcut menu. This helps to restore the default values of the modified row.

Single-Ended Signals (V)		Differential Signals (V)					
Iteration #	Corner	VIH(ac) min	VIL(ac) max	VIH(dc) min	VIL(dc) max	VREF(dc)	VDDQ
1	Typ	0.925	0.575	0.85	0.65	0.75	1.5

9. Select the following check boxes in the *Measurement Options* section: *Waveform Quality*, *Eye Quality*, *Timing*, *Delay*, and *Worst Case Summary Only*. Do not change the rest of the default settings.
10. Click *Generate Report*. The *Measurement Report* tab appears with detailed reports.

The screenshot shows the Cadence Topology Workbench interface with the 'Measurement...' tab selected. A new report titled 'Report1' is open. The report header reads 'DDR3 Measurement Report - Data Bus, 0.6Gbps, Write'. It includes a note that it was generated by Topology Workbench, Cadence Design Systems Inc., on Wednesday, 23 August 2023. Below the header is a 'Useful Links:' section with two items: 'Cadence website: <http://www.cadence.com>' and 'DDR3 SDRAM Specification: <http://www.jedec.org/sites/default/files/docs/JESD79-3E.pdf>'. The 'Table of Contents' section lists several sections: General Information, Simulation Setup (with sub-sections for Rank Definition, Model Selection and Stimulus, Controller, Memory, Signal Connectivity, and Simulation Description), DDR Measurement Setup (with sub-sections for AC and DC Logic Input Levels, Specs, Data Bus Write, Setup Derating Table, Hold Derating Table), and Results (with sub-sections for Data Bus Write, Waveform Quality Report, and Worst Case Summary).

Each report has a header section that displays the default title and subtitle, which can be edited in the dialog box accessed by clicking the *Customize Report* button in the *Generate Report* dialog box. The tool version and the date on which the report was

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generated are also listed in this section. The report also includes useful links to the Cadence website and a link to the DDRx specification.