

# **Topology Workbench: What's New in Release 23.1**

**Product Version 23.1**  
**October 2023**

---

© 2023 Cadence Design Systems, Inc.

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Open SystemC, Open SystemC Initiative, OSCI, SystemC, and SystemC Initiative are trademarks or registered trademarks of Open SystemC Initiative, Inc. in the United States and other countries and are used with permission.

**Trademarks:** Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522. All other trademarks are the property of their respective holders.

**Restricted Permission:** This publication is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this publication, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this publication subject to the following conditions:

1. The publication may be used only in accordance with a written agreement between Cadence and its customer.
2. The publication may not be modified in any way.
3. Any authorized copy of the publication or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
4. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

**Disclaimer:** Information in this publication is subject to change without notice and does not represent a commitment on the part of Cadence. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information.

Cadence is committed to using respectful language in our code and communications. We are also active in the removal and replacement of inappropriate language from existing content. This product documentation may however contain material that is no longer considered appropriate but still reflects long-standing industry terminology. Such content will be addressed at a time when the related software can be updated without end-user impact.

**Restricted Rights:** Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor

---

# Contents

---

|   |    |
|---|----|
| <u>Topology Workbench: What's New in 23.1</u>                                     | 5  |
| <u>Common Updates</u>   | 5  |
| <u>Floating Toolbar Replaces the Add Block Panel and Features New Block Icons</u> | 5  |
| <u>SystemSI Updates</u>   | 7  |
| <u>Eye Mask Support Added to 3D Eye Density Plots</u>                             | 7  |
| <u>USB4 Gen 4 Compliance Kit Supported</u>  | 7  |
| <u>Import CSV Data into Waveform Display</u>                                      | 9  |
| <u>Optimality Interface Enhanced to Generate a Report</u>                         | 10 |
| <u>SystemPI Updates</u>   | 11 |
| <u>Support Added for New VRM Models</u>   | 11 |

## Topology Workbench: What's New

---

---

# Topology Workbench: What's New in 23.1

---

This document describes the new features and enhancements introduced in Cadence® Sigrity™ Topology Workbench in release 23.1.

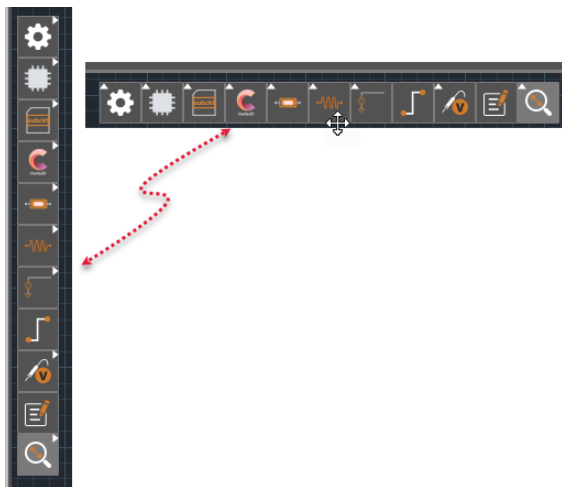
- Common Updates
- SystemSI Updates
- SystemPI Updates

For bug fixes and improvements in Allegro PCB SI in release 23.1, see *README\_CCR.txt* in the *OrCAD/Allegro 23.1 (SPB231)* page at [downloads.cadence.com](https://downloads.cadence.com).

## Common Updates

### Floating Toolbar Replaces the Add Block Panel and Features New Block Icons

In this release, the Add Block panel has been removed. Instead, a new floating toolbar is available in the main application window with controls to help with various design operations on the canvas. It is by default aligned vertically and can be docked horizontally per convenience.

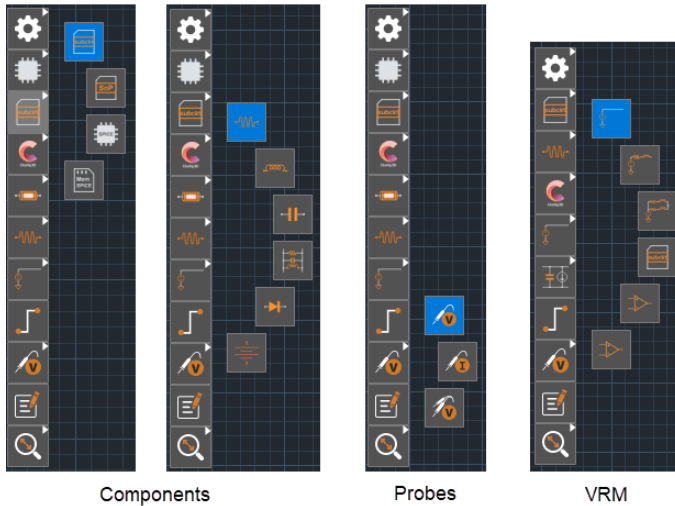


## Topology Workbench: What's New

### Topology Workbench: What's New in 23.1

---

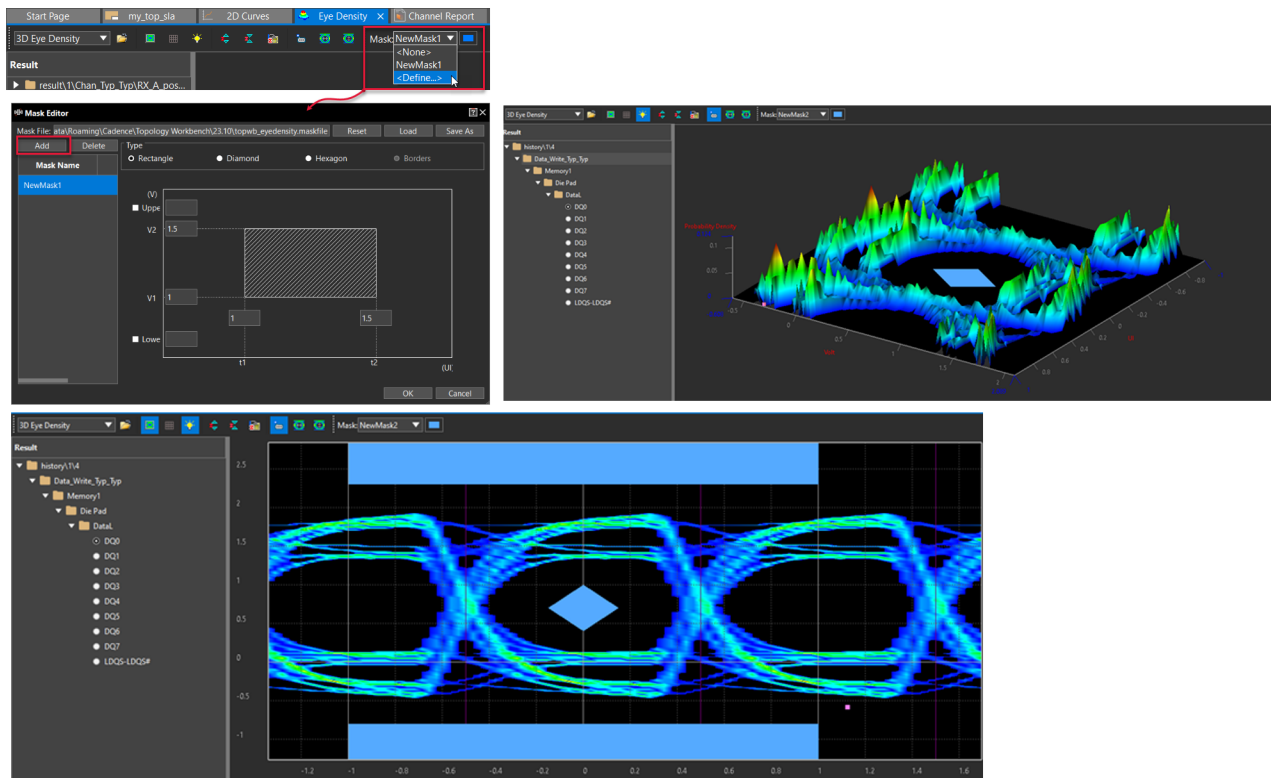
The floating toolbar features improved icons for placing blocks on the canvas. Only a subset of icons is visible at a time. To explore the additional blocks that can be added to the canvas, right-click any of the icons in the floating toolbar.



## SystemSI Updates

### Eye Mask Support Added to 3D Eye Density Plots

On completion of a channel simulation run in the Parallel Bus Analysis (PBA) or Serial Link Analysis (SLA) workflow, you can now define and apply eye mask values to the 3D plots in the Eye Density tab.



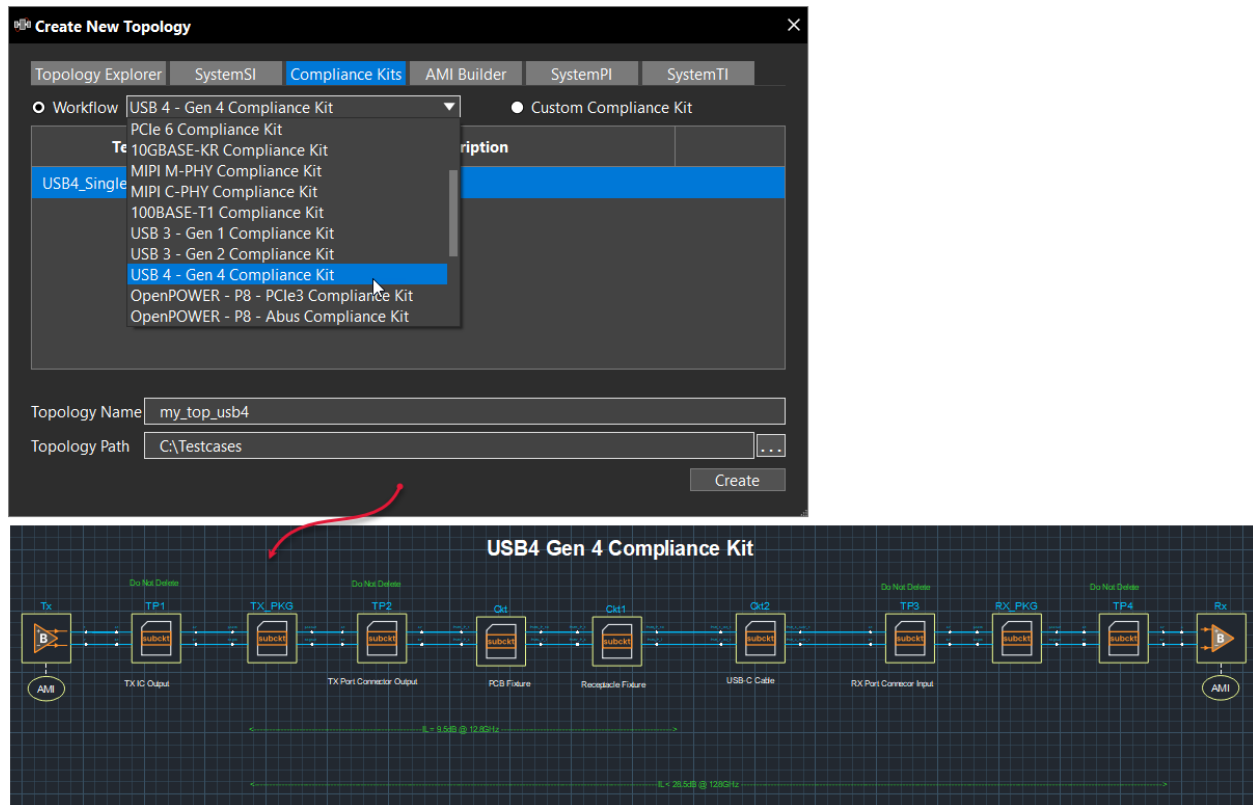
### USB4 Gen 4 Compliance Kit Supported

The Compliance Kits workflow now supports USB 4 - Gen 4 Compliance Kit. With this enhancement, you can run PAM3 simulation at a defined Baud Rate for a single lane topology comprising Tx, Rx, Tx and Rx Port Connectors, PKG, Cable, and fixtures. Except for a few

## Topology Workbench: What's New

### Topology Workbench: What's New in 23.1

components labeled as *Do Not Delete* in this sample topology, you can replace workspace items in the single-lane topology with your own design models.



The related compliance items include the transmitter and receiver tests for parameters such as:

- Tx level, Tx differential return loss, and Tx signal to noise distortion ratio (SNDR) (Section 3.2.3.4)
- Rx end-to-end channel differential insertion loss, Rx differential return loss, and Rx tolerance test (Section 3.2.4.2)

A compliance report is generated on completion of the checks.

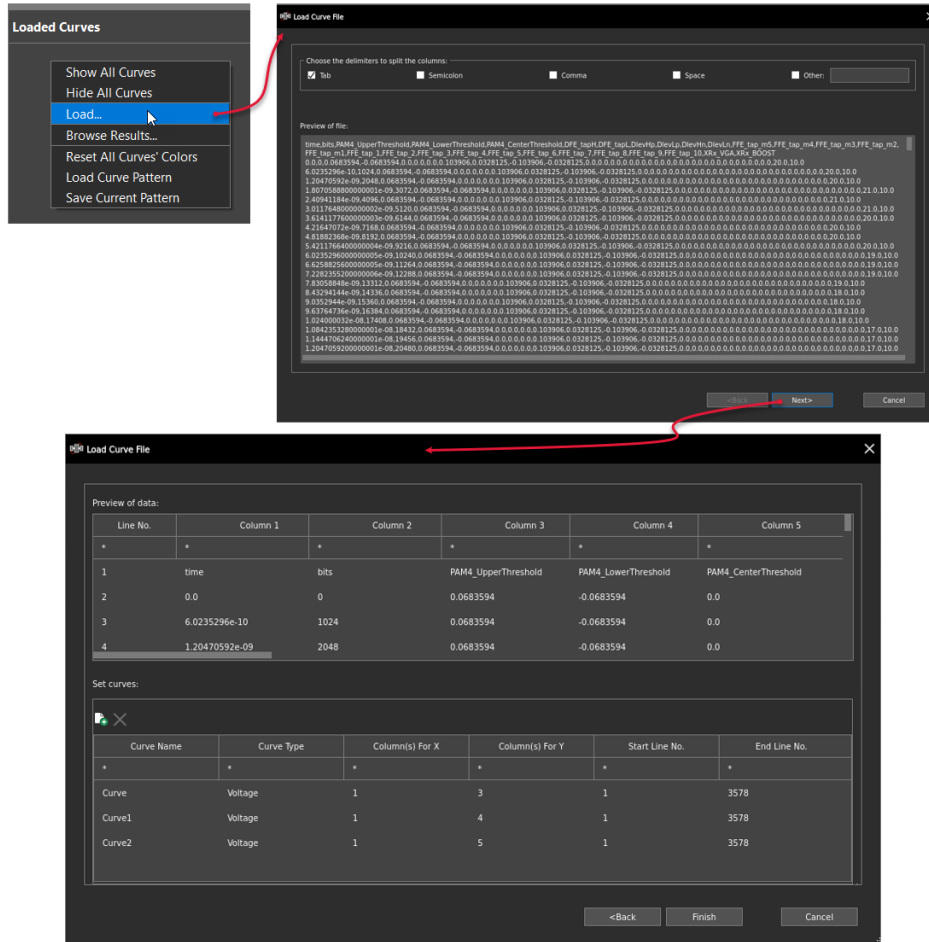


# Topology Workbench: What's New

## Topology Workbench: What's New in 23.1

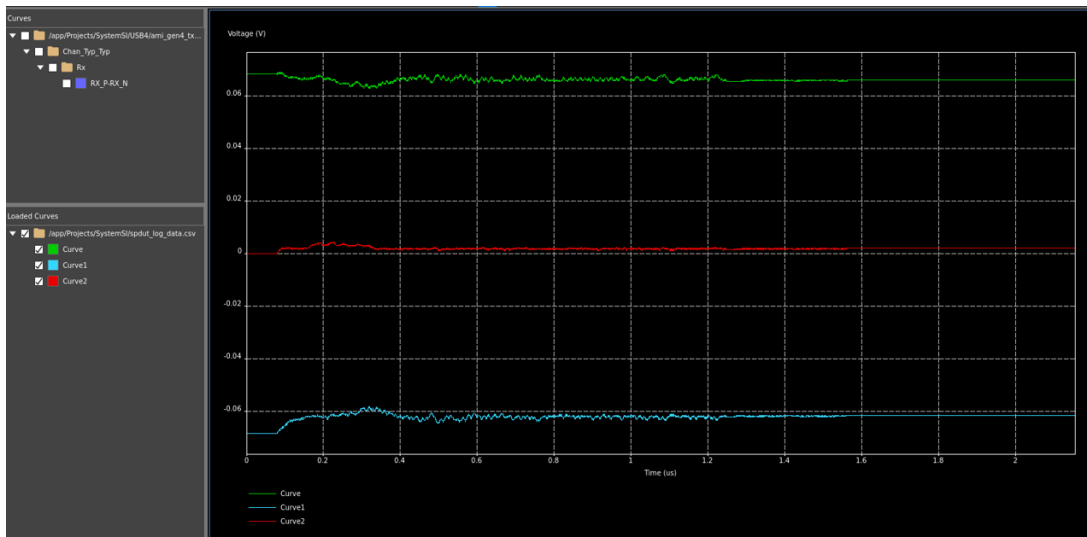
### Import CSV Data into Waveform Display

Some AMI models write data to a CSV file for post-processing and analysis. This data can now be imported and displayed in the 2D Curves tab with the simulation results.



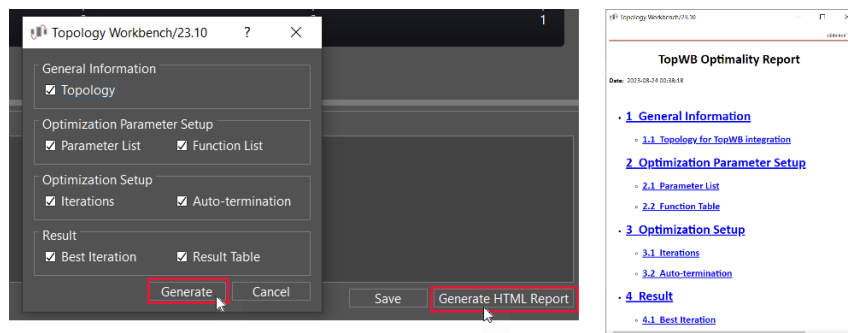
# Topology Workbench: What's New

## Topology Workbench: What's New in 23.1



## Optimality Interface Enhanced to Generate a Report

In this release, the *Generate HTML Report* button has been added to the Optimality window for Topology Workbench. Clicking this button opens a dialog box where you can configure the contents of the report and generate the Topology Workbench Optimality Report.



### 2 Optimization Parameter Setup

#### 2.1 Parameter List

| Index | Optimize | Name    | Type       | Expression | Ref Value | Unit | BoundType | LowBound | HighBound | Step | Array |
|-------|----------|---------|------------|------------|-----------|------|-----------|----------|-----------|------|-------|
| 1     | True     | Trace_W | continuous | 1mm        | 1         | mm   | relative  | 1        | 2         |      |       |
| 2     | False    | Trace_R | continuous | 2mm        | 2         | mm   | relative  |          |           |      |       |

#### [Return to Top](#)

#### 2.2 Function table

| Name | Mode       | Expression | Custom Function | Type                     | Index1 | Index2 | Target |
|------|------------|------------|-----------------|--------------------------|--------|--------|--------|
| obj  |            | E12        |                 | Objective Function(goal) |        |        |        |
| E12  | single_end |            |                 | Average                  | 1      | 2      |        |

### 4 Result

#### 4.1 Best Iteration

Best Iteration: 5

#### [Return to Top](#)

#### 4.2 Result Table

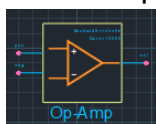
| Index | obj      | E12      | Trace_W  |
|-------|----------|----------|----------|
| 0     | 0.999261 | 0.999261 | 1.23412  |
| 1     | 0.978154 | 0.978151 | 1.54421  |
| 2     | 0.951231 | 0.951231 | 1.1325   |
| 3     | 0.983121 | 0.983121 | 1.32489  |
| 4     | 0.977281 | 0.977281 | 1.525494 |
| 5     | 0.923211 | 0.923211 | 1.85421  |

## SystemPI Updates

### Support Added for New VRM Models

The following two operational amplifier (Op-Amp) blocks have been added to model voltage regulator modules (VRM) more accurately:

- **Ideal Op-Amp**, which is a model with a simple voltage-controlled voltage source (VCVS) with an input impedance resistor and output impedance resistor.



| Name             | Value   |
|------------------|---------|
| Block Name       | Op-Amp  |
| Input Impedance  | 1e7Ohm  |
| Gain             | 10000   |
| Output Impedance | 0.1 Ohm |

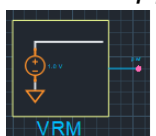
- **Bandwidth-Limited Op-Amp**, which is a model with an ideal op-amp with a bandwidth limit.



| Name             | Value   |     |
|------------------|---------|-----|
| Block Name       | Op-Amp1 | V   |
| Input Impedance  | 2e6Ohm  |     |
| Gain             | 2e5     | NEW |
| Bandwidth        | 1e6Hz   | NEW |
| Output Impedance | 0.1 Ohm |     |

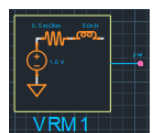
In addition, the following VRM blocks have been updated:

- **Ideal Supply (VDC) VRM**, which is a simple DC model.



| Name                | Value |
|---------------------|-------|
| Block Name          | VRM   |
| Nominal Voltage     | 1.0 V |
| ▼ Power Net         |       |
| Net Name            | PWR   |
| # of Pins           | 1     |
| Pin Name            | pwr   |
| Pin Resistance(Ohm) | 0     |
| ► Ground Net        |       |

- **RL VRM**, which is a 2-element model with a VDC source with a series resistor (R) and an inductor (L).



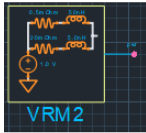
| Name            | Value |
|-----------------|-------|
| Block Name      | VRM1  |
| Nominal Voltage | 1.0 V |
| ▼ Power Net     |       |
| Net Name        | PWR   |
| # of Pins       | 1     |
| Pin Name        | pwr   |
| R_VRM(Ohm)      | 0.5m  |
| L_VRM(H)        | 50n   |
| ► Ground Net    |       |

## Topology Workbench: What's New

### Topology Workbench: What's New in 23.1

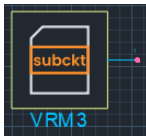
---

- ***RL//RL VRM***, which is a 4-element model with a VDC source with a parallel combination of the series resistor and inductor as in the 2-element model.



| Name            | Value |
|-----------------|-------|
| Block Name      | VRM2  |
| Nominal Voltage | 1.0 V |
| ▼ Power Net     |       |
| Net Name        | PWR   |
| # of Pins       | 1     |
| Pin Name        | pwr   |
| R_VRM(Ohm)      | 0.5m  |
| L_VRM(H)        | 50n   |
| R_damp(Ohm)     | 20m   |
| L_VRM/10(H)     | 5.0n  |
| ► Ground Net    |       |

- ***Subckt VRM***, which is a subcircuit model based on a user-supplied netlist model for a VRM model.



| Name         | Value        |
|--------------|--------------|
| Block Name   | VRM3         |
| Circuit File | vrn_Smith.sp |