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Working with Altera On-Chip Termination

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Contents

Preface

This document describes how to use on-chip termination (OCT) in Allegro® FPGA System Planner (FSP).

The document provides the conceptual and procedural information necessary while working with the OCT feature in FSP. This application note does not cover OCT and associated I/O DRC riles. It is assumed that you are familiar with the basic OCT and I/O DRC rules. For detailed information, see the Xilinx's handbook for the respective FPGAs.

Introduction to the On-Chip Termination

On-Chip Termination (OCT) helps improve signal integrity by matching impedance, and at the same time, lower design cost by eliminating the need for external resistors, reducing the PCB size, and by simplifying PCB layout. Cadence FPGA System Planner (FSP) provides a flexible use model that you can use to design your boards using the FPGA OCT features. It provides you with greater control for choosing the pins/ports on which OCT is to be applied, the type of OCT to be applied, and the RZQ pins that need to be preserved for OCT calibration.

This application note describes the following:

- Method for setting OCTs and OCT sharing when working with Altera devices in FSP
- Exchanging OCT related settings between FSP and Altera Quartus® II
- Rational behind the use model, limitations, and constraints associated with this methodo and the steps to troubleshoot issues.

FSP Flow

This section describes the steps to be followed to create a design with OCTs using FSP.

Specifying OCT the Interfaces, Protocols, or Virtual Interfaces

On all the interfaces, protocols, and virtual interfaces that are targeted to FPGA components with OCT support, you are allowed to specify the desired OCT values against the pins/ports.

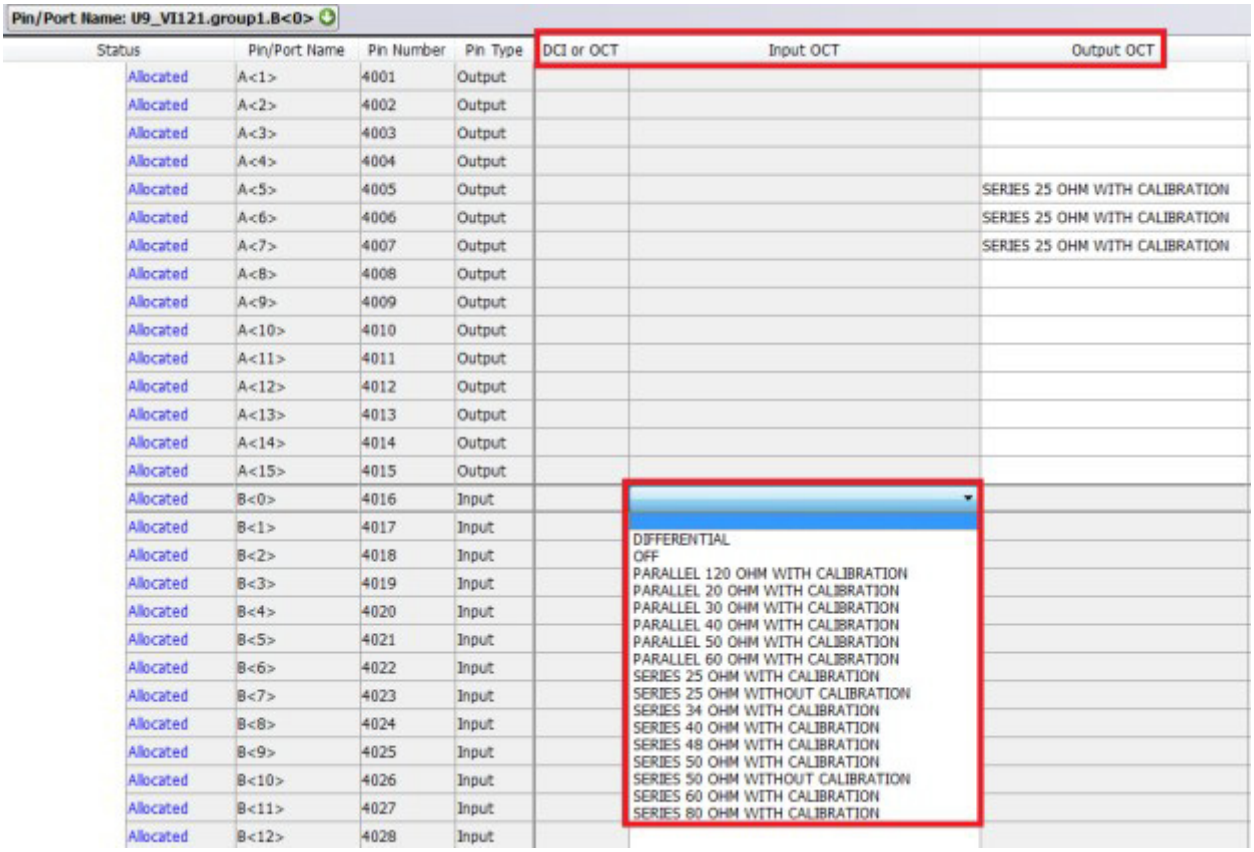
Note: Required OCT setting is captured at the originating pin/port of a net connecting to FPGA, not the FPGA pin itself. This use model helps you retain the OCT settings as you go through successive FSP synthesis iterations.

As the first step, you need to go to the originating pins/port and select the preferred OCT to be applied. FSP has three columns related to OCT settings, DCI or OCT, Input OCT, and Output OCT for each originating pin/port on the Design Connectivity Window shown in the figure below.

DCI or OCT column: Use this column to select the desired OCT setting for the families which do not support dynamic OCT (e.g. Stratix II)

Input OCT and Output OCT columns: Use this column to select the desired OCT setting for families that support dynamic OCT (e.g, Stratix V). Based on the signal direction, either, or both of the columns are enabled.

- For input pins/ports (to be connected to FPGA output or bidirectional pins), the Output OCT column is enabled.
- For output pins/ports (to be connected to FPGA input or bidirectional pins), the Input OCT column is enabled.
- For bidirectional pins/ports, both the Input OCT and the Output OCT columns are enabled allowing you to simultaneously define the input and output OCTs.



Note: FSP displays the complete list of OCT values in the selection list. It does not filter or present only supported OCT values for a given FPGA part (and pin type). This is as designed as Altera support for OCT standards set for any part/family is subject to changes. You need to refer to the latest data book from Altera and Quartus II to specify the correct OCT values. The following table lists various termination types, and the supported devices and pin types at the time of writing this document.

Termination	Supported Devices	Pin Type
SERIES 25 OHM WITHOUT CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Output
SERIES 34 OHM WITHOUT CALIBRATION	Stratix V, Arria V GZ	Output
SERIES 34.3 OHM WITHOUT CALIBRATION	Stratix V, Arria V GZ	Output

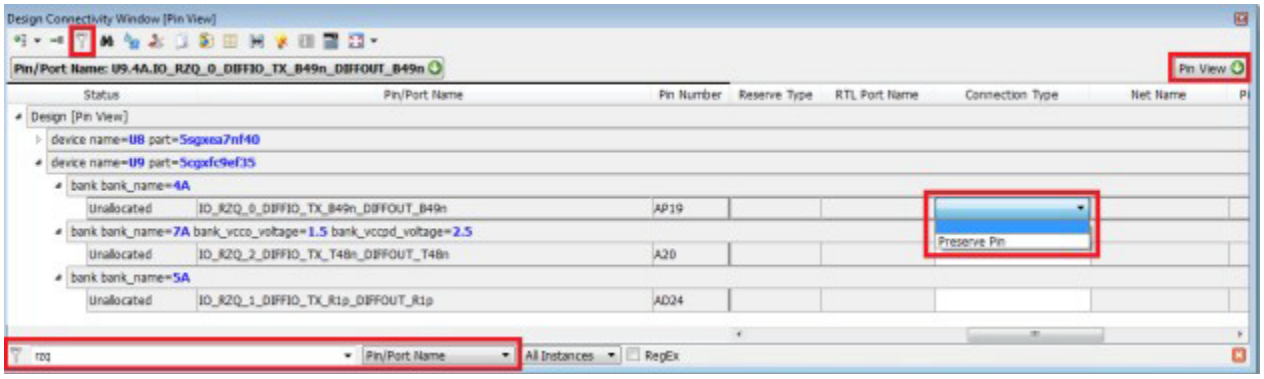
SERIES 40 OHM WITHOUT CALIBRATION	Stratix V, Arria V GZ	Output
SERIES 48 OHM WITHOUT CALIBRATION	Stratix V, Arria V GZ	Output
SERIES 50 OHM WITHOUT CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Output
SERIES 60 OHM WITHOUT CALIBRATION	Stratix V, Arria V GZ	Output
SERIES 80 OHM WITHOUT CALIBRATION	Stratix V, Arria V GZ	Output
SERIES 240 OHM WITHOUT CALIBRATION	Stratix V, Arria V GZ	Output
SERIES 25 OHM WITH CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Output
SERIES 34 OHM WITH CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Output
SERIES 40 OHM WITH CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Output
SERIES 48 OHM WITH CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Output
SERIES 50 OHM WITH CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Output
SERIES 60 OHM WITH CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Output
SERIES 80 OHM WITH CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Output
SERIES 240 OHM WITH CALIBRATION	Stratix V	Output
PARALLEL 20 OHM WITH CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Input
PARALLEL 30 OHM WITH CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Input
PARALLEL 40 OHM WITH CALIBRATION	Stratix V, Arria V, Arria V GZ, Cyclone V	Input

`PARALLEL 50 OHM WITH CALIBRATION`	Stratix V, Arria V, Arria V GZ, Cyclone V	Input
`PARALLEL 60 OHM WITH CALIBRATION`	Stratix V, Arria V, Arria V GZ, Cyclone V	Input
`PARALLEL 120 OHM WITH CALIBRATION`	Stratix V, Arria V, Arria V GZ, Cyclone V	Input
`DIFFERENTIAL`	Stratix V, Arria V, Arria V GZ, Cyclone V	Input

Preserve the required RZQ pins on device

In the latest release, FSP supports OCT sharing, which means that signals using OCT can be targeted to any bank in the device, not just the banks with RZQ pins. This is applicable to FPGA families that support OCT sharing.

Depending on the number of RZQ pins that are required to calibrate the OCTs, you need to preserve the required RZQ pins on the device from Pin View of the Design Connectivity Window as shown in the following figure. By preserving these pins, you can ensure that FSP does not assign these pins to any other pins/ports.



Synthesize the design

After the OCTs are specified and the appropriate RZQ pins are preserved, run the FSP synthesis to make connections based on defined constraints. FSP does a limited IO DRC check with respect to OCTs. The IO DRCs that are checked and not checked by FSP are listed below.

DRCs that are checked:

- The VCCO voltages are set for the bank based on the OCT calibration requirement and the IO standard.

DRCs that are not checked:

- Compatibility of the specified OCTs against the IO standards, direction and other OCTs in the bank
- Rules for OCT sharing

Note: FSP disables editing OCT settings after making connections (as a result of the synthesis run). This is to prevent users from selecting an incorrect or incompatible OCT standard from an IO DRC perspective.

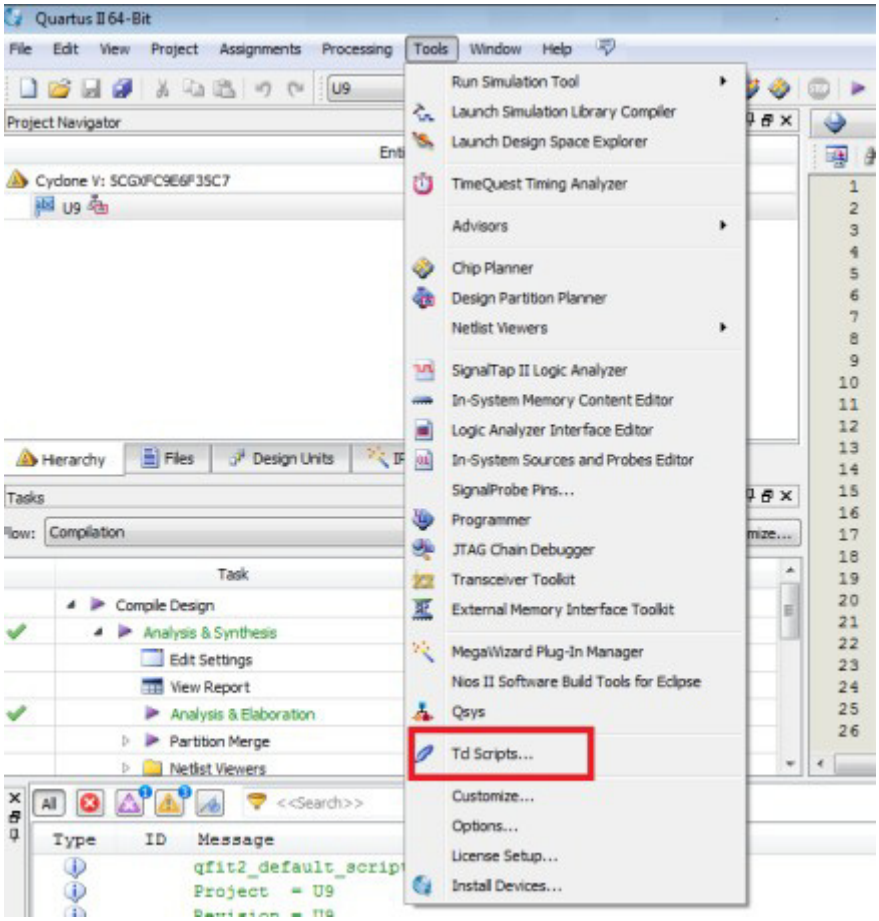
Exporting Constraints

After the FSP synthesis is done, you can export the constraints that contain information related to pin assignments, IO Standards, group assignments, allocated banks and terminations. These constraints are generated in the form of a Tcl file. Excerpts from the exported file are shown in the following figure to depict the kind of information that is depicted through these constraints.

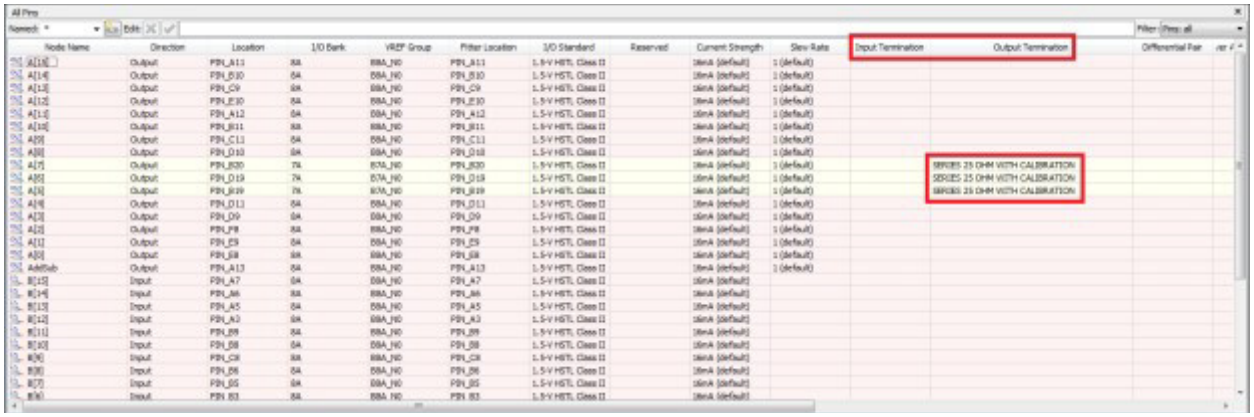
```
set_global_assignment -name DEVICE 5CGXFC9E6F35C7
set_global_assignment -name FAMILY "Cyclone V"

############## IOSTANDARD - NET ##################

set_instance_assignment -name IO_STANDARD "1.5-V HSTL Class II"                  -to  A[0]
set_instance_assignment -name IO_STANDARD "1.5-V HSTL Class II"                  -to  A[1]
set_instance_assignment -name IO_STANDARD "1.5-V HSTL Class II"                  -to  A[2]
set_instance_assignment -name IO_STANDARD "1.5-V HSTL Class II"                  -to  A[3]
set_instance_assignment -name IO_STANDARD "1.5-V HSTL Class II"                  -to  A[4]
set_instance_assignment -name IO_STANDARD "1.5-V HSTL Class II"                  -to  A[5]

############## LOCATION - NET ##################

set_location_assignment PIN_E8         -to    A[0]                      -comment "Bank : 8A"
set_location_assignment PIN_E9         -to    A[1]                      -comment "Bank : 8A"
set_location_assignment PIN_F8         -to    A[2]                      -comment "Bank : 8A"
set_location_assignment PIN_D9         -to    A[3]                      -comment "Bank : 8A"
set_location_assignment PIN_D11        -to    A[4]                      -comment "Bank : 8A"
set_location_assignment PIN_B19        -to    A[5]                      -comment "Bank : 7A"

############## TERMINATIONS - NET ##################

set_instance_assignment -name OUTPUT_TERMINATION "SERIES 25 OHM WITH CALIBRATION"        -to   A[5]
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 25 OHM WITH CALIBRATION"        -to   A[6]
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 25 OHM WITH CALIBRATION"        -to   A[7]

############## GROUP INFO ##################

set_global_assignment -name ASSIGNMENT_GROUP_MEMBER  "A[0]"                      -section_id    U9_VI121_group1
set_global_assignment -name ASSIGNMENT_GROUP_MEMBER  "A[1]"                      -section_id    U9_VI121_group1
set_global_assignment -name ASSIGNMENT_GROUP_MEMBER  "A[2]"                      -section_id    U9_VI121_group1
set_global_assignment -name ASSIGNMENT_GROUP_MEMBER  "A[3]"                      -section_id    U9_VI121_group1
set_global_assignment -name ASSIGNMENT_GROUP_MEMBER  "A[4]"                      -section_id    U9_VI121_group1
set_global_assignment -name ASSIGNMENT_GROUP_MEMBER  "A[5]"                      -section_id    U9_VI121_group1
```

Importing Constraints in Quartus

Import the constraints exported from FSP into your Quartus® II project by executing the Tcl script as shown in the following figure.



The imported OCT values are reflected in the Quartus® II Pin Planner as shown in the following figure.



Configure RZQ pins for OCT Calibration and Sharing

If you specified any OCTs that required calibration, you need to calibrate them using the appropriate calibration blocks. If your device supports OCT sharing (for example, Cyclone V, Stratix V or Arria V), you can use any RZQ pin in the device to calibrate all the OCTs of I/O banks with I/O standards that use the same VCCIO supply voltage. To calibrate the series- and parallel-calibrated terminations, connect the RZQ pin to GND through an external 100? or 240? resistor (depending on the Rs or RT OCT value). The RZQ pin shares the same VCCIO supply voltage with the I/O bank where the pin is located.

Run the IO Assignment Analysis in Quartus® II to check if there are any violations in the assignments. If you made any incorrect OCT assignments in FSP, they are flagged as errors. You can go back to FSP, correct the OCT assignments, re-export the constraints file and update your Quartus® II project. Alternately, you can alter the OCT assignments directly in Quartus® II. It is recommended to that you import the changes you made to OCT settings in Quartus® II back into FSP. This helps you avoid making the same changes in Quartus® II as you go through FSP- Quartus® II-FSP iterations. To learn how to import constraints back into FSP, refer to the application notes on mapping FPGA port mapping and export/import constraints.

Summary

FSP provides a flexible architecture to design boards with FPGAs using the OCT feature. This document outlined the FSP method to be followed when using OCTs and OCT sharing on Altera devices, the limitations of this method and how they can be overcome.