

# **Allegro® X System Capture Frequently Asked Questions**

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# Contents

---

<a href="#">What are the rules for naming Allegro X System Capture objects?</a>	8
<a href="#">How do I check which cds.lib is being read?</a>	8
<a href="#">How do I check which libraries are getting picked in my project?</a>	9
<a href="#">How do I add a local library to a project?</a>	10
<a href="#">I cannot see the libraries that are in the site cpm. Why is that?</a>	11
<a href="#">Can I configure the search order for the included libraries?</a>	11
<a href="#">How do I connect a bus to multiple pins?</a>	12
<a href="#">How do I launch Constraint Manager from Allegro X System Capture?</a>	13
<a href="#">Why is the Special Symbols panel empty?</a>	14
<a href="#">How do I add new symbols to the Special Symbols bucket?</a>	15
<a href="#">How can I control the Special Symbols panel at the site level?</a>	16
<a href="#">How do I modify properties of parts?</a>	16
<a href="#">Can I display all the net names on a page?</a>	17
<a href="#">Why do components get selected despite being disabled in the Selection Filter?</a>	17
<a href="#">Can I select or unselect objects using shortcuts?</a>	18
<a href="#">How do I set the custom pattern for auto creation of differential pairs?</a>	18
<a href="#">Can I extract the Topology for a Differential Pair from the canvas?</a>	19
<a href="#">How do I change the XNet name in Docked Constraint Manager?</a>	20
<a href="#">Can I configure the customizations of System Capture if I do not have a site?</a>	21
<a href="#">How do I change the page size in the same project?</a>	21
<a href="#">Do I need to use Part Developer to edit parts in System Capture?</a>	22
<a href="#">Where can I access materials on library development with System Capture?</a>	22
<a href="#">How do I change the grid settings?</a>	23
<a href="#">Can I Change the Grid units from Inches to Millimeters?</a>	23
<a href="#">Can I use a PSpice library in inches with designs in mm?</a>	24
<a href="#">What is a base net? How do I make a net the base net?</a>	25
<a href="#">How does System Capture determine the base net when a net is aliased?</a>	27
<a href="#">How can I highlight an entire net on a page? All segments?</a>	27
<a href="#">Why don't I see the unconnected pin symbol for Power and GND symbols?</a>	28
<a href="#">Why are the design rules not checked automatically?</a>	28
<a href="#">Where are the values set for DRCs?</a>	29
<a href="#">Can I see multiple pages of the design on different screens?</a>	30

## Allegro X System Capture: Frequently Asked Questions

---

<u>Where can I learn about variants and BOM in System Capture?</u>	30
<u>How do I use strokes in System Capture like in DE-HDL?</u>	30
<u>Why is worklib missing from my project when cds.lib has a worklib entry?</u>	30
<u>Can I configure where the packaging files get generated?</u>	30
<u>Can I configure where the physical layout files get generated?</u>	31
<u>How do I specify where the BOM reports should be saved?</u>	31
<u>Why are the netlisting files (pst*.dat) missing from the packaged folder?</u>	31
<u>I am getting errors for Physical Net Name conflicts when running the back-to-front flow. Is there a command I can use to fix this?</u>	31
<u>The Auto Shapes panel does not have the shapes I require. What can I do?</u>	32
<u>How are XNets created in System Capture?</u>	32
<u>Can I lock the grid settings at the site-level?</u>	33
<u>When I paste components, the REF DES PATTERN and other related directives are not used. Why?</u>	34
<u>Where can I specify shortcuts?</u>	35
<u>Do the standard title blocks support custom variables and images?</u>	36
<u>Why is Part Manager grayed out in the Tools menu?</u>	36
<u>A Tk script for Tcl commands is making System Capture unresponsive. How can I run it in the background?</u>	37
<u>The cds.lib file for a new project had CONCEPT_INST_DIR and not CDS_SITE. Why?</u>	37
<u>Can I lock the project type for all new projects?</u>	37
<u>If I want to use a sheet that is not recognized by System Capture, what changes do I need to do in the setup?</u>	38
<u>Can I make a copy of a project?</u>	39
<u>Can I stop extra folders from getting copied when I make a copy of a project?</u>	39
<u>How does PCB Editor process the bypass pin distance from parent that is set in System Capture?</u>	40
<u>What happens when I set the Distance to zero for bypass distance capacitors?</u>	40
<u>The default RefDes continuity has changed from left-to-right to top-to-bottom. How do I revert this?</u>	40
<u>How does REF DES PATTERN counter work with unique phys des prefix?</u>	41
<u>How do I change the currently used license in System Capture?</u>	41
<u>How do I globally unset all user-assigned references?</u>	42
<u>How does System Capture manage bus bits that get deleted from the schematic?</u>	42
<u>Why do connections break when replacing components?</u>	43
<u>Can I use an IP address of a server for the storing projects?</u>	43
<u>Why is Edit Properties showing an incorrect instance ID (spath) when I add a block?</u>	43

## Allegro X System Capture: Frequently Asked Questions

---

<u>Why am I unable to rename a scalar port to a vector port?</u>	43
<u>How is setting reuse_refdes to 'OFF' different in System Capture as compared to DE-HDL?</u>	44
<u>How do I ensure user-defined properties get passed to PCB Editor?</u>	44
<u>Why am I unable to generate a BOM or package my design?</u>	45
<u>Can I attach an interface port to power or ground nets?</u>	45
<u>Why are navigation links not working on imported blocks?</u>	46
<u>Which page opens when I use the Descend command for a block in a hierarchical design?</u>	46
<u>Can the Header Row be removed from Tables?</u>	46
<u>Why does 'Create Project based on DE-HDL design' stop working during desktop sharing or Web Ex?</u>	48
<u>How do I stop wires from being re-routed when moving components?</u>	48
<u>Why does Part Manager not report any packaging errors even if PPT files are missing?</u>	48
<u>I have parts with multiple symbols. I want the next symbol to be automatically picked after each place. Can I do that?</u>	49
<u>How do I see all the shortcuts that start with a letter?</u>	49
<u>How do I ensure that the libraries added to a project are available to imported blocks?</u>	51
<u>Can I import reuse blocks not in the root hierarchy of a design?</u>	51
<u>How is voltage for a power symbol picked?</u>	51
<u>Physical and Spacing Constraints from DE-HDL did not get imported. Why?</u>	52
<u>How do I dynamically zoom into an area?</u>	52
<u>How do I find out the page border symbol name?</u>	52
<u>How do I see the page name change in the page border as well as the open tab?</u>	53
<u>Why is the custom page border not showing the full grid?</u>	53
<u>How can I get Uncompressed Netlists in the Packaged folder?</u>	53
<u>Why am I seeing a Blank Symbol with no Pins and a Cross?</u>	54
<u>Can I use existing CAE Views HDL programs with System Capture?</u>	55
<u>Why can't I regenerate symbols for read-only blocks with unlocked symbols?</u>	55
<u>Is There a way to Build Custom Reports?</u>	55
<u>Can I build custom dialog boxes?</u>	57
<u>The TOC page number is no longer a roman number. Why?</u>	57
<u>Part Manager reported errors but Export to Physical Layout worked. Why?</u>	57
<u>Part Manager reports parts as not in sync for design imported from DE-HDL. Why?</u>	58
<u>Does System Capture support pins on Comment bodies?</u>	58
<u>Reset All is not clearing the XNet definitions even though the source is Schematic. Why?</u>	58

## Allegro X System Capture: Frequently Asked Questions

---

<u>In my design the bits of an XNet are under one bus in Constraint Manager. Why is the second bus empty?</u>	58
<u>I have created a new project based on an DE-HDL design. Can I change the XNet state migration in the new design?</u>	59
<u>How do I find a pin that has an overbar in its name?</u>	59
<u>Which application can I use to open PDFs in Linux?</u>	60
<u>Are the log files for importing blocks or sheets saved? If yes, where?</u>	61
<u>Can I export the notes in my design to an Excel file?</u>	61
<u>Can I customize menu options based on the selected license?</u>	61
<u>Why is there a cross on the symbol of an uninstantiated block?</u>	63
<u>I used the Replace command, but the Ref Des letter did not change. Why?</u>	63
<u>Ref Des does not follow the REF_DES_PATTERN directive in hierarchical designs. How to correct that?</u>	63
<u>Why does the Replace command open Find and Replace sometimes and not Unified Search?</u>	64
<u>Can I change the Text Editor that open for the Edit Externally command?</u>	64
<u>Is there any way to Export to PCB without running Part Manager?</u>	64
<u>Changing the symbol version removes the variant data. Is there a way to stop this?</u>	65
<u>How can I prevent display issues on 4K monitors?</u>	65
<u>How do I change the Pulse dashboard language to English?</u>	65
<u>How can I display Chinese characters in Unified Search when using Capture CIS flow in System Capture?</u>	66
<u>Can I run specific commands before and after an operation or command?</u>	66
<u>Why doesn't System Capture show a star on pages to indicate the unsaved changes?</u>	67
<u>Can I use DE-HDL property names in scripts in System Capture?</u>	67
<u>How can I prevent table column widths on PDFs from shrinking when printed on non-local displays?</u>	68

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# Frequently Asked Questions

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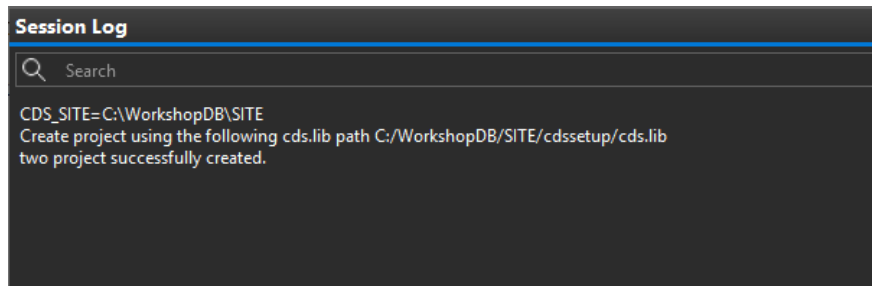
This document contains answers to the most frequently asked questions by customers when capturing about the *Allegro X System Capture* solution. This document is periodically updated to list the issues our customers face while working with Allegro X System Capture.

## What are the rules for naming Allegro X System Capture objects?

The rules for naming System Capture objects, such as projects, properties, and signals, is the same as that for Design Entry HDL (DE-HDL). Refer to the [\*Naming Rules and Conventions\*](#) section in the DE-HDL documentation. System Capture works with the correct by design philosophy and whenever an incorrect character is added for naming objects, it provides corrective messages immediately.

## How do I check which cds.lib is being read?

The cds.lib file contains the list of libraries that are available for use in the project. The cds.lib file used at the time of creating the project is mentioned in the Session Log. To open the session log, choose *View – Panels – Session*, and check the location of the cds.lib file is being read by the current project.

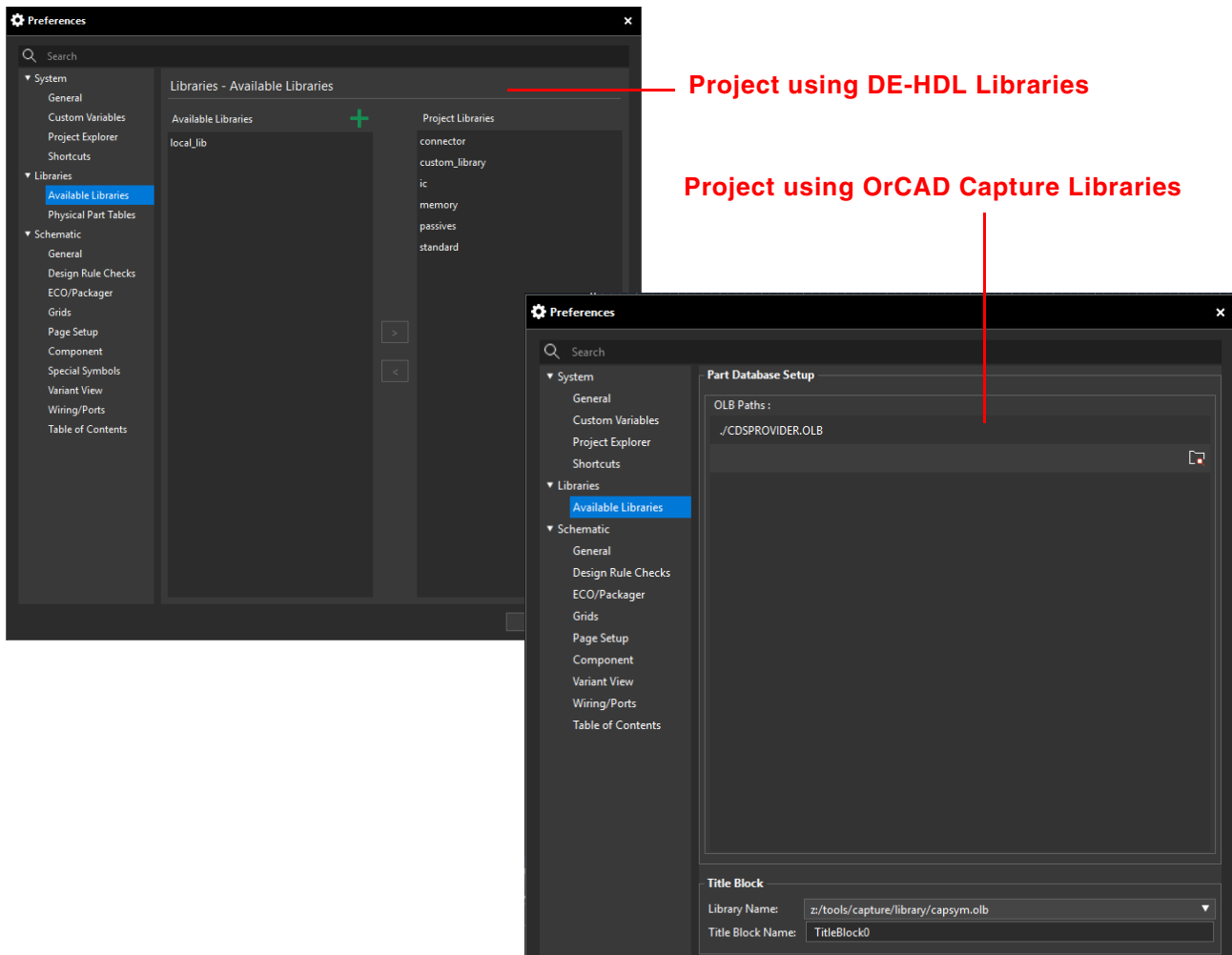




## How do I check which libraries are getting picked in my project?

To see which libraries have been added to the project:

1. Choose *Edit – Preferences*.
2. Open the *Libraries - Available Libraries* tab.



Depending on the project type, you will see a different layout for DE-HDL and OrCAD Capture libraries.

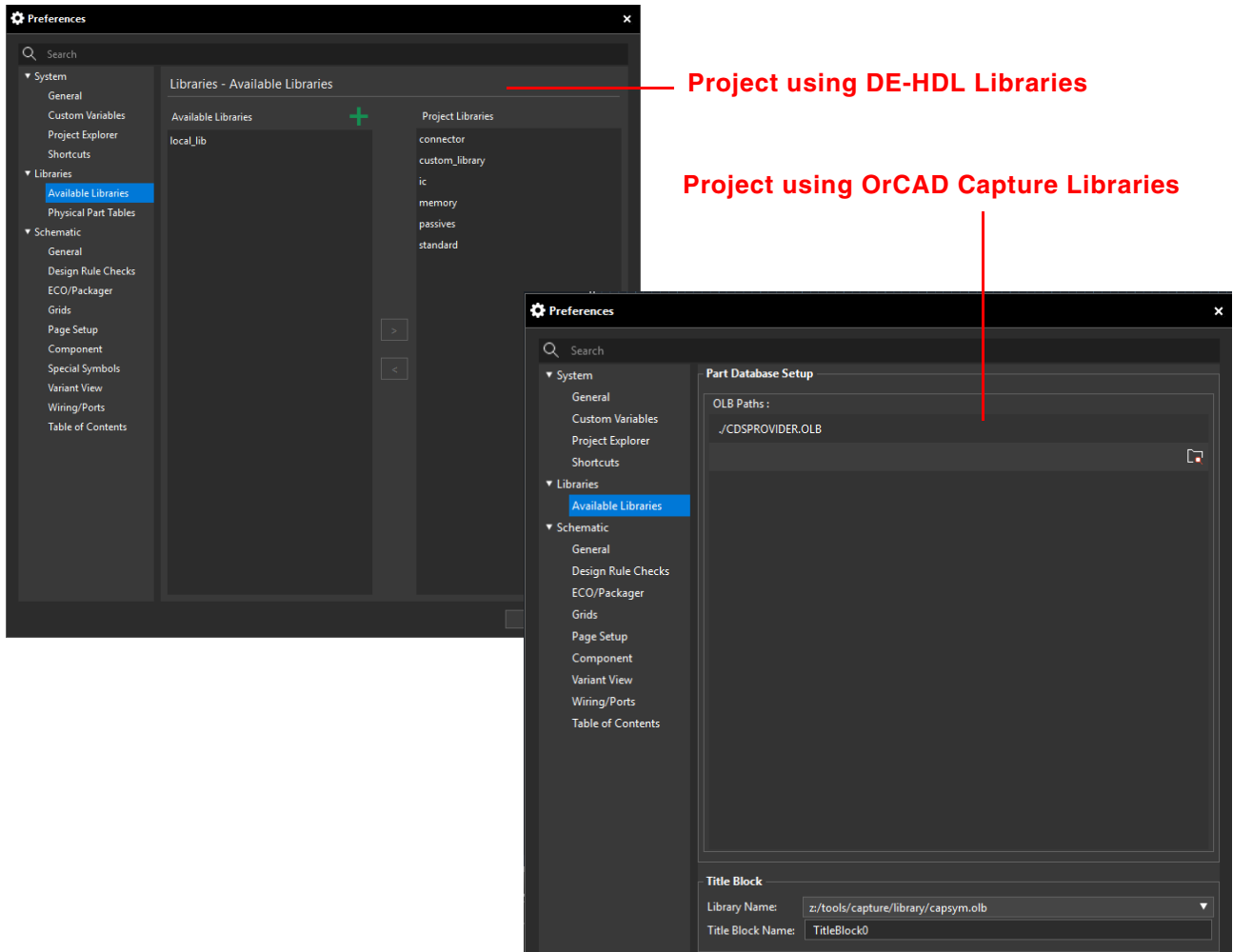
# Allegro X System Capture: Frequently Asked Questions



## Frequently Asked Questions

### How do I add a local library to a project?

To add libraries to an open project:

1. Choose *Edit – Preferences*.
2. Open the *Libraries - Available Libraries* tab.



3. Click the  or  button, depending on the library type.

4. Navigate to the folder that contains the library.

You can use Ctrl and Shift keys to select multiple folders simultaneously.

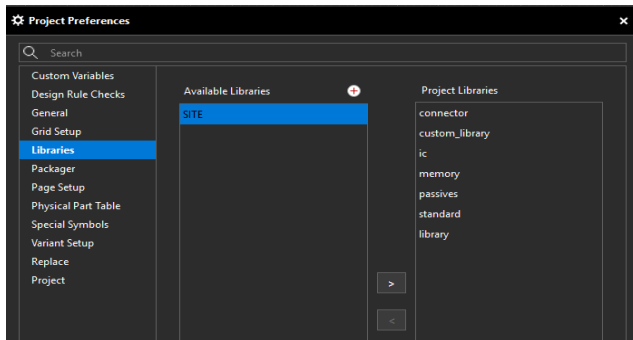
5. Add the libraries.

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

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6. Click  to add the library to the *Project Libraries*, for DE-HDL libraries.



7. Click *OK* to close the *Project Preferences* window.

You can now add components from the newly added library to your project.

## I cannot see the libraries that are in the site cpm. Why is that?

Check if the HOME location specified on your computer already has a cds.lib file. When any new project is created, System Capture looks for cds.lib in the following order:

Project -> Home -> Site -> Installation

So, if the site cpm is not getting read, there is probably a cds.lib in the HOME location. Rename or remove that cds.lib and then create a new project.

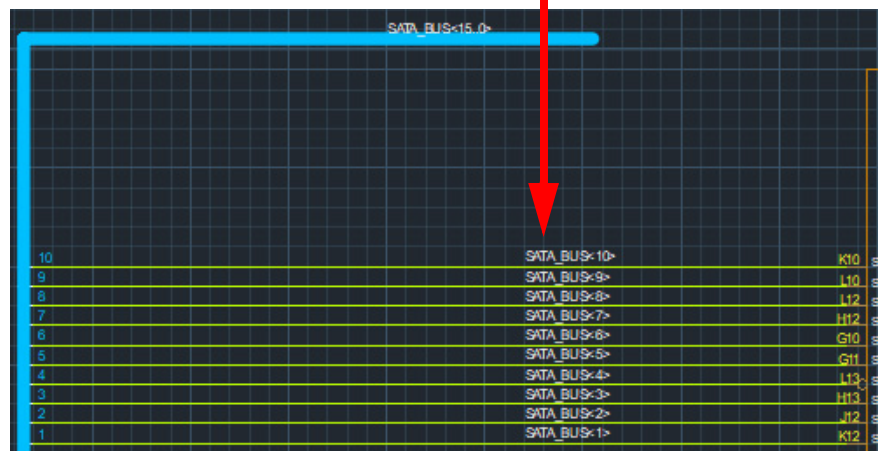
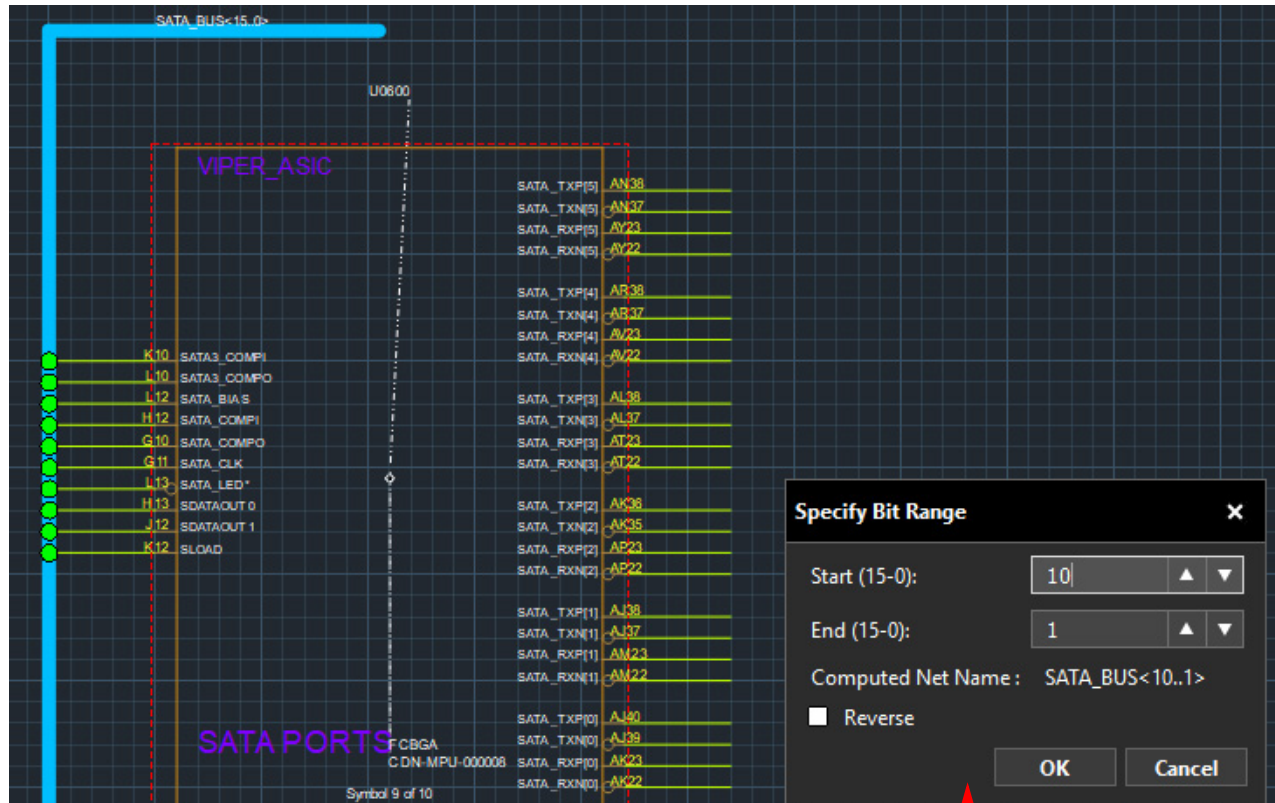
## Can I configure the search order for the included libraries?

You can configure to set the search order for the libraries. When the site is not set, System Capture picks the file in the installation and adds all the libraries available in that file. After setting the site variable and reopening the project, the settings remain same and you do not get the libraries by default. In case for this project you would like to add the libraries, you would need to do it manually by editing the cds.lib file and including the \$CDS\_SITE/cdssetup/cds.lib file. Next, you need to add the new libraries coming from the included file into the project. This needs to be done from the *Edit – Preferences – Library* tab. After this the libraries would be available for addition.

When you set the site and create a new project, the cds.lib file from the site area gets picked and all the libraries get added.

## How do I connect a bus to multiple pins?

To connect a bus to multiple pins, first draw wire stubs on selected pins or all the pins, and then select all the wire stubs and drag and drop them on the bus. A dialog pops up where you can specify the bus bit range. The signals are named according to the name of the bus and the bit range you specify.

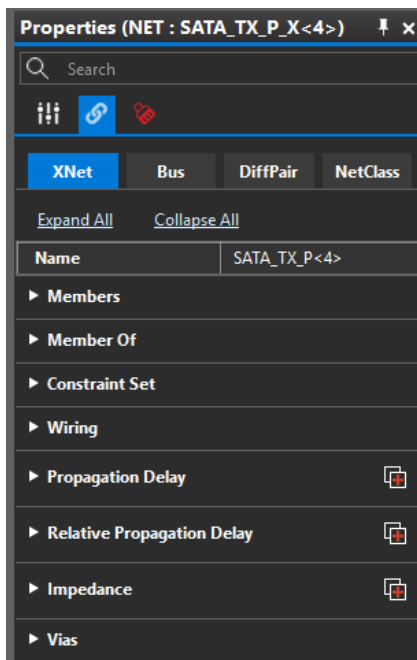


## How do I launch Constraint Manager from Allegro X System Capture?

There are two ways of accessing and setting up constraints in System Capture:

### ■ Docked Constraint Manager

Allegro X System Capture provides a docked Constraint Manager that uses the same database as Allegro Constraints Manager. You can edit constraints on the currently selected object(s) on the canvas, and capture all the Electrical constraints, as well as apply all types of Constraints Sets from the docked Constraint Manager. To access this screen, select the net(s), and click the *Constraints* tab in the *Edit Properties* window.



### ■ Allegro Constraint Manager

To launch Constraint Manager from System Capture, choose *Tools - Constraint Manager*.

## Why is the Special Symbols panel empty?

Ensure that the libraries containing the power, ground, and port symbols are available, and an entry exists for the libraries in the library configuration file, cds.lib.

To check:

- Which libraries are used in the current project, choose *Edit – Preferences – Library*.
- The Special Symbols configured, choose *Edit – Preferences – Schematic – Special Symbols*.

Configure special symbols using the directives in the site.cpm file. The configured special symbols will then be available in the *Special Symbols* list:

- For Power and Ground Symbols

```
power_symbols '+1_5V!1.5V:standard:p1_5v:sym_1 '
'GND!0V:standard:gnd:sym_1 '
'standard:p1_2v:sym_1 ' "
```

### **Important**

Ground can also be used instead of GND.

- For Port Symbols
  - ❑ INPORT

```
'standard.inport:sym_1 '
```
  - ❑ OUTPORT

```
'standard.outport:sym_1 '
```
  - ❑ IOPORT

```
'standard.ioport:sym_1 '
```
- For Off Page Symbols
  - ❑ OFFPAGE\_INPUT


```
'standard.offpage:sym_1 '
```
  - ❑ OFFPAGE\_OUTPUT

```
'standard.offpage:sym_2 '
```
  - ❑ OFFPAGE\_IO

```
'standard.offpage:sym_3 '
```
- For Alias Body

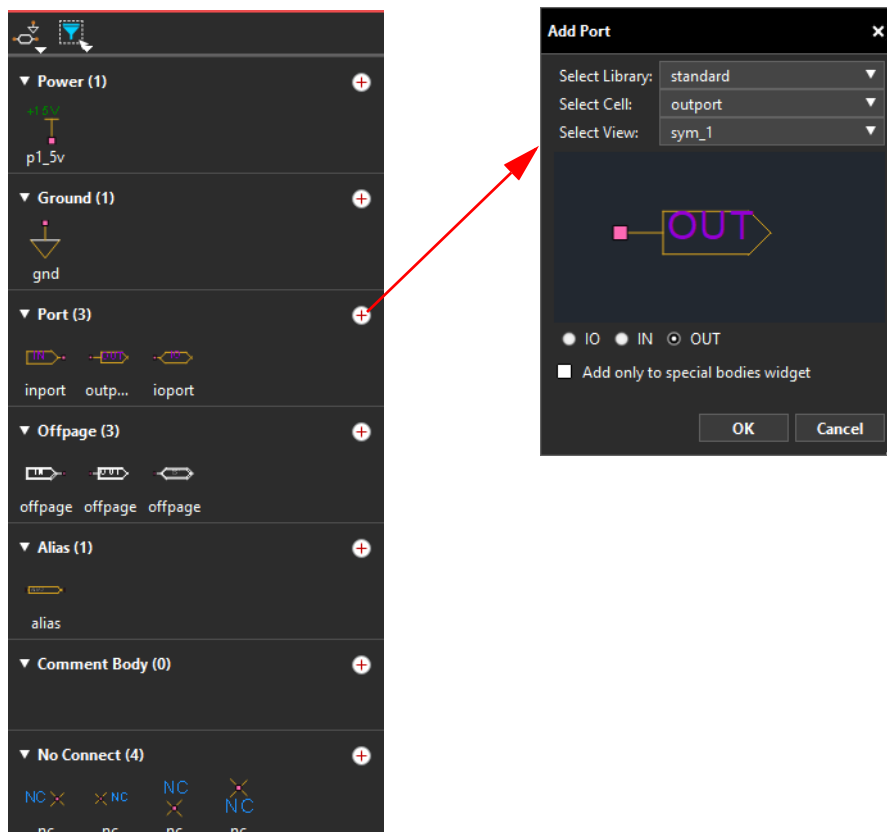
```
ALIASBODY 'standard.alias:sym_1 '
```

## How do I add new symbols to the Special Symbols bucket?

*Special Symbols* are components that are not packaged but provide logic to the design, such as power symbols, ground symbols, ports, offpage symbols, alias symbols, and so on. To add a new symbol, click the  button in any of the required category in the *Special Symbols* panel. A dialog box opens where you select the library, cell, and view.

### Important

You can add symbols using the red plus button only if CDS\_SITE is defined, and the project is using DE-HDL libraries.



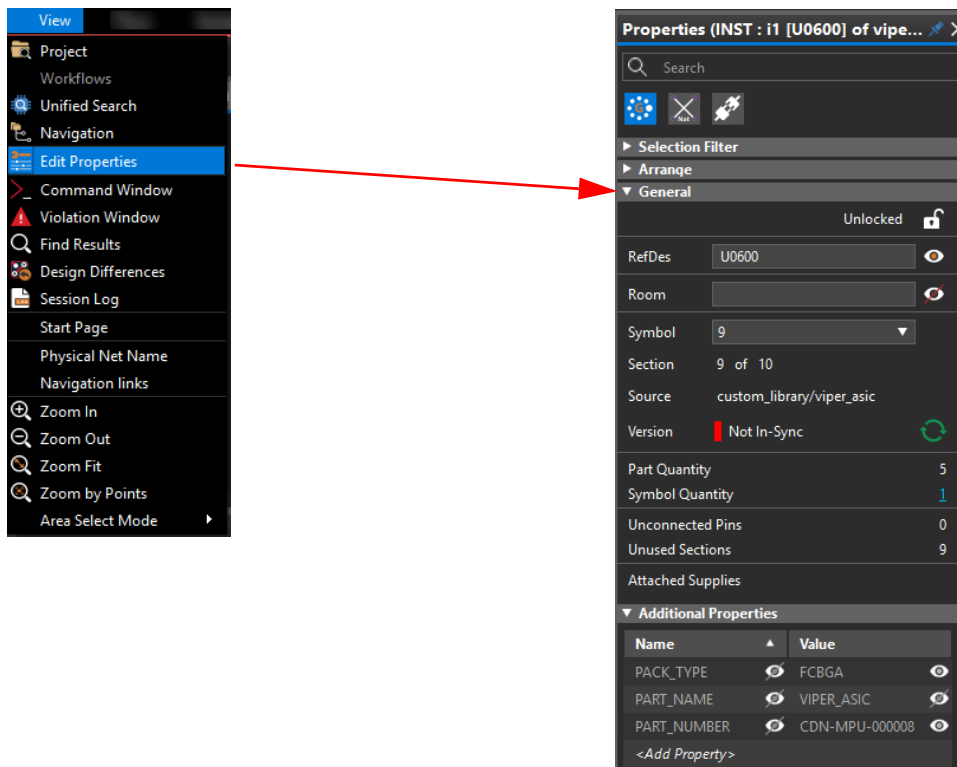
By default, the symbol gets added to the panel as well as gets available for placing. If you only want to add it to the panel and not place it immediately, choose *Add only to special bodies widget*.

## How can I control the Special Symbols panel at the site level?

The special symbols that are displayed are picked from the project (cpm) file. First the project.cpm file is checked, and, if no entries are found, the site.cpm file is checked, if available. When you use the + button and add the new special symbols, the settings get written in the <project>.cpm file and are available in the current project. You can move this content from the <project>.cpm file to the site.cpm file.

## How do I modify properties of parts?

To view the properties of any selected part, choose *View– Edit Properties*. In the *Properties* window, make the required modifications.

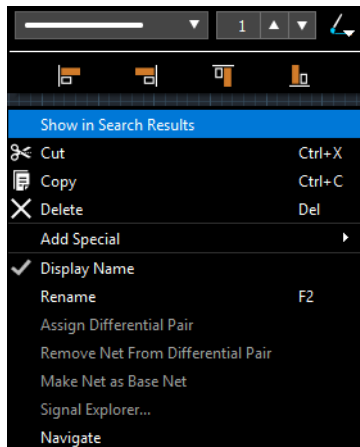


If the property is visible on the canvas, you can also edit it in-place.



## Can I display all the net names on a page?

Yes, you can display all the net names on a page. Set the Selection Filter to *Wire Only*, select all the objects on schematic, right-click and choose *Display Name*.



## Why do components get selected despite being disabled in the Selection Filter?

When you draw a selection rectangle by dragging the mouse on the canvas, all objects that lie within the selection rectangle based on the currently set selection filter get added to the application's internal selection set. The count next to each object type in the *Selection Filter* indicates the number of objects of that type in the internal selection set.

At this stage, if you change the selection filter settings, the object selection gets changed.

- If the selection filter is unchecked for an object type, the selected objects in that category get unselected.  
Whereas, the count of objects displayed remains the same.
- If you select the category again, all objects of that type get selected.
- If a category which was earlier not selected and now selected, there is no change in the selection of objects.
- To include the objects of the newly selected category, you need to create the selection box again on the schematic.

For object types that are enabled in the filter, System Capture shows selection handles around them. All operations are performed only on the objects with the selection handles

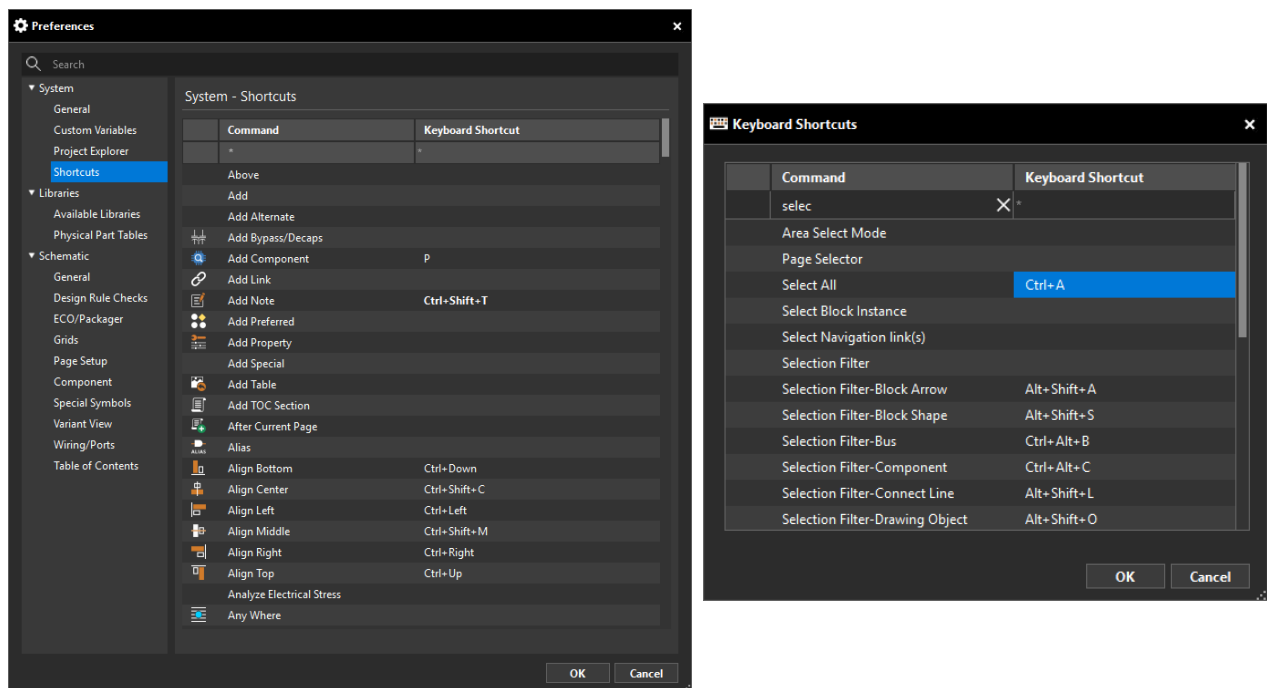
## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

shown. This allows you to perform multiple operations on an initially selected set by turning on or off the filters.

## Can I select or unselect objects using shortcuts?

Yes, with the help of custom shortcuts, you can achieve this. The default shortcuts available in System Capture are shown in the following screenshot. To select all the objects, use Ctrl + A. Next, other shortcuts can be used for selecting only a type of objects from the current selection.



## How do I set the custom pattern for auto creation of differential pairs?

The custom pattern is picked from a file in the site that you have set. Modify this file to define the new pattern, and the changed pattern will come into effect. The config file is:

```
... \CDS_SITE\cdssetup\canvas\resources\unison\sch\
```

where, CDS\_SITE is a variable that points to the site.

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

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#### Tip

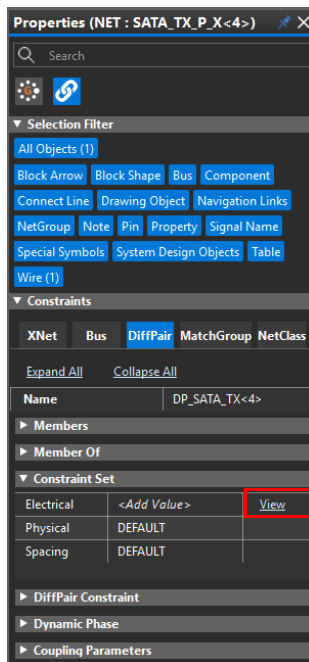
Use the `cnsAutoCreateDiffPair` Tcl command to automatically create Differential Pairs.

See the [Using Net Naming Patterns to Create Differential Pairs Automatically](#) section in the *System Capture User Guide*.

## Can I extract the Topology for a Differential Pair from the canvas?

When you extract a net that is part of a differential pair, only one leg of the differential pair gets extracted. To extract the topology of a differential pair:

1. Select a net that is a part of a diff pair.
2. Open the docked Constraint Manager  
The parent differential pair tab is displayed.
3. Select the *DiffPair* tab.
4. Click *View* in the *Constraints Set* section.



## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

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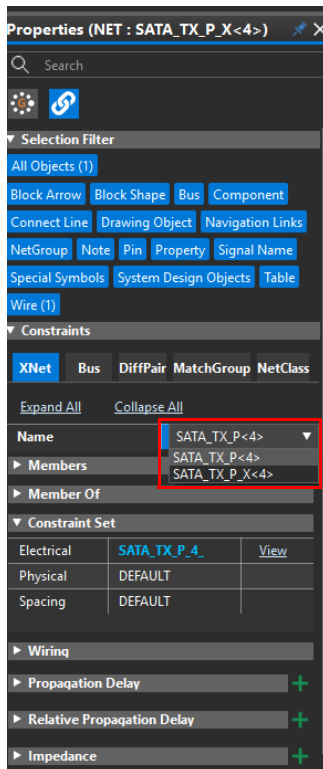
The differential pair gets extracted and is displayed in Signal Explorer (SigXP).

## How do I change the XNet name in Docked Constraint Manager?

To change the system-assigned XNet name using the docked Constraint Manager, do the following in the docked CM:

1. Click the XNet name.

A drop-down list is displayed.



2. Select another member of the XNet.

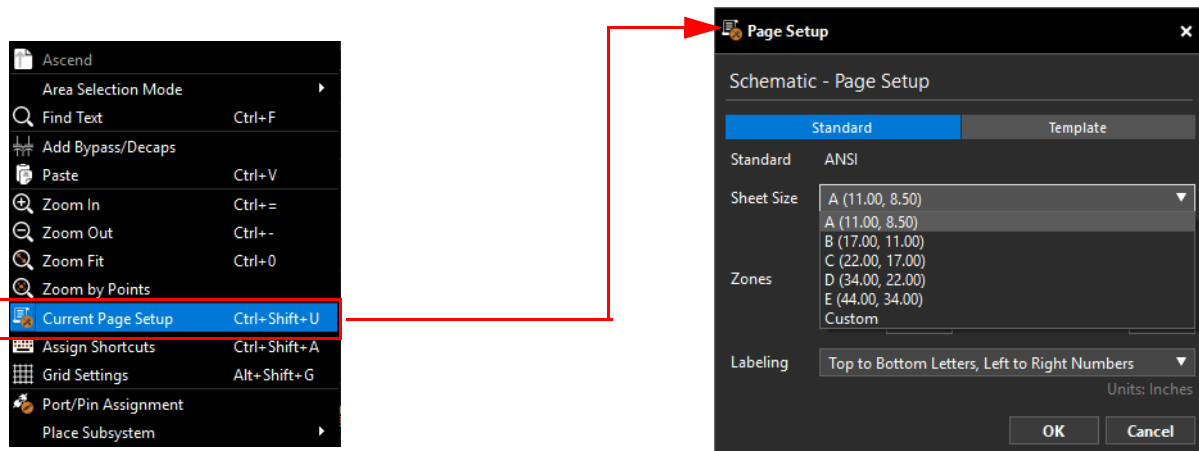
The XNet name changes.

## Can I configure the customizations of System Capture if I do not have a site?

No, a site is mandatory for doing any customizations. If you change settings in a project, they affect the current project only.

## How do I change the page size in the same project?

To change the page size for the current page, right-click in the empty area on the page and choose a different page size.

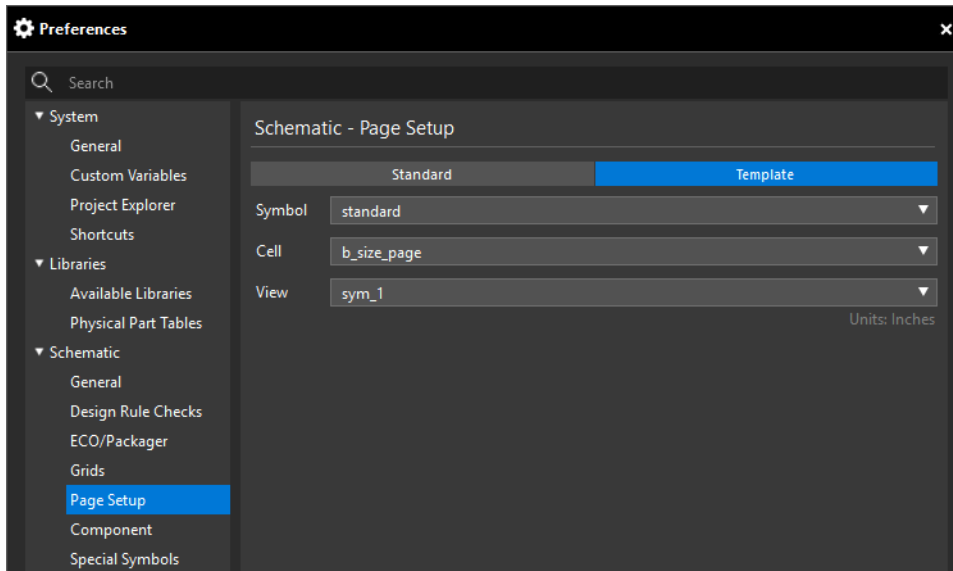


## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

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You can also set a different default Page Border for any new pages that are added to the design. Choose *Edit – Preferences – Schematic – Page Setup*, and specify the page size you want as the default.



## Do I need to use Part Developer to edit parts in System Capture?

You can edit block symbols within System Capture provided you have the required permissions for editing the part are available.

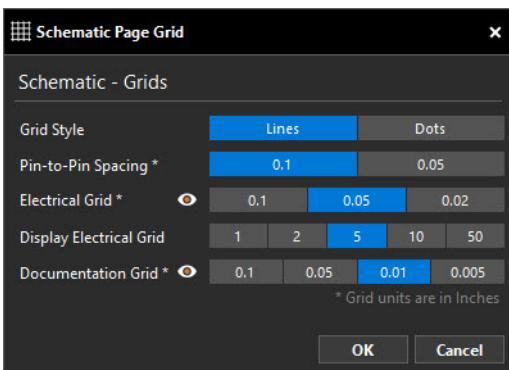
To learn more, see the *Symbol Editor User Guide*.

## Where can I access materials on library development with System Capture?

Library development in System Capture is the same as in DE-HDL, that is Part Developer is used for creating and managing library parts. You can access the tutorial in the documentation.

## How do I change the grid settings?

Changing the grid settings is not recommended, as this might impact the placement and routing of existing objects. Usually the grid is modified for accommodating documentation objects, such as text, images, drawing bodies and so on. For this, you should change only the Documentation Grid. The display settings of the Grid can be modified to adjust how it should look on the canvas.



To change grid settings, right-click on the canvas and choose Grid Settings. Or, choose *Edit – Preferences – Schematic – Grids*.

## Can I Change the Grid units from Inches to Millimeters?

The default unit for grids is inches because the Cadence-provided Standard libraries use inches for all components. If you are certain your libraries use millimeters, change the unit from inches to millimeters. To change the grid unit from inches to millimeters, modify the site or project CPM.

In the *START\_CANVAS* section, change the following:

```
GRID_UNIT_MEASURE 'INCHES'
```

```
GRID_PIN_PITCH '0.1'
```

to

```
GRID_UNIT_MEASURE 'MILLIMETER'
```

```
GRID_PIN_PITCH '1.00'
```

The changed grid unit will come into effect the next time System Capture is started.

## Can I use a PSpice library in inches with designs in mm?

By default, System Capture designs are configured to work with grids in inches. To use a PSpice library that has grids in mm, follow these steps:

1. Delete all ASCII and style files from the shipped PSpice DE-HDL library.
2. Use any of the following design grid settings to successfully use these PSpice DE-HDL library parts:
  - a. 0.1 inch  
pin-pitch: 0.1 inch  
grid snap fraction: 1.0
  - b. 0.05 inch  
pin-pitch: 0.1 inch  
grid snap fraction: 0.5  
Or  
pin-pitch: 0.05 inch  
grid snap fraction: 1.0
  - c. 0.5 mm  
pin-pitch: 1.0 mm  
grid snap fraction: 0.5  
Or  
pin-pitch: 0.5 mm  
grid snap fraction: 1.0)



***The 1.0 mm, pin-pitch: 1.0 mm, and grid snap fraction: 1.0 design grid setting will not work with the currently shipped PSpice DE-HDL library.***



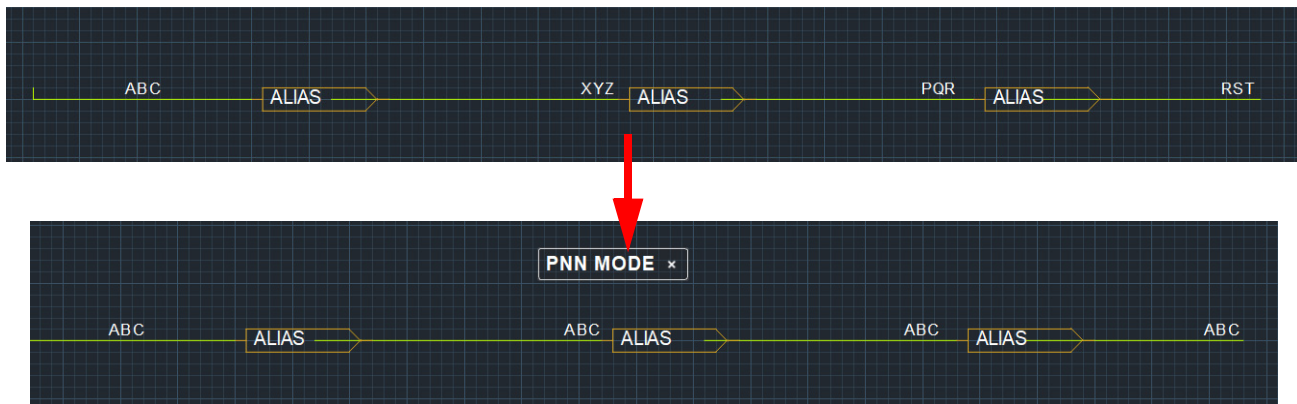
## What is a base net? How do I make a net the base net?

You can create aliases for nets by using the *Alias* body or the *Synonym* body from the *Special Symbols* window.

When you create aliases for nets, they all show up with the same physical net name that will also show in the netlist. By default, the common name for all the aliased nets is picked in the lexical order. For example, following nets are aliased:

- ABC
- XYZ
- PQR
- RST

The physical net name ABC will be used for all. To see the physical net names, choose *View – Physical Net Name*.

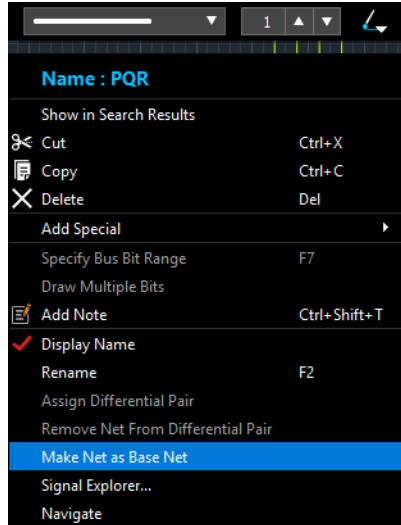


## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

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If you want to use another name, switch off the PNN View and right-click the net and select *Make Net as Base Net*.



Again, activate the PNN View, you will see the chosen net name for all aliased nets.



## **How does System Capture determine the base net when a net is aliased?**

System Capture decides the winning base net name based on the following:

1. Net at the higher level of hierarchy wins
2. Net with the Global scope wins over Interface, which in turn wins over Local
3. Named nets win over internal or unnamed nets
4. Lexicographical comparison based on the name of the net

## **How can I highlight an entire net on a page? All segments?**

Here are the key and click combinations for selecting a net and its segments:

- Clicking a wire, selects the wire segment only
- Double-click selects the wire segment and all wire segments connected to it
- Ctrl + Double-click selects all the connected as well as disjoint wire segments of the net on the entire page

## **Why don't I see the unconnected pin symbol for Power and GND symbols?**

The unconnected pin marker indicates that a pin is not connected to a net in the design. By definition, placing a power or ground on the schematic page add the corresponding net in the design which is connected to the symbol pin. That's why the unconnected pin marker is not displayed on symbol pins.

If you wish to see whether a wire is connected to the power/ground pin, use the option to turn on unconnected wire-end markers that would then display all wire ends not connected to pins.

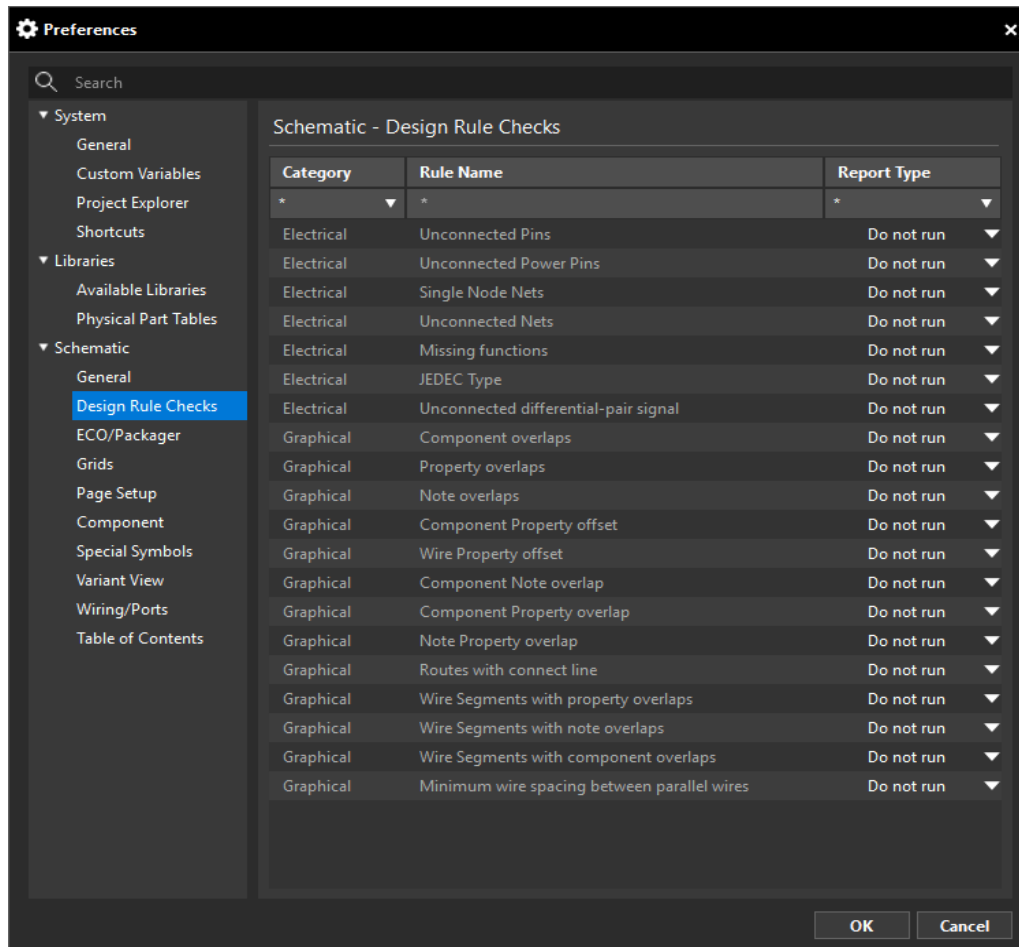
## **Why are the design rules not checked automatically?**

The rules that are part of the DRCs are optional rules that you can enable for improving the designs you are working on. These rules are not critical for design creation and, therefore, not run by default.

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

You can configure each of the DRCs to run and report violation as an Error, Warning, or Info from the Project Preferences dialog box.



To run DRC on the design, choose *Tools - Design Rule Checks*.

## Where are the values set for DRCs?

DRCs, such as the property overlap DRC, are controlled by the values set for the variables defined in the `<INSTALL>/share/cdssetup/canvas/rules_include/overrideValues.tcl` file. In case of false DRCs, check the values set for the following;

```
set ::ASDA_WIRE_PROP_OFFSET 500
set ::ASDA_INST_PROP_OFFSET 1000
set ::ASDA_MIN_WIRE_SPACING_DISTANCE 99
set ::ASDA_BBOX_TOLERANCE 0.25
```

## Can I see multiple pages of the design on different screens?

Yes. You can drag the page tab outside the current window to open a new workspace. Or, right-click on the tab, and choose *Dock To – New*. You can move multiple pages in one workspace, or create multiple workspaces.

## Where can I learn about variants and BOM in System Capture?

Both Variants and BOM reports are supported in System Capture. The [\*Managing Variants in System Capture\*](#) section contains modules covering these topics.

## How do I use strokes in System Capture like in DE-HDL?

System Capture does not support strokes. The common DE-HDL operations that were executed using strokes are now available in System Capture as single-key shortcuts, simple mouse movements, or accessible buttons.

## Why is worklib missing from my project when cds.lib has a worklib entry?

The support for *worklib* entry in the cds.lib file is for continuity. That is, to ensure legacy utilities that used to work with DE-HDL continue to work with System Capture.

## Can I configure where the packaging files get generated?

Yes. To specify where the packaging files get generated, update the following directive in the project cpm file:

```
START_CANVAS
packaged_folder './output/^(design_name^)/packaged'
END_CANVAS
```

## **Can I configure where the physical layout files get generated?**

You can specify this by setting the following directive:

```
START_CANVAS  
physical_folder './output/^(design_name^)/physical'  
END_CANVAS
```

## **How do I specify where the BOM reports should be saved?**

You can specify this by setting the following directive:

```
START_CANVAS  
bom_folder './output/^(design_name^)/bom'  
END_CANVAS
```

## **Why are the netlisting files (pst\*.dat) missing from the packaged folder?**

System Capture generates the netlisting files inside a compressed file that can be easily shared with those working on the layout. You have an option to configure the generation of these files in the extracted form with the following directive:

```
START_CANVAS  
preserve_dat 'ON'  
END_CANVAS
```

## **I am getting errors for Physical Net Name conflicts when running the back-to-front flow. Is there a command I can use to fix this?**

In case there are nets whose Signal Name and Physical Net Name do not match with PCB Editor (backend) origin, Physical Net names get annotated to a net while another net already has the same Physical Net Name attached.

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

---

To resolve this issue, run the following command in the Command Window:

```
regeneratePhysNetNames
```

This updates the Physical Net names based on the signal name.

## The Auto Shapes panel does not have the shapes I require. What can I do?

The Auto Shapes available in System Capture, such as block shapes and arrows, are configured in the following xml file:

```
$CDSROOT/share/cdssetup/canvas/resources/cdsbde.xml
```

You can add new shapes and block arrows to this file and place the modified file in the following folder to make the newly added shapes available:

```
$CDS_SITE/cdssetup/canvas/resources/cdsbde.xml
```

## How are XNets created in System Capture?

System Capture does not use DML for creating XNets. It operates in an DML-independent mode. XNet creation is done in one of two ways in the DML-independent mode. This is pre-configured in the site area so that all the projects have the same mode. When a new design is created, the mode is read from the site area and the new design is created accordingly. The modes of operation are:

- Automatic XNet creation across discrete devices when the devices are added to the design

In the Automatic XNet creation mode:

- ☐ XNets are created automatically between pins of a discrete device
- ☐ XNets can also be created between pins of non-discrete devices by adding the XNET\_PINS pin-level property
  - ☐ Pins of a component instance with the same value of the property would create a single XNet
- ☐ XNets are not created automatically when:
  - ☐ The component is not a discrete device
  - ☐ Any of the pins are connected to a DC Net



## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

---

- Pin limit is exceeded; the default maximum is 25 pins
- NO\_XNET\_CONNECTION property is found on the instance

#### ■ Manual XNet creation across discrete devices

In case of manual XNet creation mode:

- ❑ XNets are not automatically created between the pins of a discrete device.
- ❑ XNets can be created between pins of devices by adding the XNET\_PINS pin-level property
  - Pins of a component instance with the same value of the property creates a single XNet
- ❑ In this mode, even if the XNET\_PINS property is defined, XNets are not created when:
  - Any of the pins are connected to a DC Net
  - Pin limit is exceeded; the default maximum is 25 pins
  - The NO\_XNET\_CONNECTION property is found on the instance

#### ■ The following directive defines the XNet creation mode – Automatic or Manual

AUTO\_XNETS\_USING\_GATES

- ❑ Value of ON means, it's Automatic XNet creation mode
- ❑ Value of OFF means, it's Manual XNet creation mode

## Can I lock the grid settings at the site-level?

Yes, you can set a few directives at the site.cpm level and the grids get locked at the site level. The same grid settings get enforced across all the designs for all the designers.

Here is an example that shows how to lock the grid settings to a particular set of values:

#### 1. Set values for the grid settings:

```
START_CANVAS
```

```
...
```

```
GRID_DISPLAY_ENABLED 'both'
```

```
GRID_DISPLAY_MULTIPLE '5'
```

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

---

```
GRID_DOC_SNAP_FRACTION '0.100000'  
GRID_PIN_PITCH '0.100000'  
GRID_SNAP_FRACTION '0.500000'  
GRID_STYLE 'LINES'  
GRID_UNIT_MEASURE 'INCHES'  
...  
END_CANVAS
```

#### 2. Add the following lines to lock the grid settings site-wide:

```
START_CANVAS_CONTROL_SETTINGS  
GRID_DISPLAY_ENABLED LOCK  
GRID_DISPLAY_MULTIPLE LOCK  
GRID_DOC_SNAP_FRACTION LOCK  
GRID_PIN_PITCH LOCK  
GRID_SNAP_FRACTION LOCK  
GRID_STYLE LOCK  
GRID_UNIT_MEASURE LOCK  
END_CANVAS_CONTROL_SETTINGS
```

#### **Important**

When importing designs which have a different grid setting, System Capture attempts to adjust the components to match the destination design. It is recommended that this automatic adjusting be disabled for components and only the documentation grid is changed, as needed. To lock the grid adjustments, set the `CDS_SYSCAP_ENABLE_GRID_CHECK` system variable to 1.

## When I paste components, the REF\_DES\_PATTERN and other related directives are not used. Why?

While pasting any components after a cut operation, the reference designators from source are preserved. However, if you want the pasted components' reference designators be based

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

---

on the `REF_DES_PATTERN` applied to the project, you need to reassign the reference designators for the selected components. To reassign:

1. Select the set of components pasted.
2. Right-click and choose *Re-assign RefDes*.

In case the component is copied and then pasted, or the paste again option is used, the `REF_DES_PATTERN` is used for RefDes assignment.

## Where can I specify shortcuts?

System Capture shortcuts are defined at the following levels:

- Installation-wide
- Site-wide
- Local for a user

System Capture first picks the installation-level file, merges the data from the site-level file, and then merges the data from the user-level to get the final list of shortcuts.

The installation-level shortcuts are the default ones shipped with System Capture. If a user modifies any of the default shortcuts, the changed shortcuts are stored in the user's home area in:

```
$HOME/cdssetup/canvas/resources/cpUserShortcuts.txt
```

### **Important**

This file stores only those shortcuts that are different from the System Capture defaults.

Shortcuts can also be defined at the site level so that all users who are using the site get them by default. To add shortcuts to the site level in System Capture:

1. Define all the required shortcuts.

These get stored in the user-level shortcuts file.

2. Copy the shortcuts file to the site:

```
$CDS_SITE/cdsetup/canvas/resources
```

3. Rename it to `cpSiteShortcuts.txt`

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

---

You should have the following:

```
$CDS_SITE/cdsetup/canvas/resources/cpSiteShortcuts.txt
```

The shortcuts will now be available to all the users pointing to the site.

## Do the standard title blocks support custom variables and images?

All the custom variables in System Capture are available for adding to the schematic as part of Notes. These notes can be placed anywhere on the schematic sheet and need not be confined to the Page Border or Title Block. To add a custom variable to the note, put a \$ sign and it would display the list of all the custom variables available for adding.

In case you are using a standard size page, it would not have a title block attached to it. Add a Title block using the Special Symbols bucket. Once the Title block is placed (optional), the custom variable can be added to it. Also, the page border or title block can be configured to have a custom variable already added to it and they would get populated by the specified value.

## Why is Part Manager grayed out in the Tools menu?

The Part Manager menu is related to caching of parts in the System Capture design. The caching of the parts in the design occur only when you created a new project with the following directive set:

```
CREATE_CACHE_PROJECT
```

If you have a design that was not created with caching enabled and now you would like to make it cache-enabled, you need to.

Set the `CREATE_CACHE_PROJECT=true`

1. Use the following TCL command:

```
convertToCache
```

This caches all the parts that are currently used in the design and enables the *Part Manager* menu option. When you choose *Tools – Part Manager*, System Capture compares the parts in the design with the parts in the reference library and display the differences.

## A Tk script for Tcl commands is making System Capture unresponsive. How can I run it in the background?

Tk is not supported in System Capture. You can use HTML5 or JavaScript. If System Capture is getting blocked when an external process is launched, launch it in the background, using the following command:

```
exec <process...> &
```

## The cds.lib file for a new project had CONCEPT\_INST\_DIR and not CDS\_SITE. Why?

Check the location the CDS\_SITE environment variable points to. It seems to be an invalid location. When a new project is created, the contents of the cds.lib file are generated based on the following checks:

- If CDS\_SITE is defined and the location it points to is valid, cds.lib gets the following entry:

```
INCLUDE "$CDS_SITE/cdssetup/cds.lib"
```

- If CDS\_SITE points to an invalid location, check the CONCEPT\_INST\_DIR variable.

- If this is valid, cds.lib gets the following entry:

```
INCLUDE "$CONCEPT_INST_DIR/share/cdssetup/cds.lib"
```

- If both the variables point to invalid locations, no include statement gets added.

## Can I lock the project type for all new projects?

Yes. To lock the new project libraries mode, set the CDS\_SYSCAP\_NEWPROJ\_LIBMODE system environment variable to any of the following:

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

---

Type of Libraries	Value
Allegro unified library (ldax)	■ unified
	■ libdb
DE-HDL	■ DE-HDL
	■ dehdl
OrCAD Capture	capture

### If I want to use a sheet that is not recognized by System Capture, what changes do I need to do in the setup?

Add the following information to the `cref.dat` file in the site:

```
pagename "name_of_the_sheet"
```

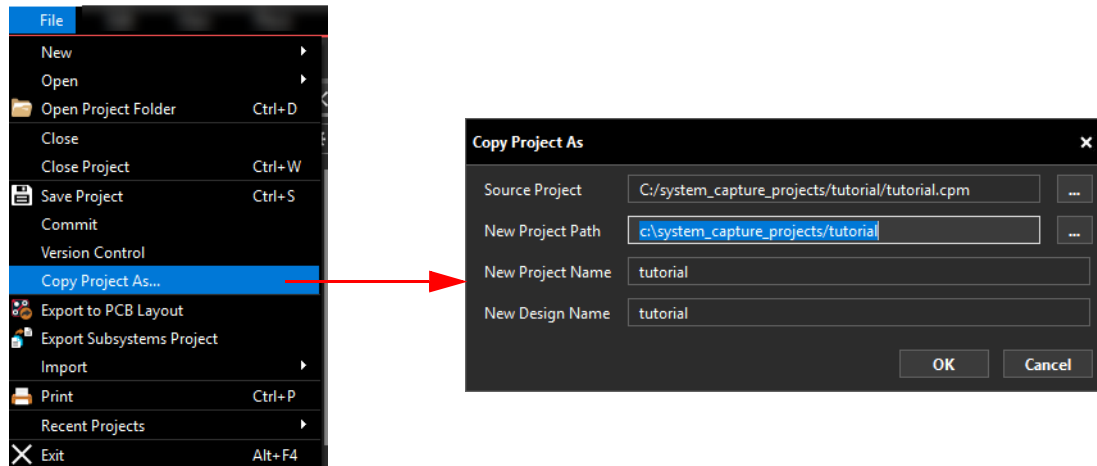
```
version 1
```

```
lowerleft (100, 100)
```

```
upperright (3650, 5250)
```

## Can I make a copy of a project?

Yes, use the *File – Copy Project As* command.



Add the details for the new project, and click *OK*. See

This creates a copy of the project at the specified location, and checks if you want to open the new project.

## Can I stop extra folders from getting copied when I make a copy of a project?

You can set two directives in the site.cpm before copying projects.

- `rename_folders_on_copyproj`
- `delete_folders_on_copyproj`

See the *Allegro Front-End CPM Directive Reference Guide* to learn more about setting up these directives.

## **How does PCB Editor process the bypass pin distance from parent that is set in System Capture?**

In System Capture, you can define the maximum distance that a capacitor can be placed from the power pin. Distance defined acts as the input to PCB editor to show a circle when the capacitor is moved beyond the specified distance.

The bypass capacitors are associated with the power pins of their parent component (by virtue of same net connection). For more information, refer to the PCB Editor documentation.

## **What happens when I set the Distance to zero for bypass distance capacitors?**

If any value greater than zero, is changed to zero in the Distance field of the Add Bypass Capacitors screen, the distance property is deleted and not passed to PCB Editor.

## **The default RefDes continuity has changed from left-to-right to top-to-bottom. How do I revert this?**

Allegro System Capture packages instances the moment they get added to the design. In case multiple instances are required to be processed as a single operation, for example because of copy-paste actions, sheet imports, sheet copy-paste, adding bypass rails, and so on, System Capture packages the instances from top-to-bottom and then left-to-right. To change this behavior back to original behavior, set the following directive:

```
START_CANVAS
...
SORT_INSTANCE_BY_ROW 'ON'
...
END_CANVAS
```



## How does REF\_DES\_PATTERN counter work with unique phys\_des\_prefix?

If the `REF_DES_PATTERN_FIX` directive is used in conjunction with `REF_DES_PATTERN` directive, the RefDes counter starts from 1 for each `PHYS_DES_PREFIX`.

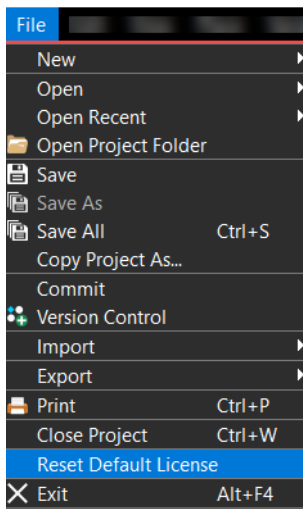
For example:

Instead of assignments as C1, C2, R3, R4, U5...

They are now made as C1, C2, R1, R2, U1...

## How do I change the currently used license in System Capture?

Use the *File – Reset Default License* command.



You can also run the `cps::resetLicenseCache` in the Command Window.

Restart System Capture and select a license.

## How do I globally unset all user-assigned references?

To reset user-defined reference designators to tool-defined reference designator for all instances in the design, use the following command:

```
changeRefdes -toolDef all
```

Some situations where this command is helpful are:

- Circuitry has been copied from another design that has hard locations
- Pages in the design have been rearranged and you want to restart the references on a specific page

## How does System Capture manage bus bits that get deleted from the schematic?

When bus bits are added to a schematic, System Capture updates its database to the highest value. This value remains in the database even after the net is deleted. Here are a few examples to explain this behavior.

### ***Example 1***

1. Add a bus C<0..10>
2. Add a net C<30>
3. Delete the net C<30>
4. Launch Constraint Manager

You will see that the net is from C0 to C30 although the bits C<11..30> do not exist in the design. You can add constraints for the nets C11 to C30 and they are retained even after you close the current session.

### ***Example 2***

1. Right-click a bus entry, such as FBUS<0..10>.  
You cannot tap the bits other than 0 to 10.
2. Create a wire and name it FBUS<20>.

**3. Connect FBUS<20> to FBUS<0..10>**

You will see that the bus name does not get updated. There will be a bus named FBUS<0..10> with bit F<20> connected to it.

## **Why do connections break when replacing components?**

When replacing components, System Capture retains connectivity based on pin positions. If the size of symbols is different, there is a possibility disconnection would happen.

## **Can I use an IP address of a server for the storing projects?**

You cannot directly use an IP address, such as *199.183.110.204/shared\_designs/*, for the `SYSTEM_CAPTURE_NEW_PROJECT_PATH` variable. This might result in errors when placing components. Map the IP address to a drive and then create projects.

## **Why is Edit Properties showing an incorrect instance ID (spath) when I add a block?**

The value that you see in the Edit Property property widget is the instance name, whereas the instance id is what seen as a part of the spath. Instance ID is generated and internally used by System Capture. This is not visible to the users.

## **Why am I unable to rename a scalar port to a vector port?**

Renaming a port from scalar to vector, or reverse, is unsupported. It is treated as deleting and adding two different ports by System Capture.

## How is setting reuse\_refdes to 'OFF' different in System Capture as compared to DE-HDL?

Assume the site.cpm file has the following directive:

```
reuse_refdes 'OFF'
```

When you delete a component in System Capture and add a new one, it gets the same reference designator (RefDes). This is in contrast with DE-HDL. In System Capture, the `REUSE_REFDES` directive stops the use of reference designators that have been exported to PCB Layout, that is only the reference designators that have been exported to the PST\* files are *not* reused.

As DE-HDL does not have online packaging, all reference designator assignments make it to pst\* files. Whereas, System Capture has online assignment, the assignment itself does not imply that it has been exported for PCB Layout. Consequently, any deleted instances get reused again.

However, once you run *File – Export for PCB Layout*, the reference designators exported to Layout do not get reused with `REUSE_REFDES` set to 'OFF'.

## How do I ensure user-defined properties get passed to PCB Editor?

Properties added on a part go as function properties. To make them flow on the refdes, define them as component instance.

By default, all user properties are passed to PCB Editor. The `netrev` command is invoked with the `-u` option that transfers all user-property definitions.

As properties added on instance are, by default, function instance properties, they are *not* visible in PCB Editor unless you choose to view *Function Instance* properties too.

To make a user property a *Component Instance* property rather than *Function Instance* property, follow these steps:

1. Right-click the *Component Properties Worksheet* Selector in the left panel of Constraint Manager UI and choose *Customize Worksheet*.
2. Right-click and choose *Select Add Column*.
3. Choose *User Property* from the list of user-defined properties.
4. Select *Edit* to edit the property definition.

5. Check the *PackageSameVal* flag under the Flow section.
6. Click *OK*.
7. Save the design and restart System Capture

Now when you package the design and export to PCB Layout, the property is available on the Component Instance.

## Why am I unable to generate a BOM or package my design?

There might be a packaging error because of mismatched pins in a symbol present in the reference library as compared to the symbol in the design.

To correct the mismatch:

1. Select the instance with the error.

This can be done in either of the following ways:

- ☐ Select the instance on the schematic
- ☐ Double-clicking the error in the violation window.

2. Enter the `refreshSymbol` command in the *Command* window.

This replaces the symbol in the design with the latest symbol present in the reference library and the error in the violation window is removed and BOM will be generated.

## Can I attach an interface port to power or ground nets?

No, you cannot connect interface port to power or ground nets in System Capture. The reason is that a power or ground net already has a Net Scope defined for it. Now, when an interface port is connected to it, System Capture attempts to change the Net Scope of the net to interface. This is not supported.

## Why are navigation links not working on imported blocks?

Currently, *View – Navigation Links* work only on the root design. In case you have imported a design or block and it is not yet instantiated in root, navigation links will not work.

Instantiate the block in the project hierarchy for generating navigation links for the block.

Change the root design in the *cpm* file and launch System Capture. Now when you choose *View – Navigation Links*, the links will work.

## Which page opens when I use the Descend command for a block in a hierarchical design?

The *Descend* command opens the page containing the port for the symbol pin appearing earliest alphabetically (lexicographically smallest).

For example, if a block instance has the following pins:

- *IO*
- *bus<0..3>*
- *A*
- *A1*
- *GND*

The page that contains the signal *A* is opened.

## Can the Header Row be removed from Tables?

The header row is a normal row with a different fill color to distinguish it from other rows of the table. The following directives control the appearance for different rows of a table:

```
START_CANVAS
TABLE_ALTERNATE_FILL_COLOR '#D2DDEF'
TABLE_FILL_COLOR '#E8EFF7'
TABLE_HEADER_FILL_COLOR '#5998D2'
```

## **Allegro X System Capture: Frequently Asked Questions**

### **Frequently Asked Questions**

---

END\_CANVAS

To have a table without a header row, add the table and then change the color of the header row using the Formatting options.

## **Why does ‘Create Project based on DE-HDL design’ stop working during desktop sharing or Web Ex?**

This is a known limitation of WebEx interfering with the functioning of the application being shared. In such cases, one workaround would be to share the application instead of the desktop. If that doesn't work, you should stop sharing, continue with the application processing and restart sharing.

## **How do I stop wires from being re-routed when moving components?**

Move the component while keeping the `Shift` key pressed. When the `Shift` key is pressed and the selection is moved, it moves only in one direction, horizontal or vertical. This ensures that the wires get extended only in one direction and not completely re-routed.

## **Why does Part Manager not report any packaging errors even if PPT files are missing?**

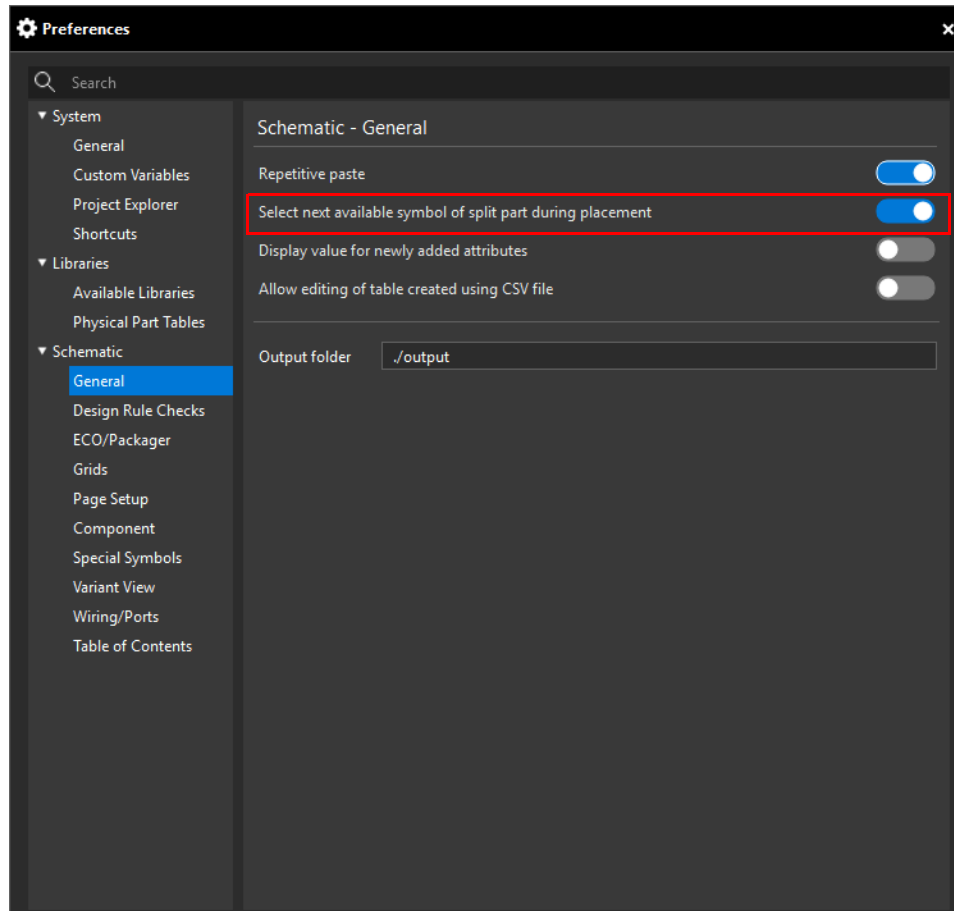
System Capture does not report packaging on not setting a correct PTF path because it adds parts logically and packages. This results in a potentially problematic scenario. The properties now are user-defined and can be edited or deleted.

For such designs, where PPT property is set in the source designs but not set in the destination design, System Capture reminds the user of this situation and confirms before proceeding.



## I have parts with multiple symbols. I want the next symbol to be automatically picked after each place. Can I do that?

Choose *Edit – Preferences – Schematic – General* there is an option to automatically select the next version for a split part.



For examples, if a part has ten symbols, System Capture will first place the first symbol, then the second, then the third, and so on.

## How do I see all the shortcuts that start with a letter?

To find all the shortcuts that start with a letter, you can use wildcard characters. For example, to find all the shortcuts that start with the letter A:

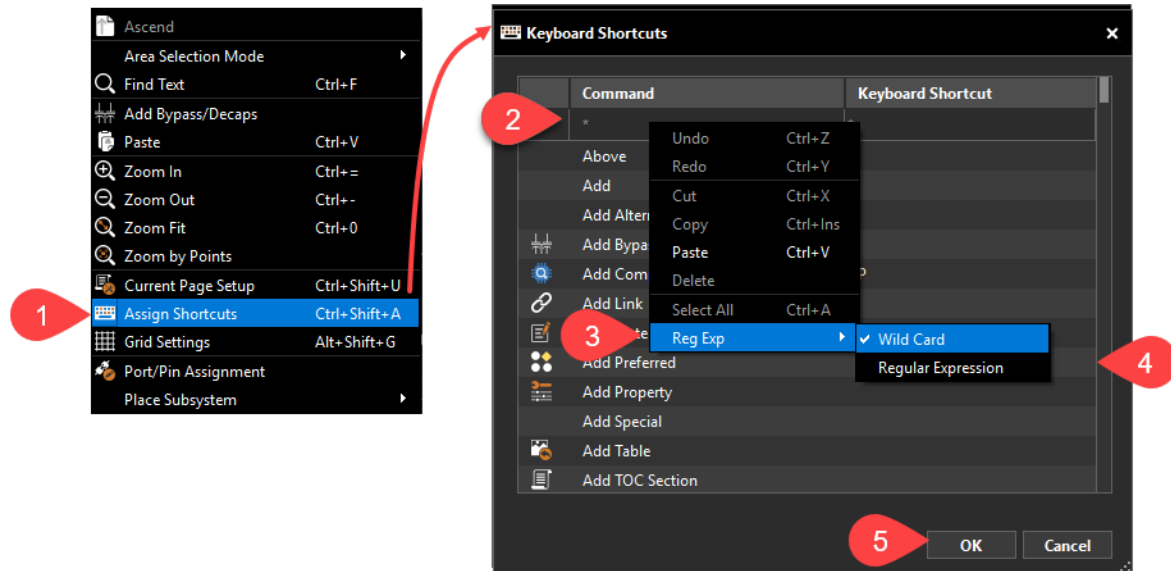
1. Right-click on the canvas.

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

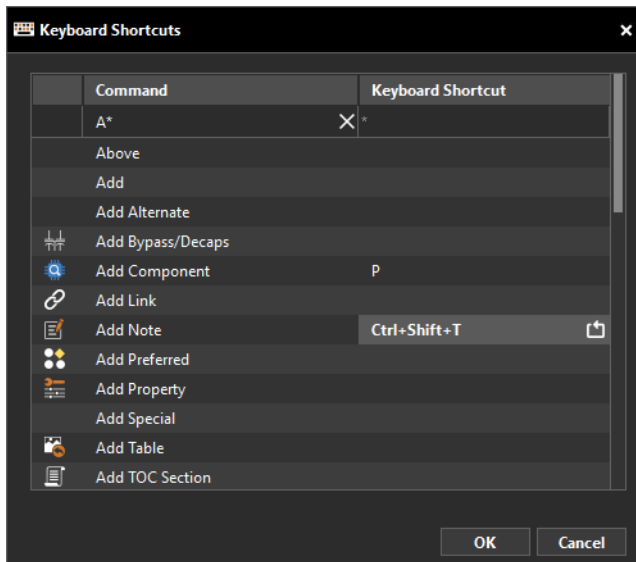
2. Choose *Assign Shortcut*.

3. Right-click in the search below the Command column and choose *Reg Exp - Wild Card*.



4. Type `A*` in the search box under *Command* column.

All the commands that match are shown.



## How do I ensure that the libraries added to a project are available to imported blocks?

In case you add additional libraries to a project and then import a block, the imported block will not contain any parts from the newly added libraries.

To ensure the libraries are available, you can use either of the following options:

- Add libraries before the block is imported so that it is available before the import happened.
- In case you have already imported a block before adding the libraries, switch the project to cached mode if it's not a cache-enabled project. Running Part Manager and updating the design differences will solve the problem.

## Can I import reuse blocks not in the root hierarchy of a design?

yes, System Capture import block can show the blocks outside a DE-HDL design hierarchy under a separate node and you can choose blocks from libraries other than the design library.

Set the `SHOW_ALL_BLOCKS_FOR_IMPORT` directive to `YES` in the `CANVAS` section.

**Note:** Default value set to 'NO'. (not added in cds.cpm)

## How is voltage for a power symbol picked?

The voltage value property is read from the symbol file. For example, if a cpm has the following entry:

```
POWER_SYMBOLS '+1_5V!1.5V:standard:p1_5v:sym_1'  
'GND!0V:standard:gnd:sym_1'
```

This is the `lib:cell:view` format and **not** the voltage of the power symbol. If the power cell does not have a voltage property, the default value is set as 0.

## Physical and Spacing Constraints from DE-HDL did not get imported. Why?

In any 17.2 design, to ensure that the Physical and Spacing constraints are imported, set the following directive in the project cpm in the START\_CANVAS section:

```
IMPORT_DEHDL_PNS_CONSTRAINTS 'ON'
```



In 17.4 designs, Physical and Spacing constraints are imported by default.

## How do I dynamically zoom into an area?

To dynamically zoom using the middle mouse-button:

1. Place the cursor where you want to zoom-in or zoom-out.
2. Keep the `Ctrl` key and scroll button (middle-mouse button) pressed and drag the mouse.
  - ☐ Drag up to zoom in
  - ☐ Drag down to zoom out

## How do I find out the page border symbol name?

To extract the lib/cell/view of the page border used by the current page, type the following in the *Command Window*:

```
sch::dbGetLibCellView <dbid of page>
```

For example:

```
set lcv [sch::dbGetLibCellView [sch::dbGetActivePage ]]  
puts $lcv
```

## How do I see the page name change in the page border as well as the open tab?

To show the page name or sheet title on the page border, add the custom variable `PAGE_TITLE` to symbol of the page border in the authoring application, such as Symbol Editor. You can edit the page name from the *Project Explorer* panel or the *Properties* panel.

## Why is the custom page border not showing the full grid?

For custom page border symbols, a `cref.dat` file is required to correctly display the grids, zones, and canvas. You can use the sample file present at `<INSTALL>\share\cdssetup\creferhdl\cref.dat` location and provide the required information. This file contains the required information for the Cadence-supplied page borders.

## How can I get Uncompressed Netlists in the Packaged folder?

By default, the `.pst` files get generated inside a single file database. But, if required, you can configure the project to create separate files. As the most common use model is to save the `.pst` files outside, System Capture generates them in the folder `output/<design_name>/packaged` based on entries in `cds.cpm`. The generated file is a single compressed file containing all the `pst` files. You can also create individual files by setting another project (`cpm`) file directive. The directives used here are:

```
START_CANVAS
```

```
packaged_folder './output/^design_name^/packaged'
```

```
preserve_dat 'ON'
```

```
END_CANVAS
```

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

---

where:

<code>packaged_folder</code>	Specifies location of output
<code>preserve_dat</code>	Ensures that .dat files are created

## Why am I seeing a Blank Symbol with no Pins and a Cross?

When a block is instantiated as a read-only block, the symbol in the cache gets updated but the instantiated cell does not get updated. As a result, System Capture cannot detect port rename on next reload. In case you see such a block, make the block editable (read-write) or re-import the block. The correct symbol along with pins will get displayed.

## Can I use existing CAE Views HDL programs with System Capture?

Yes, you can use existing programs. The CAE Views program code need not be changed for System Capture. All required changes are handled internally by System Capture. For physical design load, set the following directive in the site area:

```
START_CANVAS  
  
packaged_folder './worklib/^design_name^/packaged'  
  
END_CANVAS
```

This enables *Export Physical* to generate packaged output in specified location. Now, you can evaluate CAE Views programs based on physical database.

## Why can't I regenerate symbols for read-only blocks with unlocked symbols?

For unlocked symbols, *Regenerate Symbol* is not required as it would regenerate the symbol in preserve mode resulting in no graphical changes to the symbol. In case of a port mismatch error, clicking *Resolve* updates the symbol.

## Is There a way to Build Custom Reports?

Yes, you can add a *Generate Reports* menu option by following these steps:

1. Open the Command Window
2. Enter command:

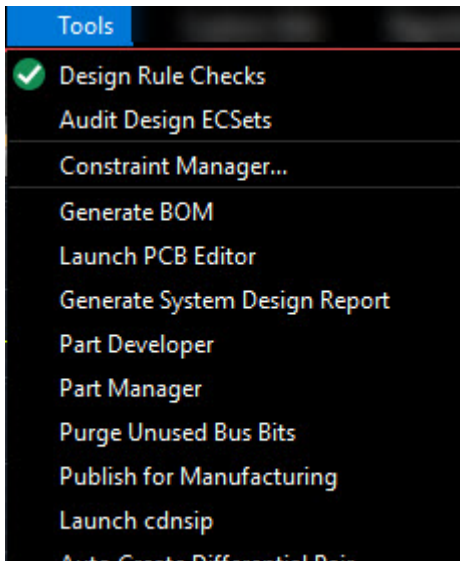
```
package require sdaReportGenerator
```

## Allegro X System Capture: Frequently Asked Questions

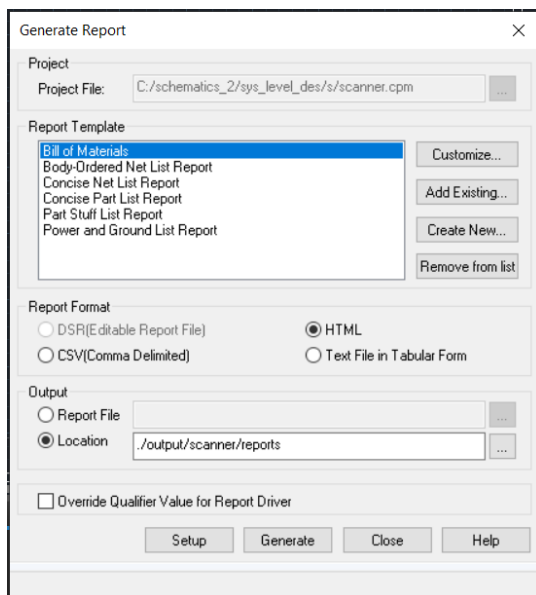
### Frequently Asked Questions

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A new option *Generate Reports* gets added to the *Tools* menu.



### 3. Choose *Tools – Generate Reports*.





## **Can I build custom dialog boxes?**

To create custom dialog boxes, or user interfaces (UIs), you require HTML5 or JavaScript. A sample is available in the installation at:

```
<SPB_INSTALL_ROOT>/share/cdssetup/canvas/samples/customGUI
```

Where the entry file is `customGUILoader.tcl`

For details, see the application note at:

```
<SPB_INSTALL_ROOT>/share/cdssetup/canvas/appnotes/Allegro System  
Capture AppNote - Custom GUIs.pdf
```

## **The TOC page number is no longer a roman number. Why?**

The page number for TOC has been changed from roman numbers to the same format as other page numbers starting with the 17.4 release. Consequently, if you open any design from an earlier version, in 17.4, the TOC page number changes.

## **Part Manager reported errors but Export to Physical Layout worked. Why?**

Starting from 17.4 QIR1, all the properties for the parts get annotated to the schematic. As a result, properties from Reference Libraries are not checked and netlisting is done based on the properties on the schematic. So, System Capture is not verifying if the properties on the schematic are in sync with the properties in the reference library. If due to any reason the properties are not annotated on the schematic, then System Capture queries the Reference Libraries for the properties and at that time checks if any of the schematic properties are current or not.

The annotation of all the properties on the schematic is controlled by the project file directive `ANNOTATE_ALL_PROPS`. When this directive is set, all the library part properties (PTF

properties) are annotated on the instance and *Export Physical* does not consider the mismatch of parts and proceeds with the schematic to layout translation.

## **Part Manager reports parts as not in sync for design imported from DE-HDL. Why?**

If a DE-HDL design is configured for upper case input, the library properties get annotated in uppercase even if the part definition has the properties in mixed case. System Capture does a case-sensitive comparison in Part management and reports these properties as not-in sync. Update the design with the correct syntax from library and get the parts in sync.

## **Does System Capture support pins on Comment bodies?**

No, System Capture does not support pins on Comment body. The reason is that comment bodies are pure documentation objects and do not provide any logic to the design. In contrast, power symbols add logic to the design. So, in case your designs have power or ground symbols, ensure comment bodies are **not** attached to them

## **Reset All is not clearing the XNet definitions even though the source is Schematic. Why?**

This happens when the definition of XNet pins is done in the master schematic for a block and that block also gets instantiated in the design. In such cases, the definition for the instance can be overridden on the block in context of the top-level design only. When you reset the instance, the definition from the master block shows up and the definitions are not removed.

## **In my design the bits of an XNet are under one bus in Constraint Manager. Why is the second bus empty?**

When you create an XNet of bits of different buses, the XNet goes under one of the winning bus entry. For example:

`strb_p<0>` and `strb_n<0>` are two bus bits that are connected using a resistor. They both appear under `strb_n` bus with the XNet name `strb_n<0>` as its bit.

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

---

The diff pair appears as:

```
DP1 --> strb_n<0>, strb_p<0>
```

The XNet is made from two nets, but both the bits appear under single bus:

BUS: strb\_n(2) with members: strb\_n<0> and strb\_p<0>

BUS: strb\_p is blank with no bits

## I have created a new project based on an DE-HDL design. Can I change the XNet state migration in the new design?

The XNet state is controlled at the time of design creation by the directive `AUTO_XNETS_USING_GATES` set in the `site.cpm`. If the value for this directive is different in the DE-HDL design, you cannot change it later.

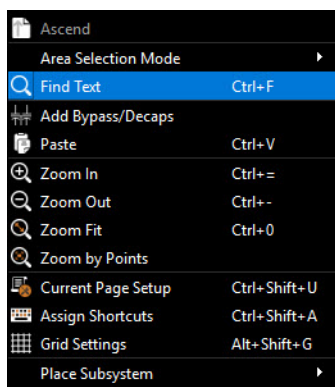
## How do I find a pin that has an overbar in its name?

To search for a pin with an overbar in its name:

1. Open the *Find* dialog box.

Use any of the following

- ☐ Press `Ctrl+F`
- ☐ Right-click on the canvas and choose *Find*.



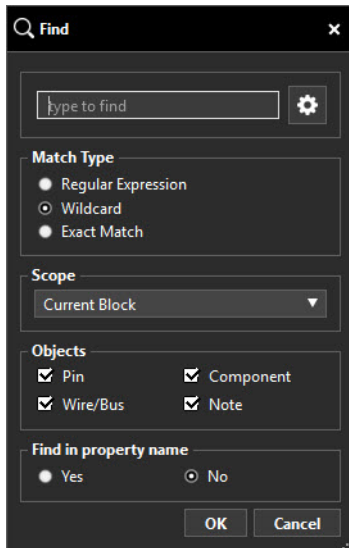
The *Find* dialog box opens.

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

---

2. Click the *Settings* icon.



3. Ensure *Pin* is selected.

You can use Exact Match or Regular Expressions.

- ☐ Go to [step 4](#) for using *Exact Match*.
- ☐ Go to [step 7](#) for using *Regular Expression*.

4. Select *Exact Match*.

5. Specify the name.

6. Go to [step 10](#).

7. Select *Regular Expression*.

8. Use back slashes as escape sequences.

9. For example: To find `C\L\R\` specify the string `C\\L\\R\\`

10. Click *OK*.

## Which application can I use to open PDFs in Linux?

You can use any available PDF reader, such as Foxit Reader.

## Are the log files for importing blocks or sheets saved? If yes, where?

The import process creates log files that are saved in the `<project>/temp/` folder. The file names are self-explanatory.

- `import_block.log`
- `import_reimport_block.log`
- `import_sheet.log`

## Can I export the notes in my design to an Excel file?

There is no direct way to accomplish this currently. But you can find all the notes in a design and then export them to a CSV file using Tcl commands as follows:

1. Find all the notes in the design.

```
find -scope "Entire Design" -types "note" {}
```

All the notes in the design will be displayed in the *Find Results* window. These results can be saved as a CSV file.

2. Export the find results to CSV.

```
cps::dumpSearchResults <path to folder> <string suffix>
```

Ensure the folder specifies already exists.

For example:

```
cps::dumpSearchResults ../search_data "design_notes"
```

This exports the find results to a file named `search_result_Notes_Design_Notes.csv` in the `search_data` folder. You can now open this file in Excel.

## Can I customize menu options based on the selected license?

Yes, you can show a specific list of the menu items based on the license chosen when System Capture is launched using a Tcl script.

## Allegro X System Capture: Frequently Asked Questions

### Frequently Asked Questions

---

Check the license selected using:

➡ `cps::getCheckedOutLicense`

Customize the menu options available.

For details of Tcl commands available for menu customization, refer to **Allegro System Capture Tcl Commands**.

## Why is there a cross on the symbol of an uninstantiated block?

Symbols in uninstantiated blocks are not refreshed on generation and a cross is seen on symbol. If a block port change is resolved, open the parent block once. Or, run the `refreshSymbol` command. The cross mark will be removed.

## I used the Replace command, but the Ref Des letter did not change. Why?

When using the *Replace* command, reference designators are not preserved for parts with a different `PHYS_DES_PREFIX`.

For example, if a resistor is replaced with a capacitor, the reference designator  $R^*$  is changed to the reference designator  $C^*$ .

## Ref Des does not follow the REF\_DES\_PATTERN directive in hierarchical designs. How to correct that?

System Capture performs packaging at all levels of the designs. As a result, the patterns are applied at the time of master block packaging and not reapplied for components in context.

To achieve pattern-based assignment in hierarchy, use the following:

```
REF_DES_PATTERN ' ($PHYS_DES_PREFIX) [0-9] [0-9] [0-9] (001) '
```

```
BLOCK_REF_DES_PATTERN ' ($PHYS_DES_PREFIX) ($DOMAIN) ($SOURCE_VAL) '
```

## Why does the Replace command open Find and Replace sometimes and not Unified Search?

The behavior of the *Replace* command depends on how many components are selected when you right-click and choose the *Replace* option.

- If only one component is selected, the Unified Search panel is opened for selecting a replacement component.
- If multiple components are selected, the Find and Replace dialog box is opened.

## Can I change the Text Editor that open for the Edit Externally command?

Yes, you can. By default, on Windows systems, Notepad opens. If you require another editor, such as Notepad++, use the `text_editor` directive.

Ensure that the editor supports blocking mode, which means when the editor is launched in foreground, it blocks the current process, and System Capture waits for the process to complete. To launch Notepad++ in blocking mode, pass the `-nosession` parameter in the command line, for example:

```
START_CANVAS
AUTO_XNETS_USING_GATES 'OFF'
BASE_NET_OVERLAY 'ON'
text_editor '"C:\\Program Files\\Notepad++\\notepad++.exe" -nosession'
```

**Note:** Remember to use escape character for the backslash character.

## Is there any way to Export to PCB without running Part Manager?

This is not a recommended practice, but if needed can be done.

Choose the option to Annotate all Properties on component instances, ensure the electrical parts are in *Manual Sync*.



The netlist generated may not be complete.

## Changing the symbol version removes the variant data. Is there a way to stop this?

After creating a variant, if you assign a new preferred part, change its version, and save the design, then the variant changes are lost. To prevent this, add the following to the cpm.

```
START_CANVAS
```

```
VAR_SYNC_ON_REFDES 'ON'
```

```
END_CANVAS
```

## How can I prevent display issues on 4K monitors?

The underlying framework of System Capture might cause display issues. To disable 4K support, set the following environment variable:

```
CDS_CP_DISABLE_HIGH_DPI=1
```

## How do I change the Pulse dashboard language to English?

To view the Pulse dashboard in another language, append a language argument to the dashboard URL. For example, to view the dashboard in English, append `en` as follows:

```
http:<host name>:<port>/projects?lang=en
```

The Pulse dashboard menus support the following languages:

Chinese - Append the following to the server URL: `zh`

Japanese - Append the following to the server URL: `ja`

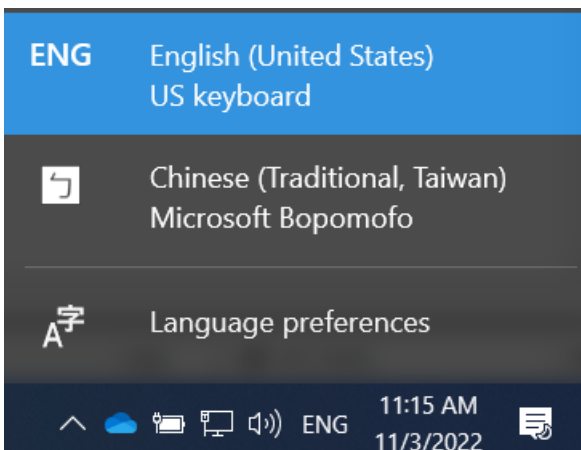
## How can I display Chinese characters in Unified Search when using Capture CIS flow in System Capture?

To display the Chinese characters in *Unified Search*, perform the following steps on your machine:

1. Click *Start – Settings*.
2. Click *Time & Language – Select Language*.
3. Click *Administrative language settings* in *Related settings*.
4. In the *Region* dialog box, click *Change System Locale*.
5. Select the check-box *Beta: Use Unicode UTF-8 for worldwide language support*.
6. Click *OK*.

Restart the machine to apply the changes.

The selected language options are displayed on the machine.



## Can I run specific commands before and after an operation or command?

Yes, it is possible to run commands before or after an operation with the `cps::registerCommand Tcl` functionality. The *Allegro System Capture Tcl Commands Reference Guide* has details in the [registerCommand](#) section.

## Why doesn't System Capture show a star on pages to indicate the unsaved changes?

System Capture is a design editor, and not a page-editor. That is when you add a wire or bus on a page in the design, it is immediately available on all the pages of the block. So, even though you have added the object to just one page, you have edited the entire design. Therefore, showing a '\*' on just one page is not the correct representation of the design state. This is why System Capture does not show '\*' on pages.

## Can I use DE-HDL property names in scripts in System Capture?

Yes, you can reuse scripts that use DE-HDL property names. The property names in DE-HDL and System Capture are the same internally, only the display names are different. For example:

- Property name is LOCATION and display name is Refdes
- Property name is PN and display name is Pin number
- Property Name is JEDEC\_TYPE and display name is Footprint
- Property Name is SEC and display name is Section

### *Important*

The \$ prefix is not supported for property names in System Capture so avoid this prefix for property names.

## **How can I prevent table column widths on PDFs from shrinking when printed on non-local displays?**

Make sure that the resolution of xvfb (X virtual framebuffer) matches the display resolution for correct PDF output. This issue is not seen in local displays, such as your local machine.