

OrCAD® X Capture with OrCAD® X Presto Tutorial

Product Version 23.1
September 2023

© 2023 Cadence Design Systems, Inc. All rights reserved.

Portions © Apache Software Foundation, Sun Microsystems, Free Software Foundation, Inc., Regents of the University of California, Massachusetts Institute of Technology, University of Florida . Used by permission. Printed in the United States of America.

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Product PSpice contains technology licensed from, and copyrighted by: Apache Software Foundation, 1901 Munsey Drive Forest Hill, MD 21050, USA © 2000-2005, Apache Software Foundation. Sun Microsystems, 4150 Network Circle, Santa Clara, CA 95054 USA © 1994-2007, Sun Microsystems, Inc. Free Software Foundation, 59 Temple Place, Suite 330, Boston, MA 02111-1307 USA © 1989, 1991, Free Software Foundation, Inc. Regents of the University of California, Sun Microsystems, Inc., Scriptics Corporation, © 2001, Regents of the University of California. Daniel Stenberg, © 1996 - 2006, Daniel Stenberg. UMFPACK © 2005, Timothy A. Davis, University of Florida, (davis@cise.ul.edu). Ken Martin, Will Schroeder, Bill Lorensen © 1993-2002, Ken Martin, Will Schroeder, Bill Lorensen. Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, Massachusetts, USA © 2003, the Board of Trustees of Massachusetts Institute of Technology. All rights reserved.

Trademarks: Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522.

Open SystemC, Open SystemC Initiative, OSCI, SystemC, and SystemC Initiative are trademarks or registered trademarks of Open SystemC Initiative, Inc. in the United States and other countries and are used with permission.

All other trademarks are the property of their respective holders.

Restricted Permission: This publication is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this publication, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this publication subject to the following conditions:

1. The publication may be used only in accordance with a written agreement between Cadence and its customer.
2. The publication may not be modified in any way.
3. Any authorized copy of the publication or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
4. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

Disclaimer: Information in this publication is subject to change without notice and does not represent a commitment on the part of Cadence. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information. Cadence is committed to using respectful language in our code and communications. We are also active in the removal and/or replacement of inappropriate language from existing content. This product documentation may however contain material that is no longer considered appropriate but still reflects long-standing industry terminology. Such content will be addressed at a time when the related software can be updated without end-user impact.

Restricted Rights: Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor.

Contents

1

Tutorial Overview	7
<u>Audience</u>	7
<u>Using the tutorial</u>	7
<u>Sample Design</u>	8

2

Creating a Schematic Design	9
<u>Creating a New Project</u>	11
<u>Creating Design in Capture</u>	15
<u>Subdesign 1: 12 Volt to 5 Volt Converter</u>	15
<u>Subdesign 2: 12 Volt to 3.3 Volt Converter</u>	24
<u>Subdesign 3: Smart Multi-Channel Switch Circuit</u>	27
<u>Summary</u>	33

3

Simulating a Design	35
<u>Getting the Design Ready for Simulation</u>	35
<u>Creating a Stimulus File</u>	36
<u>Creating a New Simulation Profile</u>	37
<u>Running the Simulation</u>	41
<u>Viewing Output Waveforms</u>	41
<u>Summary</u>	48

4

Preparing for PCB Layout Creation	49
<u>Adding and Placing Connectors</u>	49
<u>Updating Footprints</u>	55
<u>Updating Footprints Associated with Resistors</u>	55

OrCAD X Capture with OrCAD X Presto Tutorial

<u>Updating Footprints Associated with Capacitors</u>	59
<u>Updating Footprints Associated with Inductors</u>	59
<u>Configuring the PSpiceOnly Property</u>	59
<u>Adding Constraints</u>	62
<u>Summary</u>	67
5	
<u>Creating a Board Design</u>	69
<u>Creating a Blank Board</u>	69
<u>Summary</u>	73
6	
<u>Setting Up Layout Editor Design Environment</u>	75
<u>Adding Footprints and Padstacks Libraries</u>	75
<u>Modifying Default Design Outline</u>	76
<u>Setting Up Design Parameters</u>	77
<u>Viewing Cross Section and Material Information</u>	78
<u>Adding Artwork Views</u>	79
<u>Summary</u>	81
7	
<u>Placing Components Interactively</u>	83
<u>Setting Grid for Placement</u>	83
<u>Placing Components</u>	84
<u>Summary</u>	88
8	
<u>Routing Nets Interactively</u>	89
<u>Setting Up Constraints</u>	89
<u>Assigning Color to Power and Ground Nets</u>	91
<u>Routing Design Interactively</u>	93
<u>Renaming Components</u>	95
<u>Summary</u>	96

9

<u>Validating the Design</u>	97
<u>Analyzing the Design in 3D</u>	97
<u>Generating Reports</u>	103
<u>Summary</u>	105

10

<u>Exporting Manufacturing Output</u>	107
<u>Generating Output Files</u>	107
<u>Summary</u>	113

OrCAD X Capture with OrCAD X Presto Tutorial

Tutorial Overview

This tutorial enables you to evaluate the power of OrCAD® X Capture CIS, PSpice Advanced Analysis, and OrCAD® X Presto. You can run through the steps in the tutorial to perform the basic tasks in the PCB design process.

You will start with capturing the circuit diagram in Capture CIS, followed by running circuit simulation using PSpice, through to designing the PCB layout and generating the manufacturing output in OrCAD X Presto to complete the design cycle.

This tutorial does not cover all the features of each of the OrCAD X tools. It only highlights the tasks that you need to perform so that your design works smoothly through the flow.

Audience

This tutorial is useful for:

- Designers who want to use OrCAD X tools for the complete PCB design flow or for analog and digital simulation flow.
- First-time users of Capture CIS, PSpice, and OrCAD X Presto.

Using the tutorial

To run through the complete tutorial, you need the following tools available with the OrCAD X Professional and OrCAD X Standard licenses:

- Capture CIS
- PSpice Advanced Analysis
- OrCAD X Presto

OrCAD X Capture with OrCAD X Presto Tutorial

Tutorial Overview

Sample Design

The design created by the end of this tutorial is available at the following location:

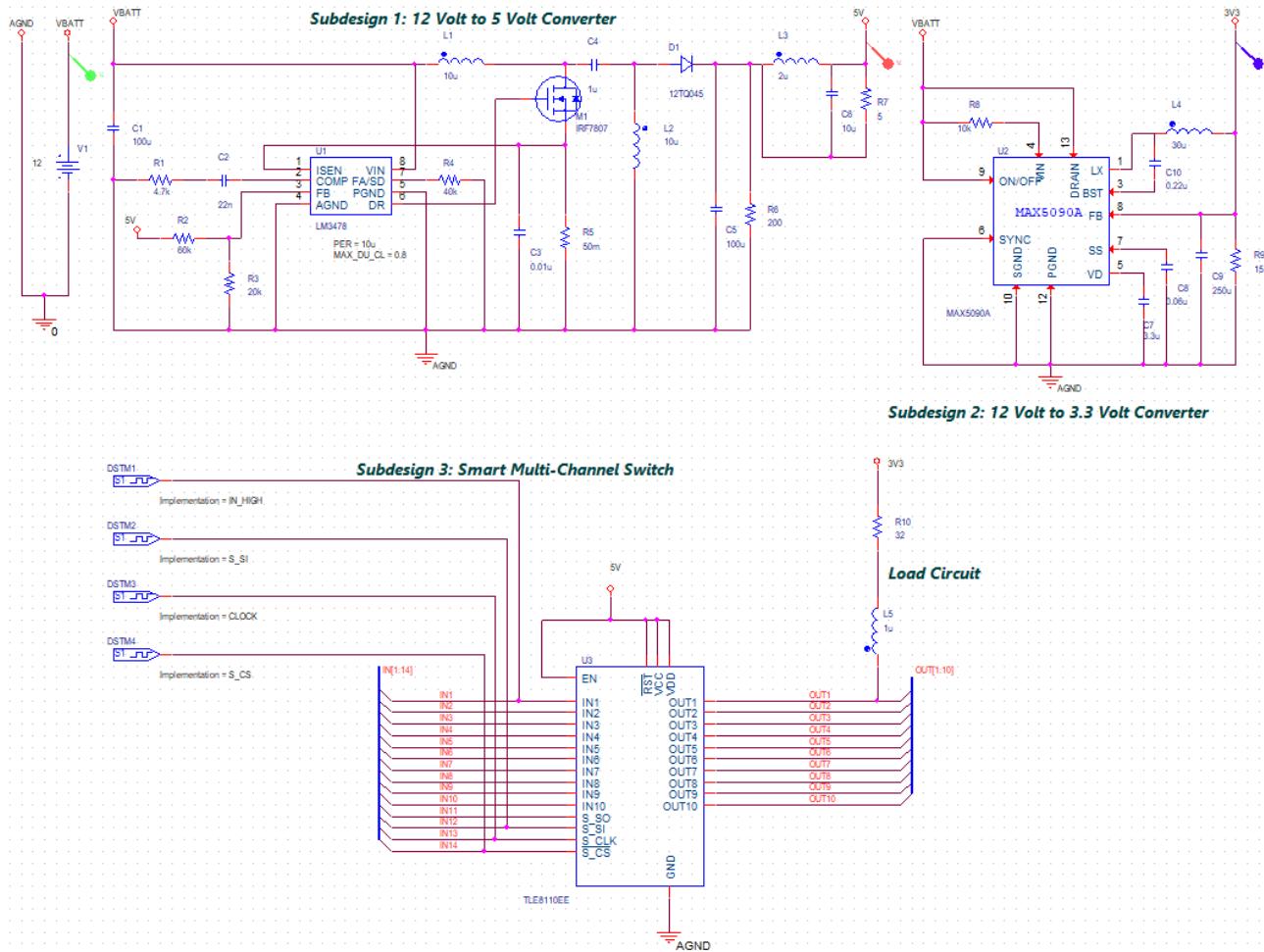
`<install_directory>\share\orcad\tutorial\tutorial.opj`

Cadence > SPB_23.1 > share > orcad > tutorial >				
Name	Date modified	Type	Size	
allegro	9/25/2023 12:02 PM	File folder		
tutorial-PSpiceFiles	9/25/2023 12:02 PM	File folder		
stimulus.stl	8/13/2019 6:14 AM	STL File	1 KB	
TUTORIAL.DSN	1/20/2020 4:45 AM	DSN File	188 KB	
tutorial.opj	1/20/2020 5:26 AM	OPJ File	9 KB	

Creating a Schematic Design

In this section, you will create a schematic design for a fan-control module with three subdesigns as illustrated in the following figure:

Schematic design for the complete fan-control module



OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

The following table provides a brief description of the function of each subdesign:

Subdesigns in the fan module circuit

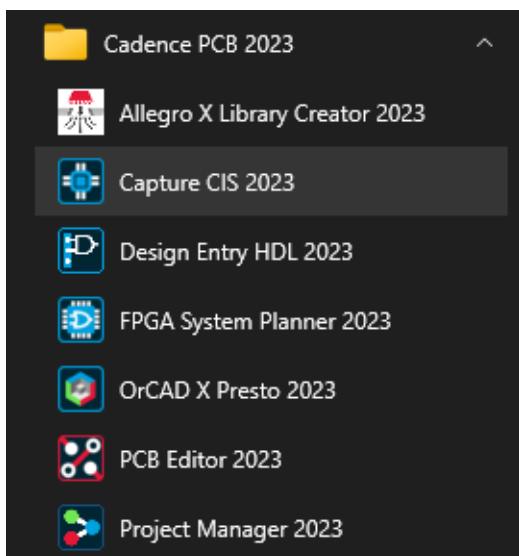
Subdesign	Function
Subdesign 1	A step-down DC-DC converter. It uses IC LM3478, a low-side n-channel MOSFET controller for switching regulators, which converts 12 volt to 5 volt. The output of 5 volts is the internal power supply for this circuit. It provides supply voltage to IC TLE8110EE (in subdesign 3).
Subdesign 2	A step-down DC-DC converter that uses the IC MAX5090A to convert 12 volt to 3.3 volt.
Subdesign 3	A smart multi-channel switch, TLE8110EE powered by a 5 volt supply. This switching of IC, TLE8110EE can control multiple load types (fan load in this tutorial). It has 10 input channels and a serial peripheral interface (SPI). It has 10 output pins, which can control up to 10 fans.

Creating a New Project

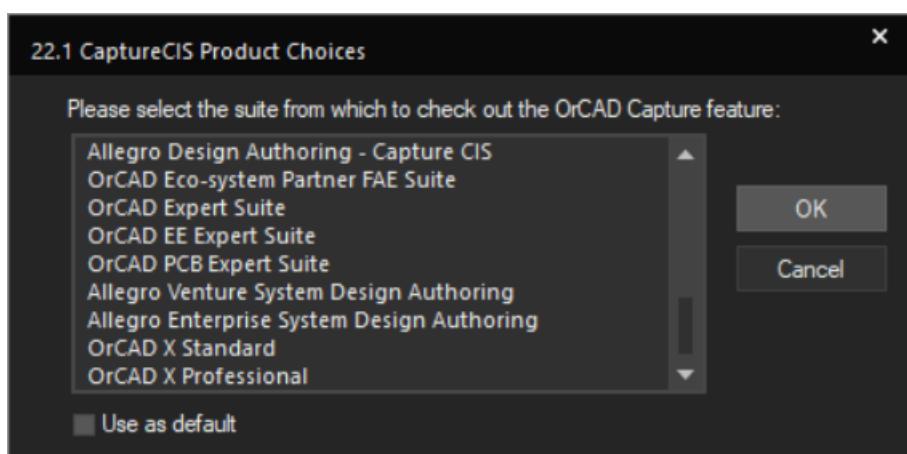
A project file (.OPJ) is a container for the design file (.DSN). In addition, a project file also includes simulation profile and layout information.

To create a new project, do the following:

1. From the Start menu, select *Capture CIS 2023*.



The 23.1 *CaptureCIS Product Choices* dialog box opens.



2. Select *OrCAD X Professional* and click *OK*.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

The OrCAD X Capture CIS window opens. When you open Capture with an OrCAD X license, you are prompted to provide your login credentials to access OrCAD X-enabled features.

Note: This step is not mandatory for the purpose of this tutorial. You can skip this step by closing the login window and moving to the next step.

To learn about OrCAD X Capture CIS part authoring capability, see [OrCAD X Part Authoring Tutorial](#).

3. Choose *File – New – Project*.

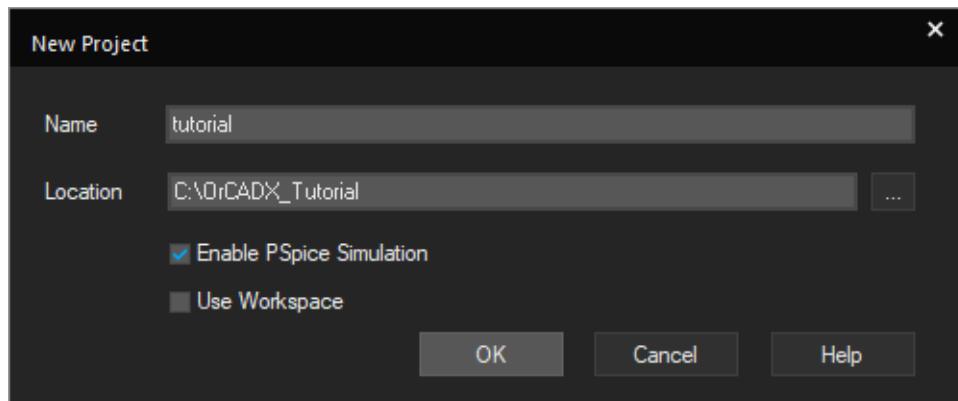
4. In the *New Project* dialog box, specify the project name as *tutorial*.

At the time of creating a new project, you can decide if you want to store the project in the OrCAD X Cloud workspace. If you select the *Use Workspace* option in the *New Project* dialog box, the Cloud workspace location is pre-seeded and cannot be changed later:

`%HOME%\cdssetup\workspace\`

5. For the purpose of this tutorial, deselect the *Use Workspace* option.

6. Specify the location as: *C:\OrCADX_Tutorial*.



The *Enable PSpice Simulation* option is selected by default.

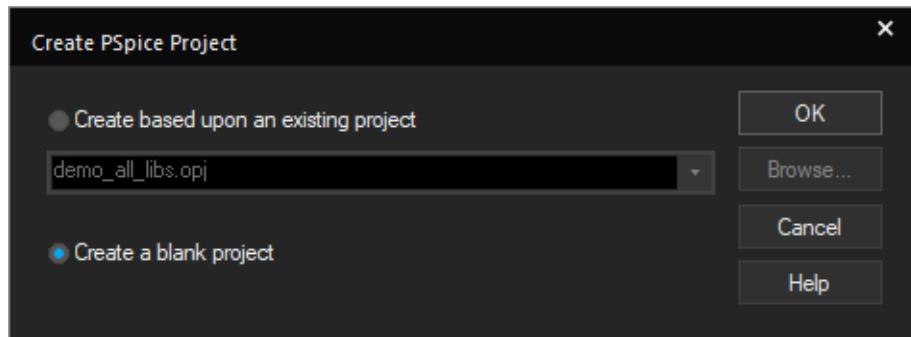
7. Click *OK*.

The *Create PSpice Project* dialog box opens.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

8. Select *Create a blank project*.

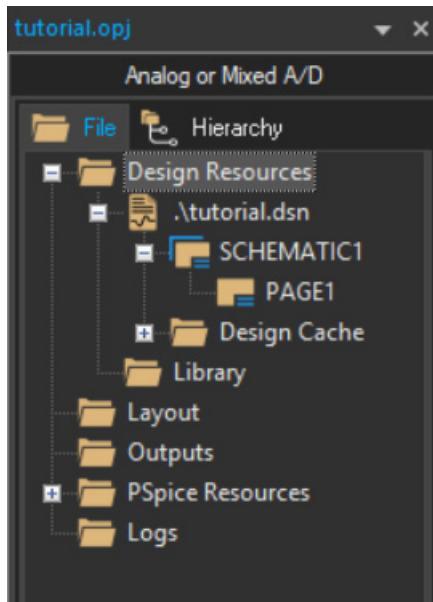


When you create a blank project, the project can be simulated in PSpice, but libraries are not configured by default. When you base your project on an existing project, the new project has the same configured libraries.

9. Click **OK**.

The tutorial project is created. In the project manager window, a design file, `tutorial.dsn`, is created. Under the design file, a schematic folder with the name `SCHEMATIC1` is created. This folder contains a schematic page named `PAGE1`.

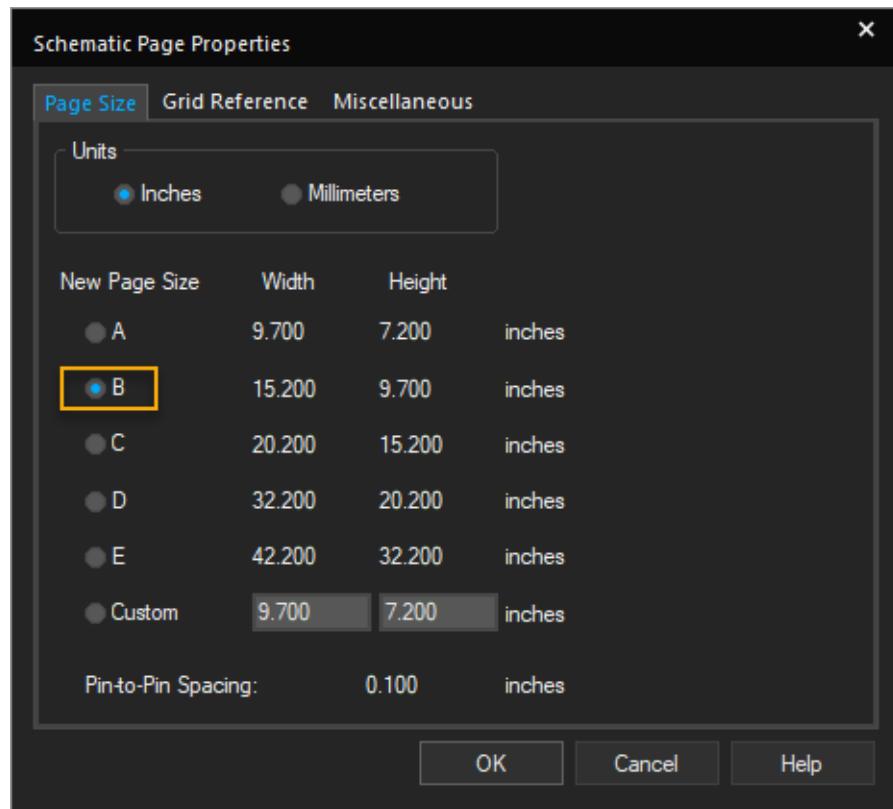
Project Manager Window



OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

10. Choose *Options – Schematic Page Properties*, and select the page size as B.



11. Click OK.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

Creating Design in Capture

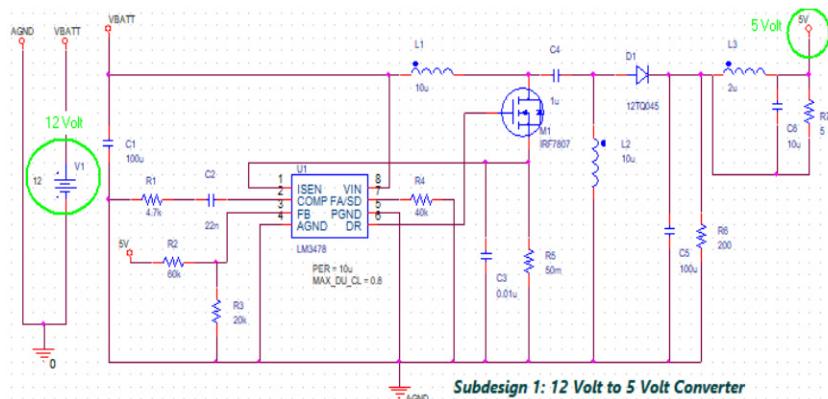
You will now create the three subdesigns of the fan module.

Subdesign No.	Instructions for subdesign creation are in the section...
1	Subdesign 1: 12 Volt to 5 Volt Converter
2	Adding Subdesign 2: 12 Volt to 3.3 Volt Converter
3	Subdesign 3: Smart Multi-Channel Switch Circuit

Subdesign 1: 12 Volt to 5 Volt Converter

Subdesign 1 consists of two parts, a 12 volt main power supply and a 12 volt to 5 volt converter as illustrated in the following image:

Subdesign 1: Main power supply and 12V to 5V converter



OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

Part 1: Creating Subdesign 1A

To create the subdesign for the main power supply, you must place the components listed in the following table:

Component	Source
DC voltage source (V1)	Place – PSpice Part – Modeling Application
Ground symbols	Place – PSpice Part – PSpice Ground
Power ports	Place – Power

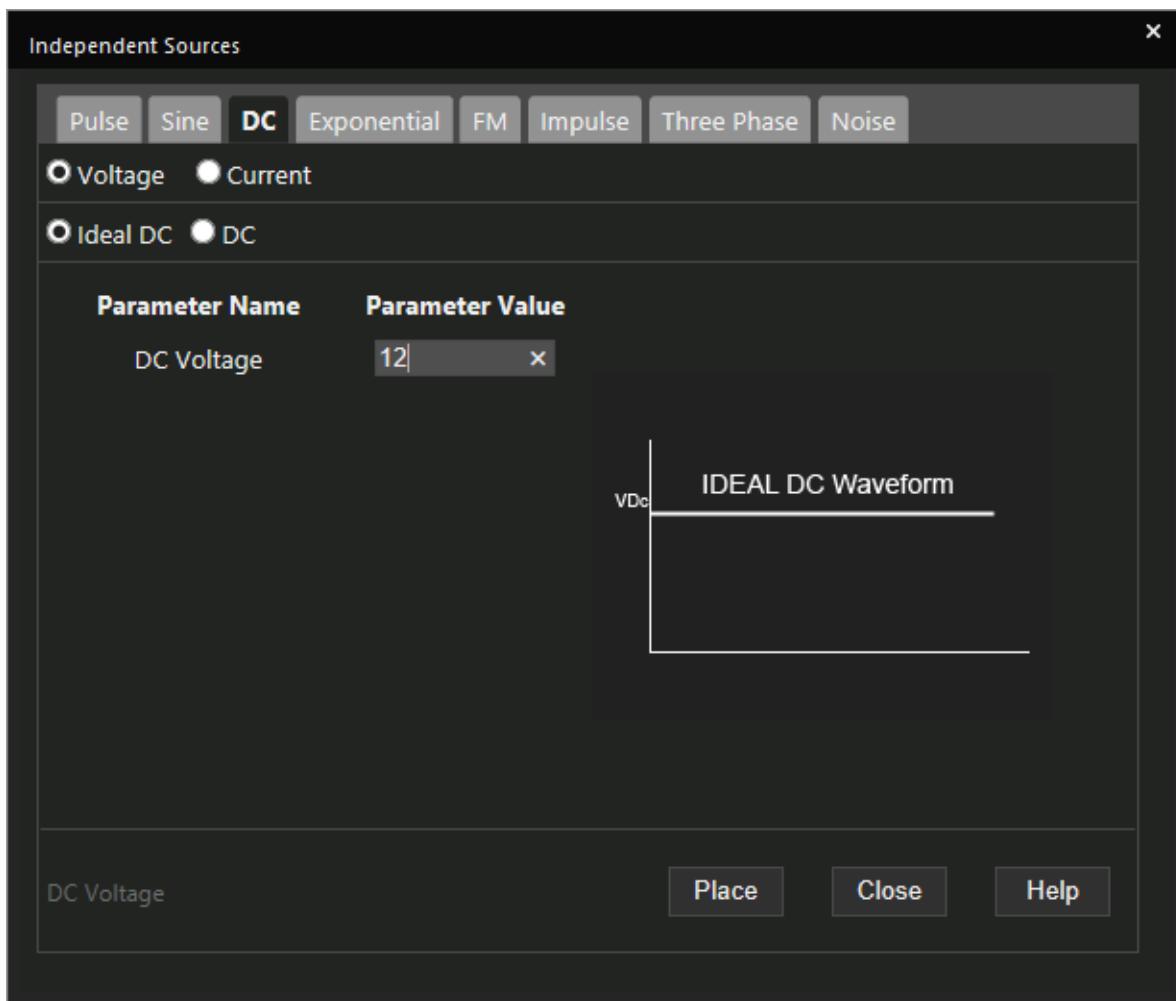
Placing Components for Subdesign 1A

1. To instantiate an ideal DC voltage source on the schematic page(SCHEMATIC1 : PAGE1), choose *Place – PSpice Part – Modeling Application*. Alternatively, click the *Modeling Application* icon () on the PSpice toolbar.
The *Modeling Application* pane opens.
2. Select *Sources – Independent Sources*.
3. Click *DC*.
4. Select *Voltage* and *Ideal DC*.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

- Specify the value of DC Voltage as 12.



- Click *Place*.

The PSpice component is attached to the cursor.

- Click to place the component on the schematic.
- To place a ground symbol, choose *Place – PSpice Part – PSpice Ground*.
- Click on the schematic page to place the part.
- Right-click and select *End Mode* or press *Esc*.

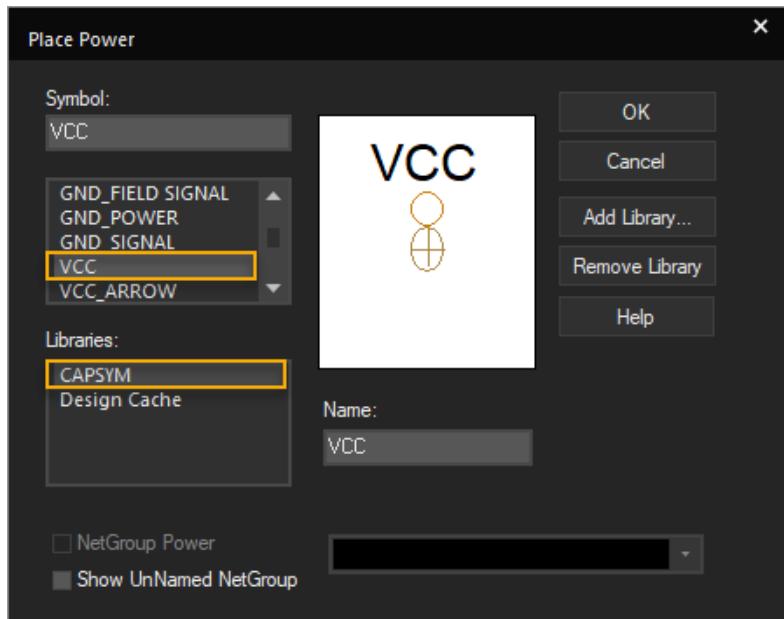
Next, you need to place a power port, VCC with its value set to VBATT, and another one with its value set to AGND from the CAPSYM library.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

To place power components, do the following:

1. Choose *Place – Power*. Alternatively, press *f* or click the *Place power (F)* icon (⊕) on the *Draw Electrical* toolbar.
2. Select CAPSYM from the *Libraries* list box.
3. Select VCC from the *Symbol* list box.

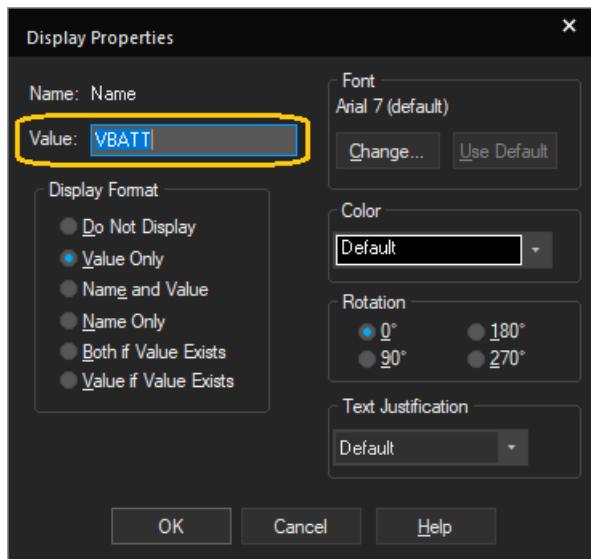


4. Click *OK*.
5. Click the schematic page to place this power port above the 12 volt DC source.
6. Press *Esc*.
7. Double-click VCC to open the *Display Properties* dialog box.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

8. Specify VBATT in the *Value* fields and click *OK*.



9. Repeat steps 1 through 7 to add another power port, VCC, and set its value to AGND.

Connecting the Components

1. Choose *Place – Wire*. Alternatively, press *w* or click the *Place wire* icon () on the *Draw Electrical* toolbar.
The cursor shape changes from pointer to cross-hair.
2. Draw the wire from the connection points of port AGND, PSpice ground, 12 volt DC voltage source, to the VBATT port as illustrated in the figure, [Subdesigns in the fan module circuit](#).

Part 2: Creating Subdesign 1B

To create the subdesign for the main power supply, you must place the components listed in the following table:

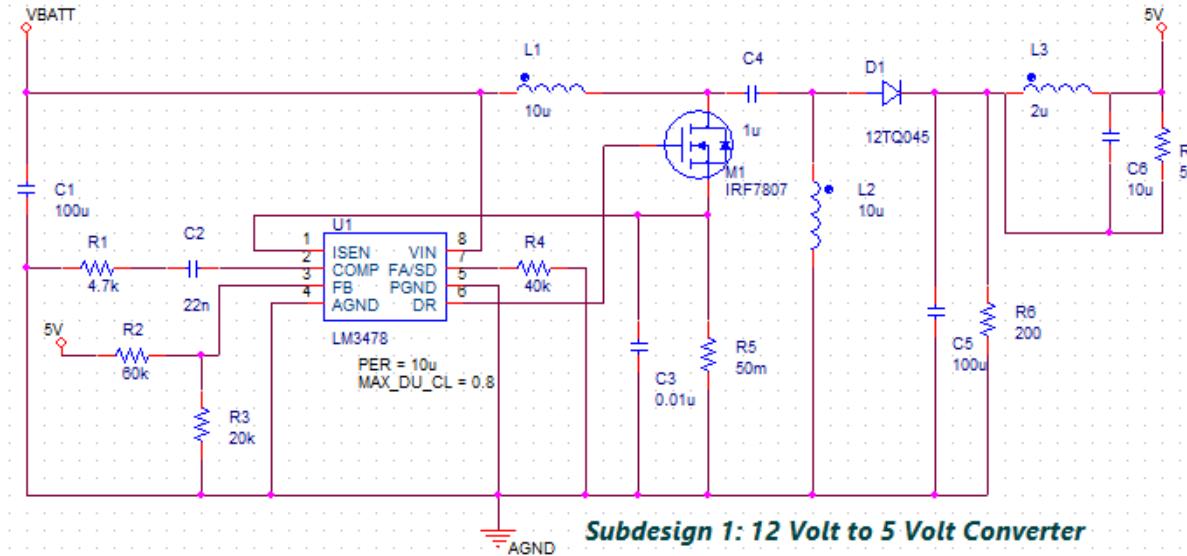
Component	Source
DC-DC converter IC LM3478	Place – Component – Component Explorer

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

Component	Source
MOSFET IRF7807	Place - Component - Component Explorer
Power ports	Place - Power
Discrete components: Capacitor, Inductor, and Resistor	Place - PSpice Part

Subdesign 1B: 12V to 5V Converter



Placing Components for Subdesign 1B

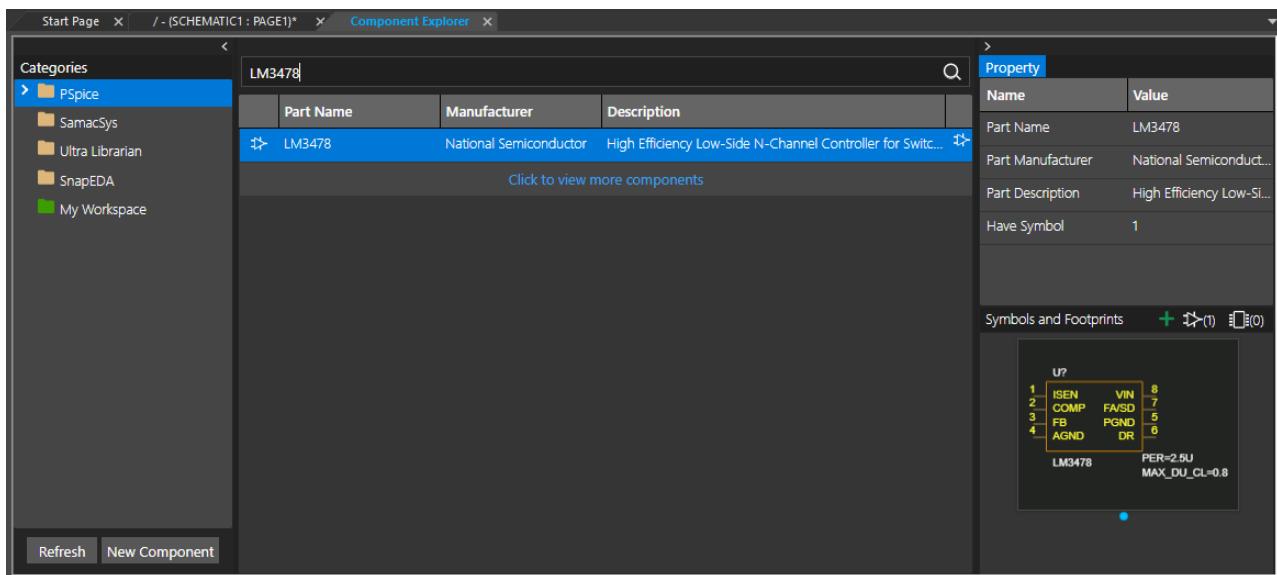
1. To place the DC-DC converter IC LM3478, choose *Place – Component*.

The *Component Explorer* interface opens. By default, the Cadence-supplied library, *PSpice*, is displayed.

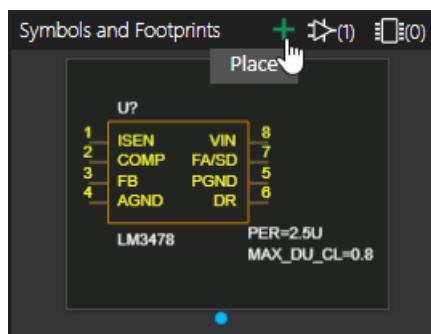
OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

- Specify LM3478 in the *Search here* text box and press *Enter* or click the magnifying lens icon.



- Double-click LM3478 in the search results. Alternatively, right-click LM3478 in the search results and choose *Place*.
You can also click the *Place* icon in the *Symbols and Footprints* bar in the right pane.



- Click the schematic page to place the converter IC.
- Right-click and select *End Mode* or press *Esc*.
- Double-click *PER* and set its value to *10u* in the *Display Properties* dialog box.
This value sets the frequency of the IC. Changing the value to *10u* ($1/10\mu = 100\text{KHz}$) sets the IC frequency to 100 KHz .
- Follow steps 2-5 to place the MOSFET, IRF7807.
- Place the VBATT and the two 5V power ports shown in subdesign 1.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

Placing Discrete Components

To place the commonly used discrete components, capacitor, inductor, and resistor, do the following:

1. Choose *Place – PSpice Part* –
 - Capacitor* to place a capacitor.
 - Inductor* to place an inductor.
 - Resistor* to place a resistor.
2. Click the schematic page to place each component and press `Esc` when done.
3. To change the value of discrete components:
 - a. Double-click their value to open *Display Properties* window.
 - b. In the *Value* field, specify the required value of the discrete component.
 - c. Click *OK*.

For reference, see [Example - Placing the 100u Capacitor, C1](#).

4. Similarly, add other discrete components as specified in the following table:

PSpice Part Name	PSpice Part Value
C2	22n
R1	4 . 7k
R2	60k
R3	20k
R4	40k
L1	10u
C3	0 . 01u
C4	1u
R5	50m
L2	10u
C5	100u
R6	200

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

PSpice Part Name	PSpice Part Value
L3	2u
C6	10u
R7	5

5. Search for 12TQ045 diode in the *PSpice* node in Component Explorer and place it on the schematic.
6. Place the AGND port on the schematic.

Example - Placing the 100u Capacitor, C1

1. Choose *Place – PSpice Part – Capacitor*.
2. Click the schematic page to place the capacitor C1 below the VBATT port as shown in the figure, [Circuit for smart multi-channel switch, TLE8110EE](#)
3. Right-click and choose *End Mode* or press *Esc*.
4. Double-click the value, 1n.
The *Display Properties* dialog box opens.
5. In the *Value* field, specify the value of C1 as 100u.
6. Click *OK*.

Connecting all the Components in Subdesign 1

1. Draw a wire from pin 1 of LM3478 to the source of MOSFET M1, IRF7807.
2. Draw a wire from pin 6 LM3478 to the gate of MOSFET M1, IRF7807.
3. Draw a wire from 10u inductor, L1 to the drain of MOSFET M1, IRF7807.
4. Similarly, add wires to the subdesign 1 until all the components are connected as shown in the figure, [Subdesign 1B: 12V to 5V Converter](#).

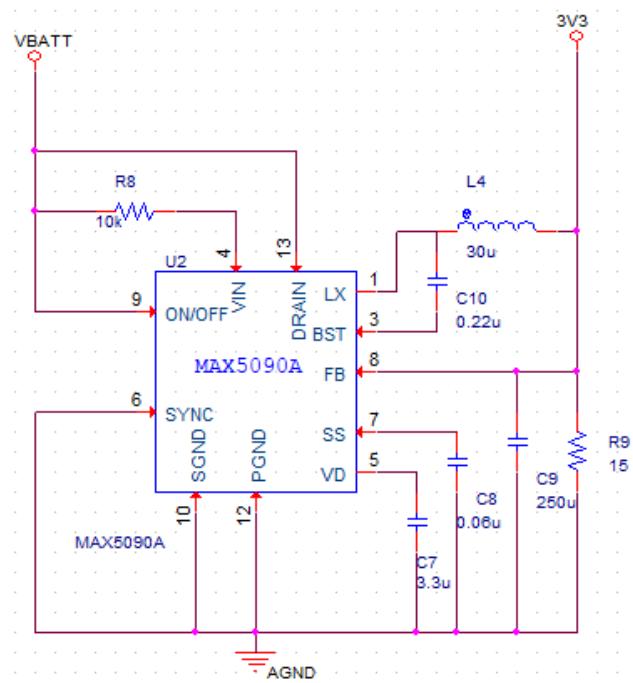
OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

Subdesign 2: 12 Volt to 3.3 Volt Converter

The subdesign 2 of the fan module uses the IC, MAX5090A, which is a DC-DC converter that is down converting 12 volt to 3.3 volt. The output of 3.3 volt powers the fan.

Circuit for 12 Volt to 3.3 Volt converter



Subdesign 2: 12 Volt to 3.3 Volt Converter

Creating Subdesign 2

To create subdesign 2, you must place the following components as listed in the following table:

Component	Source
DC-DC converter MAX5090A	Place - Component - Component Explorer
Ground symbols	Place - PSpice Part - PSpice Ground
Power ports	Place - Power

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

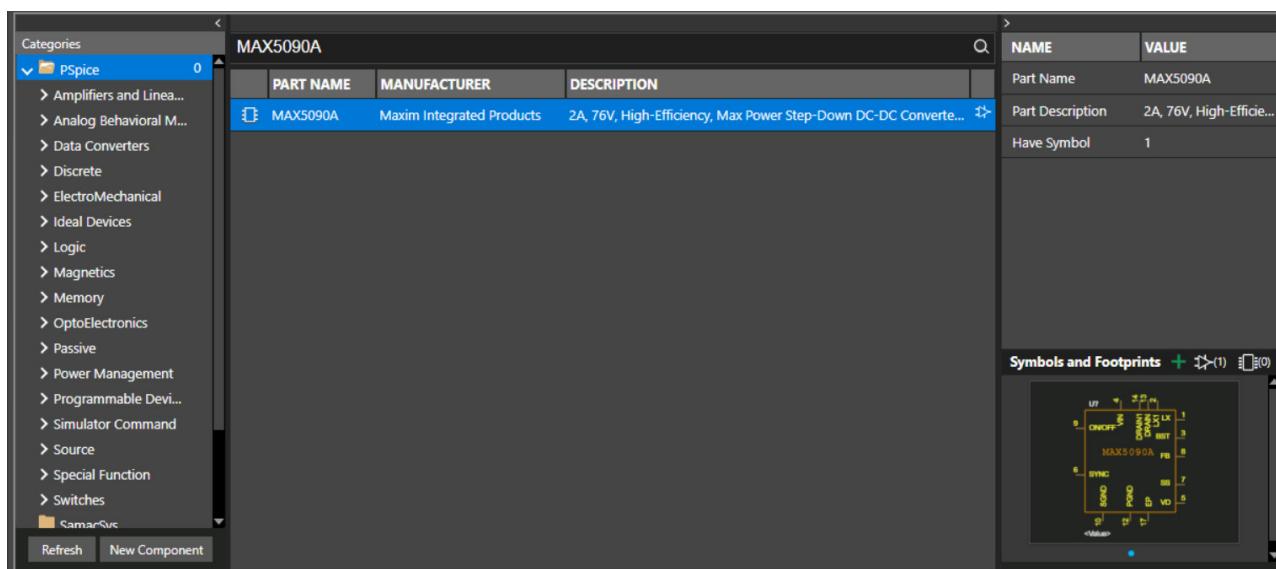
Component Placement for Subdesign 1A

1. To place the DC-DC converter, MAX5090A.

- a. Choose *Place – Component*.

In the *Component Explorer* interface, the *PSpice* node is selected by default in the *Categories* pane.

- b. Specify MAX5090A in the *Search here* text box and press *Enter* or click the magnifying lens icon.



- c. Double-click MAX5090A in the search results.

- d. Click the schematic page to place the component and press *Esc*.

2. Place the VBATT, AGND, and 3V3 power ports shown in figure, [Circuit for 12 Volt to 3.3 Volt converter](#).
3. Place the remaining discrete components in figure, [Circuit for 12 Volt to 3.3 Volt converter](#)) and specify their values from the following table:

PSpice Part Name	PSpice Part Value
L4	30u
C10	0.22u
R8	10k

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

PSpice Part Name	PSpice Part Value
C7	3.3u
C8	0.06u
C9	250u
R9	15

4. Right-click C8 and choose *Edit Properties*.
5. Set the value of *IC* as 0.
6. Add wires to the subdesign 2 until all components are connected as shown in figure,
[Circuit for 12 Volt to 3.3 Volt converter](#).

OrCAD X Capture with OrCAD X Presto Tutorial

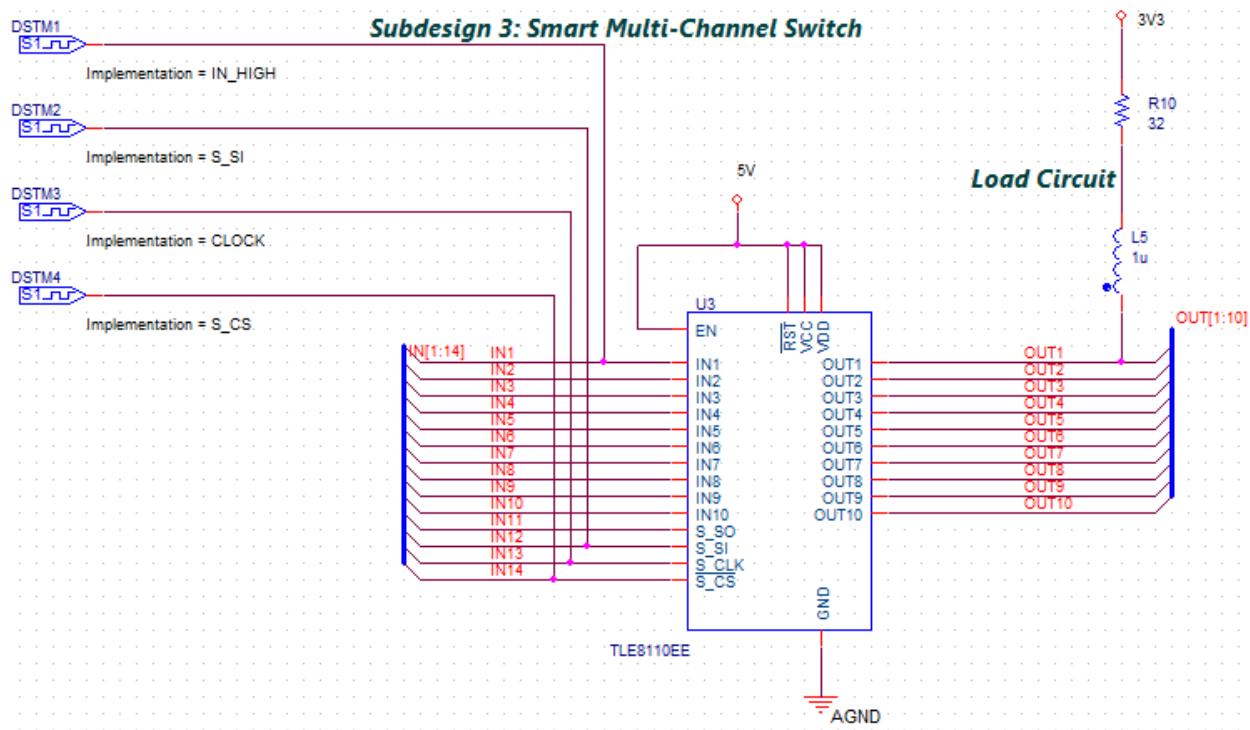
Creating a Schematic Design

Subdesign 3: Smart Multi-Channel Switch Circuit

In subdesign 3, you will create the circuit for a smart multi-channel switch as shown in figure, Circuit for smart multi-channel switch, TLE8110EE.

In this subdesign an IC, TLE8110EE is placed to be interfaced with an off-board micro-controller. The input to the 10 channels of this IC are digital signals generated from a micro-controller. For this tutorial, these digital signals are modeled using digital stimulus sources.

Circuit for smart multi-channel switch, TLE8110EE



Creating Subdesign 3

To create the subdesign 3, you must place the following components as listed in the following table:

Component	Source
IC TLE8110EE	Place - Component - Component Explorer

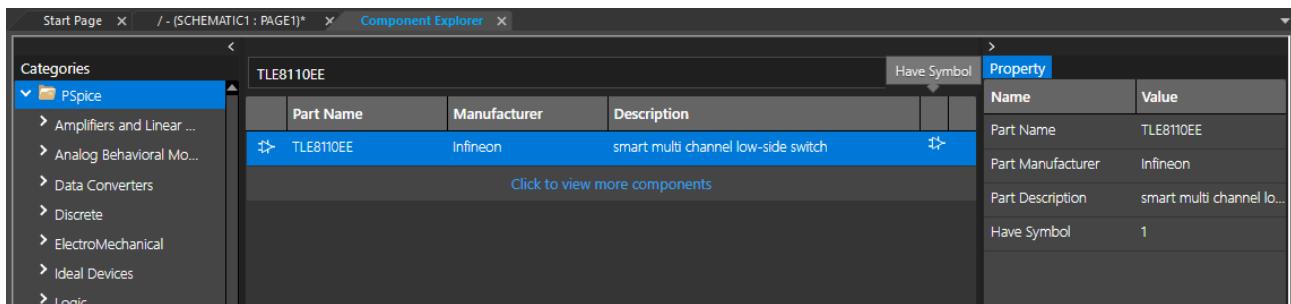
OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

Component	Source
Ground symbols	Place - PSpice Part - PSpice Ground
Power ports	Place - Power
Discrete components: Inductor and Resistor	Place - PSpice Part
Digital stimulus DIGSTIM1	Place - Component - Component Explorer

Component Placement for Subdesign 3

1. Place the IC, TLE8110EE from the *PSpice* node of the Component Explorer interface.



2. Place the AGND, 5V, and 3V3 power ports shown in figure, [Circuit for smart multi-channel switch, TLE8110EE](#).
3. Place the discrete components as shown in figure, [Circuit for smart multi-channel switch, TLE8110EE](#) and specify their values from the following table:

PSpice Part Name	PSpice Part Value
R10	32
L5	1u

This resistor forms the RL circuit for the fan type of load.

This inductor forms the RL circuit for the fan type of load.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

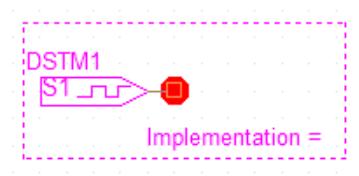
4. Place the digital stimulus sources from the *PSpice* node in the *Component Explorer* interface.

These are 1-bit digital stimulus sources.

To add these, search for `DIGSTIM1` in the *PSpice* node of *Component Explorer* and select `DigStim1` from the results.

DIGSTIM1			
	PART NAME	MANUFACTURER	DESCRIPTION
	DigStim1	PSpice	1 Bit Digital Stimulus Source for StmEd
	DigStim16	PSpice	16 Bit Digital Stimulus Source for StmEd

5. Double-click the `Implementation` property of a digital stimulus source.



The *Display Properties* dialog box opens.

6. In the `Value` field, specify the value of this `Implementation` property as shown in the following table:

Digital Stimulus Source Name	Value of Implementation property
DSTM1	IN_HIGH
DSTM2	S_SI
DSTM3	CLOCK
DSTM4	S_CS

Note: The stimulus data from these sources is read from a `.stl` file.

Placing and Connecting Buses

1. Select *Place – Bus* or press **B**. Alternatively, click the *Place bus* icon () on the *Draw Electrical* toolbar.

OrCAD X Capture with OrCAD X Presto Tutorial

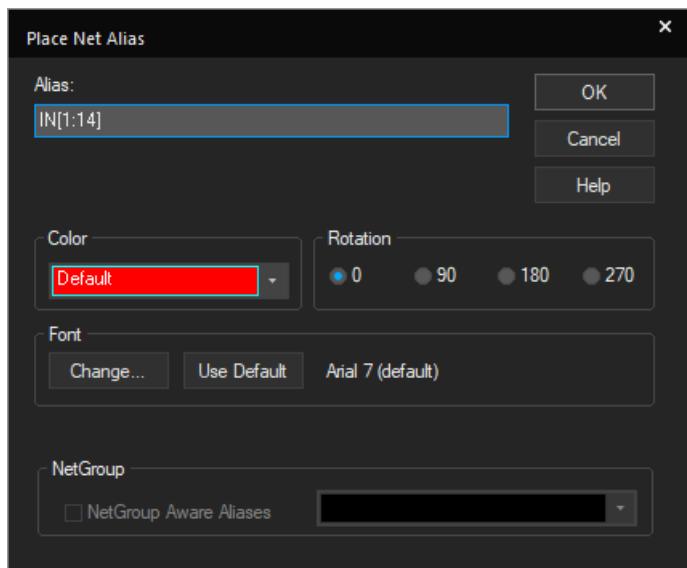
Creating a Schematic Design

The cursor shape changes from pointer to cross-hair.

2. Draw the bus before the input pins and after the output pins of TLE8110EE as shown in figure, [Placing Buses](#).
3. Select *Place – Net Alias* or press **N**. Alternatively, click the *Place net alias* icon () on the *Draw Electrical* toolbar.

The *Place Net Alias* dialog box appears.

4. Specify the value in the *Alias* field as `IN[1:14]`.

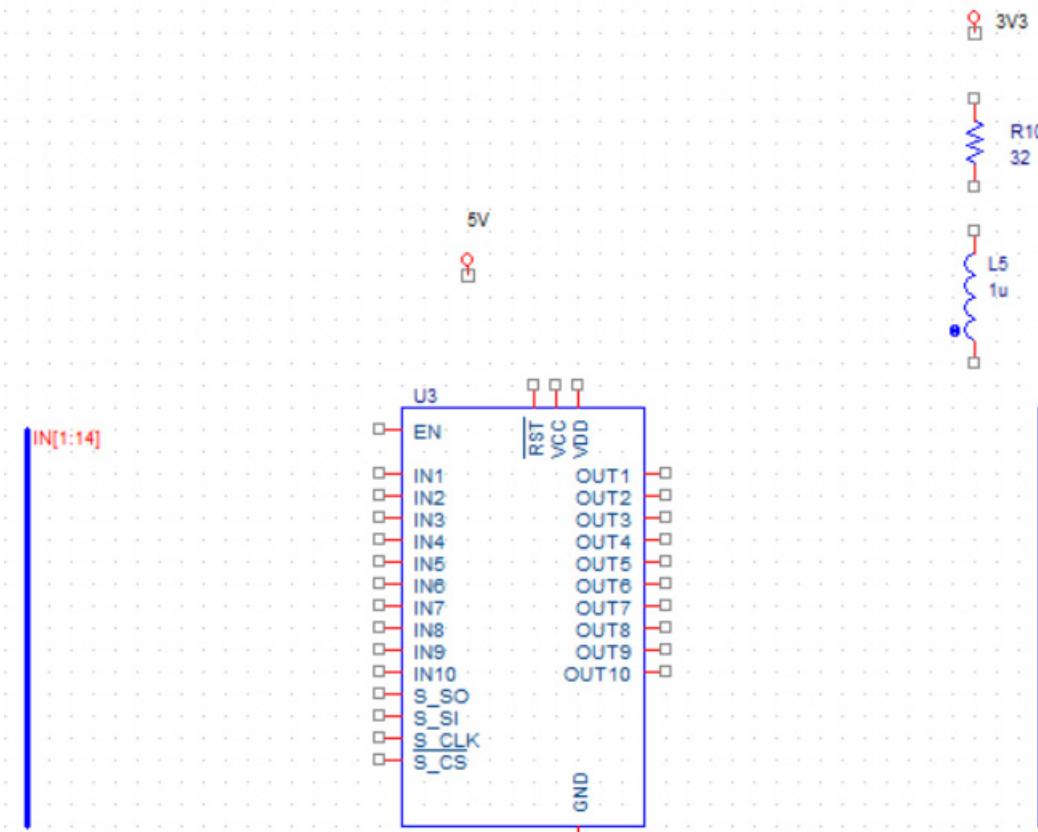


5. Click **OK**.
6. Move the cursor on the bus and place the net alias name as shown in the following figure:

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

Placing Buses

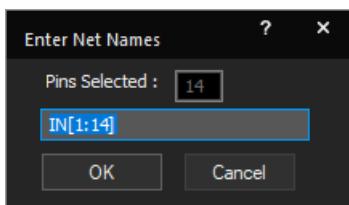


7. Select all the input pins of TLE8110EE (except EN), right-click the selection, and choose *Connect to Bus*.

The cursor shape changes from pointer to cross-hair.

8. Click the bus placed before the input pins.

The *Enter Net Names* dialog box appears.



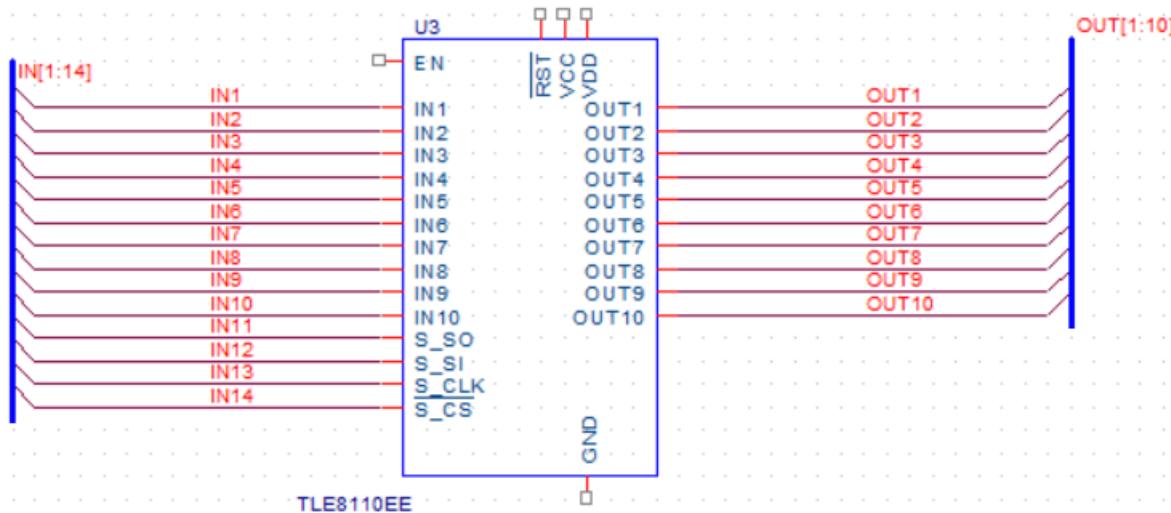
9. Click *OK*.

Net names appear on each net from the input pins to the bus.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

10. Repeat steps 3 to 10 to place the OUT [1:10] net alias on the bus placed next to the output pins of TLE8110EE, and to connect the output pins of TLE8110EE to this bus as shown in the following figure:



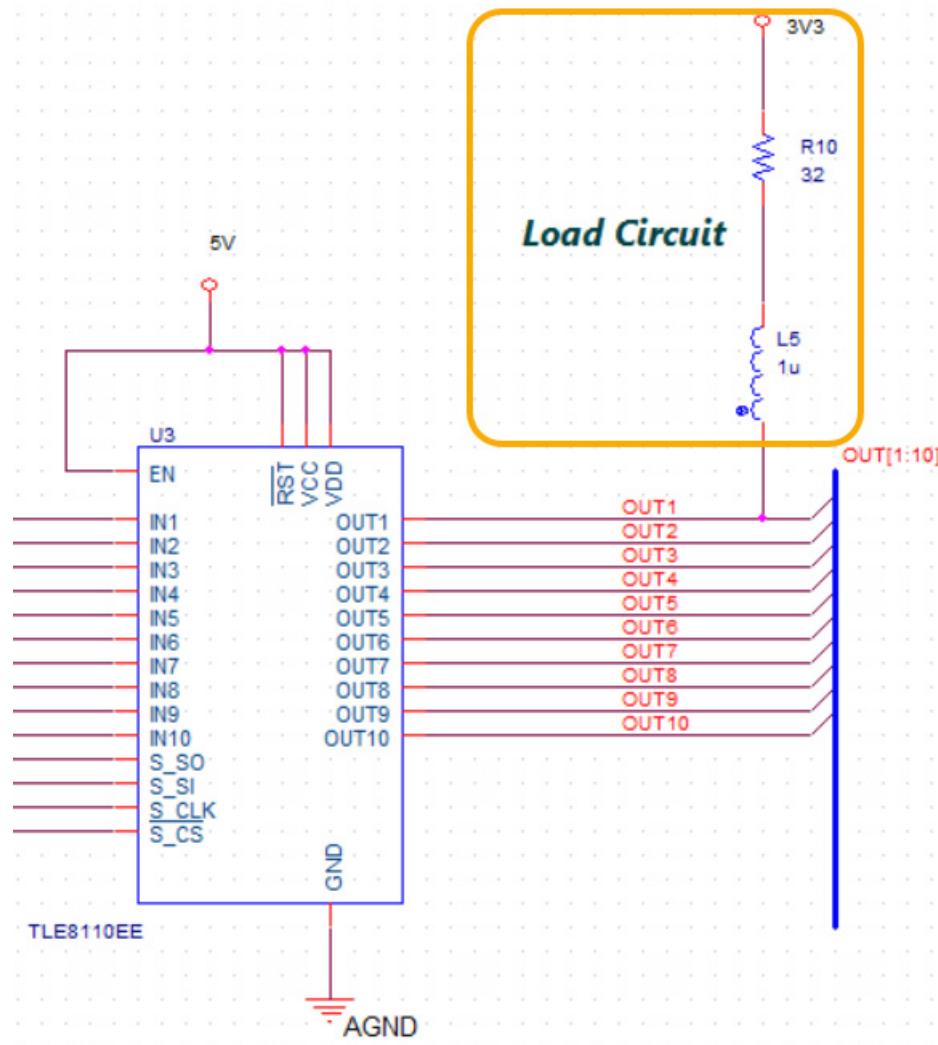
Connecting Components of Subdesign 3

1. Draw a wires from the pins, RST, VCC, and VDD to the 5V power port.
2. Draw a wire from the 5V power port to the input pin, EN of TLE8110EE.
3. Draw a wire from the GND pin to the power port, AGND.
4. Draw a wire from the output pin of:
 - DSTM1 (with implementation=IN_HIGH) to net IN1.
 - DSTM2 (with implementation=S_SI) to net IN12.
 - DSTM3 (with implementation=S_CLK) to net IN13.
 - DSTM4 (with implementation=S_CS) to net IN14.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

5. Connect the load circuit to the net, OUT1 as shown in the following figure:



Summary

This section covered the steps to create a schematic design using Capture CIS. In the process, you were introduced to some of the basic design creation tasks, such as creating a project, placing parts, editing property values, and connecting parts.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Schematic Design

Simulating a Design

In this section, you will use PSpice to simulate the design created in the previous section using Capture CIS. You will also learn about transient analysis that is performed using PSpice.

Getting the Design Ready for Simulation

To simulate a design, the PSpice simulator needs information about circuit topology, analysis type, and stimulus definitions.

The analysis type, stimulus definition, and the information related to the initial digital state of the simulation is provided by a simulation profile (*.SIM). In the following section, you will create a simulation profile.

Creating a Stimulus File

Before creating the simulation profile, you need to specify the stimulus definition to be used for simulating the circuit. For this, you need to create a stimulus file and then specify its location in the *Simulation Setting* dialog box to create the simulation profile.

- To create the stimulus file, copy the following information in a text editor (.txt) file and save it as `stimulus.stl`.

```
.STIMULUS IN_HIGH STIM (1, 1)
+ 0 0
+ +0 1

.STIMULUS S_SI STIM (1, 1)
+0ms 0
+808.400000000u 0
+ +200ns 1
+ +200ns 1
+ +200ns 1
+ +200ns 0
+ +200ns 0
+ +200ns 0
+ +200ns 1
+ +200ns 0
+ +200ns 0
+ +200ns 1
+ +200ns 0

.STIMULUS CLOCK STIM (1, 1)
+ 0 0
+ +0 1
+REPEAT FOREVER
+ +100n 0
+ +100n 1
+ ENDREPEAT

.STIMULUS S_CS STIM (1, 1)
+0u 0
+807.763636u 1
+808.333363636u 0
+811.56335227u 1
```

OrCAD X Capture with OrCAD X Presto Tutorial

Simulating a Design

```
+812.13370351u 0
```

Creating a New Simulation Profile

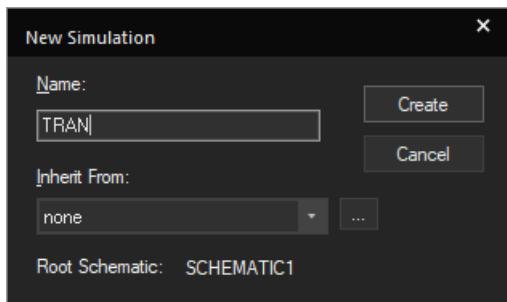
To view the behavior of this circuit over time, transient analysis will be used. To perform this analysis, you will specify this analysis type when creating the simulation profile.

To create a new simulation profile, do the following:

1. Choose *PSpice – New Simulation Profile*, or click the *New Simulation Profile* icon on the PSpice toolbar.

The *New Simulation* dialog box opens.

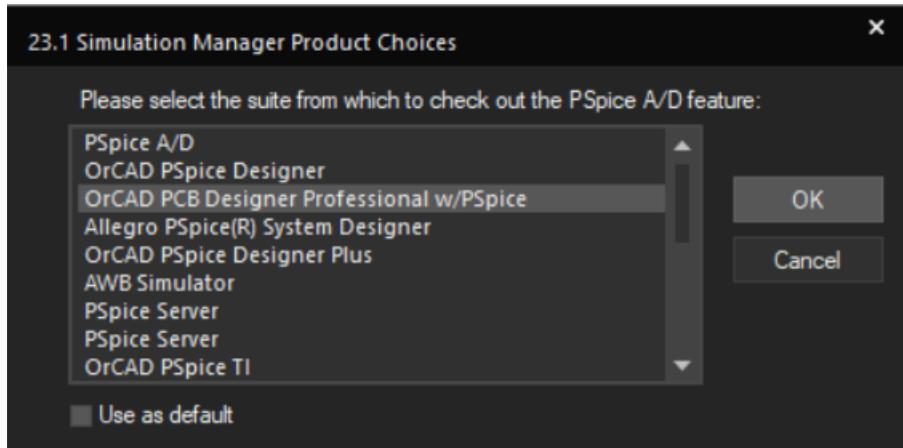
2. Specify the name of the new simulation profile as **TRAN**.
3. In the *Inherit From* drop-down list, ensure that **none** is selected and click *Create*.



4. In the product choices dialog box, select the *OrCAD PCB Designer Professional w/ PSpice* option and click *OK*.

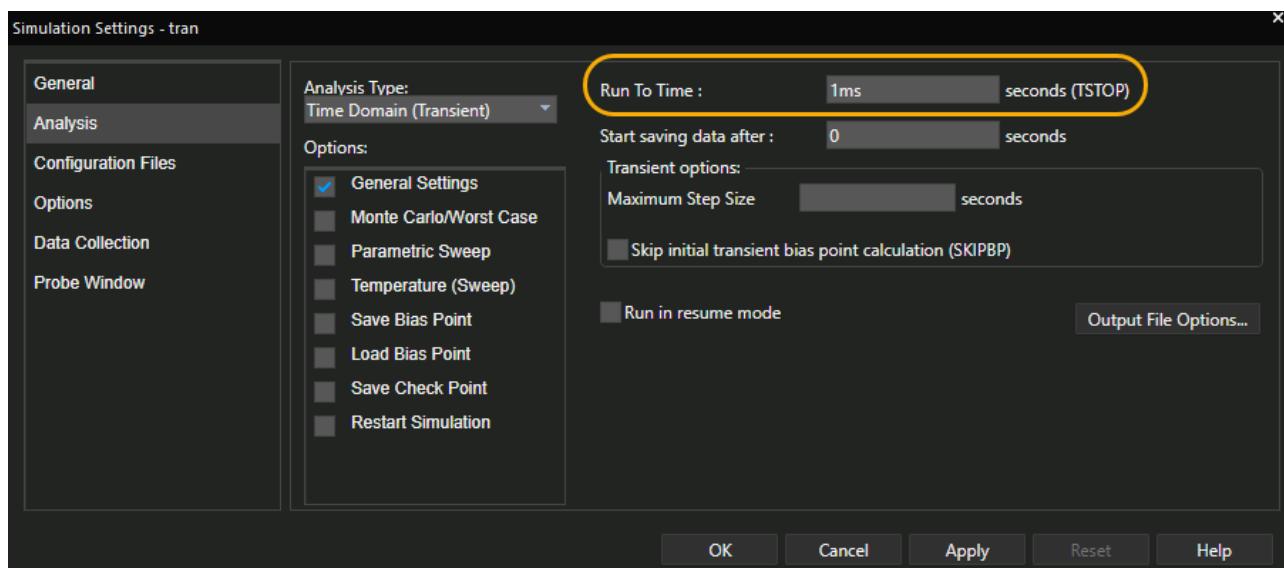
OrCAD X Capture with OrCAD X Presto Tutorial

Simulating a Design



The *Simulation Setting* dialog box appears with the *Analysis* tab selected.

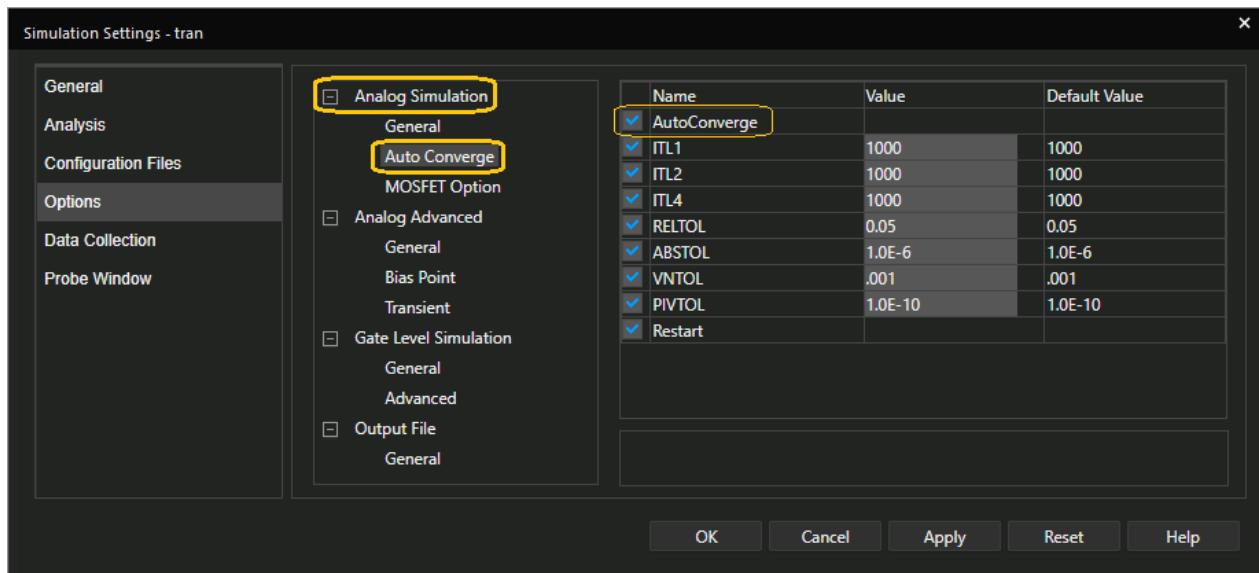
5. In the *Analysis Type* drop-down list, Time Domain (Transient) is selected by default. Retain this default setting.
6. To run a transient analysis, specify time as 1ms in the *Run To Time* text box.



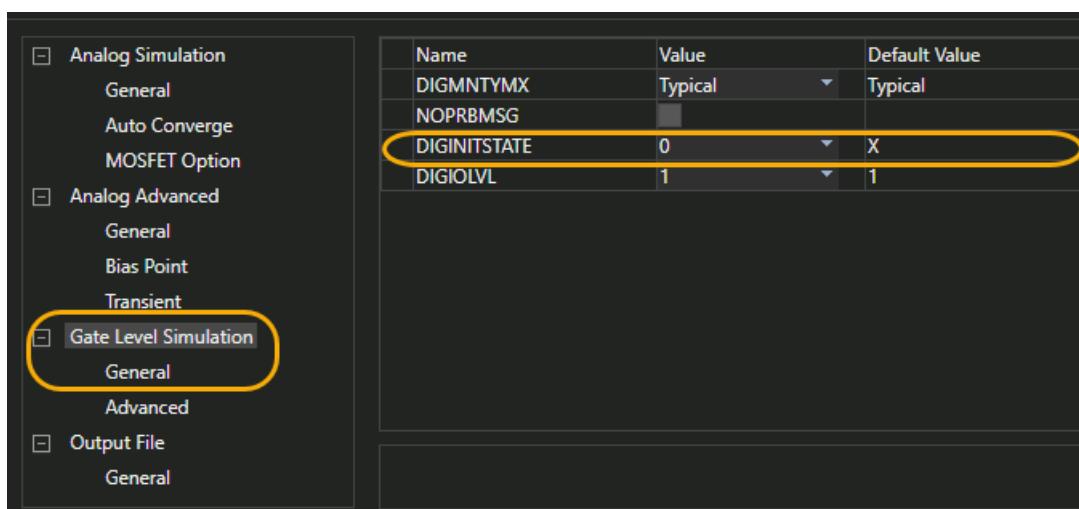
OrCAD X Capture with OrCAD X Presto Tutorial

Simulating a Design

7. To prevent any convergence issues, in the *Options* tab, select the *Auto Converge* check box under Analog Simulation.



8. To set the initial digital state of the simulation to 0, click *Gate Level Simulation* and set *DIGINISTATE* as 0.

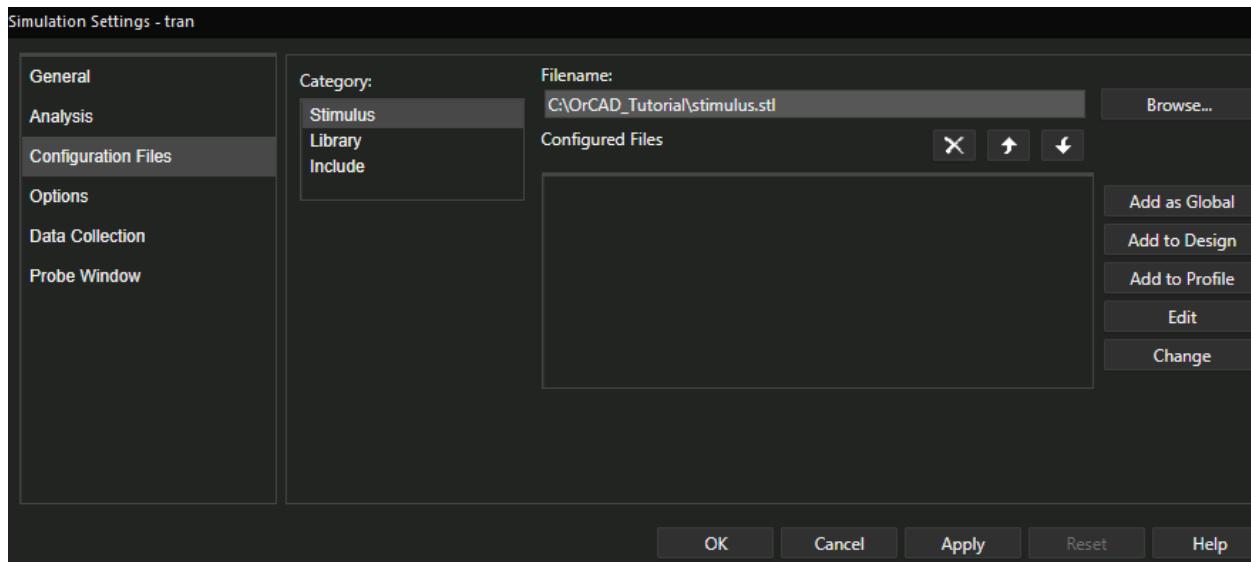


9. In the *Configuration Files* tab, select *Stimulus* from the *Category* list.

OrCAD X Capture with OrCAD X Presto Tutorial

Simulating a Design

10. Click the *Browse* button to navigate to the `stimulus.stl` file and click *Open*.



11. Click the *Add to Design* button.

12. Click *OK* to save your modifications.

When the simulation is run from the schematic, the simulator reads the SPICE models connectivity information (netlist) from the design files, and the analysis type and the stimulus details from the simulation profile.

Running the Simulation

- To simulate the design, choose *PSpice – Run* or click the *Run PSpice* icon.

The Schematic1-TRAN - PSpice window opens.

Viewing Output Waveforms

To visualize the circuit behavior and determine the validity of your circuit design, you can plot the output waveforms in the *Probe* window. By analyzing the output waveforms you can evaluate your circuit for performance.

For PSpice to display output waveforms in the *Probe* window, you need to place markers in your circuit design in Capture to indicate the points where you want to see simulation waveforms displayed in PSpice.

Markers can be placed:

- before simulation to limit results written to the waveform data file, and automatically display those traces in the active *Probe* window.
- during or after simulation, to automatically display traces in the active *Probe* window.
- To add markers, choose *PSpice – Markers* or use the icons provided on the PSpice toolbar.



To view the markers in the simulation results, the schematic design must be open.

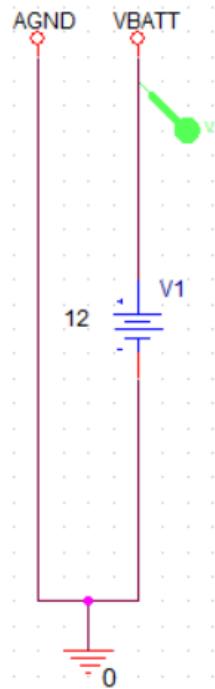
You will now add voltage markers to view the output waveforms in the *Probe* window. To do so:

1. Select *PSpice – Markers – Voltage Level*, or click the *Voltage/Level Marker* icon on the PSpice toolbar.

OrCAD X Capture with OrCAD X Presto Tutorial

Simulating a Design

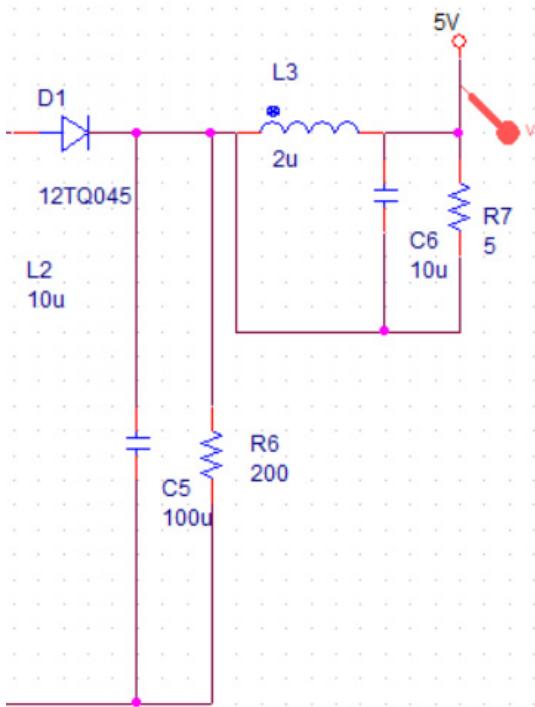
2. Place the marker at the main power supply, that is at the 12 Volt VBATT power net.



OrCAD X Capture with OrCAD X Presto Tutorial

Simulating a Design

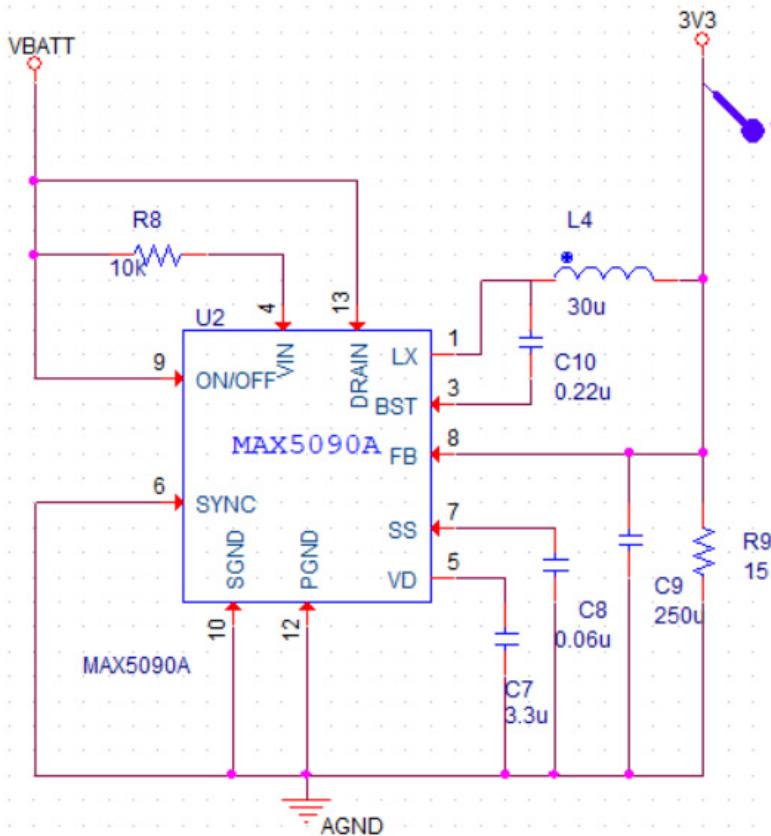
3. Place the marker at the end of the first subdesign (12V to 5V converter) at the 5V power net, as shown in the following figure:



OrCAD X Capture with OrCAD X Presto Tutorial

Simulating a Design

4. Place another voltage marker at the end of the third subdesign (12V to 3.3V converter), at the 3V3 power net, as shown in the following figure:



Note: If you add markers before simulating the design, the output waveforms are displayed automatically in the *Probe* window after the simulation is complete.

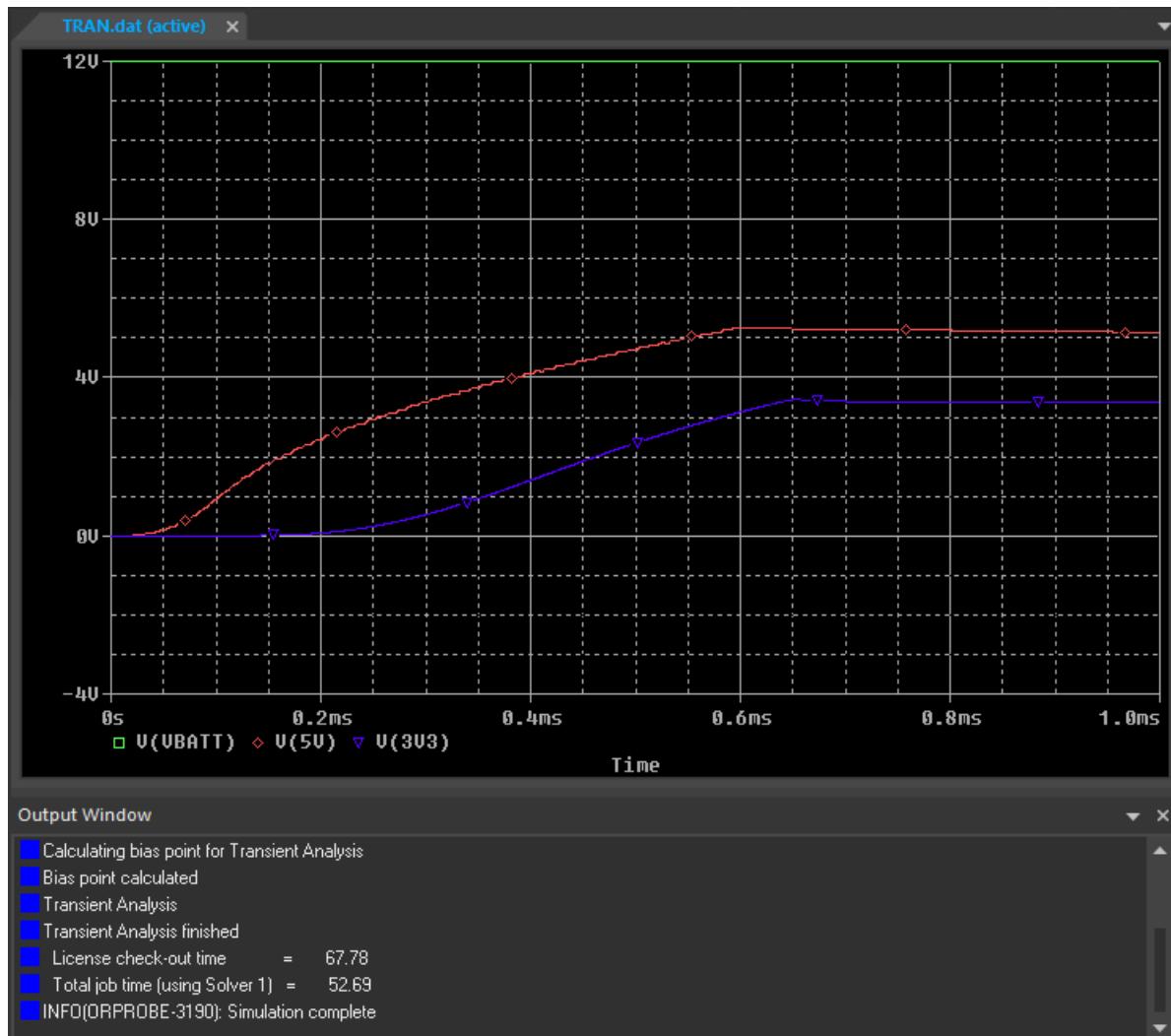
5. Switch to the *Probe* window to view the output waveform.

The output waveform appears as shown in the following figure:

OrCAD X Capture with OrCAD X Presto Tutorial

Simulating a Design

Output Waveform - Probe window



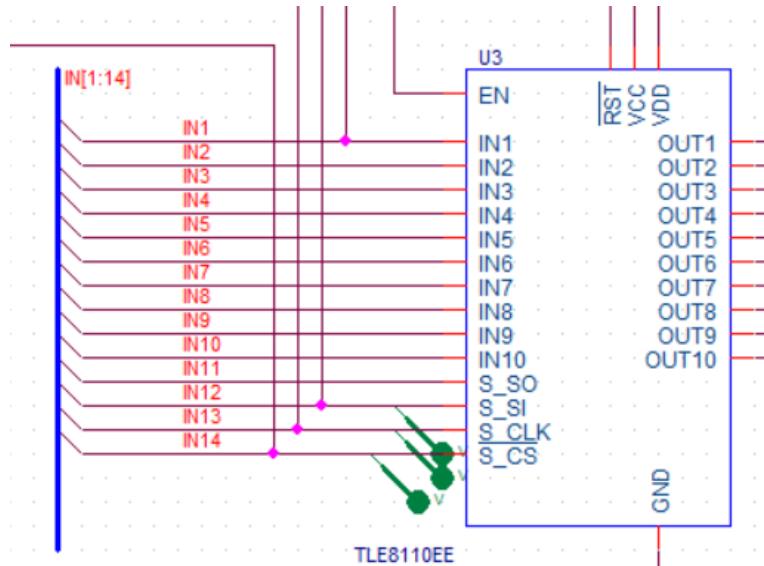
6. To view the waveform of the digital stimulus sources at the input of the switching IC TLE8110EE, place voltage markers on the following nets:

- IN12 (connected to pin S_SI)
- IN13 (connected to pin S_CLK)

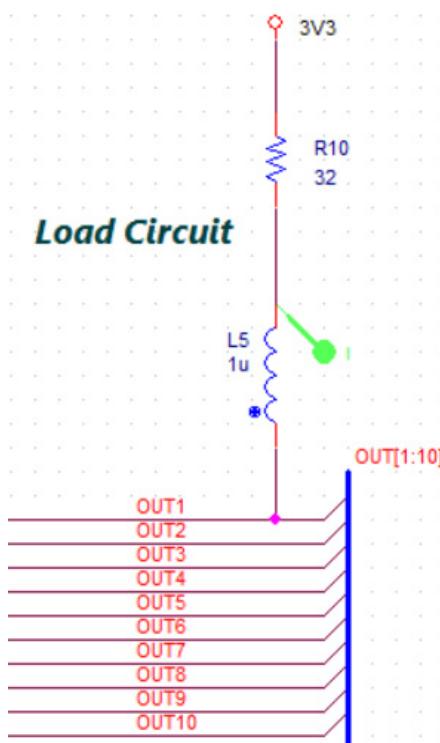
OrCAD X Capture with OrCAD X Presto Tutorial

Simulating a Design

- IN14 (connected to pin S_CS)



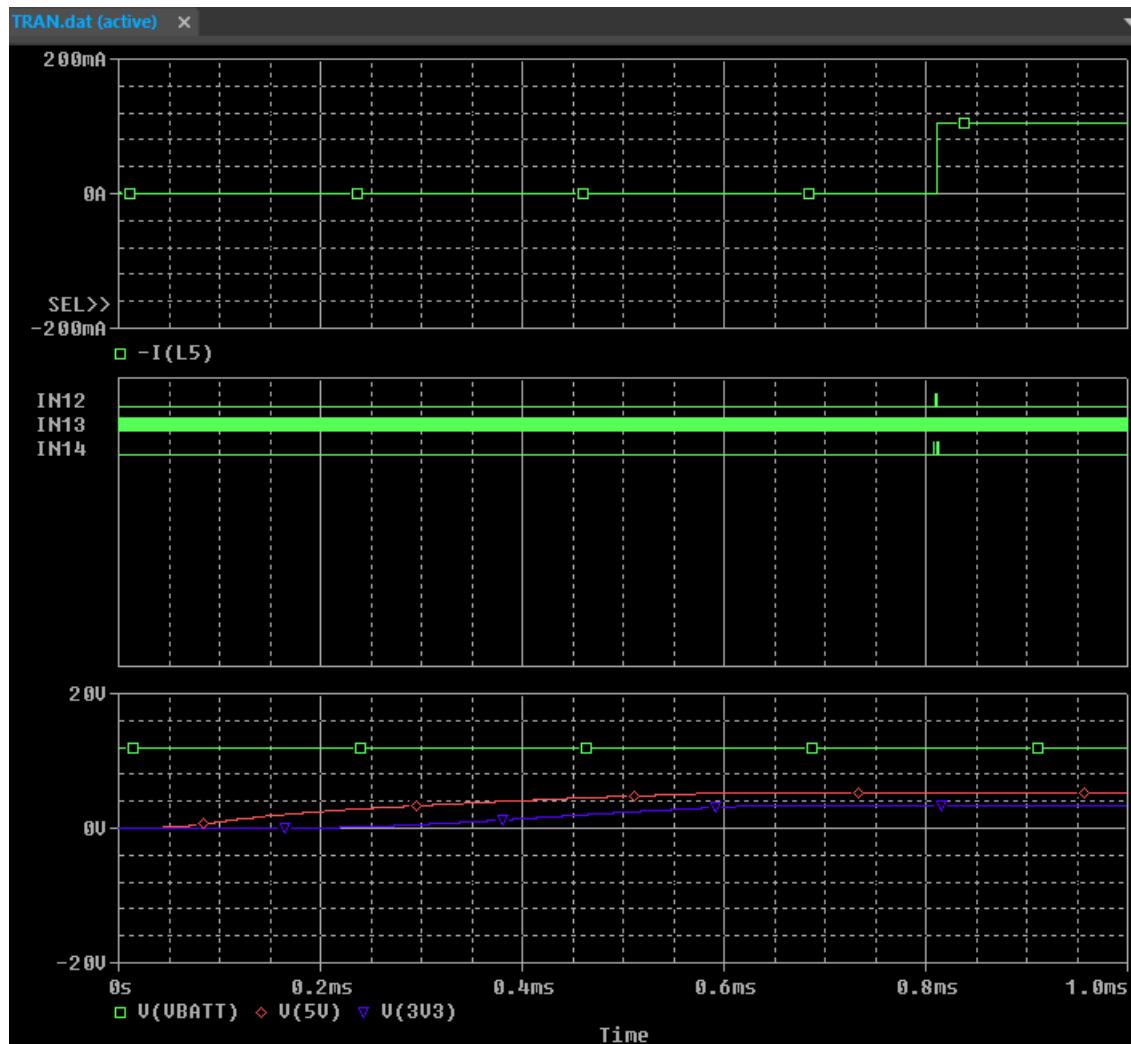
7. In PSpice, select *Plot – Add Plot to Window*.
8. In Capture, place a current marker (using the *Current Marker* icon on the pin of the inductor as shown in the following figure):



OrCAD X Capture with OrCAD X Presto Tutorial

Simulating a Design

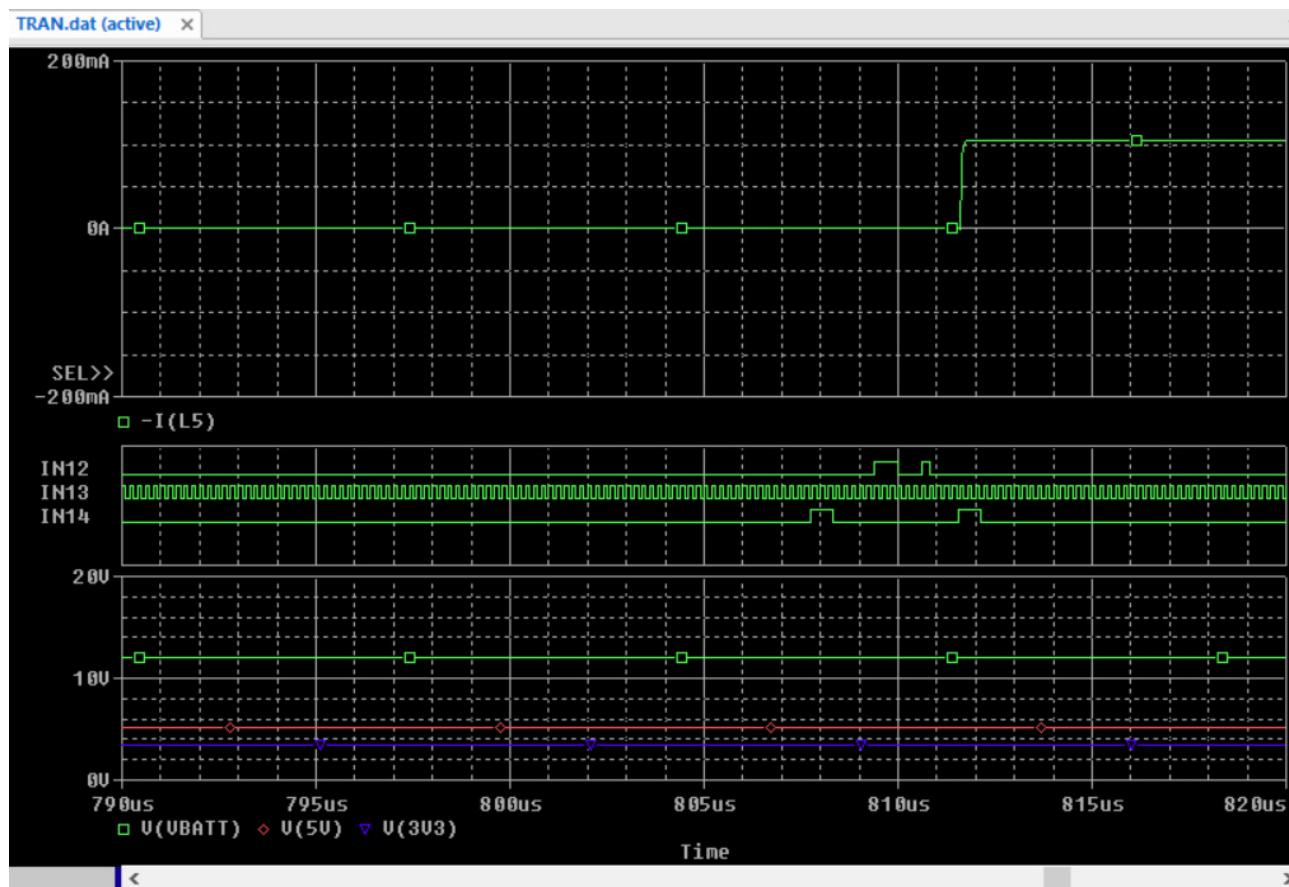
The changes in the waveform are displayed in the following figure:



OrCAD X Capture with OrCAD X Presto Tutorial

Simulating a Design

The command to turn on the fan is sent to the `S_SI` pin. This command is read and executed at the low to high transition of the `S_CS` signal. The input signal through the `S_SI` pin is sent from the duration `808us` to `811us`, as shown in the following figure:



Summary

This section covered the steps to simulate the fan module design using PSpice. In this section, you were introduced to various tasks involved in the simulation process, such as creating a simulation profile, running simulation, placing markers, and analyzing simulation results.

Preparing for PCB Layout Creation

Now that you have verified the performance of your logical circuit through simulations, you can start designing the physical layout of the PCB board for this schematic design.

Before you create the PCB layout, you need to ensure that the design has no open or unconnected signals, footprint information is available for all components, and electrical constraints, if any, are specified.

Adding and Placing Connectors

To connect the fan module with a system, connector components are required to be placed in the schematic design.

To add and place connectors in this schematic design, do the following:

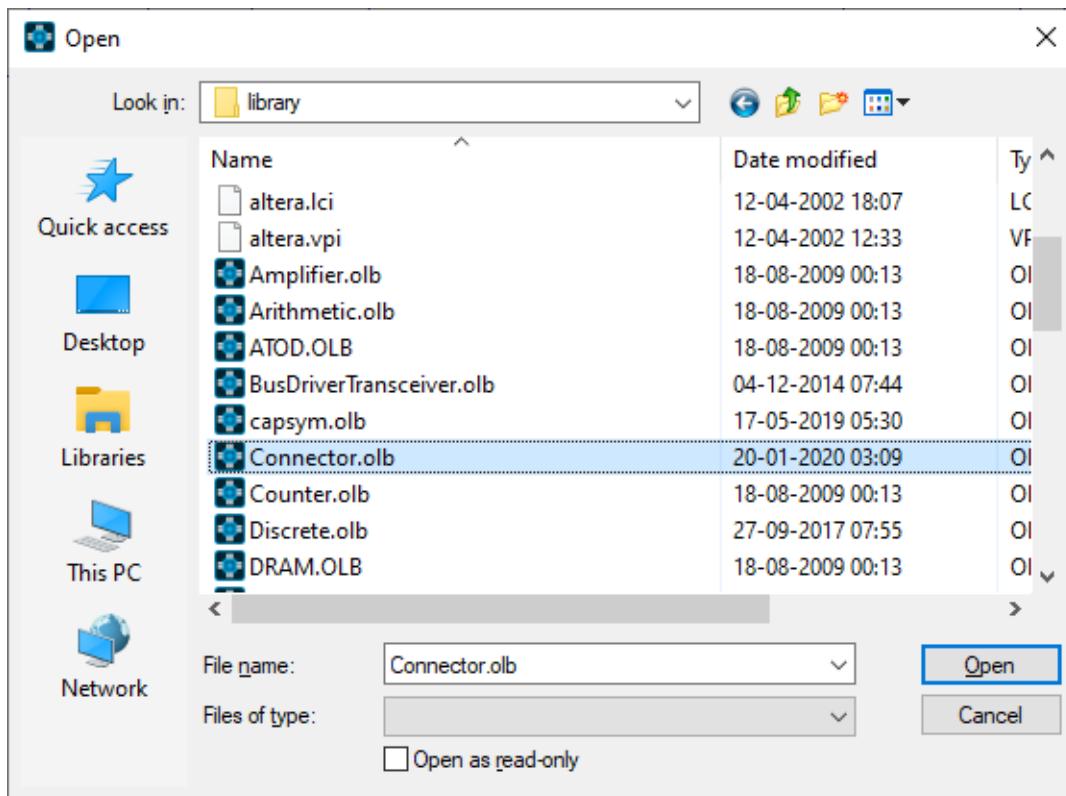
1. Open your Capture CIS design.
2. Select *Place – Part*, press *P*, or click the Place part icon ().
The *Place Part* pane opens.
3. To add *Connector.olb* to the project, click the *Add Library* icon ().
The *Browse File* dialog box opens.

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

4. Browse to

`<installation_directory>\tools\capture\library\Connector.olb.`



5. Select Connector.olb and click Open.

The CONNECTOR library appears in the *Libraries* list box.

6. Search for CON2_M from the *Part* list box.

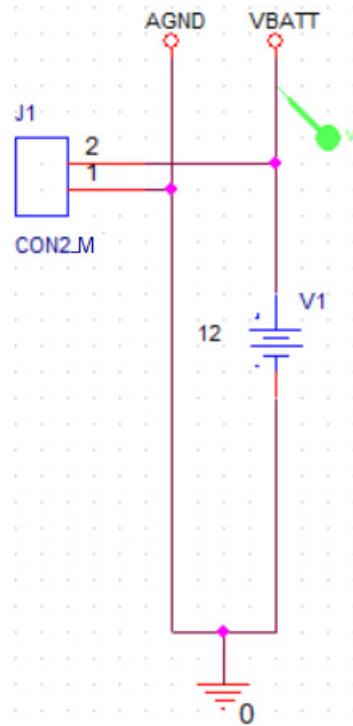
7. Click the *Place Part* icon () or press Enter.

The part symbol is attached to the cursor.

8. Click the schematic page where you have placed the 12 volt DC source and place the connector J1 and press Esc.

9. Right-click this connector and select *Rotate* and then connect it as shown in figure, Connector at the main power supply.

Connector at the main power supply



Similarly, add a 14-pin connector (CON14_M) to the input and output channels of the smart multi-channel switch IC.

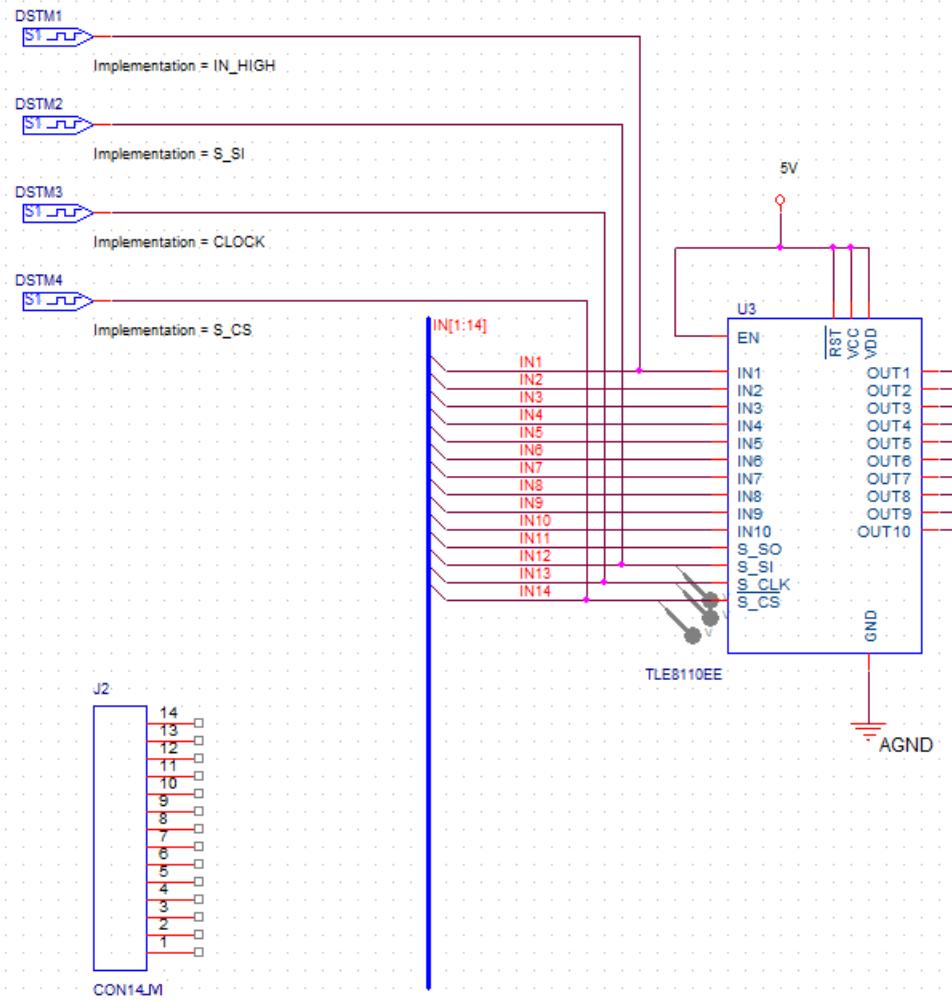
To add the connectors in the smart multi-channel switch circuit, do the following:

1. In the *Place Part* pane, search and select CON14_M from the *Part* list box.
2. Click the *Place Part* icon (or press Enter.
The part symbol is attached to the cursor.
3. Click the schematic page before the IC TLE8110EE and place the connector J2 as shown in figure, [Placing connector, J2](#).
4. Right-click J2 and select *Rotate*.
5. Extend the bus before the input pins of TLE8110EE as shown in figure, [Placing connector, J2](#).

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

Placing connector, J2



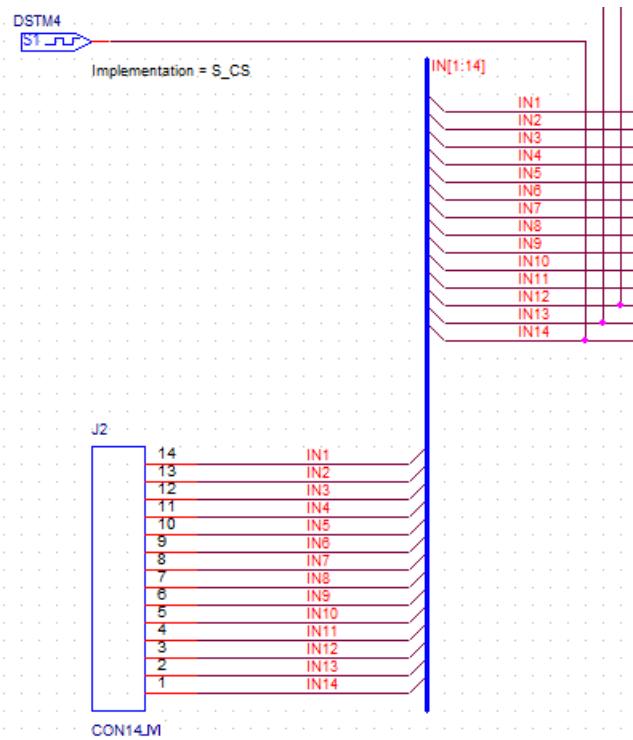
6. Select all the pins of connector J2, right-click the selection, and choose *Connect to Bus*.
7. Click the bus that you had extended in step 5.
The *Enter Net Names* dialog box appears.
8. Click *OK*.

Net names appear on each net from the connector pins to the bus.

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

Connecting J2 to bus at the input of TLE8110EE



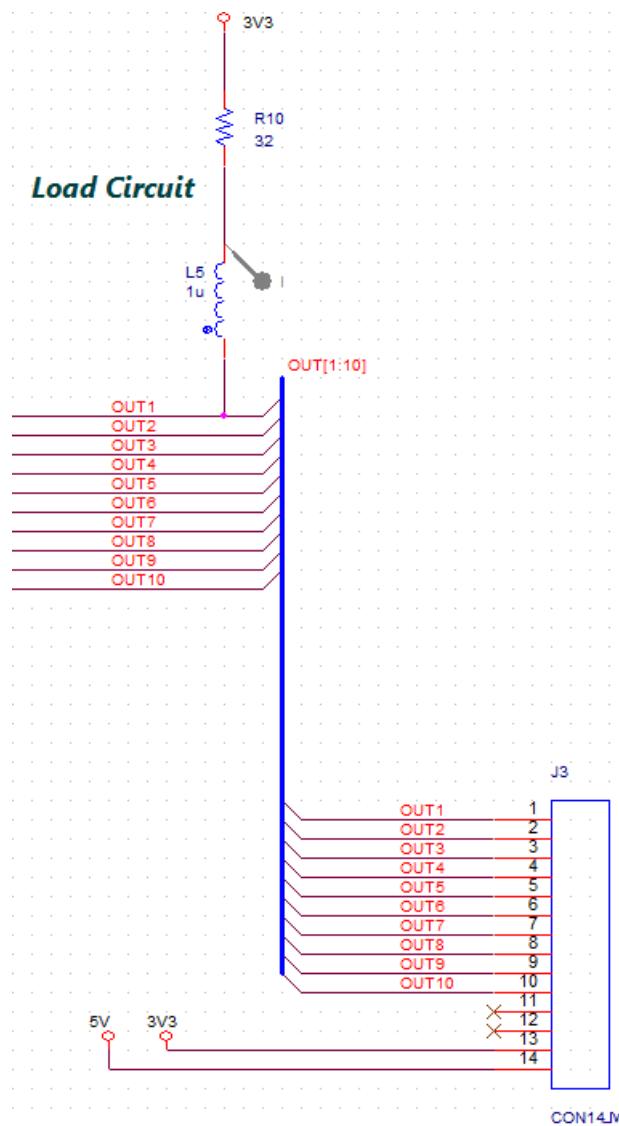
9. Similarly, place another connector, J3 and do the following:

- a. Connect its first 10 pins as shown in figure, [Connecting J3 to bus at the output of TLE8110EE](#).
- b. Click the No Connect icon () or press X, and connect it to pins 11 and 12 of connector J3.
- c. Connect 3V3 and 5V power ports to pins 13 and 14 of connector J3.

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

Connecting J3 to bus at the output of TLE8110EE



Updating Footprints

As the first step to preparing your design for layout creation, update the footprint associated with all the resistors in the design.

Updating Footprints Associated with Resistors

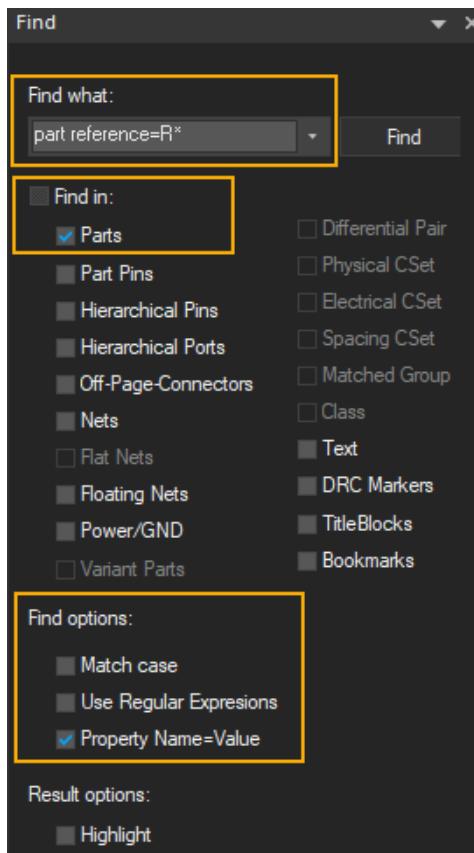
To assign footprints to all the resistors, do the following:

1. Choose *Edit – Find* or press CTRL+F.
The *Find* pane appears.
2. Specify part reference=R* in the *Find what* field.
3. Select the *Parts* check box under *Find in*.
4. Select the *Property Name=Value* check box under *Find options*.

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

Specifying search criteria in Find pane



5. Click the *Find* button.

The Find Results window appears with a list of all the resistors in the design.

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

Viewing search results in Find Results window

Find Results										
Parts										
Part Reference	Value	Source Part	Source Library	Page	Page Number	Schematic	Zone	Location X-Coordinate	Location Y-Coordinate	
R1	4.7k	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	5D	170	150	
R2	60k	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	5D	210	220	
R3	20k	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	5C	250	270	
R4	40k	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	4D	380	150	
R5	50m	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	4D	480	210	
R6	200	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	3D	710	210	
R7	5	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	3D	880	110	
R8	10K	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	2D	1080	90	
R9	15	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	1D	1380	210	
R10	32	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	2C	990	450	

- To select all the rows in the Find Results window, click the first row, press SHIFT and then click the last row.
- To modify the properties of the selected results, right-click the selection and choose *Edit Properties* or press CTRL+SHIFT+E.

Editing properties of search results

Find Results										
Parts										
Part Reference	Value	Source Part	Source Library	Page	Page Number	Schematic	Zone	Location X-Coordinate	Location Y-Coordinate	
R1	4.7k	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	5D	170	150	
R2	60k	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	Edit Properties (Ctrl+Shift+E)				
R3	20k	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1					
R4	40k	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1					
R5	50m	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1					
R6	200	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1					
R7	5	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1					
R8	10K	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1					
R9	15	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	1D	1380	210	
R10	32	R	C:\CADENCE\ORCADX_23.1\TOOLS\CAPTURE\LIBRARY\PSPICE\ANALOG.OLB	PAGE1	1	SCHEMATIC1	2C	990	450	

The Browse Spreadsheet window opens.

- Change the value from AXRC05 to SMR2512 for *PCB Footprint* corresponding to each resistor.

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

Changing PCB Footprint values in Browse Spreadsheet window

	TC1	MAX_TEMP	DIST	VOLTAGE	POWER	PSpice Model Type	PCB Footprint	TOLERANCE	PSpiceTemplate
1	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@REFDES
2	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@REFDES
3	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@REFDES
4	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@REFDES
5	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@REFDES
6	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@REFDES
7	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@REFDES
8	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@REFDES
9	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@REFDES
10	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@REFDES

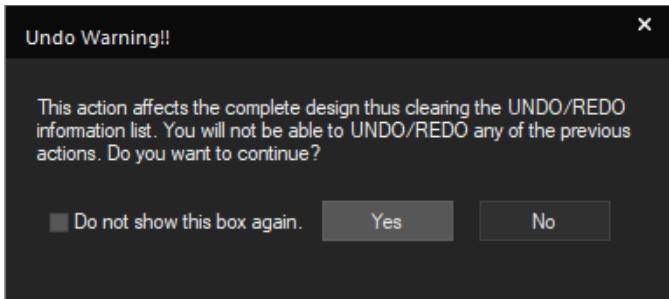
	TC1	MAX_TEMP	DIST	VOLTAGE	POWER	PSpice Model Type	PCB Footprint	TOLERANCE	PSpiceTemplate
1	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@REFDES
2	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@REFDES
3	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@REFDES
4	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@REFDES
5	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@REFDES
6	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@REFDES
7	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@REFDES
8	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@REFDES
9	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@REFDES
10	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@REFDES

9. Click OK.

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

An undo warning appears to confirm the changes.



10. Select the *Do not show this box again* check box and then click Yes.

Updating Footprints Associated with Capacitors

Similarly, update footprints associated with all the capacitors with the following changes and save the design:

- Specify part reference=C* in the *Find what* field.
- Change the value from cap196 to SMC0603 for *PCB Footprint* corresponding to each capacitor.

Updating Footprints Associated with Inductors

Update footprints associated with all the inductors in the design with the following changes and save the design:

- Specify part reference=L* in the *Find what* field.
- Change the value from DISC350x1 to SML0805 for *PCB Footprint* corresponding to each inductor.

Configuring the PSpiceOnly Property

Some components are added only to represent the fan loads and are not required for the physical layout. To ignore them in the board design, you need to specify the *PSpiceOnly* property.

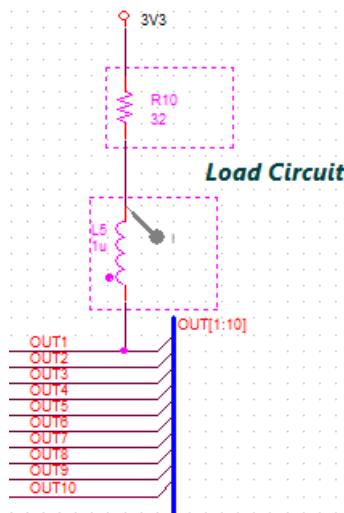
To assign the *PSpiceOnly* property to the inductor and the resistor of the load circuit, do the following:

1. Select the inductor and resistor in the load circuit.

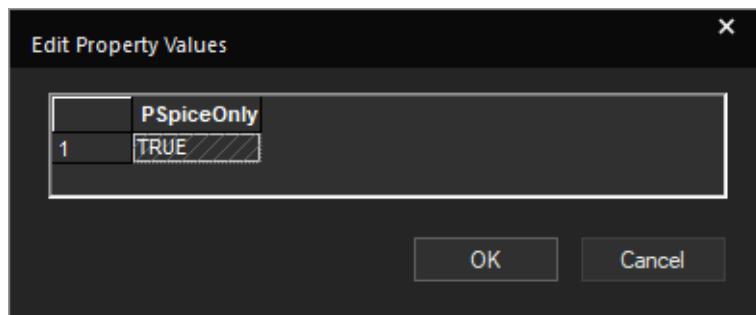
OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

Selecting components of load circuit



2. Right-click and choose *Edit Properties*.
3. Click the *Parts* tab in the *Property Editor* window.
4. From the *Filter by* drop-down list, select *Capture PSpice*.
5. Right-click the cell for the *PSpiceOnly* property and choose *Edit*.
6. Specify *TRUE* as the value in the *PSpice Only* cell and click *OK*.



Parts tab in Property Editor Window

	MNTYMXDLY	Name	Part Reference	Source Library	Source Package	PSpiceTemplate	PSpiceOnly	Reference
1	SCHEMATIC1 : PAGE1	INS18041	L5	C:\ICADENCE\SPB_23.1	L	L^@REFDES %1 %2 ?TOL%	TRUE	L5
2	SCHEMATIC1 : PAGE1	INS12892	R10	C:\ICADENCE\SPB_23.1	R	R^@REFDES %1 %2 ?TOL%	TRUE	R10

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

7. Save the design.

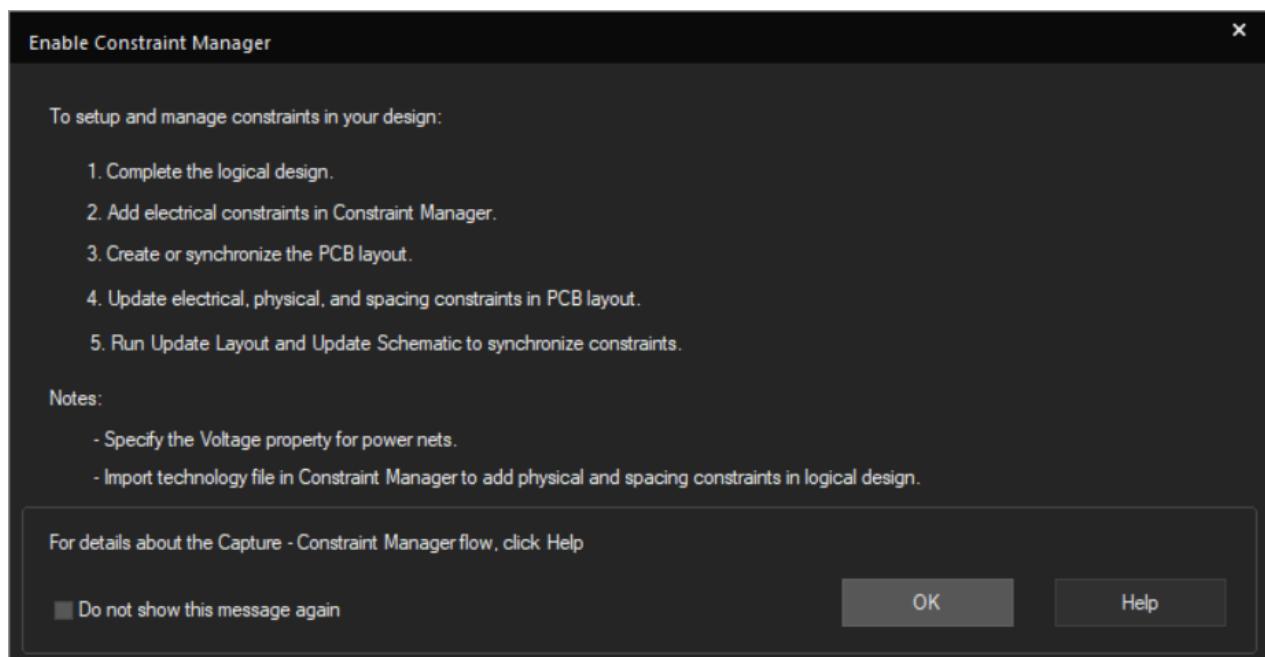
Adding Constraints

You will now specify the minimum value of the total etch length of each net in Constraint Manager launched from Capture.

To add this electrical constraint in the schematic design, do the following:

1. Choose *PCB – Constraint Manager* or click the *Constraint Manager* icon () on the PCB toolbar.

An information window appears to explain the Capture-Constraint Manager flow.



2. Click OK.

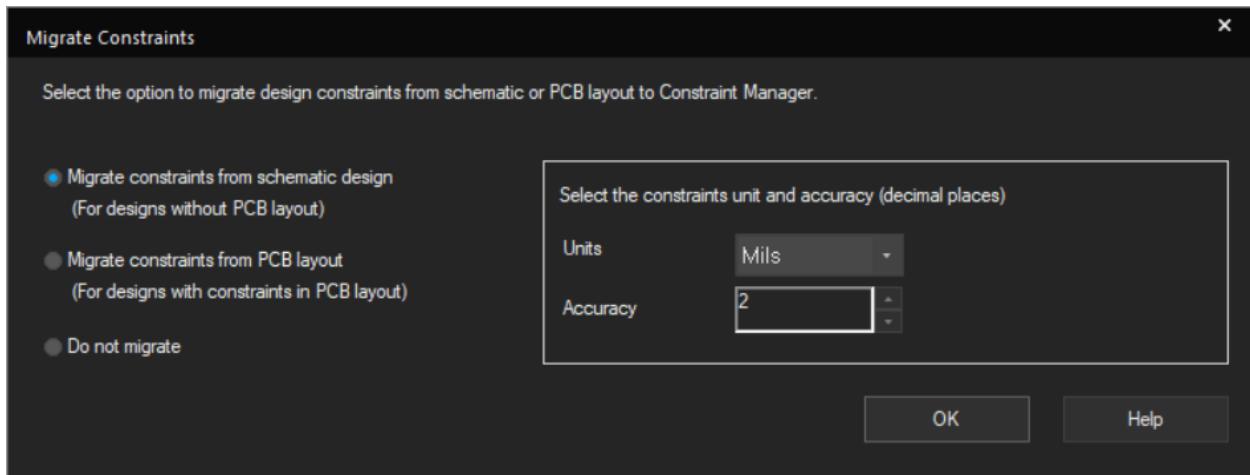
The *Migrate Constraints* dialog box appears.

3. Select *Migrate constraints from schematic design*.
4. Specify the unit to be used for physical and spacing constraints in the Constraint Manager window.

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

PCB Editor uses Mils as the default unit. For this tutorial, select Mils from the *Units* drop-down list.



5. Click OK.

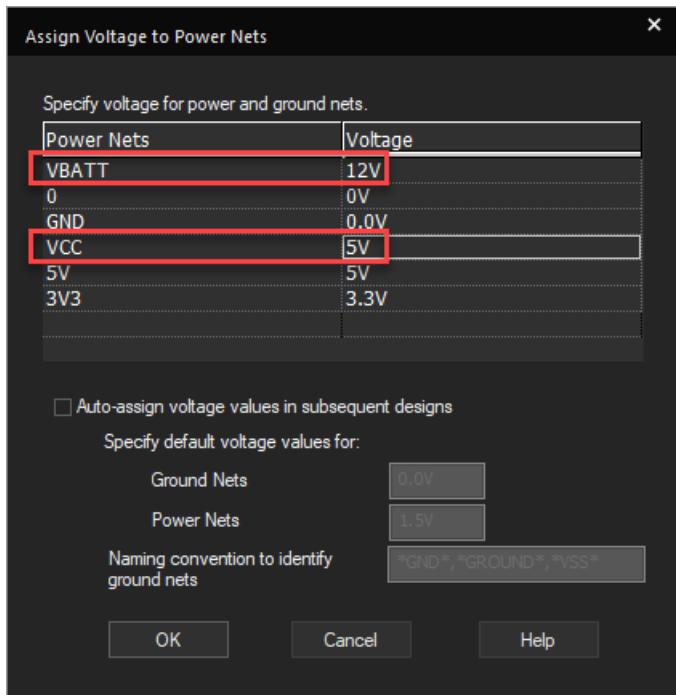
The Assign Voltage to Power Nets window opens. This has predefined voltage values for all the power nets.

6. Modify these voltage values as follows:

- VBATT = 12V
- VCC=5V

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation



You can also open this dialog box from *SI Analysis – Identify DC Nets*.

7. Click OK.

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

The Constraint Manager window opens.

The screenshot shows the OrCAD Constraint Manager window with the following details:

- Worksheet Selector:** Shows the 'Electrical' tab selected.
- Tree View:** Under 'Electrical Constraint Set', 'Net' is expanded, showing 'Routing' and 'Total Etch Length' selected.
- Design Instance/Block filter:** Shows 'TUTORIAL' checked.
- Table:** The main table lists various nets with their properties. The 'Total Etch Length' column has two rows: 'Min' and 'mil'.

Objects			Referenced Electrical CSet	Total Etch Length
Type	S	Name		Min
*	*	*		mil
Dsn		TUTORIAL		
Net		IN1		
Net		IN2		
Net		IN3		
Net		IN4		
Net		IN5		
Net		IN6		
Net		IN7		
Net		IN8		
Net		IN9		
Net		IN10		
Net		IN11		
Net		IN12		
Net		IN13		
Net		IN14		
Net		N00419		
XNet		N00510		
Net		N00682		
Net		N00873		
Net		N01131		
XNet		N01720		
Net		N02063		

- Specify the minimum total etch length for the IN1 net as 100 mils as shown in the following figure:

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

Specifying minimum total etch length value in schematic design

Objects			Referenced Electrical C Set	Total Etch Length			
Type	S	Name		Min	Actual	Margin	
				mil	mil	mil	
*	*	*	*	*	*	*	
Dsn		▲ TUTORIAL					
Net		IN1		100.00			
Net		IN2					
Net		IN3					
Net		IN4					
Net		IN5					
Net		IN6					
Net		IN7					
Net		IN8					
Net		IN9					
Net		IN10					
Net		IN11					
Net		IN12					
Net		IN13					
Net		IN14					
Net		N00419					
XNet		N00510					
Net		N00682					

9. To specify the same value for *Total Etch Length* in all the nets, select the next row up till the last net in this window.
10. Release the mouse and specify 100 in the last row.

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

All the nets and Xnets in the design are assigned the same value.

Objects			Referenced Electrical CSet	Total Etch Length			
Type	S	Name		Min	Actual	Margin	
				mil	mil	mil	
*	*	*	*	*	*	*	
Dsn		TUTORIAL					
Net		IN1		100.00			
Net		IN2		100.00			
Net		IN3		100.00			
Net		IN4		100.00			
Net		IN5		100.00			
Net		IN6		100.00			
Net		IN7		100.00			
Net		IN8		100.00			
Net		IN9		100.00			
Net		IN10		100.00			
Net		IN11		100.00			
Net		IN12		100.00			
Net		IN13		100.00			
Net		IN14		100.00			
Net		N00419		100.00			
XNet		N00510		100.00			
Net		N00682		100.00			
Net		N00873		100.00			
Net		N01131		100.00			
XNet		N01720		100.00			
Net		N02063		100.00			
Net		N02685		100.00			
Net		N03504		100.00			
Net		N03592		100.00			
XNet		N04181		100.00			
XNet		OUT1		100.00			
Net		OUT2		100.00			
Net		OUT3		100.00			
Net		OUT4		100.00			
Net		OUT5		100.00			
Net		OUT6		100.00			
Net		OUT7		100.00			
Net		OUT8		100.00			
Net		OUT9		100.00			
Net		OUT10		100.00			

11. Save the design.

Summary

This section covered the steps for preparing the schematic design for designing the physical layout of the PCB board. In the process, you were introduced to tasks, such as placing

OrCAD X Capture with OrCAD X Presto Tutorial

Preparing for PCB Layout Creation

connectors, adding footprint information, and adding electrical constraints using Constraint Manager.

Creating a Board Design

After the logic design is completed, the next step is to create the layout of the PCB. This section walks you through the basics of the layout creation steps, such as placement, routing, and generating output data to create a layout of the fan-control module design in OrCAD X Presto.

In this section, you will learn how to create a layout design, `tutorial.brd` for the logic design you created and simulated in the previous sections. The sample logic design file is available at the following location:

`<install_directory>\share\orcad\tutorial\tutorial.opj`

Creating a Blank Board

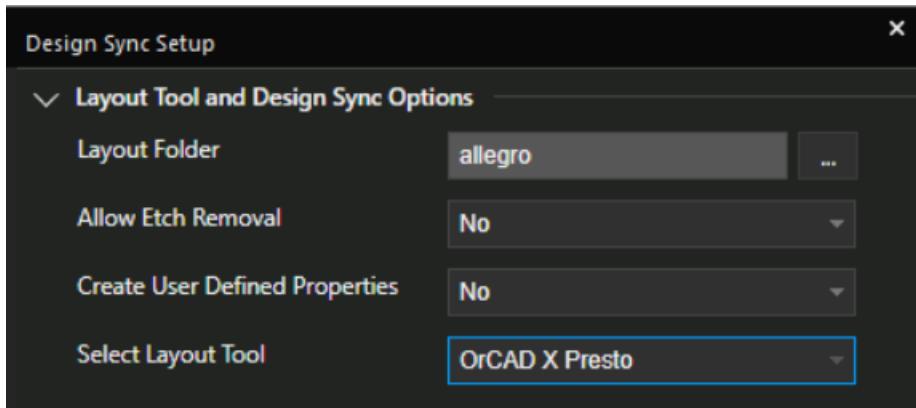
The first task is to create a new blank board design. Perform the following steps to create a blank board design:

1. Open `tutorial.opj` in Capture CIS.
2. Choose *PCB – Design Sync Setup* to select the layout tool.

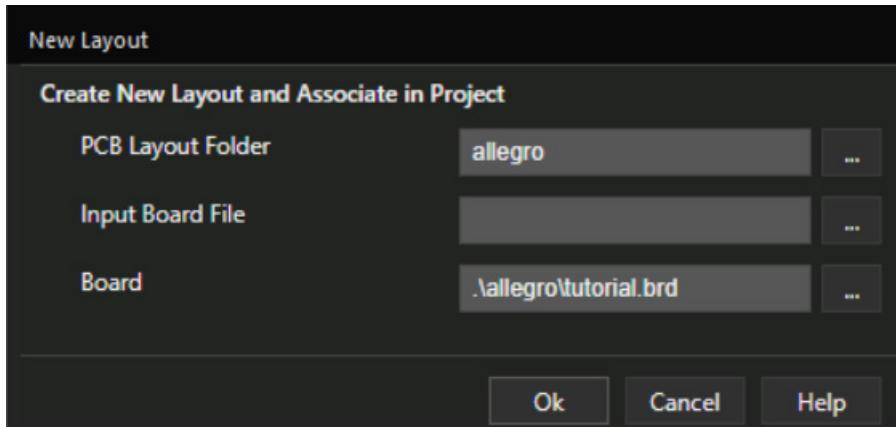
OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Board Design

3. In the *Design Sync Setup* dialog box, choose *OrCAD X Presto* in the *Select Layout Tool*.



4. Click *OK* to close the dialog box.
5. Choose *PCB – New Layout*.



The new board design will be created in the default PCB Layout folder `allegro` inside the working project directory.

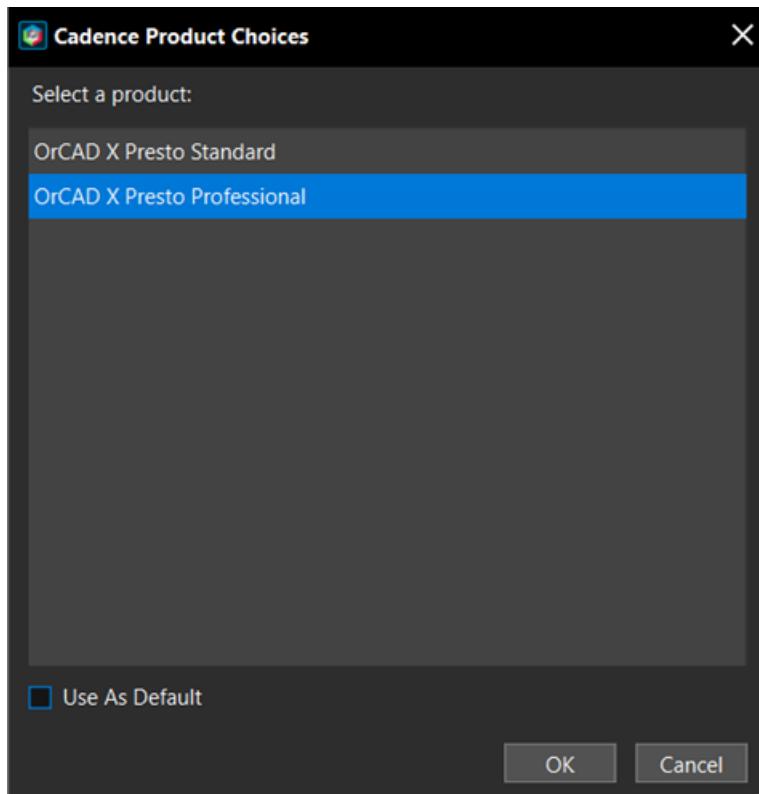
6. To create a blank board design, leave the *Input Board File* name field blank.
7. Specify the output board file name as `tutorial` and click *Ok*.

The *Cadence Product Choices* dialog box is displayed.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Board Design

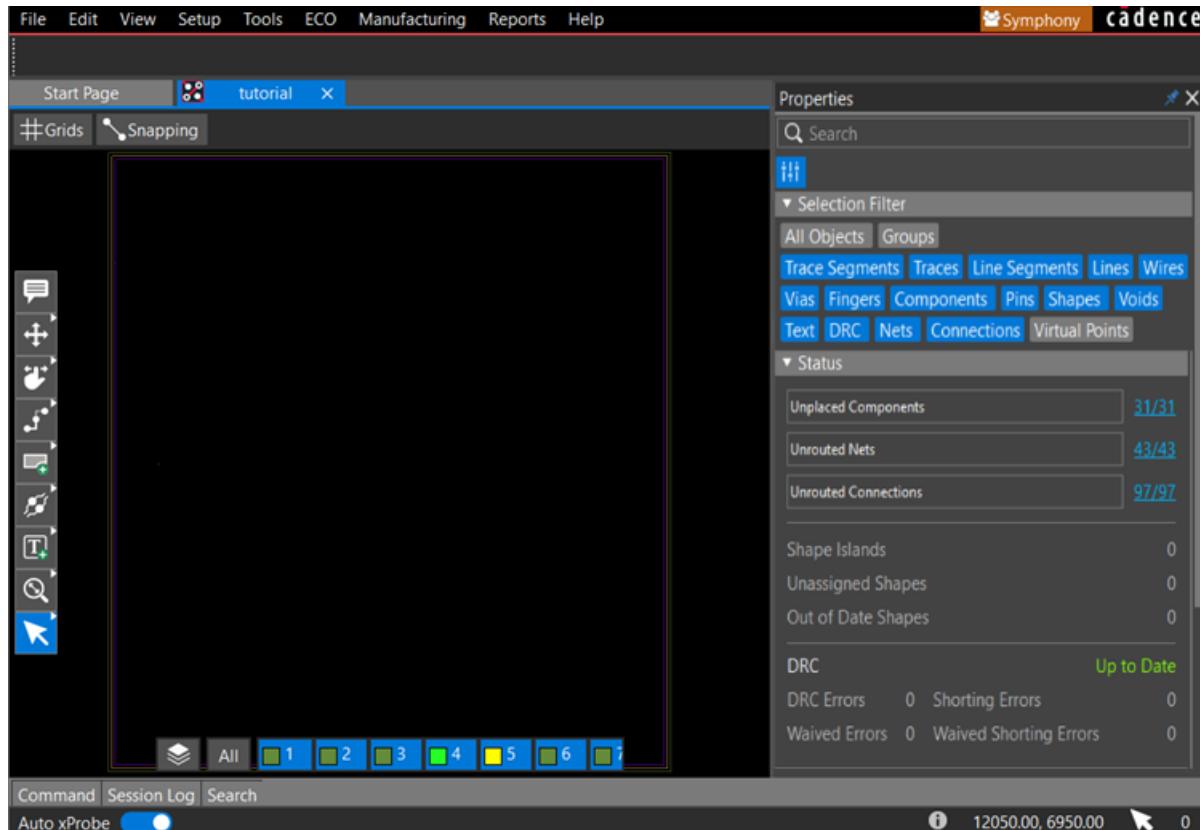
8. Select the *OrCAD X Presto Professional* option and click *OK*.



OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Board Design

A blank design `tutorial.brd` is opened in OrCAD X Presto layout editor. The logic design data is transferred to the layout and is saved in the `allegro` directory.



The *Status* section of the *Properties* panel shows the number of unplaced components, unrouted nets, and unrouted connections.

1. Click the Out of Date icon for the DRCs.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Board Design

The status changes to *Up to Date*.

Status	
Unplaced Components	31/31
Unrouted Nets	42/42
Unrouted Connections	98/98
Shape Islands	0
Unassigned Shapes	0
Out of Date Shapes	0
DRC	Up to Date
DRC Errors	0
Shorting Errors	0
Waived Errors	0
Waived Shorting Errors	0

Summary

This section covered the generation of PCB board from the schematic with netlist data. In this section, you learned how to set up the layout tool for creating and syncing a board.

OrCAD X Capture with OrCAD X Presto Tutorial

Creating a Board Design

Setting Up Layout Editor Design Environment

To create the board design efficiently, you first need to set up the design environment of OrCAD X Presto.

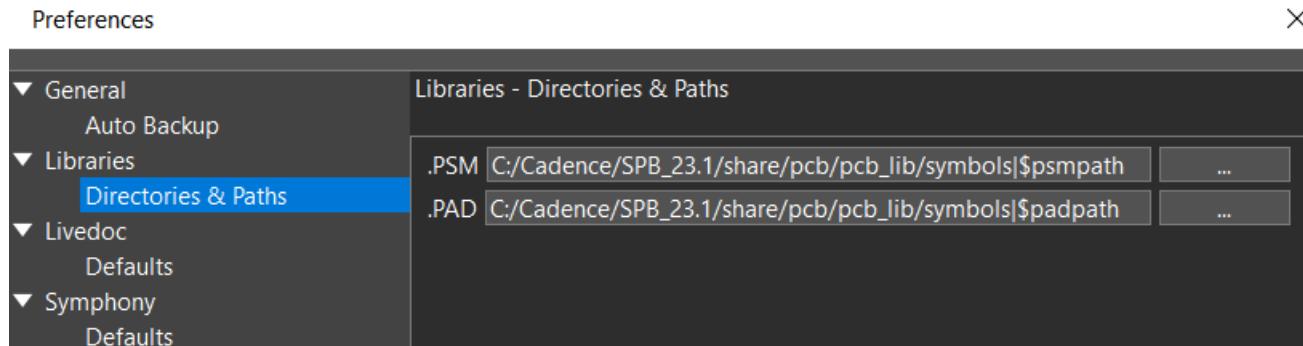
Adding Footprints and Padstacks Libraries

The tutorial design uses default OrCAD X libraries. You need to set the path to the footprints and padstacks libraries in OrCAD X Presto. To add the libraries, so the following:

1. Choose *Edit – Preferences*.

The *Preferences* dialog box opens.

2. Select the *Directories & Paths* folder under *Libraries*.
3. Make sure the following padstack library paths are set for both *.PSM* and *.PAD*:



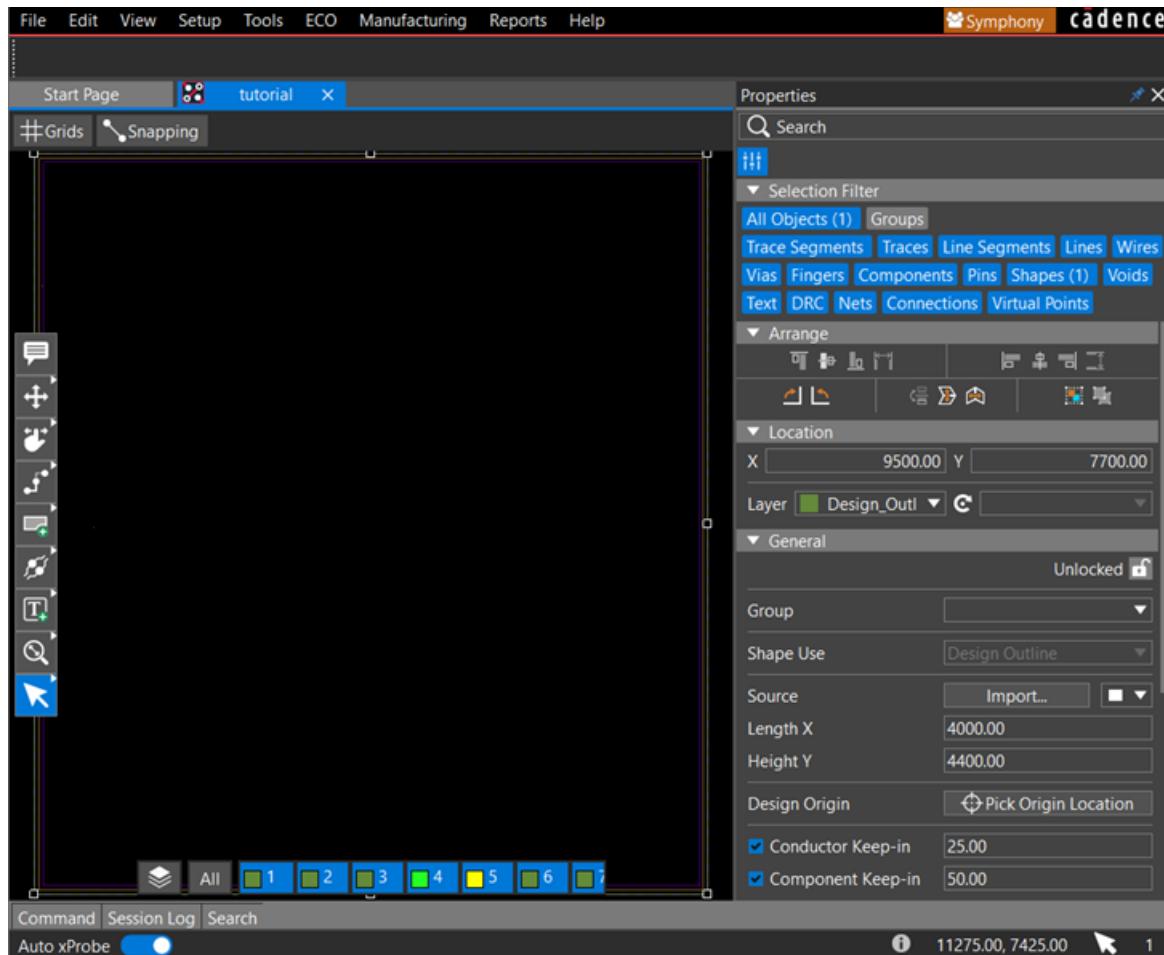
4. Click *OK* to close the *Preferences* dialog box.
5. Choose *File – Save tutorial.brd* to save the design.
6. Click *Yes* if prompted to overwrite the design.

Modifying Default Design Outline

OrCAD X Presto creates a rectangular design outline, by default, when you create a new design. You can adjust the size of the design outline according to the size of your PCB by following these steps:

1. In the *Properties* panel, ensure that *Shapes* is selected.
2. Double-click the design outline shape.

The design outline shape is selected and the anchor points are visible.



3. In the *General* pane of the *Properties* panel, modify the *Length X* and *Height Y* of the design outline. Change the values to 4000 and 4400, respectively.

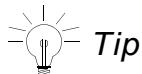
Alternatively, double-click an anchor point and drag the mouse to extend or shorten the selected edge of the design outline shape.

The length and height of the shape is updated in the *General* pane.

OrCAD X Capture with OrCAD X Presto Tutorial

Setting Up Layout Editor Design Environment

4. Click anywhere in the blank space or press Esc.



Tip

To modify the shape of the design outline from rectangle to polygon, double-click a point on any edge. A new anchor point is added to the shape. Dragging the new anchor point creates a new vertex of the polygon-shapes design outline.

5. To view the entire board in the design canvas, click the zoom fit icon  from the functional toolbar.

Alternatively, choose *View – Zoom – Zoom Fit* to center the board outline in the design window.

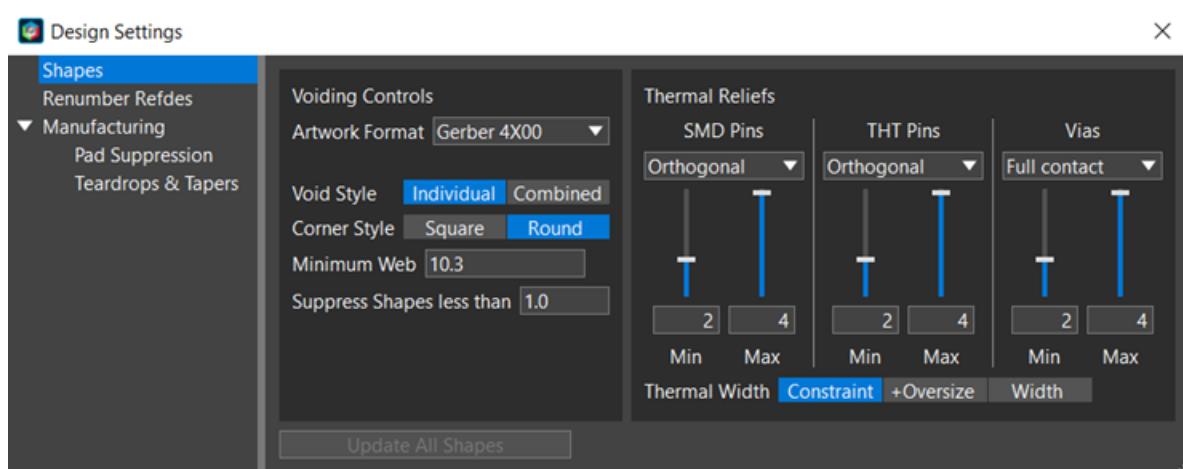
6. Choose *File – Save tutorial.brd* to save the design and click Yes to overwrite the file.

Setting Up Design Parameters

Drawing parameters for shapes and manufacturing process can be configured at the design level using the *Design Settings* dialog box. To modify the default design settings, perform the following steps:

1. Choose *Setup – Design Parameters Editor*.

The *Design Settings* dialog box opens and displays the *Shapes* settings.

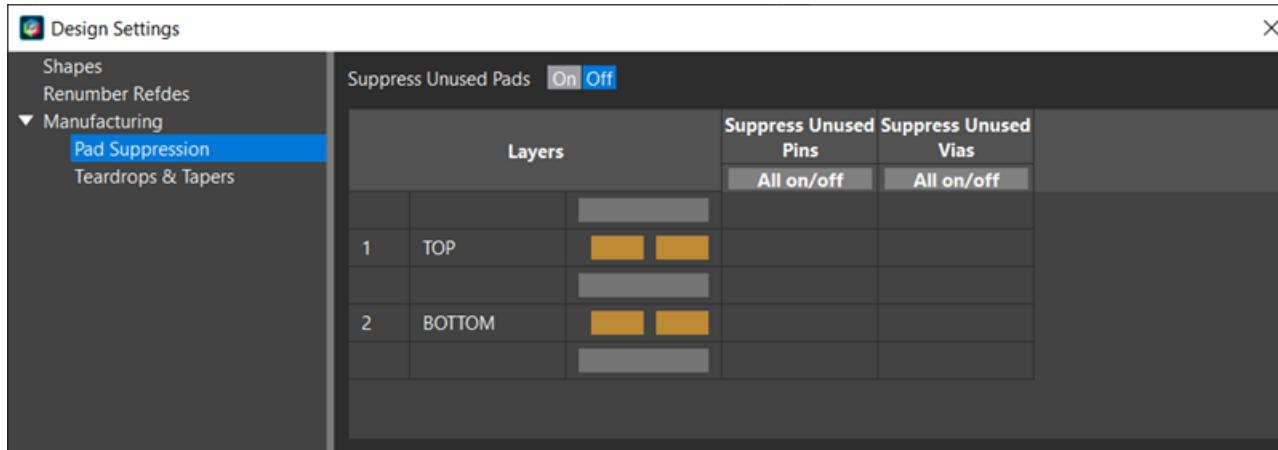


2. In the *Voiding Controls* pane, ensure that *Artwork Format* is set to *Gerber RS274X*.
3. In the *Thermal Reliefs* pane, ensure that *Thermal Width* is set to *Constraint*.
4. Select *Pad Suppression* under *Manufacturing* in the tree view. Ensure that the *Suppress Unused Pads* option is set to *Off*.

OrCAD X Capture with OrCAD X Presto Tutorial

Setting Up Layout Editor Design Environment

Disabling this option ensures optimal routing and shape voiding.



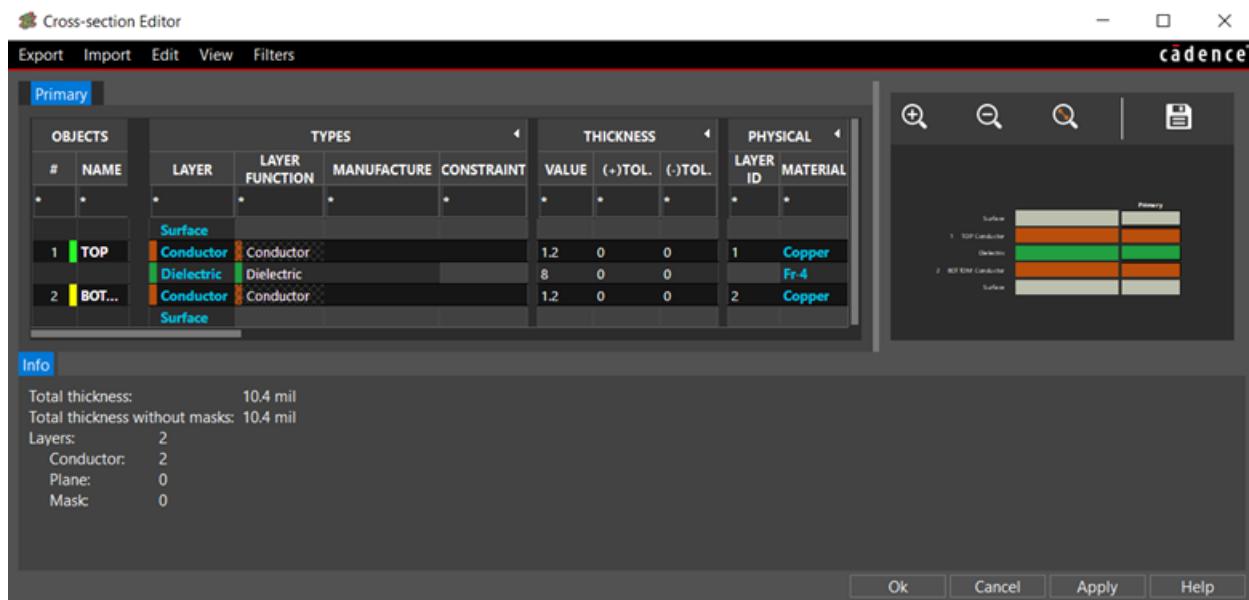
5. Close the *Design Settings* dialog box.

Viewing Cross Section and Material Information

The tutorial design uses a single-layer PCB, which has copper on the BOTTOM layer and components on the TOP layer and uses default values for all parameters.

1. Choose *Tools – Cross Section* to view the layer setup.

The Cross-section Editor window is displayed.



OrCAD X Capture with OrCAD X Presto Tutorial

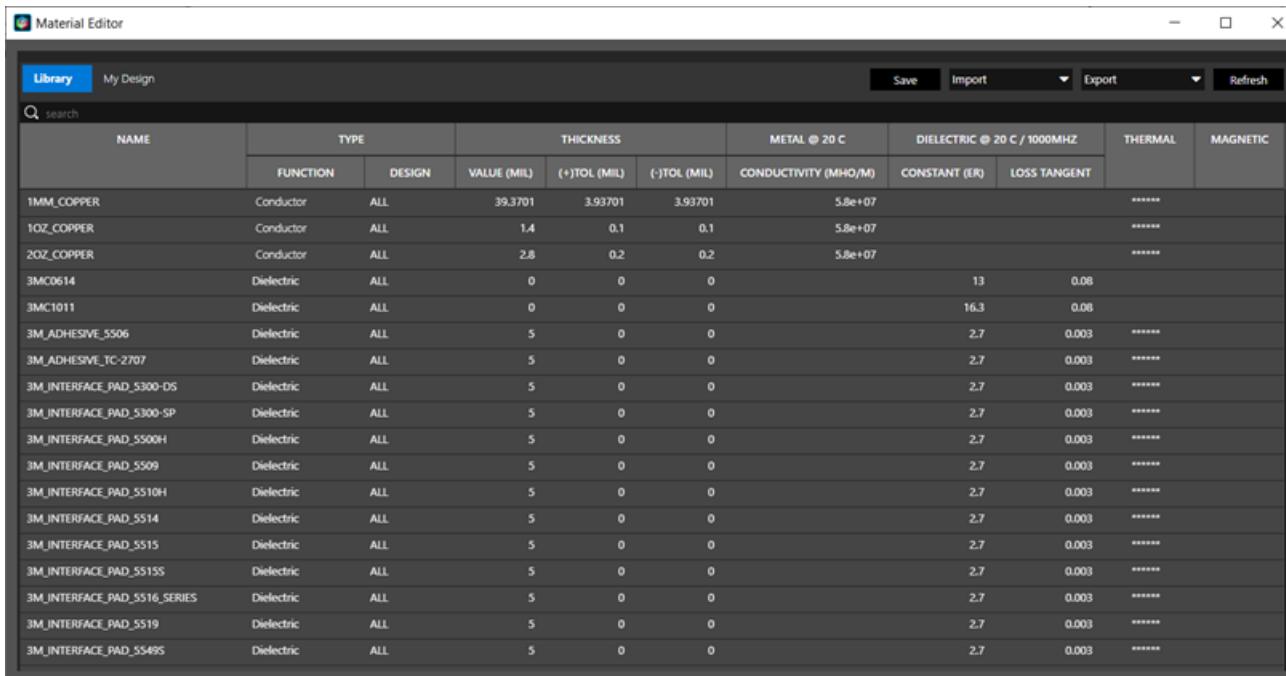
Setting Up Layout Editor Design Environment

The conductor layers TOP and BOTTOM are for placing components. In the Cross-section Editor window, you can specify layer properties, such as material type, thickness, and so on.

2. Close the Cross-section Editor window.

3. Choose *Tools – Material Editor*.

The Material Editor window opens and displays the list of materials available from the default library that is shipped with the installation.



The screenshot shows the Material Editor window with the 'Library' tab selected. The main area displays a table of materials with the following columns: NAME, TYPE, FUNCTION, DESIGN, VALUE (MIL), (+)TOL (MIL), (-)TOL (MIL), METAL @ 20 C, CONDUCTIVITY (MHO/M), DIELECTRIC @ 20 C / 1000MHZ, CONSTANT (ER), LOSS TANGENT, THERMAL, and MAGNETIC. The table lists various materials like 1MM_COPPER, 1OZ_COPPER, 2OZ_COPPER, etc., with their respective properties. The 'My Design' tab is also visible at the top left.

NAME	TYPE		THICKNESS			METAL @ 20 C		DIELECTRIC @ 20 C / 1000MHZ		THERMAL	MAGNETIC
	FUNCTION	DESIGN	VALUE (MIL)	(+)TOL (MIL)	(-)TOL (MIL)	CONDUCTIVITY (MHO/M)	CONSTANT (ER)	LOSS TANGENT			
1MM_COPPER	Conductor	ALL	39.3701	3.93701	3.93701	5.8e+07					
1OZ_COPPER	Conductor	ALL	1.4	0.1	0.1	5.8e+07					
2OZ_COPPER	Conductor	ALL	2.8	0.2	0.2	5.8e+07					
3MC0614	Dielectric	ALL	0	0	0		13	0.08			
3MC1011	Dielectric	ALL	0	0	0		16.3	0.06			
3M_ADHESIVE_5506	Dielectric	ALL	5	0	0		2.7	0.003			
3M_ADHESIVE_TC-2707	Dielectric	ALL	5	0	0		2.7	0.003			
3M_INTERFACE_PAD_5300-DS	Dielectric	ALL	5	0	0		2.7	0.003			
3M_INTERFACE_PAD_5300-SP	Dielectric	ALL	5	0	0		2.7	0.003			
3M_INTERFACE_PAD_5500H	Dielectric	ALL	5	0	0		2.7	0.003			
3M_INTERFACE_PAD_5509	Dielectric	ALL	5	0	0		2.7	0.003			
3M_INTERFACE_PAD_5510H	Dielectric	ALL	5	0	0		2.7	0.003			
3M_INTERFACE_PAD_5514	Dielectric	ALL	5	0	0		2.7	0.003			
3M_INTERFACE_PAD_5515	Dielectric	ALL	5	0	0		2.7	0.003			
3M_INTERFACE_PAD_5515S	Dielectric	ALL	5	0	0		2.7	0.003			
3M_INTERFACE_PAD_5516_SERIES	Dielectric	ALL	5	0	0		2.7	0.003			
3M_INTERFACE_PAD_5519	Dielectric	ALL	5	0	0		2.7	0.003			
3M_INTERFACE_PAD_5549S	Dielectric	ALL	5	0	0		2.7	0.003			

4. Open *My Design* tab to view the materials used in the tutorial design.

5. Close the Material Editor window.

Adding Artwork Views

To create artwork files, OrCAD X Presto reads film control records to determine the number of artwork files to produce, their names, and the list of classes and subclasses to include in each artwork file.

To add artwork view, do the following:

1. Choose *Manufacturing – Export to Manufacturing*.

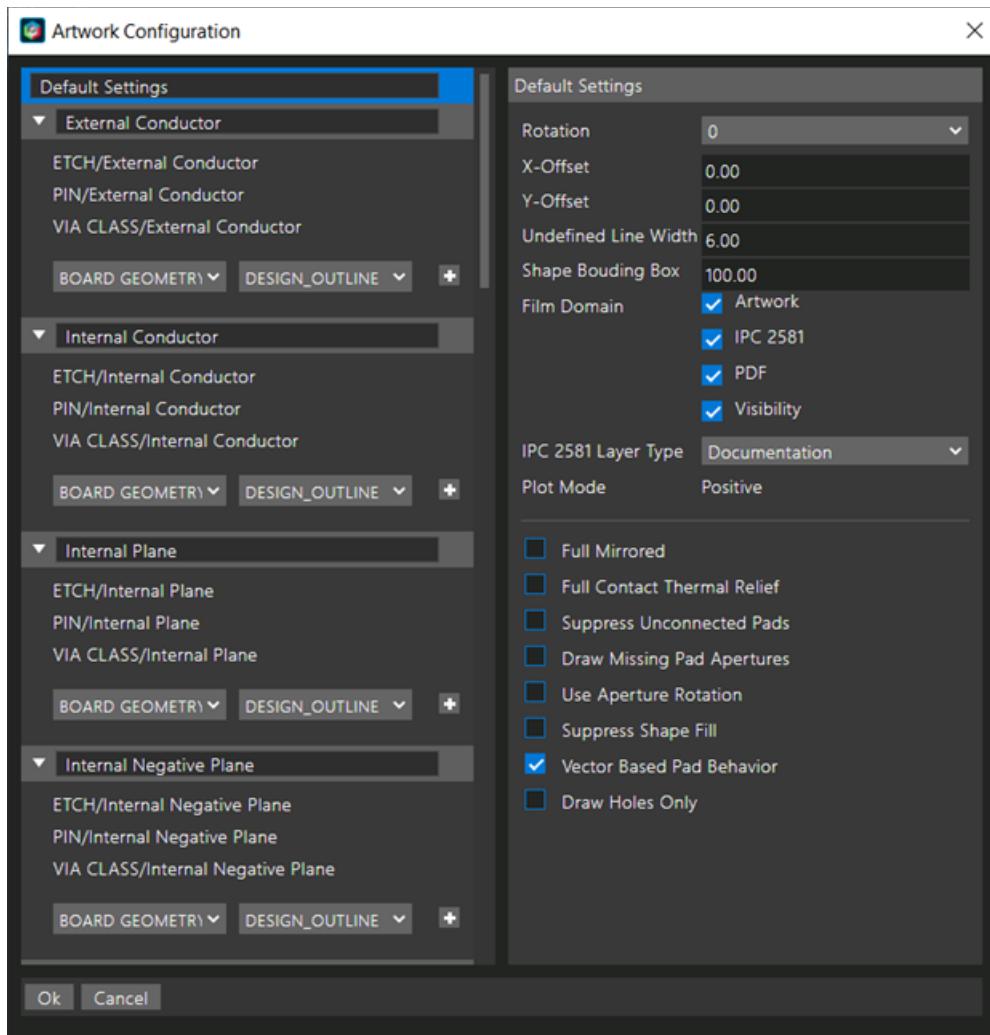
The *Exports* dialog box opens.

OrCAD X Capture with OrCAD X Presto Tutorial

Setting Up Layout Editor Design Environment

- Click the *Configure Artwork Films* option.

The *Artwork Configuration* dialog box opens with default settings.



- In the *Default Settings* pane, deselect the check box for the *Film Domain* type *PDF*.
- Select the *Suppress Unconnected Pads* check box.
- Click *OK* to close the *Artwork Configuration* dialog box.
- Close the *Exports* dialog box.
- Choose *File – Save tutorial.brd* to save the design.

Summary

This section covered the tasks for setting up the OrCAD X Presto environment for creating a board design, quickly and efficiently.

OrCAD X Capture with OrCAD X Presto Tutorial

Setting Up Layout Editor Design Environment

Placing Components Interactively

Component placement is an important task in PCB designing to facilitate easy routing and optimal electrical performance.

Setting Grid for Placement

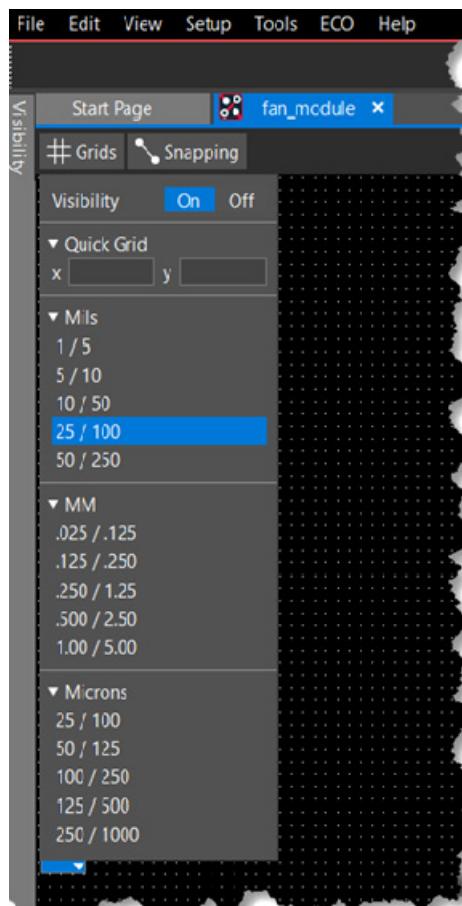
To ease the process of component placement, enable the placement grid by following these steps:

1. Click the *#Grids* tab from the upper-left corner of the design canvas to display the *Grids* pane.
2. Click the *On* button to enable the visibility of the grids.

OrCAD X Capture with OrCAD X Presto Tutorial

Placing Components Interactively

3. Choose the grid value 25/100 in the *Mils* section.



When placing components, the origin of the package symbol snaps to this grid.

4. To hide the *Grids* pane, click anywhere in the blank space.

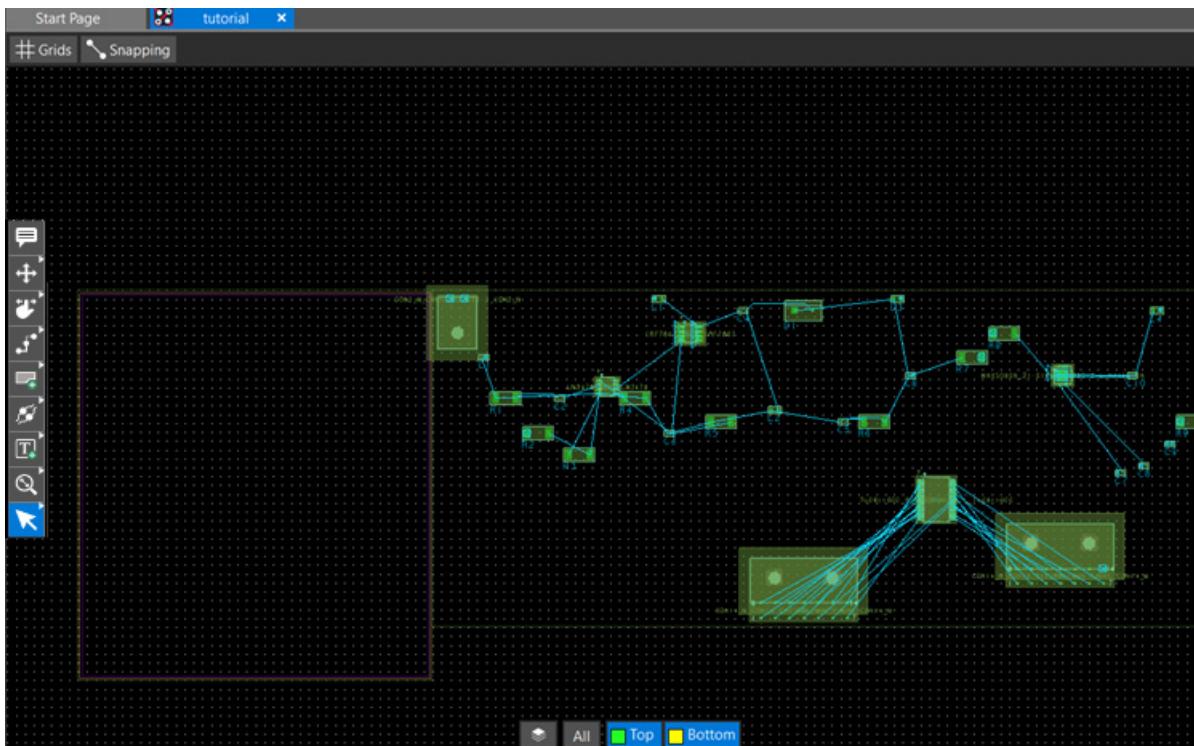
Placing Components

OrCAD X Presto provides interactive commands to place components quickly and efficiently in a design.

OrCAD X Capture with OrCAD X Presto Tutorial

Placing Components Interactively

1. Choose *ECO – Quickplace Components* to place all the components in the design canvas in a single step.



All the components are placed along the longest edge of the design outline shape. Rats are displayed between pins of the same net and help you place components that are connected close to each other.

2. Click the *Move* icon from the functional toolbar and click the $\text{J}3$ symbol to move it inside the design outline.

The symbol gets attached to the cursor.

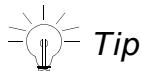
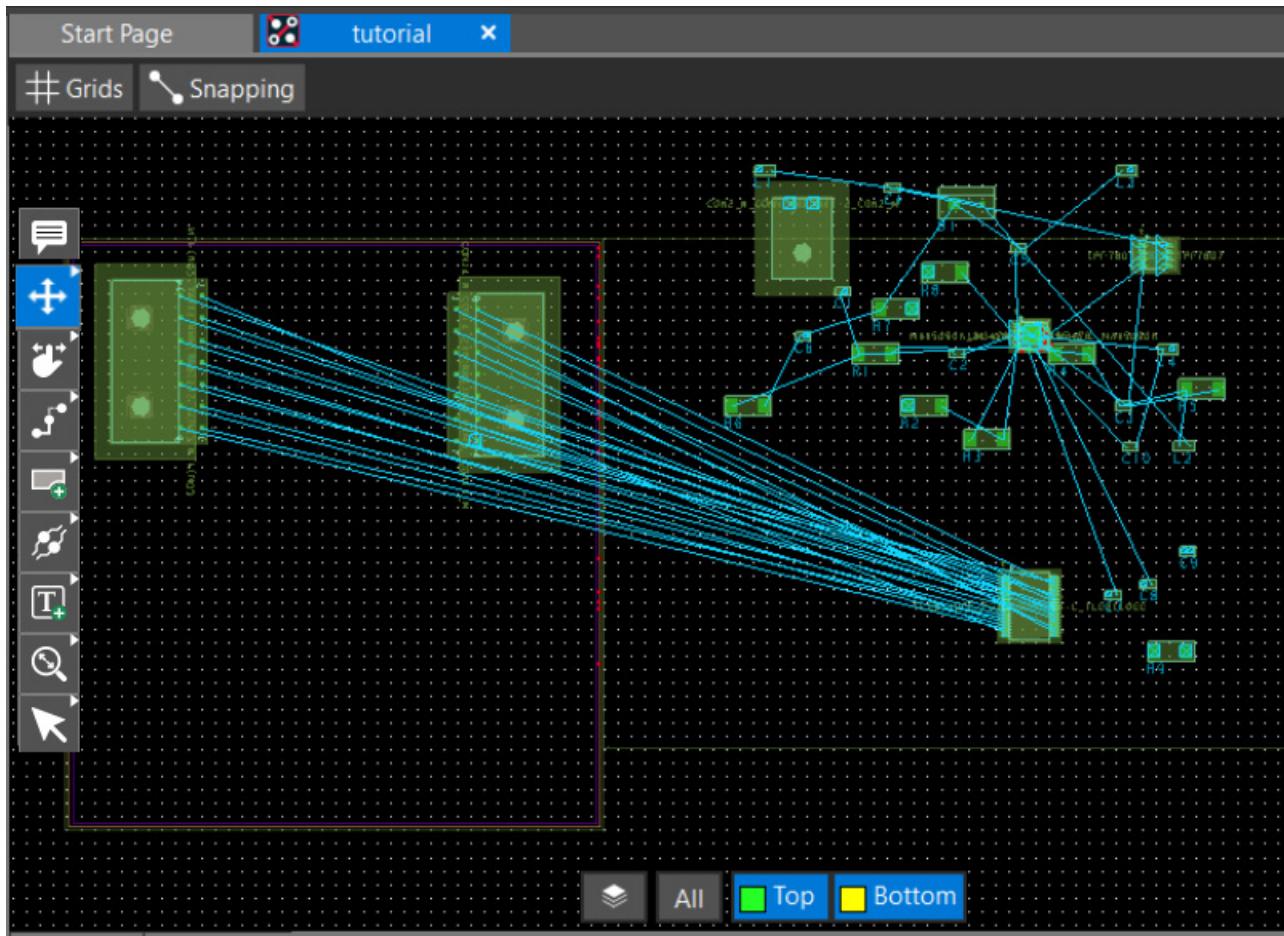
3. Move the cursor near the left boundary of the outline.
4. In the *Arrange* pane of the *Properties* panel, click the *Rotate Left* button to rotate the symbol by 90 degrees anti-clockwise.
5. Click to place the symbol $\text{J}3$ in the design canvas.

Note: The move command remains active until you press the *Esc* button.

OrCAD X Capture with OrCAD X Presto Tutorial

Placing Components Interactively

6. Select the J2 symbol, click the *Rotate Right* button in the *Arrange* pane of the *Properties* panel and place it along the right boundary of the design outline as shown in the following image:

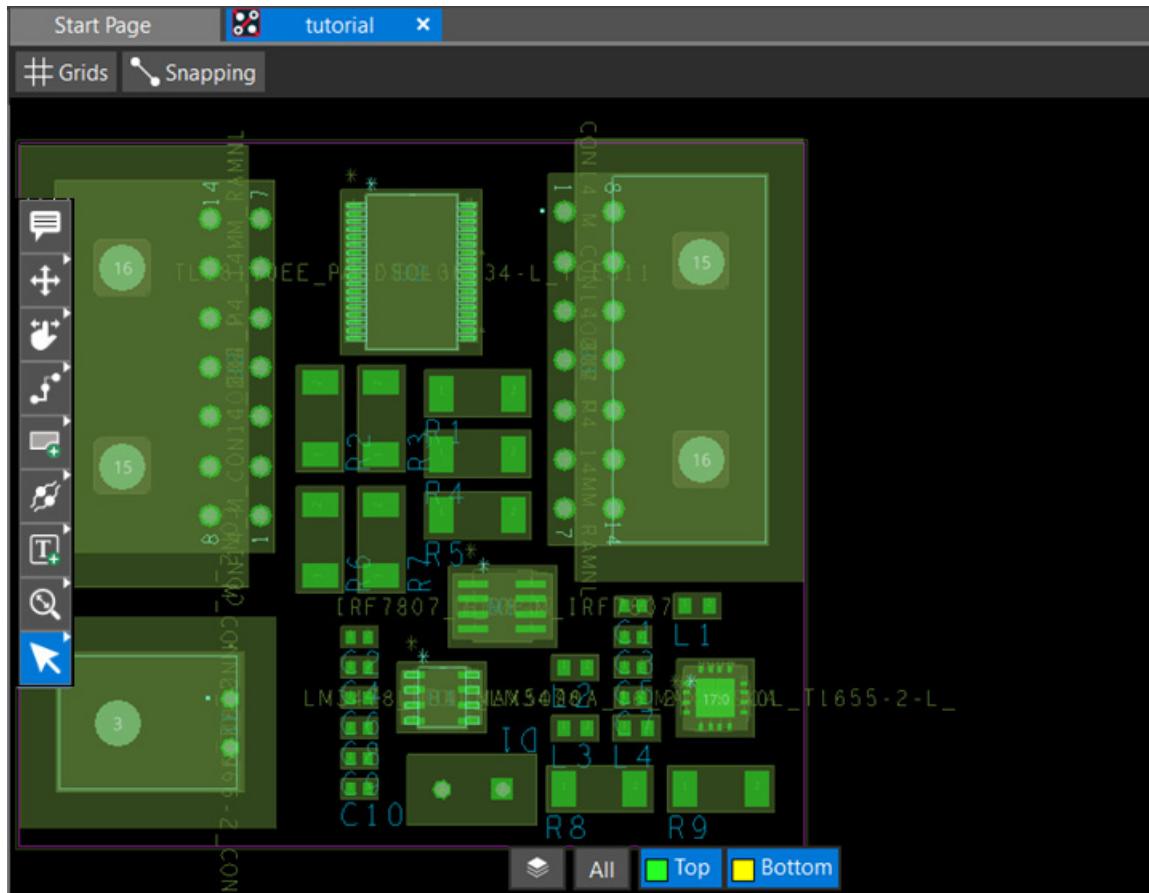


To delete a component from the design canvas, right-click the symbol and choose *Delete* or use the *Delete* key.

OrCAD X Capture with OrCAD X Presto Tutorial

Placing Components Interactively

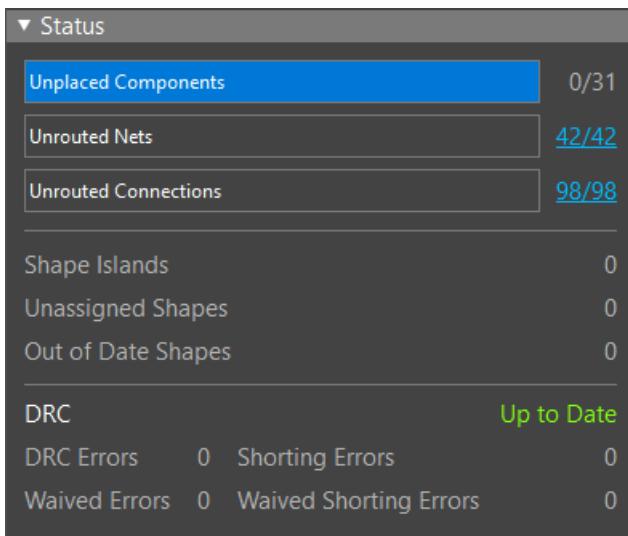
7. Similarly, select each symbol to place all the component symbols inside the design outline. The following image depicts a sample placed board:



OrCAD X Capture with OrCAD X Presto Tutorial

Placing Components Interactively

8. To verify that all the components are placed, check the *Status* pane for *Unplaced Components* in the *Properties* panel.



The *Status* section indicates that there are 0 *Unplaced Components*.

9. Choose *File – Save tutorial.brd* to save the design.

For more information, see [Quick Reference Guide to OrCAD X Presto Interface and Commands](#) in the documentation set.

Summary

This section introduced the methods to place components in OrCAD X Presto.

Routing Nets Interactively

Routing is the process of laying down the tracks to connect components on the board. Before connecting the components, you need to define the physical and spacing constraints.

Setting Up Constraints

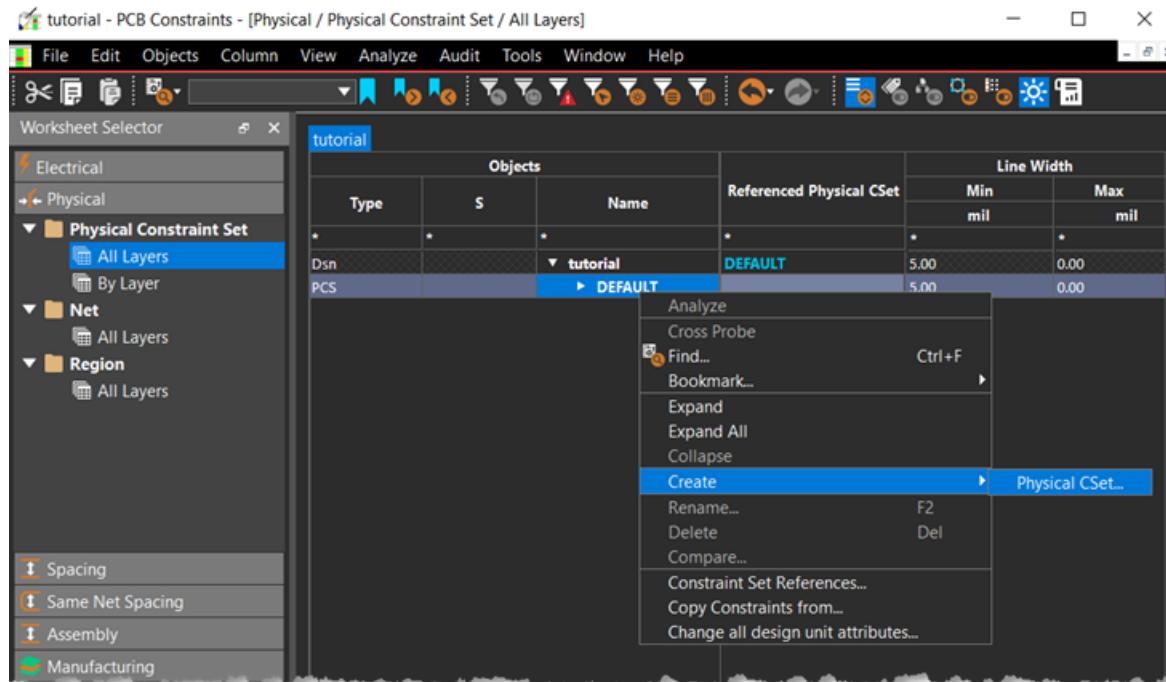
You can define spacing and physical design rules within OrCAD X Presto using Constraint Manager. To route the tutorial design, follow these steps:

1. Choose *Tools – Constraint Manager*.
The Constraint Manager window opens.
2. Click *Physical* and choose the *All Layers* worksheet in the *Physical Constraint Set* folder.

OrCAD X Capture with OrCAD X Presto Tutorial

Routing Nets Interactively

3. In the worksheet, select the default physical constraint set and right-click and choose *Create – Physical CSet*.



The *Create Physical CSet* dialog box is displayed.

4. Specify the name as `POWER_NET_CSET` and click *Ok*.
5. Change the value of *Min Line Width* to `15 mil` from `5 mil` and *Max Neck Length* to `100 mil` from `0 mil` for both the `TOP` and `BOTTOM` layers.

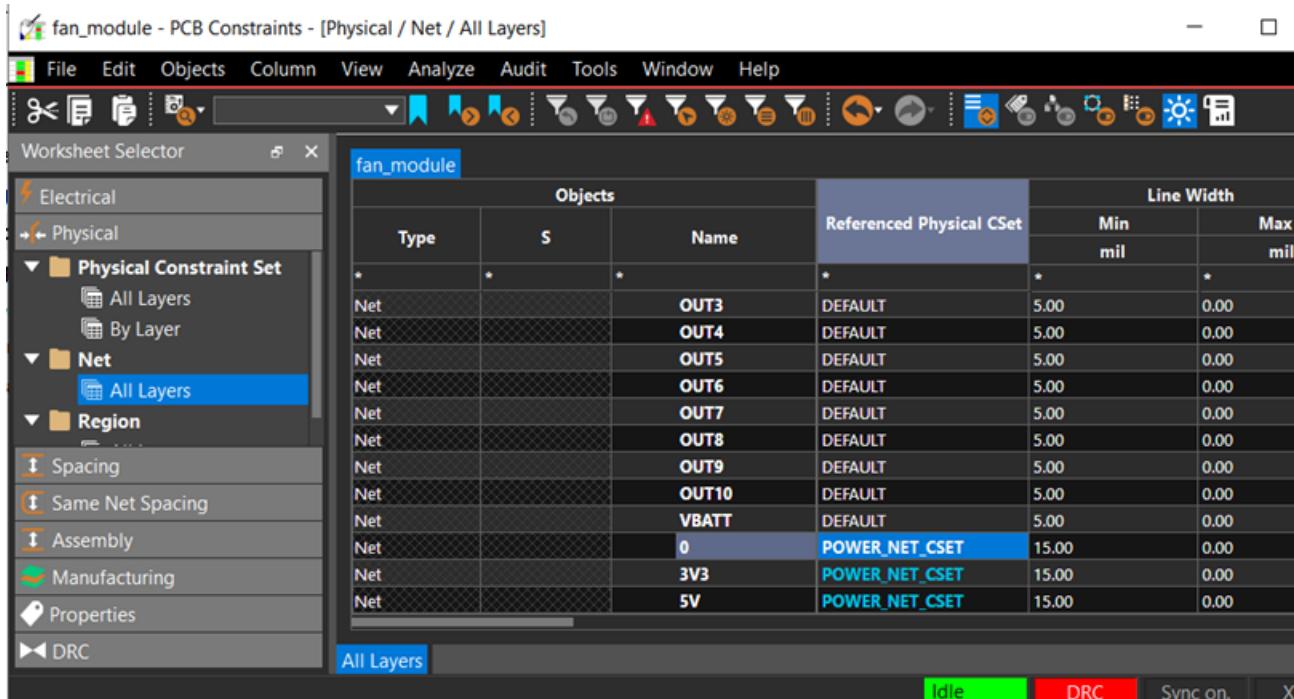
Type	S	Name	Referenced Physical CSet	Line Width		Neck		Min Line Spacing	Prim
				Min mil	Max mil	Min Width mil	Max Length mil		
Dsn		tutorial	DEFAULT	5.00	0.00	5.00	0.00	0.00	0.00
PCS		▶ DEFAULT		5.00	0.00	5.00	0.00	0.00	0.00
PCS		▼ POWER_NET_CSET		15.00	0.00	5.00	100.00	0.00	0.00
LTyp		▶ Conductor		15.00	0.00	5.00	100.00	0.00	0.00
Lyr	1	TOP		15.00	0.00	5.00	100.00	0.00	0.00
Lyr	2	BOTTOM		15.00	0.00	5.00	100.00	0.00	0.00

OrCAD X Capture with OrCAD X Presto Tutorial

Routing Nets Interactively

Changing values for the parent (Conductor) layer also changes the values in the child layers (TOP and BOTTOM) automatically.

6. Choose *Net – All Layers* folder.
7. In the *All Layers* worksheet, select the net 5V.
8. Set the *Referenced Physical CSet* to **POWER_NET_CSET**.
9. Similarly, select the nets 3V3 and 0 and set *Referenced Physical CSet* to **POWER_NET_CSET**.



10. Choose *File – Close* to close Constraint Manager.

Assigning Color to Power and Ground Nets

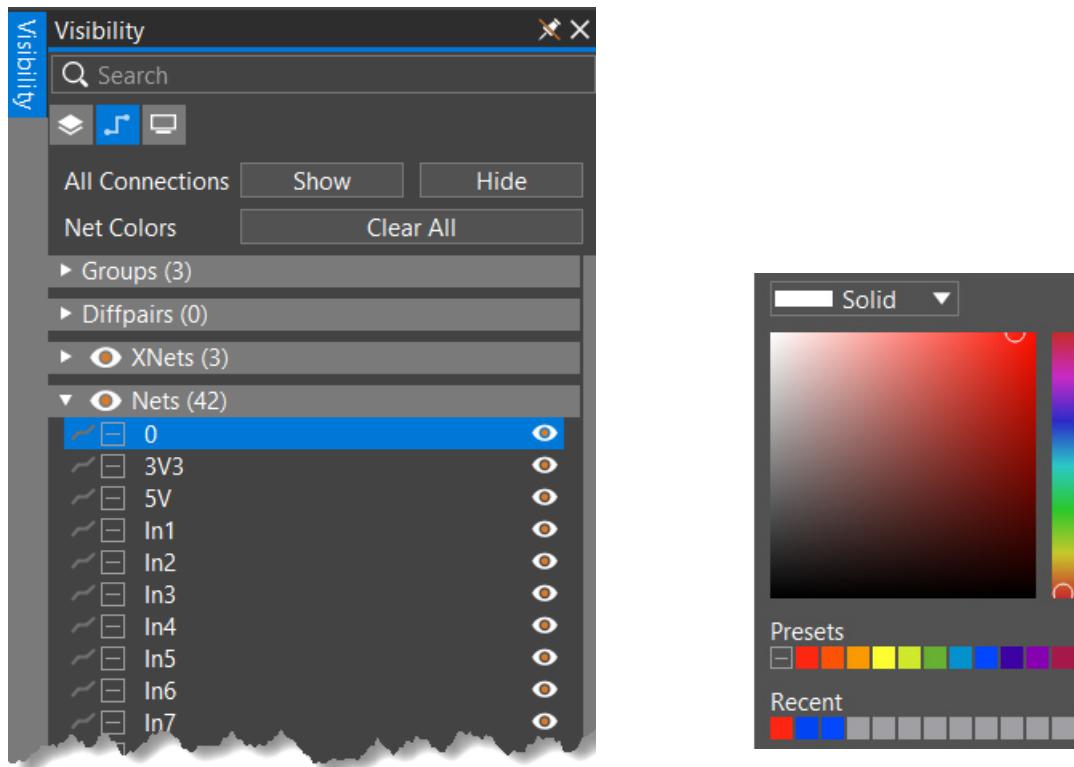
Changing the visibility of power and ground nets makes them easier to route. To change the visibility of nets, follow these steps:

1. Choose *View – Panels – Visibility* to open the *Visibility* panel.
2. Expand the *Nets* pane and select the net 0 from the list.

OrCAD X Capture with OrCAD X Presto Tutorial

Routing Nets Interactively

3. Click the color box associated with the net 0 and choose blue from the *Presets*.

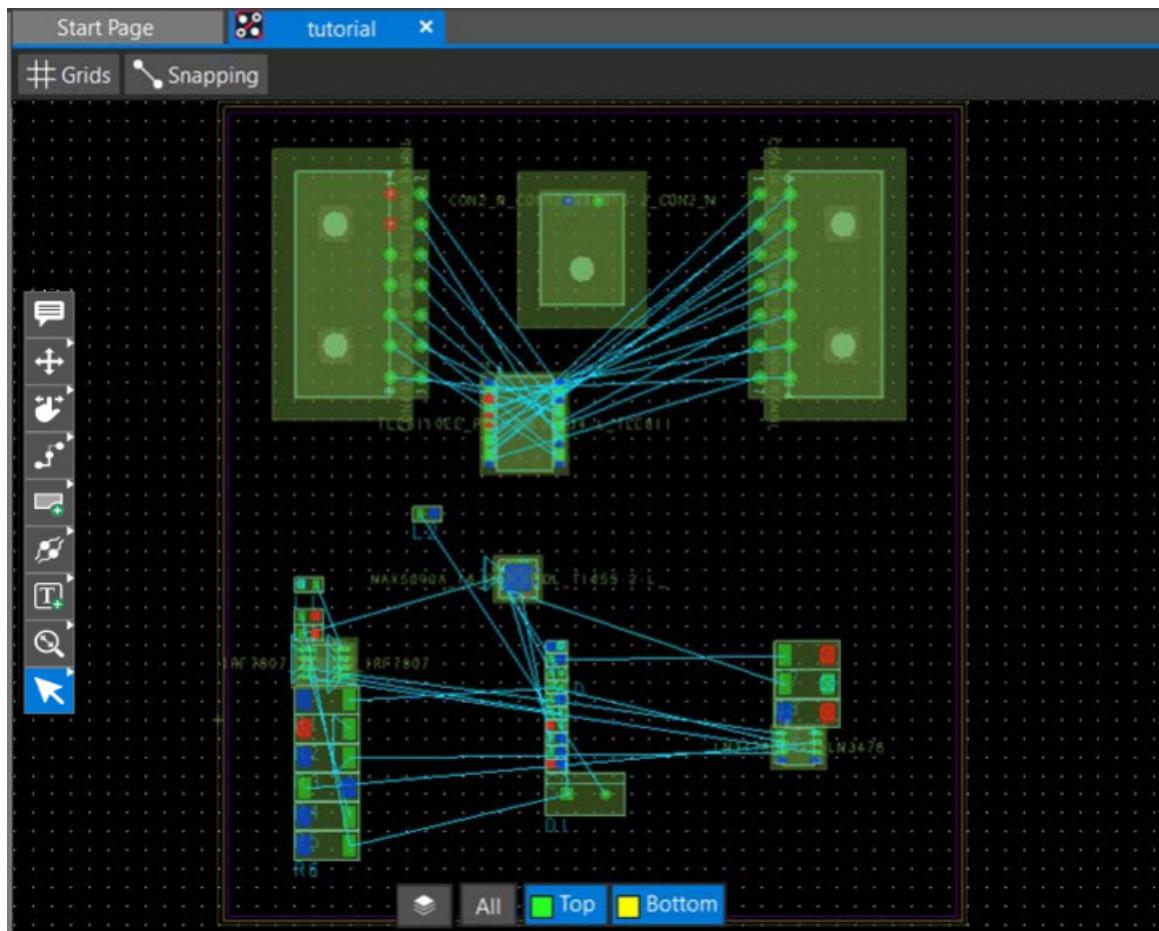


All the pins, vias, traces, and shapes that are connected to net 0 are shown in blue on the design canvas.

OrCAD X Capture with OrCAD X Presto Tutorial

Routing Nets Interactively

4. Similarly, change colors for 3V3 and 5V to red in the *Presets*.



All the pins, vias, traces and shapes that are connected to nets 3V3 and 5V appear in red in the design.

5. Choose *File – Save tutorial.brd* to save the design.

Routing Design Interactively

You can route a design in the interactive mode using various options. To route the design in OrCAD X Presto, do the following:

1. Click the *Add Connect*  icon from the functional toolbar.

A pane opens, providing options for routing single connect lines (traces) and differential pairs.

2. Set the *Route Mode* to *Manual*.

OrCAD X Capture with OrCAD X Presto Tutorial

Routing Nets Interactively

3. Set *Trace Width* to *Constraint*.

This setting takes the connect line width as defined in Constraint Manager.

4. Select a net to connect it to symbols, J3 and U2 and start routing.

The trace is added on the TOP layer.

5. To route the trace on the BOTTOM layer, double-click to insert a via.

6. To adjust the route, click the *Slide* icon from the functional toolbar.

A pane opens with options to slide the traces.

7. Set the *Slide Mode* to *Manual*.

8. Manually route all the nets in the design.

9. Click the zoom fit icon from the functional toolbar to view the complete design.



OrCAD X Capture with OrCAD X Presto Tutorial

Routing Nets Interactively

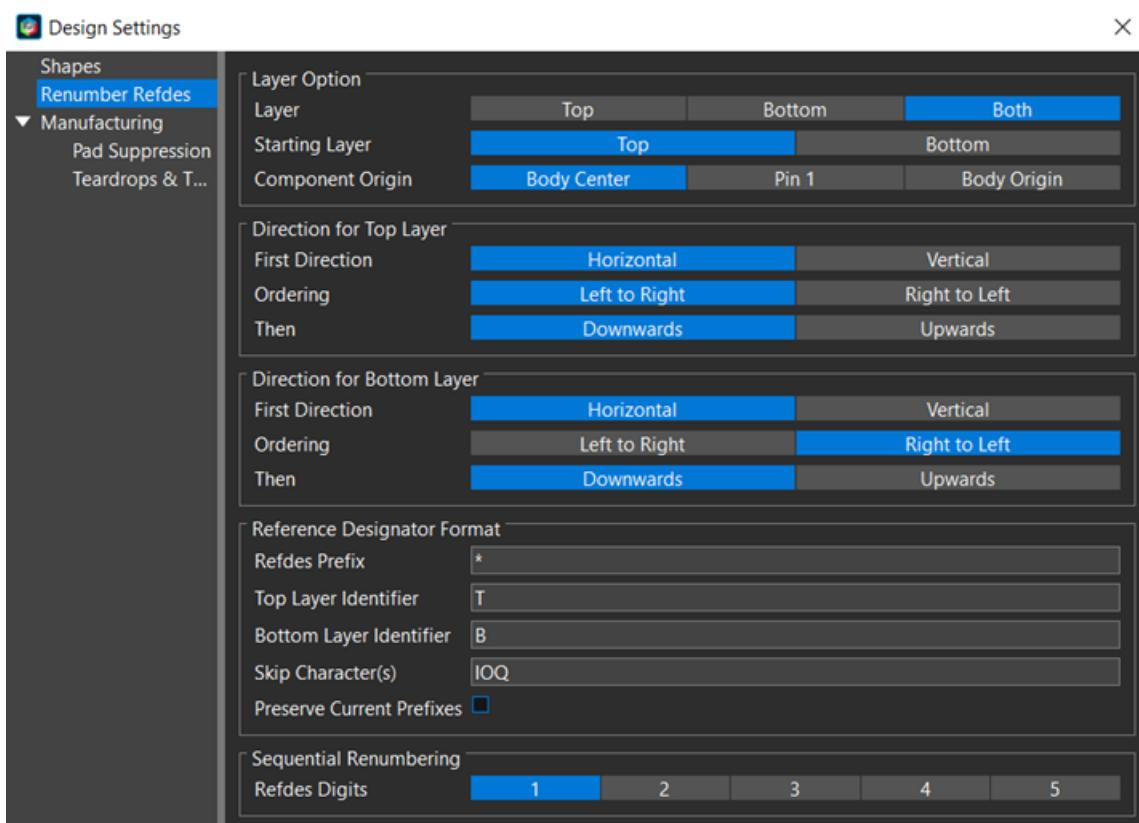
10. To verify that all the nets are routed, check the design status for *Unrouted Nets* in the *Properties* panel.
11. Choose *File – Save tutorial.brd* to save the design.

Renaming Components

After you have completed the placement and routing you can reorder the reference designators of components on the board in a specific pattern. This step makes the testing and assembly process easier.

1. Choose *Setup – Design Parameters Editor*.

The *Design Settings* dialog box opens and displays *Renumber Refdes* page.



2. In the *Design Settings* dialog box, make the following changes:

- a. Remove layer identifier for TOP and BOTTOM layers.
- b. Enable the *Preserve Current Prefixes* check box.
- c. Close the dialog box.

3. Choose *File – Save tutorial.brd* to save the design.

For more information, see [Quick Reference Guide to OrCAD X Presto Interface and Commands](#) in the documentation set.

Summary

This section covered the steps for setting up constraints required to route the board design and also introduced a set of routing commands to route the nets in a board design, interactively.

Validating the Design

This section covers how to use the 3D analysis and report generation functions to validate the routing and placement of the board design to make it ready for manufacturing.

OrCAD X Presto has a built-in 3D visualization capability that lets you preview the board design at any time during the design process. You can open the design in 3D and verify the design as a complete assembly. To analyze a design, 3D models must be assigned to all the symbols. You can map a 3D model either at a symbol level or at the design level. For the components used in this tutorial, 3D models are mapped with symbols.

Analyzing the Design in 3D

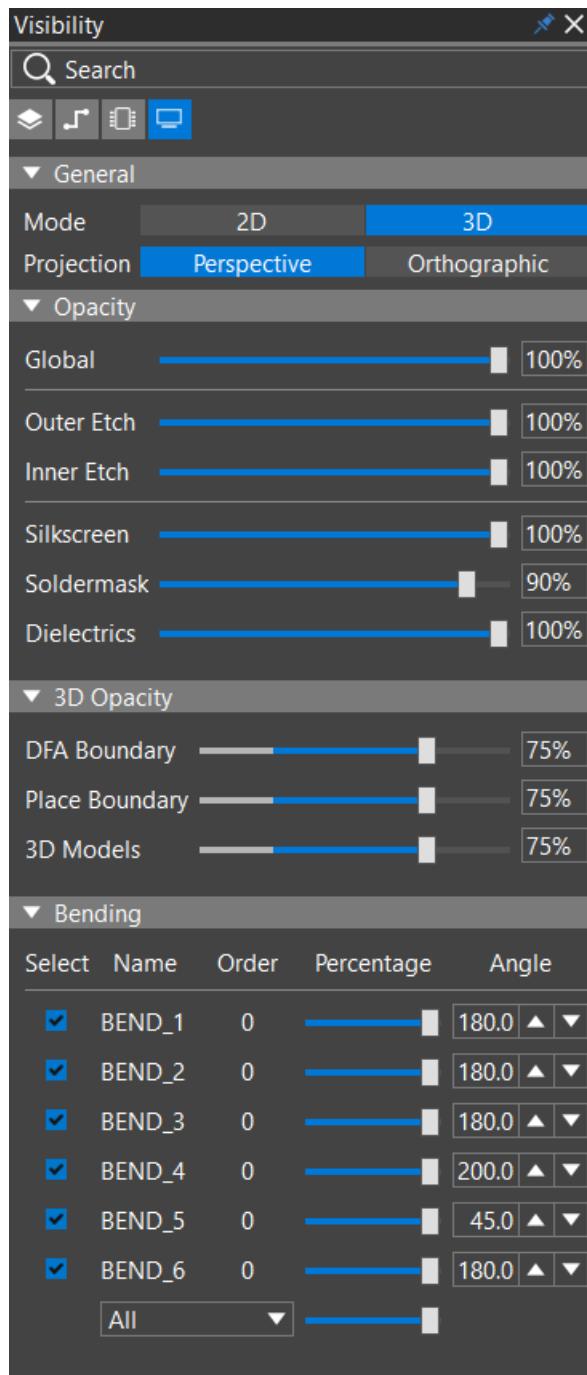
To do 3D analysis of a design, follow these steps:

1. Choose *View – Panels – Visibility* to open the *Visibility* panel.

OrCAD X Capture with OrCAD X Presto Tutorial

Validating the Design

2. In the *General* pane, switch the display mode from *2D* to *3D*.



OrCAD X Capture with OrCAD X Presto Tutorial

Validating the Design

3. OrCAD X Presto generates the 3D view of the active design and loads it under the design name tab of OrCAD X Presto.

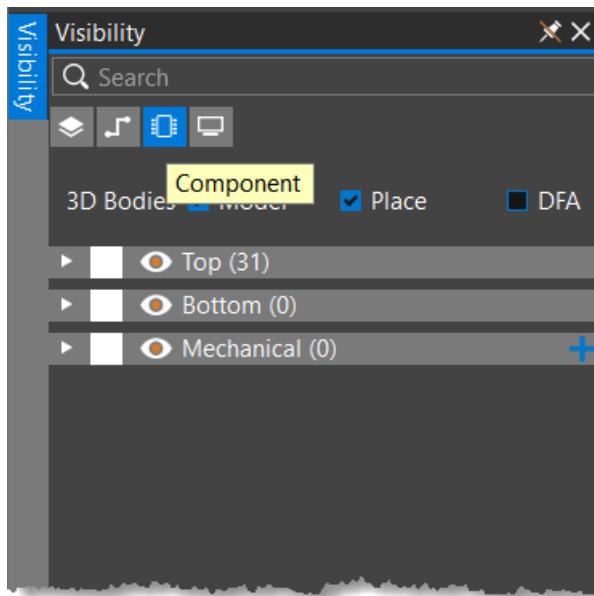


4. To control the visibility of symbols, open the *Component* pane of the *Visibility* panel.

OrCAD X Capture with OrCAD X Presto Tutorial

Validating the Design

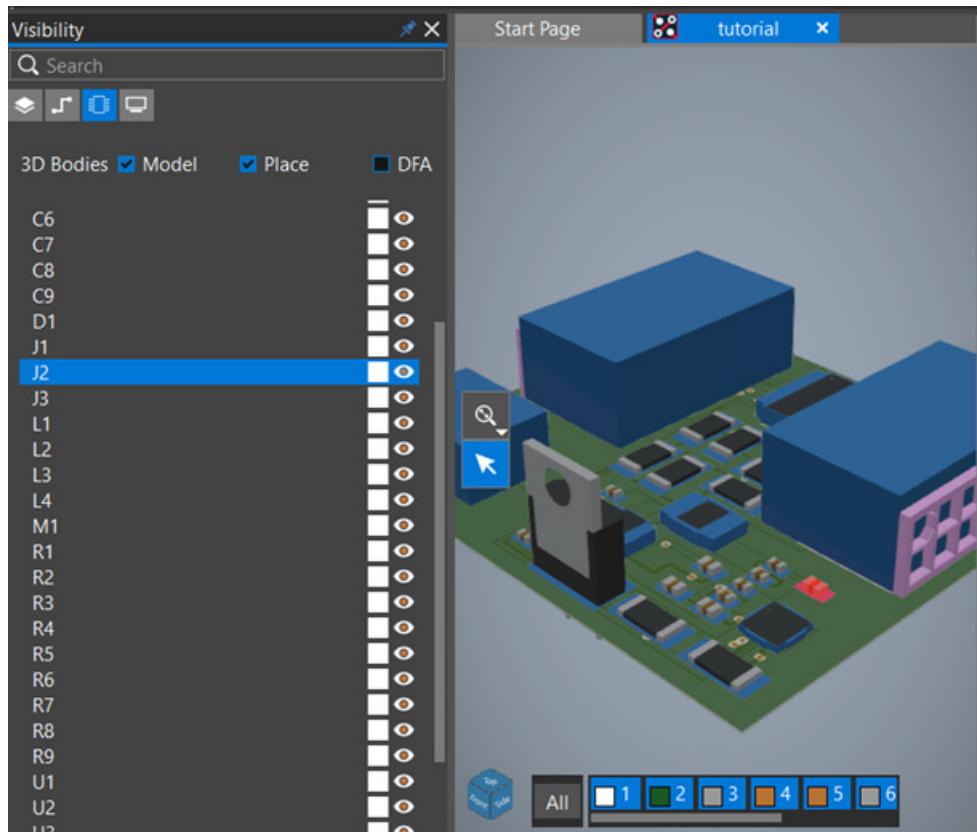
The symbols are listed under the layer names.



OrCAD X Capture with OrCAD X Presto Tutorial

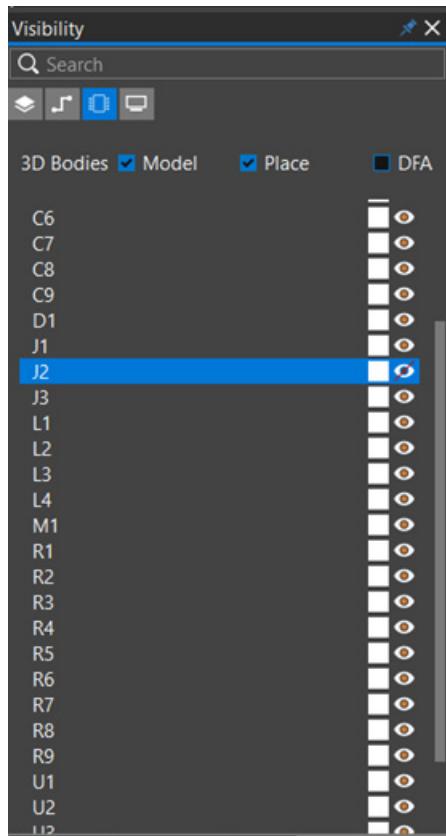
Validating the Design

5. Expand *Top* to view the symbols in the *TOP* layer, and toggle the visibility for *J2*.



OrCAD X Capture with OrCAD X Presto Tutorial

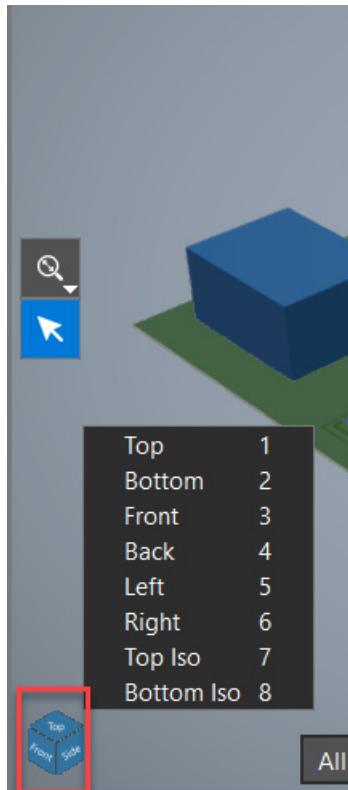
Validating the Design



OrCAD X Capture with OrCAD X Presto Tutorial

Validating the Design

6. Click the 3D cube to choose camera options from the shortcut list for analyzing the design in different perspectives.



7. Click anywhere or press Esc to hide the shortcut list.
8. Click the layers toolbar to show and hide design layers while reviewing the design.

Generating Reports

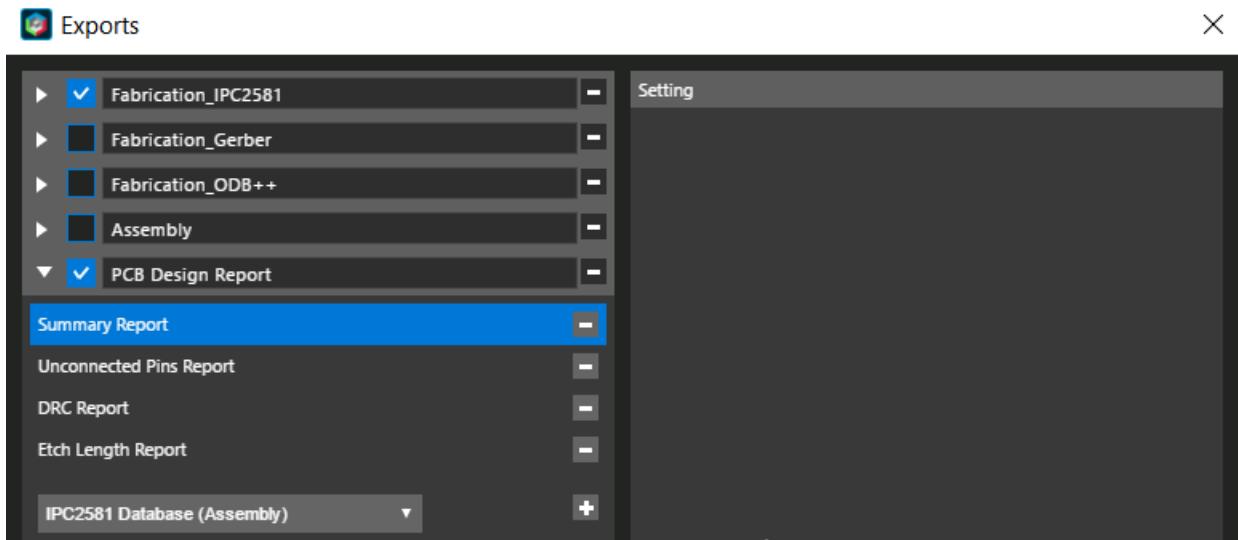
You can generate reports to extract design information from the board design. To generate reports in OrCAD X Presto, do the following:

1. Ensure that you have switched back to the 2D display mode.
2. Choose *Manufacturing – Export to Manufacturing*.
3. In the *Exports* dialog box, select the *PCB Design Report* check box.
4. Ensure that *Summary Report*, *Unconnected Pins Report*, *Etch Length Report*, and *DRC Report* are added.

OrCAD X Capture with OrCAD X Presto Tutorial

Validating the Design

5. Remove *Database Diary Report* from the list using  control.



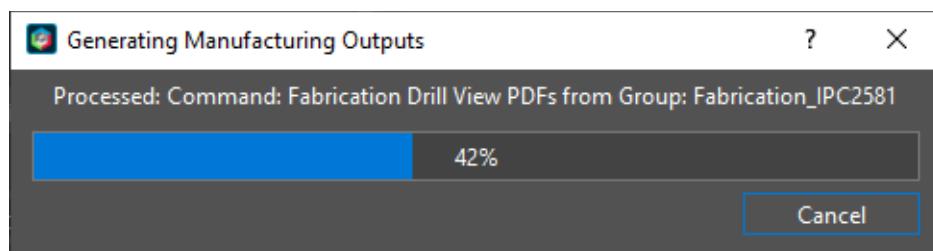
6. Deselect the *Create Archive* option.

7. Click *Export* to generate reports.

A confirmation message appears informing that the current Gerber layer definitions will be replaced with new definitions.

8. Click *Yes* to proceed.

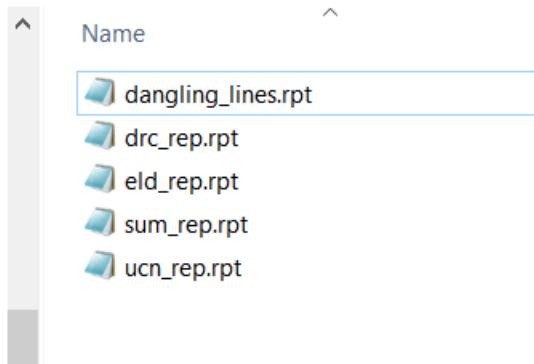
A progress bar is displayed:



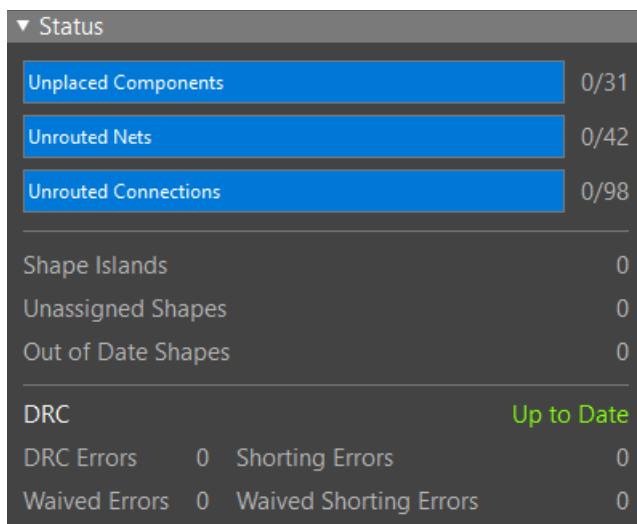
OrCAD X Capture with OrCAD X Presto Tutorial

Validating the Design

Reports are generated in the *fan_module_PCB Design Report* folder in the working directory.



9. Open the saved report in a text editor.
10. Click *Close* to close the *Exports* dialog box.
11. To verify the design status, check the *Status* pane in the *Properties* panel.



The status indicator for DRC is turned green and displays *Up to Date*.

Summary

This section covered the 3D analysis and report generation functions for validating the routing and placement of the board design to make it ready for manufacturing.

OrCAD X Capture with OrCAD X Presto Tutorial

Validating the Design

Exporting Manufacturing Output

In this section, you will create standard output files required by the fabrication houses to manufacture a PCB. The steps included in this section help you generate the following types of output files:

- Artwork (Gerber): OrCAD X Presto reads film control records to determine the number of artwork files to produce, their names, and the list of classes and subclasses to include in each artwork file.
- NC Drill: NC Drill output files are created for numerically-controlled (NC) drills and router and help in assessing the cost of PCB manufacturing. The drill output files include drill legend tables and drill files. Drill legend tables are used in fabrication drawing and show the number, type, and tolerance of plated and non-plated holes in the design. An NC drill file is created based on the parameters specified for the drill coordinate data format.
- IPC 2581: IPC2581 is an XML-based data exchange format used for providing physical design data for fabrication and assembly of PCBs.

Generating Output Files

In OrCAD X Presto, you can generate all the required fabrication and assembly data from the *Exports* dialog box. You can select the type of manufacturing output and generate all the data in an archived file in a single step.

To generate output files, follow these steps:

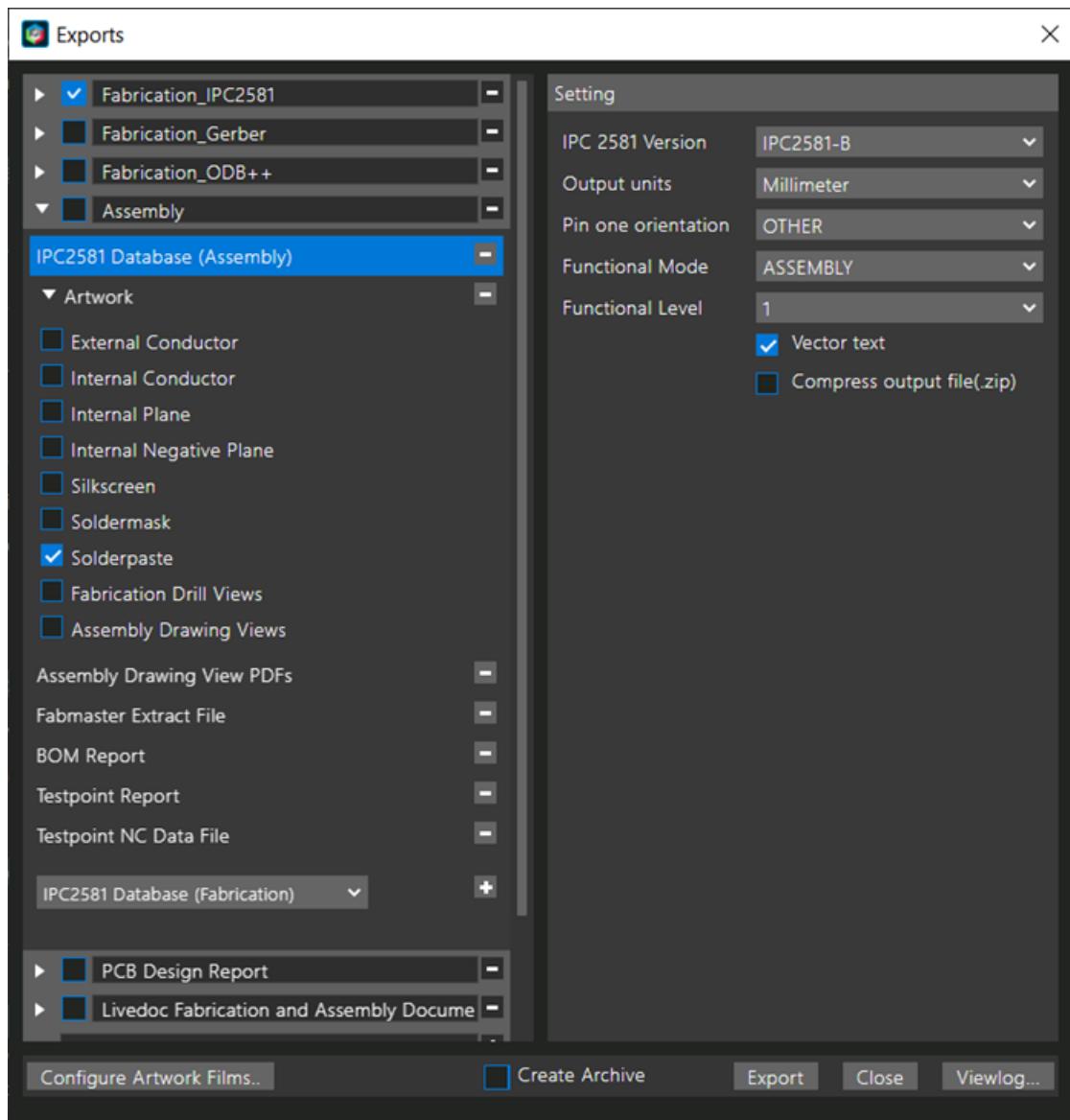
1. Choose *Manufacturing – Export to Manufacturing*.

The *Exports* dialog box opens. The left pane of this dialog box displays processing groups and associated manufacturing outputs. The settings are displayed in the right

OrCAD X Capture with OrCAD X Presto Tutorial

Exporting Manufacturing Output

pane for the selected manufacturing output type. You can add or remove export groups or manufacturing outputs using or controls.



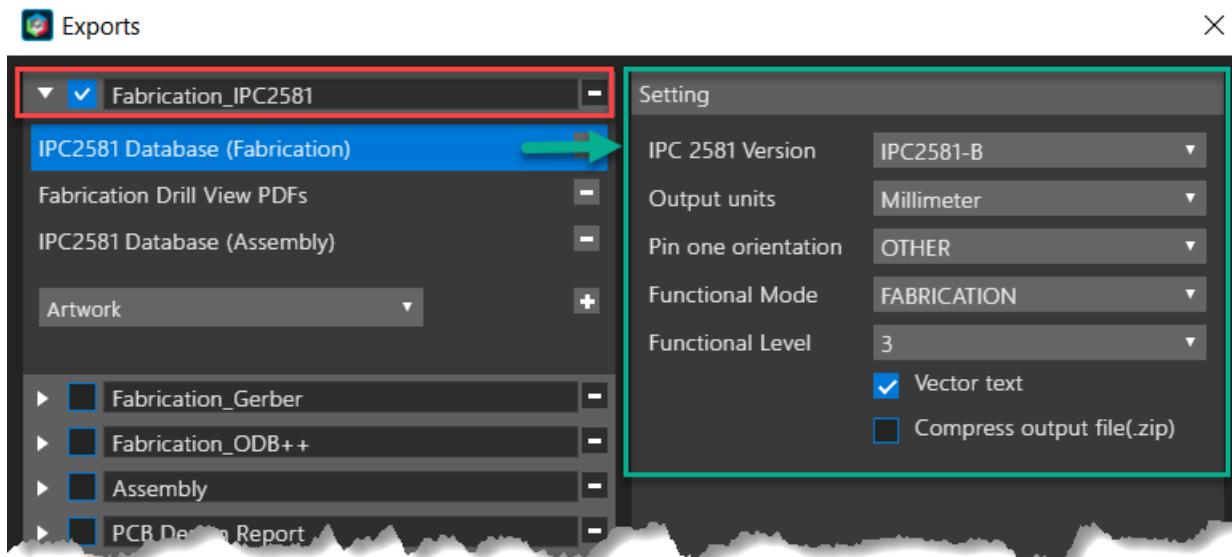
2. Enable the first export group *Fabrication_IPC2581* and do the following:

- Click to select *IPC2581 Database (Fabrication)* from the list.

OrCAD X Capture with OrCAD X Presto Tutorial

Exporting Manufacturing Output

The settings for IPC2581 database are displayed in the right pane



- b. In the *Settings* section, specify the following for *IPC2581 Database (Fabrication)*:

 - Set *IPC 2581 Version* to *IPC2581-B*.
 - Set *Output units* to *Millimeter*.
 - Set *Functional Mode* to *DESIGN*.
 - Set *Functional Level* to *3*.
- c. Remove *Fabrication Drill View PDFs*.
3. Enable export group *Fabrication_Gerber* and do the following:

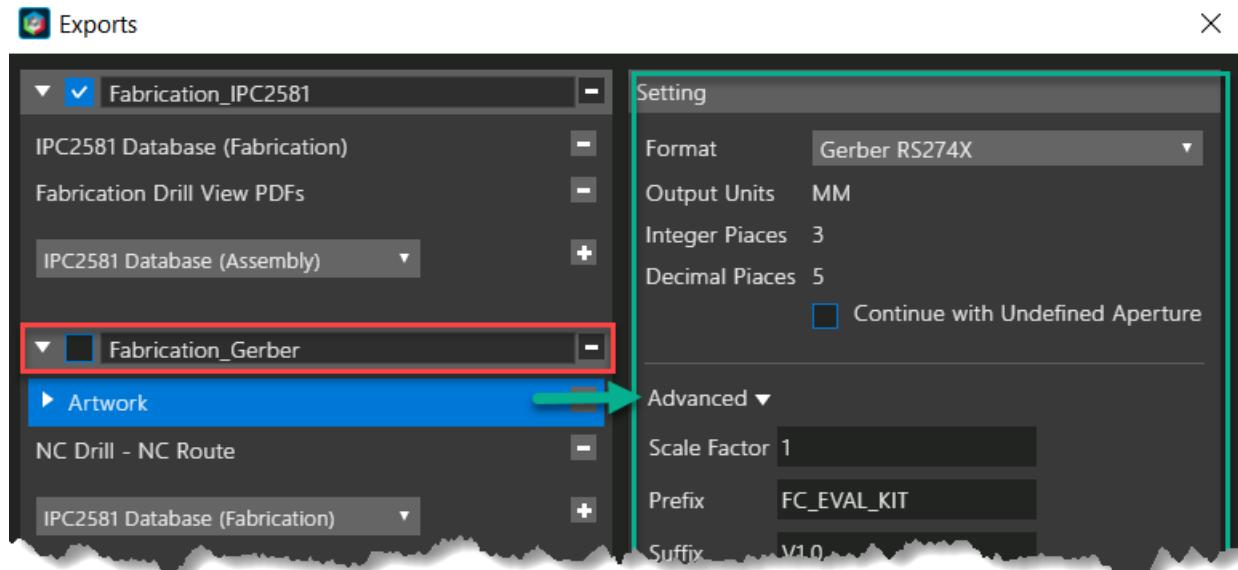
 - a. Click *Artwork* manufacturing output.

The Artwork settings read the cross-section and auto-generate one film record for each etch subclass, and include etch, pins, and vias.
 - b. Do not modify Artwork settings.
 - c. Click to select *NC Drill – NC Route* manufacturing output.
 - d. Do not modify *NC Drill* settings.

OrCAD X Capture with OrCAD X Presto Tutorial

Exporting Manufacturing Output

- e. Remove *IPC-D-356 Netlist*, *Backdrill Report*, *Fabrication Drill View PDFs*, *Artwork Film Record PDFs*.

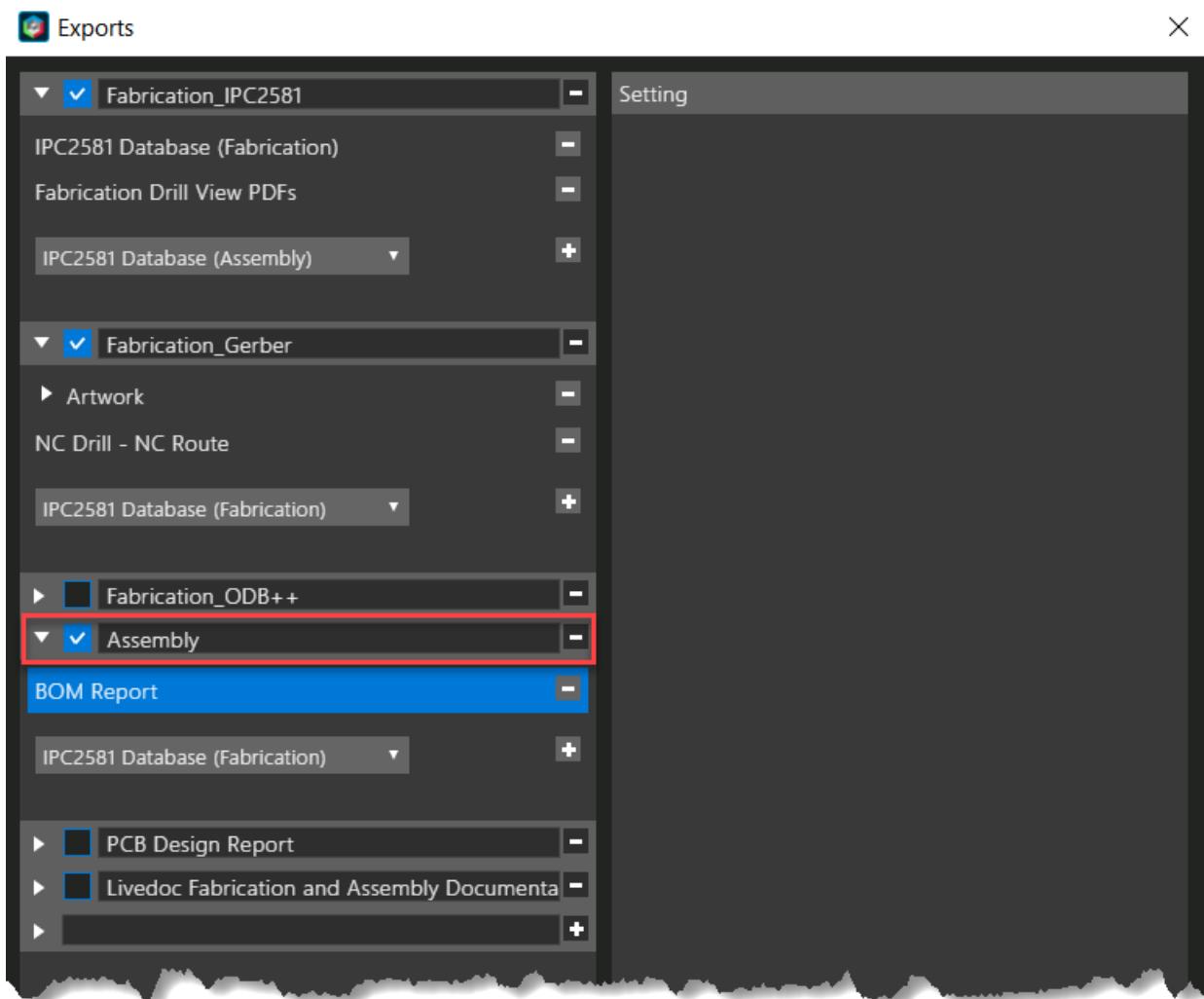


4. Enable export group *Assembly* and ensure that the *BOM Report* option is added.

OrCAD X Capture with OrCAD X Presto Tutorial

Exporting Manufacturing Output

5. Remove all the other types of outputs under the *Assembly* export group.

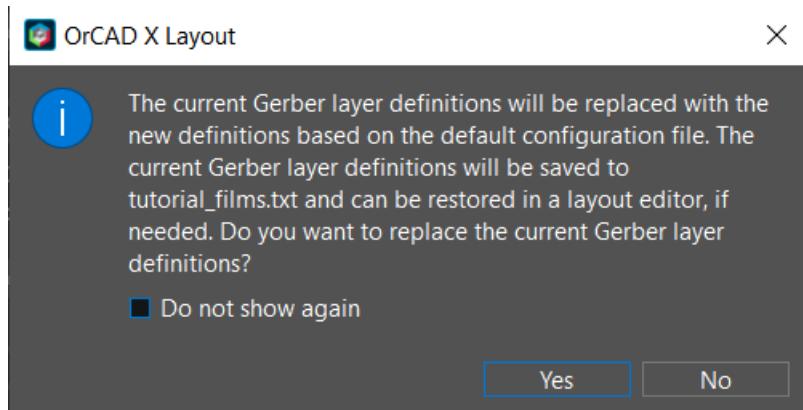


6. Ensure that the *Create Archive* option is enabled.
7. Click *Export* to generate all the selected manufacturing outputs as archived files.

OrCAD X Capture with OrCAD X Presto Tutorial

Exporting Manufacturing Output

8. Click Yes in the following message prompt.



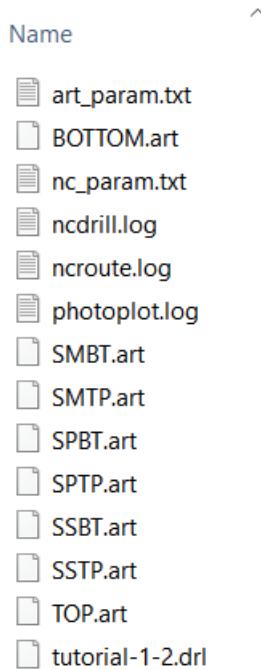
A progress bar displays the status of the export process.

9. Click *Viewlog* to open `single_exports.log`.
10. Open the working directory and verify the following output files:
 - a. `fan_module_Fabrication_IPC2581.zip`,
`fan_module_Fabrication_Gerber.zip`, and `fan_module_Assembly.zip` are created.
 - b. Extract all the archived files.
 - c. The `fan_module_Fabrication_IPC2581` folder contains `ipc2581_out.log` and `fan_module.xml` files.

OrCAD X Capture with OrCAD X Presto Tutorial

Exporting Manufacturing Output

- d. The *fan_module_Fabrication_Gerber* folder contains artwork for the TOP and BOTTOM layers, drill data, and the log files as shown in the following image:



- e. The *fan_module_Assembly* folder contains extract.log and bom_rep.rpt files.

11. Close the *Exports* dialog box.

Summary

This completes the task of creating a board design and generating manufacturing files for the board design. In this section, you were introduced to the steps for generating artwork and IPC 2581 data for design hand off.