Allegro® X
PCB Editor User Guide: High Density Interconnect (HDI)

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Contents

Working with HDI

The design methodology of high-density interconnect (HDI) technology allows for greater wiring density, utilizing lines and spaces under 3 mils and microvias (holes less than 6 mils, capture pads less than 13.8 mils) leading to greater miniaturization and reduced package size.

This section describes these key aspects of HDI requirements and the tool features supporting them, such as microvias, DRCs for same net and net-net conditions, unused inner-layer pad removal, rules for via tangency (vias touch but do not overlap) and stacking (coincident location of adjacent layer vias), and dynamic filleting.

Microvias and Padstacks

Microvias are a principal feature of HDI, defined by the IPC as vias whose diameter is less than 6 mils with capture pads less than 13.8 mils. Microvias set up the clearance matrix associated with the technology, such as microvia-to-microvia and microvia-to-core via spacing rules. Prior to 16.2, all non-standard vias (buried and blind) were categorized by the database object BB Via. Allegro PCB Editor lets you differentiate microvias from mechanically drilled blind and buried vias using the *Microvia* option on the `Padstack Editor`.

Pad Usage Options

■ *Microvia*: Use on HDI boards where spacing rule sets differ between HDI and conventional blind and buried or core vias. The Microvia option can only be applied to a blind and buried via to represent mechanical drilled vias, such as the core via on an HDI design. The Spacing and Same Net Spacing Constraint domains of Constraint Manager support these two via types.

■ *Allow Suppression of Unconnected Internal Pads*: Enable to suppress unused inner layer pads, thereby making them unavailable for DRC, routing, and display, with the *Suppress Unconnected Pads* option on the *Film Control* tab of the Artwork Control Form, available by choosing *Manufacturing – Artwork* (`film param` command) or with dynamic unused pad suppression, available by choosing *Setup – Cross Section* (`xsection`command).

■ *Enable Antipads as Route Keepouts (ARK):* Enable to use antipads associated with mechanical pins as an implicit route keepout area to reduce the need to draw keepout shapes associated with the mechanical symbol. Use in conjunction with the design-level

mechanical hole DRCs. You can activate mechanical hole checks in the Analysis Modes dialog using *Setup – Constraints – Modes* menu in layout editors or *Analyze – Analysis Modes* menu option in Constraint Manager.

For more information, see the Padstack Designer in the *Allegro PCB and Package Command Reference* and *Types of Padstacks You Can Create* in <u>Defining and Developing Libraries</u> in your documentation set.

Non Standard Drill Types

The Padstack Editor supports the following list of Non-standard drill types, most of which are used for HDI vias. These drill types are exclusively used with NC Drill applications and do not contribute toward Design Rule Checks. Use these non-standard types if you wish to separate those drills into their own individual files.

■ Laser

■ Plasma

■ Punch

■ Wet/Dry Etching

■ Photo Imaging

■ Conductive Ink Formation

■ Other

For more information, see the Padstack Designer in the *Allegro PCB and Package Command Reference*.

User-Definable Mask Layers

The Padstack Editor supports up to16 user-definable mask layers. Mask layers can be used for custom applications, such as via plugging, filling, and gold deposition. DRC checking is not performed on these layers.

Figure 1-1 Mask Layers
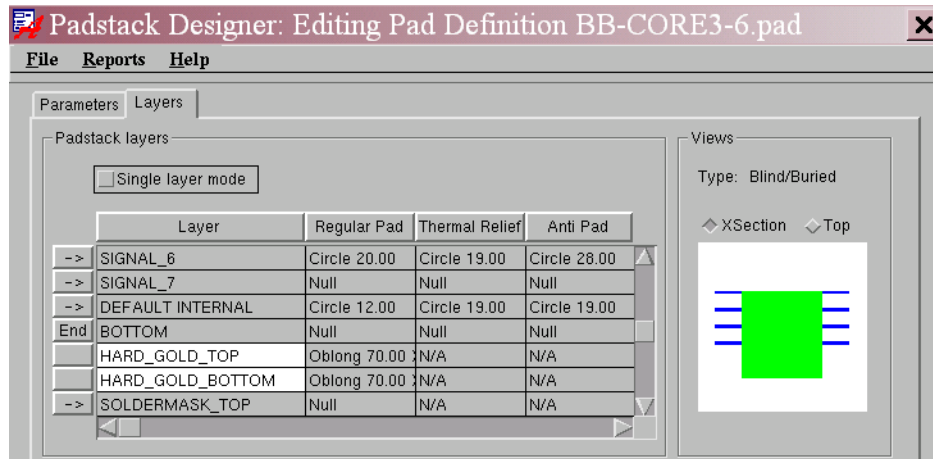
For more information, see the Padstack Designer in the *Allegro PCB and Package Command Reference* and *Developing Libraries* in your documentation set.

Plural Microvias

Plural vias are used in high current applications. The plural or *Multiple Drill* section of the Padstack Editor supports negative clearance entries if you want to overlap the drill hole.

Figure 1-2 Example of Multiple Microvias
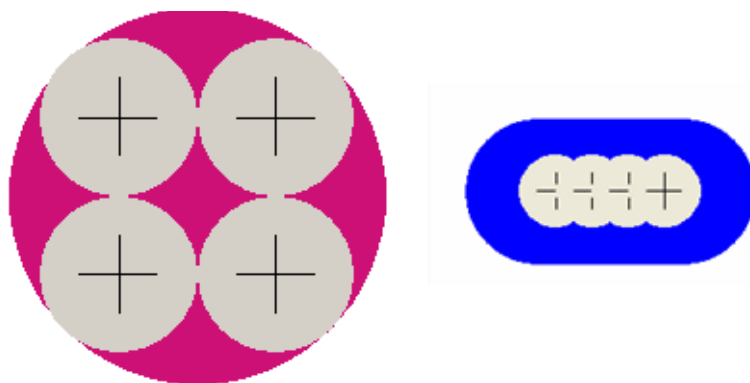
Blind and Buried Via Span Labels

Via span labels graphically identify the beginning and ending layers of a single via or a series of stacked vias using numerals within the pad extents. A colon between the beginning and ending layers indicates the span of a single blind and buried via; a dash represents a stacked series of blind and buried vias. Enable via span labels using the *Display* tab of the *Design Parameter Editor*, available by choosing *Setup – Design Parameters* (`prmed` command). The label's color defaults to white, but is customizable through the *Display* tab of the *Color* dialog box, available by choosing *Display – Color/Visibility* (`color192` command).

Layer numbers ascend in numerical sequence; for example, Layer Top = 1, Inner Layer 1 = 2, Plane 1 = 3, etcetera. The mapping between the display and actual layer names is not user configurable. Labels do not appear on through-hole vias or pins.

For more information, see the *Color* dialog box in the *Allegro PCB and Package Command Reference.*

Figure 1-3 Via Span Labels on Single (l) and Stacked Vias (r)
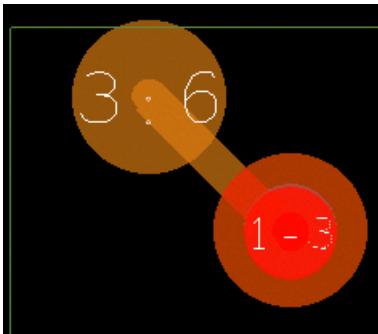
Via List Enhancements

The Via List, an object in the Physical Constraint Set, supports bitmaps and *Start/End* layer fields to identify the via type and its range. The list represents a selectable order of vias when used with *Route – Add Connect* (`add connect` command).

For more information, see the *Edit Via List* in the *Allegro Constraint Manager Reference.*

Figure 1-4 Via List

Blind or buried via

Through Hole Via

Microvia

Die Pad

Surface Mount Pad

Via list:			
Name	Start	End	
BB1-2	TOP	SIGNAL_2	
BB2-3	SIGNAL_2	SIGNAL_3	
BB-CORE3-6	SIGNAL_3	SIGNAL_6	
BB6-7	SIGNAL_6	SIGNAL_7	
BB7-8	SIGNAL_7	BOTTOM	
VIA019	TOP	BOTTOM	

Same Net DRC Overview

Using the Same Net Spacing domain in Constraint Manager, the Same Net DRC system drives many rules for via tangency (vias that touch) and inset (vias that overlap) used on HDI designs.

Each Spacing DRC has a respective Same Net DRC whose values can be set independently of Net to Net Spacing DRCs. For example, a Via to Pin rule can now be set to 6 mils Net to Net and 3 mils for Same Net. Same Net DRC error codes are a lower-case version of those for Net to Net. Same Net DRC modes can also be set on an individual basis.

Spacing differentiation is available for the following via combinations:

■   Microvia to Microvia

■   Microvia to Core Via (represented as blind and buried Via)

■   Microvia to Thru-hole

■   Core Via to Core Via

■   Core Via to Thru-hole

Etch edit applications align with the changes made to the Same Net DRC system, including bubbling, which makes sliding vias to other vias or pins on the same net more efficient. The add-via model adds via structures while obeying Same Net rules. Physical domain settings

control stacking, and stacked vias are seen as a group entity with options for breaking the stack when necessary.
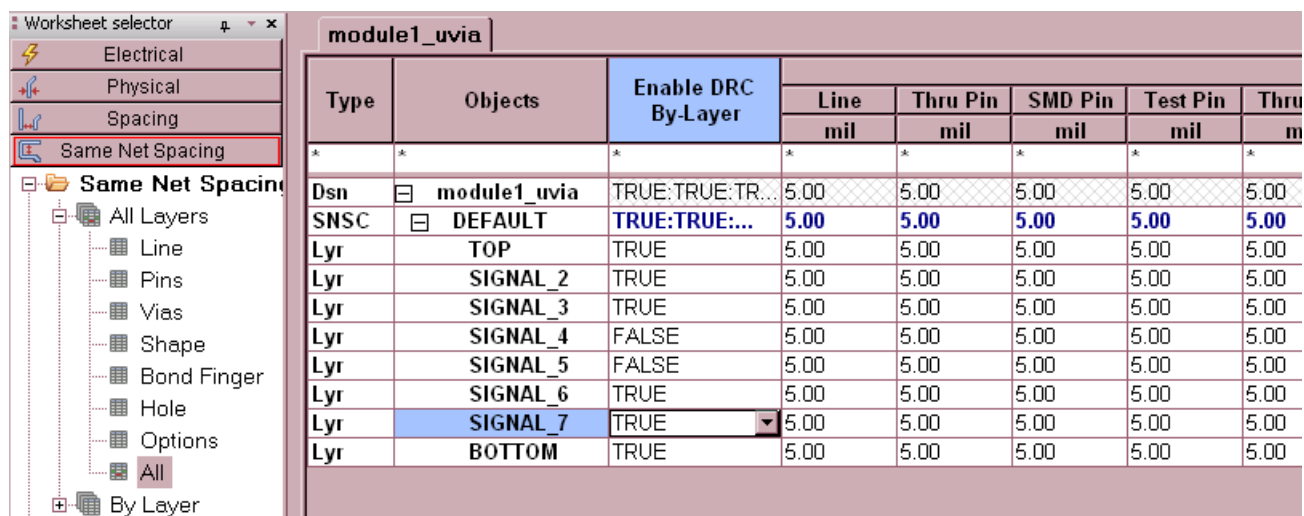
For more information, see *Working with Constraint Objects* in the *Constraint Manager User Guide*.

Constraint Manager – Same Net Spacing Domain

Same Net Spacing rules are managed entirely within the Same Net Spacing domain in Constraint Manager. An equivalent Same Net DRC represents each Spacing DRC. The Same Net domain is structured similarly to the Spacing domain, in terms of constraint inheritance and overrides. Constraint objects unsupported in the domain are Net Class-Class and Region Class-Class, as they are used exclusively for net-net rules.

For more information, see *Domains, Workbooks, Worksheets, and Cells* in the *Constraint Manager User Guide.*

Figure 1-5 Same Net Spacing Domain

Same Net Constraint Set

The Same Net system supports a Same Net CSet, abbreviated SNSC, which can be applied to net or hierarchical elements. The CSet enables the Same Net DRC on a layer basis.

For more information, see the *Objects – Create – Same Net Spacing CSet* command in the *Constraint Manager Reference.*

Same Net Spacing Modes

Mode settings are supported for each Same Net constraint. Unlike Net to Net, where all spacing constraints are usually relevant, Same Net requirements are often a subset of the complete list. For example, it may be necessary to enable Same Net Via to Via, Line to Line, Pin to Via, but not Shape to Shape or Pin to Pin. Certain modes may produce DRCs that fall into an irrelevant category, such as those that may have been waived.

Figure 1-6 Same Net Spacing Modes
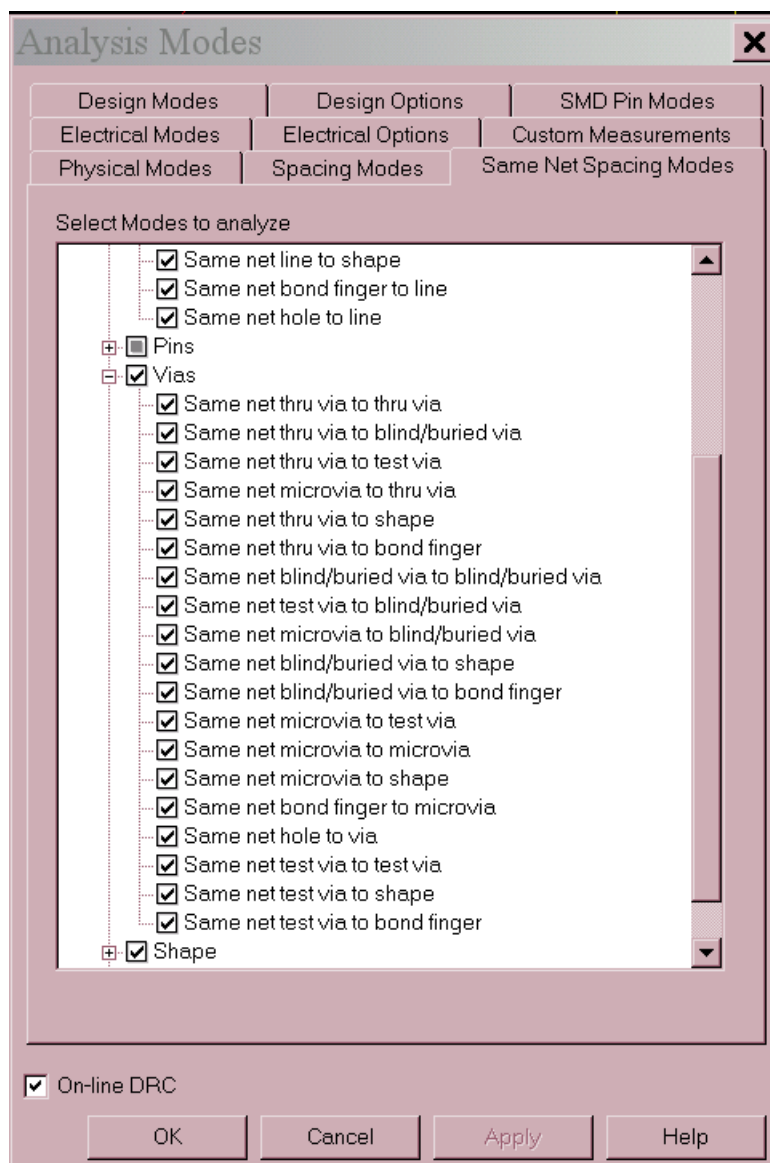
For more information, see the *Analyze – Analysis Modes* command in the *Constraint Manager Reference.*

Same Net Spacing - DRC Markers

Same Net DRCs utilize the same letter codes as Net to Net, but lower case. For example, a Net to Net via to via DRC is V-V; a Same Net DRC, v-v. The Constraint Manager – DRC workbook lists Same Net DRCs.

For more information, see the *Dictionary of DRC Error Marker Codes* in the *Allegro Platform Constraints Reference* and *Same Net Spacing DRC Modes* in the *Constraint Manager User Guide*.

Etch Edit Support for Same Net Rules

Etch-editing integrates the bubble code (shove/hug) to allow it to work with certain Same Net conditions. Sliding HDI vias in proximity with other vias or pins is more efficient due to the adherence of Same Net rules. Other enhancements include:

■ Sliding of via stacks as a single entity

■ Splitting the stack (etch now connected to via, previously orphaned)

■ Sliding a via, then snapping it into a stack if rules permit

■ Adding HDI via structures while obeying Same Net Rules during insert

■ Staggered, Stacked, and Inset

■ Sliding of vias from pad will maintain etch connection (previously orphaned)

Constraint Regions

Same Net rules are supported in constraint regions. The following figure shows region-defined rules for a Same Net SMD Pin to BB Via and Microvia. The blue font indicates values that are directly set or an override state. These terms are used interchangeably. An override supersedes values inherited from a CSet, and an override applies to all layers. If layer-based settings are required, assigning a CSet is recommended.

Figure 1-7 Constraint Regions
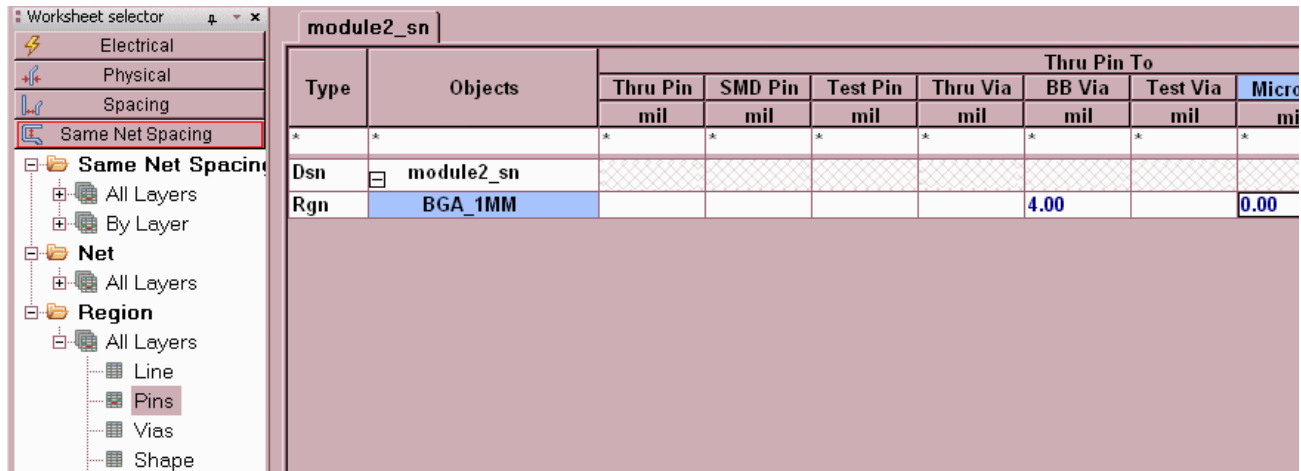
For more information, see the *Differential Pair Constraint Data Sheets* in the *Allegro Platform Constraints Reference* and *Differential Pairs* in the *Constraint Manager User Guide*.

Via-in-Pad Overview

Via-in-Pad is a common fanout strategy used on HDI designs, in particular on sub 0.5-mm BGAs. With Via-in-Pad, component placement can be more compact: Capacitors can be placed closer to the device pins they need to bypass. Via-in-pad also has its drawbacks, as it can introduce soldering issues in manufacturing. Solder can wick down through the open holes, if not plugged, drawing solder off the component pad.

Different rules may exist for metal- and soldermask-defined pads. For metal-defined pads, a via should be contained within the SMD pad boundary; otherwise, the solderpaste spreads to include the via, resulting in possible tomb-stoning of components.

With soldermask-defined pads, a via may be allowed to float within the SMD pad up to the point where the center of the via hole intersects the edge of the SMD pad.

Typically, thru-hole vias are not allowed in SMD pads. Thru-hole vias can result in solderpaste flowing down the hole barrel. However, capabilities must exist to allow such conditions for thermal, RF shielding, and power applications.

Component Fanout

The Allegro PCB Editor offers several interactive and automatic controls for component fanout, a process also known as pin escaping. The options include:

■ Fanout By Pick, which invokes Allegro PCB Router

■ Use of `.do` files to be used with Allegro PCB Router

■ Interactively add/copy within Allegro PCB Editor

■ Build fanouts into library symbols

■ Interactive fanout commands, including via structures for HDI

Via-in-Pad DRC Suite

Running at the design level, Via-in-Pad DRC ensures that vias are placed properly within SMD pads. Properties can be used to override these checks at the symbol level.

Via at SMD - Fit On targets metal-defined pad applications where vias must be totally contained within the boundary of the SMD pad. A DRC occurs if the via pad protrudes outside the SMD pad. The examples below show legal via-in-pad placement.

Figure 1-8 Via at SMD Fit On
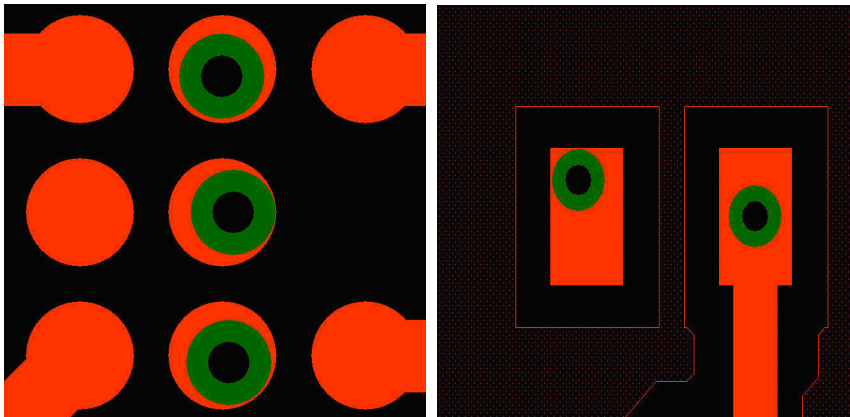
Via at SMD - Fit Off targets soldermask-defined pads where a via is allowed to float outside the edge of an SMD pad up to the point where the via center remains inside the SMD pad. Floating the via center beyond the pad edge results in acid trap formations. Other applications for this check might include vias placed in narrow SMD pads, ones typically associated with quad flatpack devices.

Figure 1-9 Via at SMD Fit Off
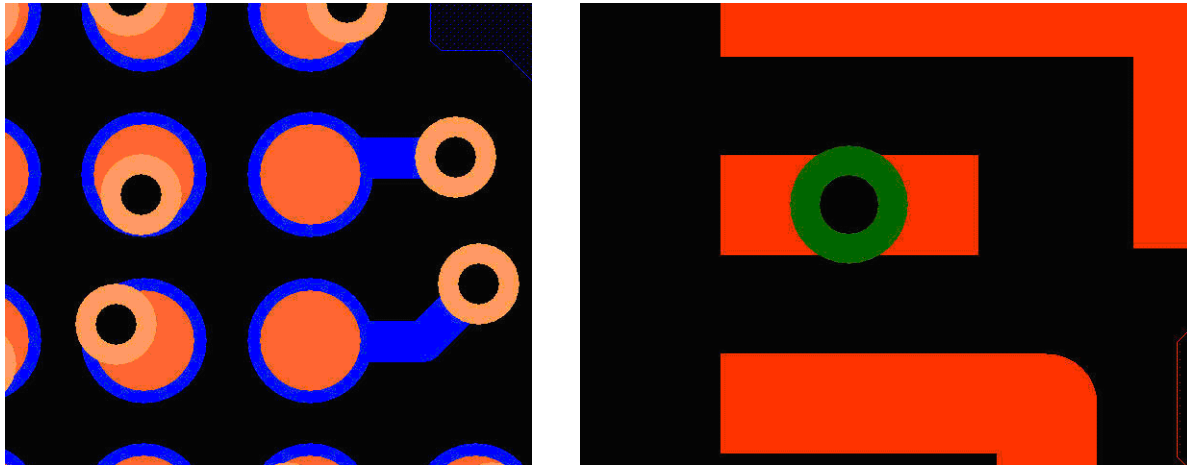
Via at SMD Thru detects placement of thru-hole vias within the SMD pad boundary.

For more information, see the *SMD Pin Data Sheets* in the *Allegro Platform Constraints Reference*.

Via in Pad DRC Mode Settings

Mode settings for Via-in-Pad constraints appear in *Constraint Manager – Analyze – Analysis Modes – SMD Pin Modes*. The constraints align with the names used in Allegro PCB Router.

■ Via at SMD Pin: On activates the Via-in-Pad DRC Check

■ Via at SMD fit: On indicates the via pad must be contained within SMD pad

■ Via at SMD fit: Off indicates the center of via cannot extend beyond the pad edge

■ Via at SMD thru: On indicates tat Thru vias are allowed in SMD pads

■ Via at SMD thru: Off indicates that Thru vias not allowed in SMD pads

Figure 1-10 Via in Pad DRC Modes
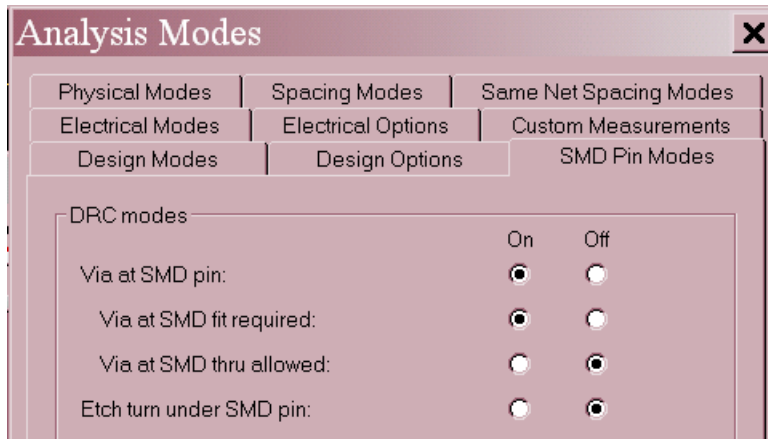
For more information, see the *Analyze – Analysis Modes* command in the *Constraint Manager Reference*.

Property Overrides

Not all packages may conform to a design-level check. It may be common to enable Via at SMD Pin Fit as a design-level check, but certain packages may lend themselves to disabling it. Specific properties are available for the Via at SMD Pin checks that override the design-level check:

■ VIA_AT_SMD_Fit applied to pins or symbols

■ VIA_AT_SMD_ Thru applied to pins or symbols

For more information, see the *Spacing and Same Net Spacing Data Sheets* in the *Allegro Platform Constraints Reference*.

For more information, see *Constraint Overrides* in the *Analysis Modes Constraints Reference*.

HDI Via Structures

This methodology to add both conventional and HDI via structures includes a working layer model based on the concept of multiple alternate layers, in conjunction with a via popup interface. Double-clicking in the canvas displays the Via Popup interface, populated by the layers enabled in the *Working Layer Setup* dialog box that displays along with access to the via list.

This combination automates the sequence of layer transitions using stacked, staggered, and inset vias by localizing the steps of layer transition near the point of occurrence to maintain focus on the working board area, limiting travel to side panels or to the toolbar during routing. Metrics can be established to measure increased productivity and efficiency, relative to the number of mouse clicks to complete a connection.

For more information, see _Use Models for Adding Vias_, in Chapter 8 of the _Routing the Design_ user guide in your documentation set.

Working Layer Model

A list of layers currently in use for routing, working layers offer more flexibility than the availability of a single alternate layer. Working layers are only valid within the Route Connect (`add connect` command) and are expected to be a subset of visible layers. The active layer is typically expected to be one of the working layers, but it is not required to be.

The Working Layers mode addresses the challenges of working on HDI designs. In this mode, the _Working Layers_ dialog box displays all the etch layers in the current design and controls the layers that appear in the Via Popup interface. Instead of being confined to routing from an active layer to a single alternate layer, a double-click in this mode launches the pop-up interface with all working layers available for selection. A single pick on any layer resumes routing on that respective layer. When routing to HDI rules, you can automatically add stacked vias or semi-automatically add staggered vias across multiple layers. Additionally, you do not need to continually navigate from your design to the _Options_ pane in order to select individual vias for each layer.

For more information, see _Adding Vias Using the Working Layers Mode_ in Chapter 8 of the _Routing the Design_ user guide in your documentation set.

Add Via Popup Interface

The Via popup interface combines the selection of a layer and a via into one graphical display. This facilitates the transition of signals across HDI layers, accounting for stacking and staggering rules, as well as standard thru-hole technology. For more information, see _Adding Preferred and Alternative Vias_ in Chapter 8 of the _Routing the Design_ user guide in your documentation set.

Ordered Via List

An ordered via list lets you select the target layer to which to route while Allegro populates the preferred vias in the layer series. In Working Layers mode, you must have predefined vias in

the constraint set via list for the layers upon which you want to route; however, this mode assumes that you have defined an "ordered via list" for CSets in Constraint Manager. The vias listed in the Edit Via List are available for adding when you route interactively

For more information, see *Setting Up Ordered Via Lists* in Chapter 8 of the *Routing the Design* user guide in your documentation set.

Stacked HDI Vias

A via stack comprises two or more Same-Net vias that are directly connected at the same location, with adjacent vias in the stack each sharing one common layer.

A Split Stack option available from a right-mouse popup menu allows one or more vias to be split from their via stack if required. When sliding a via (or stack of vias) outside the pin pad, a cline is added as necessary to avoid orphan vias, or those that become disconnected from the net.

Staggered HDI Vias

A microvia on one layer connecting to a via on the second layer can be staggered, or offset such that the pad diameters are tangential or greater when vias are not allowed to be stacked.

HDI Utilities

HDI design utilities automate interactive tasks, among them a line-fattening program that increases line width between tangent HDI vias, and a report and gloss application that detect and remove unused blind and buried vias in a stack.

Line Fattening between Tangent Vias

A post-route task associated with HDI design increases the line width between two tangent vias based on a user-defined, edge-to-edge clearance to remove the acute angle formation between the vias' junction.

Figure 1-11 Acute Angle at Junction

The algorithm determines the line width based on the smaller of the two vias. Available options let you waive impedance or maximum line width DRCs that may result. Run this utility near the end of the design process, as it's not possible to reset line width.

For more information, see *Route – Line Fattening* (line fattening command) in the *Allegro PCB and Package Command Reference.*

Elimination of Unused Blind and Buried Vias in a Stack

Often, vias in a stack may become orphaned due to changes made during routing or clip-boarding. The end result leaves unwanted vias that occupy valuable routing real-estate and also contribute to stub effects on the signal. Use either of the following:

■ Delete_hdiviastubs environment variable in the *Early Adopter* category of User Preferences, available by choosing *Setup – User Preferences* (enved command).

■ *Eliminate Unused Stacked Vias* option in the *Via Eliminate* application of the Glossing Controller, available by choosing *Route – Gloss – Parameters* (gloss param command).

Unused Blind and Buried Via Report

The *Unused Blind/Buried Via Report* detects unused buried or blind vias in a stack. Removing these vias can open routing real estate and reduce stub effects at the via site.

Run the report by using *Tools – Reports* (reports command).

Dynamic Unused Pad Suppression

Dynamic Unused Inner Layer Pad Suppression moves what has been historically a post-processing application to reduce capacitance effects at each hole site into the design database. Typically the fabricator's CAM department handled this application prior to film generation, and possibly the OEM removed the pads as a function of artwork generation.

With the ever-increasing demand to make product smaller, lighter and cheaper, unused inner layer pads are being removed not only for electrical but also for physical effects. Removing pads increases higher routing densities by allowing traces to be closer to the hole edge.

High-temperature, lead-free soldering requires that pads be left on unconnected thru pins, but not on unconnected vias. This application is not only object-based (pin versus via), but also layer based to retain the pads on thru pins on the signal layers closest to the surface layers.

User Interface

Unused Pads Suppression is available by choosing *Setup – Cross Section* (`xsection` command). Each layer of the stack-up is represented; conductor in yellow, planes in red. Settings for pins and vias can be enabled on a per- layer basis. Right-click and choose *Enable All Layers* to enable all layers under either the *Pin* or *Via* category. Enabling the *Dynamic Unused Pads Suppression* option automatically enables the display of padless holes.

Layer Restrictions

Layers unavailable for pad suppression include the Top and Bottom, negative planes, and the beginning and ending layers of a blind and buried via. Outer and plane layers display for reference only.

Other Restrictions

■ Pads associated with mechanical pins are not eligible for removal.

■ The pad definition must have the *Allow Suppression of Unconnected Internal Pads* option enabled to make a pad eligible for removal.

Figure 1-12 Allow Suppression of Unconnected Internal Pads Option
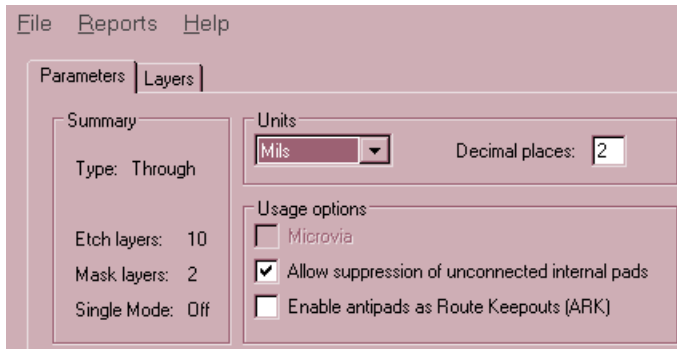
Dynamic Suppression

Pad suppression becomes dynamic once the *Dynamic Unused Pad Suppression* option is enabled, and the dialog box closes. Suppression or restoration occurs on the fly. Upon closing the form, all eligible pads are suppressed. Pads are restored as connections are made to pins or vias. In contrast, pads are dynamically suppressed if traces are deleted from pins or vias.

Disabling the dynamic option restores all pads on pins and vias. DRCs may result if traces become closer to the drill hole. The pad definition remains unchanged as a result of suppression.

Exception Properties

The UNUSED_PADS_IGNORE property prevents pad suppression at the symbol, net, pin, or via level. Once applied, pads remain static on the respective elements.

The UNUSED_PADS_OVERRIDE property allows pads to be removed on outer layers. The property is restricted to a symbol with values of Top, Bottom, or Top:Bottom. Consider using on edge connectors to minimize the amount of gold used during plating.

Artwork Alignment

When *Dynamic Unused Pads Suppression* is enabled, the legacy film control *Suppress Unconnected Pads* option and functionality appears enabled for all films, but grayed out and non-editable: Database-driven suppression occurs. If dynamic suppression is not enabled; however, the checkboxes are individually editable as needed, and legacy suppression occurs instead. Legacy suppression handles blind and buried vias where the begin and end layer pads must never be suppressed, even if unconnected and on an internal layer.

Router Interface

Full pad definitions pass to the Allegro PCB Router, which cause DRCs within the router application.

Drill to Metal DRC

Drill hole to metal-based checking covers both holes associated with circuitry (pins and vias) and holes associated with mechanical pins, where the antipad can be used as an implicit route keepout area.

Drill holes are commonly referred by their plating category; plated or non-plated. The suite of drill hole checks are based on Allegro PCB Editor pin types (connect and mechanical pins). Typically connect-pin-based holes are plated; mechanical-pin-based holes, non-plated. It is possible, however, to define each type as plated or non-plated. Logic can only be assigned to a connect pin.

The term hole is used in the DRC system and Constraint Manager as the drill hole associated with circuit-based pins and vias. Unlike computer-aided-manufacturing checks, where generic PTH to metal checking occurs against minimum constraint values, an integrated CAD system must provide the flexibility to check holes against the diverse set of net-based rules. For example, if the rules for a 60V net to GND via or pin require a 1-mm clearance, this same clearance would be required to the edge of the padless holes associated with these elements.

A hole-to-metal check occurs only when the respective hole is void of pads on conducting layers. This can be a result of Null pad entries in the padstack definition or instance or using the dynamic pad suppression. When pads exist on pins and vias, the hole check yields to the conventional pin and via checks.

The following example illustrates the potential benefits of drill-based checks. The channel width with pads present restricts the number of lines routed between the pin pads to just one. The removal of used pads, coupled with a hole-to-line space that permits the line to be routed closer to the hole edge but tangent to the annular ring, opens the channel to permit two lines between.

Figure 1-13 Drill-based Checks
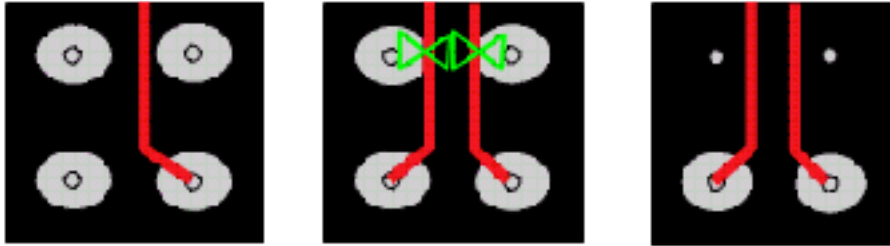
Constraint Manager Integration

Hole to metal-based constraints can be driven from Spacing CSets or directly set on Net-based objects in Constraint Manager. Both the Spacing and Same Net Spacing domains support a suite of Hole to (Line, Pin, Via, Shape and Hole) spacing checks. On new boards, hole-based constraints default to 8 mils; all other spacing constraints default to 5 mils. On uprev'd boards, hole-based constraints are derived from the Spacing CSets to ensure metal-to-hole spacing aligns with net-spacing rules.

A hole-to-metal DRC occurs when the hole is seen as the outer extent of the pin/via element. If a pad is present and larger than the hole, the spacing DRC heck geometry against the pad extents. Both a hole and a pin/via pad violation cannot occur on the same element.

Dynamic Filleting

The gloss-based fillet application updates fillets dynamically on pins, vias, or T-junctions. The application continues to support interactive or batch mode as well as existing parameters. The *Dynamic Fillets* option on the *Pad and T Connection Fillet* dialog box offers the convenience of filleting during interactive etch editing with no additional procedures. When this option is enabled, fillets are added when a connection is made to an element or deleted when removed.

Shape-based Fill

The fill associated with fillets has transitioned from line to shape-based. A single entity fillet is managed more efficiently in the database. For DRC considerations, the fillet should be regarded as an extension of the pin or via.

Parameters

Parameters associated with the fillet application include:

■ *Allow DRCs:* Creates fillets with DRCs.

■ *Dynamic Fillets:* Updates per parameter settings; fillets are then automatically added/ deleted during design editing.

■ *Curved Fillets:* Adds curved style fillets whose radius is determined by the algorithm.

■ *Max Line Width*: Prevent fillets from being added when the junction line width is equal to or greater than this value.

Fillet Algorithm

The algorithm first tries to create the fillet at the desired angle, tangent to the pad. If the fillet cannot be created, the angle increments to the *Max Angle*. If the fillet length, pad tip to vertex of fillet, is greater than the *Max Offset*, the vertex is adjusted by an amount to satisfy the *Max Offset* requirement. The end points of the fillet are adjusted by the same amount to maintain the angle.

Reporting

The *Missing Fillets Report* lists junctions with missing or partial fillets and is accessed with *Tools – Reports* or *Tools – Quick Reports*.