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Allegro® X PCB Editor - Frequently Asked Questions

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1

Frequently Asked Questions in PCB Editor

This document lists answers to the frequently asked questions about Allegro PCB Editor and its utilities.This document will be periodically updated to resolve the issues our customers face while working with Allegro PCB Editor.

To view the answer to any question, click that question in the list below.

How do I generate netlist in batch mode from PCB Editor in DOS mode?

How do I create user-specific license packages?

How do I fix space-related issues for MainWin on Linux?

Can I place two mechanical symbols in a layout design?

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Why does metal usage report show less percentage of metal for an embedded layer?

How do I pick a point on the canvas without snapping to the grid?

How do I generate artwork output files without extension?

Why does SHAPE_ISLAND_OVERSIZE DRC not report unrouted connections?

How can I check the height restriction for components?

How do I generate netlist in batch mode from PCB Editor in DOS mode?

To export back annotation netlist from layout editors in DOS, use `genfeedformat` batch program.

You can also run the `report` batch command from the DOS prompt. To generate a netlist report in CSV format, type either

```
report -v nbn <design> <netlist.txt>
```

or

```
report -v net <design> <netlist.txt>
```

How do I create user-specific license packages?

Allegro PCB Editor supports user-defined license packages to customize license configuration. CAD administrators can create a local license package file and use it at site level.

This local license package file contains a custom name for the package, base product license, and option licenses. The name of the file is `license_packages_<exe>.txt`, where `<exe>` can either be `allegro`, `apd` or `cdnsip`.

The file is located by CDS_SITE method using the *`localpath`* environment variable. The default path for this variable are:

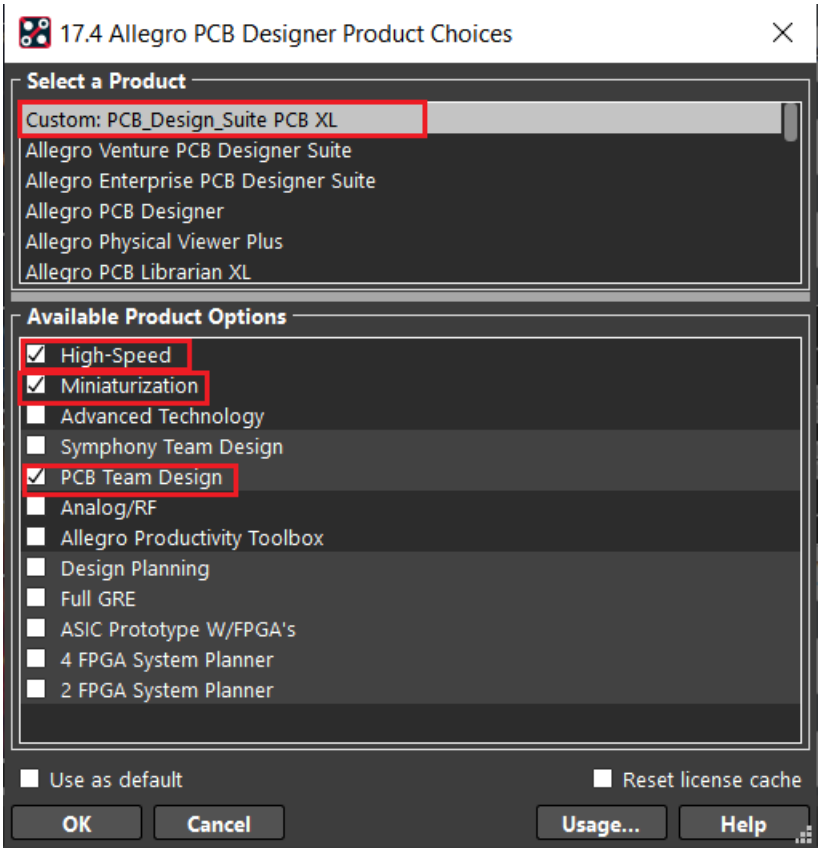
- <HOME>/`pcbenv`
- <ALLEGRO_SITE> (`<installation_hierarchy>/share/local/pcb`)

Example

Following sample file `license_packages_allegro.txt` creates a user-defined package *PCB_Design_Suite* for Allegro PCB Editor.

```
package PCB_Design_Suite PCB XL
command_line pcb_xl
license Allegro_performance
option Allegro_PCB_HighSpeed_Option
option Allegro_PCB_Mini_Option
option Allegro_PCB_Partitioning
```

Save this file to the `pcbenv` directory and launch PCB Editor. The Allegro Product Choices dialog picks up the new product set with associated product options and displays at the top of the products list.



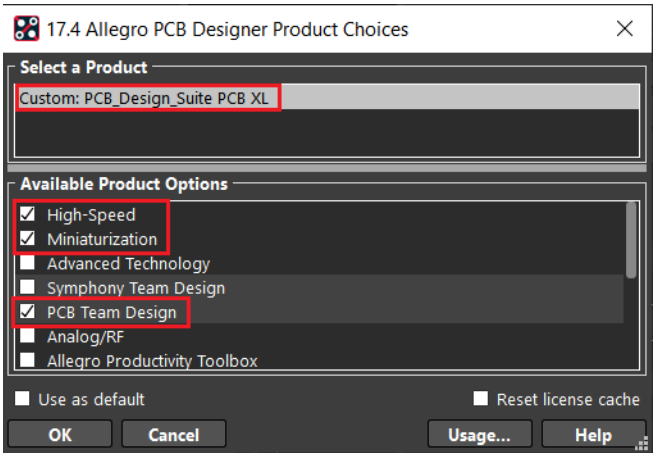
File Syntax

The `license_packages_<exe>.txt` file requires following keywords to create a package definition:

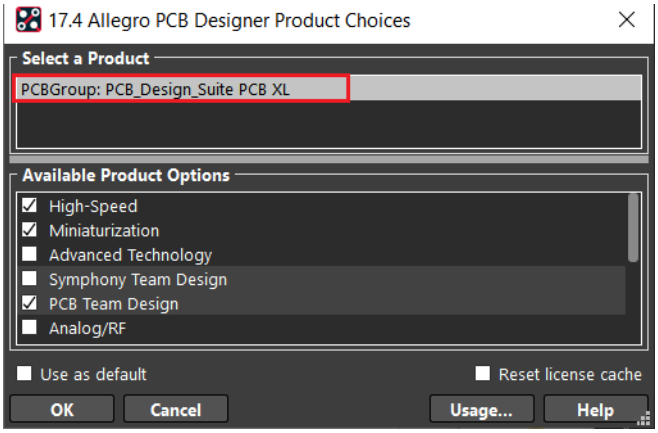
```
#  [filter nocadence]
#  [custom <name> ]
#  package <name of package so show in Change Editor dialog>
```

```
#   license <base product>
#   [command_line <name>]
#   version  <software version>
#   option <license1>
#   option <license2>
#   [version <sofware_version>]
#   [allegro_license_group <allegro_license_group>]
```

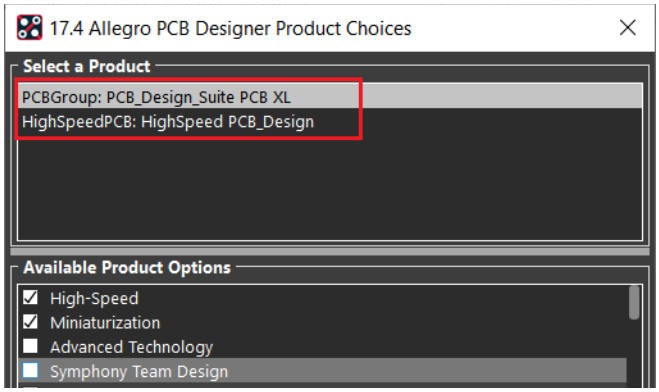
Keyword	Value	Status	Description
`filter`	`nocadence`	Optional	Inhibits the display of default Cadence products.



`custom`	`<name>`	Optional	Replaces the default prefix *Custom* with a string for the package name.



Note: Define this keyword at the top of package definition.

`package`	`<name of package>`	Required	Name of the package displays in the *Change Editor* dialog. You may define multiple packages in the file.
			
`license`	`<name of the base product license>`	Required	Name of the license for the base product. The license name for the base product can be obtained by clicking on the Help button in the *Change Editor* (`toolswap`) dialog.
`command_line`	`<name>`	Optional	Name to invoke the user-defined package from command line. For example, to launch the package defined in the sample file run following command: `allegro -product pcb_xl`
`version`	`<software version>`	Optional	Displays version of the user-defined package.
`option`	`<license1>`	Optional	Name of the product options for a package. The product options can be obtained by clicking on the Help button in the *Change Editor* (`toolswap`) dialog.
`allegro_license_group`	`<allegro_license_group>`	Optional	Displays the package if the value of the environment variable *`allegro_license_group`* matches the value given by this option.

You can refer to Cadence provided sample file (`license_packages_template.txt`). This file is located at `<installation_directory>/share/local/pcb` directory.

How do I fix space-related issues for MainWin on Linux?

Sometimes layout editors do not launch on Linux and throw errors. This problem occurs when the layout editor was terminated abnormally multiple times.

Depending on the Linux version, you may get the following errors:

```
"No room for process"
"out of shared memory"
"No semaphore
"No space left of device"
“MainWin can not run due to lack of system resources (Hint:) To check the status of system resurces use the ipcs command. Free up resources with the ipcrm command.”
```

To fix this error, perform the following steps:

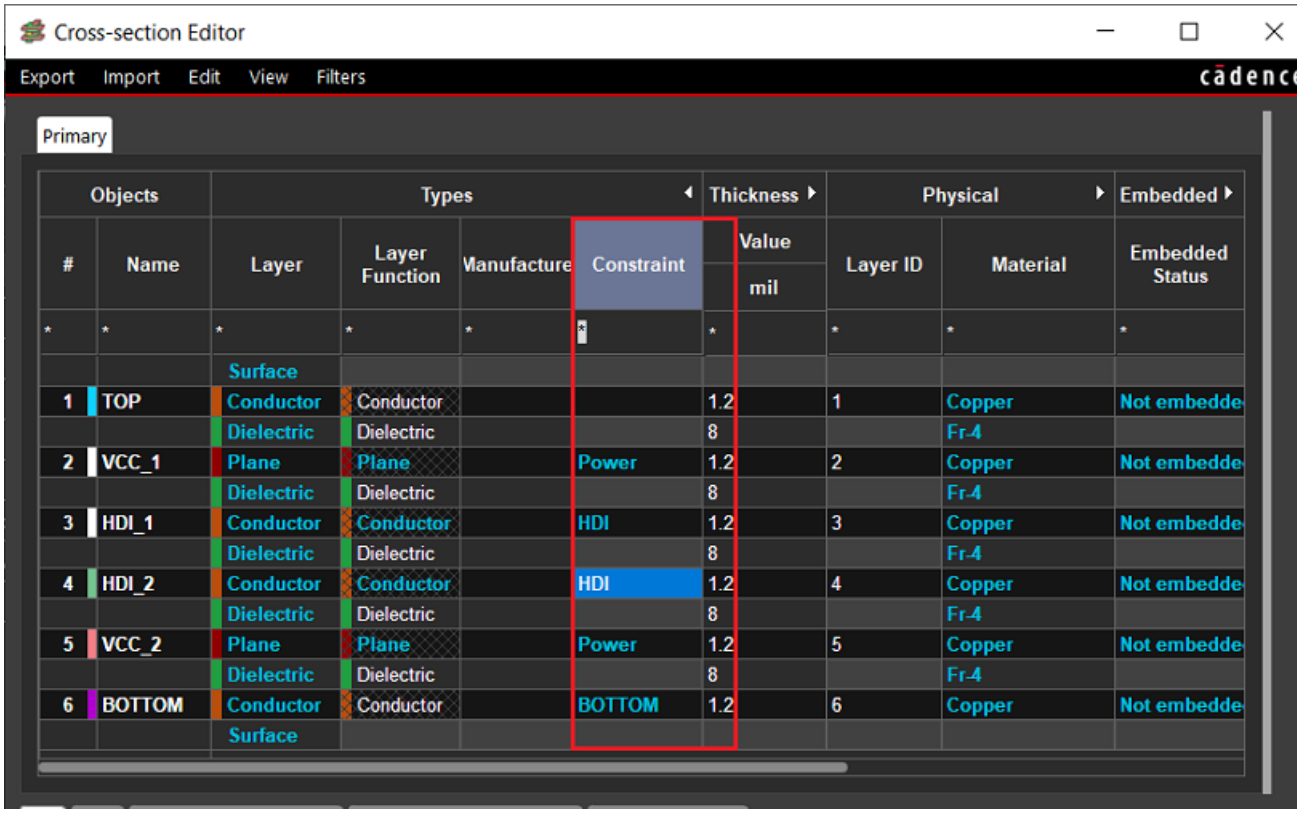
1. Ensure that no program is running.
2. Navigate to `installation_hierarchy>/tools/bin` directory.
3. Run the `fix_noprocess` shell script.

Can I place two mechanical symbols in a layout design?

Yes, you can place two instances of a mechanical symbol in a layout (PCB Editor, SiP and APD). But only one symbol can contain a route keepin or place keepin.

How can I export generic cross-section information in release 17.4-2019?

In release 17.4-2019, use the *Cross-Section Editor* dialog to configure generic cross-section layers. To define a layer as generic, choose a type in *Constraint*. This creates a layer type. For example, *Plane/Power* or *Conductor/HDI* in the following image.



In Constraint Manager, layers are grouped together by their layer type (*LTyp*). For example, *VCC_1* and *VCC_2* are displayed as layers of type *Plane/Power*.

Objects			Referenced Physical CSet	Line Width		Neck
Type	S	Name		Min	Max	Min Width
				mil	mil	mil
*	*	*	*	*	*	*
Dsn		▼ cds_routed	DEFAULT	5.00	0.00	5.00
PCS		▼ DEFAULT		5.00	0.00	5.00
LTyp		▼ Conductor		5.00	0.00	5.00
Lyr	1	TOP		5.00	0.00	5.00
LTyp		▼ Plane/Power		5.00	0.00	5.00
Lyr	2	VCC_1		5.00	0.00	5.00
Lyr	5	VCC_2		5.00	0.00	5.00
LTyp		▼ Conductor/HDI		5.00	0.00	5.00
Lyr	3	HDI_1		5.00	0.00	5.00
Lyr	4	HDI_2		5.00	0.00	5.00
LTyp		▼ Conductor/BOTTOM		5.00	0.00	5.00
Lyr	6	BOTTOM		5.00	0.00	5.00

When you export generic cross-section information from Constraint Manager, constraint information is saved for the different layer types. When you import technology file(`.tcfx`) or constraints file(`.dcfx`) with generic cross-section information, the constraint information updates layer types in the destination design.

How can I restore information messages disabled in PCB Editor?

Information messages are often provided with *Do not show this message again* checkbox. Enabling this checkbox stops showing them.

To view them again in PCB Editor, delete the file `allegro_remember.txt` in `pcbenv` directory.

Can I run a script when starting Allegro Free Viewer?

Opening Allegro Free Viewer from the command line lets you specify the design along with the script, which will run as soon as viewer is launched.

Use the following command line options to run a script when free viewer starts:

```
allegro_free_viewer -b <design> -s <script>
```

Can I dimension air gap between two pad edges of a symbol?

Yes, using dimension environment you can dimension air gap between pads. The following steps help you in setting up the dimension between pads:

1. In Symbol Editor, choose *Dimension – Dimension Environment*.

   All the dimensioning commands are available on right-click menu.

2. Right-click and choose *Linear dimension*.
3. In *Find* filter, select *Pins*.
4. Select the first pad and right-click to choose *Snap pick to – Pad Edge.*

Note: You can also choose other two snapping options *Pad Edge Vertex* and *Pad Edge Midpoint*.

5. Move the cursor towards second pad and right-click to choose *Snap pick to – Pad Edge*.

   The dimension value is attached to the cursor.

6. Click a location to place the dimension value.

Can I show the dollar character in layout editor similar to Windows?

Allegro layout editors use vectorized fonts for drawing text on the canvas. The vector definitions of all the fonts are stored in the `ansifont.dat` and `ansifont0.dat` files located at `<installation_directory>/share/pcb/text`.

You can customize the vector definition for any printable character in the `ansifont.dat` file. For example, add a diagonal line or a dot in the middle to change the default display of a vector font. Editing the vector definitions only affects artwork outputs not the default vector definitions of the layout editor.

Allegro layout editors show the dollar character with two vertical lines, but Windows shows it with only one vertical line. To edit the dollar character definition in `ansifont.dat` file, modify the file as shown in the following image.

```
18                /*** $ ***/
1 0 3276              /* Move to 0 3276 */
3 0 0            /* Draw vertically to 0 0 */
4 5461 -5461                /* Draw to 5461 -5461 */
2 27306 -5461               /* Draw horizontally to 27306 -5461 */
4 32767 0             /* Draw to 32767 0 */
4 32767 5461                /* Draw to 32767 5461 */
4 27306 10922               /* Draw to 27306 10922 */
4 5461 10922                /* Draw to 5461 10922 */
4 0 16383             /* Draw to 0 16383 */
4 0 21844             /* Draw to 0 21844 */
4 5461 27306                /* Draw to 5461 27306 */
2 27306 27306               /* Draw horizontally to 27306 27306 */
4 32767 21844               /* Draw to 32767 21844 */
3 32767 18568               /* Draw vertically to 32767 18568 */
1 21845 32767               /* Move to 21845 32767 */
3 21845 -10922              /* Draw vertically to 21845 -10922 */
1 10922 -10922              /* Move to 10922 -10922 */
4 10922 32767               /* Draw to 10922 32767 */
```

Figure 1-1 Original definition in anifont.dat

```
16                /*** $ ***/
1 0 3276              /* Move to 0 3276 */
3 0 0            /* Draw vertically to 0 0 */
4 5461 -5461                /* Draw to 5461 -5461 */
2 27306 -5461               /* Draw horizontally to 27306 -5461 */
4 32767 0             /* Draw to 32767 0 */
4 32767 5461                /* Draw to 32767 5461 */
4 27306 10922               /* Draw to 27306 10922 */
4 5461 10922                /* Draw to 5461 10922 */
4 0 16383             /* Draw to 0 16383 */
4 0 21844             /* Draw to 0 21844 */
4 5461 27306                /* Draw to 5461 27306 */
2 27306 27306               /* Draw horizontally to 27306 27306 */
4 32767 21844               /* Draw to 32767 21844 */
3 32767 18568               /* Draw vertically to 32767 18568 */
1 16384 32767               /* Move to 16384 32767 */
3 16384 -10922              /* Draw vertically to 16384 -10922 */
```

Figure 1-1 Modified definition in ansifont.dat

Can I store ansifont.dat and ansifont0.dat files in a CDS_SITE location?

Yes. The location of the `ansifont.dat` and `ansifont0.dat` files is controlled by the value of the VECTORFONTPATH variable. This variable is set in the global `env` file located at `<installation_directory>/share/pcb/text`.

You can change the value of VECTORFONTPATH and points it to the site environment location. The following image displays the drawing font section of the global env file.

```
#-----------------------------------------------
# Drawing font
set VECTORFONTPATH = . $GLOBAL
set ANSIFONT = ansifont
set KANJIFONTPATH = . $GLOBAL/fonts/kanji
set KANJIFONT1 = kanjifont1
set KANJIFONT2 = kanjifont2
```

How do I reset all constraints in Constraint Manager?

To reset all constraints in a design import the default constraint values from a new design by performing the following steps:

1. Create a new design in layout editor.
2. Open Constraint Manager and choose *File – Export – Constraints* to generate a constraint (`.dcfx`) file with default values.
3. In the *Export Constraints* form, set the *Physical and spacing constraints* and the *Export cross-section – Generic* checkboxes.

   This step is required to reset physical and spacing constraints.
4. Specify a constraint file name and click *Save*.
5. Open the target design and start Constraint Manager.
6. Choose *File – Import – Constraints* and specify the constraint file created in step 4.
7. In the *Import Mode* section, ensure *Overwrite (Update all information)* checkbox is enabled.
8. Click *Open* in the *Import Constraints* form.

In the target design, all the constraint values will reset to default.You can verify the changes using the *Constraint Differences Report* that opens once the import process is completed.

How do I place a Sigrity-generated via structure in layout editors?

The origin of a via structure may lie within a blank space between two vias if generated in Sigrity tools. But layout editors expect an origin, which can be the center of pins, vias, fingers, or end of clines, to snap the via structures.

Sigrity-generated via structures when exported to layout editors can be placed in the design in the following two ways:

- Enabling *Free place via structures* option in the `add via structure` command
  - **a.** Choose *Route – Via Structure – Add*.
  - **b.** In the *Add Via Structure* form, ensure *Free place via structures* checkbox is selected.
  - **c.** Click to place via structure anywhere in the design.
- Setting up via structures list in Constraint Manager and using them with the `add connect` command
  - **a.** Start Constraint Manager and select the *Electrical* domain.
  - **b.** Select *Routing – Vias* worksheet under the *Electrical Constraint Set* folder.
  - **c.** Choose *Objects – Create – Electrical CSet* and specify a name to create an ECSet. For example, *ECset_via_struct*.
  - **d.** Select the *Via Structures* column for *ECset_via_struct*.
  - **e.** In the *Edit Via Structure List* form, select via structures to create a list and close.
  - **f.** Select *Routing – Vias* worksheet under the *Nets* folder.
  - **g.** Select the net, which may use via structure when routed interactively.
  - **h.** In the *Referenced Electrical CSet* drop-down list, choose *ECset_via_struct* to assign CSet to the net.
  - **i.** Repeat the above step for nets, which may use via structures.
  - **j.** In layout editor, choose *Route – Add Connect* command.

The *Via* drop-down list shows all via structures for a net that has *ECset_via_struct* assigned.

k. Select a via structure and place it while routing.

How are user-defined mask layers different from pastemask, soldermask, and coverlay mask layers?

User-defined mask layers, created using Padstack Editor and applied to symbols, use different class/subclass model than pastemask, soldermask, and coverlay mask layers to properly handle placement of embedded components or placement of components in a rigid-flex zone.

Pin class is always used to add user-defined mask layers. While the subclass name is the same as the user mask subclass name, for example, user_mask. Irrespective of the layer where component is placed (TOP, BOTTOM, embedded, or top/bottom of a rigid-flex zone), the user-defined mask is always placed on the Pin class and user_mask subclass. All such components will have user_mask pad on the same subclass of Pin class.

In the case of pastemask, soldermask, and coverlay mask layers, the actual subclass assigned to a particular pad depends on the layer where the component is placed.

- If the component is placed on TOP layer: The soldermask_top or pastemask_top subclasses are automatically assigned to the pad.
- If the component is placed on BOTTOM layer: The soldermask_bottom or pastemask_bottom subclasses are automatically assigned to that pad.
- If the component is embedded between layers: Specific subclasses are created for each pad with name soldermask_<layer_name> or pastemask_<layer_name>. The <layer_name> is the name of the embedded layer on which the component is placed.
- If the component is place in a rigid-flex area of the design: The subclass used for coverlay pad depends on the definition of the zone, layer stackup and the names of the coverlay layers. If the component is placed on top or bottom of a zone and these layers are not TOP or BOTTOM layers and if the zone has a coverlay mask layer defined on the top of the stackup for top-mounted components or on the bottom of the stackup for bottom-mounted components, the coverlay pad use coverlay mask layer on top or bottom of the zone, respectively. The coverlay pad is suppressed if no coverlay mask is specified for the zone.

How can I remap read-only key modifiers for layout editors?

For consistent experience, some of the modifier keys in layout editors bind to default actions. These key bindings or mappings are read-only and follow industry standards. For example, Ctrl-S, Ctrl-C, Ctrl-P, and Ctrl-X are read-only and perform actions such as save, copy, paste, and cut respectively.

You can reconfigure the key assignment using a simple SKILL code. This code remaps specified key bindings on application startup during the initialization process. The following is a piece of sample SKILL code that unlocks the ~S key binding and assigns the slide action to it.

```
procedure( UnprotectAlias(t_unprotect)
       axlProtectAlias( "~S" nil)
       axlSetAlias( "~S" "slide")
   )
   axlTriggerSet('open  'UnprotectAlias)
```

In the above example, you can change `axlSetAlias` to any binding. Similarly, use the same trigger to update or set any other bindings. To run the example during layout editor startup, save the code in the `allegro.ilinit` file.

Why am I seeing the “0 width line found” error during Artwork generation process?

The artwork generation process displays a warning with text “0 width line found” if unfilled shape outlines, lines, or texts are found in the design.

You can resolve this message by removing the unfilled shapes. However, you might also want to avoid this message instead of resolving it, for example, you will see this message in context of lines if you included Design Outline in the Artwork.

To avoid this warning, in the Artwork Control Form, set the value of *Undefined line width* to a value greater than zero. Ensure that undefined line width is not set to zero for each artwork film record if you include the design outline shape in the artwork files.

Why does metal usage report show less percentage of metal for an embedded layer?

The metal percentage calculated by the metal usage report can be less because of incorrect embedded flag settings for a layer in Cross-section Editor.

If a layer is flagged as embedded, regardless of its status, the cavity outlines on that layer are considered as a gap in the layer. As a result, when metal is deposited, the cavity area is considered empty. Hence, drawing metal inside the cavity does not affect the metal usage calculation because there will be no metal in production.

To get the correct value of metal usage, do the following:

1. Choose *Setup – Cross-section* to open Cross-section Editor.
2. In the *Embedded* column, change the *Embedded Status* from *Protruding allowed* to *Not embedded* for the layer.
3. Click *OK* to close Cross-section Editor.

How do I pick a point on the canvas without snapping to the grid?

To pick a non-grid location when performing or automating design tasks, use either of the following two ways:

- From pop-up: Choose *Snap pick to – Off-grid Location*
- From the Command window prompt: Set up the grid for the layers you want to use to a lower granularity before using the `pick` command.

How do I generate artwork output files without extension?

To generate artwork files without file extension, set the value of the *`ext_artwork`* variable to space by entering the space character within single quotes (' ').

A blank *`ext_artwork`* causes the default file extension `(.art)` to be used.

Why does SHAPE_ISLAND_OVERSIZE DRC not report unrouted connections?

The *SHAPE_ISLAND_OVERSIZE* DRC detects orphaned negative shape islands. However, it does not check for plane island disconnects caused by voids generated during the manufacturing output and does not report them as unrouted connections.

To identify orphaned shape islands as unrouted connections, use positive dynamic planes. Positive planes break a shape into separate islands and report the broken shape regions as unrouted connections.

How can I check the height restriction for components?

Component height limitations can be checked using the PACKAGE_HEIGHT_MIN property. To the region of the design where you want to run the check, create a package keep out shape and assign PACKAGE_HEIGHT_MIN property to it. DRCs are generated for the components that exceed the value of the property.

2

Frequently Asked Questions in Padstack Editor

This document lists answers to the frequently asked questions about Padstack Editor.This document will be periodically updated to resolve the issues our customers face while working with Padstack Editor.

To view the answer to any question, click that question in the list below.

How do I save a zero-size pad with pad geometry in Padstack Editor?

How do I compare padstack data after uprev in release 17.4-2019?

Why modifying an antipad diameter in the padstack definition does not change the pin clearance?

How do I change the pick-up point for package symbols?

Why do shape pads on symbols not translate to artwork files?

How can I remove unused internal layers from a design?

How do I save a zero-size pad with pad geometry in Padstack Editor?

To save a zero-size pad with pad geometry, launch Padstack Editor and:

1. Change the regular pad geometry to Null.
2. Add thermal and antipad to the begin, end, and default internal layers.

How do I compare padstack data after uprev in release 17.4-2019?

To compare padstack data, use the `extracta` command. This command extracts and compares padstack data in releases 17.4-2019,17.2-2016 and 16.6.

```
extracta <design> <cmdfile> <outputfile>
```

Here `<cmdfile>` can be any baseview file (`*_bv`), which is a command file containing selected data fields for extracting one type of data from a design; for example, `symbol_bv.txt` to extract padstack data. Cadence provided baseview files are located at `<installation_hierarchy>\share\pcb\text\views`.

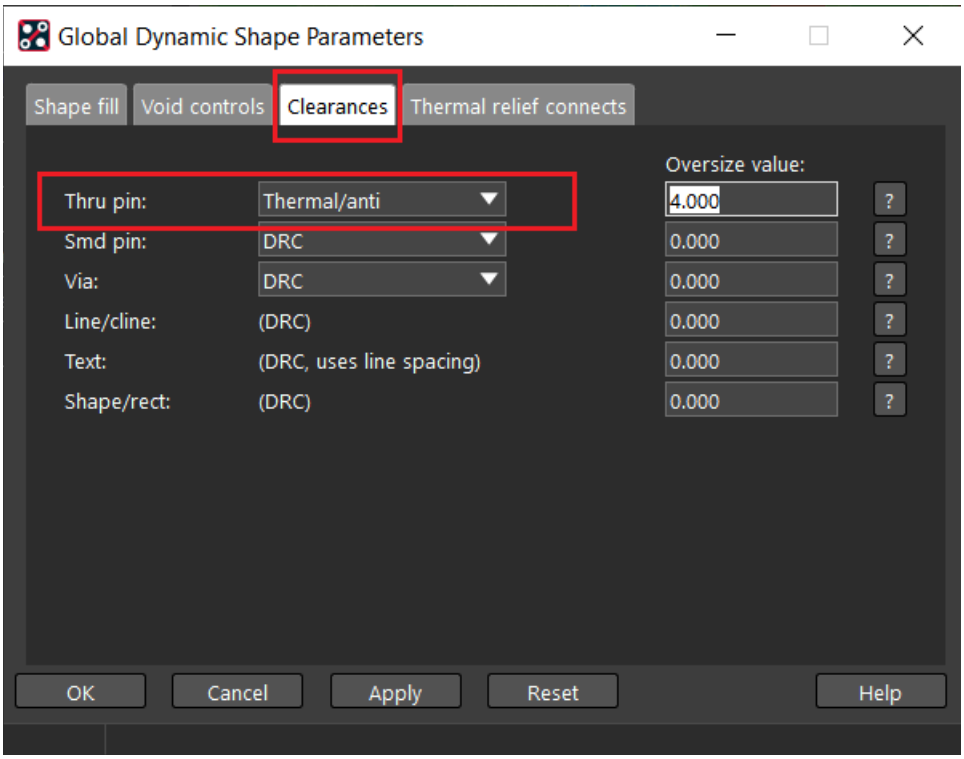
Example

At the command prompt, run following command using `extracta` versions of releases 17.4-2019, 17.2-2016 and release16.6:

```
extracta C:\library\smd_symbols\sym1.dra
<installation_hierarchy>\share\pcb\text\views\sym_bv.txt
C:\library\smd_symbols\extracta_result.txt
```

Why modifying an antipad diameter in the padstack definition does not change the pin clearance?

Clearance values are determined by the shape parameters. Controls to modify the clearance values are available in the *Clearance* tab of Global Dynamic Shape Parameters (`shape global param`). Setting them to *Thermal/Anti* calculates the clearance values from thermal relief or antipad as defined in the padstack definition of a pin or via.



Note: Oversize value does not increase the clearance on negative plane layers as the padstack definition is used exclusively.

How do I change the pick-up point for package symbols?

Pick-up point defines the optimum location for an automatic assembly machine to pick up the package. The pick-up point may lie anywhere on the package outline.

Layout editors consider the center of a component's package symbol body as the pick-up point. To calculate the center of the package symbol body, a two-step algorithm is used by layout editors:

1. If a line or a rectangle is defined on the package_geometry class and the body_center subclass, then the center of that line or rectangle is used as the center of the package symbol body.
2. If nothing is defined on the body_center subclass, then a bounding box is drawn around all the shapes that are defined on the package_geometry class and place_bound_top, place_bound_bottom, dfa_bound_top, and dfa_bound_bottom subclasses. In case of embedded components, their equivalent subclasses are used. The center of this bounding box is used as the center of the package symbol body.

To change pick-up point, add a line or rectangle on package_geometry class and body_center subclass in such a way that the center of the line or rectangle coincides with the required pick-up point.

Note: The origin of the text string on the body_center subclass is used as the origin point when moving the component with *Point* is set to *Body Center* in the Options panel.

Why do shape pads on symbols not translate to artwork files?

Padstacks with flash symbols are no longer supported. Therefore, padstacks that include shape geometries do not translate to artwork files.

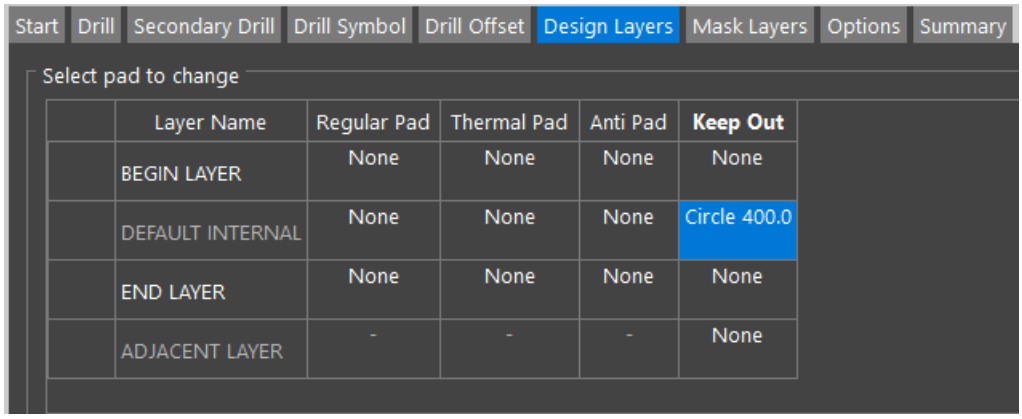
To include shape geometries in the Gerber files, remove the flash names from the padstack definitions before generating the artwork.

How can I remove unused internal layers from a design?

You cannot delete internal layers from a design if route keepout shapes are defined on these layers in symbol or padstack definitions. To delete these layers, remove the keepout shapes from the symbols and their padstacks.

Keepout shape geometry for internal layers can be set up in Padstack Editor without adding stackup layers. Perform the following step to assign keepouts to pads without adding stackup layers:

1. Start Padstack Editor and open the pad.
2. In the *Design Layers* tab, select the *Keep Out* cell for *DEFAULT INTERNAL*.
3. Choose the shape geometry and specify its dimension.



Why can I not change drill symbol information for oval and rectangular slots?

For oval and rectangular slots, the dimensions of the finished slot are automatically matched by the drill figure shape and size. Using drill figure geometry consistent with the finished slot size accurately represents the slot on fabrication drawings to convey design intent. The drill figure rotates with the pin or via by maintaining the correct orientation of the routed slots on the fabrication drawing if it fits the slot type.

How do I update the vias in the Physical CSets when a via name is changed?

Use the `rename padstack` command to automatically update the name of existing vias in a design. This command adds the new via name and deletes the old via name, preventing messages about not being able to find a library padstack when you run the `add connect` command, which requires you to purge the via list constraints.

3

Frequently Asked Questions in Constraint Manager

This document lists answers to the frequently asked questions about Allegro PCB Editor and its utilities.This document will be periodically updated to resolve the issues our customers face while working with Allegro PCB Editor.

To view the answer to any question, click that question in the list below.

How can I create an ECSet based upon routed interconnect of an XNet or differential pair?

How do I create a list of objects and their members in Constraint Manager?

How do I set shape properties by layer in a design?

How can I restore information messages disabled in Constraint Manager?

How do I reset all constraints in Constraint Manager?

Can I apply constraint region spacing for differential pair routing?

Why do estimated crosstalk analysis results not retained in Constraint Manager?

How can I generate DRC for non-plated via holes?

How do I fix corrupt values for the Min Line Spacing constraint?

Why does same net spacing DRC not shown if cline segment is shorter than maximum parallel length constraint?

Why are the Length Ignore constraint violations not reported if the Adjacent Void Spacing constraint is specified?

How do technology files generated by PCB Editor, Constraint Manager, and CM SKILL API differ?

How can I create an ECSet based upon routed interconnect of an XNet or differential pair?

1. Open the design in PCB Editor with *High-Speed* option.
2. Launch Constraint Manager and choose *Tools – Options*.
3. Enable *Include routed interconnect* in the *Options* dialog.
4. Select an XNet or differential pair net.
5. Right-click, and choose SigXplorer to extract the selected net.
6. In SigXplorer, choose *Edit – Transform – For Constraint Manager*.

   The interconnect elements are removed but net schedule and constraints are preserved.
7. Click *File – Update Constraint Manager.*

   The ECSet is updated in Constraint Manager.

How do I create a list of objects and their members in Constraint Manager?

Choose *Export – Worksheet File* in Constraint Manager to generate a file listing objects and their member nets. For example, creating a list of Net Groups and Match Groups, and their members.

Perform the following steps to generate a worksheet file with Net Group and Match Group information:

1. In the *Electrical* domain, open *Vias* worksheet from the Net-level folder.
2. Choose *Objects – Filter*.
3. Disable all the object types except *Match Group* and *Net Group* in the *Filter* dialog box.
4. Ensure *Always show group members* checkbox is enabled.
5. Click *OK* to save the filter settings.

   Rows showing Match Group and Net Group are only displayed in the active worksheet.
6. Choose *File – Export – Worksheet File*.
7. Enter the name and path of the file and in the *Export Worksheet File* dialog and click *Save*.

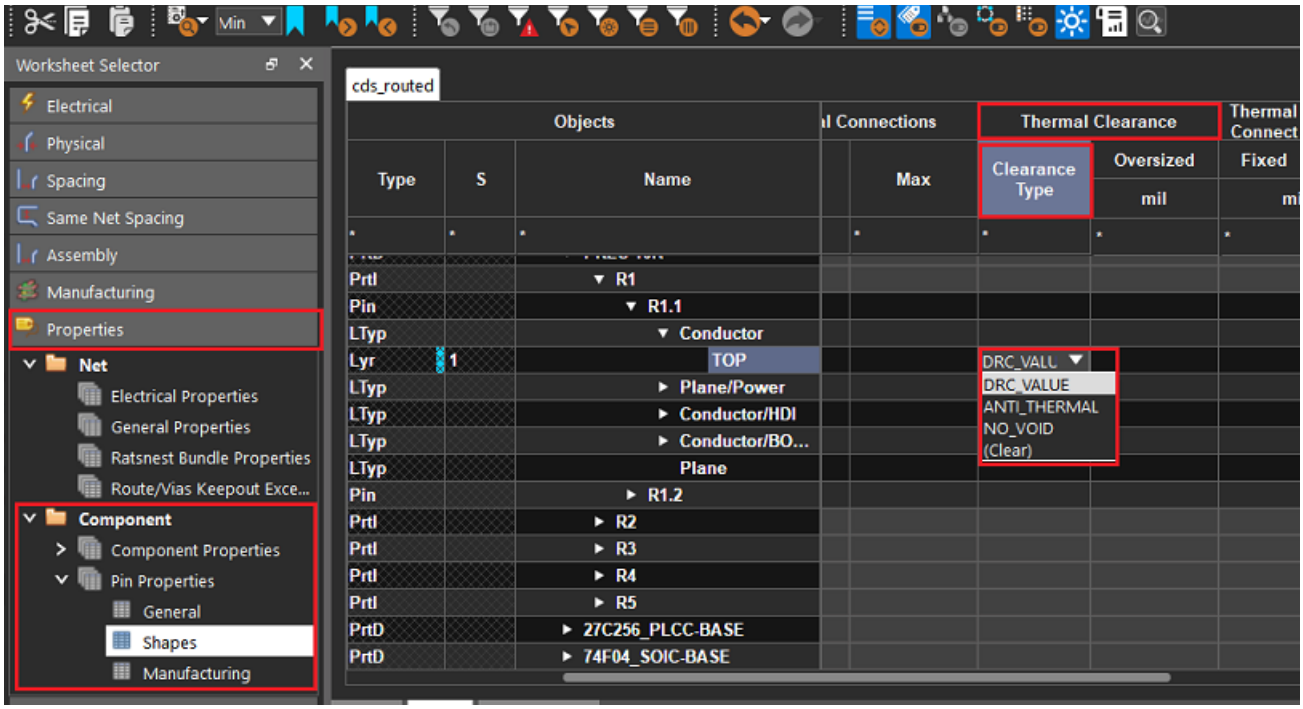
   An ASCII text file, listing all Net Groups and Match Groups and their members, is created at the specified path.

Note: You can create three types of files from the active worksheet: tab-delimited (`.txt`), comma-delimited (`.csv`), or space-delimited (`.prn`).

How do I set shape properties by layer in a design?

Use the *Component* and *Pin Properties* worksheets in the *Property* domain of Constraint Manager to set shape properties per layer. You can either set default values for a layer type, say CONDUCTOR, or specify different values for each layer, say one of TOP and another for BOTTOM.

For example, in the following illustration for the pin R1.1, different values are set for the thermal clearance property on the conductor layers.



How can I restore information messages disabled in Constraint Manager?

Information messages are often provided with *Do not show this message again* checkbox. Enabling this checkbox stops showing them.

To view them again in Constraint Manager, choose *View – View Options* command and enable *Restore default settings* checkbox in the *UI Options* dialog box.

How do I reset all constraints in Constraint Manager?

To reset all constraints in a design import the default constraint values from a new design by performing the following steps:

1. Create a new design in layout editor.
2. Open Constraint Manager and choose *File – Export – Constraints* to generate a constraint (`.dcfx`) file with default values.
3. In the *Export Constraints* form, set the *Physical and spacing constraints* and the *Export cross-section – Generic* checkboxes.

   This step is required to reset physical and spacing constraints.
4. Specify a constraint file name and click *Save*.
5. Open the target design and start Constraint Manager.
6. Choose *File – Import – Constraints* and specify the constraint file created in step 4.
7. In the *Import Mode* section, ensure *Overwrite (Update all information)* checkbox is enabled.
8. Click *Open* in the *Import Constraints* form.

In the target design, all the constraint values will reset to default.You can verify the changes using the *Constraint Differences Report* that opens once the import process is completed.

Can I apply constraint region spacing for differential pair routing?

Yes. By default for differential pair, inside a constraint region the minimum line spacing values from ECSet takes precedence over physical and spacing domain values.

To route differential pair with region-specific spacing, do the following in Constraint Manager:

1. In *Electrical* domain, open *Differential Pair* worksheet under the *Electrical Constraint Set* folder.
2. Select the ECSet that apply to differential pair nets and clear all the differential pair properties in the right pane.
3. In *Physical* domain, select *All layers* worksheet under *Region* folder.
4. Select the region or region class that contains differential pair.
5. Specify values for Min Line Spacing and neck gap in the *Differential Pair* column and close the Constraint Manager.

Why do estimated crosstalk analysis results not retained in Constraint Manager?

Constraint Manager, by default, populates the analysis results every time it is opened. Distinct colors (green, red, and yellow) reflects the state of DRC, if the DRCs are up-to-date and the online check is enabled in the Analysis Modes dialog. Actual and margin numerical values can be computed by explicitly performing the Analyze command.

Crosstalk analysis results defy this behavior and do not retained in Constraint Manager because these checks depend on crosstalk tables which may have changed since the Constraint Manager was last opened.

How can I generate DRC for non-plated via holes?

By default, non-plated via holes are not considered while running DRCs. To manage DRCs between non-plated via holes and other objects you can set an environment variable *`cds_dfm_support_legacy_hole`*. Add this variable to the `env.txt` file in `PCBENV` directory. If set, this variable treats non-plated via holes as non-plated mechanical holes and generate DRCs.

How do I fix corrupt values for the Min Line Spacing constraint?

When specifying a value for the *Differential Pair Min Line Spacing* constraint for a layer. you may encounter the following message:

```
Min Line Spacing may not be larger than Primary or Neck Gap less (-) Tolerance.
```

This message is displayed when an existing *Min Line Spacing* constraint value is invalid. The constraint value is considered invalid if it is greater than the difference of *Primary Gap* and *(-)Tolerance* or difference of *Neck Gap* and *(-)Tolerance*.

To reset the *Min Line Spacing* constraint value on a layer, perform the following steps:

1. Set a single valid value for the CSet.
2. Expand the CSet and set a single value for all *Conductor* or *Plane* layers.
3. Expand *Conductor* or *Plane* layers and set the values for the specific conductor or plane layers.

Why does same net spacing DRC not shown if cline segment is shorter than maximum parallel length constraint?

The same net spacing DRC is generated only when the clines exceed separation plus distance and then loop back to within the spacing.

parallel length is shorter aIf parallel length is larger, it displays the Same_net Spacing DRC error.

However when Parallel length is reduced or made shorter, the Same net Spacing DRC error does not appear on canvas.lthough Air Gap is same when length is larger. he Same_net Spacing DRC error should be displayed even when Parallel length is reduced as Air Gap is still the same.

Configurations such as the ones described are actively filtered by the system. Only when connect lines exceed separation plus distance and then loop back to within the spacing This falls into the filter for short segments and is not report. This

filter is used to eliminate short tuning segments from false drcs. distance are they considered to be true errors.

Why are the Length Ignore constraint violations not reported if the Adjacent Void Spacing constraint is specified?

The *Length Ignore* constraint of the return path is considered when the center line of a cline intersects the void, and the intersected length of the cline is greater than the value of the *Length Ignore* constraint `(MAX_RTP_IGNORE_LENGTH)`. The *Adjacent Void Spacing* constraint of the return path is considered when a cline is closer to a void than the value specified for the *Adjacent Void Spacing* constraint `(RTP_VOID_SPACING)`.

The value of the *Adjacent Void Spacing* constraint is always positive, hence generating a spacing violation when a cline intersects a void. As a result, all *Length Ignore* violations are reported as *Adjacent Void Spacing* DRCs. To get only *Length Ignore* violations, remove *Adjacent Void Spacing* spacing constraints in the Constraint Manager.

How do technology files generated by PCB Editor, Constraint Manager, and CM SKILL API differ?

Technology files generated from PCB Editor, Constraint Manager, and CM SKILL API have the same syntax. However, the file varies in terms of content. The <Contents> element of a technology (or Constraint) file, captured at the top of the file, differs in the following ways:

- Techfile generated from PCB Editor export command: CContains hard-coded content and includes almost all the data. This technology file does not include information about Funcs, which contains all user-defined SKILL codes associated with advanced constraints.
- Techfile generated from Constraint Manager export command: Contains user-defined content as specified in the export dialog box. This technology file includes information about Funcs and cross-section type, such as design-specific or generic.
- Techfile generated from CM SKILL API, cmxlExportFile(): Supports parameters to control the content. However, parameters are difficult to use because a BIT mask manages the content. The CM SKILL API, by default, generates all the content.