

Getting Started with Allegro® X PCB Editor

Product Version 23.1
September 2023

© 2023 Cadence Design Systems, Inc. All rights reserved.

Portions © Apache Software Foundation, Sun Microsystems, Free Software Foundation, Inc., Regents of the University of California, Massachusetts Institute of Technology, University of Florida . Used by permission. Printed in the United States of America.

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Allegro® Design Entry HDL contains technology licensed from, and copyrighted by: Apache Software Foundation, 1901 Munsey Drive Forest Hill, MD 21050, USA © 2000-2005, Apache Software Foundation. Sun Microsystems, 4150 Network Circle, Santa Clara, CA 95054 USA © 1994-2007, Sun Microsystems, Inc. Free Software Foundation, 59 Temple Place, Suite 330, Boston, MA 02111-1307 USA © 1989, 1991, Free Software Foundation, Inc. Regents of the University of California, Sun Microsystems, Inc., Scriptics Corporation, © 2001, Regents of the University of California. Daniel Stenberg, © 1996 - 2006, Daniel Stenberg. UMFPACK © 2005, Timothy A. Davis, University of Florida, (davis@cise.ulv.edu). Ken Martin, Will Schroeder, Bill Lorensen © 1993-2002, Ken Martin, Will Schroeder, Bill Lorensen. Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, Massachusetts, USA © 2003, the Board of Trustees of Massachusetts Institute of Technology. All rights reserved.

Trademarks: Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522.

Open SystemC, Open SystemC Initiative, OSCI, SystemC, and SystemC Initiative are trademarks or registered trademarks of Open SystemC Initiative, Inc. in the United States and other countries and are used with permission. All other trademarks are the property of their respective holders.

Restricted Permission: This publication is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this publication, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this publication subject to the following conditions:

1. The publication may be used only in accordance with a written agreement between Cadence and its customer.
2. The publication may not be modified in any way.
3. Any authorized copy of the publication or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
4. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

Disclaimer: Information in this publication is subject to change without notice and does not represent a commitment on the part of Cadence. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information. Cadence is committed to using respectful language in our code and communications. We are also active in the removal and/or replacement of inappropriate language from existing content. This product documentation may however contain material that is no longer considered appropriate but still reflects long-standing industry terminology. Such content will be addressed at a time when the related software can be updated without end-user impact.

Restricted Rights: Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor.

Contents

1

Preface

<u>About this Tutorial</u>	7
<u>Prerequisites</u>	8
<u>Tutorial Flow</u>	8
<u>Tutorial Design</u>	9
<u>Syntax Conventions</u>	11
<u>Related Information</u>	12

1

Getting Started

<u>Tutorial Database</u>	13
<u>Starting Allegro X PCB Editor</u>	13
<u>Setting Your Working Directory</u>	15
<u>The current directory is set to a location specified during the software installation. This directory name appears in the title bar of Allegro PCB Editor. All files that are created or saved from within Allegro PCB Editor are saved to the current directory by default.</u>	17
<u>Creating Board Outline</u>	20
<u>Viewing Cross-section</u>	21
<u>Summary</u>	22
<u>What's Next</u>	23
<u>Recommended Reading</u>	23

2

Importing Logic Information

<u>Importing Logic</u>	25
<u>Summary</u>	31
<u>What's Next</u>	31
<u>Recommended Reading</u>	32

3

<u>Placing Components</u>	33
<u>Setting Non-Etch Grid</u>	33
<u>Placing Components</u>	34
<u>Summary</u>	44
<u>What's Next</u>	45
<u>Recommended Reading</u>	45

4

<u>Routing the Design</u>	47
<u>Setting up Grids</u>	47
<u>Assigning Color to Power and Ground nets</u>	49
<u>Routing Design Using Automatic Router</u>	51
<u>Generating Reports</u>	53
<u>Summary</u>	55
<u>What's Next</u>	55
<u>Recommended Reading</u>	56

5

<u>Validating Design</u>	57
<u>Viewing Design in 3D Canvas</u>	57
<u>Generating Reports</u>	58
<u>Summary</u>	62
<u>Recommended Reading</u>	62

6

<u>Generating Manufacturing Output</u>	63
<u>Renaming Reference Designator</u>	63
<u>Generating Silkscreen</u>	65
<u>Setting visibility for silkscreen</u>	65
<u>Generating Silkscreen</u>	69
<u>Generating Manufacturing Files</u>	72
<u>Creating Artwork</u>	73

Getting Started with Allegro X PCB Editor

<u>Creating NC Drill</u>	74
<u>Creating IPC2581 Files</u>	78
<u>Summary</u>	80
<u>Recommended Reading</u>	81

Getting Started with Allegro X PCB Editor

Preface

PCB Editor is a layout design tool that uses a logic netlist created by a schematic-design tool (AllegroX System Capture, Allegro Design Entry HDL, or Capture CIS) as an input and generates layout files as an output for photoplotters and mechanical tools. The output files, such as Gerber files, drill files, and so on, are used to manufacture the PCBs.

Using PCB Editor you can design a simple as well as a complex PCB. Some of the key features of PCB Editor are:

- Intuitive and easy-to-use
- Strong editing and viewing capability
- Fully-integrated constraint management tool that allows you to define physical, spacing, and high-speed (electrical) manufacturing requirements. As Constraint Manager is also integrated to the Cadence schematic tools, these constraint values can be specified early in the design cycle, before the start of the schematic design, and can be managed
- Controlled auto-routing
- Supports design for manufacturing checks
- Available on both Windows and LINUX-based operating systems

About this Tutorial

The tutorial provides step-by-step introduction to the PCB design flow using a single-layer PCB with through-hole and SMD components in a sample design example. This tutorial does not cover schematic capture and uses the default settings in the PCB Editor for creating the tutorial design. The tutorial is based on Allegro X PCB Designer 23.1 (build September, 2023). Audience

The tutorial is designed for new users who are either beginners to the PCB design process, or have design experience with other layout design tools and are unfamiliar with Allegro X PCB Editor.

Prerequisites

To work successfully with the PCB Editor, you must have basic knowledge of printed circuit board (PCB) design.

Before starting with creating layout, you should download the schematic netlist files from the tutorial database. The tutorial begins with importing a netlist from the schematic. Further steps involve placement of components, routing and generation of output files and reports.

Tutorial Flow

This tutorial includes following sections:

- Getting Started: This section provides instructions on how to setup the PCB Editor environment for creating layout.
- Importing Logic: This section provide steps to transfer the logic design data into PCB Editor.
- Placing Components: This section describes the component placement process in PCB Editor.
- Routing the Design: This section gives you stepwise details for auto-routing the design.
- Validating Design: This section shows how to verify the design data by running different reports, DRC checks, and 3D view.
- Generating Output: This section explains how to get your design ready for generating output files for manufacturing.

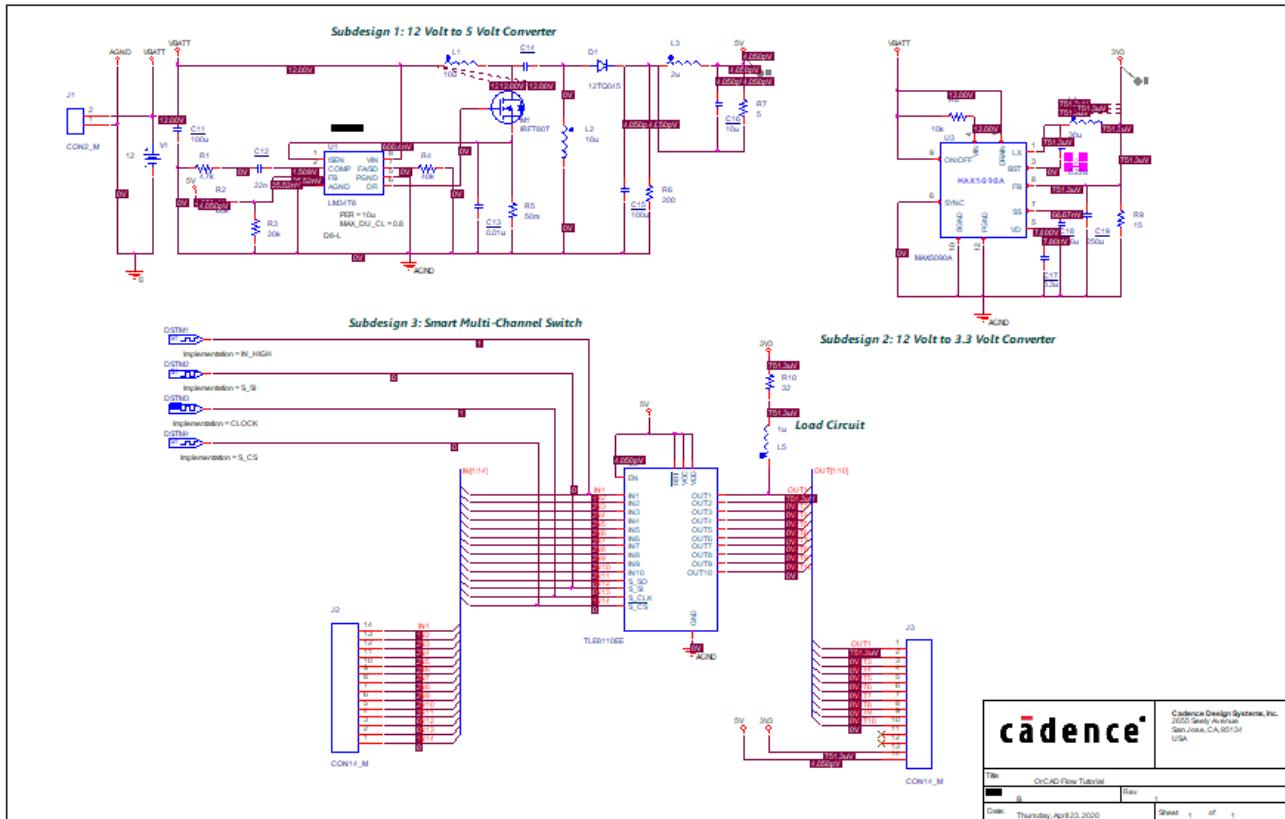
This tutorial is designed for Windows 10, but most of the things should be easy to extended for LINUX or UNIX.

Tutorial Design

This tutorial is an example of fan module circuit that uses transistors, voltage divider, discrete components, and connectors. A sample of schematic and layout designs are shown in the following figures.

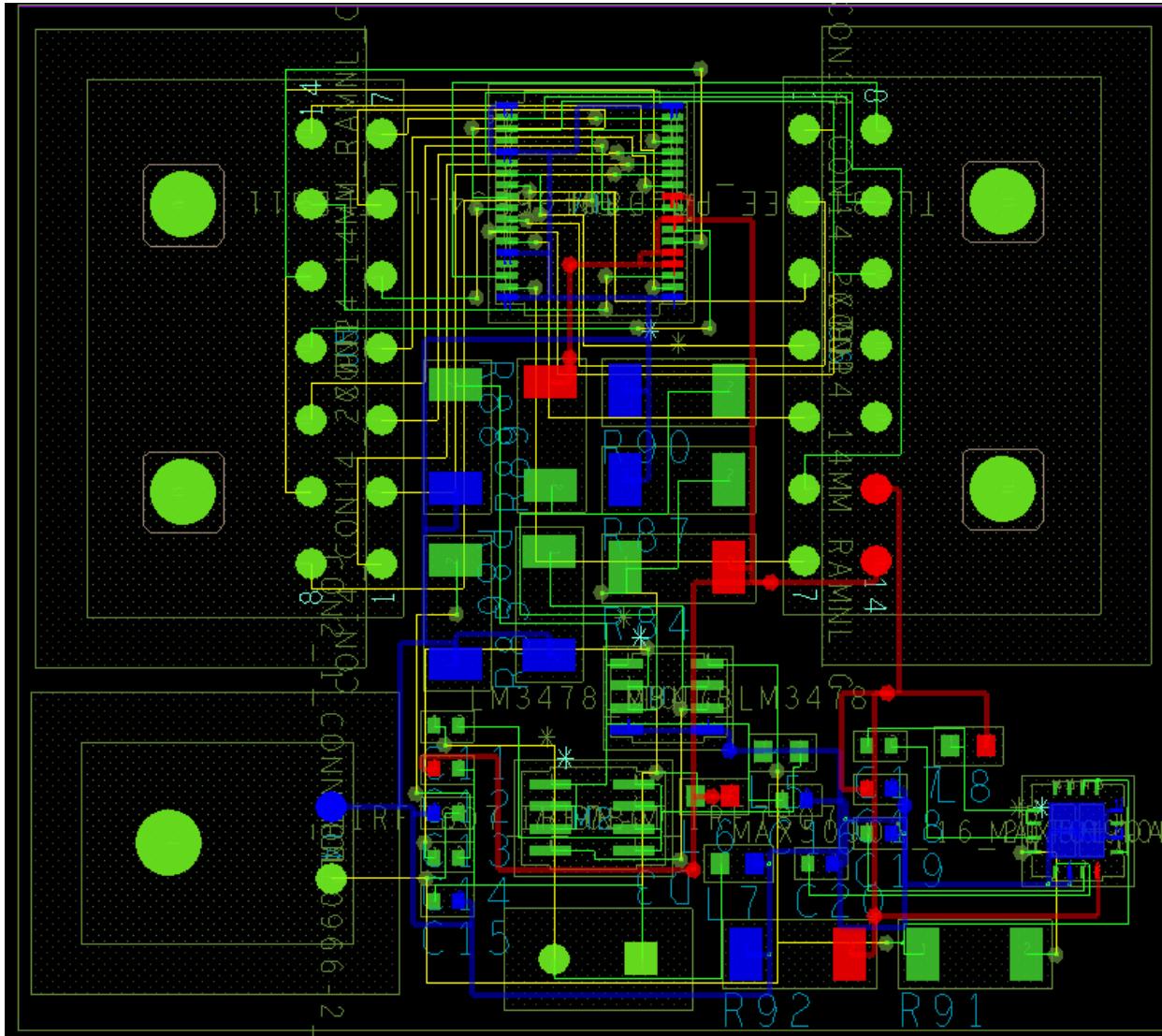
Getting Started with Allegro X PCB Editor

Preface



Getting Started with Allegro X PCB Editor

Preface



Syntax Conventions

This list describes the syntax conventions used in this tutorial.

literal	Key words that you must enter literally. These keywords represent commands (functions, routines) or option names.
Courier font	Indicates command line examples.
<i>UI</i>	Words in this font refer to menus, labels, fields, or tabs on the user interface.

variable Words in this font refer to arguments for which you must substitute a value.

Related Information

At the end of each lesson, you will find hyperlinks to related sections of the *Allegro X PCB Editor User Guide*, and the *Allegro X PCB and Package Physical Layout Command Reference*. You can also access these manuals from the Help menu.

For more information, see the [*Allegro User Guide: Getting Started with Physical Design*](#) and [*Allegro PCB and Package Physical Layout Command Reference*](#) in the documentation set.

Getting Started

This section explains how to invoke Allegro X PCB Editor, set the path for custom libraries using environment variables and set up PCB Editor environment for creating layout.

Tutorial Database

To run the tutorial, you need to copy the netlist files to your local machine. Before using the tutorial, ensure that you do the following:

1. Create a local directory `fan_module_proj`.

Use this location to save board files, log files, and reports when you work on your project.

2. Create a `packager_files` subdirectory in the `fan_module_proj` directory and copy all the files, from `<installation_directory>\doc\algrgo_tut\examples\packager_files` to the `fan_module_proj\packager_files` directory.

This directory contains netlist (output) files from OrCAD X Capture.

Starting Allegro X PCB Editor

You can start Allegro X PCB Editor in one of the following ways depending on whether you are working on Windows or LINUX.

Procedure

1. Open PCB Editor using one of the following methods:

- a. On Windows, click the Windows *Start* button (bottom left of your screen) and expand *Cadence PCB 2023* folder.
- b. Double-click the *PCB Editor 23.1* icon.

Or

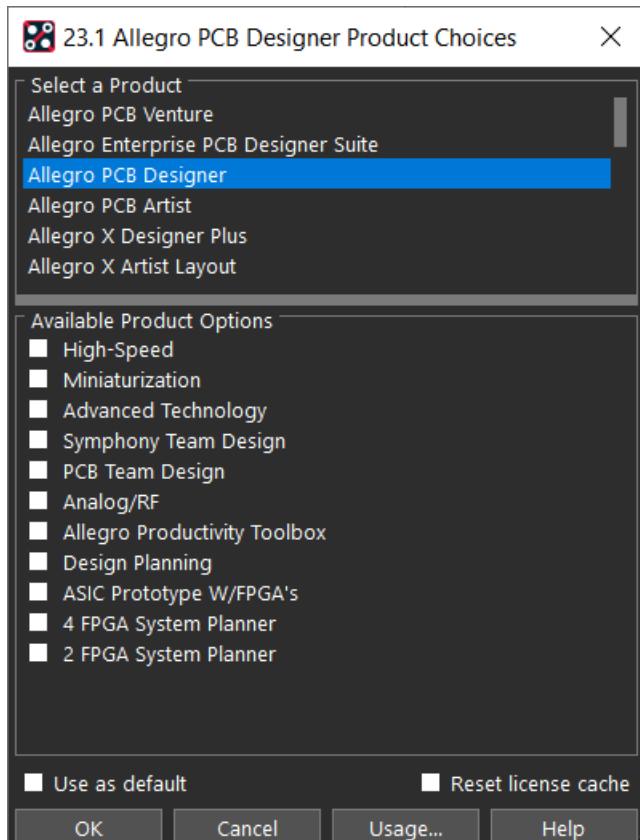
Getting Started with Allegro X PCB Editor

Getting Started

- a. On LINUX, at the shell prompt, type:

```
allegro &
```

The first time you launch Allegro X PCB Editor, the *Cadence 23.xx Allegro X Product Choices* dialog box appears listing all available licenses.



If you do not enable the *Use As Default* option, the *Cadence 23.xx Allegro X Product Choices* dialog box appears each time you use Allegro PCB Designer.

2. For this tutorial, select *Allegro PCB Designer*.

This sets Allegro PCB Designer as default license and is used for the lessons in this tutorial.

Getting Started with Allegro X PCB Editor

Getting Started

The first time you start Allegro X PCB Editor, a start page is displayed.



Setting Your Working Directory

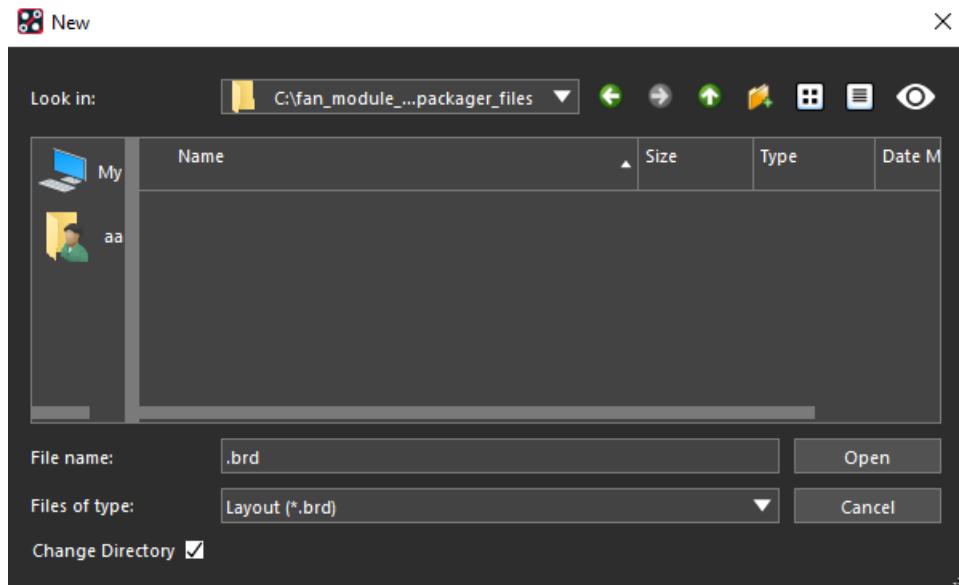
To set the directory location to the tutorial design, do the following:

1. Choose *File – New*.
A *New Drawing* window opens.
2. Click the *Browse* button.
A new file browser window is displayed.
3. Navigate to the `fan_module_proj` directory.

Getting Started with Allegro X PCB Editor

Getting Started

4. Verify that the *Change Directory* box is checked.

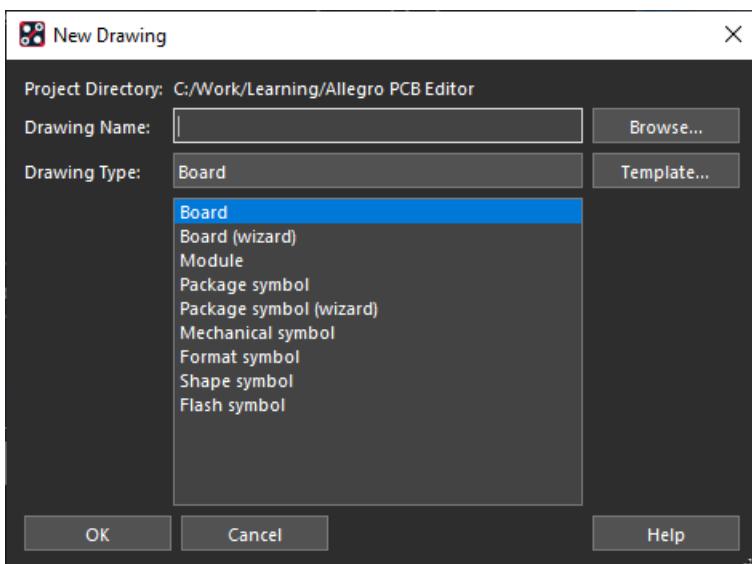


This option sets your working directory to `fan_module_proj`.

Note: The two buttons below the *Help* button are preview buttons. When pressed, the left button provides a text preview and the right button provides a graphics preview of the selected design.

5. Specify the *File name* as `tutorial.brd` and click *Open*.

6. Click *OK* in the New Drawing window.



A blank `tutorial.brd` opens in Allegro PCB Editor.

Getting Started with Allegro X PCB Editor

Getting Started

The current directory is set to a location specified during the software installation. This directory name appears in the title bar of Allegro PCB Editor. All files that are created or saved from within Allegro PCB Editor are saved to the current directory by default.

Adding Custom Libraries for Footprints and Padstacks

The Allegro X PCB Editor stores the system and configuration information in a text file `env.txt`. This file contains the information in the form of environment variables and their default values. You can add or modify the environment variables as per your preferences.

To set the path of footprints and padstacks libraries, set the `psmpath` and `padpath` variables in PCB Editor using the following steps:

1. Choose *Setup – User Preferences* or type `enved` in the command window.

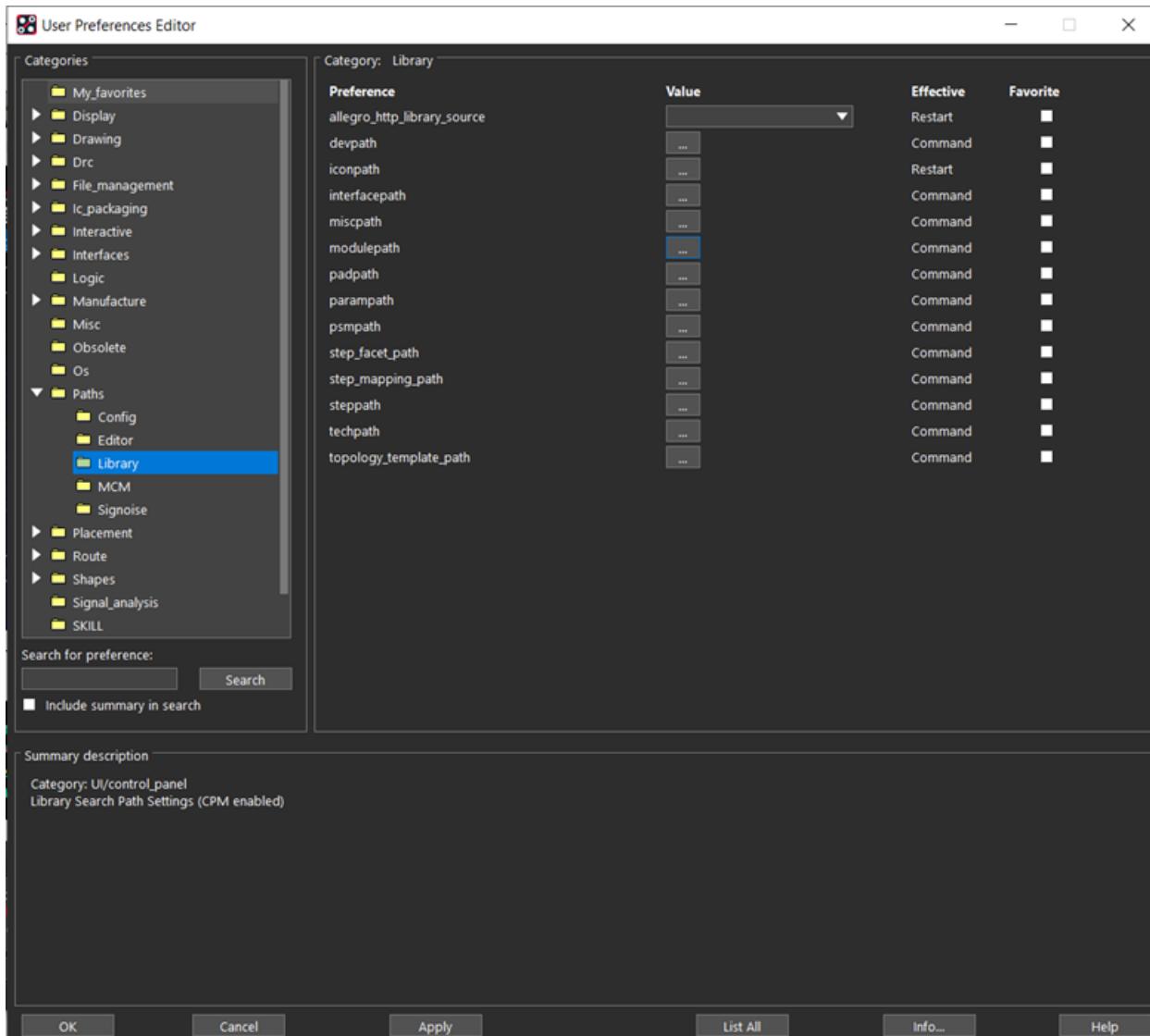
User Preferences Editor opens.

2. Expand the *Paths* folder in the *Categories* section.

Getting Started with Allegro X PCB Editor

Getting Started

3. Select *Library* folder.



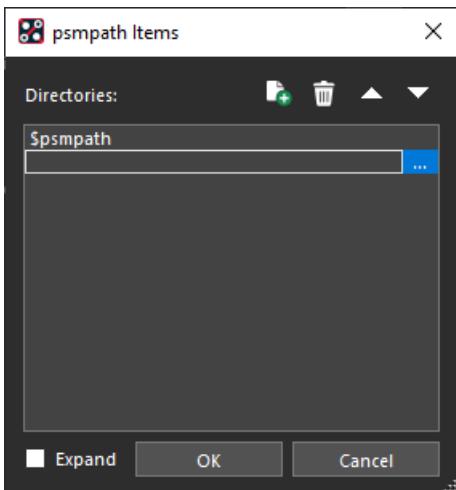
4. Click the *Value* button for *psmpath* variable that defines the path for package symbol (footprints).

The *psmpath Items* dialog box is displayed.

Getting Started with Allegro X PCB Editor

Getting Started

5. Click add directory icon.



An empty item gets added to the list.

6. Click the browse button of the new item.

The *Select Directory* dialog box opens.

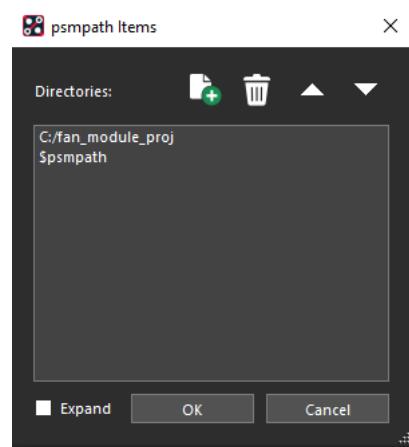
7. Navigate to your custom footprints directory.

8. Click *OK* to select this directory.

9. Click `$psmpath` and then *Move Down* arrow button, to set the path for local libraries before default libraries denoted by `$psmpath`.

Note: If there are common components in both libraries, the library that appears first in the list used first.

10. Click *OK* to close the *psmpath Items* dialog box.



Getting Started with Allegro X PCB Editor

Getting Started

11. Repeat the steps from [step 4](#) to 10 for *padpath* variable to add padstack library.
12. Click *OK* to close the *User Preferences Editor*.

Creating Board Outline

Board outline specifies the boundary within which components can be placed. It is necessary to create a board outline when transferring design data for ECAD-MCAD evaluation.

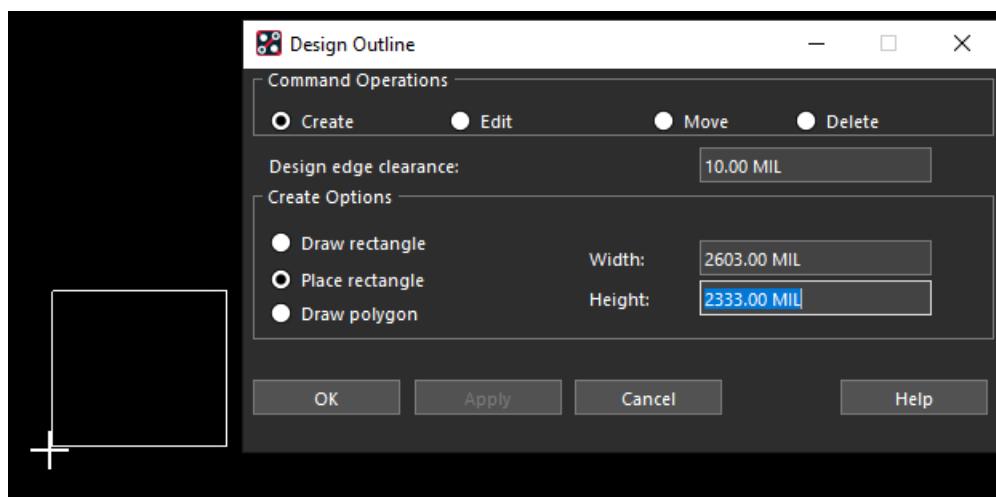
1. Choose *Setup – Outlines – Design Outline* or type `board outline` in the command window.

The *Active Class and Subclass* fields are by default set to *Board_Geometry* and *Design_Outline* in the Options tab.

2. In the *Design Outline* dialog box, select *Place rectangle* and set *Width* and *Height* values to 2603 and 2333 MIL, respectively.
3. Set *Design edge clearance* value to 10 MIL.

This value defines the space between the board outline and package and route keepin boundaries which is required to accommodate manufacturing tolerances, testing, and assembly.

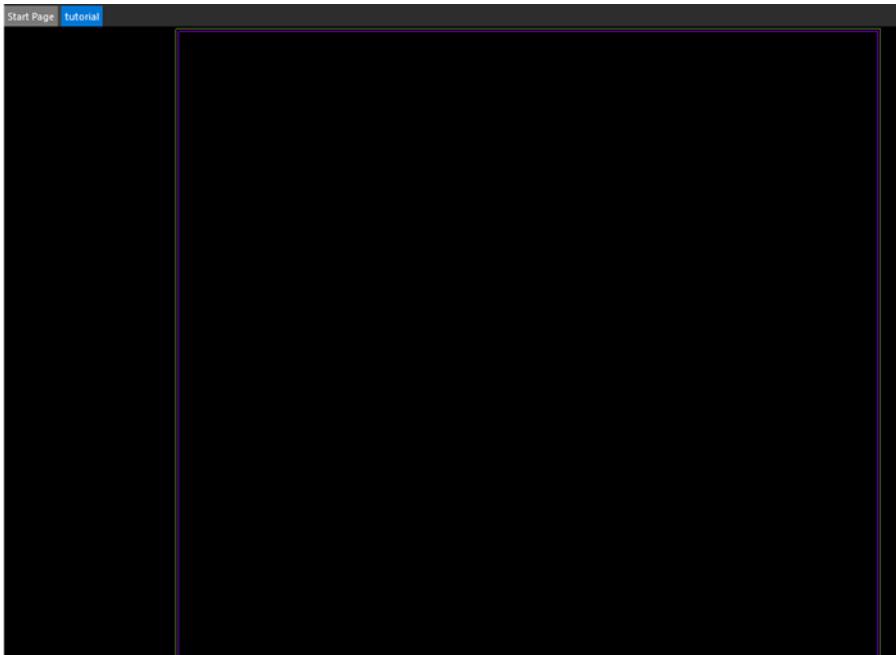
A rectangular design outline is attached to the cursor.



4. Click anywhere in the design canvas to place the outline.
5. Click *OK* to close the *Design Outline* dialog box.

A rectangular board outline is created with package and route keepin areas.

6. To view the entire board in the design canvas, choose *View – Zoom Fit* to center the board outline in the design window.



7. Choose *File – Save* to save the design.

A journal file `allegro.jrl` is created in your `$HOME` directory. This file records the sequence of events that takes place in each session of PCB Editor, for example, menu picks, keyboard activity, and so on.

Viewing Cross-section

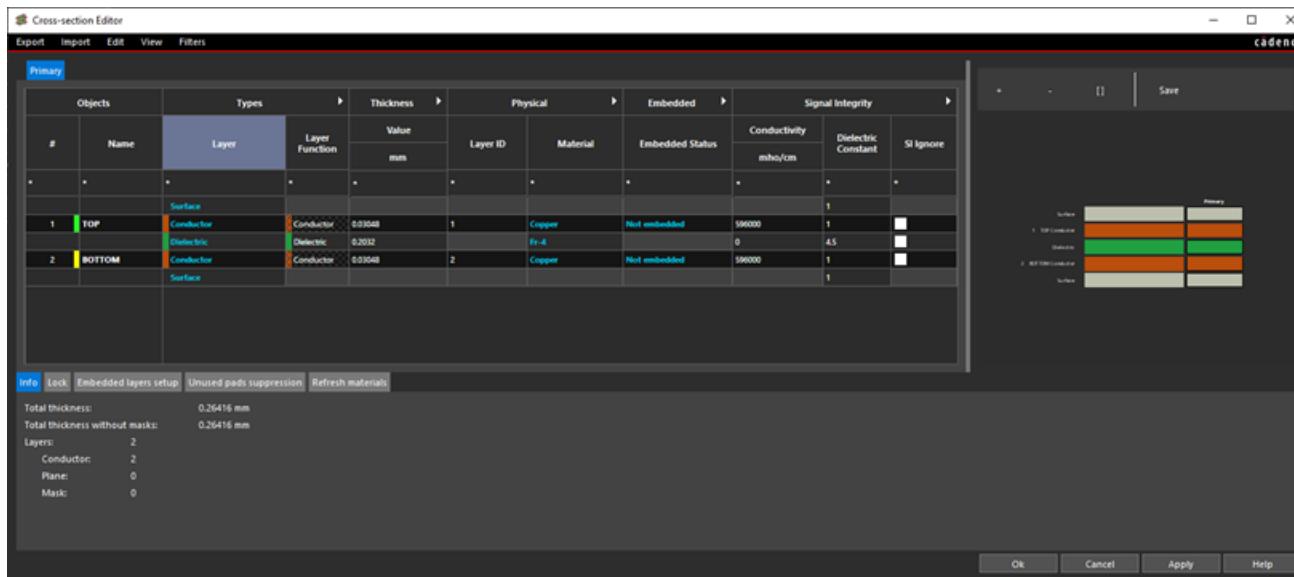
To define the layer stackup or cross-section of the design, use Cross-section Editor. The tutorial design uses a single-layer PCB which has copper on the bottom and components on the top and uses default values for all parameters.

1. Choose *Setup – Cross-section* or type `xsection` in the command window, to view the layer setup.

Getting Started with Allegro X PCB Editor

Getting Started

The Cross-section Editor window is displayed.



The two conductor layers **TOP** and **BOTTOM** are used to place the components. Using this dialog box you can specify different properties such as conductor or dielectric material type, its thickness and so on.

2. Click *OK* to close the Cross-section Editor window.
3. Choose *File – Save* to save the file `tutorial.brd` in the project directory.

Summary

You now know how to set a working directory, start the PCB Editor, and open a board design. You also learned how to set environment variables, create design outline and specify the layer stackup of a design. You have learned the following:

- **New menu commands:** *File – New, Setup – User Preferences, Setup – Outlines – Design Outline, View – Zoom Fit, Setup – Cross-section, File – Save*
- **New console commands:** `allegro, new, enved, board outline, zoom fit, xsection, save`
- **New window and dialog box:** Cadence 17.xx Allegro X Product Choices, User Preferences Editor, New Drawing dialog box, Design Outline, and Cross-section Editor.
- **New files created:** `allegro.jrl, tutorial.brd`

What's Next

In the next section, you will import the netlist created by the schematic design tool in the Allegro X PCB Editor.

Recommended Reading

For more information, see the [Allegro User Guide: Getting Started with Physical Design](#) and [Allegro PCB and Package Physical Layout Command Reference](#) in the documentation set.

Getting Started with Allegro X PCB Editor

Getting Started

Importing Logic Information

The design information is transferred from schematic design to the PCB Editor in form of netlist that contains list of components and their connections (nets), reference designators, footprint information, and so on. For this tutorial, we will use the logical netlist generated by a OrCAD X Capture schematic. The netlist consists of packager files (`pstxprt.dat`, `pstxnet.dat`, `pstchip.dat`, and `pstcmdb.dat`). Packaging a design combines the logic devices with physical packages, assigning a reference designator and physical pin numbers to each symbol in the schematic. The PCB Editor reads the netlist (packager) files from schematic design tool and updates the board file.

Importing Logic

To import the netlist created by the OrCAD X Capture into the PCB Editor perform the following steps:

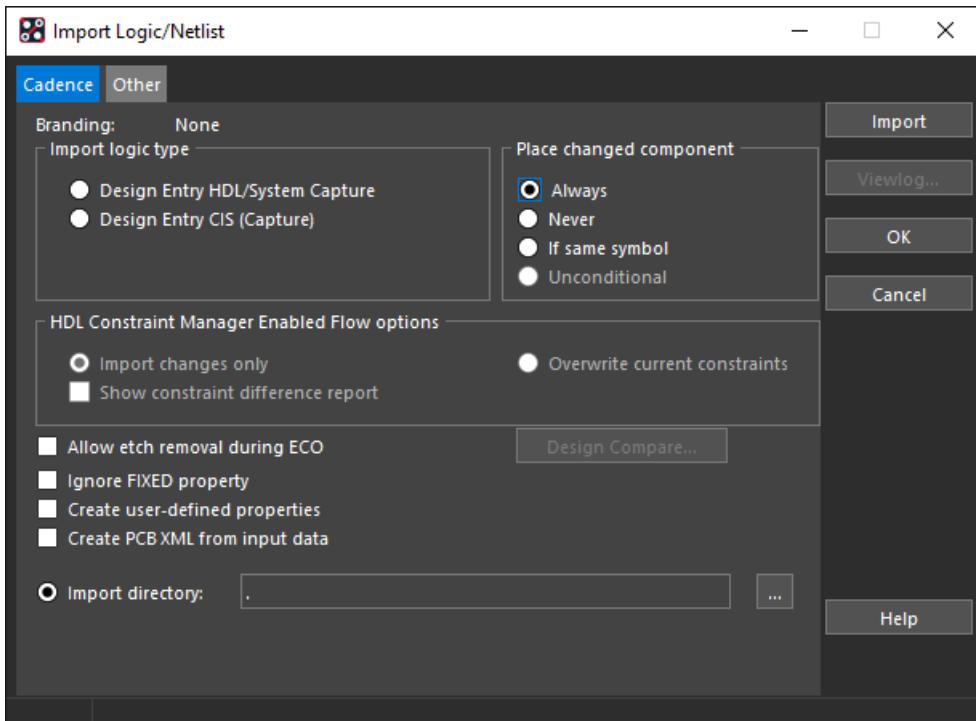
1. Choose *File – Import – Logic/Netlist* from the top menu or type `netin` in the command window.

Import Logic/Netlist dialog box is displayed.

Getting Started with Allegro X PCB Editor

Importing Logic Information

2. In the *Cadence* tab, enable the *Design Entry CIS (Capture)* checkbox in the *Import logic type* section.

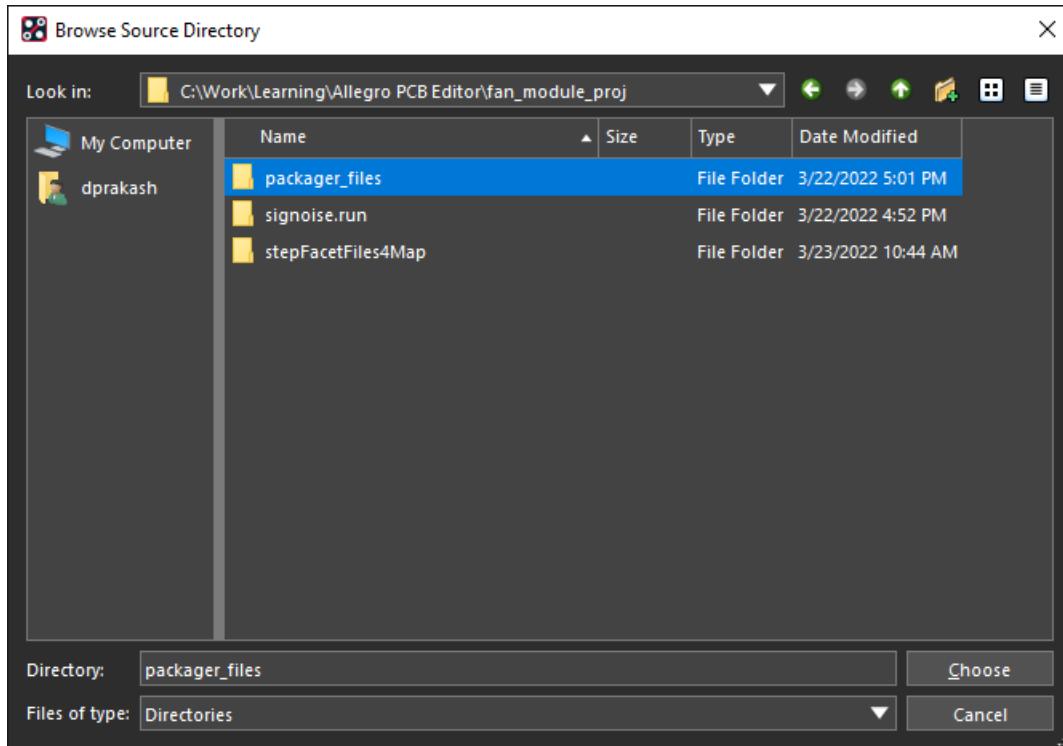


3. Click the browse button to set the *Import directory* path.

Getting Started with Allegro X PCB Editor

Importing Logic Information

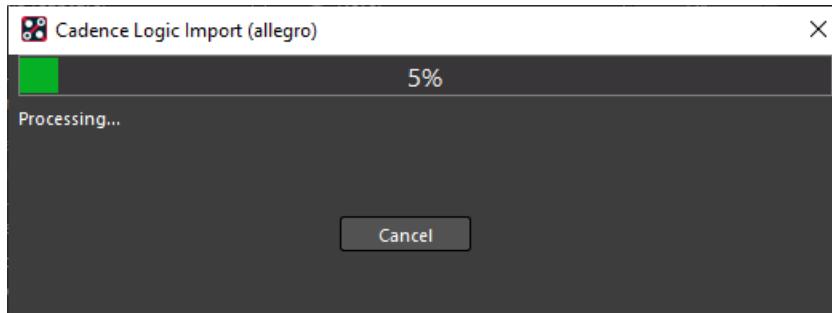
4. Select the *packger_files* folder in the Browse Source Directory window.



Note: The Import directory should be set to the directory where you exported the netlist from OrCAD X Capture.

5. Click *Import Cadence* to start importing logical information.

The *Cadence Logic Import* progress dialog box appears.



Getting Started with Allegro X PCB Editor

Importing Logic Information

- To verify that the logical netlist is imported successfully, choose *File – Viewlog* to view the `netrev.lst` log file.



The screenshot shows a window titled "View of file: netrev.lst". The window contains the following log file content:

```
(-----)
(
( Allegro Netrev Import Logic
(
( Drawing      : tutorial.brd
( Software Version : 23.1D001
( Date/Time    : Tue Aug  8 10:33:55 2023
(
(-----)

----- Directives -----

Ripup etch:          No
Ripup delete first segment: No
Ripup retain bondwire: No
Ripup symbols:        Always
Missing symbol has error: No
DRC update:          Yes
Schematic directory: 'C:/Work/Learning/Allegro PCB Editor/fan_module_proj/packager_files'
Design Directory:    'C:/Work/Learning/Allegro PCB Editor/fan_module_proj'
Old design name:     'tutorial.brd'
New design name:     'tutorial.brd'

CmdLine: netrev -S -i C:/Work/Learning/Allegro PCB Editor/fan_module_proj/packager_files -y 1 -h -q netrev_constraint_report.xml

----- Preparing to read pst files -----

Starting to read C:/Work/Learning/Allegro PCB Editor/fan_module_proj/packager_files/pstchip.dat
Finished reading C:/Work/Learning/Allegro PCB Editor/fan_module_proj/packager_files/pstchip.dat (00:00:00.98)
Starting to read C:/Work/Learning/Allegro PCB Editor/fan_module_proj/packager_files/pstxprt.dat
Finished reading C:/Work/Learning/Allegro PCB Editor/fan_module_proj/packager_files/pstxprt.dat (00:00:00.00)
Starting to read C:/Work/Learning/Allegro PCB Editor/fan_module_proj/packager_files/pstxnet.dat
Finished reading C:/Work/Learning/Allegro PCB Editor/fan_module_proj/packager_files/pstxnet.dat (00:00:00.00)

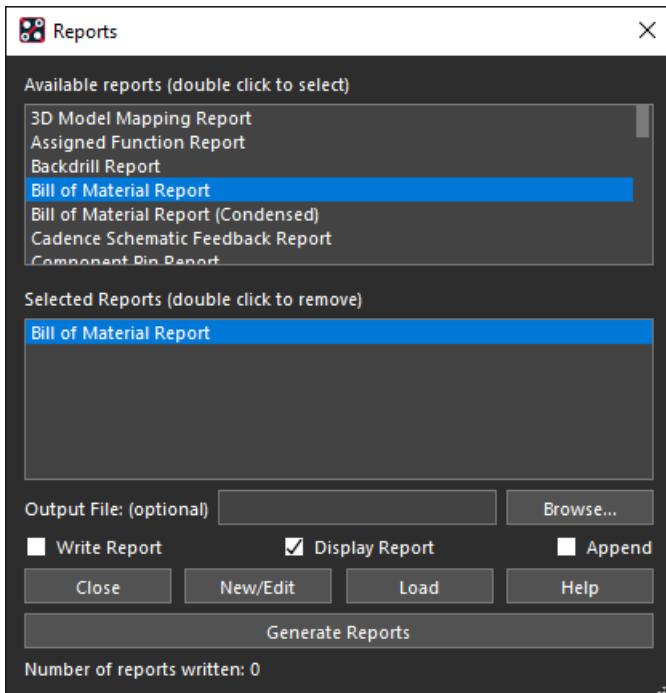
----- Oversights/Warnings/Errors -----
```

- Close the log file window.
- To view the number of components imported, choose *Tools – Reports* from the top menu or type `reports` in the command window.

Getting Started with Allegro X PCB Editor

Importing Logic Information

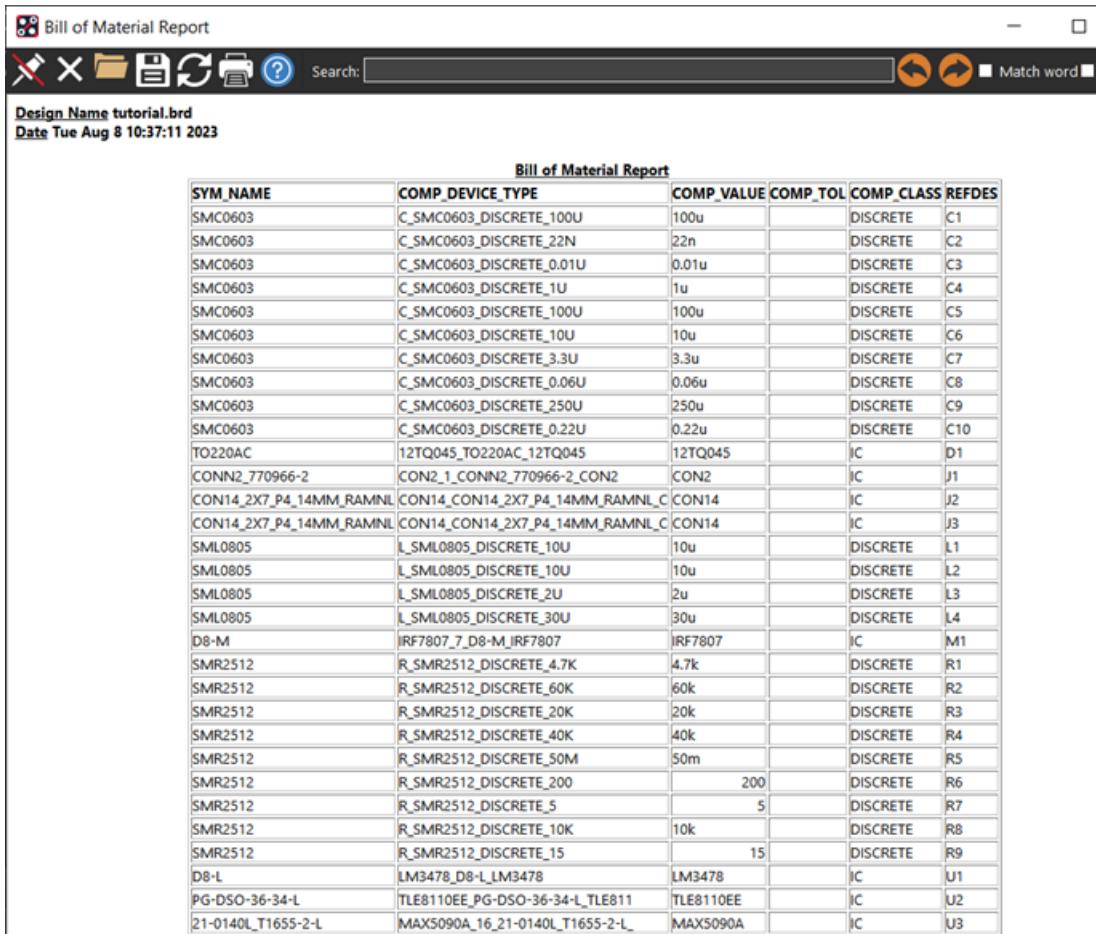
9. Double-click *Bill of Material Report* in the *Reports* dialog box to select the report and click *Generate Reports*.



Getting Started with Allegro X PCB Editor

Importing Logic Information

The report shows all the components that are imported to the database.



The screenshot shows the 'Bill of Material Report' window in the Allegro X PCB Editor. The window title is 'Bill of Material Report'. At the top, there are standard window controls (minimize, maximize, close) and a toolbar with icons for new, open, save, print, and search. A search bar with placeholder 'Search:' and a 'Match word' checkbox is located at the top right. Below the toolbar, the text 'Design Name tutorial.brd' and 'Date Tue Aug 8 10:37:11 2023' is displayed. The main content is a table titled 'Bill of Material Report' with the following columns: SYM_NAME, COMP_DEVICE_TYPE, COMP_VALUE, COMP_TOL, COMP_CLASS, and REFDES. The table lists various components such as SMC0603, TO220AC, CONN2_770966-2, CON14_2X7_P4_14MM_RAMNL, SML0805, D8-M, SMR2512, and PG-DSO-36-34-L, along with their respective values and reference designators.

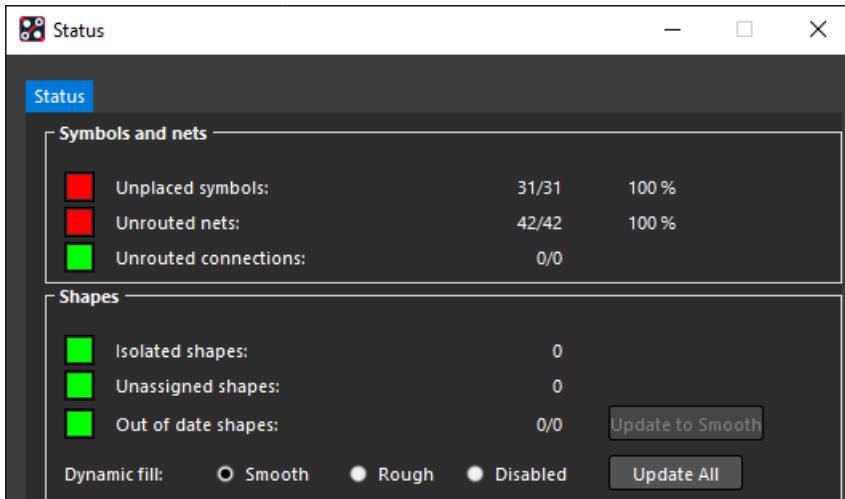
SYM_NAME	COMP_DEVICE_TYPE	COMP_VALUE	COMP_TOL	COMP_CLASS	REFDES
SMC0603	C_SMC0603_DISCRETE_100U	100u		DISCRETE	C1
SMC0603	C_SMC0603_DISCRETE_22N	22n		DISCRETE	C2
SMC0603	C_SMC0603_DISCRETE_0.01U	0.01u		DISCRETE	C3
SMC0603	C_SMC0603_DISCRETE_1U	1u		DISCRETE	C4
SMC0603	C_SMC0603_DISCRETE_100U	100u		DISCRETE	C5
SMC0603	C_SMC0603_DISCRETE_10U	10u		DISCRETE	C6
SMC0603	C_SMC0603_DISCRETE_3.3U	3.3u		DISCRETE	C7
SMC0603	C_SMC0603_DISCRETE_0.06U	0.06u		DISCRETE	C8
SMC0603	C_SMC0603_DISCRETE_250U	250u		DISCRETE	C9
SMC0603	C_SMC0603_DISCRETE_0.22U	0.22u		DISCRETE	C10
TO220AC	I2TQ045_I2TQ045	I2TQ045		IC	D1
CONN2_770966-2	CONN2_1_CONN2_770966-2_CONN2	CONN2		IC	J1
CON14_2X7_P4_14MM_RAMNL	CON14_CON14_2X7_P4_14MM_RAMNL_C	CON14		IC	J2
CON14_2X7_P4_14MM_RAMNL	CON14_CON14_2X7_P4_14MM_RAMNL_C	CON14		IC	J3
SML0805	L_SML0805_DISCRETE_10U	10u		DISCRETE	L1
SML0805	L_SML0805_DISCRETE_10U	10u		DISCRETE	L2
SML0805	L_SML0805_DISCRETE_2U	2u		DISCRETE	L3
SML0805	L_SML0805_DISCRETE_30U	30u		DISCRETE	L4
D8-M	IRF7807_7_D8-M_IRF7807	IRF7807		IC	M1
SMR2512	R_SMR2512_DISCRETE_4.7K	4.7k		DISCRETE	R1
SMR2512	R_SMR2512_DISCRETE_60K	60k		DISCRETE	R2
SMR2512	R_SMR2512_DISCRETE_20K	20k		DISCRETE	R3
SMR2512	R_SMR2512_DISCRETE_40K	40k		DISCRETE	R4
SMR2512	R_SMR2512_DISCRETE_50M	50m		DISCRETE	R5
SMR2512	R_SMR2512_DISCRETE_200	200		DISCRETE	R6
SMR2512	R_SMR2512_DISCRETE_5	5		DISCRETE	R7
SMR2512	R_SMR2512_DISCRETE_10K	10k		DISCRETE	R8
SMR2512	R_SMR2512_DISCRETE_15	15		DISCRETE	R9
D8-L	LM3478_D8-L_LM3478	LM3478		IC	U1
PG-DSO-36-34-L	TLE8110EE_PG-DSO-36-34-L_TLE811	TLE8110EE		IC	U2
21-0140L_T1655-2-L	MAX5090A_16_21-0140L_T1655-2-L	MAX5090A		IC	U3

10. Close the report and the Reports dialog box.
11. Choose *Display – Status* from the top menu.

Getting Started with Allegro X PCB Editor

Importing Logic Information

The status indicators for Unplaced Symbols and Unrouted nets are shown in red color.



12. Click *OK* to close the *Status* dialog box.

13. Choose *File – Save* to save the design.

Summary

You learned how to load and import the netlist into the PCB Editor. You also learned how to generate a report and view the status to verify the design.

In this section, you have learned the following:

- **New menu commands:** *File – Import – Logic/Netlist, File – Viewlog, Tools – Reports, Display – Status*
- **New console commands:** `netin, viewlog, reports, status`
- **New window and dialog box:** Import Logic/Netlist dialog box, Reports, and Status
- **New files created:** `netrev.lst`

What's Next

In the next section, you will learn how to use place commands to place the components in the layout.

Recommended Reading

For more information, see the [Allegro User Guide: Transferring Logic Design Data](#) and [Allegro PCB and Package Physical Layout Command Reference](#) in the documentation set.

Placing Components

The component placement is an important step for layout designing. An optimum component placement ensures easy routing and good electrical performance.

This section explains the commands you will use for placing components on the board. You can place the components based on reference designators, mechanical symbols, package symbols, and format symbols in the PCB Editor.

Setting Non-Etch Grid

Before beginning the component placement adjust the placement grid

- 1. . Choose *Setup – Grids*.**

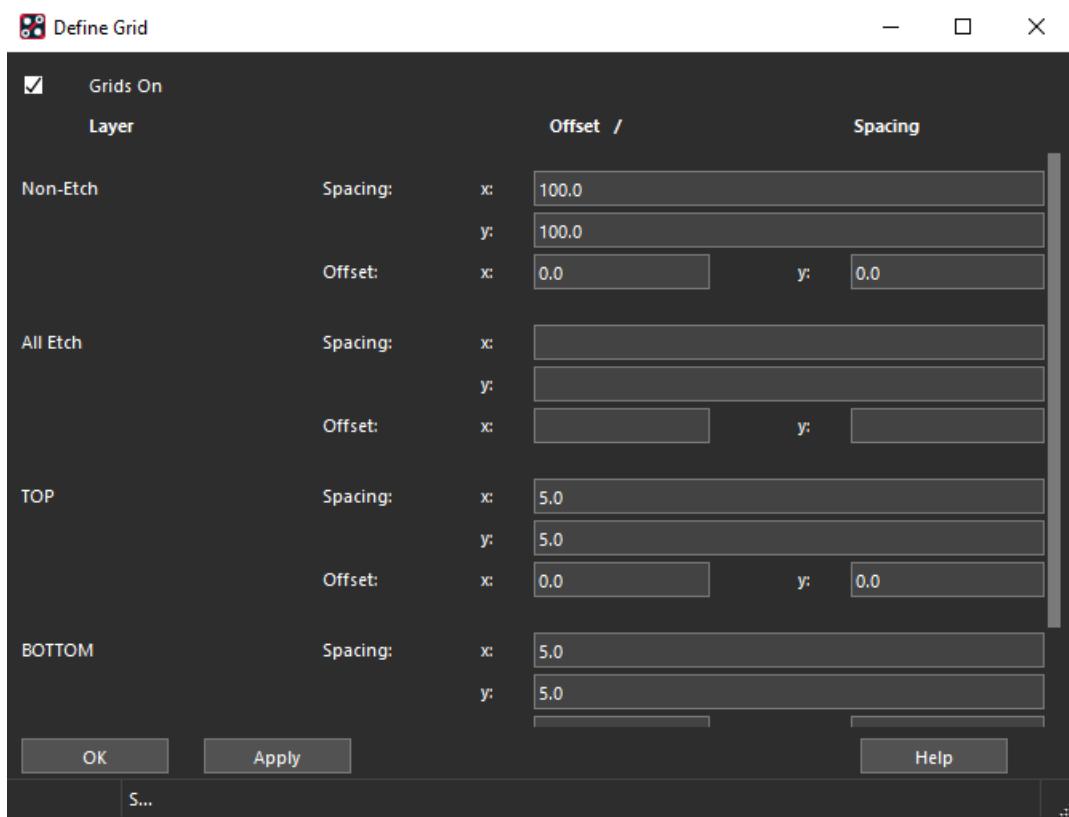
The Define Grid window is displayed.

- 2. Enable *Grids On* check box.**

- 3. Click *OK* to apply the grid settings.**

Getting Started with Allegro X PCB Editor

Placing Components



The visibility of Non-Etch grid is turned on. When placing components, the origin of the package symbol snaps to this grid.

Placing Components

For placing components, do the following:

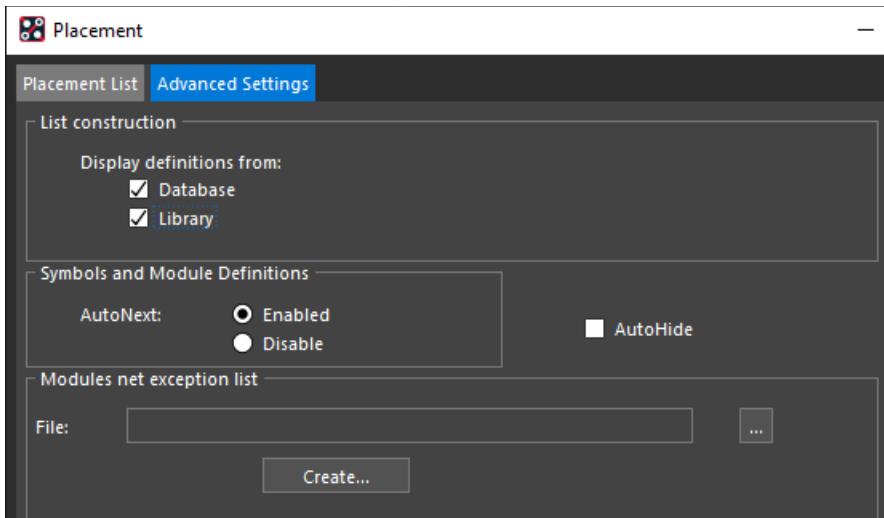
1. Choose *Place – Manually*.

The *Placement* dialog box opens.

Getting Started with Allegro X PCB Editor

Placing Components

2. In the *Advanced Settings* tab, enable *Autohide* check box in the *Symbols and Module Definitions* section to automatically hide the *Placement* dialog box during component placement.

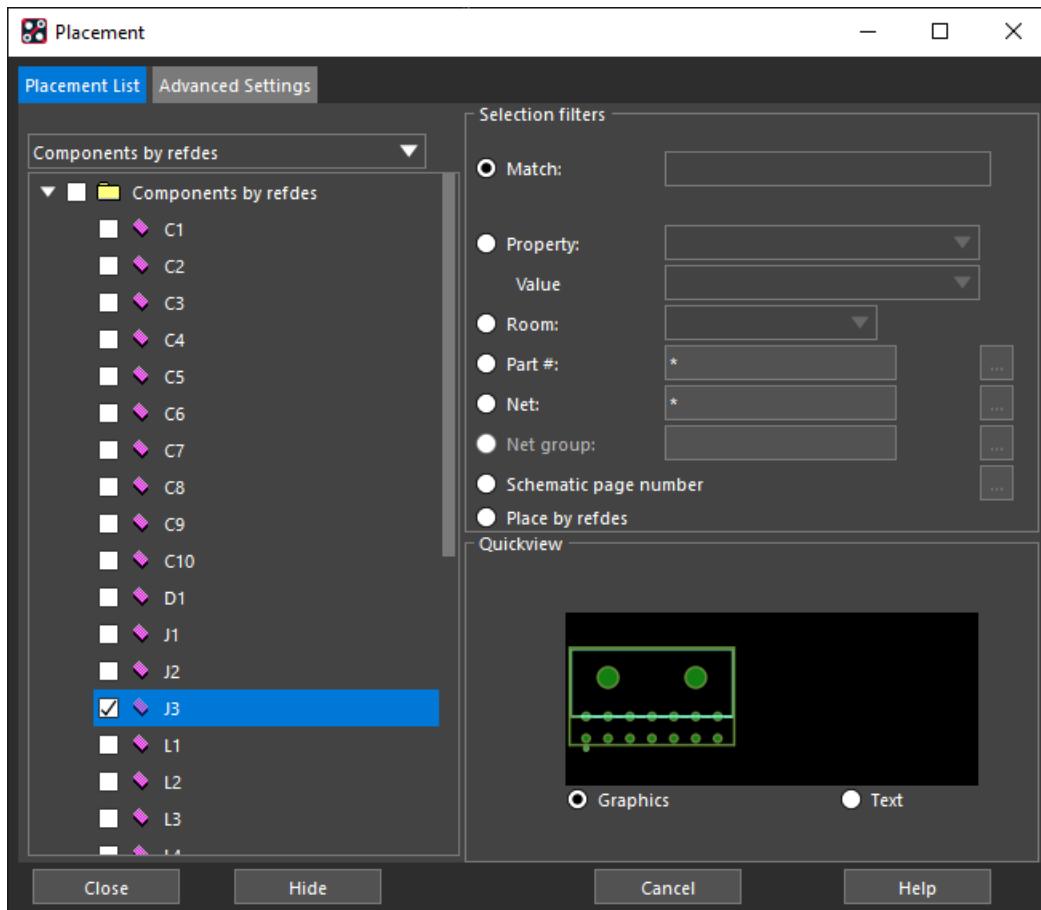


3. In the *Placement List* tab, choose *Components by refdes* from the pull-down menu.

Getting Started with Allegro X PCB Editor

Placing Components

4. In the components list, select the check box for J3.



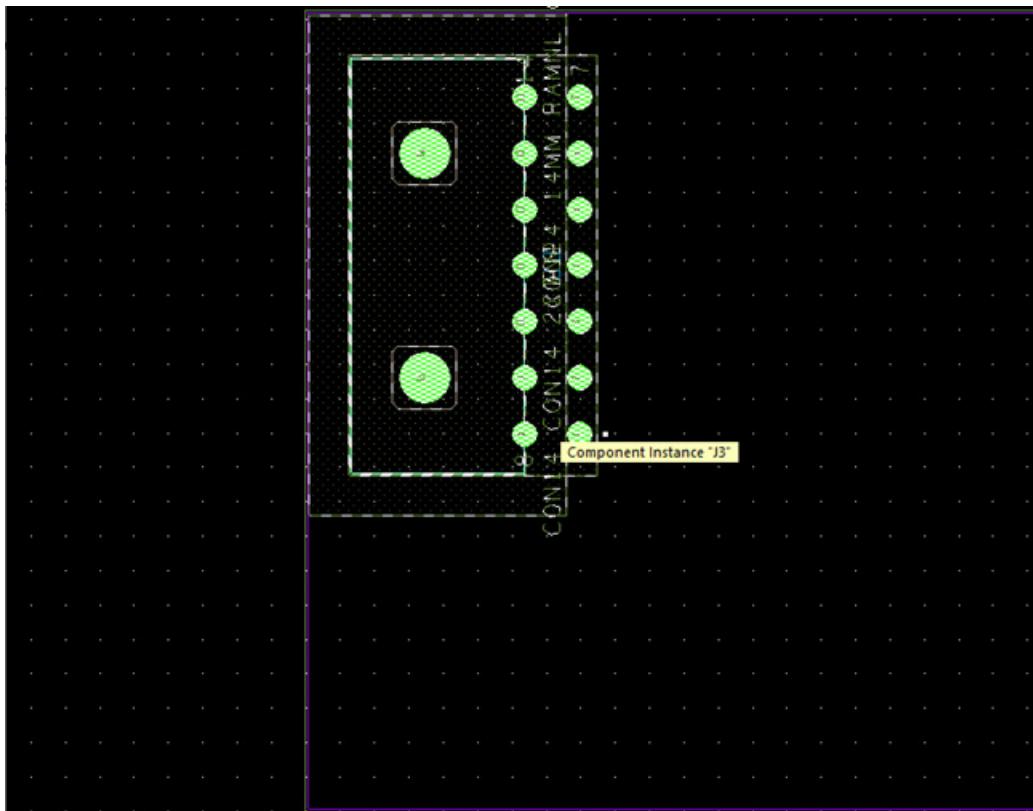
The graphical preview of the footprint is displayed in the *Quickview* window and the symbol gets attached to the cursor.

5. Move the cursor near the left boundary of the outline and right-click to choose *Rotate*. Use the handlebar to rotate the symbol by 90 degrees in anti-clockwise direction.

Getting Started with Allegro X PCB Editor

Placing Components

6. Click to place the symbol in the design canvas.

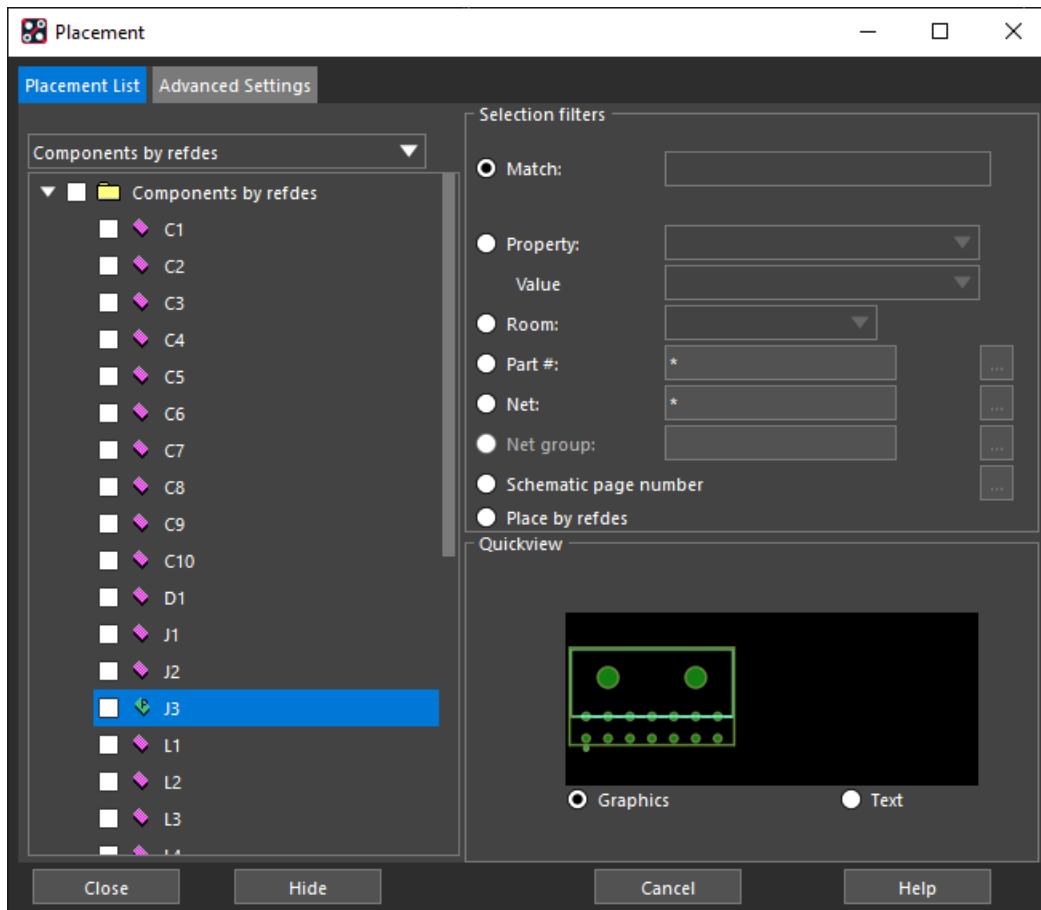


7. Right-click and choose *Done*.

Getting Started with Allegro X PCB Editor

Placing Components

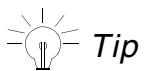
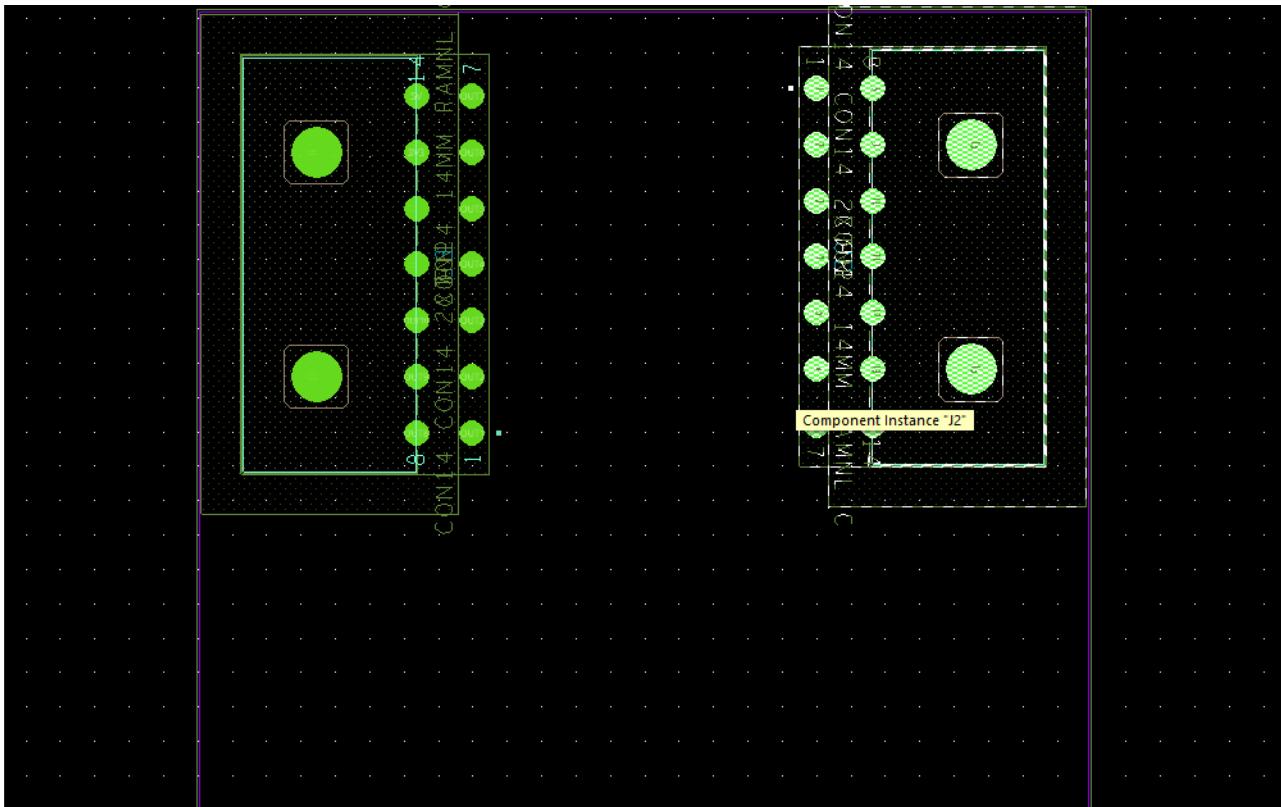
The placed component J3 is now indicated with (green P).



Getting Started with Allegro X PCB Editor

Placing Components

8. Similarly, select J2 from the list and place it along the right boundary of the design outline.

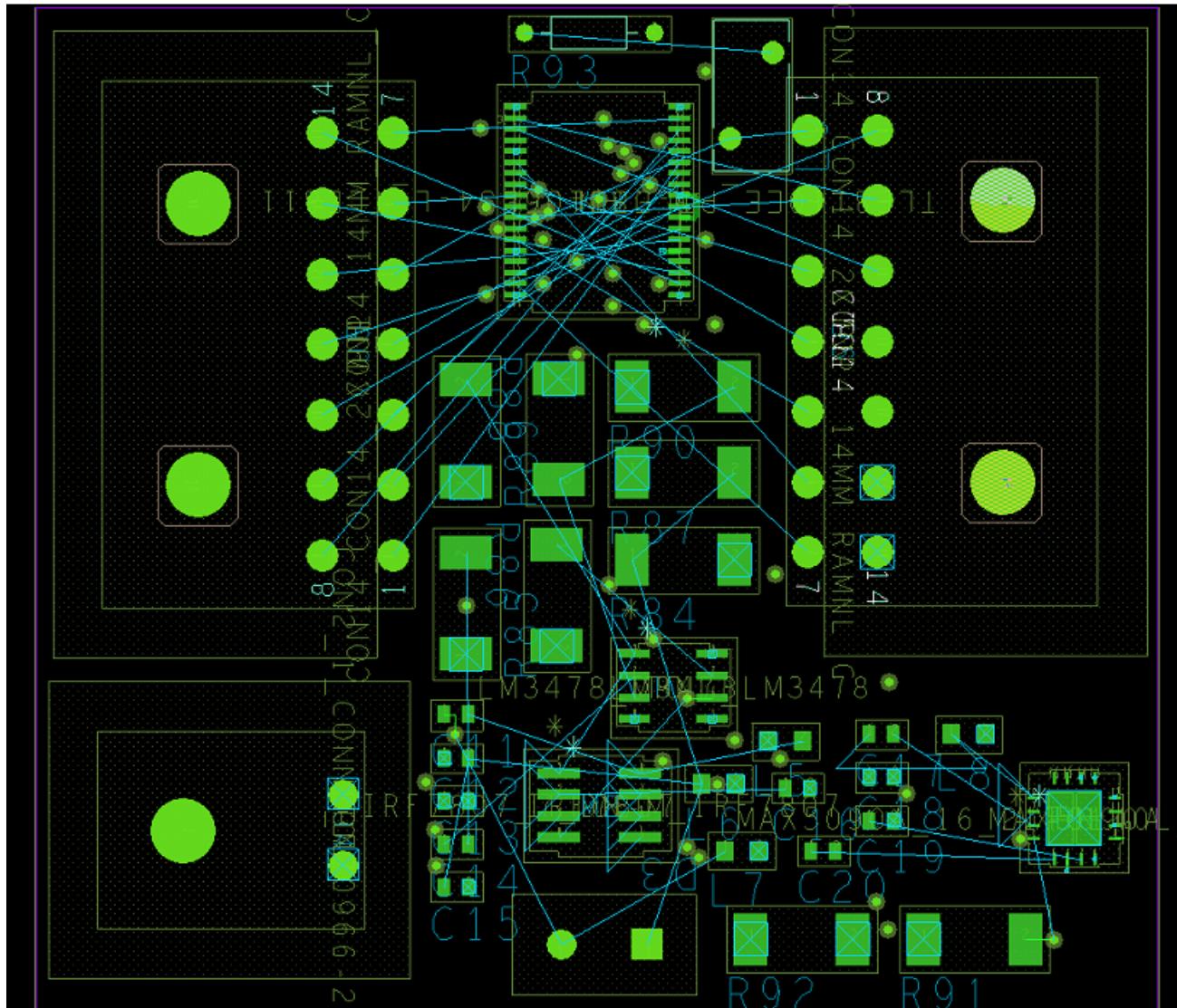


To delete a component, set *Find* filter to *Symbols* and select *Edit – Delete* or right-click and choose *Unplace component* from the pop-up menu.

Getting Started with Allegro X PCB Editor

Placing Components

9. Similarly, select each reference designator one by one to place all the component symbols. The following image depicts a sample placement.



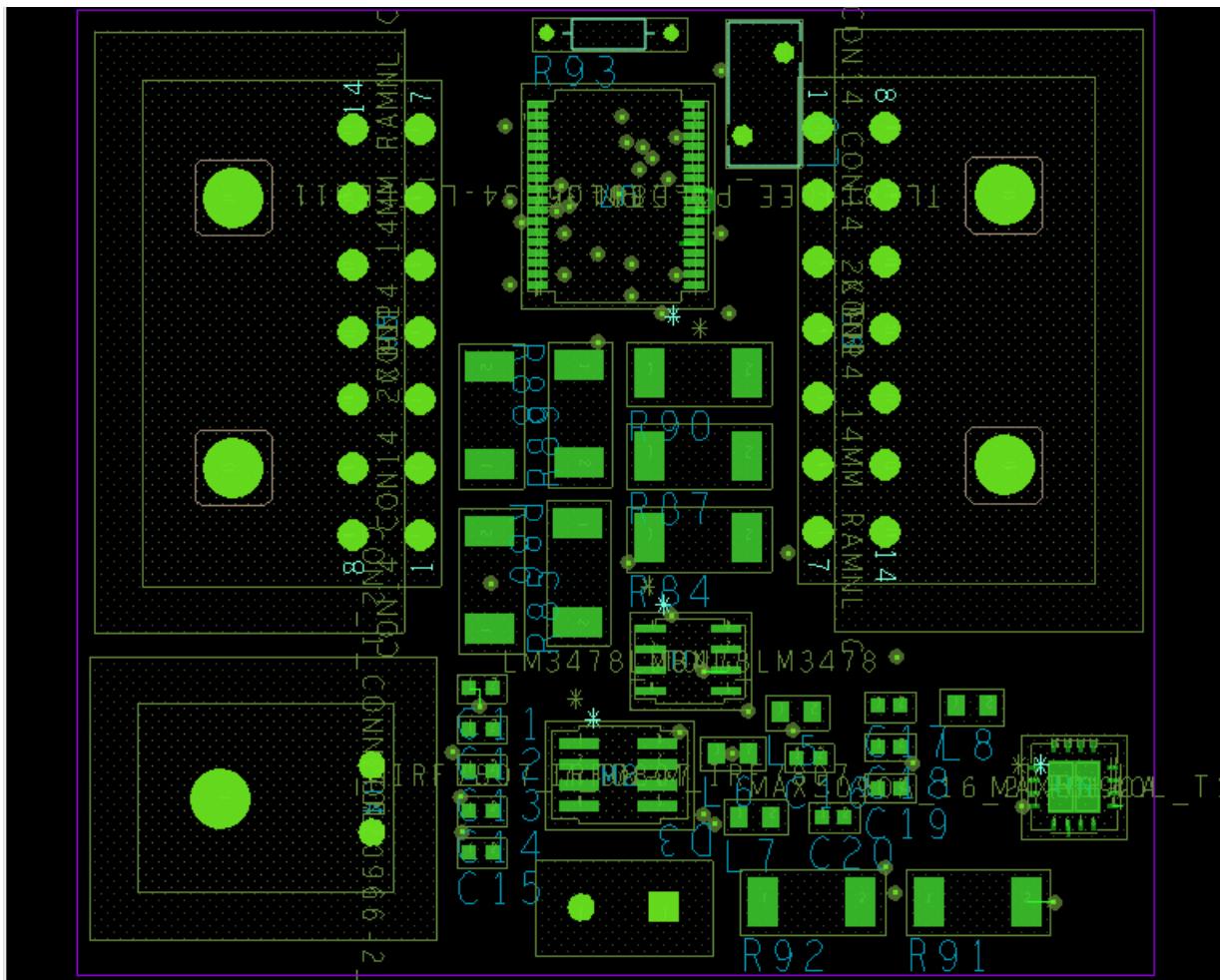
Ratsnests lines are displayed between pins of the same net and helps placing components that are connected close to each other.

10. Choose *Display – Blank Rats – All* to hide all ratsnests from the design.

Getting Started with Allegro X PCB Editor

Placing Components

The figure shows the design with all components are placed.

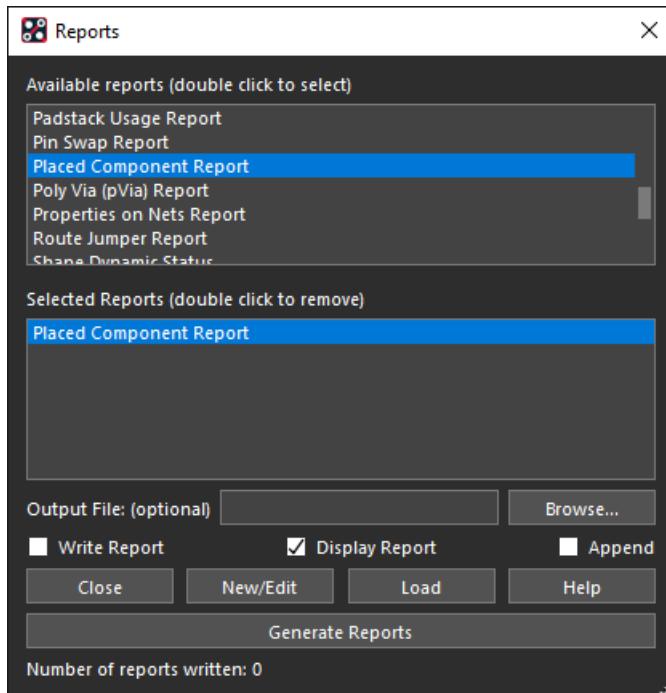


11. To verify that all the components are placed, choose *Tools – Reports*.

Getting Started with Allegro X PCB Editor

Placing Components

12. Double-click to select *Placed Component Report* to select and click *Generate Reports*.



13. The report window displays list of all placed components.

Placed Component Report								
REFDES	COMP_DEVICE_TYPE	COMP_VALUE	COMP_TOL	SYM_NAME	SYM_X	SYM_Y	SYM_ROTATE	SYM_MIRROR
C1	C_SMC0603_DISCRETE_100U	100u		SMC0603	9600.0	11800.0	0.000	NO
C2	C_SMC0603_DISCRETE_22N	22n		SMC0603	9600.0	11700.0	0.000	NO
C3	C_SMC0603_DISCRETE_0.01U	0.01u		SMC0603	9600.0	11600.0	0.000	NO
C4	C_SMC0603_DISCRETE_1U	1u		SMC0603	9600.0	11500.0	0.000	NO
C5	C_SMC0603_DISCRETE_100U	100u		SMC0603	9600.0	11400.0	0.000	NO
C6	C_SMC0603_DISCRETE_10U	10u		SMC0603	9600.0	11300.0	0.000	NO
C7	C_SMC0603_DISCRETE_3.3U	3.3u		SMC0603	9600.0	11200.0	0.000	NO
C8	C_SMC0603_DISCRETE_0.06U	0.06u		SMC0603	10500.0	11800.0	0.000	NO
C9	C_SMC0603_DISCRETE_250U	250u		SMC0603	10700.0	11800.0	0.000	NO
C10	C_SMC0603_DISCRETE_0.22U	0.22u		SMC0603	10900.0	11800.0	0.000	NO
D1	12TQ045_TO220AC_12TQ045	12TQ045		TO220AC	10100.0	11200.0	180.000	NO
J1	CONN2_1_CONN2_770966-2_CONN2	CONN2		CONN2_770966-2	9300.0	11500.0	270.000	NO
J2	CONN14_CONN14_2X7_P4_14MM_RAMNL_C	CONN14		CONN14_2X7_P4_14MM_RAMNL	10400.0	13100.0	270.000	NO
J3	CONN14_CONN14_2X7_P4_14MM_RAMNL_C	CONN14		CONN14_2X7_P4_14MM_RAMNL	9400.0	12100.0	90.000	NO
L1	L_SML0805_DISCRETE_10U	10u		SML0805	10300.0	11600.0	0.000	NO
L2	L_SML0805_DISCRETE_10U	10u		SML0805	10500.0	11600.0	0.000	NO
L3	L_SML0805_DISCRETE_2U	2u		SML0805	10300.0	11500.0	0.000	NO

Getting Started with Allegro X PCB Editor

Placing Components

14. Close the *Placed Component Report*.
15. Double-click *Placed Component Report* in the *Selected Reports* section to remove it from the list.
16. Find and choose *Unplaced Component Report* in the *Selected Reports* section.
17. Click *Generate Reports*.



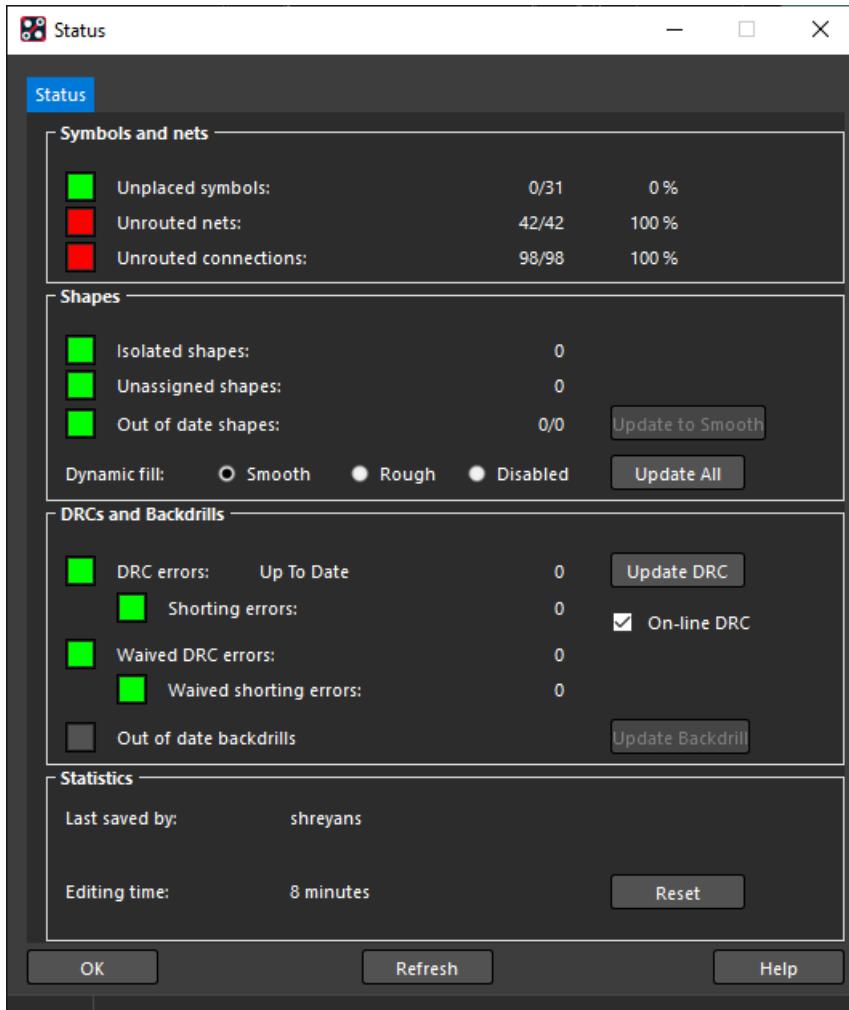
The report shows that total unplaced components are zero.

18. Close the report window.
19. Click *Close* to close the *Reports* dialog box.
20. Choose *Display – Status*.

Getting Started with Allegro X PCB Editor

Placing Components

The status indicators for *Unplaced symbols* is turned green.



21. Click *OK* to close the *Status* dialog box.

22. Choose *File – Save*.

A message windows is displayed stating that this file already exists.

23. Click *Yes* to confirm the override.

Summary

You learned how to interactively place the components in the Allegro X PCB Editor. You also learned how to generate the report and view the status to verify the design.

In this section, you have learned the following:

- **New menu commands:** *Setup – Grids, Setup – Application Mode – Placement Edit, Place – Manually, Display – Blank Rats – All.*
- **New console commands:** define grid, placementedit, place manual, unrats all.
- **New window and dialog box:** Define Grid and Placement.
- **New files created:** none

What's Next

In the next section you will learn how to automatically route the nets in the layout.

Recommended Reading

For more information, see the [Allegro User Guide: Placing the Elements](#) and [Allegro PCB and Package Physical Layout Command Reference](#) in the documentation set.

Getting Started with Allegro X PCB Editor

Placing Components

Routing the Design

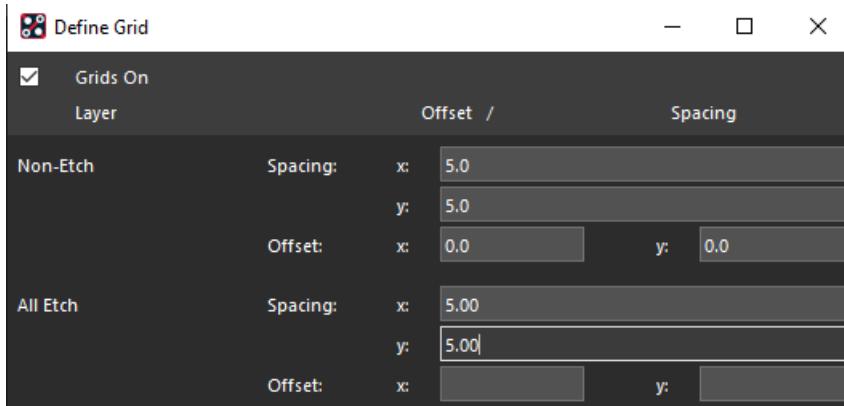
Routing is the process of laying down the tracks to connect components on the board. This section introduces the use of auto-router to route the nets in the design.

Setting up Grids

1. Choose *Setup – Grids*.

The *Define Grid* window is displayed.

2. Ensure that the *Grids On* checkbox is enabled.
3. In the *All Etch* section, set spacing to 5 mils for both *X* and *Y* directions.
4. Click *OK* to apply the grid settings.



Defining Constraints

The design constraints are the rules required to route the design. You can define spacing and physical design rules within the PCB Editor using the Constraint Manager. The basic rules include the minimum width of the cline and spacing between two clines.

Getting Started with Allegro X PCB Editor

Routing the Design

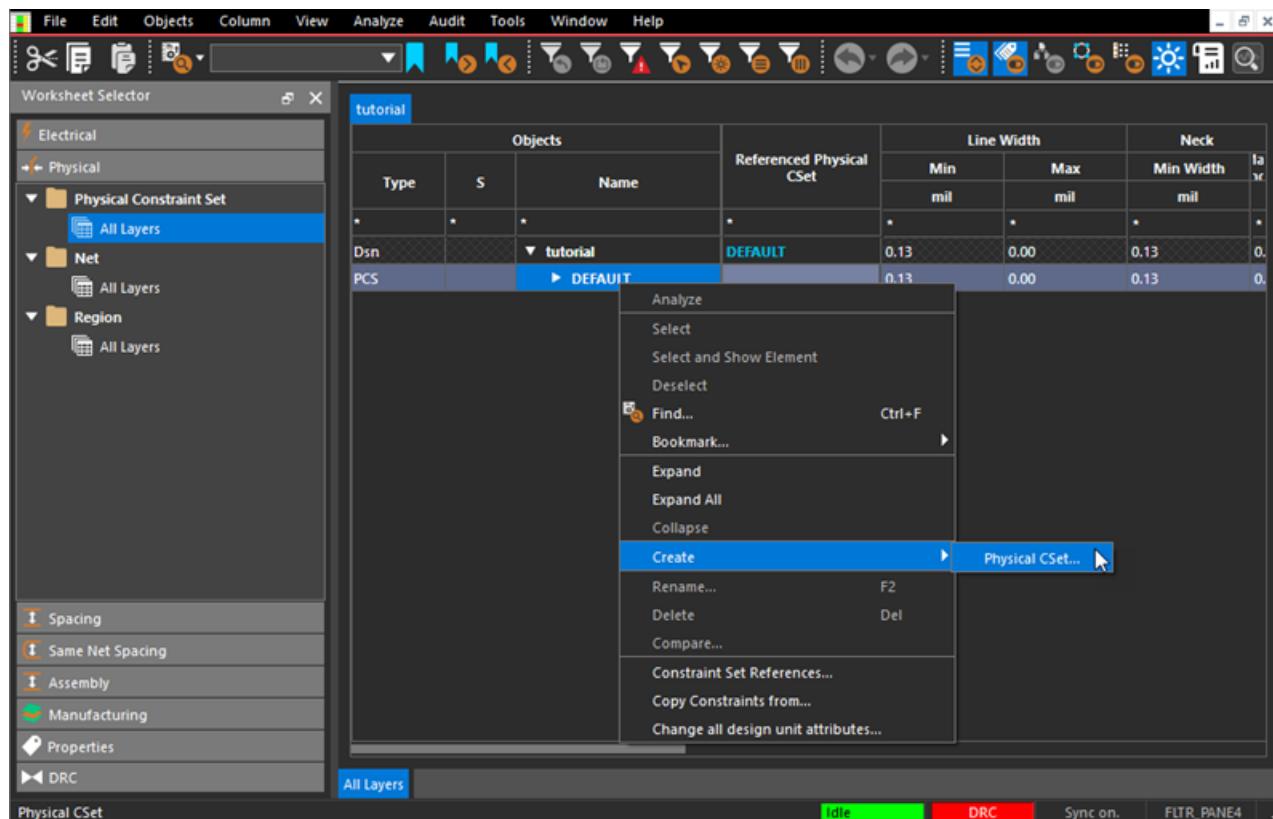
Note: You can set all constraints in either the schematic editor or in the layout editor or in both. When a design is exported from the schematic design editor, the constraints are also exported and honored by PCB Editor.

For this tutorial, specify two constraints for routing power nets: minimum thickness of the cline and maximum length of cline in neck mode.

1. Choose *Setup – Constraints – Constraint Manager* or type `cmgr` in the command window.

The *Allegro Constraint Manager* opens.

2. Click *Physical* and choose *All Layers* worksheet in the *Physical Constraint Set* folder.
3. In the worksheet, select the default physical constraint set and right-click to choose *Create – Physical CSet*.



The *Create PhysicalCSet* dialog box is displayed.

4. Specify the name as `POWER_NET_CSET` and click *OK*.

Getting Started with Allegro X PCB Editor

Routing the Design

5. Change the value of *Min Line Width* to 15 mil and *Max Neck Length* to 100 mil for both TOP and BOTTOM layers.

Type	S	Name	Referenced Physical CSet	Line Width		Neck	
				Min	Max	Min Width	Max Length
				mil	mil	mil	mil
*	*	*	*	*	*	*	*
Dsn		▼ tutorial	DEFAULT	5.00	0.00	5.00	0.00
PCS		► DEFAULT		5.00	0.00	5.00	0.00
PCS		▼ POWER_NET_CSET		15.00	0.00	5.00	100.00
LTyp		▼ Conductor		15.00	0.00	5.00	100.00
lyr	1	TOP		15.00	0.00	5.00	100.00
lyr	2	BOTTOM		15.00	0.00	5.00	100.00

6. Choose *Net – All Layers*.
7. In the *All Layers* worksheet, select the net 5V.
8. Set the *Referenced Physical CSet* to POWER_NET_CSET.
9. Similarly, select the nets 3V3 and 0 and set *Referenced Physical CSet* to POWER_NET_CSET.
10. Choose *File – Close* to close *Constraint Manager*.

Assigning Color to Power and Ground nets

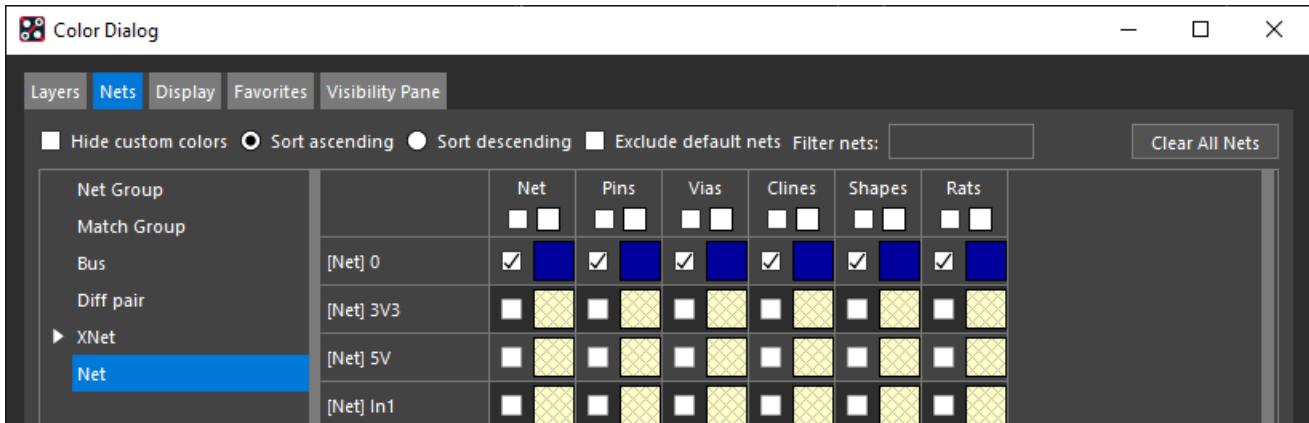
Changing the visibility of power and ground nets makes them easier to route.

1. Choose *Display – Color/Visibility* or click *Color192* icon.
The *Color Dialog* opens.
2. Open *Nets* tab and select *Net* in the left-hand pane.
All the nets in the design are displayed in the right-hand pane.

Getting Started with Allegro X PCB Editor

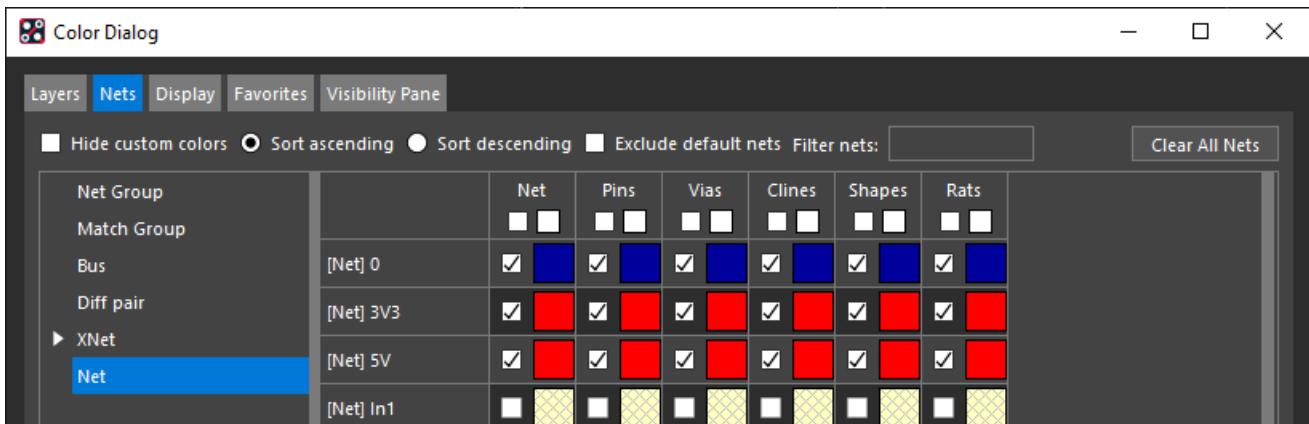
Routing the Design

3. Choose a blue color chip from the *Available Colors* section and select [Net] 0.



All the pins, vias, clines and shapes that are connected to [Net] 0 are shown in blue color on the design canvas.

4. Similarly, select red color from the *Available Colors* section and apply to [Net] 3V3 and [Net] 5V.



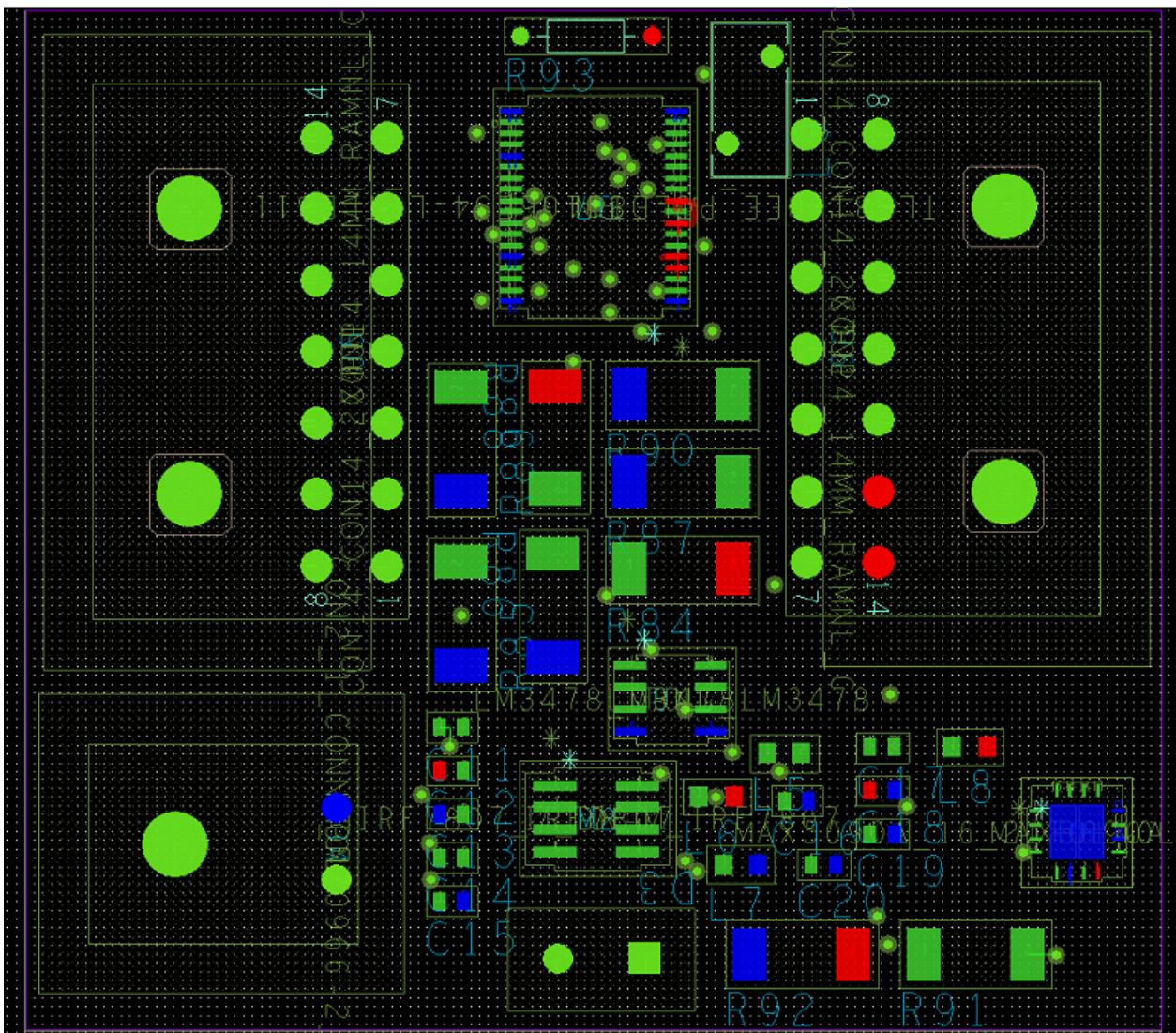
All the pins, vias, clines and shapes that are connected to [Net] 3V3 and [Net] 5V are colored with red color in the design.

5. Click *OK* to close the *Color Dialog*.

Getting Started with Allegro X PCB Editor

Routing the Design

6. Click *View – Zoom Fit* to view the entire board.



7. Choose *File – Save* to save the file.

Routing Design Using Automatic Router

1. Choose *Setup – Application Mode – Etch Edit*.

The environment to perform routing related command is set.

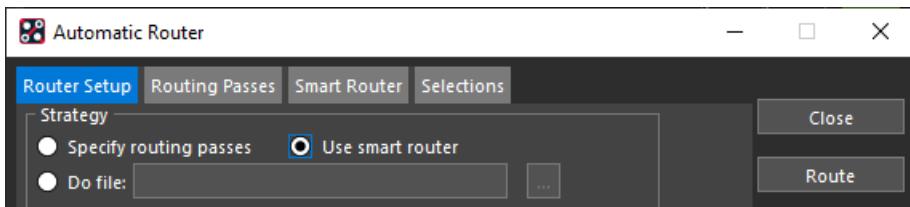
2. To show all rats, choose *Display – Show Rats – All*.
3. Choose *Route – PCB Router – Route Automatic*.

Getting Started with Allegro X PCB Editor

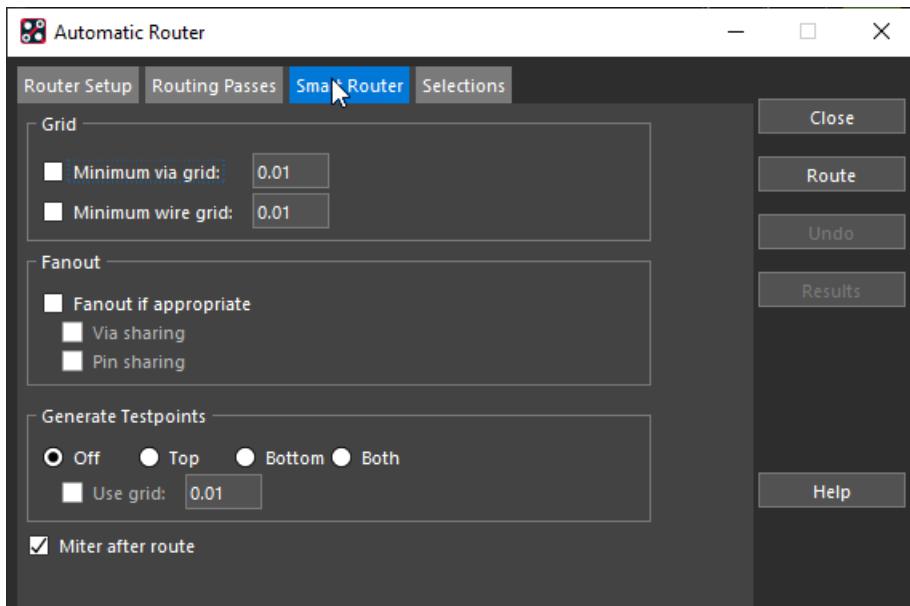
Routing the Design

The *Automatic Router* dialog box opens.

4. In the *Router Setup* tab, enable *Use smart router* checkbox in the *Strategy* section.



5. Open *Smart Router* tab and enable *Miterafter route* checkbox.

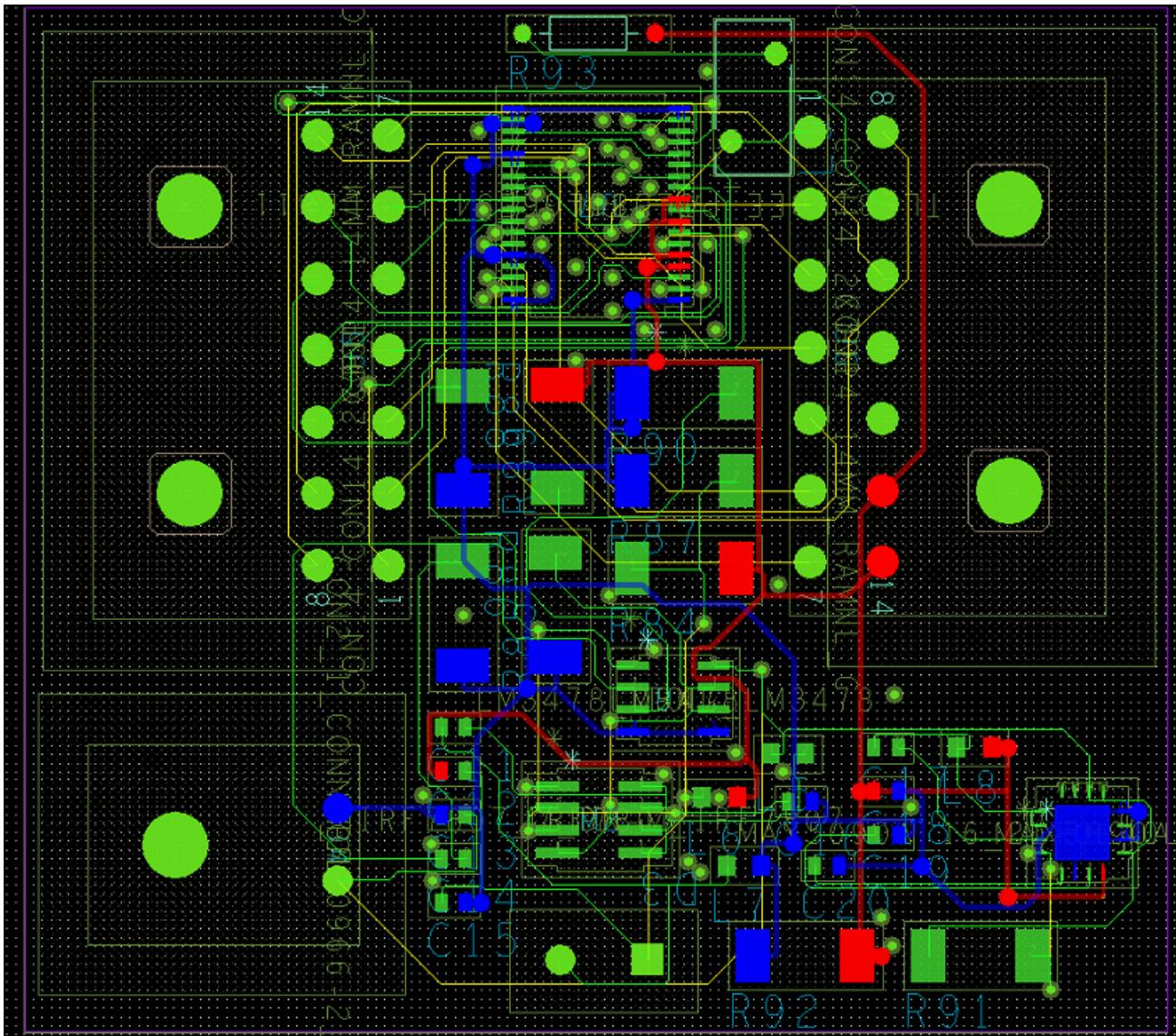


6. Click *Route* to start the automatic routing process.
7. When routing is completed, click *Close* in the *Automatic Router* dialog box.

Getting Started with Allegro X PCB Editor

Routing the Design

8. Click *View – Zoom Fit* to see the complete board.



Note: Your screen may look differently depending on the current visibility settings.

9. Choose *File – Save* to save the design.

Generating Reports

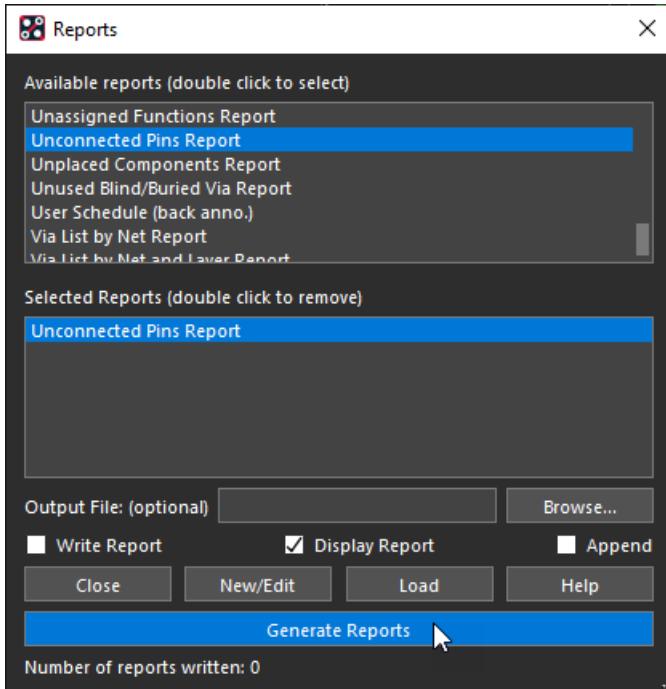
1. Choose *Tools – Reports*.

The *Reports* dialog box opens.

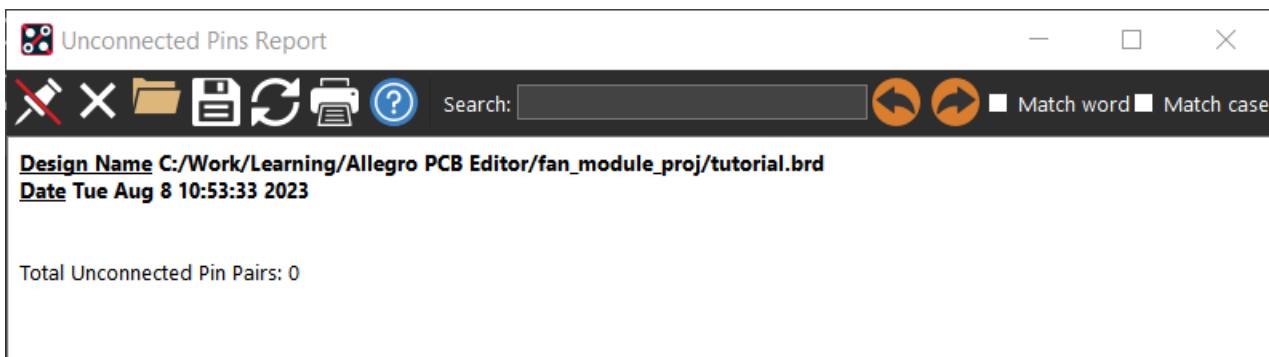
Getting Started with Allegro X PCB Editor

Routing the Design

- Double-click *Unconnected Pins Report* in the *Reports* dialog box and click *Generate Reports*.



- The report window displays list of unconnected pins.

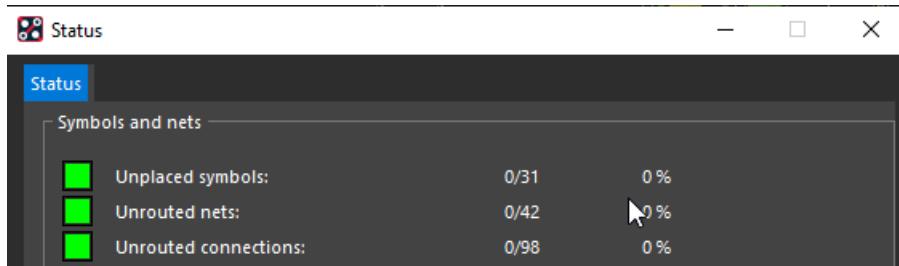


- Close the *Unconnected Pins Report*.
- Click *Close* to in the *Reports* dialog box.
- Click *Display – Status* from the top menu to verify if all the nets are routed.

Getting Started with Allegro X PCB Editor

Routing the Design

The status indicators for *Unrouted nets* and connections are now turned green.



7. Click *OK* to close the Status dialog.

8. Choose *File – Save*.

A message windows is displayed stating that this file already exists.

9. Click *Yes* to confirm the override.

Summary

You learned how to route the nets using auto-router. You also learned how to generate the report and view the status to verify the design.

- **New menu commands:** *Setup – Constraints – Constraint Manager, Display – Color/Visibility, Setup – Application Mode – Etch Edit, Display – Show Rats – All, Route – PCB Router – Route Automatic*
- **New console commands:** `cmgr`, `color192`, `etchedit`, `rats all`, `auto_route`
- **New window and dialog box:** Allegro Constraint Manager, Color Dialog, Automatic Router
- **New files created:** `none`

What's Next

In the next section, you will learn how to verify the design using 3D Canvas and generate reports.

Recommended Reading

For more information, see the [Allegro User Guide: Routing the Design](#) and [Allegro PCB and Package Physical Layout Command Reference](#) in the documentation set.

Validating Design

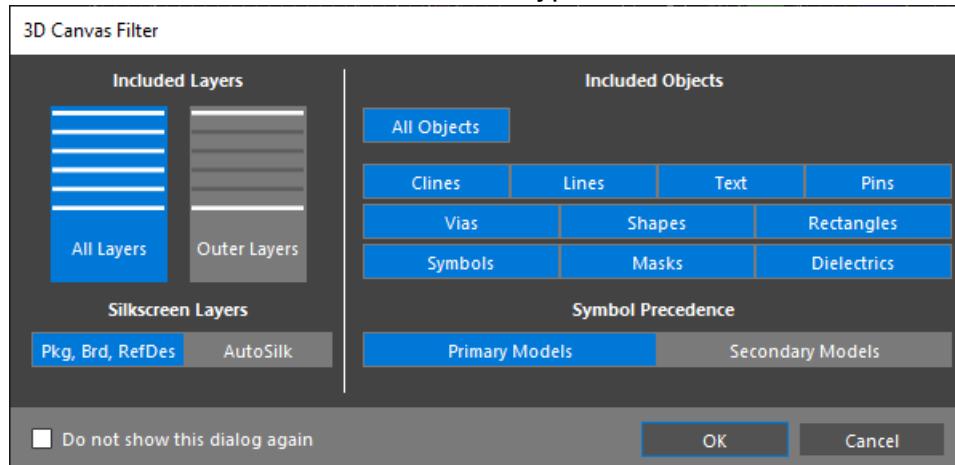
This section explains how to verify in the 3D to get it ready for manufacture.

Viewing Design in 3D Canvas

The built-in 3D visualization tool of Allegro PCB Editor lets you preview the board design at any time during the design. You can open the design in 3D Canvas and verify the design as a complete assembly.

To analyze a design, 3D models must be assigned to all the symbols. You can map a 3D model either at a symbol level or at the design level. PCB Editor, by default, supports STEP models for 3D visualization. For the components used in this tutorial, 3D models are mapped with symbols.

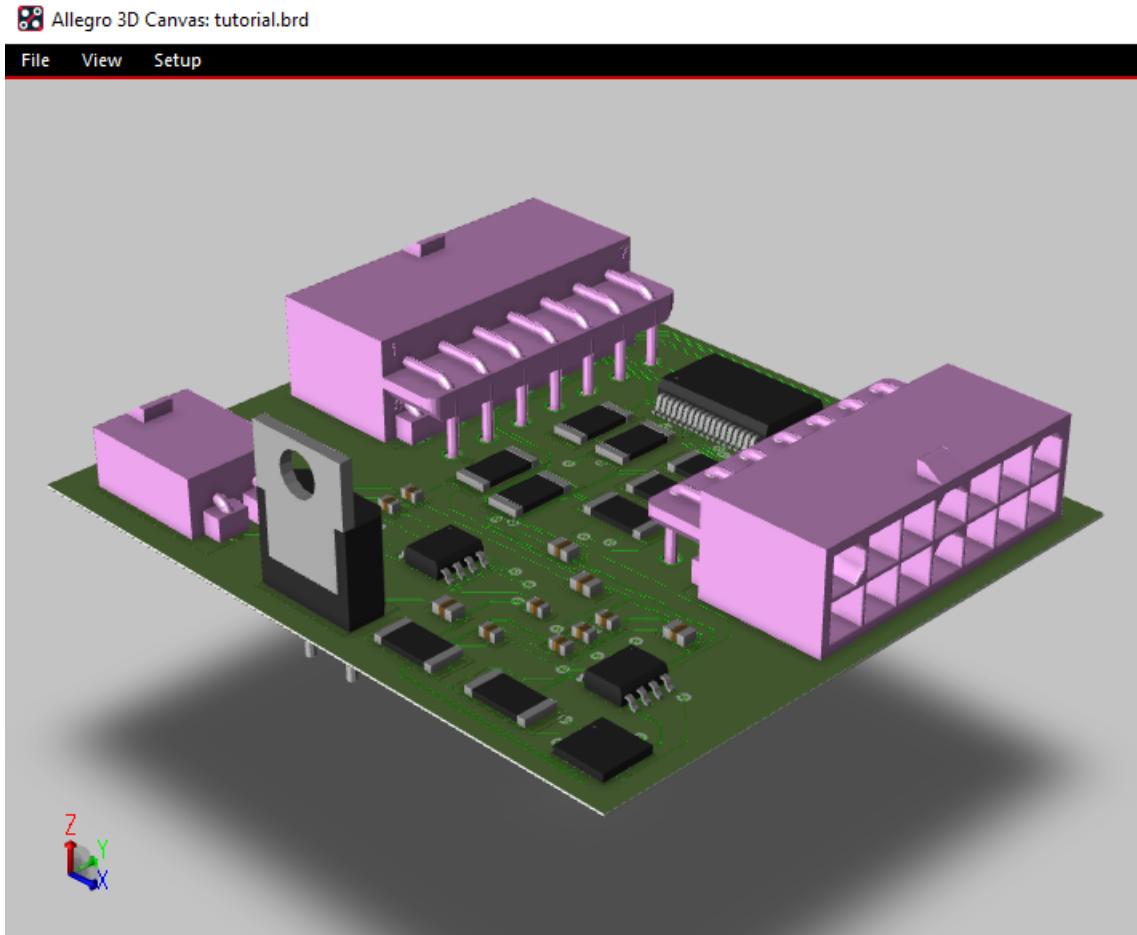
1. Choose *View – 3D Canvas* or type `3d` in the command window.



Getting Started with Allegro X PCB Editor

Validating Design

A progress bar displays while loading the design into 3D Canvas.



2. Choose *View – Camera* options to view the design in different perspectives.
3. Close *3D Canvas*.

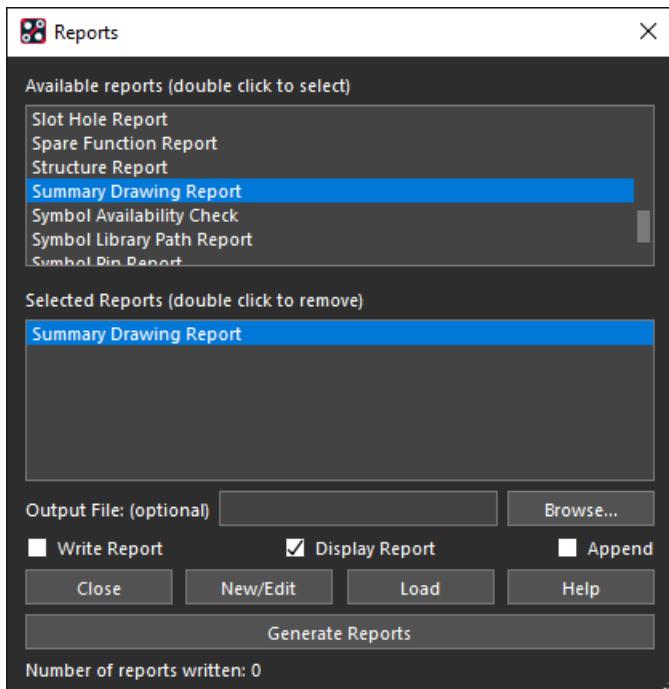
Generating Reports

1. Choose *Tools – Reports*.

Getting Started with Allegro X PCB Editor

Validating Design

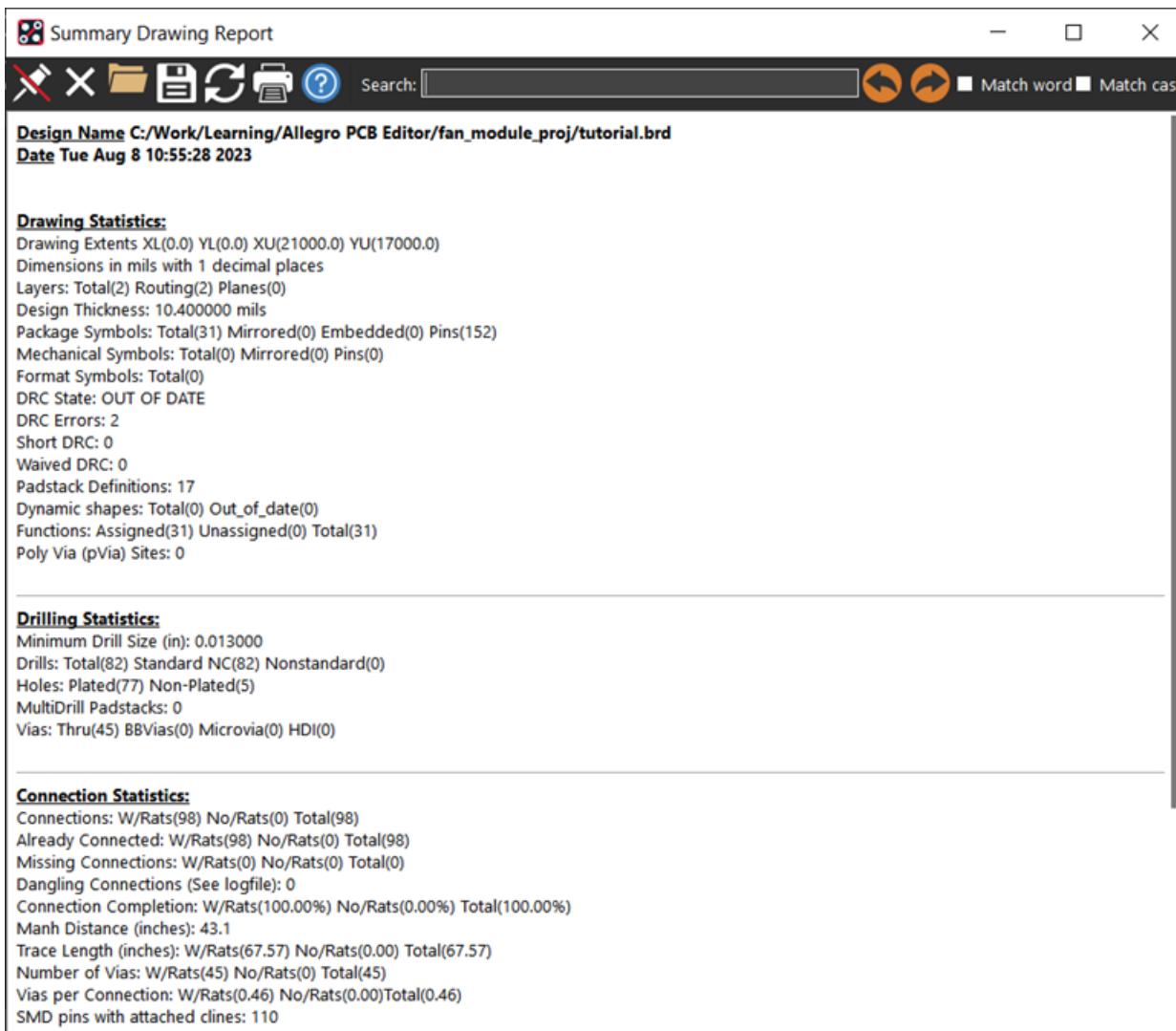
2. In the Reports dialog, choose *Summary Drawing Report* and click *Generate Reports*.



Getting Started with Allegro X PCB Editor

Validating Design

3. The report windows displays the summary of the design.



The screenshot shows the 'Summary Drawing Report' window in Allegro X PCB Editor. The window title is 'Summary Drawing Report'. The toolbar includes icons for New, Open, Save, Print, and Help, along with a search bar and two filter checkboxes: 'Match word' and 'Match case'. The main content area displays the following information:

Design Name: C:/Work/Learning/Allegro PCB Editor/fan_module_proj/tutorial.brd
Date: Tue Aug 8 10:55:28 2023

Drawing Statistics:

- Drawing Extents: XL(0.0) YL(0.0) XU(21000.0) YU(17000.0)
- Dimensions in mils with 1 decimal places
- Layers: Total(2) Routing(2) Planes(0)
- Design Thickness: 10.400000 mils
- Package Symbols: Total(31) Mirrored(0) Embedded(0) Pins(152)
- Mechanical Symbols: Total(0) Mirrored(0) Pins(0)
- Format Symbols: Total(0)
- DRC State: OUT OF DATE
- DRC Errors: 2
- Short DRC: 0
- Waived DRC: 0
- Padstack Definitions: 17
- Dynamic shapes: Total(0) Out_of_date(0)
- Functions: Assigned(31) Unassigned(0) Total(31)
- Poly Via (pVia) Sites: 0

Drilling Statistics:

- Minimum Drill Size (in): 0.013000
- Drills: Total(82) Standard NC(82) Nonstandard(0)
- Holes: Plated(77) Non-Plated(5)
- MultiDrill Padstacks: 0
- Vias: Thru(45) BBVias(0) Microvia(0) HDI(0)

Connection Statistics:

- Connections: W/Rats(98) No/Rats(0) Total(98)
- Already Connected: W/Rats(98) No/Rats(0) Total(98)
- Missing Connections: W/Rats(0) No/Rats(0) Total(0)
- Dangling Connections (See logfile): 0
- Connection Completion: W/Rats(100.00%) No/Rats(0.00%) Total(100.00%)
- Manh Distance (inches): 43.1
- Trace Length (inches): W/Rats(67.57) No/Rats(0.00) Total(67.57)
- Number of Vias: W/Rats(45) No/Rats(0) Total(45)
- Vias per Connection: W/Rats(0.46) No/Rats(0.00) Total(0.46)
- SMD pins with attached clines: 110

4. Close the *Summary Drawing Report*.
5. Double-click *Summary Drawing Report* to remove it from the list.
6. Find and select *Etch Length by Layer Report* in the *Selected Reports* section.

Getting Started with Allegro X PCB Editor

Validating Design

7. Click *Generate Reports*.

Design Name C:/Work/Learning/Allegro PCB Editor/fan_module_proj/tutorial.brd
Date Tue Aug 8 10:57:36 2023

Net Name	Layer Name	Etch Length (mils)
0	BOTTOM	1074.0
0	TOP	6901.3
3V3	BOTTOM	2899.8
3V3	TOP	1333.5
5V	TOP	4586.1
IN1	TOP	1943.9
IN2	TOP	1888.0
IN3	BOTTOM	1938.9
IN3	TOP	260.5
IN4	BOTTOM	988.7
IN4	TOP	356.8
IN5	BOTTOM	782.6
IN5	TOP	347.6
IN6	BOTTOM	713.3
IN6	TOP	335.5
IN7	BOTTOM	764.5
IN7	TOP	310.6
IN8	TOP	1355.5
IN9	TOP	905.7
IN10	TOP	774.2
IN11	BOTTOM	2138.5
IN11	TOP	72.0
IN12	BOTTOM	438.7
IN12	TOP	332.4
IN13	BOTTOM	353.9
IN13	TOP	335.5
IN14	BOTTOM	1022.5
IN14	TOP	55.0

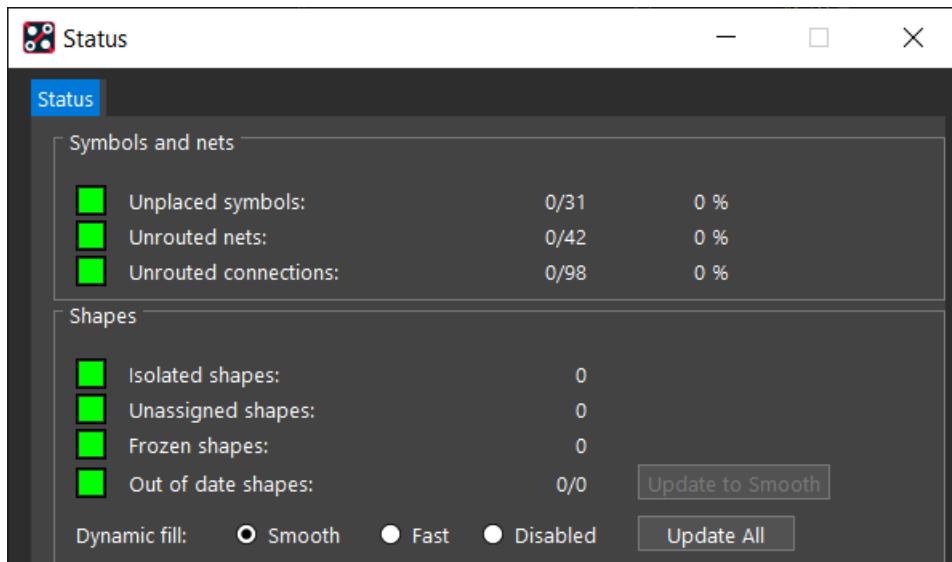
- 8. Close the *Etch Length by Layer Report*.**
- 9. Remove the *Etch Length by Layer Report* in the *Selected Reports* section.**
- 10. Repeat the process from step 6 to 9 to generate the following reports:**
 - Etch Length by Net Report
 - Etch Length by Pin Pair Report
 - Design Rules Check (DRC) Report
- 11. Click *Close* to close the *Reports* dialog box.**

Getting Started with Allegro X PCB Editor

Validating Design

12. Click *Display – Status* from the top menu to verify if all the components are placed.

The status indicators for Symbols and DRCs are turned green.



13. Close OK to close the *Status* window.

Summary

You learned how to view the design in 3D Canvas. You also learned how to generate various reports from the final design.

- **New menu commands:** *View – 3D Canvas*
- **New console commands:** `3d`
- **New window and dialog box:** Allegro 3D Canvas
- **New files created:** none

Recommended Reading

For more information, see the [Allegro PCB Editor 3D Canvas User Guide](#) and [Allegro PCB and Package Physical Layout Command Reference](#) in the documentation set.

Generating Manufacturing Output

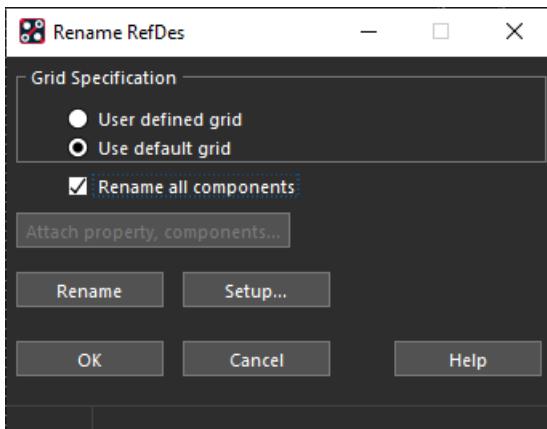
This section introduces the steps you need to perform to create output files for manufacturing.

Renaming Reference Designator

After you have completed the placement and routing you can reorder the reference designators of components on the board in a specific pattern. This steps makes the testing and assembly process easier.

1. Choose *Logic – Auto Rename RefDes – Rename* or type `rename param` in the command window.

The *Rename RefDes* dialog box opens showing grid settings and option to select all the components for renaming action.



2. In *Grid Specification* section, ensure that *Use default grid* option is enabled.
3. To rename all the components, let the *Rename all components* option selected.
4. Click the *Setup* button to specify more options.

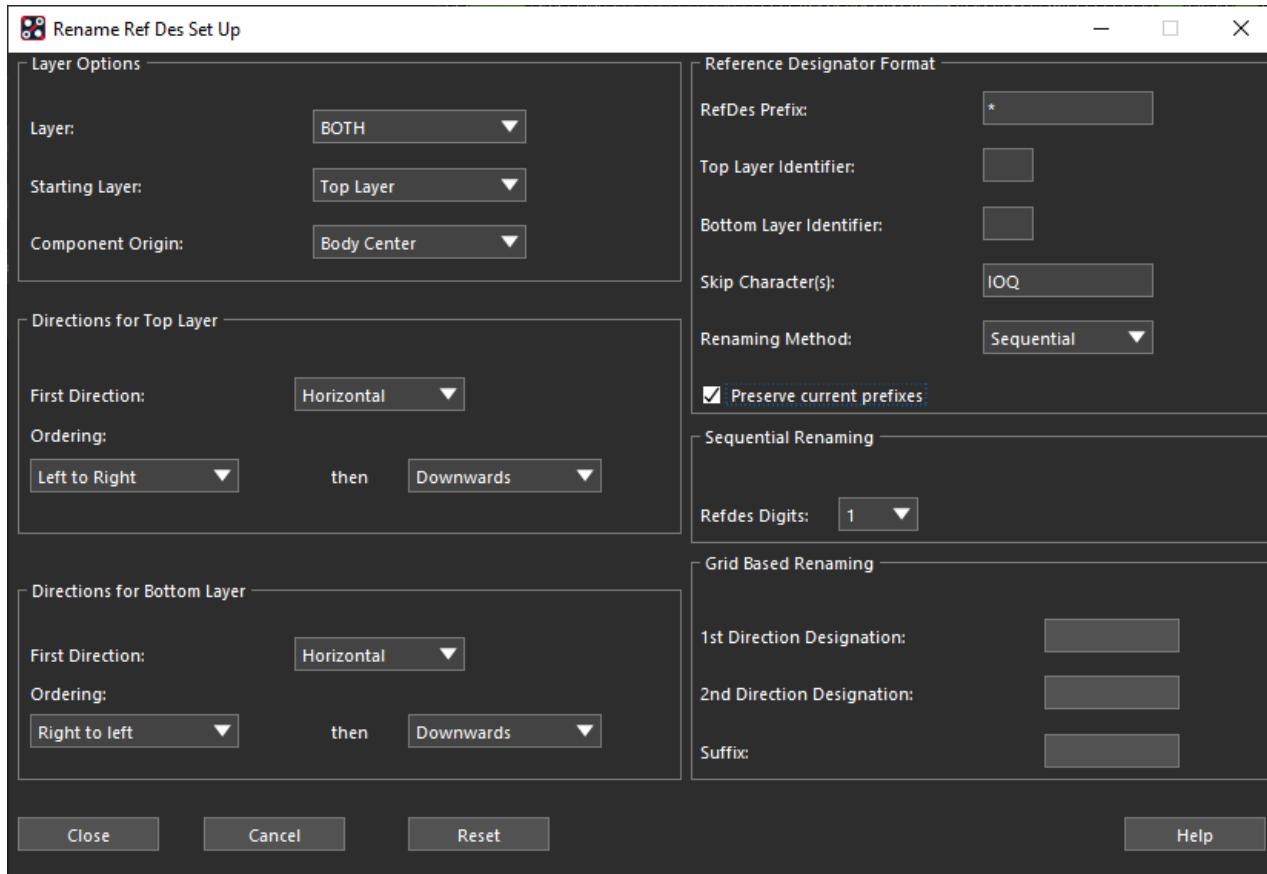
The *Rename Ref Des Set Up* dialog box opens.

5. In the *Reference Designator dialog box*, do the following:

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

- a. Remove layer identifier for TOP and BOTTOM layers.
- b. Enable the *Preserve Current prefixes* checkbox.

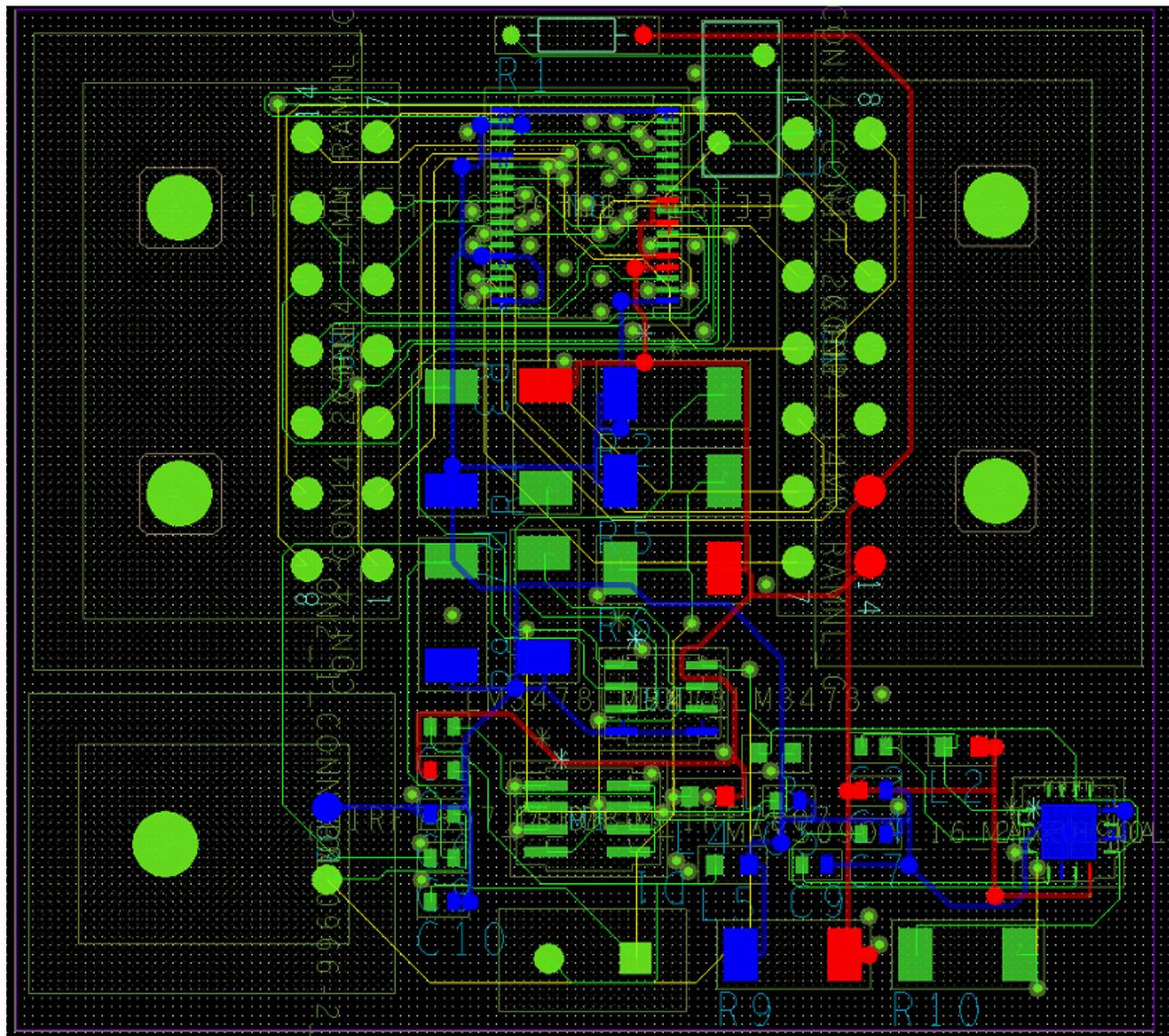


6. Close the *Rename Ref Des Set Up* dialog box.
7. Click the *Rename* button in the *Rename RefDes* dialog box.
Renaming of reference designators starts from the upper-left corner of the board in the horizontal direction and the numbers are increasing in the downward direction.
8. Click *OK* to close the *Rename RefDes* dialog box.
9. Choose *File – Save* to save the design.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

10. Choose *View – Zoom Fit* to fit the design in the design window.



Generating Silkscreen

The silkscreen layer is known as component layer, placed on the top of the board that contains component outlines, reference designators and other additional text.

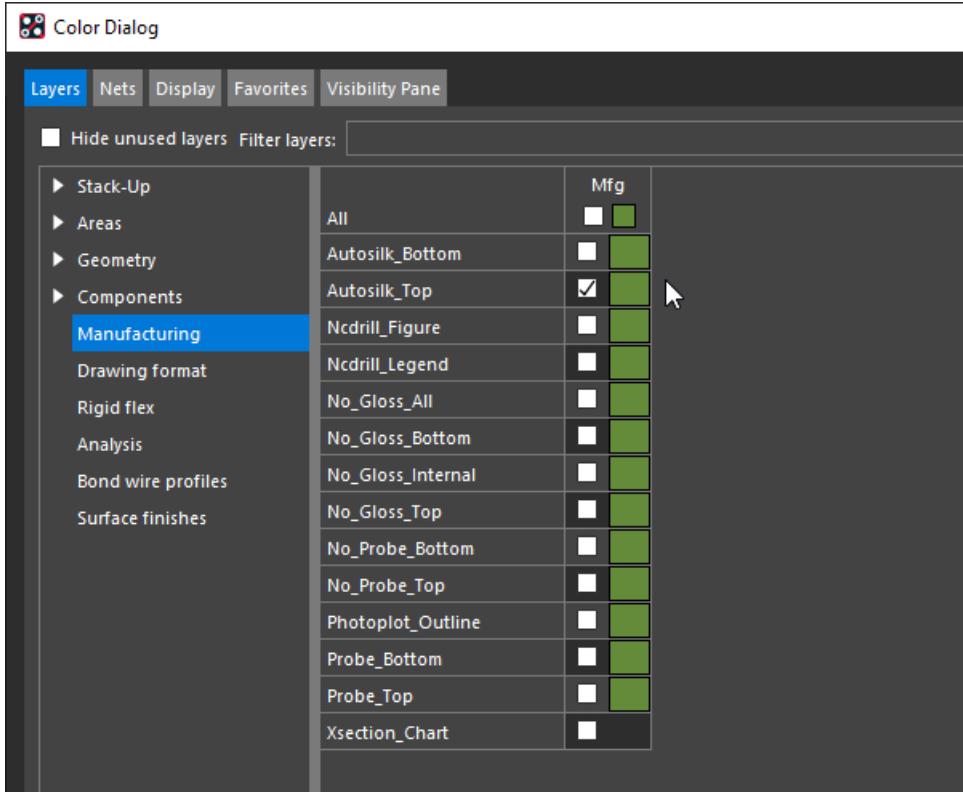
Setting visibility for silkscreen

1. To set the visibility for silkscreen, choose *Display – Color/Visibility*.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

2. In the *Color Dialog*, turn off the *Global Visibility* option.
3. In the *Layers* tab, choose *Manufacturing* folder and enable the visibility of *Autosilk_top* subclass.
4. Select white color from the *Available Colors* and apply to *Autosilk_top* subclass.



5. Expand the *Stackup* folder. Select *Conductor* and enable the visibility of the following subclasses:
 - a. Pin on Top and Bottom subclasses.

Getting Started with Allegro X PCB Editor

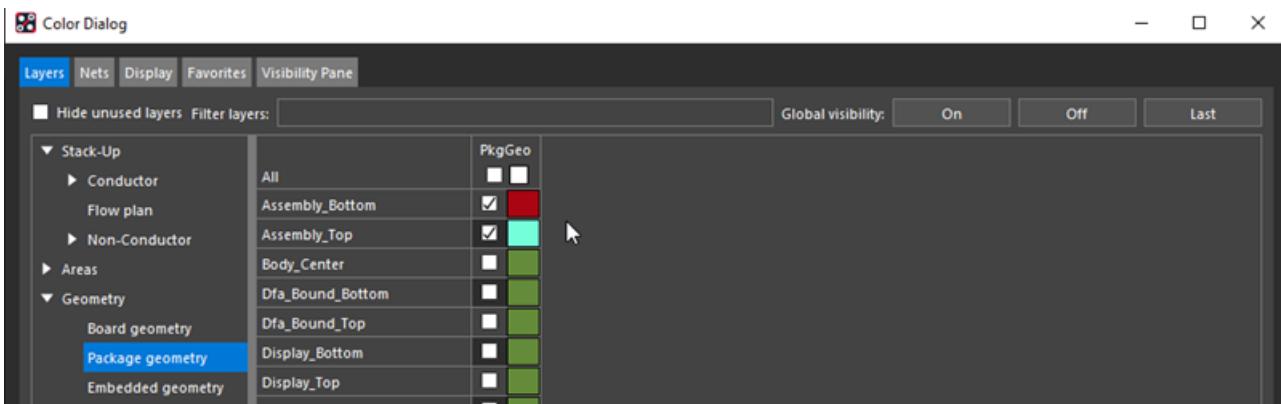
Generating Manufacturing Output

b. Via on Top subclass.



6. Expand *Geometry* folder and select *Package Geometry*.

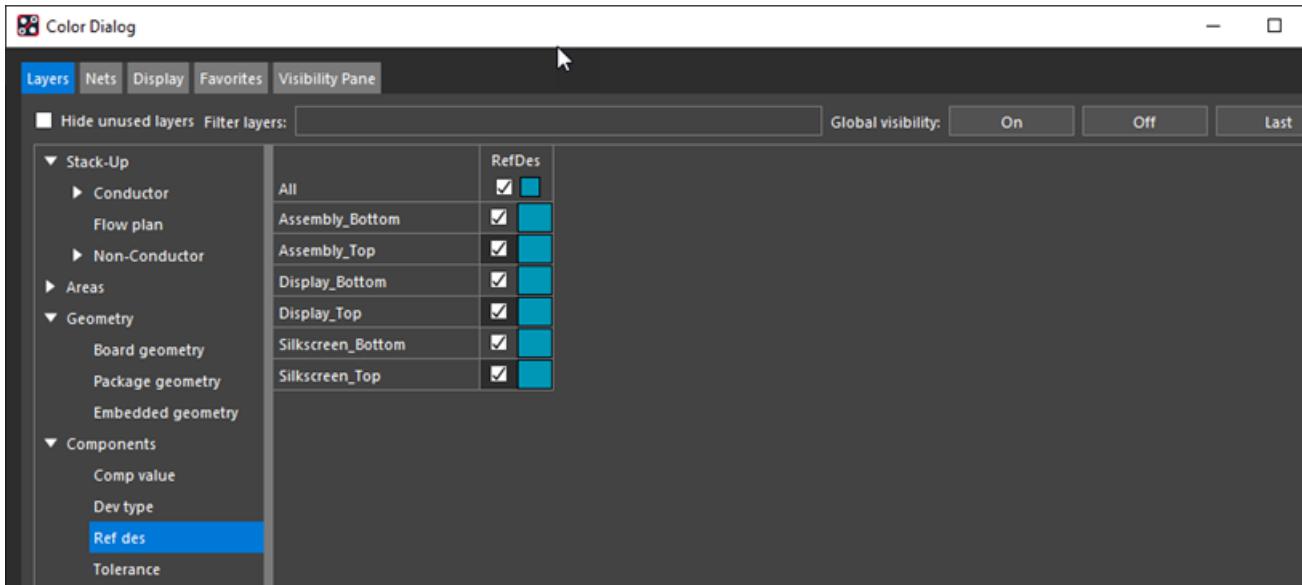
7. Enable visibility for Assembly_Top and Assembly_Bottom subclasses.



Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

8. Expand *Components* folder. Select *Ref des* and enable the visibility of all the subclasses.

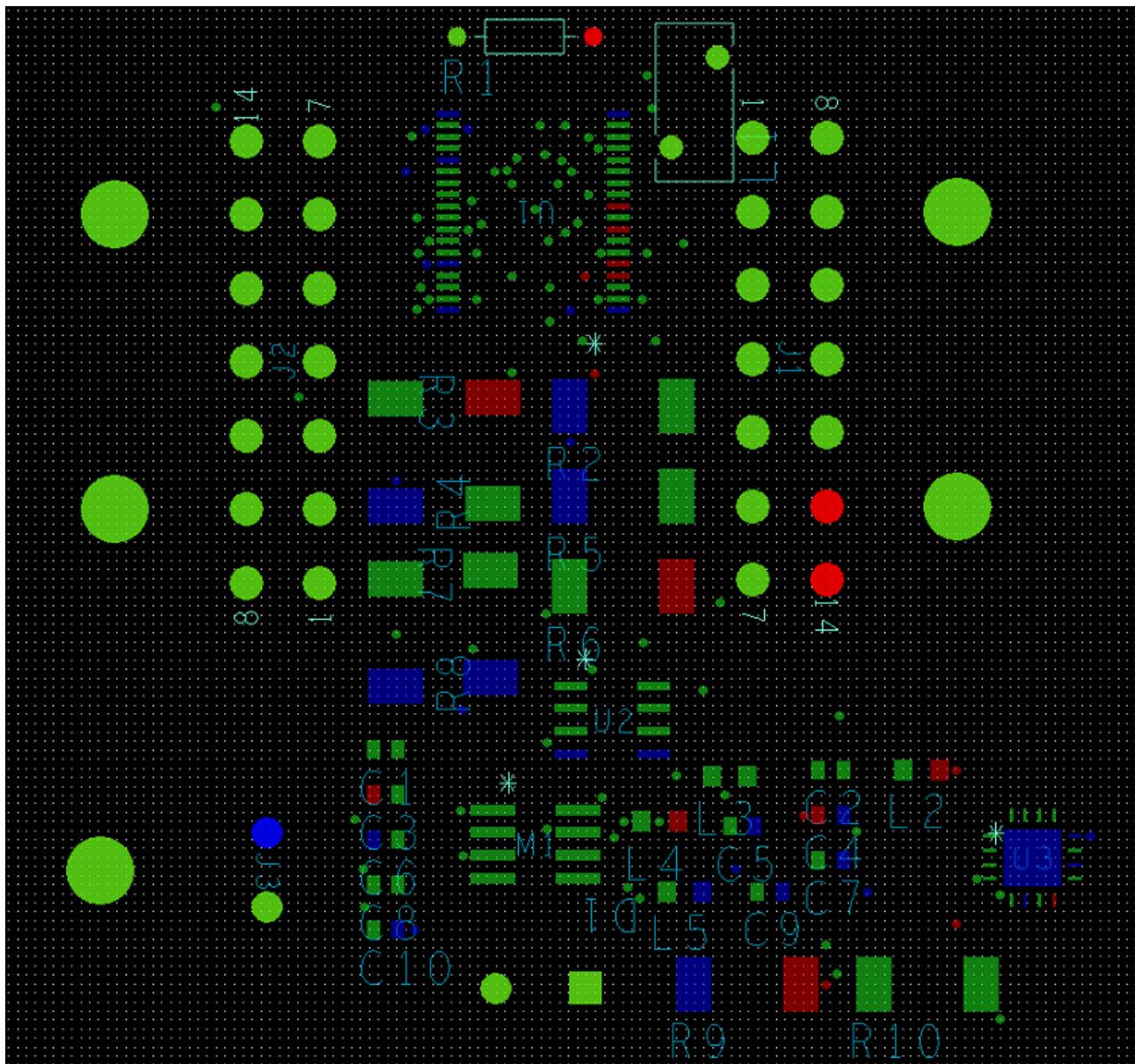


9. Click *Apply* to apply the visibility settings.
10. Click *OK* to close the *Color Dialog*.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

11. Choose *View – Zoom Fit* from the top menu.



Generating Silkscreen

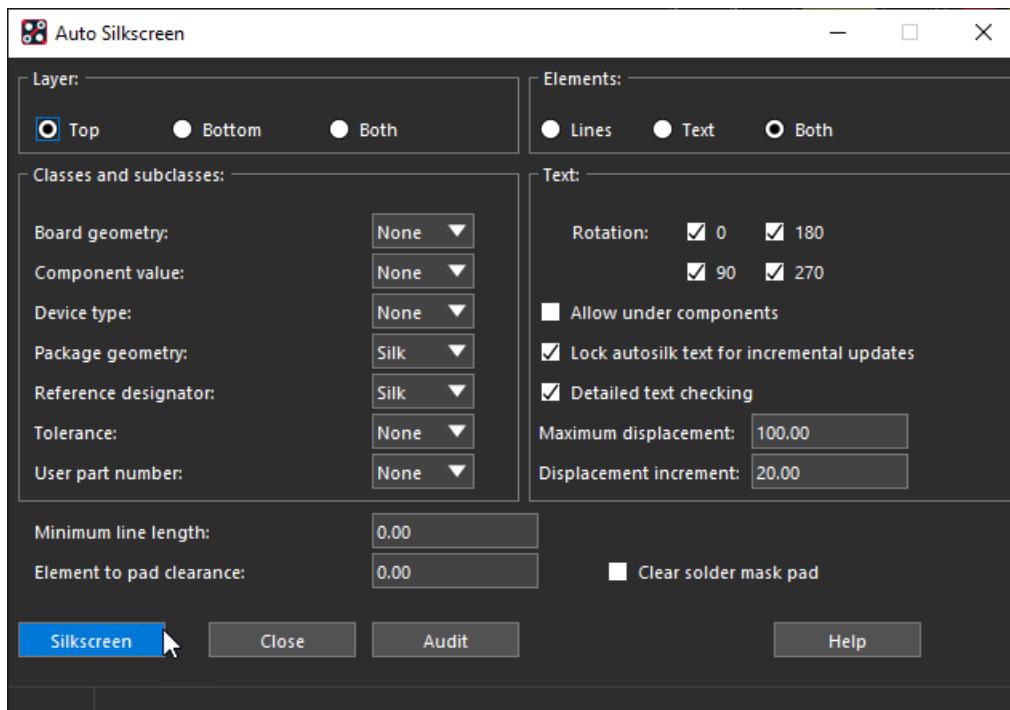
1. Choose *Manufacture – Silkscreen*.
2. In the Auto Silkscreen dialog box, make the following changes:
 - c. In *Classes and Subclasses section*, set subclass to *None* for all the classes except *Package geometry* and *Reference designator*.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

The *Package geometry* and *Reference designator* classes are copied to Autosilk subclass.

- d. Disable *Allow under components* checkbox.
- e. Enable *Lock autosilk text for incremental updates* checkbox.
- f. Specify *Displacement increment* to 20 mils.

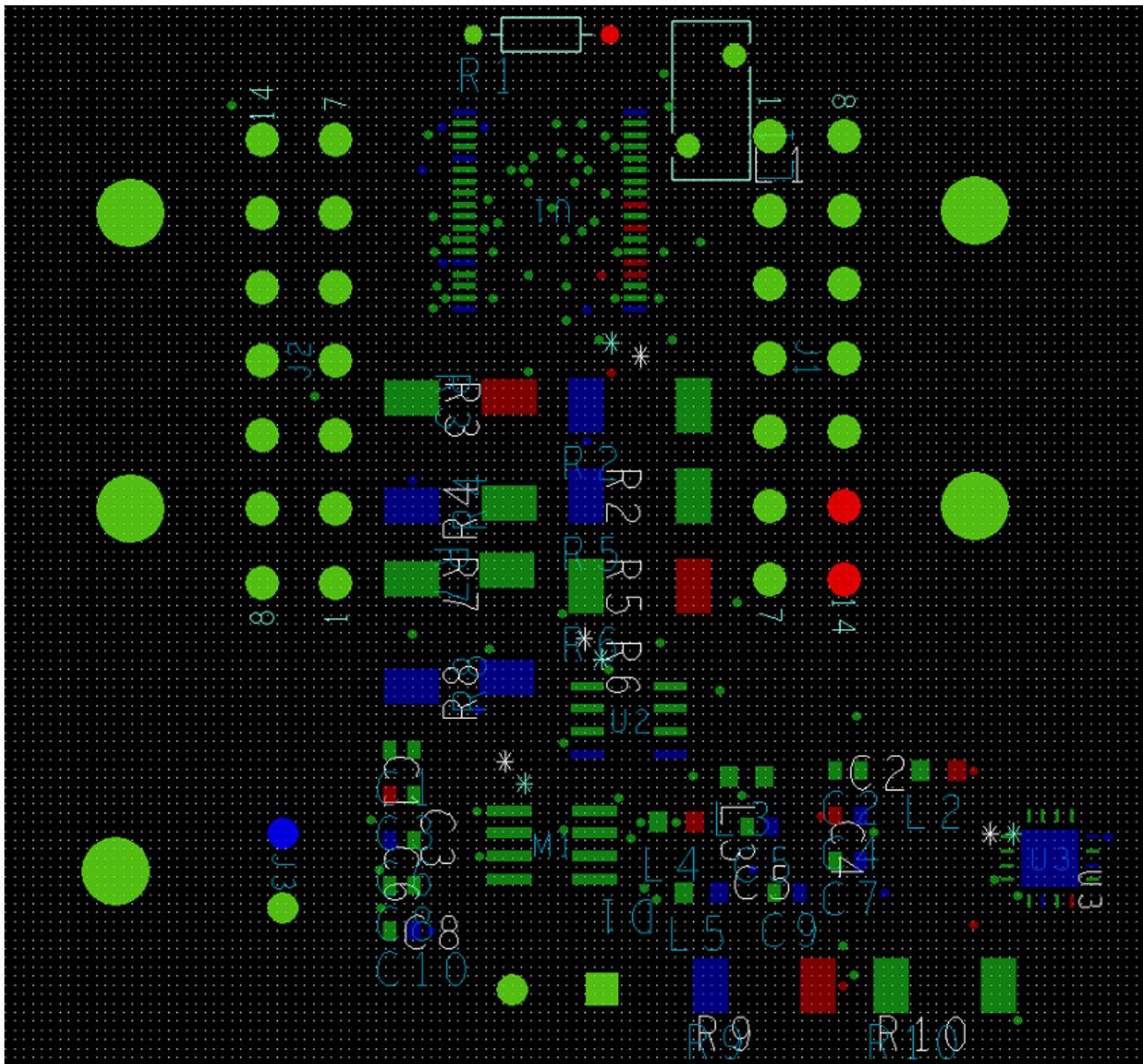


3. Click *Silkscreen*.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

The automatic silkscreen process starts and silkscreen reference designator are placed.

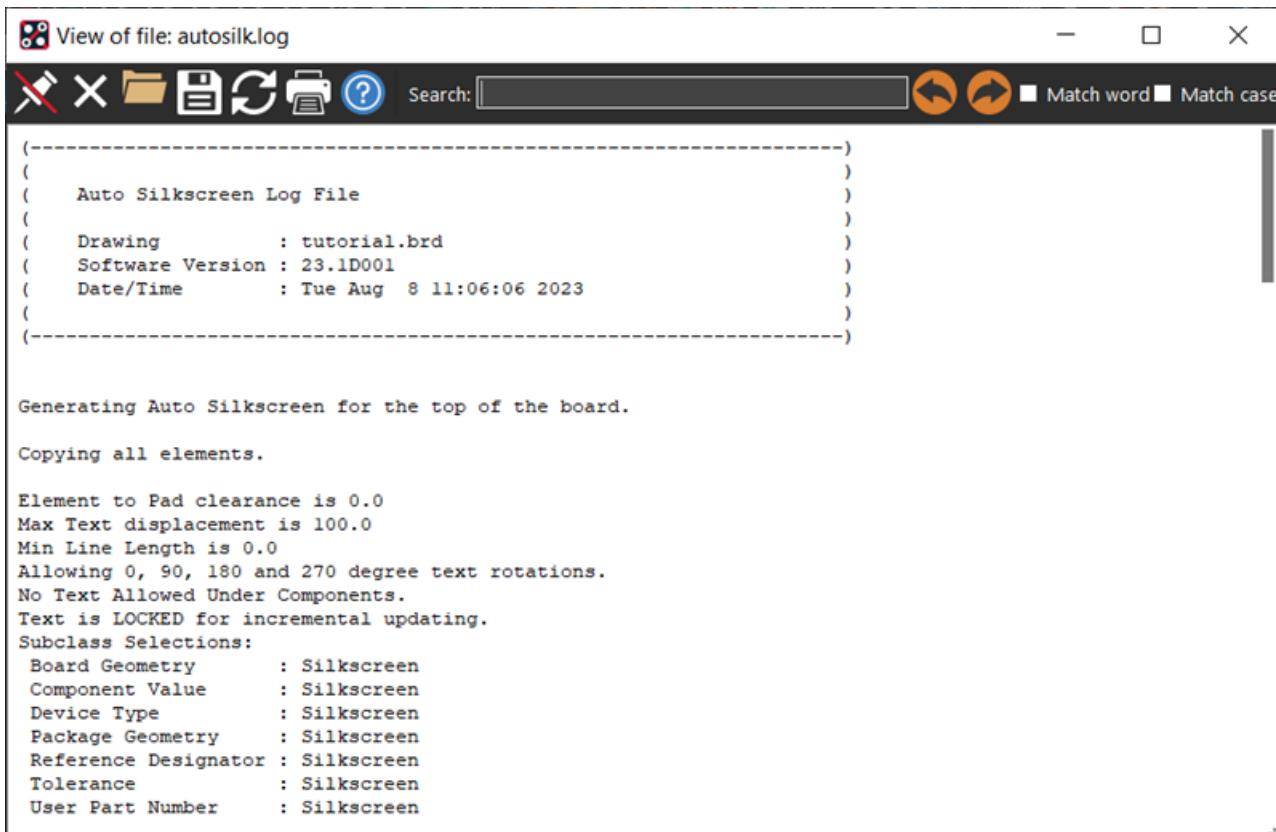


4. Click *File – Viewlog*.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

The `autosilk.log` is opened in a window and shows the silkscreen results.



The screenshot shows a text editor window titled "View of file: autosilk.log". The window contains the following log file content:

```
(-----)
(
( Auto Silkscreen Log File
(
( Drawing      : tutorial.brd
( Software Version : 23.1D001
( Date/Time    : Tue Aug  8 11:06:06 2023
(
(-----)

Generating Auto Silkscreen for the top of the board.

Copying all elements.

Element to Pad clearance is 0.0
Max Text displacement is 100.0
Min Line Length is 0.0
Allowing 0, 90, 180 and 270 degree text rotations.
No Text Allowed Under Components.
Text is LOCKED for incremental updating.
Subclass Selections:
Board Geometry      : Silkscreen
Component Value     : Silkscreen
Device Type         : Silkscreen
Package Geometry    : Silkscreen
Reference Designator : Silkscreen
Tolerance           : Silkscreen
User Part Number    : Silkscreen
```

5. Close the logfile.

Generating Manufacturing Files

The final task is to generate various types of output files of the physical design data. You can create Gerber files, Excellon NC Drill files, DXF files, IPC2581, ODB++, and printer/plotter files. These files are standard files and are required by the fabrication houses to manufacture a PCB.

For this tutorial, create three types of output files:

- Artwork (Gerber)
- NC Drill
- IPC2581

Creating Artwork

To create artwork files, PCB Editor reads film control records to determine the number of artwork files to produce, their names, and list of classes and subclasses to include in each artwork file.

To specify classes and subclasses for an artwork file, use Color Dialog to set the visibility of required classes and subclasses.

1. Choose *Display – Color/Visibility*.

The Color Dialog opens.

2. In the *Layers* tab, click the *Off* button for *Global Visibility*.

The visibility of all the classes and subclass are turned off.

3. In the *Stack-Up* folder, select *Soldermask_Top* and *Pastemask_Top* layers and enable the checkbox for *Pin* only.

The soldermask and pastemask layers of pins becomes visible in the design canvas.

4. Similarly, in the *Geometry* folder, select *Soldermask_Top* and *Pastemask_Top* layers and enable the checkbox for *All* objects.

The visibility of soldermask and pastemask layer is set on both board and package geometry.

5. Click *OK* to close the Color Dialog.

6. Choose *Manufacture – Artwork*.

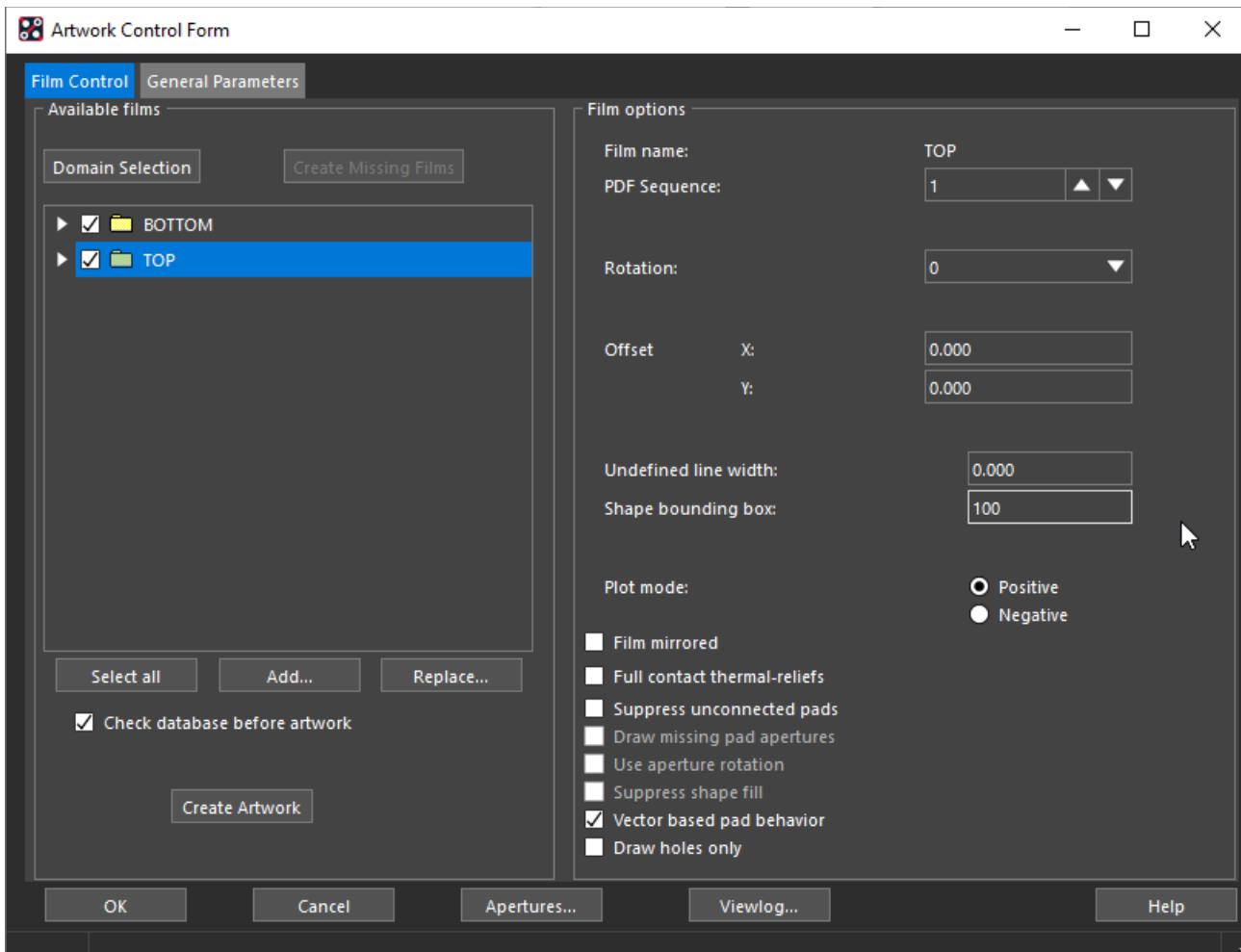
The *Artwork Control* dialog box opens which reads the cross-section and auto-generates one film record for each etch subclass and includes etch, pins, and vias.

7. In *Artwork Control* dialog box, select both the TOP and BOTTOM layers.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

8. Click *Create Artwork* to generate artwork.



Two artwork files (`TOP.art` and `BOTTOM.art`) are created in your working directory.

9. Click *Viewlog* to review the `photoplot.log` file.
10. Click *OK* to close the *Artwork Control* dialog box.

Creating NC Drill

NC Drill output files are created for numerically-controlled (NC) drills and router and helps in assessing the cost of PCB manufacturing. The drill output files includes drill legend tables and drill files.

Generating Drill Legend

Drill legend tables are used in fabrication drawing and shows the number, type, and tolerance of plated and non-plated holes in the design.

1. Choose *Display – Color/Visibility*, click *On* to enable *Global Visibility* and close the dialog box.

2. Choose *Manufacture – NC – Drill Legend*.

The *Drill Legend* dialog box opens.

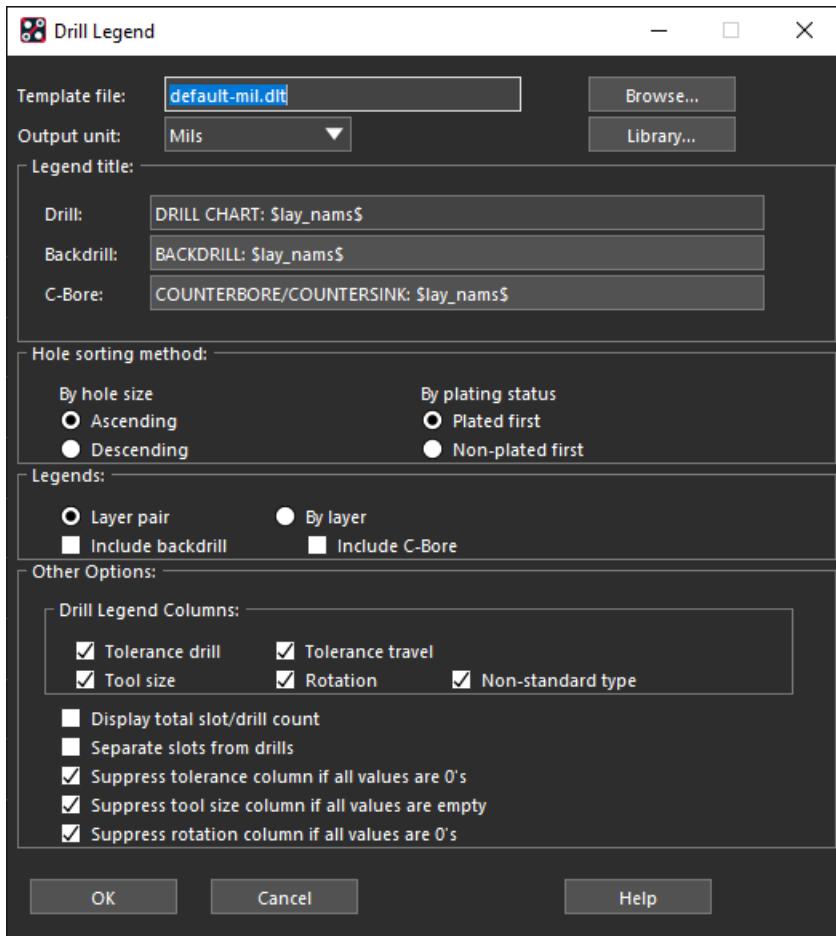
3. Click *OK* to generate the drill legend symbol.

The drill legend symbol gets attached to the cursor.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

4. Left-click to place the drill legend in the design canvas.



DRILL CHART - TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED SIZE	DRILLED SIZE	PLATED	QTY
.....	.13.0	-	PLATED	57
.	.14.0	-	PLATED	2
.	.15.0	-	PLATED	2
.	.18.0	-	PLATED	28
,	.152.0	-	NON-PLATED	1
,	.154.0	-	NON-PLATED	4

Generating NC Drill

NC drill file is created based on the parameters specified for the drill coordinate data format.

1. Choose *Manufacture – NC – NC Drill*.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

The *NC Drill* dialog box opens.

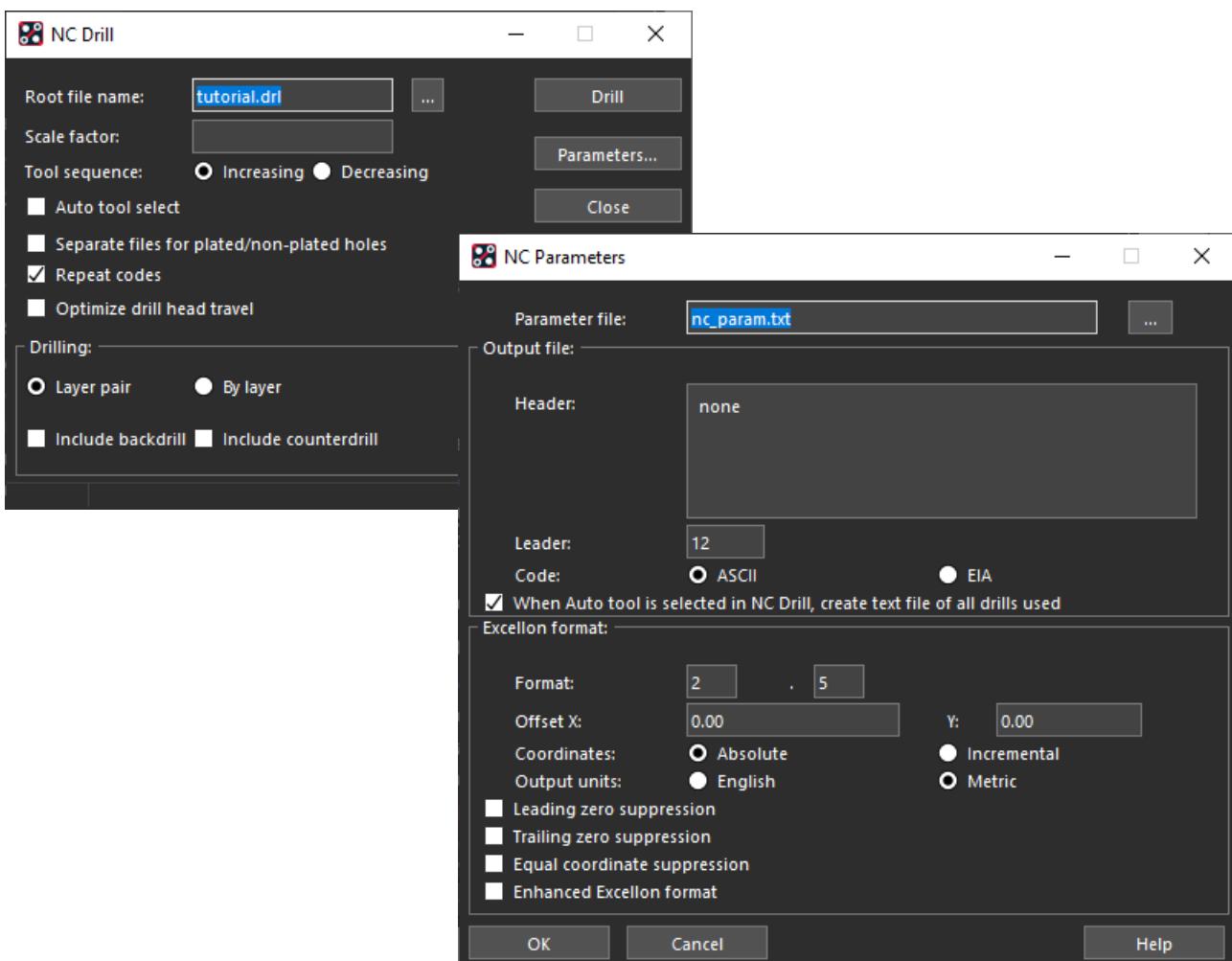
2. Click *Parameters* to open *NC Parameters* dialog box.

3. Enable the *Enhanced Excellon format* checkbox.

A header in the NC Drill and NC Route output files is generated that uses Excellon commands.

4. Click *OK* to save the parameters.

5. Click *Drill* to generate the drill file.



The NC Drill file (`tutorial.drl`) is created in your working directory.

6. Click *View/log* to review the log file.

7. Click *Close* to close the dialog box.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

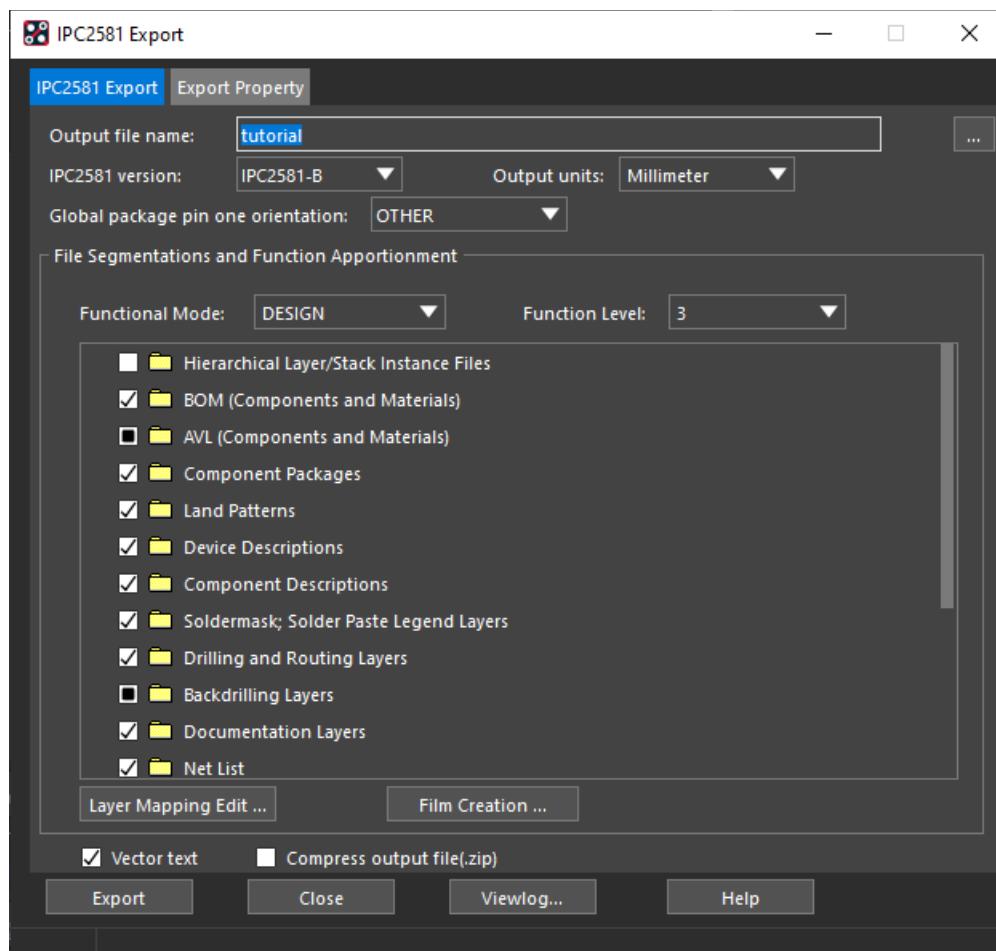
Creating IPC2581 Files

IPC2581 is an XML-based data exchange format used for providing physical design data for fabrication and assembly of PCBs.

For this tutorial, create IPC2581 output using default values.

1. Choose *File – Export – IPC2581*.

The *IPC2581 Export* dialog box opens.



2. Leave the *IPC2581 version* to default, which is set to the latest version *IPC2581-B*.
3. Select *Output units* to Millimeter.
4. Set the *Functional Mode* to DESIGN and *Function Level* to 3.

Five functional modes are supported and each mode consists of three levels that define the complexity and detail of the output file.

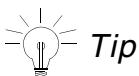
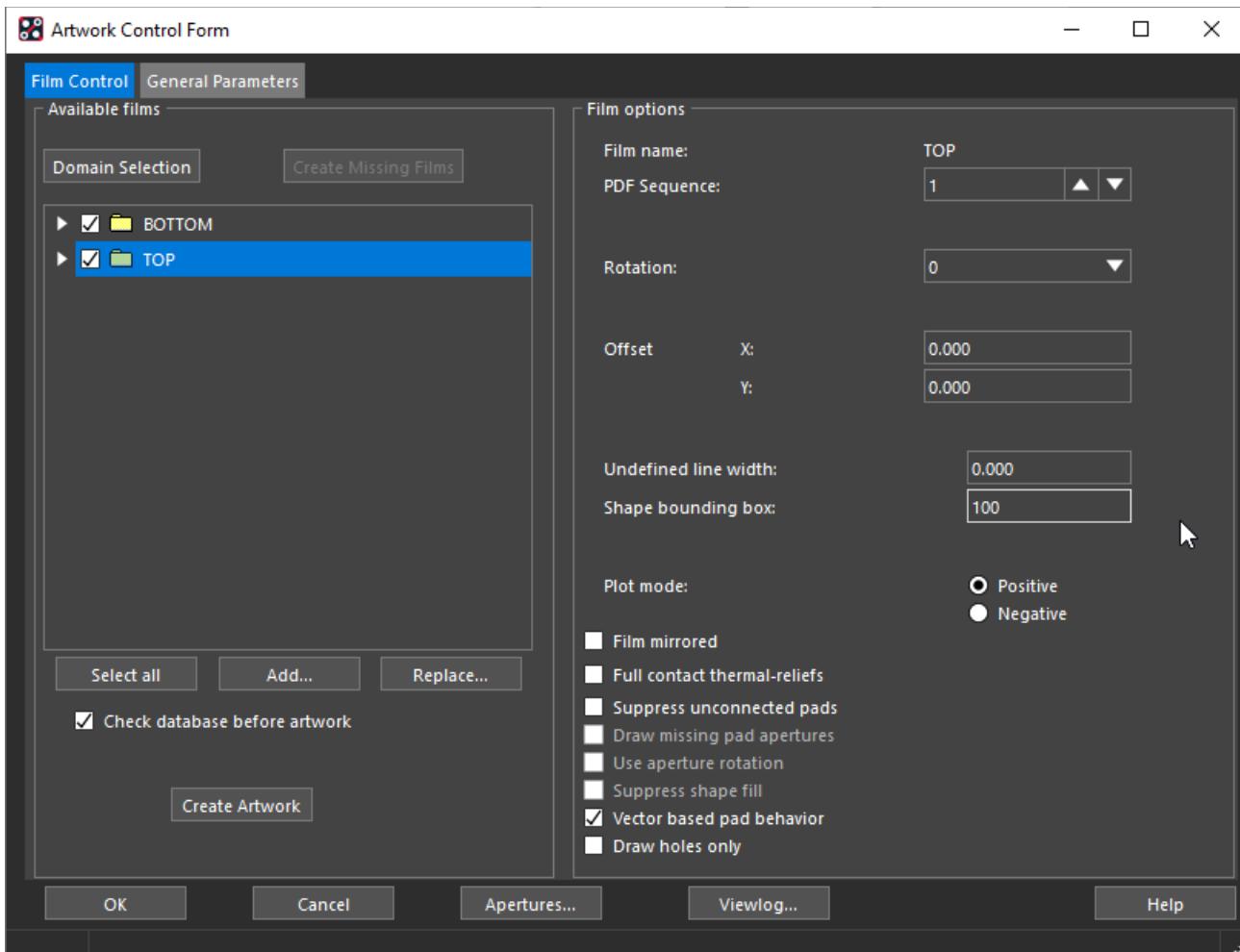
Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

5. Click *Film Creation* to add class and subclass for film records.

The *Artwork Control* dialog box opens.

6. Select both the TOP and BOTTOM layers and click *OK* to close the dialog box.



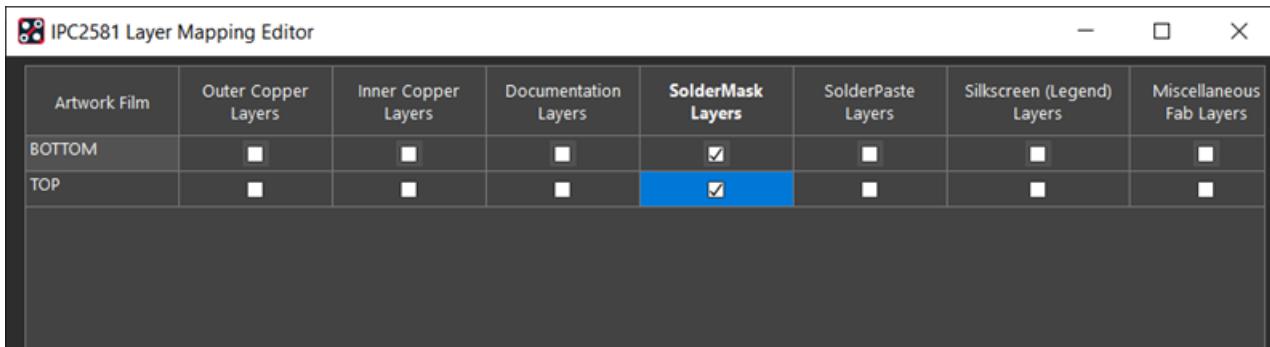
When exporting IPC2581, it is recommended to enable *Dynamic unused pads suppression* option in Cross-section Editor to suppresses unconnected pads for the selected object types (pin/via) on the selected inner layers.

7. Click *Layer Mapping Editor* to specify layer type for each artwork film.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output

8. Select the checkboxes for *Soldermask* and *SolderPaste Layers* for both the artwork films and click *OK* to close the dialog box.



9. To generate IPC2581 file, click *Export*.

An XML file (`tutorial.xml`) is created in your working directory.

10. Click *Viewlog* to review the log file.

You have completed the task of creating a board design and generating manufacturing files for the PCB of fan module circuit.

Summary

You learned how to prepare the design for post-processing and how to create artwork files. You also learned how to generate drill files and IPC2581 data for sharing with manufacturers.

- **New menu commands:** *Logic – Auto Rename RefDes – Rename, Manufacture – Silkscreen, Manufacture – Artwork, Manufacture – NC – Drill Legend, Manufacture – NC – NC Drill, File – Export – IPC2581*
- **New console commands:** `rename param`, `silkscreen param`, `artwork`, `ncdrill legend`, `nctape_full`, `ncdrill param`, `ipc2581 out`
- **New window and dialog box:** *Rename RefDes, Auto Silkscreen, Artwork Control dialog box, Drill Legend, NC Drill, NC Parameters, IPC2581 Export*
- **New files created:** `autosilk.log`, `TOP.art`, `BOTTOM.art`, `photoplot.log`, `tutorial.drl`, `tutorial.xml`

Recommended Reading

For more information, see the [Allegro User Guide: Preparing Manufacturing Data](#) and [Allegro PCB and Package Physical Layout Command Reference](#) in the documentation set.

Getting Started with Allegro X PCB Editor

Generating Manufacturing Output
