cadence™

Allegro®
Design Entry HDL Tutorial

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Contents

1

Introduction to Design Entry HDL Tutorial

This chapter contains the following information:

Overview

This tutorial demonstrates the major tasks involved in creating a schematic. Design Entry HDL is the tool used for Design Entry (also known as Design Capture) in the printed circuit board (PCB) design flow. With Design Entry HDL, you can create a project, place components (parts), connect parts, name signals, add ports, and save designs.

When you save a design, Design Entry HDL checks for errors and helps you locate the areas on the schematic where connectivity errors have occurred.

Design Entry HDL comprises two menu use models—post-select and pre-select. In the post-select use model, you first select the command and then select the schematic component. In the pre-select use model, the schematic component is selected first and then the command.

For example, you want to delete a schematic component. The steps in the post-select use model are:

- Choose *Edit – Delete*.
- Select the component to be deleted.

In the pre-select use model, the steps are:

- Choose the component to delete.
- Choose *Edit – Delete*.

By default, Design Entry HDL supports the post-select model for schematic operations. This tutorial is in the post-select mode. To know about the pre-select mode, see Setting the Pre-Select Use Model on page 30.

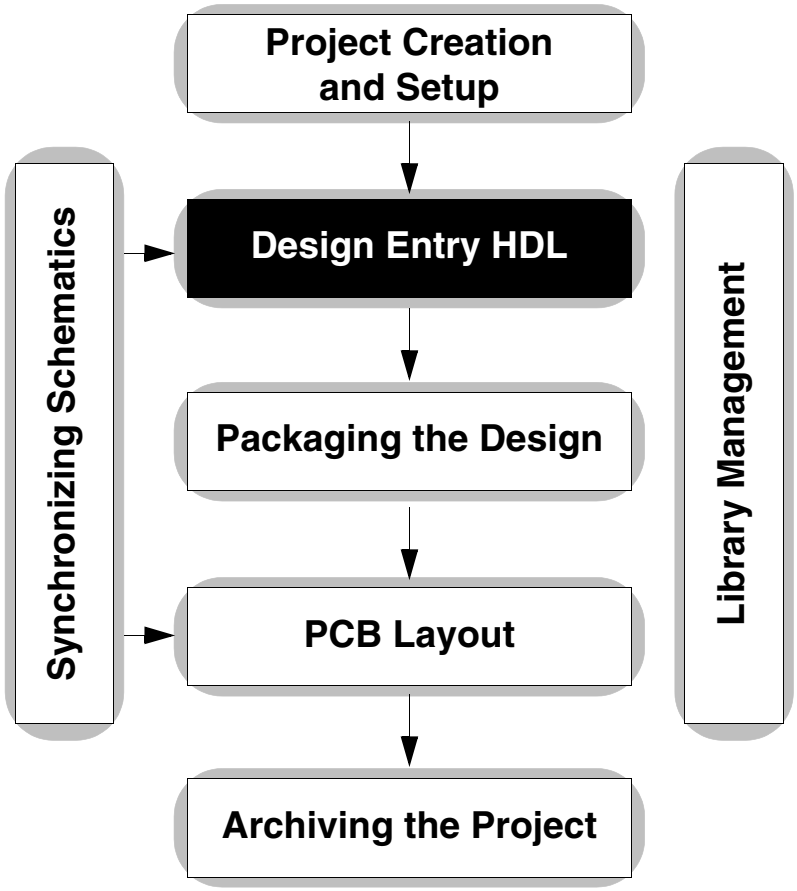
Important

It is important that you follow the steps in this tutorial in a sequential order.

Design Entry HDL in the PCB Flow

This tutorial explains how to create a schematic design by using Design Entry HDL. Design Entry HDL helps you capture the design of a PCB in a schematic form. This design is packaged and opened in Allegro PCB Editor to place and route your board-level design.

The completed board design is then sent to manufacturing for the production of the printed circuit board. The following figure illustrates the overall design flow for printed circuit boards and highlights the space where Design Entry HDL fits in:



How To Use this Tutorial

This tutorial provides a hands-on exercise in creating a design using Design Entry HDL. To understand how you can use Design Entry HDL to create designs, you should follow the steps in the sequence in which they appear in the chapters of this tutorial.

Important

The Design Entry tutorial is written in the flow in which a schematic is usually created. Follow the steps in the tutorial in the order in which they are covered. This way, you easily assimilate the methods for creating a schematic. You should complete the tutorial in one session, which will require approximately eight hours of effort. If you plan to complete the tutorial across days, then complete at least one chapter in each session.

Before using the tutorial, ensure that you do the following:

- Unzip the file *local_lib.zip* and save it locally.
- Ensure that this work area where you extract the samples is a local directory for which you have write permissions.
- The `local_lib` library, which is a directory, contains the parts that you will use while creating a schematic using this tutorial.
- For the commands specified in the tutorial, you need to replace your work area with the name of the local directory in which you have copied the samples.
- Ensure that you unset the CDS_SITE environment variable on your computer if it is set.

Brief Outline of Chapters

The Design Entry HDL Tutorial is divided into four chapters:

- Creating a Project on page 11

  This chapter contains procedures to create and set up a project. It also, in brief, explains libraries, the `cds.lib` file, and the project file.

- Creating a Schematic: Basics on page 27

  This chapter explains the basic tasks involved in creating a simple multi-page schematic. The tasks covered include adding parts, connecting parts, saving and checking the design, creating buses, tapping buses, and adding physical information.

- Creating a Schematic: Advanced on page 93

  This chapter explains the advanced tasks you perform while creating hierarchical designs. It explains the two methods that may be followed for creating a hierarchical design. This is followed by procedures to create a hierarchical design using the top-down and the bottom-up methods. The chapter also explains the method to package the design. If errors are detected while packaging, *Global Find* is used to locate the components. To edit the properties attached to components, the Attributes dialog is used. After you have fixed the errors, the design must be re-packaged.

- Enhancing the Schematic on page 75

  This chapter explains how you can enhance a schematic. It explains how you can work in the Windows mode to edit the schematic. This chapter also explains how you can use different fonts and color to enhance your design schematic.

2

Creating a Project

This chapter contains the following information:

Important

Remember to follow the steps in this tutorial in a sequential order.

Overview

The first task you perform in designing a PCB is creating a project. A design project includes paths to libraries, part tables, tool settings, global settings, view directory names, and other related settings for designing a PCB to required specifications.

A design project consists of the following:

- Reference libraries
- Local libraries (design libraries)
- `cds.lib` file
- Project file (`.cpm` file)

Reference Libraries

Design Entry HDL references all parts in a schematic from various libraries that are located in the reference or local area. These libraries are called reference libraries. For example, the `standard` library is a reference library. For more information on libraries, see the Understanding Libraries section in *Allegro® Front-to-Back User Guide*.

The cds.lib File

When you create a project, Project Manager creates a *cds.lib* file. The *cds.lib* contains:

- A directive to include the installed Cadence libraries. (For example: `INCLUDE <your_install_dir>/share/cdssetup/cds.lib`)
- A define statement that maps the logical project library (projectname_lib) to its physical name (worklib). (For example: `DEFINE myproject_lib worklib`)

The contents of a typical *cds.lib* file are as follows:

```
DEFINE 54alsttl ../../library/54alsttl
DEFINE 54fact ../../library/54fact
DEFINE tutorial_lib worklib
INCLUDE $CONCEPT_INST_DIR/share/cdssetup/cds.lib
DEFINE local_lib local_lib
```

Creating a Project

When you create a new project, Allegro Project Manager creates a project file called `<projectname>.cpm` in the project directory. For more information on project files and directives you can set in project files, see *Allegro Front-End CPM Directives Reference Guide*. To create a project, you use Project Manager.

1. To start Project Manager, choose *Start – Programs – Cadence – Release 17.2 – Project Manager*.

2. Select *Allegro Design Entry HDL XL (Concept HDL Expert)*.

Project Manager appears.

In this chapter, you will create a new project called `se_demo`.

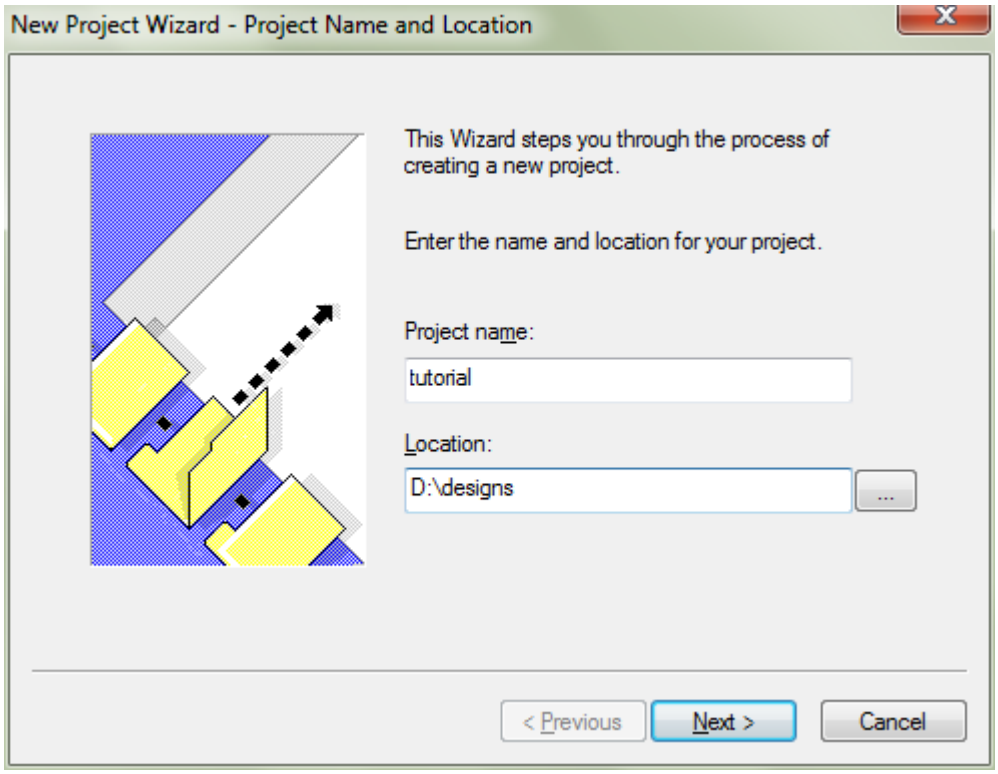
3. To start creating the project, click *Create Design Project*.

   The New Project Wizard appears. In the first step of the wizard, specify the project name and the location where the project files should be created.

4. Enter the project name as `tutorial`.

5. Enter the location as `D:\designs`.

If a directory named *designs* does not exist, Project Manager creates it for you. You can also use the browse button to specify the location of the project.



6. Click *Next*.

The New Project Wizard - Project Libraries page appears.

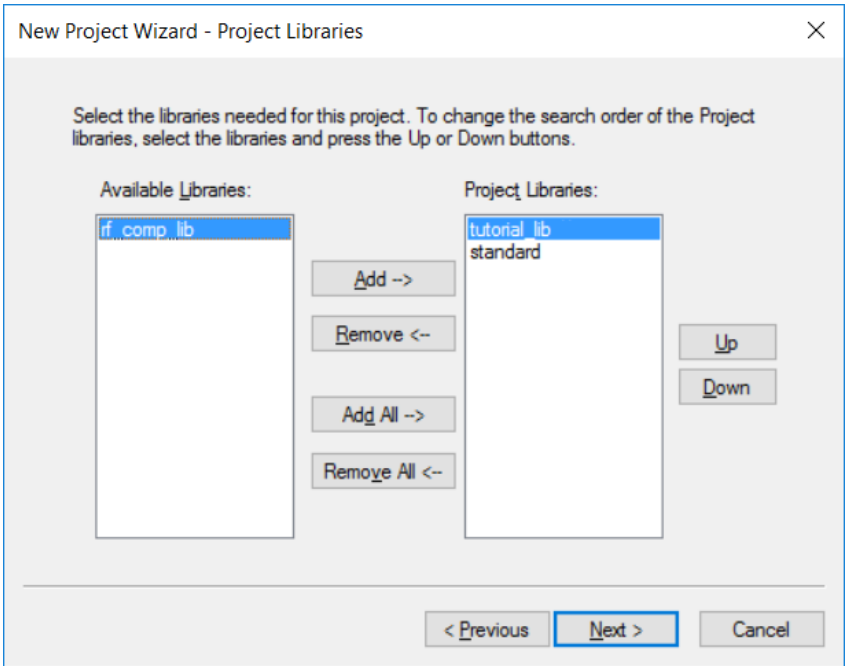


Figure 2-1 New Project Wizard - Project Libraries

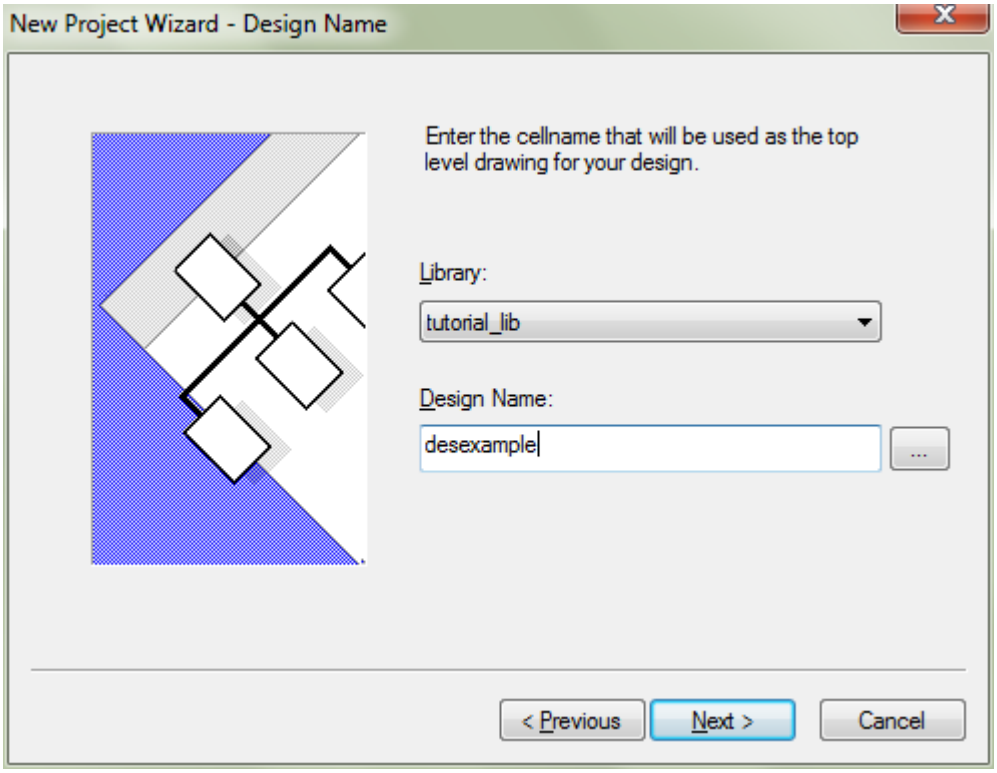
The *Project Libraries* page allows you to select the libraries for your project from a list of available libraries. By default, the `standard` and `tutorial_lib` (`<project_name>_lib`) libraries are added to the Project Libraries list. This is the logical library name. After the project is created, the physical name of this library will be `worklib`. The `cds.lib` file defines `tutorial_lib` as `worklib`.

Note: All the libraries listed in the New Project Wizard - Project Libraries figure on page 16 are available to you only if you install the Cadence Libraries CD. To add other libraries to the Available Libraries list, you can edit the `cds.lib` file. For more information, see Adding Libraries Using Project Setup on page 20.

7. Click *Next*.

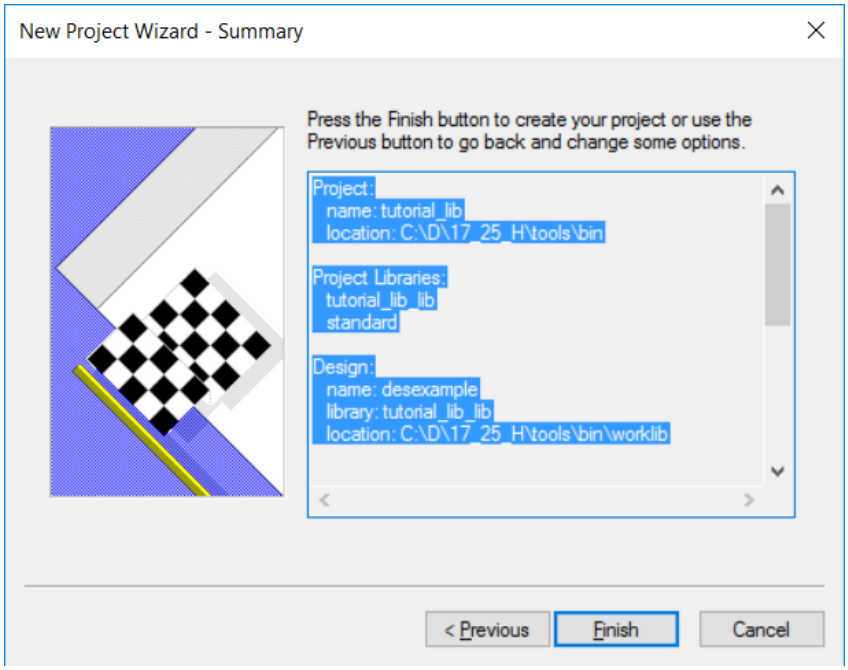
The Design Name page appears. The default design library is *tutorial_lib*. The top-level design will be placed under the `tutorial_lib` library.

8. Type `desexample` as the top-level design name. The name must be in lowercase letters.



9. Click *Next*.

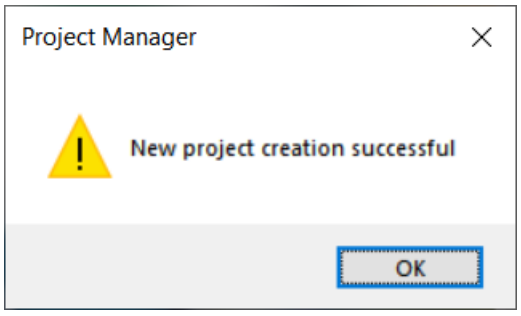
The Summary page appears.



To modify the details, click *Previous* to go back to the previous steps.

10. Click *Finish*.

A message confirms the new project creation.



11. Click *OK*.

Project Manager creates the project and displays the board design flow.

Video

See the multimedia demonstration titled *Creating a Project* for an example of the design project creation.

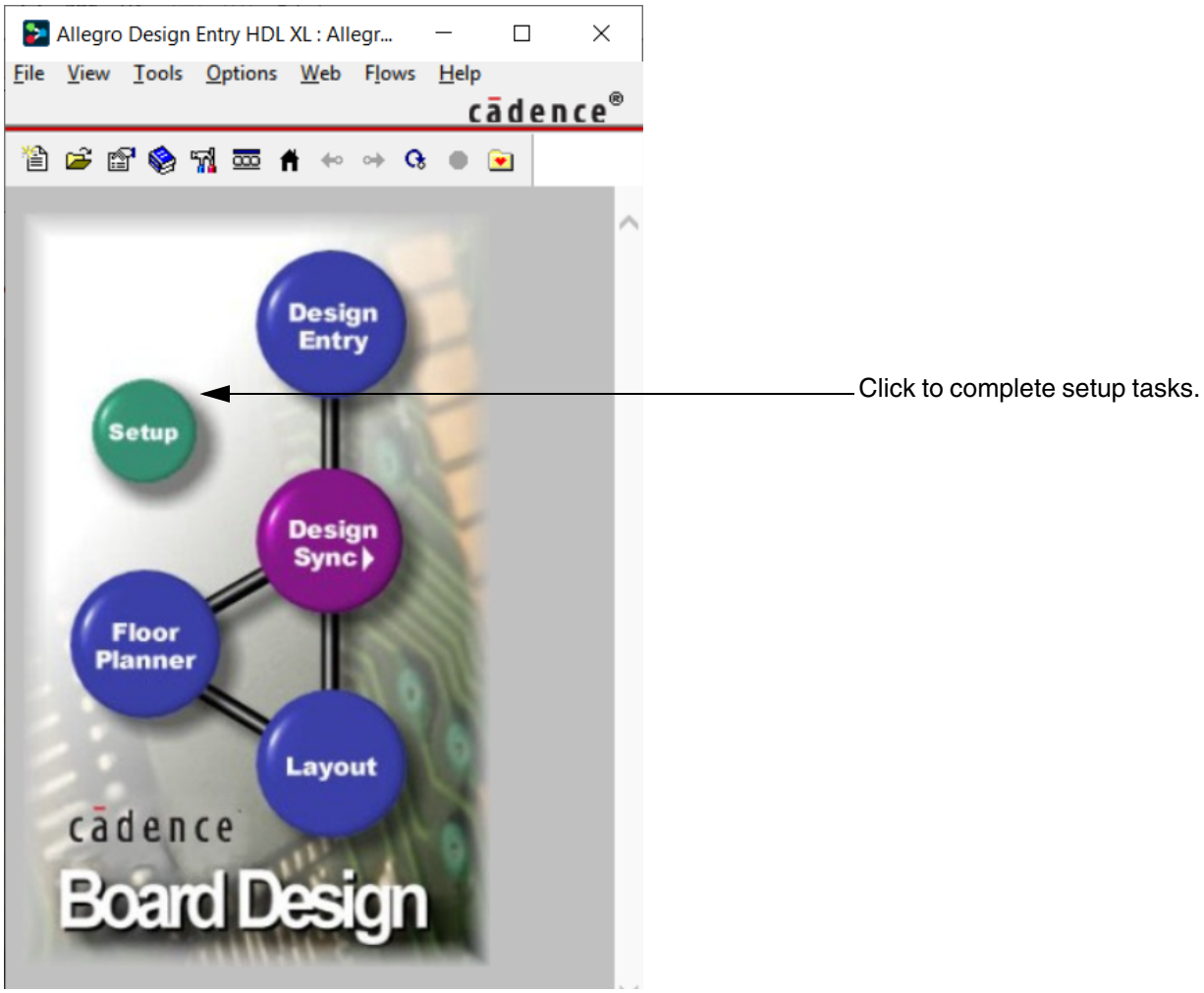
Adding Libraries Using Project Setup

After you have created a project using the New Project Wizard, you can make changes, such as adding new libraries and cells, to the project. In this section, you will add the `local_lib` library to the list of Project Libraries.

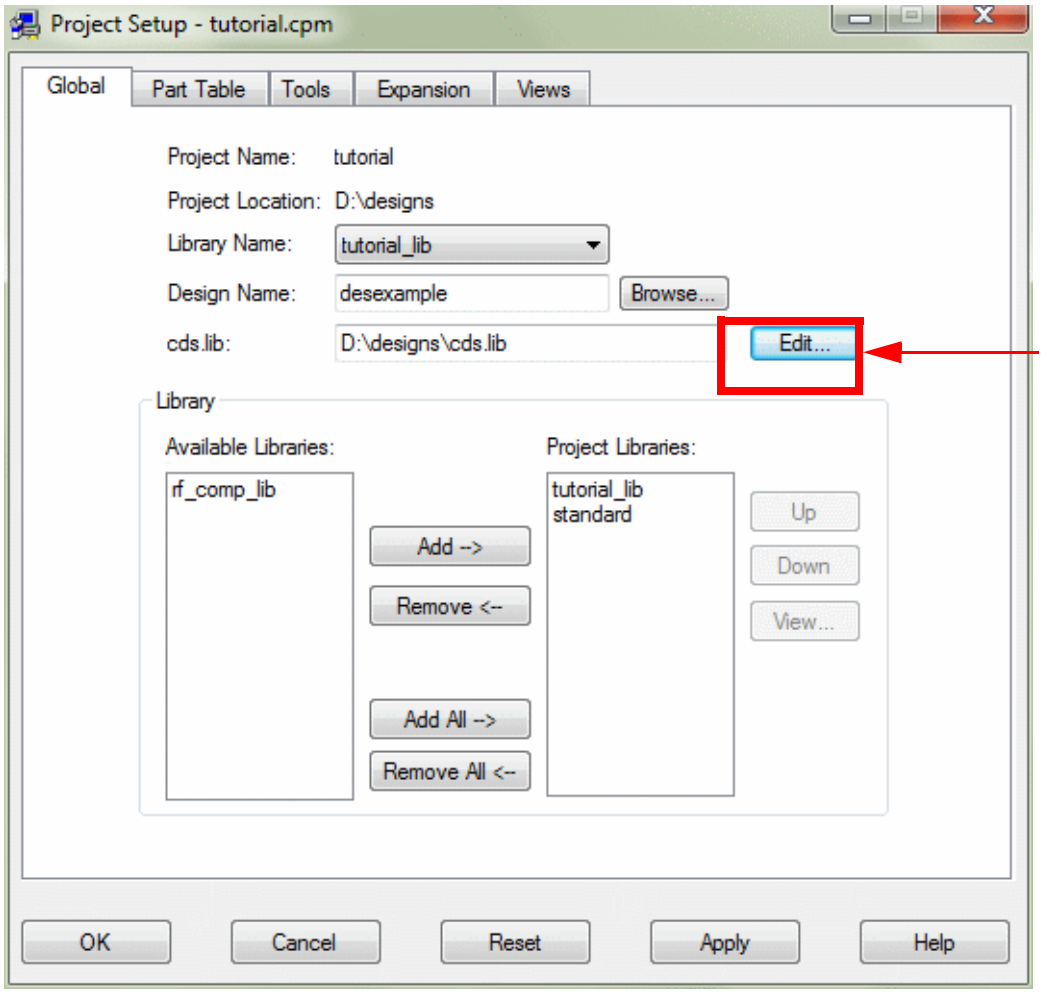
1. On a Windows system, unzip *local_lib.zip*, available at *<your_inst_dir>*`/doc/concepthdl_tut/tutorial_examples` and extract the contents to a directory of your choice.

Note: The `local_lib` library is created only for the current tutorial and is not a standard library file.

2. Click the *Setup* icon in the Project Manager window.



The Project Setup dialog appears.



3. Click *Edit* next to the `cds.lib` field.

   Project Manager opens the `cds.lib` file in a text editor.

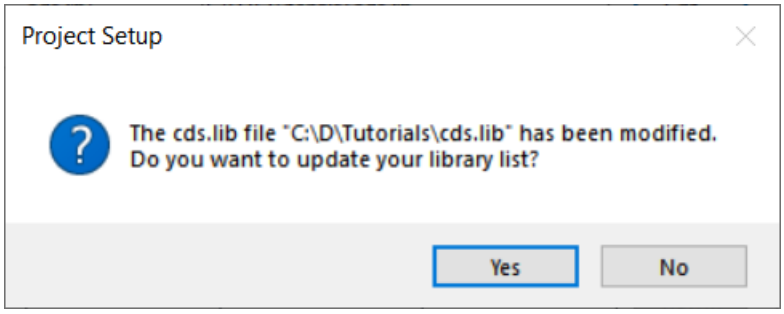
4. To include the local library in your available libraries list, enter the following line in the `cds.lib` file.

   ```
   DEFINE local_lib
   <your_work_dir>concepthdl_tut\174\tutorial_examples\local_lib
   ```

   These lines in the `cds.lib` file includes the path to the `local_lib` library and adds the `local_lib` library to the Available Libraries list.

5. Save and close the `cds.lib` file.

Project Manager displays the following message.

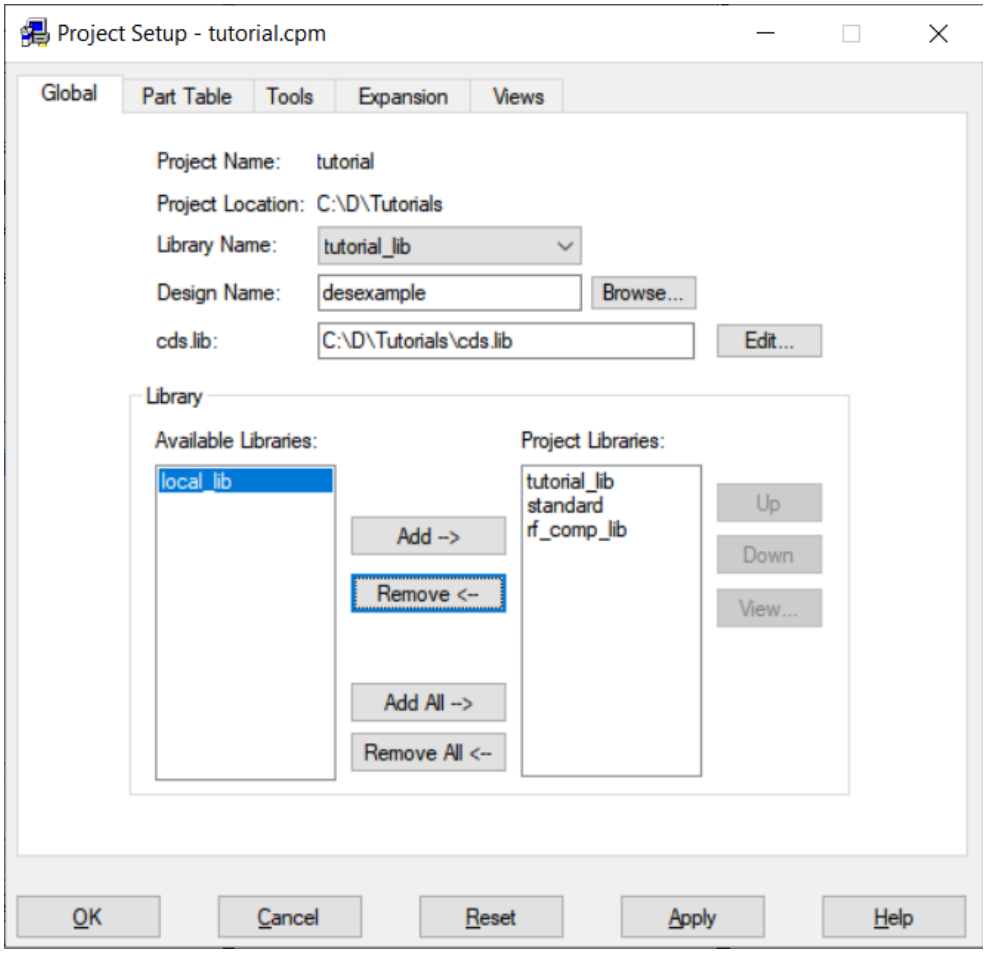


6. Click *Yes*.

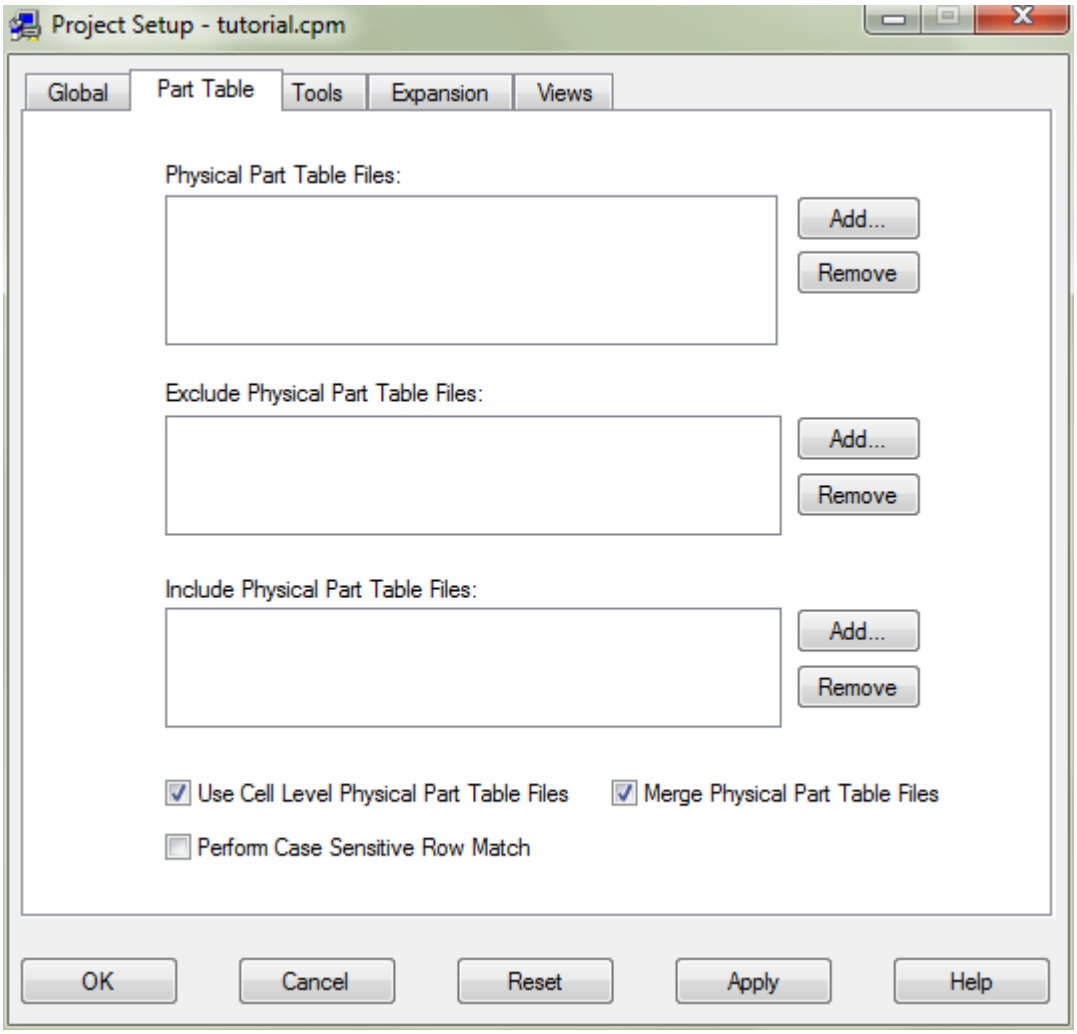
   Project Manager updates the *Available Libraries* list with the `local_lib` library.

7. Select *local_lib* from the *Available Libraries* list.

8. Click *Add*.

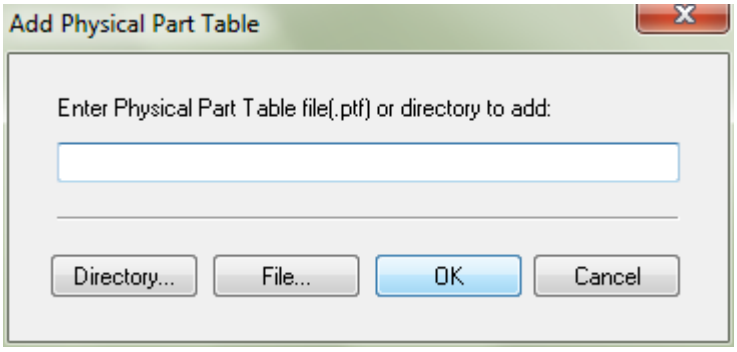


9. Select *local_lib* from the *Project Libraries* list. Ensure that `local_lib` is after *tutorial_lib* in the *Project Libraries* list. Use the *Up* and *Down* buttons, if required.
10. Click *Apply*.
11. Click the *Part Table* tab.



12. Click *Add* near the *Physical Part Table Files* field.

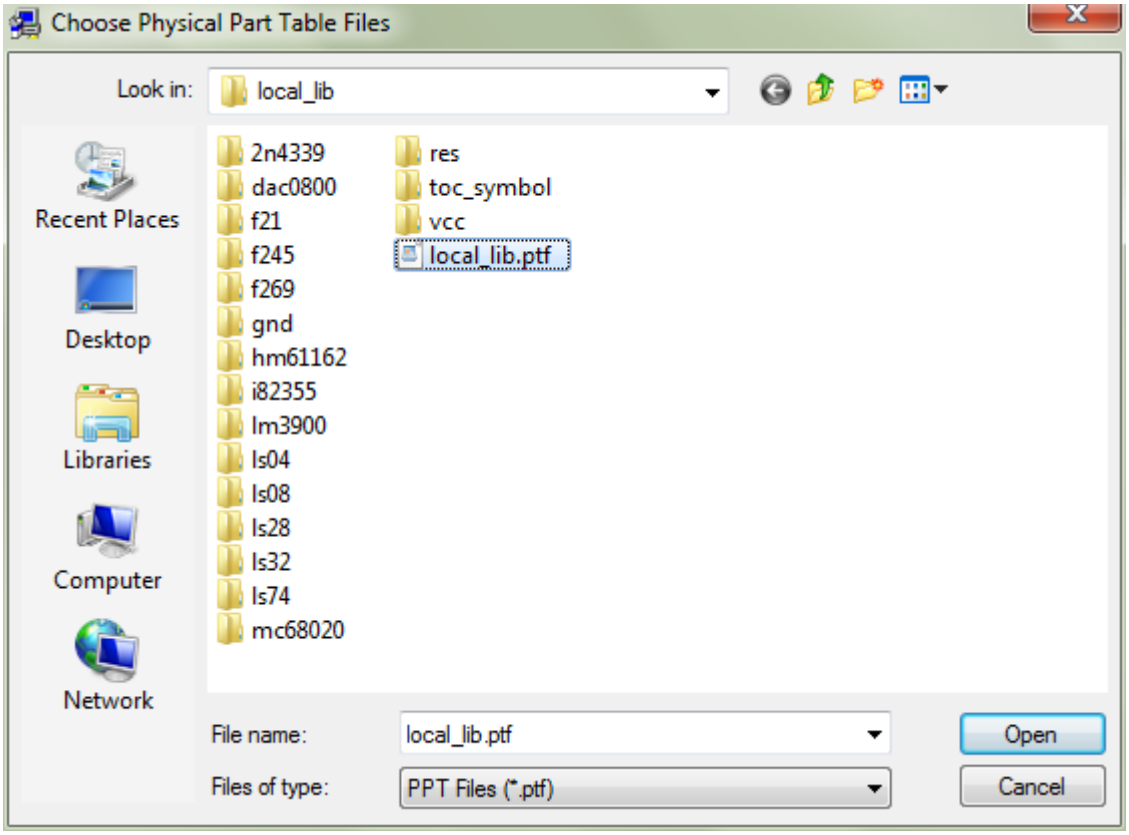
The Add Physical Part Table dialog box appears.



13. Click *File*.

A file browser appears.

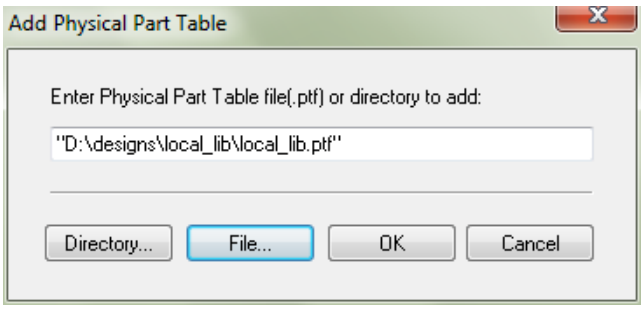
14. Open the `local_lib` folder from your `<your_work_dir>`.



15. Select the `local_lib.ptf` file.

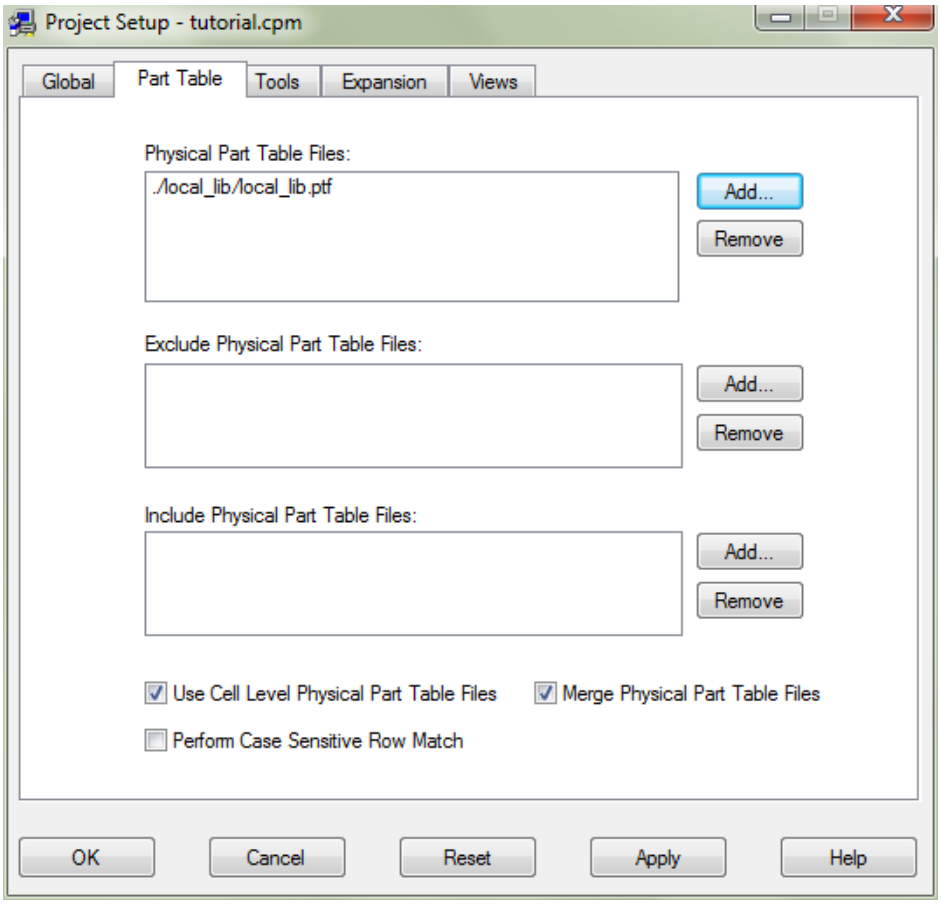
16. Click *Open*.

In the Add Physical Part Table dialog box, the *Enter Physical Part Table file(.ptf) or directory to add* field displays the path to the `local_lib.ptf` file.



17. Click *OK*.

The *Physical Part Table Files* field in the *Part Table* tab displays the path to the `local_lib.ptf` file.



18. Click *OK*.

The Project Setup dialog is closed and you are back to the Project Manager flow.

3

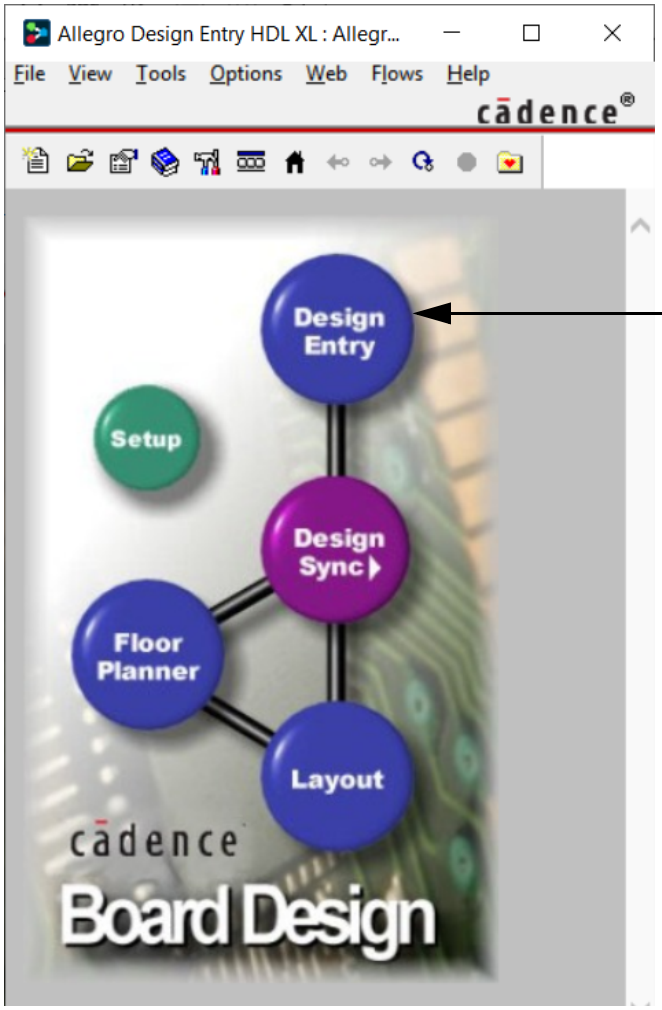
Creating a Schematic: Basics

Overview

This chapter contains the following information:

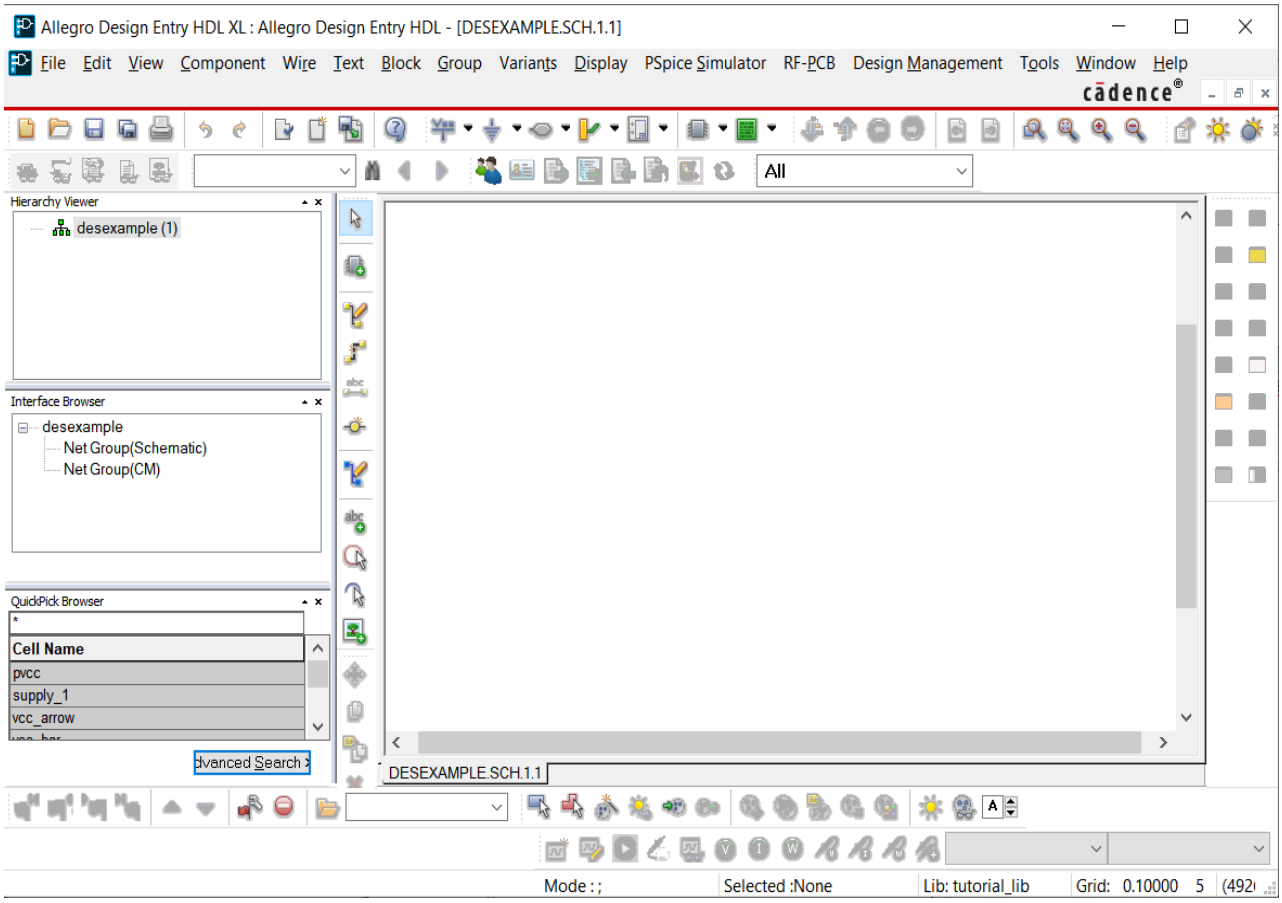
Starting Design Entry HDL

The first step in creating a logic design is starting Design Entry HDL. Using Design Entry HDL, you will place the components from project libraries and connect them to create a logic design. In Project Manager, click *Design Entry*.

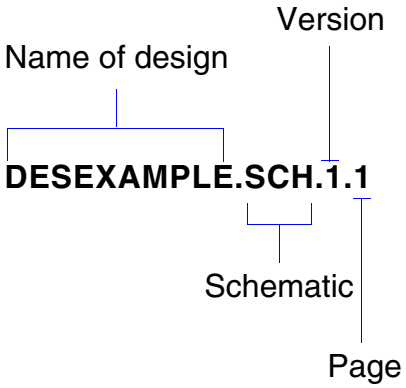


Click to start Design Entry HDL

Allegro Design Entry HDL appears displaying the design name in the title bar.



The following figure explains the naming convention followed by Design Entry HDL.



You can ascend or descend into the various pages and levels in this design by using *File – Edit Hierarchy – Ascend* and *File – Edit Hierarchy – Descend*, respectively. You can also use *File – Return* to return to the previous page you had viewed.

Setting the Pre-Select Use Model

The two use models supported by Design Entry HDL are pre-select and post-select. The default use model is post-select. This tutorial is explained using the post-select mode.

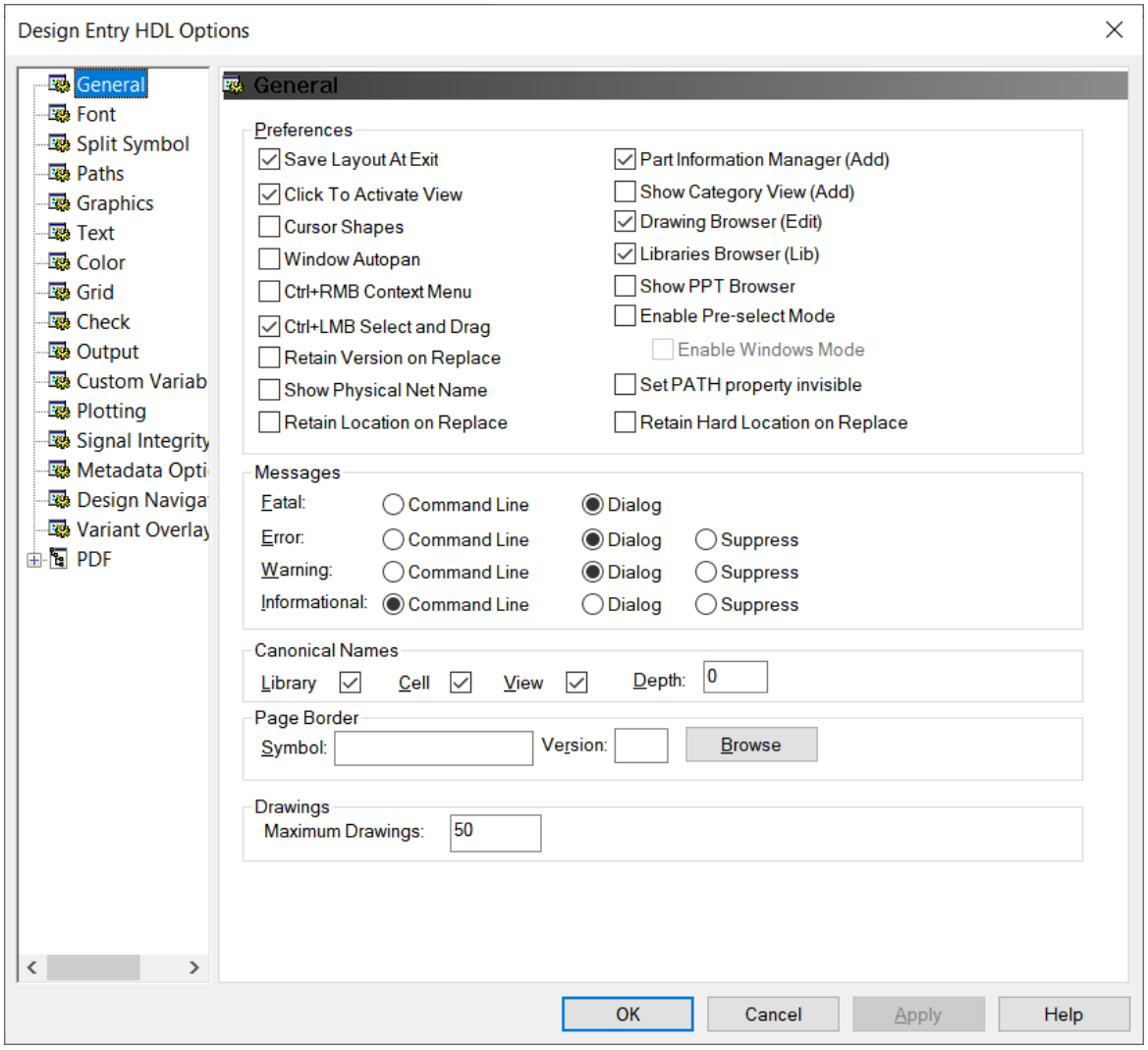
To learn how to work in the pre-select model, change the settings of Design Entry HDL. To set Design Entry HDL in the pre-select model, do the following:

1. Choose *Tools – Options*.

   The Design Entry HDL Options dialog appears.

2. Click *General* in the left pane of the Design Entry HDL Options dialog.

   In the *Preferences* section, select the *Enable Pre-select Mode* check box.



As soon as you select the *Enable Pre-select Mode* check box, the *Enable Windows Mode* option is enabled allowing you to switch to the Windows mode of Design Entry HDL. The Windows mode provides support for common Windows operations in Design Entry HDL such as cut, copy, paste, and delete on schematic objects, and reorganized menus that conform to Windows standards.

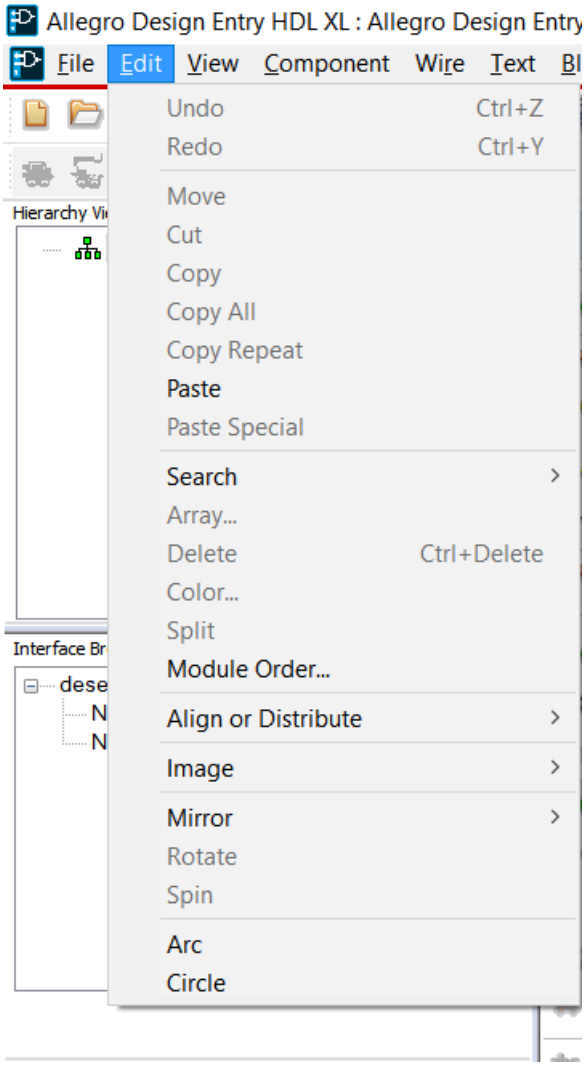
Note: For more information on the Windows mode, refer to *Allegro Design Entry HDL User Guide*.

3. Click *OK* to save the settings and close the Design Entry HDL Options dialog.

   The pre-select mode is enabled.

Note: You can verify whether the pre-select model is enabled or not by viewing the *Edit* pull-down menu. In the pre-select model, command options such as *Copy*, *Move*, *Delete*, *Rotate*, and *Spin* are disabled by default. These options are enabled only after you select a schematic component.

Edit Pull-Down Menu in the Pre-select Mode



Copy, Move, Delete, Rotate, and Spin are unavailable because the pre-select mode is enabled.

4. Deselect the *Enable Pre-select Mode* check box in the *General* tab of the Design Entry HDL Options dialog.

Adding a Page Border

The first step while creating any design is to add a page border. You can have a design without page borders, but it is a good design practice to add page borders. Page borders are required when you cross-reference a design. When you plot a schematic, it is often difficult to trace a signal or instances of a part. Cross Referencer traces the signals and parts in a schematic and annotates the location of each one in a file. Cross Referencer writes the page number and the location of the part or signal with relation to the page border.

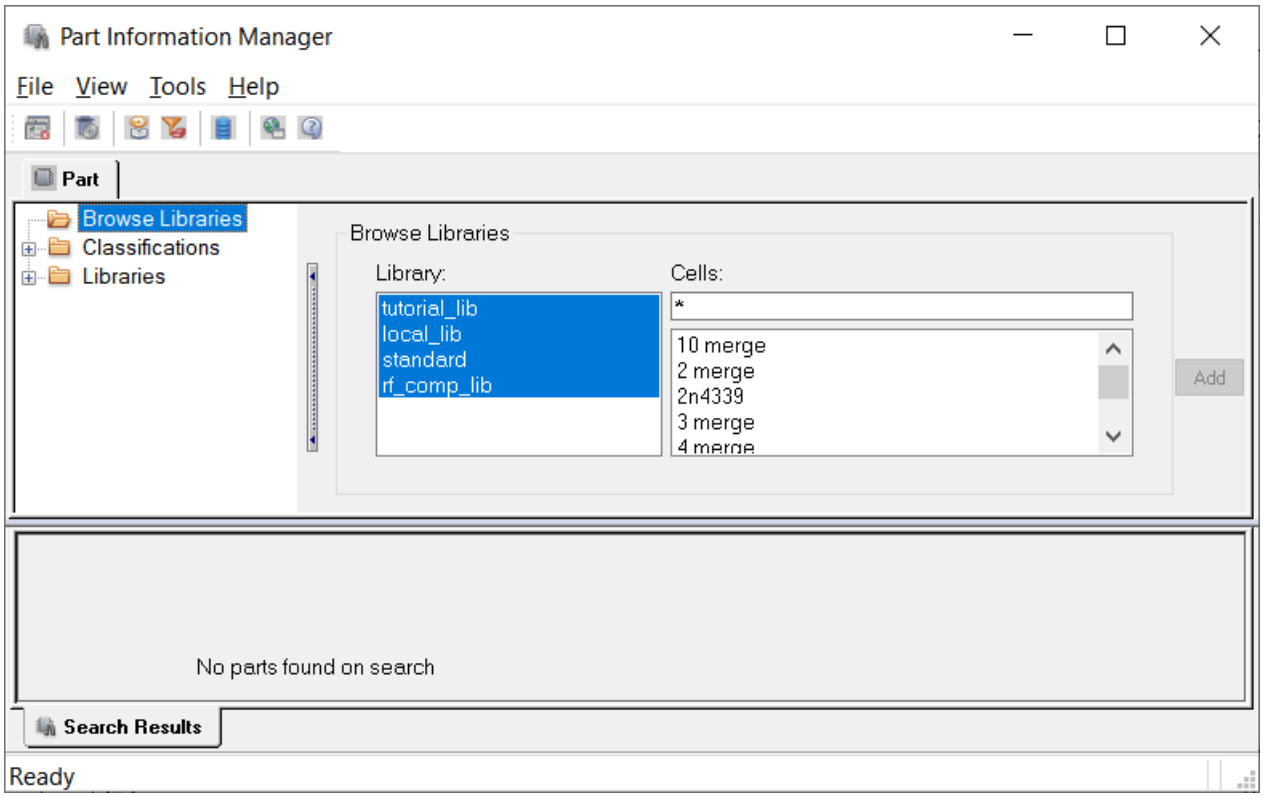
There are two ways in which you can add a page border. The first method is adding the page border manually on each page and the second method is to set Design Entry HDL options so that a page border is added as soon as a new page is created.

Adding a Page Border Manually

Design Entry HDL treats page borders as components.

1. To select and place a page border, choose *Component – Add*.

   Part Information Manager appears.



2. Choose *standard* in the Library field in the *Browse Libraries* node.

   The components in the standard library appear in the *Cells* list.

3. Choose *cadence a size page* from the *Cells* list.
4. Click *Add*.
5. Click in the design window.

   Design Entry HDL displays the page border.

6. Right-click the page border and choose *Done* from the pop-up menu.
7. In Part Information Manager, choose *File – Exit* to close Part Information Manager.
8. choose *File – Save*.

Adding a Default Page Border

You can set options in Design Entry HDL to add a page border by default whenever a new page is added to the design.

1. Choose *Tools – Options*.

   The Design Entry HDL Options dialog appears with the *General* tab selected.

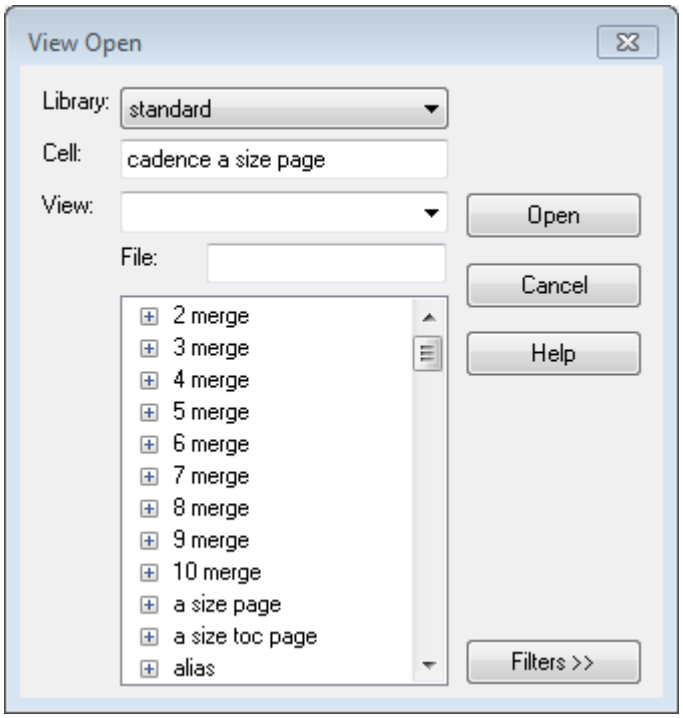
2. In the *Page Border* section specify the name and version of the page border symbol that is to be added to all the pages.

   To specify the symbol name, click *Browse*.

   The View Open dialog appears.

3. Select the `standard` library.

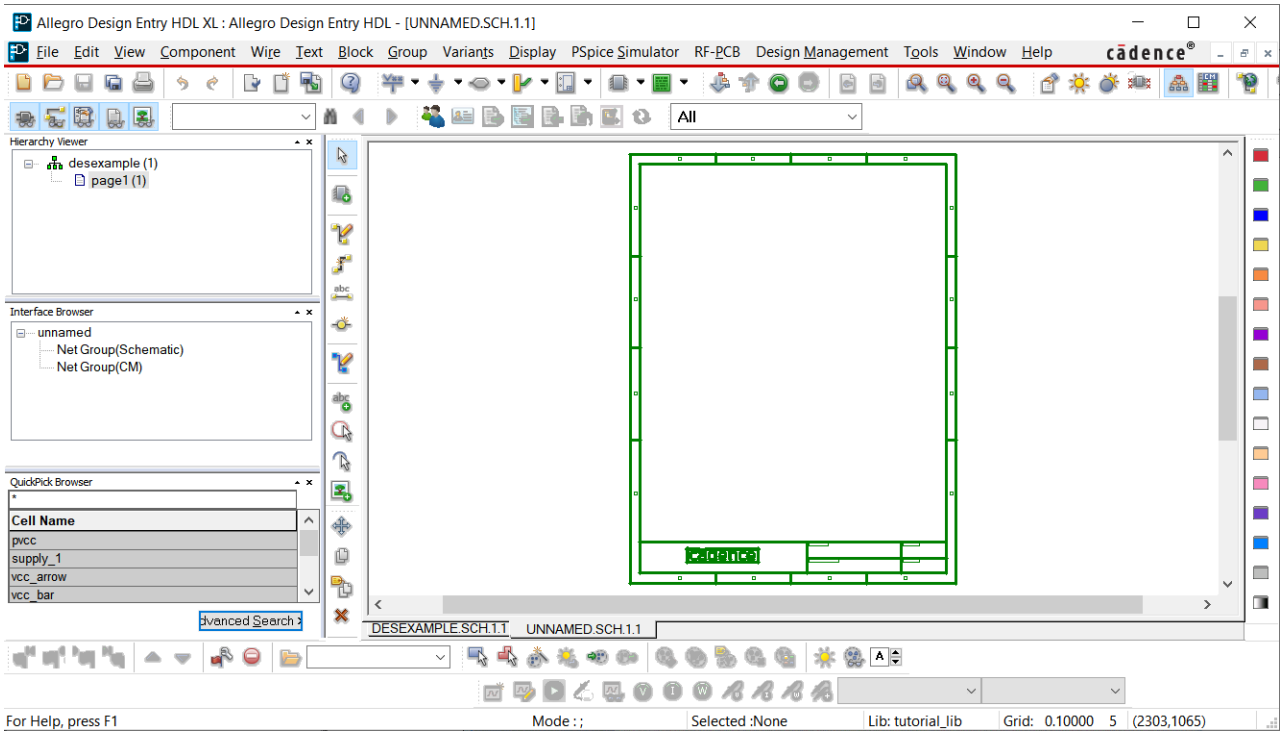
The list of components available in the *standard* library appears.



4. From the list, select a page border.
5. For this tutorial, select *cadence a size page* and click *Open*.

   The Design Entry HDL Options dialog reappears with the *Symbol* and *Version* of the page border added.
6. Click *OK* to save the settings.
7. Choose *File – New* in the Design Entry HDL design window.

   A new design named *UNNAMED.SCH.1.1* appears with the page border added. All new designs or pages added to the design will now have the defined page border.



1. Choose *File – Close t*o close the UNNAMED.SCH.1.1 design and return to the DESEXAMPLE.SCH.1.1 design.

Adding Text (Notes)

You can add additional details to the schematic, such as the following:

- Title (name of the design)
- Engineer (name of the engineer who created the design)
- Date (date of creation)
- Page (page number)

To add text to the page border, you need to zoom into the area where you can enter text.

To zoom into an area

1. Click the *Zoom Points* button () on the Standard toolbar.

2. Click at the start of the area you want to zoom into. Drag the mouse to the end of the area. Click again to stop drawing the rectangle. Design Entry HDL zooms into the area.

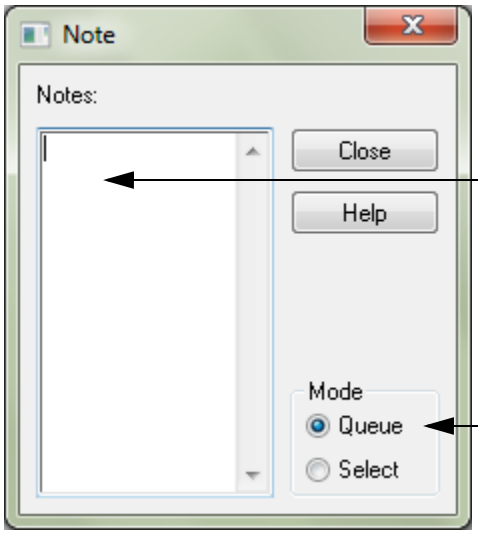
1. Click the start of the area you want to zoom into.

2. Drag the mouse to the end of the area. Click again to stop drawing the rectangle.

To add text (notes) in the page border

1. Choose *Text – Note.*

The Note dialog box appears.

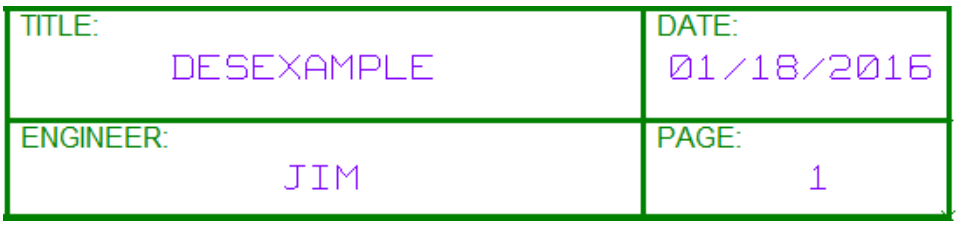


Enter text in the order in which you want to place it on the page border.

Ensure that the Queue option is selected.

2. Enter the following text in the Notes field:
   - ❑ DESEXAMPLE
   - ❑ JIM
   - ❑ 01/18/2016
   - ❑ 1
3. Click the following fields in the page border in the following order:
   a. TITLE
   b. ENGINEER
   c. DATE
   d. PAGE

   Design Entry HDL adds notes in the order in which you enter them in the Notes field, at the places you click in the page border.



4. Click *Close* in the Note dialog box.
5. Click the *Zoom Fit* button () on the Standard toolbar to view the entire page.

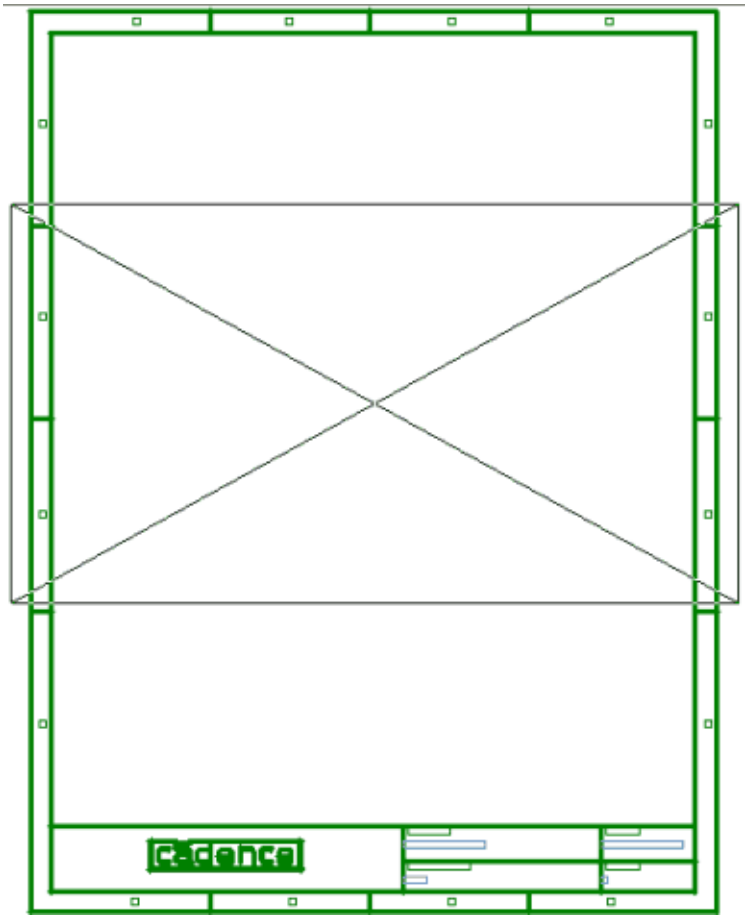
   Design Entry HDL fits the entire page in the design window.

Choosing and Adding Components

Creating a project using Design Entry HDL involves different steps, such as adding components, connecting the components using wires, and adding input/output ports.

The components are stored in different libraries. Use Part Information Manager to choose components from project libraries and place them in the Design Entry HDL design window.

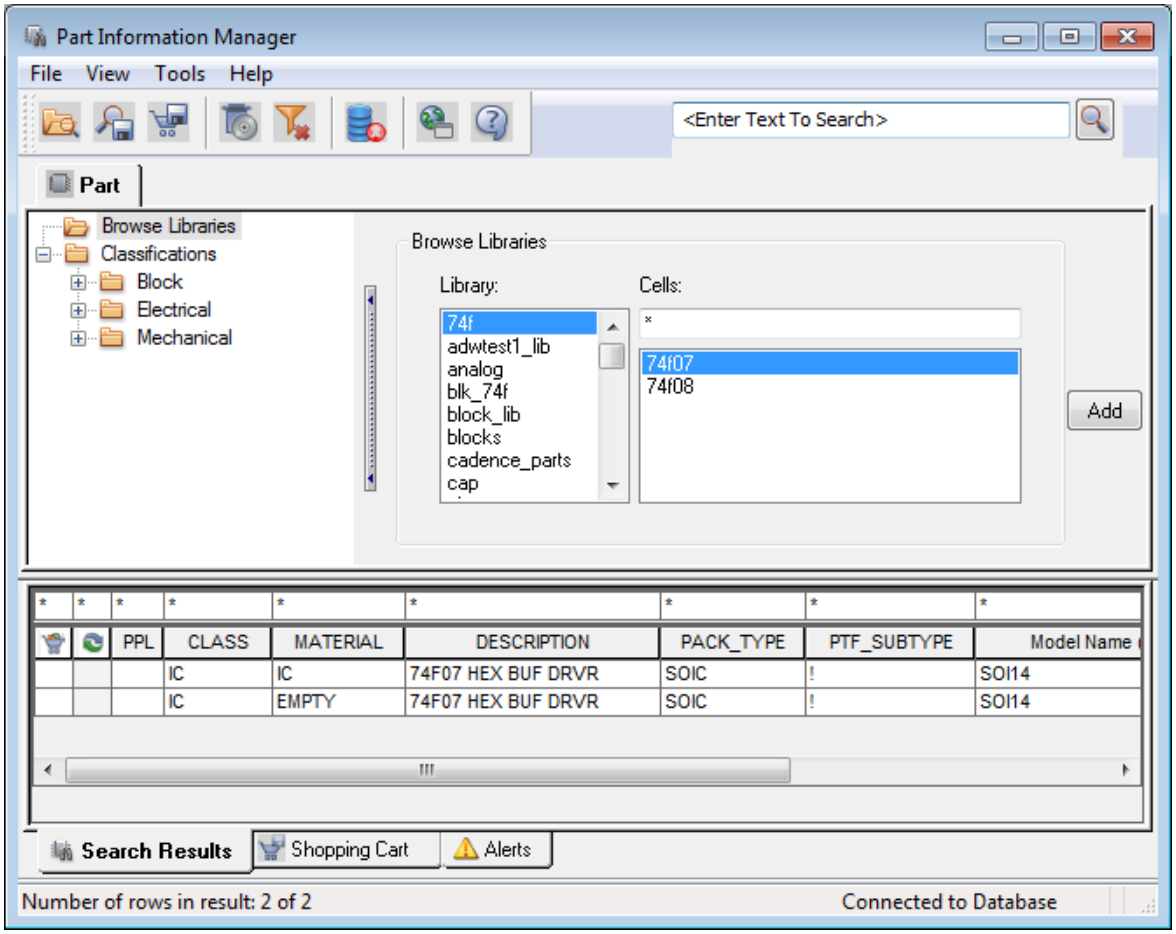
1. Click the *Zoom Points* button and zoom into the area shown below.



Design Entry HDL zooms into the selected area.

2. Choose *Component – Add* to start adding components.

Part Information Manager appears.



3. Select `local_lib` in the *Library* field.

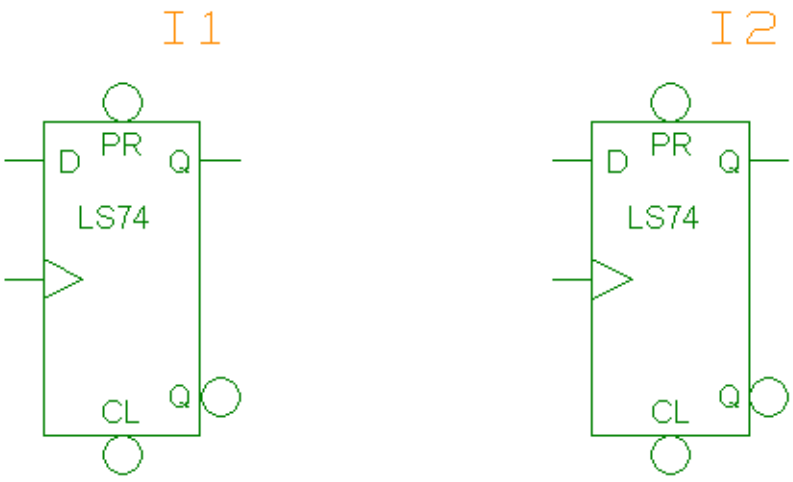
   The components of the *local_lib* library appear in the Cells list.

4. Select `LS74` from the *Cells* list and click *Add*.

5. Click in the design window. When you click in the window, leave enough space to add another component next to `LS74`.

   The `LS74` component is placed on the schematic.

6. Place another instance of `LS74` adjacent to the first instance of `LS74`. Click *Edit - Copy* and select the first instance of `LS74`. Click beside it to place another instance of `LS74`.



7. Right-click on the second instance of `LS74` and choose `Done` from the pop-up menu.
8. In Part Information Manager, choose *File – Exit* to close Part Information Manager.

   For each instance of a component you place, Design Entry HDL automatically assigns a PATH property. This property has a unique value that helps identify the instance, for example, `I1, I2, I3...In`.

   In the previous example, the two instances of the component `LS74` are identified as `I1` and `I2`.

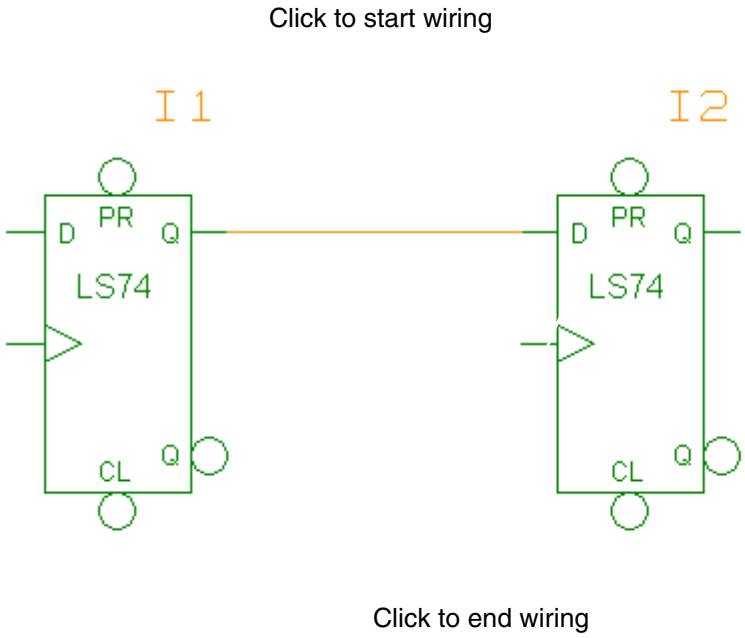
Connecting Parts

After placing the components on the Design Entry HDL design window, you need to connect the components by using wires.

1. Choose *Wire – Draw.*
2. Click first at the tip of pin `Q` of `I1` and then at the tip of pin `D` of `I2` to connect the components.

   Note: While drawing wires, start the wire from the tip of the pin and do not cover the pin completely.

Design Entry HDL connects pin `Q` of `I1` and pin `D` of `I2` as shown in the following figure:



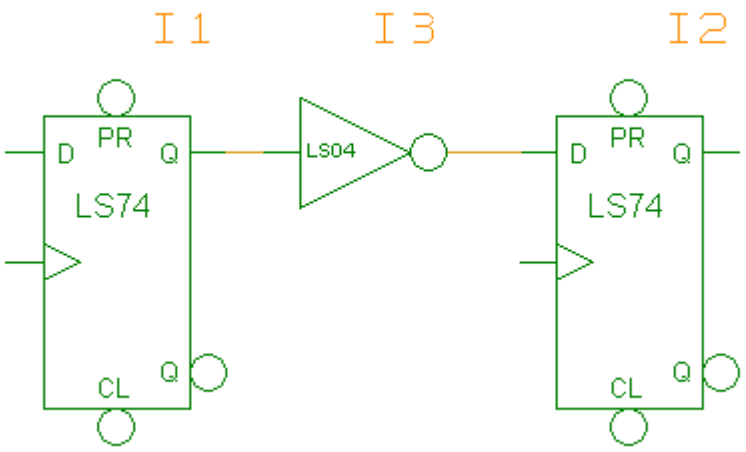
3. Choose *Component – Add*.

   Part Information Manager appears.

4. Choose the `LS04` component from the *local_lib* Cells list and place it on the wire connecting `I1` and `I2`.

5. Close Part Information Manager.

`LS04` is connected with I1 and I2 as shown in the figure below.

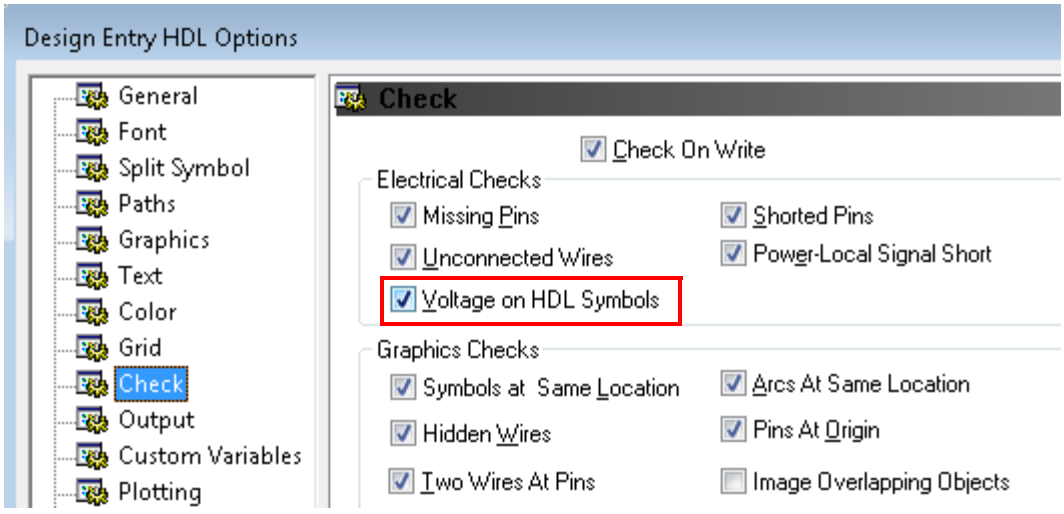


6. Choose *File – Save* to save the schematic.

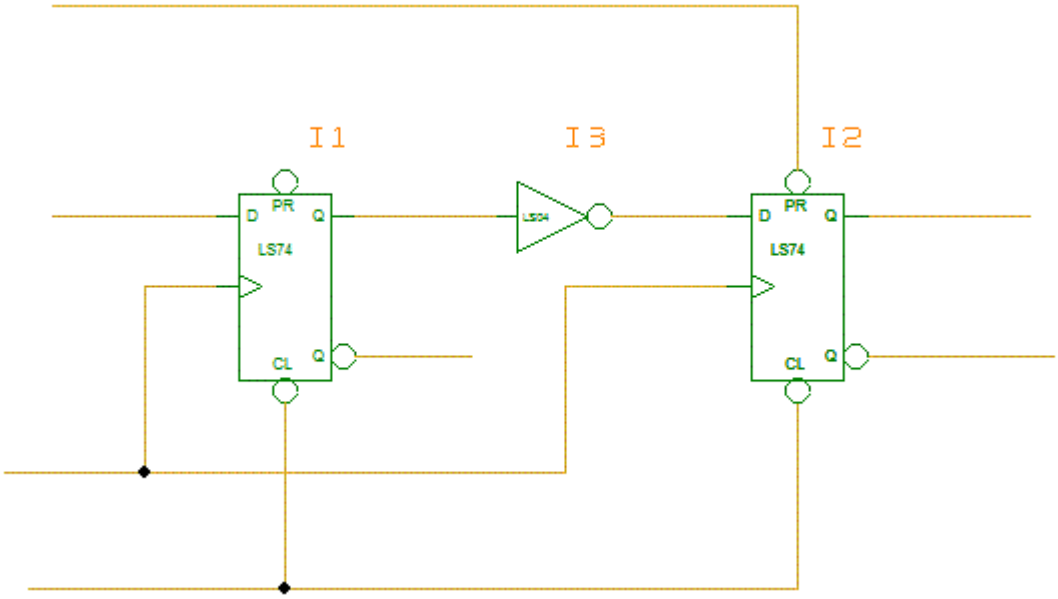
Design Entry HDL saves the schematic without any errors.

Note: If you see errors related to HDL power symbols, choose *Tools – Options*.

The Design Entry HDL Options dialog appears. Choose *Check* in the left pane. Uncheck the *Voltage on HDL Symbols* box and click *OK* to close the dialog.



7. Add more wires to the components as shown in the following figure:



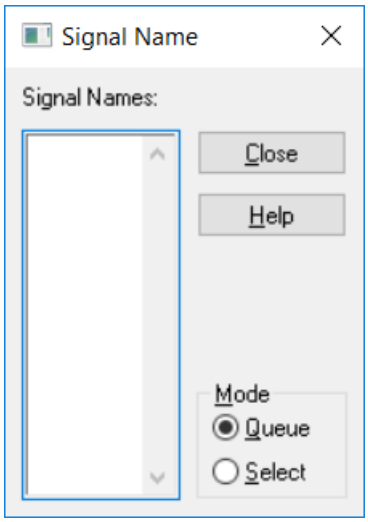
After drawing each wire, right-click the wire and select *Done* from the pop-up menu. Click and then click again to terminate a wire at a location that is not a pin or another wire.

Naming Wires

Design Entry HDL supports connection by name. If two signals on the same or different pages of the same design have the same name, Design Entry HDL considers them to be the same signals. Design Entry HDL does not require the use of off-page connectors for signals spanning multiple pages.

1. Choose *Wire – Signal Name*.

   The Signal Name dialog box appears.

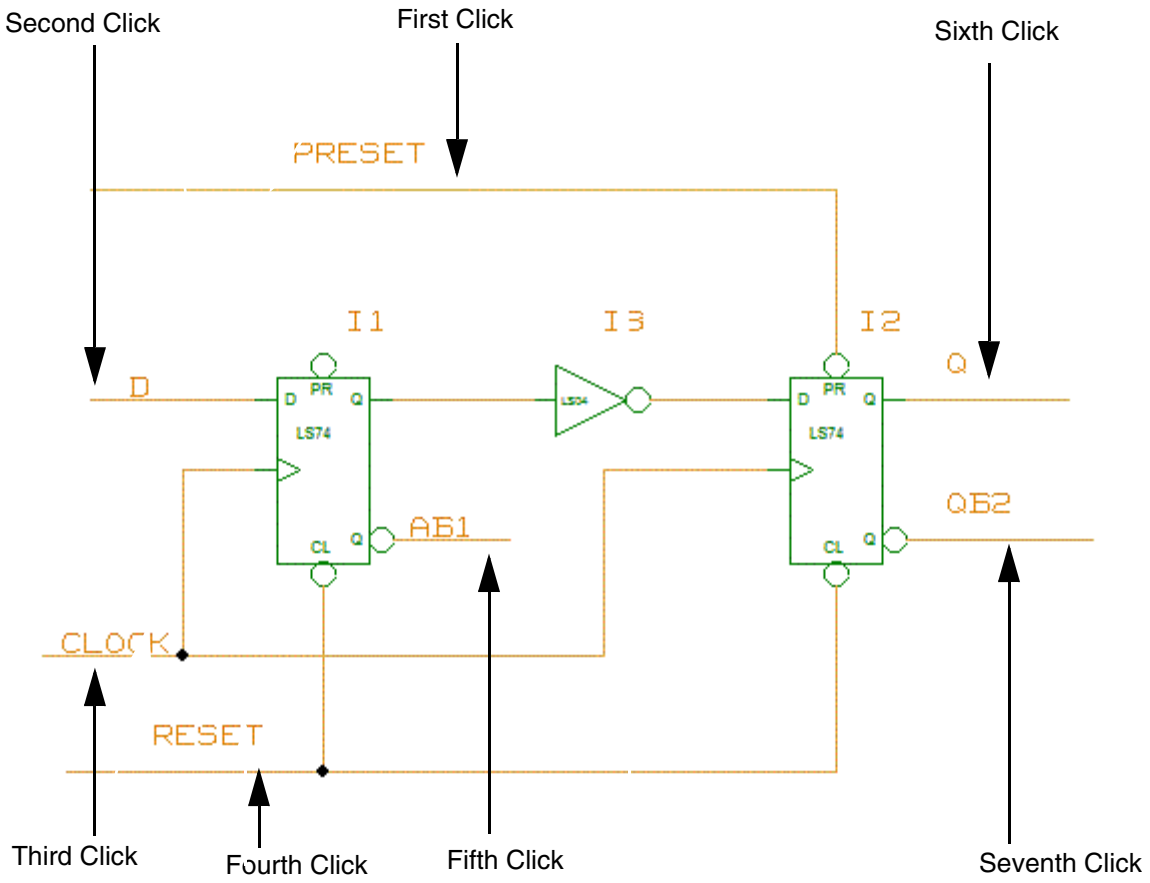


2. Enter the following text in the given sequence in the *Signal Names* field.

   - ❑ PRESET
   - ❑ D
   - ❑ CLOCK
   - ❑ RESET
   - ❑ AB1
   - ❑ Q
   - ❑ QB2

   Note: Ensure that the *Queue* option is selected.

3. Click the wires one after another to name each as shown in the following figure:



Adding Ports

Cadence supplies input and output ports in the standard library. You can use Part Information Manager to select and place a port in the schematic.

1. Choose *Component – Add.*

   Part Information Manager appears.

2. Choose `Standard` as the *Library*.

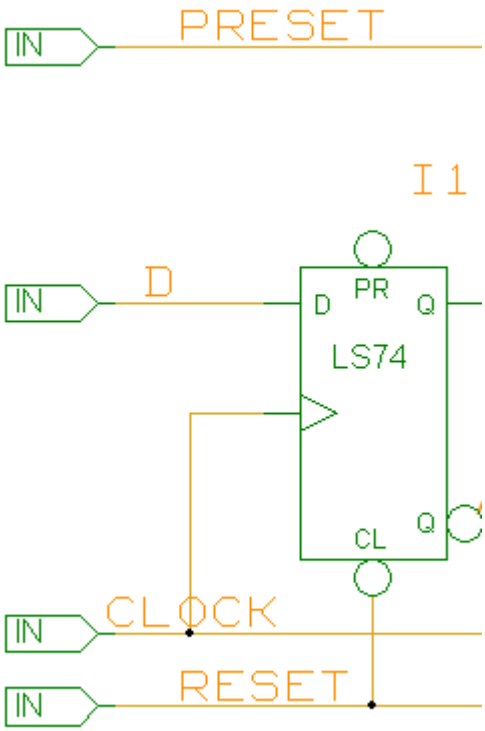
3. Choose `INPORT` from the *Cells* list and click *Add*.

4. In the design window, click at the tip of the wire named `PRESET` to place `INPORT`.

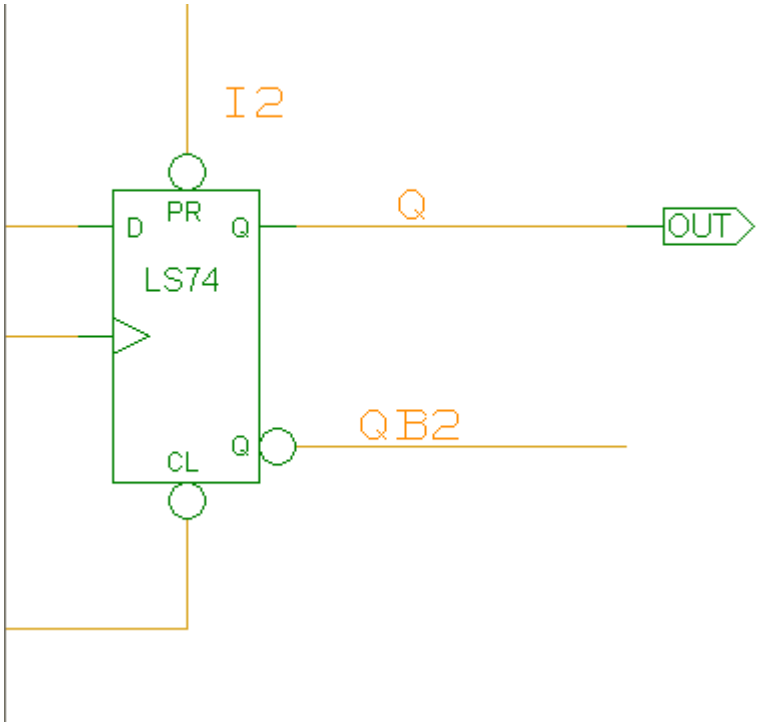
   This defines PRESET as an input port.

5. Click the schematic to instantiate INPORT again.
6. Click at the tip of wire D to place INPORT.

   Similarly, instantiate and place INPORT on wires as shown in the figure below.



7. In Part Information Manager, select `OUTPORT` from the *Cells* list and click at the tip of the wire named `Q` to place `OUTPORT` as shown in the following figure:



8. Close Part Information Manager.

Adding Power and Ground

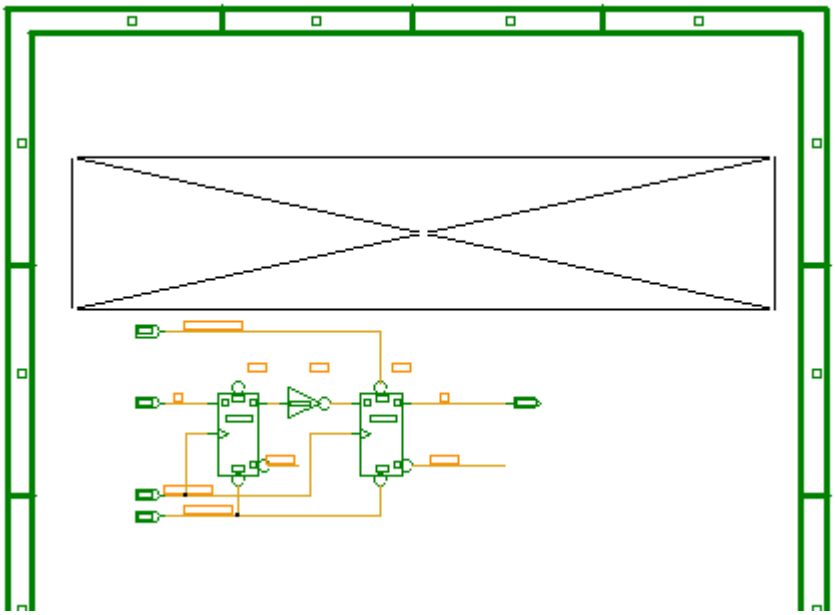
The next step is to add power to the `AB1` wire and ground to the `QB2` wire. The required power and ground pins are available in the `local_lib` library.

1. Click the *Zoom Fit* button on the Standard toolbar.

   Design Entry HDL fits the schematic page in the design window.

2. Click the *Zoom Points* button on the Standard toolbar.

3. Select the area to zoom in as shown in the following figure:



1. Click at the start of the area you want to zoom into.

2. Drag the mouse to the end of the area.Click again to stop drawing the rectangle and zoom into the selected area.

Design Entry HDL zooms into the selected area.

4. Choose *Wire – Draw*.

5. Draw a horizontal wire as shown in the following figure:

6. Right-click and choose *Done*.

7. Choose *Edit – Copy*.

8. Click the wire and click above to paste as shown in the following figure:

9. Right-click and choose *Done*.

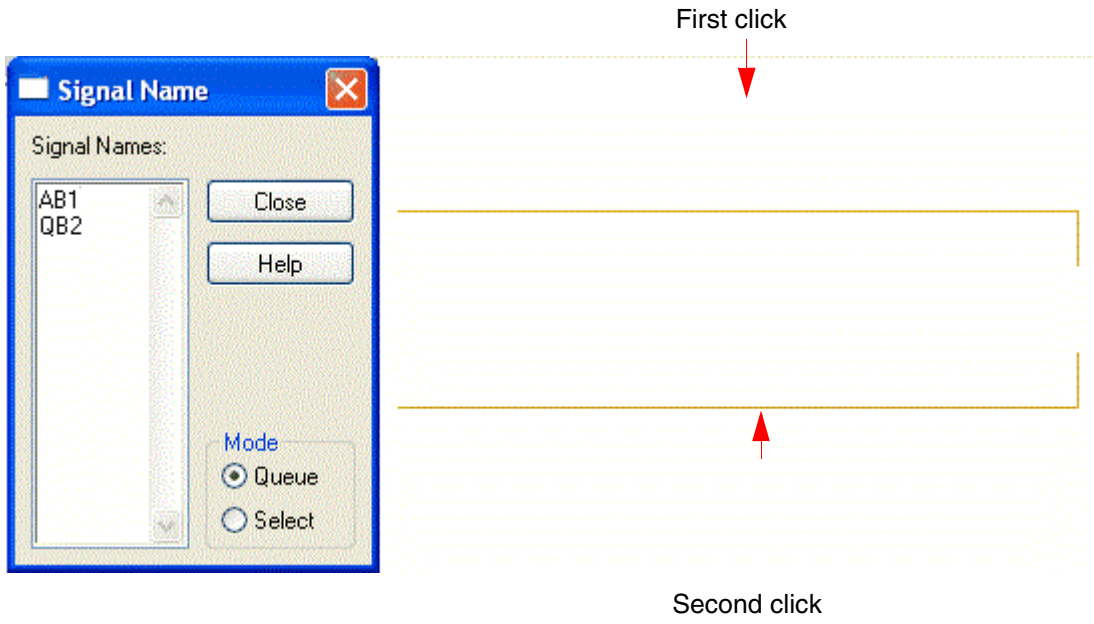
10. Extend the wires as shown in the following figure:

11. Right-click and choose *Done*.

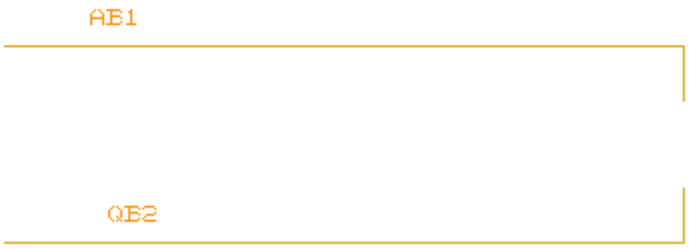
12. Choose *Wire – Signal Name*.

The Signal Name dialog box appears.

13. Enter `AB1` and `QB2` as signal names and click the wires as shown in the following figure:



Design Entry HDL names the wires as shown below:



14. Click *Close* in the Signal Name dialog box.

15. Choose *Component – Add*.

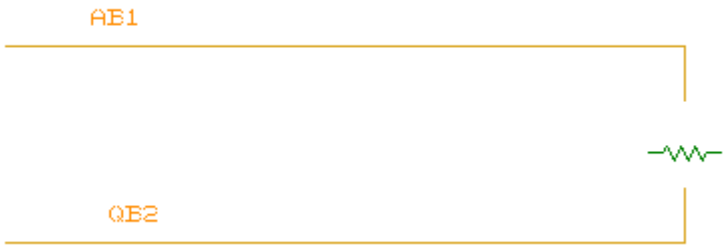
Part Information Manager appears.

16. Choose `local_lib` as the library.

17. Choose `RES` from the *Cells* list.

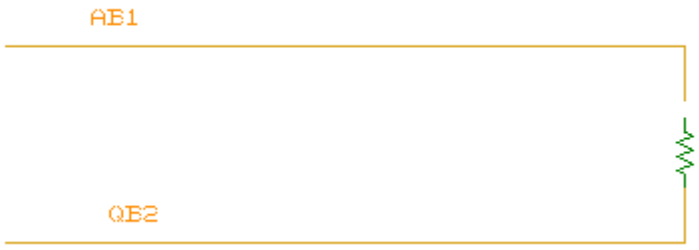
18. Click the *Add* button.

19. Click in the design window to place the resistor as shown in the figure below.



20. Choose *Edit – Rotate* and click the resistor, or click the resistor, right-click and select *Rotate*.

Design Entry HDL rotates the resistor as shown below.



21. Right-click and choose *Done*.

22. Choose *Edit – Copy*.

23. Click `RES` and click again to paste a copy of `RES` as shown in the following figure:

24. Choose *Edit – Move*.

25. Click a resistor and connect it to the wire.

26. Click the second resistor to connect the second wire as shown in the following figure:

27. Choose *Wire – Draw*.

28. Draw wires at the ends of the resistors as shown in the following figure:

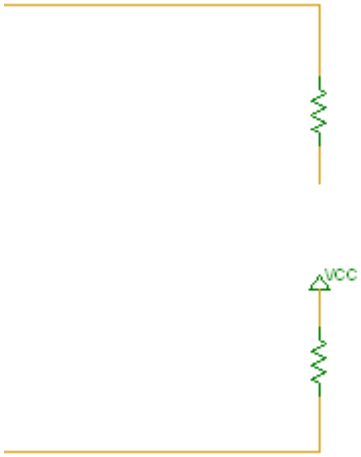
29. Choose *Component – Add*.

Part Information Manager appears.

30. Choose *local_lib* as the *library*.

31. Choose *VCC* from the Cells list and click *Add*.

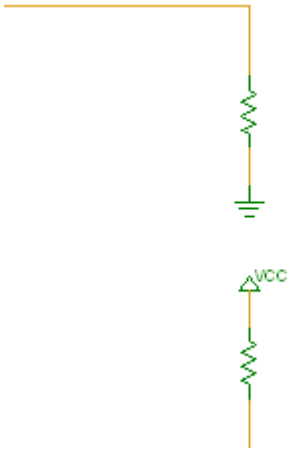
32. Click in the design window to place `VCC` as shown in the following figure:



33. Choose *standard* as the *library.*

34. Choose `gnd_power` from the Cells list and click *Add*.

35. Click in the design window to place `gnd_power` as shown in the following figure:



36. Choose *local_lib* as the library.

37. Choose *LS04* from the Cells list.

38. Place `LS04` on `AB1` and `QB2` as shown in the following figure:

39. Right-click on the `LS04` component and choose *Done*.

40. Close Part Information Manager.

41. In the schematic, click the *Zoom Fit* button on the Standard toolbar.

Design Entry HDL fits the page on the design window.

42. To save the design, choose *File – Save*.

Video

See the multimedia demonstration titled *Creating a Schematic* for an example of the schematic creation process.

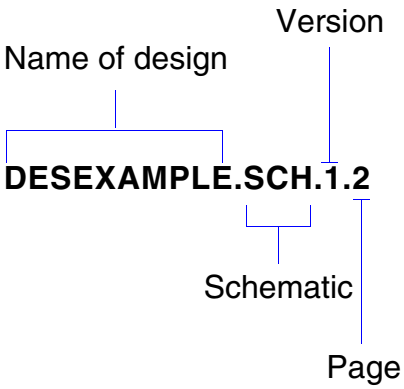
Adding Pages to the Schematic

While creating a design, it is not always possible to fit the entire design in a single page. You can have a schematic design that has multiple pages.

1. To add a new page to the schematic, choose *File – Edit Page/Symbol – Add New Page*.

   A new page is added and displayed. The title bar shows [DESEXAMPLE.SCH.1.2].

   The following figure explains the naming convention followed by Design Entry HDL:

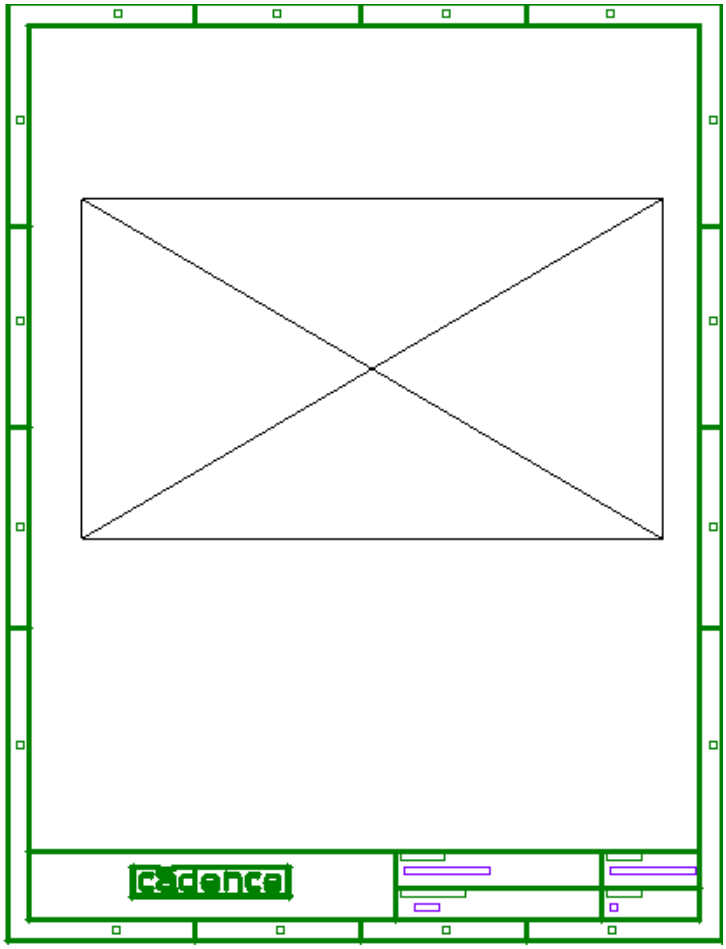


2. The new page appears with the page border added.

   Add text on the page border to specify the name of the engineer, title of the design, date of creation, and the page number. Specify the page number as `2`.

3. Click the *Zoom Points* button on the Standard toolbar.

4. Select the area to zoom in as shown in the following figure:



Design Entry HDL zooms into the selected area. Add the `MC68020` component to the schematic page.

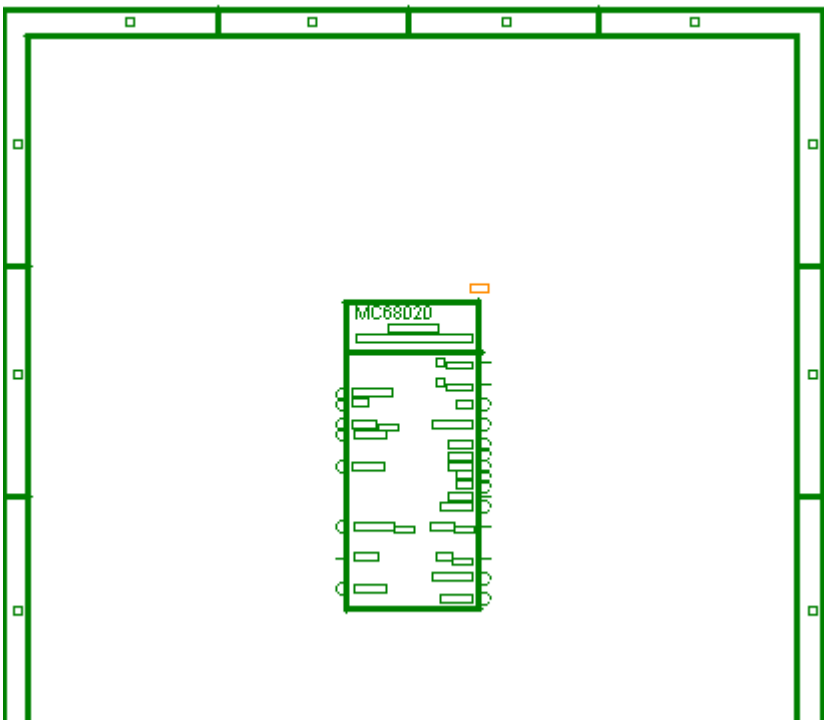
5. To add the `MC68020` component, choose *Component – Add*.

   Part Information Manager appears.

6. Select `local_lib` from the *Library* list.

7. Select `MC68020` from the *Cells* list and click *Add*.

8. Click in the design window to place `MC68020`.

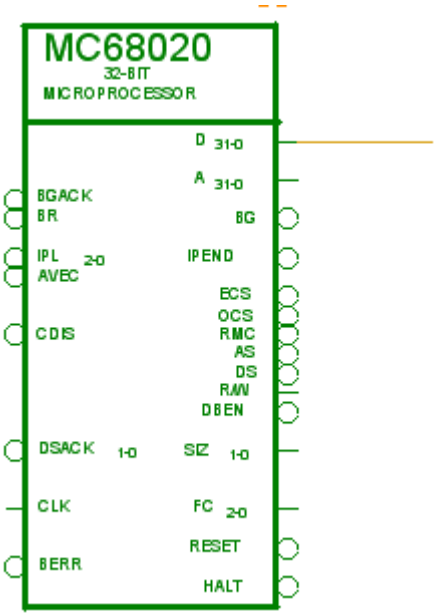


9. Close Part Information Manager.

Creating Buses

Creating buses is similar to creating wires, but the naming convention used is slightly different. The convention used is name<n-1..0> where n represents the bus size in bits. A 16-bit bus named DATA is represented as DATA<15..0>, and a 32-bit bus with the same name is represented as DATA<31..0>.

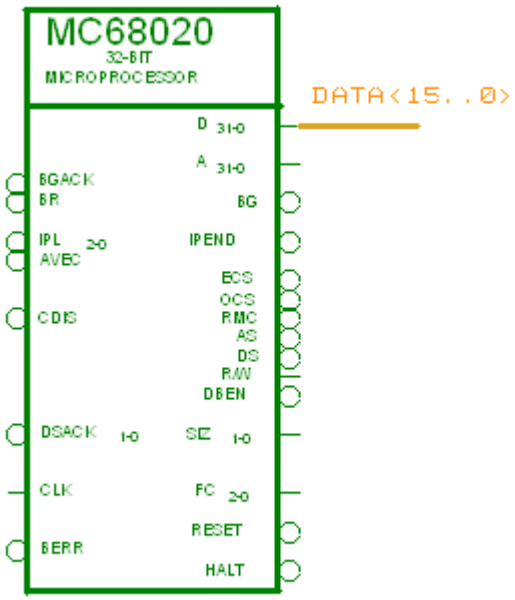
1. Choose *Wire – Draw*.
2. Draw a wire on pin D 31-0 as shown in the following figure:



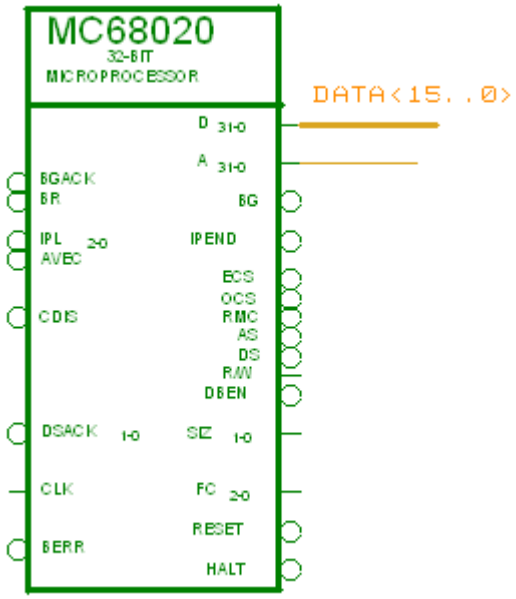
3. Choose *Wire – Signal Name*.

   The Signal Name dialog box appears.
4. Enter `DATA<15..0>` as the signal name.
5. Click the wire to name it.

Design Entry HDL attaches the name to the wire and thickens the wire to convert it to a 16-bit bus as shown in the following figure:



6. Choose *Wire – Draw* to add a 32-bit bus on pin A31-0.
7. Draw a wire on pin A 31-0 as shown in the following figure:



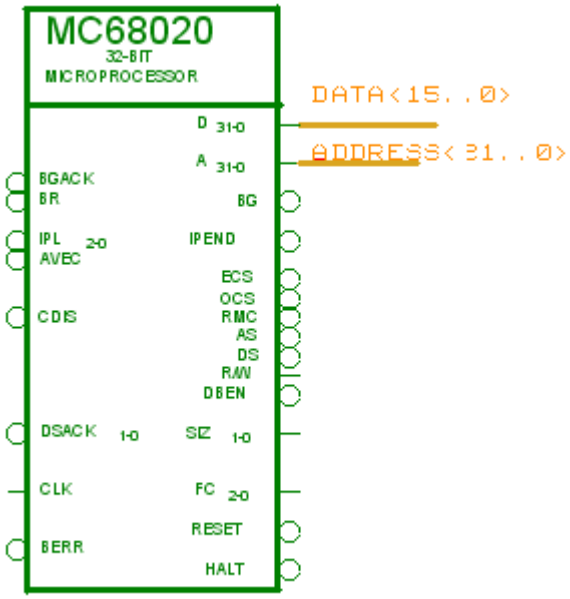
8. Choose *Wire – Signal Name*.

   The Signal Name dialog box appears.

9. Enter `ADDRESS<31..0>` as the signal name.

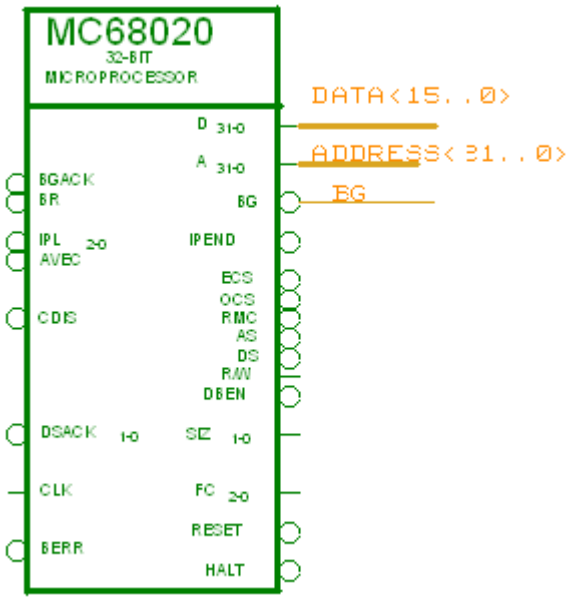
10. Click the wire to name it.

    Design Entry HDL attaches the name to the wire and thickens the wire to convert it to a 32-bit bus as shown in the following figure:

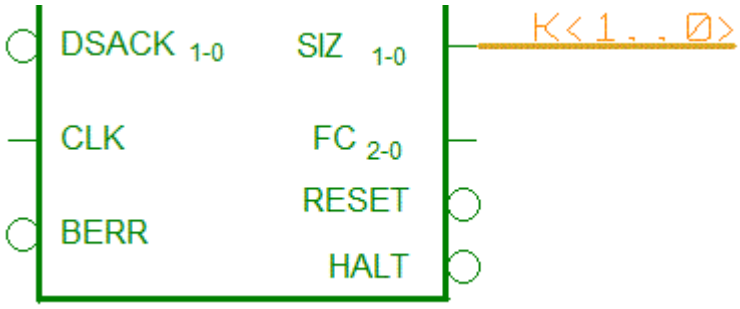


11. Add a wire to the BG pin.

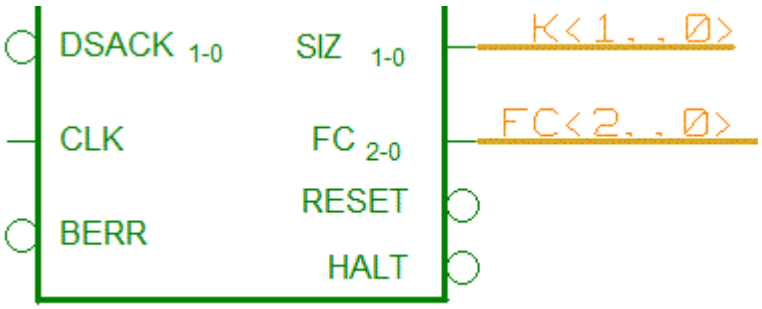
12. Specify `BG` as the name of the wire.



13. Add a wire to *SIZ1-0* and name it `K<1..0>` as shown in the following figure:



14. Add a 3-bit bus to pin `FC<2..0>` as shown in the following figure:



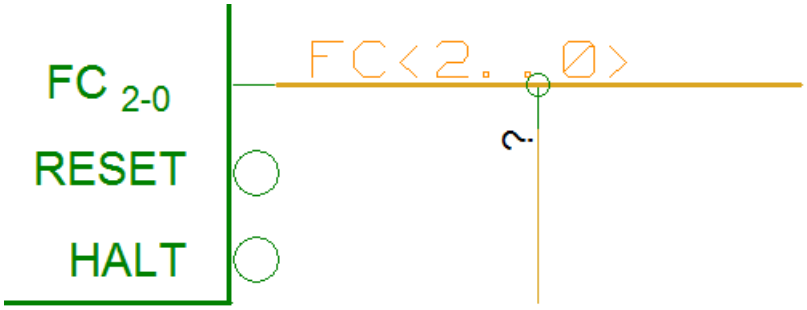
Tapping a Bus

While designing a circuit, use a particular bit from a bus as an input to a component in the circuit. To extract a particular bit from a bus, you need to tap a bus. In this section, you will tap the 3-bit bus, `FC<2..0>`, to extract the value stored in bit 1.

1. Zoom into `FC<2..0>`.

   Design Entry HDL zooms into the bus as shown in the following figure:

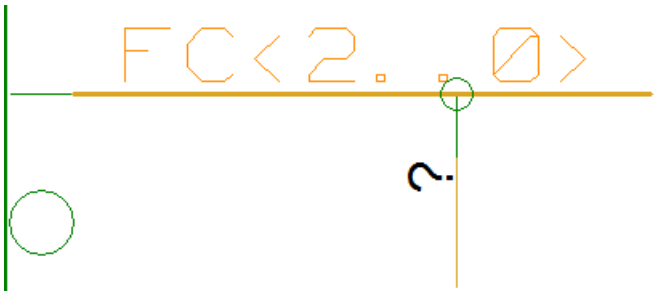
2. Choose *Wire – Bus Tap* to tap the bus.
3. Click `FC<2..0>` to place the bus tap symbol.
4. Extend the wire downwards, and double-click.
5. Right-click and choose *End Tap*.



   A question mark appears on the bus tap symbol. Replace this symbol with the bit number that is to be extracted.

6. Choose *Text – Change*.
7. Double-click the question mark.

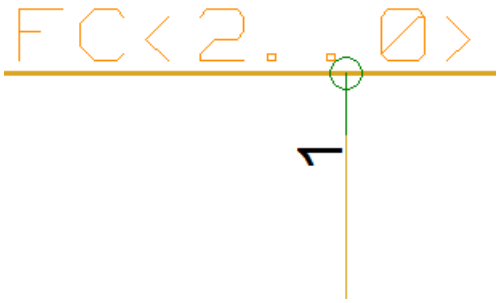
Design Entry HDL places a cursor on the question mark.



8. To indicate that you want to extract bit 1 in the schematic design, delete the question mark and enter 1.
9. Press `Enter`.

   Design Entry HDL marks 1 as the BN property (Bit Number) value.

   Note: If a tapped signal is not named, Design Entry HDL names the signal automatically.



Adding Physical Information

One of the factors that influences the PCB design is the behavior of components used in a circuit. A design is also influenced by factors such as temperature and component tolerance.

While creating a schematic design, you can specify the physical information of a component. The physical information is added on a component using the Physical Part Filter in Part Information Manager. The Physical Part Filter displays the Part Table File (`.ptf`) associated with a component or a library.

The Part Table File associates a logical part with physical parts that have varying physical properties. Each row in the Part Table file (and in the Physical Part Filter) corresponds to a physical part.

Note: You can create a part table file using Part Developer.

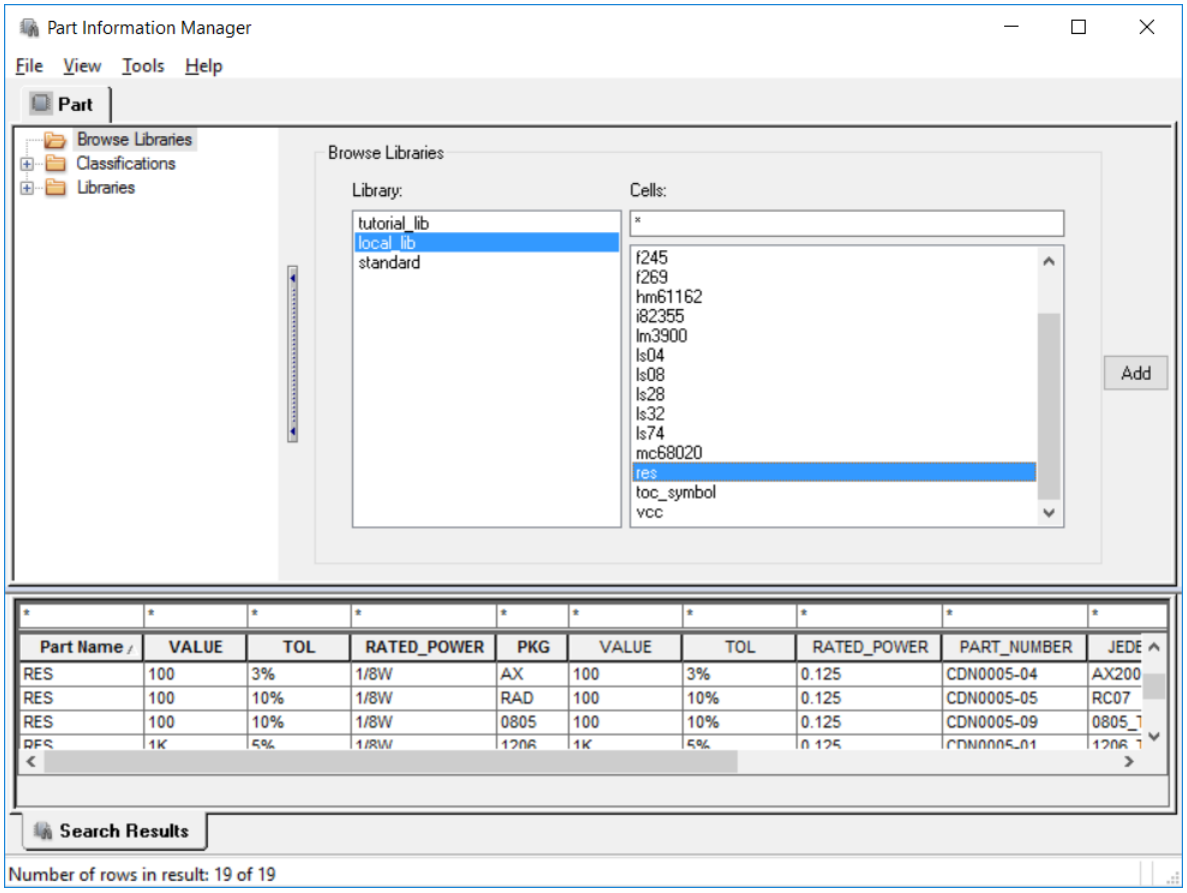
In this section, you will add a resistor and its physical information to the schematic design.

1. Choose *Component – Add*.

   Part Information Manager appears.

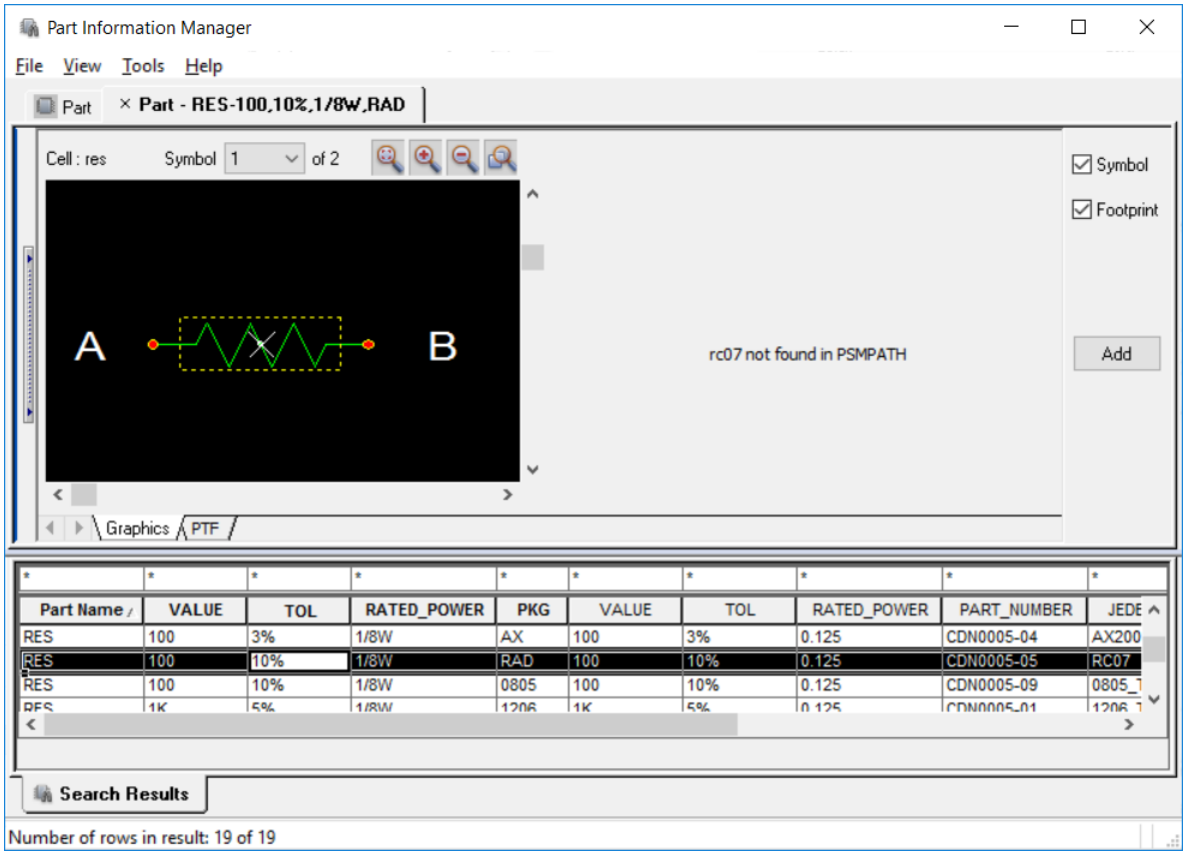
2. Select `local_lib` as the library.

3. Select `RES` from the Cells list and note the physical part filter.



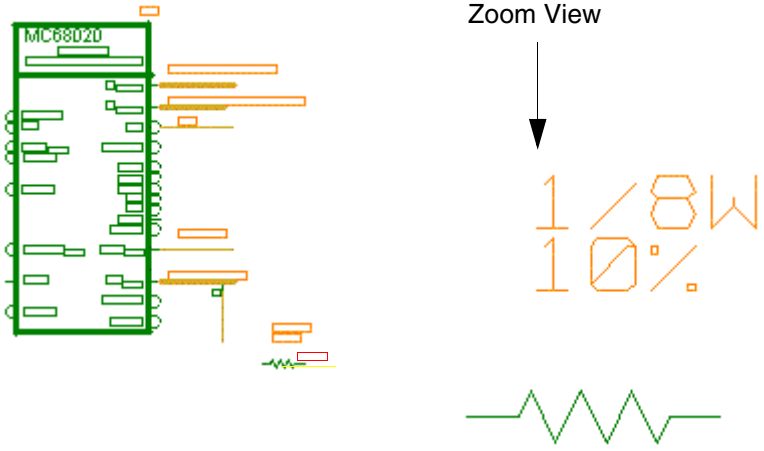
While creating the schematic design, for optimum performance, the resistor value should be 100 ohms and the tolerance limit should be 10%.

4. Select the required row from the physical part filter as shown in the following figure:

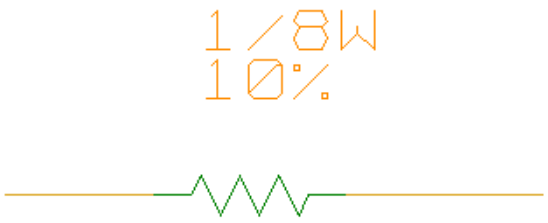


5. Click the *Add* button.

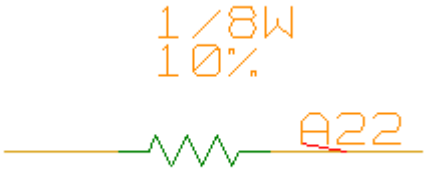
6. Click the design window to place the part with the physical properties as shown in the following figure:



7. Add wires to `RES` as shown in the following figure:



8. Specify `A22` as the signal name.

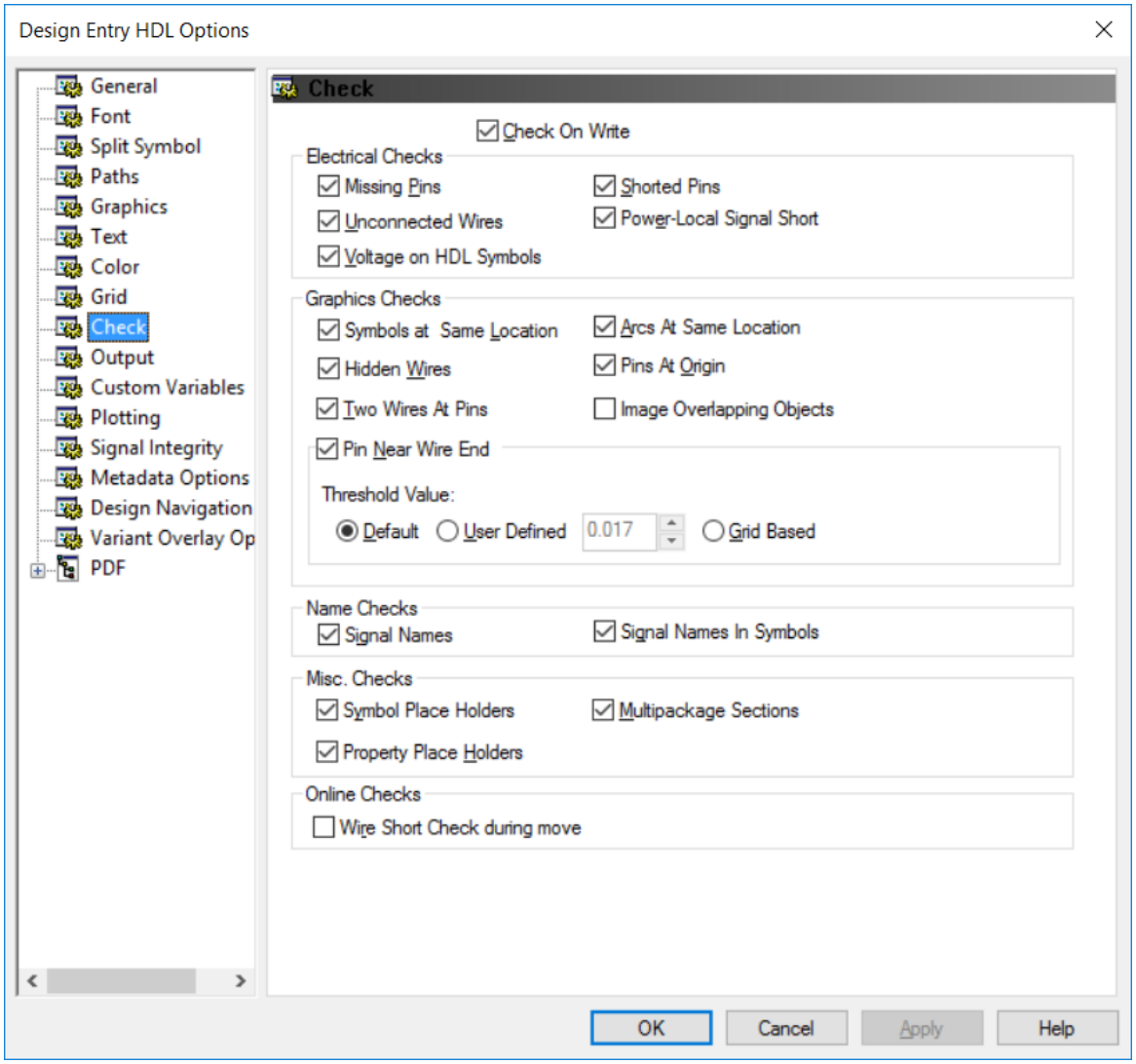


Saving and Viewing Errors

Design Entry HDL runs various checks, such as electrical checks, graphic checks, and name checks, before saving the schematic design. You can change the default settings and specify the checks that should be performed by Design Entry HDL while saving any schematic.

1. Choose *Tools – Options – Check* to view the default settings or to change the settings.

   The Design Entry HDL Options dialog appears.



Note: Design Entry HDL performs various checks before saving a schematic because, by default, the *Check On Write* check box is selected. If you deselect this check box, Design Entry HDL will not perform any checks when saving schematics.

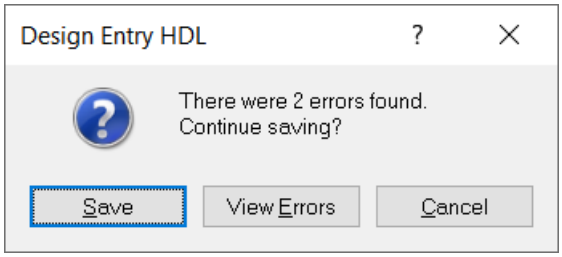
For this tutorial, do not change the default settings.

2. Click *OK* to close the Design Entry HDL Options dialog.

   In addition to the checks available at *Tools – Options – Check*, Design Entry HDL also runs another set of checks for connectivity errors.

3. To save the schematic, choose *File – Save*.

   The Design Entry HDL dialog box appears.

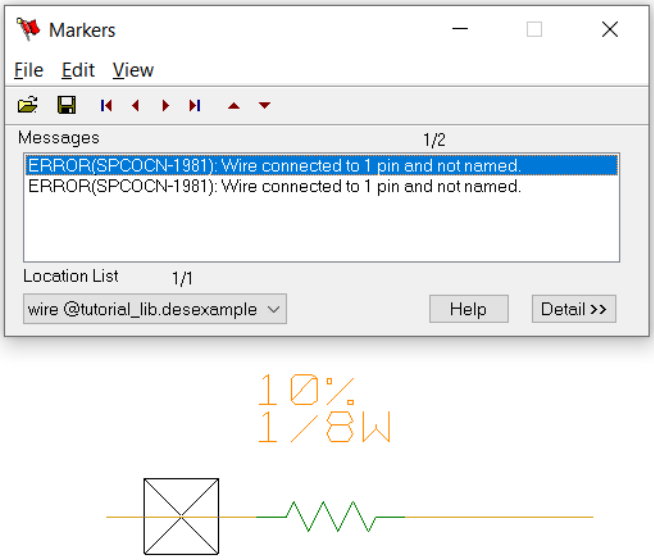


4. Click *View Errors*.

   The Markers dialog box appears displaying the errors.

5. Select the first error.

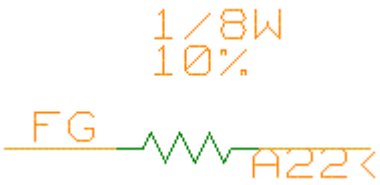
   Design Entry HDL highlights the location of the error in the schematic.



   This error is a result of an unnamed wire. Name the wire.

6. Choose *Wire – Signal Name*.

7. Name the unnamed wire as FG.



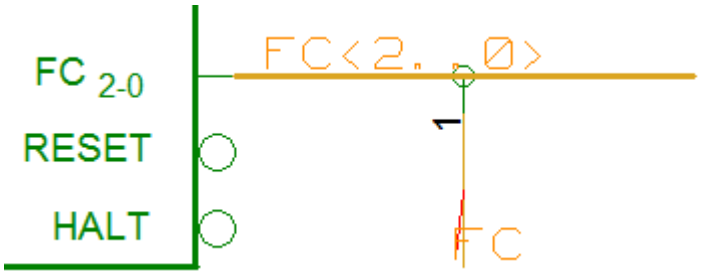
8. Select the second error.

   Design Entry HDL highlights the location of the error in the schematic.

   This error is also the result of an unnamed wire.

   Note: If the tap signal is connected to a component, Design Entry HDL automatically names it. In the preceding design example, the signal is not connected to any pin, so it must be named.

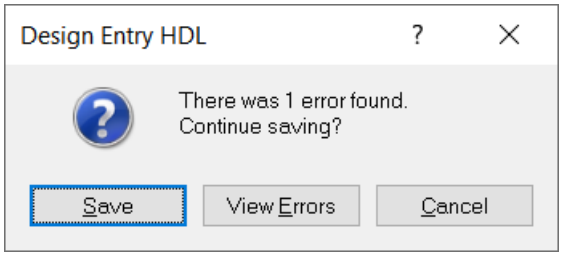
9. Choose *Wire – Signal Name* to name the wire as FC as shown in the following figure:



10. Click *File – Close* in the Markers dialog box.

11. Choose *File – Save* again.

    Design Entry HDL runs a check for connectivity errors and reports them.



12. Click *View Errors*.

    The Markers dialog box appears displaying connectivity errors.

13. Select the first error.

14. Choose *Text – Change* and change the wire name of *FC* to `FC1`.

15. Select the next error.

Design Entry HDL highlights the location of the error in the schematic.

This error occurred because a 16-bit bus is connected to a 32-bit pin.

16. Choose *Text – Change*.

17. Click `DATA<15..0>` and change it to `DATA<31..0>`.

18. Press Enter.

19. Choose *File – Close* to close the Markers window.

20. Choose *File – Save* to save the design.

Design Entry HDL saves the design you created without any errors.

4

Enhancing the Schematic

Overview

This chapter contains the following information:

Important

Remember to follow the steps in this tutorial in a sequential order.

Working in the Windows Mode

Design Entry HDL has an added feature to support common Windows commands and operations. The Windows mode provides support for common Windows operations in Design Entry HDL, such as cut, copy, paste, deleting schematic objects, and reorganized menus that conform to Windows standards.

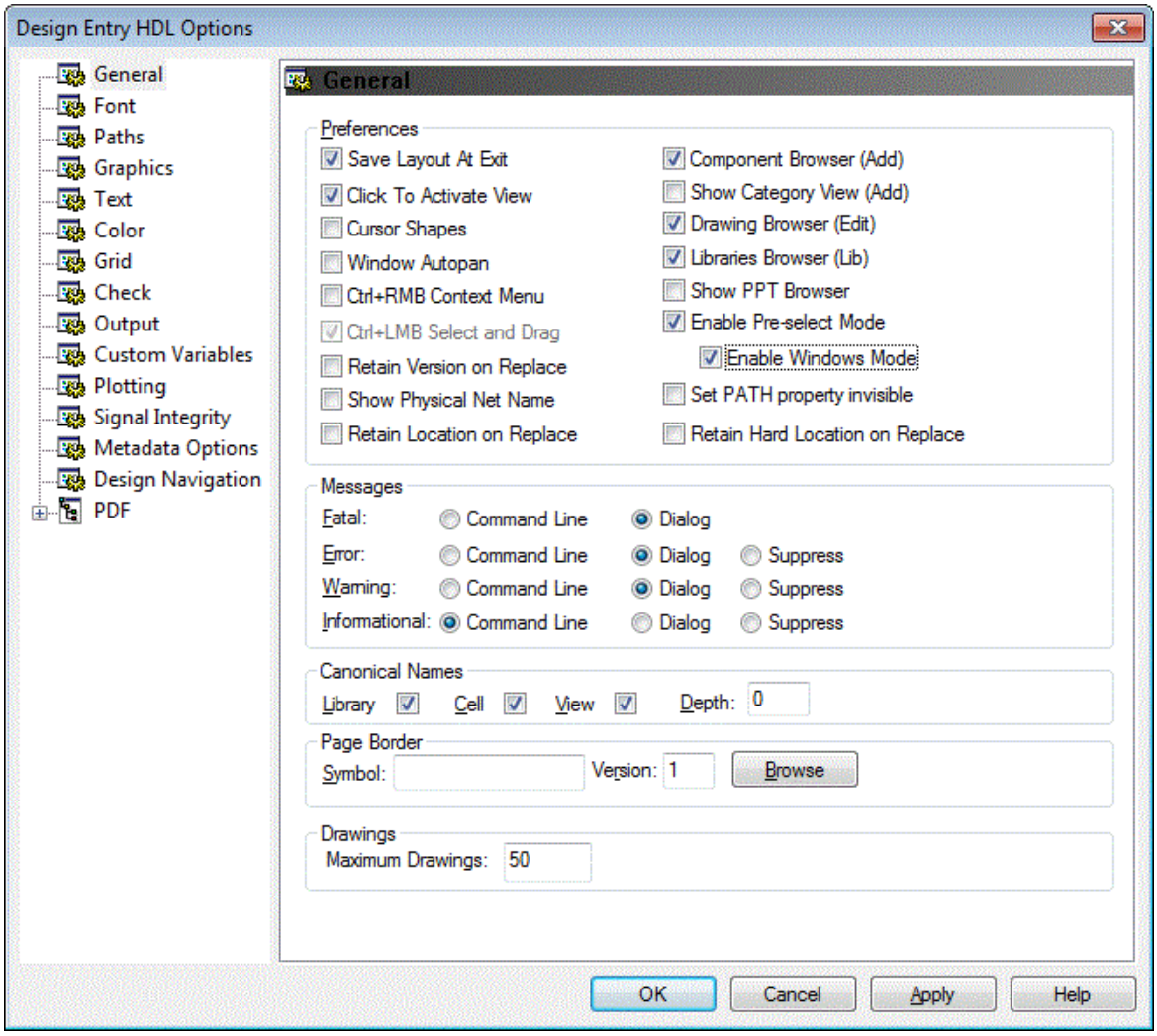
Enabling the Windows Mode

When you open Design Entry HDL, the Windows mode is disabled by default. To enable the Windows mode, do the following:

1. Choose *Tools – Options*.

   The Design Entry HDL Options dialog appears.

2. On the General tab of the Design Entry HDL Options dialog, select the *Enable Pre-select Mode* check box in the Preferences section.



3. Click *OK* to save the settings and close the Design Entry HDL Options dialog.

   As soon as you select the *Enable Pre-select Mode* check box, the *Enable Windows Mode* check box is enabled allowing you to switch to the Windows mode of Design Entry HDL.

Note: For more information on the Windows mode, refer to *Allegro Design Entry HDL User Guide*.

4. Uncheck the *Enable Pre-select Mode* box in the Preferences section to move out of the Windows mode. The following sections describes instructions for the non-Windows mode.

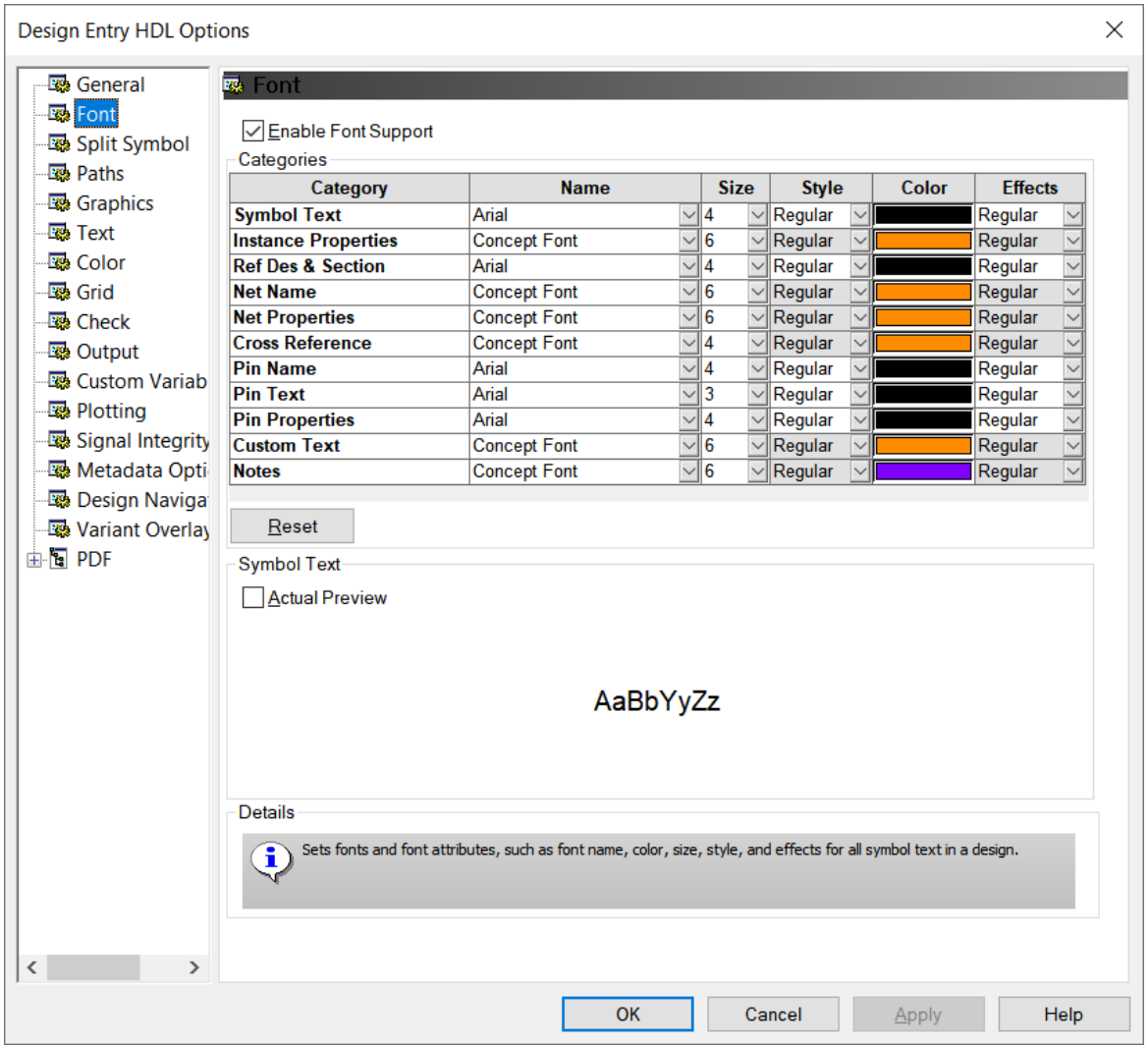
Support for Fonts

DE-HDL includes support for different fonts. This feature allows you to set fonts for different categories of text objects.You can set fonts and font attributes, such as font name, color, size, style, and effects, for a category of text objects. You can change these values using the Font tab.

Enabling Fonts

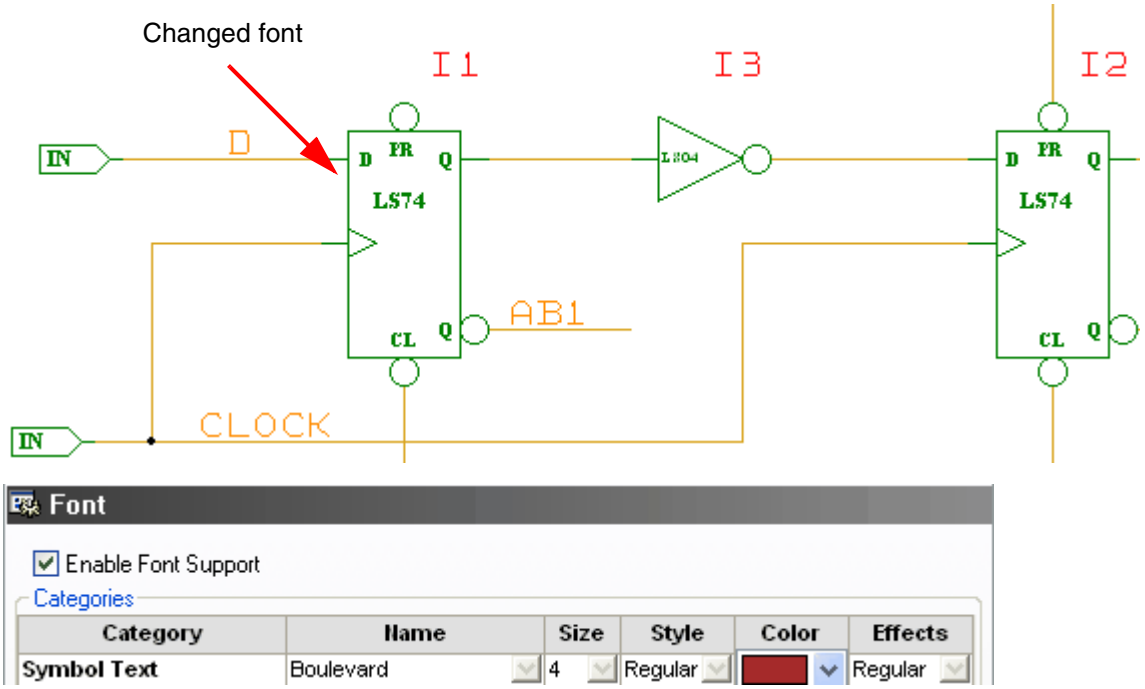
1. Choose *Tools – Options*.
2. In the Design Entry HDL Options dialog, choose *Font*.

In the Fonts page of the Design Entry HDL Options dialog, you can specify font attributes for different types of schematic text objects. The *Enable Font Support* box is checked by default to support the display of different fonts.



3. To change the font of the pin name, select *Times New Roman* from the font list.
4. Click *Apply* after you select the font.
5. Click *OK* to close the dialog.

   The pin names reflect the changed font.
6. To change the font color, select the color red from the drop-down list.
7. Click *Apply* after you set the color preference.



8. Click *OK* to close the dialog.

Note: When you open a pre-16.3 design, text objects are rendered in the selected fonts and attributes. However, since there is no change in the database, the font color and size for existing objects do not change.

Note: For more information on support for fonts, see the *Support for Fonts* section in *Allegro Design Entry HDL User Guide*.

Publishing a PDF

After creating your schematic designs, you can publish and view them in a Portable Document Format (PDF). Allegro Design Publisher (the publish PDF utility) helps you share complex schematic designs with experts who might not have Design Entry HDL installed on their systems. You can view the design on any platform, as PDF documents are viewable on almost any platform.

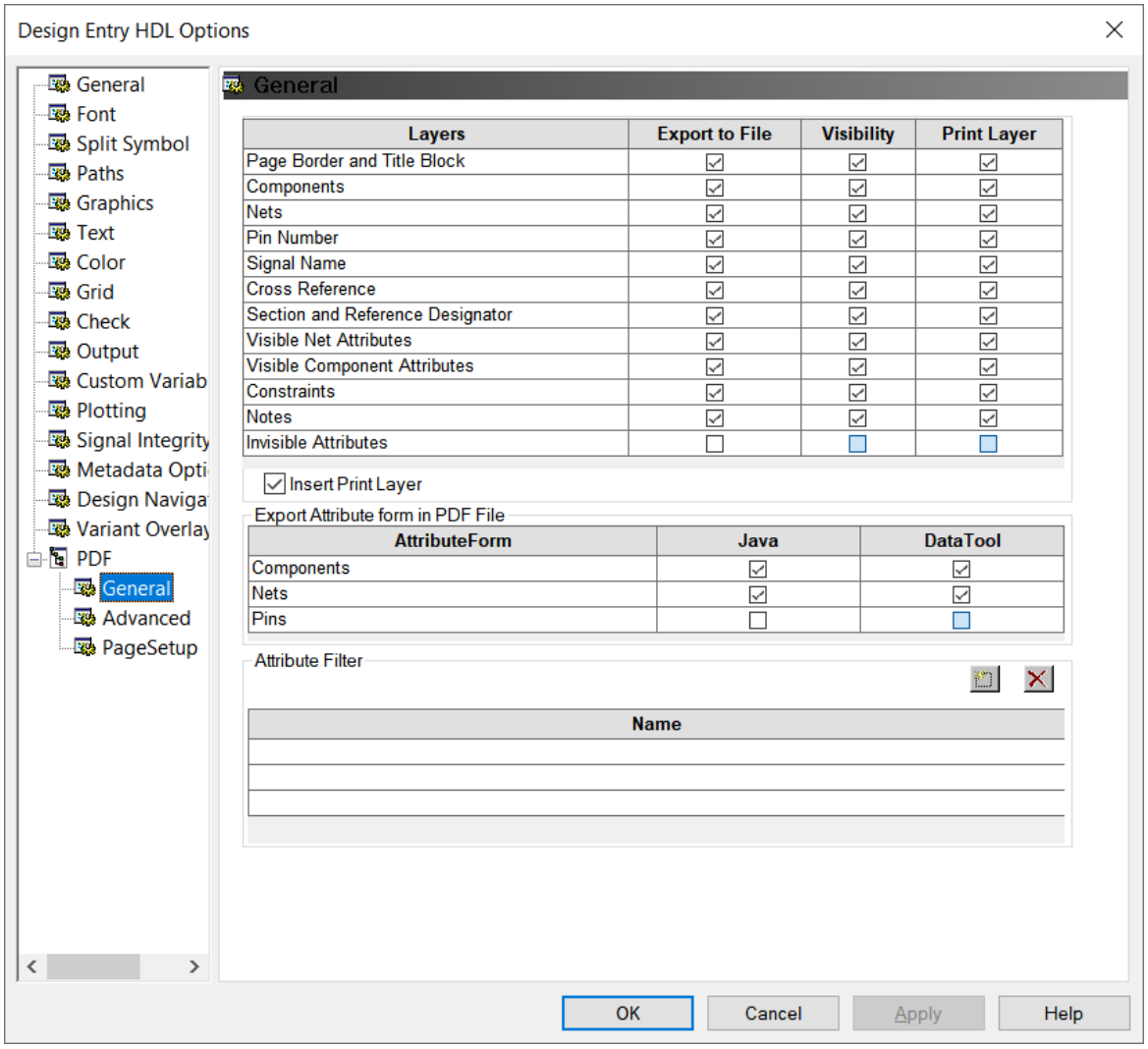
Setting up Preferences for Publishing

Before you publish a PDF document of a schematic, you can set preferences to specify what information is to be exported to the PDF document. You can set the preferences in the Design Entry HDL Options dialog.

To set PDF preferences, do the following:

1. Choose *Tools – Options*.
2. Expand the *PDF* option on the left pane.
3. Click *General*.

The Design Entry HDL Options dialog appears where you can set *General* and *Advanced* options.



Note: You can also set PDF options in the Publish PDF dialog, which you can access from *File – Publish*.

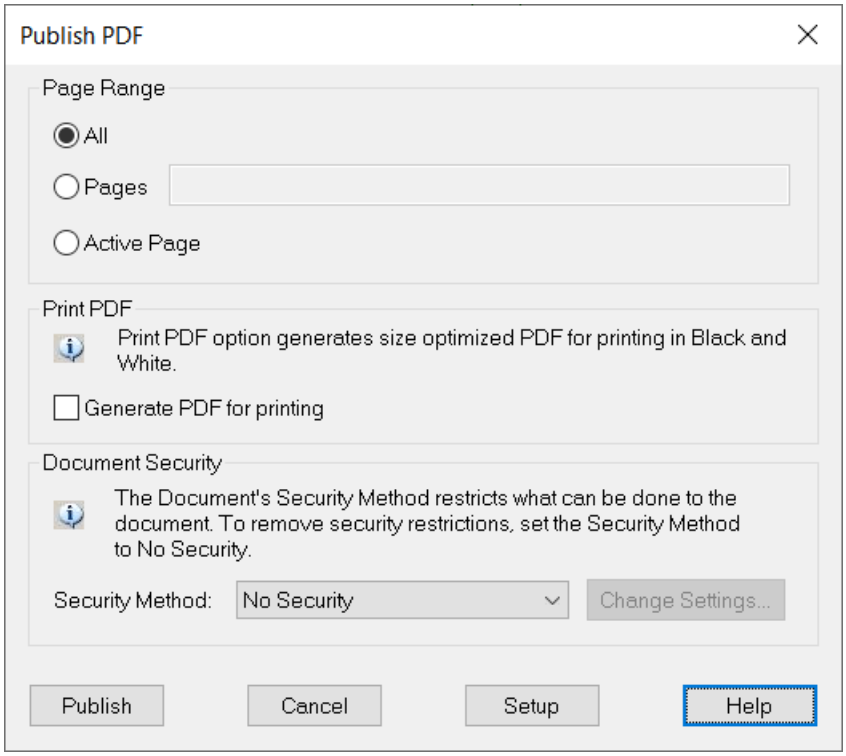
4. Click *OK*.

Publishing the PDF

After setting up the required preferences for exporting information, you can publish the schematic design as a PDF document. To publish a PDF document of a schematic, do the following:

1. Choose *File – Publish PDF*.

   Publish PDF appears.



2. Select the *Pages* option in the *Page Range* section and specify the page range as `1 to 2`.

   You can choose to print the entire schematic, a specified range of schematic pages (n-m), comma-separated page numbers (n, n), or just the currently active page.

3. Select the *Generate PDF for printing* option, to publish the document in a printable, black and white format.

   You can specify Document Security options to restrict access to the document. The default security method is *No Security*. Retain the default settings.

Note: For more information on security settings, see *Allegro Design Publisher User Guide*.

4. To make changes to the PDF setup, click the *Setup* button.

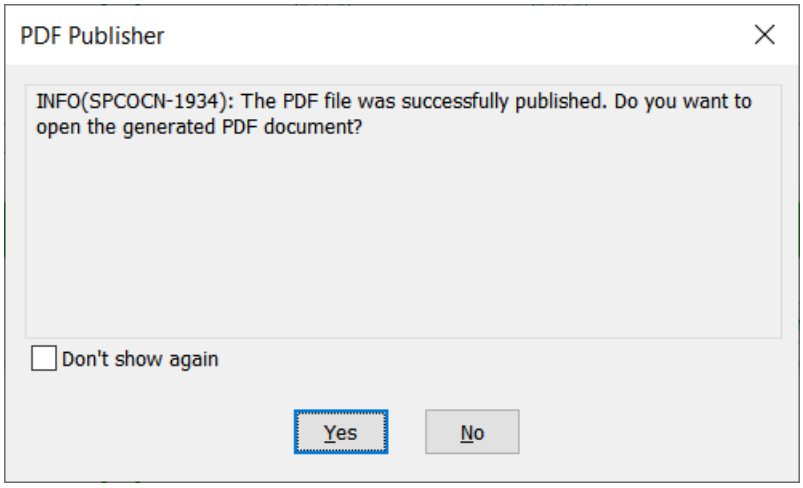
   The PDF Setup dialog appears, which is effectively the same as the PDF tab of the Design Entry HDL Options dialog. Close the PDF Setup dialog.

5. Click *Publish.*

6. Specify the location as the `designs` folder on the `D:\` drive.
7. Specify the name as `super_design` in the *File name* field to save the published PDF document.
8. Click *Save*.

   A progress dialog box appears showing the progress of the PDF document being published.

   After successful generation of the PDF document, a message appears which prompts you to view the published PDF document:



9. Click *Yes* to view the PDF.
10. The PDF opens with only two pages as specified in the page range section.

    The PDF opens in black and white only because you selected the *Generate PDF for printing* option.

Note: You will only be able to generate a PDF file if you have a PDF publishing license. For details on generating a PDF file for a design, see *Allegro Design Publisher User Guide.*

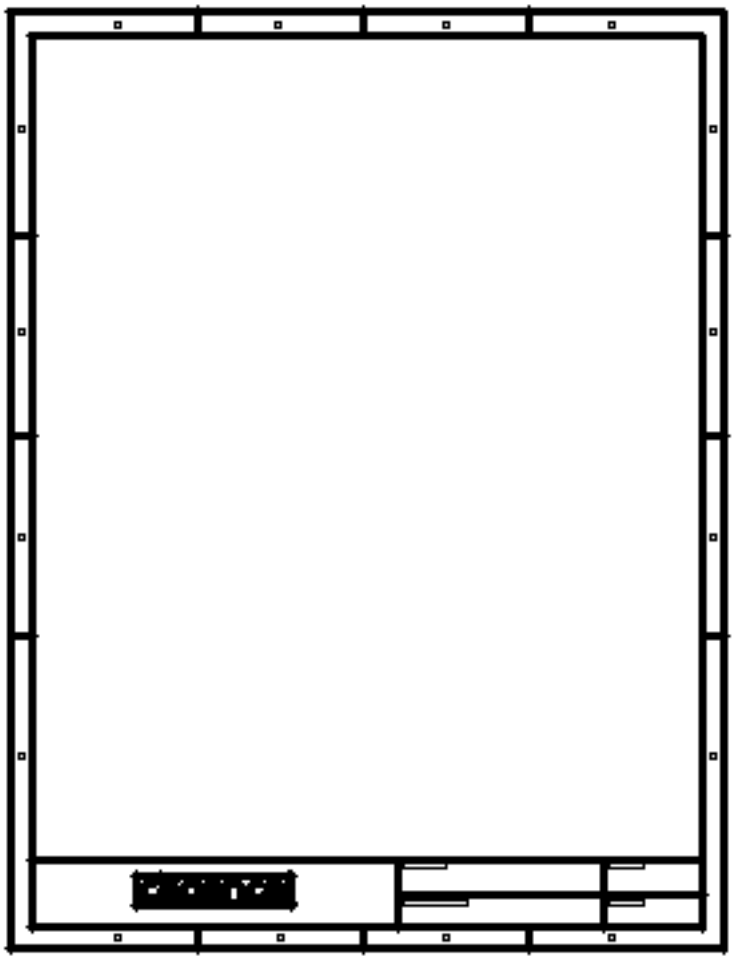
Adding a Table of Contents

Design Entry HDL provides functionality for creating and automatically updating the table of contents (TOC) with design information. You can create a custom TOC symbol for your design and instantiate the symbol in your design. For this tutorial, you will first create a TOC symbol. You will then instantiate the symbol in the design. The TOC will be automatically updated with relevant information from the design.

Creating a TOC Symbol

1. Select a sheet with a page border in Hierarchy Viewer. For example, select page 1.
2. Double-click the page border.

   The symbol displays.



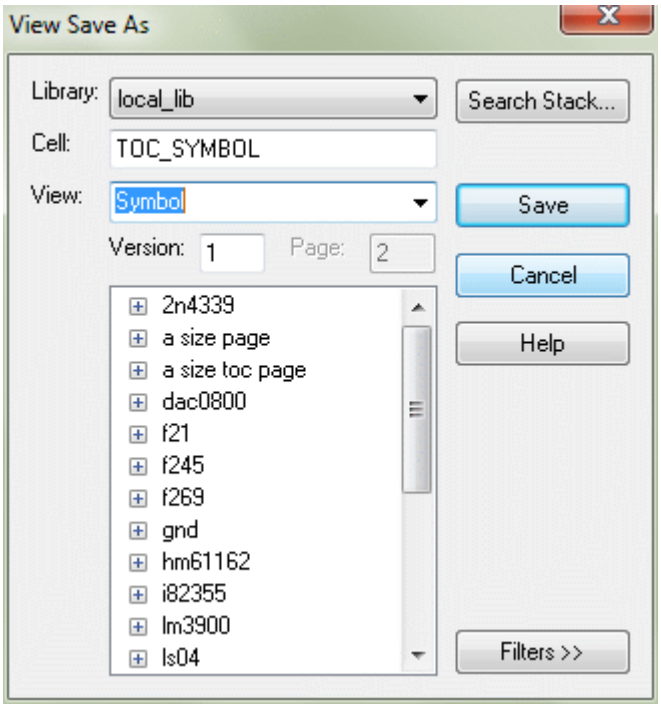
3. Choose *File – Save As* to save the symbol.

   The View Save As dialog appears.

4. Select *local_lib* from the *Library* drop-down list.

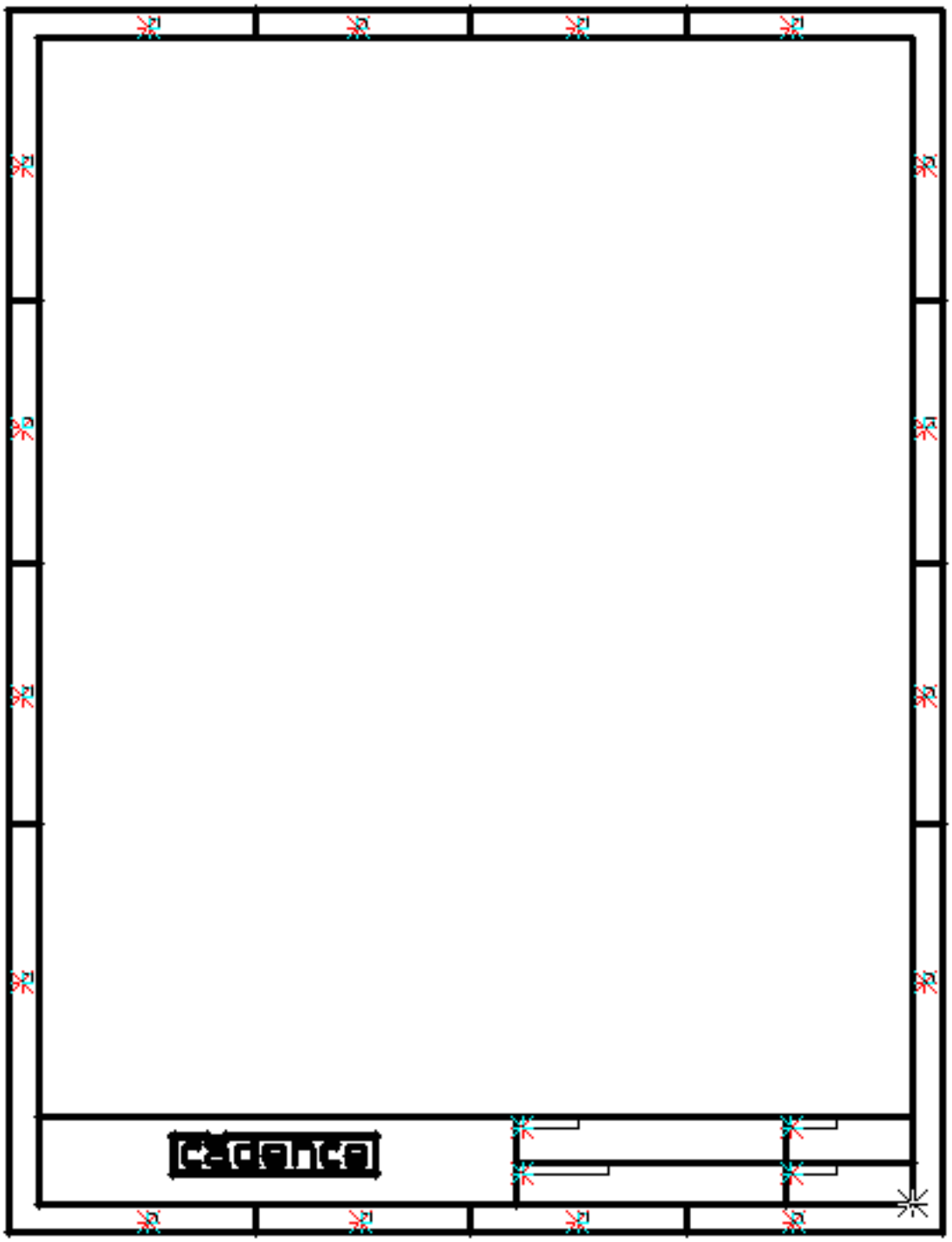
5. Type `TOC_SYMBOL` in the Cell field.

6. Select *Symbol* from the *View* drop-down list.



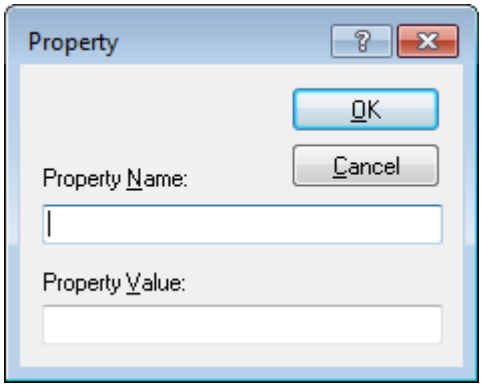
7. Click *Save* to save the TOC Symbol.

8. Choose *Display – Origins* to display the origin of the symbol.



9. Set the `TOC_SYMBOL` property to `TRUE` and attach it to the origin of the symbol by doing the following:

a. Choose *Text – Property*.

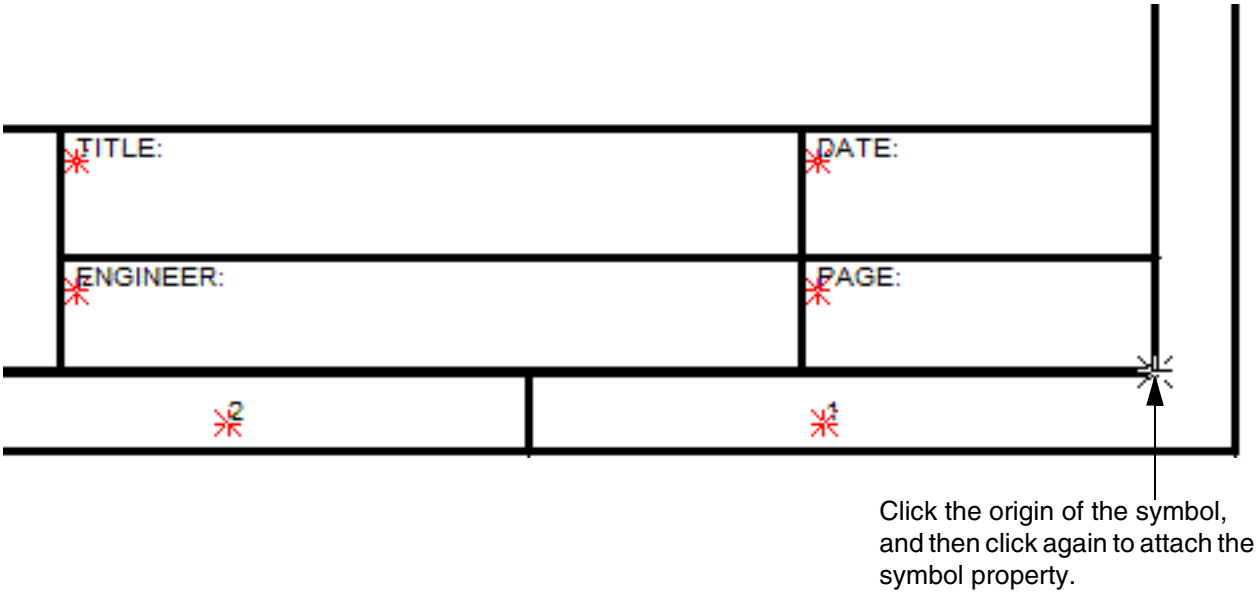


b. Type `TOC_SYMBOL` in the Property Name field.

c. Type *TRUE* in the Property Value field.

d. Click *OK*.

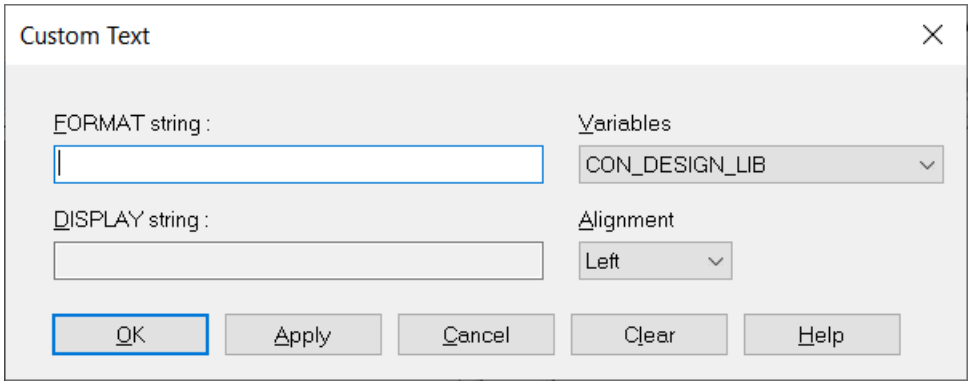
10. Click the origin of the symbol, and then click again to attach the symbol property.



11. Choose *File – Save* to save the symbol.

12. Choose *Text – Custom Text*.

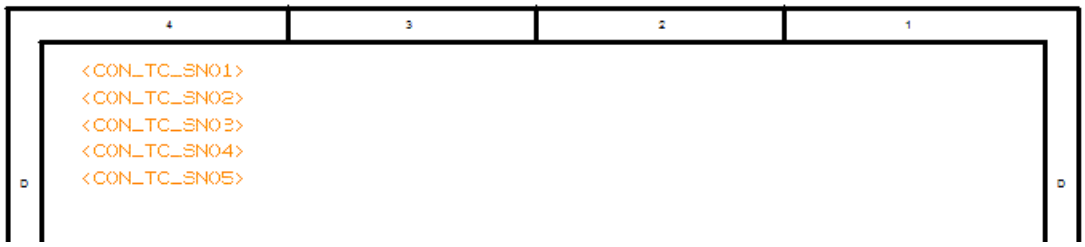
13. In the Custom Text dialog box, select *CON_TC_SNO* from the *Variables* drop-down list. To ensure that <CON_TC_SNO> displays in the *FORMAT string* field, you may have to click the *Clear* button then select CON_TC_SNO from the *Variables* drop-down list.



14. Enter 5 in the Repeat field.

15. Click *OK* and return to the sheet.

16. Click on the top left part of the sheet, and click again to place the custom text variable. Based on the repeat count specified in the Custom Text dialog box, the custom text entries are added to the symbol one below the other.



17. Similarly, add the CON_TC_SNM and CON_TC_BNM custom variables to the TOC symbol:

a. Choose *Text - Custom Text*.

b. Click the *Clear* button.

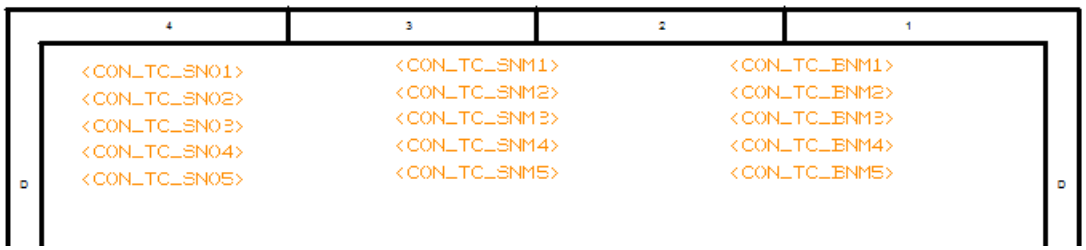
c. Select the CON_TC_SNM variable.

d. Enter 5 in the Repeat field.

e. Click *OK* to return to the sheet.

f. Place the custom text variable next to the CON_TC_SNO variable.

g. Repeat steps `a` to `e` to add the `CON_TC_BNM` variable to the TOC symbol.



18. Choose *File – Save*.

19. Exit Design Entry HDL.

Instantiating the TOC symbol in the Design

You can now instantiate this symbol in a schematic.

1. Launch Design Entry HDL.

2. In the schematic, insert a new sheet before page 1.

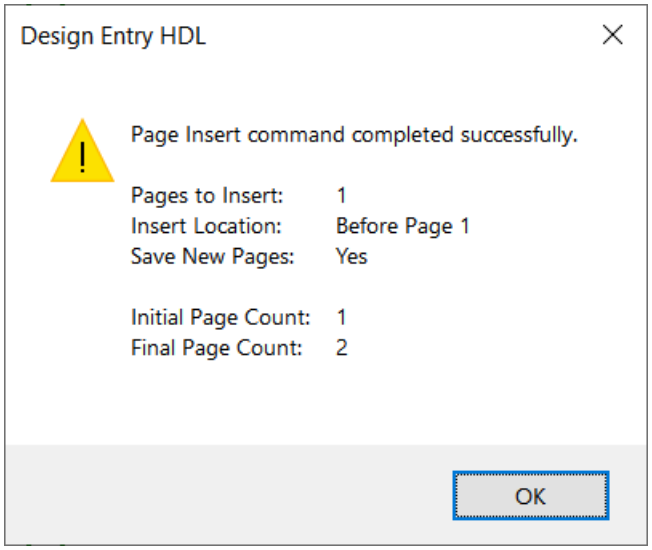
h. Click sheet 1 in Hierarchy Viewer.

i. Choose *File – Edit Page/Symbol – Insert Page*.

j. Click *OK* when prompted to insert the new page before page 1.

k. Click *OK*.

l. Click OK in the resulting message box.



The sheet opens with the default page border.

3. Replace the page border with the TOC symbol.

a. Right-click on the symbol (page border of the new page) and choose *Replace* from the pop-up menu.

b. In the Replace Component dialog box, select *local_lib* from the list of libraries.

c. Select *toc_symbol* in the Cells list.

d. Click the *Replace* button.

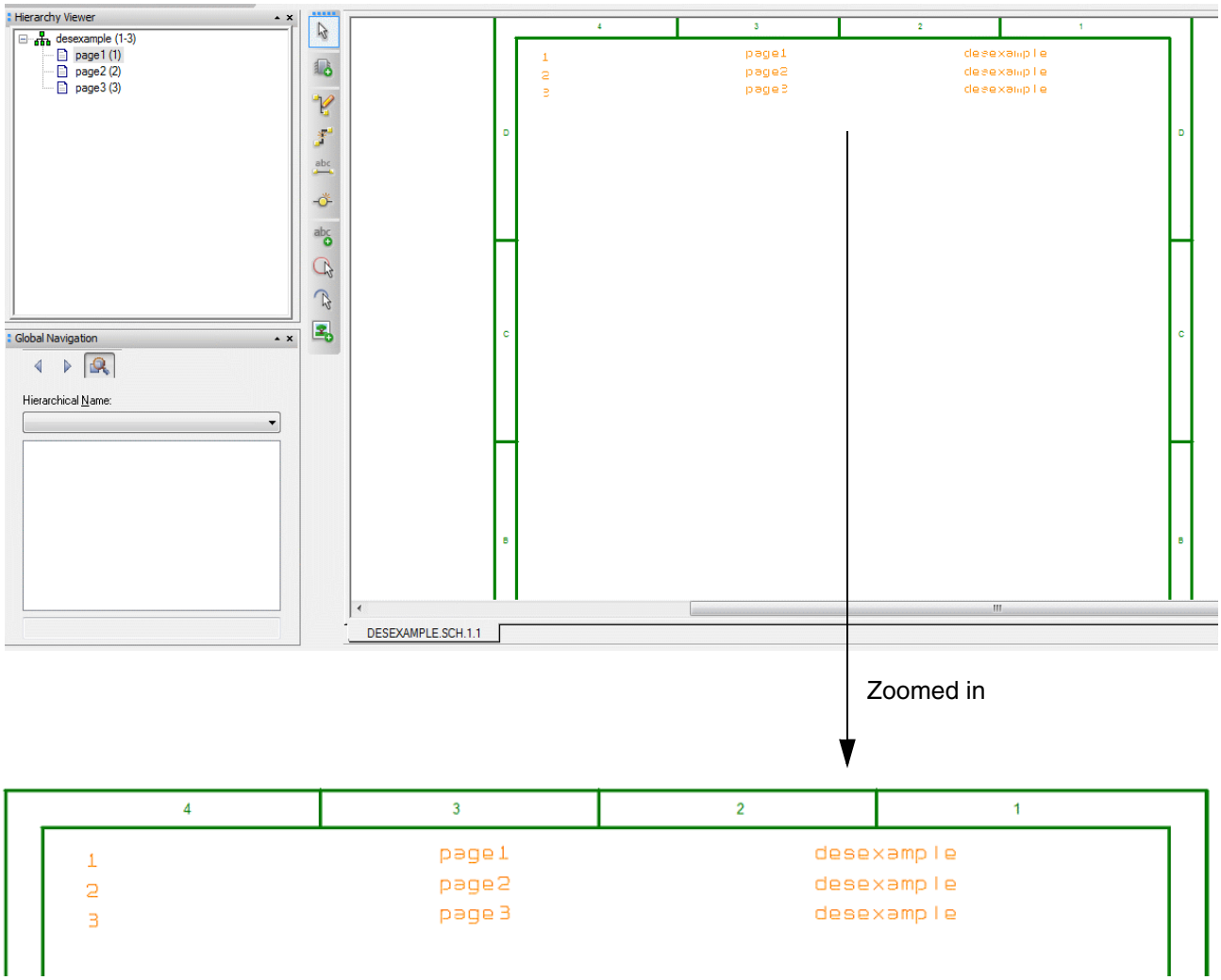
e. Click on the border of the new page in the schematic canvas.

f. Right-click and choose *Done* from the pop-up menu.

4. Choose *File – Save* to save the design.

Note: A message box may display with netlisting errors. Close the box. The error will be

addressed as you proceed with the steps.



The TOC is updated with the relevant page information. Note that you had added five TOC rows. However, only three rows are displayed here. This is because the tutorial design currently contains only three pages. As you add more pages to the design, you can add more rows to the TOC symbol and the TOC of the design is automatically updated.

5

Creating a Schematic: Advanced

This chapter contains the following information:

Using Groups

When you have multiple objects, such as parts and wires, that you want to move, copy, or perform other edit operations on, you can enclose them in a group and perform the operations on all of the objects together in the group. Groups are useful when you want to perform a single task on multiple objects.

Design Entry HDL provides the following three methods for creating groups:

- By Expression
- By Rectangle
- By Polygon

To create a group, you first need to open the schematic design. Run Project Manager, and load the tutorial project. When you open the project in Design Entry HDL, `DESEXAMPLE.SCH.1.1` is displayed. Navigate to `DESEXAMPLE.SCH.1.2` of the design.

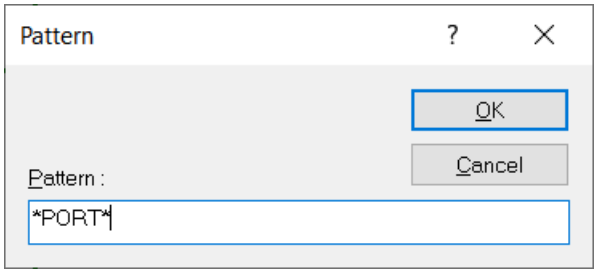
Creating a Group By Expression

In this session, you will create a group of all objects in the schematic that have the text string `PORT` in their name.

1. Choose *Group – Create – By Expression*.

   The Pattern dialog box appears.

2. Type `*PORT*` in the *Pattern* field.



3. Click *OK*.

   Design Entry HDL highlights all objects in the schematic that include the text PORT in their names.

   By creating groups, you can delete, copy, or move multiple objects with PORT in their name in a single step.

4. To delete all objects in a group, choose *Group – Delete*[A].

   In this case, Design Entry HDL deletes all the objects in the schematic that include the text PORT in their names.

5. Choose *Edit – Undo* to reverse the deletion.

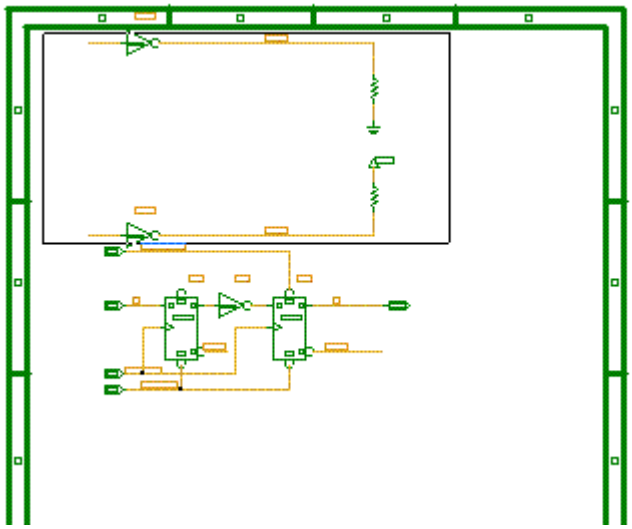
   Design Entry HDL places all the deleted objects back in their original positions in the schematic.

Creating a Group By Rectangle

The second method of creating a group is to select a part of the schematic design. The selection is done by drawing a rectangle. The part of the schematic design that is enclosed by the rectangle forms a group.

1. Choose *Group – Create – By Rectangle*.
2. Click at the start of the area in which you want to select the objects. Drag the mouse to the end of the area. Click again to stop drawing the rectangle.

   The part of the schematic design within the rectangle is highlighted in red.



3. To move the objects in the group to a different part in the schematic design, choose *Group – Move*[A].

   The selected group attaches to the cursor.

4. Click a location in the schematic to place the group.
5. Right-click and choose *Done*.

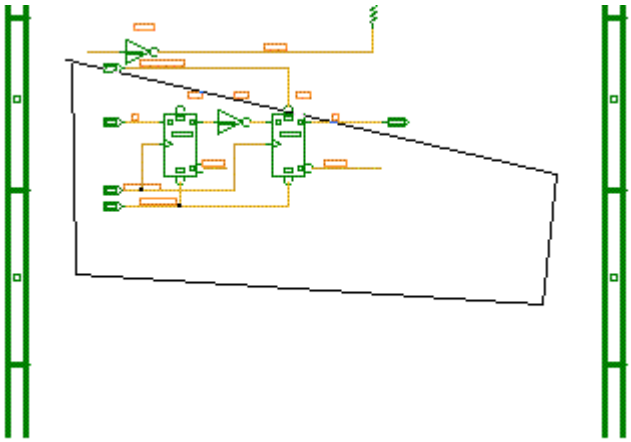
6. Choose *Edit – Undo* to reverse the move.

   Design Entry HDL places all the moved objects back in their original positions in the schematic.

Creating a Group by Using a Polygon

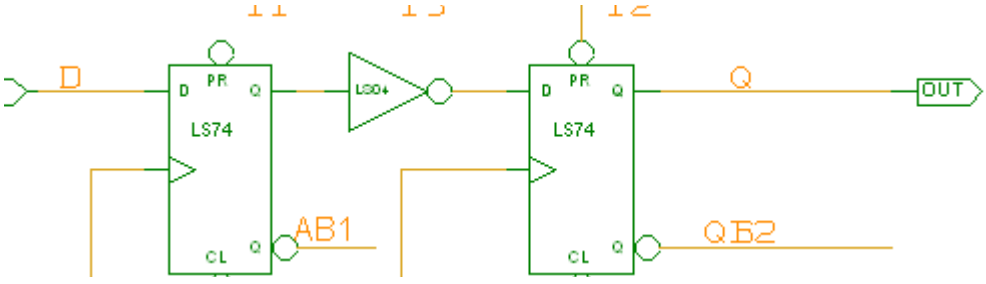
If a part of the schematic design cannot be enclosed within a rectangle, you can create a group by drawing a polygon that encloses the required part of the schematic.

1. To create a group by drawing a polygon, choose *Group – Create – By Polygon*.
2. Click, release the left mouse button, and click again to draw one side of the polygon.
3. Complete the polygon as shown in the following figure.



4. Right-click and choose *Done*.

   The part of the schematic design within the polygon is highlighted in red.



You can now copy, move, and delete, the group.

Creating Hierarchical Designs

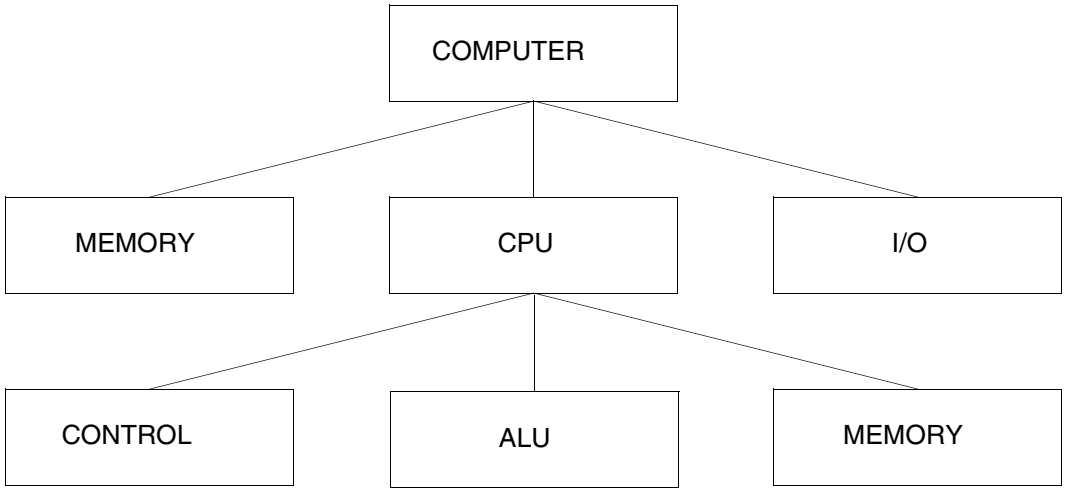
Use the hierarchical design technique to develop complex designs that comprise many modules. This method is useful for designs that reuse many of the same circuit functions, and for isolating portions of the design for teamwork assignments.

A hierarchical design results in print sets that are easy to read and the design produces modules that can be effectively debugged. Hierarchical designs, such as structured designs, reduce the amount of data entry and interconnections required by the design, thereby reducing the chances for errors. Creating a hierarchical design is a natural extension of the entire design process.

For example, if the design to be implemented is a computer, you begin the design by planning the parts of the computer. The computer can be divided into the CPU, MEMORY, and I/O modules. The CPU module can be further divided into the ALU, MEMORY, and CONTROL modules.

This represents three levels of hierarchy in the design. There are no limits to the number of levels you can include in a hierarchical design.

Figure 5-1 Levels of Hierarchy



To create a hierarchical design in Design Entry HDL, choose any of the following methods:

- Top down
- Bottom up

The Top-Down Method

In the top-down method, you visualize the design at a high level of abstraction. The schematic that represents this high-level of abstraction contains blocks that logically divide the design into subdesigns.

After the top-level design (also called the root design) is created with all the blocks, you create schematics that correspond to each block in the top-level schematic. These schematics can also have blocks that represent further logical divisions represented by lower-level schematics.

Use the top-down method when you clearly understand all aspects of the design. Before you create the design, you should know the interface signals with their directions (in, out, and inout).

Consider the computer example (see Levels of Hierarchy). In such a situation, to use a top-down approach, you start by creating the top-level schematic for COMPUTER. In this schematic, add blocks named MEMORY, CPU, and I/O. After naming these blocks, create schematics named MEMORY, CPU, and I/O.

In the CPU schematic, create three blocks: CONTROL, ALU, and MEMORY. After creating these blocks, create three corresponding schematics named CONTROL, ALU, and MEMORY.

Double-click a block in Design Entry HDL to descend into a lower level schematic. To ascend to a higher-level schematic, choose *File – Edit Hierarchy – Ascend*.

The Bottom-Up Method

In the bottom-up method, you create the schematics at the lowest level of the hierarchy. After the schematic is created, a symbol view is generated for this schematic by using `Genview` (Choose *Tools – Generate View* in Design Entry HDL). This symbol is instantiated (placed) on a schematic at a higher level in the hierarchy.

Continuing with the computer example (Levels of Hierarchy), here is how the bottom-up method would be applied. You would first create the schematics for the CONTROL, ALU, and MEMORY functions. After creating the schematics, you would use `GenView` to generate symbol views for each one of them.

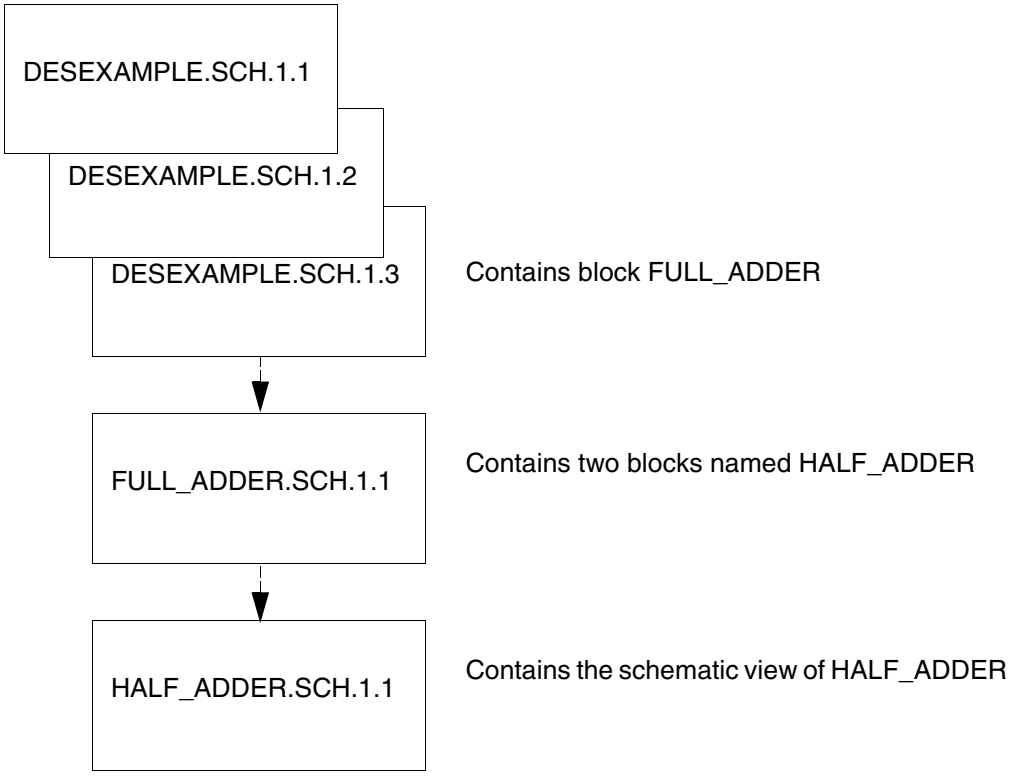
Next, you would need to create the schematics for the subdesigns MEMORY, CPU, and I/O. In the schematic for CPU, instantiate the symbols for CONTROL, ALU, and MEMORY.

After the schematics at this level of hierarchy have been completed, generate symbols for each one of them. These three symbols can be instantiated to create the schematic for COMPUTER.

Creating a Hierarchical Design by using the Top-Down Method

In this section, the design discussed in the previous section (Levels of Hierarchy) will be created by using the top-down structure. The following figure displays the structure of the design that will be created.

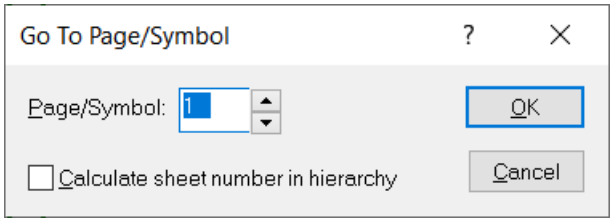
Figure 5-2 Design Structure



To implement the top-down approach for the Levels of Hierarchy design, do the following:

1. Open `DESEXAMPLE.SCH.1.1`.
2. Choose *File – Edit Page/Symbol – Go To*.

   The Go To Page/Symbol dialog box appears.

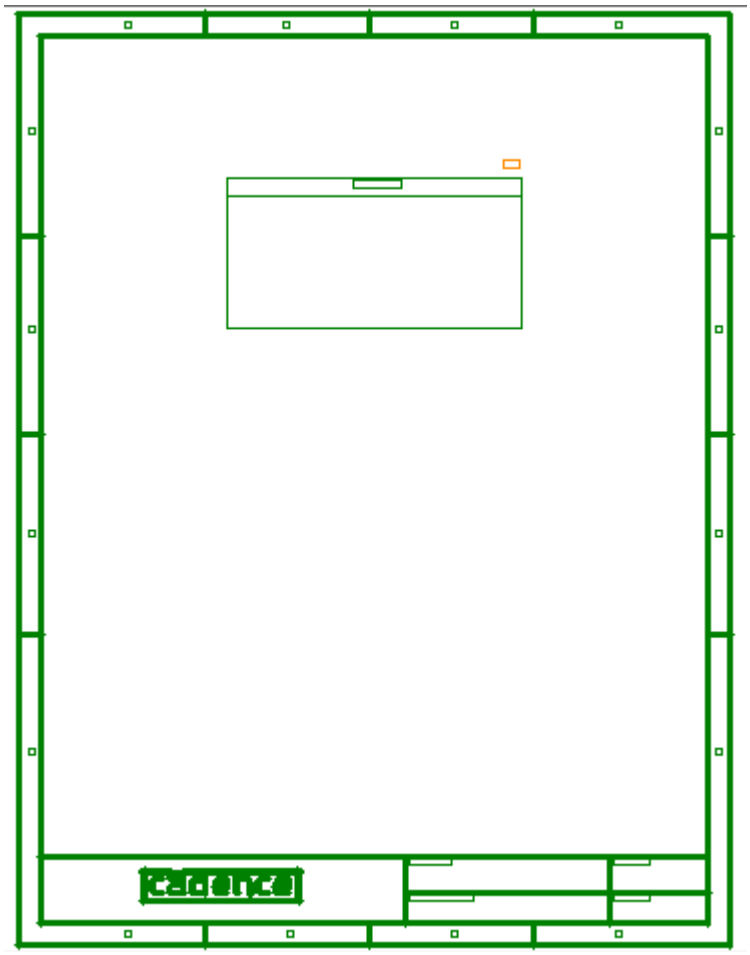


3. Enter `4` in the *Page/Symbol* field and click *OK*.

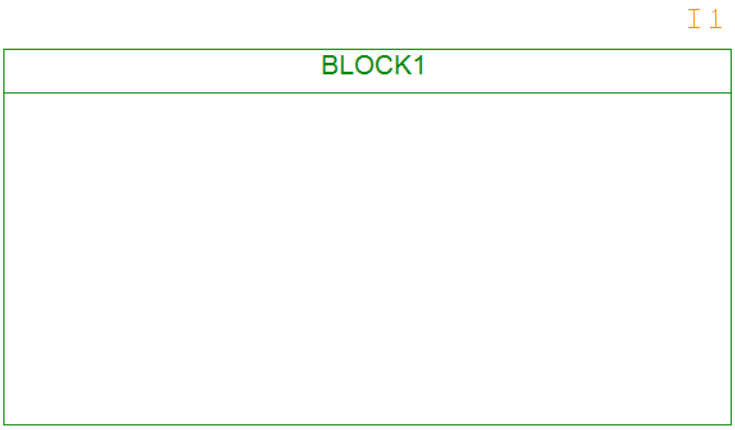
   Design Entry HDL prompts you for confirmation to create a new page.
4. Click *Yes*.

   Design Entry HDL opens a blank schematic page named DESEXAMPLE.SCH.1.4.
5. To add a block, FULL_ADDER, to the page, choose *Block – Add*.

6. Click in the schematic, release the left mouse button, and click again to create a rectangular block.



Design Entry HDL displays the block, and by default, names the block `BLOCK1`.



7. Right-click and choose *Done*.
8. Zoom into the block using the Zoom Points button.

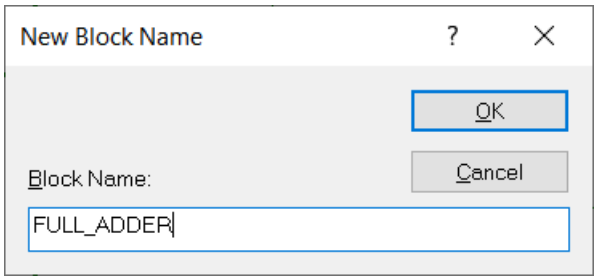
Renaming the Block

By default, the block is named `BLOCK1`.

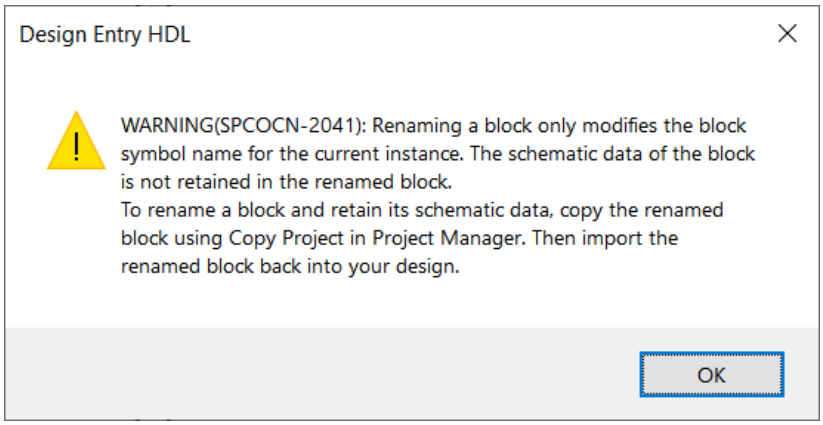
1. Choose *Block – Rename* to change the name of the block.

   The New Block Name dialog box appears.

2. Type `FULL_ADDER` as the block name and click *OK*.



Design Entry HDL attaches FULL_ADDER to the cursor. A warning message is displayed.

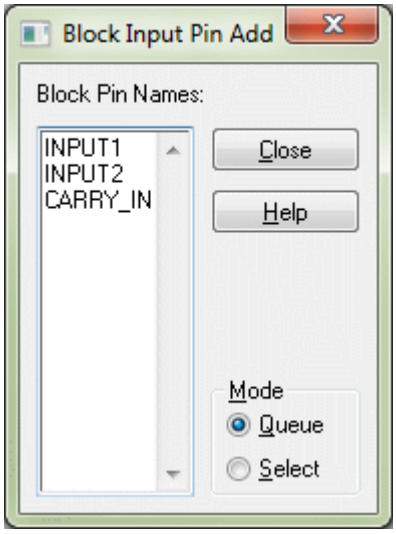


3. Click *OK.*
4. Click the default block name, *BLOCK1*.

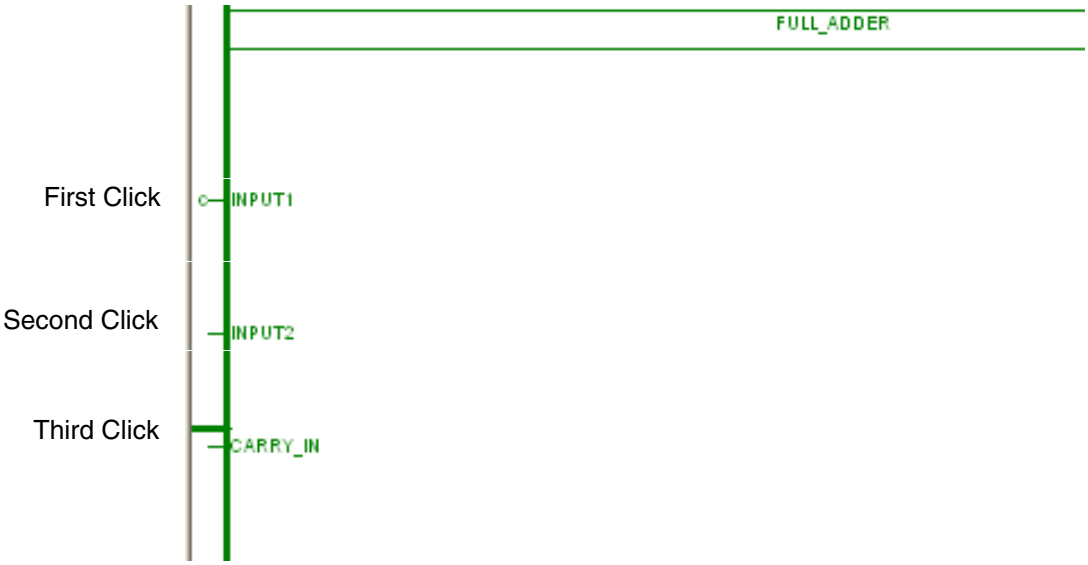
   Design Entry HDL replaces the block name `BLOCK1` with `FULL_ADDER`.
5. Choose *Block – Add Pin – Input Pin*.

   The Block Input Pin Add dialog box appears.

6. Enter the following as input pins:
   - ❑ INPUT1
   - ❑ INPUT2
   - ❑ CARRY_IN



7. Place the input pins on the block as shown in the following figure:



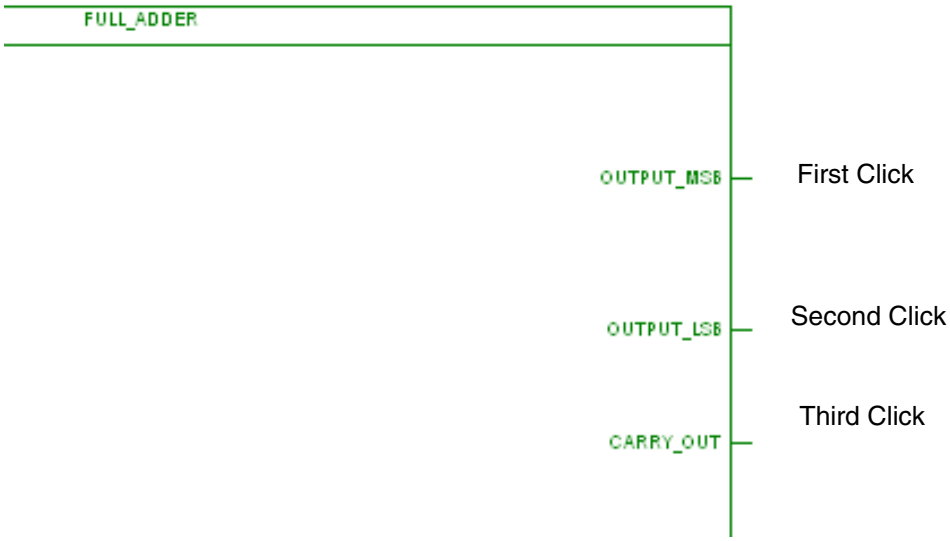
8. Click *Close* in the Block Pin Input Add dialog box.

9. Choose *Block – Add Pin – Output Pin*.

The Block Output Pin Add dialog box appears. In the dialog box, enter the following:

- ❑ OUTPUT_MSB
- ❑ OUTPUT_LSB
- ❑ CARRY_OUT

10. Click the block to add pins as shown in the following figure:



11. Click *Close.*

12. Choose *Wire – Draw* to add wires to the pins.

Add wires as shown in the following figure:

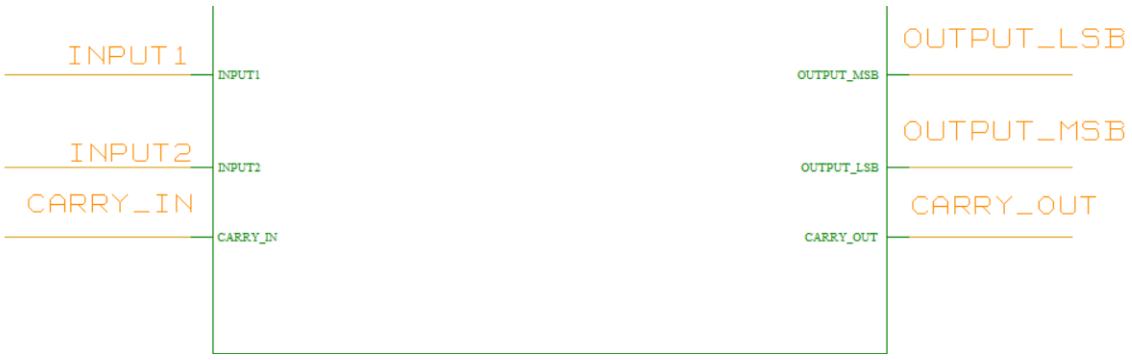
13. Choose *Wire – Signal Name*.

    The Signal Name dialog box appears.

14. Specify the following signal names:

    - INPUT1
    - INPUT2
    - CARRY_IN
    - CARRY_OUT
    - OUTPUT_MSB
    - OUTPUT_LSB

15. Click the wires to add the signal names as shown in the following figure:



16. Click *Close* in the Signal Name dialog box.

Adding Ports

Typically, input ports are placed on the left on the block, and output ports are placed on the right. The ports available in the `Standard` library (INPORT, OUTPORT) can be added using Part Information Manager.

1. Choose *Component – Add*.

   Part Information Manager appears.

2. Select `Standard` in the *Library* field.

3. Select *inport* and click *Add*.

4. Click in the design window and then click at the end of the INPUT1 wire.
5. Double-click to add *inport* to the INPUT2 and CARRY_IN wires.
6. In Part Information Manager, select *outport* and click *Add*.
7. Click in the design window and then click at the end of the CARRY_OUT wire.
8. Double-click to add *outport* to the OUTPUT_MSB and OUTPUT_LSB wires.

   The following figure displays the block FULL_ADDER with the added ports:

9. Choose *File – Exit* to close Part Information Manager.
10. Choose *File – Save*.

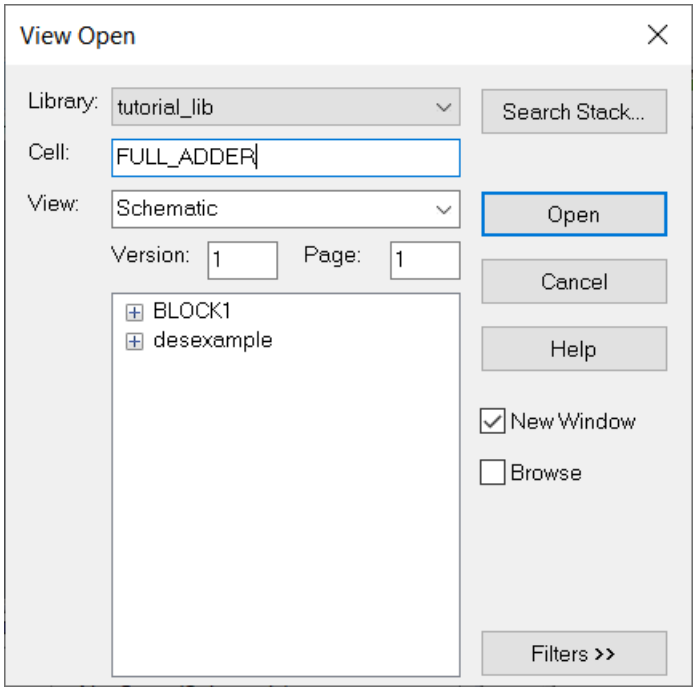
    Note: A message box may display with netlisting errors. Close the box. The error will be addressed as you proceed with the steps.

Creating the Schematic View of FULL_ADDER

1. Choose *File – Open*.

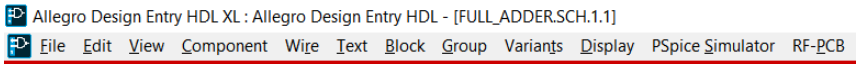
   The View Open dialog appears. Make sure that `tutorial_lib` is selected as the *Library*.

2. Type `FULL_ADDER` in the *Cell* field.

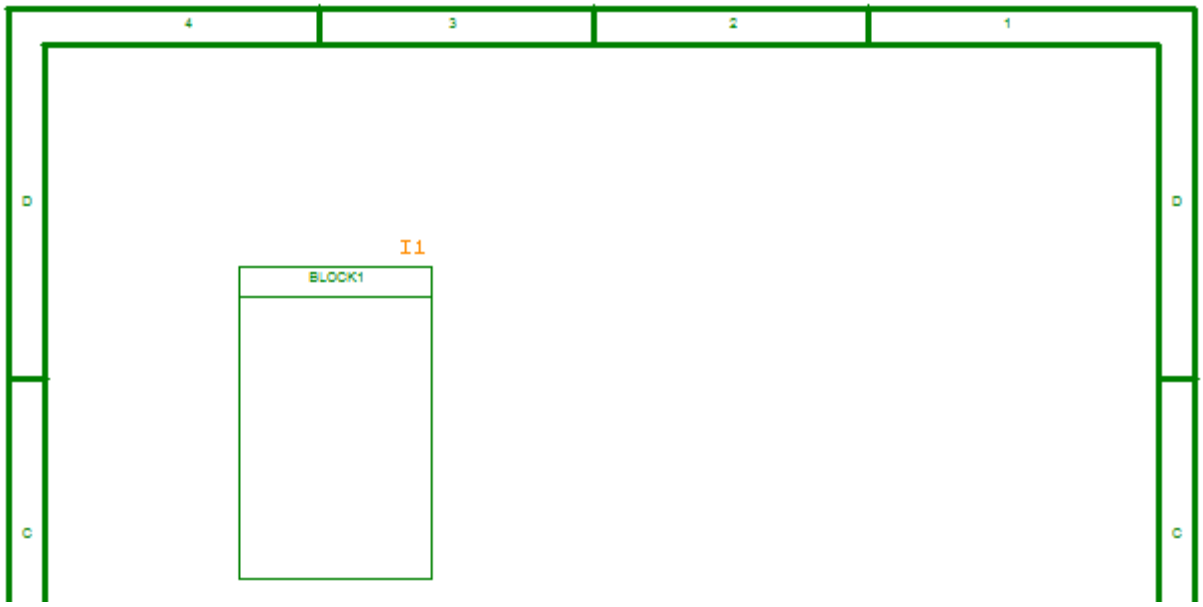


3. Click *Open*.

   Design Entry HDL opens a schematic page named `FULL_ADDER.SCH.1.1`.



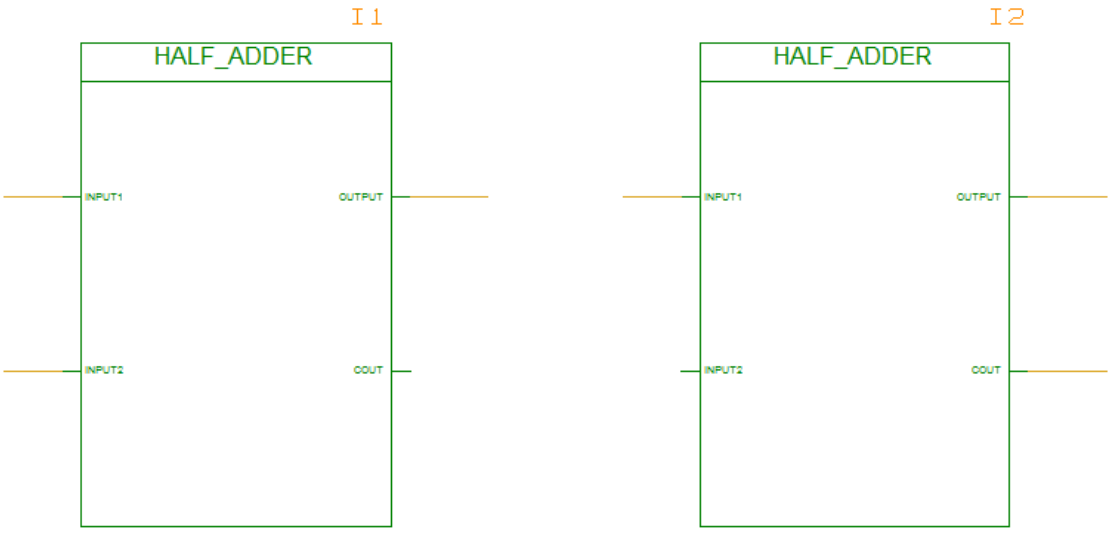
4. Choose *Block – Add* to add a block to the schematic page.



5. Name it `HALF_ADDER` using *Block – Rename*.
6. Add the following input pins on the left of the block:
   - ❑ INPUT1
   - ❑ INPUT2
7. Add the following output pins on the right of the block:
   - ❑ OUTPUT
   - ❑ COUT
8. Choose *Edit – Copy* to copy.
9. Click the block *HALF_ADDER*.

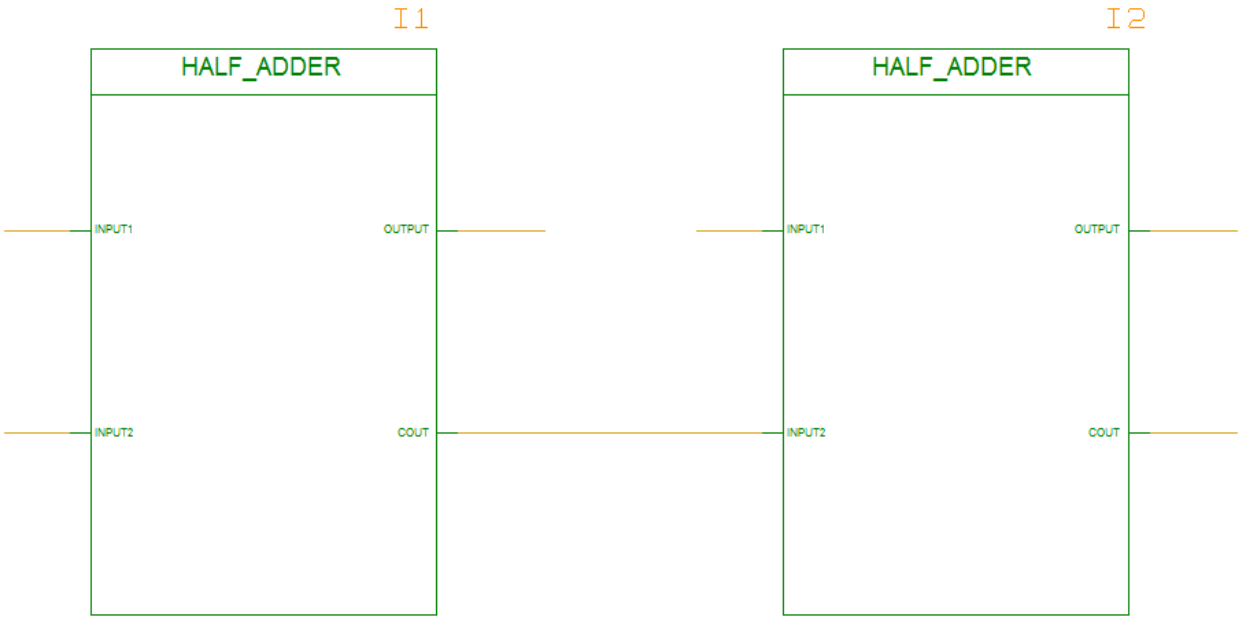
10. Click to paste the copy as shown in the following figure.

11. Choose *Wire – Draw* to draw wires as shown in the following figure.



12. Choose *Wire – Route* to connect `COUT` and `INPUT2`.

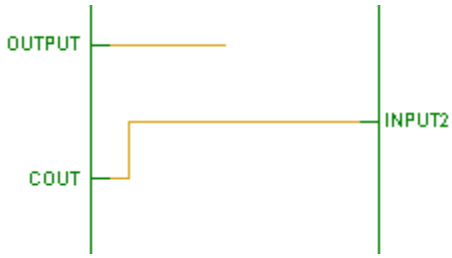
13. Click at the tip of the COUT pin and click again at the tip of the INPUT2 pin as shown in the following figure.



14. Select the HALF_ADDER I3 block.

15. Right-click and select *Move*. Place the selected block a little higher than HALF_ADDER I1.

Design Entry HDL connects COUT and INPUT2 with a wire that bends at right angles as shown in the following figure.



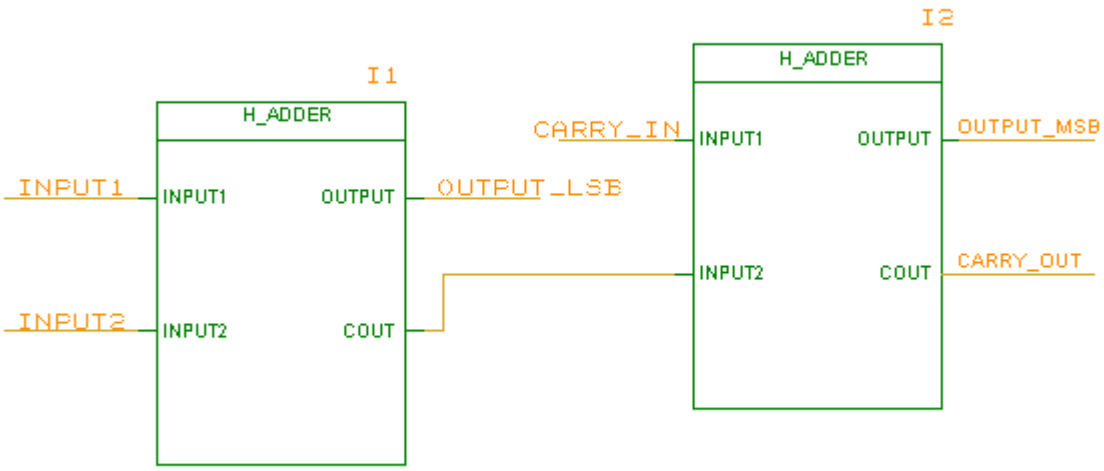
Add signal names. The signal names should be the same as that of the parent drawing.

16. Choose *Wire – Signal Name* to name wires with the following names:

- ❑ INPUT1
- ❑ INPUT2

- ❑ CARRY_IN
- ❑ OUTPUT_LSB
- ❑ OUTPUT_MSB
- ❑ CARRY_OUT

17. Assign names to the wires as shown in the following figure:



18. Add INPORTs to the following signals:

- ❑ INPUT1
- ❑ INPUT2
- ❑ CARRY_IN

19. Add OUTPORTs to the following wires:

- ❑ OUTPUT_LSB
- ❑ OUTPUT_MSB
- ❑ CARRY_OUT

Note: The signal names in the schematic diagram of a *HALF_ADDER* must be the same as the pin names in the *FULL_ADDER* block.

20. Choose *File – Save* to save the design.

21. To view the FULL_ADDER block, choose *File – Edit Hierarchy – Ascend*.

Design Entry HDL displays `DESEXAMPLE.SCH.1.4` that contains the block `FULL_ADDER`.

22. Double-click the *FULL_ADDER* block in Hierarchy Viewer.

Design Entry HDL descends into `FULL_ADDER.SCH.1.1`.

Creating a Schematic for HALF_ADDER

Finally, you create a schematic design for the HALF_ADDER block.

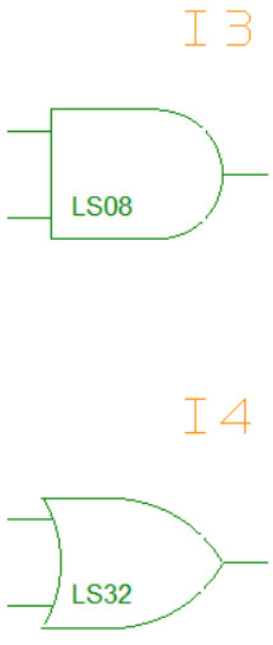
1. Choose *File – Open*.

   The View Open dialog appears.

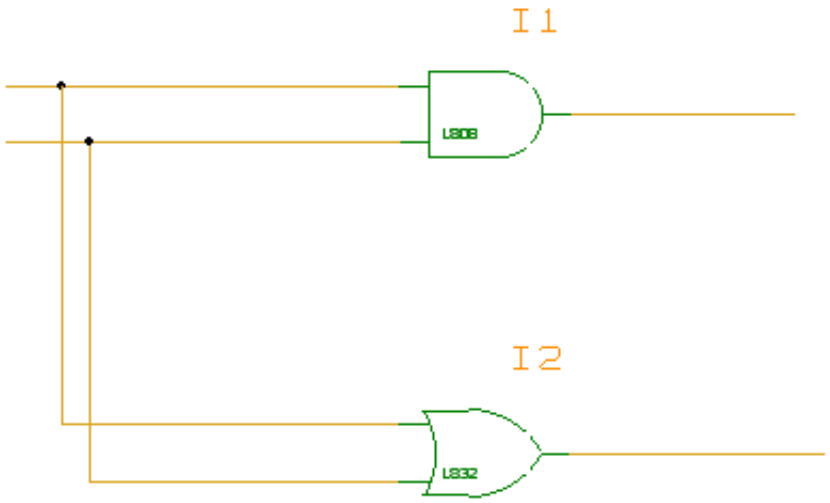
2. Select `tutorial_lib` from the *Library* drop-down list.
3. Enter `HALF_ADDER` in the *Cell* field.
4. Click *Open*.
5. Choose *Component – Add*.

   Part Information Manager appears.

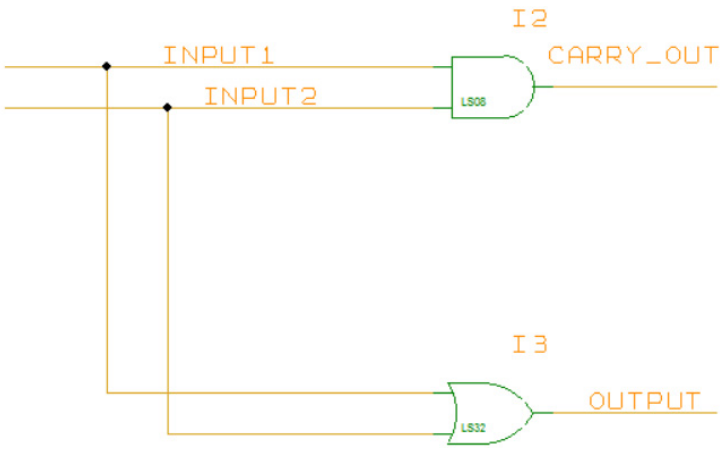
6. Select the *local_lib* library and the `LS08` cell.
7. Click *Add*.
8. Click the schematic to place `LS08`.
9. Select `LS32` from *local_lib* and place on schematic as shown in the following figure:



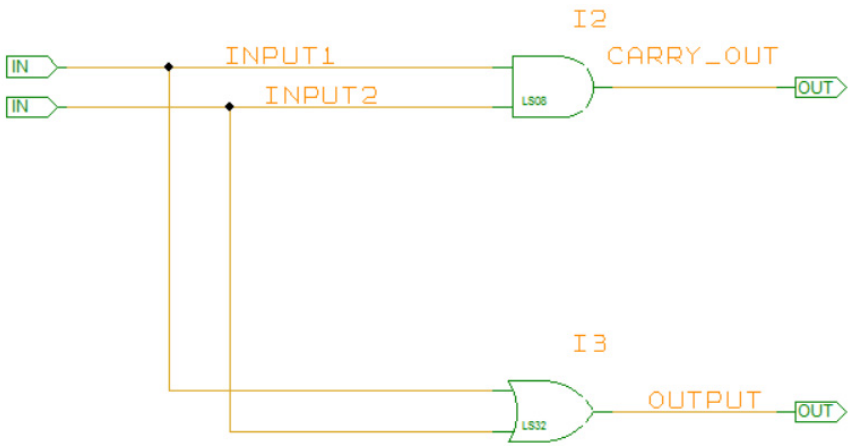
10. Choose *Wire – Draw* to connect the components as shown in the following figure:



11. Choose *Wire – Signal Name* to name the signals as shown in the following figure:



12. Add INPORTs and OUTPORTs from the `Standard` library as shown in the following figure:



13. Choose *File – Save* to save the design.

You have now created a multi-page hierarchical design using the top-down method.

14. To go through the entire design, starting from the top-level cell, choose *File – Open*.

The View Open dialog appears.

15. Select `tutorial_lib` as the *library*.

16. Double-click DESEXAMPLE.

17. Double-click `sch_1`.

18. Select Page1 and click *Open*.

Design Entry HDL displays DESEXAMPLE.SCH.1.1.

19. Choose *File – Edit Page/Symbol – Next*.

Design Entry HDL displays `DESEXAMPLE.SCH.1.2`.

20. Choose *File – Edit Page/Symbol – Next*.

Design Entry HDL displays `DESEXAMPLE.SCH.1.3`.

21. Choose *File – Edit Page/Symbol – Next*.

Design Entry HDL displays `DESEXAMPLE.SCH.1.4`.

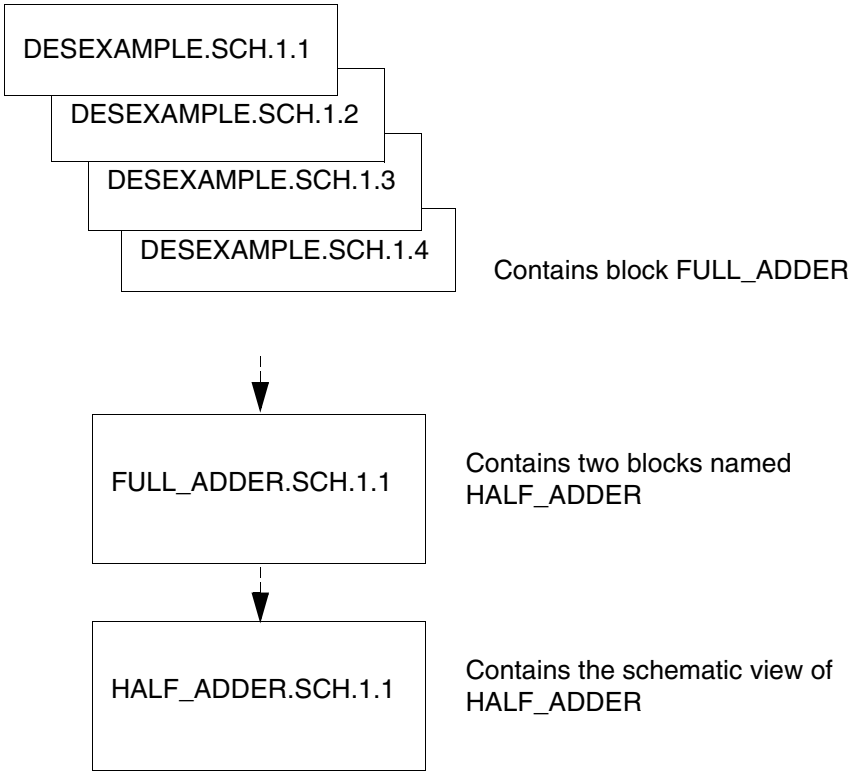
22. Double-click the FULL_ADDER block.

Design Entry HDL displays `FULL_ADDER.SCH.1.1`.

23. Double-click the HALF_ADDER block.

Design Entry HDL opens `HALF_ADDER.SCH.1.1`.

The structure of the hierarchical design you have created is illustrated in the following figure.



1. Close Design Entry HDL.
2. Close Project Manager.

Creating a Hierarchical Design Using the Bottom-Up Method

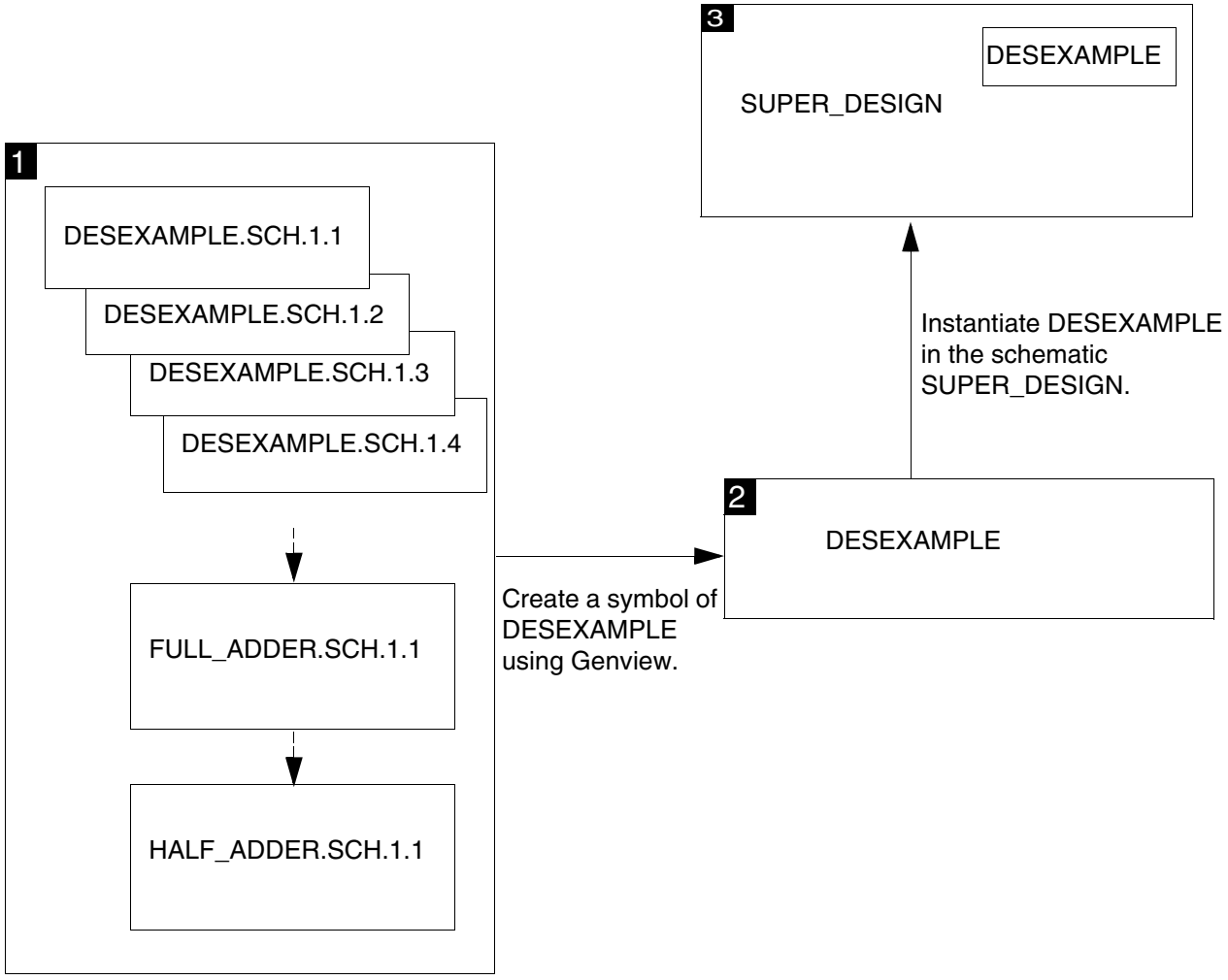
When you create a hierarchical design using the bottom-up method, you need to create a schematic page for the lower levels of the hierarchy and then add pages for the higher levels.

In the bottom-up method of creating a design, you perform the following steps:

- Create symbols for lower-level schematics.
- Create a schematic page for the higher design level and instantiate the symbols of the lower-level schematics in the schematic.
- Change the top-level design.

In this section, you use the design, DESEXAMPLE, as a lower-level design and add a schematic page called SUPER_DESIGN.SCH.1.1 at a higher hierarchical level. The following figure shows the planned design.

Figure 5-3 Bottom-Up Design

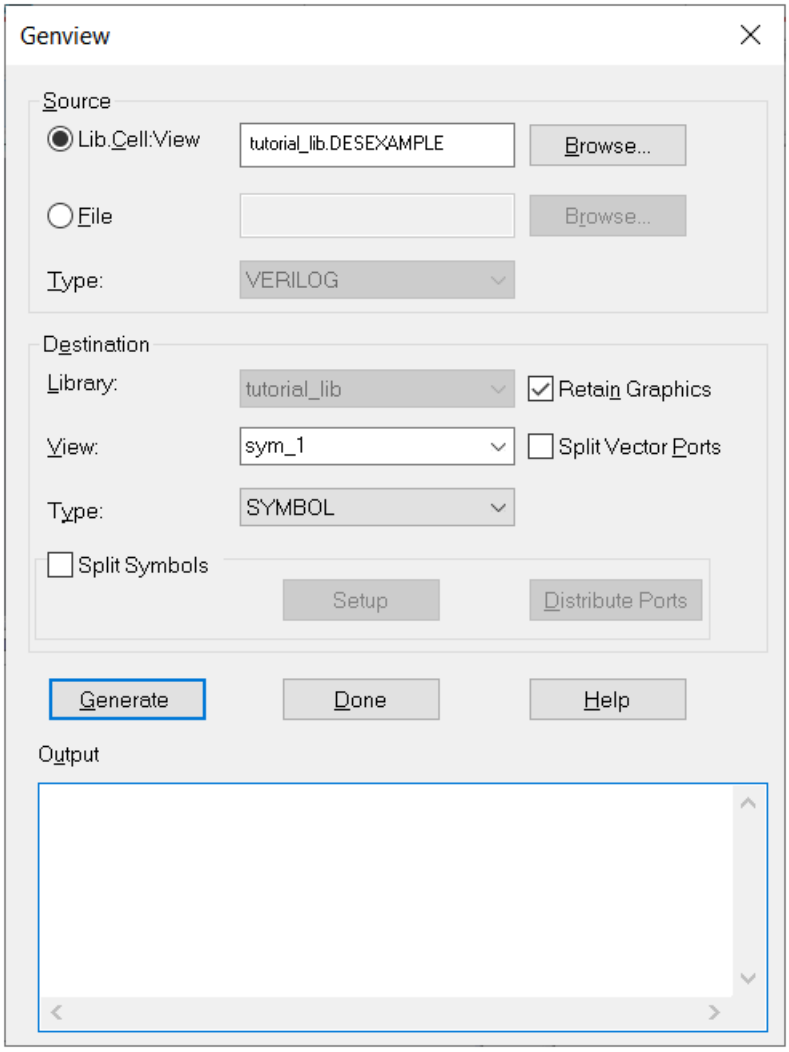


Creating a Symbol

1. Start Project Manager.
2. Load the tutorial project and open Design Entry HDL on the project.

   Design Entry HDL appears displaying DESEXAMPLE.SCH.1.1.
3. Choose *Tools – Generate View*.

The Genview dialog appears.



4. Click *Generate*.

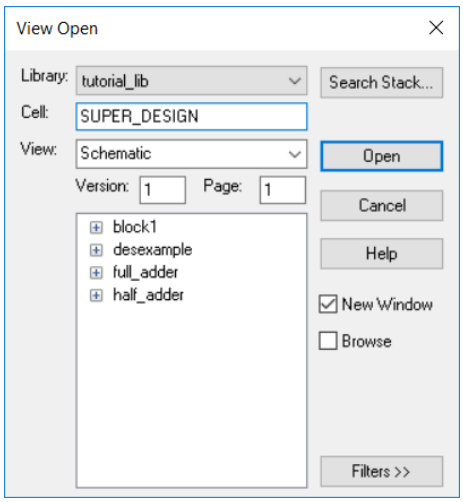
   The Genview status is displayed in the *Output* section of the Genview dialog and an information message box is displayed.

5. Click *OK* in the message box then click *Done* in the Genview dialog.

Creating a Schematic Page at a Higher Hierarchy Level

You will now create a new schematic page in which the symbol can be instantiated.

1. Choose *File – Open*.
2. Select `tutorial_lib` from the *Library* drop-down list.
3. Enter `SUPER_DESIGN` in the *Cell* field.



4. Click *Open*.

   Design Entry HDL creates a blank schematic page named SUPER_DESIGN.SCH.1.1.

5. Choose *Component – Add*.

   Part Information Manager appears.

6. Select `tutorial_lib` from the *Library* drop-down list.
7. Choose `desexample` from the *Cells* list and click *Add*.
8. Click in the design window to place the component.
9. Right-click and select *Done*.

10. Choose *File – Save* to save the schematic.

11. Choose *File – Exit*.

Design Entry HDL exits.

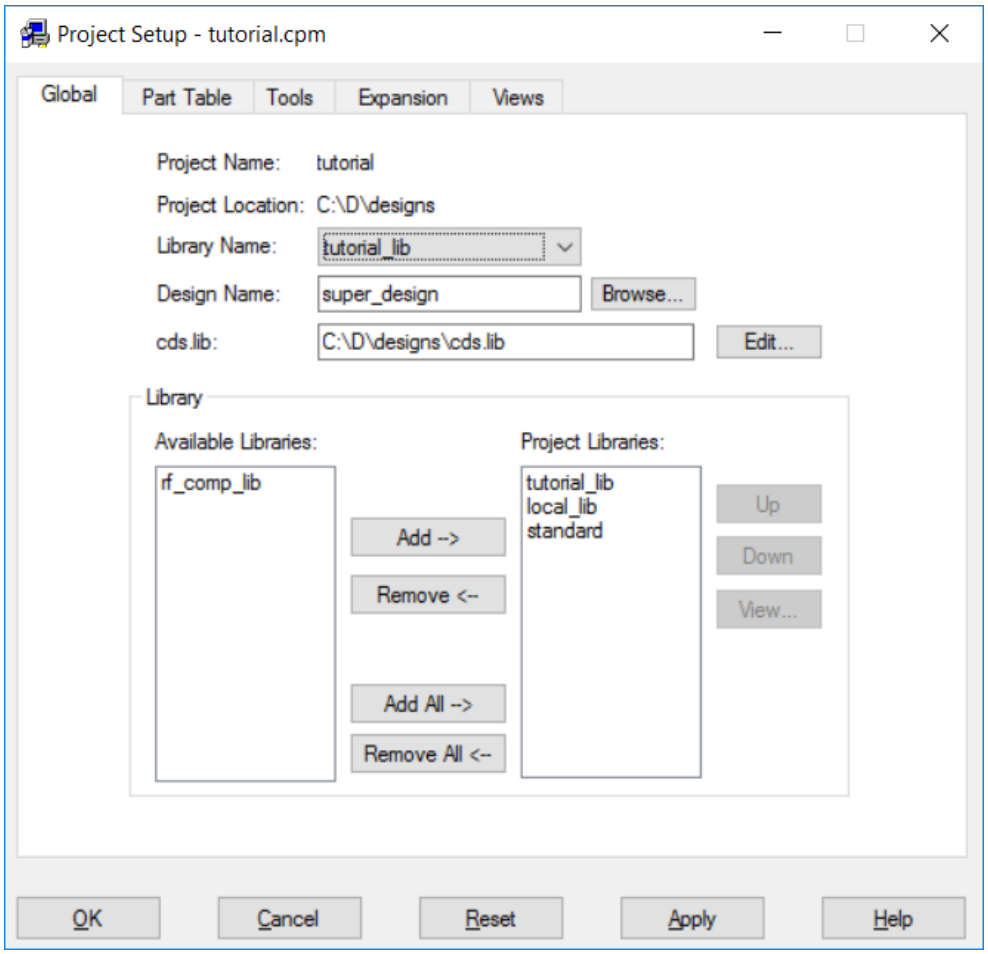
Changing the Top-Level (Root) Design

In the design you have created, DESEXAMPLE is the top-level design. The top-level design is also known as the root design.

1. Open Design Entry HDL.
2. Click *Setup* in Project Manager.

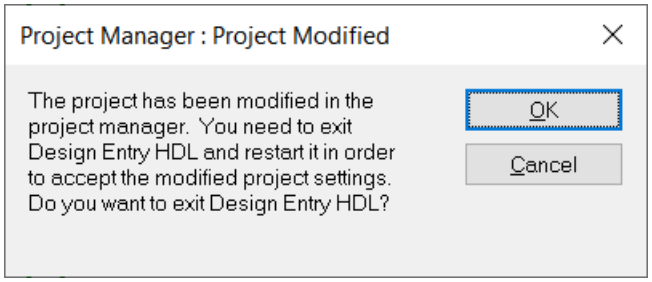
   The Project Setup dialog appears.
3. Click *Browse* next to the *Design Name* field.

   The Select Cell dialog box appears and displays all the cells in the `tutorial_lib` library.
4. Select `super_design` from the list and click *OK*.



5. Click *OK*.

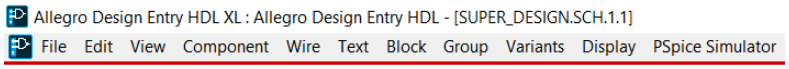
   A message box prompts you to exit Design Entry HDL.



6. Click *OK*.

   Design Entry HDL changes the top-level design from `DESEXAMPLE` to `SUPER_DESIGN` and closes Design Entry HDL.

To view the changes in the design structure, start Design Entry HDL by clicking *Design Entry* in Project Manager. Design Entry HDL opens SUPER_DESIGN_SCH.1.1.



Plotting a Schematic Design

Sometimes, you might need to print your design for tasks such as debugging and documentation. Design Entry HDL provides support for plotting your designs.

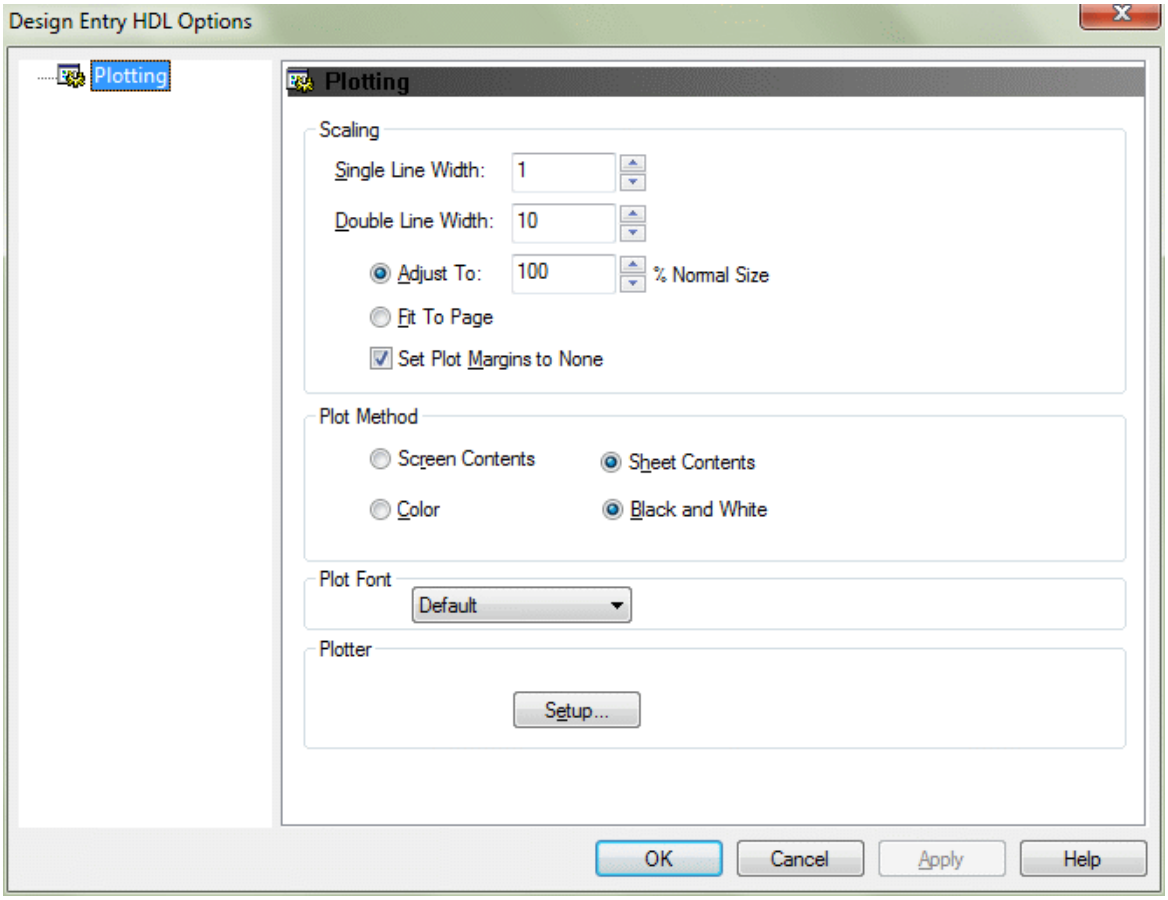
To plot a design, you need to do the following:

- Setting up plotting
- Previewing
- Plotting

Setting up the Plotting Options

1. To set up plotting, choose *File – Plot Setup*.

The Design Entry HDL Options dialog appears with the *Plotting* tab.



You can also choose *Tools – Options* to display the Design Entry HDL Options dialog. By default, the *General* tab will be displayed. Then select the *Plotting* tab.

2. In the *Scaling* section, accept the default values for *Single Line Width* and *Double Line Width*.

3. Select *Fit To Page* so that the complete schematic page is adjusted to fit into one page of the specified paper size.

4. Select a suitable *Plot Method*.

   a. Select *Screen Contents* if you want to plot only that part of the design which is visible on the screen. To plot the complete design, select *Sheet Contents*.

   For the current design, select *Sheet Contents*.

   b. Select the color to plot the drawing.

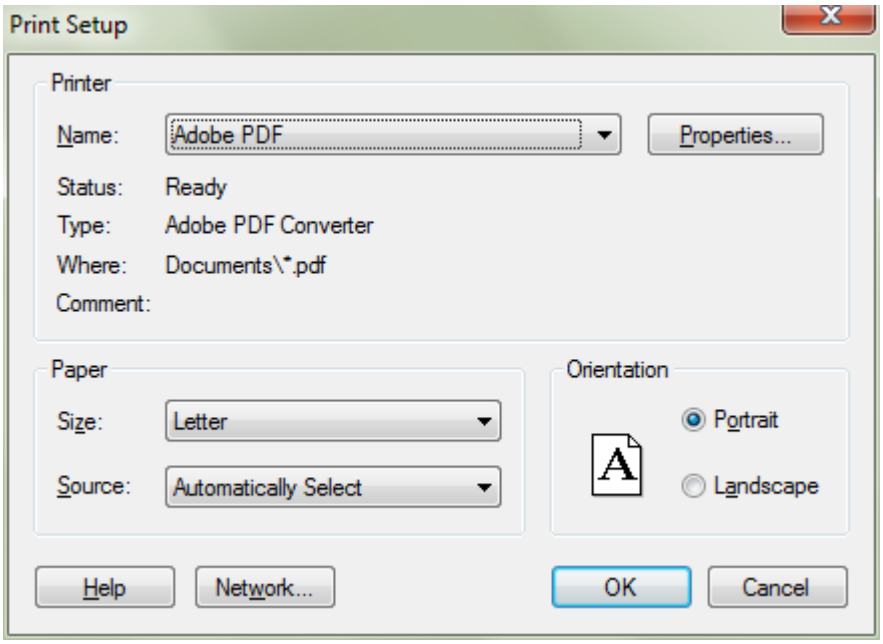
   Select *Color* if you want to plot the drawing in color.

Select *Black and White* to plot drawings in black and white. If you select *Color* on a black and white plotter, the printout has different scales of gray.

For the current design, select *Black and White*.

5. Click *Setup*.

The Print Setup dialog appears.



6. Select the printer from the *Name* drop-down list.

   For the current design example, accept the default printer.

7. Choose *Paper Size* and *Source*.

   In this example, we will accept the default values.

8. Select the *Orientation* as `Landscape`.

9. Click *OK* to save the settings and to close the Print Setup dialog.

10. Click *OK* to save the settings and to close the Design Entry HDL Options dialog.

Previewing the Plot

Before you take a printout of the design, it is good practice to preview the design. If the preview is not according to your requirements, you can modify the setup.

1. To preview the design, choose *File – Plot Preview*.

   The complete schematic page is adjusted to fit into one sheet of the paper.

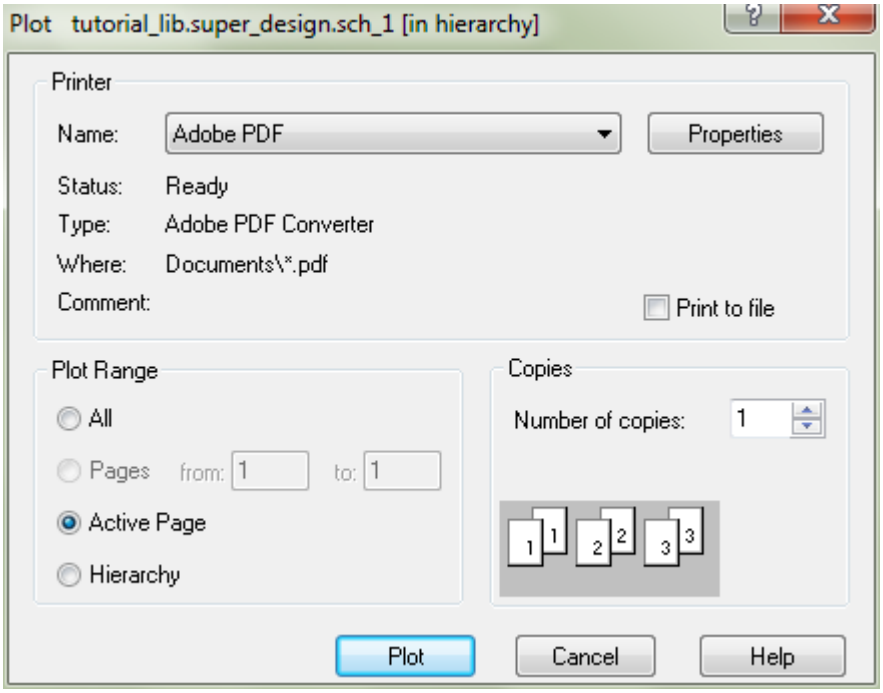
2. Click *Close* to close the preview window.

   Note: You can plot the design from the preview window by clicking *Print*.

Plotting the Design

1. To plot the design, choose *File – Plot*.

   The Plot dialog appears.



2. Click *Plot* to plot the design.
3. Browse to the location where you want to save the printed output and click *Save*.

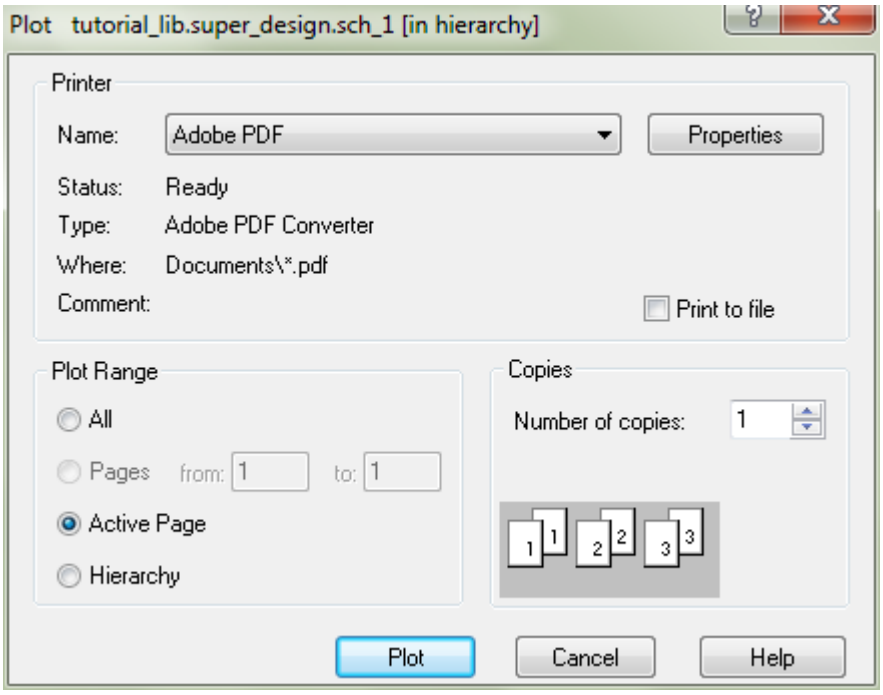
Hierarchical Plotting

An important feature supported by Design Entry HDL is hierarchical plotting. This feature is available in both Windows Plotting and HPF Plotting. For more information on Windows Plotting and HPF Plotting, see the *Plotting Your Design* chapter in *Allegro Design Entry HDL User Guide*.

Using hierarchical plotting, you can customize the way in which you plot various hierarchies in your design. To know more about how you can re-organize modules in your design, see *Module Ordering* in *the Working with Designs* chapter of the *Allegro Design Entry HDL User Guide.*

1. To plot the hierarchies in your design, choose *File – Plot*.

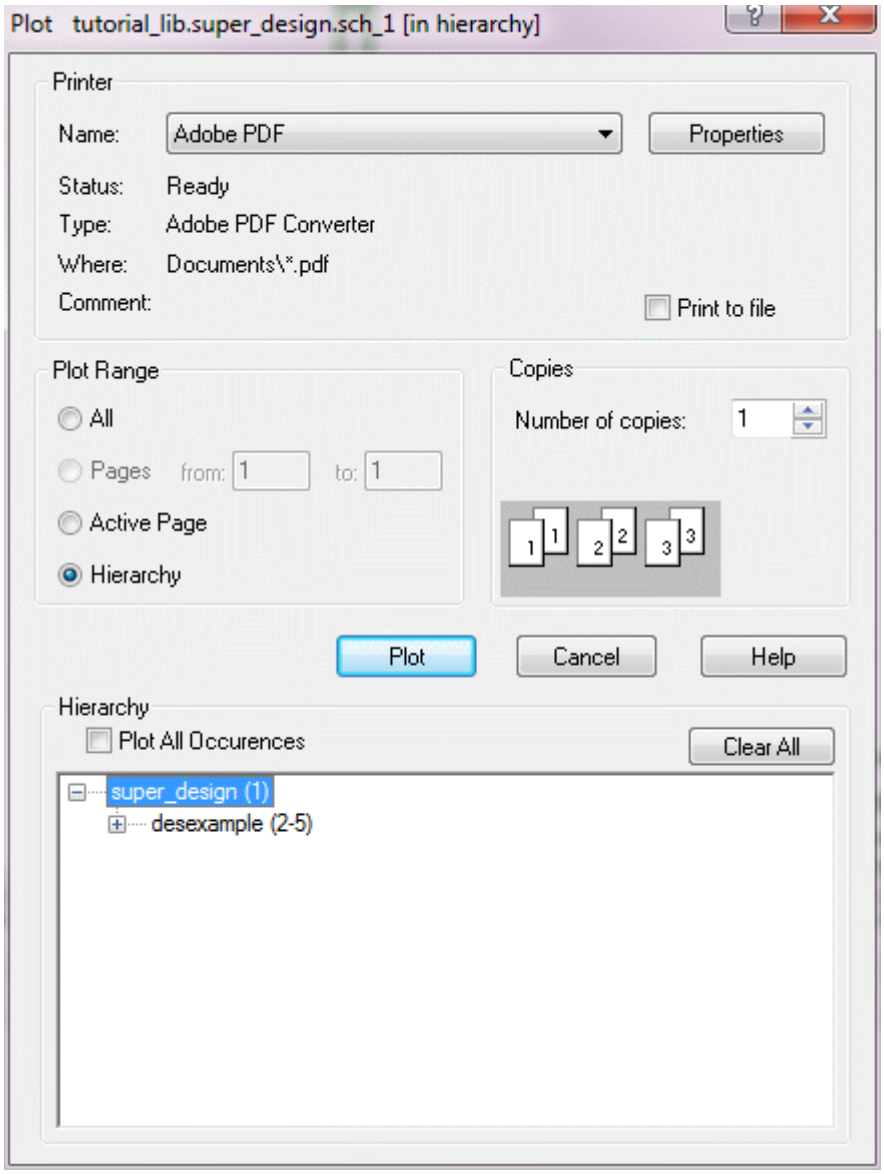
   The Plot dialog appears.



   Note: The *Print to file* check box in the Plot dialog appears only on Windows computers.

2. In the *Plot Range* section, select `Hierarchy`.

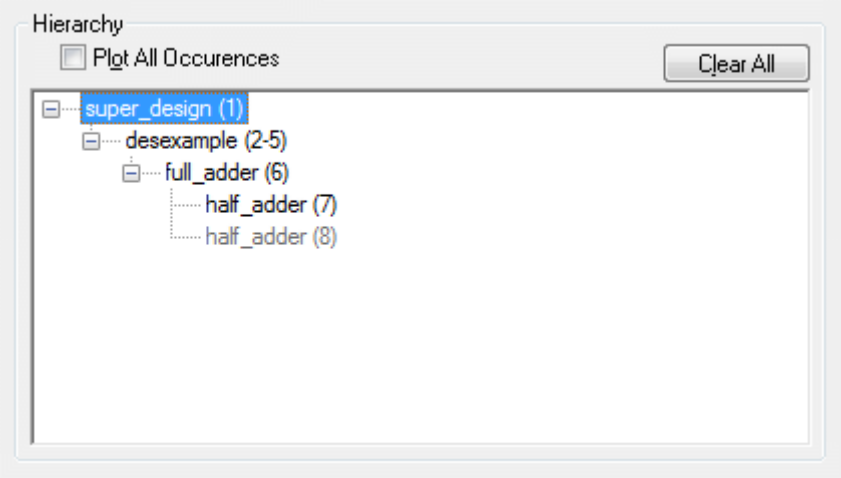
The *Hierarchy* section appears.



Note: The hierarchy tree visible in the hierarchy section of the dialog is the same as the module ordering tree.

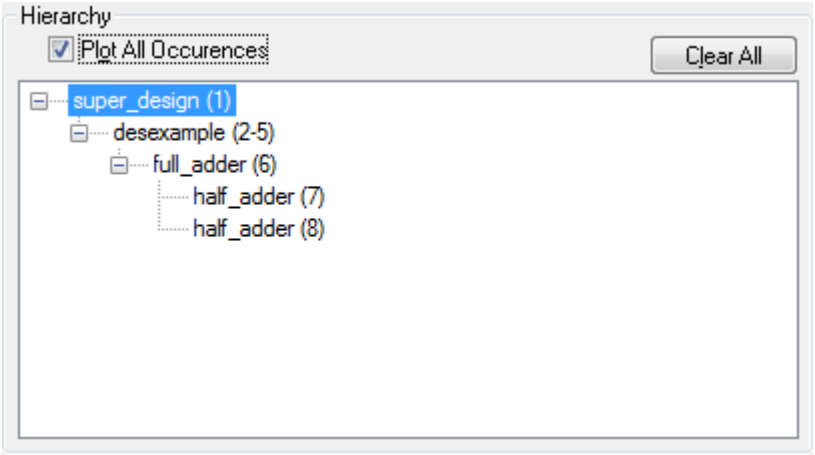
3. To expand the design, click the + sign.

A list of subdesigns under the design appear. Similarly, you can descend further down the hierarchy.



There are two occurrences of the block `half_adder` in the figure. The second occurrence of the block `half_adder` is grayed out. This is because only one occurrence of a block is plotted by default.

4. Select the *Plot All Occurrences* check box to plot both occurrences of the block `half_adder` in the design.



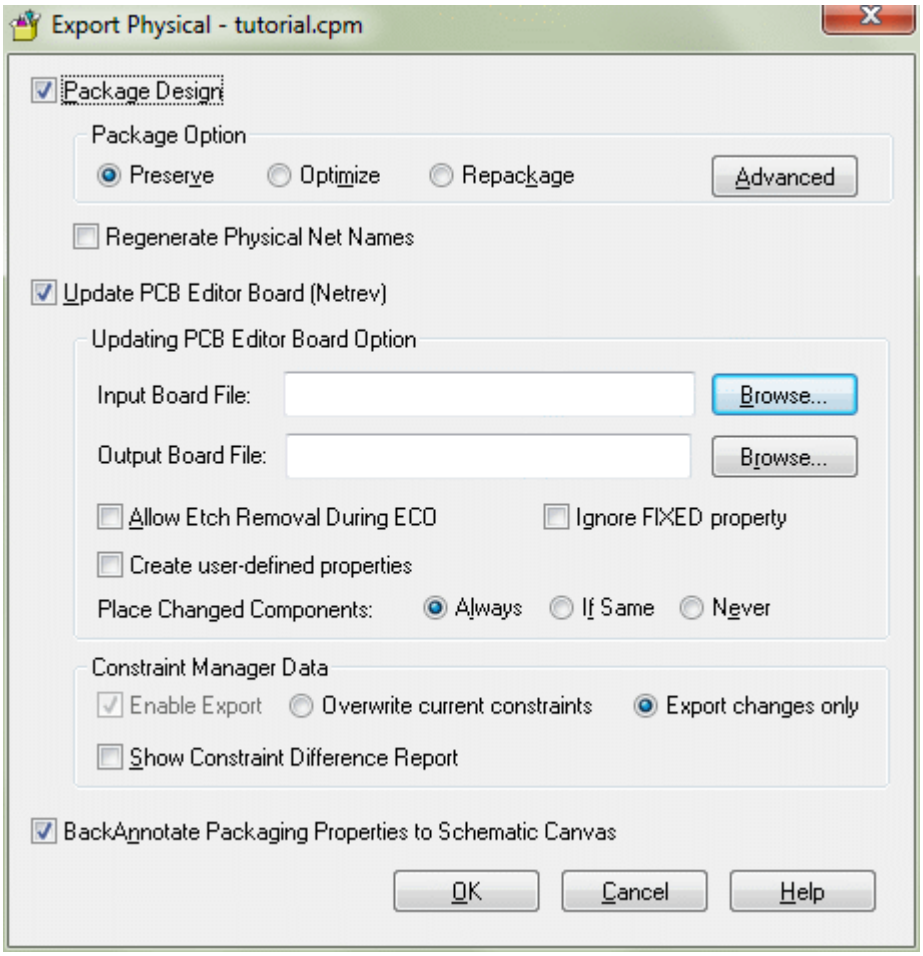
5. Click *Plot*.
6. Browse to the location where you want to save the printed output and click *Save*.

Packaging Your Design

Packaging involves translating your logical design (schematic) into a physical design ready for placement and routing. The tool used for performing placing and routing is PCB Editor.

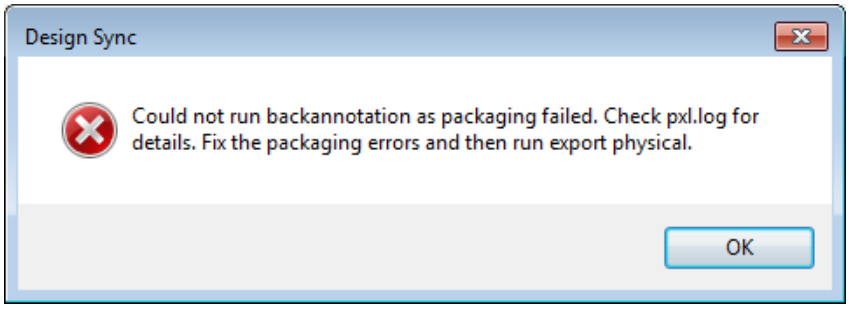
1. Choose *File – Export Physical*.

   The Export Physical dialog appears as shown in the figure.



2. Select *Repackage*.
3. Uncheck the *Update PCB Editor Board (Netrev)* box.
4. Click *OK*.

An error message appears.



5. Click *Yes* when prompted to view the log file.

The log file is opened in a text editor. The log file lists the following two errors in assigning physical parts:

```
 ****************************************
 *  Starting to assign physical parts.  *
 ****************************************
#1  ERROR(1053): Cannot find a ppt part that matches the instance properties.
        Ppt Name: RES
      Schematic instance: @TUTORIAL_LIB.SUPER_DESIGN(SCH_1):PAGE2_I1@TUTORIA~
L_LIB.DESEXAMPLE(SCH_1):PAGE2_I15@LOCAL_LIB.RES(CHIPS)
        Property Name: VALUE
        Property Value: 100
        Property Name: TOL     (OPT=5%)
        Property Value:
        Property Name: RATED_POWER
        Property Value:
        Property Name: PKG
        Property Value: RAD
 #2  ERROR(1053): Cannot find a ppt part that matches the instance properties.
        Ppt Name: RES
      Schematic instance: @TUTORIAL_LIB.SUPER_DESIGN(SCH_1):PAGE2_I1@TUTORIA~
L_LIB.DESEXAMPLE(SCH_1):PAGE2_I16@LOCAL_LIB.RES(CHIPS)
        Property Name: VALUE
        Property Value: 100
        Property Name: TOL     (OPT=5%)
        Property Value:
        Property Name: RATED_POWER
        Property Value:
        Property Name: PKG
        Property Value: RAD
```

```
*********************************************
 *  End assigning physical parts.  (00:00:00)  *
 *********************************************

 ***************
 *  Packaging  *
 ***************

 ******************************
 *  End packaging  (00:00:00)  *
 ******************************

2 errors detected
No warnings detected
    Start time   10:06:07
    End time     10:06:35
    Elapsed time  0:00:28

 *******************************************
 *  ERROR Packager-XL exiting with status 1  *
 *******************************************
```

The errors in assigning physical parts occur when Packager-XL matches the part table information for the component RES with the properties present on the component and is unable to match any row in the part table file with the properties on the component.

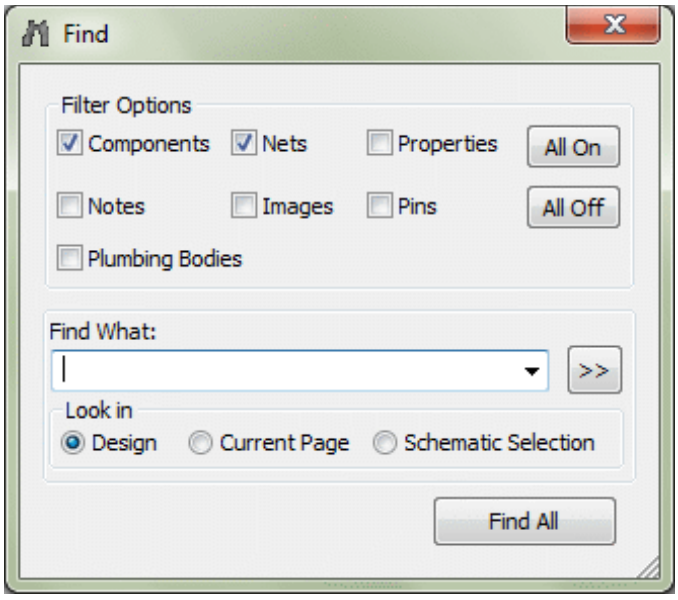
6. Close the text editor.
7. Click *Close* in the Progress window.

You will now use the *Find* utility in Design Entry HDL to locate the parts in the design named RES.

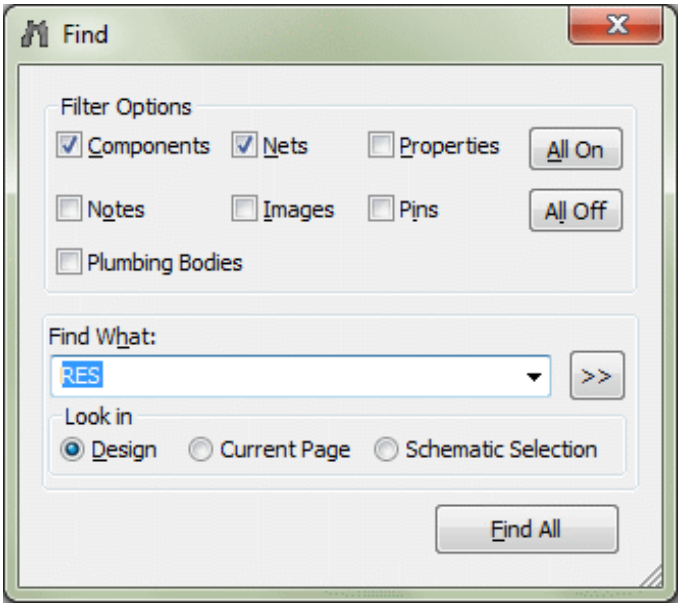
Using the Find Utility

1. Click the *Search options* () button on the Search toolbar.

The Find dialog appears.

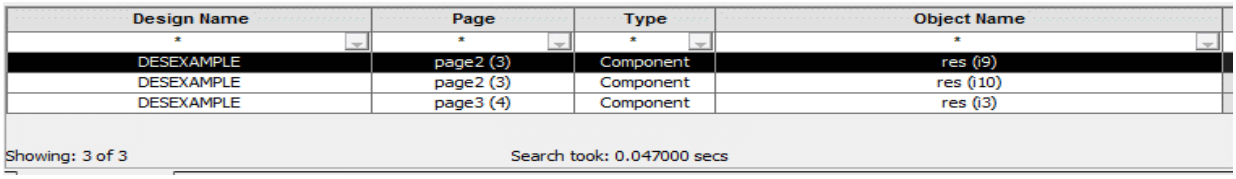


2. Type `RES` in the *Find What* field.



3. Click *Find All* in the Find box.

   Design Entry HDL locates three instances of RES in the design and displays the names in the Search Result dockable window.



4. Double-click the first instance.

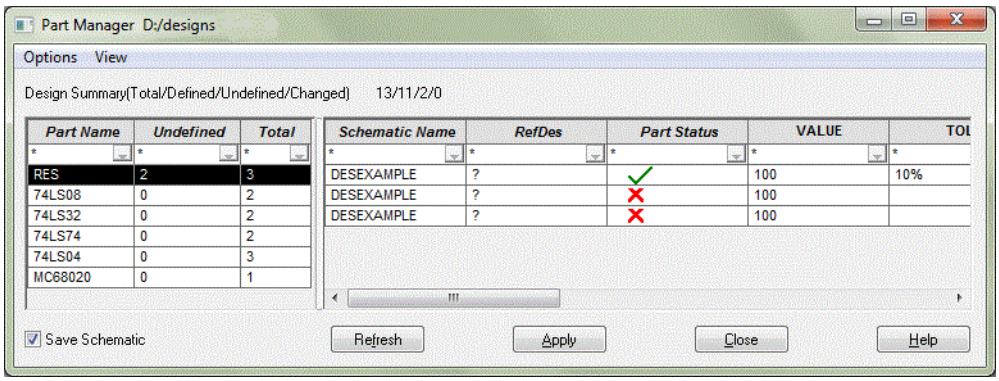
   Design Entry HDL highlights the instance with red color in the schematic DESEXAMPLE.SCH.1.2.

Correcting Errors in Assigning Physical Parts Using Part Manager

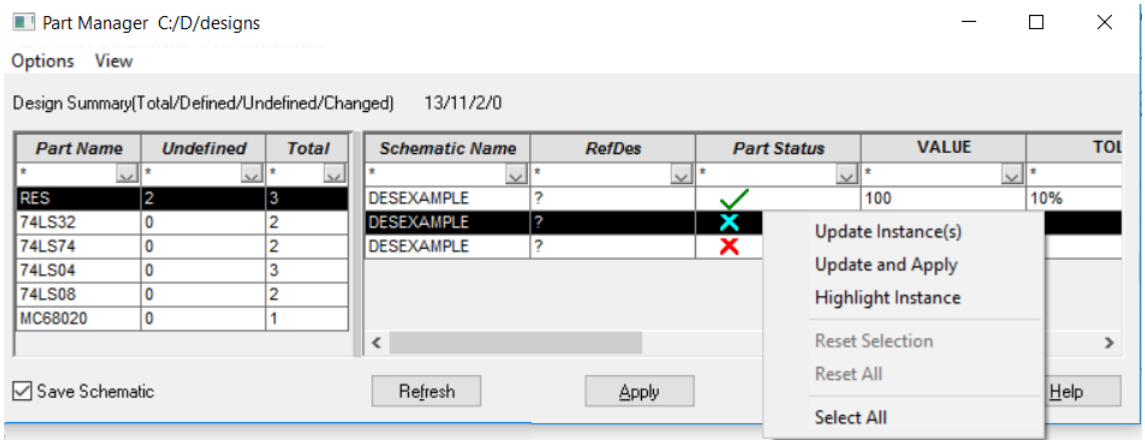
The Part Manager utility in Design Entry HDL provides you a convenient way of viewing and correcting information about the part table file (ptf) rows associated with part instances on a schematic. To correct errors in assigning physical parts, follow these steps:

1. Choose *Tools – Part Manager*.

   Part Manager appears. The box displays a summary of all the parts of the design and their status. A green tick mark in the *Part Status* column indicates that the part instance matches a row in the part table. A red cross mark in the *Part Status* column indicates that the part instance does not match any row in any part table file.

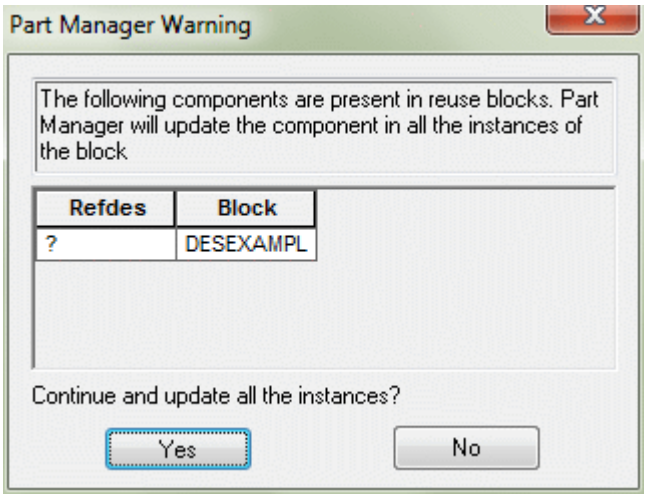


2. To correct the part, select a row with a mismatched status and then right-click.



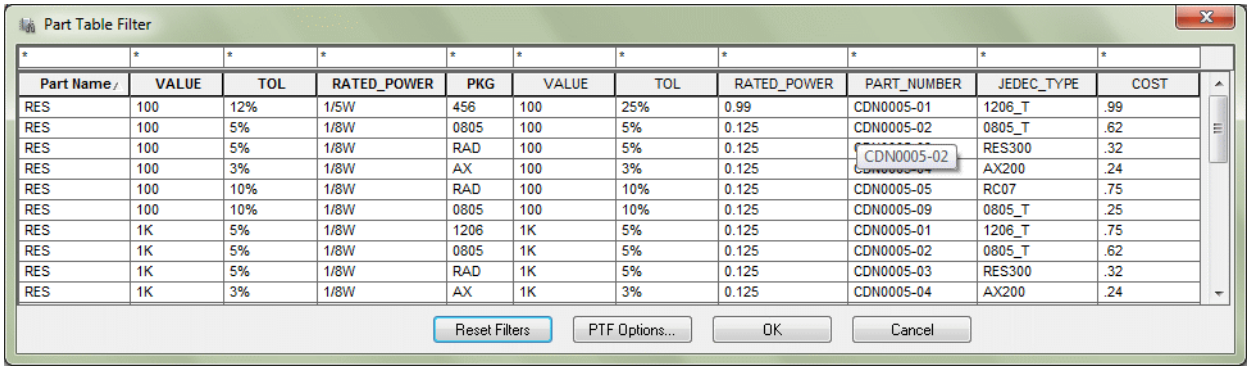
3. Click *Update Instance(s)*.

   A warning message is displayed.

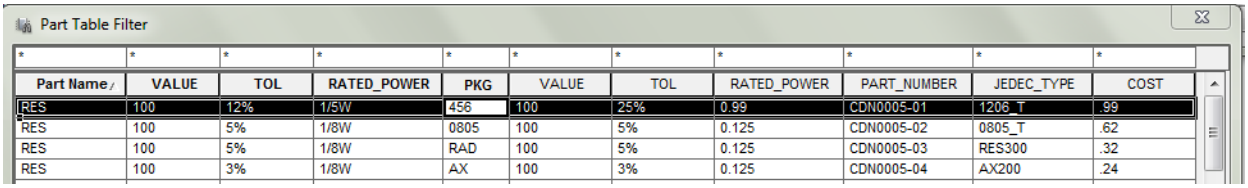


4. Select the row and click *Yes*.

The Part Table Filter dialog appears.

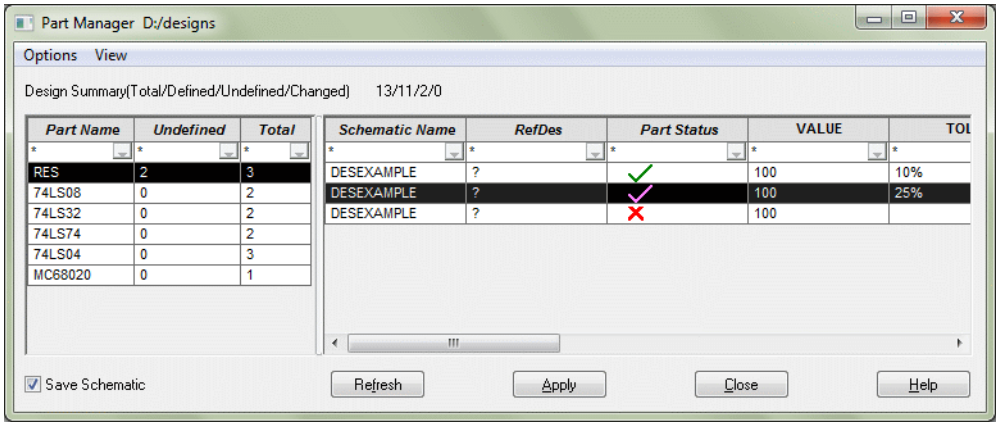


5. Select the first row in the Part Table Filter dialog.



6. Click *OK* in the Part Table Filter dialog.

   The status of the mismatched part changes to green.



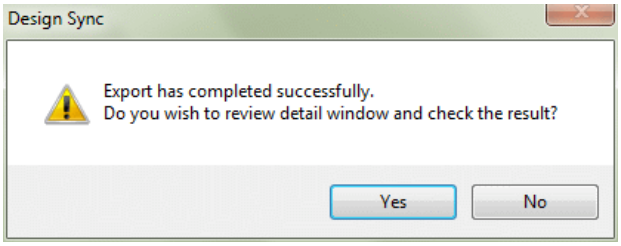
7. Select the next mismatched row and right-click.
8. Repeat steps 3 to 6.
9. Click the *Apply* button.
10. Click *Close* in the Part Manager.

Packaging the Design after Fixing Errors

1. Choose *File – Save*.
2. Choose *File – Export Physical*.

   The Export Physical dialog appears.
3. Select *Repackage*.
4. Deselect the *Update PCB Editor Board (Netrev)* check box.
5. Click *OK*.

   Design Entry HDL displays a message window indicating that packaging is complete.



6. Click *No*.

6

Multimedia Demonstrations in Design Entry HDL

The following multimedia demonstrations explain the important features of Design Entry HDL. Most of the demonstrations listed in the following table were created or updated before the current release and are available on the *SPB Video Library* page on Cadence Online Support (COS). Clicking a link to a demonstration on COS requires you to log on to Cadence Online Support. Once your login credentials are verified, you are directed to the relevant demonstration.

Demo	Objective
Tracing a Signal Using Cref Links	Demonstrates how to trace signals in a design using Cross Referencer hyperlinks (Cref links).
Displaying Page Names in Hierarchy Viewer	Illustrates how the Design Navigation feature of Design Entry HDL facilitates the display of page names in Hierarchy Viewer.
Implementing RF-PCB IFF Import	This demonstration shows you how to use RF-PCB IFF Import to import a radio-frequency (RF) design into a Design Entry HDL schematic.
Publishing a Design as a PDF Document	To publish a design as a PDF document using the Allegro Design Publisher solution (Publish PDF utility).
Copying a Project using the Copy Project Functionality	To copy a project from one location to another using the *Copy Project* functionality.
Copying Components	To copy a component from one design to another by using Design Entry HDL.

Copying Designs to External Editors	To copy a design to an external editor. The demo also shows you how to change capture settings, such as the background color
Copying Images from External Editors	To copy an image created in an external graphics editor to a schematic
Copying Schematic Objects Across Designs	To copy schematic objects, such as components, wires, and nets, from one design to another. The demo also shows you how to change signal names while pasting a net.
Copying Text from External Editors in Design Entry HDL	To copy text from an external text editor to schematic. The demo also shows you how to retain casing while pasting text
Setting Up QuickPick Browser	To set up the QuickPick browser
Working with Component Revision Manager	Provides an overview of the interface elements of the Component Revision Manager tool. Also shows you how to update schematic instances from your reference libraries
Creating a Project	To create a new project file using Project Manager
Creating a Schematic Block for the Design Reuse Flow	To create a logical schematic by using Design Entry HDL
Hierarchy Viewer	To highlight the features of the Hierarchy Viewer window. The demo includes procedures for viewing the complete hierarchy of a design, navigating through a design, and reordering modules in the hierarchy.
Part Manager	To highlight the features of the Part Manager utility. The demo includes procedure for updating part instances on a schematic with appropriate PTF (part table file) rows
Global Update	To explain how to delete or modify a net, pin, or component property and replace a component in a design

Cross-referencing a design	To explain how to cross reference a design and read different cross references. The demo includes description of different CRefer reports.
Assign Power Pins in Design Entry HDL	To highlight the features of the Assign Power Pins dialog box. The demo includes procedures for creating new properties for a component, creating new properties for a group of components, and for passing properties across components.

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