

Allegro Sigrity PI Flow Guide

Product Version 23.1
September 2023

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Allegro Sigrity PI

This chapter covers the following topics:

- [Introduction to Allegro Sigrity PI](#)
- [Licensing and Packaging](#)
- [Launching Allegro Sigrity PI](#)
- [Calling Cadence Sigrity Tools from Allegro Sigrity PI](#)
- [Opening Allegro Sigrity PI Layout Files in Cadence Sigrity Tools](#)
- [Updating Sigrity Layout Tools with Allegro Sigrity PI Data](#)

Introduction to Allegro Sigrity PI

Allegro Sigrity PI is intended for power integrity (PI) analysis of Allegro PCB, IC Package, and SiP designs. The product provides an integrated solution for layout and analysis. The *PI Signoff and Optimization* option of the product provides detailed and accurate analysis and examination of decoupling capacitor values and placement.

Allegro Sigrity PI includes:

- A layout editor for floorplanning, editing, and routing.
- Integrated Cadence Sigrity technology for DC Analysis including cross-probing between the analysis results and the floorplanner.
- Power Feasibility Editor (PFE) to drive the creation of PI Constraint Sets. PFE enables you to select and analyze a set of capacitors to create a decoupling strategy for a particular device. This strategy is then captured as a PICSet which is then passed back to the design and can be managed in Constraint Manager.
- The *Decap Place* command to provide placement guidance to place capacitors based on the PICSet.
- The *Decap Placement Replication* command to apply the placement template to several instances of the same device.
- Back annotating decap information from OptimizePI.

Licensing and Packaging

The Allegro Sigrity PI product (PA5800) is available for the three database types: PCB, IC Package, and SiP.

Allegro Sigrity PI Product Options

There are two product options available for Allegro Sigrity PI that combine Allegro Sigrity PI tools and include CAD translators to support PCB and Package designs from all the major vendors:

- **PI Signoff & Optimization (SIGR925)**
- **Package Analyze**

These options are integrated with the Allegro Sigrity PI product to provide expert-level power integrity analysis on top of an editing canvas that allows for the design to be changed and re-

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analyzed in an integrated fashion. This option includes the ability to run all the Cadence Sigrity tools either directly from Allegro Sigrity PI or as point tools.

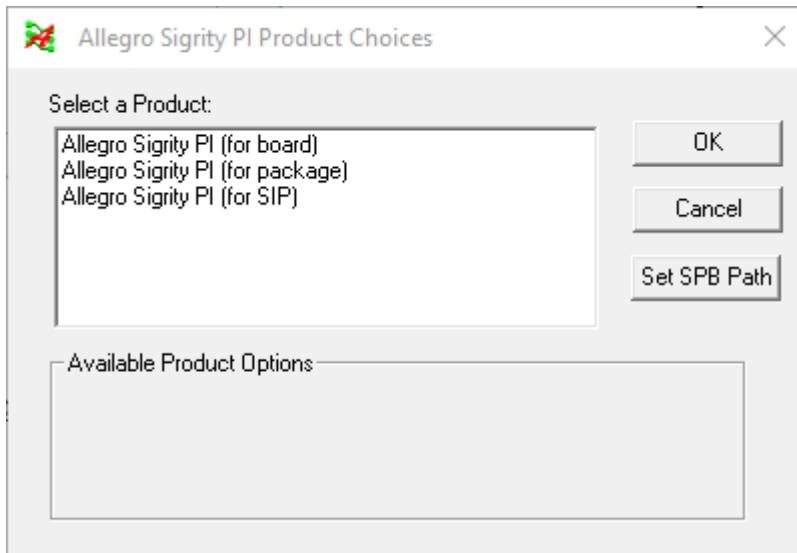
The *Package Analyze* option is only available for Package databases: IC Package and SiP. It includes hybrid and 3D solvers, packages electrical assessment, and DC power analysis.

Launching Allegro Sigrity PI

To launch Allegro Sigrity PI, do the following:

- Choose *Cadence Release 17.2-2016 – Power Integrity* from the *Start* menu.
- OR
- Type `allegrosigritypi.exe` in the command prompt and press *Enter*.
This executable is located in the `<SPB_install_directory> - tools - bin` folder.

The Allegro Sigrity PI Product Choices box offers the following product options:

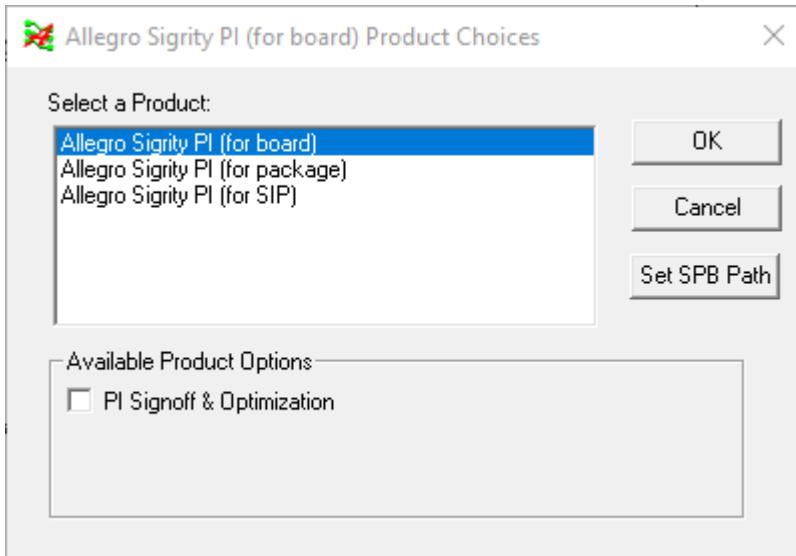


If you select *Allegro Sigrity PI (for board)*, the following product option is available:

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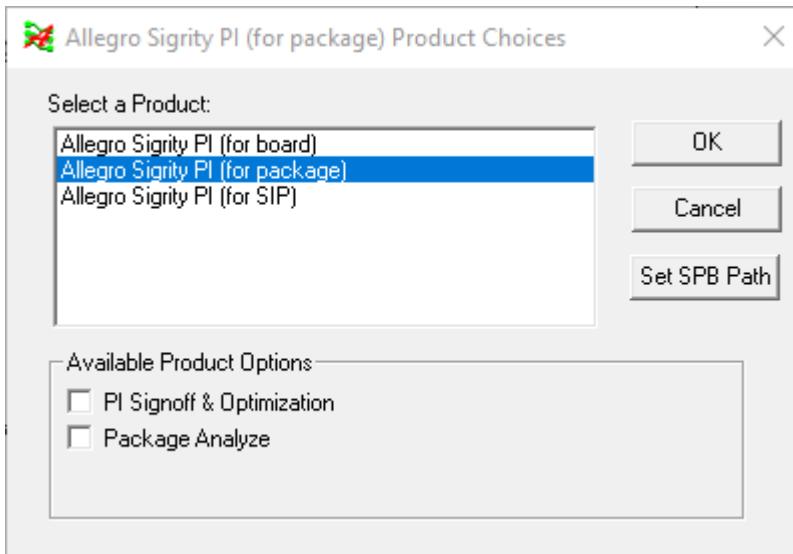
Allegro Sigrity PI

■ PI Signoff & Optimization



If you select *Allegro Sigrity PI (for package)* or *Allegro Sigrity PI (for SIP)*, the following product options are available:

- PI Signoff & Optimization
- Package Analyze



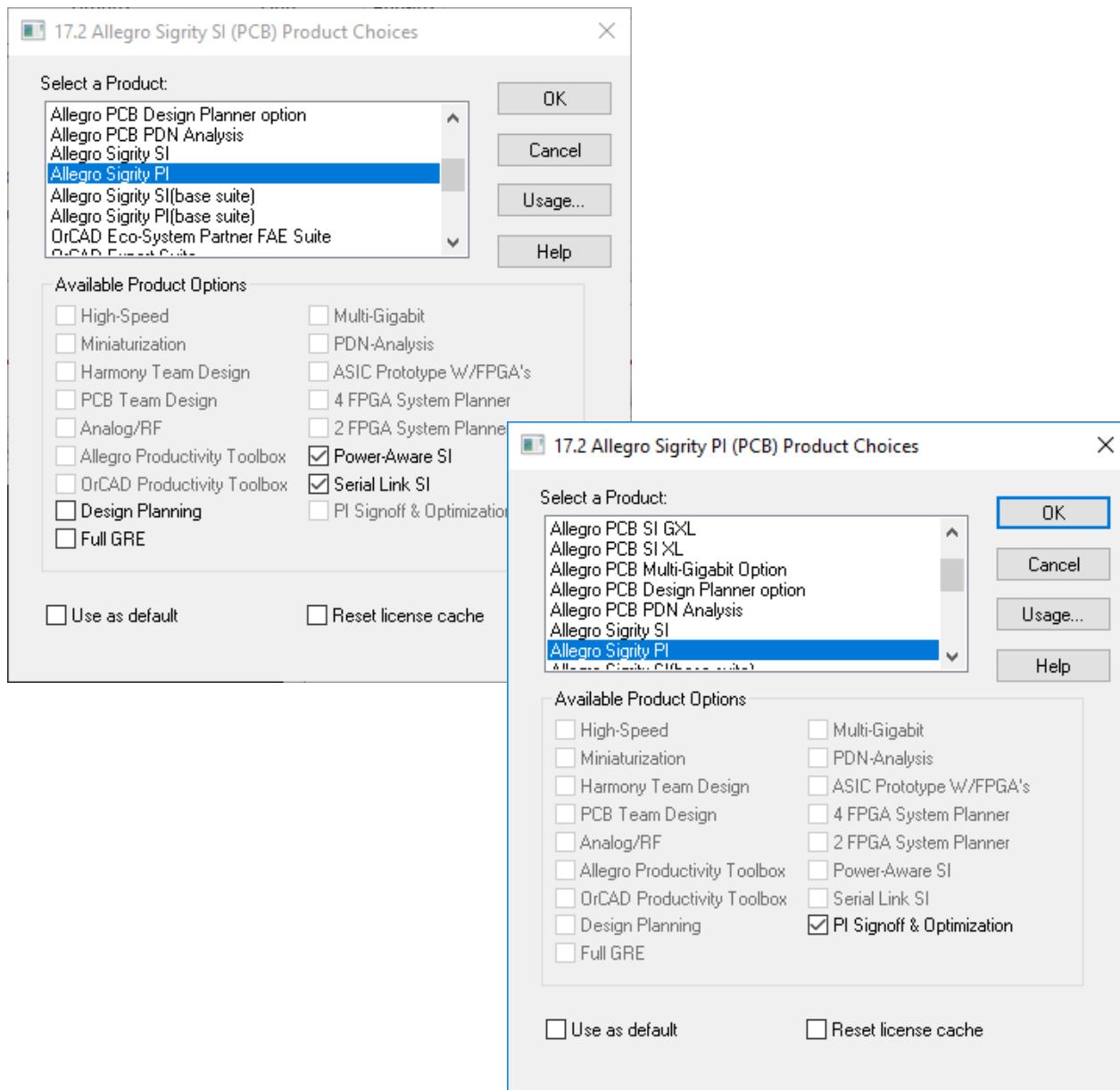
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Allegro Sigrity PI with Other Products

Allegro Sigrity PI is available for selection in the product list in the following products:

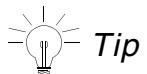
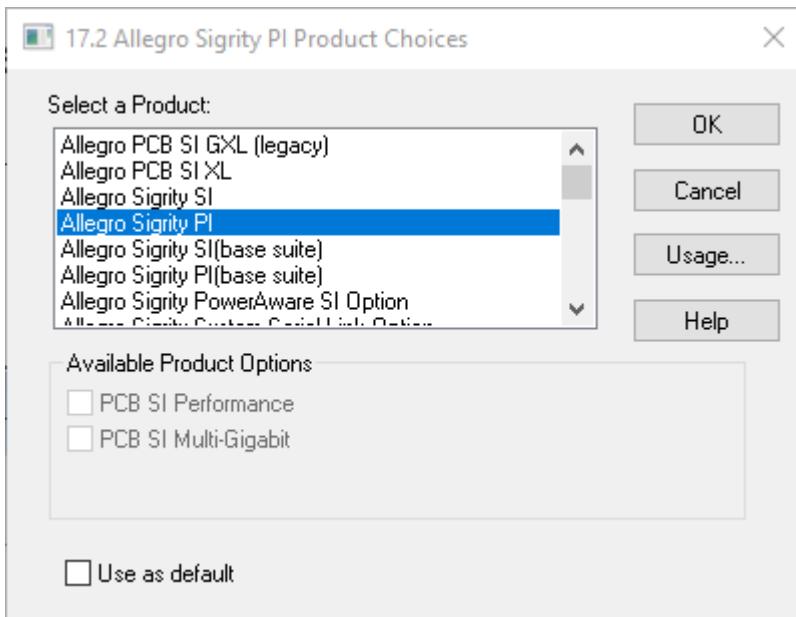
- Allegro PCB Editor and PCB SI
- Allegro Package Editor and APD SI product
- Allegro SIP Editor and SiP Digit SI product



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- Allegro Sigrity PI is also available for selection in the product list for Allegro SigXplorer.

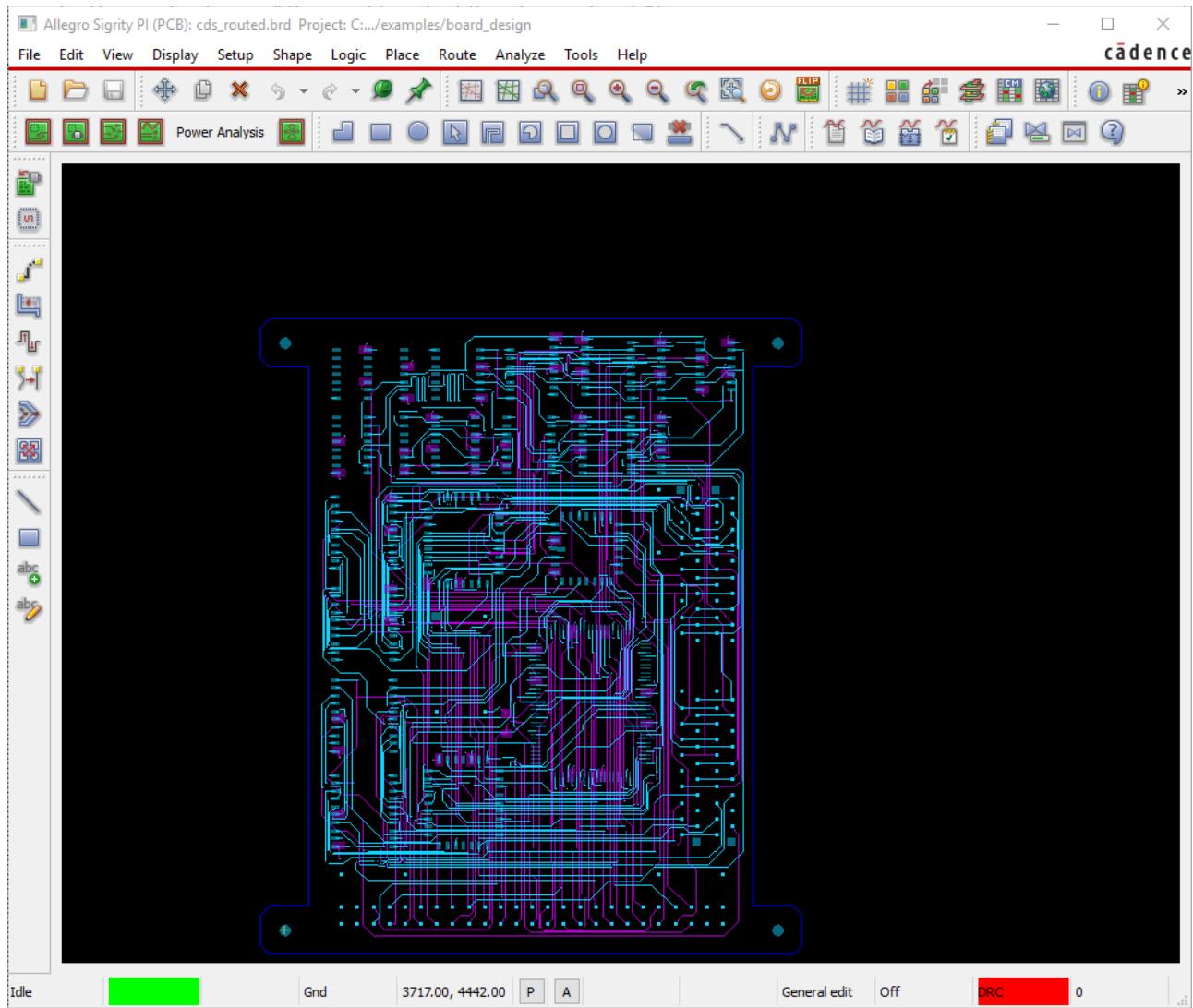


You can also use the *File – Change Editor* command to switch to the Allegro Sigrity PI product from within your current Allegro product selection.

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Depending on the database, board, package, or SIP, with which you want to use the product, you can make a choice from the list along with the available product options. When you have made the selection, Allegro Sigrity PI is launched.

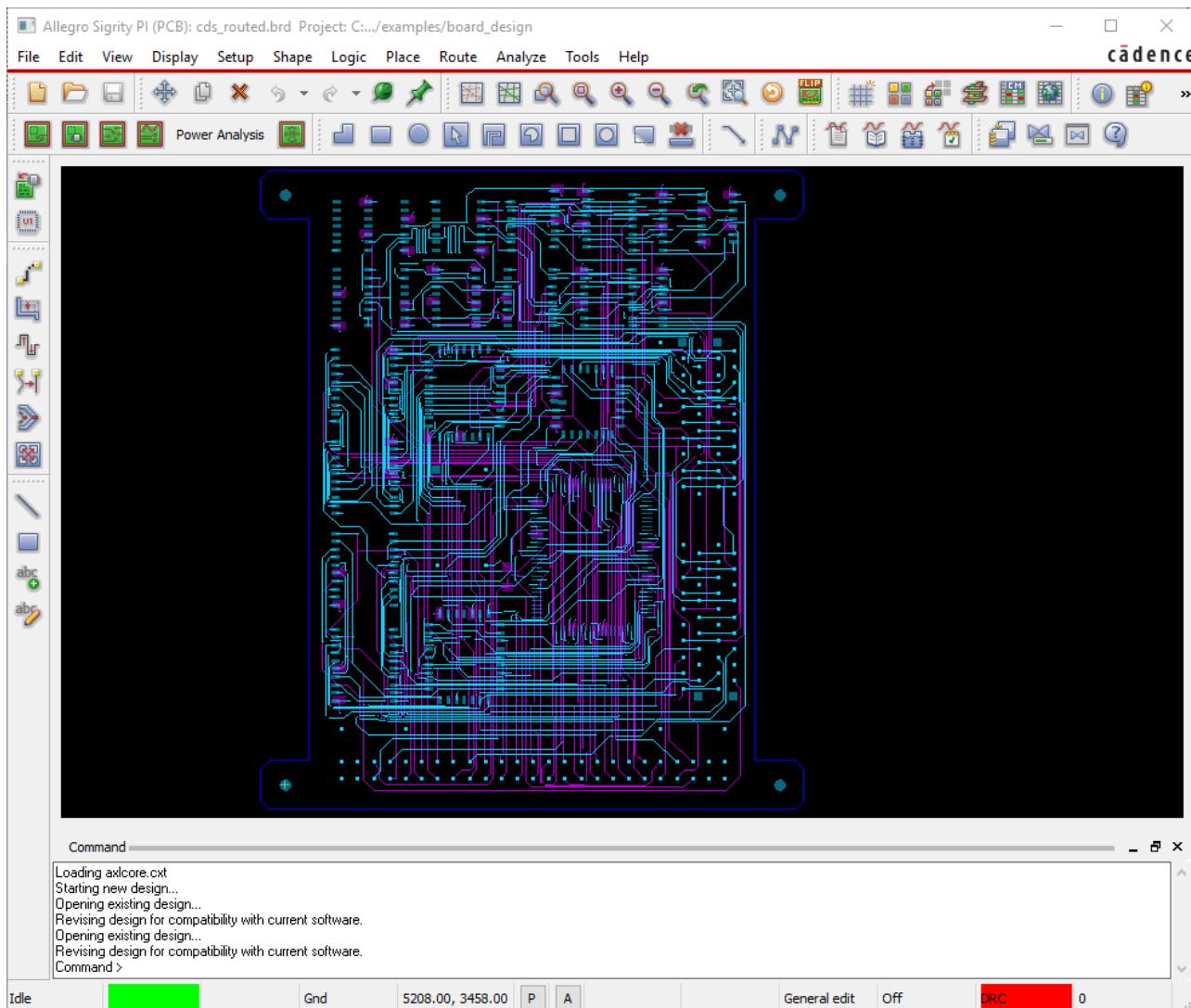


Calling Cadence Sigrity Tools from Allegro Sigrity PI

From within Allegro Sigrity PI, you can directly open Allegro board files (.brd), APD files (.mcm), and SIP files (.sip) in a Cadence Sigrity tool without having to first explicitly translate the files into the Cadence Sigrity tools format.

Note: The Cadence Sigrity tools work with a translated database (.spd) from a variety of file formats.

1. Launch Allegro Sigrity PI and open a .brd file.



2. Launch any Cadence Sigrity tool. For example, PowerSI.

You can launch the Cadence Sigrity tools from the following two menus:

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- ❑ *Tools – <tool_name>*: When the tool is launched from the *Tools* menu, it opens a blank workspace. You can create a new design or open an existing design.
- ❑ *Analyze – <tool_name>*: When the tool is launched from the *Analyze* menu, first the XNet Selection dialog box appears where you select the nets and XNets to be analyzed. The Allegro layout is then internally translated and opened in the desired Cadence Sigrity tool.

When you choose to launch any of the Cadence Sigrity tools from the *Analysis* menu, the XNet Selection dialog appears.

Note: You can also launch the Cadence Sigrity tools by Suppressing the XNet Selection Dialog.

Selecting XNets for Analysis

You can select the nets or XNets from the available nets and launch the appropriate Cadence Sigrity tool to analyze the selected nets.

3. Select the required XNets.

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You can also set a few preferences before launching Cadence Sigrity tools from within Allegro Sigrity PI.

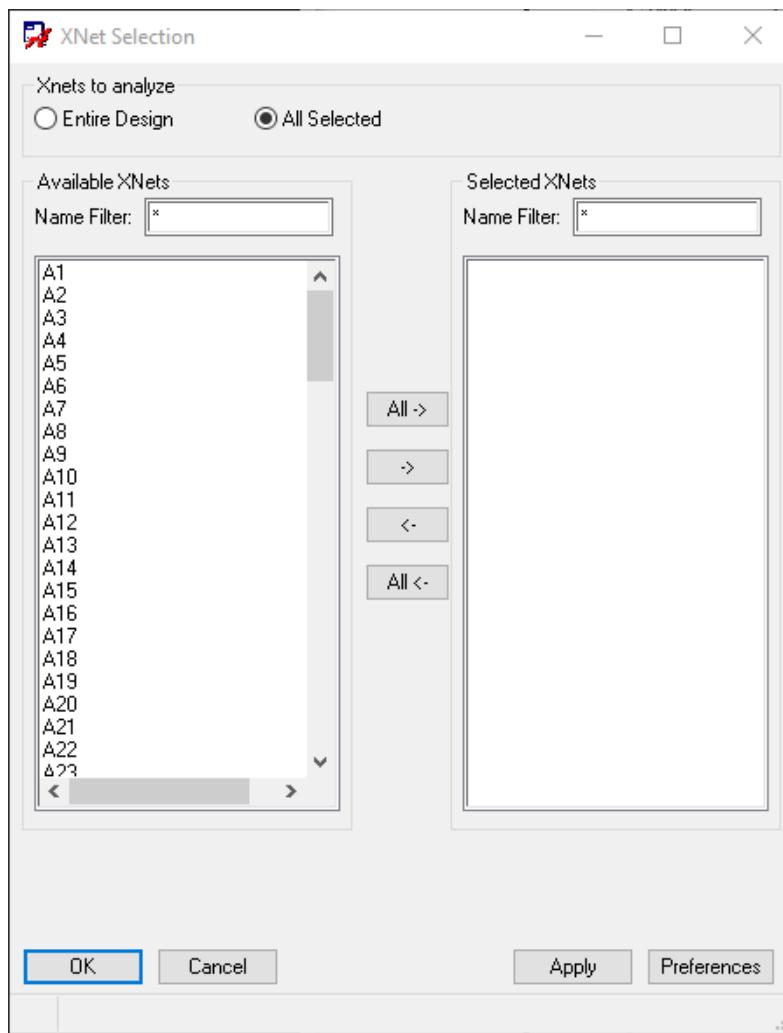


Table 1-1 XNet Selection Dialog

Option	Description
XNets to analyze	Specify whether to analyze the selected XNets or all the XNets in the entire design.
Available XNets	Displays a list of all the XNets in the design.

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Selected XNets Displays a list of selected XNets from the design.

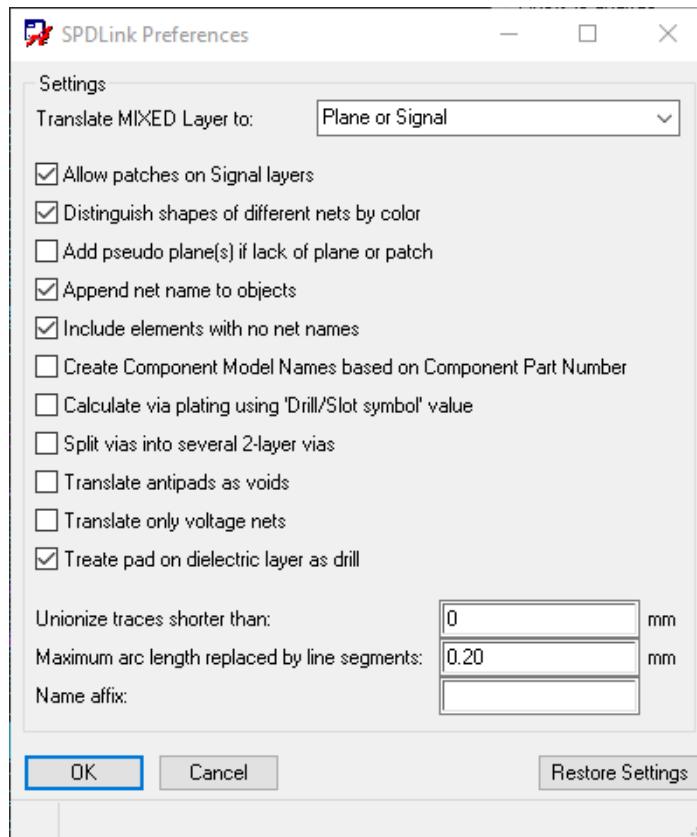
Apply Saves the XNet selection for later commands and analysis.

Preferences Launches the [Preferences Dialog](#) to change the settings for opening the layout file in the Cadence Sigrity tool.

Setting Preferences to Export Allegro Layout to Cadence Sigrity Tools

You can set these preferences and parameters in the *Preferences* dialog.

4. To launch the Preferences dialog, click the *Preferences* button in the [XNet Selection dialog box](#).



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Table 1-2 Preferences Dialog

Option	Description
Translated MIXED Layer to	Determines how to translate mixed layers in the Allegro layout file to the Allegro Sigrity format. <i>Plane Layer</i> is selected by default. <ul style="list-style-type: none"> ■ <i>Plane Layer</i>: The MIXED layers are translated to Plane layers. Traces on these layers are ignored. ■ <i>Plane or Signal</i>: The translator checks if the MIXED layer contains traces. If traces are found, it translates the layer to a Signal layer. Else, it translates the layer to a Plane layer. ■ <i>Signal</i>: The MIXED layers are translated to Signal layers.
Allow patches on Signal layers	Translates patches on signal layers. This option is selected by default.
Distinguish shapes of different nets by color	The translator assigns shape components of nets with colors of the selected nets. If this option is unchecked, the translator assigns shape components with the default color of the shape. This option is selected by default.
Add pseudo plane(s) if lack of plane or patch	The translator adds an extra pair of Planes to the bottom of the structure in the output file, if all metal layers do not have patches. If only one metal layer has patches, an extra metal Plane layer is added to the bottom of the structure in the output file.
Append net name to objects	The translator adds net names to object names. This option is selected by default.
Include elements with no net names	Translates elements without net names. If this option is cleared, the translator will NOT translate elements without net names. This option is selected by default.
Create Partial Ckt Names based on Component Part Number	The translator creates partial Ckt names based upon component part number.
Calculate via plating using 'Drill/Slot symbol' value	The translator uses the "Drill/Slot hole" as the outer diameter and "Drill/Slot symbol" as inner diameter.
Split vias into several 2-layer vias	The translator splits vias into several 2-layer vias to show inner pads (pad on all layers).

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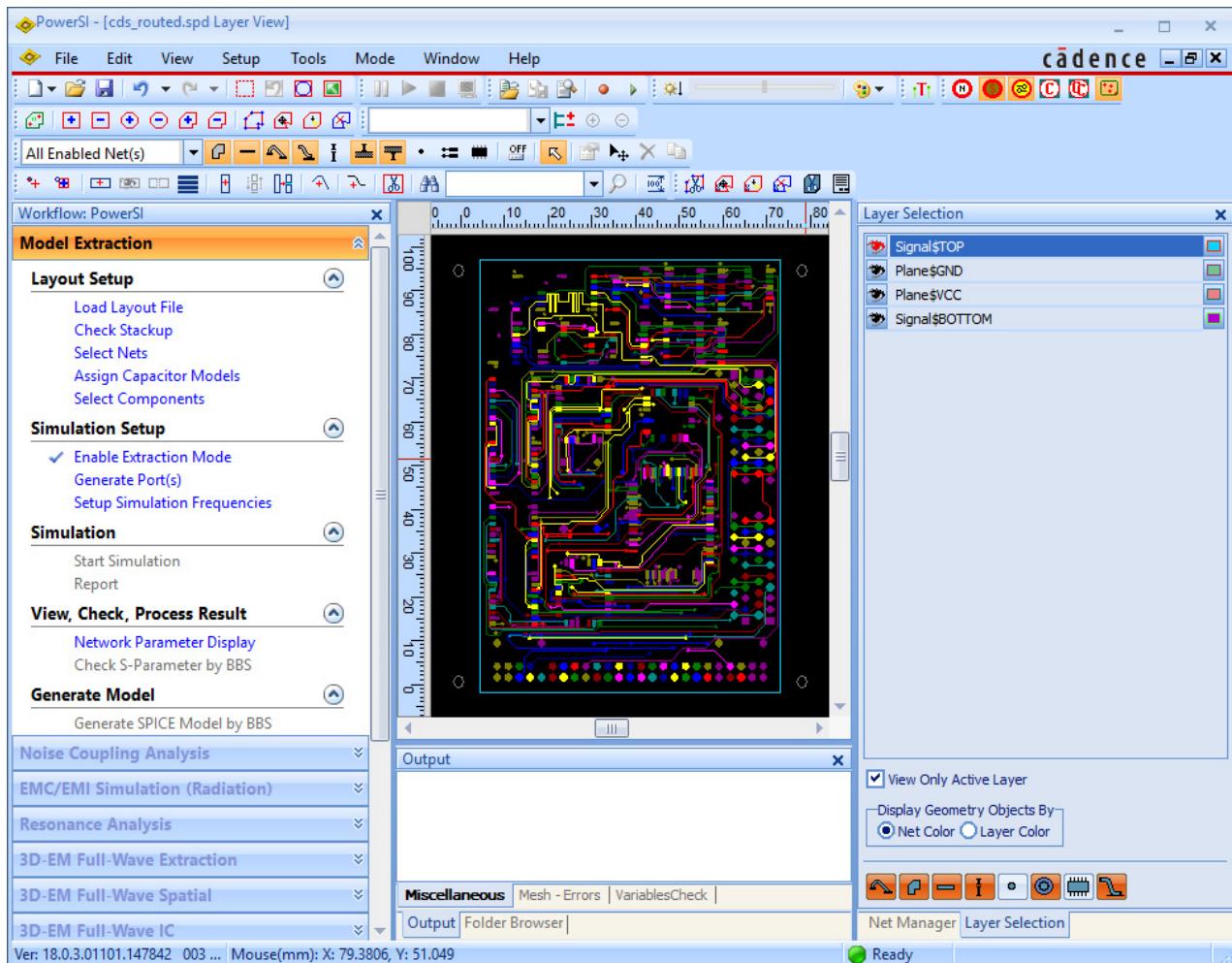
Option	Description
Translate antipads as voids	Translates antipads as voids.
Translate only voltage nets	Translates only voltage nets.
Treat pad on dielectric layer as drill	The translator treats a pad on the dielectric layer as drill. This option is selected by default.
Unionize traces shorter than	The translator discards any traces shorter than this value. The default value is 0 mm, implying that by default no traces are discarded.
Maximum arc length replaced by line segments	Translates arcs to line segments of this value or shorter to ensure smooth appearance. The default value is 0.2 mm.
Name affix	<p>The translator adds this string in the field to the names of all the layers, nodes, vias, and traces.</p> <p>This option is useful when you combine two .spd files together.</p>

5. Click *OK* to close the Preferences dialog.
6. Click *OK* in the XNet Selection dialog to launch the Allegro Sigrity tool.

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The Cadence Sigrity tool launches.



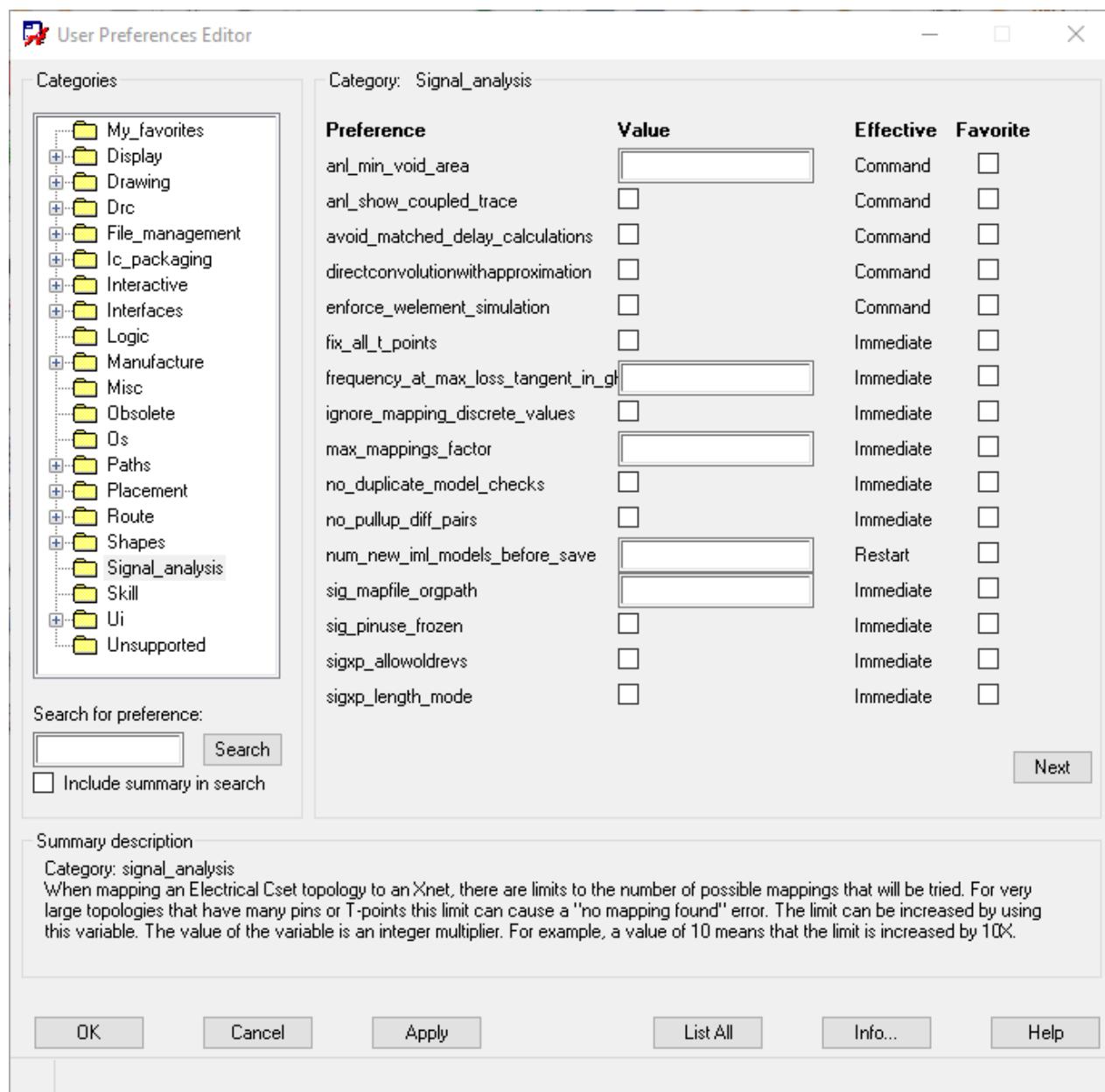
Suppressing the XNet Selection Dialog

When you launch a Sigrity application from Allegro Sigrity PI, you might want to translate the entire design instead of specific nets and Xnets selected in the [XNet Selection dialog box](#). You can choose to launch the Cadence Sigrity tool directly by translating the entire design without displaying the XNet Selection dialog. To do this, select the *translate_entire_design*

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attribute under the *Signal_analysis* category of *User Preferences Editor* in Allegro Sigrity PI:

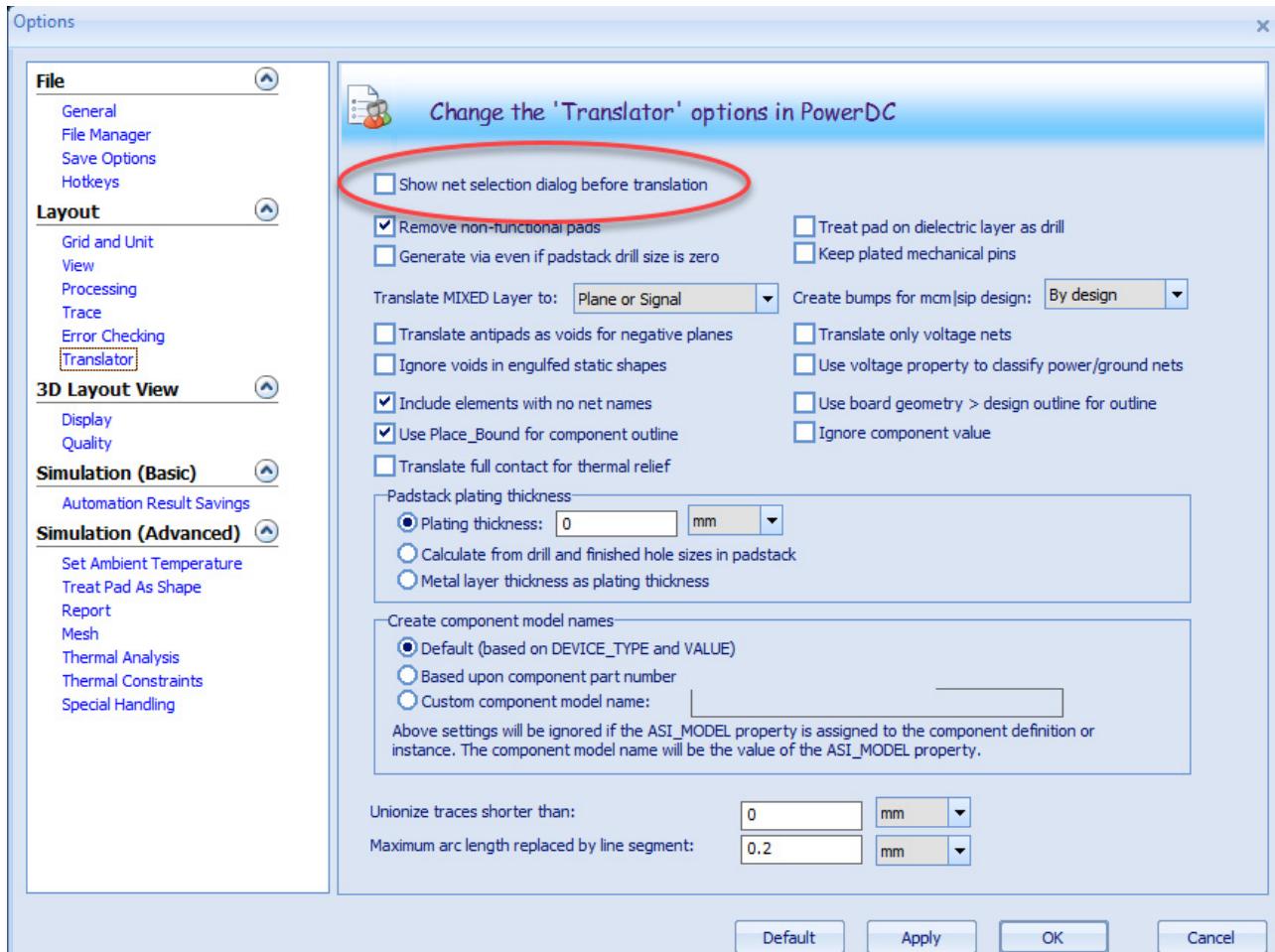


On the other hand, when loading an Allegro Sigrity PI database directly in a Cadence Sigrity tool (*File – Open*), you might want to choose specific nets and Xnets before launching the

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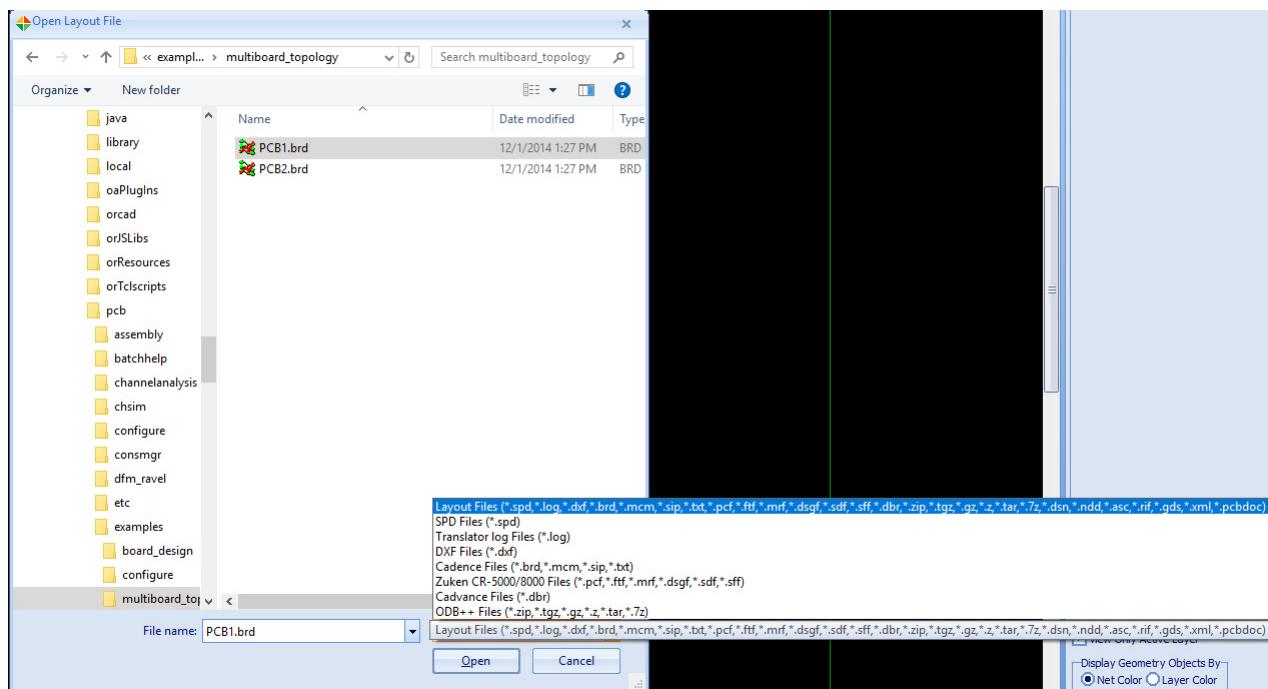
database. For such cases, you can select the *Show Net Selection Dialog before Translation* option in the Options dialog box in the Cadence Sigrity tool.



Opening Allegro Sigrity PI Layout Files in Cadence Sigrity Tools

You can also open the Allegro Sigrity PI layout files (.brd, .mcm, and .sip) directly from the Cadence Sigrity tools.

1. Choose *File – Open*.
2. In the Open dialog, browse to the location which stores the Allegro layout files.
3. Select the file type as .brd, .mcm, or .sip.
The available layout files of the selected file type will be listed.
4. Click *Open* to open the layout file in the Cadence Sigrity tool.

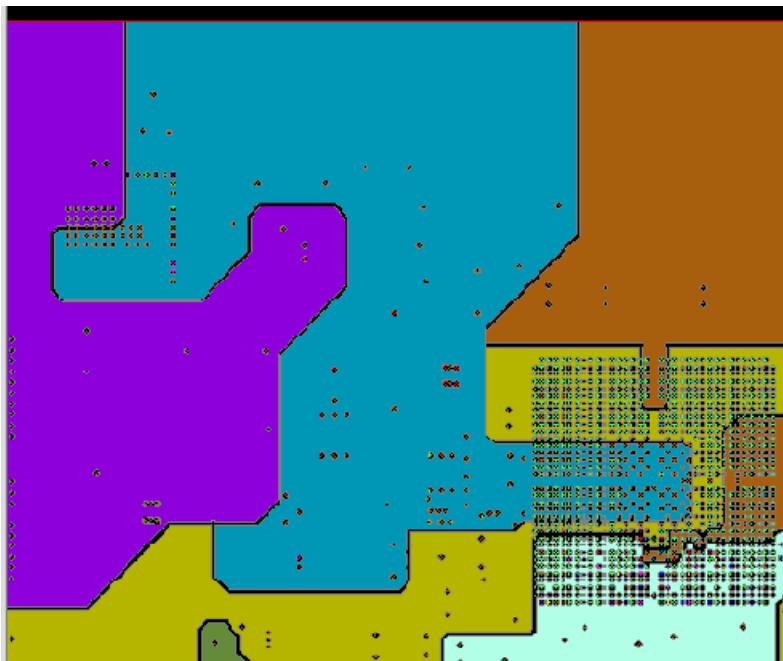


Updating Sigrity Layout Tools with Allegro Sigrity PI Data

The updates made in Allegro Sigrity PI layout can be reflected in a Cadence Sigrity layout tool almost immediately, without having to translate the entire database each time an update is made. For example, edits to a shape or a trace can be updated directly to sync the two applications.

Example

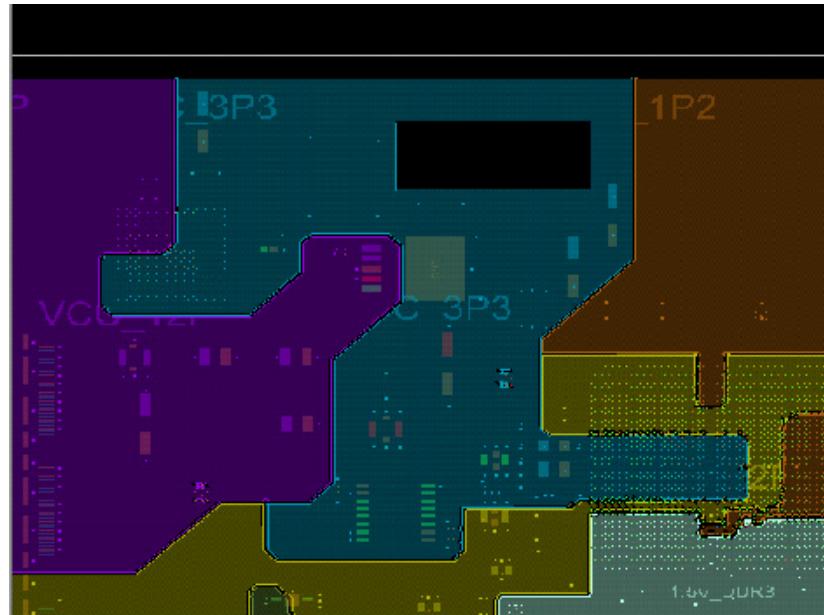
The shape illustrated in the following figure in a Cadence Sigrity tool appears exactly as it does in Allegro Sigrity PI:



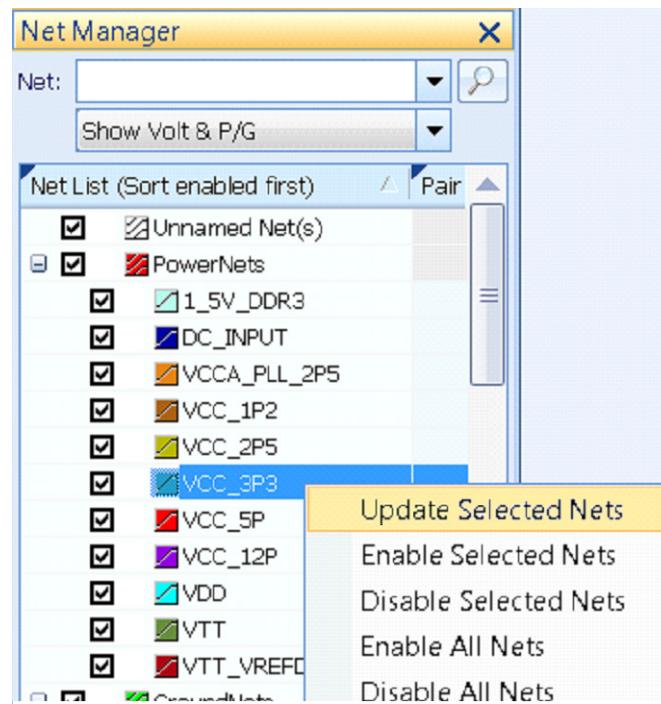
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To perform a what-if analysis, a void is added in Allegro Sigrity PI as illustrated in the following image:



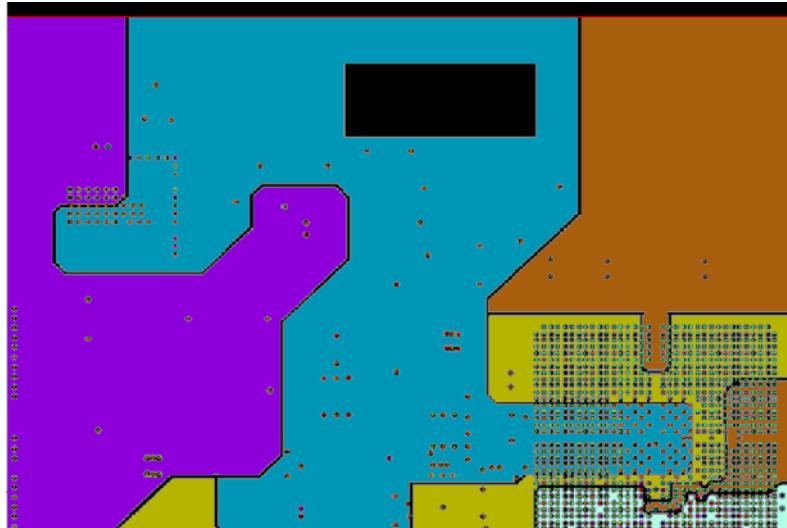
To update the Cadence Sigrity tool with the Allegro Sigrity PI data, right-click the nets you want to update in *Net Manager* and choose *Update Selected Nets* from the context menu.



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The change is instantly reflected in the Cadence Sigrity tool's canvas.



This feature is only available in the following Sigrity layout-based tools launched from Allegro Sigrity SI or Allegro Sigrity PI:

- PowerDC
- PowerSI
- SPDGEN
- XtractIM

Note: Both Allegro Sigrity PI and the launched Sigrity application must remain open to enable this dynamic syncing.

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Working with the Decap Flow

This chapter covers the following topics:

- [Overview](#)
- [Decap Template](#)
- [Working with Power Feasibility Editor](#)
- [Using Decap Templates in Constraint Manager](#)
 - [Selecting Decoupling Capacitors](#)
 - [Referencing PICSet](#)
 - [Creating a PICSet in Constraint Manager](#)
 - [Editing PICSets](#)
 - [Auditing PICSet](#)
 - [Reusing PICSets](#)
- [Placing Decaps](#)
- [Displaying Power Pins and Effective Radius Post Placement](#)
- [Replicating Decap Placement](#)

Overview

A *Decap Template* defines the number, types, and placement of Decoupling Capacitors (decaps) for each power rail of an IC. A decap template is associated with the power distribution system of an IC. As part of the Allegro Sigrity PI Decap flow, Power Feasibility Editor (PFE) can be used to generate a decap template in the pre-layout phase. The flow can be used to add decaps to the design or to identify and place decaps already in the design.

Decap Template

You can create a decap template using PFE. The template you create in PFE is saved as a Power Integrity CSet (PICSet) in Constraint Manager, and the related IC components store the name of the PICSet as a property. You apply a PICSet to devices in Constraint Manager. You can also add, edit, and analyze a decap template in Constraint Manager. You can then place the decaps according to the template in the Allegro design.

For more information, see [Using Decap Templates in Constraint Manager](#).

A Decap Template contains the following information:

- Name of the template
- Voltage rails for the part
- For each of the rails:
 - Setback distance
 - Same layer
 - Opposite layer
 - Part number and quantity of discrete capacitors required
 - For each cap/Part number:
 - Quantity on the same layer, opposite layer, underneath
 - Package name

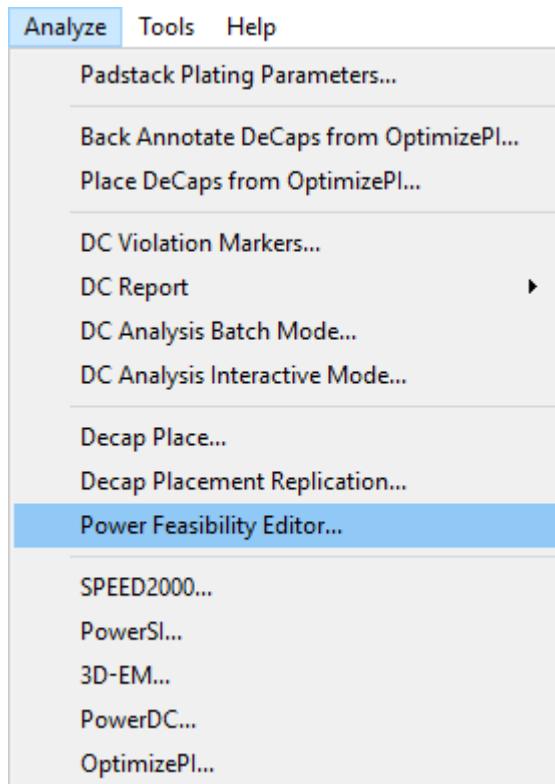
Working with Power Feasibility Editor

You use Power Feasibility Editor to create a decap template. PFE is available only with the Allegro Sigrity PI license. PFE provides the Decap Selection Flow. It also provides you with an option to customize the workflow. There are two use models that PFE follows:

- **No Simulation:** Data in PFE is either read from an IC model or entered directly in the user interface. You can select decaps without performing any additional analysis.
- **Simulation-based:** You can load a target impedance profile and PFE performs simple calculations for the profile. Decap selection is driven by the Single Node Analysis capability within PFE.

Regardless of which use model is employed, results are passed to the layout as a decap template. To generate a decap template, do the following steps:

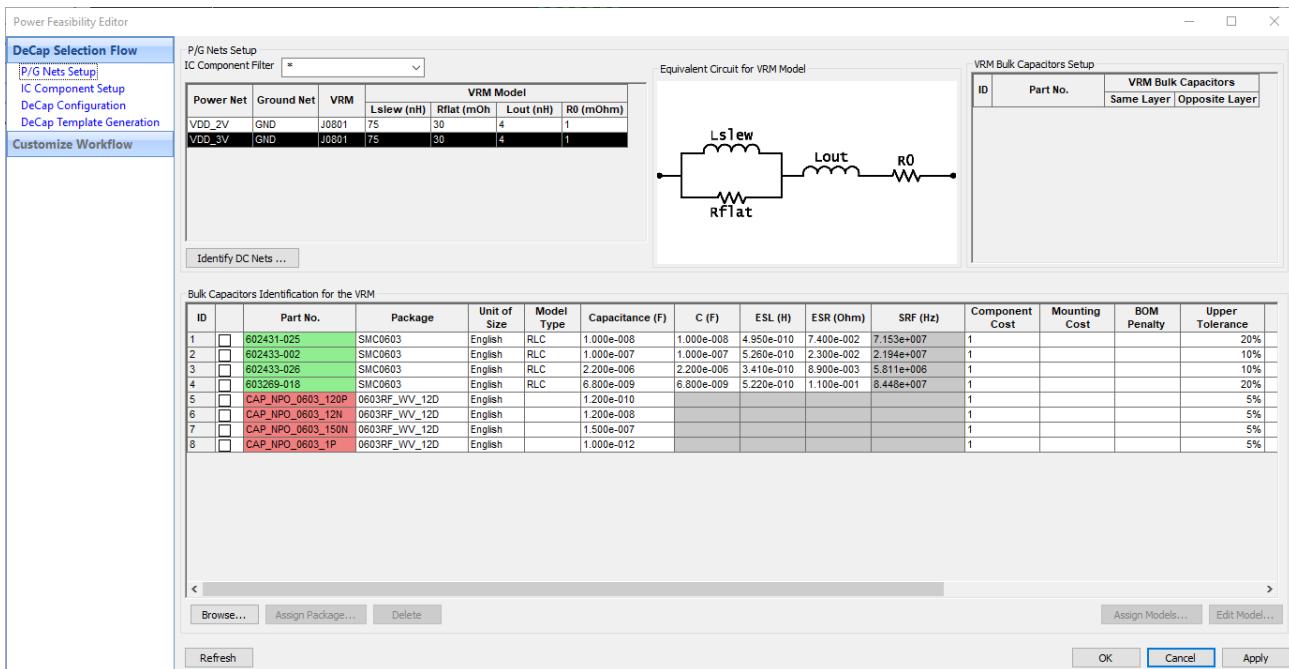
1. Launch Allegro Sigrity PI.
2. Open the board design.
3. Choose *Analyze – Power Feasibility Editor*.



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Working with the Decap Flow

The PFE window opens.



Selecting Decoupling Capacitors

The following tasks comprise the Decap Selection workflow:

- Set up P/G Nets
- Set up IC Components
- Set Up Decap Preferences
- Generate Decap Template

Set up P/G Nets

1. Click *P/G Nets Setup* to identify the power and ground nets.
2. Set up the power and ground net pair for the required power nets.

Power nets can be filtered by an IC component. For example, if you select U1 as the IC Component Filter, only the power nets attached to U1 are listed. If you select All as the IC Component Filter, all the power nets will be listed.

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Working with the Decap Flow

3. If no DC nets are populated here or if the power nets to be listed here are not populated, click *Identify DC Nets* to identify DC nets.
4. Define a ground net for each power net to determine and complete the connectivity of components in the design.

This step is necessary for decap verification.

Identify a Component as the VRM Component

1. Identify a component as the VRM component for the power ground net pair selected earlier from the component list under the VRM column.
2. Define the VRM model by specifying the following parameters under *VRM Model*:
 - Lslew (nH)
 - Rflat (mOh)
 - Lout (nH)
 - R0 (mOhm)
3. You can view the Equivalent Circuit for VRM Model to decide how to define the VRM model.

Table 2-1 Power Feasibility Editor – P/G Nets Setup

Field	Description
<i>IC Component Filter</i>	Filters power nets by IC component. For example, if you specify U1 in the filter, only the power nets attached to U1 are listed. By default, the filter is set to * (asterisk) which means that all the power nets are listed. If you select an IC component and then start PFE, the filter is set to the selected IC component and the attached power nets are listed.
<i>Identify DC Nets</i>	Opens the <i>Identify DC Nets</i> dialog to assign a valid DC value for each DC net.
<i>Power Net</i>	Displays the net name of the power net.
<i>Ground Net</i>	Displays the net name of the ground net.
<i>VRM</i>	Select an IC/IO as VRM from the component list.

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Working with the Decap Flow

Field	Description
<i>VRM Model</i>	Defines a simple VRM model based on the following parameters: <ul style="list-style-type: none">■ Lslew (nH)■ Rflat (mOhm)■ Lout (nH)■ R0 (mOhm)

Identify Bulk Capacitors for the VRM

All the capacitors in the design are displayed. You can add more Capacitors to the list from the Capacitor library, if required.

You need to select the capacitors associated with the VRM component you identified in the previous step. The capacitors with correct modeling information are colored green while the ones in red have some issues with model assignment. A capacitor marked as selected belongs to the current selected power net.

1. In the Bulk Capacitors Identification for the VRM section, select the capacitors associated with the VRM component identified in the previous step.
2. Select each capacitor by selecting the check box to the left of the capacitor part number.

As you select a capacitor, it is added to the list of parts in the VRM Bulk Capacitors Setup section. Caps are associated with a VRM is used only in the Single node analysis.

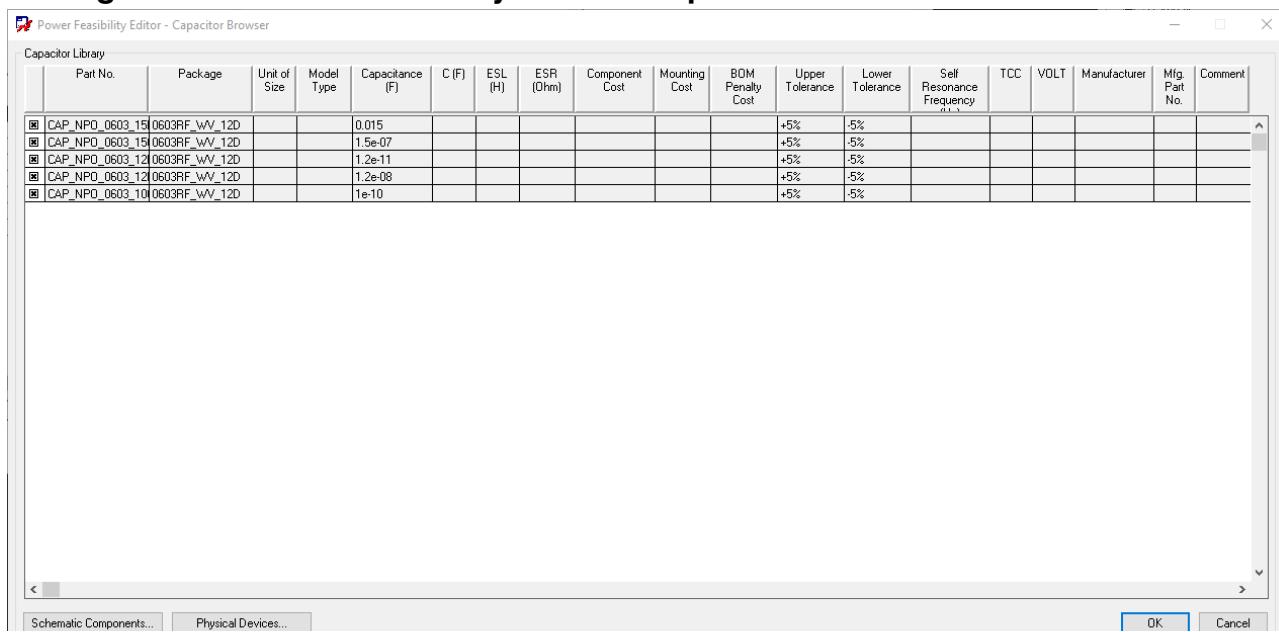
3. Click the *Browse* button.

The *Power Feasibility Editor — Component Browser* opens. You add capacitors to the list from either the schematic or the physical design.

Allegro Sigrity PI Flow Guide

Working with the Decap Flow

Figure 2-1 Power Feasibility Editor – Capacitor Browser



You can also add other capacitors from schematic components or physical devices from the Capacitor Browser.

4. Click *Schematic Components*, specify the path to the cpm file.

The Capacitor Browser is populated with the capacitors from the logical schematic.

5. To add physical devices, click *Physical Devices*.

6. Select physical devices files from the Library Browser one at a time.

Component Browser is populated with the physical devices you selected.

If the package definition for any device is not found, an error message appears.

Fields	Description
<i>ID</i>	Capacitor model index number. Click on the ID can highlight the capacitor in the list.
<i>Part No.</i>	Capacitor part number.
<i>Package</i>	Package symbol of capacitor.
<i>Unit of Size</i>	Unit of package size which could be English or Metric. Default is English.
<i>Model Type</i>	Model type of capacitor which could be RLC or SPICE.

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Working with the Decap Flow

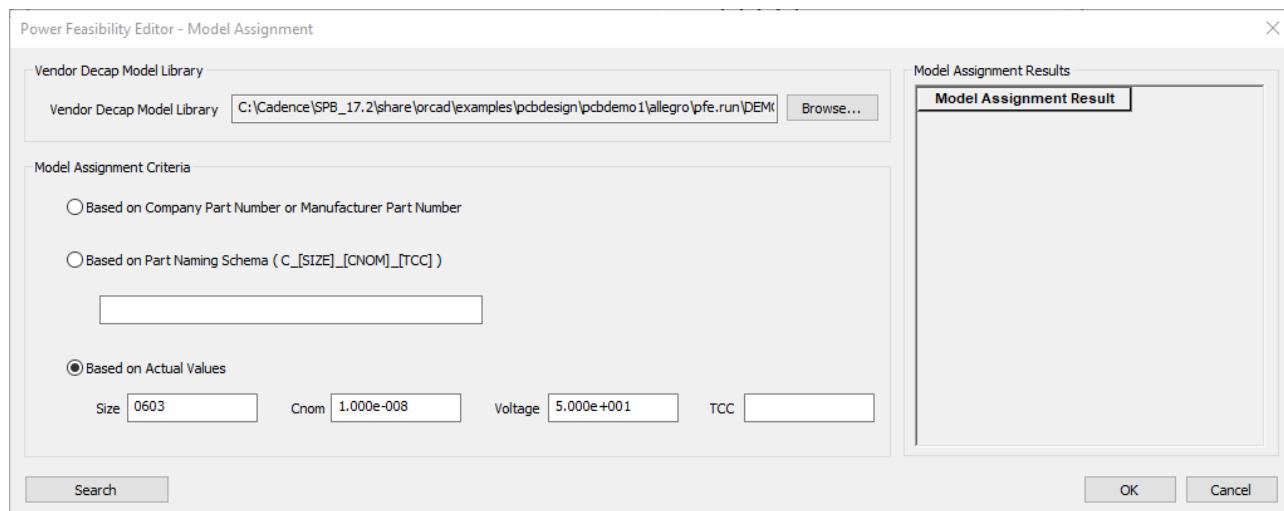
Fields	Description
<i>Capacitance (F)</i>	Capacitance of the component.
<i>C (F)</i>	C value specification for simple RLC model.
<i>ESL (H)</i>	ESL value specification for simple RLC model.
<i>ESR (Ohm)</i>	ESR value specification for simple RLC model.
<i>Component Cost</i>	Capacitor component cost (CC).
<i>Mounting Cost</i>	Assembly cost (MC).
<i>BOM Penalty</i>	Additional assembly cost for mounting the first component (BOM). Assume there are N components selected, the total cost is $TC=N^*(CC+MC)+BOM$.
<i>Upper Tolerance</i>	Upper tolerance of a capacitor expressed in percentage.
<i>Lower Tolerance</i>	Lower tolerance of a capacitor expressed in percentage.
<i>Self Resonance Frequency (Hz)</i>	Self resonance frequency calculated by PFE.
<i>TCC</i>	Temperature characteristic, such as X5R, X7R etc.
<i>VOLT</i>	Rated voltage.
<i>Manufacturer</i>	Capacitor vendor.
<i>Mfg. Part No.</i>	Capacitor part number from vendor.
<i>Comment</i>	You can write any comments or remarks here.
<i>Browse</i>	Add capacitors from schematic components and/or physical devices.
<i>Assign Package</i>	Assign package symbol for highlighted one or more capacitors.
<i>Delete</i>	Delete the highlighted capacitors from current capacitor library.
<i>Assign Models</i>	Find matched models from vendor library and assign them to the highlighted capacitors.
<i>Edit Model</i>	Edit/create model for the highlighted capacitor.

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Working with the Decap Flow

Assign Model

You can also assign models to selected capacitors in this form. Click the *Assign Models* button and the PFE – Model Assignment dialog is displayed. You can assign models to decaps by specifying a model assignment criteria.



Field	Description
<i>Vendor Decap Model Library</i>	Specify the path to one of the vendor libraries.
<i>Model Assignment Criteria</i>	Based on Company Part Number or Manufacturer Part Number – Find matched decap models based on company part number or manufacturer part number. Based on Part Naming Schema – Find matched decap models based on the part naming schema that you define. Based on Actual Values – If you have selected only a single capacitor for model assignment, a matching model can be found based on some key values, such as Size (package size), Cnom (capacitance), Voltage (rated voltage) and TCC (temperature characteristics).
<i>Search</i>	Finds a matched models from the specified vendor library based on the model assignment criteria defined.
<i>Model Assignment Results</i>	Displays the results of the matching models. The checked model under each capacitor will be assigned to the capacitor. The first model under each capacitor is enabled by default.

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Working with the Decap Flow

Set up VRM Bulk Capacitors

The VRM Bulk Capacitors Setup list shows the number of capacitors to be placed at the same layer and at the opposite layer for each selected capacitors for the VRM.

ID	Part No.	VRM Bulk Capacitors	
		Same Layer	Opposite Layer
1	602431-025		
2	602433-002		
3	602433-026		
4	603269-018		
7	CAP_NPO_0603_150N		

Table 2-2 Power Feasibility Editor –VRM Bulk Capacitors Setup

Field	Description
<i>ID</i>	Capacitor index number.
<i>Part No.</i>	Capacitor part number.
<i>VRM Bulk Capacitors</i>	Setup VRM bulk capacitors for selected power ground net pair.

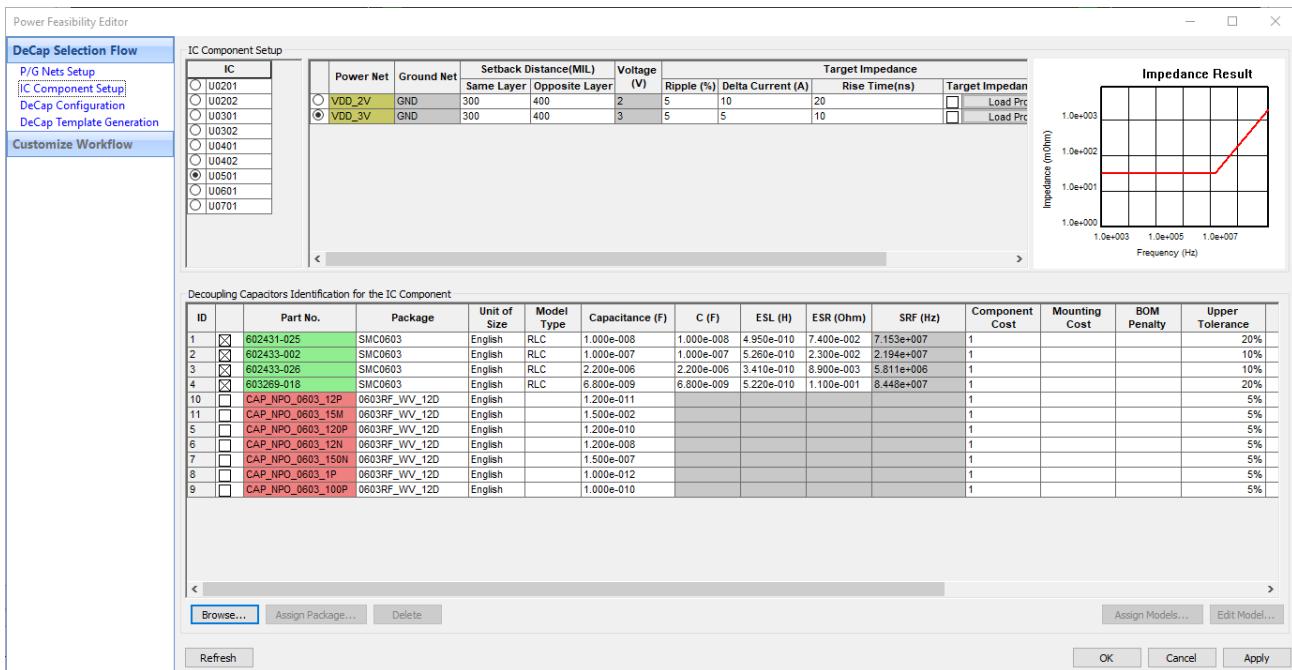
Set up IC Components

Next, you need to specify parameters to set up IC components:

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1. Click *IC Component Setup*.



2. Select an IC from the IC component list.

The power rails attached to the selected IC are populated.

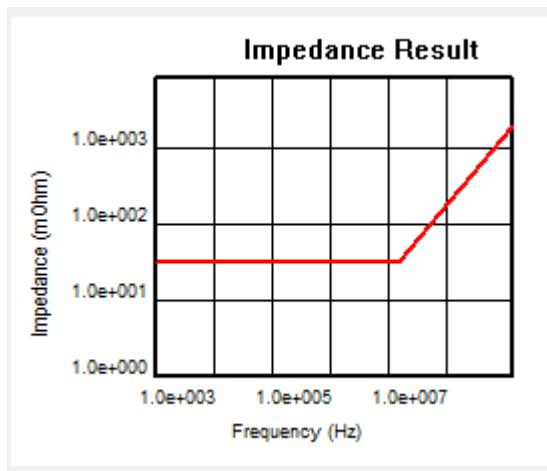
3. Select a power ground net pair.
4. Specify input setback distances.
5. Define Target Impedance.

The Target Impedance can be defined by Voltage Ripple (%), Delta Current (A) and Rise Time (ns). It also can be defined by loading a profile which defines the target impedance

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at each frequency point. You can view a simple target impedance curve at the top-right corner of the form.



6. Select the decaps for the currently selected IC and power ground net pair.

The capacitor library lists all the capacitors for the current design. The capacitors which belong to the selected DC nets and selected IC component are marked as selected.

This process is the same as the one followed for VRM, however, here the capacitors are selected as decaps to be part of the template.

Set Up Decap Preferences

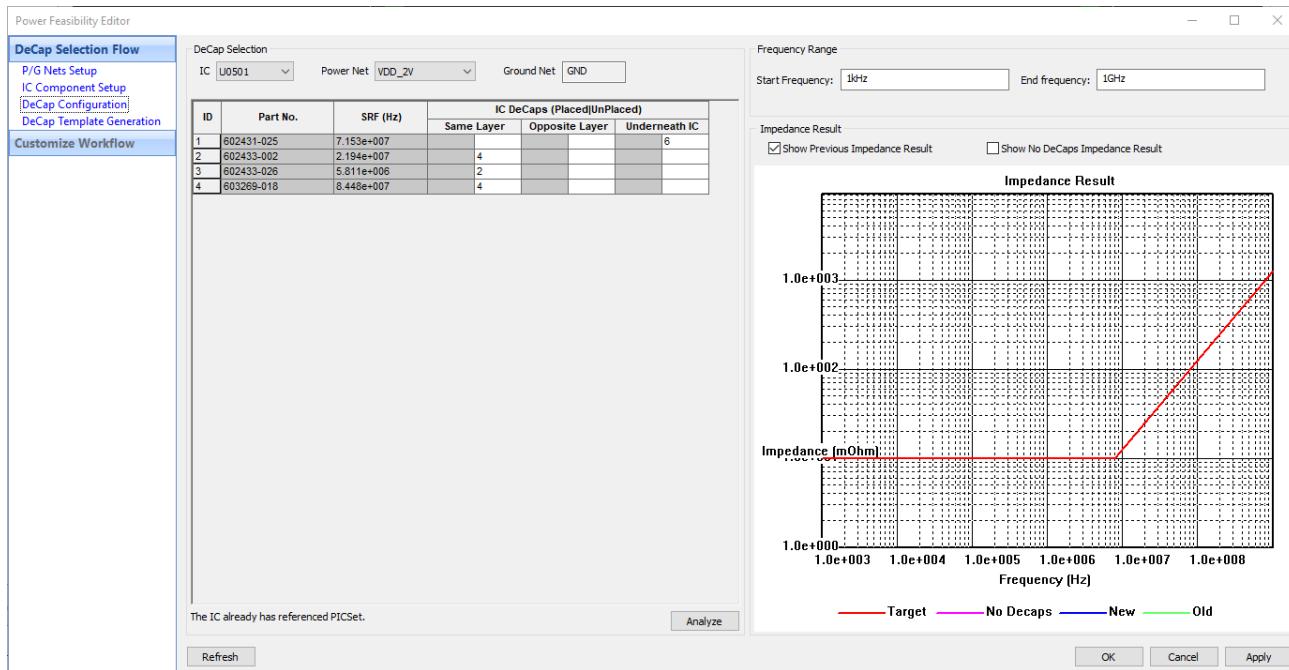
After setting up preferences for IC components, you need to specify decap preferences.

1. Click *DeCap Configuration*.
2. Specify the number of IC decaps to be placed on the same and opposite layers for the selected decaps.

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The greyed out columns represent the capacitors which are already placed in the design. The white columns are editable.



3. To view the impact of the decap selection, define the simulation frequency range.

4. Click Analyze to do an impedance analysis.

You can perform what-if analysis of the impedance by changing numbers of decaps assigned to various layers.

Table 2-3 Power Feasibility Editor – DeCap Setup

Field	Description
<i>ID</i>	Capacitor index number.
<i>Part No.</i>	Capacitor part number.
<i>Self Resonance Frequency (Hz)</i>	Self resonance frequency calculated by PFE.

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Field	Description
<i>IC DeCaps (Placed/UnPlaced)</i>	All Capacitors marked as selected in IC Component Setup are listed here. Placed: The number of decaps already placed in the design. UnPlaced: The number of decaps to be placed.
<i>Analyze</i>	Click to do an impedance analysis to verify current decap selection.
<i>Frequency Range</i>	Start Frequency: Define start frequency for analysis. End Frequency: Define end frequency for analysis.
<i>Impedance Results</i>	Target impedance and analysis results are displayed here. You can view these results to verify the decap selection.

Generate Decap Template

Finally, generate the decap template.

1. Click *DeCap Template Generation*.
2. Click *Generate* to generate a decap template.

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Working with the Decap Flow

The decap template are generated and sent to Constraint Manager and the summary is shown for reference.

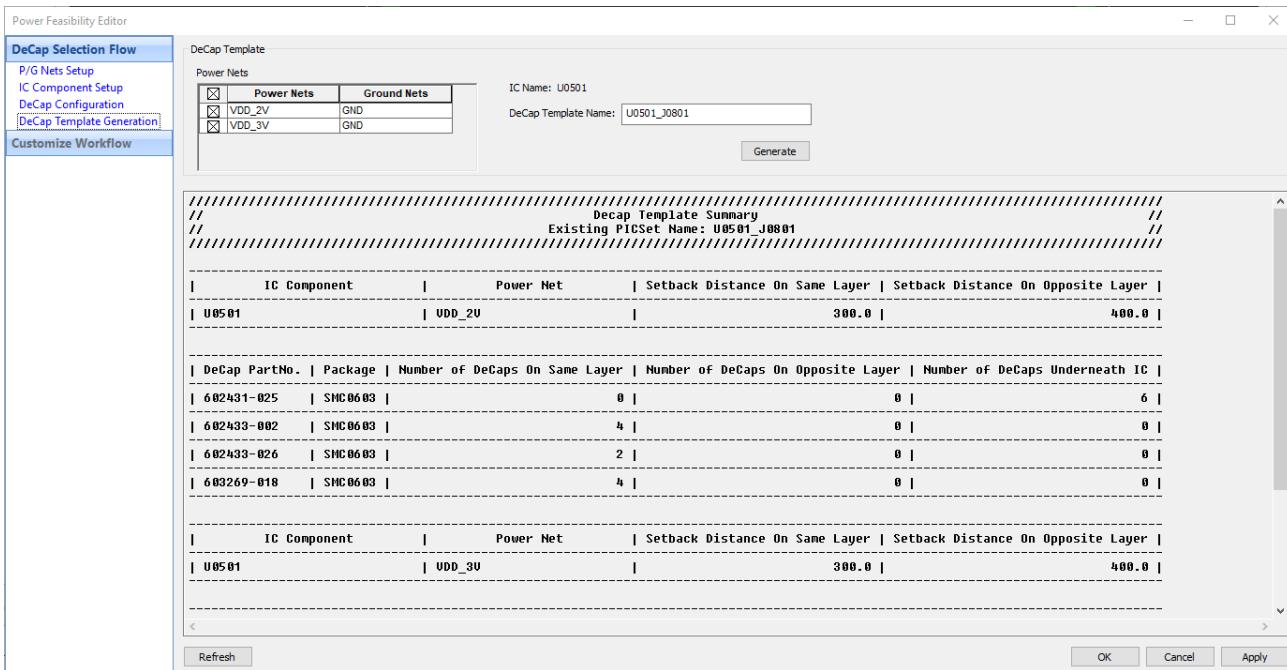


Table 2-4 Power Feasibility Editor – DeCap Template Generation

Field	Description
<i>DeCap Template Name</i>	PFE assigns a default decap template name. You can change it, if required.
<i>Generate</i>	Generates the decap template and send it to CM by API.
<i>DeCap template summary</i>	Provides a quick view of the content of the decap template.

Using Decap Templates in Constraint Manager

The decap template is saved in a PICSet in Constraint Manager, and the related IC component store the name of the PICSet as a property. You can modify the decap template created in Constraint Manager.

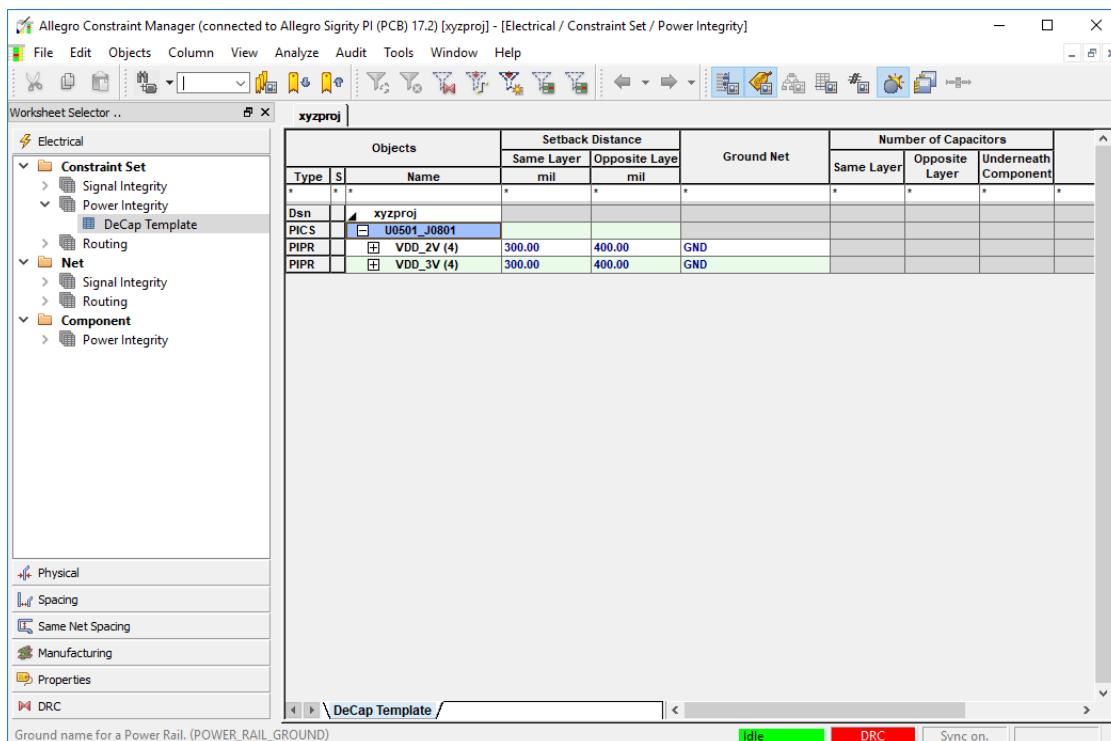
A PICSet serves as a convenient mechanism to communicate updated placement guidance or requirements for updates on decap selection (either type or quantity) for a specific device instance or all devices to which a PICSet is applied. Any changes to a PICSet also conveys information back to the design engineer and enables automated update of the schematic and BOM.

Referencing PICSet

To work with PICSet in Constraint Manager, do the following:

1. Choose *Setup – Constraints – Constraint Manager*. The Constraint Manager appears.
2. Click *Constraint Set – Power Integrity – Decap Template*.

Note that the decap template created in PFE, U0501_J0801 appears as a PICSet.



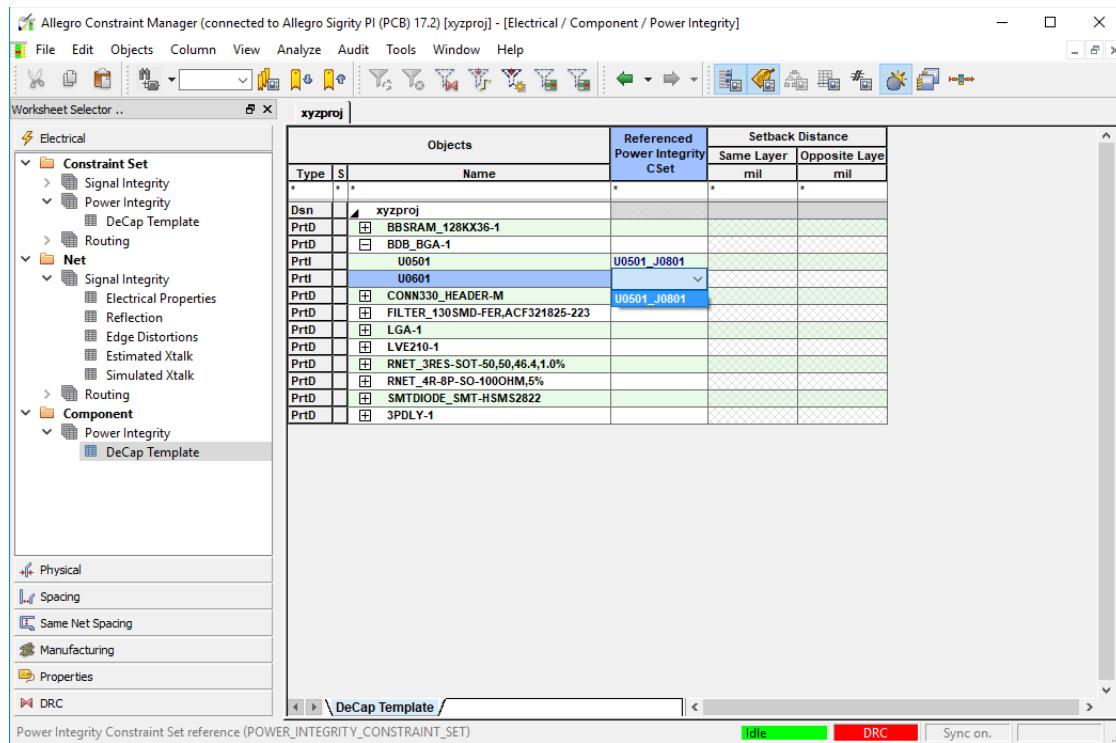
Allegro Sigrity PI Flow Guide

Working with the Decap Flow

3. Click Component – Power Integrity – DeCap Template.

In this example, PICSet, U0501_J0801, is referenced for U0501. A PICSet may be referenced by multiple IC components, allowing the decap template information to be reused.

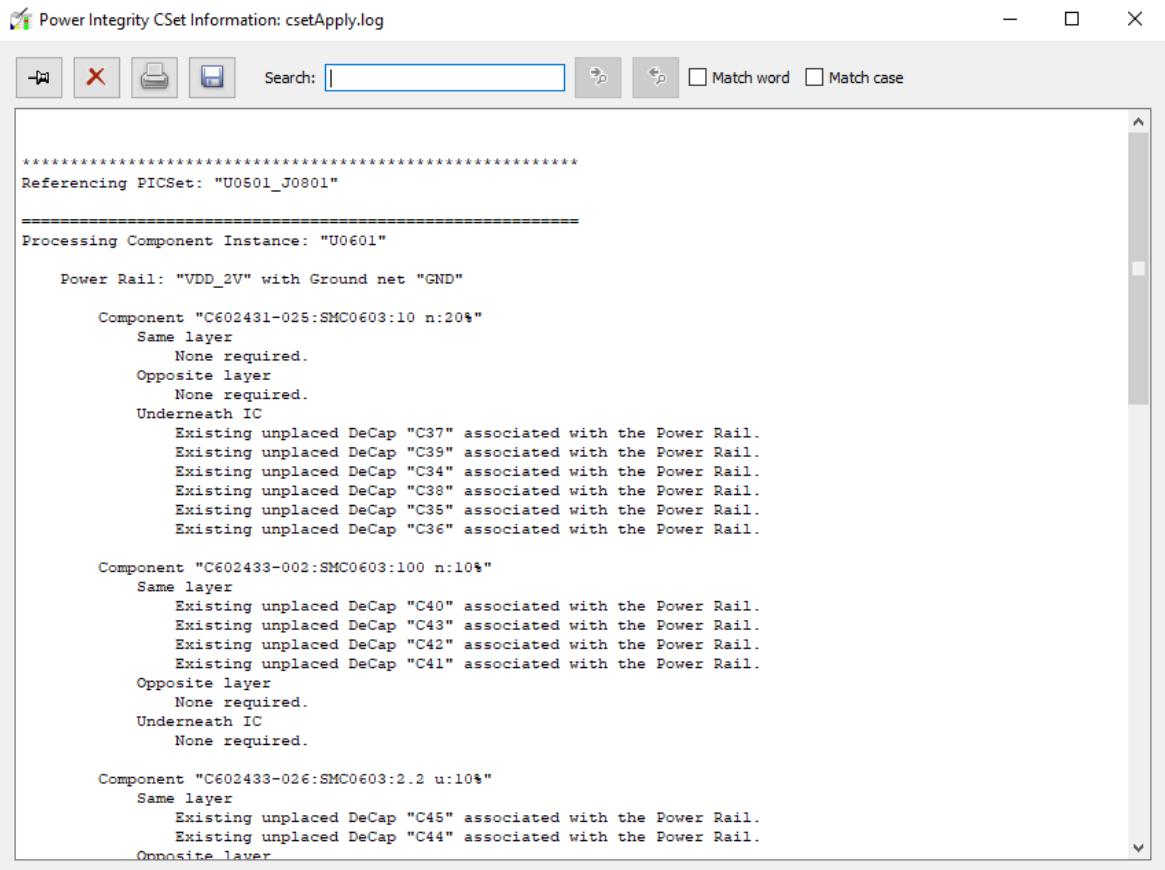
To reference the PICSet from another part instance, choose the PICSet from the drop-down list box in the *Referenced Power Integrity CSet* column for the part instance.



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Working with the Decap Flow

As soon as the PICSet is applied, the PICSet application information is displayed. This information lists the capacitors used in the design and those added to the design.



The screenshot shows a Windows application window titled "Power Integrity CSet Information: csetApply.log". The window has a standard title bar with minimize, maximize, and close buttons. Below the title bar is a toolbar with icons for file operations like Open, Save, Print, and Copy/Paste, followed by a search bar and two checkboxes for "Match word" and "Match case". The main content area is a text log window displaying the following text:

```
*****
Referencing PICSet: "U0501_J0801"
=====
Processing Component Instance: "U0601"
Power Rail: "VDD_2V" with Ground net "GND"
Component "C602431-025:SMC0603:10 n:20%"
    Same layer
        None required.
    Opposite layer
        None required.
    Underneath IC
        Existing unplaced DeCap "C37" associated with the Power Rail.
        Existing unplaced DeCap "C39" associated with the Power Rail.
        Existing unplaced DeCap "C34" associated with the Power Rail.
        Existing unplaced DeCap "C38" associated with the Power Rail.
        Existing unplaced DeCap "C35" associated with the Power Rail.
        Existing unplaced DeCap "C36" associated with the Power Rail.

Component "C602433-002:SMC0603:100 n:10%"
    Same layer
        Existing unplaced DeCap "C40" associated with the Power Rail.
        Existing unplaced DeCap "C43" associated with the Power Rail.
        Existing unplaced DeCap "C42" associated with the Power Rail.
        Existing unplaced DeCap "C41" associated with the Power Rail.
    Opposite layer
        None required.
    Underneath IC
        None required.

Component "C602433-026:SMC0603:2.2 u:10%"
    Same layer
        Existing unplaced DeCap "C45" associated with the Power Rail.
        Existing unplaced DeCap "C44" associated with the Power Rail.
    Opposite layer
```

Creating a PICSet in Constraint Manager

You can also create a PICSet with decap template information in Constraint Manager directly.

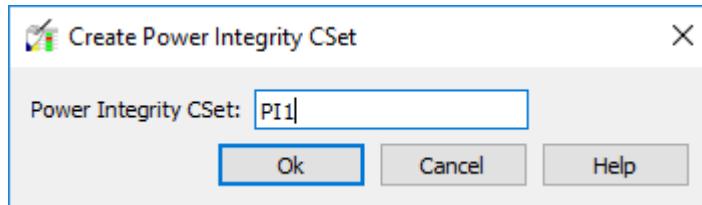
To create a PICSet in Constraint Manager, do the following:

1. Choose *Constraint Set – Power Integrity – Decap Template*, and right-click the design name.

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Working with the Decap Flow

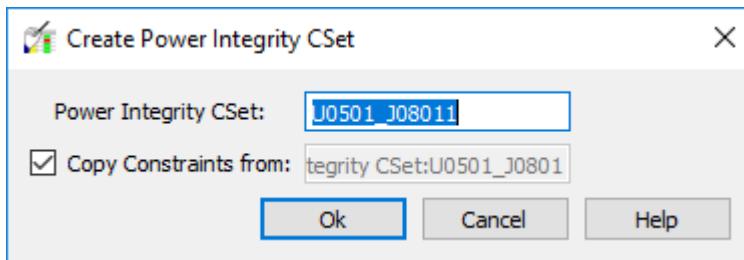
2. Choose *Create – Power Integrity CSet* from the context menu.



3. Specify a name for the PICSet and click *OK*.

You can also create a PICSet based on an existing PICSet:

1. Right-click an existing PICSet.
2. Choose *Create – Power Integrity CSet* from the context menu.



3. Specify a name for the PICSet, if you do not want to keep the default name.

Note: The *Copy Constraints From* check box is already selected and the name of the PICSet is also selected.

4. Click *OK*. A new PICSet is created and assigned values from the specified PICSet.

Adding Power Rails

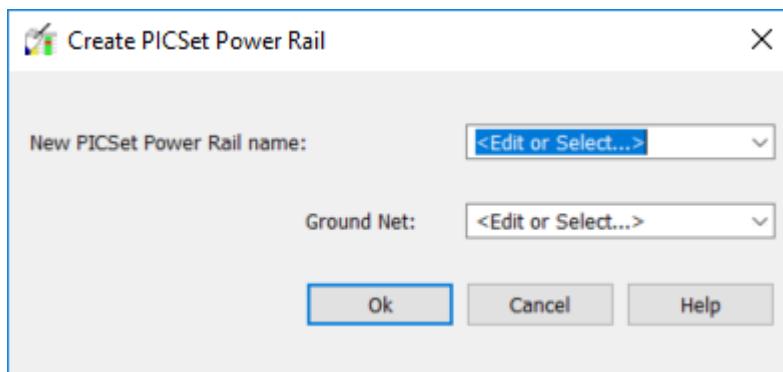
You can add Power Rails to a PICSet in Constraint Manager.

1. Right-click the desired PICSet.

Allegro Sigrity PI Flow Guide

Working with the Decap Flow

2. Choose *Create – Power Rail* from the context menu.

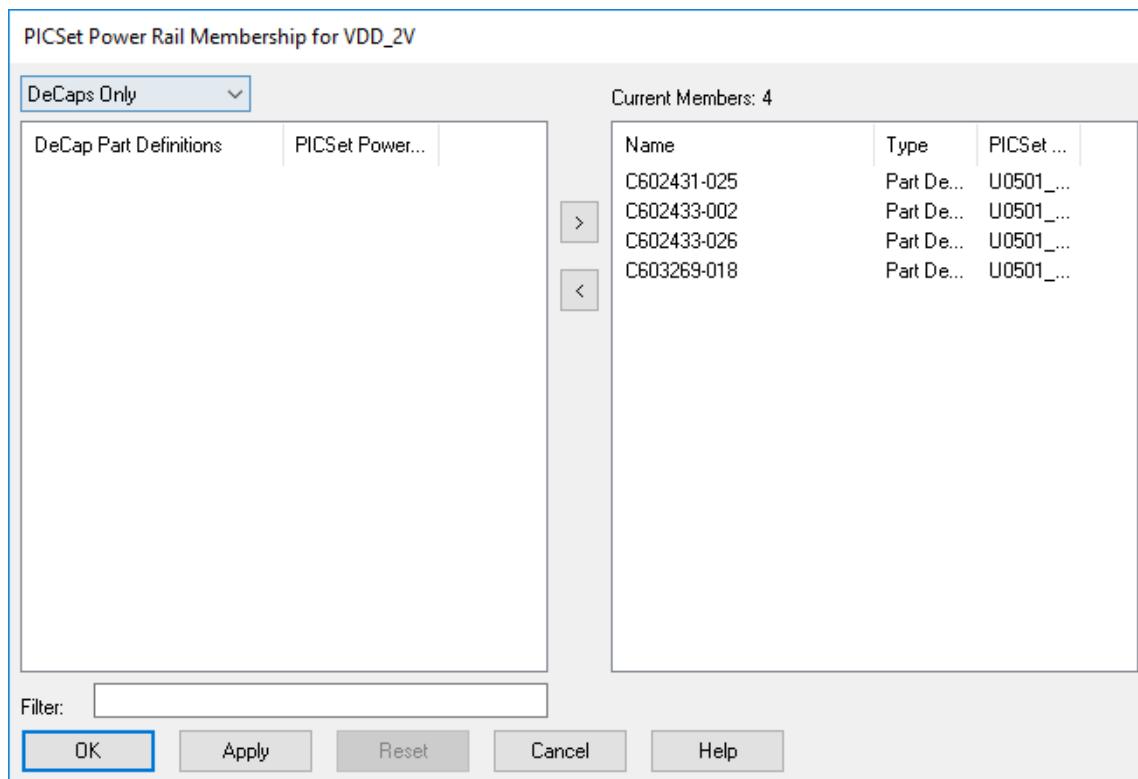


3. Specify a name for the power rail or select from a list of Voltage Nets.

When the PICSet is referenced, any Power Rails with net names which do not exist in the design result in an error.

You can also add Decaps to a Power Rail by performing the following steps:

1. Right-click the Power Rail (PIPR) and choose *PICSet Power Rail members* from the context menu.

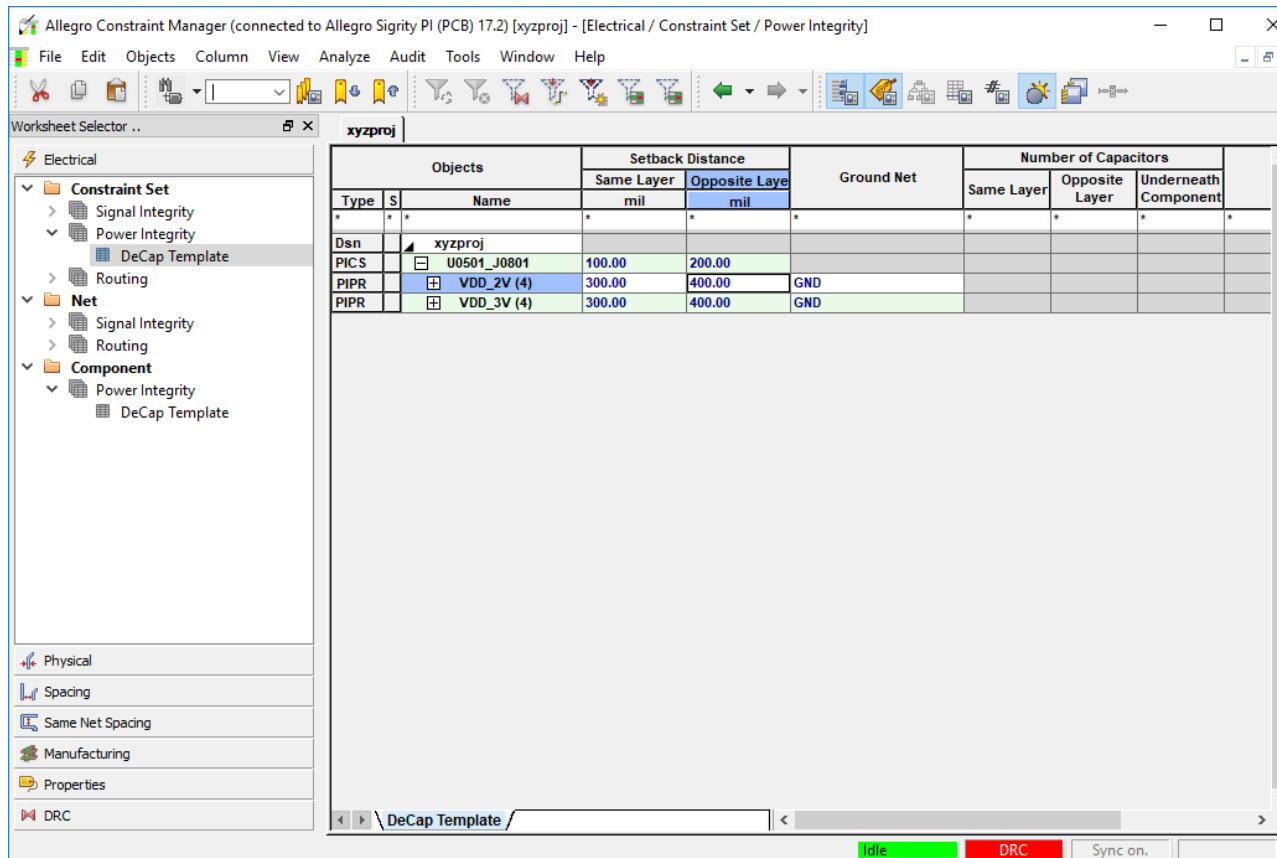


Allegro Sigrity PI Flow Guide

Working with the Decap Flow

Editing PICSets

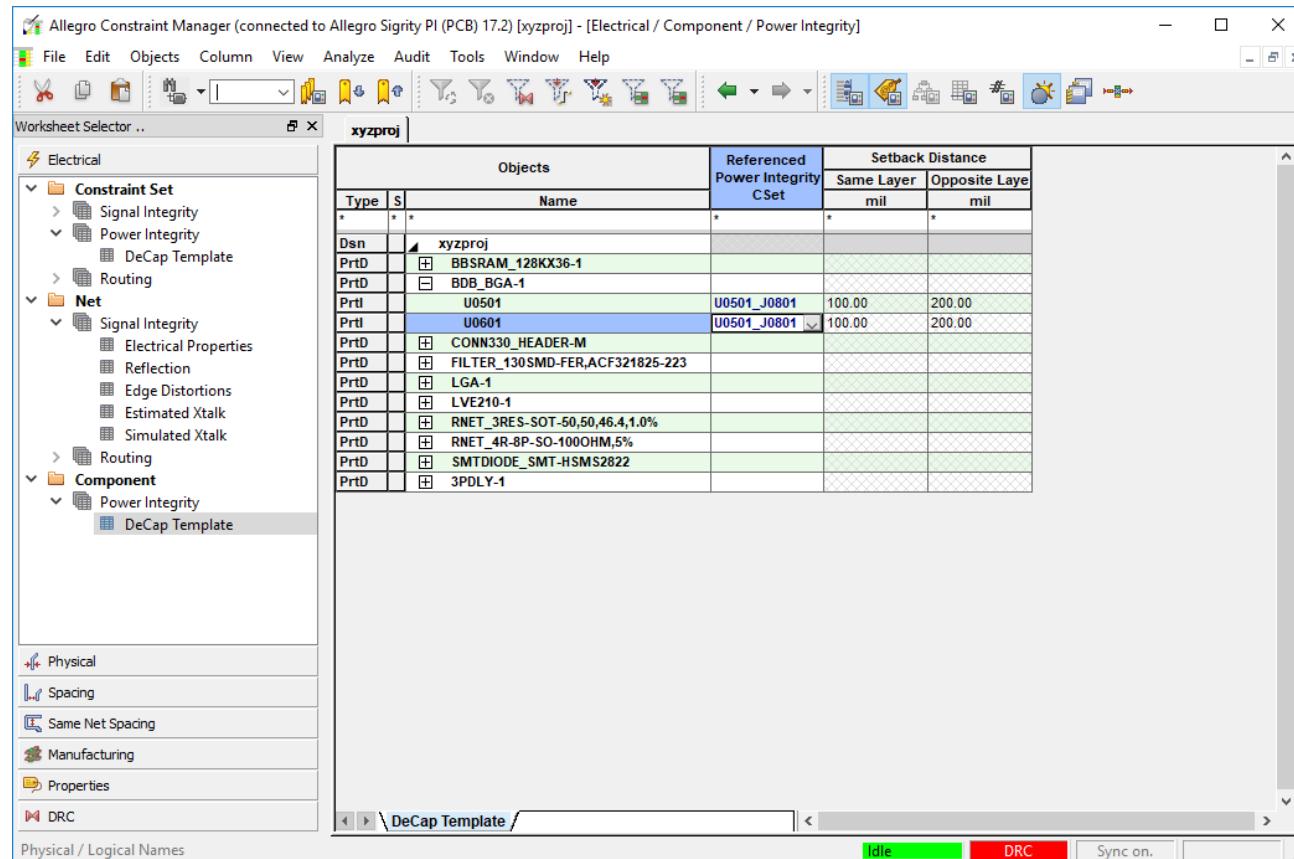
When the structure of the PICSet is complete, you can add or edit values for the various properties in the grid. Standard Constraint Manager rules of inheritance apply. You can use other standard Constraint Manager features, such as Rename, Delete, or Remove for various objects, as well.



Allegro Sigrity PI Flow Guide

Working with the Decap Flow

You can apply a PICSet to an IC component so that it contains the required Decap template information.



Note that the worksheet shows referenced PICSet and the associated setback distances for each IC component. You can apply PICSet references on Part Definition (PrtD) or Part Instance (Prtl) rows.

The following table explains the color-coding for each PICSet Reference:

Color Coding	Description
Blue	The reference is directly set and the PICSet information has been successfully applied.
Black	The reference is inherited from a parent object, such as a Part Definition or Part Class, and the PICSet information has been successfully applied.

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Working with the Decap Flow

Color Coding	Description
Yellow	<p>The reference is out-of-date, the PICSet has changed and the PICSet information needs to be re-applied to the IC.</p> <p>You need to run the <i>Audit – Power Integrity CSet</i> command to re-apply the PICSet and bring the IC information up-to-date.</p>
Red	<p>Indicates that an error occurred while applying the PICSet. You can hover the mouse over the error to view the error message on the status line.</p> <p>You can run the <i>Audit – Power Integrity CSet</i> command to generate a report containing all the errors for the reference.</p>

Auditing PICSet

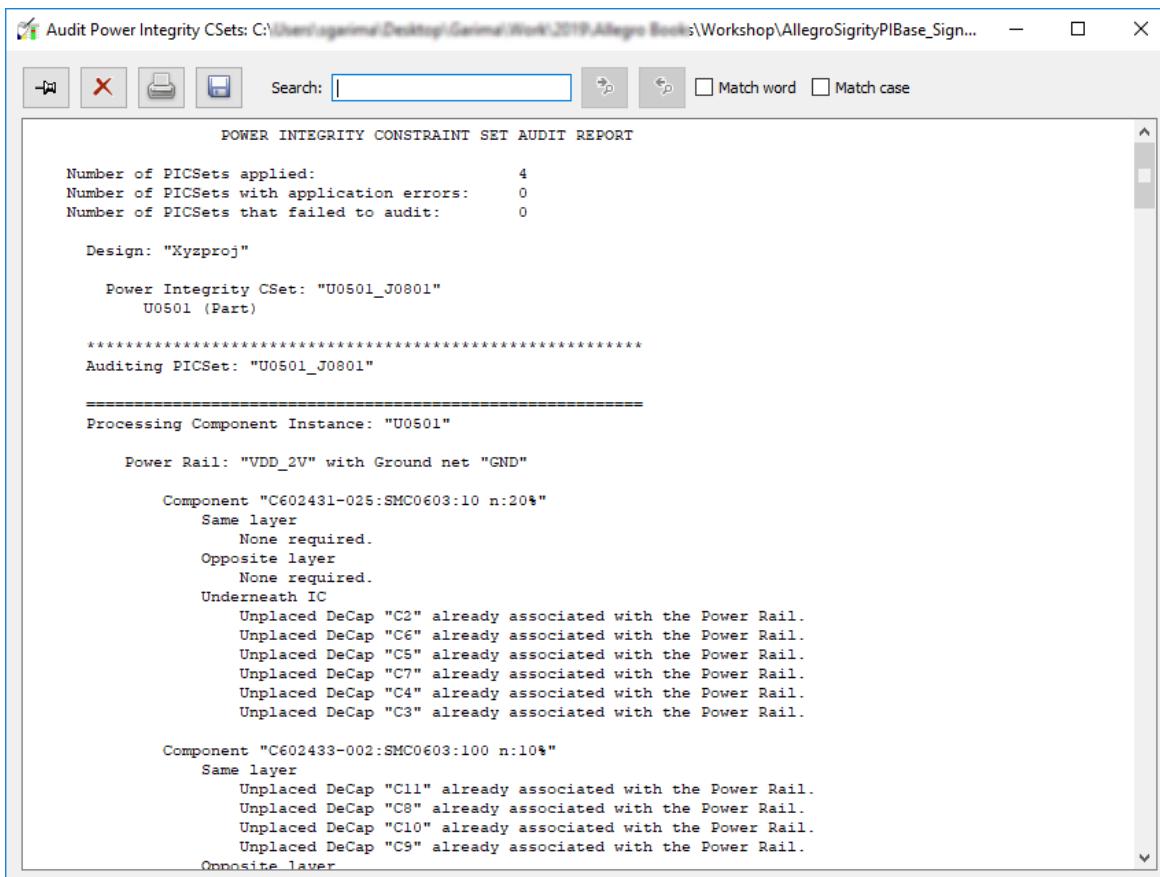
Constraint Manager supports a PICSet audit report which contains the IC specific decap information based upon a referenced PICSet.

1. Choose *Audit – Power Integrity CSets*.

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Working with the Decap Flow

2. Specify a name for the report and click **Save**. The generated report is displayed.



The screenshot shows a Windows application window titled "Audit Power Integrity CSets". The window contains a text-based audit report for a component instance "U0501_J0801". The report details the number of PICSets applied (4), the number of PICSets with application errors (0), and the number of PICSets that failed to audit (0). It also specifies the design as "Xyzproj" and the component as "U0501 (Part)". The report then provides a detailed breakdown of the audit process for the component instance, including power rail associations and decap placement status for various components like C602431-025 and C602433-002.

```
POWER INTEGRITY CONSTRAINT SET AUDIT REPORT

Number of PICSets applied: 4
Number of PICSets with application errors: 0
Number of PICSets that failed to audit: 0

Design: "Xyzproj"

Power Integrity CSet: "U0501_J0801"
U0501 (Part)

*****
Auditing PICSet: "U0501_J0801"

=====
Processing Component Instance: "U0501"

Power Rail: "VDD_2V" with Ground net "GND"

Component "C602431-025:SMC0603:10 n:20%"
    Same layer
        None required.
    Opposite layer
        None required.
    Underneath IC
        Unplaced DeCap "C2" already associated with the Power Rail.
        Unplaced DeCap "C6" already associated with the Power Rail.
        Unplaced DeCap "C5" already associated with the Power Rail.
        Unplaced DeCap "C7" already associated with the Power Rail.
        Unplaced DeCap "C4" already associated with the Power Rail.
        Unplaced DeCap "C3" already associated with the Power Rail.

Component "C602433-002:SMC0603:100 n:10%"
    Same layer
        Unplaced DeCap "C11" already associated with the Power Rail.
        Unplaced DeCap "C8" already associated with the Power Rail.
        Unplaced DeCap "C10" already associated with the Power Rail.
        Unplaced DeCap "C9" already associated with the Power Rail.

Onnsite layer
```

The report contains information on all the PICSets and their references in the current design.

The report also contains all error messages that occur while applying a PICSet. For example:

- ❑ Power Rail Net does not exist in the design. Power Rail will need to be renamed or Net will need to be created in the schematic and pushed forward.
- ❑ Decap instance could not be created. User must ensure Component Definition (library element) exists in the design to address this problem.

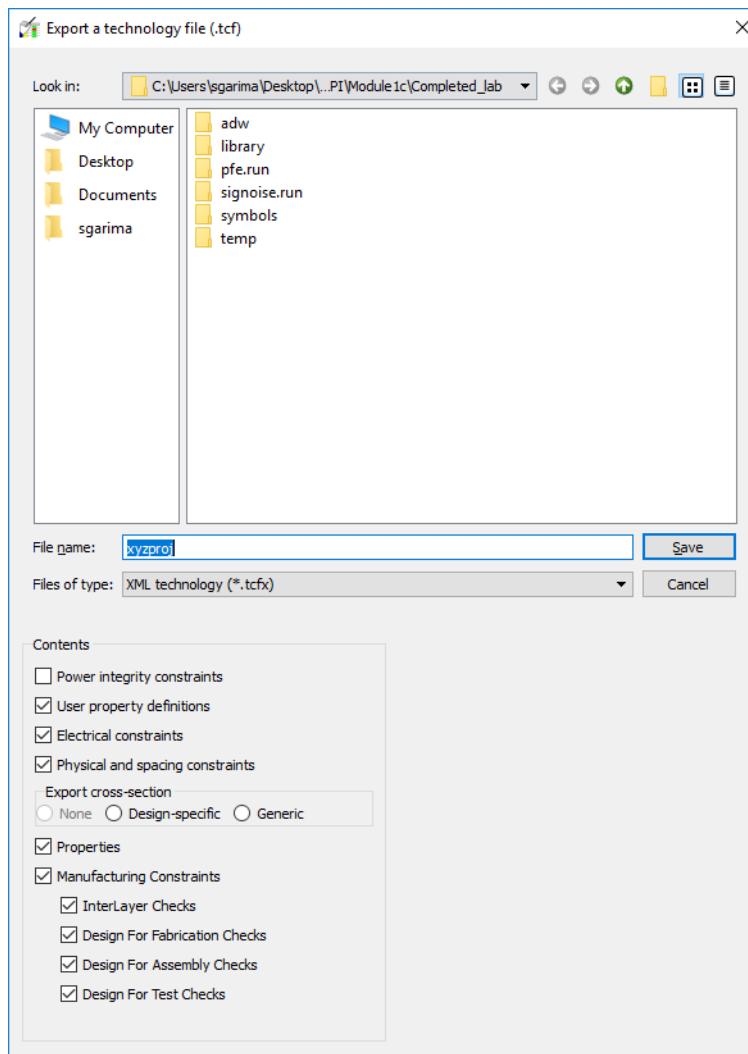
Reusing PICSets

You can preserve a PICSet and reuse it in any other design.

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Working with the Decap Flow

1. In Constraint Manager, choose *File – Export – Technology File*.



In the Export dialog, you specify the name of the technology file along with its contents.

2. For a file that contains only PICSet information, deselect all the options except *Power Integrity constraints*.
3. Specify the Export cross-section option as *None* and save the technology file.

When reusing a PICSet exported from an existing design,

1. Choose *File – Import – Technology File* to import the contents of the technology file into a different design.

The PICSets from the original design will be available in the new design.

Allegro Sigrity PI Flow Guide

Working with the Decap Flow



Caution

The PICSets imported from another design may result in errors in the new design when they are referenced.

Placing Decaps

After creating PICSets and Decap templates in Constraint Manager, you are ready to place them on the layout canvas.

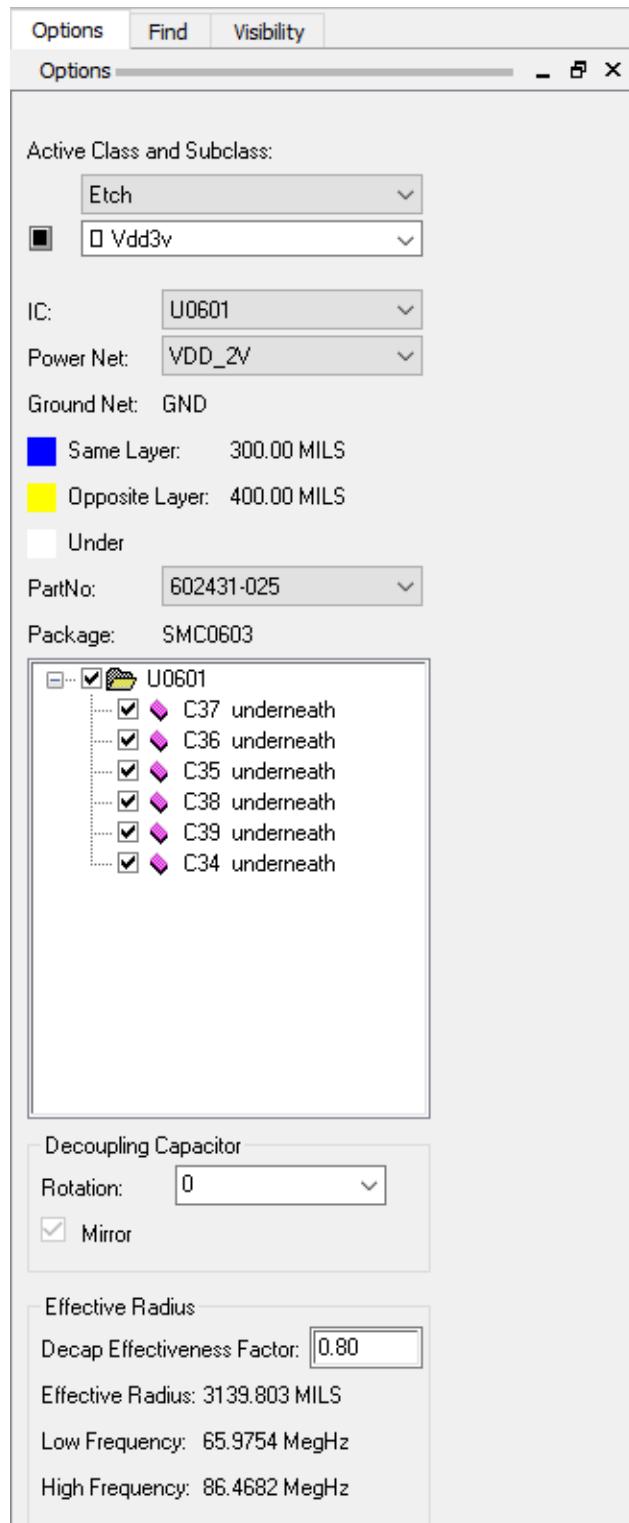
To place Decaps in a design, do the following:

1. In Allegro Sigrity PI, choose *Analyze – DeCap Place*.

Allegro Sigrity PI Flow Guide

Working with the Decap Flow

The Options window presents the Decap for each IC component.



Allegro Sigrity PI Flow Guide

Working with the Decap Flow

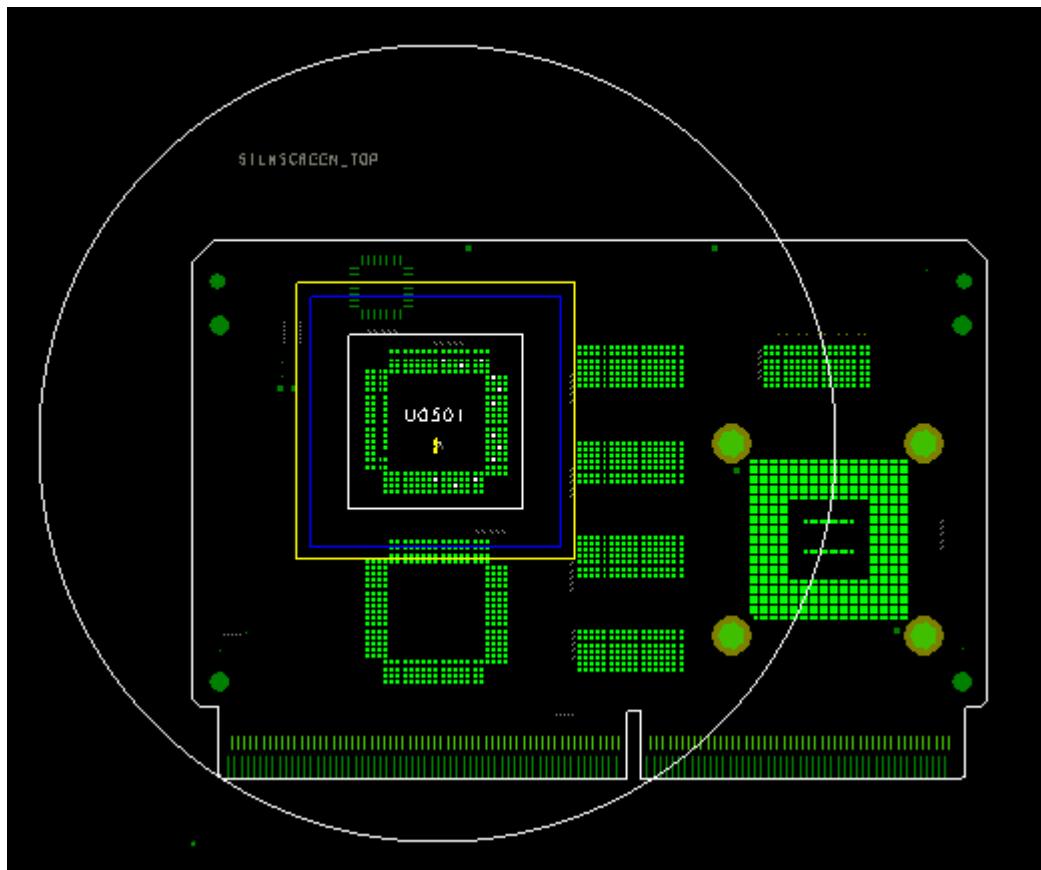
When an IC component is selected, the related decap template of the selected IC is displayed. The canvas is zoomed in, the selected IC is highlighted and the decap is attached to the mouse pointer.



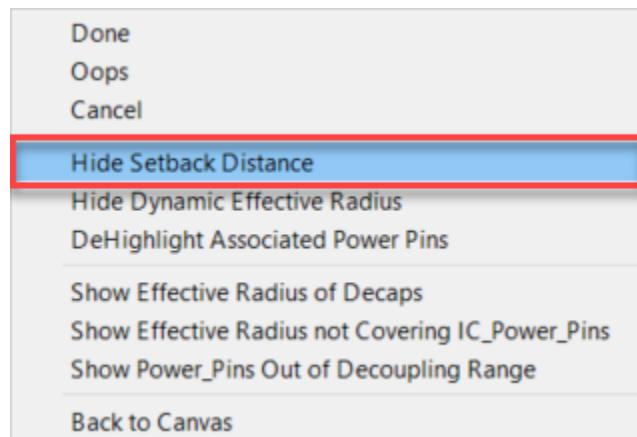
Allegro Sigrity PI Flow Guide

Working with the Decap Flow

As you place the decap, the setback distances for the IC component are displayed as blue and yellow rectangular boxes enclosing the IC component, as shown below:



This setback distances are picked from the PICSet referenced by the IC component in Constraint Manager. The setback distances are displayed by default. You can hide or display them by choosing *Hide/Show Setback Distance* from the context menu.

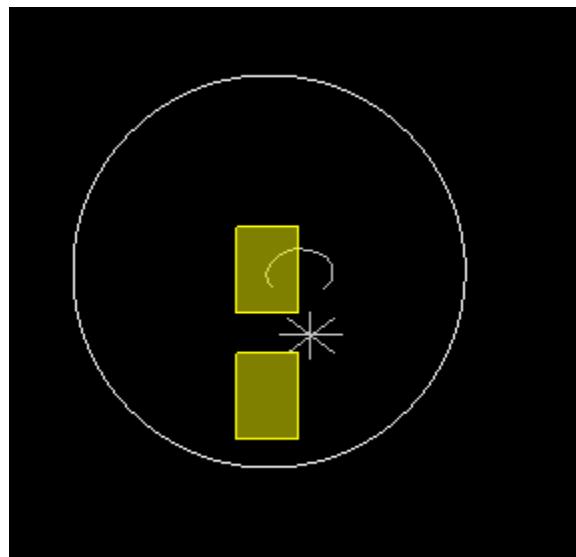


Allegro Sigrity PI Flow Guide

Working with the Decap Flow

2. Select the decap to place from the Options window.

Choose *Show Dynamic Effective Radius* from the context menu to see the effective radius of the decap before you place it.



The decap effective radius guides you where to place the decap by showing the maximum distance at which the decap is maximally effective. It is dynamically computed as the cursor moves due to local availability of metal shapes on the associated power and ground layers. You can see the dynamic radius circle as you move a decap around to place it.

If you cannot see the dynamic radius circle, it may be because it is too large or the cap cannot see the power plane below it. Use the *Hide Dynamic Effective*

3. Click to place the decap on the canvas.

Field	Description
<i>IC</i>	Select the target IC for which you want to place the decap.
<i>Power Net</i>	Lists the voltage rails information in the decap template.
<i>PartNo</i>	Lists the cap/ PartNo of the selected voltage rail.
<i>Package</i>	Name of the package.

Allegro Sigrity PI Flow Guide

Working with the Decap Flow

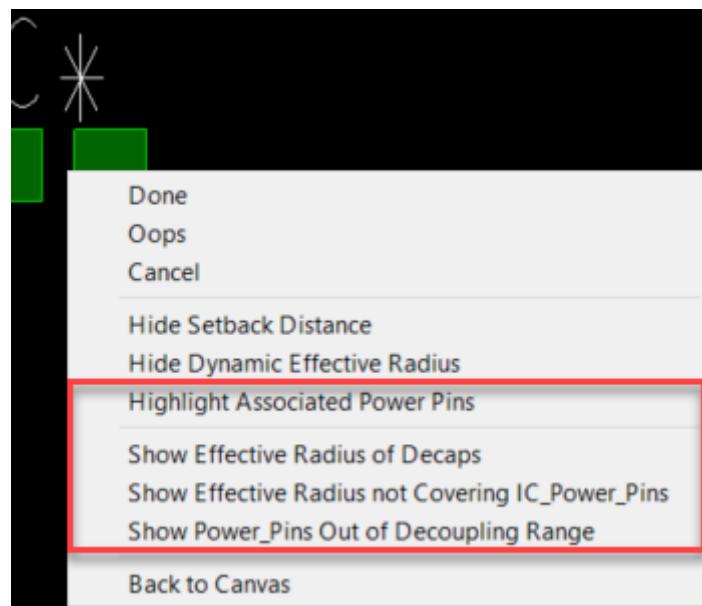
Field	Description
<i>Decap tree view</i>	Display the decaps of the selected PartNo. Each decap is marked <i>SameSide</i> , <i>OppSide</i> (for Opposite Side), or <i>underneath</i> as the case might be. You can select the decap you want to place from this list.
<i>Rotation</i>	Specify the angle of rotation for the decap.
<i>Mirror</i>	This option is read only. It is an indicator that the current decap will be placed on top or bottom layer.
<i>Effect radius</i>	Displays the effective radius of the selected cap/ PartNo.

4. When done, right-click and choose *Done* from the context menu.

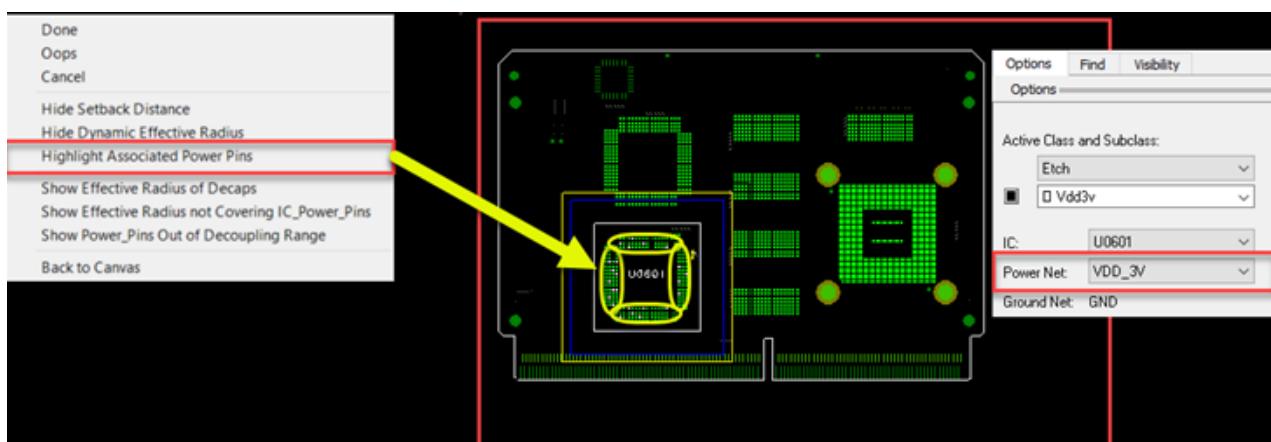
The selected decap is placed on the canvas.

Displaying Power Pins and Effective Radius Post Placement

You can display and change the placement of decaps and power pins according to the effective radius of the placed decaps. The following options are available in the context menu when you choose the *Analyze – Decap Place* command.



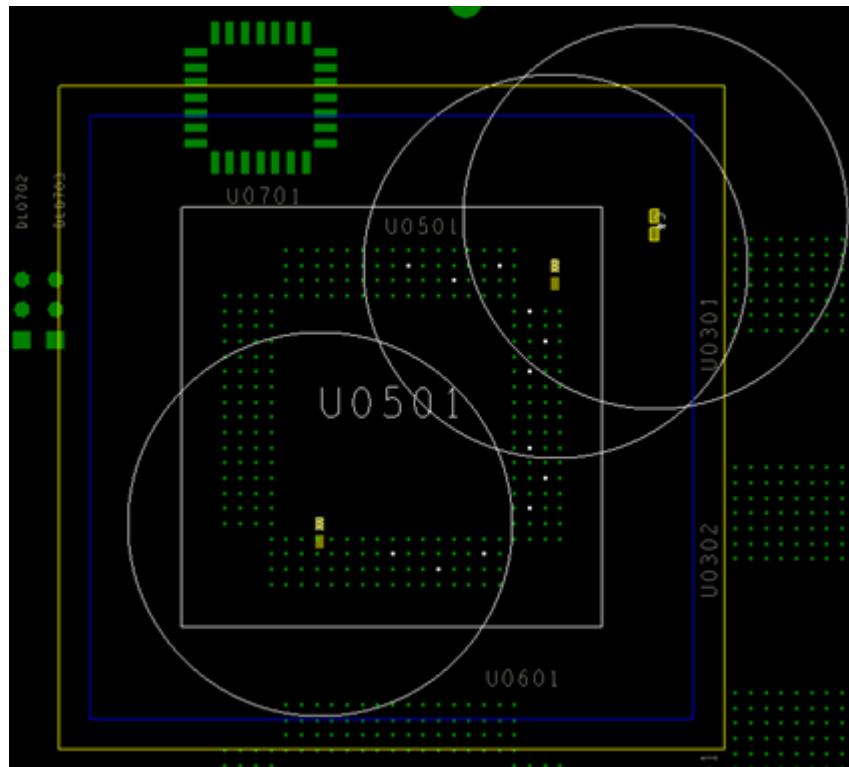
- *Highlight Associated Power Pins* — This command provides the ability to highlight all the power pins of the IC and the decap for the currently selected power net.



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Working with the Decap Flow

- *Show Effective Radius of Decaps* — This command displays the effective radius of the placed decaps.



With this command selected, as you move the mouse pointer with the decap attached to it, you can specify the decap effectiveness factor in the *Decap Effectiveness Factor* field in the Options window.

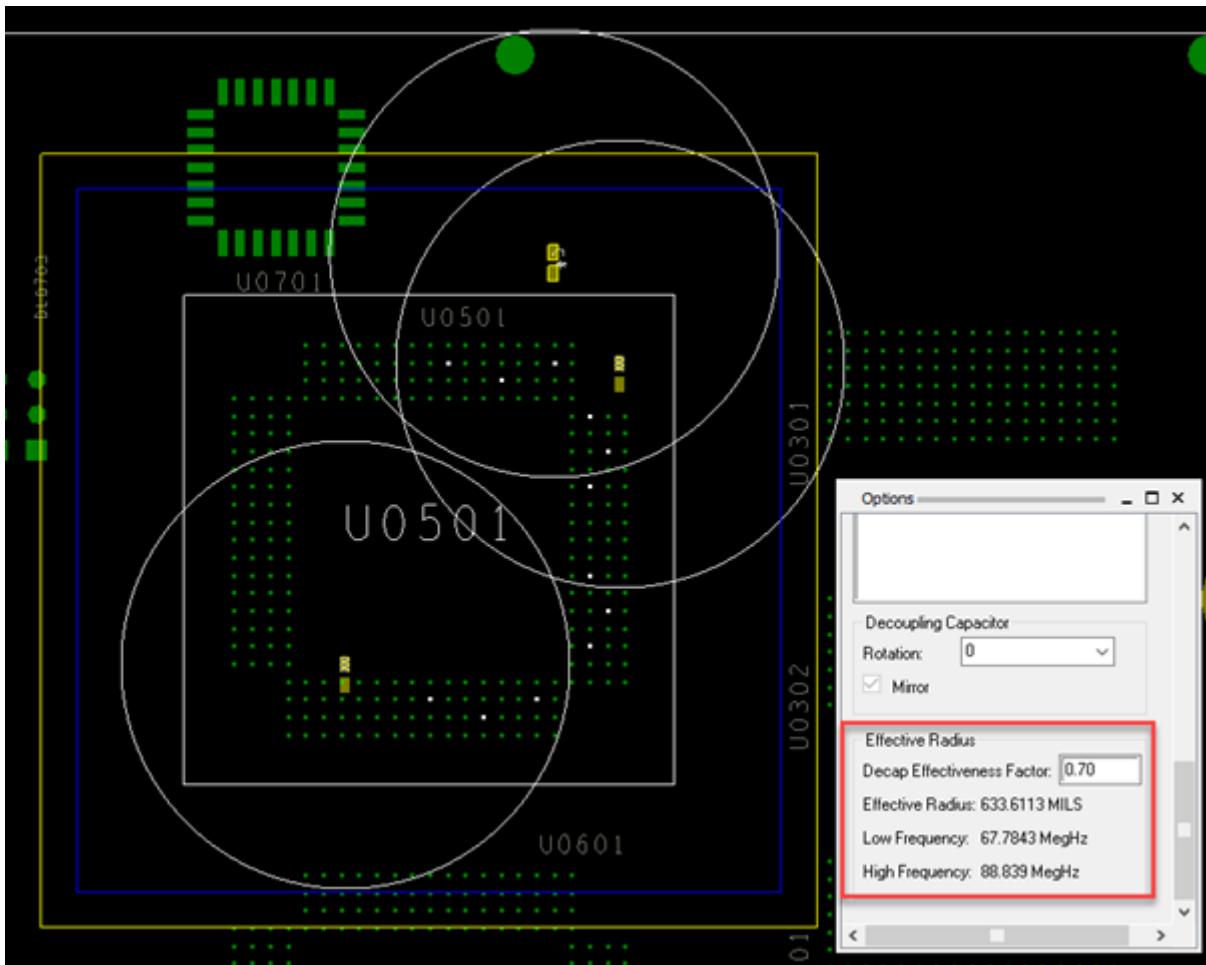
The following factors are also displayed in the Options window:

- Effective Radius*
- Low Frequency*
- High Frequency*

Allegro Sigrity PI Flow Guide

Working with the Decap Flow

The following figure shows these values when the *Decap Effectiveness Factor*:

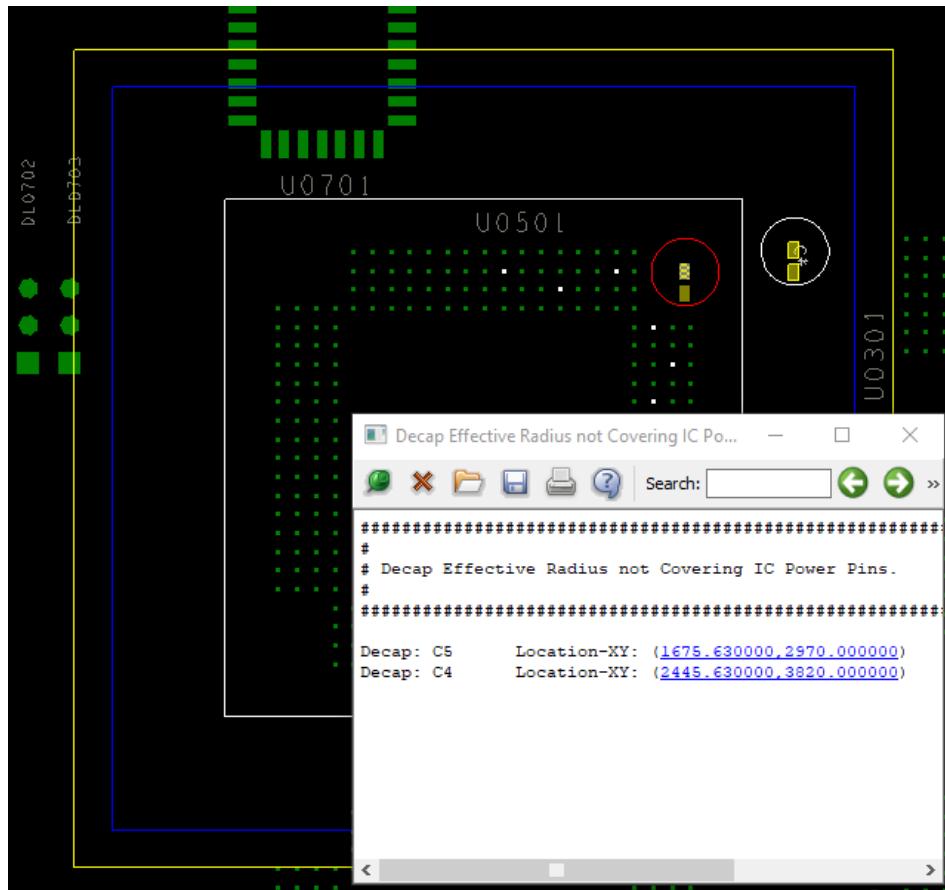


- **Show Effective Radius not Covering IC Power Pins** — This command displays the effective radius of a placed decaps, which cannot cover any related power pin of the IC. The highlighting circle is displayed in red. Meanwhile, a report recording the decap components and their locations is also displayed. From the links in the report, you can zoom to the specific components.

Allegro Sigrity PI Flow Guide

Working with the Decap Flow

Note: If the radius extends beyond the extents of the design, the decap is not displayed.

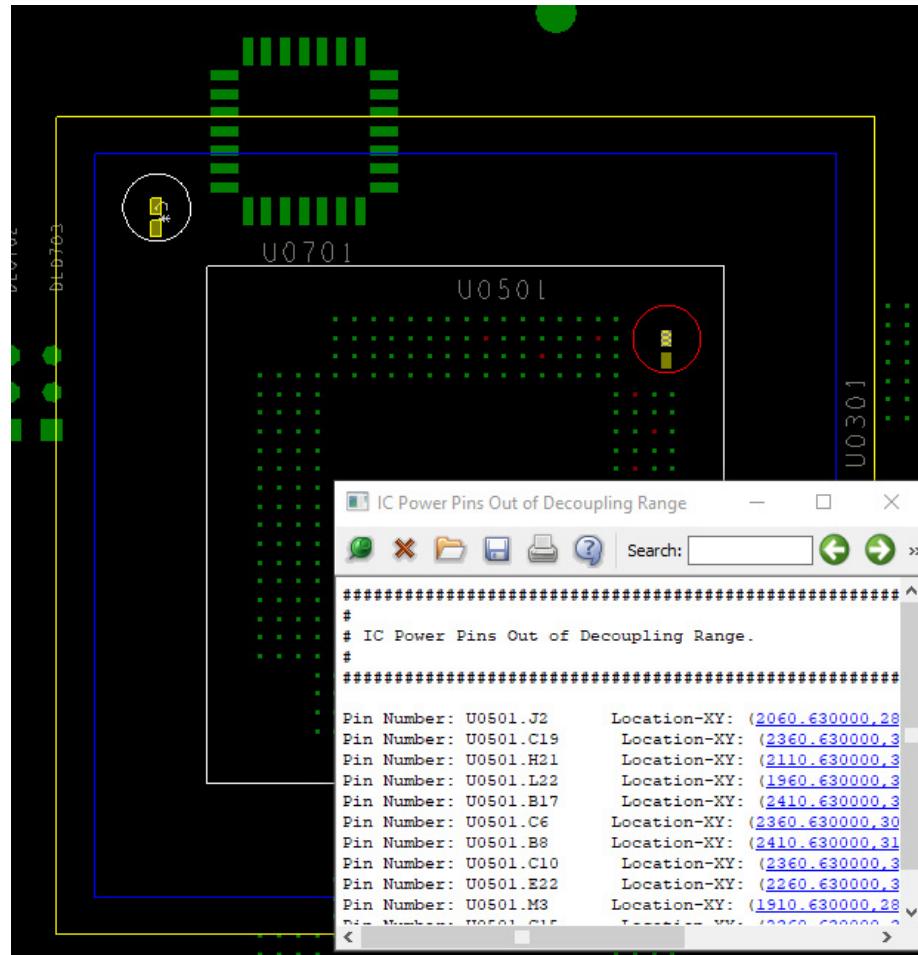


- *Show/Hide Power Pins Out of Decoupling Range* — Use this command to display the power pins which cannot be covered by the effective radius of the placed decaps from

Allegro Sigrity PI Flow Guide

Working with the Decap Flow

the same power net. The selected pins are displayed in red. A report is also displayed with links to the power pins and their locations on the canvas.



Replicating Decap Placement

A decap template can be applied to several instances of the same device, if there are at least two instances of the same device (IC) associated with the same PICSet, and all the decaps in the PICSet are placed for at least one instance. This instance is used as the template to replicate. An additional condition is that for at least one instance, none of the decaps should be placed.

For an IC, if decaps from a PICSet or Decap template are already placed, use the *Analyze – Decap Place* command to manually complete the placement.

To replicate the placement of a decap, do the following:

1. Choose *Analyze – Decap Placement Replication*.

The Decoupling Capacitors Placement Replication dialog is displayed.

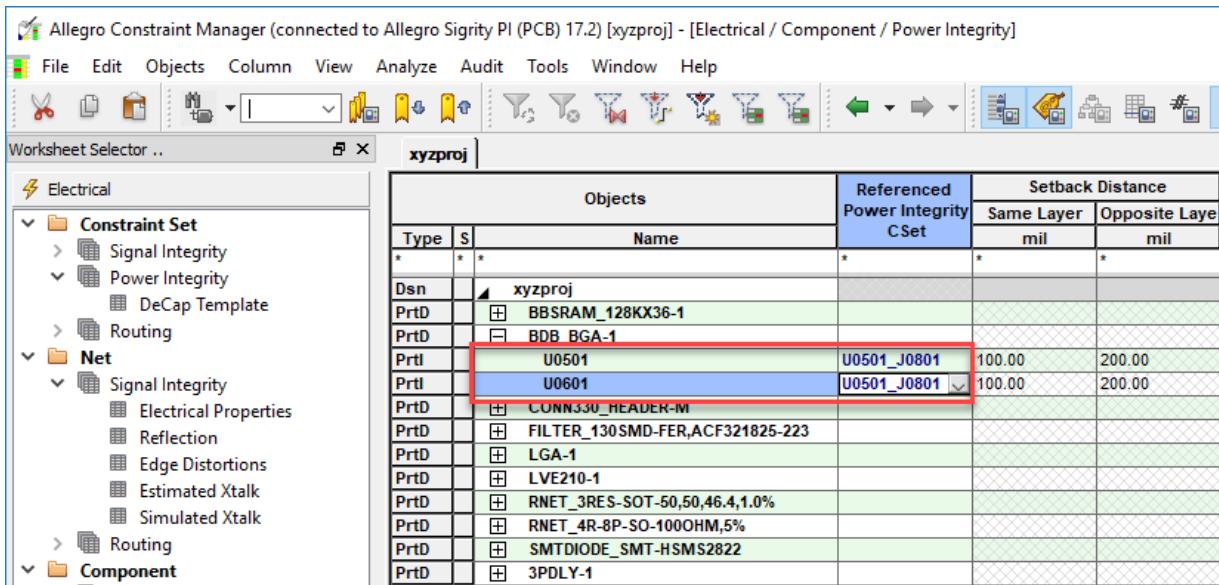
Table 2-5 Decoupling Capacitors Placement Replication

Field	Description
<i>PICSet</i>	Identifies the <i>PICSet</i> applied to the IC (RefDes) on which the placement template is to be replicated.
<i>RefDes</i>	Lists the ICs for which related decap placement template are found in the design, and none of the decaps from the PICSet are placed.
<i>Placement Template</i>	Lists available decap placement template of the RefDes. You can select one of templates to apply.
<i>Oops</i>	Rolls back the replication operation.
<i>Replicate</i>	Applies the placement template to the selected IC.

Allegro Sigrity PI Flow Guide

Working with the Decap Flow

You can assign a PICSet to several instances of the same device from Constraint Manager.



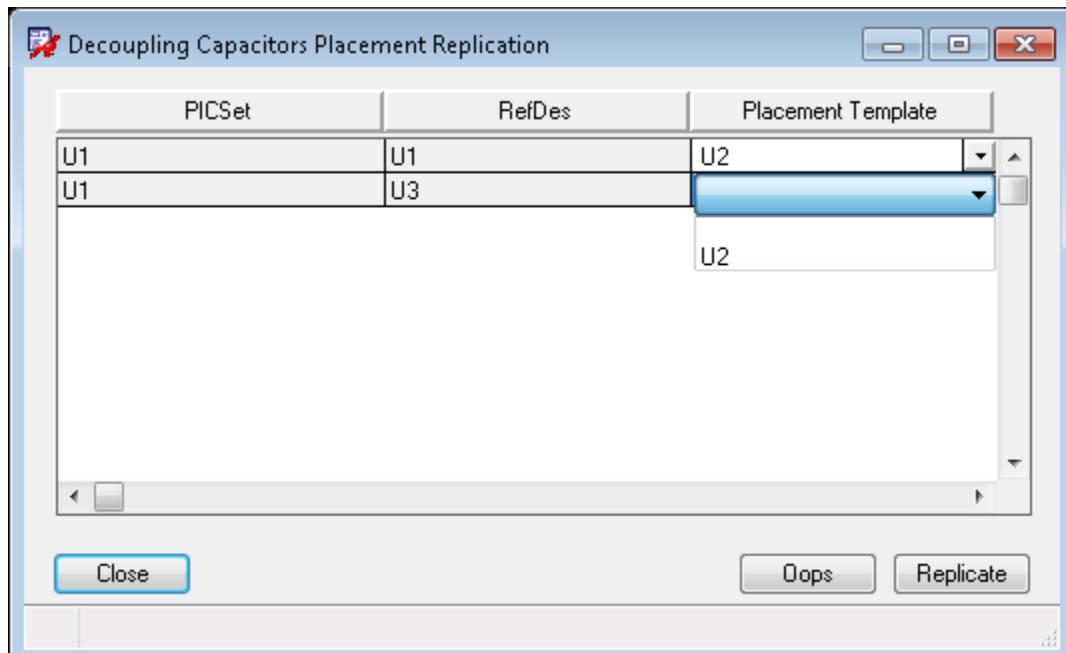
2. Select the placement template from the list *Placement Template* drop-down list.

The following figure illustrates an example where you select *U2* as a placement template for instance *U3*. Observe that the three instances, *U1*, *U2*, and *U3* have the same PICSet *U1*. For the placement template *U2*, all the decaps from PICSet *U1* have been

Allegro Sigrity PI Flow Guide

Working with the Decap Flow

fully placed. Therefore, U2 provides a placement template which can be applied to the instance U3.

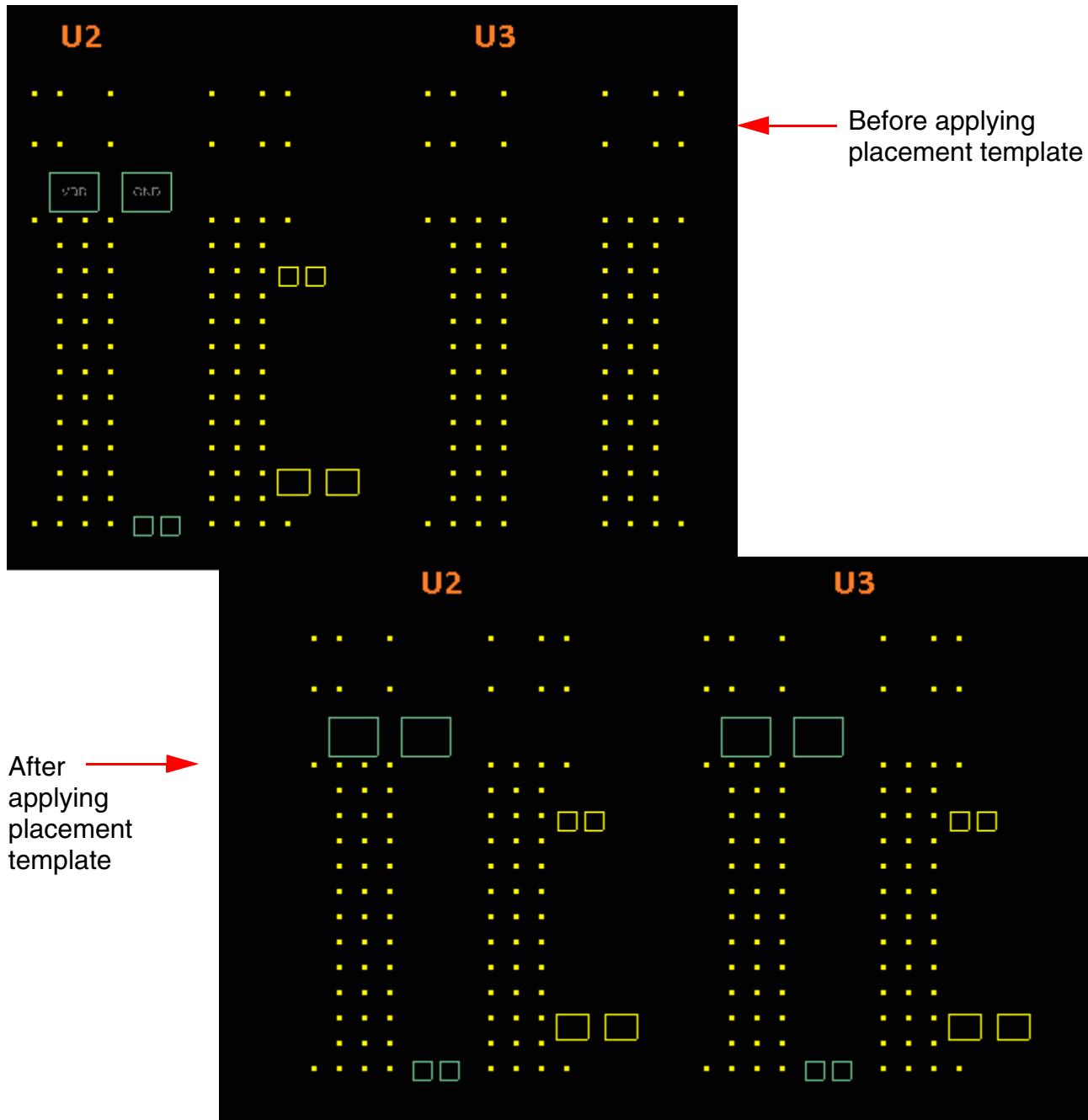


3. Click *Replicate*.

Allegro Sigrity PI Flow Guide

Working with the Decap Flow

The placement template *U2* is applied on the instance *U3*.



Allegro Sigrity PI Flow Guide

Working with the Decap Flow

Allegro Sigrity PI Tools

This chapter covers the following topics:

- [Allegro Sigrity PI Tools Available with Various Product Options](#)
- [PowerDC in Allegro Sigrity PI and Higher Versions](#)

Allegro Sigrity PI Tools Available with Various Product Options

In the Allegro Sigrity PI environment, you can open your board/package/SiP design and start working with the Allegro Sigrity Power Integrity and Package Analysis tools, which are available under the *Tools* and *Analyze* menus.

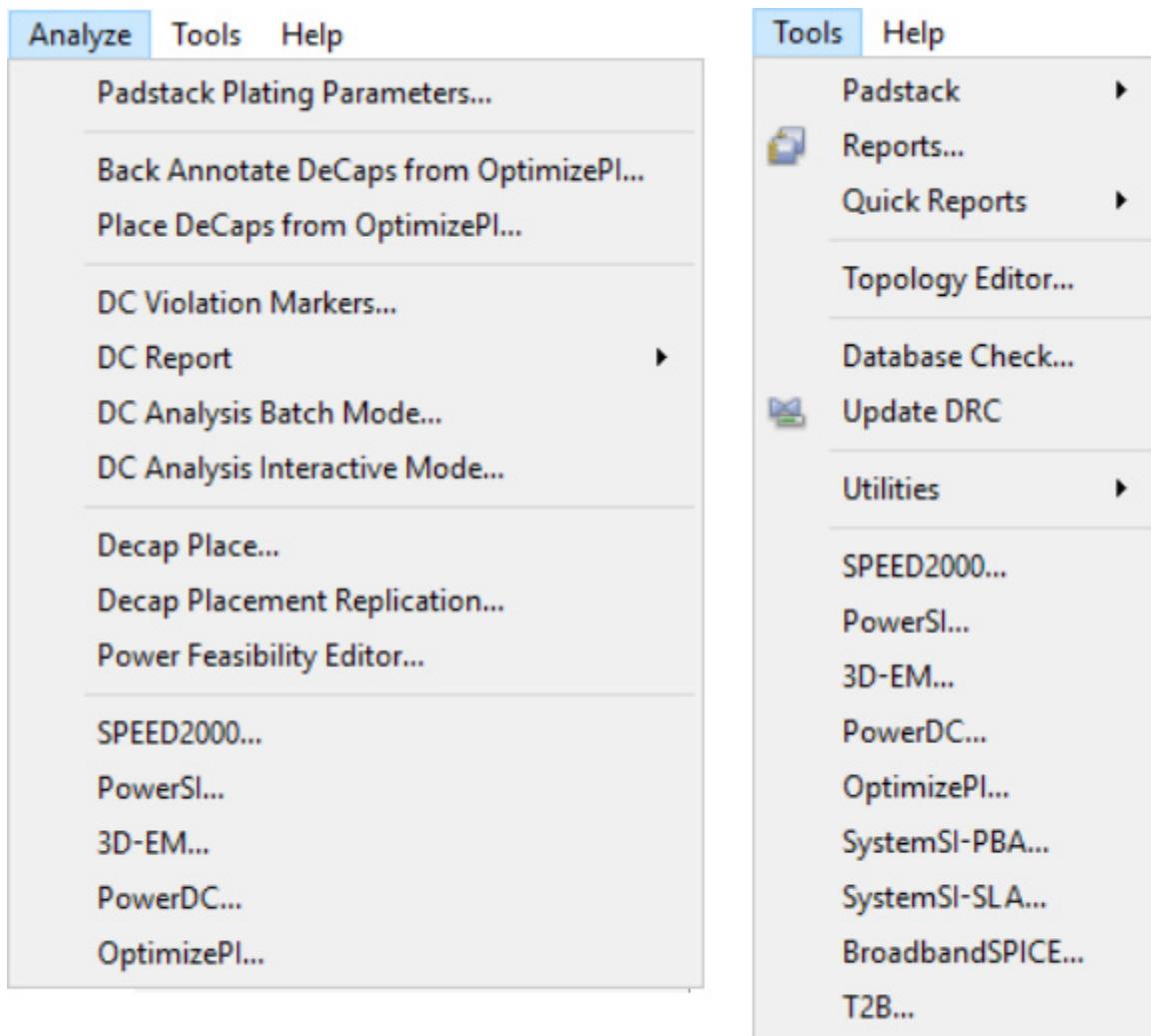
You can launch the following tools from Allegro Sigrity PI:

- SPEED2000
- PowerSI
- 3D-EM
- XtractIM - Only with Allegro Sigrity PI (ICP) and Allegro Sigrity PI (SIP)
- PowerDC
- OptimizePI
- SystemSI – PBA
- SystemSI – SLA
- Broadband SPICE
- T2B

Allegro Sigrity PI Flow Guide

Allegro Sigrity PI Tools

Figure 3-1 The Analyze and Tools Menus for Allegro Sigrity PI (Board)

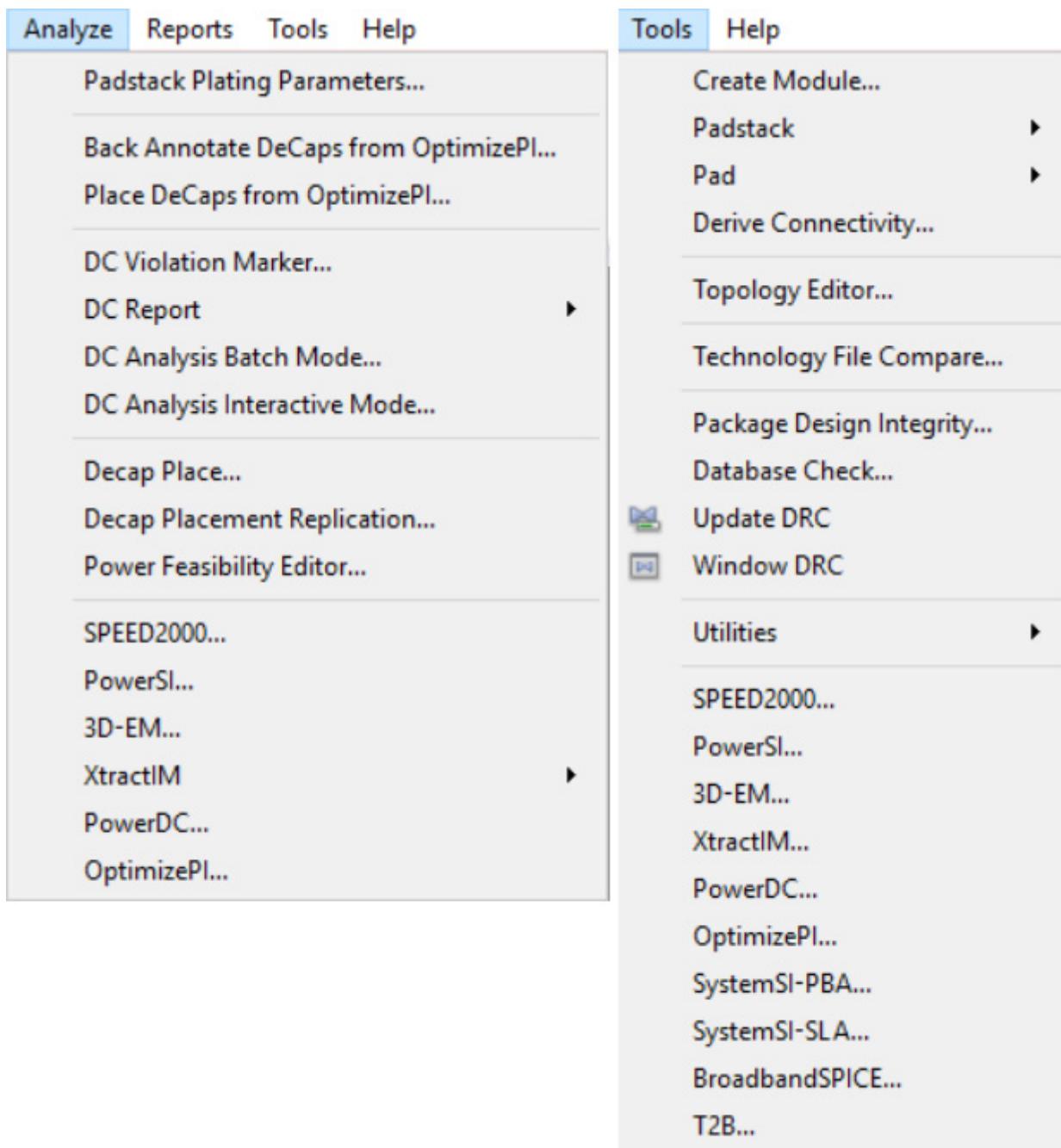


Allegro Sigrity PI (PCB)

Allegro Sigrity PI Flow Guide

Allegro Sigrity PI Tools

Figure 3-2 The Analyze and Tools Menus for Allegro Sigrity PI (ICP)

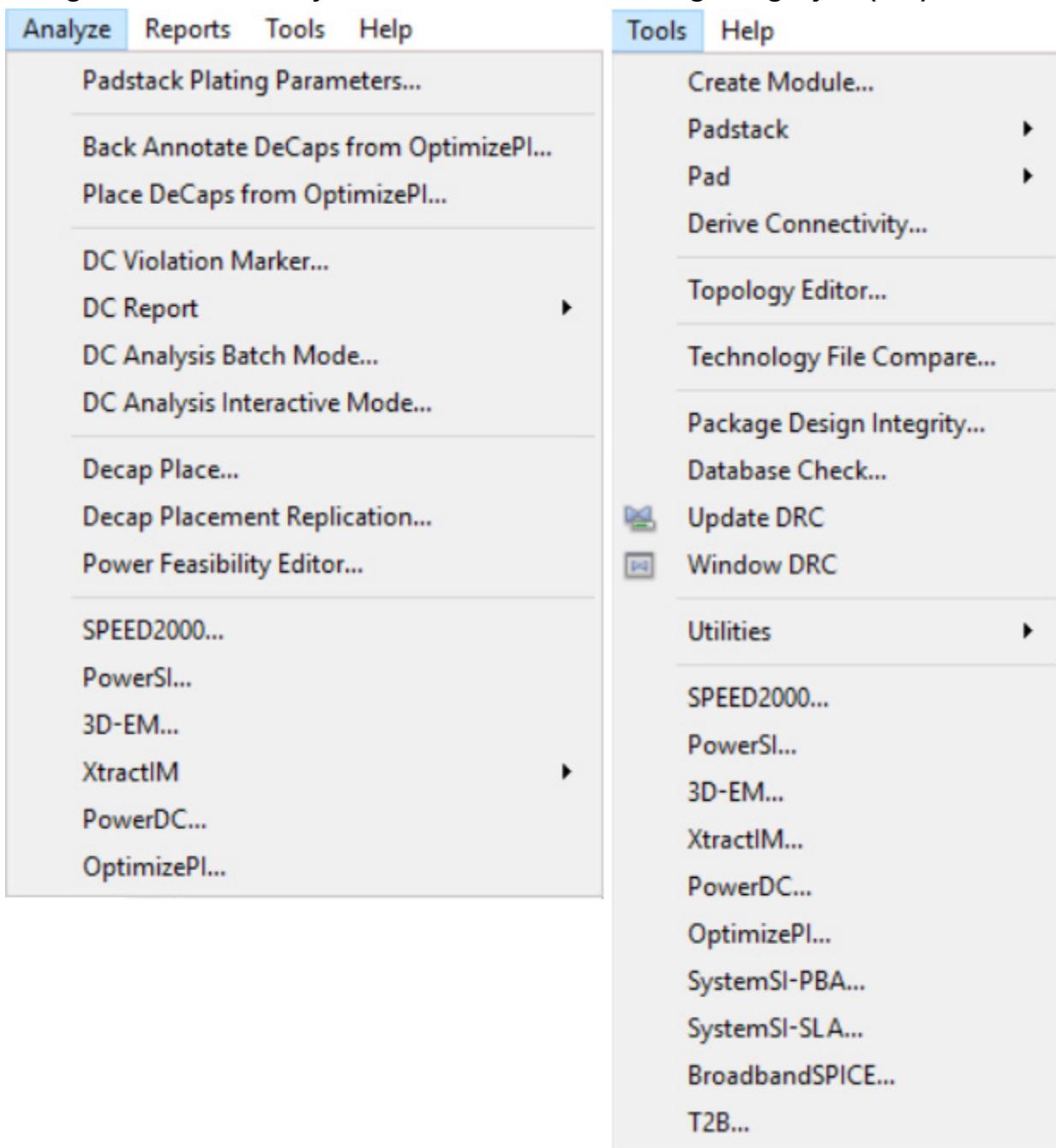


Allegro Sigrity PI (ICP) - apd

Allegro Sigrity PI Flow Guide

Allegro Sigrity PI Tools

Figure 3-3 The Analyze and Tools Menus for Allegro Sigrity PI (SIP)



Allegro Sigrity PI (SIP) - cdnsip

PowerDC in Allegro Sigrity PI and Higher Versions

The following table lists the various features of PowerDC available from the Allegro Sigrity PI product (PA5800) viz-a-viz PowerDC with higher versions:

Table 3-1

Workflow/Features	Available in PowerDC from Allegro Sigrity PI (PA5800)?	Available in PowerDC from Allegro Sigrity PI + PI Signoff & Optimization (PA5800 + SIGR925)?
■ Single-Board/Package IR Drop Analysis workflow	Yes	Yes
■ Single-Board/Package E/T Co-Simulation	No	Yes
■ Multi-Board/Package IR Drop Analysis		
■ Multi-Board/Package E/T Co-Simulation		
■ Pin Location Effectiveness		
■ Package Thermal Characterization		
■ Resistance Measurement Generation		
■ Resistance Network Model Generation		
Panes:	No	Yes
■ TCL Reader		
■ TCL Command		
Workspace Commands:		

Allegro Sigrity PI Flow Guide

Allegro Sigrity PI Tools

Workflow/Features	Available in PowerDC from Allegro Sigrity PI (PA5800)?	Available in PowerDC from Allegro Sigrity PI + PI Signoff & Optimization (PA5800 + SIGR925)?
■ Start Simulation	Yes	Yes
■ Stop Simulation		
■ Report		
■ Simulation Results		
■ Export to Image File		
■ Reuse Ports	No	Yes
■ Layout File		
■ Merge		
Distribution Commands		
■ Voltage Distribution Plot	Yes	Yes
■ Plane Current Density Plot		
■ Via Current Plot		
■ Switch to Normal Layer View		
■ Plane Power Density Plot	No	Yes
■ Power Loss Plot		
■ Pin Voltage/IRdrop Plot		
■ Pin Resistance Plot		
■ Export to Text Files		

Edit Commands

Allegro Sigrity PI Flow Guide

Allegro Sigrity PI Tools

Workflow/Features	Available in PowerDC from Allegro Sigrity PI (PA5800)?	Available in PowerDC from Allegro Sigrity PI + PI Signoff & Optimization (PA5800 + SIGR925)?
■ Stack Up	Yes	Yes
■ Pad Stack Library		
■ Load Material File	No	Yes
■ WireBond Model Library		
■ Load Model Editor		
■ Transform Stack Up		
■ Transform Stack Up By Nodes		
■ Inner Lead Converter		
■ Node		
■ Trace		
■ WireBond		
■ Via Shape		
■ Thermal Test Board		
■ Balls/Bumps		
■ Rotate		
■ Move		
■ Delete		
■ Copy		
■ Cut		

Setup Commands

Allegro Sigrity PI Flow Guide

Allegro Sigrity PI Tools

Workflow/Features	Available in PowerDC from Allegro Sigrity PI (PA5800)?	Available in PowerDC from Allegro Sigrity PI + PI Signoff & Optimization (PA5800 + SIGR925)?
■ Macro	Yes	Yes
■ Component Manager		
■ Net Manager		
■ Cutting Boundary	No	Yes
■ Sweeping Manager		
 Tools Commands		
■ Check	Yes	Yes
■ Power line width calculator		
■ Background	No	Yes
■ MCP Editor...		
■ S Model Checking...		
■ Effective Thermal Conductivity Calculation		

For detailed information on these commands and functions of the PowerDC tool, see the *PowerDC User's Guide*.

Note: For detailed information on each of the tools, refer to the documentation of the respective tool.

Allegro Sigrity PI Flow Guide

Allegro Sigrity PI Tools

Working with DC Analysis Options

This chapter covers the following topics:

- [Overview](#)
- [Running DC Analysis](#)
 - [DC Analysis in Interactive Mode](#)
 - [Simulation Time vs Result Accuracy](#)
 - [Cross-Probing between Allegro Layout and PowerDC](#)
 - [Via Plating Editing in DC Analysis](#)
 - [Passing Component Height and Outline Information](#)
 - [DC Analysis Setup Automation with PowerTree and AMM](#)
 - [DC Analysis in Batch Mode](#)
 - [Running DC Analysis in PowerDC](#)
- [Adding DC Analysis Violation Markers](#)
 - [Manually Adding PowerDC Violation Markers in Allegro Canvas](#)
 - [Automatically Adding PowerDC Violation Markers in Allegro Canvas](#)
- [Viewing DC Analysis Reports](#)
 - [Violation Report](#)
 - [Full Report](#)

Overview

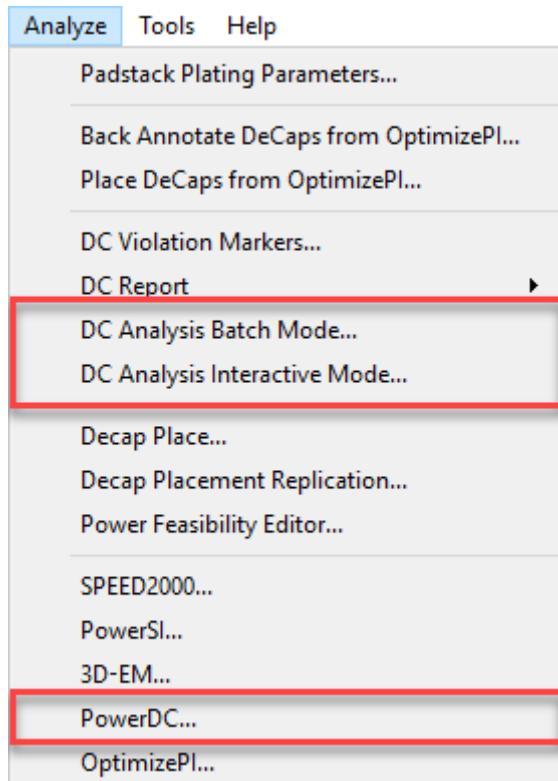
You can perform fast and accurate DC analysis for PCBs and IC packages along with thermal analysis that also supports electrical and thermal co-simulation using the PowerDC tool. Targeting both pre and post-layout applications, the PowerDC approach enables you to quickly identify IR drop, current density, and thermal issues that are among the leading field failure risks.

Running DC Analysis

There are three ways of running the DC analysis solution in Allegro Sigrity PI:

- Interactive mode
- Batch mode
- In PowerDC

These modes are available from the following *Analyze* menu commands in Allegro Sigrity PI:



Allegro Sigrity PI Flow Guide

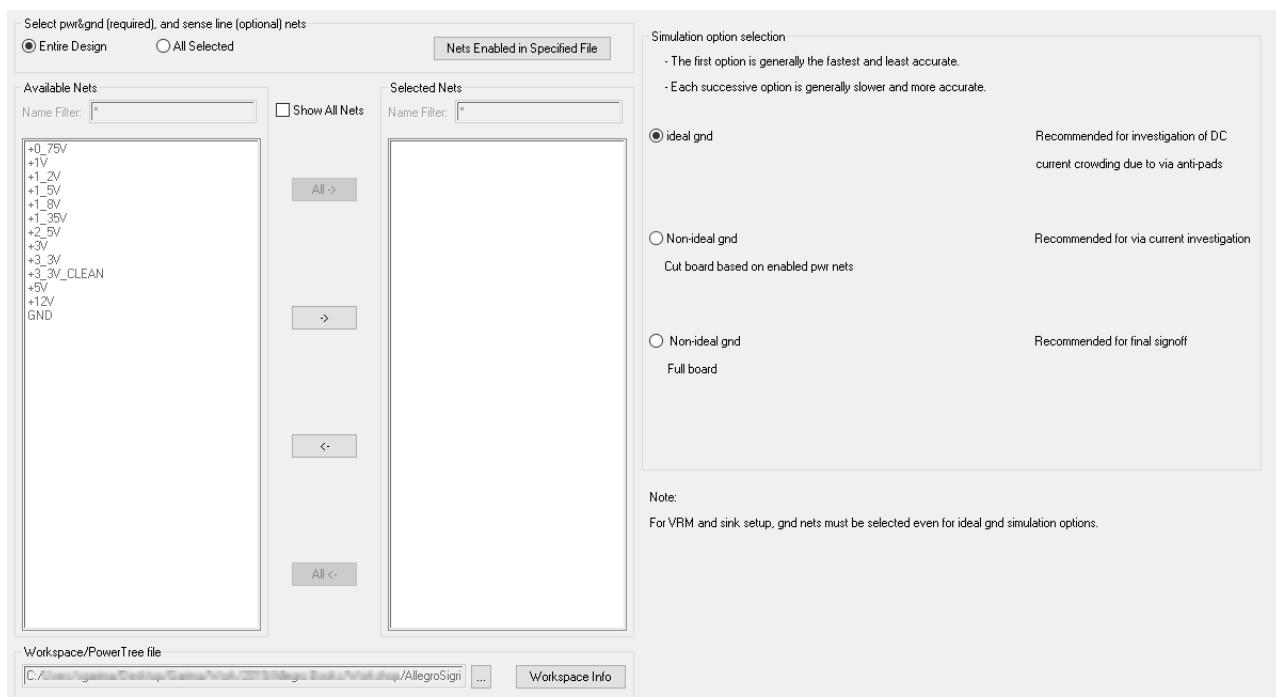
Working with DC Analysis Options

DC Analysis in Interactive Mode

In the interactive mode, DC analysis is performed in the PowerDC environment. When PowerDC launches from the *Analyze – DC Analysis* command, the Allegro layout window closes and the PowerDC window appears where you set up the design and run analysis.

To run DC analysis in the interactive mode, perform the following steps:

1. Choose *Analyze – DC Analysis Interactive Mode*.



In the XNet Selection dialog, select the required nets or XNets from the list.

Alternatively, you can also choose to select only those nets which are enabled in the workspace. Using an existing workspace file lets you reuse an existing setup and re-simulate it after you make changes to the layout.

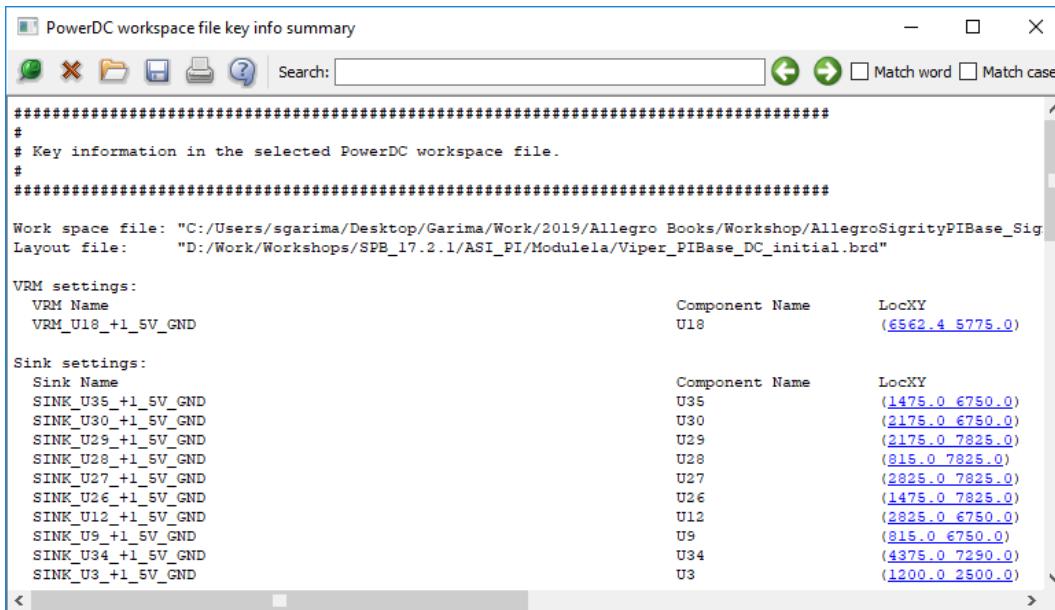
To do so, perform the following steps:

- Browse to the workspace file in the *Workspace/PowerTree file* field.

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

A summary of the workspace file is displayed.



The screenshot shows a Windows application window titled "PowerDC workspace file key info summary". The window contains a search bar and several buttons. The main area displays configuration information for a workspace file. It includes sections for "VRM settings" and "Sink settings", each listing components with their names and coordinates. The "VRM settings" section shows a VRM named "VRM_U18_+1_5V_GND" located at (6562.4, 5775.0). The "Sink settings" section lists multiple sinks, each with a name like "SINK_U35_+1_5V_GND" and a corresponding coordinate pair in parentheses.

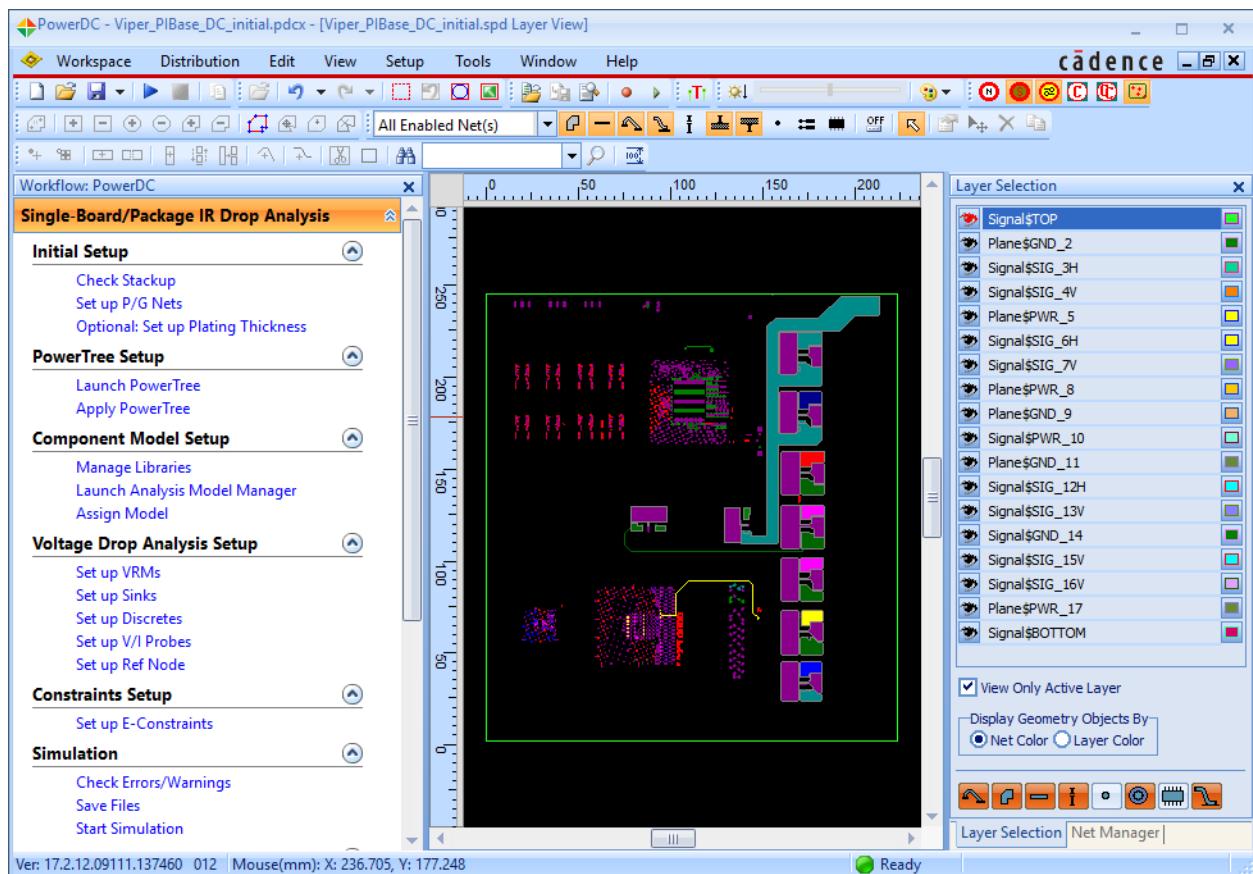
Component Name	LocXY
U18	(6562.4 5775.0)
U35	(1475.0 6750.0)
U30	(2175.0 6750.0)
U29	(2175.0 7825.0)
U28	(315.0 7825.0)
U27	(2825.0 7825.0)
U26	(1475.0 7825.0)
U12	(2825.0 6750.0)
U9	(815.0 6750.0)
U34	(4375.0 7250.0)
U3	(1200.0 2500.0)

Click the *Nets Enabled in Workspace Only* button.

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

2. Click OK.



Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

PowerDC application opens and the analysis report is displayed after the analysis completes.

The screenshot shows a software interface titled "POWERDC SIMULATION REPORT". At the top left, there is a date and time stamp: "Date: 14:53 March 13, 2019". Below it is a "Pass/Fail:" status indicator. The main content area is a hierarchical navigation menu:

- [**1 General Information**](#)
 - [**1.1 Spd File Name and Location**](#)
 - [**1.2 Board Stackup**](#)
 - [**1.3 Layout Top and Bottom Layer Views**](#)
- [**2 Simulation Setup**](#)
 - [**2.1 Electrical Setup**](#)
- [**3 Results**](#)
 - [**3.1 Electrical Result Table**](#)
 - [**3.2 DC Analysis Block Diagram Result**](#)

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

Simulation Time vs Result Accuracy

The three simulation options provide varying degrees of result accuracy and simulation performance.

Simulation option selection

- The first option is generally the fastest and least accurate.
- Each successive option is generally slower and more accurate.

ideal gnd

Recommended for investigation of DC current crowding due to via anti-pads

Non-ideal gnd

Recommended for via current investigation

Cut board based on enabled pwr nets

Non-ideal gnd

Recommended for final signoff

Full board

Note:

For VRM and sink setup, gnd nets must be selected even for ideal gnd simulation options.

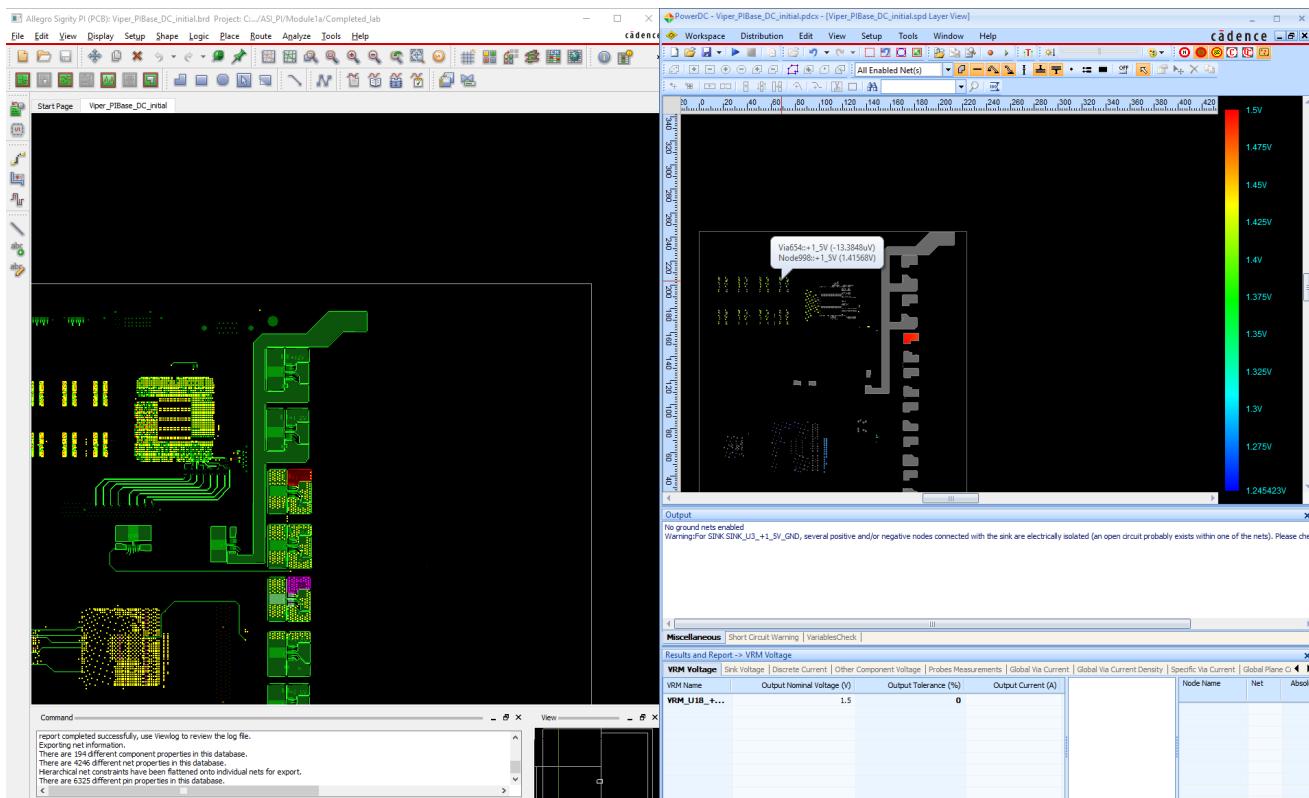
- *Ideal gnd* — Provides the fastest simulation results. However, the accuracy is the lowest when compared to the other options. This option is recommended for the analysis of DC current crowding due to a large number of via antipads.
- *Non-ideal gnd - Cut board based on enabled pwr nets* — The simulation run time and the result accuracy are higher than the Ideal ground option. Based on the enabled power nets range, the system automatically finds the bounding box and cuts the board to translate. None of the nets outside of the bounding box are translated.
- *Non-ideal gnd - Full board* — Provides the slowest but the most accurate simulation results of the three simulation options. This option is recommended for the final signoff

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

Cross-Probing between Allegro Layout and PowerDC

Cross-probing is enabled between the Allegro layout window and the IR Drop result display window (PowerDC) for layer visibility and the zoom or pan functionality. When the analysis is complete, the dual window configuration appears as shown in the following image.



You can cross-probe between the Allegro layout and PowerDC. When you zoom or pan in the Allegro layout, PowerDC zooms or pans simultaneously. The reverse is also true. Similarly, when you select a specific layer in one, the corresponding layer is selected in the other. The flow also supports importing results from an external run in PowerDC.

Via Plating Editing in DC Analysis

Via Plating Thickness can be edited in DC Analysis when accessed from Allegro Sigrity PI.

Passing Component Height and Outline Information

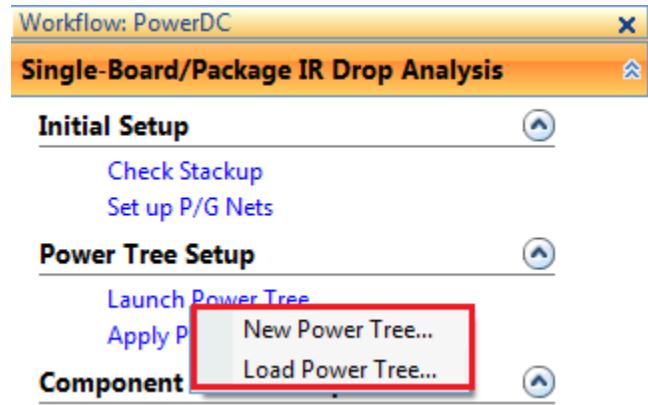
Component height and outline information is passed from Allegro Sigrity PI to PowerDC to reduce the setup effort needed for thermal analysis.

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

DC Analysis Setup Automation with PowerTree and AMM

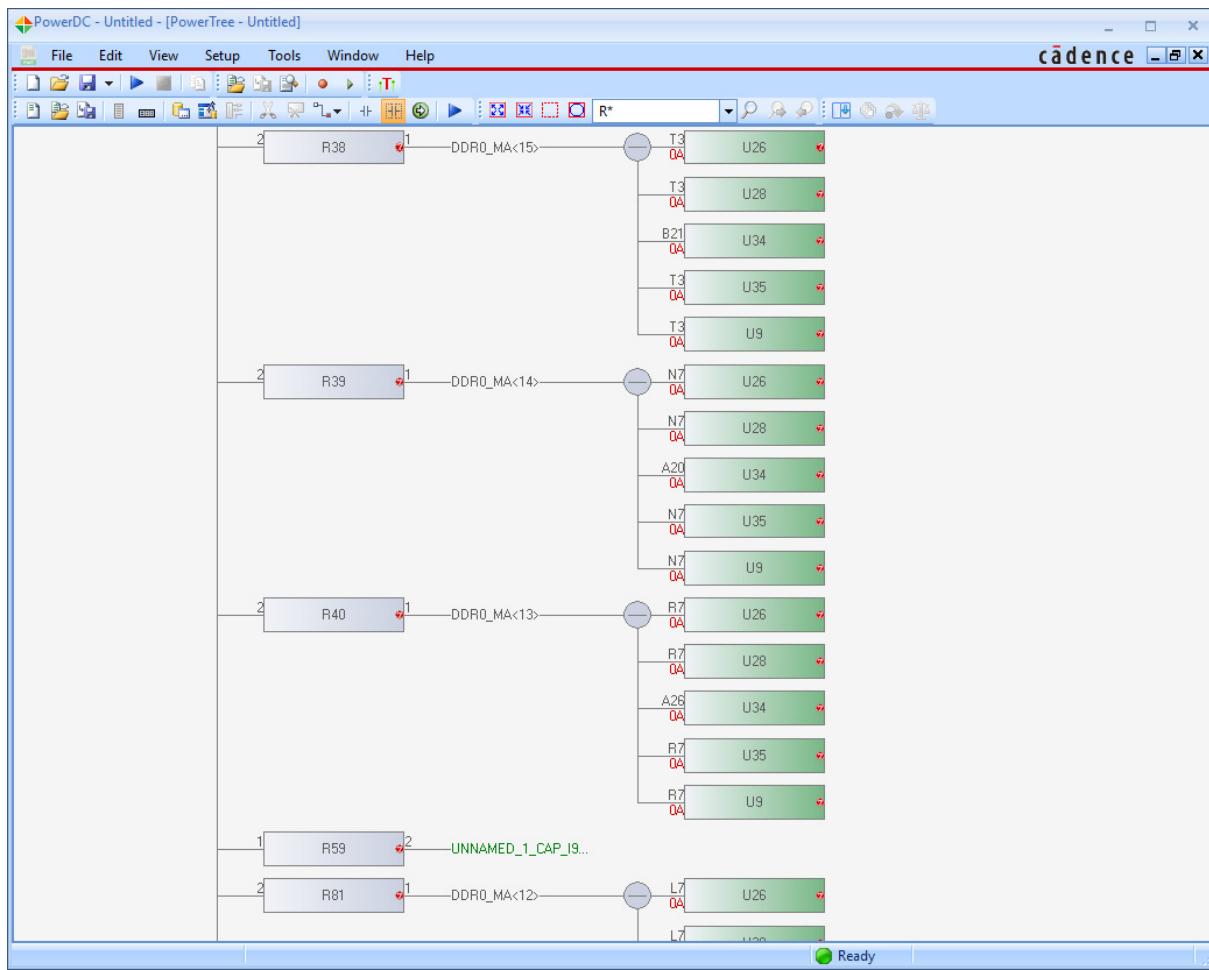
In Allegro Sigrity PI driven PowerDC (*DC Analysis Interactive Mode*), you can create or load a power tree. To create a new power tree, the system automatically uses the board file.



Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

You can specify the starting component for power tree generation. In the PowerTree canvas, AMM can be launched if you want to use AMM data to overwrite the PowerTree properties. After the power tree is ready, you can apply it to PowerDC to create the workspace.



For more information about the PowerTree application, refer to *PowerTree User Guide* and *PowerDC User Guide*.

DC Analysis in Batch Mode

In the batch mode, you can run DC analysis and view the results and report directly in the Allegro layout environment, without having to launch the PowerDC user interface. You specify a workspace that includes all the settings for the simulation. An HTML report is generated and displayed at the end of the simulation.

Note: You can also run DC analysis in batch mode using the *Allegro PCB Designer product with the High Speed option*, with the Allegro Sigrity PI (PA5800) license.

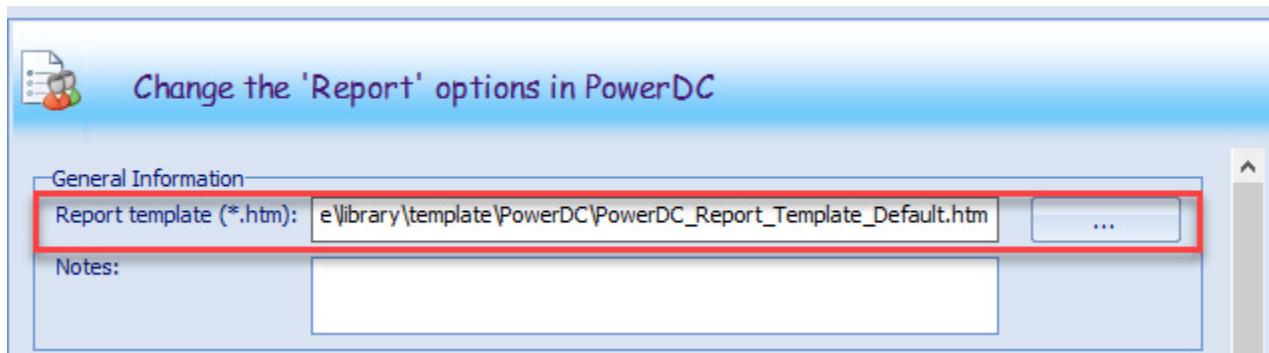
Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

The following capabilities of DC analysis are available in the batch mode:

- Cross-probing between the report and the Allegro layout
- DRC marks can be backed to the Allegro layout
- Workspace settings can be reused
- An option is provided to control the nets to be translated from workspace

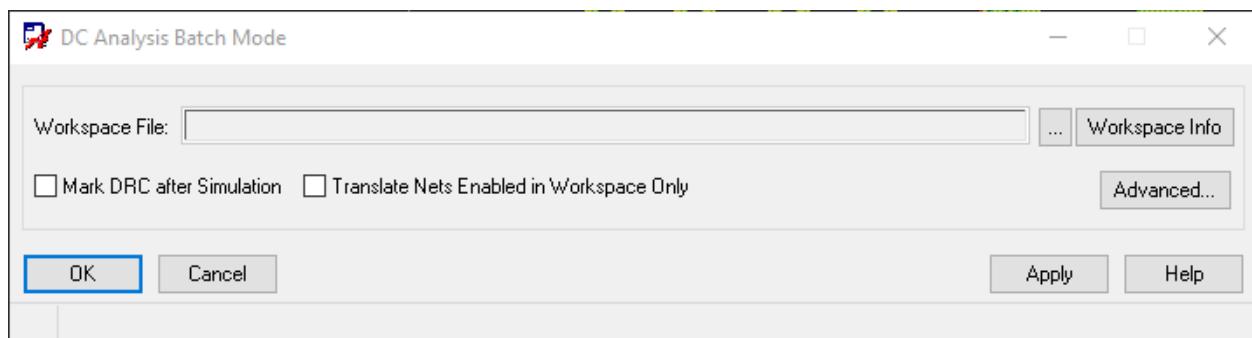
Note: Specify the HTML template in PowerDC from *Tools – Options – Edit Options* in the *Report* section before running the batch mode in Allegro Sigrity PI.



Working in the Batch Mode

To run DC analysis in the batch mode, perform the following steps:

1. Choose *Analyze – DC Analysis Batch Mode*.

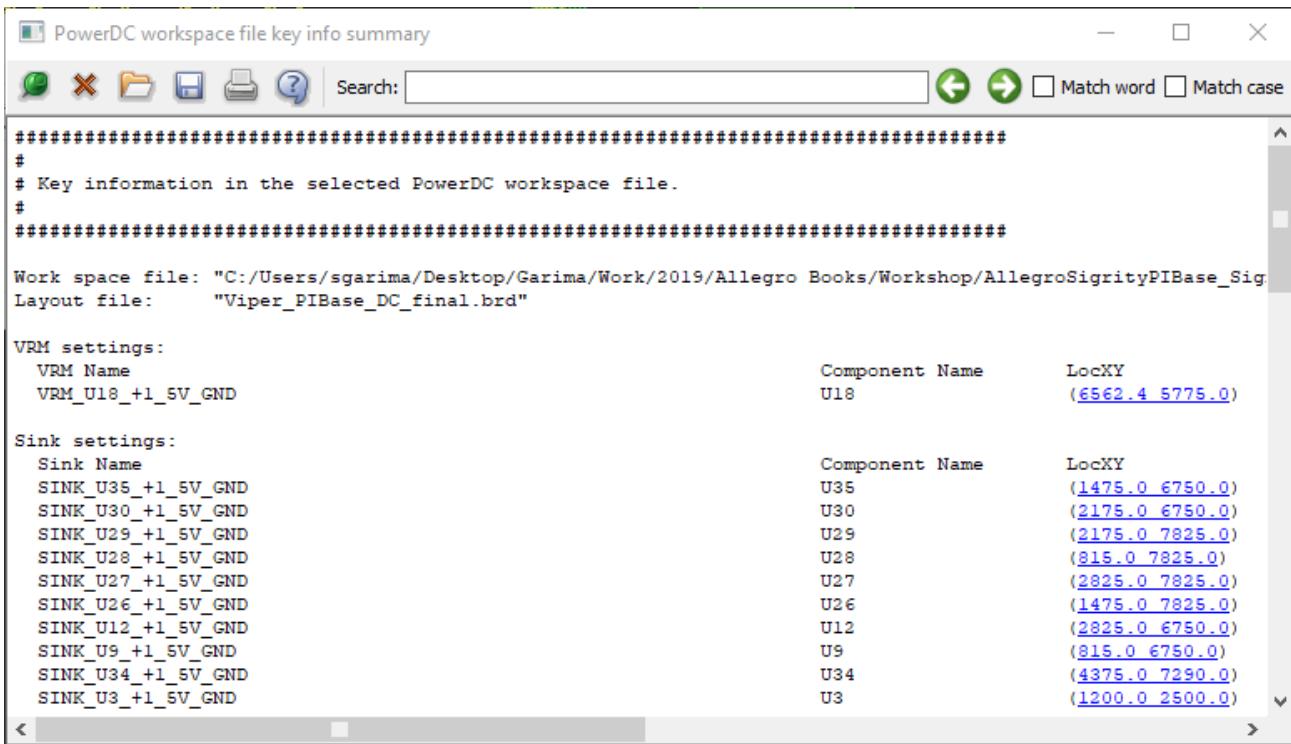


2. Select the workspace to be used for DC analysis in the batch mode.

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

A summary of the workspace is displayed.



The screenshot shows a window titled "PowerDC workspace file key info summary". It contains a search bar and several icons. The main content area displays configuration details:

```
#####
# Key information in the selected PowerDC workspace file.
#
#####
Work space file: "C:/Users/sgarima/Desktop/Garima/Work/2019/Allegro Books/Workshop/AllegroSigrityPIBase_Sig
Layout file:      "Viper_PIBase_DC_final.brd"

VRM settings:
  VRM Name          Component Name    LocXY
  VRM_U18_+1_5V_GND U18              (6562.4 5775.0)

Sink settings:
  Sink Name          Component Name    LocXY
  SINK_U35_+1_5V_GND U35              (1475.0 6750.0)
  SINK_U30_+1_5V_GND U30              (2175.0 6750.0)
  SINK_U29_+1_5V_GND U29              (2175.0 7825.0)
  SINK_U28_+1_5V_GND U28              (815.0 7825.0)
  SINK_U27_+1_5V_GND U27              (2825.0 7825.0)
  SINK_U26_+1_5V_GND U26              (1475.0 7825.0)
  SINK_U12_+1_5V_GND U12              (2825.0 6750.0)
  SINK_U9_+1_5V_GND   U9               (815.0 6750.0)
  SINK_U34_+1_5V_GND U34              (4375.0 7290.0)
  SINK_U3_+1_5V_GND  U3               (1200.0 2500.0)
```

Note: This workspace should be created in PowerDC in the standalone mode.

Workspace Reuse Check

In a PowerDC workspace, some physical nodes associated with VRMs/Sinks might not be reusable if changes are made to a shape, trace, or a via in the layout in the Allegro layout environment. This can lead to discrepancies between the updated layout and the original physical node names in the workspace when the design is loaded in the Sigrity environment.

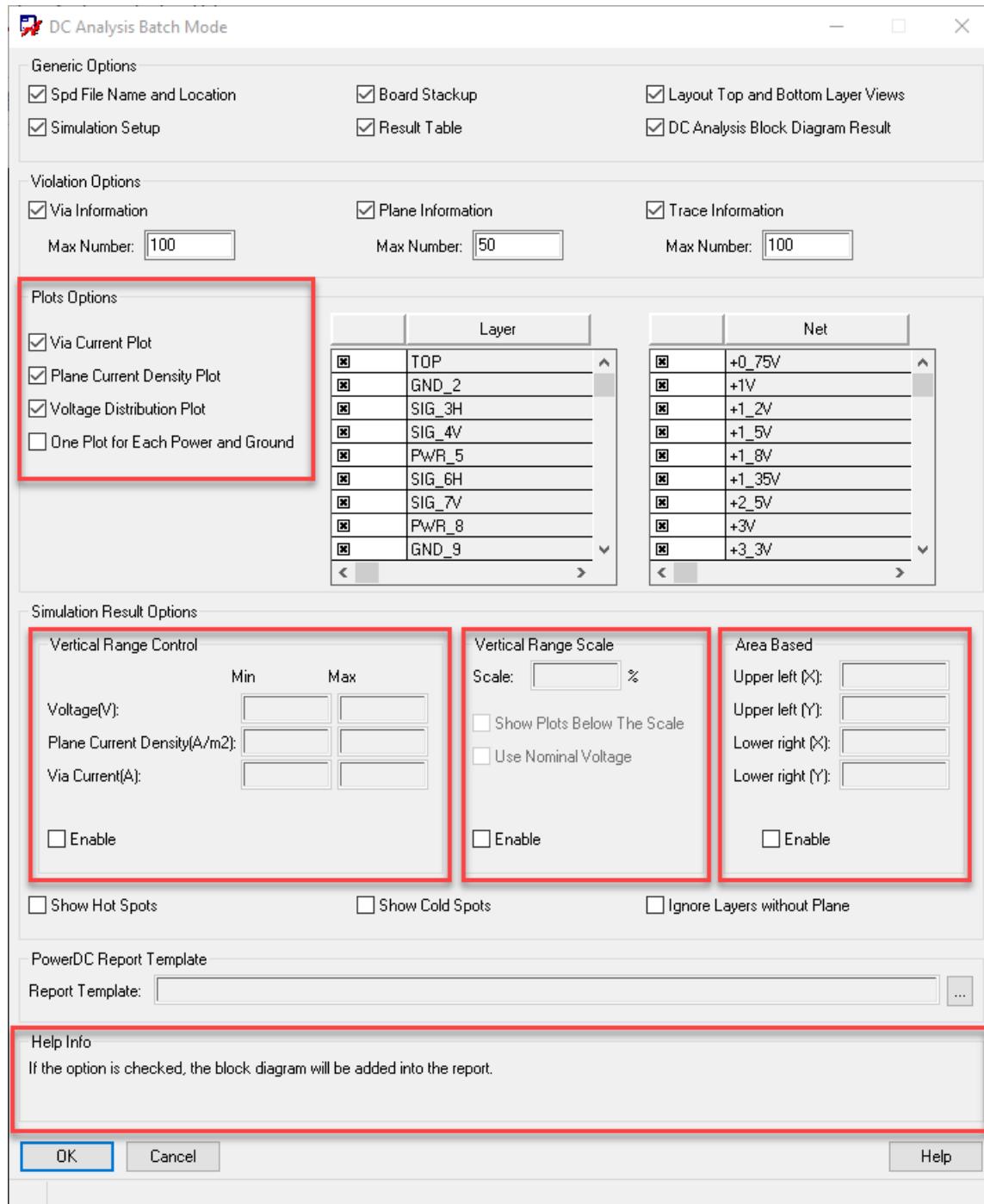
A check flags this situation as a warning if you continue to use the same workspace for DC setup.

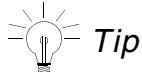
3. To automatically mark violations in the Allegro layout after the simulation, click the *Mark DRC after Simulation* check box.
4. To translate only those nets which are enabled in the workspace, click the *Translate Nets Enabled in Workspace Only* check box.
5. To set options for DC Analysis reports, click the *Advanced* button.

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

DC Analysis Batch Mode - Advanced form is displayed. In this form, you can set options to generate specific distribution plots in the report:



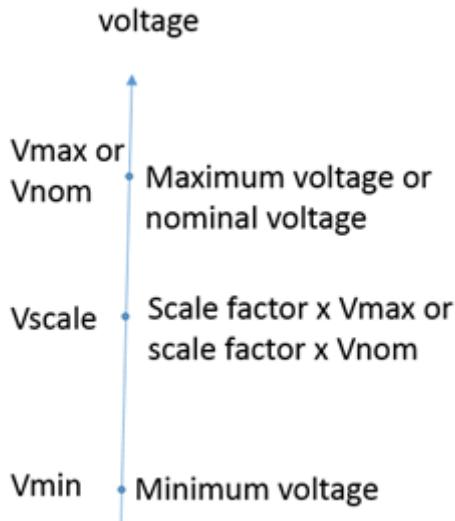


Tip

Hover the mouse pointer over the various fields and options in the form to view the help information in the *Help Info* section of the form.

6. Click the *Enable* check box in the *Vertical Range Control* section.
7. Specify the minimum and maximum values for *Voltage*.

Vertical Range Scale: For voltage plots, the maximum value or nominal value is used to calculate the middle point based on the scale factor. For other plots, the maximum value of the color bar is always be used to calculate the middle point.



8. Select the *Enable* check box in the *Vertical Range Scale* section.
9. Specify a scale factor in the *Vertical Range Scale* field.

Use Nominal Voltage: When selected, the voltage distribution plot range is from minimum to nominal voltage. Other plots still use maximum value to calculate the middle point. The maximum value on the color bar for all distribution plots is used if this option is not selected.

Show Plots Below the Scale: If this option is selected, the distribution plots range is from minimum to (1-scale) maximum.

10. Select the *Enable* check box in the *Area Based* section.

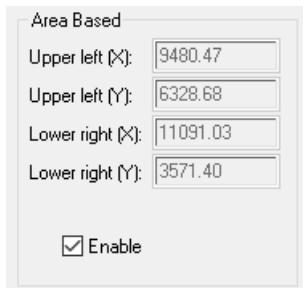
This displays area-based distribution plots in the report.

11. Draw a bounding box in the Allegro canvas to select an area for report generation.

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

The XY coordinates of the bounding box are populated in the corresponding fields in the Area Based section:



Some other options to control the distribution plots in the report include:

- Show Hot Spots*: Click this check box to display all the hot spots in the plots.
- Show Cold Spots*: Click this check box to display all the cold spots in the plots.
- Ignore Layers without Plane*: Click this check box to hide the layers without shapes in the distribution plots for the report.

12. Click *OK* to close the DC Analysis Batch Mode advanced settings form.

13. Click *OK* to close the DC Analysis Batch Mode form.

DC analysis is run in the batch mode and a report in the HTML format is displayed.

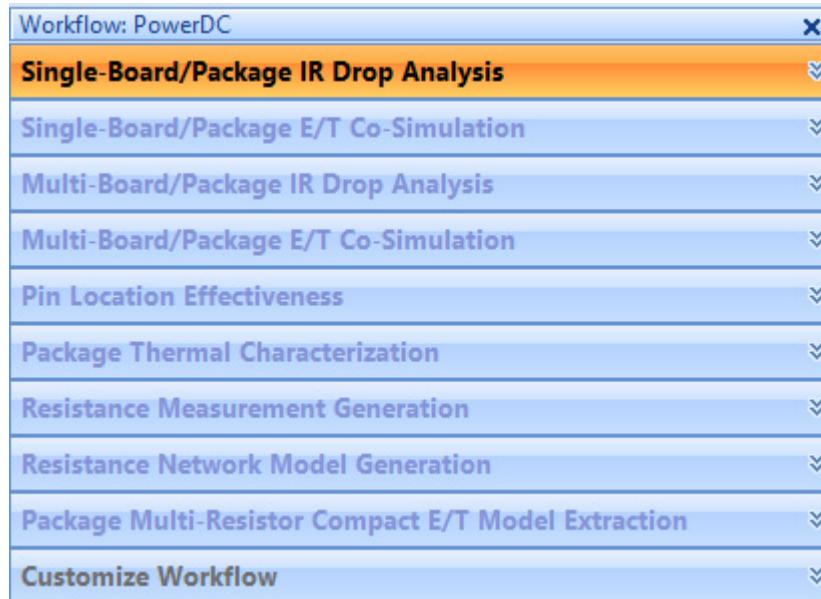
Running DC Analysis in PowerDC

Only the *Single-Board/Package IR Drop Analysis* workflow with limited functions is enabled in PowerDC in the interactive mode. To leverage the true capabilities of PowerDC,

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

use *Analyze – PowerDC* to launch PowerDC where all the nine flows of the PowerDC solution are enabled.

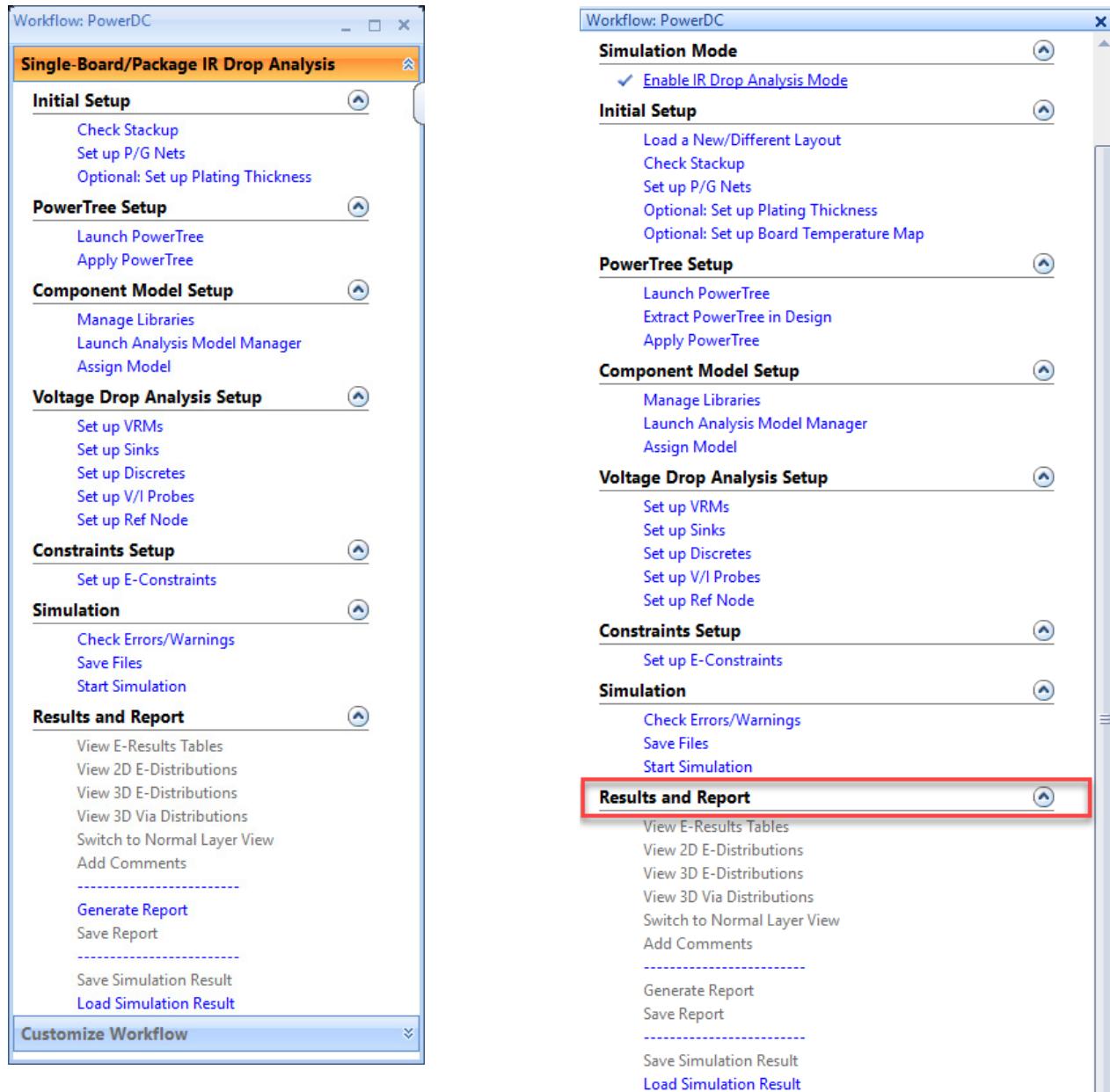


For detailed information on PowerDC, see the *PowerDC User Guide*.

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

The functionalities available in PowerDC when you open it from *Analyze* menu are illustrated in the following image:



Analyze – DC Analysis Interactive Mode:
Only a limited set of tasks in the
Single-Board/Package IR Drop Analysis
flow

Analyze – PowerDC: All the
Complete functionality available for the
Single-Board/Package IR Drop Analysis flow

Adding DC Analysis Violation Markers

This section covers the following topics:

- [Overview](#)
- [Manually Adding PowerDC Violation Markers in Allegro Canvas](#)
- [Automatically Adding PowerDC Violation Markers in Allegro Canvas](#)

Overview

The PowerDC DRC marking process in Allegro Sigrity PI helps you identify problem areas, such as high current density locations. Once identified, you can edit the layout to resolve these hotspots with ease. In the existing process of adding PowerDC DRC to Allegro canvas, after running a PowerDC simulation, you need to run SKILL functions to add DRC markers to Allegro canvas.

With the enhancement in the current release, PowerDC DRC marking on Allegro canvas is just a matter of a few clicks in the GUI. You can now select a specific PowerDC simulation results file and manually mark DC violations on the Allegro canvas. Allegro Sigrity PI also provides the functionality to automatically add the markers to Allegro canvas after a PowerDC simulation completes.

Manually Adding PowerDC Violation Markers in Allegro Canvas

You can manually select the type of DRCs from the list of available DRCs, such as sink voltage, discrete current, global via current, and so on, and add them to the Allegro canvas. You use the DC Violation Marker dialog to select and mark DRCs.

Note: Before marking violations on the canvas, you need to ensure that design rules and E-constraints are set using Constraints Setup in PowerDC. Without setting up these constraints, violations cannot be captured in PowerDC. For information on how to set up constraints in PowerDC, refer to PowerDC Tutorial.

To mark DRCs on the canvas, perform the following steps:

1. Launch Allegro Sigrity PI.
2. Choose *File – Open* to open the board file.
3. Choose *Analyze – DC Violation Marker*.

The DC Violation Marker form is displayed.

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Working with DC Analysis Options

4. Browse to the PowerDC results file.

The number of violations recorded in the `.xml` file appear along with the DRC type.

Figure 4-1 DC Violation Marker Dialog

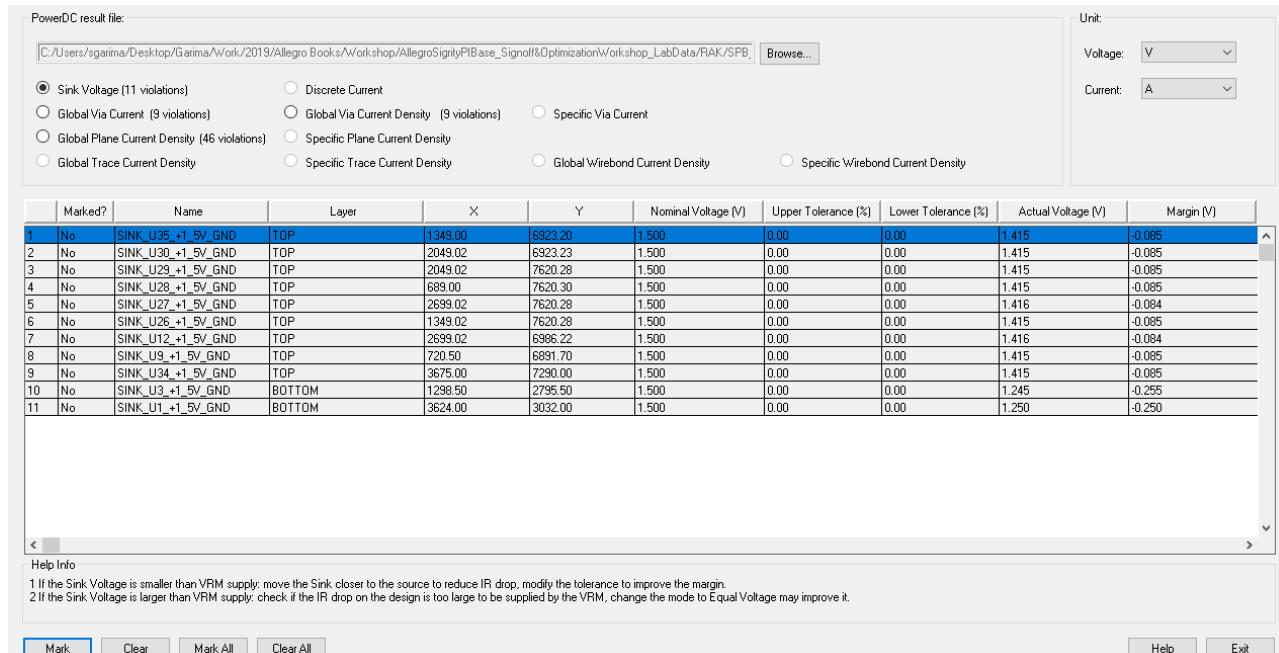


Table 4-1 DC Violation Marker Dialog

Field	Description
<i>PowerDC result file</i>	Browse to the PowerDC simulation results file (<code>.xml</code>), which contains the PowerDC violations. After the file is selected, the PowerDC DRC information is read and displayed in this dialog.
<i>DRC types to mark</i>	Select the type of DRC you want to mark on the canvas. The number of violations recorded in the <code>.xml</code> file appear along with the DRC type.
<i>Unit</i>	Select the units for <i>Voltage</i> and <i>Current</i> from the drop-down lists.
<i>Mark</i>	Click this button to mark the selected DRC types on the Allegro canvas. When done, the DRC mark appears on the canvas and the details of the DRC information are also displayed in a text editor.

Allegro Sigrity PI Flow Guide

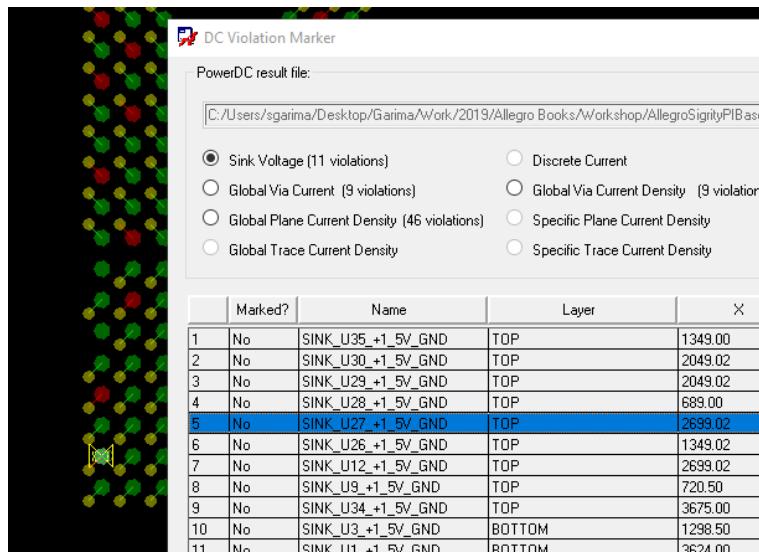
Working with DC Analysis Options

Field	Description
<i>Clear</i>	Clear the related DRC mark on the Allegro canvas.
<i>Mark All</i>	Click this button to mark all the DRC types on the Allegro canvas.
<i>Clear All</i>	Clear all the related DRC marks on the Allegro canvas.

When you select a row in this dialog, the selected component is zoomed-in to the exact location on the canvas.

5. Select a row.

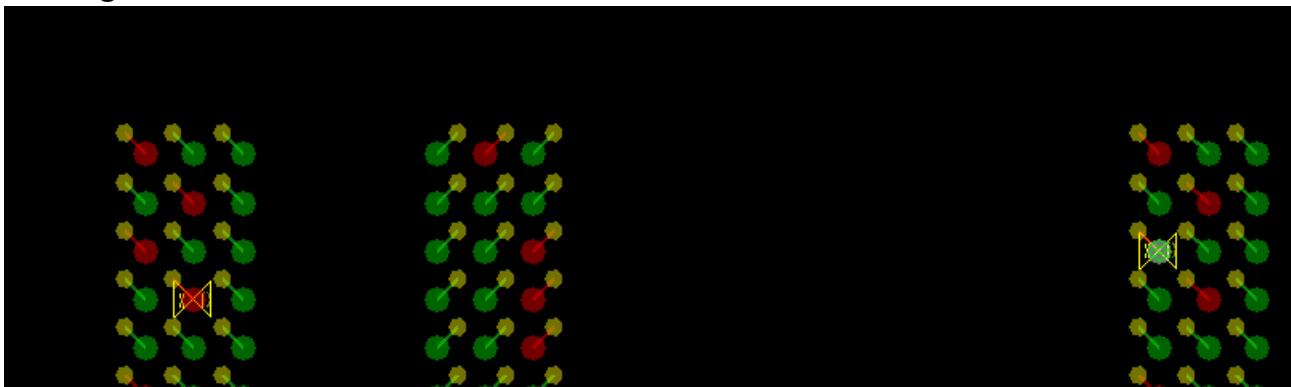
Figure 4-2 PowerDC DRC Viewer Dialog - Selecting a Row



6. Click *Mark* in the DC Violation Marker dialog.

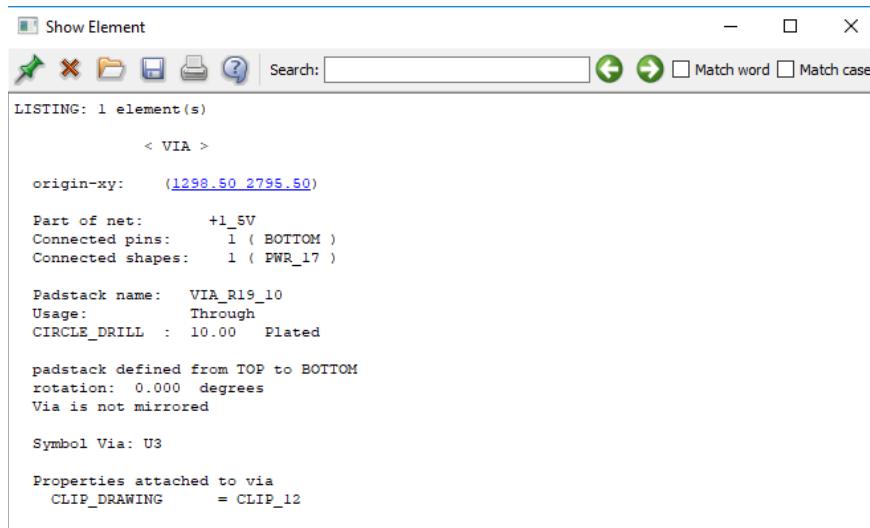
The selected DC violations are marked on the canvas.

Figure 4-3 DC Violations Marked on Canvas



7. Right-click the canvas and choose *Done* from the context menu to complete placing the markers.
8. To check the details of a DRC, right-click the marker and choose *Show Element* from the context menu.

Figure 4-4 DRC Details for the Selected Element



9. Close the Show Element editor.

This completes manual addition of a PowerDC DRC marker to the Allegro canvas.

Automatically Adding PowerDC Violation Markers in Allegro Canvas

You can also mark PowerDC DRC markers to the Allegro canvas automatically. You launch the DC Analysis flow from Allegro Sigrity PI and run the simulation. When the simulation completes, DRCs are marked automatically in the Allegro canvas.

Allegro Sigrity PI Flow Guide

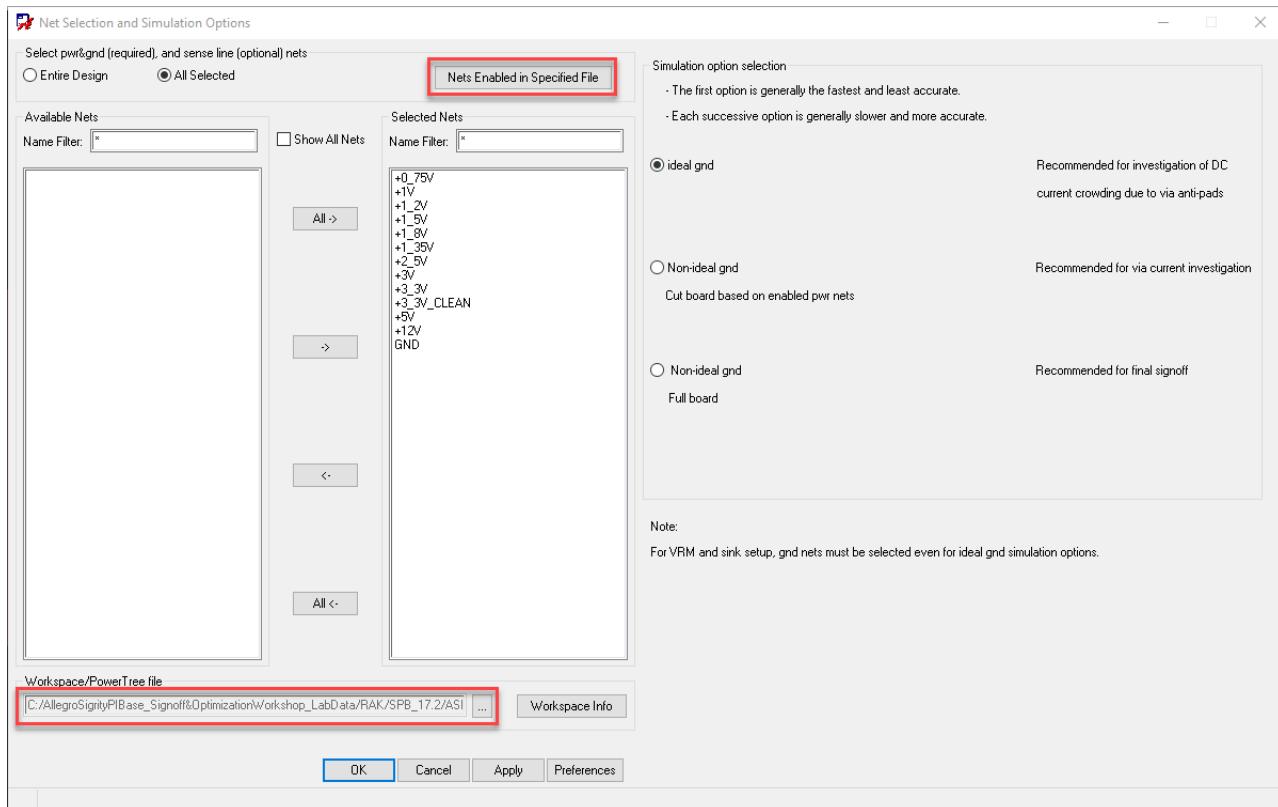
Working with DC Analysis Options

To automatically mark DC violations on the canvas, do the following:

1. Launch Allegro Sigrity PI.
2. Choose *File – Open* to open the board file.
3. Choose *Analyze – DC Analysis Interactive Mode* to start the DC analysis flow.

The XNet Selection dialog appears. You can optionally specify the existing workspace file to be opened in PowerDC in the *Workspace file* field. When PowerDC launches, the selected workspace file is loaded along with all the settings in it.

Figure 4-5 XNet Selection Dialog – Specifying Workspace File

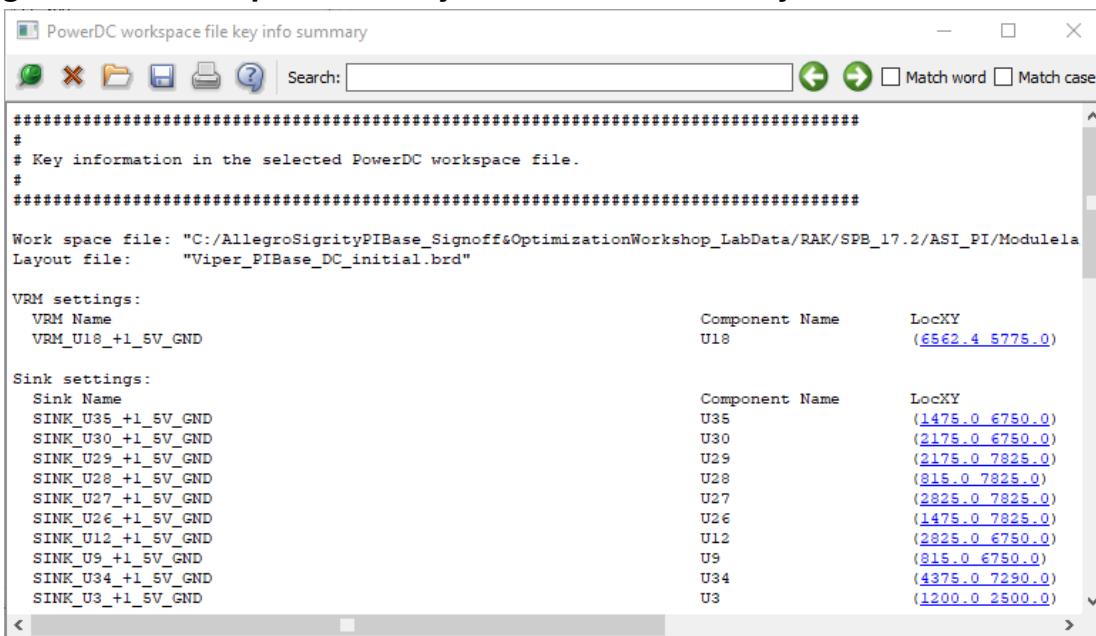


As soon as you select the existing workspace file, the summary of its contents is displayed. You can also open the workspace file and view it by clicking the ellipsis (...) next to the *Browse* button.

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

Figure 4-6 Workspace File Key Information Summary



The screenshot shows a window titled "PowerDC workspace file key info summary". The content displays key information from a workspace file, including the workspace and layout files, VRM settings, and sink settings. The VRM settings table lists a single component U18 at location (6562.4, 5775.0). The sink settings table lists multiple components (U35 to U3) with their respective locations.

Component Name	LocXY
U18	(6562.4 5775.0)

Sink Name	Component Name	LocXY
SINK_U35_+1_5V_GND	U35	(1475.0 6750.0)
SINK_U30_+1_5V_GND	U30	(2175.0 6750.0)
SINK_U29_+1_5V_GND	U29	(2175.0 7825.0)
SINK_U28_+1_5V_GND	U28	(815.0 7825.0)
SINK_U27_+1_5V_GND	U27	(2825.0 7825.0)
SINK_U26_+1_5V_GND	U26	(1475.0 7825.0)
SINK_U12_+1_5V_GND	U12	(2825.0 6750.0)
SINK_U9_+1_5V_GND	U9	(815.0 6750.0)
SINK_U34_+1_5V_GND	U34	(4375.0 7250.0)
SINK_U3_+1_5V_GND	U3	(1200.0 2500.0)

4. Click OK.

PowerDC launches. You can edit the workspace in the PowerDC GUI, and run the simulation. When the simulation process completes, all the specific DRCs are automatically marked in the Allegro canvas.

Viewing DC Analysis Reports

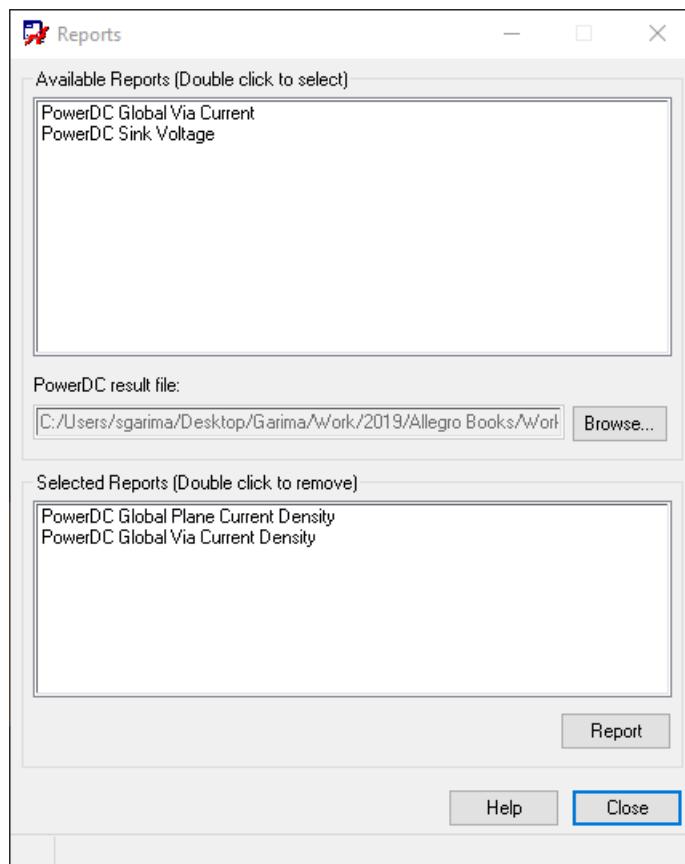
DC analysis reports are accessible from the *Analyze – DC Report* menu:

- Violation Report
- Full Report

Violation Report

To view a violation report, perform the following steps:

1. Choose *Analyze – DC Report – Violation Report*.
2. Browse to the PowerDC simulations results file.
3. Double-click one of the available reports to move it to the selected reports list and click *Report*.



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Working with DC Analysis Options

The selected report is displayed.

PowerDC Global Plane Current Density						
Layer	Left Top	Right Bottom	Global Plane Current Density Constraint(A)	Actual Plane Current Density(A)	Margin(A)	
PWR_17	(6389.685 6042.756)	(6415.827 6012.756)	155.000	202.911	47.911	
PWR_17	(6419.410 6067.756)	(6480.591 6025.118)	155.000	304.592	149.592	
PWR_17	(6519.410 6067.756)	(6580.591 6029.370)	155.000	300.735	145.734	
PWR_17	(6619.410 6067.756)	(6677.638 6029.370)	155.000	301.009	146.008	
PWR_17	(7300.000 5990.000)	(7332.992 5947.284)	155.000	177.988	22.988	
PWR_17	(5424.843 3352.284)	(5472.244 3320.512)	155.000	263.879	108.878	
PWR_17	(5326.614 3352.205)	(5374.331 3320.512)	155.000	266.322	111.322	
PWR_17	(5250.512 3074.488)	(5298.229 3044.449)	155.000	238.346	83.345	
PWR_17	(5506.536 3074.488)	(5554.252 3042.874)	155.000	244.652	89.652	
PWR_17	(6619.410 6170.630)	(6673.110 6127.244)	155.000	282.354	127.354	
PWR_17	(6519.410 6170.630)	(6580.591 6132.244)	155.000	302.038	147.038	
PWR_17	(6419.410 6170.630)	(6480.591 6132.244)	155.000	303.387	148.387	
PWR_17	(6389.685 6187.244)	(6415.827 6157.244)	155.000	202.257	47.257	
PWR_17	(6584.173 6092.756)	(6615.827 6057.244)	155.000	248.244	93.243	
PWR_17	(6584.173 6042.756)	(6615.827 6018.898)	155.000	194.529	39.528	

Allegro Sigrity PI Flow Guide

Working with DC Analysis Options

Full Report

You can load an existing DC analysis report (html file) directly from the *Analyze – DC Reports – Full Report*. If a report is available for the current layout, that report is automatically selected.

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1.2 Board Stackup

Layer #	Layer Name	Thickness(mm)	Material	Conductivity(S/m)	Er	Loss Tangent	Fill-in Dielectric	ShapeName	TraceWidth(nm)	Roughness(nm)
	Medium\$40	0.0508	FR_4_1	0						
1	Signal\$TOP	0.03302	COPPER				FR_4_1	Signal\$TOPpkgshape	0.1016	0
	Medium\$42	0.0762	FR_4_1	0						
2	Plane\$GND_2	0.01524	COPPER				FR_4_1	Plane\$GND_2pkgshape		
	Medium\$44	0.0762	FR_4_1	0						
3	Signal\$SIG_3H	0.01524	COPPER				FR_4_1	Signal\$SIG_3Hpkgshape	0.1016	0
	Medium\$46	0.254	FR_4_1	0						
4	Signal\$SIG_4V	0.01524	COPPER				FR_4_1	Signal\$SIG_4Vpkgshape	0.1016	0
	Medium\$48	0.0762	FR_4_1	0						
5	Plane\$PWR_5	0.01524	COPPER				FR_4_1	Plane\$PWR_5pkgshape		
	Medium\$50	0.0762	FR_4_1	0						
6	Signal\$SIG_6H	0.01524	COPPER				FR_4_1	Signal\$SIG_6Hpkgshape	0.1016	0
	Medium\$52	0.254	FR_4_1	0						
7	Signal\$SIG_7V	0.01524	COPPER				FR_4_1	Signal\$SIG_7Vpkgshape	0.1016	0
	Medium\$54	0.0762	FR_4_1	0						
8	Plane\$PWR_8	0.03302	COPPER				FR_4_1	Plane\$PWR_8pkgshape		
	Medium\$56	0.2032	FR_4	0						
9	Signal\$GND_9	0.03302	COPPER				FR_4_1	Plane\$GND_9pkgshape	0.1	0
	Medium\$58	0.0762	FR_4_1	0						
10	Signal\$PWR_10	0.03302	COPPER				FR_4_1	Plane\$PWR_10pkgshape	0.1	0
	Medium\$60	0.0762	FR_4_1	0						
11	Plane\$GND_11	0.03048	COPPER				FR_4	Plane\$GND_11pkgshape		
	Medium\$62	0.2032	FR_4	0						
12	Signal\$SIG_12H	0.01524	COPPER				FR_4_1	Signal\$SIG_12Hpkgshape	0.1016	0
	Medium\$64	0.254	FR_4_1	0						
13	Signal\$SIG_13V	0.01524	COPPER				FR_4_1	Signal\$SIG_13Vpkgshape	0.1016	0
	Medium\$66	0.0762	FR_4_1	0						

You can also display a PowerDC sign-off report using the *Allegro PCB Designer product with the High Speed option*.

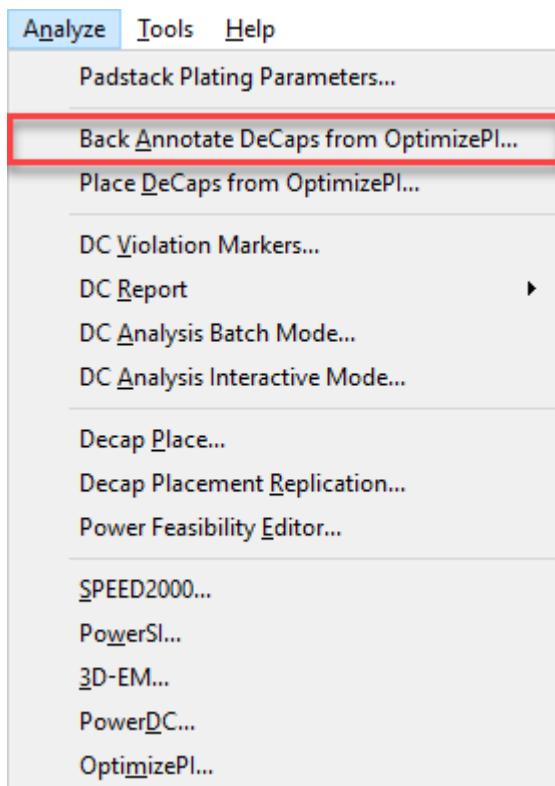
Working with OptimizePI

This chapter covers the following topics:

- [Overview](#)
- [Decap Back-Annotation from OptimizePI](#)
- [Place DeCaps from OptimizePI](#)

Overview

OptimizePI helps you make cost versus performance trade-off decisions based on interactive post-processing of optimization results. Allegro Sigrity PI provides commands to work with OptimizePI from within Allegro layout. You can place decaps in the layout from OptimizePI. Based on the analysis results, you can decide to remove a decap or replace it with a different decap.



Decap Back-Annotation from OptimizePI

You can use OptimizePI to optimize a design by removing decaps from an existing design, replacing decaps, or adding new decaps (for EMI decaps). All these changes need to be back annotated to the Allegro Sigrity PI database automatically.

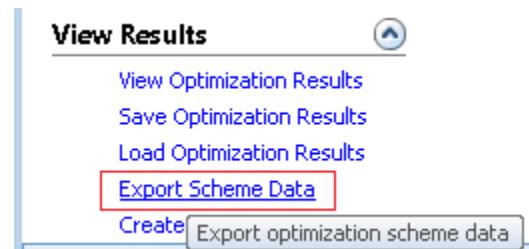
- Use the *Analyze – Back Annotate DeCaps from Optimize* to backannotate the updates in OptimizePI to the Allegro layout database.

To generate the report file and netlist file for a specific scheme, perform the following steps:

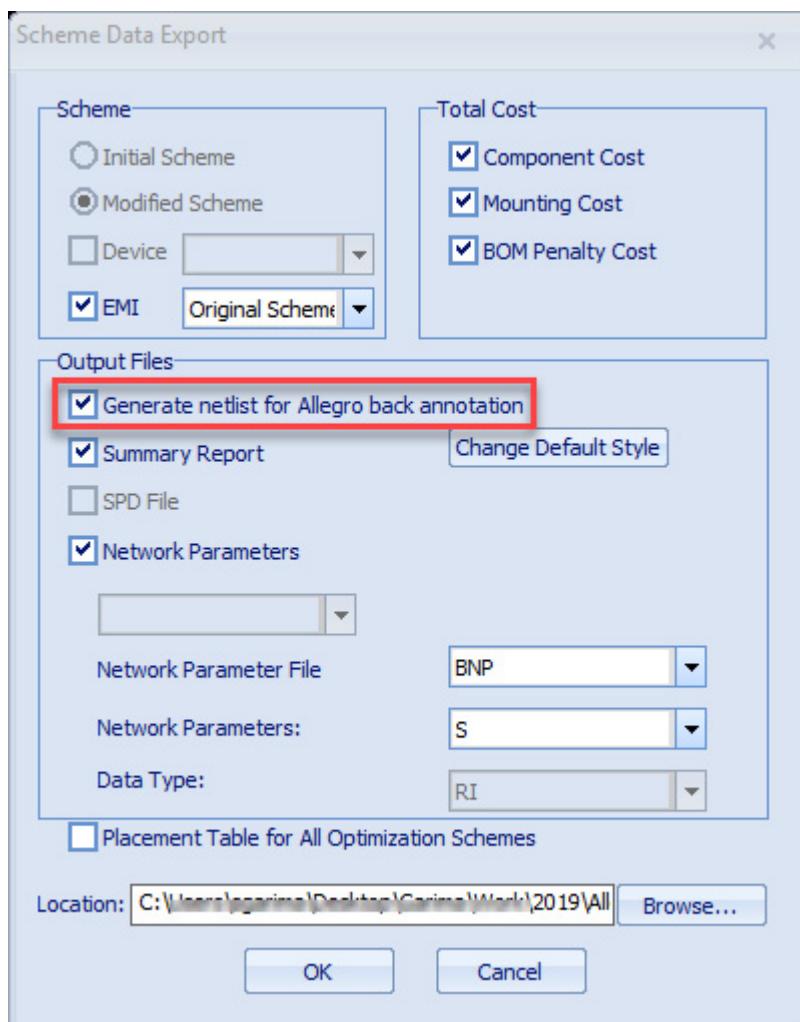
Allegro Sigrity PI Flow Guide

Working with OptimizePI

1. In Optimize PI, after the simulation completes, select *Export Scheme Data* in the workflow.



2. Select the *Generate netlist for Allegro back annotation* option in the Scheme Data Export dialog.

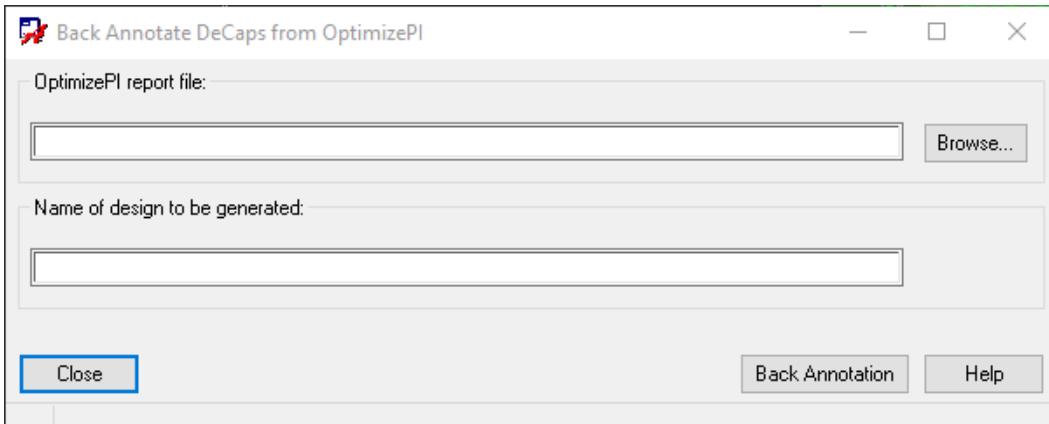


3. Click *OK*.

Allegro Sigrity PI Flow Guide

Working with OptimizePI

4. In Allegro Sigrity PI, open the original board file.
5. Choose *Analyze – Back Annotate DeCaps from OptimizePI*.



6. Browse to the report file for backannotation generated in OptimizePI.
7. Specify a name for the generated design.
8. Click *Back Annotation*.
All the changes are back annotated to the board file.
9. Click *Close*.

Place DeCaps from OptimizePI

After backannotating the changes to the board file, you can place or unplace decaps in Allegro layout.

1. Choose *Analyze – Place DeCaps from OptimizePI*.
2. Browse to the report file generated in OptimizePI.

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Working with OptimizePI

All the decaps changed are listed as illustrated in the following figure:

The screenshot shows a Windows dialog box titled "Place DeCaps from OptimizePI". At the top, there is a "Report File:" dropdown set to "C:\...\OptimizePI\Reports\10212023\Workshop\AllegroSigrityPIBase_Signoff\Optimization\Workshop_LabData\RAK\SPB_17.2\ASI_PI\Module", with a "Browse..." button. Below the header is a table with the following columns: Refdes, Status, PartNo, Original PartNo, Package Symbol, Layer, LocXY, and Rotation. The "Status" column uses color coding: red for "Unplaced" components and green for "Placed" components. The table lists 22 rows of component information, all with the package symbol "CAPC1608N" and layer "BOTTOM". The "Rotation" column shows values like 180.00, 0.00, and 120.00. At the bottom of the dialog are "OK", "Cancel", "Place", and "Help" buttons.

Refdes	Status	PartNo	Original PartNo	Package Symbol	Layer	LocXY	Rotation
C181	Unplaced	CAP_0603-CDN-CAP_7009	CAP_0402-CDN-CAP_0038	CAPC1608N	BOTTOM	(11915.00:850.00)	180.00
C312	Unplaced	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(11590.00:1170.00)	0.00
C317	Placed	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(10185.00:2420.00)	0.00
C379	Placed	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(8240.00:1475.00)	0.00
C388	Placed	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(8382.00:600.00)	180.00
C389	Placed	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(10395.00:1525.00)	180.00
C393	Unplaced	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(10395.00:1585.00)	180.00
C394	Unplaced	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(10120.00:975.00)	0.00
C395	Placed	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(9800.00:1615.00)	180.00
C396	Unplaced	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(9780.00:980.00)	180.00
C399	Unplaced	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(10395.00:1360.00)	180.00
C400	Unplaced	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(10120.00:920.00)	0.00
C401	Unplaced	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(10395.00:1305.00)	180.00
C403	Unplaced	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(10275.00:920.00)	0.00
C404	Unplaced	CAP_0603-CDN-CAP_7009	CAP_0603-CDN-CAP_7001	CAPC1608N	BOTTOM	(10395.00:1195.00)	180.00

3. Place or remove decaps in the design.

You can choose browse from the Package Symbol drop-down list box to find a proper footprint if the package symbol is not found.

