

Topology Workbench Known Problems and Solutions

Product Version 23.1
October 2023

© 2023 Cadence Design Systems, Inc.

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Open SystemC, Open SystemC Initiative, OSCI, SystemC, and SystemC Initiative are trademarks or registered trademarks of Open SystemC Initiative, Inc. in the United States and other countries and are used with permission.

Trademarks: Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522. All other trademarks are the property of their respective holders.

Restricted Permission: This publication is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this publication, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this publication subject to the following conditions:

1. The publication may be used only in accordance with a written agreement between Cadence and its customer.
2. The publication may not be modified in any way.
3. Any authorized copy of the publication or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
4. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

Disclaimer: Information in this publication is subject to change without notice and does not represent a commitment on the part of Cadence. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information.

Cadence is committed to using respectful language in our code and communications. We are also active in the removal and replacement of inappropriate language from existing content. This product documentation may however contain material that is no longer considered appropriate but still reflects long-standing industry terminology. Such content will be addressed at a time when the related software can be updated without end-user impact.

Restricted Rights: Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor

Contents

<u>Topology Workbench: Known Problems and Solutions</u>	5
<u>Incorrect simulation results produced in SystemSI for a non-standard IBIS-AMI model</u>	5
<u>CCR 2353552: Allegro IDA Reflection should set default frequency to 50MHz</u>	6

Topology Workbench Known Problems and Solutions

Topology Workbench: Known Problems and Solutions

This document describes the known problems in Cadence® Sigrity™ Topology Workbench and suggests the corresponding workarounds. Each problem is identified by a Cadence Change Request (CCR) number.

Note: Unless otherwise stated, the problems described in this document were identified in a OrCAD® and Allegro® 23.1 release or a corresponding Sigrity release. For information about problems that were fixed in this release, see the README file accompanying this release. You can read this file online at downloads.cadence.com.

For information about features of Topology Workbench, see *Topology Workbench User Guide* and *Topology Workbench Frequently Asked Questions*.

Incorrect simulation results produced in SystemSI for a non-standard IBIS-AMI model

Problem: A non-standard IBIS-AMI model created by Synopsys (`synopsys_mp32_ibis_ami`) does not produce correct simulation results in SystemSI. This model can be identified by the following model-specific parameters:

- 'Tstonefile' and 'Rx_R' in the Rx AMI model
- 'Tstonefile', 'Tx_V' and 'Tx_R' in the Tx AMI model

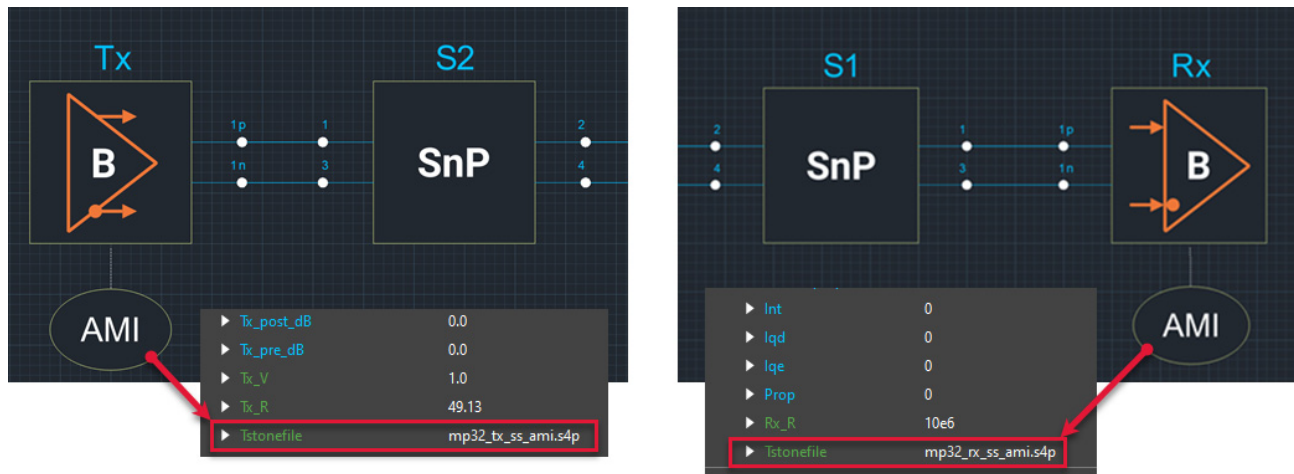
The model attempts to accomplish the functionality found in the IBIS-AMI standard 7.0 and later by the Reserved Keyword 'Ts4file'. It is noteworthy that so far, this model is simulated correctly only in the third-party tool ADS by Keysight.

Solution: Place the S Parameters indicated by the 'Tstonefile' into a *SnP* block and connect the block to the output of the Tx IBIS model and the input of the Rx IBIS model. Connect Ports

Topology Workbench Known Problems and Solutions

Topology Workbench: Known Problems and Solutions

1 and 3 to the output pins of the Tx block and the input pins of the RX block. Refer to the images below for the connection details.



CCR 2353552: Allegro IDA Reflection should set default frequency to 50MHz

Problem: The current Allegro IDA default of 500MHz is way too fast to capture reflection data reliably.

A pulse stimulus is used in the IDA Reflection workflow to enable one simulation to produce results for rising and falling edges. To capture reflection measurements (for example, ring back, overshoot) cleanly, you need to have clear delineation between the rising and falling edges. This means that you want the rising edge to happen, cleanly settle out, and then have a falling edge. This allows the measurement algorithms to differentiate between the rising edge and the falling edge so that the high state and low state measurements can be taken reliably.

If the stimulus pulse frequency is too fast, you get inter-symbol interference (ISI) mixed in with the reflection effects, where the rising edge waveform features get mixed in with the falling edge features. This makes measurements much more difficult, and sometimes unreliable. The whole purpose of the Reflection simulation is to isolate the effects of reflections to enable the user to address them. Therefore, the ISI effects need to be kept out.

Solution: Click *Analysis Options* from the *Reflection* workflow and reduce the *Data Rate* setting to a value significantly slower, for example 50MHz. This typically allows sufficient settling time between the rising and falling edges at the receiver.

If you want to go to the next level of detail and look at the reflection and ISI effects together, use the *Topology Extraction* workflow, and extract the signal into Topology Workbench.

Topology Workbench Known Problems and Solutions

Topology Workbench: Known Problems and Solutions

There you can use bit pattern stimuli to generate full eye diagrams that reflect the impact of both of these effects together.