cadence®

Sigrity Aurora Flow Guide

Product Version 23.1
September 2023

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Contents

1

Signal Analysis using Sigrity Aurora

Sigrity™ Aurora is a signal and power integrity solution integrated into the Allegro® front-to-back PCB design environment.

The purpose of Sigrity Aurora is to enable PCB design engineers to check for potential SI problems within the Allegro environment. It provides analysis in two environments:

- Layout-level analysis in the Allegro IDA (In-Design Analysis) environment
- System-level analysis in the Topology Explorer schematic environment

There are also integrated links between the layout and topology environments that help extract signals from Allegro IDA into Topology Explorer, and capture and pass constraints from Topology Explorer to the PCB Editor design.

Some of the intended use models for Sigrity Aurora are:

- Pre-design floorplanning, feasibility trade-offs, and topological solution space exploration to develop design constraints
- Fast in-design analysis, bringing analysis and result access to the design environment, where design changes can be rapidly made and re-analyzed, to minimize iterations and reduce design cycle time
- Post-layout screening and full-board post-route SI/PI analysis, where large portions of the design can be quickly analyzed for potential problems and outliers can be reviewed and addressed before handing off the design for final sign off with the Sigrity Advanced SI and Advanced PI solutions by SI/PI analysis experts.

Software Prerequisites

To use Sigrity Aurora, Allegro IDA, Topology Explorer, or SystemSI products from Allegro schematic or layout editors, you require ***both*** the following installations:

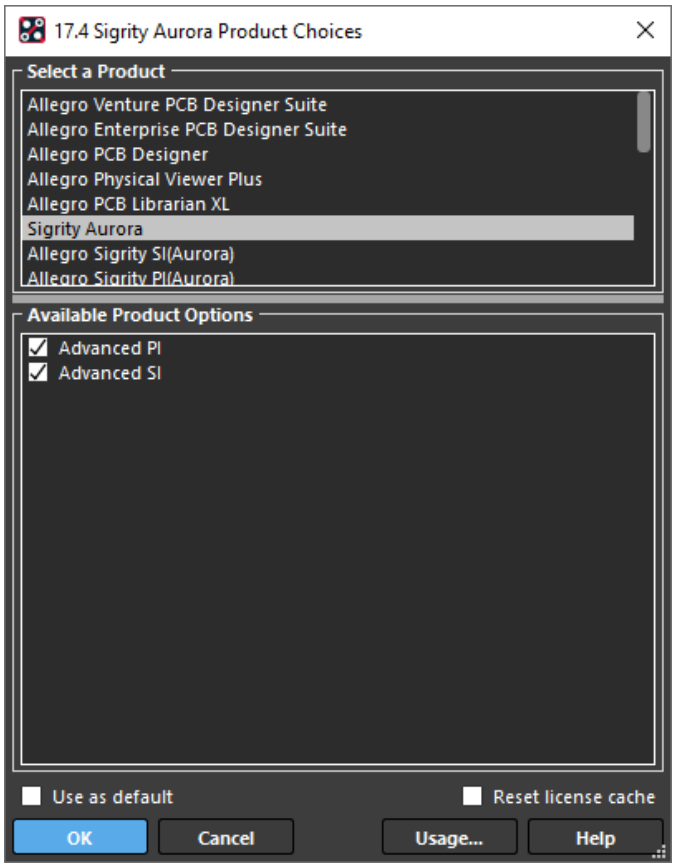
- Sigrity 2019 Hotfix 001 or higher
- OrCAD® and Allegro® Release 17.40-2019 QIR1 or higher

When you install Sigrity 2019 Hotfix 001 or higher, the `SIGRITY_EDA_DIR` variable is set to point to the installation location. This variable is used by the Allegro schematic and layout editors to access the Sigrity 2019 installation when using Sigrity Aurora, Allegro IDA, Topology Explorer, or SystemSI products.

Using PCB Editor with the Sigrity Aurora License

To perform layout-level analysis and system-level analysis from within PCB Editor, perform these steps:

1. Launch PCB Editor
2. Choose the Sigrity Aurora license.
3. Select both the product options as shown.



4. Set *Use as Default, if needed*
5. Click *OK*.

PCB Editor is launched.

6. Open a design.

The Sigrity technology driven high-speed analysis and checking environment is now available that provides analysis and checking capability as workflows.

Performing Layout-Level Analysis in Allegro IDA

Workflows for the following six analyses types are available from PCB Editor:

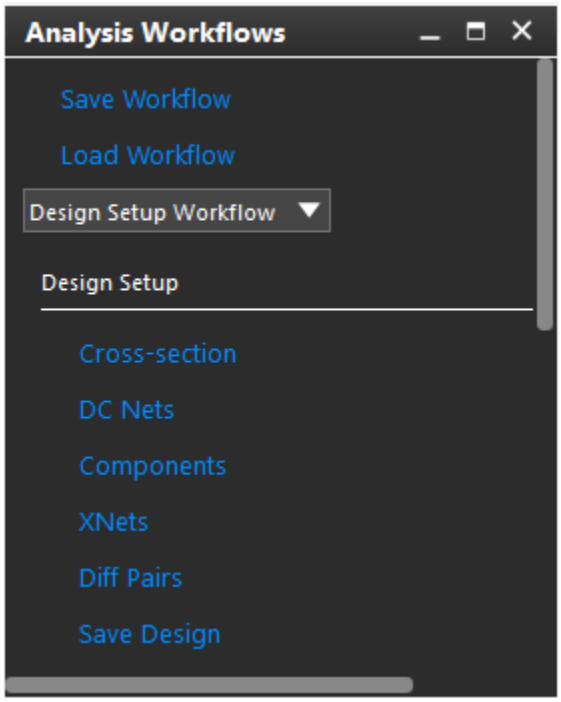
- Impedance
- Coupling
- Crosstalk
- Return Path
- Reflection
- IR Drop

Before running any of these analyses, use the Design Setup Workflow to set up and audit your design. It is important that the PCB design is correctly setup before the advanced IDA screens are run. In the Design Setup Workflow, you can set up the cross-section, DC nets, components, XNets, and differential pairs in the design. You can then save the design with the setup changes.

To perform layout-level analysis using Allegro IDA:

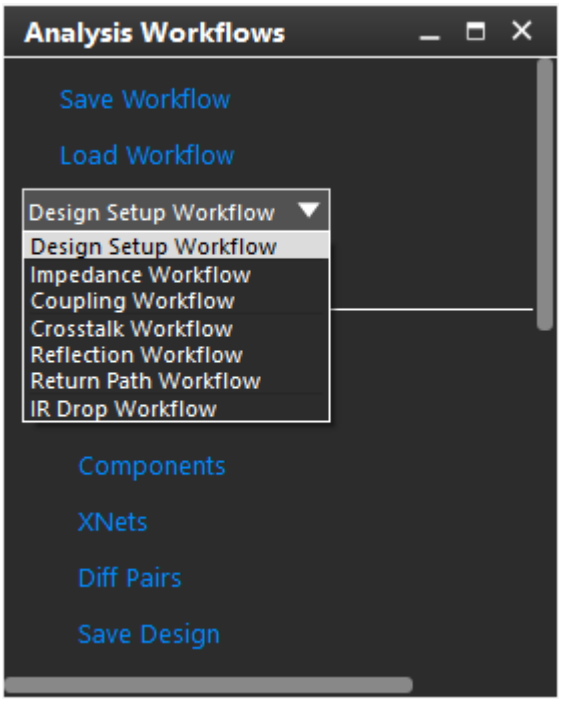
1. Choose *Analyze – Workflow Manager.*

The *Analysis Workflows* panel opens. These easy-to-use workflows are for first pass screens to check for potential SI and PI problems within the Allegro environment without the need of another tool.



You can dock this panel in any margin.

2. Open the *Design Setup Workflow* drop-down list.



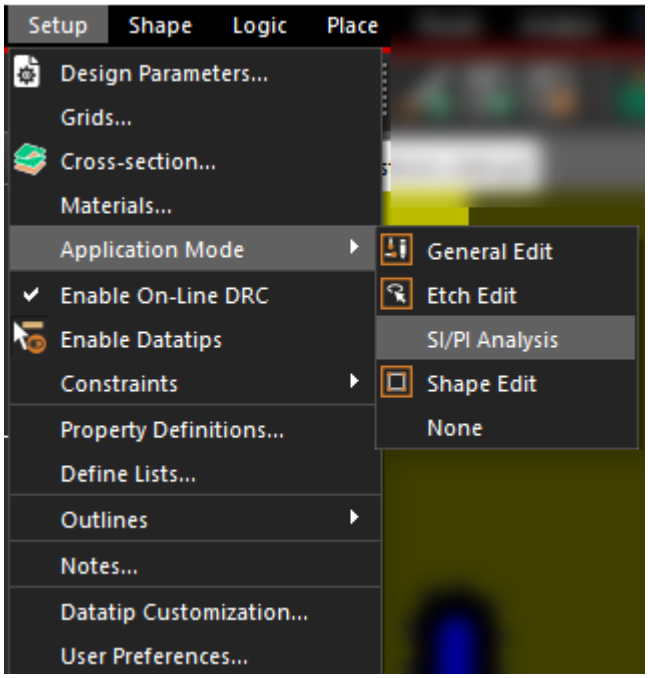
The options in the workflow pane change depending on the analysis selected.

To learn more about the workflows, see the *Allegro Integrated Analysis and Checking* chapter in the *Routing the Design* user guide.

Performing System-Level Analysis in TopXplorer

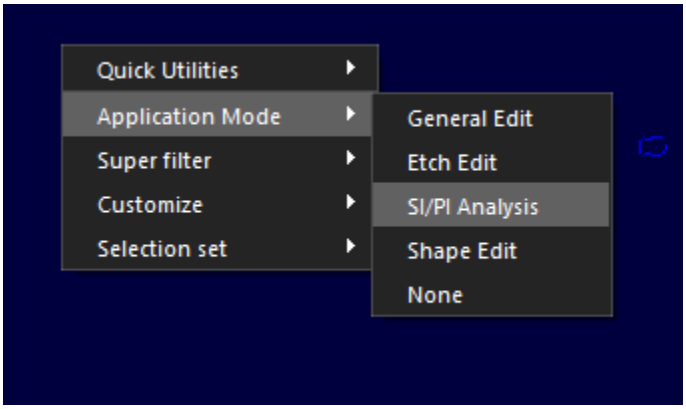
To export a topology for SI analysis into TopXplorer:

1. Choose *Setup – Application Mode – SI/PI Analysis*.

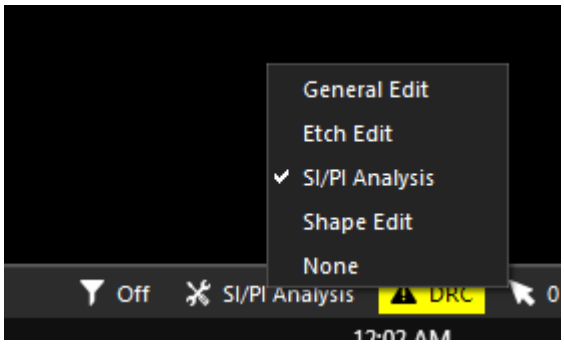


You can also right-click the layout canvas or from the status bar of the Sigrity Aurora window as shown.

Right-click on canvas

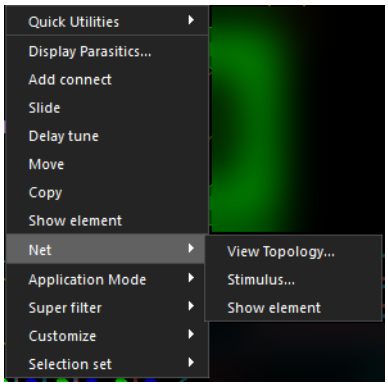


Status Bar

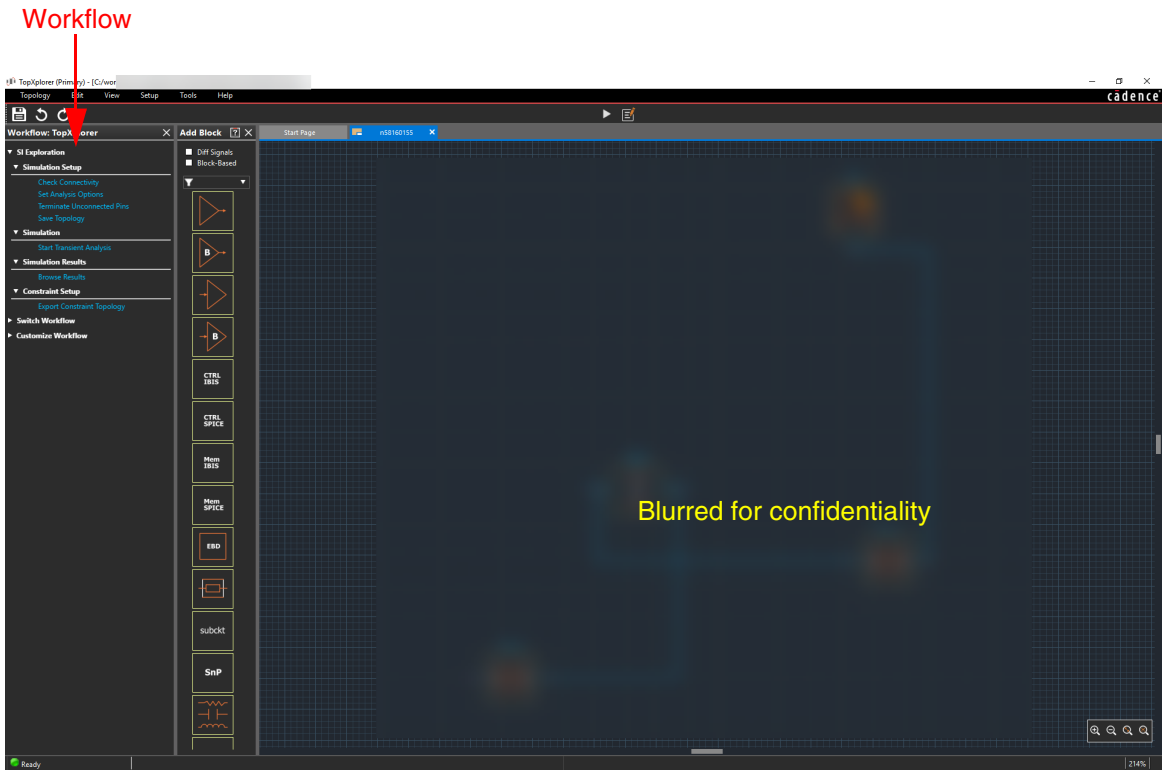


You can now extract the topology of any net in TopXplorer.

2. Right-click the net and choose *Net – View Topology*.



TopXplorer opens in the SI Exploration workflow with the topology displayed in the canvas:



The SI Exploration workflow is targeted for general-purpose signal integrity analysis, optionally including non-ideal power effects. To learn more about the SI Exploration workflow, see the *Using SI Exploration Workflow* chapter in the *Topology Explorer User Guide*.