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Allegro® X Layout Editors Known Problems and Solutions

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Contents

Known Problems and Solutions in Allegro X Layout Editors in Older Releases

This document describes the known problems and solutions for the Allegro layout editors, Allegro X PCB Editor and Allegro X Advanced Package Designer (APD). The known problems and solutions (KP&S) listed in this document will be reviewed at regular intervals and updated when new issues arises or an existing issue is fixed. Up-to-date known problems and solutions are also published on Cadence Online Support.

CCR 2859549: Segmentation fault shown on exiting Allegro X PCB Editor

Description: A segmentation fault might occur when exiting Allegro X PCB Editor on a Linux system with an Nvidia GPU.

Solution: Set the value of the variable, _GLX_VENDOR_LIBRARY_NAME to nvidia.

CCR 2631494: Allegro ECAD-MCAD Library Creator is not opening on Windows 11 systems

Description: When you try to open Allegro ECAD-MCAD Library Creator on a Windows 11 system, the following error message is flagged:

```
The code execution cannot proceed because MSVCE120.dll was not found.
Reinstalling the program may fix this problem.
```

Solution: This error message appears if Microsoft Visual C++ 2013 is not installed on the Windows 11 system. To resolve the error, download and install the Microsoft Visual C++ 2013 package from here.

CCR 2110045: Design Sync user interface does not read the location of the packaged folder

Description: To run design sync between OrCAD Capture schematic and PCB Editor layout, you need to select the packager (`*.pst`) files. The Design Sync dialog does not read the location of packaged folder and throws an error.

Solution: Select a *pst*.dat* file inside the folder to select the packaged folder.

CCR 2104972: Duplicate canvas displayed on loading a saved UI setting (View - UI Settings) on Linux

Description: On loading a saved UI setting from *View – UI Settings* menu, a duplicate window might be displayed intermittently on Linux due to issues with graphics/communication protocol primitives of the operating system.

Solution: Resize the application window.

CCR 2091550: Quickview does not show package symbols that are generated using releases earlier than 17.4-2019

Description: The graphics for packages generated using an earlier release are not shown in the Quickview window in release 17.4-2019 because the `.psm`(`.dra`) attachments needed to display a quick view has been enhanced in release 17.4-2019.

Solution: Save the symbol files (`.dra`) generated using an earlier release in release 17.4-2019 to view graphics in Quickview window

CCR 323684: Two RF components do not connect completely

Description: When snapping an RF component to connect to another RF component, it appears that these two RF components are already connected, but, actually they are not completely connected. This happens because two RF components are connected on their edges rather than on their pins, which are shifted a bit towards the inside of the edge. Due to the griddles characteristics of RF design, two RF components may not be connected firmly on their edges. They may be overlapped or not connected at all with a tiny gap between the edges.

Solution: A workaround solution for this problem is to use *RF-PCB – Edit – Snap* to reconnect them.

CCR 423324: Need to be able to manually trim RF Elements to maintain connectivity

Description: When importing ADS data, there can be connectivity errors due to resolution differences between Allegro and ADS databases. In ADS, seven decimal places are supported whereas in Allegro only four places are possible. This results in rounding off. An ability to check these connectivity issues using a 'trim' option to snap RF elements together is required. This task involves trimming back to remove an overlap, or, stretching to close an opening.

Solution: The workaround solution is to use *RF-PCB – Edit – Snap* to reconnect the RF circuit and shift the open gap/overlap to some single RF trace location, such as MLIN. Use *RF-PCB – Edit – Change* to stretch or reduce the length of the RF trace. Another possible solution to cover the gap is to add a short cline with the same width as the RF trace.

CCR 354941: Difficult to pick a cline point with the Edit - Vertex command on curved clines

Description: When modifying lines with rounded corners, and using *Edit - Vertex*, it is very difficult to select the rounded section of line. Several clicks are required to get the line to attach to the cursor. The line can be made of any number of classes (that is, Clines, Board Geometry, and so on.).

Solution: This is happening because the database unit is set to mm with high accuracy. This is causing an overflow when checking if a point is on the arc. Reduce the accuracy to correct the problem.

CCR 323953: DFA_UPDATE changes circular PLACE_BOUND into rectangles

Description: On running DFA_UPDATE on a part where the PLACE_BOUND is a circular shape, the DFA_BOUND_TOP is created as a rectangle.

Solution: Manually add the circular DFA_BOUND_TOP to the updated symbol. On running the DFA_UPDATE, Allegro PCB Editor tries to determine where the package side and end are. This decision is based on the longer/shorter dimensions of the package symbol. If Allegro PCB Editor cannot determine the side or end, such as a circular boundary, it uses the most conservative values and draws the DFA_BOUND as a rectangle around the extent of the circular boundary.

CCR 329469: The wrong mate is selected while manually routing or sliding a via on a differential pair.

Description: When sliding vias on a differential pair, and selecting one of the vias, the wrong mate via is selected. Selecting the other via, of the initial expected pair, the correct via mate is selected to slide.

It is similar to route from discrete pins of a differential pair and the wrong pin to route with is being selected. When starting to route at a pair of resistors in a differential pair, the pin one side of the resistors should route together. However, when pin one of the first resistor is picked then pin two of the second resistor is automatically chosen. If you cancel the route and start on either of the resistors' pin two side, then the subsequent resistor's pin two becomes active as expected.

Solution: Use *Single trace mode* to individually slide the vias or start the routing of the pairs. In either of these cases, when routing or sliding, right-click to select the *Single trace mode*.