cadence®

Allegro®
Layout-Driven RF Design User Guide

Product Version 23.1
September 2023

© 2023 Cadence Design Systems, Inc. All rights reserved.
Portions © Apache Software Foundation, Sun Microsystems, Free Software Foundation, Inc., Regents of the University of California, Massachusetts Institute of Technology, University of Florida. Used by permission. Printed in the United States of America.

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Apache Software Foundation, 1901 Munsey Drive Forest Hill, MD 21050, USA © 2000-2005, Apache Software Foundation. Sun Microsystems, 4150 Network Circle, Santa Clara, CA 95054 USA © 1994-2007, Sun Microsystems, Inc. Free Software Foundation, 59 Temple Place, Suite 330, Boston, MA 02111-1307 USA © 1989, 1991, Free Software Foundation, Inc. Regents of the University of California, Sun Microsystems, Inc., Scriptics Corporation, © 2001, Regents of the University of California. Daniel Stenberg, © 1996 - 2006, Daniel Stenberg. UMFPACK © 2005, Timothy A. Davis, University of Florida, (davis@cise.ulf.edu). Ken Martin, Will Schroeder, Bill Lorensen © 1993-2002, Ken Martin, Will Schroeder, Bill Lorensen. Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, Massachusetts, USA © 2003, the Board of Trustees of Massachusetts Institute of Technology. All rights reserved.

Trademarks: Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522.

Open SystemC, Open SystemC Initiative, OSCI, SystemC, and SystemC Initiative are trademarks or registered trademarks of Open SystemC Initiative, Inc. in the United States and other countries and are used with permission.

Restricted Permission: This publication is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this publication, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this publication subject to the following conditions:

1. The publication may be used only in accordance with a written agreement between Cadence and its customer.
2. The publication may not be modified in any way.
3. Any authorized copy of the publication or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
4. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

Disclaimer: Information in this publication is subject to change without notice and does not represent a commitment on the part of Cadence. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information.

Cadence is committed to using respectful language in our code and communications. We are also active in the removal and/or replacement of inappropriate language from existing content. This product documentation may however contain material that is no longer considered appropriate but still reflects long-standing industry terminology. Such content will be addressed at a time when the related software can be updated without end-user impact.

Restricted Rights: Use, duplication, or disclosure by the Government is subject to restrictions as set forth

in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor.

Contents

© 2023 All Rights Reserved.

© 2023 All Rights Reserved.

Preface

About This User Guide

The *Layout-Driven RF Design User Guide:*

- Explains how to use the RF PCB Import feature to import radio-frequency (RF) circuitry changes in the layout into the Design Entry HDL schematic
- Lists the different ways of starting RF PCB Import
- Describes the user interface of RF PCB Import
- Lists the key limitations in the current implementation of RF PCB Import

Before you use the RF PCB Import feature, you should be familiar with using Design Entry HDL and PCB Editor.

Finding Information in This User Guide

This user guide covers the following topics:

See...	For Information About...
Importing RF Circuitry Changes into the Schematic	Explains how to import RF circuitry changes in the layout into the Design Entry HDL schematic
Limitations of RF PCB Import	Lists the key limitations in the current implementation of RF PCB Import

Related Documentation

You can also refer to the following documentation to know more about related tools and methodologies:

© 2023 All Rights Reserved.

Design Entry HDL

- For information on the new features available in the current release, see *Allegro Design Entry HDL: What's New in Release 17.0*.
- For learning Design Entry HDL, see *Allegro Design Entry HDL Tutorial*.

PCB Editor

- For information on the new features available in the current release, see *Allegro PCB Editor: What's New in Release 17.0*.

Related Tools and Flows

- For information on various PCB design working environments, such as a team of designers working on a Design Entry HDL project, implementing FPGAs in designs, working with high-speed constraints, importing IFF files for radio-frequency designs, and reusing existing modules, see *Allegro PCB Design Flows*.
- For learning how to create new Design Entry HDL projects and configure various settings for them, see *Project Manager User Guide*.
- For learning how to use the Design Entry HDL utilities, such as CRefer, Archiver, and BOM, see *Design Entry HDL Utilities User Guide*.
- To know more about RF PCB, see *Allegro PCB Editor User Guide: Working with RF PCB*.
- To know more about the component libraries delivered with Allegro RF PCB, see *Allegro RF PCB Library Reference*.

© 2023 All Rights Reserved.

Typographic and Syntax Conventions

This list describes the syntax conventions used for this user guide:

`literal`	Nonitalic words indicate keywords that you must enter literally. These keywords represent command (function, routine) or option names.
`argument`	Words in italics indicate user-defined arguments for which you must substitute a name or a value.
|	Vertical bars (OR-bars) separate possible choices for a single argument. They take precedence over any other character.
`[ ]`	Brackets denote optional arguments. When used with OR-bars, they enclose a list of choices. You can choose one argument from the list.
`{ }`	Braces are used with OR-bars and enclose a list of choices. You must choose one argument from the list.

© 2023 All Rights Reserved.

© 2023 All Rights Reserved.

1

Importing RF Circuitry Changes into the Schematic

Typically, the RF circuitry in a design undergoes frequent changes in the layout. Manually updating the schematic with the RF circuitry changes in the layout is tedious and error-prone. In the Cadence Board Design Solution, a layout-driven RF PCB Import flow is integrated with the traditional Import Physical flow to enable you to synchronize the RF circuitry in the schematic with that in the layout.

© 2023 All Rights Reserved.

Extracting RF Circuitry as RF Topologies

In RF PCB import, RF circuitry is extracted from the schematic and the layout as RF topologies. The primary reason for extracting the RF circuitry in modular parts is to ensure that the schematic drawn for the changed RF circuitry is readable. For each changed RF topology, a separate schematic is drawn on one or more sheets.

Note: For circuitry that does not belong to any RF topology, RF PCB import does not make any update in the schematic.

Each RF topology is a network of directly connected RF components and includes discrete components that are directly connected to the network.

RF PCB Import identifies the constituent components of an RF topology in the following way:

1. An RF component is included in an RF topology by default.

   Note: An RF component is identified by the `ISRFELEMENT` property in the `symbol.css` file.

   Note: Cadence provides standard RF components in the `rfcomp` and `rfcomp_mm` libraries at <*`your_install_directory`*>`\share\library`.

2. Two RF components directly connected belong to the same RF topology.

   Note: A discrete or non-RF component is not considered part of an RF topology. If the topology terminates at such a component, the connection is considered part of the topology.

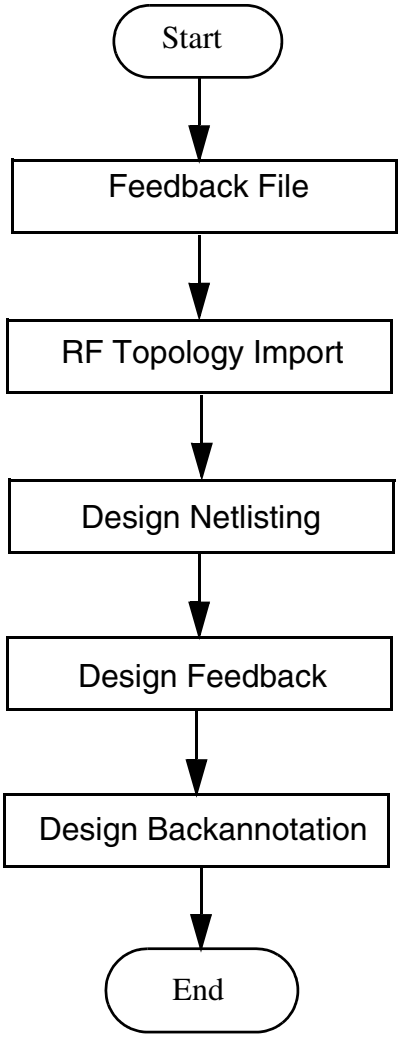
3. If a discrete component is directly connected through a non-DC net or a non-interface net to a component in an RF topology, it is made part of the same RF topology.

© 2023 All Rights Reserved.

RF PCB Import Flow

The following flowchart depicts the integration of the RF PCB Import flow with the traditional backannotation flow:

Figure 1-1



The RF PCB Import Flow:

- The RF PCB Import flow starts from Design Sync's Import Physical dialog.
- The RF circuitry in the schematic is compared with the layout and changes identified bring the schematic in sync with the layout.
- Schematic cleanup takes place to incorporate the changes in the RF circuitry.

© 2023 All Rights Reserved.

- The schematic is updated automatically and marker file is generated. to help navigate to the changes/updates in the schematic. You can load the marker file in DE-HDL and see all the changes listed in the marker dialog. On clicking a specific change, the relevant page is displayed and the relevant area is zoomed.
- RF PCB Import automatically detects which portion of the RF Topology lies in which block and for each block finds the first page that contains the connectivity to that RF Topology. The new components of this RF Topology assigned to the current block land on that first page.
- The new RF components are added outside the page border. In case there is no page border, the extent of the existing schematic on that page is automatically computed and the schematic is placed beyond that extent. In case the page border is present but the `cref.dat` file is not specified or does not have the drawing information for that page border, the drawing area of the page border is automatically computed and the schematic of the new RF components is placed beyond the computed area. The generated schematic for new components of each RF Topology are placed on the top-right side of the page border (or drawing extent in case page border is not used). The newly generated schematic is placed one below the other, starting from the top-right.
- When the RF PCB Import flow is complete, load the `rfpcbimport.mkr` marker file. Net names that need connection are made visible and the regions which involve a net connection are highlighted.

Note: In case of a replicated block, updates to RF Topology is not allowed in the backend.

Note: If an RF Topology spans across hierarchy (contains an interface net), the import flow determines which portion of the RF Topology lies in which block and updates the schematic in individual blocks for that RF Topology. For new RF components, if there is any ambiguity as to which block it should go to, it is placed at the top-most block that the interface net goes to.

Note: If an RF component is deleted in the layout, it is deleted from the schematic as well and minimal schematic cleanup takes place.

The RF PCB Import flow takes care of only connectivity updates and relies on the traditional Import Physical flow to backannotate the schematic changes. If there are no connectivity changes detected, the schematic will not be changed by RF PCB Import. For a full Import Physical, you need to select netlisting and backannotation. This will update the schematic with the property changes coming from the layout.

© 2023 All Rights Reserved.

Feedback File Generation

The backannotation flow begins with the generation of feedback files. If RF circuitry is found in the layout, the `rftopologyview.dat` file is generated in this step along with other view files generated in the traditional backannotation process. The `rftopologyview.dat` file is created in the `packaged` folder of the root block.

Extracting RF Topologies from the Layout

RF PCB Import uses the `rftopologyview.dat` file to extract information about the RF topologies in the layout.

The `rftopologyview.dat` file stores the following information about each RF topology in the layout:

- Component details, such as parameters and placement and orientation information
- Connectivity information

Extracting RF Topologies from the Schematic

RF PCB Import uses Packager data to extract information about the RF topologies in the schematic.

Important

The RF PCB Import flow requires the Packager data to be more recent than the schematic for proper extraction of RF topologies from the schematic. In case the Packager data is old, the RF PCB Import flow exits and the schematic needs to be exported to generate the latest Packager data.

RF Topology Import

After the RF topologies are extracted from the layout and the schematic, RF PCB Import compares the RF topologies in the two sources to identify the differences that will require the schematic to be updated and the type of update required.

Important

For all RF topologies, the layout is considered the master.

RF PCB Import identifies four types of differences between the schematic and the layout as listed in column 1 of Table 1-1 on page 16. However, because the RF PCB Import flow takes

© 2023 All Rights Reserved.

care of only connectivity updates and relies on the traditional Import Physical flow to backannotate the schematic changes, the schematic is updated with all types of changes only if connectivity changes exist.

In case of connectivity changes, RF PCB Import cleans up the impacted sheets of the schematic. The following table lists each type of changes identified in RF PCB import and whether schematic clean up is required for that type of change:

Table 1-1 Types of Differences and Updates

Type of Change	Schematic Clean up
Change in property attributes (RF parameters)	No
New properties	No
New RF component and connection	Yes
Change in connectivity	Yes
Deletion of an RF component	Yes

Changes in Property Attributes (RF Parameters)

Changes in property attributes are identified for backannotation. The schematic is not redrawn and the property attribute changes are updated in the schematic as part of the traditional Import Physical flow.

New Properties

New properties are identified for backannotation. The schematic is not redrawn to accommodate new properties. The properties are added in the schematic as part of the traditional Import Physical flow.

New RF Components

Updating the schematic to include new components involves connectivity changes. Therefore, if RF PCB Import identifies new components in the layout, it adds the new RF components outside the page border of the corresponding page. The original connectivity may change, but all existing components stay at their original positions.

© 2023 All Rights Reserved.

Important

RF PCB Import does not support addition of non-RF components in the layout, which are not present in the schematic. In such a case, you need to add the component in the schematic and export the schematic before running RF PCB Import or use the Design Association flow to update the schematic.

Important

RF PCB Import fails if it finds unpackaged or unplaced RF components in the layout.

Changes in Connections

Changes in connections are often made in the layout for routing. If RF PCB Import identifies changes in connections, it cleans up the schematic to reflect the connectivity changes.

RF Schematic Cleanup

After RF topology changes are identified for backannotation, RF sheets are updated for RF topologies that have undergone connectivity changes:

- New connections because of new components getting added
- Modified connections
- Net name changes

New components are added beyond the page border.

Important

If there is an entirely new RF topology, it is created and added outside of the page border at the topmost level page.

Schematic Cleanup Rules

The following rules are applied for schematic cleanup:

Hierarchical Designs

- If RF PCB Import identifies changes in a read-only block, it exits the backannotation process.

© 2023 All Rights Reserved.

- If RF PCB Import identifies changes in a replicated block, it exits the backannotation process. This is because it is unable to identify the changes on replicated blocks.

Important

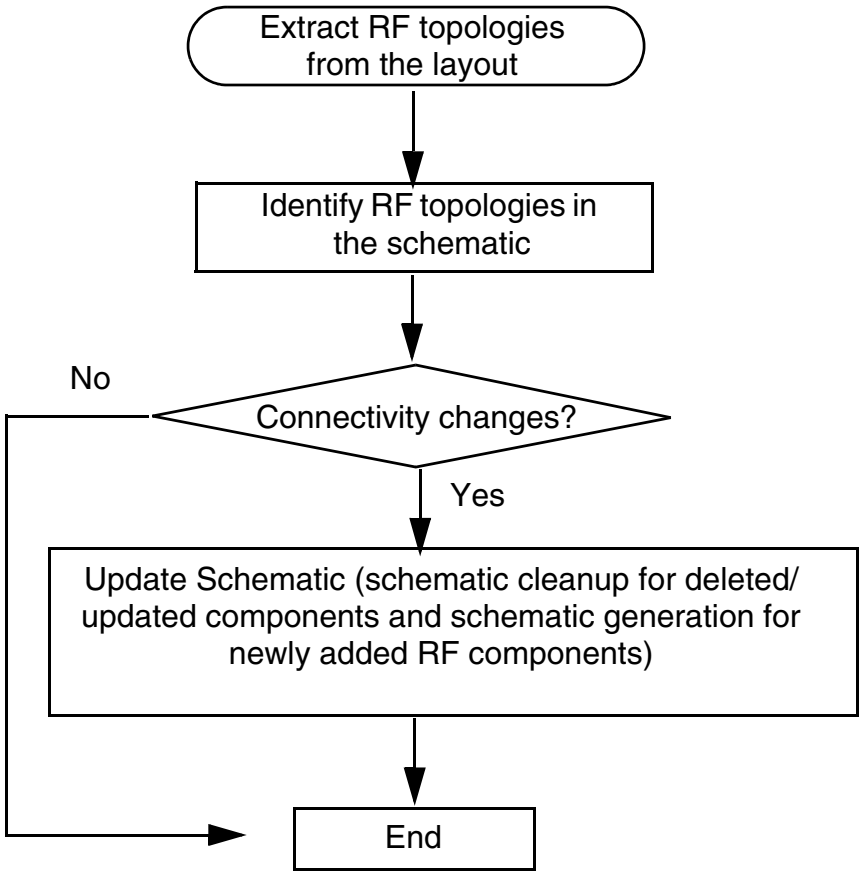
To ensure that RF backannotation works properly, Allegro PCB Editor disallows editing replicated blocks.

- If an RF component is added in a block and its connectivity is limited within that block, RF PCB Import updates the schematic of only that block.
- If an RF component is added and its connectivity spans across a block, the new RF component is added at the topmost level page.
- If an interface net of an RF topology block undergoes changes, RF PCB Import updates the block by breaking the interface nets and adding the new interface nets as global nets. In such a scenario, you need to manually move new RF components from the top to appropriate blocks and modify the global nets according to the intent of the design.

The following figure shows how layout-driven RF backannotation works.

© 2023 All Rights Reserved.

Figure 1-2



© 2023
All Rights Reserved.

Preparing for RF PCB Import

Before you run RF PCB Import, ensure the following:

- The design is packaged

  RF PCB Import uses Packager data to extract information about the RF topologies in the schematic. Therefore, it is imperative that the schematic and layout are in sync. Packaging the design (running Export Physical without updating the board) before running RF PCB Import ensures that your schematic and package are in sync.

- `SIG_NAME` values are assigned to all interface nets in your design

  If the design being updated using RF PCB import has unnamed nets, the Packager flow assigns default names, which might cause rip-ups in the layout. To avoid this problem, it is recommended that you assign `SIG_NAME` values to all interface nets in your design.

Running RF PCB Import

You can run RF PCB Import in the following ways:

- From Project Manager or Design Entry HDL
- From the Command Line

From Project Manager or Design Entry HDL

To import RF circuitry changes into a schematic, follow these steps:

1. Open the schematic to be updated with RF circuitry changes in the layout.
2. Launch Import Physical.

   You can launch the Import Physical utility in the following ways:

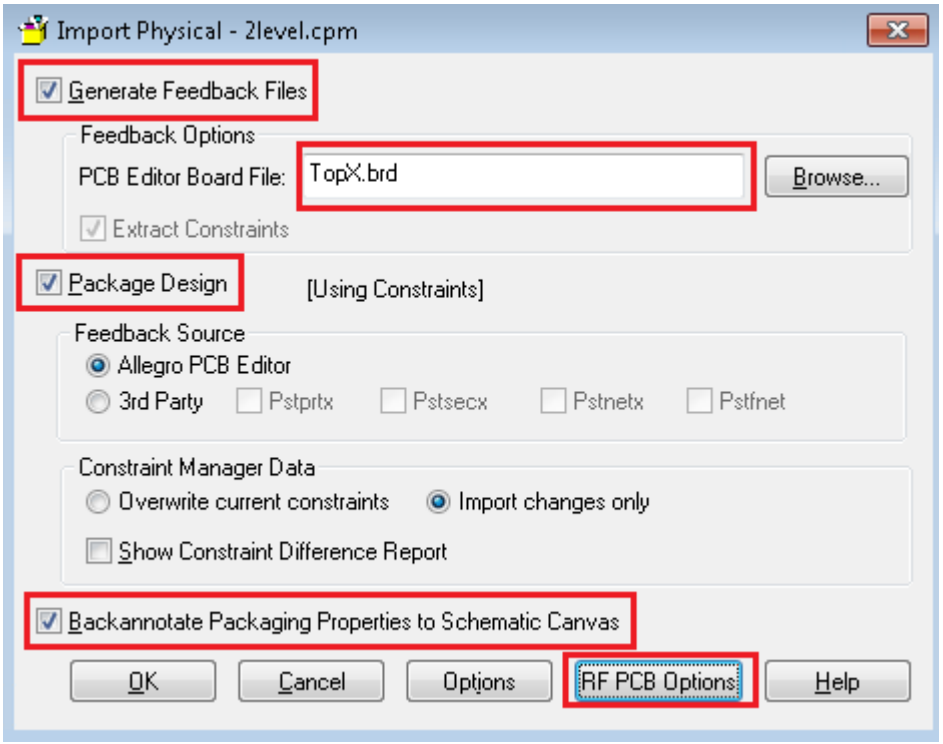
   a. From Project Manager, click the *Design Sync* icon *and choose Import Physical.*

   b. From Project Manager, choose *Tools – Design Sync – Import Physical*.

   c. From DE-HDL, choose *File – Import Physical*.

© 2023 All Rights Reserved.

Figure 1-3

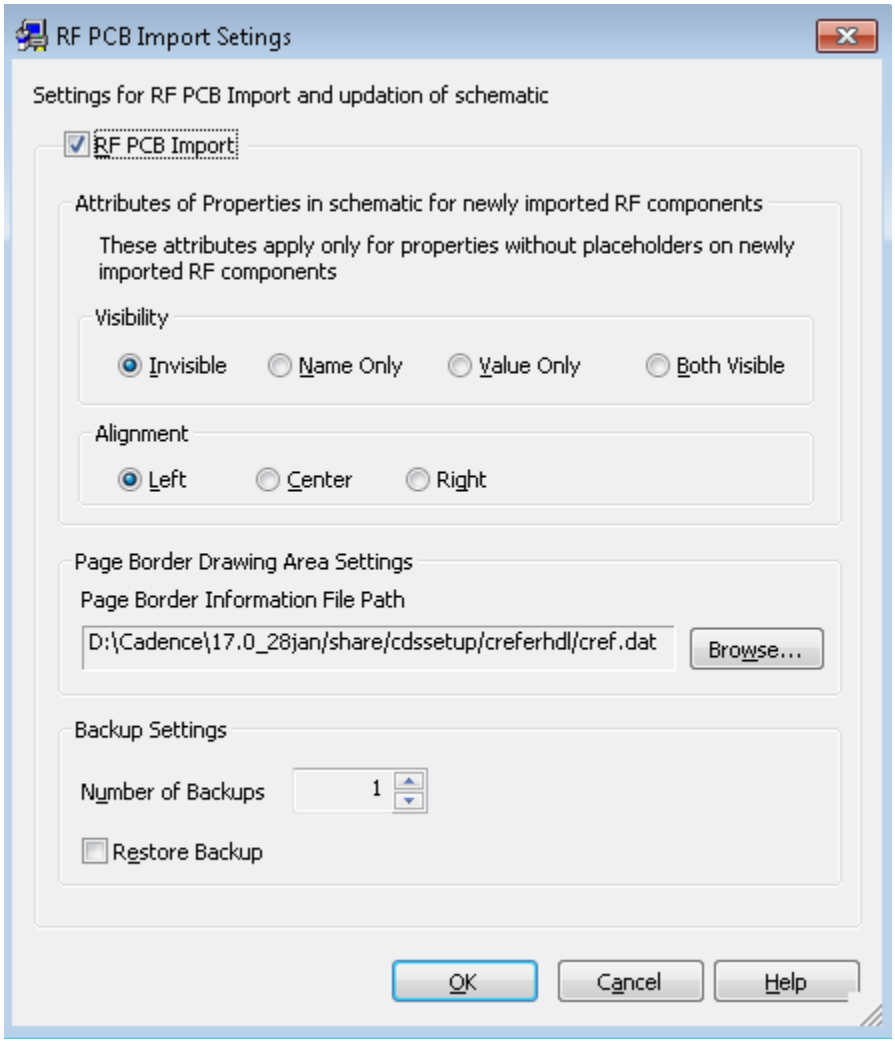


3. Select the *Generate Feedback Files* check box.
4. Select the *Package Design* check box.
5. Specify the name of the board file in the *PCB Editor Board File* field in the *Generate Feedback Files* group box.
6. Select the *Backannotate Packaging Properties to Schematic Canvas* check box.
7. Click the *RF PCB Options* button.

   The RF PCB Import Settings Dialog Box is displayed.

© 2023
All Rights Reserved.

Figure 1-4



8. Select the *RF PCB Import* check box.

Important

If you do not select the *RF PCB Import* check box and continue with Import Physical, a warning is displayed. If you ignore the warning, the schematic is backannotated without RF circuitry changes.

9. Browse to the path of the `cref.dat` file, if required. The drawing area of a page border is determined from the `cref.dat` file.

10. Select the *Restore Backup* checkbox to restore the last backup automatically. The `.csb` file of the affected pages is backed up as `.csb, 1`. Restoring essentially means replacing the current `.csb` with the corresponding `.csb, 1` and removing the corresponding `.csa` file.

© 2023 All Rights Reserved.

Note: The maximum backup is 5.

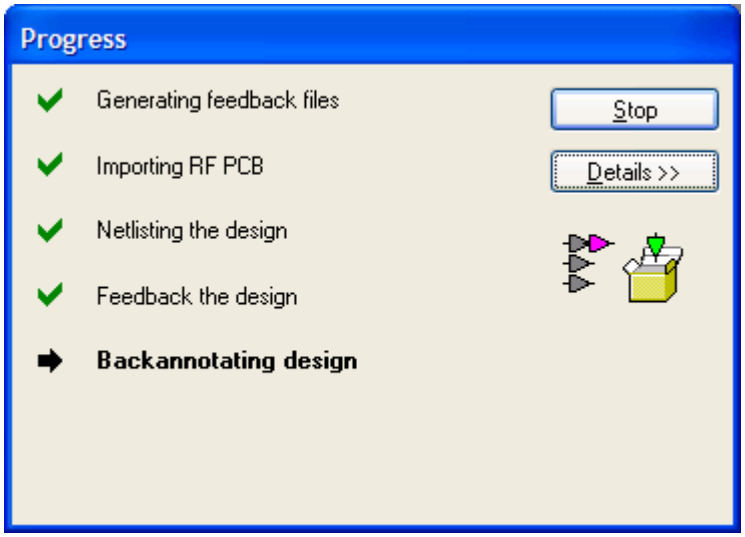
11. Click *OK*.

This closes the RF PCB Import Settings dialog box.

12. Click *OK*.

RF PCB import starts.

Figure 1-5



From the Command Line

To run RF PCB Import from the command line:

➤ Type `rfpcbtopologyimport -proj` *`proj_file`* `-product` *`license_string`* and press Enter.

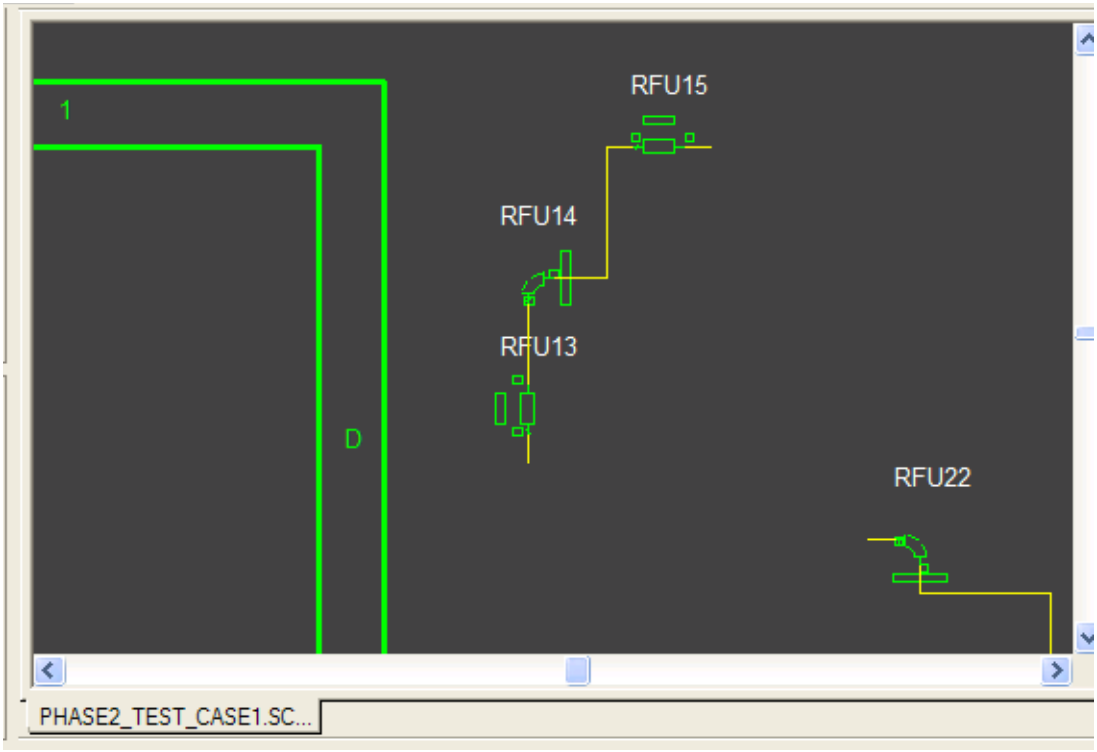
Viewing an RF Design in Schematic

The schematic is automatically updated and marker file are generated. Marker files aid in navigating to the changed portions of the design after the import operation. RF PCB Import detects which portion of the RF Topology lies in which block and for each block finds the first page that contains the connectivity to that RF Topology. The new components of this RF Topology assigned to the current block will land on that first page.

© 2023 All Rights Reserved.

The new RF components are added outside the page border as shown in Figure 1-6 on page 24. In case there is no page border, the extent of the existing schematic on that page will be automatically computed and the schematic will be placed beyond that extent

Figure 1-6

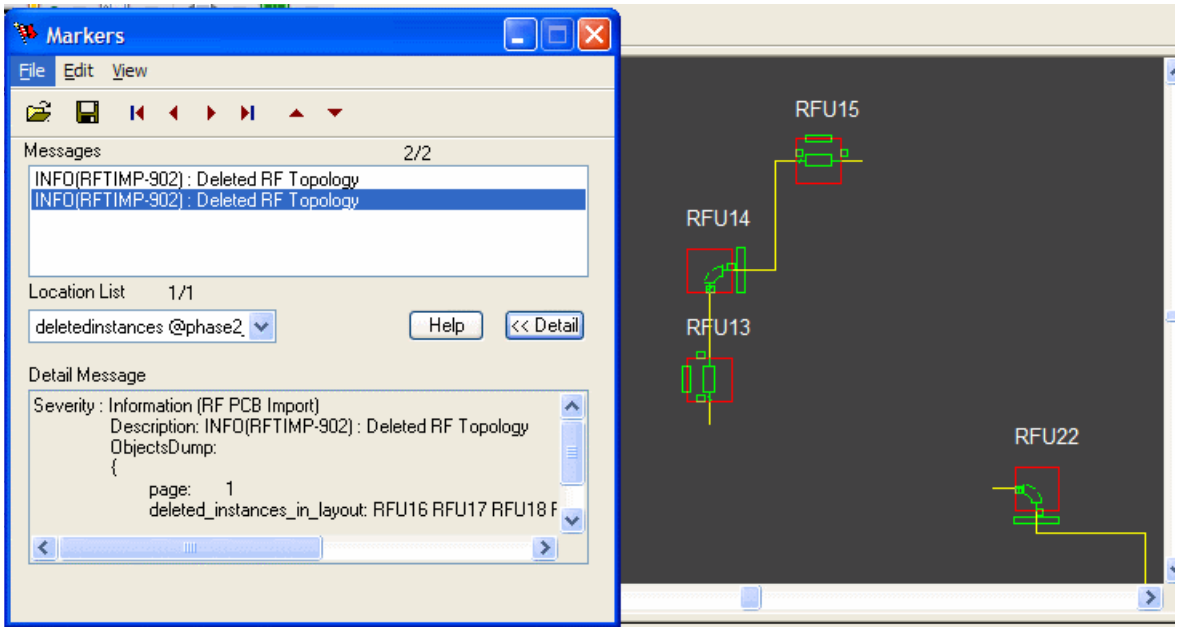


You load the marker file to navigate to the affected parts of the design. For each portion of a specific RF Topology on a page, there is an entry in the marker file.

➡ Load the marker file, `rfpcbimport.mkr` file, from the *Tools – Markers – RF PCB Import* menu.

© 2023 All Rights Reserved.

Figure 1-7



Location list in the marker file contains the list of component for that portion of the RF Topology. If you select a component in the list, it is zoomed in the schematic. The message in the *Detail Message* section of the dialog box displays all the relevant details. There are separate entries for net names which need changes, RF components or topology that were deleted in the layout.

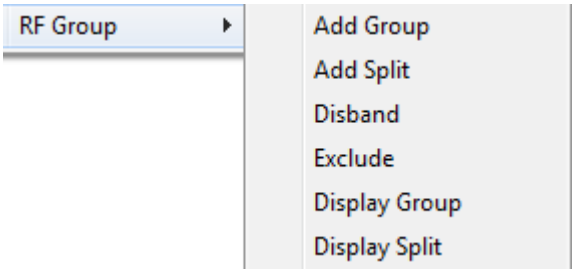
Similarly, for each connection update or new connection with already existing components, there are separate messages and the location list displays the pointer to connection points. Selecting a pointer zooms to the relevant stub of the net. This helps in navigating to the connections that were updated because of the RF PCB Import.

AutoPlace Enhancements in De-HDL

Autoplace is a very important step for RF layout creation after the schematic is transferred to layout. The system will automatically create groups based on connectivity during the autoplace process. This will result in many groups in autoplace and it's difficult to find the proper groups during autoplace. There are some commands added in DE-HDL to support

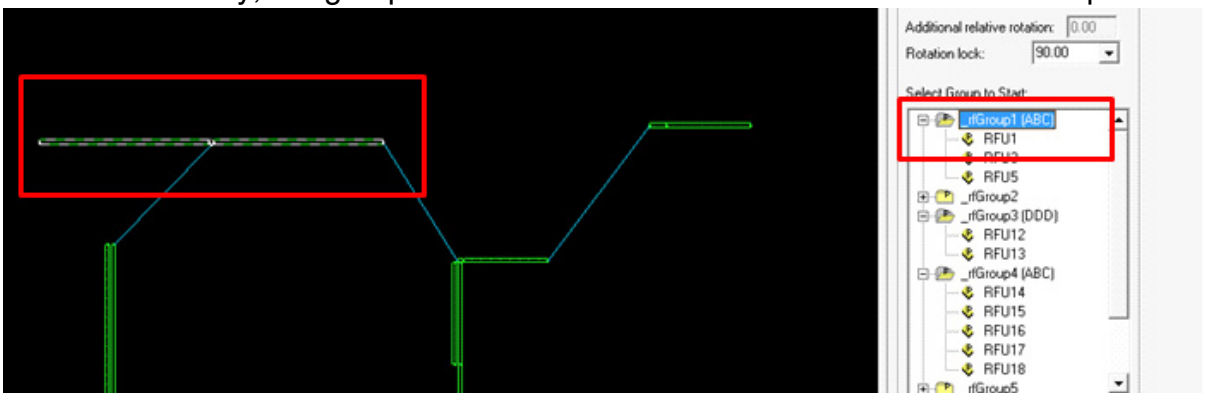
© 2023 All Rights Reserved.

grouping. The groups in autoplace can be controlled using these commands. All these commands are available when the pre select mode is enabled in DE-HDL.



- Using the Add Group option enables you to attach a property (RFGROUP) to the selected components.
- Using the Add Split option enables you to attach a property (RFSPLIT) to the wires selected. If a wire is attached with this property, then the logic group is broken where the property is added (one big logic group is split into two logic groups).
- Using the Disband option enables you to remove the RFGROUP property from each RF component for the specific group.
- Using Exclude enables you to remove the property for selected objects (RFGROUP for RF components or RFSPLIT for wires).
- Using the Display Group option enables you to highlight/report the RF components within a specific group.
- Using the Display Split option enables you to highlight all wires with the RFSPLIT property.

If you transfer the schematic to layout and launch Autoplace, you will see the groups are classified differently, the group names added in schematic are reflected in autoplace.

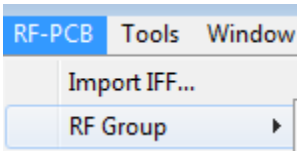


You can use the Group filter to easily find/locate some specific groups to perform autoplace.

© 2023 All Rights Reserved.

RF Grouping in Front End

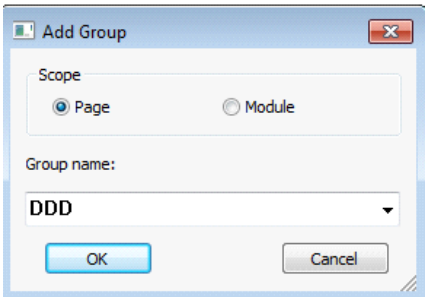
To use the grouping functionality in schematic, click Tools – Options and check the “Enable Pre-select Mode”, you will see the RF PCB menu as following:



Note: If you check “Enable Windows Mode” then Import IFF… menu is not available in the RF-PCB menu. You can find it from File– Import–Import IFF…– RF-PCB.

Add Group

To use this command, first select some RF components (or non-RF components) and then click RF-PCB– RF Group – Add Group, the following dialog appears:



You can enter a new group name or select an existing group from the drop-down list. If the existing group includes elements outside the current page, you need to select Module radio option.

Note: You can only select the components in current page to add to a group.

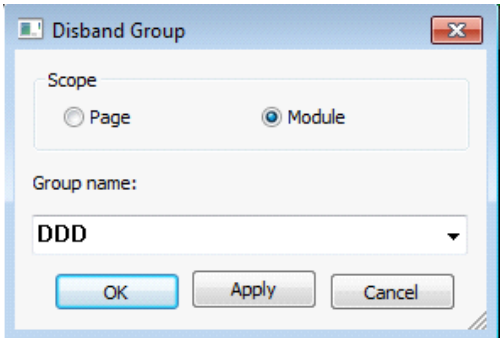
Add Split

Select a wire or multiple wires and then click RF-PCB– RF Group– Add Split, the RFSPLIT property is attached to the wires selected. You cannot select wires crossing pages to add split.This means that you can only select the wires in the current page for this command.

Disband

© 2023 All Rights Reserved.

Click RF-PCB– RF Group – Disband, the following dialog box appears:



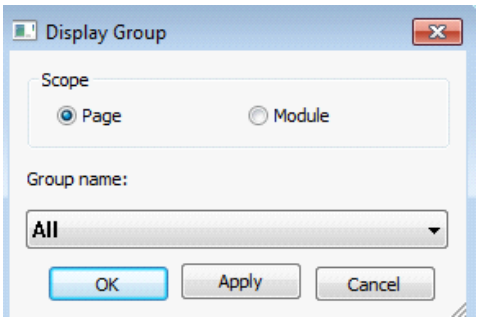
All available groups are listed in the drop-down list. Select a group and select the proper scope and then apply Disband Group. The RFGROUP property will be removed from each component of the group.

Exclude

Select one or more components with the RFGROUP property attached or one or more wires with the RFSPLIT attached and then click RF-PCB– RF Group – Exclude, the property is removed for the selected objects. This command also works for the current page objects only.

Display Group

Click RF-PCB– RF Group– Display Group, the following dialog box appears:



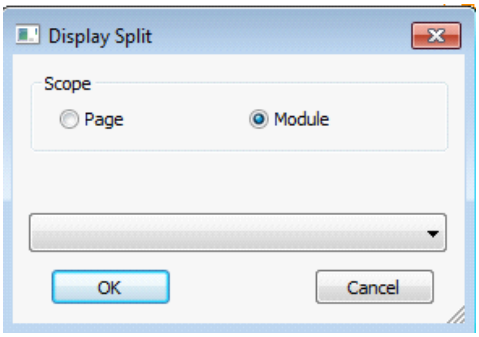
You can display one group from the drop-down list or all groups by selecting *All* from the drop-down list. To display a group includes elements in other pages, you can select Module radio option.

Click *Apply* or *OK*, all components in the selected groups are listed in the command line. If the module option is selected then the components of the selected groups are highlighted in current page.

© 2023 All Rights Reserved.

Display Split

Click RF-PCB->RF Group->Display Split, the following dialog box appears:



Click *OK* to highlight the wires with RFSPLIT property in the current page. To obtain the description of each wire with RFSPLIT property in the current page, select the Page option, to obtain the description of each wire with RFSPLIT property in the complete design, select the Module option. The command line will show the following information:

```
Page 1 contains 1 wire(s) with RFSPLIT property.
(2750:17503500:1750)
Page 2 contains 1 wire(s) with RFSPLIT property.
(1050:17501800:1750)
```

Automatic Block Assignment Rules for an RF Topology

An RF Topology from the layout can potentially span across hierarchies. For this, all the components in the RF Topology are scanned and the following steps are performed to assign components to relevant blocks:

- For each net in the RF Topology coming from the layout, it is determined whether there is an interface net in the front-end.
- For all RF components in the RF Topology, it is determined if they already exist in the front-end. Each RF component is assigned to the block where it was found.
- Identify all the RF components in the RF Topology for which blocks have not been assigned. For any such component, its non-interface connections to other RF components that have been assigned to blocks are identified. If connections to only one block are found, the component is assigned to the same block. Else, it is ignored.
- All the RF components which are not assigned to any block are assigned to the top block. For all such components, the nets that must now be interfaces are made global nets and you need to edit them while placing the new RF Schematic at the appropriate location.

© 2023 All Rights Reserved.

Markers are generated to highlight those portions of new RF Schematic for which block placement are to be determined.

© 2023 All Rights Reserved.

RF PCB Import Settings Dialog Box

The RF Topology Import Settings dialog box appears when you click the *RF PCB Options* button in the Import Physical dialog box.

The following information is displayed in the RF PCB Import Settings dialog box:

Option	Description
RF PCB Import check box	Enables RF PCB Import. If the RF PCB Import check box is not selected, the traditional Import Physical flow is run. You can also enable RF PCB Import by setting the value of the `RF_PCB_IMPORT` directive in the `START_RFPCB` section of the `.cpm` file.
Attributes of Properties in schematic for newly imported RF components	Specifies the visibility and alignment settings of newly imported properties
Visibility	
Invisible	
Name Only	
Value Only	
Both Visible	
Alignment	
Left	
Center	
Right	
Page Border Drawing Area Settings	
Page Border Information File Path	Enables you to browse to the `cref.dat` file to provide information about the drawing area of the page border.

© 2023 All Rights Reserved.

Option	Description
Backup Settings	
Number of Backups	Enables you to specify the number of backups alive at any point. The default number is 1. You can also set the number of backup by setting the `RESTORE_BACKUP` directive in the `.cpm` file.
Restore Backup checkbox	Restores data from the previous run of RF import. During the import operation, ensure that this option is deselected,

Archiving an RF Design

When you archive an RF design, you might find that the archived library does not include the cells of components added in the layout. In such a case, you need to manually copy the required cells in the archived library.

© 2023 All Rights Reserved.

2

Limitations of RF PCB Import

This appendix describes the limitations in the current implementation of the RF PCB Import feature.

Changes in Read-Only Blocks in the Layout Cause Failure of RF PCB Import

RF PCB Import fails upon commit if it identifies changes in read-only blocks in the layout.

Changes in Replicated Blocks in the Layout Cause Failure of RF PCB Import

RF PCB Import fails if it identifies changes in replicated blocks in the layout.

Note: To ensure that RF backannotation works properly, Allegro PCB Editor disallows editing replicated blocks.

Non-RF Components Added in the Layout Cause Failure of RF PCB Import

RF PCB Import fails if it identifies a non-RF component in the layout that does not exist in the schematic. In such a case, you need to add the component in the schematic through the Design Association flow and package the design before running RF PCB Import.

© 2023 All Rights Reserved.

Constraints Need Manual Updating If Components Are Moved to New Pages

If components are moved to new pages during RF PCB Import, constraints that involve canonical paths are lost. In such a case, you need to manually add the constraints after import.

Vectored Signals not Supported in RF Topology

RF PCB Import does not support vectored signals. It assigns signal names on the pins with the correct bits.

Page Border Specified in RF PCB Import Setup Not Added If the Page Border File Is Missing or Incorrect

Newly generated RF sheets might not have a page border even if you selected the *Add Page Border for New RF Sheet* check box in RF PCB Import setup. To avoid this problem, ensure that the `cref.dat` file you specify in setup exists in the specified location, has read permissions, and has the required information about the drawing area.

Hierarchy View in the Design Entry HDL Viewers Does Not Display the Module Order of Temporary Views

In the Design Entry HDL viewers launched in the preview, the module order displayed in the Hierarchy Viewer pane is same as that of the original schematic. Therefore, you cannot use t

© 2023 All Rights Reserved.

Index

Symbols

B

C

I

K

L

N

O

R

V

© 2023 All Rights Reserved.