cadence®

PSpice A/D Modeling Applications Reference Guide

Product Version 23.1
September 2023

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Contents

1

Introducing Modeling Applications

Modeling applications enhance the usability of Capture-PSpice solution for analog and digital designs by enabling designers to quickly develop models during the schematic entry phase. These applications provide an easy and well-integrated way to model various types of devices at the schematic entry stage. You can generate a model and place schematic components associated with the newly created model, without having to get out of the schematic entry interface of OrCAD Capture. These modeling applications also take care of simulation profile configuration and automatically include newly created libraries in the simulation profile to ensure successful simulation.

For example, if you want to simulate a capacitor with a parasitic, you can directly specify the electrical information from the datasheet to generate the required model and place it on the schematic. This is different from the traditional method of searching a model on the web, downloading it, generating the corresponding logical symbol, and then using it in simulation.

The modeling applications are simulator or project specific. The following applications are accessible only from a project enabled for the PSpice A/D simulation.

Device Category	Device Name and the Corresponding Modeling Application
MOSFET	
	Power MOSFET
Circuit Protection	
	Transient Voltage Suppressors (TVS)
Diodes	
	Zener Diode
	Light-Emitting Diode (LED)
	Power Diode
Passives	
	Capacitor

	Inductor
Sources	
	Independent Sources
	PWL Sources
	Digital Pulse
	Digital Stimulus
System Modules	
	Switch
	Transformer
	Voltage Controlled Oscillators (VCO)
Digital	
	Gates Buffer/Inverter, XOR/XNOR, OR/NOR, AND/NAND
	Flip Flops Clocked SR, Clocked SR - Set/Reset, Clocked JK, Clocked JK - Set/Reset, Clocked D, Clocked D - Set/Reset, Clock T, Clocked T- Set/Reset
	Latches SR, SR - Set/Reset, D, D - Set/Reset
	Digital Constant

Accessing Modeling Applications

Modeling applications are accessible from the *Place* menu in OrCAD Capture. To do so:

1. Select *Place – PSpice Component – Modeling Application*.

   Alternatively, click  from the PSpice toolbar.

   The Modeling Application pane opens.

2. Select the required modeling application from which the model is to be created.
   For example, to create a new inductor model:

   a. Click *Passives.*

   b. Click *Inductor*.
      The PSpice Modeling Application - Non Ideal RF Inductor dialog box opens.

3. Specify the value of the required parameters.

4. Click *Place*.
   The PSpice component is attached to a pointer.

Related Topics

PSpice A/D Modeling Applications

2

Accessing Models for Simulation

Modeling applications are used to create new models and associate device instances. To create a new model using modeling applications, perform the following tasks:

1. Select the device type.
2. Specify parameters for the selected device.
3. Place device instance on schematic and complete the connectivity.

When a new device is placed on the schematic, a master index library file is automatically configured at the design-level in the currently active simulation profile for some of the models. This ensures that the project is ready for simulation and the newly created model library is available to PSpice for simulation. The library, `PSpiceModelApps_Include.lib`, is created and all models for the design that require a library are stored in this library. This library file is placed in the `PSpiceModelApps` folder under the *`<project_name>`*`-PSpiceFiles` folder.

Each new unique model instance is added to this library file, which is included at design-level. This makes the models for newly developed devices available for all simulation profiles under that project.

All modeling applications may not require a new model definition; hence, no additional model library will be required. For example, inductors and capacitors do not require a separate model definition. All necessary simulation information for these devices is stored on the schematic instance.

Related Topic

Editing Models

3

Editing Models

You can edit models that are created using modeling applications. To do so, you need to change the device parameters to update the existing model.

To edit an existing model, perform the following tasks:

1. In OrCAD Capture, open the schematic page with the device instance to be modified.
2. Right-click the device instance, and choose *More – Edit PSpice Component* from the pop-up menu.
   Alternatively, choose *Edit – Edit PSpice Component*, or press `SHIFT+N`.
   Modeling application corresponding to the device instance opens.
3. Modify the parameters.
4. Click *Update*.

Related Topic

PSpice A/D Modeling Applications

4

PSpice A/D Modeling Applications

The integrated Capture – PSpice flow supports analog and digital devices in Modeling Application.

- Analog Devices
- Digital Devices

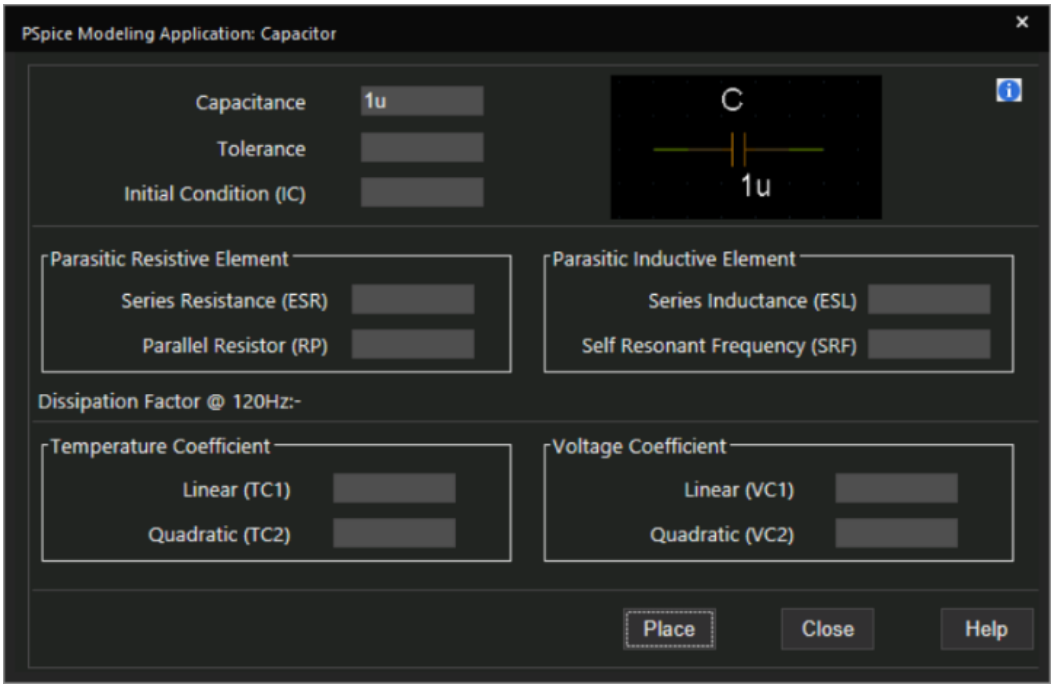
Analog Devices

Modeling Application supports the following analog devices:

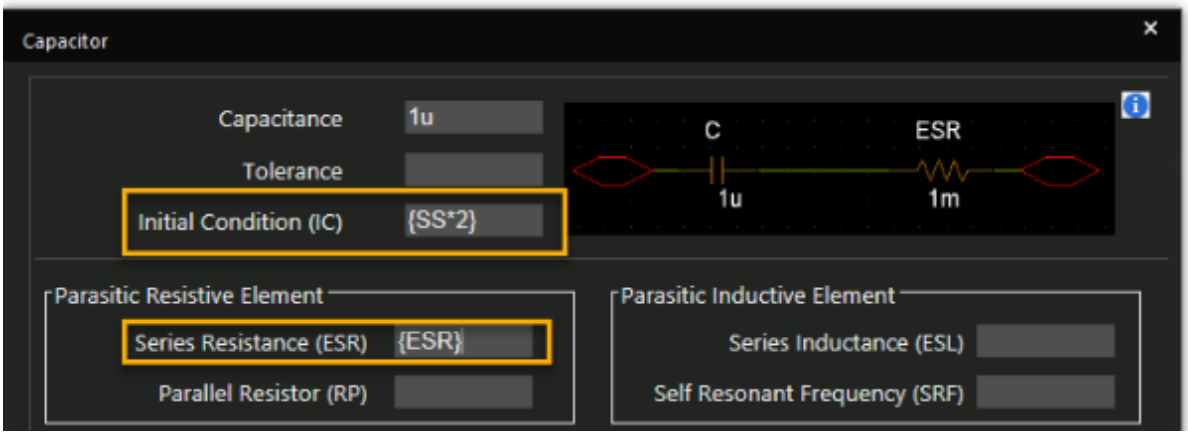
- Capacitor
- Inductor
- Independent Sources
- PWL Sources
- Transient Voltage Suppressors (TVS)
- Zener Diode
- Light-Emitting Diode (LED)
- Switch
- Transformer
- Voltage Controlled Oscillators (VCO)
- Power MOSFET
- Power Diode

Capacitor

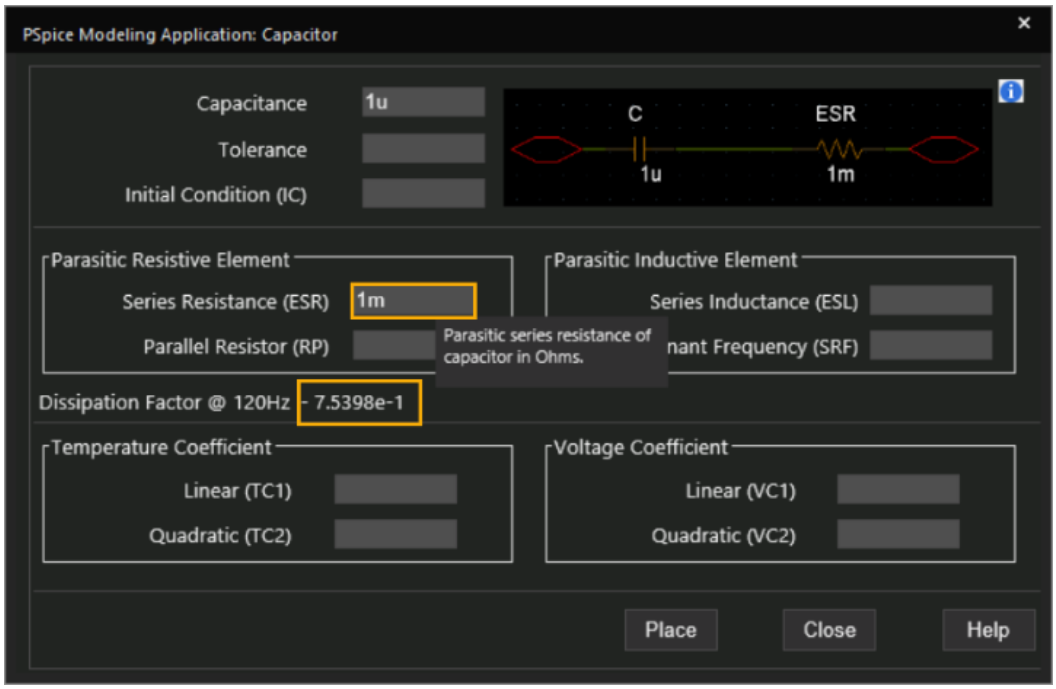
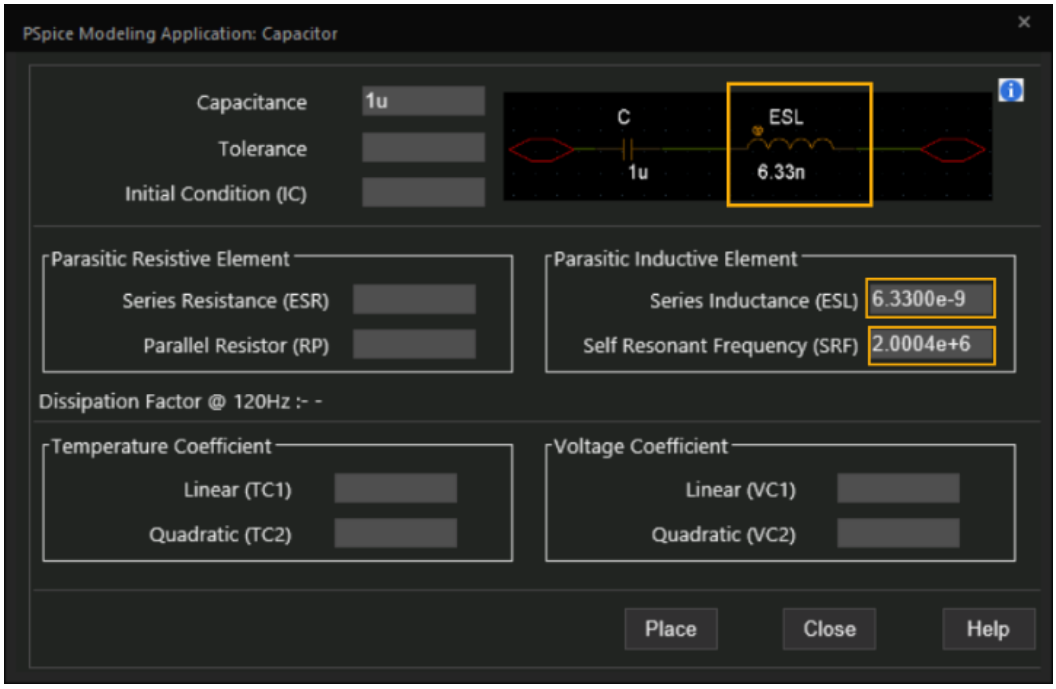
Use the Capacitor modeling application to model non-ideal capacitors with resistive and inductive parasitic. The default values are populated in the mandatory fields.



Use expressions instead of values when defining a capacitor. You can use expressions for *Initial Condition (IC)*, *Series Resistance (ESR)*, *Parallel Resistor (RP)*, *Series Inductance (ESL)*, *Linear (TC1)* and *Quadratic (TC2)* Temperature Coefficients, and *Linear (VC1)* and *Quadratic (VC2)* Voltage Coefficients. Define a parameter and then use the parameter to create an expression. The expression must be enclosed in curly braces. An example is shown below with expressions being used for *IC* and *ESR*.

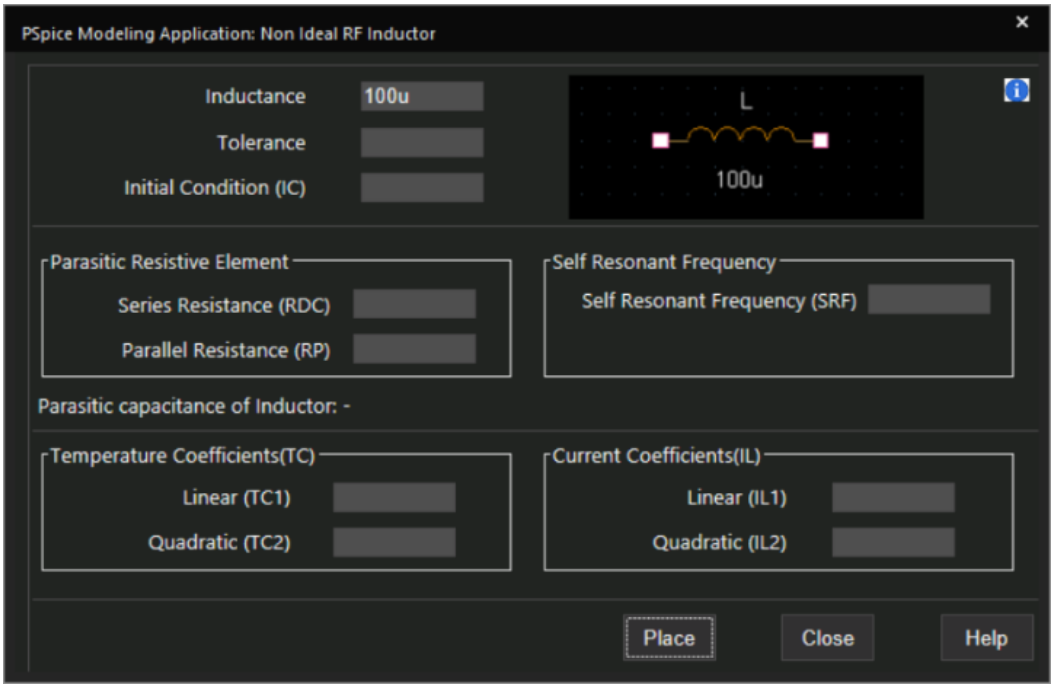


To create a model, use manufacturer data to specify *Tolerance* and *Initial Condition*.

How to work with the modeling application	Example
To add a resistance in series and in parallel, specify the *Equivalent Series Resistance (ESR)* and *Parallel Resistor (RP)* values in ohm. For example, when you specify the ESR value as `1m`, the application displays the value of *Dissipation Factor*, as shown in the following figure.	
To add inductive parasitic, specify either the *Equivalent Series Inductance (ESL)* or the *Self Resonant Frequency (SRF)* mentioned by the manufacturer. The application calculates the other value based on the following equation and displays the result in the corresponding field. $ESL = \frac{1}{((2\pi.SRF)^2 C)}$	

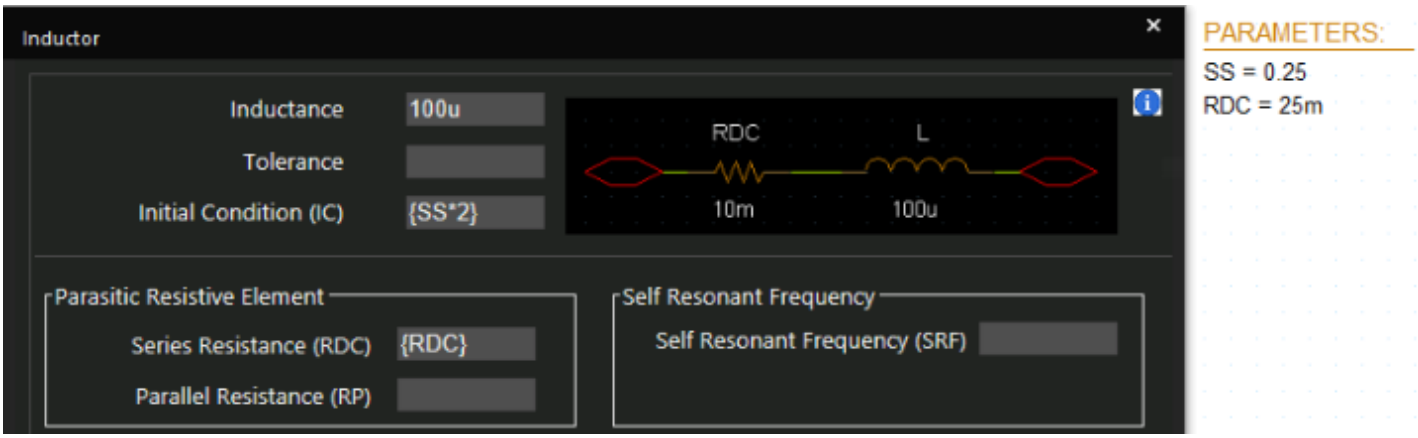
Inductor

Inductor models are frequently used for analog applications, especially those involving a wide range of frequency or high DC currents, such as EMI and DC filters.

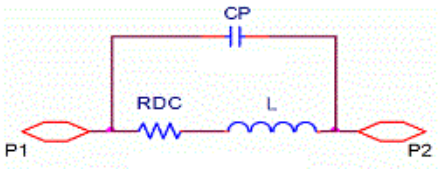


Use this modeling application to model general-purpose non-ideal RF inductors that exhibit resonance due to parasitic capacitance.

Use expressions instead of values when defining an inductor. You can use expressions for *Initial Condition (IC)*, *Series Resistance (RDC)*, *Parallel Resistor (RP)*, *Linear (TC1)* and *Quadratic (TC2)* Temperature Coefficients, and *Linear (IL1)* and *Quadratic (IL2)* Current Coefficients. Define a parameter and then use the parameter to create an expression. The expression must be enclosed in curly braces. An example is shown below with expressions being used for *IC* and *RDC*.



You can model a non-ideal inductor using the DC resistance, wire capacitance, and magnetic core loss to represent the non-linear characteristics. The non-ideal behavior of an inductor is because of the DC resistance of the wire and the self-capacitance. This can be represented in a circuit, with a capacitor in parallel (CP) and a resistance in series (RDC) with the inductor (L).



You can add RDC value directly in the application. However, the value of capacitor in parallel (CP) labeled as *Parasitic capacitance of Inductor* in the application is calculated based on the value specified for *Self-Resonant Frequency (SRF)*.

The parasitic capacitance is calculated using SRF based on the equation:

$$Cp = \frac{1}{((2\pi SRF)^2 \times L) + (Rdc \times 2\pi SRF)}$$

Where:

- `SRF` is the self-resonant frequency of the inductor
- `RDC` is the DC resistance
- `L` is the inductance

The inductor model generated using this application does not include core model; therefore, it will not demonstrate any saturation characteristics. The effect of DC current causing magnetic saturation can be approximately modeled using *Current Coefficients (IL)*, as explained in the Example section.

In this modeling application, you can configure *Inductance*, DC series resistance (RDC), and *Self-Resonant Frequency (SRF)*. Based on these inputs, the application calculates the parasitic capacitance value (*Parasitic capacitance of Inductor*). You can also configure an additional *Parallel Resistance (RP)* in the inductor model by specifying its value in the application. This is an optional parameter of model and is specified to model the magnetic loss.

Current Coefficient (IL) affects the inductance value according to the following equation:

$$L = L_o + IL_1 \times I + IL_2 \times I^2$$

Where:

- L_0 is the nominal value of the inductor, labeled as *Inductance* in the modeling application
- L is the effective inductance at current I
- IL_1 is the linear current coefficient
- IL_2 is the quadratic current coefficient

Inductor specification gives the DC current, I, at which the inductance falls to 75% of its nominal value, L_0. This is modeled using current coefficients as:

$$0.75L_o = L_o + IL_1 \times I^2 + IL_2 \times I^2$$

Assuming $IL_1 = 0$, this becomes:

$$IL_2 = (-0.25)/I^2$$

The *Temperature Coefficients (TC)* affect the inductance as per the following formula:

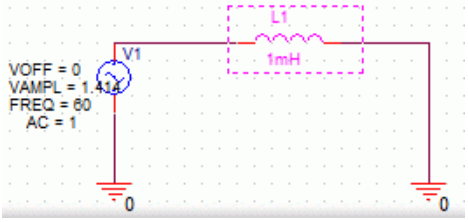
$$TC1 \times (T - T_{nom}) + TC2 \times (T - T_{nom})^2$$

Where:

- $TC1$ is the linear temperature coefficient
- $TC2$ is the quadratic temperature coefficient
- T_{nom} is the nominal temperature.
  T_{nom} is the default value for simulation and is $27°C$. To edit this value, you need to specify a new value in the Simulation Settings dialog box.

Example

This is an example circuit with a non-ideal inductor modeled using this application.

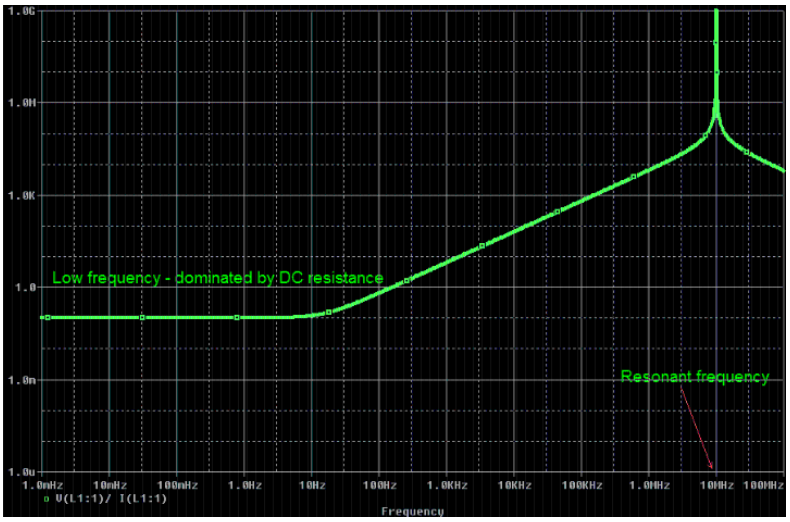


The inductor is placed with the following values specified in the modeling application:

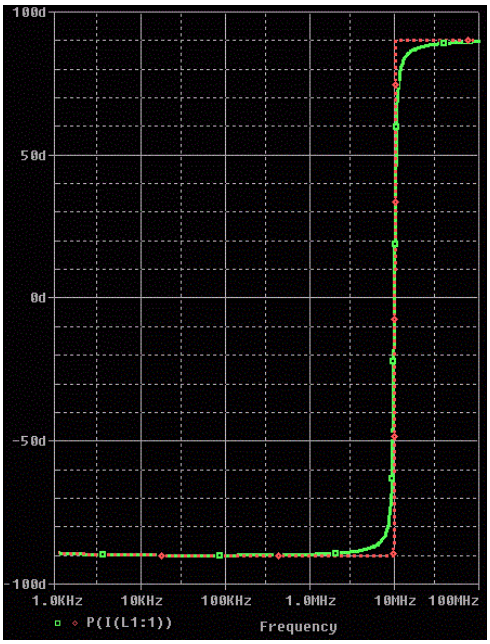
- Inductance: $1m$
- Series Resistance (RDC): $100m$
- Self-Resonant Frequency (SRF): $10Meg$

When the circuit is simulated for impedance, you see the following result. In non-ideal inductors, there is a loss of phase shift because of a high resistive element at low frequencies. The impedance value is constant, dominated by

DC resistance, at low frequencies. As frequency increases, the impedance rises to a peak at the resonant frequency (as shown in the following figure) and then starts falling. Beyond the resonant frequency, the parasitic capacitance dominates and the inductor behaves like a capacitor.



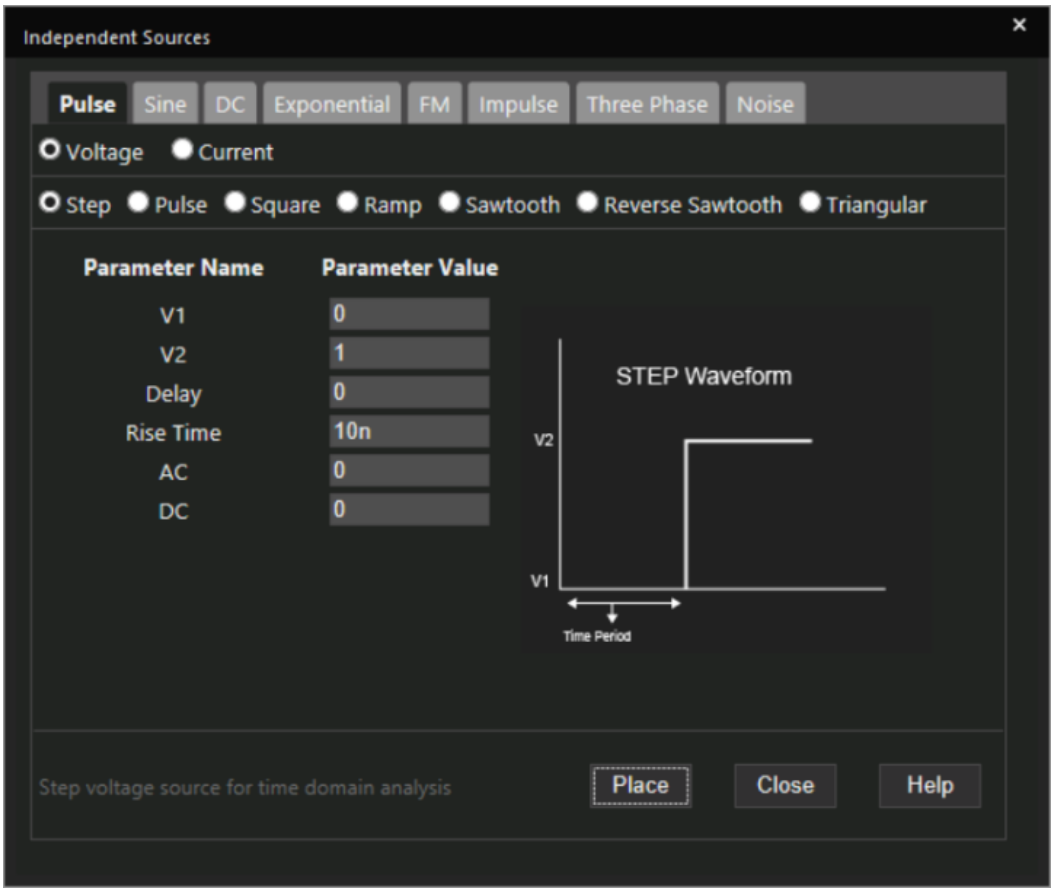
Phase plot of the same circuit, with and without the parallel resistance is described in the following figure. The green trace is for simulation with parallel resistance (RP) of `1Meg` and the red trace is without the parallel resistance. Beyond the resonant frequency (`10Meg`), the phase lag of 90 degrees (Inductive behavior) swings to a phase lead of 90 degrees (capacitive behavior).



Independent Sources

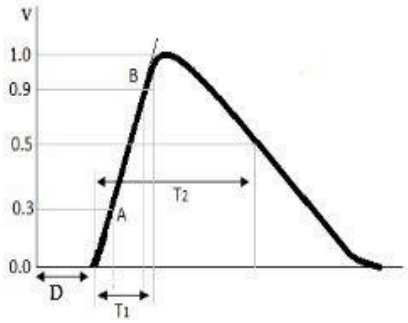
Using the Independent Sources modeling application, the following types of voltage or current sources can be modeled:

- *Pulse:*
  Includes the following pulse types: Step, Pulse, Square, Ramp, Sawtooth, Reverse Sawtooth, and Triangular. You can use expressions instead of values for the following parameters: I1, I2, V1, V2, Delay, Pulse Width, AC, and DC.
- *Sine*:
  Includes the following sinusoidal wave types: Sine, Cosine, and AC Source. You can use expressions instead of values for the following parameters: Offset, VAMPL, IAMPL, Frequency, Delay, Phase, Damping Factor, AC, DC, AC Voltage, and DC Voltage
- *DC*:
  Includes the following DC types: Ideal DC and DC (non-ideal DC).
  An ideal DC source is one that does not have an internal resistance. You can use expressions instead of values for the following parameters: DC Voltage and Source Resistance.
- *Exponential*:
  You can use expressions instead of values for the following parameters: V1, V2, I1, I2, Rise Delay, Rise Time Constant, Fall Delay, Fall Time Constant, AC, and DC.
- *FM*:
  You can use expressions instead of values for the following parameters:
  Offset, Amplitude, Carrier Frequency, Modulation Index, Modulation Frequency, AC, and DC.
- *Impulse*:
  Includes the following Impulse types:1.2/50 µSec, 4/10 µSec,4/20 µSec, 8/20 µSec, 10/350 µSec, and 10/1000 µSec.
  You can use expressions instead of values for the following parameters: VP, IP, and Delay.
- *Three Phase* (Only voltage):
  Includes the following two configurations, DELTA and STAR.
  You can use expressions instead of values for the following parameters: Frequency, Source Inductance, and Source Resistance.
- *Noise* sources:
  Includes the following types of sources: DC, Sine, Pulse, Exponential, and Random Noise.
  You can use expressions instead of values for the following parameters: I1, I2 V1, V2, DC Current, DC Voltage, Offset, Noise Amplitude, VAMPL, IAMPL, Frequency, Delay, Rise Delay, Rise Time Constant, Fall Delay, Fall Time Constant, Pulse Width, Phase, and Damping Factor.



Impulse Sources

In this application, this is referred to as Lightning Voltage Impulse Source. A lightning impulse voltage rises very quickly, in a few microseconds, to its peak value and then falls to 0 relatively slowly. In context of the *Impulse* source, you can use lightning impulse voltages to test the effect of external source of high voltages such as lightning strike on your designs. Designs, such as power supply systems, are often required to be qualified against effect of such impulses. These sources, modeling critically damped lightning impulses, are available as both current and voltage types.
A sample representation of a lightning impulse voltage is shown in the following figure.



The maximum voltage reached, P, is the peak voltage. The intersection of the straight line that connects the points

where the rising wave reaches `0.9` (`B`) and `0.3` (`A`) of the peak voltage is the virtual origin. The time between the origin and the virtual origin is the delay, `D`. The part of the wave from the virtual origin to `P` is the front and the trailing part of the wave is termed tail. The time taken for the impulse to reach the peak from the virtual origin, `T1`, is the front time. Similarly, the time taken to fall to half the peak value, `T2`, is the half time.

The following table lists the voltage and current waveform sources and the corresponding Front and Half times.

Wave (In µ seconds)	Front Time (T1)	Half Time (T2)
1.2/50	1.2 µs	50 µs
4/10	4 µs	10 µs
4/20	4 µs	20 µs
8/20	8 µs	20 µs
10/350	10 µs	350 µs
10/1000	10 µs	1000 µs

Three Phase Sources

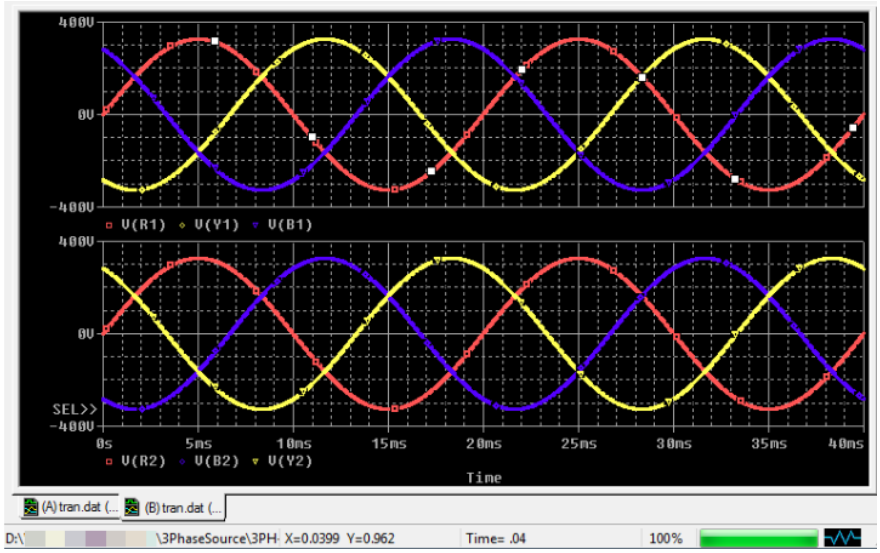
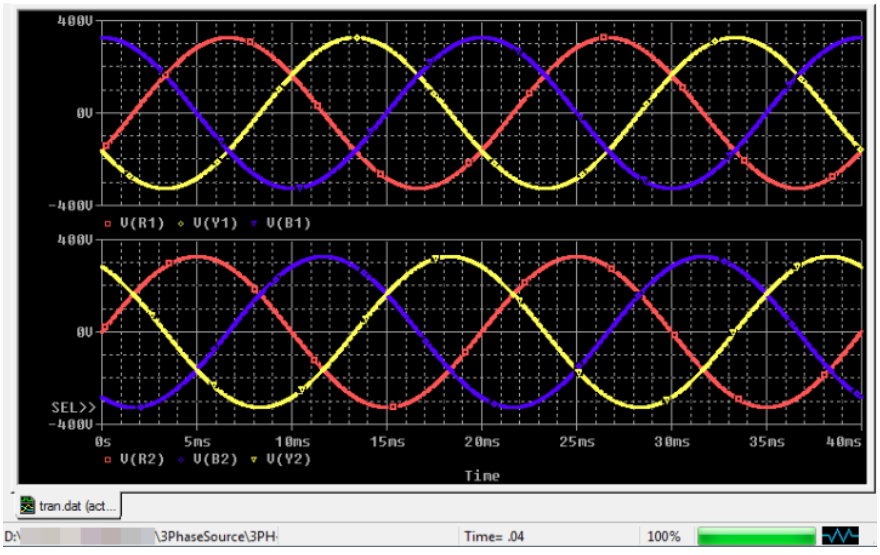
This application enables you to quickly generate balanced three-phase sources. You can select either *Delta* or *Star* configuration.

You can define the following parameters for these two configurations.

Parameter	Description
Line Voltage	The voltage or potential difference between two lines of different phases. The line voltage in three phase systems exists between the RY, RB, and YB phases.

Phase Voltage	The voltage or potential difference between a line and a common neutral point. The relationship between phase voltage and line voltage depends upon the type of configuration used.
	• Star connection
	  ◦ Phase Voltage = Line Voltage / √3
	  ◦ Phase Current = Line Current
	• Delta Connection
	  ◦ Phase Voltage = Line Voltage
	  ◦ Phase Current = Line Current / √3

Frequency	Frequency of operation

Source Inductance	An inductance inserted in series with each phase. This offers source impedance. This is an optional parameter. Use `0` as a value to make it an ideal source.
Source Resistance	A resistance inserted in series with each phase. This is an optional parameter. Use `0` as a value to make it an ideal source.
Phase Sequence	The order in which the phase voltages reach their maximum magnitude. If the Phase sequence is *RYB*, then Phase voltage at *R* will reach its maximum value first, followed by *Y*, and then *B*. In the following figure, the top plot shows the waveform for phase sequence *RYB* and the bottom plot shows phase sequence *RBY*. 
Phase Lag	The lag or lead of Phase R at t=0. For phase lag the value is negative. In the following figure, the bottom plot shows the waveform with zero phase lag and the top plots shows a waveform for 30 degree phase lag (input in UI is -30). For a phase lead of 30-degree UI value should be 30. 

Noise Sources

This source type enables you to add random noise models for most of the standard sources in the schematic design. It supports both voltage and current noise sources. The voltage and current noise sources are further classified as DC, Sine, Pulse, Exponential, and Random Noise, which is an independent random transient noise source.

You can specify Noise Amplitude and various other noise parameters depending on the noise source you select. Noise Amplitude can be defined as the difference between the maximum voltage limit (5.5V) and minimum voltage limit (4.5V). For example, as seen in the following figures, if the voltage magnitude is 5V and Noise Amplitude is 1V, the output of the noise source will fluctuate in the range of 5.5V and 4.5V.

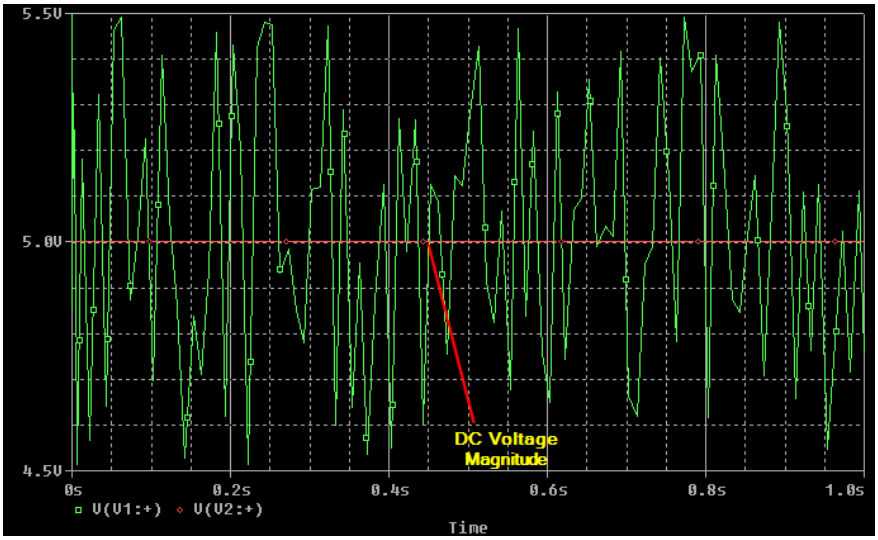


Figure - DC Voltage Noise

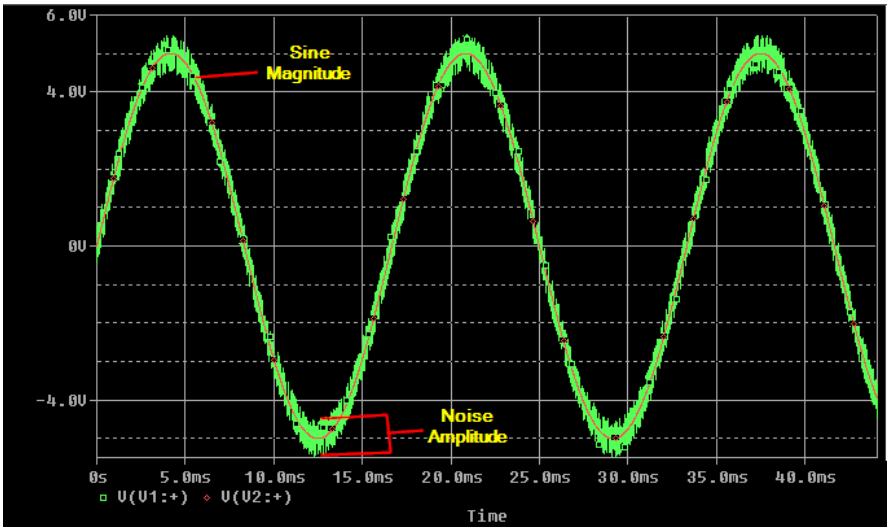
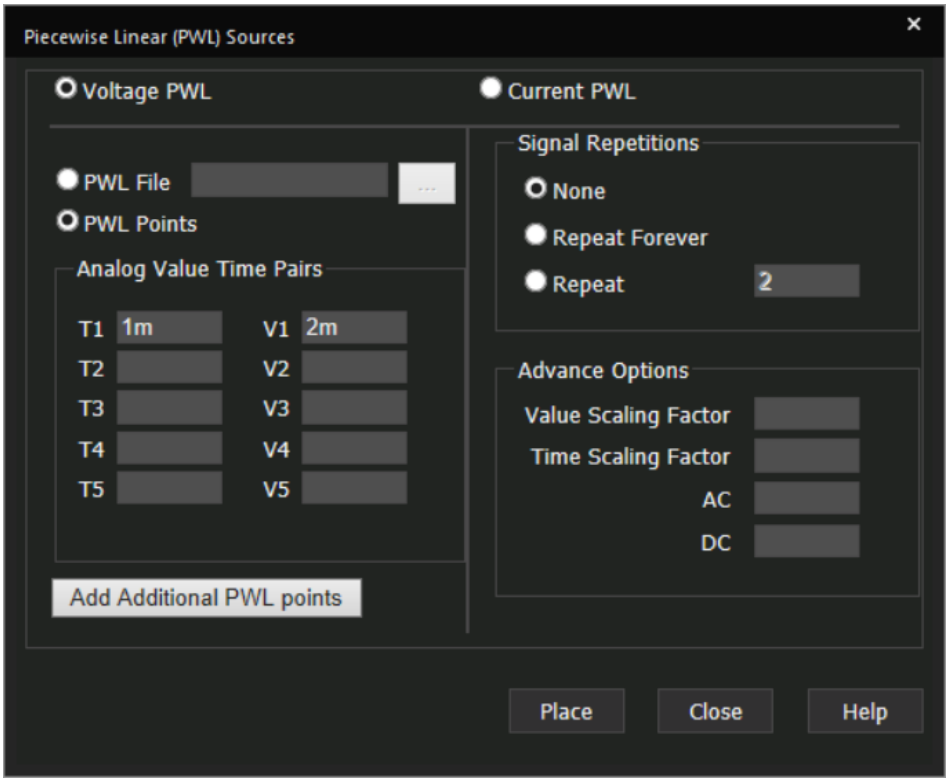


Figure - Sine Voltage Noise

PWL Sources

Use the Piecewise Linear (PWL) Sources modeling application to model time-dependent PWL sources.



You can specify time and amplitude relationship to define a PWL source model with a large set of data points. To do so, either specify a *PWL File* or *PWL Points* to model a PWL source. You can also define *Signal Repetitions* and *Scaling Factors* through this interface.

The description of each parameter is shown in the following table.

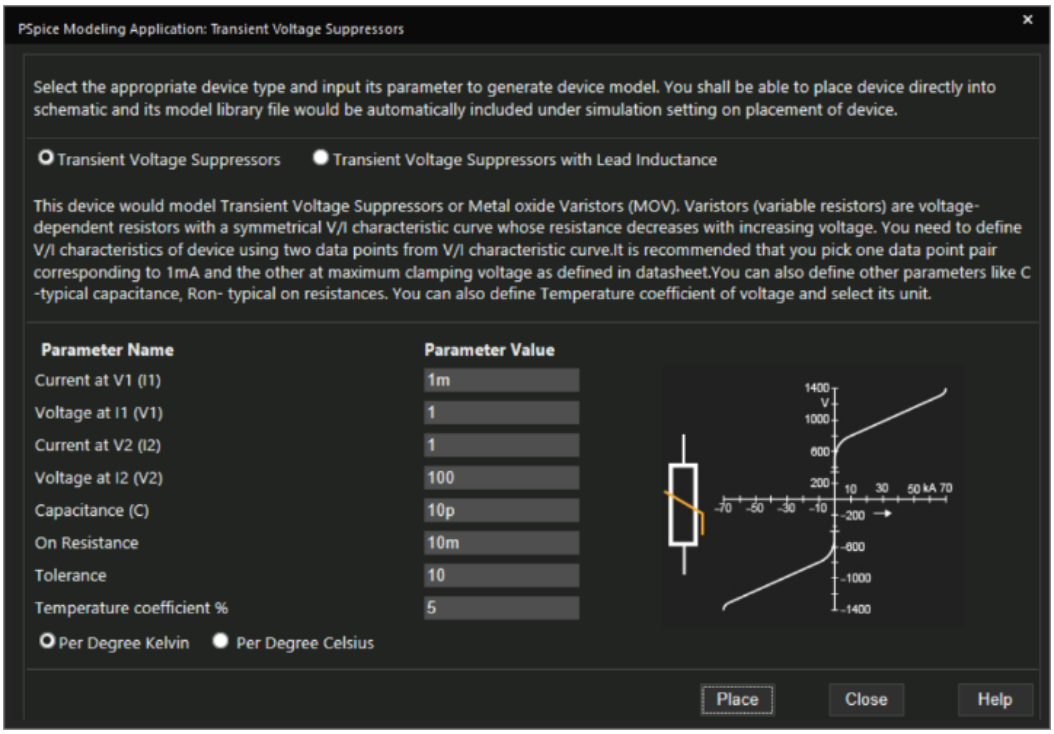
Parameter	Description
PWL File	Select to specify a file that lists the time-value pairs. A time and value pair must be separated by a space.
PWL Points	Select to enable the fields under *Analog Value Time Pairs* to specify the time and value pairs in the user interface.
Analog Value Time Pairs	Enabled if you select *PWL Points*. At least one pair of values must be entered for simulation source. You can increase it by clicking *Add Additional PWL Points*.

Signal Repetitions	Specify the number of periodic repetitions for the given set of points. You can select any one of the following: • *None*: Select to specify no repetitions. • *Repeat Forever*: Select to periodically repeat the complete PWL signals from the start until the end of simulation. • *Repeat*: Select and specify a whole number to set the number of repetitions. By default the value is 2.
Advance Options	Specify the following optional advanced options: • *Value Scaling Factor*: Specify the factor by which the value in each PWL pair will be multiplied. Note that Value Scaling Factor or VSF is sometimes referred to as Voltage Scaling Factor in context of Voltage PWL sources. Refer to PSpice Help online help document. • *Time Scaling Factor*: Specify the factor by which the time in each PWL pair will be multiplied. • *AC*: Specify the AC magnitude for an AC sweep analysis. • *DC*: Specify the DC voltage magnitude for a bias point and transient analysis.

Transient Voltage Suppressors (TVS)

A transient voltage suppressor (TVS) is used to protect electronics circuit against voltage transients such as lightning surges etc. You can connect TVS models in parallel to devices and circuits to protect from voltage surges.

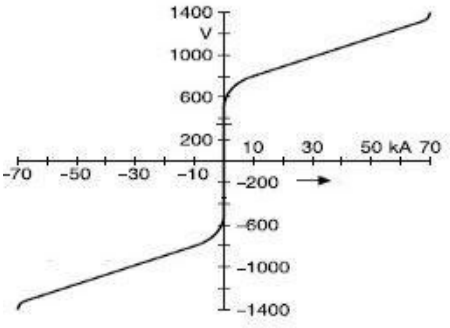
Use the TVS modeling application to create TVS or metal oxide varistor (MOV) devices.



To create the TVS device using this application, you can specify the parameter information directly from the datasheet. The models support temperature effects, tolerances, and package parasitic. You can specify Temperature Coefficient in:

- `Percentage per Degree Celsius`
- `Percentage per Degree Kelvin`

TVS resistance decreases with increase in voltage, acting as a resistance shunt as shown in the following `V/I` curve.



The equation for a TVS device is:

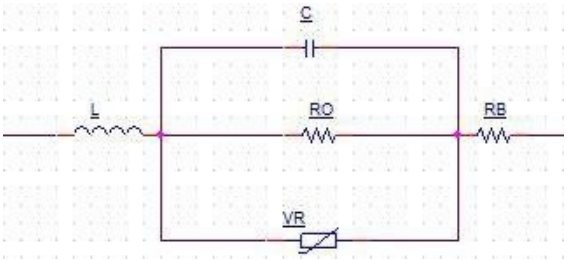
$I=KxV^{\alpha}$

Where:

- `I` is the current through the device
- `K` is a constant depending on the type of the device

- α is the nonlinearity exponent and is a measure of the steepness of the V/I characteristics of a TVS

The behavior of the TVS device for different current ranges can be derived from the following circuit.



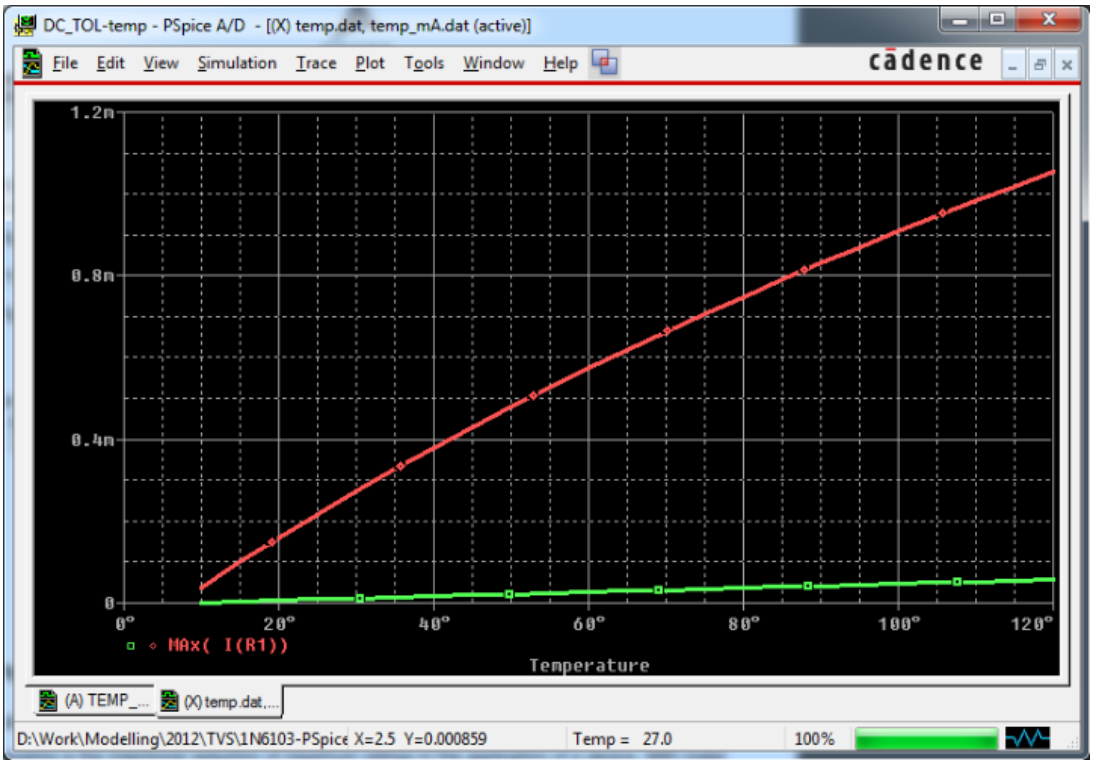
In this circuit:

- L is the lead inductance
- RO is the ohmic resistance of the devices and it has very high value
- RB is the bulk resistance
- C is the capacitance
- VR is an ideal varistor

Based on the V/I curve of a TVS device, following characteristics are observed:

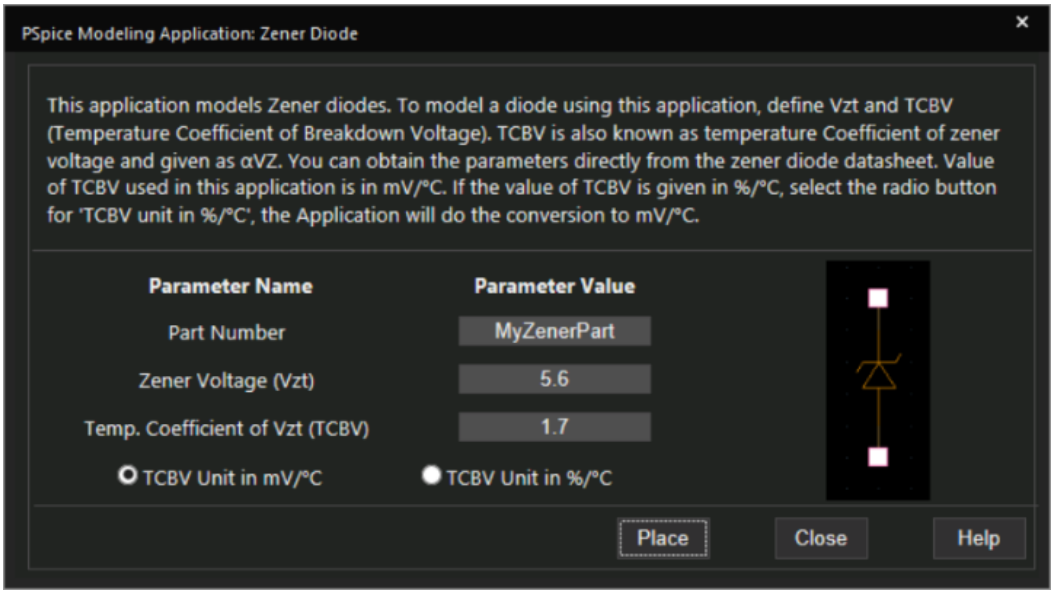
- **Leakage current region**: At a very low current, of the order of less than 10^{-4}A, the ideal varistor has infinite resistance and RO determines the behavior of the circuit. The leakage current will increase with temperature. In this region the V/I curve becomes linear.
- **Normal operating region**: At the normal operating range (10^{-5} to 10^{3}A) the VR determines the behavior.
- **High current region**: At currents above 10^{3}A, the varistor has zero resistance and RB determines the behavior.
- **Lead inductance**: Lead inductance affects the response time of varistors. The varistor should use the shortest possible leads to reduce inductance.
- **Varistor voltage**: The voltage drop across a varistor for a 1mA current is the varistor voltage. This value is only used to specify varistors.
- **Tolerance**: The varistor voltage at 25°C with 1mA passed in shown in the figure below. The trace at the center represents the varistor voltage at nominal value and the other two traces represent the values at either side of the tolerance band.

- **Temperature coefficient**: The transient voltage suppressors show a negative temperature coefficient of voltage. An increase in leakage current is consequently noticeable at higher temperatures, especially in the higher leakage current region. The following figure shows the variation of leakage current against temperature. The green waveform operates it at voltage, thus higher leakage current and variation against temperature.



Zener Diode

Use the Zener diode modeling application to model general-purpose zener diode.



To create a model, specify Zener voltage and temperature coefficient of Zener breakdown voltage (TCBV) given as αVZ. These parameter values can be obtained directly from the Zener diode datasheet.

You can select one of the following units for TCBV:

- `mV/°C`
- `%/°C`

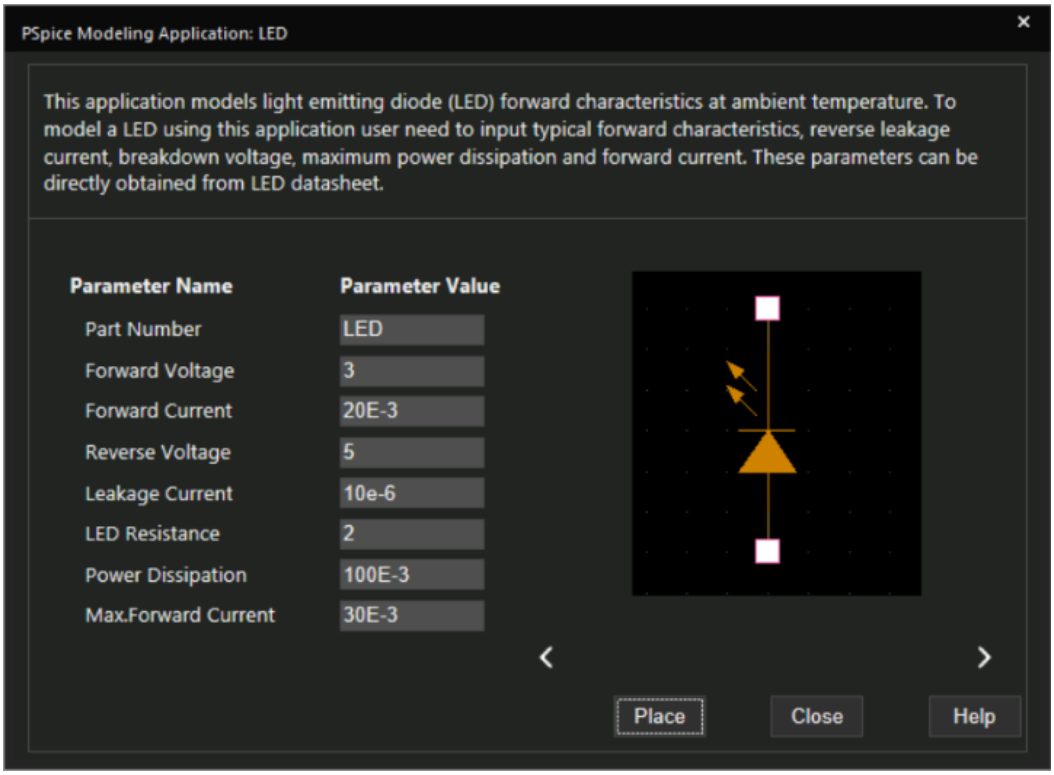
This application internally converts and uses TCBV in `mV/°C`. This conversion is based on the following equations:

$$\alpha VZ = \frac{\Delta Vz}{\Delta T} (V/°C$$

$$\alpha VZ = \frac{\Delta Vz}{\Delta T} \times \frac{1}{\Delta Vz} \times 100(\%/°C$$

Light-Emitting Diode (LED)

Use the LED model to represent general-purpose LED devices in your schematic design.

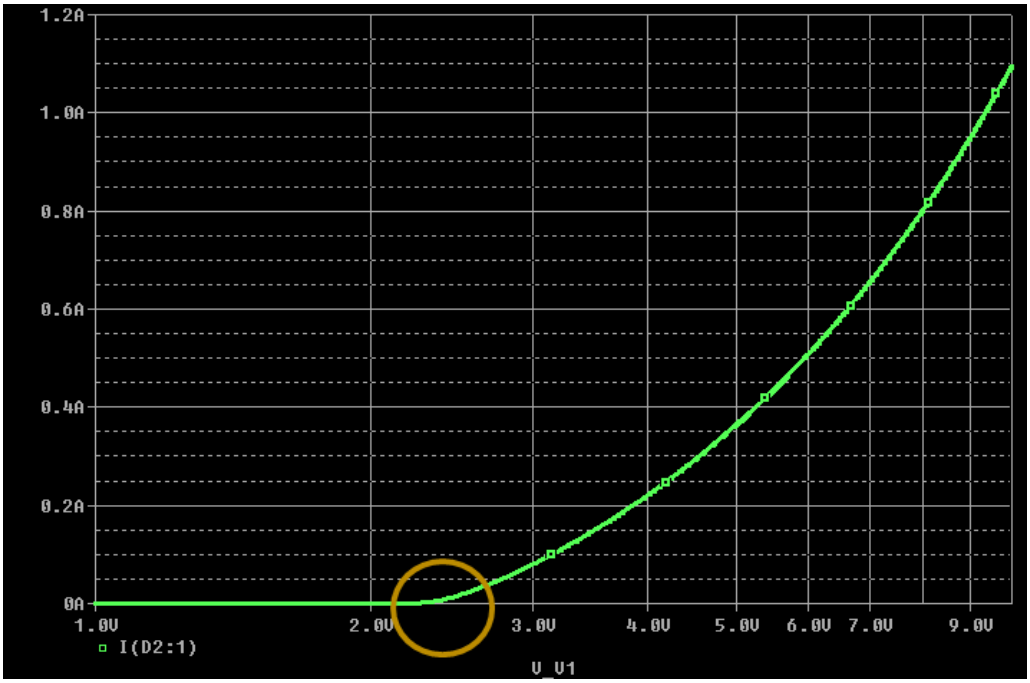


To create a model of LED, you need to define the following parameters using datasheet values:

- Forward Voltage
- Forward Current
- Reverse Voltage
- Leakage Current

- LED Resistance
- Power Dissipation
- Maximum Forward Current

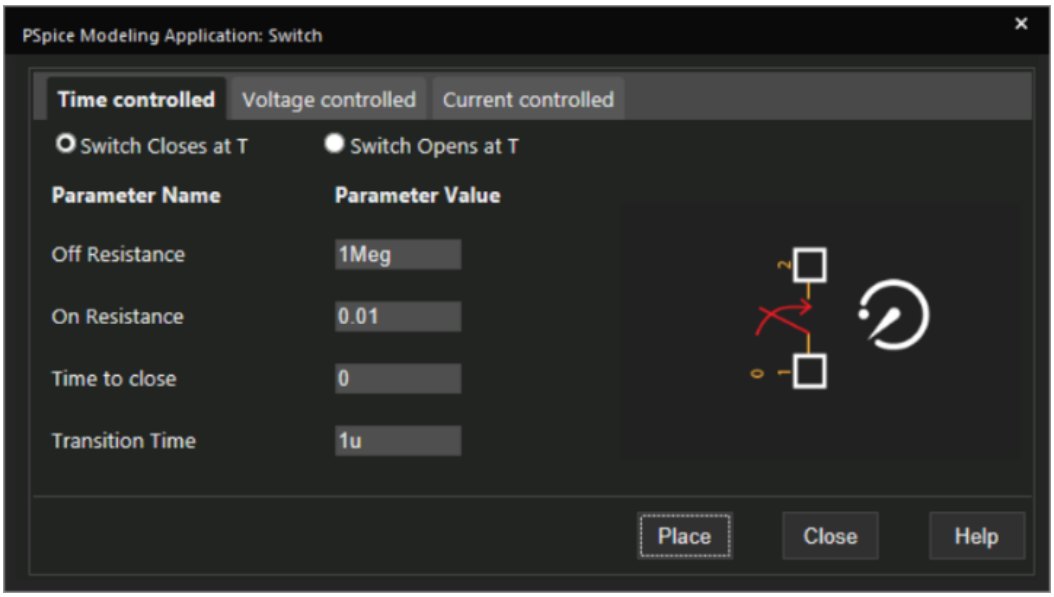
To understand the relation between the forward characteristics of the LED devices and the LED model, define the forward voltage as `2.25V` in the LED model. In the following figure, notice that the forward voltage rises after `2.25V`, which was defined in the LED device model.



Switch

Use the Switch modeling application to create the following type of switches:

- **Time controlled**: These switches change or toggle their state at a specified time. Here the specified time is the simulation time.
- **Voltage controlled**: These switches change their state at a specified voltage.
- **Current controlled**: These switches change their state at a specified current.



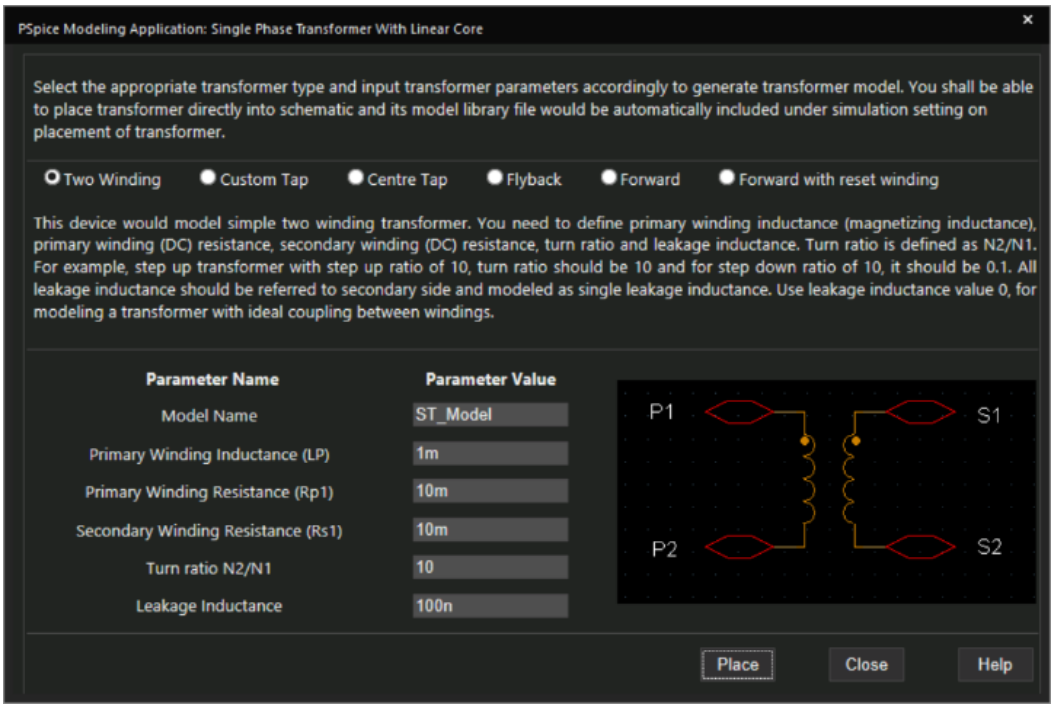
You can create multiple types of switches, such as simple switches or switches with hysteresis.

The switch models have built-in checks for a dynamic range of parameters. If there are any violations or errors in the specified values, then these are displayed in the user interface.

You can use expressions instead of values for the following parameters: Off Resistance, On Resistance, VOFF, VON, IOFF, ION, Time to Close, Transition Time, Threshold voltage, Hysteresis voltage, Threshold current, Hysteresis current, and Delay.

Transformer

Use the Transformer modeling application to model general-purpose transformers.



You can create the following types of transformers:

- Two Winding: It generates a model for a simple two-winding transformer.
- Custom Tap: It generates a model for a custom tap transformer.
- Center Tap: It generates a model for a center tap transformer.
- Flyback: It generates a model for a single-ended flyback converter transformer.
- Forward: It generates a model for a single-ended forward converter transformer.
- Forward with Reset Winding: It generates a model for a single-ended forward converter transformer with auxiliary reset winding.

Parameter	Description	Unit	Default Value (Can be edited)
Model Name	Name of the model.		
Primary Winding Inductance (LP)	The primary winding inductance or magnetizing inductance to determine the flux that will link the cores. The unit is Henry.	Henry	1m
Primary Winding Resistance (Rp1)	The resistance of the primary winding. The unit is Ohm.	Ohm	10m
Secondary Winding Resistance (Rs1)	The resistance of the secondary winding. The unit is Ω (Ohm)	Ohm	10m

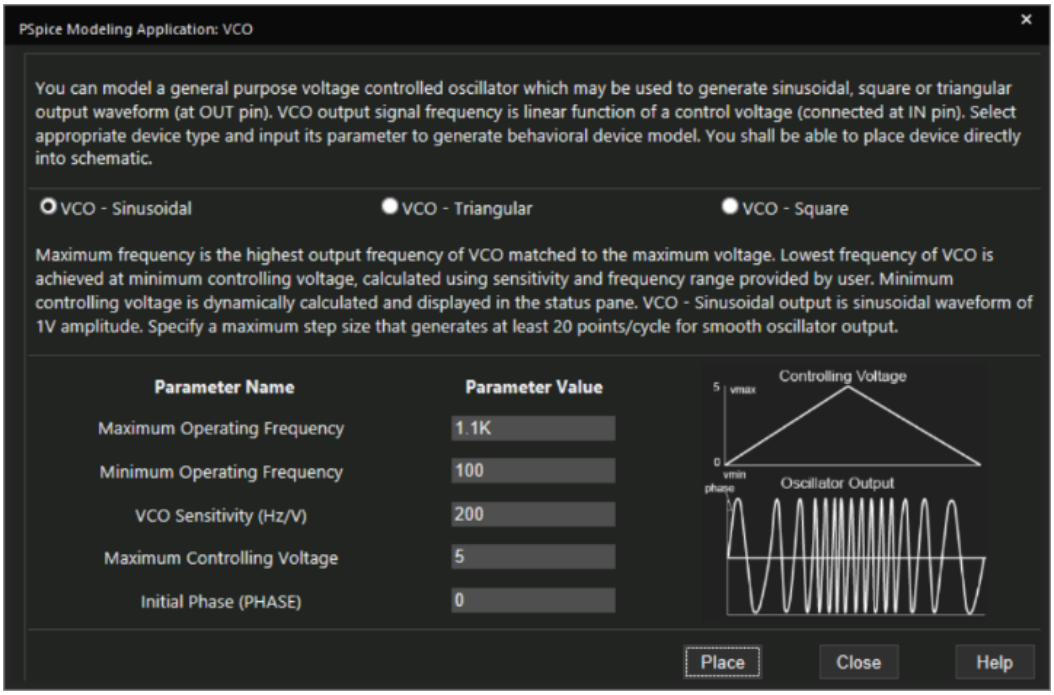
Turn ratio N2/N1	The turn ratio in terms of the number (N2) of turns for the secondary winding by the number (N1) for the primary winding.		10
Leakage inductance	The leakage inductance represents energy stored in the non-magnetic regions between windings, caused by imperfect flux coupling.	Henry	100n
Tap %	The tap percentage specifies where the tap is required to achieve the turns ratio required. This parameter is available only when *Custom Tap* is selected.		10
Primary Tap %	The tap percentage is specified for the primary winding. Available only when *Custom Tap* is selected.		Selected
Secondary Tap %	The tap percentage is specified for the secondary winding. Available only when *Custom Tap* is selected.		Not selected
Primary Tap	The centre tap is specified for the primary winding only. Available only when *Centre Tap* is selected.		Selected
Secondary Tap	The centre tap is specified for the secondary winding only. Available only when *Centre Tap* is selected.		Not selected
Both	The centre tap is specified for both the primary and the secondary winding. Available only when *Centre Tap* is selected.		Not selected
Reset Winding Turn Ratio	The reset winding turn ratio is the ratio of the reset turns to the primary winding. Available only when *forward with reset winding* is selected.		1

Important
You can use the inductors and coupling parts, `Kbreak` and `K_linear`, to model different types of transformers. The following three example circuits will help in understanding the usage of `Kbreak` and `K_Linear` symbols. You can access these from *Help – Learning PSpice* under the topic, *PSpice Application Notes – Using the Inductor Coupling Symbols*.

- Simple two winding transformer
- Modeling dot convention of a transformer
- Centre-tapped full-wave rectifier transformer

Voltage Controlled Oscillators (VCO)

Voltage Controlled Oscillator (VCO) is an oscillator having an output whose frequency is proportional to an applied voltage. VCOs are widely used in applications such as Function Generators, PLLs, Frequency Synthesizers, and so on. This modeling application allows you to create VCOs with *Sinusoidal*, *Triangular*, and *Square* waveforms as output.



Specify the following parameters to define your model.

Parameter	Description
Maximum Operating Frequency	Maximum frequency of oscillator, in `Hz`
Minimum Operating Frequency	Minimum frequency of oscillator, in `Hz`
VCO Sensitivity	VCO Sensitivity, in `Hz/V`
Maximum Controlling Voltage	Maximum input voltage which produces the highest oscillator frequency, in `V`
Initial Phase (PHASE)	Initial phase of oscillator output, in `degrees`

Example

You need a VCO to operate in the frequency range `Fmin=1E6Hz` and `Fmax=10E6Hz`. The controlling voltage is in the range of `5V` to `10V`. This gives VCO sensitivity of `1.8E6 Hz/V`. This calculated using the formula:

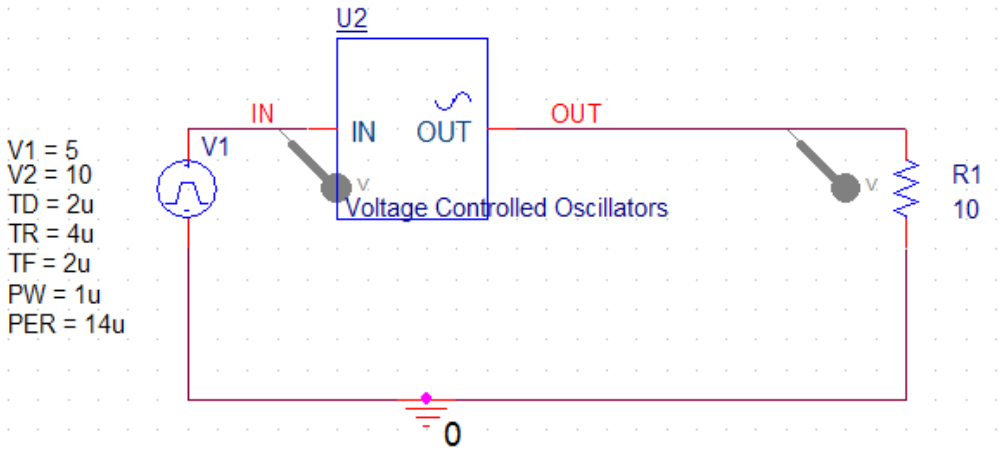
```
(Fmax-Fmin)/(V2-V1)
```

Specify the parameter values in the VCO user interface as:

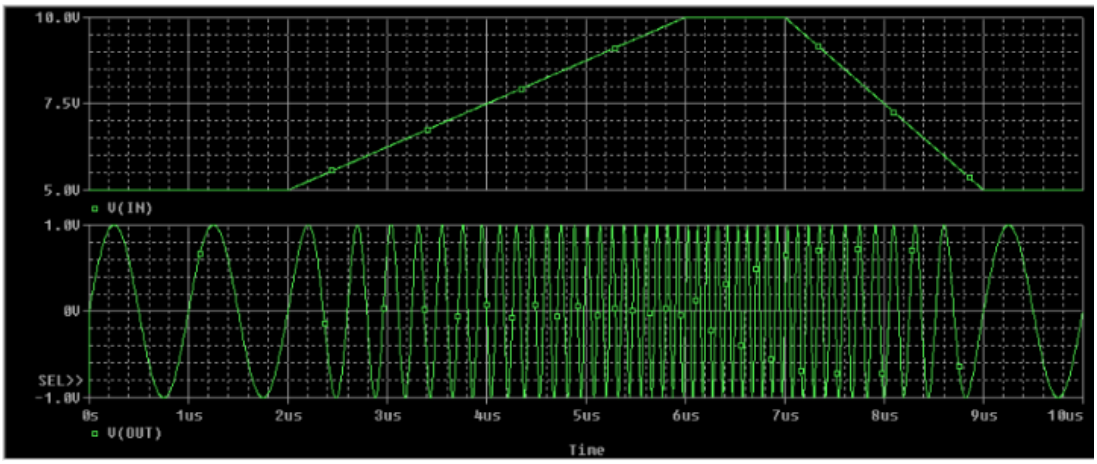
- Maximum Operating Frequency (`Fmax`) = `10E6Hz`
- Minimum Operating Frequency (`Fmin`) = `1E6Hz`

- VCO Sensitivity = `1.8E6Hz/V`
- Maximum Controlling Voltage = `10V`
- Initial Phase = `0 Degree`

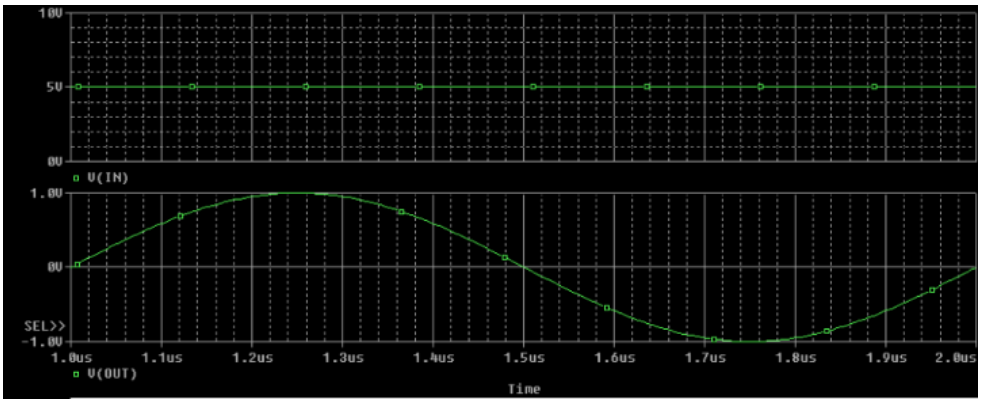
The VCO generated using the application is used in the following circuit is with Ramp (ranging from `5V` to `10V`) at input and load `R1` at output.



Output waveforms show VCO frequency changing with input voltage. The maximum time step value for simulation (as specified in the Simulation Settings) is at `0.005µs` to get a smooth output.



The minimum frequency comes out to be at `5V` input.



On zooming this waveform from `1µs` to `2µs`, and when the input voltage is `5V`, the frequency comes out to be `1/1µs= 1MHz.`

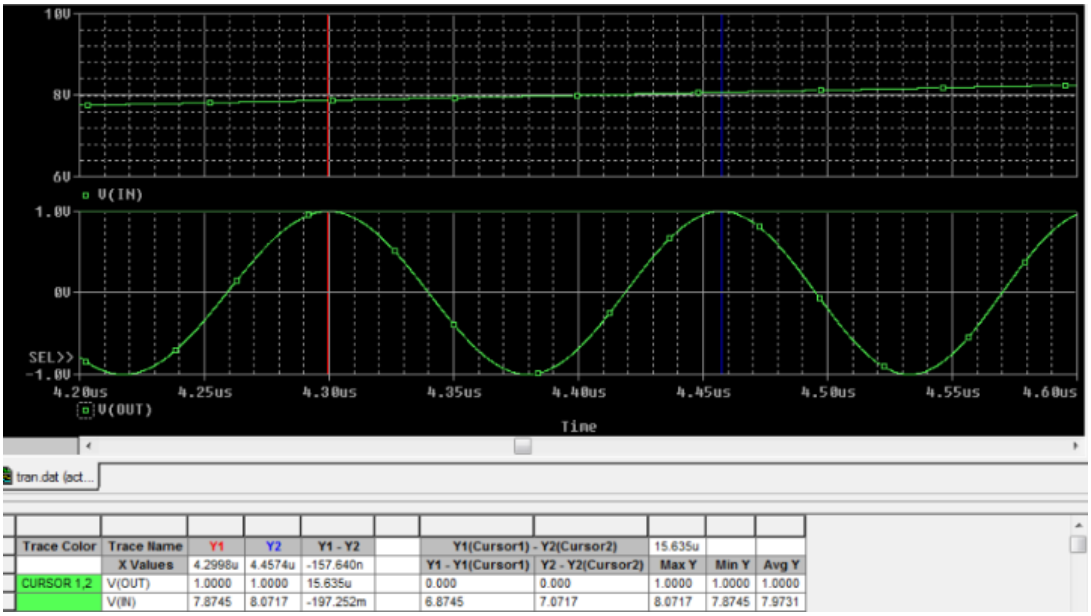
Similarly, you can find out the expected frequency for a given input, say at `8V`, for the following given values:

- Minimum Operating Frequency (`Fmin`) = `1E6Hz`
- Minimum Controlling Voltage (`Vmin`) = `5V`
- VCO Sensitivity = `1.8E6Hz/V`

This gives expected frequency (at `8V`) = `1 + (3*1.8) = 6.4MHz`

(Using the formula, `Fmax = (V2-V1)* VCO sensitivity + Fmin`)

To measure the frequency from simulation results, zoom the area around `8V` input.



Time period (with the help of cursor) = `4.4574µ - 4.2998µ = 0.1576µ`

Frequency comes out to be `1/0.1576µ = 6.345MHz`

Measured frequency comes close to expected frequency. For the measured frequency to be exactly same as

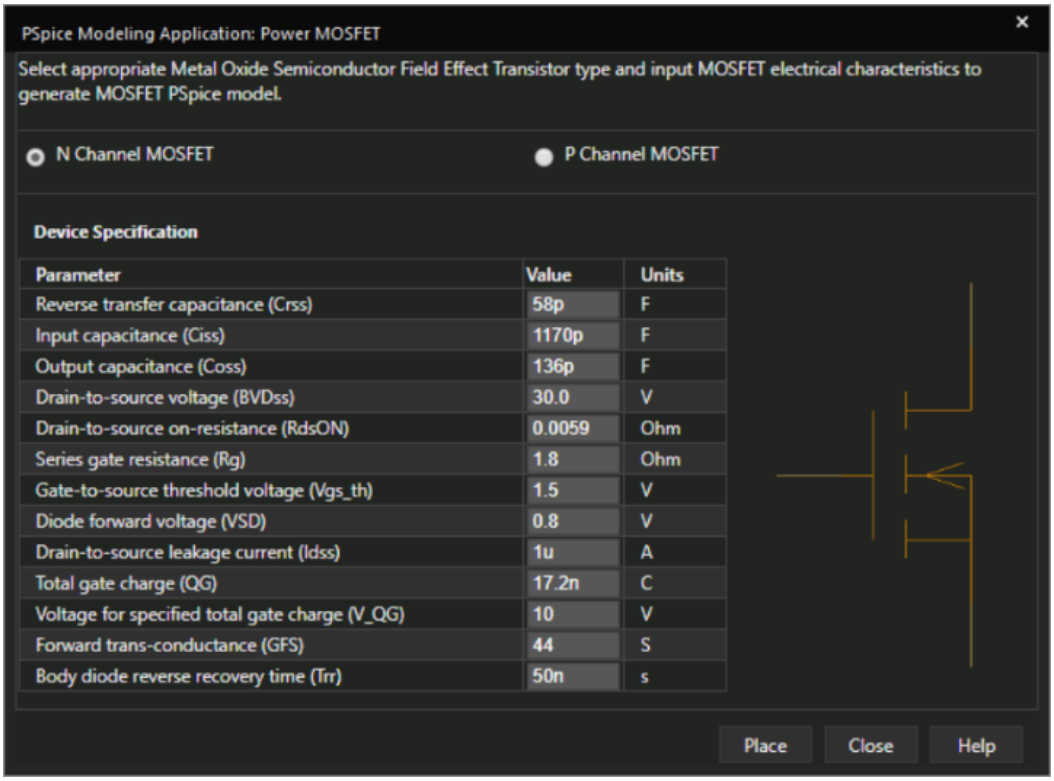
expected frequency, you need to provide step in input at `8V`.

Similarly, the maximum frequency of `10MHz` comes out to be at `10V` Input. VCO output amplitude is fixed at `1V`. This can be modified by using E device from `analog.olb`, specifying a suitable GAIN value, and placing it after VCO.

Power MOSFET

You can add the parameterized Metal Oxide Semiconductor Field Effect Transistor (MOSFETs) using the *Power MOSFET* modeling application interface. The parameters specified in the *Power MOSFET* modeling application enable you to simulate and test the model in various conditions. As a result, you can quickly observe and analyze the performance of the parameterized model in the design.

Select the appropriate MOSFET type (*N Channel MOSFET* or *P Channel MOSFET*) and specify the MOSFET electrical characteristics to generate the Power MOSFET PSpice model.



The specific parameters for MOSFET models and their default values are provided in the following tables:

N Channel MOSFET

Parameter	Description	Default Value (can be edited)	Minimum Value	Maximum Value	Units
Crss	Reverse transfer capacitance	58p	0	10n	F
Ciss	Input capacitance	1170p	0	10n	F

Coss	Output capacitance	136p	0	10n	F
BVDss	Drain-to-source voltage (maximum voltage across MOS)	500	1	1k	V
RdsON	Drain-to-source on-resistance	0.0059	1n	100	ohm
Rg	Series internal gate resistance	1.8	1n	100	ohm
Vgs_th	Gate-to-source threshold voltage (gate voltage at which the MOS starts conducting)	1.5	1n	10	V
Vsd	Diode forward voltage	0.8	0.3	1.0	V
Idss	Drain-to-source leakage current	1u	1p	1m	A
QG	Total gate charge (during complete switching transient)	17.2n	1p	100u	C
V_QG	Voltage for specified total gate charge	10	1u	10k	V
GFS	Forward trans-conductance (ΔIds/ΔVgs for fixed VDS)	44	1m	1e5	S
TRR	Body diode reverse recovery time	50n	0	1	s

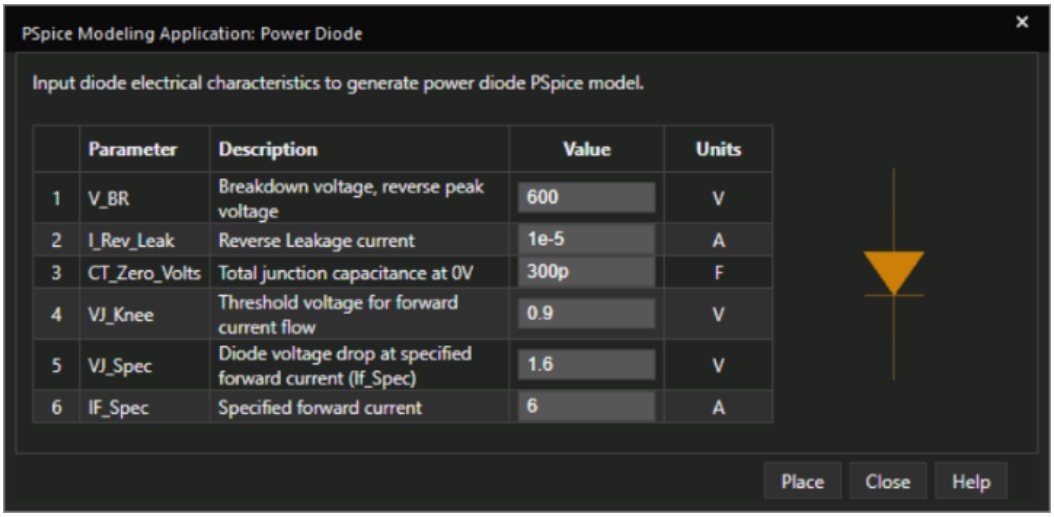
P Channel MOSFET

Parameters	**Description**	**Default Value** (can be edited)	**Minimum Value**	**Maximum Value**	**Units**
Crss	Reverse transfer capacitance	52p	0	10n	F
Ciss	Input capacitance	1630p	0	10n	F
Coss	Output capacitance	902p	0	10n	F
BVDss	Drain-to-source voltage (maximum voltage across MOS)	-500	-1	-1k	V
RdsON	Drain-to-source on-resistance	5.5m	1n	100	ohm
Rg	Series internal gate resistance	0.8	1n	100	ohm
Vgs_th	Gate-to-source threshold voltage (gate voltage at which the MOS starts conducting)	-0.9	-1n	-10	V
Vsd	Diode forward voltage	-0.8	-0.3	-1.0	V
Idss	Drain-to-source leakage current	1u	1p	1m	A

QG	Total gate charge (during complete switching transient)	10.8n	1p	100u	C
V_QG	Voltage for specified total gate charge	-4.5	-1u	-10k	V
GFS	Forward trans-conductance (ΔIds/ΔVgs for fixed VDS)	47	1m	1e5	S
TRR	Body diode reverse recovery time	50n	0	1	s

Power Diode

You can add the parameterized diode using the *Power Diode* modeling application interface. The parameters specified in the *Power Diode* modeling application enable you to simulate and test the model in various conditions. As a result, you can quickly observe and analyze the performance of the parameterized model in the design. Specify the diode electrical characteristics to the generate the Power Diode PSpice model.



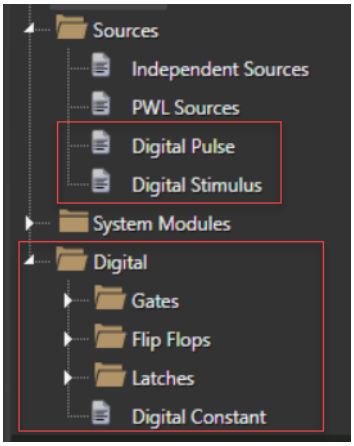
The specific parameters for diode models and their default values are provided in the following table:

Parameters	**Description**	**Default Value** (can be edited)	**Minimum Value**	**Maximum Value**	**Units**
V_BR	Breakdown voltage, reverse peak voltage across diode	600	3	5k	V
I_Rev_Leak	Reverse leakage current when diode is reverse biased	1e-5	1n	500u	A
CT_Zero_Volts	Total junction capacitance at 0V across diode	300p	0	100n	F
VJ_Knee	Threshold voltage (forward bias voltage required for diode to start conducting)	0.90	0.4	5	V

VJ_Spec	Diode voltage drop at specified forward current (IF_Spec)	1.6	0.5	7	V
IF_Spec	Specified forward current	6	10u	1k	A

Digital Devices

Digital devices and sources are now supported in Modeling Applications. You can model various digital devices such as gates (Buffer, Inverter, AND, OR, and so on), flip flops(Clocked SR, Clocked JK, and so on), latches (SR, D, and so on), and sources (digital stimulus, digital clock) and place them on the schematic.

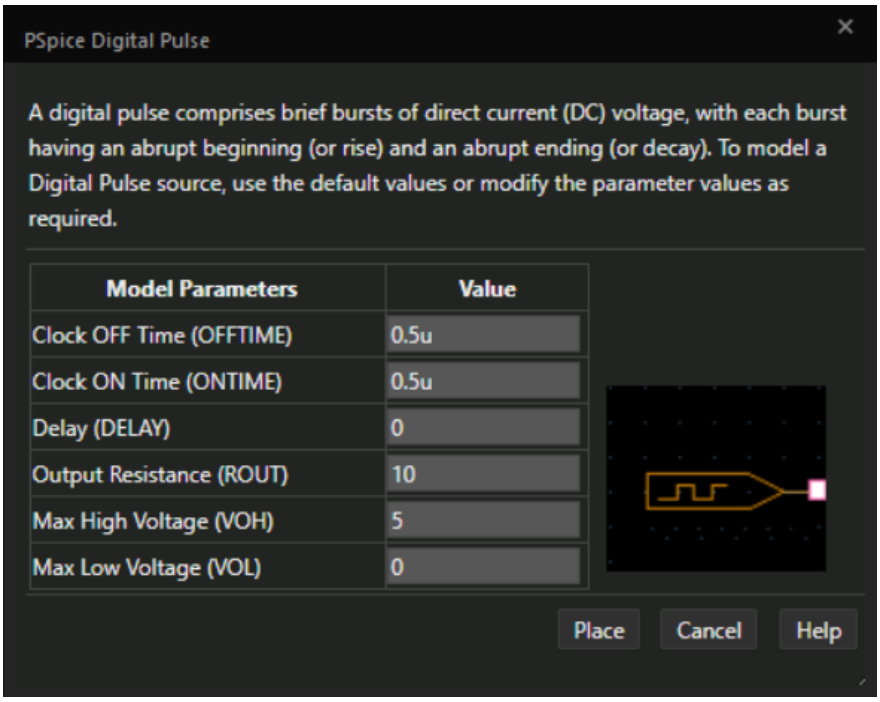


Modeling Application supports the following digital devices:

- Digital Pulse
- Digital Stimulus
- Gates
- Flip Flops
- Latches
- Digital Constant

Digital Pulse

This application is used to model PSpice digital pulse sources. A digital pulse comprises brief bursts of (DC) voltage, with each burst having an abrupt beginning (or rise) and an abrupt ending (or decay). To model a digital pulse source, use the default values or modify the parameter values as required.

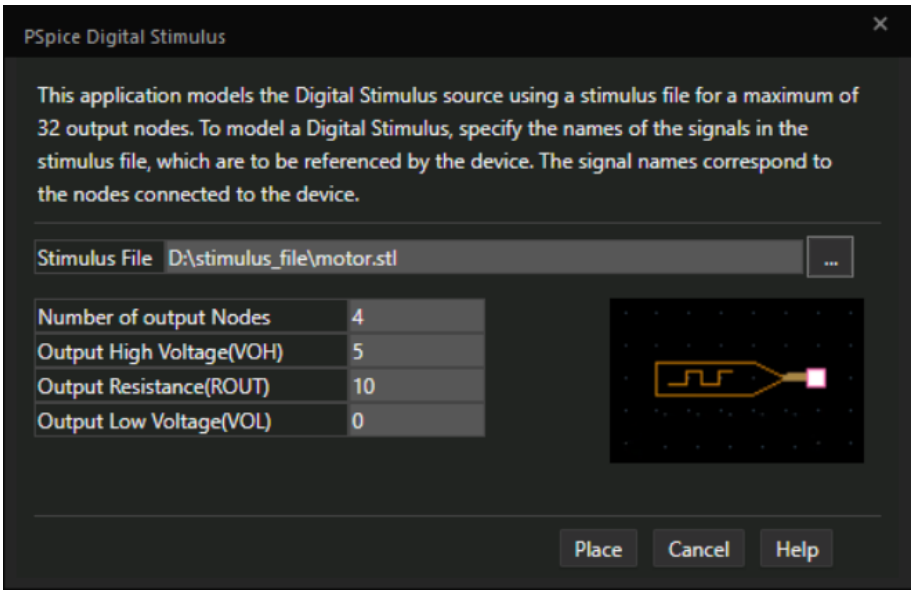


To model a PSpice digital pulse source, specify the following model parameters or use their default values provided in the following table:

Model Parameters	Description	Default Value
Clock OFF Time (OFFTIME)	The time duration when the clock is LOW. **Note**: The default unit is seconds, in case no unit is specified.	0.5us
Clock ON Time (ONTIME)	The time duration when the clock is HIGH. **Note**: The default unit is seconds, in case no unit is specified.	0.5us
Delay (DELAY)	The delay at the output pin (in seconds).	0
Output Resistance (ROUT)	The output pin series resistance, if connected to an analog device (in ohm).	10
Max High Voltage (VOH)	The output high voltage if connected to an analog device (in volts).	5
Max Low Voltage (VOL)	The output low voltage if connected to an analog device (in volts).	0

Digital Stimulus

This application models PSpice digital stimulus source through a stimulus file containing up to 32 output nodes. You need to browse to a location and specify the location of the stimulus file. The device refers to the name of the signal specified in the stimulus file.



You are required to use the stimulus file in the following format:

```
out1 out2 out3 out4 out5

0ns  00001
1us  10001
2us  10101
3us  10001
4us  10101
5us  10001
6us  10101
7us  10001
8us  11101
20ms 11001
21ms 11101
36ms 11001
37ms 11101
47ms 11001
48ms 11101
56ms 11001
57ms 11101
64ms 11001
65ms 11011
200ms 10011
300ms 10010
```

where,

- The first row is reserved for output bit names
- The first column is reserved for time.
- The second column is reserved for binaries.

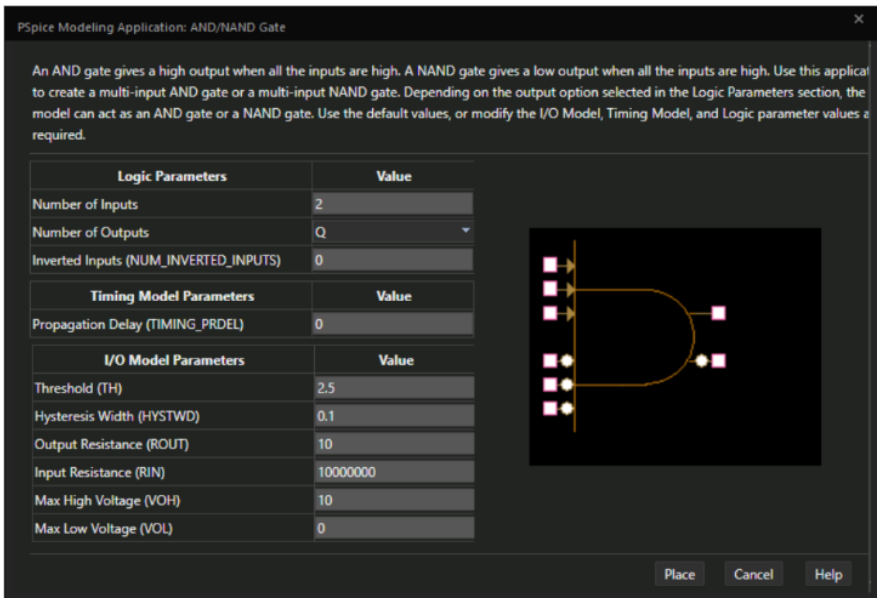
To model a PSpice digital stimulus, specify the following parameters in this application:

Parameters	Description	Default Value
No of output nodes	The total number of signals defined in the stimulus files.	4
Output High Voltage	The output high voltage if connected to an analog device (in volts).	5
Output Resistance	The output pin series resistance if connected to an analog device (in ohms).	10
Output Low Voltage	The output low voltage (in seconds) if connected to an analog device (in volts).	0

Gates

PSpice A/D Modeling Application models the following logic gates:

Buffer/Inverter	A buffer passes the same logic from the input to the output. An inverter complements the logic at the input and passes it to the output. Use this application to create a buffer or an inverter model. Depending on the output pin used in the design, the model can act as a buffer or an inverter. Use the default values or modify the I/O Model and Timing Model parameter values as required.
XOR/XNOR	An XOR gate gives a high output when there is exactly one true input. An XNOR gate gives a low output for the same. Use this application to create an XOR or an XNOR model. The XOR and XNOR gates have two input and two output pins. Depending on the output pin used in the design, the model can act as an XOR gate or an XNOR gate. Use the default values or modify the I/O Model and Timing Model parameter values as required.
OR/NOR	An OR gate gives a high output when one or more inputs are high. A NOR gate gives a low output when one or more inputs are high. Use this application to create a multi-input OR or NOR gate. Depending on the output option selected in the Logic Parameters section, the model can act as an OR or NOR gate. Use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.
AND/NAND	An AND gate gives a high output when all the inputs are high. A NAND gate gives a low output when all the inputs are high. Use this application to create a multi-input AND gate or a multi-input NAND gate. Depending on the output option selected in the Logic Parameters section, the model can act as an AND or NAND gate. Use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.



To model a buffer, an inverter, XOR or XNOR gates, specify the following parameters or use their default values provided in the following table:

Timing Model Parameters	Description	Default Value
Propagation Delay (TIMING_PRDEL)	Delay from the time when input on a pin changes its state until the output changes (in seconds).	0

I/O Model Parameter	Description	Default Value
Threshold (TH)	The threshold value of a logic gate (in volts).	2.5
Hysteresis Width (HYSTWD)	The hysteresis width of a logic gate (in volts). Input is HIGH when it rises above Threshold + (Hysteresis Width/2). Input is LOW when it falls below Threshold - (Hysteresis Width/2).	0.1
Output Resistance (ROUT)	The output resistance of the logic gate (in ohms).	10
Input Resistance (RIN)	Input resistance at each input pin of the logic gate (in ohms).	10000000
Max High Voltage (VOH)	Output high voltage of the logic gate (in volts).	5

Max Low Voltage (VOL)	Output low voltage of the logic gate (in volts).	0

To model OR, NOR, AND, and NAND gates, specify the following parameters or use their default values provided in the following table:

Logic Parameter	Description	Default Value
Number of Inputs	Numbers of active high logic inputs.	2
Number of Outputs	Output pins Q, QBAR, or both.	Q
Inverted Inputs (NUM_INVERTED_INPUTS)	Numbers of active low logic inputs.	0

Timing Model Parameters	Description	Default Value
Propagation Delay (TIMING_PRDEL)	Delay from the time when input on a pin changes its state until the output changes (in seconds).	0

I/O Model Parameter	Description	Default Value
Threshold (TH)	The threshold value of a logic gate (in volts).	2.5
Hysteresis Width (HYSTWD)	The hysteresis width of a logic gate (in volts). Input is HIGH when it rises above Threshold + (Hysteresis Width/2). Input is LOW when it falls below Threshold - (Hysteresis Width/2).	0.1
Output Resistance (ROUT)	The output resistance of the logic gate (in ohms).	10
Input Resistance (RIN)	Input resistance at each input pin of the logic gate (in ohms).	10000000
Max High Voltage (VOH)	Output high voltage of the logic gate (in volts).	10

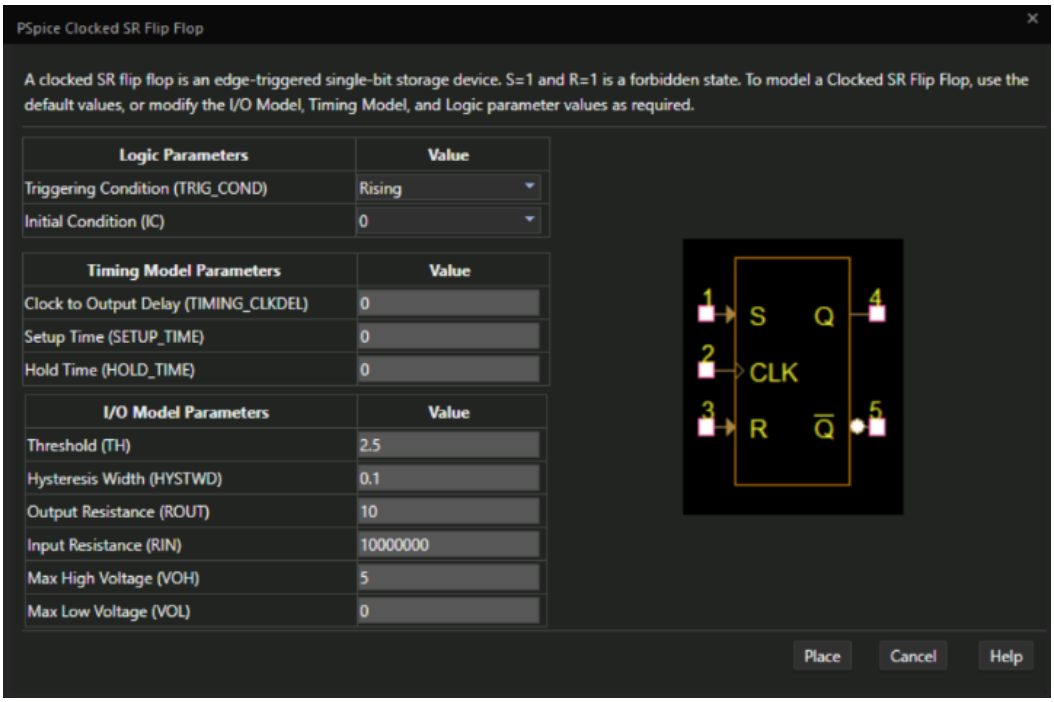
Max Low Voltage (VOL)	Output low voltage of the logic gate (in volts).	0

Flip Flops

This application models the flip-flops, such as Clocked SR, Clocked JK, Clocked D, Clocked T, Clocked SR - Set/Reset, Clocked JK - Set/Reset, Clocked D - Set/Reset, Clocked T - Set/Reset.

Clocked SR	A clocked SR flip-flop is an edge-triggered single-bit storage device. S=1 and R=1 is a forbidden state. To model a PSpice Clocked SR flip-flop, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.
Clocked SR – Set/Reset	A clocked SR flip-flop is an edge-triggered single-bit storage device. The set and reset pins work as preset and clear to initialize the flip-flop. To model a PSpice Clocked SR flip-flop with Set and Reset, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.
Clocked JK	A clocked JK flip-flop is an edge-triggered single-bit storage device that can toggle its output for J=1 and K=1 input. To model a PSpice Clocked JK flip-flop, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.
Clocked JK – Set/Reset	A clocked JK flip-flop is an edge-triggered single-bit storage device that can toggle its output for J=1 and K=1 input. The set and reset pins work as preset and clear to initialize the flip-flop. To model a PSpice Clocked JK flip-flop with Set and Reset, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.
Clocked D	A clocked D flip-flop is an edge-triggered device that transfers input data to output pin on rising or falling edge of the clock. To model a PSpice Clocked D flip-flop, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.
Clocked D – Set/Reset	A clocked D flip-flop is an edge-triggered device that transfers input data to output pin on rising or falling edge of the clock. The set and reset pins work as preset and clear to initialize the flip-flop. To model a PSpice Clocked D flip-flop with Set and Reset, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.
Clocked T	A clocked T flip-flop toggles state when T input is high and retains the previous state if T input is low. To model a PSpice Clocked T flip-flop, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.

Clocked T – Set/Reset	A clocked T flip-flop toggles state when T input is high and retains the previous state if T input is low. The set and reset pins work as preset and clear to initialize the flip-flop. To model a PSpice Clocked T flip-flop with Set and Reset, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.



To model Clocked SR, Clocked JK, Clocked D, and Clocked T flip-flops, specify the following parameters or use their default values provided in the following table:

Logic Parameter	Description	Default Value
Triggering Condition (TRIG_COND)	A flip-flop toggles the state when the input is high and retains the previous state if the input is low.	Rising
Initial Condition (IC)	The initial condition of a flip-flop.	0

Timing Model Parameters	Description	Default Value
Clock to Output Delay (TIMING_CLKDEL)	The delay is calculated from the triggering edge of the clock to the output (in seconds).	0
Setup Time (SETUP_TIME)	Time duration for which the input remains stable before the arrival of the clock edge (in seconds).	0

Hold Time (HOLD_TIME)	Time duration for which the input remains stable after the clock edge (in seconds).	0

I/O Model Parameter	Description	Default Value
Threshold (TH)	The threshold value of a flip-flop (in volts).	
Hysteresis Width (HYSTWD)	The hysteresis width of a flip-flop (in volts). Input is HIGH when it rises above Threshold + (Hysteresis Width/2). Input is LOW when it falls below Threshold - (Hysteresis Width/2).	0.1
Output Resistance (ROUT)	The output resistance of the flip-flop (in ohms).	10
Input Resistance (RIN)	Input resistance at each input pin of the flip-flop (in ohms).	10000000
Max High Voltage (VOH)	Output high voltage of the flip-flop (in volts).	5
Max Low Voltage (VOL)	Output low voltage of the flip-flop (in volts).	0

To model Clocked SR - Set/Reset, Clocked JK - Set/Reset, Clocked D - Set/Reset, Clocked T - Set/Reset flip-flops, specific the following parameters or use their default values provided in the following table:

Timing Model Parameters	Description	Default Value
Clock to Output Delay (TIMING_CLKDEL)	The delay from the triggering edge of the clock to the output (in seconds).	0
Set/Reset Delay (TIMING_SRDEL)	Set or reset the delay of a flip-flop (in seconds).	0
Setup Time (SETUP_TIME)	Time duration for which the input remains stable before the arrival of the clock edge (in seconds).	0
Hold Time (HOLD_TIME)	Time duration for which the input remains stable after the clock edge (in seconds).	0

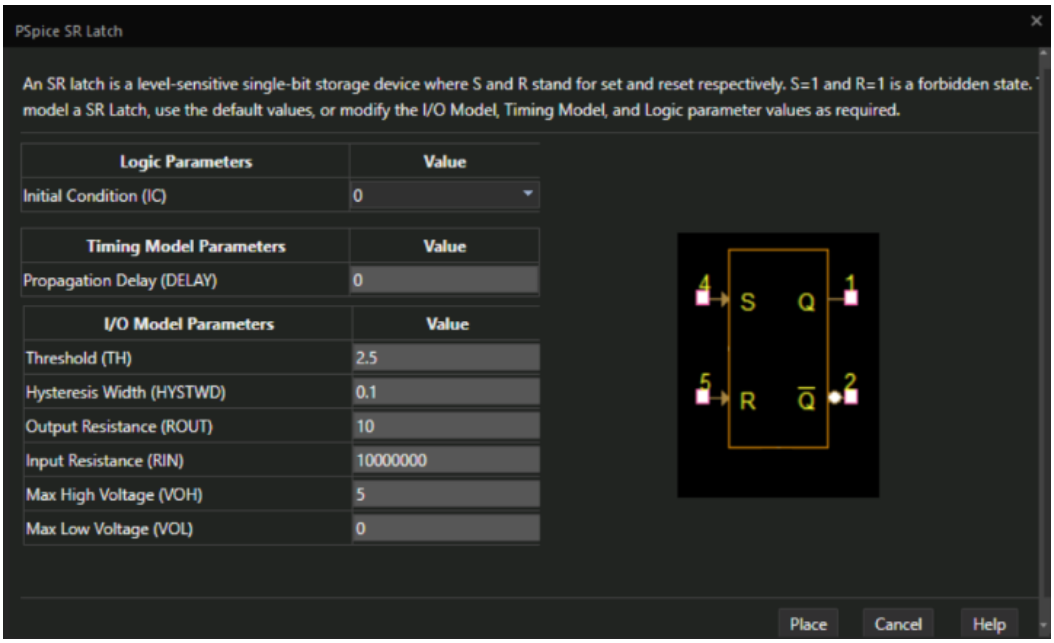
I/O Model Parameter	Description	Default Value
Threshold (TH)	The threshold value of a flip-flop (in volts). Input is HIGH when it rises above Threshold + (Hysteresis Width/2) Input is LOW when it falls below Threshold - (Hysteresis Width/2)	2.5
Hysteresis Width (HYSTWD)	The hysteresis width of a flip-flop (in volts). Input is HIGH when it rises above Threshold + (Hysteresis Width/2). Input is LOW when it falls below Threshold - (Hysteresis Width/2).	0.1
Output Resistance (ROUT)	The output resistance of the flip-flop (in ohms).	10
Input Resistance (RIN)	Input resistance at each input pin of the flip-flop (in ohms).	10000000
Max High Voltage (VOH)	Output high voltage of the flip-flop (in volts).	5
Max Low Voltage (VOL)	Output low voltage of the flip-flop (in volts).	0

Latches

This application models the latches, such as SR, SR - Set/Reset, D, D - Set/Reset.

SR	An SR latch is a level-sensitive single-bit storage device where S and R stand for set and reset respectively. S=1 and R=1 is a forbidden state. To model a PSpice SR Latch, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.
SR – Set/Reset	An SR latch is a level-sensitive single-bit storage device where S and R stand for set and reset respectively. The set and reset pins work as preset and clear to initialize the latch. To model a PSpice SR Latch with Set and Reset, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.
D	A D latch is a level-sensitive device that transfers input data to the output pin on a change of the control signal. To model a PSpice D Latch, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.

D – Set/Reset	A D latch is a level-sensitive device that transfers input data to the output pin on a change of the control signal. The set and reset pins work as preset and clear to initialize the latch. To model a PSpice D Latch with Set and Reset, use the default values, or modify the I/O Model, Timing Model, and Logic parameter values as required.



To model SR, SR - Set/Reset, D, D - Set/Reset T latches, specify the following parameters or use their default values provided in the following table:

Logic Parameter	Description	Default Value
Initial Condition (IC)	The initial condition of a latch.	0

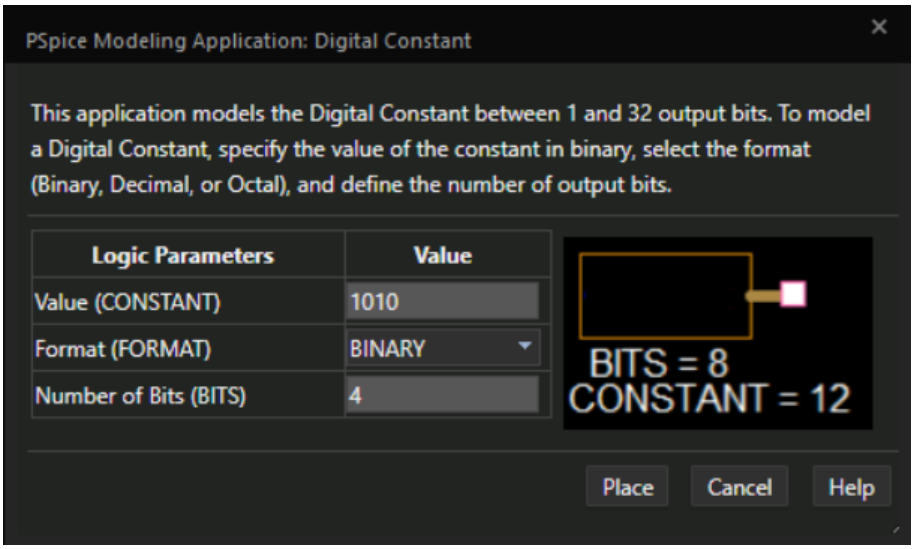
Timing Model Parameters	Description	Default Value
Propagation Delay (DELAY)	Delay from the time when input on a pin changes its state until the output changes (in seconds).	0

I/O Model Parameter	Description	Default Value

Threshold (TH)	The threshold value of a latch (in volts). Input is HIGH when it rises above Threshold + (Hysteresis Width/2) Input is LOW when it falls below Threshold - (Hysteresis Width/2)	2.5
Hysteresis Width (HYSTWD)	The hysteresis width of a latch (in volts). Input is HIGH when it rises above Threshold + (Hysteresis Width/2). Input is LOW when it falls below Threshold - (Hysteresis Width/2).	0.1
Output Resistance (ROUT)	The output resistance of the latch (in ohms).	10
Input Resistance (RIN)	Input resistance at each input pin of the latch (in ohms).	10000000
Max High Voltage (VOH)	Output high voltage of the latch (in volts).	5
Max Low Voltage (VOL)	Output low voltage of the latch (in volts).	0

Digital Constant

This application models the digital constant between 1 and 32 output bits. To model a PSpice digital constant, specify the value of the constant, select the format (Binary, Decimal, or Octal), and define the number of output bits.



To model a PSpice digital constant, specific the following logic parameters or use their default values provided in the following table:

Model Parameters	Description	Default Value
Value (CONSTANT)	Specify the value of the constant in binary.	1010
Format (FORMAT)	Select a format, either Binary, Decimal, or Octal.	BINARY
Number of Bits (BITS)	Define the number of output bits.	4