cadence®

Migrating DE-HDL Designs to Allegro® X System Capture

Product Version 23.1
October 2022

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Contents

1

Importing Design Entry HDL Designs

This document for those designers and organizations who are looking to migrate their designs from Design Entry HDL (DE-HDL) to System Capture. This document:

- Describes methods in which you can reuse existing DE-HDL projects in System Capture
- Compares the benefits of each method
- Explains the DE-HDL components that you need to review before continuing your schematic design tasks in System Capture

In this document, the term source is used for the incoming design from DE-HDL and destination is for the System Capture design, existing or new.

Before You Move Designs from DE-HDL to System Capture

When migrating designs from DE-HDL to System Capture, all the libraries and parts used in the DE-HDL design must be available to the destination design.

Ensure Part Information is Available

There are two ways of ensuring this:

- Setting CDS_SITE

  Point to a CDS_SITE which has the libraries used, project settings for packager, and PTFs in the `site.cpm`

- Using a DE-HDL Project

  In case a DE-HDL design uses local libraries, create an archive, and use it to create a new System Capture project. All the parts used in the source project are available to the destination project. However, the project settings are not available in System Capture.

Save the Design in DE-HDL

To ensure Ref Des are correctly brought into System Capture and packaging errors are avoided, save the design in DE-HDL first and then import into System Capture.

Check Mandatory Elements are Included

While most of the DE-HDL design elements are recognized and use models continued, there are some areas where System Capture operates differently. The section Analyzing the Import Limitations explains all details, but before you attempt to bring any DE-HDL, check the following in the DE-HDL source.

- All parts used must be available to the destination design.

  Parts can be in different libraries in the destination design as compared to the source. System Capture can handle the library difference without any user intervention.

- Part Table Files must be available

- Backannotation must be done after the design is packaged to ensure that all the packaging properties are updated on the schematic

Unsupported DE-HDL Elements

The following DE-HDL elements are not brought into System Capture:

- BOM
- Generated Physical files
- Packaged data - except state data (`pxl.state`)

  Import block brings in the state file, import sheet does not.
- Variants

  Importing sheets does not bring in variants. If you need to bring in design variants, import design as blocks or use *Create Project from Existing Design.*
- Constraints

  Constraints are brought in only when creating a new project based on existing designs or when importing blocks. Importing sheets does not bring in constraints.

Important

Only special symbols instantiated in the source designs being imported are brought into the System Capture design.

Control Component Nudging

By default, the pin-pitch and grid settings are based on the values set in `site.cpm` or installation. To use the source design's settings, set:

```
ALLOW_IMPORT_DESIGN_AT_SITE_UNIT = 'NO'
```

When set to `'NO'`, off-grid components are nudged to the nearest grid point.

To stop the components movements, set:

```
ALLOW_IMPORT_DESIGN_NUDGE_OFFGRID_OBJECTS = 'NO'
```

When this directive is set to `'NO'`, if the design can be the design can be brought in with a finer grid setting, System Capture changes the grid and brings the design in. If not, the import is stopped.

Configure Pin Text Visibility

In DE-HDL designs, the `PIN_TEXT` is always displayed, regardless of the visibility set in the `symbol.css`. The display of pin text is also controlled by the symbol-level property `PIN_TEXT_VISIBLE`.

On the other hand, System Capture follows the visibility set in the `symbol.css`. This results in a display difference in the DE-HDL imported schematics and when placing the symbols. The pin text appears missing for all the imported symbols at times.

To ensure the same visibility of `PIN_TEXT` as the original DE-HDL design, set the following directive in the CANVAS section of site.cpm:

```
'HONOR_DEHDL_PIN_TEXT_VISIBILITY' = 'TRUE'
```

Migrating DML-Dependent Designs

Migrating a DE-HDL Design that DML dependent directly to System Capture is not supported. If you have such designs, you need to change the DE-HDL design to the DML Independent state (Xnet ON/Xnet ON) state using the following directives and then migrate the design to System Capture.

```
START_CONSTRAINT_MGR

AUTO_XNETS_USING_DML 'OFF'

AUTO_XNETS_USING_GATES 'ON/OFF'

END_CONSTRAINT_MGR
```

Check the AUTO_XNETS_USING_GATES Directive

Before importing DE-HDL designs, ensure the value of the `AUTO_XNETS_USING_GATES` is the same in the design being imported and in `site.cpm`. The value in the `site.cpm` is what is followed by the newly created System Capture design. And later on, this directive cannot be changed and if you export to the same board created from DE-HDL, System Capture reports errors.

Global PTF Properties in Designs

By default, System Capture does not access PTF data from reference libraries. As a result, global PTF properties are not accessible in the designs imported from DE-HDL. To overcome any potential information losses, such as XNets and related constraints, set the `ANNOTATE_GLOBAL_PTF_PROPS` directive to *`true`* in the `site.cpm`.

Methods to Reuse DE-HDL Designs

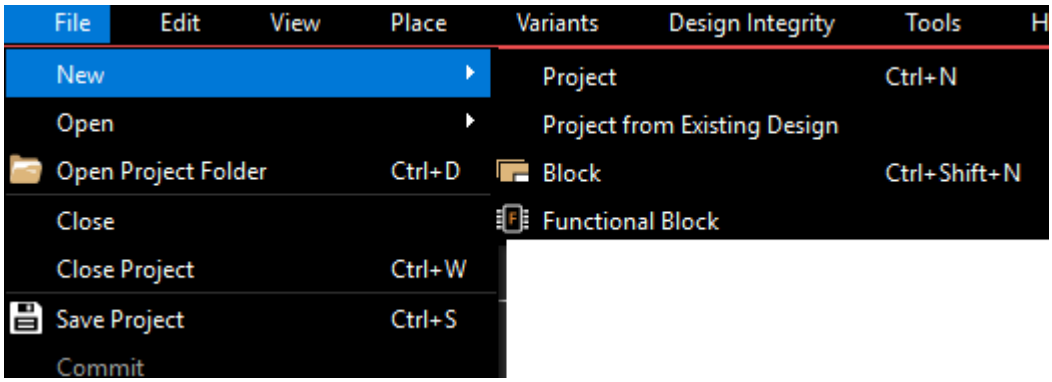
You can:

- Create a new design using an existing DE-HDL design
- Import a DE-HDL design as a block in a hierarchical design
- Import specific sheets from a DE-HDL design

Creating Designs Based on Existing DE-HDL Designs

In DE-HDL, create a project archive using Project Manager. And then open System Capture and choose the following command:

1. *File – New – Project from Existing Design*



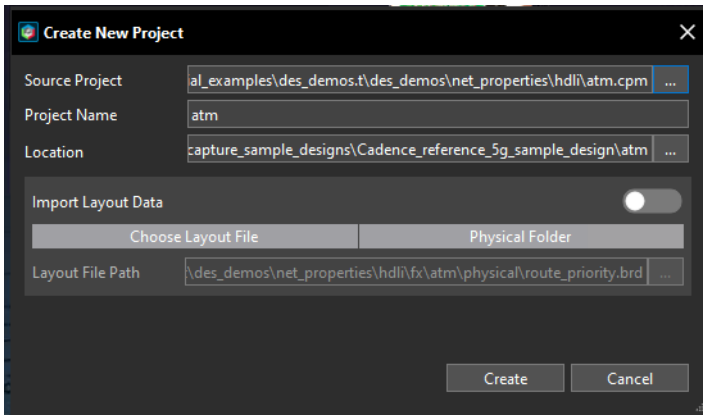
2. Specify the DE-HDL project.

   You can choose any one of the following:

   - DE-HDL design archive

     Or

- Design pointing to a CDS_SITE where all the libraries are stored



The *Project Name* and *Layout File Path* fields are populated automatically based on the selected project.

3. Change the project name, if needed.
4. Specify a location for the new project.

   You can import the layout data for the project `Physical` folder in the selected project or select a specific layout file.

   - To import the compete Physical folder, select *Physical Folder*.
   - To pick a specific board file, select *Choose Layout File*.
5. Click *Create*.

The design is opened in System Capture.

Pay attention to the following before you proceed with the schematic design.

- Notes are added to the design canvas where the unsupported connections have been removed. See the Analyzing the Import Limitations section for the more information on the changes to expect and suggested corrective actions.
- A log file lists the unsupported features and the changes made by the import process. Some of the problems might be reported in the Violations window.

In the System Capture design, the following are included:

- Library data from DE-HDL source
- Local libraries that are referenced in the DE-HDL project
- Project settings for Part Table Files, PPT option sets, and Custom Variables

- Information for relative paths
- DE-HDL design data

Additionally,

- Part information gets cached in System Capture
- Part Manager synchronizes design parts with the reference library
- The pin-to-pin spacing and grid units for the design are not based on the source design. In case you need to enforce the spacing and units from the source design, set the following directive in the `site.cpm`

  ```
  ALLOW_IMPORT_DESIGN_AT_SITE_UNIT 'NO'
  ```

- If `MULTI_FORMAT` and `SquareBracketAsScalars` directives are not in sync.

  The `MULTI_FORMAT` directive in DE-HDL controls how special characters, such as `[ ]`, `< >`, and `()`,are used in pin or net names. When set to on, these characters denote vector signals. System Capture uses `SquareBracketAsScalars` to achieve the same functionality. At the time of import, these two directives are compared.

  Importing a DE-HDL design as a block fails if,

  - `MULTI_FORMAT = on` in DE-HDL design being imported and `SquareBracketAsScalars = on` in the System Capture design
  - `MULTI_FORMAT = off` in DE-HDL design being imported and `SquareBracketAsScalars = off` in the System Capture design
- Compare with red text below
- The '`SquareBracketAsScalars`' directive value is set as the opposite of the `MULTI_FORMAT` directive value to implement the same behavior, that is:
  - If `MULTI_FORMAT` = `ON`

    then

    `SquareBracketAsScalars` = `OFF`

    Net names with special characters in their names are treated as vector nets or buses.
  - If `MULTI_FORMAT` = `OFF`

    then

`SquareBracketAsScalars` = `ON`

Net names with special characters in their names are treated as scaler nets.

Importing a DE-HDL Design as a Block

Some points to note when importing DE-HDL designs as blocks:

- The design being imported must have the same pin-to-pin spacing and compatible grid settings.
- All the libraries in the source design must be available to the target design.
- In case a block being imported contains sub-blocks, all the blocks get imported along with the main block.
- If any block already exists in the destination design, the block is not imported from the source.
- All the data that is a part of the source block, including sheet titles, packaging information, constraints, and block symbols, gets imported with the block. This data can be reused in the target design.
- If the source block does not have a symbol view present, it gets generated when the block is imported. This schematic symbol is available in System Capture for the instantiating the block.
- If `MULTI_FORMAT` and `SquareBracketAsScalars` directives are not in sync.

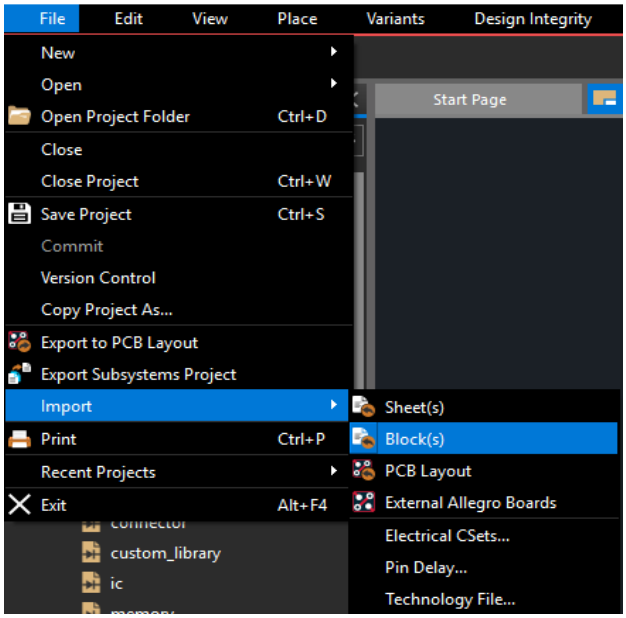
  The `MULTI_FORMAT` directive in DE-HDL controls how special characters, such as `[ ]`, `< >`, and `()`,are used in pin or net names. When set to on, these characters denote vector signals. System Capture uses `SquareBracketAsScalars` to achieve the same functionality. At the time of import, these two directives are compared.

  Importing a DE-HDL design as a block fails if,

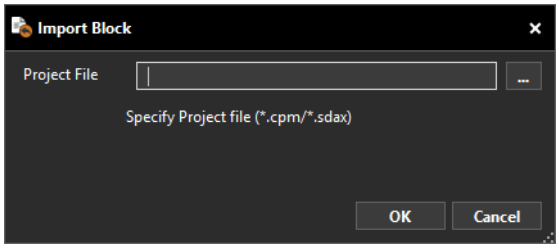
  - `MULTI_FORMAT = on` in DE-HDL design being imported and `SquareBracketAsScalars = on` in the System Capture design
  - `MULTI_FORMAT = off` in DE-HDL design being imported and `SquareBracketAsScalars = off` in the System Capture design
- During import block, the source design net type and scope is retained. That is:
  - If the scope of the net is interface in the source design and a port is connected in the design/sheets being imported then only, the net scope is set to ‘Interface’
  - The type of the Interface net if fetched from the source design only

To import a DE-HDL block:

1. Choose *File – Import – Block(s)*.



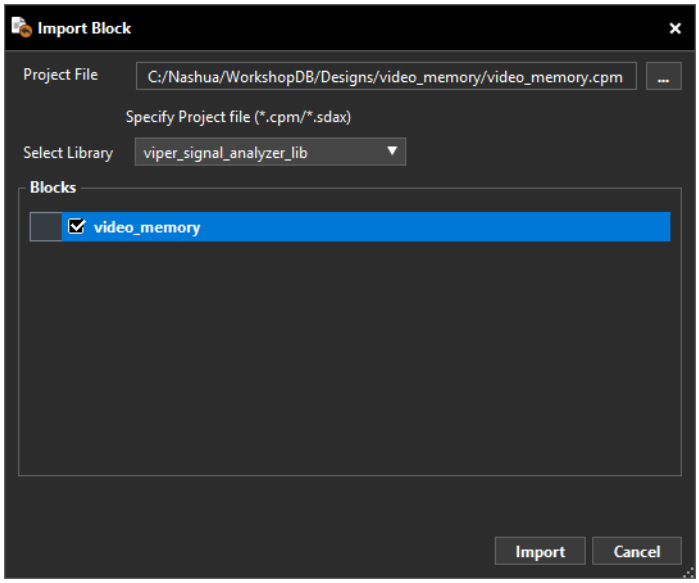
The *Import Block* dialog is displayed.



2. Browse to the DE-HDL project file, such as `video_memory.cpm` project.

   After the project is selected, all the blocks of the project are listed.

3. From the list of blocks, select the blocks to import.

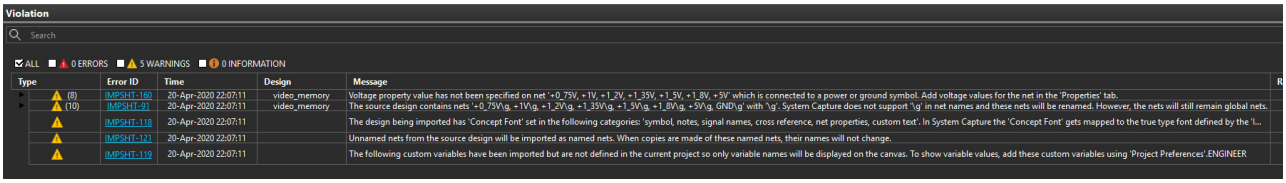


4. Click *Import*.

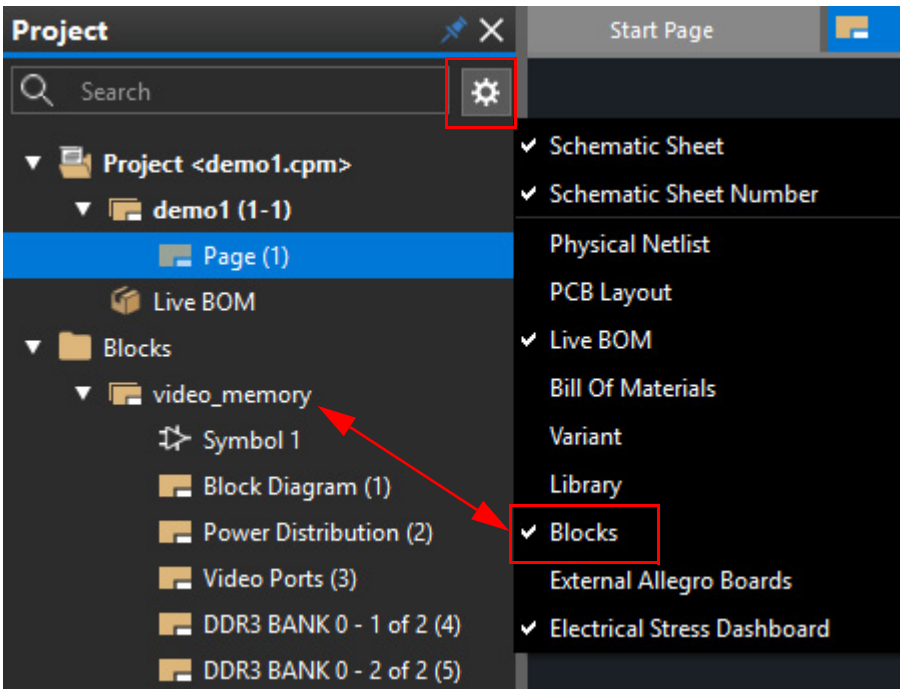
   In case any unsupported features are found, you see a message.

5. Click *View Log* to see the details or check the *Violation Window*.

   For example:



The block is imported and displayed in the Project viewer if the *Blocks* option is selected in the Project viewer display.



If the block is successfully imported without any errors and warning, the symbol for the block is attached to the cursor and is ready to be placed.

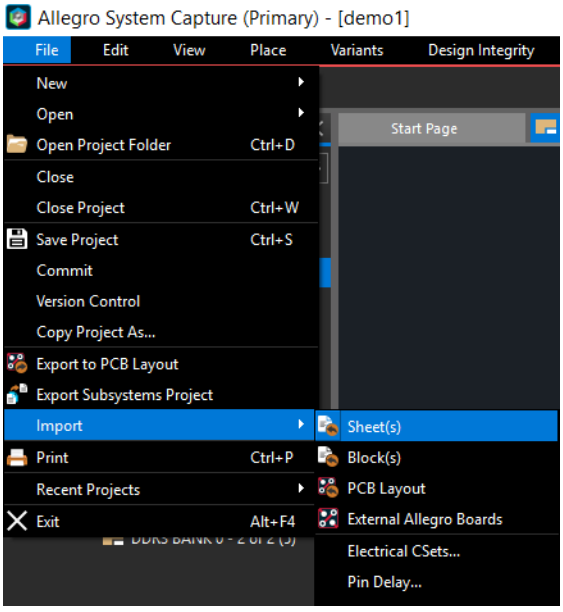
Note: All DE-HDL designs are imported as editable blocks.

Importing Sheets from a DE-HDL Design

You can import sheets from DE-HDL as well as System Capture designs. In this document, the focus is on DE-HDL designs. To import a sheet:

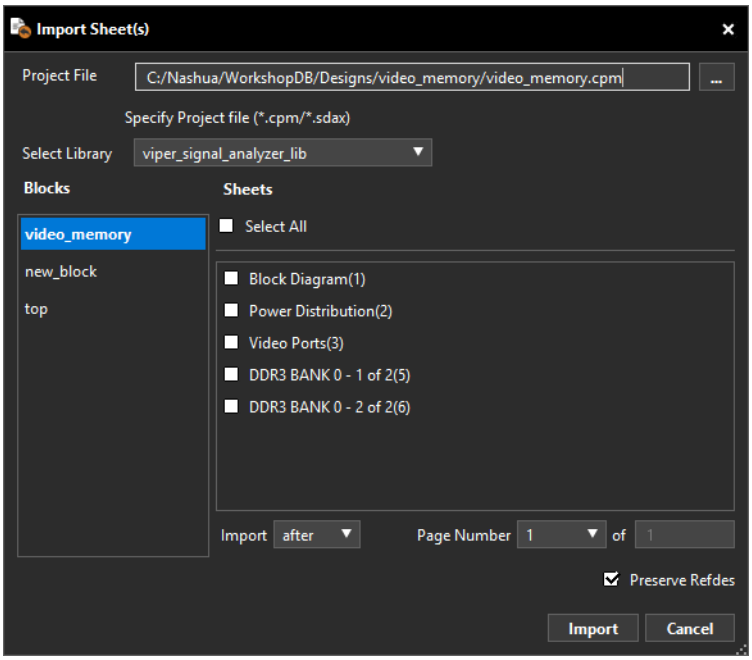
1. Choose *File – Import – Sheet(s)*.

   The *Import Sheet(s)* dialog is displayed.



2. Browse to the folder where the source design is located.

The project data is loaded and the different libraries and blocks are listed.



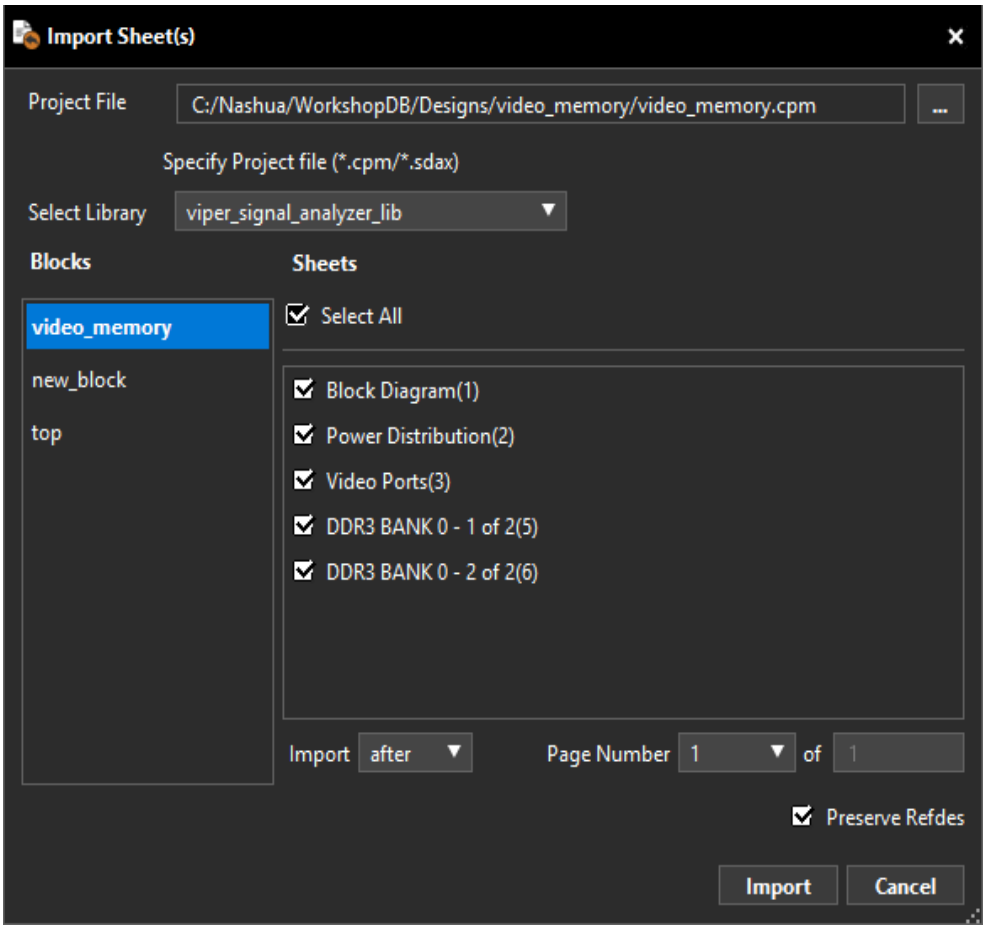
3. Select a block.

   In case there are multiple blocks at the same level, you can import only one at a time.

4. Select the sheets.

5. Specify where using the *Import* drop-down list.

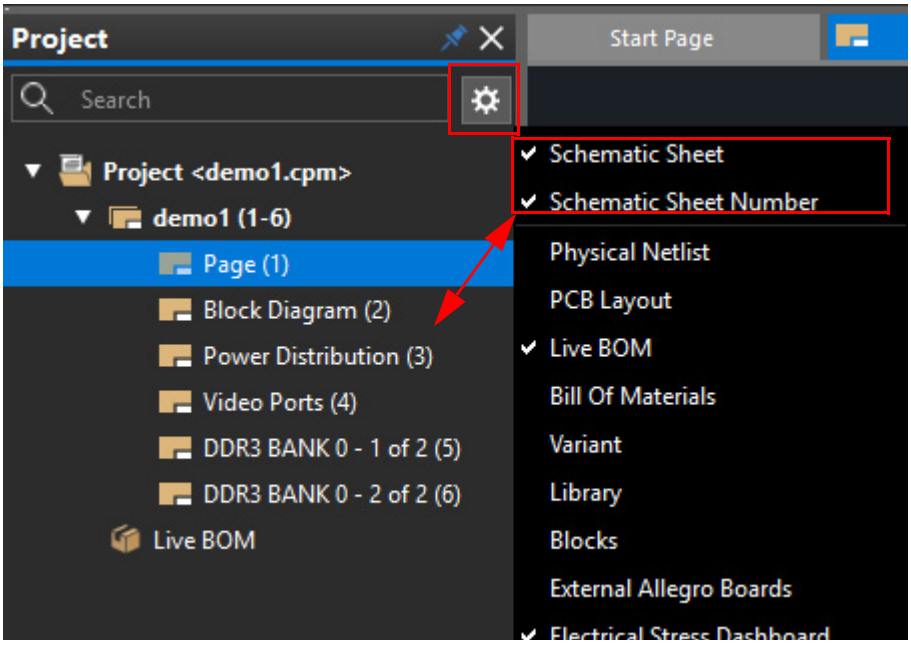
6. Click *Import* to start the import process.



The sheet is imported along with all the packaging data. Any unsupported features found, are listed in the *Violations* Window. A confirmation message provides this information along with the path of the log file for the import process.

7. Close the confirmation message box.

The Project viewer shows the sheets and along with page numbers.



This completes the import of sheets from a DE-HDL design. Note that:

- If Navigation Links are ON, they are recomputed based on the imported sheets.

- XNet overrides on the page are imported.
- In case of a net is connected to a power symbol and port,
  - The net type is retained for interface' and global nets.
  - The power symbols connected to an interface net and port connected to global nets are deleted.
  - Ports can be connected to a local power.
  - The current design scope and type is retained, if net exists in the design. Only in case, the current design has net type as local and the source design has type interface or global the type is changed. Also, for interface net, scope is set to 'IO' in case of mismatch

Analyzing the Import Limitations

When importing designs from DE-HDL into System Capture, the areas where your intervention is needed can be sorted into the following categories:

- Design cannot be imported unless changes are made in the DE-HDL source
- Some elements get imported but changes are needed based on the messages from the Import process
- Design gets partially imported or with minor connectivity loss. You needs to review the reported sections before continuing with the design.
- Some elements of the source design get changed that do not impact connectivity, such as net names or fonts

Design Cannot be Imported

If System Capture finds any of the following in the source design, the import process stops with an error message.

Table 1-1 Unsupported features

Problem Area	What is Expected/Reason	Corrective Action
Design being imported has hierarchical blocks with duplicate pins.	Blocks with duplicate pins are not supported in System Capture.	Remove duplication from the source design.

Table 1-1 Unsupported features

Problem Area	What is Expected/Reason	Corrective Action
Missing libraries Symbol is missing	When importing blocks or sheets, the libraries must be available to the destination design. Component information of the parts places is read from the libraries. An important point to note is that parts used in design must be available in any of the referenced libraries, it does not have to be in the same library as in the source design. Creating Project from DE-HDL project can work without the referenced libraries if all the parts in the source design are from local libraries, that is flat lib or work lib.	Ensure that CDS_SITE includes are the required libraries.
Same block with both full symbol and hierarchical-split symbols	System Capture supports only one type of symbol view for a block.	Ensure only one type of symbol view is instantiated for block.
Merge body symbols	System Capture does not support merge bodies. A note is added to the imported design.	Remove from source
`SIG_NAME` property does not match the connected pin	In System Capture, the `SIG_NAME` property on a pin must be exactly the same as the connected net name	Correct in DE-HDL
NetGroup has 'SIG_NAME' property or is connected directly to a net	In System Capture, NetGroups must be connected to a signal or net using a tap body.	Correct in DE-HDL

Table 1-1 Unsupported features

Problem Area	What is Expected/Reason	Corrective Action
Net object type is different in source vs destination but they have the same names For example: NG_test is a NetGroup in the source and is a scalar net in the destination	Same name cannot be used for different net objects.	Correct in DE-HDL
CTAP symbol is missing	Incoming design has NetGroups but the CTAP symbol is missing from the destination libraries.	Add the libraries and ensure CTAP is available

Imported Elements that Need Checking

The following elements and aspects of a DE-HL design are not supported in System Capture and you have to examine them before continuing with the design.

Table 1-2 Modified design elements

Problem Area	Reason/What Will Happen	Corrective Action
Custom text-related: ■ On page border ■ Display ■ Colors	System Capture handling of Custom text is different from DE-HDL. ■ Custom text on page border is not evaluated and is shown as custom variable. ❑ A warning is displayed after import report. ❑ Also custom text on page border cannot be selected. ❑ If custom text is invisible in DE-HDL on page border, it will still display in System Capture.	Review the changes and correct if needed.

Table 1-2 Modified design elements

Problem Area	Reason/What Will Happen	Corrective Action
	■ In DE-HDL custom text is shown inside <>, in System Capture it is shown as $NAME ■ DE-HDL supports applying different colors on custom text. In System Capture the color is always picked from page border symbol. ■ Custom text on comment-body but not on page border is not supported in System Capture. A warning is issued.	
Components placed outside the page border	System Capture does not support objects placed outside the page border.	To import such designs, move the objects within the page border and import.
Cell that looks like a bus tap symbol but has no BN property	System Capture needs the BN property on tap symbols. Notes are added to the imported design at the locations of the tap symbols.	Add connections with a different tap body if there was connectivity in DE-HDL If it was used just for visual effect and did not affect connectivity, no action is needed.
Bustaps with invalid BN properties	Taps without proper connection or taps with invalid range are deleted.	Check the reported instances before continuing the design tasks
Table of Contents symbols	Page is brought in but without entries.	Contact Cadence for a Tcl script.
Source design has out of sync parts with reference library	Library state of parts is different from design	Run Part Manager

Table 1-2 Modified design elements

Problem Area	Reason/What Will Happen	Corrective Action
Part definition (chips) is out of sync with the destination design / reference libraries	Chips view has different information as compared to design	Run Part Manger
Pins of parts do not match the part in the reference library	Library state of part does not match design	Run Part Manager
Rotated page border	Not supported in System Capture. Rotation will be lost.	Correct the page border symbol
Symbols with custom text	Except on page border, all custom text is lost System Capture evaluates only custom text on page border.	Add Notes in System Capture
Missing Part Table Files	Key and injected properties are no longer valid. All properties are treated as user-defined properties	Add PTFs to the site before import.

Table 1-2 Modified design elements

Problem Area	Reason/What Will Happen	Corrective Action
`Concept Font` is set	Leads to font and text differences. DE-HDL works only with Concept font, whereas System Capture has True Fonts support. The default font for System Capture is Arial in Windows and Helvetica in Linux.	To use different fonts for imported designs, set the font name in the cpm directive `IMPORT_FONT_NAME` in the `CANVAS` section.  *Tip* Preferably, in the site.cpm. When you set `IMPORT_FONT_NAME`, ***all*** fonts get converted to the specified font. For example: If *Arial* is set as the font in DE-HDL, and `IMPORT_FONT_NAME` is set as *Courier,* then on importing all instances of *Arial* font get converted to *Courier*.
Custom variables that are not defined in destination design	System Capture handles only those variables that are on the page border	Add to System Capture design then these variables will be populated.
Voltage value for nets is different in source vs destination	Import cannot overwrite existing values in the destination design so the voltage value there remains unchanged.	Change the voltage value, if needed

Table 1-2 Modified design elements

Problem Area	Reason/What Will Happen	Corrective Action
Unnamed nets	Unnamed nets are not supported in System Capture and such nets get assigned system-generated names and are reported. There is no impact on the netlist. **Note:** In case copies of these unnamed net are made, their name will not be changed.	No action needed
Unnamed signal starting with `UN$`	In DE-HDL, the names of unnamed nets and system nets start with `UN$`, which gets replaced with the PNNs used in the netlist when brought into System Capture, such as `unanmed_` The wires without the `SIG_NAME` property in DE_HDL are actually graphical lines.	No action needed
Nets have invalid voltages	System Capture cannot process the value set in DE-HDL as voltage. Nets will be brought in with voltage property.	Correct in *Properties*.
Voltage missing from nets connected to power or ground symbols	In System Capture, nets connected to power or ground symbols, must have voltage values.	Correct in *Properties*.
Diff pairs not imported during Import Sheet	Constraints and diff pairs are not imported	Add the diff pairs again
Constraints on nets are not imported when importing sheets	Not supported in System Capture	Add the constraints again

Table 1-2 Modified design elements

Problem Area	Reason/What Will Happen	Corrective Action
User-defined properties that are present as injected properties in PTF	Part Manager does not compare user-defined property values with the library properties.	To convert user-defined properties to injected properties, if they exist in the Part table, set the `RESET_INSTANCE_INJECT_PROP` directive to `'ON'` in the `CANVAS` section of the CPM.
Design has 'POWER_GROUP' property assigned	■ If the POWER_GROUP property is assigned property, it is brought into System Capture ■ If the POWER_GROUP is changed in DE-HDL, it will be brought into System Capture. ■ Group changes on instance, will not be brought in ■ Group assignment changes from chips.prt on instance, will be brought in.	Add connectivity to the pins after import.
Components have different POWER_GROUP values	Will not be imported. The POWER_GROUP values are imported only for components that have the same POWER_GROUP values.	Check the reported instances before continuing the design tasks
POWER_PINS property	Gets translated into the power assignment if the schematics power pins matches the power pins in the part definition. If pins are regrouped, this property is not translated.	None

Table 1-2 Modified design elements

Problem Area	Reason/What Will Happen	Corrective Action
NC_PINS property	Will not be imported because it is a reserved property in System Capture.	Check the reported instances and add connections as needed.
BODY_TYPE = COMMENT property	Refdes of component changes/property does not transfer to the component in System Capture. A part with one or more pins with chips view is not recognized as a comment body part System Capture but is recognized as a connectivity part.	Either delete the chips folder for the part in project library or add the property `PACK_IGNORE` with value `TRUE` on the symbol.

The following table lists the design elements that are not completely and exactly replicated in System Capture.

Table 1-3 Design Elements with Loss

Problem	Reason/What Happens	Corrective action
Nets with the following in their names:	Signal name will be different in System Capture. For example: In DE-HDL, if a signal name is `TEST\I`, in System Capture it becomes `TEST`	No action needed

Table 1-3 Design Elements with Loss

Problem	Reason/What Happens	Corrective action
■ `\R (case-insensitive)`	All bits of a vector pin can be connected to a scalar net by using replication (\R) For example: All 4 bits of `PinA<3..0>` have to be connected to net *TEST*. Then add a signal `TEST \R 4` in DE-HDL. All bits of pin get connected to *TEST*. But in System Capture such connectivity is not supported.	Use Alias body.
■ `\I (case-insensitive)`	Nets will no longer be Interface nets. They will be Local nets only.	Apply a port to change to interface net. Based on port type of pin, choose an appropriate port.
■ `\G (case-insensitive)`	Will remain global net	It is recommended that you attach power symbols to such nets to avoid any problems.
■ `!`	Will remain global net	
■ `/`	Will remain global net	
■ `\Base in name`	Will remain the winning net name but the `\base` from its name will be dropped	

Note: All these names with special characters do not go to the netlist in DE-HDL.

Navigation Links /CRefer	System Capture uses a different mechanism for navigation links.	Add manually. There must be a `CREFER.dat` entry in the `CANVAS` section of the CPM.

Table 1-3 Design Elements with Loss

Problem	Reason/What Happens	Corrective action
Block with both full symbol and hierarchical-split symbol views	System Capture supports only one type of symbol view. Here is how it computes which view to import:	
	Both views are available	Hierarchical-split symbol view is imported
	Both views are available but only the *full* symbol is instantiated	Full symbol view is imported
	Both views are available but only the *hierarchical* symbol is instantiated	Hierarchical-split symbol view is imported
Vector pin/port connected to vector net of different width	Connecting vector pins with a net having different width is not supported in System Capture and this connection is broken. Notes are added to the imported design at the locations where the connections have been removed.	Correct the net width to re-establish connectivity.
Power symbols are shorted	Shorting two power symbols is not supported in System Capture. Notes are added to the imported design at the locations where the connections have been removed.	Add an alias body to re-establish connectivity.
Comma separated net names	System Capture does not support comma separated net names, such as: `GND, GND1, GND2, 1V8_TX<1>`. Any segment or net with such a name is ignored	Add the required connectivity

Table 1-3 Design Elements with Loss

Problem	Reason/What Happens	Corrective action
Scalar pin (Ground/VCC) is connected to a bus	Scalar signal cannot be connected to bus or vector pin Notes are added to the imported design at the locations where the connections have been removed.	Replace the note with 'syn1ton' body.
Properties not annotated in the design but read from part table file	Not brought in. Errors might be reported in Constraint Manager.	Annotate the property in DE-HDL before import
Same cell found in multiple libraries	This is not allowed in System Capture. Cells from one library would be skipped during import. A warning message would be given and a warning note would be added at the instance location.	Correct the design to match the netlist with DE-HDL design.

Imported with Changes

The following table lists the situations where you need to review the changes made and make corrections.

Table 1-4 Review the changes made

Element	Reason/What Happens	Corrective Action
Different blocks with identical names exist in both source and destination designs	Different blocks cannot have the same name.	Review the messages from the Import process and choose as needed

Table 1-4 Review the changes made

Element	Reason/What Happens	Corrective Action
NC net is connected to an alias body	Not supported in System Capture. Notes are added to the imported design at the locations of the NC nets.	No impact on connectivity
Power symbol connected to interface net	Connecting interface net to a port and a global power symbol is not supported in System Capture. The power symbol is removed without any loss of connectivity and the net is now an interface net. Notes are added to the imported design at the locations where the connections have been removed.	Check the connectivity to ensure design intent is maintained.
Port symbol connected to global net	Connection between global net to a port and a power symbol is not supported in System Capture. The port symbol connected to this net has been removed without any loss of connectivity and the net is now a global net. Notes are added to the imported design at the locations where the connections have been removed.	Check the connectivity to ensure design intent is maintained.

Table 1-4 Review the changes made

Element	Reason/What Happens	Corrective Action
NC net connected to alias/ synonym symbol	Connection between NC net and an alias body is not supported in System Capture, and has been deleted. This has no effect on the connectivity. Notes are added to the imported design at the locations where the connections have been removed.	Check the connectivity to ensure design intent is maintained.
NetGroups with same names as in destination	In case the parent is same and the members are same, there is no change. In case the parent is different, names in the destination get changed	Review the changes
Font size of Note/Net Name/ Properties increases	In DE-HDL designs, a note is preceded with spaces. The note text is in the Concept font which has a fixed character size, whereas System Capture supports true type fonts, which has varying font size according to the letter. Due to this the space size reduces in System Capture. This makes the note seem incorrectly placed.	Review the changes

Table 1-4 Review the changes made

Element	Reason/What Happens	Corrective Action
Rotated notes	Position and orientation might appear shifted because in System Capture, the notes are rotated around their center. In DE-HDL a rotated note is not processed much and can reach an unreadable state. In System Capture, rotated objects are processed again to ensure readability.	Review the changes
Connection dots shown even for graphical lines	In DE-HDL, graphical lines and wires are same objects, so the graphical lines cross-section has junction dots same as wires. But in System Capture, graphical lines and wires are different objects and graphical lines cross-section does not have junctions dots.	Review the changes
Page title font color and font changes	Unlike DE-HDL, System Capture does not allow editing the reserved custom text entries, such as page titles.	Review the changes
Page titles in different colors	`PAGE_TITLE` is blue in System Capture In DE HDL, most of the sheets have the instance color applied to the custom text and very few have the color from the symbol. In System Capture, the symbol color gets applied to all the custom text. This is a change from DE-HDL, that applies the instance color to custom texts.	Review the changes

Table 1-4 Review the changes made

Element	Reason/What Happens	Corrective Action
NetGroups with different formatting on segments	Different styles can be applied to different unconnected segments in the source design, but System Capture does not support this. At times, the wires may appear thick or thin. One style is applied to all segments of the NetGroup.	Review the changes
Color on junction dot is different from wire	This is not supported in System Capture. The junction dot color will always be the same as the wire color.	No change needed
Signal names placement changes	Due to font translations, the appearance changes.	Check the `IMPORT_FONT_NAME` set. You can adjust the fonts but the problem might persist.
Visible annotated constraints on the DE-HDL canvas	Constraints cannot be added as properties in System Capture so these cannot be shown as attributes and their annotation will also be lost.	No change needed
Color changes	DE-HDL works on 16-bit color and System Capture supports the full RGB range. There may be a slight difference in appearance of colors. Many colors are controlled by the System Capture theme, which offers a ricer display as compared to DE-HDL.	Review the changes

Table 1-4 Review the changes made

Element	Reason/What Happens	Corrective Action
Zooming display	DE-HDL works on custom different zoom levels and System Capture follows the newer, industry-standard zoom behavior. If you do the same zoom in or out, the display is different in both.	Not applicable
Lines and circle shapes	If a connectivity object and a graphical object are placed in the same area, the connectivity objects gets placed on top of the graphical shapes.	To select shapes, send the component back.
BN property with bit range with angular brackets	Values with angular brackets are not supported in System Capture for BN property, that is BN property format '<0..7>' is invalid and will get changed to '0..7'.	
Changed pin number colors or visibility	Pin numbers that are not annotated on canvas do not have any colors applied. DE-HDL by default shows this in red. As these are not annotated we are getting the orange as the default property color for the pins and the same is being assigned.	To ensure the properties are annotated, export the design with the Back Annotate option checked. Once exported, import the design again in the System Capture. Now the pin numbers will be are visible in the System Capture too.

After, going through all the reported messages and changes, you can continue working on the design just as any other design authored in System Capture.

A

Color Mapping for System Capture

Design Entry HDL (DE-HDL) supports 16 colors whereas System Capture supports a much larger number of colors. When a DE-HDL design is imported, these 16 colors are mapped to their nearest matching colors in System Capture. At times, the colors might not be exactly what you require. Additionally, you can benefit from the large number of color choices available in System Capture. This section describes how to:

- Set up the default colors in the CDS_SITE.
- Map colors when the canvas background is changed between dark, black, and white.
- Change the colors for imported designs
- Use a different color than the used in the DE-HDL schematics

You can set the color mapping for each session by running this Tcl command or create a color mapping Tcl file and run it once every session. Or, if running System Capture using a script, source the Tcl file in the script itself.

Important

Color mapping changes are applicable for DE-HDL schematic, that is design, block, or sheet, imported, in that session. There is no impact on native System Capture colors.

Sample Colormap File

The colormap file maps the colors that System Capture uses when importing designs from other authoring tools and when the canvas theme is changed between dark, black, and white.

To set the default colors and fonts, create a text file called `colormap.txt` and place it at:

`<site>/cdssetup/canvas/resources folder`

Here is a sample file that you can use as a starting point:

```
//Give the colors to replace in the section defined for the background color.
//syntax
// Define grid color for each background color
//<background color>
//{
//GRID_COLOR:<grid color>
// <original color > : <replacement color>
// <original color > : <replacement color>
// <original color > : <replacement color>
//}
//SCHEMATIC_GRID_COLOR:<grid color>
// Light : <replacement color> Light
// Mid   : <replacement color> Mid
// Dark  : <replacement color> Dark
//RED {255 0 0}
//GREEN {0 255 0} #00ff00 #ff00ff
//BLUE {0 0 255}
//ORANGE {255 165 0}
//YELLOW {255 255 0} #ffff00 #0000ff
//}


white
{
GRID_COLOR:#CCEDFF
```

```
Light:#B3B3B3
Mid:#999999
Dark:#808080
white:black
#ffff00:#0000ff
#00ff00:#ff00ff
}

#222830
{
GRID_COLOR:#3a5264
Light:#1E2830
Mid:#1B2026
Dark:#14171C
#222830:white
black:white
#ff00ff:#00ff00
#0000ff:#ffff00
}

#000000
{
GRID_COLOR:#3a5264
Light:#1E2830
Mid:#1B2026
Dark:#14171C
#222830:white
black:white
#ff00ff:#00ff00
#0000ff:#ffff00
}
```

Customizing the Color Mapping

You can change the color mapping per session or using a Tcl file.

Changing Colors For Current Session

Follow these steps to specify the changed color for incoming DE-HDL designs.

1. In the command window, set the color mapping using the following Tcl command:

   ```
   setDEHDLImportColorMapping color_name {R G B}
   ```

   For example,

   ```
   setDEHDLImportColorMapping green {0 0 255}
   ```

   ```
   setDEHDLImportColorMapping yellow {255 0 0}
   ```

   This changes green to blue and yellow to red, respectively.

2. Import a DE-HDL design

The colors will be changed as per the new mapping.

Refer to the Allegro System Capture Tcl Commands Reference Guide for details of these and all the other Tcl commands:

- `getDEHDLColorNames`
- `getDEHDLImportColorMapping color_name`

Creating a Mapping Tcl File

When a DE-HDL design is being imported to System Capture, the tool chooses colors that closely resemble the colors in DE-HDL. To select the colors used during import, use the following commands:

- `getDEHDLColorNames`

  Provides a list of colors supported by DE-HDL.

- `setDEHDLImportColorMapping`

  Maps a DE-HDL color to an equivalent System Capture color.

To store these settings, create a Tcl file, such as `importColorMapping.tcl`, with all the color preferences and place it in:

`<site>/cdssetup/canvas/resources/syscap folder`

This mapping applies to importing a new design, sheet, and block.