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System Connectivity Manager Known Problems and Solutions

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Contents

System Connectivity Manager Known Problems and Solutions

System Connectivity Manager (SCM) known problems and solutions (KP&S) will be reviewed and updated when new issues arise.

Status of Problems Reported in Earlier Releases

The following problems reported in previous releases are valid for 23.1 as well.

CCMPR01339523: SCM needs to find out a way to let the user know if a design is already open

Description: Even if a System Connectivity Manager design has already been opened by one user, SCM allows another user to work on it because SCM does not generate a .lck file to prevent another user from opening the design.

Workaround: None

CCMPR00866657:Allow adding a differential pair property in a DE-HDL block that is opened from System Connectivity Manager

Description: When you launch a block from SCM in Design Entry HDL, you cannot add a differential pair to it.

Workaround: Launch the standalone version of Design Entry HDL to add and edit differential pairs.

CCMPR00685188: Logical name of aliased signals is not displayed in the exported schematics

Description: Exported schematics work on the physical design and the alias signals are not tracked. Only the base net names are used and displayed in the exported schematic.

Workaround: Schematic Generator works off the physical database of the design (base nets in terms of connectivity data structures). As a result, it does not have any information about alias nets — only the winning base net is considered for all routing purposes. From a design point of view, the generated board contains only the base net and not its aliases. Thus, there is no loss of information.

CCMPR00685623: Routing not getting completely preserved

Description: During Schematic Generation, sometimes, the preserve mode does not behave as expected. Manually routed connections may not be preserved completely.

Workaround: Manually reroute the connections in Design Entry HDL.

CCMPR00660174: Bypass capacitors may not be evenly distributed amongst the rails

Description: When you generate a schematic with a large number of bypass capacitors, bypass capacitors are not evenly distributed amongst the rails.

Workaround: Edit the rails manually in Design Entry HDL.

CCMPR00492705: Deleting all the members of a match group does not delete the match group object in Constraint Manager opened from System Connectivity Manager

Description: If you delete all the members of a match group, the match group object is not automatically deleted in Constraint Manager launched from System Connectivity Manager.

Workaround: Manually delete the match group in Constraint Manager.

CCMPR00563512: The MSB and LSB of vector signals display incorrectly in the Component Connectivity Details Pane

Description: If you connect the MSB of a vector pin to the LSB of a vector signal or vice versa, the connection displayed in the Component Connectivity Details pane is incorrect. For example, if you connect `pin<8..0>` to `signal <0..8>`, the display changes to `signal<8..0>`. Expanding the signal however displays the correct connections.

Workaround: None

CCMPR00584192: Different PNN vector nets are added in blocks on updating connectivity in SCM

Description: When you add a vector net on a physical design that spans a hierarchy in an SCM logical design, on when running Import Physical, an interface net is not created and the nets are added with different Physical Net Names (PNNs) for each hierarchical block.

Workaround: None

CCMPR00587917: Issues with updating multi-section and split parts and their connectivity in SCM

Description: If you make any changes to split or midsection parts in a physical design, on running Import Physical, the changes are not updated if the section or split part is not in the SCM design. In midsection parts, an incorrect section is added; for split parts, symbols are not added.

Workaround: Ensure that the symbols for the sections are in the SCM design before you update changes made in the physical design.

CCMPR00588817: In-context changes are not retained in the same session when a block is reloaded

Description: If you make any in-context changes to a block, the changes are not retained if you reload the block in the same session.

Workaround: Relaunch SCM and then reload the block. The changes are retained.

CCMPR00600321: You are unable to cross-probe from the Physical View to board

Description: Cross-probing does not work in the following cases:

- Selecting a component in the physical view does not highlight it in the board file.
- Selecting components in the Physical View does not highlight them in the Constraint Manager.
- Changing the selection of components/nets in Constraint Manager does not change the selection in the Physical View of System Connectivity Manager.

Workaround: Use cross-probing from the Logical View for System Connectivity Manager.

Problem: Tooltip displays user-defined differential pair for all types of differential pairs within blocks

Description: SCM treats differential pairs ports of a block as “user-defined”. Therefore, tooltips display the differential pair type as “user-defined.”

Workaround: None

Problem: POWER_GROUP property is not updated on aliasing a net or running Import Physical

Description: The POWER_GROUP property is not updated when you alias a net or rename a net in a physical design and then do an Import Physical operation.

Workaround: Update the POWER_GROUP property after aliasing the net or running Import Physical.

Problem: Comments on nets and components are not displayed on replacing the component.

Description: On replacing a component, the comments on the component or the nets are not displayed because the user interface is not refreshed.

Workaround: Close the tab and then reopen it. The comment list is refreshed and displayed.