

# **Working with DCI Cascading**

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# Contents

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<u>Preface</u> .....	7
<u>Working with DCI Cascading</u> .....	9
<u>Determining Master and Slave Banks in FSP</u> .....	9
<u>Enabling DCI Cascading</u> .....	10
<u>Specifying DCI I/O Standards</u> .....	12
<u>Preserving VRP/VRN Pins</u> .....	13
<u>Running Synthesis</u> .....	13
<u>Before Running Synthesis</u> .....	13
<u>After Running Synthesis Process</u> .....	14
<u>Assigning Use Bank Setting</u> .....	14
<u>Changing Master Bank</u> .....	16
<u>Exporting Constraints</u> .....	16
<u>Importing Constraints from an External File</u> .....	17

## Working with DCI Cascading

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# Preface

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This document describes the use of digital controlled impedance (DCI) cascading in Allegro® FPGA System Planner (FSP).

This application uses the following terms, definitions, and abbreviations.

- DCI – Digitally controlled impedance is the technology that eliminates the need for termination resistors on a board, reduces board routing difficulties and component count, and improves signal integrity.
- I/O – Input/output
- Intervening Bank – A bank which exists between the master and slave banks.
- Master Bank – A bank in which an N reference pin (VRN) is connected to the VCCO by a reference resistor, and a P reference pin (VRP) is connected to ground by another reference resistor. In FSP, when you use DCI cascading, the VRN/VRP pins are preserved in the master bank. Preserving the VRP/VRN pins in the master bank represents that you can connect these pins to external reference resistors in schematics.
- Slave Bank – A bank which uses DCI standards with the same impedance from master bank, without connecting the VRN/VRP pins to external reference resistors. Instead, you can use the VRN/VRP pins as general purpose I/Os in a slave bank. In FSP, when you use DCI cascading, you are allowed to use the VRN/VRP pins as general purpose I/Os.
- VRN/VRP – These are multi-purpose reference pins. DCI uses these pins in a master bank to control the impedance of the driver or the parallel termination value for all of I/O pins in master banks.

This document explains DCI cascading concepts using Xilinx Virtex 6 FPGA as a reference; however, the information is applicable for other FPGAs as well. This document does not cover DCI cascading and associated I/O DRC rules. It is assumed that you are familiar with the basic DCI cascading and I/O DRC rules. For detailed information, see the [Xilinx handbook](#) for the respective FPGAs.

# **Working with DCI Cascading**

## Preface

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# Working with DCI Cascading

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When a DCI I/O standard is allocated to a bank, the two multipurpose reference pins, VRN/VRP, pins cannot be used as regular I/Os. Instead, these pins should be connected to external reference resistors. The N reference pin (VRN) must be connected to VCCO by a reference resistor, and the P reference pin (VRP) must be connected to ground by another reference resistor. DCI adjusts the impedance of the I/O to match the impedance of the external reference resistance. The other banks such as slave banks in the same column can use the DCI standards with the same impedance from the master bank, without connecting the VRN/VRP pins to external resistors.

**Note:** DCI cascading is supported for Xilinx's Virtex-5, Virtex-6, Virtex-7, and Kintex-7 family devices. There are several rules that are followed to support DCI cascading across the IO banks of these FPGA devices. Some rules are common for all the FPGA family devices, whereas some rules are specific to each family of FPGAs.

## Determining Master and Slave Banks in FSP

When you enable the Use DCI Cascading feature, master and slave banks may not always be determined automatically after synthesis. In this case, to determine the master and slave banks manually, you can either use the Use Bank setting or import the DCI cascading details from a constraints file.

For more information on how to:

- Use the DCI cascading feature, see the Enabling DCI Cascading section.
- Use the Use Banks settings, see the Assigning Use Bank Setting section.
- Import constraints, see the Importing Constraints from an External File section.

When you run the synthesis process (with Use DCI cascading enabled), the slave bank(s) are determined first. During synthesis, the I/O pins are completely occupied followed by the VRP/VRN pins of the banks that are in the same column. Of these banks, any bank whose VRP/VRN pins are occupied is declared as a slave bank; however, the slave bank should contain at least one DCI I/O standard. If there are more banks in which VRP/VRN pins are occupied all those banks are considered to be slave banks. Once the slave banks are determined, the master bank is determined based on the DCI cascading rules supported by the respective FPGA family devices.

## Working with DCI Cascading

### Working with DCI Cascading

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In a column, there may be multiple banks that are eligible as master banks for the slave banks. In this case, a master bank is determined based on the following rules:

- If a master bank already exists in the device (or column) that is compatible with the new slave banks, the existing master bank is selected for the slave banks. By default, this rule has the highest priority.
- An empty bank in which either or both the VRP/VRN pins are preserved and are compatible with the new slave banks is eligible to be the master bank.
- A bank in which the VRP/VRN pins are not preserved and are compatible with the new slave banks is eligible to be a master bank.
- An empty bank is eligible to be a master bank. This rule has the least priority.

**Note:** FSP consider all the rules above with the corresponding DCI cascading rules.

**Note:** While following the above rules, FSP checks for compatible banks that are above or below the slave banks and that can be defined as a master bank.

A master bank is also determined based on the availability of intervening banks. There are various rules associated with the intervening banks that FSP follows to determine a master bank. For more information on the rules, refer to the Xilinx FPGA family's handbook.

After determining a master bank, you can change the master bank with other banks. FSP provides you a list of bank names that are eligible master banks. You can select a bank from the list and set that bank as a master bank.

The VRP/VRN pins of a master bank do not appear in the Power Connection window.

## Enabling DCI Cascading

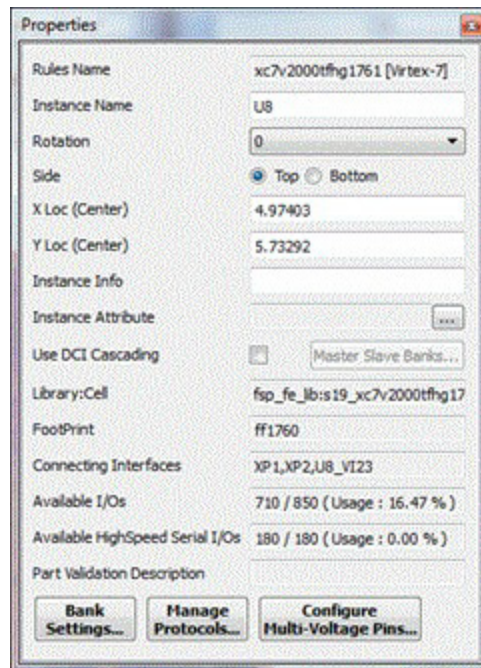
To use DCI cascading, first enable the DCI Cascading feature. To enable this feature, do the following:

1. Right-click the device and choose *Instance Properties*. The Properties dialog box appears.

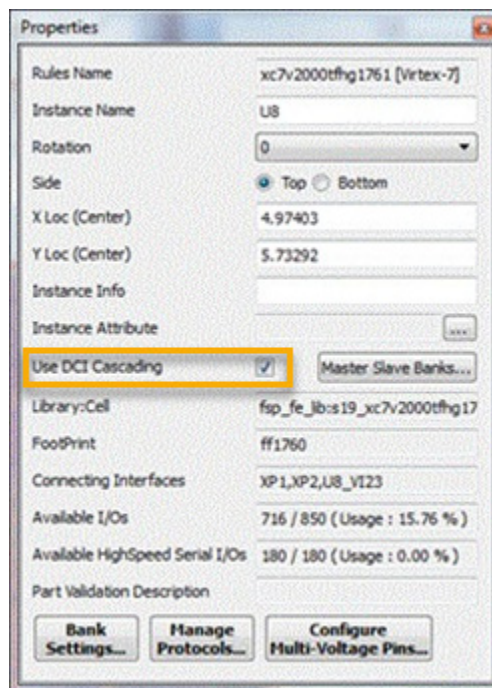
## Working with DCI Cascading

### Working with DCI Cascading

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2. Select *Use DCI Cascading*.



**Note:** To disable DCI cascading, deselect *Use DCI Cascading*. When you deselect the box, a confirmation window appears prompting you about the removal of all the DCI IO

standard signals in the design.

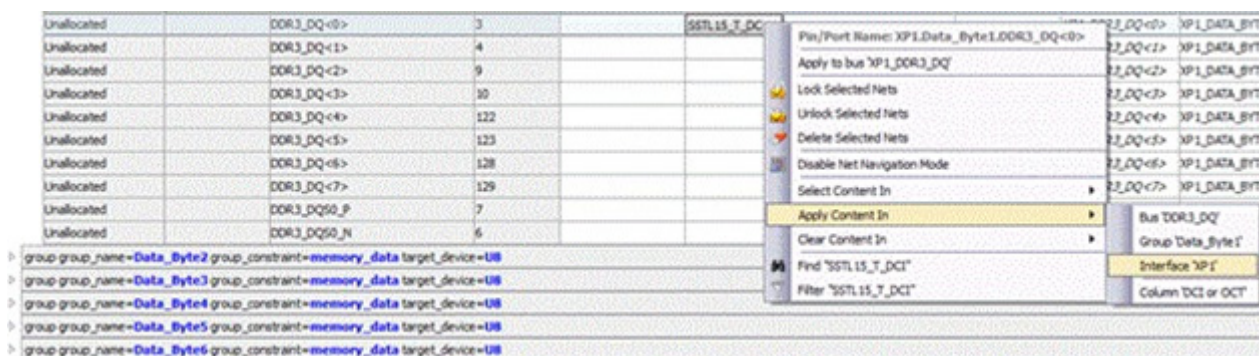
## Specifying DCI I/O Standards

Before running the synthesis process, you must specify DCI I/O standards in the interface instance. To specify DCI I/O standards, do the following:

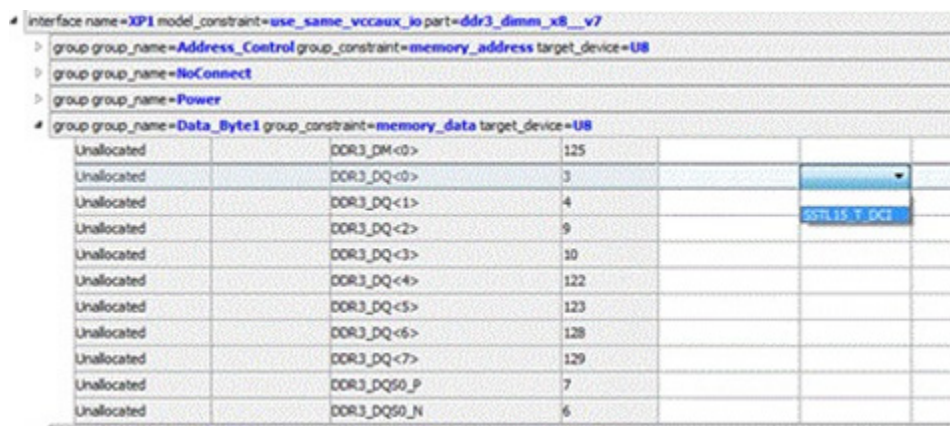
1. Click *Design Connectivity Window* in the toolbar.

In Design Connectivity Window, click > to expand the interface instance node and group nodes.

- 2. Under the DCI or OCT column, select a DCI I/O standard from the drop-down list.**



**Note:** To quickly apply the selected DCI I/O standard to all the pins of the interface, right-click on the cell and choose *Apply Content In – Interface <interface name>*.



After specifying the DCI I/O standards, you can do one of the following tasks:

- ❑ Preserve VRP/VRN Pins

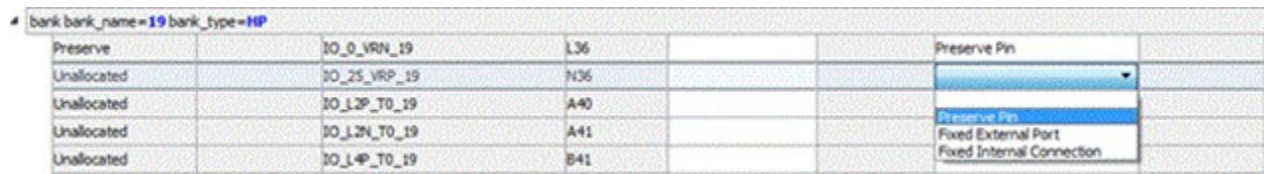
- ❑ Run the Synthesis Process

## Preserving VRP/VRN Pins

You can define any bank as a master bank. This is useful if you do not want FSP to automatically determine the master bank during synthesis. Preserve the VRP/VRN pins in a bank to define it as a master bank.

To preserve the VRP/VRN pins, do the following:

- Under the Connection Type column in Design Connectivity Window, select *Preserve Pin* from the drop-down list for both the VRP/VRN pins.



bank	bank_name	bank_type	Connection Type
Preserve	IO_0_VRN_19	L36	Preserve Pin
Unallocated	IO_25_VRP_19	N36	Preserve Pin
Unallocated	IO_12P_T0_19	A40	
Unallocated	IO_12N_T0_19	A41	
Unallocated	IO_14P_T0_19	B41	

## Running Synthesis

Run the synthesis process to enable the DCI cascading.

## Before Running Synthesis

You must remember the following points before running the synthesis process:

- If you have not preserved the VRP/VRN pins, the master bank is automatically determined based on the connections and availability of slave banks. For more information on how a master bank is determined, refer to the Before you Begin section.
- If you have preserved the VRP/VRN pins in a bank, the bank is considered to be a master bank.

To run the synthesis process, do the following:

1. Choose *Design – Run*.

The Process Options Editor dialog box appears.

2. Click *Run* to run the synthesis process.



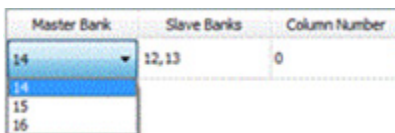
## After Running Synthesis Process

When synthesis process completes, you may notice the following:

- If you had preserved the VRP/VRN pins, FSP displays the master bank and slave banks information in the corresponding bank-level nodes in Design Connectivity Window as shown in the following figure.

```
bank_instance bank_name=12 bank_number=12 bank_vcco_voltage=1.5 bank_vref_voltage=0.75 do_master_bank=14
bank_instance bank_name=13 bank_number=13 bank_vcco_voltage=1.5 bank_vref_voltage=0.75 do_master_bank=14
bank_instance bank_name=14 bank_number=14 bank_vcco_voltage=1.5 bank_vref_voltage=0.75 do_slave_banks=12,13
```

- If you have not preserved the VRP/VRN pins, FSP may determine the master and slave banks; however, you can see a list of banks that are suitable to become master banks. To see the list, click Master Slave Banks in the Properties window. You will notice a list of banks names under the Master Bank column as shown in the following figure.



## Assigning Use Bank Setting

If the master and slave banks are not determined after synthesis, you can use the VRP/VRN pins by targeting all the pins of a group or an interface to a specific bank. This task will help you to use all the pins including VRN/VRP pins in a bank. When the VRP/VRN pins in a bank are used, the bank is automatically considered to be a master bank in the same column.

To set the Use Bank setting, do the following:

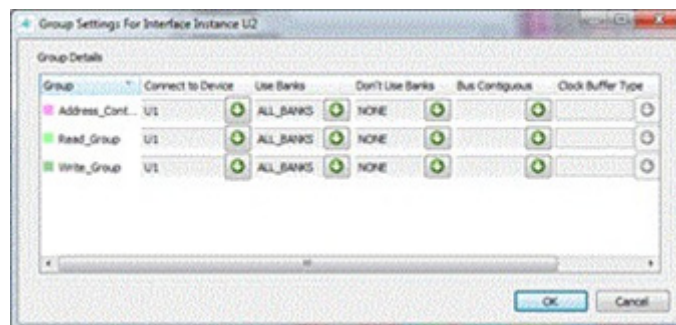
1. Right-click on the Interface Instance. The Properties dialog box appears.

## Working with DCI Cascading

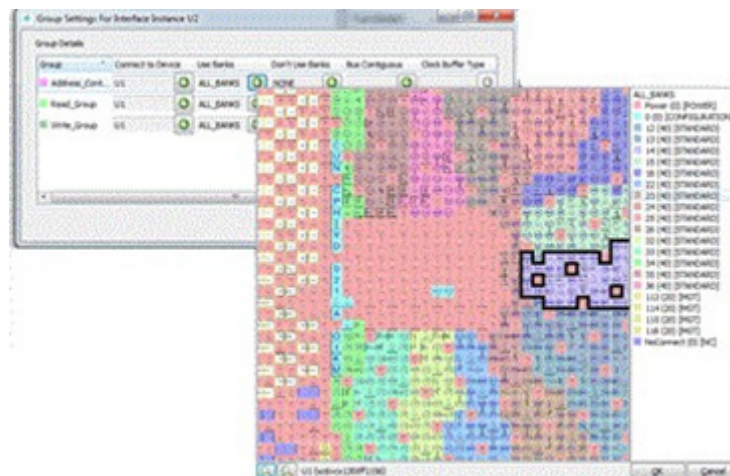


- 2. Click Group Settings.**

The Group Settings for Interface Instance <instance\_name> dialog box appears.



- 3.** Click on the *Use Banks* column name and click on any drop-down button.



4. Select a bank name from the list and click *OK*.
5. Click OK in the Group Settings for Interface Instance <instance\_name> dialog box.

After defining the Use Bank settings, run the synthesis process again.

## Changing Master Bank

After synthesis process completes, master and slave banks are determined. FSP provides an option to change the master bank. This means that you can select a different bank as a master bank that is compatible with the existing slave banks.

To select a master bank, do the following:

1. Click *Master Slave Banks* in Properties of the device instance.

The DCI Master Slave Banks dialog box appears.

2. Under the Master Bank column, select a bank from the drop-down list.
3. Click OK.

**Note:** The Slave Banks column displays the bank numbers of the slave banks that are compatible with the master bank.

The Column Number column displays the column number in which the master and slave banks exist.

## Exporting Constraints

After you define the DCI cascading connections, you can export the DCI cascading information, such as master and slave banks names to a constraint file. These details are exported with the pin assignments. When you export constraints, the DCI cascading information for every master-slave group with compatible I/O standards is exported to the constraint file.

You will notice the following syntax in the constraint file:

```
CONFIG DCI_CASCADE = "<dci_master bank><dci_slave bank1>< dci_slave bank2>..." ;
```

<dci master bank> is the device bank number which is determined as master bank.

<dci\_slave bank1><dci\_slave bank2>.. are the device bank numbers that are determined as slave banks for the <dci\_master bank>.



## Importing Constraints from an External File

You can also define the DCI cascading connections, such as master bank and associated slave banks, by importing the DCI cascading information from an external file. You can perform this task either at the beginning of the design, i.e., after you have placed the instances on the canvas or if the master and slave banks are not determined after running the synthesis process.

Before you import the constraints, ensure that the DCI cascading syntax information is present in the external file and the Use DCI Cascading option is selected in the Properties window of the device instance. When you import constraints, the first bank number in the syntax is considered to be the master bank, and the VRP/VRN pins of that bank are preserved. This implies that the bank is set as a master bank; however, the bank is determined as a master bank after the synthesis process completes.

You should remember the following points when you import constraints from an external file:

- When you import constraints, you will notice that the Preserve value is not set for the VRP/VRN pins in the master bank under the Status column; however, they are considered to be preserved and will not be used for any connections. If you run constraint optimization on the device, the bank in which the VRP/VRN pins are chosen to be preserved will be set as a master bank; however, if you run the entire design, the master banks are determined after completion of synthesis.
- After running synthesis, it is not mandatory that banks that are set as master banks in the constraint file will be set as the master banks unless there are any compatible slave banks available near the master banks. FSP may select other banks as the master bank; however, you may change the master bank to the bank specified in the external file using the DCI Master Slave Banks dialog box.
- When you import constraints, the VRP/VRN pins will be preserved even though the master bank that is determined by FSP is not the same as the master bank specified in the external file. It is recommended that you not preserve the VRP/VRN pins.
- You can also specify the 'Assign to Pins' constraint in the constraint file. This option is useful when you want to assign signals on the VRP/VRN pins of the slave banks. If you assign signals on the VRP/VRN pins and if there is at least one DCI standard signal assigned in the same bank then you should enable the Use DCI Cascading option. If you do not enable this option, you may get incorrect pin connections.
- If the DCI Cascading syntax in the constraint file contains one bank number then the master bank information is ignored and the Use DCI Cascading option in Properties is enabled.

To import constraints from an external file, do the following:

## Working with DCI Cascading

### Working with DCI Cascading

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1. Right-click on the device instance and choose *Constraints – Import Constraints*.

The Select Constraints File dialog box is displayed.

2. Navigate to the file that you want to import, select the file, and click *Open*.

The Import Constraints for Device Instance dialog box is displayed.

3. Select the appropriate options to import.

4. Click *OK* to import constraints.

For detailed information on how to import constraints from an external file, see the Allegro FPGA System Planner User Guide section.

After you import the constraints, you can either run the synthesis process for the complete design or run it for individual groups or interfaces.