cadence®

High Speed Package Flows

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Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor.

Contents

Using 3D Extraction and Simulation Capabilities in Allegro Package SI

This tutorial describes a Synchronous Switching Network (SSN) analysis flow using 3D extraction functionality in Allegro Package SI.

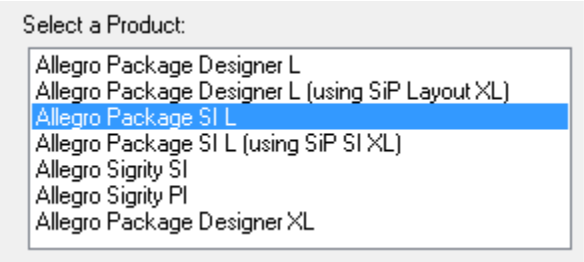
Important

Before you begin, ensure that you have Sentinel-NPE field solver from ANSYS Inc. installed on your operating system.

1. Create a directory on your hard drive; for example: `APD_SSN_tutorial`.
2. Access the sample database, `ssn_demo.mcm`, at the following location in your installation hierarchy:

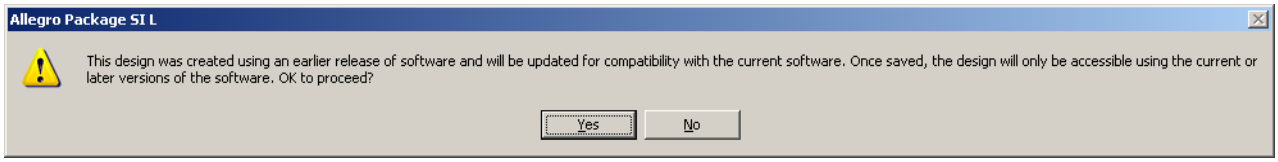
   `<install_dir>\doc\HS_Pkg_flows\examples`
3. Copy the database into the directory you created.
4. Run *apd*.
5. Choose *Allegro Package SI L* and click *OK*.

Figure 1-1



6. Open `ssn_demo.mcm`.

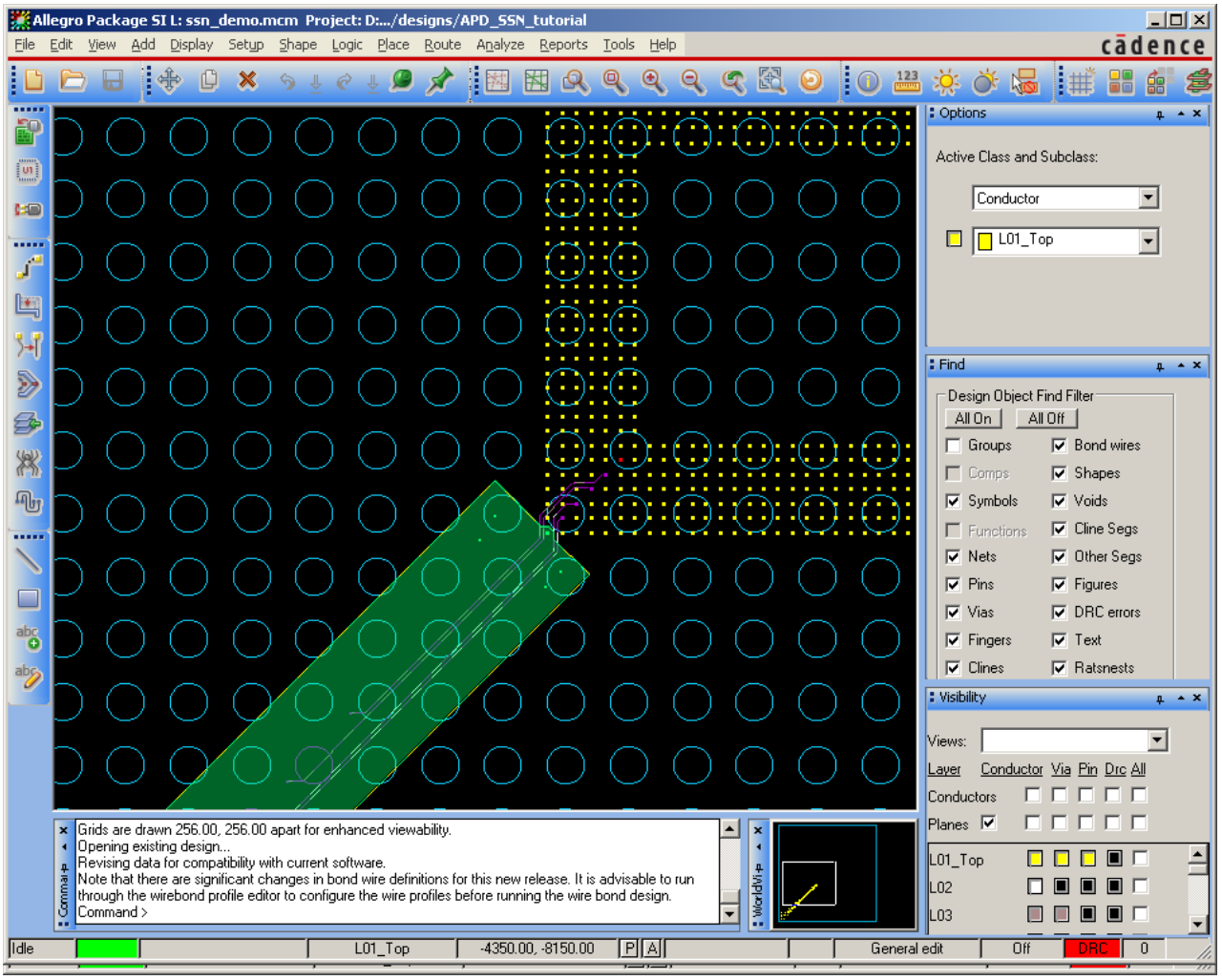
Figure 1-2



7. Click *Yes* when prompted to upgrade the design to the latest version of the software.

There are four signals and one power/ground net, as shown in Figure 1-3.

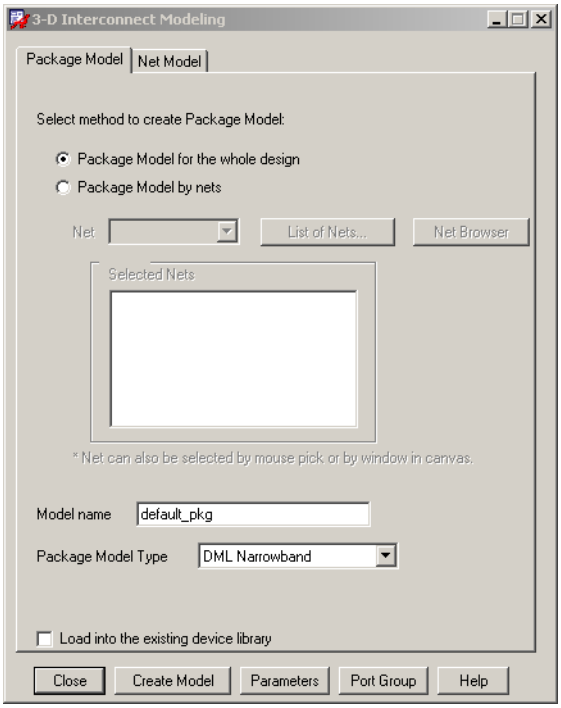
Figure 1-3



8. Choose *Analyze – 3-D Modeling*.

The 3-D Interconnect Modeling form opens, as shown in Figure 1-4.

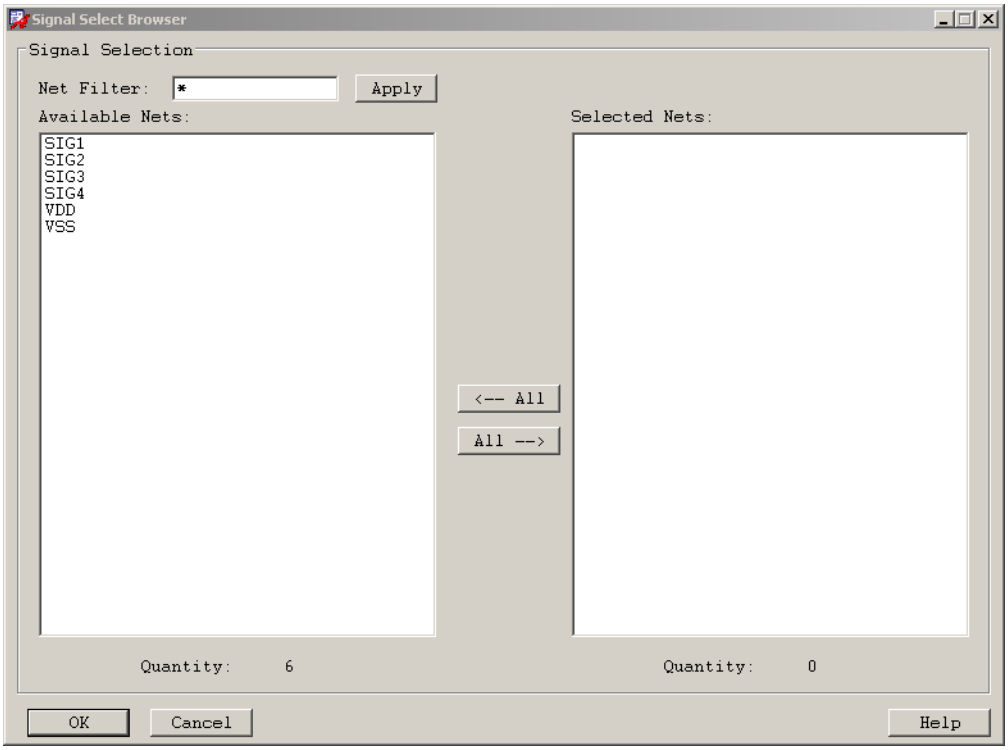
Figure 1-4



9. In the Net Model tab, click *Net Browser*.

The Signal Select Browser opens, as shown in Figure 1-5.

Figure 1-5



10. Select net VDD in the *Available Nets* window and click *OK*.

11. In the 3-D Interconnect Modeling form, click *Parameters*.

The 3-D Modeling Parameters form opens.

12. Fill in the following parameters in the *General* tab of the form:

- ❑ Solder Ball Location: Auto-detect
- ❑ Design unit: 1000MHz
- ❑ Number of coupling nets:1
- ❑ Minimum via diameter: 50um
- ❑ Ignore void diameter: 0um
- ❑ RL mesh density: Fine
- ❑ CG mesh density: Fine
- ❑ CG planar boundary box: Medium
- ❑ CG z-directional boundary box: Medium

- ❑ Enable multiport: YES
- ❑ Controlled sources in model: YES
- ❑ Number of subcircuit segments: 5
- ❑ Start frequency: 0MHz
- ❑ Number of frequency ports: 256
- ❑ Frequency sweep scale: Linear
- ❑ Reference impedance: 50ohm

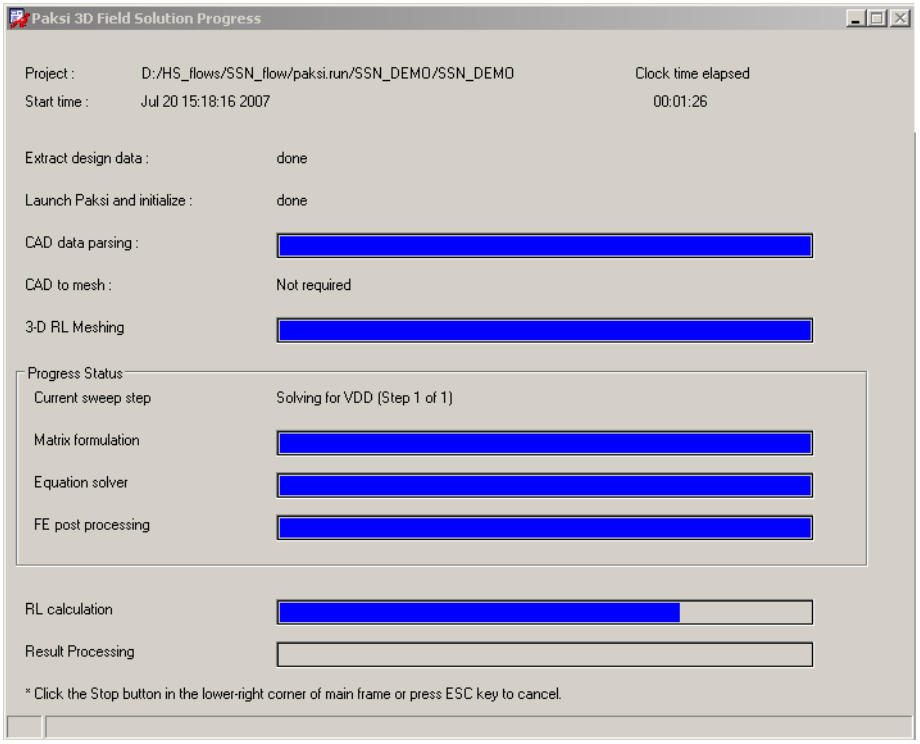
13. Click *OK* to close the Parameters form.

14. In the 3-d Interconnect Modeling form, set *Model name* to `ssn_vdd`.

15. Select `DML narrowband` in *Net Model Type*.

16. Click *Create Model* to start 3D model extraction. The process window is shown in Figure 1-6.

Figure 1-6



When the extraction finishes, a messages appears indicating that the 3D model of net VDD was successfully created.

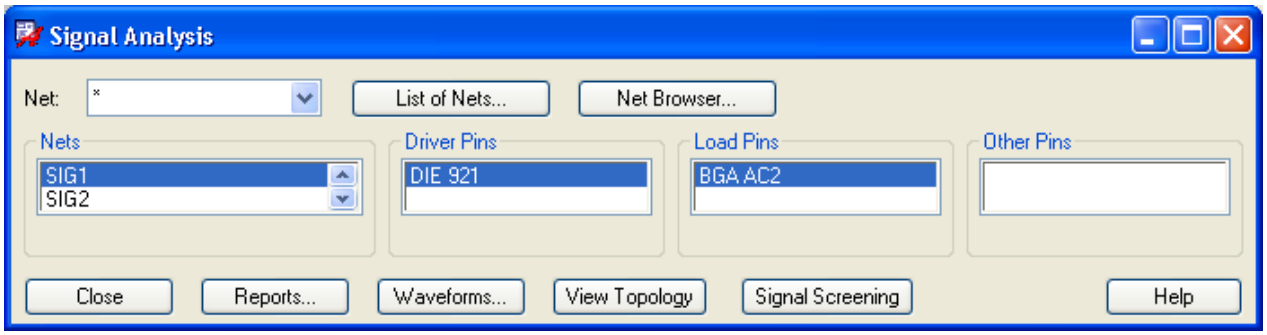
17. Repeat steps 10 through 16 to create a model for net VSS.

18. Select *Analyze – Probe* in the menu bar of Package SI.

The Signal Analysis form opens

19. Select * from the *Net* drop-down list to display the signal nets, as shown in Figure 1-7.

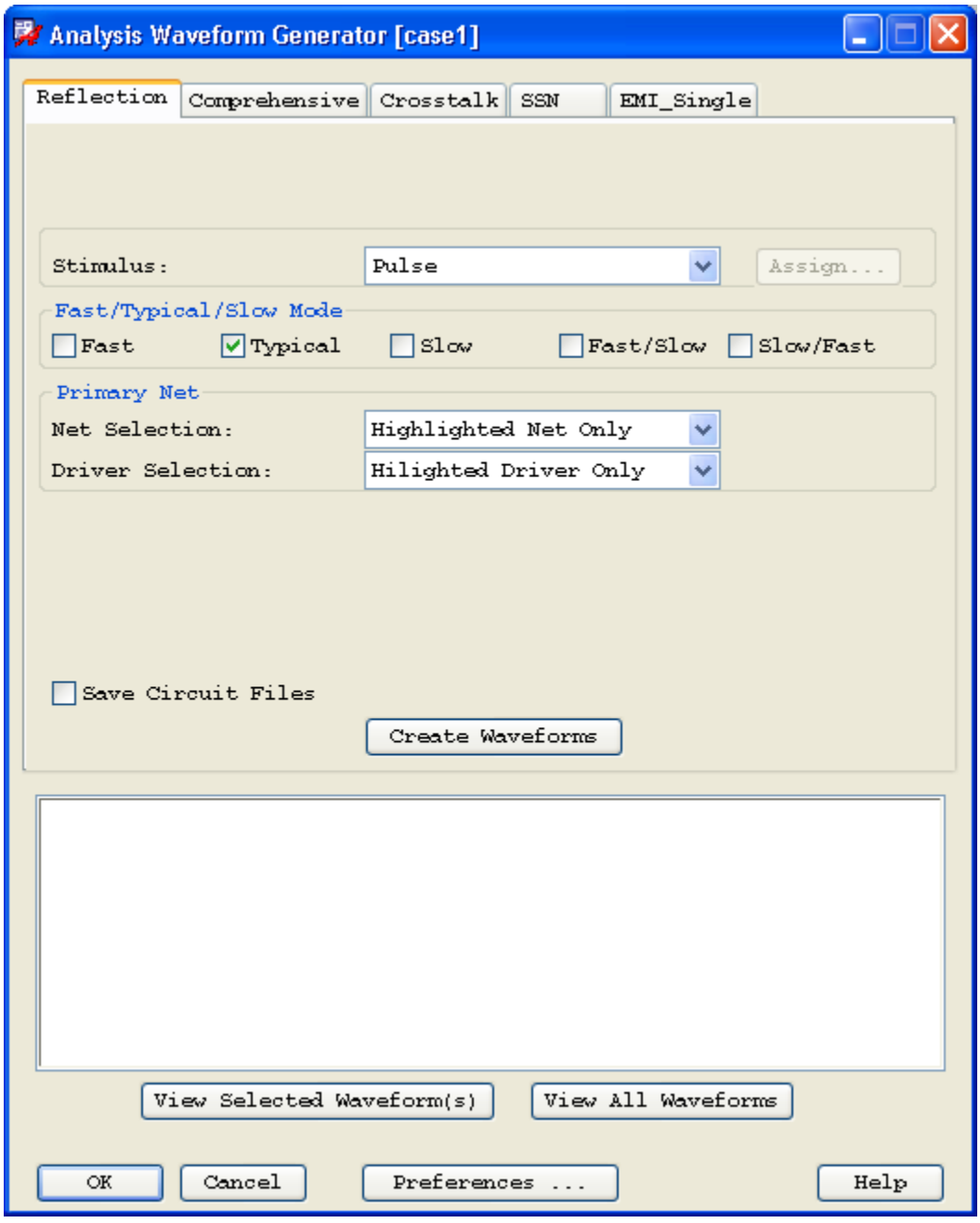
Figure 1-7



20. Select one signal bus from the *Nets* list. The others will be included automatically when you run an SSN analysis.

21. Click *Waveforms* to open the Analysis Waveform Generator, shown in Figure 1-8.

Figure 1-8



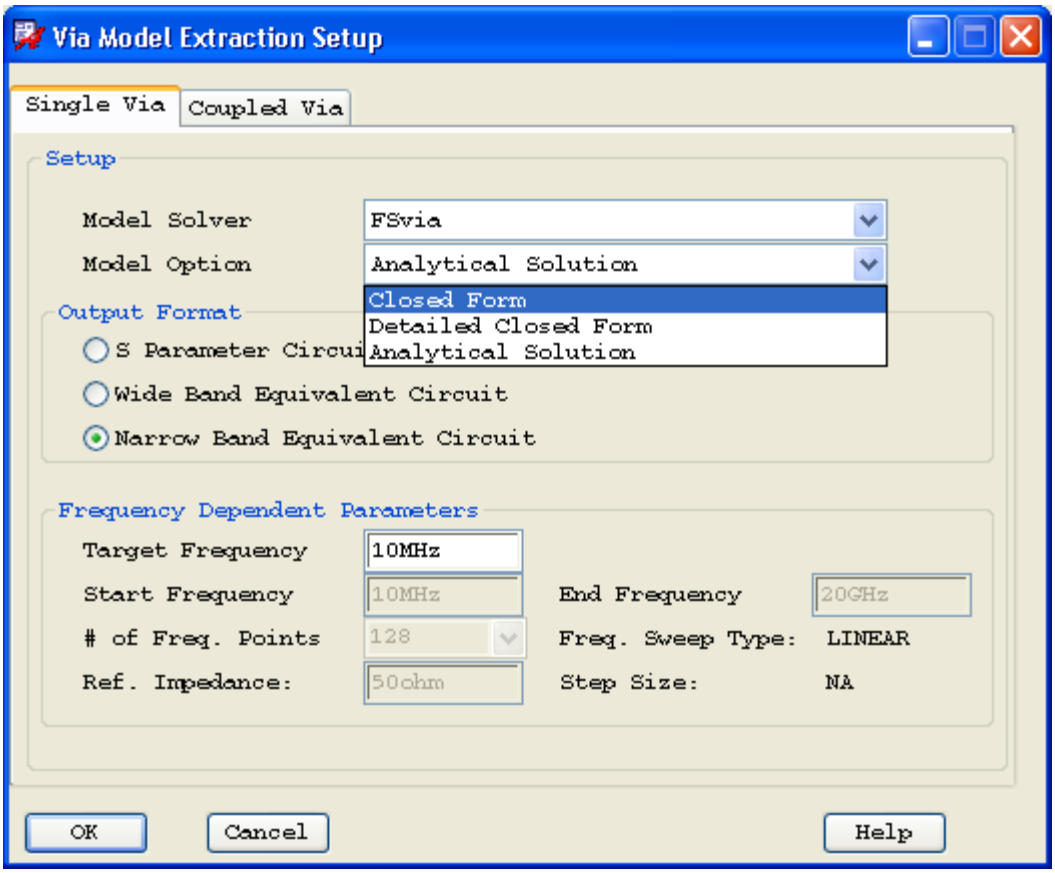
22. In the *SSN* tab, click *Preferences* to open the Analysis Preferences form.

23. In the *InterconnectModels* tab, check the *3-D Modeling - Sentinel-NPE* option.

24. Click *Via Modeling Setup* to open the Via Model Extraction Setup form.

25. In the *Single Via* tab of the form, select *Closed Form* from the drop-down menu of *Model Generation Options*, as shown in Figure 1-9.

Figure 1-9



26. In the *Coupled Via* tab, select *Coupled Disabled* from the Model Option drop-down list.

27. In the *Simulation* tab of the Analysis Preferences form, change *Pulse Clock Frequency* to 66MHz.

28. Click *OK* on the Analysis Preferences and Via Model Extraction Setup forms to save your changes and close the forms.

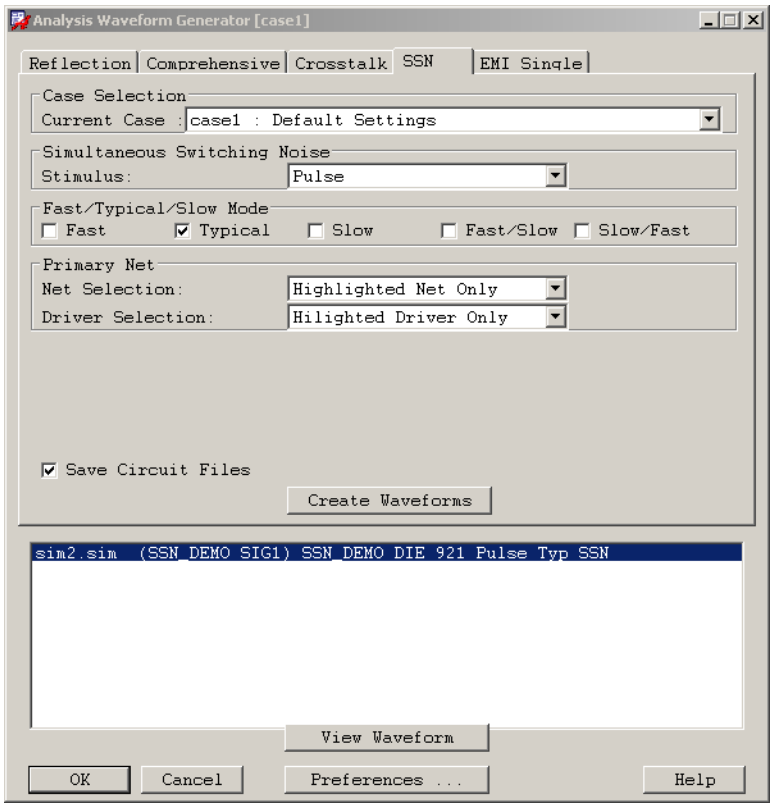
29. In the Analysis Waveform Generator dialog, check *Save Circuit Files*.

30. Click *Create Waveforms* to begin the SSN simulation.

The Field Solution Progress dialog starts as the process is invoked automatically for signal bus modeling.

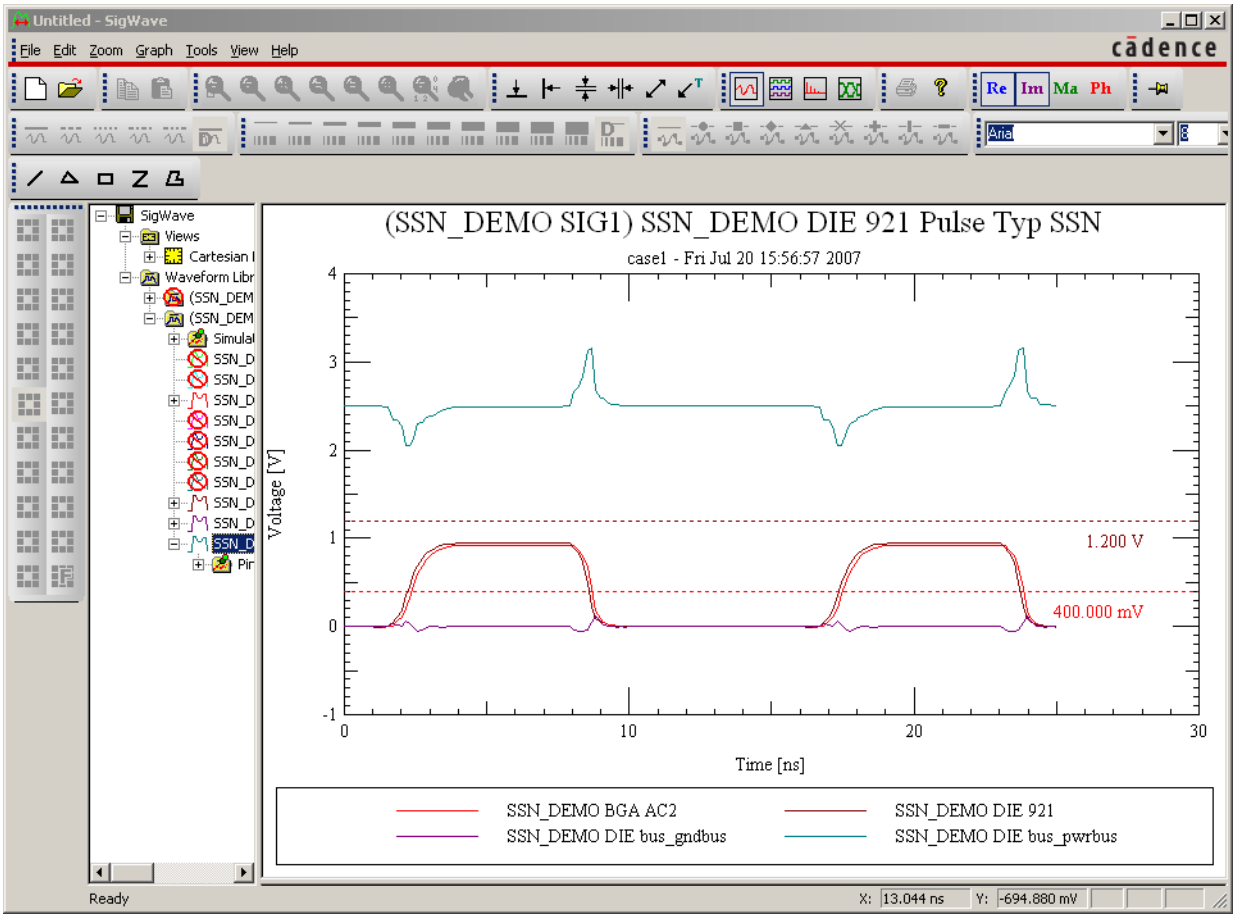
When the simulation is complete waveforms will be generated as `sim1.sim`, as shown in Figure 1-10.

Figure 1-10



31. Click *View Waveform* to view the results of the simulation in SigWave, as shown in Figure 1-11.

Figure 1-11



32. You can now measure the power/ground bounce values in the waveform display using the functionality in SigWave.

Note: For details on how to set up power, ground, and signal buses using Allegro Package SI, refer to the tutorial, *Performing SSN Analysis in Early Design Stage Within Allegro Package SI Environment*, at `http://allegro/products/digitalsip/digitalsip_ds.html`.

Using 3D Extraction and Multi-Port Group Capabilities in Allegro Package SI

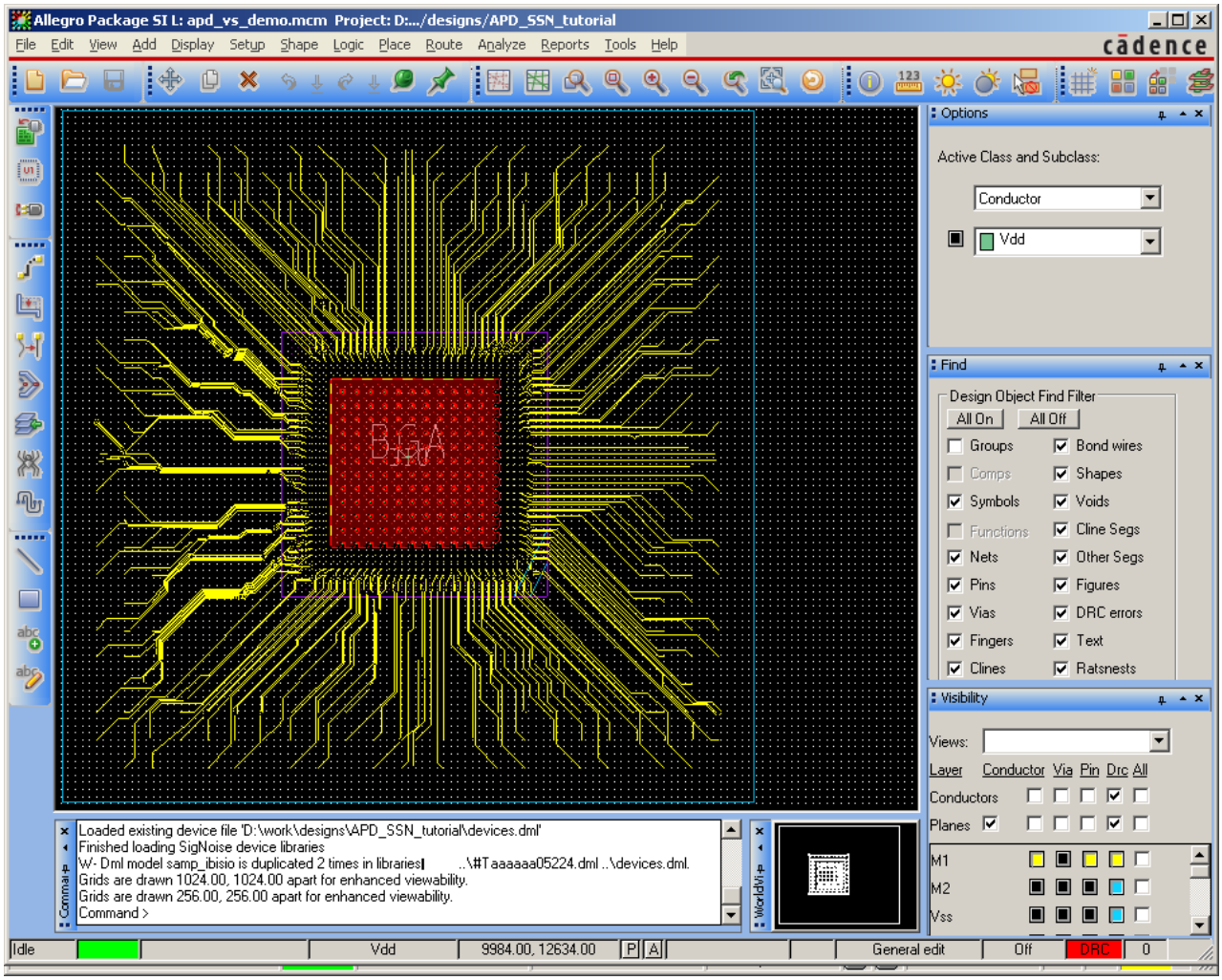
This tutorial describes an APD – VoltageStorm flow for extracting 3D models using the modeling functionality in Allegro Package SI. VoltageStorm is a Cadence IC tool that analyzes on-chip IR-drop.

1. Create a directory on your hard drive; for example: `APD_VS_tutorial`.
2. Access the sample database, `apd_vs_demo.mcm`, at the following location in your installation hierarchy

   `<install_dir>\doc\HS_Pkg_flows\examples`
3. Copy the database into the directory you created.
4. Run *apd*.
5. Choose *Allegro Package SI L* and click *OK*.
6. Open `apd_vs_demo.mcm`.
7. Click *Yes* when prompted to upgrade the design to the latest version of the software.

   The database opens as shown in Figure 1-1.

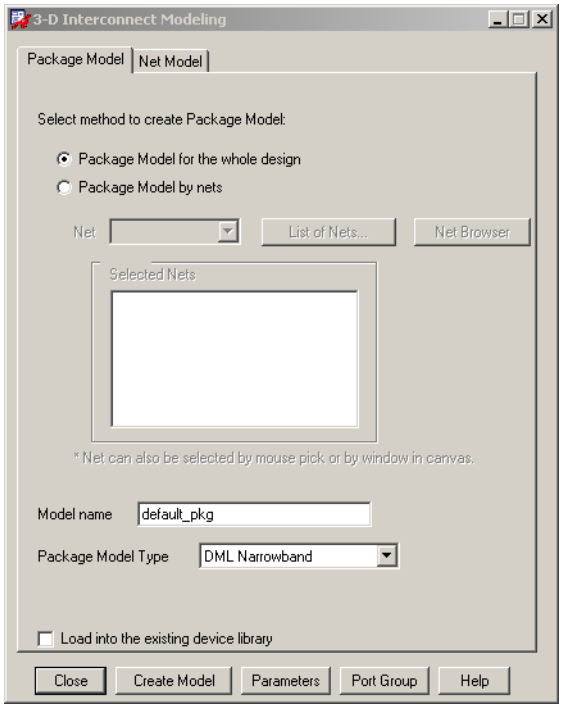
Figure 1-1



8. From the APD menu bar, choose *Analyze – 3-D Modeling*.

The 3-D Interconnect Modeling form opens, as shown in Figure 1-2.

Figure 1-2



9. In the Net Model tab, click *Net Browser*.

The Signal Select Browser opens, as shown in Figure 1-3.

Figure 1-3

10. Select net VDD in the *Available Nets* window and click *OK*.

11. In the 3-D Interconnect Modeling form, click *Parameters*.

The 3-D Modeling Parameters form opens.

12. Fill in the following parameters in the *General* tab of the form:

- ❑ Solder Ball Location: Auto-detect
- ❑ Design unit: 500MHz
- ❑ Number of coupling nets:1
- ❑ Minimum via diameter: 50um
- ❑ Ignore void diameter:0um
- ❑ RL mesh density: Fine
- ❑ CG mesh density: Fine
- ❑ CG planar boundary box: Medium
- ❑ CG z-directional boundary box: Medium

- ❑ Enable multiport: YES
- ❑ Controlled sources in model: NO
- ❑ Number of subcircuit segments: 5
- ❑ Start frequency: 0MHz
- ❑ Number of frequency ports: 256
- ❑ Frequency sweep scale: Linear
- ❑ Reference impedance: 50ohm

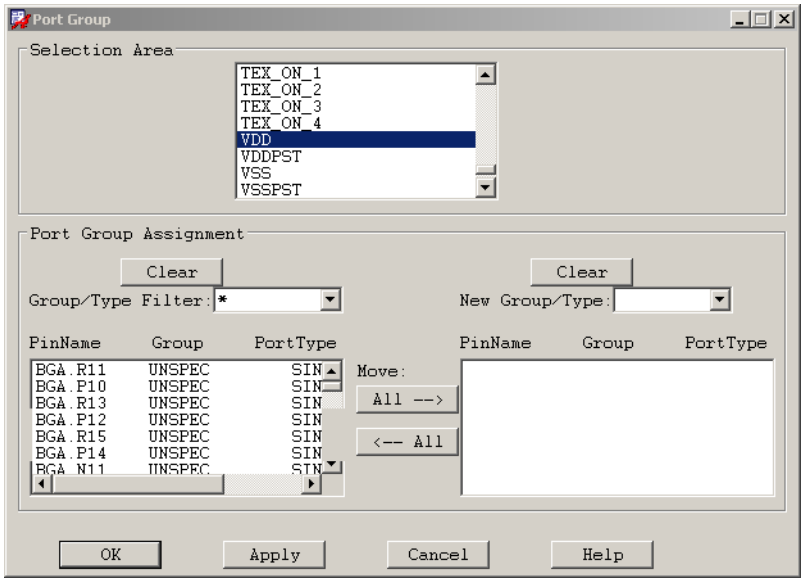
13. Click *OK* to close the Parameters form.

14. In the 3-D Interconnect Modeling form, click *Port Group*.

15. In the selection area of the Port Group form, select net `VDD`.

All the pin names in the selected net are displayed, as shown in Figure 1-4.

Figure 1-4



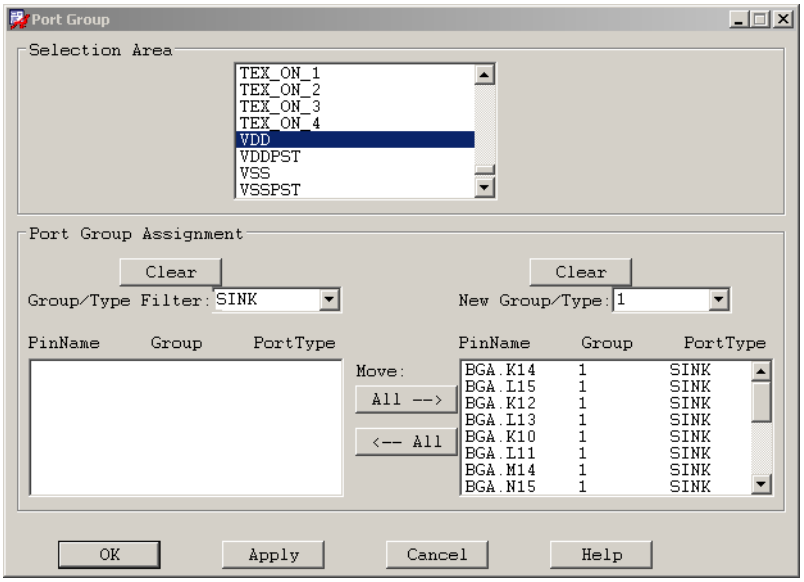
16. In the *Group/Type Filter*, select `Sink`.

The list is filtered to display only the Sink-type pins. (These are all BGA pins.)

17. Click *All->* to move all the BGA pins to the window on the right side of the form.

18. Select **1** in the *New Group/Type* filter to assign all BGA pins as one group. This configuration is shown in Figure 1-5.

Figure 1-5



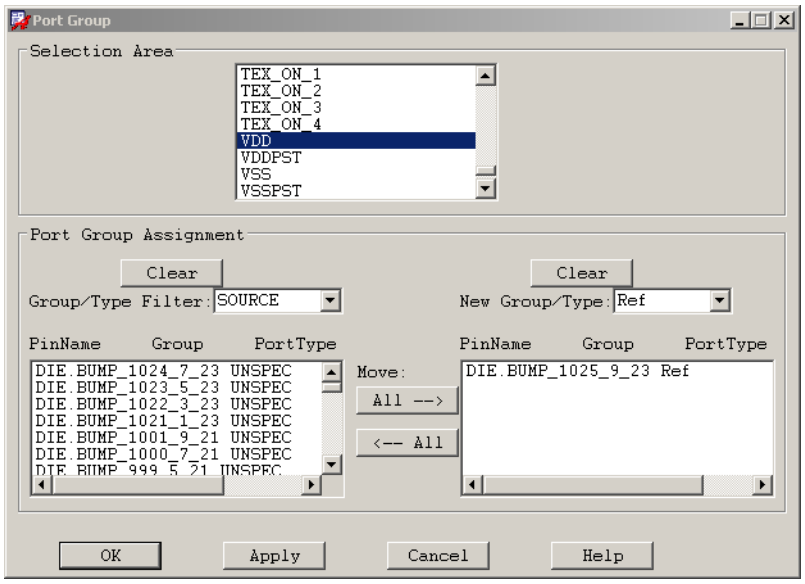
19. Click *<--All* to move this group back into the left window.

20. Select `Source` in the *Group/Type Filter*.

The list is filtered to display only the Source-type pins. (These are all DIE.BUMP pins.)

21. Select the bump pin in the list, `DIE.BUMP_1025_9_23`, and assign it as group **Ref**, as shown in Figure 1-6.

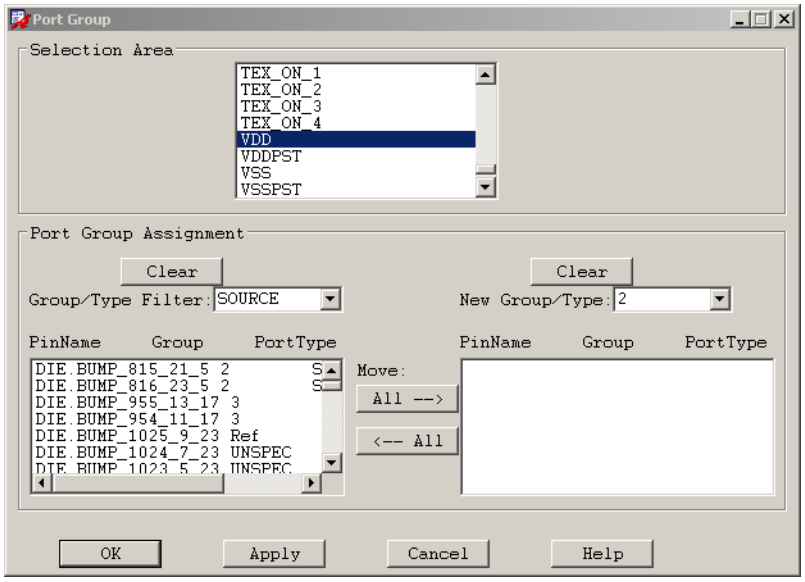
Figure 1-6



22. Move `DIE.BUMP_1025_9_23` back into the left side window.

23. Repeat the previous step to assign pins `DIE.BUMP_954_11_17` and `DIE.BUMP_955_13_17` to group `3` and pins `DIE.BUMP_815_21_5` and `DIE.BIUMP_816_23_5` to group `2`. Leave the rest of the pins unspecified (`UNSPEC`), as shown in Figure 1-7.

Figure 1-7



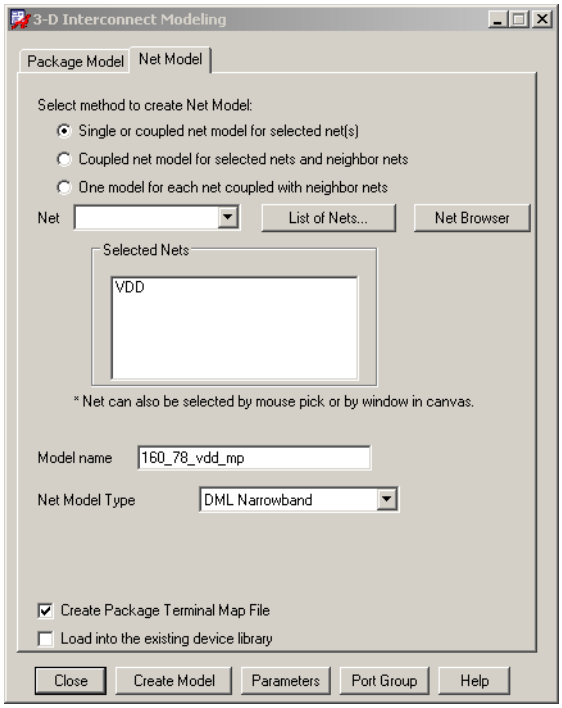
24. Click *OK* to close the Port Group form.

25. In the 3-d Interconnect Modeling form, set *Model name* to `vdd_mp`.

26. Select `DML narrowband` in *Net Model Type*.

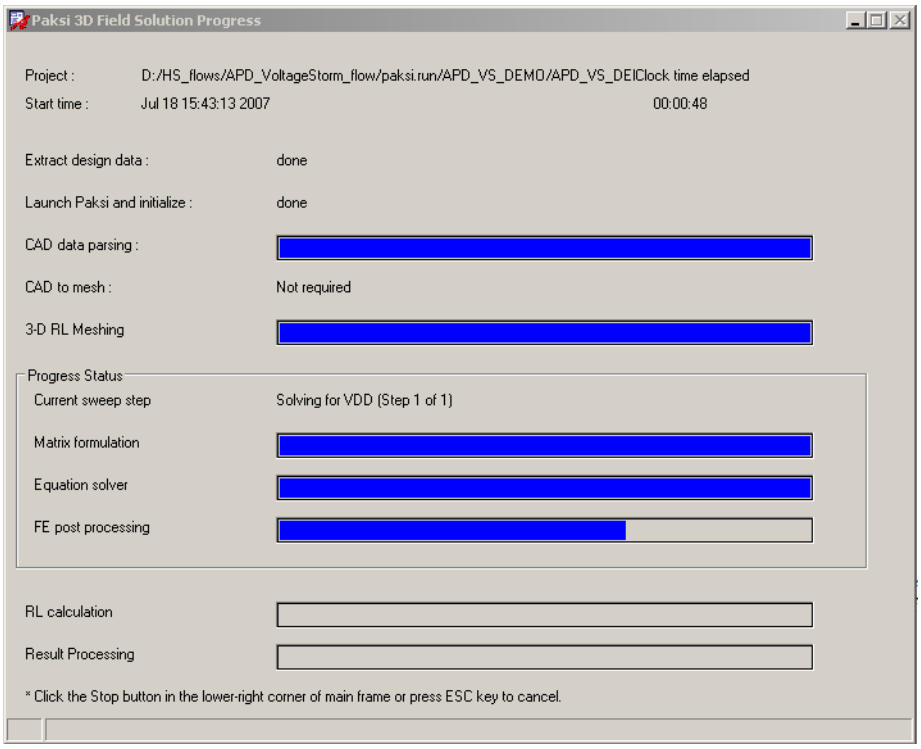
27. Check *Create Package Terminal Map File*. This configuration is shown in Figure 1-8.

Figure 1-8



28. Click *Create Model* to start 3D model extraction. The process window shown in Figure 1-9.

Figure 1-9



When the extraction finishes, two messages appear indicating that the 3D model of VDD net and its corresponding terminal mapping file are successfully created. These message windows are shown in Figure 1-10.

Figure 1-10

29. View the model files `vdd_mp.csv` and `vdd_mp.dml` and the terminal mapping file `s_400.ptmf` in the directory you created at the beginning of the tutorial. Check the spice subcircuit file, `s400.ckt` in the subdirectory `..\paksi.run\APD_VS_DEMO\subckt\`. VoltageStorm reads in `.ckt` and `.ptmf` files to build simulation netlists for the purpose of including package effects in its IR-Drop analysis.

Note: For more details on how to create co-design die using Allegro Package Designer in APD/VoltageStorm flow, please refer to the tutorial at `http://allegro/products/digitalsip/digitalsip_ds.html`.