cadence®

Allegro Sigrity SI Flow Guide

Product Version 23.1
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Allegro Sigrity SI

This chapter covers the following topics:

- Introduction
- Licensing and Packaging
- Launching Allegro Sigrity

Introduction

Allegro Sigrity SI (or Allegro Sigrity as used later in this chapter) is a product (PA5700) for the SI analysis of Allegro PCB, IC Package, and SiP designs. This product integrates Allegro with Sigrity's signal- and power- integrity and package analysis product offerings, which facilitate Power-Aware SI Analysis, Power Integrity, System-Level Serial Link Analysis, and Package Assessment and Model Extraction.

Allegro Sigrity features a layout editor for floorplanning, editing, routing, first order TD SI analysis, and SI related ERCs. Other core components include Constraint Manager and SigXplorer.

Licensing and Packaging

The Allegro Sigrity SI product is available for the three database types: PCB, IC Package, and SiP. The common product options for all the databases are *Power Aware SI* and *Serial Link SI*. The *Package Analyze* option is only available for Package databases: IC Package and SiP.

Important

In case, your SPB Installation and Allegro Sigrity SI installation are in different directories, ensure that the `sigrity_eda_dir` environment in the `<CDSROOT>/share/pcb/text/env` file points to the directory where Allegro Sigrity SI is installed.

Allegro Sigrity Product Options

There are five product options available with Allegro Sigrity SI, which combine Cadence Sigrity tools and include CAD translators to support PCB and Package designs from all of the major vendors.

The available product options are:

- **Power-Aware SI**
- **Serial Link SI**
- **Design Planning**
- **Full GRE**
- **Package Analyze**

The packages Include layout-based TD and FD simulation with or without ideal power, system-level simulation of parallel buses, and supporting tools for model conversion, extraction, and correction, all of the modeling and simulation capabilities needed for system-level channel analysis, 3D solvers, packages electrical assessment, and DC power analysis.

Cadence Sigrity tools

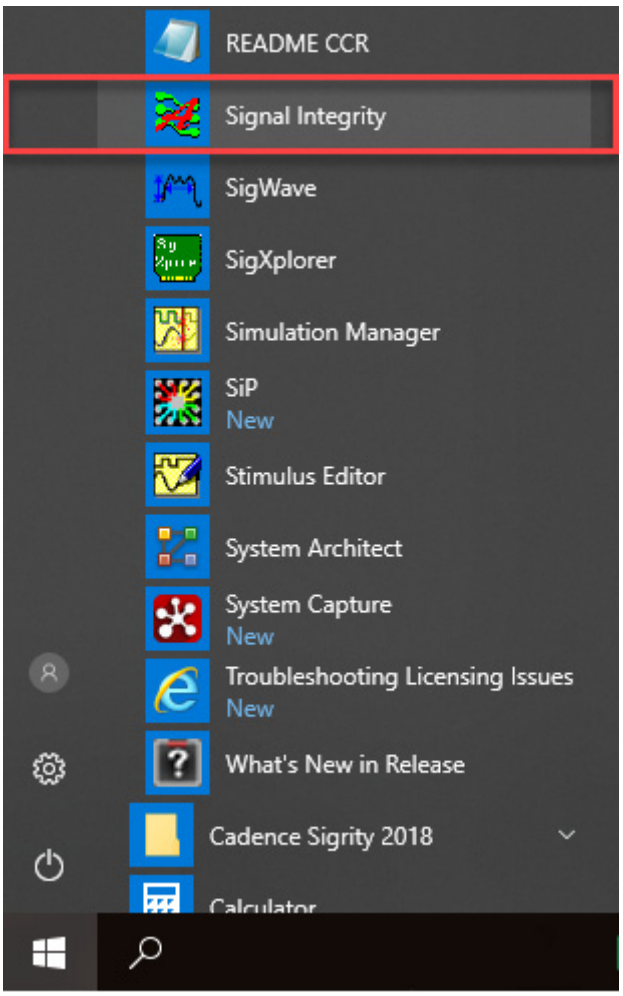
The Cadence Sigrity tools included in the Allegro Sigrity SI license are:

- SPEED2000
- PowerSI
- 3D-EM
- PowerDC
- OptimizePI
- SystemSI – PBA
- SystemSI – SLA
- Broadband SPICE
- T2B
- XtractIM — Only with Allegro Sigrity SI (ICP) and Allegro Sigrity SI (SIP)
- 3D-EM
- PowerDC

Launching Allegro Sigrity

To launch Allegro Sigrity using the Allegro Sigrity SI (PA5700) license:

➡ Choose *Cadence Release 17.2-2016 — Signal Integrity* from the *Start* menu.



OR

➡ Type `allegrosigritysi.exe` in the command prompt and press Enter.

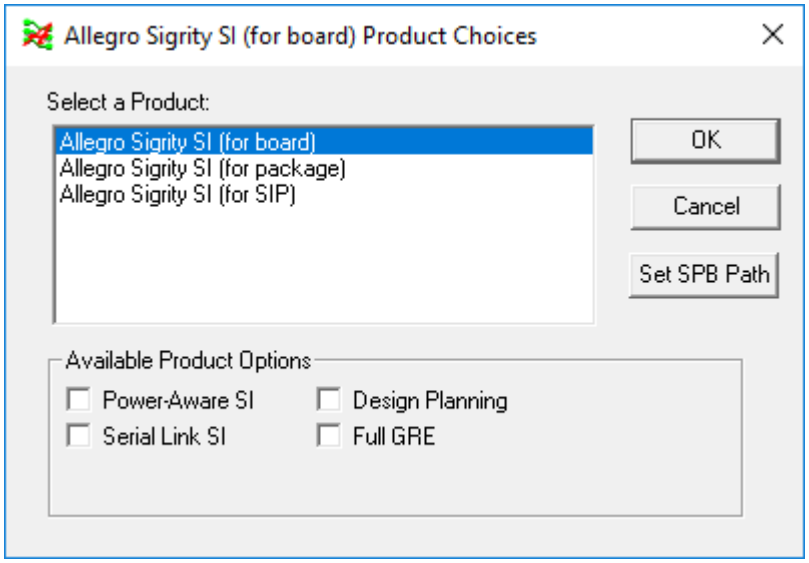
This executable is located in the `<SPB_install_directory>` – `tools` – `bin` folder.

OR

1. Start any of the four layout editors, PCB, PCB SI, APD (ICP), or CDNSIP (SIP).

2. Choose *File – Change Editor* and select the *Allegro Sigrity SI* license.

The Allegro Sigrity SI Product Choices box offers the following product options:



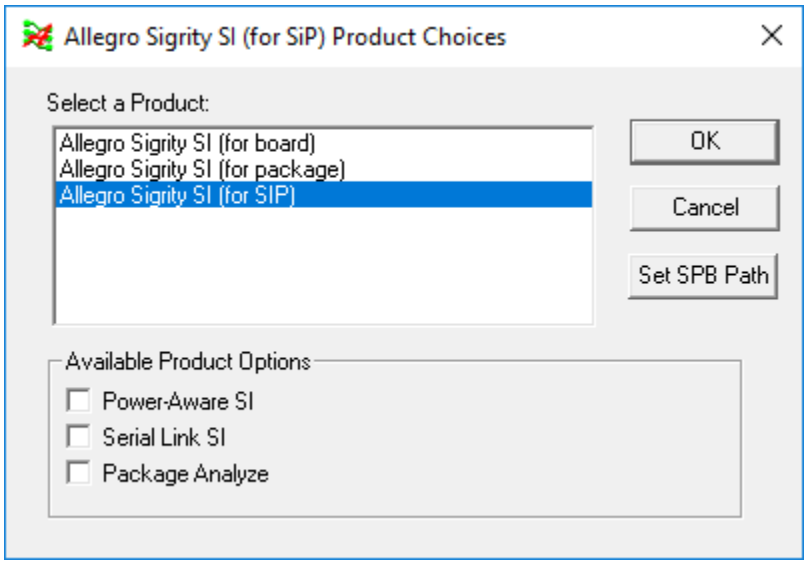
If you select *Allegro Sigrity SI (for board),* the following product options are available:

- *Power-Aware SI*
- *Serial Link SI*
- *Design Planning*
- *Full GRE*

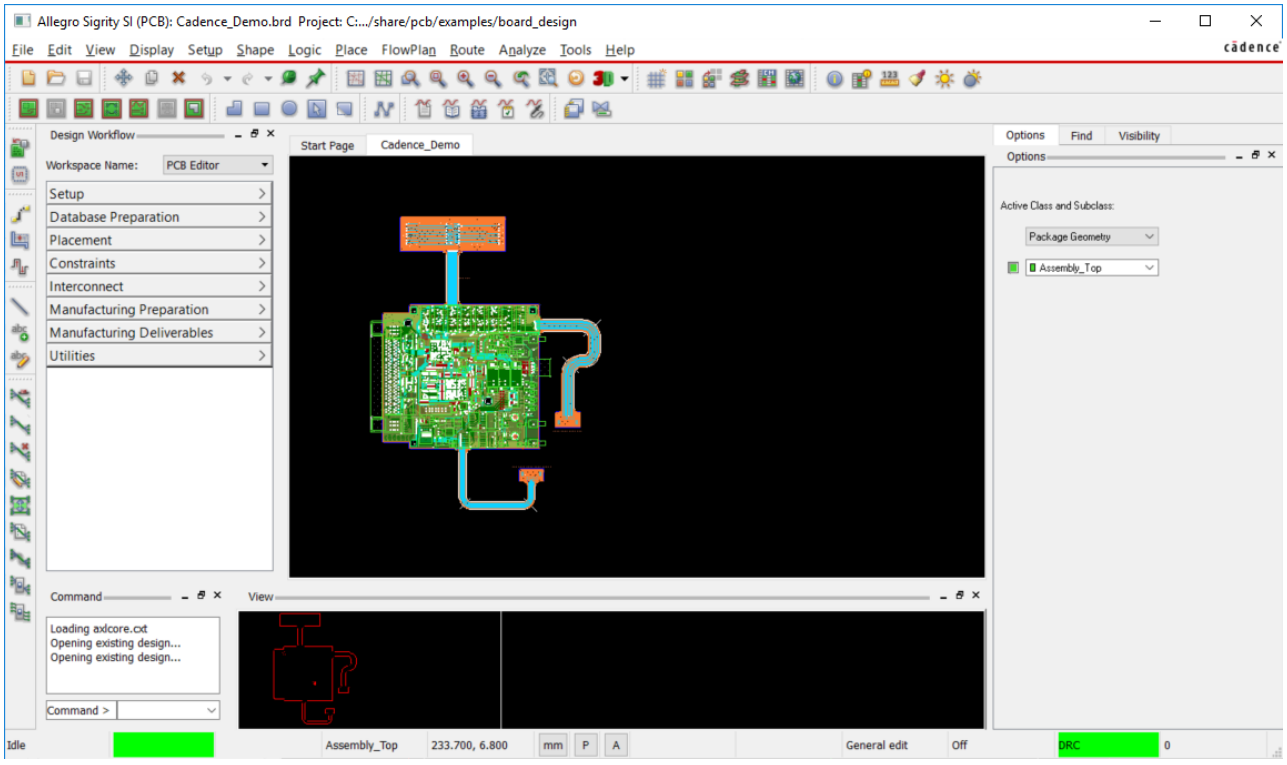
If you select *Allegro Sigrity SI (for package)* or *Allegro Sigrity SI (for SiP)*, the following product options are available:

- *Power-Aware SI*
- *Serial Link SI*

- *Package Analyze*



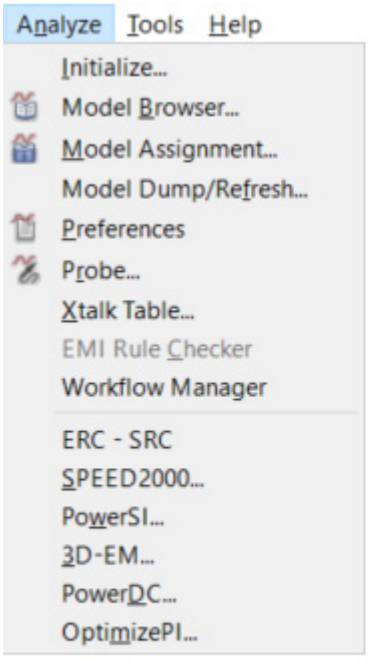
Depending on whether you want to use the product with board layout, package layout, or SiP layout, you can make a choice from the list along with the available product options. When you have made the selection, Allegro Sigrity SI is launched.

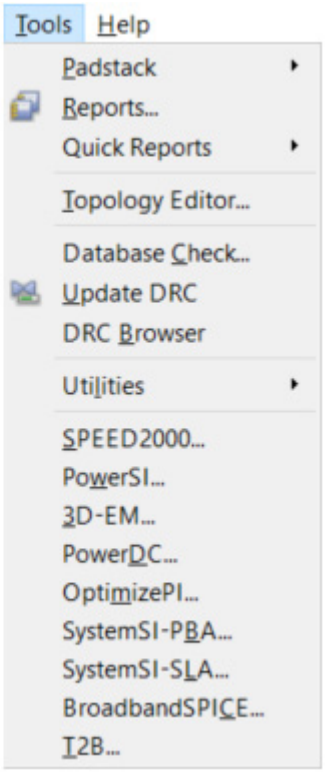


In the Allegro Sigrity environment, you can open your board/package/SiP design and start working with the Cadence Sigrity tools, which are available under the *Tools* and *Analyze* menus.

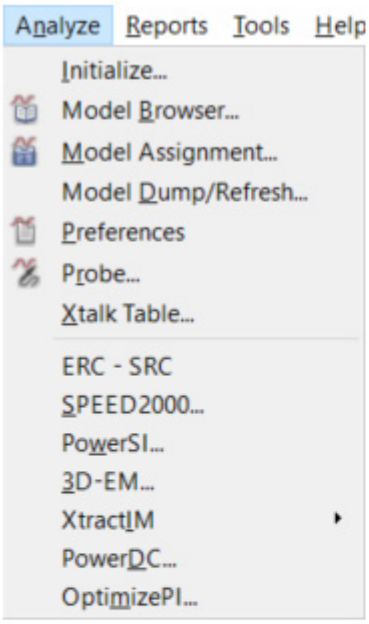
Tools Available with Various Product Options:

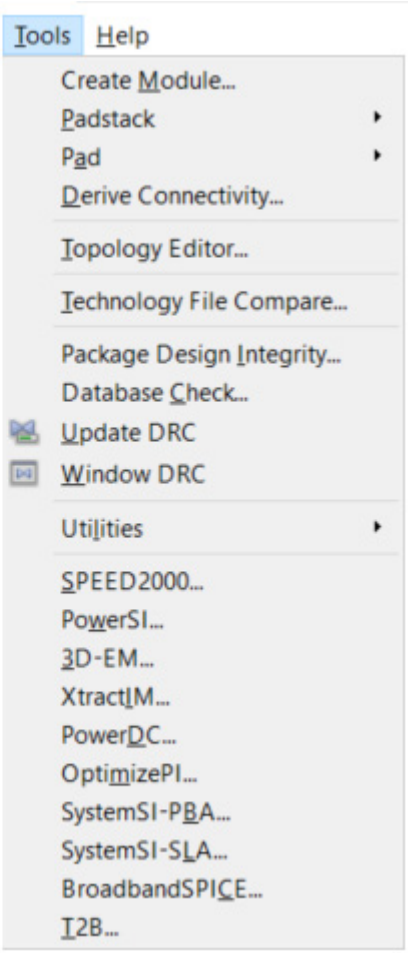
- Allegro Sigrity SI (PCB)



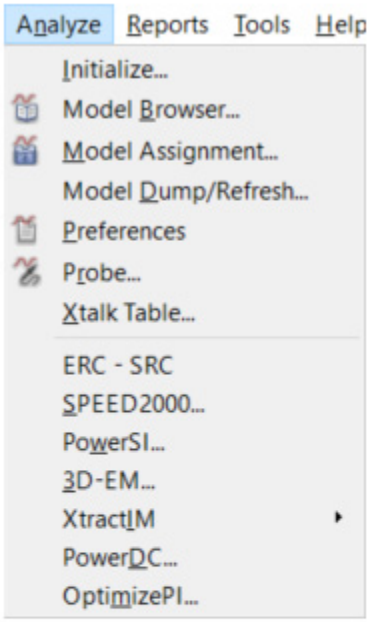


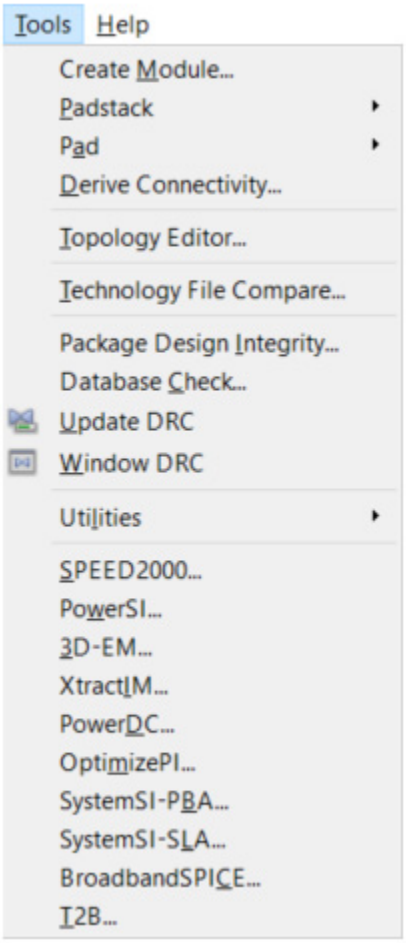
- Allegro Sigrity SI (ICP) - apd





- Allegro Sigrity SI (SIP) - cdnsip





2

Working with Cadence Sigrity Tools

This chapter covers the following topics:

Cadence Sigrity Tools

You can launch the following tools from Allegro Sigrity SI:

- SPEED2000
- PowerSI
- 3D-EM
- PowerDC
- SystemSI-PBA
- System-SLA
- XtractIM
- Broadband SPICE
- T2B

SPEED2000

SPEED2000 is available with Allegro Sigrity SI license with the *Power-Aware SI* option.

PowerSI

PowerSI is available with Allegro Sigrity SI license with the *Power-Aware SI* or *System-level Serial Link Analysis* options.

3D-EM

3D-EM is available with Allegro Sigrity SI license with the *Power-Aware SI* or *System-level Serial Link Analysis* options or Package Assessment and Model Extraction option license.

PowerDC

PowerDC is available with the SI license with the Package Assessment and Model Extraction options.

SystemSI-PBA

SystemSI-PBA is available with the SI license with the Power-Aware SI Analysis option.

System-SLA

SystemSI-SLA is available with the SI license with the System-Level Serial Link Analysis option.

XtractIM

XtractIM is available with the SI license with Package Assessment and Model Extraction options.

Broadband SPICE

Broadband SPICE is available with the SI license with the Power-Aware SI Analysis or System-Level Serial Link Analysis options. Broadband SPICE does not need a `.spd` file to launch.

T2B

T2B is available with the SI license with the Power-Aware SI Analysis or System-Level Serial Link Analysis options. T2B does not need a `.spd` file to launch.

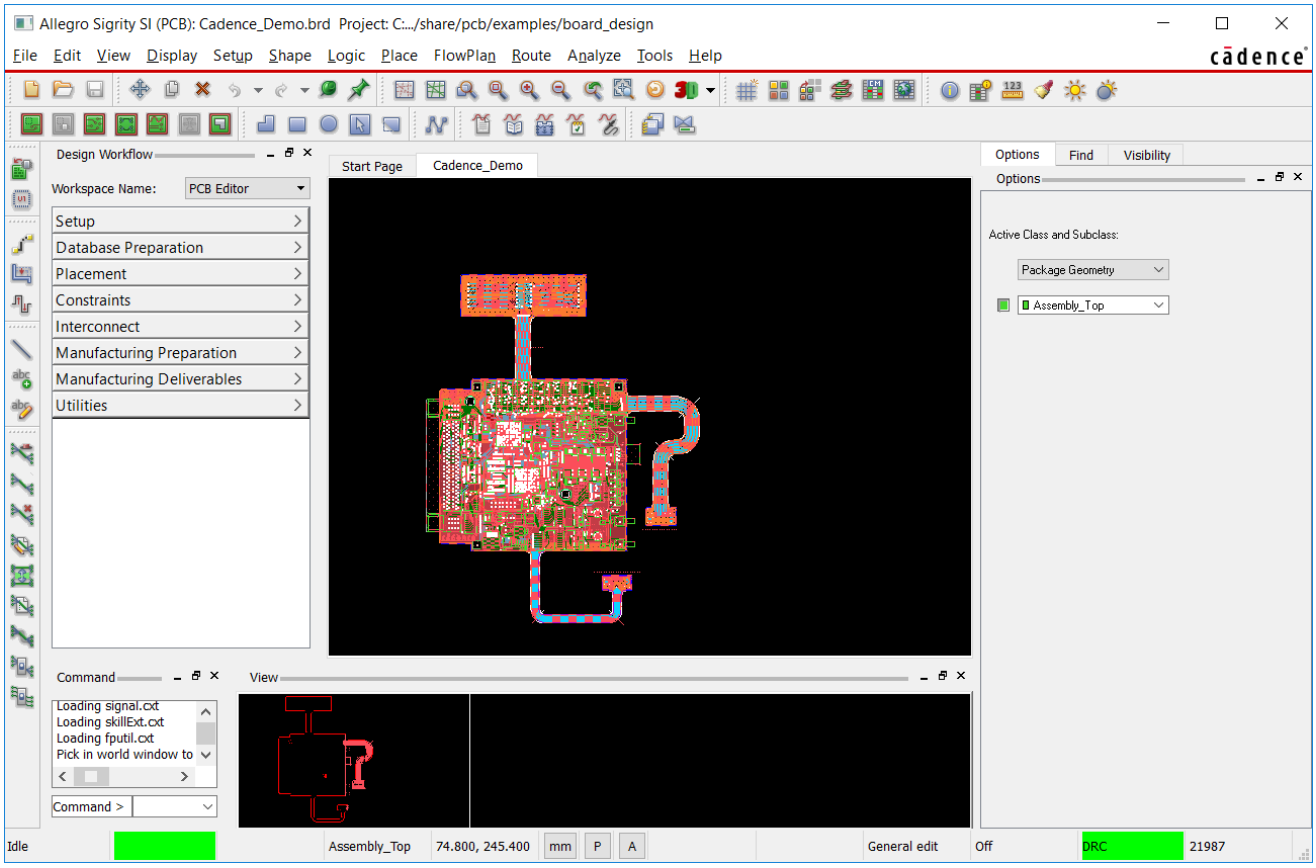
Note: For detailed information on each of the tools, refer to the documentation of the respective tool.

Calling Cadence Sigrity Tools from Allegro Sigrity SI

From within Allegro Sigrity SI, you can directly open Allegro board files (`.brd`), APD files (`.mcm`), and SIP files (`.sip`) in a Cadence Sigrity tool without having to first explicitly translate the files into the Cadence Sigrity tool's format.

Note: The Cadence Sigrity tools work with a translated database (`.spd`) from a variety of file formats.

1. Launch Allegro Sigrity SI and open a board.



2. Launch an Cadence Sigrity tool. For example, PowerSI.

   You can launch the Cadence Sigrity tools from the following two menus:

- *Tools – <tool_name>*: When the tool is launched from the *Tools* menu, it opens a blank workspace. You can create a new design or open an existing design.
- *Analysis – <tool_name>*: When the tool is launched from the *Analysis* menu, first the *XNet Selection dialog box* appears where you select the nets and Xnets to be analyzed. The Allegro layout is then internally translated and opened in the desired Cadence Sigrity tool.

  When you choose to launch any of the Cadence Sigrity tools from the *Analysis* menu, the XNet Selection dialog appears.

Selecting XNets for Analysis

You can select the nets or Xnets from the available nets and launch the appropriate Cadence Sigrity tool to analyze the selected nets.

3. Select the required XNets.

You can also set a few preferences before launching Cadence Sigrity tools from within Allegro Sigrity SI.

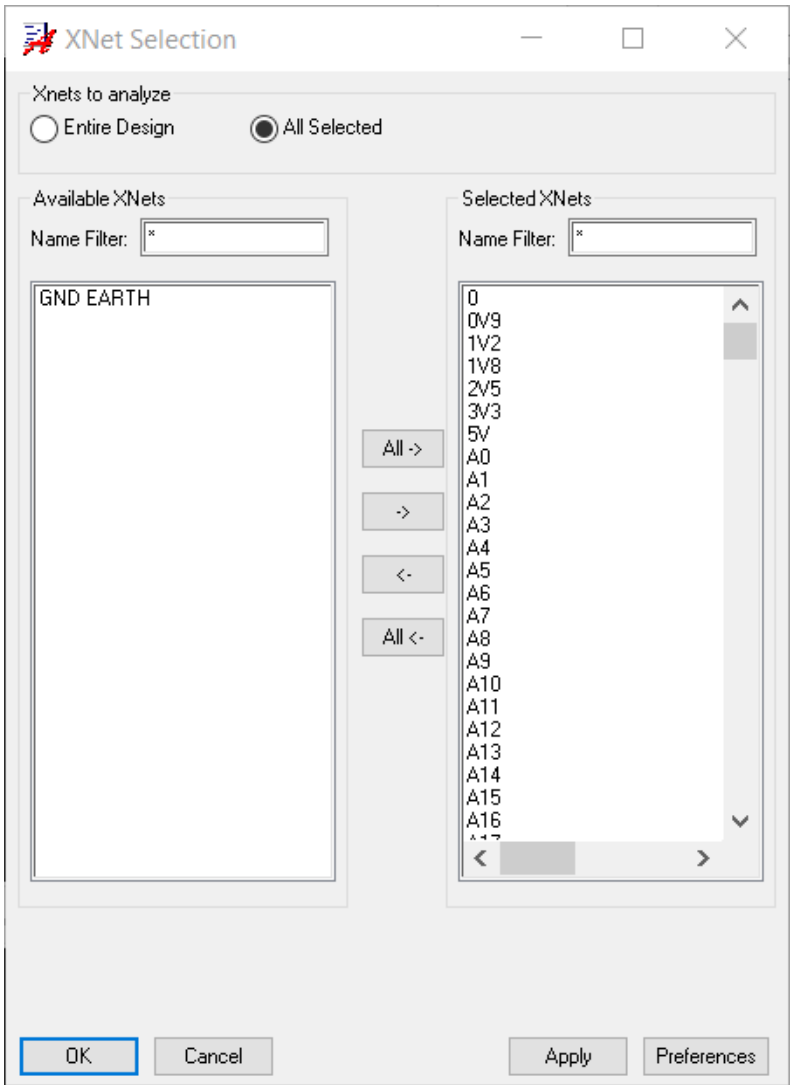


Table 2-1 XNet Selection Dialog

Option	Description
XNets to analyze	Specify whether to analyze the selected XNets or all the XNets in the entire design.
Available XNets	Displays a list of all the XNets in the design.
Selected XNets	Displays a list of selected XNets from the design.

Apply	Saves the XNet selection for later commands and analysis.
Preferences	Launches the Preferences Dialog to change the settings for opening the layout file in the Cadence Sigrity tool.

Setting Preferences to Export Allegro Layout to Cadence Sigrity Tools

You can set these preferences and parameters in the *Preferences* dialog.

4. To launch the Preferences dialog, click the *Preferences* button in the *XNet Selection dialog box*.

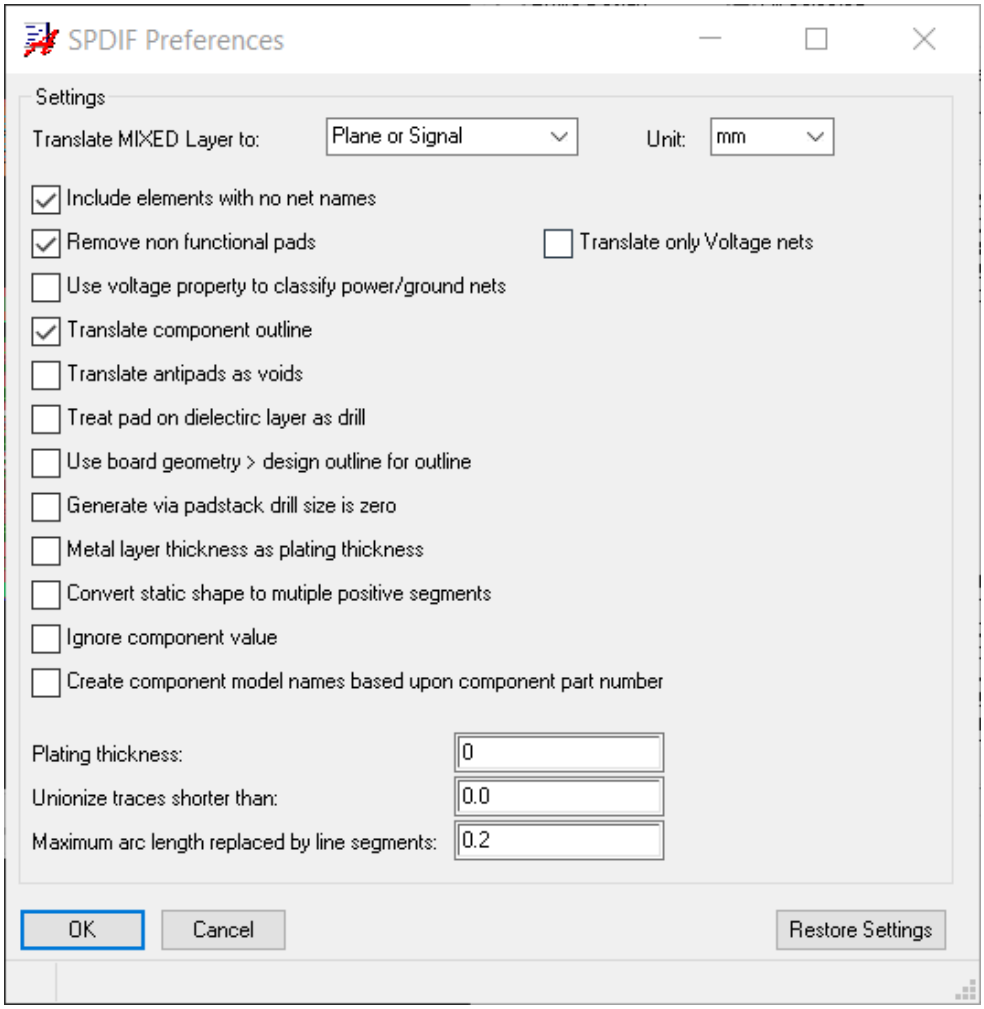


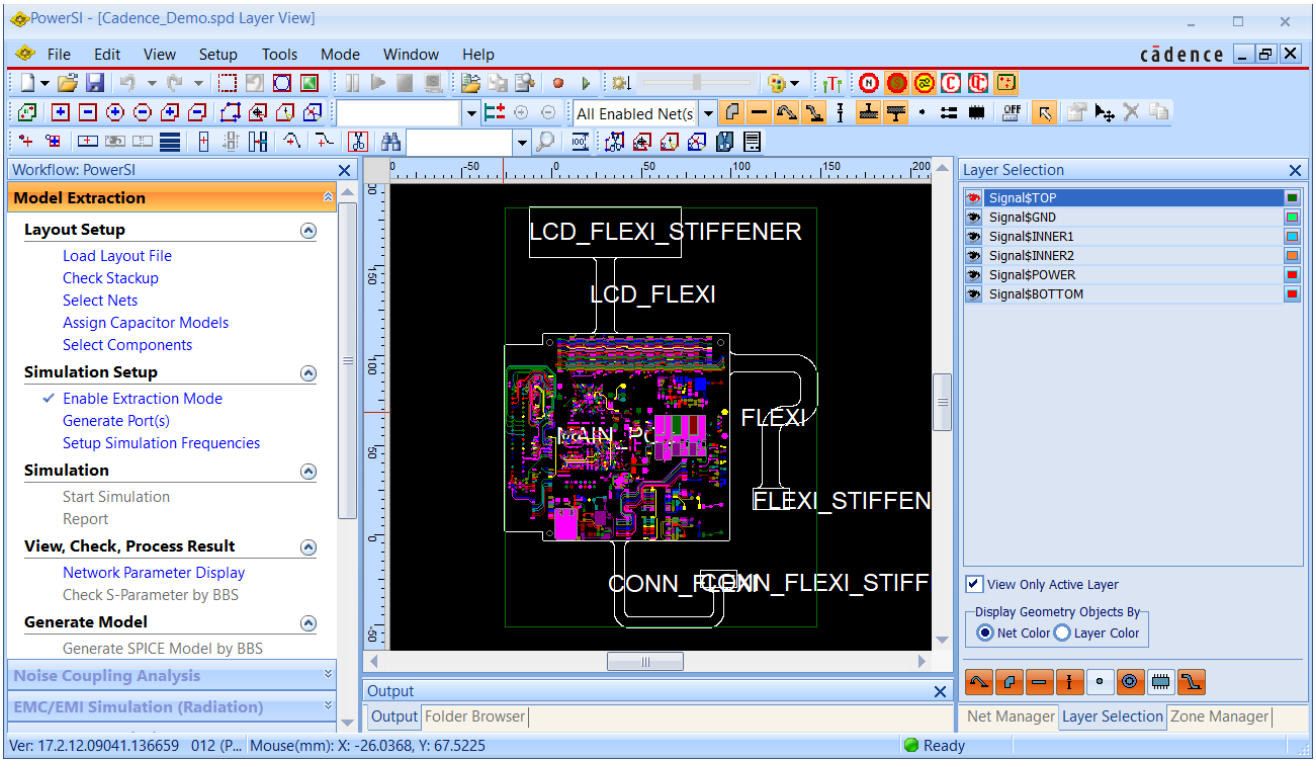
Table 2-2 Preferences Dialog

Option	Description
Translated MIXED Layer to	Determines how to translate mixed layers in the Allegro layout file to the Allegro Sigrity format. *Plane Layer* is selected by default. ■ *Plane Layer*: The MIXED layers are translated to Plane layers. Traces on these layers are ignored. ■ *Plane or Signal*: The translator checks if the MIXED layer contains traces. If traces are found, it translates the layer to a Signal layer. Else, it translates the layer to a Plane layer. ■ *Signal*: The MIXED layers are translated to Signal layers.
Allow patches on Signal layers	Translates patches on signal layers. This option is selected by default.
Distinguish shapes of different nets by color	The translator assigns shape components of nets with colors of the selected nets. If this option is unchecked, the translator assigns shape components with the default color of the shape. This option is selected by default.
Add pseudo plane(s) if lack of plane or patch	The translator adds an extra pair of Planes to the bottom of the structure in the output file, if all metal layers do not have patches. If only one metal layer has patches, an extra metal Plane layer is added to the bottom of the structure in the output file.
Append net name to objects	The translator adds net names to object names. This option is selected by default.
Include elements with no net names	Translates elements without net names. If this option is cleared, the translator will NOT translate elements without net names. This option is selected by default.
Create Partial Ckt Names based on Component Part Number	The translator creates partial Ckt names based upon component part number.
Calculate via plating using 'Drill/Slot symbol' value	The translator uses the "Drill/Slot hole" as the outer diameter and "Drill/Slot symbol" as inner diameter.

Option	Description
Split vias into several 2-layer vias	The translator splits vias into several 2-layer vias to show inner pads (pad on all layers).
Translate antipads as voids	Translates antipads as voids.
Translate only voltage nets	Translates only voltage nets.
Treat pad on dielectric layer as drill	The translator treats a pad on the dielectric layer as drill. This option is selected by default.
Unionize traces shorter than	The translator discards any traces shorter than this value. The default value is 0 mm, implying that by default no traces are discarded.
Maximum arc length replaced by line segments	Translates arcs to line segments of this value or shorter to ensure smooth appearance. The default value is 0.2 mm.
Name affix	The translator adds this string in the field to the names of all the layers, nodes, vias, and traces. This option is useful when you combine two `.spd` files together.

5. Click *OK* to close the Preferences dialog.
6. Click *OK* in the XNet Selection dialog to launch the Cadence Sigrity tool.

The Sigrity tool launches.

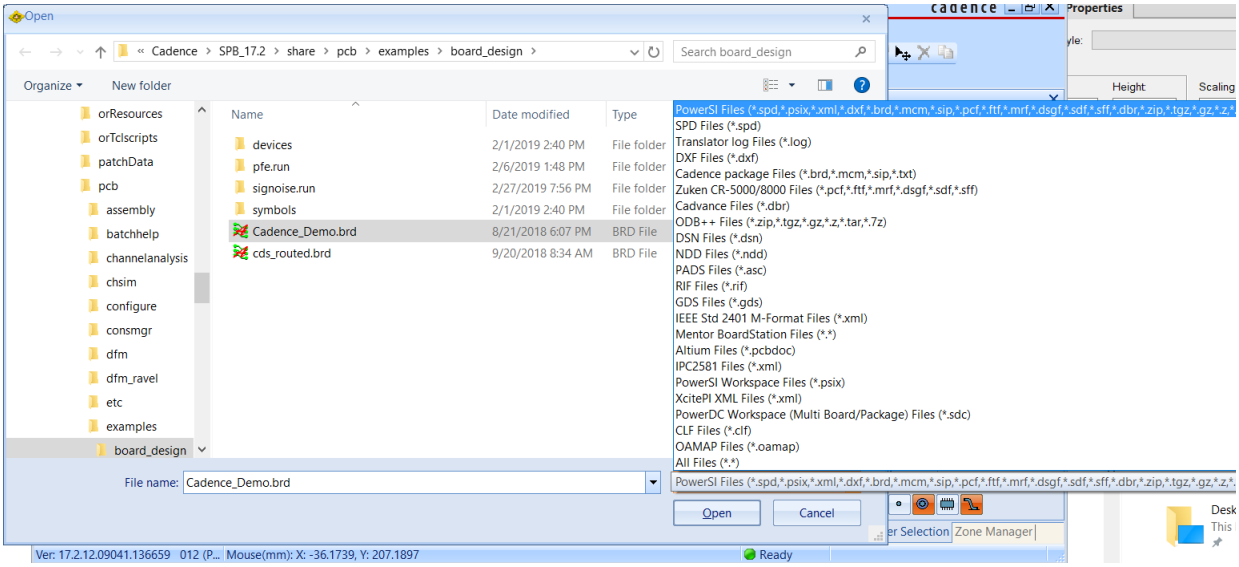


Opening Allegro Layout Files in Cadence Sigrity Tools

You can also open the Allegro layout files (`.brd`, `.mcm`, and `.sip`) directly from the Cadence Sigrity tools.

1. Choose *File – Open*.
2. In the Open dialog, browse to the location which stores the Allegro layout files.
3. Select the file type as `.brd`, `.mcm`, or `.sip`.

   The available layout files of the selected file type will be listed.
4. Click *Open* to open the layout file in the Cadence Sigrity tool.



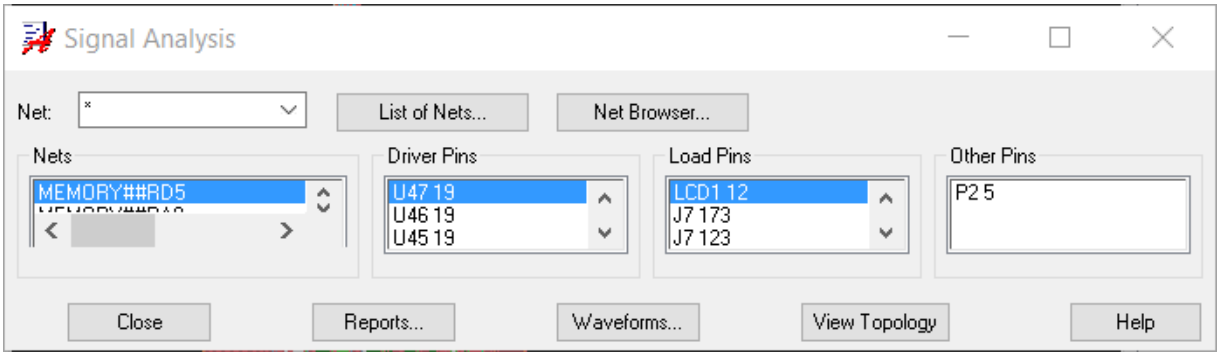
Generating Simulation Reports and Waveforms in SystemSI

From Allegro Sigrity SI, you can create reports and waveforms on selected nets. The reports and waveforms are generated and displayed in SystemSI. Use the Signal Analysis dialog to generate reports and waveforms.

Generating a Report

To generate a report:

1. Choose the *Analyze – Probe* menu.
2. In the Signal Analysis dialog, select the desired net, driver pin, and load pin.

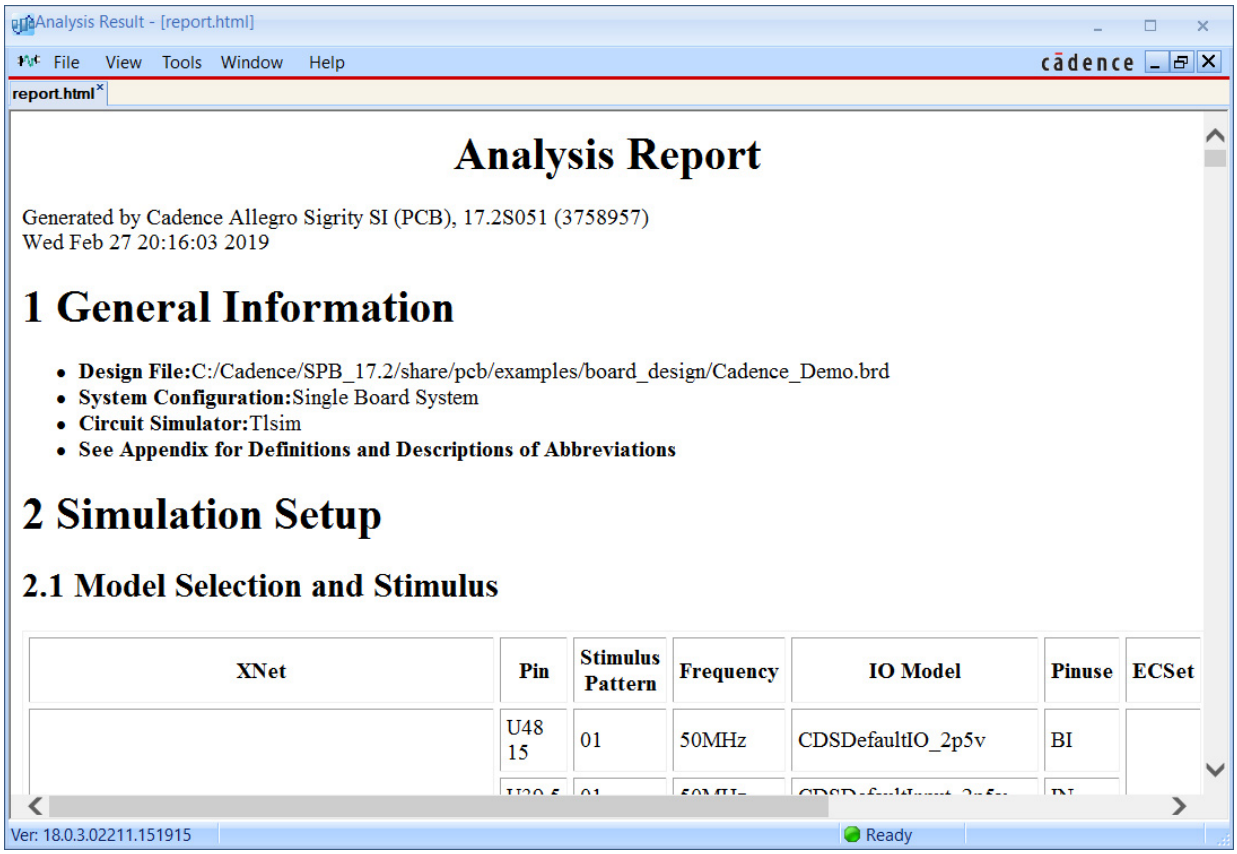


3. Click the *Reports* button.
4. Ignore errors, if any, and continue.

5. In the Analysis Report Generator dialog, specify the report type and simulation preferences based on requirements.

6. Click *Create Report*.

SystemSI is called and the report is generated and displayed in the SystemSI report viewer.



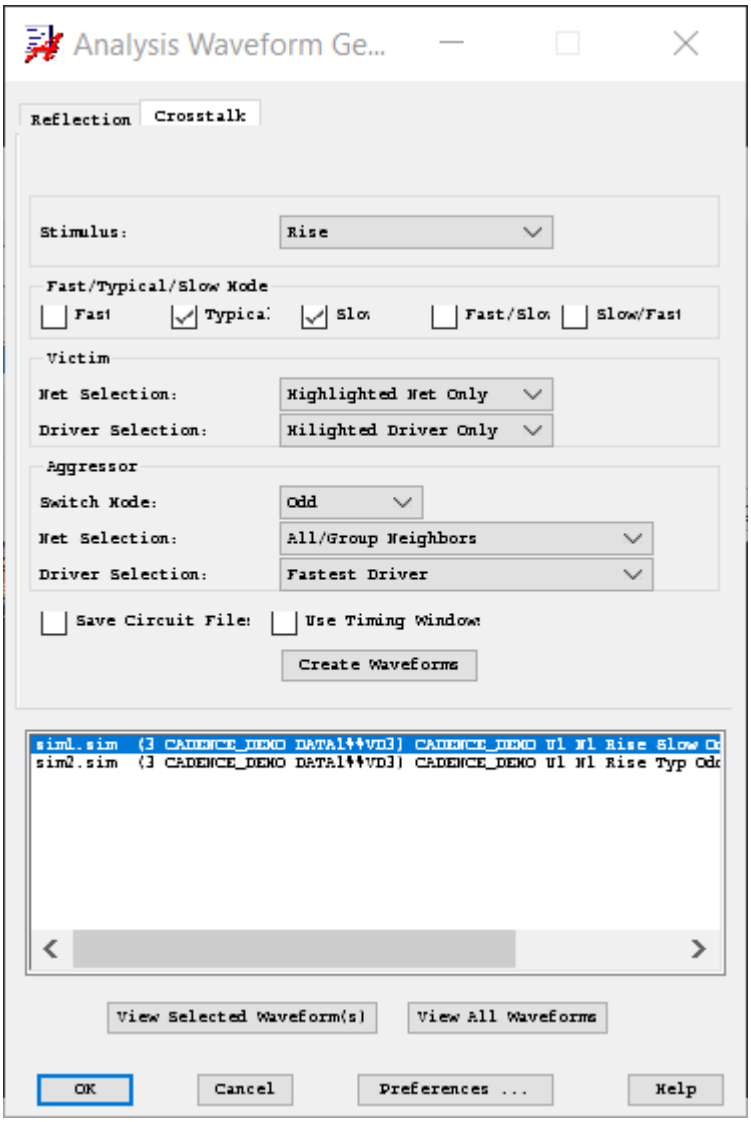
Generating a Waveform

Just as you generated and displayed a report in SystemSI, you can also generate and view a waveform in SystemSI.

To generate a waveform, perform the following steps:

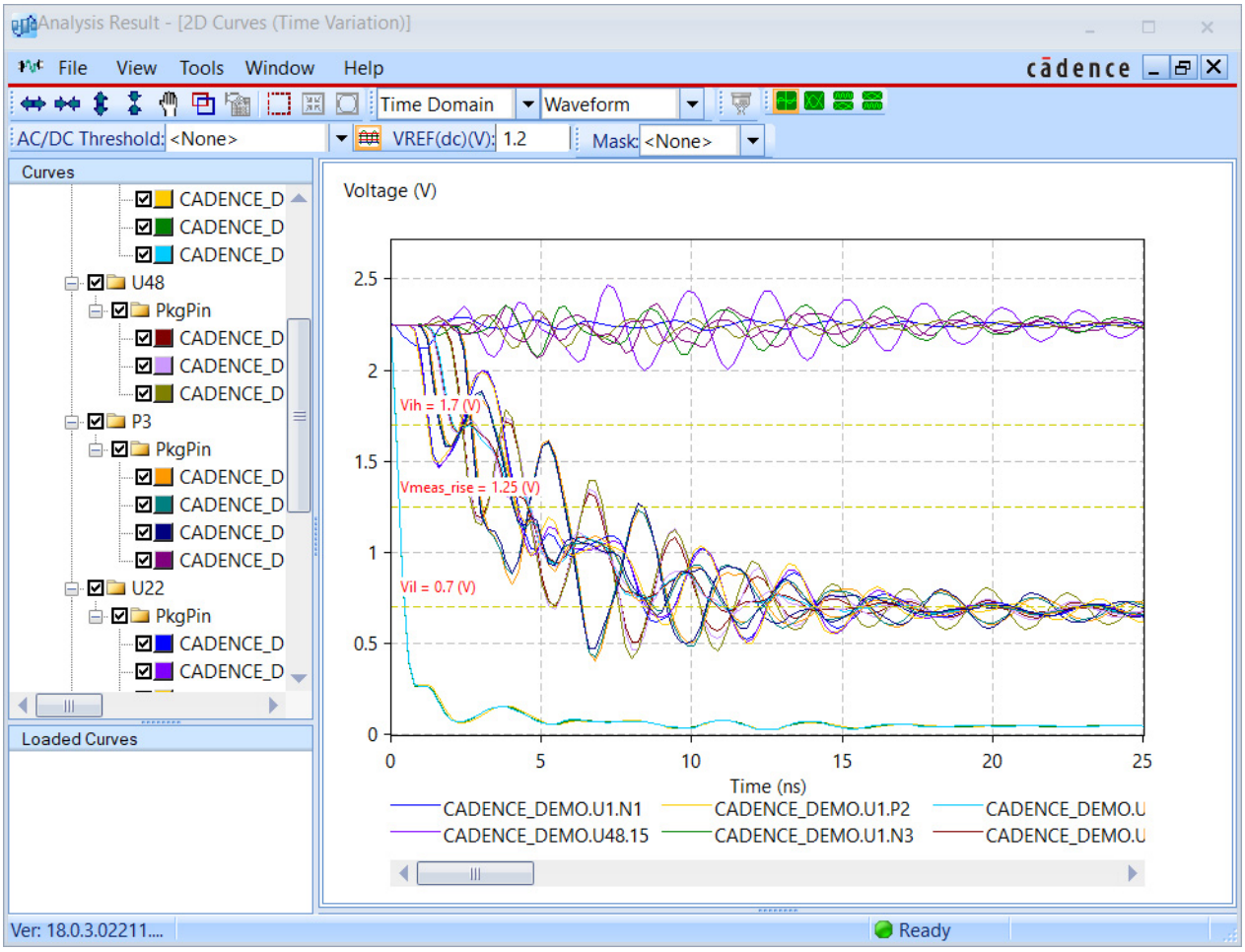
1. Back in the Signal Analysis dialog, click *Waveforms*.
2. In the Analysis Waveform Generator, make the desired choice for either a *Reflection* or a *Crosstalk* report.
3. Click *Create Waveform*.

The simulation starts and when it completes, the names of the generated waveforms appear in the Analysis Waveform Generator dialog.



4. Select a waveform from the list and click *View Selected Waveform(s)*.

The waveform is displayed in the SystemSI's waveform viewer.

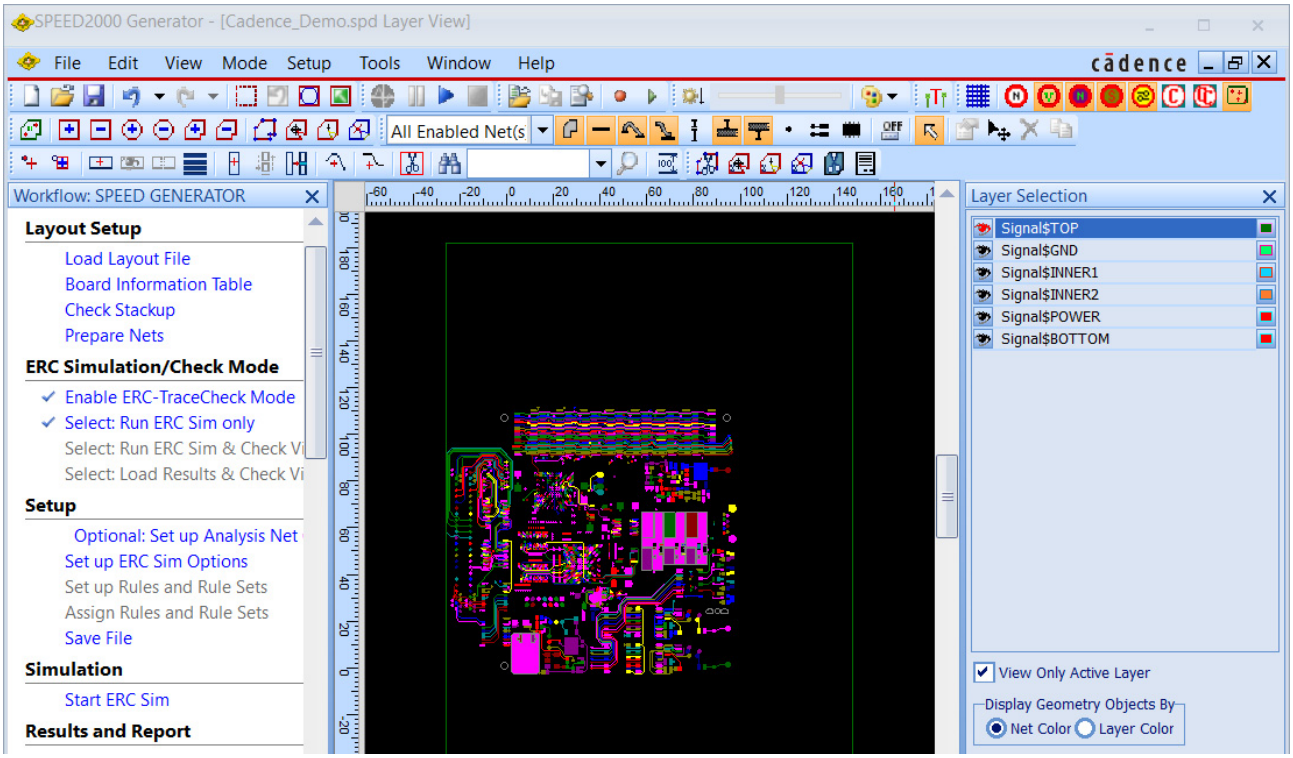


Performing ERC and SRC Simulation

You can launch SPEED2000 from the *Analyze* menu to perform trace impedance/coupling/reference check simulation (ERC) and SI metrics check simulation (SRC).

1. Choose *Analyze – ERC - SRC*. The *XNet Selection dialog box* appears.
2. Select the nets and Xnets to be analyzed and click *OK*.

   SPEED2000 Generator launches with the *ERC - Trace Imp/Cpl/Ref Check* layout check mode enabled.



   You can click *SRC - SI Metrics* in the workflow pane to change the layout check mode and perform SI metrics check.

3

Assigning and Browsing Models in Allegro Sigrity SI

This chapter covers the following:

Overview

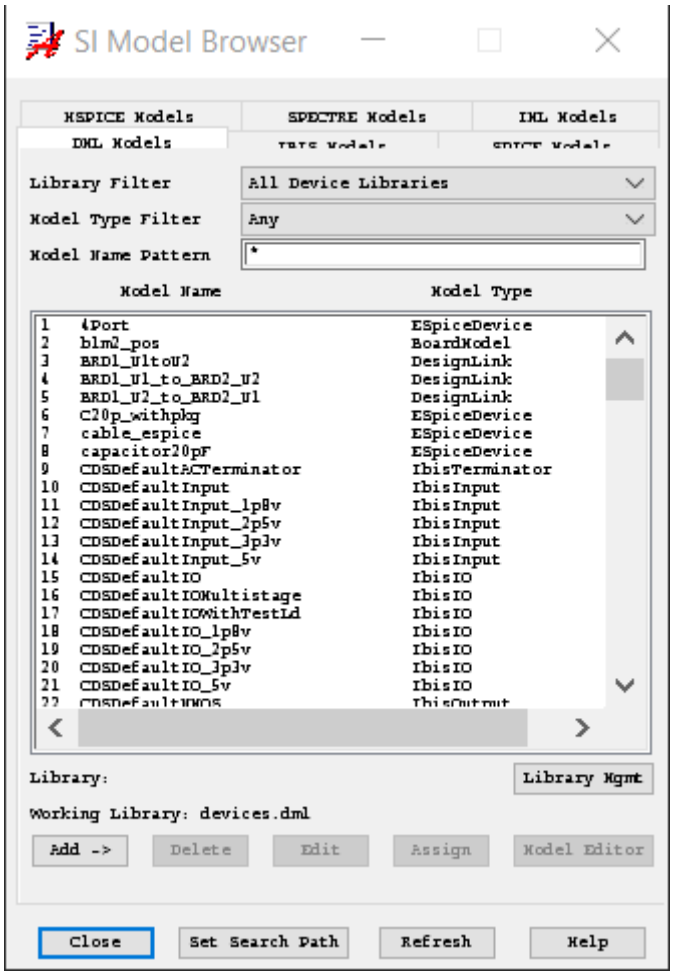
You use the SI Model Browser to manage your libraries of device and interconnect models, and launch Model Editor. You can also use SI Model Browser to specify which IBIS, device, and interconnect libraries you want the tool to access, as well as the order of library access.

Working with Model Browser

The tabbed interface of the SI Model Browser accommodates three model types, IBIS, ESpice, and IML. Each tab contains a field for filtering the listed models, as well as a button to set the library search path of the model and to set its associated file extensions.

➡ To access the SI Model Browser dialog box from Allegro Sigrity SI, choose *Analyze – Model Browser*.

The Model Browser is displayed.

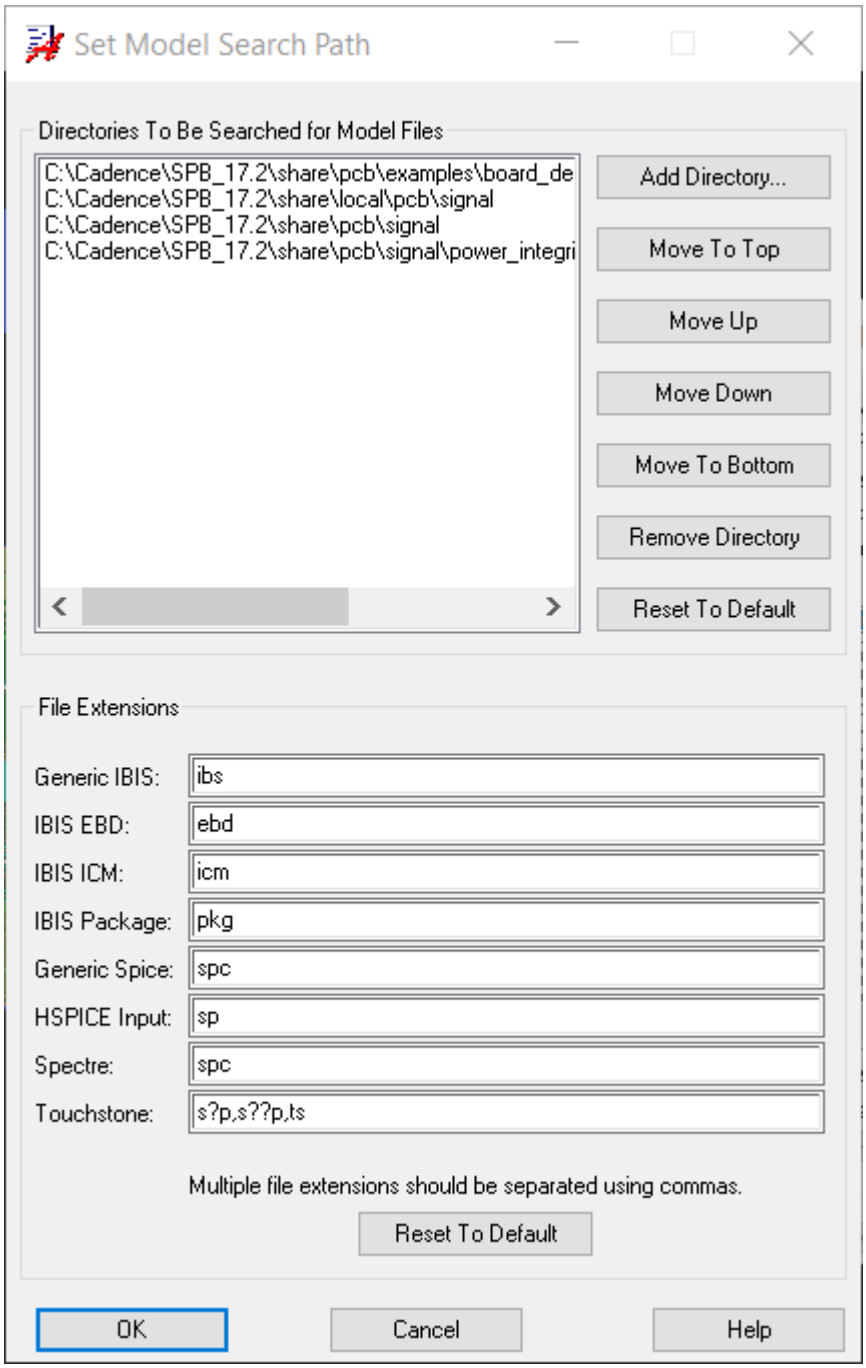


Use the SI Model Browser to specify the IBIS, device, and interconnect libraries used by the simulator during signal analysis. These libraries contain the DML, IBIS, Spice, HSpice, SPECTRE, and interconnect (IML) models used by the simulator to build circuit simulations. Other associated dialog boxes launched from the SI Model Browser enable you to create and edit device and interconnect models contained in these libraries.

Note: You can select multiple model files so that multiple files can be parsed at once.

- *Edit* – Click the *Edit* button to open a text editor for the selected model.
- *Set Search Path* – Click this button to launch the Set Model Search Path dialog. In this dialog, you can specify the directories in which to search for signal models, and their

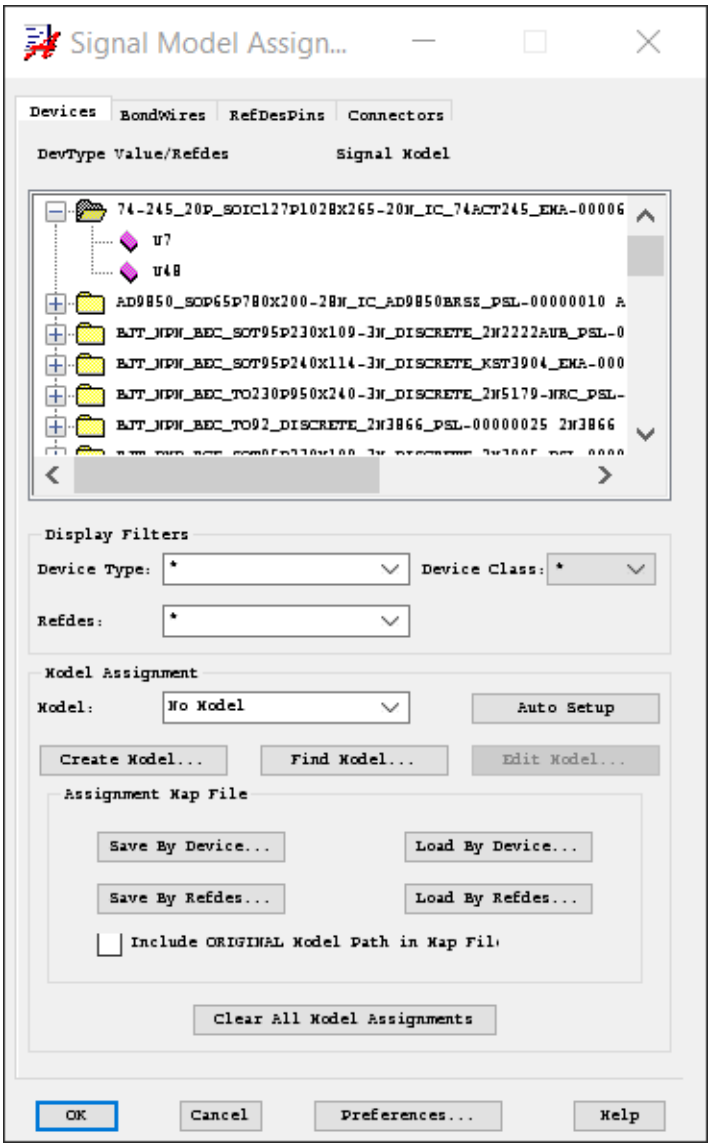
search order. You can manage the search path and file extensions for all model formats here.



Assigning Models

Use the Signal Model Assignment dialog box to assign signal models to design components.

➡ To open the Signal Model Assignment dialog, choose *Analyze – Model Assignment*. Ignore errors, if any.



Devices Tab

Use the Devices tab to assign device models to components; automatically or manually. You can access the Model Browser to find device models, modify existing models before assigning them, and create new models. You can also load and save the Assignment Mapping file for the design

BondWires Tab

Use the BondWires tab to locate and assign trace models to bondwire connections. You can also modify trace models using the Model Browser.

RefDesPins Tab

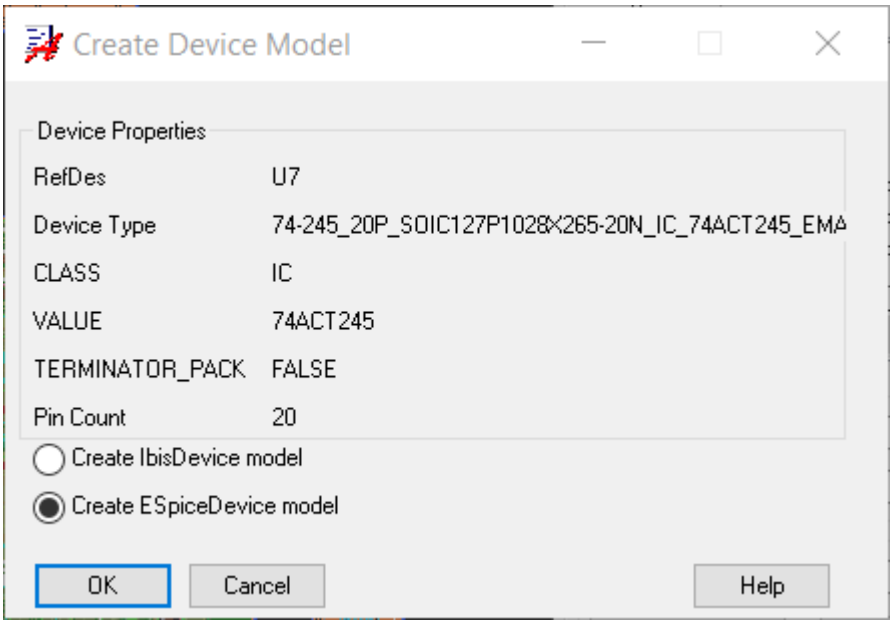
Use the RefDesPins tab to assign IOCell models to specific pins. You can also assign models to pins that have a selection of programmable buffer models.

Connectors Tab

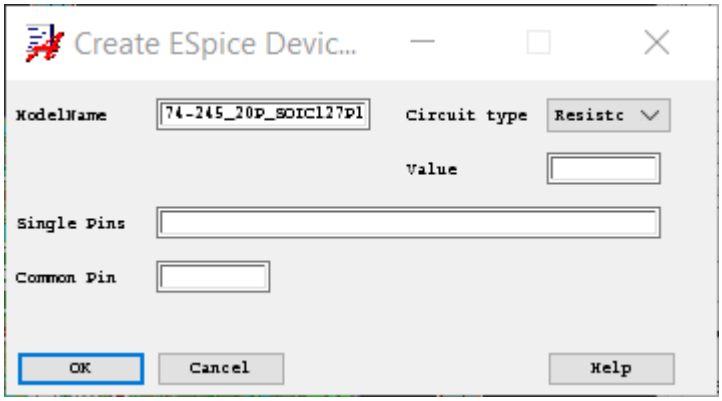
Use the Connectors tab to assign coupled connector models to components such as male/female connectors, PCI slots, and other components that connect one design to another.

- *Auto Setup* – Use this to automatically assign device models to simple components such as capacitors and resistors using the device type prefix as a reference. In order for automatic model assignment to succeed, components must have reasonable value property data in the design database.

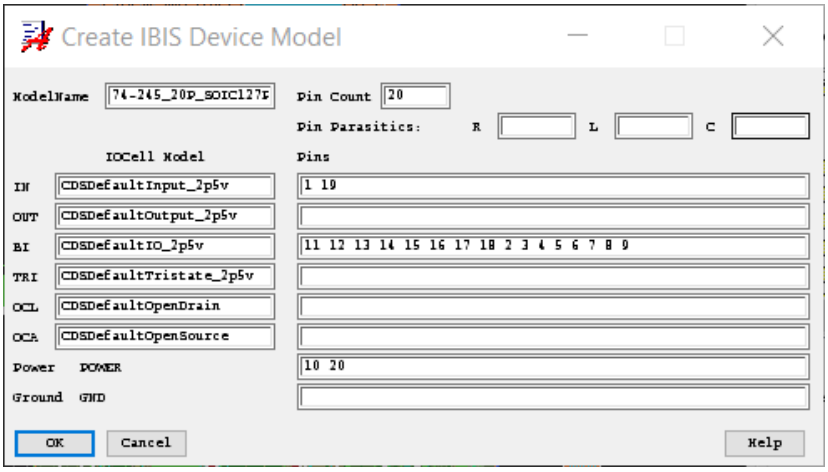
- *Create Model* — Click this button to create an ibis Device or ESpice Device model. Clicking this button opens the Create Espice Device Model dialog box.



If you select the *Create EspiceDevice Model* radio button and click *OK*, the *Create Espice Device Model* dialog is displayed where you define an Espice device model.



If you select the *Create ibisDevice Model* radio button and click *OK*, the *Create IBIS Device Model* dialog is displayed where you define an IBIS device model.



4

Integration with XtractIM

This chapter covers the following:

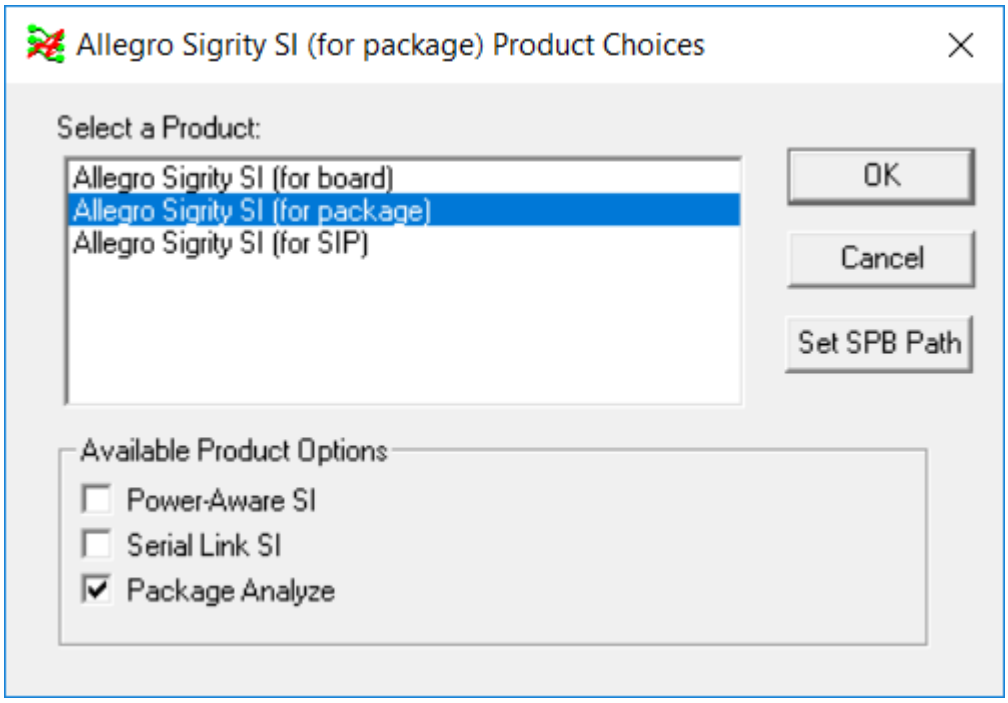
Overview

When you launch XtractIM from Allegro Sigrity SI for a package design, the workflow setup information of XtractIM is automatically completed by accessing package information stored in the design. The package information includes package type recognition, component classification, power/ground nets identification and solder ball/bump geometry.

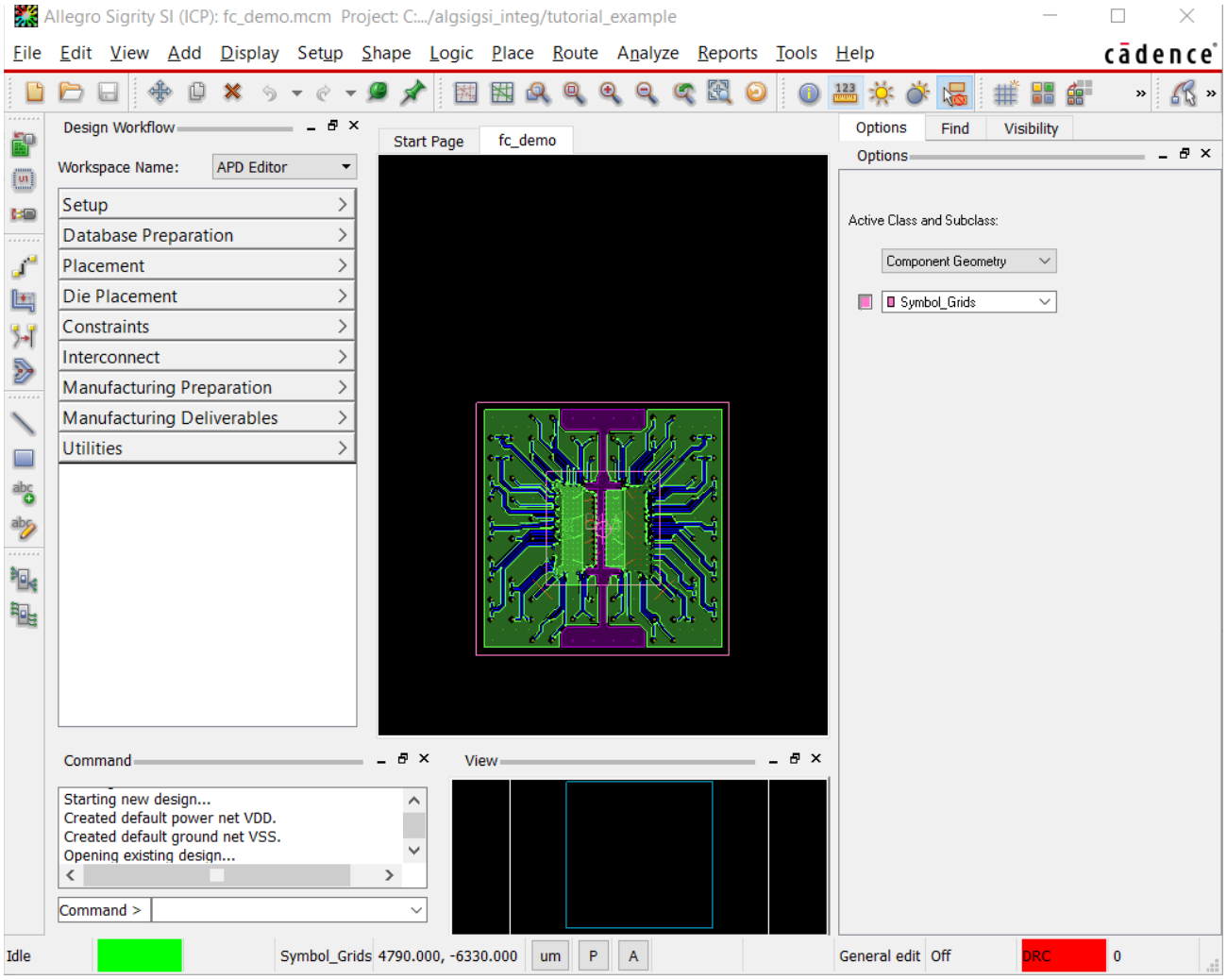
Launching XtractIM from Allegro Sigrity SI

You can launch XtractIM from Allegro Sigrity SI in two modes, XtractIM GUI mode and Batch mode. When you launch XtractIM from Allegro Sigrity SI, the *3-D Interconnect Modeling dialog* appears. This is where you specify the mode in which you want to launch XtractIM.

1. Run Allegro Sigrity SI (for package) with the *Package Analyze* product option.



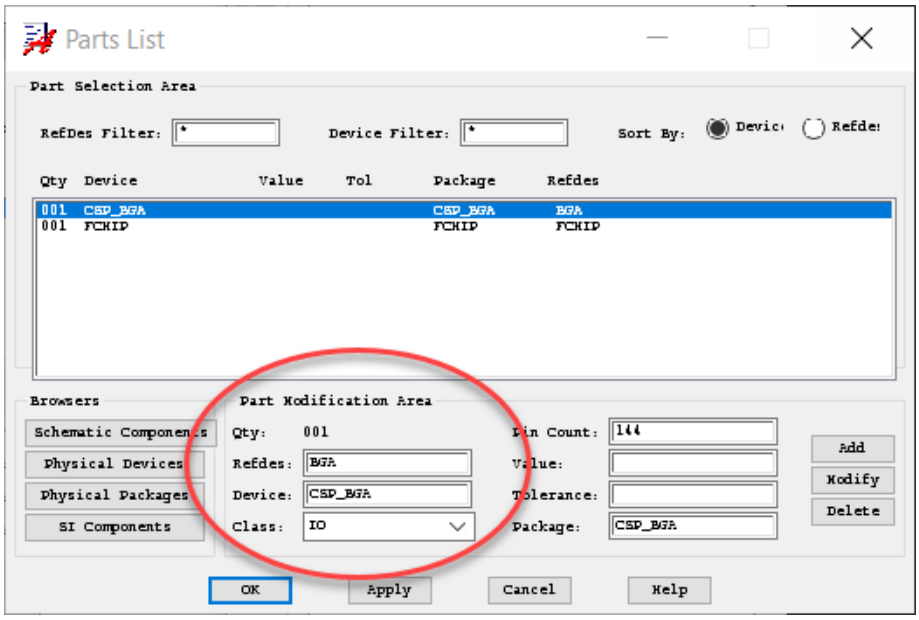
2. Open the package file `fc_demo.mcm`.



Preparing Package Information

Before you launch XtractIM from Allegro Sigrity SI, you need to prepare the packaging information for it to be usable in XtractIM. Start with classifying the component type.

1. Choose *Logic — Edit Part List* to check the component class.



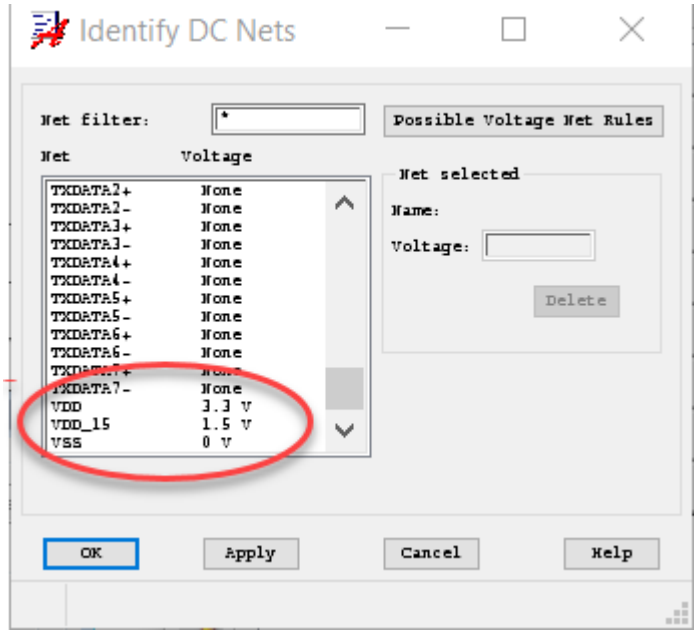
At least one component in the setup must be classified as IO type. Other Die components should be classified as IC type.

Next, you need to set up power and ground nets which will be used as reference nets in running simulation in XtractIM.

2. Choose *Logic – Identify DC Nets* to set appropriate DC value for power and ground nets.

The nets for which voltage is specified (DC nets) are recognized as power and ground nets in XtractIM.

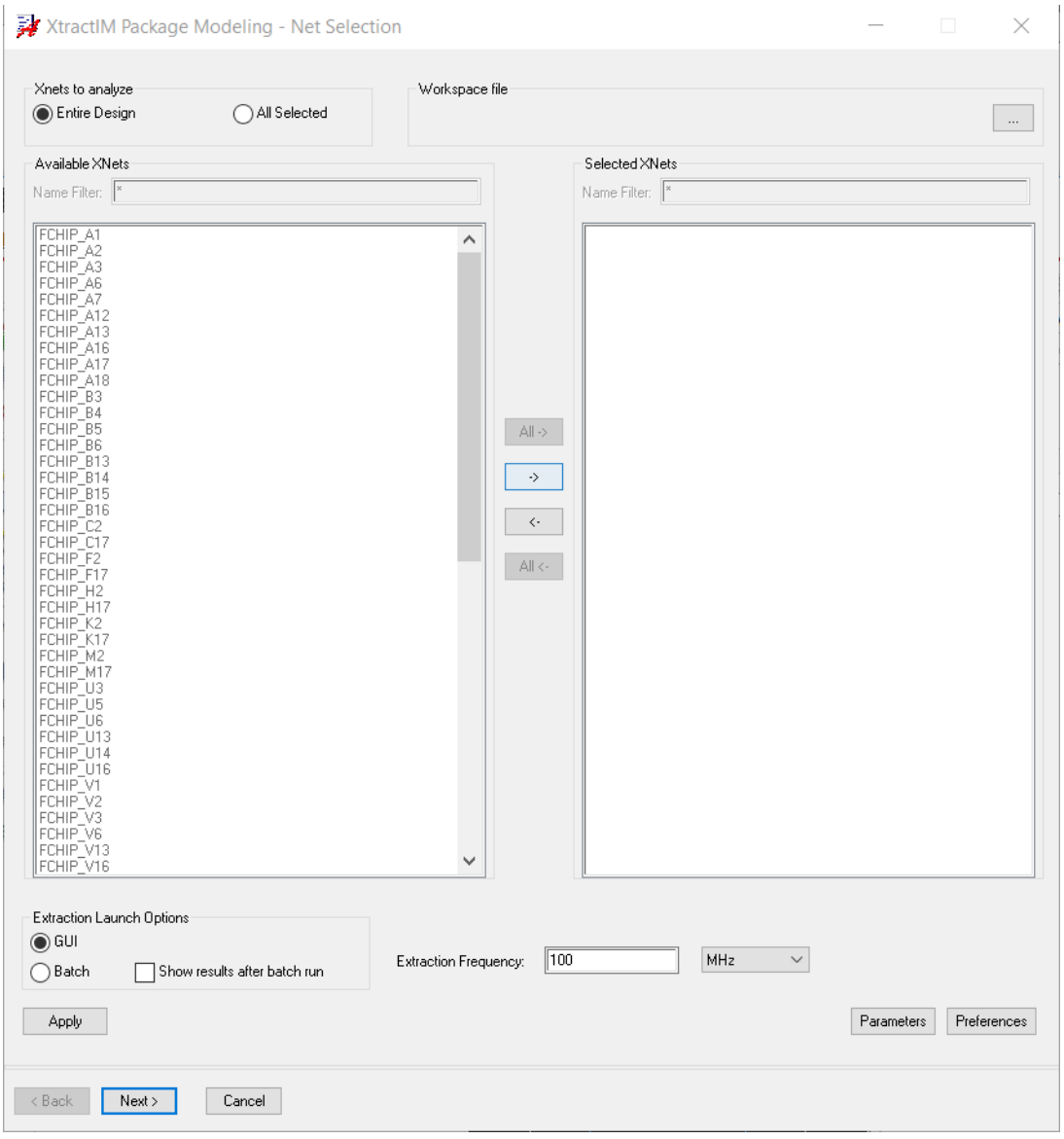
In this example, VDD and VDD_15 are the power nets and VSS is the ground net. With the DC value in nets, they will be recognized as power and ground nets in XtractIM.



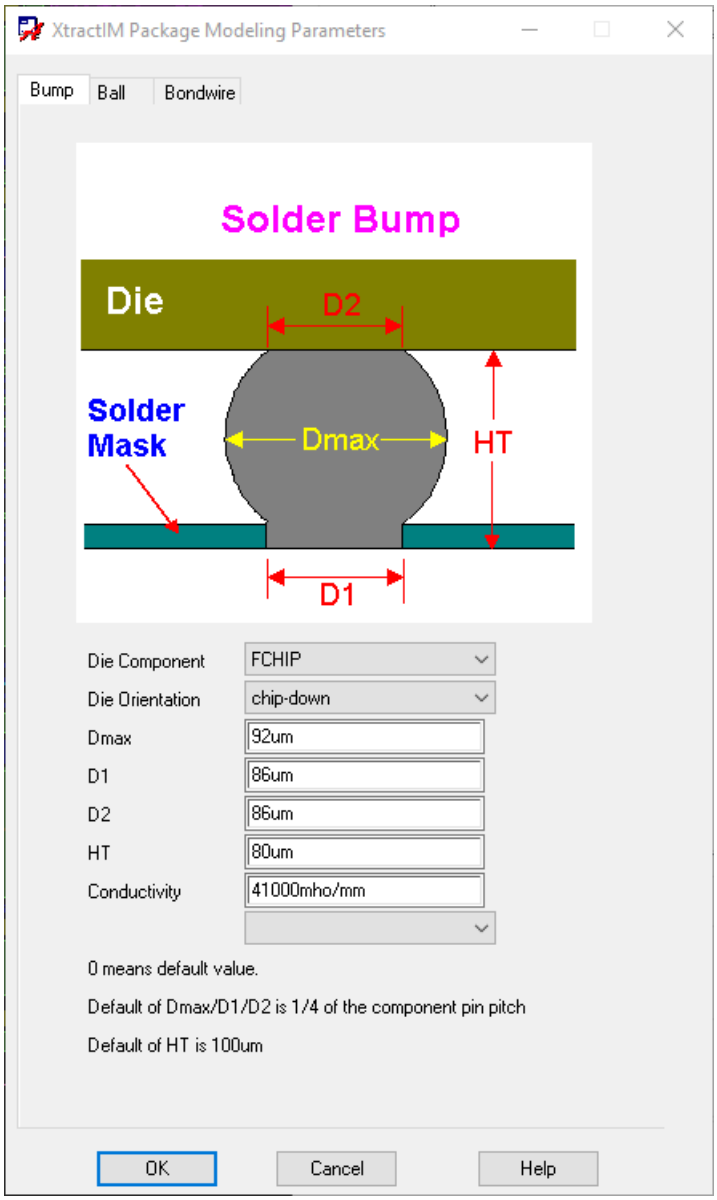
Running XtractIM Simulation

Next you need to set up solder ball and bump geometry.

1. Choose *Analyze — XtractIM — Extraction*.

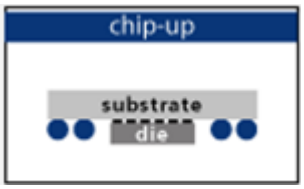
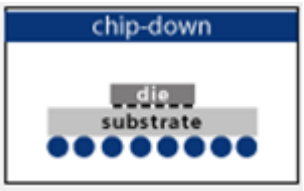


2. Click *Parameters*.



3. In the *Bump* tab, select a die component from the *Die Component* drop-down list box, to set up bump geometry. In this example, `FCHIP` is used to set up the bump geometry.

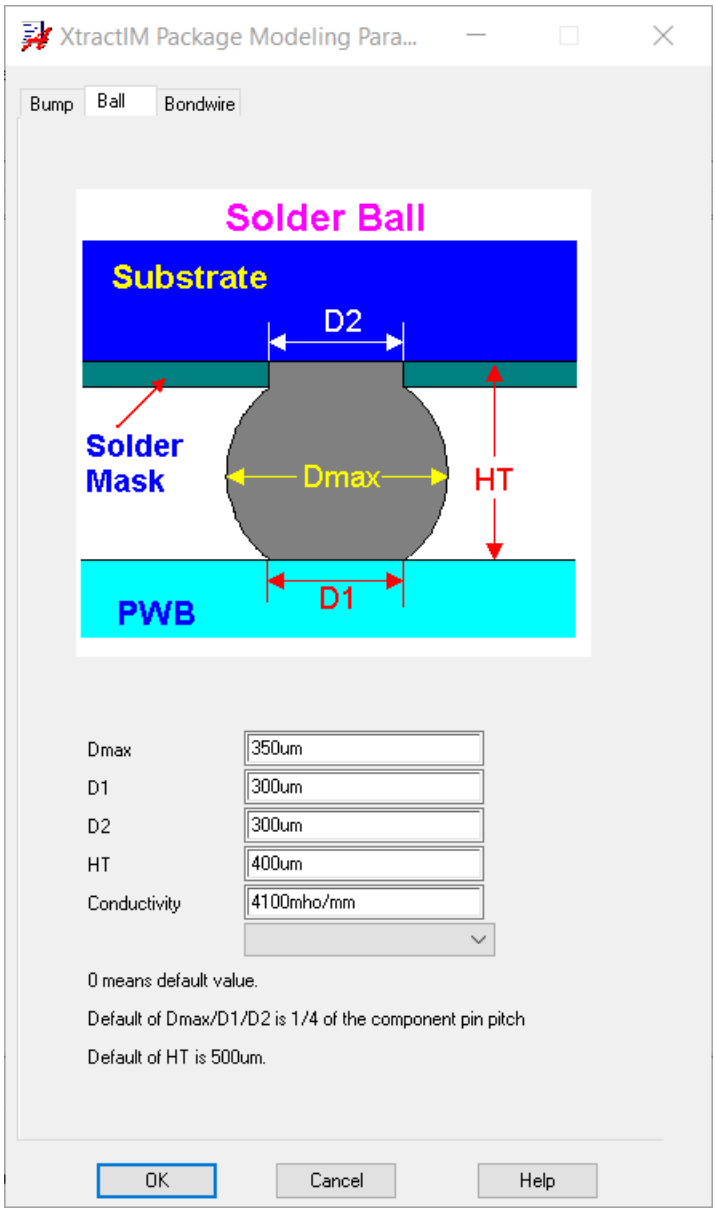
Bump Tab

Option	Description
Die Component	■ `FCHIP`: A flip chip is used as the die component. **Note:** If no value is specified, XtractIM uses the component defined in the layout. You can also choose the die component in XtractIM.
Die Orientation	Specifies the orientation of the solder bumps. It can be set to: ■ `chip-up`: The die is placed on the same side as the solder bumps.  ■ `chip-down`: The die is placed on the opposite side of the solder bumps.  **Note:** If no value is specified, XtractIM uses the orientation defined in the layout. You can also set the die orientation in XtractIM.
Dmax	Specifies the maximum diameter for the solder bumps. *Important* Using a value that is too large risks solder bump overlap.

Option	Description
D1	Specifies the bottom diameter of the solder bumps. **Note:** This value must be less than or equal to *Dmax*.
D2	Specifies the top diameter of the solder bumps. **Note:** This value must be less than or equal to *Dmax*.
HT	Specifies the height of the bumps.
Conductivity	Specifies the conductivity for the solder bumps.

Note: A value of zero for *Dmax, D1*, *D2*, or *HT* indicates that the bumps are not modeled in the layout. However, XtractIM uses 1/4th of the value of the component pin pitch as the default value of *Dmax*, *D1*, and *D2*. And, it uses `100um` as the default value of *HT*.

4. To set up the solder ball geometry, select the *Ball* tab and specify the values for the parameters.



Ball Tab

Option	Description
Dmax	Specifies the maximum diameter for the solder balls.

Option	Description
D1	Specifies the bottom diameter of the solder balls. **Note:** This value must be less than or equal to *Dmax*.
D2	Specifies the top diameter of the solder balls. **Note:** This value must be less than or equal to *Dmax*.
HT	Specifies the height of the balls.
Conductivity	Specifies the conductivity for the solder balls.

Note: A value of zero for *Dmax, D1*, *D2*, or *HT* indicates that the balls are not modeled in the layout. However, XtractIM uses 1/4th of the value of the component pin pitch as the default value of *Dmax*, *D1*, and *D2.* And, it uses `500um` as the default value of *HT*.

5. To set up the bondwire modeling compound relative permitivity, select the *Bondwire* tab.

   By default, the *Modeling Compound Relative Permitivity (Er)* is set to `3`.

   You can either specify another value manually. Or, choose a compound from the drop-down list box, and the relative permitivity is set accordingly.

6. Click *OK* to close the dialog.

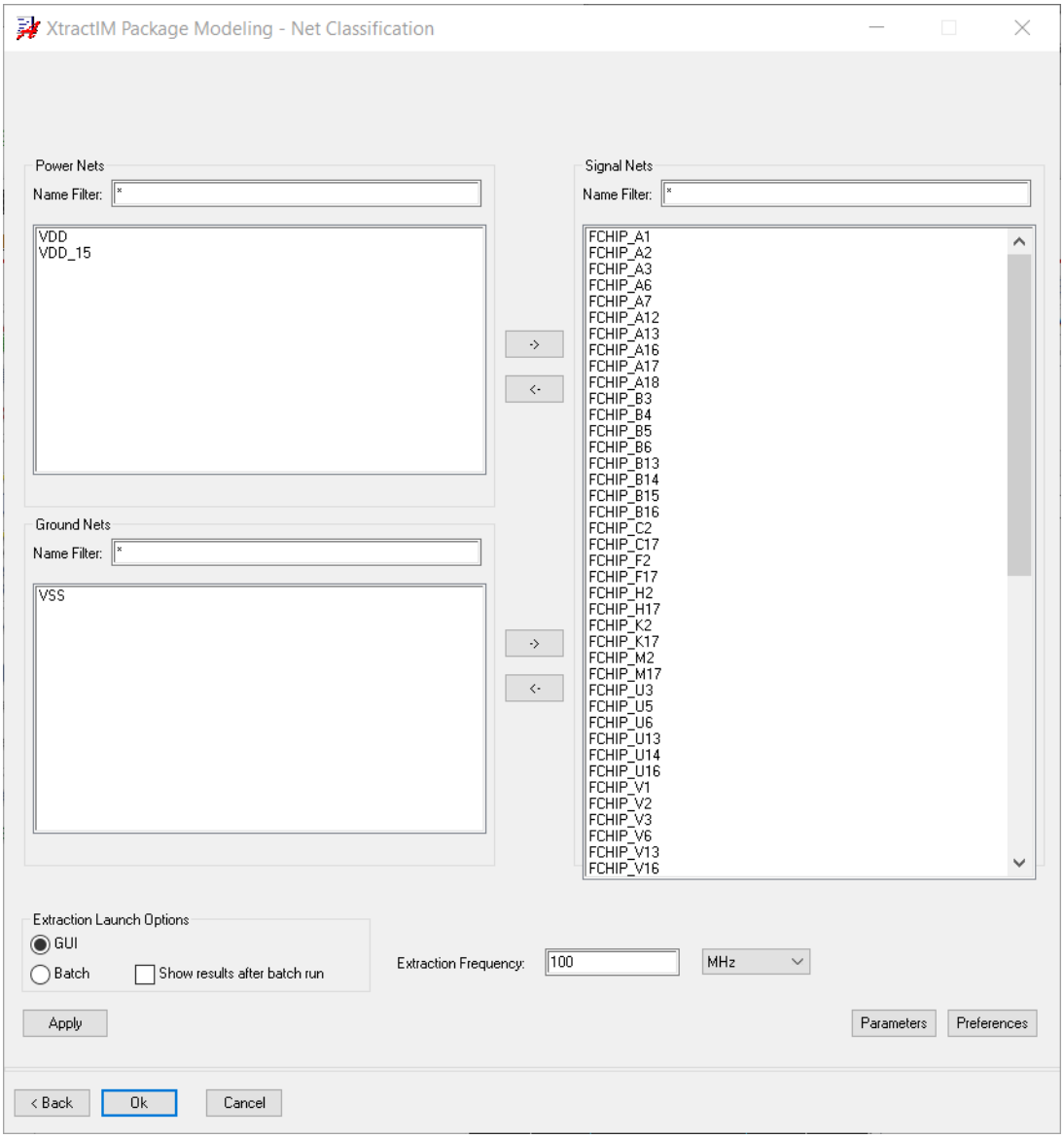
7. Back in the XtractIM Package Modeling - Net Selection dialog, set the extraction frequency. The default value is `100MHz`.

Note that there are two modes to start XtractIM:

- *Batch mode*: In the batch mode, you need to select the nets to be analyzed and specify the extraction frequency. The workspace file (`.ximx`) is automatically generated based on the APD/SiP database and XtractIM is run in batch mode. The RLCG and SPICE model are generated in the same job folder.
- *GUI mode*: In the GUI mode, the workflow setup is automatically completed when launching XtractIM from Allegro Sigrity SI. The workspace file (`.ximx`) is automatically generated based on the APD/SiP database for the selected nets. You can then proceed to run XtractIM in either extraction or electrical performance assessment modes.

GUI mode is selected by default.

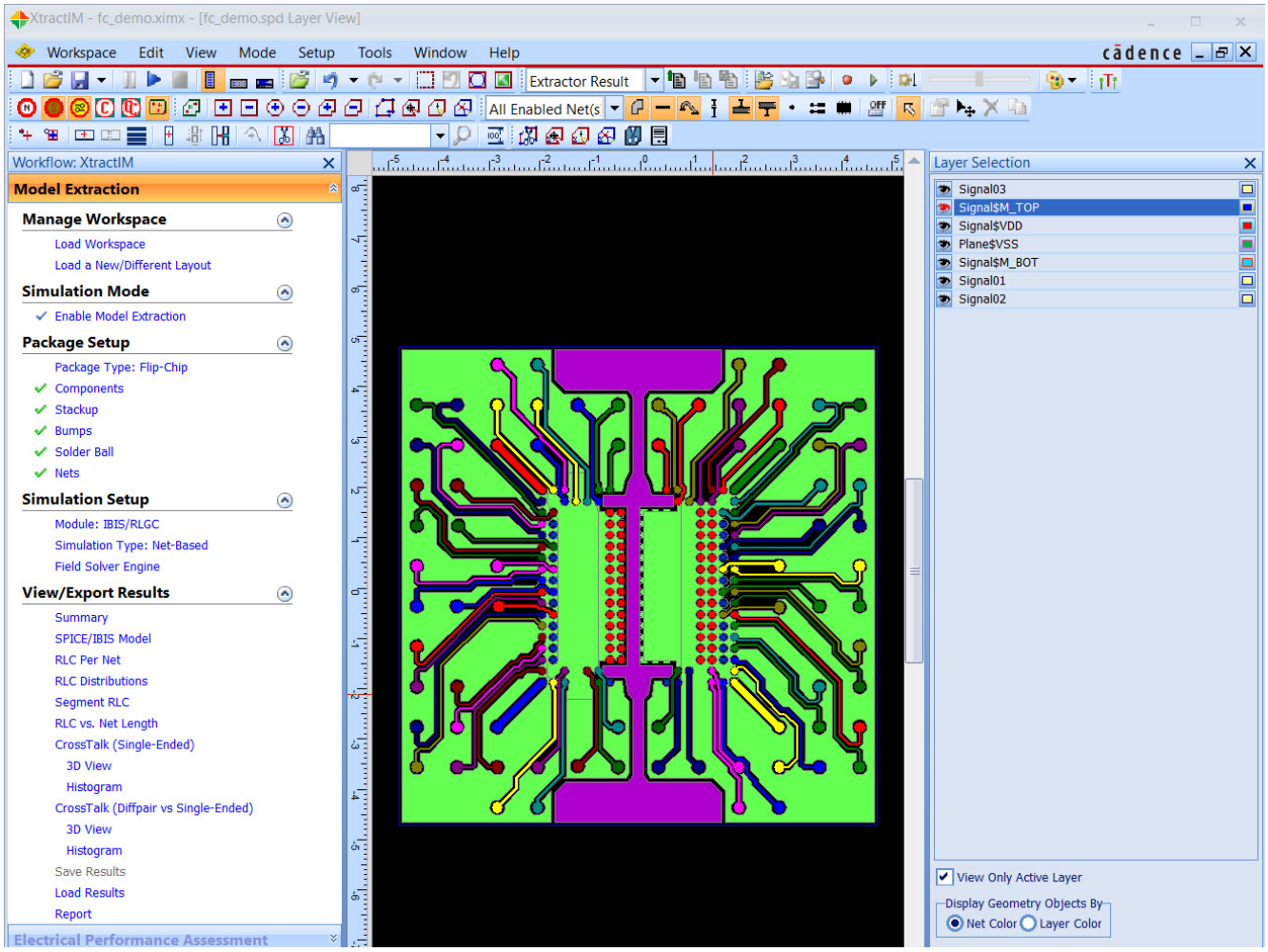
8. Click *Next*. The XtractIM Package Modeling - Net Selection dialog appears.



Here you can classify the nets as Power Nets, Ground Nets, or Signal Nets.

9. Click *OK*.

XtractIM is launched with the complete package setup done, and it is ready for model extraction and electrical performance assessment.



However, if you start XtractIM in *Batch mode*, XtractIM Model Extraction is run in the background and the RLC table and SPICE and IBIS mode are generated in the same folder as the package design.