

Allegro® X User Guide

Product Version 23.1
September 2023

© 2023 Cadence Design Systems, Inc. All rights reserved.

Portions © Apache Software Foundation, Sun Microsystems, Free Software Foundation, Inc., Regents of the University of California, Massachusetts Institute of Technology, University of Florida. Used by permission. Printed in the United States of America.

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Allegro Platform tools contain technology licensed from, and copyrighted by: Apache Software Foundation, 1901 Munsey Drive Forest Hill, MD 21050, USA © 2000-2005, Apache Software Foundation. Sun Microsystems, 4150 Network Circle, Santa Clara, CA 95054 USA © 1994-2007, Sun Microsystems, Inc. Free Software Foundation, 59 Temple Place, Suite 330, Boston, MA 02111-1307 USA © 1989, 1991, Free Software Foundation, Inc. Regents of the University of California, Sun Microsystems, Inc., Scriptics Corporation, © 2001, Regents of the University of California. Daniel Stenberg, © 1996 - 2006, Daniel Stenberg. UMFPACK © 2005, Timothy A. Davis, University of Florida, (davis@cise.ulf.edu). Ken Martin, Will Schroeder, Bill Lorensen © 1993-2002, Ken Martin, Will Schroeder, Bill Lorensen. Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, Massachusetts, USA © 2003, the Board of Trustees of Massachusetts Institute of Technology. vtkQt - copyright 2000-2005 Matthias Koenig. All rights reserved.

Trademarks: Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522.

Open SystemC, Open SystemC Initiative, OSCI, SystemC, and SystemC Initiative are trademarks or registered trademarks of Open SystemC Initiative, Inc. in the United States and other countries and are used with permission. All other trademarks are the property of their respective holders.

Restricted Permission: This publication is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this publication, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this publication subject to the following conditions:

1. The publication may be used only in accordance with a written agreement between Cadence and its customer.
2. The publication may not be modified in any way.
3. Any authorized copy of the publication or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
4. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

Disclaimer: Information in this publication is subject to change without notice and does not represent a commitment on the part of Cadence. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information. Cadence is committed to using respectful language in our code and communications. We are also active in the removal and/or replacement of inappropriate language from existing content. This product documentation may however contain material that is no longer considered appropriate but still reflects long-standing industry terminology. Such content will be addressed at a time when the related software can be updated without end-user impact.

Restricted Rights: Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor.

Contents

Allegro User Guide 5

The Allegro® Layout Editors Information Set 5

Allegro X User Guide

Allegro User Guide

The Allegro® Layout Editors Information Set

The information set for Cadence® Allegro® layout editor information set consists of fourteen books. These books explain features of the layout editors, Allegro® PCB Editor and Allegro® Package Designer Plus (APD Plus). If a feature is available in only one of the layout editors, either a note is provided mentioning the tool or the title of the topic is marked as such.

These books are available in *Cadence Help* under *Allegro User Guide*. All documentation is accessible from the *Help – Documentation* menu in the layout editors.

The following table lists book names and their descriptions. The order of books two through nine correspond to a typical PCB design flow.

Manual Name	Description
<u>Getting Started with Physical Design</u>	Describes the user interface of the layout editors. It also contains information on generic functions, setup and configuration information, and on the front-to-back flows.
<u>Defining and Developing Libraries</u>	Describes how to create libraries – a collection of graphic symbols – representing packages, mechanical elements, drawing formats, and custom pads and padstacks.
<u>Transferring Logic Design Data</u>	<p>Describes how to transfer native and third-party design logic data to the back-end layout editors such as PCB Editor and Allegro Package Design Plus(APD Plus); and how to backannotate that data.</p> <p>Native logic transfer refers to the data derived from the Cadence schematic design capture tools, such as Allegro System Capture, Allegro Design Entry HDL, System Connectivity Manager, or Allegro PCB Design CIS.</p>

Preparing the Layout

Describes the tasks involved in the preparation of a layout, before placing components in the design:

- Defining the layout cross-section
- Adding graphic elements
- Editing layout padstacks and pad shapes
- Creating interactive blind and buried vias
- Creating and editing etch/conductor shapes

Creating Design Rules

Describes how to create and modify design rules for a design. The topics included are:

- Design Rule Checking (DRC)
- Properties
- Constraints
- Defining the layout cross-section

Placing the Elements

Describes how to place elements manually and automatically, and how to swap pins, functions, and components after placement.

Routing the Design

Describes how to perform basic and automatic routing in the physical designs and post-routing tasks. Topics included are:

- Interactive routing
- Automatic routing with Allegro PCB Router
- Glossing to improve the appearance and manufacturability of a physical design.

Allegro X User Guide

Allegro User Guide

Completing the Design

Describes tasks performed before sending a design out for fabrication:

- Renaming reference designators
- Running audits
- Extracting information from your design
- Generating coupons

Preparing Manufacturing Data

Describes the processes to create manufacturing data and the output files generated as a result of these processes:

- Numerically controlled (NC) drills and routers
- Silkscreen
- Penplotting
- Artwork (photocopying)

SKILL Reference

Describes the AXL (Allegro eXtension Language) use model, how to start AXL, and how to use each AXL function.

Working with RF PCB

Describes a unified design solution for complex mixed-signal projects. From the schematic, to layout, to manufacturing, a total front-to-back design flow that helps in streamlining entire RF design process.

High Density Interconnect (HDI)

Describes the key aspects of HDI requirements and the features supporting them, such as microvias, DRCs for same net and net-net conditions, unused inner-layer pad removal, rules for via tangency (vias touch but do not overlap) and stacking (coincident location of the adjacent layer vias), and dynamic filleting.

Allegro X User Guide

Allegro User Guide

Allegro Timing Environment

Describes methodologies for solving timing relationships (differential phase, match groups and relative match groups) and other delay related constraints using the ATE (Allegro Timing Environment).

This environment contains technology focused on visualizing and solving the delay issues.

Getting Started with Symphony Team Design

Describes team design methodologies for working in a concurrent and collaborative environment.

[Allegro Layout Editor Environment Variables Reference](#)

Describes user preference environment variables.

[Allegro Layout Editor Design Parameters Reference](#)

Describes layout editor design parameters.