cadence®

Allegro® X
Constraint Manager with PCB Editor
Tutorial

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Contents

Introduction to the Tutorial

Design rules are known as Constraints in the PCB Editor. These rules must be followed while routing the design. You can define spacing and physical design rules within the PCB Editor user interface using the Constraint Manager.

The Allegro Constraint Manager Tutorial describes the different types of physical and spacing constraints that you can capture in Constraint Manager. You learn to create and assign them in Constraint Manager and see the effect while routing.The tutorial also highlights the tight integration between Constraint Manager, and PCB Editor.

A constraint is a user-defined restriction applied to an object when it is routed and placed on the board. The tutorial focuses on the following procedures:

- Setting up default constraints
- Capturing Physical and Spacing constraints
- Setting up constraints modes
- Routing with constraints
- Constraints DRC

Audience

This tutorial is designed for the Allegro PCB Editor users. Constraint Manger, when connected to PCB Editor helps you capture physical and spacing constraints.

Prerequisites

It is assumed that you are familiar with PCB Editor but not with Constraint Manager. The scope of this tutorial does not include details of various modes and properties in PCB Editor but will cover basic Constraint Manager procedures in detail.

Note: To learn about PCB Editor, see the *Allegro X PCB and Package User Guide: Getting Started with Physical Design*.

Advantages of Using Constraint Manager with Allegro PCB Editor

Constraint Manager is a spreadsheet-based application with an easy-to-use interface for entering constraints. Another advantage of using Constraint Manager is that it allows you to create generic constraints that you can apply to multiple nets or Xnets at the same time. These reusable constraints are called CSets (Constraint Sets). At a later point in time, if your design requirements change, you can edit the generic rule. The updated rule will be automatically applied to the nets or Xnets that refer to the rule. The existing routes will not modify, but may show DRCs.

Using the Tutorial

To use the Allegro Constraint Manager you need the following tools and Tutorial Database:

- Constraint Manager
- PCB Editor

Note: The Allegro PCB Editor suite contains all these tools.

Tutorial Database

To run the tutorial, you need to unzip the design files and copy them to your local machine. The design files contain the Board and the other files required to perform the procedures explained in this tutorial.

Before using the tutorial, ensure that you do the following:

- Unzip the file <*your_inst_dir*>/doc/algroCM_tut/tutorial_examples/project.zip on Windows or <*your_inst_dir*>/doc/algroCM_tut/tutorial_examples/project.t.Z on UNIX and save it locally to your work area.

  Ensure that this work area where you extract the samples is a local directory for which you have write permissions.

- For the commands specified in the tutorial, you need to replace your work area with the name of the local directory in which you have copied the samples.
- Ensure that you unset the CDS_SITE environment variable on your computer if it is set.

Understanding the Tutorial Database Structure

The design database consists of the following directories and files:

Directory/File	Purpose
.brd	This is the layout file

Summary

The Allegro Constraint Manager with Allegro PCB Editor Tutorial should be used by layout designers who want to capture physical and spacing constraints while implementing the logic of the design. Constraint Manager lets you set constraints in a convenient, faster, and error-free manner.

What's Next

In the next chapter, Setting Physical Constraints on Nets, you will use Constraint Manager with Allegro PCB Editor for setting physical constraint. You will set the default values for constraints, create constraint set for nets, net class, assign constraint set, route, set up analysis mode.

Recommended Reading

For more information about the Constraint Manager tool, see the *Allegro Constraint Manager User Guide*

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Setting Physical Constraints

Objectives

To learn how to set physical constraints on nets in your layout using Constraint Manager and route with them in Allegro PCB Editor.

At the end of the lesson, you will be able to

- Set up default physical constraints
- Create physical constraint set
- Set constraint set values for Line Width, Neck Width, Max Neck Length and Via list
- Create Net Class
- Assign physical constraint set to Objects
- Route with Physical Constraints

Nature of Chapter

Skill (includes concepts and practice).

Starting Allegro PCB Editor

Task Overview

You will start Allegro PCB Editor and open the `start_allegro_cm.brd` file in it.

Steps

1. In Unix, launch Allegro PCB Editor by typing the following command in the command window:

   ```
   allegro
   ```

   -Or-

   On Windows, launch PCB Editor from *Start – Cadence PCB 2023 – Allegro PCB Editor 2023.*

   The PCB Editor Product Choices dialog box is displayed.

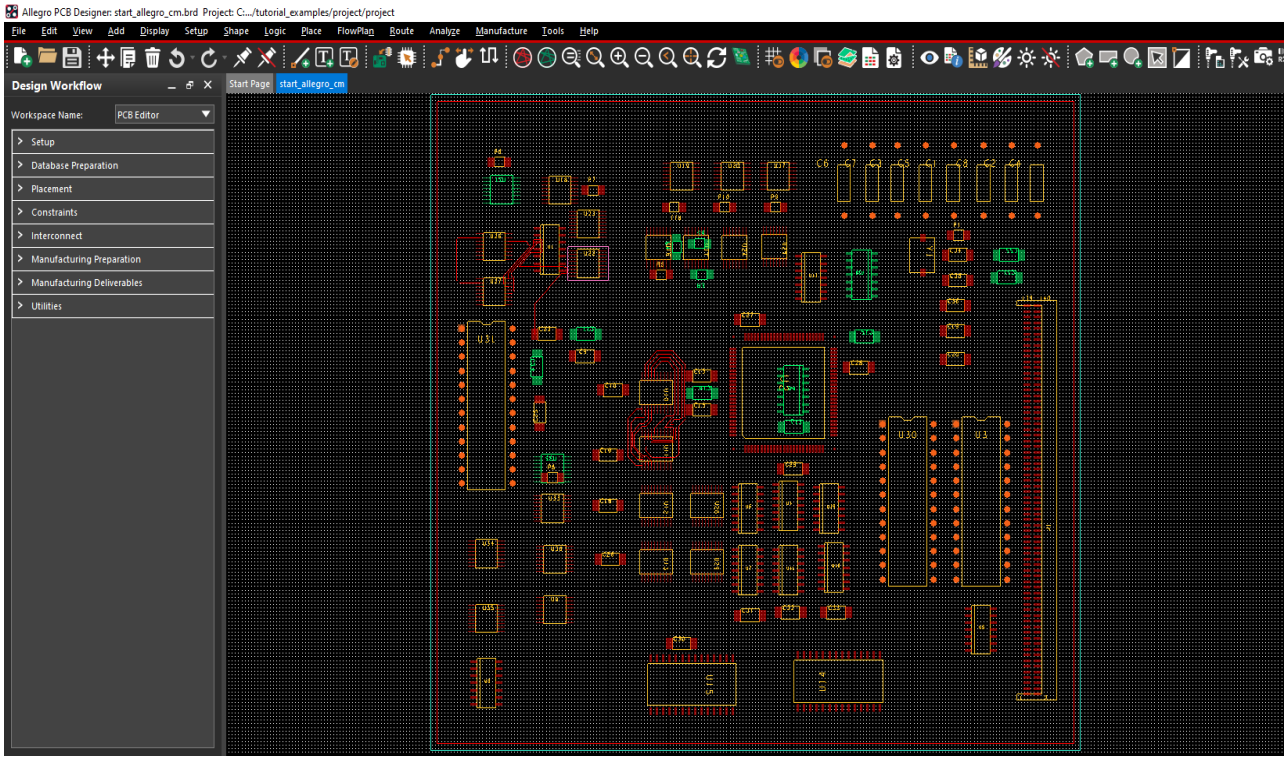
   Note: If you have set the default suite previously, the Allegro PCB Editor window opens automatically and you can skip step 2.

2. Select *Allegro PCB Designer*.

   The Allegro PCB Designer window appears.

3. Locate and open the `start_allegro_cm.brd` file.

The Allegro PCB Designer window opens showing the layout for `start_allegro_cm.brd` as follows:



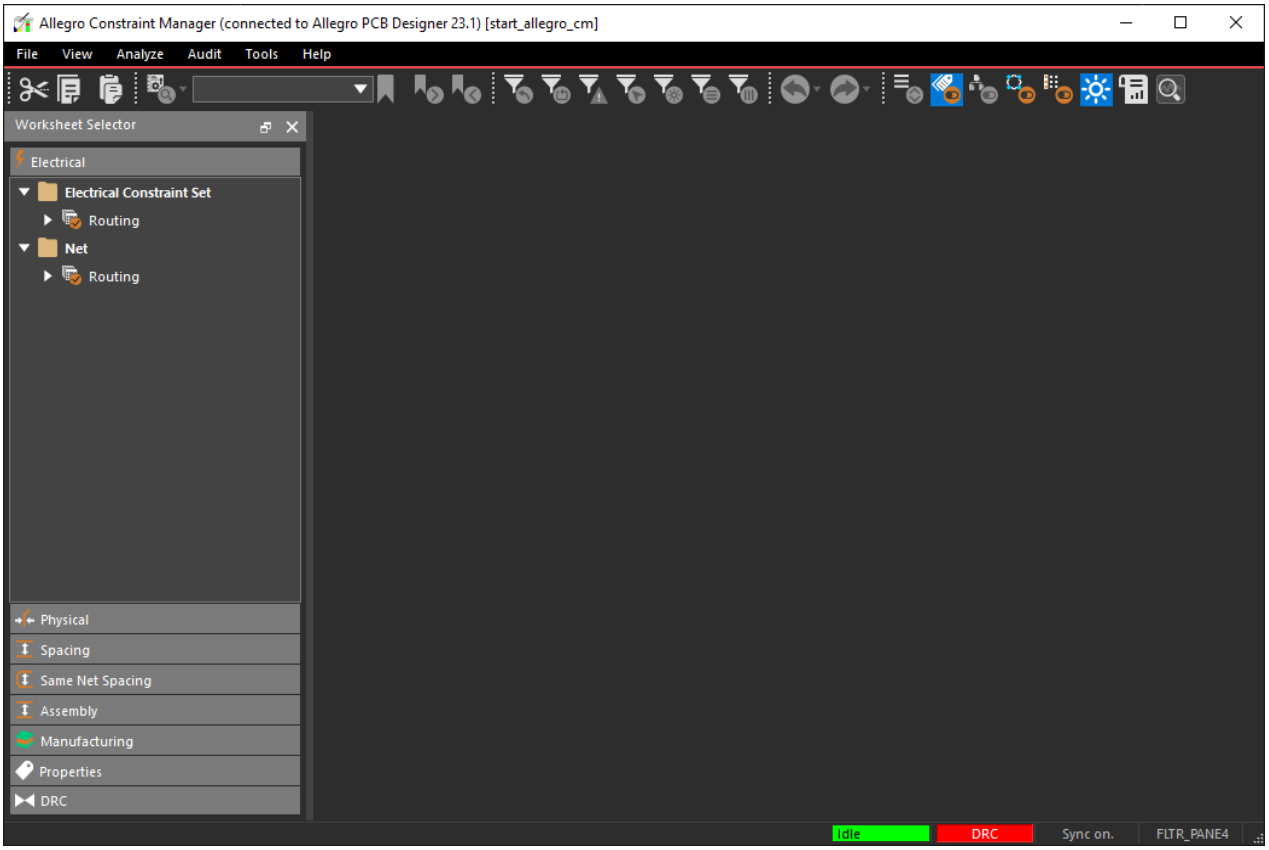
Starting Constraint Manager

Task Overview

You will start Constraint Manager from PCB Editor and create physical constraints.

Steps

1. In PCB Editor, choose *Setup – Constraints – Constraint Manager*.



Note: The title bar of the Constraint Manager window shows that Constraint Manager is launched from Allegro PCB Editor.
For details on the Constraint Manager user interface, refer to *Constraint Manager User Guide.*

The Constraint Manager spreadsheet is set up hierarchically. You can expand or contract any domain by clicking the domain name.

Setting Physical Constraints

A Physical Constraint is a rule that characterizes and constrains the physical instantiation of a net. For example Line Width and layer and via restrictions. Physical constraints apply to both the Xnet and Net level.

Allegro PCB Editor has a set of predefined rules and you can define values for each of these rules within the context of a constraint set. A Physical Constraint Set (Physical CSet) consists of one value per layer for each physical constraint.

The Allegro Constraint Manager provides two categories of constraint sets:

- DEFAULT
- Special

The DEFAULT CSet is used to specify the rules to be applied to nets that have no special routing requirements.These values will take effect if you do not explicitly assign a constraint.

Nets that need different rules applied to them fall into the Special category. For these nets, you must identify the nets requiring the special rules, and also create and set the special rule values.

Modifying DEFAULT Physical Constraint Set Values

The values of the DEFAULT CSets are predefined, but you can modify them to suit your design requirements. When you edit DEFAULT CSet values, all objects that reference the CSet will automatically inherit these changes.

Note: You cannot delete or rename the DEFAULT Physical CSet.

Task Overview

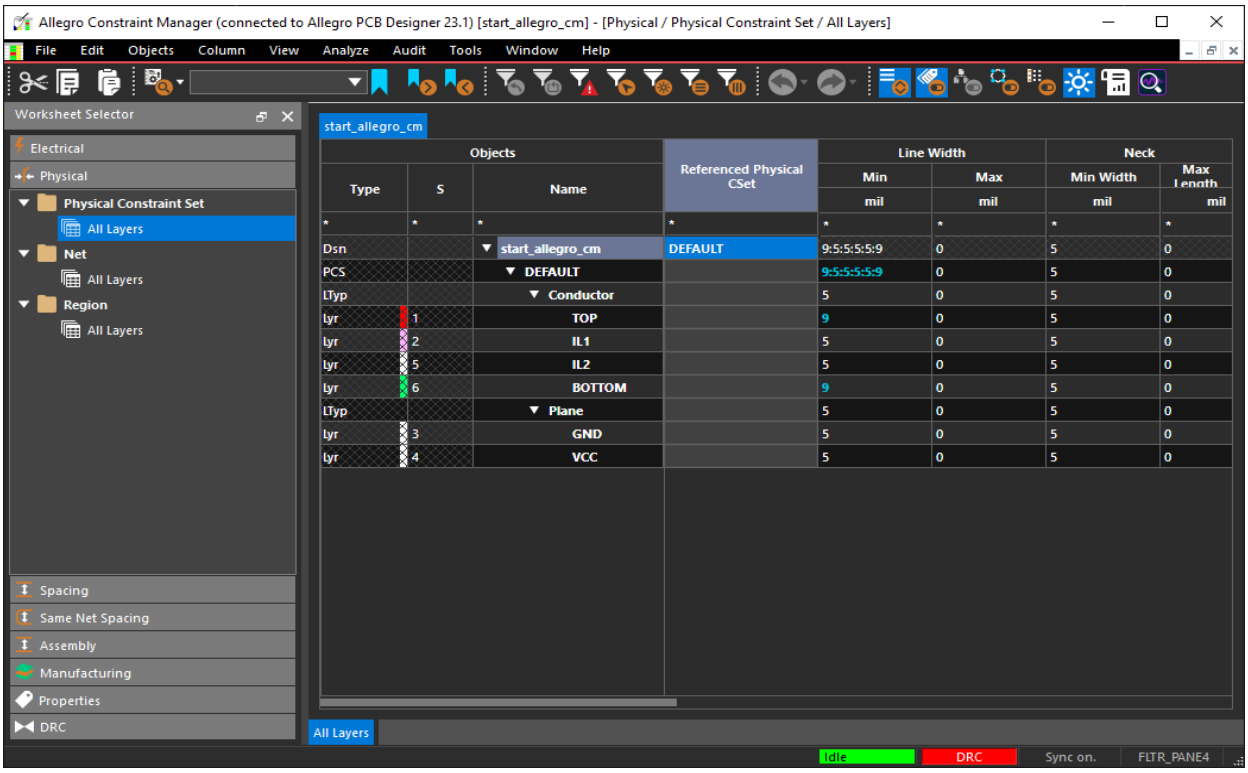
You will now modify the values of DEFAULT Physical CSet for all the layers.

Steps

1. In the *Physical Constraint Set* workbook, click *All Layers*.

   The *All Layers* worksheet appears. Notice the *Line Width, Neck, Differential Pair, Vias, BB Via Stagger, and Allow* tabs in this workbook. All the layers are displayed

under groups as Hierarchical layer types: Conductor and Plane in the worksheet in the right pane.



Note: You can see the design layers that are listed under DEFAULT Physical constraint set.

2. Right-click the *Min Line Width* column for DEFAULT and select *Change*.

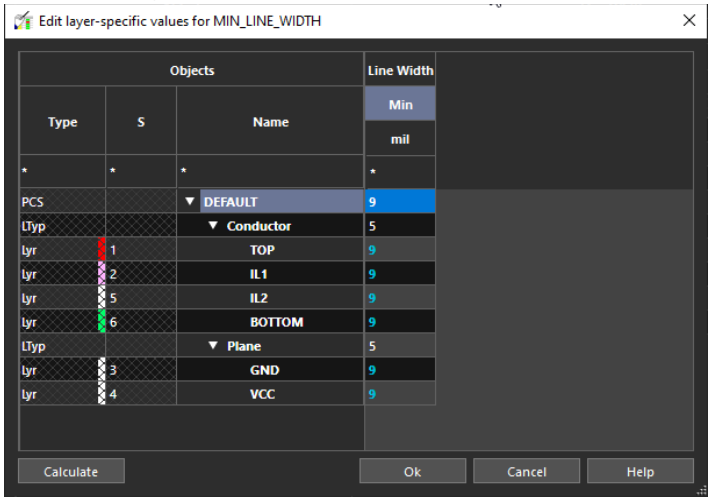
   Since layers have different values, the *Edit layer-specific values* window appears.

Note: The minimum line width is the minimum width of cline segment.

3. Expand DEFAULT and select layer IL1.
4. Change the value of IL1 from 5 to 9.
5. Similarly, change the value for layers GND, VCC and IL2 from 5 to 9.

Note: You can assign value to hierarchical layers Conductor and Plane. The values will be inherited by all the child layers.

6. Click *Ok* to apply the changes.



7. Close Constraint Manager.
8. Save the layout by choosing *File - Save* from the Allegro PCB Editor main menu.

Creating a new Physical Constraint Set from DEFAULT Physical CSet

You can create different rules for special nets which have values different from the DEFAULT CSet.

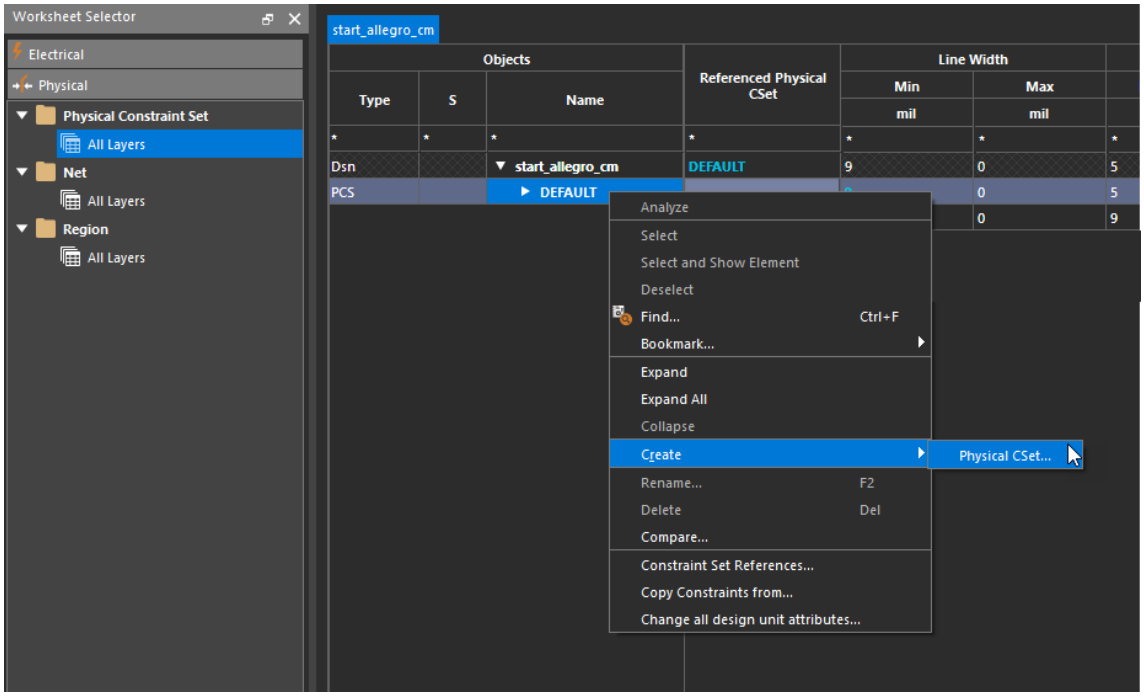
Task Overview

You will create Physical CSet from the DEFAULT and assign constraints to it.

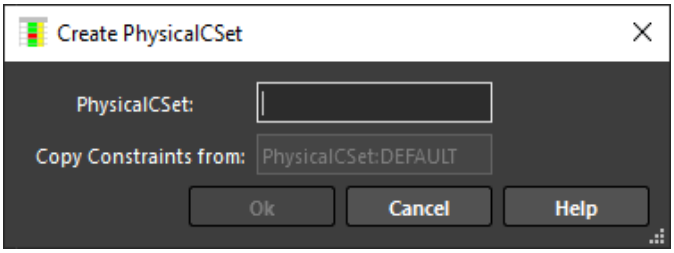
Steps

1. Open Constraint Manager and select *Physical* domain.
2. Select *All Layers* worksheet under *Physical Constraint Set* workbook.

3. Click the DEFAULT cell under the *Name* column and right-click to select *Create – Physical CSet menu item.*

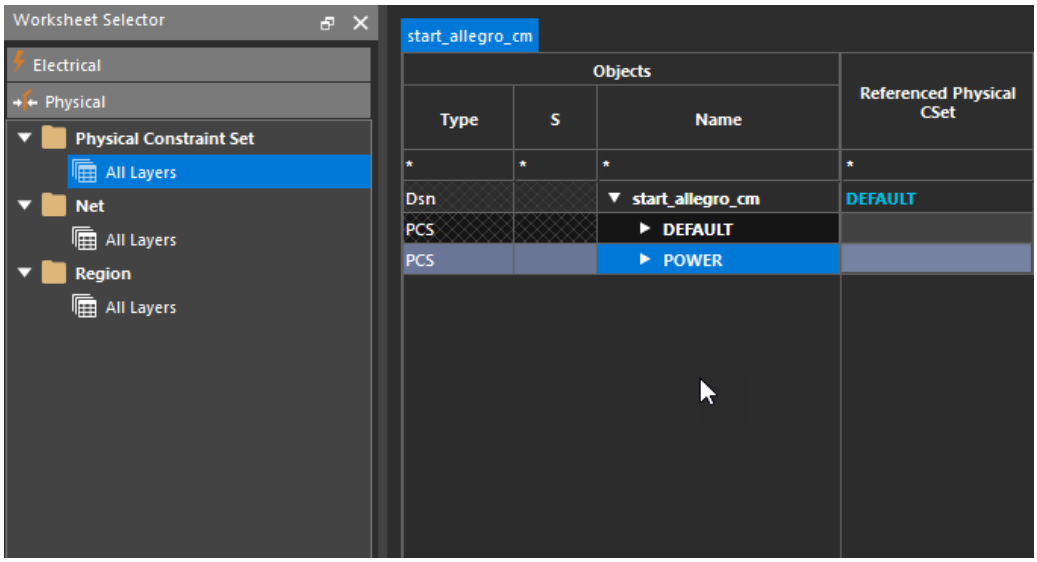


The *Create PhysicalCSet* dialog box appears.



4. Enter the new Physical CSet name as `POWER` in the *PhysicalCSet* field.
5. Click *Ok*.

The instance of the CSet POWER is displayed in the *Objects* column.



You will now enter the new values to the rules.

6. Select the *Min Line Width* value and double-click to change it to 15.

Tip

You can use `Tab` key to navigate along the spreadsheet.

7. Select *Min Neck Width* value and double-click to change it to 9.
8. Select *Max Neck Length* value and double-click to change it to 500.
9. Double-click the *Via* constraint.

   The *Edit Via List* dialog is displayed.
10. Double-click a via from the *Select a via from the library or database* list to add it to the *Via list*.

11. Select the via and click *Up* to move it up in the *Via list*.

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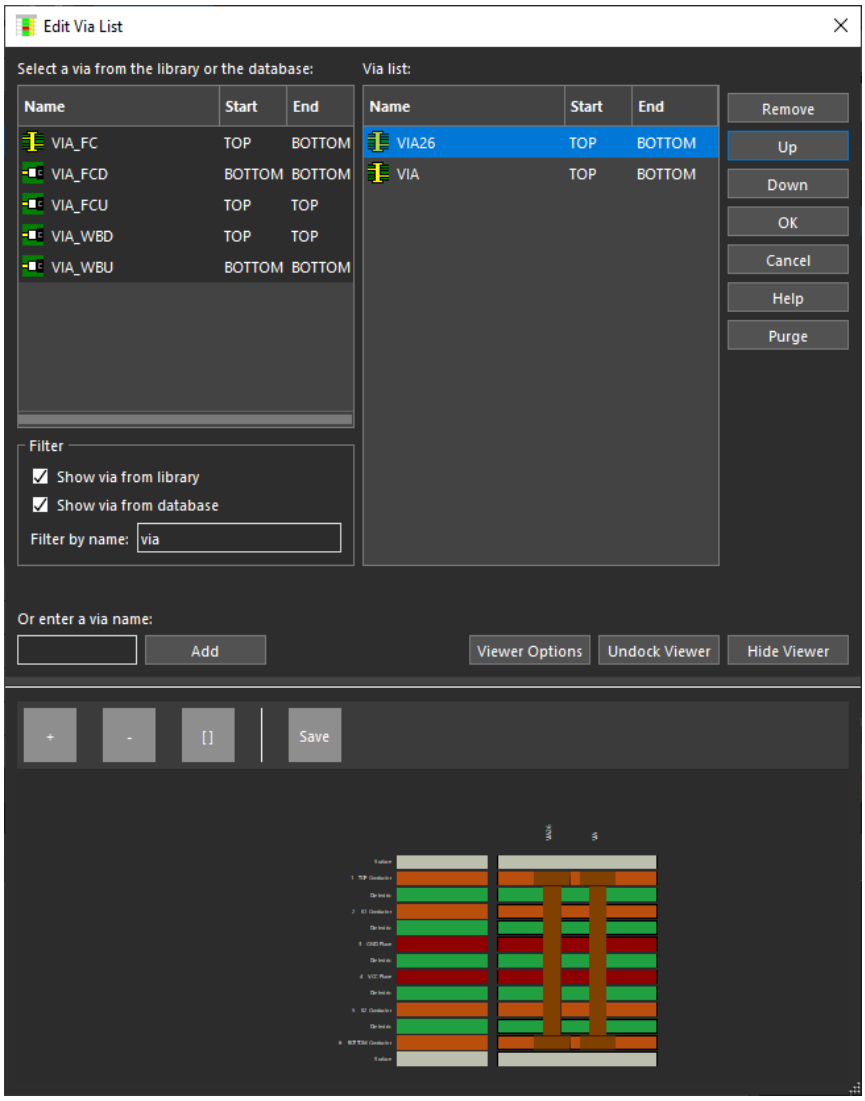

12. Click *OK*.

The *Edit Via List* dialog box closes.

13. Close Constraint Manager.

Creating a new Physical Constraint Set from existing Physical CSet

Task Overview

You will create Physical CSet from the existing CSet and assign values to it.

Steps

1. Open Constraint Manager and select *Physical* domain.
2. Select *All Layers* worksheet under *Physical Constraint Set* workbook.
3. Select POWER CSet in the worksheet and choose *Objects – Create – Physical CSet.*

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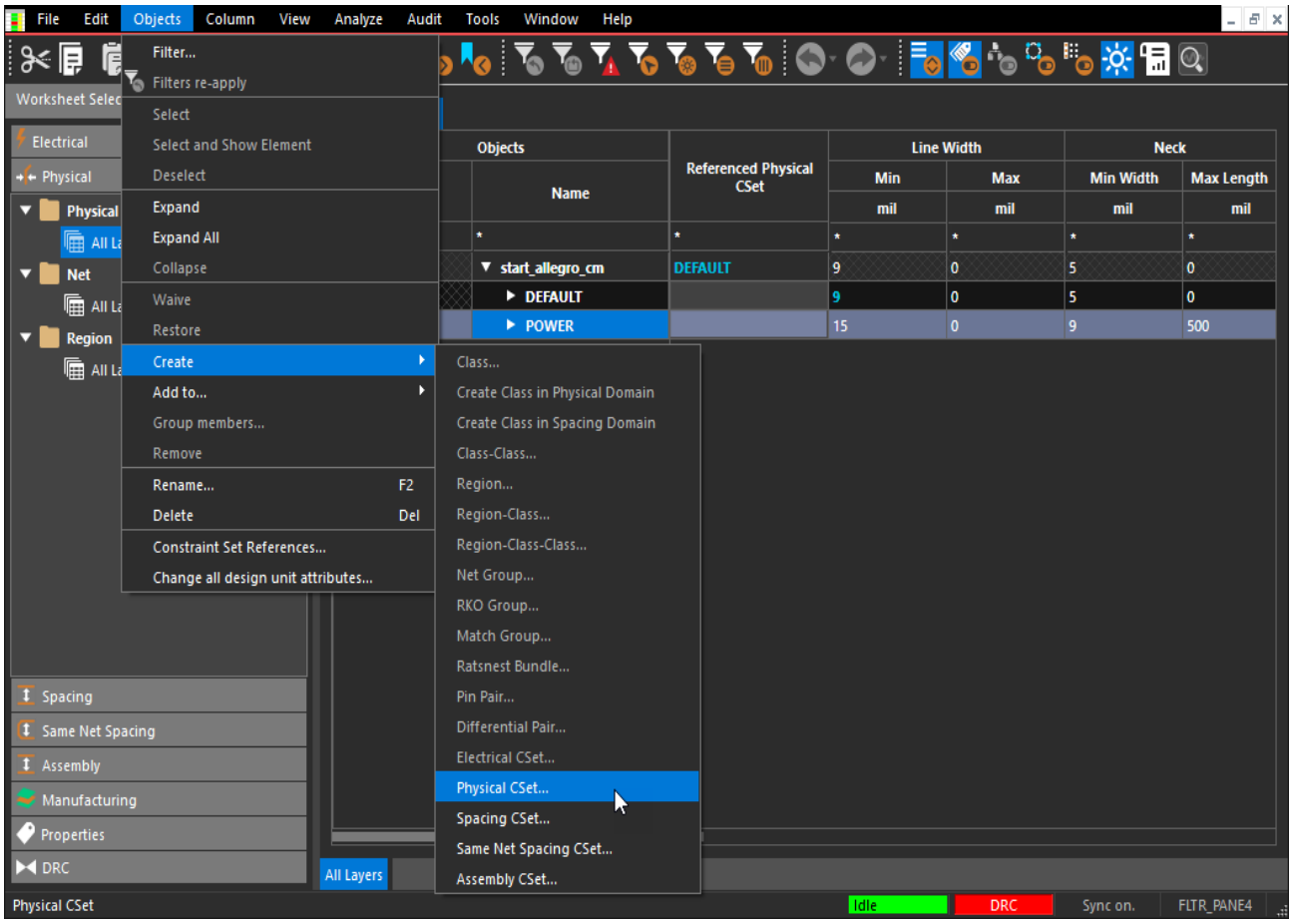
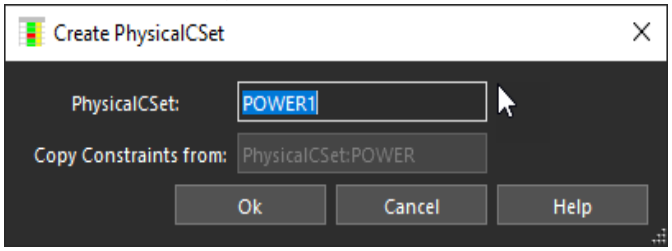
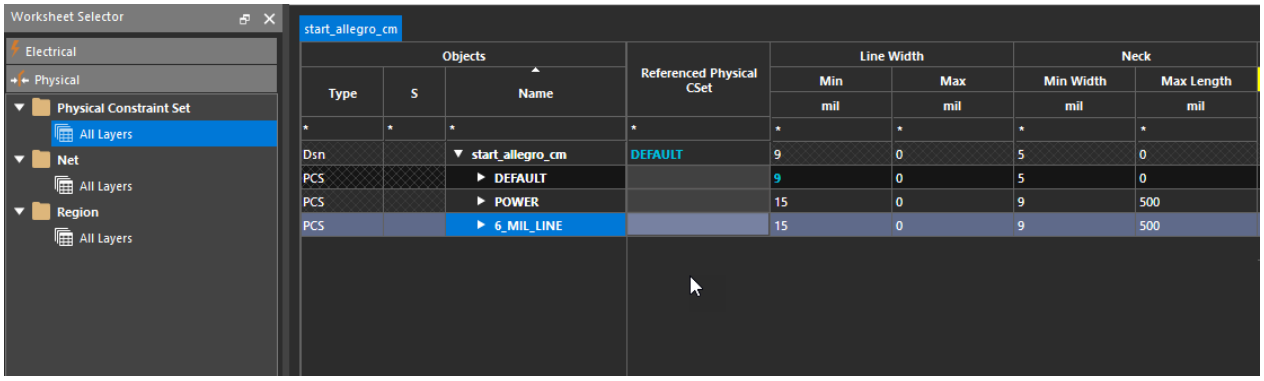


The *Create PhysicalCSet* dialog box appears



4. Enter the Physical CSet name as `6_MIL_LINE` in the *PhysicalCSet* field.
5. Click *Ok*.

   The instance of the new CSet is displayed in the *Objects* column below POWER CSet.

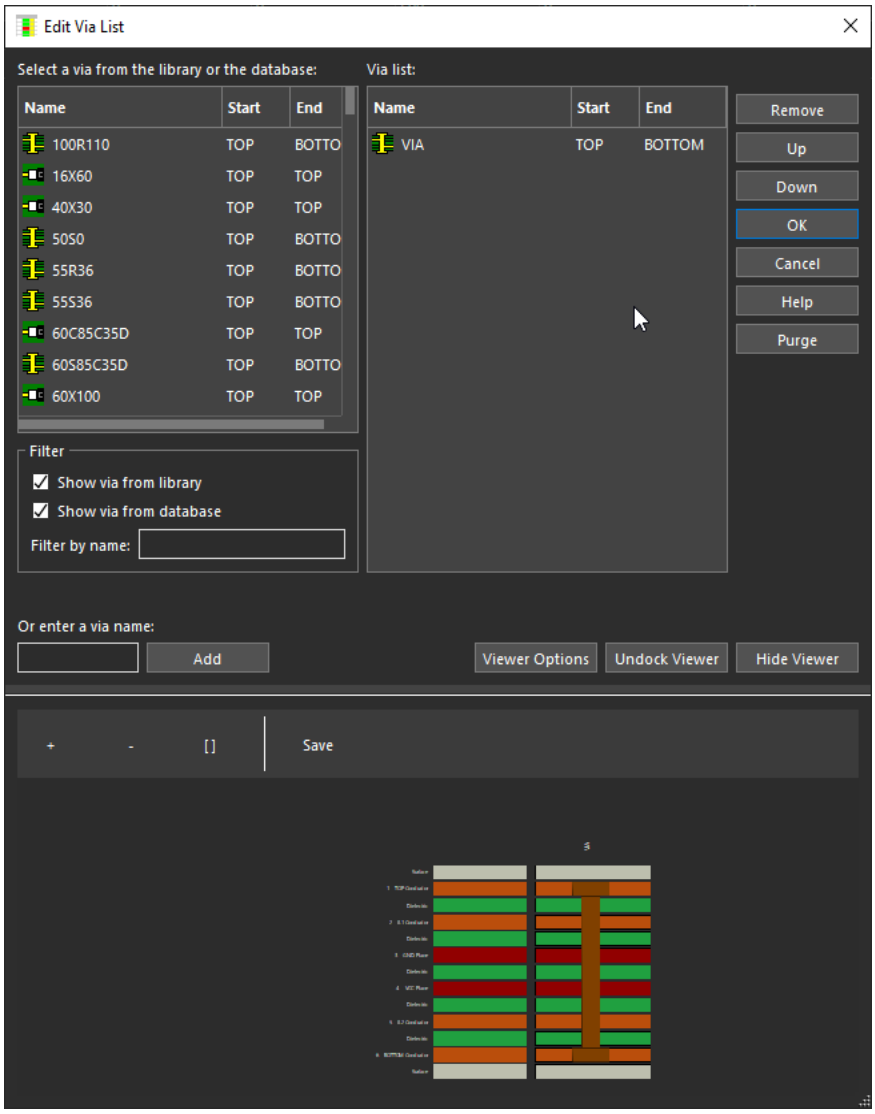


6. Select the *Min Line Width* value and double-click to change it to 6.

Note: You can use `Tab` key to navigate along the spreadsheet.

7. Select *Min Neck Width* value and double-click to change it to 3.
8. Select *Max Neck Length* value and double-click to change it to 200.
9. Double-click the *Via* constraint to open *Edit Via List* window.

10. Select the via you added to the POWER CSet from the *Via list* and click *Remove*.



11. Click *OK*.

12. Close Constraint Manager.

Creating Constraint Set for Region

Constraint regions are the areas meant for special routing in the design and can have different physical constraints rules.

Task Overview

You will create Region Physical CSet from the existing CSet and assign constraints to it.

Steps

1. Open Constraint Manager and select Physical domain.
2. Select *All Layers* worksheet under *Physical Constraint Set* workbook.
3. Right-click the POWER cell and choose *Create – Physical CSet* from the pop-up menu.

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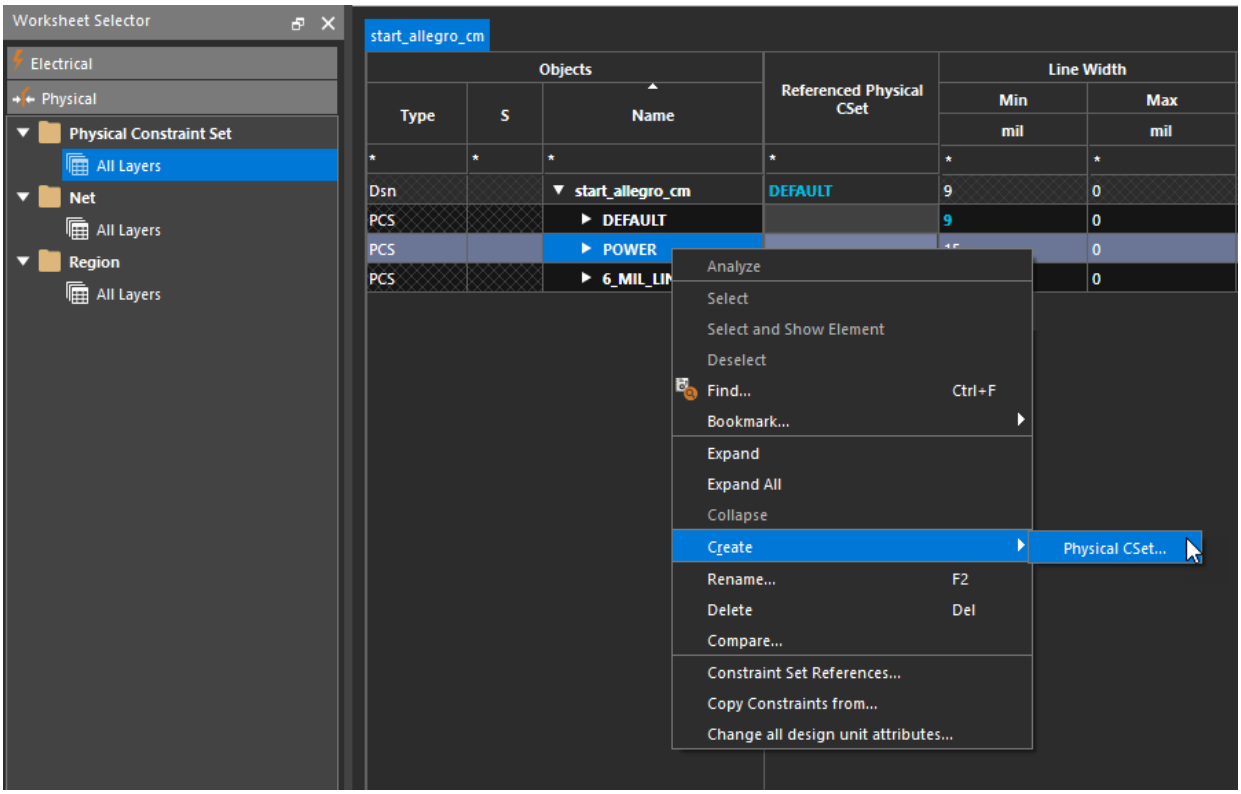
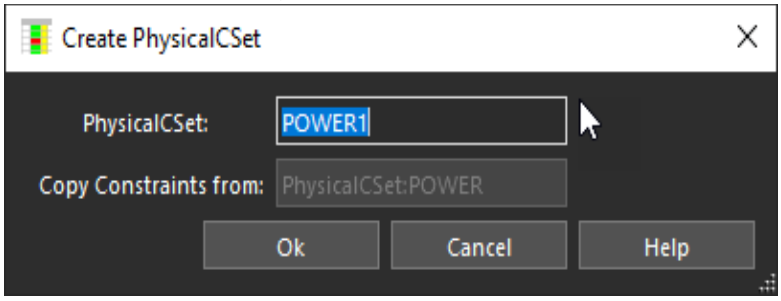
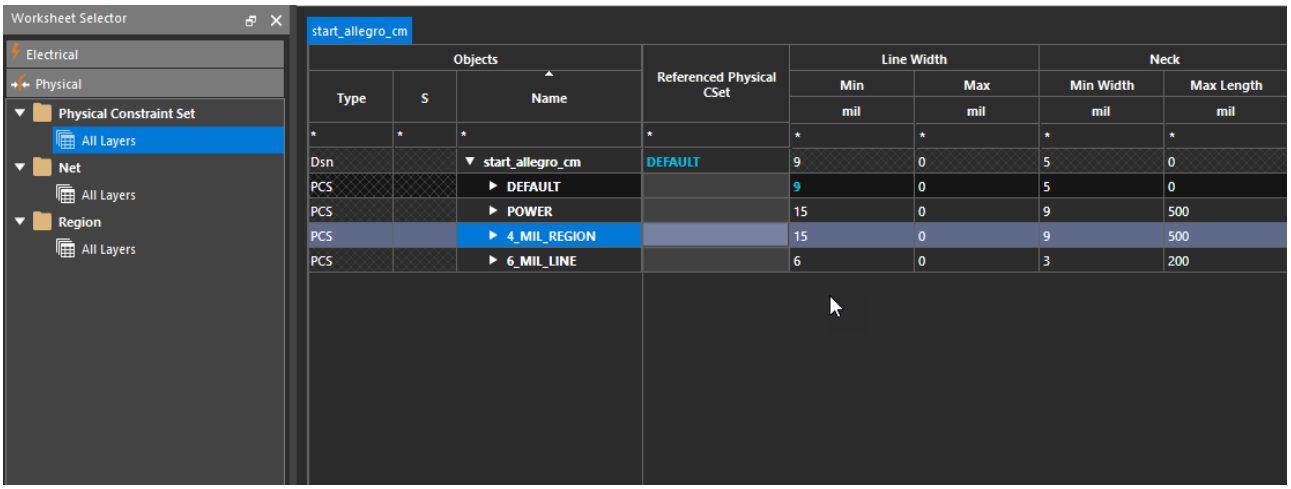


The *Create PhysicalCSet* dialog box appears



4. Enter the Physical CSet name as `4_MIL_REGION` in the *PhysicalCSet* field.
5. Click OK.

   The instance of the new CSet is displayed in the *Objects* column below POWER CSet.



Note: You can see the constraints are copied from the POWER physical CSet.

6. Select the *Min Line Width* value and double-click to change it to 4.
7. Select *Min Neck Width* value and double-click to change it to 4.
8. Select *Max Neck Length* value and double-click to change it to 0.
9. Click the *Via* constraint to open *Edit Via List* window.
10. Select the via you added to the POWER CSet from the *Via list* and click *Remove*.
11. Click *OK*.
12. Close Constraint Manager.

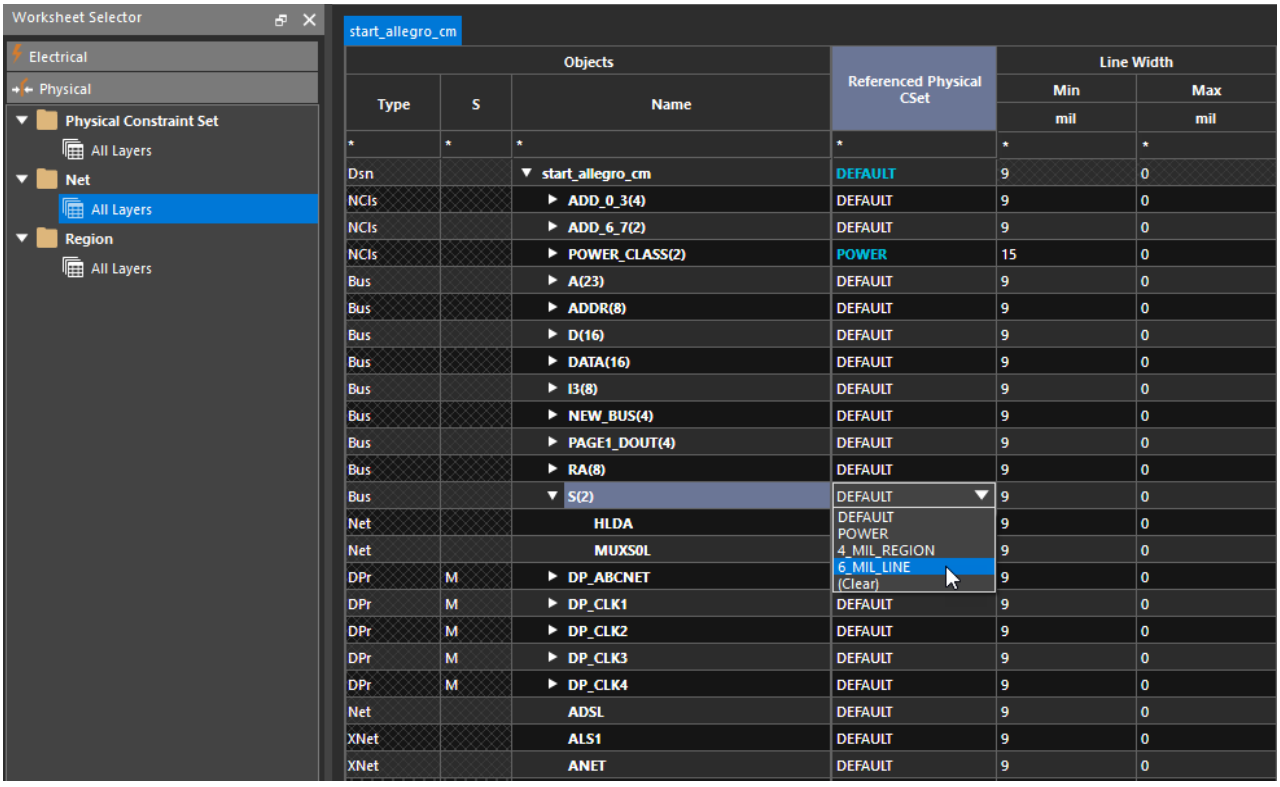
Assigning Physical Constraint Sets to Objects

Task Overview

You will now assign Physical CSet to the nets.

Steps

1. Open Constraint Manager and select *Physical* domain.
2. Select *All Layers* worksheet under *Net* workbook.
3. Expand the object *S*.
4. Select *6_MIL_LINE* from the drop-down list under the *Referenced Physical CSet* column for the object *S*.



The bus *S*, which contains two nets *HLDA* and *MUXS0L*, will use the *6_MIL_LINE* rule such that when either of these two nets are routed they will be using 6 mils line width.

Creating Net Class

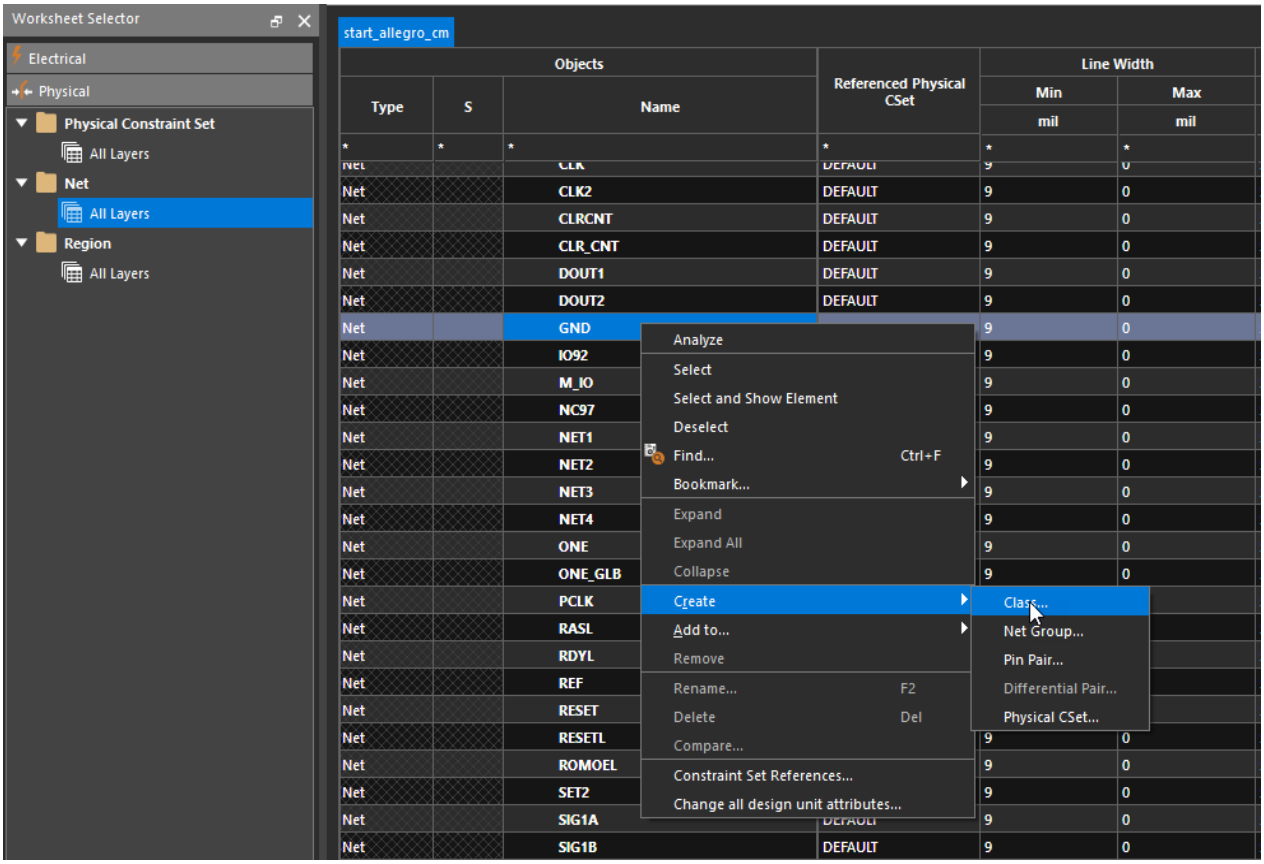
Net Class is used to group the nets with same physical requirement.

Task Overview

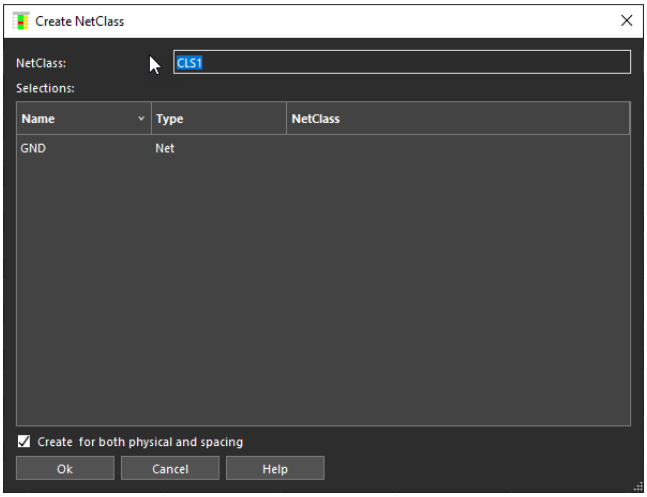
You will now create a Net Class.

Steps

1. Select the *All Layers* worksheet under the *Net* workbook in the *Physical* domain.
2. Right-click the net *GND* and choose *Create – Class* menu item.



The *Create NetClass* dialog box appears.



3. Enter a new Net Class name as `POWER_CLASS` in the *NetClass* field.

Note: You can create this new class in both the physical and the spacing section.

4. Click *Ok*.

   The net GND is now placed under the *POWER_CLASS* net class.

Assigning Nets to Net Class

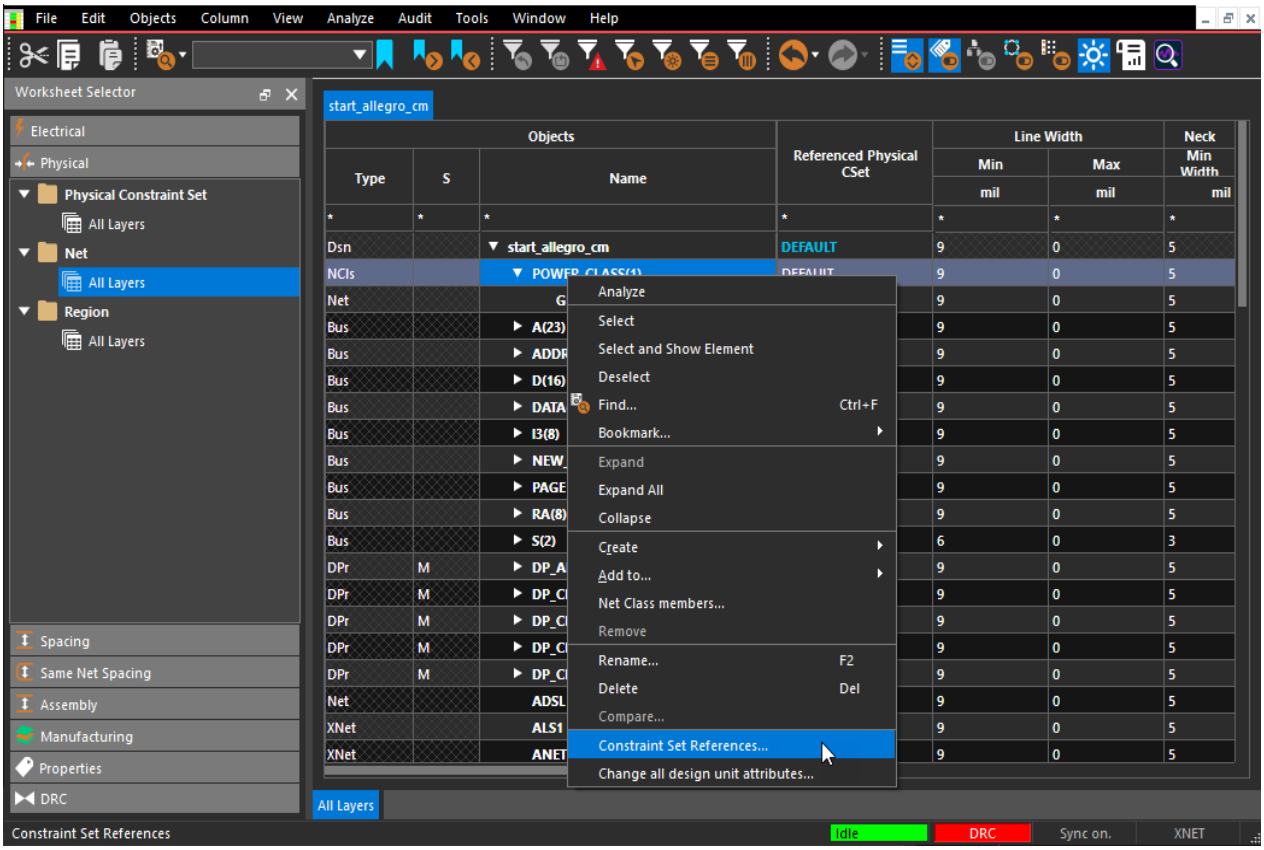
Task Overview

You will now assign Net to a Net Class.

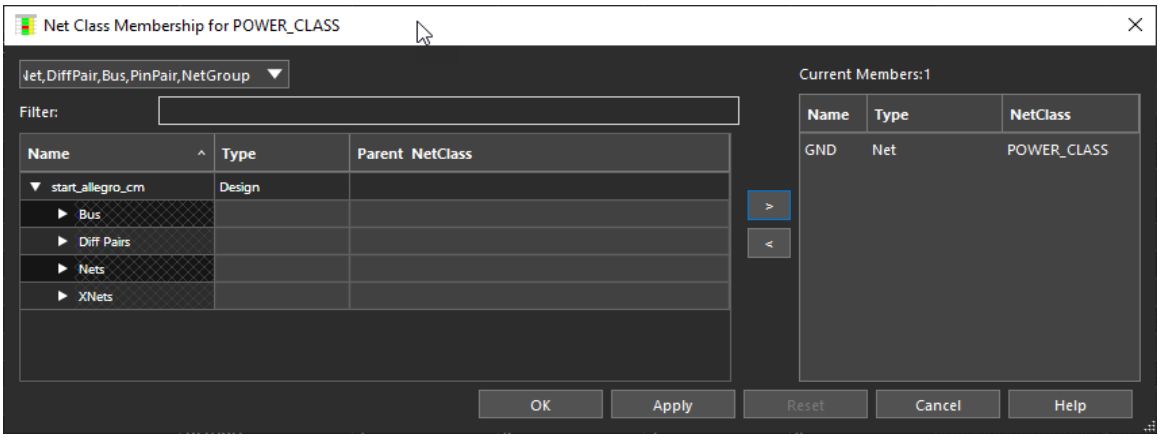
Steps

1. Select the *All Layers* worksheet under the *Net* workbook in the *Physical* domain.

2. Right-click the Net Class *POWER_CLASS* and select *Net Class members from the pop-up* menu.



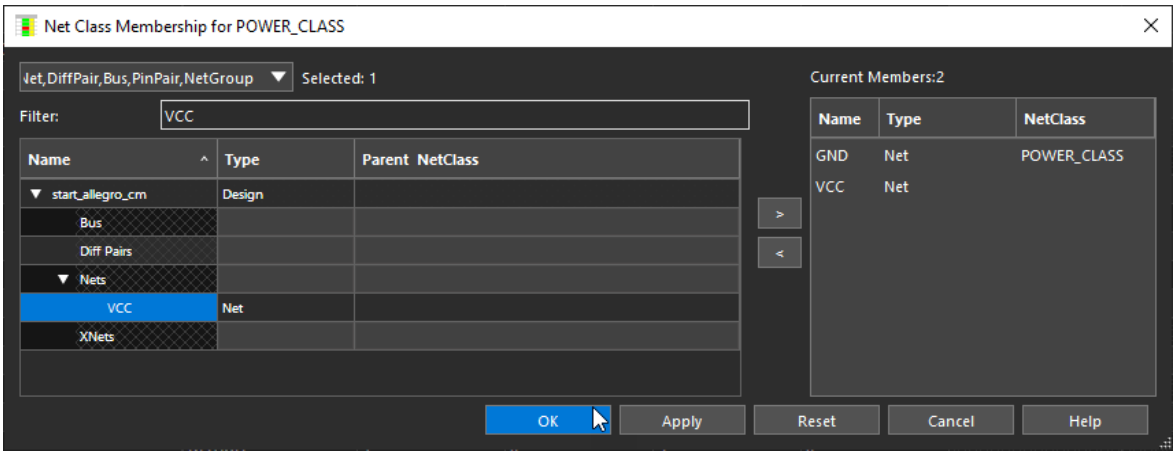
The *NetClassMembership* dialog box appears.



3. Type VCC in the *Filters* field.

4. Double-click *VCC* under *Nets* in the *Name* column.

   The net *VCC* is added to the *Current Members* list.



5. Click *OK*.

Assigning CSet to Net Class

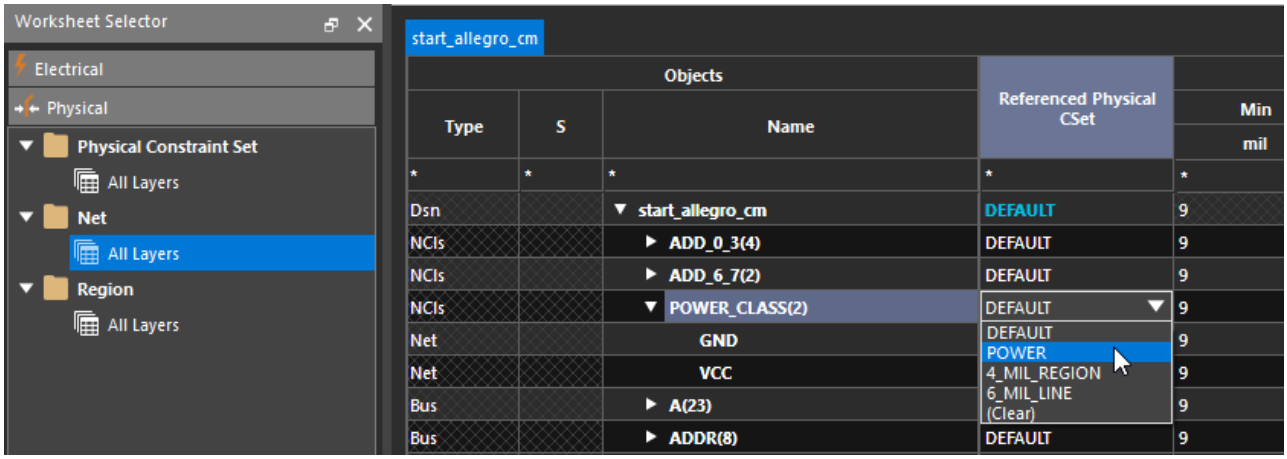
Task Overview

You will now assign CSet to a Net Class.

Steps

1. Select the *All Layers* worksheet under the *Net* workbook in the *Physical* domain.

2. Select *POWER* from the drop-down list under the *Referenced Physical CSet* column for the object *POWER_CLASS*.



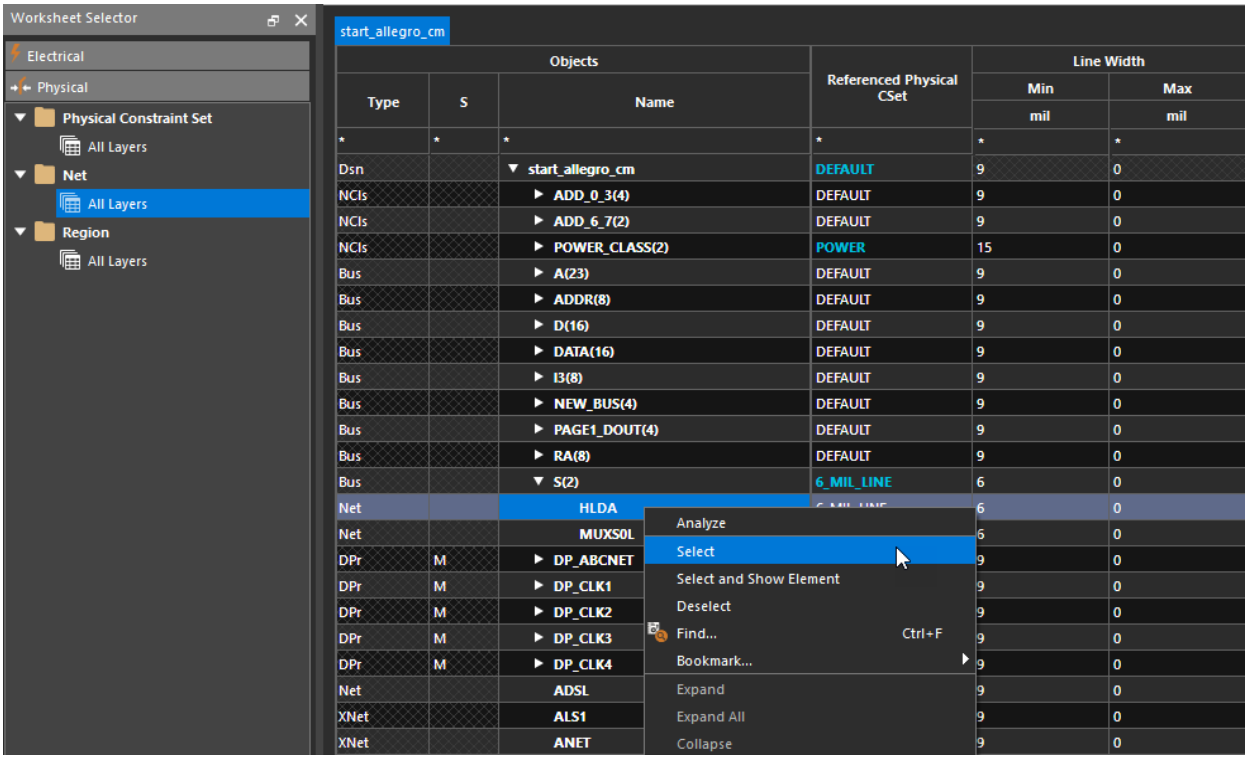
The Net Class, which contains two nets *GND* and *VCC*, will use the *POWER* rule such that when either of these two nets are routed all etch will be routed using constraints defined in POWER Physical CSet. (15mils width).

3. Close Constraint Manager.

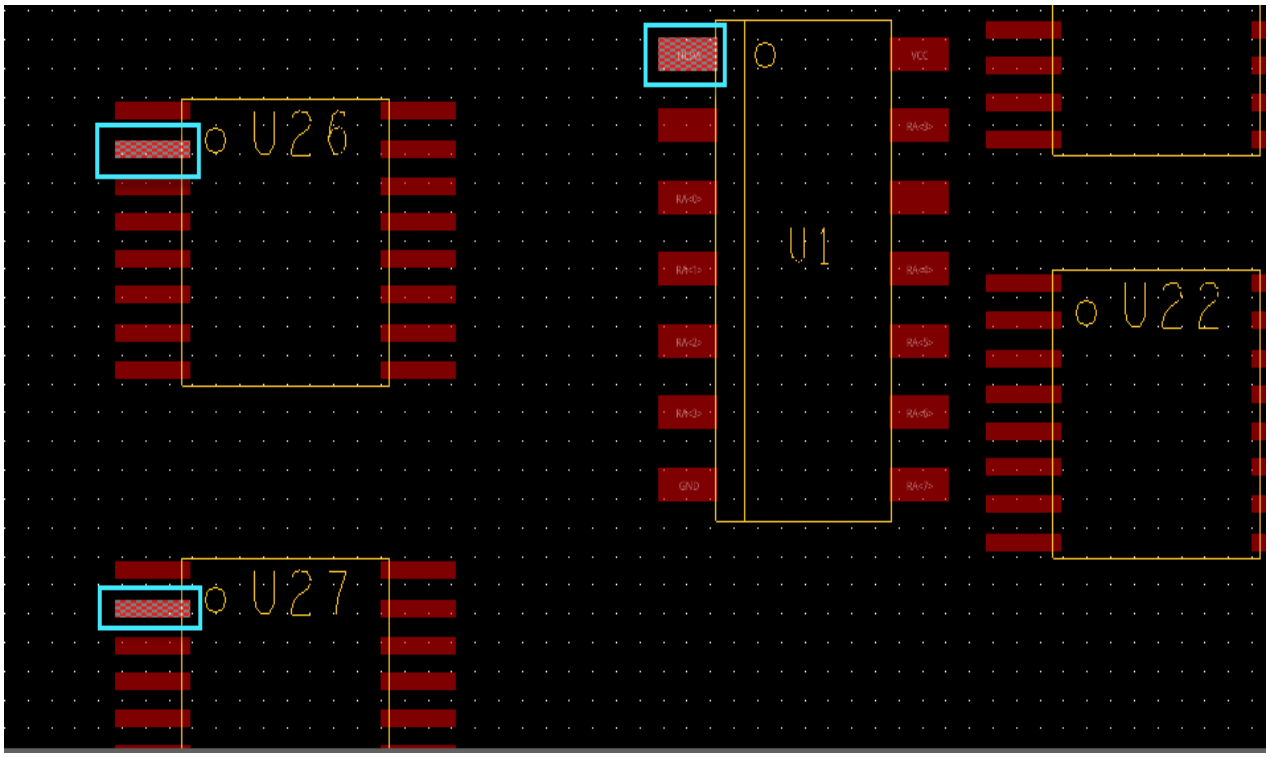
Routing with Physical Constraints

Routing with 6_MIL_LINE Constraint

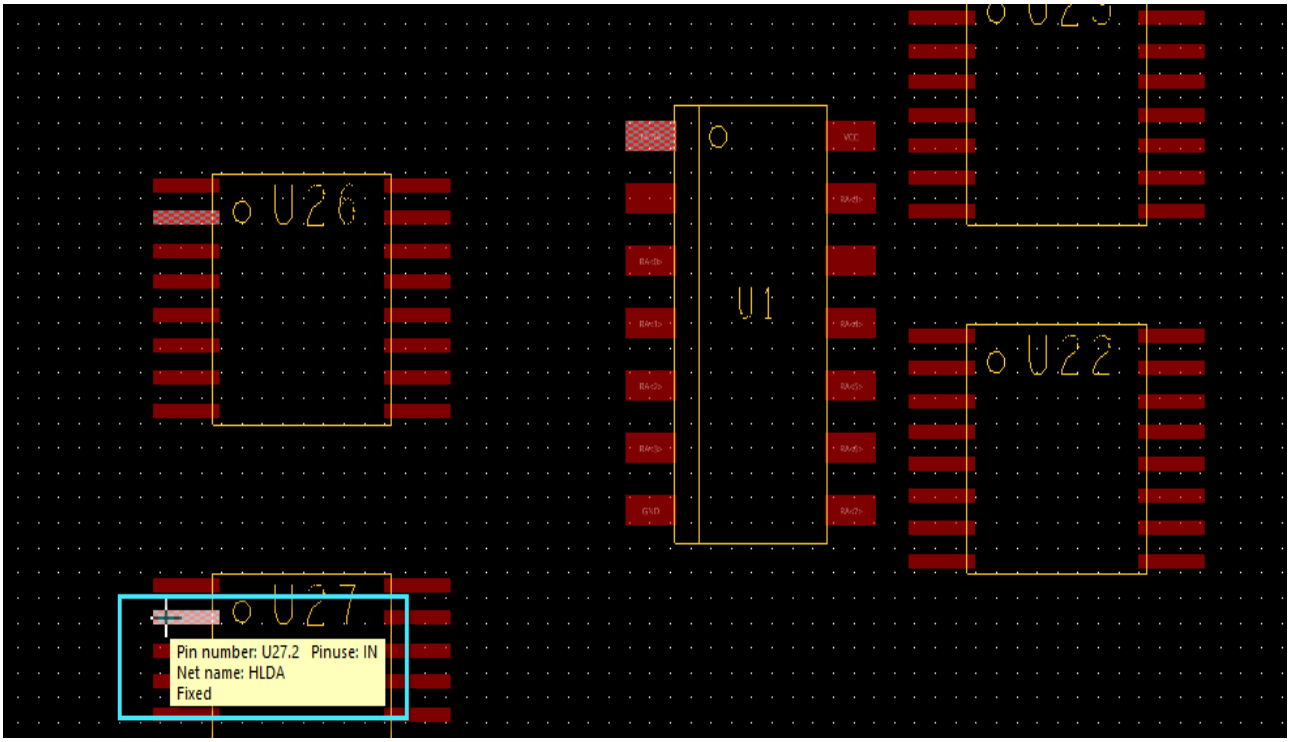
1. Select the *All Layers* worksheet under the *Net* workbook in the *Physical* domain.
2. Right-click the net *HLDA* under the bus *S* and choose *Select* from the pop-up menu.



Allegro PCB Editor highlights the net on the components U26, U27 and U1 on the board.



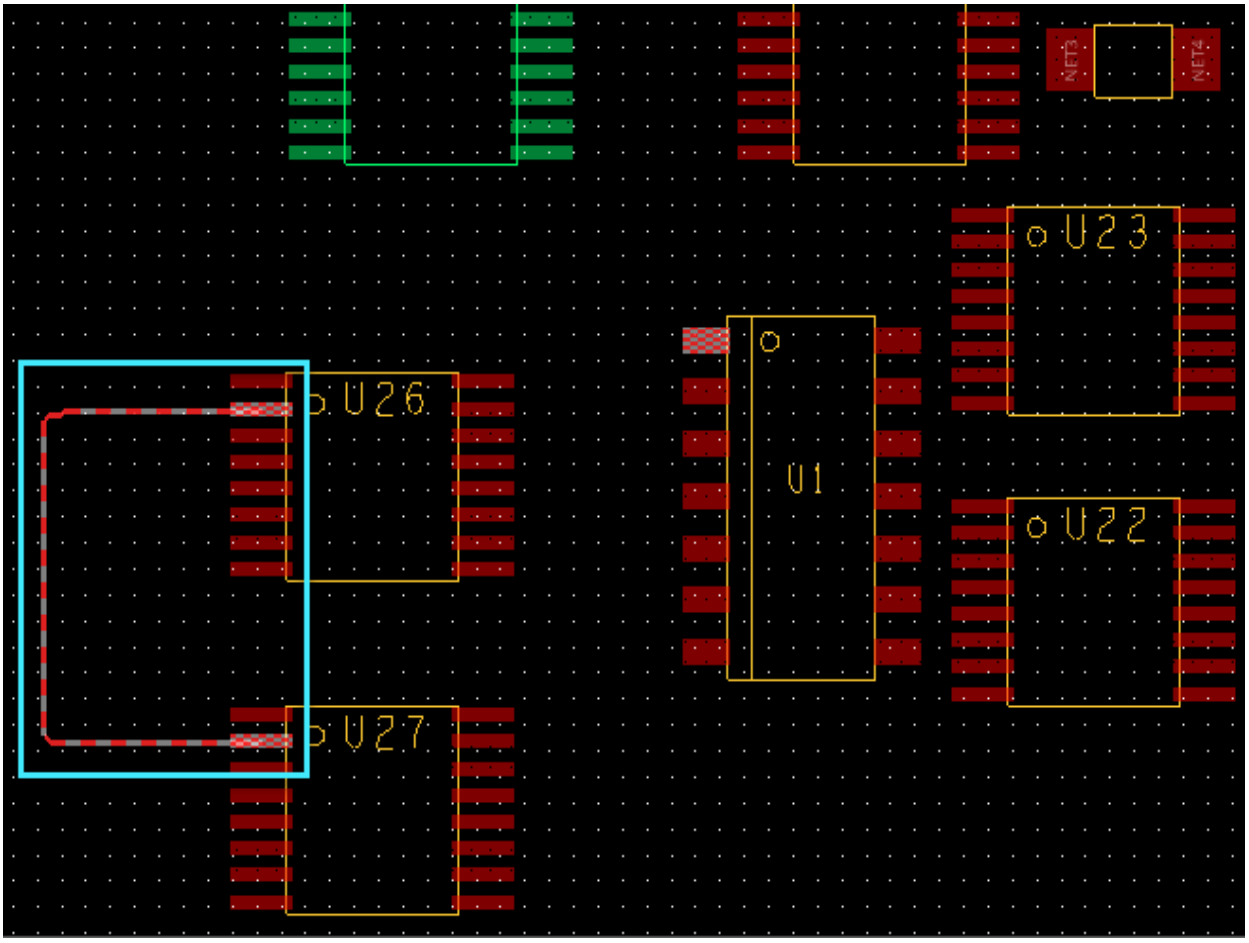
3. Hover your cursor over the highlighted pin on U27 from which you start adding etch/conductor. A data tip identifies its name.



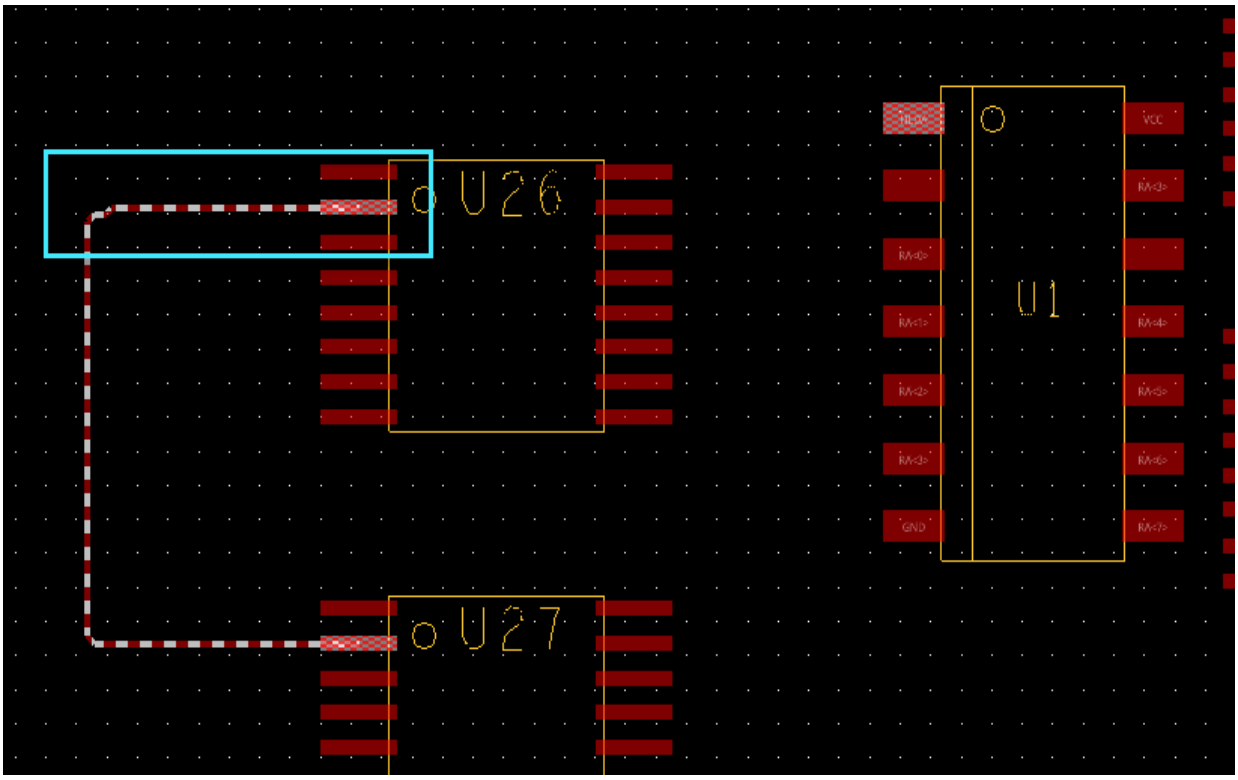
4. Choose *Route – Connect* in PCB Editor.
5. Select the pin with net HLDA on U27.

   A line is attached to the cursor.

6. Move the cursor and use single-click to create the route, and double-click to add vias as shown in the following figure.



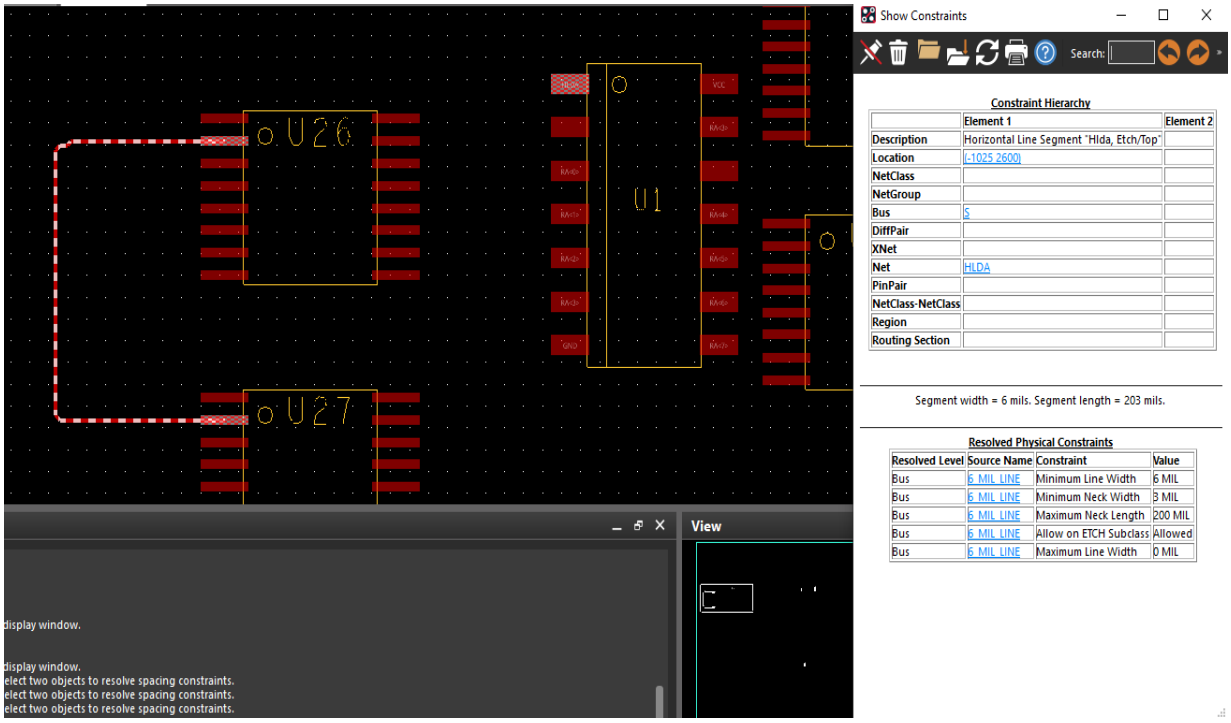
7. Move the cursor to end the route on the pin with net HLDA on U26.



8. Right-click and choose *Done* to terminate the routing.
9. Choose *Display - Constraint* or from tool bar icon click  .
10. Select the route.

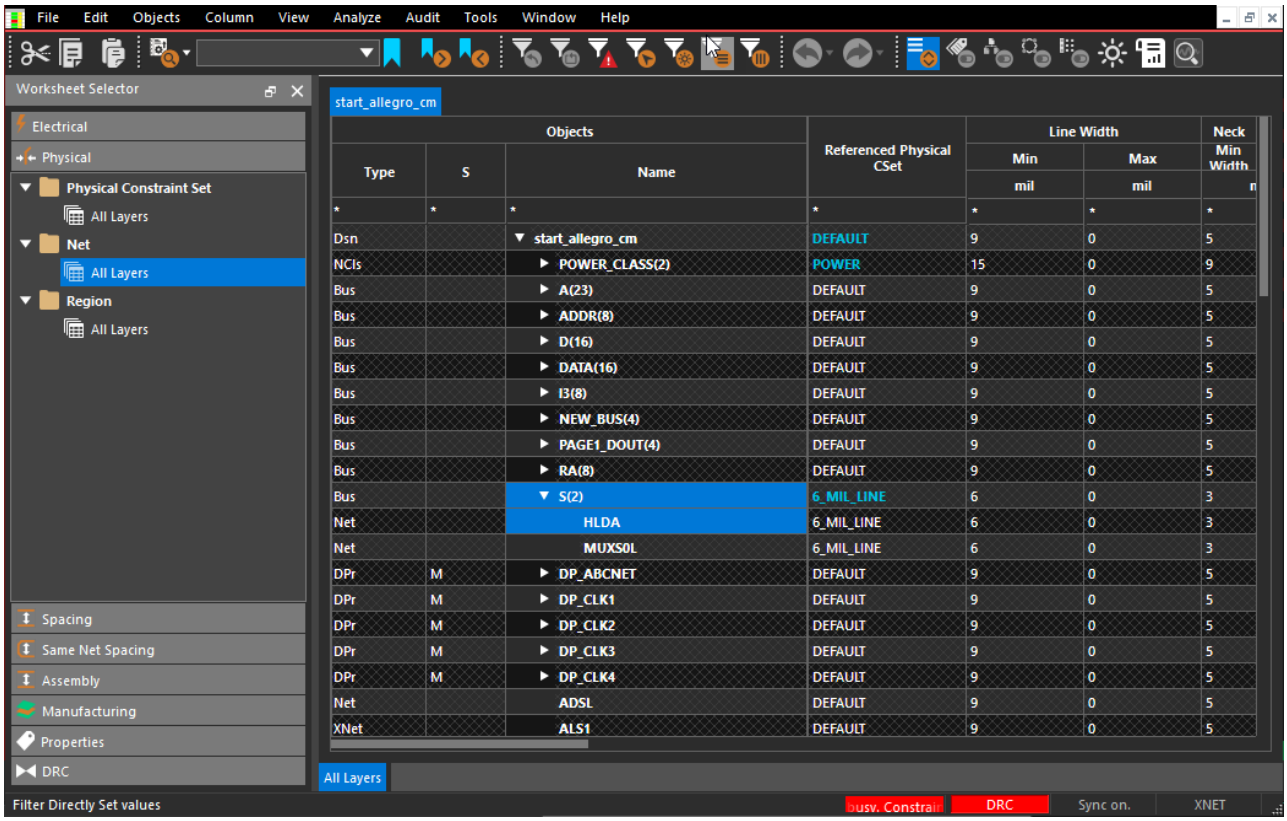
    Show Constraints window is displayed.

The *Constraint Hierarchy* table displays that the net *HLDA* is an element of bus *S*. The *Resolved Physical Constraints* table displays the constraint rules followed by the net *HLDA*.



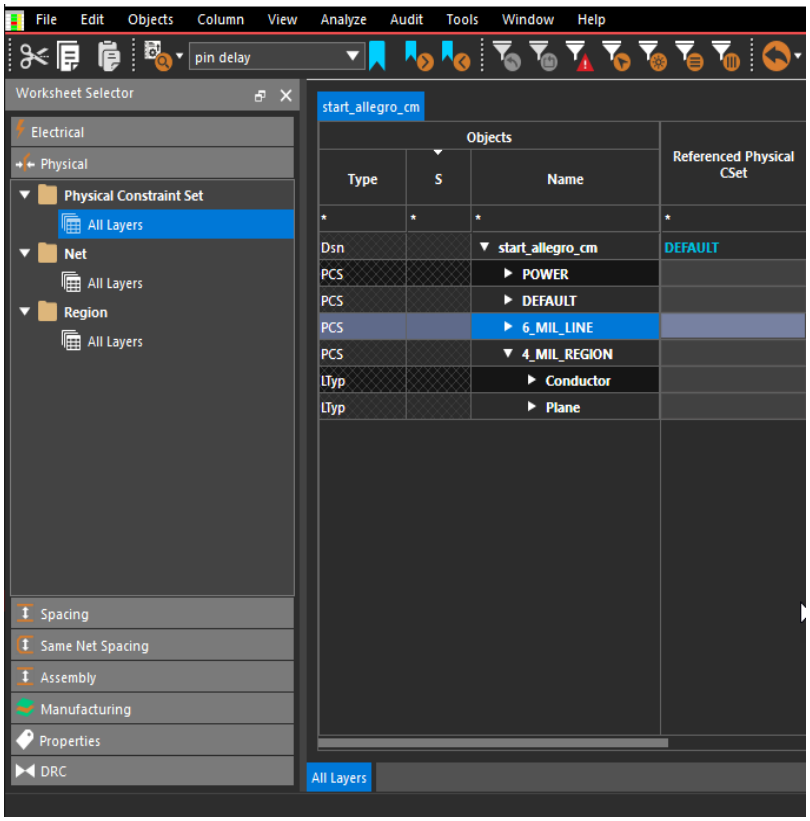
11. Click the bus *S* in the *Show Constraint* window to cross-probe between board and Constraint Manager.

The tool highlights the same in Constraint Manager.



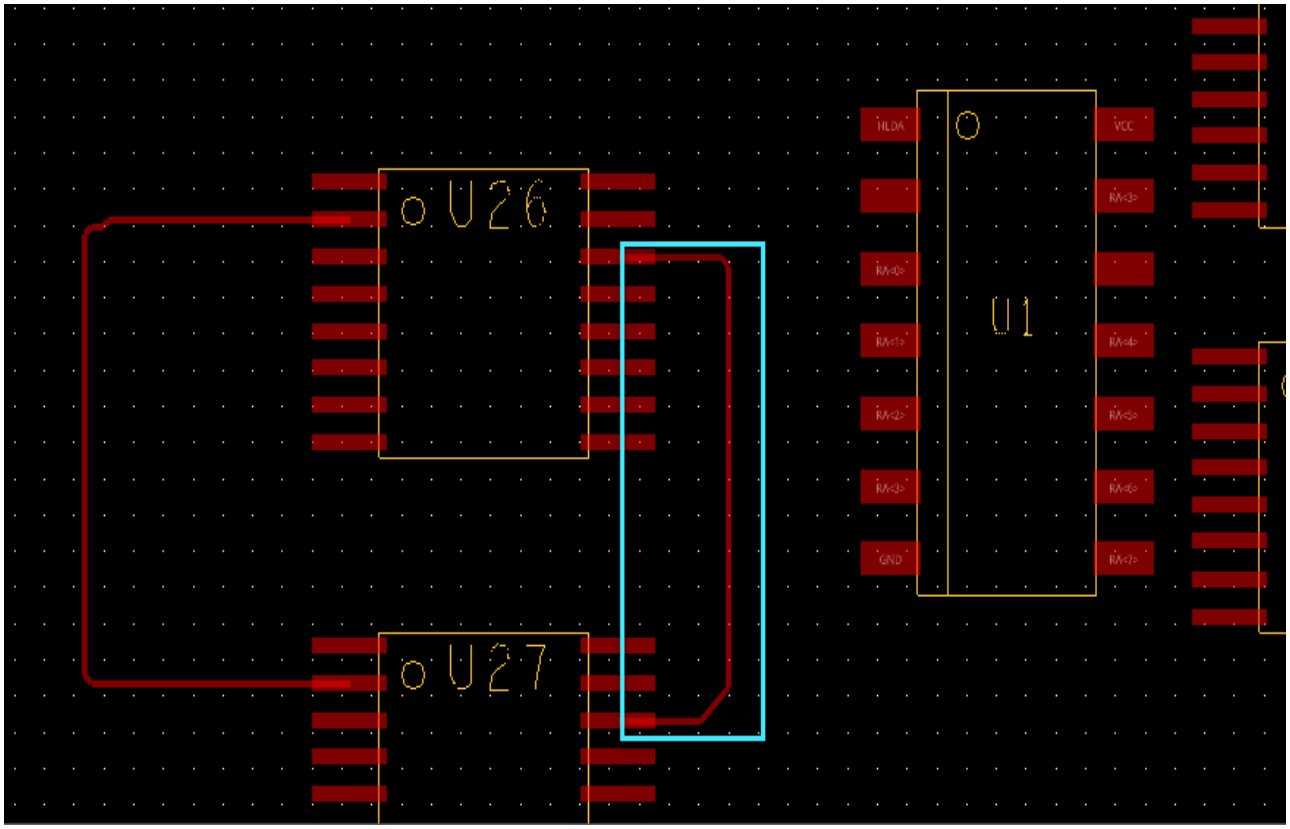
12. Click *6_MIL_LINE* constraint under Source Name column in the Show Constraints window.

The tool highlights the Physical CSet in Constraint Manager.



13. Choose *Route – Connect* in PCB Editor.

14. Select the pin with net *MUXS0L* on U26 and move the cursor to end the route at the pin with net *MUXS0L* on U27.



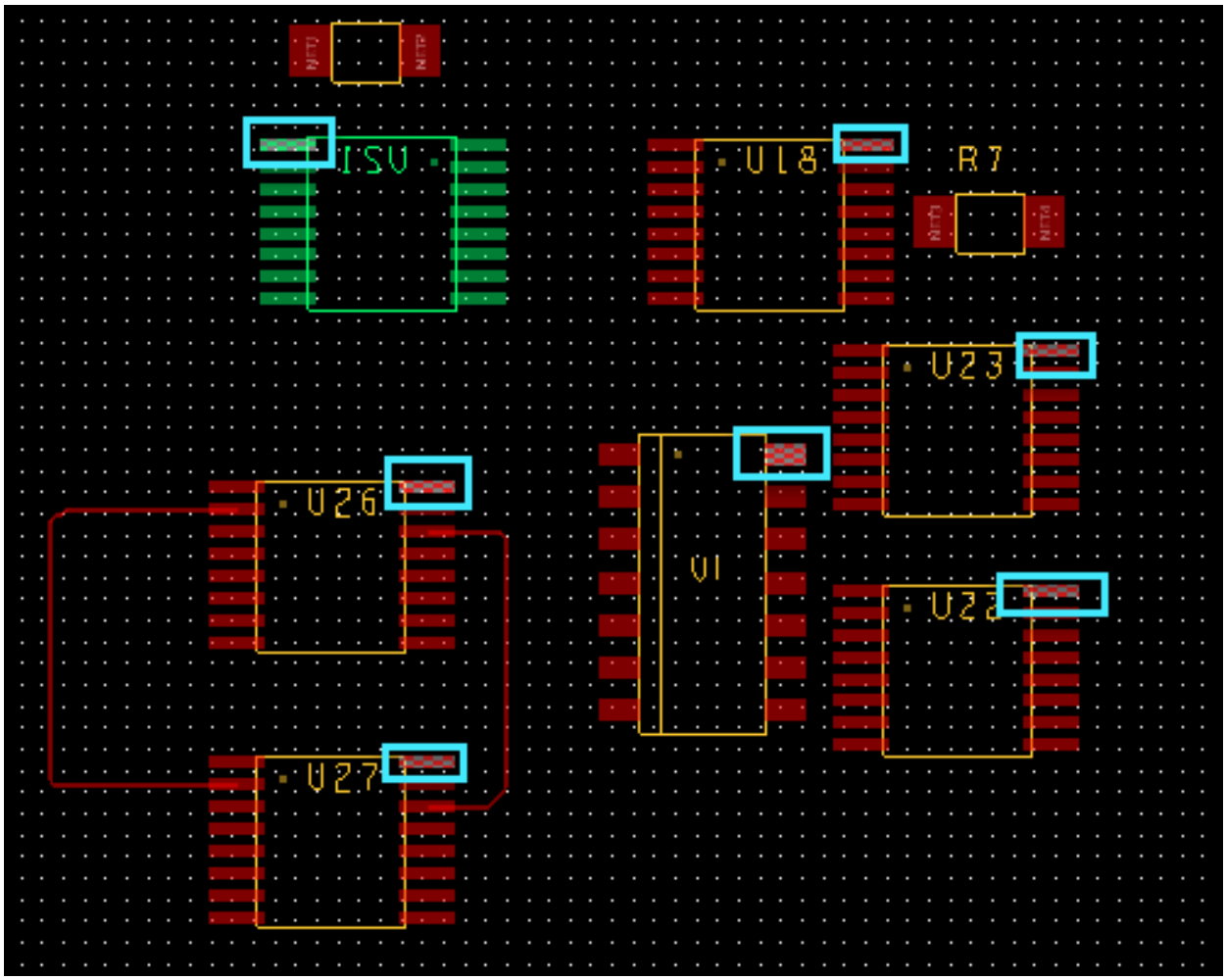
15. Right-click and choose *Done* to terminate the routing.

Routing Net Class

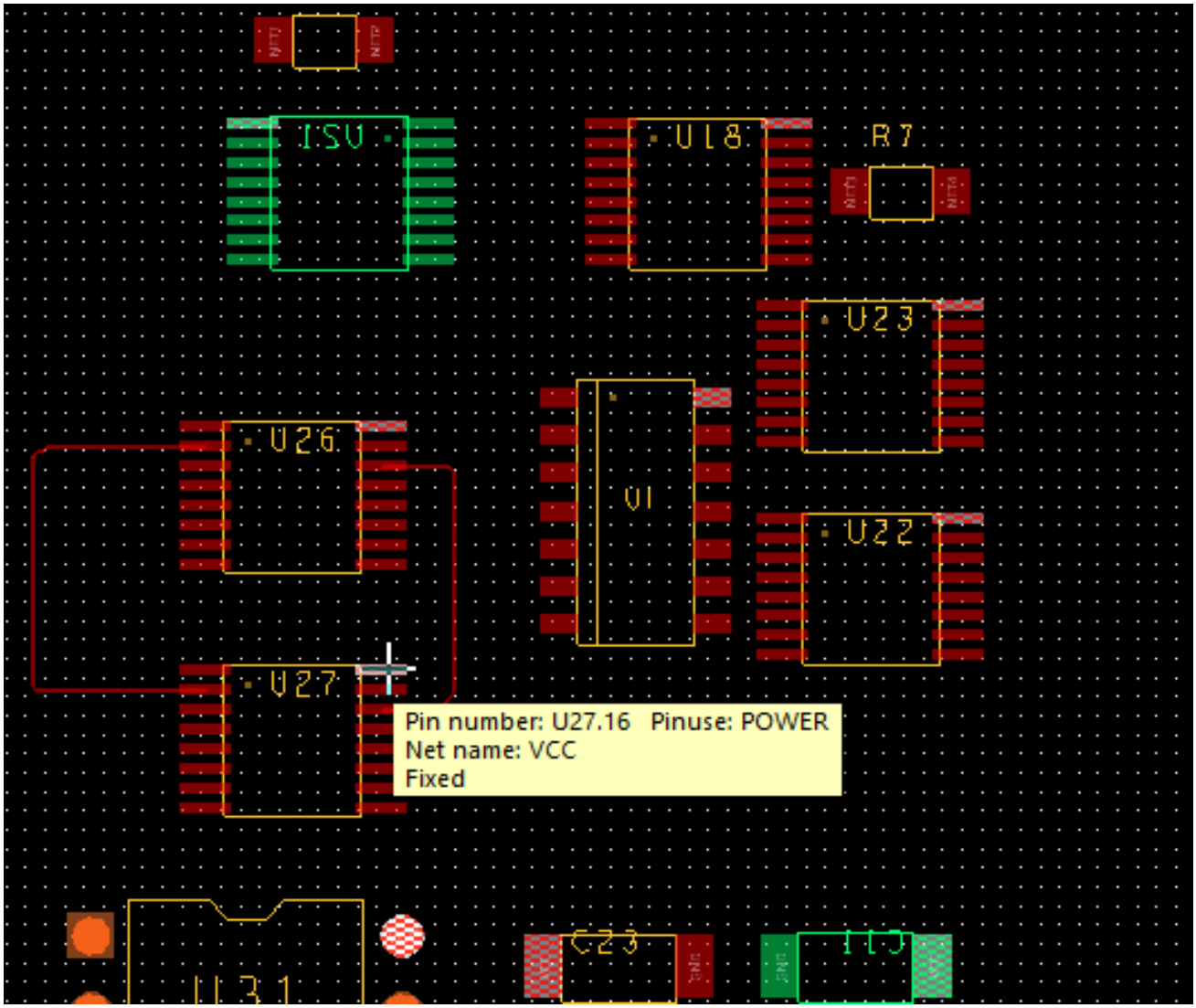
1. In Constraint Manager, select the *All Layers* worksheet under the *Net* workbook in the *Physical* domain.

2. Right-click the net *VCC* under the Net Class *POWER_CLASS* and choose *Select* from the pop-up menu.

Allegro PCB Editor highlights the net VCC on all the components on the board.



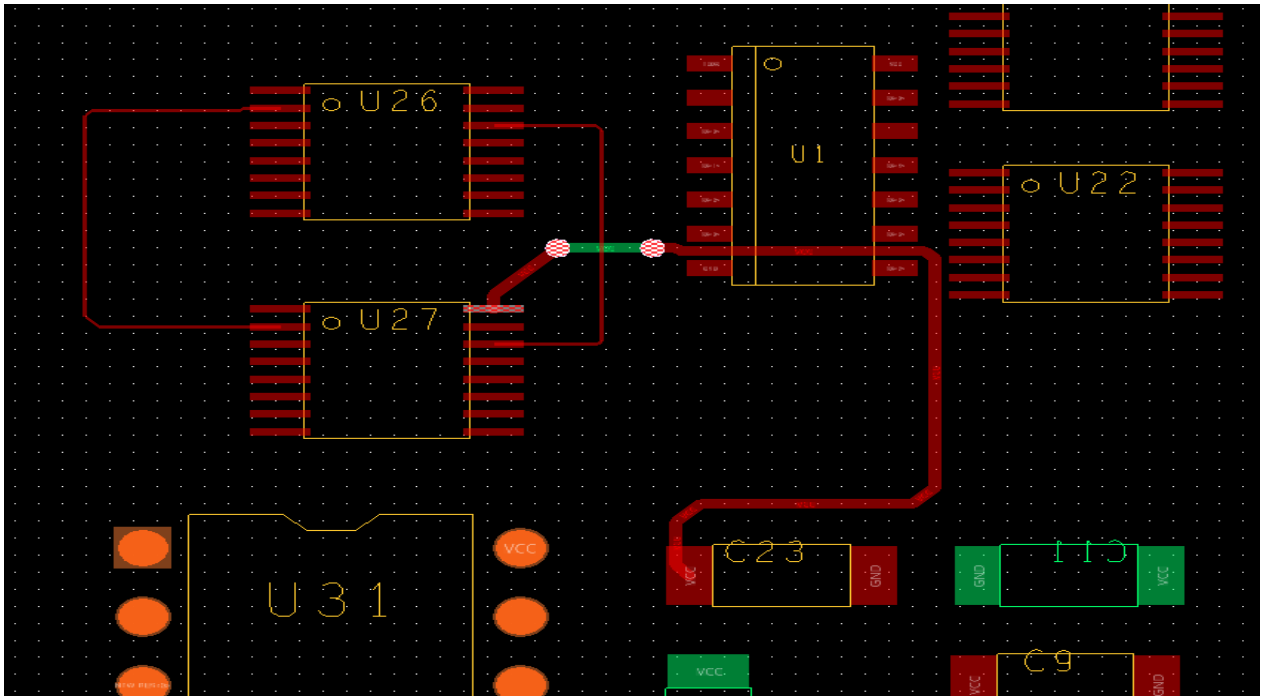
3. Hover your cursor over the pin with net VCC on U27 from which you start adding etch/conductor. Data tip identifies its name.



4. Choose *Route – Connect*.
5. Select the pin with net VCC on U27.

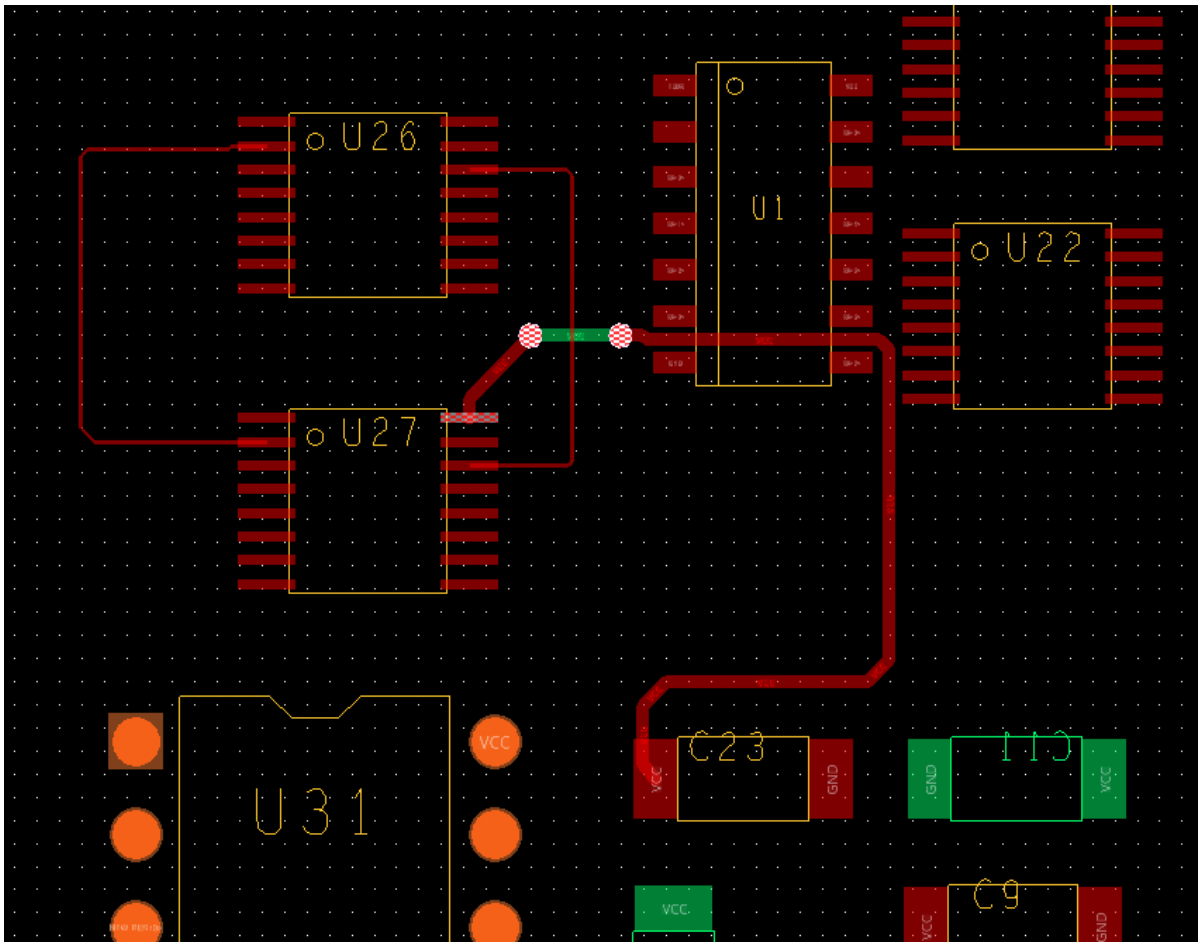
   A line is attached to the cursor.

6. Move the cursor and use single-click to create the route, and double-click to add vias as shown in the following figure.



7. Right-click and select *Neck Mode* from pop-up menu.
8. Route across U1 and deselect the *Neck Mode* from pop-up menu.

9. Terminate the route at the pin with net VCC of C23.

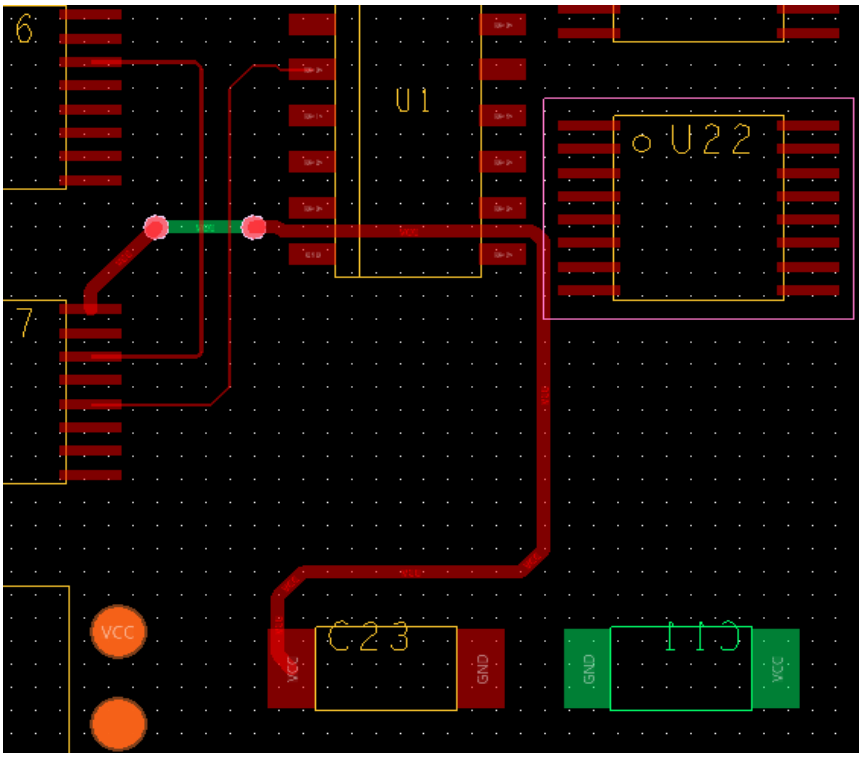


Routing in Constraint Region

Defining Constraint Region

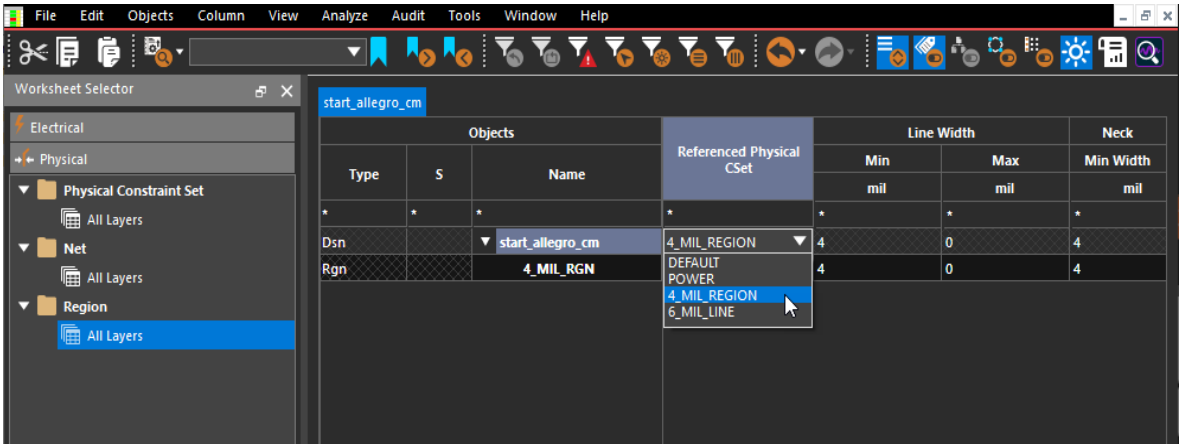
1. In Allegro PCB Editor, choose *Shape – Rectangular*.
2. Select *Constraint Region* from the *Active Class and Subclass* drop-down list in the *Options* panel.
3. Choose subclass as *All*.
4. Type the region name as `4_MIL_RGN` in the *Assign to region* field.
5. Draw the constraint region around U22.

6. Right-click and select *Done* to end the shape command.



Assign Region Constraint CSet to Region

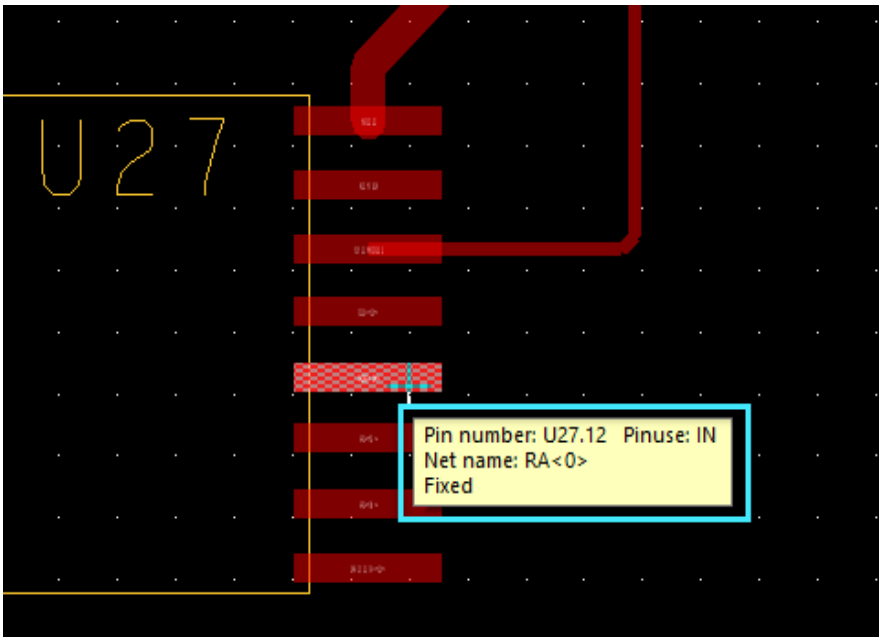
1. In Constraint Manager, select *All Layers* worksheet under *Region* workbook of *Physical* domain.
2. Choose the *Referenced Physical Set* column and select *4_MIL_REGION* from the drop-down menu as shown in the following image.



The region CSet *4_MIL_REGION* is assigned to the *4_MIL_RGN* region.

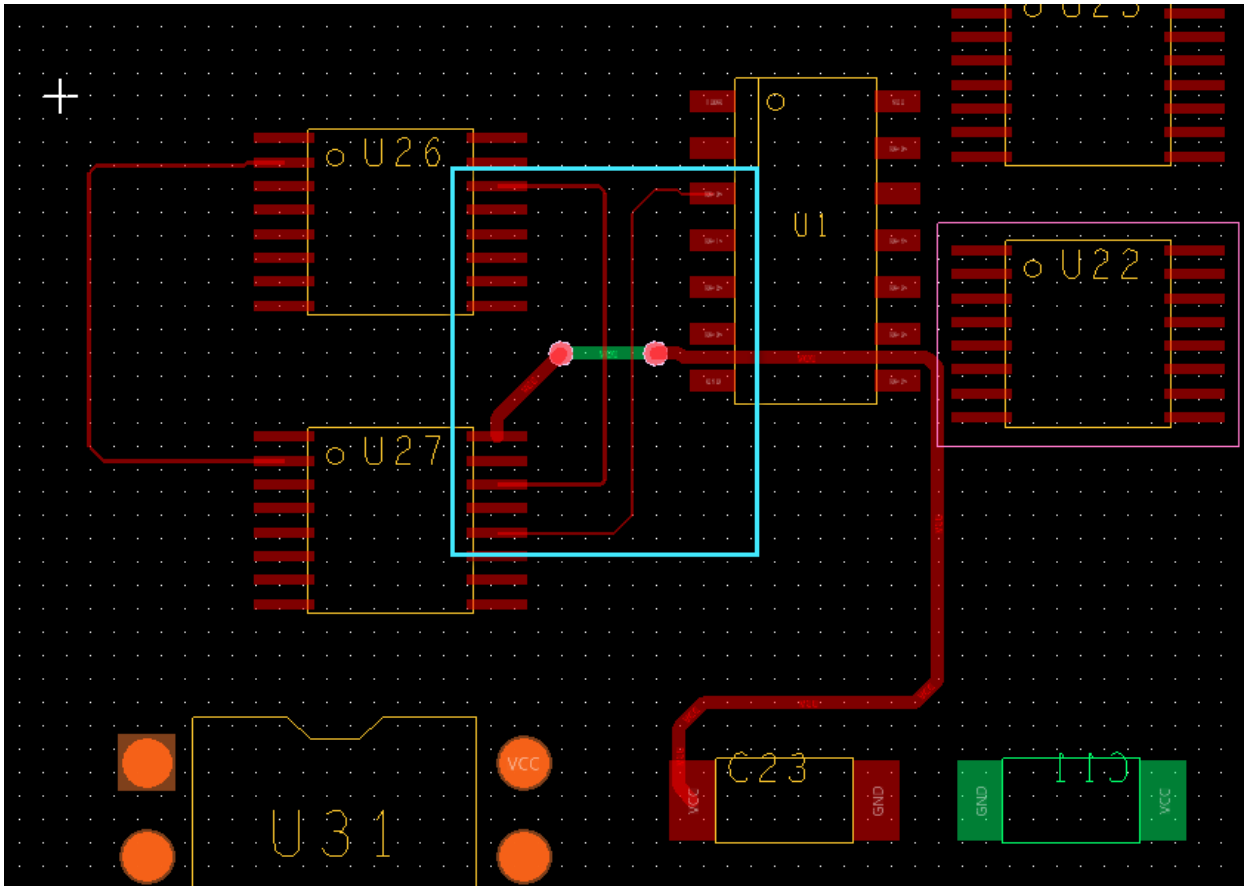
Routing in Constraint Region

1. In Allegro PCB Editor, choose pin with net *RA<0>* on U27 from which you start adding etch/conductor. Data tip identifies its name.



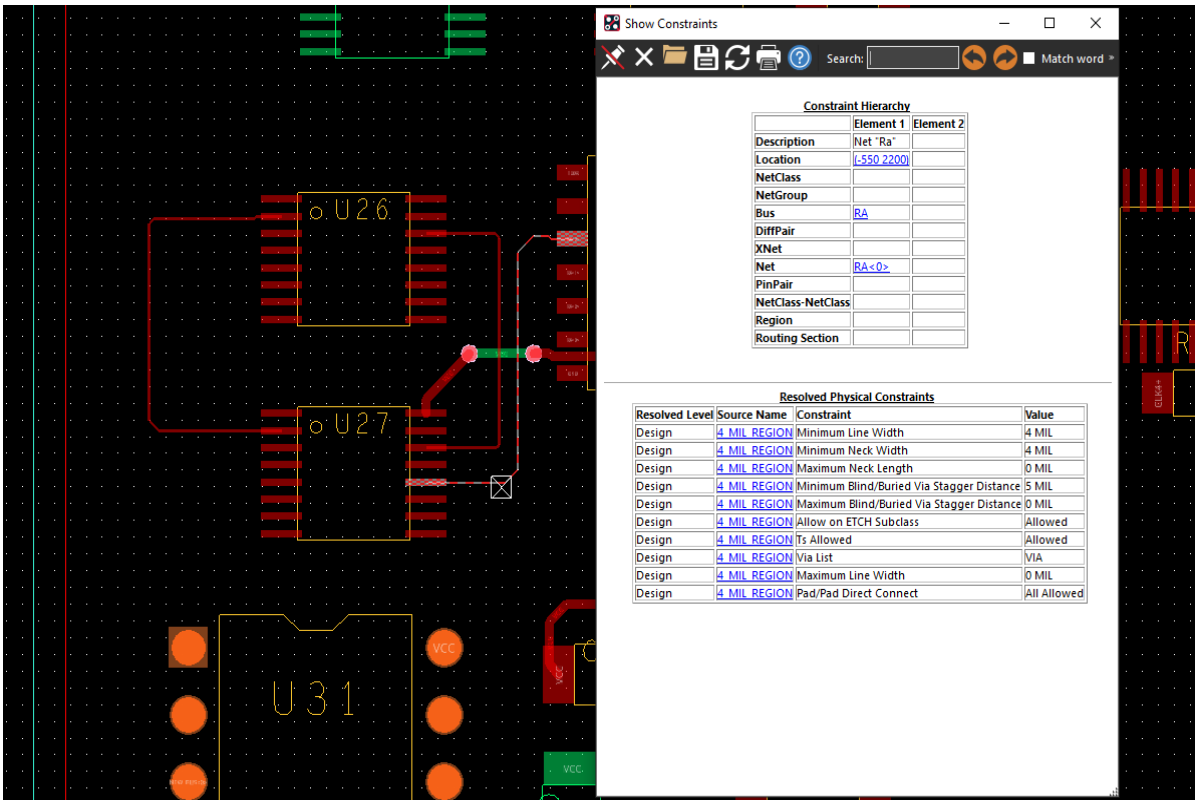
2. Choose *Route – Connect*.

3. Select the pin with net *RA<0>* on U27 and move the cursor to end the route at the pin with net *RA<0>* on U1.



4. Right-click and choose *Done* to terminate the route.
5. Select from menu *Display – Constraint* or from tool bar icon  .
6. Select the route.

Show Constraints window is displayed.



Summary

You learned to create physical constraint set for nets, net class and constraint region. You also learned to route with these physical constraints.

What's Next

In the next chapter, you will learn how to set Spacing Constraints, how to create and route with spacing constraints.

Recommended Reading

For more information about how physical constraints are handled in Allegro Constraint Manager, see the *Constraint Manager User Guide*.

2

Setting Spacing Constraints

Objectives

To learn how to set Spacing Constraints on nets in your layout using Constraint Manager and route them in Allegro PCB Editor.

At the end of the lesson, you will be able to

- Set up default Spacing Constraints
- Create Spacing Constraint set
- Set constraint set values for line-to-line spacing, line-to-thru-pin spacing, and via-to-thru-pin spacing.
- Create Net Class
- Create Net Class-Class
- Assign Spacing Constraint set to objects
- Route Spacing Constraints

Nature of Chapter

Skill (includes concepts and practice)

Setting Spacing Constraints

Spacing constraints are constraints that govern the spacing between objects on different nets. For example, the edge to edge distance between a connect line and a through pin.

Setting DEFAULT Spacing Constraint Set Values

The values of the DEFAULT Spacing CSet are predefined, but you can modify them to suit your design requirements. When you edit the values of a DEFAULT Spacing CSet, all of its objects automatically inherit the changes.

Note: You cannot delete or rename the DEFAULT Spacing CSet.

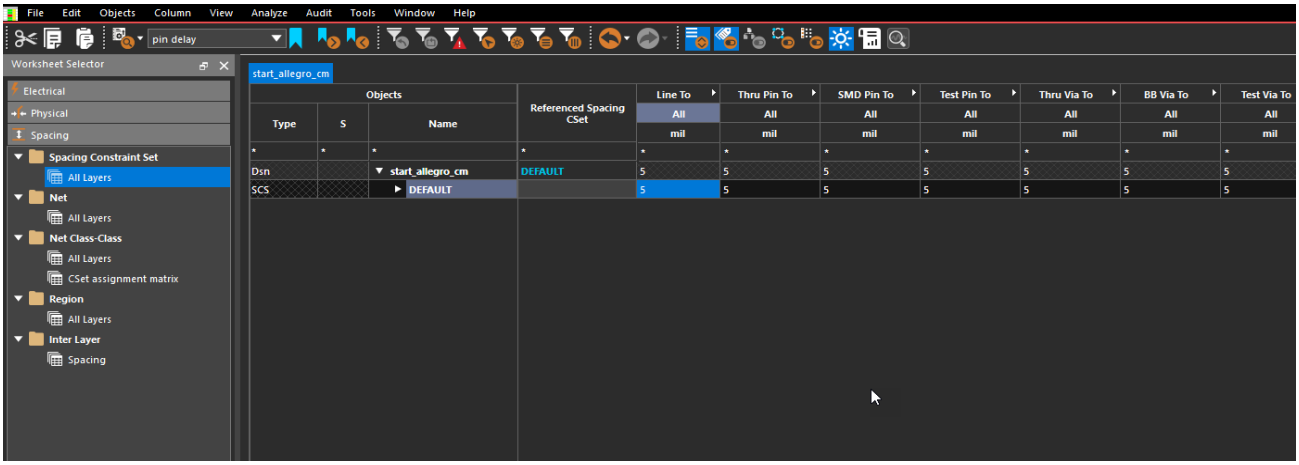
Task Overview

You will now modify the values of DEFAULT Spacing CSet for all the layers.

Steps

1. In the *Spacing Constraint Set* workbook under *Spacing* domain, click *All Layers.*
2. Double-click to expand the *Line To* column.

   The *Line To* constraints appears. Notice the *Line to Line, Line to Thru Pin, Line to SMD Pin* and other columns in this workbook.



Note: Double-click *DEFAULT* under *Name* column to see all the design layers that are listed under DEFAULT Spacing Constraint set.

3. Click the value in the *Line to Line* column for DEFAULT.

   The cell becomes editable. Since layers have different values the *Edit layer-specific values* window appears.

Tip

You can also right-click the cell and choose *Change* to edit the value.

4. Change the value from 5 to 6.

   If all the layers do not have the same value then layer specific window will open up.

5. Similarly, change the value for all the *Line to* columns from 5 to 6.
6. Close Constraint Manager and save the layout in Allegro PCB Editor.

Creating a new Spacing Constraint Set from DEFAULT CSet

You can create different rules for special nets which have values different from the DEFAULT CSet.

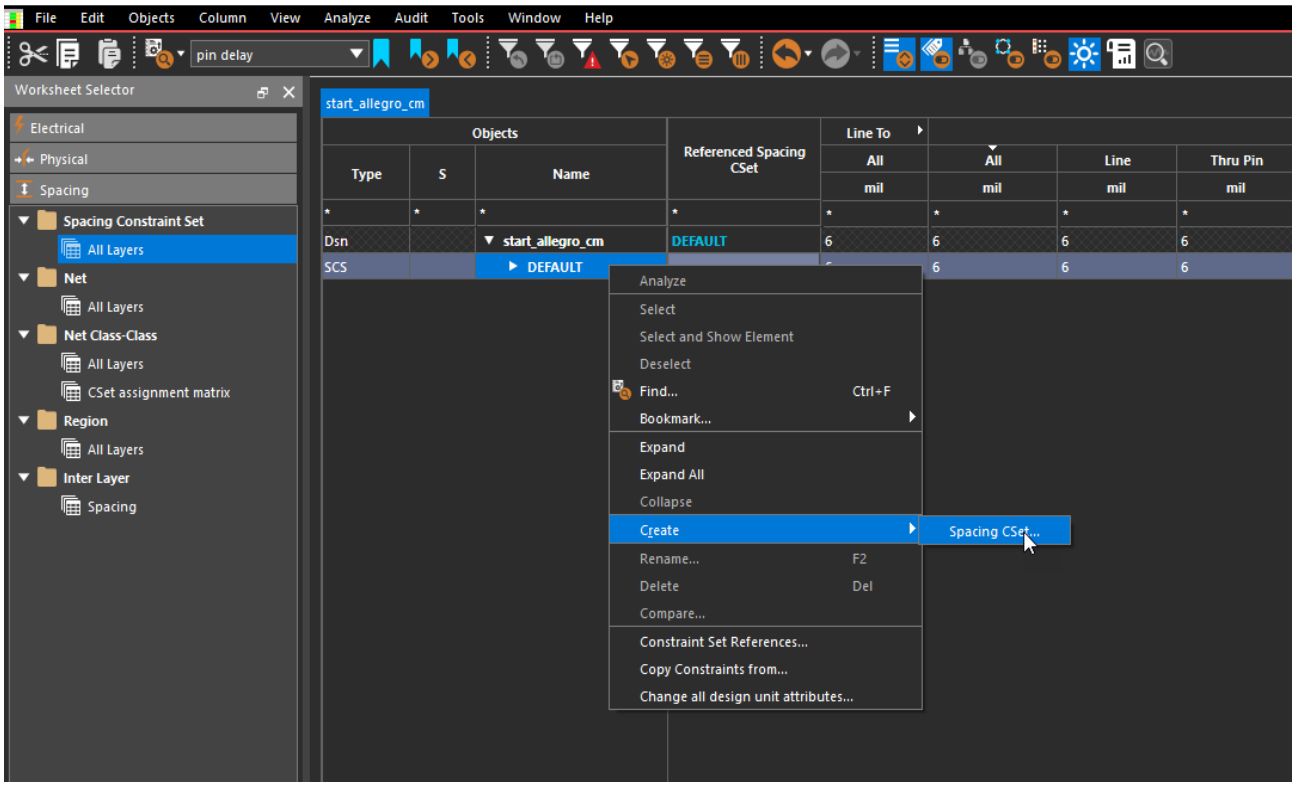
Task Overview

You will create a Spacing CSet from the DEFAULT and assign constraints to it.

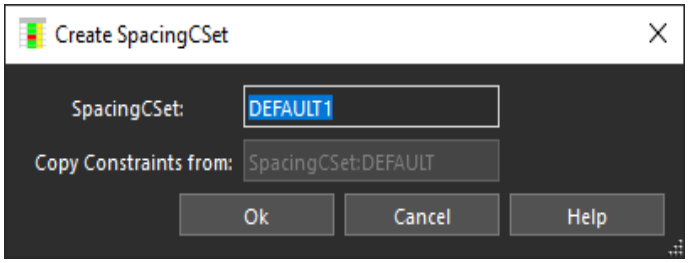
Steps

1. Open Constraint Manager and select *Spacing* domain.
2. Select *All Layers* worksheet under *Spacing Constraint Set* workbook.

3. Click the DEFAULT cell and choose *Create – Spacing CSet* from the right-click pop-up menu.



The *Create SpacingCSet* dialog box appears.

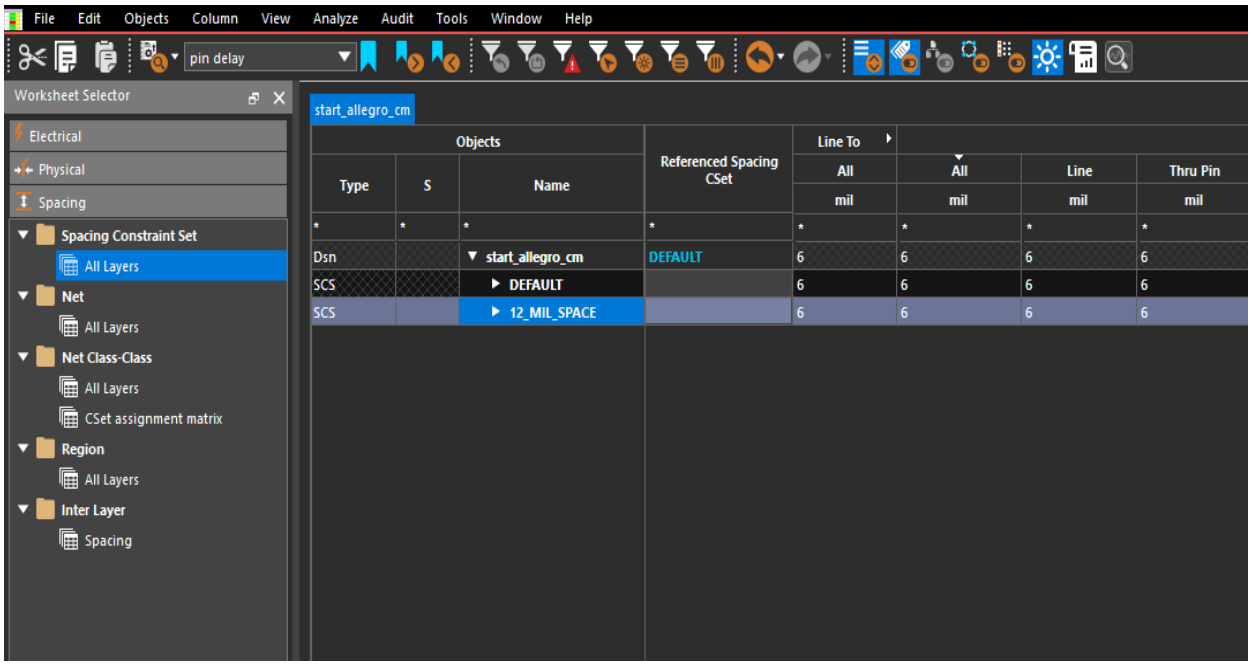


4. Enter the new Spacing CSet name as `12_MIL_SPACE` in the *SpacingCSet* field.

Note: You can see the constraints are copied from the DEFAULT spacing CSet.

5. Click *Ok*.

The instance of the CSet *12_MIL_SPACE* is displayed in the *Objects* column.



You will now enter the new values to the rules.

6. Change the value for all the *Line to* columns from 6 to 12 for 12_MIL_SPACE.

Tip

You can change the values of all columns simultaneously. Select the first cell and user `Ctrl` + click or `Shift` + click to select multiple cells. Now enter the new value and press `Enter`. The values for all columns are updated.

Creating a new Spacing Constraint Set from existing Spacing CSet

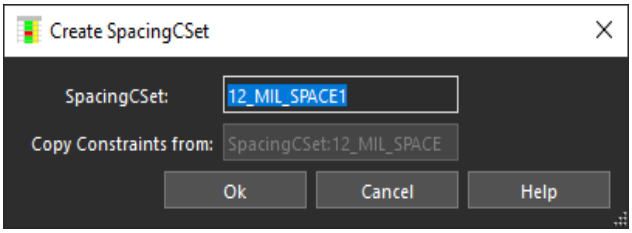
Task Overview

You will create Spacing CSet from the existing CSet and assign values to it.

Steps

1. Select *All Layers* worksheet under *Spacing Constraint Set* workbook.
2. Click the *12_MIL_SPACE* cell and choose *Create – Spacing CSet* from the right-click pop-up menu.

The *Create SpacingCSet* dialog box appears.

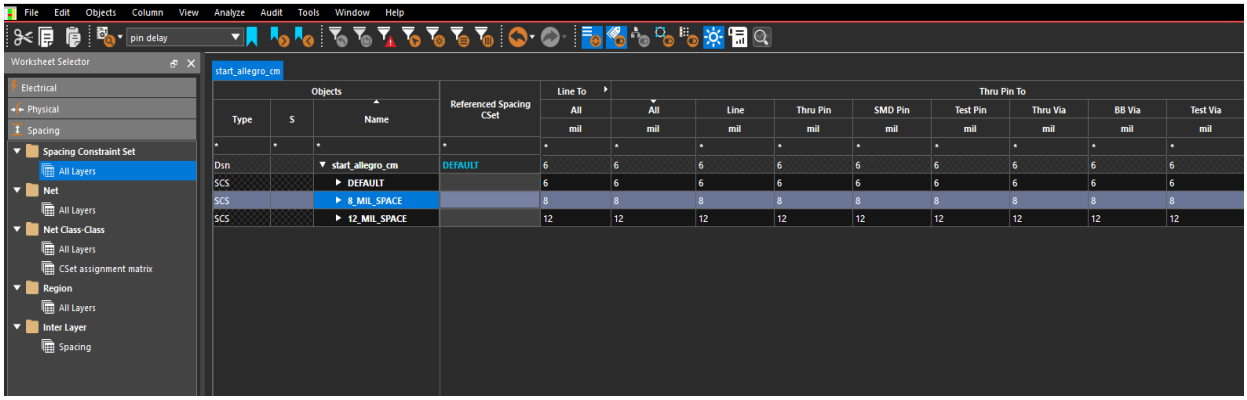


3. Enter `8_MIL_SPACE` in the *SpacingCSet* field.
4. Click *Ok*.

   The instance of the new CSet is displayed in the *Objects* column under DEFAULT CSet.

Note: You can see the constraints are copied from the 12_MIL_SPACE spacing CSet.

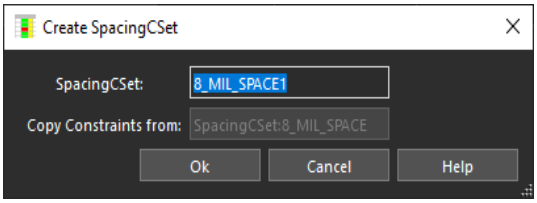
5. Change the value for all the *Line To* columns from 12 to 8.



Similarly, create one more spacing CSet.

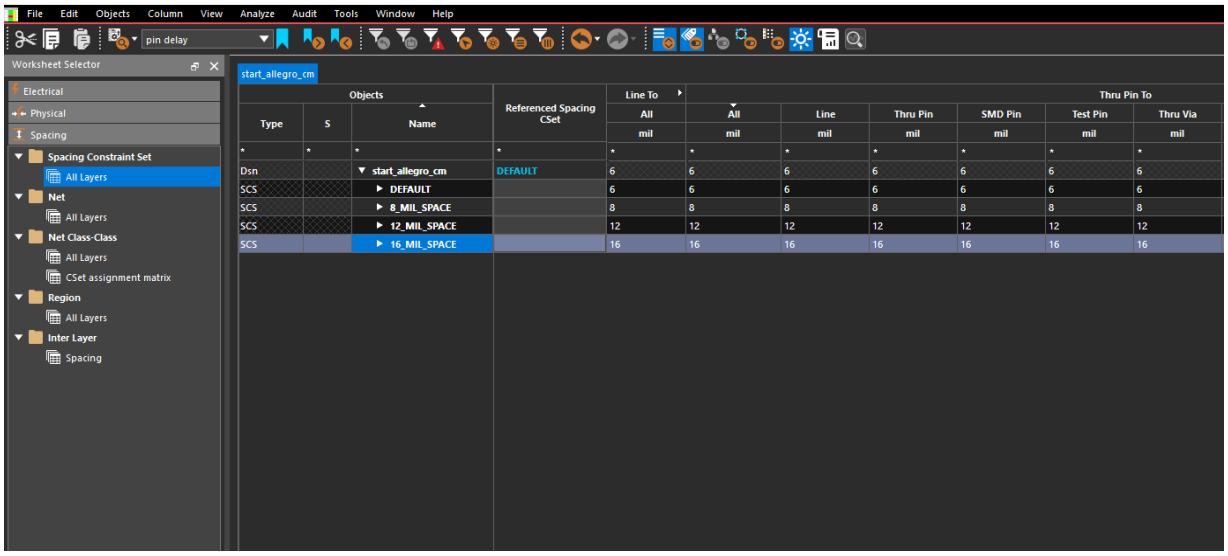
6. Click the *8_MIL_SPACE* cell and choose *Objects – Create – Spacing CSet*

   The *Create SpacingCSet* dialog box appears.



7. Enter `16_MIL_SPACE` in the *SpacingCSet* filed.
8. Click *Ok*.

The instance of the new CSet is displayed in the *Objects* column above 12_MIL_SPACE CSet.



9. Change the value for all the columns under *Line To* from 8 to 16.

   Similarly, create one more spacing CSet.

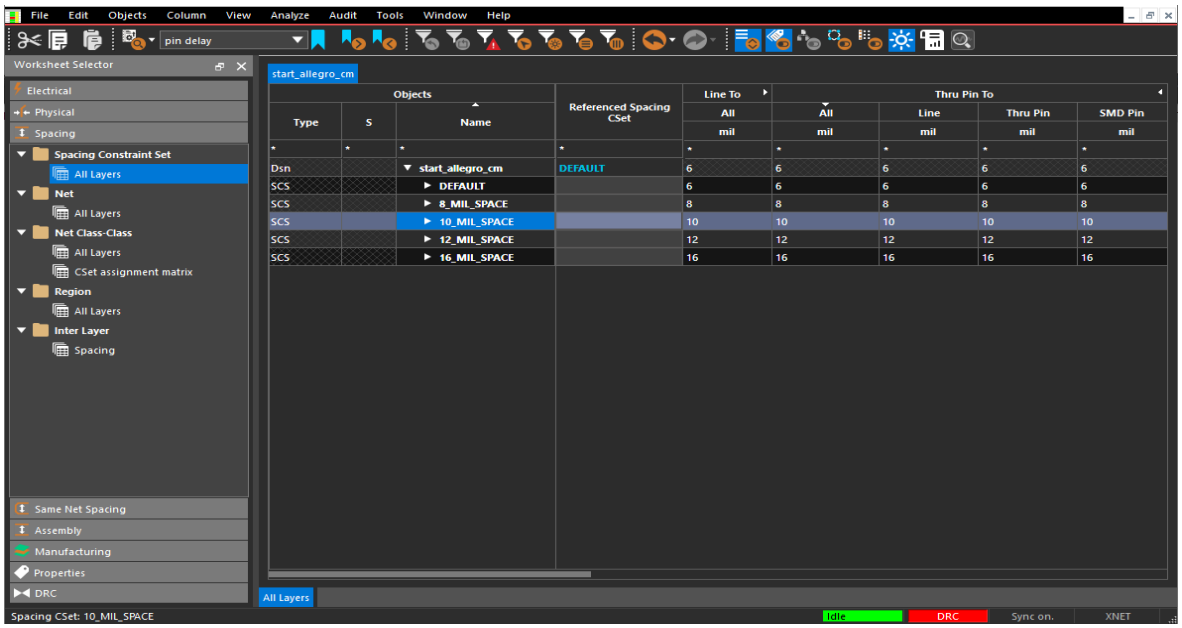
10. Select the *8_MIL_SPACE* cell and choose *Create – Spacing CSet* from the pop-up menu.

11. Enter the Spacing CSet name as 10_MIL_SPACE in the *SpacingCSet* filed.

12. Click *Ok*.

    The instance of the new CSet is displayed in the *Objects* column above 12_MIL_SPACE CSet.

13. Change all the values for 10_MIL_SPACE from 8 to 10.



14. Close the Constraint Manager and save the layout in Allegro PCB Editor.

Assigning Spacing Constraint Sets to Objects

Task Overview

You will now assign spacing CSet to nets.

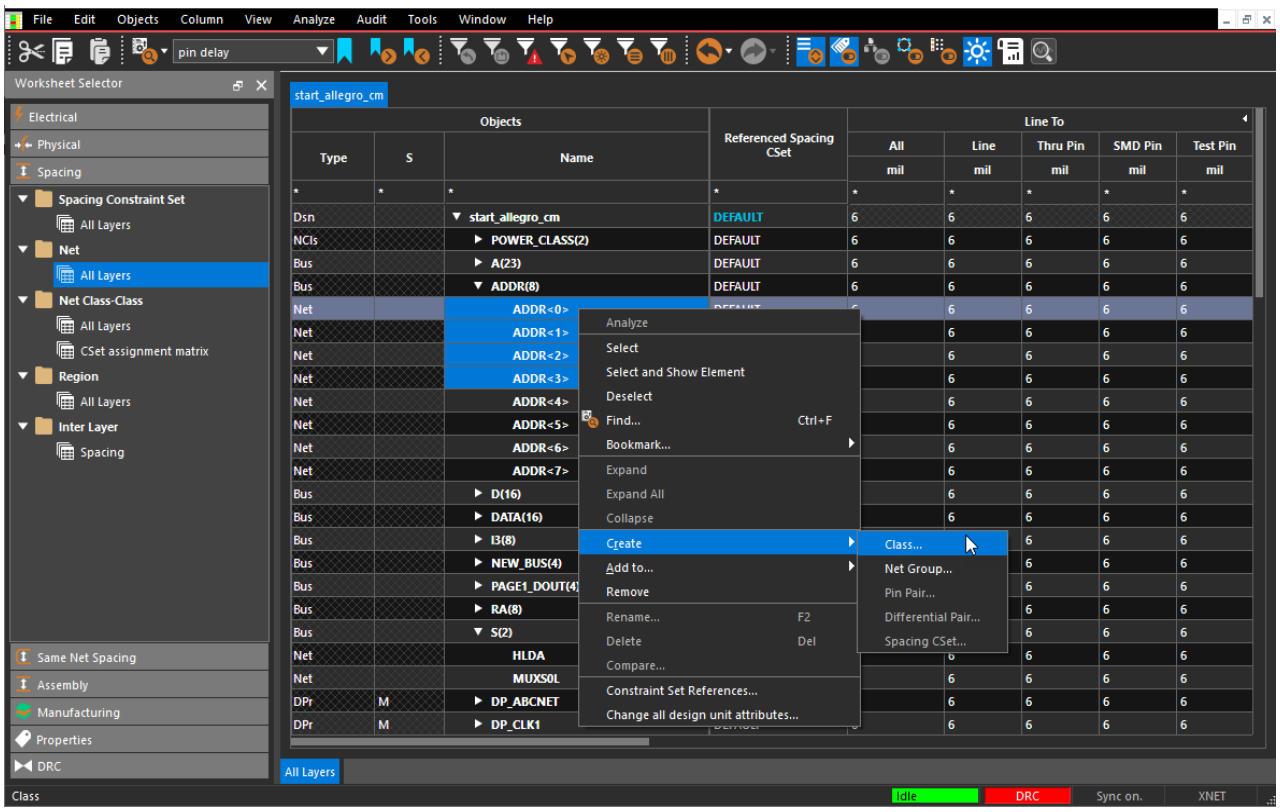
Creating Net Class

Net Class is used to group the nets with same spacing requirement.

To create a Net Class:

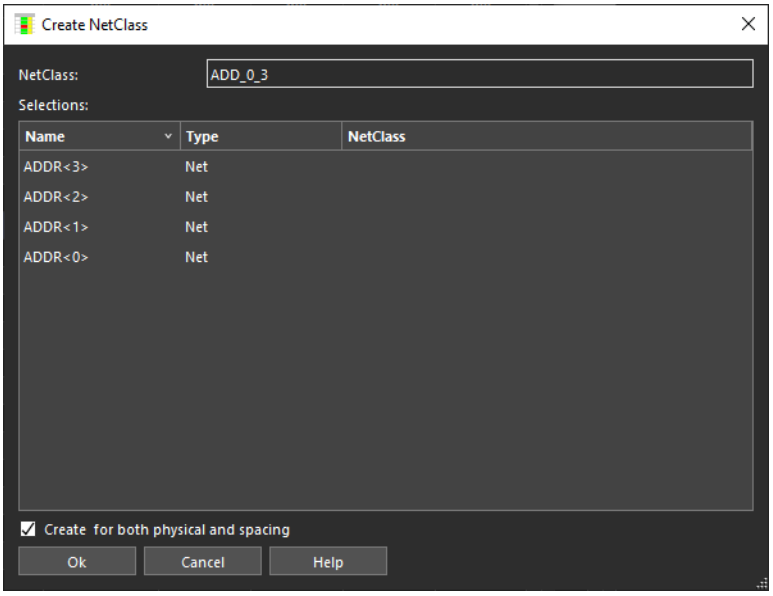
1. Launch Constraint Manager.
2. In the *Net* workbook under *Spacing* domain, click *All Layers.*
3. Double-click to expand the *Line To* column.
4. Expand the bus *ADDR* and select the nets *ADDR<0>* to *ADDR<3>*.

5. Right-click the selection and choose *Create – Class* from the right-click pop-up menu.



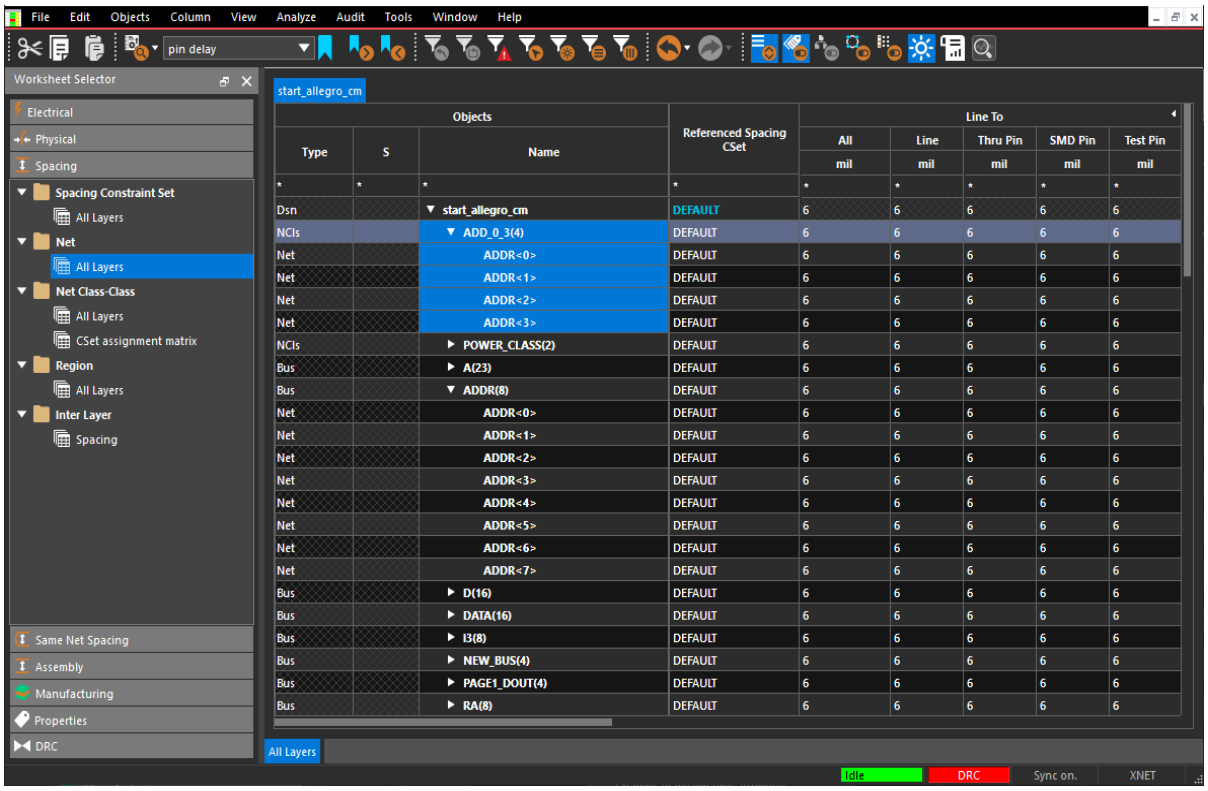
The *Create Net Class* dialog box appears.

6. Enter `ADD_0_3` in the *NetClass* filed.

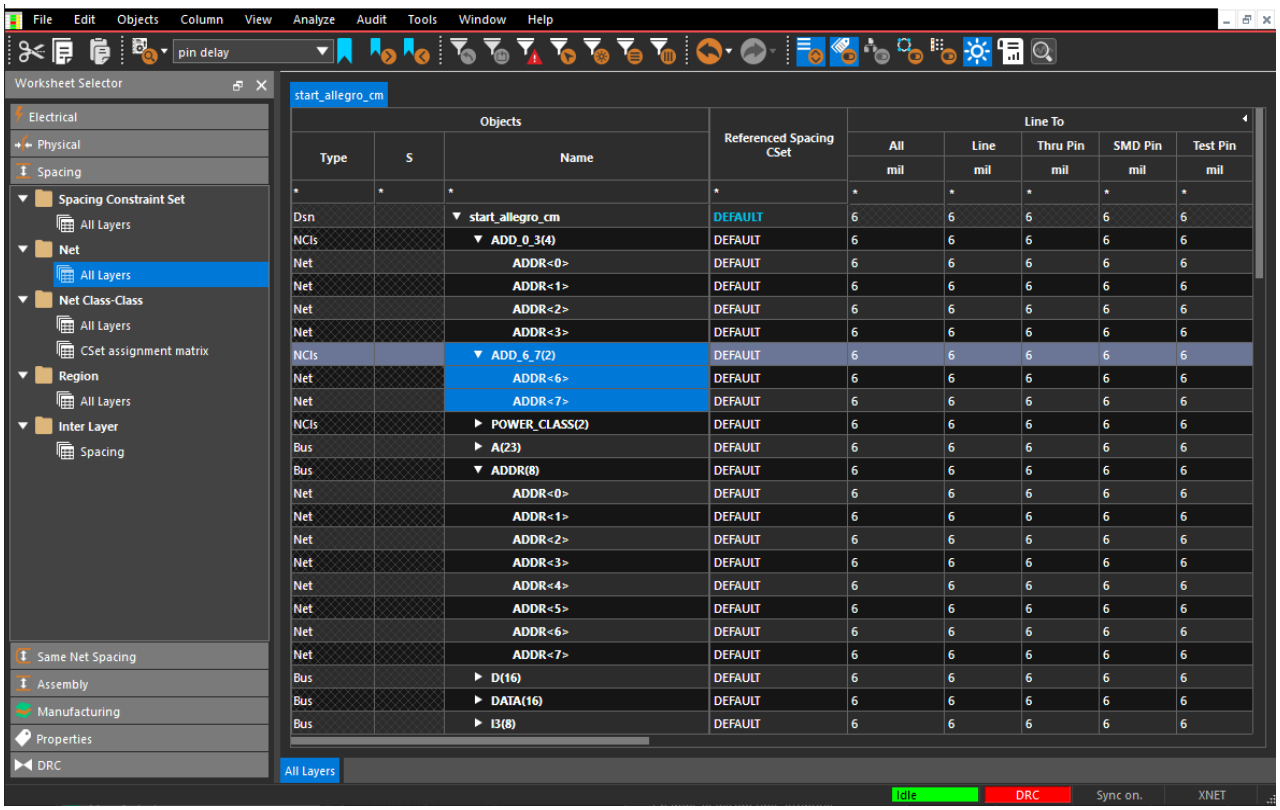


7. Click *Ok*.

The four nets are now placed in the net class *ADD_0_3*.



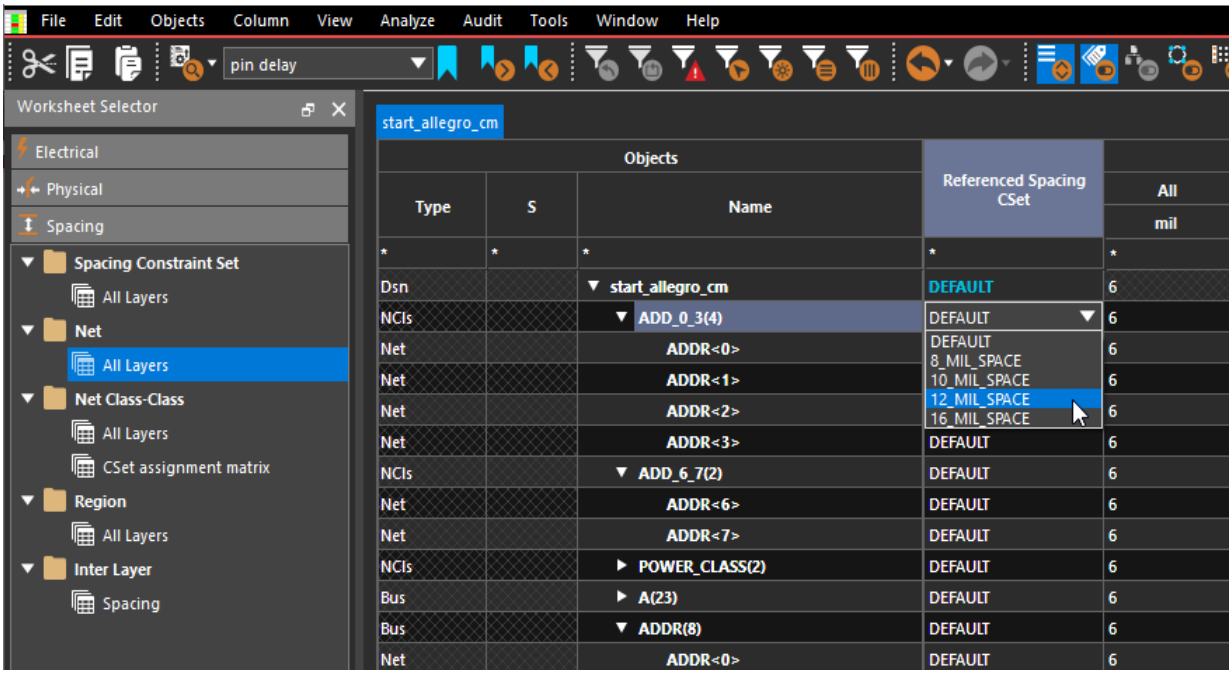
8. Similarly, create Net Class *ADD_6_7* which includes two nets *ADDR<6>* and *ADDR<7>.*



Assigning CSet to Net Class

1. In the *Net* workbook under *Spacing* domain, click *All Layers.*
2. Double-click the *Line To* column to expand it.
3. Select the Net Class *ADD_0_3*(4).

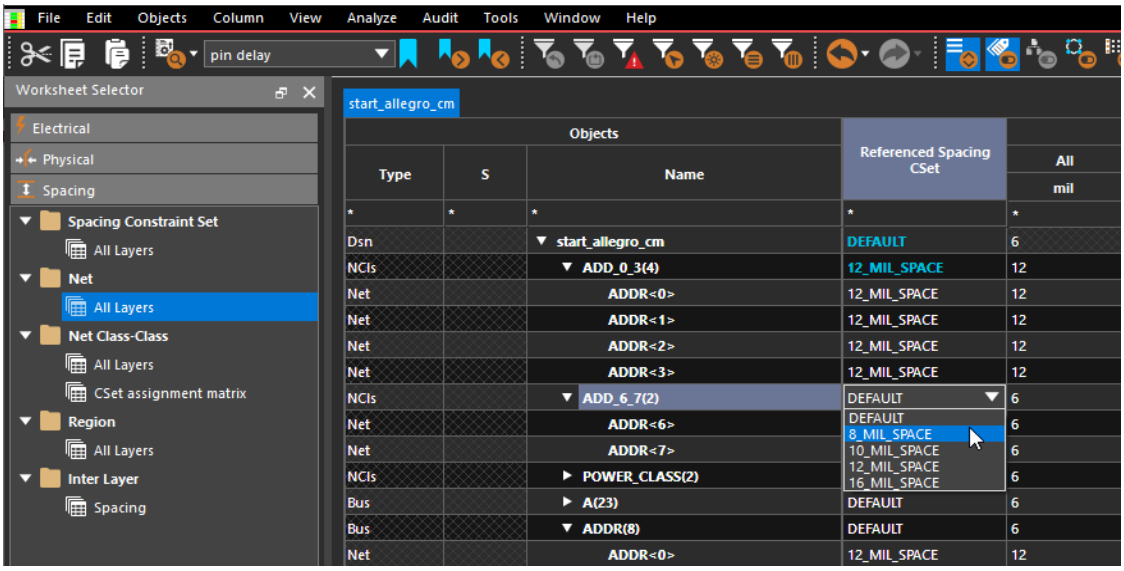
4. Click the column *Referenced Spacing CSet* and select *12_MIL_SPACE* from the drop-down list.



The Net Class *ADD_0_3*(4) that contains four nets *ADDR<0>* to *ADDR<3>*, will use the *12_MIL_SPACE* rule such that when these nets are routed, all etch will remain 12 mils away.

5. Select the Net Class *ADD_6_7*(2).

6. Click the column *Referenced Spacing CSet* and select *8_MIL_SPACE* from the drop-down list.



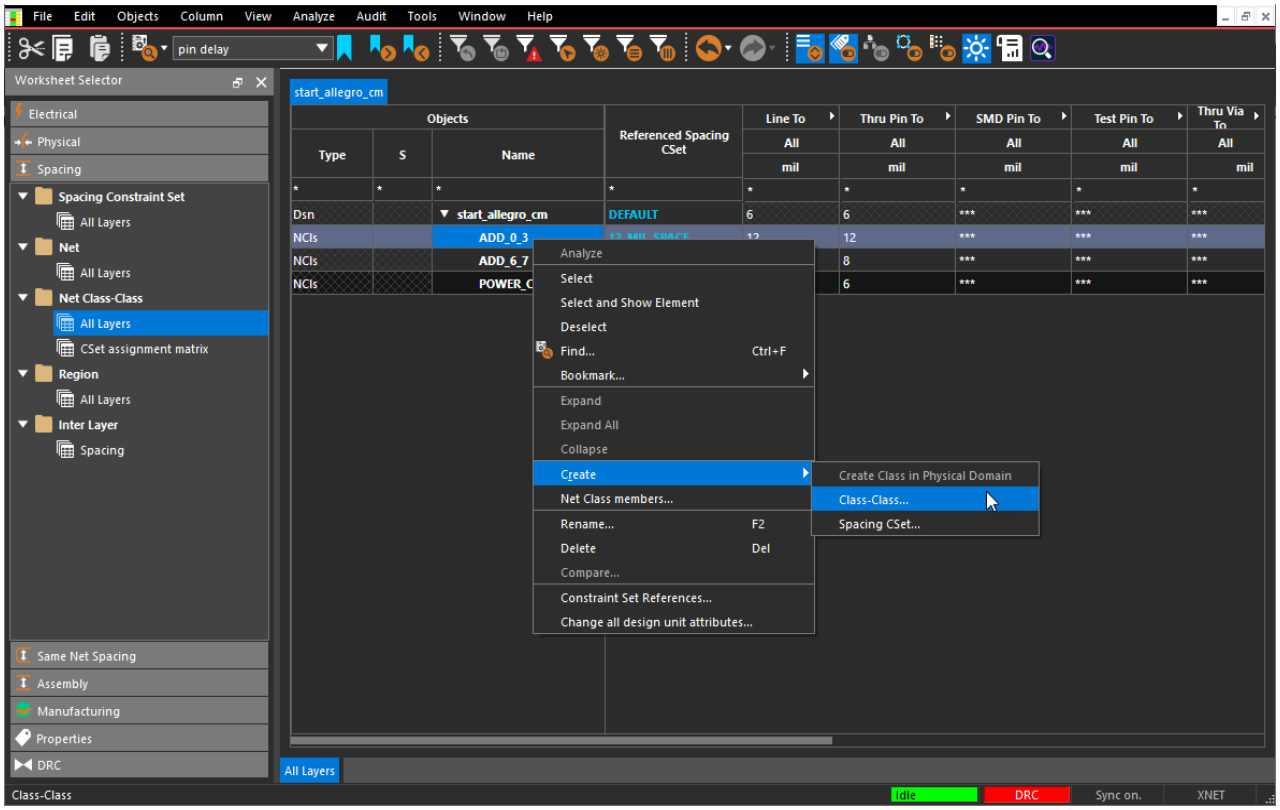
The Net Class *ADD_6_7*(2) that contains two nets *ADDR<6>* to *ADDR<7>*, will use the *8_MIL_SPACE* rule.

Creating Net Class-Class

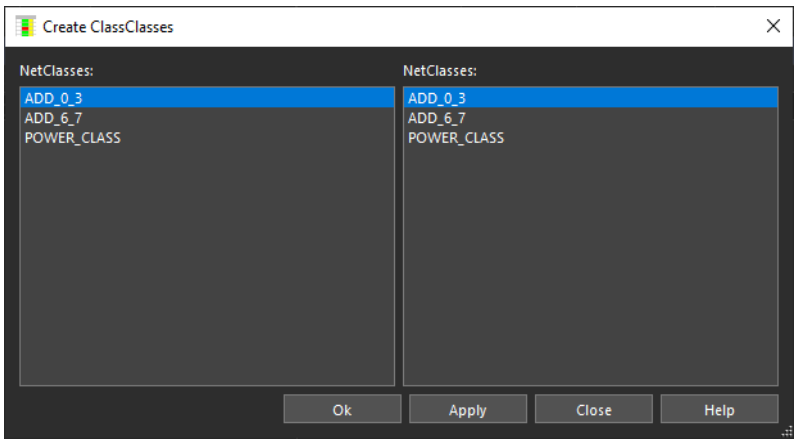
To create a Net Class-Class:

1. In the *Net Class-Class* workbook under *Spacing* domain, click *All Layers.*

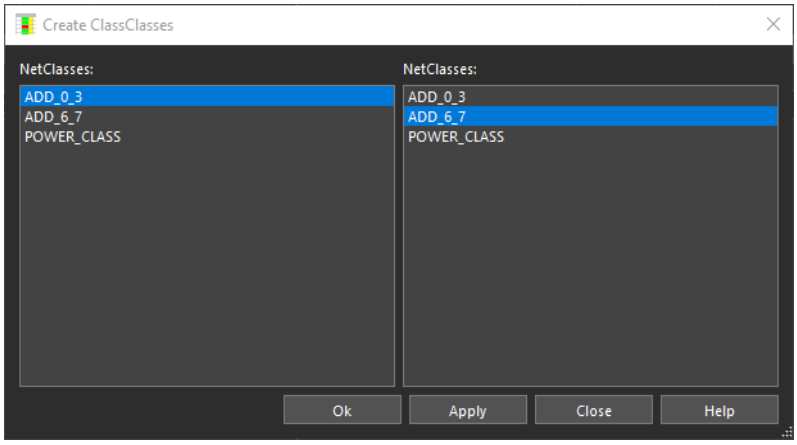
2. Right-click Net Class *AD_0_3* and choose *Create – Class-Class* from the right-click pop-up menu.



The *Create ClassClasses* dialog box appears.

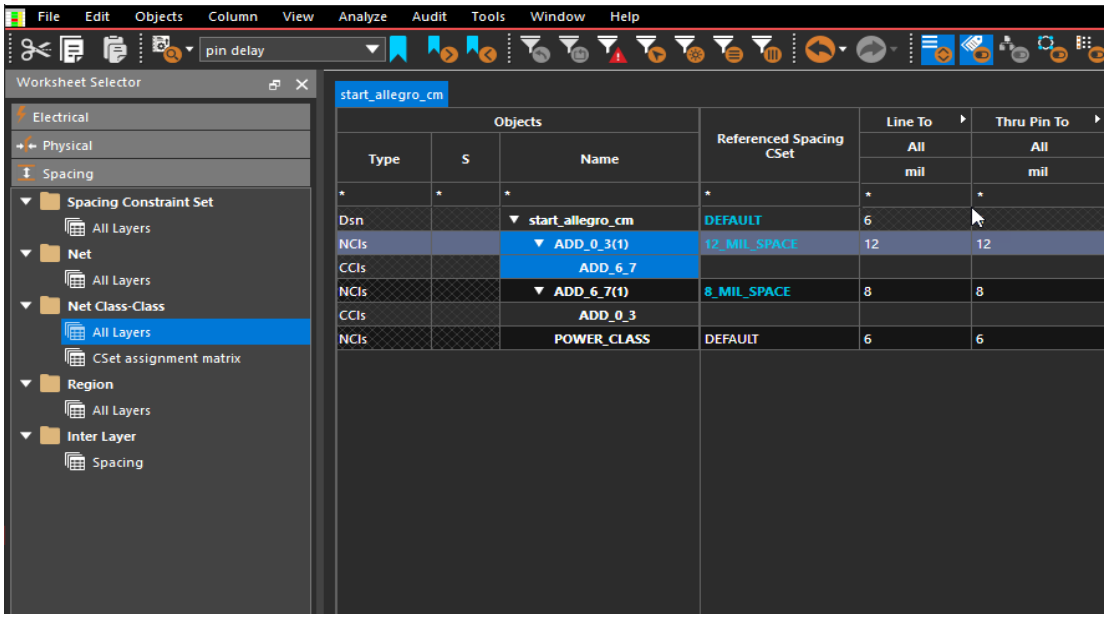


3. Select Net Classes *ADD_0_3* and *ADD_6_7* from the left and right *Net Classes* list respectively.



4. Click *Apply* and then click *Ok.*

The Net Class-Class *ADD_0_3:ADD_6_7* is created.

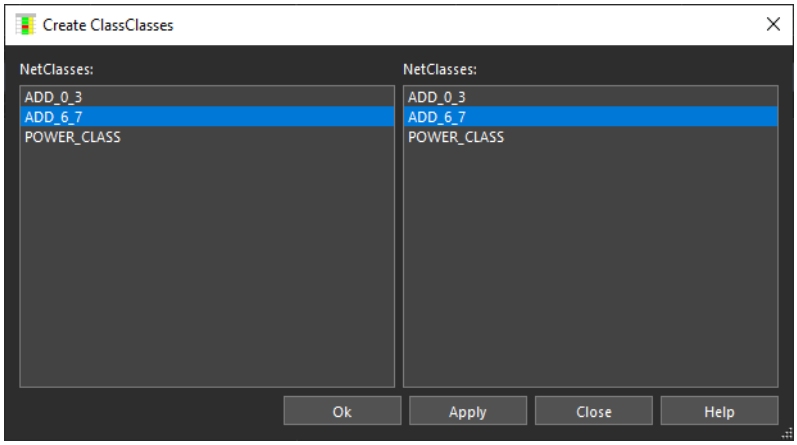


Similarly, create Net Class-class for Net Class *ADD_6_7.*

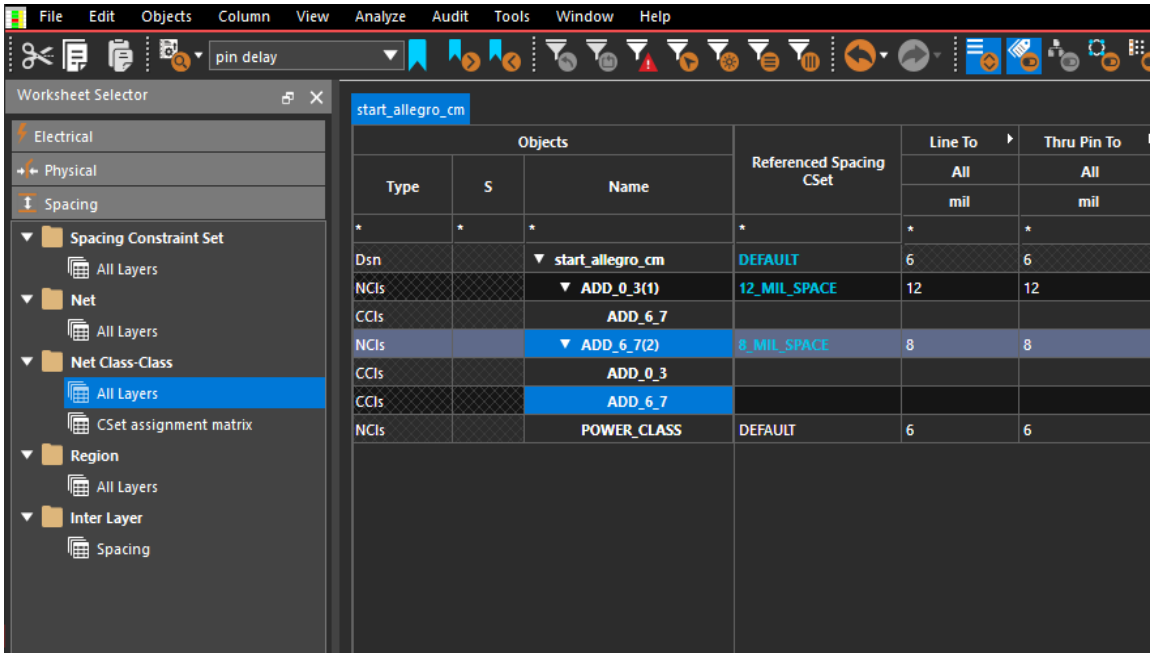
5. Right-click Net Class *AD_6_7(1)* and choose *Create – Class-Class* from the pop-up menu.

The *Create ClassClasses* dialog box appears.

6. Select Net Classes *ADD_6_7* from the left and right *Net Classes* list respectively.



7. Click *Apply* and then *Ok.*
8. The Net Class-Class *ADD_6_7:ADD_6_7* is created.

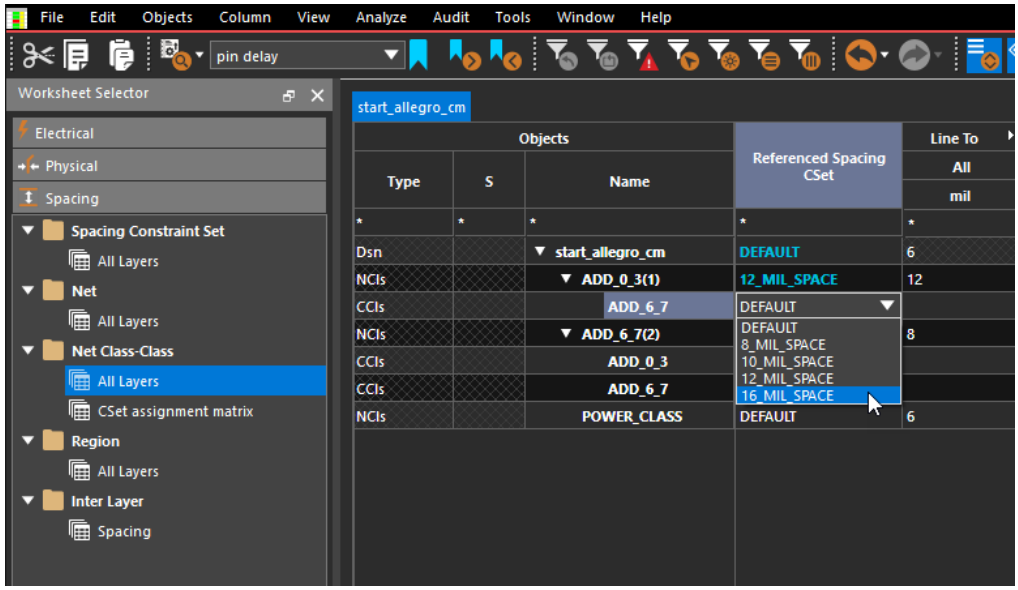


Assigning CSet to Net Class-Class

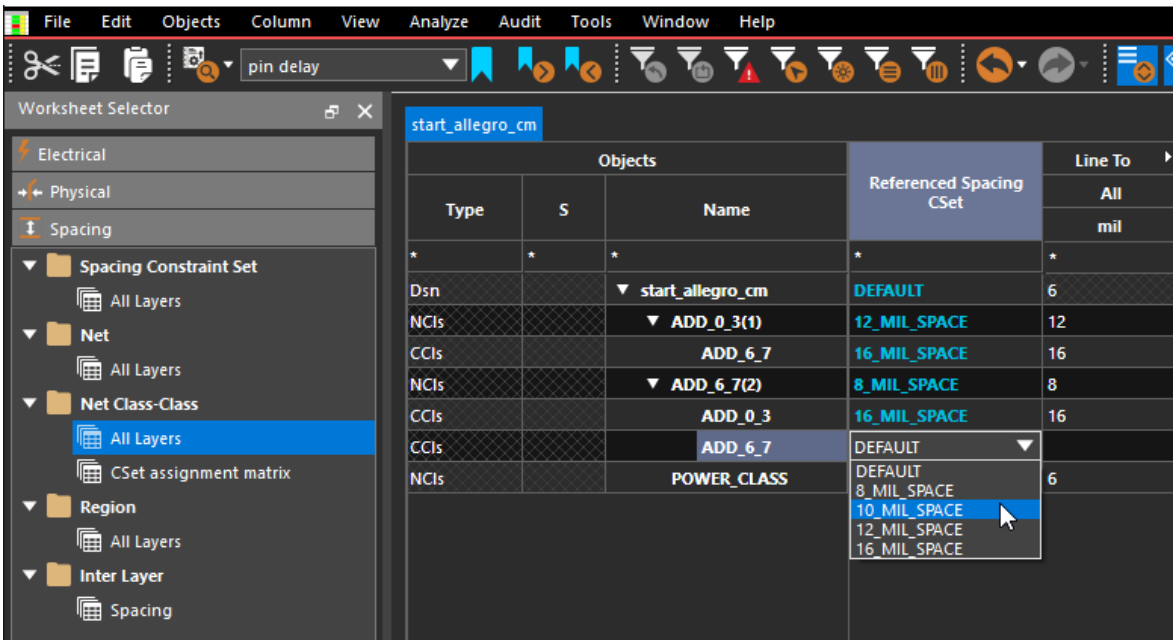
To assign CSet to a Net Class-Class:

1. In the *Net Class-Class* workbook under *Spacing* domain, click *All Layers.*
2. Select Class-Class *ADD_6_7* under the Net Class *ADD_0_3*(1).

3. Select *16_MIL_SPACE* from the drop-down list in the *Referenced Spacing CSet* column.



4. Select *10_MIL_SPACE* from the drop-down list in the *Referenced Spacing CSet* column for Net Class-Class *ADD_6_7* under Net Class *ADD_6_7(2)*.

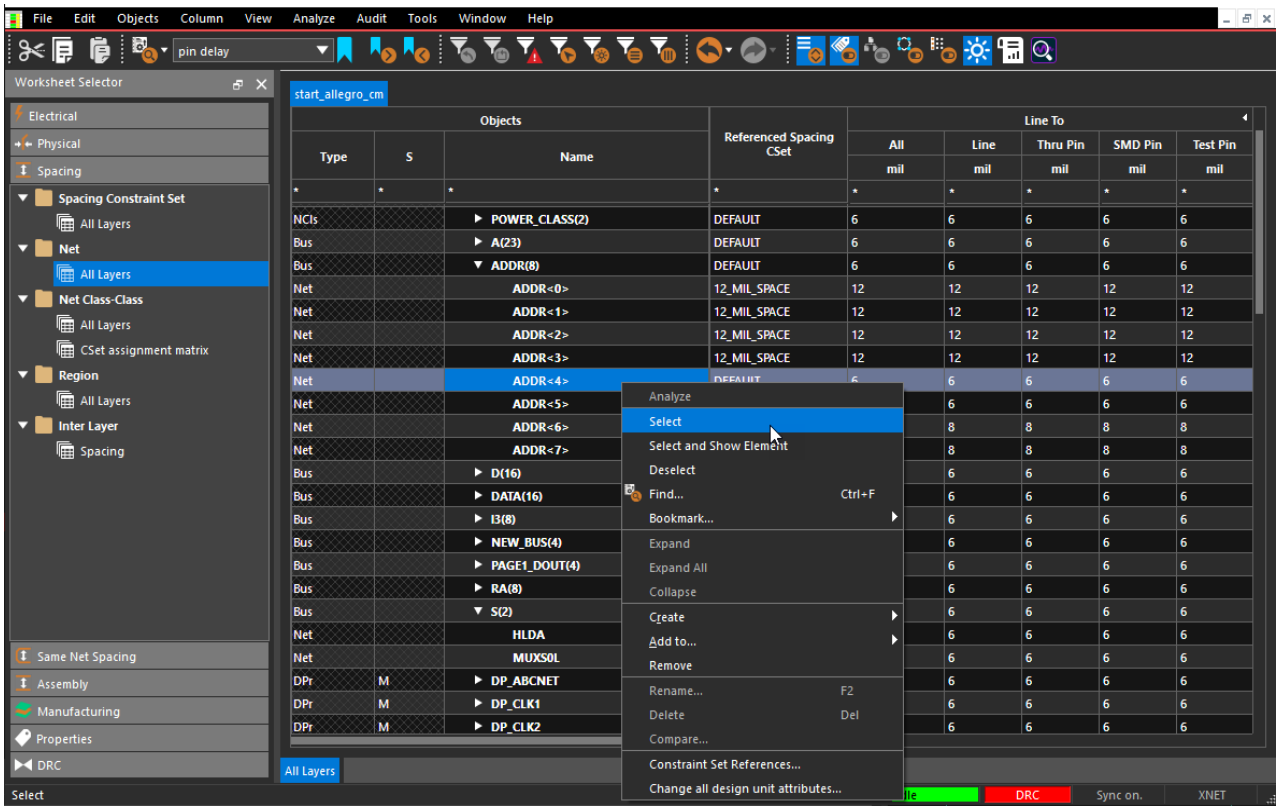


5. Close the Constraint Manager and save the layout in Allegro PCB Editor.

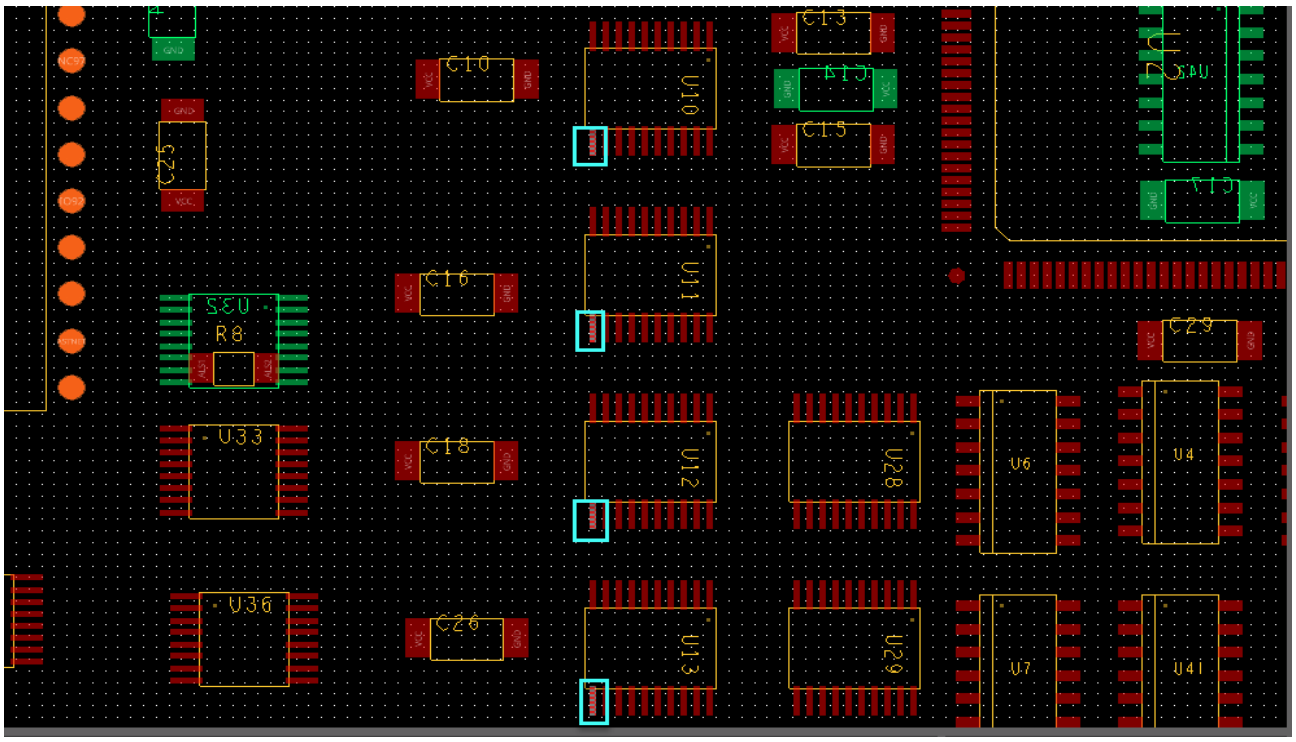
Routing with Spacing Constraints

Routing with DEFAULT Constraint

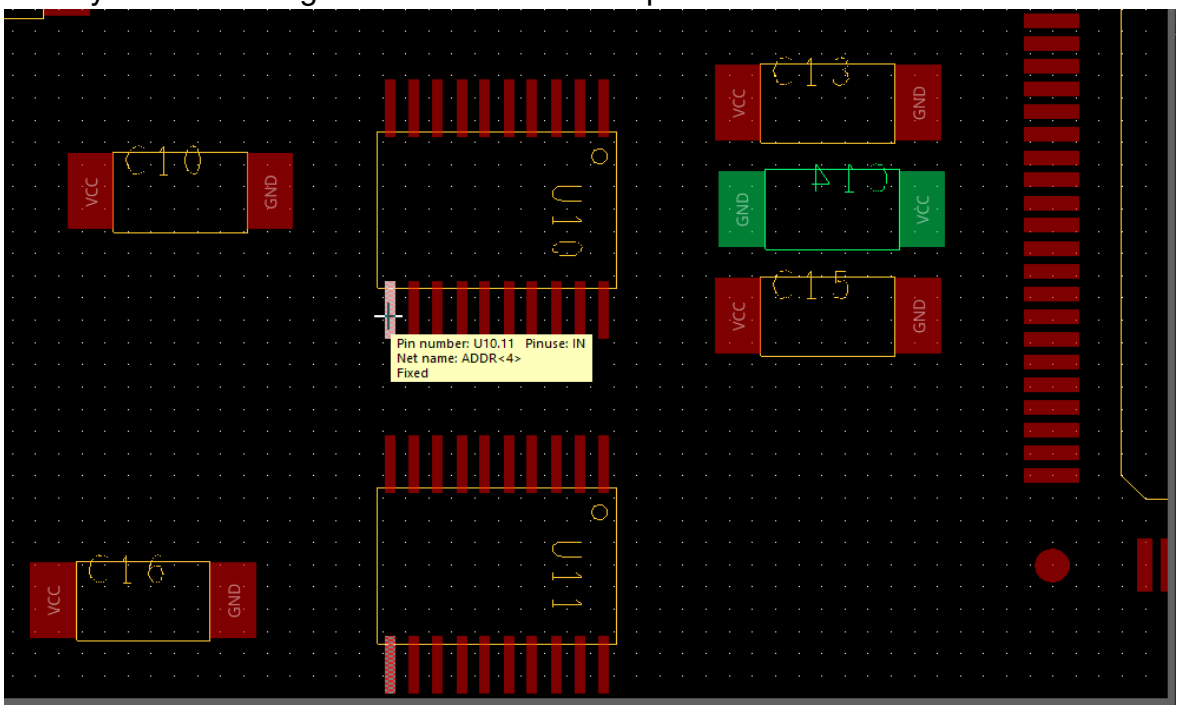
1. Launch Constraint Manager.
2. In the *Net* workbook under *Spacing* domain, click *All Layers.*
3. Right-click the net *ADDR<4>* under the bus *ADDR* and choose *Select* from the pop-up menu.



Allegro PCB Editor highlights the net on the components U10, U11, U12 and U13 on the board.

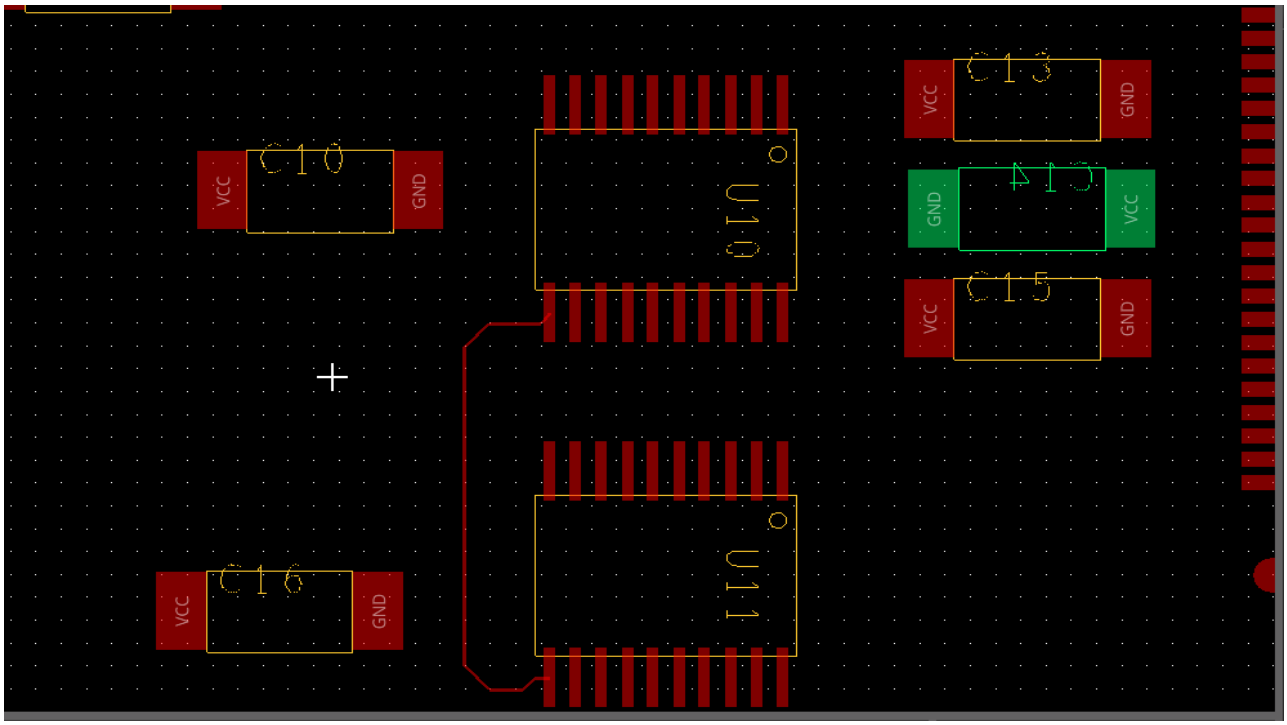


4. In Allegro PCB Editor, hover your cursor over the highlighted net (Addr<4>) on U10 from which you start adding etch/conductor. Data tip identifies its name.



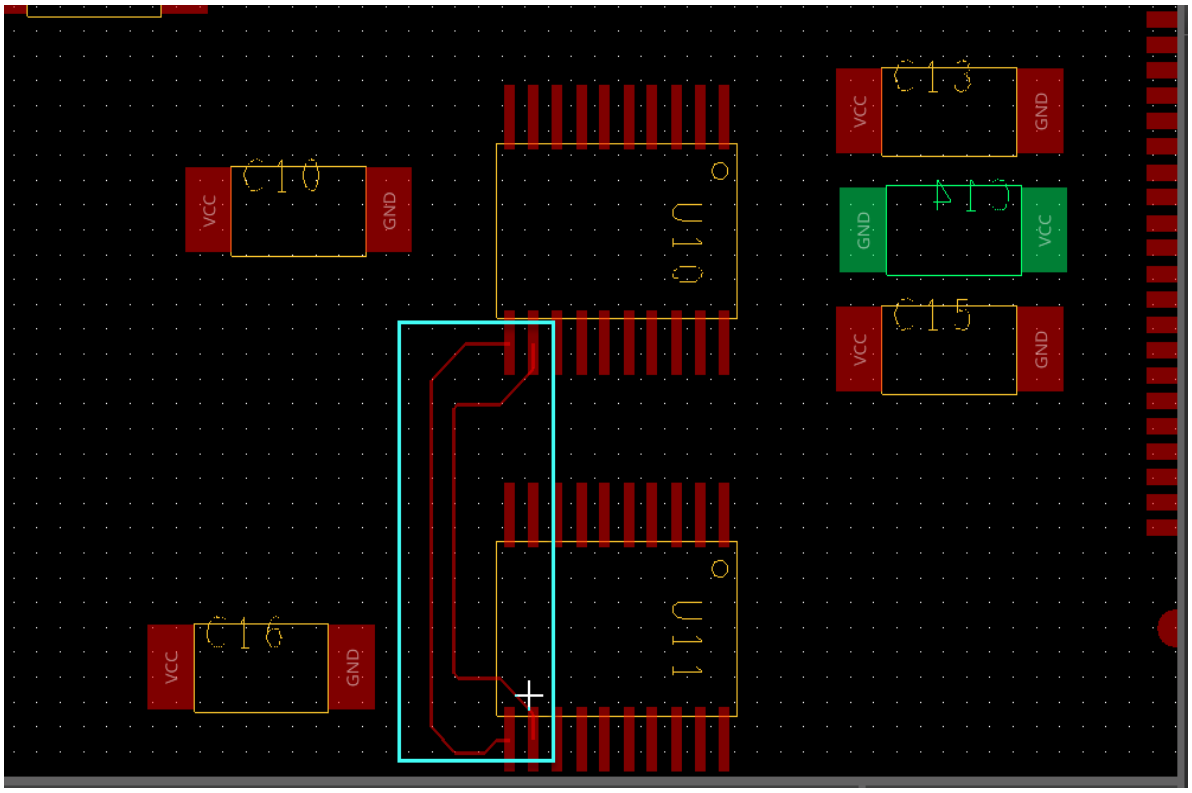
5. Choose *Route – Connect*.
6. Select the pin with net ADDR<4> on U10.

   A line is attached to the cursor.



7. Move the cursor to end the route at net ADDR<4> on U11.

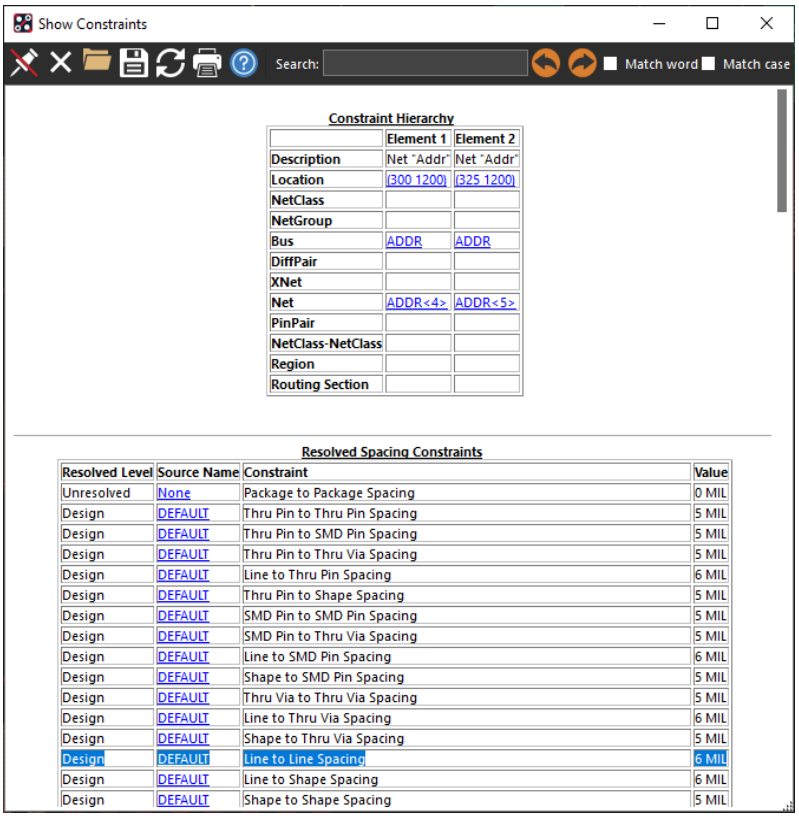
8. Similarly route the net *ADDR<5>* from U10 to U11.



9. Choose *Display – Constraint* or from tool bar click the  icon.

10. Select both the nets *ADDR<4> and ADDR<5>.*

The *Show Constraint* window is displayed.



The *Constraint Hierarchy* section displays that the nets *ADDR<4>* and *ADDR<5>* are elements of bus *ADDR*. The *Resolved Spacing Constraints* section displays the DEFAULT constraint rule is followed by the nets.

11. Close the *Show Constraint* form and choose *Done* from the right-click pop-up menu.

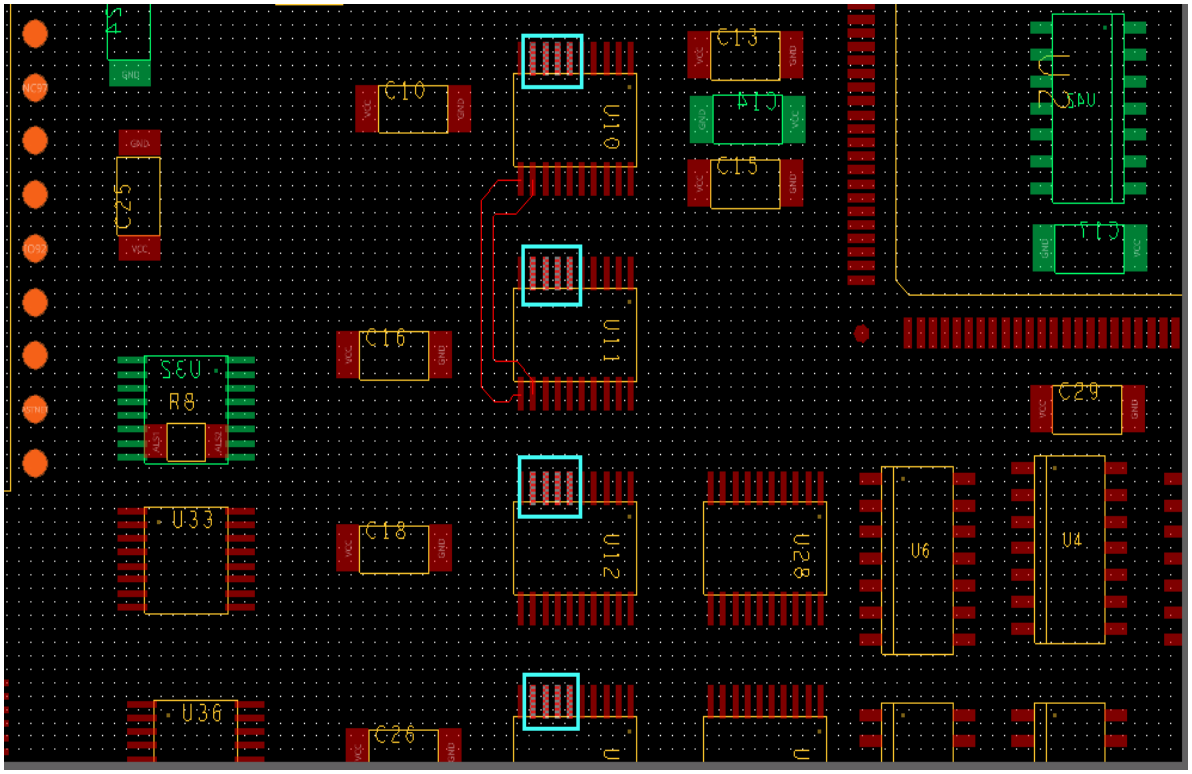
12. Close the Constraint Manager and save the layout in Allegro PCB Editor.

Routing with Net Class

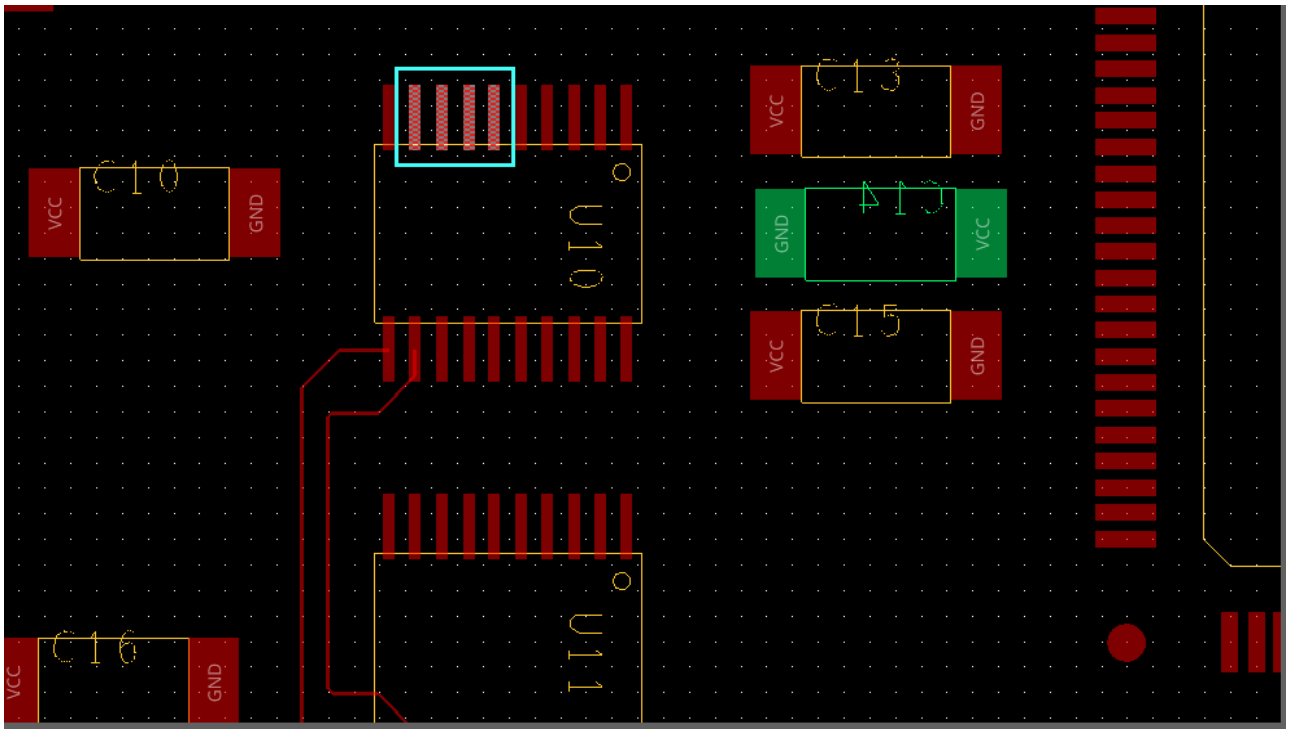
1. In the *Net* workbook under *Spacing* domain, click *All Layers.*

2. Select and right-click the nets *ADDR<0>* to *ADDR<3>* under the bus *ADDR* and choose *Select* from the pop-up menu.

Allegro PCB Editor highlights the net on the components U10, U11, U12 and U13 on the board.



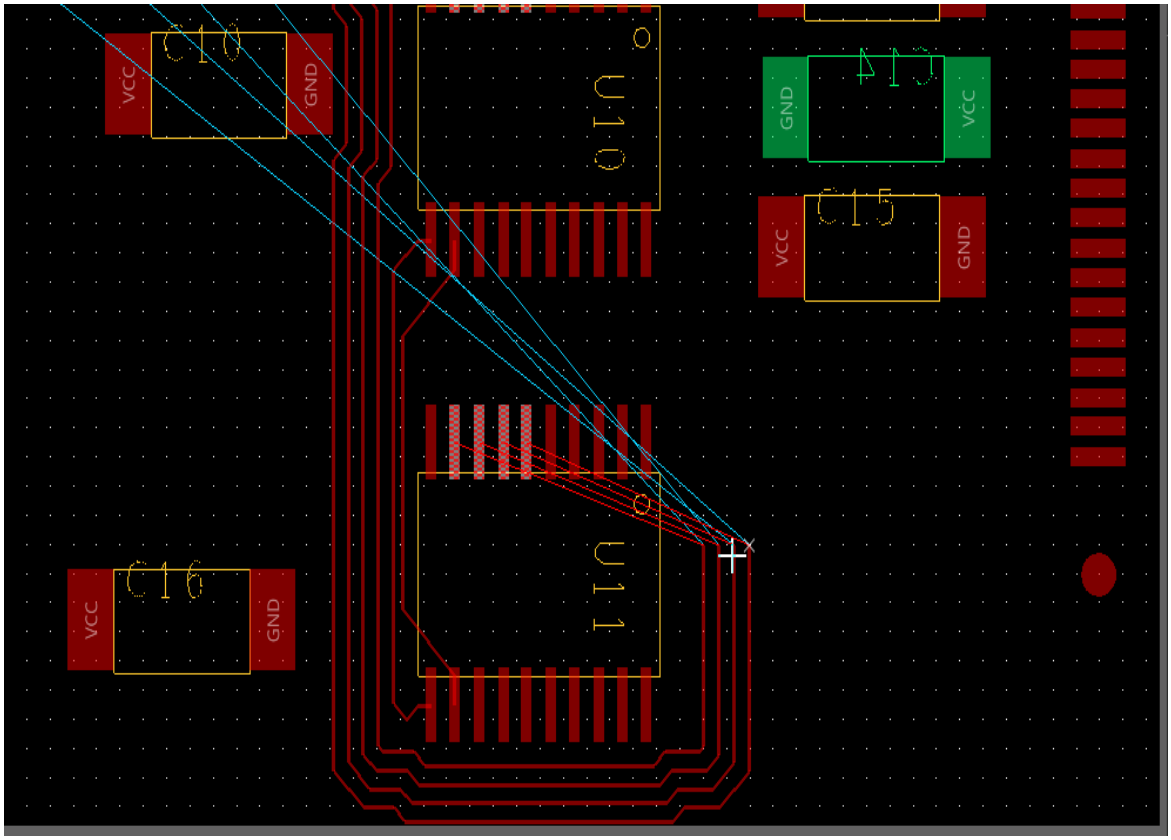
3. In Allegro PCB Editor, select the pins with nets *ADDR<0>* to *ADDR<3>* on U10.



4. Choose *Route – Connect* and click the pins with selected nets on U10.

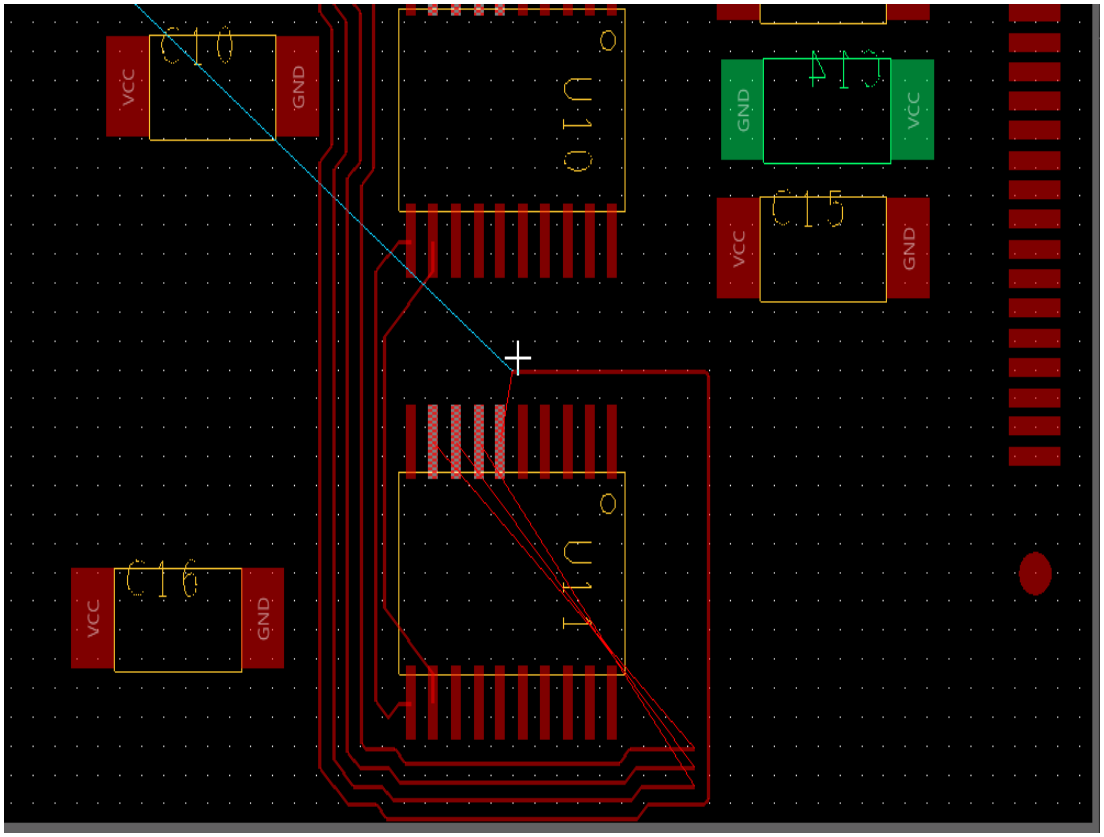
Four lines are attached to the cursor.

5. Move the route to the nets *ADDR<0>* to *ADDR<3>* on U11 as shown in the following figure.

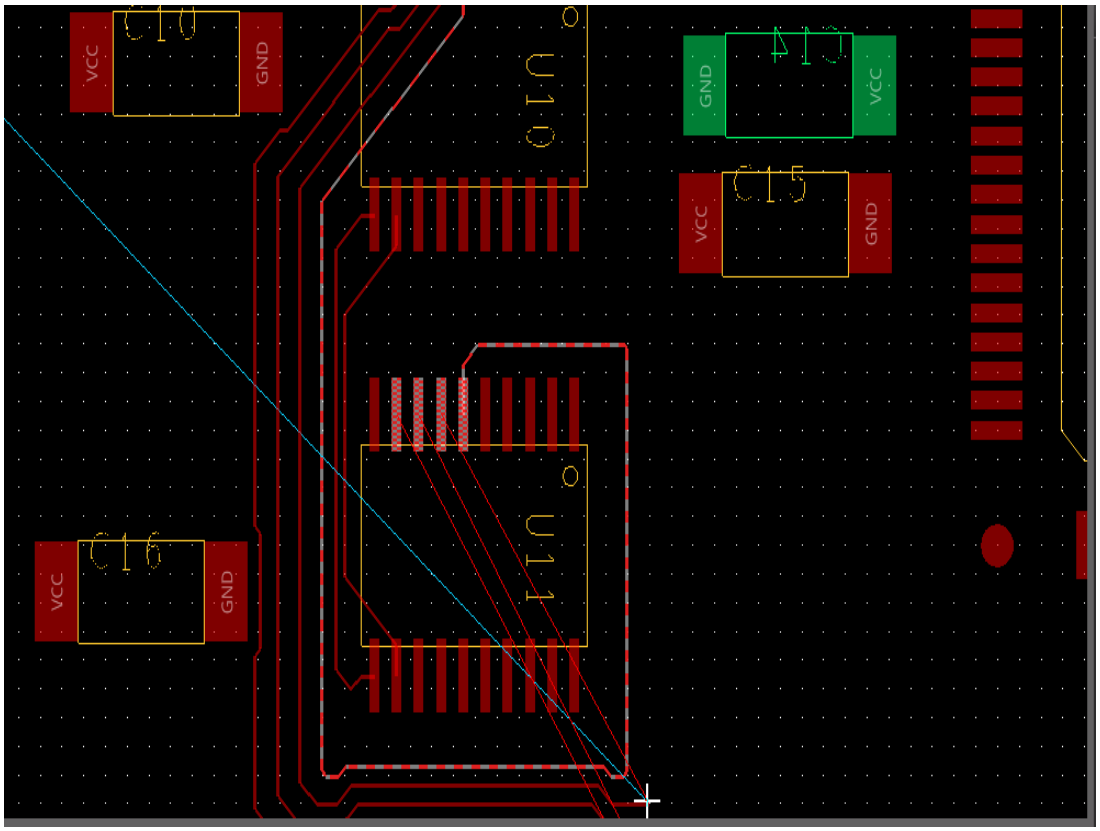


6. Right-click and select *Sinlge Trace Mode* from pop-up menu.

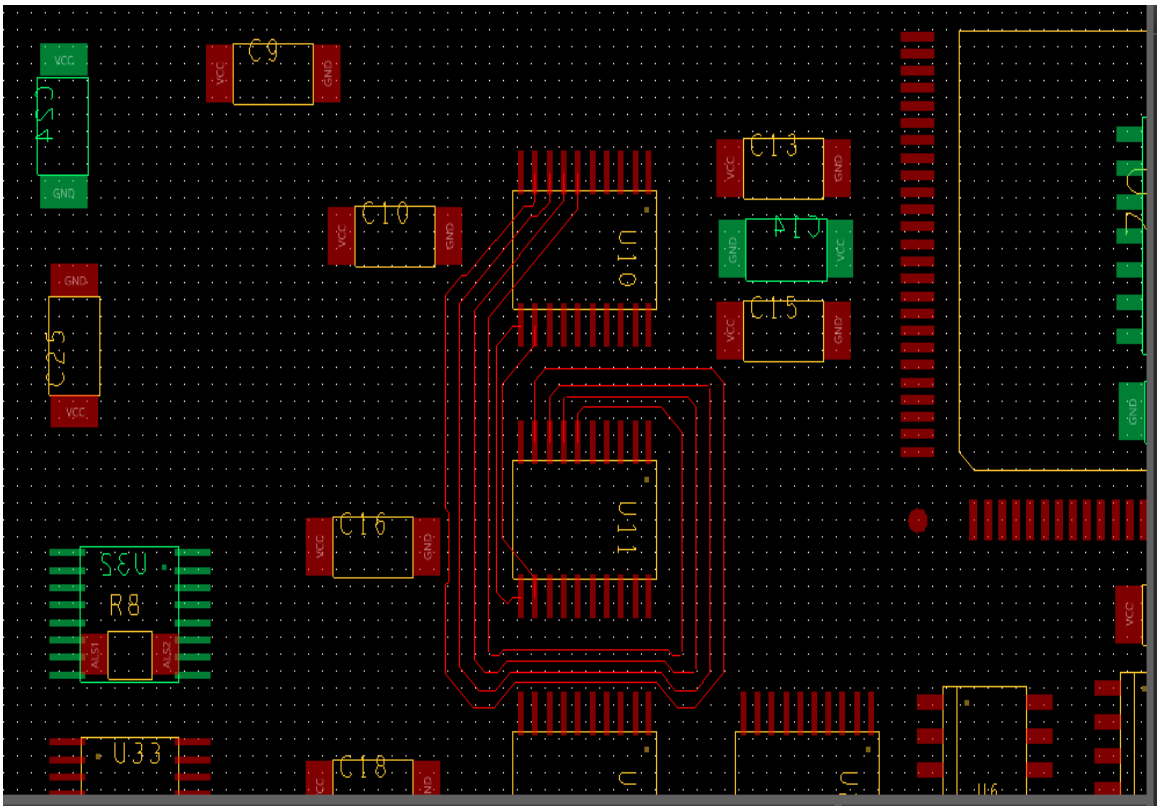
Single Trace Mode allows you to route one net at a time when routing more than one nets.



7. Terminate the route at net ADDR<3> on U11.

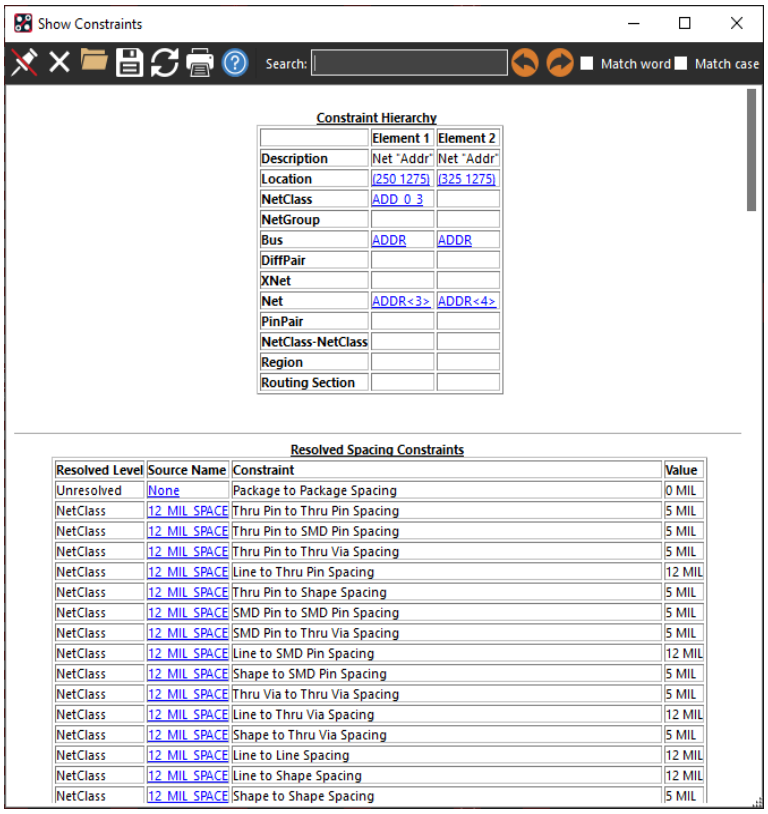


8. Similarly terminate other three routes at their respective nets on U11.



9. Choose *Display - Constraint* or from tool bar icon  to open the *Show Constraint* form.

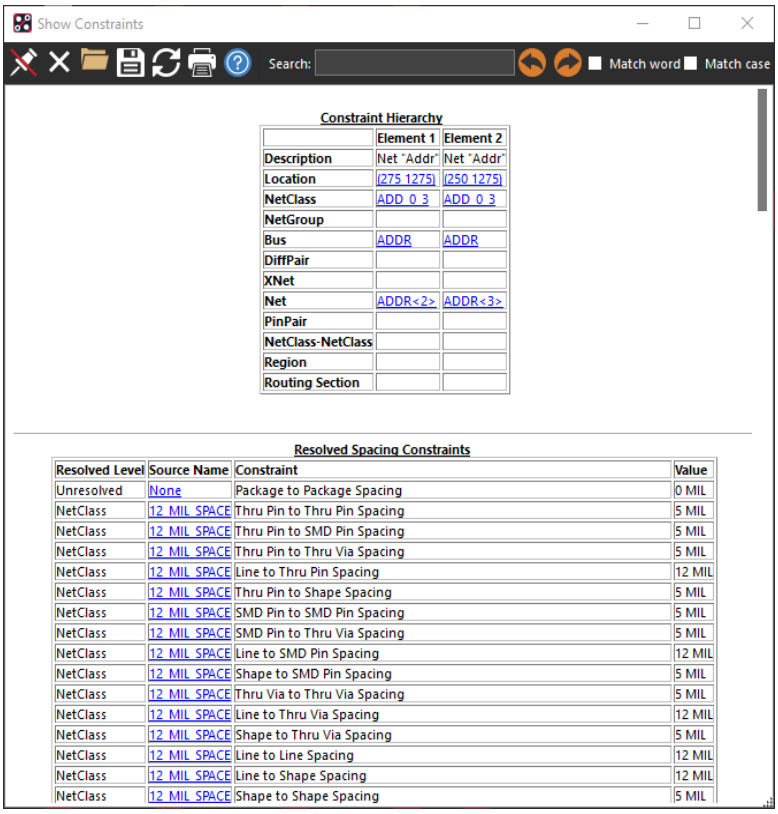
10. Select both the nets *ADDR<3> and ADDR<4>.*



The *Constraint Hierarchy* section shows that nets *ADDR<3>* and *ADDR<4>* are elements of bus *ADDR*. The net *ADDR<3>* is a part of Net Class *ADDR_0_3*; whereas the net *ADDR<4>* is not a part of any Net Class. The *Resolved Spacing Constraints* section shows that the 12_MIL_SPACE constraint rule assigned to Net Class *ADDR_0_3* is followed by the nets.

11. Close the *Show Constraint* window.

12. Now, select the nets *ADDR<2> and ADDR<3>.*



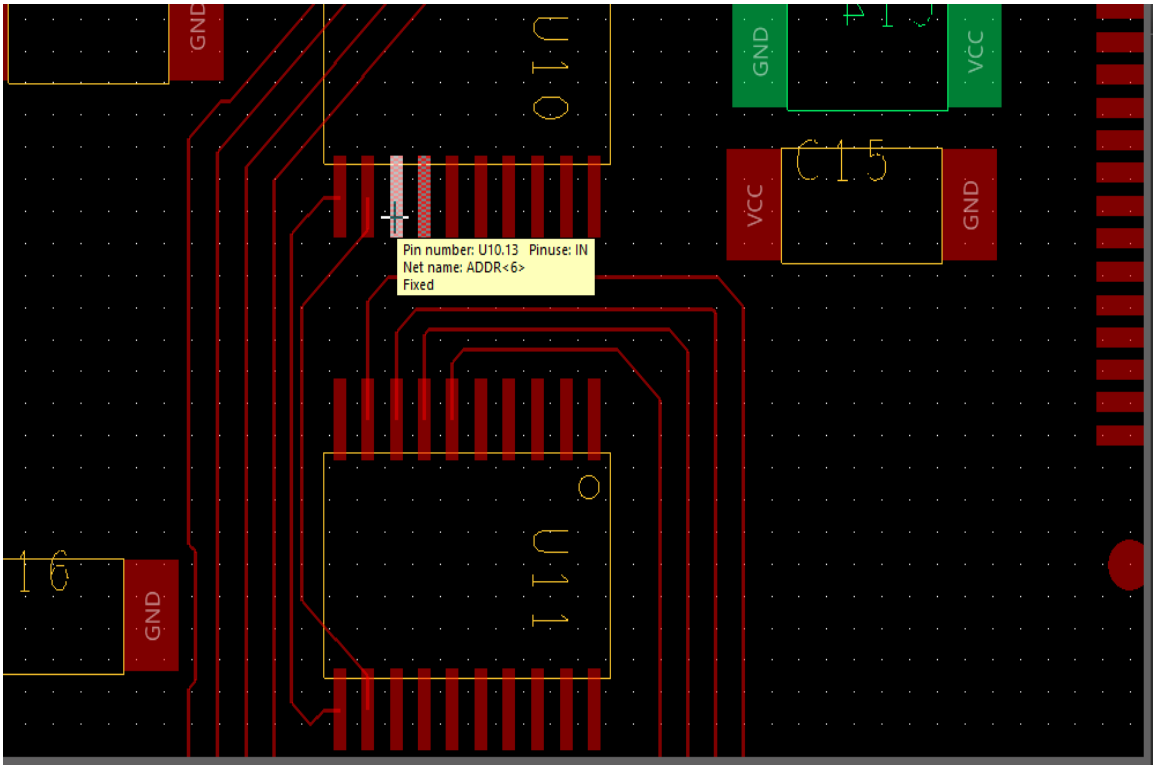
The *Constraint Hierarchy* section shows that nets *ADDR<3>* and *ADDR<2>* are elements of bus *ADDR*. The Net Class *ADDR_0_3* is assigned to both the nets. The *Resolved Spacing Constraints* section shows that the 12_MIL_SPACE constraint rule assigned to Net Class is followed by the nets.

13. Close the *Show Constraint* window and select *Done* from the right-click pop-up menu.

14. Close the Constraint Manager and save the layout in Allegro PCB Editor.

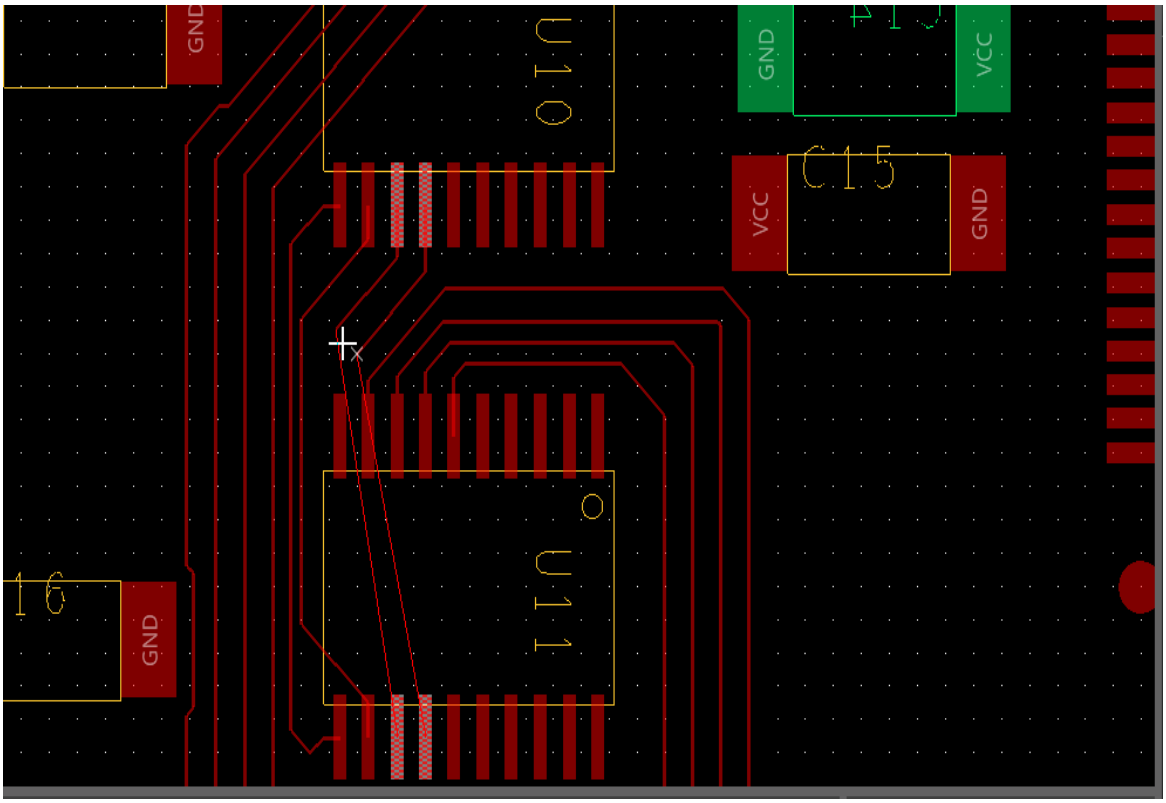
Routing with Net Class-Class

1. Select the pins with nets *ADDR<6>* and *ADDR<7>* on U10.

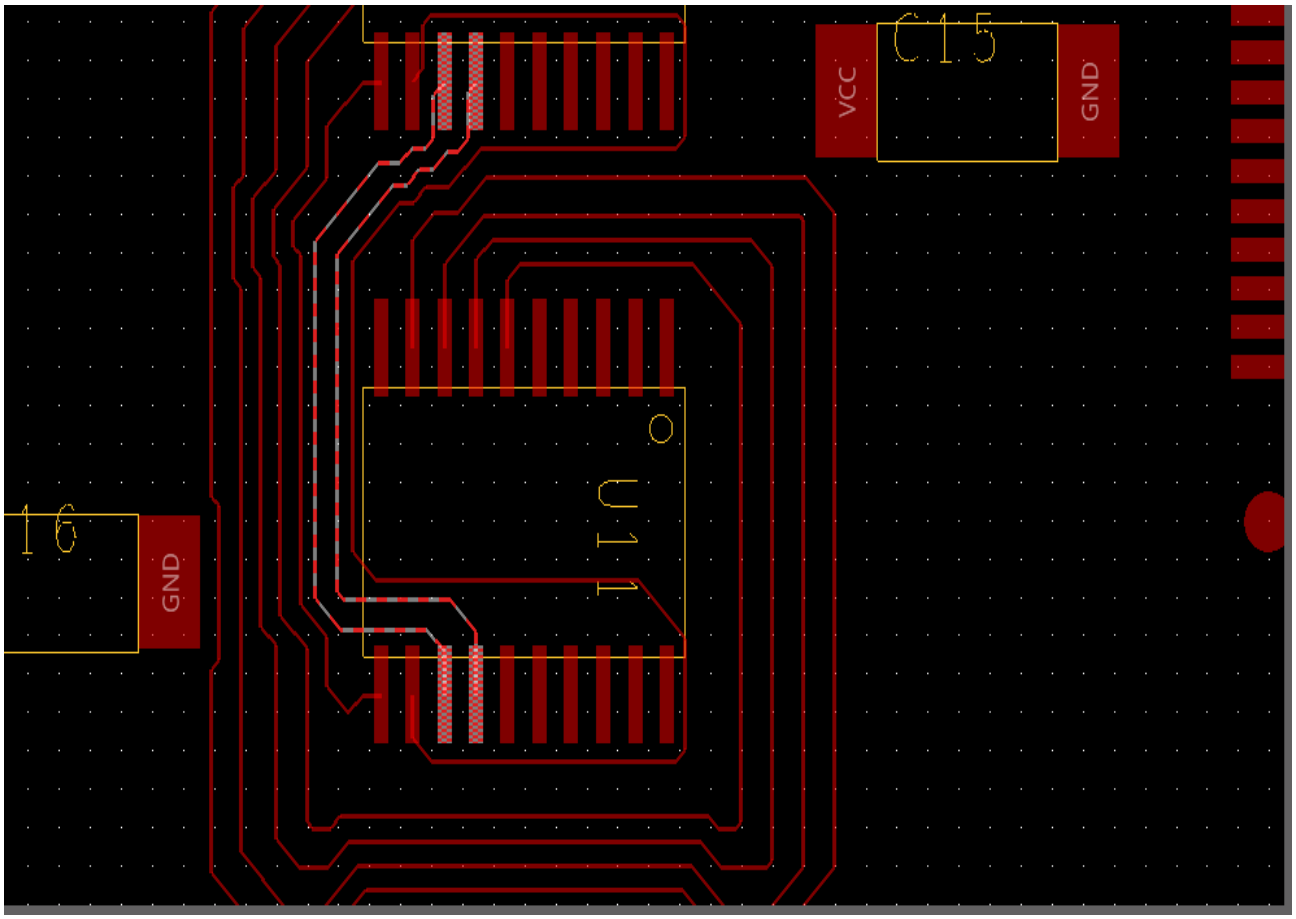


2. Choose *Route - Connect.*

Two lines are attached to the cursor.



3. Terminate the routes at nets *ADDR<6>* and *ADDR<7>* on U11.

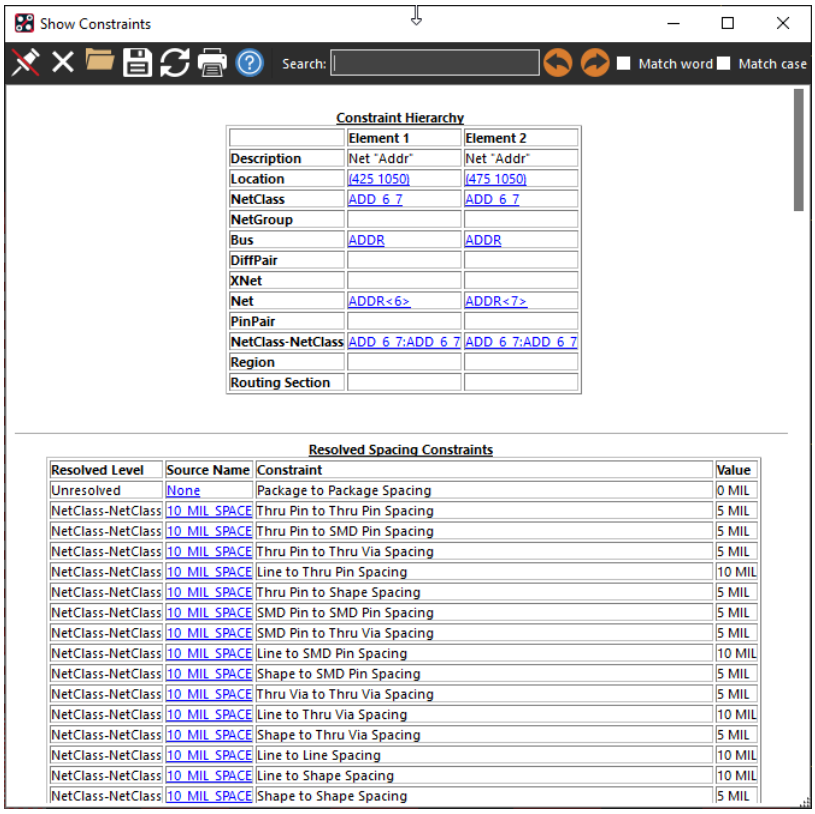


4. Right-click and select *Done* from the pop-up menu.

5. Choose *Display - Constraint* or from tool bar icon click the *Cns show* icon .

The *Show Constraint* window is displayed.

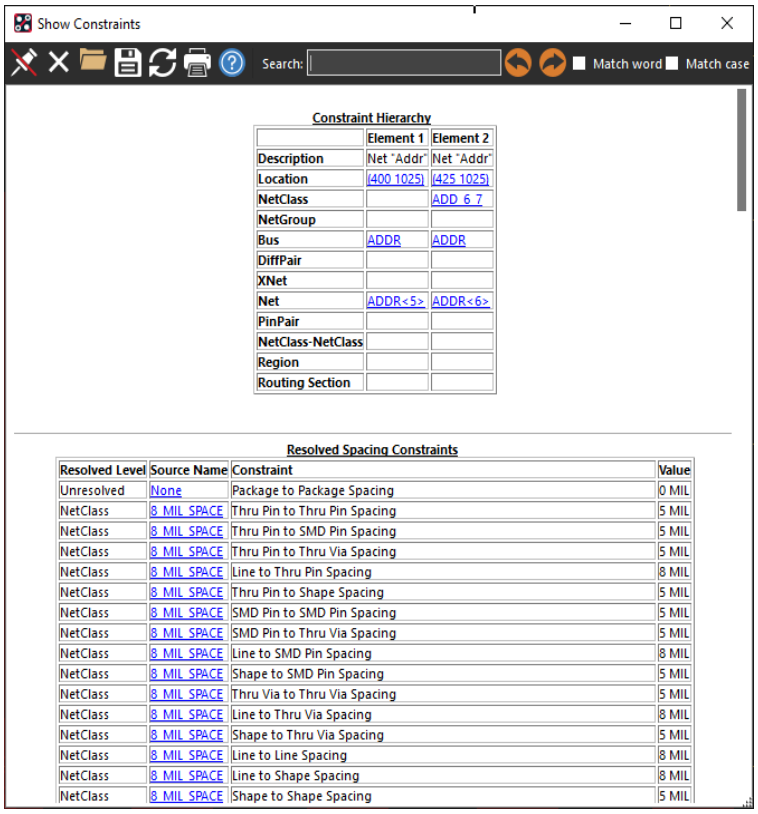
6. Select the nets *ADDR<6> and ADDR<7>.*



The *Constraint Hierarchy* section shows that nets *ADDR<6>* and *ADDR<7>* are elements of bus *ADDR*. The Net Class *ADDR_6_7* is assigned to both the nets. The *Resolved Spacing Constraints* section shows that the 10_MIL_SPACE constraint rule is followed by Net Class-Class relation between nets of the same Net Class.

7. Close the *Show Constraint* window.

8. Now, select the nets *ADDR<5> and ADDR<6>.*



The *Constraint Hierarchy* section hows that net *ADDR<5>* and *ADDR<6>* are elements of bus *ADDR*. The net *ADDR<6>* is a part of Net Class *ADDR_6_7*; whereas the net *ADDR<5>* is not a part of any Net Class. The *Resolved Spacing Constraints* section shows that the 8_MIL_SPACE constraint rule is followed. This rule is assigned to Net Class *ADDR_6_7* and is used for the nets that are not part of any Net Class-Class relation with Net Class *ADDR_6_7*.

Note: The nets that are not assigned to any Net Class use the Net Class constraint for a specific net which is the neighboring net with Net Class.

9. Close the *Show Constraint* window and select *Done* from the right-click pop-up menu.

Summary

You learned to create Spacing Constraint set for nets and net class. You also learned to route with these Spacing Constraints.

Recommended Reading

For more information about how Spacing Constraints are handled in Allegro Constraint Manager, see the *Constraint Manager User Guide*.