cadence®

R Commands

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Contents

1

R Commands

radial router	rail generator	ratbundle
rats all	rats blank	rats bundled blank_all
rats bundled show_all	rats component	rats end_inview
rats layer	ratsnest	rats net
rats outside partition	rats show	rats show_all unplanned
rats show unplanned	rats toggle	rats unbundled show_all
rd_stream	readme	readonly
record	recordmacro	redefine via structure
redisplay	redo	redraw
refdes	refresh_padstack	refresh_symbol
refresh_vs	refresh padstack	refresh symbol
refresh syminst	refresh via structure	reftxt
reject	relative copy	relative move
rename	rename area design	rename area list
rename area room	rename area window	rename execute
rename padstack	rename param	repeat_again

replace padstack	replace temp_devices	replace temp_symbols
replace via structure	replace via with structure	replay
report	reports	rep padstack
reset dockwindows	resizewindow	restore waived drc
restore waived DRC errors	return	rf_ac_assemble
rf_ac_delete	rf_ac_disassemble	rf_ac_init
rf_ac_setup	rf_add_component	rf_add_connect
rf_any_angle_bend	rf_autoplace	rf_break
rf_chamfer	rf_change	rf_cline_convert
rf_component2shape	rf_delete	rf_display_info
rf_display_newcomp	rf_flip	rf_group_add
rf_group_copy	rf_group_disband	rf_group_exclude
rf_group_info	rf_iff_export	rf_iff_import
rf_libxlator	rf_load_module	rf_manualplace
rf_measure	rf_modify_net	rf_padstack_export
rf_push	rf_quickplace	rf_scaled_copy
rf_setup	rf_shape2component	rf_single_segment_connect
rf_snap	rf_tapered_connect	rf_varedit
rfedit	rfedit_appm	rfplace
rfreplace_ripup	rfsip route	ripup etch

roam	room outline	rotate
route_by_pick	route priority	rplan blank
rplan blank_all	rplan bundled blank	rplan bundled blank_all
rplan bundled show	rplan bundled show_all	rplan bundled toggle
rplan commit	rplan convert	rplan convert spatial
rplan convert topological	rplan delete	rplan optimize
rplan plan	rplan plan accurate	rplan plan spatial
rplan plan topological	rplan progress	rplan show
rplan show_all	rplan status	rplan toggle
rplan unbundled blank_all	rplan unbundled show_all	rplan unbundled toggle
rpn	run	

radial router

The `radial router` command lets you choose a number of die pins and pull them out in a fanned pattern to increase the spacing between clines for better escape routes. The increased spacing makes it easier to automatically route the bond pads to the package pins for a wire bonded or TAB attached package.

A radial pattern for escape routes is necessary if the die pins are closer together than the package pins. You can control both the angle and the length of the escape routes in the radial pattern.

> ⓘ The command is available only with Allegro X Advanced Package Designer (APD).

When you select the radial router command, you can choose to do the following tasks from the *Options* panel:

- Set the subclass on which the radial lines are to be added

- Set the angle of the radial pattern

- Set the direction in which the radial pattern will emerge from the pins

- Set the width of the radial lines
  The default value is the specified minimum width of the active layer.

- Drag radial lines using the angle of the pins

Related Topics

- Increasing the Spacing Between Clines for Better Escape Routes

Radial Router Command: Options Panel

Access Using

- Menu Path: *Route – Router – Route Radial*

Active subclass	Choose a CONDUCTOR subclass on which the radial lines are to be added
Guide angle	Specify an integer from 10 to 90. The guide angle is determined relative to the route direction. The smaller the number, the sharper the angle. A value of 45 creates a guide angle shown in the example to the left. A value of 90 creates a flat guide angle.
Route direction	Specify the direction you want the guide angle to point.
Line Width	Specify the width of the clines. The default is the minimum line width specified for the active layer.
Align Clines with Pad Rotation	Enable this button to extend the line at the same angle as the pin or via to which it is connected.

Increasing the Spacing Between Clines for Better Escape Routes

To achieve automatic routing of bond pads to the package pins you may need to increase the spacing between clines to improve escape routes. Perform the following steps to increase spacing between clines:

1. Choose *Route – Router – Route Radial* or run `radial router` in the Command window.

2. Set the routing parameters in the *Options* panel.

3. Choose the die pins you want to route.

4. Move the cursor to the point that determines the length of the clines to route.
   A guide angle pattern follows the cursor.

5. Click to set the cline paths.
   The nets for the selected clines are automatically selected and highlighted for subsequent routing.

6. Finish the operation with one of the following menu choices: *Done* or *Finish*.

7. Click the right mouse button and choose *Done* to set the radial lines but not to complete the route.
   You can choose the same items later to finish the routing.

8. Click right and choose *Finish* to complete the routing.
   You can specify how the routing operation will be performed by invoking the Automatic Router by clicking right and choosing Route Setup before choosing *Finish*. For a picture of a completed routing from this operation, see Completed Route in the Sample Outputs section below.
   Any selected items that are not assigned to part pins (for example, those on a power or ground net) are not routed.

Sample Outputs

- Guide Angle: 70; Route Direction: Right; Align Clines with Pad Rotation: Off
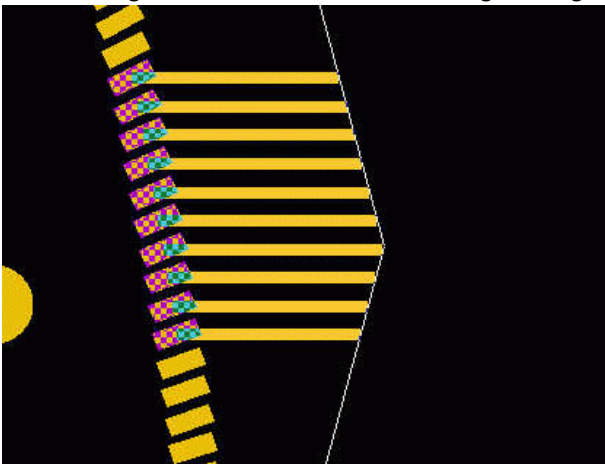
- Guide Angle: 50; Route Direction: Up; Align Clines with Pad Rotation: On
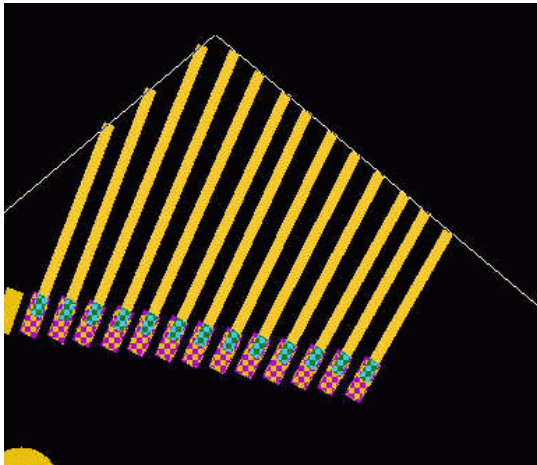
- Fanout Lines
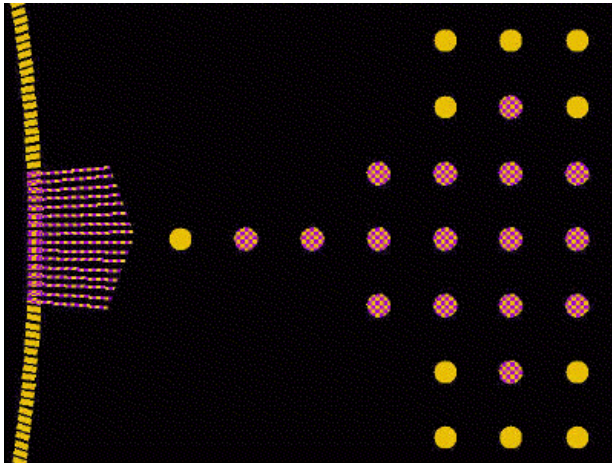
- Completed Route
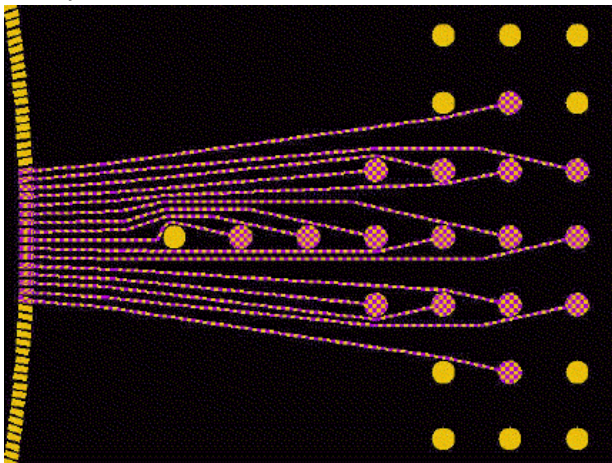
Related Topics

- radial router

rail generator

Creates IC style Power and Ground Rails (Stripes) and via arrays based on specified parameters through the layer stackup in alternating horizontal and vertical schemes across multiple power and ground domains.

⚠ Available when the *Silicon Layout* option is selected in Allegro X Advanced Package Designer (APD).

Power/Ground Rail Generator Dialog Box

Access using:

- Menu path: *Si Layout – Power Delivery – Rail Generator*.

Control	Description
Generate All	Click to generate complete sequence of power rail based on configuration.
Remove All	Click to remove last sequence of power rail.
Save All	Click to save the result of last sequence run.
Select Rail Boundary	Select a shape in the design to serve as the region in which to generate rails.
Rail Shape Setup	Creates Power and Ground rails for selected nets in an alternating horizontal and vertical scheme across multiple power and ground domains. Power and Ground nets must have Ratsnest Schedule and Voltage properties to be available for selection in the Rail Generator.
Create Dynamic Shapes	Select to create rails as dynamic shapes. Selected by default. If not selected, rails are created as static shapes.
Sequence	Sequence in the rail generation at which rail should be added. If empty, rail will not be created on the layer.
Layer	Specify the layer.
Style	Specify the style. Valid value can be *Vertical* or *Horizontal*.
Origin	Specify the origin of the rails Valid value can be *Left*, *Top*, *Center*, *Right*, *Bottom*, or *Custom*. *Center* is selected by default. *Top* and *Bottom* are available for Horizontal style and and are available for Vertical style. If you select *Custom*, the rail starts from the location you specify for *Start Coordinate* and expands in both directions.
Start Coordinate	Specify the origin of the rails if you choose *Custom* for Origin.

Net Sequence	Specify sequence of nets for rails on the layer as a list where each net is separated by a comma. The sequence starts with the first net in the list till the end in each direction. Right-click and choose Select to select Nets to be used for rails.
Space Sequence	Specify the space between rails as a list of values separated by comma. The sequence will be repeated till the end for each net in the list for that layer. You can specify a single value.
Width Sequence	Specify the width of the rails as a list in order of the nets. The sequence will be repeated till the end for each net in the list for that layer.
Generate Rails	Click to generate rails for the target region and the layers configured.
Remove Rails	Click to remove all rails from the active region and layers that are not fixed.
Stitching Via Setup	Creates Via arrays for overlapping Power and Ground rails created with the Power Delivery Rail Generator. Rail shapes must have *Generated Rail* property to run Stitching Via Setup.
Create individual vias for each hole	Select to create single hole vias. Selected by default. ⚠ Although this option provides flexibility by creating one hole per via, the size of the database and performance might be affected.
Sequence	Sequence in the rail via generation. If empty, rail will not transition between layer pair.
Layer	Name of dielectric layer. Top and bottom conductor layers, if unnamed.
Padstack	Specify padstack to use to create vias.
Hole Size	Specify the size of holes to be created in the dielectric layers. Holes are round by default.
Reference	Specify the reference point for via array placement. Valid value can be *Top Left*, *Top Right*, *Center*, *Bottom Left*, or *Bottom Right*.
Offset	Specify the offset from the reference.
Pitch XY	Specify the distance between the coordinates of centers of the via openings.
Adjacent Hole Spacing	Specify the space between holes in the layer and holes in the adjacent layers.
Array Size	Specify the row and column of vias to be placed in the initial pass.
Place Vias	Click to place vias as configured.
Remove Vias	Click to remove placed vias.

Import	Import spreadsheet to specify via configuration.
Export	Generate a spreadsheet that can be modified externally and then imported using the Import option. Import using *Simple* for a minimal configuration and using *Complete* for detailed editing.

ratbundle

The `ratbundle` command is used to select a bundle in the design by name via the command line. It can be used directly before or after certain commands that operate on the named bundle. For example, `bundle edit` to edit the named bundle, or `show element` to display information about the named bundle, and others.

Syntax

`ratbundle <bundle_name>`

Related Topics

- Editing Bundle

Displaying Bundle Information

Follow these steps to display bundle information:

1. In the console window, type `ratbundle` followed by the name of a bundle in the design. For example:

   `ratbundle bndl_5`
   The bundle highlights in the design canvas.

2. Run the `show element` command.
   Information about the named bundle is displayed in the Show Element window.

Editing Bundle

Follow these steps to edit bundles:

1. In the console window, type `ratbundle` followed by the name of a bundle in the design. For example:

   `ratbundle bndl_10`

   The bundle highlights in the design canvas.

2. Run the `bundle edit` command, then select rats in the design to add or remove from the named bundle.

Related Topics

- bundle edit
- bundle split
- ratbundle

R Commands
R Commands--rats all

rats all

The `rats all` command displays all existing ratsnest lines in a design.

To control the way in which the ratsnest lines are displayed, use them with the following commands:

color192	Controls the color of ratsnest lines.
property edit	Suppresses ratsnesting on an entire net, such as power or ground. Set NO_RAT on the Set Net dialog box.

To display ratsnest lines as straight or jogged lines, run the prmed command to launch the *Design Parameter Editor*, click the *Display* tab and set *Ratsnest Geometry.*

Access Using

- Menu Path: *Display – Show Rats – All*
- Toolbar Icon:

rats blank

The `rats blank` command hides the rat display of one or more selected objects associated with the route plan. The following objects are supported:

.

Object	Rats affected
Bundle	Rat members of the bundle.
Component or Symbol	Rats that terminate at the component or symbol.
Net	Rats in the net.

Access Using

- Menu Path: *Display – Blank Rats – Of Selection*

Hiding Rats Display of Selected Objects

Perform these steps to hide rats display of selected objects:

1. Set the application mode as Flow Planning.

2. Limit the find criteria to just one type of object by right-clicking in the design canvas, then choosing *Super filter – <object_type>* from the menu.

3. Select one or more objects associated with the route plan whose rats you want to hide.
   The selected objects highlight and also appear in the *WorldView* window.

4. Choose *Display – Blank Rats – Of Selection* or run `rats blank` in the Command window.
   The rats associated with the selected objects are hidden.

5. Repeat the above steps to hide the rat display of other objects as needed.

Related Topics

- Object Selection Shortcuts

- rats show

rats bundled blank_all

The `rats bundled blank_all` command hides the display of all bundled rats in the design.

Access Using

- Menu Path: *Display – Blank Rats – All Bundled Rats*

Hiding the Display of All Bundled Rats

Perform this step to hide the display of all bundled rats:

1. Choose *Display – Blank Rats – All Bundled Rats*.
   All bundled rats are hidden.

rats bundled show_all

The `rats bundled show_all` command displays all bundled rats in the design.

Access Using

- Menu Path: *Display – Show Rats – All Bundled Rats*

Showing All Bundled Rats

1. Choose *Display – Show Rats – All Bundled Rats.*
   All bundled rats appear.

Related Topics

- rats blank

rats component

The `rats component` command displays existing ratsnest lines attached to component pins.

To control the way in which the ratsnest lines are displayed, use them with the following commands:

color192	Controls the color of ratsnest lines.
property edit	Suppresses ratsnesting on an entire net, such as power or ground. Set NO_RAT on the Set Net dialog box.

To display ratsnest lines as straight or jogged lines, run the prmed command to display the *Design Parameter Editor*, click the *Display* tab and set *Ratsnest Geometry.*

Access Using

- Menu Path: *Display – Show Rats – Component*

Displaying Existing Ratsnest Lines Attached to Component Pins

To display existing ratsnest lines which are attached to component pins:

1. Choose *Display – Show Rats– Component* or run `rats component` in the Command window.

2. Select a component in the design canvas.
   Ratsnest lines to pins on the components that you choose are displayed.

rats end_inview

The rats end_inview command reduces the density of the rat display. This commands filtered out the rats from the display that are either pass-through or those not terminating to a pin in view.

Access Using

- Menu Path: *Display – Show Rats – End In View Only*

Displaying Rats of Selected Objects

To display rats of selected objects:

1. Pan to a section of design for viewing.

2. Choose *Display – Show Rats – End In View Only*.
   The pass-through rats are filtered out from the display.

rats layer

The `rats layer` command allows you to turn the display of rat lines on or off depending on the net's primary routing layer. You can also permanently highlight nets based on their primary routing layer.

Related Topics

- Displaying Rats by Layer

Rats Display by Layer Dialog Box

When you run the *rats layer* command, the *Rats Display by Layer* dialog box appears. You can change the following settings in the spreadsheet to define how you want the rats displayed.

Access Using

- Menu Path: *Display – Rats by Layer*

Column	Description
Layer Name	The name of the layer. Includes two special items: ○ *ALL LAYERS*: Changes made in this row will apply to all rows in the grid. ○ *UNASSIGNED LAYER*: Changes made here apply to nets which are not assigned a layer (when there is no `ASSIGN_ROUTE_LAYER` property). Otherwise, there is one row per conductor layer in the design, in order, top to bottom.
Rats	If enabled, the rats are displayed for this layer. Otherwise, they are turned off. The default setting is off, except for unassigned layers.
Highlight	If enabled, the rats assigned to this layer are highlighted in the color specified in the *Color* column. The default setting is off, except for unassigned layers.
Color	Indicates the color chosen to highlight the rats on this layer.

Active Color	Specifies the color that is active in the *Color Palette.*
Color Palette	Click the desired color from the palette. Then click the box in the *Color* column for the layers to which you are assigning this color. By default, the color matches the color that is assigned for conductor traces on this layer. For more information about assigning colors, see the description of the color192 command in Allegro PCB and Package Physical Layout Command Reference.

Command	Description
Update	Updates the database (and display) based on the settings shown in the spreadsheet. The dialog box remains displayed.
Clear	Restores the original highlighting that was configured before the `rats layer` command was executed.

Close	Closes the *Rats by Layer* dialog box and exits the command. The current display settings in the database are not changed.
Help	Invokes context-sensitive Help for this command.

Displaying Rats by Layer

⚠ The `rats layer` command is intended primarily for use after you run the `auto assign net` command. By using the `rats layer` command in this way, you can quickly gauge the routability of the solution derived from assigning the nets.

To display rats by layer, follow these steps:

1. Import the die/BGA components.

2. Assign layers to any nets that must go to a specific layer using the `assign routing layer` command.

3. Perform `auto assign net` from the die to package or package to die (depending on design flow).

   ⚠ Be sure to enable easi or use the constraint-driven algorithm so that the assign route layer properties are created on nets which were not assigned a layer in the previous step.

4. From the *Display* menu, choose *Rats by Layer* or type `rats layer` at the command prompt.
   The *Rats Display by Layer* dialog box appears.

5. Enable the highlighting and color assignments you want to apply to each layer of the design.

   ⊘ For best results, view the assignments one layer at a time. Define the highlight settings for a particular layer and click *Update* to see the assignments for that layer. Then repeat the process for each subsequent layer until you have the display the way you want it.

6. Click *Update* to refresh the display or click *Close* to dismiss the highlight settings and exit the dialog box.

Related Topics

- rats layer

ratsnest

The `ratsnest` command displays the Ratsnest dialog box for blanking (making invisible) or displaying specific ratsnest lines or groups of lines. A ratsnest line represents a connection as it exists prior to routing. Selections in the Ratsnest dialog box aid in the specification of critical component locations.

Related Topics

- Showing and Hiding Ratsnest in the Design

Ratsnest Dialog Box

Access Using

- Menu Path: *Display – Ratsnest*

Select By	*Net* controls the visibility of all ratsnest lines in the selected nets. *Component* controls the visibility of all ratsnest lines in each net connected to the selected component.
Net Filter	When you choose by *Net*, filters the nets displayed in the Net Name list box.
Net Name	When you choose by *Net*, lists the names of all selected nets.
Refdes Filter	When you choose by *Component*, filters components shown in the Refdes/Device list box by reference designation.
Device Filter	When you choose by *Component*, filters components shown in the Refdes/Device list box by device name.
Sort	When you choose by *Component*: *Refdes* sorts the components shown in the *Refdes / Device* list box by reference designation. *Device* sorts the components shown in the *Refdes / Device* list box by device name.
Refdes / Device	When you choose by *Component*, lists the selected components by reference designation and device name.
Select All	Changes all nets or everything in a component symbol to the color currently selected by way of the hilight command.
Show	Shows the ratsnest line or lines.
Hide	Hides the ratsnest line or lines.

Related Topics

hilight

Showing and Hiding Ratsnest in the Design

Controlling the display of ratsnest in a design can be done either by selecting nets or components. Do the following to show or hide selective ratsnest from a design:

1. Choose *Display – Ratsnest* or run `ratsnest` in the Command window.
   The *Display – Ratsnest* dialog box appears.

2. Set the *Select By* radio button on *Net* or *Component*.

3. Use the filter field to narrow the display of net or component names.

4. Click the *Show* or *Hide* radio button. Alternately, click the *Select All* button.

5. Click the name of the net or the component reference designator or device for the ratsnest you want to show or hide.
   The ratsnest associated with the selected net or component is hidden or shown in the design canvas.

6. Click OK to apply the setting and close the dialog box.

Related Topics

- ratsnest

rats net

The `rats net` command displays existing ratsnest lines attached to pins on a net.

To control the way in which the ratsnest lines are displayed, use them with the following commands:

color192	Controls the color of ratsnest lines.
property edit	Suppresses ratsnesting on an entire net, such as power or ground. Set NO_RAT on the Set Net dialog box.

To display ratsnest lines as straight or jogged lines, run the prmed command to display the *Design Parameter Editor*, click the *Display* tab and set *Ratsnest Geometry*.

Access Using

- Menu Path: *Display – Show Rats – Net*

Displaying Existing Ratsnest Lines Attached to Pins on a Net

To display existing ratsnest lines attached to pins on a net, follow these steps:

1. Choose *Display – Show Rats – Net* or run `rats net` in the Command window.

2. Choose a net.
   Ratsnest lines to pins on the nets that you choose are displayed.

rats outside partition

The `rats outside partition` command displays all the existing ratsnest lines outside the active partition when you are working with the Design Partition feature.

To control the way in which the ratsnest lines are displayed, use them with the following commands:

- color192: Controls the color of ratsnest lines.

- property edit: Suppresses ratsnesting on an entire net, such as power or ground. Set the NO_RAT property.

To display ratsnest lines as straight or jogged lines, run the prmed command to display the *Design Parameter Editor*, click the *Display* tab and set *Ratsnest Geometry.*

ⓘ This command is available only when the *PCB Team Design* option is selected.

Access Using

- Menu Path: *Display – Show Rats – Outside Partition*

Displaying All Ratsnest Lines Outside a Partition

Perform these steps to display all ratsnet lines outside a partition:

1. Once you have the Design Partition feature running, open the partitioned design (. `dpf,` `dps,` or . `dpm`).

2. Run the `rats outside partition` command.
   All ratsnest lines outside the partition appear.

rats show

The `rats show` command displays the rats associated with one or more selected objects. The following objects are supported:

Object	Rats affected
Bundle	Rat members of the bundle.
Component or Symbol	Rats that terminate at the component or symbol.
Net	Rats in the net.

Access Using

- Menu Path: *Display – Show Rats – Of Selection*

Displaying the Rats of Selected Objects

Follow these steps to display the rats of selected objects:

1. Set the application mode as Flow Planning.

2. Limit the find criteria to just one type of object by right-clicking in the design canvas, then choosing *Super filter – <object_type>* from the menu.

3. Select one or more objects associated with the route plan whose rats you want to hide.
   The selected objects highlight and also appear in the *WorldView* window.

4. Choose *Display – Show Rats – Of Selection* or run `rats show` in the Command window.
   The rats associated with the selected objects are displayed.

5. Repeat the above steps to show the display of rats of other objects as needed.

Related Topics

- Object Selection Shortcuts

- rats blank

rats show_all unplanned

The `rats show_all unplanned` command displays all rats in the design that have no route plan and hides all other rats. The rats displayed either were not planned or were left unconnected by the GRE route engine.

Access Using

- Menu Path: *Display – Show Rats – Unplanned Rats*

Related Topics

- rats show unplanned

Displaying all Unplanned Rats in the Design

Perform this step to display all unplanned rats in your design:

1. Choose *Display – Show Rats – Unplanned Rats*.
   Rats that were not planned or left unconnected by the GRE route engine are displayed and others are hidden.

rats show unplanned

The `rats show unplanned` command displays rats in the design that have no route plan and hides all other rats. The rats displayed either were not planned or were left unconnected by the GRE route engine. When objects (bundles, components, or symbols) are pre-selected, unplanned rats associated with the selection set are displayed and others are hidden. When nothing is selected, the command displays all unplanned rats in the design and hides all others.

The following objects are supported for selection:

Object	Rats affected
Bundle	Rat members of the bundle.
Component or Symbol	Rats that terminate at the component or symbol.

Related Topics

- rats show_all unplanned

Displaying Unplanned Rats Associated with Selected Objects

You can display unplanned rats associated with selected objects by following these steps:

1. Set the application mode as Flow Planning.

2. Limit the find criteria to just one type of object by right-clicking in the design canvas, then choosing *Super filter – <object_type>* from the menu.

3. Select one or more supported objects (bundles, components, or symbols).
   The selected objects highlight and also appear in the *WorldView* window.

4. With your cursor on a selected object, right-click and choose *Show Unplanned Rats* from the menu.
   Only associated rats that were not planned or left unconnected by the GRE route engine are displayed.

5. Repeat the above steps to display unplanned rats of other objects as needed.

Related Topics

- Object Selection Shortcuts

rats toggle

The `rats toggle` command lets you turn the display of all ratsnest lines in the design on or off.

Access Using

- *Menu Path:*
    - *Display – Show Rats – All*

    - or -

    - *Display– Blank Rats – All*

Toggling the Display of Ratsnest Lines in the Design

To toggle the display of ratsnest lines in your design:

1. Choose *Display – Show Rats – All or r*un the `rats toggle` command in the Command window.
   Ratsnest lines are displayed.

2. Run the command again.
   Ratsnest lines are turned off.

rats unbundled show_all

The `rats unbundled show_all` command displays all rats in the design that are not bundled.

Access Using

- Menu Path: *Display – Show Rats – All Unbundled Rats*

Displaying Unbundled Rats in the Design

1. Choose *Display – Show Rats – All Unbundled Rats*.
   All unbundled rats are displayed.

rd_stream

The r_{d_stream} batch command lets you takes a stream format file and output the data into standard ASCII text format. This ASCII view of the stream file is for display purposes only.

The *stream_file* (`.sf`) is the name of the stream file from which the ASCII text file is generated.

The `rd_stream` command produces an ASCII text file called `stream_file.txt` that can be displayed to identify the data that has been converted. Note that the file is an ASCII representation and cannot be used as input into any system that reads stream.

Syntax

```
rd_stream <input_file>
```

readme

The `readme` command displays the product notes for the currently running version of your Cadence tool.

readonly

The `readonly` command restricts modification of environment variables or their current values. System administrators can use this command in company-wide environment files to control users' ability to change certain environment variables.

Syntax

```
readonly <variable name>
```

Specify a variable to protect it from modification. If you enter no argument, a list of all current environment variables appears.

Example

To prevent users from changing `psmpath` or `padpath`, add the following to *<cdssite>*`/share/local/pcb/site.env`:

```
set psmpath = /myCompanySymbols


readonly psmpath


set padpath = /myCompanyPadstacks


readonly padpath
```

record

The `record` command records a script under a script name you specify. If you enter the command name without a script name, a file browser is displayed. The `record` command can be embedded in other scripts and can be nested up to five levels.

> ⚠ You can also activate script recording by way of the Scripting dialog box, displayed when you run script.

> ⊘ It is helpful to understand the difference between scripts and macros. Scripts are typically used to perform global tasks. For example, scripts can be used for setting up fields in forms, adding objects to multiple databases at the same location, and duplicating drawings. Macros are typically used to perform operations that need to be repeated on a board drawing. For example, macros can be used to repeat complex geometric operations.

Related Topics

- recordmacro
- replay
- scriptmode

Recording a Script

To record a script:

1. Type `record` in the Command window, followed by a script name.
   The script begins running.

2. When you want to end the recording, type `stop`

–or–

1. Type `record` with no argument in the Command window.
   A file browser is displayed.

2. Choose or enter a script name and click *Save*.
   The script begins running.

3. When you want to end the recording, type `stop`.

recordmacro

The `recordmacro` command records a macro under a name you specify. If you enter the command without argument, a file browser is displayed. The `recordmacro` command can be embedded in other scripts and can be nested up to five levels.

⚠ You can also activate script recording by way of the Scripting dialog box, displayed when you run script and choose macro mode.

⊘ It is helpful to understand the difference between scripts and macros. Macros are typically used to perform operations that need to be repeated on a board drawing. For example, macros can be used to repeat complex geometric operations. Scripts are typically used to perform global tasks. For example, scripts can be used for setting up fields in forms, adding objects to multiple databases at the same location, and duplicating drawings.

Related Topics

- replay
- scriptmode

Recording a Macro

To record a macro:

1. Type `recordmacro` in the Command window, followed by a macro name.
   The macro begins running.

2. When you want to end the recording, type `stop`

–or–

1. Type `record` with no argument in the Command window.
   A file browser is displayed.

2. Choose or enter a macro name and click *Save*.
   The macro begins running.

3. When you want to end the recording, type `stop`.

redefine via structure

The `redefine via structure` command selects a structure and updates definition of all placed instances to match the selected structure. If any property is added or removed from the structure, the command also updates the properties during the redefining process.

You can modify a structure by applying interactive commands to any of the objects that belongs to a structure. For example, `slide, move, rotate, mirror,` and `delete`.

Access Using

- *Menu Path: Route – Structures – Redefine*

Related Topics

- Redefining a Structure

Modifying a Structure

Perform these steps to modify a structure:

1. In *Find* filter, ensure that only *Symbols* is selected.

2. Hover the cursor over a structure and right-click to choose *Unlock to Edit* from the pop-up menu.

3. Choose *Route – Slide.*

4. Select a cline segment from the structure and slide to a different position.

5. Right-click and choose *Done* from the pop-up menu.

6. Hover the cursor over the modified symbol and right-click to choose *Lock Via Structure* from the pop-up menu.
   The definition of the structure has changed.

Redefining a Structure

Follow these steps to redefine a structure:

1. Run `redefine via structure` or choose *Route – Structures – Redefine.*

2. Click to choose a modified structure. The command window displays following message:

   Structure definition <structure_name> redefined.
   A confirmer dialog box is displayed.

3. Click *Yes* to refresh all instances to match new definition.
   Properties modified are updated when redefining structures.

4. Right-click and choose *Done* from the pop-up menu.

Related Topics

- redefine via structure

redisplay

The `redisplay` command updates and redraws the current design window.

Related Topics

- redraw

redo

The `redo` command reapplies the results of the most recent action reversed with undo. You can reapply a series of interactive operations that were reversed with `undo` by repeating this command. Redo-enabled commands are used to edit physical database entities such as lines, vias, shapes, voids, pins, components, etc.

When you click the *Redo* toolbar icon as shown below, a history of commands used in the current session appears, which lists the most recent actions that can be reapplied using `redo`. The most recently used command appears at the top of the history: The program reapplies it first when you execute `redo`. The *Redo* toolbar icon grays out when no commands are available to be reapplied.
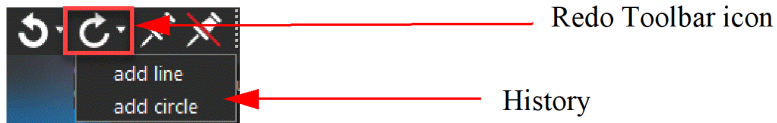
Access Using

- Menu Path: *Edit – Redo*

- Toolbar Icon:

Reapplying the Most Recent Actions Using the Redo Command

To reapply the most recent action using the redo command:

1. Choose *Edit – Redo* or run `redo` in the Command window.

   The last operation undone is reapplied. (If you choose a command from the history, all commands above the selected command are reapplied.)

2. Repeat step one as many times as required to reapply other operations in the reverse order that they were undone.

redraw

The redraw command refreshes the work area.

Access Using

- Menu Path: *View – Refresh*

- Toolbar Icon:

Related Topics

- redisplay

refdes

The `refdes` command is used in conjunction with an active command. It lets you find/choose a component when you type in the command followed by the object's reference designator.

Finding a Component

1. With a command active, type `refdes` followed by a reference designator at the command console prompt of your user interface.
   The component is selected or found, based upon the command that is active.

Example

1. Run the `place manual` in the Command window.

2. Type `refdes U1` at the console command prompt.
   The component specified is selected for placement from the list of components in the Placement dialog box.

refresh_padstack

The `refresh_padstack` batch program lets you read library padstacks from an existing design and ensures that the design contains the most recent version of the padstacks in the library. You can also run this program interactively from your user interface using refresh padstack.

Syntax

`refresh_padstack <input_design> <output_design>`

Entering only the output filename updates all of the padstacks in the design. If you want to restrict the padstacks that are refreshed, use the following syntax:

`refresh_padstack [-l <padfile>] <input_design> <output_design>`

-l <padfile>	Refreshes only the padstacks that are identified in the padstack list file that you created. The <*padfile*> variable specifies the list file that contains the names of the padstacks that you want to refresh. The padstack list is an ASCII text file that has a `.lst` file extension.
-version	Prints the version.
input_design	Specifies the name of the design file whose padstacks you want to update. The editor assumes the `.brd` extension if you do not provide it.
output_design	Specifies the output design file to contain the updated padstacks. The editor adds the `.brd` extension if you do not provide it. If you do not provide the *output_design* argument, `refresh_padstack` puts the output in *input_design*.

Related Topics

- *Updating a Library Padstack in a Symbol*

Reading Library Padstacks from an Existing Design

Perform the following steps to read library padstacks from an existing design:

1. Enter `refresh_padstack` from an operating system prompt.

   You are prompted to enter an existing design filename.

2. Enter the filename.

   You are prompted to enter an output filename. This file is written to the current working directory unless otherwise specified.

refresh_symbol

The `refresh_symbol` batch command reads symbols from an existing design and ensures that the design contains the most recent version of the symbols in the library.

The `refresh_symbol` command does not reload padstacks from the library. To do this, use the Padstack Editor. Because `refresh_symbol` does not rip up etch/conductor, a pin moved to a new location in the library symbol might result in dangling etch/conductor. Also, the command does not replace pin escapes attached to symbols. If you choose a symbol with pin escapes from a library, the pin escapes can land on top of those from a previous symbol. This can cause multiple drill holes in the same location if the pin escapes contain vias. DRC violations can occur if merging etch/conductor from the previous symbols. Do not refresh symbols with pin escapes.

Any repositioned symbol text is maintained. The `refresh.log` file, located in the current working directory, records `refresh_symbol` processing.

Syntax

`refresh_symbol [`*`switch`*`] [-version]<`*`input_design`*`> [<`*`output_design`*`>]`

switch	If you do not provide a switch option, processing refreshes all symbols. These are the switches:
-a	Refreshes all symbol types.
-p	Refreshes package/part symbols only.
-b	Refreshes mechanical symbols only.
-o	Refreshes format symbols only.
-h	Refreshes shape and flash symbols only.
-f	Same as `-o`.
-m	Same as `-b`.
-g	Refreshes STEP mapping data only for package and mechanical symbols.
-k	Refreshes the padstacks from library used by package and mechanical symbols.
-K	Preserves design padstacks on pins.
-s|l <list file>	Refreshes only symbols identified in the symbol list text file that you created. The *symfile* is the name of the list file.

-t	Resets text locations in symbols to that of the library symbol. By default, text locations in the board are preserved.
-d	Refreshes customizable drill data of the padstack. Used when symbols are updated using -k switch.
-e	Resets pin escapes (fan outs). Loads pins escapes defined for a symbol in library and deletes design pin escapes.
-x	Ripup etch connected to symbol pins.
-z	Ignores the FIXED property, allowing replacement of symbols "fixed" in the design.
-version	Prints the version.
<input_design>	Specifies the name of the design file whose symbols you want to update. The editor assumes the .brd extension if you do not provide it.
<output_design>	Specifies the output design file, into which the updated symbols are placed. The editor adds the .brd extension if you do not provide it. If you do not provide the *output_design* argument, refresh_symbol puts the output in *input_design*.

Examples

The following examples suggest uses for refresh_symbol:

- To refresh all mechanical and package symbols in the design named input and stores the results in the file named output

  refresh_symbol -b -p input output

- To refresh all mechanical, package, format, and pad shape symbols in the design named input and stores the results in the file named output .

  refresh_symbol input output

- To refresh all mechanical symbols, plus any symbols (other and package) referred to in the file named symbols.lst in the design named input and stores the results in the file named output .

  refresh_symbol -b -s symbols.lst input output

Related Topics

- Updating Libraries to Convert Units of Measure for Symbolsrefresh_symbol

Updating Symbols in the Design

Follow these steps to update symbols in your design:

1. Enter `refresh_symbol` from an operating system prompt.

   You are prompted to enter an existing layout filename.

2. Enter the filename.

   You are prompted to enter an output filename. This file is written to the current working directory unless otherwise specified.

   To update specific symbols, symbol types, or symbol padstacks, follow the syntax conventions.

Updating Libraries to Convert Units of Measure for Symbols

If refreshing symbols relocates pins, use the following procedure:

1. Choose *Display – Status* (status command). The Status dialog box's Status Tab appears.

2. Disable *On-Line DRC.*

3. Choose *Shape – Change Shape Type* (shape change type command) to change all shapes to static solid and disable your dynamic shapes.

4. Run refresh_symbol.

5. Choose *File – Save* to save the design.

6. Choose *File – Import Logic* (netin command). The Import Logic dialog box appears.

7. Disable *Allow etch removal during ECO.*

8. Choose *Tools – Derive Connectivity* (derive connectivity command) to add etch/conductor to reconnect the clines to the pins.

9. Change planes to dynamic by choosing *Shape – Change Shape Type*.

10. Update your shapes' Dynamic Copper Fill mode to *Smooth* by choosing *Shape - Global Dynamic Params* (shape global param command). On the Global Dynamic Shape Parameters Dialog Box's Shape Fill Tab, click *Update to Smooth*. Or, on the Status Dialog Box's Status Tab, click *Update to Smooth.*

11. Choose *Display – Status* and enable *On-Line DRC.*

Related Topics

- refresh_symbol
- refresh_symbol

refresh_vs

The `refresh_vs` batch command lets you update the structures in your design to agree with the current library definitions of those structures.

Before running `refresh_vs`, remember the following conditions of the command:

- New structure definitions that you use to refresh old ones must have a starting element that can connect to the original structure's parent item.

- You cannot refresh a non-structure symbol instance with a structure definition.

- You can override the fixed property attachment to refresh a structure in a tile.

- When you refresh an old structure instance with an updated definition, you must replace all the instances of that via in the design.

- The `.xml` or `.exml` file of the current library definition must be present in $PADPATH.

Syntax

`refresh_vs <source_design> <destination_design>`

Entering only the output filename updates all of the structures in the design. If you want to restrict the structures that are refreshed, use the following syntax:

`refresh_vs [-l <.lst> -f] <source_design> <destination_design>`

-l <.lst>	Refreshes only the structures that are identified in the structure list file that you specify. The <.lst> variable specifies the list file that contains the names of the structures that you want to refresh. The structure list is an ASCII text file that has a `.lst` file extension.
-f	Lets you refresh structures that contain the FIXED property attachment. If you do not use this option, structures with a FIXED property attachment are not refreshed.If you do not use this option, even structure definitions that contain only individual elements with a FIXED property attachment will remain unrefreshed.
source_design	Specifies the name of the design file whose structures you want to update.
destination_design	Specifies the output design file to contain the updated structures. If you do not provide the *destination_design* argument, `refresh_vs` puts the output in *source_design*.

refresh padstack

The `refresh padstack` command lets you update the padstacks in your design to agree with the padstacks in your library.

When you choose this command, the Refresh Padstacks dialog box appears. This dialog box lets you update all of the padstacks in your design or only those padstacks that you specify in a padstack list. You can also run this program in batch mode as refresh_padstack.

Related Topics

- Updating Padstacks in the Design

Refresh Padstacks Dialog Box

Access Using

- Menu Path: *Tools – Padstack – Refresh*

Refresh All Padstacks	Indicates you want all padstacks in the design updated to agree with the library padstacks.
View Log	Displays the `refresh_padstack.log` file.
Padstack List	Indicates you want to update only the padstacks in the named list to agree with the library padstacks. The padstack list is an ASCII text file that has a `.lst` file extension. Click ... to display an Open browser window from which you can choose the Padstack List filename.
Reset Customizable Drill Data	Choose to update or refresh drill customizable data fields in the Drill Customization spreadsheet (*Positive/Negative Tolerance, Symbol Figure, Symbol Characters*, and *Symbol Size X/Y*) during subsequent updating or refreshing of padstacks. "Customizable drill data" is all the padstack data that can potentially be modified within the Drill Customization spreadsheet. This includes *Positive Tolerance, Negative Tolerance*, *Symbol Figure*, *Symbol Characters,* and *Symbol Size* X/Y. If this field is not enabled, subsequent updating or refreshing of padstacks deletes any changes previously made to these customizable fields in the Drill Customization spreadsheet. This option is disabled by default to prevent accidental loss of customized padstack drill information. Refreshing will not update any of the padstack data that could have been modified within the Drill Customization spreadsheet unless you enable this option. In order to refresh all of the padstack data, including the tolerances and drill figure, you must enable *Reset Customizable Drill Data*. Otherwise, the tolerances will not be updated from the library. If you have added padstack tolerances to your library, an older board design from your archive will contain the original padstacks without tolerances. You must enable *Reset Customizable Drill Data* when refreshing the padstacks or the tolerances will not be refreshed in the legacy board. ⚠ The layout editor does not mark padstacks that may have been modified in any way. Drill customization may have updated a padstack, or you may have modified them using the Padstack Editor.
Refresh	Updates the padstacks you chose with the latest library files and generates the `refresh_padstack.log` file.
Close	Closes the Refresh Padstack dialog box and ignores any input.

Updating Padstacks in the Design

To update padstacks in your design, follow these steps:

1. Choose *Tools – Padstack – Refresh or* Run `refresh padstack` in the Command window.
   The Refresh Padstack dialog box appears.

2. Choose the padstacks to update with the latest library files.

   > ⚠ You must enter the name of a list file if you want to update padstacks from a list.

3. Click *Refresh* to update your padstacks.

4. Click *View Log* to view the `refresh_padstack.log` file, which is generated in the current working directory each time you update your padstacks.

Related Topics

- refresh padstack

refresh symbol

The `refresh symbol` command is the interactive version of the batch command refresh_symbol, which reads symbols from an existing design and ensures that the design contains the most recent version of the symbols in the library.

The `refresh symbol` command does not reload padstacks from the library. To do this, use the Padstack Editor. Because `refresh symbol` does not rip up etch/conductor, a pin moved to a new location in the library symbol might result in dangling etch/conductor.

Use this command to replace new flash symbols in the database with new versions from the disk. Then choose the definitions for update and update the symbol padstacks.

Any repositioned symbol text is maintained. Note that components within a module can be updated independently of the module in which they reside.

The `refresh.log` file, located in the current working directory, records `refresh_symbol` processing.

Related Topics

- Updating Symbols in Your Design

Update Symbols Dialog Box

In the placement edit application mode, access the *Update Symbols* dialog box by right-clicking anywhere in the design canvas to display the *Quick Utilities* pop-up menu and choose *Refresh Symbol.*

Access Using

- *Place – Update Symbols* (in Layout mode)

- *Tools – Update Symbols* (in Symbol mode)

Select definitions for update	Choose one or more symbols from the tree view. **Note:** Place replicate modules are those created with the suite of place replicate commands and are differentiated from traditional modules, which are driven by the REUSE_MODULE property definition.
Enter a file containing a list of symbols	To update a symbol from a list, enter the name of a list file or click the browse button to find the file.
Update STEP mapping data only	Update STEP mapping information for package and mechanical symbols.
Keep design padstack names for symbol pins	Preserves design padstack on symbol pins.
Update symbol padstacks from library	The padstacks in the design are updated with those found in the library. For details on updating unassociated library padstacks, see *Updating Layout Padstacks* your product documentation.
Reset Customizable Drill Data	Choose to update or refresh drill customizable data fields in the Drill Customization spreadsheet (*Positive/Negative Tolerance, Symbol Figure, Symbol Characters*, and *Symbol Size X/Y*) during subsequent updating or refreshing of padstacks. If this field is not enabled, subsequent updating or refreshing of padstacks deletes any changes previously made to these customizable fields in the Drill Customization spreadsheet.
Reset symbol text locations and size	The symbol text and size is reset as it is defined in the symbol definition as opposed to how it is defined in your design, if different.

Reset pin escapes (fanouts)	Reset predefine pin escapes from the symbol.
Ripup Etch	Etch associated with symbol pins is removed during refresh symbol.
Ignore FIXED property	Replace a symbol to which the FIXED property has been assigned.
Viewlog	Displays a log file containing errors and warnings.

Updating Symbols in Your Design

To update symbols in your design, follow these steps:

1. Run `refresh symbol`.

   The Update Symbols dialog box appears.

2. Choose the symbols you want to update/refresh. –or– To choose a symbol list file, enter the list name in the box or click the browse button to locate the list file.

3. Check the options you want.

4. Click *Refresh*.

Related Topics

- refresh symbol

refresh syminst

The refresh syminst command lets you refresh the symbol instance that is already placed on the board. This command restores the data related to the symbol. For example, the silkscreen outline or text. You can access this command from the pop-up menu in the *Placement Edit* application mode.

> ⚠ This command however, does not refresh the symbol in the library.

refresh via structure

The `refresh via structure` command lets you update the structures in your design to agree with the current library definitions of those structures.

When you choose this command, the Refresh Structures dialog box appears. This dialog box lets you update all of the structures in your design or only those structures that you specify in a structure list. You can also run this program in batch mode as refresh_vs.

Before using `refresh via structure`, remember the following conditions:

- New structure definitions that you use to refresh old ones must have a starting element that can connect to the original structure's parent item.

- You cannot refresh a non-structure symbol instance with a structure definition.

- You can override the fixed property attachment to refresh a structure. By default, a fixed structure will not be refreshed.

- When you refresh an old structure instance with an updated definition, you must replace all the instances of that structure in the design.

- The `.xml` or `.exml` file of the current library definition must be present in $PADPATH.

- New structure definition does not preserve the properties attached to the old structure.

Related Topics

- Refreshing Via Structures in a Design
- refresh_symbol

Refresh Structures Dialog Box

Access Using

- Menu Path: *Route – Structures – Refresh*

Ignore Fixed Property	When checked, this option lets you refresh structures that contain the FIXED property attachment. The default condition of this option is unchecked. **Note:** Left unchecked, even structure definitions that contain only individual elements with a FIXED property attachment will remain unrefreshed
Structures to refresh	
Structure list	When checked, lets you browse for a list of design structures to update with the current library definitions of the same structures. The structure list is an ASCII text file that has a `.lst` file extension.
Select from the following list	When checked, lets you update only the design structures in the *Refresh* list to agree with the XML structures. Structures that you leave or move into the *Ignore* list are not updated.
Refresh (list)	Lists the design structures you want to refresh from their current library definitions. You can move individual structures into the *Ignore* list by clicking on the structure name.
Ignore (list)	Lists the design structures you do not want to refresh. You can move individual structures into the *Refresh* list by clicking on the structure name.
Ignore All >>	Lets you move all the structures into the *Ignore* list.
<< Refresh All	Lets you move all the structures into the *Refresh* list.
View Log	Displays the `refresh_structure.log` file.
Refresh	Updates the structures you chose with the latest library files and generates the `refresh_structure.log` file.
Close	Closes the Refresh Structures dialog box and ignores any input.

Refreshing Via Structures in a Design

To refresh via structures in your design, perform these steps:

1. Run `refresh via structure`.
   The Refresh Structures dialog box appears.

2. Check *Ignore Fixed Property* if you want to refresh structures that contain the FIXED property attachment.

3. Choose the structures to update with their current library definitions in one of the following manners:
   From an ASCII text list

   a. Click *Structure list*.

   b. Enter or browse for the name of a list file containing the structures you want to update.

   From structures in your design or XML

   a. Click *Select from the following list.*
      All the structures in your design appear in the *Refresh* list.

   b. Click on individual structures you do not want to refresh. They move into the *Ignore* list.

4. Click *Refresh* to update the selected structures.

5. Confirm your intent to refresh the structures.

   ⓘ You cannot undo the act of refreshing the structures once you choose *Yes* from this dialog box.

6. Click *View Log* to view the `refresh_structure.log` file, which is generated in the current working directory each time you update your structures.

7. When you have completed refreshing the selected structures in your design, click *Close* to exit the command.

Related Topics

- refresh via structure
- refresh_symbol

reftxt

The `reftxt` batch command reads in a text file that renames existing reference designators in a layout design.

This program is different than the automatic rename program (rename param) that may be available within your product. The `reftxt` command lets you rename any number and type of reference designators simultaneously, and apply new ones with any number of characters. If you plan to change to lengthy designators, make sure your symbols have been built with reference designator placement that accommodates them.

Related Topics

- Sample reftxt.log File
- Error Messages in the reftxt.log File
- Running the Batch Rename Reference Designator Command

The reftxt.log File

The `reftxt` program creates a log file named `reftxt.log`, which contains the following information:

- A header with the start time and date, name of input text file, name of the existing drawing being processed, name of new drawing created

- A list of all reference designator name changes that were made

- Any errors or warnings detected

- Final statistics of counts of the numbers of errors, warnings, and successful reference designators names that were changed

- Ending time and date

Related Topics

- Error Messages in the reftxt.log File

- Running the Batch Rename Reference Designator Command

Sample reftxt.log File

```
(          RENAME BY TEXT FILE            )

(            )

(          Drawing    : smdemo.brd            )

(          Date/Time  : Thu Mar 15 13:10:56 2003            )

...............

Input rename text file: rename_sample.txt

Drawing to be saved: changed.brd

*WARNING: The old and new names in the following line are the same: Z3 Z3

This line will be ignored

*NOTE: Refdes Z5 changed to Z1

*NOTE: Refdes Z1 changed to Z2

*NOTE: Refdes C18 changed to C1

*NOTE: Refdes C13 changed to C2

...............

Total number of error messages: 0

Total number of warning messages: 1

Total number of successful renames: 39
```

```
Termination Date/Time: Thu Mar 14 13:10:57 2003
```

Related Topics

- reftxt

- Running the Batch Rename Reference Designator Command

Error Messages in the reftxt.log File

If any of the following errors occur, the errors are reported in the log file and the output drawing is not saved:

- An input file cannot be opened
- An output file cannot be created
- A syntax error exists in the input rename file
- A corruption exists in the design database
- An old reference designator that does not exist in the design is listed in the input rename file
- A new reference designator that already exists and has not been renamed in the rename file
- More than one rename specified for the same reference designator
- More than one old reference designator being renamed to same new name

A reference designator on a component with the HARD_LOCATION property is being changed

Syntax

```
reftxt rename_file design_name [output_name] [-version]
```

rename_file	Specifies a text file that contains a "was/is" list of reference designator changes, one per line.
design_name	Specifies the name of the layout to be changed.
output_name	Is an optional field that specifies the name to assign the layout after it is changed. If not specified, the original layout name is kept and the database is overwritten.
-version	Prints the version.

Related Topics

- reftxt
- The reftxt.log File
- refresh_symbol

Running the Batch Rename Reference Designator Command

Follow these steps to run the batch rename reference designator command:

1. Create a text file that lists the existing and new reference designators. For example, `rename_sample.txt`:

   25 Z1

   Z1 Z2

   Z3 Z3

   .....

   C18 C1

   C13 C2

   C17 C3

2. At the command line, type the `reftxt` command and identify the text file, the old drawing, and the new drawing as follows:

   reftxt *rename_file old_drawing* [*new_drawing*]

   The following is an example command line entry and the subsequent processing activity that occurred:

   reftxt rename_sample.txt smdemo.brd changed.brd

   Input rename file: rename_sample.txt

   Drawing to be opened: smdemo.brd

   Drawing to be saved: changed.brd

   *** Drawing saved successfully

Related Topics

- reftxt
- The reftxt.log File
- refresh_symbol
- Sample reftxt.log File

reject

The `reject` command lets you deselect and dehighlight an element(s) selected during the current interactive command, continues the find process at the same location selected, and highlights the next element found.This command is also available on the pop-up menu.

Use the `reject` command to choose the element you require when it is too near or directly superimposed over other elements that you do not want to have selected by the interactive command.

relative copy

The `relative copy` command creates copies of various elements (arc, circle, rectangle, frectangle, line, and text) that are relative to a line. These copies are a mirror image of the original element. You can set the direction and the angle of rotation for the relative line in the *Options* panel.

Related Topics

- Using the Relative Copy Command

Relative Copy Command: Options Panel

Access Using

- *Menu Path: Manufacture – Drafting – Relative Copy*

Relative mode	Controls the line around which the element is mirrored. The choices are: *Horizontal Line, Vertical Line, and Odd Line.* By default, *Horizontal Line* is selected*.*
Rotation type	Specifies the mode of rotation. The choices are: *Absolute*, and *Incremental*. Absolute: to read the number entered in the *Rotation angle* field as the angle at which to rotate the element. Incremental: for dynamic control over turning the element. Use the number entered in the *Rotation angle* field as the amount by which to increment each rotation. This option is disabled for *Horizontal Line,* and *Vertical Line* modes*.*
Rotation angle	Specifies the angle of rotation. In Incremental mode, this field specifies the number of degrees comprising each increment as you dynamically rotate the element. In Absolute mode, this field specifies the angle of rotation from the 0,0 orientation when the command is executed and the layout editor rotates the element immediately to that angle. Type a number between 0 and 360 or choose an option from the pop-up menu. Choose from 0, 45, 90, 135, 180, 225, 270, and 315. This option is disabled for *Horizontal Line,* and *Vertical Line* modes*.*

Using the Relative Copy Command

To create copies of elements relative to a line:

1. Choose *Manufacture – Drafting – Relative Copy* or run the `relative copy` command.

OR

1. Set *General Edit* application mode and select an element. Right-click and choose *Drafting – Relative Copy.*

2. Select an element.

3. Click to choose an origin point.
   A rubber band line is attached to the cursor with origin as the first end point and a possible copy of the selected element is also dynamically visible.

4. Click a point to place a copy of the element.
   A mirrored image of the selected element is created at the specified location.

5. Right-click and choose *Next* to continue or *Done* to complete the operation.

Related Topics

- relative copy

relative move

The `relative move` command moves different types of elements (arc, circle, rectangle, frectangle, line, and text) to a new location that is relative to a line. You can set the direction and the angle of rotation for the relative line in the *Options* panel.

Related Topics

- Moving Elements Relative to a Line

Relative Move Command: Options Panel

Access Using

- *Menu Path: Manufacture – Drafting – Relative Move*

Relative mode	Controls the line around which the element is moved. The choices are: *Horizontal Line, Vertical Line, and Odd Line.*
	By default, *Horizontal Line* is selected.
Rotation type	Specifies the mode of rotation. The choices are: *Absolute*, and *Incremental*. Absolute: to read the number entered in the *Rotation angle* field as the angle at which to rotate the element. Incremental: for dynamic control over turning the element. Use the number entered in the *Rotation angle* field as the amount by which to increment each rotation. This option is disabled for *Horizontal Line,* and *Vertical Line* modes.
Rotation angle	Specifies the angle of rotation. In Incremental mode, this field specifies the number of degrees comprising each increment as you dynamically rotate the element. In Absolute mode, this field specifies the angle of rotation from the 0,0 orientation when the command is executed and the layout editor rotates the element immediately to that angle.
	Type a number between 0 and 360 or choose an option from the pop-up menu. Choose from 0, 45, 90, 135, 180, 225, 270, and 315. This option is disabled for *Horizontal Line,* and *Vertical Line* modes.

Moving Elements Relative to a Line

To move elements relative to a reference line:

1. Choose *Manufacture – Drafting – Relative Move* or run the `relative move` command.

OR

1. Set *General Edit* application mode and select an element. Right-click and choose *Drafting – Relative Move.*

2. Select an element.

3. Click to choose an origin point.
   A rubber band line is attached to the cursor with origin as the first end point and a copy of the selected element is also dynamically visible.

4. Click a point where the element is to be moved.
   The selected element is moved to the specified location.

5. Right-click and choose *Next* to continue or *Done* to complete the operation.

Related Topics

- relative move

rename

The `rename` command lets you rename your design file. This command is similar to the `save_as` command, but not identical.

Renaming Your Design

Follow these steps to rename your design:

1. Type `rename`, followed by a new filename, at the command console prompt.

   The file is renamed. If the filename you entered as an argument already exists in the same location, a confirmer window is displayed. You can save your file with an existing name if you provide a path to a different location.

2. Run `save` to write the file to the new name.

rename area design

The `rename area design` command lets you automatically rename every component on a design in a single operation. When you run the command, it sets the automatic rename mode to RENAME OF ENTIRE BOARD and sets the rename area as the design extents.

Access Using

- *Menu Path: Logic – Auto Rename Refdes – Design*

Renaming Components in Your Design

1. Type `rename area design` at the command console prompt of your user interface.

rename area list

The `rename area list` command displays the LIST AREA dialog box showing the current automatic reference designator rename mode and the areas for renaming.

Access Using

- *Menu Path: Logic – Auto Rename Refdes – List*

rename area room

The `rename area room` command lets you designate a room for automatic reference designator renaming. When you run this command, it sets the automatic rename mode to RENAME BY ROOM with the room you designated as the active room.

Access Using

- *Menu Path: Logic – Auto Rename Refdes – Room*

Designating a Room for Automatic Reference Designator Renaming

To designate a room for automatic reference designator renaming:

1. Run `rename area room`.

   The Room browser appears, which lists rooms defined in the design (using the add rect command).

2. Select a room name from the list and click *OK*.

rename area window

The `rename area window` command lets you define an area for automatic reference designator renaming by making two diagonal selections. When you run the program, it sets the automatic rename mode to RENAME BY WINDOW with the coordinates of the window you selected.

Access Using

- *Menu Path: Logic – Auto Rename Refdes – Window*

Designating an Area for Automatic Reference Designator Renaming

Follow these steps to designate an area for automatic reference designator renaming:

1. Enter two diagonal clicks in the design, designating the window area to be renamed.

2. Click right to display the pop-up menu and click *Done*.

rename execute

The `rename execute` command automatically renames reference designators as defined by the parameters set on the Rename RefDes dialog box. The command performs the same function as the *Rename* button in the Rename RefDes dialog box when you run rename param.

Renaming reference designators can also be accomplished by creating a text file and running the reftxt command in batch mode. In a single text file you can indicate changes anywhere on the design. There is no limit to the number of characters in a reference designator contained in this file.

The text file is a "was/is" list. Each line describes one reference designator to be changed, followed by at least one space or tab and the reference designator that is to be substituted. Reference designators can be listed in any order. Previous ones do not affect those further down the list.

The rename batch command `reftxt` can also be used to accommodate reference designators that might otherwise be too long for the automatic rename function. For example, the `reftxt` command can be used to change reference designators to include part numbers or other company-defined information. If you plan to change to lengthy reference designators, make sure that your symbols have been built with reference designator placement that accommodates them.

Automatically Renaming Reference Designators

1. Type `rename execute` at the command console prompt of your user interface.
   A message appears on the status line stating that the automatic renaming of reference designators is in progress. The command displays status information during processing. When it completes, the command displays a message showing the number of components that were renamed.

rename padstack

This command allows you to change the name of existing padstacks in a design. This command changes the following for the changed padstack name; all references in constraint via lists; all via, bond finger, and pin references to the padstack; and stored name mappings.

⚠ The `rename padstack` command will not update the `.pad` file in your library. If you are updating the padstack for a symbol pin, the definition will be updated as well. As a result, a refresh of symbols on that drawing would reset it to the original name, as the library symbol would need to be manually updated.

Related Topics

- Renaming a Padstack

Rename Padstack Command: Options Panel

Access Using

- *Menu Path: Tools – Padstacks – Rename (APD)*

Existing padstack	Select the padstack you want to change. Lists all the padstacks in the design in alphabetical order. By default, the first padstack is shown.
New name	Specify the new name for the selected padstack. By default, shows the existing name of the selected padstack.
Rename Padstack	Changes the name of the padstack across the design.
	The *Options panel* also displays the *Start layer* and *End layer* information of the padstack being renamed.

Renaming a Padstack

To rename a padstack:

1. Choose *Tools – Padstack – Rename*

2. Select the existing padstack name from the *Existing padstack* list.
   If you select a padstack before accessing the Rename option, the existing name will be selected, by default.

3. Specify a new name in the New name box.

4. Click *Rename Padstack*.
   The padstack name is changed and the references to the padstack are updated in Constraint Manager.

Related Topics

- rename padstack

rename param

The `rename param` command automatically renames every component on a design in a single operation. Renaming is performed on both sides of the board.

Reference designator renaming is controlled by placement grid line locations only or by sequential renaming within grid blocks. You can control both the direction (horizontal or vertical) and the order (left-right, right-left, up-down) of the renaming process. You can define grid descriptions either alphabetically or numerically. You also can edit grid descriptions to fit renamed components.

When you run `rename param`, the Rename Ref Des dialog box appears. On this dialog box you can specify whether you want to use the default grid or define your own grid.

You also can choose to rename individual components by attaching the AUTO_RENAME property to them.

Related Topics

- Renaming All Reference Designators from the Rename Refdes Dialog Box
- Attaching the AUTO_RENAME Property

Rename Param Dialog Boxes

Access Using

- *Menu Path: Logic – Auto Rename Refdes – Rename*

Rename RefDes

Use this dialog box to specify whether you want to use the default grid or define your own grid for renaming the components in a design in a particular pattern (Left to right, top to bottom and so on. You can choose to rename all components or to attach the AUTO_RENAME property to individual components.

User Defined Grid	Lets you specify the grid by choosing *Place – Autoplace – Top Grids* (place set topgrid) command or *Place – Autoplace –Bottom Grids* (place set bottomgrid) command.
Use Default Grid	Uses the default (or sequential) grid, which constitutes an internal method of renaming components. This is the non-etch grid set in the *Define Grid* form. It consists of a single grid block sized the same as the design outline, used in conjunction with the pattern (left to right, top to bottom, etc.). Choosing this option does not override any grid you may have defined.
Rename ALL Components	Renames all the components on both sides of the design
Attach Property Components	Renames specific components in your design. Use the Find filter to find the components you want to attach the AUTO_RENAME property too. You use both the Find By Name/Property Form and Edit Property Form in this process.
More	Displays the Rename Ref Des Set Up dialog box on which you set all the reference designator parameters.
OK	After you have set all other options, executes the Rename function.
Close	Closes the dialog box.
Cancel	Cancels the operation.

Rename Ref Des Setup

Use this dialog box to set parameters to control the renaming.

Layer Options

Layer	Specifies the layer on which you want to rename the reference designators. You can choose from Top/Surface, Bottom/Base, or Both (default).Note: If you checked the Rename ALL Components on the Rename Ref Des dialog box and choose either the Top/Surface or the Bottom/Base layer, then the renaming does not affect the unselected layer.
Starting Layer	Specifies the layer on which renaming begins. You can choose from Top/Surface (default) or Bottom/Base. This field is active when you choose Both in the Layer field.
Component Origin	Specifies an origination point on the component. You can choose from Pin1, Body Center (default), or Symbol Origin.

Directions for Top(Surface)/Bottom(Base) Layer Options

You can set the direction and order for the layer specified in the Layer field. For example, if you Top/Surface in the Layer field, the directions for the Bottom/Base layer are grayed out.

First Direction	Specifies either horizontal or vertical to set the initial direction by which components are renamed. The Ordering field options change depending on the First Direction field. For example, if you choose horizontal as the first direction the default ordering is right to left then downwards. If you choose vertical, the default ordering is then right to left.
Ordering	Specifies the order that the components are renamed.
Left to Right	Always renames the components in a row from the left side to the right side.
Right to Left	Always renames the components in a row from the right side to the left side.
Downwards	Always renames the components in a column from the top to the bottom.
Upwards	Always renames the components in a column from the bottom to the top.

Reference Designator Format Options

RefDes Prefix	Specifies the prefix of the reference designator you want to rename. Use uppercase alphabetic characters for the prefix. The default value is an asterisk (*).Use the default value (*) if you want to rename the reference designators and store the prefix in that components symbol definition. Any prefixes based on component instance and component definition are overwritten. When *Preserve current prefixes* is not selected, the value defined in the package symbol (R*, C*, U*…) is used as the prefix value. If *Preserve current prefixes* is selected, then the prefix values used are the ones already defined in the logic (and may include any suffixes).

Top(Surface)/ Bottom(Base) Layer Identifier	The default is T for Top/Surface and B for Bottom/Base. The character is appended to each new reference designator on the appropriate layer.
Skip Character(s)	Specifies the characters you want to skip during Grid Based renaming. The specified value is used during grid row and column assignment by excluding certain characters. Default values are I, O, and Q.
Renaming Method	Specifies Sequential (default) or Grid Based.

Preserve current prefixes	Keeps the current prefix during renaming of reference designators. If you defined the Top or Bottom Layer identifier field, the editor appends that letter to the current prefix. If this field is not selected, parts annotate sequentially and use the prefix defined in the symbol footprint. The Symbol Prefix must be defined with letter and star (R*, C*, U*...). If this field is selected, prefixes and suffixes defined in the Packager setup or generated according to the subdesign suffix in module design are preserved. If the prefix pattern is ($PHYS_DES_PREFIX)[0-9], then the $PHYS_DES_PREFIX part will be used as the preserved prefix. If the pattern is more complex, ($PHYS_DES_PREFIX)[0-9]_{$PAGE}, then the prefix includes the ($PHYS_DES_PREFIX) in the beginning and the _{$PAGE} at the end. The increment number [0-9] renumbers. For example, a reference designator of R23_2 (where R is the resistor prefix, and _2 is the page), might renumber to R1_2 if the part is placed in the upper left. The 23 changes to 1. Only the number portion of the reference designator renumbers. For subdesigns, the subdesign suffix (as assigned by the Packager) also appends to the end of the reference designator string. Prefix extraction: All <chars> before the last number in the RefDes are taken as the prefix. ('-' preceding a digit is considered a part of the number). For example:

RefDes	Prefix Identified§	Renumbered as§
C1	C	Cnnn§
R1	R	Rnnn§
CR1	CR	CRnnn§
U1A2	U1A	U1Annn§
<alpha>*	<alpha>	<alpha>nnn§
<alpha>22-34	<alpha>	<alpha>nnn§
<alpha>2-2DS	<alpha>	<alpha>nnn§
A-Z34	A-Z	A-Znnn§
CR46A32FF	CR46A	CR46Annn //<chars> before last num§
<alpha>	""	nnn§
4324	""	nnn§
num<alpha>	""	nnn§

Sequential Renaming Options

Refdes Digits	Specifies the number of digits to be used in renaming components. You can choose from 1, 2, 3, 4, or 5. If you choose 3 digits, for example, the components are renamed 001, 002 This field is grayed out if you choose Grid Based as the Renaming Method.

Grid Based Renaming Options

This section is grayed out if you choose Sequential as the Renaming Method.

1st Direction Designation	Row/column position of the first assigned reference designator. The default is A.
2nd Direction Designation	Row/column position of the first assigned reference designator. The default is 1.
Suffix	Specifies an alphanumeric character to be used as a suffix to differentiate between two or more components that occupy the same grid location. The default is 1.

Related Topics

- Attaching the AUTO_RENAME Property

Renaming All Reference Designators from the Rename Refdes Dialog Box

Perform these steps to rename all reference designators from the Rename Refdes dialog box:

1. Run `rename param` to display the Rename RefDes dialog box.

2. Specify a grid type.

3. Check *Rename all components*.
   If you do not want to rename all the components in your design, you must assign the AUTO_RENAME property to specific elements, as described in Attaching the AUTO_RENAME Property.

4. Set up the controls.

5. Click *Close* to close the RefDes Set Up dialog box and save the settings.

   ⚠ *Cancel* closes the dialog box without saving any of the changes. *Reset* returns the settings to their previous values.

6. Click *OK* in the Rename Ref Des dialog box to run the rename function.

Related Topics

- rename param

Attaching the AUTO_RENAME Property

When you run the rename process on an individual component or on one group of components at a time, you must define the components to be renamed by attaching the AUTO_RENAME property to them individually.

When you are renaming groups of reference designators, there may be certain components that you do not want to include in the renaming process. To prevent these components from being renamed, attach the HARD_LOCATION property to them.

To attach the AUTO_RENAME property to a component in the design, follow these steps:

1. In the Rename Ref Des dialog box, click *Attach Property - Components*.

2. Click the Find filter in the control panel. Make sure *Comps* is checked. (You may turn off all other elements if you want.)

3. Choose *Comp* (or *Pin*) in the *Find By Name* box of the Find filter.

4. Click *More*. The Find By Name/Property dialog box appears.

5. Choose one or more components from the list, using one of the following methods:

    ○ Click on one or more components in the Available Objects list box

    ○ Enter a component name or a component prefix followed by an asterisk in the Name Filter box, then click *All->*.

    The components appear in the Selected Objects list box.

    ⚠ Some components contain more than one prefix character. If you want to rename only components with a specific prefix (for example, C), make sure you filter out components that may have CA, CB... etc. reference designators.

6. Click *Apply*.
   The selected components are highlighted in the design window, and the Edit Property dialog box and Show window are displayed.
   The property and its value appear in the right area of the dialog box.

7. Click *Apply*.
   The AUTO_RENAME property is attached to the component(s), as indicated in the Show window.
   After executing the rename process, the AUTO_RENAME property is removed from each successfully renamed component.

Related Topics

- rename param

- Rename Param Dialog Boxes

repeat_again

The `repeat_again` command is used to create a continually running script, typically for demonstration purposes.

Replaying a Script Multiple Times

Follow these steps to replay a script multiple times:

1. Run record followed by your script name.

2. Type repeat_again as the last action of your script.

3. Run stop to finish recording.
   When you replay the script, `repeat_again` causes it to "loop" back to its starting point.

4. To stop replaying the script, click the *Stop* button in the Status window of your user interface.

replace padstack

The `replace padstack` command lets you replace an existing padstack with a new padstack. When you choose this command, the *Options* panel of the user interface is reconfigured for the command. The controls let you set the padstacks and other parameters that govern the replacement process. The `replace padstack` feature also lets you replace single vias when you choose the single via replace option.

To replace flash symbols in the database with new version from the disk, choose *Place – Update Symbols* (refresh symbol command)

Related Topics

- Replace Padstack Command: Options Panel

- Replacing Padstacks/multiple Vias

- Replacing Single Vias

Replace Padstack Command: Options Panel

Access Using

- *Menu Path: Tools – Padstack – Replace*

Old Padstack	Identifies the padstack that is to be replaced.
New Padstack	Identifies the name of the new padstack. If this padstack does not already exist in the design, it is loaded. Choose your padstack library.
Symbol Name	Identifies the name of the symbols whose padstacks are to be replaced. You can use a wildcard in this field to indicate more than one type of symbol. The default value is an asterisk (*).
Pin Number	Indicates the number of the pins whose padstacks are to be replaced. You can use a wildcard in this field to indicate multiple pin numbers. The default value is an asterisk (*) to indicate that any pin number is acceptable.
Ref Des	Specifies the reference designator of the components whose padstacks are to be replaced. You can use a wild card in this field to indicate multiple reference designators. The default value is an asterisk (*) to indicate that any reference designator is acceptable. The combination of Old Padstack, Symbol Name, Pin Number, and Ref Des values identifies the padstacks that are to be replaced. Only padstacks that match the values in all of these field options are modified. For example, if Ref Des is U22 and Pin Number is 5, only the padstack on pin number 5 of component U22 are changed. If Ref Des is U*2 and Pin Number is *3, the padstacks of a group of pins (such as U12.3, U12.13, U22.3, and U22.13) are changed.
Net Name	Indicates the name of the net whose padstacks are to be replaced.
Replace	Executes the Replace Padstack command using the values that you set in the preceding field options, and performs DRC.
Reset	Clears any values that you entered in the control fields.

Related Topics

- Replacing Single Vias

Replacing Padstacks/multiple Vias

To replace padstacks or multiple vias together, follow these steps:

1. Run `replace padstack`.
   The *Options* panel is reconfigured to display the controls for replacing the padstack.

2. In your design, choose the padstack that you want to replace. You can also type in, or browse for, the name of the padstack that you want to replace.
   The name of the selected padstack appears in the Old Padstack field.

3. Choose the padstack with which you want to replace the old padstack, or type in the name of the new padstack in the New Padstack field.
   The name of the edited padstack appears in the New Padstack.

4. Click *Replace*.
   The padstack is replaced.

5. Repeat steps 2 through 4 for each padstack that you want to replace.

6. If you want to cancel the entries you have selected or entered in the fields, click *Reset*.

Related Topics

- replace padstack

Replacing Single Vias

To replace a single via:

1. Run `replace padstack`.
   The *Options* panel is reconfigured to display the controls for replacing the padstack.

2. In your design, choose the via that you want to replace. You can also type in, or browse for, the name of the padstack containing the via that you want to replace.
   The name of the selected padstack appears in the Old Padstack field.

3. Check the Single via replace mode check box.

4. Choose the via with which you want to replace the old via. You can also type in, or browse for, the name of the new padstack containing the replacement via.
   The name of the edited padstack appears in the New Padstack.

5. Click *Replace*.
   The padstack is replaced.

6. Repeat steps 2 through 4 for each padstack that you want to replace.

7. If you want to cancel the entries you have selected or entered in the fields, click *Reset*.

Related Topics

- replace padstack
- Replace Padstack Command: Options Panel

replace temp_devices

The `replace temp_devices` command displays the Replace Temporary Devices dialog box that lets you replace any temporary devices created in Allegro PCB SI with information from your product library. The library browser dialog box also appears to help you find the correct information.

Related Topics

- Replacing Temporary Devices Created In Allegro PCB SI With Information from Your Product Library

Replace Temporary Devices Dialog Box

Access Using

- *Menu Path: Place – Replace SQ Temporary – Devices*

Temporary device info

Name	Indicates the name of the Allegro PCB SI temporary device you highlight from the complete list. This device is replaced when you choose one from your product library.
Pin count	Indicates the number of pins associated with the device.

Replacement device info

Name	Indicates the name of the product device you are replacing the Allegro PCB SI temporary device with.
Execute	Click to replace the device highlighted with the one you have chosen.
Print	Click to print the device information. You can choose to print to a file, the printer, or to a script.

Library Browser

File Filter	Indicates the search pattern for filtering files. This field is automatically set to *.txt*.

Replacing Temporary Devices Created In Allegro PCB SI With Information from Your Product Library

Follow these steps to replace a temporary device in your design:

1. Run `replace temp_device`s.

   The Replace Temporary Devices dialog box appears along with a Library Browser.

2. Click the device you want to replace in the *List of Temporary Devices from Allegro SI*.
   The name and pin count is echoed in the *Temporary device info* section of the dialog box.

3. Type the name of the replacement device in the *Name* box. –or– Click the device name in the library browser.

4. Click *Execute* to replace the temporary device and update the drawing. You can continue to replace other temporary devices. –or– Click *OK* to replace the temporary device, update the drawing, and exit the dialog box.

Related Topics

- replace temp_devices

replace temp_symbols

The `replace temp_symbols` command displays the Replace Temporary Symbols dialog box that lets you replace any temporary symbols created in Allegro PCB SI with information from your product library. The library browser dialog box also appears to help you find the correct information.

Related Topics

- Replacing Temporary Symbols Created In Allegro PCB SI With Information from Your Product Library

Replace Temporary Symbols Dialog Box

Access Using

- *Menu Path: Place – Replace SQ Temporary – Symbols*

Temporary symbol info

Name	Indicates the name of the Allegro PCB SI temporary symbol you highlight from the complete list. This symbol is replaced when you choose one from your product library.
Pin count	Indicates the number of pins associated with the symbol.

Replacement symbol info

Name	Indicates the name of the product symbol you are replacing the Allegro PCB SI temporary symbol with.
Execute	Click to replace the symbol highlighted with the one you have chosen.
Print	Click to print the symbol information. You can choose to print to a file, the printer, or to a script.

Library Browser

File Filter	Indicates the search pattern for filtering symbol files. This field is automatically set to *.psm*.

Replacing Temporary Symbols Created In Allegro PCB SI With Information from Your Product Library

Perform these steps to replace temporary symbols from your design:

1. Run `replace temp_symbols`.

   The Replace Temporary Symbols dialog box appears along with a Library Browser.

2. Click the symbol you want to replace in the *List of Temporary Symbols from Allegro SI*.
   The name and pin count is echoed in the *Temporary symbol info* section of the dialog box.

3. Type the name of the replacement symbol in the *Name* box. –or– Click the symbol name in the Library Browser.

4. Click *Execute* to replace the temporary symbol and update the drawing. You can continue to replace other temporary symbols. –or– Click *OK* to replace the temporary symbol, update the drawing, and exit the dialog box.

Related Topics

- replace temp_symbols

replace via structure

The `replace via structure` command lets you replace some or all instances of an existing structure with a new structure. When you choose this command, the *Options* panel of the Control Panel is reconfigured, letting you set the parameters that govern the replacement process. The `replace via structure` command also lets you override structures that have a FIXED property attachment.

Before running the `replace via structure` command, keep in mind the following conditions of the command:

- New structures that replace old ones must have a starting element that can connect to the original structure's parent item.

- Replacing a structure with a new one having an identical name is not allowed. Use `refresh symbol` command instead.

- You can override the FIXED property attachment to replace a structure.

- Based on the settings you entered in the *Options* panel, if one or more selected instances of a structure definition cannot be replaced in the design, the operation fails to replace any of them.

- If you replace multiple structures, you can undo only the last structure that you replaced. To reverse multiple replacements, right-click and use the *Cancel* option in the pop-up menu.

- New structure definition does not preserve the properties attached to the old structure.

Related Topics

- Replacing Structures

Replace Via Structure Command: Options Panel

Access Using

- *Menu Path: Route – Structures – Replace*

Ignore Fixed Property	When checked, lets you replace structures that contain the FIXED property attachment. The default setting is unchecked. If you replace a structure that has the FIXED property attached, the new structure will also have the FIXED property.
Structure names	
Old	Identifies the structure in the database that you want to replace. You can type the name of the structure in the field, pick it from the design, or click the *Browse* button. The *Browse* button opens a database/library browser from which you select the structure that you want to replace. **Note:** You must specify a database structure in this field. Library structures are not accepted.
New	Identifies the structure that you want to use for the replacement. You can type the name of the structure in the field, pick it from the design, or click the *Browse* button. If this structure is not in the design database, you must load one from the library of structure `.xml` or `.exml` files on disk. **Note:** If the new structure name is present in both the design database and the library, the structure from the database replaces the old structure.
Assign return path net	Choose to assign a net for return path via. Only available if high-speed via structures selected as new structure has return path connections identified.
Selection Method	Choose either *Window Selection or Manual Filter.*
Window Selection	Click this button to use *Window Selection*. Use window drag to select the structures or Right-click and choose *Temp Group* from the pop-up menu. In the design, pick the instances of structure to be replaced. Then right-click and choose *Complete* from the pop-up menu. When you use window drag, only the structures that are partly inside the window and are instances of the *Old Structure* are selected and replaced. Instances of other structure definitions that exist in the window are not replaced.
Net	To further limit the replacement of structure instances to one or some nets, use the net browser (…) to select the net name, or type the net name in the *Net* field. You can use a wildcard in this field to indicate more than one net or use the asterisk (`*`) default value that represents all nets in the design. The asterisk (*) represents one or more characters. Examples such as `*s, s*, t*s` are legal.

Manual Filter	*Click this button to use the four fields to filter out the structure instances to be replaced.*
Symbol	Identifies the name of one or more symbols connected to the structure that you want to replace. You can type the symbol name in the field or pick it from the design. You can use a wildcard in this field to indicate more than one symbol or use the asterisk (*) default value that represents all symbols in the design. For example, if the structure you are replacing contains six instances that connect to pins on devices of type DIE1 and DIE2, you can enter *1 in this field to replace only the structure connections to instances of DIE1.
Ref Des	Specifies one or more component reference designators connected to the structure that you want to replace. You can type the name of the reference designator in the field or pick it from the design. You can use a wildcard in this field to indicate more than one reference designator or use the asterisk (*) default value that represents all reference designators in the design. For example, if your selected *Ref Des* is U22, only the structure on component U22 is changed. If your selected *Ref Des* is U*2, the structures of a group of reference designators (such as U12, U22, U32, and U42) are changed.
Pin #	Indicates the number of one or more pins connected to the structure that you want to replace. You can type the pin number in the field or you can pick it from the design. You can use a wildcard in this field to indicate more than one pin or use the asterisk (*) default value that represents all pins in the design. For example, if your selected pin number is 5, you change only the structure on pin number 5 of the selected design element (symbol/RefDes). If your selected pin number is *3 on *RefDes U12,* you change the structure of a group of pins on the selected reference designator (U12.3, U12.13, and so on).
Net	Indicates the name of the net connected to the structure that you want to replace. You can type the name of the net in the field, pick it from the design, or use the net browser (...) to select a name. You can use a wildcard in this field to indicate more than one net or use the asterisk (*) default value that represents all nets in the design.
Replace	Executes the command using the values that you set in the preceding field options, and performs DRC. This option is enabled only after you have specified old and new structure names for replacement.
Reset	Clears any values that you entered in the control fields.

Replacing Structures

Follow these steps to replace structures in your design:

1. Run the `replace via structure` command.
   The *Options* panel of the Control Panel displays the controls for replacing the structure.

2. In your design, pick the structure that you want to replace. You can also type in, or browse for, the name of the structure that you want to replace in the *Old* (tructure name) field.
   The selected structure is highlighted and its name appears in the text box.

3. In your design, pick the structure with which you want to replace the old structure. You can also type in, or browse for the name of the new structure in the *New* (structure name) field.
   The selected structure is highlighted and its name appears in the text box.

4. Choose either *Window Selection* or *Manual Filter* as a selection method.
   If you choose *Window Selectio*n:

   a. To select the instances of structure to be replaced, either use window drag or right-click and choose *Temp Group* from the pop-up menu.

   b. To further limit the replacement, type a net name in the Net field or use the browser (...) to select the net.

   If you choose *Manual Filter*, pick the symbol, RefDes, pin, and net connected to the structure you want to replace, or type the names of these elements in the appropriate fields. Note that you must pick in this order. The command sets up the *Find Filter* selection so that you must pick in the order stated. Alternatively, you can use the asterisk (*) default value that represents all noted element types present in your design.

5. Click *Replace*.
   The structures are replaced.

6. Repeat steps 2 through 6 for each structure that you want to replace.

7. To cancel the entries you have selected or entered in the fields, click *Reset*.

8. To complete the operation and return to an idle state, choose *Done* from the right-button pop-up menu.

Related Topics

- replace via structure

replace via with structure

The `replace via with structure` command lets you replace some or all instances of an existing via with a structure. When you choose this command, the *Options* panel of the Control Panel is reconfigured, letting you set the parameters that govern the replacement process. The `replace via with structure` command also lets you override structures that have a FIXED property attachment.

Using this command you can also replace a structure with a via.

Before running the `replace via with structure` command, keep in mind the following conditions of the command:

- New structures that replace an existing via must have a starting element that can connect to the original via.

- Based on the settings you entered in the *Options* panel, if one or more selected instances of a via cannot be replaced in the design, the operation fails to replace any of them.

- If you replace multiple vias, you can undo only the last via that you replaced. To reverse multiple replacements, right-click and use the *Cancel* option in the pop-up menu.

- New structure definition does not preserve the properties attached to the old via or structure.

Related Topics

- Replacing Vias with Structures

Replace Via with Structure Command: Options Panel

Access Using

- *Menu Path: Route – Structures – Replace Via with Structure*

Replacement	Single via	
Ignore Fixed Property	When checked, lets you replace vias that contain the FIXED property attachment. The default setting is unchecked. If you replace a via that has the FIXED property attached, the new structure will also have the FIXED property.	
Replace structure with vias	When checked, lets you replace a structure with a via.The default setting is unchecked.	
Structure Selection		
	Structure	Choose a structure from the drop down list that you want to replace.
	Select	Select structure from the canvas
Via Padstack for Replacement		
Via Selection Filter		
	Padstack	Choose a via from the drop down list that you want to replace.
	Select	Select via from the canvas
Structure for Replacement	Choose a structure from the drop down list that you want to use for the replacement. The structures listed in the box may come from one or both of the following sources:	
	Design	Displays only the structures present in the current design.
	Library	Displays all the structures present in directories defined in the environment variable $PAD_PATH
	Assign return path net	Choose to assign a net for return path via. Only available if high-speed via structures selected in structure has return path connections identified..
Via pitch tolerance		

Batch replace all instances	Executes the command using the values that you set in the preceding field options, and performs batch replacement.

Replacing Vias with Structures

You can replace vias with structures by following these steps:

1. Run the `replace via with structure` command.
   The *Options* panel of the Control Panel displays the controls for replacing via with structure.

2. Choose an existing via available in the design from the drop-down list that you want to replace.
   The name of the selected via appears in the text box.

3. Choose the structure with which you want to replace the via.
   The name of the structure appears in the text box.

4. Click *Batch replace all instances.*

5. Repeat steps 2 through 6 for each via that you want to replace.

6. To cancel the entries you have selected or entered in the fields, right-click and choose *Reset*.

7. To complete the operation and return to an idle state, choose *Done* from the right-button pop-up menu.

Related Topics

- replace via with structure

replay

The `replay` command executes a specified script when you enter the command followed by a script name. If no script name is specified, a dialog box prompts you for a script filename. The `replay` command can be embedded in other scripts and can be nested up to five levels.

> ⚠ The functionality of this command is identical to what occurs when you choose a script and press the *Replay* button in the Scripting dialog box (script).

For additional information on scripting, see record, scriptmode, repeat_again, stop.

Related Topics

- Running the Replay Command

Select Script to Replay Dialog Box

This dialog box is a standard file browser. To choose an object, type the name in the search field, or highlight it in the list box, and click *OK*.

To narrow the list, enter a search string in the search field and click the *OK* button. The asterisk (`*`) displays the complete list. For example, a search string of `MTG*` returns all objects beginning with MTG. Your last search is remembered.

Running the Replay Command

To run the replay command:

1. Type `replay`, followed by a script name at the command console prompt of your user interface.
   The specified script is played.

—or—

1. Type `replay` without specifying a script name.

2. The *Select Script to Replay* dialog box is displayed.

3. Choose a script, then click *OK*.
   The specified script is played.

Related Topics

- replay

report

The `report` batch command lets you display or print information about your design. For descriptions of available reports, see the List of Available Reports.

Syntax

```
report <-v > <-v film> <brd> <out> [-version] [-versionLong]
```

-v	A required 3-character keyword associated with a Cadence-defined report (such as. `bom`) or the name of a user-defined `extracta` command file.
-v film	Skips calculations and displays just film data.
-H	Displays report in an HTML format. Not valid for all types of reports. If specified flags an error. The default name of the HTML report is `<code>.html`.
brd	Name of the design upon which to run a report with or without the file extension (for example, `abc.brd` or `abc`). Prior to generating a report, execute a `save` or `exit` on the active design to ensure values from the latest version of the design are included in the report, because the `report` command reads the last saved (not active) copy of the design.
out	Creates an output file and writes the generated report to it. This field is optional. If you omit an output filename, the report appears on screen.
-version	Prints the program version and exits.
-versionLong	Prints the program's long version if available and exits.

Command line arguments for creating reports are listed in the following table.

Report List

The list of the reports are:

Code	Name
`asf`	Assigned Function
`bom`	Bill of Materials

cbm	Bill of Materials (Condensed)
cmp	Component
cpn	Component Pin
drc	Design Rules Check
drc_shorts	DRCs that report shorting conditions
dpf	Design Partitions
dpg	Diffpair Gaps
fcn	Function
fpn	Function Pin
ean	ECL Act/Sched (net) (no html
eas	ECL Act/Sched(pct mnht) (no html)
ecl	ECL(long)(eclrep.log) (-e) (no html)
ecs	ECL(short)(eclrep.log) (-h) (no html)
ecp	Embedded Components
eld	Etch Detailed Length
ell	Etch Length by Layer
eln	Etch Length by Net
elp	Etch Length by Pinpair
elw	Etch Length by Layer and Width
film	Film report (no copper area calculation) (no html)
film_area	Film report with copper area calculation (long running) (no html)
jcp	Route jumpers
mod	Module (no html)
net	Netlist
net loop	Loops within nets
ban	Netin (back anno:$FCN) (no html

nbn	Netin (non-back:$PACK) (no html)
pad	Padstack Definition
psu	Padstack Usage
psw	Pin Swap
pcp	Placed Component
npr	Properties on Nets
spf	Spare Function
sum	Summary Drawing and Dangle Line Reports
slp	Symbol Library Path
slt	Slot Holes
spn	Symbol Pin
uaf	Unassigned Function
ucn	Unconnected Pin
upc	Unplaced Component
user_schedule	User schedule nets (back anno format) (no html)
ecl_schedule	ECL schedule report (for backward capability)(no html
vfb	Cadence Schematic Feedback
vialist_net	Vias by net
vialist_netlayer	Via by Net and Layer
waived_drc	Waived Design Rule Check
waived_shorts	Waived Shorts (sub-set of waived DRCs)
x-section	Cross Section

Running a report in batch mode

You can run a report in batch mode by following these steps:

1. Type `report` at your operating system prompt.

   To run old style reports set Allegro environment variable

   `ALLEGRO_OLD_REPORT`

1. Type a report list code at the blinking prompt.

2. Press Return/Enter.

   You are prompted to type a layout name.

3. Enter an existing board design name and press Return/Enter.

   You are prompted to type a report filename.

4. Enter an existing output filename and press Return/Enter.

   The program returns status similar to the following:

```
Text File (*.txt): practice
Extract started: command file is '/cds/15.2/v15-2-19/share/pcb/text/views/net_re
p.txt'.
Extract: 50 reads, 50 writes.
Extract: 100 reads, 99 writes.
Extract: 150 reads, 147 writes.
Extract: 200 reads, 197 writes.
Extract: 250 reads, 247 writes.
Extract: 300 reads, 297 writes.
Extract: 350 reads, 345 writes.
Extract: 400 reads, 387 writes.
Extract: 450 reads, 430 writes.
Extract: 500 reads, 472 writes.
Extract: 550 reads, 515 writes.
Extract: 600 reads, 557 writes.
Extract: 650 reads, 607 writes.
Extract: 700 reads, 649 writes.
Extract: 750 reads, 697 writes.
Extract: 800 reads, 739 writes.
Extract ended.
Report written to practice.txt
>> █
```

By default, the report format uses comma (,) as a separater. You can replace comma with a pipe character (|) by setting an environment variable *report_separator_pipe* in the *Reports* category of the *Manufacture* section of the *User Preferences Editor*.

Example

The following example writes a component report from `test.brd` to the `cmp.rpt` file:


```
report -v cmp test cmp
```

reports

Produces reports that provide information about your design. The List of Available Reports defines available reports.

> ⚠ If you ran the `old_reports` command and clicked the Help button from the *Reports* dialog box that subsequently displayed, which was previously available in releases prior to 15.1, refer to the `old_reports` command in the documentation set in that release for more information.

You simultaneously can display reports on screen and save the output to a file using the Text (.rpt, Comma Separated Value (`.csv`) format, or the HTML(`.htm, .html`) format. If you generate 2 to 10 reports, a separate window opens for each one on screen. The message area at the lower edge of the dialog box displays the number of reports written.

By saving reports in a CSV format, which is a Microsoft Excel-compatible ASCII text data table, you can open them directly in spreadsheet programs such as Microsoft Excel or import them via its Text Import Wizard. Each line of the file is a separate data record, and a comma separates each field within the record. All records have the same number of fields. The file's first line is the header row, which specifies the names of each field. You can view web-ready reports by saving reports in HTML. Ensure that the file starts with an <HTML> tag.

You can also generate the following Cadence-provided reports that are not based on `extracta` command files:

- All Shapes
- Constraints
- Design Status
- Design Partition
- Net Single Pin and No Pin
- Parallelism
- Slot Hole
- Symbol Availability
- Testprep

> ⚠ These reports cannot be run using the `report` batch command.

To create and display a report without using the *Reports* dialog box, choose *Tools – Quick Reports* or include the name of the report on the command line. For example, to display the *Dangling Lines, Via and Antenna Report*, type the following, being sure to use quotes to enclose the report name:

```
reports "Dangling Lines, Via and Antenna Report"
```

Quick reports are not automatically saved. To save the report, select the Save option in the report window.

Related Topics

- Viewing Reports On Screen in HTML Format

- Saving a Report to an Output File in CSV format

- Saving Multiple Reports to Output Files in CSV format

- Creating a report for all pins considered "dummy" or unused nets

- List of Available Reports

Reports Dialog Box

Access Using

- *Menu Path: Tools – Reports*

- *Menu Path: Tools – Quick Reports (bypasses Reports Dialog Box)*

- Toolbar Icon:

Available Reports	Lists the existing reports in the paths specified by the `textpath` environment variable, accessible in the `Config_path` folder in the `Categories` section of the *User Preferences* dialog box. The `textpath` environment variable points to the list of available extract definition (view) files. These are predefined `extracta` command files provided by Cadence or user defined. Double click on the reports you want to generate, which then appear in the *Selected Reports* list.
Selected Reports	Displays the reports you chose to generate in the *Available Reports* list. You can generate up to ten reports at a time. To delete a report from this list, double click on it.
Output File (optional)	Enter a custom name of an output file to which to write the generated report.
Append	*Choose to combine individual reports into one output file, the name of which you entered in the Output File field.*
Write Report	Choose to save the report(s) as a text file in Comma Separated Value (CSV) format. If you generate a predefined Cadence-provided report, you also automatically generate the output filename consisting of the keyword associated with the chosen report with an `.rpt` extension appended. You can save the report to a file and display it on screen by enabling both this field and the *Display Report* field. For example, the output filename for the Bill of Materials report is `bom_rep.rpt`. If you generate a custom report configuration, such as `myreport.txt,` the written output file is `myreport.rpt.`
Display Report	Choose to view the generated reports on screen in an HTML-enabled window. If you generate two to ten reports, a separate window opens on screen for each report. You can save the report to a file and display it on screen by enabling both this field and the *Write Report* field.
New/Edit	Click to display the *Extract UI* dialog box, from which you can create new customized reports or edit existing ones.
Browse	Click to open a file browser where you can choose a the path for writing a report.

Load	Click to open a file browser where you can choose a custom report configuration file.
Generate Reports	Click to generate the reports that are displayed in the *Selected Reports* section.
Close	Click to close the dialog box without generating any reports.

Related Topics

- Saving a Report to an Output File in CSV format

- Saving Multiple Reports to Output Files in CSV format

- Creating a report for all pins considered "dummy" or unused nets

- List of Available Reports

Viewing Reports On Screen in HTML Format

To view a report in screen in HTML format:

1. Run `reports`.

2. Choose up to ten reports from the *Available Reports* list by double clicking on each one.
   The specified reports then appear in the *Selected Reports* list. (To delete a report from this list, double click on it.)

3. Enable the *Display Report* field to view the reports on screen.

4. Click *Generate Reports* to generate the reports.
   The specified reports each appear in their own HTML-enabled window. You can print, save, or search for text within each report.

Related Topics

- replay
- Saving Multiple Reports to Output Files in CSV format
- Creating a report for all pins considered "dummy" or unused nets
- List of Available Reports

Saving a Report to an Output File in CSV format

Follow these steps to save a report to a CSV output file:

1. Run `reports`.

2. Choose the specified reports from the *Available Reports* list by double clicking on it.
   The specified reports then appear in the *Selected Reports* list. (To delete a report from this list, double click on it.)

3. Enable the *Write Report* field to save the report as a text file in CSV format.

4. Click *Generate Reports* to generate the reports.

Related Topics

- replay
- Reports Dialog Box
- Creating a report for all pins considered "dummy" or unused nets
- List of Available Reports

Saving Multiple Reports to Output Files in CSV format

Perform these steps to save multiple reports to CSV output files:

1. Run `reports`.

2. Choose the specified reports from the *Available Reports* list by double clicking on it.
   The specified reports then appear in the *Selected Reports* list. (To delete a report from this list, double click on it.)

3. Enable the *Write Report* field to save the reports as text files in CSV format.

4. To *combine individual reports into one output file, enter a custom filename in the Output File field and then choose Append.*

5. Click *Generate Reports* to generate the reports. An output file is created for each report.

Related Topics

- replay
- Reports Dialog Box
- Viewing Reports On Screen in HTML Format
- List of Available Reports

Creating a Report for all Pins Considered "Dummy" or Unused Nets

Several methods exist for reporting on dummy or unused nets.

1. Use extracta to create a command file with the following and save it with a `.txt` extension.

```
LOGICAL_PIN

NET_NAME = ""

REFDES

REFDES_SORT

PIN_NUMBER_SORT

PIN_NUMBER

END
```

1. Place this `.txt` file where `extracta` can locate it, based on the TEXTPATH variable.

2. Run *Tools – Reports* and choose the command file by double clicking on it. Then click *Report.*

In the second method, choose *Display – Element*. Enable *Nets* in the Find Filter. Window select all components.

Example:

```
Item 1          < NET >

This is a DUMMY net

Via Count:       0

  Total Etch Length:      0 MIL

  Net path data not applicable ( NO_RAT )
```

```
Pin(s):


   RP2.5


No connections found in net
```

In the third method, choose *Export – IPC 356,* and use the file's section on dummy nets:

Example:

```
C  ***********************************            0112


C    DUMMY NET PINS ON THE BOARD          0        0113


C  ***********************************              00114


C                 00115


C                 00116


317N/C        K1     -9    D0360PA00X+043000Y+023000X0600Y0600                    S3
```


In the fourth method, choose *Manufacturing – Testprep – Automatic* (testprep automatic command), and enable the *Test Unused Pins* field. Use the data from the testprep.log for unused pins (dummy).

Example:

```
 Probes accessing both sides of the board.


 No restrictions on pad type.


 Pin type restricted to 'PIN'.


 Minimum pad dimension is : 0


 ...
```

Related Topics

- replay

- Reports Dialog Box

- Viewing Reports On Screen in HTML Format

- Saving a Report to an Output File in CSV format

List of Available Reports

You can create and display a report using the *Reports* dialog box. Alternatively, choose the report you want to create from the *Tools – Quick Reports* menu, or include the name of the report on the command line. For example, to display Netlist Report, type the following, being sure to use quotes to enclose the report name:

```
reports "Netlist Report"
```

Assigned Function Report

Lists all assigned functions, sorted by function designator.

Backdrill Report

Lists all backdrill data (start layer and must-cut-layer) saved on pins and vias. The report also includes total backdrills and manufacturing stub length.

Bill of Material Report

Lists all components in the design, sorted by reference designator.

Bill of Material [Condensed] Report

Lists all components in the design, sorted by symbol type.

Cadence Schematic Feedback Report

Creates a back-annotation file for a Cadence front-end tool and lists the nets attached to each pin on the board, sorted by component and device type. This report excludes power and ground nets or pins. Originally intended for Design Entry HDL or System Connectivity Manager users, the information is valid for customers using third party logic as well. Obtained from the design file, the four columns are:

- <Reference Designator>

- <Device Type>
- <Pin>
- <Net Name>

Component Pin Report

Lists all component pins in the design, sorted first by reference designator then by pin number.

Component Report

Lists all components in the design, sorted by reference designator.

Dangling Lines, Via, and Antenna Report

This report shows dangling connect lines, vias and antenna vias in the design. See the report header for detail content description.

> ⓘ You cannot generate this report if a `sum_rep.txt` file is located in the same directory as the `.brd` file.

Design Partition Report

Generates a history of partition parameters, including the names and number of partitions, their database status, path, designer, and any notes when you choose to partition a design.

Design Rules Check Report

Lists all design rule violations.

Etch Length By Layer Report

Lists total etch length on each etch layer for each net.

Etch Length By Layer and Width Report

Lists net name, layer name, and etch length by layer.

Etch Length By Net Report

Lists net name, etch length by net, etch length, manhattan length, and percent manhattan.

Etch Length By Pin Pair Report

Lists net name and etch length by pin pair.

> ⚠ Power and ground nets are excluded from the report if a net have any of the following:

- RATSNEST_SCHEDULE of POWER_AND_GROUND

- NO_RAT property

- pin count greater than 500

Film Area Report

Lists film name, class, subclass, area, and metal percentage between copper and board-outline (or route keep-in, when board outline is added as lines instead of a shape). While calculating metal percentage, all objects present on the film, irrespective of their location — they can be located either inside or outside board outline — are considered.

The metal percentage calculation takes place as follows:

- If the board outline is added as a shape then the metal percentage is calculated between copper and board outline.

- If the board outline is drawn with lines then the metal percentage is calculated between copper and route keep-in. However, if the route keep-in is not defined, metal percentage is not reported.

Function Pin Report

Lists all assigned and unassigned function pins, sorted first by function designator, then by pin name.

Function Report

Lists all assigned and unassigned functions, sorted by function designator.

Missing Fillets Report

Lists Pad and T fillet parameters used to generate fillets as well as missing and partial fillets, the latter of which occur when the tool creates a portion of a fillet. You can click on the coordinates in the report to precisely locate missing or partial fillets in the design. Other information includes net name, item, location, and subclass.

Module Report

Lists module instance, module definition, x and y coordinates, angle, module path and total module count.

Netlist Report

Lists connections, sorted first by net name then by pin number.

Net Single Pin and No Pin

Lists nets that have only a single pin or no pins attached to them.

> ⚠ The layout editors do not allow nets without any pins, so these nets will not appear in the report.

> ⚠ You can add OK_NET_ONE_PIN property to the net to suppress it from being reported.

Netin Back (back anno.)

Creates a netlist file that you can load or back-annotate. Writes the `$FUNCTIONS` section by device type, function type, and function designator; writes `$NETS` section by net name, function designator, and pin name.

Netin (non back)

Creates a netlist file that you can load. Writes the `$PACKAGES` section by device type, symbol name, and reference designator; writes `$NETS` section by net name, reference designator, and pin number.

Padstack Definition Report

Lists all pad definitions in the design.

Padstack Usage Report

Lists symbol pins that use padstack definitions.

Placed Component Report

The Placed Component report lists all placed components, sorted by reference designator. Other information supplied in the report includes:

- Device type

- Package/Part symbol

- Value and tolerance

- x, y coordinates

- Placement angle

- Whether the symbol is mirrored

Properties on Nets Report

Lists properties attached to nets, sorted by net name.

Shape Dynamic State Report

Lists the state of all shapes, either out-of-date or smooth.

Shape Islands Report

Lists all shapes on the net that are not attached.

Shape No Net Report

Lists all etch or conductor shapes that are not assigned to a net.

Shape Report

Lists dynamic shape settings; generation results, including number of dynamic etch shapes and their areas; shape fill type; thermal relief connects; void controls; and clearance settings.

Slot Hole Report

Details information about oval and rectangularly shaped slot holes for fabrication purposes when you do not want to generate NC Route output. For each slot hole, the report lists the X/Y location of the hole center; the padstack-defined Size X, Size Y, the start and end layer, and Plating settings; and the rotation inherited from the symbol using the padstack. Size X and Size Y represent the values at 0 rotation without mirroring.

Spare Function Report

Lists functions available on a placed or unplaced component.

Summary Drawing Report

Lists major statistics of the drawing.

Symbol Availability Check Report

Lists the library paths of all unplaced symbols.

Symbol Library Path Report

Lists the path to each symbols library of origin.

Symbol Pin Report

Lists all symbol pin instances, sorted first by reference designator, then by pin number. Also reports a pin's X/Y coordinates, symbol name, comp device type, padstack name, and net name.

Testprep Report

Organizes data regarding the testpoint coverage of a design, highlighting untestable nets, as well as the percentage coverage, number of nets covered, number of testpoints, and number/percentage of testpoints on top/bottom sides.

Unassigned Functions Report

Lists all unassigned functions, sorted by function designator.

Unconnected Pins Report

Lists all unconnected pins in the design with hyperlinks to X/Y coordinates, net names, and total unconnected pins.

Unplaced Components Report

Lists all unplaced components in the design.

Unused Blind/Buried Via Report

Identifies unused blind and buried vias associated with a via stack structure, which can comprise coincidently placed microvias, blind and buried vias, or a combination of both. For example, consider the via stack Micro1-2, BB2-7, and Micro7-8. If a trace connects to the stack on Layers 3 and 6, Micro1-2 and Micro7-8 are identified as unused. Click on the hyperlink to navigate to their location. Unavailable in Allegro PCB Design L, OrCAD, and Allegro PCB Performance option L.

User Schedule [back anno.]

Lists the third party $SCHEDULE netlist.

Via List by Net Report

Lists net name, total vias, through vias, BB vias and via name.

Via List by Net and Layer Report

Lists net name, total vias, through vias, BB vias and via name in each layer.

Via Structure Report

Lists via structure net name, via structure symbol name, return net name assigned to the return path connections for high-speed via structure, via structure type as high-speed or standard, rotation angle, mirroring status, modification status, and the location (X, Y coordinates) of the via structure symbol.

In case of multi-net via structure, each net assigned to the via structure is listed in a separate row. If a net is connected with two or more via structures, then each via structure is listed in a separate row for the same net. Via structures not assigned to any net are displayed in the end of the table.

Total number of rows and the number of the via structures placed in the design are displayed at the bottom of the report.

Waived Design Rules Check Report

Lists all waived design rule violations in the design.

Related Topics

- replay
- Reports Dialog Box
- Viewing Reports On Screen in HTML Format
- Saving a Report to an Output File in CSV format
- Saving Multiple Reports to Output Files in CSV format

rep padstack

The `rep padstack` command lets you replace padstacks with new padstacks when you are in generaledit mode and the items you select use the same padstack. You can replace selected instances, all instances, or you can filter instances for replacement.

Related Topics

- 47981

- Rep Padstack Command When Filtering Instances: Options Panel

- Replacing Padstacks/Multiple Vias

- Replacing Single Vias

Rep Padstack Command When Filtering Instances: Options Panel

Single via replace mode	Check this box to select only one bond finger or pin for which you want to change the padstack.
Padstack names	
Old	Identifies the padstack being replaced.
New	Identifies the name of the new padstack. If this padstack does not already exist in the design, it is loaded. Choose your padstack library.
Symbol	Identifies the name of the symbol whose padstacks are to be replaced. You can use a wildcard in this field to indicate more than one type of symbol. The default value is an asterisk (*).
Pin #	Indicates the number of the pins whose padstacks are to be replaced. You can use a wildcard in this field to indicate multiple pin numbers. The default value is an asterisk (*) to indicate that any pin number is acceptable.
RefDes	Specifies the reference designator of the components whose padstacks are to be replaced. You can use a wild card in this field to indicate multiple reference designators. The default value is an asterisk (*) to indicate that any reference designator is acceptable. The combination of Old Padstack, Symbol Name, Pin Number, and Ref Des values identifies the padstacks that are to be replaced. Only padstacks that match the values in all of these field options are modified. For example, if Ref Des is U22 and Pin Number is 5, only the padstack on pin number 5 of component U22 are changed. If Ref Des is U*2 and Pin Number is *3, the padstacks of a group of pins (such as U12.3, U12.13, U22.3, and U22.13) are changed.
Net	Indicates the name of the net whose padstacks are to be replaced.
Replace	Executes the `rep padstack` command using the values that you set in the preceding field options, and performs DRC.
Reset	Clears any values that you entered in the control fields.

Related Topics

- [Replacing Single Vias](#)

reset dockwindows

Resets the UI and display reduced toolbars and icons. This command reduces clutter by increasing design canvas size and displaying relevant toolbars and icons. The command restores the *Options, Worldview, Find, Visibility*, and *Command* foldable window panes to display in their original positions. You must resize and dock or undock these panes individually.

⚠ Executing this command resets any tool bars you customized using *View – Customize Toolbar* as well.

To show all window panes in the positions in which you last viewed them, use *View – Windows – Show All* (show_allpanes command).

To restore the legacy all toolbars icons view, you can either choose *View – Reset UI to All toolbars* menu or access default configuration settings from the *View – Manage UI Settings*.

Syntax

```
reset dockwindows
```

Access Using

- *Menu Path: View – UI Settings – Reset UI to Default*

Displaying All Foldable Window Panes to Default Positions

1. Choose *View – UI Settings – Reset UI to Default*.

Displays relevant toolbars with minimum icons. The *Options, View, Find, Visibility*, and *Command* foldable window panes display in their original positions.

resizewindow

The `resizewindow` command lets you resize the dimensions of your user interface by a specified factor, using the upper-left corner of the UI as the "anchor point" for the resizing.

Resizing the Design Window

1. Type `resizewindow` followed by two numbers. The numbers you enter represent the height and width dimensions of the resizing.

restore waived drc

Returns a waived DRC error to active status. It is the opposite of the `waive drc` command. When you finish restoring the waived DRC error, the DRC error count updates in the *Status* tab of the *Status* dialog box, available by choosing *Display – Status* (status command), but the status remains out-of-date until you click *Update DRC*.

This command functions in a pre-selection use model, in which you choose an element first, then right-click and execute the command.

Valid objects:

- DRC Errors

> ⚠ If you window select a group of DRC errors that contain both waived and restored DRCs, both *Waive DRC* and *Restore DRC* appear in the pop-up menu, and you can use either as required. To restore all the waived DRCs within the group, right-click and choose *Quick Utilities – Restore All Waived DRCs* from the pop-up menu.

For additional information on waiving DRC errors, see show waived drcs, blank waived drcs, and restore waived drcs, and the *Creating Design Rules* user guide in your documentation set.

Access Using

- *Menu Path: Display – Waive DRCs – Restore*

Restoring a Waived DRC Error to Active Status

To restore a waived DRC error to active status:

1. Hover your cursor over a DRC error marker or window select a group of DRCs. The tool highlights it, and a datatip identifies its name.

2. Right-click and choose *Restore DRC* from the pop-up menu.
   The waived DRC error marker reverts to the active DRC error marker color and rotates 90 degrees.

restore waived DRC errors

Returns all waived DRC errors to active status. When you finish restoring the waived DRC errors, the DRC error count updates in the *Status* tab of the Status dialog box (*Display – Status*), but the status remains out-of-date until you click *Update DRC*.

This command functions in a pre-selection use model, in which you choose an element first, and then right-click and execute the command.

Valid objects:

- DRC Errors

If you window select a group of DRC errors that contain both waived and restored DRCs, both *Waive DRC* and *Restore DRC* appear in the pop-up menu, and you can use either as required. To restore all the waived DRCs within the group, right-click and choose *Quick Utilities – Restore All Waived DRCs* from the pop-up menu.

For more information on waiving DRC errors, see waive drc, show waived drcs, blank waived DRC errors, and restore waived drc, and *Waiving Design Rule Check Errors* in your product documentation.

Access Using

- *Menu Path: Display – Waive DRCs – Restore All*

Restoring All Waived DRC Errors to Active Status

Follow these steps to restore all waived DRC errors to active status:

1. Window select a group of waived DRC errors.

2. Right-click and choose *Quick Utilities – Restore All Waived DRCs* from the pop-up menu.

3. Click *Yes* in the confirmation dialog box that appears.
   The waived DRC error markers restore to the active DRC error marker color and rotate 90 degrees.

return

An internal Cadence engineering command.

rf_ac_assemble

The `rf_ac_assemble` command lets you include available Route Keep Outs and clearance objects (etch shapes, vias, pins, clines, clearance shapes, and existing clearance assemblies) into a new clearance assembly. It can also be used to merge existing clearance assemblies.

Using the `rf_ac_assemble` command you can create clearance objects for RF components that are part of a module.This command also fixes the assembling of asymmetrical clearance shapes and RF components contained in hard reused module instances.

For further information, see *Assembling Clearance Shapes* in the *Allegro User Guide: Working with RF PCB*.

Related Topics

- Choosing the Elements to Assemble

- Assembling the Selected Objects

RF AC Assemble Command: Options Panel

Access Using

- *Menu Path: RF-PCB — Clearances — Assemble*

Disbanded assemblies in modules	Displays and select module instances that have disbanded asymmetrical clearance objects, grouped with same definition name.
Fix disbanded assemblies	Choose to fix the selected modules with disbanded asymmetrical clearance assemblies.

Related Topics

- Assembling the Selected Objects

Choosing the Elements to Assemble

To choose elements to assemble, follow these steps:

1. Choose *RF-PCB — Clearances — Assemble.*
   The console window displays the following message:
   ```
   Select objects to assemble...
   ```

2. Select objects by clicking on a single element or holding the left mouse button and drag a bounding box around several elements. You can also use the Temp Group selection mode.

3. Alternatively, select modules with disbanded assemblies from the *Options* panel.
   The last-picked module is zoomed in.

Related Topics

- rf_ac_assemble

Assembling the Selected Objects

Follow these steps to assemble selected objects:

1. Click on the board to create a clearance assembly.

2. If a module instance is selected from the *Options* panel then click *Fix disbanded assemblies*.
   The DRC errors caused by route keepout shapes to etch objects are removed.

3. A report is displayed. You can verify and check any warnings or errors that may have occurred. The log file is saved in your working directory.

4. Right-click and choose *Done* to complete the command or choose *Next* to save the changes and start a new assemble session.

Related Topics

- rf_ac_assemble
- RF AC Assemble Command: Options Panel

rf_ac_delete

The `rf_ac_delete` command lets you delete clearance shapes from a clearance assembly or multiple clearance assemblies.

You can also delete clearance shapes for RF components that are part of a module.

For further information, see *Asymmetrical Clearances* in the *Allegro User Guide: Working with RF PCB*.

Related Topics

- Choosing the Clearance Shapes to Delete
- Deleting the Clearance Shapes

RF AC Delete: Options Panel

Access Using

- *Menu Path: RF-PCB — Clearances — Delete*

Class/ subclass: Route Keepout	Check (enable) to select the layers from which to delete the clearance shapes. If you select all layers, all clearance shapes for those selected clearance assemblies will be deleted. If the deletion results in any of the clearance assemblies to be empty, the empty clearance assembly is deleted as well.

Related Topics

- Deleting the Clearance Shapes

Choosing the Clearance Shapes to Delete

To choose the clearance shapes for deletion:

1. Choose *RF-PCB — Clearances — Delete.*
   The console displays the following message:
   ```
   Select RF components to delete...
   ```

2. Select objects by clicking on a single element or holding the left mouse button and drag a bounding box around several elements. You can also use the Temp Group selection mode.
   The console displays the following message:
   ```
   Select RF components to delete...
   ```

OR

1. In the rfedit_appm application mode, right-click over the element, or over any one of the group of elements.

2. Choose RF Clearance Delete from the right-click menu.

The delete clearance options display in the *Options* panel.

Related Topics

- rf_ac_delete

Deleting the Clearance Shapes

Follow these steps to delete the clearance shapes:

1. From the *Options* panel, select the layers from which to delete the clearance shapes.

2. Click on the board to delete the clearance shape from the selected clearance assembly.

3. Right-click and choose *Done* to complete the command or choose *Next* to save the changes and start a new delete session.

Related Topics

- rf_ac_delete
- RF AC Delete: Options Panel

rf_ac_disassemble

The `rf_ac_disassemble` command lets you disband existing clearance assemblies on the board. There are two modes in which a clearance assembly can be dis-assembled.

In one mode, the command can be used to deconstruct a clearance assembly, and the clearances shapes that constituted the clearance assembly are not deleted, but they are no longer members of the clearance assembly.

In the other mode, the command can be used to delete all the clearance shapes within the clearance assembly and then remove the clearance assembly. If there are etch shapes from RF symbols contained in the disbanded clearance assembly, the initial clearance shapes are created for all related RF symbols with new individual clearance assembly for each RF symbol.

You can also disband clearance objects for RF components that are part of a module.

For further information, see *Asymmetrical Clearances* in the *Allegro User Guide: Working with RF PCB*.

Related Topics

- Choosing the Elements to Disassemble
- Disassemble the Selected Objects

RF AC Disassemble Command: Options Panel

Access Using

- *Menu Path: RF-PCB — Clearances — Disassemble*

Re-initialize Clearance Shapes	When selected (checked), on disassembling a clearance assembly, deletes all the clearance shapes and removes the clearance assembly. If there are any etch shapes from RF symbols contained in the removed clearance assembly, the command will create initial clearance shapes for each of the RF symbols. The created initial clearance shapes can be put in a whole new clearance assembly or put in new clearance assemblies on a RF symbol basis.
Group Asymmetrical Clearances	When selected (checked), all initial clearance shapes created for RF symbols are put in a whole new clearance assembly. Otherwise, multiple clearance assemblies will be created to hold initial clearance shapes on a RF symbol basis.
Retain Clearance Shapes	When selected (checked), on disassembling a clearance assembly, retains the original clearance shapes, but the clearance assembly is removed.

Pop-Up Menu Options

When you are in `rf_ac_disassemble`, right-click in your design canvas to display the pop-up menu.

Item	Description
Clearance Settings	Opens the Clearance Settings dialog box to edit the clearance shape settings.

Related Topics

- Disassemble the Selected Objects

Choosing the Elements to Disassemble

Follow these steps to choose the elements to disassemble:

1. Choose *RF-PCB — Clearances — Disassemble.*
   The console displays the following message:
   ```
   Select objects to disassemble...
   ```

2. In the *Options* panel select *Re-initialize Clearance Shapes* or *Retain Clearance Shapes*.

3. Select objects by clicking on a single clearance assembly or holding the left mouse button and drag a bounding box around several clearance assemblies. You can also use the Temp Group selection mode.

OR

1. In the rfedit_appm application mode, right-click over the clearance assembly, or over any one of the group of clearance assemblies.

2. Choose RF Clearance Disassemble from the right-click menu.

3. In the *Options* panel select *Re-initialize Clearance Shapes* or *Retain Clearance Shapes*.

Related Topics

- rf_ac_disassemble

Disassembling Selected Objects

To disassemble selected objects:

1. Click on the board to disassemble the clearance assembly.

2. Right-click and choose Done to complete the command or choose Next to save the changes and start a new disassemble session.

Related Topics

- rf_ac_disassemble
- RF AC Disassemble Command: Options Panel

rf_ac_init

The `rf_ac_init` command lets you create initial clearance shapes for the selected RF objects and puts them in new clearance assemblies. The command also specifies setup options for creating clearance shapes.

You can also create initial clearance shapes for RF components that are part of a module.

For further information, see *Asymmetrical Clearances* in the *Allegro User Guide: Working with RF PCB*.

Related Topics

- Initializing Clearance Shapes for RF Objects

RF AC Init Command: Options Panel

Access Using

- *Menu Path: RF-PCB — Clearances — Initialize*

Group Asymmetrical Clearances	Check to create one clearance assembly to hold all the initiated clearance shapes for selected RF symbols. A merge is performed on the initiated clearance shapes before adding them in the clearance assembly. When you select multiple RF symbols only the "Surrounding" clearance mode is allowed. Uncheck to create individual clearance assemblies to hold the initiated clearance shapes for selected RF symbols. No merge is performed on the initiated clearance shapes.
View clearance shape by layer	Specify the layer to preview the dynamic path of the clearance shape on the selected layer.
Clearance Settings	
Layer	Check to allow creation of clearance shapes on the selected layer.
RF comp	Specify the offset value for an RF component on the selected layer.
Cline/Trace Side 1	Specify the offset value for a cline or trace shape on the left side of the selected layer.
Cline/Trace Side 2	Specify the offset value for a cline or trace shape on the left side of the selected layer.
Shape	Specify the offset value for a generic shape on the selected layer. - For a shape that is connected to two pins and both the pins are close to shape boundary, asymmetrical clearance is supported. - For all the other generic shapes, symmetrical clearance is supported.
Transmission Line Clearance mode	
Sidewalk	Select this mode to create the clearance shape by expanding the bounding box of the etch shape in the two directions that don't lead to pins or connections.
Surrounding	Select this mode to create the clearance shape by expanding the bounding box of the etch shapes in all directions.

Display Transmission Lines	Displays a list of RF components that are defined as transmission lines in a separate window.
Override global clearance settings	Enable to edit and use local clearance settings. These setting are retained during command process. If disabled, the global clearance settings are not editable and all the RF commands share the same global clearance settings.

Pop-up Menu Options

Done	Terminates the command, saving actions performed while the command was active.
Cancel	Terminates the command without saving.
Next	Saves the changes and start a new initialize session
Swap	Swap the left/right offset values for the clearance shapes.

Initializing Clearance Shapes for RF Objects

Perform these steps to initialize the clearance shapes for RF objects:

1. From the menu bar, choose *RF-PCB — Clearance — Initialize*.

2. To group the clearance shapes into a clearance assembly, check *Group Asymmetrical Clearances* in the *Options* panel.

   > ⊘ Set the *Find Filter* to filter out the undesired objects. The filter settings are retained by the tool even after the command is exited.

3. Enable *Override Global Clearance Settings* to edit and use local clearance settings during the command process.

4. Select the layers on which to create the clearance shapes.

5. Specify the offset values for RF comp, cline, RF trace, and shape for different layers.

6. Choose *Sidewalk* or *Surrounding* to specify the mode to use while creating clearance shapes for transmission line components.

7. Specify the objects in the *Find* filter.

8. Click to select single RF object or drag a window to select multiple objects. *Temp Group* mode can also be used from Right Mouse Button menu to select multiple RF objects.

9. Choose layer from *View clearance shape by layer* to preview the shape on the selected layer.

10. Optionally, select *Swap* from pop-up menu to swap left/right offset values for the clearance shapes. Right-click and choose *Complete* to complete the swapping.

11. Click on the board to add a clearance shape to the selected RF object.

12. Right-click and choose *Done* to complete the command or choose *Next* to save the changes and start a new initialize session.

OR

1. In the rfedit_appm application mode, right-click over the element, or over any one of the group of elements.

2. Choose *RF Initialize clearance* from the right-click menu.
   The flip options display in the *Options* panel.

3. To group the clearance shapes into a clearance assembly, check *Group Asymmetrical Clearances* in the *Options* panel.

4. Enable *Override Global Clearance Settings* to edit and use local clearance settings during the command process.

5. Select the layers on which to create the clearance shapes.

6. Specify the offset values for RF comp, cline, RF trace, and shape for different layers.

7. Choose *Sidewalk* or *Surrounding* to specify the mode to use while creating clearance shapes for transmission line components.

8. Specify the objects in the *Find* filter.

9. Choose layer from *View clearance shape by layer* to preview the shape on the selected layer.

10. Optionally, select *Swap* from pop-up menu to swap left/right offset values for the clearance shapes.Right-click and choose *Complete* to complete the swapping.

11. Click on the board to add a clearance shape to the selected RF object.

12. Right-click and choose *Done* to complete the command or choose *Next* to save the changes and start a new initialize session.

Related Topics

- rf_ac_init

rf_ac_setup

The `rf_ac_setup` command lets you specify the settings for asymmetrical clearances.

For further information, see *Asymmetrical Clearances* in the *Allegro User Guide: Working with RF PCB*.

Related Topics

- Specifying Settings for Asymmetrical Clearances

RF AC Setup Command Dialog Box

Access Using

- *Menu Path: RF-PCB — Clearances — Settings*

Layer	Check to allow creation of clearance shapes on the selected layer.
RF comp	Specify the offset value for an RF component on the selected layer.
Cline/Trace Side1	Specify the offset value for cline or trace shape on the left side on the selected layer.
Cline/Trace Side 2	Specify the offset value for cline or trace shape on the right side of the selected layer.
Shape	Specify the offset value for a generic shape on the selected layer. ○ For a shape that is connected to two pins and both the pins are close to shape boundary, asymmetrical clearance is supported. ○ For all the other generic shapes, symmetrical clearance is supported.
Transmission Line Clearance mode	
Sidewalk	Select this mode to create the clearance shape by expanding the bounding box of the etch shape in the two directions that don't lead to pins or connections.
Surrounding	Select this mode to create the clearance shape by expanding the bounding box of the etch shapes in all directions.
Display Transmission Lines	Displays a list of RF components that are defined as transmission lines in a separate window.
Restore Default	Click to restore the default layer selection and offset values.
Save as Default	Click to save the current layer selection and offset values as default.

Specifying Settings for Asymmetrical Clearances

Follow these steps to specify the settings for asymmetrical clearances:

1. From the menu bar, choose *RF-PCB — Clearance — Settings.*

   > ⚠ You can also choose *Clearance Settings* options from the right-click menu of several RF PCB commands, such as `rf_add_connect`, `rf_add_component`.

   The Clearance Settings dialog box displays.

2. Select the *Layers* on which to create the clearance shapes.

3. Specify the offset values of the clearance shapes for RF comp, clines, and RF traces.

4. Choose *Sidewalk* or *Surrounding* to specify the mode to use while creating clearance shapes for transmission line components.

5. Close the dialog box or right-click on the board and choose *Done.*

The settings you enter in the dialog box are retained in the current session of PCB Editor. To retain these values in other sessions use *Save as Default* and *Restore Default* options.

Related Topics

- rf_ac_setup

rf_add_component

The `rf_add_component` command lets you place RF components into your design. You can select the component type from several different component categories. For further information, see *RF Placement* in the *Allegro User Guide: Working with RF PCB*.

Related Topics

- RF Add Component Command: Options Panel

- Placing RF Components in your Design

- Inserting an RF Component Between Two Connected Components

Right Mouse Button Menu Options for RF Add Component Command

Loop Pin Forward	Changes the pin to connect point by shifting forward to the next pin on the RF component. The net of the connect pin updates as the pin changes. The net of the connect pin does not change if there are no objects connected at the connect point. When you reach the maximum pin number of the component, the looping begins again starting with the first pin.
Loop Pin Backward	Changes the pin to connect point by shifting backward to the next pin on the RF component. The net of the connect pin updates as the pin changes. The net of the connect pin does not change if there are no objects connected at the connect point. When you reach the maximum pin number of the component, the looping begins again starting with the first pin.
Pick Connect Pin	Picks the desired connect pin on the dynamic display of a multi-pin RF component.
Flip Symbol	Flips the RF component. Provides flexibility in controlling the physical positioning of the component. You cannot flip a component before you establish the pin to connect point.
Snap pick to	Activates the available snapping modes. For more information on snapping, see the *Allegro User Guide: Getting Started with Physical Design*.
Clearance Settings	Opens the Clearance Settings dialog box to edit the clearance shape settings.
Show/Hide GUI Form	Choose to toggle the display settings for the edit dialog box specific to the component.

Related Topics

- Placing RF Components in your Design

- Inserting an RF Component Between Two Connected Components

RF Add Component Command: Options Panel

Access Using

- *Menu Path: RF-PCB — Add Component*

Active Layer

Lets you specify the etch subclass on which to place new RF components.

Component Categories

Microstrip	Sets the component category to Microstrip.
Multi-Layer	Sets the component category to Multi-Layer.
Waveguide	Sets the component category to Waveguide.
Lumped	Sets the component category to Lumped.
Stripline	Sets the component category to Stripline.
PCB	Sets the component category to PCB.
Miscellaneous	Sets the component category to Miscellaneous.
Special Vias	Sets the component category to Special Vias.

Element Type

Displays the name of the current library and lets you choose the RF component type from a list of options. The MWO library includes only microstrip and stripline components.

Show ADS compatible

When checked, display only ADS compatible RF components from Unified RF library. This option is grayed out if the *Current RF Library* is not set as *CDN Unified*.

Show MWO compatible

When checked, display only MWO compatible RF components from Unified RF library. This option is grayed out if the *Current RF Library* is not set as *CDN Unified*.

Snap to connect point

When checked, enables automatic determination of the correct start point and rotation angle for the RF component in the following sequence.

- Checks for database objects at the mouse pick point.

  - If there are no database objects, the start point is set to the mouse pick point and the net logic is not changed.

  - If there are database objects at the point, the possible start points, rotation angle, and logic information is determined by the database type in order of precedence.

Snap to pad edge

When checked, snaps the pin of an RF component to the pad edge of a non-RF component.

If this option is disabled or both the components are RF, the pin is snapped to the center of the pad.

Offset to connect point

Used to specify the distance at which the component must be placed away from the connect point. The default value is Zero, and the component is snapped to the connect point. You can provide negative or positive offset values.

Enable insertion

Used to insert the component between two connected RF components on the canvas. This option is only available if Snap to connect point option is selected.

Enable DRC check

Enables DRC checking. If placing a component results in a design rule violation, and this option is enabled, the component is not placed. If this option is disabled, the component is placed with a DRC error.

Initialize Clearance

When checked, adds a clearance shape to the RF component.

Add into existing assembly

When checked, adds the clearance shape generated along with the RF component, to the existing clearance assembly

Related Topics

- rf_add_component

- Inserting an RF Component Between Two Connected Components

Placing RF Components in your Design

Follow these steps to place RF components in your design:

1. From the menu bar, choose *RF-PCB — Add Component*.
   Alternatively, In the rfedit_appm application mode, right-click and choose Quick Utilities - RF Add component.
   The Add Component options display in the *Options* panel.

2. Click the *Active Layer* drop-down arrow, and specify the etch subclass where you want your RF components to be placed.
   The selected subclass icon appears in the dialog box and the layer is now active.

3. Click on an RF component category to select it.

4. Optionally, click *Select Show ADS compatible* only or *Show ADS compatible only* or both the options.
   The *Element type* lists shows components as per the selection.

5. Select a component to place from the *Element type* list.
   An instance of the selected component appears on your cursor.

6. To enable snap, check *Snap to connect point* and specify a *Offset to connect point* value.

7. Optionally, check the *Snap to connect point* and *Snap to pad edge* options.
   If the source is an RF symbol, the dynamic path of RF symbol is attached to the cursor and the ratsnest is displayed. You can snap to the middle of the pad edge of the destination pin. If the cursor moves near another pad edge, the dynamic path is updated and you can snap to that pad edge.
   The snapping direction (inward/outward) is determined by the cursor position relative to the destination symbol pin.

8. Check *Enable DRC check* to apply design rules to validate the add component process.

9. Drag the component instance to its placement location in the design, then click to anchor it.

10. After anchoring the component, right-click and choose *Show/Hide GUI form* to display the parameters dialog box. You can set component parameters and specify nets for component pins.

11. Set the component parameters as desired using the *Parameters* tab in the dialog box, then assign nets to component pins using the *Nets* tab.

   ⚠ When you place an RF component, the tool assigns an appropriate net name.

   See the procedure for the rf_change command for further details on setting parameters and assigning nets.

12. The component is placed and pivots about its anchor point as you move your cursor. Continue to move your cursor to adjust the component orientation as desired, then click again to lock it.
   The component color changes to the color of the active layer and is now placed in the design.

Related Topics

- rf_add_component

- Right Mouse Button Menu Options for RF Add Component Command

Inserting an RF Component Between Two Connected Components

When adding RF components, you have the option to insert the component between two connected components on the canvas. You can do so by following these steps:

1. Perform steps 1 to 4 in the procedure Placing RF Components in your Design.

2. Check *Snap to connect point* and specify a *Offset to connect point* value.

> ⚠ To insert an RF component, you need check *Snap to connect point.* You may specify an *Offset to connect point* value or leave the default value, 0.00.

3. To insert the component between two connected components, check the Enable insertion option.

4. Check *Enable DRC check* to apply design rules to validate the add component process.

5. Drag the component instance to the right or left of the connecting point of the two currently connected components.

6. Right-click and choose Snap pick to - Pin.
   Notice the dynamic path for the inserted component. To change the connect pin, right-click and choose Loop Pin Forward or Loop Pin Backward or Pick Connect Pin.

Related Topics

- rf_add_component
- Right Mouse Button Menu Options for RF Add Component Command
- RF Add Component Command: Options Panel

rf_add_connect

The `rf_add_connect` command lets you add RF traces in your design. All trace segments and bends are considered RF components. You can also insert other RF components in-line as you route.

For a component that is part of module instance, you can route with an interface pin.

Related Topics

- Setting Up for Trace Routing

- Routing a Trace From a New Point

- Inserting an RF Component While Routing

- Routing a Trace From a Supported Object (pin, via, symbol, cline vertex, or shape)

- Connecting Two Points or Components with a Direct Trace

- Connecting Two Points or Components with a Meander Trace

RF Add Connect: Options Panel

Access Using

- *Menu Path: RF-PCB — Add Connect*

Act	Specifies the active routing layer.	
Alt	Specifies the alternate routing layer.	
Via	Specifies a via to use for a layer change.	
Ground above	Specifies the reference plane above the signal trace (for simulation purposes).	
Ground below	Specifies the reference plane below the signal trace (for simulation purposes).	
Net	Specifies the net name for the starting pin of the route. Click the browse button to select a net.	
Route Mode	Select a routing mode	
	Trace	Specifies the Trace mode for adding connects.
	Meander	Specifies the Meander mode for adding connects.
Bend Mode	Specifies the type of bend to use for the Trace mode. Choices are:	
	90D Unmitered	90 degree corner with no miter.
	90D Mitered	90 degree bend with a miter controlled by a miter fraction.
	90D Opt-Mitered	90 degree bend with an optimal miter fraction.
	Curved	A curved bend with a specified radius.
	Specifies the type of bend to use for the Meander mode. Choices are:	
	None	No bends.
	Mitered	A mitered bend with a specified radius.
	Curved	A curved bend with a specified radius.

Line Width	*Specifies the width of the trace. Units are determined by the drawing units.* Enter a new value or choose the line width value from the drop-down list that is saved as global setting.
Radius	Specifies the radius used for curved bends. Note: This option is available only when: ○ In Trace mode, *Bend mode* is *Curved*. ○ In Meander mode, *Bend mode* is either *Mitered* or *Curved*.
Miter Fraction	Specifies the factor used to calculate the bend miter. Note: This option is available only in *Trace* mode when *90D Mitered* bends are specified*.
Line lock	Specifies the trace angle increment when routing. This option is available only in the *Trace* mode. Choices are:

	45	Trace segments route at 45 degrees.
	90	Trace segments route orthogonally.
	Off	Trace segments route at any angle.
	Relative	Enable (check), to specify if the Line lock angle specified is relative.

Req/Max leg spacing	The required spacing from leg to leg (inner edges) when a physical length is specified (*Lambda/N* unchecked). The maximum spacing from leg to leg (inner edges) when an electrical length is specified (*Lambda/N* checked).
Req/Max leg length	The required length of each leg when a physical length is specified (*Lambda/N* unchecked). The maximum length of each leg when an electrical length is specified (*Lambda/N* checked).
Insert RF Component	Displays the Add Component options enabling you to choose and insert an RF component in-line. ⚠ This option is available only in the **Trace** mode.
Snap to connect point	When checked, snaps to a destination pin within range. If no destination pin exists within range, the router connects to the current mouse position and suggests a dynamic path for you to complete the trace.
Snap to pad edge	When checked, snaps the pin of an RF component to the pad edge of a non-RF component. If this option is disabled or both the components are RF, the pin is snapped to the center of the pad.

Variable line width	When checked, the initial line width is equal to the pad edge in the exit direction. When unchecked, the *Line Width* value is used. ⚠ If this option is checked with *Snap to connect point*, line width value may change automatically if the start point is snapped to a supported object. If you undo the command, the previous line width value is restored.
Taper width difference	When checked, adds a taper at the connect point if widths of the two elements are different.
Physical Length	Displays the physical length of the trace as you route.
Lambda/N	When unchecked, specifies the required leg spacing and length. When checked, specifies maximum leg spacing and length.
Desired electrical lenght	The electrical length of the connection. This option is enabled only if *Lambda/N* is checked.
Working Frequency	Specifies a working frequency for the trace so that RF PCB can calculate and display its electrical length in the *Electrical Length* field as you route.
Electrical Length	Displays the electrical length of the trace as you route.
Initialize clearance	When checked, adds a clearance shape to the RF route.
Add into existing assembly	When checked, adds the clearance shape generated along with the RF route, to the existing clearance assembly

Pop-up Menu Options

Add Via	Adds a via to use for a layer change.
Insert RF component	Enabled when Insert RF component tab is enabled in *Options* panel.
Accurate length	Displays a dialog box to input the length in MILS, MM, MILLIMETERS, and so on. The length is calculated from the start point of the current dynamic path to the destination point. To input an electrical length, lambda should be used.
Clearance Settings	Opens the *Clearance Settings* dialog box to edit the clearance shape settings.
Snap pick to	Activates the available snapping modes. For more information on snapping, see the *Allegro User Guide: Getting Started with Physical Design*.

Related Topics

- Routing a Trace From a New Point

- Inserting an RF Component While Routing

- Routing a Trace From a Supported Object (pin, via, symbol, cline vertex, or shape)

- Connecting Two Points or Components with a Direct Trace

- Connecting Two Points or Components with a Meander Trace

Setting Up for Trace Routing

To set up for trace routing:

1. From the menu bar, choose *RF-PCB — Setup*.
   Alternatively, In the rfedit_appm application mode, right-click and choose Quick Utilities - RF Setup.
   The RF PCB Settings parameters display in the *Options* panel.

2. Select the *Miscellaneous* parameter set.

3. Click on the *RF Routing Mode* drop-down arrow and select a routing mode to use.

4. Right-click on the board and choose *Done*.

5. Choose *RF-PCB — Add Connect*.
   The RF Add Connect options display in the *Options* panel.

6. Select layer, via, ground plane, and other settings.

7. Enter a value for *Line Width* or choose from the drop-down list.

8. Enter a value for *Working frequency* (if electrical length calculation and feedback is desired).

Related Topics

- rf_add_connect

- Inserting an RF Component While Routing

- Routing a Trace From a Supported Object (pin, via, symbol, cline vertex, or shape)

- Connecting Two Points or Components with a Direct Trace

- Connecting Two Points or Components with a Meander Trace

Routing a Trace From a New Point

To route a trace from a new point:

1. Enter a net name in the *Net* field of the RF Add Connect *Options* panel to assign to the starting pin of the route.

2. Select a routing mode: Trace or Meander.

3. Click on a location in the design where you want to start routing the trace.

4. Move your mouse to begin routing the trace, clicking to insert a vertex whenever you want to change direction.

> ⚠ In single segment mode, a bend is followed by a trace. In multi-segment mode, a group of traces and bends are automatically routed using the current bend mode and line lock.

When you click, the previous trace segment becomes fixed and changes to the current layer color.

> ⊘ As you route, right-click to access the extended route options such as *Oops*, *Next, Add Via, and Clearance Settings*. Use the *Next* option when you end the connection on a component and begin the next trace on a different pin.

5. Repeat the previous step until the trace is completely routed, then right-click and choose *Next* from the pop-up menu.

6. Route other RF traces on the board.

7. When completed, click *OK,* or right-click and choose *Done* from the pop-up menu to complete the command.

Related Topics

- rf_add_connect
- RF Add Connect: Options Panel
- Routing a Trace From a Supported Object (pin, via, symbol, cline vertex, or shape)
- Connecting Two Points or Components with a Direct Trace
- Connecting Two Points or Components with a Meander Trace

Inserting an RF Component While Routing

To insert an RF component while routing:

1. Click *Insert RF Component* in the RF Add Connect *Options* panel.
   The Add RF Component options display in the *Options* panel.

2. Choose the type of component to insert.

3. Set the parameters as necessary. You can only place a component on the active layer. Similarly, Snap to Connection is enabled to connect the new component to the current RF route.
   The cursor dynamics of RF component is displayed with pin1 chosen as the current pin.

4. Right-click to choose *Loop Connect Pin Forward* and *Loop Connect Pin Backward* to change the pin to the connect point.
   The net logic and symbol rotation also changes.

5. Alternatively, choose *Pin Connect Pin* to pick the desired pin based on the pin mark on the cursor dynamics.
   The cursor dynamics reflects the changes depending on which pin is selected.

6. Click in the design or right-click and choose *Done* from the pop-up menu to insert the component.

Related Topics

- rf_add_connect
- RF Add Connect: Options Panel
- Setting Up for Trace Routing
- Connecting Two Points or Components with a Direct Trace
- Connecting Two Points or Components with a Meander Trace

Routing a Trace From a Supported Object (pin, via, symbol, cline vertex, or shape)

Follow these steps to route a trace from a supported object:

1. Click on the object where you want to begin routing the trace.
   A start point is automatically chosen along with an angle.

2. Click to turn on *Snap to connect point* and *Snap to pad edge*.
   When you click to start the routing, the tool automatically selects a proper routing layer. If the selected routing layer does not match with the current active subclass, the tool updates the active subclass, alternative layers, ground layers and some of the other global RF parameters.
   For more information, see Automatic layer selection in RF Routing in the *Allegro User Guide: Working with RF PCB*.

3. Move your mouse to begin routing the trace, clicking to insert a vertex whenever you want
   When you click, the previous trace segment becomes fixed and changes to the current layer color.

   > ⊘ As you route, click the right mouse button to access the extended route options such as *Oops, Next, Add Via, and Clearance Settings*. Use the *Next* option when you end the connection on a component and begin the next trace on a different pin.

4. Repeat the previous step until the trace is completely routed, then click the right mouse button and choose *Done* from the menu.

5. Route other RF traces on the board or right-click and choose *Done* to complete the operation.

Related Topics

- rf_add_connect
- RF Add Connect: Options Panel
- Setting Up for Trace Routing
- Routing a Trace From a New Point
- Connecting Two Points or Components with a Meander Trace

Connecting Two Points or Components with a Direct Trace

Perform these steps to connect two points or components with a direct trace:

1. From the menu bar, choose *RF-PCB — Add Connect*.

2. Choose the ground planes above and below the signal.

3. Choose *Trace* for the connection mode, then choose a bend mode.

4. Enter the trace line width or choose from the drop-down list.

5. Enter the frequency.

6. Do one of the following based on what you want to connect.
   Click on the first point in the design to connect, then click on the second point.
   A trace appears directly connecting the two points.
   - or -
   Click on the first component to connect, then click on the second component.
   A trace appears directly connecting the two components beginning and ending on the pins closest to where you clicked on the components.

7. Click the right mouse button and choose *Done* to end the command.

Related Topics

- rf_add_connect

- RF Add Connect: Options Panel

- Setting Up for Trace Routing

- Routing a Trace From a New Point

- Inserting an RF Component While Routing

Connecting Two Points or Components with a Meander Trace

To connect two points or components with a meander trace, follow these steps:

1. From the menu bar, choose *RF-PCB — Add Connect*.

2. Choose the ground planes above and below the signal.

3. Choose *Meander* as the connection mode, then choose the bend mode.

4. Enter values for trace line width or select from the drop-down list.

5. Enter values for frequency.

6. Enter physical length values for *Req Leg Spacing* and *Req Leg Length.*

7. If you want to specify an electrical length for the trace, click (check) the *Lamda/N* option, then enter the electrical length in the *lamda* entry box.

> ⚠ Check the leg spacing and length values again as they are now maximum values for the electrical length rather that physical values.

8. Do one of the following based on what you want to connect.

   a. Click on the first point in the design to connect.

   b. If you are using an electrical length, watch the dynamic readout (*lamda*) in the dialog box as you move your mouse.

   c. Click on the second point.
   A meander trace appears limited by the specified parameters.
   - or -

   d. Click on the first pin in the design to connect.

   e. If you are using an electrical length, watch the dynamic readout (*lamda*) in the dialog box as you move your mouse.

   f. Click on the second pin.
   A meander trace appears limited by the specified parameters.
   Click the right mouse button and choose *Done* to end the command.

Related Topics

- rf_add_connect

- RF Add Connect: Options Panel

- Setting Up for Trace Routing

- Routing a Trace From a New Point

- Inserting an RF Component While Routing

- Routing a Trace From a Supported Object (pin, via, symbol, cline vertex, or shape)

rf_any_angle_bend

The `rf_any_angle_bend` command lets you connect two pins with any angle bend and two MLIN or SLIN segments.

This command calculates possible paths to connect two pads based on the input parameters and displays the shortest dynamic path.This command lets you connect two pads by edge to edge connection and by center to center connection.

Related Topics

- Connecting Two Pins with Any Angle Bend

RF Any Angle Bend Connect: Options Panel

Access Using

- *Menu Path: RF-PCB — Any Angle Bend Connect*

Act	Specifies the active routing layer.
Alt	Specifies the alternate routing layer.
Ground above	Specifies the reference plane above the signal trace (for simulation purposes).
Ground below	Specifies the reference plane below the signal trace (for simulation purposes).
Line Width	*Specifies the width of the trace. Units are determined by the drawing units. This option is disabled if* Variable line width is checked.
Miter Fraction	Specifies the factor used to calculate the bend miter.
Taper Length	Specifies the length of the taper. This option is enabled only if Taper width difference is checked.
Snap to connect point	When checked, snaps to a destination pin. By default, this option is always checked and disabled.
Snap to pad edge	When checked, snaps the pin of an RF component to the pad edge of a non-RF component. If this option is disabled or both the components are RF, the pin is snapped to the center of the pad. This option is enabled only if *Snap to connect point* is checked.
Variable line width	When checked, the initial line width is equal to the pad edge of the exit direction. When unchecked, the *Line Width* value is used for the connection. You cannot change the width of the trace in the *Line Width* field. This option is enabled only if *Snap to connect point* is checked.
Taper width difference	When checked, adds a taper substitution for MLIN/SLIN at the end of connect point. This option is enabled only if *Snap to connect point* is checked.
Initialize clearance	When checked, initializes the clearance for a route.
Add into existing assembly	When checked, adds the clearance from an existing clearance assembly. This option is enabled only if Initialize clearance is checked.

Pop up menu options

Switch	Shows another dynamic path, if exists.
Snap pick to	Activates the available snap pick to in the component mode when Clearance Settings are selected.
Clearance Settings	Opens the Clearance Settings dialog box to edit the clearance settings.

Connecting Two Pins with Any Angle Bend

Perform these steps to connect two pins with Any Angle Bend:

1. From the menu bar, choose *RF-PCB — Setup*.
   Alternatively, In the rfedit_appm application mode, right-click and choose Quick Utilities - RF Setup.
   The RF PCB Settings parameters display in the *Options* panel.

2. Choose *RF-PCB — Any Angle Bend Connect.*
   The RF Any Angle Bend Connect options display in the *Options* panel.

3. Select layer, ground plane, and other settings.

4. Enter a value for *Line width*.

5. Enter a value for *MitterFraction*.

6. Click on a location in the design to choose a start point or pad edge, where you want to start routing the trace.

7. Click on a location in the design to choose an end point or pad edge where you want to end routing the trace.
   If the selection is incorrect, the Allegro X PCB Editor displays an error in the command window. You need to choose the input parameters again.
   If the selection is correct, the shortest dynamic path is shown, if exist.

8. Optionally, enter the new name to remove ratsnest.

9. Right-click and choose *Next* from the pop-up menu.

10. Route other RF traces on the board.

11. When completed, click *OK,* or right-click and choose *Done* from the pop-up menu to complete the command.

Related Topics

- rf_any_angle_bend

rf_autoplace

The `rf_autoplace` command checks the components in your design, attaches new package information to them, and then places them back into the design. This information includes the physical footprint of the components according to parameter values assigned in the schematic.

> ⚠ You need to run the `rf_autoplace` command when you:

- Initially transfer an RF schematic from Design Entry HDL to Allegro X PCB Editor.

- Delete a component symbol in the layout using the PCB Editor delete command.

- Change the accuracy or units of your layout in PCB Editor.

When you run the `rf_autoplace` command, all RF components are grouped according to the logical connectivity. You must specify a component or a group to start the autoplacing process. The tool will auto-place and connect the remaining components within the group based on their logic connectivity. The path of the created RF component is attached to the mouse pointer. You then click at the position in the design to place the RF components within the group. You can repeat this process for the other groups, or manually stop the process using the right-click menu options.

You can also autoplace if your design contain unplaced RF module instances. In this case, the `rf_autoplace` command lets you place the modules first and then continue with RF components. To skip the placement of modules use right-click menu options. You can choose to include components in the modules that are listed in groups for autoplacement.

You can specify a default angle for all two-pin non-RF components for placement during the autoplace process. You can exclude components or specific nets by adding them in the Net exceptions and the Component exceptions parameter sets. For example, to exclude DC nets in the repackage process add them by selecting and adding the nets to the Net Exceptions List using the Net Exceptions parameter set.

To store the current settings for autoplacement you need to save the design when the command is finished. When the `rf_autoplace` command is relaunched, the command restores the settings from the design attachment.

Related Topics

- Autoplacing the RF components in your Design

Autoplace: Options Panel

Access Using

- *Menu Path: RF-PCB — Autoplace*

General parameter set	
Fix selected symbol/pin	If enabled (checked), symbols already placed on the board are displayed with their pin numbers, so that you can select the pin directly. Unplaced symbols are displayed without pin numbers. If this option is checked *Enable rotation for non RF,* and *Additional Relative Rotation* are automatically disabled.
Include components in modules	If enabled (checked), includes components in the hard-reused modules for autoplacement. ⚠ The field is disabled if no hard-reused modules are present in the design.
Ignore FIXED property	If enabled (checked), ignore the FIXED property attached to any object and autoplace it irrespective of the setting.
Zoom to selected symbols	If enabled (checked), the selected group or component is zoomed to fit and displayed in the board. You can zoom in to a specific RF component or group.
Enable rotation for non RF	Predefines a relative rotation angle when discrete devices connect to other components.
Additional Relative Rotation	Specifies the additional angle to rotate the symbol before final placement in the design.
Rotation Lock	Specifies the incremental angle Allegro will rotate the symbol before final placement in the design.
Select Group to start:	Specifies the group or a component within a group for autoplacing. ⊘ The groups and components that are already placed have a "P" denoted on the icon.

Group Filter	Lets you find a group by group name or one component name within the group.
Progress	Displays information about the progress of the autoplace operation.
Start	Activates the autoplace and placement process. You can abort the process using the right-click menu.

Net Exceptions parameter set	
Exclude DC nets in autoplacing	Excludes DC Nets from inclusion in the auto place process.
Net filter	Specifies filtering parameters to restrict the list of net names displayed in the *Available nets* list.
Available nets	Displays all net names based on the filtering criteria you created.
Add nets	Adds net names from the *Available nets* list to the *Net Exceptions List*. If you add all DC nets, *Exclude DC nets in autoplacing* is automatically enabled in the *Options* panel.
Net exceptions list	Displays all net names you want to exclude during the autoplacing process. You can remove net names, clear non-DC nets, or clear all nets from this list using the options described below.
Remove nets	Specifies which net names to exclude from the *Net Exception List*.
Clear non-DC nets	Specifies which non-DC net names to exclude from the *Net Exception List*.
Clear all nets	Specifies the deletion of all net names from the *Net Exception List*.

Component Exceptions parameter set	
Ignore IC components	If enabled (checked), selects the IC components in the *Component exceptions list*.
Ignore IO components	If enabled (checked), selects the IO components in the *Component exceptions list*.

Ignore discrete components	If enabled (checked), selects the discrete components in the *Component exceptions list*.
Component exceptions list	Displays a list of components. The check marks next to the component indicate if the component is selected for exception during the auto place process. You can select or deselect a component by clicking on the check box next to the component.

Pop-up Menu Options

Skip placing current module	Skips the placement of module before autoplacement starts.
Skip placing all modules	Skips the placement of all the modules before autoplacement starts.
Stop	Stops the current autoplace process, but does not exit the command.
Loop connect pin	Changes the pin to connect point by shifting forward to the next pin on the RF component. When you reach the maximum pin number of the component, the looping begins again starting with the first pin.
Pick Fixed Symbol	Picks the desired symbol on the dynamic display of RF component.
Pick Fixed Pin	Picks the desired connect pin on the dynamic display of a RF component.

Autoplacing the RF components in your Design

Follow these steps to autoplace the RF components in your design:

1. From the menu bar, choose *RF-PCB – Autoplace*.
   Alternatively, In the rfedit_appm application mode, right-click and choose Quick Utilities - RF Autoplace.
   The Autoplace options display in the *Options* panel.

2. Customize the auto place process by choosing from the following options (see the Autoplace: Options
   Panel for descriptions).

   - *Fix selected symbol/pin*

   - Include components in modules

   - Ignore FIXED property

   - *Zoom to selected symbols*

   - *Enable relative rotation for Non RF*

   - *Additional Relative Rotation*

   - *Rotation Lock*

3. In the *Net Exceptions* parameter set,

   - Select *Exclude DC Nets in Repackaging*

   - adjust the *Net Filter*, or add or delete net names from the *Net Exceptions List*.

4. In the Component exceptions parameter set,

   - Select components to exclude in the auto place process

5. In the General Parameter set, Click the group or component that you want to use to start placement. You
   can also use *Group filter* to find a group/multiple groups and then select the specific group/component to
   start autoplacement.

6. Click the *Start* button.
   The chosen group attaches to your cursor and a marker appears when you click at the starting point of
   the first RF component. The ratsnests appears if there are connections from this group to the components
   placed in the canvas.
   This message appears in the console window prompt:

   ```
   Enter destination point for the group...
   ```

7. Click the location in the design where you want to place the component.
   The console window prompt displays this message:

   ```
   Enter the rotation angle for the group
   ```

8. Optionally, change the rotation of the component.

The "A" mark is attached for each component of the group in the *Autoplace* pane.

9. Click to place the component in the design.
The tool automatically places and connects the remaining components based on their logic connectivity. After placing the last component, the repackage process is complete. A log file appears describing the status for each RF component.

10. Right-click and choose *Done* to exit the command.You can manually stop the repackaging process at any time by choosing *Done* or *Stop* from the right-click menu, or click *Oops* from the right-click menu to undo the last action.

Related Topics

- rf_autoplace

rf_break

The `rf_break` command lets you break an RF component by the angle of the curvature (in the case of curved components) or the length (in the case of non-curved components). Also, the option to break a component by its electrical length is available only for RF components that support this property.

When breaking a component, you use the break mode Split or Truncate, to either split the component at the breaking point or to truncate the component. In the Truncate mode, the part closer to pin1 is retained and the other part is destroyed.

> ⚠ If you select the rf_break command on an RF component, the fields in the *Options* panel are editable only if the component is breakable. For a list of breakable components see the Breakable RF components list.

Related Topics

- Breakable RF components
- Breaking Components in your Design

RF Break: Options Panel

Access Using

- *Menu Path: RF-PCB — Edit — Break*

Percentage	Choose this option to break the component in percentage terms.
Electrical length	Choose this option to break the component in terms of its electrical length (in lambda).
Length	Choose this option to break the component in terms of its physical length. ⚠ The unit of physical length is determined by the current design unit.
Angle	Choose this option to break the component in terms of the angle of the curve.
Value text boxes	Enter the breaking values in the two value text boxes. The values in these text boxes are assigned to the part of the break depending on the orientation and type of component. When entering the break value in the right and left value text boxes, the left value box specifies the value of the section closer to pin1. For example, if the rotation of a horizontal line is 180 degree, the left value box specifies the value of the right section of the break because the pin1 is on the right side.
Value Trackbar	Use this control to dynamically adjust the breaking values in the value text boxes.
Split	Choose this option to ensure that the component is split into two parts and both the parts are retained on the canvas.
Truncate	Choose this option to ensure that after the command is executed, only the part on the side of pin1 is retained on the canvas. The other part of the break is destroyed.
AutoShove Connected Objects	Choose this option to *ensure* connected components move after you break the component such that any existing connection remain unbroken.
Clearance	Enables Clearance shapes and assemblies. as per the selected option.
Update clearance shapes to default	When selected (enabled), deletes the clearance shapes and removes the existing clearance assembly. It then creates new initial clearance shapes in a new clearance assembly.

Retain clearance shapes	When selected (enabled), retains the original clearance shapes and assemblies.

Pop up menu options

Clearance Settings	Opens the Clearance Settings dialog box to edit the clearance shape settings.

Related Topics

- Breaking Components in your Design

Breakable RF components

The following table describes the RF components types and their effective breaking parameters.

	Percentage	Length	Angle	Electrical Length
MACLIN	P	P	O	O
MACLIN3	P	P	O	O
MCLIN	P	P	O	O
MCURVE	P	O	P	P
MCURVE2	P	O	P	P
MLIN	P	P	O	P
MTAPER	P	P	O	O
SBCLIN	P	P	O	O
SCLIN	P	P	O	O
SCURVE	P	O	P	O
SLIN	P	P	O	O
SOCLIN	P	P	O	O
PCCURVE	P	O	P	O
PCLIN1	P	P	O	O
PCLINn	P	P	O	O
PCTAPER	P	P	O	O
PCTRACE	P	P	O	O

⚠ You cannot use this command to break non-RF components.

Related Topics

- rf_break

Breaking Components in your Design

There are two ways you can break components in your design:

Choose the elements to break

1. From the menu bar, choose *RF-PCB – Edit – Break.*
   The break options display in the *Options* panel.

2. Select an object by clicking on a single RF element.

OR

1. In the rfedit_appm application mode, right-click over the RF element.

2. Choose RF Break from the right-click menu.
   The break options display in the *Options* panel.

Set the break options in the Options panel

1. Choose the breaking parameter:

   ○ Percentage

   ○ Electrical Length (in lambda)

   ○ Length in the case of a LINE component
      OR

   ○ Angle in the case of a CURVE component.

2. In the value text boxes, specify the values of the two breaking sections.
   OR
   Use the track bar to adjust the values of the two breaking sections.

3. Use the Use the *AutoShove Connected Objects to ensure* connected components move after you break
   the component such that any existing connection remain unbroken.

4. Right-click and choose *Done* to complete the command.

Related Topics

- rf_break
- RF Break: Options Panel

rf_chamfer

The `rf_chamfer` command lets you change the bend type on one or more routed RF traces. For example, you can change all curved bends to mitered bends. This command converts all bends on selected traces composed of consecutive RF line segments, RF Bends and other RF components.

For more information, see *RF Routing* in the *Allegro User Guide: Working with RF PCB*.

Related Topics

- Changing the Bend Type on a Routed RF Trace

RF Chamfer: Options Panel

Access Using

- *Menu Path: RF-PCB – Convert – Chamfer*

RF Smooth Type

Curved -> Mitered	Convert all curved bends to mitered bends.
Mitered -> Curved	Convert all mitered bends to curved bends.
Unmitered -> Curved	Convert all unmitered bends to curved bends.
Curved -> Unmitered	Convert all curved bends to unmitered bends.
Unmitered -> Mitered	Convert all unmitered bends to mitered bends.
Mitered -> Unmitered	Convert all mitered bends to unmitered bends.

Miter Fraction

Lets you choose the size for mitered bends.

Clearance

Lets you choose the settings for clearance shapes and assemblies

Update clearance shape to default

Removes existing clearance shapes and assemblies and creates new default clearance shapes.

Retain clearance shapes

Retains the existing clearance shapes.

Pop-up Menu Options

| Chamfer | Performs the desired Chamfer operation on the selected RF objects. |

Changing the Bend Type on a Routed RF Trace

To change the bend type on a routed RF trace, follow these steps:

1. From the menu bar, choose *RF-PCB – Convert – Chamfer*.
   The RF Smoothing options display in the *Options* panel.

2. Choose a smoothing type.

3. If converting to mitered bends, enter a value in the *Miter Fraction* entry box to specify the bend size.

4. Select an option for handling clearances.

5. Click on or drag a window around one or more RF traces.
   All bends on all selected traces are converted as specified.

OR

1. In the rfedit_appm application mode, right-click over the element, or over any one of the group of elements.

2. Choose RF Chamfer from the right-click menu.
   The RF Smoothing options display in the *Options* panel.

3. Choose a smoothing type.

4. If converting to mitered bends, enter a value in the *Miter Fraction* entry box to specify the bend size.

5. Right-click and choose Done.
   All bends on all selected traces are converted as specified.

Related Topics

- rf_chamfer

rf_change

The `rf_change` command lets you resize a selected RF component and edit its parameters and pin-to-net assignments. When you finish editing one component, you can continue to select and edit other RF components.

For details on the allowable value range for component parameters, refer to the specific component in the *Allegro RF PCB Library Reference*.

For the list of component types that can be changed using the rf_change command see Change Component Types. Also, if you are using the line to taper type conversion see the Criterion for Start - End Width Parameters in Line to Taper Type Change.

Related Topics

- Editing Parameters and Pin-to-Net Assignments of an RF Element

- Change Component Types

- Criterion for Start - End Width Parameters in Line to Taper Type Change

RF Change: Options Panel

Access Using

- *Menu Path: RF-PCB – Edit – Change*

> ⚠ Parameter changes may break existing connections of RF components, so use the *AutoShove Connected Objects* option to keep the components connected after you make the changes.

Scaling Factor	Specifies a scale factor to apply to the component whose parameters you are changing.
AutoShove Connected Objects	Enables existing connected components to move after you change the parameters so that they remain connected.
Enable Symbol Rotation	Enables you to rotate the selected object using the mouse pointer.
Enable DRC Check	Enables DRC checking. If changing an object results in a design rule violation, and this option is enabled, the action is reversed. If this option is disabled, the object is placed with a DRC error.
Clearance	Enables Clearance shapes and assemblies as per the selected option.
Update clearance shapes to default	When selected (enabled), deletes the clearance shapes and removes the existing clearance assembly. It then creates new initial clearance shapes in a new clearance assembly.
Retain clearance shapes	When selected (enabled), retains the original clearance shapes and assemblies.

Component Dialog Box

To view the Component dialog box, select the component and then right-click and choose *Show/Hide GUI Form*.

> ⚠ The *Parameters* tab on each component dialog box is composed of a subset of the following fields. For a graphic description of parameters, refer to the component diagram (click *Show Diagram*) in the dialog box.

If the value fields are read-only, it means a variable is associated with that component. Click the display button

beside the grayed-out fields to see the variable name. Use the `rf_varedit` command to edit the variable, and the tool automatically updates the parameters for the component. For additional information on variable editing, see the *Allegro User Guide: Working with RF PCB*.

For additional information on component parameters, refer to the specific component in the *Allegro RF PCB Library Reference*

Parameters Tab

Layer	Specifies the etch subclass for the component.
Ground	Specifies the etch subclass for the reference plane of Microstrip type components.
Ground 1	Specifies the etch subclass for the upper reference plane of Stripline and Macro type components.
Ground 2	Specifies the etch subclass for the lower reference plane of Stripline and Macro type components.
Ref Layer	Specifies the etch subclass for the reference plane of CPW type components.
Begin Layer	Specifies the etch subclass for the pad on the begin layer for Special Via type components.
End Layer	Specifies the etch subclass for the pad on the end layer for Special Via type components.
Layer <n>	Specifies the etch subclass for the <n> conductor for certain Multi-layered type components. <n> is a number.
Pin <n> Net	Specifies the logic name for pin <n> of the component. <n> is a number.
Working Frequency	Specifies the working frequency of Trace type components. This value is used to calculate the approximate electrical length for the trace.
Electrical Length	Displays the calculated approximate electrical length for the component. The value is in lambda units.
Rotation Lock	Specifies the rotation increment when changing the orientation of the component during placement. Choices are:
	Off — Free rotation
	45 — Forty-five degree increments.
	90 — Ninety degree increments.
Coupling Mode	Controls the coupling of two or more components. Choices are:
	Right Coupling — Coupling to the right of the first conductor.
	Left Coupling — Coupling to the left of the first conductor.
Show/Hide Diagram	Controls the display of the component diagram in the dialog box.

Pop-up Menu Options

Loop Pin Forward	Changes the pin to connect point by shifting forward to the next pin on the RF component. The net of the connect pin updates as the pin changes. The net of the connect pin does not change if there are no objects connected at the connect point. When you reach the maximum pin number of the component, the looping begins again starting with the first pin. This option is displayed when you have selected an RF component.
Loop Pin Backward	Changes the pin to connect point by shifting backward to the next pin on the RF component. The net of the connect pin updates as the pin changes. The net of the connect pin does not change if there are no objects connected at the connect point. When you reach the maximum pin number of the component, the looping begins again starting with the first pin. This option is displayed when you have selected an RF component.
Flip Symbol	Flips the symbol geometry of the RF component. Provides flexibility in controlling the physical positioning of the component. You cannot flip a component before you establish the pin to connect point.
Line to Taper	Changes a line type to taper
Line to Gap	Changes a line type to gap
Taper to Gap	Changes taper type to gap
Gap to Taper	Changes gap type to taper
Gap to Line	Changes gap type to line
Taper to Line (N)	Changes taper type to line N indicates that the line width is defined by the width of the narrow end of the taper.
Taper to Line (W)	Changes taper type to line W indicates that the line width is defined by the width of the broad end of the taper.
Show/Hide GUI Form	Choose to toggle the display settings for the edit dialog box specific to the component.

Related Topics

- Change Component Types

- Criterion for Start - End Width Parameters in Line to Taper Type Change

Editing Parameters and Pin-to-Net Assignments of an RF Element

Perform the following steps to edit parameters and pin-to-net assignments of an RF element:

1. From the menu bar, choose *RF-PCB – Edit – Change.*
   The change options display in the *Options* panel.

2. Click on a single element.

3. Change the scaling factor and check *AutoShove Connected Objects.*

4. Click *Enable Symbol Rotation* if you want to change the orientation of the selected object.

5. Click on an RF component to edit in the design.
   The component highlights and if rotation is enabled, an outline displays the new size and orientation of the component.

6. Right-click and choose *Show/Hide GUI Form* to toggle the display settings for the edit dialog box specific to the component.

7. Right-click and choose the component type to change from the available list of component type change options in the menu. For details see Change Component Types.

8. On the *Parameters* tab, enter or change the values in the entry boxes as desired. If necessary, refer to the component documentation in the *Allegro RF PCB Library Reference* for allowable parameter value ranges.

9. On the *Nets* tab, for each pin whose net assignment you need to change, click on its Browser button (right side) and choose a different net from the Data Browser to associate with the pin.

10. When you have finished making changes to the component, indicate this by clicking in an empty area of the design.
    The component loses its highlight and the edit dialog box disappears.

11. Click on another RF component to edit and repeat steps 3, 4, and 5.
    - or -
    Right-click and choose *Done.*

OR

1. In the rfedit_appm application mode, right-click over the RF element.

2. Choose *RF Change* from the right-click menu.
   The change options display in the *Options* panel.

3. To specify the change options in the *Options* panel, perform steps 3 to 8 of the RF PCB menu procedure described above.

4. When you have finished making changes to the component (or components), indicate this by clicking in an empty area of the design.

The component loses its highlight and the edit dialog box disappears.

Related Topics

- rf_change
- Criterion for Start - End Width Parameters in Line to Taper Type Change

Change Component Types

The following table describes the RF component types that can be changed. It also describes the destination type and the command to change the type:

Source Type	Destination Type	Right-click menu Command
MLIN	MTAPER	Line to Taper
PCLIN1	PCTAPER	Line to Taper
PCTRACE	PCTAPER	Line to Taper
MLIN	MGAP	Line to Gap
MGAP	MLIN	Gap to Line
MGAP	MTAPER	Gap to Taper
MTAPER	MGAP	Taper to Gap
MTAPER	MLIN	Taper to Line (N)
PCTAPER	PCLIN1	Taper to Line (N)
MTAPER	MLIN	Taper to Line (W)
PCTAPER	PCLIN1	Taper to Line (W)

Related Topics

- rf_change
- RF Change: Options Panel

Criterion for Start - End Width Parameters in Line to Taper Type Change

When a line is changed to a taper component type, the start and end width parameters are determined using the following criterion:

> ⚠ 2856628566Figure 1-1, Figure 1-2 and Figure 1-3 are used as examples to describe the scenarios.

- The objects connected to the two pins of the line component are selected to calculate the start and end width parameters for the taper. Only symbol and cline segment types of objects are selected. Etch shapes and vias are not considered. In Figure 1-1 there are multiple objects connected to one pin of the MLIN component to be changed to MTAPER. But only the connected MLIN and cline segments are selected for calculation. Vias and etch shapes are not used.

- The connected symbols, if any, are picked out before handling cline segments. Only symbols with physical pin-pin connection with the line component are used. In Figure 1-1, both pins of the MLIN component have RF components connected. The start and end width parameters of the MTAPER would be the conductor width of MLIN and MCURVE, respectively. If the connected symbol is a non-RF component, the pad width or pad height is used as the width parameter. The conversion result is displayed in Figure 1-2.

- If no symbol is connected to the pin of the line, any cline segments connected to the pins are then used for calculation. In the Figure 1-1, if we remove the MLIN component connected to the MLIN to be changed, the cline segments are used to calculate the width. Only the cline segment that has zero connection angle with the MLIN is used. Other cline segments are not used. The conversion result is displayed in Figure 1-3.

- If neither symbol nor cline segment is connected to the pin of the line, the width of the line itself is used for the width parameter. This may lead to a taper with same start and end width parameters. You can then edit the taper to change the width parameters.
  Figure 1.1:
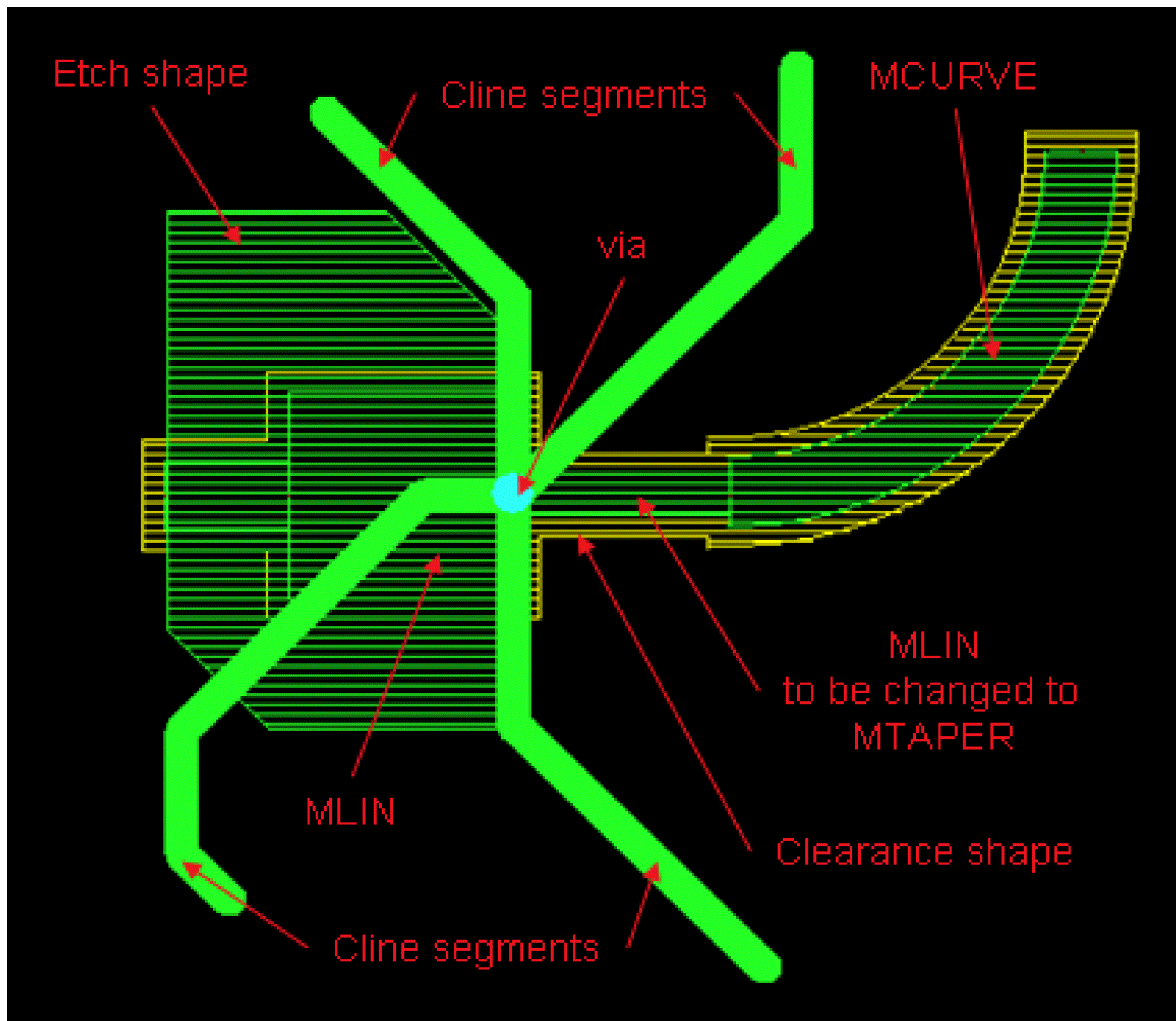
Figure 1.2:
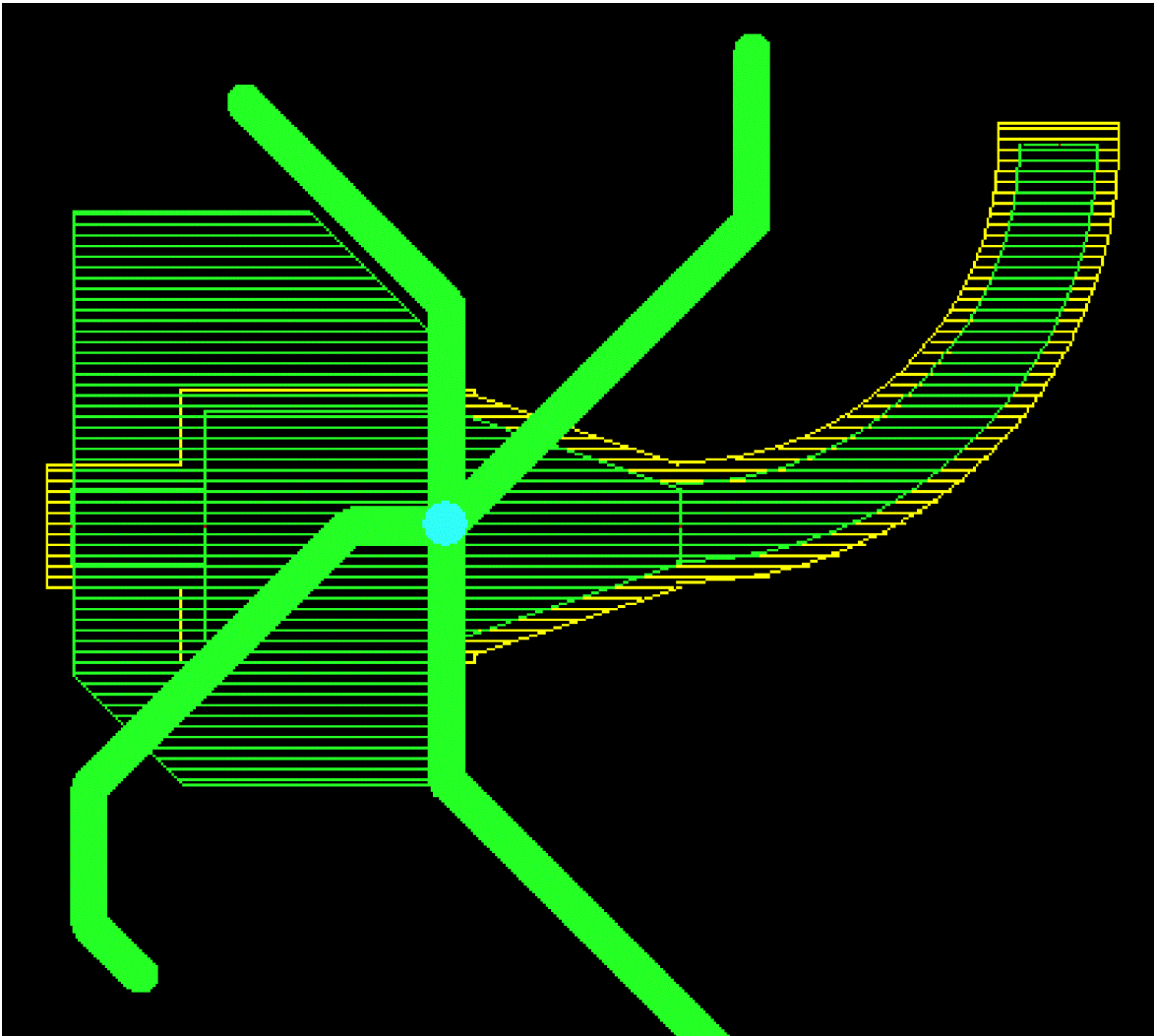
Figure 1.2:
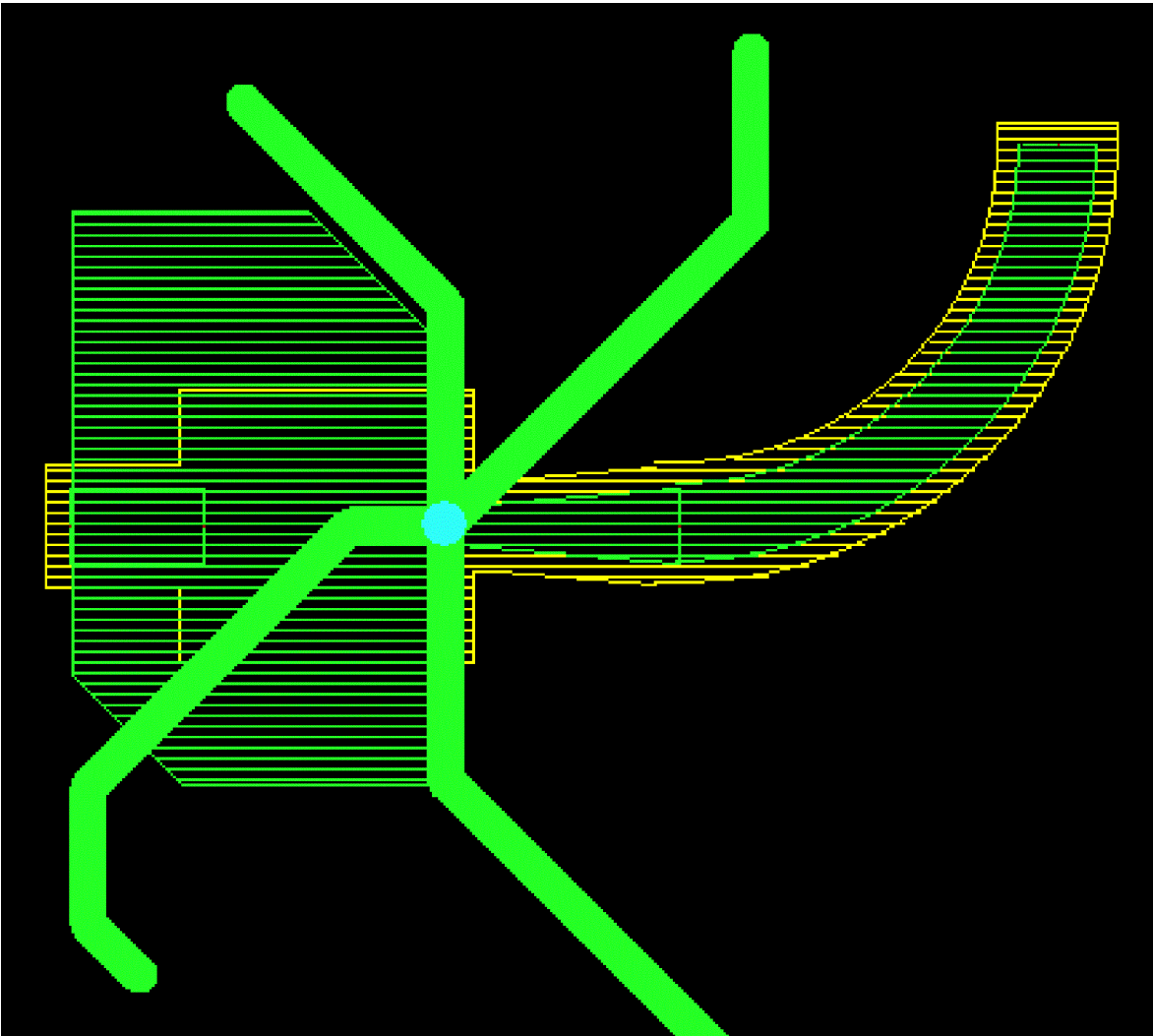
Related Topics

- rf_change
- RF Change: Options Panel
- Editing Parameters and Pin-to-Net Assignments of an RF Element

rf_cline_convert

The `rf_cline_convert` command lets convert clines to compatible RF transmission line components. Cline decomposition will not convert all combinations of RF topological structures. For further information, see RF Post Processing in the *Allegro User Guide: Working with RF PCB.*

Access Using

- *Menu Path: RF-PCB – Convert – Cline to Tline Conversion*

Converting Clines to RF Transmission Line Components

You can convert clines to RF transmission line components by following these steps:

1. From the menu bar, choose *RF-PCB – Convert – Cline to Tline Conversion*.

2. Choose a net that contains clines.
   or
   Right-click and choose *Temp Group* to select more than one net. Choose multiple nets and then click *Complete* when finished.

OR

1. In the rfedit_appm application mode, right-click over the element, or over any one of the group of elements.

2. Choose RF Cline to Tline Covariation from the right-click menu.

The command analyzes the net and converts the clines.

Error Messages

You must choose a net that contains clines or the following error messages appear:

If you choose...

A dummy net	*ERROR (RFC2T-481): Dummy or null net not supported.*
A differential pair net	*ERROR (RFC2T-482): Differential pair net not supported.*
A net that does not contain cline segments	*ERROR (RFC2T-483): Selected net contains no cline segments.*
A net that is not fully routed	*ERROR (RFC2T-484): Only fully routed nets are supported.*
A net that contains unsupported cline topologies	*ERROR (RFC2T-480): Net <netname> contains unsupported cline topologies.*

rf_component2shape

The `rf_component2shape` command lets you convert RF components in your design to shapes. You can select components individually, by drawing a bounding box around them, or you can specify all RF components in the design.

⚠ You can also merge shapes resulting from previously connected RF components. For further information, see RF Editing in the *Allegro User Guide: Working with RF PCB*.

Related Topics

- Converting RF Components to Shapes

RF Component to Shape Dialog Box

Access Using

- *Menu Path: RF-PCB – Convert – Component to Shape*

Conversion Mode

All RF symbols	Converts all RF components in the design to shapes.
By user selection	Converts all RF components that you select individually, or select either wholly or partially within a region that you draw with your mouse.
By logic connectivity	Converts the selected components including their interconnect to shapes.

Merge shapes after conversion

When enabled (checked), merges the shapes of connected components into a single shape.

Delete clearance shapes

When enabled (checked), deletes any clearance shapes or assemblies associated with the RF component.

Pop-up Menu Options

Convert	Performs the desired Convert operation on the selected RF objects.

Converting RF Components to Shapes

Follow these steps to convert RF components to shapes:

1. From the menu bar, choose *RF-PCB – Convert – Component to Shape*.
   The RF Component to Shape options display in the *Options* panel.

2. Choose a conversion mode.

   > ⚠ If you choose *All RF symbols*, all RF components located on etch layers in the design are immediately selected (highlighted) for conversion. Skip the next step.

3. Select components on etch layers to convert.
   The selected components highlight.

   > ⊘ In the Temp Group selection mode, you can de-select RF components by pressing Ctrl key while clicking or window selecting.

4. If you want to merge the shapes of connected components upon conversion, enable (check) the *Merge shapes after conversion* option.

5. Click on the design canvas or right-click and choose *Convert*.
   The components are converted to shapes.

6. Repeat steps 2 through 5 to convert other components.
   - or -
   Click the right mouse button and choose *Done* to complete and exit the command.

OR

1. In the rfedit_appm application mode, right-click over the element, or over any one of the group of elements.

2. Choose RF Component to shape from the right-click menu.
   The RF Component to Shape options display in the *Options* panel.

3. If you want to merge the shapes of connected components upon conversion, enable (check) the *Merge shapes after conversion* option.

4. Select components on etch layers to convert.

Related Topics

- rf_component2shape

rf_delete

The `rf_delete` command lets you remove RF components from your design. You can select components individually by clicking on them or by drawing a bounding box around them. The Temp Group selection mode is also available.

> ⚠ This command does not operate on non-RF elements.

> ⓘ This command permanently deletes selected RF components from the design database. If you only want to remove their package symbol from the design, use the existing PCB Editor delete command. However, be aware that you may need to repackage the component after deleting its symbol in order to use it again in your design.

Access Using

- *Menu Path: RF-PCB – Edit – Delete*

Deleting RF Elements

Perform the following steps to delete RF elements:

1. From the menu bar, choose *RF-PCB – Edit – Delete.*
   A prompt asks you to select RF elements in the design.

2. Delete individual RF elements by clicking on them.
   - or -
   Delete several RF elements by drawing a bounding box around them (hold the left mouse button and drag).
   The RF elements disappear from the design window.

3. Repeat step 2 until all desired RF elements are removed from the design.

4. Click the right mouse button and choose *Done* to end the command.
   - OR -
   Click the right mouse button and choose *Oops* to undo the removal of the last RF element.
   - OR -
   Click the right mouse button and choose *Cancel* to reverse the entire delete operation.

OR

1. In the rfedit_appm application mode, right-click over the element.
   OR
   To delete several RF elements draw a bounding box around them (hold the left mouse button and drag) and right-click over any one of the selected elements.

2. Choose RF Delete from the right-click menu.

To reverse the entire delete operation, choose Edit - Undo.

rf_display_info

The `rf_display_info` command lets you display property information for selected RF elements in your design. You can select elements individually, or by drawing a bounding box around them. You can also use the Temp Group selection mode.

Access Using

- *Menu Path: RF-PCB – Display – Information*

Displaying RF Elements Property Information

Perform the following steps to display the property information of RF elements:

1. From the menu bar, choose *RF-PCB – Display– Information*.
   You are prompted to select one or more RF elements.

2. Select objects by clicking on a single element or holding the left mouse button and drag a bounding box around several elements. You can also use the Temp Group selection mode.
   A Text Display dialog box appears with property information for all selected elements.

3. Read the information, then choose *Close* to dismiss the dialog box.

OR

1. In the rfedit_appm application mode, right-click over the element, or over any one of the group of elements.

2. Choose RF Display Information from the right-click menu.
   A Text Display dialog box appears with property information for all selected elements.

3. Read the information, then choose *Close* to dismiss the dialog box.

> ⊘ You can save the information to a file or send it to a printer by choosing *File – Save As* or *File – Print* from the menu bar of the dialog box.

rf_display_newcomp

The `rf_display_newcomp` command lets you view newly introduced RF components by highlighting all of them in your design using the default permanent highlight color. This helps you distinguish between new RF components and existing ones. A RF component is said to be a new one if it has the RFNEWCOMP property. The permanent highlight color can be changed in the Color dialog box. If you choose, you can also use the command to dehighlight them by removing their RFNEWCOMP property.

⚠ Newly created RF components automatically have the RFNEWCOMP property attached to them.

🛈 Dehighlighting cannot be undone.

Related Topics

- Displaying Newly Introduced Components

RF Display New Component Options Panel

Access Using

- *Menu Path: RF-PCB – Display – New Components*

Highlight	Highlights all new components when first placed on the board. When checked, the selection modes are not available.
Highlight color	Displays the highlight color. Click the color box to show the *Assign Color* dialog box, using which you can set the highlight color.
Dehighlight	Dehighlightes and removes the RFNEWCOMP property from the selected new RF components.
Selection mode:	
All new RF components	Dehighlights all new RF components.
By user selection	Dehighlights new components by user selection.

Displaying Newly Introduced Components

to display the newly introduced components in your design:

1. Choose *RF-PCB – Display – New Component*.
   The Highlight and dehighlight options are displayed in the *Options* panel.
   By default *Highlight* operation mode is enabled, and all new components in the design are highlighted.

2. Click *Dehighlight* and choose which option you want to use to select the components:

   - *All new RF components*

   - *By user selection*

3. Click in the design and choose the components to dehighlight.

4. When you are finished, right-click and choose *Done* from the pop-up menu.
   A message appears, warning you that dehilighting the components cannot be undone and may have severe impact on synchronization between the schematic and the layout.

Related Topics

- rf_display_newcomp

rf_flip

The `rf_flip` command lets you flip and rotate the geometrics of the selected objects using supported flip and rotate modes.

For additional information, see Editing Groups of Objects in the *RF PCB User Guide.*

Related Topics

- Flipping RF Elements

RT Flip: Options Panel

Access Using

- *Menu Path: RF-PCB — Edit — Flip*

Enable DRC Check	When checked, checks for DRC errors immediately after a flip/rotation action. If any DRC errors are found, the action is cancelled.
Ignore Fixed Property	Specifies that fixed objects can flip or rotate when checked.
Flip Axis Mode	Click to choose a mode from the pull-down list of all supported flip axes.
Pick Segment for Axis	When checked, allows you to select a line segment as the flip axis.
Rotation Type	Specifies the pre-defined rotation type used for rotating selected objects.
Rotation Angle	Specifies the pre-defined rotation angle used for rotating selected objects.
Include Clearance Assembly	When checked, if any selected object is a member of some clearance assembly, all the objects in that clearance assembly are selected for flipping and rotation.

Right Mouse Button Menu Options

Rotate	Activates the rotation options you specified. You provide a point for the origin of the rotation. You can perform *Rotate* before and after you flip the group of objects. This option is only available after you have selected the objects.
Snap to	Activates the available snapping modes.
Clearance Settings	Opens the Clearance Settings dialog box to edit the clearance shape settings.

Flipping RF Elements

You can flip RF elements in two ways:

Choose the elements to flip

1. From the menu bar, choose *RF-PCB – Edit – Flip.*
   The flip options display in the *Options* panel.

2. Select objects by clicking on a single element or holding the left mouse button and drag a bounding box around several elements. You can also use the Temp Group selection mode.

OR

1. In the rfedit_appm application mode, right-click over the element, or over any one of the group of elements.

2. Choose RF Flip from the right-click menu.
   The flip options display in the *Options* panel.

Set the flip options in the Options panel

1. Select the check boxes that apply:
   Enable DRC Check - check this to run a check for errors.
   Ignore Fixed Property - check to specify that fixed objects can flip or rotate.
   Include Clearance Assembly - check to flip the clearance assembly.

   > ⚠ If you set *Flip Axis Mode* to *Diagonal Line* or *Odd Line*, you are prompted to specify the start point of the axis line.

   ```
   Enter first point for the flip axis...
   ```
   A dynamic view of the flip axis displays.

2. Optionally, right-click and choose *Rotate* to specify the rotation options. The rotation options become enabled in the *Options* panel.
   Enter values in the *Rotation Type* and *Rotation Angle* fields in the *Options* panel.

   > ⚠ The rotation operation is only available after you select the group of objects. If *Rotation Type* is set to Absolute, the rotation action performs immediately after you provide the origin. If *Rotation Type* is set to Incremental, you are prompted to enter the angle for the rotation.

   If *Pick Segment for Axis* is on, you are prompted to pick a line segment.
   ```
   Pick a line segment as the flip axis...
   ```
   If you pick an arc segment, an error message appears.
   ```
   E – (SPRFPC-190): Operation not applicable on arc segment.
   ```

3. Click on the design canvas to perform the flip action.

4. Right-click and choose *Done* to accept the changes and exit the command, or *Next* to start a new flip session.

You can only flip an object on the same layer. You cannot create a new package symbol during the flipping process.

Related Topics

- rf_flip

rf_group_add

The `rf_group_add` command lets you add RF components to a group for autoplacement. You can select components individually, or by drawing a bounding box around them. You can also use the Temp Group selection mode. The RFGROUP property is added to the selected components.

This command also creates a generic group of components and add the selected components to it.

For additional information, see Grouping functionality for autoplace in the *RF PCB User Guide.*

Access Using

- *Menu Path: RF-PCB – Group – Add*

Adding RF Components to a Group

To add RF components to a group, perform the following steps:

1. From the menu bar, choose *RF-PCB – Group – Add.*
   The Group Name displays in the *Options* panel.

OR

1. In the rfedit_appm application mode, right-click over the RF element.

2. Choose RF Add group from the right-click menu.
   The Group Name displays in the *Options* panel.

3. Select objects to add into RF group by clicking on a single element or holding the left mouse button and drag a bounding box around several elements. You can also use the Temp Group selection mode.

4. Enter a new group name in the *Options* panel.
   The selected RF group is highlighted.

5. Alternatively, choose an existing RF group from the drop-down list. A warning message is displayed to check if a generic group with the same name exists or not.

   a. Click *Yes* to add components to the generic group.

   b. Click *No* to specify a new group name.

6. Click at the canvas to confirm.
   The selected components are added to the group.

7. Right-click and choose Done from the pop-up menu.

rf_group_copy

The `rf_group_copy` command lets you copy groups of selected objects and move them to another location in your design. You can select components individually, or by drawing a bounding box around them. You can also use the Temp Group selection mode. Component copies are generated with reference designators and have the same parameters as the originals. You can perform other actions on the copied components before or after the copy operation by choosing *Flip*, *Rotate*, or *Snap* from the right-click pop-up menu.

For additional information, see Editing Groups of Objects in the *RF PCB User Guide.*

Related Topics

- Copying a Group of Objects

RF Group Copy Command: Options Panel

Access Using

- *Menu Path: RF-PCB – Edit – Copy*

Enable DRC Check	When checked, checks for DRC errors immediately after a copy action. If any DRC errors are found, the action is cancelled.
Ignore Fixed Property	Specifies that fixed objects can flip or rotate when checked.
Reference Layer	Displays the uppermost layer of the selected group of objects.
Destination Layer	Displays the available etch layers for the destination of the selected group of objects.
Flip Options	
Flip Axis Mode	Click to choose a mode from the pull-down list of all supported flip axes.
Pick Segment for Axis	When checked, allows you to select a line segment as the flip axis.
Rotation Options	
Rotation Type	Specifies the pre-defined rotation lock angle used for incremental rotation or as the rotation angle for absolute mode.
Rotation Angle	Specifies the pre-defined rotation angle used when rotation is required.
Include clearance assembly	Enable (check), to use clearance assembly rather than parts of its members for copy and related actions.

Right Mouse Button Menu Options

Flip	Flips the group of objects according to the flip options you set. You can perform *Flip* before and after you copy the group of objects.
Rotate	Activates the rotation options you specified. You provide a point for the origin of the rotation. You can perform *Rotate* before and after you copy the group of objects.
Snap to	Activates the available snapping modes.

Copying a Group of Objects

You can copy a group of objects is multiple ways:

Choose the elements to copy

1. From the menu bar, choose *RF-PCB – Edit – Copy.*
   The copy options display in the *Options* panel.

2. Select objects by clicking on a single element or holding the left mouse button and drag a bounding box around several elements. You can also use the Temp Group selection mode.

OR

1. In the rfedit_appm application mode, right-click over the RF element, or over any one of the group of elements.

2. Choose RF Grouped Copy from the right-click menu.
   The copy options display in the *Options* panel.

Set the copy options in the Options panel

1. Check the check boxes that apply:
   Enable DRC Check - check this to run a check for errors.
   Ignore Fixed Property - check to specify that fixed objects can flip or rotate.

2. Optionally, right-click and choose *Flip.* Choose values for the *Flip axis mode* and *Pick segment for axis*.

   > ⚠ If you set *Flip Axis Mode* to *Diagonal Line* or *Odd Line*, you are prompted to specify the start point of the axis line.

   ```
   Enter first point for the flip axis...
   ```
   A dynamic view of the flip axis displays.

3. Optionally, right-click and choose *Rotate*. Enter values in the *Rotation Type* and *Rotation Angle* fields. The rotation operation is only available after you select the group of objects. If *Rotation Type* is set to *Absolute*, the rotation action performs immediately after you provide the origin. If *Rotation Type* is set to *Incremental*, you are prompted to enter the angle for the rotation.
   If *Pick Segment for Axis* is on, you are prompted to pick a line segment.
   ```
   Pick a line segment as the flip axis...
   ```
   If you pick an arc segment, an error message appears.
   ```
   E - (SPRFPC-190): Operation not applicable on arc segment.
   ```

4. Click on a point near or directly on the component or component group you are copying.
   Copies of the components attach to your cursor (at the source point), and you are prompted to enter a destination point.

5. Drag the component copies to their destination in your design and click to place them.

6. Right-click and choose *Done* from the pop-up menu to complete the copy session.

> ⚠ You can only copy an object on the same layer. You cannot create a new package symbol during the copy process.

Related Topics

- rf_group_copy

rf_group_disband

The `rf_group_disband` command lets you disband the RF group. The generic group is disbanded as well.

This command removes RFGROUP property from each component of the group.

For additional information, see Grouping functionality for autoplace in the *RF PCB User Guide.*

Access Using

- *Menu Path: RF-PCB – Group – Disband*

Disbanding an RF Group

To disband an RF group:

1. Choose *RF-PCB – Group – Disband.*
   The Group Name displays in the *Options* panel.

OR

1. In the rfedit_appm application mode, right-click over the RF element.

2. Choose RF Disband group from the right-click menu.
   The Group Name displays in the *Options* panel.

3. Choose any existing RF group or ALL from the drop-down list in the *Options* panel.
   All the members of the RF group are highlighted.

4. Alternatively, choose any existing RF group from the design canvas.
   All the members of the RF group are highlighted.

5. Click at the canvas to confirm.
   The RFGROUP property is removed from each component of the group.

6. Right-click and choose Done from the pop-up menu.

rf_group_exclude

The `rf_group_exclude` command lets you remove a RF component from a particular group. The selected component is also removed from the generic group. This command removes RFGROUP property from the excluded components.

For additional information, see Grouping functionality for autoplace in the *RF PCB User Guide.*

Access Using

- *Menu Path: RF-PCB – Group – Exclude*

Removing an RF Component from a Group

To remove an RF component from a group:

1. Choose *RF-PCB – Group – Exclude.*

2. Select components to remove from the RF group by clicking on a single element or holding the left mouse button and drag a bounding box around several elements. You can also use the Temp Group selection mode.

OR

1. In the rfedit_appm application mode, right-click over the RF element.

2. Choose RF Exclude group from the right-click menu.

3. Click at the canvas to confirm.
   The RFGROUP property is removed from the selected components. The selected components are removed from the generic group as well.

4. Right-click and choose Done from the pop-up menu.

rf_group_info

The `rf_group_info` command shows information of the selected RF group. This command displays a dialog box that contains detail information of all the members of the selected group.

For additional information, see Grouping functionality for autoplace in the *RF PCB User Guide.*

Access Using

- *Menu Path: RF-PCB – Group – Display*

Displaying Information for Selected RF Group

To display the information for selected RF groups, perform these steps:

1. From the menu bar, choose *RF-PCB – Group – Display.*
   The Group Name displays in the *Options* panel.

OR

1. In the rfedit_appm application mode, right-click over the RF element.

2. Choose RF Display group from the right-click menu.
   The Group Name displays in the *Options* panel.

3. Select any existing RF group or ALL from the drop-down list in the *Options* panel.
   All the components of selected group are highlighted.

4. Click on the canvas to confirm.
   The RF Group Information dialog box is displayed.

> ⚠ If any component is added to the generic group, a warning message is displayed. Click *OK* to display the RF Group Information dialog box.

1. Right-click and choose Done from the pop-up menu.

rf_iff_export

The `rf_iff_export` command lets you translate a portion or an entire RF PCB design to an IFF formatted file. Once translated to IFF, you can then import the design file into ADS or MWO Layout to perform EM simulation using Momentum.

This command exports components, lines, shapes, and vias.

⚠ If a design includes any negative planes, they are converted to positive planes as negative planes are not recognized during an ADS or MWO simulation.

Related Topics

- Translating an RF PCB Design to an IFF Formated File

RF IFF Export Command Dialog Boxes

Access Using

- *Menu Path: RF-PCB – IFF Interface – Export*

RF IFF Export Mode	RF IFF Export Layer Map
RF IFF Export	RF IFF Export Options

RF IFF Export Mode Dialog Box

Export All	Translates all components, shapes, lines, clines, vias, pads and discrete components to IFF.
Export All RF Components	Translates all RF components to IFF.
Export Region	Translates all components, shapes, lines, clines, vias, pads and discrete components captured within a bounding box to IFF.
Cut Shape	Exports a shape or a partial shape. This option is only available when exporting a region. Shapes along with other elements for exporting highlight when they fall completely within the selected region. If you are exporting only part of a shape, a dynamic path indicates which part of the shape will export.
Export Selection	Translates all components, shapes, lines, clines, vias, pads and discrete components that you select individually to IFF. Note: To de-select an element, click on it again.
Export Connectivity	Translates all components, clines, and discrete components associated with nets that you select to IFF. Note: Only the connected pad of a digital component is exported. All elements connected to all RF components are exported.

RF IFF Export Dialog Box

IFF Directory	The directory path where the generated IFF export file is stored.
Export Stackup	When enabled (checked), exports the board stackup to the IFF directory as *board _name*.slm. ⚠ This option is disabled when your design contains MWO components.
Export Format	Choose to select the export format as ADS or MWO from the pull-down list when current RF library is set to *CDN Unified*.
Discrete component name mapping	When enabled (checked), renames the discrete components to be consistent with Allegro Discrete Library Translator. ⚠ This option is enabled only if discrete components are selected for export. ⚠ This option is disabled when your design contains MWO components.
Layer map	Displays the RF Layer Map dialog box to let you map layers in the translated design to layers in ADS or MWO Layout.
More options	Displays the RF IFF Export Options dialog box to let you fine tune the IFF translation parameters for specific RF elements.

RF IFF Export Layer Map Dialog Box

New layer map mode (ADS)	Adds options to modify Allegro to ADS layer mapping file. This option is disabled when MWO export format is selected.
Layer in Allegro	The layers in your design.
Layer in ADS/MWO	The layers in ADS/MWO to which each layer in your design maps.
Add	Adds additional ADS layer names to which to map. ⚠ This option does not exist if you export a design with MWO components. The MWO uses the same layers as they are defined in the Allegro.

RF IFF Export Options Dialog Box

Object	Design objects to translate.
Transfer	When enabled (checked), translates the named object to IFF. You can right-click the column head and choose *Select All* or *Deselect all* to change all the items in the column.
Transfer Mode	The translation mode for the named object. You can right-click the column head and choose options *Change all to...* to change mode for all the items in the column.
Arc resolution	The arc resolution for translated curved shapes.
Export static shape	Check to export a dynamic shapes as static, complete shapes. If unchecked only shape boundaries are exported. This option is only available when a dynamic shape is selected for export.
No prompt when changing transfer mode	When enabled (checked), turns off confirmation pop-ups when translating elements to non-default types.
Via group name	Specifies the parameter Via group name in ADS. The value of this field is the same as the Via group name field when exporting padstacks to ADS. The default value is the design name. ⚠ This option is disabled for MWO designs.

Translating an RF PCB Design to an IFF Formated File

To export your RF design to IFF, the procedure is same for both ADS- and MWO- compatible designs:

1. From the menu bar, choose *RF-PCB – IFF Interface – Export*.
   Alternatively, In the rfedit_appm application mode, right-click and choose Quick Utilities - RF IFF export.
   The RF IFF Export Mode dialog box appears.

2. Choose an export mode.

   ⊘ If you want to export visible elements to IFF, be certain to make the etch class or pin class visible for those elements before selecting them.

3. Select the elements to export based on the export mode you chose.
   The selected components highlight.

   ⊘ If you previously selected *Export Selection*, you can de-select components by clicking on them again.

   ⊘ You will be unable to select objects placed on negative planes. ADS/MWO is unable to process objects placed on negative planes; to use such objects convert such planes to positive before selecting objects on it.

4. Click *OK.*
   The RF IFF Export dialog box appears.

5. In the *IFF Directory* text box, enter the path name to write the generated IFF export file to.
   - or -
   Click the Browse button to choose a directory using a file browser.

   ⚠ The default directory for writing IFF export files to is: *your_working_directory*/IFF

6. If you want to export the stackup for your design to simplify simulation setup in ADS, enable (check) the *Export Stackup* option and specify the path name for the stackup export (.slm) file.

   ⚠ The default directory for writing stackup export files is: *your_working_directory* – IFF

7. Choose *Export Format.*

   ⚠ This option is enabled only if the *CDN Unified* library is set for the design.

8. Check the *Discrete component name mapping* check box to rename the selected discrete components to

be consistent with Allegro Discrete Library Translator after export

> ⚠ This option is enabled only if you have selected discrete components for export.

9. If you opted not to export your board stackup in the previous step, you can use the following sub-procedure to map layers in your design to layers in ADS Layout. Otherwise, proceed to the next step.

   a. Click *Layer map*.
   The RF IFF Export Layer Map dialog box appears.

   b. Optionally, enable the *New layer map mode (ADS)* option to modify layer information.
   Two new buttons *Edit* and *Reset* are added to the dialog box for editing layer mapping file.

   c. In the *Layer in ADS* column, click the drop-down arrow in each row to select an alternate layer in ADS to map the Allegro layer to.

   > ⚠ Optionally, you can click *Add*, to add names of other layers in ADS to the choice list.

   d. Click *OK* to dismiss the dialog box.

10. Optionally, use the following sub-procedure to fine tune the IFF translation parameters for specific RF elements. Otherwise, proceed to the next step.

   a. Click *More options*.
   The RF IFF Export Options dialog box appears.

   b. In the *Transfer* column on each tab, click the check box to enable or disable the transfer of the named object to IFF. Be sure to select the *Transfer Mode* if enabling transfer.

   c. Optionally, enter an alternate value in the *Arc resolution* text box to control the display of curved objects in ADS. Otherwise, proceed to the next step.

   d. Optionally, enable the *No prompt when changing transfer mode* option to turn off confirmation pop-ups when translating elements to non-default types. Otherwise, proceed to the next step.

   e. Click *OK* to dismiss the dialog box.

11. Click *OK* at the bottom of the RF IFF Export dialog box to start the export translation.
    The IFF translation files generate and a message dialog box appears asking if you want to view the translation report. Click *Yes* or *No*.
    - or -
    The export fails and you receive a warning message at the bottom of the RF IFF Export dialog box.

After a successful export, you must save the board to update the design from ADS.

Related Topics

- rf_iff_export

rf_iff_import

The `rf_iff_import` command lets you import an IFF layout and schematic file in Allegro X PCB Editor. You can import IFF using the following mode:

- Importing an IFF Design into Allegro X PCB Editor

> ⓘ When importing IFF, Allegro X PCB Editor uses the current resolution and units for all elements. To maintain the correct precision of the Allegro database, if some of the incoming IFF elements cannot be changed during import, the import process will abort. In this case, you will need to change the resolution and units of the incoming IFF design manually and then retry the IFF import.

When you change units, also change accuracy to maintain adequate precision within the database. Reference the following table to determine the appropriate accuracy.

Units	Min Accuracy	Max Accuracy	Delta
mils	0	4	0 (more then 2 not advised due Gerber)
inches	2	4	3
microns	0	4	0
millimeters	1	1	3
centimeters	2	2	4

- Decreasing accuracy is not recommended.
- Switching units between Metric and English is not recommended due to inevitable rounding issues.
- Use the new delta to decide what the accuracy should be when changing units.

> ⓘ When importing IFF form ADS, Allegro X PCB Editor maps the pcbVia component to the existing generic via with the specified padstack according to its parameter.

Related Topics

- Importing an IFF Design into Allegro X PCB Editor

RF IFF Import Dialog Boxes

Access Using

- *Menu Path: RF-PCB – IFF Interface – Import*

RF IFF Import	RF IFF Layer Map

RF IFF Import Dialog Box

Layout IFF file	Specifies the IFF RF design file to import into Allegro X PCB Editor.	
Schematic IFF file	Specifies the IFF schematic file to use for importing.	
Import Stackup	When enabled (checked), imports the specified IFF stackup file into Allegro.	
Import Mode	Specifies how to import the IFF design. Choices are:	
	new design	Imports IFF into a new board as a new design.
	insert	Imports IFF into the current board as new data.
	update	Imports IFF into the current board as an update.
Copy current stackup	When enabled (checked), copies the stackup from the current design, if you import into a new design. This option is only displayed if the *Import Mode* is *new design*.	
Layer Map	Displays the RF Layer Map dialog box to let you map layers in ADS Layout to layers in the translated design.	
OK	Click to start the import process.	

RF IFF Layer Map Dialog Box

Layer in ADS	The layers in the IFF design.
Transfer	When enabled (checked), specifies that elements in the corresponding ADS layer transfer to Allegro.
Class	The class in Allegro that contains the layer to be mapped to the ADS layer.
Subclass	The layers in Allegro to which each layer in the IFF design maps.

Importing an IFF Design into Allegro PCB Editor

Perform the following steps to import an IFF design:

1. From the menu bar, choose *RF-PCB – IFF Interface– Import*.
   Alternatively, In the rfedit_appm application mode, right-click and choose Quick Utilities - RF IFF import.
   The RF IFF Import dialog box displays.

2. In the *Layout IFF file* text box, enter the pathname of the IFF layout file to import.
   -or-
   Click the *Browse* button to choose the layout file using a file browser.

   > ⚠ The default directory for IFF design files is: *your_working_directory* – `IFF`

3. Some necessary information may only exist in the schematic, so you need to import the schematic file as well. Enter the pathname of the schematic file to import.
   -or-
   Click the *Browse* button to choose the schematic file using a file browser.

4. If you also want to import the stackup for the IFF design, enable (check) the *Import Stackup* option and specify the pathname to the new design (`.slm`) file.

   > ⚠ By default, this file should be in the same directory as the (`.iff)` file.

   -or-
   Click *Copy current stackup*, if you are importing into a new design and want to keep the current stackup information.

5. If you opted not to import the stackup in the previous step, use the following sub-procedure to map layers in ADS Layout to layers in your design. Otherwise, proceed to the next step.

   a. Click *Layer map*.
      The RF IFF Layer Map dialog box appears.

   b. In the *Class* column, click the drop-down arrow in each row to select a class containing the layer in Allegro to map the ADS layer to.

   When you select a class, the *Subclass* drop-down is populated with the layers corresponding to the class you select in the *Class* column.

   a. In the *Subclass* column, click the layer to map the ADS layer to.

   b. Click *OK* to dismiss the dialog box.

6. Click *OK* at the bottom of the RF IFF Import dialog box to start the import process.
   If you are creating a new design or inserting into the current design, the IFF design appears on your

cursor and is ready for placement on the board.
-OR-
If you are updating the current design, the elements to update highlight in your design window. Click somewhere in the design window to start the update.

> ⚠ If the import failed and a warning message appears at the bottom of the RF IFF Import dialog box, fix the problem and retry.

If the import is successful, a message dialog displays asking if you want to import the schematic design as well.

7. T*o import the* IFF *schematic file*, use the following sub-procedure. Else, only the layout file imports.

   a. Click *Yes* in the prompt dialog box.
      The RF-PCB Schematic IFF Import dialog box appears.

   b. Click *Next* to continue the import process.
      If non-parameterized RF components exist in the design, a window appears displaying the symbol mapping.

   c. Click *Next* to continue.
      A dialog box appears displaying the results of the symbol mapping and import of the schematic design.

   d. Click *Finish* to complete the import process.
      Design Entry HDL launches, and you can add the imported block to the schematic design area.

   After the import procedure is complete, you are prompted to view the Report file.

8. Click Yes to view the report.

> ⚠ This prompt displays if you choose to import only the layout or both the layout and the schematic. The prompt also displays if the import procedure encountered an error in the schematic import process.

Import as a New RF Design

When you import IFF as a new design, you should also import the stackup file for the design (if possible), otherwise you will need to perform layer mapping between ADS and Allegro as part of the import process. You are given the opportunity to choose the name of the new design. Upon doing so, the new design is automatically opened in Allegro X PCB Editor and ready to accept the placement of the IFF import.

> ⚠ The tech file of the current design is used in the new design, if you did not check the *Import Stackup* option.

Import as an RF Insertion into an Existing PCB Design

When you insert IFF into an existing Allegro PCB design, be aware that some extra (non RF) elements may be introduced with the import.

Import as an Update to an Existing Mixed-signal RF PCB Design

This option is only available if you started the original design in Allegro X PCB Editor, exported RF components to ADS for simulation and optimization, and are now back-annotating the changes to Allegro X PCB Editor. When the import takes place, element correspondency is checked and only matching elements between Allegro and ADS receive the update.

Related Topics

- rf_iff_import

rf_libxlator

The `rf_libxlator` command lets you translate the layout and schematic information of surface mount parts before transferring the design from ADS to Design Entry HDL/Allegro enabling you to store and use them in the local library.

ⓘ SMT library translator is supported only on Windows OS.

Related Topics

- SMT Library Layer Mapping Dialog Box
- SMT Library Translator - Library Dialog Box
- SMT Library Translator - Components Dialog Box
- Setting Up the SMT Library Translator
- Changing Part Types in the SMT Library Translator - Library Dialog Box
- Changing Package Names in the SMT Library Translator - Components Dialog Box

SMT Library Translator - Setup Dialog Box

Access Using

- Menu Path: *RF-PCB – IFF Interface – SMT Library Translator*

-

Path	
Input Schematic IFF File	Specify the name of the schematic IFF file that you are importing or browse to choose a file.
Input Layout IFF File	Specify the name of the layout IFF file that you are importing or browse to choose a file.
Output Library Directory	Specify the name of the library directory that you are exporting or browse to choose a directory. A `chips`, `sym_1`, `entity` and `part_table` subdirectory are also part of this directory and each translated library symbol has a JEDEC_TYPE property.
Output Package Symbol Directory	Specify the name of the package symbol directory that you are exporting or browse to choose a directory.
Output Padstack Directory	Specify the name of the padstack directory that you are exporting or browse to choose a directory.
Option	
Overwrite existing paths	Click to overwrite existing parts during the import process and turn off the message prompt.
Schematic IFF only	Click to clear the *Input Layout IFF File* field and choose the footprint symbols in mapping mode.
Layer Map	Displays the SMT Library Layer Mapping Dialog Box that lets you change the layer mapping relationships between ADS and Allegro.
Next	Displays the SMT Library Translator - Library Dialog Box.
Cancel	Exits the dialog box without saving any changes.

Related Topics

- SMT Library Translator – Library Dialog Box

- SMT Library Translator – Components Dialog Box

- Setting Up the SMT Library Translator

- Changing Part Types in the SMT Library Translator - Library Dialog Box

- Changing Package Names in the SMT Library Translator - Components Dialog Box

SMT Library Layer Mapping Dialog Box

Layer in ADS	Specify the layer in ADS that you want to change.
Class in Allegro	Specify the layer in your design to map to the ADS layer.
Subclass in Allegro	Specify the subclass layer in your design to map to the ADS layer.
OK	Exit the dialog box and save the changes.
Cancel	Exit the dialog box without saving any changes.

Related Topics

- rf_libxlator

- SMT Library Translator – Components Dialog Box

- Setting Up the SMT Library Translator

- Changing Part Types in the SMT Library Translator – Library Dialog Box

- Changing Package Names in the SMT Library Translator – Components Dialog Box

SMT Library Translator - Library Dialog Box

Library List	Lists the libraries extracted from the IFF files you imported. When you choose a library, the *Part Type* field updates letting you edit the part types.
Part Type	Specify a component and the default part type for that component appears in the list. There are six default part types: • Resistor • Capacitor • Inductor • Diode • Triode • SMT IC The tool automatically checks the part validity as soon as you change it. If it is not valid, an error message appears.
Back	Click to return to the SMT Library Translator - Setup Dialog Box where you can change your previous settings.
Next	Displays the SMT Library Translator – Components Dialog Box.
Cancel	Exit the dialog box without saving any changes.

Related Topics

- rf_libxlator

- SMT Library Translator - Setup Dialog Box

- Setting Up the SMT Library Translator

- Changing Part Types in the SMT Library Translator - Library Dialog Box

- Changing Package Names in the SMT Library Translator - Components Dialog Box

SMT Library Translator - Components Dialog Box

Package List	Displays a list of available packages extracted from the IFF files. You can change the package name, update the JEDEC type, and edit the package symbol of the chosen component.
Footprint	
Mapping Mode	Click to choose the package symbol from the local file. If unchecked, the tool generates the package symbol according to the IFF file format. If *Schematic IFF only* is checked in the SMT Library Translator – Setup dialog box, this mode is automatically checked.
JEDEC type	Displays the default JEDEC type of the component. The footprint information comes from the layout IFF file with a prefix of RFSMD. If you change the default JEDEC type, a diamond icon displays beside the component name.
Padstack	Specifies the name of the pad used in the component. If using *Mapping Mode*, this field is not editable, but the padstack will display.
Current component	Displays the name of the selected component.
Back	Click to return to the SMT Library Translator – Library dialog box to change your settings.
Translate	Starts the translation process. A progress meter appears displaying the status of the translation.
Cancel	Exits the dialog box without saving any changes.

Related Topics

- rf_libxlator

- SMT Library Translator - Setup Dialog Box

- SMT Library Layer Mapping Dialog Box

- Changing Part Types in the SMT Library Translator - Library Dialog Box

- Changing Package Names in the SMT Library Translator - Components Dialog Box

Setting Up the SMT Library Translator

To set up the SMT Library Translator:

1. Choose *RF-PCB – IFF Interface – SMT Library Translator*.
   The SMT Library Translator - Setup dialog box appears.

2. Enter filenames or browse to locate the files for *Input Schematic IFF*, *Input Layout IFF*, and enter directory names or browse to the directories for the *Output Library Directory, Output Symbol Directory*, and *Output Padstack Directory*.

3. Enable *Overwrite existing parts,* if required. See the SMT Library Translator dialog box description for details.

4. Enable *Schematic IFF only*, if required. See the SMT Library Translator dialog box description for details.

5. Click *Layer Map* if you also want to change the layer mapping relationship and do the following. Otherwise proceed to the next step.
   The SMT Library Layer Mapping dialog box appears.

   a. Edit the mapping by using the drop-down arrows next to the *Class in Allegro* and *Subclass in Allegro* columns.

   b. Click *OK* to close the dialog box, save the changes, and return to the SMT Library Translator - Setup dialog box, or *Cancel* to close the dialog box without any action.

6. Click *Next* to continue.
   The translator checks for SMT components and consistency between the IFF layout and schematic files. The results of the check appear in the translation log file.

Related Topics

- rf_libxlator

- SMT Library Translator - Setup Dialog Box

- SMT Library Layer Mapping Dialog Box

- SMT Library Translator – Library Dialog Box

- Changing Package Names in the SMT Library Translator – Components Dialog Box

Changing Part Types in the SMT Library Translator - Library Dialog Box

To change part types in the Library dialog box of the SMT Library Translator:

1. Choose a part name from the list.
   The *Part Type* field updates with the default type of the part you chose.

2. Change the part type, if desired.
   If you change the default part type to a non-valid part type, a warning message appears.

3. Repeat the preceding step until you complete the part type changes.

4. Click *Back* to return to the SMT Library Translator – Setup dialog box and change your preferences.
   or
   Next to proceed to the SMT Library Translator – Components dialog box.

Related Topics

- rf_libxlator

- SMT Library Translator - Setup Dialog Box

- SMT Library Layer Mapping Dialog Box

- SMT Library Translator - Library Dialog Box

- SMT Library Translator - Components Dialog Box

Changing Package Names in the SMT Library Translator - Components Dialog Box

To change the package names in the Components dialog box of the SMT Library Translator:

1. From the *Package List* field, choose a package or a package symbol that you want to edit.
   The *Footprint* section of the dialog box updates with the component name and *JEDEC type*.

2. Edit the package name or the name of a group of components.

   ⚠ The default JEDEC type comes from the footprint information in the layout IFF file unless the component includes a DEVICE property for compatibility with previous versions of Allegro X PCB Editor.In this case, the translator uses that information as the default JEDEC type. Once you change the JEDEC type, a diamond appears beside the changed component in the list of packages.

3. Optionally, enable (check) *Mapping mode*, if you want to map the footprint to a package symbol in a local file.

4. Once you are satisfied, click *Translate* to start the translation process.
   Once you start the translation process, a progress bar appears tracking the translation status. When finished, a pop-up appears giving you the option to view the translation report.

Related Topics

- rf_libxlator
- SMT Library Translator - Setup Dialog Box
- SMT Library Layer Mapping Dialog Box
- SMT Library Translator - Library Dialog Box
- SMT Library Translator - Components Dialog Box
- Setting Up the SMT Library Translator

rf_load_module

The `rf_load_module` command lets you load and reuse previously defined RF design modules in your current design. You use the `create module` command to create a module that contains RF components. A module can be created and reused in the same design or in other designs. You can also load several copies at the same time.

> ⓘ To use an RF module, the stackups of the module and the receiving design must match. For further information, see *RF Module Reuse in the Allegro User Guide: Working with RF PCB*.

Related Topics

- Loading an RF Module

Load RF Module: Options Panel

Access Using

- *Menu Path: RF-PCB – Load Module*

Module File	Displays a file browser to select a module (.mdd) file to load.	
Number of tiles	The number of module copies to load.	
Horizontal tile spacing	The horizontal distance between module copies.	
Vertical tile spacing	The vertical distance between module copies.	
Logic Method	Specifies the mode for handling logic for the elements of the module. Choices are:	
	From Module Definition	Use logic from the module definition.
	No logic	No logic.
Rotation Lock	The angle increment used for rotating the module once placed.	
Disband groups	When enabled (checked), the module is loaded devoid of groups and comprised of individual elements only.	
Place at original position	When enabled (checked), places the module at its original location on the board. Note: This option is intended for same-board reuse.	
Restore original net names	When enabled (checked), the nets of the module keep their original names. Otherwise, a module name prefix is added to all net names.	

Loading an RF Module

To load an RF module:

1. Choose *RF-PCB – Load Module*.
   The Load RF Module options appear in the *Options* panel.

2. Click the *Module File* button.
   A File browser appears.

3. Use the File browser to select a module (`.mdd`) file to load.
   An instance of the module appears on your cursor.

4. In the *Number of tiles* entry box, enter the number of module copies you intend to load.

5. If you intend to load multiple copies of the module, enter values for the *Horizontal Spacing* and *Vertical Spacing* between module copies.

6. Click the drop-down arrow for the *Logic Method* option and choose *From Module Definition* (generate components) or *No Logic* (generate symbols).

7. Click the drop-down arrow for the *Rotation Lock* option and choose an angle increment for rotating the module once placed.

8. Enable or disable *Disband groups*, *Place at original position*, and *Restore original net names* as required. See the Load RF Module dialog box description for details.

9. Using your mouse, drag the module instance to its location in the design and click to place it.
   The module instance is released from the cursor and a rotation handle appears.

10. Move your mouse around the module instance to rotate it to the desired orientation, then click again.
    The module orientation is fixed.

11. Click the right mouse button and choose *Done*.
    The module is loaded into the design.

Related Topics

- rf_load_module

rf_manualplace

The `rf_manualplace` command lets you manually place RF components in a design.You can place either:

- Unplaced components: Components that are not yet placed in the design, or
- Revised components: Already placed components with some parametric change and required update

For more information, see *RF Placement* in the *Allegro User Guide: Working with RF PCB*.

Related Topics

- Placing an Unplaced RF Component
- Revising a Placed RF Component

RF Placement: Options Panel

Access Using

- *Menu Path: RF-PCB — Manualplace*

Placement parameters	
Zoom to selected symbols	If enabled, the selected component is zoomed to fit and displayed in the board.
Enable snap/snap to pad edge	When checked, snaps the pin of an RF component to the pad edge of a non-RF component. If this option is disabled or both the components are RF, the pin is snapped to the center of the pad.
Enable auto-shove	Enables existing connected components to move after you place or update the selected component so that they remain connected.
Initialize clearance	When checked, adds a clearance shape to the selected RF component for place or update.
Merge into clearance assembly	When checked, adds the clearance shape of the selected RF component to an existing clearance assembly when an RF component is paced or updated. This option is enabled when Initialize clearance is turned on.
Rotation lock	Specifies the incremental angle for an unplaced component before final placement in the design. The choices are: 0 free rotation without lock. 45 rotation angle locked at an increment of 45 degrees. 90 rotation angle locked at an increment of 90 degrees.
Components to place/update	Displays a list of unplaced or revised components.

Right Mouse Button Menu Options

Skip	Skips the current component and selects next for placement, if multiple components are selected.
Loop Connect Pin	Changes the pin to connect point by shifting forward to the next pin on the RF component. When you reach the maximum pin number of the component, the looping begins again starting with the first pin.
Pick fixed pin	Picks the desired connect pin on the dynamic display of a RF component.
Rotate	Rotate the component before picking the destination location for placement.
Snap pick to	Activates the available snapping modes. For more information on snapping, see the *Allegro User Guide: Getting Started with Physical Design*.

Related Topics

- Revising a Placed RF Component

Placing an Unplaced RF Component

To place an unplaced RF component:

1. Choose *RF-PCB — Setup*.
   Alternatively, In the rfedit_appm application mode, right-click and choose Quick Utilities - RF Setup.
   The RF PCB Settings parameters display in the *Options* panel.

2. Right-click on the board and choose *Done*.

3. From the menu bar, choose *RF-PCB — Manualplace*.
   The Manualplace options display in the *Options* panel.

4. Select a component to place from the *Components to place/update* list.
   An instance of the selected component appears on the cursor.

5. Optionally, select multiple or all the components from the *Components to place/update* list.
   An instance of the first component appears on the cursor.

6. Optionally, right-click and choose *Skip* to skip the existing component and select the next.
   An instance of the second component appears on the cursor.

7. Select the start pin to specify the location of pin 1 for placement.

8. Optionally, select the checkbox *Enable snap/snap to pad edge*.

9. Optionally, right-click and choose *Rotate* option to rotate the component before choosing a destination point.

10. Drag the component instance to its placement location in the design, then click to anchor it.

11. The component is placed and pivots about its anchor point as you move your cursor. Continue to move your cursor to adjust the component orientation as desired, then click again to lock it.
    The component color changes to the color of the active layer and is now placed in the design.

12. Select Initialize clearance option.
    A new clearance assemble is created for the placed component.

13. Optionally select Merge into clearance assembly option.
    The new clearance assembly is merged into the existing clearance assembly of etch objects that are connected to the placed component.

14. Optionally, right-click and choose *Enable auto-shove* option to perform shoving of etch and non-etch objects after the component is placed.

15. Right-click and choose Done to complete the command.

> ⚠ If you choose an another component from the *Components to place/update* list, the placement is cancelled for the selected component.

Related Topics

- rf_manualplace

Revising a Placed RF Component

You have the option to update a component that already exist in the design:

1. Perform steps 1 to 3 in the procedure Placing an Unplaced RF Component.

2. Select a component to place from the *Components to place/update* list.
   An instance of the selected component highlights in the design.

3. Optionally, right-click and choose *Pick fixed pin* to change the start pin for placement.

4. Confirm the update by clicking on the canvas.

5. Select Initialize clearance option.
   The clearance assemble for the updated component is re-initilaize.

6. Optionally select Merge into clearance assembly option.
   The clearance assembly for the updated component is merged into existing clearance assembly that includes the updated component or objects connected to the updated component.

7. Optionally, right-click and choose *Enable auto-shove* option to perform shoving of etch and non-etch objects after the component is placed.

8. Right-click and choose *Done* from the pop-up menu.

⚠ If you choose an another component from the *Components to place/update* list, the placement is cancelled for the selected component.

Related Topics

- rf_manualplace
- RF Placement: Options Panel

rf_measure

The `rf_measure` command lets you measure and display length or distance in your design. You can measure the:

- length of a trace segment

- total trace length

- distance between two points

- centered spacing between two trace segments

Related Topics

- Measuring the Distance between Two Points

rf_modify_net

The `rf_modify_net` command lets you quickly change pin logic connectivity for RF components. This command only works for RF components.

Related Topics

- Modifying Pin Logic Connectivity of RF Components

Modify Connectivity Dialog Box

Access Using

- *Menu Path: RF-PCB – Edit – Modify Connectivity*

Source Component

Name:	Displays the name of the selected source component.
Pin #:	Displays the pin number.
Net:	Displays the net name of the component.

Destination Component

Name:	Displays the name of the selected destination component.
Pin #:	Displays the pin number.
Net:	Displays the net name of the component.

Ignore FIXED property	
Snap and auto shove	Allows the source or destination component and connected objects to automatically snap to the destination or source component. This field works with the *Fix Source* or *Fix Destination* fields.
Snap to pad edge	Snaps the pin of a component to the pad edge of another component, provided one of the components or both the components are not RF. If this option is disabled or both the components are RF, the pin is snapped to the center of the pad. Enabled when *Snap and auto shove* is checked.
Fix source component	Specifies that the destination component and all connected objects snap to the source component. Enabled when *Snap and auto shove* is checked.
Fix destination component	Specifies that the source component and all connected objects snap to the destination component. Enabled when *Snap and auto shove* is checked.

Include clearance assembly	Check (enable) to move the attached clearance assembly during *Snap and auto shove* operation. By default, this option is unchecked.
Rotation lock	Specifies the incremental angle Allegro will rotate the symbol before its placement in the design. Enabled when *Snap and auto shove* is checked.
Swap pin nets	Swaps nets on the pins of RF components. If a pin of non-RF component is selected an error is displayed. You can autoshove along with swapping nets on pins by enabling *Snap and auto shove* and Swap pin nets option. When this option is checked, the *Snap to pad edge, Fix source component,* and *Fix destination component* options will be disabled automatically.

Modifying Pin Logic Connectivity of RF Components

You can modify pin logic connectivity of RF components in multiple ways:

Choose the elements to modify

1. From the menu bar, choose *RF-PCB – Edit – Modify Connectivity.*
   The connectivity options display in the *Options* panel.

2. Select objects by clicking on a single element or holding the left mouse button and drag a bounding box around several elements. You can also use the Temp Group selection mode.

OR

1. In the rfedit_appm application mode, right-click over the RF element.

2. Choose RF Modify connectivity from the right-click menu.
   The connectivity options display in the *Options* panel.

Set the connectivity options in the Options panel

1. Optionally, check *Snap and auto shove* and either *Fix Source* or *Fix Destination* to activate automatic snapping.
   The component moves and snaps to either the source or destination pin.

2. Optionally, check the *Snap and auto shove* and *Snap to pad edge* options.
   If the source is an RF symbol, the dynamic path of the RF symbol is attached to the cursor and the ratsnest is displayed. You can snap to any edge of the pad of the destination pin. If the cursor moves near another pad edge, the dynamic path is updated and you can snap to that pad edge.
   The snapping direction (inward/outward) is determined by the cursor position relative to the destination symbol pin.

3. Optionally, check *Include clearance assembly* to move the clearance assembly along with the component.

4. Click on the source RF component in the design.
   The source component information populates in the *Source component* area in the *Options* panel.
   The nearest pin to the mouse point is the source pin. If you choose the wrong pin, use *Oops* from the right-click pop-up menu to undo your selection.

5. Click on the destination RF component in the design.
   The destination component information populates in the *Destination component* area in the *Options* panel.
   The nearest pin to the mouse point is the destination pin. After the source and destination pins are selected, the modification of logic is performed together with desired snapping and auto shoving.

6. Right-click and choose *Done* from the pop-up menu.

Swapping nets on the pins

1. Check *Swap pin nets* to activate net snapping.

2. Choose source pin.

3. Choose destination pin.

4. Right-click and choose *Done* from the pop-up menu.

> ⚠ The net swapping does not work if either of the pin belongs to non-RF component.

For additional information, see Swapping nets on pins in the *RF PCB User Guide.*

Related Topics

- rf_modify_net

rf_padstack_export

The `rf_padstack_export` command lets you transfer the padstack definition from Allegro to ADS.

This command exports the padstack definition into three files (.ael, .dat and .xml). The .ael file is used to recognize the padstack when imported into ADS.

Related Topics

- Transferring Padstack Definition from Allegro to ADS

Padstack Export to ADS Dialog Box

Access Using

- *Menu Path: RF-PCB — Export Padstacks to ADS*

Available padstack names	Specifies the list of all the available padstack names in the current design that can be exported.
Selected padstack names	Specifies the list of all the selected padstack names that are exported to ADS.
Add	Add padstack name to the list *Selected padstack names*.
Add All	Add all the padstack names to the list *Selected padstack names.*
Remove	Remove padstack name from the *Selected padstack names* field.
Remove All	Removes all the padstack names rom the *Selected padstack names* field.
Padstack filter	Filters out the *Available padstack names*.
Via group name	Specifies the parameter via group name in ADS. By default, the value of this field is the design name.
Output directory	Specifies the path of directory to which the file is exported.
Export	Starts the export process.

Transferring Padstack Definition from Allegro to ADS

Perform these steps to transfer padstack definitions from Allegro to ADS:

1. Choose *RF-PCB — Export Padstacks to ADS.*

2. Choose the padstack names from the *Available padstack names.*

3. Click *Add* to add the padstack names in the *Selected padstack names.*

4. Specify the *Via group name.*

5. Browse to choose the output directory.

6. Click *Export* to start the export.

Related Topics

- rf_padstack_export

rf_push

The `rf_push` command allows you to frequently change the layer specification of a group of supported RF objects in the Z-order.

For additional information, see Editing Groups of Objects in the *RF PCB User Guide.*

Related Topics

- Choosing Elements To Push
- Setting Push Options In The Options Panel

RF Push Command: Options Panel

Access Using

- *Menu Path: RF-PCB – Edit – Push*

Options	
Enable DRC Check	Enables a check for errors after you push the objects. If errors occur, they invalidate the push action.
Ignore FIXED property	Allows objects with the FIXED property to push when checked.
Layers of Selected Objects	
Start/Ref Layer:	Displays the name of the top layer which by default is the starting layer.
End Layer:	Displays the bottom layer of the selected objects.
Actions	
Push Up	Pushes the selected objects up one layer at a time. This option is disabled if the objects cannot move one more layer.
Push Down	Pushes the selected objects down one layer at a time. This option is disabled if the objects cannot move one more layer.
Push to	Pushes the objects to the destination layer that you choose from the pull-down menu.
Include clearance assembly	Enable (check) to push the attached clearance assembly during *Push* operation.

Related Topics

- Setting Push Options In The Options Panel

Choosing Elements To Push

Follow these steps to choose elements to push:

1. From the menu bar, choose *RF-PCB – Edit – Push.*
   The push options display in the *Options* panel.

2. Select objects by clicking on a single element or holding the left mouse button and drag a bounding box around several elements. You can also use the Temp Group selection mode.

OR

1. In the rfedit_appm application mode, right-click over the element or over any one of the group of elements.

2. Choose RF Push from the right-click menu.
   The push options display in the *Options* panel.

Related Topics

- rf_push

Setting Push Options In The Options Panel

Perform the following steps to set push options in the *Options* panel

1. Click *Enable DRC Check* or *Ignore FIXED property* in the Push Operation dialog box, if desired.

2. When you complete your selections, right-click and choose *Complete* from the pop-up menu.
   The *Action* buttons are enabled, and the *Start/Ref Layer* and *End Layer* fields update according to the relative position of the selected structure in the stackup.
   The available destination layer list updates in the pull-down menu.

3. Check *Include clearance assembly* to move the clearance assembly along with the component.

4. Choose *Push Up*, *Push Down*, or choose a layer from the pull-down list to *Push To* to push the elements.
   The elements move to the selected layer and change to the color of that layer.

   > ⚠ During the push operation, you can activate *Oops* or *Next* from the right-click pop-up menu. The *Oops* action will only undo the most recent action. If *Next* is activated, all changes save, and the current push session is finished.

5. You can also activate *Done* or *Cancel* from the right-click popup menu to finish the push command. If *Done* is activated, all unacknowledged changes commit. If *Cancel* is activated, all unacknowledged changes disappear.

When you choose a cline segment to push to a different layer, two vias automatically insert at the end points of the segment. When a packaged part is included in the group, the tool automatically checks which objects can push and applies the pushing operation on those objects.

Related Topics

- rf_push
- RF Push Command: Options Panel

rf_quickplace

The `rf_quickplace` command lets you floorplan your RF design faster in the layout editor. You can quickly place RF symbols outside the board outline, or at a specified location.

You can also place components in hard-reused modules using this command.

Related Topics

- Placing Components in a User-Defined Location
- Placing Components Around Package Keepin

Quickplace: Options Panel

Access Using

- *Menu Path: RF-PCB — Quickplace*

Placement Position	Specifies placement location.
By user Pick	Places components starting from a user-defined location alongside one of the board outlines specified by the edge parameter. Pick a location in the design, and then click Select Origin. The location coordinates appear to the right of the button. You can only select one edge at a time when placing by user pick. ⚠ The command chooses this mode if the board or substrate outline is not defined.
Select Origin	Specifies a placement starting point. Once you pick a location in the design, its coordinates appear on the *Options* panel.
Around package keepin	Places components around one or more edges of the package keepin.Symbols are placed alongside the board outline in the following order: *Top*, *Right*, *Bottom*, *Left*.
Edge	Places components on one or more board edges. The default is Top.
Board side for Non RF Components	Specifies whether non-RF symbols are placed normally or mirrored. The default is Top.
Placement Filter	This section lets you filter and select the RF-related parts to place. Select the unplaced parts by checking next to the icon.
Place all RF-related components	Displays all RF-related components.
Place by refdes	Filters the RF-related components by Refdes. You can filter by *IC*, *IO*, *Discrete,* and *RF.*

Place components in modules	If enabled (checked), includes components in the hard-reused modules for quickplacement. ⚠ The field is disabled if no hard-reused modules are present in the design.
Start	Places the specified components in the specified configuration.

Related Topics

- Placing Components Around Package Keepin

Placing Components in a User-Defined Location

To place components in user defined locations:

1. Choose *RF-PCB — Quickplace*.
   Alternatively, In the rfedit_appm application mode, right-click and choose Quick Utilities - RF Quickplace.
   The Quickplace options appear in the *Options* panel.

2. Choose *By user pick* in the Placement Position area.

3. Click Select Origin.

4. Pick a location in the design. The location coordinates appear on the *Options* panel.

5. Choose a board edge in the *Edge* field. You can select only one at a time, when placing by user pick.

6. Choose a *Board Side for Non-RF Components*.

7. In the Placement Filter area select the components to place.

8. Alternatively, chose *Place components in modules* to include the components contained in modules for quick placement.

9. Click *Start* to add the components. The components are placed on the design.

10. Right-click on the design area and choose *Done*.

Related Topics

- rf_quickplace

Placing Components Around Package Keepin

To place components around package keepin:

1. Choose *RF-PCB — Quickplace*.
   The Quickplace options appear in the *Options* panel.

2. Choose *Around package keepin* in the Placement Position area.

3. Choose a board edges in the *Edge* area. You can select multiple edges at a time, when placing by package keepin.

4. Choose a *Board Side for Non-RF Components*.

5. In the Placement Filter area select the components to place.

6. Alternatively, chose *Place components in modules* to include the components contained in modules for quick placement.

7. Click *Start* to add the components. The components are placed on the design.

8. Right-click on the design area and choose *Done*.

Related Topics

- rf_quickplace
- Quickplace: Options Panel

rf_scaled_copy

The `rf_scaled_copy` command lets you create a scaled copy of a component in your design.

Related Topics

- [Creating a Scaled Copy of an RF Component](#)

RF Scaled Copy Command: Options Panel

Access Using

- *Menu Path: RF-PCB — Edit — Scaled Copy*

Source	Displays the name of the component to copy.
Destination	Specifies a reference designator to assign the copy. By default the tool assigns an available reference designator to use (sort ascend).
Scale factor	Specifies a scale factor to apply to the copy. Note: A scale factor less than 1 reduces the size of the copy.
Snap to connect point	Controls the retrieval of both physical positioning and logic information for a new RF component. The tool calculates the start point and rotation of the new RF component based on any object that it touches. The logic of the pin that connects to that object inherits from the connection.
Snap to pad edge	When checked, snaps the pin of an RF component to the pad edge of a non-RF component. If this option is disabled or both the components are RF, the pin is snapped to the center of the pad. This option is enabled only if *Snap to connect point* is checked.
Offset to connect point	Specifies the distance at which the component must be placed away from the connect point. The default value is Zero, and the component is snapped to the connect point. You can provide negative or positive offset values.
Enable insertion	Enables component insertion. Used to insert the component between two connected RF components on the canvas. This option is only available if Snap to connect point option is selected.
Enable DRC Check	Enables DRC checking. If changing an object results in a design rule violation, and this option is enabled, the action is reversed. If this option is disabled, the object is placed with a DRC error
Clearance	
Update clearance shapes to default	Creates a new clearance shape after the scaled copy operation.
Copy clearance shapes	Copies the current clearance shape along with the scaled copy of the RF component.

Pop-up Menu Options

Loop Pin Forward	Changes the pin to connect point by shifting forward to the next pin on the RF component. The net of the connect pin updates as the pin changes. The net of the connect pin does not change if there are no objects connected at the connect point. When you reach the maximum pin number of the RF component, the looping begins again starting with the first pin.
Loop Pin Backward	Changes the pin to connect point by shifting backward to the next pin on the RF component. The net of the connect pin updates as the pin changes. The net of the connect pin does not change if there are no objects connected at the connect point. When you reach the maximum pin number of the RF component, the looping begins again starting with the first pin.
Pick Connect Pin	Picks the desired connect pin on the dynamic display of a multi-pin RF component.
Flip Symbol	Flips the symbol geometry of an RF component. Provides flexibility in controlling the physical positioning of the component. You cannot flip a component before you establish the pin to connect point.
Show/Hide GUI Form	Choose to toggle the display settings for the edit dialog box specific to the component.

Creating a Scaled Copy of an RF Component

You can create a scaled copy of an RF component in multiple ways:

Choose the element to create scaled copy

1. From the menu bar, choose *RF-PCB – Edit – Scaled Copy.*
   The scaled copy options display in the *Options* panel.

2. Click on a component in the design to copy.
   The name of the component appears in the *Source* field and the scaled copy appears on your cursor.

OR

1. In the rfedit_appm application mode, right-click over the RF element.

2. Choose RF Scaled Copy from the right-click menu.
   The scaled copy options display in the *Options* panel.
   The name of the component appears in the *Source* field and the scaled copy appears on your cursor.

Create a scaled copy of the RF component

1. In the *Destination* field, specify a reference designator.

2. In the *Scale factor* field enter a scale factor to use for the copy.

3. Enable *Snap to connect point* to snap the copy to the nearest connect point.

4. Optionally, check the *Snap to connect point* and *Snap to pad edge* options.
   If the source is an RF symbol, the dynamic path of the RF symbol is attached to the cursor and the ratsnest is displayed. You can snap to the middle of the pad edge of the destination pin. If the cursor moves near another pad edge, the dynamic path is updated and you can snap to that pad edge.
   The snapping direction (inward/outward) is determined by the cursor position relative to the destination symbol pin.

5. Specify an *Offset to connect point*.

6. Move your mouse to locate the copy in your design, then click to anchor it.

7. Move your mouse to rotate the component and click to place it.

8. Right-click and choose *Show/Hide GUI Form* to edit parameters for the selected object.

Right-click and choose *Done* or *Next* to complete the operation.

Insert a a scaled copy of the RF component between two connected components

1. In the *Destination* field, specify a reference designator.

2. In the *Scale factor* field enter a scale factor to use for the copy.

3. Enable *Snap to connect point* to snap the copy to the nearest connect point.

> ⚠ To insert an RF component, you need check *Snap to connect point*. You may specify an *Offset to connect point* value or leave the default value, 0.00.

4. Optionally, check the *Snap to connect point* and *Snap to pad edge* options.
   If the source is an RF symbol, the dynamic path of the RF symbol is attached to the cursor and the ratsnest is displayed. You can snap to the middle of the pad edge of the destination pin. If the cursor moves near another pad edge, the dynamic path is updated and you can snap to that pad edge.
   The snapping direction (inward/outward) is determined by the cursor position relative to the destination symbol pin.

5. Specify an *Offset to connect point*.

6. Drag the component instance to the right or left of the connecting point of the two currently connected components.

7. Right-click and choose Snap pick to - Pin.
   Notice the dynamic path for the inserted component. To change the connect pin, right-click and choose Loop Pin Forward or Loop Pin Backward or Pick Connect Pin.

Right-click and choose *Done* or *Next* to complete the operation.

Related Topics

- rf_scaled_copy

rf_setup

The `rf_setup` command lets you perform global RF parameter initialization for your design. You may need to run the command if you:

- change your design units.

- run into initialization problems during RF design layout.

- try to use RFPCB functionality on the current design for the first time.

The `rf_setup` command initializes parameters that control:

- the structure of transmission lines.

- physical dimensions for generating RF components or routing RF traces.

- other miscellaneous default settings.

Related Topics

- Initializing Your Design For RF And Mixed Signal Design

RF PCB Settings: Options Panel

Access Using

- *Menu Path: RF-PCB — Setup*

Parameter Set

Select a parameter set to display and set the parameters for the following parameter sets

Default layers & groundings
Default physical dimensions
Miscellaneous
Customize

Default layers & groundings parameters set

Microstrip

Conductor	Specifies the default layer for a microstrip conductor.
Ground	Specifies the reference layer for a microstrip structure.

Stripline

Ground Above	Specifies the reference layer above the conductor layer.
Conductor	Specifies the default layer for a stripline conductor.
Ground Below	Specifies the reference layer below the conductor layer.

Broadside / offset coupled striplines

Ground Above	Specifies the upper reference layer for a stripline conductor.
Conductor	Specifies the active conductor layer for the structure.
Secondary	Specifies the coupled conductor layer for the structure.
Ground Below	Specifies the lowest reference layer for a stripline conductor.

Co-planar Waveguide

Conductor	Specifies the active layer for CPW.
Lower Ground	Specifies the reference layer for CPW.

Default Physical Dimensions parameter set

Conductor dimensions

Conductor width	Specifies the default width for routing traces.
Curve radius	Specifies the default radius for curved bends when routing.
Miter fraction	Specifies the default mitered fraction for mitered bends when routing.

Default line lock

Line lock	Specifies the step increment of rotation for a trace segment during routing. Choices are:	
	45	Increments of forty-five degrees.
	90	Increments of ninety degrees.
	Off	No increment (free angle of rotation).

Bend modes

Microstrip	Specifies the default bend for microstrip routing.
Stripline	Specifies the default bend for stripline routing.

Miscellaneous parameter set

Working frequency	Specifies the default working frequency used to calculate approximate electrical length values.	
RF Component display	Specifies settings for RF component display	
	All RF Component Text Off	Disables text display for RF Components in the trace report.
	RF Trace Components Text Off	Disables text display for RF Trace Components in the trace report.
	All RF Component Text On	Enables text display for RF Components in the trace report.
Display RF traces	Displays a report of RF traces.	
RF routing mode	Specifies the default mode for routing RF traces. Choices are:	
	Single Segment Mode	Routes traces with alternating straight and bend segments.
	Multi-Segment Mode	Routes traces using several straight segments and a bend, multiple times, with a heads-up display.
RF Component Diagram	*Show RF component diagram*	When enabled (checked), specifies the automatic display of the component diagram in all component dialog boxes when they appear.
Project file	Specifies the path of the project file (*.cpm) that contains the logical design for the current board file.	
	⚠ This field is non-editable if you've opened the board file using the Project Manager.	
	⚠ This field is available if you've opened the design in PCB Editor.	

Variable definition file directory	Specifies the path of the variable definition file (*.dat) that contains the logical design for the current APD design. ⚠ This field is available if you've opened the design in APD.

Current RF Library	Specifies the current RF library. Options are: *CDN Unified, ADS Compatible, and MWO Compatible.*
	
	• If the layout design contains RF components that are created from export physical process, the logical path indicates the associated RF schematic library. The correct library is set and the option is fixed.
	
	• If the layout design contains RF components that are created from layout side, following checks determine the correct library:
	
	  ○ If the layout design contains no MWO components, the library is set to *CDN Unified.* The library selection field is enabled to change it back to ADS. Changing library to *MWO Compatible* causes an error and the field is restored to the previously set library.
	
	  ○ If the layout design contains no ADS components, and
	
	    ■ the layout design contains MWO components that are compatible with ADS, the library is set to *MWO Compatible* and the option is disabled.
	
	    ■ the layout design contains only MWO components that are not compatible with ADS, the library is set to *CDN Unified.* The library selection field is enabled to change it back to MWO. Changing library to *ADS Compatible* causes an error and the field is restored to the previously set library.
	
	  ○ If the layout design contains both ADS and MWO components, and
	
	  ○ the MWO components are incompatible to ADS, the library is set to *CDN Unified* and the option is disabled.
	
	  ○ some of the MWO components are compatible with ADS, the design is considered as corrupted.

Customize Parameter set

Float Forms	Select the checkbox to enable the form for floating.

Initializing Your Design For RF And Mixed Signal Design

Perform these steps to initialize your design for RF and mixed signal design:

1. From the menu bar, choose *RF-PCB – Setup*.
   Alternatively, In the rfedit_appm application mode, right-click and choose Quick Utilities - RF Setup.
   The RF PCB Settings display in the *Options* panel.

2. Choose the *Default layers & groundings* parameter set and specify default RF layer settings.

3. Choose the *Default physical dimensions* parameter set and specify default values for trace dimensions and bend types.

4. Choose the *Miscellaneous* parameter set and specify default values for working frequency, route mode, and other RF options.

5. Click *Apply* button or right-click on the drawing area and choose *Apply* to save the settings.

6. Right-click on the drawing area and choose *Done* or *Cancel* to complete the command.

Related Topics

- rf_setup

rf_shape2component

The `rf_shape2component` command lets you convert multiple static shapes in your design to customized RF components. Once you select a shape and specify pin locations, you can convert it to a user-defined component and use it in your design. Optionally, you can save it to your library for future reuse.

Notes:

- User-defined components are limited to eight pins.

- Pins cannot be located on arc edges.

- The shape may contain voids.

- User-defined components may contain multiple etch shapes which may or may not have pins on them.

Related Topics

- Converting A Static Shape To An RF Component

Shape to Component: Options Panel

Access Using

- *Menu Path: RF-PCB – Convert – Shape to Component*

Pins area

Number of pins	Specifies the total number of pins (up to eight) that you want to place on the components.
Locate Pin	Click this button and then locate the pin by clicking on the desired line edge of an etch shape. Note: Pins cannot be located on arc edges.
Choose pin ID	Specifies which pin you are locating.
Pin on	Select the layer on which to place the pin.
Pins specified	Highlights the number of the pin that you are placing. The remaining pins also display but are dimmed.

Nets area

Pin#	Specifies the net assignment for the pins. Click the browse button to change it.

Save converted package

Enable to save the converted package.

Convert

Click the convert button to convert the shape to component.

Pop-up Menu Options

Convert	Performs the desired convert operation on the selected RF objects.

Converting A Static Shape To An RF Component

You can convert a static shape to an RF component in multiple ways:

Choose the components to convert

1. From the menu bar, choose *RF-PCB – Convert – Shape to component.*
   The conversion options display in the *Options* panel.

2. Select objects by clicking on a single element or holding the left mouse button and drag a bounding box around several elements. You can also use the Temp Group selection mode.

OR

1. In the rfedit_appm application mode, right-click over the element, or over any one of the group of elements.

2. Choose RF Shape to component from the right-click menu.

The following prompts appear in the console window.

```
Select etch shapes to convert . . .
```

Enter a point or a box:

Set the conversion options in the Options panel

1. In the *Number of pins* field, click the drop-down arrow and select a number representing the total number of pins for the component.

2. Chose the pin number to locate and then click the *Locate Pin* button.
   The following prompt appears in the Console window.
   ```
   Click at desired pin location:
   ```

3. In the *Pin on* field, click the drop-down arrow to select the layer on which to place the pin.

4. Click a location for the pin on the shape.
   The pin number is now bold in the *Pins specified* field.
   Only the selected shapes on the current active layer are used in the pin location specification. If you specify a location but there are no selected shapes on the current active layer, or if a location is not near enough to some of the selected shapes on the current active layer, an error message appears, warning you that an invalid pin location exists. If a location is in the overlapped area of several selected shapes on the current active layer, the shape that is nearest the location is used. Once a pin location is correctly specified, a square cross mark appears at the pin location.

5. Repeat steps 4 and 5 until all pins are located.

6. Click *Convert* to convert the shape with internally assigned nets to all pins.
   - or -
   In the *Nets* area, click the button next to one or more pins to change their net assignment, then click *Convert* to begin the shape conversion.
   If the conversion is successful, a confirmation dialog box appears that gives you the option to write the symbol (.dra and .psm files) to a storage location for future reuse. Otherwise, an error dialog box appears with a message and gives you an opportunity to return to the procedure to fix the problem.

Related Topics

- rf_shape2component

rf_single_segment_connect

The `rf_single_segment_connect` command lets you connect two pins with a single line segment (MLIN or SLIN).

Related Topics

- Connecting Two Pins with a Single Line Segment

RF Single Connect: Options Panel

Access Using

- *Menu Path: RF-PCB — Single Segment Connect*

Act	Specifies the active routing layer.
Alt	Specifies the alternate routing layer.
Ground above	Specifies the reference plane above the signal trace (for simulation purposes).
Ground below	Specifies the reference plane below the signal trace (for simulation purposes).
Line Width	*Specifies the width of the trace. Units are determined by the drawing units.*
Snap to connect point	When checked, snaps to a destination pin.
Initialize clearance	When checked, initializes clearance for a route.
Add into existing assembly	When checked, adds the clearance from an existing clearance assembly. This option is enabled only if Initialize clearance is checked.

Pop up menu options

Snap pick to	Activates the available snap pick to component mode when the Clearance Settings are selected.
Clearance Settings	Opens the Clearance Settings dialog box to edit the clearance settings.

Connecting Two Pins with a Single Line Segment

Follow these steps to connect two pins with a single line segment:

1. From the menu bar, choose *RF-PCB — Setup*.
   Alternatively, In the rfedit_appm application mode, right-click and choose *Quick Utilities - RF Setup*.
   The RF PCB Settings parameters display in the *Options* panel.

2. Select layer, ground plane, and other settings.

3. Enter a value for *Line Width*.

4. Click on a location in the design to choose a start point or pad edge, where you want to start routing the trace.

5. Click on a location in the design to choose an end point or pad edge where you want to end routing the trace.

6. Optionally, enter the new name to remove ratsnest.

7. Right-click and choose *Next* from the pop-up menu.

8. Route other RF traces on the board.

9. When completed, click *OK,* or right-click and choose *Done* from the pop-up menu to complete the command.

Related Topics

- rf_single_segment_connect

rf_snap

The `rf_snap` command lets you move and physically connect a component by specifying pin logic. Once you select a source pin on the component to move the component snaps into proper position.

> ⚠ When snap connecting two components, the rotation angle of the moving component adjusts automatically.

Related Topics

- SnapConnecting A Component In Your Design
- SnapConnecting to a Component When Snap to Pad Edge Option is Enabled

RF Pin Snap Command: Options Panel

Access Using

- *Menu Path: RF-PCB — Edit — Snap*

Source Component	Displays the names of the Pin and Net of the source component.
Destination Component	Displays the names of the Pin and Net of the destination component.
Additional Rotation	Check this to add an angle to the rotation angle of the component to be snapped in the transformation of the symbol.
Direction:	
○ *Fix source component*	Choose to keep the source pin fixed and the destination pin and connected objects are snapped to the source pin.
○ *Fix destination component*	Choose to keep the destination pin fixed and the source pin and connected objects are snapped to the destination pin.
Snap to pad edge	Enable this option to snap the pin of a component to the pad edge of another component, provided one of the components or both the components are not RF. If this option is disabled or both the components are RF, the pin is snapped to the center of the pad.
AutoShove	Controls whether the connected components transform as well as the selected one. If this field is checked, the snap operation is effective on the group of connected components containing the selected source.
Zoom to selected pin	Enable (check) to zoom in to the selected pin for a larger view.
Ignore FIXED property	Enable (check) to ignore the FIXED property attached to any object and snap it irrespective of the setting.
Include Clearance Assembly	Enable (check), to move the clearance assemblies attached to the objects and move them along with the object during snapping. By default, this is unchecked.
Rotation lock	Specifies the incremental angle Allegro will rotate the symbol before its placement in the design.This option is not available if *Snap to pad edge* is enabled.

Pop up menu options

Snap pick to	Activates the available snapping modes.
Clearance Settings	Opens the Clearance Settings dialog box to edit the clearance shape settings.

Related Topics

- SnapConnecting to a Component When Snap to Pad Edge Option is Enabled

SnapConnecting A Component In Your Design

Follow these steps to snap connect a component in your design:

1. From the menu bar, choose *RF – PCB – Edit – Snap*.
   The *Options* panel shows the options for the snap mode.

2. You can click to select objects. To select multiple objects, hold the left mouse button and drag a bounding box around the objects. You can also use the *Temp Group* selection mode.

OR

1. In the rfedit_appm application mode, select any RF element.

2. Choose *RF Snap* from the right-click menu.
   The *Options* panel shows the options for the snap mode.

3. Click the source pin.
   The name of the pin appears in the *Source component* area of the *Options* panel.
   If the connectivity is unique, the *Destination component* area shows the target pin.
   If the connectivity is not unique, you can select a target from the drop-down list in the *Destination component* area. You can also click a pin in the design to select a target pin.

   > ⚠ If the *Snap to pad edge* option is enabled and if the source is an RF symbol, the dynamic path of the RF symbol is attached to the cursor and the ratsnest is displayed.

4. Click in the design canvas to confirm the operation.
   The source symbol is positioned with its center snapped to the connect point of the destination pin. The rotation angle of the source symbol is determined by the position of the cursor and the connect point of the destination pin and by the rotation lock.
   All of the group of connected components containing the selected source pin snap together. The angle is added to the snapped pin during transformation.
   If the *Snap to pad edge* option is enabled and if the source is an RF symbol, you can snap to any edge of the pad of the destination pin. If the cursor moves near another pad edge, the dynamic path is updated and you can snap to that pad edge.
   The snapping direction (inward/outward) is determined by the cursor position relative to the destination symbol pin.

5. Repeat steps 3 and 4 to snap connect other components.
   - or-
   Right-click and choose *Done* to complete the command.

Related Topics

- rf_snap

SnapConnecting to a Component When Snap to Pad Edge Option is Enabled

Follow these steps to snap connect to a component when snap to pad edge option is enabled:

1. From the menu bar, choose *RF – PCB – Edit – Snap*.
   The *Options* panel shows the options for the snap mode.

2. You can click to select objects. To select multiple objects, hold the left mouse button and drag a bounding box around the objects. You can also use the *Temp Group* selection mode.

OR

1. In the rfedit_appm application mode, select any RF element.

2. Choose *RF Snap* from the right-click menu.
   The *Options* panel shows the options for the snap mode.

3. Click the source pin.

   a. If the source pin is on non-RF component, the nearest edge of the source pin is selected automatically when you pick the source pin.

   b. If the destination pin is on non-RF component, the nearest edge of the destination pin is selected automatically when you pick the destination pin.

   c. If either the source or the destination pin is non-RF, then you need to decide the snapping angle between the two pins. Move the mouse to control the dynamic cursor of the object to the proper position and click the canvas to confirm the snapping.

   The name of the pin appears in the *Source component* area of the *Options* panel.
   If the connectivity is unique, the *Destination component* area shows the target pin.
   If the connectivity is not unique, you can select a target from the drop-down list in the *Destination component* area. You can also click a pin in the design to select a target pin.

   ⚠ If the *Snap to pad edge* option is enabled and if the source is an RF symbol, the dynamic path of the RF symbol is attached to the cursor and the ratsnest is displayed.

4. Click in the design canvas to confirm the operation.
   The source symbol is positioned with its center snapped to the connect point of the destination pin. The rotation angle of the source symbol is determined by the position of the cursor and the connect point of the destination pin and by the rotation lock.
   All of the group of connected components containing the selected source pin snap together. The angle is added to the snapped pin during transformation.
   If the *Snap to pad edge* option is enabled and if the source is an RF symbol, you can snap to any edge of the pad of the destination pin. If the cursor moves near another pad edge, the dynamic path is updated and you can snap to that pad edge.

The snapping direction (inward/outward) is determined by the cursor position relative to the destination symbol pin.

5. Repeat steps 3 and 4 to snap connect other components.

- or-

Right-click and choose *Done* to complete the command.

The following table defines the conditions when *Snap to pad edge* is available. The snapping between two components depends on their type.

Source	Destination	Fix source	Snapping to pad edge is available
RF	RF	False	No (RF snapped to RF)
RF	RF	True	No (RF snapped to RF)
RF	non-RF	False	Yes (RF snapped to non-RF)
RF	non-RF	True	Yes (non-RF snapped to RF)
non-RF	RF	False	Yes (non-RF snapped to RF)
non-RF	RF	True	Yes (RF snapped to non-RF)
non-RF	non-RF	False	Yes (non-RF snapped to non-RF)
non-RF	non-RF	True	Yes (non-RF snapped to non-RF)

Related Topics

- rf_snap
- RF Pin Snap Command: Options Panel

rf_tapered_connect

The `rf_tapered_connect` command lets you change trace connections to non-RF components (IC, connector, discretes) to tapered connections. The taper begins at the edge of the component pad.

> ⚠ You cannot taper connections to lumped components with RF properties using this command. If you want to implement a tapered connection from a pad, you can insert a width taper to the pin or pad of the component.

Related Topics

- Changing Trace Connections To Tapered Connections

Tapered Pin Connect Command: Options Panel

Access Using

- *Menu Path: RF-PCB – Convert – Tapered Pin Connect*

Pin Selection Mode	
Single Pin	Specifies that only the selected pin is to have its connection tapered.
Single Component	Specifies that all the pins of the selected component are to have their connections tapered.
Tapered Length	Specifies the taper length from the pin of the non-RF component to the trace.

Changing Trace Connections To Tapered Connections

To change trace connections to tapered connections:

1. Choose *RF-PCB – Convert – Tapered Pin Connect*.
   The Tapered Pin options display in the *Options* panel.

2. In the *Pin Selection Mode* area, choose *Single Pin* to have just the connection of the selected pin tapered, or choose *Single Component* to have all the connections of the selected component tapered.

3. In the *Tapered Length* entry box, enter a value for the length of the taper.

4. Click on the pin or component in the design.
   The pin or component connections change to tapered connections.

5. Repeat steps 2, 3, and 4 to taper other connections.
   - or -
   Right-click and choose *Done* to complete the operation.

OR

1. In the rfedit_appm application mode, right-click over the element, or over any one of the group of elements.

2. Choose *RF Tapered Pin* connect from the right-click menu.
   The Tapered Pin options display in the *Options* panel.

3. In the *Pin Selection Mode* area, choose *Single Pin* to have just the connection of the selected pin tapered, or choose *Single Component* to have all the connections of the selected component tapered.

4. In the *Tapered Length* entry box, enter a value for the length of the taper.

5. Right-click and choose *Done* to complete the operation.

Related Topics

- rf_tapered_connect

rf_varedit

The `rf_varedit` command lets you edit variables and expressions imported with schematic IFF files. The tool creates the variable definition file (`vardef.dat`) during the import process if the schematic IFF file contains any VAR components and stores it in the project directory. You can use the Variable Editing dialog box to edit the values or the Equation Generator (accessed from the Variable Editing dialog box) to create complex expressions for the variables.

Related Topics

- Equation Generator Dialog Box
- Editing Variables Imported From An IFF Schematic File

Variable Editing Dialog Box

Access Using

- *Menu Path: RF-PCB – Edit – VAR Edit*

Variable Definition File	Displays the read-only variable definition file (`vardef.dat`) created during the IFF import process and stored in the project directory of the current design.
Variable List	Displays all variables and expressions in the variable definition file.
Variable	Displays the name of the variable once you choose a variable from the list. You cannot edit the name of a variable.
RefCount	Displays the number of component instances that uses the variable.
Value	Displays the value for the current variable.
OK	Closes the dialog box and saves the changes.
Cancel	Closes the dialog box without saving any changes.

Related Topics

- Editing Variables Imported From An IFF Schematic File

Equation Generator Dialog Box

Variable	Displays the variable you chose in Variable Editing dialog box.
Functions	Displays all supported pre-defined names to use in the expression.
Operators	Displays all supported pre-defined names to use in the expression.
Constants	Displays all supported pre-defined names to use in the expression.
OK	Closes the dialog box, returns you to the Variable Editing dialog box and saves the changes to the variable definition file.
Cancel	Closes the dialog box without saving any changes.

Related Topics

- rf_varedit

Editing Variables Imported From An IFF Schematic File

Follow these steps to edit variables imported from an IFF schematic file:

1. Run `rf_varedit`.

   The Variable Editing dialog box appears if a variable definition file exists. If no variable definition file exists, a message appears indicating that there are no VAR components in the schematic file.

2. Click on the variable you want to edit.

   The name of the variable appears in the read-only *Variable* field, and its value appears in the *Value* editable text field.

3. Enter a new expression in the *Value* field or click the button next to the Value field to use the Equation Generator to generate complex expressions.

   The Equation Generator Dialog Box appears and provides pre-defined names of supported functions, operators, and constants for you to use.

4. When you complete editing variables, click *OK*.

   If you made changes, a dialog box appears informing you that you need to repackage the components in order to refresh the variable expressions.

Related Topics

- rf_varedit
- Variable Editing Dialog Box

rfedit

The `rfedit` command lets you edit PCells.

For additional information, see *Working with RF PCells* in the *Allegro User Guide: Placing the Elements.*

Related Topics

- Invoking the RF Module

Edit RF Properties Dialog Box

Access Using

- *Menu Path: RF Module – Edit RF Components*

Pcell Type	Indicates whether a shape or a Pcell component is being placed.
Pcell Name	The names of the Pcell.
Net Name	The name of the net in which the Pcell is being placed.
Pcell Components	Displays the reference designator of the selected Pcell.
Property Name	Name of the property on the Pcell.
Property Value	Value of the property on the Pcell.
Property Type	Type of property on the Pcell, such as simulation, physical and so on.
Annotate	Determines whether the property should get annotated to the layout or not.
Property Description	Description of the property.
Analyze	Generates the electrical values for the rf component on the basis of the given physical properties.
Synthesize	Generates the physical values for the rf component on the basis of the given electrical properties.
Default	Restores the Pcell property values to original values.
Apply	Applies the changes.
OK	Applies the changes and closes the dialog box.
Cancel	Closes the dialog box without applying the changes.
Help	Launches help.

Invoking the RF Module

To use the RF module:

1. Choose *RF Module – Edit RF Components*.

2. Select the RF component in the design, such as a capacitor.
   The Edit RF Properties dialog box appears.

3. Specify the changes as required, such as finger width, length of overlap and so on by entering the required values in the appropriate *Property Value* column next to the Property Name

4. Click *Analyze* to regenerate the electrical values for the RF component.

5. Ensure that the *Annotate* option is selected to ensure that the changed values get annotated to the layout.

6. Click *OK* to close the Edit RF Properties dialog box.

Related Topics

- rfedit

rfedit_appm

RF Edit application mode customizes your environment to provide context sensitive RF commands. This implies that if you are in this application mode and your right-click on an RF element, the RF commands specific to that element will display in the right-click menu. For example, if you right-click on an RF component, in this application mode, the right-click menu is populated with RF command, like rf_change, rf_delete, rf_flip, specific to this type of object.

> ⚠ This application mode is available for the following products on selecting the *Analog/RF* option.

- ○ Allegro X Advanced Package Designer

- ○ Allegro Venture PCB Designer Suite

- ○ Allegro PCB Designer

An application mode provides an intuitive environment in which commands used frequently in a particular task domain, such as rf_change, rf_flip, rf_push, are readily accessible from right-mouse- button popup menus, based on a selection set of design elements you have chosen.

This customized environment maximizes productivity when you use multiple commands on the same design elements or those in close proximity in the design. The application mode configures your tool for a specific task by populating the right-mouse-button popup menu only with commands that operate on the current selection set.

In conjunction with an active application mode, your tool defaults to a pre-selection use model, which lets you choose a design element (noun), and then a command (verb) from the right-mouse-button popup menu. This pre-selection use model lets you easily access commands based on the design elements you have chosen in the design canvas, which the tool highlights and uses as a selection set, thereby eliminating extraneous mouse clicks and allowing you to remain focused on the design canvas.

Use *Setup – Application Mode – None* (noappmode command) to exit from the current application mode and return to a menu-driven editing mode, or verb-noun use model, in which you choose a command, then the design element.

For more information on the RF Edit application mode, see the *Getting Started with Physical Design* user guide in your documentation set.

Access Using

- *Menu Path: Setup – Application Mode– RF Edit*

- Toolbar Icon:

Accessing Command Help for Right Mouse Button Options within an Application Mode

To access command help for the right mouse button options within an application mode:

1. Type `helpcmd` in the console window.
   The Command Browser dialog box appears.

2. Enable the *Help* radio button at the top of the dialog box to place the browser in Help mode.

3. Scroll the command list and select (double-click) the command you want help on.

The command documentation displays in the Cadence Help documentation browser momentarily.

rfplace

The `rfplace` command allows you to place RF shapes.

Related Topics

- Placing an RF Component

Placing an RF Component

To place an RF component:

1. Choose Edit RF Components – Place RF Shape.

2. Select the location in the board where you want to place the shape.
   The Edit RF Properties dialog box appears.

3. Select the Pcell name that is to be placed from the Pcell Name pull-down list box.

4. Select the net name from the Net Name list box.

5. Specify the changes as required, such as finger width, length of overlap and so on by entering the required values in the appropriate *Property Value* column next to the Property Name

6. Click *Analyze* to regenerate the electrical values for the RF component.

7. Ensure that the *Annotate* option is selected to ensure that the changed values get annotated to the layout.

8. Click *OK* to close the Edit RF Properties dialog box.

Related Topics

- rfplace

rfreplace_ripup

The `rfreplace_ripup` command enables you to replace Pcells that got ripped off due to netrev process at exactly the same places where they were placed originally.

Access Using

- *Menu Path:* RF Module – Replace Pcells

Replacing Ripped Up PCells

1. Choose RF Module – Replace Pcells.

rfsip route

The `rfsip route` command lets you create an RF route.

RFSip Route: Options Panel

Access Using

- *Menu Path: RF Module – RF Route – Create Route*

Default Shape	Use this drop-down list to specify the RF shape to be used for creating the RF route. The default shape used is MLIN, however, you can select any shape from the drop-down list.
Default Bend	Specifies the RF shape to be used when the direction or the layer of the RF route changes. The available shapes are: • MBEND2 — Use this shape to add a bend and change the direction of a route on the top or the bottom layer. • MCURVE — Use this shape to add a 90 degree circular bend to the route create on the top or the bottom layer. • SBEND — This shape is used when the direction of a route, created on intermediate metal layers, is changed. • SCURVE — Use this shape to add circular bends, when changing the direction of a route, created on intermediate metal layers.
APDLAYER_A	The value of this property indicates the layer on which the route is being created.
APDLAYER_B	The value of this property indicates the ground layer for the metal layer specified by the APDLAYER_A property.
APDLAYER_D	This property is specified only for striplines. It indicates the second ground layer for the metal layer specified by the APDLAYER_A property.
Auto Snap Start Point	Select this option to ensure that the RF route to be created is automatically snapped to a component pin, a via or to an RF shape connection point.
Line Width	Indicates the width of the RF route. For the same shape, the width of the route can be increased while creating the route itself. The width of the route is specified in microns.
Bend Proximity	Specifies the minimum distance between two consecutive bends. By default, the value is specified in microns.

Route Length	This is a non-editable field, that displays the total length of the route being created. For example, if you start the route in one layer and then take it to another layer using a via, then the Route length displayed in this field is the sum of the route length in both the layers. ⚠ Via length is not included in the route length.
Route Net	This drop-down list lists all the nets in the APD design. To create RF route on any one net, select the net from the drop-down list and then start creating the route. If you start creating an RF shape route from an existing pin or connection point, the associated net name is automatically assigned to the new RF shape route and this field is grayed out. ⚠ The ratsnest is replaced with the RF route only if the connectivity of the route is complete.

ripup etch

Deletes physical entities associated with selected nets. You can also select rat bundles within IFP application mode (GXL product only). This command functions within a pre-selection use model. You choose design objects first, then right-click to choose the command. Objects ineligible for use with this command generate a warning and are ignored.

The following table lists entities that are ignored by the command depending on whether a selected object is a net or a bundle.

Selected Object	Entities Not Deleted
Net	Fixed entities, pin escapes, plan lines, and plan vias.
Bundle	Fixed entities, pin escapes, shapes, plan lines, plan vias, and etch that is also part of a completed connection of another rat (unless it is associated with another selected bundle or net).

⚠ Etch and connected vias added as a part of a symbol remain intact. To delete them, enable *Symbol Etch* on the *Options* panel and use the delete command.

Access Using

- *Right Mouse Button option: Ripup Etch*

Related Topics

- Ripping Up Etch Associated with Rat Bundles

Ripping Up Etch Associated with Nets

To rip up the etch associated with nets:

1. Hover your cursor over a net or drag your cursor over a group of nets.
   This action highlights the selected objects.

2. Right-click and choose *Ripup Etch* from the pop-up menu.
   The etch associated with the selected nets is removed.

Ripping Up Etch Associated with Rat Bundles

To rip up the etch associated with rat bundles:

1. In IFP application mode, hover your cursor over a bundle or drag your cursor over a group of bundles. The selected objects highlight.

2. Right-click and choose *Ripup Etch* from the pop-up menu.
   The etch associated with the rat members of selected bundles is removed.

   > ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

Related Topics

- ripup etch

roam

The `roam` command lets you move the design across the working area of your user interface. An increment value in screen units is required for x and y modes; x indicates roam is horizontal, and y indicates roam is vertical. The `roam` command is available for possible scripting but is not required for many working scripts because interactive commands ignore the view window. You may want to remove `roam` commands to improve performance.

Syntax

```
roam <x increment-value> <y increment-value>
```

Moving Your Design

To move your design:

1. Type roam followed by *x* and *y* coordinates.

2. The design view shifts accordingly.

Right-button Option

The `roam` command lets you move through the Design window and in the *WorldView* window as though you were using the right mouse button. To view the parts of a design that do not fit on the display, you can click the right mouse button to roam across the design. Hold down the right button and slide the mouse in the direction in which you want the window to move. The design display slides inside the window as if attached to the button. When you release the button, the design stays in its new position.

In the Design window, the window moves in the direction in which you slide the mouse until you release the right mouse button (the design itself appears to move in the opposite direction). In the *WorldView* window, the current window outline moves in the direction in which you slide the mouse until you release the right mouse button. The design display in the Design window moves constantly to the new window location as you move the mouse in the *WorldView* window. The window moves with the mouse until you release the mouse button.

In the *WorldView* window, click the right mouse button to change the window center to that point.

Example

In the horizontal direction, *roam x 400* is equivalent to sliding the mouse rightward, and the design appears to move to the left

roam x -400 is equivalent to sliding the mouse leftward, and the design appears to move to the right.

In the vertical direction, *roam y 256* is equivalent to sliding the mouse down, and the design appears to move up

roam y -256 is equivalent to sliding the mouse up.

room outline

The `room outline` command lets you create rooms, name rooms, specify the board layer on which to situate rooms, and control when DRC errors display under various placement conditions. For more information about using rooms during placement, see *Creating a Floorplan Using Rooms* in the user guide of your product documentation.

Related Topics

- Creating a Room

- Deleting a Room

- Editing a Room

- Moving a Room

Room Outline Dialog Box

Access Using

- *Menu Path: Setup – Outlines – Room Outline*

Command Operations

Functions on the Room Outline dialog box change depending on the task you choose in Command Operations:

Create	Creates a new room outline. Choose an option in the *Create/Edit Options* area of the dialog box.
Edit	Edits an existing room outline.
Move	Moves an existing room outline.
Delete	Deletes an existing room outline.

Room Name

Name	When *Create* is active, names a new room. When *Edit*, *Move* or *Delete* is active, choose from a drop-down menu of existing rooms.

Side of Board (When Create or Edit is active)

Top	Assigns room to top of board.
Bottom	Assigns room bottom of board.
Both	Assigns room to both sides of board.

ROOM_TYPE Properties (When Create or Edit is active)

For more information on the ROOM_TYPE property, see *Using the ROOM and ROOM_TYPE Propertie*s in the *Placing the Elements* user guide in your documentation set.

Room	HARD: Allows components belonging to this room to be placed entirely within its room boundary. DRC errors occur when you place a component outside this room. Any components that are not members of this room, yet are placed entirely within the room boundary, cause DRC errors (U1 in example). SOFT: Generates no DRC errors for any components placed in this room. INCLUSIVE: Results in behavior similar to that produced by the *HARD* value, but DRC errors occur when components belonging to this room straddle the room boundary. HARD_STRADDLE: Results in behavior similar to that produced by the *HARD* value, but allows components belonging to this room to straddle the room boundary without generating DRC errors. DRC errors occur when non-member components are placed completely inside the room boundary. INCLUSIVE_STRADDLE: Results in behavior similar to that produced by the *HARD* value, but allows all components to be placed entirely in the room or to straddle the boundary without generating DRC errors. DRC errors occur when components belonging to this room are placed entirely outside the room.
Design Level	Controls behavior for all rooms in the design without an assigned ROOM_TYPE property, using the same values as above. If no ROOM_TYPE property is found for a room, then SOFT behavior is used.

Create/ Edit Options

When Create is active, the following options display:

Draw Rectangle	Enables you to create and size a rectangle freehand.
Place Rectangle	Enables you to create a rectangle according to dimensions you specify. When selected, two type-in fields appear to accept your dimensions.
Draw Polygon	Enables you to create and size a polygon freehand.

When Edit is active, the following options display:

Available room area used	The amount of room area the components require. (The relationship between the percentage and room area is inverse the larger the percentage, the smaller the room and vice versa). When you expand or contract the room outline the aspect ratio remains constant.
Autosize	Automatically resizes the selected room outline to the percent specified.

Related Topics

- Deleting a Room
- Editing a Room
- Moving a Room

Creating a Room

Follow these steps to create a room:

1. Run room outline.
   The Room Outline dialog box appears.

2. Assign a name to the room by doing one of the following:

   ○ Leave the default room name in the *Name* field.

   ○ Click in the *Name* field, then edit the default room name or replace it with a name of your choosing.

   ○ Click the drop-down next to the *Name* field.

   If any other room names exist, you can choose one of them.

3. Choose either *Top*, *Bottom*, or *Both* to indicate the board layers on which the rooms are to be created.

4. Choose *Soft* as a ROOM_TYPE property value to disable DRC error reporting. -or- Choose to enable DRC error reporting under various placement situations by specifying HARD, INCLUSIVE, HARD_STRADDLE, or INCLUSIVE_STRADDLE as the value of the ROOM_TYPE property.

5. Click *Create* (Create is the default selection when you open the dialog.)
   Choose one of the following buttons that appear on the dialog box (this is the default condition when no room exists):

   ○ Draw Rectangle

     ■ Click *Draw Rectangle*.

     ■ Click one set of coordinates in the board outline.

     ■ Click a different set of coordinates.
       A rectangular room is created.

   ○ Place Rectangle

     ■ To place a rectangle of fixed dimensions, click *Place Rectangle*.
       Two fields appear to the right: Wdt (width) and Hgt (height).

     ■ Use the default values and units that are already entered in the fields, or enter new values. If you enter units other than mil, the value in mil is calculated and substituted.

     ■ Click a coordinate within the board outline.
       A rectangular room with a fixed height and width is created.

   ○ Draw Polygon

     ■ Click *Draw Polygon*.

     ■ Click three or more coordinates in the board outline.

- Click the original starting point to close the polygon.

- Click *OK* in the Outline dialog box.

- Click *Edit*, *Move*, or *Delete* in the Outline dialog box.
  A polygon room is created.

Related Topics

- room outline

- Editing a Room

- Moving a Room

Deleting a Room

Perform the following steps to delete a room:

1. Run `room outline`.
   The Room Outline dialog box appears.

2. Choose an existing room by doing one of the following:

   - Leave the default room name if one appears in the *Name* field.

   - Click in the *Name* field, then enter an existing room name.

   - Click the drop-down next to the *Name* field and choose an existing room name.

   - Click a room in the design.

3. Click *Delete*.
   If the Name field contains a valid room name, a confirmer pops up.

4. Click Yes in the confirmer.
   The room is deleted.

Related Topics

- room outline
- Room Outline Dialog Box
- Moving a Room

Editing a Room

Follow these steps to edit a room:

1. Run `room outline`.
   The Room Outline dialog box appears.

2. Click *Edit*.

3. Choose an existing room by doing one of the following:

   - Click in the *Name* field, then enter an existing room name.

   - Click the drop-down next to the Name field and choose an existing room name from the scroll list.

   - Click a room in the design.

   The room is highlighted, and handles (squares) appear on the corners and midpoints of every line segment.

4. In the design, click any handle on the room.
   The handle attaches to the cursor.

5. Drag the handle to the target coordinates.
   Continuous line segments are automatically merged.

6. To create a new segment within an existing segment, click two points on the existing segment.
   The new segment attaches itself to the cursor.

7. Drag the new segment to the target coordinates.

8. To autosize a room, use the percentage displayed in the Available Room Area Used display area as a basis for calculating a new percentage of available room area.
   The percentage figure represents the amount of room area the components require. This relationship between the percentage and room area is inverse the larger the percentage, the smaller the room (and vice versa). When you expand or contract the room outline the aspect ratio remains constant.

9. Leave the *Autosize To* field set to the default percentage or enter a scale factor.

10. Click *Autosize*.
    The room is resized in relation to the specified scale factor (in percent).

Related Topics

- room outline

- Room Outline Dialog Box

- Creating a Room

Moving a Room

Follow these steps to move a room:

1. Run `room outline`.
   The Room Outline dialog box appears.

2. Click *Move*.

3. Choose an existing room by doing one of the following:

   ○ Leave the room name that appears in the *Name* field.

   ○ Click in the *Name* field, then enter an existing room name.

   ○ Click the drop-down next to the *Name* field and choose an existing room name from the scroll list.

   In the design, an outline of the room and assigned components attaches to the cursor at the lower left corner.

4. Click the target coordinates.
   The room moves to the new location.

Related Topics

- room outline
- Room Outline Dialog Box
- Creating a Room
- Deleting a Room

rotate

The rotate command is used in conjunction with the move and spin commands to rotate an element while it is being moved. The command requires you to enter data into the *Options* panel.

Related Topics

- Rotating an Element During Movement

Rotation Controls: Options Panel

You must set the values in these fields before you choose an element to move. The values have no effect until you run `rotate`.

Type	Specifies the mode of rotation Absolute In this mode, the number entered in the Angle field is the angle at which to rotate the element. When you choose Done from the pop-up menu it automatically turns the element once to match that angle. Incremental controls turning the element, and uses the number entered in the *Angle* field as the amount by which to increment each turn.
Angle	Specifies the angle of rotation; but has a different meaning with each mode. In Incremental mode, this field specifies the number of degrees of each increment as you dynamically rotate the element. In Absolute mode, this field specifies the angle of rotation from the 0,0 orientation; when you choose an element, the element rotates immediately to that angle. Type a number between 0 and 360 or choose an option from the pop-up menu. Choose from: 0, 45, 90, 135, 180, 215, 270, and 315. Accuracy is provided to three decimal places (0.001 degree).
Point	Indicates the position around which the element turns. Symbol Origin : The 0,0 point of the element. Body Center is at the center of an invisible boundary it draws around the very edge of the element. User Pick asks you to choose a point of rotation on the element. **Symbol Pin #** invokes a field in which to enter the number. Symbol Pin # is displayed only when you choose Symbol Pin # as the rotation point. Enter the designated pin number.

Rotating an Element During Movement

To rotate an element during movement:

1. Run `move` or `spin`.

2. Enter the rotation you want into the *Options* panel controls.

3. Choose the element.

4. Type `rotate` at the command console prompt (or choose Rotate from the pop-up menu).

5. If the rotation is incremental, dynamically rotate element to proper angle.

6. Choose destination point for element.

7. Continue choosing elements to move; or choose Done from the pop-up menu.

Related Topics

- rotate

route_by_pick

The `route_by_pick` command lets you route specific nets and components in your design rather than the entire database. When you choose this command, Allegro PCB Router is invoked in the background and a design (`.dsn`) file is created. Cross-probing is also allowed.

> ⓘ The `route_by_pick` command does not automatically protect existing etch when routing. If you want to do this, you must apply the FIXED property to any net that you do not want modified by subsequent routing passes.

If you run the specctra or specctra_out command, any existing etch is protected in the Allegro PCB Router .

Access Using

- *Menu Path* (System Connectivity Manager and Allegro PCB SI products)*:* Route – Route Net(s) by Pick
- *Menu Path* (Allegro Package products)*:* Route – Router – Route by Pick

Routing Specific Nets and Components

To route specific nets and components in your design:

1. Run `route_by_pick`.

   You are prompted to enter a selection point.

2. In the Find filter, choose the object types you want to route. *Components* and *Nets* are on by default.

3. Click one or more objects to route or drag a window around a group of objects.
   The objects are highlighted.

   > ⚠ To deselect a component or net, press the *Control* key and click the component or net you want to deselect.

4. Choose *Route* from the pop-up menu.
   Routing takes place in the background and the design updates with the results of the route.

5. Repeat steps 3 and 4 to perform additional routes or click right and choose one of the options from the pop-up menu, as described below.

Done	Terminates the command, saving any routing performed while the command was active.
Cancel	Terminates the command without saving any routing.
Route	Runs the PCB Router, using the setup parameters established in previous sessions. You might want to choose *Setup* first to see the parameters.
Undo	Removes the results of the last route.
Results	Opens the routing results form to display the results of the current routing session.
Setup	Opens the Automatic Router dialog box.

route priority

The `route priority` command assigns priority to selected nets.

Related Topics

- Assigning a Priority to Nets
- Changing the Priority on Nets
- Removing Any Priority from Nets

Define Net Priority Dialog Box

Access Using

- *Menu Path: Route – Define Net Priority* (in Allegro Package SI products and Allegro PCB SI products)

Net Filter	Uses asterisk as wildcard to narrow the search of available nets. For example, edit the filter to read CLK*.
Priority Filter	Use the asterisk wildcard to limit the display of priority numbers.
Net- Priority window left	Shows all nets allowed by the filter, and priorities assigned to them.
New Priority	Enter a number to assign to a net you will move to the right Net - Priority box.
Net- Priority window right	Shows all nets you have moved by clicking on them in the left side window. All nets in the right side window assume the value entered in the New Priority field.
All ->	Moves all nets (allowed by the filter) into the Nets - Priority window right.
<- All	Moves all nets in the Nets - Priority window right back into the window left.

Related Topics

- Changing the Priority on Nets
- Removing Any Priority from Nets

Assigning a Priority to Nets

To assign a priority to nets, follow these steps:

1. Run `route priority`.
   The Router Priority dialog box appears.

2. Leave the Net Filter and Priority Filter set to `*` to list all available nets or wild cards to narrow the search.

3. Enter an integer into the *New Priority* field.
   The lowest number assigns the highest priority. (Critical nets should have a high priority.) All nets in the right list box assume this new value.

4. Choose individual nets in the left list box.
   Each selected net moves to the right list box and assumes the New Priority value.

5. To move all nets to the right list box, click *All ->*.

6. When you are finished assigning a given priority, click *<- All* to move those nets back to the left list box.

Related Topics

- route priority
- Removing Any Priority from Nets

Changing the Priority on Nets

To change net priority, perform these steps:

1. Run `route priority`.
   The Router Priority dialog box appears.

2. Enter an integer or none into the New Priority field.
   All nets in the right list box assume this new value.

3. Choose individual nets in the left list box.
   Each selected net moves to the right list box and assumes the New Priority value.

4. To move all nets to the right list box, click *All ->*.

5. When you are finished changing the priority, click *<- All*.

6. Repeat the process to change the priority of other nets.

Related Topics

- route priority
- Define Net Priority Dialog Box

Removing Any Priority from Nets

To remove any priority from nets, follow these steps:

1. Run `route priority`.
   The Router Priority dialog box appears.

2. Enter `NONE` in the *New Priority* field.
   All nets in the right list box assume this new value.

3. Choose individual nets in the left list box.
   Each selected net moves to the right list box and assumes the NONE value. A net with a priority of NONE is not autorouted.

4. To move all nets to the right list box, click *All ->*.

Related Topics

- route priority
- Define Net Priority Dialog Box
- Assigning a Priority to Nets

rplan blank

The `rplan blank` command lets you hide graphic feedback from the GRE route engine that shows how it plans to route selected objects in the design. If no objects are selected, then all graphic feedback from the GRE route engine is hidden.

Access Using

- *Menu Path: Display – Blank Router Plan – Of Selection*

Related Topics

- rplan bundled blank_all
- rplan bundled blank
- rplan unbundled blank_all
- rplan blank_all

Hiding Route Plan Lines For Selected Objects

Perform the following steps to hide all route plan lines for selected objects:

1. In IFP application mode, select one or more objects associated with the route plan (bundles, rats, components, pins, etc.)

    ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

    The selected objects highlight and also appear in the *WorldView* window.

2. Choose *Display – Blank Router Plan – Of Selection* from the menu.
    The route plan lines for the selected objects are hidden.

3. Repeat steps 1 and 2 to hide route plan lines for other objects as needed.

rplan blank_all

The `rplan blank_all` command lets you hide graphic feedback from the GRE route engine that shows how it plans to route the design.

Access Using

- *Menu Path: Display – Blank Router Plan – All*

Related Topics

- rplan bundled blank_all
- rplan bundled blank
- rplan unbundled blank_all
- rplan blank

Hiding all Route Plan Lines

1. Choose *Display – Blank Router Plan – All* from the menu.
   All route plan lines are hidden.

rplan bundled blank

The `rplan bundled blank` command lets you hide graphic feedback from the GRE route engine that shows how it plans to route bundled connections associated with selected objects in the design.

Access Using

- *Menu Path: Display – Blank Router Plan – Bundle Plan of Selection*

Related Topics

- rplan bundled blank_all
- rplan blank_all
- rplan unbundled blank_all
- rplan blank

Hiding Route Plan Lines Of Bundled Connections Associated With Selected Objects

Follow these steps to hide route plan lines of bundles connections associated with selected objects:

1. In IFP application mode, select one or more objects associated with the route plan (rats, bundles, nets, components, pins, etc.)

   ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   The selected objects highlight and also appear in the *WorldView* window.

2. Choose *Display – Blank Router Plan – Bundle Plan of Selection* from the menu.
   The route plan lines for the bundles of the selected objects are hidden.

3. Repeat steps1 and 2 to hide route plan lines for bundled connections of other objects as needed.

rplan bundled blank_all

The `rplan bundled blank_all` command lets you hide graphic feedback from the GRE route engine that shows how it plans to route all bundled connections in the design.

Access Using

- *Menu Path: Display – Blank Router Plan – All Bundles*

Related Topics

- rplan unbundled blank_all

- rplan blank_all

- rplan blank

- rplan bundled blank

Routing Plan Lines Of All Bundled Connections In The Design

1. Choose *Display – Blank Router Plan – All Bundles* from the menu.
   The route plan lines of all bundled connections are hidden.

rplan bundled show

The `rplan bundled show` command lets you display graphic feedback from the GRE route engine that shows how it plans to route bundled connections associated with selected objects in the design.

Access Using

- *Menu Path: Display – Show Router Plan – Bundle Plan of Selection*
- Right Mouse Button Option: *Show Bundle Router Plan*

Related Topics

- rplan bundled show_all
- rplan show
- rplan unbundled show_all
- rplan show_all

Displaying Route Plan Lines of Bundled Connections Associated with Selected Objects

Perform these steps to display the route plan lines of bundled connections associated with selected objects:

1. In IFP application mode, select one or more objects associated with the route plan (rats, bundles, nets, components, pins, and so on.)

   > ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   For tips on multi-object selection, see the Object Selection Shortcuts table.
   The selected objects highlight and also appear in the *WorldView* window.

2. With your cursor on a selected object, right-click and choose *Show Bundle Router Plan* from the menu.
   The route plan lines of bundled connections associated with selected objects display.

3. Repeat steps1 and 2 to display route plan lines of bundled connections associated with other objects as needed.

rplan bundled show_all

The `rplan bundled show_all` command lets you display graphic feedback from the GRE route engine that shows how it plans to route all bundled connections in the design.

Access Using

- *Menu Path: Display – Show Router Plan – All Bundles*

Related Topics

- rplan bundled show
- rplan show
- rplan unbundled show_all
- rplan show_all

Displaying Route Plan Lines For All Bundled Connections

1. Choose *Display – Show Router Plan – All Bundles* from the menu.
   The route plan lines for all bundled connections appear.

rplan bundled toggle

The `rplan bundled toggle` command lets you reverse the display state of graphic feedback from the GRE route engine that shows how it plans to route bundled connections in the design. When no objects are selected, plan lines of bundled connections that are displayed are hidden. If all plan lines of bundled connections were previously hidden, they are all displayed. When design objects are selected, the command determines the current visibility state for plan lines of associated bundled connections and reverses it.

> ⊘ For convenience, consider mapping this command to a function key. See the funckey command for details.

Related Topics

- Toggling the Display of Route Plan Lines for All Bundled Connections in the Design

- rplan unbundled toggle

- rplan toggle

rplan commit

The `rplan commit` command instructs the GRE route engine to convert existing route plan lines to etch (c-lines and vias) in the design database.

Access Using

- *Menu Path: FlowPlan – Commit Plan*

- Right Mouse Button Menu Option: *Commit Plan*

- Toolbar Icon:

Related Topics

- Committing All Existing Route Plan Lines In The Design

- rplan plan_accurate

- rplan_plan_topological

- rplan status

- rplan optimize

Committing Existing Route Plan Lines Associated with Selected Objects

To commit existing route plan lines associated with selected objects, perform these steps:

1. In IFP application mode, select one or more objects associated with the route plan (nets, components, bundles, pins, or rats).

   > ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   The selected objects highlight and also appear in the *WorldView* window.

2. With your cursor on a selected object, right-click and choose *Commit Plan* from the menu.
   The plan lines associated with the selected objects are converted to etch.

3. Repeat steps1 and 2 to commit plan lines associated with other objects as needed.

Committing All Existing Route Plan Lines In The Design

To commit all existing route plan lines in the design:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Choose *FlowPlan – Commit Plan* from the menu bar.
   A message appears asking if you want to commit the entire plan.

3. Click the *Yes* button in the message dialog box.
   All route plan lines for the entire design are converted to etch.

Related Topics

- rplan commit

rplan convert

The `rplan convert` command down-converts c-lines, vias, and applicable plan data to the plan level that is specified with a command option. Valid command options are `spatial` or `topological`. When the option is unspecified, the default is `spatial`.

The resulting plan data is more easily modified by the GRE route engine during re-planning operations. The command lets you select a mixture of c-lines and plan data. However, only applicable plan data is processed. For example, when using the `spatial` command option, spatial plan data is ignored. Plan DRC's are updated after the conversion so that markers appear in cases where resulting connections are in violation.

Related Topics

- rplan convert spatial
- rplan convert topological

rplan convert spatial

The `rplan convert spatial` command down-converts c-lines, vias, and applicable plan data to a plan level of spatial. The resulting plan data is more easily modified by the GRE route engine during re-planning operations. The command lets you select a mixture of c-lines and plan data. However, only applicable plan data is processed. For example, spatial plan data is ignored. Plan DRC's are updated after the conversion so that markers appear in cases where resulting connections are in violation.

Access Using

- *Menu Path: FlowPlan – Convert – to Spatial*

- Right Mouse Button Menu Option: *Convert – to Spatial*

Related Topics

- Converting All C-Lines and Plan Data in the Design to a Plan Level of Spatial

- rplan convert topological

Converting Selected C-Lines And Plan Data to a Plan Level of Spatial

You can convert selected clines and plan data to plan level of spatial by following these steps:

1. In IFP application mode, select one or more objects (nets, components, bundles, pins, or rats) associated with the c-lines and plan data that you want to convert.

   ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   The selected objects highlight and also appear in the *WorldView* window.

2. With your cursor on a selected object, right-click and choose *Convert – to Spatial* from the menu. The selected c-lines and plan data is down-converted to a plan level of spatial. All non-applicable plan data is ignored.

Converting All C-Lines and Plan Data in the Design to a Plan Level of Spatial

To convert all clines and plan data in the design to a plan level of spatial:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Choose *Flowplan – Convert – to Spatial* from the Allegro menu bar.
   A dialog box appears asking you to confirm the operation.

3. Click *Yes* to confirm the conversion.

4. All c-lines and plan data in the design is down-converted to a plan level of spatial. All non-applicable plan data is ignored.

Related Topics

- rplan convert spatial

rplan convert topological

The `rplan convert topological` command down-converts c-lines, vias, and applicable plan data to a plan level of topological. The resulting plan data is more easily modified by the GRE route engine during re-planning operations. The command lets you select a mixture of c-lines and plan data. However, only applicable plan data is processed. For example, spatial and topological plan data is ignored. Plan DRC's are updated after the conversion so that markers appear in cases where resulting connections are in violation.

Access Using

- *Menu Path: FlowPlan – Convert – to Topological*

- Right Mouse Button Menu Option: *Convert – to Topological*

Related Topics

- Converting All C-Lines and Plan Data in the Design to a Plan Level of Topological

- rplan convert spatial

Converting Selected C-Lines and Plan Data to a Plan Level of Topological

You can convert selected clines and plan data to plan level of topological by following these steps:

1. In IFP application mode, select one or more objects (nets, components, bundles, pins, or rats) associated with the c-lines and plan data that you want to convert.

   ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   The selected objects highlight and also appear in the *WorldView* window.

2. With your cursor on a selected object, right-click and choose *Convert – to Topological* from the menu. The selected c-lines and plan data is down-converted to a plan level of topological. All non-applicable plan data is ignored.

Converting All C-Lines and Plan Data in the Design to a Plan Level of Topological

To convert all clines and plan data in the design to a plan level of topological:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Choose *Flowplan – Convert – to Topological* from the Allegro menu bar.
   A dialog box appears asking you to confirm the operation.

3. Click *Yes* to confirm the conversion.

4. All c-lines and plan data in the design is down-converted to a plan level of topological. All non-applicable plan data is ignored.

Related Topics

- rplan convert topological

rplan delete

The `rplan delete` command removes route plan lines associated with selected objects in the design. If no objects are selected, then all route plan lines in the design are removed.

Access Using

- *Menu Path: FlowPlan – Delete Plan*

- Right Mouse Button Menu Option: *Delete Plan*

Related Topics

- Deleting All Route Plan Lines In The Design

- rplan plan_accurate

- rplan_plan_topological

- rplan status

- rplan optimize

Deleting Existing Route Plan Lines Associated With Selected Objects

You can delete existing route plan lines associated with selected objects by following these steps:

1. In IFP application mode, select one or more objects associated with the route plan (nets, components, bundles, pins, or rats).

   ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   The selected objects highlight and also appear in the *WorldView* window.

2. With your cursor on a selected object, right-click and choose *Delete Plan* from the menu.
   The plan lines associated with the selected objects are removed from the design.

Deleting All Route Plan Lines In The Design

You can delete all route plan lines in the design by performing these steps:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Choose *FlowPlan – Delete Plan* from the menu.
   A message appears asking if you want to delete the plan lines in the entire design.

3. Click the *Yes* button in the message dialog box.
   All route plan lines in the design are removed.

Related Topics

- rplan delete

rplan optimize

The `rplan optimize` command instructs the GRE route engine to optimize the connections (etch only) associated with selected objects in the design. If no objects are selected, then the connections for the entire design are optimized. Optimization attempts to improve pin/pad entry and make other quality interconnect improvements by exceeding what design constraints currently specify.

> ⓘ This command operates on c-lines only and returns plan lines that must be committed back to c-lines. For details on committing plan lines to c-lines, see the rplan commit command.

Related Topics

- Optimizing Route Plan Data Associated With Selected Objects

- Optimizing All Route Plan Data In The Design

- rplan plan_accurate

- rplan_plan_topological

- rplan status

- rplan plan_spatial

Plan Progress Dialog Box

Access Using

- *Menu Path: FlowPlan – Optimize*

- Right Mouse Button Menu Option: *Net – Optimize*

⚠ You can right-click in the cells of this dialog box to access additional commands.

Command Completion	Shows the overall progress of the plan phase by indicating a percentage of plan tasks completed thus far.
Task Completion	Shows the individual progress of each plan task.
Automatic	When enabled (checked), specifies a user-defined time interval for the display of periodic updates of the graphic plan data in the canvas. ⚠ Updates are pre-empted when an interactive command is in progress. This includes a manual update (*Update Now*). When the interactive command finishes, the update is resumed.
Update Now	Requests an immediate update to the plan data and overrides the currently specified *Automatic* time interval.
Object	Specifies the name of the design object that status is being reported for. In addition to design objects, the following items are included at the top of the list:
	DesignSummary *SelectionSummary* *RandomLogic* — The entire design. Pre-selected objects. Unbundled connections.
Guided	Specifies whether the GRE route engine is being guided by the bundle flow line.
Rat Count	Specifies the number of rats or connections in the bundle.
Unroutes	Specifies the number of unroutes that remain in the plan.

Plan Level	The level of planning that has been completed thus far for elements associated with the object.
	⚠ If the object has associated elements with mixed levels of planning completed, then the value displayed is the lowest level of planning that has been completed for all elements.
	Plan level values are:

	Spatial Topological Accurate Clines	Spatial planning completed. Topological Planning completed. Accurate planning completed. Committed plan or existing etch.

Via Count	The number of vias used in the plan.
Overloads	Specifies the unique number of overloaded spaces that were found in the plan.
	⚠ A space is overloaded when there are more objects passing through it than can physically fit due to spacing or clearance rules.
Crossing Errors	Specifies the unique number of crossover errors that were found in the plan.
Delay Errors	Specifies the number of delay errors that remain in the plan. This includes: Min/max physical delay Relative delay Match group delay
	⚠ It does not include delay issues for differential pairs such as uncoupled length and phase mismatch.
Diff Pair Errors	Specifies the number of errors that remain in the plan for differential pairs in the bundle.
	⚠ This number is a summation of any Allegro supported DRC errors for differential pairs.
Electrical Errors	Specifies the number of electrical constraint violations other than delay or differential pair errors. This includes: Max via count violations Max exposed length violations Layer set violations Impedance violations Stub length violations Crosstalk violations

Pause/Resume	Temporarily pauses the Plan phase after the current connection is complete. Once the Plan phase is paused, the button label changes to *Resume* and can be used to continue the plan run.
	⚠ While the Plan phase is paused, you cannot change any parameters that may affect planning. You can, however, change visibility settings.
Stop	Stops the Optimize phase after its current connection is complete and displays graphical plan data in the design.
	⚠ If the GRE route engine is routing a bundle when the stop is requested, that bundle's plan data is reverts back to its last known good state.
View Log	Displays the current GRE route plan log file.

Related Topics

- Optimizing All Route Plan Data In The Design
- Plan Dialog Cell Commands

Optimizing Route Plan Data Associated With Selected Objects

Follow these steps to optimize the route plan data associated with selected objects:

1. In IFP application mode, select one or more objects associated with the route plan (bundles, nets, components, pins, rats, c-lines, etc.)

   ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   The selected objects highlight and also appear in the *WorldView* window.

2. With your cursor on a selected object, right-click and choose *Optimize* from the menu.
   The Optimize Progress dialog box appears and connections for the selected objects are optimized.

3. Repeat steps1 and 2 to optimize route plan data associated with other objects as needed.

Related Topics

- rplan optimize

Optimizing All Route Plan Data In The Design

Perform the following steps to optimize all route plan data in the design:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Choose *FlowPlan – Optimize* from the menu.
   The Optimize Progress dialog box appears and all connections in the design are optimized.

Related Topics

- rplan optimize
- Plan Progress Dialog Box

rplan plan

The `rplan plan` command instructs the GRE route engine to re-run the last plan operation for the connections of selected objects in your design. If no objects are selected, then the last plan operation is re-run for all connections in the design.

⊘ This command is convenient to use when you want to plan the connections of several objects, one at a time, using the same plan phase. This gives you an opportunity to check object-specific plan results in between plan runs.

Related Topics

- GRE View Errors Dialog Box
- Planning Routes Associated with Selected Objects
- Planning All Routes in the Design
- rplan status
- rplan_plan_topological
- rplan plan_spatial
- rplan_plan_accurate
- rplan optimize
- rplan commit

Plan Dialog Cell Commands

Except for column head cells, you can make multi-cell selections for these commands using either a mouse-drag, a Ctrl-click, or a Shift-click.

Right-click with the cursor in . . .	Command	Function
a column head cell	*Sort Ascending*	Sorts column data in ascending order. A double-click in the column head cell also performs this function if this is not the current sort column or if the previous sort was descending.
a column head cell.	*Sort Descending*	Sorts column data in descending order. A double-click in the column head cell also performs this function if this is not the current sort column or if the previous sort was ascending.
a bundle cell in the *Object* column.	*Select*	Selects and zooms to the named object in the design canvas. A double-click in the bundle cell also performs this function.
a bundle cell in the *Object* column.	*Select and Show Element*	Selects and zooms to the named object in the design canvas and displays the Show Element dialog box.
a bundle cell in the *Object* column.	*Deselect*	Deselects the named object.
a bundle cell in the *Object* column.	*View Errors*	Shows all plan DRC errors associated with the *Object* cell. The following actions are performed: • Displays the View Errors dialog box and reports applicable plan DRC errors. • Highlights applicable plan DRC errors in the design canvas with the option to zoom the display to a specific error using the DRC marker location link in the report.

a bundle cell in the *Object* column.	*Plan*	Selects the named object and runs a planning command that you choose from the sub-menu. For a bundle cell, the entire bundle is planned. Choices are: *Spatial* - Runs the `rplan spatial` command. *Topological* - Runs the `rplan topological` command. *Accurate* - Runs the `rplan accurate` command.
an error cell for a bundle. For example, *Overloads*.	*View Errors*	Shows plan DRC errors of the type specified (per chosen error column) that are associated with the rats of the selected bundle (per chosen *Object* row). The following actions are performed: • Displays the View Errors dialog box and reports applicable plan DRC errors. • Highlights applicable plan DRC errors in the design canvas with the option to zoom the display to a specific error using the DRC marker location link in the report. A double-click in the error cell also performs this function.

Related Topics

- GRE View Errors Dialog Box

GRE View Errors Dialog Box

⚠ Similar errors displayed in this report are listed together using the following sort priority: error type, subclass, x-location, y-location. When multi-cell selection is used, errors in this report are also grouped by bundle.

📌	Sticks the dialog box to the design canvas so that it remains open.
🖱	Un-sticks the dialog box from the design canvas so that it can close.

✕	Closes the dialog box.
💾	Saves the report to a named file.
🖨	Prints the report.
Search:	Searches the report to find instances of a specified text string. Press the Enter key consecutively to find the next instance.
☐ Match word	When enabled (checked), searches only for whole words containing the specified string.
☐ Match case	When enabled (checked), searches for the specified string considering its font case (exactly as entered).
Bundle / Constraint	Column specifying the names of the bundle objects being reported. In addition to the bundle name, the constraint name associated with a plan DRC is shown when applicable.
DRC Marker Location	Column specifying the coordinates of the plan DRC marker location in the design canvas. ⊘ You can click on the location link in the report to center the canvas on the DRC marker for closer examination.
Subclass	Column specifying the subclass (layer) associated with the plan DRC.
Required Value	Column specifying the required constraint value associated with the plan DRC.
Actual Value	Column specifying the actual constraint value associated with the plan DRC.
Element 1	Column specifying the name of the first design object associated with the plan DRC error. ⊘ You can verify the design objects associated with an error by using *DRC Marker Location*, hovering your cursor over the plan DRC marker, and noting which objects highlight in the design canvas.

Element 2	Column specifying the name of the second design element associated with the plan DRC error.
	⊘ You can verify the design objects associated with an error by using *DRC Marker Location*, hovering your cursor over the plan DRC marker, and noting which objects highlight in the design canvas.

Related Topics

- rplan plan
- Planning All Routes in the Design

Planning Routes Associated with Selected Objects

Planning All Routes in the Design

To plan all routes in the design:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Choose *FlowPlan – Plan – Plan Accurate* from the menu.
   The Plan Accurate Progress dialog box appears. All routes are planned and plan lines appear in the design.

Related Topics

- rplan plan

- Plan Progress Dialog Box

- GRE View Errors Dialog Box

rplan plan accurate

The `rplan plan accurate` command instructs the GRE route engine to develop and display accurate level plan data for the connections of selected objects in your design. If no objects are selected, then accurate level plan data is developed and displayed for all connections in the design. Accurate plan data is detailed and meets electrical as well as physical design constraints. As the command is running, the Plan Progress dialog box is displayed to provide feedback on the plan run.

Accurate Plan Status

Once the plan accurate level has been achieved for a connection, its status label is set to *Plan=Accurate* in the design. However, a bundle achieves accurate status only when all of its members have achieved that plan level. Otherwise, a bundle's status is set to match the plan status of the member with the lowest level of planning.
You can display the plan status label for a connection (plan line, rat, or bundle) by hovering your cursor over it in the canvas. Alternately, you can use the `rplan status` command to check the plan level.

Connections that have achieved a plan level of Accurate meet the following criteria.

Accurate Success Criteria
Topological requirements satisfied
Electrical constraints met

Related Topics

- Planning Accurate Routes Associated With Selected Objects

- Planning All Routes In The Design Accurately

- rplan commit

- rplan optimize

- rplan_plan_topological

- rplan status

- rplan plan_spatial

Planning Accurate Routes Associated With Selected Objects

Perform the following steps to plan accurate routes associated with selected objects:

1. In IFP application mode, select one or more objects associated with the route plan (bundles, nets, components, pins, rats, c-lines, etc.)

   ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   The selected objects highlight and also appear in the *WorldView* window.

2. With your cursor on a selected object, right-click and choose *Plan – Plan Accurate* from the menu. The Plan Accurate Progress dialog box appears. Routes for the connections of selected objects are planned and plan line feedback is displayed in the canvas.

3. Repeat steps1 and 2 to accurately plan the routes associated with other objects as needed.

Related Topics

- rplan plan accurate
- object selection shortcuts

Planning All Routes In The Design Accurately

To accurately plan all routes in the design, follow these steps:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Choose *FlowPlan – Plan – Plan Accurate* from the menu.
   A message appears asking if you want to plan the entire design.

3. Click the *Yes* button in the message dialog box.
   The Plan Accurate Progress dialog box appears. Routes for all connections in the design are planned and plan line feedback is displayed in the canvas.

Related Topics

- rplan plan accurate
- Plan Progress Dialog Box

rplan plan spatial

The `rplan plan spatial` command instructs the GRE route engine to develop and display plan data that is spatially correct for the connections of selected objects in your design. If no objects are selected, then spatial level plan data is developed and displayed for all connections in the design. Spatial plan data is assigned a routing channel and adheres to line width and line spacing constraints. As the command is running, the Plan Progress dialog box is displayed to provide feedback on the plan run.

Spatial Plan Status

Once spatial planning has been achieved for a connection, its status label is set to *Spatial* in the design. Otherwise, it is set to *Unplanned*. However, a bundle achieves Spatial status only when all of its members have achieved that plan level. Otherwise, a bundle's status is set to match the status of the member with the lowest level of planning.
You display the plan status label for a connection (plan line, rat, c-line, net, etc.) or bundle by hovering your cursor over it in the canvas. Alternately, you can use the `rplan status` command to check the plan status of bundles associated with selected objects in the design.

Connections that have achieved a plan level of Spatial meet the following criteria.

Spatial Success Criteria
Initial routing channel assigned
Spatial constraints (line width and line spacing) met
Layer usage (layer sets) met
Differential pair connections are gathered and coupled
No unroutes
No crossovers
No overloads
No chaining order errors

⚠ Spatial plan data cannot be converted to c-lines. Connections must achieve a plan status of Topological or better to be eligible for commitment to etch.

Related Topics

- Planning Routes Associated with Selected Objects, Quickly

- Planning All The Routes In The Design Quickly

- rplan_plan_topological

- rplan optimize

- rplan_plan_accurate

- rplan commit

- rplan status

Planning Routes Associated with Selected Objects, Quickly

Follow these steps to quickly plan routes associated with selected objects:

1. In IFP application mode, select one or more objects associated with the route plan (bundles, nets, components, pins, rats, c-lines, and so on).

   > ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   For tips on multi-object selection, see the Object Selection Shortcuts table.
   The selected objects highlight and also appear in the *WorldView* window.

2. With your cursor on a selected object, right-click and choose *Plan – Plan Spatial* from the menu.
   The Plan Spatial Progress dialog box appears. Routes for the connections of selected objects are planned and plan line feedback is displayed in the canvas.

3. Repeat steps1 and 2 to quickly plan the routes associated with other objects as needed.

Related Topics

- rplan plan spatial

Planning All The Routes In The Design Quickly

You can plan all the routes in the design quickly by following these steps:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Choose *FlowPlan – Plan – Plan Spatial* from the menu.
   A message appears asking if you want to plan the entire design.

3. Click the *Yes* button in the message dialog box.
   The Plan Spatial Progress dialog box appears. Routes for all the connections in the design are planned and plan line feedback is displayed in the canvas.

Related Topics

- rplan plan spatial
- Plan Progress Dialog Box

rplan plan topological

The `rplan plan topological` command instructs the GRE route engine to develop and display plan data that is topologically correct for the connections of selected objects in your design. If no objects are selected, then topological level plan data is developed and displayed for all connections in the design. Topological plan data is detailed and more refined than spatial plan data while continuing to meet all physical constraints. As the command is running, the Plan Progress dialog box is displayed to provide feedback on the plan run.

Topological Plan Status

Once Topological planning has been achieved for a connection, its status label is set to *Topological* in the design. However, a bundle achieves Topological status only when all its members have achieved that plan level. Otherwise, the bundle's plan status is set to match the status of the member with the lowest level of planning.
You display the status label for a connection (plan line, rat, or net) or bundle by hovering your cursor over it in the canvas. Note that IFP application mode must be enabled to view plan status labels. Alternately, you can use the `rplan status` command to check the plan status of bundles associated with selected objects in the design.

Connections and bundles that have achieved a plan level of Topological meet the following success criteria.

Topological Success Criteria
Spatial requirements satisfied
Physical constraints re-checked and met
Differential pair connections are in phase, and have improved pin/pad entry.

Related Topics

- Plan Progress Dialog Box

- Planning Routes Topologically Associated With Selected Objects

- Planning All Routes Topologically In The Design

- rplan plan_spatial

- rplan optimize

- rplan_plan_accurate

- rplan commit

- rplan status

Planning Routes Topologically Associated With Selected Objects

Perform these steps to plan routes topologically associated with selected objects:

1. In IFP application mode, select one or more objects associated with the route plan (bundles, nets, components, pins, rats, c-lines, etc.)

   ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   The selected objects highlight and also appear in the *WorldView* window.

2. With your cursor on a selected object, right-click and choose *Plan – Plan Topological* from the menu. The Plan Topological Progress dialog box appears. Routes for the connections of selected objects are planned and plan line feedback is displayed in the canvas.

3. Repeat steps1 and 2 to topologically plan the routes associated with other objects as needed.

Related Topics

- rplan plan topological
- object selection shortcuts

Planning All Routes Topologically In The Design

To plan all routes topologically in the design, follow these steps:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Choose *FlowPlan – Plan – Plan Topological* from the menu bar.
   A message appears asking if you want to plan the entire design.

3. Click the *Yes* button in the message dialog box.
   The Plan Topological Progress dialog box appears. Routes for all the connections in the design are planned and plan line feedback is displayed in the canvas.

Related Topics

- rplan plan topological
- Plan Progress Dialog Box

rplan progress

You can use the `rplan progress` command to re-display the Plan Progress dialog box while a planning phase is active and the Plan Progress dialog box is either hidden or minimized.

Access Using

- Right Mouse Button Menu Option: *Progress of Active Planning*

Related Topics

- rplan status

Re-displaying the Plan Progress Dialog Box

1. Right-click in a blank area of the design canvas and select *Progress of Active Planning* from the menu.

rplan show

The `rplan show` command lets you display graphic plan feedback from the GRE route engine that shows how it plans to route the connections of selected objects in the design.

Access Using

- *Menu Path: Display – Show Router Plan – Of Selection*

Related Topics

- rplan show_all
- rplan bundled show_all
- rplan bundled show
- rplan unbundled show_all

Displaying Route Plan Lines For Selected Objects

To display route plan lines for selected objects, perform these steps:

1. In IFP application mode, select one or more objects associated with the route plan (bundles, rats, components, pins, etc.).

   ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   For tips on multi-object selection, see the Object Selection Shortcuts table.
   The selected objects highlight and also appear in the *WorldView* window.

2. Choose *Display – Show Router Plan – Of Selection* from the menu.
   The route plan lines for the selected objects appear.

3. Repeat steps 1 and 2 to display router plan lines for other objects as needed.

rplan show_all

The `rplan show_all` command lets you display graphic plan feedback from the GRE route engine that shows how it plans to route all connections in the design.

Access Using

- *Menu Path: Display – Show Router Plan – All*

Related Topics

- rplan show
- rplan bundled show_all
- rplan bundled show
- rplan unbundled show_all

Displaying All Route Plan Lines

1. Choose *Display – Show Router Plan – All* from the menu.
   Route plan lines appear for all connections in the design.

rplan status

The `rplan status` command displays the route plan status of connections associated with one or more selected objects (such as bundles, rats, nets, and components). If no objects are selected, then the route plan status for all connections in the design are displayed.

Related Topics

- Displaying The Route Plan Status Of Selected Objects

- Displaying The Route Plan Status For The Entire Design

- rplan commit

- rplan optimize

- rplan plan topological

- rplan plan

- rplan plan spatial

- rplan plan accurate

Plan Status Dialog Box

Access Using

- *Menu Path: FlowPlan – Plan Status*

- Right Mouse Button Menu Option: *Plan Status*

- Toolbar Icon:

⚠ You can right-click in the cells of this dialog box to access additional commands.

Object	Specifies the name of the rat bundle that plan status is being reported for. In addition to individual bundle names, the following items are included at the top of the list:	
	DesignSummary SelectionSummary RandomLogic	All connections in the design Connections of pre-selected objects Unbundled connections
Guided	Specifies whether the GRE route engine was guided by the bundle flow line.	
Rat Count	Specifies the number of rats in the connection.	
Unroutes	Specifies the number of unroutes that remain in the design.	
Plan Level	The level of planning that was completed for elements associated with the object. ⚠ If the object has associated elements with mixed levels of planning completed, then the value displayed is the lowest level of planning that was completed for all elements. Plan level values are:	
	Unplanned Spatial *Topological Accurate* Optimize *Clines*	Planning not completed. Spatial planning completed. Topological planning completed. Accurate planning completed. Plan optimization completed. Committed plan or existing etch.
Via Count	The number of vias used to route the connections associated with the object. ⚠ This number includes existing fanout vias.	

Overloads	Specifies the unique number of overloaded spaces that were found in the plan. ⚠ A space is overloaded when there are more objects passing through it than can physically fit due to spacing or clearance rules.
Crossing Errors	Specifies the unique number of crossover errors that were found in the plan.
Delay Errors	Specifies the number of delay errors that remain in the plan. This includes: Min/max physical delay Relative delay Match group delay ⚠ It does not include delay issues for differential pairs such as uncoupled length and phase mismatch.
Diff Pair Errors	Specifies the number of errors that remain in the plan for differential pairs in the bundle. ⚠ This number is a summation of any Allegro supported DRC errors for differential pairs.
Electrical Errors	Specifies the number of electrical constraint violations other than delay or differential pair errors. This includes: Max via count violations Max exposed length violations Layer set violations Impedance violations Stub length violations X-talk violations
View Log	Displays the current GRE route plan log file that shows additional information about the route plan run.

Related Topics

- Displaying the Route Plan Status for the Entire Design
- Plan Dialog Cell Commands

Displaying The Route Plan Status Of Selected Objects

To display the route plan status for selected objects, perform these steps:

1. In IFP application mode, select one or more objects associated with the route plan (bundles, nets, components, pins, rats, etc.).

   > ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   For tips on multi-object selection, see the Object Selection Shortcuts table.
   The selected objects highlight and also appear in the *WorldView* window.

2. With your cursor on a selected object, right-click and choose *Plan Status* from the menu.
   The Plan Status dialog box appears and displays the status for connections associated with the selected objects.

3. Repeat steps1 and 2 to display the plan status of other objects as needed.

Related Topics

- rplan status

Displaying The Route Plan Status For The Entire Design

To display the route plan status for the entire design:, perform these steps:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Click on the `rplan status` icon in the FlowPlan toolbar.
   - or -
   Choose *FlowPlan – Plan Status* from the menu bar.
   The Plan Status dialog box appears and displays the status for all connections in the design.

Related Topics

- rplan status
- Plan Status Dialog Box

rplan toggle

The `rplan toggle` command lets you reverse the display state of graphic feedback from the GRE route engine that shows how it plans to route all connections in the design (bundled and unbundled). When no route plan lines in the design are selected, those that are displayed are hidden. If all plan lines were previously hidden, they are all displayed. When plan lines are selected, the command determines their current visibility state and reverses it.

Access Using

- Toolbar Icon:

Related Topics

- Toggling The Display Of All Route Plan Lines In The Design
- rplan bundled toggle
- rplan unbundled toggle

Toggling The Display Of Selected Route Plan Lines In The Design

To toggle the display of selected route plan lines in the design, perform these steps:

1. In IFP application mode, select one or more route plan lines in the design.

   ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   For tips on multi-object selection, see the Object Selection Shortcuts table.
   The selected plan lines highlight and also appear in the *WorldView* window.

2. Click on the `rplan toggle` icon in the toolbar.

   The visibility state of all selected plan lines is reversed.

Toggling The Display Of All Route Plan Lines In The Design

To toggle the display of all route plan lines in the design, perform these steps:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Click on the `rplan toggle` icon in the FlowPlan toolbar.
   All route plan lines in the design previously displayed are hidden.
   - or -
   If all route plan lines were previously hidden, they are all displayed.

Related Topics

- rplan toggle

rplan unbundled blank_all

The `rplan unbundled blank_all` command lets you hide graphic feedback from the GRE route engine that shows how it plans to route all random logic in the design.

Access Using

- *Menu Path: Display – Blank Router Plan – All Random Logic*

Related Topics

- rplan bundled blank_all
- rplan bundled blank
- rplan blank_all
- rplan blank

Hiding Route Plan Lines For All Random Logic

1. Choose *Display – Blank Router Plan – All Random Logic* from the menu.
   The route plan lines for all random logic are hidden.

rplan unbundled show_all

The `rplan unbundled show_all` command lets you display graphic feedback from the GRE route engine that shows how it plans to route all the random logic in the design.

Access Using

- *Menu Path: Display – Show Router Plan – All Random Logic*

Related Topics

- rplan bundled show_all
- rplan bundled show
- rplan show all
- rplan show

Displaying Route Plan Lines For All Random Logic

1. Choose *Display – Show Router Plan – All Random Logic* from the menu.
   The route plan lines for all random logic appear.

rplan unbundled toggle

The `rplan unbundled toggle` command lets you reverse the display state of graphic feedback from the GRE route engine that shows how it plans to route unbundled connections in the design. When no objects are selected, plan lines of unbundled connections that are displayed are hidden. If all plan lines of unbundled connections were previously hidden, they are all displayed. When design objects are selected, the command determines the current visibility state for plan lines of associated unbundled connections and reverses it.

> ⊘ For convenience, consider mapping this command to a function key. See the funckey command for details.

Related Topics

- rplan bundled toggle

- rplan toggle

Toggling The Display Of Route Plan Lines For Bundled Connections Associated With Selected Objects In The Design

To toggle the display of route plan lines for bundled connections associated with selected objects in the design, perform these steps:

1. In IFP application mode, select one or more objects in the design (nets, components, bundles, pins, or rats).

   > ⊘ Design density may make object selection difficult. You can limit the find criteria to just one type of object by right-clicking in the Design window, then choosing *Super filter – <object_type>* from the menu.

   For tips on multi-object selection, see the Object Selection Shortcuts table.
   The selected plan lines highlight and also appear in the *WorldView* window.

2. Type `rplan unbundled toggle` in the Command Console window.

   The visibility state for plan lines of unbundled connections associated with the selected objects is reversed.

Toggling The Display Of Route Plan Lines For All Bundled Connections In The Design

To toggle the display of route plan lines for all bundled connections in the design, perform these steps:

1. Ensure that nothing in the canvas is selected. In IFP application mode, right-click in the canvas background and choose *Selection set – Clear all selections* from the menu.

2. Type `rplan unbundled toggle` in the Command Console window.
   All route plan lines for unbundled connections in the design previously displayed are hidden.
   - or -
   If all route plan lines for unbundled connections were previously hidden, they are all displayed.

Related Topics

- rplan unbundled toggle

rpn

Automatic die pad renumbering lets you easily renumber die pads when it becomes necessary to alter their positions in a symbol drawing (.dra). This most typically occurs when you need to stagger aligned pins to reduce the spacing between them.

By setting parameters in the *Options* panel, you can renumber die pads starting with any number, as well as in any direction. You can also automatically set spacing requirements for rows/columns of die pads, and edit text.

In most instances, pin renumbering is performed on pin layouts one side at a time. For example, on a 4-sided peripheral pin layout, you would perform the renumbering function four times.

ⓘ This command is available only in the Allegro Package Symbol Editor.

Related Topics

- Renumbering Pins Automatically
- Renumbering Pins to a Specific Sequence

RPN Command: Options Panel

Access Using

- *Menu Path: Layout – Pin Renumbering*

Re-Number Pin	Click to activate the Start Pin Number option. If you do not activate this option, pin numbers remain the same though you can use the other options to modify the appearance of the numbers and the spacing of staggered pins.
Start Pin Number	Enter a starting pin number for the selected pin array block. The number sequence does not affect pin numbers outside the array you choose. Choose the direction of pin numbering from the options: top-to-bottom, right-to-left, left-to-right, bottom-to-top.
Compress Pin	This feature lets you automatically compress an entire pin array. Click to activate the Staggered Pin Spacing option.
Staggered Pin Spacing	This option lets you set minimum spacing compression for selected pin blocks. Enter the value in design units (established in Setup > Drawing Size) by which staggered pins will be spaced. Note that you must move pins into a staggered formation before applying this option. Pin arrays that are aligned horizontally/vertically (that is, not staggered) are not affected.
Text Parameters	Set the text fields to display the correct size and location of the pin numbers appropriate to your design. These setting are implemented in the pin array you choose.

Related Topics

- Renumbering Pins to a Specific Sequence

Renumbering Pins Automatically

- If you are adding new pins to your drawing, run add pin.

- If new or existing pins need to be staggered, use the move command to form the specified pattern.

> ⚠ Note: the Compress Pin feature in the *Options* panel does not automatically stagger pins according to the space setting.

When you renumber pins automatically you can click the right mouse button and use the following options to choose multiple pins:

Use	To...
Temp Group	Choose individual pins in an array for renumbering/staggering
Complete	Complete your selection of pins in a temporary group

1. Run `rpn`. The *Options* panel displays the pin numbering parameters.

2. When you have set the options (as described above), click and drag the left mouse button to choose the pin array to be renumbered and/or staggered. A bounding box appears around the pin array you choose. When you release the mouse button, the pin array renumbers according to the option settings.

   - If you choose only pin renumbering, the pin numbers change and appear after you choose the pin array.

   - If you choose pin compression, the pin array is highlighted and you are prompted to choose a stationary pin. Click on the pin that remains stationary during the compression process. The pin array spacing changes according to the option settings.

3. When the pins are renumbered, click right and choose *Done* from the pop-up menu.

Related Topics

- rpn

Renumbering Pins to a Specific Sequence

If, in the process of editing pins, you have a broken sequence of pin numbers that you want to resequence, you must first renumber the pins starting with a number greater than the last pin number, and then renumber the pins again from 1 to the end.

For example, if you have a PGA with pin numbers 1 to 7 and then 10 to 18, renumber the pins as follows:

1. Run `rpn`.

2. Set the Start Pin Number in the *Options* panel to a number greater than the last numbered pin you have; for example, 1000.

3. Choose a row of pins.

4. Choose an origin (the starting pin) where renumbering is to begin.

5. Repeat steps 3 and 4 until all rows have been selected and the pins are renumbered; for example, from 1000 to 1015.

6. Reset the Start Pin Number in the *Options* panel to 1, then repeat steps 3 and 4 until all rows of pins have been selected and the pins renumbered.

7. Click right and choose *Done* from the pop-up menu.

Related Topics

- rpn
- RPN Command: Options Panel

run

Replaces the `system` command in both the old- and new-look interfaces. This change is for compatibility with a Cadence corporate standard for the `system` command. The script convertor changes all instances of `system` to `run`.

Syntax

`run <command_list>`

Example

```
run mv abc.brd ../lib
```