cadence™

Allegro®
Design Synchronization Tutorial

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1

Introduction to the Tutorial

Purpose

The Design Synchronization tutorial describes how to keep schematics and boards in sync using the Design Synchronization toolset. The tutorial focuses on the following set of procedures:

- Annotating the connectivity changes made in the board back to the schematic
- Annotating the property changes made in the board back to the schematic
- Synchronizing the schematics and boards using the Design Synchronization toolset

Audience

This tutorial is designed for first time users of the Design Synchronization toolset. If you are a schematic or board designer, you will often need to synchronize the schematic and the board. This need may arise if you make property or connectivity changes to the schematic or the board after initial packaging. The use of the Design Synchronization toolset helps you to keep the schematic and the board in sync.

Prerequisites

It is assumed that you are familiar with Allegro Design Entry HDL and Allegro PCB Editor. This document will not discuss the details of taking a design from the schematic to the board as it is assumed that you are familiar with these tools.

Note: To learn about Design Entry HDL or PCB Editor, see *Allegro Design Entry HDL User Guide* and *Allegro PCB and Package User Guide: Getting Started with Physical Design* in CDSDoc.

Design Synchronization Toolset

Design Synchronization tools are used to compare schematics and boards and provide categorized output. They also provide the facility to update changes from a board to the schematic and from a schematic to the board.

The Design Synchronization toolset consists of:

- Design Differences
- Design Association
- Packager-XL
- Netrev
- Genfeedformat

The Design Differences and Design Association tools are the focus of this tutorial.

Design Differences - This tool compares a schematic and a board, and presents the differences in connectivity, nets, parts, net properties, pin properties, and component properties. Using the Design Differences tool, you can control updating the schematic or the board. Design Differences is also referred to as Visual Design Differences (VDD).

Design Association - Design Differences saves the connectivity changes between the schematic and the board in a file named `dessync.mkr`. Design Association reads these changes and allows you to update the schematic in a controlled manner.

Packager-XL - Packager-XL is the interface between the logical design (schematic) and the physical layout (board) for the Cadence Board Design Solution. It has two modes of operation:

- In the Forward mode, Packager-XL translates a logical design entered in Design Entry HDL into a physical design ready for layout by PCB Editor.
- In the Feedback mode, Packager-XL receives changes made in PCB Editor and incorporates the property/swapping changes back to the logical design.

Netrev - Netrev loads the Packager output into a database for physical layout, which can be operated on by PCB Editor or Allegro SI.

Genfeedformat - Genfeedformat extracts connectivity and property information from the board into view files that are used by Design Differences and Packager-XL (in the Feedback mode).

Overview

Design Synchronization tools are used to compare a schematic and a board, and synchronize any changes in them. Design synchronization keeps track of all the changes that occur in the board or the schematic after the initial transfer of packaged information to the board.

Four types of changes occur in the board after the initial transfer of packaged information from the schematic. The changes are listed below.

1. Component changes

   Add new components in the design to handle signal integrity and electromagnetic compatibility problems. These components may include termination resistors, series or shunt buffers, and bypass capacitors.

2. Connectivity changes

   Make connectivity changes to facilitate routing after the initial placement of components. Connectivity changes may be caused by pin swaps, section swaps, and reference designator (refdes) swaps.

3. Reference designator changes

   Change reference designators to debug board problems.

4. Property changes

   Modify components in the board. These modifications cause property changes.

Besides the changes in the board after the initial transfer of packaged information from the schematic, certain changes, such as Engineering Change Order (ECO), are also made in the schematic. The need for the Design Synchronization toolset arises from the need to synchronize these differences between the schematic and the board.

This tutorial covers the Design Differences and Design Association tools. You will use these tools to synchronize a given schematic and board, which are part of the database available with the tutorial.

Note: For more information about different Design Synchronization tools and how they fit in the Front-to-back flow for PCB system design, see the Cadence document *Design Synchronization and Packaging User Guide* in CDNShelp.

The tutorial consists of eight chapters. Each chapter deals with a particular type of difference between the board and the schematic. The names of the chapters are:

- Chapter 2, “Handling Swaps”

- Chapter 3, “Handling Section Swaps”
- Chapter 4, “Handling Section Swaps Between Components”
- Chapter 5, “Synchronizing Net Properties Differences”
- Chapter 6, “Synchronizing Component Properties Differences”
- Chapter 7, “Synchronizing Pin Properties Differences”
- Chapter 8, “Handling Bypass Capacitors”
- Chapter 9, “Handling Series Terminators”

Tutorial Structure

This section explains the installation and structure of the tutorial. Each chapter includes additional information about specific features of the tools. After completing this tutorial, you will be able to use the tools fluently in their design process.

Installing the tutorial

Unzip the *des_demos.zip* file located in the <*your_inst_dir*>/doc/dessync_tut/tutorial_examples, and extract it to an empty directory, say des_demos. On extracting the des_demos.zip file, you will find eight sub-directories under the des_demos directory. Each of these sub-directories has a design relevant to each section of the tutorial.

Structure of the Demo Database

The des_demos database consists of eight directories, each of which contains a design with all the required views. The directory contains one schematic and one or more boards. The project directory is hdli for all the sections. The design directory is called fx, while the project file is atm.cpm.

In brief, the steps you will perform in the following chapters are as follows:

1. Launch Project Manager and load atm.cpm. The names of the directories from which you must load atm.cpm are listed in the following chapters.
2. Open the schematic file in Design Entry HDL.
3. Open the board file sync.brd using PCB Editor. There are other boards present, which are not in sync with the schematic.

4. Use Design Differences to verify that the schematic and the `sync.brd` file are in sync.
5. Use Design Differences to view the differences between the board and the schematic.
6. Update the Design Entry HDL schematic.
7. Run `backannotate` in Design Entry HDL and view the changes.

   Note: You can also directly backannotate the schematic from Export Physical and Import Physical.
8. Save and package the schematic.
9. Use Design Differences to ensure that the new schematic and difference board are in sync.

In each directory, you must delete the files and folders in the `fx` directory, and copy the files and folders in `fx.orig` to the `fx` directory to reuse the tutorial database.

You must ensure that the `OVERWRITE_CONSTRAINTS` directive in the `START_PKGRXL` section of each `atm.cpm` file in each directory is set to ON

2

Handling Swaps

Objective

To become familiar with Design Differences and understand how pin swap information is displayed in Design Differences

At the end of this chapter, you will be able to:

- Launch Design Differences from Design Entry HDL.
- Use Design Differences to view the differences caused by pin swaps in the board.
- Synchronize the schematic with the pin swaps made in the board.

Starting SPB Tools

To understand the working of Design Differences, you need know about Allegro Project Manager, Design Entry HDL, and PCB Editor. All these tools are SPB tools.These tools call Design Differences to identify differences between the schematic and the board.

Task Overview

You will open the `atm.cpm` file in the `des_demos/pinswap/hdli` directory in Project Manager, and view the schematic in Design Entry HDL and the board in PCB Editor.

Steps

1. Launch Project Manager:
   - On Windows NT, choose *Start – Cadence PCB 2023 – Project Manager 2023*.
2. Choose *Allegro Design Authoring* and click *OK*.

3. In Project Manager, choose *File – Open*.

   The Open Project window appears.

4. Navigate to the `des_demos/pinswap/hdli` directory and load the `atm.cpm` file.

   The Project Manager title bar displays the name of the opened project, `atm.cpm`.

5. Click *Design Entry* to open the schematic in Design Entry HDL.

   Design Entry HDL opens the `atm.cpm` project and displays the schematic.

6. Click *Layout* in Project Manager to launch PCB Editor.

   PCB Editor opens the `atm.cpm` project and displays the board.

   You may get a license error when you click *Layout* in Project Manager. If you do, click *OK* in the message box. The *Cadence 23.1 Allegro Product Choices* dialog appears. Select *Allegro PCB Designer* and click *OK*. The board is displayed.

Starting Design Differences

Task Overview

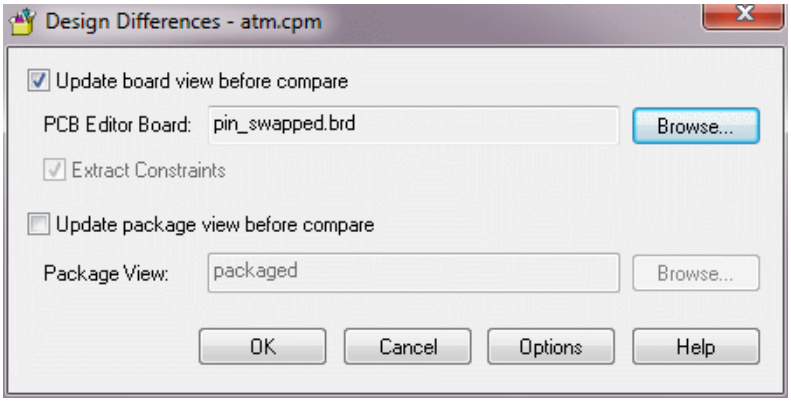
Start Design Differences from Design Entry HDL, and load the `sync.brd` board file. This enables you to view the differences between the schematic and the board.

Steps

1. Choose *Tools – Design Differences* in Design Entry HDL to start Design Differences.

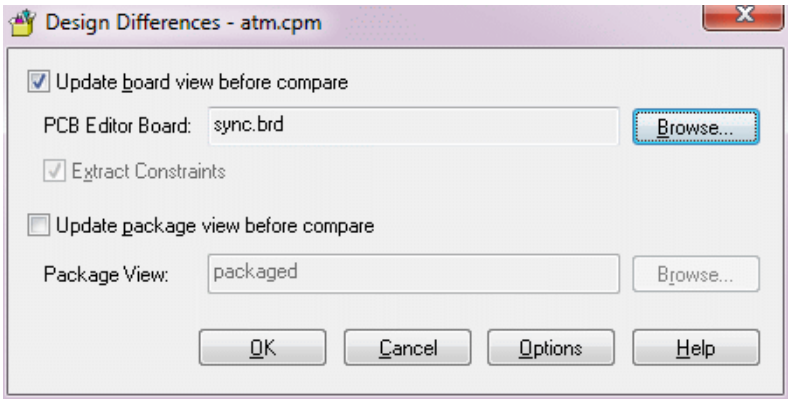
   The Design Differences dialog appears with the title Design Differences - atm.cpm.

Figure 2-1 Design Differences Dialog



2. Ensure that the *Update board view before compare* is selected. This option is selected to enable the Browse button.
3. Click *Browse*.

   The Select Board File dialog box opens.
4. Select `sync.brd`.



5. Clear the *Update package view before compare* check box.

   When the *Update board view before compare* check box is selected, Design Differences compares the packager feedback files (generated by running `genfeedformat` on the board) with the packager files and generates feedback files for the selected board. If this check box is not selected, Design Differences uses the view files already present to compare differences.

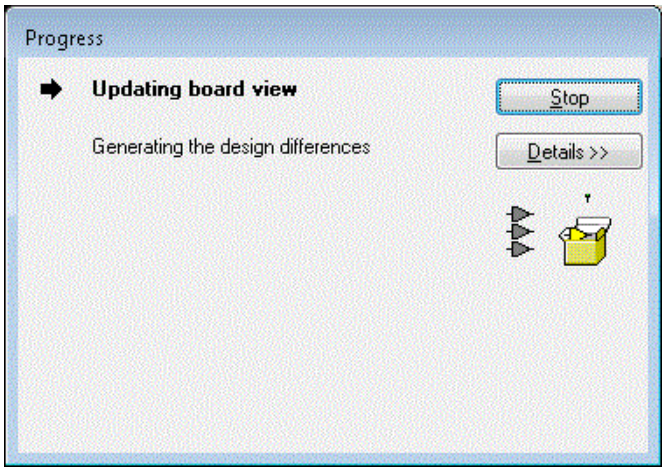
   Similarly, if you select the *Update package view before compare* check box, Design Differences packages the saved schematic (by calling Export Physical).

The *Options* button brings up the packaging options form. Do not select this option because the schematic has not changed after it was packaged initially.

6. Click *OK* in the Design Differences dialog.

   The Progress Window appears.

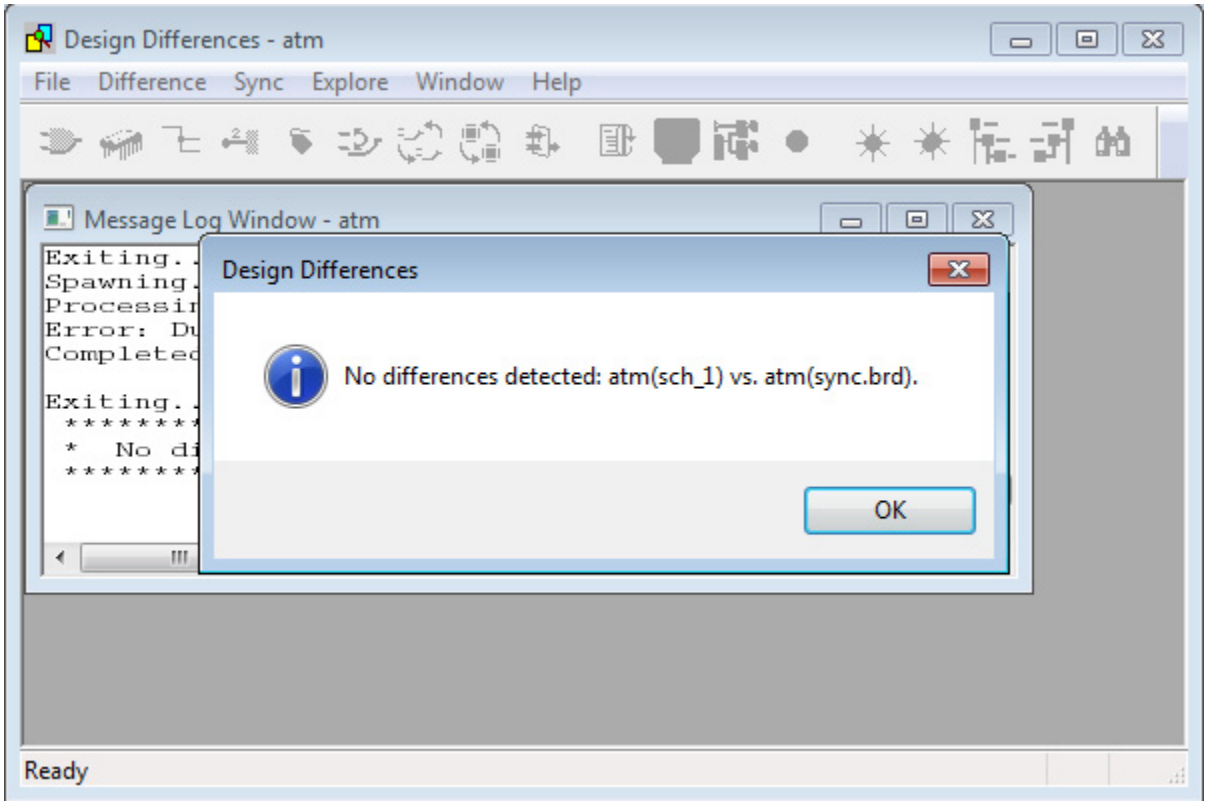
Figure 2-2 Progress Window



The progress window disappears as soon as the views are updated.

The message log and a message box with the information that there are no design differences between the schematic and the board are displayed.

Figure 2-3 Design Differences Window



7. Click *OK* in the Design Differences message box.

Viewing Pin Swap Design Differences

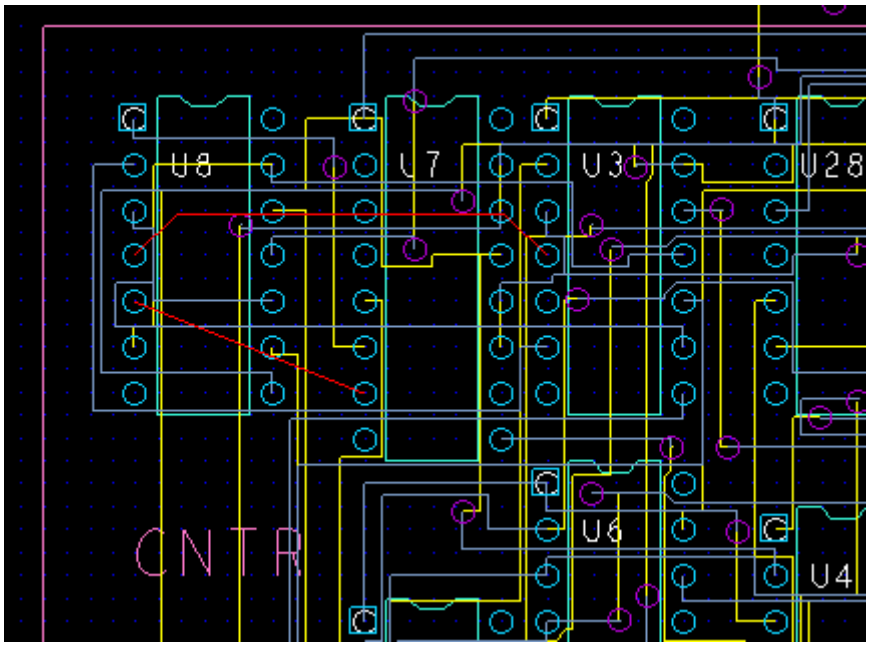
Task Overview

You have so far verified that the schematic is in sync with the `sync.brd` board file. You now compare the schematic with a board, in which a pin swap has occurred, by using Design Differences. First, you will view the differences manually, then you will see how the differences show up in the Design Differences window.

Steps

1. Choose *File – Open* in PCB Editor and load the `pin_swapped.brd` board file.

Note the two flight lines (rat's nest lines) in red. One line connects the pins `U7.7` and `U8.5`, and the other line connects pins `U3.4` and `U8.4`.



2. Choose *File – Edit Hierarchy – Descend* in the Design Entry HDL window.

Descend into the `CNTR10` block in the top-level schematic by clicking the *Descend* button on the toolbar. Locate the OR gates in `U8` in the lower left corner of the schematic.

Use the command `find u8` in the Design Entry HDL console window to find U8 and use `next` to get to the right pins. Note that `U8.4` is connected to `U7.7`, and `U8.5` is connected to `U3.4`.

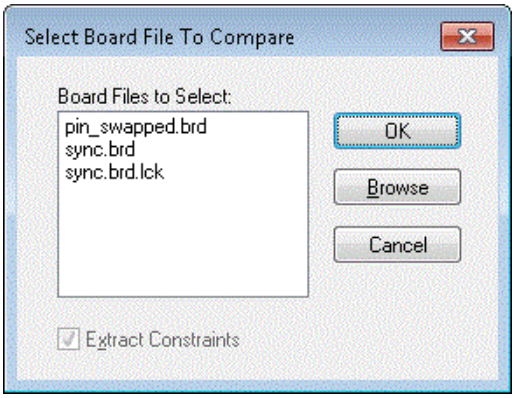
SCHEMATIC	BOARD
U3.4 -U8.5	U3.4 - U8.4
U7.7 - U8.4	U7.7- U8.5

You will next view the same information in the Design Differences window.

3. Choose *File – Load PCB Editor Board* in the Design Differences window.

   The Select Board File To Compare dialog box appears.

Figure 2-4 Select Board File To Compare Dialog Box



4. Select the `pin_swapped.brd` file from the *Board Files to Select* list and click *OK*.

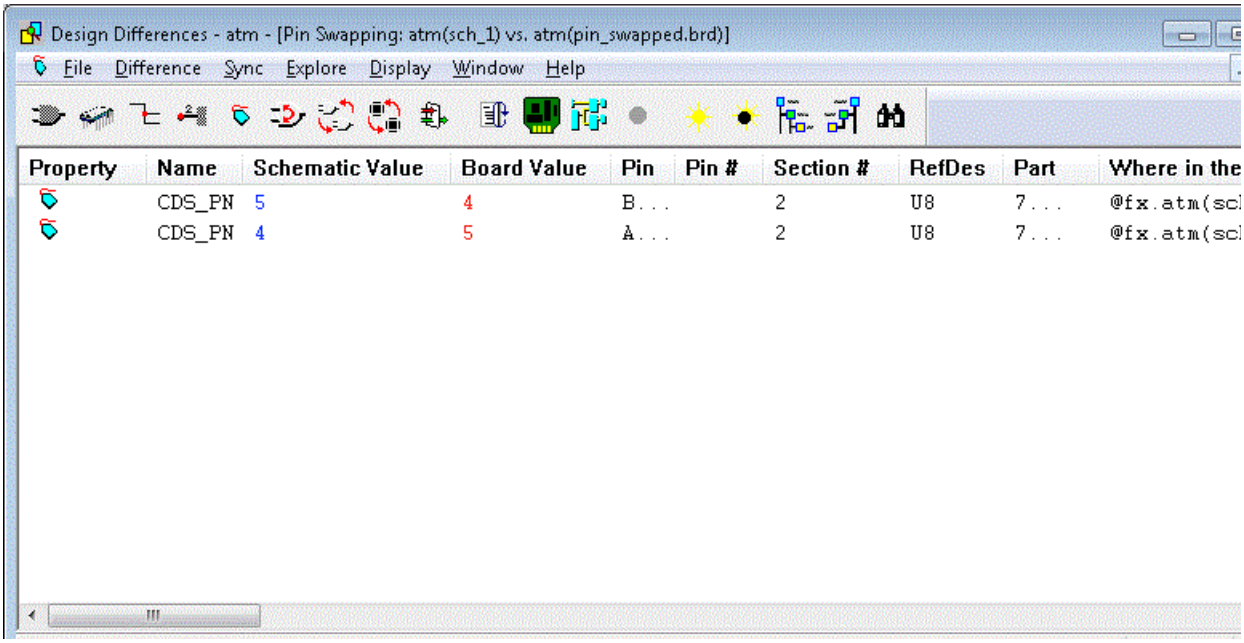
   Design Differences loads the board and displays a message box with a successful completion status.

5. Click *OK* to proceed.

   The Message Log Window and the Pin Swapping window appear.

   If the Pin Swapping window is not in front, choose *Difference – Pin Swapping* to bring it to the front.

Figure 2-5 Pin Swapping Window



The Pin Swapping differences window shows the differences in the `CDS_PN` property, which has the physical pin number information. The first line indicates that the `Refdes U8`, part `74F32-BASE`, section 2, schematic instance pin `b<0>` is mapped to pin number `5` in the schematic, but maps to the pin number `4` on the board.

Synchronizing the Schematic and the Board With Pin Swap Changes

Task Overview

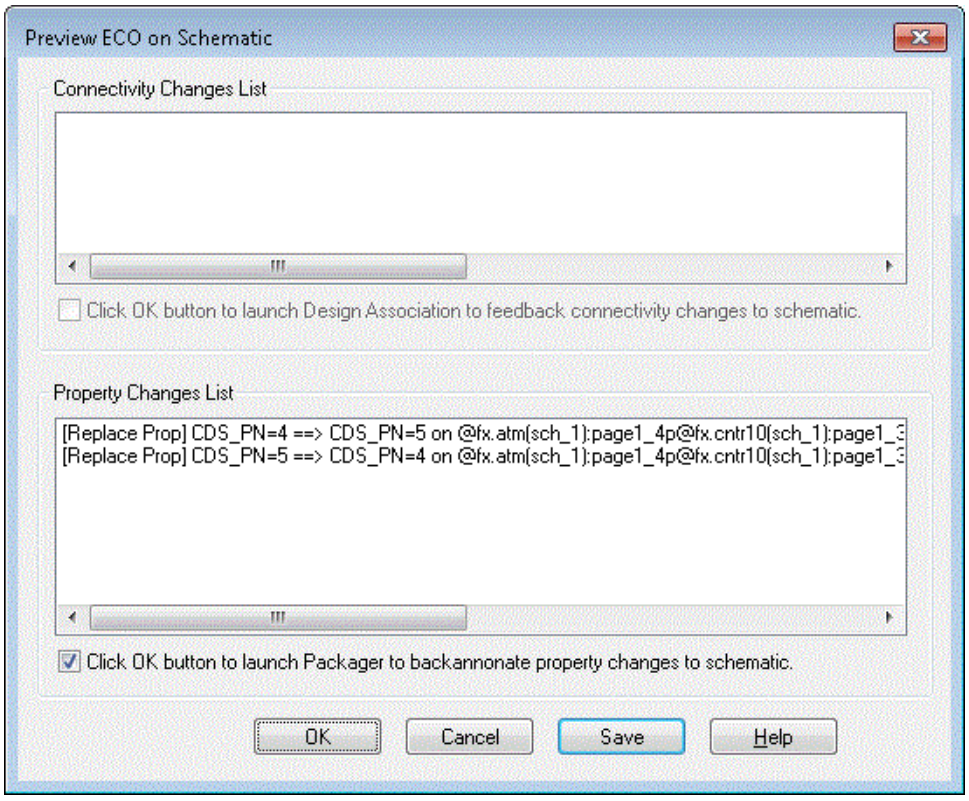
Update the schematic with the difference information and verify that the schematic is in sync with the `pin_swapped.brd` board.

Steps

1. Choose *Sync – Update Design Entry HDL Schematic* from the Design Differences window.

   The Preview ECO on Schematic dialog appears.

Figure 2-6 Preview ECO on Schematic Dialog



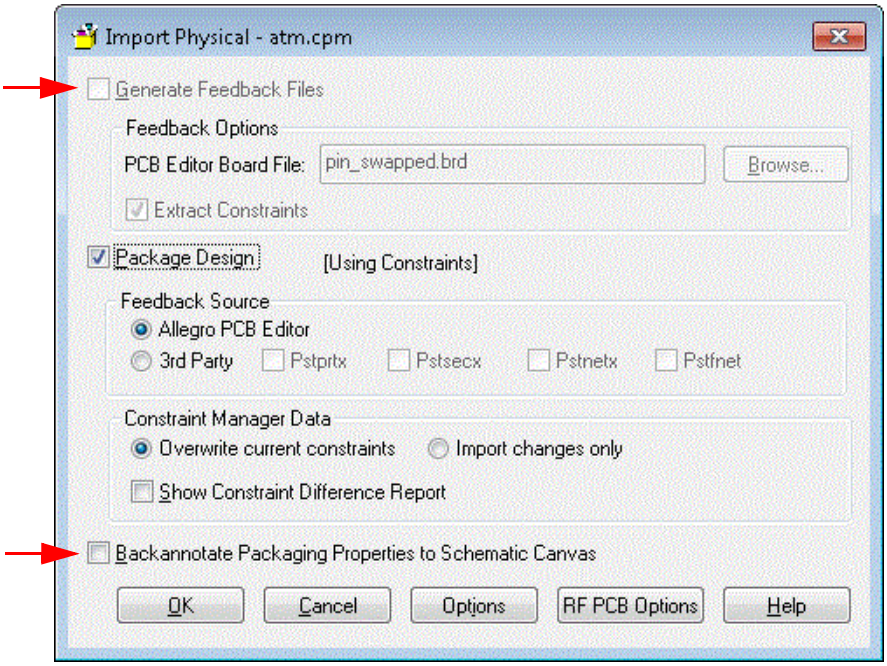
This dialog summarizes the changes needed in the schematic to bring it in sync with the board.

You will now Launch Packager-XL in the feedback mode to update the pin swap information back to the packager files. Look at the changes in the *Property Changes List*. These changes will be carried out by Packager-XL when it runs in the Feedback mode.

2. Click *OK* to update the schematic.

   The message log in the Design Differences window is updated and the Import Physical dialog appears.

Figure 2-7 Import Physical dialog: For Design Differences



Note that you are not allowed to generate the feedback files.

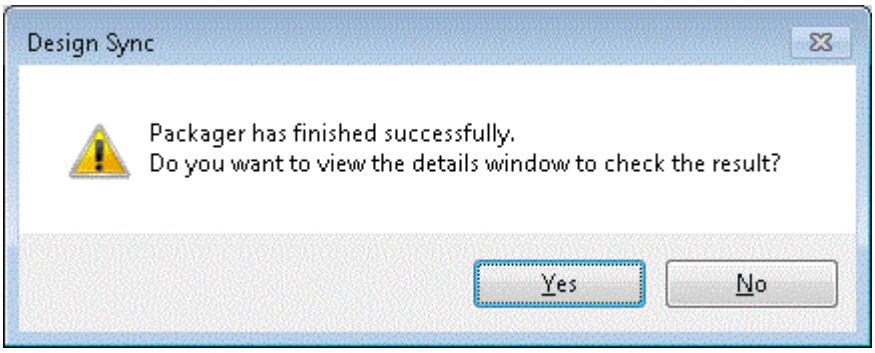
3. Leave the *Overwrite current constraints* radio button selected.

   There is an option to backannotate the schematic. If you select the backannotate option, you will not be able to see the differences between the schematic and the board. For the purpose of this tutorial, do not select the *Backannotate Packaging Properties to Schematic Canvas* check box.

4. Click *OK*.

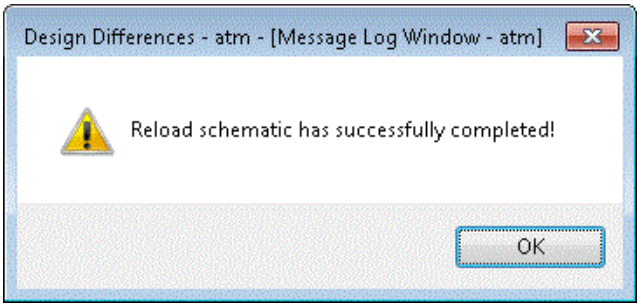
   A Progress dialog box appears with the information that the design is netlisted and being fed back. A message box prompts you to see the Packager results.

Figure 2-8 Design Sync Message Box



5. Click *No*.

   A message box displays information that the reload was successfully completed.

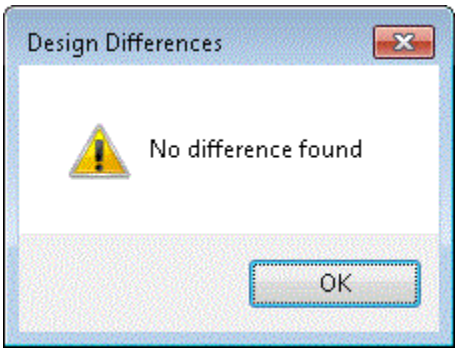


   Click *OK*.

   The message log and the Constraints Differences (Physical and Logical) windows are displayed in the Design Differences window. Close the Constraints Differences windows.

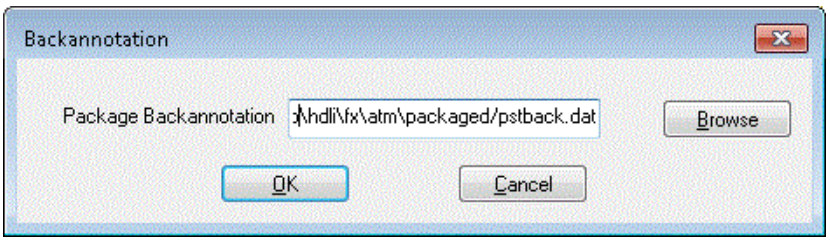
6. To view whether there are any design differences, click the *Pin Swap* button on the toolbar or use *Difference – Pin Swapping*.

A message box appears confirming that there are no differences.



7. Choose *Tools – Back Annotate* in the Design Entry HDL window to update the Design Entry HDL schematic with the changes in the packager files using the `pstback.dat` file.

Figure 2-9 Backannotation Dialog Box



Note that the `pstback.dat` file is selected for backannotation.

8. Click *OK*.

Design Entry HDL schematic is updated with the latest property information from the board.

Locate the `U8` component in Design Entry HDL and see its pin configuration. You will find that the pins are swapped. The new pin connection for the `U8` component is the same as in the PCB Editor board.

SCHEMATIC	BOARD
U3.4 -U8.4	U3.4 - U8.4
U7.7 - U8.5	U7.7- U8.5

9. Choose *File - Exit* in Design Differences, PCB Editor, Design Entry HDL, and Project Manager. If prompted, do not save any changes.

3

Handling Section Swaps

Objective

To view section swap information in Design Differences and to update the schematic with the swap information.

At the end of this chapter, you will be able to,

- open Design Differences from Project Manager.
- use Design Differences to view the differences caused by section swaps in the board.
- synchronize the schematic with the section swaps made in the board.

Launching Design Differences from Project Manager

Task Overview

You will open the `atm.cpm` file in the `des_demos/section_swap/hdli` directory in Project Manager, and view the schematic in Design Entry HDL and the board in PCB Editor.

Steps

1. Launch Project Manager.
2. Choose *Allegro Design Authoring* and click *OK*.
3. Load the `atm.cpm` file located in the `des_demos/section_swap/hdli` directory.

   The Project Manager title bar displays the name of the opened project, `atm.cpm`.
4. Click *Design Entry* to open the schematic in Design Entry HDL.

   Design Entry HDL opens the `atm.cpm` project and displays the schematic.

5. Click *Design Sync* in Project Manager, and select *Design Differences*.

   The Design Differences dialog appears.

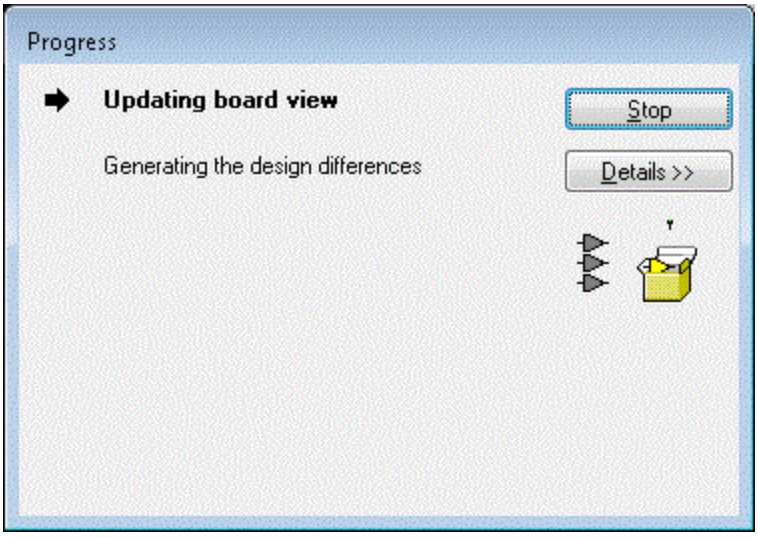
6. Select the *Update board view before compare* check box if it is not selected.

7. Click *Browse*, and select the `sync.brd` file. Ensure that the *Update package view before compare* check box is not selected.

8. Click *OK* to launch Design Differences.

   The Progress window appears. You can click *Details* in this window to see the progress log.

Figure 3-1 Progress Window



   The Progress window disappears after the views are updated. The message log and a message box with the information that there are no design differences between the schematic and the board are displayed.

9. Click *OK* to close the message box.

Viewing Section Swap Differences in Design Differences

Task Overview

Load the `section_swapped.brd` board file in Design Differences to view the section swap differences between the schematic and the board.

Steps

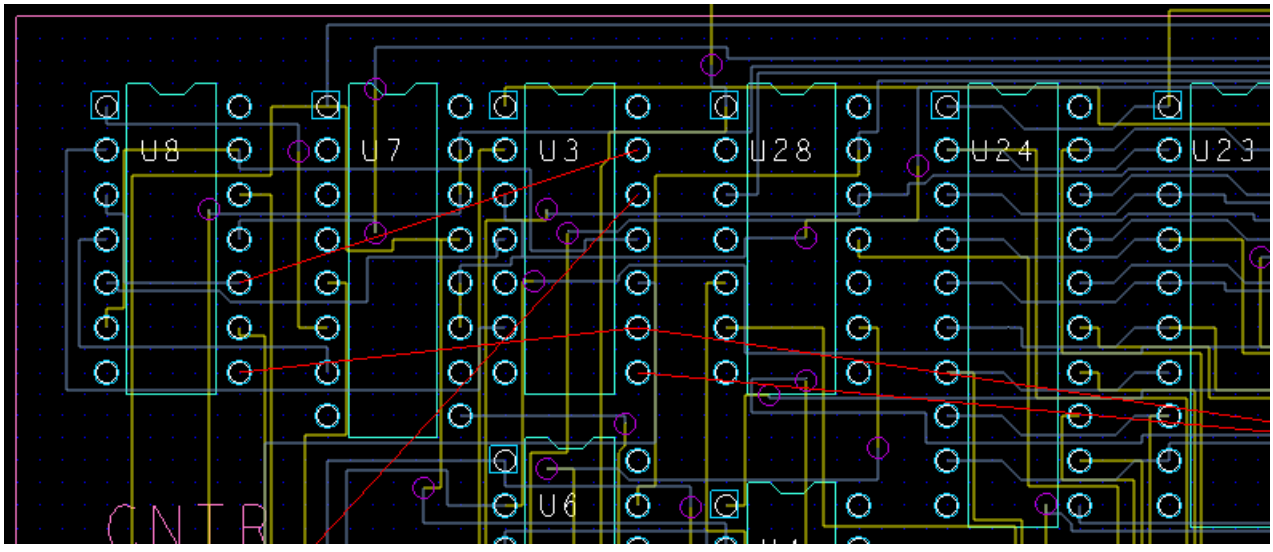
1. Click *Layout* in Project Manager to launch PCB Editor.

   PCB Editor opens the `atm.cpm` project and displays the board.

   You may get a license error when you click *Layout* in Project Manager. If you do, click *OK* in the message box. The *Cadence 23.1 Allegro Product Choices* dialog appears. Select *Allegro PCB Designer* and click *OK*. The board is displayed

2. Choose *File – Open* and load the `section_swapped.brd` board file.

   Note the two red flight lines (rat's nest lines), which show the section swap.



3. Choose *File – Load PCB Editor Board* in Design Differences window.

   The Select Board File To Compare dialog box appears.

4. Select `section_swapped.brd` from the *Board Files to Select* list and then click *OK*.

Design Differences loads the board and displays a message box with a successful completion status.

5. Click *OK* to proceed.

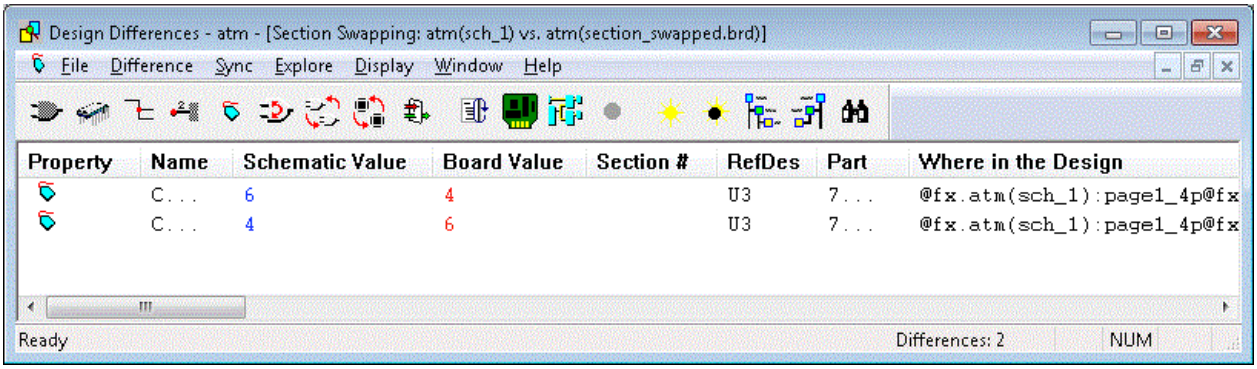
   The Message Log and Section Swapping windows appear.

6. Scroll up to the top of the message log window.

   View the messages that appear. Note that the date and time of loading are mentioned at the top.

7. Press `Ctrl-F6` to bring the Section Swapping window to front.

Figure 3-2 Section Swapping window



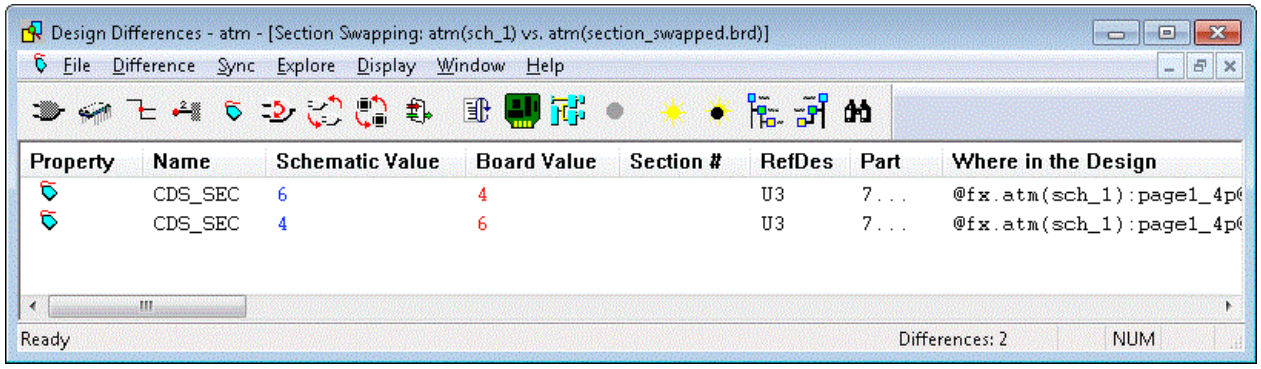
The title reads *Section Swapping: atm(sch_1) vs. atm(section_swapped.brd)*. This window displays the top-level schematic and the name of the board being compared.

The *Name* column represents the name of the property that is different between the board and the schematic. Note that the name is incomplete and is represented by C.

8. Expand the *Name* column by hovering the cursor over the divider line between the *Name* and *Schematic Value* columns. The cursor shape changes. Click the line and drag the mouse to extend the column to the required size.

   The enlarged window with the expanded *Name* column is shown below.

Figure 3-3 Section Swapping Window: Fields Adjusted



Note that the property name is `CDS_SEC`. You can adjust the size of any field in the Design Differences window. Also note that section `4` on `U3` has been swapped with section `6` on the same IC.

Viewing Simultaneous Section and Pin Swap Changes in the Board

Task Overview

Load the `section_swapped2.brd` board file in Design Differences to view the section swap and pin swap differences between the schematic and the board.

Steps

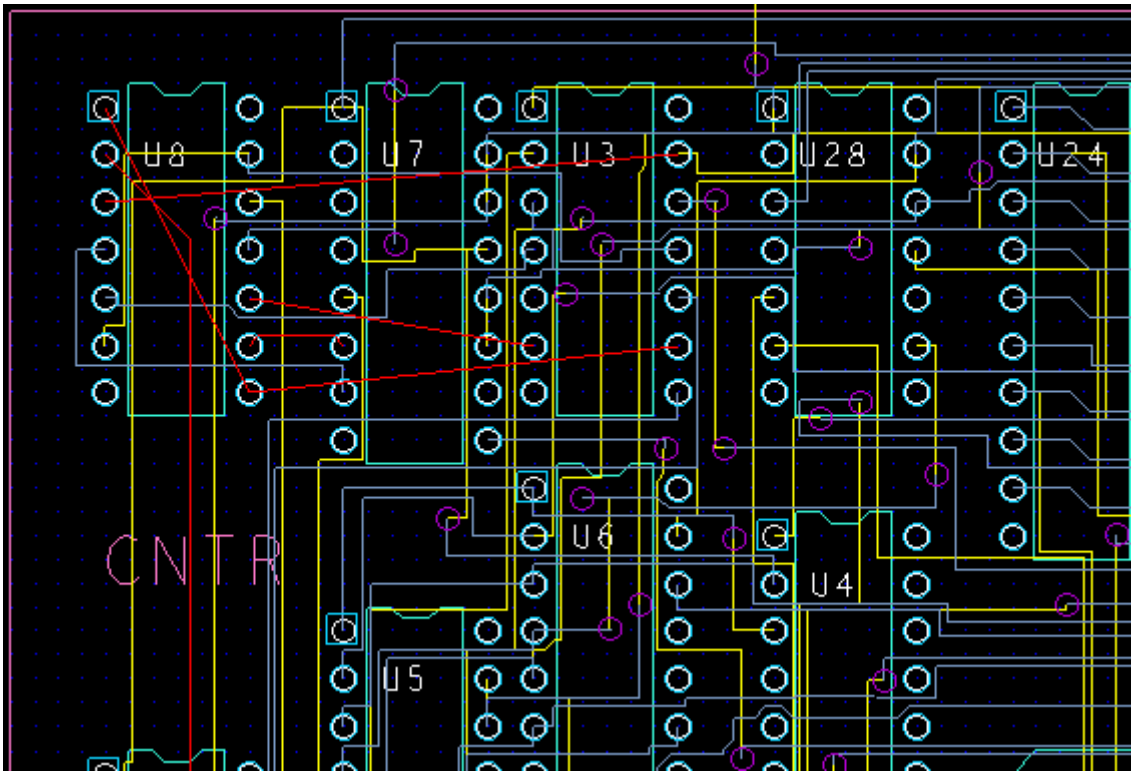
1. Choose *File – Open* in the PCB Editor window.

   If you are prompted to save the `section_swapped.brd` file, click *No*.

2. Load the `section_swapped2.brd` board, which is created by swapping section `1` with section `3` on `U8` on `sync.brd`.

   Note: The highlighted nets are connected between `U8.1` and `U9.6` and between `U8.2`

and `U8.8`.



3. Choose *File – Load PCB Editor Board* in Design Differences window and then select the `section_swapped2.brd` board file in the Select Board File to Compare dialog box.

   A message box reports the successful loading of the board file.

4. Click *OK* to proceed.

   You see some messages scrolling in the message log window within Design Differences. The Message Log Window, the Section Swapping window, and the Pin Swapping window appear.

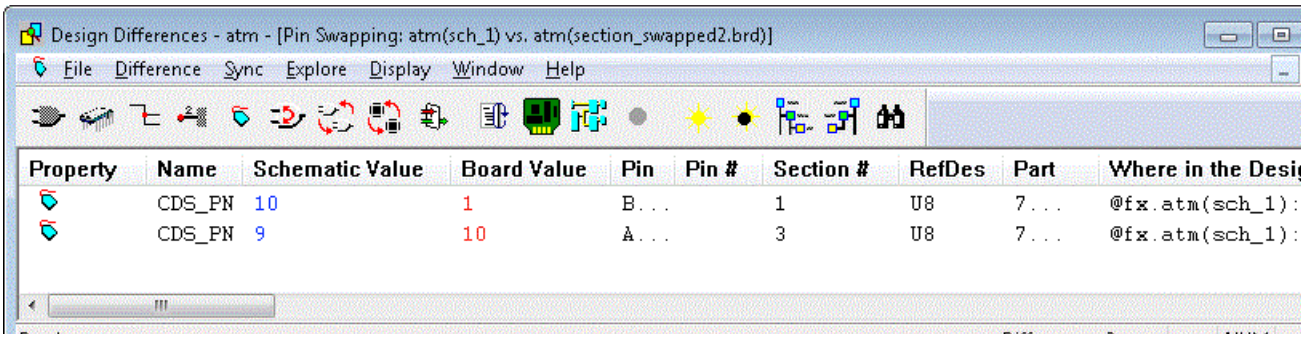
   Note: You can import swapped pin information for ‘size-able’ components that have the “HAS_FIXED_SIZE” property back to Design Entry HDL by setting the following directive in the atm.cpm file:

   ```
   START_PKGRX

   IMPORT_HFS_HARDSEC_ON_SWAP_PINS 'ON'

   END_PKGRXL
   ```

You can set this directive only if you are performing pin swaps in Allegro for ‘size-able’ components that have the `HAS_FIXED_SIZE` property. These components in Design Entry HDL need special handling as they have the `SECTION` property present on pins along with the `PN` property.

5. Choose *Window – Horizontal Tile* in Design Differences window. This helps in viewing the section swap and pin swap information simultaneously. The Pin Swapping window is displayed below.

Figure 3-4 Pin Swapping Window



Note that pin `10` on the schematic is connected to pin `1` on the board, and pin `9` on the schematic is connected to pin `10` on the board.

Synchronizing the Schematic and the Board With Section Swap Changes

Task Overview

You will now update the schematic and ensure that the schematic and board are in sync after the update.

Steps

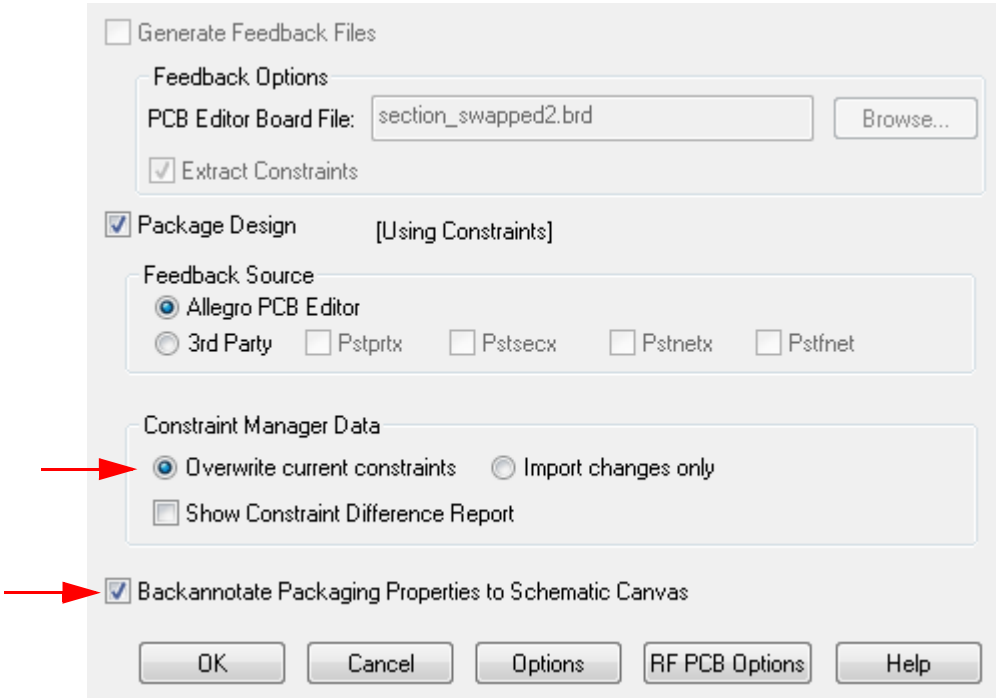
1. Choose *Sync – Update Design Entry HDL Schematic* from the Design Differences window.

   The *Preview ECO on Schematic* dialog appears. The *Property Changes List* displays section swaps and pin swaps. Note that the *Click OK button to launch Packager to backannotate property changes to schematic* check box is selected.

2. Click *OK* to update the schematic**.**

   The message log in the Design Differences window is updated and the Import Physical dialog appears.

3. Leave the *Overwrite current constraints* radio button and the *Backannotate Packaging Properties to Schematic Canvas* check box selected, and then click *OK*.



A Progress dialog box appears with the information that the design is netlisted and being fed back. Finally, a message box appears that the import is successful and prompts you to review the details and see the Packager results.

4. Click *No*.

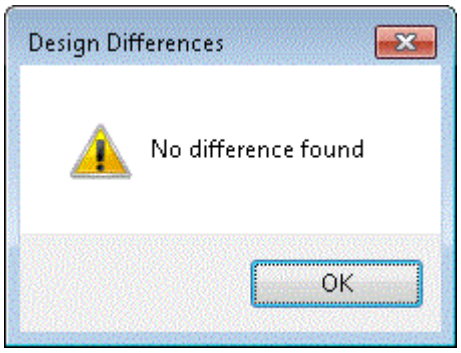
   In the Design Differences window, a message box appears with the information that the schematic is successfully loaded.

5. Click OK.

   Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Design Entry HDL schematic.

6. To view whether there are any differences between the schematic and the `section_swapped2.brd` board file, click the *Section Swap* button on the toolbar or use *Difference – Section Swapping*.

A message box appears confirming that there are no differences.



7. Click *OK* to close the message box.
8. Choose *File – Exit* in Design Differences, PCB Editor, Design Entry, and Project Manager. Do not save any changes.

4

Handling Section Swaps Between Components

Objective

To view section swaps between components in Design Differences and update the schematic to reflect the swap

At the end of this chapter, you will be able to,

- open Design Differences from the command line.
- use Design Differences to view the differences caused by section swaps between components in the board.
- synchronize the schematic with the section swaps between components made in the board.
- cross-probe differences between the schematic and Design Differences.

Setting Up and Launching Design Differences

Task Overview

You will open the `atm.cpm` file in the `des_demos/component_swap/hdli` directory in Project Manager, and view the schematic in Design Entry HDL and the board in PCB Editor.

Steps

1. Launch Project Manager.
2. Choose *Allegro Design Authoring* and click *OK*.
3. Load the `atm.cpm` file located in the `des_demos/component_swap/hdli` directory.
4. Click *Design Entry* to open the schematic in Design Entry HDL.

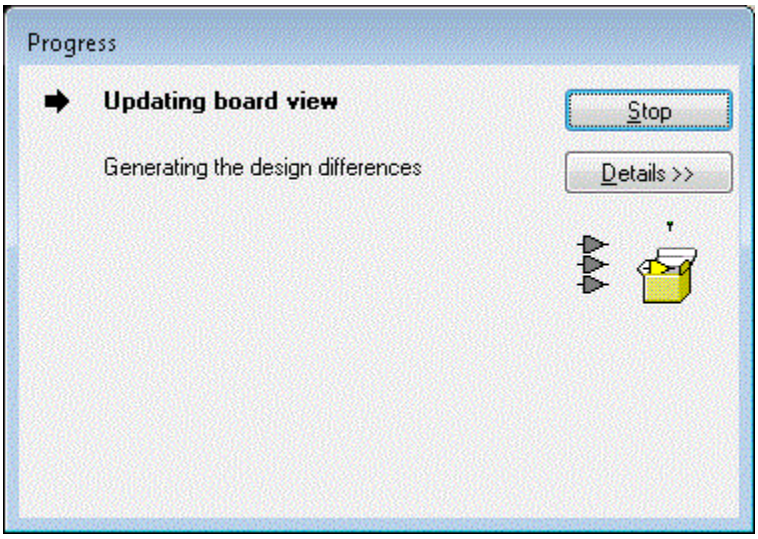
   Design Entry HDL opens the `atm.cpm` project and displays the schematic.
5. Choose *Tools – Design Differences* in the Design Entry HDL window to launch Design Differences.

   The Design Differences dialog appears. Note that the *Update board view before compare* check box is selected.

   To launch Design Differences directly from the command-line prompt, type `vdd&`.
6. Click *Browse* and select the `sync.brd` file in the Select Board File dialog box.
7. Ensure that the *Update package view before compare* check box is not selected.
8. Click *OK* to launch Design Differences.

   The Progress window appears. You can click *Details* in this window to see the progress log.

Figure 4-1 Progress Window



The Progress window disappears as soon as the views are updated. The message log and a message box with the information that there are no design differences between the schematic and the board are displayed. Click *OK* in the message box.

Viewing Differences Caused by Section Swap Between Components

Task Overview

You have verified that the schematic is in sync with the `sync.brd` board. You can now compare the schematic with a board in which a section swap has occurred between two components using Design Differences. The `section_swapped_u3-u10.brd` board in the `physical` directory under the `atm` design includes a section swap between the `U3` and `U10` components.

First, you will view the differences manually in PCB Editor, and then verify the differences in Design Differences.

Steps

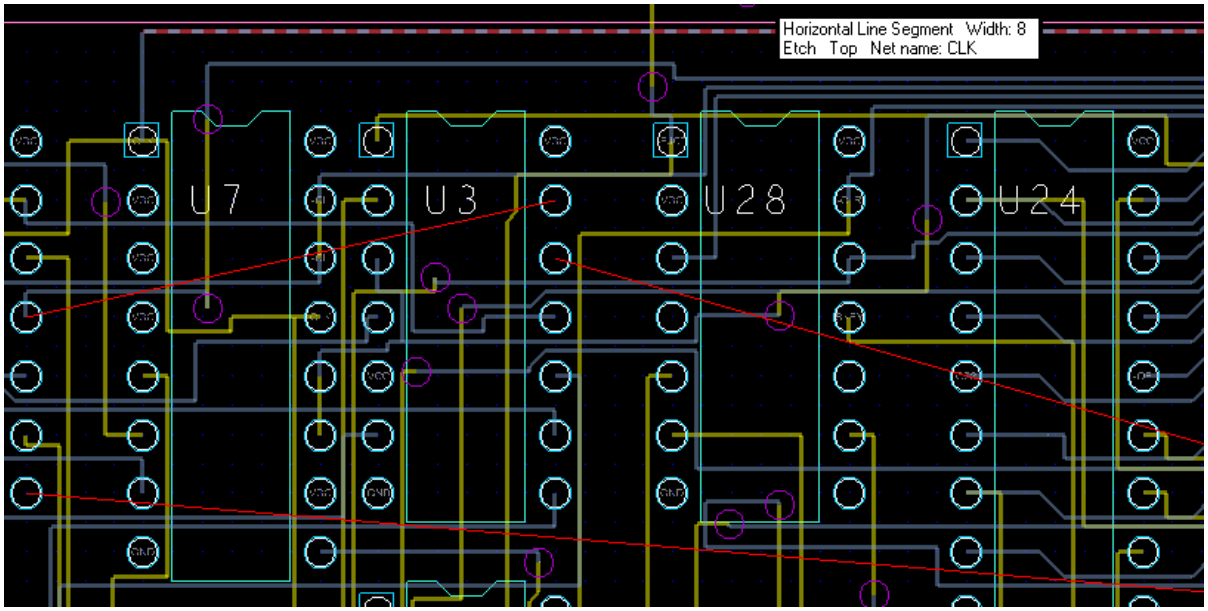
1. Click *Layout* in Project Manager to launch PCB Editor.

   PCB Editor opens the `atm.cpm` project and displays the board.

   You may get a license error when you click *Layout* in Project Manager. If you do, click *OK* in the message box. The Cadence 23.1 Allegro Product Choices dialog appears. Select *Allegro PCB Designer* and click *OK*. The board is displayed

2. Choose *File – Open* in PCB Editor, and load the `section_swapped_u3-u10.brd` board file.

Note the red flight lines (rat's nest lines), which show the section swap.



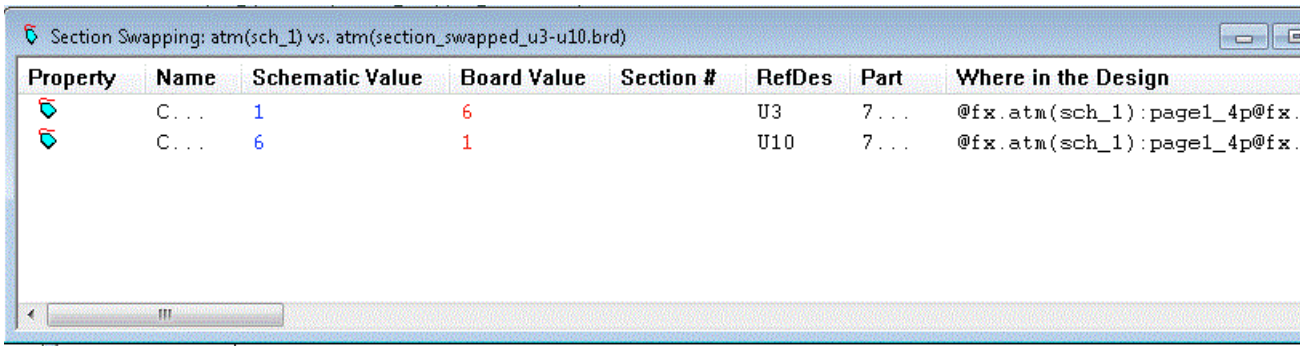
3. Choose *File – Load PCB Editor Board* in Design Differences.
4. Select `section_swapped_u3-u10.brd` in the Select Board File to Compare dialog box.
5. Click *OK*.

   A message box reports the successful reloading of the board file.
6. Click *OK* to proceed.

   The Message Log Window, RefDes Difference and Section Swapping windows appear.

   The Section Swapping window displays the `CDS_SEC` property in the schematic and the board is swapped. As a result, the `RefDes U3` has the value `1` in the schematic and `6` in the board while `RefDes U10` has the value `6` in the schematic and `1` in the board.

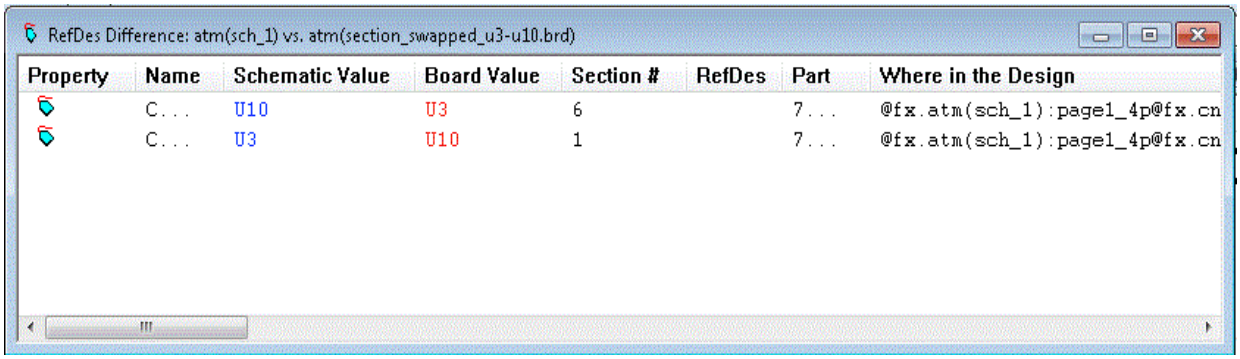
Figure 4-2 Section Swapping Window



7. Press `Ctrl-F6` to bring the RefDes Difference window to front.

   The RefDes Difference window becomes active. Note that the `CDS_LOCATION` property in the schematic and the board are swapped. Section `1` of `U10` has moved to `U3` and section `6` of `U3` has moved to `U10`.

Figure 4-3 RefDes Difference Window



Cross-Probing Between the Schematic and Design Differences

Task Overview

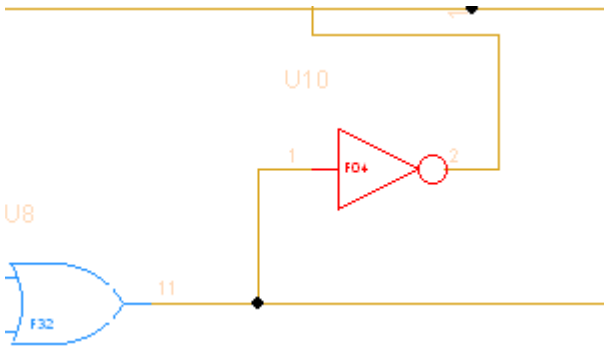
You will now cross-probe the difference between the schematics and Design Differences. This helps you understand what happens in the schematic after the differences are synchronized.

Steps

1. Move the Design Entry HDL and Design Differences windows so that both are simultaneously visible.
2. Bring the Refdes Difference window in Design Differences to the front, and select the first line with the schematic value `U10`.
3. Choose *Display – Highlight Source* in Design Differences to highlight an instance in the schematic.

   This highlights `U10` in Design Entry HDL as shown in the figure below.

Figure 4-4 Source highlighted in Design Entry HDL



4. Choose *Display – Dehighlight Source* in Design Differences to dehighlight the highlighted instance.

   The highlight from section `6` of `U10` is removed in Design Entry HDL.
5. Bring the Section Swapping window to the front in Design Differences and then select the first line, that is,
   `CDS_SEC 1`.
6. Click the *Highlight* button ( ) to highlight the selection in Design Entry HDL.
7. Right-click the line reading `CDS_SEC 1` and select *Dehighlight Source* to remove the highlight in Design Entry HDL.

   Note: Select a row in any Design Differences window and double-click it. This causes the selection corresponding to the difference to be highlighted in Design Entry HDL.

Updating the Schematic with the Changes in the Board

Task Overview

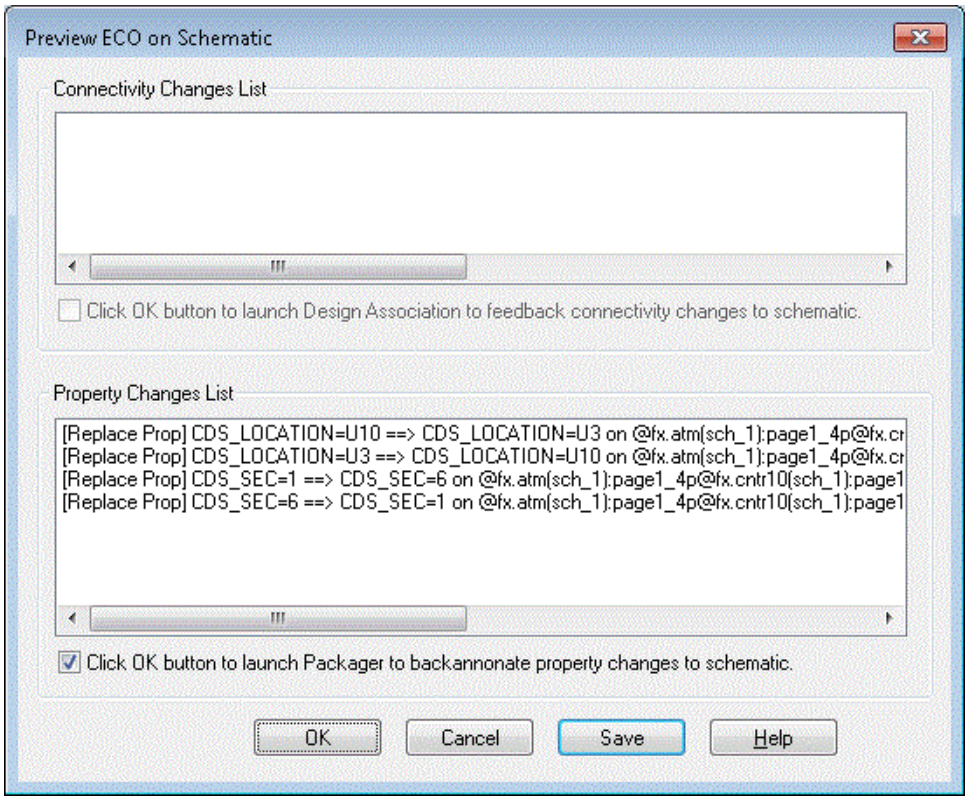
You will now update the schematic and ensure that the schematic and board are in sync after the update. Update the schematic by using the `Backannotate` command in Design Entry HDL.

Steps

1. Choose *Sync – Update Design Entry HDL Schematic* in Design Differences.

   The Preview ECO on Schematic dialog appears. The *Property Changes List* displays the list of changes in properties.

Figure 4-5 Preview ECO on Schematic Dialog



2. Click *OK* to update the schematic.

The message log in the Design Differences window is updated and the Import Physical dialog is displayed.

3. Click *OK* in the Import Physical dialog.

   A Progress window appears with the information that the design is netlisted and being fed back. Finally, a message box appears prompting you to review the details and see the Packager results.

4. Click *No*.

   In the Design Differences window, a message is displayed that the schematic has successfully loaded.

5. Click *OK*.

   Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Design Entry HDL schematic.

6. Choose *Tools – Backannotate* in the Design Entry HDL window to update the Design Entry HDL schematic with the changes in the packager files using the `pstback.dat` file.

   Note that the `pstback.dat` file is selected for backannotation.

7. Click *OK*.

   Design Entry HDL schematic is updated with the latest property information from the board.

   The design differences are updated in Design Entry HDL. Confirm these changes, if prompted.

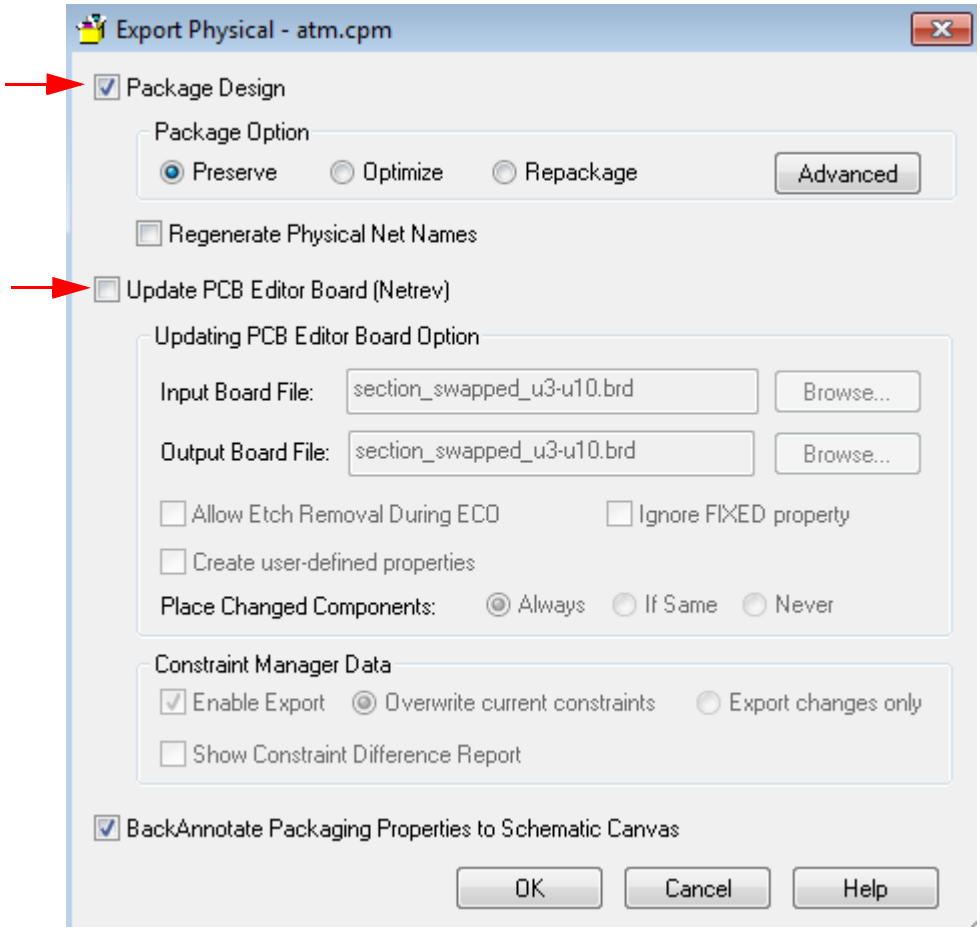
   However, a better way to find whether design differences exist between the schematic and the board is to use Design Differences. Since the schematic has changed, you need to repackage it before you use Design Differences.

8. Choose *File – Export Physical* from Design Entry HDL to repackage the schematic.

   The Export Physical dialog appears.

9. Select the *Package Design* check box.

10. Clear the *Update PCB Editor Board(Netrev)* check box.



11. Click *OK*.

The design is packaged and a message box appears prompting you to review the log files.

12. Click *No*.

13. Choose *File – Update Differences* in Design Differences.

A message log and the Constraints Differences Physical and Logical windows appear.

14. Choose *Difference – Section Swapping* to check if there are any differences between the schematic and the sync.brd board file.

A message box appears confirming that there are no differences.

Click *OK* to close the message box.

15. Choose *File – Exit* in Design Differences, PCB Editor, Project Manager, and Design Entry HDL. Do not save any changes.

5

Synchronizing Net Properties Differences

Objective

To view net property differences in Design Differences and update the schematic with the differences

At the end of this chapter, you will be able to,

- use Design Differences to view the differences caused by changes in net properties.
- decide which property difference to view and ignore in Design Differences.
- backannotate property changes to the schematic using Design Differences.

Viewing Net Property Differences

Task Overview

You will open the `atm.cpm` file in the `des_demos/net_properties/hdli` directory in Project Manager, and view the schematic in Design Entry HDL and the board in PCB Editor. First, compare the differences between the schematic and the `sync.brd` file. Next, compare the differences between the schematic and the `route_priority.brd` file.

Steps

1. Launch Project Manager.
2. Choose *Allegro Design Authoring* and click *OK*.
3. Load the `atm.cpm` file located in the `des_demos/net_properties/hdli` directory.
4. Click *Design Entry* in Project Manager to open the schematic in Design Entry HDL.

Design Entry HDL opens the `atm.cpm` project and displays the schematic.

5. Choose *Tools – Design Differences* in Design Entry HDL.

   The Design Differences dialog appears.

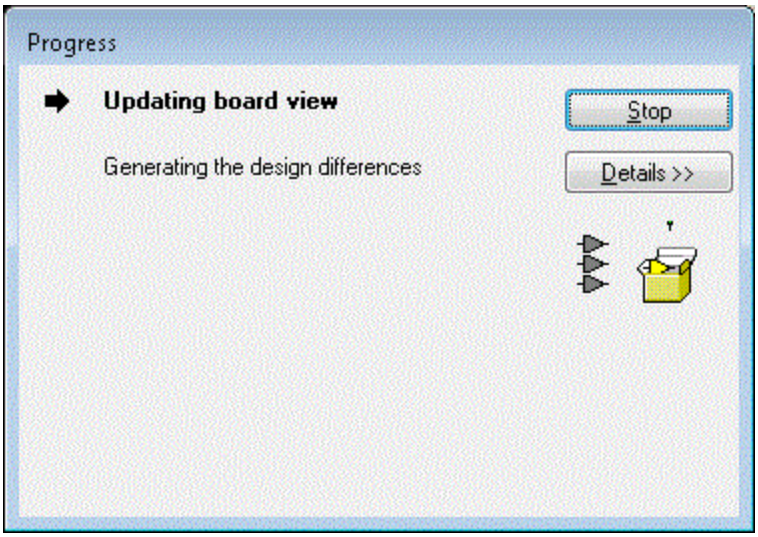
6. Select the *Update board view before compare* check box, click *Browse* and select the `sync.brd` file in the Select Board File dialog box.

7. Select the *Update package view before compare* check box in the Design Differences dialog and click *OK*.

   The Export Physical dialog appears. Leave the default options checked. Click *OK*.

   A Progress window appears with the information that the design is netlisted and being fed back. A message box appears prompting you to review the details and see the results. Click *No*.

Figure 5-1 Progress Window



The Progress window disappears as soon as the views are updated. The Message Log and the Constraints Differences windows are displayed in the Design Differences window.

To view if there are any design differences, select *Difference - Logical Constraints*. A message box appears confirming that there are no differences between the schematic and the `sync.brd` file for the `route_priority` property. You will now compare whether differences exist between the schematic and the `route_priority.brd` file.

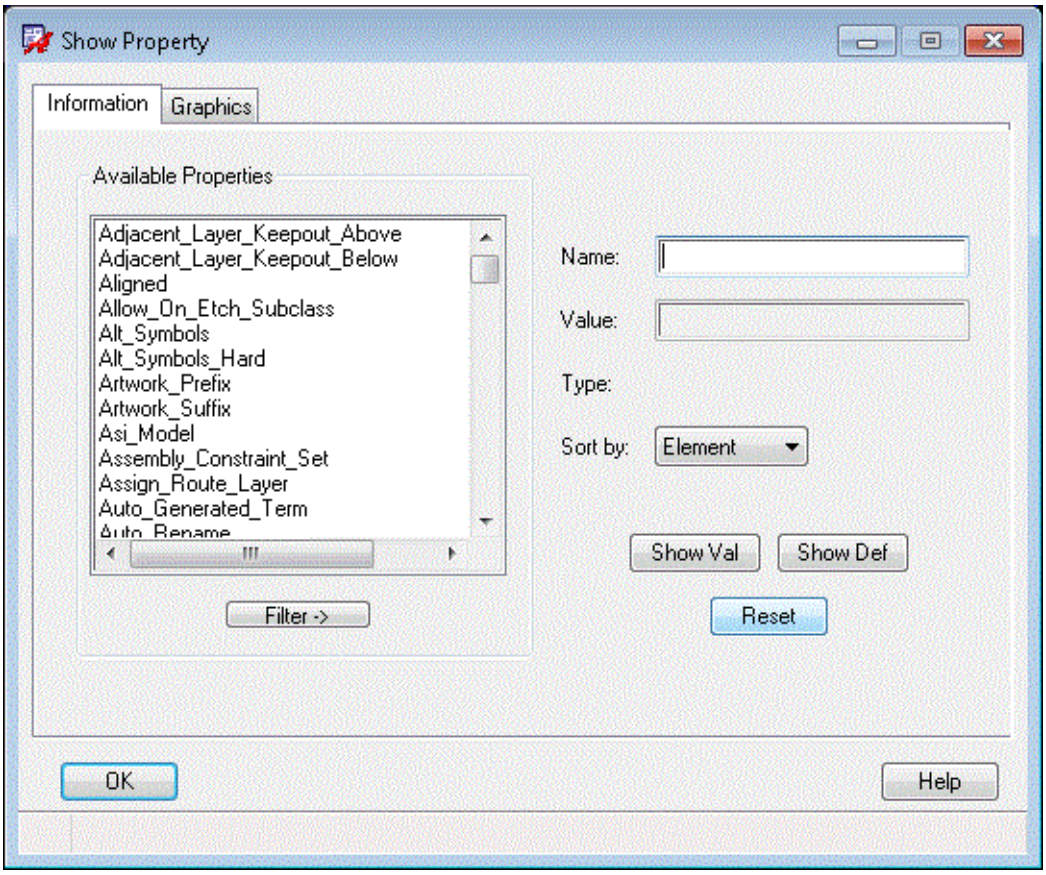
8. Click *Layout* in Project Manager to launch PCB Editor.

9. Choose *File – Open* in PCB Editor and load the `route-priority.brd` board file.

10. Choose *Display – Property* in PCB Editor.

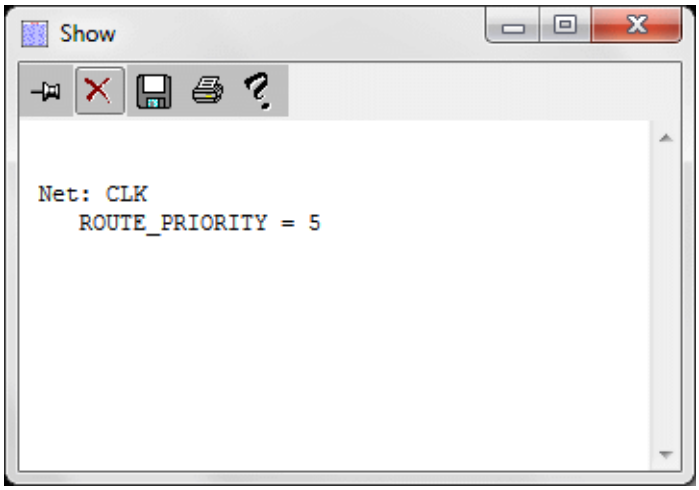
The Show Property dialog appears.

Figure 5-2 Show Property Dialog



11. Select the `ROUTE_PRIORITY` property from the *Available Properties* list, and click *Show Val*.

Show window appears and displays that the CLK net has the ROUTE_PRIORITY property attached to it.



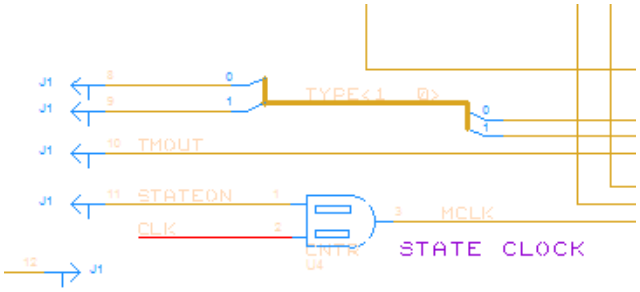
12. Close the Show window.
13. Verify that the CLK net in Design Entry HDL does not have the property ROUTE_PRIORITY attached to it.

Tip

Use the *Search options* button on the search toolbar to search for the CLK net and then check its properties.

14. Click *Search option*s on the Search toolbar in Design Entry HDL.
15. Type CLK in the *Find What* field.
16. Select the *Nets* check box.
17. Click *Find All*.
18. Click the result.

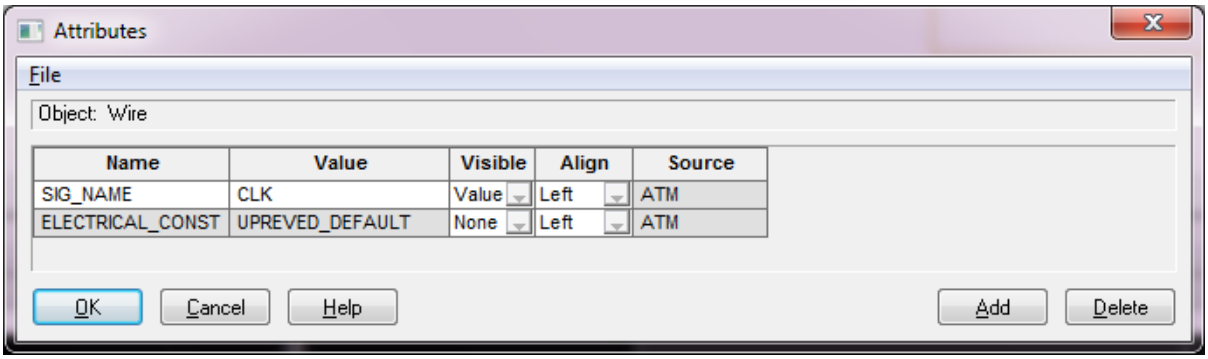
The signal CLK is highlighted in red. Check its properties.



19. To check the properties of the CLK signal, click the *Display Attributes* toolbar button and select the signal.

The Attributes dialog box appears. Verify that the `CLK` net in Design Entry HDL does not have the property `ROUTE_PRIORITY` attached to it.

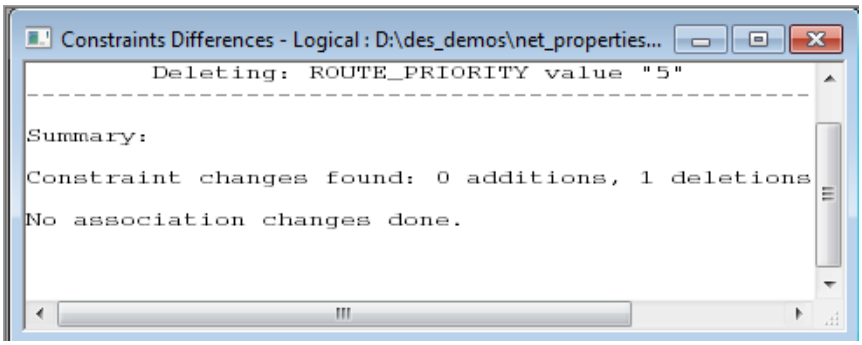
Close the Attributes dialog box.



20. Choose *File – Load PCB Editor Board* in Design Differences, and load the `route_priority.brd` board file in the Select Board File to Compare dialog box, and click *OK*.

A message box reports the successful loading of the board file. Click *OK*.

The Message Log Window and the Constraints Differences windows appear. The Constraints Differences - Logical window displays that the `route_priority` property has been deleted indicating that the property is in the board file but not in the schematic.



Changing the Property Flow Setup

Overview

The Property Flow Setup defines the properties that should be transferred between Design Entry HDL and PCB Editor. The design example in the `des_demos/net_properties/hdli` directory had the `ROUTE_PRIORITY` property defined as transferable between Design Entry HDL and PCB Editor.

Important

Define all properties that you want to transfer between Design Entry HDL and PCB Editor *before* you run Design Differences.

Task Overview

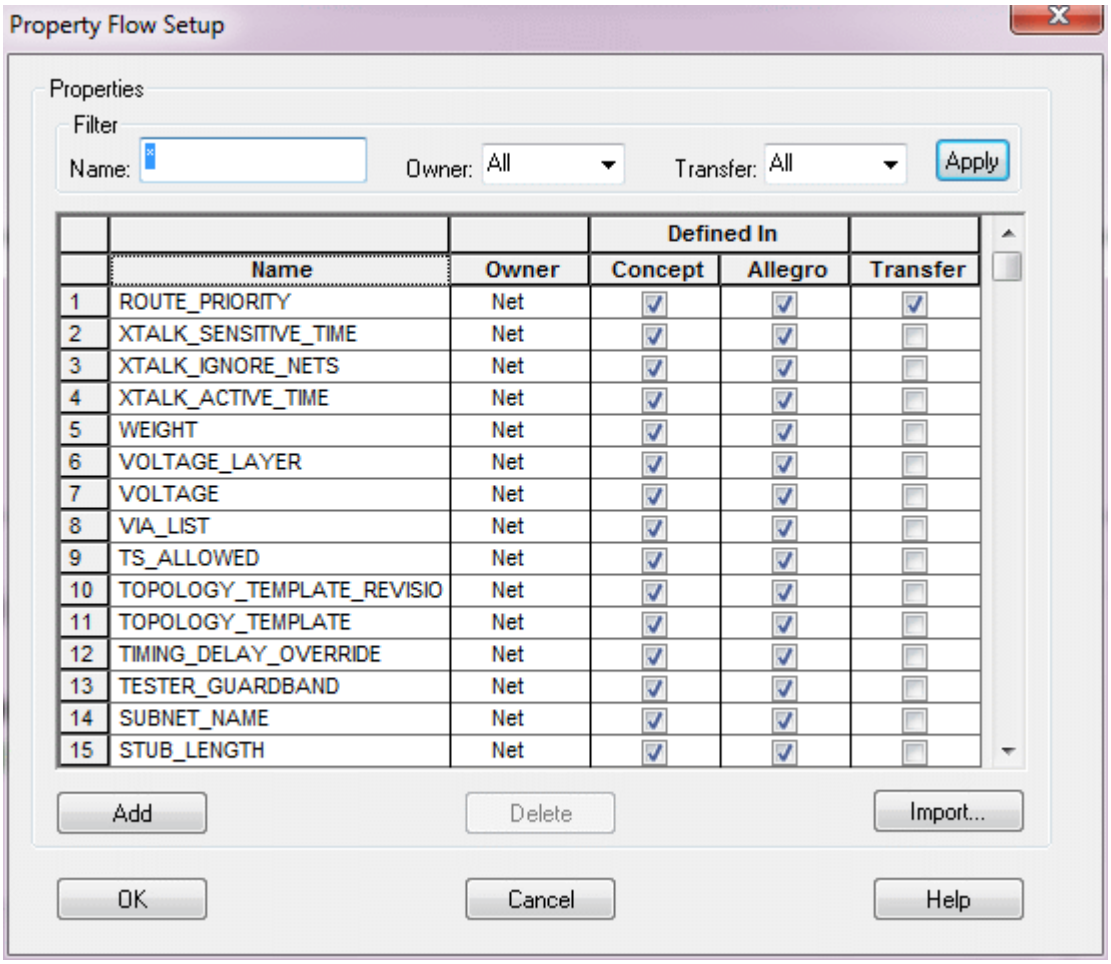
You will learn to change the Property Flow Setup by defining the `ROUTE_PRIORITY` property first as transferable and then as non-transferable.

Steps

1. Choose *Difference – Property Flow Setup* in Design Differences.

   The Property Flow Setup dialog appears.

Figure 5-3 Property Flow Setup dialog



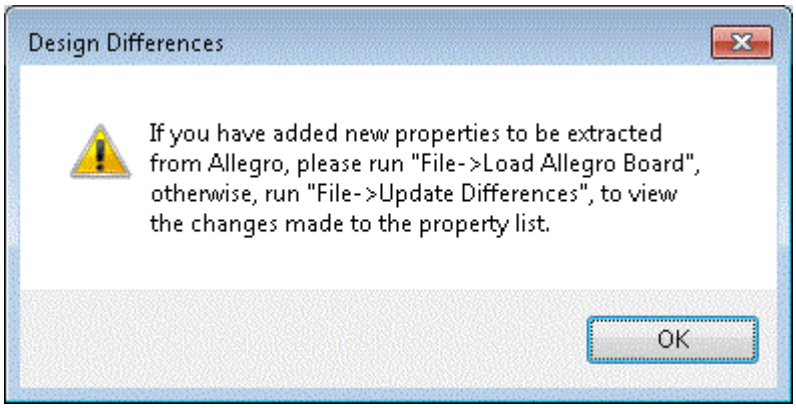
The Property Flow Setup dialog lists properties and defines whether these properties apply to Design Entry HDL, PCB Editor, or both. If you want any of these properties to be transferred from Design Entry HDL to PCB Editor, and back, you need to select its *Transfer* check box.

Note that the `ROUTE_PRIORITY` property has its *Transfer* check box selected.

2. Clear the *Transfer* check box corresponding to the `ROUTE_PRIORITY` property, and click *OK* to close the dialog.

   A message box appears with the prompt that you have made changes to the property list. You are prompted to reload the PCB Editor board or update differences.

Figure 5-4 Design Differences Message Box



3. Click *OK* to close the message box.
4. Choose *File – Update Differences* in Design Differences.

   The Message Log Window and Constraints Differences windows appear.
5. Re-define the `ROUTE_PRIORITY` property as transferable.
6. Click *OK* to close the Property Flow Setup dialog and click OK to the message that appears.
7. Select *File – Update Differences* again.

Exercise

1. Load the `max_via_count.brd` board in Design Differences and check the property differences between the schematic and the `max_via_count.brd` board.
2. Define the `MAX_VIA_COUNT` property as non-transferable in the Property Flow Setup dialog for the `max_via_count.brd` board and then use Design Differences to again check property differences between the schematic and the `max_via_count.brd` board.

Updating the Schematic with the Property Changes in the Board

Task Overview

You will now update the schematic with property differences in the `route_priority.brd` board file. Ensure that the schematic and board are in sync after the update.

Steps

1. Choose *File – Load PCB Editor Board* in Design Differences.
2. Select the `route_priority.brd` board file in the Select Board File to Compare dialog box and click *OK*.

   A message reports the successful reloading of the board file.
3. Click *OK* to proceed.
4. Choose *Sync – Update Design Entry HDL Schematic* in Design Differences.

   The message log in the Design Differences window is updated and the Import Physical dialog appears. Note that the *Backannotate Packaging Properties to Schematic Canvas* check box is selected. Leave it selected.
5. Click *OK*.

   A Progress window appears with the information that the design is netlisted and being fed back. The Design Entry HDL schematic is updated with the latest property information from the board. Finally a message box appears prompting you to view the results.
6. Click *No*.

   The control is passed back to Design Differences, which displays a message that the schematic has successfully loaded.
7. Click *OK*.

   Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Design Entry HDL schematic.
8. Click *OK* to close the message box.

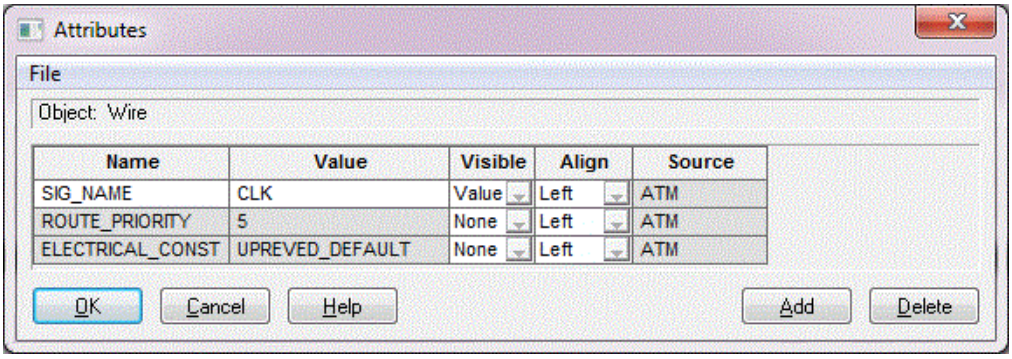
9. Open the Design Entry HDL schematic to confirm visually that the schematic has been updated.

Tip

Use the *Search options* button in Design Entry HDL to look for the CLK net. The CLK signal is highlighted.

10. Click the *Display Attributes* toolbar button and select the CLK signal.

    The Attributes dialog box appears. Verify that the `CLK` net in Design Entry HDL has the property `ROUTE_PRIORITY` property attached to it.



11. Close the Attributes dialog box.

12. Choose *File – Exit* in Design Differences, PCB Editor, Design Entry HDL, and Project Manager. Do not save any changes.

6

Synchronizing Component Properties Differences

Objective

To view differences in component properties in Design Differences and update the schematic as per the differences

At the end of this chapter, you will be able to

- Use Design Differences to view differences caused by changes in component properties.
- query the logical design or the physical design from Design Differences.
- update instance property changes to the schematic.

Viewing Component Property Differences

Task Overview

You will open the `atm.cpm` file in the `des_demos/component_properties/hdli` directory in Project Manager and view the schematic in Design Entry HDL and the board in PCB Editor. Compare the differences between the schematic and the `u6_props_mod.brd` file.

Steps

1. Load the `atm.cpm` file located in the `des_demos/component_properties/hdli` directory in Project Manager.
2. Click the *Design Entry* button in Project Manager to open the schematic in Design Entry HDL.

Design Entry HDL opens the `atm.cpm` project and displays the schematic.

3. Click *Layout* in Project Manager to launch PCB Editor.
4. Choose *File – Open* in PCB Editor and load the `u6_props_mod.brd` file.
5. Choose *Display – Property* in PCB Editor.

   The Show Property dialog appears.
6. Choose the property `ROOM`, and set the value as `CPU`.
7. Click *Show Val*.

   The Show window displays the following values.

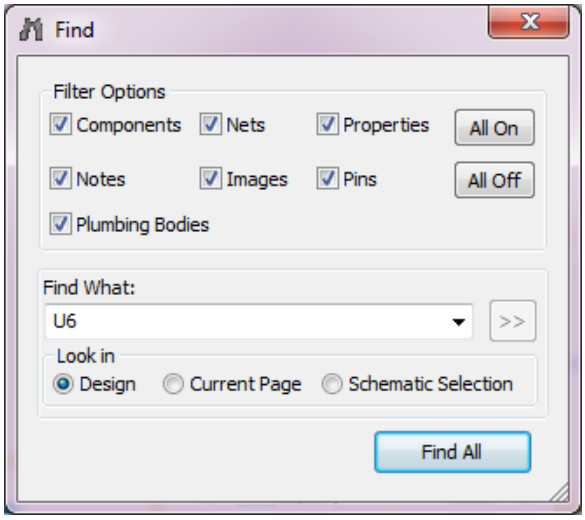
```
Component: U6
   ROOM = CPU
Function: F7
   ROOM = CPU
```

8. Close the Show window to return to the *Show Property* window.
9. Click *OK.*

   Switch to Design Entry HDL. Verify that no component in Design Entry HDL schematic has the `ROOM` property with the value `CPU`.
10. In Design Entry HDL, click the *Search options* button on the search toolbar.

    The Find dialog box is displayed.

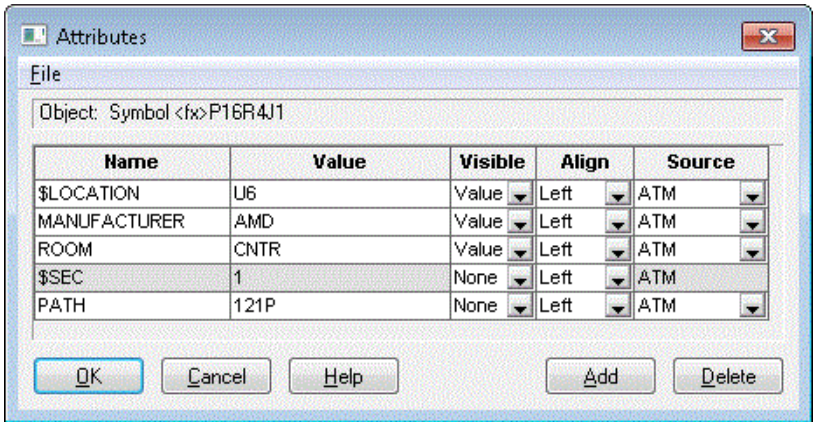
11. Search for the `U6` component.



The `U6` component in the schematic is highlighted.

12. Right-click the component (symbol P16R4J1) and select *Attribute*.

The Attributes window is displayed.



Click *OK* to close the Attributes window and close the Find dialog box.

13. Choose *Tools – Design Differences* in Design Entry HDL.

The Design Differences dialog appears.

14. Select `u6_props_mod` as the PCB Editor board.

15. Ensure that the *Update package view before compare* check box is selected.

16. Click *OK* to start Design Differences.

The Export Physical dialog appears. Note that the *Update PCB Editor Board (Netrev)* check box is grayed out. You cannot update the board. Ensure that *Backannotate Packaging Properties to Schematic Canvas* is selected.

17. Click *OK* to package the design.

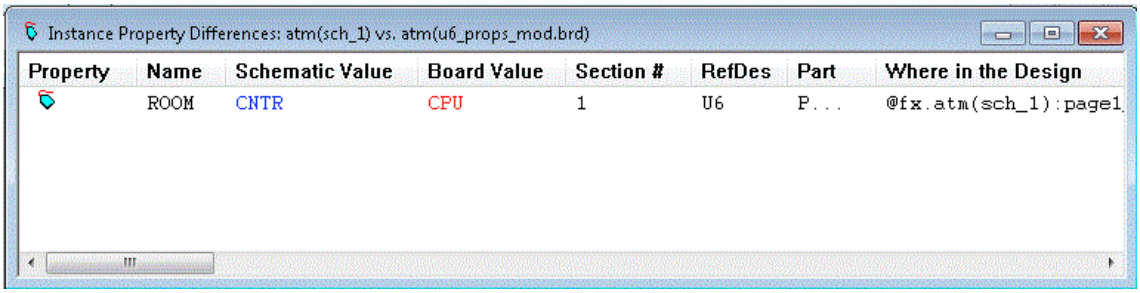
The Progress window appears with the information that the design is being netlisted and packaged. After the packaging of the design is completed, a message box appears prompting you to view the results.

18. Click *No*.

The control is passed back to Design Differences, which compares the board and the schematic information.

The Message Log Window, Constraints Differences, and Instance Property Differences windows appear. The Instance Property Differences window lists differences in the `ROOM` property. Note that the `ROOM` property has the value `CNTR` in the schematic and the value `CPU` in the board.

Figure 6-1 Instance Property Window



You have verified that differences exist between the `sch_1` schematic and the `u6_props_mod.brd` board file. You will now use Design Differences to find these differences.

Exploring Logical and Physical Designs in Design Differences

Task Overview

Use Design Differences to browse to the logical design, that is, the schematic, and the physical design, that is the board. Additionally, you can use Design Differences to browse to any component, net, or part and find any property attached to it.

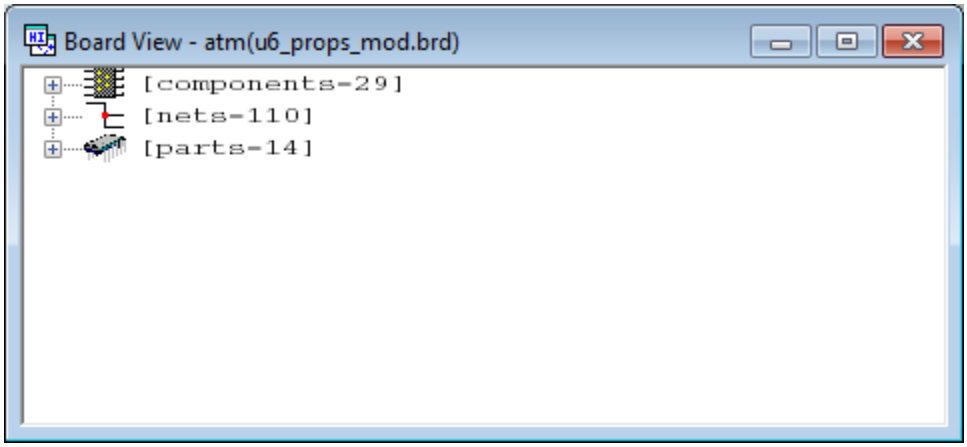
You will now browse through the physical design and verify the value of the `ROOM` property attached to the `U6` component.

Steps

1. Choose *Explore – Physical Design* in Design Differences.

   A window named Board View appears. The board name `atm(u6_props_mod.brd)` is displayed on the title bar.

Figure 6-2 Board View window



   You will now browse through this window to find out how many components have the `ROOM` property attached and why this property is causing differences.

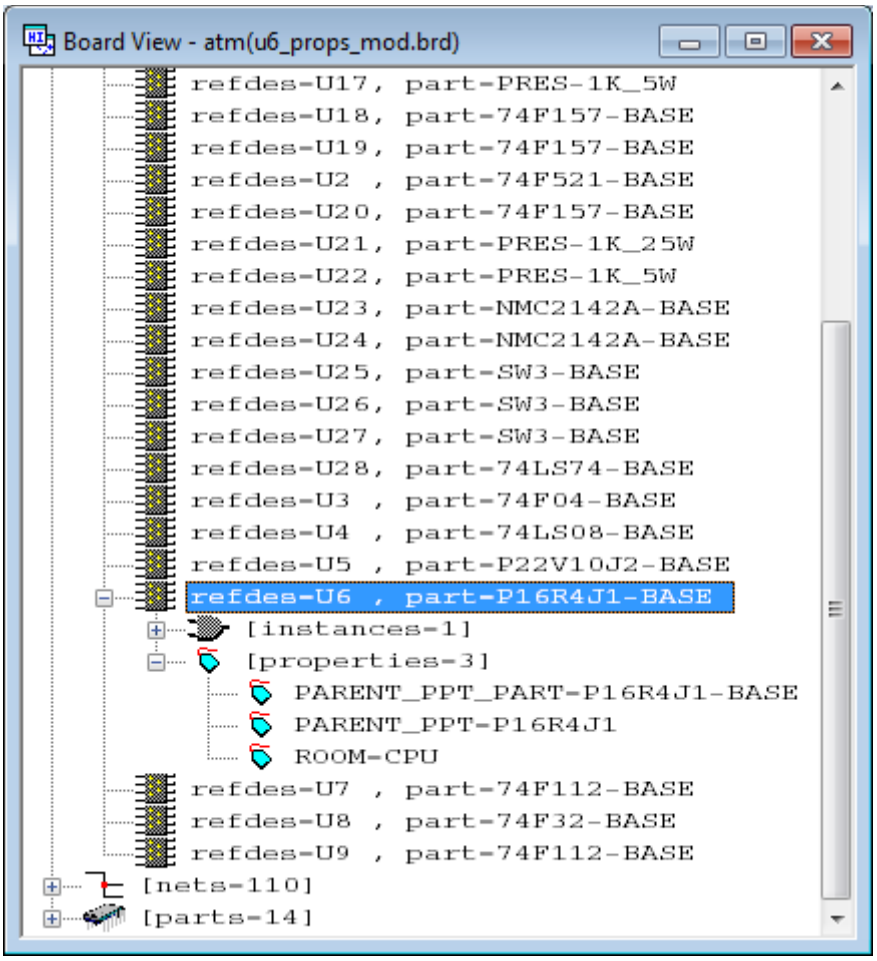
2. Expand the *Components* branch by clicking the + button to the left of the *(Components=29)* row.

3. Double-click the branch *`refdes=U6`*.

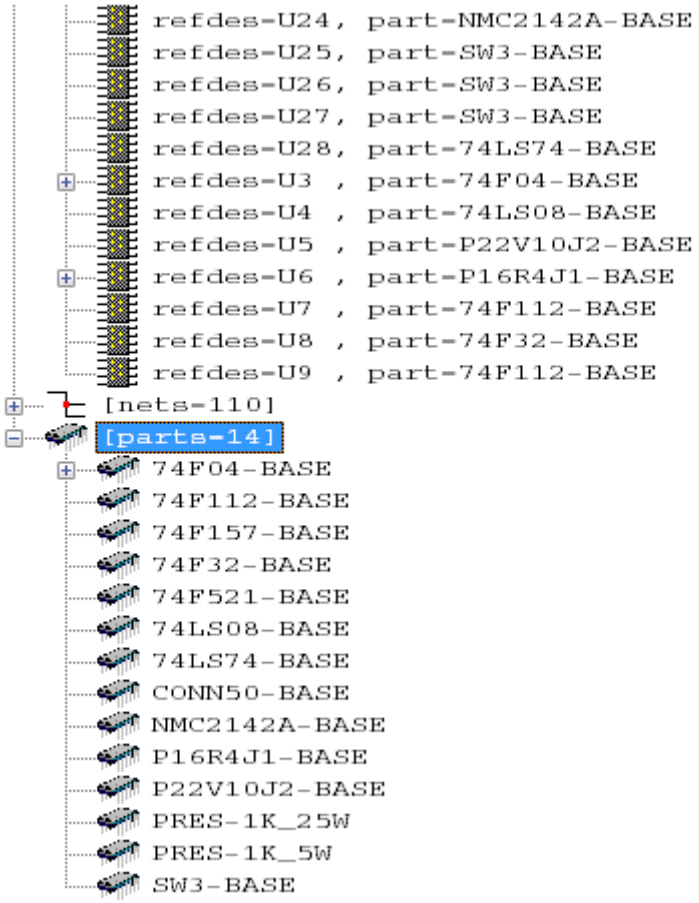
4. Expand the *[properties=3]* row.

   Note that the `ROOM` property is attached to the `U6` component. See Figure 6-3.

Figure 6-3 Board Window: Expanded



5. Explore another branch. For example, determine how many `74F04` inverters are being used in the design. Expand the branch *`[parts=14]`*.



6. Double-click the *`74F04`* part.

   Note that the `74F04` part is a two-pin component with 11 default properties and that there are three such components on the board.

7. Expand the *[components=3]* row.

   The reference designators of the three components appear. You can further expand the rows corresponding to these components and find information about instances and properties of each component.

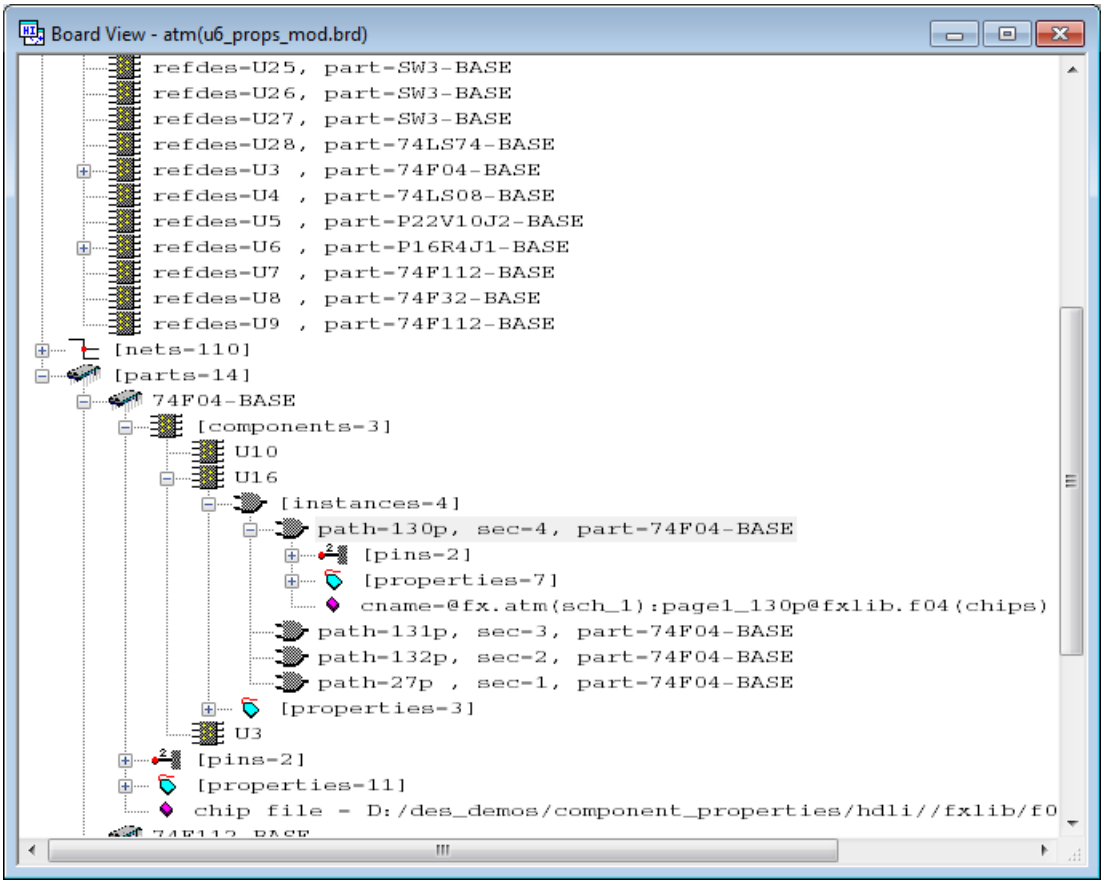
8. Expand the *`U16`* component.

   The `U16` component has four instances and three properties attached to it.

9. Expand the *[instances=4]* row.

10. Expand the first instance with *path = 130p*.

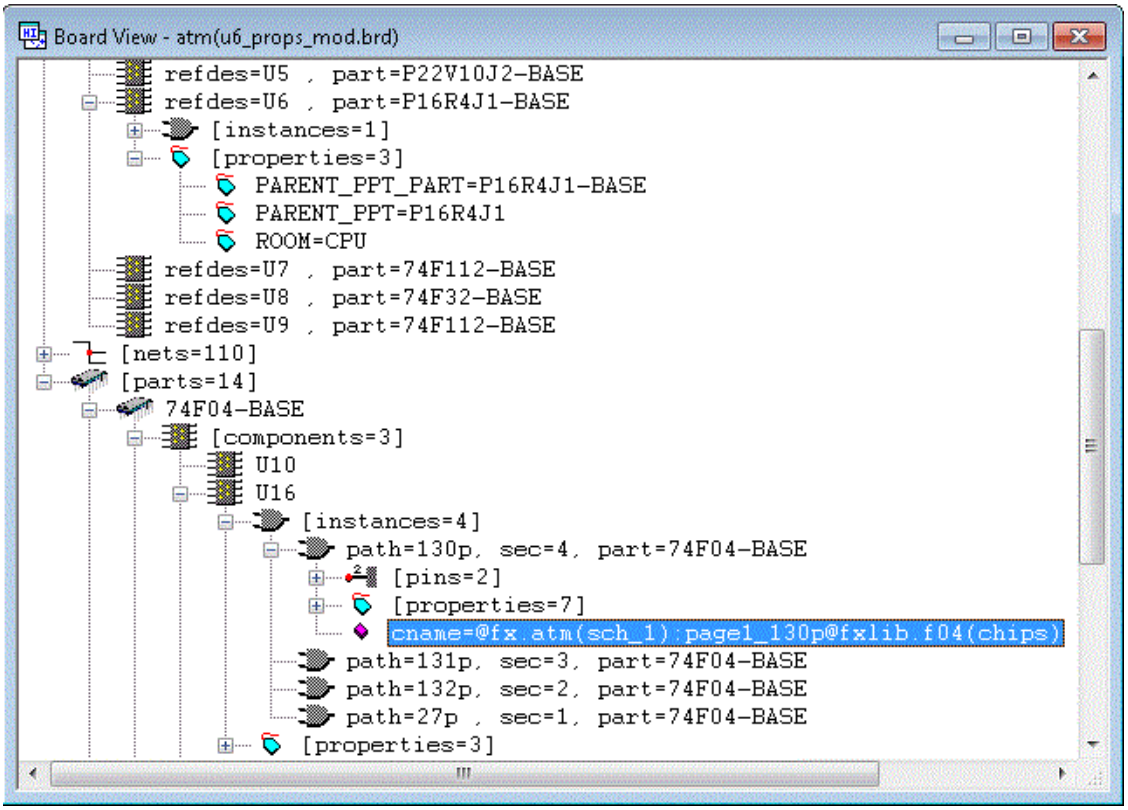
Information about the pins, instance properties, and canonical name appears.



Note: To find the component that corresponds to a row in Design Differences, right-click the row in Design Differences and select *Highlight Source*.

11. Select the row corresponding to the canonical name `cname=@fx.atm`.

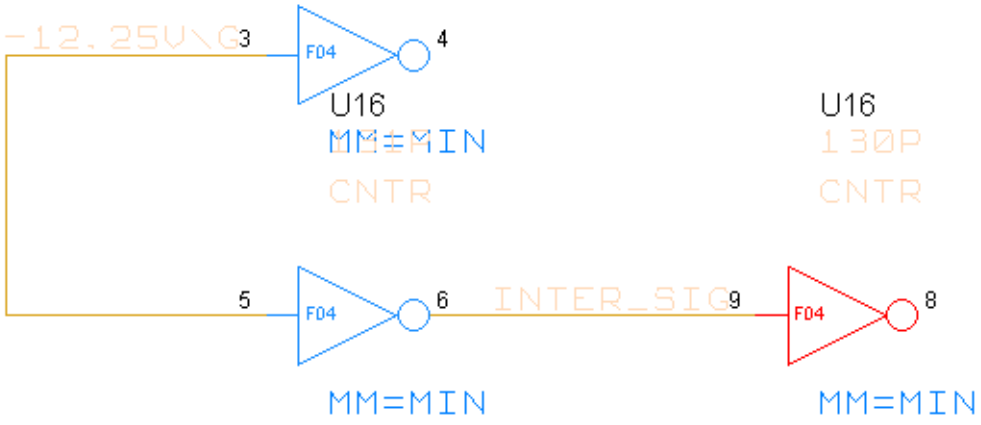
Figure 6-4 Board View Window: Canonical Path Selected



12. Right-click and select *Highlight Source*.

The following figure displays the component corresponding to the canonical name `cname=@fx.atm` highlighted in Design Entry HDL.

Figure 6-5 Design Entry HDL: Source Selected



Exercise

Browse the logical design to verify the values of different properties for the `U6` component.

Tip

Choose *Explore - Logical Design* and expand the design.

Querying a Design from Design Differences

Task Overview

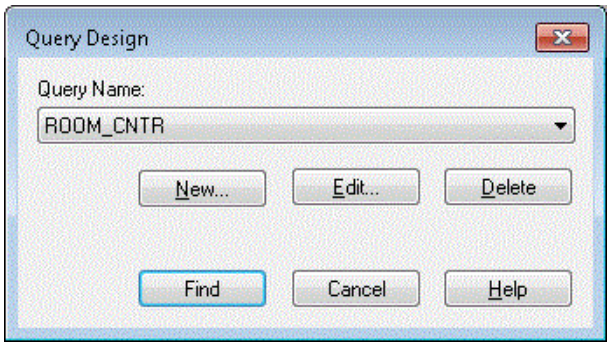
Query the design for specific properties in both the logical and physical designs. Query the design for an instance that has the `ROOM` property with the value `CNTR` attached to it.

Steps

1. Choose *Explore – Query Design* in Design Differences.

   The Query Design dialog box appears.

Figure 6-6 Query Design Dialog Box

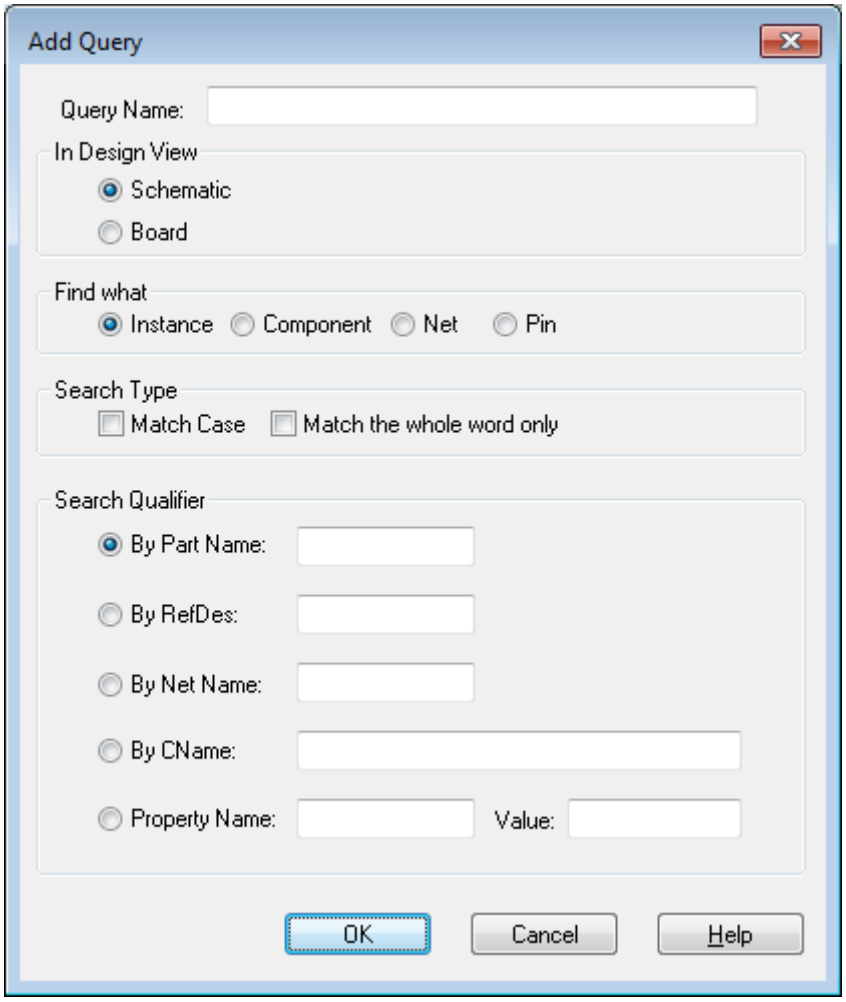


   The *Query Name* field displays existing queries. To create new queries, click *New*. Similarly, to edit an existing query, click *Edit*.

2. Click *New* to create a new query.

   The Add Query dialog appears.

Figure 6-7 Add Query Dialog



3. Set the following values in the *Add Query* dialog:

   ```
   Query Name = ROOM_CNTR

   In Design View = Schematic

   Find what = Instance

   Property Name = ROOM

   Value = CNTR
   ```

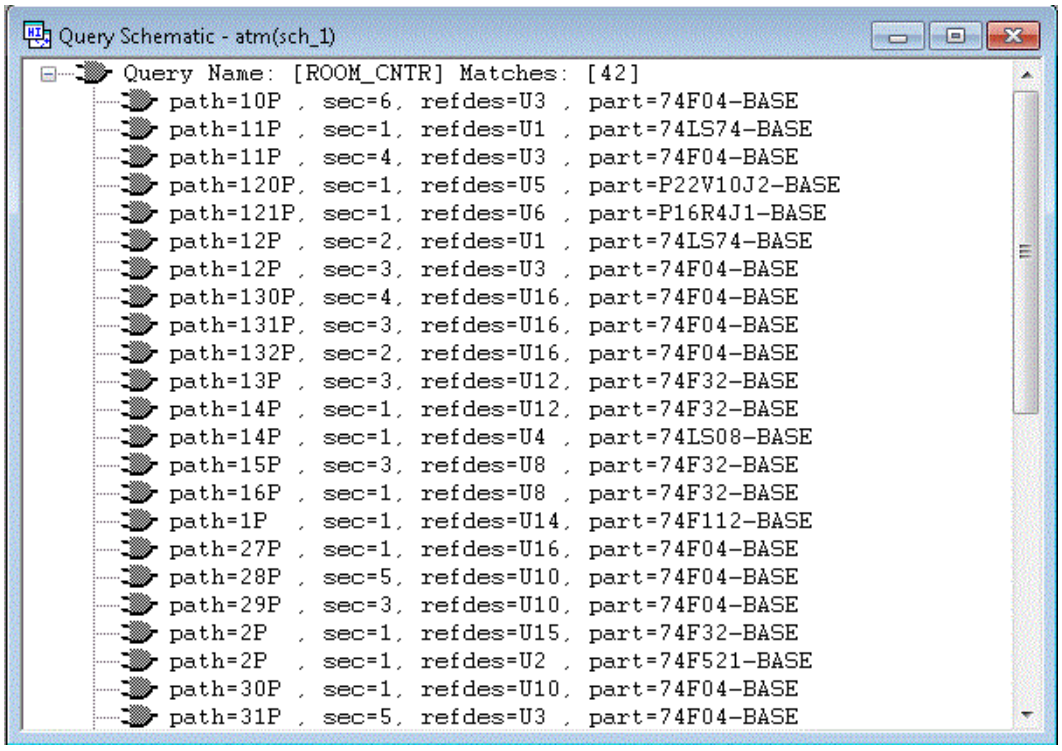
4. Click *OK* to save the query.

   The Query Design dialog box appears.

5. Choose *Find* to run the query.

   The Query Schematic window appears with all the matching instances listed.

Figure 6-8 Query Schematic Window



The first line in the Query Schematic shows the name of the query. Note that 42 matches are returned.

Note: Expand any of the instances to see the pin and property details about the instances.

Exercise

Query the physical design to locate all instances where the `ROOM` property has the value `CPU`.

Hint

Define a new query and choose the design view as board.

Note: You can have more than one query window open. Use these windows to compare designs by using specific sets of properties.

Updating the Schematic with Component Property Differences

Task Overview

You will now update the schematic with property differences in the `u6_props_mod.brd` board file. Ensure that the schematic and board are in sync after the update.

Steps

1. Choose *File – Load PCB Editor Board* in Design Differences.

   The Select Board File to Compare dialog box appears.

2. Select the `u6_props_mod.brd` board file and click *OK*.

   A message box informs you that the board is successfully loaded.

3. Click *OK* to proceed.

4. Choose *Sync – Update Design Entry HDL Schematic* in Design Differences.

   The Preview ECO on Schematic dialog box is displayed. The *Property Changes List* displays differences in the `ROOM` property.

5. Click *OK* to update the schematic.

   The message log in the Design Differences window is updated and the Import Physical dialog appears.

6. Clear the *Backannotate Packaging Properties to Schematic Canvas* check box if it is selected.

7. Click *OK*.

   A Progress window appears with the information that the design is netlisted and being fed back. Finally a message box appears prompting you to view the Packager results.

8. Click *No*.

   The control is passed back to Design Differences, which displays a message that the schematic is successfully loaded.

9. Click *OK*.

   Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Design Entry HDL schematic.

10. Select *Difference – Inst Property* to check whether the board and the schematic are in sync.

    A message box appears confirming that there are no differences.

11. Click *OK* to close the message box.

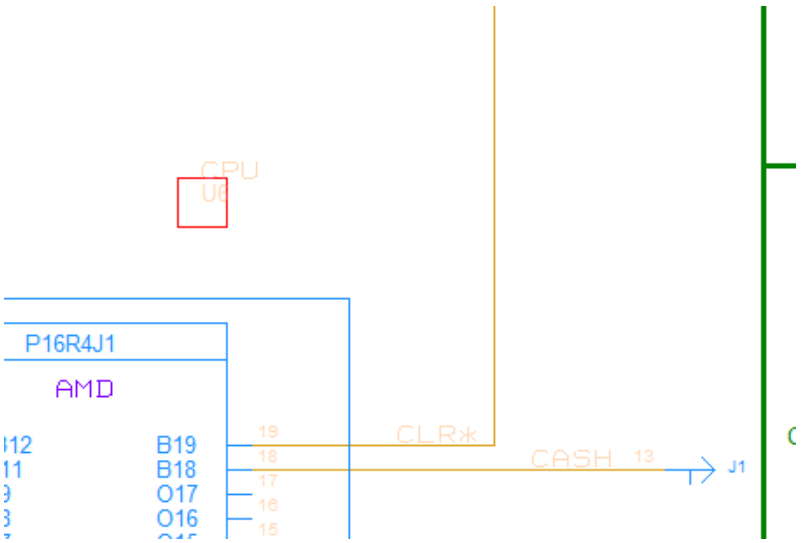
12. Choose *Tools – Back Annotate* in the Design Entry HDL window to update the Design Entry HDL schematic with the changes in the packager files using the `pstback.dat` file.

    Note that the `pstback.dat` file is selected for backannotation.

13. Click *OK*.

    The Design Entry HDL schematic is updated with the latest property information from the board.

14. Confirm visually that the schematic has been updated.



15. Choose *File – Exit* in Design Differences, PCB Editor, Design Entry, and Project Manager. Do not save any changes.

7

Synchronizing Pin Properties Differences

Objective

To view differences in pin properties by using Design Differences and to update the schematic with the differences

At the end of this chapter, you will be able to:

- use Design Differences to view differences caused by changes in pin properties.
- view differences in pin properties between the schematic and the board.
- save difference information and view the differences later.

Viewing Pin Property Differences

Task Overview

You will open the `atm.cpm` file in the `des_demos/pin_properties/hdli` directory in Project Manager, and view the schematic in Design Entry HDL and the board in PCB Editor. First, compare the differences between the schematic and the `u16_pin_properties.brd` file. Next, compare the differences between the schematic and the `syncs.brd` file.

Steps

1. Load the `atm.cpm` file located in the `des_demos/pin_properties/hdli` directory in Project Manager.
2. Click *Design Entry* in Project Manager to open the schematic in Design Entry HDL.

   Design Entry HDL opens the `atm.cpm` project and displays the schematic.
3. Choose *Tools – Design Differences* in Design Entry HDL.

The Design Differences dialog appears.

4. Click *Browse*.

   The Select Board File dialog box appears.

5. Select `sync.brd`.

6. Clear the *Update package view before compare* box.

7. Click *OK* to start Design Differences.

   The Message Log Window and Constraint Differences windows are displayed.

8. Select *Difference – Pin Property* to check whether there are differences between the schematic and the `sync.brd` file.

   A message box appears confirming that there are no differences between the schematic and the board (`sync.brd`). Click *OK* to close the box.

   Now check if differences exist between the schematic and the `u16_pin_properties.brd` file.

9. Click the *Layout* button in Project Manager to launch PCB Editor.

10. Choose *File – Open* in PCB Editor and load the `u16_pin_properties.brd` file.

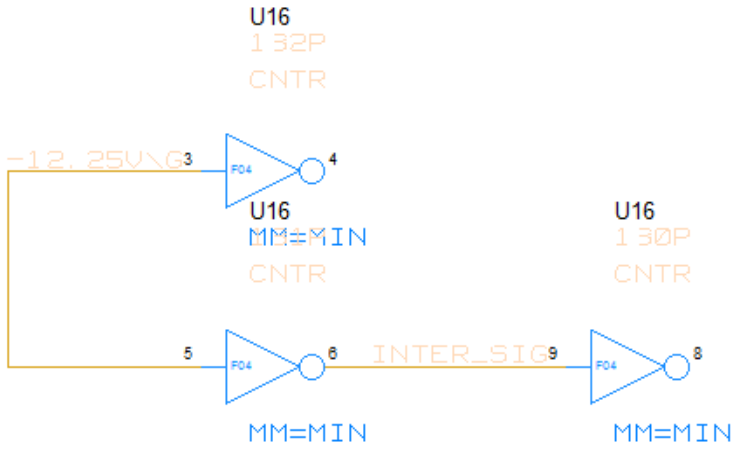
11. Choose *Display – Property* in PCB Editor.

    The Show Property dialog appears.

12. Select the property `PINUSE` from the *Available Properties* list, and click *Show Val*.

    Show window appears displaying that the `U16` and `U22` components have the `PINUSE` property with the value `BI`.

13. In Design Entry HDL, verify that the `U16` component in the schematic does not have the `PINUSE` property with the value `BI`.



14. Close the Show Property dialog in PCB Editor.

15. Choose *Difference – Property Setup* in Design Differences.

The Property Flow Setup dialog appears.

16. Ensure that the *Transfer* check box corresponding to the `PINUSE` property is selected.

17. Click *Cancel* to close the Property Flow Setup dialog.

18. Choose *File – Load PCB Editor Board* in Design Differences, and select the `u16_pin_properties.brd` board file in the Select Board File to Compare dialog box.

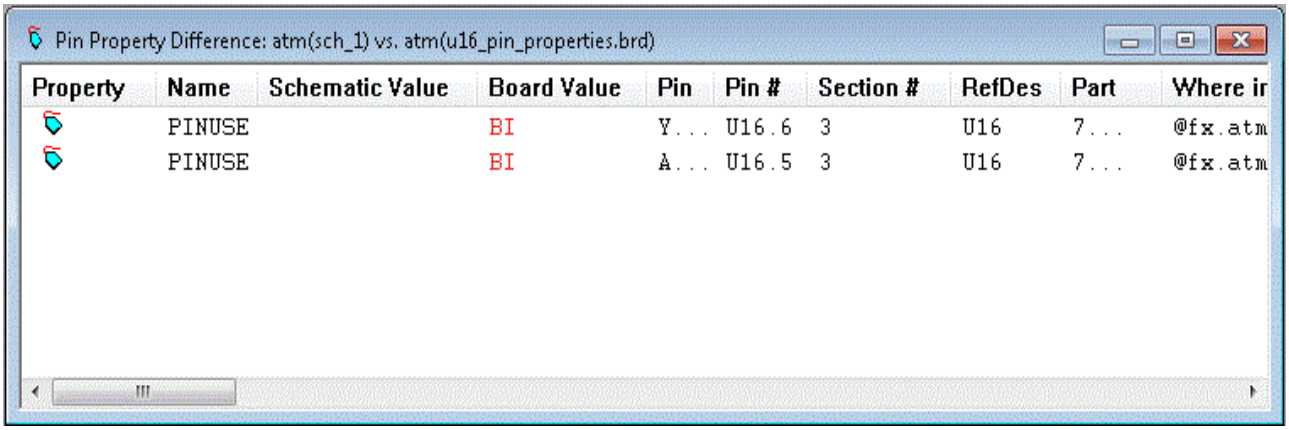
19. Click *OK*.

A message informs you that the board has been successfully loaded.

20. Click *OK* to proceed.

The Message Log Window, Constraints Differences, and the Pin Property Difference windows appear.

Figure 7-1 Pin Property Difference Window



The Pin Property Difference window lists differences in the `PINUSE` property. Note that the `PINUSE` property has the value `BI` in the board. This property is not listed in the schematic.

Saving the Output Difference Information

Task Overview

You can save the difference information in a text file for future reference. You will also save the pin property difference information that you generated in the last procedure to a text file. You will view this file using Design Differences.

Tip

You can view any text file from within Design Differences.

Steps

1. Ensure that the Pin Property Difference window is active. For this, choose *Difference – Pin Property* in Design Differences, if needed.
2. Choose *File – Output Difference* to display the pin property differences in the `pinprop.dif` file.

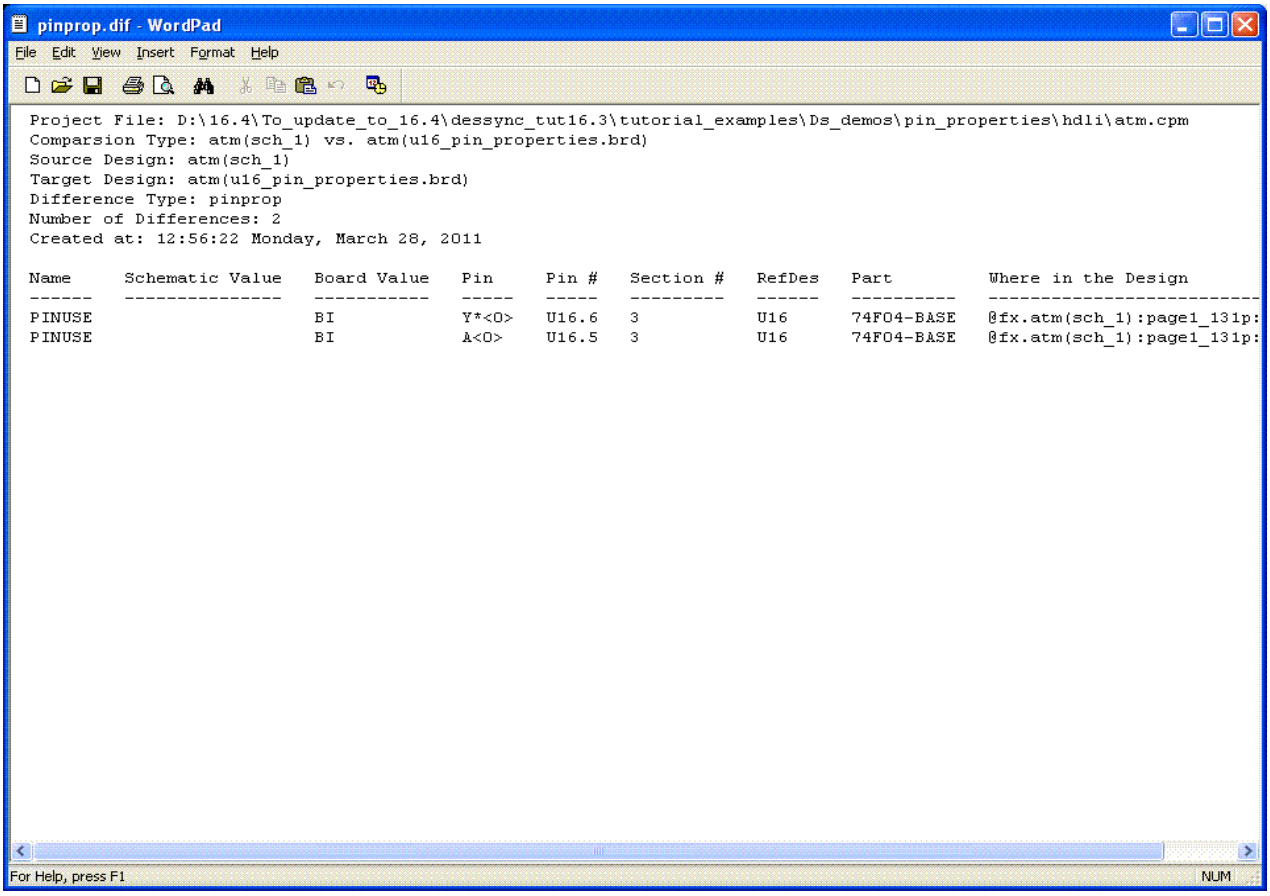
   A text window displays the `pinprop.dif` file. Note that this file is generated in the `packaged` view.
3. Close the `pinprop.dif` file.

4. Choose *File – View File* in Design Differences to open the `pinprop.dif` file from within Design Differences.

   The Choose File browser appears.

5. Select the `pinprop.dif` file from `des_demos/pin_properties/hdli/fx/atm/packaged`, and click *Open*.

Figure 7-2 Pin Property Difference File (pinprop.dif)



Updating the Schematic with Pin Property Differences

Task Overview

You will now update the schematic with the pin property differences in the `u16_pin_properties.brd` board file, and then ensure that the schematic and board are in sync after the update.

Steps

1. Choose *File – Load PCB Editor Board* in Design Differences.

   The Select Board File to Compare dialog box appears.

2. Select the `u16_pin_properties.brd` board file.

3. Click *OK* to proceed.

4. Click *OK* to close the message box that appears.

   A message log, the Constraints Differences - Physical windows, and the Pin Property Difference window appears.

5. Choose *Sync – Update Design Entry HDL Schematic* in Design Differences.

   The Preview ECO on Schematic dialog is displayed. The *Property Changes List* displays differences in the `PINUSE` property.

6. Click *OK* to update the schematic.

   The message log in the Design Differences window is updated and the Import Physical dialog appears.

7. Select *Overwrite current constraints*.

8. Leave the other default options selected and click *OK*.

   A progress window appears with the information that the design is netlisted and being fed back. Finally, a message box appears prompting you to view the results.

9. Click *No*.

   The control is passed back to Design Differences, which displays a message that the schematic has loaded successfully.

10. Click *OK*.

Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Design Entry HDL schematic.

11. Select *Difference – Pin Property* to check whether there are differences between the board file and the schematic.

A message box appears confirming that there are no differences.

12. Click *OK* to close the message box.

Taking New Pin Properties to the Board

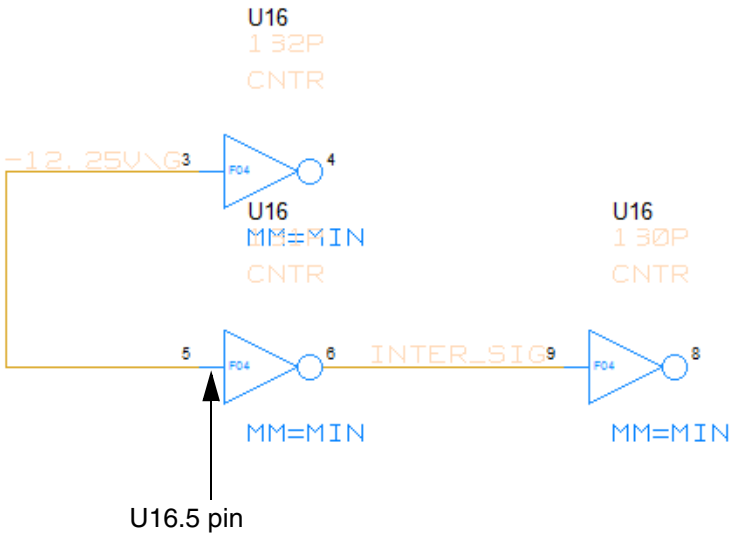
Task Overview

You will now define a new property, `LEAD_RESISTANCE`, in the schematic, and update it to the board.

Steps

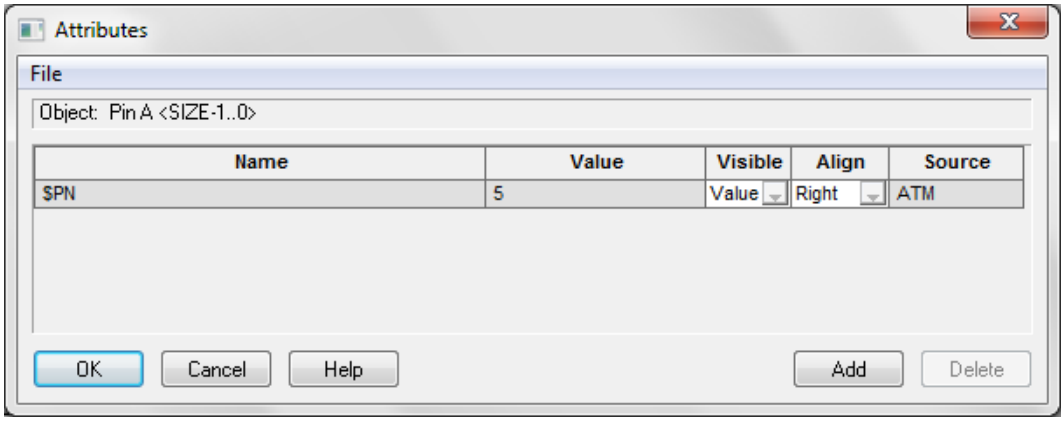
1. Choose *Text – Attributes* in Design Entry HDL.

2. Click the *Search options* button and perform a search for the *U16* pin.



3. Attach the `LEAD_RESISTANCE` property with a value `0.05` to the *U16.5* pin. To attach the `LEAD_RESISTANCE` property, click the *Display Attributes* ( ) toolbar button and select the *U16.5* pin.

The Attributes dialog box appears.



a. Click the *Add* button and specify `LEAD_RESISTANCE` in the Name field of the new row.

b. Enter the value as `0.05`.

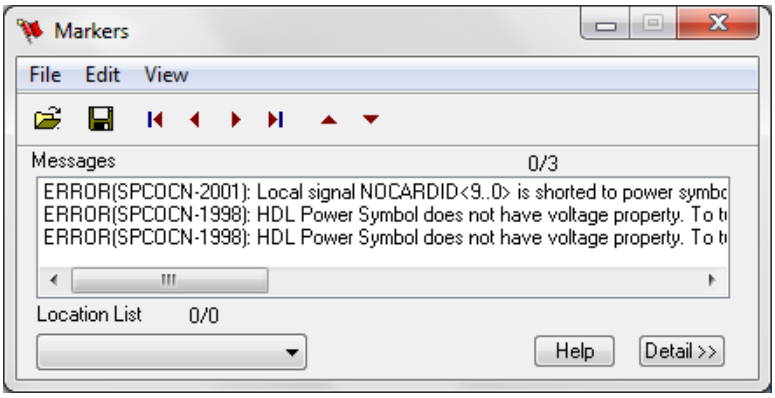
c. Click *OK* to add the property and close the Attributes dialog box.

You will now update this property to the board.

4. Choose *File – Save* in Design Entry HDL to save the schematic.

A message box indicating three errors may appear. Ignore the errors and click *Save* in the Design Entry HDL message box.

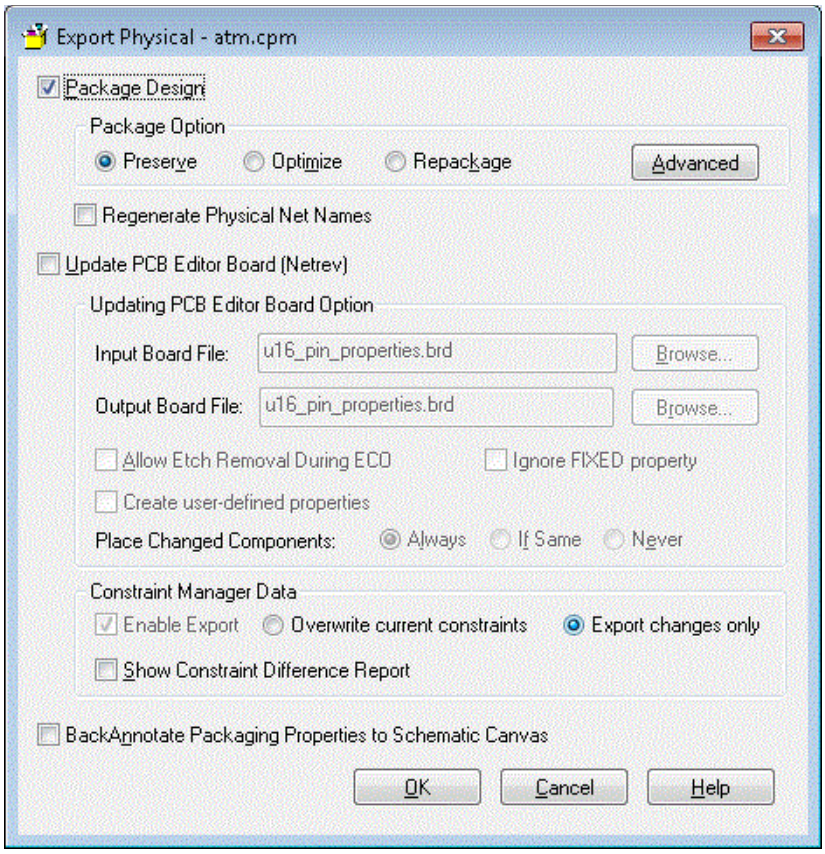
You can click on *View Errors* if you want to view the error details.



5. Choose *File – Export Physical* to package the design.

The Export Physical dialog appears.

Figure 7-3 Export Physical dialog



6. Choose only the *Package Design* option, set the option to *Preserve*, deselect all the other options, and click *OK* to package the design.

   A message box appears with the information that packaging has finished successfully and prompts you to check the results.

7. Click *Yes*.

8. Click *View Results* in the Progress message box and select the `pstxnet.dat` file. Click *OK*.

   The `pstxnet.dat` file opens in a text editor.

9. Search for the text `LEAD_RESISTANCE` in the file.

   The `LEAD_RESISTANCE` property is defined in the file.

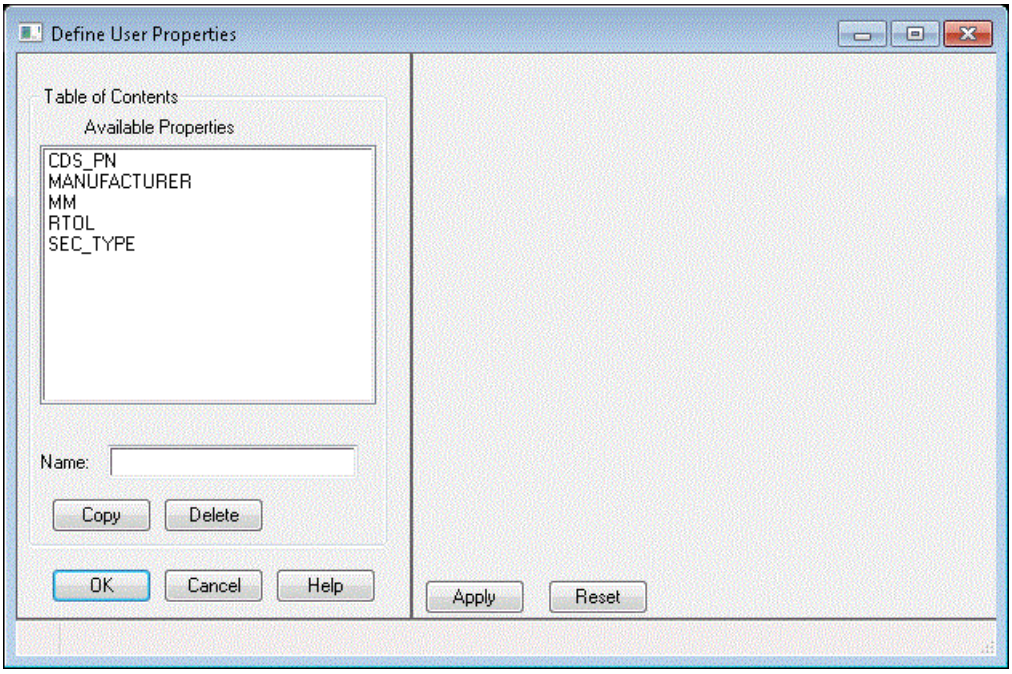
10. Exit the text editor, and close the Progress window.

    You need to define the `LEAD_RESISTANCE` property on the board.

11. Open the `u16_pin_properties.brd` board in PCB Editor.
12. Choose *Setup – Property Definition*s.

    The Define User Properties dialog appears.

Figure 7-4 Define User Properties Dialog



13. Type `LEAD_RESISTANCE` as the property name in the *Name* field, and click *Apply*.
14. Clear all the check box under *Data Elements section* except the *Pins* check box, choose *STRING* in the *Data Type* drop-down list, and then click *OK.*
15. Choose *File – Save As* and save the board as `lead_resistance.brd`.
16. Choose *Display – Property* in PCB Editor.
17. Choose the `LEAD_RESISTANCE` property and click *Show Val.*

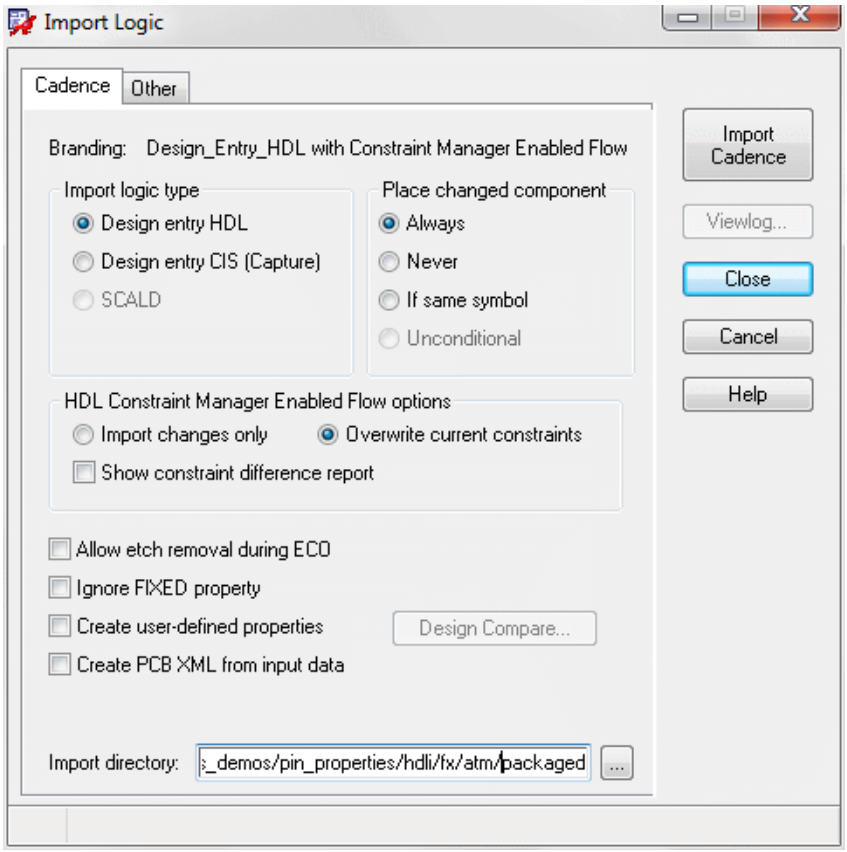
    The following message appears in the PCB Editor console window:

    ```
    W- (SPMHGE-249):No Instances of property LEAD_RESISTANCE found.
    ```

    Close the Show Property dialog. You will now import the schematic into this board.
18. Choose *File – Import – Logic* in PCB Editor.

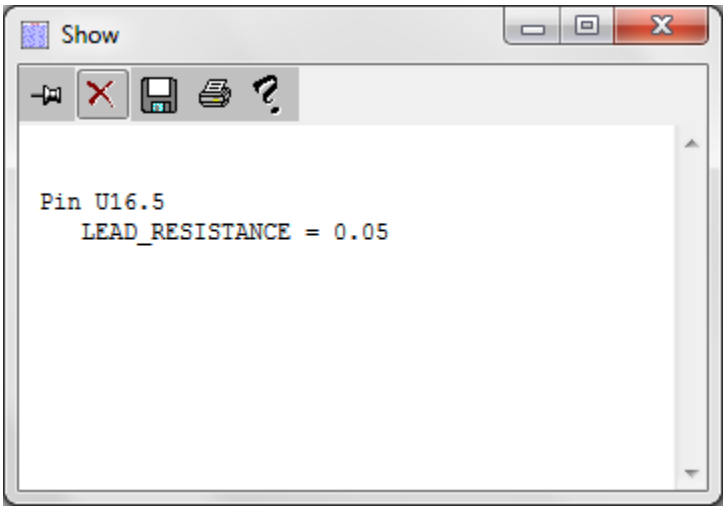
    The Import Logic dialog appears.

Figure 7-5 Import Logic dialog



19. Select *Design Entry HDL* in the *Import logic type* section.
20. Ensure that *Overwrite current constraints* is selected in *HDL Constraint Manager Enabled Flow options* section.
21. Select the `packaged` directory in the *Import directory* field.
22. Click *Import*.
23. Choose *Display – Property* in PCB Editor.
24. Select the property `LEAD_RESISTANCE`, and click *Show Val*.

A box appears showing that the `U16.5` pin has the `LEAD_RESISTANCE` property with the value `0.05`.



Synchronizing Differences Caused By New Properties in PCB Editor

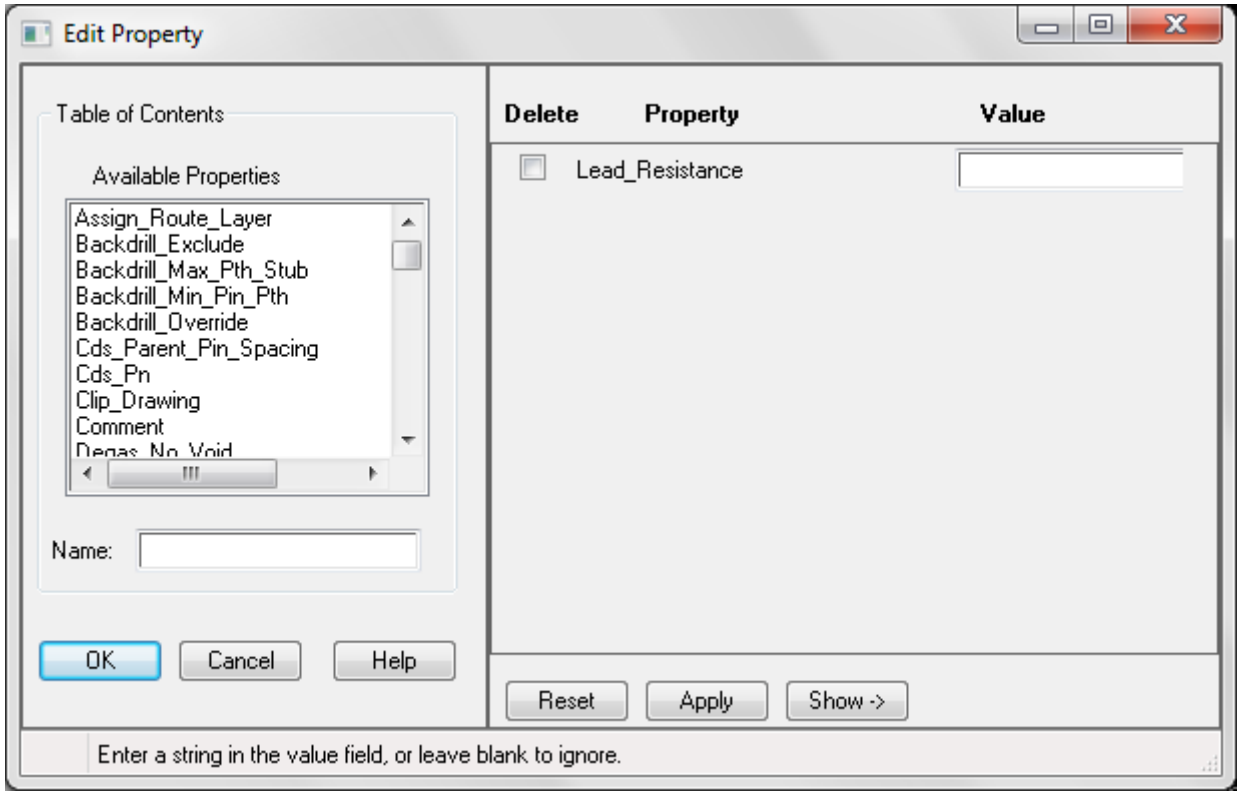
Task Overview

You will now edit the `LEAD_RESISTANCE` property in the `lead_resistance.brd` board, and then synchronize the schematic using Design Differences.

Steps

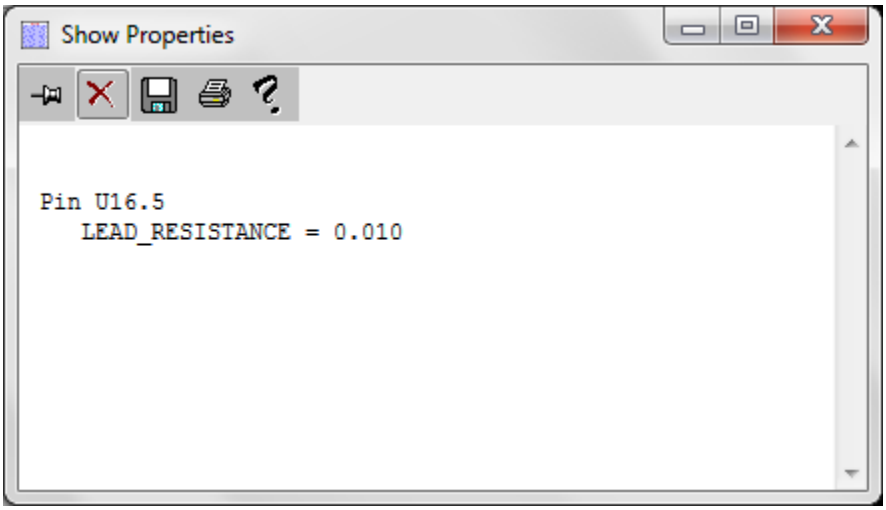
1. Choose *Edit – Properties* in PCB Editor and ensure that only the *Pins* check box is selected in Find Filter.
2. Click *More* and select *Property* in *Object type*.
3. Select `LEAD_RESISTANCE = 0.05` and click *OK*.

The Edit Property dialog appears. You can edit the property in this dialog.



4. On the right side of the Edit Property dialog, in the `Value` edit box for the `LEAD_RESISTANCE` property, type the value `0.010`, and click *Apply*.

   Note that the property value has changed in the Show Properties window.



5. Click *OK* to close the Edit Property window.
6. Save the board with the name `lead_resistance_changed.brd`.
7. Choose *Difference – Property Setup* in Design Differences.

   The Property Flow Setup dialog appears.

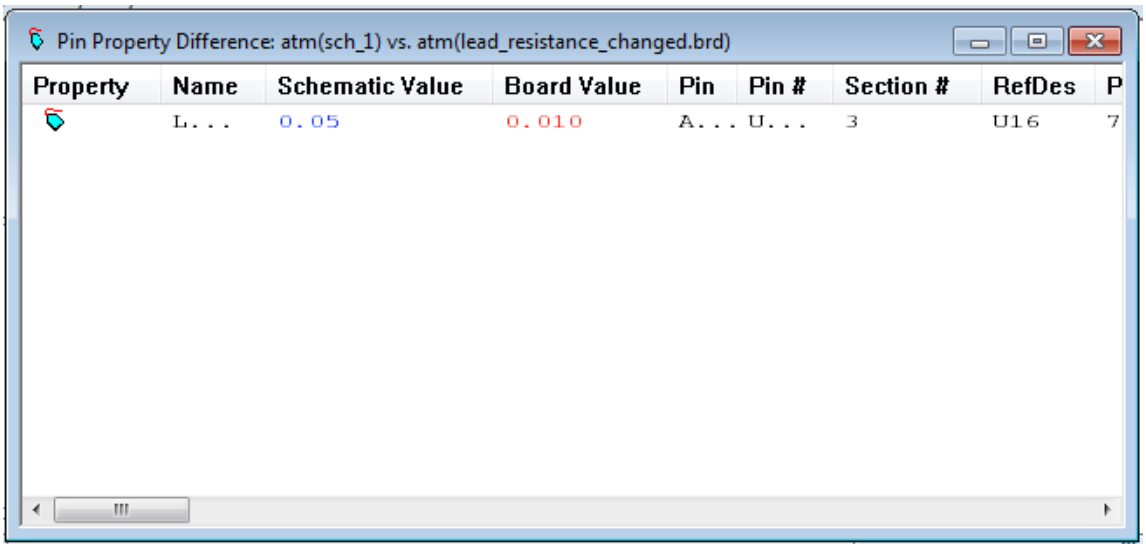
   If the `LEAD_RESISTANCE` property is not available in the properties list, click *Add* and define a new property named `LEAD_RESISTANCE` and define it as transferable between the schematic and the board.
8. Click *OK* to close the Property Flow Setup dialog, and click *OK* to close the message box.
9. Close Design Differences and open it again.
10. Select the `lead_resistance_changed.brd` board file in the *PCB Editor Board* field, ensure that the *Update package view before compare* check box is selected, and click *OK* to proceed.

    The Export Physical dialog appears with the *Package Design* check box selected.
11. Click *OK.*

    A progress window appears with the information that the design is netlisted and being fed back. Finally a message box appears prompting you to see the results.
12. Click *No*.

    The Control is passed back to Design Differences, which displays a message log, the Constraints Differences, and the Pin Property Difference windows.

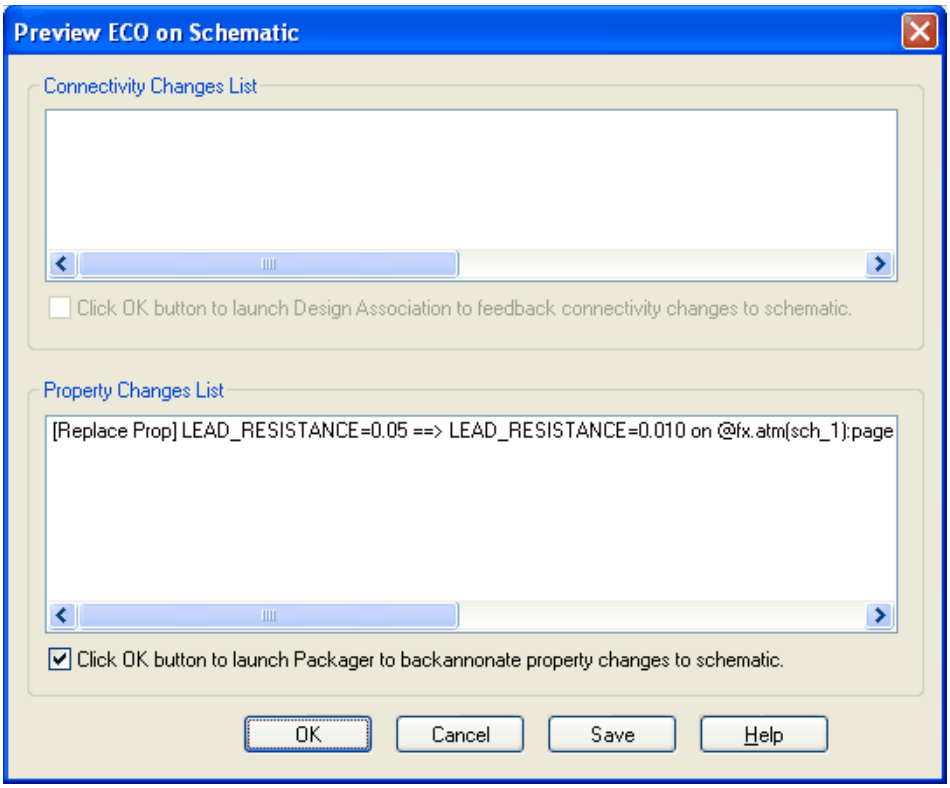
The Pin Property Difference window shows that the value of the `LEAD_RESISTANCE` property on the board is `0.010`, while the value on the schematic is `0.05`.



13. Choose *Sync – Update Design Entry HDL Schematic* in Design Differences.

The Preview ECO on Schematic dialog appears.

Figure 7-6 Preview ECO on Schematic Dialog



14. Click *OK* to update the schematic.

The message log in the Design Differences window is updated and the Import Physical dialog appears.

15. Click *OK*.

A Progress Window appears mentioning that design is netlisted and being fed back. Finally a message box appears prompting you to see Packager results.

16. Click *No*.

The control is passed back to Design Differences, which displays a message that the schematic has successfully loaded.

17. Click *OK*.

Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Design Entry HDL schematic.

18. Select *Difference – Pin Property* to check whether there are differences between the schematic and the `lead_resistance_changed.brd` board file.

A message box appears confirming that there are no differences.

19. Click *OK* to close the message box.

20. Open the Design Entry HDL schematic to confirm visually that the schematic has been updated.

21. Choose *File – Exit* in Design Differences, PCB Editor, Design Entry HDL, and Project Manager. Do not save any changes.

8

Handling Bypass Capacitors

Objective

To view netlist differences that are caused by adding new components and to update the schematic with the differences

At the end of this chapter, you will be able to:

- Use Design Differences to view differences caused by the addition of bypass capacitors.
- Use Design Association to migrate connectivity changes to the schematic.

Viewing Connectivity Differences

Task Overview

You will open the `atm.cpm` file in the `des_demos/bypass_caps/hdli` directory in Project Manager, and view the schematic in Design Entry HDL and the board in PCB Editor. First, compare the differences between the schematic and the `sync.brd` file. Next, compare the differences between the schematic and the `bypass_cap.brd` file.

Steps

1. Load the `atm.cpm` file located in the `des_demos/bypass_caps/hdli` directory in Project Manager.
2. Click *Design Entry* to open the schematic in Design Entry HDL.
3. Choose *Tools – Design Differences* in Design Entry HDL.

   The Design Differences dialog appears.
4. Select `sync.brd` as the board.

5. Clear the *Update package view before compare* check box.
6. Click *OK* to start Design Differences.

   A message log and the Constraints Differences - Physical window are displayed.
7. Select *Difference – Instance* to check whether there are differences between the schematic and the board (`sync.brd`).

   A message box appears confirming that there are no differences.
8. Click *OK* to close the message box.

   You will now compare whether differences exist between the schematic and the `bypass_cap.brd` file.
9. Click the *Layout* button in Project Manager to launch PCB Editor.
10. Choose *File – Open* in PCB Editor and load the `sync.brd` board file. If you zoom in, you will note that there is only one capacitor—`CAP1`.

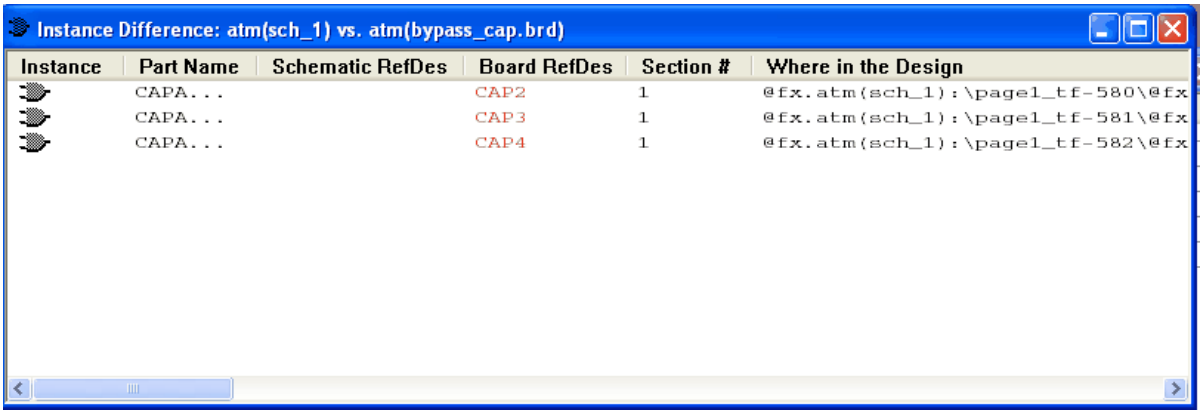
    Choose *File – Open* in PCB Editor and load the `bypass_cap.brd` board file.

    If you search for capacitors in this board, you will find that there are four capacitors, named `CAP1`, `CAP2`, `CAP3`, and `CAP4`, placed on the lower middle part of the board. The capacitors are connected between `VCC` and `GND`.
11. Choose *File – Load PCB Editor Board* in Design Differences, and select the `bypass_cap.brd` board file in the Select Board File to Compare dialog box.

    A message reports the successful loading of the board file.
12. Click *OK* to proceed.

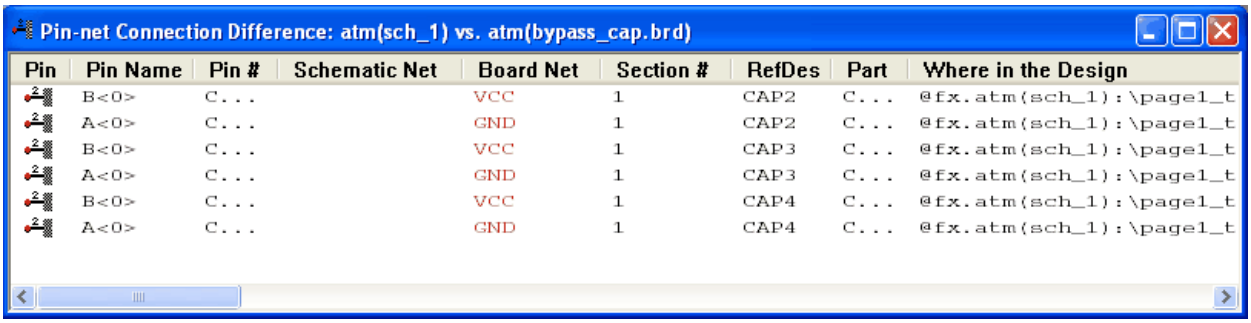
    A message log and the Instance Difference and Pin-net Connection Difference windows appear.

Figure 8-1 Instance Difference Window



The Instance Difference window lists `CAP2`, `CAP3`, and `CAP4` as extra instances in the board. The components available on the board are shown in red. The field below the *Schematic RefDes* is empty, which indicates that these components are not available on the schematic.

Figure 8-2 Pin-net Connection Difference Window



The Pin-net Connection Difference window lists the differences in the pin-net connections in the schematic and the board. Differences exist for pin names `A<0>` and `B<0>`. The Pin-Net Connection Difference window shows the nets that are connected differently from the schematic. There are six rows for the six new pin-net connections.

13. Choose *File – Exit* to close PCB Editor.

Writing the Marker File

Task Overview

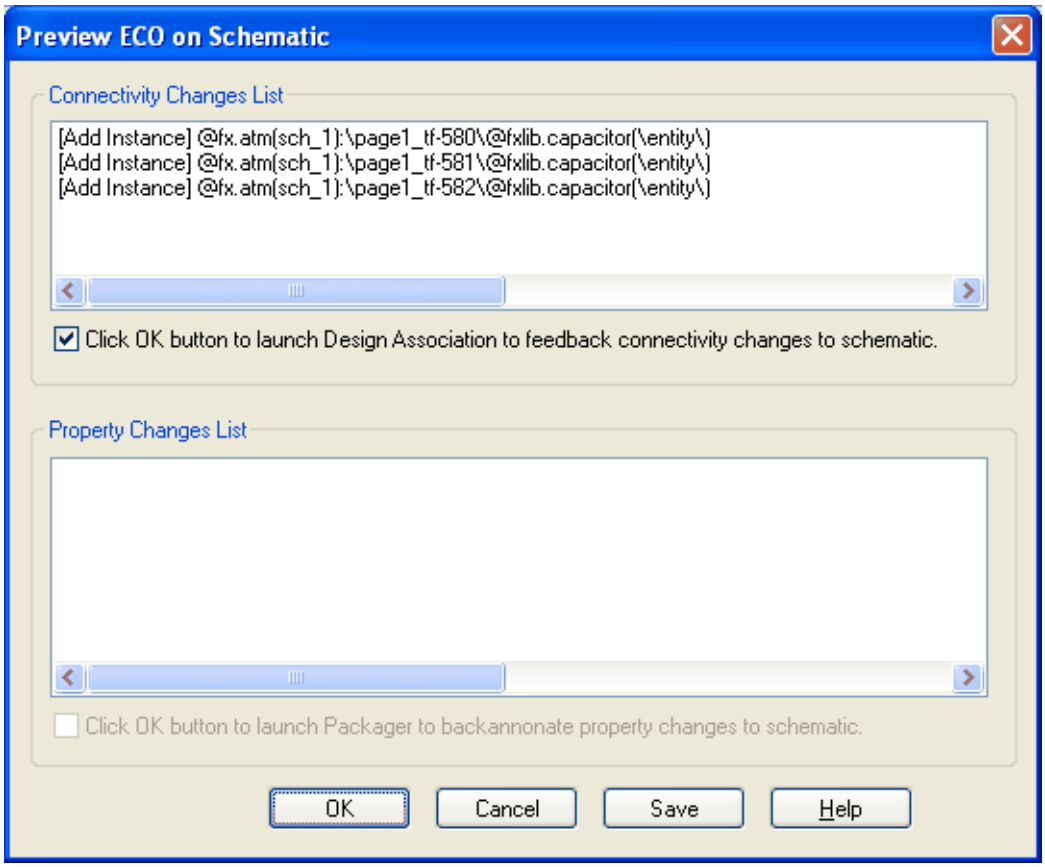
You will write the connectivity changes in a file called `dessync.mkr`. Design Association uses this file to update the Design Entry HDL schematic.

Steps

1. Choose *Sync – Update Design Entry HDL Schematic* in Design Differences to launch the Preview ECO on Schematic dialog.

   The Preview ECO on Schematic dialog appears.

Figure 8-3 Preview ECO on Schematic Dialog

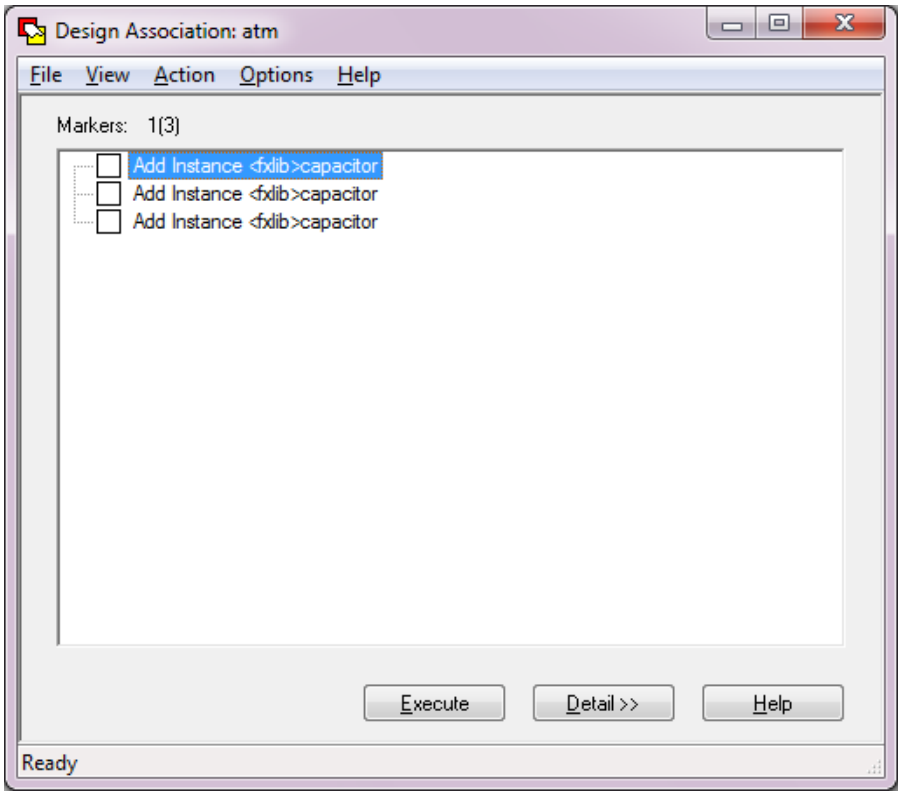


Note that the top section of the dialog shows the changes that are needed in the schematic. This section shows that three actions require the addition of an instance to the schematic.

2. Click *OK*.

   Design Association appears with the marker file loaded. See figure 8-4. Note that the three actions that need to be executed are shown in three lines.

Figure 8-4 Design Association



3. If you want to see the components in the schematic and the board, you can do the following:

   - Choose *Explore – Logical Design* in Design Differences to display the schematic view.

     The Schematic View window appears. Note that the total number of components is 30.

   - Choose *Explore – Physical Design* to display the schematic view.

The Board View window appears. Note that the total number of components is 33. You can explore both the logical design and physical designs from Design Differences.

4. Choose *File – Exit* to close Design Differences.

Updating the Design Entry HDL Schematic Using Design Association

Task Overview

You will use Design Association to update the Design Entry HDL schematic with connectivity.

Steps

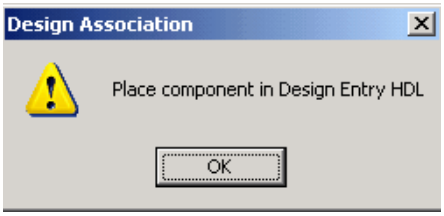
1. Select the first marker.

   Note that the number of the action selected is shown on the window in the format `Markers: 1(3).`

2. Click *Execute*.

   The Design Association box appears and you are prompted to place the component in Design Entry HDL.

Figure 8-5 Design Association Message Window



3. Click *OK*.

   The Design Entry HDL window is now active and a component is attached to the cursor in an `add component` operation.

4. Click in an empty location on the schematic to place the component.

   When you place the component, signal names are automatically attached to the pins.

5. Zoom in to the location to view the signal names.

   A blue cross is placed in the Design Association window against the action to indicate that the action has completed successfully.

6. Choose *Text – Attributes*, and select the capacitor.

7. Set the value to `50nf`.

   Note that the location property is set to `CAP2`.

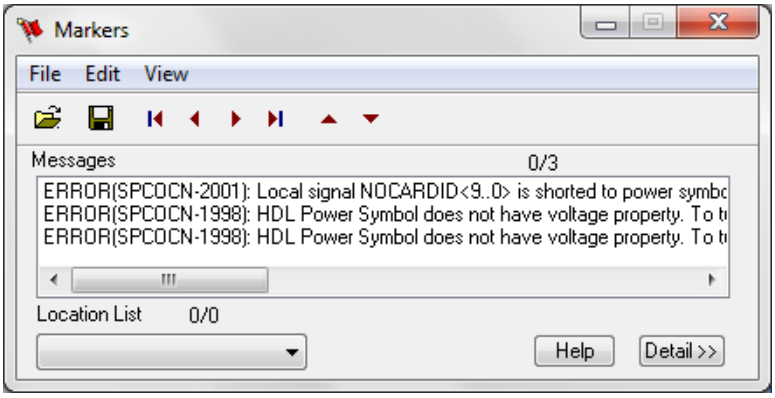
8. Click *OK* to close the attribute window.

9. Repeat steps 2-9 to place the other two capacitors on the Design Entry HDL schematic. Set the value of both capacitors to `50nf`.

   Note: You need to assign values to the capacitors because you cannot save the schematic until all the markers are assigned values.

10. Choose *File – Save* to save the schematic.

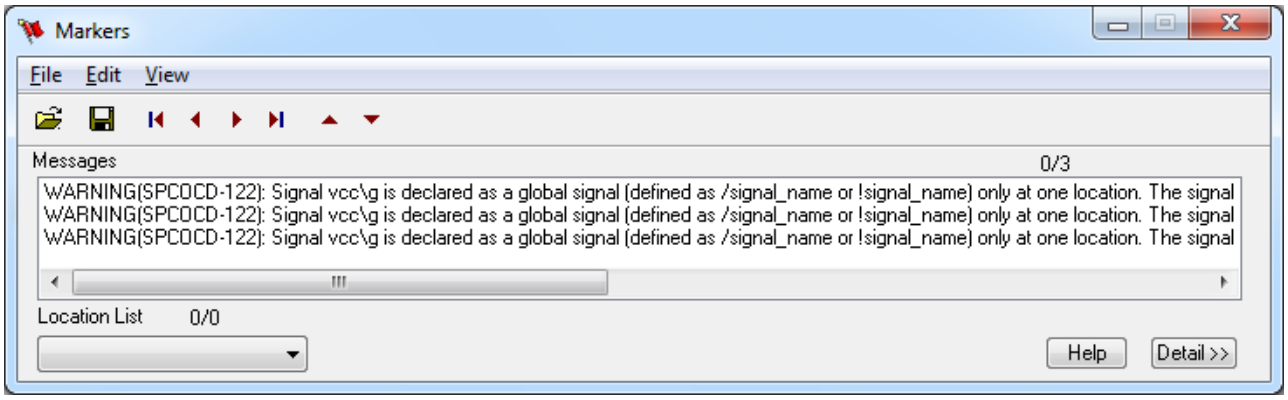
    A message box indicating that there are three errors will pop up. You can click on *View Errors* to view the error details:



11. Ignore the errors and click *Save* in the Design Entry HDL message box.

    When you click Save, a message box may pop up prompting you to view netlisting warnings.

Click *No* in the netlisting warning message box. If you want to view the errors, you can click on *View Errors* to view the warnings:



12. Choose *File – Export Physical* to package the design.

    The Export Physical dialog appears.

13. Select the *Package Design* check box.

14. Select the *Preserve* option.

15. Select the *Update PCB Editor Board (Netrev)* and *Backannotate Packaging Properties to the Schematic Canvas* check boxes.

16. Ensure that the input and output board files are `bypass_cap.brd`.

17. Click *OK* to package the design.

    A progress window appears. When the design is packaged, a window appears with the information that packaging was successful and prompts you to check the results.

18. Select *No*.

19. Select *Tools – Design Differences* in DE HDL.

    The Design Differences dialog appears.

20. Ensure that only the *Update board view before compare* check box is selected.

21. Click *OK.*

    A message log, and the Instance Difference and Pin-net Connection Difference windows appear.

22. Select *Difference – Instance* in Design Differences to check whether there are differences between the schematic and the board.

A message box appears confirming that there are no differences.

23. Choose *File – Exit* in Design Differences, PCB Editor, Design Entry HDL, and Project Manager. Do not save any changes.

9

Handling Series Terminators

Objective

To view netlist differences caused by the addition of series terminators and how the differences are updated to the schematic

At the end of this chapter, you will be able to:

- Use Design Differences to view differences caused by the addition of series terminators.
- Use Design Association to update the addition of series terminators in the board back to the schematic.

Viewing Connectivity Differences Caused by Series Terminator Additions

Task Overview

You will open the `atm.cpm` file in the `des_demos/series_term/hdli` directory in Project Manager, and view the schematic in Design Entry HDL and the board in PCB Editor. First, compare the differences between the schematic and the `sync.brd` file. Next, compare the differences between the schematic and the `ser_term.brd` file.

Steps

1. Load the `atm.cpm` file located in the `des_demos/series_term/hdli` directory in Project Manager and launch Design Entry HDL from Project Manager.
2. Choose *Tools – Design Differences* in Design Entry HDL.

   The Design Differences dialog appears.
3. Select `sync.brd` as the board.

4. Clear the *Update package view before compare* check box.
5. Click *OK*.

   A message log and the Constraints differences - Physical window appear.

   Select *Difference – Instance* to check whether there are differences between the schematic and the board (`sync.brd`).

   A message box appears confirming that there are no differences.

   You will now compare whether differences exist between the schematic and the `ser_term.brd` file.
6. Click the *Layout* button in Project Manager to launch PCB Editor.
7. Choose *File – Open* in PCB Editor and load the `sync.brd` board file.

   Note that there is only one capacitor, called `CAP1`, placed on the lower middle part of the board.
8. Choose *File – Open* in PCB Editor and load the `ser_term.brd` board file.

   Note that there is a component called `TERM2` placed on the lower middle part of the board.

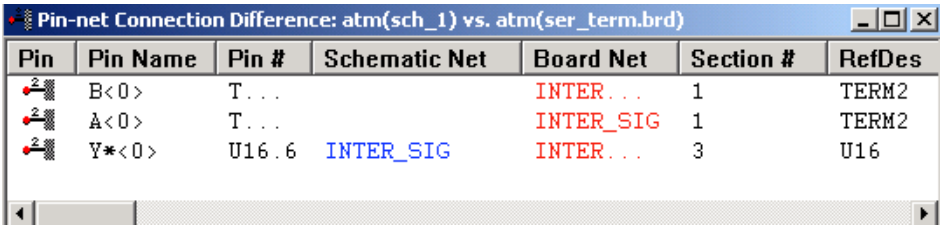
   This component is a series terminator on the net `INTER_SIG`. One end of the resistor is attached to the pin `U16.6` and the other end is attached to the pin `U16.9`.
9. Choose *File – Load PCB Editor Board* in Design Differences, select the `ser_term.brd` board file in the Select Board File to Compare dialog box and click *OK*.

   A message box reports that the board has been loaded. Click *OK*.

   A message log, and the Pin-net Connection Difference, Net Difference, and Instance Difference windows display.

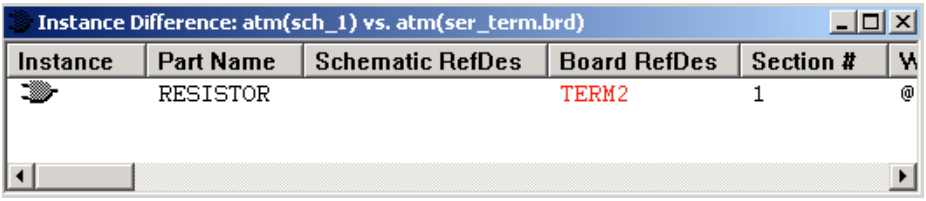
   The Pin-net Connection Difference window shows the difference caused by the addition of the series terminators.

Figure 9-1 Pin-net Connection Difference Window



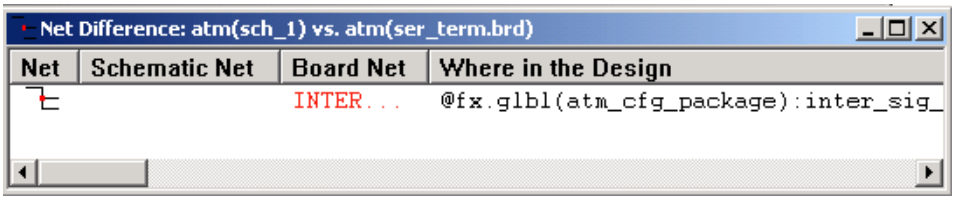
The Instance Difference Window shows that the board has one component that is not on the schematic.

Figure 9-2 Instance Difference Window



The Net Difference Window shows that the board has one component that is not present on the schematic.

Figure 9-3 Net Difference Window



10. Choose *File – Exit* to close PCB Editor.

Synchronizing Series Terminator Additions in the Schematic

Task Overview

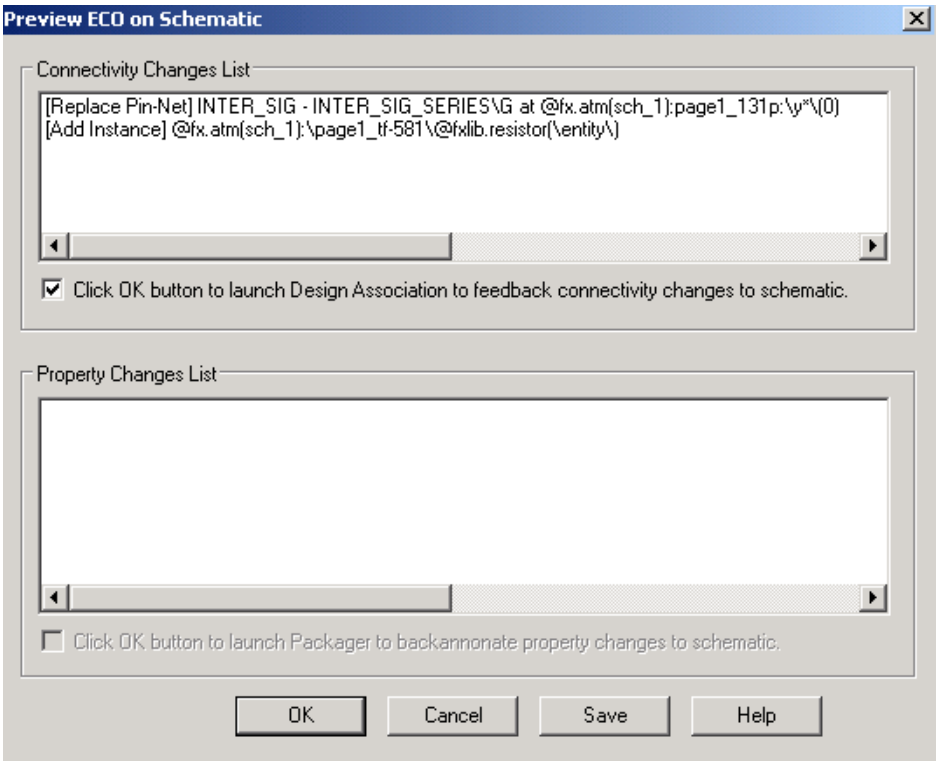
You will use Design Association to synchronize the schematic with the changes caused by the addition of series terminators in the board.

Steps

1. In Design Difference, choose *Sync – Update Design Entry HDL Schematic* to display the Preview ECO window.

Figure 9-4 appears. The top section of the Preview ECO on Schematic dialog shows the changes that need to be carried out in the schematic. Note that the action involves adding an instance to the schematic.

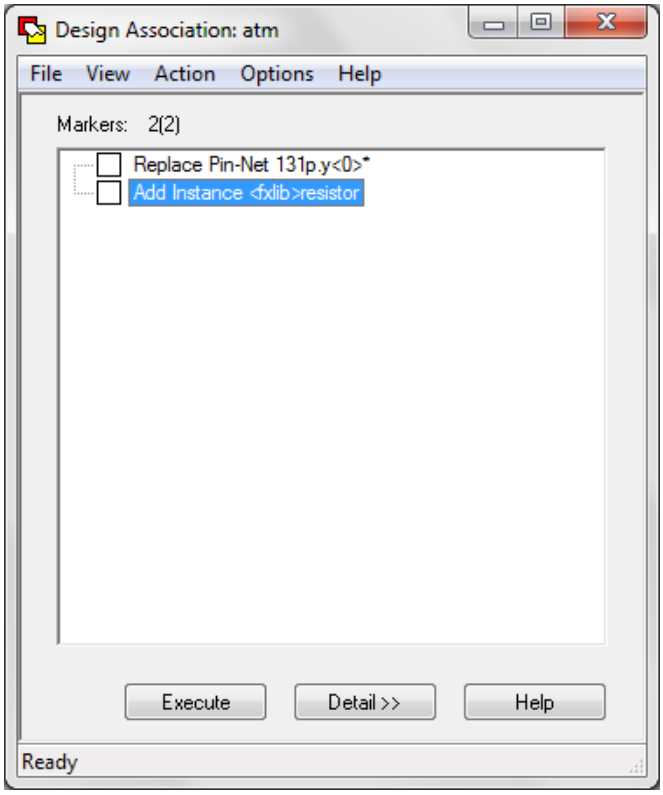
Figure 9-4 Preview ECO on Schematic Dialog



2. Ensure that the *Click OK button to launch Design Association to feedback connectivity changes to Schematic* box is checked.
3. Click *OK*.

   The Design Association window displays with the correct marker file.

Figure 9-5 Design Association



4. Select *Add Instance <fxlib>resistor* and click *Execute* to add the resistor in Design Entry HDL.

   A message box appears prompting you to place the component in Design Entry HDL.

5. Click *OK*.

   As soon as you click on Execute, a resistor is attached to your cursor. You need to now place this resistor on the schematic in a similar manner as it is placed on the board.

6. Place the resistor on the wire with the `INTER_SIG` signal.

Tip

To locate the wire easily, you can perform a search for the INTER_SIG signal in Design Entry HDL.

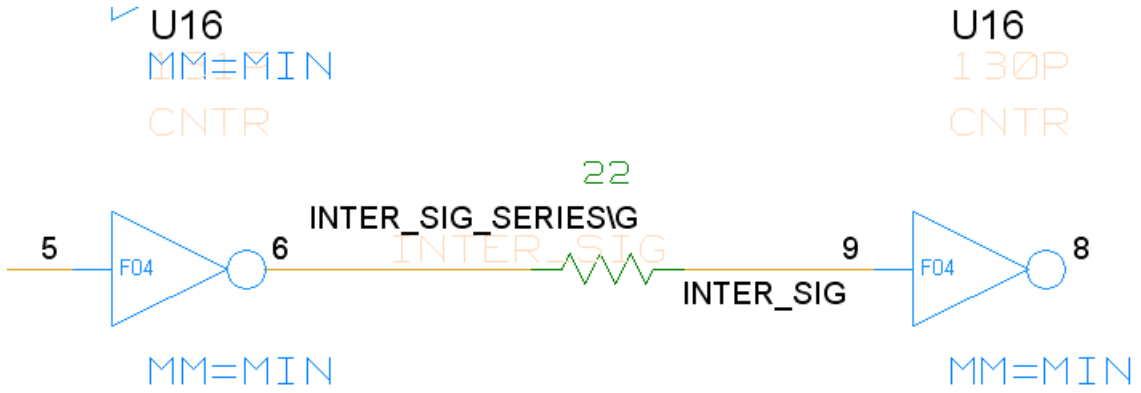
Figure 9-6 Design Entry HDL Design Before Execution of Action

The resistor is embedded into the wire like in the board.

Caution

Place the resistor as shown in the following figure. If not, design differences between the schematic and the board might result.

Figure 9-7 Design Entry HDL Design After Execution of Action



1. Choose *File – Save* to save the schematic.

   A message box indicating three errors may appear. You can ignore these errors.

2. Choose *File – Export Physical* to package the design.

   The Export Physical dialog appears.

3. Select the *Package Design* option.

4. Set the packaging option to *Preserve.*

5. Clear the *Update PCB Editor Board (Netrev)* and *BackAnnotate Packaging Properties to Schematic Canvas* check boxes.

6. Click *OK* to package the design.

   A progress window appears stating that packaging has finished successfully and asks if you want to check the results.

7. Select *No* to close the window.

8. Choose *File – Exit* in Design Differences, Design Association, PCB Editor, Design Entry HDL, and Project Manager. Do not save any changes.

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