cadence®

Allegro Design Entry HDL Known Problems and Solutions

Product Version 23.1

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Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Contents

Design Entry HDL Known Problems and Solutions

Allegro® Design Entry HDL known problems and solutions (KP&S) will be reviewed at regular intervals and updated when new issues arise. Up-to-date known problems and solutions are published on Cadence Online Support.

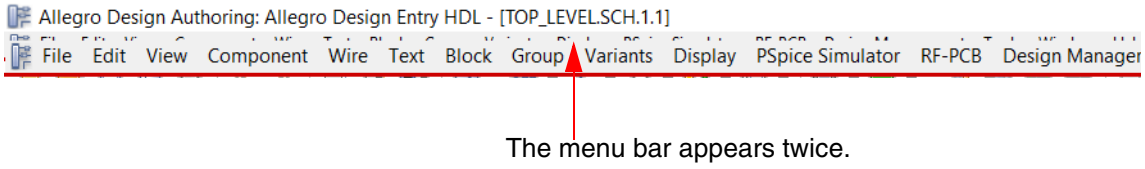
Status of Problems Reported in Earlier Releases

The following problems reported in previous releases are valid for 23.1 as well:

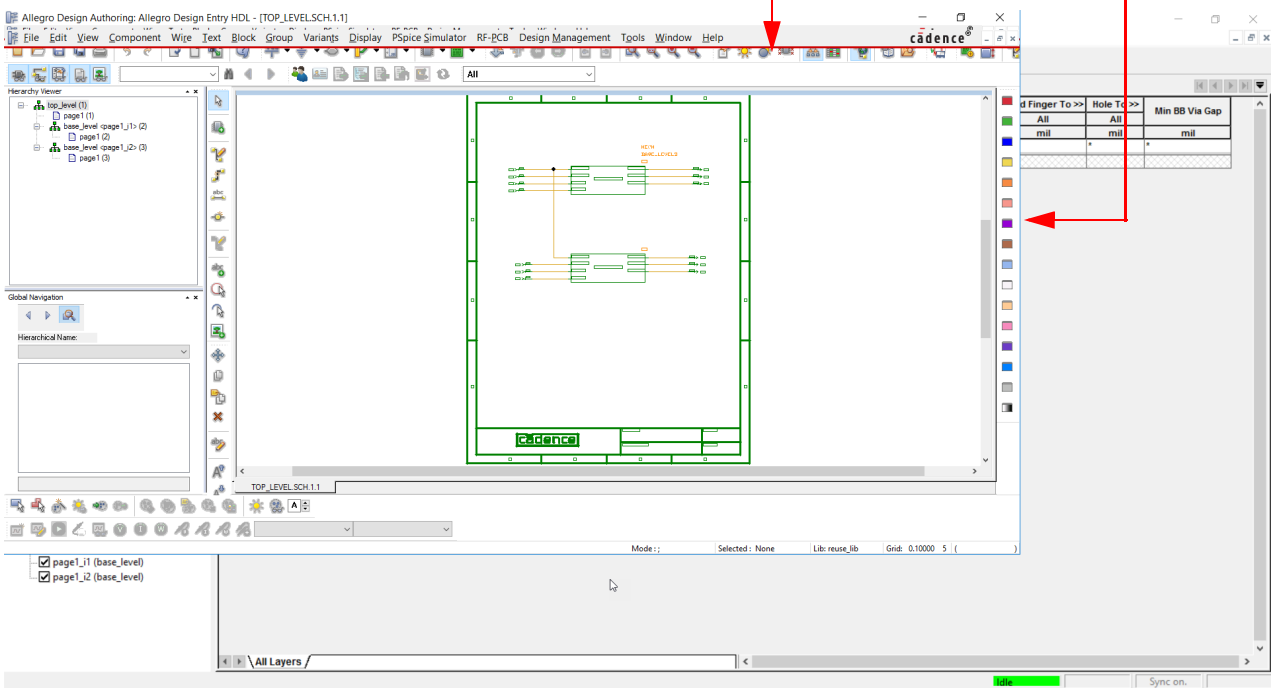
CCMPR01822494: DE-HDL-Constraint Manager on Windows 10 machines with Intel graphic cards might have display issues

Description: When Constraint Manager is launched from DE-HDL on Windows 10 machines with Intel graphic cards, you may observe some display issues. In DE-HDL for example, the menu bar appears twice and the size of the menu bar and icons reduces. In Constraint Manager, the font size of the menu bar increases, a distorted menu bar might sometimes be displayed and some dialogs show text with a higher resolution.

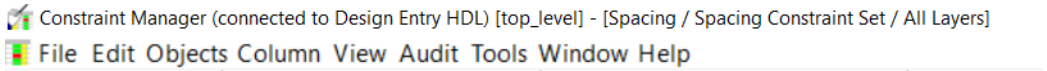
In the DE-HDL window



The size of the menu bar and icons reduces.

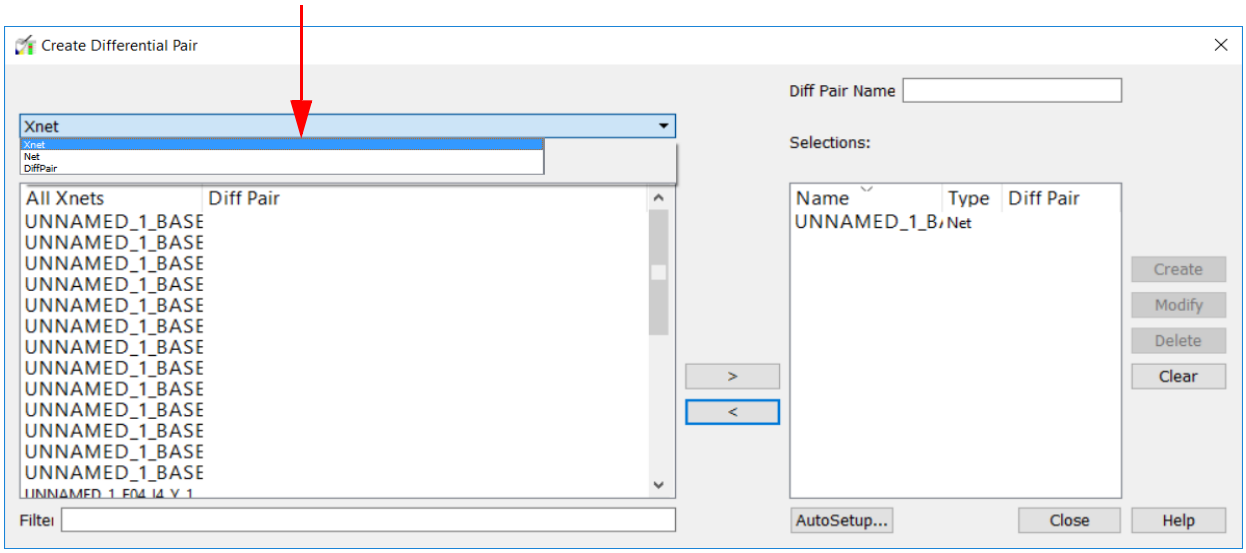


In the Constraint Manager window



The font size of the menu bar increases and a distorted menu bar might sometimes be displayed

Some dialogs show text with a higher resolution.



Solution: To fix this issue, do the following:

1. Close Constraint Manager and DE-HDL.
2. Click *Start* and choose *Cadence Release 17.2-2016*.
3. Right-click on *Design Entry HDL*.
4. Choose *More — Open file location*.
5. Right-click on *Design Entry HDL* and select *Properties*.
6. In the Design Entry HDL Properties dialog, click the *Compatibility* tab and select the *Disable display scaling on high DPI settings* check box.
7. Click *OK*.
8. Restart DE-HDL and launch Constraint Manager.

CCMPR00885839: Modeless: Voltage property lost on delete instead of rippling the original value

Description: Editing the voltage on a global net and then deleting the voltage on one of the nets, leads to voltage loss. For instance, consider that you have a simple design with two peer blocks MID and BLOCK1. A global signal runs through both MID and BLOCK1. Go to the MID block and edit the voltage, and save the design. You will notice that this edit change is

reflected in both the blocks. Now, delete this value in MID. Save the design again and package it. You will notice that after packaging, the voltage is lost in the other block too.

Solution: Add VOLTAGE on that net again in either the block or in the root design.

CCMPR00850625: Modeless: Multiple properties are not editable and are not visible in Show index

Description: Multiple properties cannot be edited at a time in the Show index mode. For instance, add two properties on a bus and save the design. Choose the Show index mode and edit the values of both properties. Save the design. On reopening the design, only the last edit is retained. Change it back to global bus, and the property is not visible.

Solution: You can only add, delete, and edit one property at a time. For instance, if you want to change the values of the properties on a bus, edit the value of one property and save the design. Then reopen the design and edit the value of a second property and save the design again. On reopening the design, Show index will be updated with the new values.

CCMPR00788708: Netlisting errors are not highlighted when the design is upreved

Description: Netlisting errors that are reported while upreving a design are not highlighted. When you view the errors from the marker file, and highlight the errors, the marker does not point to the location of the netlisting errors.

Solution: None

CCMPR00689398: Wire line is missing after RF PCB import

Description: If two components are placed in close proximity or if there is another wire placed very close to the pin, DE-HDL attaches the SIG_NAME property to the pin when the schematic is updated because there is not enough space to draw a wire. As a result, the schematic seems to have missing pin connections after RF PCB import.

Solution: In this case, though the schematic connectivity is correct, you might want to manually draw a wire to the pin after RF PCB import.

CCMPR00682028: Alignment: Object overlap is not detected

Description: The alignment operation does not detect whether objects overlap post-alignment.

Solution: None

CCMPR00694930: DE-HDL selecting net name based on vectored boundary even after enabling font support

Description: On enabling font support, the boundary box of a net name in a vector font is reduced. When you hover the mouse pointer over the area where the original boundary box existed in a vector font, the complete net name is shown and the net name is selected when you click on it even though the original boundary of the net name is reduced.

Solution: None

CCMPR00673443: LDDP and MDDP names should not be annotated on schematic

Description: If you have `DIFFERENTIAL_PAIR` placeholders on schematic, the Library-Defined Differential Pair (LDDP) and Model-Defined Differential Pair (MDDP) names are annotated on the schematic.

If you rename the LDDP or MDDP name on the schematic, it is not updated in Constraint Manager.

Solution: Do not annotate or rename LDDPs or MDDPs on the schematic.

CCMPR00685098: Properties that are changed cannot be restored by using the Restore Backup option

Description: Properties are annotated through the traditional import physical flow. Backup is not done for pages that have only property updates as the RF import flow only keeps a backup of pages that have undergone connectivity changes. As a result, these pages are not restored when restoring the backup.

Solution: When you update properties on a schematic and want to restore the changes, you need to re-import the old version of the board to restore the existing values on the schematic.

CCMPR00679260: Restoring block does not restore the differential pair names from the lower block

Description: If you rename a lower-level block's differential pair in the top-level design, and restore it from its definition, the differential pair name is not restored from the lower-level block.

Solution: By default, the *Restore* command does not rename a block. To change the default behavior, set the environment variable `CM_MERGE_RENAME` to `TRUE`.

CCMPR00603112: Default Physical and Spacing Csets are not created in Constraint Manager connected to Design Entry HDL and System Connectivity Manager on importing a cross-section only technology file.

Description: A technology file must contain cross-sections and at least one Physical and Spacing CSet to be used in the front-end flow. For example, if you export a technology file from the board which has only cross-sections, it means the technology file only contains layer information and no Physical and Spacing Csets. When you create a design and import that technology file in Constraint Manager, the layers are visible but you cannot create any Physical or Spacing Csets.

This is a current limitation in the Design Entry HDL - Constraint Manager flow.

Note: This problem is not there in the Allegro PCB Editor - Constraint Manager because it always contains default CSets.

Solution: You must use a technology file with at least one Physical and Spacing CSet to use it in the front-end flow.

CCMPR01517312: When archiving or copying a project that has been enabled for design management, the project state is changed to read only

Description: When you archive a design or copy a project, the design becomes a read-only project; it should be writable.

Solution: None

CCMPR00604263: Copying and pasting a TOC component on a schematic shows existing TOC entries in the pasted TOC component.

Description: When you instantiate a TOC component in a schematic, the table of contents is populated with the relevant entries. If you copy this instantiated component and paste it anywhere on the schematic, the existing TOC entries are also copied. As a result, the entries in the originally placed TOC component are displayed in the pasted component as well.

Solution: Do not copy and paste a TOC component on a schematic. Always instantiate the TOC component on the schematic using Component Browser.

CCMPR00305435: Some limitations in Constraint Manager connected to Design Entry HDL 15.7.

Problem 1:

Description: If a differential pair created in Constraint Manager and backannotated, and then deleted in Design Entry HDL it continues to appear in Constraint Manager on a subsequent launch of Constraint Manager.

Solution: Launch Constraint Manager once before deleting the differential pair from the schematic canvas.

Problem 2:

Description: If you are using the Allegro Design Entry HDL L (previously Studio) license and if the constraints view exists for a design, an error occurs when you run the *Export Physical* command in case the schematic canvas has pin-pair constraints.

Solution: Before you run the *Export Physical* command on a design while using the Allegro Design Entry HDL L (or Studio) license, run the following command:

```
concept2cm -proj <project_name>.cpm -export -forward -uprev
```

CCMPR00323630: A differential pair is not deleted on exiting Constraint Manager if the same differential pair is applied on more than two nets.

Description: Consider a case where a differential pair, let's say `DP1`, created on nets `NET1` and `NET2`, is also applied on nets `NET3` and `NET4` in a schematic. On launching Constraint Manager, you notice that the differential pair `DP1` is visible only on nets `NET1` and `NET2`. On exiting Constraint Manager when the constraints are synchronized between Constraint

Manager and the schematic, the differential pair `DP1` is not deleted from `NET3` and `NET4` in the schematic.

Workaround: Run *Update Schematic* to update the schematic.

CCMPR00327311: The Bookmark panel shows the complete hierarchy even for a single page of a PDF document.

Description: Bookmarks in a published PDF document of a design appear for all the pages regardless of the *Page Range* option you select for PDF generation. Therefore, even if you publish only the currently active schematic page as a PDF document, the published document shows complete design hierarchy in the Bookmark panel.

Solution: None

CCMPR00270476: Sized devices cannot be extracted into Signal Explorer

Description: If a design contains a sized device and you try to extract a net which is connected to the sized device, only one instance of the device is shown in the Signal Explorer canvas.

Solution: None

CCMPR01514113: Signal models assigned to components in read-only blocks are lost after relaunching DE-HDL

Description: If you assign signal models to components in read-only blocks that are not assigned to you, signal models are assigned to these components in the in-context mode. You can save the design after the signal models are assigned. However, on launching DE-HDL again, the signal model assignment is lost.

Solution: None

Problem: FLEXID dongle 9 is not recognized on X86_64 or EM64T systems

Description: A FLEXID dongle 9 is not recognized on X86_64 or EM64T systems after you install the dongle driver with Macrovision's `FLEXidInstaller.exe v10.0.0.159` driver installer and reboot the system.

Solution: Install the more recent HASP4 device driver, which you can download from `http://www.aladdin.com/support/hasp/hasp4/enduser.asp`.

CCMPR00208971: Plots taken in opf will not print the packaged pin-pair values

Description: If you add a logical pin-pair in a lower-level block making it the root design, it appears in both the `.dcf` and the `.opf` files. Later, if you place the block in a top-level design and launch Constraint Manager, the pin-pair appears correctly with the updated pin name with a suffix added to the existing pin-pair name. When you package the design, the pin-pair is changed with packaged data.

However, the Attributes form continues to show the logical pin-pair coming from the `.opf` file of the lower-level block. You cannot see the updated pin-pair on the schematic canvas or the Attributes form in Design Entry HDL.

Solution: None

Solution: For cells containing blank spaces in the primitive names, recreate the metadata using the SPB 15.5 hierarchy.

CCMPR00217887: Match group inheritance becomes overridden for bits

Description: In Constraint Manager connected to Design Entry HDL, if units are set to `mils` and you specify the value in `microns`, the value is converted to `mils` before getting written to the schematic. When the next time you launch Constraint Manager, the value will be overridden by the value in the schematic.

Solution: None

CCMPR00219676: Pin-pair with driver in top-level and receiver in lower-level block is removed

Description: If you open a pre-15.5 hierarchical design in Design Entry HDL 15.5 which contains a pin-pair with the driver in the top-level design and the receiver in the lower-level block and the pin-pair annotated on a net in the lower-level block, the pin-pair will be removed.

Solution: None

CCMPR00225478: Image getting distorted after insert in HP

Description: If you insert a 32-bit image on the schematic canvas on an HP system with a display setting of 256 colors, the image is distorted.

Workaround1: Before inserting an image on the schematic, open it once in image editor and save in the `.gif` format.

Workaround2: Change the display settings on the system by changing the depth value to 24 to view the plot correctly. Use the following command to modify the depth setting on system:

```
sudo /usr/sbin/m64config
```

Usage:

```
m64config [-dev devname] [-file machine | system][-res video-mode [now] [noconfirm]
[nocheck] [try]] [-depth 8|24|32] [-defaults] [-propt] [-prconf] [-help]
```

Note: You will need the root access to modify the depth value.

RF-PCB Known Problems and Solutions

RF-PCB known problems and solutions (KP&S) will be reviewed at regular intervals and updated when new issues arise. Up-to-date known problems and solutions are published on Cadence Online Support.

Status of Problems Reported in Earlier Releases

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CCMPR00685098: Properties that are changed cannot be restored by using the Restore Backup option

Description: Properties are annotated through the traditional import physical flow. Backup is not done for pages that have only property updates as the RF import flow only keeps a backup of pages that have undergone connectivity changes. As a result, these pages are not restored when restoring the backup.

Solution: When you update properties on a schematic and want to restore the changes, you need to re-import the old version of the board to restore the existing values on the schematic.

CCMPR00690301: IC and discrete insertion in the layout causes RF PCB Import flow to abort

Description: The RF Import flow supports insertion and deletion of RF components in the layout. Inserting or deleting non-RF components, such as ICs and discrete components, is not supported.

Solution: Use the Design Association flow. RF Import flow will only update the connectivity of the discrete and pins of IC that form part of the RF topology.

Variant Editor Known Problems and Solutions

Variant Editor known problems and solutions (KP&S) will be reviewed at regular intervals and updated when new issues arise. Up-to-date known problems and solutions are published on the *Cadence Online Support* website.

Status of Problems Reported in Earlier Releases

The following problems reported in previous releases are valid for 23.1 as well:

CCMPR01100481: Global Quick Find feature is not working for variant views

Description: Variant-specific properties are not located by the Find feature when you perform a search for:

- a design object with the *look in Design* option selected.
- *Components* and *Properties*, or *Nets* and *Properties*.

This is because variant-specific properties are not written to a `.dcf` file, which stores all the properties on components and nets in a base design.

Solution: None

CCMPR01115970: Issues in variant dynamic overlay functionality in team designing

Description:

When multiple users work on a design that has been enabled for team design, variants are not dynamically updated across different user sessions of DE-HDL. For example, if User1 adds new variants to a design, other users can view these variants in the Variant tab, only after closing and then reopening the design. Similarly, if a user adds or deletes pages in a particular block in the design, other users will need to re-launch DE-HDL to refresh all the variants.

Solution: None

Problem: Limitations in Replacing Component

Description: If you replace a component say `conn64`, with another component, for example `bnc_conn`, component `bnc_conn` has the following limitations:

- After backannotation the symbol is not replaced. After component `bnc_conn` replaces component `conn64`, the symbol of component `bnc_conn` continues to remain the same as that of component `conn64`.
- The properties of component `conn64` continue to exist in component `bnc_conn`. This means that component `bnc_conn` has its own properties, and those it acquires from component `conn64`.
- The reference designator of the replaced component `bnc_conn` is the same as the component replacing it, that is, `conn64`.
- When `bnc_conn` is placed on the board, its footprint remains the same as `conn64`.

Solution: None

Problem: Variant Editor is unable to backannotate components having the SIZE property.

Description: If you have `SIZEABLE` components on a design and use Variant Editor to backannotate to the design, Variant Editor will not backannotate the instances which have `SIZEABLE` components on a design.

Solution: None