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Topology Workbench Known Problems and Solutions

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Contents

Topology Workbench: Known Problems and Solutions

This document describes the known problems in Cadence® Sigrity™ Topology Workbench and suggests the corresponding workarounds. Each problem is identified by a Cadence Change Request (CCR) number.

Note: Unless otherwise stated, the problems described in this document were identified in a OrCAD® and Allegro® 23.1 release or a corresponding SIGRITY release. For information about problems that were fixed in this release, see the `README` file accompanying this release. You can read this file online at downloads.cadence.com.

For information about features of Topology Workbench, see *Topology Workbench User Guide* and *Topology Workbench Frequently Asked Questions*.

Incorrect simulation results produced in SystemSI for a non-standard IBIS-AMI model

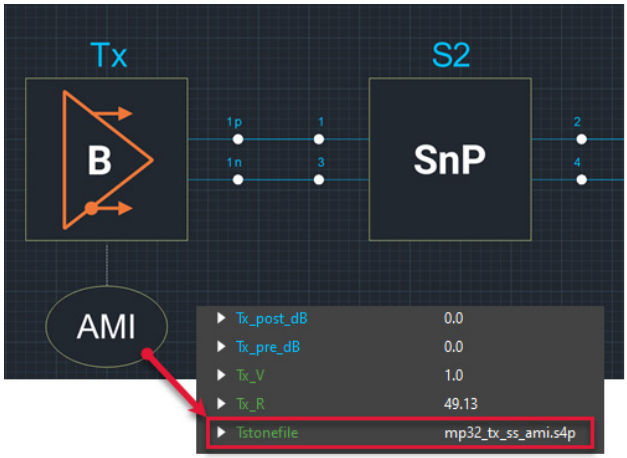
Problem: A non-standard IBIS-AMI model created by Synopsys (`synopsys_mp32_ibis_ami`) does not produce correct simulation results in SystemSI. This model can be identified by the following model-specific parameters:

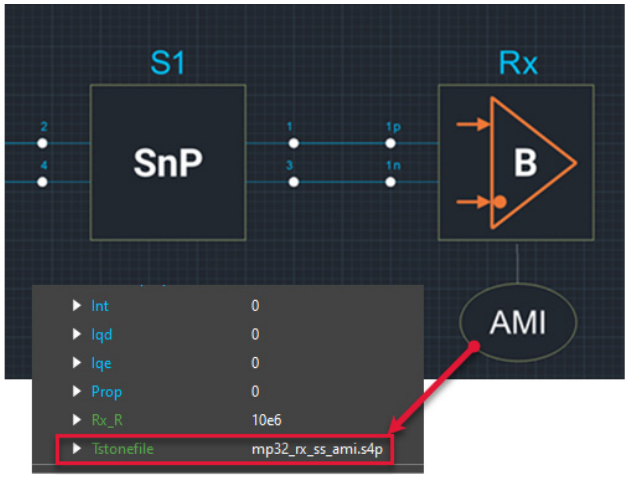
- 'Tstonefile' and 'Rx_R' in the Rx AMI model
- 'Tstonefile', 'Tx_V' and 'Tx_R' in the Tx AMI model

The model attempts to accomplish the functionality found in the IBIS-AMI standard 7.0 and later by the Reserved Keyword 'Ts4file'. It is noteworthy that so far, this model is simulated correctly only in the third-party tool ADS by Keysight.

Solution: Place the S Parameters indicated by the 'Tstonefile' into a *SnP* block and connect the block to the output of the Tx IBIS model and the input of the Rx IBIS model. Connect Ports

1 and 3 to the output pins of the Tx block and the input pins of the RX block. Refer to the images below for the connection details.





CCR 2353552: Allegro IDA Reflection should set default frequency to 50MHz

Problem: The current Allegro IDA default of 500MHz is way too fast to capture reflection data reliably.

A pulse stimulus is used in the IDA Reflection workflow to enable one simulation to produce results for rising and falling edges. To capture reflection measurements (for example, ring back, overshoot) cleanly, you need to have clear delineation between the rising and falling edges. This means that you want the rising edge to happen, cleanly settle out, and then have a falling edge. This allows the measurement algorithms to differentiate between the rising edge and the falling edge so that the high state and low state measurements can be taken reliably.

If the stimulus pulse frequency is too fast, you get inter-symbol interference (ISI) mixed in with the reflection effects, where the rising edge waveform features get mixed in with the falling edge features. This makes measurements much more difficult, and sometimes unreliable. The whole purpose of the Reflection simulation is to isolate the effects of reflections to enable the user to address them. Therefore, the ISI effects need to be kept out.

Solution: Click *Analysis Options* from the *Reflection* workflow and reduce the *Data Rate* setting to a value significantly slower, for example 50MHz. This typically allows sufficient settling time between the rising and falling edges at the receiver.

If you want to go to the next level of detail and look at the reflection and ISI effects together, use the *Topology Extraction* workflow, and extract the signal into Topology Workbench.

There you can use bit pattern stimuli to generate full eye diagrams that reflect the impact of both of these effects together.