cadence®

Topology Workbench: Topology Explorer Tutorial

Product Version 23.1
October 2023

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Contents

1

Topology Explorer Tutorial: An Overview

The Topology Explorer workflow of Topology Workbench is targeted for general-purpose signal integrity analysis, optionally including non-ideal power effects. You can include complex interconnect models and connect them to a single driver/receiver/discrete symbol that automatically replicates the circuit for each of the ports on the interconnect model. In addition to building custom system-level topologies, this workflow lets you run transient simulations.

In this tutorial, you will know how to use the Topology Explorer workflow of Topology Workbench to create and extract topologies for the critical nets in a PCB and derive Electrical Constraint Set (ECSet) using this topology to optimize the design.

This tutorial captures the step-by-step instructions on exploring the Topology Workbench canvas, creating a topology from scratch, doing pre-layout extraction and post-layout routed interconnect extraction, and updating the ECSet using Constraint Manager.

For detailed conceptual information, see the Using Topology Explorer Workflow chapter of the *Topology Workbench User Guide*.

Organization of this Document

Each chapter in this tutorial has been written to be a standalone module that covers specific tasks. Review the following chapters for the typical steps you will perform to create, edit, and simulate a parallel bus interface:

Chapter 1, “Topology Explorer Tutorial: An Overview”	
	This is the current chapter. It covers the basic overview of the Topology Explorer tutorial and the additional resources.
Chapter 2, “Getting Started with Topology Explorer”	
	Covers the introductory information about Topology Workbench and its interface. The chapter provides guidance on how to create a simple topology for the Topology Explorer workflow.

Chapter 3, “Pre-layout Extraction and Export of Topology Constraints”	
	Explains how to extract a topology from Constraint Manager on an unrouted board. In addition, the chapter covers how to use this topology to create a constraint set for the board.
Chapter 2, “Getting Started with Topology Explorer”	
	Explains how to extract a post-layout routed interconnect into Topology Workbench. In addition, the chapter covers how to use this topology to create a constraint set for the board.

Sample Test Case Files

The test case files provided along with this tutorial can be classified into two types: default templates and samples.

- The default template files for Chapter 2 are accessible from the Topology Workbench interface.
- The following sample files are available in the `<INSTALL_DIR>\share\topxp\Tutorials\SIE_Tutorial` directory:
  - `prelayout_Module1.brd` – physical layout file to be used in Chapter 3
  - `postlayout_Module1.brd` – physical layout file to be used in Chapter 4

Note: Instead of updating the files in the sample directory, it is recommended that you copy these files to your working directory and then work on them.

This tutorial document does not provide conceptual details or familiarity with different user interface elements. For such information, refer to the documents listed in the Related Documents section.

Related Documents

In addition to this tutorial, you can refer to:

- *Topology Workbench Frequently Asked Questions* to find answers to a few commonly encountered questions.
- *Topology Workbench User Guide* for detailed procedural information related to the Topology Explorer, Parallel Bus Analysis, Serial Link Analysis, AMI Builder, and Compliance Kits workflows of Topology Workbench.

- *Topology Workbench: Parallel Bus Analysis Tutorial* covers typical steps you will perform to create, edit, and simulate a parallel bus interface by using a default template from the install hierarchy and by creating a topology from scratch.

Additional Learning Resources

Cadence offers training courses that enable you to understand the applications better. For specific information about the courses available in your region, visit Cadence Training or write to training_enroll@cadence.com.

Note: The links in this section open in a separate web browser window when clicked in Cadence Help.

Customer Support

For assistance with Cadence products:

- Contact Cadence Customer Support

  Cadence is committed to keeping your design teams productive by providing answers to technical questions and to any queries about the latest software updates and training needs. For more information, visit: https://www.cadence.com/support

- Log on to Cadence Online Support

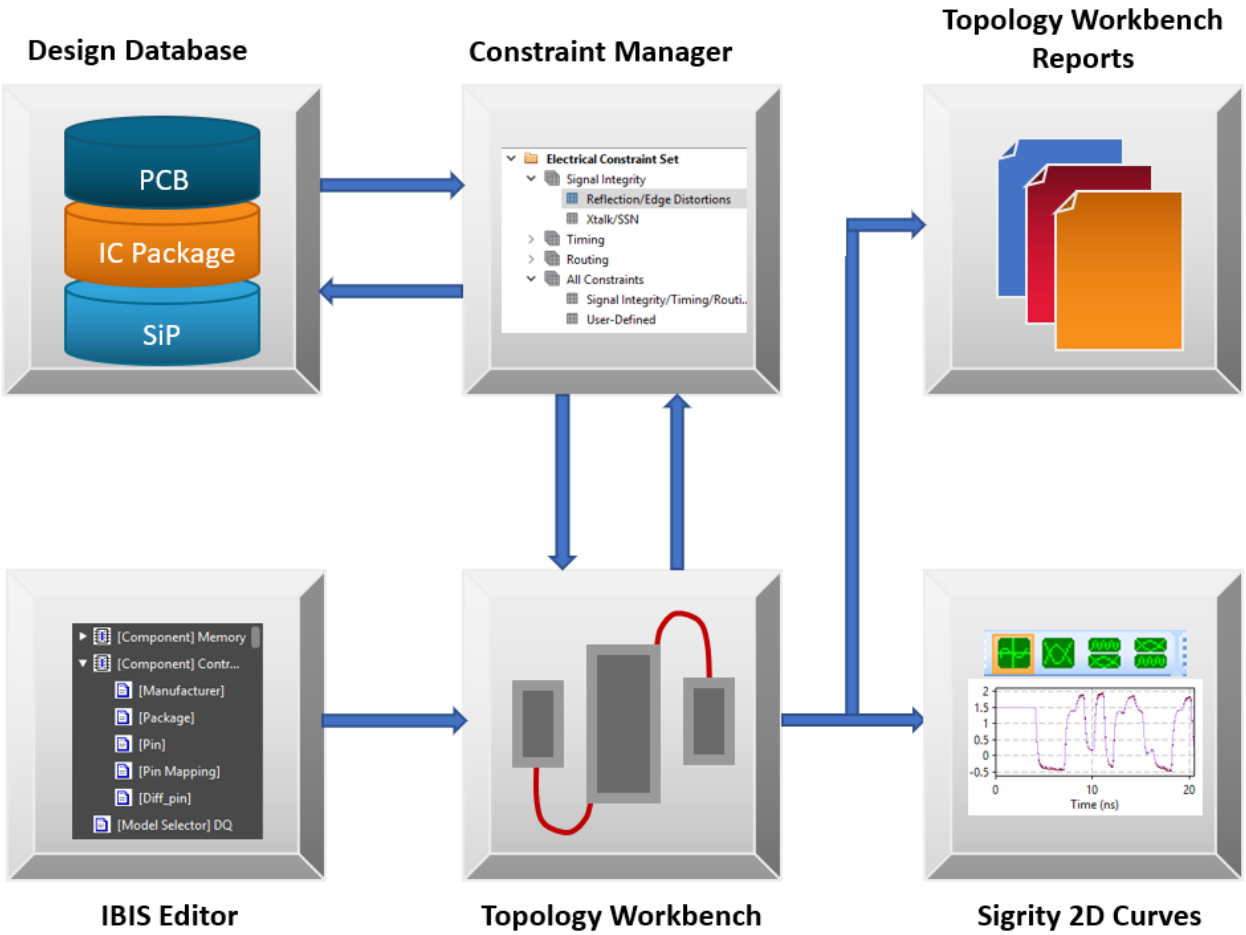
  Customers with a maintenance contract with Cadence can obtain the latest information about various tools at: https://support.cadence.com

2

Getting Started with Topology Explorer

Topology Workbench is an advanced SPICE-based simulation and analysis environment that enables exploring, identifying, and solving the adverse analog effects of high-speed digital systems. It is the next-generation topology environment that replaces both Sigrity System Explorer and Cadence SigXplorer tools from SPB 17.2 and earlier releases.

You can optimally use Topology Workbench along with the other tools for exploration, pre-route analysis, and post-route verification. The figure below shows the pre-route analysis process flow:

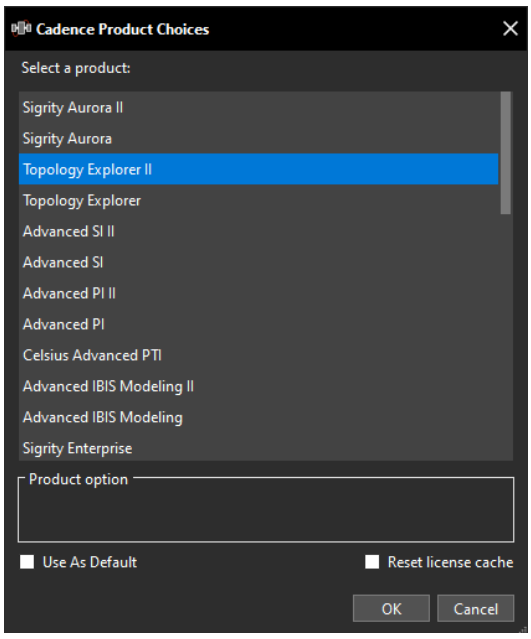


The easy-to-use interface of Topology Workbench lets you visually:

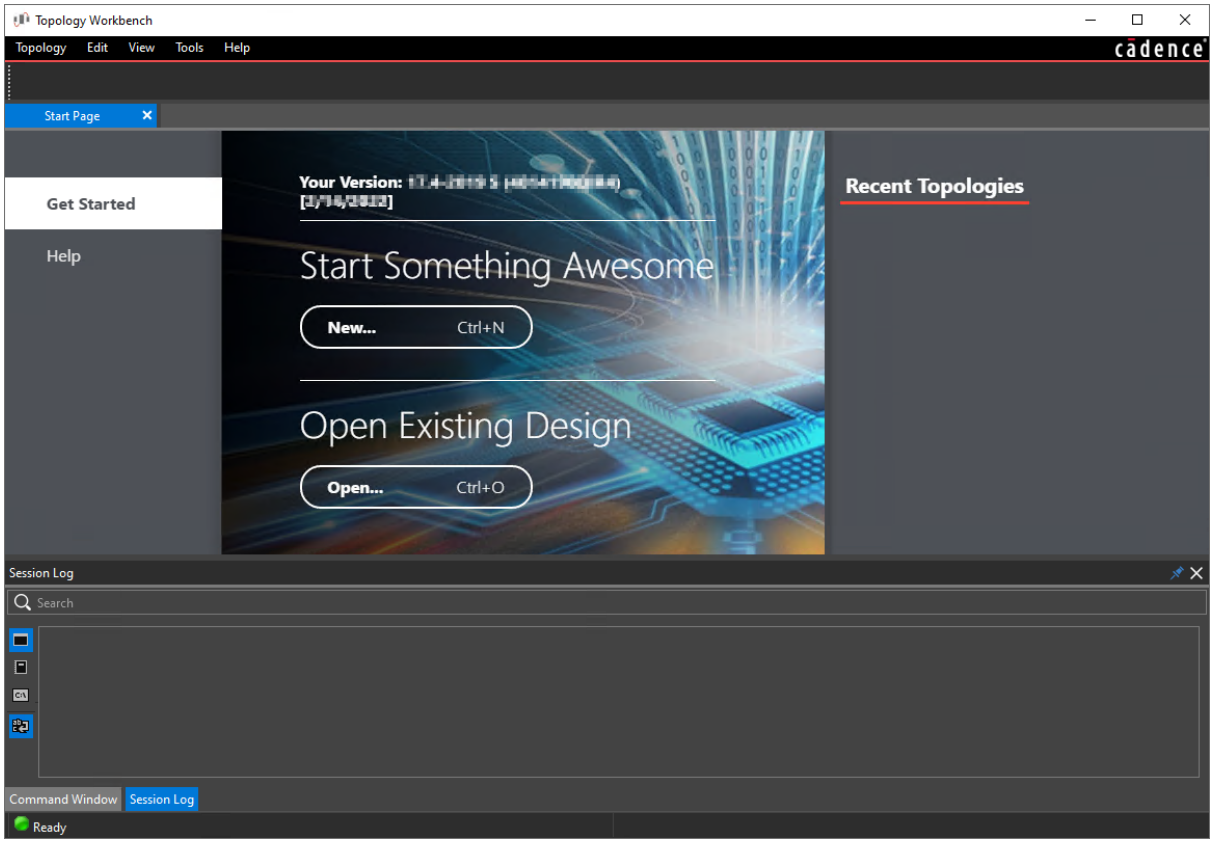
- Construct or extract interconnect topologies for signals or Power Distribution Networks (PDNs).
- Run simulations or sweep multiple scenarios with a series of simulations.
- Generate reports to review results.
- Capture constraints to be passed back to the Allegro PCB/package layout environment.

Create a New Blank Topology

1. Start Topology Workbench in standalone mode.
   - In Windows, use one of the following ways:
     - *Start – Run*, and type `TopWb`
     - *Start – Programs – Cadence Systems Analysis <release_number> – Sigrity Topology Workbench*
   - In UNIX, type `TopWb` in a Shell window.
2. Select *Topology Explorer II* or *Topology Explorer* from the *Cadence Product Choices* dialog box that is displayed. This product choice lets you perform sandbox-style general SI analysis.



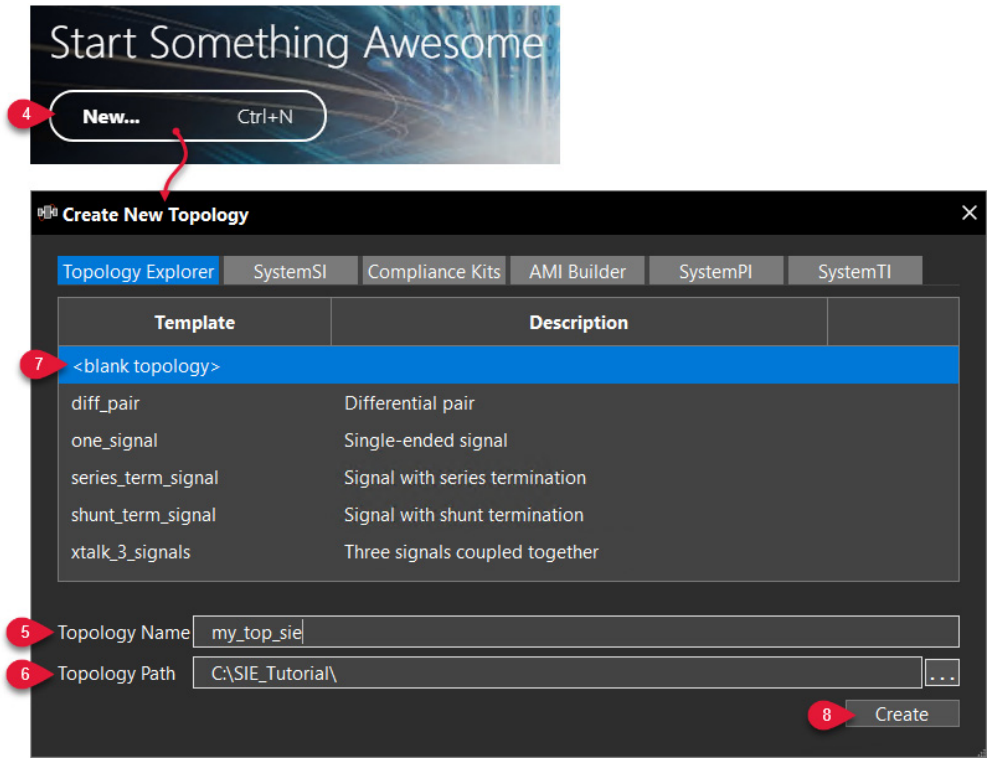
3. Click *OK*. The Topology Workbench window opens with the *Start Page* tab in focus as shown below.



Tip

To familiarize yourself with the elements of this window, refer to Exploring the Topology Workbench Interface in the *Topology Workbench User Guide*.

4. Click *New...* from the *Start Something Awesome* section on the *Start Page* tab. The *Create New Topology* dialog box is displayed with the *Topology Explorer* tab selected, as shown below.



This dialog box allows access to all capabilities in Topology Workbench. Selecting the options in the other tabs will reopen the *Cadence Product Choices* dialog box.

There are currently four methods of topology creation. The first two methods give below are available in the *Create New Topology* dialog box:

a. From scratch (the *<blank topology>* template row)

b. From a template (one of the named template rows)

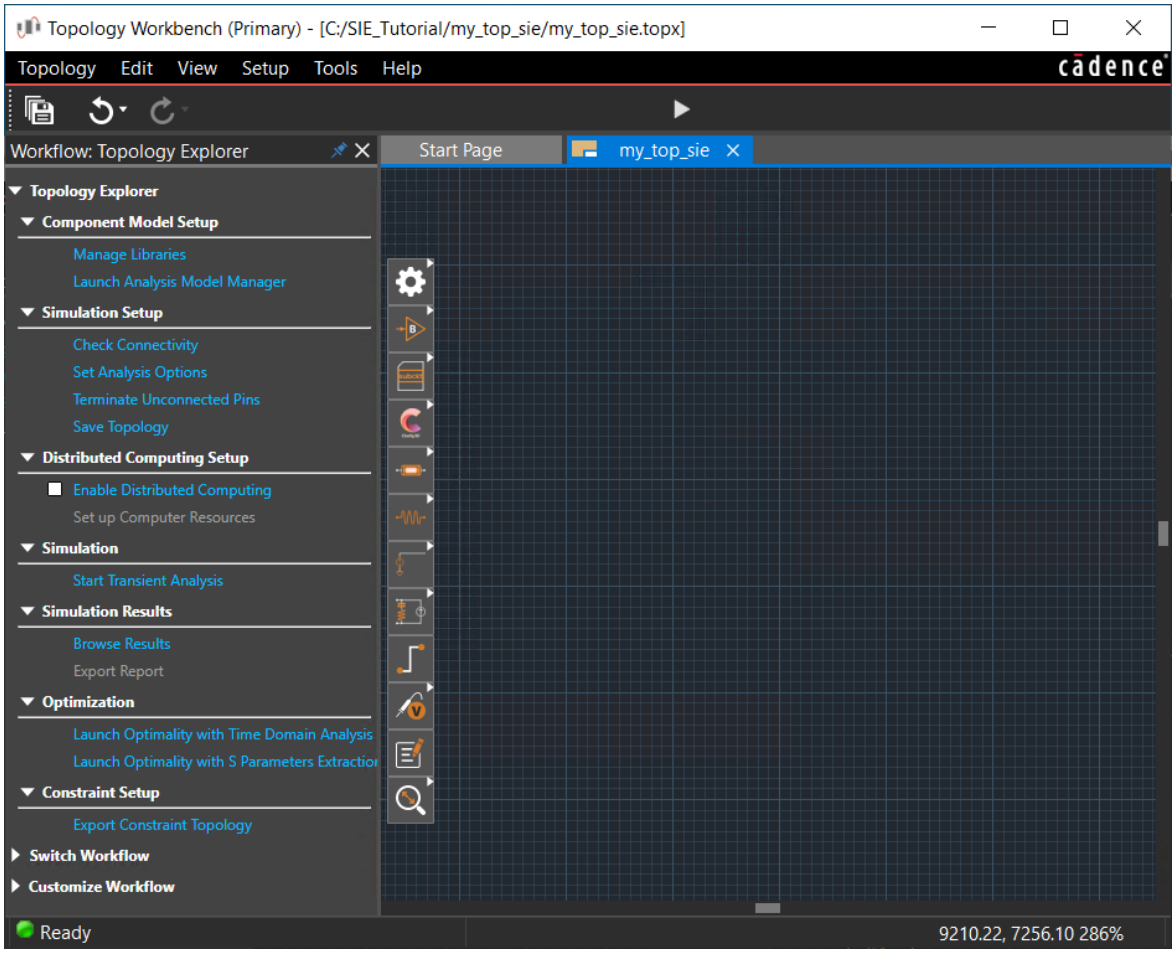
c. From old formats (`.ssix` and `.top` files using the *Open* button or a link under the *Recent Topologies* pane in the *Start Page – Get Started* tab)

d. Extract from Allegro (this is explained in Module 2)

5. Type *my_top_sie* in the *Topology Name* box.

Note: A topology's name can contain only lowercase alphanumeric characters and underscores. If a topology with the same name exists already, a message is displayed to confirm if you want to overwrite it.

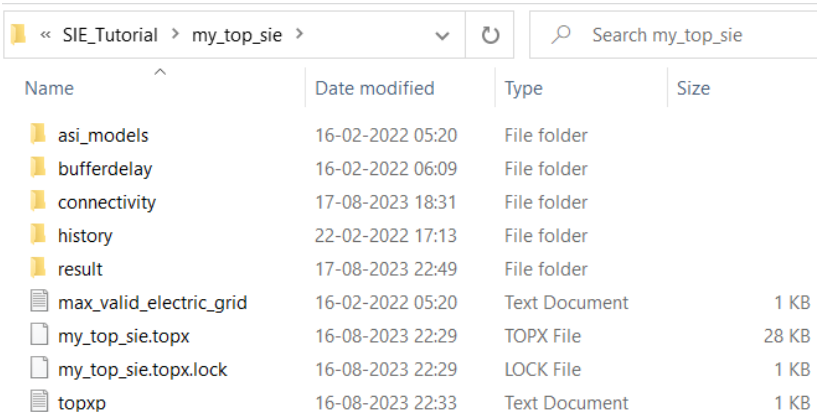
6. Browse and set the *Topology Path* to the directory where the new topology and related files should be saved on the hard drive. For example, we have browsed and selected the *SIE_Tutorial* directory, which we had created before starting this tutorial.
7. Select *<blank topology>*.
8. Click *Create*. A tab named *my_top_sie* with blank canvas opens in the Topology Workbench window.



The Topology Workbench canvas is designed to have a minimalistic layout with a few icons and panes on the left and right side of the canvas. Additional dialogs open at the bottom as needed.

A subdirectory with the given topology name, *my_top_sie*, is created at the *Topology Path* you browsed to in step 6. This directory contains the project file

(*my_top_sie.topx*), and subdirectories for the model files associated with the various blocks, history, and simulation results.



Add and Connect Blocks to Build a Topology

Before starting with the placement of blocks on the canvas to build a topology, ensure that the *Diff Signals* and *Block-Based* toggle buttons are deselected in the *Settings* option of the floating toolbar.

Let us now build a topology using the following elements:

- A *Transmitter (IBIS)* block
- A *Trace* block
- A *Receiver (IBIS)* block

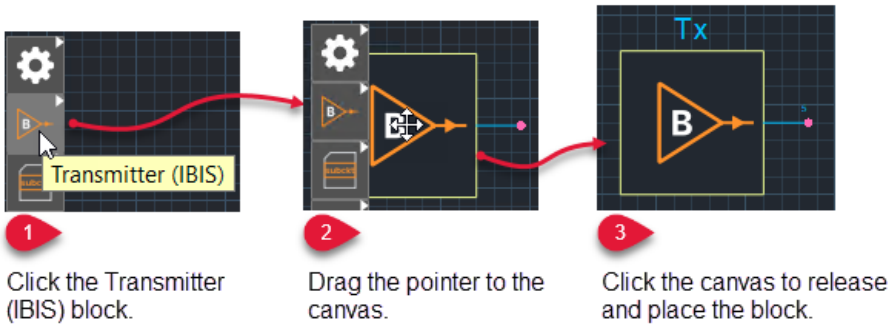
Tip

The IBIS blocks have a *B* mark on them.

For more information about the available blocks, refer to Choosing Blocks to Place on Canvas in the *Topology Workbench User Guide*.

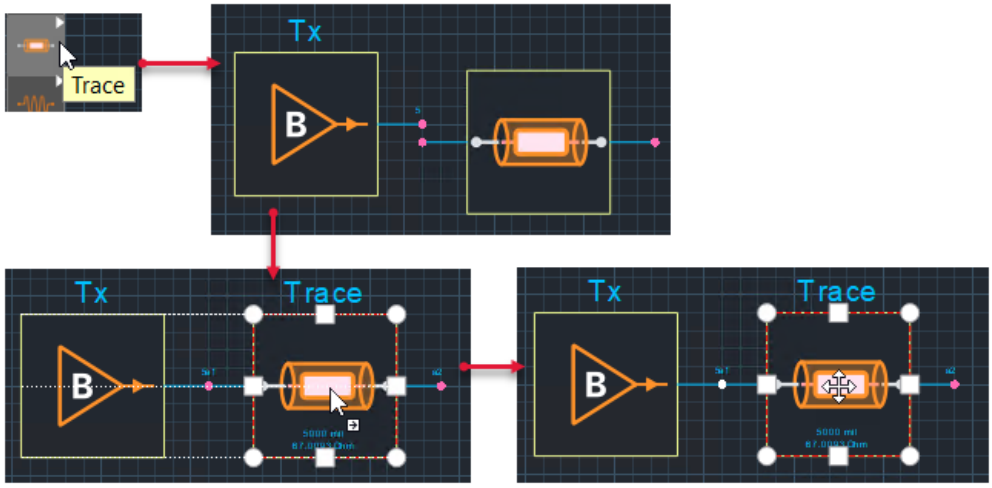
1. Click the *Transmitter (IBIS)* block in the floating toolbar. This selects and attaches the block to the pointer.
2. Drag the pointer to the canvas location where the transmitter block needs to be placed.

3. Click the canvas to release and place the *Transmitter (IBIS)* block as illustrated in the figure below. The block is assigned default name, *Tx*, which you can change in the *Edit Properties* panel.

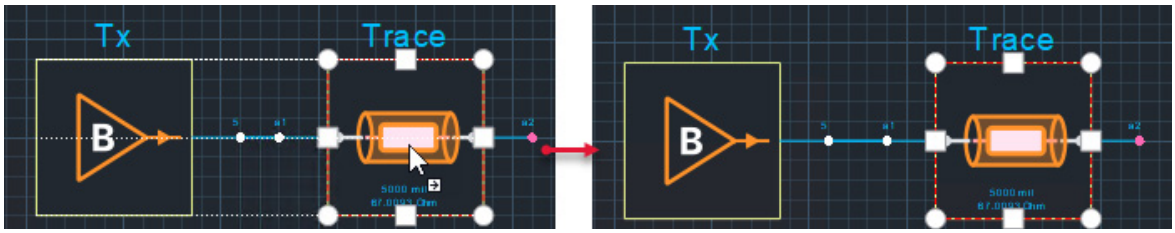


4. Select the *Trace* block in the floating toolbar and drag toward the *Transmitter (IBIS)* block on the canvas.

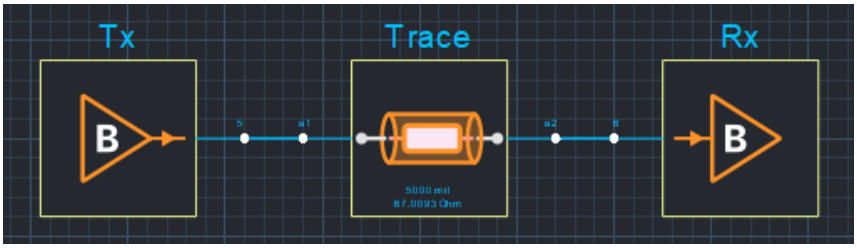
5. Overlap the left pin of the *Trace* block on that of the *Transmitter (IBIS)* block as shown below, and then click the canvas. Notice that color of the connection ports changes to white from pink.



6. Move the *Trace* block apart from the *Transmitter (IBIS)* block to view the connection line between the two blocks as shown below.

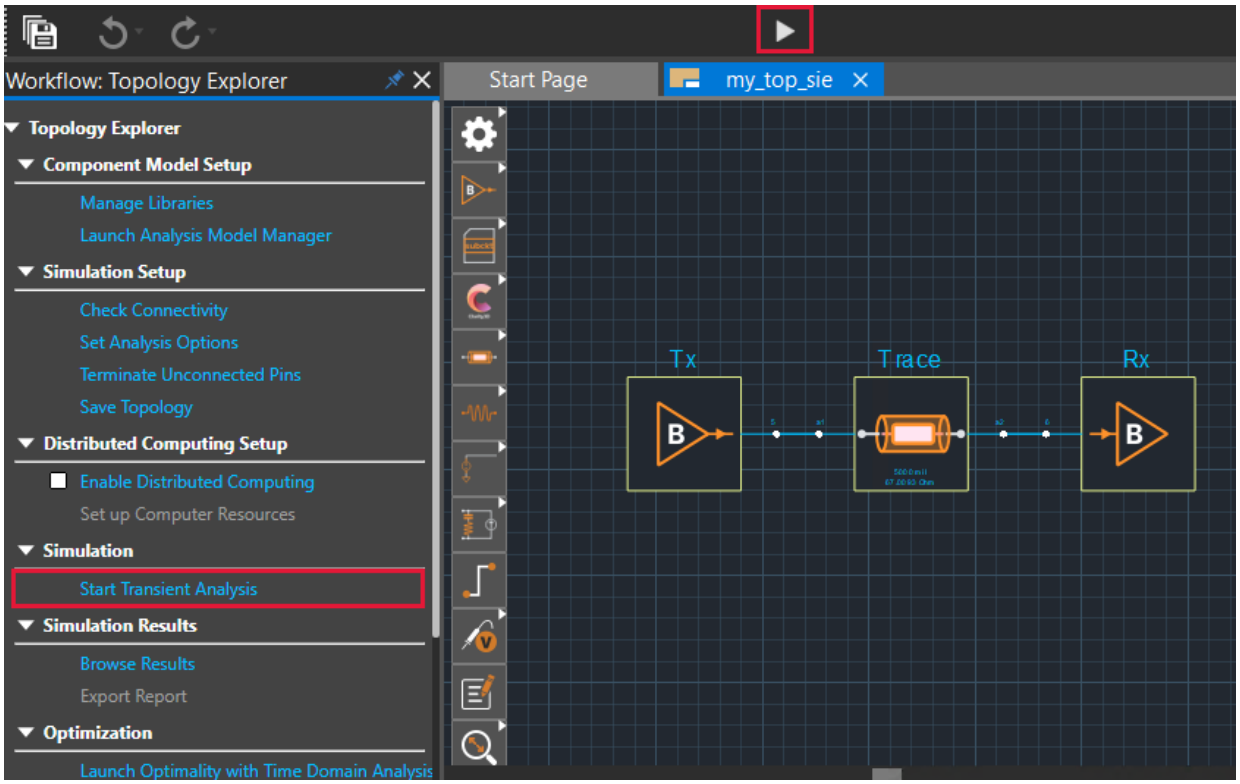


Similarly, after you place and connect a *Receiver* (IBIS) block to the right connection port of the *Trace* block, your topology should look like the following:



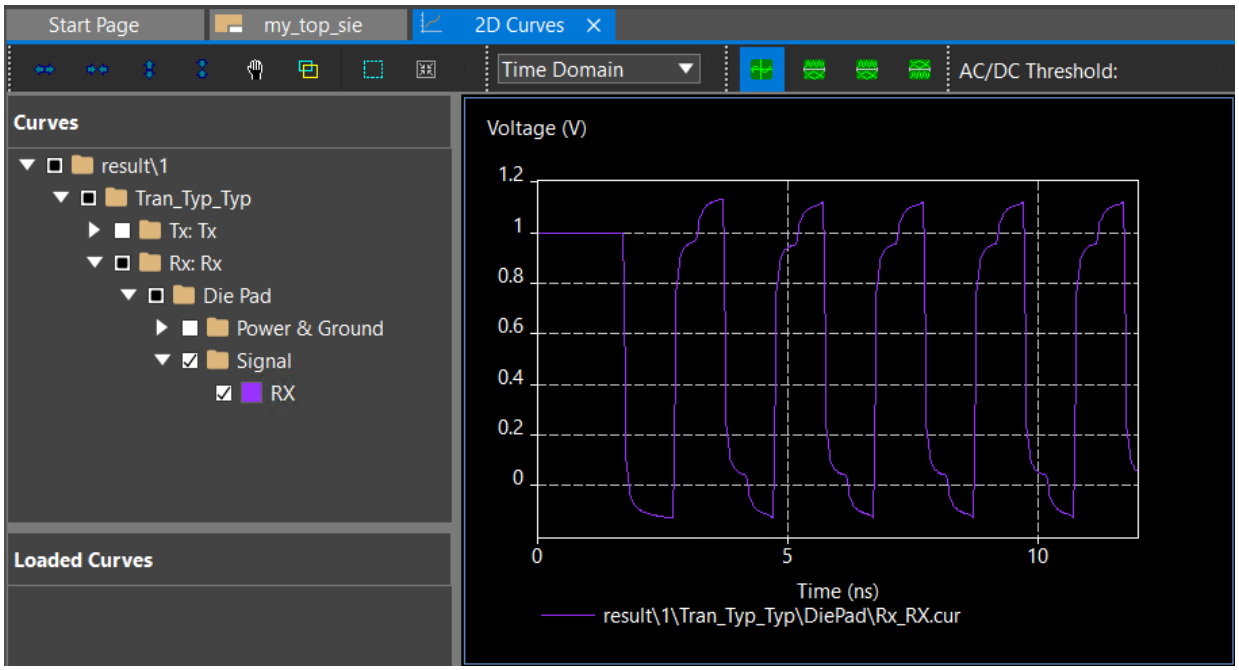
Note: With both the toggle buttons in the *Settings* option of the floating toolbar are deselected, the connectivity is single-pin-based, just like Signal Explorer (SigXplorer), and requires no model-connection protocol (MCP) to define the connectivity. Also, all blocks have default models associated.

7. Click *Start Transient Analysis* in the *Workflow* panel or click the play ( ) button.



The simulation starts to run for the topology you just created. The status bar gives you a run-time glimpse of the simulation status. It also shows the time elapsed and remaining.

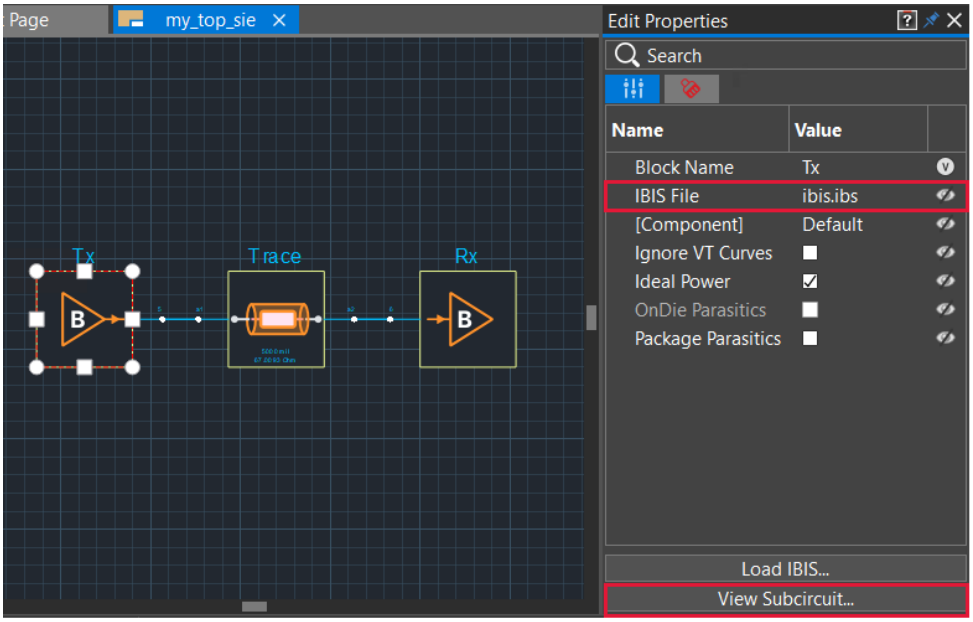
On completion of the simulation run, the results are displayed in the 2D Curves tab within the Topology Workbench window.



8. Close the 2D Curves tab.

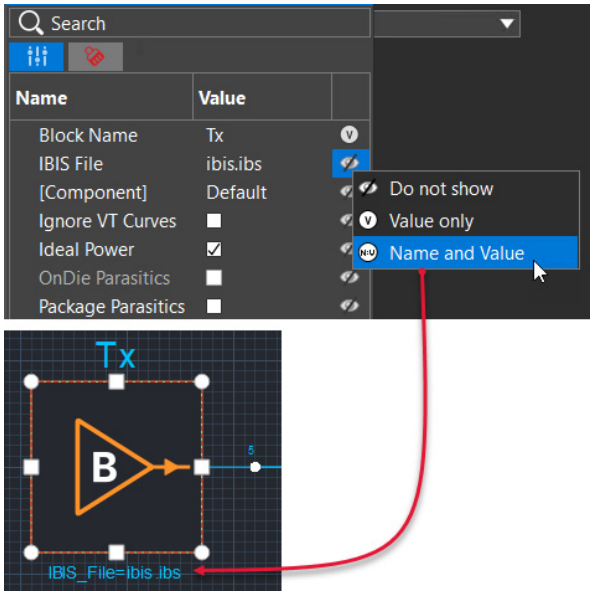
Edit and Configure the Blocks

1. Double-click the *Tx* (transmitter) block in the canvas. This displays the properties of the transmitter block in the *Edit Properties* panel. This method simplifies the use model. Notice the default IBIS model and the *View Subcircuit* button to access the subcircuit.

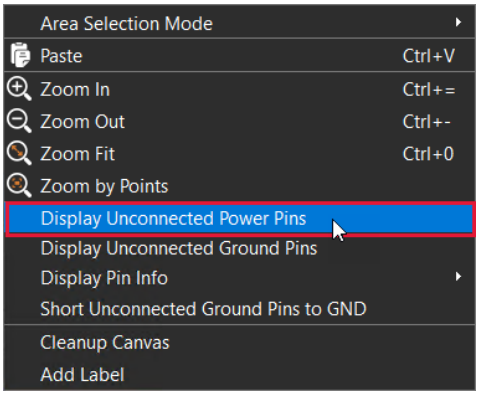


2. Click the cell in the last column of the *IBIS File* row and select *Name and Value* from the displayed options. The icons in this last column indicate visibility on the canvas and

gives you control over what gets annotated. Also, the IBIS model file's name starts to display below the transmitter block on the canvas.

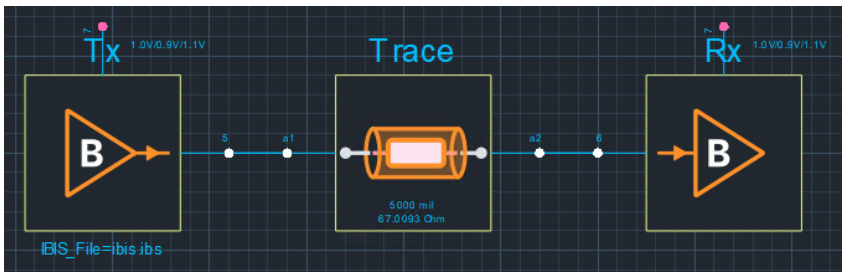


3. Right-click the blank area on the canvas and select *Display Unconnected Power Pins* from the displayed shortcut menu.

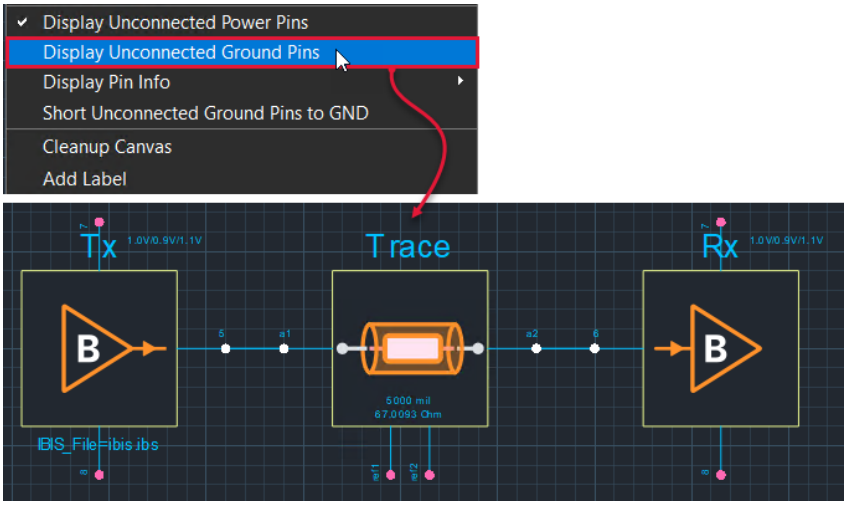


Note: Alternatively, if the Edit Properties panel is open, clicking anywhere in the blank area on the canvas displays the *Display Unconnected Power Pins* toggle button within the panel. The *Settings* option in the floating toolbar also has this toggle button.

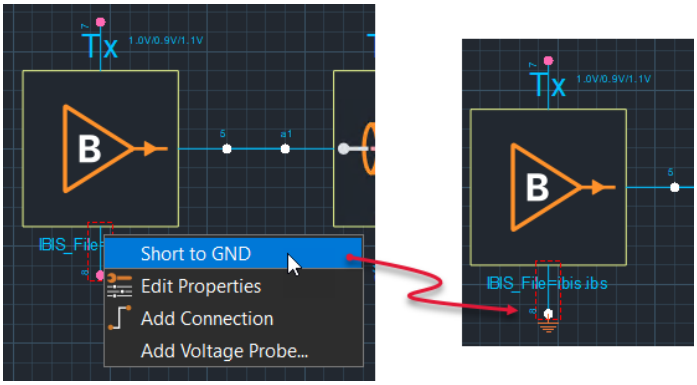
The blocks on the canvas start to show their unconnected power pins.



4. Right-click the canvas again and select *Display Unconnected Ground Pins* this time from the shortcut menu. Both the display options in the shortcut menu should now have a check mark and you will see the exposed power and ground nodes (as appropriate) on each block.

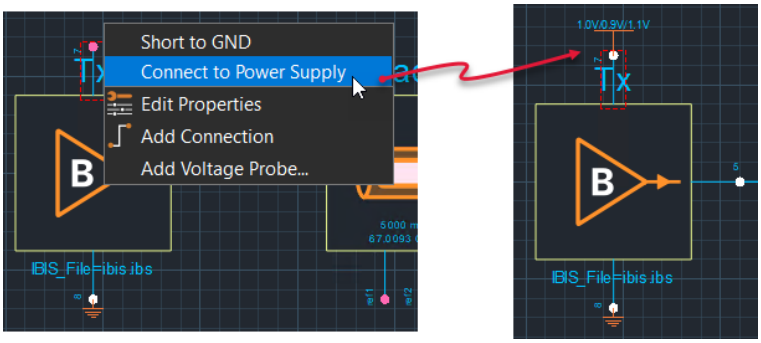


5. Right-click the ground pin for the *Tx* block and select *Short to GND* from the shortcut menu.

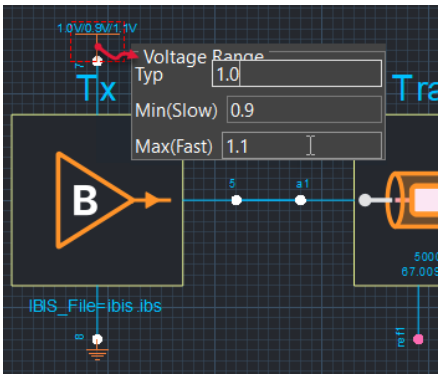


Visually, this is equivalent to not exposing the pin. The pins can be connected directly to the ground with an automatic symbol added or connected through any desired path.

6. Right-click the ground pin for the *Tx* block and select *Connect to Power Supply* from the shortcut menu. A range of values is added to the pin.



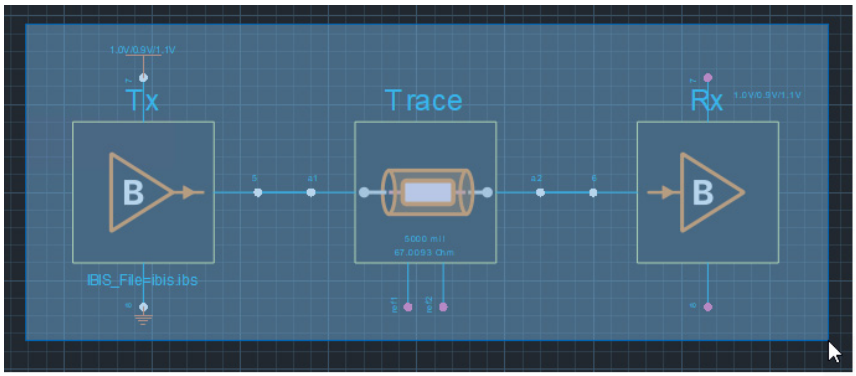
7. Double-click the same power pin of the Tx block. The *Voltage Range* on-canvas editing box opens below the voltage values as shown below:

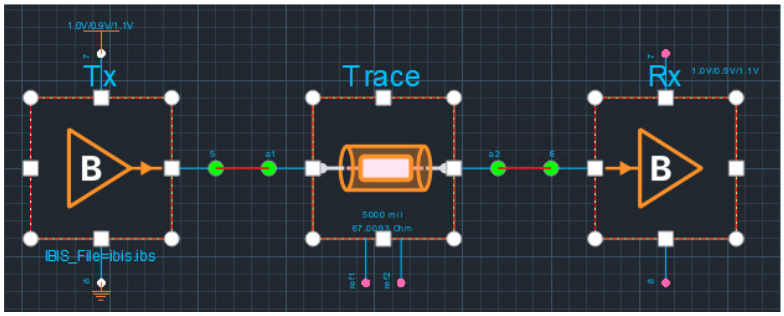


You can edit the *Typ*, *Min(Slow)*, and *Max(Fast)* voltage range values in this box like the *Edit Properties* panel. This allows you to set the voltage range for a block.

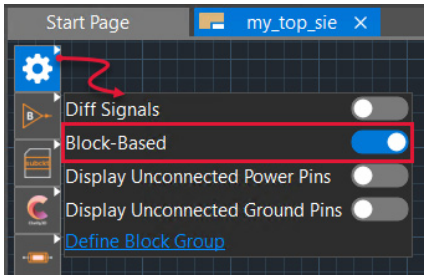
Build a Topology with Block-Based Connectivity

1. Select all components on the canvas by dragging the mouse as shown below.



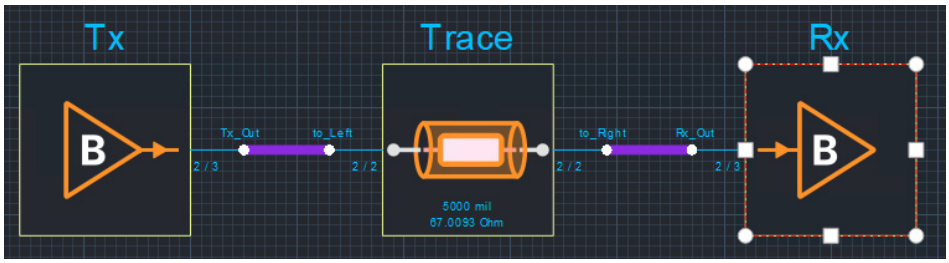


2. Press the `Delete` key to delete all selected components along with the associated connectivity.
3. Select the *Block-Based* toggle button in the *Settings* option of the floating toolbar. Any new block that you will add now will have MCP-based connectivity.



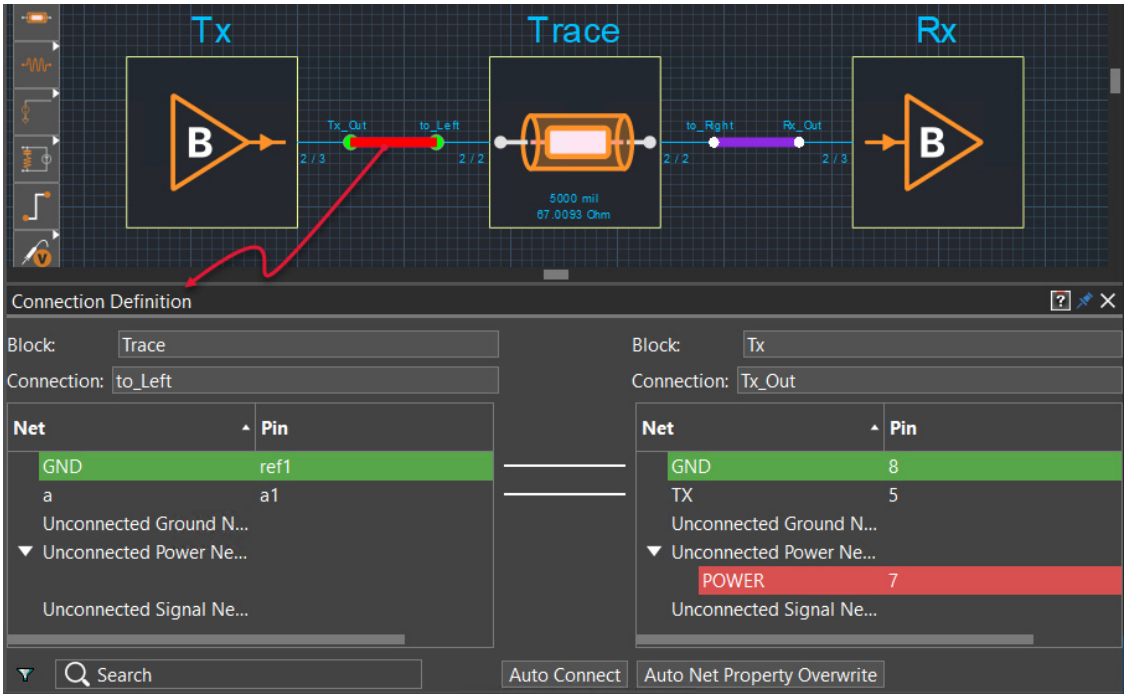
4. Re-build an exactly same topology consisting of the following blocks as you did in the Add and Connect Blocks to Build a Topology topic:
   - ❑ A *Transmitter* (IBIS) block
   - ❑ A *Trace* block

- ❑ A *Receiver* (IBIS) block



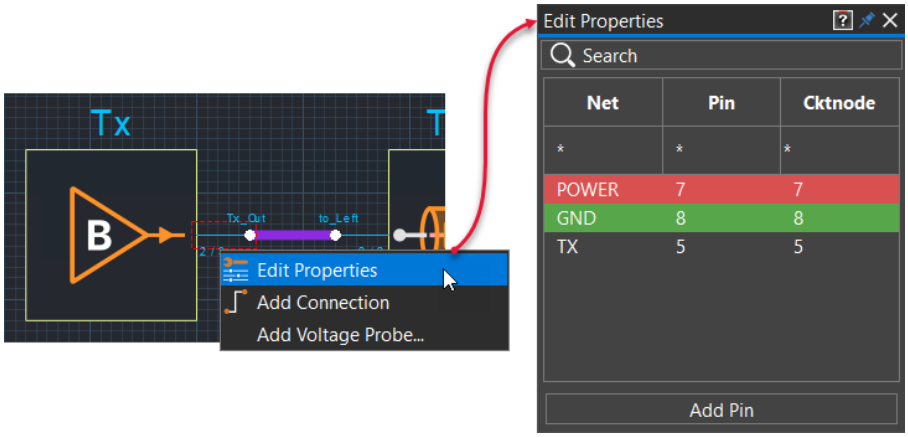
Notice the thicker connectivity lines and the number of connected or total connections indication for each pin.

5. Double-click one of the thick purple connectivity lines. The *Connection Definition* panel opens. This is the MCP connectivity panel of Topology Workbench.

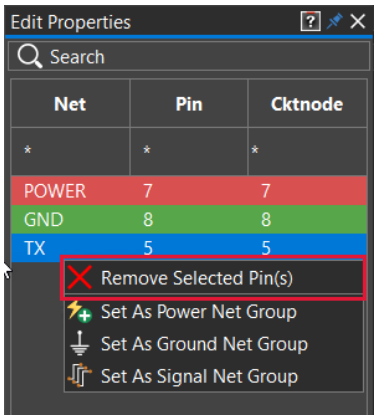


6. Click X in the title bar of the *Connection Definition* panel to close it.

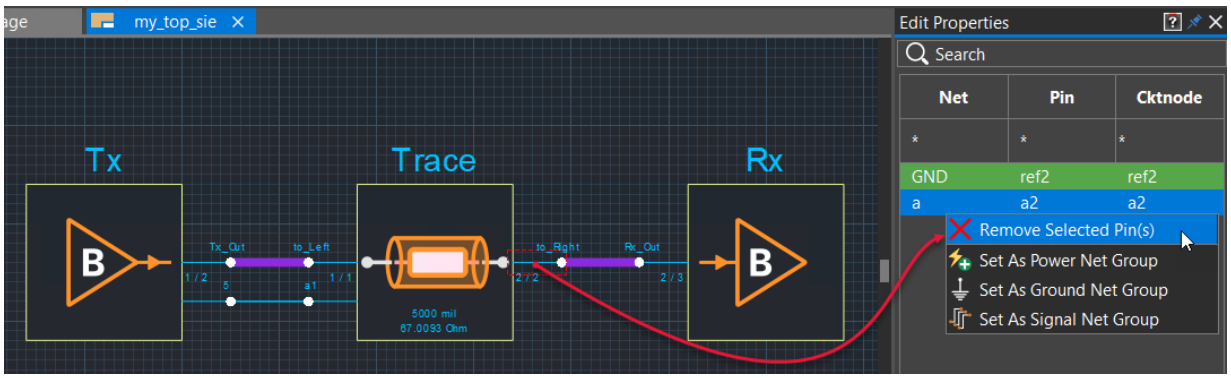
7. Right-click the *Tx_Out* pin on the *Tx* block and select *Edit Properties* to open the corresponding panel.



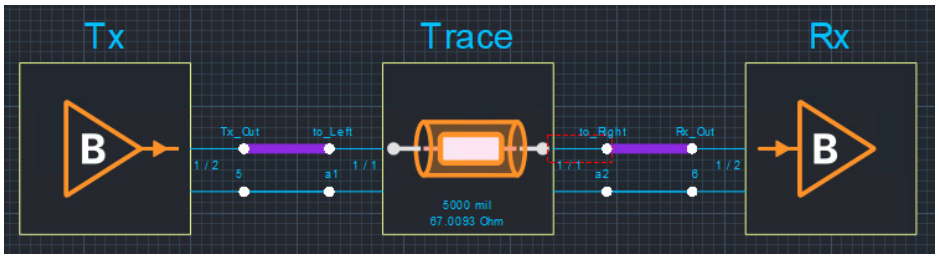
8. Right-click the *Tx* pin in the *Edit Properties* panel and select *Remove Selected Pin(s)* from the shortcut menu.



9. Repeat the process for the *to_Right* pin on the other side of the *Trace* block and remove the pin named *a*.



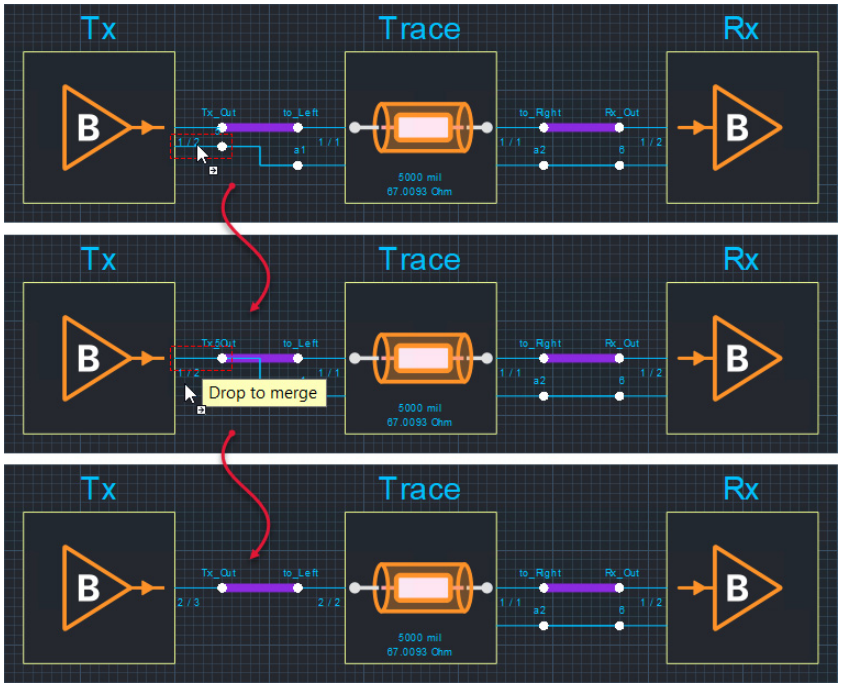
This topology now has a mix of single-pin and multi-pins. This is just some of the available customizations to have a mix of hierarchy in the canvas. You can also go the other way.



Tip

[Optional] Delete all the connecting lines on the canvas by selecting them and pressing the `Delete` key. Now, move the *Trace* block out of the way. Connect *Tx* and *Rx* by overlapping the pins and move them back into the positions illustrated above. Place *Trace* on top of the existing interconnect. As long as the pins match, the new connections will be made.

10. Select the single pin on the *Tx* block and drag it back to the pin above it. This will merge the pins as a single multi-pin.



11. Exit Topology Workbench without saving the topology.

3

Pre-layout Extraction and Export of Topology Constraints

In Getting Started with Topology Explorer, you explored the standalone interface of Topology Workbench and its capabilities while creating a simple topology for the Topology Explorer workflow. The other key aspect of Topology Workbench is the integration with the Constraint Manager-driven flow of Allegro. Majority of the existing Signal Explorer (SigXplorer) users use it for the constraint generation portion with no simulation. There are multiple use models, but the most common is extracting a topology from an existing design – schematic or layout.

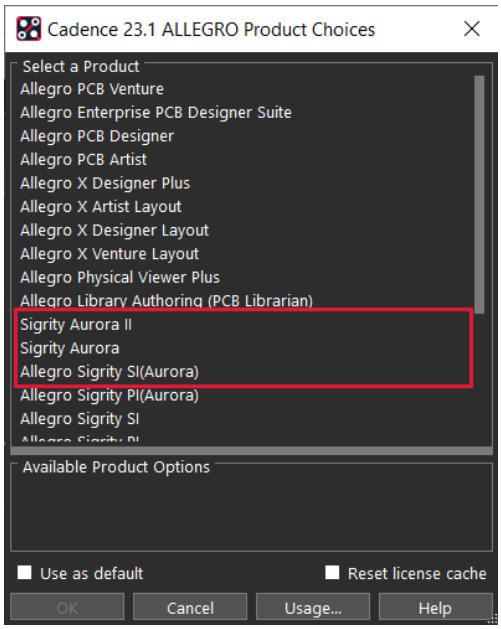
In this topic, you will learn:

- How to extract a topology from Constraint Manager on an unrouted board
- How to use this topology to create a constraint set for the board

Extract Topology from Constraint Manager

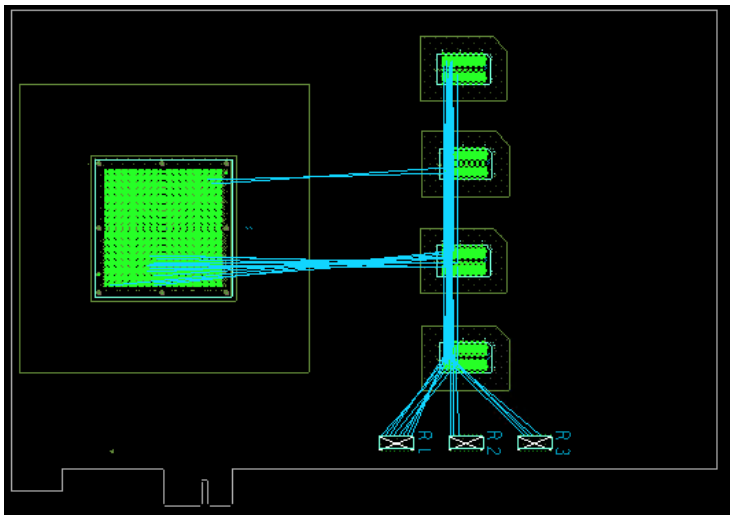
1. Select *Start – Programs – Cadence PCB <release_number> – PCB Editor <release_number>*.

2. Select *Sigrity Aurora II* or *Sigrity Aurora* in the displayed *ALLEGRO Product Choices* dialog box. If this is not available, select *Allegro Sigirty SI(Aurora)*.



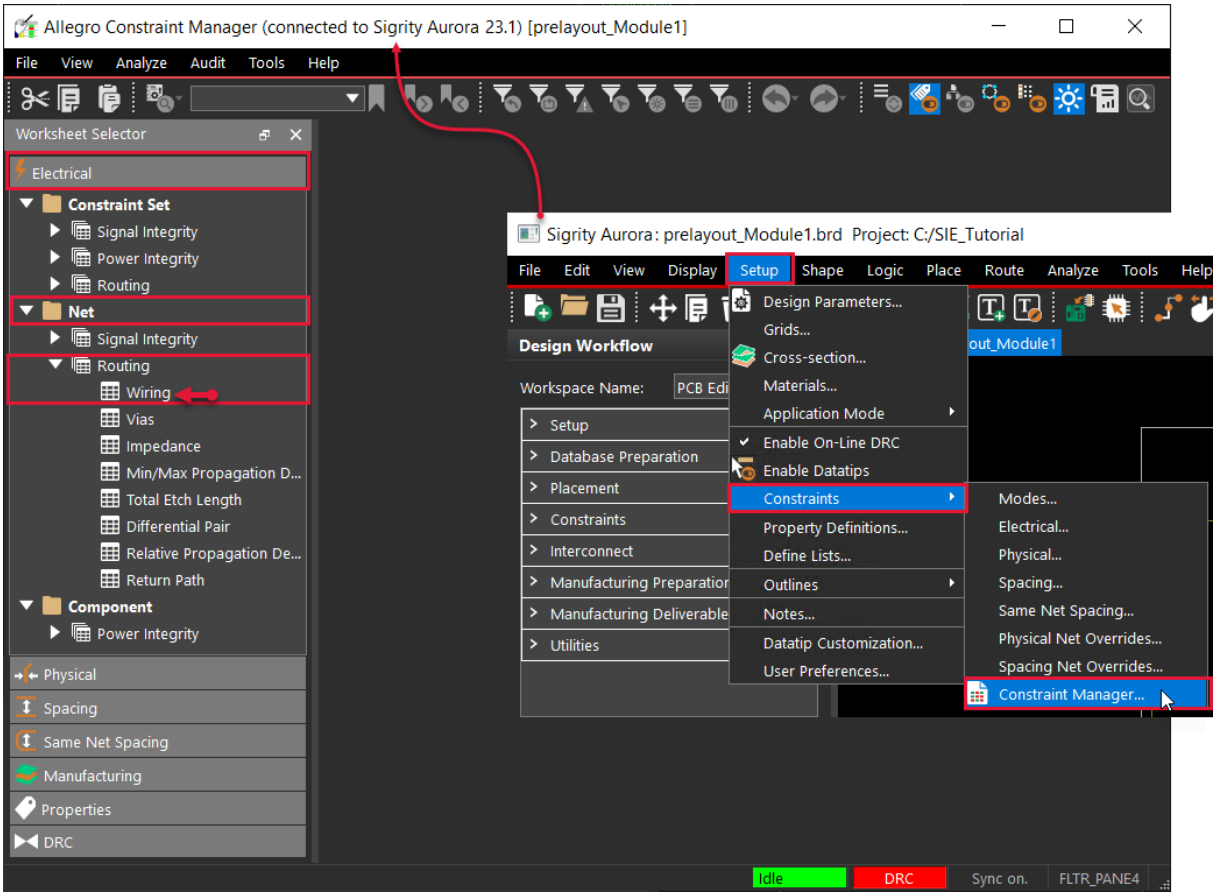
3. Open the `prelayout_Module1.brd` file from the following directory:

   `<INSTALL_DIR>\share\topxp\Tutorials\SIE_Tutorial`



This design has just the *rats* turned on for the address bus. You can see that they are not scheduled in a fly-by technology. You might not desire the default algorithm based on the shortest connection distance.

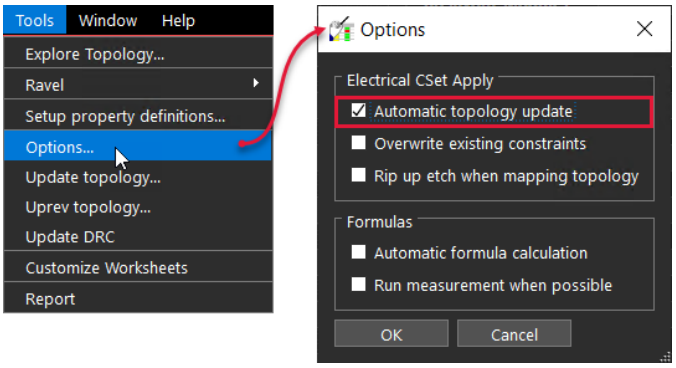
4. From the main menu, select *Setup – Constraints – Constraint Manager*. The *Allegro Constraint Manager* window opens.



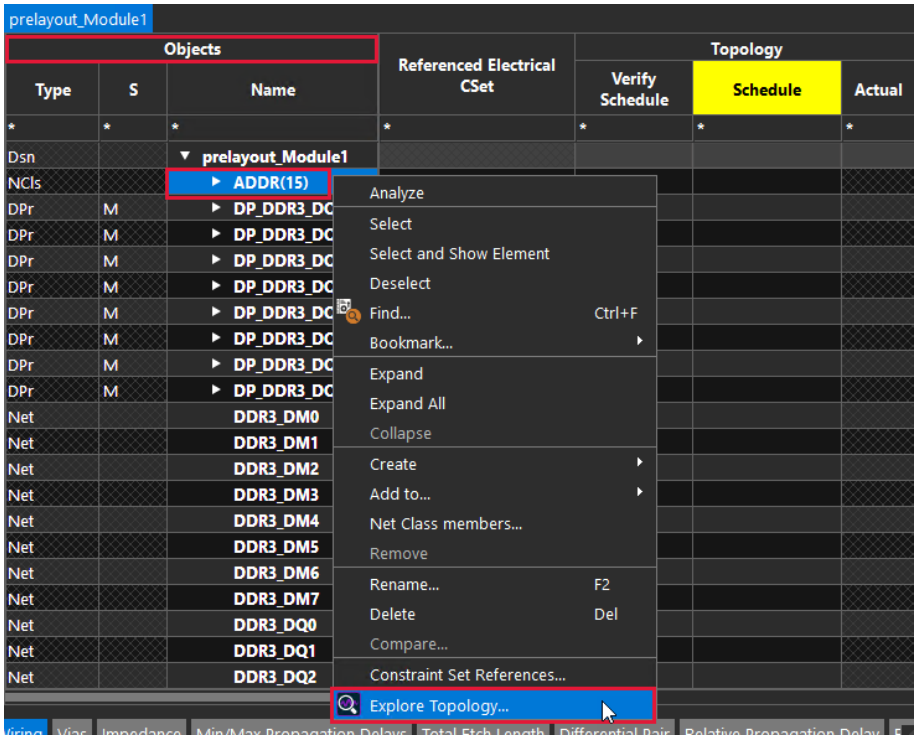
5. Open the *Electrical* module in the *Worksheet Selector* pane and select *Net – Routing – Wiring*.

   Note: You might have more workbooks in your *Worksheet Selector* depending on your license.

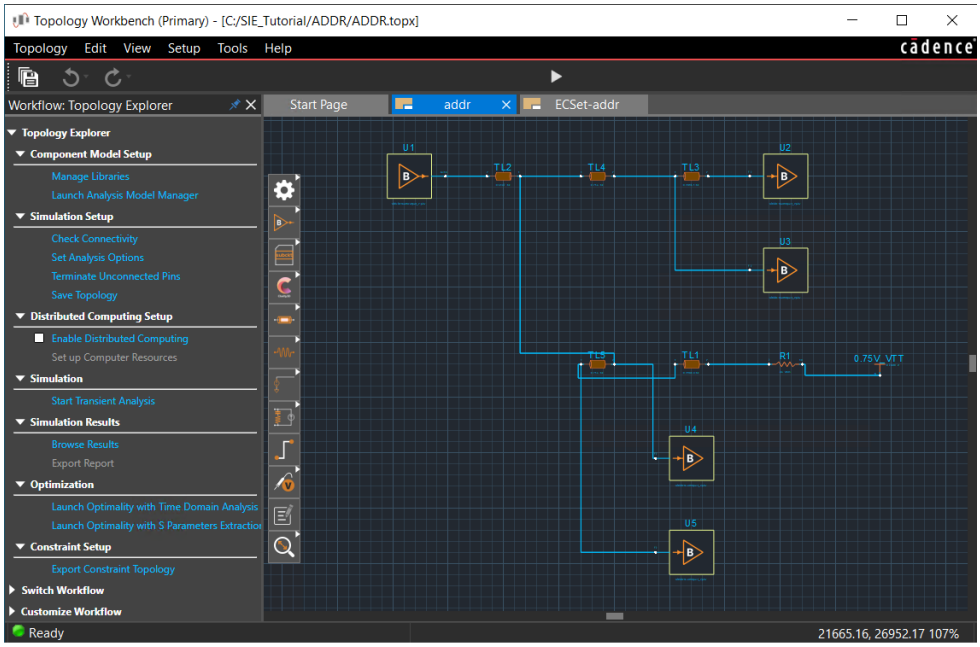
6. Click *Tools – Options*. The *Options* dialog box of Constraint Manager opens.

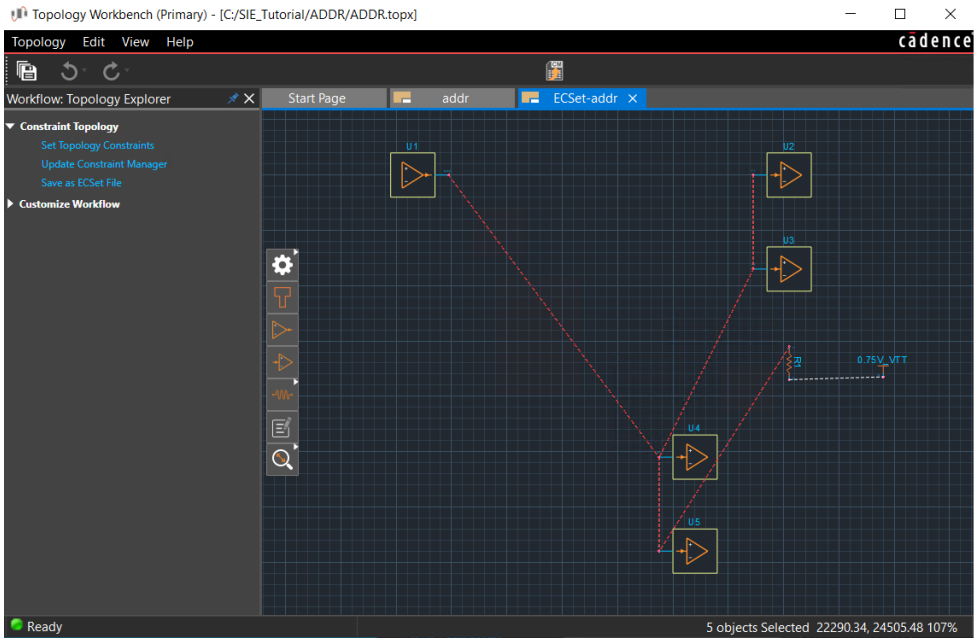


7. Ensure that the *Automatic topology update* check box is selected in the *Electrical CSet Apply* section.
8. Click *OK*.
9. Scroll to the top of the *Objects* column in Constraint Manager and right-click the *ADDR(15)* net class.
10. Select *Explore Topology* from the shortcut menu.



11. Select *Topology Explorer* in the *Cadence Product Choices* dialog box if you are prompted to and click *OK*. The topology of the selected net is extracted to the Topology Workbench window in two tabs, *<net_name>* and *ECSet-<net_name>*.





Note: The wiring on your canvas can look different than what is illustrated above.

The workflow panel in the *<net_name>* tab lets you run transient analysis for the extracted net using the Topology Explorer workflow.

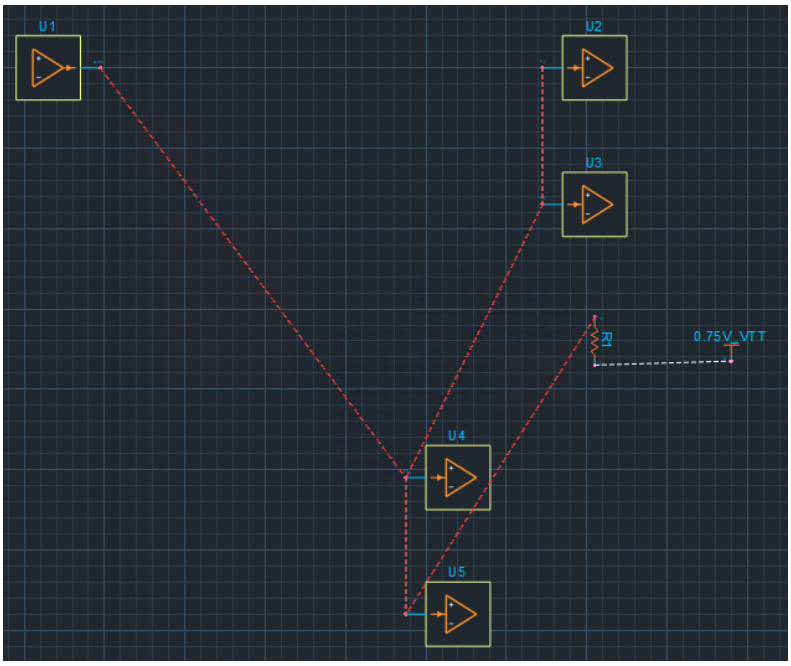
In the *ECSet-<net_name>* tab, you can set topology constraints, save the topology as a ECSet file, and update the Constraint Manager for the extracted net. In addition, the floating toolbar contains:

- Settings to toggle adding of blocks with differential signals
- Options to add blocks of the following types to the topology: TPoint, transmitter, receiver, resistor, inductor, capacitor, diode, and Vdc
- Option to add notes
- Controls to zoom in, zoom out, zoom fit, and zoom by points

Add Constraints in Topology Workbench

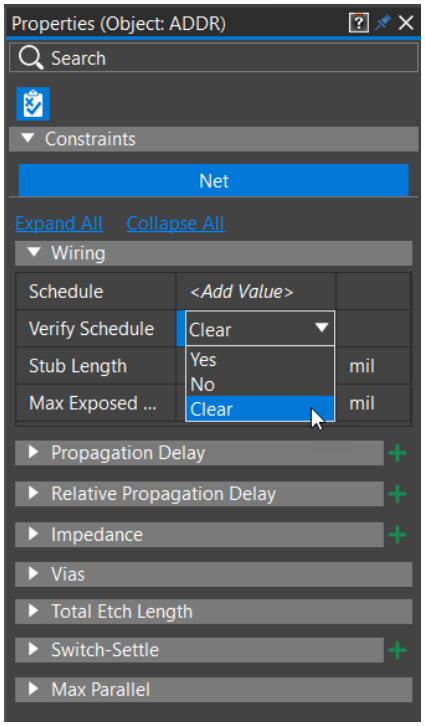
On the *ECSet-<net_name>* tab, perform the following steps to add constraints to the extracted net in Topology Workbench:

1. Check the wiring of the pins based on the new placement. Make only pin-to-pin connections and ensure that there is a white ball, instead of a pink one, at the start and end of each connection indicating that a proper connection exists. Your canvas should look like the following to show the desired *fly-by* schedule:

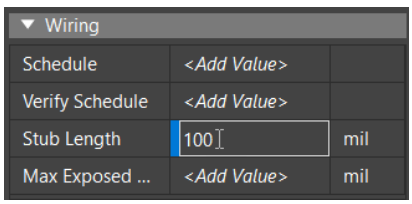


2. Click *Set Topology Constraints* in the *Workflow* panel. The *Properties (Object:ADDR)* panel opens and the wire is highlighted on the canvas.

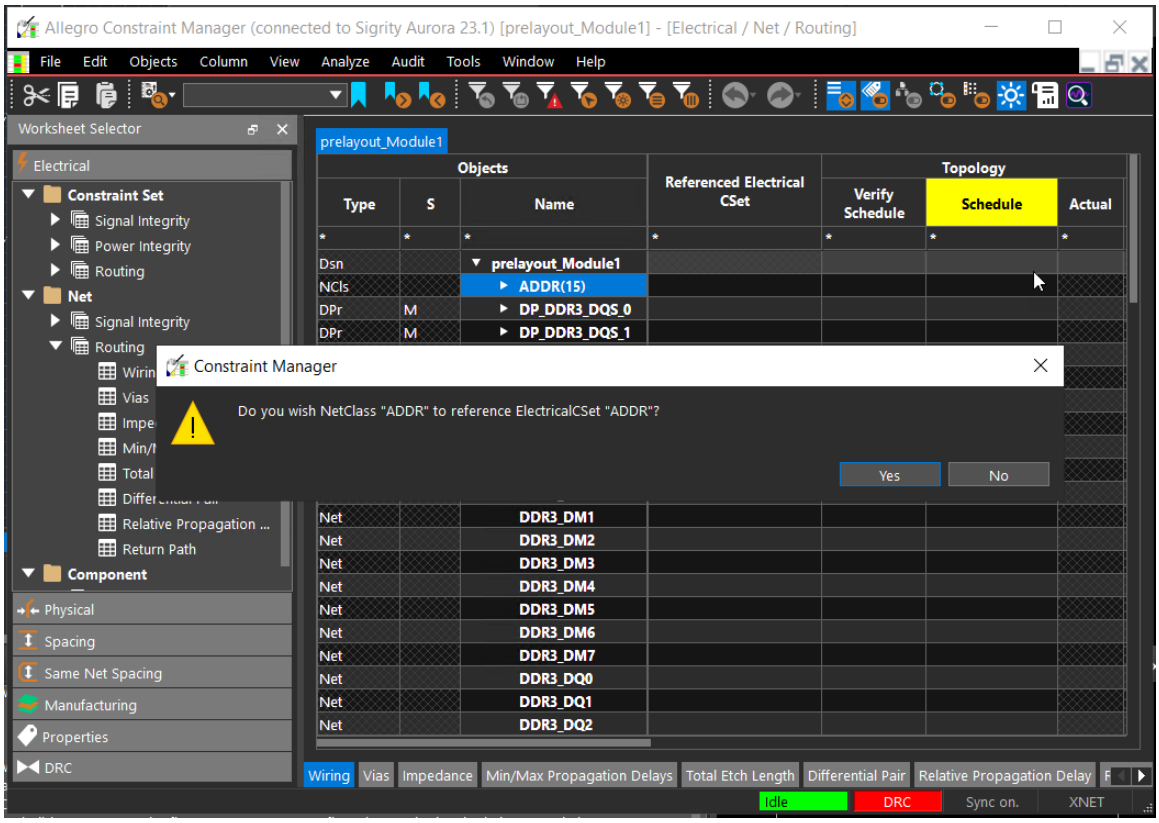
3. Click the *Wiring* schema in the *Properties* panel to expand and view the existing constraints.
4. Reset the *Schedule* value to *Clear*.
5. Reset the *Verify Schedule* value from *Yes* to *Clear*. This indicates that there are no specific design rule checks (DRC) for the topology.



6. Reset the *Stub Length* value to *100* mil.



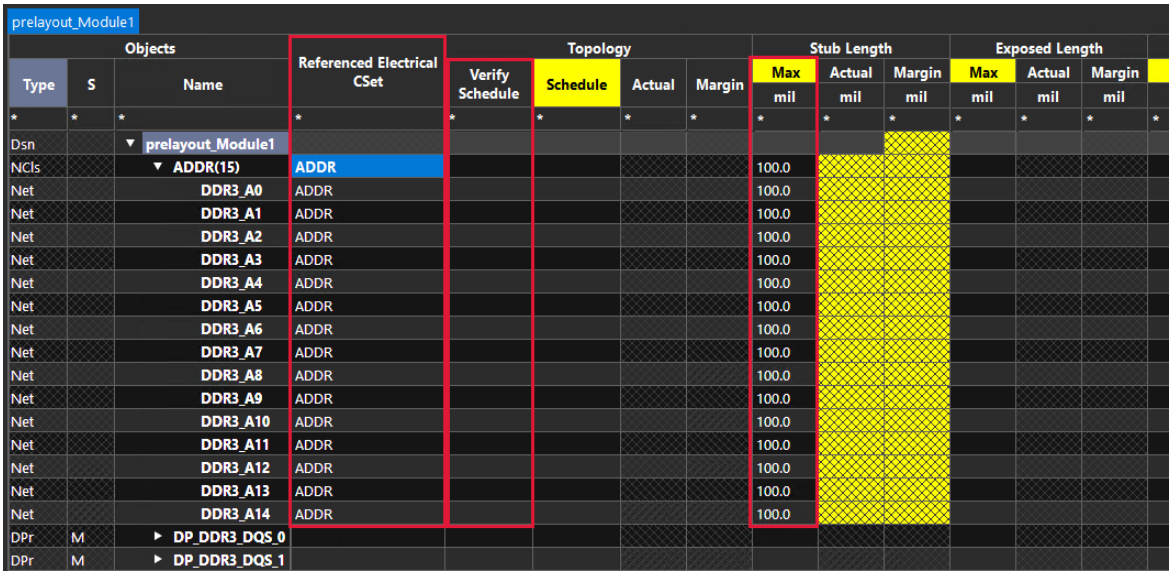
7. Click *Update Constraint Manager* in the *Workflow* panel. The Allegro Constraint Manager window comes to the foreground again and a message prompts you to confirm if you want to assign the topology to the entire class.



8. Click *Yes* in the message box. Extracting a topology at the class-level means that it can be easily applied to all members of the class after it has been constrained. In the background, a `.top` file is generated to pass back to the Constraint Manager.

   When you expand the *ADDR(15)* node in the *Objects* column, notice that the table has been updated with the *Referenced Electrical CSet* information as you had set in Topology Workbench. As shown in the example below, all values from the *Verify*

Schedule column are now cleared and the *Stub Length – Max* column shows `100` mil to match the settings you updated in step 5 and step 6, respectively.



prelayout_Module1

Objects			Referenced Electrical CSet	Topology				Stub Length			Exposed Length			
Type	S	Name		Verify Schedule	Schedule	Actual	Margin	Max	Actual	Margin	Max	Actual	Margin	
								mil	mil	mil	mil	mil	mil	
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn		prelayout_Module1												
NCls		ADDR(15)	ADDR					100.0						
Net		DDR3_A0	ADDR					100.0						
Net		DDR3_A1	ADDR					100.0						
Net		DDR3_A2	ADDR					100.0						
Net		DDR3_A3	ADDR					100.0						
Net		DDR3_A4	ADDR					100.0						
Net		DDR3_A5	ADDR					100.0						
Net		DDR3_A6	ADDR					100.0						
Net		DDR3_A7	ADDR					100.0						
Net		DDR3_A8	ADDR					100.0						
Net		DDR3_A9	ADDR					100.0						
Net		DDR3_A10	ADDR					100.0						
Net		DDR3_A11	ADDR					100.0						
Net		DDR3_A12	ADDR					100.0						
Net		DDR3_A13	ADDR					100.0						
Net		DDR3_A14	ADDR					100.0						
DPr	M	DP_DDR3_DQS_0												
DPr	M	DP_DDR3_DQS_1												

The yellow column-headers indicate that DRC is disabled for that particular check. The yellow cells in the worksheet indicate that pass or fail cannot be determined, which is because the DRC check is off. At this point, there is no benefit of verifying the routing constraints on an unrouted design.

9. Close the Topology Workbench window without saving the topology.
10. Close Constraint Manager. Let Sigrity Aurora remain open and proceed to the steps covered in Post-layout Routed Interconnect Extraction and Export of Topology Constraints.

4

Post-layout Routed Interconnect Extraction and Export of Topology Constraints

As demonstrated in Pre-layout Extraction and Export of Topology Constraints, extracting a net from Allegro (or Constraint Manager) can be easier than building a topology from scratch.

In this chapter, you will learn:

- How to extract a post-layout routed interconnect into Topology Workbench
- How to use this topology to create a constraint set for the board

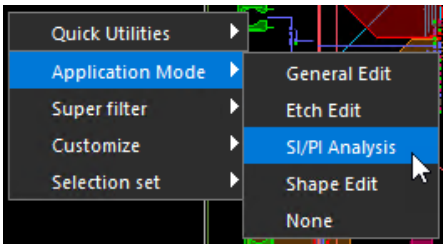
Extract Topology from Constraint Manager

1. In the Sigrity Aurora window, use the *File – Open* menu to open the `postlayout_Module1.brd` file from the following directory:

   `<INSTALL_DIR>\share\topxp\Tutorials\SIE_Tutorial`

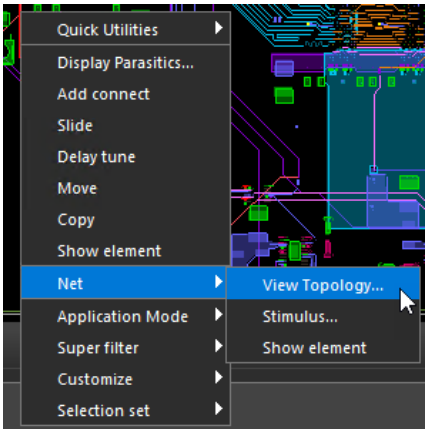
   Note: You need not save the `.brd` that is already open from the previous chapter.

2. Right-click anywhere on the canvas to open the shortcut menu and select *Application Mode – SI/PI Analysis*.

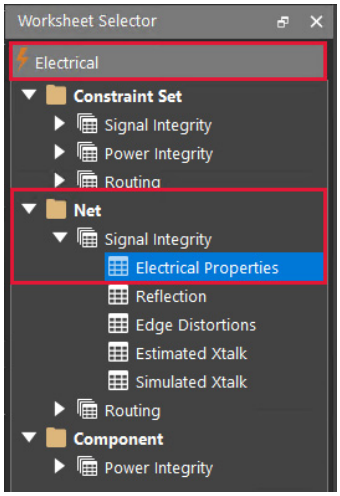


   Note: Alternatively, choose *Setup – Application Mode – SI/PI Analysis*.

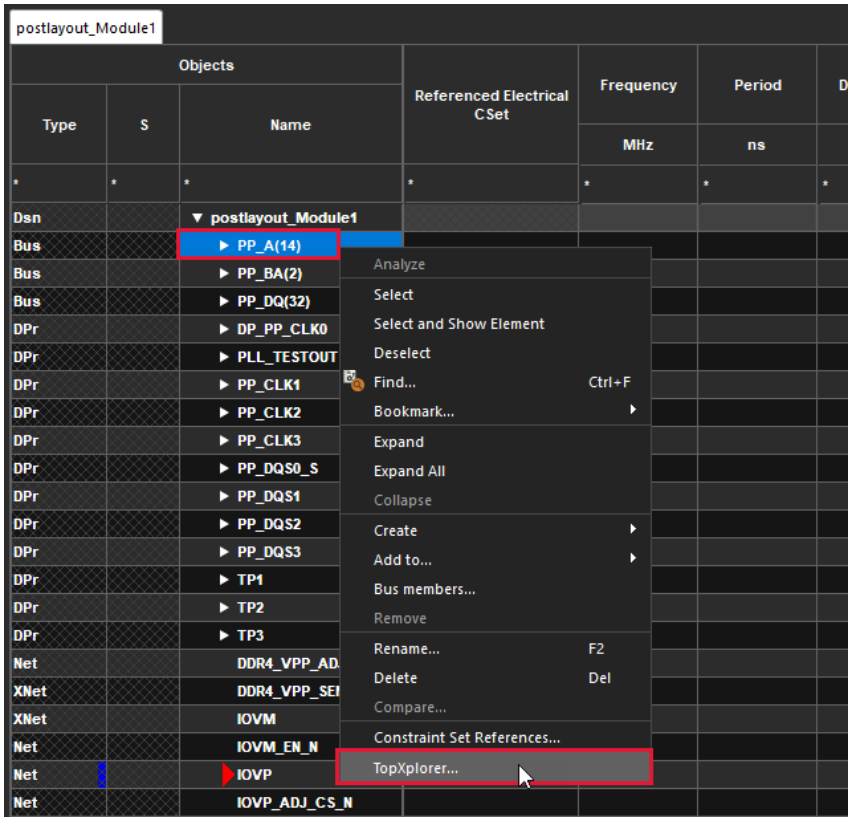
When this *Application Mode* is enabled, you can select a net and use the *Net – View Topology* shortcut menu as shown below:



3. Restart Constraint Manager from Sigrity Aurora using *Setup – Constraints – Constraint Manager*. The *Allegro Constraint Manager* window opens.
4. Click *Tools – Options* from the Constraint Manager menu bar. The *Options* dialog box opens.
5. Ensure that the *Automatic topology update* check box is selected.
6. Click *OK* to apply the changes and close the *Options* dialog box.
7. Open the *Electrical* module in the *Worksheet Selector* pane and select *Net – Signal Integrity – Electrical Properties*. The right pane displays the corresponding worksheet.

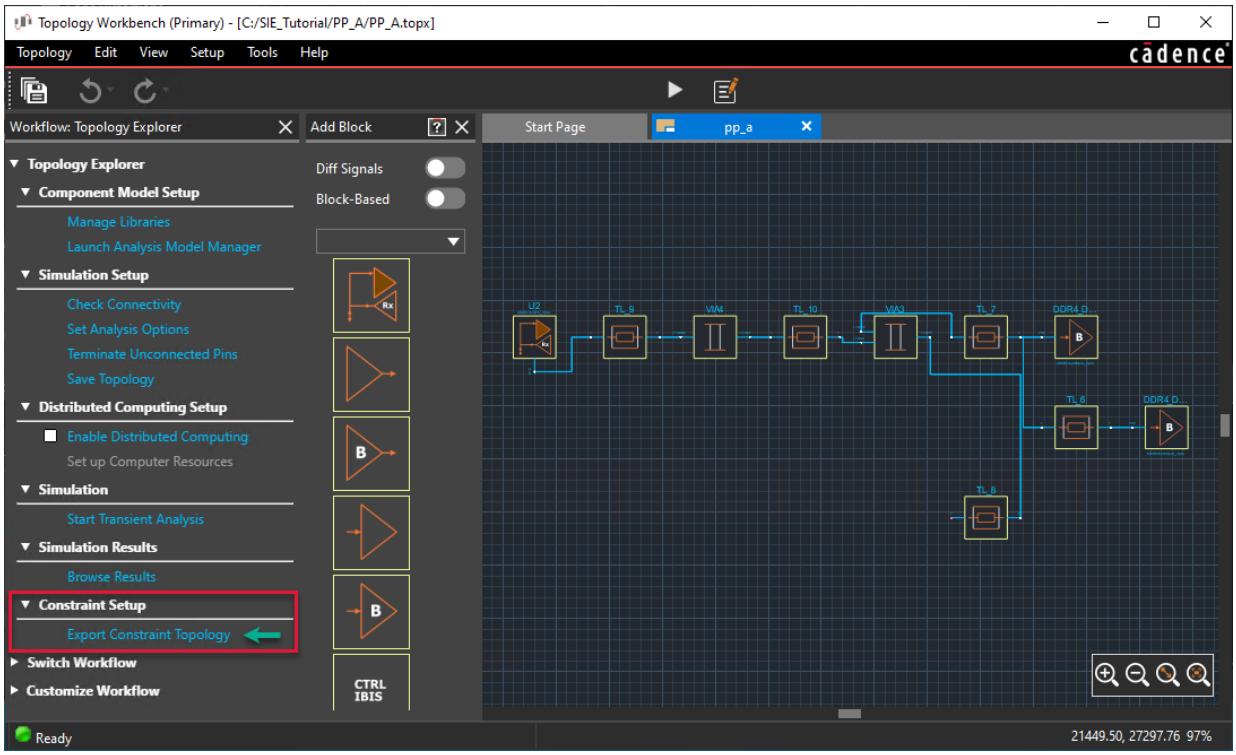


8. Right-click the *Pp_A(14)* bus and select *Explore Topology* from the displayed shortcut menu.



9. Ignore the message about discrete models by clicking *Yes* to continue. With the *Extract for simulation* option enabled in the *Options* dialog box, the topology is extracted to

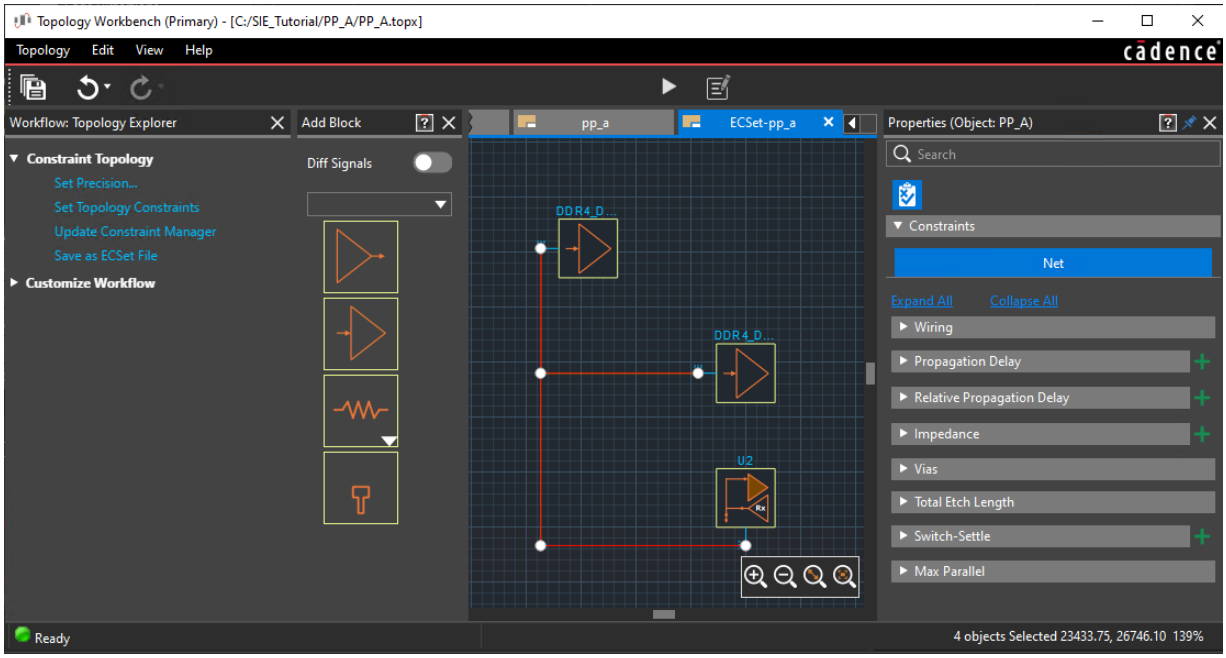
Topology Workbench in a tab named *pp_a* that opens in the Topology Explorer workflow for simulation.



10. Select *Export Constraint Topology* from the *Constraint Setup* schema of the *Workflow* panel in Topology Workbench.

A new tab with a name of the format *ECSet-<TopologyName>* opens within the Topology Workbench window, such as, *ECSet-pp_a* in case of this tutorial. The

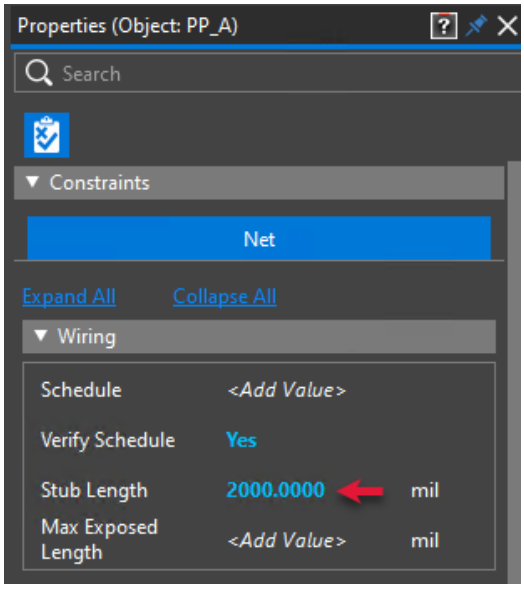
associated options in the *Workflow* panel allow you to set up the constraint topology for the extracted ECSet topology. The *Properties (Object : PP_A)* panel is also displayed.



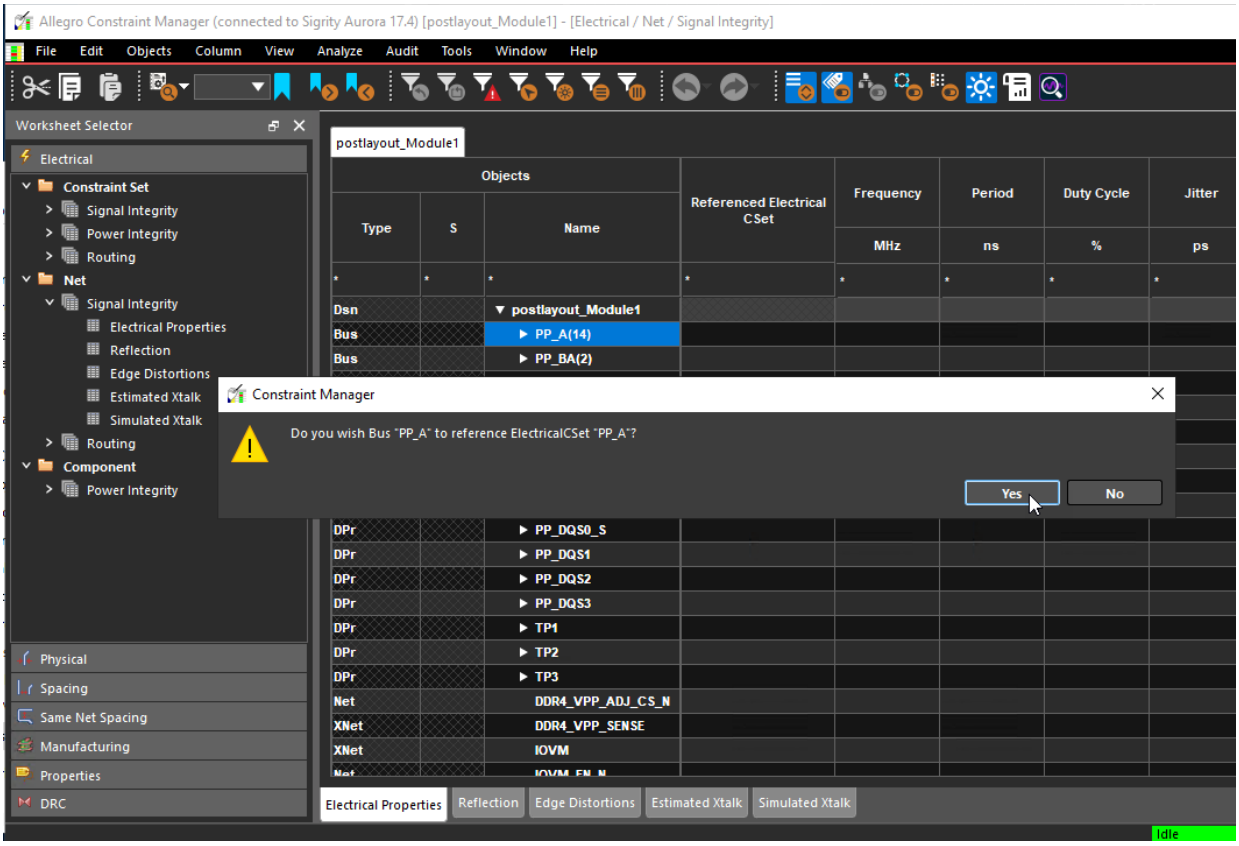
11. Click *Set Topology Constraints* in the *Workflow* panel.

12. Click the *Wiring* schema in the *Properties* panel to expand and view the existing constraints.

13. Reset the *Stub Length* value to *2000* mil.

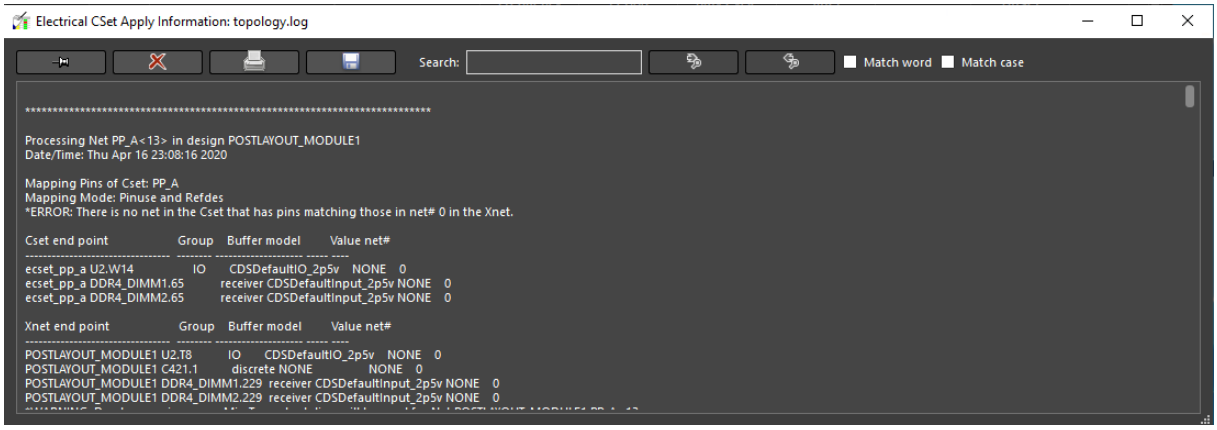


14. Click *Update Constraint Manager* in the *Workflow* panel. The Allegro Constraint Manager window comes to the foreground again and a message prompts you to confirm if you want to assign the topology to the entire class.



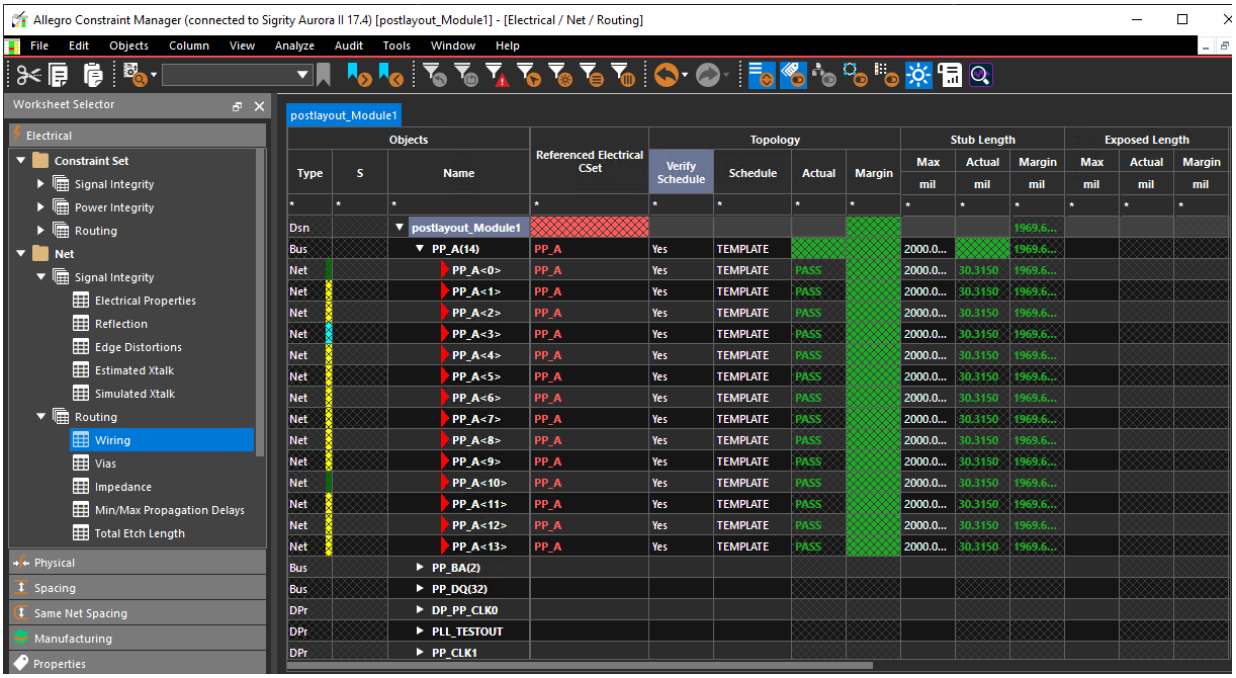
15. Click *Yes* in the message box. Extracting a topology at the class-level means that it can be easily applied to all members of the class after it has been constrained.

16. Close the *Electrical CSet Apply Information topology log* window that opens. In the background, a `.top` file is generated to pass back to the Constraint Manager.



17. Click *Net – Routing – Wiring* in the *Electrical* module of the *Worksheet Selector* pane.

18. Expand the *PP_A(14)* node in the *Objects* column and notice that the table has been updated with the *Referenced Electrical CSet* information as you had set in Topology Workbench. As can be seen in the example below, the *Stub Length – Max* column shows `2000 mil` to match the settings you updated in step 13. The *Actual* and *Margin* columns too show the updated calculations. The *Topology – Actual* column also displays *PASS* in green.



This brings this tutorial to an end. It demonstrated the method to get started with creating topologies in Topology Workbench and using it effectively in conjunction with Constraint Manager for extracting topologies and updating constraints like ECSet to be applied back to the design database.