

# **Topology Workbench User Guide**

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# Preface

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This document provides information about using Cadence® Sigrity™ Topology Workbench for performing automated die-to-die signal integrity (SI) analysis and power integrity (PI) analysis.

The Topology Workbench has the following three main modes to perform the required type of SI analysis:

- ***Topology Explorer*** for exploring end-to-end signal integrity of topologies
- ***Serial Link Analysis*** (SLA) for chip-to-chip analysis solution that focuses on high-speed SerDes designs, such as PCI Express® (PCIe®), HDMI, SFP+, XauI, Infiniband, SAS, SATA, and USB
- ***Parallel Bus Analysis*** (PBA) for source-synchronous parallel interfaces such as designs with DDRx memory

In addition, the Topology Workbench interface provides the ***SystemPI*** workflow for model-based topology environment to perform alternating current (AC), direct current (DC), and time domain power integrity analysis.

## Organization of this Document

This document covers the conceptual and workflow information in the following main topics:

<u>Getting Started with Topology Workbench</u>	
	Covers generic information about Topology Workbench, the different types of available product choices, and the supported workflows. It also familiarizes you with the Topology Workbench graphical user interface and common customizations that you can do in the view.
<u>Working with Topologies</u>	
	Describes the process of creating and configuring a topology project in all supported workflows. It also describes the common tasks involved in setting up a topology's properties.

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<u>Preparing for a Simulation Run</u>	Describes the process of setting up the topology for a simulation run.
<u>Running a Simulation and Analyzing the Results</u>	Covers information about running the simulation and reviewing the results in the dedicated result tabs, such as, 2D Curves, Eye Density, and Channel Report.
<u>Using Topology Explorer Workflow</u>	Describes the procedural details related to the Topology Explorer workflow.
<u>Using Serial Link Analysis Workflow</u>	Describes the procedural details related to the SLA workflow.
<u>Using Parallel Bus Analysis Workflow</u>	Describes the procedural details related to the PBA workflow.
<u>Working with Compliance Kits</u>	Covers information about using the standard built-in Compliance Kits available in the installation hierarchy and creating customized Compliance Kits. Also explains the frequency-domain compliance kit that OpenPOWER partners can use to determine if their high-speed serial (HSS) bus designs are compliant with IBM standards.
<u>Using the AMI Builder</u>	Describes the procedural details related to the AMI Builder.
<u>Using SystemPI Workflow</u>	Describes the procedural details related to the different SystemPI workflows.
<u>Exporting Constraints from a Topology</u>	Describes the procedural details related to exporting a topology to Constraint Manager.
<u>Using Optimality with Topology Workbench</u>	Covers information about using the Optimality Intelligence System Explorer to perform parameter optimization in Topology Workbench.

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<u>Choosing Blocks to Place on the Canvas</u>	
	Covers information about the various types of blocks that are available in the floating toolbar depending on the workflow in use.
<u>Using the Via Wizard</u>	
	Introduces the usage of the Via Wizard to generate coupled via structures in pre-layout phase.
<u>Modeling Pre-Layout Transmission Lines</u>	
	Covers information about the pre-layout transmission line (TLine) modeling capability.
<u>Using Extracted Interconnect Models from Layout</u>	
	Explains the Layout Association functionality that provides direct integration of Topology Workbench with PowerSI and SPEDEDM Generator (SPDGEN).
<u>Using the Sweep Manager</u>	
	Covers information about how the Sweep Manager lets you explore the effects of different values of a parameter on the signal integrity performance of the topology.
<u>Incorporating Crosstalk for Channel Analysis</u>	
	Explains the different crosstalk capabilities that are supported and facilitates you with information to select the desired approach for including crosstalk effects in your serial link analyses.
<u>Setting Timing Parameters in Topology Workbench</u>	
	Describes the concepts required to understand the impact of timing parameters that are specified in the <i>Timing Budget</i> panel for different types of buses. This functionality is supported in Parallel Bus Analysis (PBA) workflow.
<u>Reporting DDR Measurements</u>	
	Describes the extensive DDR data processing and specification compliance functionality that is supported in the Topology Explorer and PBA workflow.

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#### Adding Channel Simulator Controls

Explains the common *Channel Simulator Controls* that let the expert users pass specific global controls to a channel simulator. This functionality is supported in the channel-based topologies in the SLA and PBA workflows.

## Related Documents

In addition to the Topology Workbench User Guide, you can refer to the following documents:

### Tutorials

- [Topology Workbench: Topology Explorer Tutorial](#)

This tutorial captures the step-by-step instructions on exploring the Topology Workbench canvas, creating a topology from scratch, doing pre-layout extraction and post-layout routed interconnect extraction, and updating the ECSet using Constraint Manager.

- [Topology Workbench: Parallel Bus Analysis Tutorial](#)

This tutorial covers typical steps you will perform to create, edit, and simulate a parallel bus interface by using a default template from the install hierarchy and by creating a topology from scratch.

### Frequently Asked Questions

- [Topology Workbench Frequently Asked Questions](#)

This document can be read to find answers to a few commonly encountered questions related to Topology Workbench.

### References

- [Topology Workbench Tcl Command Reference](#)

This reference manual covers some useful Tcl commands that can be run in the *Command Window* panel of the Topology Workbench window.

## Additional Learning Resources

Cadence offers training courses that enable you to understand the applications better. For specific information about the courses available in your region, visit [Cadence Training](#) or write to [training\\_enroll@cadence.com](mailto:training_enroll@cadence.com).

## Customer Support

For assistance with Cadence products:

- Contact Cadence Customer Support

Cadence is committed to keeping your design teams productive by providing answers to technical questions and to any queries about the latest software updates and training needs. For more information, visit: <https://www.cadence.com/support>

- Log on to Cadence Online Support

Customers with a maintenance contract with Cadence can obtain the latest information about various tools at: <https://support.cadence.com>

## Third Party Tools

To view the videos included in this documentation, you need:

- A *Cadence Online Support* login.
- Flash-enabled web browser, for example, Internet Explorer 5.0 or later, Netscape 6.0 or later, or Mozilla Firefox 1.6 or later. Alternatively, you can download Flash Player (version 6.0 or later) directly from the [Adobe](#) website.
- Speakers and a sound card for your computer (for videos with narration).

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# Getting Started with Topology Workbench

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Topology Workbench is an advanced SPICE-based simulation and analysis environment that enables exploring, identifying, and solving the adverse analog effects of high-speed digital systems. You can use Topology Workbench to go from performing simple signal integrity (SI) exploration all the way to analyzing the most advanced serial link interfaces. It is a comprehensive and flexible system analysis environment for accurately assessing high-speed, chip-to-chip system designs.

Topology Workbench utilizes various simulation engines to perform detailed design-oriented analysis of pre-routed and post-routed, high-speed parallel bus (DDRx) systems and serial link (SerDes) systems.

You can also use Topology Workbench to perform die-to-die analysis in pre-layout or post-layout phase, or anywhere in between. The tool also provides full support for building custom system-level topologies, performing AC power ripple analysis, and running time-domain transient simulations for power integrity (PI) analysis.

Topology Workbench is based on the System Capture architecture. This next-generation topology environment replaces both Sigrity System Explorer and Cadence SigXplorer tools from the previous releases.

The easy-to-use interface of Topology Workbench lets you visually:

- Construct or extract interconnect topologies for signals or Power Distribution Networks (PDNs).
- Run simulations or sweep multiple scenarios with a series of simulations.
- Generate reports to review results.
- Capture constraints to be passed back to the Allegro PCB/package layout environment.

This enables you to execute what-if scenarios on critical high-speed signals in your board, package, or system-in-package design.

You can define parameters for ideal transmission-line models (faster, but less accurate), trace models (slower, but more accurate), vias, and circuit elements that you add to your topology. You can also define IO cell stimulus to drive simulations and specify what to measure.

You can capture the constraints that you set in a topology file, and then export it to Constraint Manager for importing as an Electrical Constraint Set (ECSet). This ECSet can then be applied to similar nets in your design, such as members of a bus.

To enable simulation of transistor-level IO models, Topology Workbench supports the Sigrity SPDSIM, SPECTRE, and HSPICE circuit simulators. Interconnects such as connectors and cables can also be included with S-Parameter data, or SPICE compatible circuit models. Synchronous design performance metrics including eye diagrams with detailed timing measurements are available as outputs.

### ***Related Topics***

- [Prerequisites for Running Topology Workbench and Other SystemSI Products](#)
- [Starting Topology Workbench](#)
- [Exploring the Topology Workbench Interface](#)
- [Identifying the Topology Workbench Workflow to Use](#)
- [Using Topology Workbench Optimally](#)
- [Customizing the View of Canvas and Windows](#)

## **Prerequisites for Running Topology Workbench and Other SystemSI Products**

To use Topology Workbench and other SystemSI products, you must install the compatible versions of the following two releases:

- Sigrity
- OrCAD® and Allegro

**Note:** For the compatibility matrix of these two releases, see README\_CCR.txt in the OrCAD/Allegro 23.1 (SPB231) page at [downloads.cadence.com](https://downloads.cadence.com).

Having both these releases is essential to access the latest Sigrity engines and functionality.

On Windows, when you install a Sigriity release, the installer automatically sets the SIGRITY\_EDA\_DIR environment variable to point to the Sigriity installation directory. However, on Linux, you need to manually set this environment variable after the installation.

On both Windows and Linux, the SIGRITY\_EDA\_DIR environment variable can also be defined in the Allegro environment file available in the pcbenv/env directory. In this case, the definition in the Allegro environment file takes precedence over the operating system-level settings.

Alternatively, during an active Topology Workbench session, you can set the path to the Sigriity installation directory using the `setSigriityEDADir` Tcl command. However, setting this Tcl command effects only the current session. Therefore, use of the SIGRITY\_EDA\_DIR environment variable is recommended.

### ***Related Topics***

- [setSigriityEDADir](#)
- [Getting Started with Topology Workbench](#)
- [Starting Topology Workbench](#)
- [Exploring the Topology Workbench Interface](#)
- [Identifying the Topology Workbench Workflow to Use](#)
- [Using Topology Workbench Optimally](#)
- [Customizing the View of Canvas and Windows](#)

## **Starting Topology Workbench**

You can start Topology Workbench as a standalone application or by extracting a topology from a layout tool, such as, Constraint Manager.

### ***Related Topics***

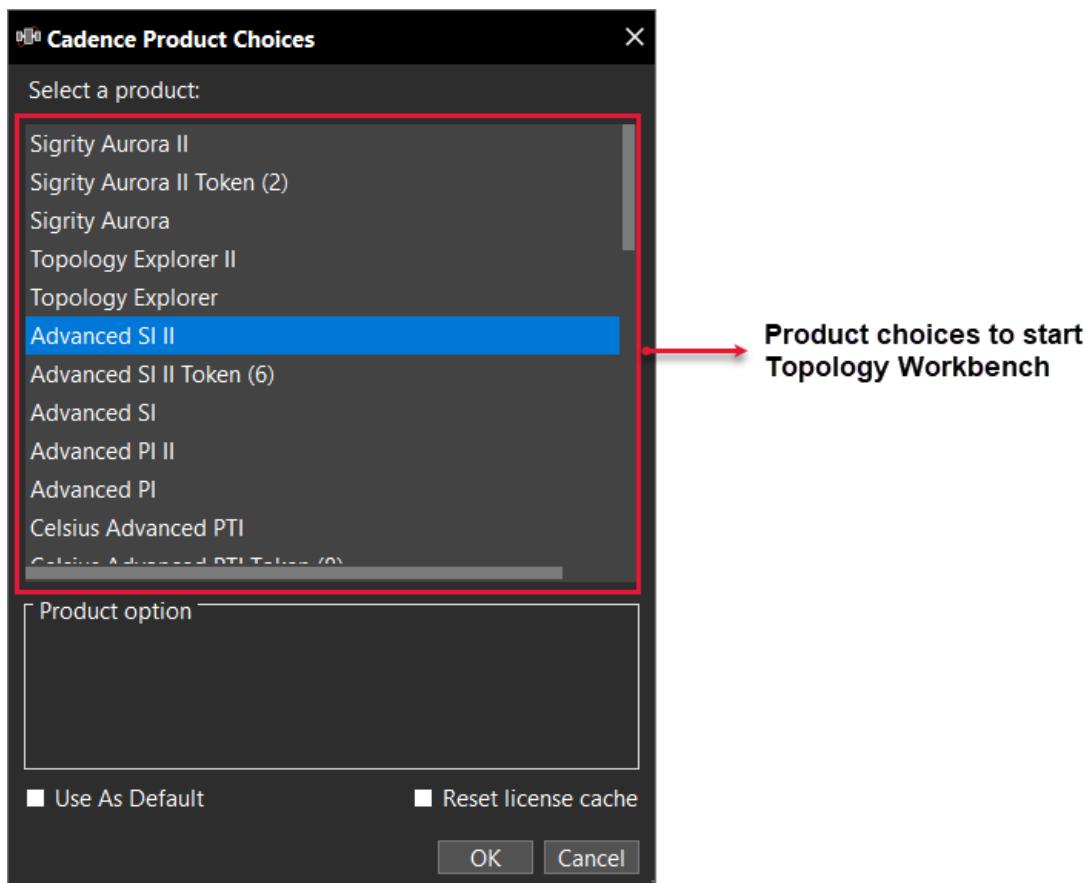
- [Opening Topology Workbench in Standalone Mode](#)
- [Opening Topology Workbench by Extracting a Topology](#)
- [Getting Started with Topology Workbench](#)
- [Prerequisites for Running Topology Workbench and Other SystemSI Products](#)

## Opening Topology Workbench in Standalone Mode

To open Topology Workbench in standalone mode:

- In Windows, use one of the following ways:
  - Click *Start – Run*, and type `TopWb`
  - Click *Start – Cadence System Analysis <release\_number> – Sigriity Topology Workbench <release\_number>*
- or-
- In UNIX, type `TopWb` in a Shell window and press `Enter`.

The *Cadence Product Choices* dialog box as shown below is displayed with a list of products for which you own the licenses.



The dialog box also has the following check boxes:

- *Use As Default* to save your product preference for the next run

- *Reset license cache* to query the server and update the list of available licenses

To start Topology Workbench in standalone mode, select one of the available product choices and then click *OK*. Use the following mnemonics to identify an appropriate product:

- **Topology Explorer II** and **Topology Explorer** for sandbox-style general SI analysis
- **Advanced PI II** and **Advanced PI** to use a model-based topology environment that enables alternating current (AC), direct current (DC), and time domain power integrity analysis

**Note:** To start Advanced PI-specific workflows in UNIX, type `TopWb -systempi` in the Shell window. In Windows, you can click *Start – Programs – Cadence System Analysis <release\_number> – Sigrity SystemPI*.

- **Advanced SI II** and **Advanced SI** to focus on analyzing advanced source-synchronous parallel buses (for example, DDR) and serial link interfaces (for example, PCI Express)

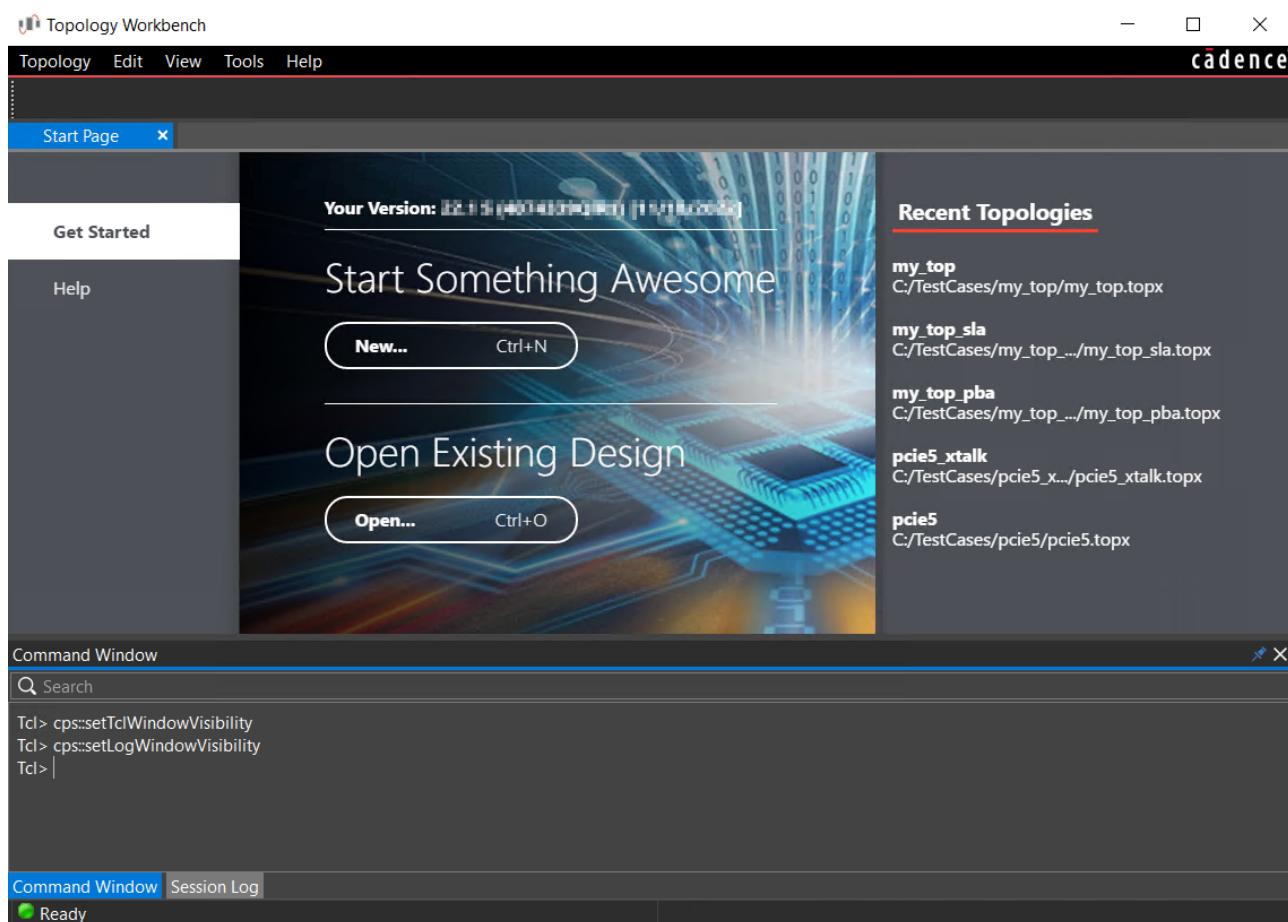
**Note:** To start Advanced SI-specific workflows in UNIX, type `TopWb -systemsii` in the Shell window. In Windows, you can click *Start – Programs – Cadence System Analysis <release\_number> – Sigrity SystemSI*.

- **Advanced IBIS Modeling II** and **Advanced IBIS Modeling** to develop I/O Buffer Information Specification (IBIS) models, including Algorithmic Modeling Interface (AMI) functionality for equalization

# Topology Workbench User Guide

## Getting Started with Topology Workbench

The Topology Workbench window opens with the *Start Page* tab in focus.



### Related Topics

- [Starting Topology Workbench](#)
- [Opening Topology Workbench by Extracting a Topology](#)

## Opening Topology Workbench by Extracting a Topology

You can extract a topology from the Allegro tools through Constraint Manager or from Sigrity Aurora. The extracted topology opens in the Topology Explorer workflow of Topology Workbench.



To enable this feature, set the `CDS_SUPPORT_TOPXP` environment variable to 1 before starting the Allegro tools.

The topics below cover the steps involved in topology extraction.

## From Constraint Manager

You can use Constraint Manager with Topology Workbench to explore circuit topologies and derive electrical constraint sets that can include custom constraints, custom measurements, and custom stimulus. The resulting topology template data can also be imported into Constraint Manager as an ECSet.

To export a constraint topology from Constraint Manager to Topology Workbench:

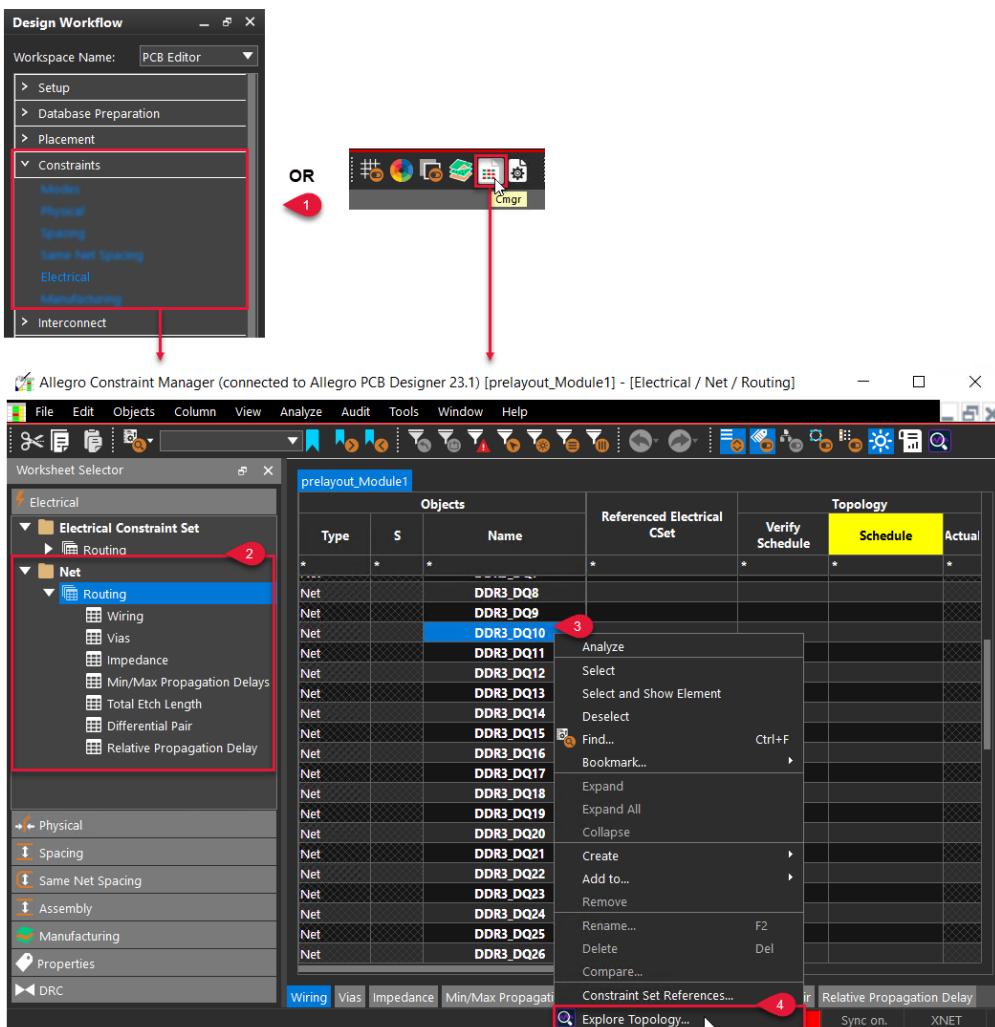
1. Open Constraint Manager using one of the following methods:

- Choose *Constraints – Electrical* from the *Design Workflow* pane on an Allegro tool.

# Topology Workbench User Guide

## Getting Started with Topology Workbench

- Choose  from the toolbar.

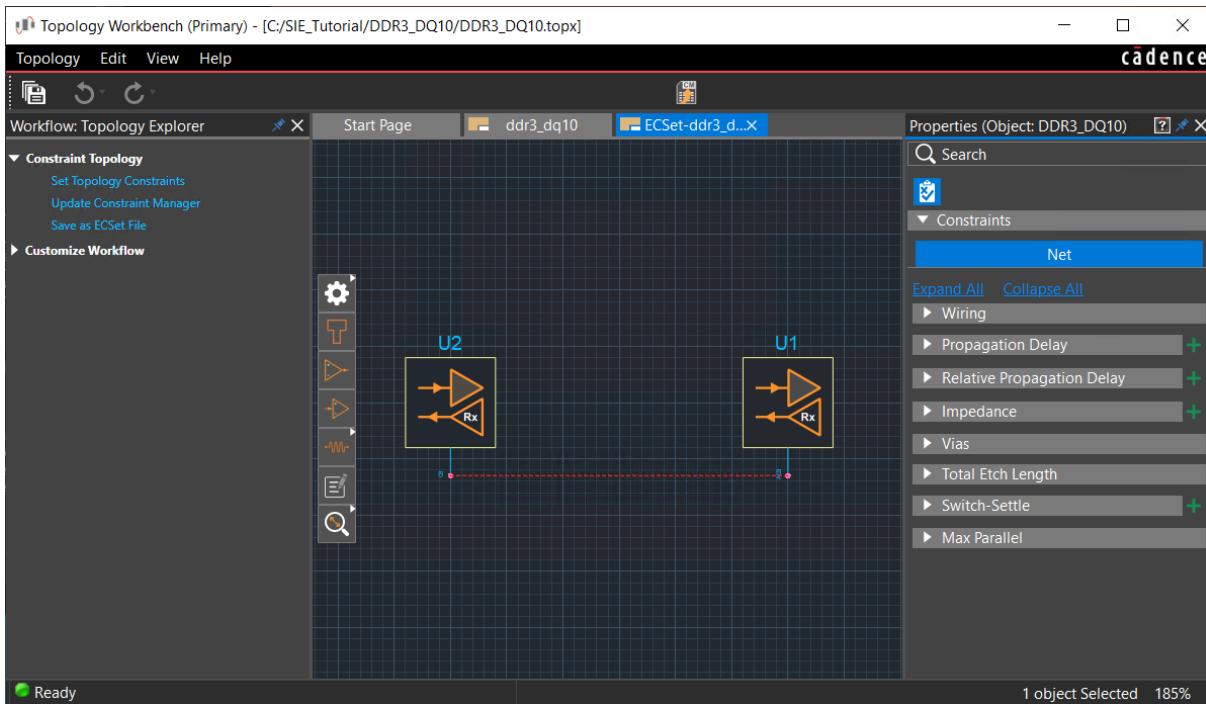


- Click **Net – Routing** from the *Worksheet Selector* pane in Constraint Manager. The worksheet corresponding to the selected option is displayed in the right pane.
- Right-click the net of the topology you want to extract. The shortcut menu is displayed.
- Choose *Explorer Topology...* from the shortcut menu options.

# Topology Workbench User Guide

## Getting Started with Topology Workbench

The topology of the selected net is extracted to the Topology Workbench window in two tabs, *<net\_name>* and *ECSet-<net\_name>*.



The workflow panel in the *<net\_name>* tab lets you run transient analysis for the extracted net using the Topology Explorer workflow.

In the *ECSet-<net\_name>* tab, you can set topology constraints, save the topology as a ECSet file, and update the Constraint Manager for the extracted net. In addition, the floating toolbar contains:

- Settings to toggle adding of blocks with differential signals
- Options to add blocks of the following types to the topology: TPoint, transmitter, receiver, resistor, inductor, capacitor, diode, and Vdc
- Option to add notes
- Controls to zoom in, zoom out, zoom fit, and zoom by points

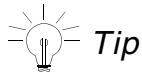
## From Sigrity Aurora

If you have a Sigrity Aurora license, you can export a topology for SI analysis in Topology Workbench as described below:

### 1. Open Sigrity Aurora.

# Topology Workbench User Guide

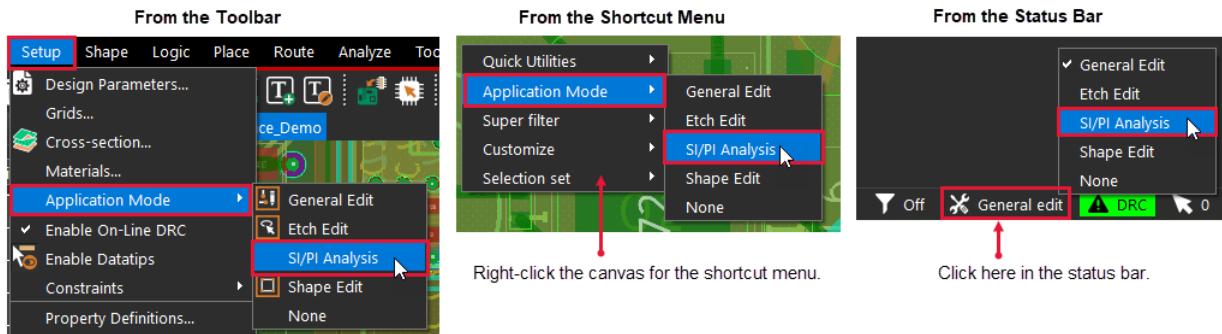
## Getting Started with Topology Workbench



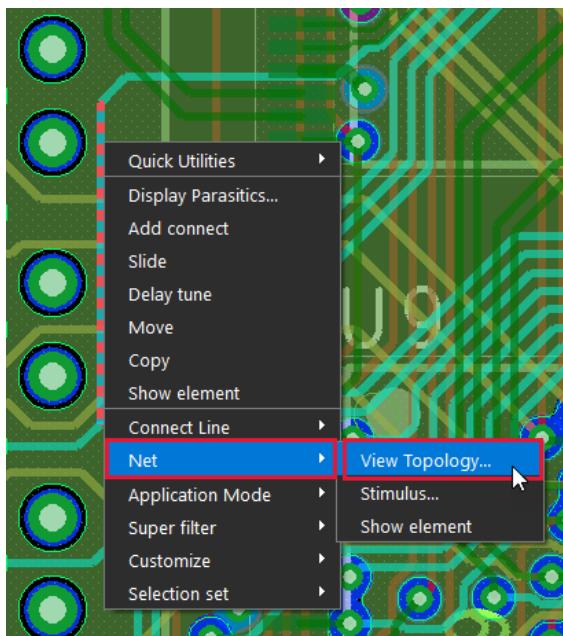
Start Allegro, select *Sigrity Aurora II* or *Sigrity Aurora* from the license window, and click *OK*. The Sigrity Aurora window opens.

2. Open a .brd file in Sigrity Aurora.
3. Choose *Setup – Application Mode – SI/PI Analysis*.

Alternatively, you can change this setting from the shortcut menu accessed by right-click on the layout canvas or from the status bar of the Sigrity Aurora window as shown below.



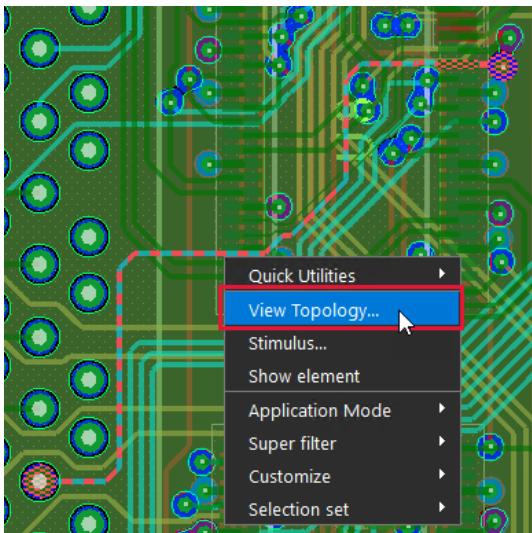
4. Click or place the cursor on the net for which the topology needs to be exported to Topology Workbench.
5. Right-click to open the shortcut menu and choose *Net – View Topology*.



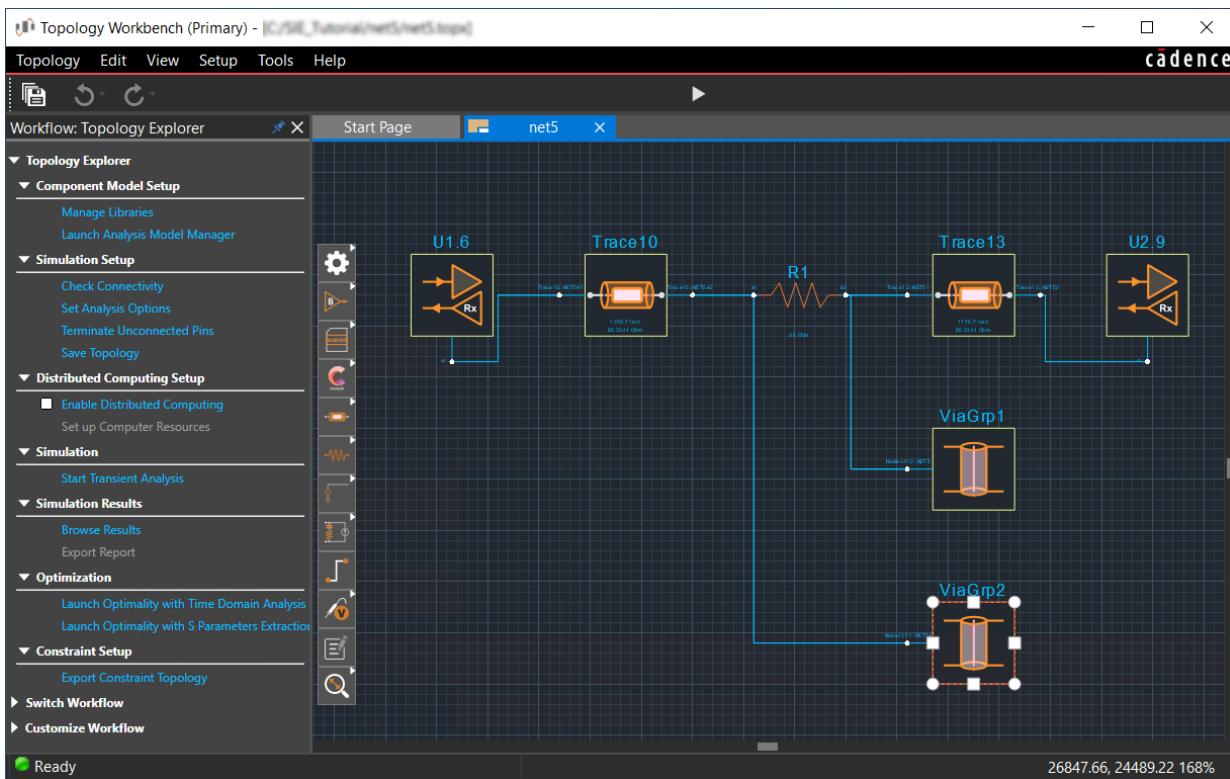
# Topology Workbench User Guide

## Getting Started with Topology Workbench

Alternatively, if you double-click a net, the entire bus to which it is associated with gets highlighted on the canvas. When you right-click this bus, the *View Topology* option is available at the first level itself of the shortcut menu as shown below:



Topology Workbench opens in the Topology Explorer workflow with the topology displayed in the canvas as shown below:

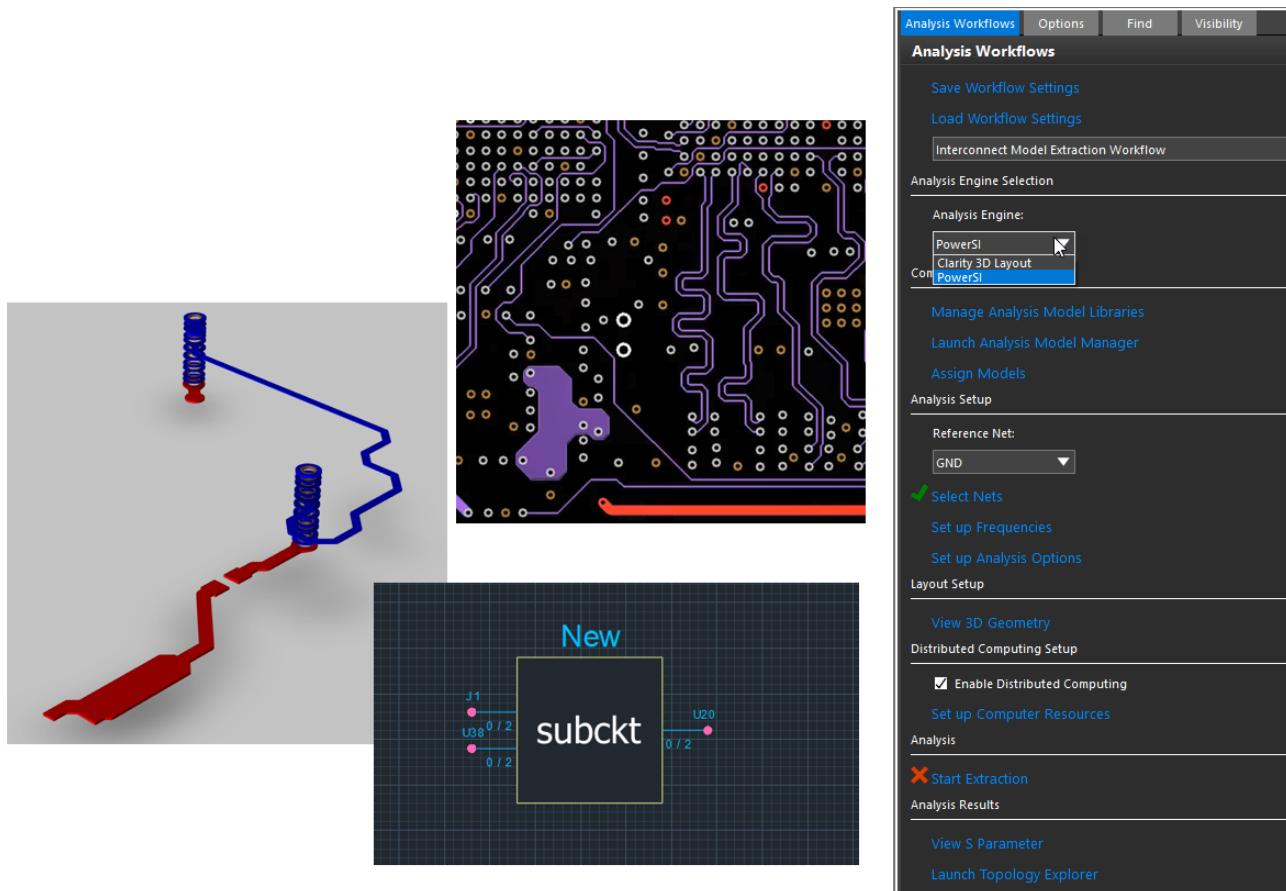


# Topology Workbench User Guide

## Getting Started with Topology Workbench

### Automated Extraction of Interconnect Models from Allegro Canvas

In Sigriy Aurora, you can choose to run *Interconnect Model Extraction Workflow* for simplified and automated extraction of interconnect models. This workflow is powered by Sigriy PowerSI and Clarity engines.



Users that are licensed to run Sigriy Aurora II and Sigriy PowerSI II and/or Clarity 3D Solver benefit from this integration when the latest compatible versions of following two releases are installed together:

- OrCAD® and Allegro®
- Sigriy and Systems Analysis

### Related Topics

- [Starting Topology Workbench](#)
- [Opening Topology Workbench in Standalone Mode](#)

- [Using Topology Explorer Workflow](#)
- [Exporting Constraints from a Topology](#)

## Identifying the Topology Workbench Workflow to Use

The selection you make in the *Cadence Product Choices* dialog box defines the workflows you will be able to work with. The following table enumerates the workflows supported for each product choice:

Product Choice	Supported Workflows
<i>Topology Explorer II</i>	<a href="#"><u>Topology Explorer</u></a>
<i>Topology Explorer</i>	
<i>Advanced PI II</i>	<a href="#"><u>SystemPI</u></a>
<i>Advanced SI II</i>	<a href="#"><u>Topology Explorer</u></a> , <a href="#"><u>Parallel Bus Analysis (PBA)</u></a> , <a href="#"><u>Serial Link Analysis (SLA)</u></a> , <a href="#"><u>Compliance Kits</u></a> , <a href="#"><u>AMI Builder</u></a>
<i>Advanced SI</i>	
<i>Advanced IBIS Modeling II</i>	<a href="#"><u>Topology Explorer</u></a> , <a href="#"><u>PBA</u></a> , <a href="#"><u>SLA</u></a> , <a href="#"><u>Compliance Kits</u></a> , <a href="#"><u>AMI Builder</u></a>
<i>Advanced IBIS Modeling</i>	

### Topology Explorer

The Topology Explorer workflow is targeted for general-purpose signal integrity analysis, optionally including non-ideal power effects. You can include complex interconnect models and connect them to a single driver/receiver/discrete symbol that automatically replicates the circuit for each of the ports on the interconnect model.

For detailed information, see [Using Topology Explorer Workflow](#).

### SystemPI

The SystemPI workflow involves taking extracted models for the power distribution network (PDN) of chip, package, and/or PCB, connecting them together, and applying a current source(s) excitation at the chip location. A transient circuit simulation is performed and the ensuing power ripple can be analyzed to verify that it remains within specification. It involves connecting together DC models for chip, package, and/or PCB. Sources and sinks are defined, and the DC circuit simulation is performed to determine if the IR drop at critical chip locations meets the chip specifications.

## Serial Link Analysis

The SLA workflow is a chip-to-chip solution that focuses on analysis of your high-speed SerDes designs, such as PCI Express® (PCIe®), HDMI, SFP+, Xaui, Infiniband, SAS, SATA, and USB. Support for industry-standard IBIS AMI transmitter and receiver models let you perform simulations of channel behavior for serial links with chips from multiple suppliers. For a chip model developer, SLA provides access to techniques that assist in IBIS-AMI model development. You can add models of multiple packages, connectors, and boards to reflect the entire channel. Simulations identify crosstalk issues and show the effectiveness of chip-level clock and data recovery (CDR) techniques. Full-channel simulations including millions of bits of data confirm overall bit-error rate (BER) to determine if jitter and noise levels are within specified tolerances.

For detailed information, see [Using Serial Link Analysis Workflow](#).

## Parallel Bus Analysis

The PBA workflow is an end-to-end solution that targets analysis of source-synchronous parallel interfaces such as designs with DDRx memory. Pre-layout capabilities enable you to begin with models that are quickly generated and connected. As the design is refined, more detailed models can be swapped in to reflect actual hardware behavior. Concurrent simulation accounts for the effects of dielectric and conductor losses, reflections, inter-symbol interference (ISI), crosstalk, and simultaneous switching noise. These simulations are able to fully account for the effects of non-ideal power-delivery systems. Graphical outputs and post-processing options give insight for rapid system improvements.

For detailed information, see [Using Parallel Bus Analysis Workflow](#).

## Compliance Kits

The Compliance Kits workflow automates the compliance testing process and supports quick identification of potential risks in high-speed SerDes designs, channels, and interfaces. It allows you to select the compliance criteria of interest, and easily generate a compliance report. The compliance kits workflow provide predefined templates that are ready-to-run as a starting point for compliance sign-off. IBIS-AMI models, when necessary, for transmitters and receivers are intended to represent specification-level functionality, and are developed according to the characteristics defined in the associated specification. This workflow provides typical interconnect topologies with example models in place that help you get started. These are not intended for detailed analysis, or to represent any specific reference standard.

For detailed information, see [Working with Compliance Kits](#).

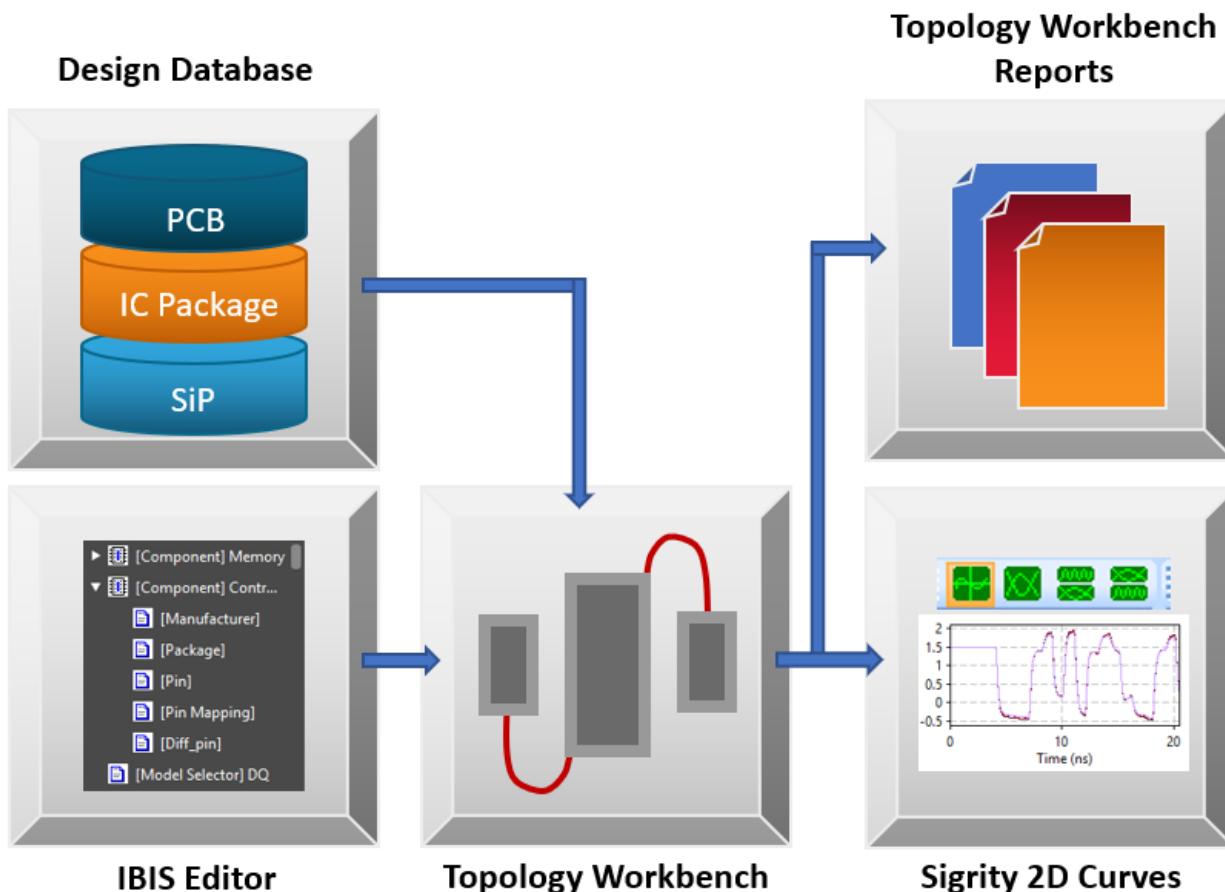
## AMI Builder

The AMI Builder workflow facilitates creation of AMI models. Such models can be generated for a particular IP that needs to be simulated, or to perform a 'what if' analysis and analyze whether a system would work with the given components. This workflow also helps to verify existing AMI models.

For detailed information, see [Using the AMI Builder](#).

## Using Topology Workbench Optimally

The following flow diagram shows how you can optimally use Topology Workbench along with the other tools for [Exploration](#), [Pre-Route Analysis](#), and [Post-Route Verification](#):



## Exploration

During exploration, your focus is on setting up access to libraries, developing signal models, and performing extensive *What-If* analysis. You may not have access to a design database, but you can speculate how a particular component and its interconnect will behave in your topology. You will simulate for reflection, crosstalk, and derive constraints, and then save them in a topology template file for later reuse.

**Tools Used:** Topology Workbench, Sigrity 2D Curves, and IBIS Editor

## Pre-Route Analysis

During pre-route analysis, your focus is on:

- Modeling a signal type for a PCB, Package, System-in-Package design, or a combination of those fabrics
- Modifying various components, pin buffers, and interconnect
- Setting a range of sweepable parameters to simulate them in the native simulator

Depending on the simulated results, you can decide to modify parameters, measurements, or simulation settings, or add a termination scheme. You can also use the imported cross-section, and modify it to see the effects on your topology. You capture constraints in a topology template file and import it to Constraint Manager as an Electrical Constraint Set (ECSet) to refresh the design.

**Note:** The Topology Workbench environment supports the HSPICE and SPECTRE simulation engines.

**Tools Used:** Topology Workbench, Sigrity 2D Curves, and IBIS Editor, Constraint Manager, and a PCB, Package, or SiP layout tool

## Post-Route Verification

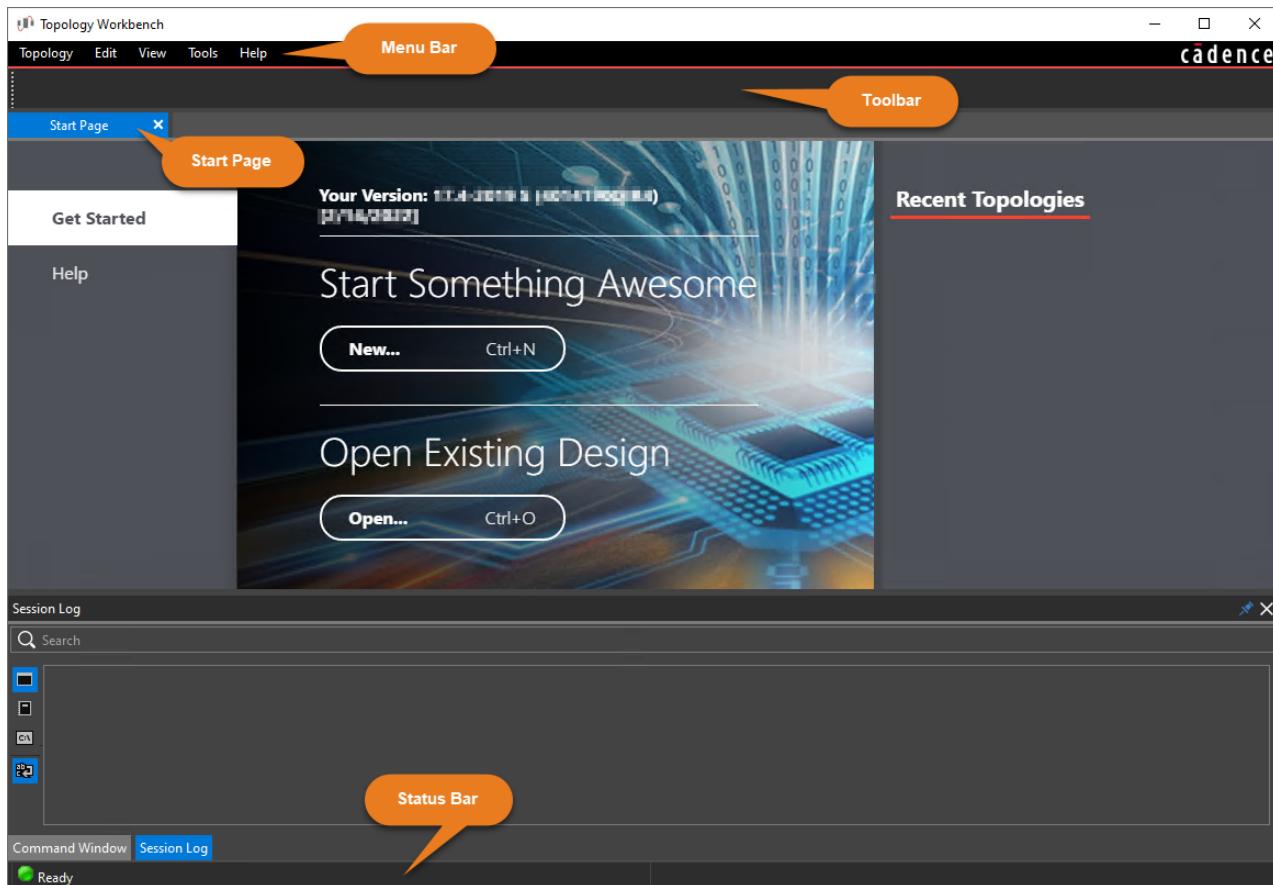
During post-route verification, your focus is on extracting signals from a PCB, Package, or SiP database (fully routed) and simulating the topology. You use the Results window of Topology Workbench, built-in reports, and Sigrity 2D Curves to verify that the integrity of the signal meets your requirements.

**Tools Used:** Topology Workbench and Sigrity 2D Curves

## Exploring the Topology Workbench Interface

When you open the Topology Workbench, the user interface of its start-up window consists of the following elements:

- Menu Bar
- Toolbar
- Start Page
- Status Bar



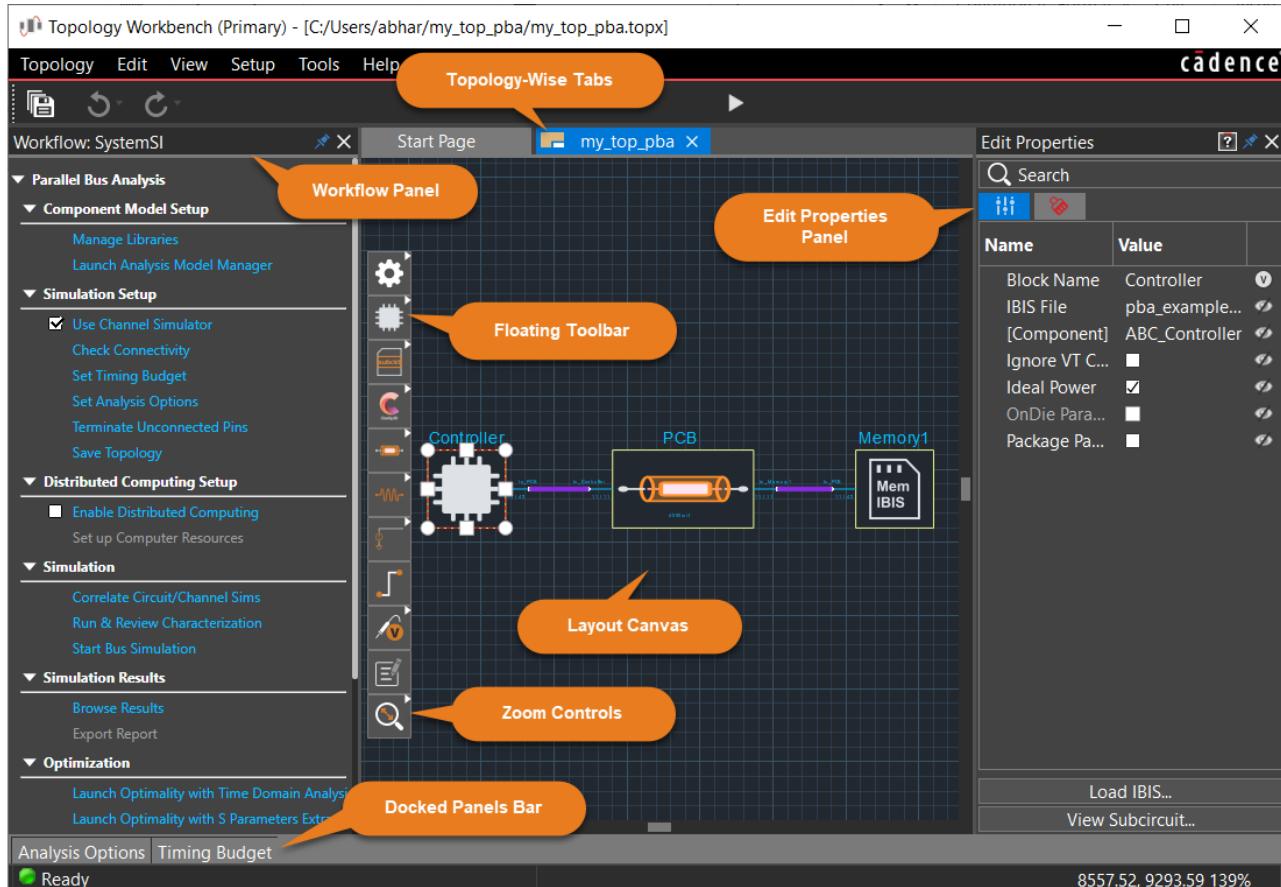
When you choose to create a new topology or to work with an existing one, the following items are added to the display:

- Workflow Panel
- Floating Toolbar
- Topology-Wise Tabs

# Topology Workbench User Guide

## Getting Started with Topology Workbench

- Layout Canvas
- Edit Properties Panel



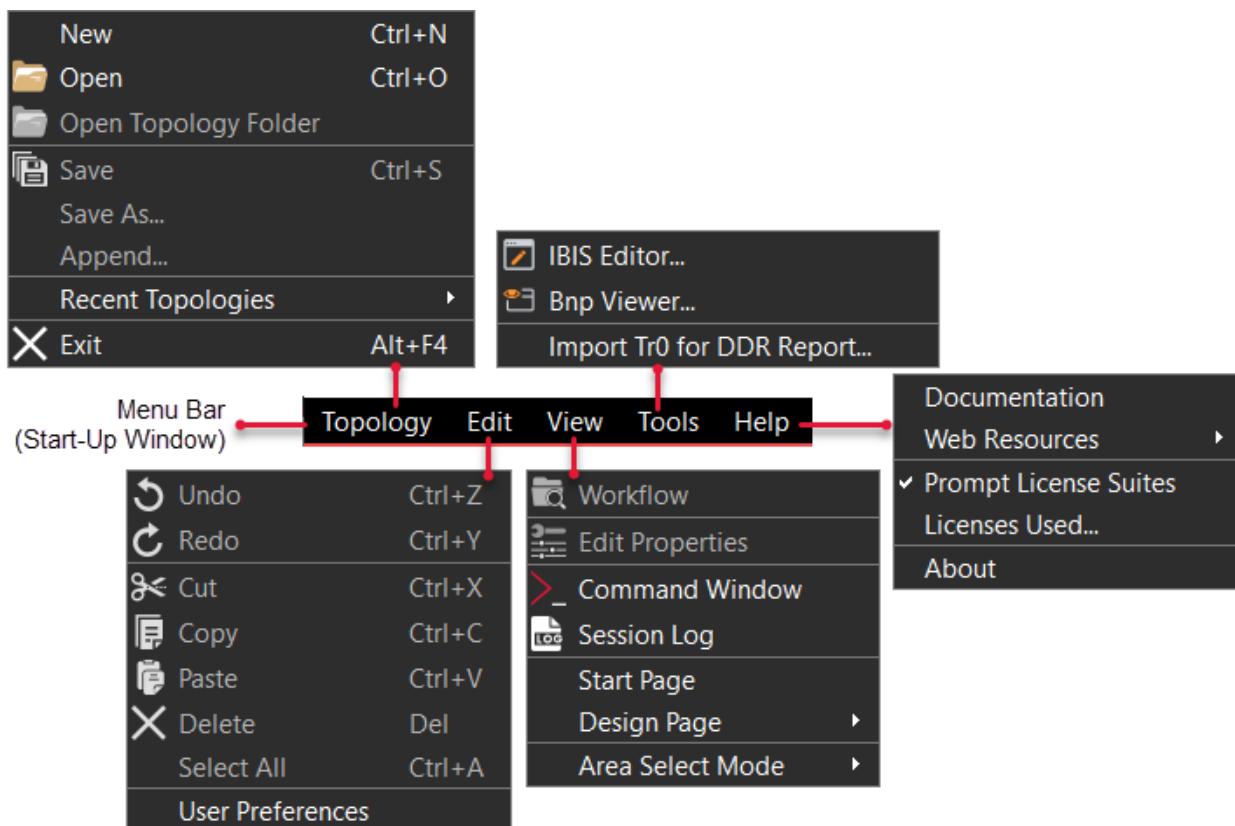
In addition, you can open the following panels from the docked panels bar at any time after Topology Workbench starts:

- Command Window Panel
- Session Log Panel

## Menu Bar

The Topology Workbench menu bar provides access to options that enable you to perform various operations on a design topology, such as opening and saving a topology, editing, and so on.

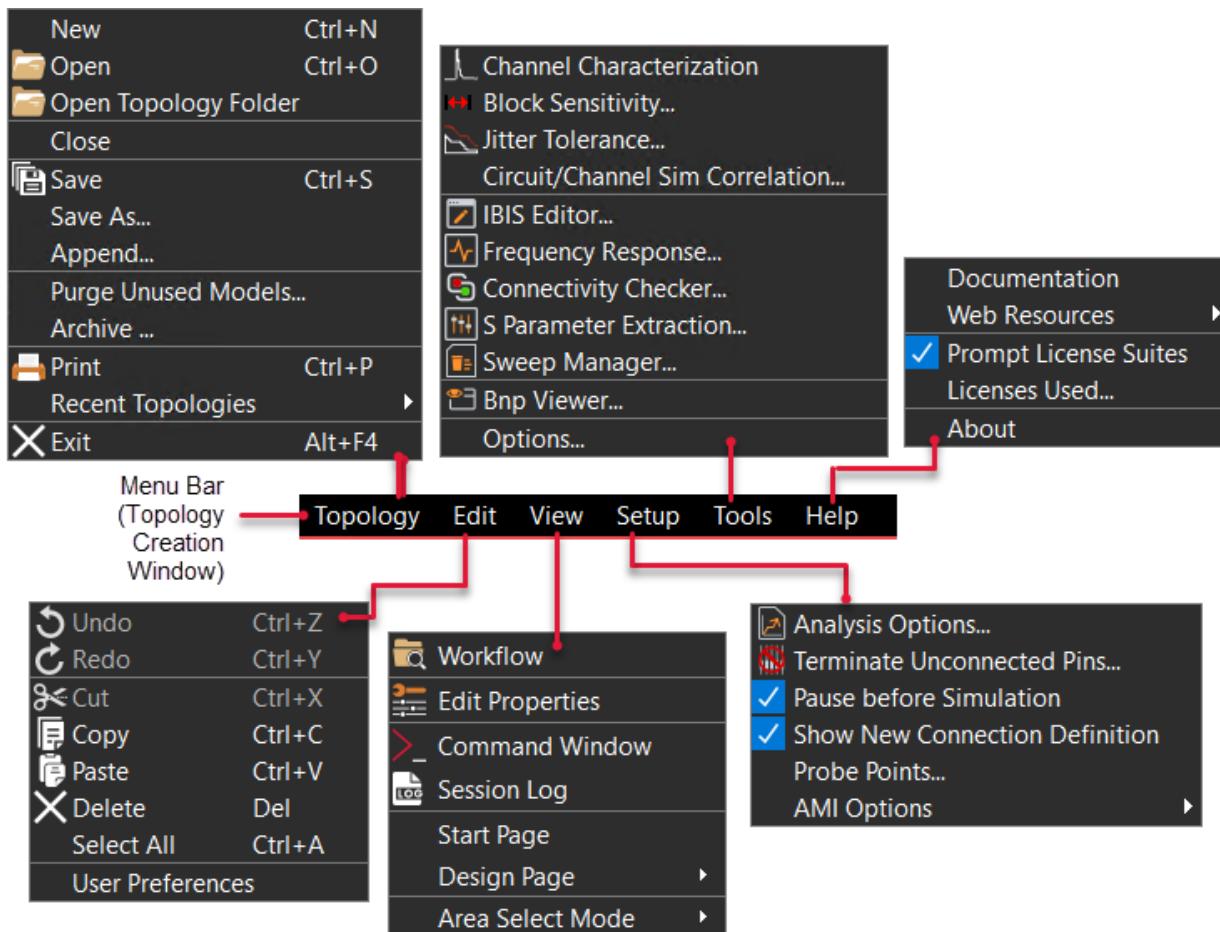
The menu bar in the Topology Workbench start-up window consists of the following menus:



# Topology Workbench User Guide

## Getting Started with Topology Workbench

When you open an existing topology or start to create a new topology, the menu bar provides additional menu options such as shown below. A few menu options might vary depending on the workflow used to open the project.



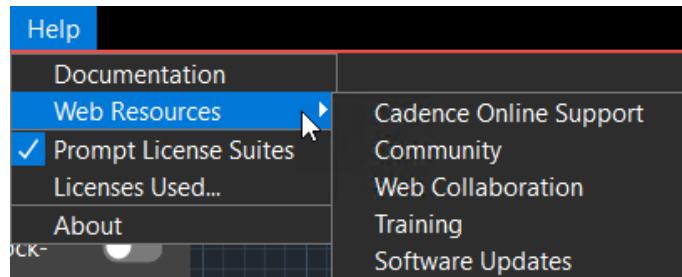
The *Tools* menu displays some generic tools that are common across workflows, such as *IBIS Editor*, *Connectivity Checker*, and *Sweep Manager*. It also displays workflow-specific tools, such as, *Timing Budget* and *Write Leveling* in PBA or *Block Sensitivity* in Custom Compliance Kit workflow.

In the *Help* menu, the *Licenses Used* option of shows the information about the licenses used for the current session of Topology Workbench. The *Prompt License Suites* option, which is selected by default, indicates to Topology Workbench that the Choose License Suites dialog box should be displayed when the environment is launched. You also have the

## Topology Workbench User Guide

### Getting Started with Topology Workbench

option to access useful Cadence Web Resources, such as, *Cadence Online Support*, *Community*, *Web Collaboration*, *Training*, and *Software Updates*.



## Toolbar

In the start-up window of Topology Workbench, all toolbar options are disabled. When you start to work with a topology, whether new or existing, the toolbar provides the options shown below:



## Start Page

The *Start Page* provides two tabs—*Get Started* and *Help*—in the left pane of the Topology Workbench window. Depending on the tab you select in the left pane, the items displayed in the middle pane and right pane change as described below:

Tab	Description
<i>Get Started</i>	<ul style="list-style-type: none"><li>■ Middle pane displays two buttons—<i>New</i> (to start a new topology) and <i>Open</i> (to open an existing topology).</li><li>■ Right pane displays a list of <i>Recent Topologies</i>.</li></ul>

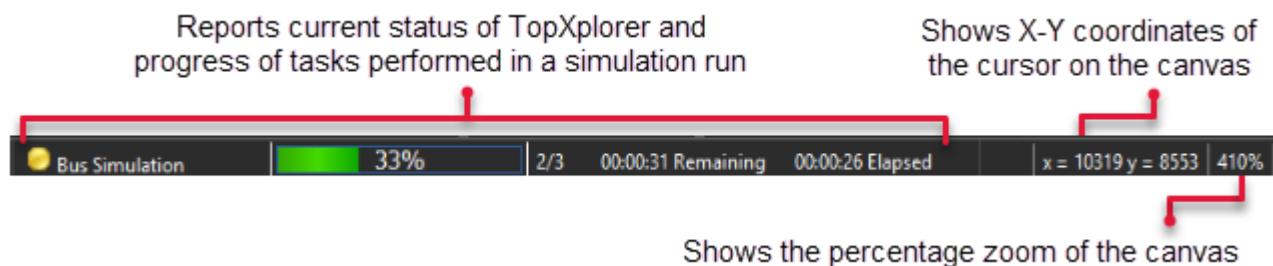
# Topology Workbench User Guide

## Getting Started with Topology Workbench

Tab	Description
Help	<ul style="list-style-type: none"><li>■ Middle pane displays buttons to open the user guide and tutorials.</li><li>■ Right pane displays a dynamic list of <i>FAQ</i> (to answer frequently asked questions and address common concerns).</li></ul>

## Status Bar

The status bar at the bottom of the Topology Workbench window shows the current status, progress, and contextual information, like the ones illustrated in the image below.



Controls and Contextual Information	Description
<i>Status and Progress</i>	
<i>Coordinates</i>	x = 11443 y = 8653
<i>Zoom Percentage</i>	116%

## Topology Workbench User Guide

### Getting Started with Topology Workbench

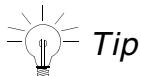
Controls and Contextual Information	Description	
<i>Minimized Panels</i>		Displays controls for each currently open, but minimized panel, such as, Connectivity Checker, Analysis Options, and Probe Points. When these controls are clicked, the corresponding panel is displayed again. You can also toggle between the minimized panels using these controls in the status bar.

## Workflow Panel

When you open a topology, the *Workflow* panel is visible by default. The contents of this panel depend on the workflow you have chosen for the topology. The standard options available in this panel include the following:

Schema	Description
<i>Component Model Setup</i>	Provides options to manage model libraries in Sigrity™ Analysis Model Manager (AMM).
<i>Topology Setup</i>	Provides options to terminate unconnected pins and save the topology.  <b>Note:</b> This schema option is available only in the SystemPI workflows.
<i>Simulation Setup</i>	Provides options to check connectivity, set analysis options, save the topology, and control other simulation setup requirements.  In the SystemPI workflows, this schema also lets you set up options for DC IR Drop Analysis and derive target impedance.
<i>Distributed Computing Setup</i>	Provides options to enable High Performance Computing (HPC) and set up the computer resources.  <b>Note:</b> This schema option is not available in the SystemPI workflows.
<i>Simulation</i>	Provides an option to run the simulation.
<i>Simulation Results</i>	Provides an option to browse the simulation results.
<i>Constraint Setup</i>	Provides an option to export constraints to the Allegro PCB / package design environment.

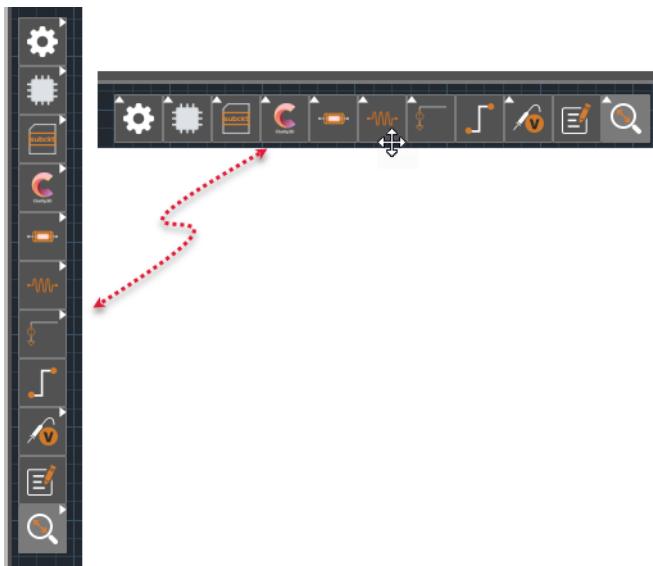
Schema	Description
<i>AMI Builder</i>	Provides options to define algorithmic models for Tx and Rx equalization for Advanced SI.
<i>Switch Workflow</i>	Provides options to switch from the current workflow to another supported workflow.
<i>Customize Workflow</i>	Provides options to edit the current workflow or to reset to the default workflow.



If the *Workflow* panel is not displayed, choose *View – Workflow* from the menu bar.

## Floating Toolbar

The floating toolbar in the main application window is by default aligned vertically and can be docked per convenience.



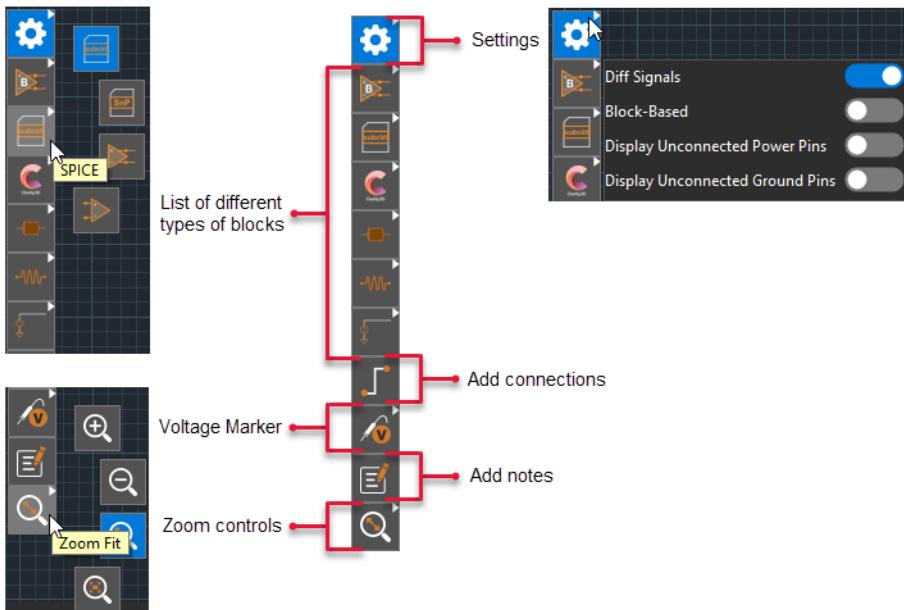
Controls on this toolbar help with design operations on the canvas, such as:

- Settings to enable display of options to add blocks of the following types:
  - Differential signals
  - Single-ended, block-based signals
- Settings to enable display of unconnected power and ground pins

# Topology Workbench User Guide

## Getting Started with Topology Workbench

- Controls to add different types of blocks that are supported in the active workflow
- Options to add connections between the blocks, add voltage markers, and add notes in the topology
- Controls to zoom in, zoom out, zoom fit, and zoom by points

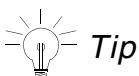
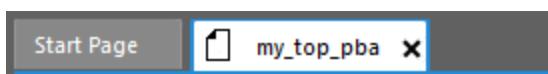


The floating toolbar is designed to show only a subset of options at a time. The options with an arrow at the top-right corner of their square container can be right-clicked to view additional options.

For information about how to use the blocks, see [Placing and Managing Components](#) and [Choosing Blocks to Place on the Canvas](#).

## Topology-Wise Tabs

A topology is opened in a tab of the same name. It displays the associated layout canvas. In addition, the [Start Page](#) tab is displayed.



You can close a topology-specific tab, but the [Start Page](#) tab cannot be closed.

## Layout Canvas

The layout canvas is a grided area where you graphically construct your topology using the required well-connected blocks.

## Edit Properties Panel

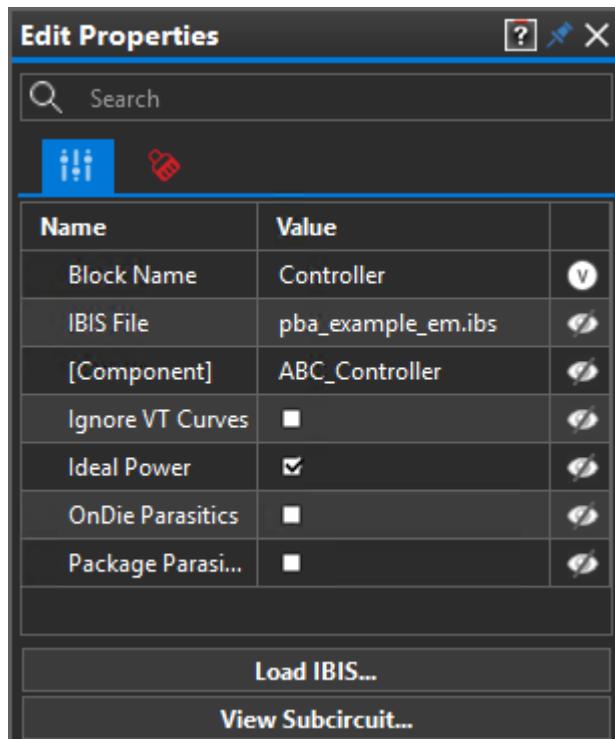
The *Edit Properties* panel can be opened by one of the following methods:

- Choose *View – Edit Properties* from the menu bar. Thereafter, as you select a component on the canvas, the displayed *Edit Properties* panel shows the associated information.
- Double-click any component on the canvas.

The *Edit Properties* panel has the following two tabs:

- *Component Properties* tab (  )

Opens the *Component Properties* tab like the one illustrated below. The contents of this tab vary depending on the component that has been selected on the canvas. The *Value* column shows the values defined for each parameter associated with the selected component.



When you place the mouse cursor on a parameter value that can be edited, an *E* button is displayed on its right, as shown above.

When viewing the properties of a block, the last column provides to you the following controls: *Do not show*, *Value only*, and *Name and value*. These options let you control whether the corresponding parameter's value and name should be displayed on the canvas.

For detailed usage information, refer to [Editing the Properties of a Component](#) in [Chapter 2, “Working with Topologies.”](#)

■ **Format Item tab (  )**

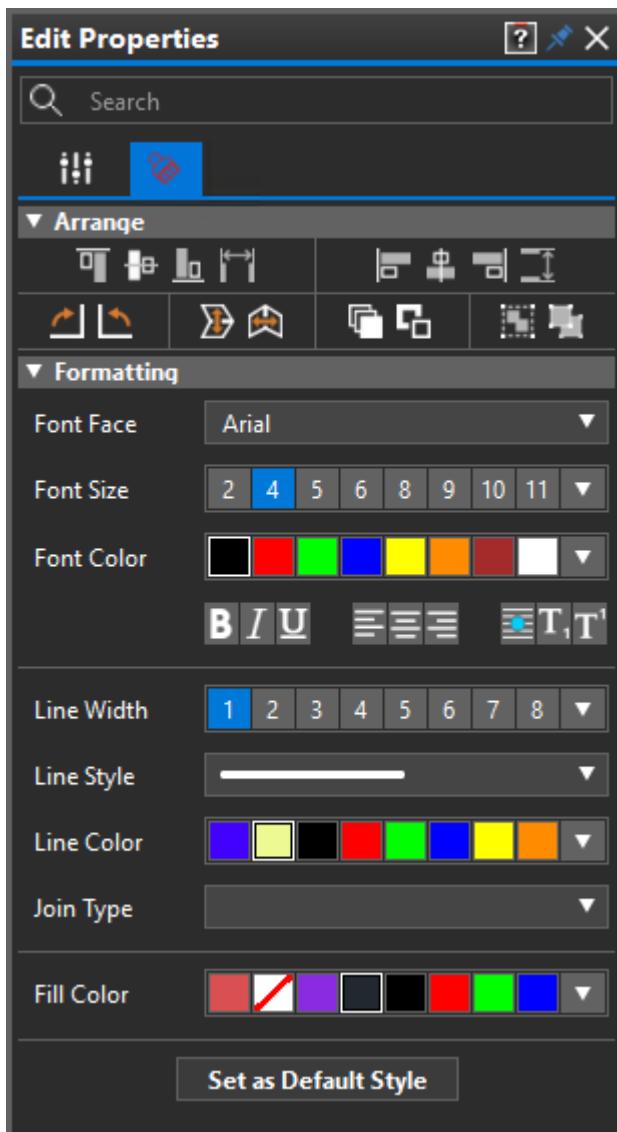
Opens the *Format Item* tab to enable you to format graphics of the selected component. For example, using the *Formatting* section on the tab, you can change the font face, size, and color of the associated text. In addition, the line and fill colors can be customized for each component on the layout.

## Topology Workbench User Guide

### Getting Started with Topology Workbench

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The *Arrange* section of the tab provides options to align, position, and group the components on the canvas.



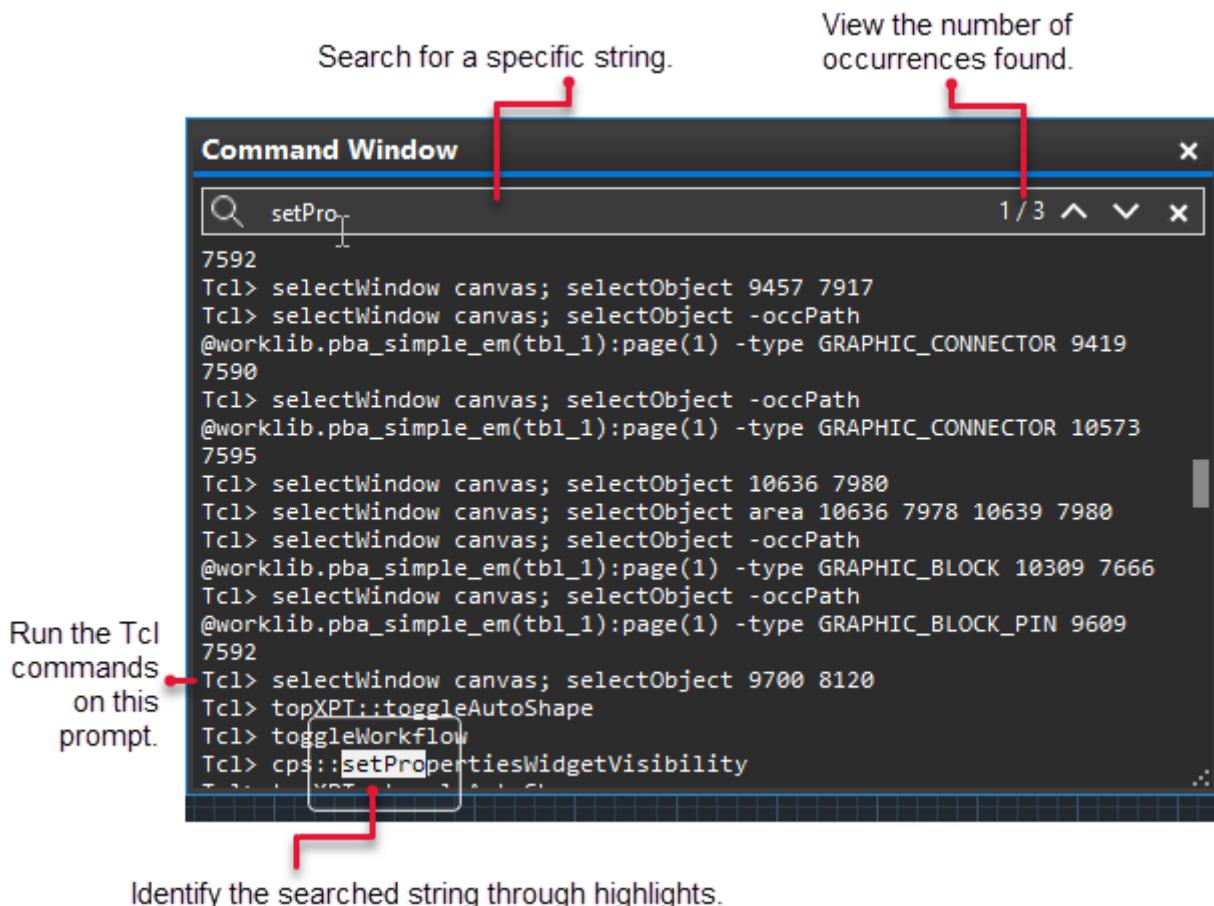
Click *Set as Default Style* to ensure that the defined formatting is reused when you add to the canvas a component of the same type again.

## Command Window Panel

To open the *Command Window* panel, choose *View – Command Window* from the menu bar.

This panel lets you run the supported Tcl commands and view the ones that are run in the

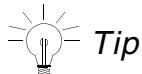
background when you perform a corresponding GUI action in the Topology Workbench window.



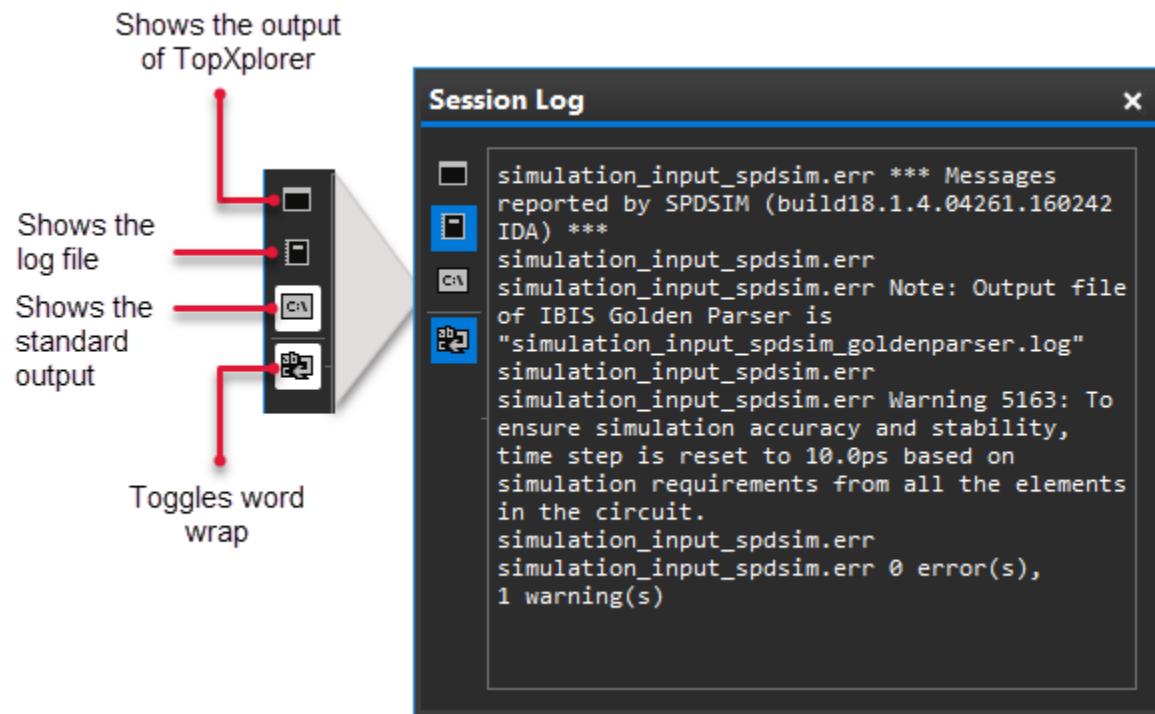
A field at the top of the *Command Window* panel lets you provide a search string. Each matching occurrence is highlighted in the panel and the total count of matching results is given on the right of the search field. You can use the up and down arrows given in this field to navigate to the location where the searched string was found.

## Session Log Panel

To open the *Session Log* panel, click *Session Log* in the docked panels bar above the status bar.



Alternatively, choose *View – Session Log* from the menu bar.



This panel provides clickable controls on the left to perform the following tasks:

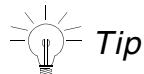
- Show the output related to Topology Workbench
- Show the log file to review error or warning messages that occur
- Show the standard output
- Toggle the word-wrap utility to allow long sentences or words to be broken and wrapped to the next line for better readability

## Customizing the View of Canvas and Windows

### Zooming and Panning for Better Visibility

The easiest way to zoom in and out, and move (roam or pan) across the canvas, is using the middle mouse button.

You can pan a topology (move across a topology in the canvas) to view different parts in it. To pan a topology, you need to hold the cursor inside the canvas, and then click and hold the middle mouse button (cursor changes to a hand) as you drag the cursor across the topology. As long as the mouse button remains pressed, you can move all areas of the topology into full view.



**Tip** Use the arrow keys on your keyboard to pan in the desired direction.

To zoom in or out, rotate the scroll wheel of the mouse. Alternatively, you can use the menu options and icons given in the following table to perform the various zoom functions:

Choose Toolbar Icons		Description
Zoom in		Magnifies the topology to make it larger and display less of it in the canvas.
Zoom out		Shrinks the topology to display more of it in the canvas.
Zoom fit		Changes the display so that the topology fills the canvas.
Zoom by points		Changes the cursor to a plus, dragging which on the canvas pans and magnifies the area of topology under it for closer examination.

## Re-sizing the Canvas

You can move the left border of the layout canvas to increase or decrease the view. You need to drag the edge of the border with your mouse, and then move the divider left or right, as required.

## Working with Foldable Panels

The foldable panels are particularly useful on a single monitor setup because they provide more workspace, while giving you the option of seeing the panel information by clicking the corresponding icon on the toolbar, such as, *Command Window*, *Edit Properties*, and *Analysis Options*. When you click the cursor on the canvas, the displayed panel closes.

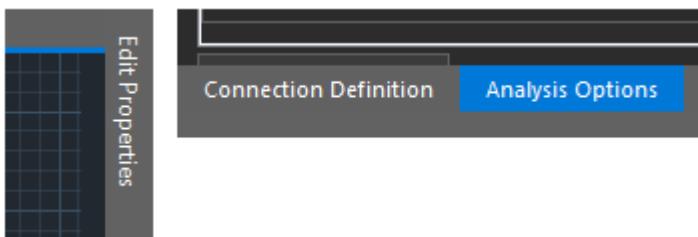
## Persistent Panels

Instead of having a panel hide automatically when you click the cursor on the canvas, you can make the visibility of the panel persistent by clicking the *Auto Hide* () pin icon on the title bar of the panel.



You can click this pin icon again (unpin) to restore the auto-hide feature of the panel, or click X to close a pinned panel.

When these panels are unpinned, they retract as a tab to the side of the Topology Workbench window in which they were placed. This tabbed placement of panels can also be noticed when you open multiple pinned panels at the same time.



## Undocking Windows

In the Topology Workbench window, by default, all panels that have a pin icon in their title bar are dockable.

To create more workspace, you can detach (undock) panel from the main Topology Workbench window and place it anywhere on the monitor. In addition, when you unpin a panel, and click

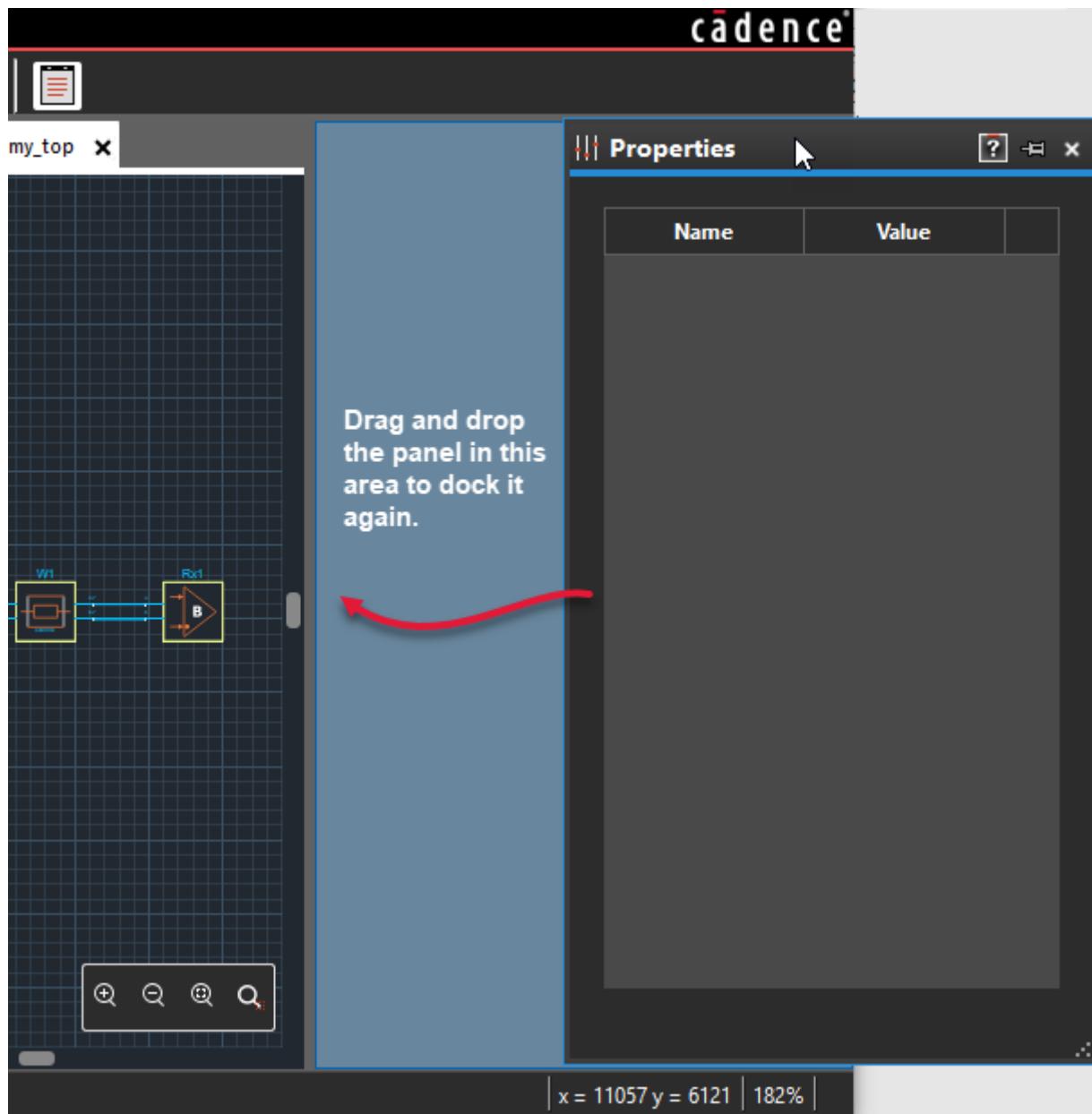
To undock a panel, click its title bar and drag it while keeping the mouse button pressed.

To attach (dock) it back again, double-click the title bar of the panel. The panel will get adjusted back to its default location in the Topology Workbench window.

## Topology Workbench User Guide

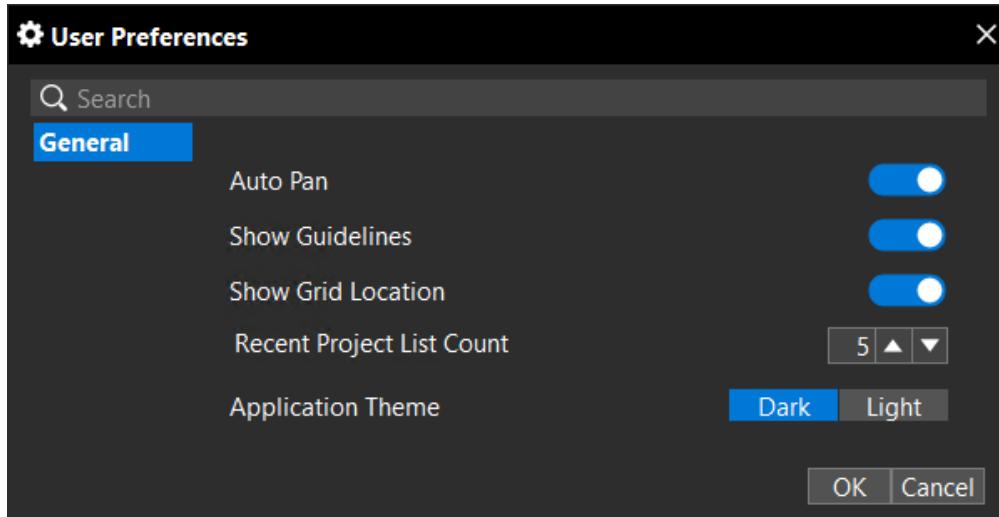
### Getting Started with Topology Workbench

Alternatively, you can drag the undocked panel by its title bar and drop it to the side of the Topology Workbench window where the window adjusts automatically as shown below:



## Setting the User Preferences

Topology Workbench allows you to set the default user preferences to suit your requirements. Choose *Edit – User Preferences* to open the dialog box shown below:



In this dialog box, you can set the following preferences and click *OK* to apply your changes:

<i>Auto Pan</i>	Select to automatically pan the area on the canvas.
<i>Show Guidelines</i>	Select to show guidelines as you plot the topology.
<i>Show Grid Location</i>	Select to show the grid location (x and y coordinates) on which the cursor is placed in the canvas. This grid location is displayed in the status bar.
<i>Recent Project List Count</i>	Select a number to identify how many recent projects should be listed in the <i>Topology – Recent Topologies</i> menu.
<i>Application Theme</i>	Choose the preferred theme of the Topology Workbench window whether <i>Dark</i> or <i>Light</i> . By default, <i>Dark</i> is selected.

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# Working with Topologies

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When working with topologies in Topology Workbench, you have the following three use models available:

- Create a new project from scratch
- Open an existing project saved from an earlier session
- Extract a topology from an Allegro-based PCB, IC Package, or SiP database

There are some common canvas and GUI operations that you can perform on any topology in Topology Workbench.

### ***Related Topics***

- [Creating a Topology Project from Scratch](#)
- [Opening an Existing Topology Project](#)
- [Placing and Managing Components](#)
- [Assigning and Editing IBIS Models](#)
- [Assigning and Extracting S Parameter Files](#)
- [Setting Up Probe Points](#)
- [Setting Up Component Model](#)
- [Setting Up Distributed Computing Options](#)
- [Switching to Another Workflow](#)
- [Customizing a Workflow](#)
- [Creating Custom Templates](#)
- [Archiving a Topology](#)
- [Appending to a Topology](#)

## Creating a Topology Project from Scratch

Topology Workbench provides an intuitive schematic entry GUI for capturing system designs as well-connected block diagrams. If you want to create a project from scratch, you can:

- Choose to create a blank topology and add components to it.

This approach benefits when you want to do sandbox-style exploratory analysis.

-or-

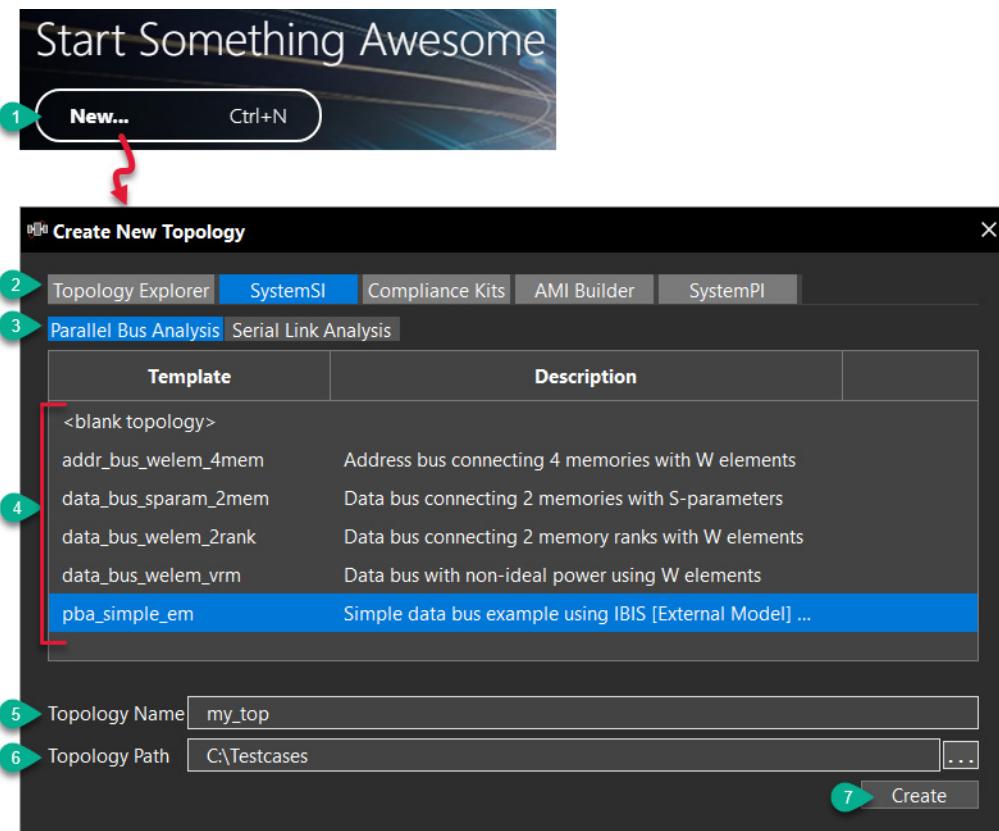
- Choose a predefined template and add/modify components as required.

The pre-constructed, ready-to-simulate templates are useful to start building a topology early with a known good state and editing it progressively for refined models.

To create a new project from scratch, do the following in the Topology Workbench window:

1. Click *New...* from the *Start Something Awesome* section on the Start Page tab.

The *Create New Topology* dialog box is displayed, as shown below.



## Topology Workbench User Guide

### Working with Topologies

**2.** Click the tab that represents the type of topology you plan to create.

The following tabs are provided with support for corresponding workflows:

- Topology Explorer* for the Topology Explorer workflow
- SystemPI for the *DC IR Drop Analysis*, *PDN Impedance Analysis*, and *Power Ripple Analysis*
- SystemSI for the Parallel Bus Analysis and Serial Link Analysis workflows
- Compliance Kits for a *Custom Compliance Kit* and workflows related to various supported SFP+, HDMI, PCIe, and OpenPOWER kits
- AMI Builder to produce Algorithmic Modeling Interface (AMI) models

**3.** Select the sub-tab that corresponds to the required workflow.

**Note:** The sub-tabs are not displayed when you choose the *Topology Explorer*, *Compliance Kit*, and *AMI Builder* tabs.

The table in the selected tab is refreshed with a list of default templates associated with the selected workflow. Within the table, an option to create a *<blank topology>* is also displayed in the following workflows: *Topology Explorer*, *Parallel Bus Analysis*, *Serial Link Analysis*, and *SystemPI*.

**4.** Select the table row that displays the *Template* of your choice or the text *<blank topology>*.

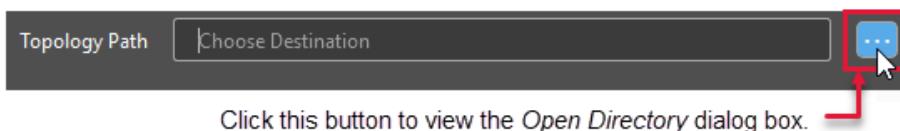
Before selecting a template, examine the brief description provided for each template. This helps you to choose a template that is most appropriate for your business requirements.

**5.** Specify a *Topology Name*.

Ensure that the topology name contains only lowercase alphanumeric characters and underscores. If a topology with the same name already exists at selected location, a message is displayed at bottom of dialog box.

**6.** Specify the *Topology Path* to identify the directory where the new topology and related files should be saved on the hard drive.

You can type in the logical path to the directory or use the  button adjacent to the field to view the *Open Directory* dialog box and browse to the required directory.



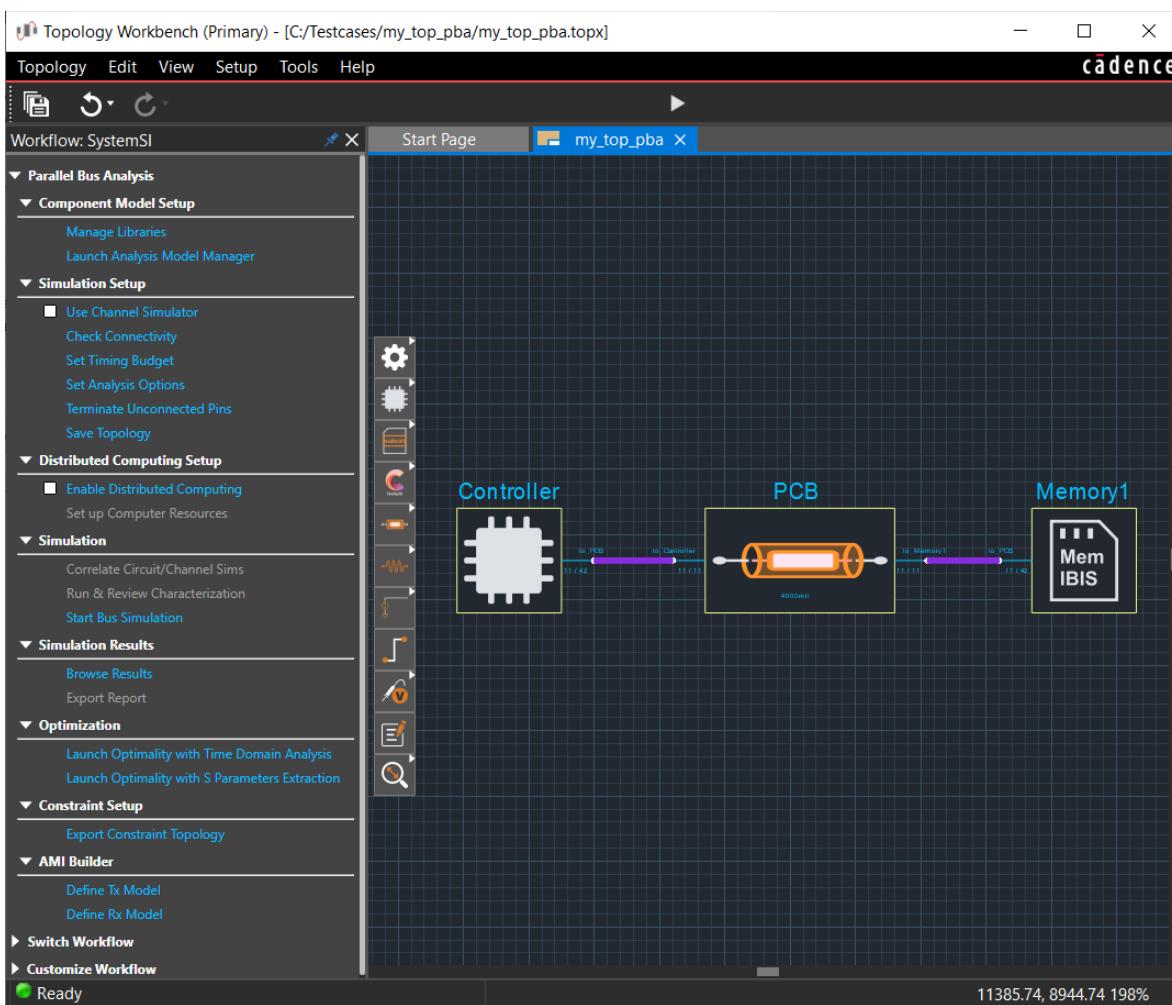
# Topology Workbench User Guide

## Working with Topologies

### 7. Click *Create*.

A new tab having the specified *Topology Name* opens. If a topology with the same name exists, a warning message box opens first to confirm if you want to overwrite it.

The project is created and the available design steps are listed in the Workflow Panel. If you created a template-based project, the layout is populated with the related blocks. You can perform various edit operations on the topology, such as, add more blocks from the floating toolbar, modify the properties of the plotted blocks, move the blocks around on the canvas, and delete the blocks that are not needed.



### *Important*

Topology Workbench provides you with the flexibility to switch between workflows and product licenses whenever required. If you choose a template associated with a module that is not supported by the product license with which Topology

Workbench was started, the *Cadence Product Choices* dialog box is displayed after you click *Create*. This time the dialog box lists only those licenses that support creation of a project using the chosen template. The caveat here is that you must own the required product licenses. For licensing-related queries, contact Cadence Customer Support for assistance.

#### ***Related Topics***

- [Opening Topology Workbench in Standalone Mode](#)
- [Identifying the Topology Workbench Workflow to Use](#)
- [Using Topology Workbench Optimally](#)
- [Exploring the Topology Workbench Interface](#)
- [Customizing the View of Canvas and Windows](#)
- [Switching to Another Workflow](#)

## Opening an Existing Topology Project

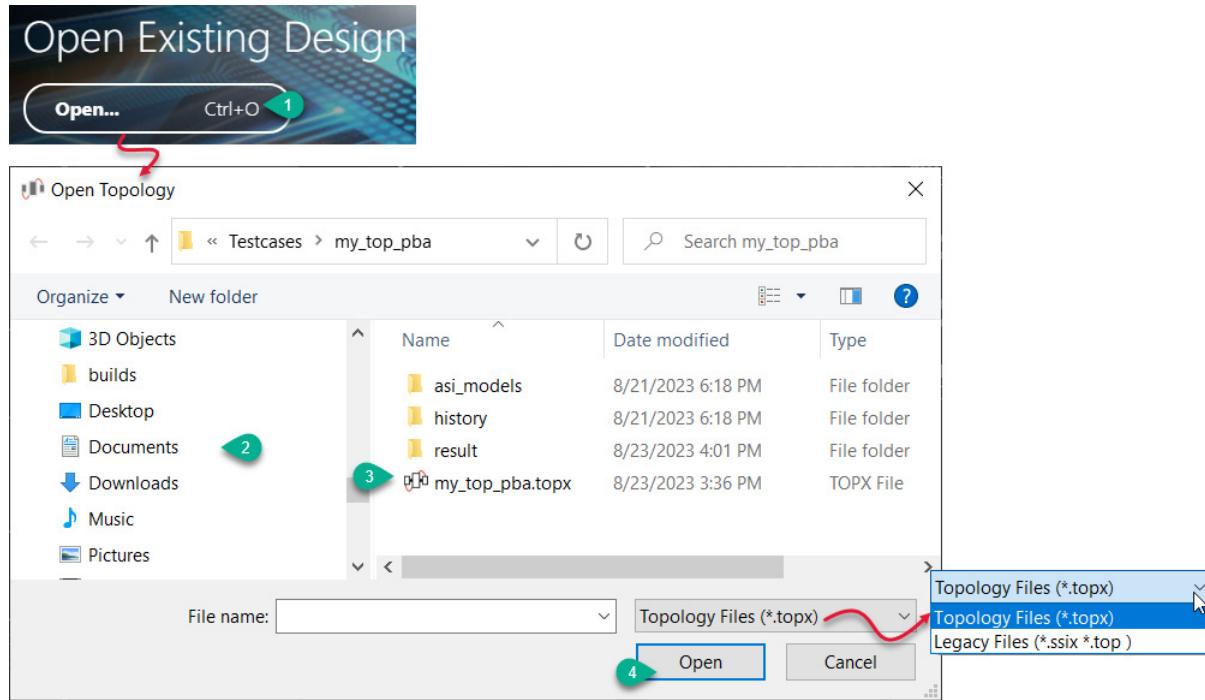
To open an existing topology project file (\*.topx) or a legacy file (\*.ssix or \*.top):

1. Click *Open...* from the *Open Existing Design* section on the [Start Page](#) tab.

## Topology Workbench User Guide

### Working with Topologies

The *Open Topology* dialog box is displayed, as shown below.



2. Browse to the directory in which the project file you want to open exists.

3. Select the project file.

To filter and view a specific type of file, you can use the list box adjacent to the *File name* text box.

4. Click *Open*.

A tab with the *Topology Name* associated with the selected project file opens. The blocks previously added to the project are plotted on canvas and the supported design steps are listed in the Workflow Panel.

## Placing and Managing Components

Once a project has been created, you can add blocks to define a topology, add connections between the block, and identify their properties to match the design requirements.

### Adding Blocks to the Canvas

Topology Workbench provides blocks of the following two default connectivity models in the Floating Toolbar:

- Single-ended, block-based signals

These are available in the Topology Explorer, SystemPI, Serial Link Analysis (SLA), and Parallel Bus Analysis (PBA) workflows.

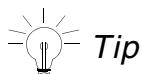
- Differential signals

These are available only in the Topology Explorer and SLA workflows.

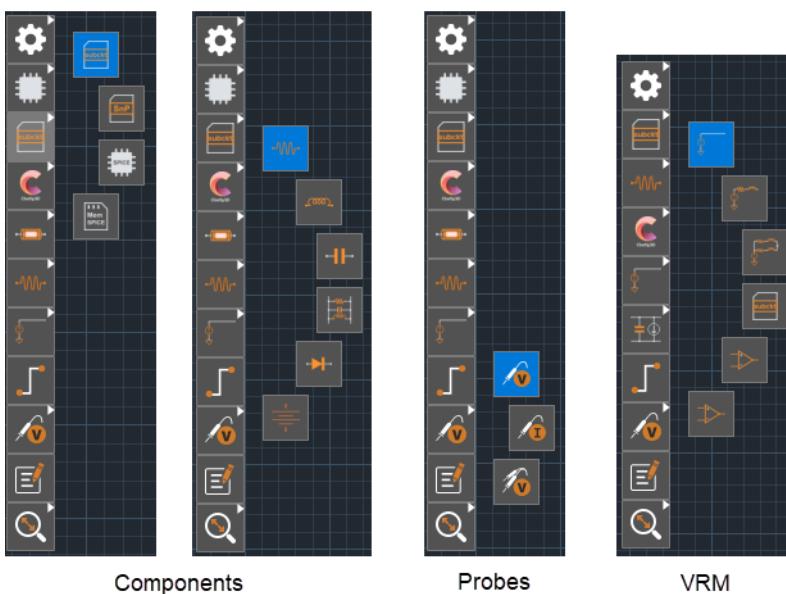
For more information about the available blocks, see [Choosing Blocks to Place on the Canvas](#)

To add a block to the canvas:

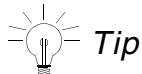
1. Place the pointer on the required block in the floating toolbar. It highlights the block under the pointer.



If a block option is not visible in the floating toolbar, right-click the blocks with an arrow to view the other available types of blocks.



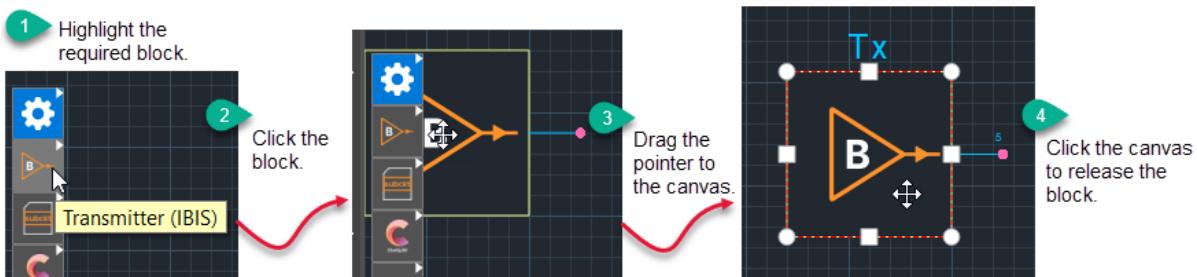
2. Click the highlighted block. This selects and attaches the block to the pointer.



### Tip

Pressing the `Esc` key releases the selected block.

3. Drag the pointer to the canvas location where the block needs to be placed.
4. Click the canvas to release the block. The block and its pins are assigned a default name, which you can change in the *Edit Properties* panel. Now, you can proceed to [connect the blocks](#).

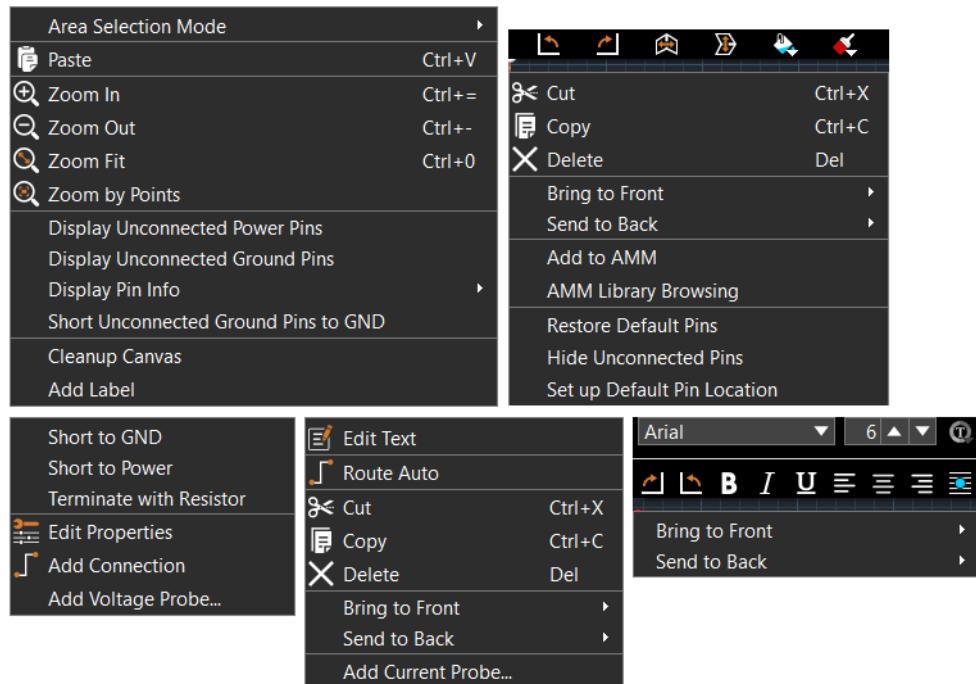


### Related Topics

- [Connecting the Blocks on the Canvas](#)
- [Changing the Orientation of a Block](#)
- [Modifying the Connection Port Location](#)
- [Managing Connections Between Blocks and Signals](#)
- [Shorting a Block](#)
- [Adding Labels to the Schematic](#)

## Performing Common Tasks on Components

After you have placed blocks on the canvas, you can right-click each component including the canvas to access a shortcut menu of the common tasks that can be performed on it.



Following are some of the common tasks that are available for various components:

- Creating a copy of the component
- Deleting a component
- Cutting and pasting a component to another place in the topology
- Changing the orientation or formatting of the component. See [Changing the Orientation of a Block](#)
- Adding connections between the blocks
- Adding and formatting labels to the components
- Editing the properties of the components
- Adding current and voltage probes
- Shorting unconnected power and ground pins
- Terminating with resistor

- Displaying or hiding unconnected power and ground pins
- Displaying pin information for *Net*, *Pin*, *Cktnode* or *None*
- Cleaning up the canvas to eliminate any routing violations between the blocks and rearrange to show the Tx/Rx channels
- Adding the IBIS model associated to a block to AMM and browsing the AMM library

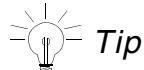
For Transmitter (Tx) and Receiver (Rx) blocks, you can also perform the following tasks:

- Add new AMI blocks.
- Create new AMI models with AMI Builder. See [Using the AMI Builder](#) for details on how.
- Add repeater connections

## Changing the Orientation of a Block

To change the orientation of a block, you can rotate it as explained below:

1. Right-click the block that needs to be rotated. The shortcut menu is displayed with options to rotate the block clockwise or counter-clockwise. You can also mirror the block horizontally (around the X-axis) or vertically (around the Y-axis).

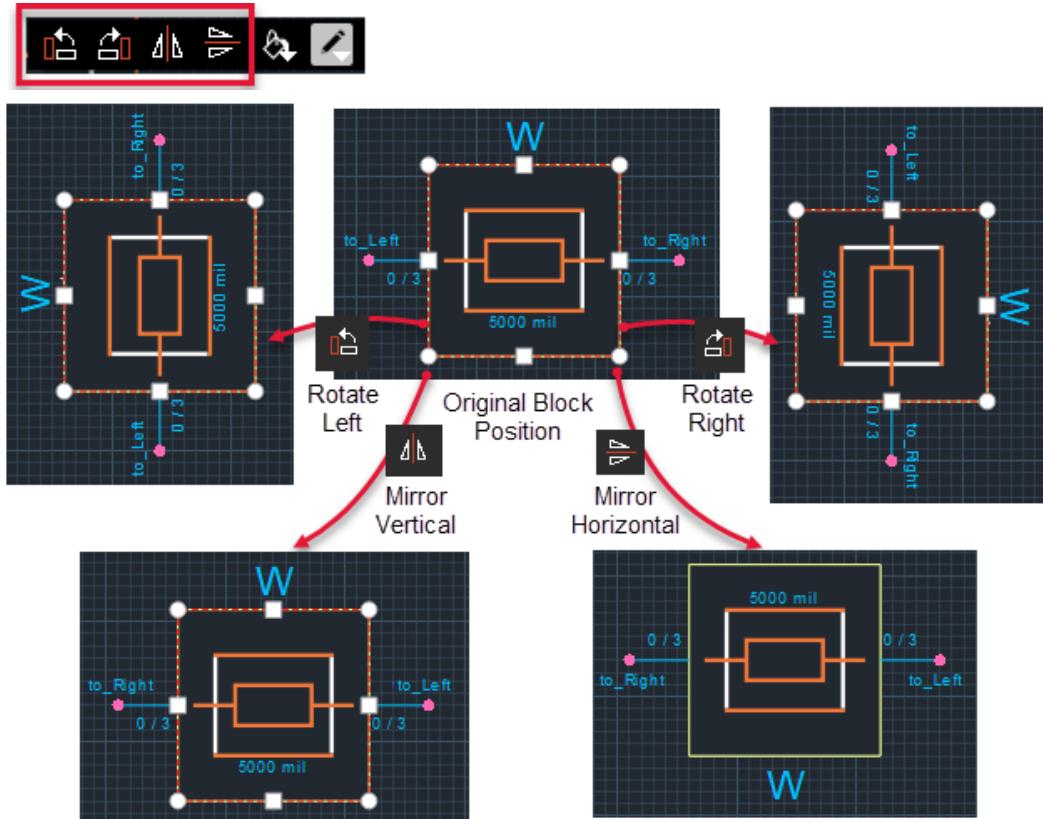


The rotation options can alternatively be accessed from the *Position* section of the *Selection Filter* panel. You can also use the *Mirror* and *Rotate* submenu options from the *Edit* menu.

# Topology Workbench User Guide

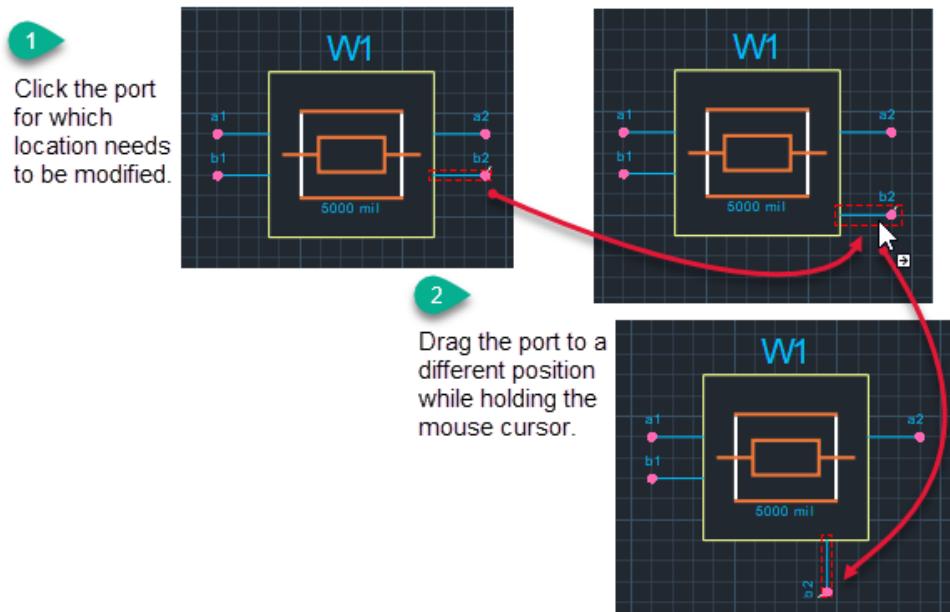
## Working with Topologies

2. Choose the option to rotate the block as required.



## Modifying the Connection Port Location

To change the default location of the connection ports on a block, select and drag it to the location of your choice while holding the mouse cursor as shown below.



## Connecting the Blocks on the Canvas

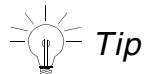
Until you connect one block to another, their connection ports appear as pink dots and indicate that no electrical model has been assigned to the block. Connecting all blocks on the canvas together helps to develop a circuit schematic and show the actual electrical connections between the blocks.

In Topology Workbench, you can connect the blocks at the net, pin, and node levels to support the following types of connection schemes on the canvas:

- Wire-Based Connectivity
- Block-Based Connectivity
- Wire-Based and Block-Based Combination Connectivity

## Wire-Based Connectivity

In the SLA and Topology Explorer workflow, you can create a topology that contains blocks with differential signals. Such blocks are connected using the wire-based connectivity scheme.



*Tip*  
Click the *Settings* option in the floating toolbar and select the *Diff Signals* toggle button to use blocks with differential signals in the topology.

Though the default mode of connectivity in the PBA and SystemPI workflows is block-based, you can use wire-based connectivity if desired. For information, see [Converting a Block-Based Connection to Wire-Based Connection](#).

To connect the signals of two blocks, you can use one of the following methods:

- [Pin-to-Pin Method](#)
- or-
- [Pin-over-Pin Method](#)

### ***Pin-to-Pin Method***

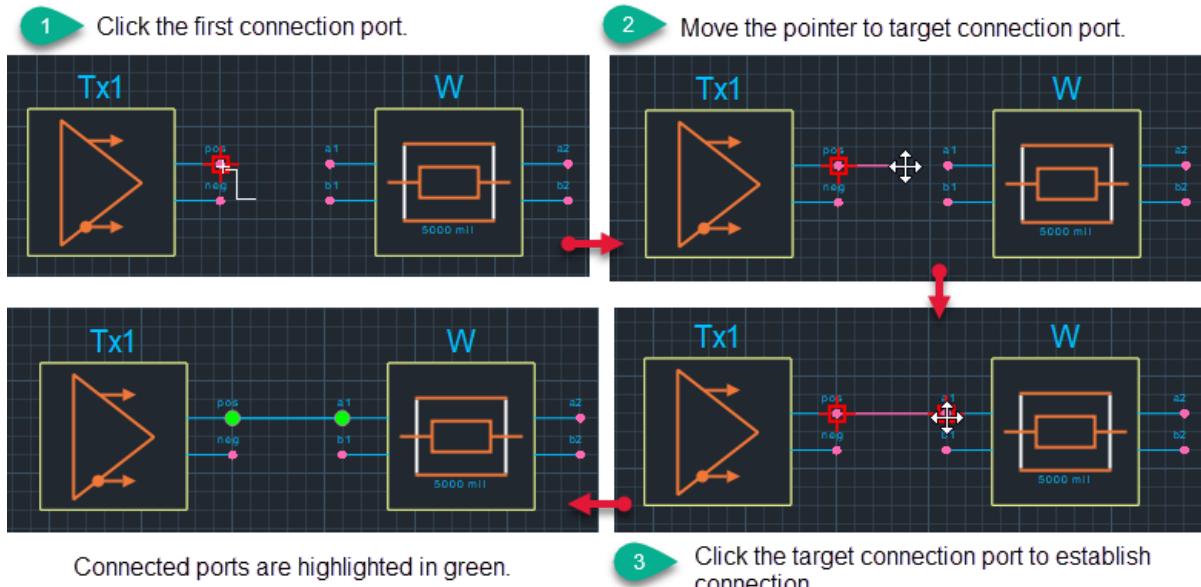
To connect two signals using the pin-to-pin method:

1. Click the connection port of a differential signal on the first block. The port gets highlighted.
2. Move the pointer to the connection port of the target signal associated with the second block. As the pointer moves, a pink line indicating the connectivity path trails. When the pointer is placed on the target connection port, this target port is highlighted too.

## Topology Workbench User Guide

### Working with Topologies

- Click the connection port of the target block. The color of the two connected ports changes to green.



### Pin-over-Pin Method

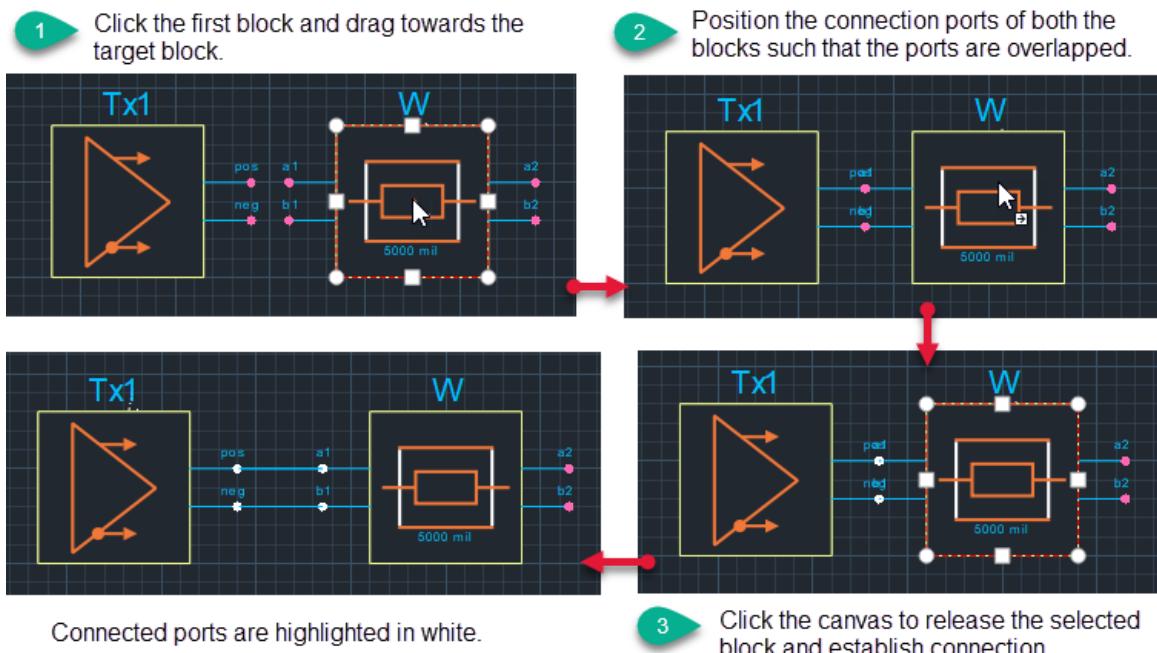
To connect two signals using the pin-over-pin method:

- Select a block for which the signal needs to be connected and drag this block towards a target block while keeping the left mouse button clicked.
- Position the connection ports of the two blocks such that the ports that need to be connected are overlapped.
- Click the canvas to release the selected block. As the connection is established, the color of the connected ports changes to white.

## Topology Workbench User Guide

### Working with Topologies

- Move one of the connected block anywhere on the canvas. Notice that the connection moves and adjusts automatically.



## Block-Based Connectivity

In the PBA, SLA, Topology Explorer, and SystemPI workflows, when the *Block-Based* toggle button is selected in the *Settings* option of the floating toolbar, you can place blocks that have single-ended signals. For connecting signals of these type of blocks, Topology Workbench supports the block-based connectivity scheme.

You can use one of the following methods for establishing block-based connectivity between signals:

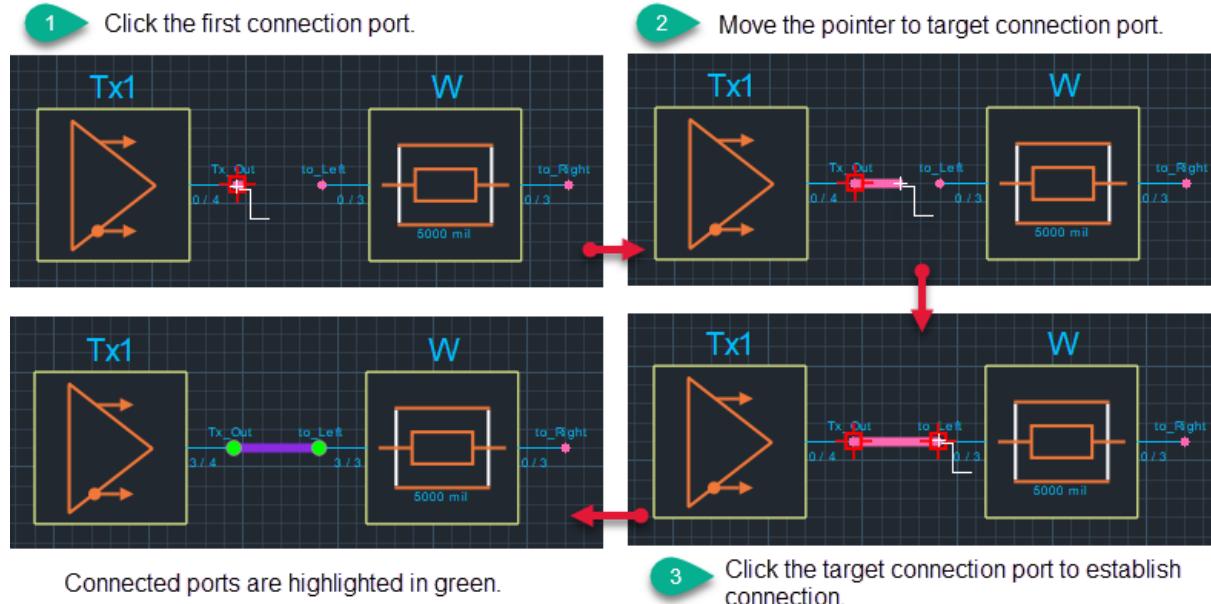
- Pin-to-Pin Method  
-or-
- Pin-over-Pin Method

**Note:** A block-based connection can be converted into a wire-based connection if required later. For the steps, see [Converting a Block-Based Connection to Wire-Based Connection](#).

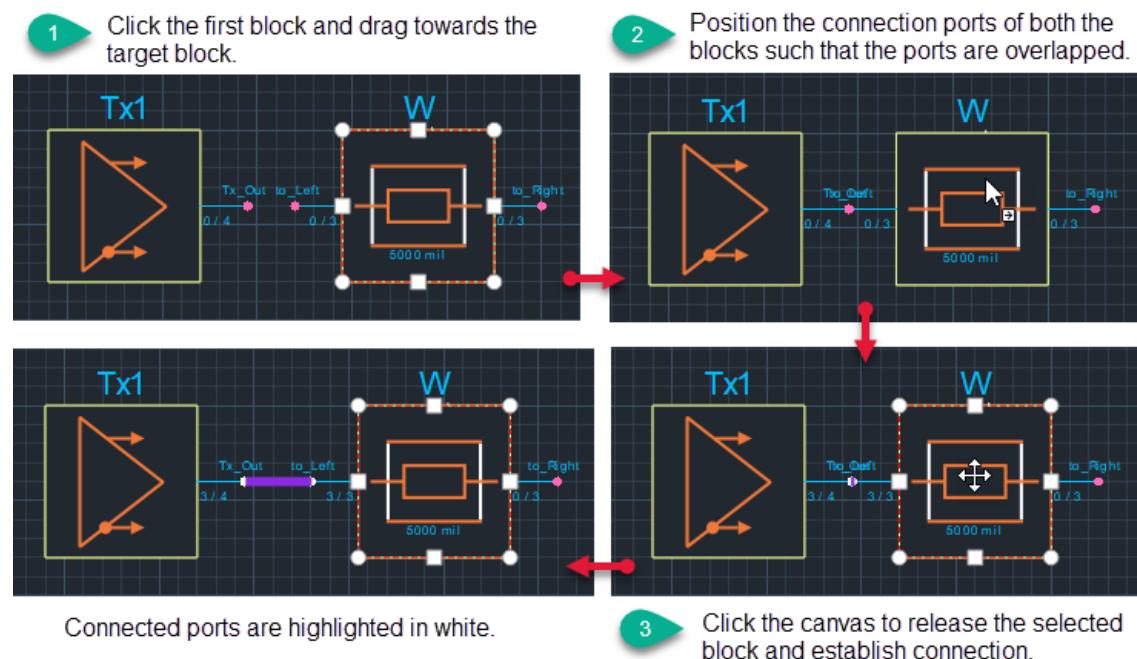
# Topology Workbench User Guide

## Working with Topologies

Following is an example of pin-to-pin method used for block-based connectivity:



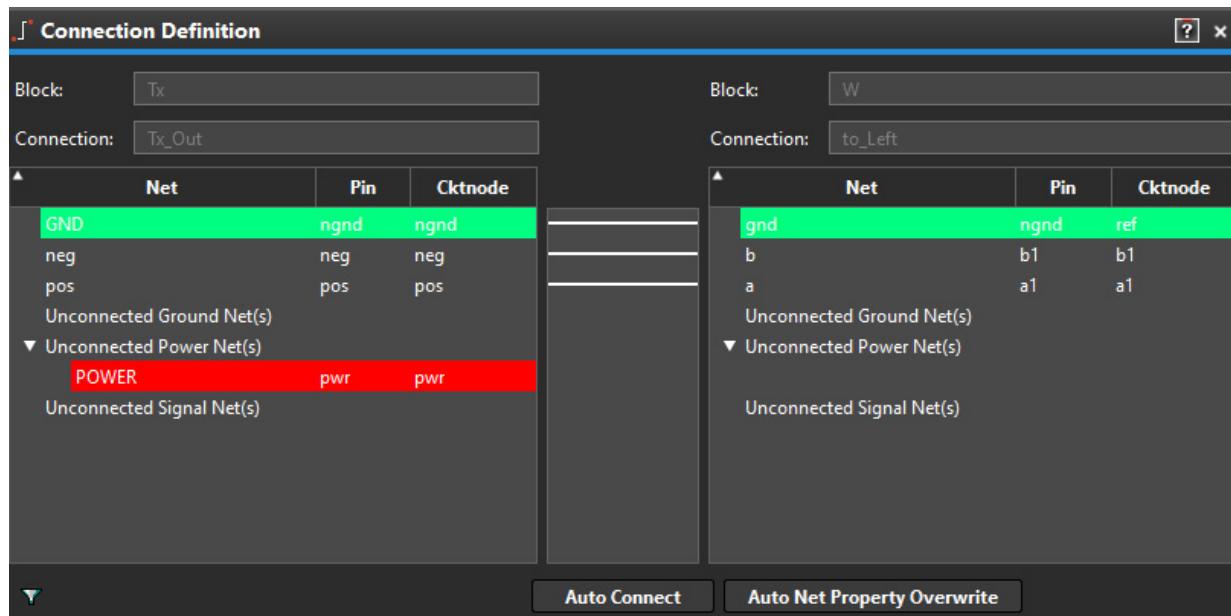
Following is an example of pin-over-pin method used for block-based connectivity:



# Topology Workbench User Guide

## Working with Topologies

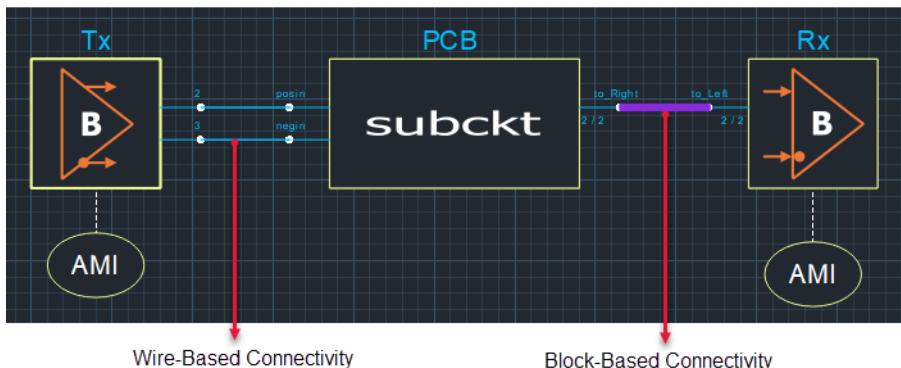
Once the block-based connectivity has been established, the *Connection Definition* dialog box opens, which is not the case in the wire-based connectivity scheme.



To facilitate easy connection, you can rotate the blocks or can modify the connection port location on the block.

## Wire-Based and Block-Based Combination Connectivity

Considering that in the SLA and Topology Explorer workflows, a topology can contain blocks with both differential and single-ended signals, Topology Workbench allows both wire-based and block-based connectivities to co-exist as shown below.



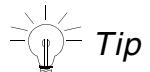
**Related Topics**

- [Changing the Orientation of a Block](#)
- [Modifying the Connection Port Location](#)
- [Managing Connections Between Blocks and Signals](#)
- [Shorting a Block](#)
- [Adding Labels to the Schematic](#)

## Converting a Block-Based Connection to Wire-Based Connection

To expose a pin from a multi-pin connection and convert a block-based connectivity into a wire-based connectivity:

1. Double-click a multi-pin to open the list of signals in the *Edit Properties* panel.



*Tip*

Alternatively, right-click the multi-pin and select *Edit Properties* from the shortcut menu.

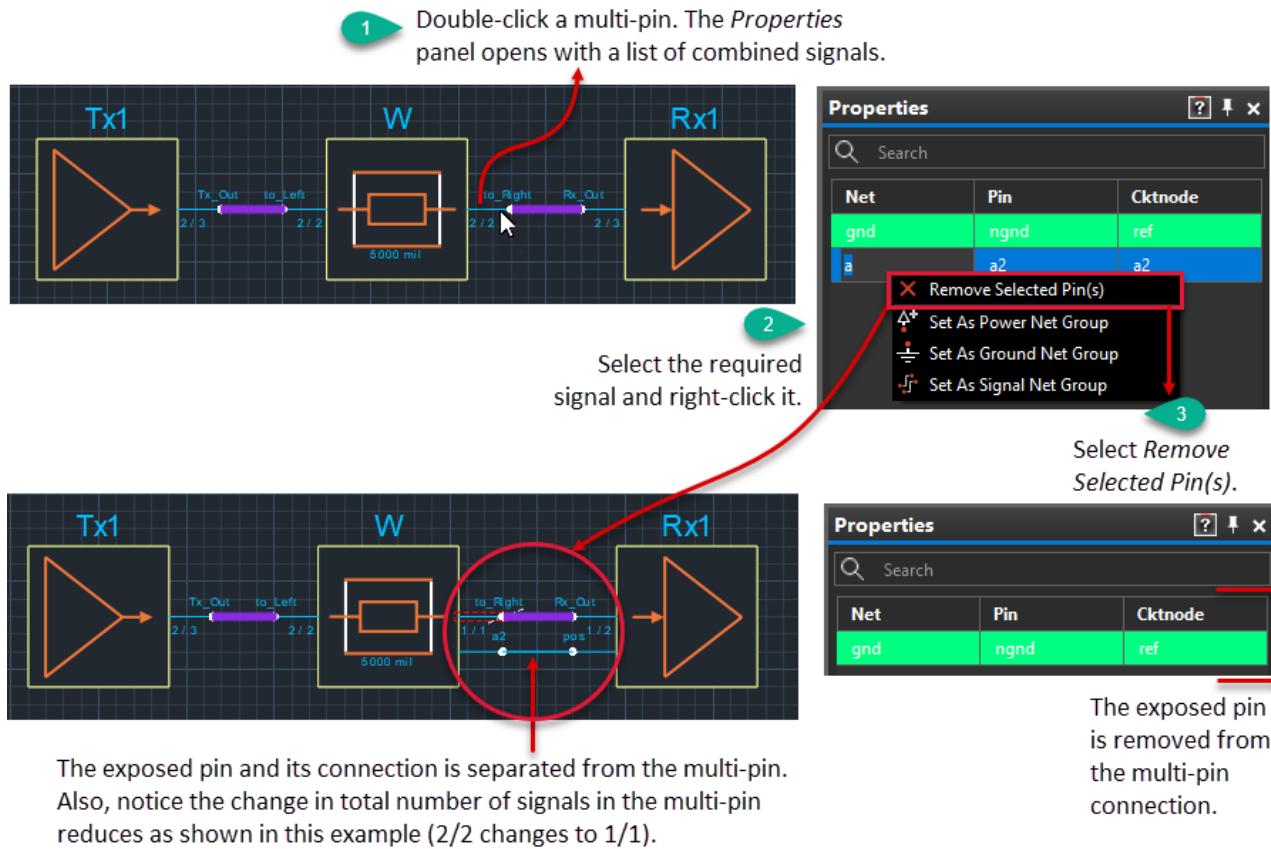
2. Select one or more signals from the list.
3. Click right and select *Remove Selected Pin(s)* from the shortcut menu to break the selected pin(s) into new individual pin(s) and expose the associated connections.

# Topology Workbench User Guide

## Working with Topologies

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The figure below illustrates the steps to expose pin *a2* from a multi-pin connection of block *W*:



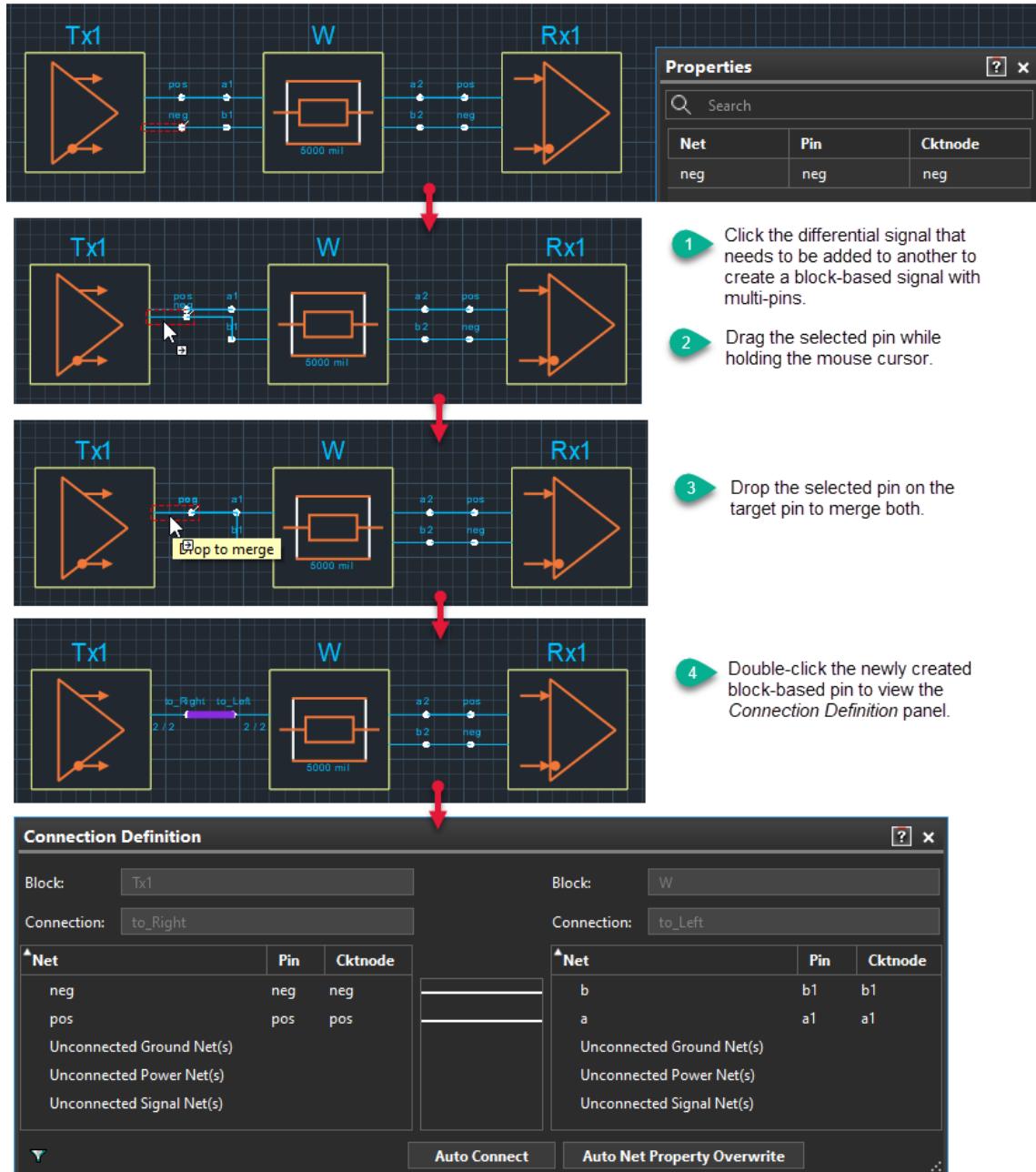
To reverse the process, select and drag a pin, and then drop it on top of another pin to merge the signals into a single pin.

# Topology Workbench User Guide

## Working with Topologies

### Converting a Wire-Based Connection to Block-Based Connection

You can also combine multiple differential signals to create a single-ended signal by dragging and dropping a differential signal on another as shown below.



## Managing Connections Between Blocks and Signals

Block-based connectivity uses multi-pins where multiple signals are combined into a single connect point. Therefore, connections of such blocks need to be represented in a multi-pin or block-based connections netlist. This netlist is inserted as a header in the circuit netlist for a component, or is created separately for a component.



Editing the multi-pin or block-based connections netlist is not recommended.

In the PBA workflow, for the Controller and Memory components, this connections netlist is created automatically from the IBIS file.

For the VRM block, the connections netlist is contained in the `.sp` file. This file also includes the model's information that can be edited.

For the PCB and other interconnects, the model's information is saved in a `.CKT` netlist file. Tools such as Sigrity PowerSI are used for generating the `.CKT` files from the network parameter simulation results.

For most system designs, the connections between components will be created automatically based on common pin names. The exception to this rule are connections between the Power and Ground nets that mostly require manual editing.

To view the signals included in the block-based connections netlist, double click the connection port and a list of the associated nets, pins, and circuit nodes are displayed in the *Edit Properties* panel in a tabular format.

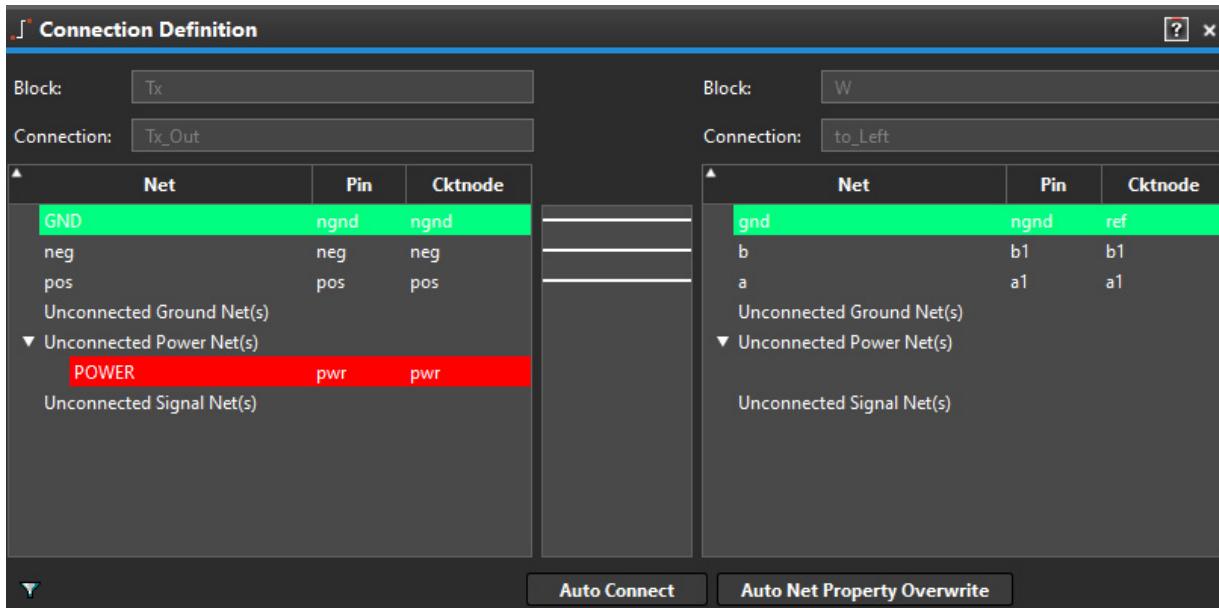
When you connect two connection ports on the canvas, Topology Workbench automatically connects the nets using the following rules:

- Nets with same pin names are connected automatically.
- If the number of unconnected nets on the two ports being connected are the same, all nets are connected one-to-one.

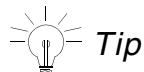
## Topology Workbench User Guide

### Working with Topologies

- If there are multiple unconnected nets, the *Connection Definition* panel opens. You can use this panel for connecting the nets automatically or manually.



You can also double-click a connection on the canvas to open the *Connection Definition* panel.



The ground nets are highlighted in green color and the power nets in red.

The *Connection Definition* panel can be used to perform the following functions:

- [Automatically Connecting Unconnected Nets](#)
- [Manually Connecting Unconnected Nets in a Single-Ended Configuration](#)
- [Manually Connecting Unconnected Nets in a Differential Configuration](#)
- [Connecting Multiple Nets by Pin Pairs in a Single-Ended Configuration](#)
- [Disconnecting the Nets](#)
- [Overwriting Property of Nets and Classes](#)

#### **Automatically Connecting Unconnected Nets**

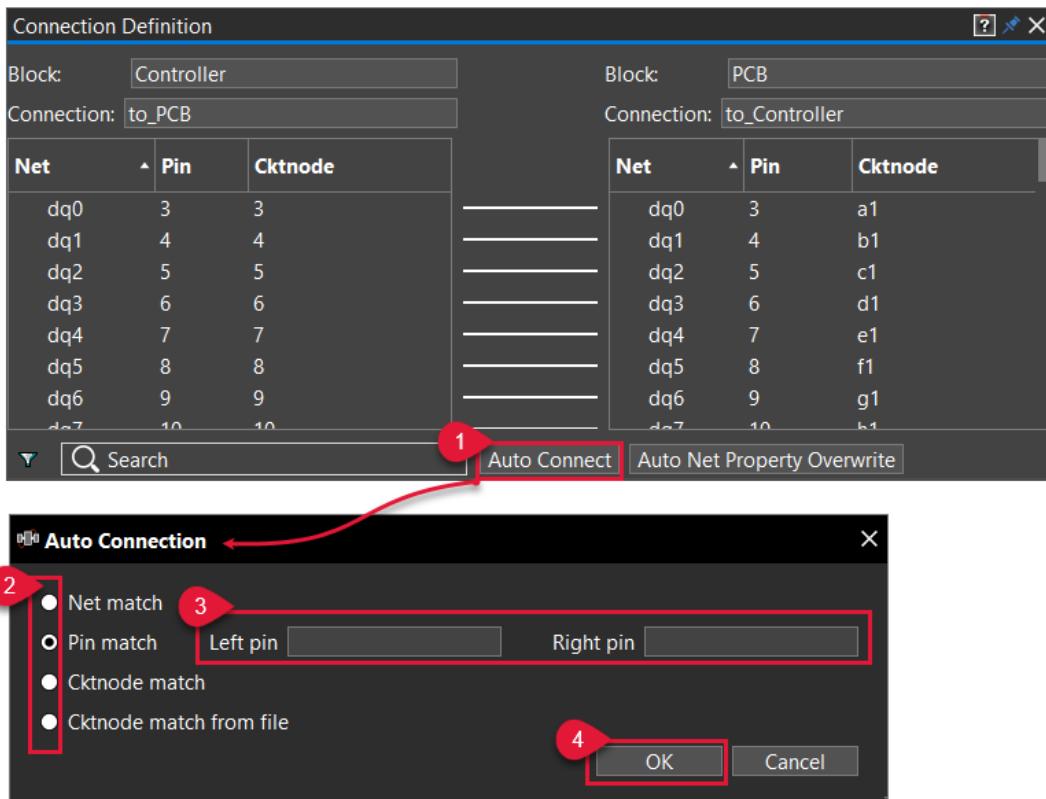
To connect the unconnected nets automatically based on a specified criteria:

# Topology Workbench User Guide

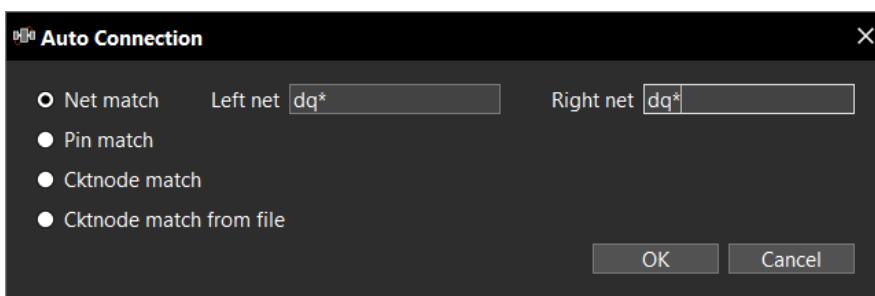
## Working with Topologies

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1. Click *Auto Connect*. The *Auto Connection* dialog box opens with the *Pin match* option selected by default.



2. Select one of the options from *Net match*, *Pin match*, *Cktnode match*, or *Cktnode match from file*. Adjacent to the *Net match*, *Pin match*, and *Cktnode match* options, two text boxes are displayed to enter the criteria based on which signals are chosen from the left and right tables to establish connections automatically. When the *Cktnode match from file* option is selected, a text box with browse button is displayed to import a CSV file using which connections can be established in the topology.
3. (Optional) Specify the left and right net names, pin numbers, or circuit node numbers. You can specify the exact values or wildcard search values such as *1\** or *DQ\** (shown in the example below).

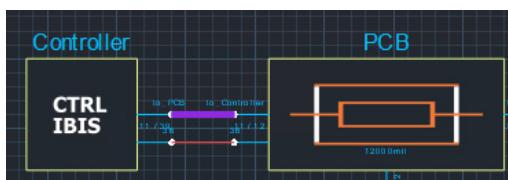


# **Topology Workbench User Guide**

## Working with Topologies

4. Click *OK*. The *Auto Connection* dialog box closes and the connections get created automatically.

**Note:** On the layout canvas, you will see that the connection line shows in green if connected with ground pin, and shows in red if connected with power pin. The example below shows connection between exposed power pins when a block-based connectivity is converted into a wire-based connectivity.

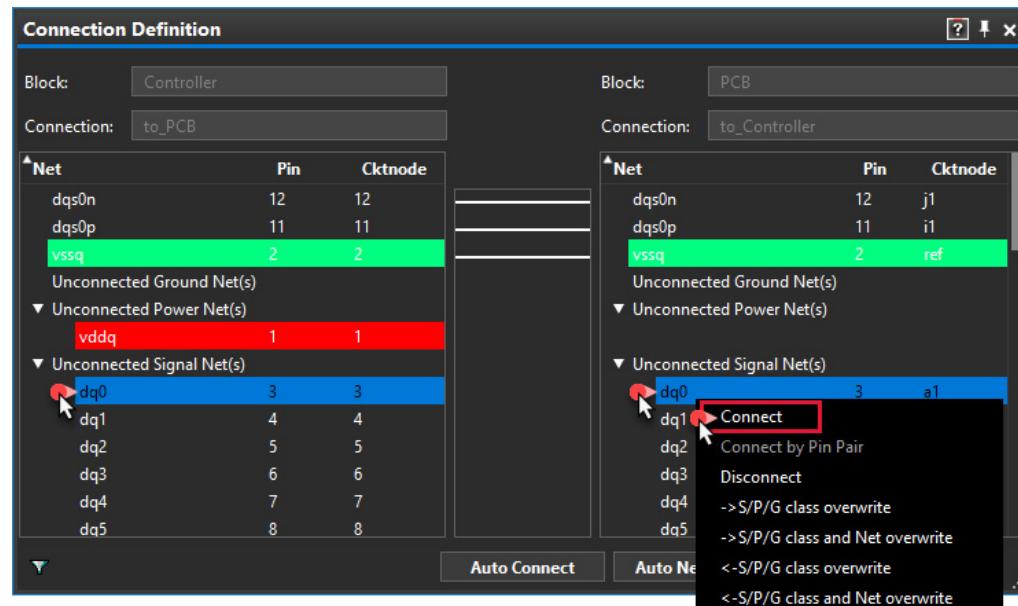


## Manually Connecting Unconnected Nets in a Single-Ended Configuration

When two specific nets should be connected to each other in a single-ended configuration, you have the option to establish the connections manually. There can be cases where data nets and some *Power* and *Ground* pins are not connected, or are incorrectly connected. This can be possible if the pin names in the .CKT file do not match the pin names directly in the IBIS files. For such cases, you need to map the pins manually.

To connect a pair of unconnected nets in a single-ended configuration:

1. Select one net each from the left and right tables in the *Connection Definition* panel.

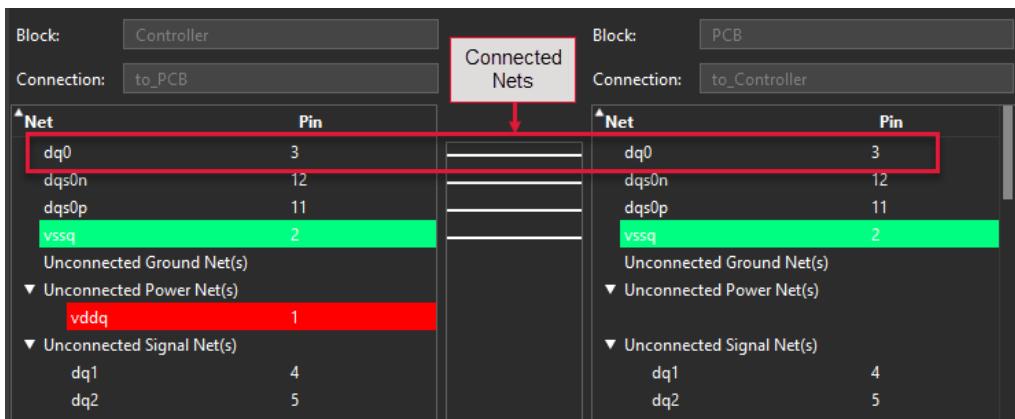


# Topology Workbench User Guide

## Working with Topologies

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2. Right-click one of the selected nets to access the shortcut menu.
3. Click *Connect*. The selected nets move to the connected nets section. Also, a horizontal line appears between the two tables indicating that one-to-one connectivity has been established between the two selected nets.



Connected Nets		
Net	Pin	Cktnode
dq0	3	
dqs0n	12	
dqs0p	11	
vssq	2	
Unconnected Ground Net(s)		
▼ Unconnected Power Net(s)		
vddq	1	
▼ Unconnected Signal Net(s)		
dq1	4	
dq2	5	

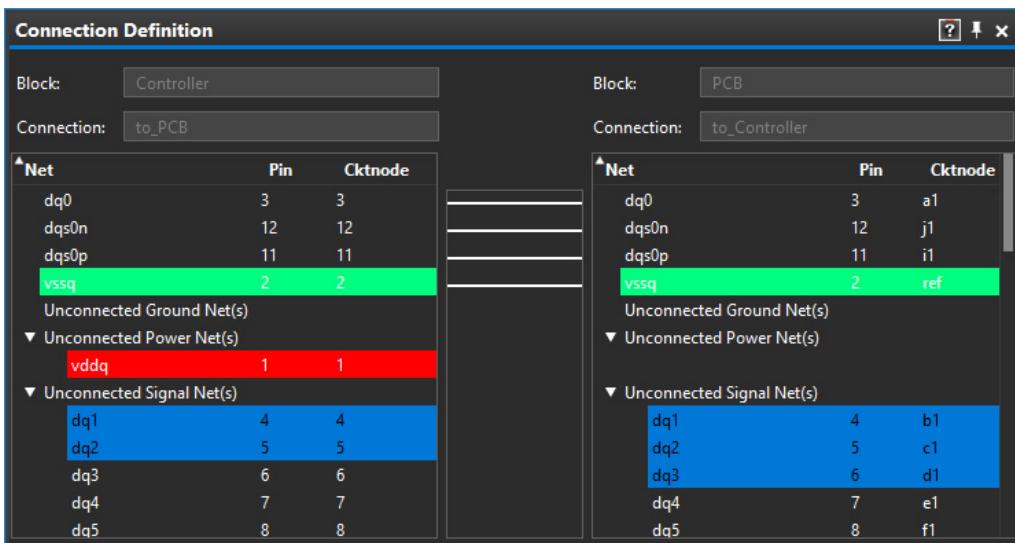
  

Connected Nets		
Net	Pin	Cktnode
dq0	3	
dqs0n	12	
dqs0p	11	
vssq	2	
Unconnected Ground Net(s)		
▼ Unconnected Power Net(s)		
▼ Unconnected Signal Net(s)		
dq1	4	
dq2	5	

### Manually Connecting Unconnected Nets in a Differential Configuration

To connect multiple unconnected nets together in a differential configuration:

1. Select the required nets from the left and right tables in the *Connection Definition* panel. Keep the *Ctrl* key pressed as you select multiple nets.



Connected Nets		
Net	Pin	Cktnode
dq0	3	3
dqs0n	12	12
dqs0p	11	11
vssq	2	2
Unconnected Ground Net(s)		
▼ Unconnected Power Net(s)		
vddq	1	1
▼ Unconnected Signal Net(s)		
dq1	4	4
dq2	5	5
dq3	6	6
dq4	7	7
dq5	8	8

Connected Nets		
Net	Pin	Cktnode
dq0	3	a1
dqs0n	12	j1
dqs0p	11	i1
vssq	2	ref
Unconnected Ground Net(s)		
▼ Unconnected Power Net(s)		
▼ Unconnected Signal Net(s)		
dq1	4	b1
dq2	5	c1
dq3	6	d1
dq4	7	e1
dq5	8	f1

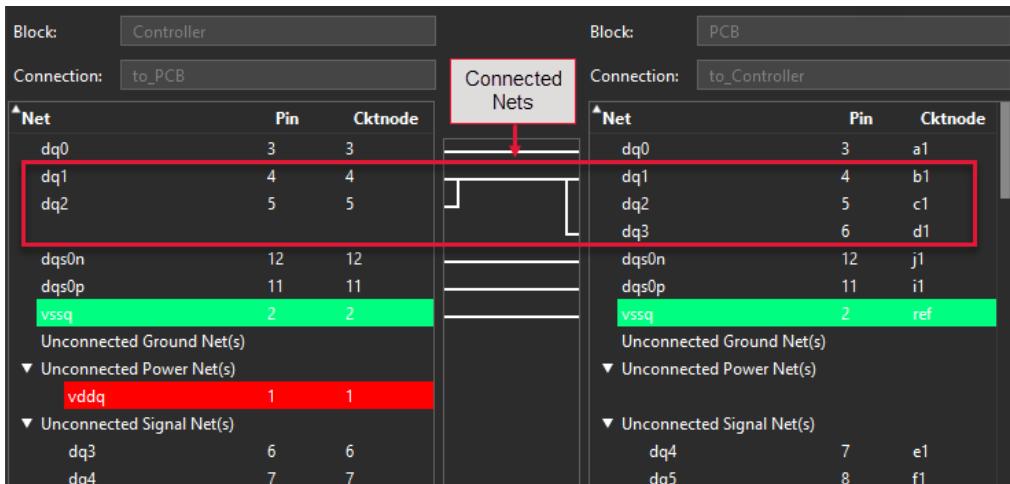
2. Right-click one of the selected nets to access the shortcut menu.

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## Working with Topologies

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- 3.** Click *Connect*. The selected nets move to the connected nets section. The forked lines between the two tables indicate that the selected nets have been connected together.

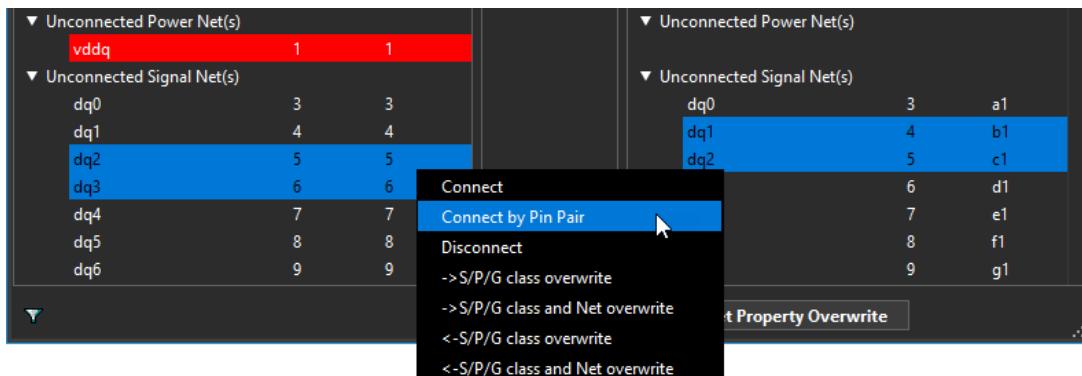


Block: Controller			Block: PCB		
Connection:	to_PCB		Connection:	to_Controller	
Net	Pin	Cktnode	Net	Pin	Cktnode
dq0	3	3	dq0	3	a1
dq1	4	4	dq1	4	b1
dq2	5	5	dq2	5	c1
dqs0n	12	12	dq3	6	d1
dqs0p	11	11	dqs0n	12	j1
vssq	2	2	dqs0p	11	i1
Unconnected Ground Net(s)					
▼ Unconnected Power Net(s)					
vddq	1	1	vssq	2	ref
▼ Unconnected Signal Net(s)					
dq3	6	6	dq4	7	e1
dq4	7	7	dq5	8	f1

### Connecting Multiple Nets by Pin Pairs in a Single-Ended Configuration

To connect multiple nets by pin pair in a single-ended configuration:

- 1.** Select equal number of signals from both left and right tables.



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### Working with Topologies

2. Right-click one of the selected signals and click *Connect by Pin Pair*, which appears as enabled in the displayed menu. Each net selected on one side gets connected to its corresponding selected net on the other side.

The screenshot shows two separate windows representing different blocks:

**Block: Controller**

Net	Pin	Cktnode
dq2	5	5
dq3	6	6
dqs0n	12	12
dqs0p	11	11
vssq	2	2

**Block: PCB**

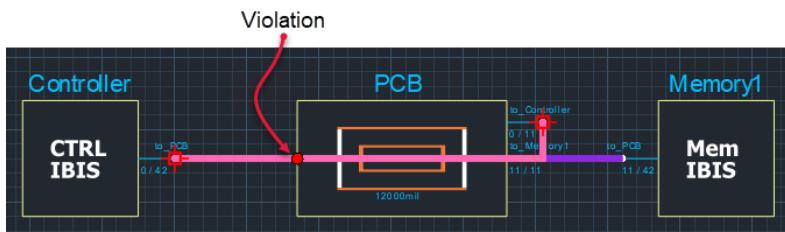
Net	Pin	Cktnode
dq1	4	b1
dq2	5	c1
dqs0n	12	j1
dqs0p	11	i1
vssq	2	ref

A red arrow points from the "Connected Nets" section of the Controller table to the "Connected Nets" section of the PCB table, indicating the connection mapping.

### Routing Pins Automatically

In Topology Workbench, the *Route Auto* option in the shortcut menu lets you establish a routing path between two pins without shorting other blocks or pins. You can use this feature to cleanup and place the blocks while automatically routing the pins on the canvas. In addition, this feature is useful when you want the pins to be routed neatly and correctly in the Allegro topology extraction flow.

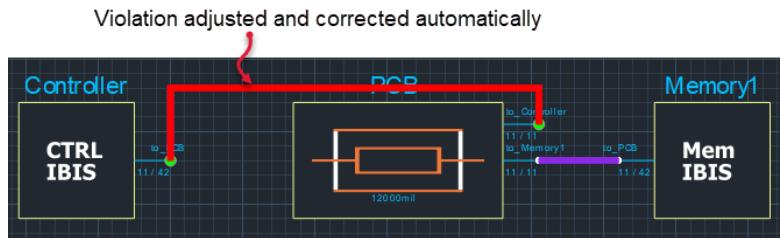
For example, while establishing block-based connectivity between signals using the [Pin-to-Pin Method](#), if the connection illegally overlaps a block, the violation is visually depicted with red highlights as shown below:



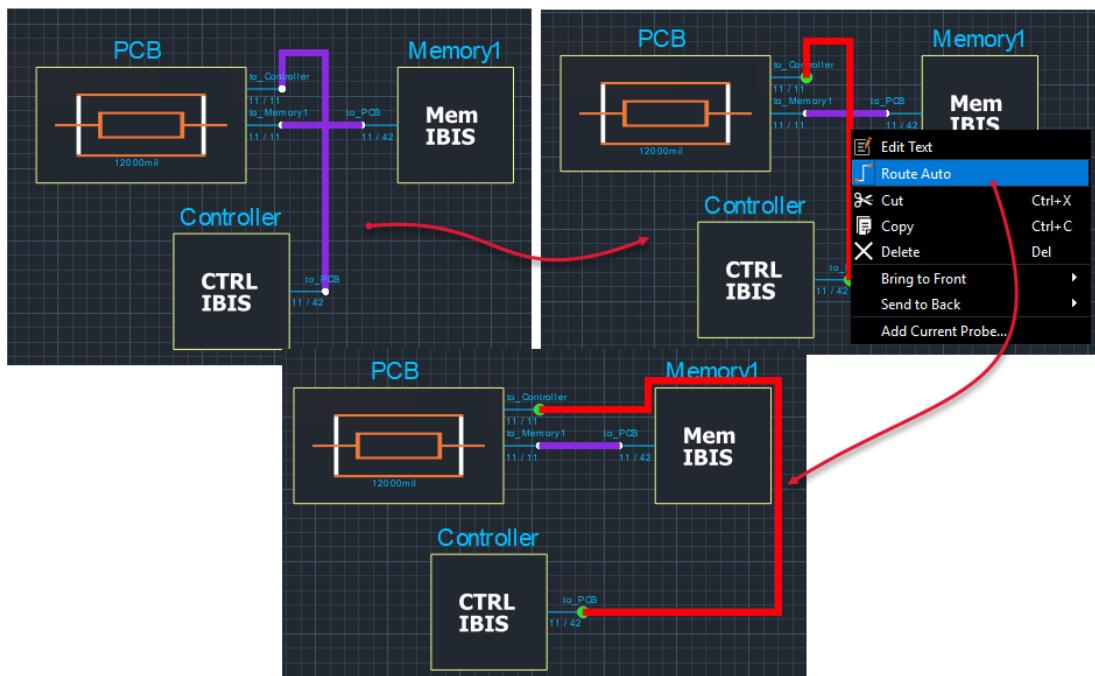
# Topology Workbench User Guide

## Working with Topologies

Once you establish the connectivity, the connection is adjusted automatically to avoid the violation.



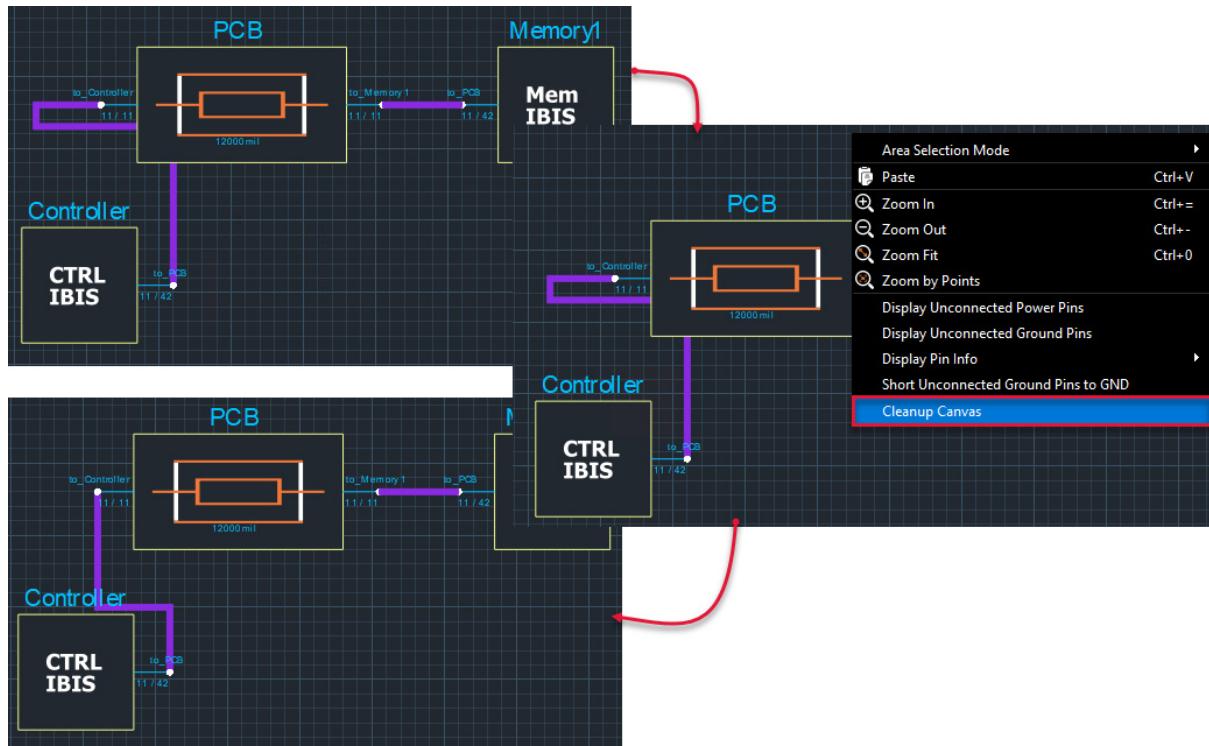
Suppose the connections are overlapping and you want to adjust the routing. Then, select the connection and right-click it to open the shortcut menu. Select the *Route Auto* option to automatically route the connection while avoiding any violations as depicted in the example below:



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## Working with Topologies

The auto-routing feature is also integrated with the *Cleanup Canvas* option of the shortcut menu displayed on a right-click on the canvas. The example below illustrates the automatic routing that happens on selecting the *Cleanup Canvas* option:



## Disconnecting the Nets

If connectivity needs to be terminated between two or more nets, you can do so directly on the canvas using the shortcut menu option or through the *Connection Definition* panel.

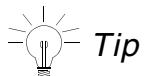
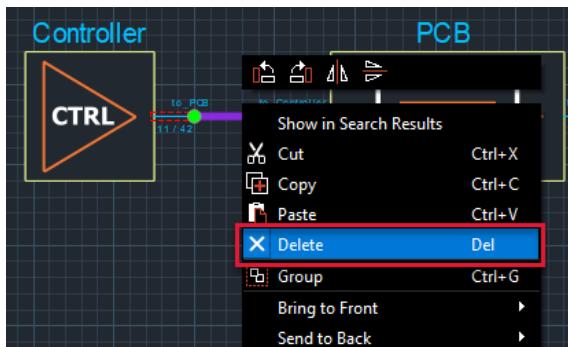
### Disconnect Nets Using the Shortcut Menu

On the canvas,

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1. Select the connection that needs to be terminated.



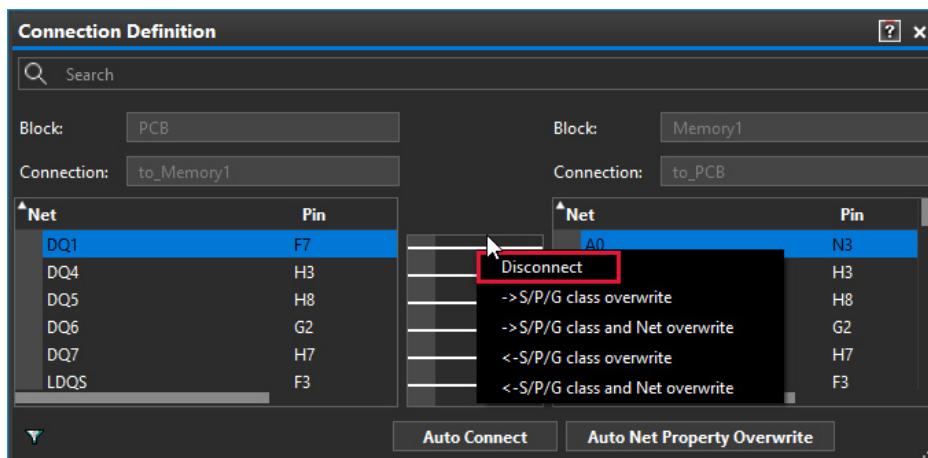
**Tip**  
To select multiple connections on the canvas for disconnecting, keep the **CTRL** key pressed while clicking the required connections.

2. Right-click a selected connection and select *Delete* from the menu.

### Disconnect Nets Using the Connection Definition Panel

In the *Connection Definition* panel,

1. Click the connectivity line for the nets that need to be disconnected. The associated signals appear as highlighted in the left and right tables.



Alternatively, you can select a specific connected net from left or right side table.

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### Working with Topologies

2. Right-click the selected net and click *Disconnect* from the displayed menu. The affected net moves to the section listing the *Unconnected \* Net(s)* depending its type, that is, power, ground, or signal. The connectivity line between these signals is also removed.

<p>Block: PCB</p> <p>Connection: to_Memory1</p> <table border="1" style="width: 100%; border-collapse: collapse;"><thead><tr><th>Net</th><th>Pin</th></tr></thead><tbody><tr><td>▼ Unconnected Signal Net(s)</td><td></td></tr><tr><td>DQ0</td><td>E3</td></tr><tr><td>DQ1</td><td>F7</td></tr></tbody></table>	Net	Pin	▼ Unconnected Signal Net(s)		DQ0	E3	DQ1	F7	<p>Block: Memory1</p> <p>Connection: to_PCB</p> <table border="1" style="width: 100%; border-collapse: collapse;"><thead><tr><th>Net</th><th>Pin</th></tr></thead><tbody><tr><td>▼ Unconnected Signal Net(s)</td><td></td></tr><tr><td>A0</td><td>N3</td></tr><tr><td>A1</td><td>P7</td></tr></tbody></table>	Net	Pin	▼ Unconnected Signal Net(s)		A0	N3	A1	P7
Net	Pin																
▼ Unconnected Signal Net(s)																	
DQ0	E3																
DQ1	F7																
Net	Pin																
▼ Unconnected Signal Net(s)																	
A0	N3																
A1	P7																

### Overwriting Property of Nets and Classes

The *Auto Net Property Overwrite* button in the *Connection Definition* panel can be used to overwrite the properties of the signal, power, and ground net based on the selected criteria.

This functionality is useful when a connection is established between two different types of nets, such as, a signal net is connected to a ground net or a power net is connected to a ground net. A red mark on the connectivity line between such nets indicates that the connection is improper.

**Connection Definition**

<p>Block: Controller</p> <p>Connection: to_PCB</p> <table border="1" style="width: 100%; border-collapse: collapse;"><thead><tr><th>Net</th><th>Pin</th><th>Cktnode</th></tr></thead><tbody><tr><td>dqs0n</td><td>12</td><td>12</td></tr><tr><td>dqs0p</td><td>11</td><td>11</td></tr><tr style="background-color: red;"><td>vddq</td><td>1</td><td>1</td></tr><tr style="background-color: green;"><td>vssq</td><td>2</td><td>2</td></tr><tr><td colspan="3">Unconnected Ground Net(s)</td></tr><tr><td colspan="3">Unconnected Power Net(s)</td></tr><tr><td colspan="3">▼ Unconnected Signal Net(s)</td></tr><tr><td>dq0</td><td>3</td><td>3</td></tr><tr><td>dq1</td><td>4</td><td>4</td></tr><tr><td>dq2</td><td>5</td><td>5</td></tr><tr><td>dq3</td><td>6</td><td>6</td></tr><tr><td>dq4</td><td>7</td><td>7</td></tr><tr><td>dq5</td><td>8</td><td>8</td></tr><tr><td>dq6</td><td>9</td><td>9</td></tr></tbody></table>	Net	Pin	Cktnode	dqs0n	12	12	dqs0p	11	11	vddq	1	1	vssq	2	2	Unconnected Ground Net(s)			Unconnected Power Net(s)			▼ Unconnected Signal Net(s)			dq0	3	3	dq1	4	4	dq2	5	5	dq3	6	6	dq4	7	7	dq5	8	8	dq6	9	9	<p>Block: PCB</p> <p>Connection: to_Controller</p> <table border="1" style="width: 100%; border-collapse: collapse;"><thead><tr><th>Net</th><th>Pin</th><th>Cktnode</th></tr></thead><tbody><tr><td>dqs0n</td><td>12</td><td>j1</td></tr><tr><td>dqs0p</td><td>11</td><td>i1</td></tr><tr style="background-color: green;"><td>vssq</td><td>2</td><td>ref</td></tr><tr><td>dq3</td><td>6</td><td>d1</td></tr><tr><td colspan="3">Unconnected Ground Net(s)</td></tr><tr><td colspan="3">Unconnected Power Net(s)</td></tr><tr><td colspan="3">▼ Unconnected Signal Net(s)</td></tr><tr><td>dq0</td><td>3</td><td>a1</td></tr><tr><td>dq1</td><td>4</td><td>b1</td></tr><tr><td>dq2</td><td>5</td><td>c1</td></tr><tr><td>dq4</td><td>7</td><td>e1</td></tr><tr><td>dq5</td><td>8</td><td>f1</td></tr><tr><td>dq6</td><td>9</td><td>g1</td></tr><tr><td>dq7</td><td>10</td><td>h1</td></tr></tbody></table>	Net	Pin	Cktnode	dqs0n	12	j1	dqs0p	11	i1	vssq	2	ref	dq3	6	d1	Unconnected Ground Net(s)			Unconnected Power Net(s)			▼ Unconnected Signal Net(s)			dq0	3	a1	dq1	4	b1	dq2	5	c1	dq4	7	e1	dq5	8	f1	dq6	9	g1	dq7	10	h1
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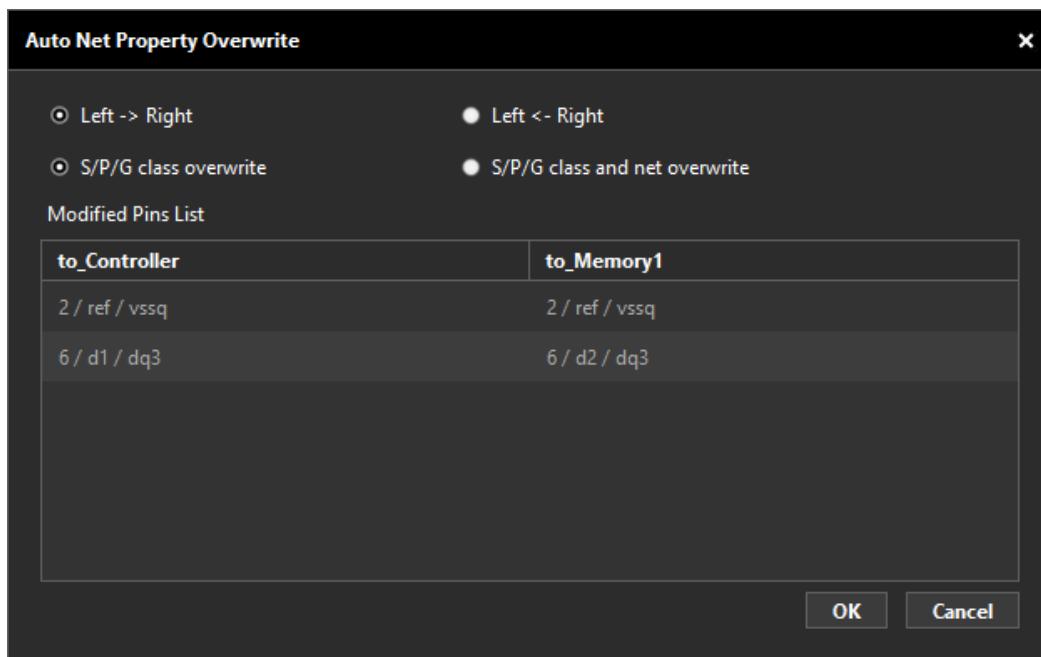
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### Working with Topologies

To resolve the conflict in a connection, overwrite their net properties as explained below:

1. Click *Auto Net Property Overwrite* to open the corresponding dialog box.
2. Select one the following options to define the direction of block in which the overwrite operation should be performed:
  - Left -> Right*
  - Left <- Right*

**Note:** Depending on the selection, the values displayed in the *Modified Pins List* section change to show which block will be impacted by the action. The *->* and *<-* arrows between *Left* and *Right* indicate the direction in which the overwrite should be applied, that is, change the nets of the block on the right as per the block on the left, or the other way round.



3. Select one of the following options to define whether the overwrite operation should impact only the class or the corresponding net name too:

- S/P/G class overwrite*

Changes only the class of the overwritten nets to make it same as that of the master net. For example, if *Left -> Right* is selected along with *S/P/G class overwrite*, and the class of net on the left is ground, then the net on the right will also become a ground net.

- S/P/G class and net overwrite*

Changes the class of the overwritten nets and their names to make them same as that of the corresponding master nets. For example, if *Left -> Right* is selected along with *S/P/G class and net overwrite*, and the class of net on the left is ground and its name is *vddq*, then the net on the right named *vssq* will become a ground net and be renamed as *vddq*.

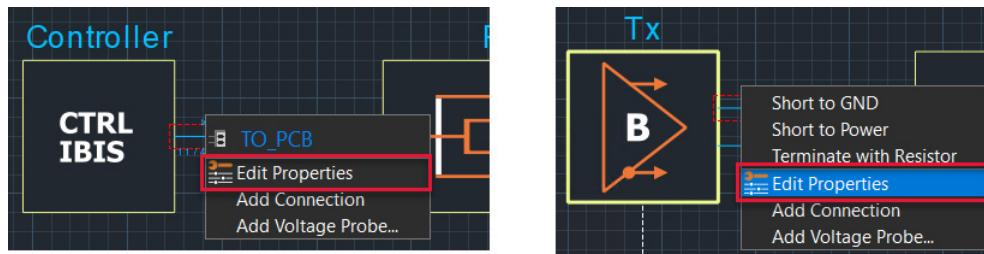
4. Click *OK*. The *Auto Net Property Overwrite* dialog box closes and the table in the *Connection Definitions* panel gets updated as per the defined overwrite criteria.

## Editing the Properties of a Component

Irrespective of the method used to create the design, if required, you can edit the properties defined for each component that is added to the canvas, including blocks, attached pins, associated IBIS files or circuit files, and so on.

Double-clicking a component on the canvas opens the corresponding *Edit Properties* panel that lets you edit the defined properties.

**Note:** To view the properties of the attached pins, you can alternatively right-click the pin and select *Edit Properties* from the shortcut menu.



The editable properties have an *E* button as shown below:

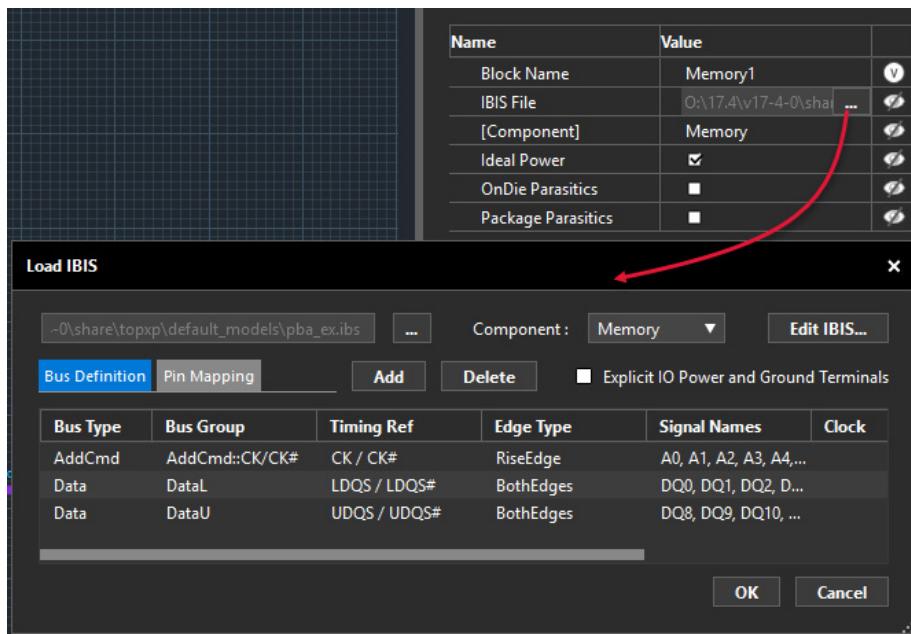
Name	Value
Block Name	Memory1
IBIS File	pba_ex.ibs

A red box highlights the 'E' button in the bottom right corner of the 'Value' column for the 'IBIS File' row. A red arrow points downwards from this button to the text 'Click to edit.'

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### Working with Topologies

Clicking the *E* button makes the value editable within the cell, such as, *Block Name*. Otherwise, the corresponding dialog box is opened. For example, the *Load IBIS* dialog box opens when you click the *E* button adjacent to the *IBIS File* name as shown below.

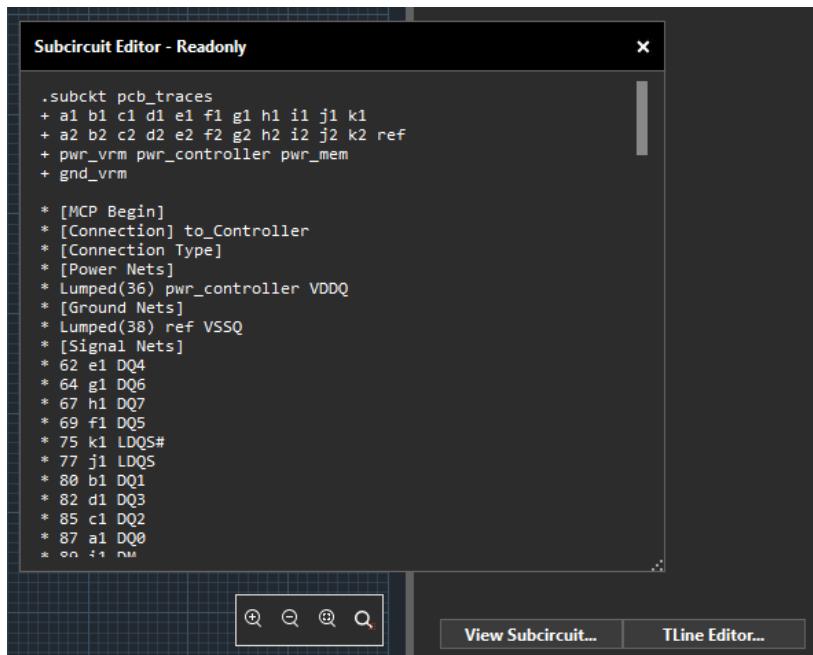


At the bottom of the *Edit Properties* panel, for most components, the *View Subcircuit...* button is provided to open the *Subcircuit Editor* in read only mode as shown below.

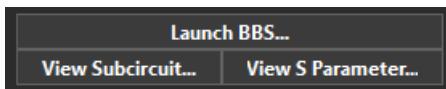
## Topology Workbench User Guide

### Working with Topologies

However, for the following types of blocks, the *Subcircuit Editor* opens in editable mode: Transmitter and Receiver SPICE-Based Blocks, Via Block, and Discrete Block.



For a S Parameter block, the *Edit Properties* panel also provides the *Launch BBS* button to open the Broadband SPICE window and the *View S Parameter* button that opens the related waveform in the BNP Viewer window.

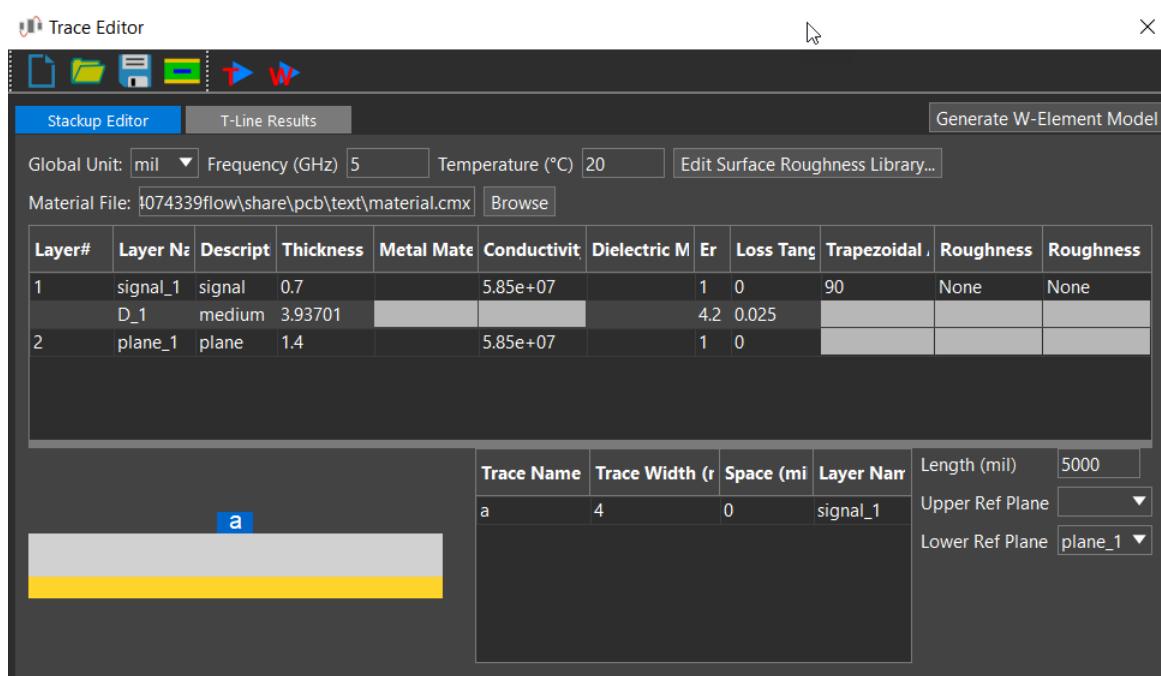


Similarly, the *Edit Properties* panel for a trace block also has a button to open the *Trace Editor* that allows you to *Generate* a TLine based on the updates you make in the editor and

# Topology Workbench User Guide

## Working with Topologies

*Restore Defaults* if needed. For details, see [Appendix C, “Modeling Pre-Layout Transmission Lines.”](#)



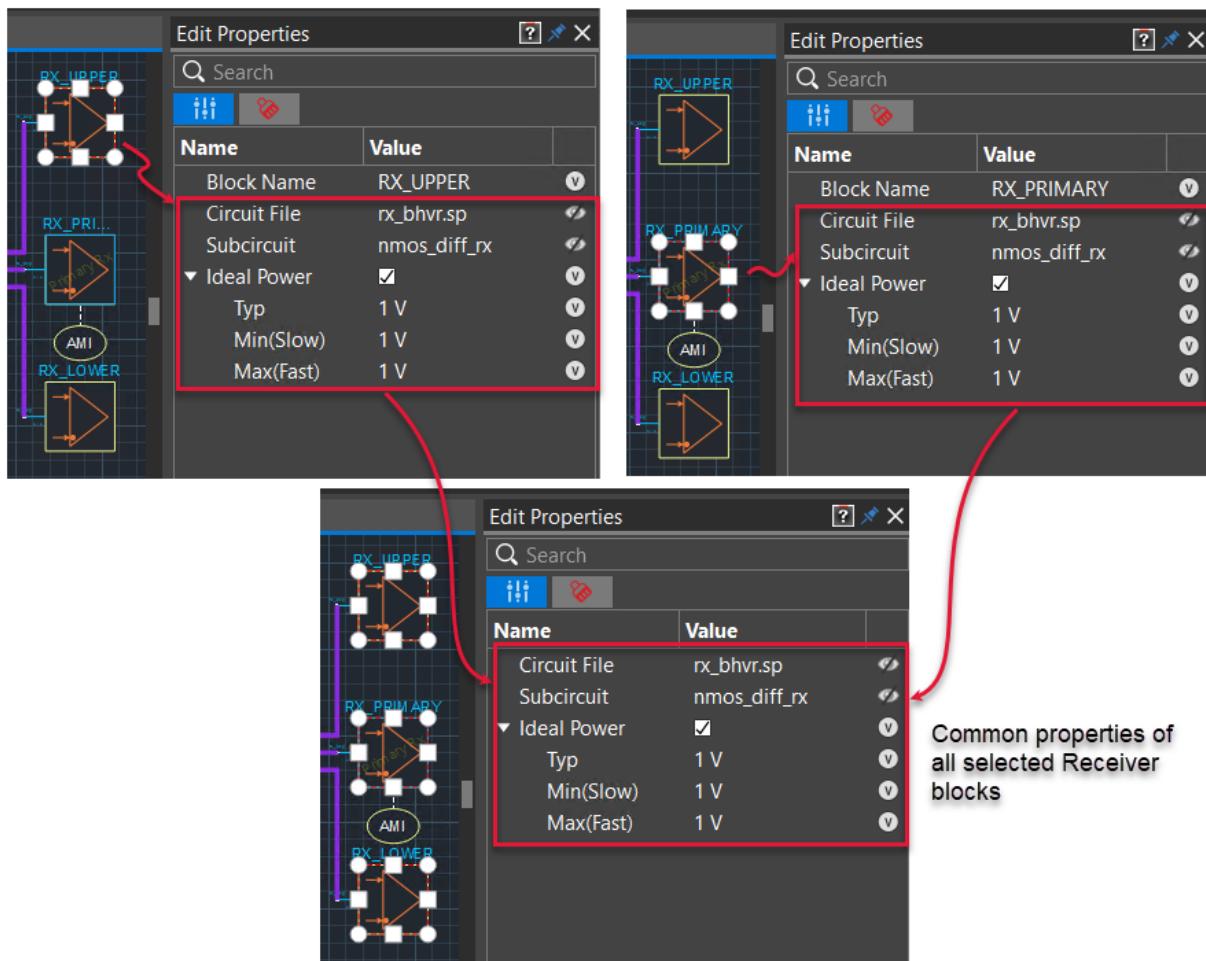
**To utilize benefits of the Trace Editor shown above, ensure that you have installed the latest compatible versions of the following two releases: Sigrity and OrCAD® and Allegro.**

When you select multiple blocks of the same type in the topology, the *Edit Properties* panel displays their common properties. This feature makes modification of the common properties faster and verification for all selected blocks easier. The example shown below illustrates how the *Circuit File*, *Subcircuit*, and *Ideal Power* properties of the three

# Topology Workbench User Guide

## Working with Topologies

selected Receiver blocks are displayed in the *Component Properties* tab of the *Edit Properties* panel:



## Topology Workbench User Guide

### Working with Topologies

#### Editing the Properties of a Block-Based Signal

When you choose to open the *Edit Properties* panel for a block-based signal, a list of all associated nets, pins, and circuit nodes is displayed as shown below.

The screenshot shows a Windows-style dialog box titled "Properties". Inside, there is a search bar and a table with three columns: Net, Pin, and Cktnode. The table contains the following data:

Net	Pin	Cktnode
VDDQ	A1	pwr_mem
VSSQ	B1	ref
A1	E3	a2
LDM	E7	i2
DQ2	F2	c2
LDQS	F3	j2
A1	F7	b2

When you click the *E* button for a Net or Pin, the name becomes editable. However, if you want to remove any pin(s), select the corresponding row, right-click to view the shortcut menu, and choose *Remove Selected Pin(s)*. Similarly, you get the option to set the selected pin(s) as a net group. To select multiple pins for performing an edit operation from the shortcut menu, click the required rows while keeping the *Ctrl* key pressed.

The screenshot shows the same "Properties" dialog box. A row for the pin "F2" under the "DQ2" net has been selected. A context menu is open over this row, displaying the following options:

- Remove Selected Pin(s)
- Set As Power Net Group
- Set As Ground Net Group
- Set As Signal Net Group

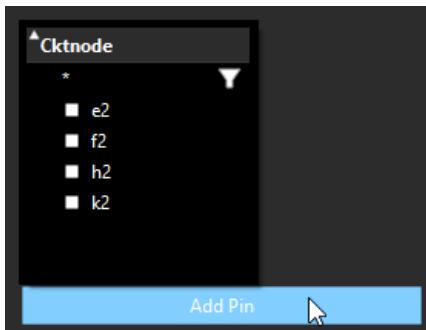
The table data is identical to the one in the first screenshot:

Net	Pin	Cktnode
VDDQ	A1	pwr_mem
VSSQ	B1	ref
A1	E3	a2
LDM	E7	i2
DQ2	F2	c2
LDQS	F3	j2
A1	F7	b2
DQ3	F8	
DQ6	G2	
LDQS#	G3	k2

## Topology Workbench User Guide

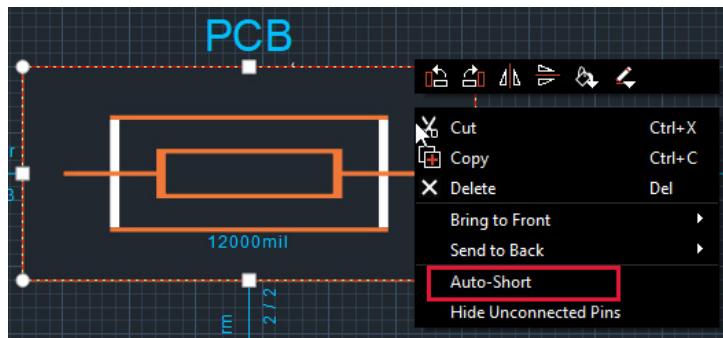
### Working with Topologies

You can also add back any removed pins using the *Add Pin* button. When you click this button, a list of disconnected pins along with check boxes adjacent to their names is displayed. Select the required check boxes and click *Add Pin* again.



## Shorting a Block

If you need to troubleshoot topologies, explore **what-if** scenarios, or pinpoint major noise contributors, you might need to disable a block temporarily, without deleting it. You can short out the subcircuit assigned to a block. Right-click the block to open the shortcut menu and choose *Auto-Short*, as shown below.



Topology Workbench runs connectivity check when a block is auto-short and caches the results for later reuse if needed.

If no matching terminal is found for a signal in the block, Topology Workbench automatically uses a fast frequency sweep to figure out the connectivity.

# Topology Workbench User Guide

## Working with Topologies

*Auto-Short* is available in the Sweep Manager when you select *Spice Models* from the *Sweep Type* list and the *Parameter* option. When you click *Run Sweeps*, on completion of the simulation run, the sweep results for auto-shorting are also shown in the *Result* tab.

The screenshot shows two views of the Sweep Manager. The top view is the 'Setup' tab, where 'Sweep Mode' is set to 'Channel Simulation', 'Sweep Type' is 'Spice Models', and 'Parameter' is selected. A red arrow points to the 'Auto-Short' row in the table, which is set to 'FALSE'. The bottom view is the 'Result' tab, showing a table of iteration results. A red arrow points to the 'Run Sweeps' button at the top right of the 'Setup' tab, and another red arrow points to the 'PCB>Auto-Short' column in the 'Result' table.

Iteration	PCB>Auto-Short	Pkg1>Auto-Short
1	TRUE	TRUE
2	FALSE	TRUE
3	TRUE	FALSE
4	FALSE	FALSE

Iterat	Folder	Eye Contour Height (mV)	Eye Contour Jitter (UI)	Eye Contour NJN	COM (dB)	BER_Eye Height (mV)	BER_Eye Width (UI)	Log BER	Delay (ns)	Intra-Pair Skew (ps)	PCB>Auto
1	res...	985	0.03	*	34.80	945	*	*	*	*	*
2	res...	540	0.12	0.65	15.00	498	0.74	-12	4.45516	26.2354	FALSE
3	res...	985	0.03	0.22	34.80	945	0.82	-12	0.029198	17.3872	TRUE
4	res...	540	0.12	0.65	15.00	498	0.74	-12	4.45516	26.2354	FALSE

## Adding Labels to the Schematic

To support implicit connections in the schematic view of a topology, you can add labels in the in the canvas. Label-based connections enable you to:

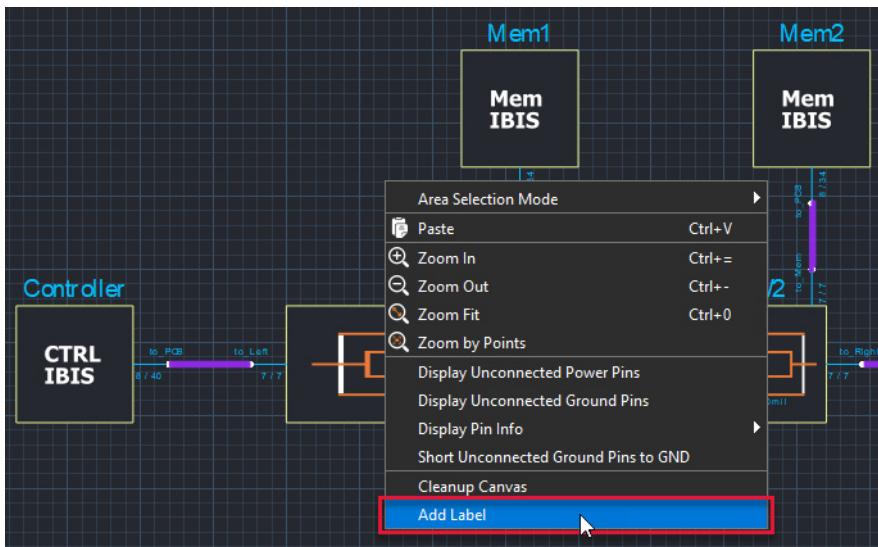
- make explicit wire connections that are easier to modify.
- support connections in the hierarchy and cross-page schematic views.
- make debugging easier when circuit simulation results are not as expected.

To add labels,

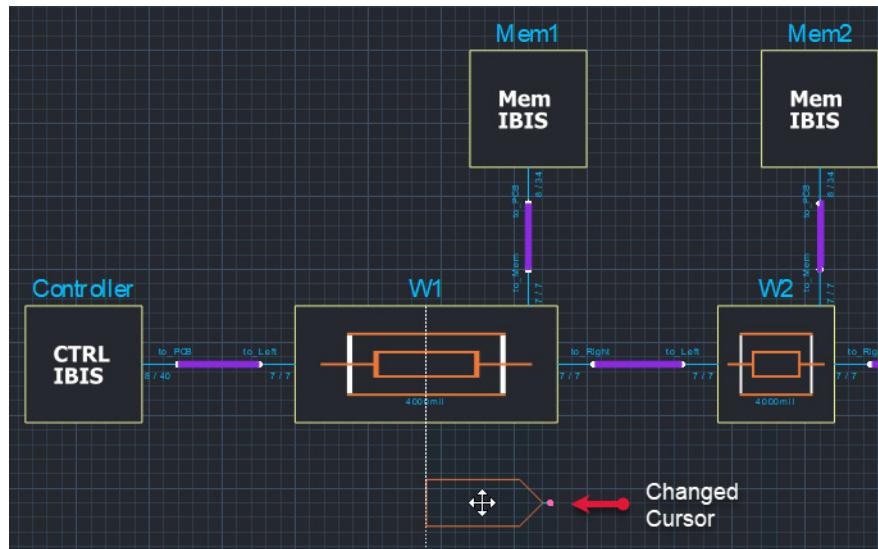
# Topology Workbench User Guide

## Working with Topologies

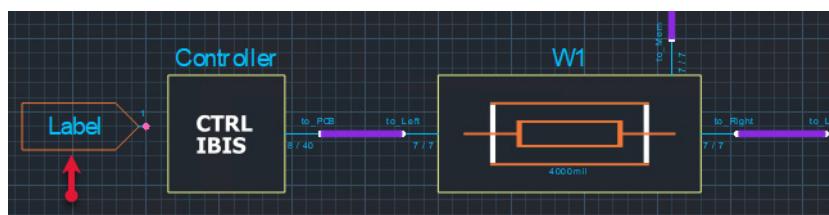
1. Right-click the canvas to open the shortcut menu.



2. Click *Add Label*. The mouse cursor changes to a tag.



3. Move the cursor and click the location where the label needs to be inserted.



4. Double-click the label to type the custom note. If you double-click the text, you can edit it directly in the canvas. If the outer boundary is double-clicked, the Edit Properties panel opens where you can change the *Value of Label Name*.

When the schematic is translated into a SPICE netlist, the locations connected to the labels with the same name are treated as one node.

## Assigning and Editing IBIS Models

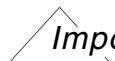
Topology Workbench uses IBIS models and allows both behavioral and transistor-level IO models for the devices used in the topology. It adds certain extensions, including keywords, to these IBIS model files and automates the connection of the IBIS files with other components in the system.

You can assign IBIS models provided by different vendors in the same canvas to the following types of blocks:

- Transmitter (IBIS) and Receiver (IBIS) blocks in the Topology Explorer and SLA workflows
- Controller and Memory blocks in the Topology Explorer and PBA workflows

The assigned IBIS models can also be edited using one of the following ways:

- Edit the IBIS model in the *IBIS Editor* window that can be accessed from the *Load IBIS* dialog box.
- Edit the bus definitions and pin mapping within the *Load IBIS* dialog box. Any changes that you make in this dialog box are updated in the IBIS file too.



Topology Workbench generates the multi-pin connections of the Controller and Memory blocks based on the bus definition, pin mapping, and the setup defined in the *Load IBIS* dialog box. These multi-pin connections cannot be modified.

### IBIS Specification

Topology Workbench supports the most recent IBIS specification. This popular behavioral modeling format is useful for memory system components like controllers and DRAM devices. To read more about IBIS, refer to the following:

- IBIS specification: <http://ibis.org/specs/>

## Topology Workbench User Guide

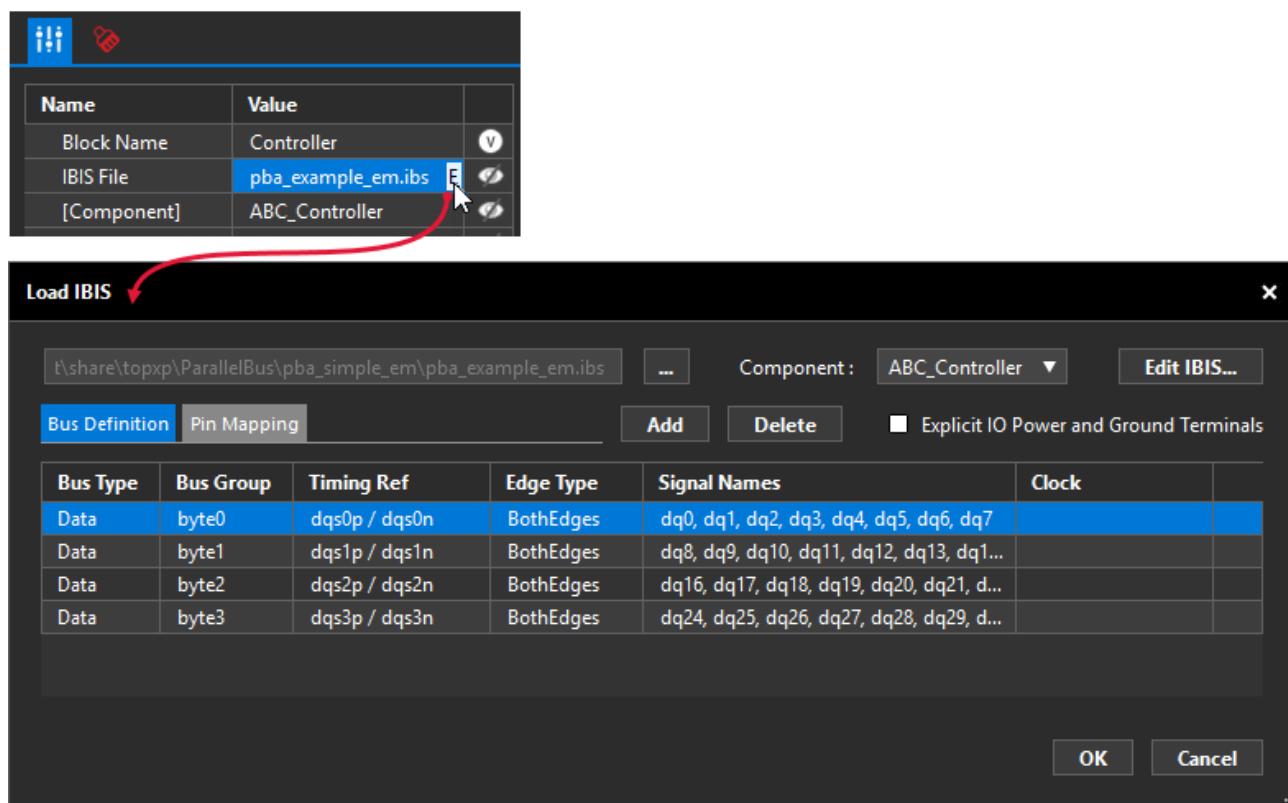
### Working with Topologies

- Pointers to IBIS models of different IC manufacturers: <http://www.eigroup.org/IBIS/ibis%20table/models.htm>

## Opening the Load IBIS Dialog Box

The *Load IBIS* dialog box lets you view the IBIS model definition for the selected block and specify a different IBIS file.

To open this dialog box, click *E* displayed in the *IBIS File* field of the *Edit Properties* panel, as shown below.



By default, the *Explicit IO Power and Ground Terminals* check box in this dialog box is not checked. This means that the circuit node, nets, and pins in a multi-pin connection are determined by the *Pin Mapping* section of the IBIS file.

## Assigning a New IBIS File

When you add a new block that supports IBIS models, Topology Workbench assigns to it a default IBIS file named `ibis.ibs`. This file resides in the following directory:

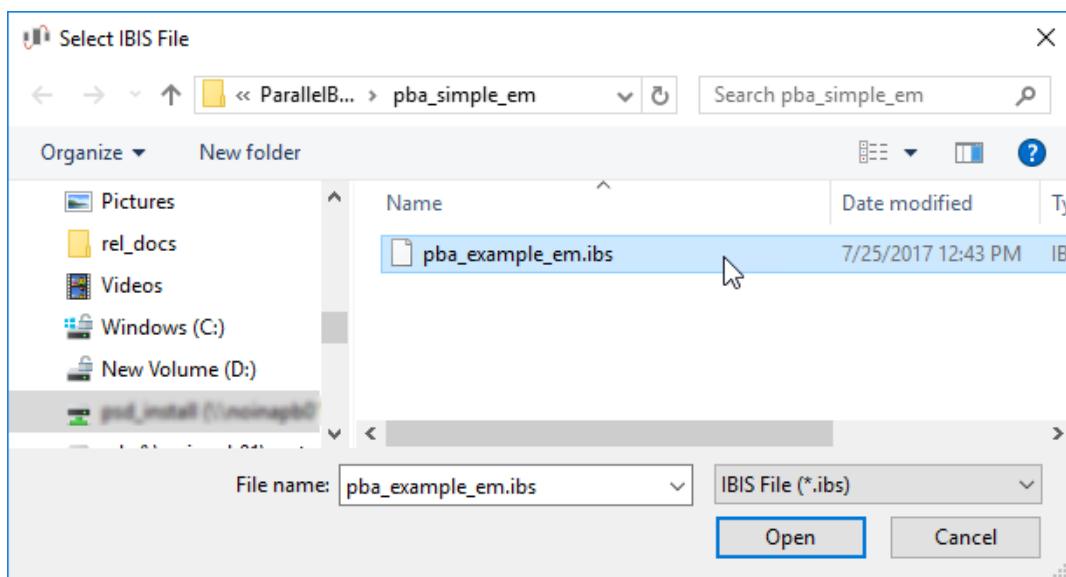
## Topology Workbench User Guide

### Working with Topologies

<INSTALL\_DIR>\share\topxp\default\_models

To replace this default IBIS file with your customized IBIS file:

1. Open the *Load IBIS* dialog box from the *Edit Properties* panel.
2. Click  next to the read-only field displaying the path to the currently assigned IBIS model. The *Select IBIS File* dialog box opens.
3. Browse to the location where the required IBIS model file (\*.ibs) resides on the hard disk and select it.



4. Click *Open*.

## Editing the IBIS File Using the IBIS Editor

The IBIS Editor is an editing tool that provides an easy-to-use editing environment to create, modify, and validate models quickly. It also lets you view IBIS curves, add die or package data, and run golden parser checks to ensure the integrity of the model data circuit simulations.

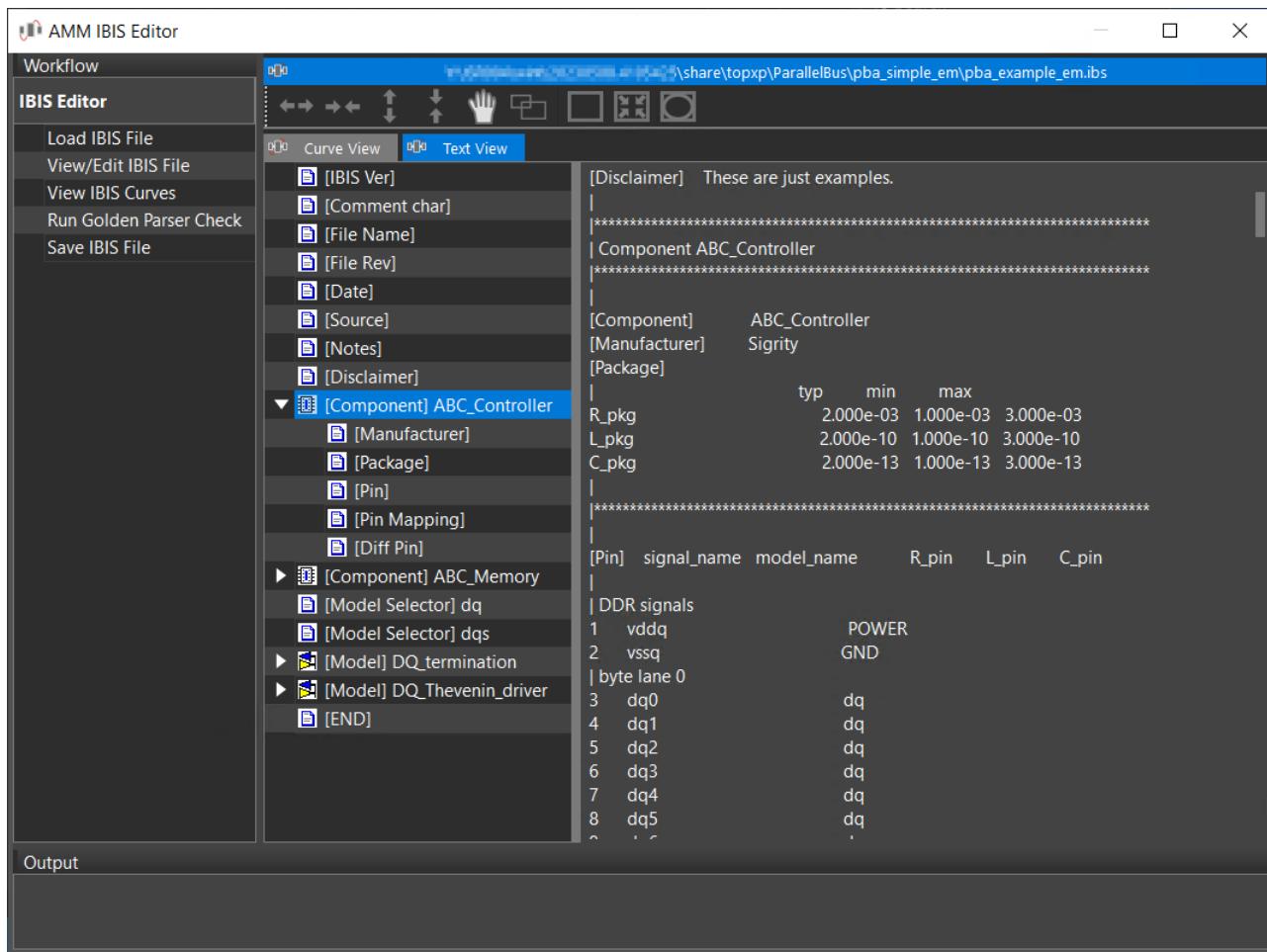
When an IBIS model is used in a Topology Workbench simulation, IBIS 7.0 checks are first run to make sure that there are no errors and then required simulation proceeds. If the IBIS file does not pass the golden parser checks, Topology Workbench generates an error message and saves the IBIS check errors in a log file if the *Run Golden Parser Check before Simulation* check box is selected in the *Message* module of the *Options* dialog box. You can disable the messages by selecting the check box in the message box that is displayed. It automatically deselects the *Run Golden Parser Check before Simulation* check box as well.

# Topology Workbench User Guide

## Working with Topologies

In Topology Workbench, to open the IBIS Editor, use one the following ways:

- Choose *Tools – IBIS Editor* from the menu bar. A blank AMM IBIS Editor window opens where you can open the required IBIS File and edit it.
- or-
- Open the *Load IBIS* dialog box from the *Edit Properties* panel of the selected block and click *Edit IBIS*. The IBIS file assigned to the selected block opens in the IBIS Editor window as shown below.



If required, you can modify the IBIS file, view IBIS curves, add die or package data, and run golden parser checks.

## **Editing an IBIS Model File in the Load IBIS Dialog Box**

The *Load IBIS* dialog box provides the following tabs that map to the corresponding keywords in the IBIS file:

- Bus Definition (in the PBA workflow)
- Pin Mapping (in the PBA, SLA, and Topology Explorer workflows)
- Single-ended Pin (in the SLA and Topology Explorer workflows)
- Diff Pin (in the SLA and Topology Explorer workflows)

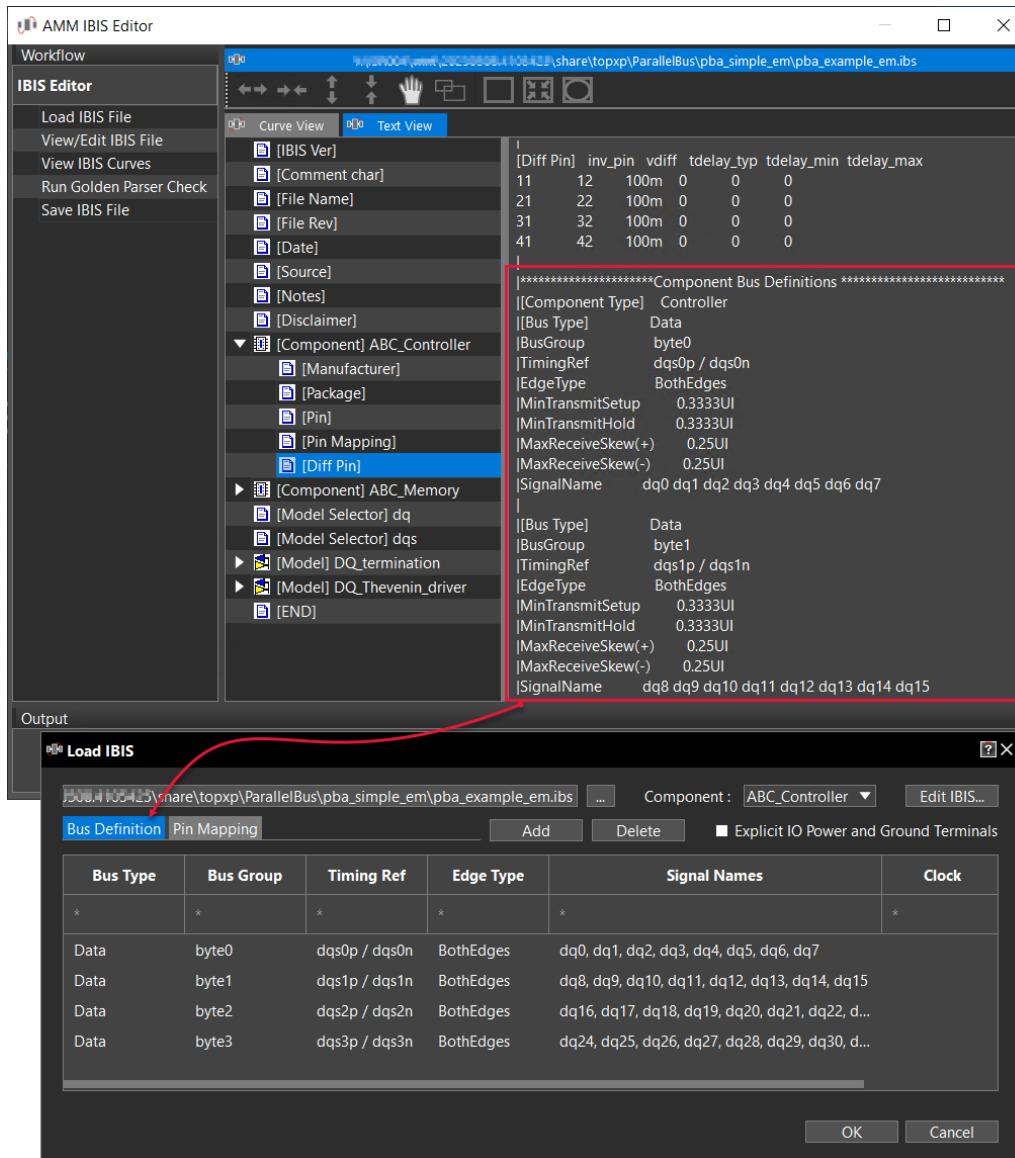
### **Bus Definition**

Parallel Bus Analysis workflow provides the ability to define signals as a bus and identify timing reference signals for the bus. You can edit the standard IBIS file of the Controller and Memory blocks to define specific bus parameters to be included in the simulation-based analysis conducted using Topology Workbench. The bus definitions are captured in the

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## Working with Topologies

[Diff Pin] section of an IBIS file, the details of which are shown to you in the *Bus Definition* tab of the *Load IBIS* dialog box.



The *Component Bus Definitions* classify the buses into three categories—Clock, Address, and Data. Though bus categorization information can be added to the IBIS file through a text editor like IBIS Editor, it is highly recommended that the Topology Workbench – Parallel Bus Analysis GUI is used to create the bus definition.

To add or update the bus definitions in PBA workflow:

1. Open the *Bus Definition* tab in the *Load IBIS* dialog box.

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### Working with Topologies

In this tab, signals are classified into different categories, the timing reference signal for that group is identified, the clocking scheme is defined, and for '*Data*' *Bus Types*, the associated clock signal is identified to enable write-leveling functionality.

2. Click *Add*. A new blank row is added to the table with *Bus Type* set to *Data* and *Edge Type* to *BothEdges* by default.

Bus Definition		Pin Mapping		Add	Delete	<input type="checkbox"/> Explicit IO Power and Ground Terminals
▲ Bus Type	Bus Group	Timing Ref	Edge Type	Signal Names	Clock	
Data	byte0	dqs0p / dqs0n	BothEdges	dq0, dq1, dq2, dq...		
Data	byte1	dqs1p / dqs1n	BothEdges	dq8, dq9, dq10, d...		
Data	byte2	dqs2p / dqs2n	BothEdges	dq16, dq17, dq18, ...		
Data	byte3	dqs3p / dqs3n	BothEdges	dq24, dq25, dq26, ...		
Data			BothEdges			

3. Specify the following information in the corresponding table cells: *Bus Type*, *Bus Group*, *Timing Ref*, *Edge Type*, *Signal Names*, and *Clock* (if needed). For details, see [Knowing the Fields on the Bus Definitions Tab](#).
4. Click *OK* to accept the changes incorporated in the *Bus Definition* tab.
5. Click *Yes* in the message box that is displayed seeking your confirmation. This will back-annotate the changes to the IBIS file.

**Note:** Bus names and signal names for Controller and Memory are local to the IBIS file, and do not have to match each other, nor do they have to match the names in other components, including the Controller. Pin names, however, are used to automate connectivity between components that have a physical connection.

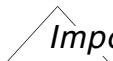
#### ***Knowing the Fields on the Bus Definitions Tab***

- *Bus Type*: Corresponds to the types of signals found in the selected component. A bus can be one of the following types:
  - *Data* – Used for the Data IO (DQ) and Data Mask (DM) signals  
Topology Workbench handles the *Data* bus type in a unique way. These bus types are assumed to drive bi-directionally for Read and Write, and can have adjustable launch delays based on write leveling.
  - *Ctrl* – Used for the control signals, such as Clock Enable (CKE), Chip Select (CS), and On-Die Termination (ODT) signals
  - *AddCmd* – Used for the Address and Command signals, such as Address (A), Bank Address (BA), and Command Inputs RAS, CAS, and WE

- ❑ *Bus Group*: Enables you to assign an intuitive name to the bus being defined.
- ❑ *Timing Ref*: Specifies the timing reference signal used to clock the bus.
  - For *Data* signals, this can be a unique Data Strobe signal for each byte lane.
  - For *Ctrl* and *AddCmd*, this can be the Clock signal.
- ❑ *Edge Type*: Specifies what edges of the *Timing Ref* signal is used to latch in the signals that are a member of the bus identified in the *Signal Names* column.
  - For *Data* signals, both edges of the Data Strobe are typically used (dual data rate).
  - For *Ctrl* and *AddCmd*, the rising edge of the clock signal is historically used, although both edges of the *Clock* are sometimes used for Address buses in higher data rate interfaces.
- ❑ *Signal Names*: Enables the signals that are members of the *Bus Group* that is being identified.
- ❑ *Clock*: For *Data Bus Groups*, a *Clock* (CK) signal can be identified to enable automated write leveling.

### Pin Mapping

The [Pin Mapping] section in an IBIS file is required by Topology Workbench for simulations with non-ideal power, for example to consider the SSN effects. However, in the IBIS specification, this section is considered optional and some components do not have the pin mapping defined. In such cases, Topology Workbench automatically defaults to an *Ideal Power* mode for all simulations.



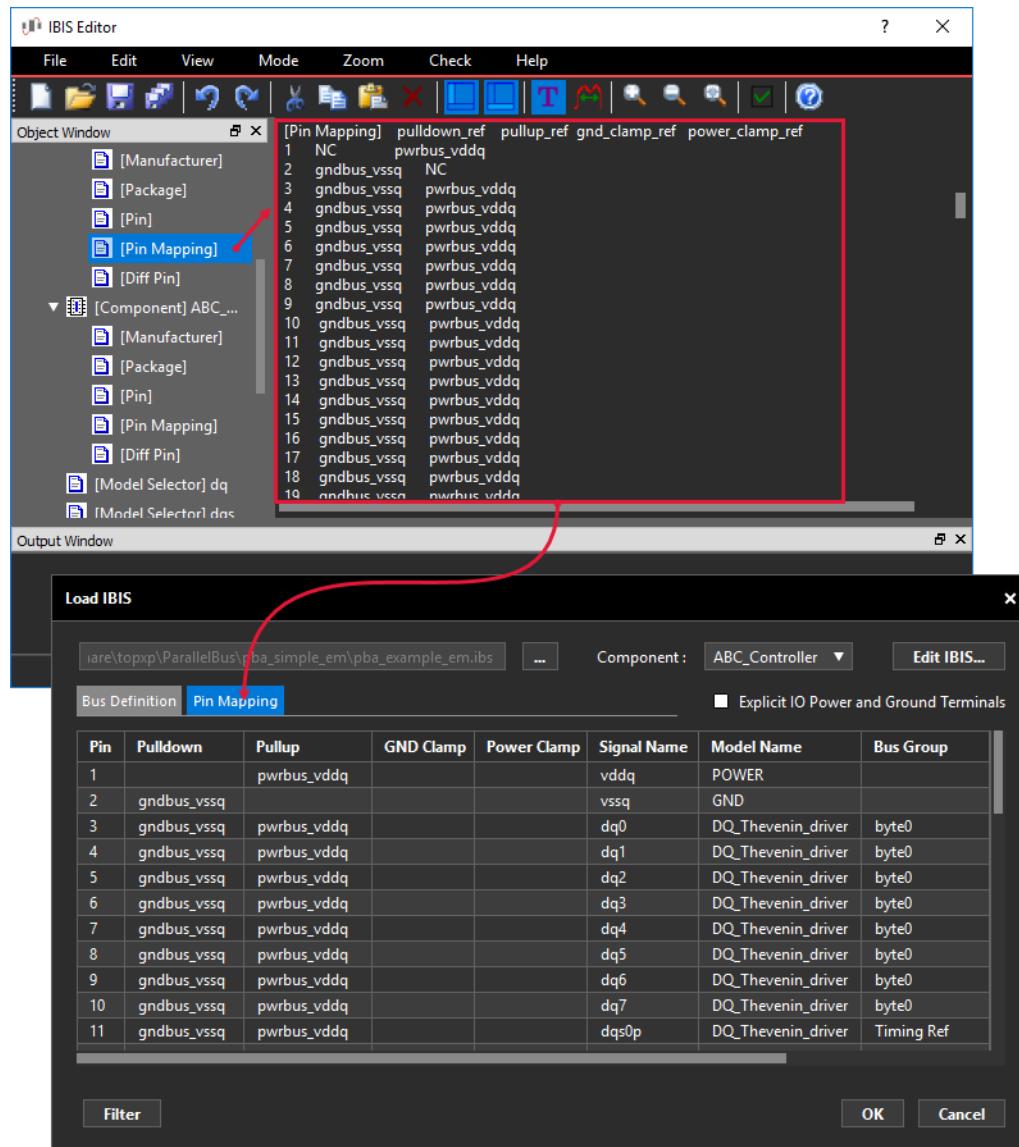
#### *Important*

To get access to all of the powerful features of the tool, including non-ideal power simulation, it is strongly recommended that a valid [Pin Mapping] section is added to the IBIS file prior to its use in Topology Workbench. A valid pin-mapping specification can be obtained from the device manufacturer and included in the IBIS file.

# Topology Workbench User Guide

## Working with Topologies

The *Pin Mapping* tab in the *Load IBIS* dialog box is an equivalent to the [Pin Mapping] section of the IBIS file, as shown below.

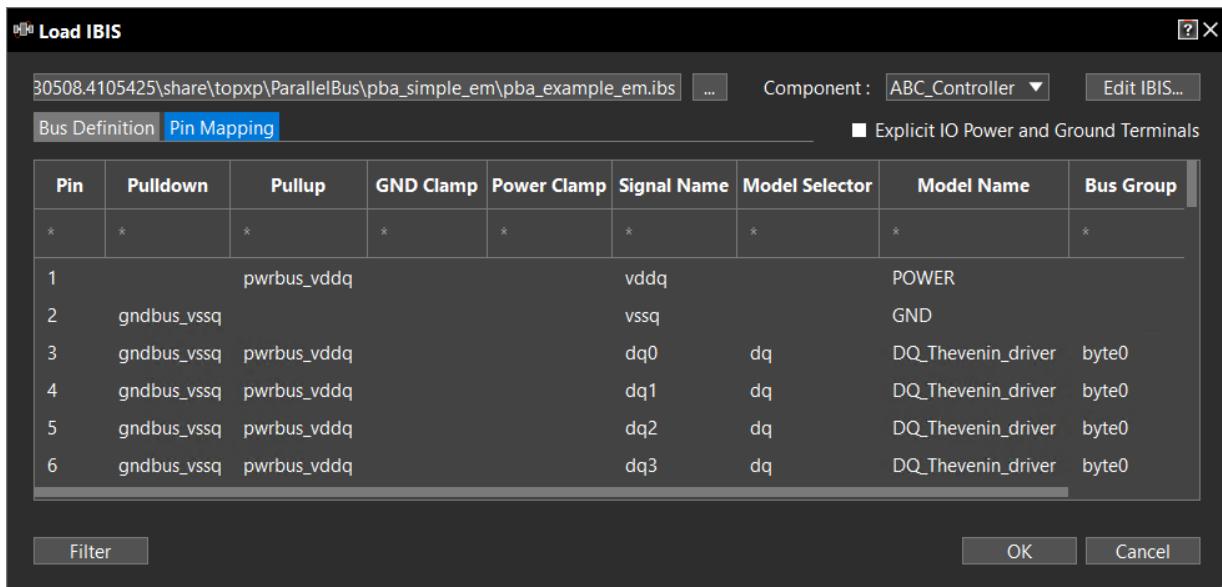


To add or update pin mapping details in the PBA, SLA, or Topology Explorer workflows:

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## Working with Topologies

1. Open the *Pin Mapping* tab in the *Load IBIS* dialog box.



This tab contains the following important information that Topology Workbench requires for analysis:

- The references, including *Pulldown*, *Pullup*, *GND Clamp*, and *Power Clamp* for the listed signals, are identified. These are the only four fields that you can edit in the *Pin Mapping* tab. Without this information, Topology Workbench uses the defaults for the ideal power and ground in all simulations.
- The *Pin* name to *Signal* name mapping is shown in the table. These pin names are used to connect the components together during the analysis.
- The *Model Selector* column corresponds to the `[Model Selector]` keyword in the IBIS model file. It is used to pick a model from a list of unique model parameters for a pin that uses a programmable buffer. The `[Model Selector]` keyword's value must match the corresponding *Model Name* listed under the `[Pin]` keyword.
- The relevant *Bus Group* (assuming that the bus definitions are already specified) is also listed for each pin to signal mapping.

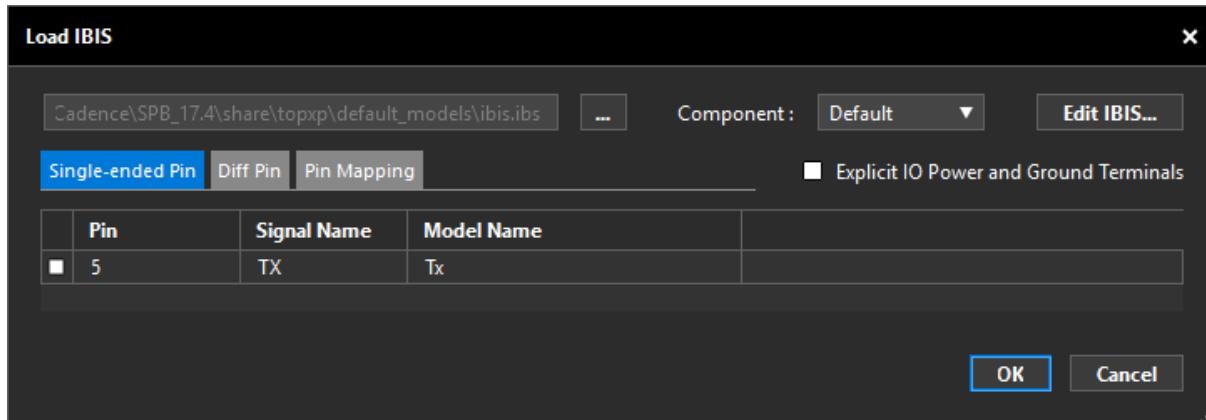
2. Click *OK* to save the changes. To close the pin mapping without saving, click *Cancel*.

## Topology Workbench User Guide

### Working with Topologies

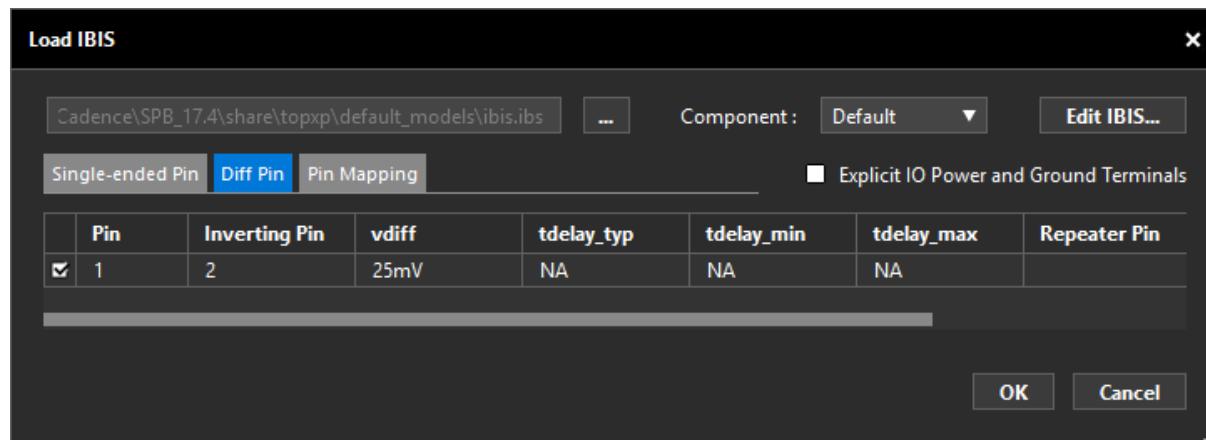
#### Single-ended Pin

The *Single-ended Pin* tab is available in the SLA and Topology Explorer workflows to allow you to select the single-ended signals. The selected signals are available for connection in the *Connection Definition* panel.



#### Diff Pin

The *Diff Pin* tab is available in the SLA and Topology Explorer workflows to allow you to select differential signals. On selecting a differential signal, both the signals in the differential pair are selected.

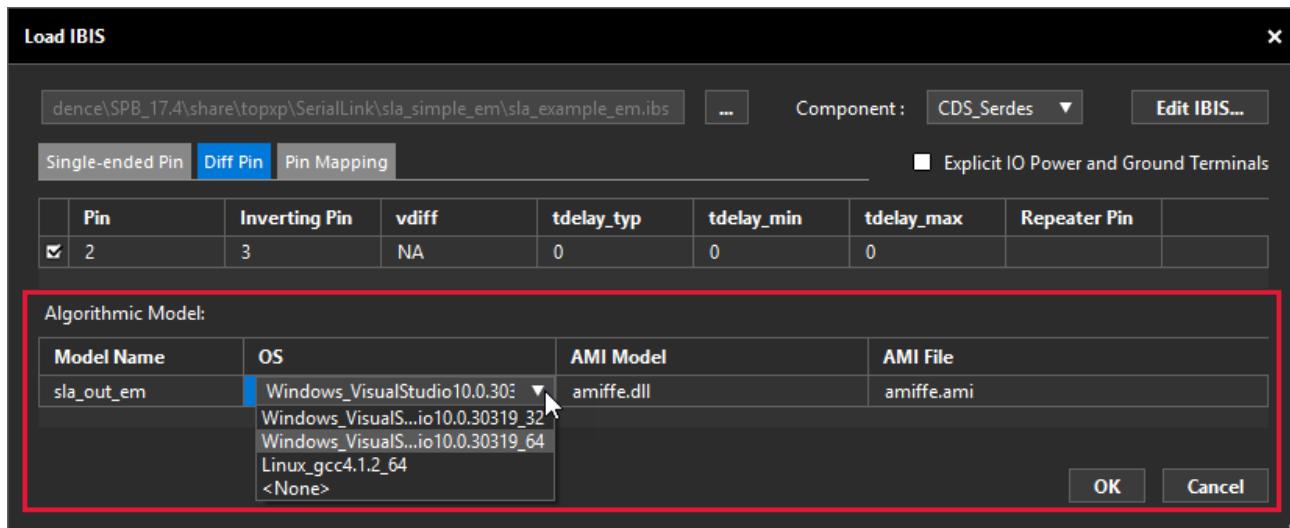


**Note:** For some licenses, Topology Workbench allows a maximum of four enabled signals to be simulated together. A differential pair of signals is treated as one signal.

## Topology Workbench User Guide

### Working with Topologies

When an AMI model is associated with the selected block, the *Algorithmic Model* section is also displayed on the *Diff Pin* tab.



Here, the name of the compiled library file is displayed in the *AMI Model* column and the AMI parameter file in the *AMI Model* column. The operating system used for compiling these files is displayed in the *OS* column, which is the only editable field in the *Algorithmic Model* section.

## Assigning and Extracting S Parameter Files

S Parameters describe the input-output relation between ports (or terminals) in a block. Using Topology Workbench, you can perform the following actions related to S Parameters:

- [Adding and Loading an S Parameter Block](#)
- [Viewing an S Parameter File](#)
- [Extracting an S Parameter Definition](#)
- [Setting Up the Default Pin Location](#)

### Adding and Loading an S Parameter Block

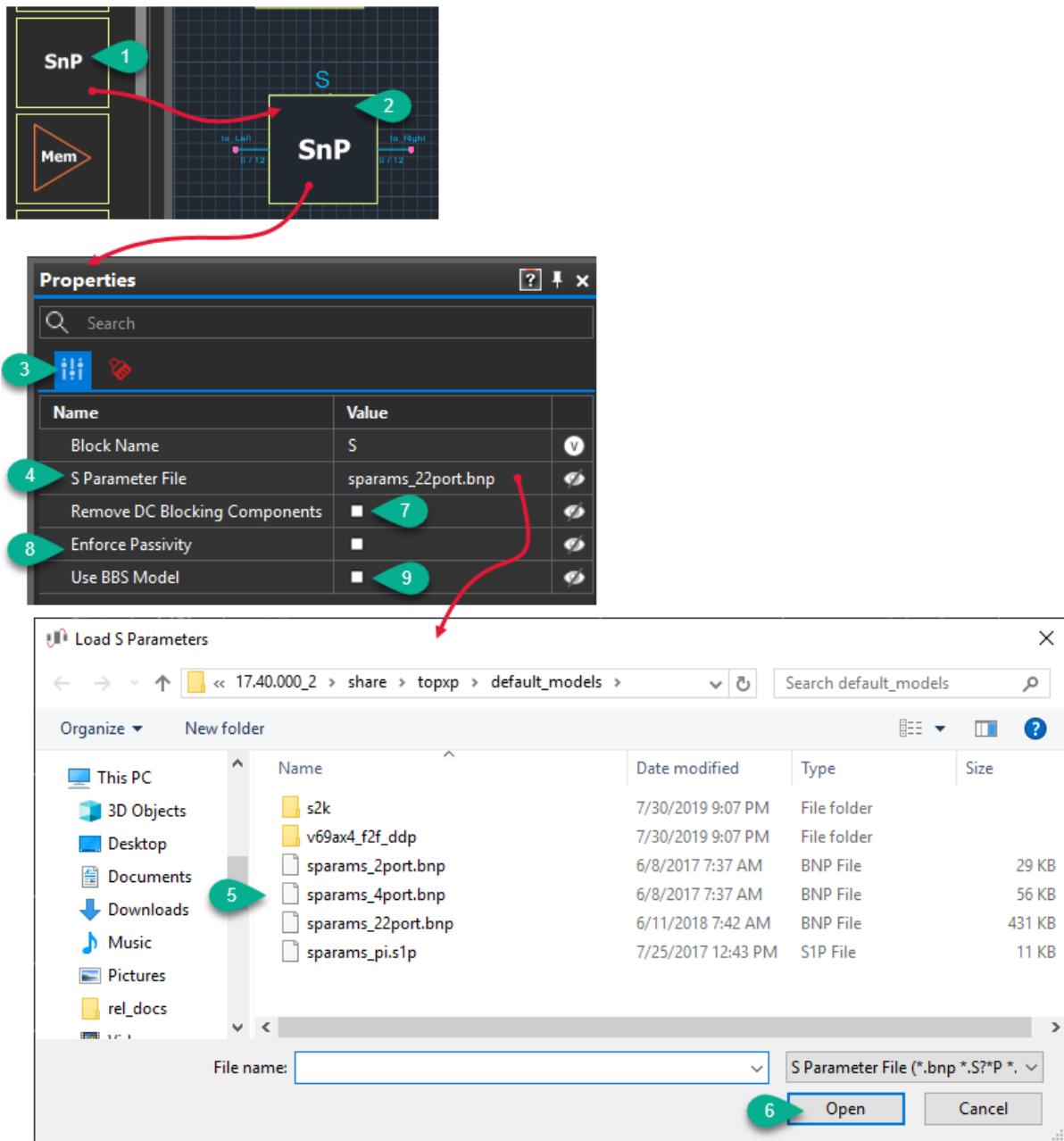
To add and configure an S Parameter block:

1. Click the *SnP* (S Parameter) block in the [Floating Toolbar](#) and drag the pointer to the canvas location where the block needs to be placed.

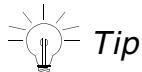
# Topology Workbench User Guide

## Working with Topologies

2. Click the canvas to release the *SnP* block.
3. Double-click the *SnP* block. The Edit Properties Panel opens.



4. Click the *E* button in the cell adjacent to the *S Parameter File* field. The *Load S Parameters* dialog box opens to let you specify an S Parameters file that needs to be attached to the block.



*Tip*

Alternatively, you can click the *Load S Parameters* button in the *Edit Properties* panel.

5. Browse and select the required S Parameter (BNP or Touchstone) file.
6. Click *Open* in the *Load S Parameters* dialog box. The path to the selected file is displayed in the *S Parameter File* field.
7. Select the *Remove DC Blocking Components* check box. This helps when simulating serial links or parallel buses with extracted S-Parameters that include AC coupling capacitances. This setting can be controlled on a block-by-block basis.

**Note:** A new S Parameter file gets created, and used in simulation, in the same folder as the original file if DC blocking components are detected and the *Remove DC Blocking Components* option is selected.

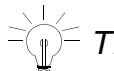
8. Select the *Enforce Passivity* check box to check passivity of the input S-element and perform passivity enforcement process if passivity violations exist. This setting can be controlled on a block-by-block basis.



*Important*

A new subcircuit file is created and used in simulation if the following conditions apply:

- DC blocking components detected and the *Remove DC Blocking Components* option is selected.  
*-OR-*
  - The *Enforce Passivity* option status (selected or not) is not the default Touchstone option of the selected simulator.
9. Select the *Use BBS Model* check box to automatically load the BBS models generated by Broadband SPICE for the S Parameter or Touchstone file. The latest BBS model is displayed at the top in the list. If there are no BBS models available for the subcircuits with an S Parameter model, the Broadband SPICE window opens.



*Tip*

Clicking the *Launch BBS* button also lets you open the Broadband SPICE window, if required.

# Topology Workbench User Guide

## Working with Topologies

If you loaded a BNP file that has information about multi-pin connections, the related section gets automatically added to the S Parameter file for connection.

For the Touchstone file, or the BNP file that does not have the multi-pin connection information, you will have to manually add the information.

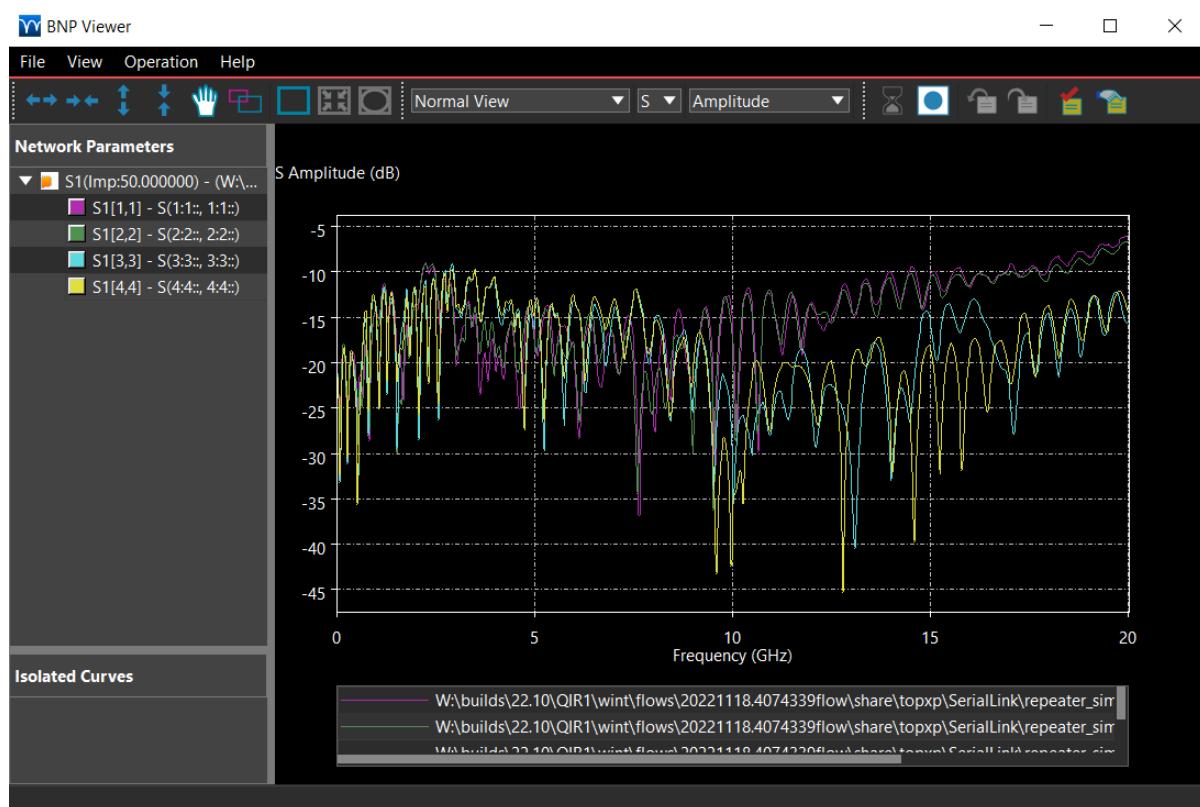


***Editing an S Parameter file for the S Parameter definitions is NOT recommended. Therefore, when View Subcircuit is clicked in the Edit Properties panel, the Subcircuit Editor opens in read-only mode.***

## Viewing an S Parameter File

To view the S Parameter file that is attached to a block:

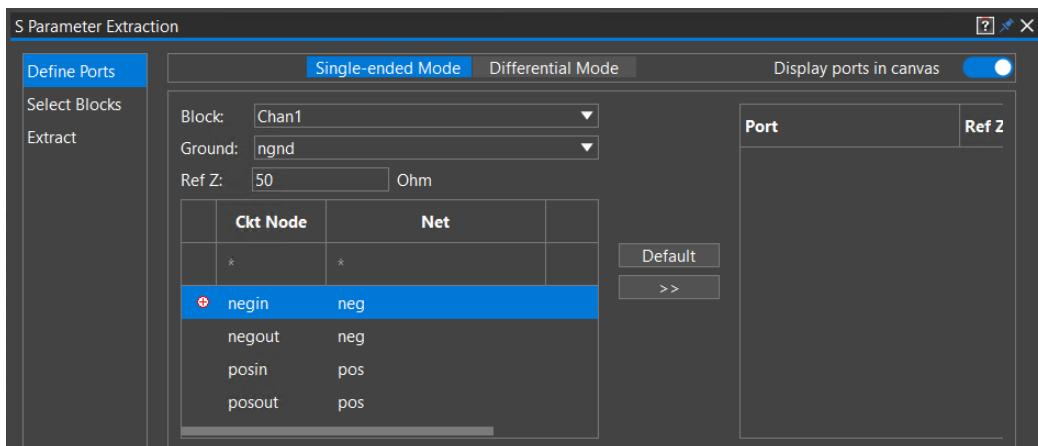
1. Double-click the block on the canvas to open the corresponding [Edit Properties Panel](#).
2. Click *View S Parameter*. The BNP Viewer window opens for reviewing the S Parameters for the selected block, as shown below:



## Extracting an S Parameter Definition

Topology Workbench supports *S Parameter Extraction* for both single-ended nets and differential nets. To extract the S Parameter definition:

1. Choose *Tools – S Parameter Extraction* from the menu bar. The *S Parameter Extraction* panel opens where the *Define Ports* module is selected by default.
2. Select the mode from the two available options, *Single-ended Mode* or *Differential Mode*.
3. Select the *Block* from the list of blocks that have S Parameter model files assigned to them.
4. Select the *Ground* net from the list.
5. Specify the *Ref Z*, that is, reference impedance value in the text box. It is set to 50 Ohm by default.



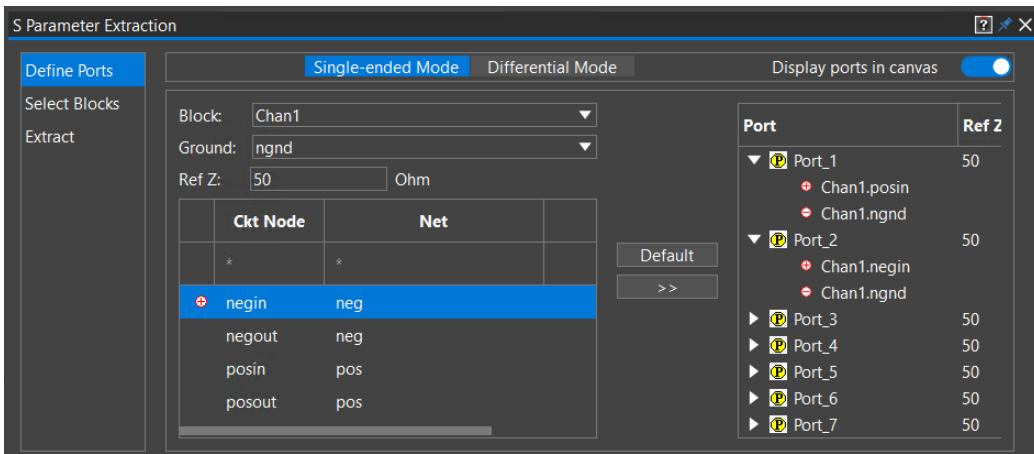
6. Select the required *Ckt Node* from the table and click the *>>* button placed in the middle of the two sections. This action is allowed only when you select *Single-ended Mode* for S Parameter extraction. Repeat this step for the other circuit nodes if they need to be defined as ports as well. Alternatively, click *Default* to let Topology Workbench automatically identify the *Port* to *Ref Z* information and display it in the table on right. For *Differential Mode*, you can only click the *Default* button.

In the *Port* list, a ground node is added as the negative node. By default, the specified *Ref Z* (reference impedance) value is assigned as the port impedance for each port. If

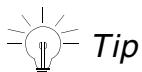
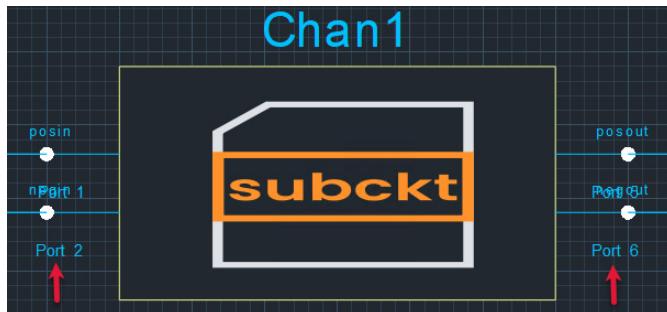
## Topology Workbench User Guide

### Working with Topologies

a different impedance is required for a port, double-click the corresponding cell under the *Ref Z (Ohm)* column and edit the value.



The *Display ports in canvas* toggle button is selected by default. This ensures that if you have defined ports on a circuit node, it is clearly highlighted on the canvas as shown in the image below. It is useful information when there are more than two ports in the design because matching the port numbers with pin numbers becomes easier.



To exclude a specific port from S Parameter extraction, right-click the port in the table and click *Delete Selected Port* from the shortcut menu.

7. Click the *Select Blocks* module from the section on left.

## Topology Workbench User Guide

### Working with Topologies

8. Select the check boxes in the *Include in S-Parameter Model* column that are adjacent to the required blocks.

Define Ports	Include in S-Parameter Model	Block	Model
Select Blocks	<input checked="" type="checkbox"/>	Chan1	channelA
Extract	<input checked="" type="checkbox"/>	Chan2	channelB

9. Click the *Extract* module from the section on left.

Starting Freq.	Ending Freq.	Sweeping Mode	# of Freq. Points	Points/Decade
0Hz	2GHz	Linear	128	<span style="color: red;">✖</span>

S Parameter File Name: S\_para      S Parameter Format: BNP      Extract

10. Set the *Sweeping Mode* to *Linear*, *Decade*, or *Adaptive*.

- If you select *Linear*, specify a value in the *# of Freq. Points* column. It defines the number of frequency points to be sampled within the specified frequency range. By default, it is set to 128 frequency points.
- If you select *Log*, specify a value in the *Points/Decade* column. By default, it is set to 10 frequency points per decade.
- If you are using SPDSIM as the circuit simulator, you can select *Adaptive* to use Adaptive Frequency Sweep.

11. Specify the frequency range in the *Starting Freq.* and *Ending Freq.* columns.

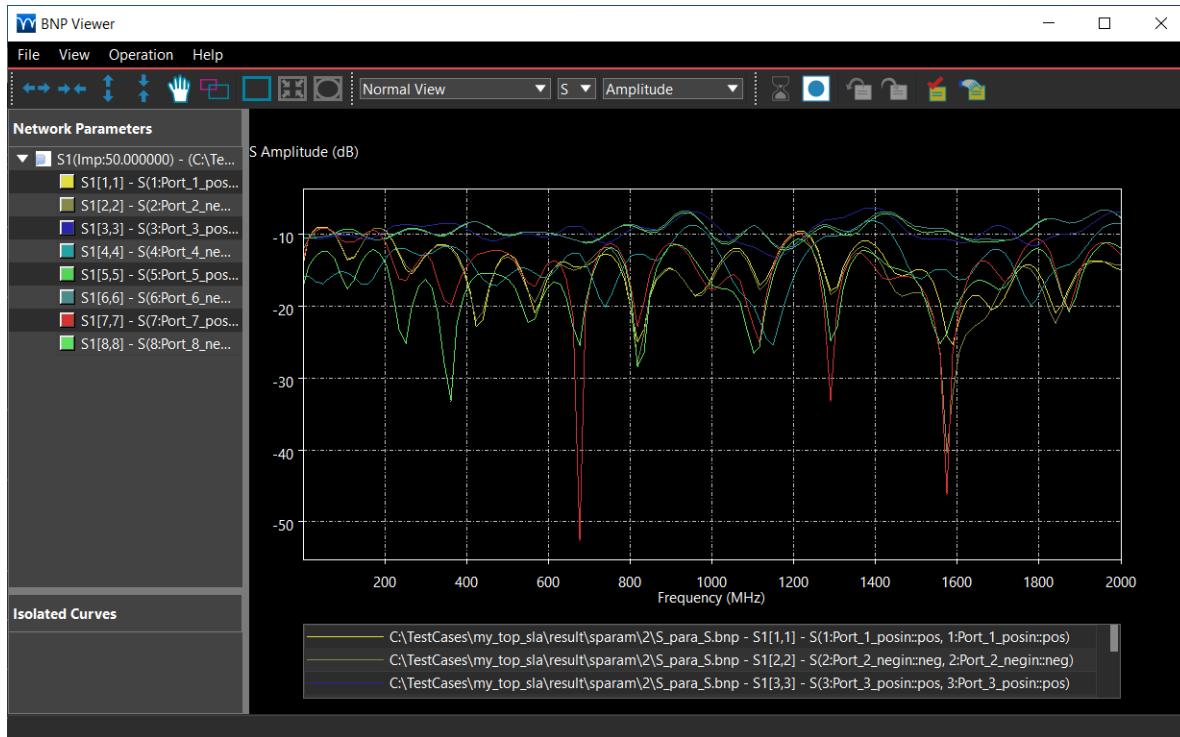
12. Specify the *S Parameter File Name*. By default, *S\_para* is specified as the output filename.

13. Select the *S Parameter Format* from the list box. If *touchstone* format is selected, files with extension *.s2p* are generated. For *BNP* format, *.bnp* files are generated.

## Topology Workbench User Guide

### Working with Topologies

14. Click *Extract* to start the S Parameter extraction process. The progress is reported in the status bar. On completion of the extraction, the results are shown in the BNP Viewer window, as shown below.



## Setting Up the Default Pin Location

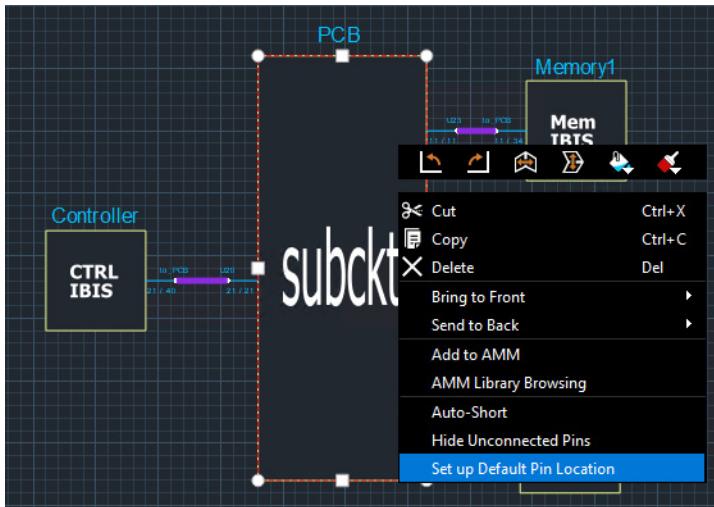
In Topology Workbench, the default location can be set for the pins associated with blocks of the following types: S Parameter, FDTD-D, Controller, Memory, Transmitter, Receiver, and Cable. The process is the same for all supported block types. Therefore, this topic explains the setting of default pins using an S Parameter block for example.

1. Select the S Parameter block in the topology.

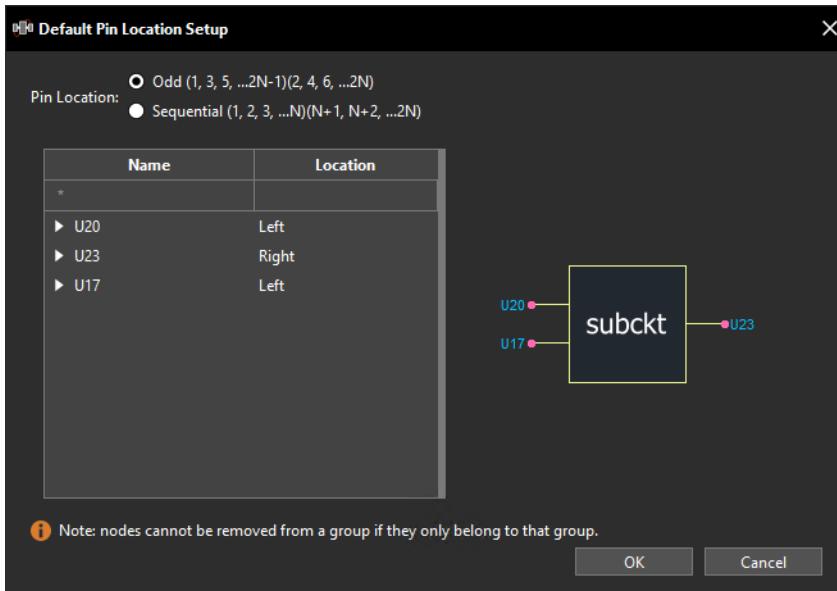
## Topology Workbench User Guide

### Working with Topologies

2. Click right to display the shortcut menu and select *Set up Default Pin Location* as shown below.



The *Default Pin Location Setup* dialog box is displayed.



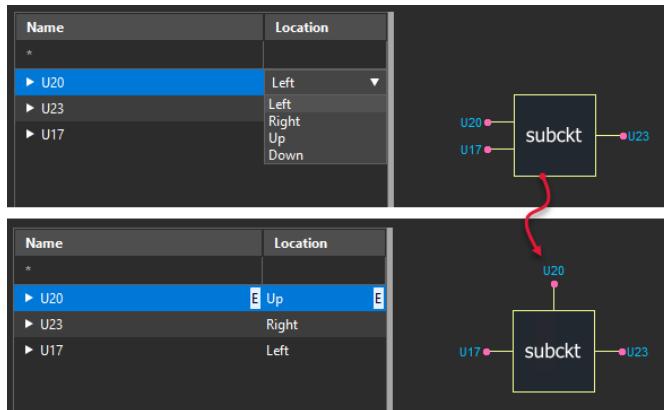
Use this dialog box to control how you want to build the symbol for the current model by renaming and/or moving pins. You can group any number of pins on either side of the block. Pins cannot be removed from a group if they belong to only that group.

3. Select the type of *Pin Location* you want to create, whether *Odd* or *Sequential*.
4. Double-click a pin name in the *Pin* column to rename it.

## Topology Workbench User Guide

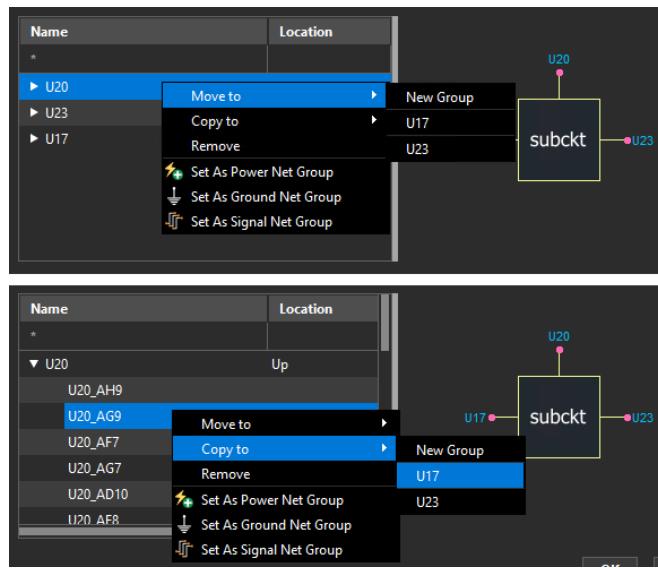
### Working with Topologies

5. Double-click the *Location* cell corresponding to the pin that needs to be moved. You have the choice to move a pin to *Left*, *Right*, *Up*, and *Down*. The pictorial representation on the right reflects the change as shown in the example below:



6. Right-click a pin name and use the shortcut menu controls as needed. You have the options to:

- Move to a New Group* or another pin
- Copy to a New Group* or another pin
- Remove*
- Set As Power Net Group*
- Set As Ground Net Group*
- Set As Signal Net Group*



**Note:** The same shortcut menu controls are also available for each pin within a power, ground, and signal net group. If the position of the pins and groups needs to changed, select them from the *Name* column and then drag and drop in the required node within the table.

7. Click *OK* to apply the changes. The updated pin locations start to reflect on the canvas.

**Note:** You cannot add or remove pins using the *Default Pin Location Setup* dialog box.

## Setting Up Probe Points

Topology Workbench lets you add current probes to the connections to observe the current that passes through the signal nets. Similarly, you can define voltage probe points to view 2D voltage plots at the end of the time-domain simulations. Voltage probe points are added to the signal nets of the specified block.

In Topology Workbench, you can define both current and voltage probes using the *Probe Points* panel that can be accessed:

- from the canvas directly
  - or-
- by the *Setup – Probe Points* menu

For detailed procedural information, refer to the [Adding Current Probes](#) and [Adding Voltage Probe](#) sections.

### Adding Current Probes

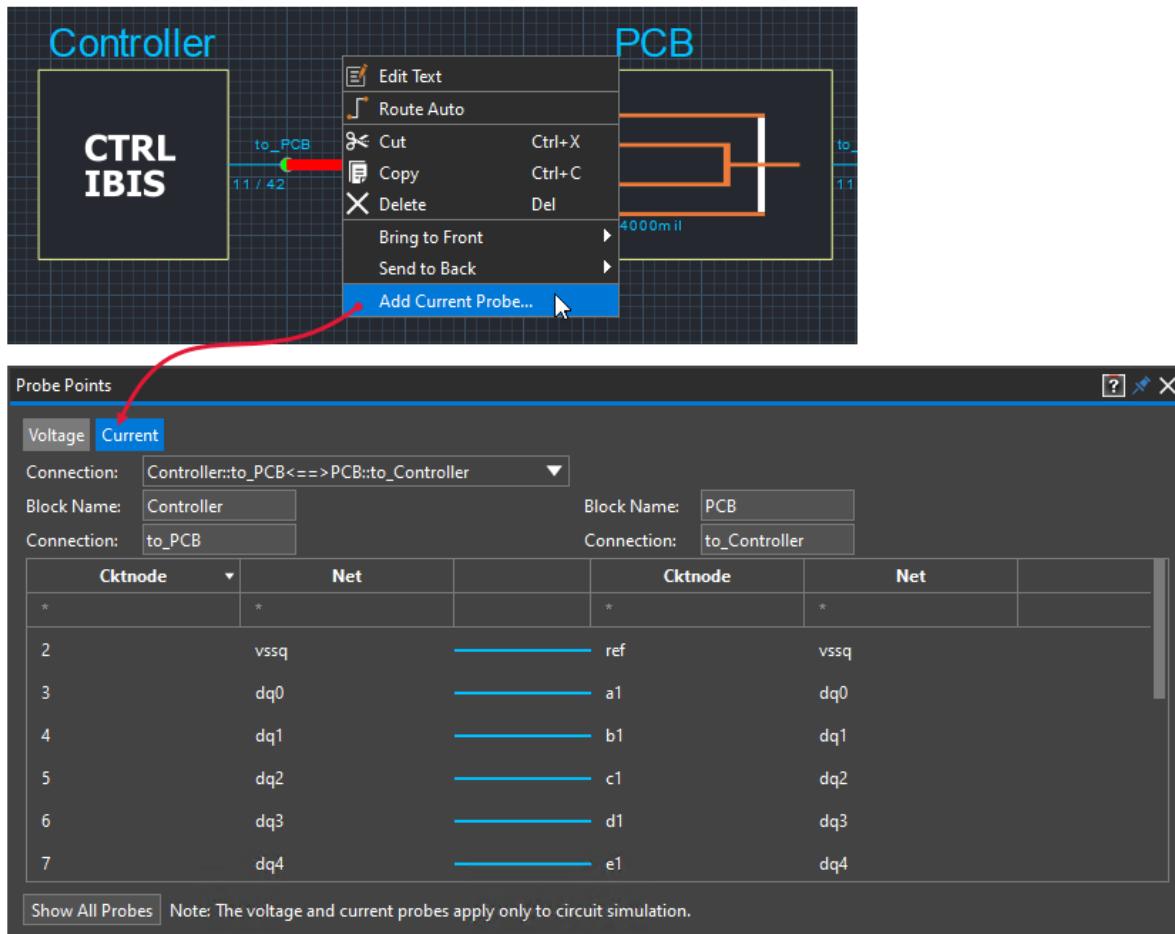
To add current probes on the selected connections:

1. Right-click a connection port of a block.

## Topology Workbench User Guide

### Working with Topologies

2. Select the *Add Current Probe* option from the displayed shortcut menu. This opens the *Probe Points* panel with the focus on the *Current* tab.



3. Choose the *Connection* from the list box.

When you access the *Probe Points* panel from the canvas by right-clicking a connection, the selected connection is selected by default. The blocks on the left and right of the chosen connection are displayed in the read only fields, *Block Name* and *Connection*.

4. Double-click the connecting line between two nets that need to be probed.

Alternatively, right-click the connecting line and select *Add Probe* from the displayed shortcut menu.

# Topology Workbench User Guide

## Working with Topologies

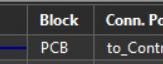
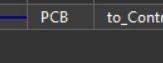
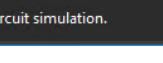
---

The  icon indicating a current probe is placed on the associated connecting line as shown below.

Cktnode	Net		Cktnode	Net
*	*		*	*
2	vssq		ref	vssq
3	dq0		a1	dq0
4	dq1		b1	dq1
5	dq2		c1	dq2
6	dq3		d1	dq3
7	dq4		e1	dq4
8	dq5		f1	dq5
9	dq6		g1	dq6
10	dq7		h1	dq7
11	dqs0p		i1	dqs0p

Show All Probes Note: The voltage and current probes apply only to circuit simulation.

- Click *Show All Probes* to view only those *Cktnode-Net* connections on which current probes have been set.

Probe Points										
Voltage		Current								
Enable	Block	Conn. Port	Ckt Node	Net		Block	Conn. Port	Ckt Node	Net	Custom Probe Name
<input checked="" type="checkbox"/>	Controller	to_PCB	8	dq5		PCB	to_Controller	f1	dq5	Controller_to_PCB_8->PCB_to_Controller_f1
<input checked="" type="checkbox"/>	Controller	to_PCB	6	dq3		PCB	to_Controller	d1	dq3	Controller_to_PCB_6->PCB_to_Controller_d1
<input checked="" type="checkbox"/>	Controller	to_PCB	3	dq0		PCB	to_Controller	a1	dq0	Controller_to_PCB_3->PCB_to_Controller_a1
<input checked="" type="checkbox"/>	Controller	to_PCB	10	dq7		PCB	to_Controller	h1	dq7	Controller_to_PCB_10->PCB_to_Controller_h1

Add Probes Note: The voltage and current probes apply only to circuit simulation.

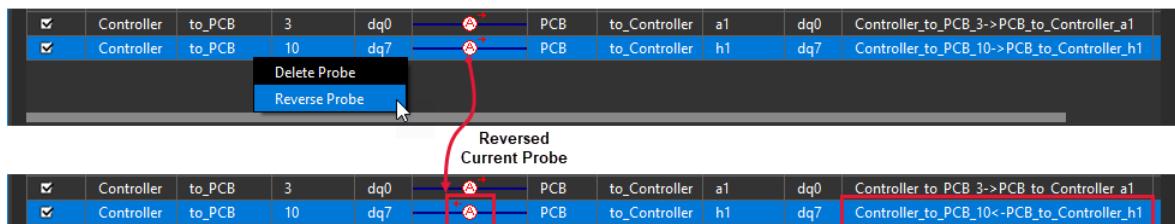
- To add more probes, click *Add Probes*. The complete list of *Cktnode-Net* connections is displayed again.
- To disable a probe, deselect the corresponding check box in the *Enable* column.
- To reverse the direction of the probe, right-click the corresponding row and select *Reverse Probe* from the displayed shortcut menu. Notice the difference in the

# Topology Workbench User Guide

## Working with Topologies

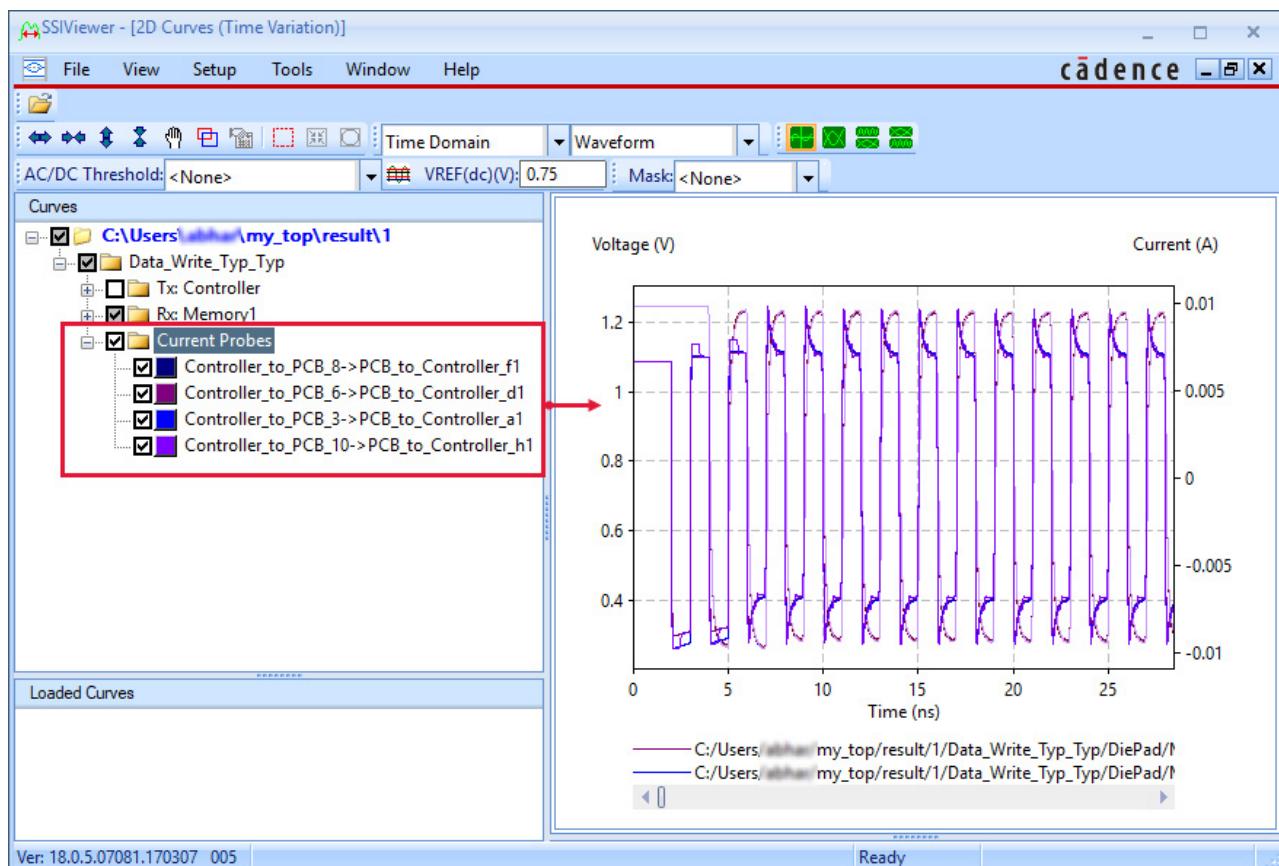
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direction of the arrow in the probe icon applied to the connecting line and the arrow used in the *Custom Probe Name* cell, as shown below.



- ❑ To delete a probe, right-click the corresponding row and select *Delete Probe* from the displayed shortcut menu.

After the simulation, the curves of all the defined *Current Probes* can be viewed in the 2D Curves tab as shown below.



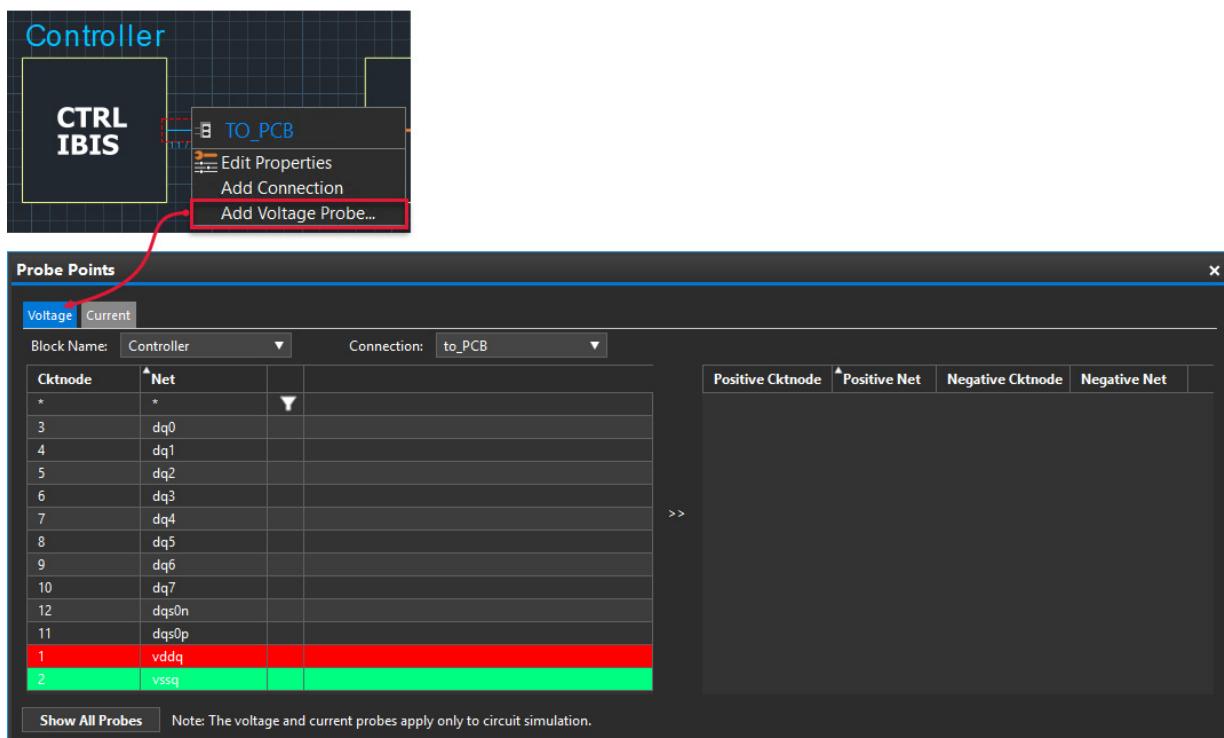
**Note:** To add current probes for a different connection, select it from the *Connection* list box in the *Current* tab of the *Probe Points* panel and repeat the steps covered in this section.

## Adding Voltage Probe

A voltage probe requires definition of a positive and a negative voltage. To add a voltage probe:

1. Right-click a pin of a block.
2. Select the *Add Voltage Probe* option from the displayed shortcut menu.

This opens the *Probe Points* panel with the focus on the *Voltage* tab. All the nodes of the selected block and the connection ports are displayed on the left and the existing voltage probes are displayed on the right.



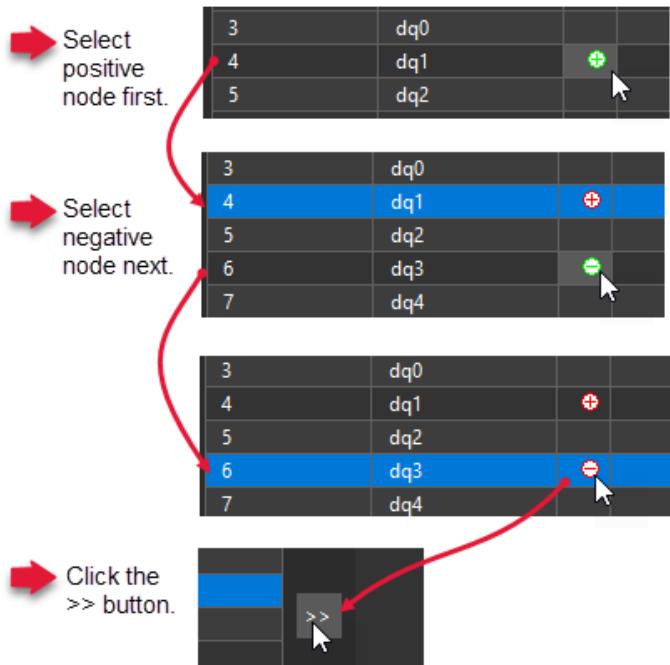
3. Choose the *Block Name* and *Connection* from the corresponding list boxes.

The values in the *Connection* list box are populated accordingly to list the blocks connected to the selected block.

## Topology Workbench User Guide

### Working with Topologies

4. Select the positive node first, and then the negative node.



5. Click the >> button while the positive and negative nodes are selected.

A screenshot of the 'Probe Points' dialog box. On the left, there's a table with columns 'Cktnode' and 'Net'. Rows include nodes 3, 4, 5, 6, 7, 8, 9, 10, 12, 11, 1, and 2, each associated with a net name like dq0, dq1, etc. Row 6 is highlighted with a blue background. On the right, there's another table with columns 'Positive Cktnode', 'Positive Net', 'Negative Cktnode', and 'Negative Net'. It contains one row with values 4, dq1, 6, and dq3. Below these tables is a '>>' button with a mouse cursor hovering over it. At the bottom left is a 'Show All Probes' button, and at the bottom center is a note: 'Note: The voltage and current probes apply only to circuit simulation.'

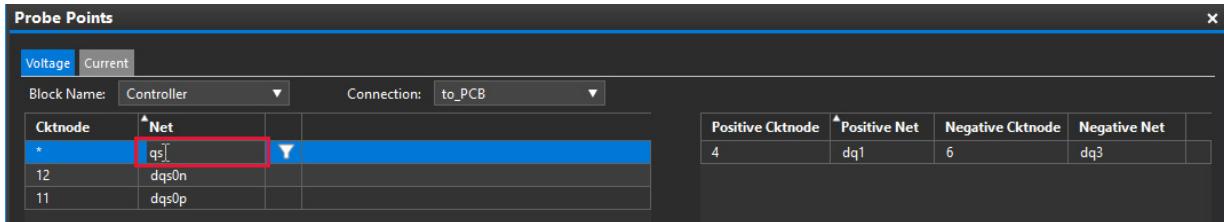
The newly added voltage probe appears in the table on the right. You can add more voltage probes by repeating steps 4 and 5 above.

The first row in the table on the left lets you filter and search for specific circuit nodes or nets. For example, when you enter *qs* in the cell with an asterisk (\*) under the *Net*

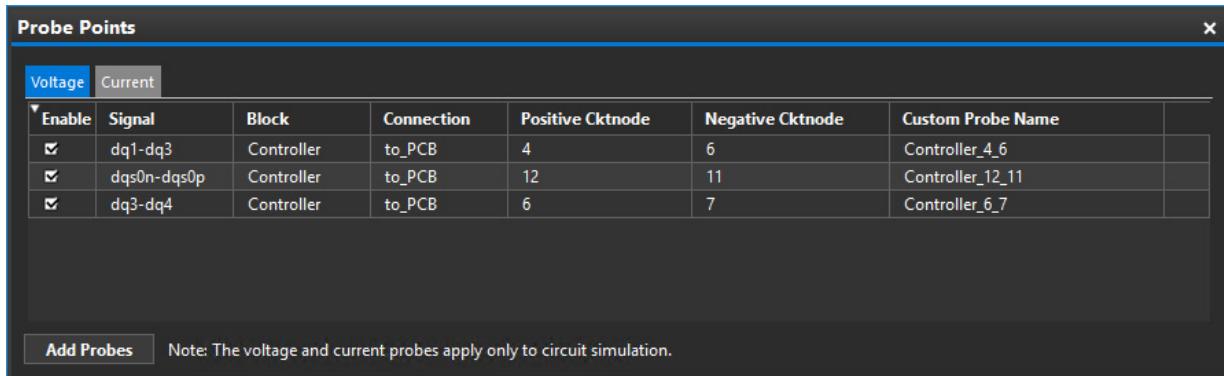
# Topology Workbench User Guide

## Working with Topologies

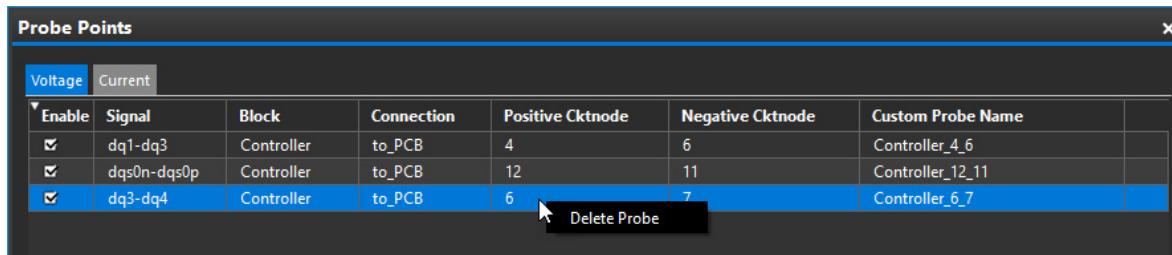
column, the nets that have *qs* in their names are filtered and displayed for you as shown below:



6. Click *Show All Probes* to display a list of all voltage probes.



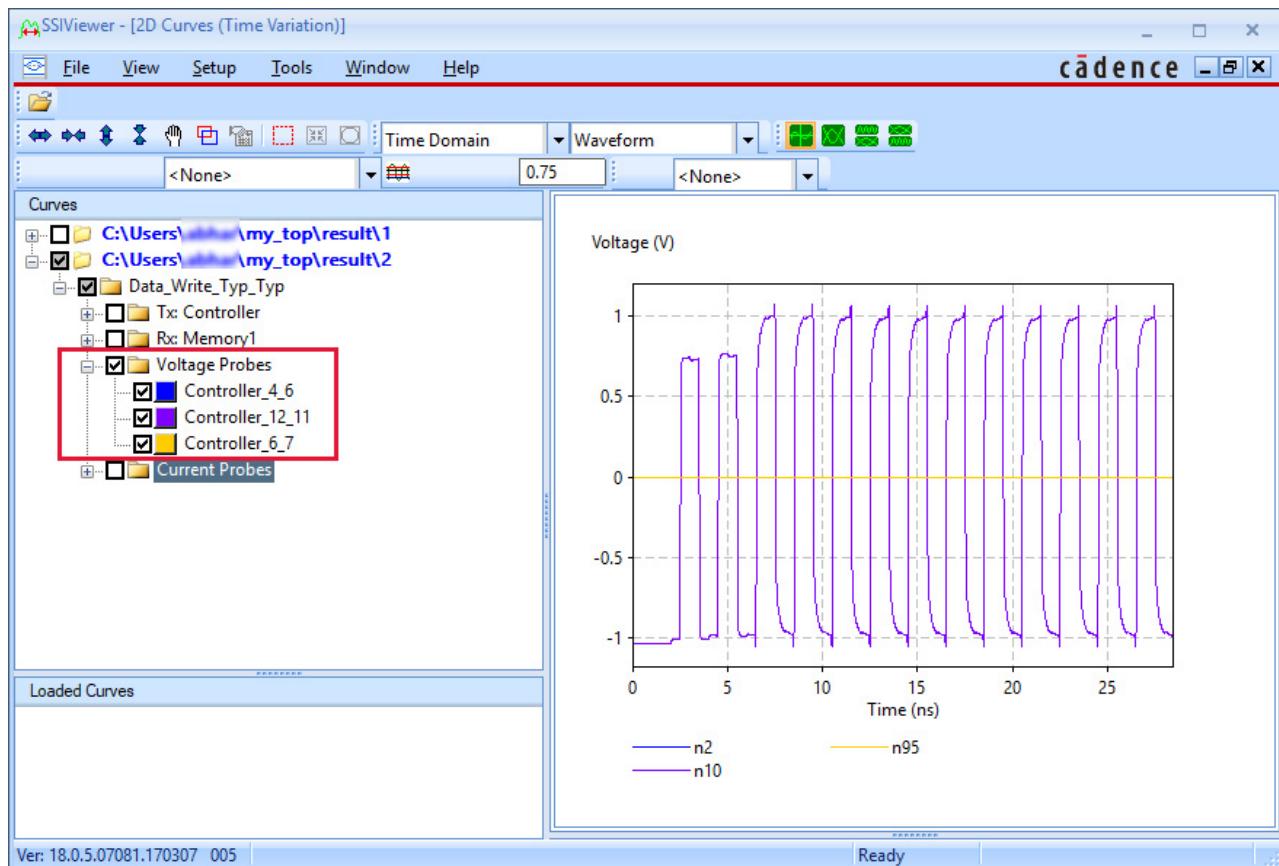
- To add more probes, click *Add Probes*. The complete list of nodes (*Cktnode* and *Net*) is displayed again.
- To disable a probe, deselect the corresponding check box in the *Enable* column.
- To delete a probe, right-click the corresponding row and select *Delete Probe* from the displayed shortcut menu.



# Topology Workbench User Guide

## Working with Topologies

After the simulation, the curves of all the defined *Voltage Probes* can be viewed in the SSIViewer (2D Curves) window as shown below.



## Defining Internal Probes

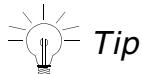
While running a Topology Workbench workflow, you have the option to define voltage and current probes within the subcircuit definition.

**Table 2-1 Syntax for Internal Voltage Probe**

Syntax	Output
.print V(node1)	Voltage at <i>node1</i> with respect to ground
.print V(node1) V(node2)	Voltage at <i>node1</i> and <i>node2</i> with respect to ground
.print V(node1 node2)	Voltage between <i>node1</i> and <i>node2</i>
.probe V(node1 node2)	Voltage between <i>node1</i> and <i>node2</i>

# Topology Workbench User Guide

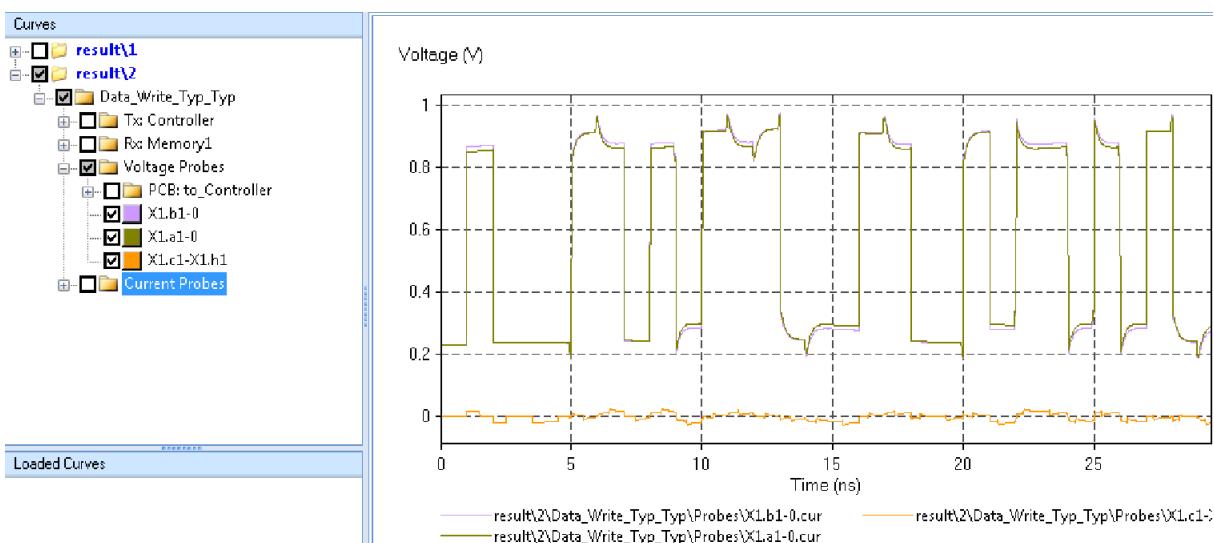
## Working with Topologies



Both the .probe and .print statements can be used to set internal probes.

For example, the curves shown in the image below are generated based on the following statements:

```
.print V(b1)
.probe V(a1)
.print V(c1 h1)
```



### Syntax for Internal Current Probe

```
.print I(device)
.probe I(device)
```

#### Example 1:

```
r_vrm2ref gnd_vrm ref 1e-6
.probe I(r_vrm2ref)
```

#### Example 2:

```
V1 node1 node2 0
.print I(V1)
```

## Setting Up Component Model

You can use Sigrity™ Analysis Model Manager (AMM) within Topology Workbench. Seamless integration of this functionality helps to avoid explicit copying of any model not originating in the default project library to the project library. With the AMM functionality, you have at hand the analysis models that explicitly have a *Timing* section to contain the required model information. You can also read and use pre-existing SystemSI – PBA IBIS models having embedded comments within Topology Workbench.

When a legacy SystemSI project is opened, an AMM project library is automatically created, any models with timing data in comments are updated to AMM format, and all models are copied to the project library.

A directory named `asi_models` is automatically added to the project directory structure where all local models used by the topology are generated, copied to, and then stored. This directory is also the default location for the AMM project libraries created for any Topology Workbench project and it is a part of the project archives. For better portability, AMM copies the IBIS models locally to the project library in the `asi_models` directory. The wrapped models in the `result` directory reference the source models in the `asi_models` directory.

With the use of AMM in IDA and the ability to extract topologies from IDA tables, any AMM model assignments in an Allegro database are passed to Topology Workbench. Existing model assignments are indicated with an *ASI\_MODEL* property on the device or instance in Allegro. In addition, an existing IDA `asi_model` directory is used as the project library for the Topology Workbench project. IDA and TopXp, when used together for topology extraction, use the same project library in the `asi_models` directory, using common models when simulating at the layout level or in the topology environment.

This section focuses on how to add new models in the project library. For more information about AMM, refer to *Model Management with AMM User Guide*.

### Related Topics

- [Adding Topology Workbench Models to AMM](#)
- [Browsing Topology Workbench Models in AMM](#)
- [Managing Libraries](#)

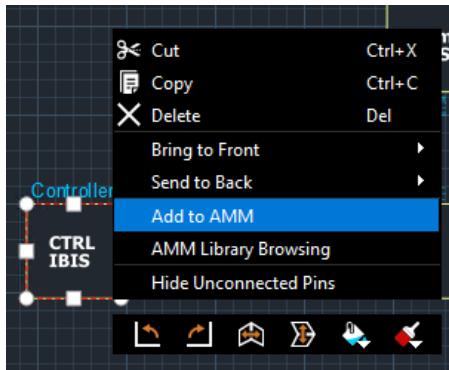
### Adding Topology Workbench Models to AMM

To add a model associated with a block to AMM:

# Topology Workbench User Guide

## Working with Topologies

1. Right-click the block on the canvas to open the shortcut menu.



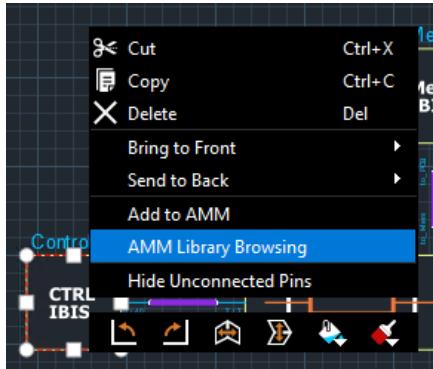
2. Select *Add to AMM*.

**Note:** Currently, this shortcut menu option is available only for the IBIS and SPICE-based blocks.

## Browsing Topology Workbench Models in AMM

To browse the model associated with a block in AMM:

1. Right-click the block on the canvas to open the shortcut menu.



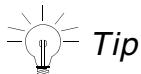
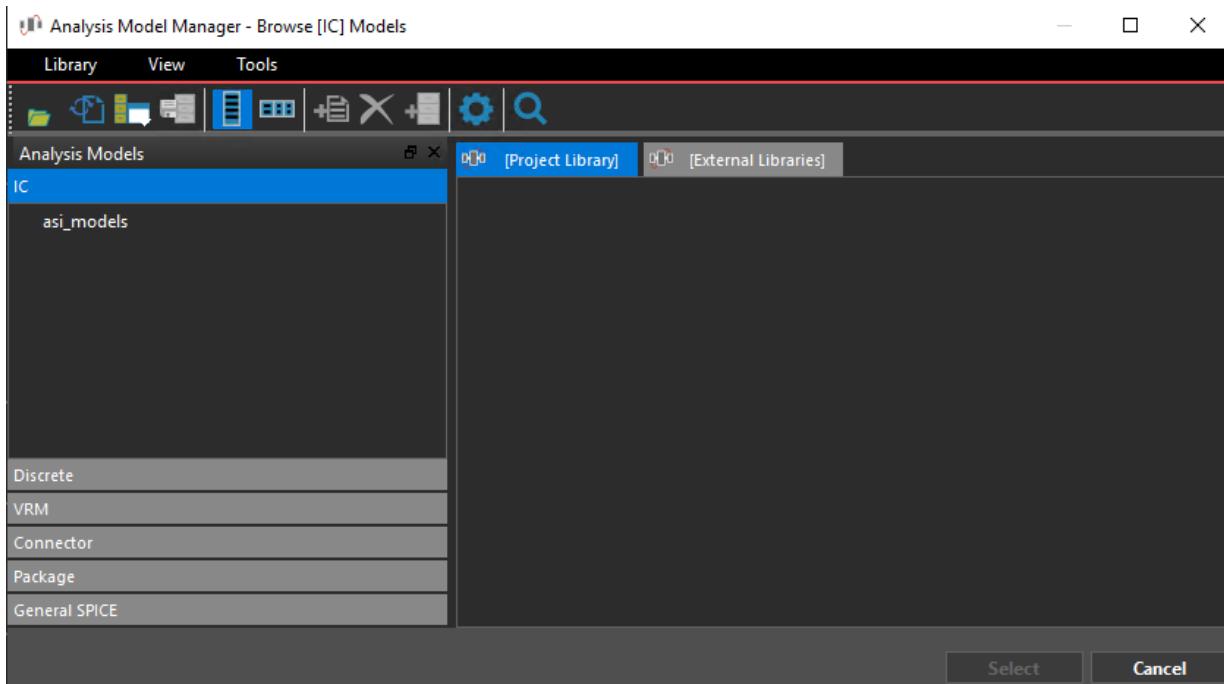
2. Select *AMM Library Browsing*.

**Note:** Currently, this shortcut menu option is available only for the IBIS and SPICE-based blocks.

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### Working with Topologies

The Analysis Model Manager - Browse [<type\_of\_model>] Models window appears as shown below. The *Analysis Models* panel in this window provides dedicated, clickable tabs for each type of model that can be added to AMM.



*Clicking Launch Analysis Model Manager from the Component Model Setup schema also opens the AMM window. Alternatively, you can click the Open Analysis Model Manager button in the AMM Library Management dialog box that is displayed when Manage Libraries is clicked from the Component Model Setup schema.*

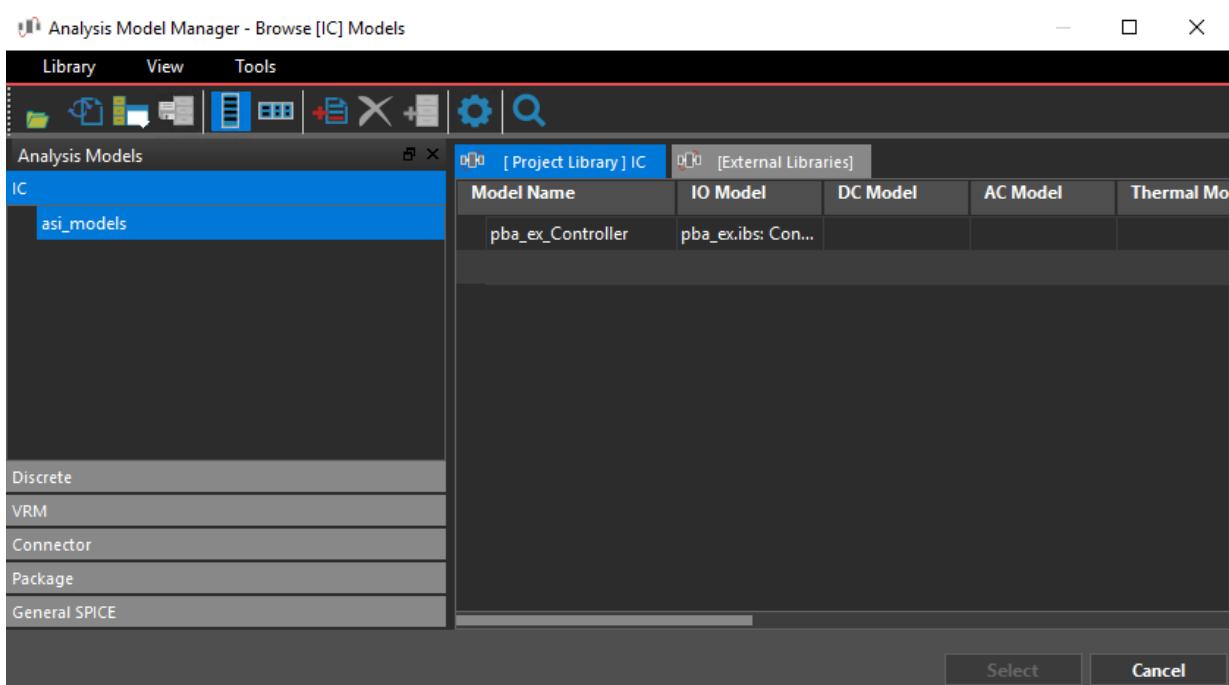
3. Click the required model category's tab in the *Analysis Models* pane. The tab expands to show the associated project library.

For example, for an IBIS-based block, click the */C* tab; for a SPICE-based block, click the *General SPICE* tab.

# Topology Workbench User Guide

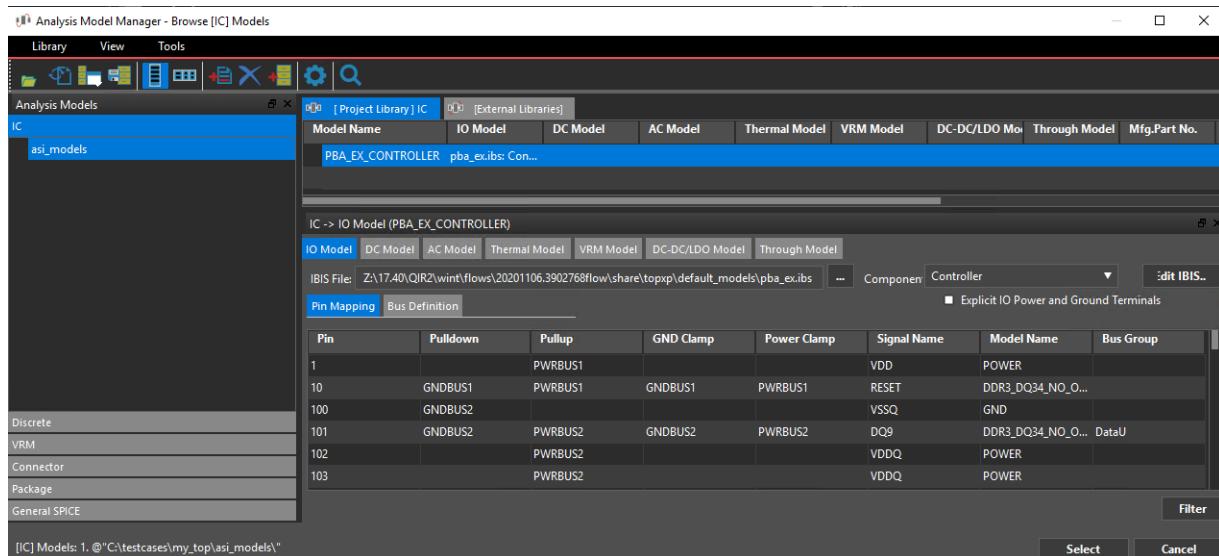
## Working with Topologies

- Click the project library. The corresponding details are displayed in the *Project Library* tab of the right pane.



- Click the model name for which details need to reviewed or updated. You can also edit the values in cells under columns such as *Model Name*, *IO Model*, *DC Model*, *AC Model*, and so on.

A pane with relevant tabs populated with detailed model information opens. A button is provided to open the associated model editor for any modifications.



6. Click *Select* to associate the selected model with the block.

## Managing Libraries

In all Topology Workbench workflows, you have the controls for managing project libraries in the *Component Model Setup* schema. To manage the project libraries, open external libraries, import a list of libraries, or opening AMM, perform the steps given below. Maintaining a model library helps you reuse data from other designs and significantly reduces the task of manually specifying new values.

### Loading a Project Library

To load a project library and some basic information of a project library:

1. Click *Manage Libraries* from the *Component Model Setup* schema. The AMM Library Management dialog box opens.
2. Click *Open Project Library* and then click *Load Library File*. The Open AMM Import Files dialog box appears.
3. Browse to select the desired library and click *Open*. You can directly load an AMM File (\*.amm), AMMX File (\*.ammx), Decap Library XML File (\*.xml), and AMM Pref File (\*.ammp).
4. Click *Open*.

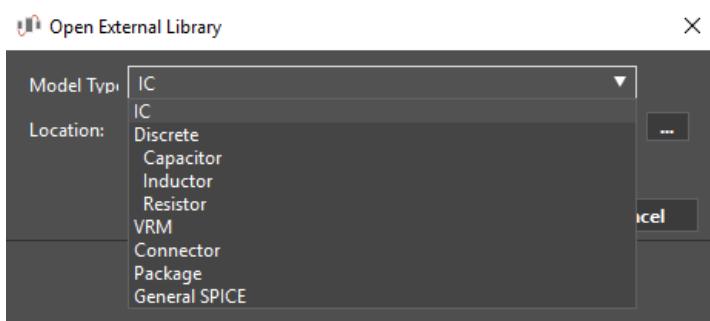
### Opening External Libraries

To open an external library and some basic information of a project library:

1. Click *Manage Libraries* from the *Component Model Setup* schema. The AMM Library Management dialog box opens.
2. Click *Open External Libraries*. A dialog box appears.



3. Select a *Model Type* from the list box.



4. Browse to the *Location* where the external library is saved and click *Select Folder*.
5. Click *OK*.

## Importing a List of Libraries

To import a list of libraries:

1. Click *Manage Libraries* from the *Component Model Setup* schema. The AMM Library Management dialog box opens.
2. Click *Import List of Libraries*. The Open Pref Files dialog box appears.
3. Browse to select the desired library of AMM Pref File (\*.ammp) format and click *Open*.

## Setting Up Distributed Computing Options

Topology Workbench utilizes the distributed computing infrastructure based on multiple machines and uses divide-and-conquer approach for analyzing large designs. You can define the resources based on your machine's setup to achieve unprecedented performance speed-up and reduce per-machine memory consumption when simulating your designs. Distributed computing is available in all SystemSI workflows of Topology Workbench.

Distributed computing allows massive parallelization and improves performance of the Sweep Manager (in Topology Explorer, SLA, and PBA workflows), multi-bus simulations (in PBA workflow), and other flows where multiple simulations can be launched independently.

**Note:** In the PBA workflow, distributed computing is applicable only to channel and sweep simulations.

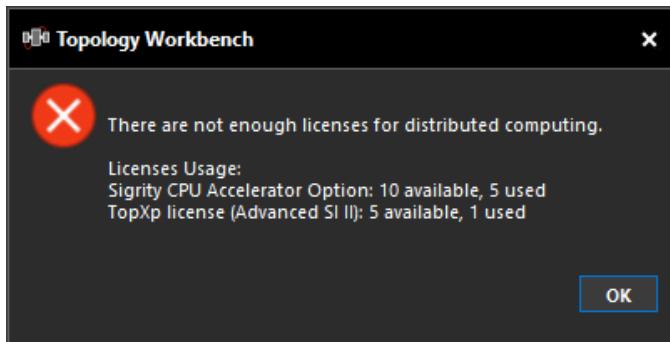
The following accelerator licenses support distributed computing in Topology Workbench and are checked out in the given order of priority:

## Topology Workbench User Guide

### Working with Topologies

- Sigiry CPU Accelerator (Product Number SIGR008) – An 8-core accelerator
- Multi-Physics Universal HPC Accelerator V8 (Product Number SYS315) – An 8-core universal accelerator
- Multi-Physics Universal HPC Token (Product Number SYS316) – A 16-core universal accelerator
- Aurora II – Allows 8 more cores (stacked)

To run distributed computing in Topology Workbench, you need enough licenses of SIGR008 and the Topology Workbench workflow that you are currently running. One SIGR008 or Topology Workbench license allows you to run simulation on 8 cores. If enough licenses are not available, a message such as following notifies you about the license status:



The scheduler can dynamically accept jobs, call various engines, and return the results to the original processes. The distributed computing flow is scalable and can use multiple computers and compute farms on Linux. For Topology Workbench, in terms of CPU/memory usage, every core needs only a maximum of 2GB, by default.

Distributed computing operation is different from SPDSIM. When distributed computing is enabled, you can run multiple simulations, such as, channel simulation after characterization or sweep. SPDSIM on the contrary is for one circuit simulation and only some part of it is distributed based on the number of cores selected.

## Enabling Distributed Computing

To run the simulation across a collection of computer systems using distributed computing:

- Select the *Enable Distributed Computing* check box in the *Distributed Computing Setup* schema.

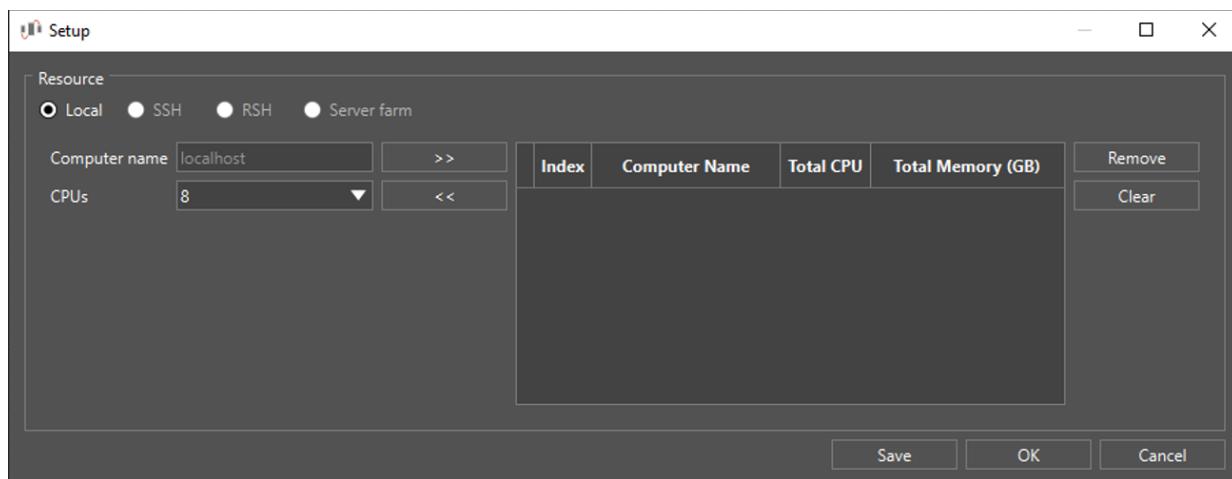
This enables the *Set up Computer Resources* option in the schema.



**To utilize the benefits of distributed computing, ensure that the latest compatible releases of Sigrity and OrCAD® and Allegro are installed. For compatibility information, see README\_CCR.txt in the OrCAD/Allegro 23.1 (SPB231) page at [downloads.cadence.com](https://downloads.cadence.com).**

## Windows Setup

1. Click the *Set up Computer Resources* icon in the *Distributed Computing Setup* schema. The *Setup* dialog box opens.



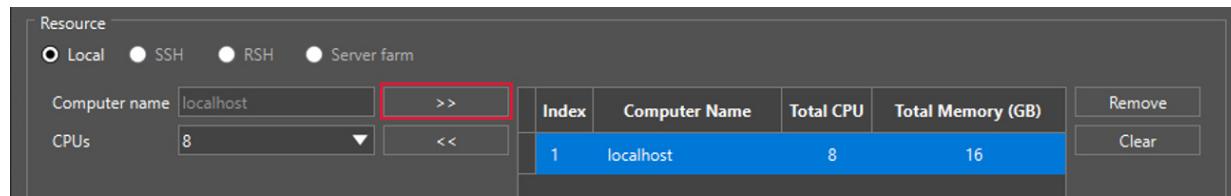
2. Specify the resource name in the *Computer name* field.

**Note:** If you are performing simulation on the local host, the *Computer name* field is not editable. It specifies the host name as the machine name.

3. Specify the number of CPUs available in the *CPU* field.

You can use the up and down arrow controls to increase or decrease the number. Topology Workbench automatically identifies the maximum number of CPUs available on the local host. You are not allowed to specify a number larger than the available CPUs.

4. Click the right arrow button to add the information to the table in the window.



5. Click *Save* and then, click *OK*.

**Note:** To run the simulation on a single computer on the Windows platform, you need to have a Hyper-V virtual machine. For more information on how to create and use a Hyper-V virtual machine, refer to the *Using Hyper-V Virtual Machine* chapter in *Cadence Sigrity 2019 Release Installation Guide*.

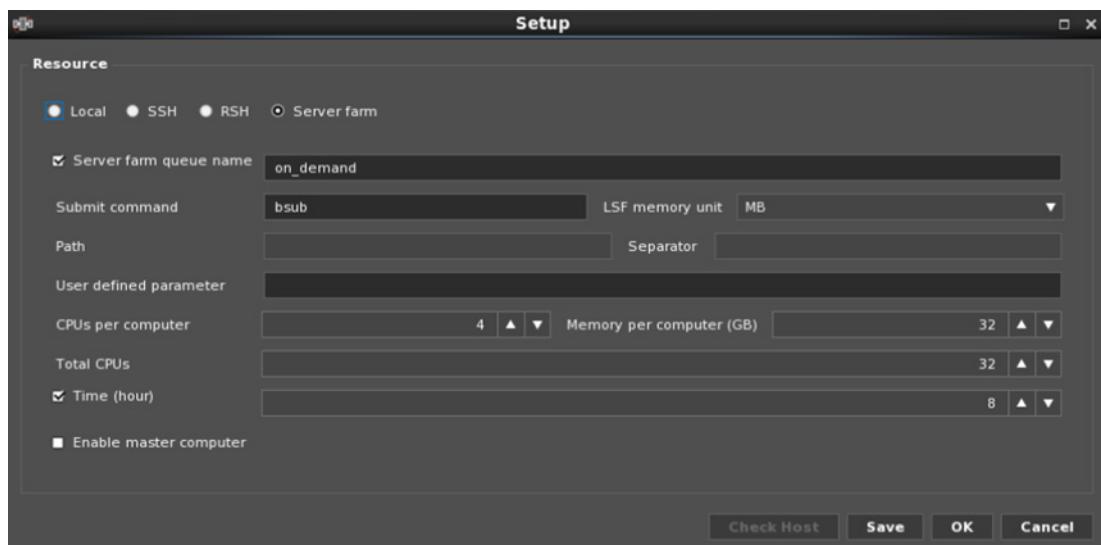
## Linux Setup

On the Linux platform, apart from the *RSH* and *SSH*, which are configured the same way as a *Local* host on Windows, you can select the *Server farm* resource types.

**Note:** The operating system of the server farm should be RHEL7.x, RHEL8.x, SUSE15, or SUSE12.

To set the server farm resource on Linux:

1. Click the *Set up Computer Resources* icon in the *Distributed Computing Setup* schema. The *Setup* dialog box opens.



2. Select *Server farm* as the resource type.
3. Specify the *Server farm queue name*.  
**Note:** Check with your IT department for the queue name of the server farm.
4. Enter the command to be used to submit the job in the *Submit command* field. For example, `bsub`.
5. Specify the *LSF memory unit*. By default, *MB* is selected.

6. Specify the script name with complete path in the *Path* field, if a script is used instead of the `bsub` command.
7. Specify the separator to be used for the script in the *Separator* field. Separator can be empty or a character can be specified depending on the server farm setting.
8. Specify the *User defined parameter* for server selection. For example, `-R 'select [OSNAME==Linux && (OSREL==EE60) ]`.
9. Specify the number of CPU cores for each process in the *CPU per computer* field.
10. Specify the memory (in GB) to be used for each process in the *Memory per computer* field. The memory required per computer is calculated automatically.
11. Specify the *Total CPUs*. The total CPU required per computer is calculated automatically.
12. Specify the time to wait for the process to complete in the *Time (hour)* field. If the simulation takes more than the specified time, the job is killed automatically.
13. Click *Save* and then, click *OK*.

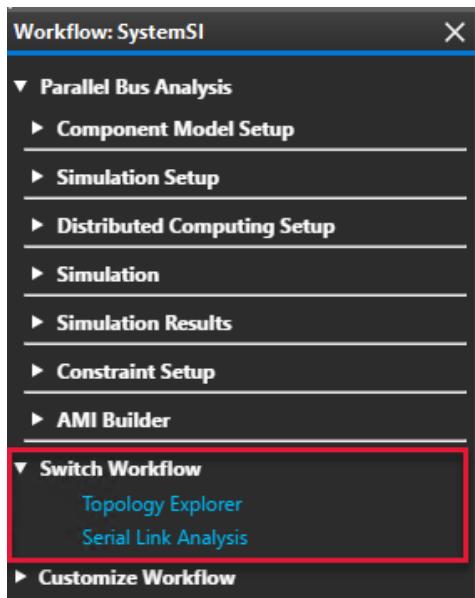
## Switching to Another Workflow

While performing an analysis on a topology, if you want to change to a different type of analysis, you can switch the workflow. The compatible workflow options are displayed in the *Switch Workflow* schema of the *Workflow* panel.

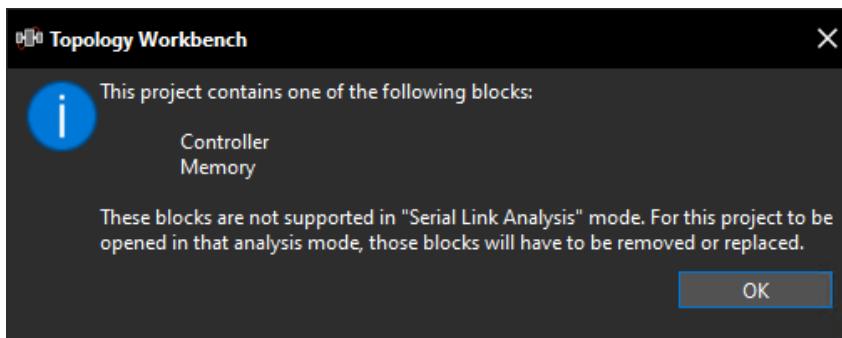
## Topology Workbench User Guide

### Working with Topologies

For example, in the *Parallel Bus Analysis* workflow, you have the options to switch to *Topology Explorer* and *Serial Link Analysis*, as shown below:



If the project contains blocks that are supported in the workflow selected for switching, the analysis options given in the *Workflow* panel change accordingly. When unsupported blocks exist in the project, an error message indicating that the issue is displayed, as shown below:



If licensing restrictions do not allow switching from one workflow to another, the *Cadence Product Choices* dialog box is displayed to select an appropriate license. For example, assume that you started Topology Workbench using the *Topology Explorer* license to perform Topology Explorer transient analysis. When you choose to switch to the Parallel Bus Analysis or Serial Link Analysis workflow, the *Cadence Product Choices* dialog box is displayed to select *Advanced SI* or *Advanced IBIS Modeling* from the list of products.

## Customizing a Workflow

Topology Workbench lets you perform the following customizations in the workflow panel:

- [Create a New Schema](#)
- [Add a New Workflow Item to a Schema](#)
- [Disable a Workflow Item](#)
- [Delete a Workflow Item](#)
- [Reset Customized Workflow Panel to Default](#)

### Create a New Schema

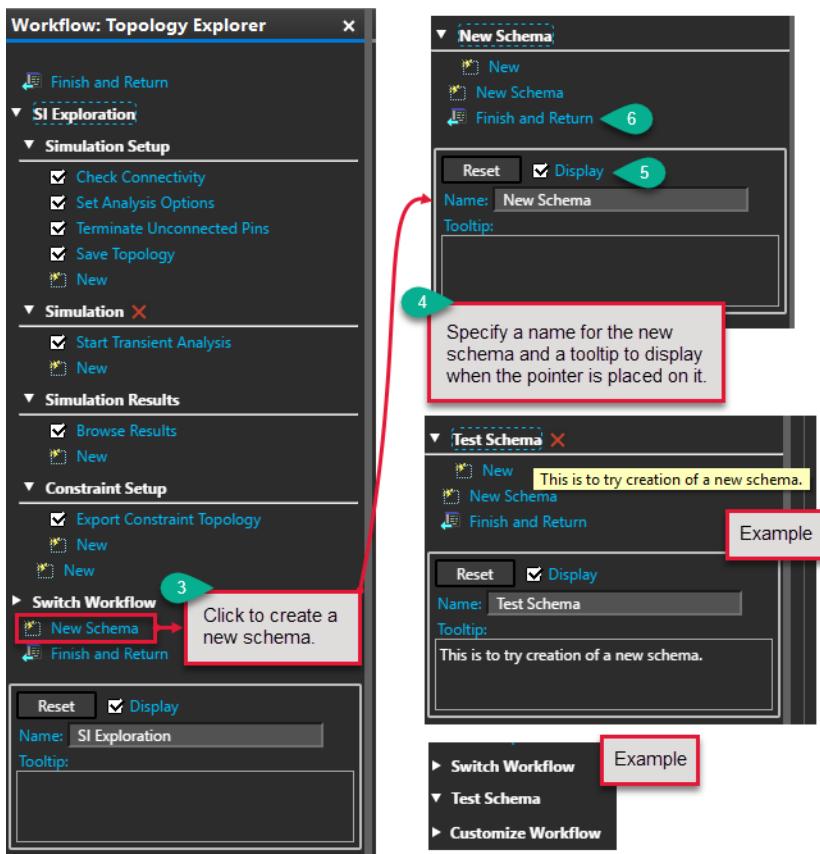
To create a new schema at the same level as the default schema such as *Simulation Setup*, *Simulation*, or *Simulation Results*:

1. Click *Customize Workflow* in the *Workflow* panel.
2. Click *Edit Current Workflow*.

# Topology Workbench User Guide

## Working with Topologies

### 3. Click *New Schema*.



4. Specify a *Name* for the new schema and a *Tooltip* that briefly describes its purpose. The tooltip is displayed when the pointer is placed on the schema's name.
5. Select the *Display* check box to ensure that after its creation, the newly created schema is displayed in the *Workflow* panel.
6. Click *Finish and Return* to save the new schema.

**Note:** Alternatively, before clicking *Finish and Return*, you can continue to do more customizations in the *Workflow* panel, such as:

- [Create a New Schema](#)
- [Add a New Step](#)
- [Add a New Group](#)

### Add a New Workflow Item to a Schema

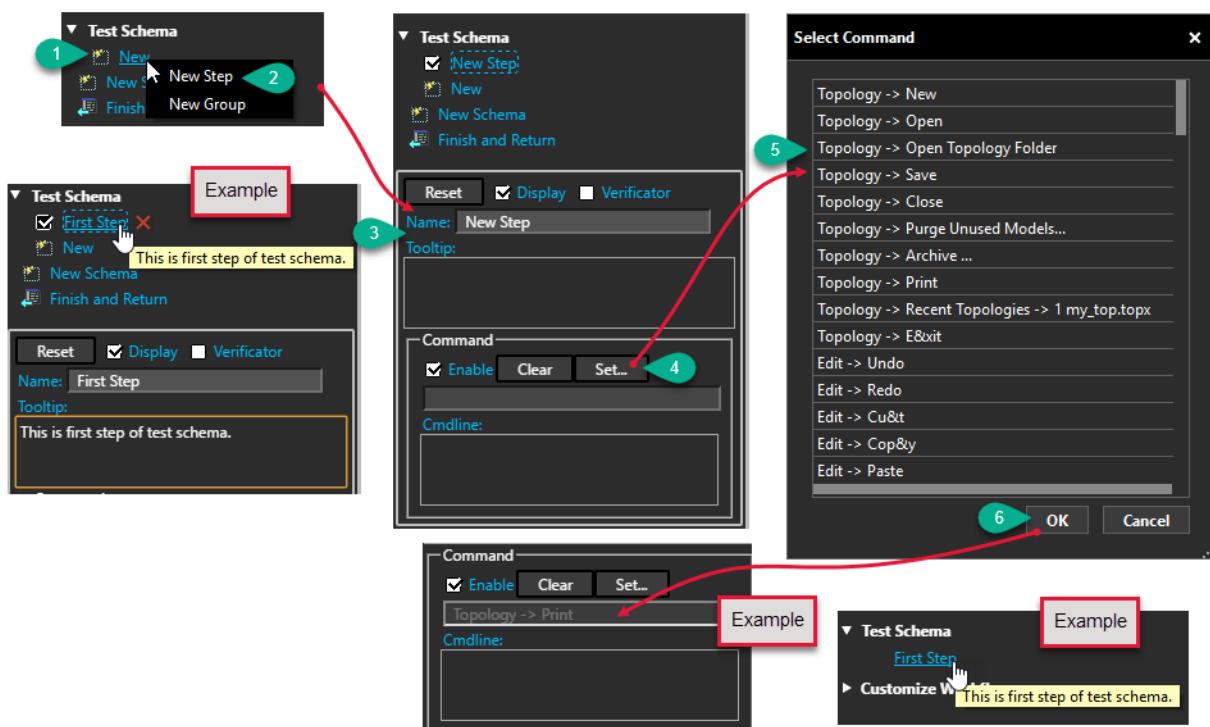
You can add the following items to a schema in the *Workflow* panel:

- [Add a New Step](#)
- [Add a New Group](#)

#### Add a New Step

To add a step to a schema:

1. Click *New* displayed below a schema.
2. Click *New Step* from the displayed shortcut menu. An item with default name, *New Step*, is added to the schema with a check box placed adjacent to it. In addition, a section appears to customize the new step.



3. Specify a *Name* for the new step and a *Tooltip* that briefly describes its purpose. The tooltip is displayed when the pointer is placed on the step's name. Ensure that the *Display* check box is selected to display the newly created step under the associated schema.

4. Click *Set* to specify a *Command* to associate with the new step. Ensure that the *Enable* check box is selected. The *Select Command* dialog box is displayed with a list of existing default preset commands of Topology Workbench.
5. Select the required command from the *Select Command* dialog box.
6. Click *OK* to associate the selected command with the new step. The *Select Command* dialog box closes and the read only text box in the *Command* section is updated accordingly.

**Note:** To disassociate a defined command from the task, click *Clear*.

7. Click *Finish and Return* to save the new step.

For example, if you set the function of the new step to be an alternative of the *Topology – Print* menu command, clicking the new step (after it is saved) will open the *Print* dialog box with a print preview of the topology and other print settings.

**Note:** Alternatively, before clicking *Finish and Return*, you can continue to do more customizations in the *Workflow* panel, such as:

- [Create a New Schema](#)
- [Add a New Step](#)
- [Add a New Group](#)

## Add a New Group

To add a group to a schema:

1. Click *New* displayed below a schema.
2. Click *New Group* from the displayed shortcut menu. An item with default name, *New Group*, is added to the schema. In addition, a section appears to customize the new group.
3. Specify a *Name* for the new group and a *Tooltip* that briefly describes its purpose. The tooltip is displayed when the pointer is placed on the group's name.
4. Select the *Display* check box to ensure that after its creation, the newly created group is displayed below the associated schema in the *Workflow* panel.
5. Click *Finish and Return* to save the new group.

**Note:** Alternatively, before clicking *Finish and Return*, you can continue to do more customizations in the *Workflow* panel, such as:

- [Create a New Schema](#)
- [Add a New Step](#)
- [Add a New Group](#)

## Disable a Workflow Item

To disable a workflow item:

1. Click *Customize Workflow* in the *Workflow* panel.
2. Click *Edit Current Workflow*.
3. Deselect the check boxes against the workflow items that need to be disabled.
4. Click *Finish and Return*. The updated *Workflow* panel is loaded without the workflow items that were disabled.

**Note:** The disabled workflow items continue to be displayed in *Edit Current Workflow* mode. You can select the check box adjacent to such workflows to enable them later as per the requirement.

## Delete a Workflow Item

To delete a workflow item:

1. Click *Customize Workflow* in the *Workflow* panel.
2. Click *Edit Current Workflow*.
3. Place the pointer on the schema, group, or step that needs to be deleted. A cross button is displayed on its right.
4. Click the cross button to delete the corresponding schema, group, or step.
5. Click *Finish and Return*. The updated *Workflow* panel is loaded without the workflow items that were deleted.

**Note:** When a schema or group is deleted, the associated steps are deleted too. The deleted workflow items are removed completely from *Edit Current Workflow* mode.

## Reset Customized Workflow Panel to Default

To restore the view of the *Workflow* panel to display the original items and remove all customizations made to it:

1. Click *Customize Workflow*.
2. Click *Reset to Default Workflow*.

## Creating Custom Templates

Advanced users can create and edit their own templates to utilize as a starting point for Topology Workbench projects. To do this:

1. Create a self-contained Topology Workbench project with all required models and connectivity.
2. Save this project in a directory, say, `my_new_template`.
3. Save the Topology Workbench project within the directory created in step 2. Ensure that the Topology Workbench project has the same name as the directory in which you are saving it. For example, `my_new_template.topx`.
4. Remove any extraneous data, for example, result and history folders, from the project and place the directory at the same location as that of default templates, that is,  
`<INSTALL_DIR>\share\topxp\<Explorer | SerialLink | ParallelBus>`.

The new template will appear when Topology Workbench is started next.

## Archiving a Topology

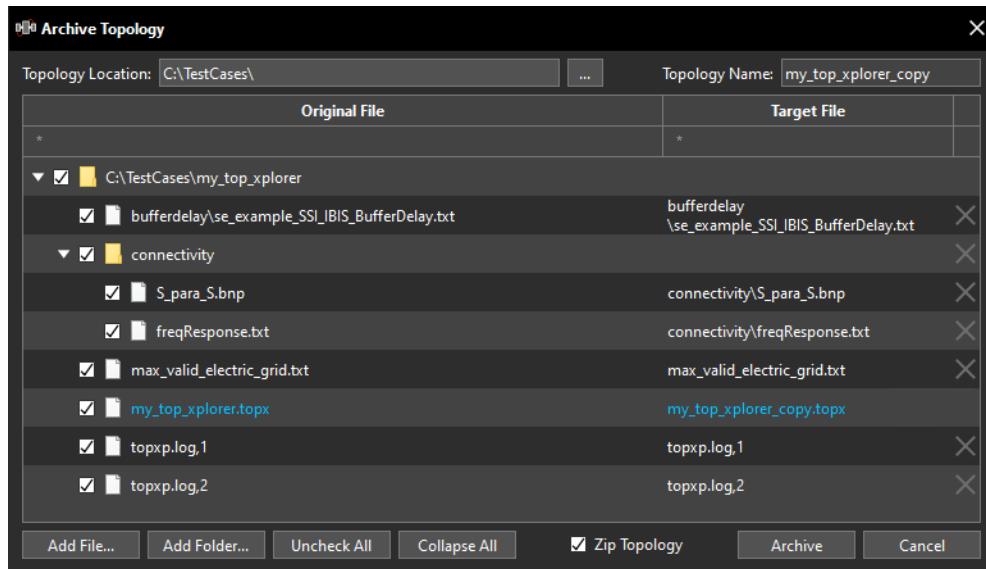
In Topology Workbench, you have the option to archive all default project files for a topology or only a specific set of related project files. To archive:

1. Save the topology.
2. Click *Topology – Archive* in the menu bar. The Archive Topology dialog box opens with files organized by their folders in a tree view. A button is provided adjacent to each folder to expand or collapse the tree node. The row below the header lets you filter the contents

# Topology Workbench User Guide

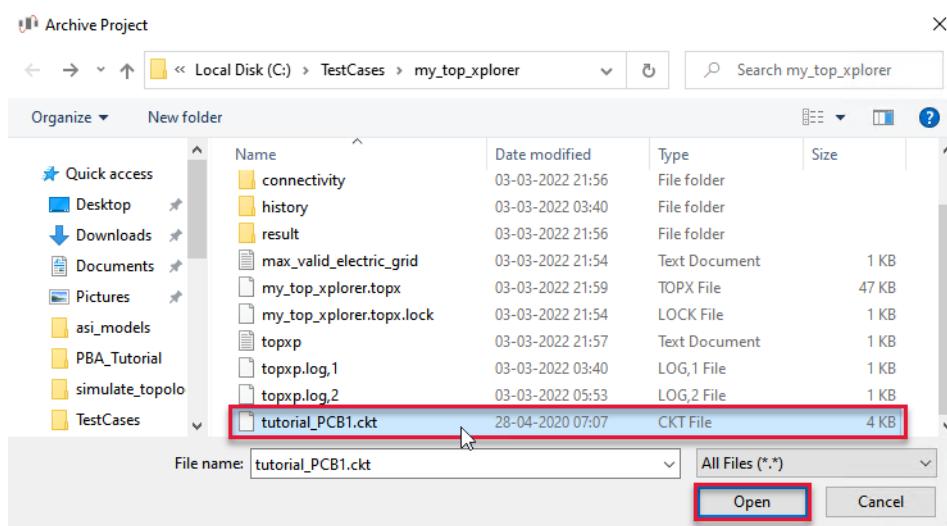
## Working with Topologies

of the tree by file path. Buttons, checkboxes, and tree-list speed up the actions and make the access smooth.



**Note:** Alternatively, you can run the `archiveProject` Tcl command.

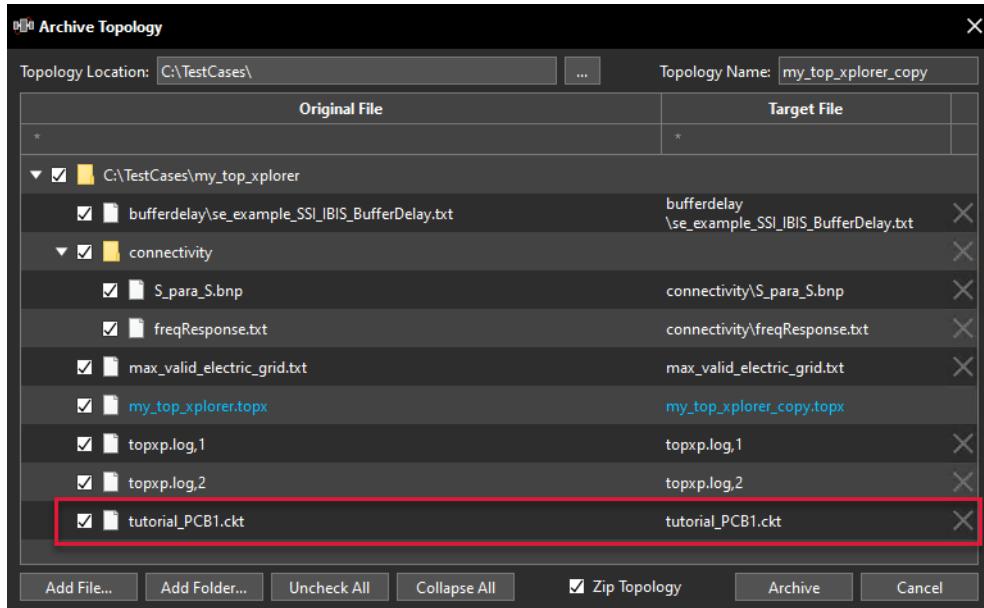
3. Browse and specify the *Topology Location*. By default, it is set to the current working directory.
4. Specify a *Topology Name*. The name given by default is of the format, `<current_topology_name>_copy`.
5. Click *Add File*.The Archive Project dialog box opens.



## Topology Workbench User Guide

### Working with Topologies

6. Browse and select the file you want to add to the archive file.
7. Click *Open*.



Similarly, you can use the *Add Folder* button for including a directory containing required files.

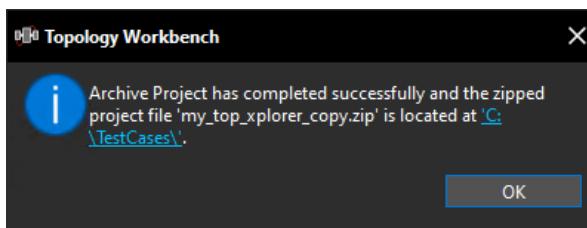
If any file or folder needs to be deleted, the cross in the last column of the corresponding row can be clicked.

By default, all items listed in the table are added to the archived project. For selective inclusion, you can click *Uncheck All* and then select the check boxes adjacent to only the required items.

The *Collapse All* button helps to collapse the tree view in a single click.

In addition, the *Zip Topology* check box is selected by default to create a zipped file of the archived project.

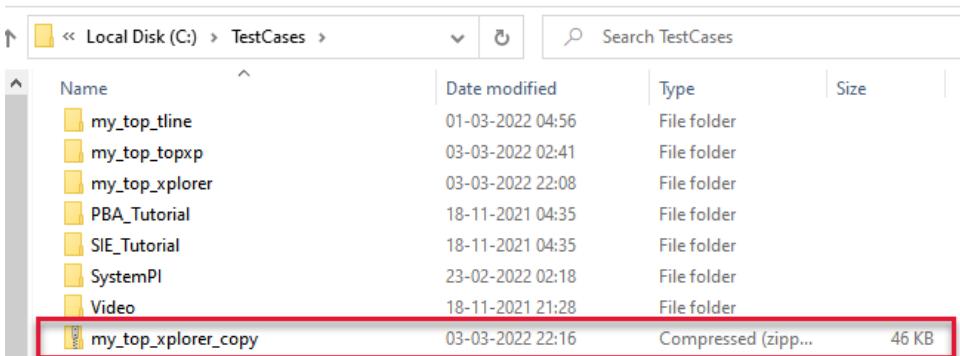
8. Click *Archive*. On completion of the process, a message box such as shown below is displayed.



## Topology Workbench User Guide

### Working with Topologies

The message box provides a hyperlink to the directory where the archived project is saved. Clicking this hyperlink opens the file browser for you.



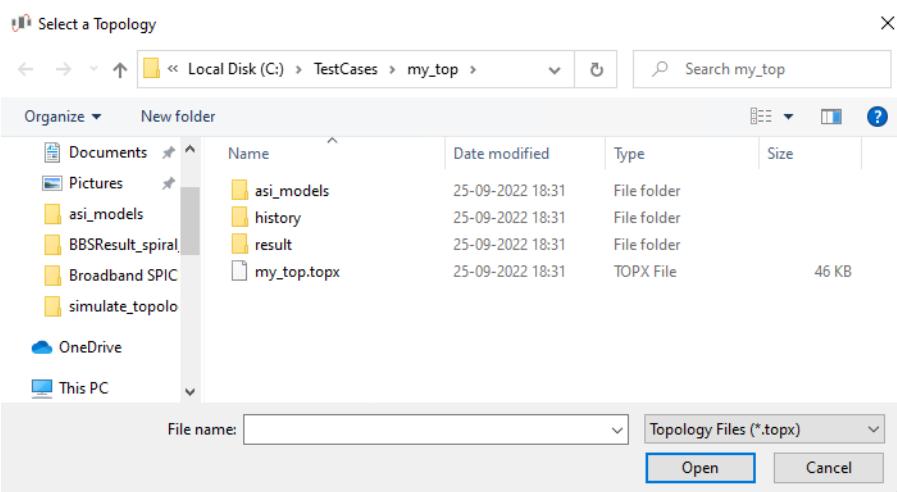
9. Click *OK* to close the message box.

## Appending to a Topology

You can append an existing .topx file or a legacy .top or .ssix file into the currently open .topx file.

To append:

1. Save the topology that is currently open in the Topology Workbench window.
2. Click *Topology – Append* in the menu bar. The Select a Topology dialog box opens.



3. Browse and select the file you want to append to the existing file. The topology refreshes and elements from the appended file can be seen.

## **Topology Workbench User Guide**

### Working with Topologies

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**Note:** Alternatively, you can run the [appendTopology](#) Tcl command in the Command Window panel.

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# Preparing for a Simulation Run

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Once a valid topology has been laid out on the canvas, you are ready to simulate it. You can use default simulation parameters to control how the simulation performs, or you can modify the simulation parameters before you start the simulation. This chapter discusses the various nuances to be considered while setting up parameters to run simulation in the Topology Explorer, SystemPI, Serial Link Analysis (SLA), and Parallel Bus Analysis (PBA) workflows.

## ***Related Topics***

- [Setting Up Simulation Options – Introduction](#)
  - [Configuring Simulation Options for Topology Explorer](#)
  - [Configuring Simulation Options for Serial Link Analysis](#)
  - [Configuring Simulation Options for Parallel Bus Analysis](#)
  - [Configuring Simulation Options for SystemPI Workflows](#)
- [Modifying Stimulus Pattern](#)
- [Calculating Write Leveling Offset \(PBA Workflow Only\)](#)
- [Setting Jitter and Noise Parameters \(Only for Channel Simulation in SLA and PBA Workflows\)](#)
- [Configuring General Simulation Options](#)
- [Checking Connectivity Between Blocks and Signals](#)
- [Terminating Unconnected Pins](#)
- [Analyzing the Frequency Response](#)

## Setting Up Simulation Options – Introduction

Before you simulate a design, basic simulation settings such as signals to be simulated, simulator to be used, simulation configuration, and simulation name can be specified in the *Analysis Options* panel. After specifying the simulation settings and running an initial simulation, you can make required changes to the design and simulation settings, and perform various experiments.

To open the *Analysis Options* panel, use one of the following methods:

- Click *Set Analysis Options* in the *Simulation Setup* schema of the [Workflow Panel](#).
- Choose *Setup – Analysis Options* from the [Menu Bar](#).

The *Analysis Options* panel is divided in workflow-specific tabs and [Restore Defaults](#).

The options displayed in the tabs of the panel vary depending on the workflow that you are using. For specific details, see the following sections below:

- [Configuring Simulation Options for Topology Explorer](#)
- [Configuring Simulation Options for Serial Link Analysis](#)
- [Configuring Simulation Options for Parallel Bus Analysis](#)

In addition, you can configure some general simulation settings, such as, setting the maximum number and percentage of CPUs to use in simulation and IBIS simulation options, viewing third-part circuit simulators, configuring message display, managing results of the previous simulations, and setting advanced characterization options for channel simulation. For more information, see [Configuring General Simulation Options](#).

### Restore Defaults

The **Restore Defaults** button on the *Analysis Options* panel can be used to restore all the changed values to their default values.

**Note:** Using the *Restore Defaults* button however, does not change the bus type selected in the [Bus Simulation](#) tab when the *Analysis Options* panel is accessed in the PBA workflow.

## Configuring Simulation Options for Topology Explorer

In the Topology Explorer workflow, to configure the simulation options in the *Analysis Options* panel:

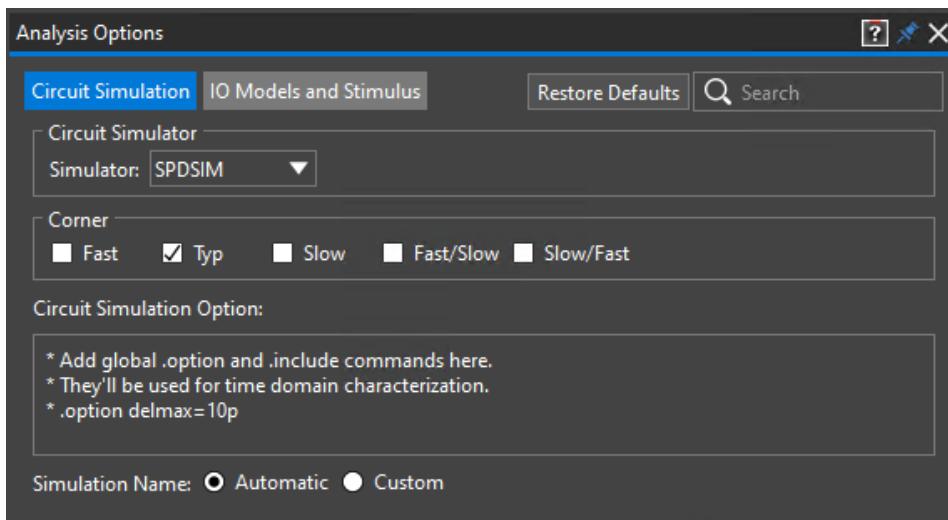
1. Specify the circuit simulator of your choice, corner settings, circuit simulations options, and simulation name in the *Circuit Simulation* tab.
2. Set the simulation parameters such as following in the *IO Models and Stimulus* tab:
  - a. Transient step time and simulation time
  - b. Signals that need to be modeled during the simulation
  - c. Stimulus pattern and offset, data rate, number of bits, and transmitter/receiver IO models

### Related Topics

- [Circuit Simulation](#)
- [IO Models and Stimulus – Topology Explorer](#)
  - [General Definition – Topology Explorer](#)
  - [Model Selection – Topology Explorer](#)
- [Restore Defaults](#)

## Circuit Simulation

The *Circuit Simulation* tab in the *Analysis Options* panel lets you specify the circuit simulator of your choice, corner settings, circuit simulations options, and simulation name option.



The *Circuit Simulation* tab has the following settings:

### ***Circuit Simulator***

Specify the circuit simulator that will be used in the simulation. The following simulators are listed in the *Simulator* list box:

**SPDSIM** Sigrity SPDSIM, a SPEEDEM simulator, is the default selection.

**Note:** When SPDSIM is used for running the simulation, the options for specifying initial DC voltages for the circuit simulator are not supported.

**Spectre** This simulator is available for use on both Windows and Linux.

To enable support on Windows, before starting Topology Workbench, set the `enable_linux_spectre` environment variable to 1. In addition, ensure that `SIGRITY_EDA_DIR` environment variable is pointing to an installation of SIGRITY 2019 HF1 or later version.

When you select *Spectre*, the *Circuit Simulation Option* box is not displayed on the *Circuit Simulation* tab, instead the user controls explained in the [Circuit Simulation Tab Settings for Spectre Simulator](#) section below are displayed.

## Topology Workbench User Guide

### Preparing for a Simulation Run

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#### **HSPICE**

This third-party simulator is visible in the *Simulator* list **only** if it is installed and the *Add HSPICE* check box is selected in the [General](#) tab of the *Options* dialog box.

When you select HSPICE, a field is displayed adjacent to the *Simulator* list. In this field, specify the path to the HSPICE simulator's executable file.

#### **Corner**

Select at least one of the following valid values to specify the *Corner* setting: *Slow*, *Fast*, *Typ*, *Fast/Slow*, and *Slow/Fast*. By default, *Typ* is selected.

The *Min/Max/Typ* IBIS IO model for the Controller, Memory, Tx, and Rx blocks is used in the simulation based on the *Slow/Fast/Typ* corner check box you selected in this section.



Multiple corners can be selected for a given simulation. In such cases, successive simulations are run, and separate results are created for each corner.

#### **Circuit Simulation Option**

Add the global `.option` and `.include` commands in this box. These commands can be used in the Time Domain characterization.

For HSPICE simulation, accurate characterization requires the `.option delmax` command to set the maximum allowable transient analysis time step size.

`.option delmax=1p`

-or-

`.option delmax=2p`

**Note:** When running a simulation using HSPICE, ensure that the `delmax` option is specified. However, the caveat is that this option increases the simulation time.

#### **Simulation Name**

Identifies how the name of the simulation results should be defined. Select one of the following two options:

##### **Automatic**

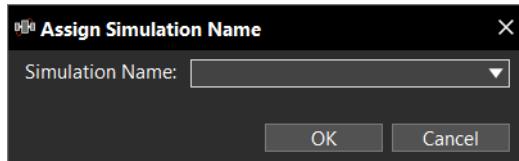
This option is selected by default. In this case, the result folder names are defined automatically according to the simulation times.

## Topology Workbench User Guide

### Preparing for a Simulation Run

#### Custom

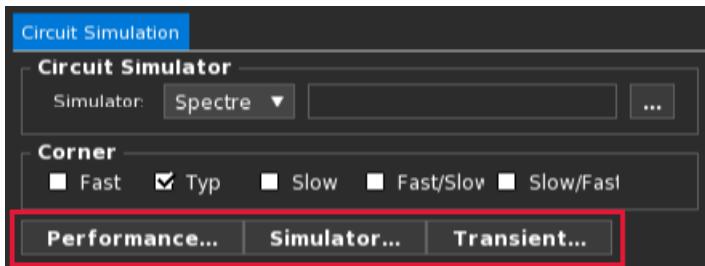
When selected, the *Assign Simulation Name* dialog box opens after you start the simulation. Enter a *Simulation Name* to identify the name of result folder before the simulation starts and click *OK*.



### Circuit Simulation Tab Settings for Spectre Simulator

#### Linux Settings

When you select the *Simulator* as *Spectre*, a field is displayed adjacent to the *Simulator* list.



In this field, specify the path to the selected simulator's executable file. Alternatively, you can set the `PATH` shell environment variable to the simulator's executable file before launching Topology Workbench, as shown below:

```
% setenv PATH /installationDir/software/Linux/spectre/bin:$PATH
```

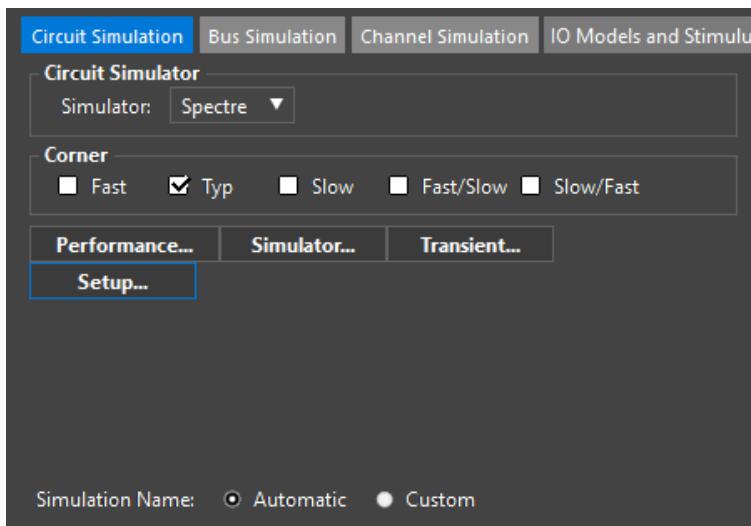
When the `PATH` shell environment variable is set, you do not need to explicitly specify the path to the simulator's executable. The field adjacent to the *Simulator* list can be left blank.

# Topology Workbench User Guide

## Preparing for a Simulation Run

### Windows Settings

In Windows, selecting the *Simulator* as *Spectre* displays the *Setup* button.



The *Setup* button opens the *Setup* dialog box, as shown below, where you need to specify the *IP Address* and *Port* of the Linux server and *Enable Remote Simulation*.



You have options to *Load Config File* and *Reconnect* to the specified remote server.

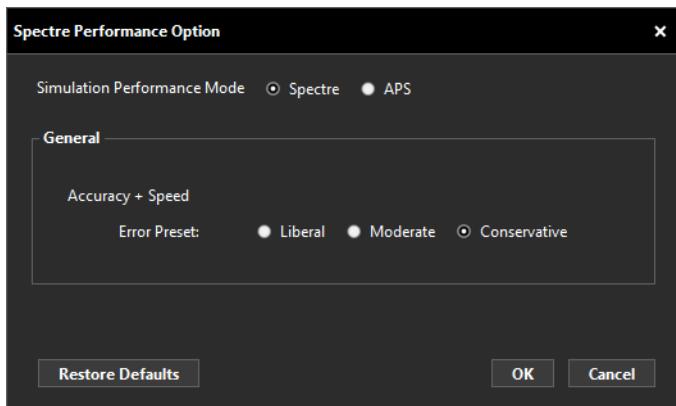
### Settings in Both Linux and Windows

The following buttons are also shown:

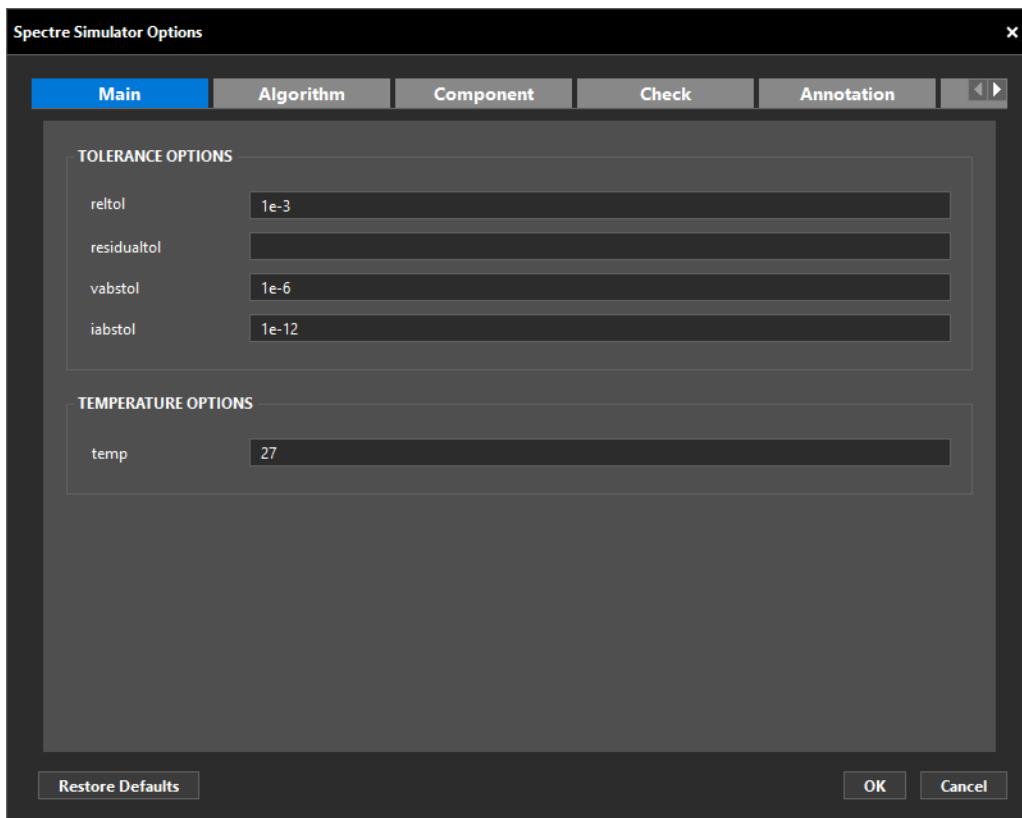
# Topology Workbench User Guide

## Preparing for a Simulation Run

- **Performance** – Opens the *Spectre Performance Options* dialog box that lets you set the simulation performance options for the Spectre simulator.



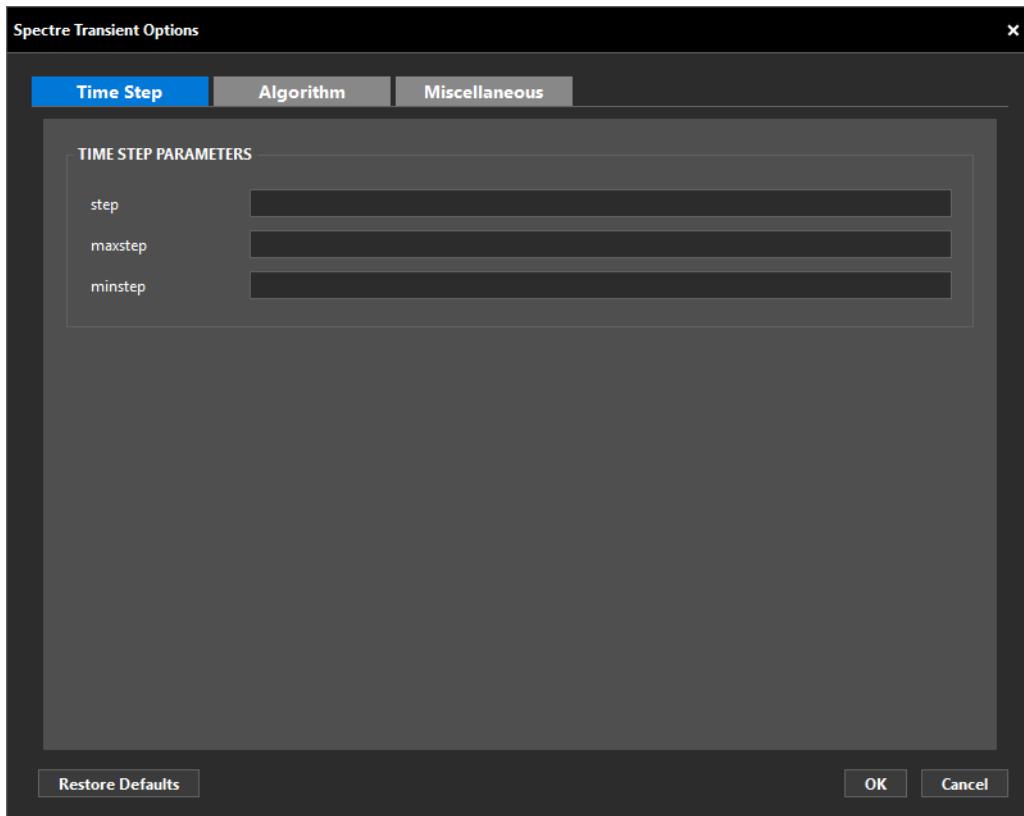
- **Simulator** – Opens the *Spectre Simulator Options* dialog box that lets you set or modify options for tolerance, temperature, convergence, matrix parameter, component, error checking, device checking, annotation, quantity, and other additional arguments. These options take effect immediately and are set while the circuit is read.



## Topology Workbench User Guide

### Preparing for a Simulation Run

- **Transient** – Opens the *Spectre Transient Option* dialog box that lets you set the parameters for time step, integration method, Newton, accuracy, and annotation.



## IO Models and Stimulus – Topology Explorer

The *IO Models and Stimulus* tab of the *Analysis Options* panel is used for source definition, including data rate, delay, and stimulus pattern. It also allows you to select IO models for Controller, Memory, Tx, and Rx blocks from the different models present in the IBIS files based on the [Model Selector] syntax.

This section is primarily divided into the following two subsections:

- [General Definition – Topology Explorer](#)
- [Model Selection – Topology Explorer](#)

### General Definition – Topology Explorer

At the top of the *IO Models and Stimulus* tab, you have the *Auto* check box selected by default. This selection ensures that Topology Workbench auto-calculates the transient step

time (*Time Step*) and simulation time (*Time Stop*) using the system-defined algorithm (see below).

To set the *Time Step* and *Time Stop* manually to a desired value, deselect *Auto*. Both the fields will be enabled.

If the *Auto* check box selected, the *Time Step* and *Time Stop* are calculated automatically based on the algorithm explained below and displayed in the read-only fields, respectively:

### ■ **Fixed Time Step Calculation**

- If the *delmax* option is specified in the *Circuit Simulation Option* section, use that value as time step.

-else-

- Check if the design has a connected Tx block. In this case, the *Time Step* is calculated as:

$$\text{TimeStep} = \text{Min}\left(\frac{1}{50 \times \text{DataRate}_{\text{signal}}}\right)$$

-else-

- Use 20p.

You can also enable time step variation algorithm using the relevant circuit simulation options. For more information, refer to the [Enabling Time Step Variation Algorithm](#) section below.

### ■ **Time Stop**

- If the design has a connected Tx block, the *Time Stop* is calculated as:

$$\text{TimeStop} = \text{Max}\left(\frac{\text{NumberOfBits}_{\text{signal}} \times 2}{\text{DataRate}_{\text{signal}}}\right) + 2 \cdot \text{Max}\left(\frac{2}{\text{DataRate}_{\text{signal}}}\right)$$

-else-

- Use 20n.

**Note:** When the *Auto* check box is selected, the *Time Step* and *Time Stop* values are recalculated if Tx, Rx, and Controller blocks are added or removed, and for any change in the *Data Rate* and number of bits.

### **Enabling Time Step Variation Algorithm**

To enable time step variation algorithm in the simulator, the following *Circuit Simulation Option* can be set in the Circuit Simulation tab of the *Analysis Options* panel:

- .option delmax=10p

This option controls circuit simulator fixed time step.

- .option auto\_timestep=1

This option enables adaptive time step. If it is set to 0, the circuit simulator uses the user-defined fixed steps. If it is set to 1 or is not set, the default step control algorithm, which uses `delmax` to calculate allowed maximum step is used.

### **Model Selection – Topology Explorer**

The *Model Selection* subsection of the *IO Models and Stimulus* tab in the *Analysis Options* panel displays tabs for each Controller, Memory, Tx and Rx block placed in the topology.

**Note:** This subsection is enabled when the block has an associated IBIS file.

The content of these tabs depend on the properties associated with the corresponding block and show related information such as signal, stimulus, and IO model definitions. The following simulation parameters can be typically set on the different tabs that are displayed:

#### **Signal Name**

Select the groups and signals to include in the simulation run. Clear the check box for the groups or signals that should not be simulated.

#### **Data Rate (Gbps)**

Specify the nominal data rate that the system will operate at.

For a transmitter (Tx) block, data rate can be defined for each signal individually or at group level. Therefore, if you have a transmitter block in the topology, the associated *Tx* tab provides the *Data Rate* column.

If you have a controller block, the *Data Rate* field is given above the table in the *Controller* tab. Based on the value specified in this text box, the *Clock Period* and *Bit Period* are calculated automatically and displayed in the respective text boxes.

### **# of Bits**

Specify the minimum number of bits to be simulated.

**Note:** This column is displayed only in the *Tx* tab, which is displayed if you have a transmitter block in the topology.

### **Stimulus Pattern**

Define a unique stimulus pattern for each data line and strobe.

To modify the default stimulus pattern of an individual signal, right-click a stimulus pattern value in the table and choose *Define Pattern* from the displayed shortcut menu. The *Stimulus Definition* dialog box appears. For more information, see [Modifying Stimulus Pattern](#).

### **Stimulus Offset**

When you set the *Stimulus Pattern*, the cells in the *Stimulus Offset* column appear as editable text fields. Enter the required stimulus offset value for the signal node or each signal line.

### **Tx IO Model and Rx IO Model**

These columns display corresponding to each signal, the IO model defined for it in the assigned model file. The cells in both these columns are non-editable.

### **Status**

This column displays the current status of the listed signal. For example, *Signal*, *Not Connected*, and so on.

## **Configuring Simulation Options for Serial Link Analysis**

In the SLA workflow, to configure the simulation options in the *Analysis Options* panel:

1. Specify the circuit simulator of your choice, corner settings, circuit simulations options, and simulation name in the *Circuit Simulation* tab.

**Note:** The settings allowed in the *Circuit Simulation* tab are the same for all workflows.

2. Specify the characterization options, the method for generating the BER eye contours (*BER\_Eyes*), and the global controls for the channel simulator in the *Channel Simulation* tab.
3. Set the simulation parameters such as following in the *IO Models and Stimulus* tab:
  - a. Ignore Time, Minimum # of Bits, Bit Sampling Rate

# Topology Workbench User Guide

## Preparing for a Simulation Run

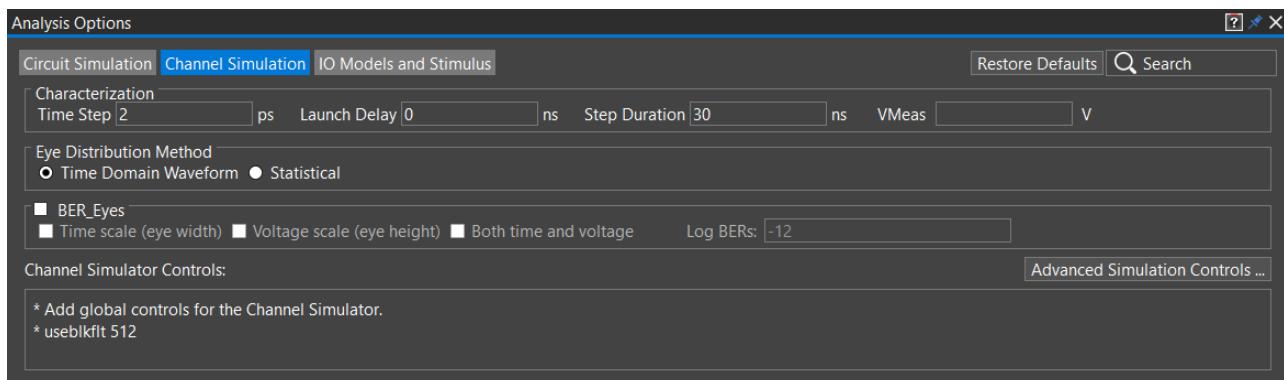
- b.** Signals that need to be modeled during the simulation
- c.** Stimulus pattern and offset, data rate, number of bits, and transmitter/receiver IO models

### Related Topics

- [Circuit Simulation](#)
- [Channel Simulation – Serial Link Analysis](#)
- [IO Models and Stimulus – Serial Link Analysis](#)
  - [General Definition – Serial Link Analysis](#)
  - [Model Selection – Serial Link Analysis](#)
- [Restore Defaults](#)

### Channel Simulation – Serial Link Analysis

The *Channel Simulation* tab lets you specify the characterization options, the method for generating the BER eye contours (*BER\_Eyes*), and the global controls for the channel simulator.



**Note:** When a channel simulator is used, you can also review the simulation correlation between the time domain circuit simulation and the channel simulation results. For this,

choose *Tools – Circuit/Channel Sim Correlation* from the menu bar. See [Correlating Circuit and Channel Simulations](#) for detailed information.

## **Characterization**

### *Launch Delay*

Specify the delay time for launching ramp-up stimulus. The impulse calculation is also shifted by the time specified in this text box.

### *Step Duration*

Specify the duration of the characterization run with the specified circuit simulator. The characterization should be run long enough to allow any reflections to settle down, and the waveforms to reach their steady state.

*VMeas*      Specify the voltage threshold at which delay is measured from the characterization. This information is included in the Channel Report as Delay. If *VMeas* value is not explicitly called out in the IBIS file associated with the Tx block, *VMeas* is taken as the midpoint of the voltage swing seen in the characterization waveform.

## **Eye Distribution Method**

### *Time Domain Waveform*

This is selected by default. Use this method if the design has an AMI model with `getwave` function, or if you want to inject Tx jitter.

### *Statistical*

Use this method to generate eye density plots, and from that derive statistical eye contours (*BER\_Eyes*).

**Note:** When you select *Statistical*, the *BER\_Eyes* section is mandatory. Therefore, the check box adjacent to the section name disappears.

## ***BER\_Eyes***

Select this check box when you want to generate *BER\_Eyes*. The following options then are enabled for selection:

- *Time scale (eye width)*
- *Voltage scale (eye height)*
- *Both time and voltage*

By default, the *BER\_Eye* generation takes into account both time and voltage scales. However, you can modify the default selection and select the *Time scale (eye width)* or *Voltage scale (eye height)* check box, or a combination of these.

**Log BERs** This is a log of the bit error ratio at which Bit Error Rate (BER) eye is generated.

When the cursor is placed in the *Log BERs* box, a tooltip with instructions about the possible values can be viewed. Use negative integers within the range of -3 to -21 to define the *Log BERs*. It is set to -12 by default.

If required, you can specify multiple values that are separated using commas. *BER\_Eye* curves are generated for each value of Log BER.

Depending on the specified *Log BERs* values and the selected *BER\_Eyes* criterion, multiple BER eye curves are generated. The generated curves are named using the following naming convention:

`eye_<criteria_keyword>_1e-<LBER_value>.cur`

where valid values of *<criteria\_keyword>* are:

- `ber` for Time scale (eye width)
- `nber` for Voltage scale (eye height)
- `jnber` for Both time and voltage

For example, curve file `eye_jnber_1e-12.cur` indicates the *BER\_Eye* curve for *Both time and voltage* and LBERs value -12.

The log BER values are entered in two places in the Analysis Option panel—one is in this field of the *BER\_Eyes* section in the *Channel Simulation* tab and second is in the *Log BER Floor* box of the *Stimulus Definition and Model Selection* section. The log BER tables in the channel simulation report shows the least BER value that is specified in these two places. For example:

- If *BER\_Eyes* has a value of -14 and *Log BER Floor* is -18, the table in the channel simulation report will show -18.
- If *BER\_Eyes* has a value of -21 and *Log BER Floor* is -18, the table in the channel simulation report will show -21.

In addition, the engine has to calculate the BER Value for all the time steps and resolutions. So, sometimes it goes one value more than the required number to ensure that the desired floor is covered.

### **Channel Simulator Controls**

A channel simulator computes the convolution of impulse response (IR) and stimulus of long bit stream. In the *Channel Simulator Controls* box expert users can pass specific controls to the channel simulator using the following syntax:

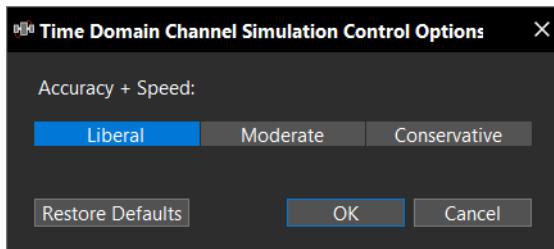
```
<command_name> <value(s)>
```

The specified controls are reflected in the simulation results.

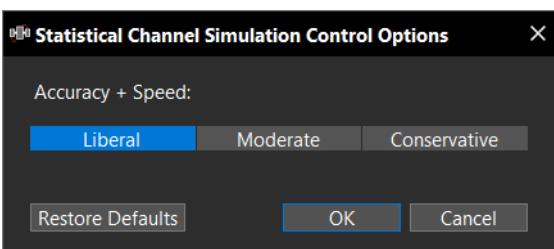
For information about some of the controls that can be input in the *Channel Simulator Controls* field, see [Adding Channel Simulator Controls](#).

### **Advanced Simulator Controls**

If *Time Domain Waveform* is selected as the *Eye Distribution Method*, clicking *Advanced Simulator Controls* opens the *Time Domain Channel Simulation Control Options* dialog box.



If *Statistical* is selected, clicking *Advanced Simulator Controls* opens the *Statistical Channel Simulation Control Options* dialog box.



The following performance and accuracy settings are provided to choose from: *Liberal*, *Moderate*, and *Conservative*.

When *Liberal* is selected, simulations generally take less time at the cost of some accuracy. *Conservative* gives more accurate results, but takes longer to run. The accuracy and speed achieved with *Moderate* is somewhere in the middle.

## IO Models and Stimulus – Serial Link Analysis

In the SLA workflow, the *IO Models and Stimulus* tab of the *Analysis Options* panel is used for source definition, including ignore time, minimum number of bits, bit sampling rate, and stimulus pattern. It also allows you to select IO models for Tx and Rx blocks from the different models present in the IBIS files, based on the [Model Selector] syntax.

This section is primarily divided into the following two subsections:

- [General Definition – Serial Link Analysis](#)
- [Model Selection – Serial Link Analysis](#)

### General Definition – Serial Link Analysis

The contents of this subsection vary depending on the workflow and the properties associated with the Controller, Memory, Tx, and Rx blocks in the topology.

#### ***Ignore Time* or *Ignore Bits***

Specify the initial time or bits to be ignored from the waveform so that the data is not corrupted with the startup time transients.

The list box adjacent to this box has the following two valid values: *ns* and *bits*. The name of the text box is shown as *Ignore Time* if you select *ns* (default), and it changes to *Ignore Bits* if you select *bits* from the list.

**Note:** You can use a lower value such as 100ns if you do not use adaptive equalizers like adaptive DFE.

See also [Difference Between Ignore Bits and Ignore Time](#) for additional related information.

#### ***Minimum # of Bits***

Specify the minimum number of bits to be simulated.

For BER computation, you need to simulate at least 100,000 bits. If you are doing crosstalk simulation, you may need to simulate more bits like 200,000.

### **Bit Sampling Rate**

This parameter controls the granularity used by the channel simulator to compute the eye density. This is analogous in nature to the timestep control in a traditional circuit simulator. The larger the number is, the longer the simulation time is. Default value is 32 samples/bit.

**Note:** Different sampling rates can produce slightly different simulation results within the scope of sampling error. For consistency, it is recommended that you base your methodology on a single sampling rate.

### **Log BER Floor**

Select the check box if the specified minimum Bit Error Rate (BER) should be used in the simulation. The default value specified in the adjacent field is -16.

### **# of Bits for Display**

Specify the number of bits worth of raw waveforms to be saved to disk and displayed. In addition, select *Last* or *First* from the adjacent list box to choose whether to save and display the last or the first number of bits. If you choose to save the last number of bits, the first several bits from the very beginning are ignored while viewing the eye diagram or generating the report.

A channel simulator generates millions of bits worth of waveforms. Saving all this data takes up significant disk space and slows down the display performance. To avoid this, ensure that you set a reasonable number in the *# of Bits for Display* field. For example, if you enter 100 in this field and select *First*, Topology Workbench saves the *first* 100 bits of raw waveform data for display.

### **xTalk Mode**

When performing Single Channel Analysis in the SLA workflow, this list box is disabled and is set to *Ignore xTalk* by default. The list box is editable **only** when you are performing Crosstalk Channel Analysis in the SLA workflow and the following crosstalk modes are available for choice:

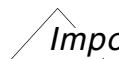
- *Ignore xTalk*
- *Invert All Aggressor Stimulus*
- *Use Aggressor Stimulus As Defined*
- *Random Aggressor Stimulus*

### **Difference Between Ignore Bits and Ignore Time**

The value for *Ignore Bits* is specified in the *Reserved Parameters* of an AMI model and defines how many bits should be ignored before the EDA tool starts collecting distribution

information (PDF) from the waveform about eye height/width. The AMI model needs these many bits for the equalization adaptation algorithms to stabilize or settle down.

*Ignore Time* is the total time that should be ignored before any statistics get collected by the channel simulation engine. This time reflects the system level delays/charge up time. For example, if the channel is made up of a long HDMI cable, the delay of the cable may be 10,000ns. The system must ignore the first 10,000ns before collecting any information about the simulation.

 **Important**

The larger of the two values is used, that is:

- If *Ignore Bits* is smaller than *Ignore Time*, the *Ignore Time* is used.
- If the *Ignore Bits* is larger than the equivalent bits for the *Ignore Time*, then *Ignore Bits* is used.

If the *Ignore Bits* value is larger than the *Ignore Time* set, the simulator does not collect samples for the distribution before the ignore bits run out, but can start collecting information on the outer bounds of the distribution and the center crossing point.

## Model Selection – Serial Link Analysis

This subsection of the *IO Models and Stimulus* tab in the *Analysis Options* panel displays tabs for each Tx and Rx block in the topology. The tabs show related signal, stimulus, and IO model definitions.

The contents of this subsection vary depending on the workflow and the properties associated with the Tx and Rx blocks in the topology. The following simulation parameters can be typically set on the different tabs that are displayed:

### **Signal Name**

Select the groups and signals to include in the simulation run. Clear the check box for the groups or signals that should not be simulated.

### **Data Rate (Gbps)**

Specify the nominal data rate that the system will operate at. For example, PCI Express 2.0 operates at 5 Gbps.

### **Baud Rate (Gbps)**

Specify the nominal data rate that the system will operate at. For example, PCI Express 2.0 operates at 5 Gbps.

Based on the value specified in the *Data Rate* text box, the *Clock Period* and *Bit Period* are calculated automatically and displayed in the respective text boxes.

### **Signaling**

Set the signaling for the stimulus pattern to generate multi-level stimulus pattern for simulation. The following types of signaling is supported:

- *NRZ* is the default option. It indicates the traditional binary signaling.
- *PAM3* and *PAM4* signaling triggers appropriate multi-level signals for the incoming bit stream stimulus for the transmitter and produces multi-level signals at the associated receivers.
- *PAM6* triggers multi-level signaling at Data Rate = Baud Rate x 2.5.
- *PAM8* triggers multi-level signaling at Data Rate = Baud Rate x 3.

**Note:** If the Tx or Rx AMI models contain the reserved parameter, Modulation, then the setting of this reserved parameter dictates the values of the *Signaling* field. As a result, the field might be disabled.

### **Stimulus Pattern**

Define a unique stimulus pattern for each data line and strobe.

To modify the default stimulus pattern of an individual signal or for a bus, right-click a stimulus pattern value in the table and choose *Define Pattern* from the displayed shortcut menu. The *Stimulus Definition* dialog box appears. For more information, see [Modifying Stimulus Pattern](#).

**Note:** This column is not displayed if you have selected *Statistical* as the *Eye Distribution Method* in the [Channel Simulation – Serial Link Analysis](#) tab.

### **Stimulus Offset**

When you set the *Stimulus Pattern* in SLA workflow, the cells in the *Stimulus Offset* column appear as editable text fields. Enter the required stimulus offset value for the signal node or each signal line.

**Note:** This column is not displayed if you have selected *Statistical* as the *Eye Distribution Method* in the [Channel Simulation – Serial Link Analysis](#) tab.

### **Leading Bits**

One of the ways to change the phase alignment during crosstalk simulation. It can also be used before the beginning of a bit stream for training pattern. When you double-click a cell under this column, the *Select Leading Bits File* dialog box opens. A sample file named `leading_bits.txt` is available at:

`<INSTALL_DIR>\share\topxp`

### **Transmit/Receive IO Model**

These columns display corresponding to each signal, the IO model defined for it in the assigned model file. The cells in both these columns are non-editable.

### **Transmit/Receive Jitter & Noise**

Set the Jitter and Noise parameters. Double-clicking a cell under this column opens the *Jitter & Noise* dialog box. For details, see [Setting Jitter and Noise Parameters](#).

### **Status**

This column displays the current status of the listed signal. For example, *Signal*, *Not Connected*, and so on.

## **Configuring Simulation Options for Parallel Bus Analysis**

In the PBA workflow, to configure the simulation options in the *Analysis Options* panel:

1. Specify the circuit simulator of your choice, corner settings, circuit simulations options, and simulation name in the *Circuit Simulation* tab.

**Note:** The settings allowed in the *Circuit Simulation* tab are the same for all workflows.

2. Configure the bus simulation run in the *Bus Simulation* tab.
3. Specify the characterization options, the method for generating the eye diagrams (*BER\_Eyes*), and the global controls for the channel simulator in the *Channel Simulation* tab.

#### **Important**

The *Channel Simulation* tab is displayed only if you selected the *Use Channel Simulator* check box in the *Workflow* panel.

4. Set the simulation parameters such as following in the *IO Models and Stimulus* tab:
  - a. Data Rate, Ignore Time, Minimum # of Bits, Bit Sampling Rate
  - b. Signals that need to be modeled during the simulation

# Topology Workbench User Guide

## Preparing for a Simulation Run

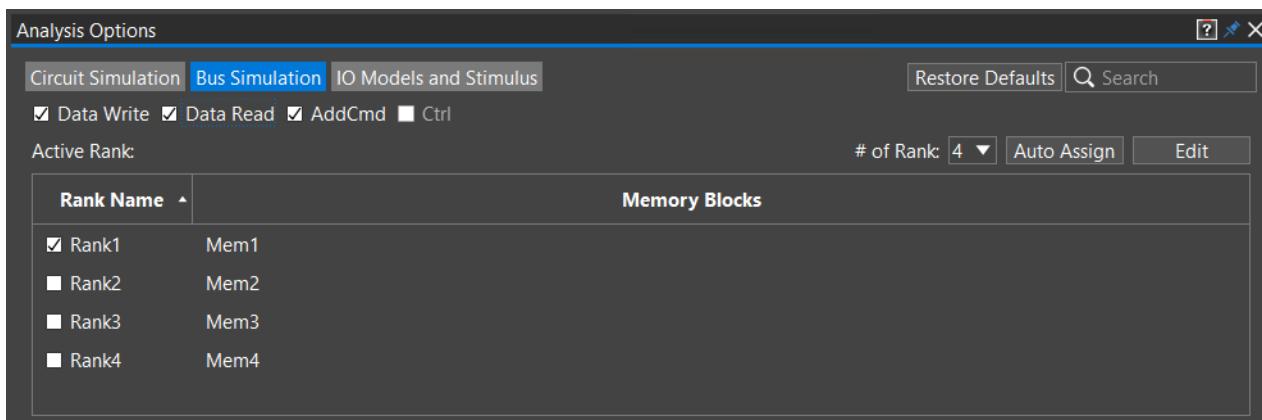
- c. Stimulus pattern and offset, transmitter/receiver IO models, and transmitter/receiver jitter and noise

### Related Topics

- [Circuit Simulation](#)
- [Bus Simulation](#)
- [Channel Simulation – Parallel Bus Analysis](#)
- [IO Models and Stimulus – Parallel Bus Analysis](#)
  - [General Definition – Parallel Bus Analysis](#)
  - [Model Selection – Parallel Bus Analysis](#)
- [Restore Defaults](#)

## Bus Simulation

This tab lets you configure a bus simulation run.



### Data Write

Select to simulate the bus as a writable data bus. When this value is selected, you need to also set *Direction*, *Active Rank*, and *# of Rank*.

**Note:** When *Data Read* is also selected, two simulations are run, one for write and the other for read. Similarly, you can select *AddCmd* to run a full bus simulation for both address and data buses in a single run.

### **Data Read**

Select to simulate the bus as a read data bus. When this value is selected, you need to also set *Direction*, *Active Rank*, and *# of Rank*.

**Note:** When *Data Write* is also selected, two simulations are run, one for write and the other for read. Similarly, you can select *AddCmd* to run a full bus simulation for both address and data buses in a single run.

### **AddCmd**

Select to simulate the bus as a AddCmd bus. Selecting this removes all other parameters from the *Bus Simulation* tab and readjusts the contents of the IO Models and Stimulus – Parallel Bus Analysis tab to display signals of *Address* type and widgets like *Signal Clocking*.

**Note:** You can select *Data Write* and/or *Data Read* along with *AddCmd* to run a full bus simulation for both address and data buses in a single run.

### **Ctrl**

Select to simulate the bus as a Ctrl bus. This check box is disabled when *Data Write*, *Data Read*, and *AddCmd* are selected.

### **# of Rank**

Select the number of ranks in which the memory blocks of a *Data* bus topology should be organized. A rank is a group of memory blocks that are active or inactive together.

Consider an example where data signals `DQ[7:0]` from the controller are connected to `Mem_U1` and `Mem_U10`, and `DQ[15:8]` are connected to `Mem_U2` and `Mem_U11`. This allows `Mem_U1` and `Mem_U2` to be grouped as *Rank1*, and `Mem_U10` and `Mem_U11` to be grouped as *Rank2*. In case of a *Write* simulation for this data bus, *Rank1* or *Rank2* will be active (that is, receiving on a *Write*), while the other rank will be placed in standby mode.

Grouping memory blocks into ranks enables more efficient simulations to be run, eliminating unnecessary combinations of active/inactive memory blocks, and reducing the number of overall simulations to be run.

By default, the *# of Ranks* list contains the maximum number as per the number of memory blocks. For example, if there are four memory blocks in the topology, the list will show numbers 1, 2, 3, and 4 as the *# of Ranks*.

### **Active Rank**

Select the check box adjacent to a *Rank Name* to identify it as an active rank.

The active rank allows a single *Data bus* simulation to contain multiple active memory blocks.

- All memory blocks in an active rank are active together.
- If more than one ranks are checked as active, the tool will do multiple simulations for active rank sweeping: each simulation will only have one active rank while others will be considered as standby.

When a number is selected from the *# of Ranks* list, multiple ranks of the selected number will be automatically added to the *Rank Name* column in the *Active Rank* table.

- If the selected # is 1, *Rank1* contains all memory blocks.
- If the selected # is maximum, each rank contains one memory.
- If the selected # is neither 1 nor maximum, the ranks are assigned randomly.

### **Auto Assign**

When the *Auto Assign* button is clicked, the tool automatically assigns the memory blocks based on Frequency Response.

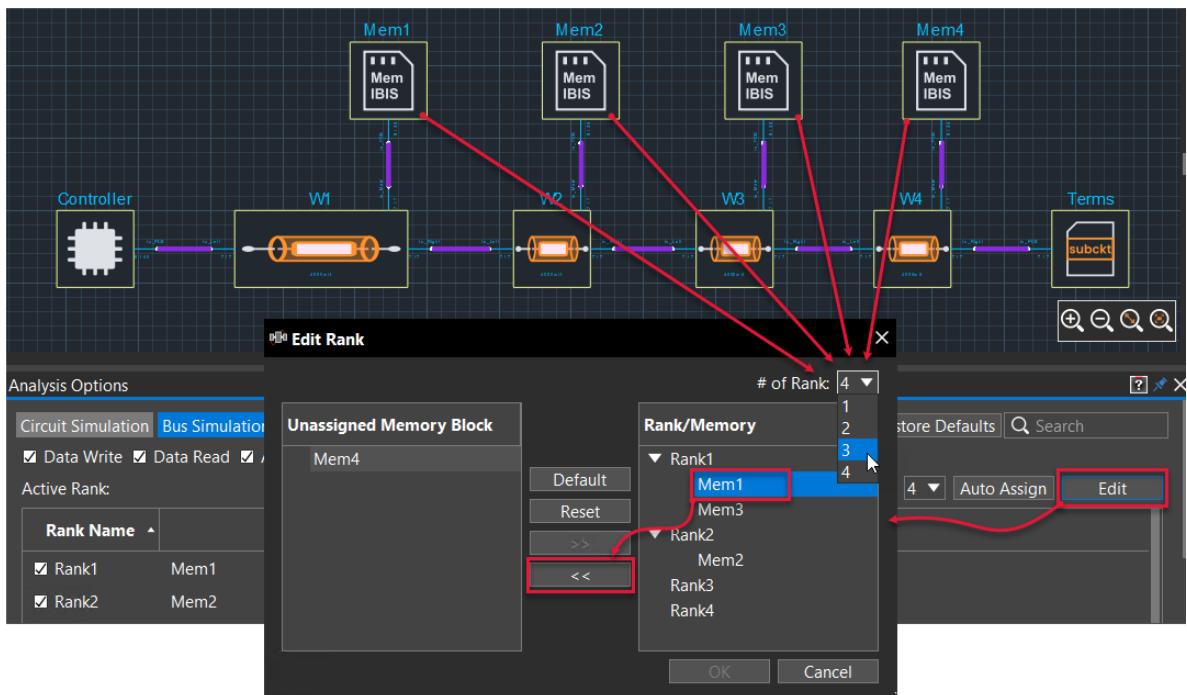
**Note:** The connectivity checker should be run before automatically assigned the memory blocks. If the checker has not been run already, a message prompts you to check the connectivity.

# Topology Workbench User Guide

## Preparing for a Simulation Run

### Edit

When the *Edit* button is clicked, the Edit Rank dialog box opens where you can manually assign the ranks to each memory block.



In the *Rank Edit* dialog box, you can:

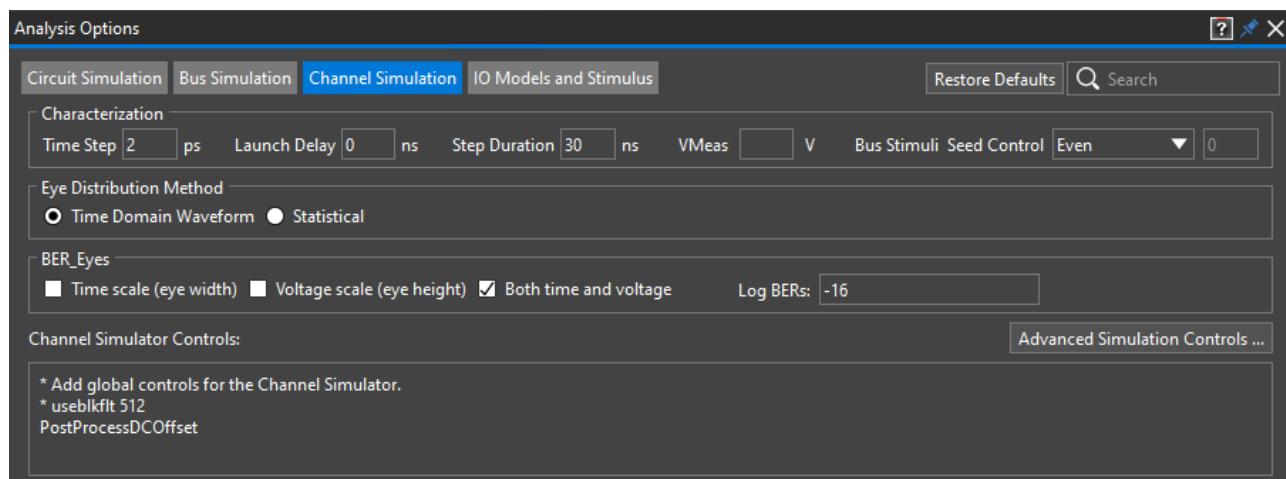
- Select a memory block in the *Unassigned Memory Block* pane, drag it to the *Rank/Memory* pane, and drop it under the rank to which it needs to be assigned.
- Select a memory block in the *Rank/Memory* pane and click the << button to remove it from the corresponding rank and move to the *Unassigned Memory Block* pane.
- Select the required number from the *# of Rank* list. The list box contains numeric values equivalent to the number of memory blocks that exist in the topology.

## Channel Simulation – Parallel Bus Analysis

### Important

In PBA workflow, the *Channel Simulation* tab is displayed **only** when you choose to use a channel simulation. Only the simulation parameters unique to PBA workflow are covered below. For information about the other common simulation parameters that can be set in the *Channel Simulation* tab, see [Channel Simulation – Serial Link Analysis](#).

The following image shows the *Channel Simulation* tab that is displayed in the PBA workflow:



**Note:** When channel simulation is run, you can also review the simulation correlation between the time domain circuit simulation and the channel simulation results. For this, choose *Tools – Circuit/Channel Sim Correlation* from the menu bar. See [Correlating Circuit and Channel Simulations](#) for detailed information. In addition, you have the option for [Running and Reviewing Characterization](#).

### **Characterization**

**Note:** In the PBA workflow, selecting the *Cycle* check box in the [Channel Simulation](#) tab of the *Options* dialog box disables the *Launch Delay* and *Step Duration* boxes.

#### *Time Step*

Define the time step to be used in the characterization.

### *Bus Stimuli*

Select the type of bus stimuli to be used during a simulation run. The following options are provided in the list:

- *Random*

Topology Workbench randomly switches the step for characterization in the opposite direction (in `simulation_input.sp`). For each `vlow`, use a random function to chose 0 or 1; `vhigh` should be 1-`vlow`.

- *Even*

When this option is checked, the stimulus on the transmitters is left as it was defined, with no inversion.

### *Seed Control*

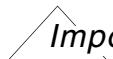
Specify a seed control value to keep the same seed selection if multiple characterization runs need to be performed.

## **IO Models and Stimulus – Parallel Bus Analysis**

The *IO Models and Stimulus* tab of the *Analysis Options* panel is used for source definition, including data rate, delay, and pattern. It also allows you to select IO models for Controller, Memory, Tx, and Rx blocks from the different models present in the IBIS files, based on the [Model Selector] syntax.

This section is primarily divided into the following two subsections:

- General Definition – Parallel Bus Analysis
- Model Selection – Parallel Bus Analysis



Some simulation parameters are specially displayed in PBA workflow when you opt to run channel simulation. These parameters have already been described in the [IO Models and Stimulus – Serial Link Analysis](#) section. Therefore, in this section, only the simulation parameters unique to PBA workflow are covered.

## General Definition – Parallel Bus Analysis

The contents of this subsection vary depending on the workflow and the properties associated with the Controller, Memory, Tx, and Rx blocks in the topology.

### **Data Rate**

Specify the nominal data rate that the system will operate at.

Based on the value specified in the *Data Rate* text box, the *Clock Period* and *Bit Period* are calculated automatically and displayed in the respective text boxes.

### **Minimum # of Bits**

Specify the minimum number of bits to be simulated.

For BER computation, you need to simulate at least 100,000 bits. If you are doing crosstalk simulation, you may need to simulate more bits like 200,000.

### **Signal Clocking**

**Note:** Displayed only when *Bus Type* is set to *AddCmd* in the Bus Simulation tab.

For address bus simulations, you can set up *1T*, *2T*, and *3T* timing to observe the signal quality and timing improvement of address bus.

## Model Selection – Parallel Bus Analysis

This subsection of the *IO Models and Stimulus* tab in the *Analysis Options* panel displays tabs for each Controller, Memory, Tx, and Rx block in the topology. The tabs show related signal, stimulus, and IO model definitions.

**Note:** This subsection is enabled when the block has an associated IBIS file.

The contents of this subsection also vary depending on the workflow and the properties associated with the Controller, Memory, Tx, and Rx blocks in the topology. The following simulation parameters can be typically set on the different tabs that are displayed:

### **Memory Block Shared IO Models**

Select this check box if the Memory blocks should share same IO model. If this option is deselected, different IO models can be specified for the memory blocks. To do this, an individual dedicated tab is displayed for each memory block on the canvas.

**Note:** For designs with single memory device, this option is selected by default and is disabled.

### **WLO/ClkMeasDelay**

This option is enabled only for data buses and is useful for designs with multiple memory blocks. To generate useful values of Write Leveling Offset (WLO) and the Delay (ClkMeasDelay), the clock and the timing reference signals must be defined and connected for data buses.

If this option is selected for Data Bus Write simulation, WLO is added to the Stimulus Offset of the data and timing reference signals at the Controller.

In case of Data Bus Read simulation, the ClkMeasDelay value is added to the *Stimulus Offset* of the data and timing reference signals at the Memory.

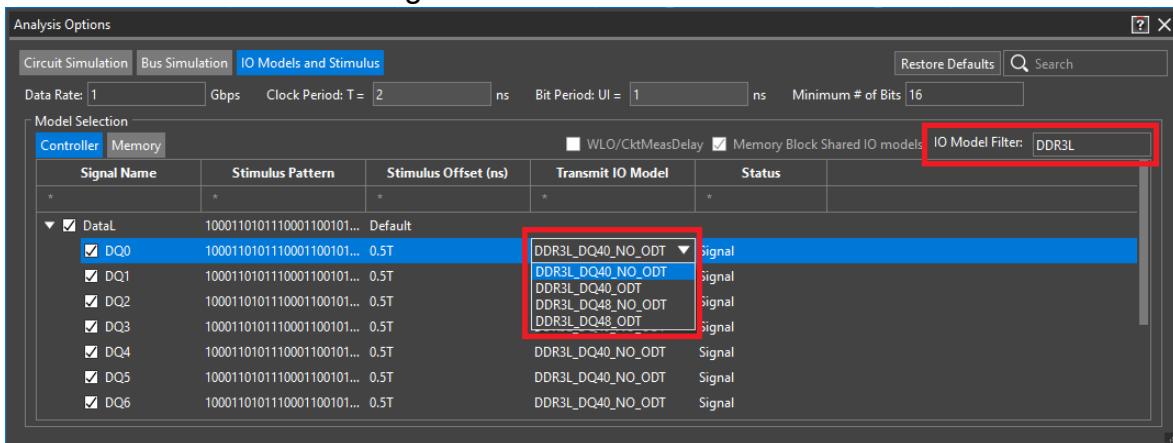
Depending on the topology, the WLO and ClkMeasDelay values are different for each Data Bus Group. The WLO and ClkMeasDelay values used during simulation are specified or calculated in the *Write Leveling* panel. For more information, see [Calculating Write Leveling Offset](#).

# Topology Workbench User Guide

## Preparing for a Simulation Run

### IO Model Filter

When a filtering criteria is specified in this box, the list displayed while editing the Transmit, Receive, and Standby IO Model fields are filtered accordingly. For example, in the image below when you enter *DDR3L* in the *IO Model Filter* box, the IO models displayed while editing *Transmit IO Model* for *DQ0* include only the ones that have name starting with *DDR3L*:



### Signal Name

Select the groups and signals to include in the simulation run. Clear the check box for the groups or signals that should not be simulated.

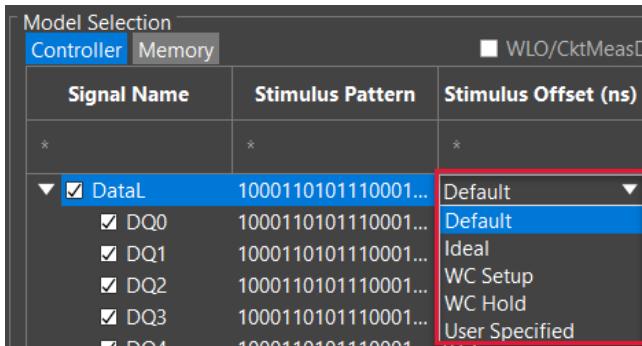
### Stimulus Pattern

Define a unique stimulus pattern for each data line and strobe.

To modify the default stimulus pattern of an individual signal or for a bus, right-click a stimulus pattern value in the table and choose *Define Pattern* from the displayed shortcut menu. The *Stimulus Definition* dialog box appears. For more information, see [Modifying Stimulus Pattern](#).

### **Stimulus Offset**

In PBA workflow, a list of supported stimulus offset options as shown below is displayed:



The stimulus offset of timing ref is set to the default stimulus offset, and that of signals is set ‘on-the-fly’.

- Default*      The timing reference signal (for example, strobe) is positioned in the middle of the bus signals’ eye. For example, in the case of a data bus, the strobe would be set to lag the data by a quarter clock cycle.
- Ideal*      Similar to the *Default* offset, but the buffer delays for the signal are taken into account to make the desired stimulus offset (for example, quarter clock cycle) more exact.

For a data bus group, if the *Stimulus Offset* is set to *Default* or *Ideal*, the following best case timing reports are generated:

- *Timing Report – Best Case Timing*
- *Timing Report – Best Case Eye Height*

#### *Important*

When performing best case timing calculation, Topology Workbench uses the measurement raw data, tDS and tDH, as input to calculate a balanced setup and hold time, not considering the derating effects and minimal setup and hold requirements.

- WC Setup*      Stimulus offsets are made to replicate the *Min Transmit Setup* value specified in the *Timing Budget* panel, accounting for buffer delays. This should represent the worst case (WC) setup condition.

## Topology Workbench User Guide

### Preparing for a Simulation Run

**WC Hold** Stimulus offsets are made to replicate the *Min Transmit Hold* value specified in the *Timing Budget* panel, accounting for buffer delays. This should represent the worst case hold condition.

#### *User Specified*

When selected, you can add or replace the existing values per the requirement.

**Note:** In case of a *Data bus*, the Controller or the Memory can drive the bus. Therefore, *Stimulus Offsets* can be defined for the *Controller* on a *Write* simulation, and for the *Memory* on a *Read* simulation. When the Memory is driving the bus, the following worst case-related options are provided:

#### *WC Tx Skew (+)*

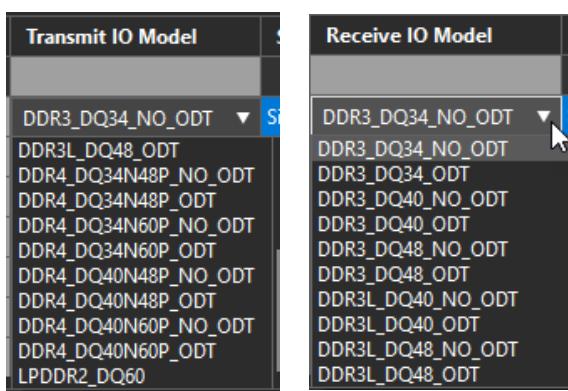
Stimulus offsets are made to replicate the *Transmit Skew (+)* value specified in the *Timing Budget* panel, accounting for buffer delays. This should represent the worst case skew condition, where the data signals lag the strobe.

#### *WC Tx Skew (-)*

Stimulus offsets are made to replicate the *Transmit Skew (-)* value specified in the *Timing Budget* panel, accounting for buffer delays. This should represent the worst case skew condition, where the data signals lead the strobe.

### ***Transmit/Receive IO Model***

These columns display corresponding to each signal, the IO model defined for it in the assigned model file. Use the cells in these column to view and assign the required models for the required signals as shown below.



**Note:** If both *Write* and *Read* options are selected in the Bus Simulation tab, a column for Receive IO model is also displayed along with Transit IO model.

### **Status**

This column displays the current status of the listed signal. For example, *Signal*, *Timing Ref*, *Not Connected*, and so on.

**Note:** There should be a single timing reference for each bus.

## **Configuring Simulation Options for SystemPI Workflows**

In the SystemPI workflows, to configure the simulation options in the *Analysis Options* panel:

1. Specify the circuit simulator of your choice, circuit simulations options, and simulation name in the *Circuit Simulation* tab.

**Note:** The settings allowed in the *Circuit Simulation* tab are similar in all workflows. However, for SystemPI – DC IR Drop Analysis, you only have to configure the *Circuit Simulation* tab.

2. Set the simulation parameters, such as, *Time Step* and *Time Stop* for SystemPI – PDN Impedance and Power Ripple Analysis. By default, these parameters are set automatically. To specify custom values, deselect the *Auto* check box.

The *Analysis Options* panel has a *Restore Defaults* button to reset the custom values to the respective defaults.

**Note:** To edit the parameters given in the table, you need to double-click the IC block on the canvas to open the corresponding *Edit Properties* panel and click the *Derive Target Impedance* button.

### **Related Topics**

- [Circuit Simulation](#)
- [Restore Defaults](#)

## **Modifying Stimulus Pattern**

To modify the stimulus pattern:

1. Right-click a cell under the *Stimulus Pattern* column in the *Model Selection* section of the *Analysis Options* panel.

**Note:** If the right-clicked cell is from the row dedicated to a data bus group, each data

## Topology Workbench User Guide

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and strobe line is impacted from the modifications that are made to the stimulus definition. However, when the right-clicked cell corresponds to a specific signal, such as *DQ1*, the stimulus pattern for only that signal is modified.

2. Choose *Define Pattern* from the displayed shortcut menu. The *Stimulus Definition* dialog box opens.
3. Select an appropriate *Data Pattern* from the list. By default, *Random* is selected.

**Note:** The options available for choice in the *Data Pattern* list depend on the workflow in which you are setting the analysis options.

4. Make the necessary changes in the UI controls that are displayed based on the *Data Pattern* option you choose. Refer to the following sections to know more about these UI controls:
  - ❑ [Topology Explorer: Controls for Setting the Stimulus Pattern](#)
  - ❑ [Serial Link Analysis: Controls for Setting Stimulus Pattern](#)
  - ❑ [Parallel Bus Analysis: Controls for Setting Stimulus Pattern](#)
5. Click *OK*. The *Stimulus Definition* dialog box closes and the defined pattern shows in the *Stimulus Pattern* column depending on the cell you right-clicked in step 1. The image given below illustrates the difference in the impact of modifying the stimulus pattern at a group level and for specific signal.

**Stimulus Pattern Changes for all Signals in the Selected Group**

Signal Name	Stimulus Pattern	Stimulus Offset	
▼ <input checked="" type="checkbox"/> DataL	10101010..	Default	
<input checked="" type="checkbox"/> DQ0	10101010..	Default	<a href="#">Define Pattern...</a>
<input checked="" type="checkbox"/> DQ1	10101010..	0.5T	<a href="#">Define Pattern...</a>
<input checked="" type="checkbox"/> DQ2	10101010..	0.5T	
<input checked="" type="checkbox"/> DQ3	10101010..	0.5T	
<input checked="" type="checkbox"/> DQ4	10101010..	0.5T	

Signal Name	Stimulus Pattern
▼ <input checked="" type="checkbox"/> DataL	0011011111001101..
<input checked="" type="checkbox"/> DQ0	0011011111001101..
<input checked="" type="checkbox"/> DQ1	0011011111001101..
<input checked="" type="checkbox"/> DQ2	0011011111001101..
<input checked="" type="checkbox"/> DQ3	0011011111001101..
<input checked="" type="checkbox"/> DQ4	0011011111001101..

**Stimulus Pattern Changes for a Specific Signal in the Group**

Signal Name	Stimulus Pattern	Stimulus Offset	
▼ <input checked="" type="checkbox"/> DataL	10101010..	Default	
<input checked="" type="checkbox"/> DQ0	10101010..	0.5T	
<input checked="" type="checkbox"/> DQ1	10101010..	0.5T	<a href="#">Default</a>
<input checked="" type="checkbox"/> DQ2	10101010..	0.5T	<a href="#">Default</a>
<input checked="" type="checkbox"/> DQ3	10101010..	0.5T	<a href="#">Default</a>
<input checked="" type="checkbox"/> DQ4	10101010..	0.5T	

Signal Name	Stimulus Pattern
▼ <input checked="" type="checkbox"/> DataL	10101010..
<input checked="" type="checkbox"/> DQ0	10101010..
<input checked="" type="checkbox"/> DQ1	0011011111001101..
<input checked="" type="checkbox"/> DQ2	10101010..
<input checked="" type="checkbox"/> DQ3	10101010..
<input checked="" type="checkbox"/> DQ4	10101010..

## Topology Explorer: Controls for Setting the Stimulus Pattern

### ***Data Pattern = Random***

(Default) A random stimulus pattern is generated by the tool based on the values specified in the *Seed* and *# of Bits* boxes.

***Seed*** Specify an integer to define the number of seeds. By default, it is set to 1.

***# of Bits*** Specify the number of bits to be simulated in the *# of Bits* box.

**Note:** This box is read-only when *Data Pattern = Data File*.

***# of Signals*** This is a read-only box that displays the number of signals for which stimulus pattern is being modified.

***Same Pattern for all Signals*** By default, this check box is selected. Therefore, all signals have the same stimulus pattern.

To specify different stimulus pattern for different signals, deselect the *Same Pattern for all Signals* check box. However, in this case, you must ensure that the pattern lines in the specified data pattern file are greater than or equal to the number of signals to be simulated. If the pattern lines in the data file are less than the number of signals, an error message is displayed when the *Same Pattern for all Signals* check box is deselected.

***Result*** This is a read-only text box that is populated with a preview of the stimulus pattern when the *Preview* button is clicked.

***Repeat*** This check box is selected by default. Select the *Repeat* check box for cases where simulation time is larger than the defined pattern. This causes the stimulus pattern to be repeated.

When you deselect the *Repeat* check box, notice that the two periods displayed at end of the sample bit pattern shown in the *Result* box are removed. These two periods are indicative of the bit pattern being repeated over and over until the desired number of bits has been reached.

### **Data Pattern = PRBS**

A Pseudo Random Binary Sequence (PRBS) stimulus pattern is generated. Each data signal is driven by the PRBS pattern.

When this data pattern is selected, an additional field, *Poly*, is displayed to enter an integer value for the PRBS Polynomial. The other controls are the same as those described for Data Pattern = Random above.

### **Data Pattern = Data File**

Stimulus pattern is read from the specified data file in which you can save the desired bit patterns to use with Topology Workbench.

Apart from the *File* box describe below, the other controls are the same as those described for Data Pattern = Random above. However, the *# of Bits* box is read-only because the value is based on the selected data file.

**File** Click the browse button (...) adjacent to this box and select the required data file containing user-defined bit pattern definitions.

While creating the user-defined bit patterns, ensure that two periods are included at the end of the bit pattern. For example:  
0101111000110100..

The two periods ensure that the bit pattern is repeated over and over until the desired number of bits has been reached. If the two periods are not included, just a short bit stream will be run. A sample bit pattern text file is provided at:

<INSTALL\_DIR>\share\topxp

### **Data Pattern = Pulse**

Defines the stimulus pattern for the Pulse Width waveform. When this *Data Pattern* is selected, you need to select one of the following options and define the *DCD: Pulse* (default), *Rise*, *Fall Quiet Hi*, or *Quiet Lo*.

### **Data Pattern = PWL**

Defines the stimulus pattern for Piecewise Linear waveform. When this *Data Pattern* is selected, you need to define the *Init* and *Switch Times* (in ns).

## **Defining Stimulus Pattern for an I/O Block in a Topology Imported from Allegro**

In a topology imported from an Allegro tool, the I/O block retains its original properties and shape. By default, this block is treated as an equivalent of a receiver block in Topology

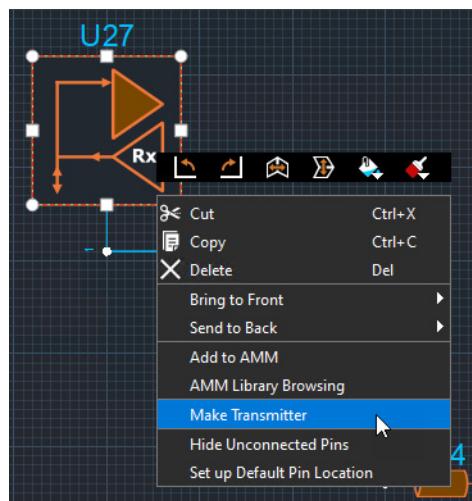
# Topology Workbench User Guide

## Preparing for a Simulation Run

Workbench. Therefore, when you review the *Analysis Options* panel for this topology, the tab specific to the I/O block shows details of a receiver:



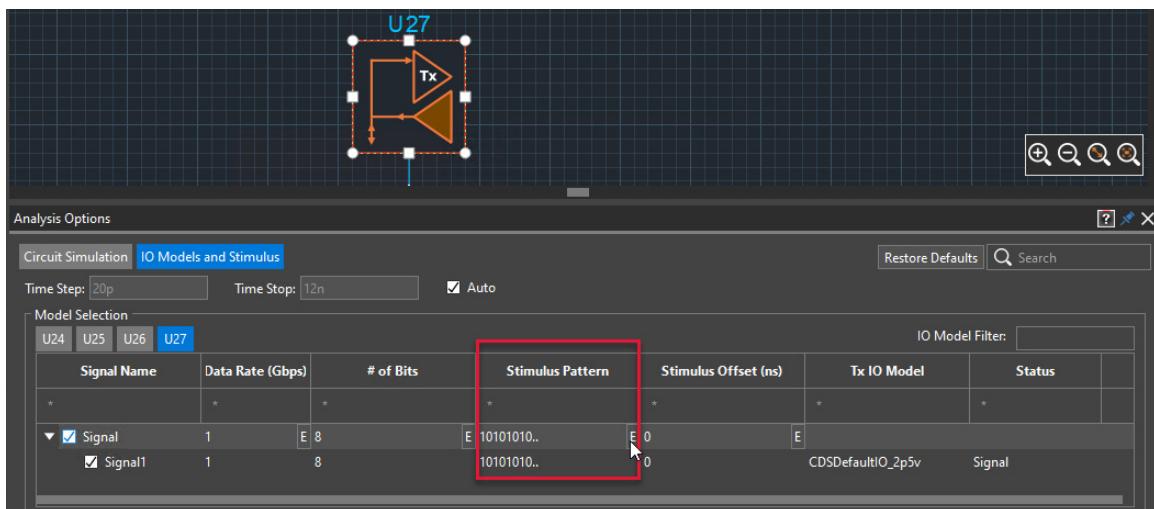
To define a stimulus for an I/O block, you need to first change its core property to that of a transmitter. Therefore, right-click the block and click *Make Transmitter* from the shortcut menu.



## Topology Workbench User Guide

### Preparing for a Simulation Run

The *Analysis Options* panel now refreshes the information in the tab for the selected I/O block. In the *Stimulus Pattern* column, you can now define the required stimulus pattern to configure the block for simulation.



## Serial Link Analysis: Controls for Setting Stimulus Pattern

### **Data Pattern = Random**

(Default) A random stimulus pattern is generated by the tool based on the specified Data Coding and Rise/Fall Time values.

### **Data Pattern = PRBS**

A Pseudo Random Binary Sequence (PRBS) stimulus pattern is generated. Each data signal is driven by the PRBS pattern.

When this data pattern is selected, you can specify Data Coding and Rise/Fall Time. Additionally, you can enter an integer value for the PRBS Polynomial in the Poly box.

### **Data Pattern = Data File**

Stimulus pattern is read from the specified data file in which you can save the desired bit patterns to use with Topology Workbench.

When this data pattern is selected, apart from the File box described below, you can specify Data Coding and Rise/Fall Time.

**File** Click the browse button (...) adjacent to this box and select the required data file containing user-defined bit pattern definitions.

While creating the user-defined bit patterns, ensure that two periods are included at the end of the bit pattern. For example:  
0101111000110100..

The two periods ensure that the bit pattern is repeated over and over until the desired number of bits has been reached. If the two periods are not included, just a short bit stream will be run. A sample bit pattern text file is provided at:

<INSTALL\_DIR>\share\topxp

#### **Data Pattern = Sinusoidal Waveform**

Defines the stimulus pattern for Sinusoidal waveforms.

When this data pattern is selected, the Data Coding check box and list box are disabled. Similarly, the Rise/Fall Time check box and the related *Rise Time* and *Fall Time* boxes are disabled.

#### **Data Pattern = Sawtooth**

Defines the stimulus pattern for sawtooth waveforms.

When this data pattern is selected, the Data Coding check box and list box are disabled. Similarly, the Rise/Fall Time check box and the related *Rise Time* and *Fall Time* boxes are disabled.

#### **Data Pattern = Clock**

Defines the stimulus pattern for the clock.

When this data pattern is selected, the Data Coding check box and list box are disabled. Similarly, the Rise/Fall Time check box and the related *Rise Time* and *Fall Time* boxes are disabled.

### **Data Coding**

Select the data coding type from the list box to place the required type of statistical bounds on the rate of signal transitions. It allows for easier clock recovery in the receiver and for DC balance. The following data coding types are available for selection:

- *8b10b*
- *64b66b (Default)*
- *64b67b*
- *128b130b*
- *128b132b*
- *16b18b*

**Note:** If you do not want to apply a data coding type, deselect the check box adjacent to *Data Coding*. Also, *Data Coding* is disabled when the *Data Pattern* is set to *Sinusoidal Waveform*, *Sawtooth*, or *Clock*.

If the Tx or Rx AMI models contain the reserved parameter, *PAM4\_Mapping*, then the setting of this reserved parameter dictates the values of the *Data Coding* field. As a result, the field might be disabled.

### **Rise/Fall Time**

The following fields are enabled when you select the check box adjacent to *Rise/Fall Time*:

<i>Rise Time</i>	Specifies the rise and fall time of the stimulus bit stream signal provided to the transmitter, 0% to 100%. This is essentially another way to introduce Duty Cycle Distortion (DCD) by enabling the definition of asymmetric rise and fall times. If no explicit rise and fall times are specified, Topology Workbench defaults to the time step of the circuit simulator used for characterization. Unless the intent is to introduce asymmetry to the stimulus signal, it is recommended to leave these parameters unset.
<i>Fall Time</i>	

## Parallel Bus Analysis: Controls for Setting Stimulus Pattern

### **Data Pattern = Random**

(Default) A random stimulus pattern is generated by the tool based on the values specified in the *Seed* and *# of Bits* boxes.

If the *Use Channel Simulator* check box is **not selected** in the *Workflow* panel, you see the same UI controls that are displayed for Data Pattern = Random in the Topology Explorer workflow. In addition, the *Data Bus Inversion* check box is available for selection. It is deselected by default. Selecting this check box lets you enable the capability to examine the effect of Data Bus Inversion (DBI) on the data bus signals. DBI limits how many signals can be driven low at a time to avoid a worst case power situation. If DBI is enabled and the driver (that is, the controller during a write or DRAM during a read) is sending out data on a lane, it counts the number of "0" (logic low) bits. For example, for an 8-bit stimulus pattern, if the number of bits driving "0" in the lane is five or more, then the entire byte is inverted. This ensures that out of the eight DQ bits, at least five bits are "1" during any given transaction.

If the *Use Channel Simulator* check box is **selected** in the *Workflow* panel, only the *Seed* box is displayed to specify an integer to define the number of seeds. By default, *Seed* is set to 1.

### **Data Pattern = PRBS**

A Pseudo Random Binary Sequence (PRBS) stimulus pattern is generated. Each data signal is driven by the PRBS pattern.

When this data pattern is selected, an additional field, *Poly*, is displayed to enter an integer value for the PRBS Polynomial. The other controls are the same as those described for Data Pattern = Random.

**Note:** The current implementation does not apply the stimulus uniformly. Therefore, when PRBS is applied as the stimulus for channel simulation in the PBA workflow, different seeds are used for each signal in the bus to be simulated. This generates different patterns for each signal.

### **Data Pattern = Data File**

Stimulus pattern is read from the specified data file in which you can save the desired bit patterns to use with Topology Workbench.

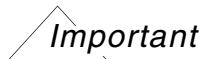
Apart from the *File* box describe below, the other controls are the same as those described for Data Pattern = Random. However, the *# of Bits* box is read-only because the value is based on the selected data file.

<b>File</b>	Click the browse button (...) and select the required data file containing user-defined bit pattern definitions.  While creating the user-defined bit patterns, ensure that two periods are included at the end of the bit pattern. For example: 0101111000110100..  The two periods ensure that the bit pattern is repeated over and over until the desired number of bits has been reached. If the two periods are not included, just a short bit stream will be run. A sample bit pattern text file is provided at: <code>&lt;INSTALL_DIR&gt;\share\topxp</code>
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#### **Data Pattern = Worst Case**

When selected, Topology Workbench automatically generates the worst case patterns for the signals.

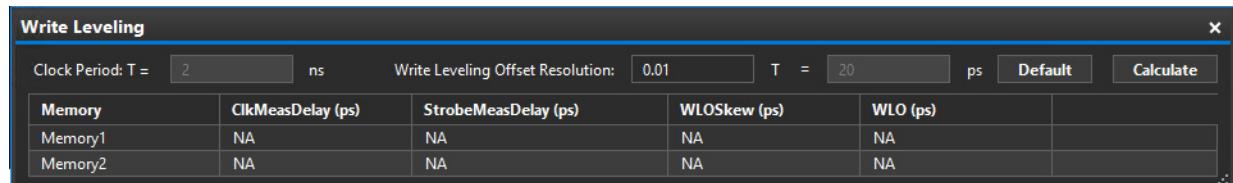
## Calculating Write Leveling Offset



The feature discussed in this section is available only in the PBA workflow.

For specifying and calculating Write Leveling Offset (WLO):

1. Choose *Tools – Write Leveling* from the menu bar. This opens the *Write Leveling* panel as shown below:

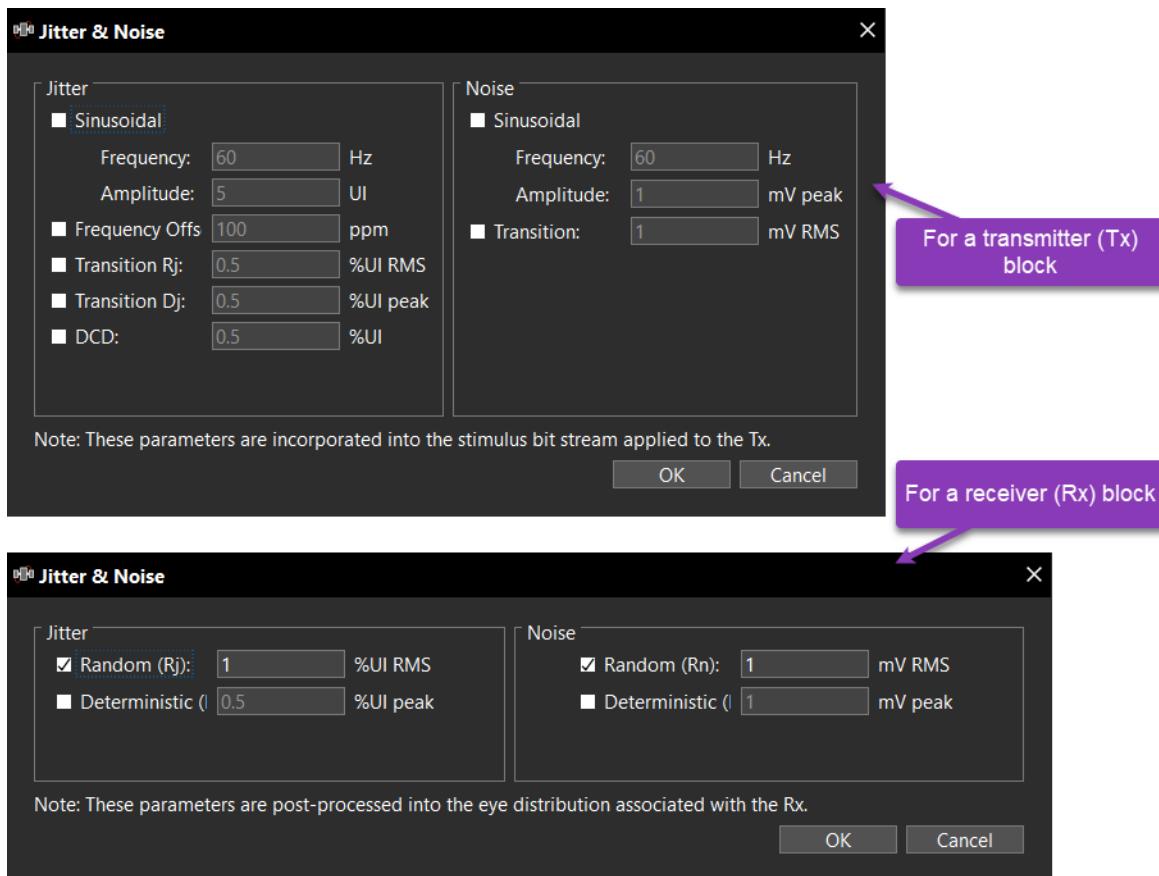


2. Specify a value in the *Write Leveling Offset Resolution* box, or click *Default* to use a default value.
3. Click *Calculate* to auto-calculate the WLO and CLK delay values by simulating the design.
- If required, you can manually edit the values in the *ClkMeasDelay*, *StrobeMeasDelay*, and *WLO* columns.
4. Click *OK* to save the WLO values.

## Setting Jitter and Noise Parameters

When channel simulation is used, the *Jitter & Noise* dialog box is accessible from the *Transmitter/Receiver Jitter & Noise* column of the *Model Selection* subsection in the *IO Models and Stimulus* tab of the *Analysis Options* panel. The dialog box is divided in two sections, *Jitter* and *Noise*.

The displayed jitter and noise elements are disabled by default. To make an element editable, select the check box adjacent to it.



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Depending on the stimulus pattern you select from the *Data Pattern* list in the *Stimulus Definition* dialog box, the contents of the *Jitter & Noise* dialog box vary. The following jitter and noise parameters can be set using this dialog box:

#### **Jitter**

##### *Sinusoidal*

Specify the frequency of the sinusoid jitter source in Hz and the amplitude in UI. This is one of the principle ways to test Jitter Tolerance.

##### *Frequency Offset*

Specify the deviation from the nominal data rate in parts-per-million or ppm. If the *Bit Rate* is 10 Gb/s, the actual rate can be 10 Gb/s +/- 1e6.

##### *Transition Rj*

Applied to each logic transition of the transmitter's incoming bit stream (that is, stimulus signal) in a Gaussian distribution.

##### *Transition Dj*

Applied to each logic transition of the transmitter's incoming bit stream (that is, stimulus signal) in a rectangular window of equal probability.

##### *DCD (%)*

Specify the type of Dj. It describes the deviation in duty cycle value from the ideal value. It can also be modeled asymmetrically between rise and fall time at the transmitter.

##### *Random Jitter (Rj) (%UI RMS)*

Jitter that has not been bounded is referred to as random jitter. It is described by a Gaussian probability distribution, and characterized by its standard deviation (RMS) value. This type of jitter is caused by thermal noise or other random noise effects in the system. Its default value is 1% of the bit time.

*Deterministic Jitter ( $D_j$ ) (%UI peak)*

Deterministic jitter is a jitter with a non-Gaussian probability density function. This type of jitter is always bounded in amplitude and with specific causes. Its default value is 1% of the bit time.

**Noise**

*Sinusoidal*

Specify the frequency of the sinusoid jitter source in Hz and the amplitude in percentage of input voltage swing. The noise that is usually introduced through the reference clock on the PLL is modeled as a sinusoid.

*Transition (mV RMS)*

It is the type of  $D_n$  and is applied at each transmitter edge.

*Random Noise ( $R_n$ ) (mV RMS)*

It is caused by random fluctuations in the signal voltage.

*Deterministic Noise ( $D_n$ ) (mV peak)*

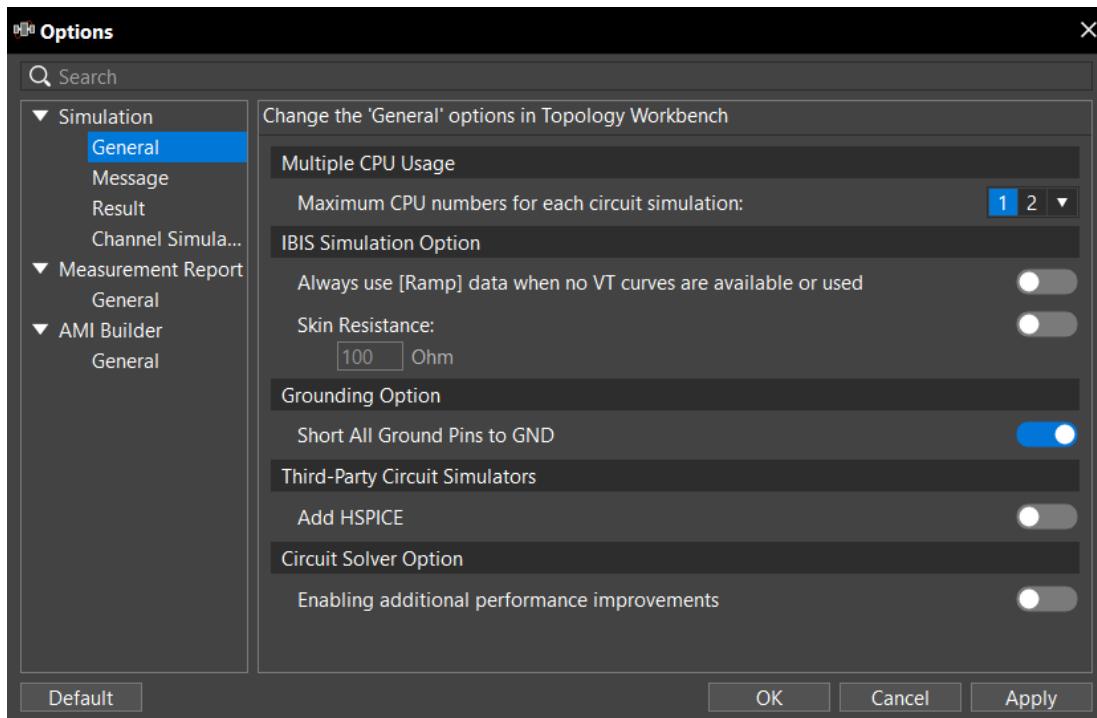
This value depends on the power supply. It can have many sources, such as, capacitive and inductive coupling.

$R_j$ ,  $D_j$ ,  $R_n$ , and  $D_n$  are all post-processed jitter and noise. They show up in the Bathtub curve, which is a cumulative distribution function. Other types of deterministic jitter are added to the Transmitter Bit Stream, such as:

- Periodic jitter
- DCD
- Duty Cycle Distortion

## Configuring General Simulation Options

The *Options* dialog box lets you set a few general simulation settings. To display this dialog box, select *Tools – Options* from the menu bar.



The *Simulation* tree in the dialog box provides the following modules:

- General
- Message
- Result
- Channel Simulation
- Frequency Sampling (SystemPI – PDN Impedance and Power Ripple Analysis workflow only)

The *Measurement Report* tree includes the *Generate Report* module to specify a *Logo File* to be used in the generated report.

In the SLA and PBA workflows, the *Options* dialog box also has the *AMI Builder* tree. Here, in the *General* module, you can choose from the following two *AMI Builder Options*:

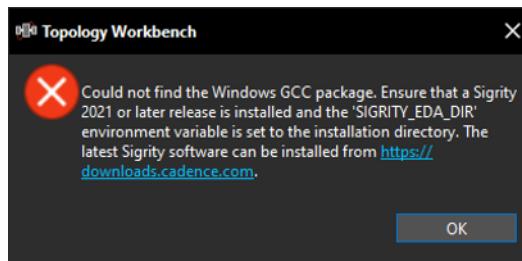
## Topology Workbench User Guide

### Preparing for a Simulation Run

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- **Use Microsoft Visual Studio:** If you select this option, specify the *Full path to MS Development Env. exe*, that is, the full path to the Visual Studio executable.
- **Use Windows GCC:** When you select this option for the first time and click *OK* or *Apply*, the .7z file is found from the Sigrity installation directory using the SIGRITY\_EDA\_DIR environment variable and unzipped in the \share\topxp\AMIBuilder\GNU folder (as populated automatically in the non-editable *Full path to Windows GCC package* box). This removes the external dependency that requires installation of a supported Visual Studio version.

If the Sigrity version does not contain the .7z file (which is under SIGRITY\_EDA\_DIR\tools\TPtools\GNU\x86\_64-8.1.0-release-posix-seh-rt\_v6-rev0.7z), an error message is displayed:



## General

The *General* module contains the following sections:

- [Multiple CPU Usage](#)
- [IBIS Simulation Option](#)
- [Grounding Option](#)
- [Third-Party Circuit Simulators](#)
- [Circuit Solver Options](#)

## Multiple CPU Usage

*Maximum CPU numbers for each circuit simulation*

Select the maximum number of CPUs that can be used for each circuit in a simulation run. The numbers displayed for choice depends on the number of CPUs available. By default, the value is set to 1.

**Note:** This setting does not apply to Spectre.

## IBIS Simulation Option

*Always use [Ramp] data when no VT curves are available or used*

Click this toggle button to always use the [Ramp] data in an IBIS model if no VT curves are available or used. If this option is not selected and VT curves are not available or used, SPDSIM calculates the timing information from a combination of C\_comp and VI curves. When this option is selected, it remains enforced for all subsequent Topology Workbench loads.

**Note:** This setting applies only to SPDSIM.

## Skin Resistance

Click this toggle button to add a resistance between the input and output pin of the package model. By default, the skin resistance is set to 100 Ohm. It gets added when *Pin RLC* is selected for package parasitics.

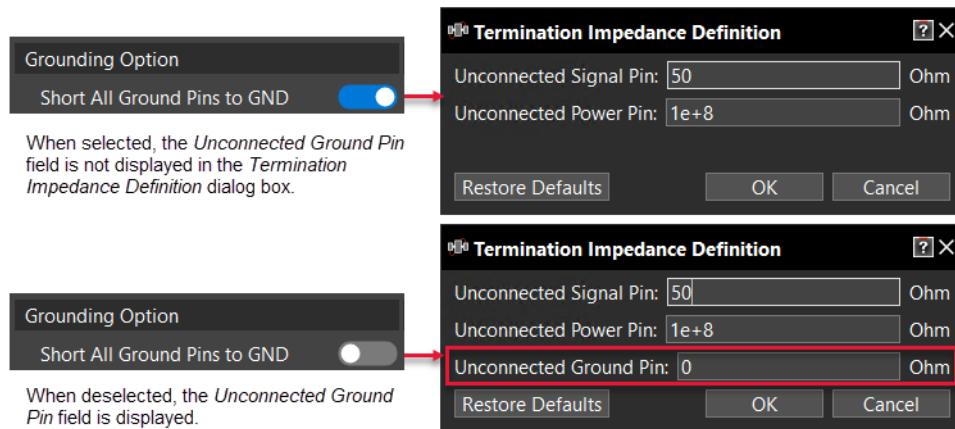
**Note:** With newer generation of IBIS models, you do not need to add *Skin Resistance*. This option has been inherited from SigXplorer for users who used PCB SI and want to correlate old low-frequency device models on SigXplorer and Topology Workbench. A resistor is added to the IBIS package model to account for some skin effect at low frequency.

## Grounding Option

### *Short All Ground Pins to GND*

Click this toggle button to short all ground pins to GND in the simulation. By default, this option is selected.

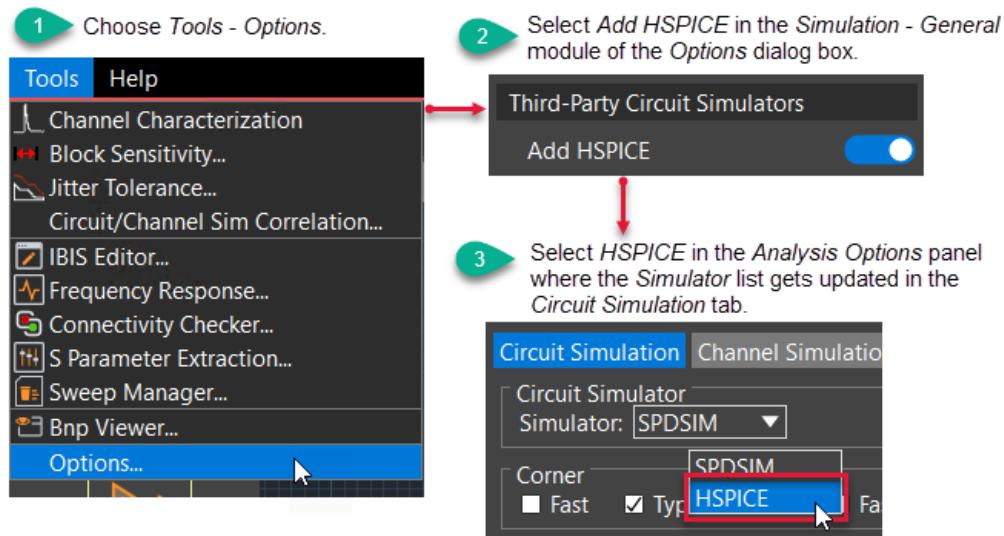
The selection or deselection of this option effects the display of the *Unconnected Ground Pin* field in the [Termination Impedance Definition](#) dialog box as shown below:



## Third-Party Circuit Simulators

### Add HSPICE

Click this toggle button to add HSPICE as an option in the *Simulator* list box on the *Circuit Simulation* tab of the *Analysis Options* panel.



## Circuit Solver Options

### Enabling additional performance improvements

Click this toggle button to enable additional SPDSIM-related performance improvements, such as, partition solver and multi-threading algorithm.

## Message

The *Message* module contains the Messages and Windows section.

### Messages and Windows

The following toggle buttons in this section control the display of the warning messages and graphs generated during simulations:

- *Show Warning Messages* (available in all workflows)

## Topology Workbench User Guide

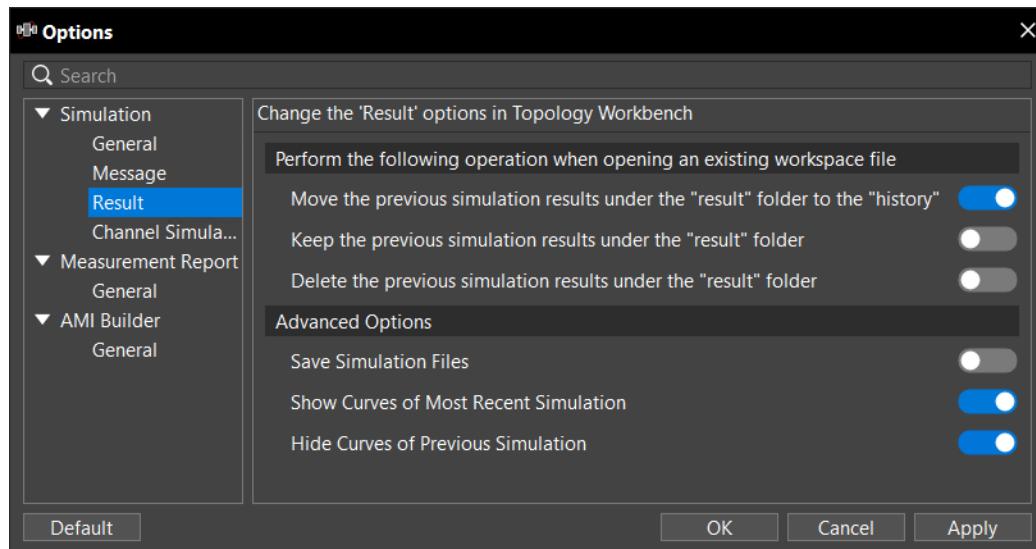
### Preparing for a Simulation Run

- *Show Real-Time Plots* (available in the Topology Explorer, SLA, and PBA workflows)
- *Run Golden Parser Check before Simulation* (available in the Topology Explorer, SLA, and PBA workflows)
- *Verify Timing Specs before Simulation* (available only in the PBA workflow)

By default, all warning messages are displayed. To hide the warning messages, click the *Show Warning Messages* toggle button and disable.

## Result

The *Result* module lets you specify what you want to do with the results of the previous simulations. Depending on your selections, the previous simulation results are saved in the `history` or `result` folder, or get deleted.



You also have the *Advanced Options* section where you can click the *Save Simulation File* toggle button if required. The *Show Curves of Most Recent Simulation* and *Hide Curves of Previous Simulation* toggle buttons are enabled by default.

## Channel Simulation

The *Channel Simulation* module is displayed only in the following scenarios:

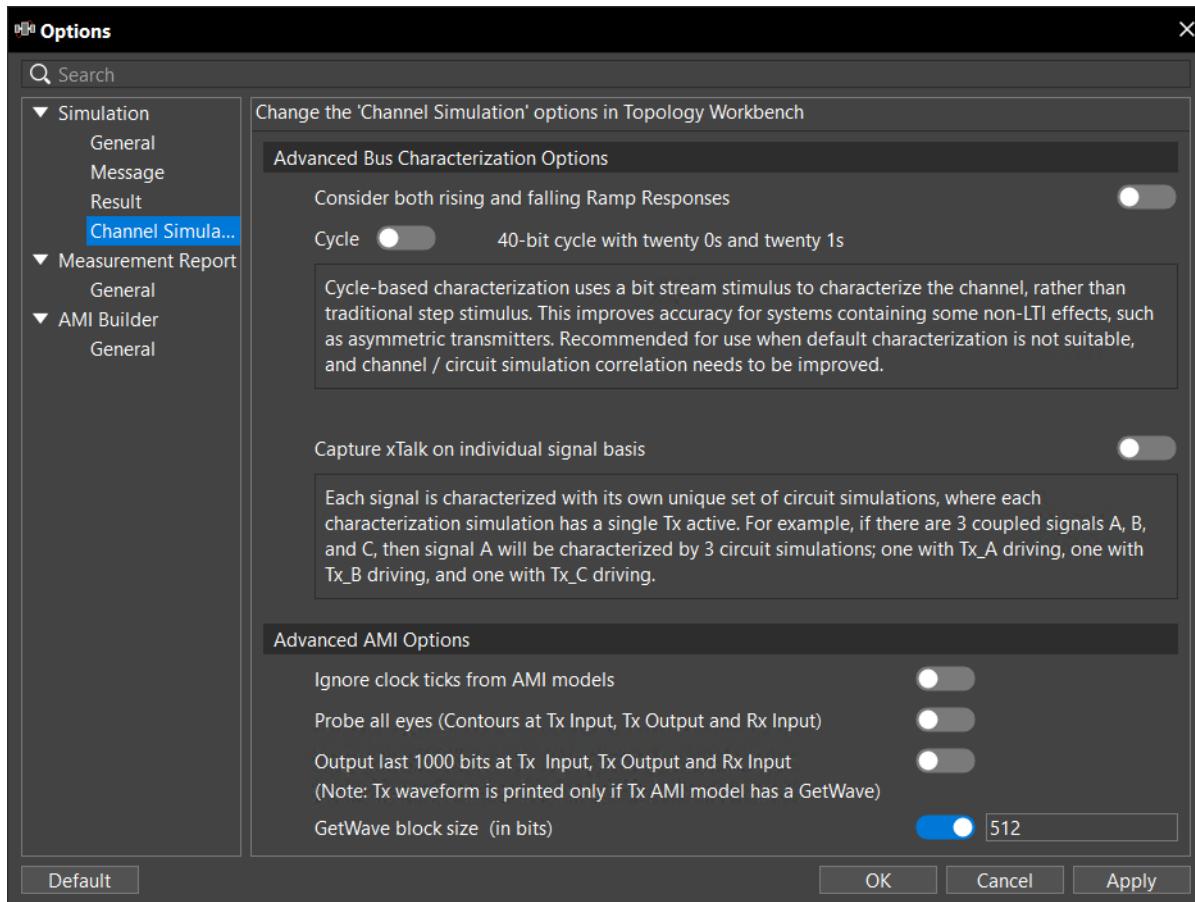
- SLA workflow where channel simulation is run by default
- PBA workflow only when the *Use Channel Simulator* check box is selected in the *Workflow* panel

# Topology Workbench User Guide

## Preparing for a Simulation Run

In both these scenarios, the *Channel Simulation* module provides the [Advanced AMI Options](#) section that lets you configure options for the AMI models.

In the PBA workflow, you additionally have the [Advanced Bus Characterization Options](#) section as shown below.



### Advanced AMI Options

Use this section to specify the simulation options for AMI models while using a channel

simulator for data bus write simulations.

*Ignore clock ticks from AMI models*

Click this toggle button to ignore the clock ticks from AMI models. With this option selected, instead of clock ticks from AMI models, clock ticks generated internally by Topology Workbench are used while sampling the waveforms.

Selecting this check box is the same as specifying the `ignoreamiclk` control in the *Channel Simulator Controls* section on the *Channel Simulation* tab of the *Analysis Options* panel.

**Note:** For this option to influence the simulation results, Rx should have an AMI model that has a `getwave` function with a CDR.

*Probe All Eyes (Contours at Tx Input, Tx Output, and Rx Input)*

By default, Topology Workbench displays the eye contour at Rx Output. Click this toggle button to print the eye contour at Tx Input, Tx Output, and Rx Input along with the default value.

Selecting this toggle button is the same as specifying the `probealleyes` control in the *Channel Simulator Controls* section on the *Channel Simulation* tab of the *Analysis Options* panel.

**Note:** The Tx curves are generated only if Tx has an AMI model with the `getwave` function.

*Output last 1000 bits at the Tx Input, Tx Output and Rx Input*

Click this toggle button to generate the time domain waveforms at the Tx Input, Tx Output, and Rx Input along with default value, Rx Output. The generated waveforms are not displayed by default. You need to manually load these in the Waveform Viewer window. The following files are generated:

- `waveform_rx_in.cur` – Curve file with time domain waveforms at Rx Input
- `waveform_tx.cur` – Curve file with time domain waveforms Tx Output
- `waveform_tx_in.cur` – Curve file with time domain waveforms Tx Input

Clicking this toggle button is the same as specifying the `wavecnt` control in the *Channel Simulator Controls* section on the *Channel Simulation* tab of the *Analysis Options* panel.

**Note:** The Tx curves are generated only if Tx has an AMI model with the `getwave` function.

### *GetWave block size (in bits)*

Click this toggle button to enter a specific size for the GetWave block to be used by the channel simulation engine. The maximum block size can be 512 bits.

Clicking this toggle button is the same as specifying the `useblkflt` control in the *Channel Simulator Controls* section on the *Channel Simulation* tab of the *Analysis Options* panel.

The channel simulation engine uses the specified number as a guidance and chooses a number that is best suited for an optimized simulation.

## **Advanced Bus Characterization Options**

The options set in this section effect the stimulus type in characterization when bus simulation is being run in channel mode, that is, when the *Use Channel Simulator* check box is selected in the *Workflow* panel of Parallel Bus Analysis workflow.

### *Consider both rising and falling Ramp Responses*

Click this toggle button if both rising and falling ramp responses should be considered during bus characterization. This option captures the circuit simulation behavior of drivers with asymmetric rising and falling edges.

### *Cycle*

Click this toggle button to run cycle-based characterization that uses a bit stream stimulus to characterize the channel, rather than traditional step stimulus.

**Note:** Selecting *Cycle* disables the *Launch Delay* and *Step Duration* text boxes in the *Characterization* section on the *Channel Simulation* tab of the *Analysis Options* panel.

### *Capture xTalk on individual signal basis*

Click this toggle button to ensure that each signal is characterized with its own unique set of circuit simulations, where each characterization simulation has a single Tx active.

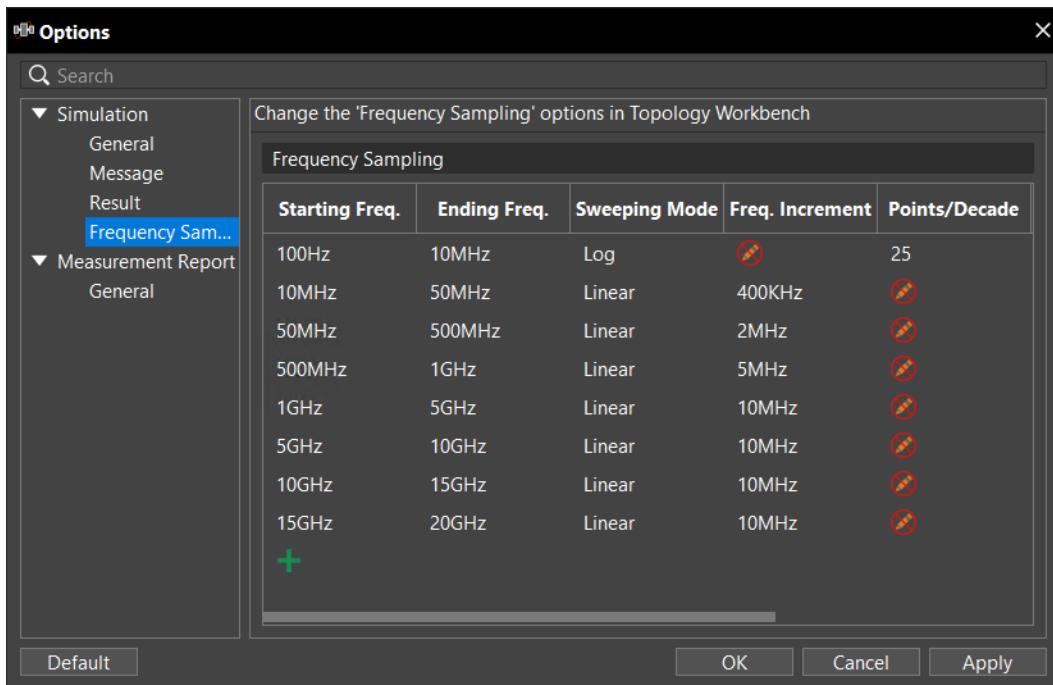
## **Frequency Sampling**

The *Frequency Sampling* module is displayed only in the SystemPI – PDN Impedance and Power Ripple Analysis workflow. The frequency sampling defined in this module contributes

## Topology Workbench User Guide

### Preparing for a Simulation Run

to the calculations and has direct impact on the optimization of results. It is populated with sample starting and ending frequency, sweeping mode, frequency of increment, and points/decade (that is, the frequency scale) values that are based on extensive studies.



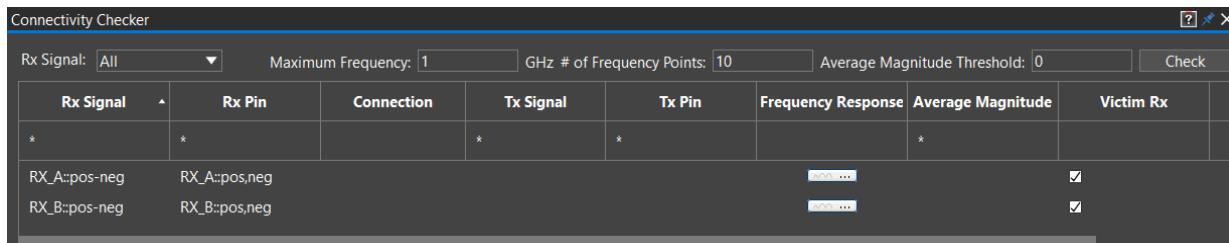
## Checking Connectivity Between Blocks and Signals

In addition to setting the simulation options, before starting the simulation, it is important to check whether the blocks and signals in the topology are connected appropriately.

To verify the connectivity of the receiver block with its intended transmitter:

1. Click *Check Connectivity* in the *Simulation Setup* schema of the Workflow Panel. This opens the *Connectivity Checker* panel as shown below.

**Note:** Alternatively, choose *Tools – Connectivity Checker* from the Menu Bar.



## Topology Workbench User Guide

### Preparing for a Simulation Run

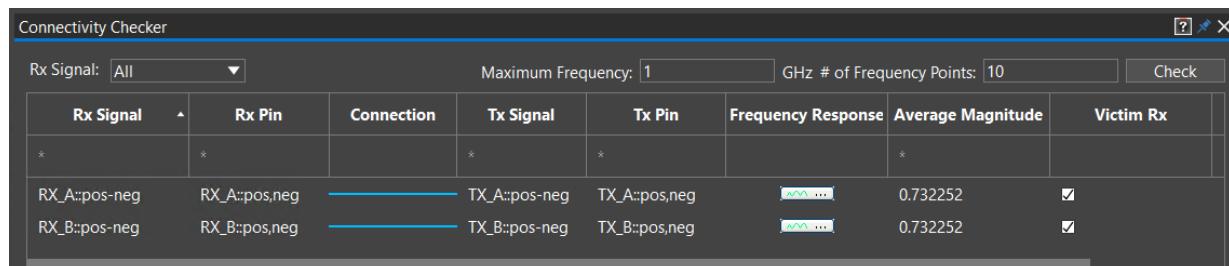
2. Select the *Rx Signal* for which the connectivity needs to be checked. By default, *All* is selected.

You can select a specific *Rx Signal* from the list. When you do this, the table within the *Connectivity Checker* panel shows rows of signals/pins associated with the selected *Rx Signal*.

3. Specify the *Maximum Frequency* in GHz.
4. Specify the *# of Frequency Points* for which the connectivity should be checked.
5. Specify the *Average Magnitude Threshold*.
6. Click *Check*.

The process starts and the progress is shown in the *Status Bar*. On completion of the checks, the button in each cell under the *Frequency Response* column is enabled.

When the *Rx Signal* is set to *All*, the *Connection*, *Tx Signal*, *Tx Pin*, and *Average Magnitude* columns are blank. These columns are populated with the corresponding information after you run the checker.



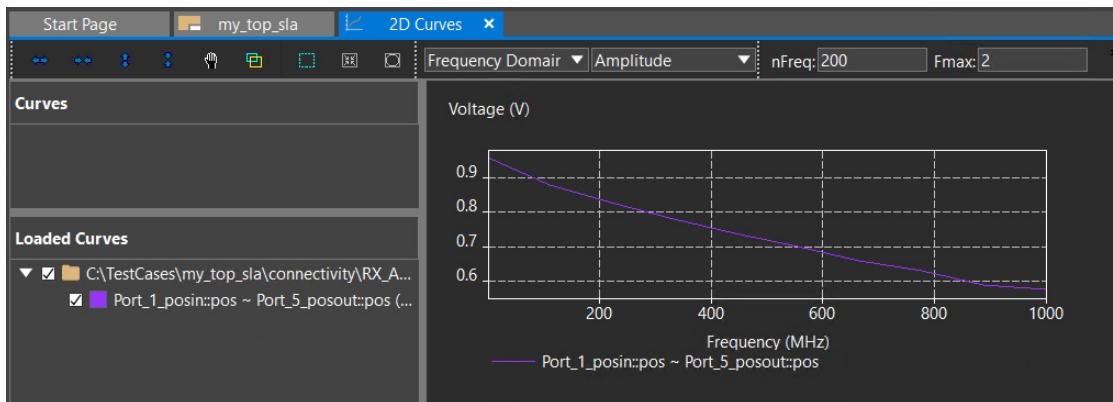
Connectivity Checker								
Rx Signal:	All	Maximum Frequency:	1	GHz	# of Frequency Points:	10	Check	
Rx Signal	Rx Pin	Connection	Tx Signal	Tx Pin	Frequency Response	Average Magnitude	Victim Rx	
*	*		*	*		*		
RX_A::pos-neg	RX_A::pos,neg	TX_A::pos-neg	TX_A::pos,neg	TX_A::pos-neg	...	0.732252	<input checked="" type="checkbox"/>	
RX_B::pos-neg	RX_B::pos,neg	TX_B::pos-neg	TX_B::pos,neg	TX_B::pos,neg	...	0.732252	<input checked="" type="checkbox"/>	

When a specific *Rx Signal* is selected, the *Tx Signal* and *Tx Pin* columns are populated, but the *Coupling Factor (%)* column is blank. After the completion of the checks, the *Coupling Factor (%)* column also shows the relevant calculated information.

## Topology Workbench User Guide

### Preparing for a Simulation Run

7. Click the required button from the *Frequency Response* column. The *2D Curves* tab opens with the extracted 2D Curve (Frequency Domain).



After the checks, the *Connection* column, which is displayed when the *Rx Signal* is set to *All*, shows a blue line indicating a successful connection. When a blue line is right-clicked, the shortcut menu provides the following two options:

- *Extract ECSet*

Opens the *Constraint Topology* of the chosen connection in a new tab within Topology Workbench, as shown below:

- *Circuit/Channel Sim Correlation*

Runs channel characterization and provides an option to view the simulation correlation between the circuit and channel simulation results.

**Note:** This option is available in PBA workflow when a channel simulator is used and in SLA workflow.

## Analyzing the Frequency Response

Topology Workbench lets you calculate the frequency response at any time in all workflows.

1. Select *Tools – Frequency Response*.

## Topology Workbench User Guide

### Preparing for a Simulation Run

The *Frequency Response* panel opens with two tabs—*Single-ended Mode* and *Differential Mode*. These tabs provide detailed information about the various controller to signal or probe mappings that exist in the topology.

**A**

Rx Signal / Probe	Block	Connection	Positive Cknode	Negative Cknode	Frequency Response
pos-gnd	RX_LOWER	rx_pkg	pos	ngnd	[three-dot]
pos-gnd	RX_PRIMARY	rx_pkg	pos	ngnd	[three-dot]
pos-gnd	RX_UPPER	rx_pkg	pos	ngnd	[three-dot]
neg-gnd	RX_LOWER	rx_pkg	neg	ngnd	[three-dot]
neg-gnd	RX_PRIMARY	rx_pkg	neg	ngnd	[three-dot]
neg-gnd	RX_UPPER	rx_pkg	neg	ngnd	[three-dot]

**B**

Rx Signal / Probe	Block	Connection	Positive Cknode	Negative Cknode	Frequency Response
pos-neg	RX_LOWER	rx_pkg	pos	neg	[three-dot]
pos-neg	RX_PRIMARY	rx_pkg	pos	neg	[three-dot]
pos-neg	RX_UPPER	rx_pkg	pos	neg	[three-dot]

Enabled button in the Frequency Response column after Analyze is clicked.

2. Define the *Maximum Frequency* and *# of Frequency Points* in the designated fields.  
By default, *Maximum Frequency* is set to 1Ghz and *# of Frequency Points* is set to 128.
3. Select from the *Tx Signal* list, the controller for which frequency response needs to be analyzed. This step needs to be done on both the tabs.
4. Click the *Analyze* button.

When the frequency response simulation run is completed, the SSIViewer window opens with *Frequency Response* curves for all signal nets in the topology.

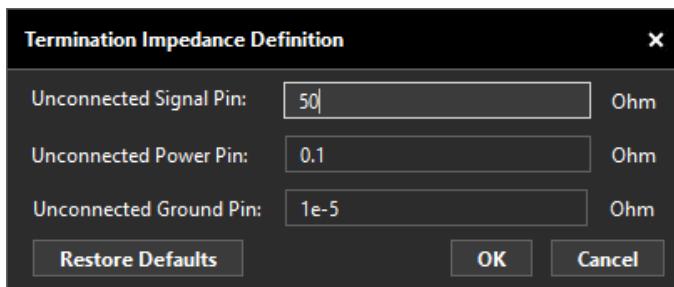
In addition, in the *Frequency Response* panel, the buttons displayed in each row under the *Frequency Response* column are enabled. Clicking a button from this column opens the corresponding frequency domain curve in the SSIViewer window.

## Terminating Unconnected Pins

If you have unconnected pins in the topology, terminate their impedance before running the simulation. To do so:

1. Click *Terminate Unconnected Pins* from the *Workflow* panel or the *Setup* menu.

The *Termination Impedance Definition* dialog box appears.



2. Specify the termination impedance values that should be applied to an *Unconnected Signal Pin*, *Unconnected Power Pin*, and *Unconnected Ground Pin*.

**Note:** The *Unconnected Ground Pin* field is displayed only when the *Short All Ground Pins to GND* option is deselected in the Grounding Option section of the *Options* dialog box.

3. Click *OK* to apply the changes. The impedance of the unconnected pins is terminated based on the specified criteria.

**Note:** Click the *Restore Defaults* button if customized impedance values should be reset to the default values as per Topology Workbench.

## Automatic Termination Rules for Unconnected Nodes

For the automatic termination of unconnected nodes, the following rules apply in the order of priority:

- When the *Short All Ground Pins to GND* option is selected in the Grounding Option section of the *Options* dialog box, set 'gnd' for the unconnected ground node.
- When the termination impedance in the *Unconnected Ground Pins* box of the *Termination Impedance Definition* dialog box is set as following:
  - *inf*: Do not auto terminate.
  - *<= 1e-5*: Automatically short to reference ground.

## Topology Workbench User Guide

### Preparing for a Simulation Run

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- >  $1e-5$ : Automatically terminate to reference ground.

The priority of the reference ground is based on the following criteria:

- Connected ground node in the same MCP
- Connected ground node in the same block
- Ground node is negative port node
- Global gnd
- For the transmitter (Tx) and receiver (Rx) blocks:
  - Do not automatically terminate unconnected power and signal nodes, and in/rxnode.
  - Automatically terminate the unconnected ground node.
- For a single pin, automatically terminate unconnected signal, power, and ground nodes.
- For multi-pin connectivity with:
  - LEVEL-1 SPICE block
    - Do not automatically terminate unconnected power and signal nodes.
    - Automatically terminate unconnected ground node.
  - Interconnect block, automatically terminate unconnected signal, power, and ground nodes.

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# Running a Simulation and Analyzing the Results

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After a successful simulation run, the *2D Curves* tab opens in the main Topology Workbench window. This tab shows the waveform results and gives option to generate measurement reports. Other tabs such as *Eye Density*, *Channel Report*, and *Measurement Report* are also displayed depending on the workflow.

After viewing the simulation results, you can modify the circuit topology and simulation parameters, and then re-simulate to examine the effects of your changes. Repeat this process until the circuit meets your requirements.

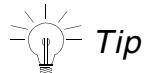
### ***Related Topics***

- [Running the Simulation](#)
- [Viewing Simulation Results](#)
- [Browsing Simulation Results](#)
- [Correlating Circuit and Channel Simulations](#)

## Running the Simulation

To start the simulation after you have set up the simulation options, checked the connectivity between the blocks and signals, and terminated the unconnected pins:

- Click the corresponding option available in the *Simulation* schema of the [Workflow Panel](#).



*Tip*

Alternatively, click in the [Toolbar](#) to run the simulation.

In each supported workflow, the option to start the simulation is named differently in the *Workflow* panel – *Simulation* schema as following:

- In Topology Explorer, select **Start Transient Analysis** from *Workflow* panel – *Simulation* schema.
- In SystemSI – Serial Link Analysis (SLA), click **Start Channel Simulation** from *Workflow* panel – *Simulation* schema.
- In SystemSI – Parallel Bus Analysis (SLA), click **Start Bus Analysis** from *Workflow* panel – *Simulation* schema.
- In SystemPI – DC IR Drop Analysis, click **Start DC IR Drop Analysis** from *Workflow* panel – *Simulation* schema.
- In SystemPI – PDN Impedance and Power Ripple Analysis, click **Start Impedance Analysis** or **Start Power Ripple Analysis** from *Workflow* panel – *Simulation* schema.

 **Important**

To keep a control over each simulation run, you can select *Setup – Pause before Simulation* from the menu bar. This ensures that a prompt is displayed seeking your confirmation before a requested simulation is run. For example, after completion of the channel simulation run for one corner type, your confirmation will be sought to start the next one for the second corner type.

The Status Bar gives you a run-time glimpse of the type of processing that Topology Workbench is running on the topology, such as, *Check Connectivity*, *Circuit Simulation*, *Channel Characterization*, and *Channel Simulation*.

When the process finishes, the *SSIViewer* window opens with the relevant waveform results that are generated based on the *Corner* options selected in the Circuit Simulation tab of the *Analysis Options* panel.

In addition, the result is saved to Simulation Results Directory within your current workspace, that is, the directory you specified in the *Topology Path* field of the *Create New Topology* dialog box.

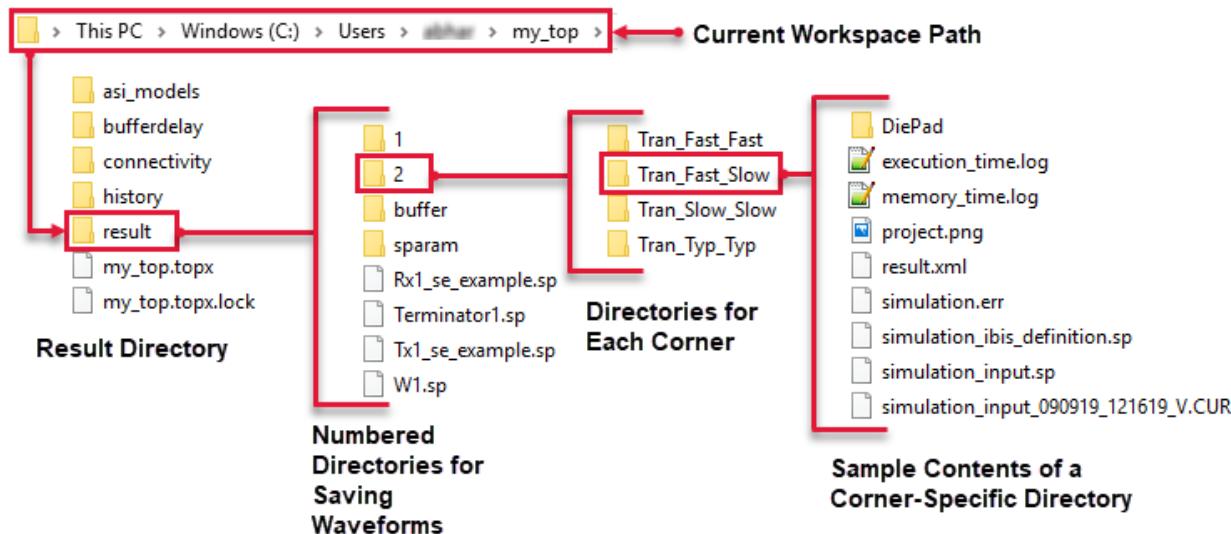
### **Simulation Results Directory**

Each simulation creates a unique directory (1, 2, 3 ...) where all the related waveform files are saved. The default destination of these numbered directories is

## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

<currentWorkspacePath>\result. The image below illustrates the directory structure that gets created after the simulation run:



The directories created for each corner type selected in the *Analysis Options* panel are named in the following format:

<SimulationType>\_<CornerType1>\_<CornerType2>. For example:

- For transient analysis in the Topology Explorer workflow, the directories are named as Tran\_Fast\_Fast, Tran\_Fast\_Slow, Tran\_Slow\_Fast, Tran\_Slow\_Slow, or Tran\_Typ\_Typ.
- For channel analysis in the SLA workflow, the directories are named as Chan\_Fast\_Fast, Chan\_Fast\_Slow, Chan\_Slow\_Fast, Chan\_Slow\_Slow, or Chan\_Typ\_Typ.
- For parallel bus analysis in the PBA workflow, the directories are named as Data\_Write\_Typ\_Typ, Data\_Write\_Fast\_Fast, Data\_Write\_Slow\_Slow, or Data\_Write\_Slow\_Fast.

By default, the `result` directory is moved to the `history` folder when an existing project is opened. To change this behavior, choose a different option in the Result module of the dialog box displayed when you select *Tools – Options* from the menu bar.

#### Related Topics

- [Configuring Simulation Options for Topology Explorer](#)
- [Configuring Simulation Options for Serial Link Analysis](#)

- [Configuring Simulation Options for Parallel Bus Analysis](#)
- [Checking Connectivity Between Blocks and Signals](#)
- [Terminating Unconnected Pins](#)
- [Monitoring a Simulation Run in Topology Explorer](#)
- [Monitoring a Simulation Run in Serial Link Analysis](#)
- [Monitoring a Simulation Run in Parallel Bus Analysis](#)
- [Viewing Simulation Results](#)
- [Browsing Simulation Results](#)
- [Correlating Circuit and Channel Simulations](#)

## Monitoring a Simulation Run in Topology Explorer

When *Start Transient Analysis* is clicked, Topology Workbench runs the simulation in the following sequence:

1. *Circuit Simulation*
2. *Buffer Delay Simulation*

**Note:** If the connectivity between the signals was not checked before the transient simulation was started, Topology Workbench first runs *Check Connectivity* and then the different types of simulations listed above. See also [Checking Connectivity Between Blocks and Signals](#).

## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

After the completion of the simulation run, the *2D Curves* tab opens with the waveform results as shown below:



For more information about the displayed results, see [Viewing Simulation Results](#).

## Monitoring a Simulation Run in Serial Link Analysis

When *Start Channel Analysis* is clicked, Topology Workbench runs the simulation in the following sequence:

1. *Channel Characterization*
2. *Channel Simulation*

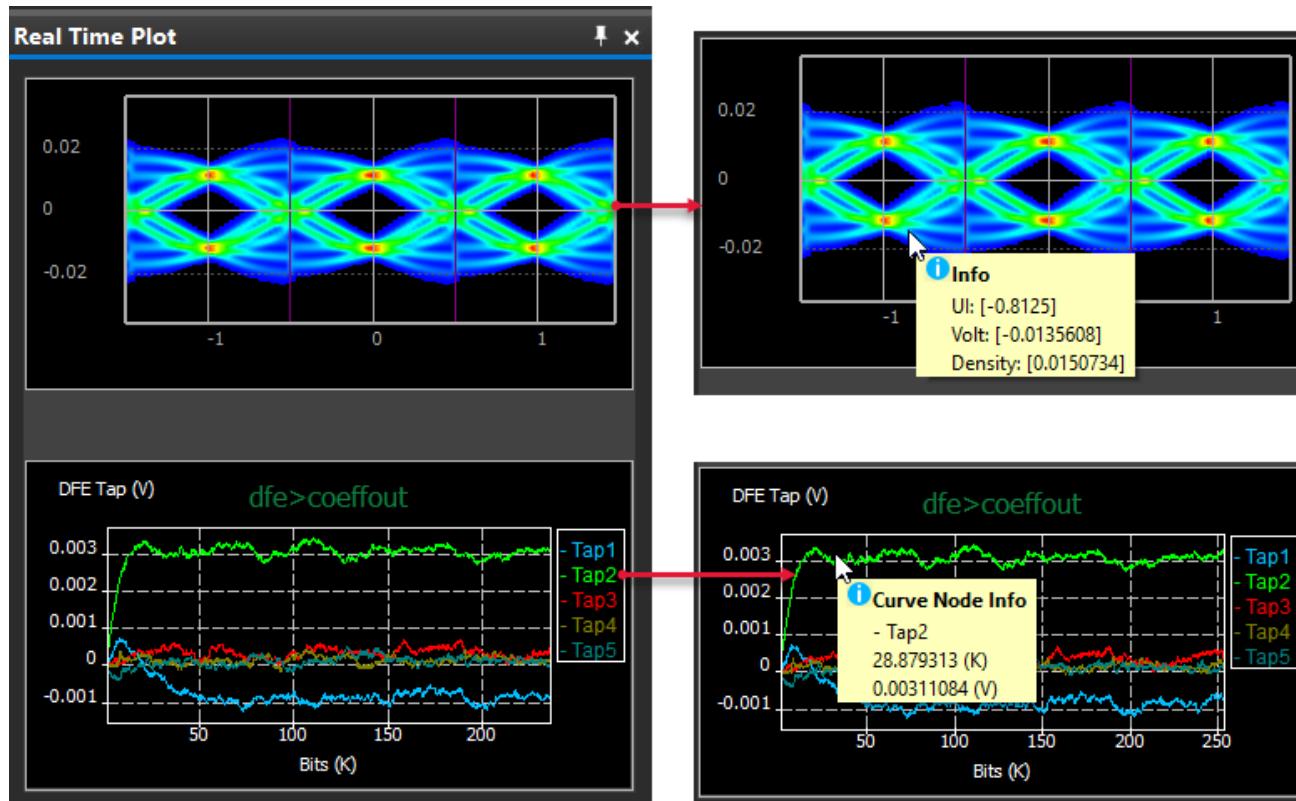
**Note:** If the connectivity between the signals was not checked before the transient simulation was started, Topology Workbench first runs *Check Connectivity* and then the different types of simulations listed above. See also [Checking Connectivity Between Blocks and Signals](#).

In Serial Link Analysis workflow, as the simulation run progresses, the *Real Time Plot* panel opens. This panel shows live plotting of the simulation results in formats, such as, eye density diagram, decision feedback equalizer (DFE) coefficients, DFE center samples, analog gain control (AGC), and continuous time equalizer (CTE) waveforms. When you place the pointer

## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

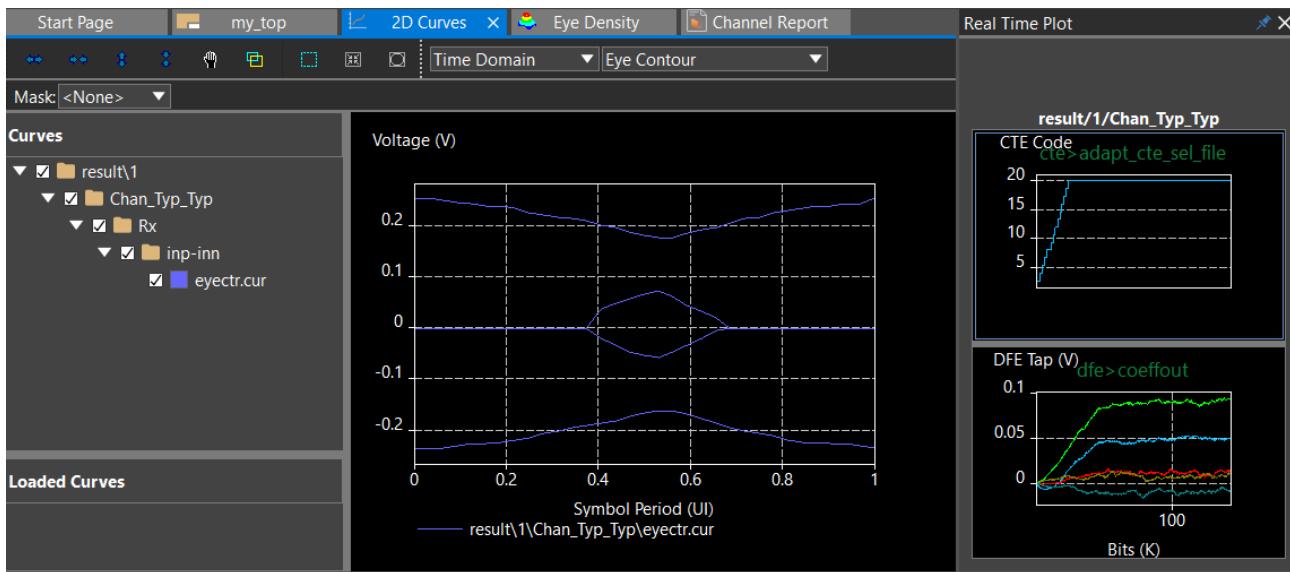
on a data point or a curve node in any of the displayed plots, an information balloon is displayed giving the related details as shown below:



## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

After the completion of the simulation run, the *2D Curves*, *Eye Density*, and *Channel Report* tabs open displaying the waveform results. The *Eye Density* tab lets you view waveforms in the *3D Eye Density* and *3D Bathtub* formats.



For more information about the results displayed in the opened tabs, see [Viewing Simulation Results](#).

#### **Additional Points to Note**

- The real-time plotting feature is not available when you choose the *Statistical* eye distribution method in the [Channel Simulation – Parallel Bus Analysis](#) tab of the *Analysis Options* panel. For more information, see [Performing Statistical Analysis](#).
- The Real Time Plot panel shows the eye density diagram for all time domain-based channel simulations. However, the Time Domain Adaptation plot is displayed **only** when the following conditions are met:
  - The Rx AMI models are generated using the AMI Builder. For information, see [Using the AMI Builder](#).
  - The various modules within the Rx AMI model have the `adapt_on` parameter set to 1 to indicate that adaptation is enabled.
- If you have any new channels in the topology, ensure that they are characterized before running a channel simulation. For this, you can use the *Run & Review Characterization* option from the *Simulation* schema available in the *Workflow* panel. All the characterization information for a channel is stored in the directory you specified in the *Topology Path* field of the *Create New Topology* dialog box.

Characterization of a channel involves finding the step or impulse response. It is recommended that you run HSPICE or SPDSIM simulation to characterize the channels.

To review a standard stimulus sub-circuit that Topology Workbench uses to generate the step response, access the file named, `standard_step.sp`, from the following location:

`<INSTALL_DIR>\share\topxp\standard_step.sp`

 **Important**

Do not edit the `standard_step.sp` file unless you are an advanced user and want to set up a different stimulus.

- If you rerun the simulation, Topology Workbench checks whether the channel has been characterized before. If yes, then Topology Workbench skips the characterization and starts the channel simulation directly.
- The waveforms displayed in the *2D Curves* tab are the most useful ones. The eye contour and bathtubs are good measures of the quality of any channel.
- After the simulation results have been generated, you can *Correlate Circuit/Channel Sims*. For more information, see [Correlating Circuit and Channel Simulations](#).

## Monitoring a Simulation Run in Parallel Bus Analysis

When *Start Bus Analysis* is clicked, Topology Workbench runs the simulation in the following sequence:

- *Bus Simulation*
- *Buffer Delay Simulation*

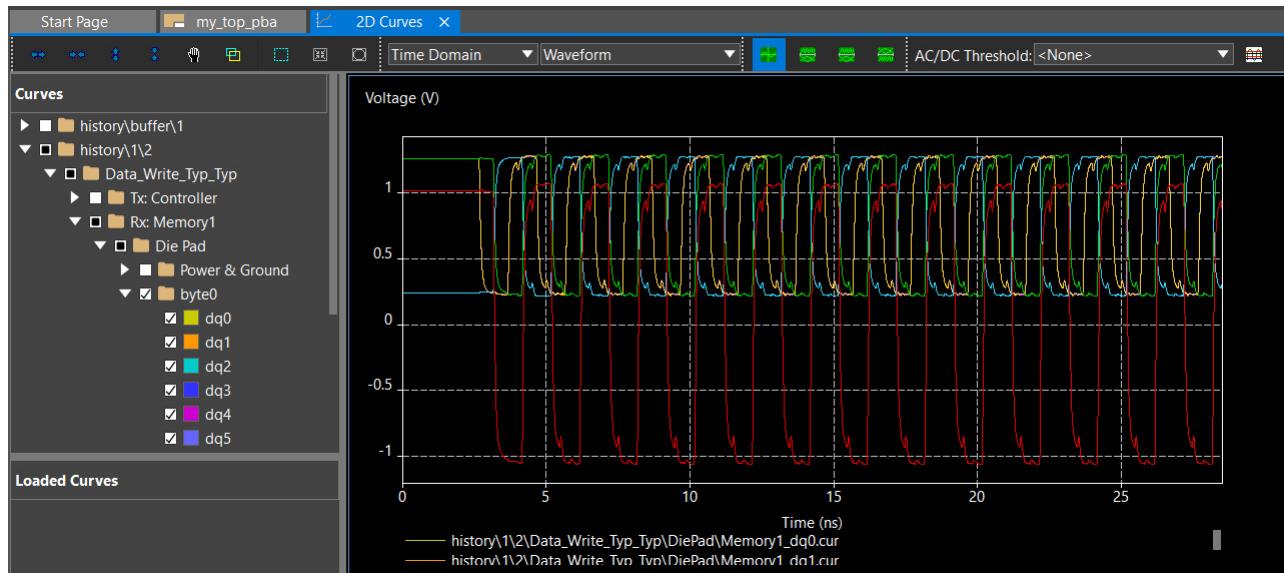
**Note:** If the connectivity between the signals was not checked before the transient simulation was started, Topology Workbench first runs *Check Connectivity* and then the different types of simulations listed above. See also [Checking Connectivity Between Blocks and Signals](#)

Before starting the simulation in the PBA workflow, ensure that the *Min Transmit Setup* and *Min Transmit Hold* specifications have been specified for a bus in the *Timing Budget* panel. These specifications are required for automatically calculating the *Worst Case Stimulus Offset* for a Controller Bus Group. For more information about how to set these using the *Set Timing Budget* option given in the *Simulation Setup* schema of the *Workflow* panel, see [Setting Up Timing Specifications](#).

## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

After the completion of the simulation run that does not use a channel simulator, the *2D Curves* tab, as shown below, opens with the waveform results plotted for *Time Domain*, by default. You can choose to view the waveform results for *Frequency Domain*.



If you choose to *Use Channel Simulator*, the following two options are also enabled in the *Simulation* schema:

■ *Correlate Circuit/Channel Sims*

For more information, see [Correlating Circuit and Channel Simulations](#).

■ *Run & Review Characterization*

For more information, see [Running and Reviewing Characterization](#).

In this scenario, Topology Workbench runs the following processes while simulating the topology:

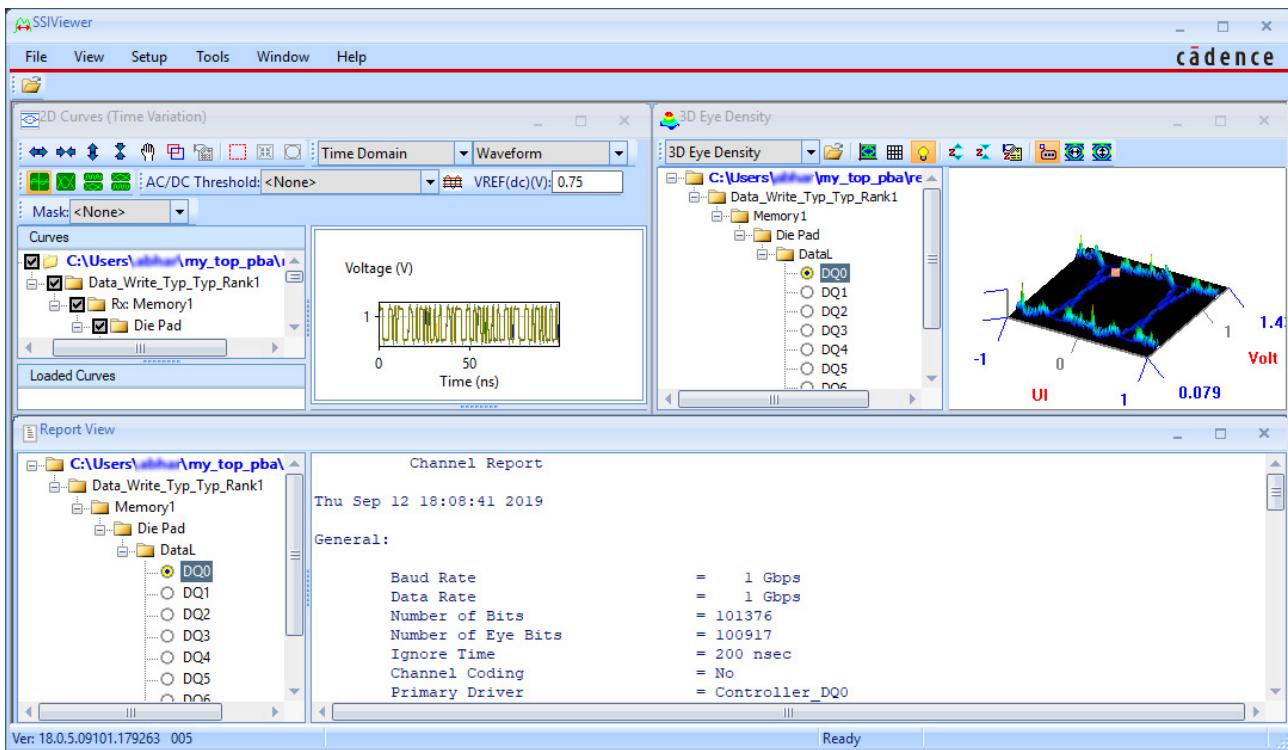
1. *Channel Characterization*

2. *Channel Simulation*

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## Running a Simulation and Analyzing the Results

The results can be viewed in the *2D Curves*, *Eye Density*, and *Channel Report* tabs as shown below.



**Note:** If the simulation is rerun, checks are run in the Topology Workbench to confirm whether the channel was characterized earlier. If yes, then characterization is skipped and channel simulation starts directly.

## Viewing Simulation Results

After the completion of the simulation run, tabs of simulation results open within Topology Workbench window. Depending on the workflow run and the properties set for various blocks in the simulated topology, the following tabs are displayed:

- [2D Curves](#)
- [3D Plots in SSIViewer](#)
- [Report View](#)

### 2D Curves

The 2D Curves tab displays the transient and channel simulation data results from Topology Workbench. It also lets you:

- Access post-processing tools for data analysis and viewing.
- Use the dedicated 2D Curves window toolbar.
- Use shortcut menus in each pane to access the functionality for the 2D Curves window.
- View previously simulated data (saved as .cur files).
- View a 2D animation of the potential difference between any two circuit nodes or any adjacent package planes.
- View currents and voltages in both [Time Domain](#) and [Frequency Domain](#).
- View computed results (such as impedance and transfer functions) in frequency domain.
- View statistical distribution function of the power and ground noise voltages.

The 2D Curves tab consists of:

Component	Description
<b>Toolbar</b>	<p>Displays an array of options that allow actions such as:</p> <ul style="list-style-type: none"><li>■ Panning and zooming of the plot – </li><li>■ Opening the <i>Curve Navigator</i> dialog box to navigate and view the plots based on the specified criteria – </li><li>■ Choosing the type of variation to plot, such as, <u>Time Domain</u> and <u>Frequency Domain</u></li><li>■ Choosing the type of plot, such as, <i>Waveform</i>, <i>Eye Contour</i>, <i>Amplitude</i>, <i>Real</i>, <i>Imaginary</i>, <i>Phase</i>, and so on</li><li>■ Selecting area, zooming out, and fitting back to original state – </li><li>■ Configuring the plots for detailed analysis. Options such as following are displayed depending on the selected plot type: <i>Mask</i>, <i>Type</i>, <i>VREF</i>, <i>AC/DC Threshold</i>, <i>Eye Measurement</i>, <i>Eye Aperture</i>, <i>Trigger Period</i>, <i>Range</i>, <i>Offset</i>, <i># of Period</i>, and so on.</li></ul> <p><b>Note:</b> For any given eye diagram, you can use existing masks or create a new mask to help determine if the waveforms satisfy the necessary requirements.</p>

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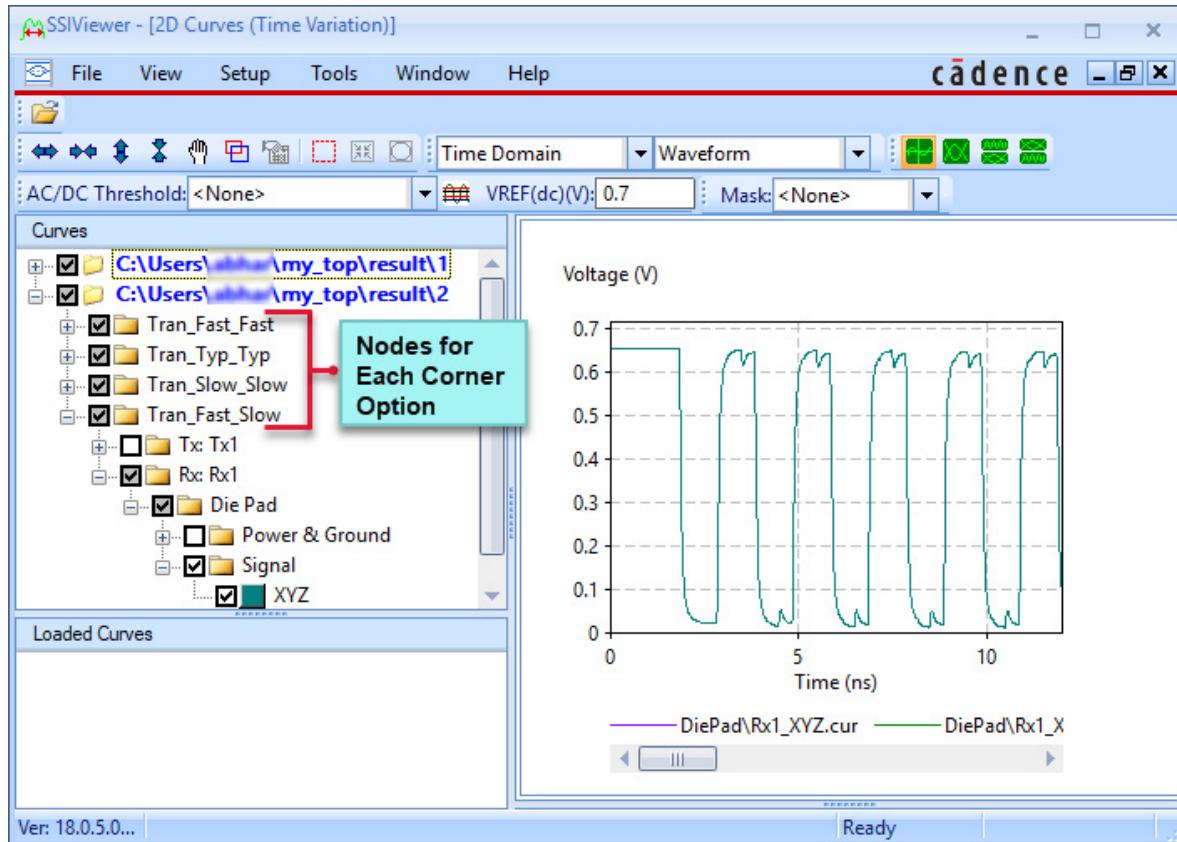
### Running a Simulation and Analyzing the Results

Component	Description
<b>Curves Pane</b>	<p>Displays a hierarchical tree of each signal in the simulated topology to enable selective viewing of the related curves data.</p> <p>Data for each signal can be selected and viewed individually as a raw waveform or an eye diagram.</p> <p> <i>Tip</i></p> <p>When multiple simulations are run, the data curves add up quickly to the plots and the <i>Curves</i> pane. You can then:</p> <ol style="list-style-type: none"><li>(1) Use the + and - buttons to expand and collapse the signals list.</li><li>(2) Right-click and choose <i>Hide All Curves</i> from the shortcut menu. Then select the check boxes adjacent to only those components for which you want to study the results.</li><li>(3) Close the <i>2D Curve</i> window to clear the data and start over in a new <i>2D Curve</i> window if needed.</li></ol> <p>The shortcut menu displayed on right-click in this pane lets you perform advanced actions such as <i>Generate Report</i> (in Topology Explorer and PBA workflows), view <i>Result Browser</i>, <i>Show/Hide All Curves</i>, <i>Unload</i> a result hierarchy, <i>Load Curve Pattern</i>, <i>Save Current Pattern</i>, and so on.</p>
<b>Plot Area</b>	<p>Displays the graphical representation of the simulation data.</p> <p>You can pan and zoom the plot area. For panning, first select the hand icon in the toolbar, then point anywhere within the plot area (notice that the cursor's shape changes to a hand), and now drag the cursor around to move the plot for reviewing the required data points. For zooming, use the mouse scroll wheel, which enlarges and decreases the plot size.</p> <p>When you place the pointer on a data point or a curve node in any of the displayed plots, an information balloon is displayed giving the related details.</p> <p>See also <a href="#">Shortcut Menu Displayed in Plot Area</a>.</p>

## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

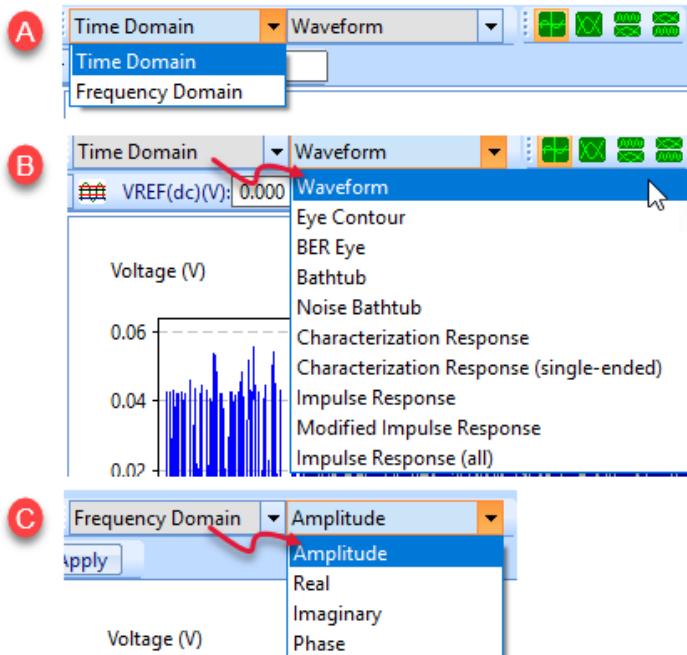
**Note:** If you selected multiple *Corner* options in the Circuit Simulation tab of the *Analysis Options* panel, nodes for each corner are added to the tree hierarchy displayed in the *Curves* pane of the SSIViewer window as shown below:



# Topology Workbench User Guide

## Running a Simulation and Analyzing the Results

The 2D Curves tab displays the *Time Domain* and *Frequency Domain* variation data.



For Time Domain, the following types of plots are generated:

■ <i>Waveform</i>	■ <i>Eye Contour</i>
■ <i>BER Eye</i>	■ <i>Bathtub</i>
■ <i>Noise Bathtub</i>	■ <i>Characterization Response</i>
■ <i>Characterization Response (single-ended)</i>	■ <i>Impulse Response</i>
■ <i>Modified Impulse Response</i>	■ <i>Impulse Response (all)</i>

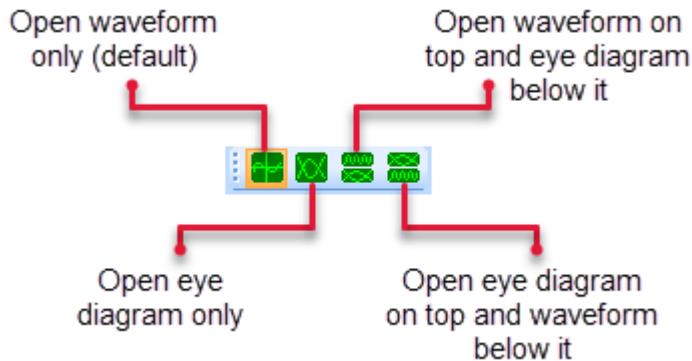
**Note:** For PAM3 and PAM4 signaling, all the eye contours and bathtubs are available for you to select and view. Their results are also included in SLA reports. For Topology Explorer workflow, only *Time Domain – Waveform* plots are generated.

For Frequency Domain, the following types of plots are generated:

■ <i>Amplitude</i>	■ <i>Imaginary</i>
■ <i>Real</i>	■ <i>Phase</i>

## Time Domain

When *Time Domain – Waveform* is selected in the *2D Curves* sub-window, the following toolbar options are also displayed:



Using these toolbar options, you can choose to plot the simulation data as a waveform or an eye density diagram. There are also options to compare both waveform and eye density diagram plots together while switching the placement of the two plots as per your preference.

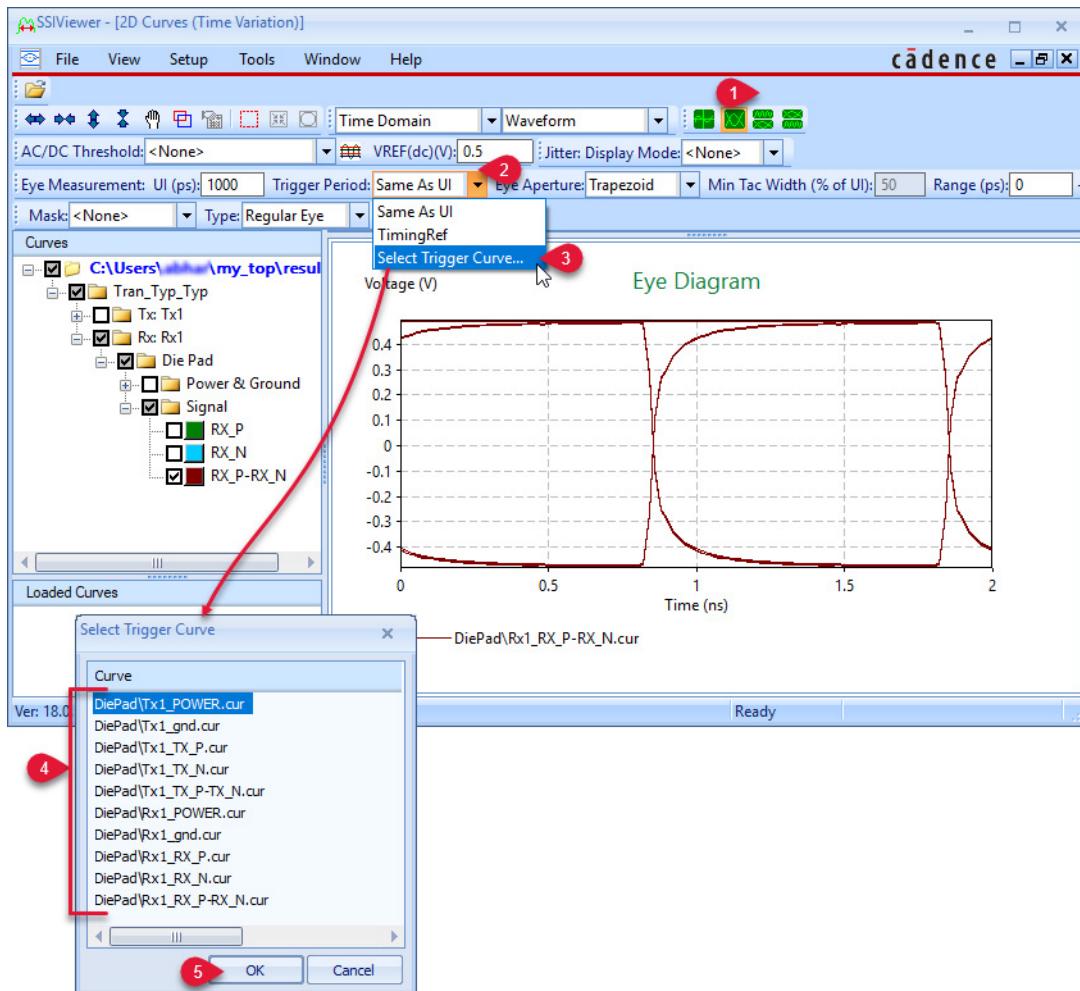
When you choose to display an eye density diagram, the toolbar provides additional measurement and data processing functions. You can specify an Eye Contour or Eye Density plot, overlay an *Eye Mask*, or measure *Eye Opening* including *Trigger Period*, *Eye Aperture*, *Min Tac Width*, *Offset* and *Range*. Jitter values can also be viewed and *Display Mode* be set to *<none>*, *Histogram*, or *Density*.

When an external clock is used as the trigger for plotting an eye density diagram, you can select the *Select Trigger Curve...* option from the *Trigger Period* drop-down list as illustrated in the figure below. This opens the *Select Trigger Curve* dialog box with a list of

# Topology Workbench User Guide

## Running a Simulation and Analyzing the Results

generated curves. Select the required curve from the list and click *OK* to enable it as a trigger curve.



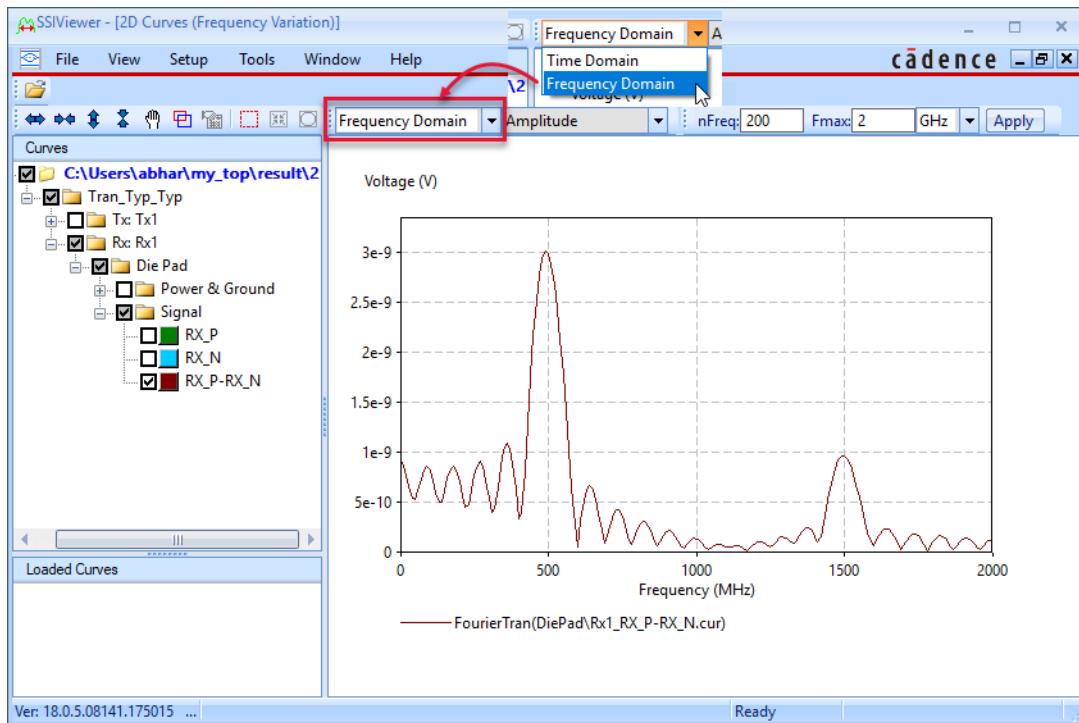
## Frequency Domain

Selecting *Frequency Domain* from the toolbar of the 2D curves window, as shown below, utilizes a Fourier transform function to convert 2D plots of simulation data from time domain to frequency domain. In frequency domain, the variable values are captured as complex

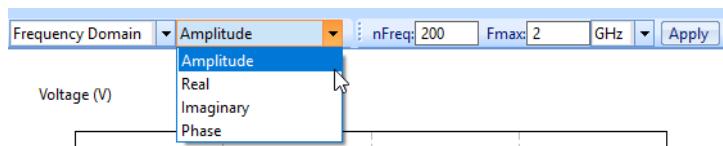
## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

numbers. Each complex number contains a real part and an imaginary part. It can also be presented by its amplitude and phase.



By default, *Amplitude* spectrum is displayed. To view other parts of the spectrum, select *Real*, *Imaginary*, or *Phase* from the drop-down list, as shown below:

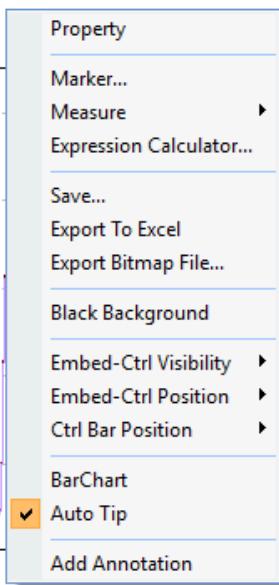


You can modify the spectrum for Fourier transformation by specifying:

- *nFreq* – Enter a value for the number of sample frequency points between 0 to *Fmax*.
- *Fmax* – Enter a value for the upper limit of frequency when making a Fourier transformation.

### Shortcut Menu Displayed in Plot Area

- Right-click the plot area of the 2D Curve window to display the following shortcut menu:



You can perform the following operations in this shortcut menu.

Operations	Description
<i>Measure</i>	Toggle the horizontal and vertical measure lines.
<i>Marker</i>	Toggle the horizontal and vertical marker lines.
<i>Expression Calculator</i>	Setup and calculation the expression.
<i>Save</i>	Save the curve.
<i>Export To Excel</i>	Export the curve to Excel.
<i>Export to Bitmap File</i>	Export the curve to Bitmap file.
<i>Black / White Background</i>	Set the background of the curve window to be black or white.
<i>Embed-Ctrl Visibility</i>	Set the visibility of the sub windows (for example, the legend bar) in the display area.
<i>Embed-Ctrl Position</i>	Toggle the sub windows between floating and docking.
<i>Ctrl Bar Position</i>	If a sub window is docked, change the position of the docking.

## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

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Operations	Description
<i>Bar Chart</i>	Toggle the plot style between a bar chart and a continuous line.
<i>Auto Tip</i>	Show or hide the tip of the objects in the Curve window when moving the mouse.
<i>Add Annotation</i>	Add a text string in the Curve window.

**Note:** All these common items are available for 2D Curve (Time variation), 2D Curve (Frequency Response), and 2D Curve (DDR Measurement). However, there is an exception. *Expression Calculator...* is not available for 2D Curve (DDR Measurement). Each 2D Curve can have additional items that are unique to the specific 2D Curve window.

## 3D Plots in SSIViewer

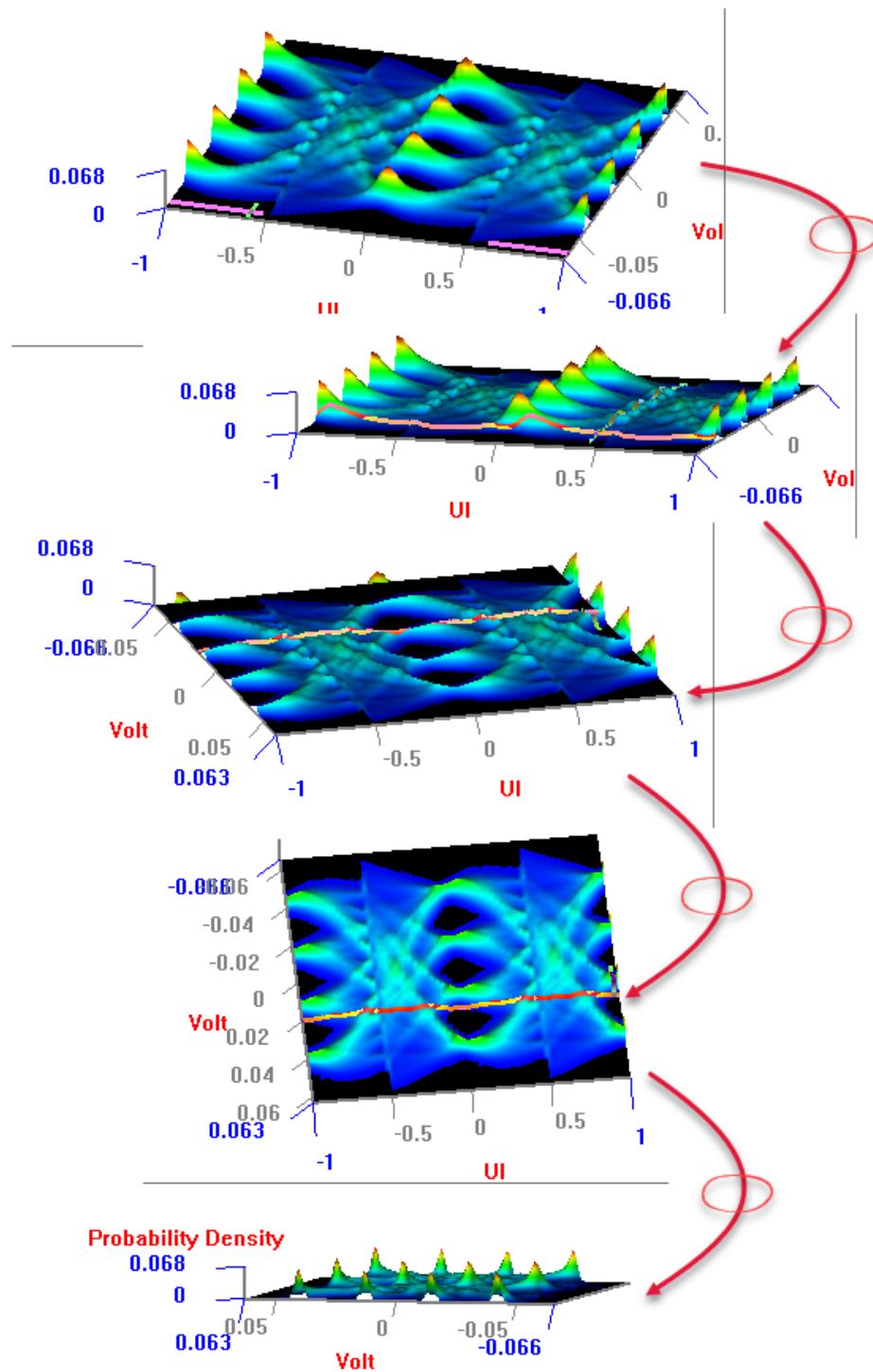
When channel simulation is used, the SSIViewer window also displays 3D plots in addition to the 2D Curves window. These plots can be zoomed in by scrolling the mouse and rotated by dragging the pointer around in all directions.

The two types of 3D plots that can be generated are shown below with illustrations:

## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

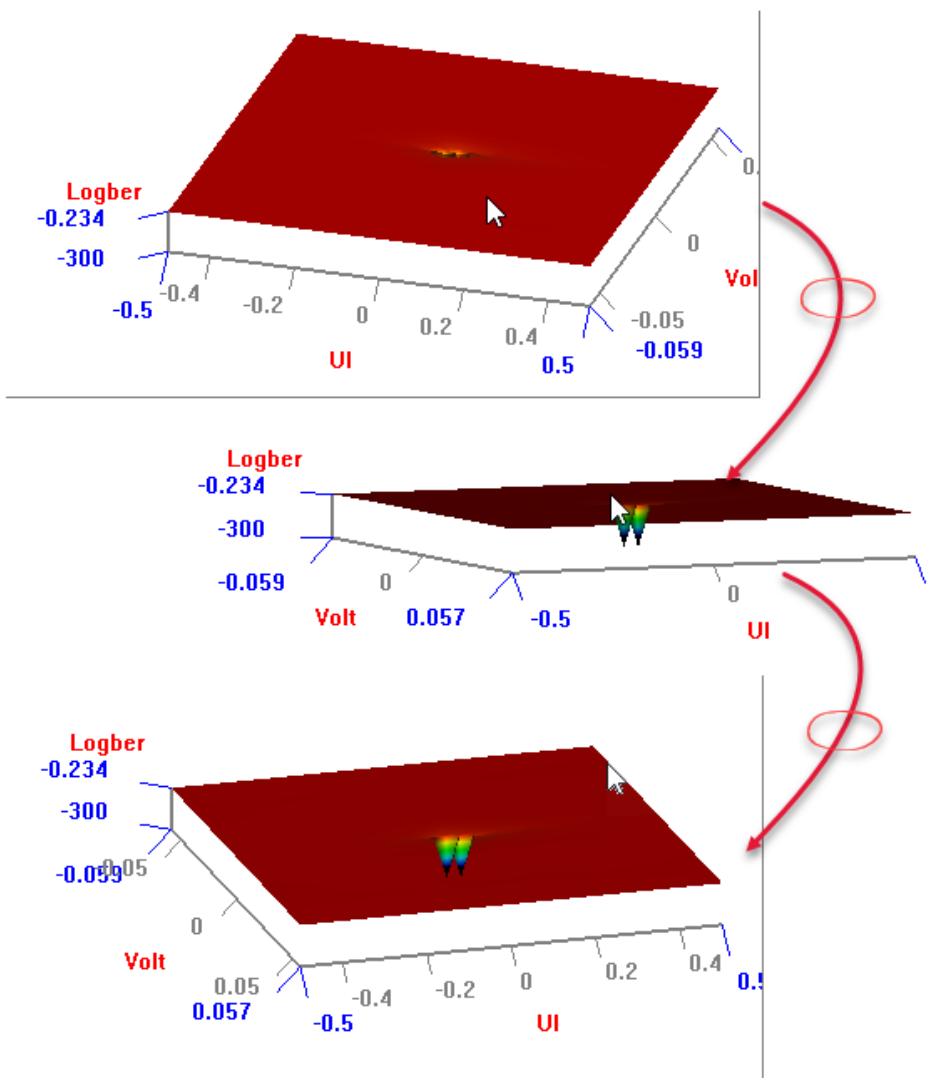
#### ■ 3D Eye Density



## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

#### ■ 3D Bathtub



## Report View

The *Report View* window is displayed for channel-based topology in SLA and PBA workflow. It displays the *Channel Report* that includes the following information:

- General information about the simulation, such as, *Baud Rate*, *Data Rate*, *Number of Bits*, *Number of Eye Bits*, *Ignore Time*, path to *Characterization Data*, and so on. The values displayed in this section are derived from your inputs in the *Analysis Options* panel.
- Algorithmic models used for the Rx and Tx models.

## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

- Jitter and noise inputs.
- Metrics used for eye contour and BER measurements.

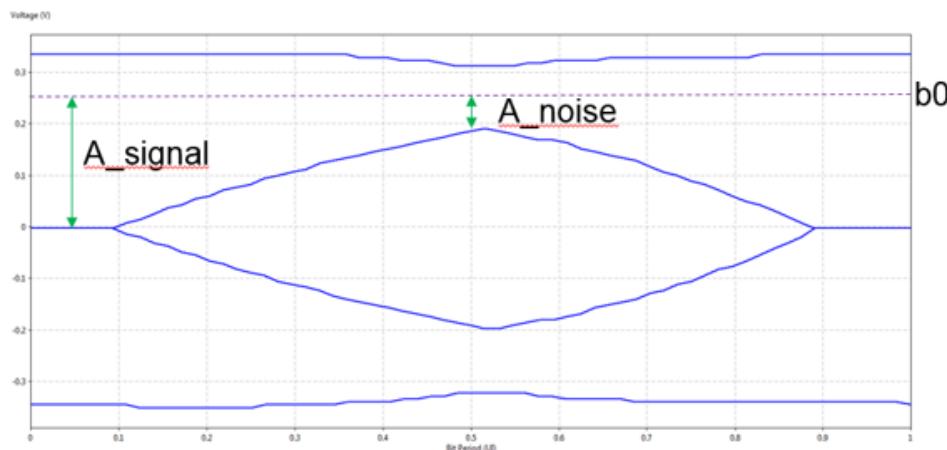
The eye contour measurement includes metrics of the Eye Height, Eye Jitter, Eye Normalized Jitter and Noise (NJN) and Channel Operating Margin (COM) as illustrated below:

Eye Height	1050 mV
Eye Height measured at	0.5 UI
Eye Jitter	0.06 UI
Eye Jitter Measured at	-6 mV
Eye Norm Jitter and Noise (NJN)	0.44
Channel Operating Margin (COM)	20.19 dB

COM is a standard metric to evaluate high speed links as described in IEEE Std. 802.3bj-2014. It is calculated by observing the vertical distribution and taking the ratio of the peak signal value to the peak noise value at the sampling point in dB. It is similar to the Normalized Jitter and Noise (NJN) metric described in the *Block Sensitivity* section because it takes into account not just the eye opening, but also the noise due to xTalk, ISI, jitter and other sources.

The COM metric is used in multiple serial link standards for signal quality. It measures from the median of the voltage distribution ( $b_0$  in the figure below) to the midpoint of the signal ( $A_{\text{signal}}$  below) and the top of the eye opening at the sampling point ( $A_{\text{noise}}$  below) to calculate COM as:

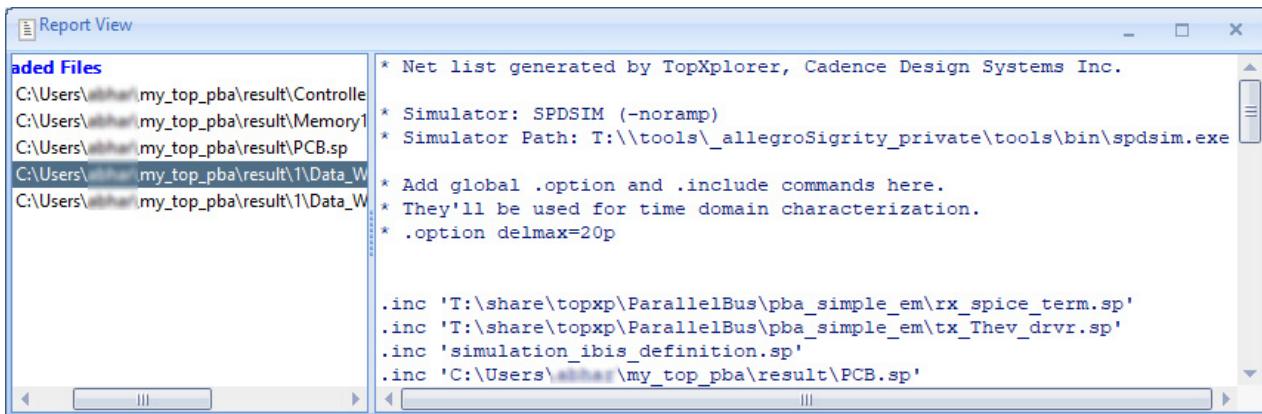
$$\text{COM (dB)} = 20 \log (A_{\text{signal}}/A_{\text{noise}})$$



## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

The *Report View* window also displays the contents of a netlist or subcircuit file when the *Show Netlist File* option is selected from the shortcut menu of the *Result Browser* panel or the *Curves* pane of the *2D Curves* window.

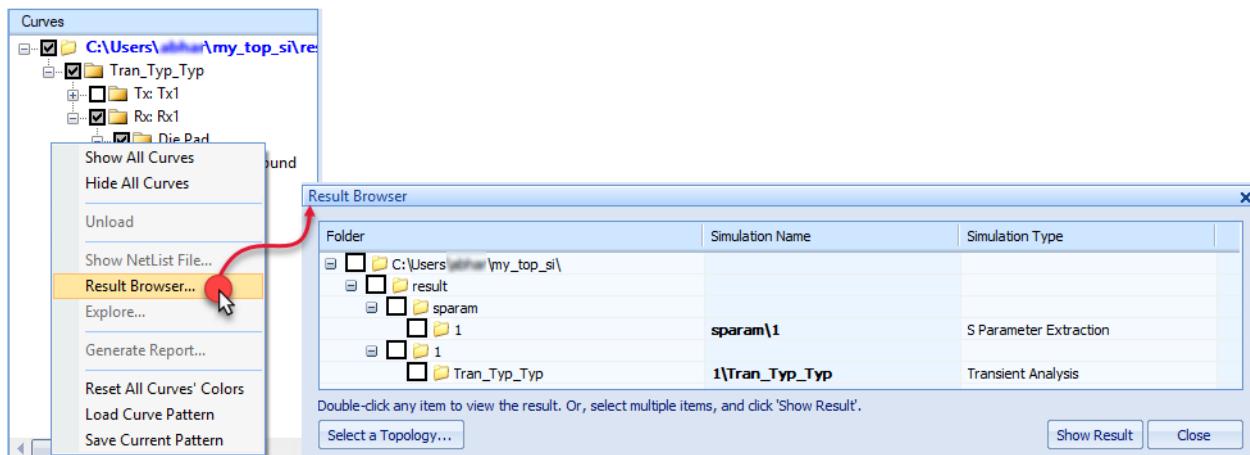


## Browsing Simulation Results

The *Result Browser* is available for all the curve windows, such as 2D Curve (Time Variation), 2D Curve (Frequency Response), S Parameter Viewer, Jitter Tolerance, Compliance Curve, 3D Eye Density, and Report View.

To open the *Result Browser* in the SSIViewer:

1. Right-click in the left panel (*Curves*) to view the shortcut menu.
2. Choose *Result Browser*. The *Result Browser* panel opens with a list of all previous results available in the *result* and *history* directory as shown below.



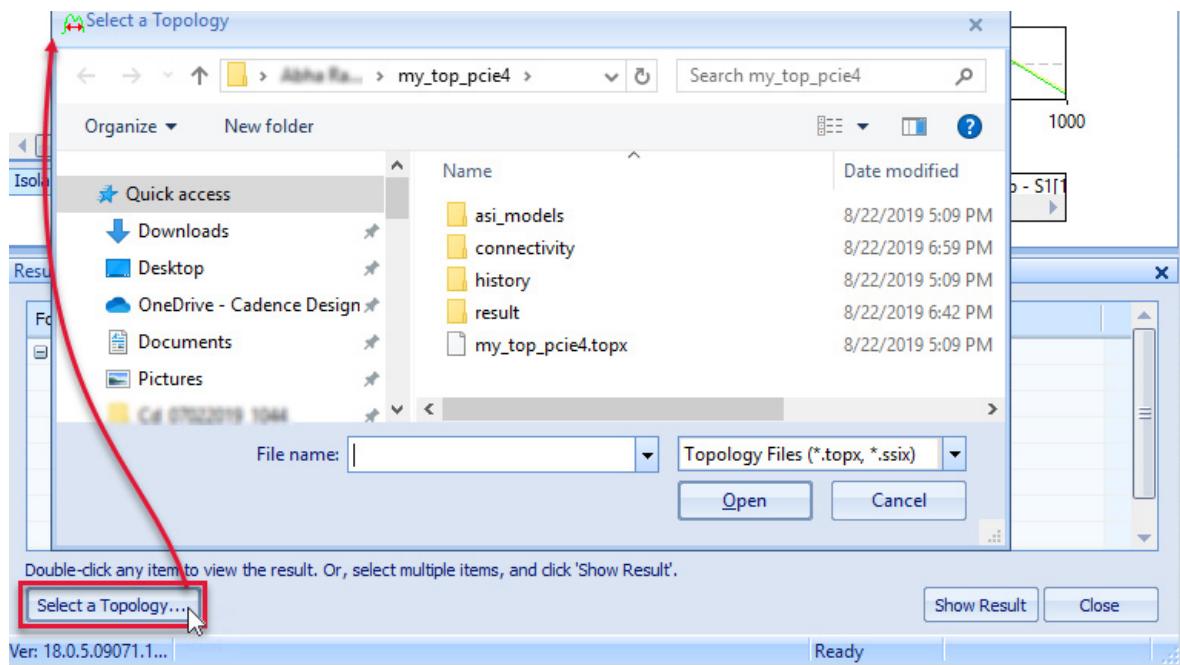
3. Double-click any item that needs to be browsed. The corresponding data is populated in the different panes of the SSIViewer window and the plot area.

The other actions that can be performed in the *Result Browser* are:

## Opening Multiple Topologies in Result Browser

To open multiple topologies in the *Result Browser* panel for analysis:

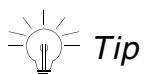
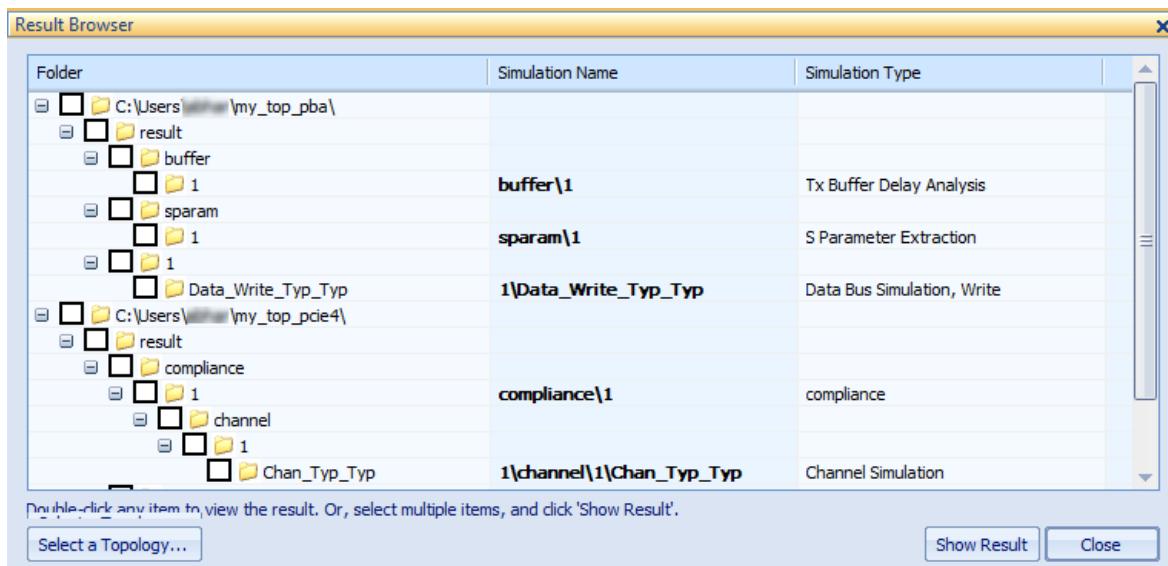
1. Click *Select a Topology* button. The *Select a Topology* dialog box is displayed.
2. Browse and select the required topology files of \*.topx or \*.ssix format.



## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

3. Click *Open* in the dialog box. The selected topology and the associated signals with corresponding simulation results are added to the list in the *Result Browser* panel as shown below.



**Tip**  
For viewing of only specific simulation results, select the check boxes displayed in the *Folder* column to choose the relevant items and then click *Show Result*. The corresponding data is populated in the different panes of the SSIViewer window and the plot area.

## Viewing Contents of a Netlist File

To view the contents of a netlist or subcircuit file generated by Topology Workbench:

1. Right-click a signal in the *Result Browser* panel.
2. Choose *Show Netlist File* from the displayed shortcut menu.

The Report View panel opens with the requested information displayed in it.

## Correlating Circuit and Channel Simulations

Circuit and channel simulation results can be automatically correlated to verify that channel simulation is faithfully reproducing circuit simulation results, and that it is appropriate to use channel simulation for the topology. Identical stimuli are used for both circuit and channel simulation, and waveforms from both circuit and channel simulations are overlaid and compared. If correlation is not acceptable, this generally means that the impulse response generated is not accurate enough, and alternative characterization methods should be explored.

**Note:** The process of correlating the circuit and channel simulation results requires that you select *SPDSIM* or *Spectre* as your simulator in the *Circuit Simulation* tab of the *Analysis Options* panel.

After a simulation run, to correlate the results of circuit and channel simulations:

1. Open *Connectivity Checker*.
2. Select *All* from the *Rx Signal* list box.
3. Right-click the blue line under the *Connection* column for the required *Rx Signal*.
4. Choose *Circuit/Channel Sim Correlation* from the displayed shortcut menu.

**Note:** Alternatively, click *Correlate Circuit/Channel Sims* from the *Simulation* section of the *Workflow* panel or choose *Tools – Circuit/Channel Sim Correlation* from the menu bar. In PBA workflow, these options are enabled only when the *Use Channel Simulator* check box is selected.

Before the correlation process starts, the following dialog boxes are displayed for confirmation if certain conditions are not met:

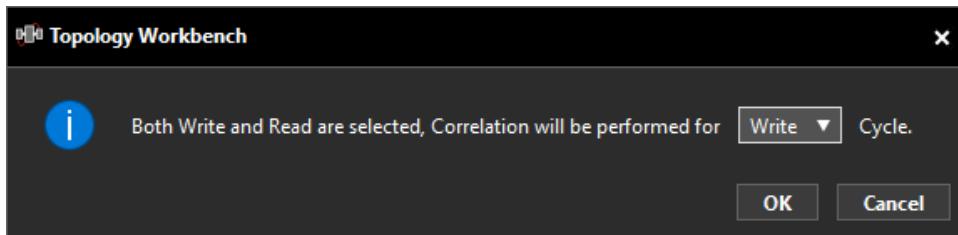
- ❑ To determine signal connectivity, the bus topology requires an AC sweep. If AC sweep has not been defined already, a message box is displayed to set the number of frequency points. The default points are set for you, which may be changed as required. Click the *Yes* or *No* button.

## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

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- ❑ In PBA workflow, when both *Write* and *Read* directions are selected in the *Analysis Options* panel, a dialog box is displayed to set the cycle for which the correlation needs to be performed, as shown below.

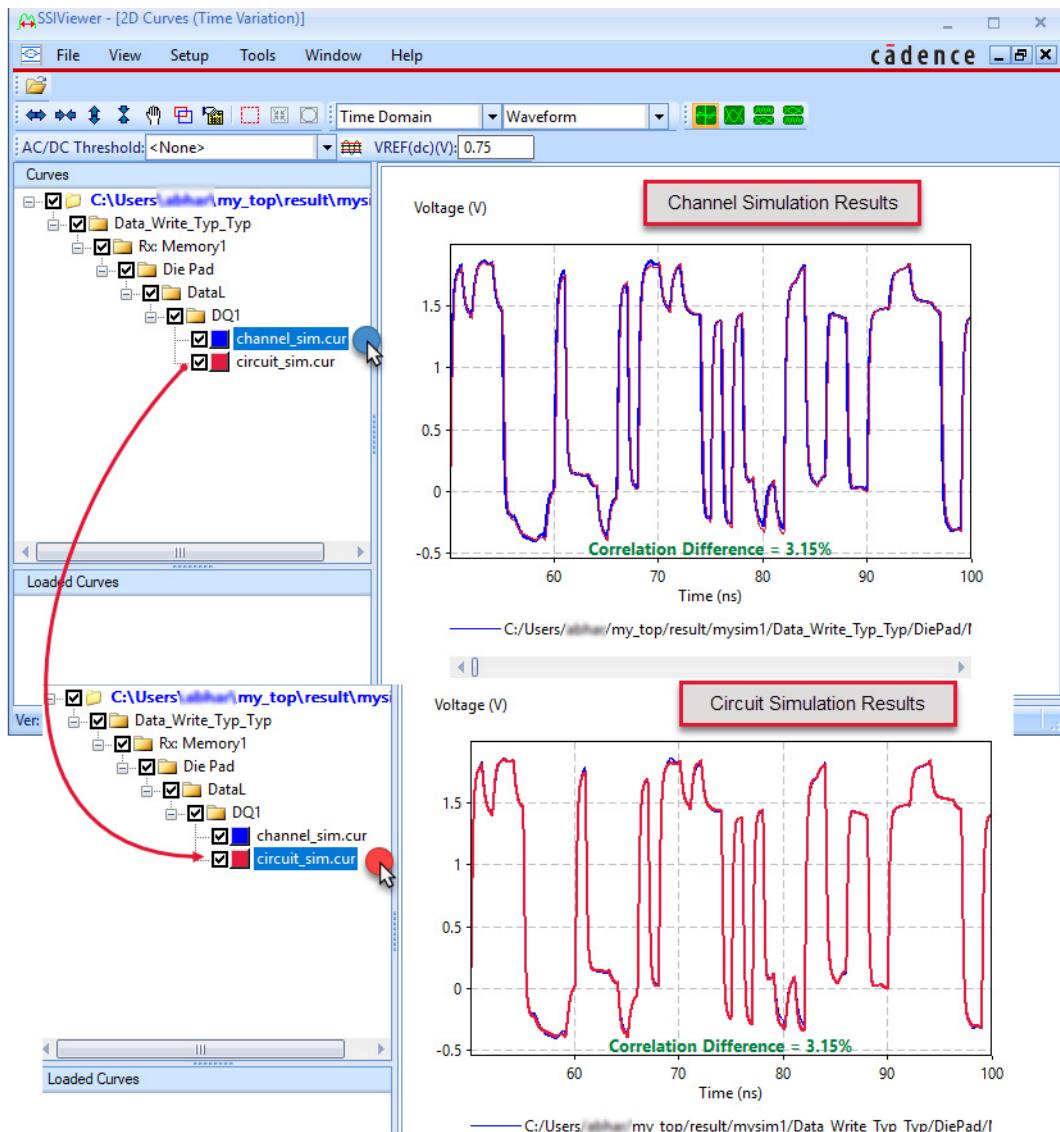


Thereafter, Topology Workbench characterizes the selected channel and then the correlation engine runs to generate the stimulus for circuit and channel simulations. The progress is displayed in the status bar.

## Topology Workbench User Guide

### Running a Simulation and Analyzing the Results

On completion of the process, the final output is displayed as waveform in the SSIViewer (2D Curves) window, as shown below.



Waveforms from both, circuit (`circuit_sim.cur`) and channel (`channel_sim.cur`) simulations, are displayed and overlaid on top of each other. A figure of merit is computed to quantify the correlation between the two. The *Correlation Difference* in terms of percentage is given at the bottom of the plot, as shown in the figure above. You can zoom in and out to draw focus to specific points of interest in the waveform.

## **Topology Workbench User Guide**

### Running a Simulation and Analyzing the Results

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## Using Topology Explorer Workflow

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In the Topology Explorer workflow of Topology Workbench, you can build custom system-level topologies and run transient simulations. You can also perform general-purpose pre-layout and post-layout exploration of topologies.

### **Related Topics**

- [Performing Transient Analysis in Topology Explorer](#)
- [Configuring the Blocks for Topology Explorer](#)
- [Using Extracted Interconnect Models in Topology Explorer](#)
- [Using Pre-Layout Transmission Line Modeling Capability](#)
- [Running Sweep Simulations](#)
- [Setting Up Constraints for Topology Explorer](#)

## Performing Transient Analysis in Topology Explorer

In the Topology Explorer workflow, transient analysis is used to look at traditional voltage versus time waveforms at receivers or probe points. A driver block is typically used to stimulate the topology in a transient circuit simulation, with waveforms being monitored at the receiver(s).

To perform transient analysis:

1. Start Topology Workbench using a method described in the [Starting Topology Workbench](#) topic.

**Note:** When you open Topology Workbench in standalone mode, choose *Topology Explorer* or *Advanced SI* from the *Cadence Product Choices* dialog box to run the Topology Explorer workflow. When a [topology is extracted from Sigrity Aurora to Topology Workbench](#), it opens in the Topology Explorer workflow.

## Topology Workbench User Guide

### Using Topology Explorer Workflow

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#### 2. Create a topology project for the Topology Explorer workflow.

For steps, refer to the [Creating a Topology Project from Scratch](#) section or the [Opening an Existing Topology Project](#) section.

When you create a new topology project, the *Topology Explorer* tab provides a list of the following default the Topology Explorer workflow-specific templates:

Template	Description
<i>diff_pair</i>	Contains differential pair signals.
<i>one_signal</i>	Contains single-ended signal.
<i>series_term_signal</i>	Contains signal with series termination.
<i>shunt_term_signal</i>	Contains signal with shunt termination.
<i>xtalk_3_signals</i>	Contains three signals that are coupled together.

Select one of these default templates or the *<blank topology>* row to start designing your own topology from scratch:

The Topology Workbench window is refreshed as following:

- A tab with the given *Topology Name* opens next to the [Start Page](#).
- The [Layout Canvas](#) is populated with the blocks as per the selected default template. If you chose to create a *<blank topology>*, the canvas is blank.
- The [Workflow Panel](#) opens with a list of tasks you need to perform during the selected type of analysis.
- The [Floating Toolbar](#) opens with a list of various types of blocks that can be used in the selected type of analysis.

#### 3. Add and place the required blocks on the canvas.

For information, see [Adding Blocks to the Canvas](#) and [Appendix A, “Choosing Blocks to Place on the Canvas.”](#)

#### 4. Connect the blocks on the canvas and configure the connections between their signals.

For information, see [Connecting the Blocks on the Canvas](#) and [Managing Connections Between Blocks and Signals](#).

#### 5. Edit and configure the properties of the various components placed on the canvas by using the [Edit Properties Panel](#).

For information, see [Editing the Properties of a Component](#).

## Topology Workbench User Guide

### Using Topology Explorer Workflow

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From the *Edit Properties* panel, you also get the options to do the following tasks:

- [Assigning and Editing IBIS Models](#)
- [Assigning and Extracting S Parameter Files](#)

**6.** Setup and manage the component model libraries.

For information, see [Setting Up Component Model](#).

**7.** Click *Check Connectivity* in the *Simulation Setup* schema to:

- Open the *Connectivity Checker* panel.
- Check whether the connectivity between the blocks is error-free.

For information, see [Checking Connectivity Between Blocks and Signals](#).

**Note:** If Topology Workbench fails to check connectivity because no port is defined for S Parameter extraction, see [Extracting an S Parameter Definition](#) for information.

**8.** Click *Set Analysis Options* in the *Simulation Setup* schema to:

- Open the *Analysis Options* panel.
- Set up the basic simulation settings such as signals to be simulated, simulator to be used, simulation configuration, and simulation name in the *Circuit Simulation* and *IO Models and Stimulus* tabs.

For information, see [Setting Up Simulation Options – Introduction](#), [Circuit Simulation](#), and [IO Models and Stimulus – Topology Explorer](#).

**9.** Click *Terminate Unconnected Pins* in the *Simulation Setup* schema to set up termination of all unconnected pins in the topology.

For information, see [Terminating Unconnected Pins](#).

**10.** Setup probe points, if needed, to view simulation results at specific points in the design. For this, use the *Probe Points* panel that can be accessed from the *Setup – Probe Points* menu.

For information, see [Setting Up Probe Points](#).

**11.** Click *Save Topology* in the *Simulation Setup* schema.

**12.** Select the *Enable Distributed Computing* check box in the *Distributed Computing Setup* schema to run the simulation across a collection of computer systems using distributed computing. This step enables the *Set up Computer Resources* option in the schema.

For information, see [Setting Up Distributed Computing Options](#).

## Topology Workbench User Guide

### Using Topology Explorer Workflow

13. Click *Start Transient Analysis* in the *Simulation* schema to run the simulation.

For information, see [Running the Simulation](#) and [Monitoring a Simulation Run in Topology Explorer](#).

After the completion of the simulation run, the 2D Curves tab, as shown below, opens with the plotted waveform results. For information, see [Viewing Simulation Results](#).



#### Related Topics

- [Configuring the Blocks for Topology Explorer](#)
- [Viewing Simulation Results](#)
- [Browsing Simulation Results](#)
- [Setting Up Component Model](#)
- [Switching to Another Workflow](#)
- [Customizing a Workflow](#)
- [Creating Custom Templates](#)
- [Archiving a Topology](#)

## Configuring the Blocks for Topology Explorer

For transient analysis in the Topology Explorer workflow, you can:

- Instantiate the required types of blocks on the canvas and connect them to form a wired topology. The blocks can be chosen from the [Floating Toolbar](#).  
See [Choosing Blocks to Place on the Canvas](#) for the complete range of blocks that can be used in the Topology Explorer workflow.
- Edit the properties of a block in the *Component Properties* tab ( ) of the [Edit Properties Panel](#) as described in the [Editing the Properties of a Component](#) section.

To know more about configuring a few commonly used blocks in the Topology Explorer workflow, see:

- [Transmitter and Receiver SPICE-Based Blocks](#)
- [Transmitter and Receiver IBIS-Based Block](#)
- [S Parameter Block](#)
- [Trace Block](#)
- [Via Block](#)
- [Discrete Block](#)
- [Terminator Block](#)
- [Current Source \(Is\) Block](#)
- [Voltage Source \(Vs\) Block](#)

### Transmitter and Receiver SPICE-Based Blocks

The Transmitter (Tx) and Receiver (Rx) SPICE-based blocks contain a SPICE subcircuit.

In the *Component Properties* tab of the *Edit Properties* panel for a Tx or Rx block, you can:

1. Assign a SPICE *Circuit File* of \*.sp or \*.ckt format.
  - a. Click *E* that is displayed when the pointer is placed in the cell adjacent to *Circuit File*. Alternatively, click *Load Circuit File*.
  - b. Browse and select the required file from the displayed dialog box.

- c. Select the *Subcircuit* from the list that is populated based on the specified circuit file.
  - d. Click *View Subcircuit* to open the *Subcircuit Editor*. You can edit the subcircuit definition in this editor and then click *OK* to save the changes.
2. Select the *Ideal Power* check box if you want to run ideal power simulation. When this check box is selected, set the ideal voltage that the block should use. By default, it is set to 1.0 V.

For ideal power simulation, ideal power supply should be defined according to the following rules:

- If power supply is not defined in the \*.sp file assigned to the Tx or Rx block, enable *Ideal Power* in the *Edit Properties* panel.
- If power supply is not defined in the \*.sp file assigned to the Tx or Rx block, disable *Ideal Power* in the *Edit Properties* panel.

For non-ideal power simulation, that is, when *Ideal Power* is not selected, both Tx and Rx blocks should get their power supply from a Voltage Regulator Module (VRM) block.

## Using Differential Transmitter and Receiver SPICE-Based Blocks

By default, the Tx and Rx blocks represent a single-ended transmitter and receiver, respectively. To use a differential Tx or Rx:

1. Click the *Settings* option in the floating toolbar.
2. Select the *Diff Signals* toggle button to use blocks with differential signals in the topology.
3. Use the differential Tx or Rx blocks from the displayed list.

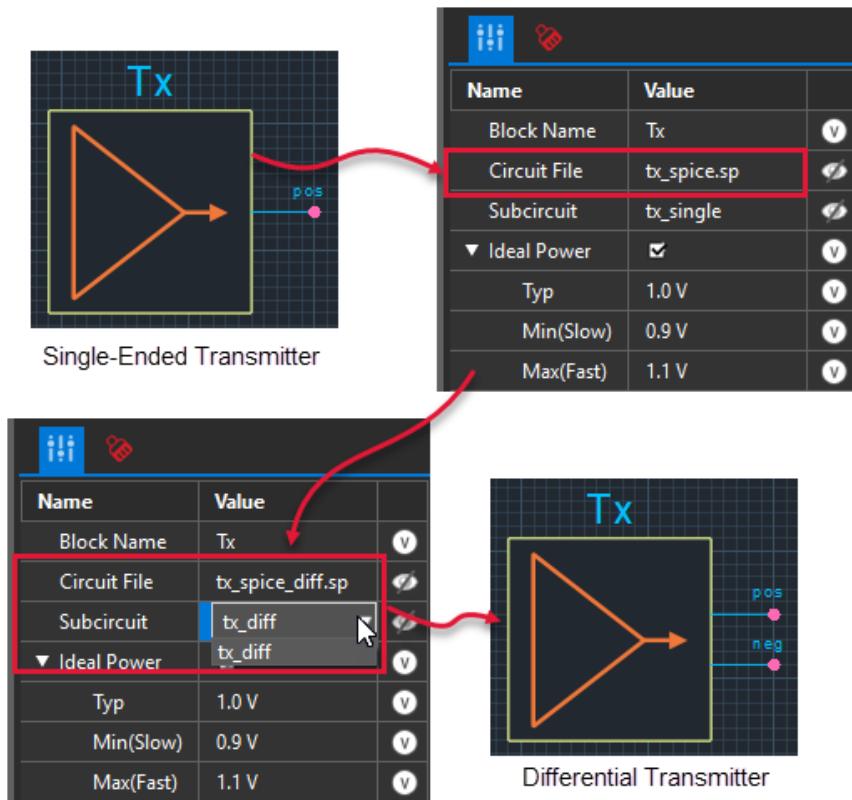
Alternatively, to represent an existing single-ended Tx or Rx block as a differential Tx or Rx, you can modify the properties of the single-ended block as following:

1. Select a SPICE-based *Circuit File* that defines differential signals. For example, you can choose the template SPICE files, tx\_spice\_diff.sp for a Transmitter block or rx\_spice\_diff.sp for a Receiver block.
2. Select the corresponding differential *Subcircuit* from the list box that gets refreshed based on the chosen SPICE file.

## Topology Workbench User Guide

### Using Topology Explorer Workflow

The following image illustrates the change that can be seen in a Transmitter block:



## Transmitter and Receiver IBIS-Based Block

For information, see [Assigning and Editing IBIS Models](#).

## S Parameter Block

For information, see [Assigning and Extracting S Parameter Files](#).

## Trace Block

Using a Trace block in the topology lets you leverage the advantages of pre-layout transmission line modeling capability. For information, see [Modeling Pre-Layout Transmission Lines](#).

## Via Block

A Via block is used for vertical layer transitions that are represented by SPICE subcircuits or S-parameters. In the *Component Properties* tab of the *Edit Properties* panel for a Via block, you can:

1. Assign a SPICE *Circuit File* of \*.sp or \*.ckt format.
  - a. Click *E* that is displayed when the pointer is placed in the cell adjacent to *Circuit File*.
  - b. Browse and select the required file from the displayed dialog box.
2. Select the *Subcircuit* from the list that is populated based on the specified circuit file.
3. Click *View Subcircuit* to open the *Subcircuit Editor*. You can edit the subcircuit definition in this editor and then click *OK* to save the changes.

For detailed information, refer to [Using the Via Wizard](#).

## Discrete Block

By default, a discrete block represents a resistor. You can modify the block properties to represent other discrete components, such as capacitors and inductors.

After adding the block, in the *Component Properties* tab of the *Edit Properties* panel for a discrete block, you can:

1. Select the *Model Type* of the discrete block.

By default, the *Model Type* is set to *Resistor*. The other available options for choice are *Inductor*, *Capacitor*, *SeriesRLC*, *ParallelRC*, and *IdealDiode*.

# Topology Workbench User Guide

## Using Topology Explorer Workflow

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As you change the selection in the *Model Type* list, the symbol within the discrete block placed on the canvas and the associated fields within the *Edit Properties* panel change, as shown below.



2. Modify the *Number of Nets* if you want more than one instance of the discrete model type to be included in the discrete block model. Else, by default, only one instance is

## Topology Workbench User Guide

### Using Topology Explorer Workflow

included. The corresponding changes that are made in subcircuit definition can be viewed in the *Subcircuit Editor* as shown below.

Properties Panel View		Subcircuit Editor View
Block Name	Discrete	
Model Type	IdealDiode	
Number of Nets	1	
Net Group	Signal	

Properties Panel View		Subcircuit Editor View
Block Name	Discrete	
Model Type	IdealDiode	
Number of Nets	3	
Net Group	Signal	

3. Select the *Net Group* from the list as *Signal* or *Power*.
4. Select the *Include POWER* check box to include non-ideal power effects during simulations.
5. Specify values greater than zero for resistance, inductance, and capacitance. All or one of these values is required based on the *Model Type* you select. Suffixes *m*, *u*, *n*, and *p* can be used to indicate milli( $10^{-3}$ ), micro( $10^{-6}$ ), nano( $10^{-9}$ ), and pico ( $10^{-12}$ ), respectively. For *IdealDiode* model type, you need to specify the cut-off voltage (*CutoffVoltage*).

## Terminator Block

Use this block to add terminations to the design.

After adding the block, in the *Component Properties* tab of the *Edit Properties* panel for a terminator block, you can specify the termination technique and the values of the components used in the termination schemes as following:

1. Select the *Model Type* of the terminator block.

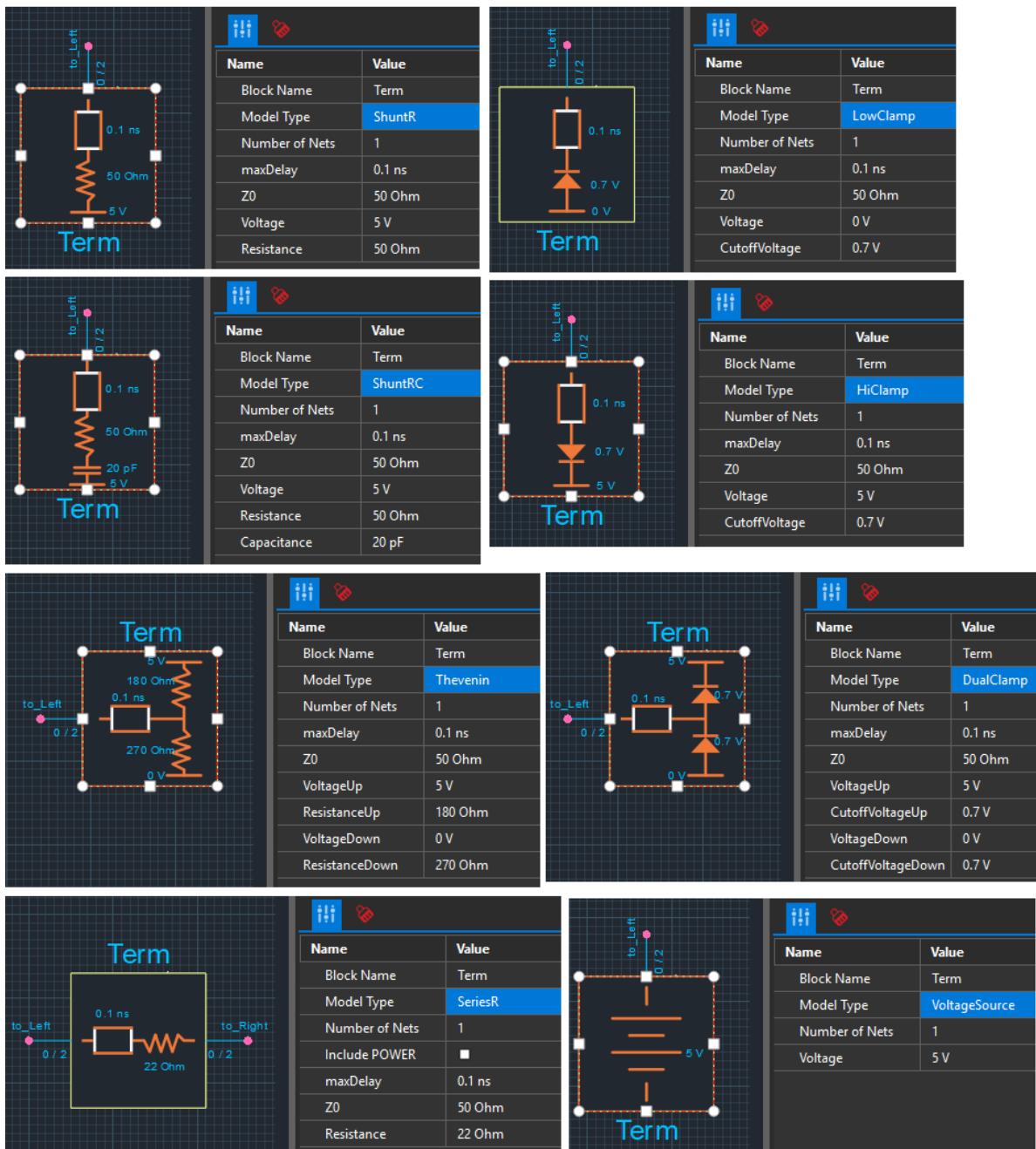
# Topology Workbench User Guide

## Using Topology Explorer Workflow

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By default, the *Model Type* is set to *ShuntR*. The other available options for choice are *ShuntRC*, *SeriesR*, *Thevenin*, *DualClamp*, *HiClamp*, *LowClamp*, and *VoltageSource*.

As you change the selection in the *Model Type* list, the symbol within the terminator block placed on the canvas and the associated fields within the *Edit Properties* panel change, as shown below.



2. Modify the *Number of Nets* if you want more than one instance of the termination technique to be included in the terminator block model. Else, by default, only one instance is included.
3. Select the *Include POWER* check box to include non-ideal power effects during simulations.
4. Specify the *maxDelay* value to define the Transmission Line (T-Line) delay
5. Specify the *Z0* value to define the T-Line Impedance in terms of Ohms ( $\Omega$ ).

A few additional properties are displayed for configuration based on the selected termination technique. For example,

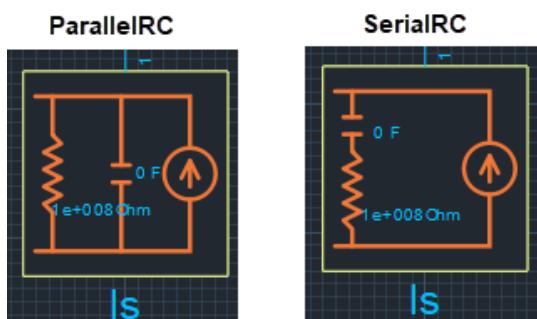
- *Voltage* needs to be specified when *Model Type* is set to *ShuntR*, *ShuntRC*, and *VoltageSource*.
- *Resistance* can be specified for *SeriesR*.
- *CutoffVoltage* (cut-off voltage) is specified for *LowClamp* and *HiClamp*.

## Current Source (Is) Block

Placement of current source blocks is useful for power integrity analysis. It enables excitation currents to be applied to a power distribution network (PDN) to observe voltage ripple in the time domain.

By default, the current source block generates the *Gaussian* waveform. To select a different waveform shape, open the *Component Properties* tab of the *Edit Properties* panel for the current source block and select one of the following options from the *Model Type* list box: *Gaussian*, *PWL*, *Pulse*, or *Sinesquare*.

In addition, you change the *Source Impedance* from the list box. The two available options are *ParallelIRC* and *SerialIRC*. Depending on the selection, the symbol within the current source block changes as shown below.

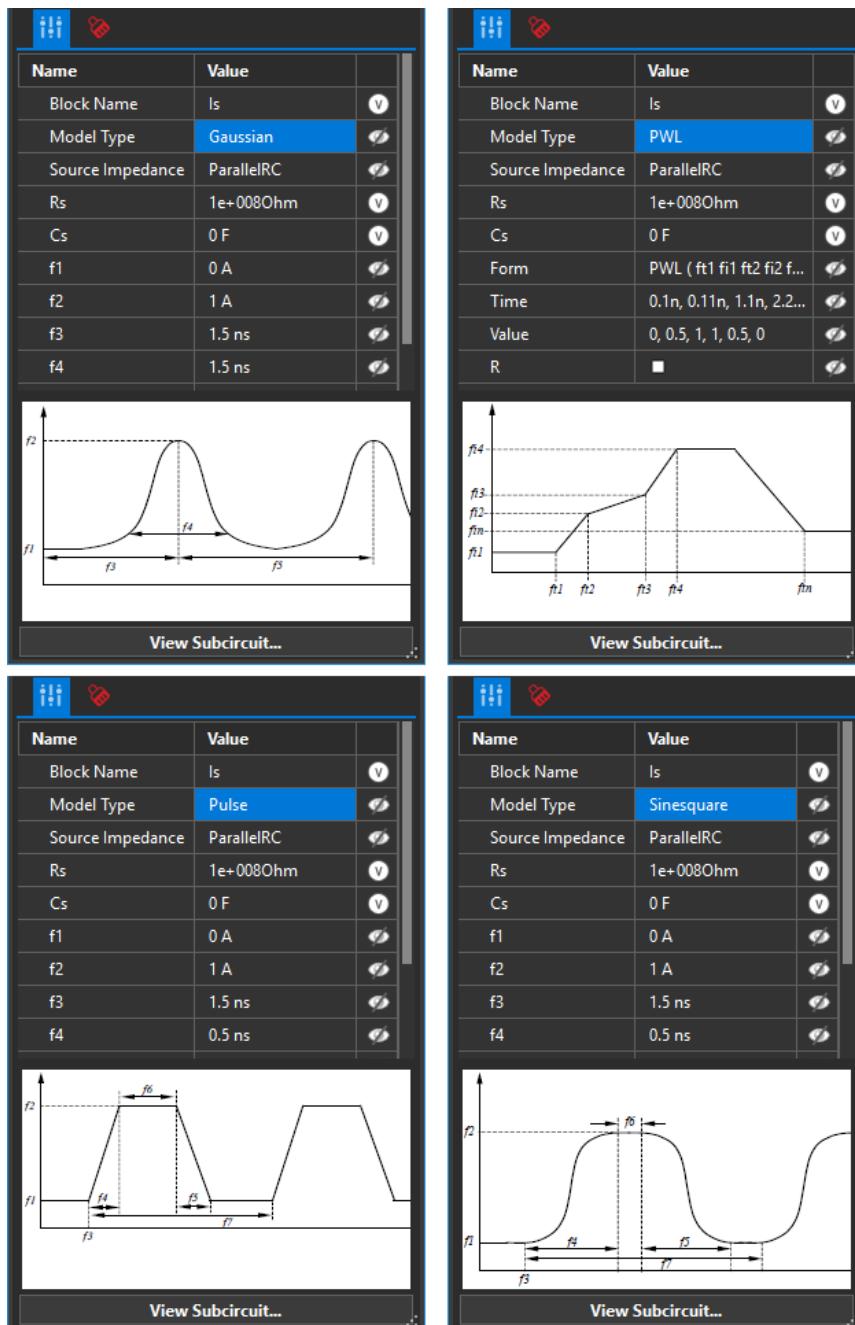


## Topology Workbench User Guide

### Using Topology Explorer Workflow

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As you change the selection in the *Model Type* list, the sample waveform shape displayed at the bottom of the *Edit Properties* panel changes accordingly, as shown below.



In addition, modify the parameter values to customize the waveform shapes. The supported waveforms and the related parameters are:

## Topology Workbench User Guide

### Using Topology Explorer Workflow

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#### ■ Gaussian waveform

Parameter	Indicates	Value
$f1$	Initial value	A (Ampere)
$f2$	Peak value	A (Ampere)
$f3$	Time Delay Recommended value: 1.3 to 1.5 times $f4$	ns (nanoseconds)
$f4$	Pulse Width Measured at 5% of (Peak value - initial value) $\frac{5}{100} \times (f2 - f1)$	ns (nanoseconds)
$f5$	Time Period	ns (nanoseconds)

#### ■ PWL (Piecewise Linear) waveform

Parameter	Indicates	Value
<i>Time</i>	Time at $ft1$ , $ft2$ , $ft3$ , ..., $ftn$	ns
<i>Value</i>	Current at $ft1$ , $ft2$ , $ft3$ , ..., $ftn$	A
<i>R</i>	Select this check box if you need to repeat the PWL waveform. It is equivalent to the <code>repeat</code> keyword in HSPICE format.  Selecting this check box enables the text box where you can specify the time to be used as the start point of the waveform to be repeated. If no value is assigned in the text box, the complete PWL waveform is repeated.	

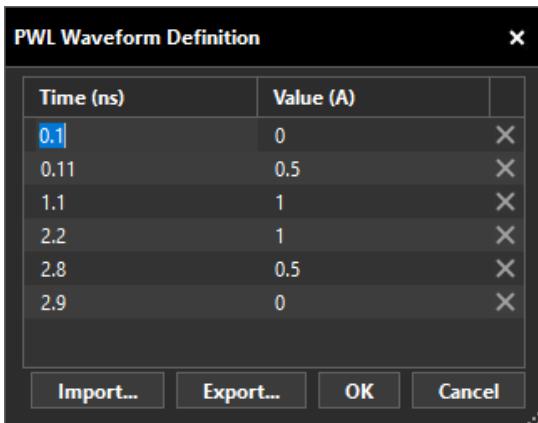
 *Important*

The time value for the repeat function cannot be greater than the maximum time specified in the PWL Waveform Definition.

## Topology Workbench User Guide

### Using Topology Explorer Workflow

**Note:** Clicking the *E* button in the *Time* or *Value* cell enables you to edit the specified values in the *PWL Waveform Definition* window, as shown below.



In this window, you can specify the custom time-current value pairs. In addition, you can import the time-current value pairs from a text file or export the time-current value pairs to a text file using the given buttons.

#### ■ Pulse waveform

Parameter	Indicates	Value
$f_1$	Initial Value of the pulse	A
$f_2$	Peak Value of the pulse	A
$f_3$	Time Delay	ns
$f_4$	Rise Time	ns
$f_5$	Fall Time	ns
$f_6$	Pulse Width	ns
$f_7$	Period. It is set to infinity (inf) by default.	ns

#### ■ Sinesquare waveform

Parameter	Indicates	Value
$f_1$	Initial Value of the pulse	A
$f_2$	Peak Value of the pulse	A
$f_3$	Time Delay	ns

<i>f4</i>	Rise Time	ns
<i>f5</i>	Fall Time	ns
<i>f6</i>	Pulse Width	ns
<i>f7</i>	Period. It is set to infinity (inf) by default.	ns

## Voltage Source (Vs) Block

By default, the voltage source block generates the *Gaussian* waveform – similar to a current-source block. Using the *Edit Properties* panel, you can modify the default output by specifying a different waveform shape or by modifying the parameter values to tweak the waveform shapes.

For information on specific parameters, see [Current Source \(Is\) Block](#).

## Using Extracted Interconnect Models in Topology Explorer

The Layout Association functionality in Topology Workbench provides direct integration with PowerSI and SPEEDEM Generator (SPDGEN), enabling automation in the extraction and model generation for blocks in Topology Workbench topologies that are based on physical layout.

For details, see [Using Extracted Interconnect Models from Layout](#).

## Using Pre-Layout Transmission Line Modeling Capability

Topology Workbench includes the pre-layout transmission line (TLine) modeling capability.

For details, see [Modeling Pre-Layout Transmission Lines](#).

## Running Sweep Simulations

The *Sweep Manager* allows multiple values to be set for key parameters in the topology. Sweeping then will automatically run multiple simulations, substituting in the relevant parameter values for each unique simulation run. Results can then be analyzed to understand the impact of the parameter values on overall performance.

For details, see [Using the Sweep Manager](#).

## **Setting Up Constraints for Topology Explorer**

In the Topology Explorer workflow, you can define constraints in a topology project as an Electrical Constraint Set (ECSet), which applies to each net, and then import them to Constraint Manager.

For details, see [Exporting Constraints from a Topology](#).

# **Topology Workbench User Guide**

## Using Topology Explorer Workflow

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# **Using Serial Link Analysis Workflow**

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The Serial Link Analysis (SLA) workflow of Topology Workbench allows you to model, simulate, analyze, and evaluate signal integrity performance of serial link systems.

### ***Related Topics***

- [Analyzing Serial Links](#)
- [Performing Statistical Analysis](#)
- [Building AMI Models for a Serial Link Topology](#)
- [Modeling Repeaters](#)
- [Working with Compliance Kits](#)
- [Using Extracted Interconnect Models in Serial Link Analysis](#)
- [Using Pre-Layout Transmission Line Modeling Capability](#)
- [Creating Extraction-Based Crosstalk Topologies](#)
- [Running Sweep Simulations](#)
- [Setting Up Constraints for Serial Link Analysis](#)

## **Analyzing Serial Links**

In the SLA workflow, you can build topologies for complete serial link interfaces, consisting of transmitter and receiver blocks that are connected through one or more blocks for the channel.

To build a serial link topology, you can use the built-in application-specific blocks available in Topology Workbench and then assign electrical models and connect all the blocks.

To perform serial link analysis:

## Topology Workbench User Guide

### Using Serial Link Analysis Workflow

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1. Start Topology Workbench using a method described in the [Starting Topology Workbench](#) topic.

**Note:** When you open Topology Workbench in standalone mode, choose *Advanced SI* or *Advanced IBIS Modeling* from the *Cadence Product Choices* dialog box to run the SLA workflow.

2. Create a topology project for the SLA workflow.

For steps, refer to the [Creating a Topology Project from Scratch](#) section or the [Opening an Existing Topology Project](#) section.

When you create a new topology project,

- a. Specify a *Topology Name* and browse the *Topology Path* to save your topology.
- b. Click the *SystemSI* tab.
- c. Click the *Serial Link Analysis* tab. A list of the following default SLA workflow-specific templates are displayed for choice:

Template	Description
<i>backplane_thru</i>	Contains a channel created through multiple daughter cards, connectors, and backplane.
<i>com_template_thru</i>	Contains blocks for Channel Operating Margin analysis.
<i>ibis_sparam_thru</i>	Contains a channel created through S-parameters using IBIS models.
<i>pam4_simple</i>	Contains a simple example that uses PAM4 signaling.
<i>measurement_xtalk</i>	Contains an example of incorporating multiple measured S-parameters.
<i>pcb_thru</i>	Contains a channel created through PCB S-parameter.
<i>repeater_simple</i>	Contains a simple example of two channels connected with a repeater.
<i>sla_simple_em</i>	Contains a simple example of a serial link using IBIS [External Model] syntax.
<i>xtalk_channel_simple</i>	Contains a serial link with crosstalk aggressors that uses coupled Traces.

## Topology Workbench User Guide

### Using Serial Link Analysis Workflow

Template	Description
<code>xtalk_channel_sparam</code>	Contains a serial link with crosstalk aggressors that uses S-parameters.

- d. Select one of the default templates or the `<blank topology>` row to start designing your own topology from scratch.
- e. Click *Create*.

The Topology Workbench window is refreshed as following:

- ❑ A tab with the given *Topology Name* opens next to the Start Page.
- ❑ The Layout Canvas is populated with the blocks as per the selected default template. If you chose to create a `<blank topology>`, the canvas is blank.
- ❑ The Workflow Panel opens with a list of tasks you need to perform during the selected type of analysis.
- ❑ The Floating Toolbar opens with a list of various types of blocks that can be used in the selected type of analysis.

3. Add and place the required blocks on the canvas.

For information, see Adding Blocks to the Canvas and Appendix A, “Choosing Blocks to Place on the Canvas.”

4. Connect the blocks on the canvas and configure the connections between their signals.

For information, see Connecting the Blocks on the Canvas and Managing Connections Between Blocks and Signals.

5. Edit and configure the properties of the various components placed on the canvas by using the Edit Properties Panel.

For information, see Editing the Properties of a Component.

From the *Edit Properties* panel, you also get the options to do the following tasks:

- ❑ Assigning and Editing IBIS Models
- ❑ Assigning and Extracting S Parameter Files

6. Setup and manage the component model libraries.

For information, see Setting Up Component Model.

7. Click *Check Connectivity* in the *Simulation Setup* schema to:

- Open the *Connectivity Checker* panel.
- Check whether the connectivity between the blocks is error-free.

For information, see [Checking Connectivity Between Blocks and Signals](#).

**8.** Click *Set Analysis Options* in the *Simulation Setup* schema to:

- Open the *Analysis Options* panel.
- Set up the basic simulation settings such as signals to be simulated, simulator to be used, simulation configuration, and simulation name in the *Circuit Simulation*, *Channel Simulation*, and *IO Models and Stimulus* tabs.

For information, see [Setting Up Simulation Options – Introduction](#), [Circuit Simulation](#), [Channel Simulation – Serial Link Analysis](#), and [IO Models and Stimulus – Serial Link Analysis](#).

**9.** Click *Terminate Unconnected Pins* in the *Simulation Setup* schema to set up termination of all unconnected pins in the topology.

For information, see [Terminating Unconnected Pins](#).

**10.** Setup probe points, if needed, to view simulation results at specific points in the design. For this, use the *Probe Points* panel that can be accessed from the *Setup – Probe Points* menu.

For information, see [Setting Up Probe Points](#).

**11.** Click *Save Topology* in the *Simulation Setup* schema.

**12.** Select the *Enable Distributed Computing* check box in the *Distributed Computing Setup* schema to run the simulation across a collection of computer systems using distributed computing. This step enables the *Set up Computer Resources* option in the schema.

For information, see [Setting Up Distributed Computing Options](#).

**13.** Click *Start Channel Simulation* in the *Simulation* schema to run the simulation.

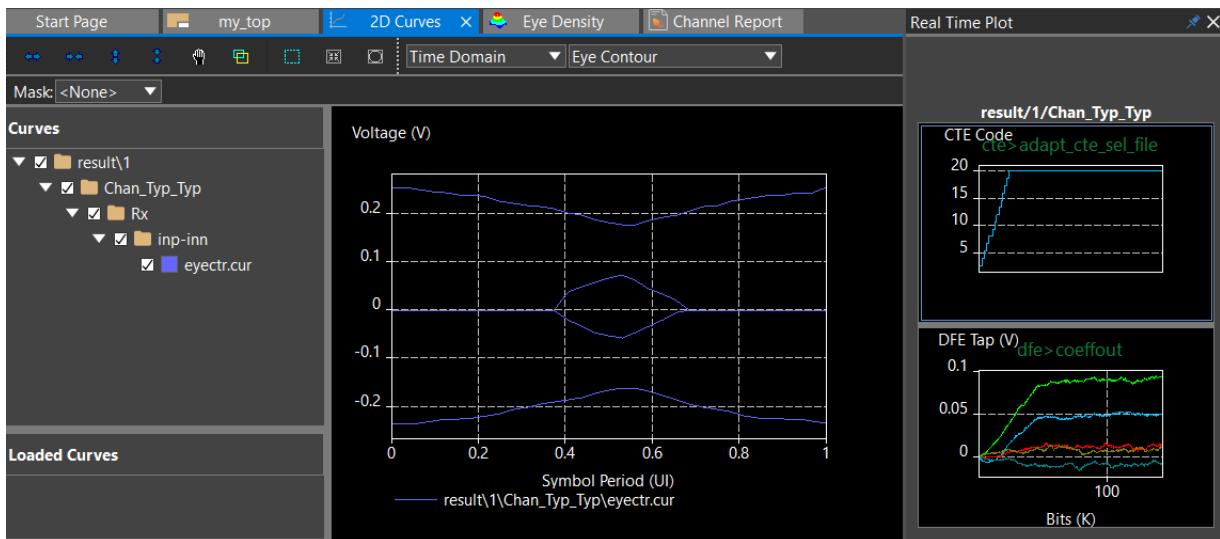
For information, see [Running the Simulation](#) and [Monitoring a Simulation Run in Serial Link Analysis](#).

While the simulation is running, the status bar shows the progress. In addition, the *Real Time Plot* panel shows to you how the waveforms are being plotted as the simulation progresses. Then, after the completion of the simulation run, the following tabs open with

# Topology Workbench User Guide

## Using Serial Link Analysis Workflow

the waveform results plotted for time domain—2D Curves, Eye Density, and Channel Report. For information, see [Viewing Simulation Results](#).



### Related Topics

- [Browsing Simulation Results](#)
- [Setting Up Component Model](#)
- [Switching to Another Workflow](#)
- [Customizing a Workflow](#)
- [Creating Custom Templates](#)
- [Using the AMI Builder](#)
- [Archiving a Topology](#)

## Performing Statistical Analysis

The traditional analysis flow used in SLA workflow involves bringing the impulse response of the channel circuit into an advanced convolution-based channel simulator, and deriving time domain waveforms at the receiver. These waveforms are then statistically post-processed to produce the eye diagrams, bathtub curves, and other outputs. More the number of bits that are run through the channel, more accurate is the result.

## Topology Workbench User Guide

### Using Serial Link Analysis Workflow

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Statistical analysis generally applies to linear, time-invariant (LTI) systems. Linearity in a system indicates that superposition applies. Time invariance indicates that for a system with  $x(t)$  input and  $y(t)$  output, a time shift  $z$  in the input, for example,  $x(t+z)$  will result in a corresponding time-shifted output,  $y(t+z)$ . Many (although not all) serial link systems can be approximated as LTI, hence statistical analysis is a useful capability to have in the serial link analysis toolbox.

The primary advantage of pure statistical analysis as opposed to time domain simulation approaches is that all inter-symbol interference (ISI) can be directly accounted for. As such, its accuracy is not dependent on the number of bits that are simulated, as is the case with the traditional time domain approach.

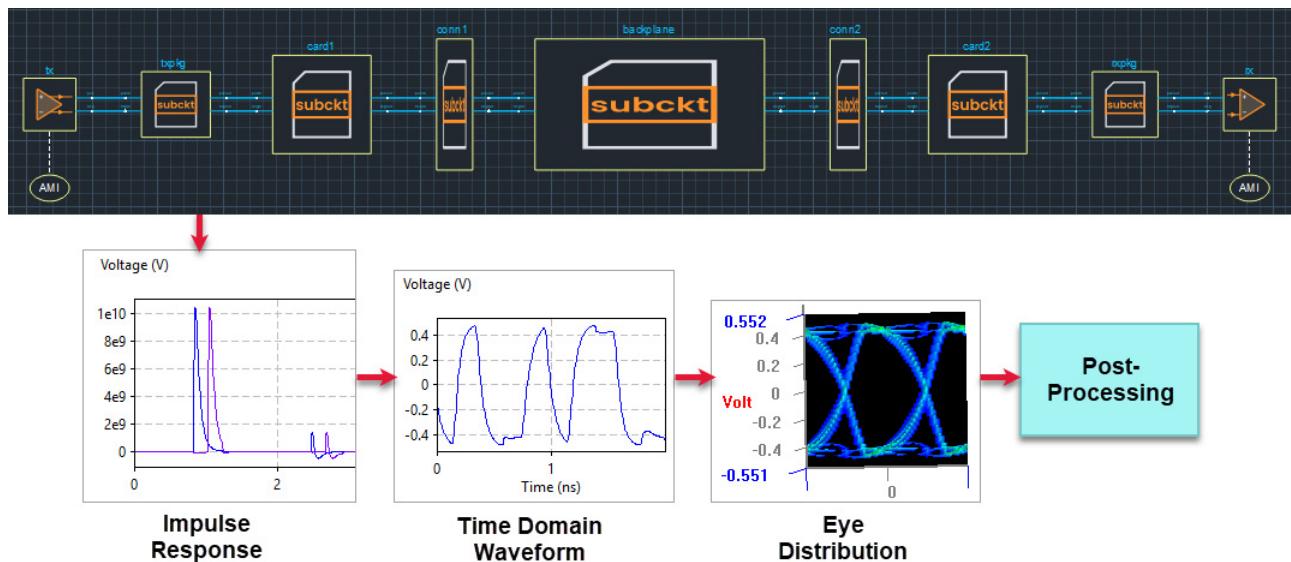
The primary limitation of statistical analysis is that it only applies to LTI systems. Algorithmic (AMI) models that use the `AMI_GetWave` function, perform real-time waveform processing and as such cannot guarantee LTI operation. Many multi-gigabit receivers that use Decision Feedback Equalization (DFE) use the `AMI_GetWave` call, and serial links that use these kinds of AMI models are not compatible with a pure statistical approach, and must be analyzed with time domain approaches.

This section covers the following topics:

- [Understanding the Statistical Analysis Capability](#)
- [Enabling Statistical Analysis Method for Eye Distribution Calculation](#)
- [Generating Statistical Eye Contours](#)

## Understanding the Statistical Analysis Capability

First, consider the traditional time domain flow for Serial Link Analysis shown below.



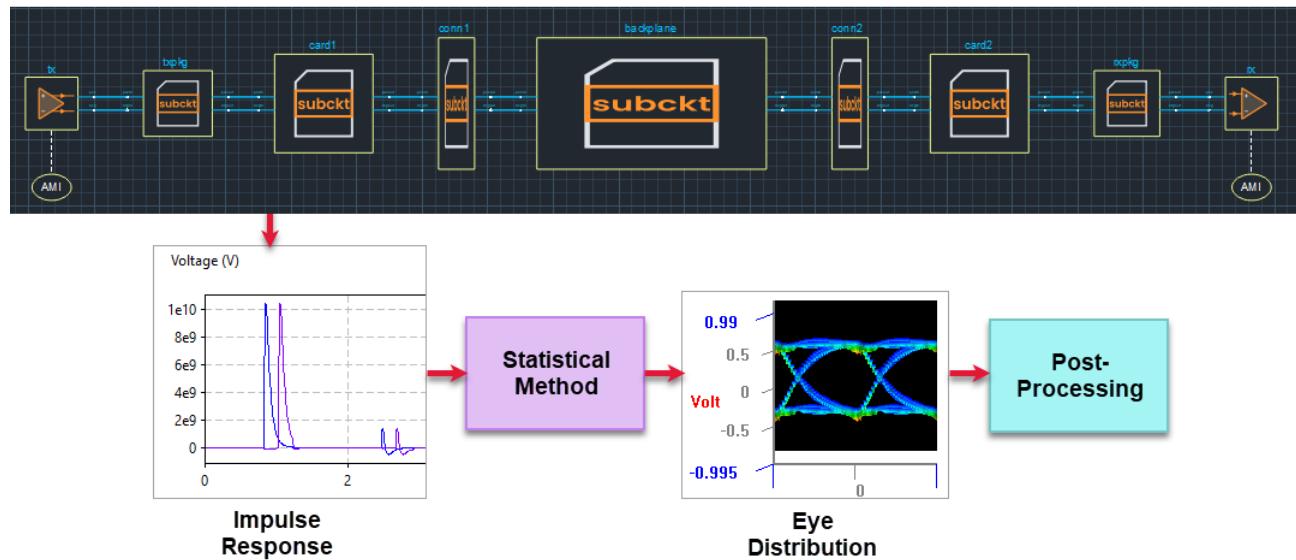
Circuit simulation is used to produce a step response at the receiver (Rx), from which the impulse response is mathematically derived. The impulse response is convolved with the incoming bit stream in the channel simulator to produce raw waveforms at the Rx. From these waveforms, the eye distribution is produced. Additional noise and jitter injections, Dj, Dn, Rj, and Rn are applied to this distribution to produce the cumulative eye distribution. This eye distribution is post-processed to produce eye contours, bathtub curves, and other outputs.

**Note:** AMI Builder supports the option to generate AMI models for `AMI_Init` that use modified impulse response. These `AMI_Init` models are applied in statistical analysis.

## Topology Workbench User Guide

### Using Serial Link Analysis Workflow

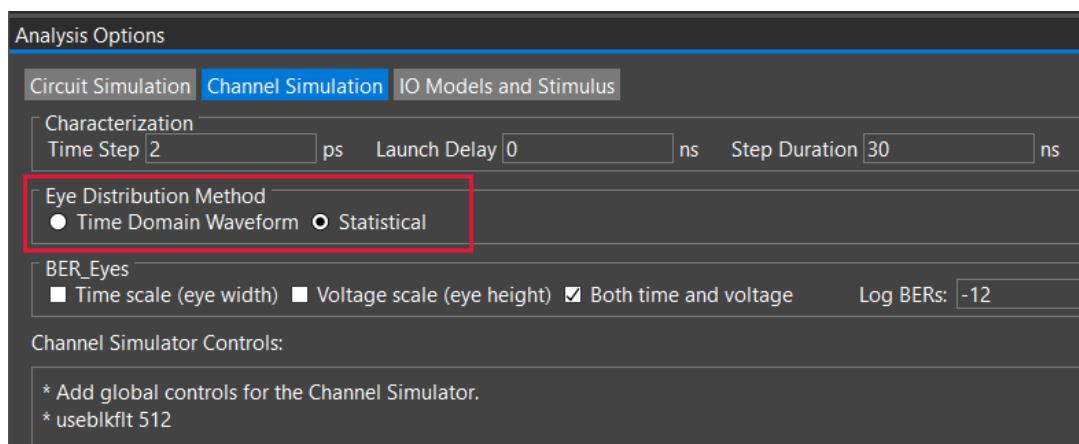
Statistical analysis capability in Topology Workbench enables using an alternative flow shown below:



This flow is identical to the previous time domain one, with one key exception; the initial eye distribution is statistically computed, as opposed to coming from raw waveforms produced by time domain simulation. From this initial eye distribution, all noise and jitter injection, as well as all post-processing, is the same.

## Enabling Statistical Analysis Method for Eye Distribution Calculation

To enable the eye distribution to be calculated statistically, in the *Analysis Options* panel, select *Statistical* as the *Eye Distribution Method*, as shown below:



## Generating Statistical Eye Contours

Serial Link Analysis has the ability to generate statistical eye contours that are referred to as *BER\_eyes*. This occurs in the post-processing section of the analysis flow (like bathtub curves generation), and can be done regardless of which method (time domain or statistical) is used to calculate the eye distribution. The significance of an eye contour computed statistically is that it represents what the eye opening would look like if a purely random bit stream of size  $1/\log\text{BER}$  was run through the channel, and is essentially another way of visualizing the jitter and noise bathtub curves. The GUI implementation for the generation of statistical eye contours enables the following:

- Ability to select which criteria to use in the statistical eye generation
- Ability to specify which BERs to generate eye contours for

This section covers the following topics:

- [Generating BER Eyes](#)
- [Specifying a List of Log BERs](#)

### Generating BER Eyes

In the Statistical Eye Distribution method, instead of eye contours produced through the time domain flow, BER eyes are generated and displayed. Therefore, specifying a choice in the *BER\_Eyes* section within the *Channel Simulation* tab of the Analysis Options panel is mandatory. The *Both time and voltage* check box in this section is selected by default. To deselect it, you need to first choose *Time scale (eye width)* or *Voltage scale (eye width)*.

#### ***Criteria for BER Eye Generation***

You can select the criteria upon which the BER eye generation should be based. The choices are:

- Time scale (eye width)
- Voltage scale (eye height)
- Both time and voltage

Selecting the time scale directs the statistical algorithm to slice and sample the eye distribution along the horizontal axis. This approach is recommended for serial links that are predominantly jitter-challenged. Alternatively, voltage scale can also be selected, in which the eye distribution will be sliced and sampled along the vertical axis. This is a good approach for serial links that are showing low eye height margins.

These two criteria are not mutually exclusive, and both can be selected together. The resulting analyses will produce statistical eyes with names such as:

- `eye_ber_1e-12.cur` > statistical eye for a BER of  $1e-12$ , based on time (jitter) scale criteria
- `eye_nber_1e-12.cur` > statistical eye for a BER of  $1e-12$ , based on voltage (noise) scale criteria

### Specifying a List of Log BERs

Within the *BER\_Eyes* section, specify the BERs that are of interest for statistical eye generation in the *Log BERs* box. This field lets you specify a single Log BER, a comma-separated list of Log BERs, and a range of Log BERs. Moving the pointer over this field shows the syntax for each of these formats.

**Note:** When *Eye Distribution Method* is set to *Statistical* in the Analysis Options form, all eye measurements that appear in reports and sweeps are automatically taken for Log BER = -12, regardless of the other Log BERs that may be specified.

## Building AMI Models for a Serial Link Topology

Serial Link Analysis workflow comes with a library of parameterized, configurable Algorithmic Modeling Interface (AMI) models for common equalization functionality, such as Feed Forward Equalization (FFE), Continuous Time Linear Equalization (CTLE), and Decision Feedback Equalization (DFE). These are used for what-if feasibility analysis, or if your Serializer/Deserializer (SerDes) supplier cannot provide you with an AMI model for the specific device used in your design.

**Note:** In the Topology Workbench – SystemSI workflows, a default control, `PostProcessDCOffset`, handles the single-ended signal measurement and coordinates with DFE. However, if the AMI model associated with a memory block contains DC voltage level control (`Vref`), you need to switch off the control in the AMI model or disable the `PostProcessDCOffset` default control in the *Analysis Options* panel. This action makes the eye contour centered.

Assignment of AMI models to implement digital signal processing techniques for signal conditioning (for example, Equalization), and clock and data recovery helps to:

- Overcome high-frequency losses in the channel component of SerDes systems
- Improve signal integrity performance of the SerDes systems

- Govern the implementation according to the requirements described in the IBIS specification

**Note:** For more information on the IBIS AMI modeling standard, see the latest IBIS specification at <http://ibis.org/specs/>.

The AMI models can be configured using the options provided in the *AMI Builder* schema of the Workflow Panel. You can also cascade the AMI Models for flexible modeling and debugging.

In addition, new and unique AMI models can be created directly in Topology Workbench using the *AMI Builder* tab in the *Create New Topology* dialog box, which can be accessed from the *Topology – New* menu.

For detailed information, see [Chapter 9, “Using the AMI Builder.”](#)

## Modeling Repeaters

Repeaters are devices that receive, recover, and re-generate serialized data at a point somewhere between the initial transmitter and final receiver of a serial link interface. This is done to improve signal quality and bit error rate (BER) of the overall interface, while enabling traditional PCB materials, long cables, and multiple connectors to be used to reduce overall system cost. From a signal integrity (SI) analysis perspective, this requires existing IBIS-AMI modeling and simulation techniques to be extended to enable multiple, cascaded channels to be simulated together for end-to-end BER analysis to be performed.

For the purposes of this appendix, a *repeater* is simply a receiver block connected to a transmitter block, effectively connecting two serial link channels together.

### Related Topics

- [Making a Repeater Connection](#)
- [IBIS-AMI Modeling for Repeaters](#)
- [Serial Link Simulations with Repeaters](#)
- [Example of a Channel Simulation with a Repeater Model](#)

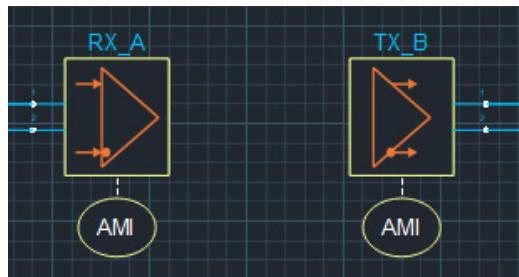
## Making a Repeater Connection

Modeling repeater devices with Topology Workbench is done by simply connecting a receiver (Rx) to a transmitter (Tx). The connection can be made with right-clicking either device and

## Topology Workbench User Guide

### Using Serial Link Analysis Workflow

selecting the appropriate shortcut menu option. Consider the following example, where the SerDes receiver of channel A is shown with the transmitter of channel B.



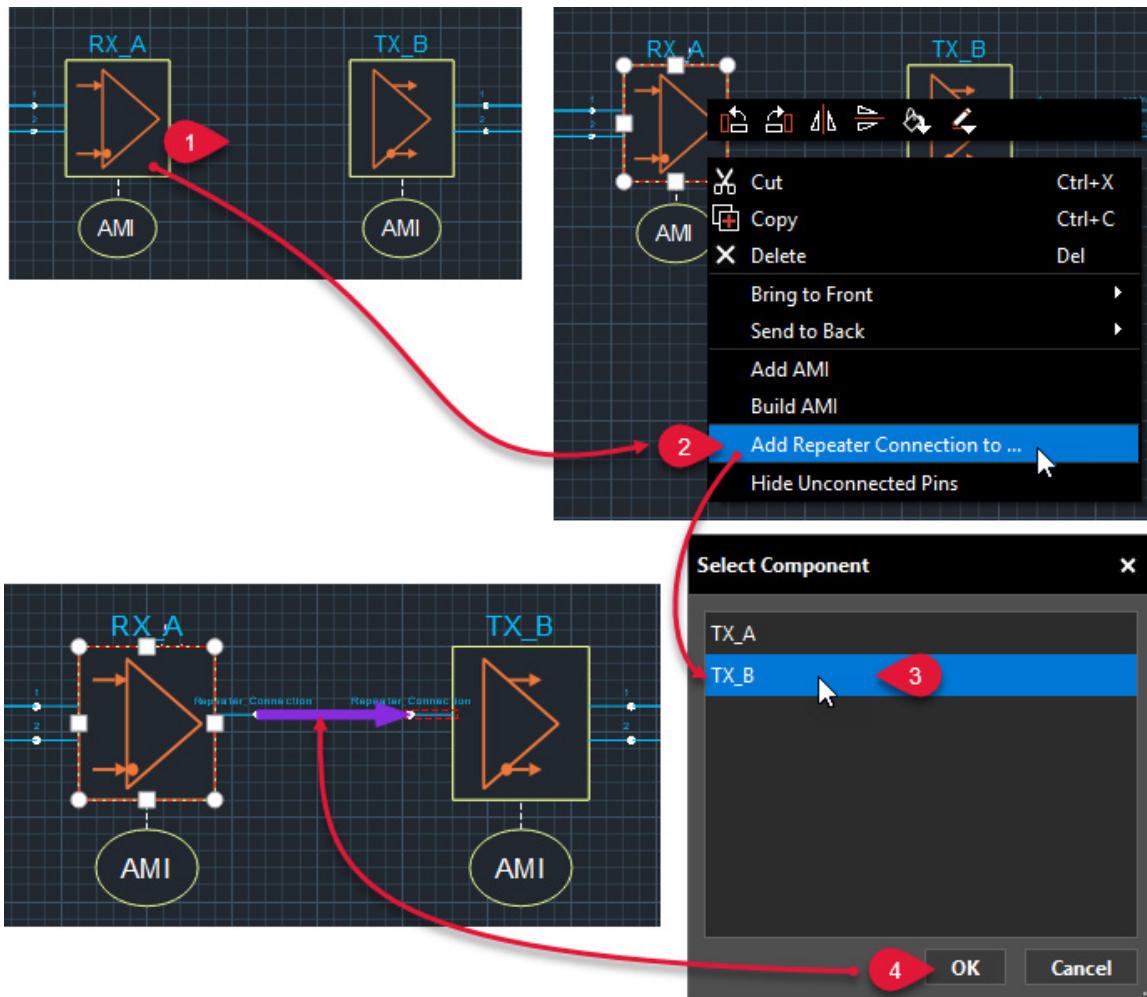
To connect the receiver and transmitter to form the repeater:

1. Right-click the receiver (*RX\_A* in this example) to display the shortcut menu.
2. Select *Add Repeater Connection to*. The *Select Component* dialog box is displayed with a name list of all transmitters that exist in the topology.
3. Select the transmitter (*TX\_B* in this example) from the list.

## Topology Workbench User Guide

### Using Serial Link Analysis Workflow

- Click OK. This forms a repeater connection between the two selected block as shown in the following diagram:



**Note:** The combination of the receiver (*RX\_A*) and transmitter (*TX\_B*) forms the overall repeater device.

## IBIS-AMI Modeling for Repeaters

As shown in diagram above, IBIS-AMI models can be directly used to form the repeater device. These models are fully IBIS compliant, and require no special syntax or specification. The functionality to cascade the serial links together into one overall simulation is handled directly by Topology Workbench.

Analog circuit models for the input stage of the *Rx* and output stage of the *Tx* are required. These are identical to those used in Topology Workbench for traditional, non-repeater

simulations. Repeaters also typically contain equalization, such as FFE, CTLE, CDR, and DFE, which are conveniently represented by algorithmic modeling, represented by the AMI bubbles. The model developer can build the repeater's equalization functionality into a single algorithmic model, or into 2 algorithmic models, as is the case in the figure. If only one algorithmic model is used, it can be associated with either the receiver or the transmitter block.

The fundamental requirement is that whatever equalization techniques and functionality are present in the repeater device, they must be represented in their algorithmic models. For example, if the repeater does a complete recovery and regeneration of the received signal, and resets the timing budget, this must be represented in the algorithmic model(s). Also, any amplitude scaling that is required between the receiver's waveform and the input to the transmitter, must also be accounted for. Device-specific jitter and noise injection can be handled in the algorithmic model as *Model\_Specific* AMI parameters. Jitter and noise injection can also be handled by Topology Workbench.

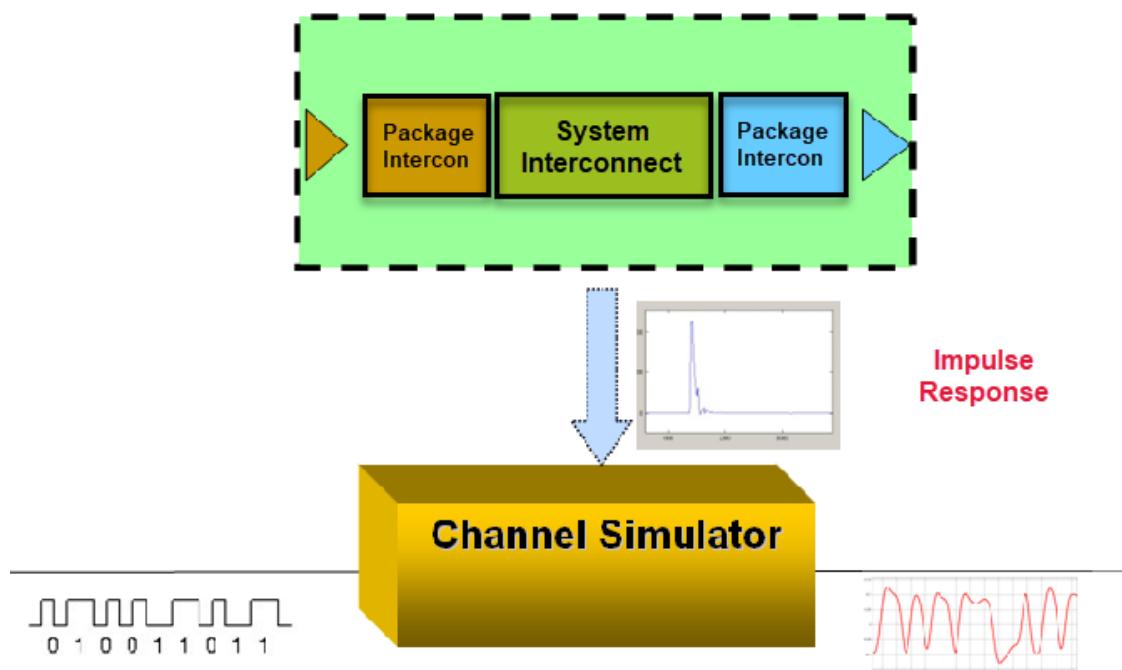
## **Serial Link Simulations with Repeaters**

The basic premise in simulation of serial links connected with repeaters is that the analog waveforms from the receiver of the first channel are fed in as the input stimulus for the next channel, effectively cascading them together. This is illustrated in the following sections:

- [Standard Channel Simulations](#)
- [Channel Simulations with Repeaters](#)

## Standard Channel Simulations

Time domain simulations of serial links involves convolving an input bit stream with the impulse response of the channel, producing waveforms at the receiver. This is illustrated in the following figure.

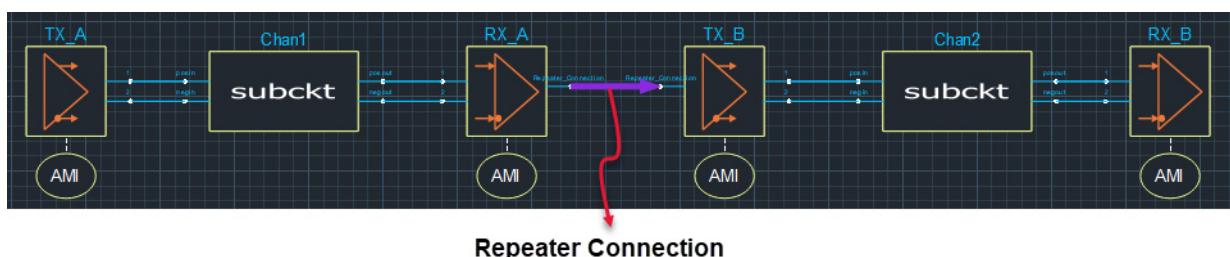


**Note:** The input bit stream in this figure is synthesized directly by Topology Workbench for the simulation and is essentially a digital waveform.

## Channel Simulations with Repeaters

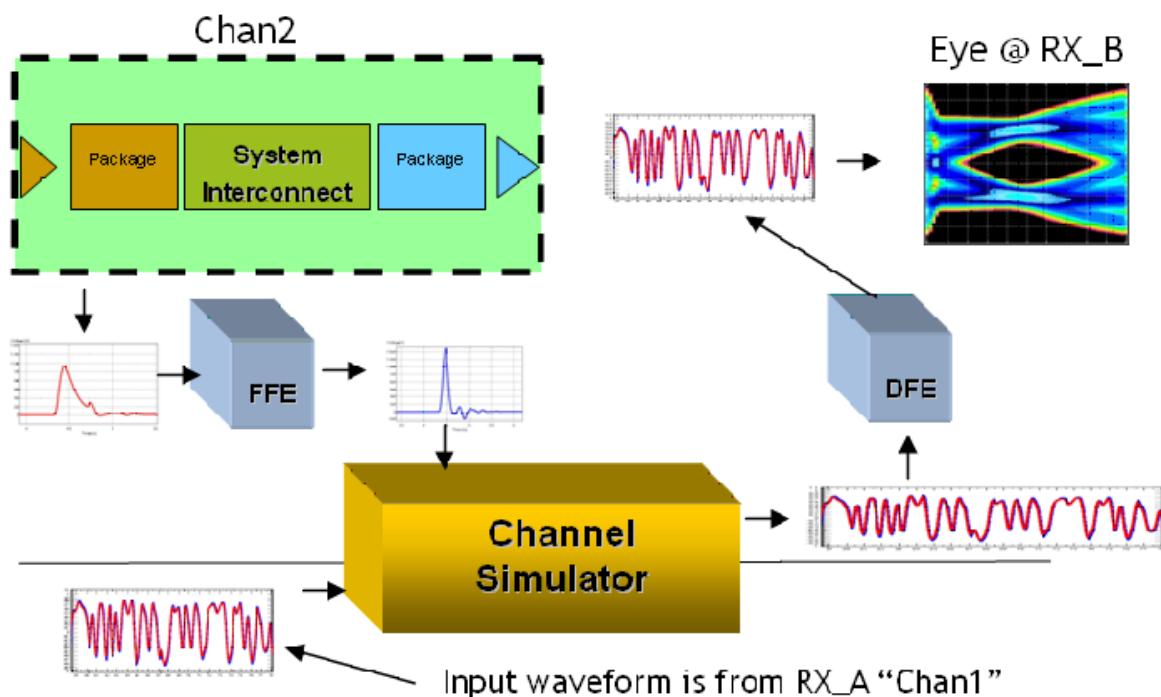
Now consider serial link simulations with a repeater connecting multiple channels together.

The default template, *repeater\_simple*, shipped with Topology Workbench creates the topology shown below.



In this topology, *Chan1* is connected to *Chan2* through a repeater device. The simulation for *Chan1* is the standard process as described in the previous section. The simulation for *Chan2* also uses the same process, except that the digital waveform synthesized by Topology Workbench is not used as input. Instead, the output waveform from *Chan1* is the input waveform for *Chan2*.

In this case, the raw analog waveform produced for receiver *RX\_A* (including any algorithmic model functionality) is provided directly as the input waveform to transmitter *TX\_B*, as shown below.



The input waveform for *Chan2* is the resulting waveform from the simulation of *Chan1*, rather than a digital waveform synthesized by the tool. This technique enables an unlimited number of channels to be cascaded together by repeaters.

## Example of a Channel Simulation with a Repeater Model

This section uses the repeater template referenced previously as a working example. This is covered in the following sections:

- [Reviewing Simulation Results with Repeaters](#)
- [Repeater Algorithmic Model](#)

# Topology Workbench User Guide

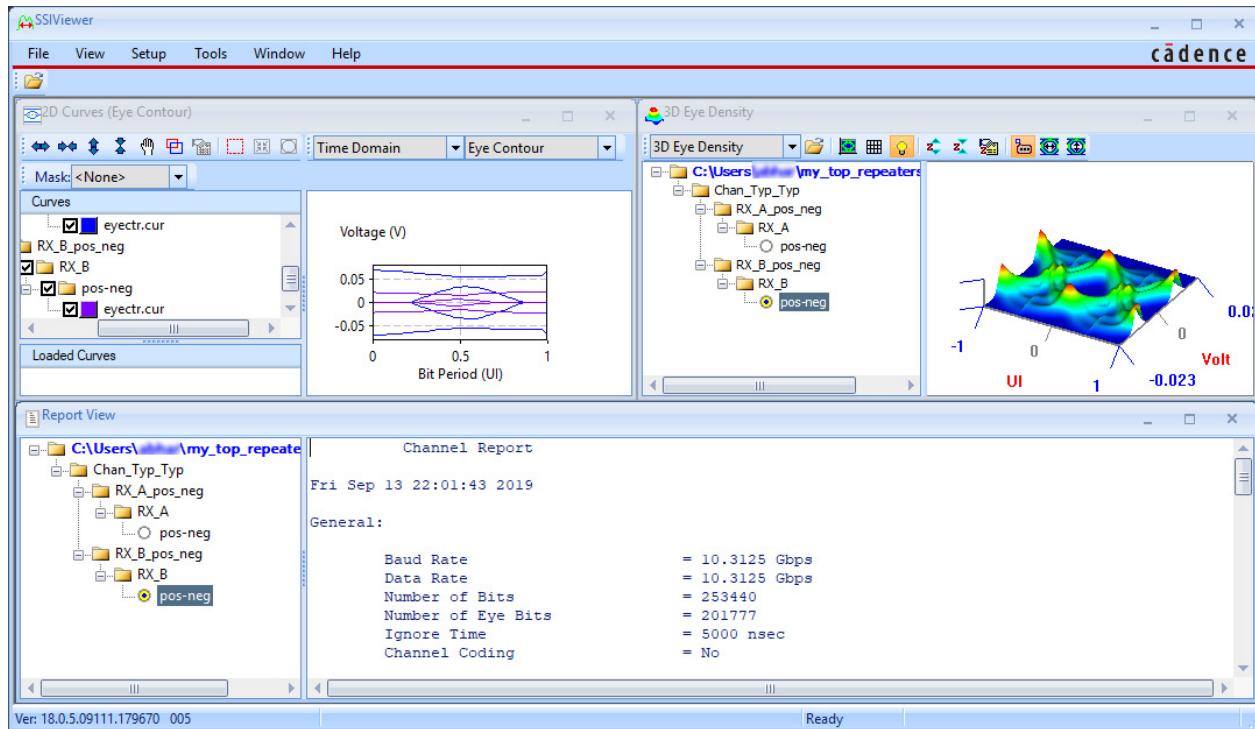
## Using Serial Link Analysis Workflow

### Reviewing Simulation Results with Repeaters

Topology Workbench runs two characterizations for this topology—one for the channel from *TX\_A* to *RX\_A*, and the other for the channel from *TX\_B* to *RX\_B*. Then, two consecutive channel simulations are run, one for each channel. The first channel is simulated in the standard manner, in which Topology Workbench synthesizes the desired digital input waveform for *TX\_A*. For the second channel, the output waveform from *RX\_A* as provided as the input waveform to *TX\_B*.

As the simulation progresses, the *Real Time Plot* panel shows to you the eye contour and DFE Tap plots.

At the end of the simulation, two complete sets of results, one for each receiver, are generated as shown below.



### Repeater Algorithmic Model

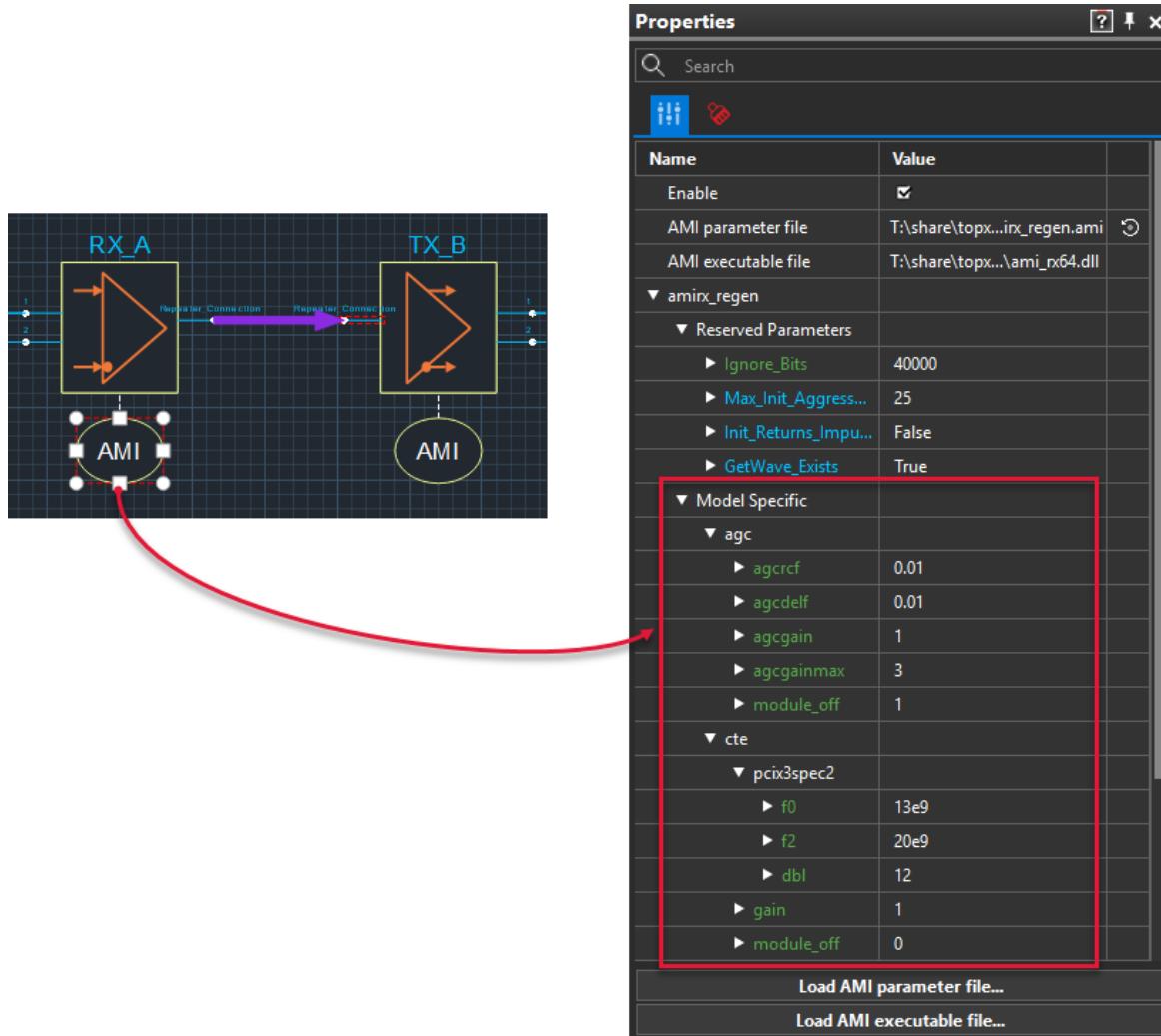
The *repeater\_simple* template has a repeater model included in the template. In the following figure, the transmitter model for the repeater is the standard FFE algorithmic model from the Topology Workbench library, with no special repeater functionality. However, the receiver model used for the repeater example does have some repeater-specific functionality, described in this section.

## Topology Workbench User Guide

### Using Serial Link Analysis Workflow

To view the AMI model associated with the receiver attached to the repeater, double-click the corresponding AMI block. In the Property window, the location of the attached AMI parameter file is listed as:

```
<INSTALL_DIR>\share\topxp\amiwin\amirx_regen.ami
```



If you open this AMI file in a text editor, you will notice a number of embedded comments that explain document contents.

When you double-click the AMI block attached to the Rx block, the *Model Specific* section of the AMI file can be examined from the *Edit Properties* panel. This section is organized into several different parts, such as, AGC, CTE, DFE, and regeneration parameters.

Of these, one of the CDR parameters, `meas_delay` is used in repeater applications. The `meas_delay` parameter defines the time delay after which CDR starts sampling. In this example topology, there are two CDR functions. One is for the repeater receiver, RX\_A, and

the second is embedded in the `DFE` block for the algorithmic model associated with receiver `RX_B`.

When multiple algorithmic models with CDR functions from the AMI library are utilized together in the same topology, the downstream model –AMI model associated with `RX_B` – needs to have its `meas_delay` parameter set for a greater value than the upstream CDR – AMI model associated with `RX_A`. This enables the eye to be properly centered for evaluation.

Another parameter in the `.ami` file, which is of relevance to repeaters, is `dfe_regenerate`. Turning this parameter on produces a complete regeneration of the recovered signal, restoring amplitude and removing any jitter or distortion.

## Working with Compliance Kits

Topology Workbench provides a set of standard built-in compliance kit templates for high-speed SerDes designs. Using these compliance kits, you can automate the compliance testing process and speed up the design process.

In addition, in the Serial Link Analysis (SLA) and Compliance Kits workflows, you have the option to create your own customized compliance kits to suit your design requirements.

For details, see the following sections:

- [Using the Standard Built-In Compliance Kits](#)
- [Creating Customized Compliance Kits](#)

## Using Extracted Interconnect Models in Serial Link Analysis

The Layout Association functionality in Topology Workbench provides direct integration with PowerSI and SPEEDEM Generator (SPDGEN), enabling automation in the extraction and model generation for blocks in Topology Workbench topologies that are based on physical layout.

For details, see [Appendix D, “Using Extracted Interconnect Models from Layout.”](#)

## Using Pre-Layout Transmission Line Modeling Capability

Topology Workbench includes the pre-layout transmission line (TLine) modeling capability. You can use a W-Element TLine model in place of an S-Parameter model of the differential traces, assigned to the Channel block.

Also, you use separate via models connected to the W-Element transmission line model of the differential traces for the purpose of exploring effects of vias on the signal integrity performance of the serial link system.

For details, see [Appendix C, “Modeling Pre-Layout Transmission Lines.”](#)

## Creating Extraction-Based Crosstalk Topologies

Extraction-based crosstalk topologies are built from interconnect circuits that are produced using extraction software, typically operating on a physical layout for a printed circuit board (PCB) or package. When multiple drivers and receivers are included in a topology, you can include crosstalk effects into Channel Analysis. With this type of multi-receiver topology, it is important that you identify the primary receiver.

For details, see [Appendix F, “Incorporating Crosstalk for Channel Analysis.”](#)

## Running Sweep Simulations

The *Sweep Manager* allows multiple values to be set for key parameters in the topology. Sweeping then will automatically run multiple simulations, substituting in the relevant parameter values for each unique simulation run. Results can then be analyzed to understand the impact of the parameter values on overall performance.

For details, see [Appendix E, “Using the Sweep Manager.”](#)

## Setting Up Constraints for Serial Link Analysis

In SLA workflow, you can define constraints in a topology project as an Electrical Constraint Set (ECSet), which applies to each net, and then import them to Constraint Manager.

For details, see [Chapter 11, “Exporting Constraints from a Topology.”](#)

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## Using Parallel Bus Analysis Workflow

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The Parallel Bus Analysis (PBA) workflow of Topology Workbench allows you to model, simulate, analyze, and evaluate signal integrity performance of parallel bus systems. You can connect the blocks using wire and/or block-based connection schemes.

You can also use advanced bus characterization for parallel bus analysis. By default, Xtalk is included in bus characterization, but you can capture Xtalk on individual signal basis by choosing to invert all aggressor stimulus, using aggressor stimulus as defined, or using random aggressor stimulus.

The bus simulations can be run using circuit and channel simulators for blocks with ideal or non-ideal power supplies. The SSIViewer window provides a unified platform for waveform and S-Parameter viewer.

### ***Related Topics***

- [Analyzing Parallel Buses](#)
- [Analyzing Parallel Bus Topologies with Channel Simulation Techniques](#)
- [Configuring the Blocks for Parallel Bus Analysis](#)
- [Augmenting an IBIS File](#)
- [Simulating Circuits That Use S-Parameter Model](#)
- [Using DDR Measurement Reports](#)
- [Building AMI Models for a Parallel Bus Topology](#)
- [Using Extracted Interconnect Models in Parallel Bus Analysis](#)
- [Running Sweep Simulations](#)
- [Setting Up Constraints for Parallel Bus Analysis](#)

## Analyzing Parallel Buses

In PBA workflow, you can perform block-based or wire-based analysis of high-speed parallel bus systems that consist of chip, package, PCB, and interconnects. Topology Workbench can be used for efficient design-oriented time domain simulations.

Using the information discussed in this section, you can model a simple parallel bus system (SPBS), with the ideal power supply. You will be using the built-in application-specific blocks that are available in the [Floating Toolbar](#) of Topology Workbench. Next, you will assign electrical models to the SPBS blocks and then perform time-domain simulations.

To perform parallel bus analysis:

1. Start Topology Workbench using a method described in the [Starting Topology Workbench](#) topic.

**Note:** When you open Topology Workbench in standalone mode, choose *Advanced SI* from the *Cadence Product Choices* dialog box to run PBA workflow.

2. Create a topology project for the PBA workflow.

For steps, refer to the [Creating a Topology Project from Scratch](#) section or the [Opening an Existing Topology Project](#) section.

When you create a new topology project,

- a. Specify a *Topology Name* and browse the *Topology Path* to save your topology.
- b. Click the *SystemSI* tab. The *Parallel Bus Analysis* sub-tab is opened by default in a new session; otherwise, click it to display the list of the following default PBA workflow-specific templates for choice:

Template	Description
<i>addr_bus_welem_4mem</i>	Contains an address bus that connects four memories with W-Elements.
<i>data_bus_sparam_2mem</i>	Contains a data bus that connects two memories with S-parameters.
<i>data_bus_welem_2rank</i>	Contains a data bus that connects two memory ranks with W-Elements.
<i>data_bus_welem_vrm</i>	Contains a data bus with non-ideal power using W-Elements.

## Topology Workbench User Guide

### Using Parallel Bus Analysis Workflow

<code>pba_simple_em</code>	Contains a simple data bus example using IBIS [External Model] syntax.
----------------------------	--

You can select one of the default templates or the *<blank topology>* row to start designing your own topology from scratch.

The Topology Workbench window is refreshed as following:

- A tab with the given *Topology Name* opens next to the [Start Page](#).
- The [Layout Canvas](#) is populated with the blocks as per the selected default template. If you chose to create a *<blank topology>*, the canvas is blank.
- The [Workflow Panel](#) opens with a list of tasks you need to perform during the selected type of analysis.
- The [Floating Toolbar](#) opens with a list of various types of blocks that can be used in the selected type of analysis.

**3.** Add and place the required blocks on the canvas.

For information, see [Adding Blocks to the Canvas](#) and [Appendix A, “Choosing Blocks to Place on the Canvas.”](#)

**4.** Connect the blocks on the canvas and configure the connections between their signals.

For information, see [Connecting the Blocks on the Canvas](#) and [Managing Connections Between Blocks and Signals](#).

**5.** Edit and configure the properties of the various components placed on the canvas by using the [Edit Properties Panel](#).

For information, see [Editing the Properties of a Component](#).

**6.** Assign device models to the controller and memory devices using the [Edit Properties](#) panel. For detailed information, refer to the following sections:

- [Assigning and Editing IBIS Models](#)
- [Assigning and Extracting S Parameter Files](#)

**7.** Setup and manage the component model libraries.

For information, see [Setting Up Component Model](#).

**8.** Click *Check Connectivity* in the *Simulation Setup* schema to:

- Open the *Connectivity Checker* panel.

## Topology Workbench User Guide

### Using Parallel Bus Analysis Workflow

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- Check whether the connectivity between the blocks is error-free.

For information, see [Checking Connectivity Between Blocks and Signals](#).

**9.** Click *Set Timing Budget* in the *Simulation Setup* schema to:

- Open the *Timing Budget* panel.
- Set up timing specifications associated with the transmitting component.

For information, see [Setting Up Timing Specifications](#).

**10.** Click *Set Analysis Options* in the *Simulation Setup* schema to:

- Open the *Analysis Options* panel.
- Set up the basic simulation settings such as signals to be simulated, simulator to be used, simulation configuration, and simulation name in the *Circuit Simulation*, *Bus Simulation*, *Channel Simulation* (displayed when the *Use Channel Simulator* check box is selected), and *IO Models and Stimulus* tabs.

For information, see [Setting Up Simulation Options – Introduction](#), [Circuit Simulation](#), [Bus Simulation](#), [Channel Simulation – Parallel Bus Analysis](#), and [IO Models and Stimulus – Parallel Bus Analysis](#).

**11.** Click *Terminate Unconnected Pins* in the *Simulation Setup* schema to set up termination of all unconnected pins in the topology.

For information, see [Terminating Unconnected Pins](#).

**12.** Setup probe points, if needed, to view simulation results at specific points in the design. For this, use the *Probe Points* panel that can be accessed from the *Setup – Probe Points* menu.

For information, see [Setting Up Probe Points](#).

**13.** Click *Save Topology* in the *Simulation Setup* schema.

**14.** Select the *Enable Distributed Computing* check box in the *Distributed Computing Setup* schema to run the simulation across a collection of computer systems using distributed computing. This step enables the *Set up Computer Resources* option in the schema.

For information, see [Setting Up Distributed Computing Options](#).

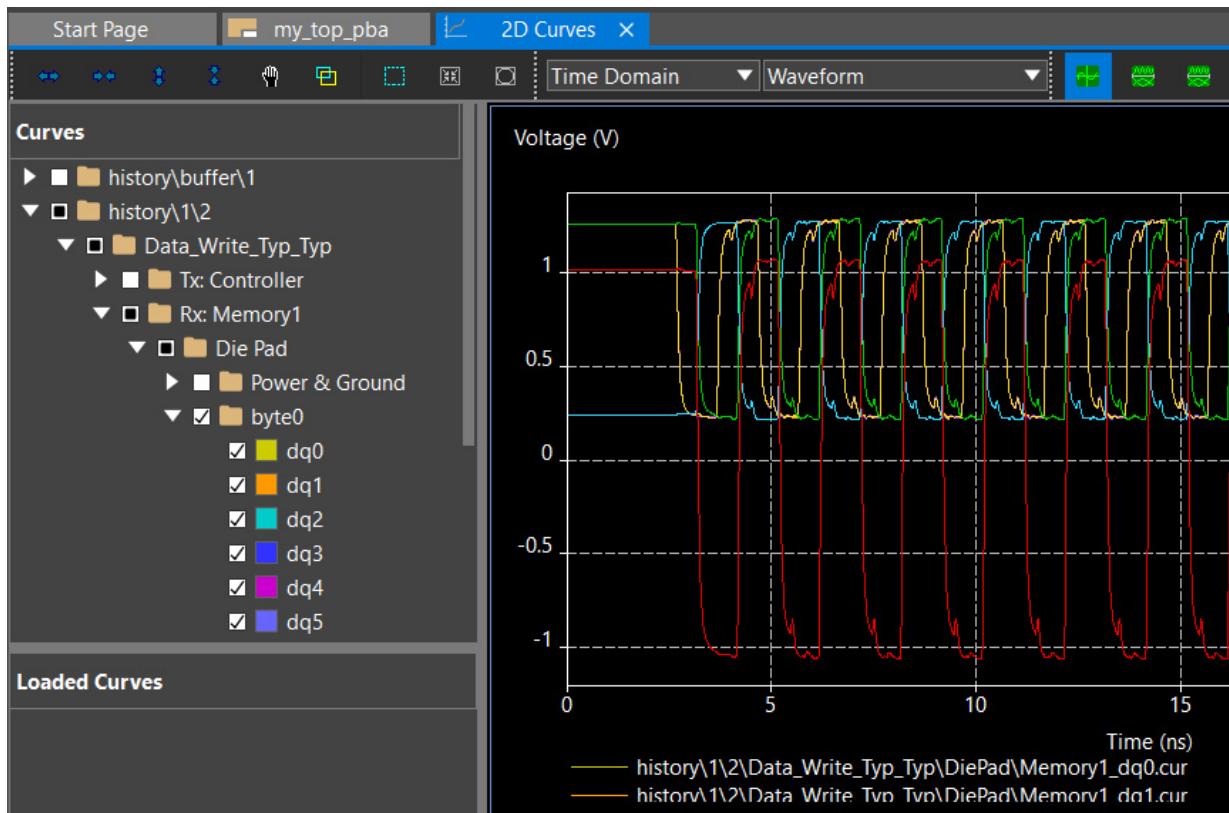
**15.** Click *Start Bus Simulation* in the *Simulation* schema to run the simulation.

For information, see [Running the Simulation](#) and [Monitoring a Simulation Run in Parallel Bus Analysis](#).

## Topology Workbench User Guide

### Using Parallel Bus Analysis Workflow

After the completion of the simulation run, the 2D Curves tab, as shown below, opens with the plotted waveform results. For information, see [Viewing Simulation Results](#).



For additional features available in PBA workflow, see [Related Topics](#) below.

#### ***Related Topics***

- [Browsing Simulation Results](#)
- [Setting Up Component Model](#)
- [Switching to Another Workflow](#)
- [Customizing a Workflow](#)
- [Creating Custom Templates](#)
- [Using the AMI Builder](#)
- [Archiving a Topology](#)

## Setting Up Timing Specifications

In the Parallel Bus Analysis workflow, an integrated tool automatically calculates the worst-case setup and hold values from the user-defined data set. The timing specifications associated with the transmitting component enables worst-case phase shifts to be applied on the timing reference signal to simulate worst-case timing conditions. On the other hand, the timing specifications associated with the receiving component allow final timing margins to be computed.

To set timing specifications for a project:

1. Open the *Timing Budget* panel using one of the following methods:

- Click *Set Timing Budget* from the *Simulation Setup* section in the Workflow panel.  
*-or-*
- Click *Tools – Timing Budget* from the menu bar.

2. Choose an appropriate *Bus Type* from the list.

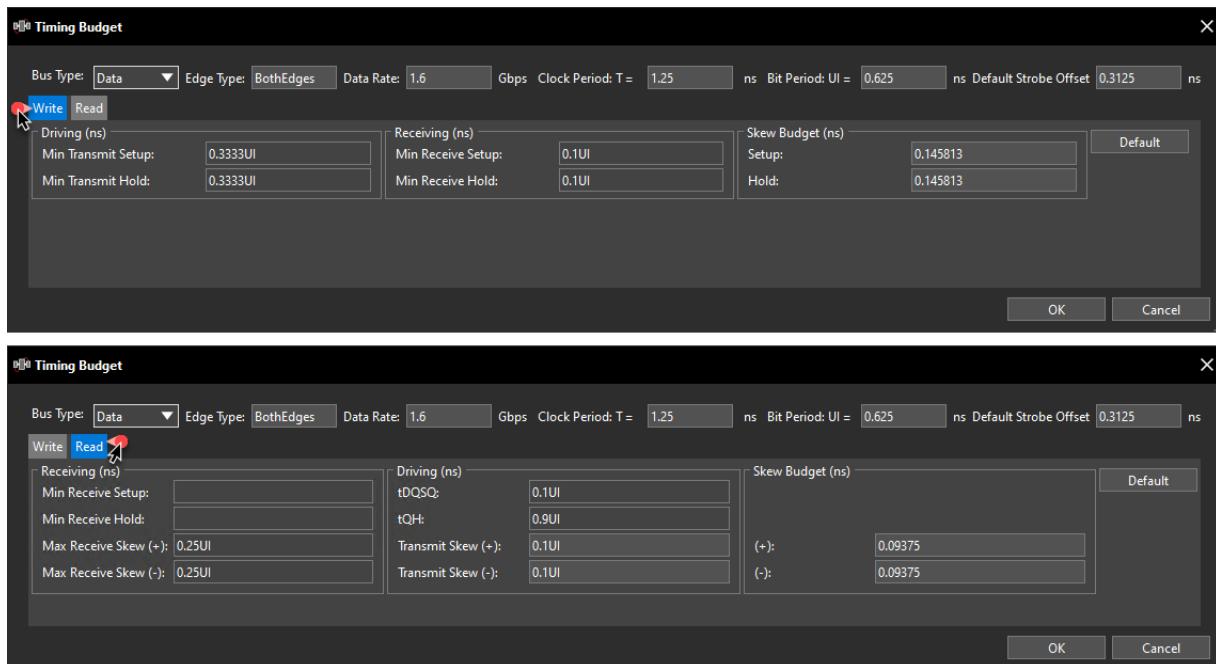
When you select *AddCmd* as the *Bus Type*, the desired setup and hold values can be specified manually in the *Driving* and *Receiving* sections or by clicking the *Default* button. Based on the specified values, the fields in the *Skew Budget* section are populated with automatically calculated values in the read-only *Setup* and *Hold* fields.

When you select *Data* as the *Bus Type*, the *Write* and *Read* tabs are displayed, as shown below, with *Driving*, *Receiving*, and *Skew Budget* sections for setting the setup

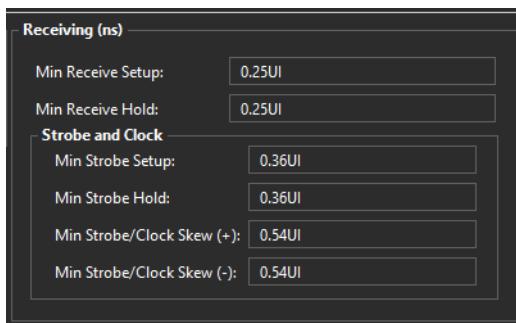
# Topology Workbench User Guide

## Using Parallel Bus Analysis Workflow

and hold values for write and read simulations. For details about the parameters that can be set on these two tabs, see [Defining the Timing Parameters](#).



**Note:** If the *Data* bus in the design has a defined and connected clock signal, for all write simulations, the *Strobe and Clock* subsection is added to the *Receiving* section as shown below. This subsection allows you to measure the timing margin between the clock and data strobe signal.



To understand the impact of different timing parameters on different types of buses, refer [Appendix G, "Setting Timing Parameters in Topology Workbench."](#)

## Defining the Timing Parameters

In the *Timing Budget* panel, the following timing parameters are available for setting based on *Write* or *Read* case:

For the **Write** case (applies to *Data*, *AddCmd* and *Ctrl* buses)

Lets you set the following *Driving* and *Receiving* parameters:

### *Min Transmit Setup*

This is the minimum amount of setup time that is guaranteed to exist between the signals and their timing reference at the driving component, that is, the *Controller*.

### *Min Transmit Hold*

This is the minimum amount of hold time that is guaranteed to exist between the signals and their timing reference at the driving component, that is, the *Controller*.

### *Min Receive Setup*

This is the amount of setup time required between the signals and their timing reference at the receiving component, that is, the *Memory*. This is typically given in data sheets as *tDS(base)* for *Data* buses and *tIS(base)* for *AddCmd* buses.

### *Min Receive Hold*

This is the amount of hold time required between the signals and their timing reference at the receiving component, that is, the *Memory*. This is typically given in data sheets as *tDH(base)* for *Data* buses and *tIH(base)* for *AddCmd* buses.

The *Skew Budget* is automatically calculated from the parameters described above, and is intended to show how much skew can be introduced by the interconnect while still meeting the timing requirements. The values are calculated as follows:

- *Setup (Skew Budget)* = *Min Transmit Setup – Min Receive Setup*
- *Hold (Skew Budget)* = *Min Transmit Hold – Min Receive Hold*

The *Default* button can be used when data sheets or timing specifications are not available. Using this button populates these fields with typical values by allocating one third of the *Signal Bit Period* for *Transmit Setup/Hold* and one quarter of the *Signal Bit Period* for *Receive Setup/Hold*.

## Topology Workbench User Guide

### Using Parallel Bus Analysis Workflow

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For the **Read** case (applies for only *Data* buses)

Lets you set the following *Receiving* and *Driving* parameters:

Min Receive Setup

Min Receive Hold

**Max Receive Skew (+)**

This is the maximum amount by which the *Data* is allowed to lag the *Strobe* at the receiving component, that is, the *Controller*.

**Max Receive Skew (-)**

This is the maximum amount by which the *Data* is allowed to lead the *Strobe* at the receiving component, that is, the *Controller*.

**Transmit Skew (+)**

This is the maximum amount that the *Data* will lag the *Strobe* signal at the driving component, that is, the *Controller*. This is derived from the *tDQSQ* parameter commonly found in data sheets for the *Memory*.

**Transmit Skew (-)**

This is the maximum amount that the *Data* will lead the *Strobe* signal at the driving component, that is, the *Controller*. This is derived from the *tQH* parameter commonly found in data sheets for the *Memory*.

The *Skew Budget* is automatically calculated from the parameters described above for both the leading and lagging case, and is intended to show how much skew can be introduced by the interconnect while still meeting timing requirements. These are calculated as follows:

- (+) (Skew Budget) = *Max Receive Skew (+)* – *Transmit Skew (+)*
- (-) (Skew Budget) = *Max Receive Skew (-)* – *Transmit Skew (-)*

The *Default* button can be used when data sheets or timing specifications are not available. Using this button populates these fields with typical values by allocating one tenth of the *Signal Bit Period* for *Transmit Skew* and one quarter of the *Signal Bit Period* for *Receive Skew*.

## Analyzing Parallel Bus Topologies with Channel Simulation Techniques

PBA workflow provides you access to the following features if you select the *Use Channel Simulator* check box in the *Simulation Setup* schema of the *Workflow* panel:

- Perform channel simulations for LPDDR4 and DDR4 Data buses, Ctrl bus, and AddCmd bus as well when *Start Bus Simulation* is clicked in the *Simulation* schema of the *Workflow* panel.
- Specify *Launch Delay*, *Step Duration*, *VMeas*, *Bus Stimuli*, *Seed Control*, and *Channel Simulator Controls* in the Channel Simulation – Parallel Bus Analysis tab that is added to the *Analysis Options* panel.
- Define jitter and noise injection parameters for the strobe and data signals in the Stimulus Definition and Model Selection section of the *Analysis Options* panel.
- Add, build, and assign AMI models to the Controller block as described in [Chapter 9, “Using the AMI Builder.”](#)
- Correlate the simulation results for the circuit and the channel using the *Correlate Circuit/Channel Sims* option that gets enabled in the *Simulation* schema of the *Workflow* panel. See [Correlating Circuit and Channel Simulations](#).
- Characterize the channel and review the results before running the channel simulation. See [Running and Reviewing Characterization](#).
- Simulate crosstalk on a victim line in the bus. For this, ensure that you disable one of the DQ lines by editing its *Stimulus Pattern* to zero in the *Analysis Options* panel, then re-simulate and see the coupled noise voltage on the victim line.

### Running and Reviewing Characterization

Characterization of a parallel bus captures the bus behavior through a circuit simulation. To start the characterization run:

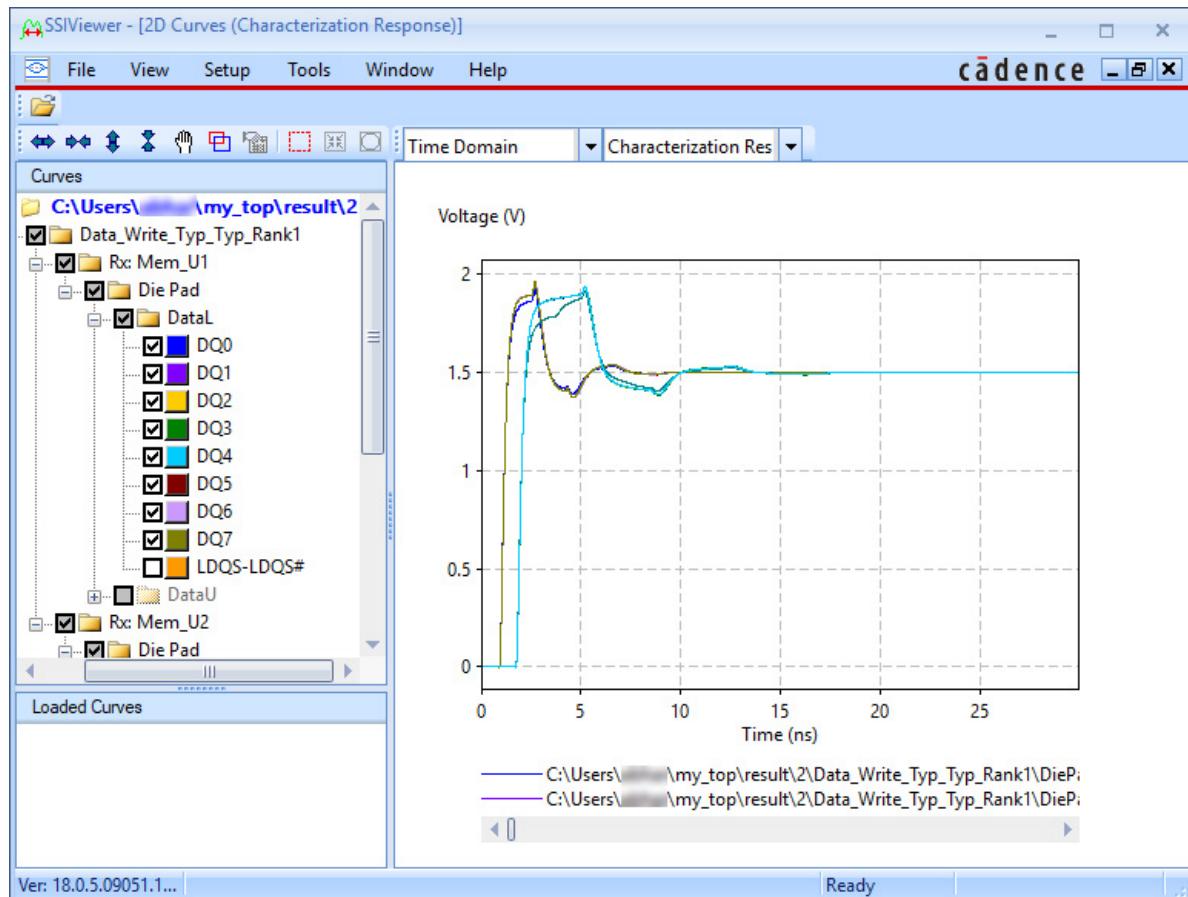
- Click *Run & Review Characterization* from the *Simulation* schema in the *Workflow* panel.

**Note:** If characterization has been run once, you need not repeat it unless the channel topology changed.

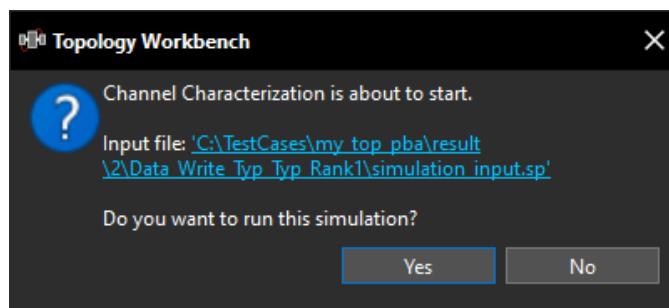
## Topology Workbench User Guide

### Using Parallel Bus Analysis Workflow

On completion of the characterization run, the *2D Curves* tab opens with the *Characterization Response* waveform displayed for further analysis, as shown below:



You can choose to characterize the channel along with the bus simulation. In such a scenario, for a control over each simulation run, you can select *Setup – Pause before Simulation* from the menu bar. A message such as following then prompts you to confirm whenever a new simulation is about to start and provides a link to open the input file for editing:



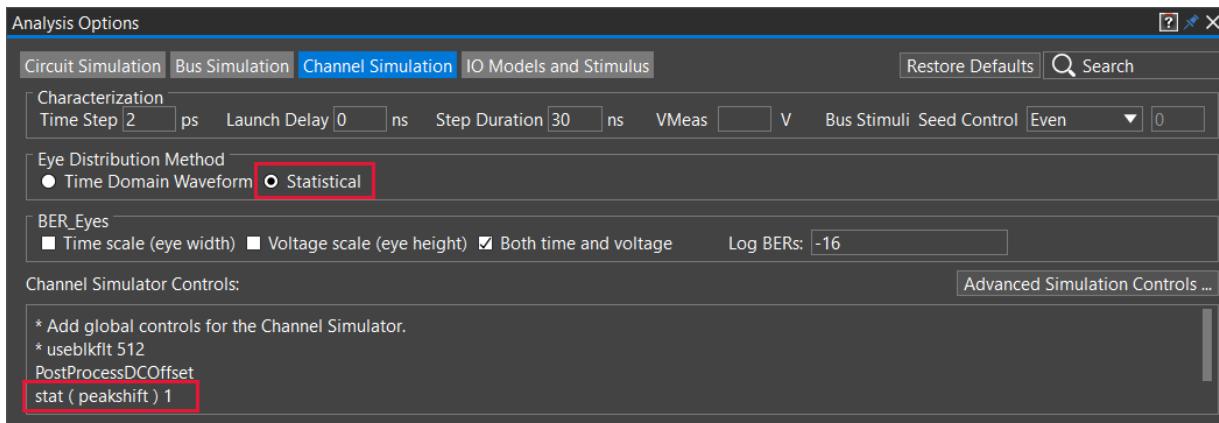
# Topology Workbench User Guide

## Using Parallel Bus Analysis Workflow

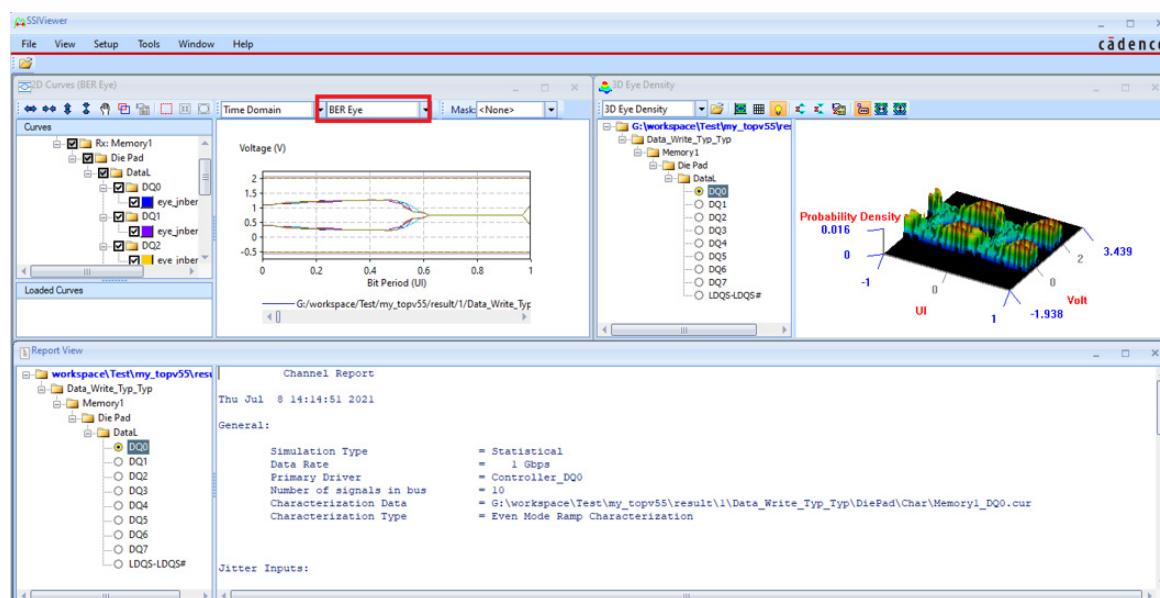
### Running Statistical Channel Simulation

To run statistical channel simulation in the SystemSI – Parallel Bus Analysis workflow, ensure to do the following:

- Select the *Use Channel Simulator* check box in the *Workflow* panel.
- In the *Channel Simulation* tab of the *Analysis Options* panel:
  - Set the *Eye Distribution Method* as *Statistical*.
  - Set `stat ( peakshift x )` in the *Channel Simulator Controls* box to adjust the eye contour position. The value of `x` can be 0, 1, or 2.



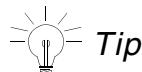
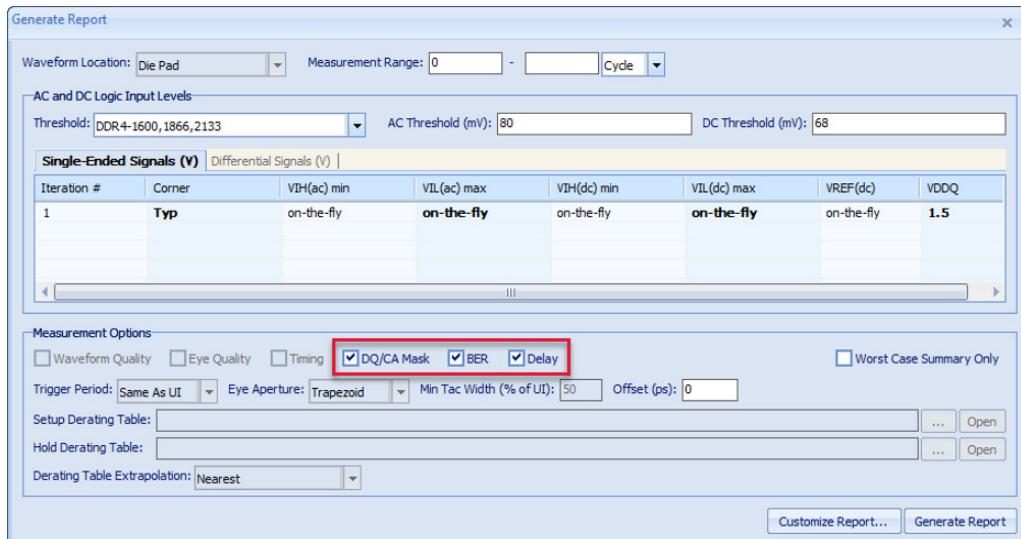
- Set *BER Eye* as default in the 2D Curves view when loading statistical result.



## Topology Workbench User Guide

### Using Parallel Bus Analysis Workflow

- Enable the *DQ/CA Mask*, *BER*, and *Delay* measurement for statistical result in the *Generate Report* dialog box.



The *Generate Report* dialog box opens when you right-click a top-level node in the *Curves* pane of the SSIViewer window and click *Generate Report* from the shortcut menu.

## Configuring the Blocks for Parallel Bus Analysis

For parallel bus analysis, you can:

- Instantiate the required types of blocks on the canvas and connect them to form a wired topology. The blocks can be chosen from the Floating Toolbar.  
See Appendix A, “Choosing Blocks to Place on the Canvas.” for the complete range of blocks that can be used in PBA workflow.
- Edit the properties of a block in the *Component Properties* tab ( ) of the Edit Properties Panel as described in the Editing the Properties of a Component section.

To know more about configuring a few commonly used blocks in PBA workflow, see:

- IBIS-Based Controller or Memory Block
- SPICE-Based Controller or Memory Block
- EBD Block

- [S Parameter Block](#)
- [Subcircuit Block](#)
- [Layout Block](#)
- [VRM Block](#)
- [Trace Block](#)

## IBIS-Based Controller or Memory Block

The controller and memory blocks can be of two types – with an IBIS model or with a SPICE subcircuit.

Though you can add multiple memory blocks, only one controller is allowed in the topology.

You cannot have a mix of IBIS-based and SPICE-based memory blocks in a topology. Therefore, if you have added a Memory IBIS block, you will be allowed to add more Memory IBIS blocks only. The option for Memory SPICE block will then be disabled in the *Add Block* panel. For information about assigning an IBIS model to the Controller IBIS and Memory IBIS blocks, see [Assigning and Editing IBIS Models](#).

In the *Component Properties* tab of the [Edit Properties Panel](#) for a Controller IBIS or a Memory IBIS block, the *OnDie Parasitics* and *Package Parasitics* check boxes can be used specify the Die and Package models, respectively. These can be separate model files, such as a PKG file, or simply the RLC package parasitics that are already included in the IBIS model.

To view the pin model in the IBIS file, select the *Model Type* as *Pin RLC* and click the *View Package Parasitics* button. The *Subcircuit Editor* opens with corresponding details displayed for review. You cannot update this definition in the *Subcircuit Editor*.

If you select the *Pin RLC* or *Package Model* option, then both Die pad and Pkg Pin (ball) waveforms get created after the simulation run.

For Parallel Bus Analysis, the *Ignore VT Curves* option is not selected by default. This is to ensure that during analysis, the simulator takes into account the non-linear behavior of the drivers by reading the VT data.

## Multi-Pin Connectivity for Controller and Memory IBIS Blocks

This section details the rules or the guidelines followed by Topology Workbench for generating multi-pins.

1. In the *Load IBIS* dialog box, if the *Explicit IO Power and Ground Terminals* check box is not selected, the *Ckt Node*, *Net*, and *Pin* in the *Connection Definition* panel are determined by the *Pin Mapping* section of the IBIS component.
  - ❑ The values in the *Ckt Node* and *Pin* columns are the same, and are read from the *Pin* column in the *Pin Mapping* tab of the *Load IBIS* dialog box.
  - ❑ The values in the *Net* section of the *Connection Definition* panel are the same as the values in the *Signal Name* column in the *Pin Mapping* section of the *Load IBIS* dialog box.
2. If the *Load IBIS* dialog box has the *Explicit IO Power and Ground Terminals* check box selected, in the generated multi-pins, each signal has its corresponding power and ground. The multi-pin connectivity is generated in the *Connection Definition* panel using following rules:
  - ❑ In case of a regular signal, the *Ckt Node* value is same as the *Signal Name* in the *Pin Mapping* section.
  - ❑ For the corresponding power signals, the values in the *Ckt Node* and *Pin* columns are the same, and these are derived by combining the signal Net and power Net.
  - ❑ Similarly, for the *Ground* of the signal, the *Ckt Node* and *Pin* values are the same, and these are derived from the signal Net and the ground Net.
3. You can click *Ckt Node* of the Controller/Memory block to sort the *Ckt Node* for easy connection.
4. The signal and its power and ground are grouped together for the Controller/Memory block to make the manual connecting easy.
5. When the *Explicit IO Power and Ground Terminals* are utilized, all the powers and grounds of the Controller/Memory must be connected to do the non-ideal power bus simulation.

## SPICE-Based Controller or Memory Block

The controller and memory blocks can be of two types – with an IBIS model or with a SPICE subcircuit.

Though you can add multiple memory blocks, only one controller is allowed in the topology.

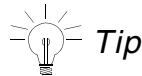
Also, you cannot have a mix of IBIS-based and SPICE-based memory blocks in a topology. Therefore, if you have added a SPICE-based memory block, you will be allowed to add more SPICE-based memory blocks only. The option for IBIS-based memory block will then be disabled in the *Add Block* panel.

## Topology Workbench User Guide

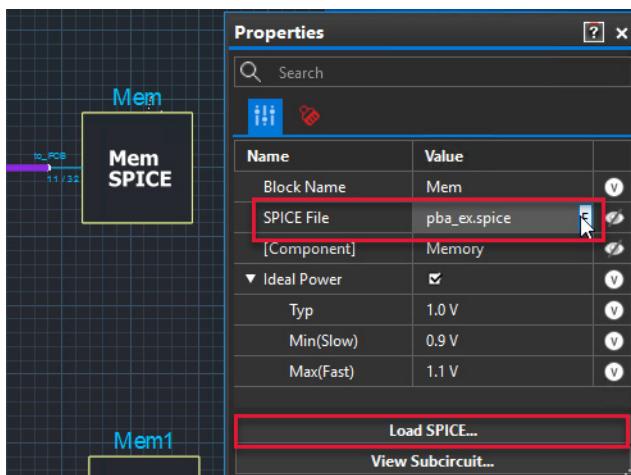
### Using Parallel Bus Analysis Workflow

In the *Component Properties* tab of the [Edit Properties Panel](#) for a Controller or Memory SPICE block, you can:

1. Select or deselect the *Ideal Power* check box. If the ideal power is required, specify the *Typ*, *Min(Slow)*, and *Max(Fast)* values.
2. Click the *E* button in the cell adjacent to the *SPICE* field.



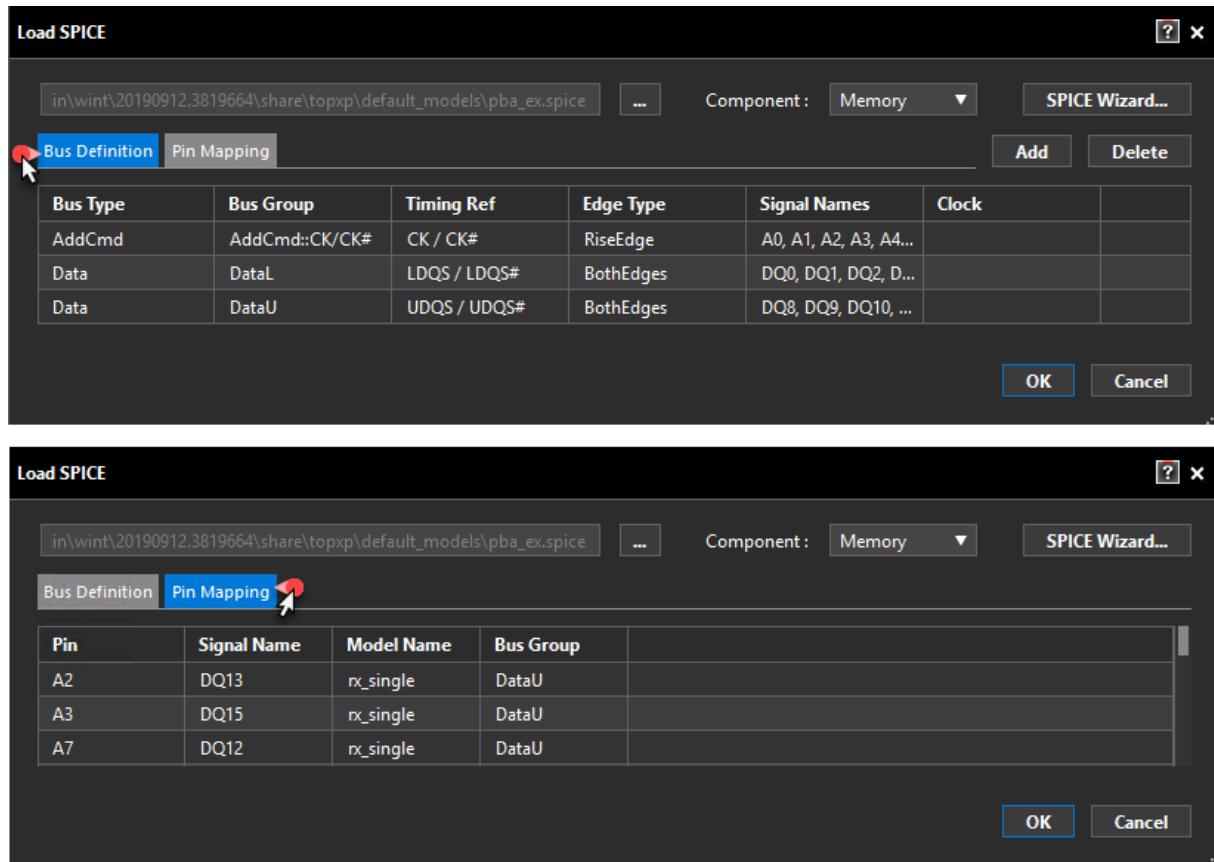
Alternatively, you can click the *Load SPICE* button in the *Edit Properties* panel.



## Topology Workbench User Guide

### Using Parallel Bus Analysis Workflow

The *Load SPICE* dialog box opens to let you specify the required SPICE model file that needs to be attached to the block and configure the corresponding bus definitions and pin mappings.



- Click the browse (...) button to select and assign a SPICE model file.

The tables on the *Bus Definition* and *Pin Mapping* tabs are populated with the data imported from the selected file.

- Select the *Component* to which the selected SPICE model file should be applied. The list box displays two options – *Controller* and *Memory*.
- Specify the following information in the *Bus Definition* tab: *Bus Type* (*AddCmd*, *Data*, or *Ctrl*), *Bus Group*, *Timing Ref*, *Edge Type* (*RiseEdge*, *FallEdge*, or *BothEdges*), and *Signal Names*.  
**Note:** Click the *Add* button if new rows need to be added to the bus definition table. To remove a row, select it and then click *Delete*.
- Review the information in the *Pin Mapping* tab. The table in this tab is populated *Bus Type* (*AddCmd*, *Data*, or *Ctrl*), *Bus Group*, *Timing Ref*, *Edge Type* (*RiseEdge*,

## Topology Workbench User Guide

### Using Parallel Bus Analysis Workflow

*FallEdge*, or *BothEdges*), and *Signal Names* (displays the *Signal* dialog box with check boxes for choice placed adjacent to the names of pins and signals).

7. Click *OK* to confirm loading of the SPICE model.

### Using SPICE Wizard for Component and Model Definitions

In the *Load SPICE* dialog box, if you click the *SPICE Wizard* button, the *SPICE Wizard* dialog box opens. This wizard has two tabs – *Component Definition* and *Model Definition*.

On the *Component Definition* tab of the *SPICE Wizard*, you can:

1. Update the *Pin* and *Diff Pin* definitions for the existing Controller and Memory components.
  - a. Edit the *Pin* information in the required cells of the table, such as *Pin* number and *Signal Name*.
  - b. Change the *Model Name* from the list displayed when a cell is clicked. The list contains the following options: ADDR, CLK, CTRL, DM, DQ, and DQS.
  - c. Edit the *Pin* and *Inverting Pin* in the *Diff Pin* table. Cells in both the columns display a list for choice when the cell is clicked.

The screenshot shows two tables within the SPICE Wizard interface. The top table is titled 'Pin' and lists pins 15 through 23 with their signal names (A7, A2, A6, A5, A1, A3, A4, A0) and model names (CLK, ADDR, ADDR, CLK, CTRL, DM, DQ, ADDR). The 'Model Name' column for pin 18 (A6) is currently set to 'ADDR' and has a dropdown arrow indicating it can be changed. The bottom table is titled 'Diff Pin' and lists pins 52, 77, and 104 with their corresponding inverting pins (51, 118, 15, 17, 18, 19, 20, 21, 22, 23, 51). The 'Inverting Pin' column for pin 52 has a dropdown menu open, showing options 118, 15, 17, 18, 19, 20, 21, 22, 23, and 51.

Pin		
Pin	Signal Name	Model Name
15	A7	CLK
17	A2	ADDR
18	A6	ADDR
19	A5	ADDR
20	A1	CLK
21	A3	CTRL
22	A4	DM
23	A0	DQ

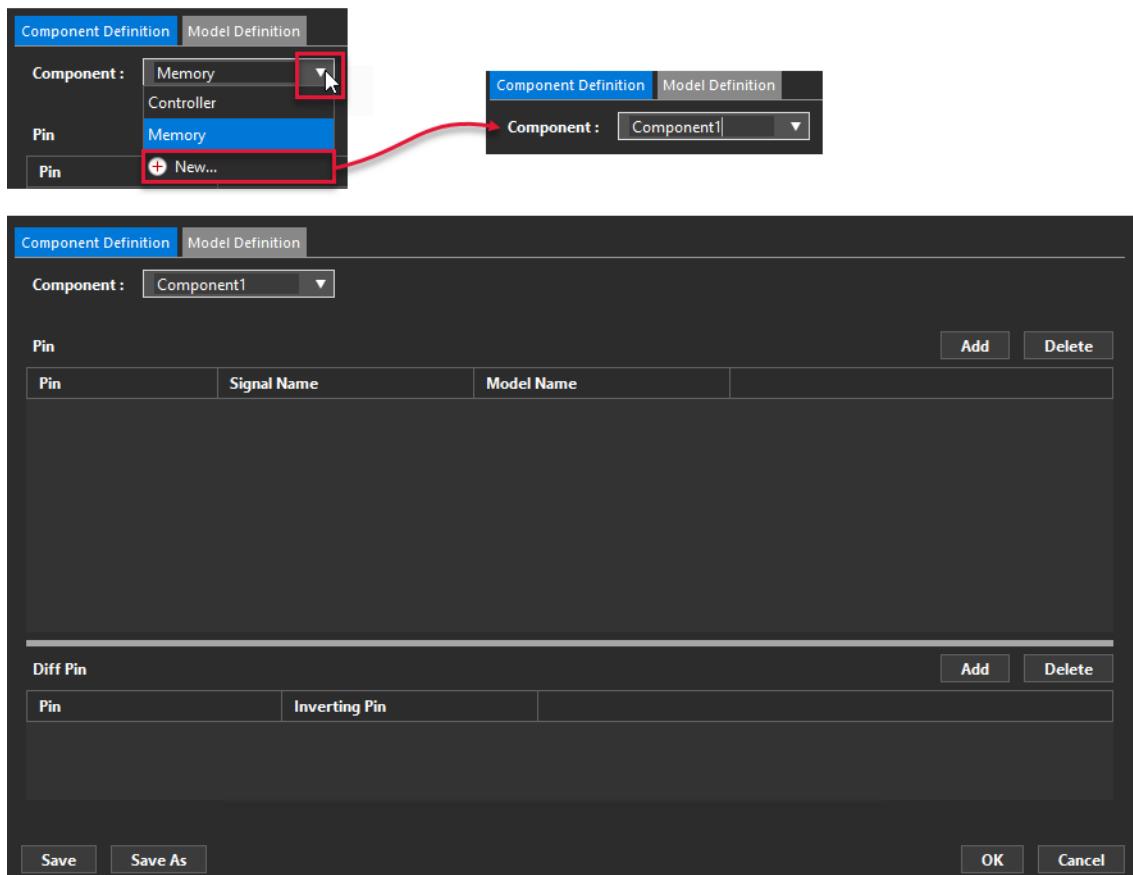
Diff Pin	
Pin	Inverting Pin
52	51
77	118
104	15
	17
	18
	19
	20
	21
	22
	23
	51

## Topology Workbench User Guide

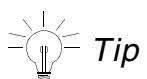
### Using Parallel Bus Analysis Workflow

#### 2. Add the *Pin* and *Diff Pin* definitions for a new *Component*.

- a. Click the *Component* list and select *New*.
- b. Specify a name for the new component.



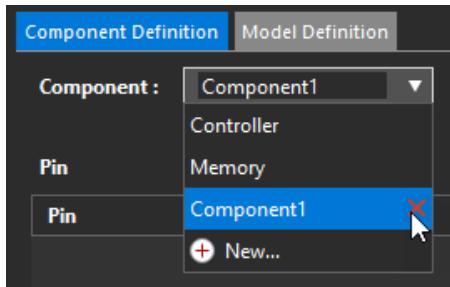
- c. Click the *Add* button to define the *Pin* and *Diff Pin* information in the respective sections.
- d. Click *Save*.



Click the *Save As* button if you want to save the SPICE definition with a different name.

#### 3. Delete the definition for a component.

- a. Click the *Component* list. Each item in the list has a cross adjacent to it to enable its deletion.
- b. Click the cross (X) corresponding to the component that needs to be deleted. All related *Pin* and *Diff Pin* information is also deleted.



On the *Model Definition* tab of the *SPICE Wizard*, you can:

1. Add a new SPICE Subcircuit model file.
  - a. Click *Add* in the *Spice Subcircuit* section of the dialog box. A new wizard opens.
  - b. Select the *Type* whether *Single-ended* (*OUTPUT* or *INPUT*) or *Diff* (*OUTPUT DIFF* or *INPUT DIFF*).
  - c. Click *Next*.
  - d. Click browse button adjacent to the *Circuit File* field and select the required file.
  - e. Select the Subcircuit from the list that is populated based on the selected SPICE Subcircuit file.
  - f. Click *Next*.
  - g. Select the *Type* for the listed *Cktnode*. By default, all are set to *Floating* type. The list displayed on clicking a cell include *Floating*, *Output*, *Stimulus*, *Power*, *Ground*, and *Short to Power*.
  - h. Click *Finish*.
2. Update *Pin Mapping* of an existing SPICE Subcircuit model file.
  - a. Click the required cell in the *Pin Mapping* column and click *E* to edit. The Node Type table is displayed.
  - b. Click the required cell in the *Type* column.
  - c. Choose the value to which the *Node Type* should be changed.

- d. Click *Finish*.
3. Delete a SPICE Subcircuit model file.
  - a. Select the row of circuit file that needs to be removed.
  - b. Click *Delete* from the *Spice Subcircuit* section of the dialog box.
4. Add a new Model Selector.
  - a. Click *Add* in the *Model Selector* section of the dialog box. A new row is added to the table with a default model type *Name*.
  - b. Edit the *Name*.
  - c. Click the cell under the *Model* column in the row created for defining a new model. The *Model Selector* dialog box is displayed.
  - d. Select the check box adjacent to the *Circuit File* that contains the required SPICE model.
  - e. Click *OK* to close the *Model Selector* dialog box. The *Model Selector* section in the *SPICE Wizard* is updated.
  - f. Click *Save*.
5. Update an existing Model Selector.
  - a. Click to select the cell that needs to be updated in the *Model Selector* section. The *Model Selector* dialog box is displayed.
  - b. Select the check box adjacent to the *Circuit File* that contains the required SPICE model.
  - c. Click *OK* to close the *Model Selector* dialog box. The *Model Selector* section in the *SPICE Wizard* is updated.
6. Delete an existing Model Selector.
  - a. Select the row of model type that needs to be removed.
  - b. Click *Delete* from the *Model Selector* section of the dialog box.

## EBD Block

While using Topology Workbench, you can import the Electrical Board Description (EBD) models that are as per the IBIS specification. EBD models are imported directly into Topology Workbench and automatically expanded out to include interconnect and referenced

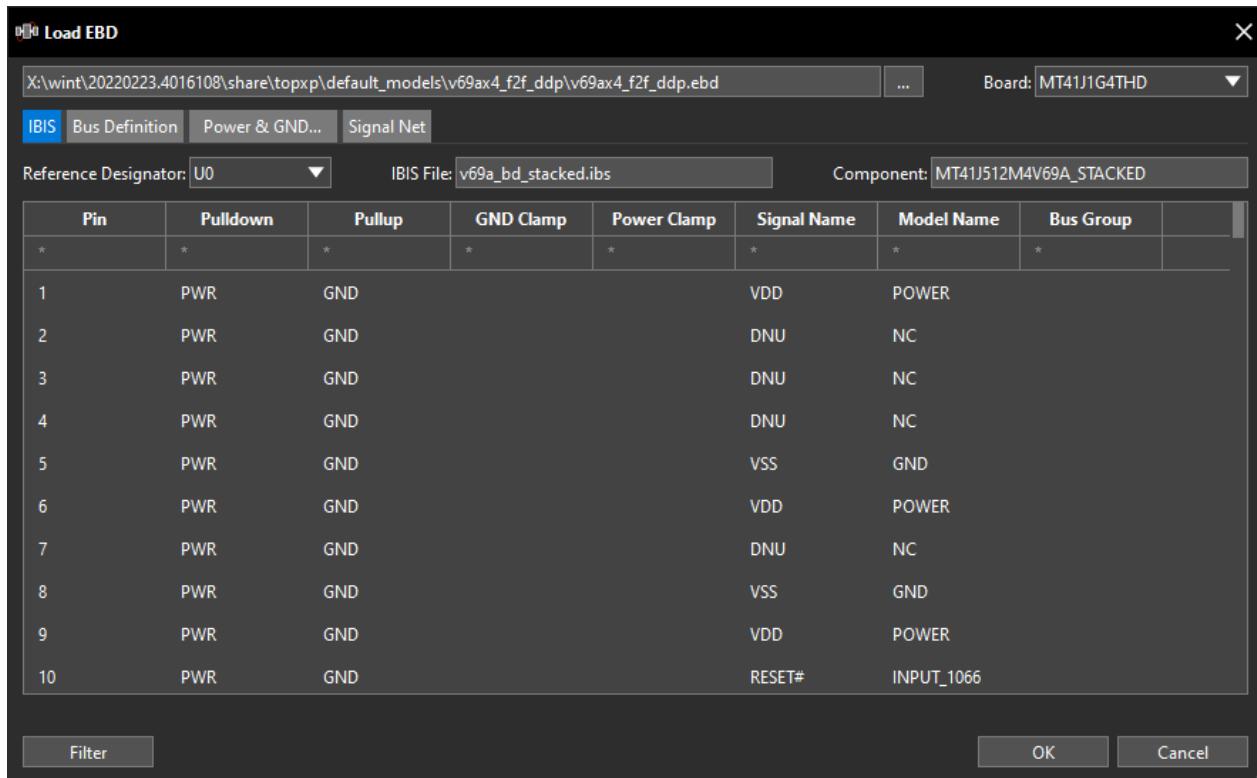
# Topology Workbench User Guide

## Using Parallel Bus Analysis Workflow

component blocks. EBD models are commonly used for modeling DIMMS. Use of different EBD models in the same PBA project is allowed.

**Note:** Topology Workbench does not support instantiating an EBD block along with a memory block.

When you associate an EBD model to an EBD block in Topology Workbench, the model information is displayed in the four tabs of the *Load EBD* dialog box, which can be accessed from the *Edit Properties* panel of the EBD block.



### ■ IBIS Tab

This tab lists all the Memory blocks and Terminators listed as Reference Designators. To view the Pin Mapping of a memory block or a terminator, from the Reference Designator drop-down list, select the refdes of the component.

A Terminator can have its own IBIS component; but all the Memory blocks must share the same component of the same IBIS file.

### ■ Bus Definition Tab

This tab lists the Bus groups defined for the Memory component. If required, use this tab to add and define new bus groups.

■ Power & GND Net Tab

The EBD model does not have the definitions for the Power and Ground nets. In order for the IBIS components to get the power supply from outside the EBD, each IBIS Power Pin must be linked to one EBD Power Pin that is connected to other blocks. The same is true for the IBIS Ground Pins.

Only the IBIS Power and Ground Pins that are associated with the defined Bus signals are listed in the Power & GND net tab.

■ Signal Net Tab

The IBIS Pins are for the defined Bus signals of the Memory blocks. If a signal is defined in the EBD file, its IBIS Pin and the EBD Pin will be listed together in the same row. All the EBD pins listed in the MCP are used for the connection to the other blocks.

When simulation is run for a topology that has an associated EBD model, the measurement is done at the DIE or package pin-level of the memory components. In the PBA workflow, measurements are also done at the input of the EBD model and the results are included in the report. This feature is useful for package models that use EBD format because the component pins then act as the EBD input and thus, necessitating measurement at such locations.

## Using EBD Models in Topology Workbench

To import an EBD models in Topology Workbench, you first add an instance of EBD block in the layout and then associate the EBD file with the EBD block.

Depending on the EBD model, new Memory blocks are automatically added to the topology.

## S Parameter Block

The S Parameter models describe the input-output relation between the ports (or terminals) in a block. Such models can be assigned to the *SnP* (S Parameter) blocks, which can be added to the topology from the *Add Block* panel.

For information about how to configure an S Parameter block, see [Assigning and Extracting S Parameter Files in Chapter 2, “Working with Topologies.”](#)

## Subcircuit Block

A *subckt* (subcircuit) block is a general purpose block that can contain an arbitrary SPICE subcircuit.

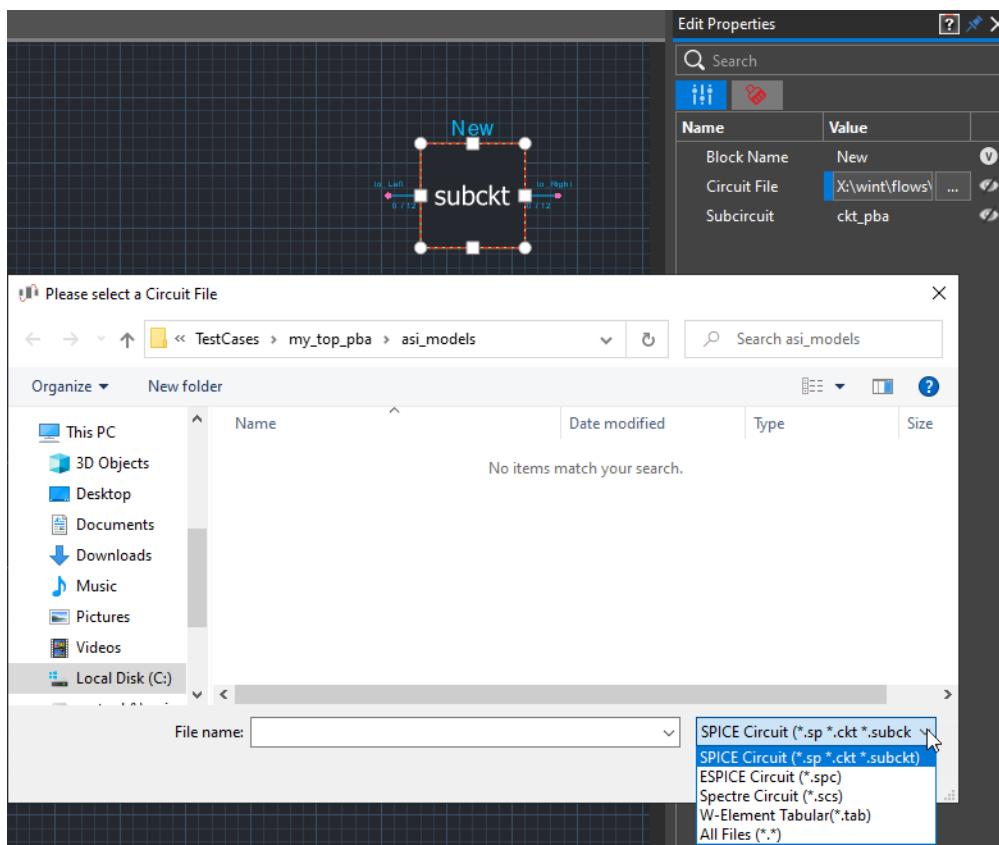
## Topology Workbench User Guide

### Using Parallel Bus Analysis Workflow

**Note:** You can set up the default pin locations for a SPICE subcircuit the same way as you can for an S Parameter block. For more information, see [Setting Up the Default Pin Location in Chapter 2, “Working with Topologies.”](#)

In the *Component Properties* tab of the *Edit Properties* panel for a subcircuit block, you can:

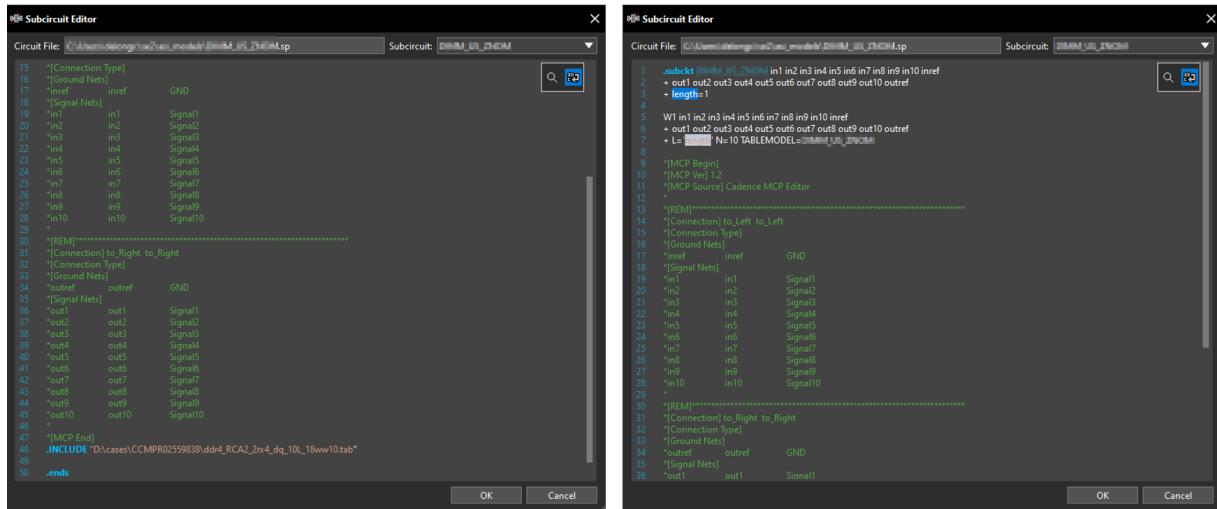
1. Assign a *Circuit File*. You can assign a circuit file of one of the following formats: *SPICE Circuit (\*.sp, \*.ckt, \*.subckt)*, *ESPICE (\*.esp)*, *Spectre Circuit (\*.scs)*, or *W-Element Tabular (\*.tab)*.
  - a. Click *E* that is displayed when the pointer is placed in the cell adjacent to *Circuit File*. Alternatively, click *Load Circuit File*.
  - b. Browse and select the required file from the displayed dialog box.
  - c. Select the *Subcircuit* from the list that is populated based on the specified circuit file.
  - d. Click *View Subcircuit* to open the *Subcircuit Editor*. You can edit the subcircuit definition in this editor and then click *OK* to save the changes.



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## Using Parallel Bus Analysis Workflow

**Note:** When you load a \*.tab file, a wrapper SPICE file is created automatically and the length parameter can be edited in the Subcircuit Editor.



If you assign a circuit file (\*.ckt) of Touchstone or a more-compact Cadence Broadband Network Parameter (BNP) format, you can use the subcircuit block to create a PCB block. In this scenario, you can:

1. Assign a *Circuit File* of \*.ckt format.
2. Select or deselect the check box to *Remove DC Blocking Components*.
3. Select or deselect the check box to *Enforce Passivity*. When selected, passivity checks are run for the input S-element and passivity enforcement process is performed if passivity violations exist.
4. Select or deselect the check box to enable or disable *Layout Extraction*. For details, see [Appendix D, “Using Extracted Interconnect Models from Layout.”](#)
5. Click the *View S Parameter* button to view the waveforms for the *Network Parameters* in the *SSIViewer [S Amplitude (dB)]* window.

## Layout Block

A *Layout* block can be used for extracting the SPICE database from the layout. You can load .brd, .mcm, and .sip files for layout block. For details, see [Appendix D, “Using Extracted Interconnect Models from Layout.”](#)

## VRM Block

Parallel Bus Analysis parameterizes the corner voltages of a Voltage Regulator Module (VRM) component including, Min, Typ, and Max VRM voltages, for fast, consistent simulation of the IBIS corner models.

In the *Component Properties* tab of the *Edit Properties* panel for a VRM block, you can:

1. Set the *Voltage Range* on the following parameters: *Typ*, *Min(Slow)*, and *Min(Fast)*.
2. Configure the associated *Power Net*.
  - a. Specify the *Net Name*.
  - b. Enter the (number) *# of Pins*.
  - c. Specify the *Pin Name* and *Pin Resistance*.
3. Configure the associated *Ground Net*.
  - a. Specify the *Net Name*.
  - b. Enter the (number) *# of Pins*.
  - c. Specify the *Pin Name* and *Pin Resistance*.

**Note:** In the extracted use models having VRM blocks, the connections of the VRM blocks are hidden by default. If you need to run non-ideal simulation for such use models, then before starting the simulation, right-click the canvas and click the *Display Unconnected Power Pin* option from the displayed shortcut menu.

## Trace Block

Using a Trace block in the topology lets you leverage the advantages of pre-layout transmission line modeling capability.

In the *Component Properties* tab of the *Edit Properties* panel for a Trace block, you can:

1. Select or deselect the *Include Power* check box. If the *Include Power* check box is selected, a VRM Block automatically gets attached to the Trace block in the layout. In addition, the *PDS Resistor* and *PDS Capacitor* properties related to the VRM block appear in the *Edit Properties* panel as a sub-property of *Include Power*.
2. Configure the VRM block. Double-click the VRM block in the layout and then review and update the corresponding properties.

3. Detach the VRM if it is not required. To do so, deselect the *Add VRM* check box in the *Edit Properties* panel for the Trace block.

**Note:** Deleting the VRM block directly from the canvas is not recommended.

4. Review the subcircuit. The *Subcircuit Editor* for a Trace opens in read-only mode.
5. Use the TLine Editor to make any required modifications. For information, see [Appendix C, “Modeling Pre-Layout Transmission Lines.”](#)

## Augmenting an IBIS File

Parallel Bus Analysis is compatible with the I/O Buffer Information Specification (IBIS), version 6.1, including BIRD95 (composite current) and BIRD98 (gate modulation effect) to allow non-ideal power and ground IO modeling. Interconnects, including boards, connectors, and cables can be modeled with frequency-domain S-Parameter data or SPICE-compatible subcircuits, and connected together with explicit power and ground connections to preserve the signal integrity (SI) behavior related to planes and power/ground pin performance. Transistor-level I/O models in HSPICE or Spectre format can also be included through the IBIS model interface. Connectivity between components is fast and robust with block-based connections.

To enable the automation provided by Parallel Bus Analysis, some augmentation of the standard IBIS files is required. Specifically, the definition of bus groups, timing reference signals, and setup/hold specifications are needed. This can all be done through the Topology Workbench window, and the comments are automatically embedded into the IBIS file itself.

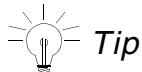
Some key IBIS file dependencies for Parallel Bus Analysis that must be present in the IBIS files for the Controller and Memory blocks include:

- The [Pin Mapping] section to indicate the power and ground buses to which a given driver, receiver, or terminator is connected. It accepts the following parameters: *pulldown\_ref*, *pullup\_ref*, *gnd\_clamp\_ref*, *power\_clamp\_ref*, and *ext\_ref*.

This section is required by Topology Workbench for simulations with non-ideal power, for example, to consider the SSN effects. The pin name to signal name mapping is crucial because it is used to connect the components together in Parallel Bus Analysis.

However, according the IBIS specification, the [PinMapping] section is optional, and may not exist in every IBIS file. If this section is not available in an IBIS file, Topology Workbench performs Parallel Bus Analysis assuming the ideal power conditions.

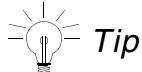
Therefore, it is strongly recommended that a valid pin-mapping specification be obtained from the device manufacturer and included in the IBIS file.



*Tip*

Use the [Pin Mapping](#) tab of the *Load IBIS* dialog box to edit the [Pin Mapping] section of the assigned IBIS file.

- Define signals as a bus and identify the timing reference signals for the bus for both Controller and Memory components. These definitions comprise a new IBIS file block with associated keywords. The bus definition classifies the buses into three categories—Clock, Address, or Data.



*Tip*

Though bus categorization information can be added to the IBIS file using a text editor like *IBIS Editor*, it is highly recommended that the [Bus Definition](#) tab of the *Load IBIS* dialog box is used to create the bus definitions.

For more information, refer to [Assigning and Editing IBIS Models](#).

## Simulating Circuits That Use S-Parameter Model

The PBA workflow in Topology Workbench adopts direct S-Parameter model simulation routines built in SPDSIM. You can use Broadband SPICE conversion when S-Parameter does not converge with all options.

The recommended flow is to use PowerSI or other S-Parameter generation tools to get a S-Parameter definition, examine the S-Parameter file, build a topology, enable S-Parameter options, and simulate. For information, see [Assigning and Extracting S Parameter Files](#) and Chapter 4, “[Running a Simulation and Analyzing the Results](#).”

When debugging a PBA topology that has S-Parameter models, try to shorten them first. It helps to isolate the issues and be sure that the problem is with the S-Parameter model. Then enforce passivity.

When a simulation involving S-Parameter has issues (for example, non-convergence), view and check the S-Parameter model for insertion loss, return loss, and xTalk. If the S-Parameter model shows problems, re-extract the model or try to change the routing.

In addition, when simulating parallel buses with extracted S-Parameters that include AC coupling capacitances, ensure that you select the *Remove DC Blocking Components* check box in the block’s *Edit Properties* panel. This setting can be controlled on a block-by-block basis.

Similarly, you might want to check the passivity of the input S-element and perform passivity enforcement process when passivity violations are found. To enable this behavior, select the *Enforce Passivity* check box. This setting can also be controlled on a block-by-block basis.

## Using DDR Measurement Reports

The PBA workflow supports extensive DDR data processing and specification compliance functionality. Standard measurements and specifications from JEDEC standards are included, with user-friendly data presentation and parsing, for unprecedented troubleshooting, all combined with the implicit accuracy that comes with unique simulation technology.

For details, see [Appendix H, “Reporting DDR Measurements.”](#)

## Building AMI Models for a Parallel Bus Topology

PBA workflow comes with a library of parameterized, configurable Algorithmic Modeling Interface (AMI) models for common equalization functionality, such as Feed Forward Equalization (FFE), Continuous Time Linear Equalization (CTLE), and Decision Feedback Equalization (DFE). These are used for what-if feasibility analysis, or if your Serializer/Deserializer (SerDes) supplier cannot provide you with an AMI model for the specific device used in your design.

**Note:** In the Topology Workbench – SystemSI workflows, a default control, `PostProcessDCOffset`, handles the single-ended signal measurement and coordinates with DFE. However, if the AMI model in a topology already has a DC-shift control, you need to either switch it off in the AMI model or disable the `PostProcessDCOffset` default control from the *Analysis Options* panel.

Assignment of AMI models to implement digital signal processing techniques for signal conditioning (for example, Equalization), and clock and data recovery helps to:

- Overcome high-frequency losses in the channel component of SerDes systems
- Improve signal integrity performance of the SerDes systems
- Govern the implementation according to the requirements described in the IBIS specification

**Note:** For more information on the IBIS AMI modeling standard, see the latest IBIS specification at <http://ibis.org/specs/>.

The AMI models can be configured using the options provided in the *AMI Builder* schema of the Workflow Panel. You can also cascade the AMI Models for flexible modeling and debugging.

In addition, new and unique AMI models can be created directly in Topology Workbench using the *AMI Builder* tab in the *Create New Topology* dialog box, which can be accessed from the *Topology – New* menu.

For detailed information, see [Using the AMI Builder](#)

To support AMI models for strobe and clock in the PBA workflow

## **Using Extracted Interconnect Models in Parallel Bus Analysis**

The Layout Association functionality in Topology Workbench provides direct integration with PowerSI and SPEEDEM Generator (SPDGEN), enabling automation in the extraction and model generation for blocks in Topology Workbench topologies that are based on physical layout.

For details, see [Appendix D, “Using Extracted Interconnect Models from Layout.”](#)

## **Using Pre-Layout Transmission Line Modeling Capability**

Topology Workbench includes the pre-layout transmission line (TLine) modeling capability.

For details, see [Appendix C, “Modeling Pre-Layout Transmission Lines.”](#)

## **Running Sweep Simulations**

The *Sweep Manager* allows multiple values to be set for key parameters in the topology. Sweeping then will automatically run multiple simulations, substituting in the relevant parameter values for each unique simulation run. Results can then be analyzed to understand the impact of the parameter values on overall performance.

For details, see [Appendix E, “Using the Sweep Manager.”](#)

## Setting Up Constraints for Parallel Bus Analysis

In PBA workflow, you can define constraints in a topology project as an Electrical Constraint Set (ECSet), which applies to each net, and then import them to Constraint Manager.

For details, see [Chapter 11, “Exporting Constraints from a Topology.”](#)

**Topology Workbench User Guide**  
Using Parallel Bus Analysis Workflow

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# Working with Compliance Kits

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Topology Workbench provides a set of standard built-in compliance kit templates for high-speed SerDes designs. Using these compliance kits, you can automate the compliance testing process and speed up the design process.

In addition, in the Serial Link Analysis (SLA) and Compliance Kits workflows, you have the option to create your own customized compliance kits to suit your design requirements.

### ***Related Topics***

- [Using the Standard Built-In Compliance Kits](#)
- [Creating Customized Compliance Kits](#)
- [Checking for OpenPOWER Compliance](#)

## Using the Standard Built-In Compliance Kits

The standard built-in compliance kits shipped with Topology Workbench automate the process of compliance checking, allowing you to select the compliance criteria of interest, and easily generate a compliance report. The compliance kits provide predefined templates that are ready-to-run as a starting point for compliance sign-off. IBIS-AMI models, when necessary, for transmitters and receivers are intended to represent *specifications-level* functionality, and are developed according to the characteristics defined in the associated specification.

The compliance kits provide typical interconnect topologies with example models in place. These interconnect models, or any other models, are example models to help you get started, and are not intended for detailed analysis, or represent any specific reference standard. You need to customize the topology as per your own application, and insert own interconnect models for detailed analysis.



**Caution**

***In no event can Cadence be held liable for any incidental, indirect, special or consequential damages, or any other damages whatsoever (including, without limitation, damages for loss of business profits, business interruption, loss of business information, or other pecuniary loss) arising out of the use, or inability to use the compliance kits, whether or not the possibility, or cause, of such damages was known to Cadence.***

### **Recommended Use Model**

Use the compliance kit templates to create your own custom templates, containing preferred interconnect (or other) models. These are a starting point for future compliance checking within a group or company for a given standard. The compliance kits can be used in the following ways:

- **Channel Compliance**

Replace the interconnect topology with one for your own application, and leave the spec-level Tx and Rx models in place. This enables the channel to be evaluated for compliance, in the context of spec-level transmitters and receivers.

- **SerDes Compliance**

Replace the interconnect topology with a reference or test channel of your choosing, and also replace one or more of the SerDes Tx or Rx models with a model for a component expected to be used in the design. This enables the SerDes of interest to be evaluated for compliance, in the context of a specific channel.

- **Interface Compliance**

In addition to replacing the interconnect topology with one for your own application, also substitute the Tx and Rx models with models for the specific components that will be used in the design. This enables you to evaluate the entire serial link interface in terms of the associated standard's compliance criteria.

### **Starting a Compliance Workflow**

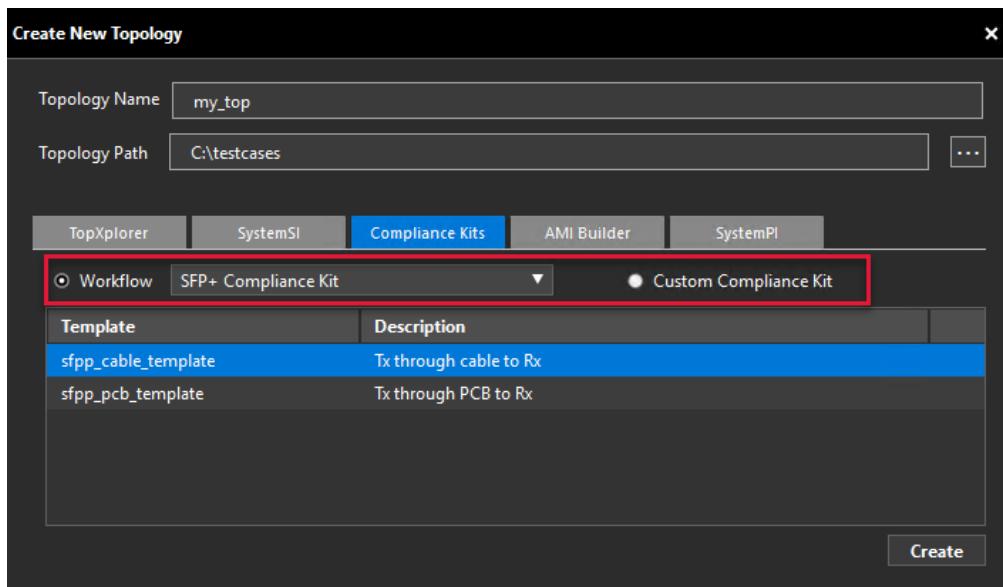
To use the standard built-in compliance kits supported in the SLA workflow, perform the following steps:

1. Start Topology Workbench.

## Topology Workbench User Guide

### Working with Compliance Kits

2. Click *New...* from the *Start Something Awesome* section on the Start Page tab. The *Create New Topology* dialog box is displayed.
3. Specify a *Topology Name* and *Topology Path*.
4. Click the *Compliance Kits* tab.



**Note:** In the *Compliance Kits* tab, you have an option choose to use a specific workflow and standard built-in compliance kit combination, or you can create a custom compliance kit. For more information about the latter, refer to [Creating Customized Compliance Kits](#).

5. Select the *Workflow* option.

**Note:** It is selected by default when the *Create New Topology* dialog box opens and then the *Compliance Kits* tab is accessed. In such cases, step 5 is not needed.

6. Select a compliance kit from the list box adjacent to the *Workflow* option. The table on the tab is refreshed to list all available default templates associated with the selected compliance kit. The following compliance kits are available:

- [SFP+ Compliance](#)
- [HDMI 1.x Compliance](#)
- [HDMI 2.0 Compliance](#)
- [PCIe 3 Compliance](#)
- [PCIe 4 Compliance](#)
- [PCIe 5 Compliance](#)

## Topology Workbench User Guide

### Working with Compliance Kits

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- [PCIe 6 Compliance](#)
- [10GBASE-KR Compliance](#)
- [MIPI M-PHY Compliance](#)
- [MIPI C-PHY Compliance](#)
- [100Base-T1 Compliance](#)
- [USB 3 - Gen 1 Compliance](#)
- [USB 3 - Gen 2 Compliance](#)
- [USB 4 - Gen 4 Compliance](#)
- [OpenPOWER Compliance](#)

7. Select the required template based on the description provided in the table.

8. Click *Create*.

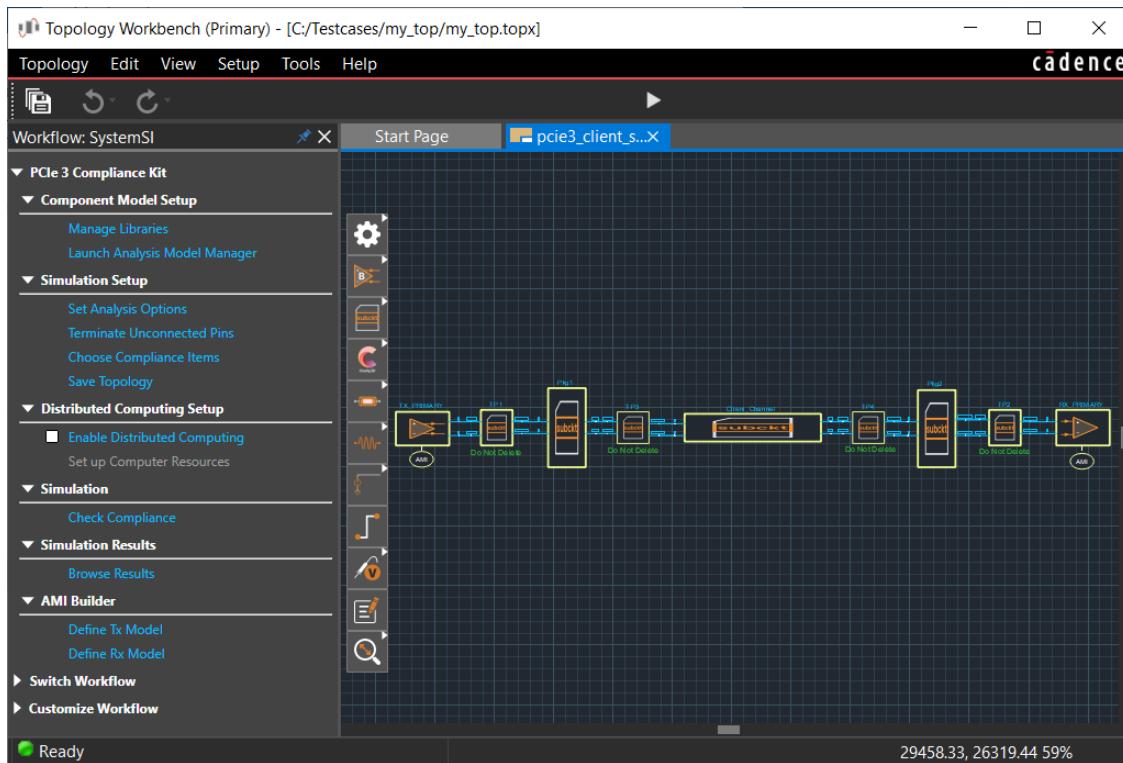
The Topology Workbench window is refreshed as following:

- A tab with the given *Topology Name* opens next to the [Start Page](#).
- The [Layout Canvas](#) is populated with the blocks as per the selected default template.
- The [Workflow Panel](#) opens with a list of tasks you can perform for the selected type of compliance check.

# **Topology Workbench User Guide**

## Working with Compliance Kits

- The Floating Toolbar opens with a list of various types of available blocks.



9. Associate appropriate models to the template blocks. Depending on the selected compliance kit, you might need to perform an extra step of setting AMI parameters.
  10. Setup and manage the component model libraries.

For information, see [Setting Up Component Model](#).

11. Click *Set Analysis Options* in the *Simulation Setup* schema to:

- ❑ Open the *Analysis Options* panel.
  - ❑ Set up the basic simulation settings such as signals to be simulated, simulator to be used, simulation configuration, and simulation name in the *Simulation Setup* and *Stimulus Definition and Model Selection* sections.

## Topology Workbench User Guide

### Working with Compliance Kits

12. Click *Choose Compliance Item* in the *Workflow* panel. A new tab with a list of compliance checks supported for the selected template are displayed.

**PCIe 3 Compliance Kit**

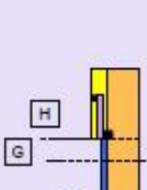
**Choose Compliance Items**

No.	Parameter	Values	<input type="checkbox"/>
<b>Channel Tolerancing Eye Mask Values (table 4-27 in PCI Express Base spec.)</b>			
1	Eye Height	25mV	<input type="checkbox"/>
2	Eye Width at Zero Crossing	0.3UI	<input type="checkbox"/>
3	Peak EH Offset from UI Center	T <sub>TX-DS-OFFSET</sub>	<input type="checkbox"/>
4	Range for DFE d1 Coefficient	V <sub>RX-DFE-COEFF</sub>	<input type="checkbox"/>
5	Eye Mask		<input type="checkbox"/>
<b>Differential Insertion Loss (figure 4-66 in PCI Express Base spec.)</b>			
6	Insertion Loss	SDD21	<input type="checkbox"/>
<b>Differential Return Loss (figure 4-56 in PCI Express Base spec.)</b>			
7	Tx Return Loss		<input type="checkbox"/>
8	Rx Return Loss		<input type="checkbox"/>
<b>Stressed/Swept Jitter Test (figure 4-74 in PCI Express Base spec.)</b>			
9	Stressed/Swept Jitter		<input type="checkbox"/>

**PCI SIG** **EXPRESS**

**Client Channel Configuration**

Seg	Description
A	MCH PKG
B	Break Out
C	MB Main 7"
D	MB post cap
F	Add in card main 3"
G	Add in card PKG Break out
H	Add in card PKG



The diagram illustrates the physical layout of the PCIe client channel. It shows a vertical stack of components labeled A through H. Segment A is the MCH PKG, B is the Break Out, C is the MB Main 7", D is the MB post cap, F is the Add in card main 3", G is the Add in card PKG Break out, and H is the Add in card PKG. Segments C, D, F, G, and H are shown as blue rectangular blocks, while A and B are shown as smaller blocks above them. A dashed line labeled 'G' indicates the location of the Add in card PKG Break out segment.

If you want to run all listed compliance checks, select the check box in the last column of the header row. Otherwise, select the individual check boxes in the last column to indicate the compliance checks that need to be performed.

**Note:** Click *Restore Defaults* to revert to the default selections.

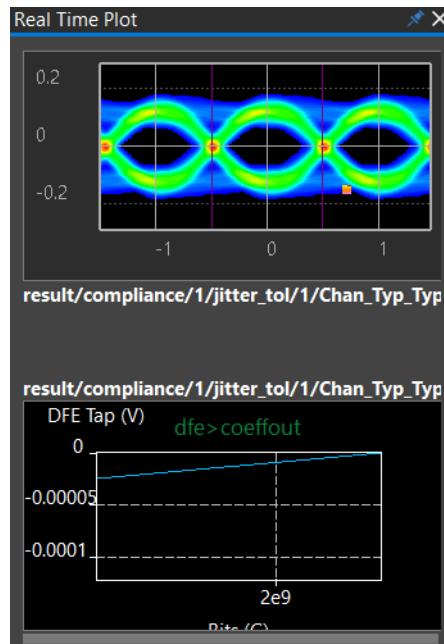
13. Click *Save Topology* in the *Workflow* panel.

Click *Check Compliance* from *Simulation* schema in the *Workflow* panel. This starts the simulation to perform the selected compliance checks. The progress is displayed in

## Topology Workbench User Guide

### Working with Compliance Kits

the status bar. The *Real Time Plot* panel also opens where you can monitor the changes in the waveforms.



# Topology Workbench User Guide

## Working with Compliance Kits

Once the simulation is complete, the simulation report is generated and displayed in the *Measurement Report* tab as shown below:

The screenshot shows the Cadence TopXp software interface for a PCIe 3 Client Channel Configuration. The top navigation bar includes 'Start Page', 'pcie3\_client...', 'Choose Complia...', 'Measurement..X', and a tab labeled 'compliance\_rep...' which is currently selected. The main content area features a title 'PCIe 3 Compliance Report' and a subtitle 'Generated by Topology Workbench, Cadence Design Systems Inc., Aug 24, 2023'. Below this is a detailed diagram of a PCIe channel structure with various segments labeled A through H. A legend identifies symbols for Via, Microstrip, and Stripline. The diagram is titled 'Client Channel Configuration' and includes a copyright notice for PCI-SIG. To the right of the diagram is the Cadence logo. The bottom section of the report contains a 'Useful Links' list with a single item: 'Cadence website: <http://www.cadence.com>'. There are also 'General Information' and 'Summary of Results' sections, both of which are currently empty.

### Useful Links

- Cadence website: <http://www.cadence.com>

### General Information

- Project File: my\_top.topx
- Circuit Simulator: SPDSIM

### Summary of Results

This report shows the results of the compliance testing using Cadence TopXp. The channel simulated passes the compliance requirements.

#### Channel Tolerancing Eye Mask Values (table 4-27 in PCI Express Base spec.)

Item	Value	Simulation Results	Pass/Fail
Eye Height (at BER=1e-12)	25 mV	111.000 mV	Pass
Eye Width at Zero Crossing (at BER=1e-12)	0.3 UI	0.410 UI	Pass
Peak EH Offset from UI Center (at BER=1e-12)	$\pm T_{RX-DS-OFFSET}$ UI	-0.031	Pass

#### Stressed/Swept Jitter Test (figure 4-74 in PCI Express Base spec.)

Item	Value	Simulation Results	Pass/Fail
Stressed/Swept Jitter		Jitter	Pass

#### Customized Contents

- Canvas Snapshot:

## Topology Workbench User Guide

### Working with Compliance Kits

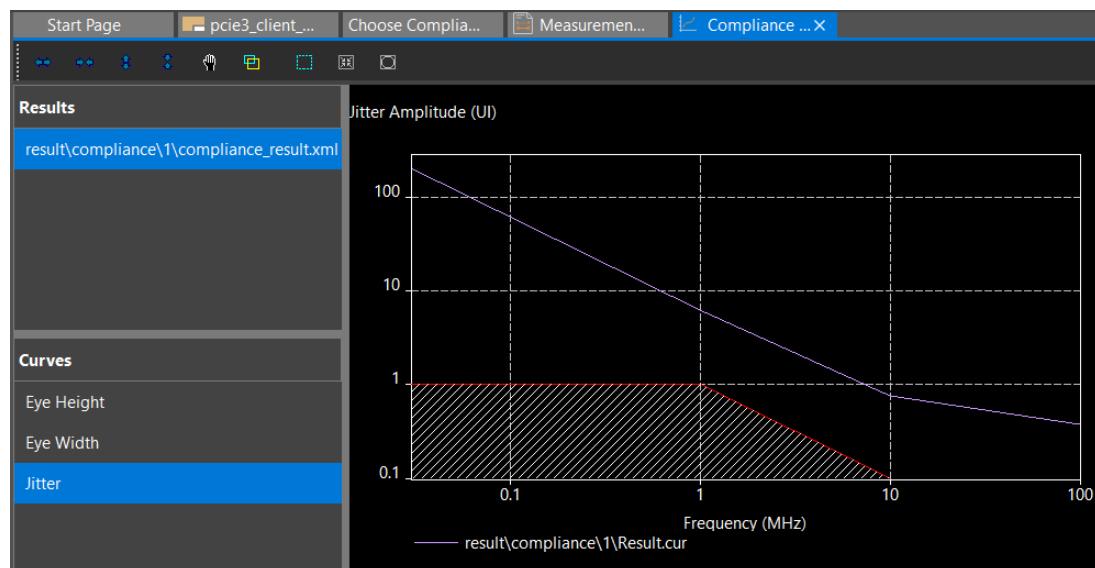
For each selected compliance check, the report shows *Pass* or *Fail* status in the *Pass/Fail* column as shown below:

Channel Tolerancing Eye Mask Values (table 4-27 in PCI Express Base spec.)			
Item	Value	Simulation Results	Pass/Fail
Eye Height (at BER=1e-12)	25 mV	<a href="#">111.000 mV</a>	Pass
Eye Width at Zero Crossing (at BER=1e-12)	0.3 UI	<a href="#">0.410 UI</a>	Pass
Peak EH Offset from UI Center (at BER=1e-12)	$\pm T_{RX-DS-OFFSET}$ UI	-0.031	Pass

Stressed/Swept Jitter Test (figure 4-74 in PCI Express Base spec.)			
Item	Value	Simulation Results	Pass/Fail
Stressed/Swept Jitter		<a href="#">Jitter</a>	Pass

The *Simulation Results* column displays the results that were arrived at as links. Clicking any of the linked result value opens the corresponding curve in the *Compliance Curves* tab as shown below:



To view a compliance curve, select the appropriate curve in the *Curves* pane of the *Compliance Curves* tab.

# Topology Workbench User Guide

## Working with Compliance Kits

### SFP+ Compliance

The SLA workflow provides SFP+ compliance checks for printed circuit boards. Following figures illustrate the various SFP+ compliance checks that are available for choice:

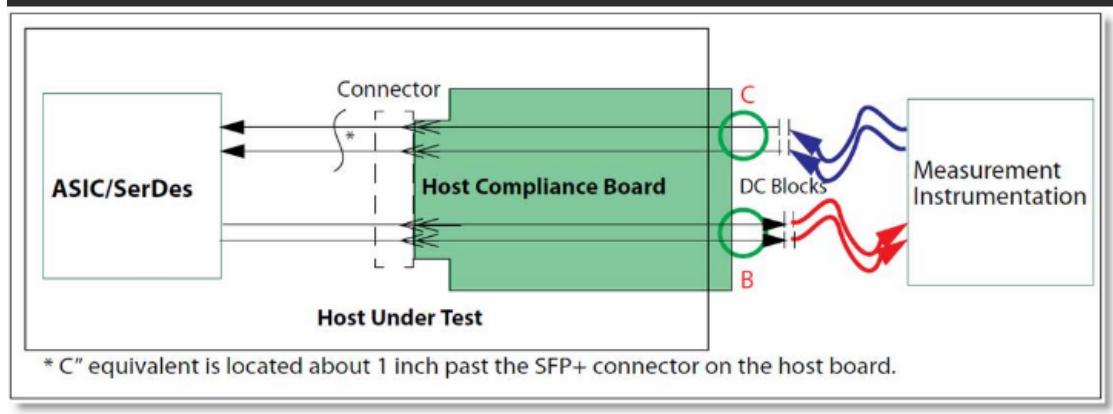
SFP+ Compliance Kit			
Choose Compliance Items			
No.	Parameter	Values	<input type="checkbox"/>
Host Transmitter Output Specification at B (table 11 in SFP+ spec.)			
1	Termination Mismatch at 1MHz	$\Delta Z_M$	<input type="checkbox"/>
2	Differential Output S-parameter	SDD22	<input checked="" type="checkbox"/>
3	Common Mode Output S-parameter	SCC22	<input type="checkbox"/>
Host Transmitter Output Jitter and Eye Mask Specification at B (table 12 in SFP+ spec.)			
4	Signal Rise/Fall Time (20% to 80%)	Tr, Tf	<input type="checkbox"/>
5	Total Jitter	TJ	<input type="checkbox"/>
6	Data Dependent Jitter	DDJ	<input type="checkbox"/>
7	Data Dependent Pulse Width Shrinkage	DDPWS	<input type="checkbox"/>
8	Uncorrelated Jitter	UJ	<input type="checkbox"/>
9	Transmitter Qsq	Qsq	<input type="checkbox"/>
10	Eye Mask		<input type="checkbox"/>
Host Receiver Input Specification at C (table 13 in SFP+ spec.)			
11	Differential Input S-parameter	SDD11	<input checked="" type="checkbox"/>
12	Reflected Differential to Common Mode Conversion	SCD11	<input checked="" type="checkbox"/>

# Topology Workbench User Guide

## Working with Compliance Kits

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SFI Channel Transfer Recommendation (table 25 in SFP+ spec.)			
13	Channel Transfer from chip pad to point B or C	SDD21	<input type="checkbox"/>
Additional SFI Channel Recommendations			
14	SFI Channel Return Loss	SDD11, SDD22	<input type="checkbox"/>
15	SFI Channel Ripple	Ripple	<input type="checkbox"/>
SFP+ Host Output Specification at B for Cu (table 33 in SFP+ spec.)			
16	Voltage Modulation Amplitude(p-p)	VMA	<input type="checkbox"/>
17	Transmitter Qsq	Qsq	<input type="checkbox"/>
18	Host Output TWDPC	PRBS9 Pattern: <input type="text" value="...mplate\prbs9_950.txt"/> <input type="button" value="..."/> Feedforward Equalizer Taps (EqNf): <input type="text" value="14"/> <input checked="" type="checkbox"/> Feedback Equalizer Taps (EqNb): <input type="text" value="5"/>	<input checked="" type="checkbox"/>



In the SFP+ cable template, all blocks, except the AMI blocks, are fixed blocks. Removing any of the fixed block causes the automated compliance tests to fail.

If the *Waveform Distortion Penalty (dWDPc or TWDPc)* check is selected, the *PRBS9 Pattern* file, *Feedforward Equalizer Taps (EqNf)*, and *Feedback Equalizer Taps (EqNb)* need to be specified as shown below:

18	Host Output TWDPc	PRBS9 Pattern: <input type="text" value="...mplate\prbs9_950.txt"/> <input type="button" value="..."/> Feedforward Equalizer Taps (EqNf): <input type="text" value="14"/> <input checked="" type="checkbox"/> Feedback Equalizer Taps (EqNb): <input type="text" value="5"/>	<input checked="" type="checkbox"/>
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**Note:** You can choose to retain the default values that are already displayed.

## Topology Workbench User Guide

### Working with Compliance Kits

Similarly, in the SFP+ compliance template for printed circuit boards, all blocks, except Connector and AMI blocks, are fixed blocks.

### HDMI 1.x Compliance

Topology Workbench provides compliance kit for verifying channel performance against High Definition Multimedia Interface (HDMI) specifications.

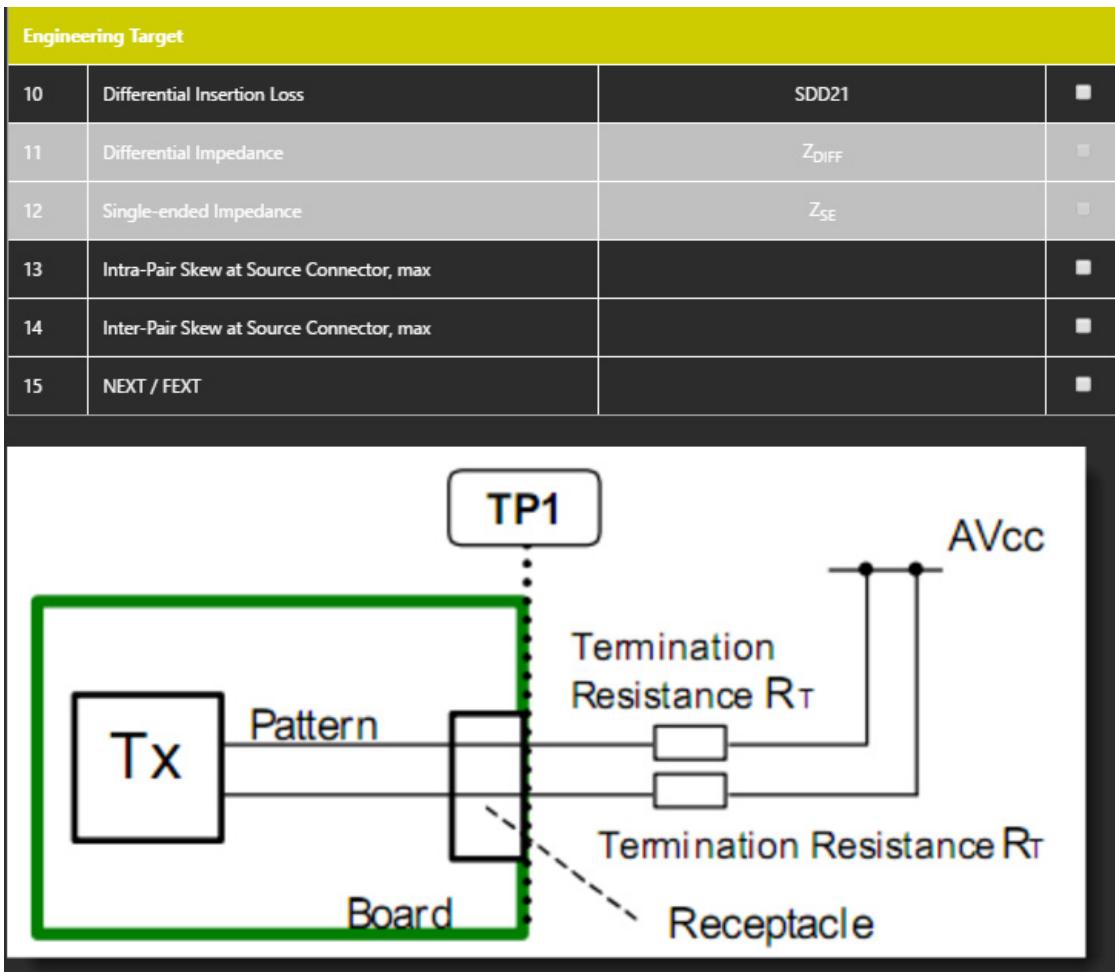
In the HDMI template, all blocks, except the Board block, are fixed blocks. If any of the fixed blocks are deleted or renamed, the compliance tests listed in the figure below might fail.

HDMI 1.x Compliance Kit			
Choose Compliance Items			
No.	Parameter	Values	<input type="checkbox"/>
Source DC characteristics at TP1			
1	Single-ended output swing voltage	$V_{swing}$	<input type="checkbox"/>
2	Single-ended high level output voltage	$V_H$	<input type="checkbox"/>
3	Single-ended low level output voltage	$V_L$	<input type="checkbox"/>
Source AC characteristics at TP1			
4	Rise time / fall time (20%-80%)		<input type="checkbox"/>
5	Intra-Pair Skew at Source Connector, max		<input type="checkbox"/>
6	Inter-Pair Skew at Source Connector, max		<input type="checkbox"/>
7	Clock duty cycle, min / average / max		<input type="checkbox"/>
8	TMDS Differential Clock Jitter, max		<input type="checkbox"/>
9	Eye Mask		<input type="checkbox"/>

## Topology Workbench User Guide

### Working with Compliance Kits

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### HDMI 2.0 Compliance

HDMI 2.0 compliance kit follows the requirements and guidelines listed in HDMI version 2.0. Using this compliance kit, you can use your own Rx AMI models, and run compliance tests with the channels as required by the HDMI2 standard, or you can use custom models for channels, packages, board, and receptacle models and verify if they pass the required compliance tests with HDMI2compliant AMI models.

For HDMI 2.0, Topology Workbench supports five templates. Of these, three templates are for test point 2 with equalizer, covering the three ranges for the different eye mask requirements for different ranges of data rates. For HDMI2.0, data rates range from 3.4 Gbps to 6 Gbps.

- Hdm2\_template\_TP1

## Topology Workbench User Guide

### Working with Compliance Kits

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Template for test point 1 (TP1)

- Hdmi2\_template\_TP2

Template for test point 2 (TP2)

- Hdmi2\_template\_TP2 eq3.4g\_to\_3.712g

Template for TP2 for data rate ranges from 3.4Gbps to 3.712 Gbps and eye mask with H = 0.6UI and V = 335mV

- Hdmi2\_template\_TP2 eq3.712g\_to\_5.94g

Template for TP2 when data rate ranges from 3.712 Gbps to 5.94 Gbps and eye mask with H = 0.5258 UI and V = 251mV

- Hdmi2\_template\_TP2 eq5.94g\_to\_6g

Template for TP2 when data rate ranges from 5.94 Gbs to 6 Gbs, and eye mask with H = 0.4 UI and V = 150mV

Following table lists the functions defining horizontal and vertical dimensions for the eye diagram at TP2\_EQ.

TMDS Bit Rate (Gbps)	H( $T_{bit}$ )	V(mV)
$3.4 < R_{bit} \leq 3.712$	0.6	335
$3.712 < R_{bit} \leq 5.94$	$-0.0332 R_{bit}^2 + 0.2312 R_{bit} + 0.1998$	$-19.66 R_{bit}^2 + 106.74 R_{bit} + 209.58$
$5.94 < R_{bit} \leq 6.0$	0.4	150

# Topology Workbench User Guide

## Working with Compliance Kits

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### HDMI 2.0 Compliance Kit

#### Choose Compliance Items

No.	Parameter	Values	<input type="checkbox"/>
<b>Source DC characteristics at TP1</b>			
1	Single-ended output swing voltage	$V_{swing}$	<input type="checkbox"/>
2	Single-ended high level output voltage	$V_H$	<input type="checkbox"/>
3	Single-ended low level output voltage	$V_L$	<input type="checkbox"/>
<b>Source AC characteristics at TP1</b>			
4	Rise time / fall time (20%-80%)		<input type="checkbox"/>
5	Intra-Pair Skew at Source Connector, max		<input type="checkbox"/>
6	Inter-Pair Skew at Source Connector, max		<input type="checkbox"/>
7	Clock duty cycle, min / average / max		<input type="checkbox"/>
8	TMDS Differential Clock Jitter, max		<input type="checkbox"/>
9	Eye Mask		<input type="checkbox"/>
<b>Engineering Target</b>			
10	Differential Insertion Loss	SDD21	<input type="checkbox"/>
11	Differential Impedance	$Z_{DIFF}$	<input type="checkbox"/>
12	Single-ended Impedance	$Z_{SE}$	<input type="checkbox"/>
13	Intra-Pair Skew at Source Connector, max		<input type="checkbox"/>
14	Inter-Pair Skew at Source Connector, max		<input type="checkbox"/>
15	NEXT / FEXT		<input type="checkbox"/>
16	Maximum Differential Voltage	$V_{high}$	<input type="checkbox"/>
17	Minimum Differential Voltage	$V_{low}$	<input type="checkbox"/>
<b>Sink Impedance characteristics at TP1</b>			
18	TDR Rise Time At TP1 (10% - 90%)		<input type="checkbox"/>

# Topology Workbench User Guide

## Working with Compliance Kits

### PCIe 3 Compliance

The PCIe 3 compliance kit follows the PCI Express Gen 3 standard, including IBIS-AMI models with back-channel support.

PCIe 3 Compliance Kit			
Choose Compliance Items			
No.	Parameter	Values	<input type="checkbox"/>
Channel Tolerancing Eye Mask Values (table 4-27 in PCI Express Base spec.)			
1	Eye Height	25mV	<input type="checkbox"/>
2	Eye Width at Zero Crossing	0.3UI	<input type="checkbox"/>
3	Peak EH Offset from UI Center	$T_{RX-DS-OFFSET}$	<input type="checkbox"/>
4	Range for DFE d1 Coefficient	$V_{RX-DFE-COEFF}$	<input type="checkbox"/>
5	Eye Mask		<input type="checkbox"/>
Differential Insertion Loss (figure 4-66 in PCI Express Base spec.)			
6	Insertion Loss	SDD21	<input type="checkbox"/>
Differential Return Loss (figure 4-56 in PCI Express Base spec.)			
7	Tx Return Loss		<input type="checkbox"/>
8	Rx Return Loss		<input type="checkbox"/>
Stressed/Swept Jitter Test (figure 4-74 in PCI Express Base spec.)			
9	Stressed/Swept Jitter		<input type="checkbox"/>

### Jitter Tolerance

Most of the compliance kits included with the SLA workflow have Jitter Tolerance included as one of the compliance checks. To run the Jitter Tolerance analysis in the *PCIe 3* workspace, select the *Stressed/Swept Jitter* compliance check. When this check selected, the compliance report includes the jitter tolerance results.

**Note:** A PCIe 3-specific jitter mask is shipped with Topology Workbench. For PCIe 3 compliance kit, load the *Pcie3\_jtolmask.txt* mask file, before running the compliance

## Topology Workbench User Guide

### Working with Compliance Kits

checks. This file is available at the following location:

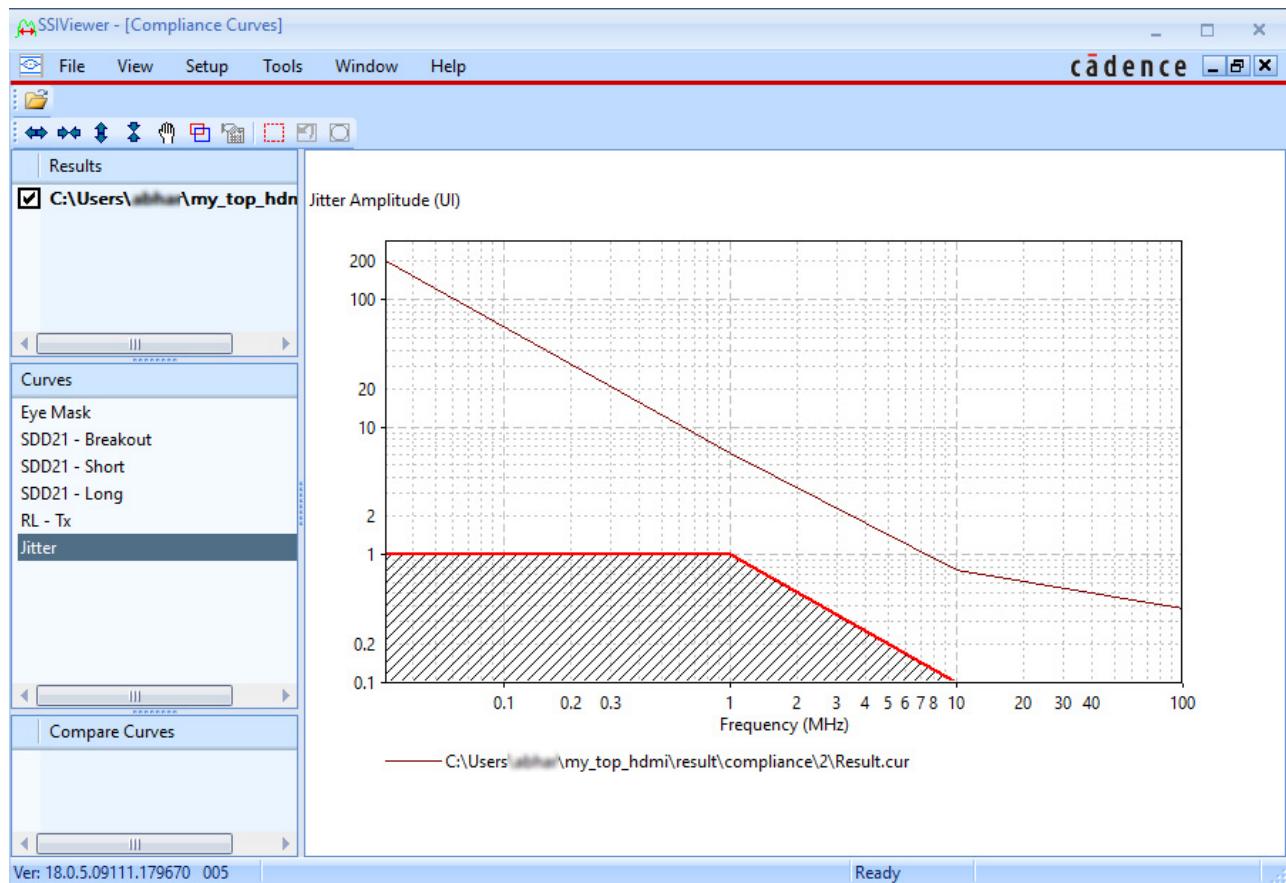
<INSTALL\_DIR>\share\topxp\ComplianceKits\jitter\_tol\mask

The generated PCIe3 compliance report includes the jitter tolerance results.

#### Stressed/Swept Jitter Test (figure 4-74 in PCI Express Base spec.)

Item	Value	Simulation Results	Pass/Fail
Stressed/Swept Jitter		Jitter	Pass

Select the *Jitter* link in the compliance report to view the jitter tolerance simulation plot as shown below.



# Topology Workbench User Guide

## Working with Compliance Kits

### PCIe 4 Compliance

You can run a PCIe4 compliance check based on the latest version of the PCIe4 specification available. The PCIe4 compliance kit consists of two different configurations for compliance tests, one is for a through channel and the other for xTalk channels.

PCIe 4 Compliance Kit			
Choose Compliance Items			
No.	Parameter	Values	<input type="checkbox"/>
Channel Tolerancing Eye Mask Values (table 9-13 in PCI Express Base spec.)			
1	Eye Height	15mV	<input type="checkbox"/>
2	Eye Width at Zero Crossing	0.3UI	<input type="checkbox"/>
3	Peak EH Offset from UI Center	$T_{RX-DS-OFFSET}$	<input type="checkbox"/>
4	Range for DFE d1 Coefficient	$V_{RX-DFE-D1-COEFF}$	<input type="checkbox"/>
5	Range for DFE d2 Coefficient	$V_{RX-DFE-D2-COEFF}$	<input type="checkbox"/>
6	Eye Mask		<input type="checkbox"/>
Differential Insertion Loss (figure 9-22 in PCI Express Base spec.)			
7	Insertion Loss	SDD21	<input type="checkbox"/>
Differential Return Loss (figure 9-19 in PCI Express Base spec.)			
8	Tx Return Loss		<input type="checkbox"/>
9	Rx Return Loss		<input type="checkbox"/>
Stressed/Swept Jitter Test (figure 9-31 in PCI Express Base spec.)			
10	Stressed/Swept Jitter		<input type="checkbox"/>

## Topology Workbench User Guide

### Working with Compliance Kits

#### PCIe 5 Compliance

You can run a PCIe5 compliance check based on the latest version of the PCIe5 specification available. The PCIe5 compliance kit consists of two different configurations for compliance tests, one is for a through channel and the other for xTalk channels.

### PCIe 5 Compliance Kit

#### Choose Compliance Items

No.	Parameter	Values	
Channel Tolerancing Eye Mask Values (table 8-14 in PCI Express Base spec.)			
1	Eye Height	15mV	<input type="checkbox"/>
2	Eye Width at Zero Crossing	0.3UI	<input type="checkbox"/>
3	Peak EH Offset from UI Center	$T_{RX-DS-OFFSET}$	<input type="checkbox"/>
4	Eye Mask		<input type="checkbox"/>
5	Lane-to-Lane Skew	5ns	<input type="checkbox"/>
6	Skew between P and N Side of Thru Diff Pair	10 ps	<input type="checkbox"/>
Differential Insertion Loss			
7	Insertion Loss	Mask File: <input type="text" value="...ks\pcie5_il.maskfile"/> <input type="button" value="Edit..."/>	<input type="checkbox"/>
Differential Return Loss (figure 8-20 in PCI Express Base spec.)			
8	Tx Return Loss		<input type="checkbox"/>
9	Rx Return Loss		<input type="checkbox"/>
Stressed/Swept Jitter Test			
10	Stressed/Swept Jitter		<input type="checkbox"/>

#### PCIe 6 Compliance

To support first mainstream usage of PAM4 signaling, you can select and simulate PCI Express Gen 6 Compliance Kit items. Based on the latest version of the PCIe6 specification available, the following compliance checks can be performed in Topology Workbench:

- Channel Tolerancing Eye Mask Values for Eye Height, Eye Width at Zero Crossing, Lane-to-Lane Skew, and Skew between P and N Side of Thru Diff Pair.

## Topology Workbench User Guide

### Working with Compliance Kits

- Differential Insertion Loss
- Differential Return Loss of Tx and Rx
- Stress/Swept Jitter Test

## PCIe 6 Compliance Kit

**Choose Compliance Items**

No.	Parameter	Values	<input type="checkbox"/>
<b>Channel Tolerancing Eye Mask Values (table 8-15 in PCI Express Base spec.)</b>			
1	Eye Height	6mV	<input type="checkbox"/>
2	Eye Width at Zero Crossing	0.1UI	<input type="checkbox"/>
3	Lane-to-Lane Skew	5ns	<input type="checkbox"/>
4	Skew between P and N Side of Thru Diff Pair	10 ps	<input type="checkbox"/>
<b>Differential Insertion Loss</b>			
5	Insertion Loss	Mask File: <input type="text" value="...ks\pcie6_il.maskfile"/> <input type="button" value="Edit..."/>	<input type="checkbox"/>
<b>Differential Return Loss (figure 8-24 in PCI Express Base spec.)</b>			
6	Tx Return Loss		<input type="checkbox"/>
7	Rx Return Loss		<input type="checkbox"/>
<b>Stressed/Swept Jitter Test</b>			
8	Stressed/Swept Jitter		<input type="checkbox"/>

The PCIe6 compliance kit templates consist of two different configurations for compliance tests, one is for a through channel and the other for xTalk channels.

# Topology Workbench User Guide

## Working with Compliance Kits

### 10GBASE-KR Compliance

The 10GBASE-KR compliance kits follow the specifications for interconnect characteristics and interference tolerance.

### 10GBASE-KR Compliance Kit

**Choose Compliance Items**

No.	Parameter	Values	<input type="checkbox"/>
Interference Tolerance (Annex 69A of the 10GBASE-KR spec.)			
1	Interference Tolerance		<input type="checkbox"/>
Interconnect Characteristics (Annex 69B of the 10GBASE-KR spec.)			
2	Skew between P and N Side of Thru Diff Pair		<input type="checkbox"/>
3	Insertion Loss		<input type="checkbox"/>
4	Fitted Attenuation		<input type="checkbox"/>
5	Insertion Loss Deviation		<input type="checkbox"/>
6	Tx Return Loss at TP1_RL		<input type="checkbox"/>
7	Rx Return Loss at TP4_RL		<input type="checkbox"/>
Channel Characteristics (Annex 93A of IEEE Std 802.3bj)			
8	Channel Operating Margin	3dB	<input type="checkbox"/>
9	Ratio of Insertion Loss to Crosstalk between TP1 and TP4		<input type="checkbox"/>

Transmitter → TP1 → Mated connector → TP4 → Receiver (including AC-coupling)

Backplane channel

NOTE—*<p>* and *<n>* represent the positive and negative traces of the differential pair

### ***Jitter Tolerance***

To run the Jitter Tolerance analysis for 10GBASE-KR compliance, select *Interference Tolerance* compliance check. With this check selected, the compliance report includes the jitter tolerance results and a link, *Jitter\_Tolerance*, that displays the compliance curve when it is clicked.

### ***Channel Characteristics***

To perform COM analysis for S-Parameter according to Annex 93A of IEEE standard 802.3bj, select the *Channel Operating Margin* option.

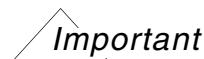
# Topology Workbench User Guide

## Working with Compliance Kits

### MIPI M-PHY Compliance

The MIPI standard is targeted for short range (less than one meter) mobile applications that require low pin count and low power consumption. Topology Workbench MIPI M-PHY Compliance kit supports high speed MIPI serial links.

MIPI M-PHY Compliance Kit			
Choose Compliance Items			
No.	Parameter	Values	<input type="checkbox"/>
TX Eye Mask Values (Table 16 in M_Phy spec version 3.0)			
1	Eye Height	80mV	<input type="checkbox"/>
2	Eye Width at Zero Crossing	0.55UI	<input type="checkbox"/>
3	Eye Mask		<input type="checkbox"/>
Channel Tolerancing Eye Mask Values(Table 21 in M_Phy spec version 3.0)			
4	Eye Height	80mV	<input type="checkbox"/>
5	Eye Width at Zero Crossing	0.48UI	<input type="checkbox"/>
6	Eye Mask		<input type="checkbox"/>
Differential Insertion Loss			
7	Insertion Loss	SDD21	<input type="checkbox"/>
Differential Return Loss(Figure 31 and 43 in M_Phy spec version 3.0)			
8	Tx Return Loss		<input type="checkbox"/>
9	Rx Return Loss		<input type="checkbox"/>
Stressed/Swept Jitter Test(Figure 44 in M_Phy spec version 3.0)			
10	Stressed/Swept Jitter		<input type="checkbox"/>



Four templates are available for this compliance check. These templates contain two fixed blocks that you cannot delete. The two blocks are needed for compliance check.

### Jitter Tolerance

To run the Jitter Tolerance analysis for *MIPI M-PHY Compliance*, select *Stressed/Swept Jitter* compliance check. With this check selected, the compliance report includes the jitter tolerance results.

## Topology Workbench User Guide

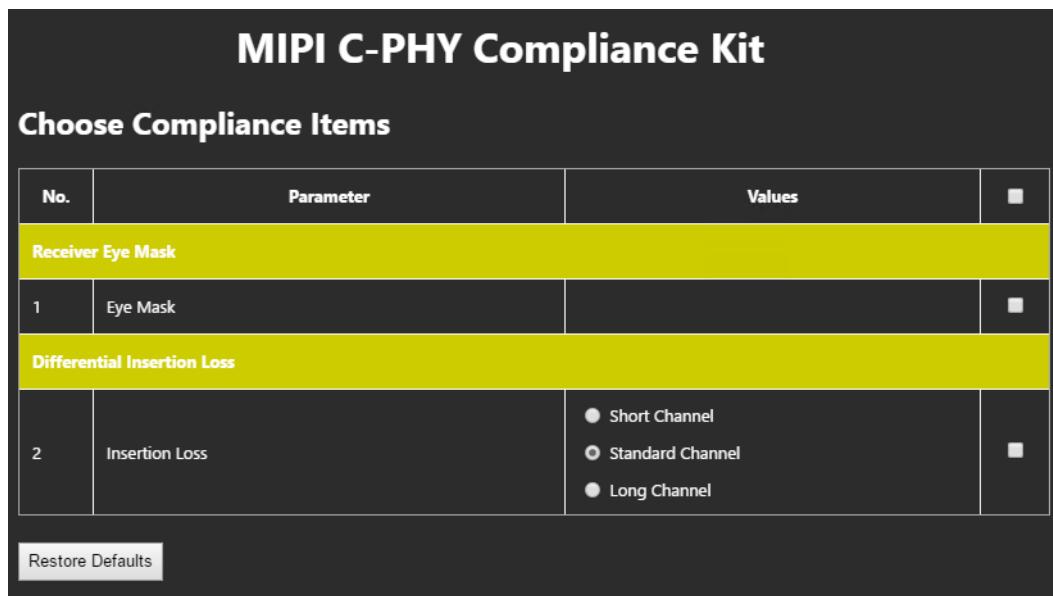
### Working with Compliance Kits

#### MIPI C-PHY Compliance

Topology Workbench lets you simulate High-Speed MIPI C-Phy topologies especially suited for mobile applications. Such topologies use three wire groups for higher throughput in a rate limited channel application. The three wires (A, B, C) comprise a lane. High speed signaling is differential for terminated data signals. At higher symbol rate, Tx and Rx equalizers are needed.

You can use the MIPI C-PHY Compliance Kit template, `mipicphy_template1`. The topology in this template includes blocks—CPhyTx and CPhyRx—each having three terminals for signals without any crosstalk.

Compliance checks are done using time domain channel simulation for Eye Metrics and S Parameter Analysis for Interconnect Specifications.



#### 100Base-T1 Compliance

100BASE-T1 is an automotive Ethernet standard that runs at 100Mbps, using PAM3 signaling with levels of -1, 0, and 1V. The Tx (transmitter) is AC coupled and will have a max peak-to-peak swing of 2.2V. The channel consists of PCBs, connectors, and long cables.

With the 100BASE-T1 compliance kit users can run a 100BaseT1 compliance based on the latest version of the 100BASE-T1 specification available at <https://standards.ieee.org/findstds/standard/802.3bw-2015.html>. This specification defines the Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable.

## Topology Workbench User Guide

### Working with Compliance Kits

The 100BASE-T1 compliance kit covers the following as described in the 100BASE-T1 specification sections 96.5 and 96.7:

- Transmitter electrical specifications
- Receiver electrical specifications
- Cabling system characteristics

#### ***Compliance Items for Tx***

For Tx compliance, all the tests are made at the MDI placed on the Tx end. The red arrow in the figure indicates where the measurements are made in the channel.

### 100BASE-T1 Compliance Kit

**Choose Compliance Items**

No.	Parameter	Values	<input type="checkbox"/>
<b>Tx Tests</b>			
1	Test mode 1--Transmit droop test mode	45%	<input type="checkbox"/>
2	Test mode 2--Transmit jitter test in MASTER mode	50 ps RMS	<input type="checkbox"/>
3	Test mode 4--Transmit distortion test		<input type="checkbox"/>
4	Test mode 5--Normal operation at full power (for the PSD mask)		<input type="checkbox"/>
5	Transmitter peak differential output	2.2 V	<input type="checkbox"/>

**Link Segment**  
Up to 15 m single balanced twisted-pair cabling with up to 4 in-line connectors and two mating connectors

Mating Connectors  
In-line Connectors

**Figure 96-28—Link segment definition**

The Tx compliance contains the following tests:

- Test mode 1 – Transmit droop test mode
- Test mode 2 – Transmit jitter test in MASTER mode

- Test mode 4 – Transmit distortion test
- Test mode 5 – Normal operation at full power (for the PSD mask) (96.5.4.4)
- Transmitter peak differential output

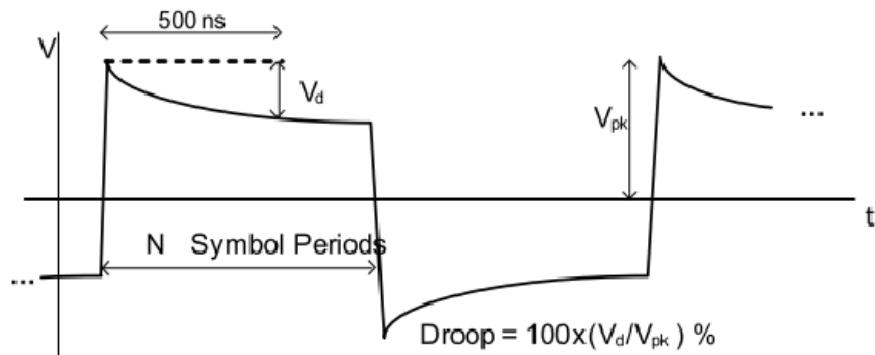
### ***Test mode 1 – Transmit droop test mode***

This test measures the strength of a transmitter based on the long channel it needs to drive.

The droop test is run with the following settings:

- The Tx generates a bit stream of continuous 40 ‘0’s and 40 ‘1’s.
- Run channel simulation at 66.66MHz.
- Apply a high pass filter to model the droop. This is done using an AMI model at the Tx.

The droop values for the positive and negative pulse is measured using the equation provided in the specification:



### ***Test mode 2 – Transmit jitter test in MASTER mode***

This test is to model any jitter in the Tx that may be present in the Tx. Transmit jitter is measured using the same template used for droop test. The AMI model is not used for this test. The settings used for this test are:

- An oscillating 0101 pulse is sent through the transmitter using PRBS2.
- Run channel simulation and observe the report to get the eye jitter(P-P) at BER1e-10.
- Divide by 12.723 to get RMS Jitter using the following formula:

$$Jitter_{P-P} = \alpha * Jitter_{RMS}$$

## Topology Workbench User Guide

### Working with Compliance Kits

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Where alpha is calculated using the table provided below:

**Table 1. Scaling Factors ( $\alpha$ ) for Different BER Tolerances**

BER	$\alpha$
$10^{-3}$	6.180
$10^{-4}$	7.438
$10^{-5}$	8.530
$10^{-6}$	9.507
$10^{-7}$	10.399
$10^{-8}$	11.224
$10^{-9}$	11.996
$10^{-10}$	12.723
$10^{-11}$	13.412
$10^{-12}$	14.069
$10^{-13}$	14.698
$10^{-14}$	15.301
$10^{-15}$	15.883
$10^{-16}$	16.444

Source: [pdfserv.maximintegrated.com/en/an/AN462.pdf](http://pdfserv.maximintegrated.com/en/an/AN462.pdf)

### ***Test mode 4 – Transmit distortion test***

This test is grayed out in the current version.

### ***Test mode 5 – Normal operation at full power (for the PSD mask) (96.5.4.4)***

This test measures the power density in the Tx and checks to see if the average PSD of the output waveform satisfies the PSD mask given in the spec.

Power Spectral Density (PSD) is the average noise power per unit of bandwidth. PSD is expressed in dBm/Hz where power is expressed in logarithmic terms with respect to a milliwatt. The settings used for this test are:

- Random bits are generated at the Tx in PAM3 mode.

## Topology Workbench User Guide

### Working with Compliance Kits

- PSD is calculated using the following formula:

$$PSD_{dBm/Hz} = 20 \log_{10} \left( \frac{|\mathcal{F}\{x(t)\}|}{\sqrt{L f_s}} \right) + 30$$

Where, L is the number of samples of the signal x(t), and fs is the sampling frequency.

#### ***Transmitter peak differential output***

The transmitter peak differential output is the max-min voltage difference of the waveform at the Tx MDI.

#### ***Compliance Items for Rx***

For Rx compliance, the cabling system characteristics can be checked along with tests of the *Eye Height* and *Eye Width*.

## 100BASE-T1 Compliance Kit

**Choose Compliance Items**

No.	Parameter	Values	
<b>Cabling system characteristics</b>			
1	Characteristic impedance		<input type="checkbox"/>
2	Insertion loss (Equation 96-6)	SDD21	<input type="checkbox"/>
3	Return loss (Equation 96-7)		<input type="checkbox"/>
4	Mode conversion loss (Equation 96-8)		<input type="checkbox"/>
<b>Rx Tests</b>			
5	Eye Height	mV	<input type="checkbox"/>
6	Eye Width	UI	<input type="checkbox"/>

**Link Segment**

Up to 15 m single balanced twisted-pair cabling with up to 4 in-line connectors and two mating connectors

## **USB 3 - Gen 1 Compliance**

The SLA workflow supports compliance testing process for USB 3.0 serial links. The USB3 standard also ensures compliance on four different configurations that include the Tx and Rx compliance tests for the host and the device. The following templates are available:

- SuperSpeed\_Rx\_Device
- SuperSpeed\_Rx\_Host
- SuperSpeed\_Tx\_Device
- SuperSpeed\_Tx\_Host

These templates have the following key features:

- You have the ability to replace behavioral SPICE Tx and Rx blocks with IBIS Tx and Rx blocks. This makes it easy for you to use your own IBIS-AMI models from your suppliers.
- In addition to the flexibility of using your own supplier-provided IBIS and IBIS-AMI models, Topology Workbench installation includes templates of compliance kit models. These templates have specification-level Tx and Rx IBIS-AMI models that use IBIS [External Model] syntax to point to behavioral SPICE subcircuits.
- The templates clearly demarcate the Host and Device components.

## **USB 3 - Gen 2 Compliance**

In addition to performing USB 3 - Gen 1 compliance checks, you can check USB3 - Gen2 SuperSpeed Plus compliance with the Universal Serial Bus 3.1 specification.

These specifications check for compliance on four different configurations including the Tx and Rx compliance tests for the host and the device. The following templates are included for this compliance check:

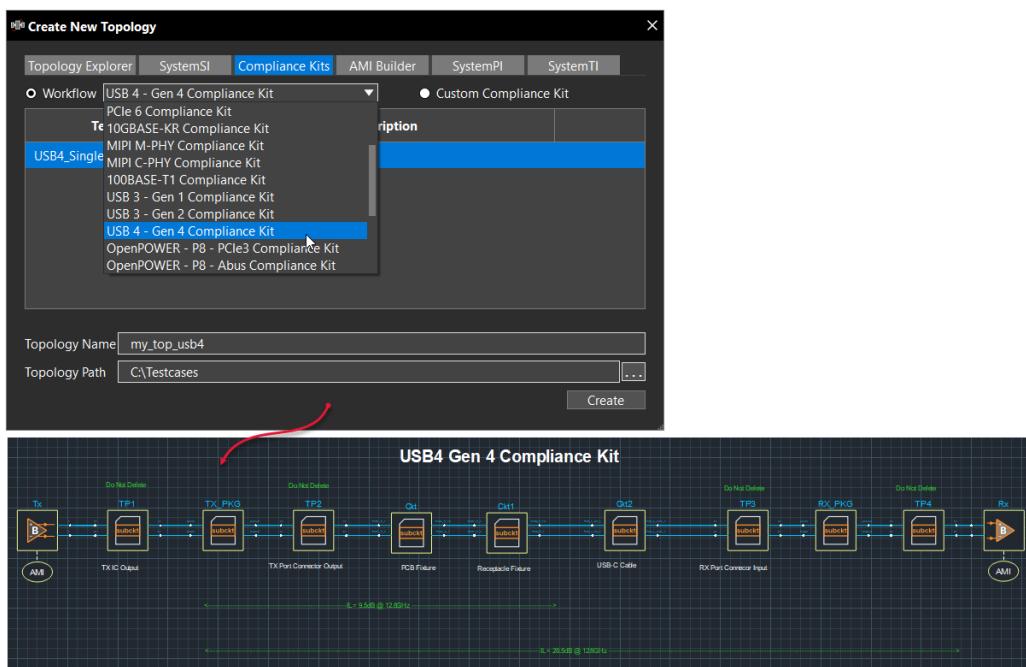
- SuperSpeedPlus\_Rx\_Device
- SuperSpeedPlus\_Rx\_Host
- SuperSpeedPlus\_Tx\_Device
- SuperSpeedPlus\_Tx\_Host

# Topology Workbench User Guide

## Working with Compliance Kits

### USB 4 - Gen 4 Compliance

With the USB 4 - Gen 4 Compliance Kit support, you can run PAM3 simulation at a defined Baud Rate for a single-lane topology comprising Tx, Rx, Tx and Rx Port Connectors, PKG, Cable, and fixtures. Except for a few components labeled as *Do Not Delete* in this sample topology, you can replace workspace items in the single-lane topology with your own design models.



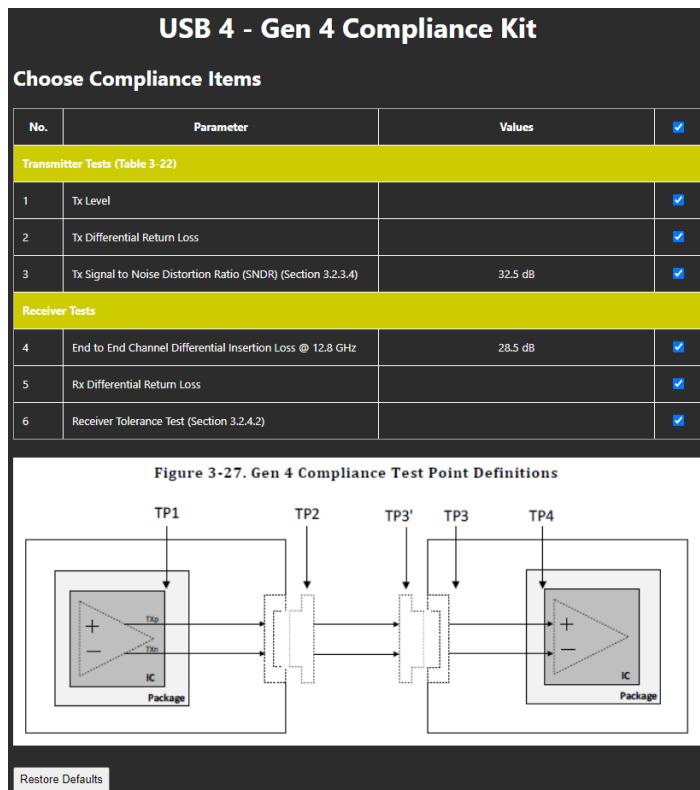
The related compliance items include the transmitter and receiver tests for parameters such as:

- Tx level, Tx differential return loss, and Tx signal to noise distortion ratio (SNDR) (Section 3.2.3.4)

# Topology Workbench User Guide

## Working with Compliance Kits

- Rx end-to-end channel differential insertion loss, Rx differential return loss, and Rx tolerance test (Section 3.2.4.2)



# Topology Workbench User Guide

## Working with Compliance Kits

A compliance report is generated on completion of the checks. This report contains a table with *Summary Results* of the transmitter and receiver tests along with their *Pass/Fail* status.

The screenshot shows a compliance report for a USB 4 channel. At the top, there's a toolbar with 'Start Page', 'usb4\_single.l...', 'Choose Complia...', 'Measuremen...', 'Compliance...', and 'compliance\_rep...'. Below the toolbar is the Cadence logo. The main title is 'USB 4 - Gen 4 Compliance Report'. Subsequent sections include:

- Figure 3-27. Gen 4 Compliance Test Point Definitions:** A diagram showing two IC packages connected by a differential pair. Four test points (TP1, TP2, TP3, TP4) are indicated: TP1 is at the output of the first IC, TP2 is between the two ICs, TP3 is at the input of the second IC, and TP4 is at its output. Arrows point from the labels to the respective connection points.
- Useful Links:**
  - Cadence website: <http://www.cadence.com>
- General Information:**
  - Project File: my\_top\_usb4.topx
  - Circuit Simulator: SPDSIM
- Summary of Results:**

This report shows the results of the compliance testing using Cadence TopXp. The channel simulated violates one or more compliance requirements.
- Transmitter Tests (Table 3-22):**

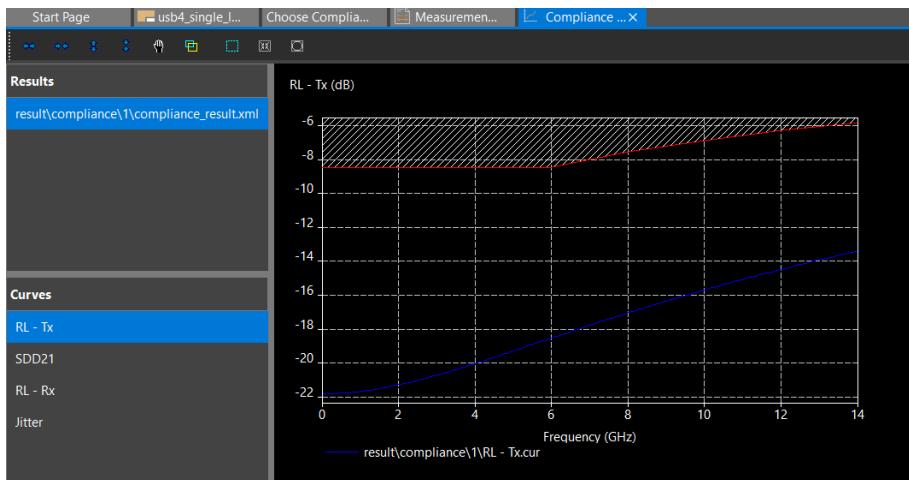
Item	Value	Simulation Results	Pass/Fail
Tx Level	800 mV	800.009	Pass
Tx Differential Return Loss		RL_Tx	Pass
Tx Signal to Noise Distortion Ratio (SNDR) (Section 3.2.3.4)	32.5 dB	30.881	Fail
- Receiver Tests:**

Item	Value	Simulation Results	Pass/Fail
End to End Channel Differential Insertion Loss @ 12.8 GHz		SDD21	Pass
Rx Differential Return Loss		RL_Rx	Pass
Receiver Tolerance Test (Section 3.2.4.2)		Jitter	Pass

## Topology Workbench User Guide

### Working with Compliance Kits

Clicking the links given in the *Summary Results* column opens the *Compliance Curves* tab containing the waveforms of the results.



### OpenPOWER Compliance

The P8 (PCIe, Abus, and DMI), P8+ (DMI, NVLink, PCIe3, and Xbus), and P9 (NVLink, PCIe4, and Xbus) compliance kits are built for the member companies of the OpenPOWER consortium. P8 stands for the IBM Power 8 processor, which is also the first processor supporting the new OpenPOWER software environment. P9 is the next processor in the series.

To test compliance of the various component of the bus, IBM devised the frequency domain compliance testing methodology. The frequency domain compliance testing analyzes the return loss of the through channel and also various crosstalk measurements to analyze the quality of the channel. For the compliance check, measurement values are matched against a table provided by IBM for each metric. If all the metrics pass for a particular index, the channel passes the compliance.

This feature enables you to run the compliance for:

- OpenPOWER P8
  - PCIe3 compliance for
    - Single-channel for both pre- and post-layout topologies
    - Crosstalk channel for both pre- and post-layout topologies
  - Abus compliance for
    - Single-channel for both pre- and post-layout topologies

## Topology Workbench User Guide

### Working with Compliance Kits

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- Crosstalk channel for both pre and post layout topologies
- DMI channel compliance checks for one card or two cards for:
  - Pre/post for single/crosstalk for P8 to Memory Controller, and Memory Controller to P8
- DMI channel compliance checks for one card and two cards for
  - Pre/post for Single/crosstalk for P8 to Memory Controller
  - Memory Controller to P8 modules
  - P8+ DMI, NVLink, PCIe3 and Xbus
- OpenPOWER P8+
  - DMI
    - Single-channel for both pre- and post-layout topologies
    - Xtalk channel for both pre and post layout topologies
  - NVLink
    - Single-channel for both pre- and post-layout topologies
    - Xtalk channel for both pre and post layout topologies
  - PCIe3
    - Single-channel for both pre- and post-layout topologies
    - Xtalk channel for both pre and post layout topologies
  - Xbus
    - Single-channel for both pre- and post-layout topologies
    - Xtalk channel for both pre and post layout topologies
- OpenPOWER P9
  - NVLink
    - Single-channel for both pre- and post-layout topologies
    - Xtalk channel for both pre and post layout topologies
  - PCIe4
    - Single-channel for both pre- and post-layout topologies

- Xtalk channel for both pre and post layout topologies
- Xbus
  - Single-channel for both pre- and post-layout topologies
  - Xtalk channel for both pre and post layout topologies

The compliance check tests each column and each row to determine whether the insertion loss and crosstalk measurement of the channel satisfy the various metrics—ILF, ILD, ILDB, ILDA, SXTF, SXTB, and SXTA.

 *Important*

This compliance check has different tasks. You do not need to select a particular compliance test as is needed with other compliance kits.

For detailed information, refer to the [Checking for OpenPOWER Compliance](#) section later in this chapter.

## Creating Customized Compliance Kits

The standard built-in compliance kits shipped with Topology Workbench are a collection of the most frequently used compliance checks that you can customize to fit your own specifications. However, in addition to this capability, Topology Workbench lets you create customized compliance kits for specifications that are currently not covered in the standard built-in compliance kits.

 *Important*

This feature is available only in the Serial Link Analysis (SLA) and Compliance Kits workflows.

### **Related Topics**

- [Start Custom Compliance Kits Workflow](#)
- [Set the Analysis Options for Custom Compliance Kits](#)
- [Configure the Ports Automatically](#)
- [Choose the Required Compliance Items](#)
- [Customize the Report](#)

## Topology Workbench User Guide

### Working with Compliance Kits

- [Run the Compliance Check](#)
- [Save the Compliance Kit](#)
- [Load a Compliance Kit](#)
- [Browse Saved Simulation Results of a Custom Compliance Kit](#)

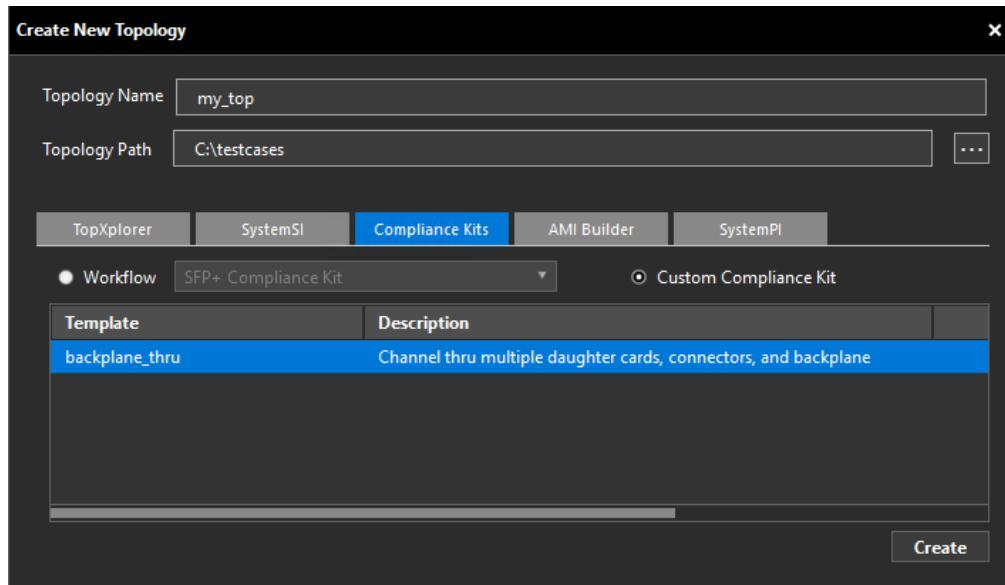
## Start Custom Compliance Kits Workflow

To create customized compliance kits, you can use one of the following two methods:

- [Create a New Template-Based Custom Compliance Kit](#)
- [Switch Workflow to Custom Compliance Kits](#)

### Create a New Template-Based Custom Compliance Kit

1. Start Topology Workbench.
2. Click *New...* from the *Start Something Awesome* section on the [Start Page](#) tab. The *Create New Topology* dialog box is displayed.
3. Specify a *Topology Name* and *Topology Path*.
4. Click the *Compliance Kits* tab.



**Note:** In the *Compliance Kits* tab, you have an option choose to use a specific workflow

## Topology Workbench User Guide

### Working with Compliance Kits

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and standard built-in compliance kit combination, or you can create a custom compliance kit. For more information about the former, refer to [Using the Standard Built-In Compliance Kits](#).

5. Select the *Custom Compliance Kit* option. The table on the tab is refreshed to list the available default template to start the process.

6. Select the required template in the template.

**Note:** Currently, as only one template is available, it is selected by default. Therefore, [step 6](#) can be skipped.

7. Click *Create*.

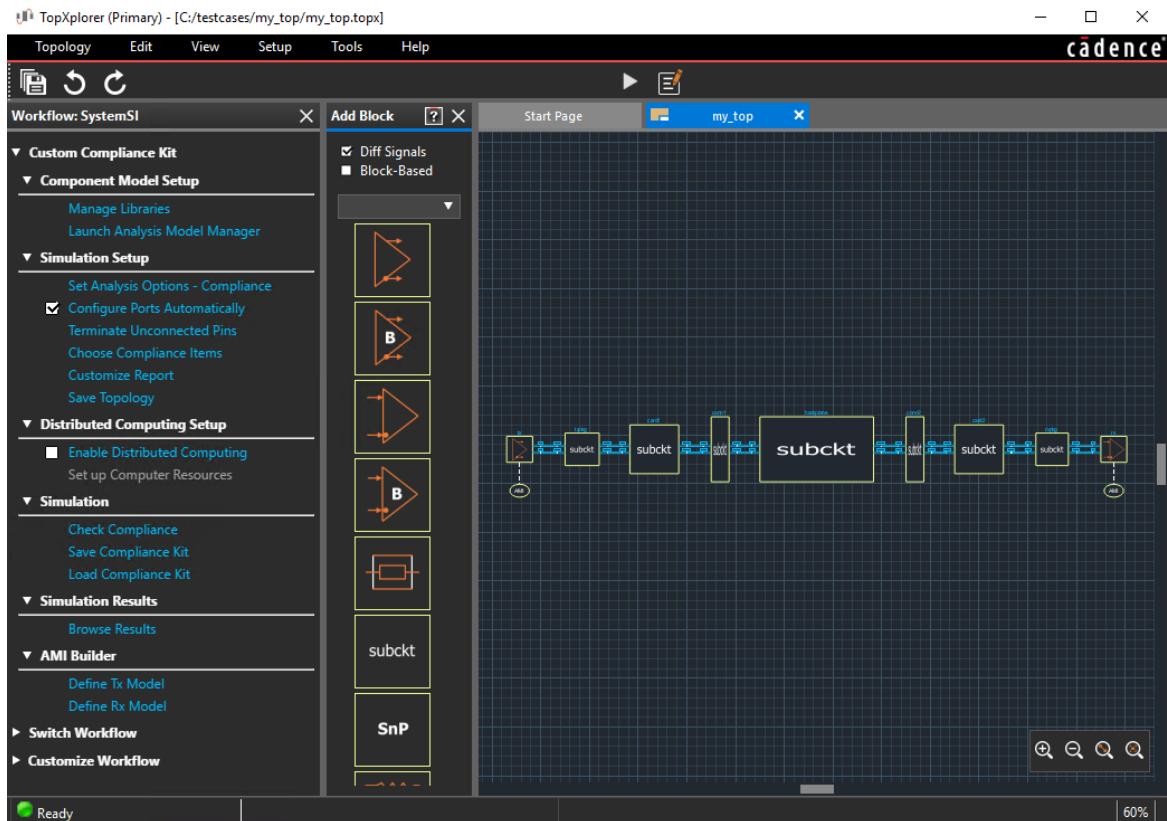
The Topology Workbench window is refreshed as following:

- A tab with the given *Topology Name* opens next to the [Start Page](#).
- The [Layout Canvas](#) is populated with the blocks as per the selected default template.
- The [Workflow Panel](#) opens with a list of tasks you can perform for the selected type of compliance check.

# Topology Workbench User Guide

## Working with Compliance Kits

- The Floating Toolbar opens with a list of various types of available blocks.



## Switch Workflow to Custom Compliance Kits

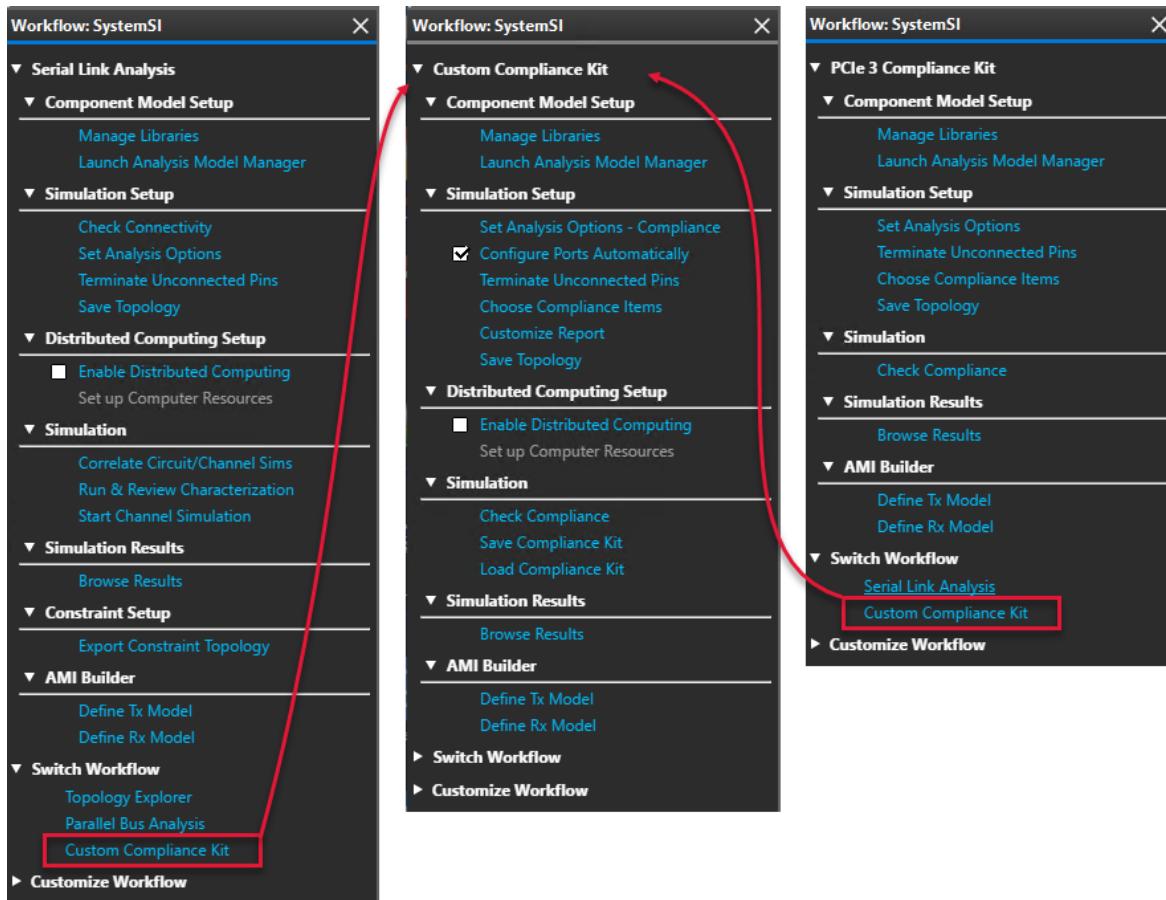
To switch to the Custom Compliance Kit workflow from the SLA workflow or while working with standard built-in compliance kits:

- Click the *Switch Workflow* schema in the *Workflow* panel. The workflows you can switch to are displayed.

# Topology Workbench User Guide

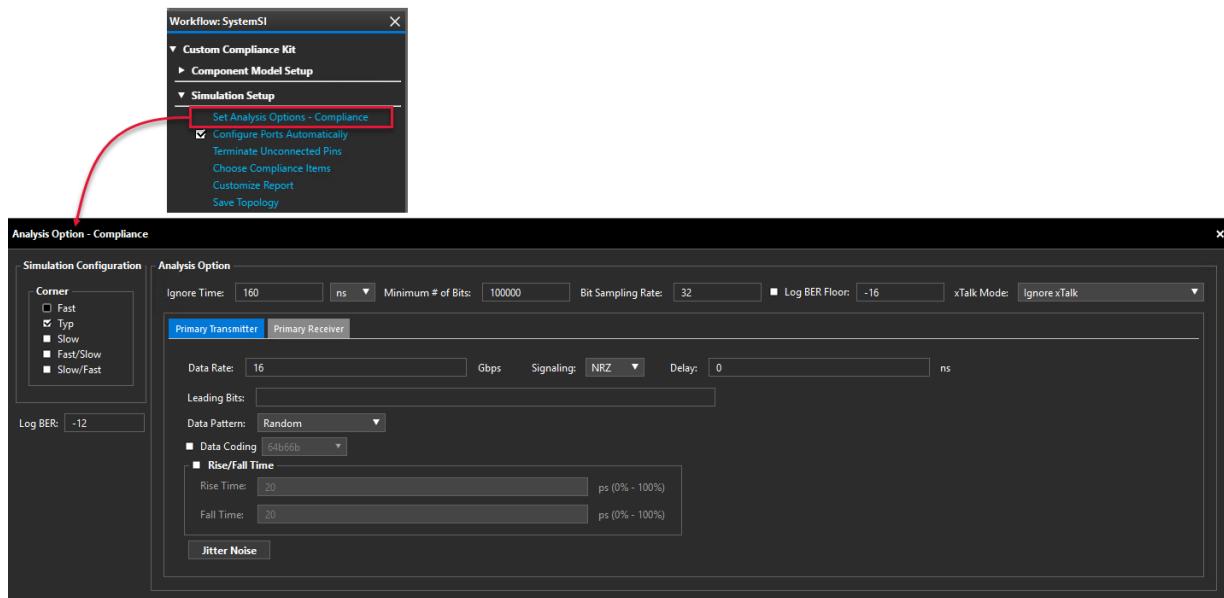
## Working with Compliance Kits

2. Click *Custom Compliance Kit*. The *Workflow* panel refreshes to show the options available in the *Custom Compliance Kit* workflow.



## Set the Analysis Options for Custom Compliance Kits

1. Click *Set Analysis Options - Compliance* from the *Simulation Setup* schema of the *Workflow* panel. The *Analysis Option - Compliance* dialog box opens.



2. Define the analysis settings to use for the compliance runs and click *OK* to save.

The *Analysis Option - Compliance* dialog box lets you set the following:

### **Simulation Configuration**

<i>Corner</i>	Select at least one of the following check boxes to specify the <i>Corner</i> setting: <i>Slow</i> , <i>Fast</i> , <i>Typ</i> , <i>Fast/Slow</i> , and <i>Slow/Fast</i> . By default, <i>Typ</i> is selected.
<i>Log BER</i>	Specify the bit error ratio at which the BER eye is generated. You can enter a negative integer within the range of -3 to -20. By default, it is set to -12.

### **Analysis Option**

<i>Ignore Time/Bits</i>	Enter the initial time/bits that should be ignored from the waveform so that the data is not corrupted with the startup time transients. By default, its unit is nanoseconds ( <i>ns</i> ), but you can change the unit to <i>bits</i> , if needed.
<i>Minimum # of Bits</i>	Enter the minimum number of bits to be simulated.

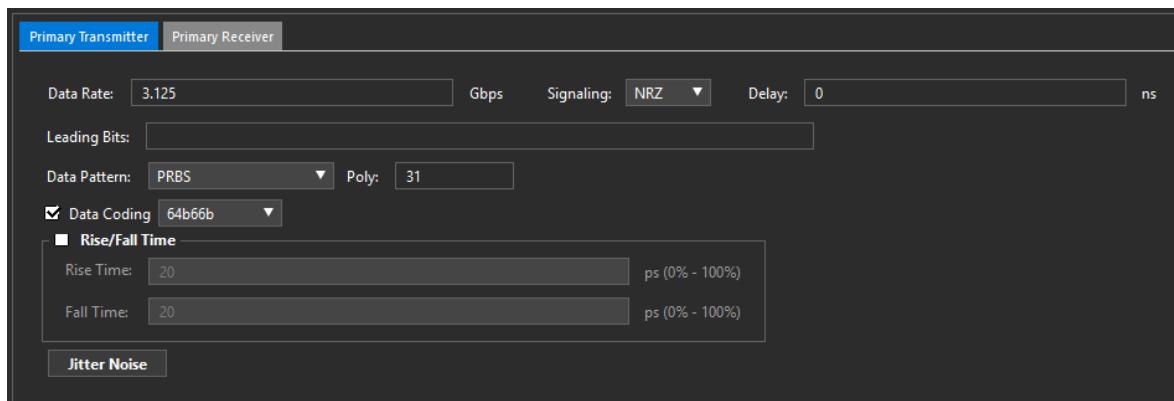
## Topology Workbench User Guide

### Working with Compliance Kits

<i>Bit Sampling Rate</i>	Enter a value that the channel simulator uses to control the granularity for computing the eye density.
<i>Log BER Floor</i>	Select the check box if the specified minimum Bit Error Rate (BER) should be used in the simulation. Also, set a value in the adjacent text box.
<i>xTalk Mode</i>	Select from the list which crosstalk mode should be used when you perform Crosstalk Channel Analysis in the SLA workflow. The <i>xTalk Mode</i> is set to <i>Ignore xTalk</i> by default. The following modes are also supported: <ul style="list-style-type: none"><li>■ <i>Invert All Aggressor Stimulus</i></li><li>■ <i>Use Aggressor Stimulus As Defined</i></li><li>■ <i>Random Aggressor Stimulus</i></li></ul>

### **Primary Transmitter**

Set the analysis options for the primary transmitter (Tx). The values you set in this tabs are used as the default for the compliance kit.

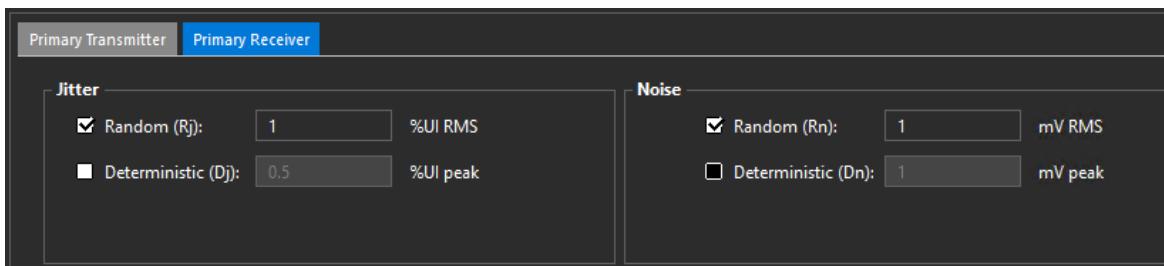


**Data Rate**      Specify the nominal data rate at which the system will operate. It is set to 8 by default.

<i>Signaling</i>	Set the signaling type for the stimulus pattern to generate multi-level stimulus pattern for simulation. <i>NRZ</i> is the default option, which indicates the traditional binary signaling. Selecting <i>PAM3</i> or <i>PAM4</i> triggers appropriate multi-level signals for the incoming bit stream stimulus for the transmitter, producing multi-level signals at the associated receivers.
	<b>Note:</b> If the Tx or Rx AMI models contain the reserved parameter, <i>Modulation</i> , then the setting of this reserved parameter dictates the values of the <i>Signaling</i> field. As a result, the field might be disabled.
	When PAM4 signaling is selected, only three PAM eyes are printed in the simulation results.
<i>Delay</i>	Specify the delay time for launching ramp-up stimulus. The impulse calculation is also shifted by the time specified in this text box.
<i>Leading Bits</i>	Enter the leading bits to change the phase alignment during crosstalk simulation. It can also be used before the beginning of a bit stream for training pattern.
<i>Data Pattern</i>	Set the <i>Data Pattern</i> and the associated settings such as <i>Data Coding</i> and <i>Rise/Fall Time</i> . For details about each enabled setting, refer to the <a href="#">Serial Link Analysis: Controls for Setting Stimulus Pattern</a> section.
	<b>Note:</b> If the Tx or Rx AMI models contain the reserved parameter, <i>PAM4_Mapping</i> , then the setting of this reserved parameter dictates the values of the <i>Data Coding</i> field. As a result, the field might be disabled.
<i>Jitter Noise</i>	Click <i>Jitter Noise</i> to display the <i>Jitter &amp; Noise</i> dialog box where you can specify the parameters that need to be incorporated into the stimulus bit stream applied to the primary transmitter. For details about each option that can be set in this dialog box, refer to the <a href="#">Setting Jitter and Noise Parameters</a> section.

## Primary Receiver

Click this tab and set the analysis options for the primary receiver (*Rx*). The values you set in this tabs are used as the default for the compliance kit.



### Jitter

Specify the jitter and noise values for the primary receiver. For details about each option that can be set in this dialog box, refer to the [Setting Jitter and Noise Parameters](#) section.

### Noise

## Configure the Ports Automatically

- Select *Configure Ports Automatically* in the *Simulation Setup* schema of the *Workflow* panel. This helps to configure the ports automatically for S Parameter extraction.

**Note:** When this check box is selected and you click a *Setup* button in the *Choose Compliance Item* tab, the displayed *S Parameter Extraction - Compliance* dialog box lets you edit only the *General Settings* module. The *Define Ports* and *Select Blocks* modules appear as read-only.

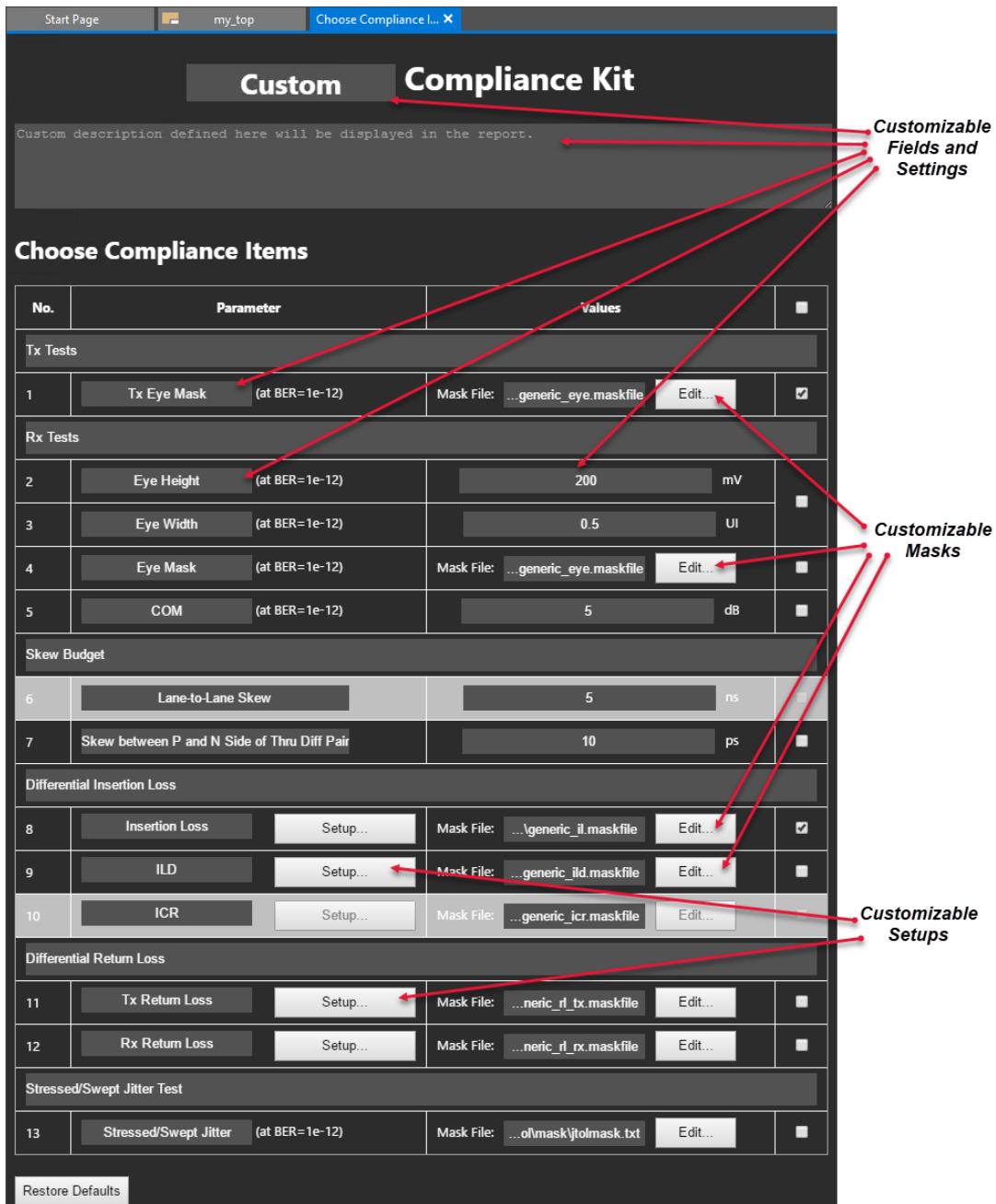
## Choose the Required Compliance Items

The *Custom Compliance Kit* workflow provides to you a set of compliance checks to build a user-defined compliance report. The variety of options include eye quality checks, skew checks, S-parameter checks, and jitter tolerance checks.

# Topology Workbench User Guide

## Working with Compliance Kits

1. Click *Choose Compliance Items* in the *Simulation Setup* schema of the *Workflow* panel. This displays a new tab titled *Choose Compliance Items* next to the tab that contains the topology's layout, as shown below.



On this new tab that opens, you can choose the compliance tests that would be run on the topology. These compliance tests are also included in the compliance report. In addition, use it to assign a name of your choice, provide a custom summary to be

displayed in the report, customize the parameters and values, and attach appropriate masks.

2. Click the text box were *Custom* is written. Replace the text with an appropriate title that you want to print for your compliance kit report.
3. Add a custom description for the report in the text box below the title.
4. Edit the category titles, parameter names, and parameter values as needed in the text boxes provided in the *Parameter* column. The default strings and values are otherwise assigned to each.

**Note:** A number of parameters are checked at the BER value you specified in the *Analysis Option - Compliance* dialog box.

5. Click *Setup* in the *Parameters* column to modify the S Parameter extraction settings for a specific compliance check. The S Parameter Extraction - Compliance dialog box opens with the *Define Ports* module selected by default.

**Note:** If the *Configure Ports Automatically* check box is selected in the *Simulation Setup* schema of the *Workflow* panel, the *General Settings* module of the *S Parameter Extraction - Compliance* dialog box opens by default. The *Define Ports* and *Select Blocks* modules appear as read-only.

6. Click *Edit* in the *Values* column to modify the mask values for a specific compliance check. The Mask Editor dialog box opens. Here, you can change the generic mask file that is assigned to the compliance check and replace it with your own. Otherwise, you can reset or edit the existing mask definitions.

**Note:** For the *Stressed/Swept Jitter Test* check, clicking *Edit* adjacent to the *Mask File* box displays the *Open* dialog box instead of the *Mask Editor*. You can browse and select the required jitter tolerance mask file, and then click *Open* to load it.

7. Select the check boxes in the last column of those parameters for which the compliance checks need to be enabled. The rows in which you customized the setup or updated the mask definition are enable automatically.

**Note:** At the end of the table of compliance items is the *Restore Defaults* button. At any time while configuring the required compliance items, clicking the button resets the parameter values to their respective defaults.

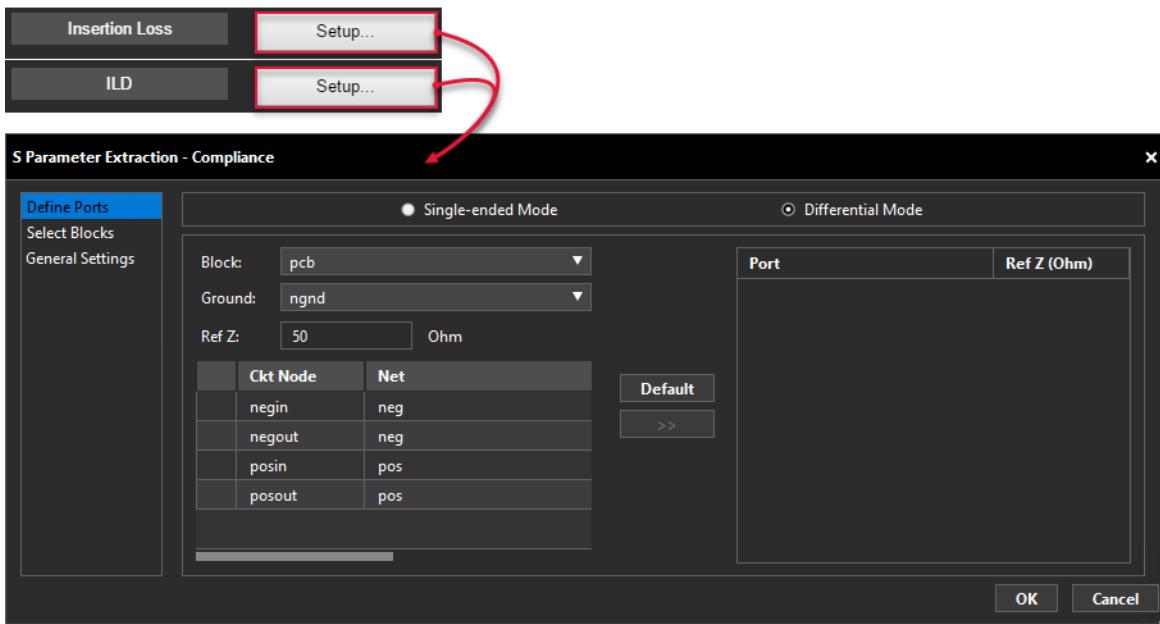
## **S Parameter Extraction - Compliance**

Topology Workbench supports *S Parameter Extraction* for both single-ended nets and differential nets. In the *Choose Compliance Kit* tab, you can set up the rules for extraction of S Parameter definition.

## Topology Workbench User Guide

### Working with Compliance Kits

1. Click the *Setup* button adjacent to a compliance parameter displayed under the *Differential Insertion Loss* or *Differential Return Loss* row. The *S Parameter Extraction - Compliance* dialog box opens.



2. Define ports, select blocks, and define general settings by accessing the three modules in the left pane of the dialog box. To do so, perform [step 2](#) to [step 10](#) and then [step 11](#) to [step 12](#) described in the [Extracting an S Parameter Definition](#) section of [Chapter 2, “Working with Topologies.”](#)
3. Click *OK* to save the updates and then close the dialog box.

Now, the updated check is automatically enabled in the *Choose Compliance Item* tab.

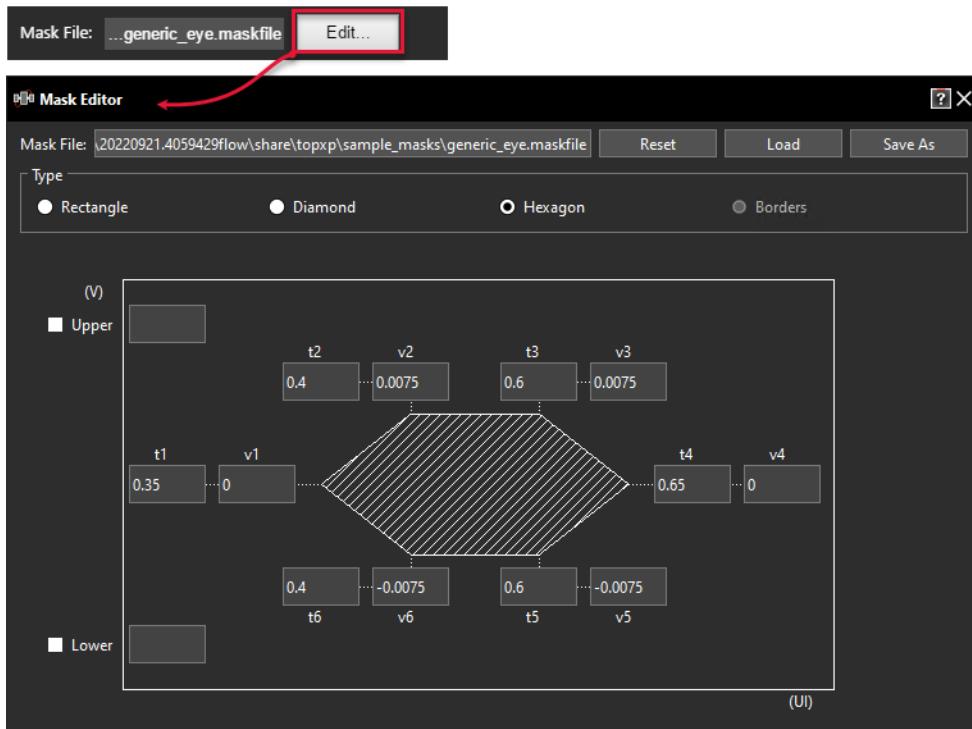
## Mask Editor

The mask values are usually based on industry standards for a channel type or are specific to the SerDes receiver. To edit the generic mask values that are defined by default in the *Choose Compliance Kit* tab:

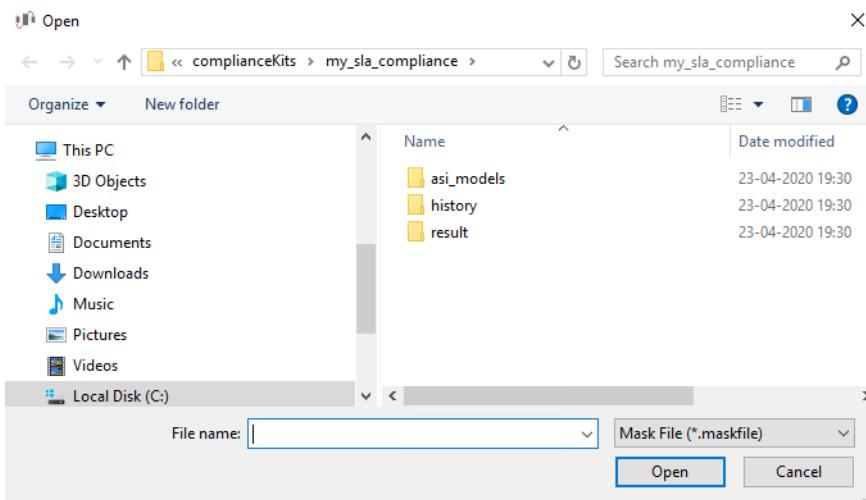
# Topology Workbench User Guide

## Working with Compliance Kits

1. Click the *Edit* button adjacent to the *Mask File* box you want to modify. The *Mask Editor* dialog box opens.



2. Click *Load* to replace the generic mask file with a custom mask file. The *Open* dialog box is displayed.



3. Browse to the location where your custom mask file resides, select the files, and click *Open*. The dialog box closes and the path to the newly loaded file is displayed in the *Mask Editor*.

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### Working with Compliance Kits

#### 4. Select the *Type* of mask and define its values.

- ❑ For an *Eye Mask*, the options available for choice include *Rectangle*, *Diamond*, and *Hexagon* (default). Specify the values for each corner in the given text boxes as shown below for a *Hexagon*:



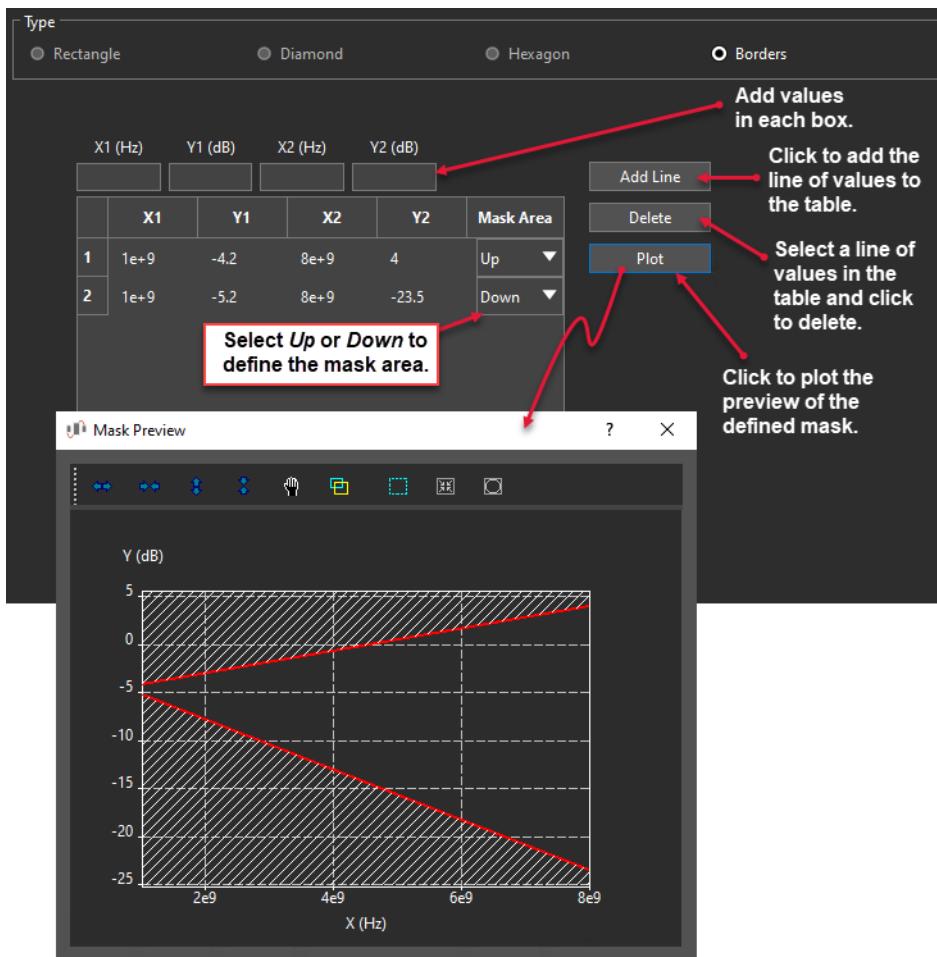
To define upper/lower voltage border for eye masks, select the *Upper* and/or *Lower* check box, and specify the required values in the corresponding text boxes.

- ❑ For masks related to the *Differential Insertion Loss* and *Differential Return Loss* checks, you can define a mask of only *Borders* type. You add a new line of

## Topology Workbench User Guide

### Working with Compliance Kits

values, select the mask area, delete an existing line, and plot a mask preview as shown below:



5. Click *Save As* to save the custom eye mask with a user-defined name at the chosen path.
6. Click *OK* to close the *Mask Editor*. If you click this button without performing step 5, the *Save As* dialog box opens and prompts you to save the updates before you proceed.

Now, the updated check is automatically enabled in the *Choose Compliance Item* tab.

## Customize the Report

The *Custom Compliance Kit* workflow gives you control over what should be displayed in your compliance report including the additional plots.

## Topology Workbench User Guide

### Working with Compliance Kits

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By default, the following information is added to the report:

- *Custom Description*
- *Canvas Snapshot*
- *Channel Model Details*
- *AMI Model Details*
- *Simulation Properties*

You can choose to include the following and a custom description for the compliance report:

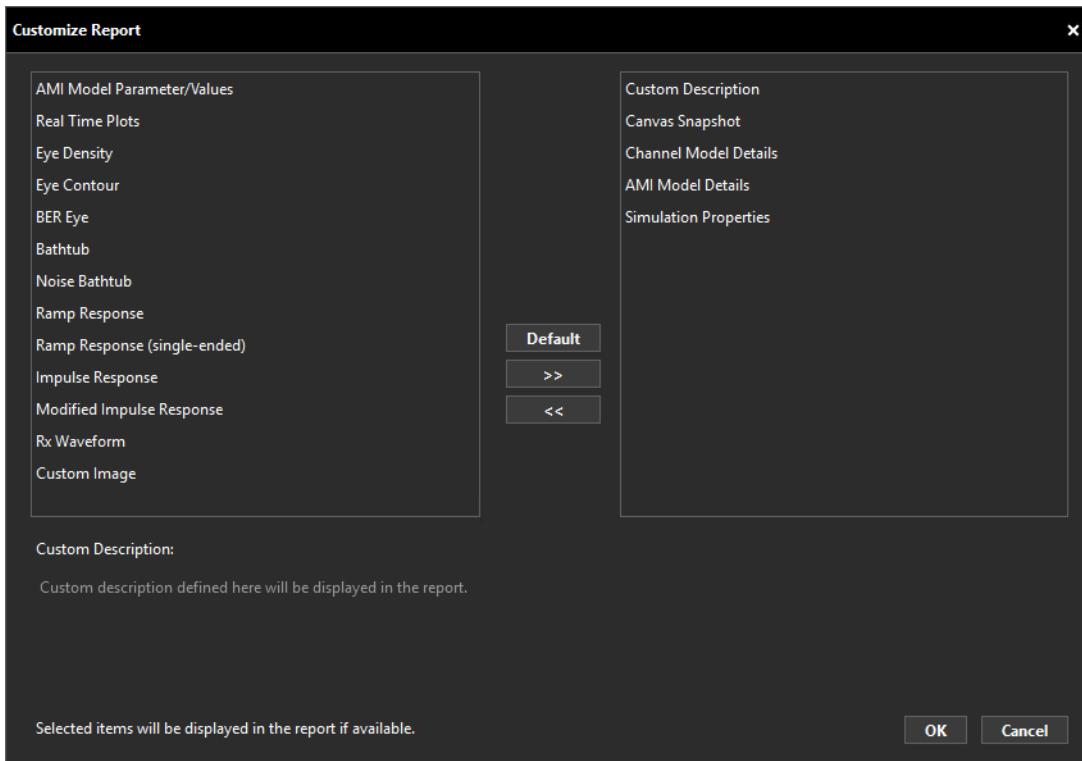
- *AMI Model Parameter/Values*
- *Real Time Plots*
- *Eye Density*
- *Eye Contour*
- *BER Eye*
- *Bathtub*
- *Noise Bathtub*
- *Ramp Response*
- *Ramp Response (single-ended)*
- *Impulse Response*
- *Modified Impulse Response*
- *Rx Waveform*
- *Custom Image*

To customize the report:

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### Working with Compliance Kits

1. Click *Customize Report* in the *Simulation Setup* schema of the *Workflow* panel. The *Customize Report* dialog box opens with the custom report items listed in the left pane and the default report items in the right pane.



2. Select a custom report item from the left pane.
3. Click the **>>** button to move it to the right where the default report items are displayed along with the other chosen custom report items.
4. Repeat step 3 for all other required custom report items.
5. Similarly, you can remove a default or custom report item that is not relevant for your custom compliance report. For this, select the unwanted report item and click the **<<** button.

**Note:** To reset the report items to their default selections, click *Default*.

6. Add a *Custom Description* in the given box. The text input in this box is shown in the custom compliance report.

**Note:** If you added a custom description in the designated box in the *Choose Compliance Items* tab, the *Custom Description* box displays that same content. Otherwise, it displays a default instruction, which is not printed in the custom compliance report. Similarly, any change made to the *Custom Description* in the *Customize*

*Report* dialog box is updated in the *Choose Compliance Items* tab as well.

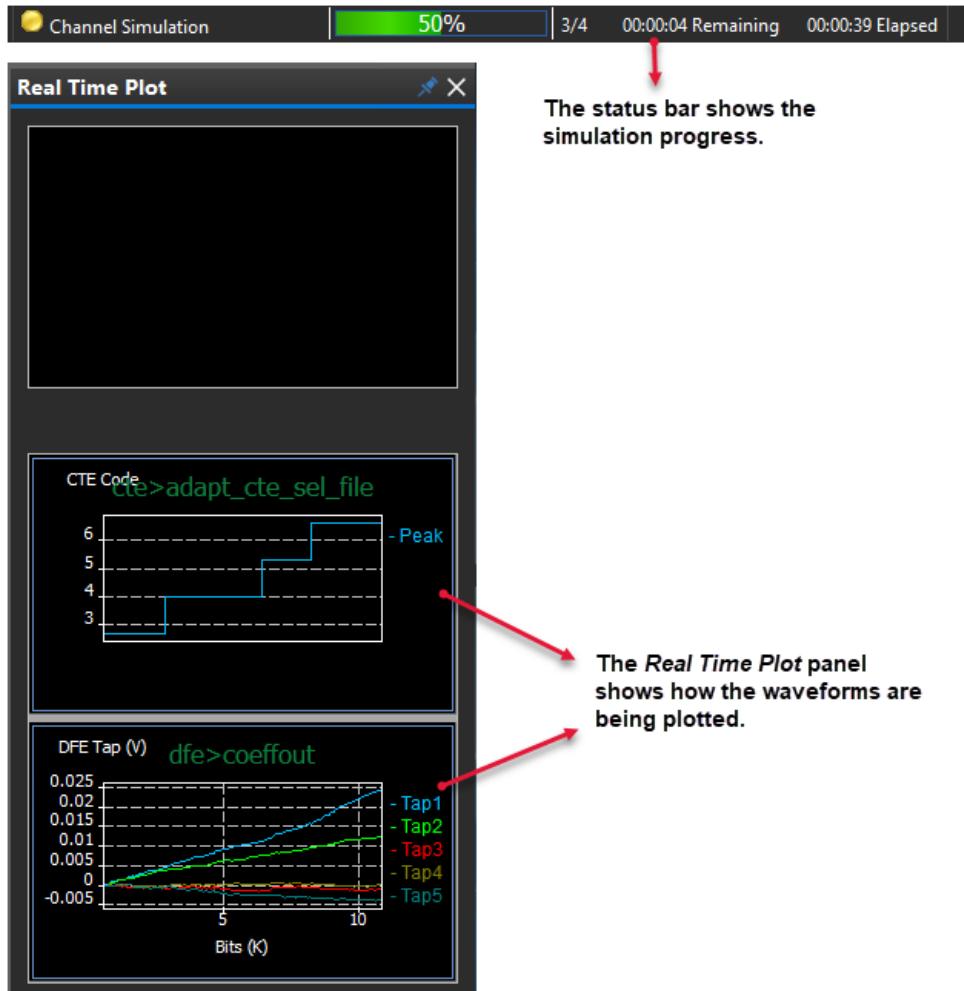
7. Click *OK* to save your customizations and close the dialog box.

## Run the Compliance Check

After you have chosen the required compliance items and have customized the report:

- Click *Check Compliance* in the *Simulation* schema of the *Workflow* panel.

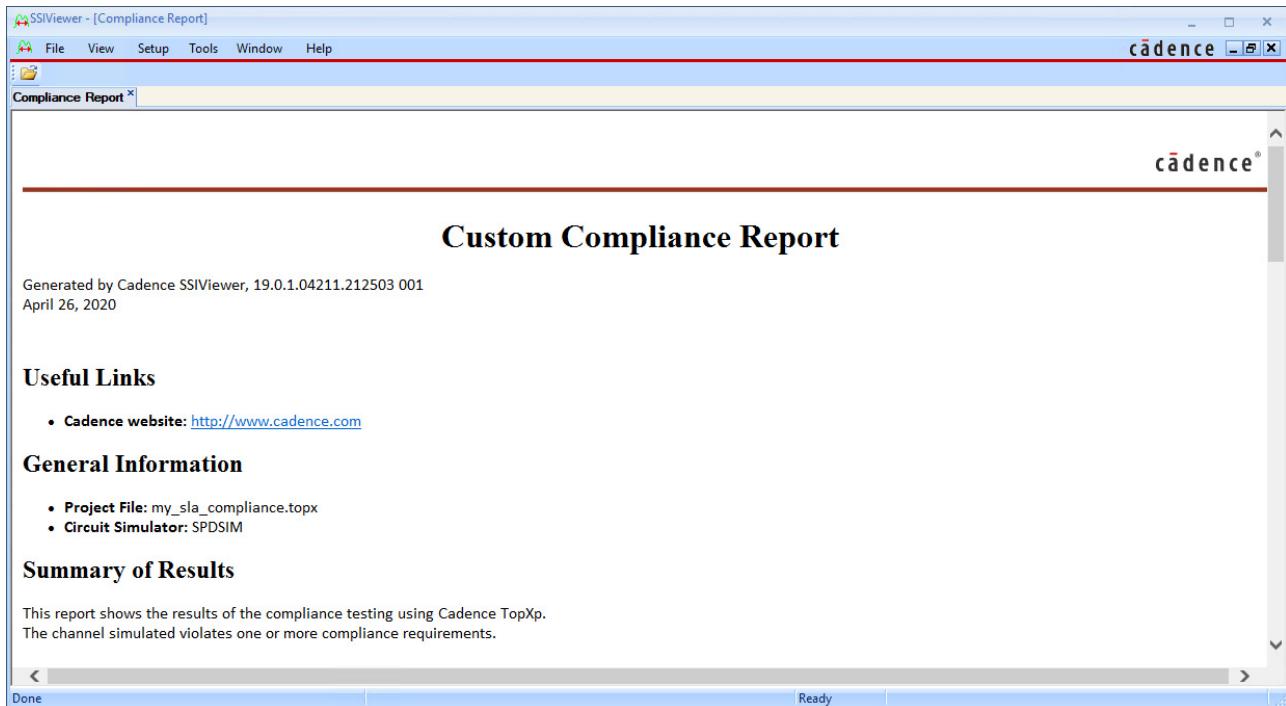
The simulation starts to run and the progress is displayed in the status bar. In addition, the *Real Time Plot* panel shows how the waveforms are being plotted as the simulation progresses.



# Topology Workbench User Guide

## Working with Compliance Kits

After the completion of the simulation run, the SSIViewer window opens with the *Compliance Report* tab displayed. The format of the report is as per the customizations you incorporated.



The *Tools* menu in the SSIViewer window lets you:

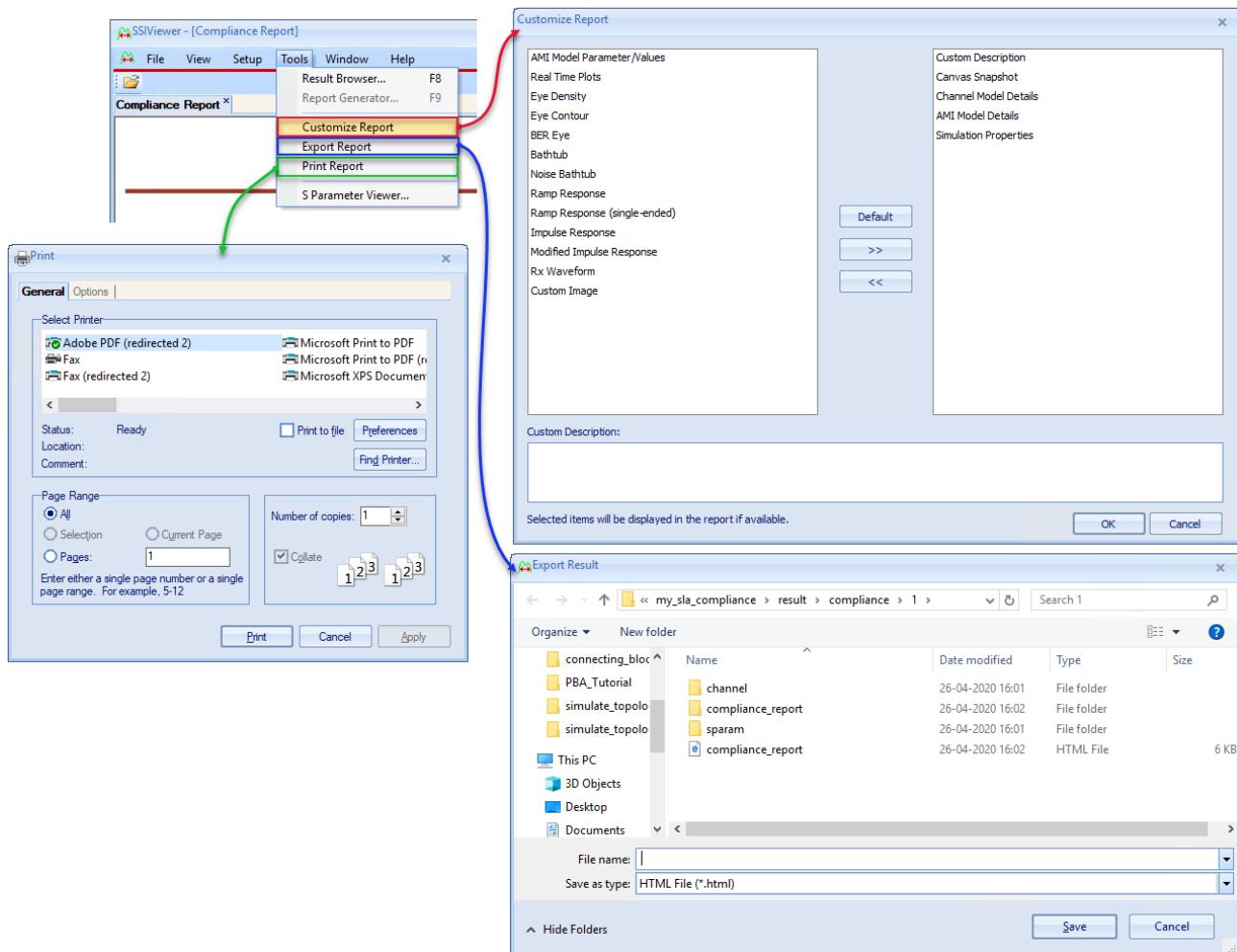
- *Customize Report* if any run-time changes are needed.
- *Export Report* as an HTML file to a specified path.

# Topology Workbench User Guide

## Working with Compliance Kits

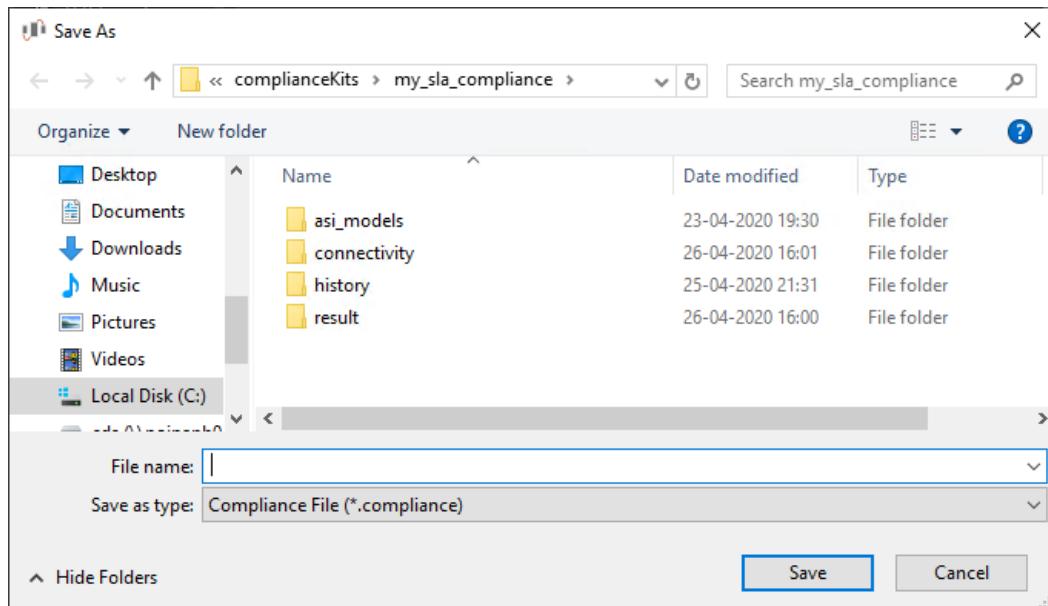
---

- *Print Report* to a printer on the network or to a file, such as, a PDF file using the Adobe PDF printer.



## Save the Compliance Kit

1. Click *Save Compliance Kit* in the *Simulation* schema of the *Workflow* panel to save all custom compliance kit settings in a file of \*.compliance format. The *Save As* dialog box opens.

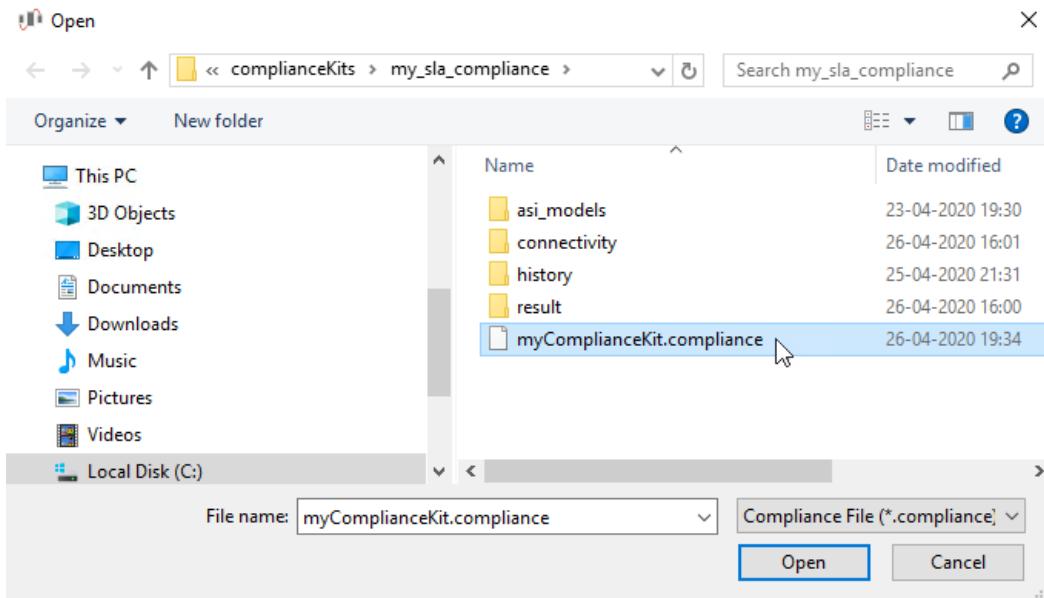


2. Browse to the path where the compliance kit needs to be saved.
3. Click *Save*.

You can save the compliance kit after you have successfully run the *Check Compliance* step and are satisfied with the incorporated customizations. The saved compliance kit, along with the custom mask files that were created, can be stored in a compliance library and reused across other projects.

## Load a Compliance Kit

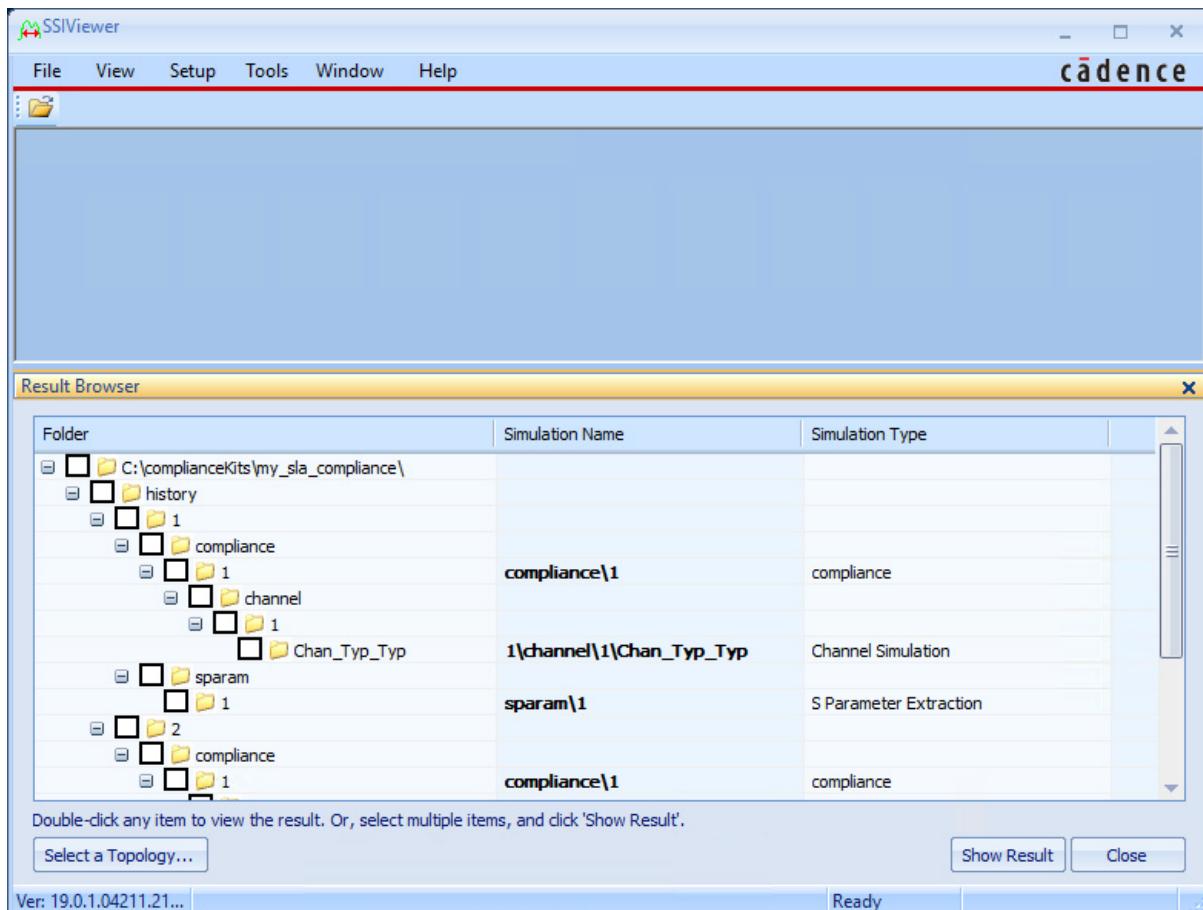
1. Click *Load Compliance Kit* in the *Simulation* schema of the *Workflow* panel to load an existing custom compliance kit from the selected \*.compliance file. The *Open* dialog box opens.



2. Browse and select the custom compliance kit that needs to be loaded.
3. Click *Open*.

## Browse Saved Simulation Results of a Custom Compliance Kit

1. Click *Browse Results* in the *Simulation Results* schema of the *Workflow* panel. The SSIViewer window opens with the *Result Browser* pane.

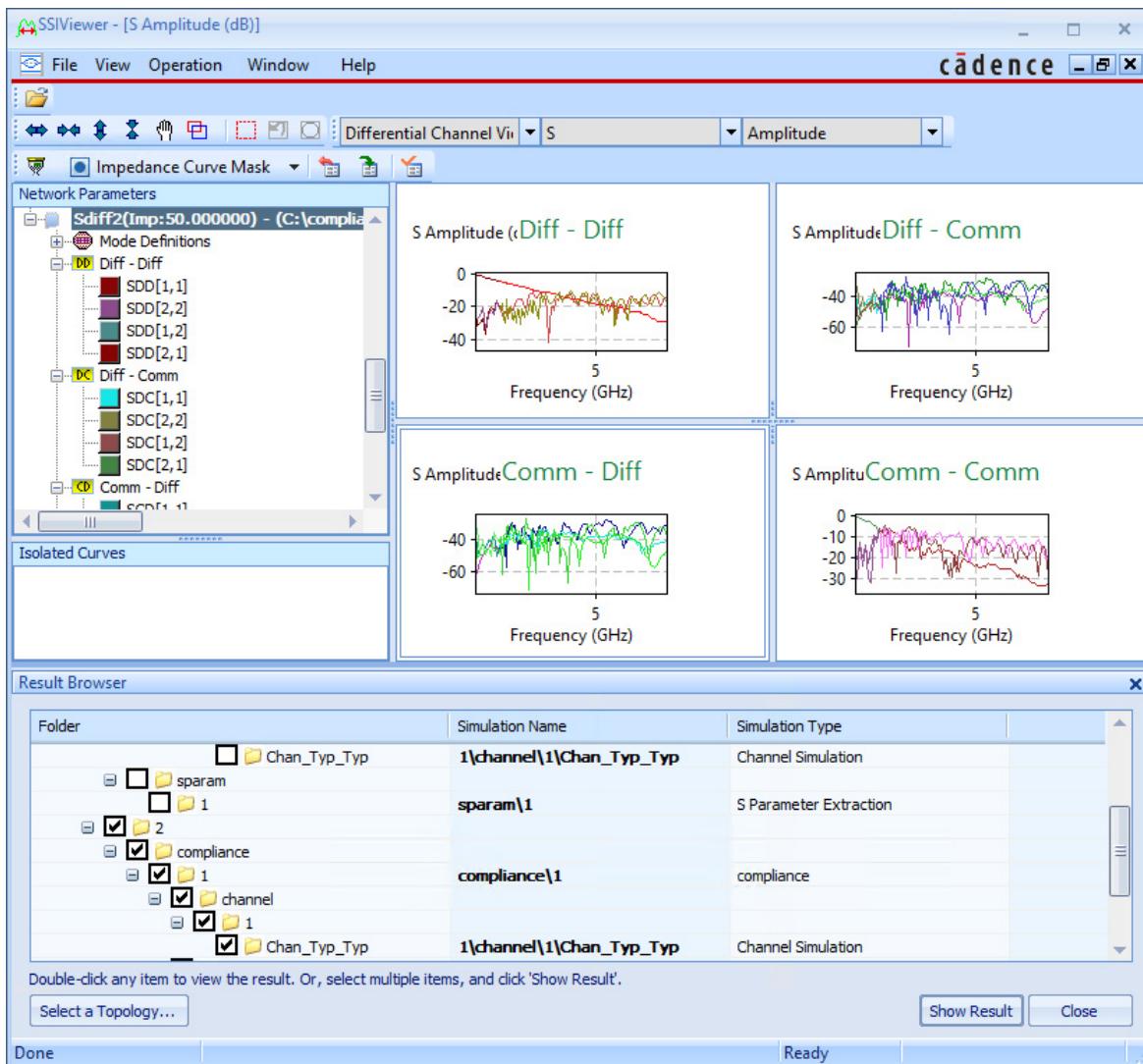


2. Select the check boxes adjacent to the custom compliance kit results you want to browse.

## Topology Workbench User Guide

### Working with Compliance Kits

3. Click *Show Result*. The selected results are displayed in the respective panes as shown below.



## Checking for OpenPOWER Compliance

Topology Workbench includes the frequency-domain compliance kit that OpenPOWER partners can use to determine if their high-speed serial (HSS) bus designs are compliant with IBM standards. The tool determines compliance based on seven frequency domain parameters describing the fully cascaded channel from C4 bump to C4 bump.

The compliance tool kit checks compliance of all HSS buses escaping from the IBM POWER8 processor. As the tool is frequency domain-based, no IBIS AMI models are needed for the

simulation to run. Ensure that you use accurate S-parameter models of the passive components in the channel describing the worst-case design space.

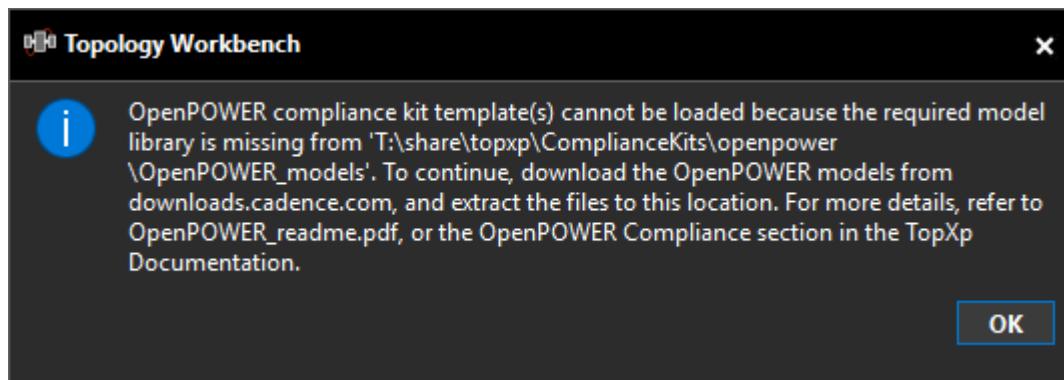
This appendix is for first-time users and will help you to run the simulation and interpret the results. A step-by-step procedure for determining a PCIe Gen3 reference channel's compliance is covered as an example.

### Related Topics

- [Setting Up the Workspace](#)
- [Running the Simulation](#)
- [Interpreting the Simulation Results](#)
- [Underlying Frequency Domain Parameters](#)
- [Using Touchstone Model Substitution](#)

### Before You Begin

In the *Compliance Kits* tab of *Create New Topology* dialog box, when you choose to create a topology using an OpenPOWER Compliance kit template, the following error message might be displayed if the OpenPOWER models are not found:



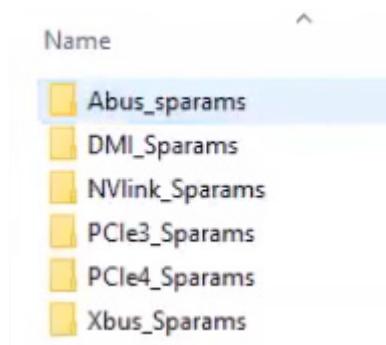
Therefore, before you begin, ensure that you have completed the following tasks to get the required OpenPOWER compliance model files:

1. Login to [downloads.cadence.com](https://downloads.cadence.com).
2. Click the *Sigrity2019* link in WINDOWS or LINUX tab.
3. Download the *.zip* file from the *Library* section.

This zip file contains the OpenPOWER models.

4. Extract the files to: <INSTALL\_DIR>\share\topxp\common\_files

The final structure must be as following:



## Setting Up the Workspace

To set up the workspace for the OpenPOWER compliance kit checks in the SLA workflow, perform the following steps:

1. Start Topology Workbench.
2. Click *New...* from the *Start Something Awesome* section on the [Start Page](#) tab. The *Create New Topology* dialog box is displayed.
3. Specify a *Topology Name* and *Topology Path*.
4. Click the *Compliance Kits* tab.
5. Select an *OpenPOWER Compliance* kit from the *Workflow* list box. The table below the list box is refreshed to list all available default templates associated with the selected compliance kit. For understanding the process, select *OpenPOWER - P8 - PCIe3 Compliance Kit*.
6. Choose a template. The following four templates are displayed: *p8\_pci\_single\_post*, *p8\_pci\_single\_pre*, *p8\_pci\_xt\_post*, and *p8\_pci\_xt\_pre*.
  - Two are pre-layout templates and two are post-layout templates
  - The *single* layouts represent only the through channel and the *xt* layout also includes the crosstalk aggressors.

Use the single templates to analyze basic feasibility. For example, a very aggressive channel in terms of length. Use this template for quick and easy checks because it only requires the models to be available for the single channel (s4p - 4 port

## Topology Workbench User Guide

### Working with Compliance Kits

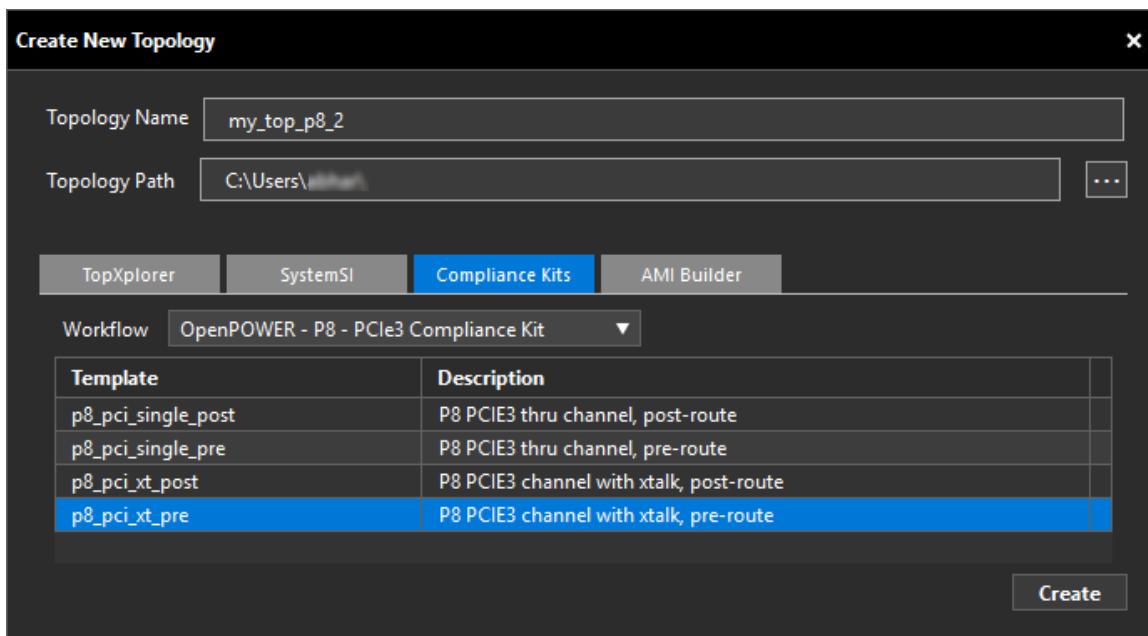
S-Parameter model for a differential pair). Also, it checks whether the channel insertion loss does not meet the budget.

**Note:** The single pre/post templates should never be used as a final test for compliance.

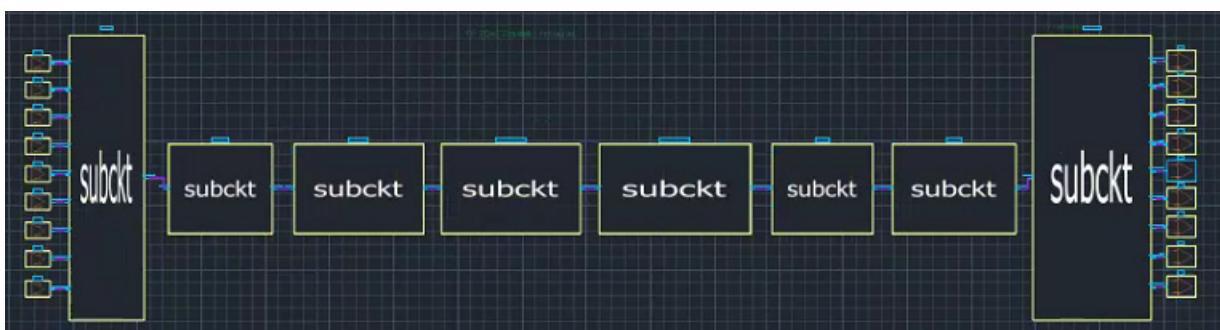
- Use *p8\_pci\_xt\_pre* to check for compliance.

This is a more inclusive template with eight crosstalk aggressors and one victim channel. You need models to be s36p (36 port S-Parameter model) for this template. As it might be difficult to generate s36p models for all channel components, ensure that eight aggressors are there to accurately represent the crosstalk noise in channel sections, such as, the wiring under the Hybrid-LGA socket connector or inside the package.

7. Select *p8\_pci\_xt\_pre* for this example and click *Create*.



The following topology is loaded in the related tab:



## Topology Workbench User Guide

### Working with Compliance Kits

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In this workspace, you can add and connect S-Parameter blocks as required. For this example, the signal path from the PCIe add-in card transmitter to the IBM POWER8 receiver will be simulated.

The passive channel is made up of the following S-Parameter models:

- PCIe add-in card
- PCIe SMT connector
- Connector PCB via
- 16 inches of open area trace
- 1 inch of under LGA wiring
- P8 module PCB via
- P8 module

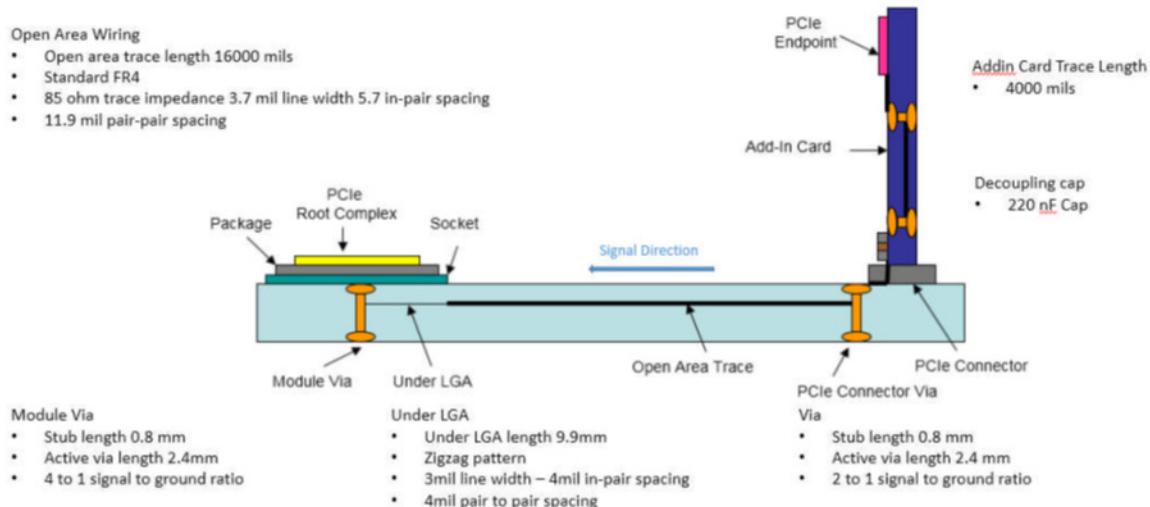
The PCIe add-in card model represents a typical PCIe Gen3 add-in card. It has 4 inches of open area trace, 4 vias, and the AC coupling cap along with the Rx package. It represents the part of that signal path that is from the C4 of the PCIe Endpoint to the card edge. The P8 module s-parameter is similar in that it is made up of a cascade of individual s-parameter models that represent the IBM package. It contains the LGA socket connector, traces inside the package (open area and escapes from die) as well as package RFP and micro- vias. All of the models with the exception of the P8 Module can be substituted with models the user has extracted or generated from their specific implementation of the channel.

The process of substituting Touchstone files in the template is explained in the [Using Touchstone Model Substitution](#) section.

# Topology Workbench User Guide

## Working with Compliance Kits

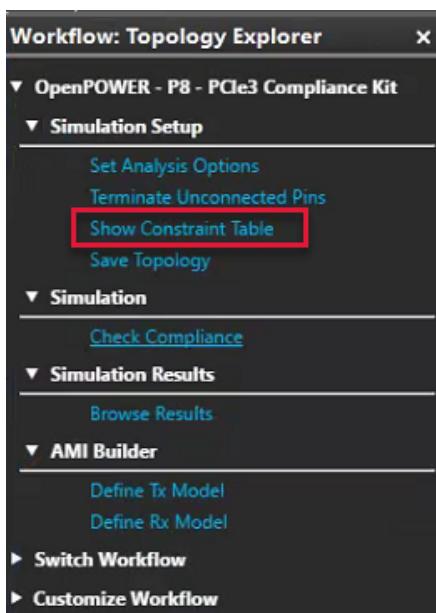
Channel properties for this reference channel are shown in the following figure.



## Running the Simulation

Once the test channel has been constructed, follow the steps given below to run the simulation:

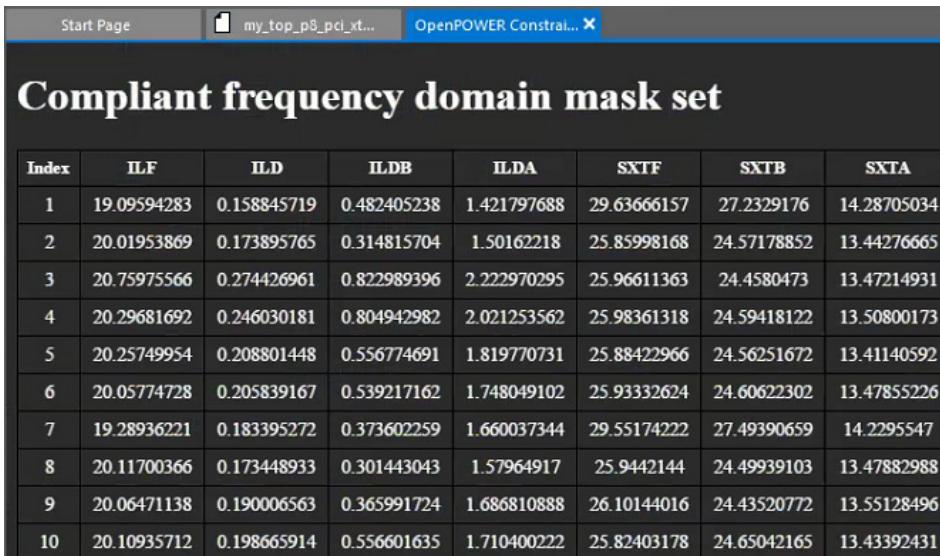
1. Choose *Simulation Setup – Show Constraint Table* in the Workflow Panel for *OpenPOWER - P8 - PCIe3 Compliance Kit*.



## Topology Workbench User Guide

### Working with Compliance Kits

The *Compliant frequency domain mask set* is displayed in a tabular format within a new tab as shown below:



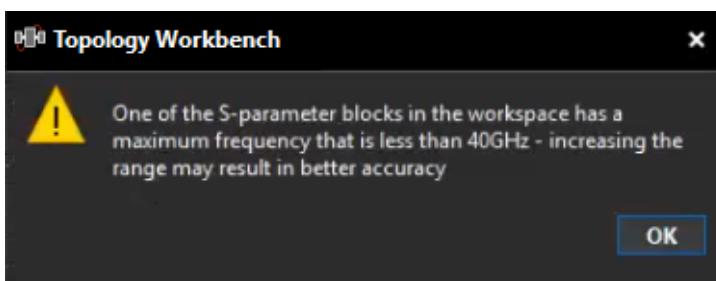
The screenshot shows a software window titled "Topology Workbench". In the top menu bar, there are three tabs: "Start Page", "my\_top\_p8\_pci\_xt...", and "OpenPOWER Constrai...". Below the tabs, the main content area has a title "Compliant frequency domain mask set". A table is displayed with the following columns: Index, ILF, ILD, ILDB, ILDA, SXIF, SXTB, and SXTA. The table contains 10 rows of data.

Index	ILF	ILD	ILDB	ILDA	SXIF	SXTB	SXTA
1	19.09594283	0.158845719	0.482405238	1.421797688	29.63666157	27.2329176	14.28705034
2	20.01953869	0.173895765	0.314815704	1.50162218	25.85998168	24.57178852	13.44276665
3	20.75975566	0.274426961	0.822989396	2.222970295	25.96611363	24.4580473	13.47214931
4	20.29681692	0.246030181	0.804942982	2.021253562	25.98361318	24.59418122	13.50800173
5	20.25749954	0.208801448	0.556774691	1.819770731	25.88422966	24.56251672	13.41140592
6	20.05774728	0.205839167	0.539217162	1.748049102	25.93332624	24.60622302	13.47855226
7	19.28936221	0.183395272	0.373602259	1.660037344	29.55174222	27.49390659	14.2295547
8	20.11700366	0.173448933	0.301443043	1.57964917	25.9442144	24.49939103	13.47882988
9	20.06471138	0.190006563	0.365991724	1.686810888	26.10144016	24.43520772	13.55128496
10	20.10935712	0.198665914	0.556601635	1.710400222	25.82403178	24.65042165	13.43392431

## 2. Choose *Simulation – Check Compliance* to run the simulation.

A warning appears that one of the S-Parameters has a maximum frequency that is less than 40 GHz. In this simulation method, it is recommended that all models have a high frequency point of 40 GHz. For this example, click *OK* to run the simulation.

It takes approximately 10 to 15 minutes for the simulation to complete for this full nine-channel template.



Once the simulation finishes, the results of the simulation are displayed as a compliance report in the SSIViewer window.

## Interpreting the Simulation Results

Shown below is an example *OpenPOWER Compliance Report* that is generated after you run the simulation:



## OpenPOWER Compliance Report

Generated by Cadence SSIViewer, 18.0.5.09101.179263 005  
16<sup>th</sup> of September 2019

### Useful Links:

- Cadence website: <http://www.cadence.com>
- OpenPOWER website: <http://openpowerfoundation.org>

### Definitions:

- Fundamental Frequency: 4GHz
- ILF: Insertion Loss at Fundamental Frequency
- ILD: Insertion Loss Deviation
- ILDB: Max Insertion Loss Deviation Below Fundamental Frequency
- ILDA: Max Insertion Loss Deviation Above Fundamental Frequency
- SXTF: Signal to Crosstalk at Fundamental Frequency
- SXTB: Signal to Crosstalk Deviation Measure Below Fundamental Frequency
- SXTA: Signal to Crosstalk Deviation Measure Above Fundamental Frequency
- Victim Tx/Rx: VCTM/Rx5

### Summary of Results

The channel simulated violates one or more OpenPOWER compliance requirements.

To check whether the test channel passed the compliance or not, select the *Only show passing indexes* check box. If an index shows up after selecting this box, the test channel passes the IBM Compliance test. If no passing cases show up, then the test channel is rendered non-compliant.

### Compliant frequency domain mask set

<input checked="" type="checkbox"/> Only show passing indexes								
	Index	ILF	ILD	ILDB	ILDA	SXTF	SXTB	SXTA
Pass/Fail	Measured Value	22.7448	0.355418	0.747748	2.14948	27.2863	27.4737	17.5867

In this example, the simulated channel did not pass the IBM PCIe Gen3 compliance test. The channel under test is a relatively long channel having main planar open area length of 16

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### Working with Compliance Kits

inches, 1 inch of under LGA pin area wire length, 4 inches of wiring on the PCIe add-in card, and the trace inside the package. This adds up to about 22 inches of total length. Therefore, it is expected that a channel of this nature would not pass due the large attenuation associated with the length.

### Compliant frequency domain mask set

Only show passing indexes

	Index	ILF	ILD	ILDB	ILDA	SXTF	SXTB	SXTA
Pass/Fail	Measured Value	22.7448	0.355418	0.747748	2.14948	27.2863	27.4737	17.5867
Fail	1	19.09594283	0.158845719	0.482405238	1.421797688	29.63666157	27.2329176	14.28705034
Fail	2	20.01953869	0.173895765	0.314815704	1.50162218	25.85998168	24.57178852	13.44276665
Fail	3	20.75975566	0.274426961	0.822989396	2.222970295	25.96611363	24.4580473	13.47214931
Fail	4	20.29681692	0.246030181	0.804942982	2.021253562	25.98361318	24.59418122	13.50800173
Fail	5	20.25749954	0.208801448	0.556774691	1.819770731	25.88422966	24.56251672	13.41140592
Fail	6	20.05774728	0.205839167	0.539217162	1.748049102	25.93332624	24.60622302	13.47855226
Fail	7	19.28936221	0.183395272	0.373602259	1.660037344	29.55174222	27.49390659	14.2295547
Fail	8	20.11700366	0.173448933	0.301443043	1.57964917	25.9442144	24.49939103	13.47882988
Fail	9	20.06471138	0.190006563	0.365991724	1.686810888	26.10144016	24.43520772	13.55128496
Fail	10	20.10935712	0.198665914	0.556601635	1.710400222	25.82403178	24.65042165	13.43392431
Fail	11	20.17070686	0.130636731	0.696891428	1.038710925	26.53720559	24.42322774	13.81536759
Fail	12	20.09427163	0.1266667824	0.567931564	0.992696542	26.40460458	24.54801804	13.83870101
Fail	13	20.31125543	0.139058785	0.484828118	1.352365607	26.50614363	24.4145876	13.76695734
Fail	14	19.21173313	0.133570591	0.832461993	1.100036541	30.39111977	27.01963241	14.53430172
Fail	15	20.10424473	0.136725874	0.587517099	1.193315624	26.44746023	24.43170394	13.74900541

To check where compliance failed, clear the *Only show passing indexes* box as shown. Each index in the table shown represents a boundary case. Each boundary case is described by values for each of the seven frequency domain parameters. Each of the 86 cases represents a point on the boundary of the solution space of compliant channels. Therefore, if the test channel is better than any one of these 86 boundary cases, the test channel lies within the solution space and is rendered compliant.

For the test channel to be considered better than a boundary case, all 7 frequency domain parameters of the test channel must be better in terms of signal integrity. This is represented by the green numbers, whereas the red numbers represent where the channel under test performed worse than the boundary case. For it to be a passing case, the entire row must be green.

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### Working with Compliance Kits

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Now, take a closer look at one of the boundary case comparisons, as shown below.

	Index	ILF	ILD	ILDB	ILDA	SXTF	SXTB	SXTA
Pass/Fail	Measured Value	22.7448	0.355418	0.747748	2.14948	27.2863	27.4737	17.5867
Fail	1	19.09594283	0.158845719	0.482405238	1.421797688	29.63666157	27.2329176	14.28705034

The first row has the measured values of the frequency domain parameters of the channel being tested. The channel considered in the example above has:

- Insertion Loss at Fundamental (ILF) frequency of 22.7448 dB
- Insertion Loss Deviation (ILD) measured of 0.355418
- Insertion Loss Deviation Below Fundamental (ILDB) frequency of 0.747748 dB
- Insertion Loss Deviation Above Fundamental (ILDA) frequency of 2.14948 dB
- Signal to Crosstalk at Fundamental (SXTF) frequency of 27.2863 dB
- Signal to Crosstalk Below Fundamental (SXTB) frequency of 27.4737 dB
- Signal to Crosstalk Above Fundamental (SXTA) frequency of 17.5867 dB

The second row represents the frequency domain parameters of a boundary channel. Here the ILF number is in red because the boundary channel has a lower number than the simulated test channel. Therefore, in terms of insertion loss the test channel is outside the solution space. This is the same for ILD, ILDB, and ILDA because more deviation degrades the signal quality. For SXTF the number is red because the test channel has less signal to crosstalk at the fundamental frequency.

This means that the signal to crosstalk ratio is higher for the test channel. The only field that the test channel performed better than this boundary case is at SXTA where it was higher and therefore green. However, this is not enough to render this channel compliant. It only would have been compliant if this entire row was green.

## Underlying Frequency Domain Parameters

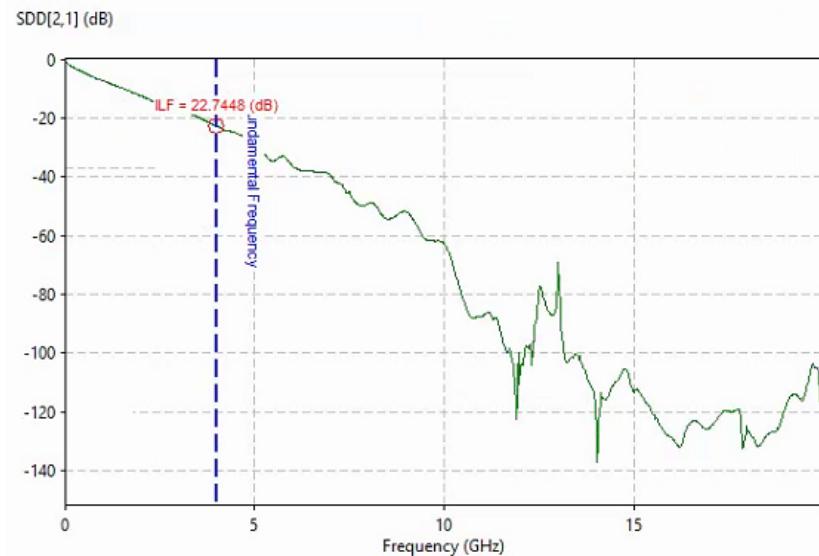
OpenPOWER compliance is based on the following frequency domain parameters:

- [Channel Differential Insertion Loss at Bus Fundamental Frequency](#)
- [Channel Insertion Loss Deviation Measure](#)
- [Channel Maximum Insertion Loss Deviation Below/Above Bus Fundamental Frequency](#)

- Channel Signal to Crosstalk Ratio at Bus Fundamental Frequency
- Channel Minimum Signal to Crosstalk Ratio Below and Above Bus Fundamental Frequency

### Channel Differential Insertion Loss at Bus Fundamental Frequency

The Insertion Loss at Bus Fundamental Frequency (ILF) parameter is calculated at 4 GHz (fundamental frequency of a PCIe-Gen3 bus) in dB. It describes mainly the attenuation of a signal traveling through the channel. Its value is affected in large by dielectric material loss properties, signal propagation distance, and channel impedance matching properties. When you click ILF from the column header in the compliance report, of this parameter is shown below:

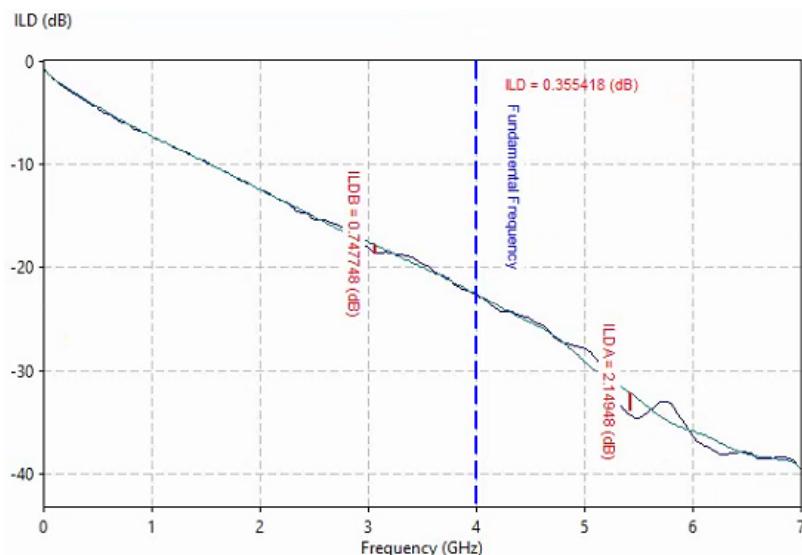


### Channel Insertion Loss Deviation Measure

The insertion loss deviation (ILD) measure is used to quantify the amount of reflections within a channel among other things. To quantify ILD, a fit of the insertion loss curve is generated between 0 Hz and a high frequency point defined at which the insertion loss is 40 dB or the highest frequency in the S-Parameter model, whichever comes first. The curve fitting of the insertion loss is done by moving average smoothing. The moving average smoothing procedure in this paper uses a window size of 51 discrete frequency points centered at the point under consideration. This window spans a 1.02GHz range with a 20MHz step S-Parameter model.

To obtain the fitted curve for insertion loss, different window sizes should be considered if a different S-Parameter frequency resolution is used.

Once the fitted line is obtained, the error between the original insertion loss curve and the fitted curve is found at each discrete frequency point in the S-Parameter model. The square of each discrete frequency point error is then found, after which the sum of all squares is calculated and divided by the total number of discrete frequency points considered. The resulting value is the insertion loss deviation measure.



### Channel Maximum Insertion Loss Deviation Below/Above Bus Fundamental Frequency

In addition to the ILD measure, the maximum insertion loss deviation below and above (ILDB/ILDA) the fundamental frequency are found by finding the maximum difference between the insertion loss curve and its fitted curve. This is because the ILD measure as defined earlier does not take into account where the deviation happens with respect to frequency.

Ripples in the insertion loss at lower frequencies have a greater effect on the channel signaling than at higher frequencies. This is due to the fact that channels typically have higher transmission amplitudes at the lower frequency. By considering the maximum deviation above and below the fundamental the ILD worst case frequency dependence is covered.

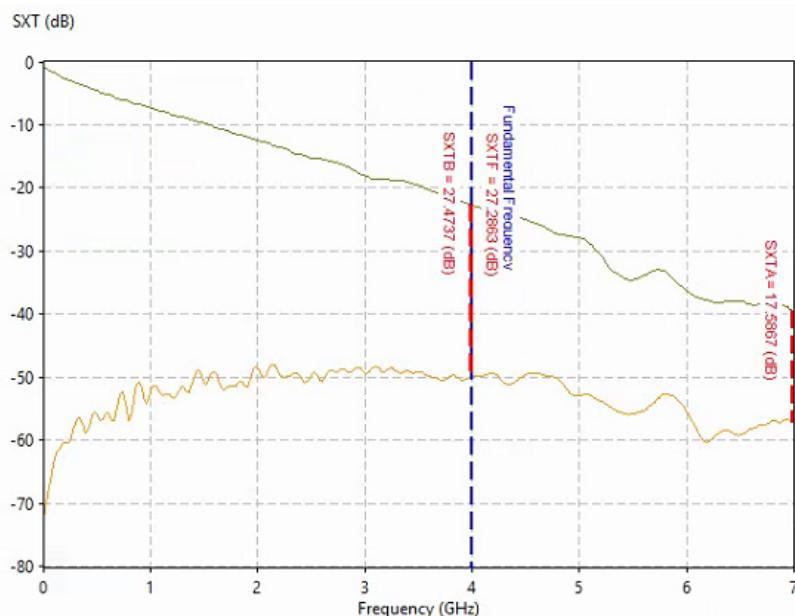
### Channel Signal to Crosstalk Ratio at Bus Fundamental Frequency

The Signal to Crosstalk Ratio at Bus Fundamental Frequency (SXTF) parameter is useful to get a measure of the amount crosstalk noise on the victim net in the channel under

## Topology Workbench User Guide

### Working with Compliance Kits

consideration at the fundamental frequency. This value is calculated by finding the difference between the insertion loss and the crosstalk aggression power sum at the fundamental frequency of the bus (4GHz). The crosstalk power sum from all the crosstalk aggressors is calculated using root sum square (RSS). The following figure shows an example signal to crosstalk ratio measure at fundamental frequency.



### Channel Minimum Signal to Crosstalk Ratio Below and Above Bus Fundamental Frequency

The channel minimum Signal to Crosstalk Ratio Below (SXTB) and Above (SXTA) bus fundamental frequency measures are considered. These are motivated by the fact that crosstalk aggression at fundamental frequency cannot solely represent the effect of crosstalk on a channel's signaling capacity. The full frequency band of the channel must be considered.

The SXTB and SXTA measures are the minimum signal to crosstalk ratio between:

- 0 Hz and bus fundamental frequency
- fundamental and the high frequency point

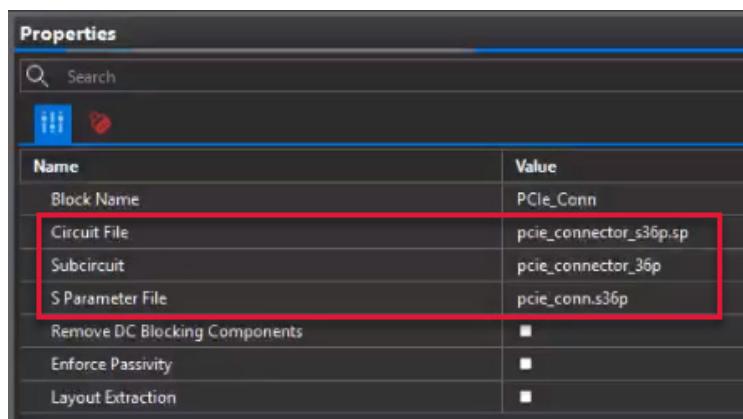
As described earlier the high frequency point is the frequency at which the insertion loss is 40 dB or the highest frequency in the S-parameter model, whichever point comes first. All discrete frequency points within these frequency ranges must be considered.

## Using Touchstone Model Substitution

You can interconnect different blocks with models associated to the block, defined by a SPICE subcircuit. The subcircuit is in standard SPICE format with the addition of a section for multi-pin or block-based connections that defines the connection port of the model to an easily identifiable name. This enables the connection between blocks to be fairly automatic if a standard naming convention is used in the multi-pin or block-based connections. For all the blocks in the OPENPOWER templates, the naming conventions are VCTMP and VCTMN for the victim channel ports, and AGR<X>P and AGR<X>N for the aggressor channels' ports where X is a number between 1 and 8 representing the 8 potential aggressor pairs. When you double-click the *PCIe\_Conn* block on the canvas, the corresponding properties are displayed in the *Properties* panel. It has the main that calls the SPICE circuit which in turn calls the Touchstone model for this interconnect.

### Identifying the Files to be Modified

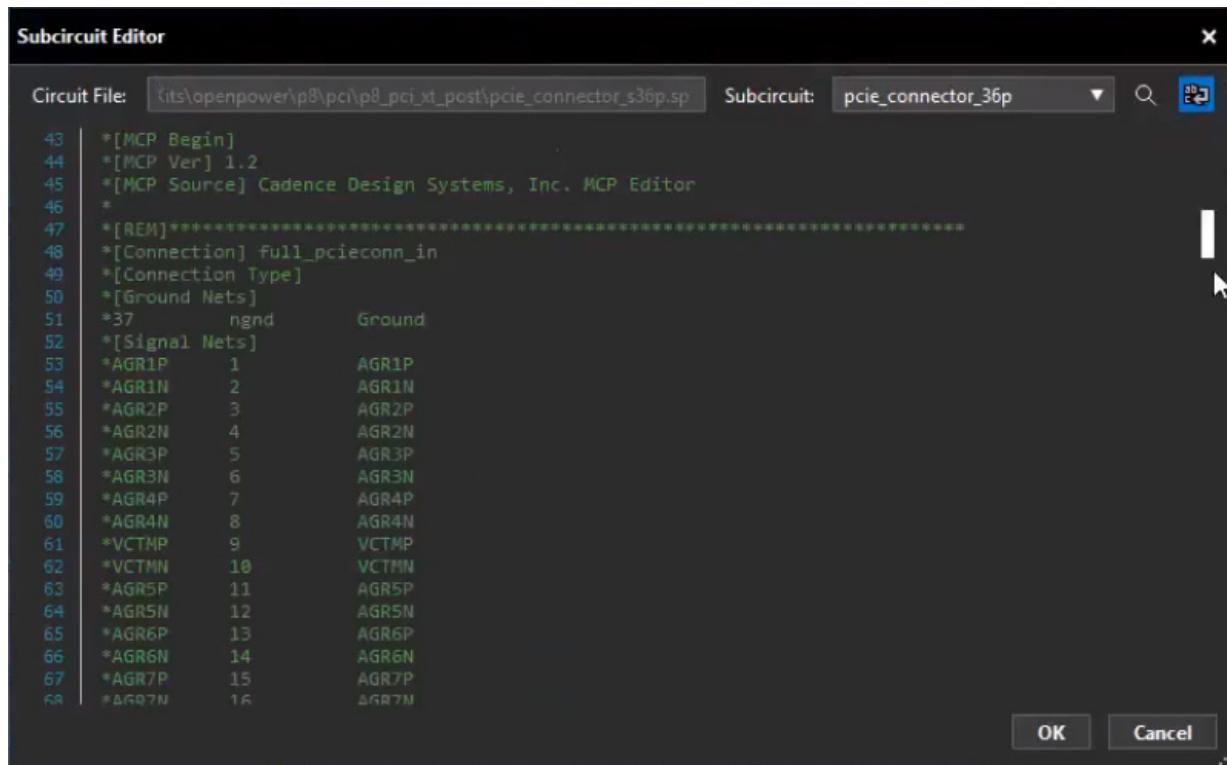
The *Circuit File* field in the *Properties* panel shows that main SPICE circuit named `2_PCIE_connector_s36p.sp` is assigned to the *PCIe\_Conn* block.



## Topology Workbench User Guide

### Working with Compliance Kits

When you click the *View Subcircuit* button, the contents of this SPICE circuit file are displayed in the *Subcircuit Editor*, which opens in editable mode.



Scroll down to the section after `[MCP End]`. where information such as following is captured to define the S-Parameter element for which the model file is output from BNP Touchstone.

...

`[MCP End]`

\*This concludes the multi-pin or block-based connections section

\* NOTE - This is the SystemSI generated sub-circuit definition for the S Parameter File:

\* 2\_pciconn36p\_S\_diff.s36p

\* Editing of sub-circuit definition is NOT recommended.

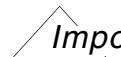
\*Define the S element, the Model file is output from BNP

```
.MODEL    Spara    S
+          TSTONEFILE = "./2_pciconn36p_S_diff.s36p"
```

The circuit file has the following:

- Defined port numbers

- Multi-pin or block-based connections section
- Call to the S-Parameter model

 *Important*

Even though the multi-pin or block-based connections section appears to be commented out, Topology Workbench interprets and uses this data.

The syntax of the lines in the multi-pin or block-based connections section is:

<PIN NAME> <CKT NODE> <NET NAME>

The S-Parameter model used here has all 18 input, that is, 8 pairs of nets for the aggressors, and one pair for the victim, nodes numbered from 1-18 and the corresponding outputs of the S-Parameter are numbered 19-36. Therefore, in this particular model the port connections are: 1<->19, 2<->20, .... 18<->36. In other models, such as *ViaField\_Conn*, the connections might be more traditional too, such as, 1<->2, 3<->4, and so on.

Double-click the connection between the *pciecard* and *PCIe\_Conn* blocks on the canvas to open the Connection Definitions panel. The 36 connections that are made between these two blocks can be seen.

The Connection definition tab shows the following information:

The panel shows the port information for each of the blocks being connected with a line to indicate which ports are being tied together. In this case, it can be seen that the *Net VCTMP* in the *PCIE\_Conn* block is tied to *Net VCTMP* in the *pciecard* block. The name in the *Conn Port* field is the name from the multi-pin or block-based connections header section of the SPICE circuit. Various connections can be defined for different connection scenarios. An example of this would be where only one of the pairs from the full 9 pair model is to be selected for a simulation.

When you use a common naming convention for the *Pin Names* when connecting blocks together, Topology Workbench automatically connects by *PinNames*. This simplifies the process of making complex connections.

The next section shows how to use a Touchstone file.

## Using the Touchstone File

Assume you created a model, *my\_pcie\_conn.s36p*, that represents the open area wiring for the P8 card implementation. Also, assume that the S-Parameter file follows the port order 1<->2, 3<->4, and so on.

## Topology Workbench User Guide

### Working with Compliance Kits

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In the folder where the template resides, multiple SPICE .sp files and Touchstone files similar to the following will be present:

- The two *template\_36p* files are for the cases where the ports are in different orders.
- The file *template\_36p\_portorder\_1to2.sp* is for the case where all the port inputs are odd numbers and outputs are even numbers, that is 1<->2, 3,>4, and so on.
- *Template\_36p\_portorder\_1to19.sp* is for the models where all the inputs are ports 1-18 and outputs are 19-36, that is 1<->19, 2<->20, and so on.

Now, perform the following steps:

1. Copy the template that represents the port order that the Touchstone model has defined and rename it to another name.

For example, copy the *pcie\_conn.s36p* and *pcie\_connector\_s36p.sp* files from the *OpenPOWER\_models > PCIe3\_Sparams* directory and paste them in your current workspace directory. Then, rename the files to *my\_pcie\_conn.s36p* and *my\_pcie\_connector\_s36p.sp*, respectively.

2. Edit the renamed file, *my\_pcie\_connector\_s36p.sp*. On the first line, change:

.SUBCKT Generic\_portorder\_1to2\_36p

to something meaningful such as:

.SUBCKT extracted\_interconn\_36p

3. Scroll to the bottom of the file and replace the string <modelname\_here> with the name of the *s36p* file. In this example, that would be *my\_pcie\_conn.s36p*.

### Example Touchstone File Before Editing

```
* NOTE - This is a SystemSI generated sub-circuit definition for an S-Parameter
file:
* <modelname_here>.s36p
* Editing of sub-circuit definition is NOT recommended.
```

\*Define the S element, the Model file is output from BNP

```
.MODEL Spara S
+ TSTONETFILE = "./<modelname_here>.s36p"
```

### Example Touchstone File After Editing

```
* NOTE - This is a SystemSI generated sub-circuit definition for an S-Parameter
File:
```

## Topology Workbench User Guide

### Working with Compliance Kits

- \* **my\_PCIE\_conn.s36p <<< This change is not mandatory.**
- \* Editing of sub-circuit definition is NOT recommended.

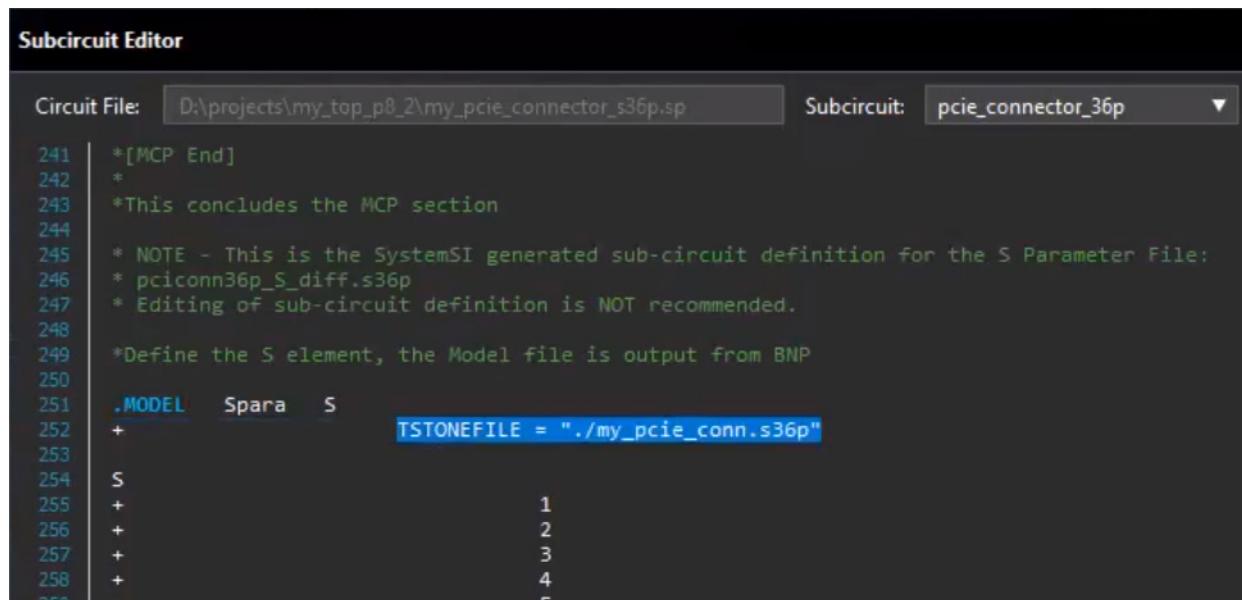
\*Define the S element, the Model file is output from BNP

```
.MODEL Spara S
+ TSTONEFILE = "./my_PCIE_conn.s36p" <<< This is required
```

**Note:** If the model resides in a different path, change the full path as required.

The newly created model can now be incorporated in Topology Workbench. For this, in the *Properties* panel, reset the path in the *Circuit File* field to access my\_PCIE\_connector\_s36p.sp. The *S-Parameter File* field is updated automatically to show the associated my\_PCIE\_conn.s36p.

When you click the *View Subcircuit* button and review the circuit file in the *Subcircuit Editor*, the changes you made to the S-Parameter file can be seen as shown below:



The screenshot shows the Subcircuit Editor interface. At the top, it displays the 'Circuit File' as 'D:\projects\my\_top\_p8\_2\my\_PCIE\_connector\_s36p.sp' and the 'Subcircuit' as 'pcie\_connector\_36p'. The main area contains the following S-parameter file code:

```
241 *[MCP End]
242 *
243 *This concludes the MCP section
244
245 * NOTE - This is the SystemSI generated sub-circuit definition for the S Parameter File:
246 * pciconn36p_S_diff.s36p
247 * Editing of sub-circuit definition is NOT recommended.
248
249 *Define the S element, the Model file is output from BNP
250
251 .MODEL Spara S
252 + TSTONEFILE = "./my_PCIE_conn.s36p"
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## **Topology Workbench User Guide**

### Working with Compliance Kits

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## **Using the AMI Builder**

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The AMI Builder feature is available in the Serial Link Analysis (SLA) and Parallel Bus Analysis (PBA) workflows.

AMI Builder is used to generate algorithmic (AMI) models to represent equalization functionality such as feed-forward equalization (FFE) and decision feedback equalization (DFE) for the SystemSI workflows in Topology Workbench.

You might need to generate AMI models in scenarios such as following:

- A particular IP needs an AMI model for simulation.
- A specification requires an AMI model.
- A 'what if' analysis needs to be performed to analyze whether a system would work with the given components.
- The existing AMI models need to be verified.

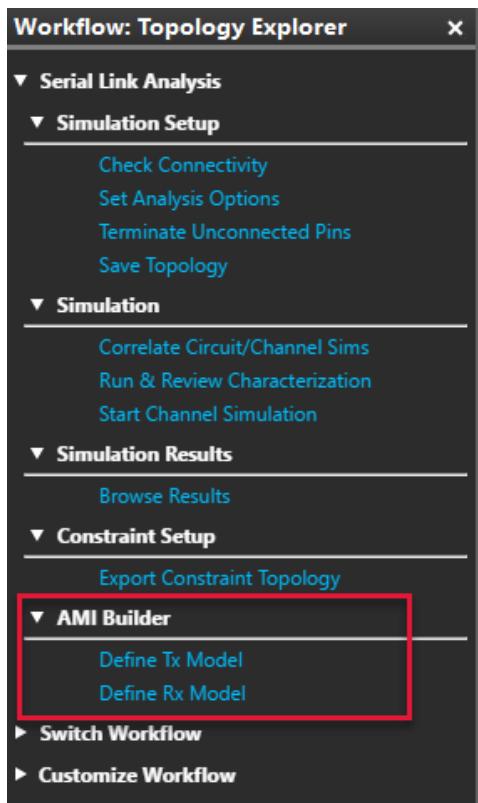
### ***Related Topics***

- [Overview of AMI Builder](#)
- [Adding Standalone AMI Models](#)
- [Adding Models with the AMI Builder Wizard](#)
- [Editing an AMI Model](#)
- [Adding Custom Blocks to Tx and Rx AMI Models](#)
- [Supported Blocks for an AMI Model](#)

## Overview of AMI Builder

Depending on whether you prefer to work in the main AMI Builder GUI, or be prompted for choices, you can pick one of the following ways to create AMI models.

- To create a standalone AMI model, use the SLA or PBA workflow. Alternatively, you can start a dedicated AMI Builder workflow as explained in the [Adding Standalone AMI Models](#) section.



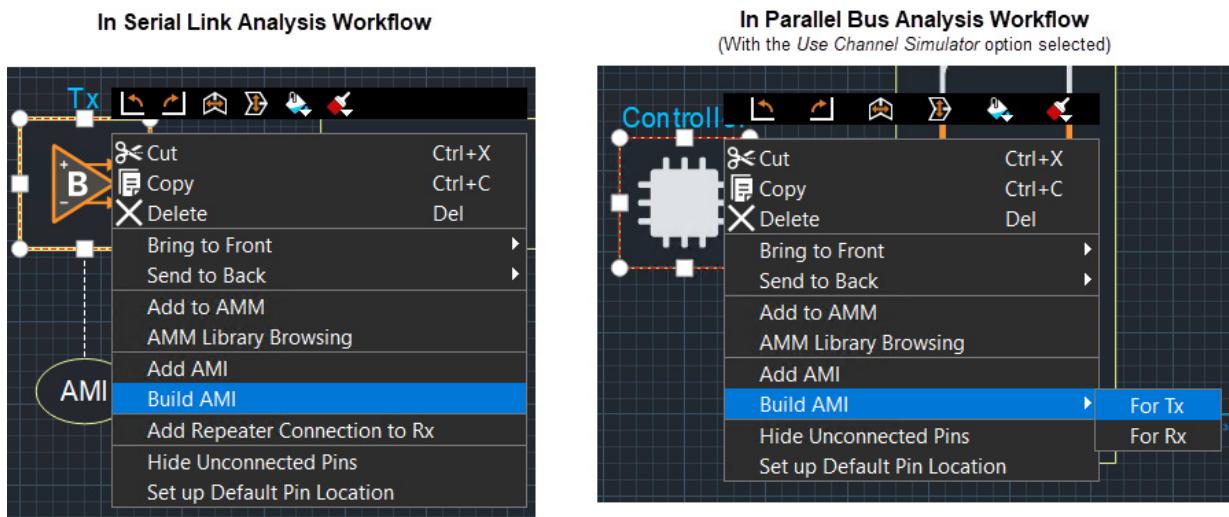
This model is not attached to an Tx or Rx component, but is built prior to simulation and stored as a part of a library, or to be shared with other users.

The [Adding Standalone AMI Models](#) section walks you through the steps for this procedure.

## Topology Workbench User Guide

### Using the AMI Builder

- To create an AMI model associated with Tx/Rx Analog model (IBIS or non-IBIS), right-click the Tx/Rx (Controller/Memory) component and choose *Build AMI* as shown below.



The *AMI Builder Wizard* opens. The [Adding Models with the AMI Builder Wizard](#) topic walks you through the steps for this procedure. You are prompted for answers about the technology for which you are creating the AMI model.

In the PBA workflow, the *Build AMI* menu also provides the *For Tx* and *For Rx* submenu options to build AMI models for the Controller and Memory blocks.

## Licensing Information

AMI Builder is available with all SLA and PBA licenses, such as:

- SIGR506 - Feature Key: SystemSI\_Serial\_IIC
- SIGR556 - Feature Key: SystemSI\_Parallel\_IIC
- SIGR915 – Feature Key: AllegroSigrity\_Pwr\_Awr\_SI\_Opt
- SIGR935 – Feature Key: AllegroSigrity\_Serial\_Link\_Opt
- SIGR575 – Feature Key: SystemSI\_Suite
- SIGR952 – Feature Key: Advanced\_IBIS\_Modeling

### **Licensed AMI Modeling**

With these licenses, IP suppliers can develop, correlate, and distribute AMI models created in Topology Workbench. **However**, these AMI models are licensed to run **only with Topology Workbench**.

### **Unlicensed AMI Modeling**

To build unlicensed AMI models that can be distributed without constraints, and run directly in any IBIS-compliant simulator, use the following Topology Workbench licenses:

- SIGR580 – Feature Key: SystemSI Advanced AMI Builder
- SIGR952 – Feature Key: Advanced\_IBIS\_Modeling
- SIGR990 – Feature Key: Sigrity Enterprise

## **Model Compilation Requirements**

An AMI model must be compiled using a platform-dependent-compiler to create an AMI model file (.d11) and a parameter file (.ami). The files produced on the Linux and Windows platforms are different because they are platform dependent. The process and compiler used are also different. However, the functions of the generated files are the same.

When working on the Linux platform, the AMI models can be compiled using the GNU Compiler Collection (gcc), which is the free compiler shipped with the Linux installation. However, ensure that the gcc version is 6.3 or higher.

On the Windows platform, you can compile the AMI models using one of the following compilers:

- Windows GCC package (*Recommended. It installs automatically when the Use Windows GCC option is selected in the Options dialog box. It removes the installation effort and any external dependency on the Microsoft products.*)
- Microsoft Visual Studio Express 2015 for Windows 10 (a *free version*)
- Microsoft Visual Studio Professional 2015

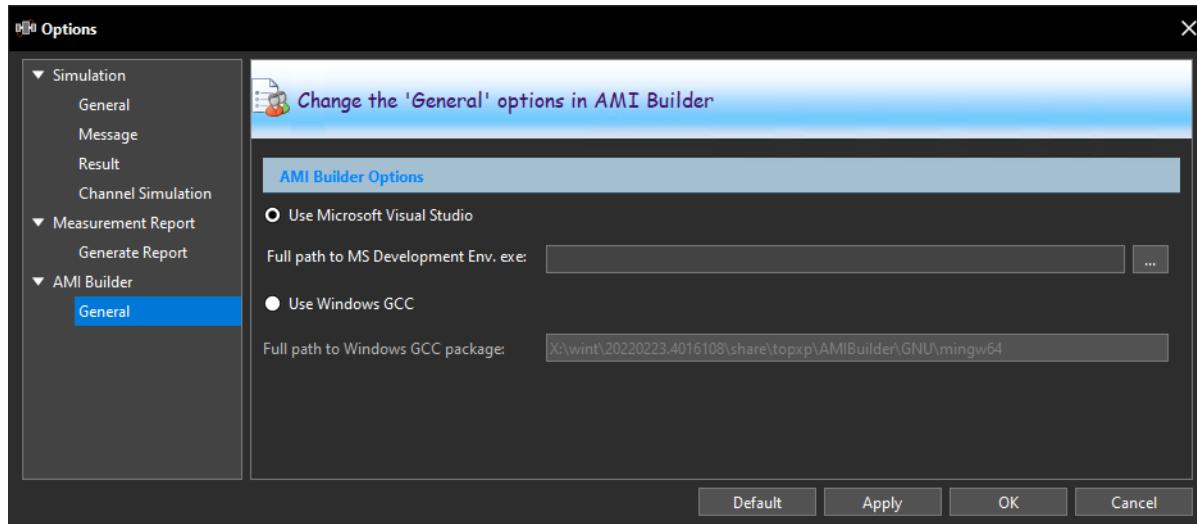
To set the preferred compiler for the Windows platform:

1. Choose *Tools – Options*. The *Options* dialog box opens.
2. Click *AMI Builder – General*.

## Topology Workbench User Guide

### Using the AMI Builder

3. Set the full path to the Visual Studio executable or Windows GCC package in the *AMI Builder Options* section.



**Note:** When you select *Use Windows GCC* for the first time and click *OK* or *Apply* in the *Options* dialog box, the Windows GCC package is installed automatically using the `SIGRITY_EDA_DIR` environment variable's value to find the `.7z` file and unzip it in the `\share\topxp\AMIBuilder\GNU` folder. Therefore, ensure that a Sigrity 2021 or later release is installed. If the Sigrity version that you have does not contain the `.7z` file, an error message is displayed.

## Understanding the AMI Model Blocks

AMI models for the Tx and Rx blocks are different.

- Tx AMI model has the following blocks:
  - Gain
  - FFE
- Rx AMI model uses:
  - AGC (Analog Gain Control)
  - CTE (Continuous Time Eq)
  - FFE block
  - DFE/CDR block (mandatory)

Both Tx and Rx also have a Custom block that is used to integrate custom code to the available modules. See the [Adding Custom Blocks to Tx and Rx AMI Models](#) section for details.

The details of the blocks are explained in the [Supported Blocks for an AMI Model](#) section.

## Adding Standalone AMI Models

To create a model using the AMI Builder GUI:

1. Create a topology project for AMI Builder workflow.

For steps, refer to the [Creating a Topology Project from Scratch](#) section or the [Opening an Existing Topology Project](#) section.

When you create a new topology project, the *AMI Builder* tab provides a list of the following default standalone AMI Builder workflow-specific templates:

Template	Description
<i>Tx AMI Model</i>	Defines a Tx model.
<i>Rx AMI Model</i>	Defines a Rx model.

Depending on the type of model you need to create, select the required default template. The Topology Workbench window is refreshed as following:

- ❑ A tab with the given *Topology Name* opens next to the [Start Page](#).
- ❑ A blank [Layout Canvas](#) is displayed.
- ❑ The [Workflow Panel](#) opens with a list of tasks you need to define the required AMI model.
- ❑ The [Floating Toolbar](#) opens with a list of various types of useful blocks.

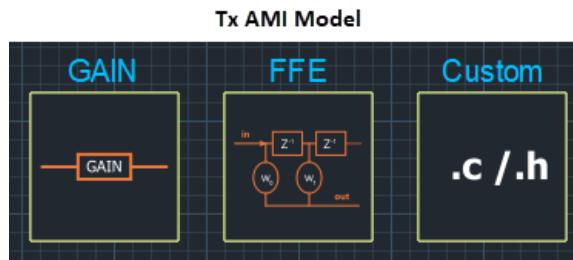
**Note:** For the Rx AMI model, the DFE/CDR block is placed on the canvas by default as all Rx AMI model contains a DFE/CDR.

2. Click *Define Tx Model* from the Workflow panel. This step is not needed if you opted to create a Tx AMI model template in the *Create New Topology* dialog box because a tab titled Rx AMI Builder will open automatically. You can then directly move to [step 3](#) onward.
3. Click the available Tx AMI Builder blocks displayed in the floating toolbar and place them on the canvas.

## Topology Workbench User Guide

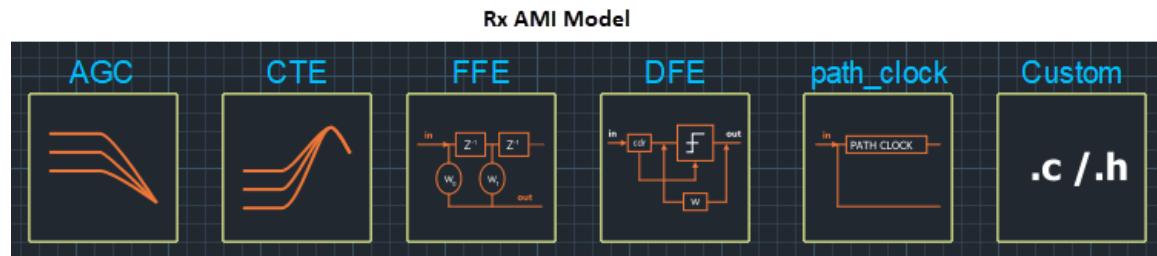
### Using the AMI Builder

There is no restriction on the number of blocks that can be placed on the canvas. The order of the block placement, however, does have an impact on how the AMI model behaves. As such the simulation will vary based on the order of block placement.



4. Click *Define Rx Model* from the Workflow panel. This step is not needed if you opted to create a Rx AMI model template in the *Create New Topology* dialog box because a tab titled Rx AMI Builder will open automatically. You need to then perform step 2 and step 3 after step 5.
5. Click the available Rx AMI Builder blocks displayed in the floating toolbar and place them on the canvas.

There is no restriction on the number of blocks that can be placed on the canvas. The order of the block placement, however, does have an impact on how the AMI model behaves. As such the simulation will vary based on the order of block placement.



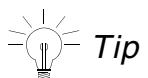
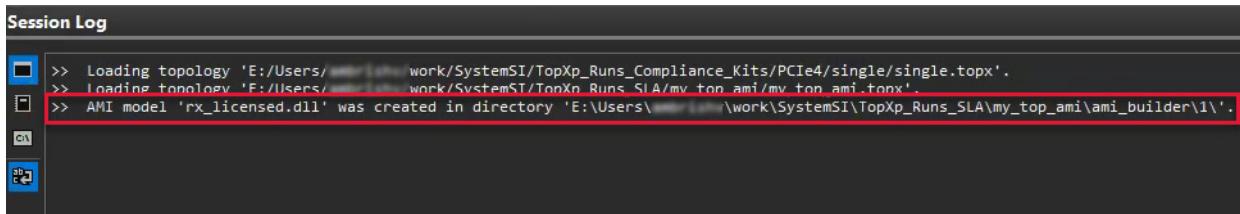
**Note:** The differences between the Tx AMI Builder and Rx AMI Builder are the available blocks that build the AMI models.

6. Click *Build AMI Model* from the *Workflow* panel or click the *play* button from the toolbar. A dialog box is displayed for you to browse the folder to save the result files.
7. Specify where to save the files and click *Select Folder*.

## Topology Workbench User Guide

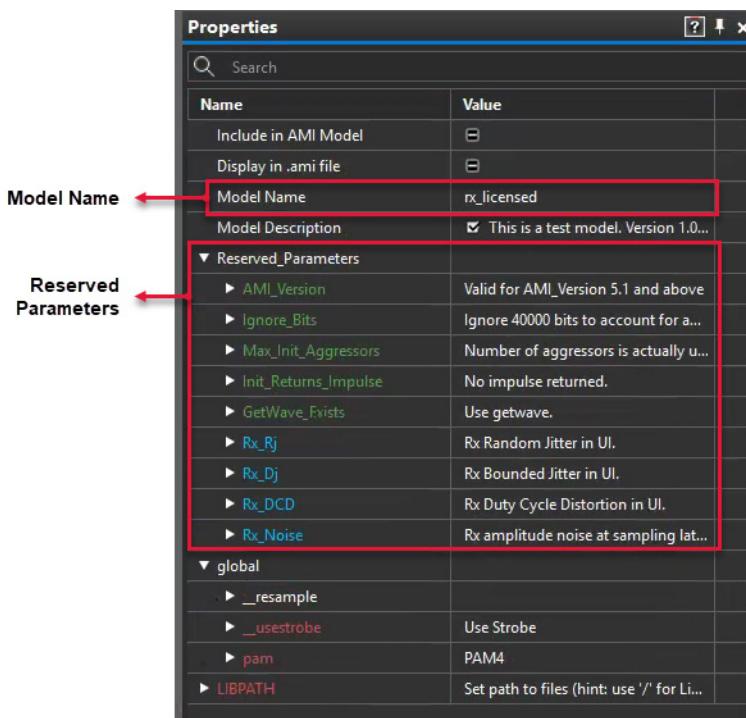
### Using the AMI Builder

This generates the required files, compiles the executable model, and saves the files. A message will be displayed in the *Output* tab of the *Session Log* panel notifying you that the model has been created and the path where it is saved.



*Tip* Choose *View – Session Log* from the menu bar to open the *Session Log* panel.

8. Choose *View – Edit Properties* from the menu bar to open the properties of the entire AMI model that you just generated.



In this window, you can:

- Edit the name of the AMI model.

## Topology Workbench User Guide

### Using the AMI Builder

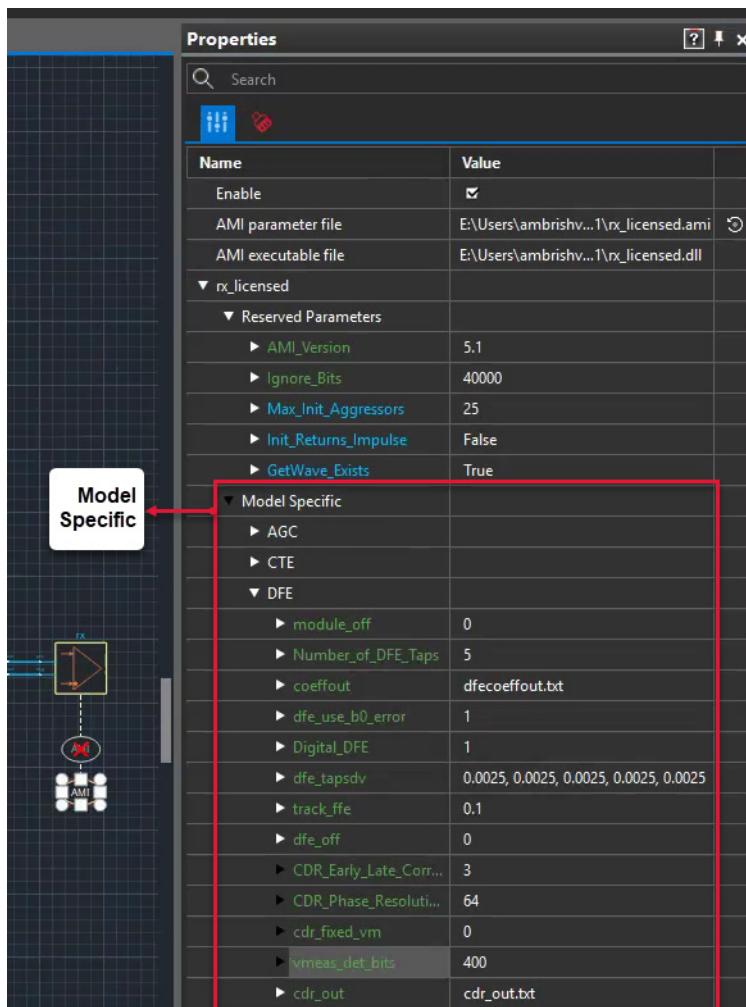
By default, the name of the AMI model is the same as the Rx or Tx block name. The model name can be changed by editing the field next to *Model Name* in the *Edit Properties* panel for the AMI Model.

- Access and edit the Reserved Parameters for the AMI model.

For this, click the *Reserved Parameter* schema in the *Edit Properties* panel.

- Access and edit all the Model Specific parameters in one window.

If the *Edit Properties* panel is already open, click each individual block in the AMI model and view their *Model Specific* parameters. Otherwise, you will need to double-click a block to open the *Edit Properties* panel with a list of corresponding parameter information.



## Topology Workbench User Guide

### Using the AMI Builder

Based on the color of each parameter displayed in the *Edit Properties* panel, you can understand whether it is only included in the AMI model or will also be displayed in the generated results. Here is the color legend:

- Green indicates that the parameter is included in the AMI model and displayed in the generated results.
- Blue indicates that the parameter is included in the AMI model, but not displayed in the generated results.
- Red indicates that the parameter is not included in the AMI model.

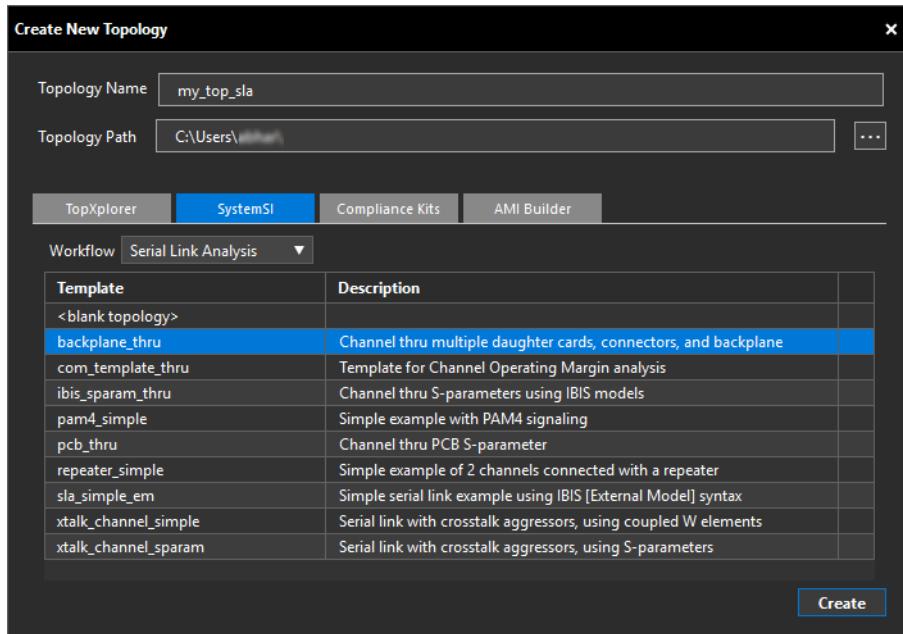
The [Editing an AMI Model](#) section has an example.

## Adding Models with the AMI Builder Wizard

This section describes how to use the AMI Builder wizard to create a receiver (Rx) equalization AMI model. Using the Rx Wizard, you can create an AMI model, make edits, and use it in a channel simulation.

### Opening a Workspace

1. Create a new Serial Link Analysis topology based on the *backplane\_thru* template.



# Topology Workbench User Guide

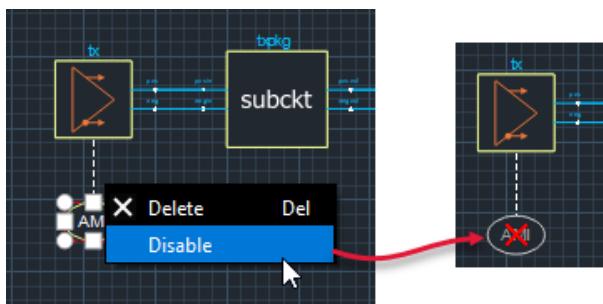
## Using the AMI Builder

The design workspace opens.

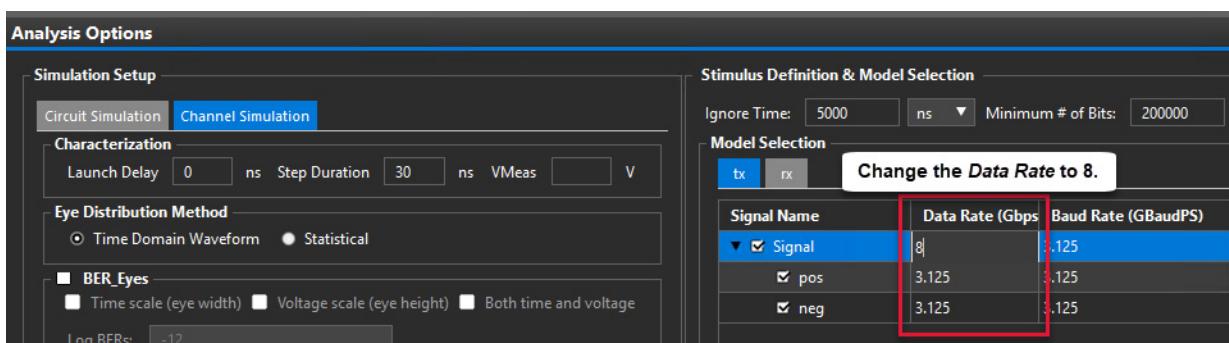


This chapter focuses on the Rx AMI model. Therefore, disable the Tx AMI model.

2. Right-click the Tx AMI bubble and choose *Disable*.



3. Click *Set Analysis Options* in the Workflow panel. The *Analysis Options* panel opens.
4. Open the *Tx* tab in the *Model Selection* section.
5. Set the *Data Rate* to 8 Gbps.

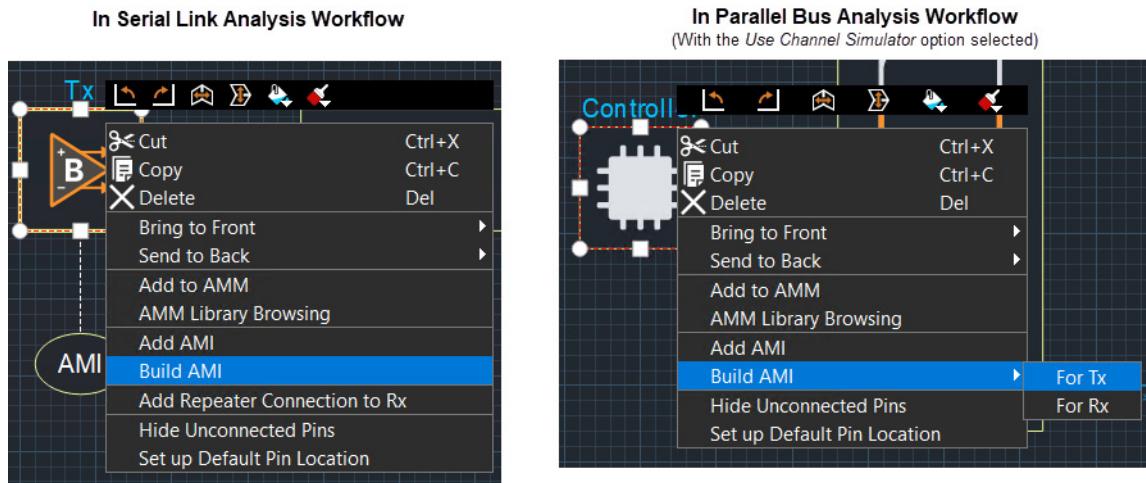


# Topology Workbench User Guide

## Using the AMI Builder

### Launching AMI Builder

1. Right-click an Rx block and choose *Build AMI* from the displayed shortcut menu.

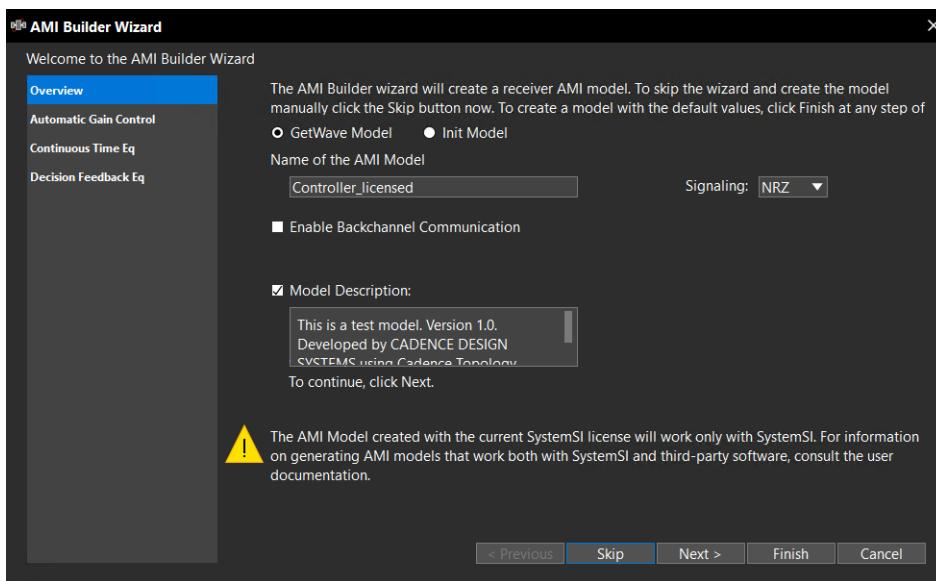


**Note:** In the PBA workflow, select *Build AMI – For Rx*.

The AMI Builder wizard opens for building a receiver (Rx) AMI model.

You will define the Automatic Gain Control (AGC), Continuous Time Equalization (CTE), and Decision Feedback Equalization (DFE) functionality. See [Rx AMI Model Blocks](#) for details of blocks.

2. Select *GetWave Model* or *Init Model* to specify the type of the AMI model.



## Topology Workbench User Guide

### Using the AMI Builder

**Note:** To use the AMI Builder GUI directly, click *Skip*.

When you create an Init model, there will be no GetWave functionality in the model and you will not be able to enable it using the Reserved Parameters, which can be set in the .

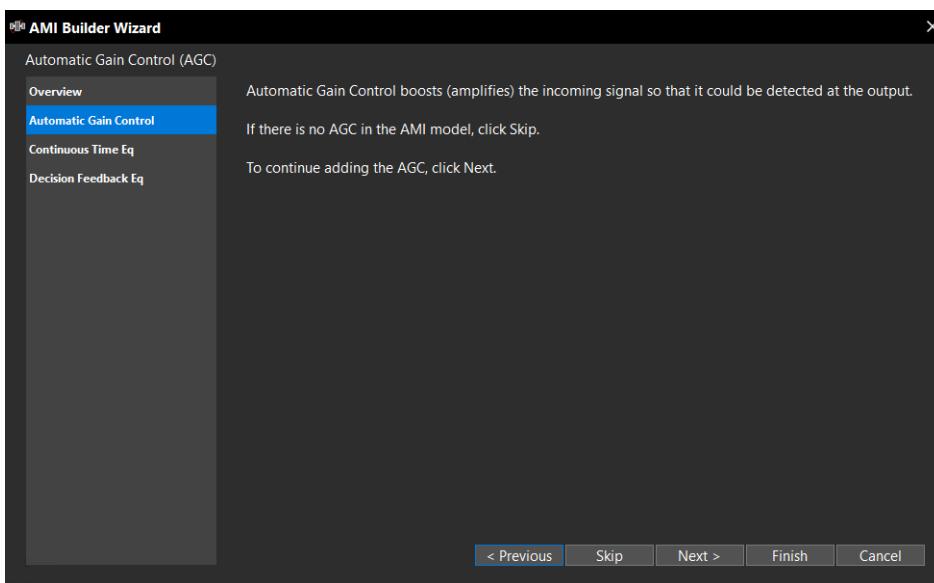
When you create a GetWave model, the Impulse modification capability is not allowed and User may not simply change the Reserved Parameter to enable Init/Statistical functionality.

3. Specify a name for the model.

4. Select the type of *Signaling* you want. By default, it is set to NRZ. You can change the selection to PAM3 or PAM4.
5. Select the *Enable Backchannel Communication* check box if you need the basic functionality for a backchannel-capable model. By default, this check box is not selected.

**Note:** The backchannel communication works only when the transmitter (Tx) has a backchannel-capable model that is compliant with the protocol used by the receiver AMI model you are creating.

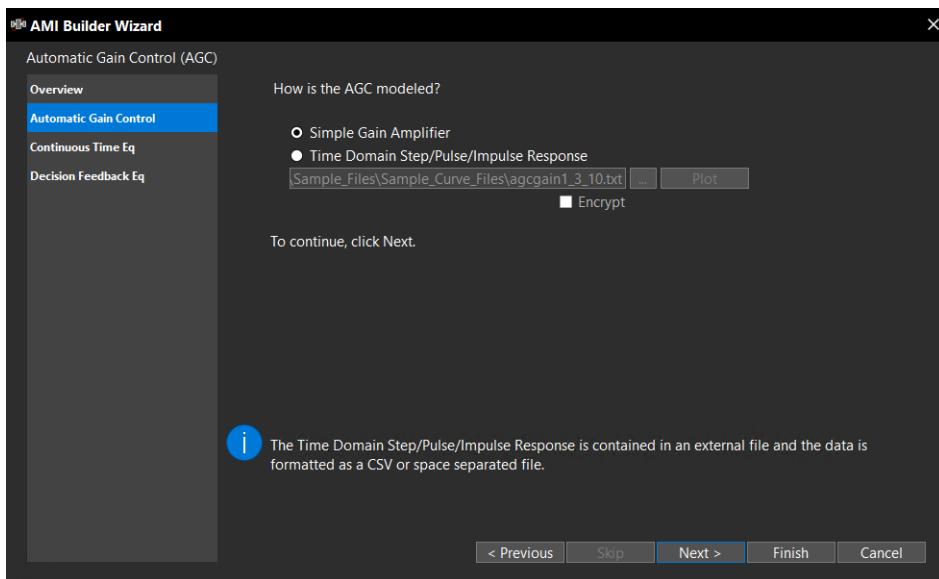
6. Click *Next* to move on to the AGC section.



## Topology Workbench User Guide

### Using the AMI Builder

7. Click *Next* to include AGC functionality in the model.



These options enable you to adapt the AGC module based on the SNR of the entire system. The AGC module can be modeled as:

- Simple Gain Amplifier* if the AGC is a simple multiplier.
- Time Domain Step/Pulse/ Impulse Response* text file if the AGC is modeled as a time domain filter. When this option is selected, the *Encrypt* check box is enabled.

Select the *Encrypt* check box to protect the IP information by encrypting the data files that are referred from the AMI model. This creates .enc files, which are encrypted versions of the csv/data files. When the *Encrypt* check box is selected, you must modify the library path to point to the local or data directory where the .enc files exist. The models decrypt the .enc files at run time irrespective of the tool these models are being used in.

**Note:** You can encrypt only data files that use the `csvfilt -file` parameters. Topology Workbench supports normal file encodings like ANSI, UTF8. For encodings that add additional characters into the text stream of the file are currently not recognized, such as, UTF8-BOM that adds 0xEF,0xBB,0xBF at the beginning.

Sample files are available at the location:

`<INSTALL_DIR>\share\topxp\AMIBuilder\Sample_Files\Sample_Curve_Files`

For example, you can:

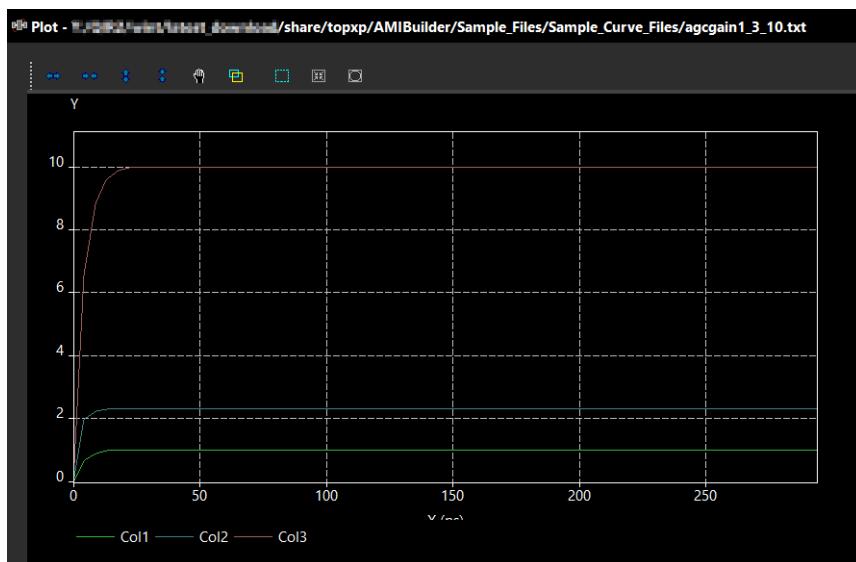
- a. Select the *Time Domain Step/Pulse/Impulse Response* option.

## Topology Workbench User Guide

### Using the AMI Builder

b. Click the browse button (...) and select a file.

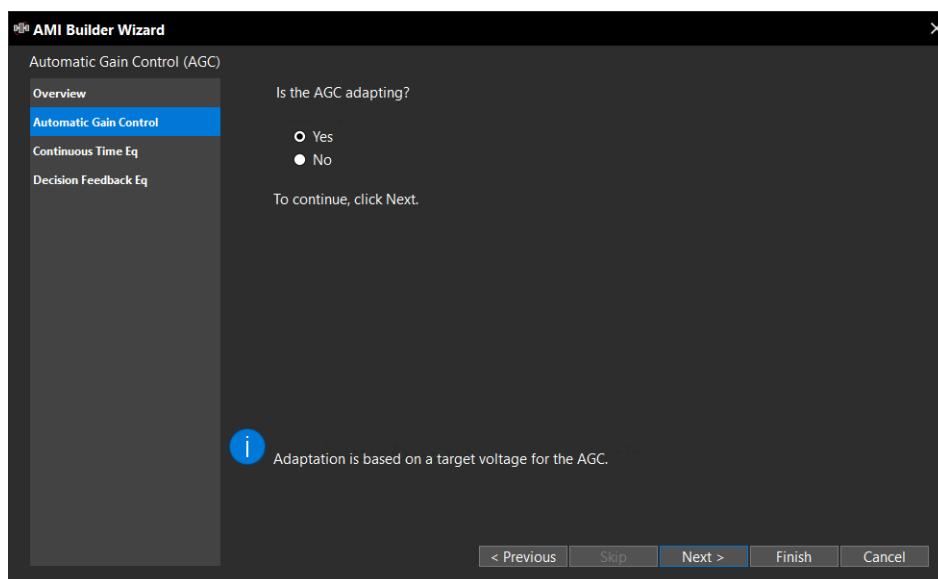
c. Click *Plot*.



In this example, AGC time domain filter contains three voltage columns (Y Axis) and one time column (X Axis). The voltage columns model the AGC as step responses.

The [Using CSV Input files with AMI Builder Wizard](#) section lists the requirements the file needs to fulfill.

8. Select *Simple Gain Amplifier* and click *Next*.

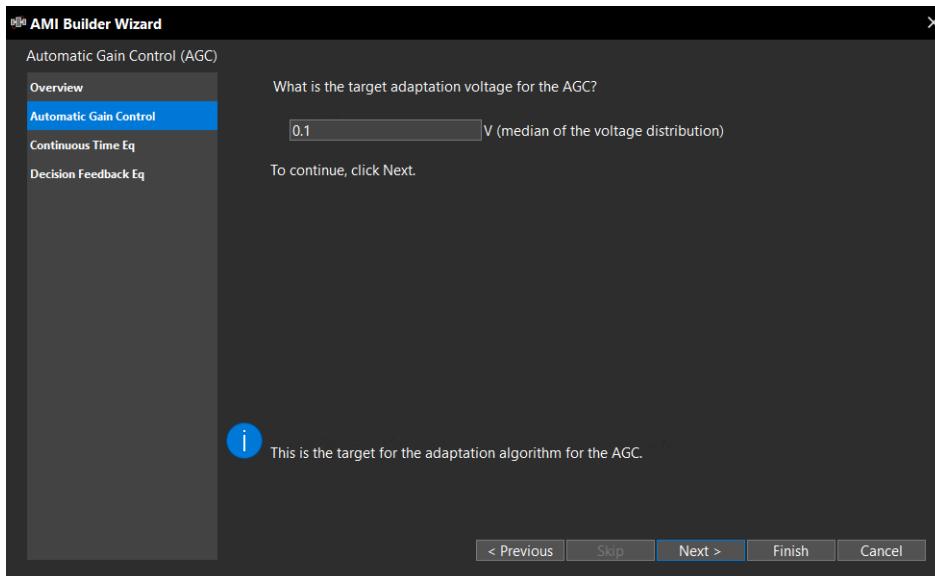


# Topology Workbench User Guide

## Using the AMI Builder

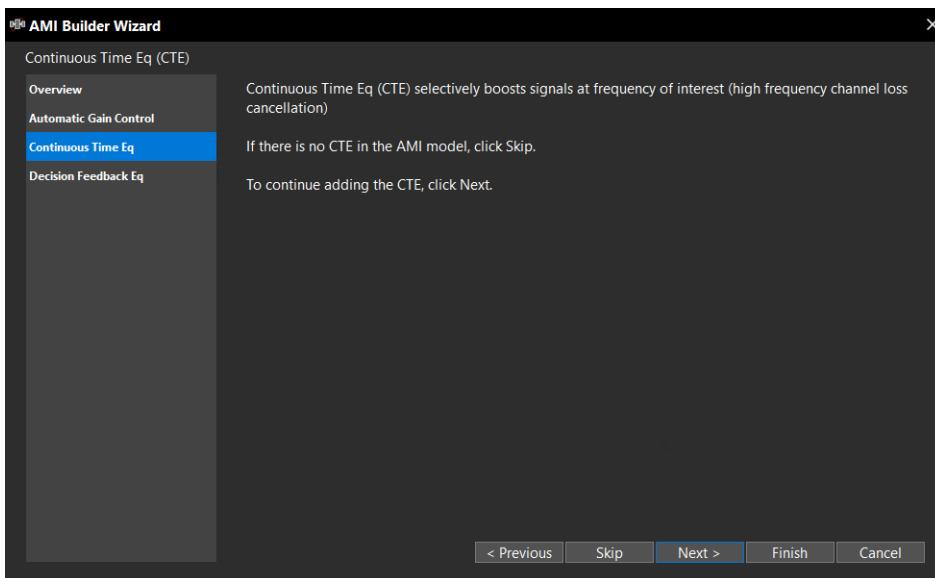
For this example, assume the AGC is adaptive.

9. Click *Yes* and then click *Next*.



Here, you define the target adaptation voltage for the AGC. Leave this as 100mV for this example.

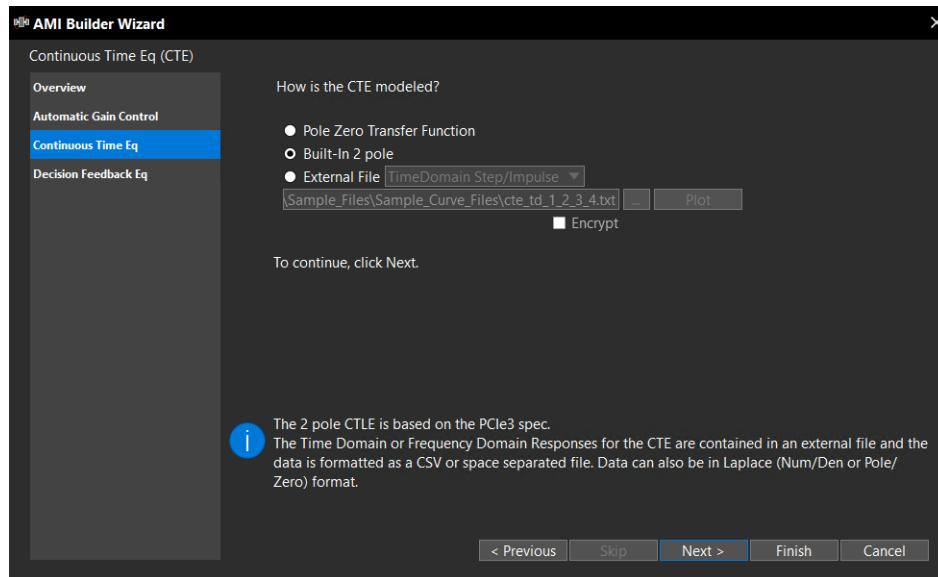
10. Click *Next* to go to the CTE module.



## Topology Workbench User Guide

### Using the AMI Builder

11. Click *Next* to include CTE functionality in the model, which is essentially a high-pass filter.



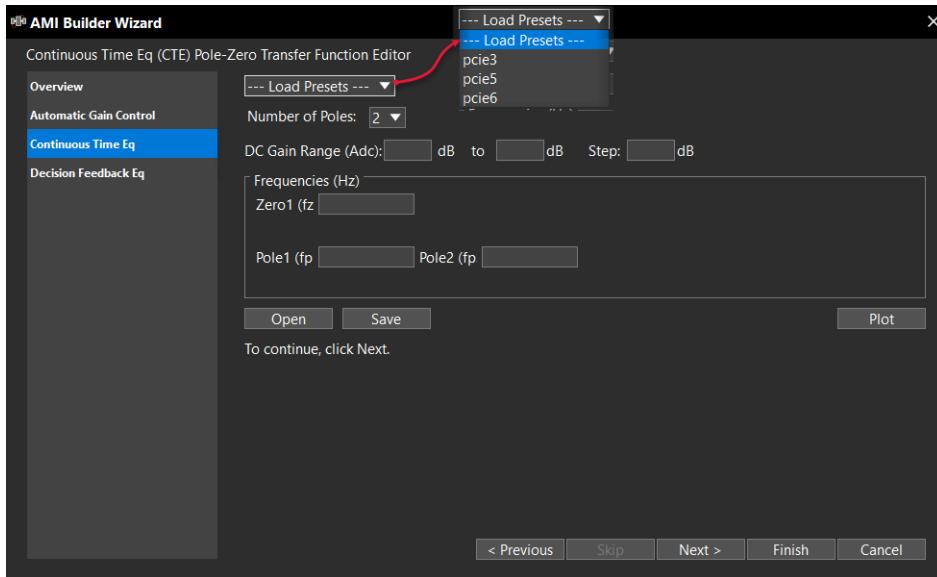
The CTE can be modeled in one of the following ways:

- ❑ *Pole Zero Transfer Function*: Select this option to use poles and zeros of the transfer function for modeling CTE. Clicking *Next* after the selection, displays the

# Topology Workbench User Guide

## Using the AMI Builder

*Continuous Time Eq (CTE) Pole-Zero Transfer Function Editor* within the wizard.



Fields	Description
<i>Load Presets</i>	Select from the listed saved presets for the published specifications. For example, PCIe3, PCIe4, PCIe5, PCIe6, USB3, USB4, HDMI2, and so on.
<i>Number of Poles</i>	Select the number of poles from the range of 2 to 7.
<i>DC Gain Range (Adc)</i>	Displays the preset DC gain range in editable fields.
<i>Steps</i>	Displays the preset steps in an editable field.
<i>Frequencies</i>	Displays the pole and zero frequencies in editable fields. The number of zeros is one less than the selected <i>Number of Poles</i> . For example, when you select 4 from the <i>Number of Poles</i> list, the <i>Frequencies</i> section displays Zero 1, Zero 2, and Zero 3 frequencies.
<i>Open</i>	Click to open an existing .pz file.
<i>Save</i>	Click to save the current settings in a .pz file.
<i>Plot</i>	Click to generate the frequency and magnitude plots of the transfer function for the specified DC gain values.

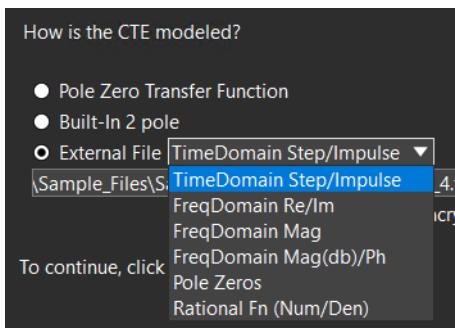
- **Built-In 2 pole:** The filter is similar to that defined in the PCI Express specification, with a cut-off and roll-off frequency, and a control for the AC gain. The model will

## Topology Workbench User Guide

### Using the AMI Builder

automatically set the cut-off and roll-off frequencies based on the data rate of the serial link.

- **External File:** The CTE filter can be described using an external file where you can specify any of the following filters:



Filter	Description
<i>TimeDomain Step/ Impulse</i>	Multi-column Time Domain step/narrow pulse response with time in the first column.
<i>FreqDomain Re/Im</i>	Multi-column Freq Domain response with frequency in the first column and Real/Imaginary values for each response.
<i>FreqDomain Mag</i>	Multi-column Freq Domain response with frequency in the first column and magnitude values for each response.
<i>FreqDomain Mag (db)/ Ph</i>	Multi-column Freq Domain response with in db/Ph fomat.
<i>Pole Zeros</i>	Filter in pole zeros form. This filter is in tree format with a select value as the parameter followed by a DC gain and poles/zeros as values.
<i>Rational Fn</i>	Filter in rational function (laplace, num/den) form. This filter is in tree format with a select value as the parameter followed by a DC gain and numerator/denominator as values.

#### 12. Select the *External File* option.

The Using CSV Input files with AMI Builder Wizard section lists the requirements the file needs to fulfill.

**Note:** When the *External File* option is selected, the *Encrypt* check box is enabled to allow encryption of the file. Select this check box to protect the IP information by encrypting the data files that are referred from the AMI model. This creates a .enc file,

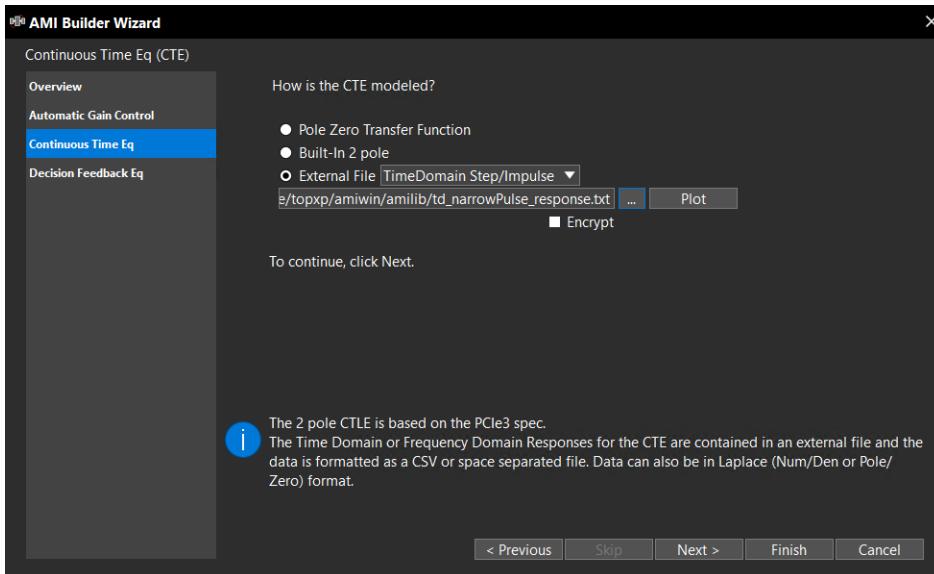
# Topology Workbench User Guide

## Using the AMI Builder

which is an encrypted version of the csv/data file. The models decrypt these files at run time irrespective of the tool these models are being used in. Only data files using the `csvfilt - file` parameters can be encrypted.

13. Choose *Time Domain Step/Impulse*.
14. Browse to the following path and select `td_narrowPulse_response.txt`:

`<INSTALL_DIR>\share\topxp\amiwin\amilib\`



You can view the contents of this file in a text editor. It is a two-column text file of data in Seconds and Volts. Multiple time domain responses can be defined in these files by

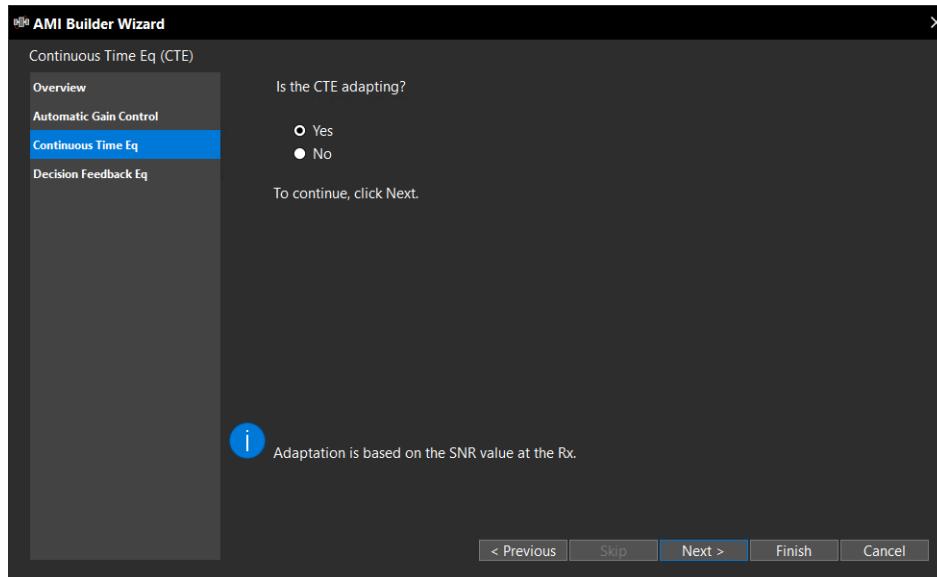
## Topology Workbench User Guide

### Using the AMI Builder

adding multiple voltage columns of data. In this case, only one time domain response is defined.

```
1 * Time Domain Transfer Function Table for
2 * CADENCE'S SystemSI - Serial Link Analysis
3 *
4 * This file contains an example Narrow Pulse transfer
5 * function for use with SystemSI's Analog Filter AMI
6 * model, which is comprised of the files amictwf.ami
7 * and amictwf.dll.
8 *
9 * The columns in the table below are for:
10 * Time in Seconds, Voltage in Volts
11
12 0 -0.003000885
13 3.91E-12 0.001953797
14 7.81E-12 0.001563143
15 1.17E-11 -0.001546511
16 1.56E-11 -0.004748831
17 1.95E-11 -0.002362388
18 2.34E-11 0.023514622
19 2.73E-11 0.08442844
20 3.13E-11 0.154282692
21 3.52E-11 0.202593883
22 3.91E-11 0.218972674
23 4.30E-11 0.202655568
24 4.69E-11 0.17128828
25 5.08E-11 0.142812291
26 5.47E-11 0.117942905
27 5.86E-11 0.094053777
28 6.25E-11 0.072378132
29 6.64E-11 0.054509818
30 7.03E-11 0.039625587
31 7.42E-11 0.026615665
32 7.81E-11 0.015641266
33 8.20E-11 0.006977796
34 8.59E-11 8.64E-05
35 8.98E-11 -0.005619522
36 9.38E-11 -0.010104403
37 9.77E-11 -0.013284073
38 1.02E-10 -0.01550325
39 1.05E-10 -0.017118743
```

#### 15. Click Next.



The CTE can be configured for a particular setting, or allowed to adapt. The time domain data has only one pulse response defined in it so does not adapt.

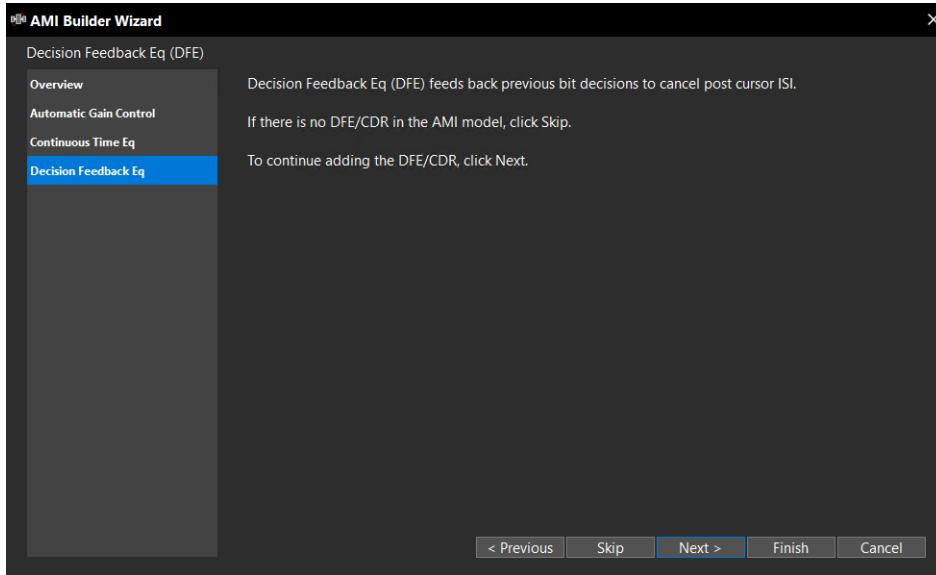
#### 16. Select No and then click Next.

Adaptation is based on the signal-to-noise ratio, or SNR.

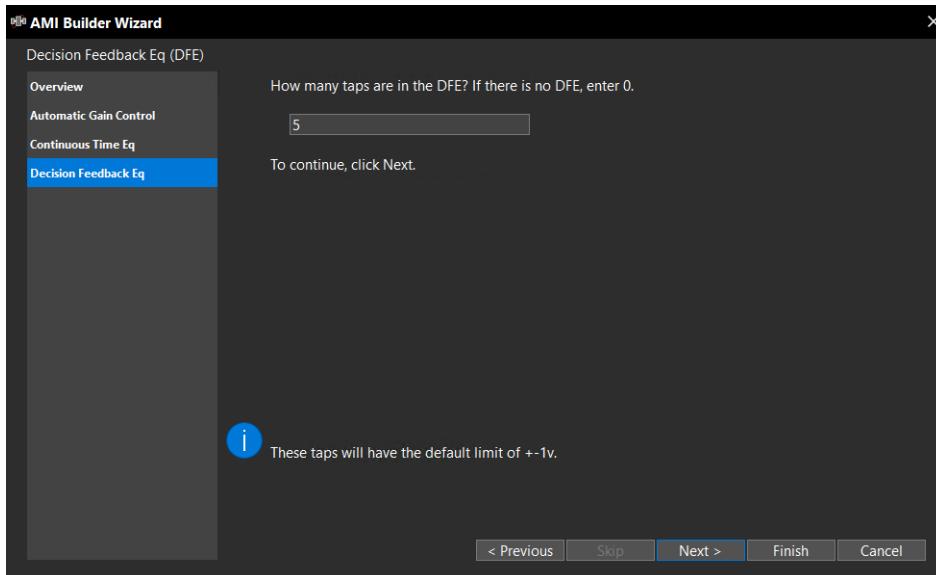
# Topology Workbench User Guide

## Using the AMI Builder

For this example, a DFE block will be included in the model.



17. Click *Next* to add a DFE block to the model.



18. Define how many taps are there in the DFE block. Set the value of 5.

19. Click *Next*.

You can define the DFE as one of the following:

- Analog

An analog DFE continuously adapts after every bit.

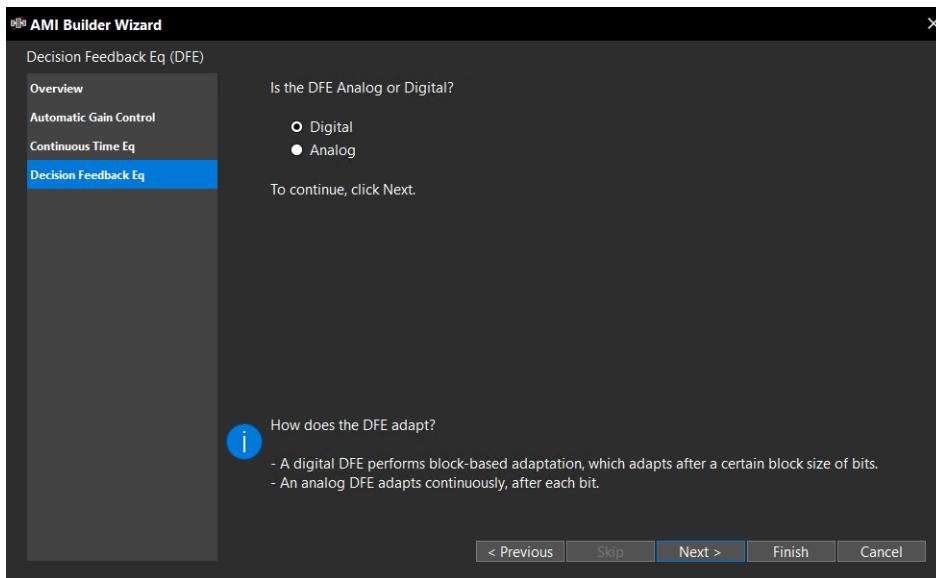
# Topology Workbench User Guide

## Using the AMI Builder

### Digital

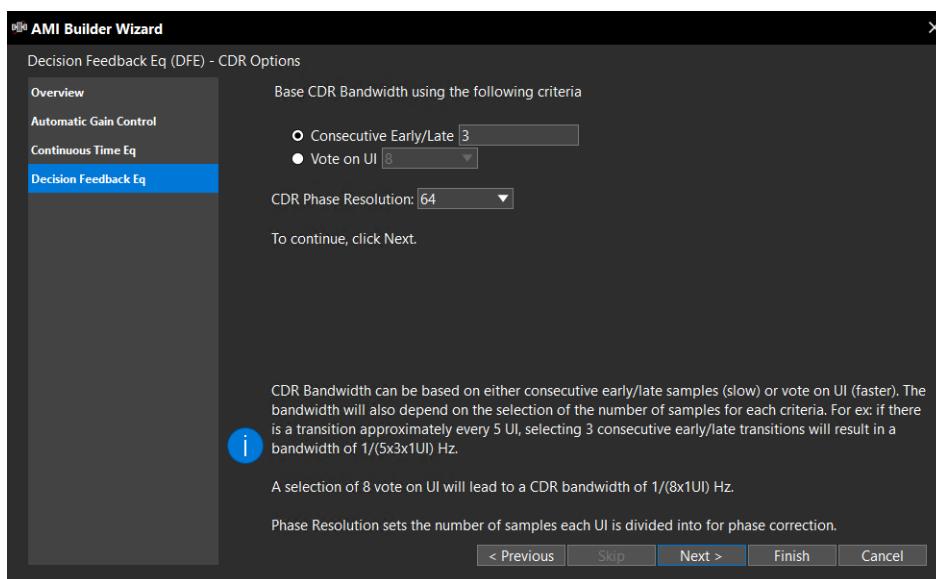
A digital DFE examines a predefined block size of bits, make a decision, and then adapt.

In this example, set this to *Digital*.



20. Click *Next*. The *Decision Feedback Eq (DFE) - CDR Options* are displayed.

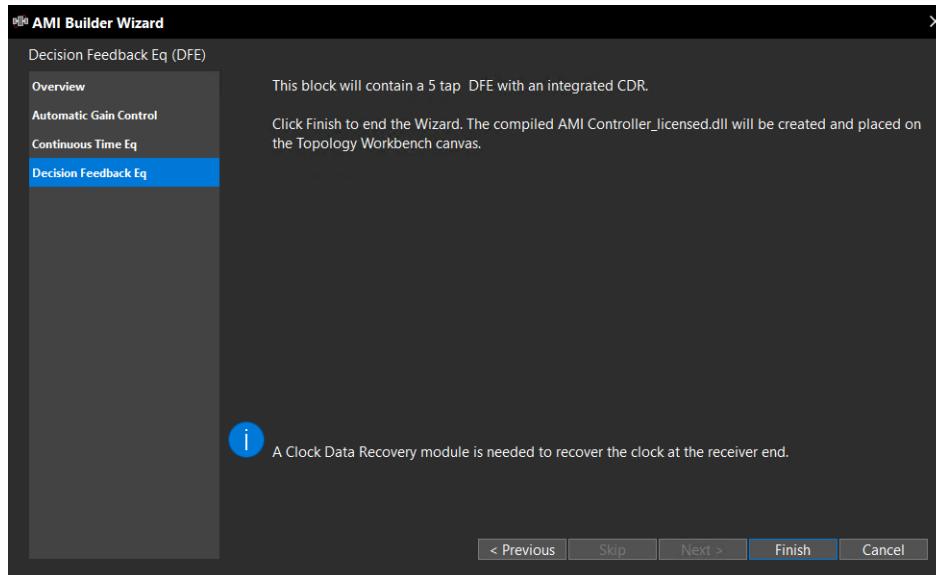
21. Specify the criteria for base CDR bandwidth.



## Topology Workbench User Guide

### Using the AMI Builder

**22.** Click *Next*. A summary of your choices is displayed.



**23.** Click *Finish* to save the specifications for the new Rx AMI model.

### Using CSV Input files with AMI Builder Wizard

You can also create a CSV file and use that as an input for AGC and CTE modules. AMI Builder Wizard checks the CSV file for the following:

- There must be a minimum of two columns
- Columns should be separated using space, tab, or comma
- each column should have the same number of data points
- Minimum of three data points
- Entries that begin with asterisks are treated as comments
- Asterisks in the middle of an entry are not supported.

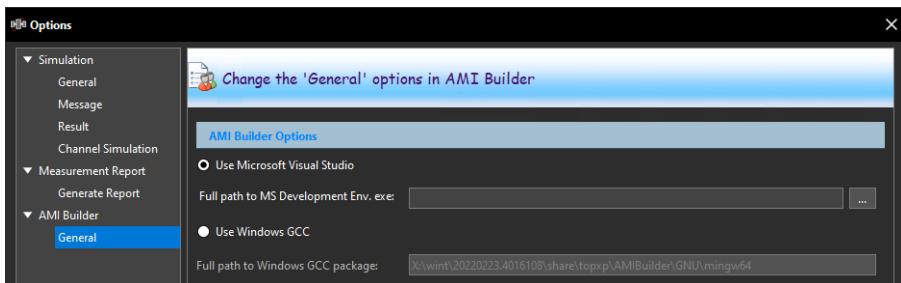
These tests are valid only for Time domain Step/Impulse, FreqDomain Re/Im, and FreqDomain Mag files.

## Topology Workbench User Guide

### Using the AMI Builder

## Compiling the AMI Model

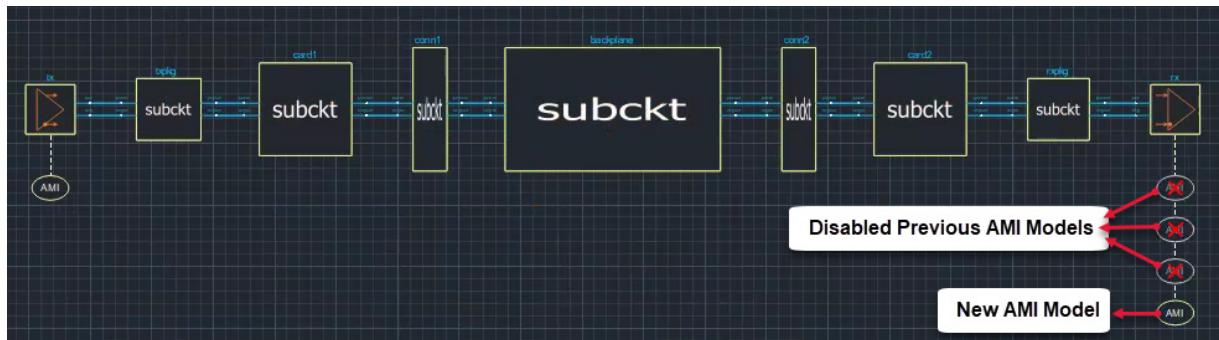
Ensure that the path to the compiler is set in *Tools – Options – AMI Builder – General*.



- Click *Build AMI Model* from the Workflow panel or click the *play* button from the toolbar. A dialog box is displayed for you to browse the folder to save the result files.

After the model compilation completes:

- The new model appears on the canvas
- The original Rx AMI model gets disabled
- A message is displayed in the *Output* tab of the Session Log Panel notifying you that the model has been created and the path where it is saved.



### Important

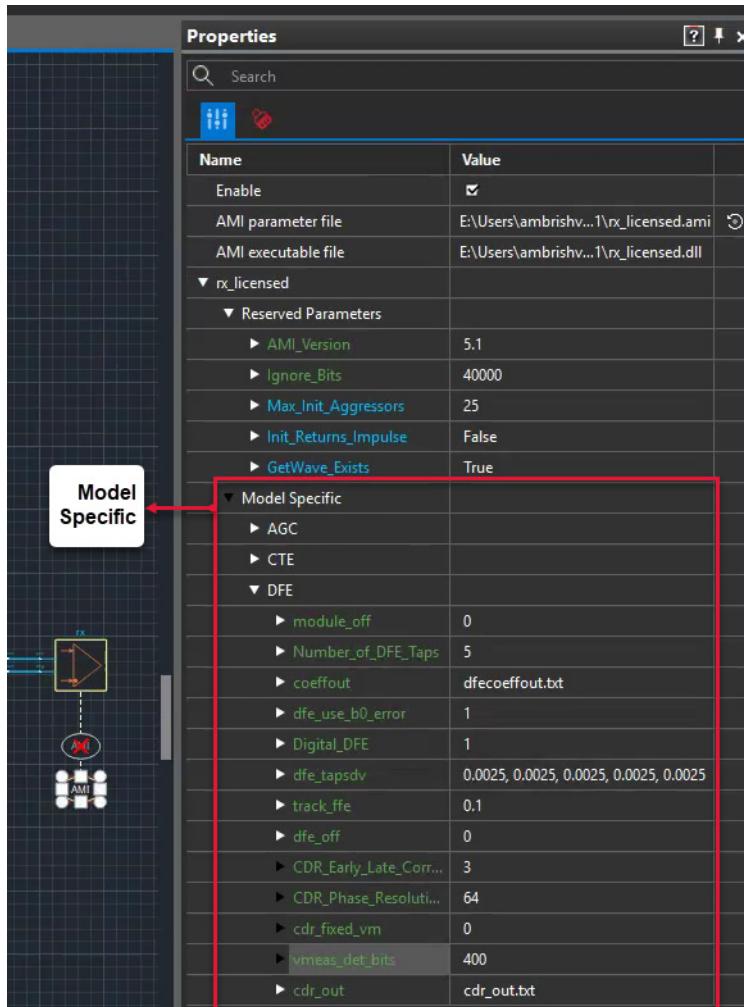
If for any reason the model is not created due to compilation errors, there will be no message displayed in the *Output* tab of the Session Log panel. To troubleshoot build failure, access the AMI builder folder and check the log files saved in it.

# Topology Workbench User Guide

## Using the AMI Builder

### Verifying the AMI Model Creation

1. Double-click the new AMI bubble to review its contents in the *Edit Properties* panel.



2. Browse to the location of the .ami and .dll files.

work > SystemSI > TopXp_Runs_SLA > my_top_ami > ami_builder > 1 >			
Name	Date modified	Type	Size
SRC	9/18/2019 10:07 AM	File folder	
build_ami.log	9/18/2019 10:07 AM	Text Document	4 KB
cdns_tx_rx.ibs	9/18/2019 10:07 AM	IBS File	3 KB
rx_licensed.ami	9/18/2019 10:07 AM	AMI File	7 KB
rx_licensed.dll	9/18/2019 10:07 AM	Application extens...	2,157 KB
rx_licensed.module	9/18/2019 10:07 AM	MODULE File	4 KB
rx_licensed.module.wiz	9/18/2019 10:07 AM	Microsoft Word W...	1 KB

All the AMI Builder wizard generated content is found here.

## Topology Workbench User Guide

### Using the AMI Builder

- ❑ A simple IBIS file `cdns_tx_rx.ibs` that is a starting point for the circuit model for the Rx.
- ❑ The `.ami` and `.dll` files comprise the AMI model.
- ❑ The `.module` file is the blueprint for the AMI model.

You can store this module in a library as a reusable element, open it as a starting point for your next AMI model, edit parameters, recompile, and produce new AMI models.

### 3. Browse into the *SRC* directory.

Name	Date modified	Type	Size
x64	9/18/2019 10:07 AM	File folder	
rx_licensed.c	9/18/2019 10:07 AM	C Source	5 KB
rx_licensed.h	9/18/2019 10:07 AM	C/C++ Header	1 KB
rx_licensed.vcxproj	9/18/2019 10:07 AM	VC++ Project	3 KB

Here you see the following:

- ❑ IBIS `cdns_tx_rx.ibs` file
- ❑ Visual Studio `.vcxproj` file
- ❑ Header `.h` file
- ❑ C code `.c` file

```
rx_licensed.c - Notepad
File Edit Format View Help
// ****
// C Source File for rx_licensed
// Developed by CADENCE DESIGN SYSTEMS using CADENCE's SystemSI AMI Builder
// Wed Sep 18 17:40:31 2019
//
// ****
#include "rx_licensed.h"

static void *recastparams (void *p)
{
void *p2=0;
void *p1=0;
void *temp=0;
char *val=0;

p1 = tlTreeCopy(p);
temp = tlParamFind2ci(p1, "AGC", "Simple_Gain");temp = tlParamFind1ci(p1, "AGC");

p2 = tlParamAddSubParamType (temp,"agcgainmax" );
p2 = tlParamAppendStr (p2,"3" );

p2 = tlParamAddSubParamType (temp,"agcgainmin" );
p2 = tlParamAppendStr (p2,"0.5" );

p2 = tlParamAddSubParamType (temp,"agcgainpts" );
p2 = tlParamAppendStr (p2,"128" );

temp = tlParamFind1ci(p1, "AGC");
p2 = tlParamFind1ci(temp, "adapt_agc_sel_file");
tlParamReplaceId (p2,"adapt_cte_sel_file" );
```

## Topology Workbench User Guide

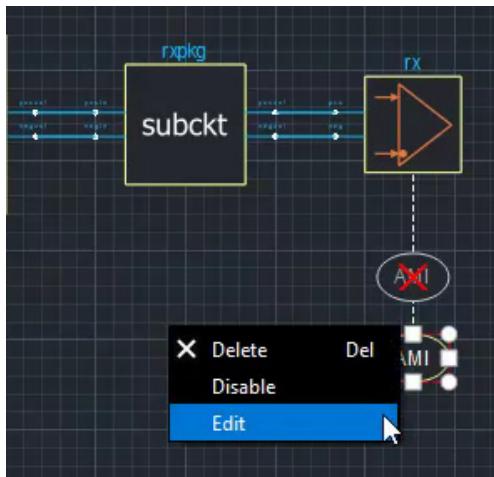
### Using the AMI Builder

Each time you compile the AMI model, a new folder gets created with an incremented number in the *History* folder.

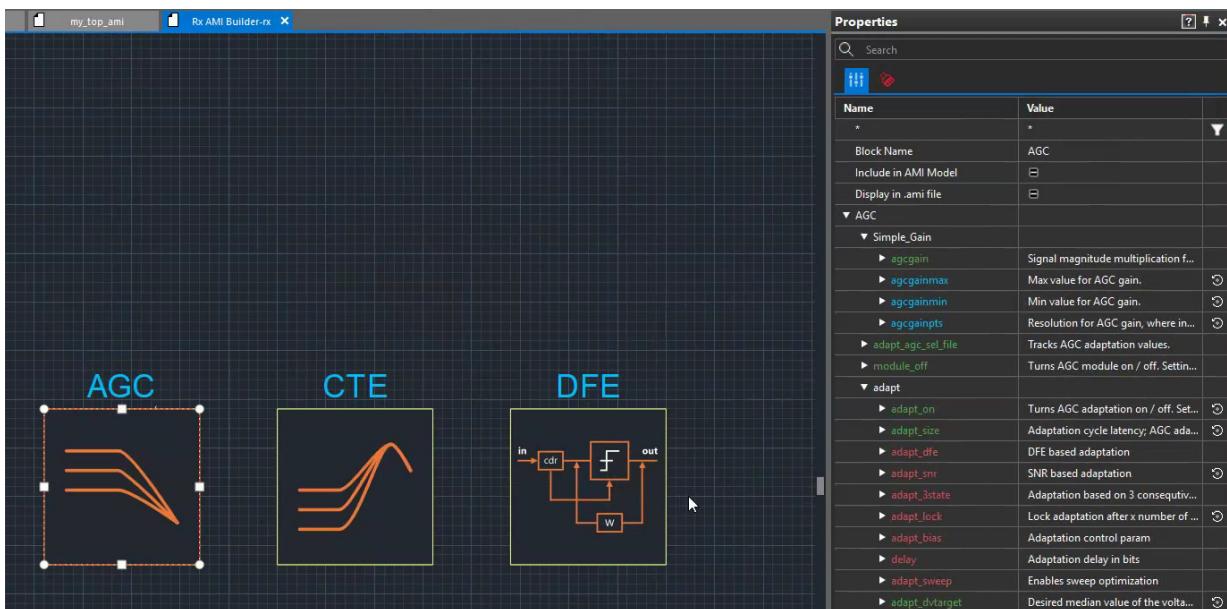
## Editing an AMI Model

To edit an AMI model created, perform the following tasks from the Topology Workbench canvas:

1. Right-click the AMI bubble, and choose *Edit*.



The three blocks from the AMI model are displayed.

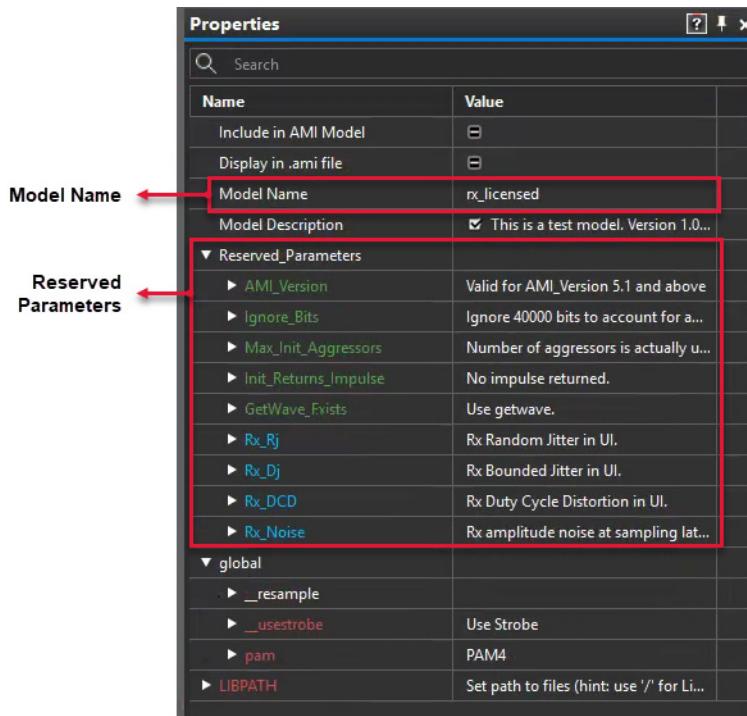


## Topology Workbench User Guide

### Using the AMI Builder

You can change the sequence of them by rearranging their order on the AMI Builder canvas, or double-click a block to open the *Edit Properties* panel for reviewing all of the *Model Specific* parameters associated with that block.

Alternatively, you can choose *View – Edit Properties* from the menu bar to open the properties of the entire AMI model.



This window shows you the *Reserved Parameters* and *global* parameters. You can rename the parameters, change their values, and control their visibility in the *.ami* file. This allows control over what parameters are exposed to the users of the model, what they are called, and what their values are.

In the next step, some sample changes have done.

**2. Make the following changes:**

- In the DFE section, look for *Number\_of\_DFE\_Taps*, and click 5.
- Deselect the *Display in the .ami file* check box to hide this parameter from the generated results.

The parameter will still be included in the AMI model, but you will not see it in Topology Workbench, or be able to edit the number of DFE taps. Its value will remain locked at 5.

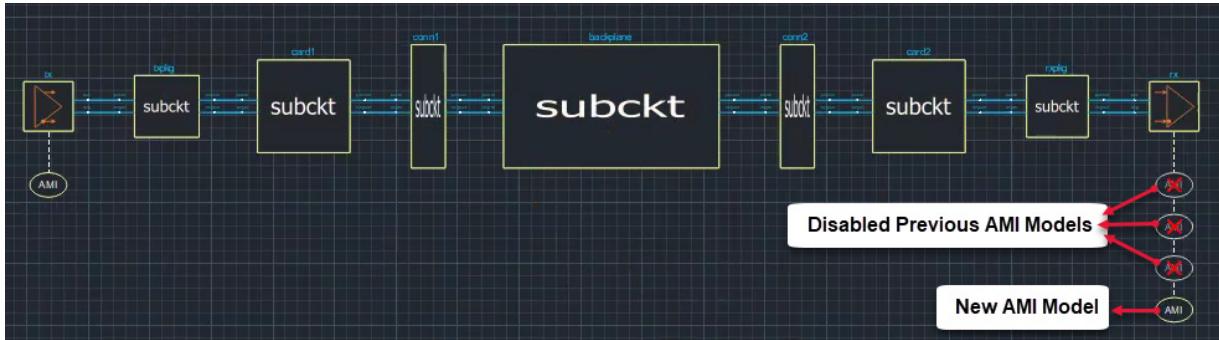
**3. Repeat step 2 for the `dfe_use_b0_error` parameter.**

## Topology Workbench User Guide

### Using the AMI Builder

4. Compile the AMI model once again to implement the changes done in steps above.
5. Click *Build AMI Model* from the *Workflow* panel or click the *play* button from the toolbar.

On completion of the compilation process for the new model, the AMI model editor tab closes, and the Topology Workbench canvas is displayed with the new model attached.

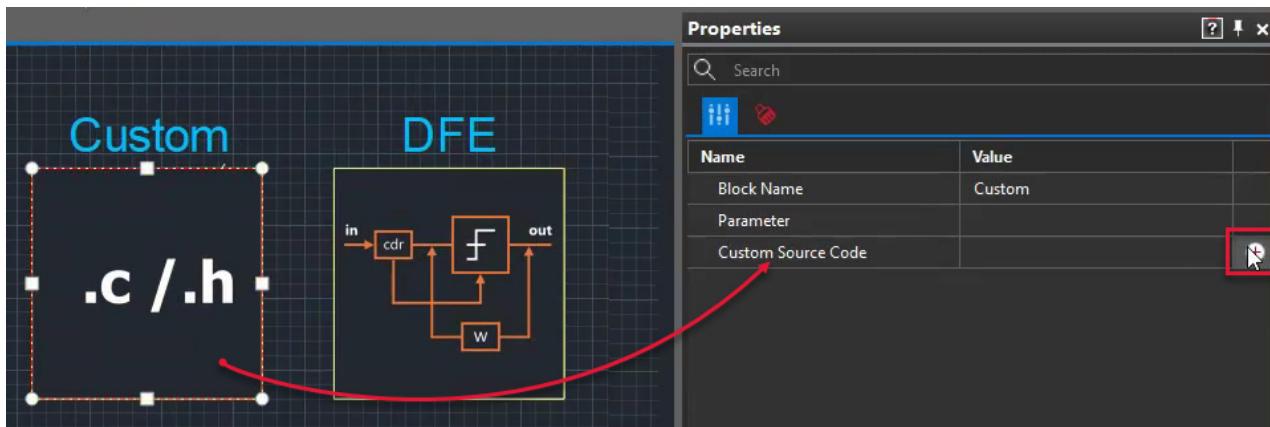


6. Double-click the new AMI bubble, and verify that those two parameters are no longer visible in the DFE section of the model.
7. Close the AMI model editor.
8. Start the simulation (click the play button) in the toolbar.
9. Right-click the Rx AMI bubble, select *Disable* and re-run the simulation to see the difference without the AMI model that was created.

**Note:** In the Topology Workbench – SystemSI workflows, a default control, PostProcessDCOffset, handles the single-ended signal measurement and coordinates with DFE. However, if the AMI model in a topology already has a DC-shift control, you need to either switch it off in the AMI model or disable the PostProcessDCOffset default control from the *Analysis Options* panel.

## Adding Custom Blocks to Tx and Rx AMI Models

You can add custom code to the Tx and Rx AMI models using the AMI Builder. This allows you to enter own C/C++ code that can work (if desired) with the available modules in AMI Builder. Use the API provided to integrate code into the AMI model.



You can add code to the custom block to include functionality that is not provided in the AMI Builder.

1. Double-click a custom block.

The *Edit Properties* panel of the custom block opens.

2. Enter all the required sections of the model-specific parameters for the custom block.

**Note:** These parameters are not modified by the AMI Builder.

3. Click the + button in the *Custom Source Code* row.

4. Enter the filenames for the custom code.

Include all the required .cxx/c.h files for the custom block for successful compilation.

The user Getwave seamlessly stitches with other modules in AMI Builder if the custom source code uses the following API ('user\_init' and 'user\_getwave') when writing the Init and the Getwave and free any object that they create using 'user\_destroy'.

### User Block API

The following API needs to be used in the user code (instead of the IBIS API) in order to integrate the user block with the rest of the AMI modules.

```
extern long user_init (double *impulse_matrix,
```

```
long row_size,  
long aggressors,  
double sample_interval,  
double bit_time,  
char *AMI_dll_parameters_in,  
char **AMI_dll_parameters_out,  
void **AMI_dll_memory_handle,  
char **msg);  
  
extern long user_getwave (void *r xm,  
                         double *wave,  
                         long wave_size,  
                         double *clock_times,  
                         char **AMI_dll_parameters_out,  
                         char *msg);  
  
extern void user_destroy (void *obj);
```

## Supported Blocks for an AMI Model

This section lists all the available blocks for an AMI model:

- [Tx AMI Model Blocks](#)
- [Rx AMI Model Blocks](#)

### Tx AMI Model Blocks

For the Tx AMI model, the available blocks are [FFE](#) and [Gain](#).

#### FFE

The FFE block specifies the number of taps for the Feed Forward Equalizer filter and other parameters that control how the FFE behaves. These include the normalized tap limits (lffe) and limit to the sum of taps (csum). The FFE also sets Preset Taps to be used for the Tx AMI model. The number of preset taps can vary. Enter the tap values for any set of preset tap. If

the ID (id) for preset taps is set to nil, the FFE block auto optimizes the tap values and uses that in the simulations.

## Gain

The Gain block is a simple analog voltage gain that multiplies the incoming waveform with a scalar factor.

## Rx AMI Model Blocks

For building an Rx AMI model, the following available blocks are available:

- [Analog Gain Control \(AGC\)](#)
- [Continuous Time Equalizer \(CTE\)](#)
- [DFE/CDR](#)

### Analog Gain Control (AGC)

The AGC boosts the analog signal to a sufficient level such that the DFE can detect the level and perform further equalization. You can choose to perform adaptation on the AGC block based on various factors, such as eye opening (`dvrf_target`) or early/late algorithms (`adapt_early_late`). Adaptation can also be optimized by the AMI model by using the `adapt_sweep` parameter.

### Continuous Time Equalizer (CTE)

The CTE is used in selective boosting at frequency of interest (high freq channel loss cancellation).

There are various ways of implementing the CTE filter in the AMI Builder. These include using table-based response files for each curve (comma separated tables), using pole-zeros of the transfer function, defining the numerator and denominator of the rational function of the transfer function and using the predefined format for the PCIe gen3 specification which defines the frequency values for the cutoff and roll off frequencies as well as a relative gain.

The CTE can be set to perform adaptive equalization based on signal to noise measurement.

## **Topology Workbench User Guide**

### Using the AMI Builder

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#### **DFE/CDR**

The DFE/CDR block contains the DFE and the CDR functions. You can turn off the DFE or the CDR. Note, however that the DFE depends on the CDR. If the CDE is turned off, no DFE functionality will be available. Choose the number of DFE taps that are needed to be modeled. This block can also be adapted based on the factors described for CTE and AGC.

## Using SystemPI Workflow

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The SystemPI workflow of Topology Workbench allows you to build custom system-level topologies and run alternating current (AC), direct current (DC), and time domain power integrity analysis. Using Topology Workbench, you can perform general-purpose pre- and post-layout exploration of topologies as discussed in this chapter.

### ***Related Topics***

- [Performing PDN Impedance and Power Ripple Analysis](#)
- [Performing DC IR Drop Analysis](#)
- [Configuring the Blocks for SystemPI Workflows](#)

## Performing PDN Impedance and Power Ripple Analysis

In the SystemPI workflow, power distribution network (PDN) impedance analysis is used to select extracted models for the PDN of a chip, package, and PCB. Then, connect these extracted models together and apply current source(s) excitation at the chip location. Power ripple analysis is used to run a transient circuit simulation and analyze the ensuing power ripple to verify that it remains within the specification.

To perform PDN Impedance and Power Ripple Analysis:

1. Start Topology Workbench using a method described in the [Starting Topology Workbench](#) topic.

**Note:** When you open Topology Workbench in standalone mode, choose *Advanced PI //* from the *Cadence Product Choices* dialog box to run SystemPI workflow. If you are switching to the SystemPI workflow from another workflow such as SystemPI – Parallel Bus Analysis or Serial Link Analysis, the *Cadence Product Choices* dialog box is displayed again with the relevant choices for selection.

2. Create a topology project for PDN Impedance and Power Ripple Analysis.

## Topology Workbench User Guide

### Using SystemPI Workflow

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For steps, refer to the [Creating a Topology Project from Scratch](#) section or the [Opening an Existing Topology Project](#) section.

When you create a new topology project,

- a. Specify a *Topology Name* and browse the *Topology Path* to save your topology.
- b. Click the *SystemPI* tab.
- c. Select *PDN Impedance and Power Ripple Analysis* from the *Workflow* list box.  
A list of the following default workflow-specific templates are displayed for choice:

Template	Description
<i>ac_multi_IC</i>	Contains multiple IC blocks with alternating current (AC) sources.
<i>ac_single IC</i>	Contains single IC block with alternating current (AC) sources.

You can select one of the default templates or the *<blank topology>* row to start designing your own topology from scratch.

The Topology Workbench window is refreshed as following:

- A tab with the given *Topology Name* opens next to the [Start Page](#).
- The [Layout Canvas](#) is populated with the blocks as per the selected default template. If you chose to create a *<blank topology>*, the canvas is empty.
- The [Workflow Panel](#) opens with a list of tasks you need to perform during the selected type of analysis.
- The [Floating Toolbar](#) opens with a list of various types of blocks that can be used in the selected type of analysis.

3. Add and place the required blocks on the canvas.

For information, see [Adding Blocks to the Canvas](#) and [Appendix A, “Choosing Blocks to Place on the Canvas.”](#)

4. Connect the blocks on the canvas and configure the connections between their signals.

For information, see [Connecting the Blocks on the Canvas](#) and [Managing Connections Between Blocks and Signals.](#)

## Topology Workbench User Guide

### Using SystemPI Workflow

5. Edit and configure the properties of the various components placed on the canvas by using the [Edit Properties Panel](#). You can also assign device models to the controller and memory devices in the displayed panel.

For information, see [Editing the Properties of a Component](#).

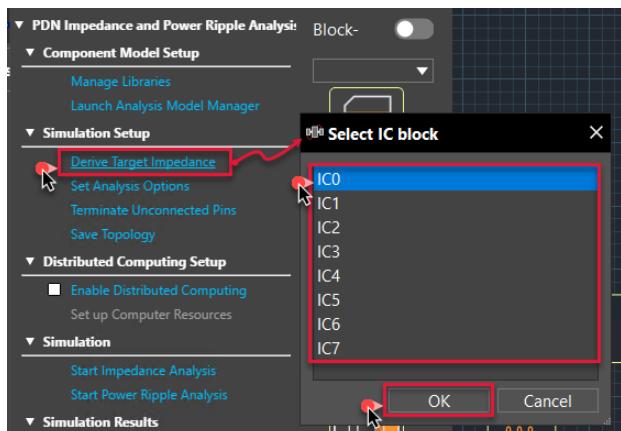
6. Setup and manage the component model libraries.

For information, see [Setting Up Component Model](#).

7. Derive target impedance for the IC blocks as needed.

- a. Click *Derive Target Impedance* from the *Simulation Setup* schema of the Workflow panel. A dialog box opens with a list of all IC blocks that are part of the topology.

- b. Select the required IC block and click *OK*.

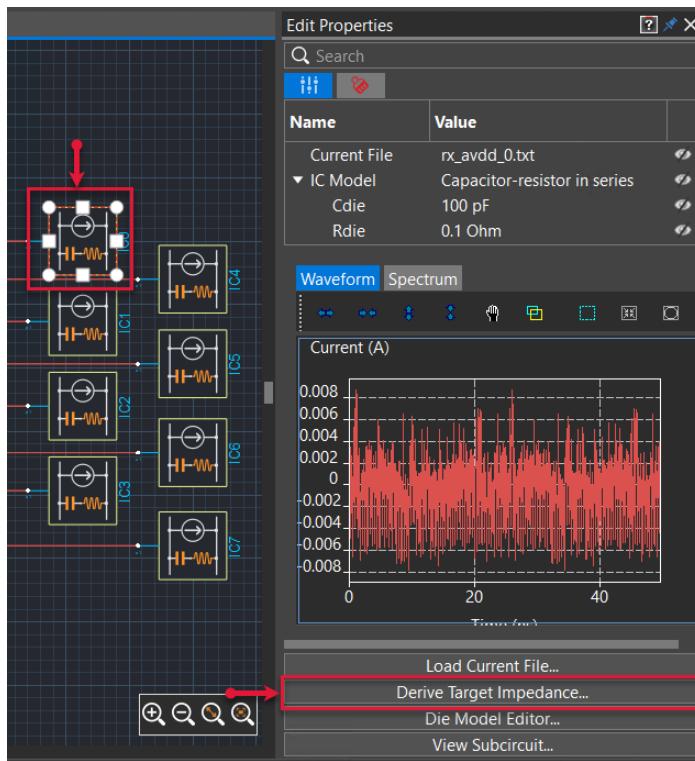


**Note:** Alternatively, double-click the IC block to open the corresponding properties

# Topology Workbench User Guide

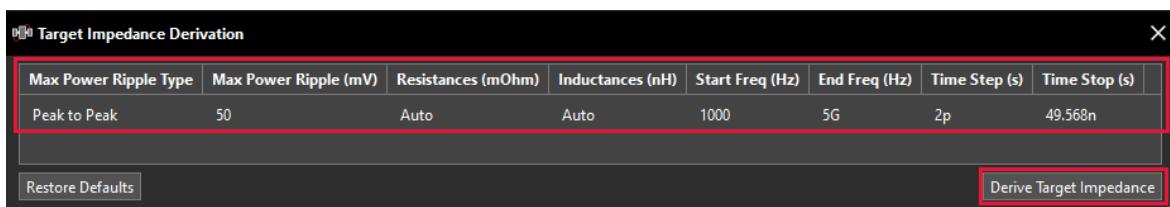
## Using SystemPI Workflow

in the *Edit Properties* panel and click the *Derive Target Impedance* button.



The *Target Impedance Derivation* dialog box opens.

- c. Edit the values, such as, maximum power ripple type (*Peak to Peak* and *Undershoot*) and value (in mV), resistances, inductances, start frequency (in Hz), end frequency (in Hz), time step (in seconds), and time stop (in seconds).

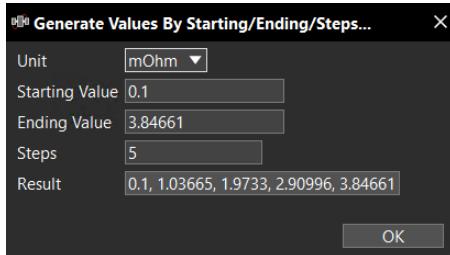


**Note:** The *Resistances* and *Inductances* are calculated automatically by default. Clicking the E button in the cell under these columns displays the Generate Values By Starting/Ending/Steps dialog box. Here, you can change the *Unit* and enter

# Topology Workbench User Guide

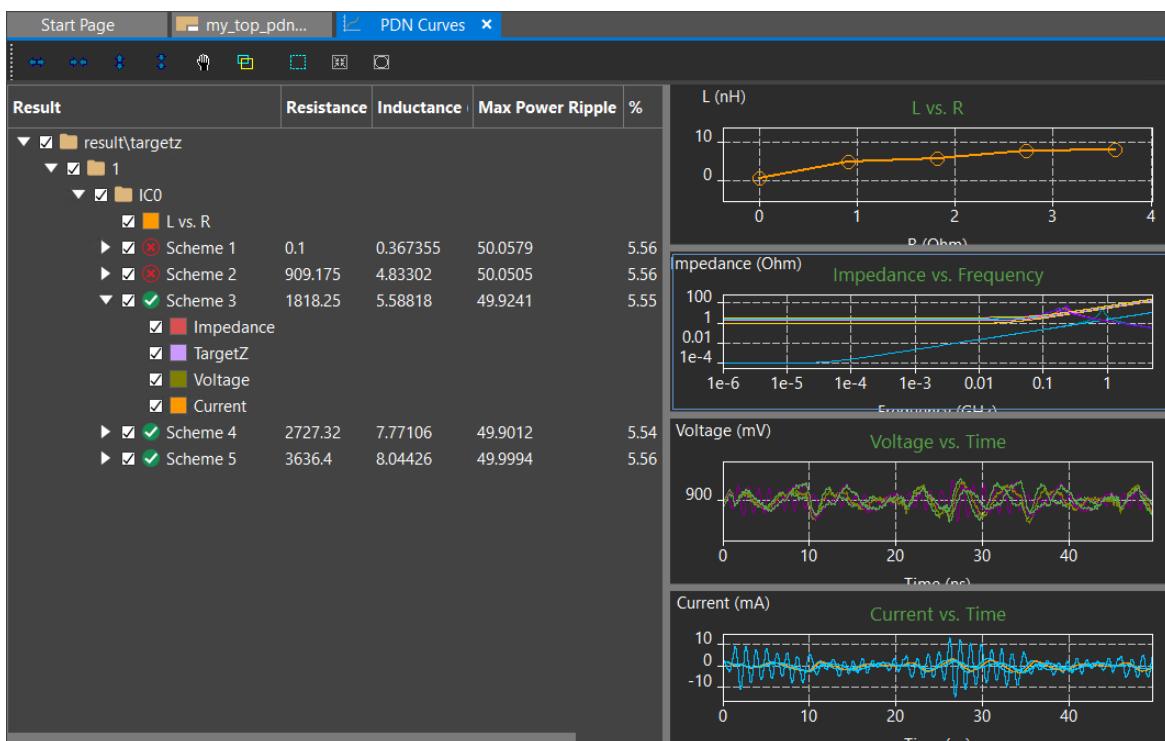
## Using SystemPI Workflow

values in the *Starting Value*, *Ending Value*, and *Steps* fields.



### d. Click *Derive Target Impedance*.

The progress of the run is shown in the status bar. On the completion of the process, the *PDN Curves* tab opens with the *L vs. R*, *Impedance vs. Frequency*, *Voltage vs. Time*, and *Current vs. Time* curves.



In the *Result* pane, the following actions can be performed:

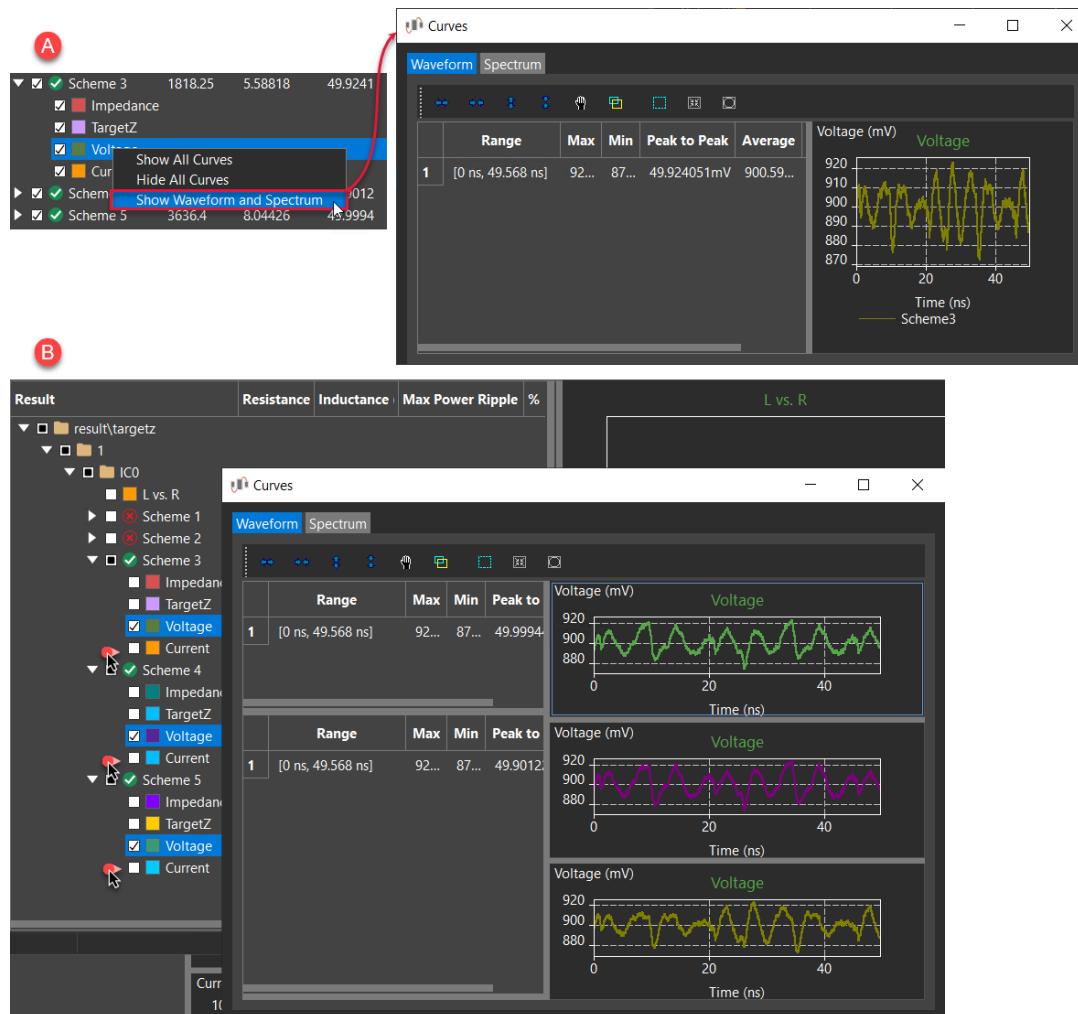
- Select and deselect check boxes in the result tree to control the view of PDN curves as per requirement.
- Click the curve that needs to be studied deeper and rollover the pointer for details shown in annotation balloons.

# Topology Workbench User Guide

## Using SystemPI Workflow

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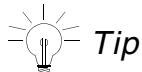
- View whether target impedance derivation passed or failed in the different schemes of optimization.
- Right-click a *Voltage* result and click the *Show Waveform and Spectrum* option. It opens the Curves dialog box to review the results in the *Waveform* and *Spectrum* tabs. This feature supports selection of multiple *Voltage* results while clicking each and keeping the *Ctrl* key pressed. Thereafter, right-click and choose the *Show Waveform and Spectrum* option from the shortcut menu.



8. Click *Terminate Unconnected Pins* in the *Topology Setup* schema to end the impedance of any unconnected pins in the topology.

For information, see [Terminating Unconnected Pins](#).

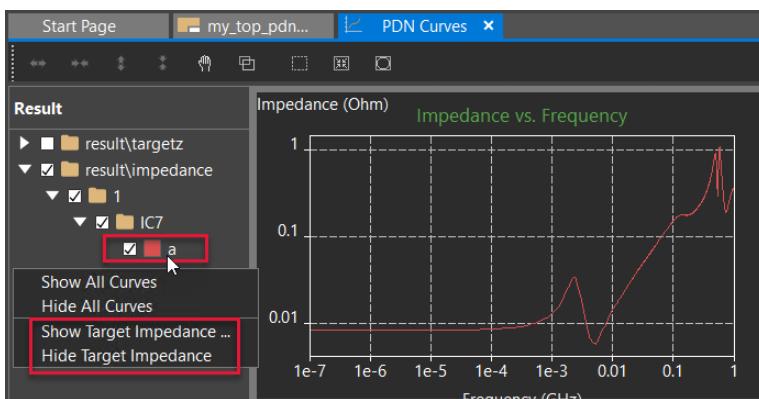
9. Click *Save Topology* in the *Topology Setup* schema.



*Tip*

Alternatively, you can save a topology by clicking in the [Toolbar](#) or choosing [Topology – Save](#) from the [Menu Bar](#).

10. Click *Set Analysis Options* in the *Simulation Setup* schema to open the *Analysis Options* panel. For more information, see [Configuring Simulation Options for SystemPI Workflows](#).
11. Click *Start Impedance Analysis* in the *Analysis Options* panel or from the *Simulation* schema. The simulation starts to run. On the completion of the process, the result is displayed in the *PDN Curves* tab showing the *Impedance vs. Frequency* curve.



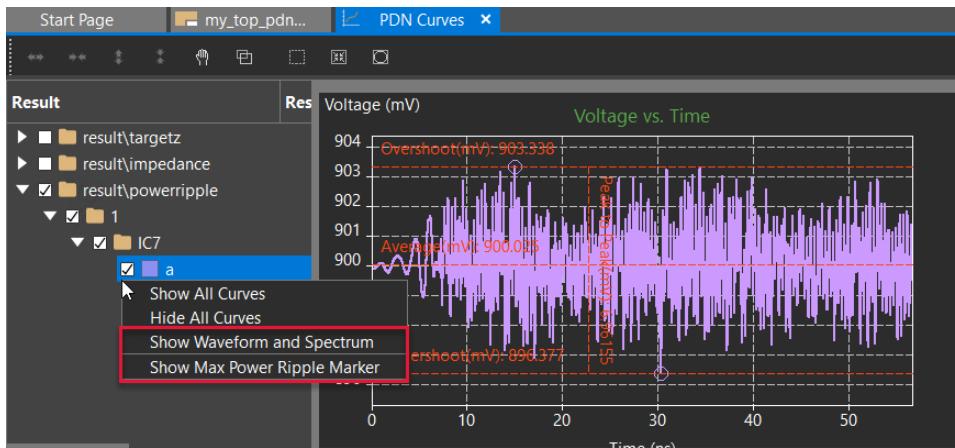
In the *Result* pane for impedance results, the following actions can be performed:

- Show and hide all curves with a single selection.
- Toggle between viewing and hiding target impedance. Right-click a signal and select *Show Target Impedance* or *Hide Target Impedance*.

## Topology Workbench User Guide

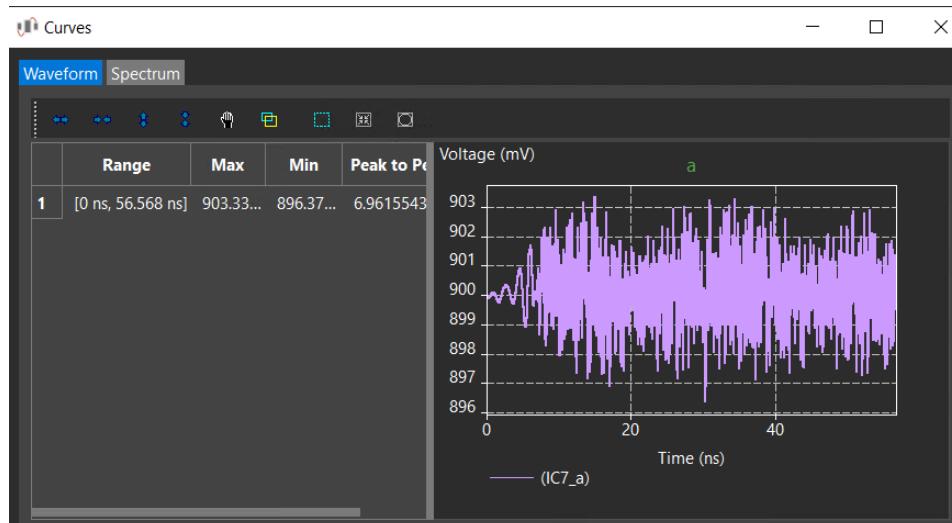
### Using SystemPI Workflow

- 12.** Click *Start Power Ripple Analysis* in the *Analysis Options* panel or the *Simulation* schema. The simulation starts to run and on completion of the process, the result is displayed in the *PDN Curves* tab showing the *Voltage vs. Time* curve.



In the *Result* pane for power ripple results, the following actions can be performed:

- Show and hide all curves with a single selection.
- Right-click a *Voltage* result and click the *Show Waveform and Spectrum* option. It opens the Curves dialog box to review the result in the *Waveform* and *Spectrum* tabs.

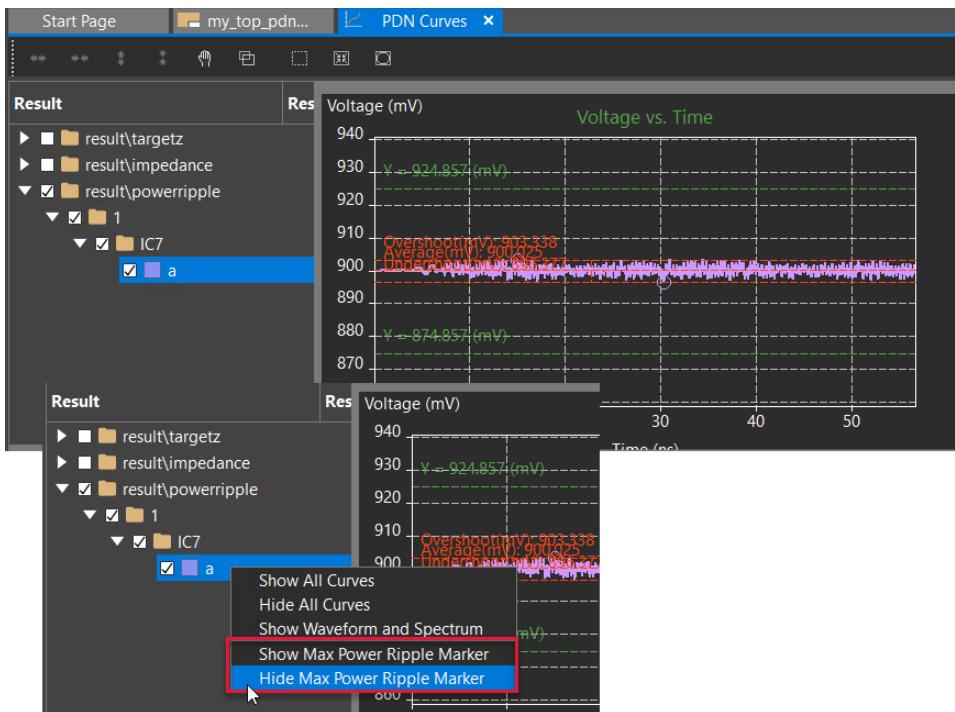


- Toggle between viewing and hiding maximum power ripple marker. When you right-click a signal, initially you have the *Show Max Power Ripple Marker* option to

# Topology Workbench User Guide

## Using SystemPI Workflow

select. When you select this option, the *Hide Max Power Ripple Marker* option is also added to the shortcut menu.



For additional features available in the workflow, see [Related Topics](#) below.

### Related Topics

- [Configuring the Blocks for SystemPI Workflows](#)
- [Viewing Simulation Results](#)
- [Browsing Simulation Results](#)
- [Setting Up Component Model](#)
- [Switching to Another Workflow](#)
- [Customizing a Workflow](#)
- [Creating Custom Templates](#)
- [Archiving a Topology](#)

## Loading PWL File

1. Double-click an IC block to open the *Edit Properties* panel.
2. Click *Load PWL File*. A dialog box is displayed.
3. Browse and select the PWL file that contains pairs of time and values.
4. Click *Open*.

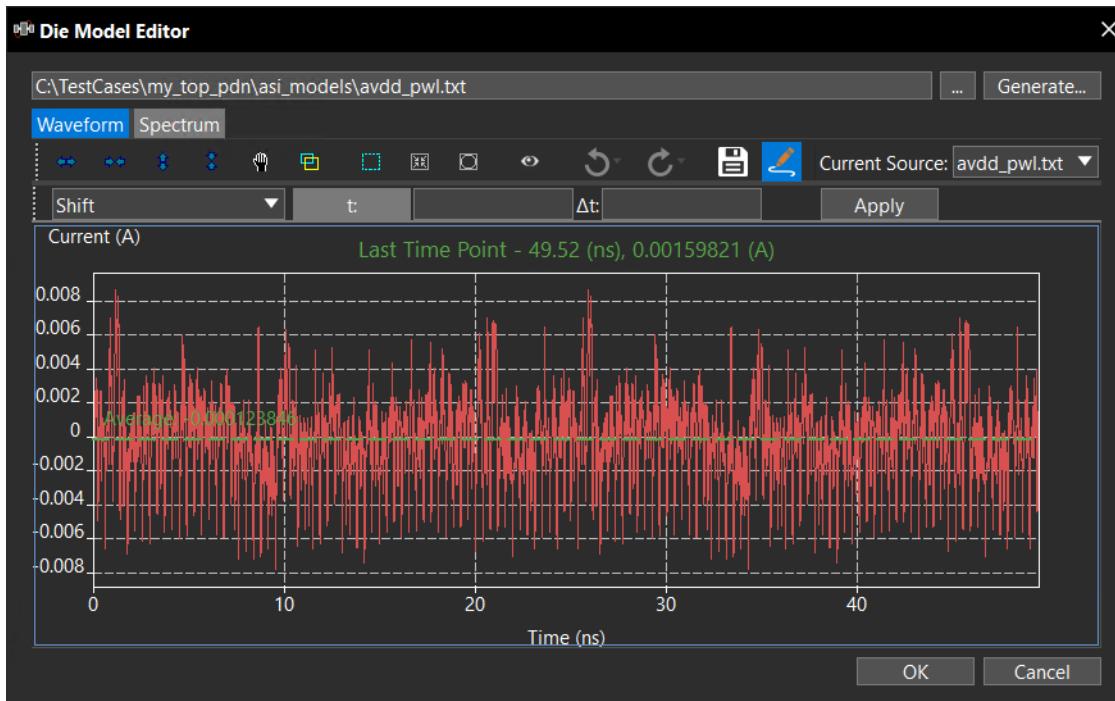
## Editing IC Models using the Die Model Editor

In the SystemPI – PDN Impedance and Power Ripple Analysis workflow, you can use the following types of die models:

- Generic IC power models – Capacitor, Capacitor-resistor in series, Capacitor-resistor in series, two-terminal SPICE subcircuit model, one-port S Parameter
- Generic IC current models – Piecewise Linear (PWL)

To use the Die Model Editor for editing the model:

1. Double-click an IC block to open the *Edit Properties* panel.
2. Click *Die Model Editor*. The editor dialog box is displayed.



## Topology Workbench User Guide

### Using SystemPI Workflow

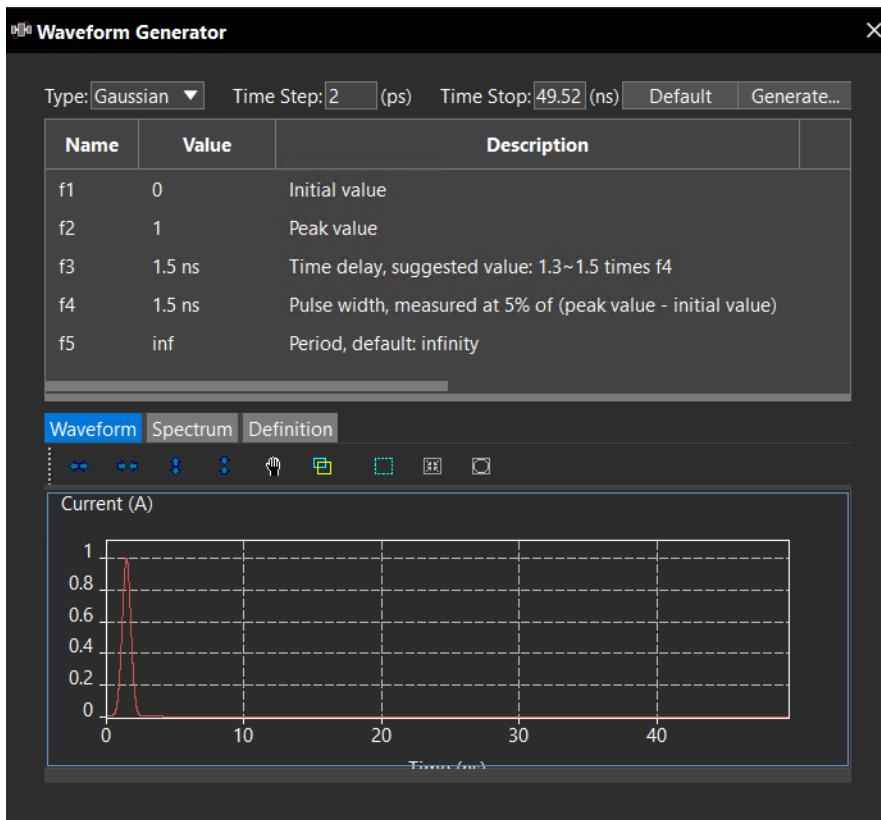
**Note:** Alternatively, click the *Tools – Die Model Editor* menu to open the Die Model Editor.

The path to the currently associated PWL file is shown in a text box. The editor has two tabs – *Waveform* and *Spectrum*. Each tab displays a toolbar containing the edit controls to enlarge or reduce X and Y scales, pan the waveform and spectrum using the cursor, navigate the curve based on time and current, select an area for analysis, zoom in and zoom out, and fit the waveform or spectrum in the designated area.

The *Waveform* tab has additional options in the toolbar, such as undo, redo, show original, and save. The tab also has an option to enable and disable the expression calculator. When the calculator is enabled, the *Waveform* tab allows you to specify the type of edit operation that needs to be performed on the waveform and the corresponding values.

If needed, you can specify a different PWL file using the Browse  button.

3. Click *Generate*. The Waveform Generator dialog box opens.



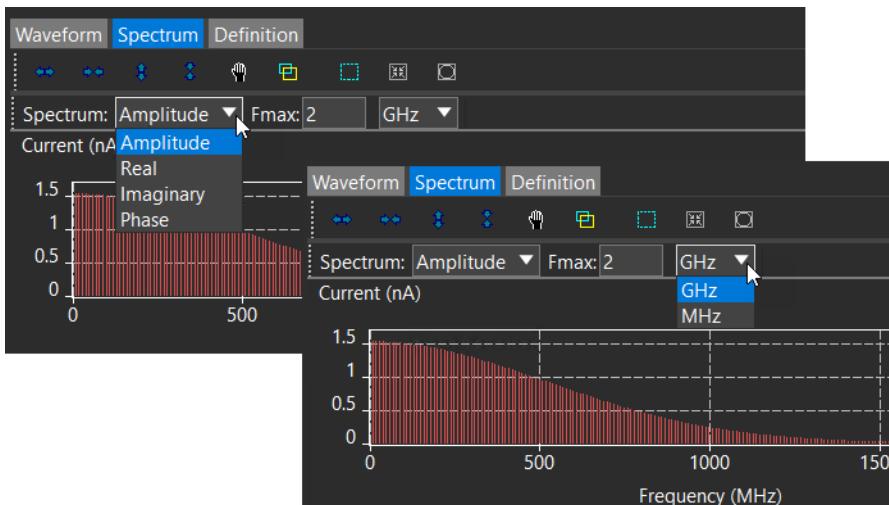
4. Specify the *Type* of waveform from the list of following options: *Gaussian* (default), *PWL*, *Pulse*, *Sinesquare*, and *Random*.

## Topology Workbench User Guide

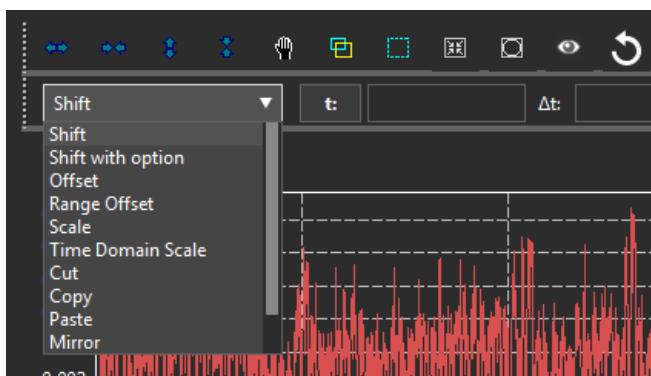
### Using SystemPI Workflow

Based on the selected type, the contents of the table and the tabs (*Waveform*, *Spectrum*, and *Definition*) change.

On the *Spectrum* tab, you can change the type of *Spectrum* (*Amplitude*, *Real*, *Imaginary*, or *Phase*), *Fmax* value, and unit (GHz or MHz).



5. Modify the *Time Step* and *Time Stop* values in the respective boxes as needed.
- Note:** At any time, you can click *Default* to reset the values to the tool defaults.
6. Click *Generate*. A dialog box opens to browse and save the time and value pairs in a file.
7. Specify a name for the file, which can be other than the one given by default, and click *Save*. The Waveform Generate dialog box closes and the contents of the Die Model Editor are refreshed accordingly. The file's name is displayed in the *Current Source* box.
8. Click the list box to select the type of edit operation you want to perform. The following valid values are given for choice: *Shift*, *Shift with option*, *Offset*, *Range Offset*, *Scale*, *Time Domain Scale*, *Cut*, *Copy*, *Paste*, *Mirror*, *Time Domain Merge*, *Current Domain Merge*, *Modulation*, *Smooth*, *Filter*, and *Decimate*.



## Topology Workbench User Guide

### Using SystemPI Workflow

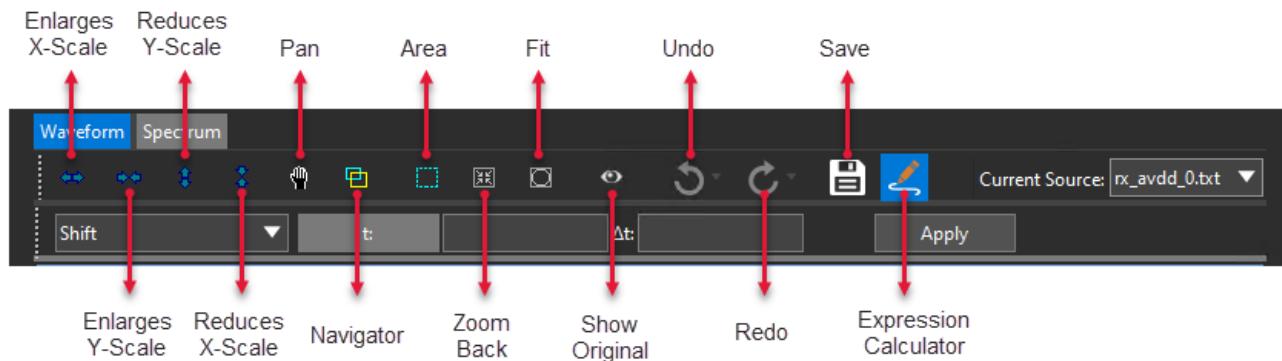
Depending on the selected edit operation, additional fields are displayed to specify the model editing criteria. For example, when you select *Range Offset*, you need to specify the  $t_1$ ,  $t_2$ , and delta value. To specify the  $t_1$  and  $t_2$  values, you can click a point in the graph area and drag the pointer while holding the left-mouse button up to the point of interest. When you release the left-mouse button, the  $t_1$  and  $t_2$  values are populated calculated based on the point you started from to the point where you left the selection. If the specified edit operation cannot be performed, a message is displayed.

When the *Filter* function is used, the frequencies are limited to Nyquist frequency or less. This limit is applied to the low and high pass frequency.

9. Click *Apply* to edit as per the specified criteria.

10. Click *OK* to close the editor.

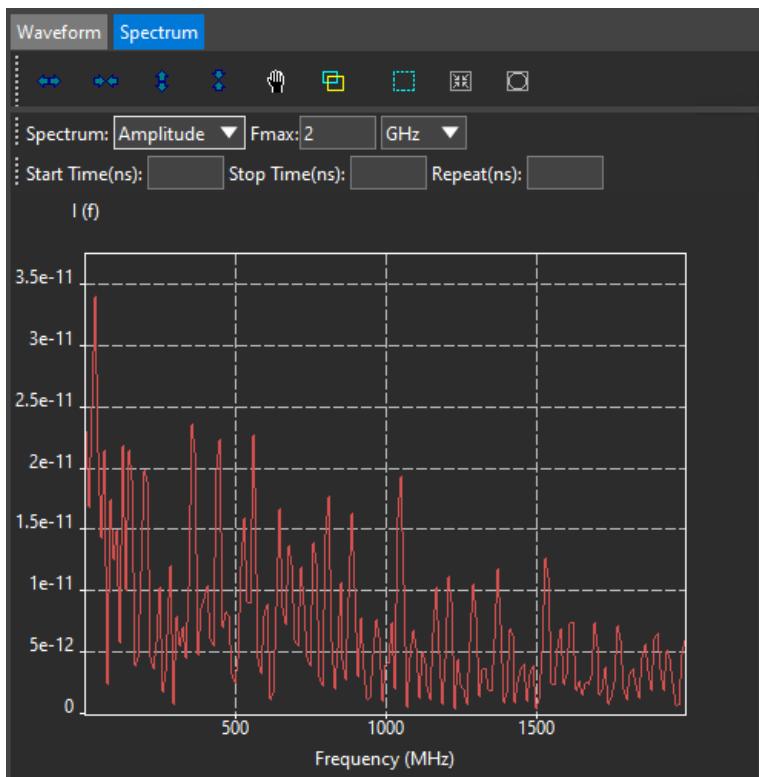
The Waveform tab of the Die Model Editor has the following controls:



## Topology Workbench User Guide

### Using SystemPI Workflow

The Spectrum tab has a subset of the controls given on the Waveform tab:



In the Spectrum tab, you can:

- Select the type of spectrum (Amplitude, Real, Imaginary, and Phase) in the *Spectrum* box.
- Specify the maximum frequency in the *Fmax* box along with its unit (*GHz* or *MHz*).
- Specify the *Start Time*, *Stop Time*, and *Repeat* parameters in nanoseconds.

The *Repeat* option replicates (and repeats) the current waveform in alignment with the specified simulation time. Though Die Model Editor provides the copy and paste option, it is a tedious manual process for longer simulation times. The *Repeat* option can be used alternatively to capture low frequency effects by running the simulation for longer times, and repeating the current waveform beyond what is defined in the die model.

## Running Sweep Simulations in PDN Impedance and Power Ripple Analysis

In the PDN Impedance and Power Ripple Analysis workflow of SystemPI, you can use the Sweep Manager to support frequency domain and time domain sweeps. Sweep Manager

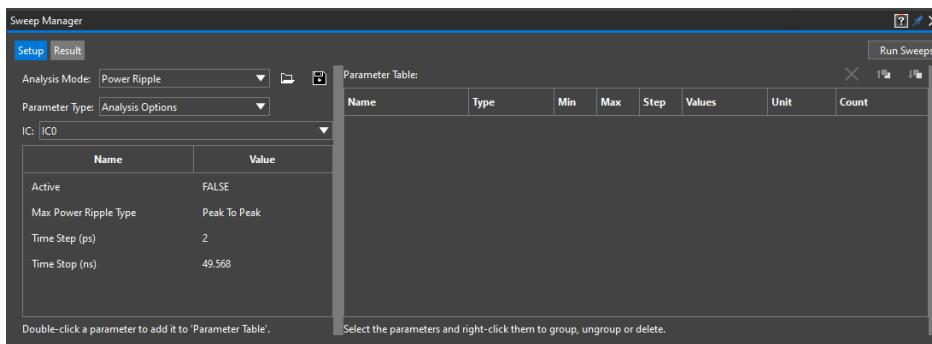
## Topology Workbench User Guide

### Using SystemPI Workflow

allows multiple values to be set for key parameters in the topology. Sweeping then automatically runs multiple simulations, substituting in the relevant parameter values for each unique simulation run. Results can then be analyzed to understand the impact of the parameter values on overall performance.

You can easily browse Sigrity OptimizePI decap libraries and automatically include them in what-if frequency and time domain simulations. In addition, the quantity of decaps of each type can be swept in the Sweep Manager.

1. Click *Tools – Sweep Manager* from the menu bar to open the *Sweep Manager* panel.



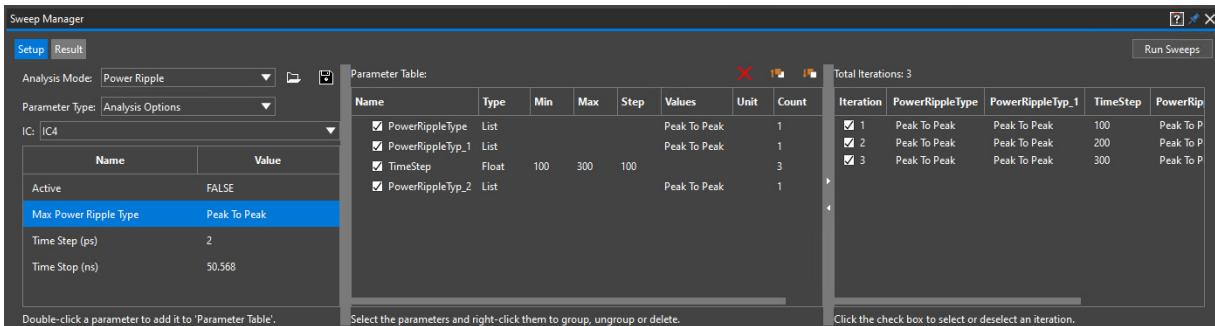
2. Select the required *Sweep Mode* on the Setup tab. You can choose *Power Ripple* or *PDN Impedance*.
3. Select the *Sweep Type*. You can choose *Analysis Options*, *SPICE Models*, or *What-If Decaps*.
  - When *SPICE Models* is selected, the *Model File*, *.Inc*, and *Parameter* options are shown for selection.
  - When *What-If Decaps* is selected, you can sweep the quantity of decaps of each type.
4. Select the IC block for which the sweep parameters need to be set. The list displays names of all IC blocks in the topology.
5. Double-click the parameter that needs to be set. It is moved to the *Parameter Table* pane.

# Topology Workbench User Guide

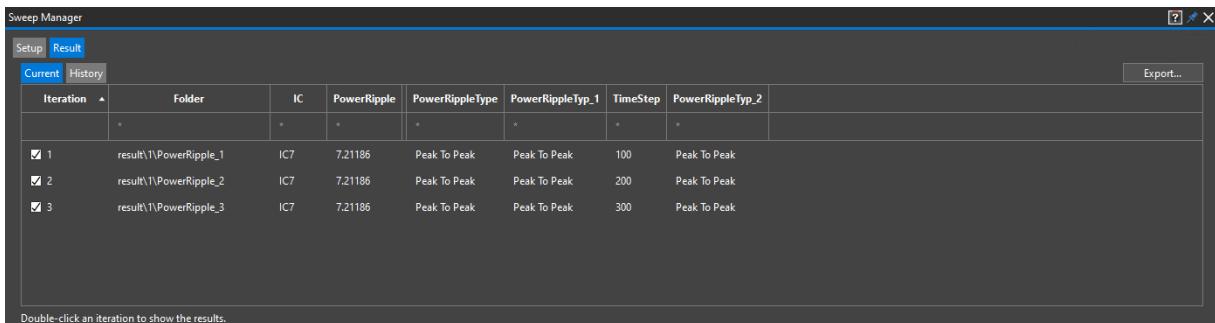
## Using SystemPI Workflow

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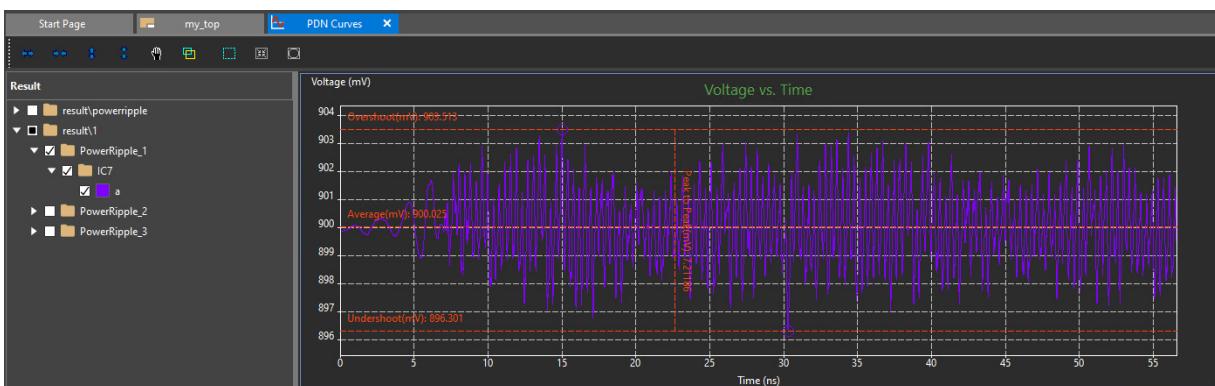
- 6.** Set the required values for the sweep parameters in the *Parameter Table* pane. Based on the specified values, the *Count* is calculated automatically and so are the *Total Iterations*.



- 7.** Click *Run Sweeps*. On successful completion of the sweep simulations, the *Result* tab is displayed.



- 8.** Double-click an iteration to view the results. The *PDN Curves* tab opens in Topology Workbench.



For details, see [Appendix E, “Using the Sweep Manager.”](#)

## Performing DC IR Drop Analysis

In the SystemPI workflow, DC IR Drop Analysis is used together with models extracted with Sigrity PowerDC, and involves connecting together DC models for chip, package, and/or PCB. Sources and sinks are defined, and the DC circuit simulation is performed to determine if the IR drop at critical chip locations meets the chip specifications.

To perform DC IR Drop Analysis:

1. Start Topology Workbench using a method described in the [Starting Topology Workbench](#) topic.

**Note:** When you open Topology Workbench in standalone mode, choose *Advanced PI II* from the *Cadence Product Choices* dialog box to run SystemPI workflow. If you are switching to the SystemPI workflow from another workflow such as SystemPI – Parallel Bus Analysis or Serial Link Analysis, the *Cadence Product Choices* dialog box is displayed again with the relevant choices for selection.

2. Create a topology project for PDN impedance.

For steps, refer to the [Creating a Topology Project from Scratch](#) section or the [Opening an Existing Topology Project](#) section.

When you create a new topology project,

- a. Specify a *Topology Name* and browse the *Topology Path* to save your topology.
- b. Click the *SystemPI* tab.
- c. Select *DC IR Drop Analysis* from the *Workflow* list box. This type of analysis is selected by default. A list of the default workflow-specific templates is displayed along with the *<blank topology>* row to start designing your own topology from scratch. Currently, only *simple\_dc\_template* is available.

The Topology Workbench window is refreshed as following:

- A tab with the given *Topology Name* opens next to the [Start Page](#).
- The [Layout Canvas](#) is populated with the blocks as per the selected default template. If you chose to create a *<blank topology>*, the canvas is empty.
- The [Workflow Panel](#) opens with a list of tasks you need to perform during the selected type of analysis.
- The [Floating Toolbar](#) opens with a list of various types of blocks that can be used in the selected type of analysis.

3. Add and place the required blocks on the canvas.

## Topology Workbench User Guide

### Using SystemPI Workflow

For information, see [Adding Blocks to the Canvas](#) and [Appendix A, “Choosing Blocks to Place on the Canvas.”](#)

4. Connect the blocks on the canvas and configure the connections between their signals.

For information, see [Connecting the Blocks on the Canvas](#) and [Managing Connections Between Blocks and Signals](#).

5. Edit and configure the properties of the various components placed on the canvas by using the [Edit Properties Panel](#). You can also assign device models to the controller and memory devices in the displayed panel.

For information, see [Editing the Properties of a Component](#).

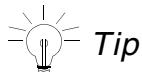
6. Setup and manage the component model libraries.

For information, see [Setting Up Component Model](#).

7. Click *Terminate Unconnected Pins* in the *Topology Setup* schema to end the impedance of any unconnected pins in the topology.

For information, see [Terminating Unconnected Pins](#).

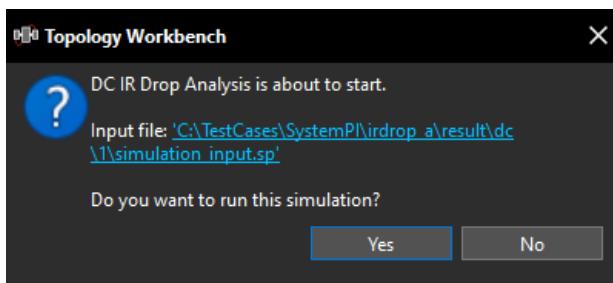
8. Click *Save Topology* in the *Topology Setup* schema.



*Tip*

Alternatively, you can save a topology by clicking in the [Toolbar](#) or choosing *Topology – Save* from the [Menu Bar](#).

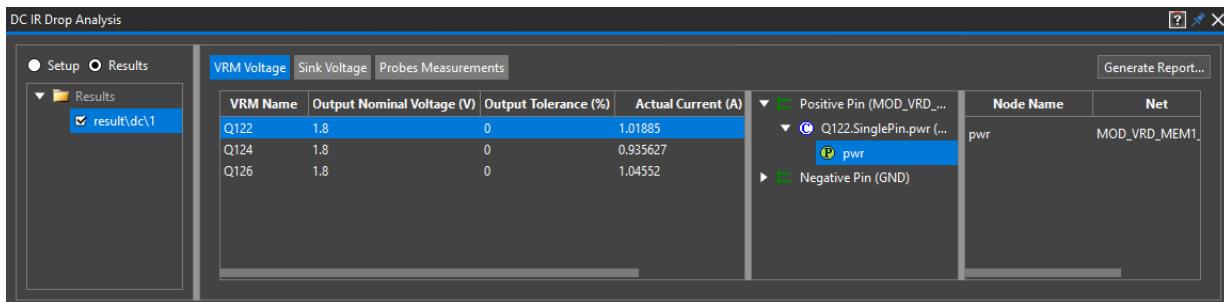
9. Click *Set Analysis Options* in the *Simulation Setup* schema to open the *Analysis Options* panel. For more information, see [Configuring Simulation Options for SystemPI Workflows](#).
10. Click *Set DC IR Drop Analysis* in the *Simulation Setup* schema to open the *DC IR Drop Analysis* panel. For procedural details, see [Configuring DC IR Drop Analysis](#).
11. Click *Start DC IR Drop Analysis* in the *Simulation Setup* schema. A message box seeks your confirmation to start the simulation.



## Topology Workbench User Guide

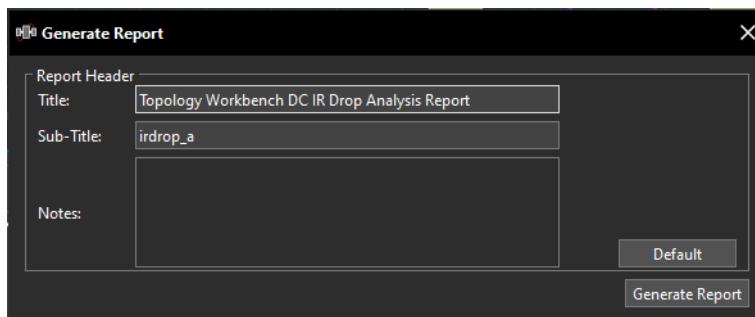
### Using SystemPI Workflow

12. Click Yes. The simulation starts to run and on completion of the process, the *DC IR Drop Analysis* panel opens with the *Results* option selected.



**Note:** You can also set up the VRMs, sinks, and probes for DC IR Drop Analysis. To do so, select the Setup option in the *DC IR Drop Analysis* panel.

13. Click *Generate Report*. A dialog box opens to specify custom information, such as, *Title*, *Sub-Title*, and *Notes*.



14. Click the *Generate Report* button given in the dialog box. The HTML report is displayed in a new tab.

For additional features available in the workflow, see [Related Topics](#) below.

#### **Related Topics**

- [Configuring the Blocks for SystemPI Workflows](#)
- [Configuring DC IR Drop Analysis](#)
- [Viewing Simulation Results](#)
- [Browsing Simulation Results](#)
- [Setting Up Component Model](#)
- [Switching to Another Workflow](#)

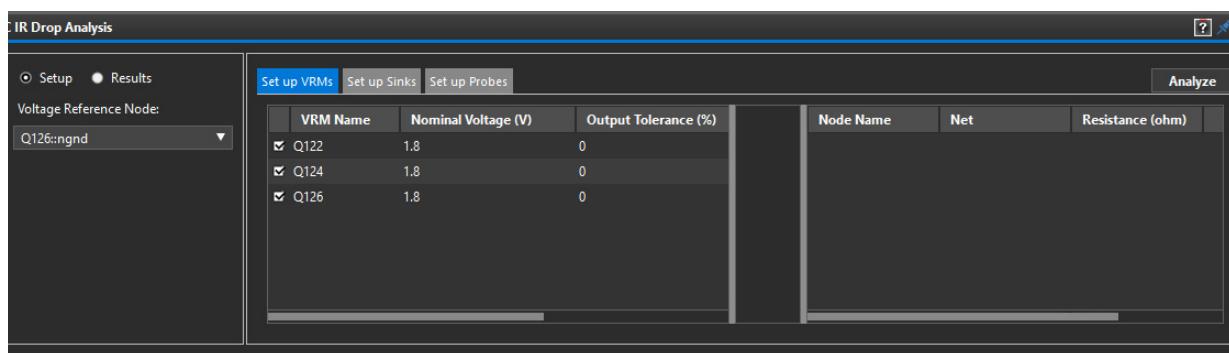
# Topology Workbench User Guide

## Using SystemPI Workflow

- [Customizing a Workflow](#)
- [Creating Custom Templates](#)
- [Archiving a Topology](#)

## Configuring DC IR Drop Analysis

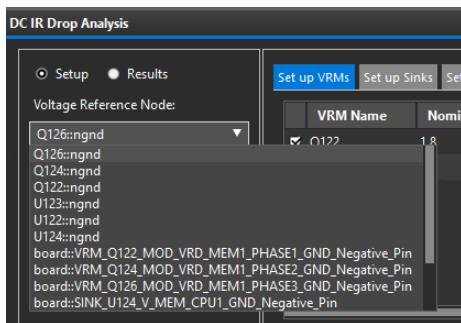
1. Click *Set DC IR Drop Analysis* in the *Simulation Setup* schema. The *DC IR Drop Analysis* panel opens as shown below.



You can configure the *Setup* and *Results* in the displayed panel. The *Setup* option is selected by default and the related settings are available for update on dedicated tabs for each type of block in the topology.

**Note:** Let the *Setup* option remain selected for the steps discussed after this point.

2. Select the required *Voltage Reference Node* from the list.

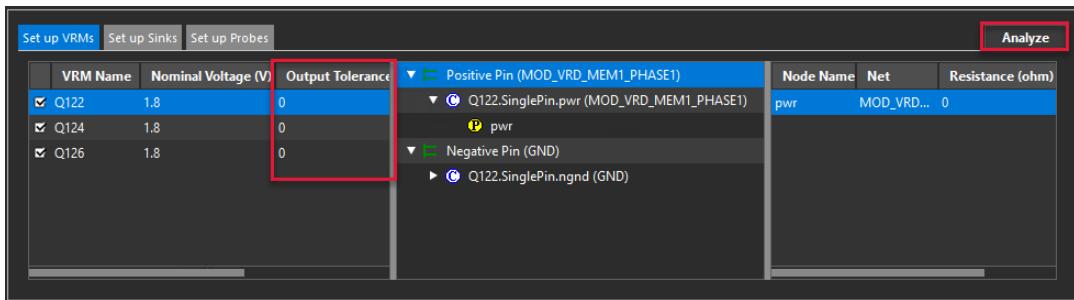


The tables in the right pane are populated accordingly. The first tab (in this case, *Set up VRMs*) is selected.

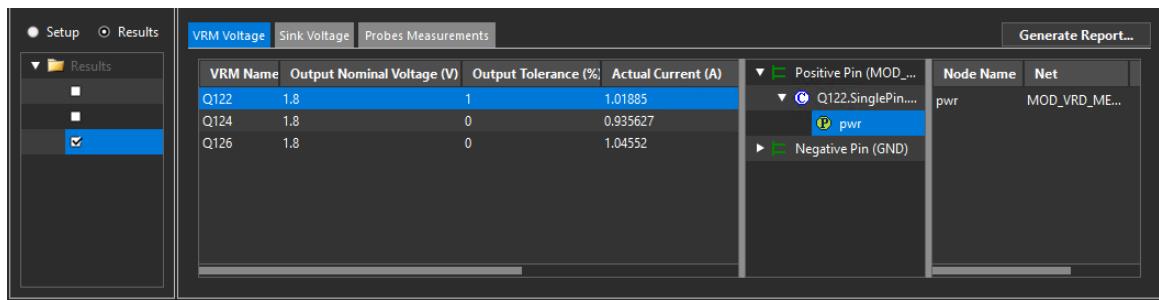
# Topology Workbench User Guide

## Using SystemPI Workflow

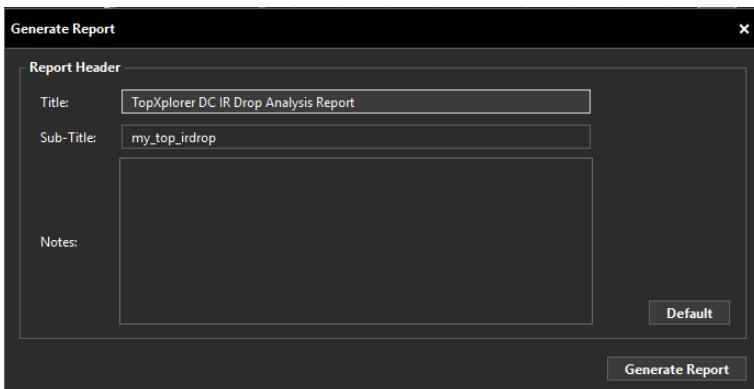
3. Select a row in the *Set up VRMs* tab.



4. Edit the *Output Tolerance (%)* value for the required VRM blocks.
5. Click *Analyze*. The *Results* are displayed after background processing. The tabs and content therein changes to *VRM Voltage*, *Sink Voltage*, and *Probes Measurements*.



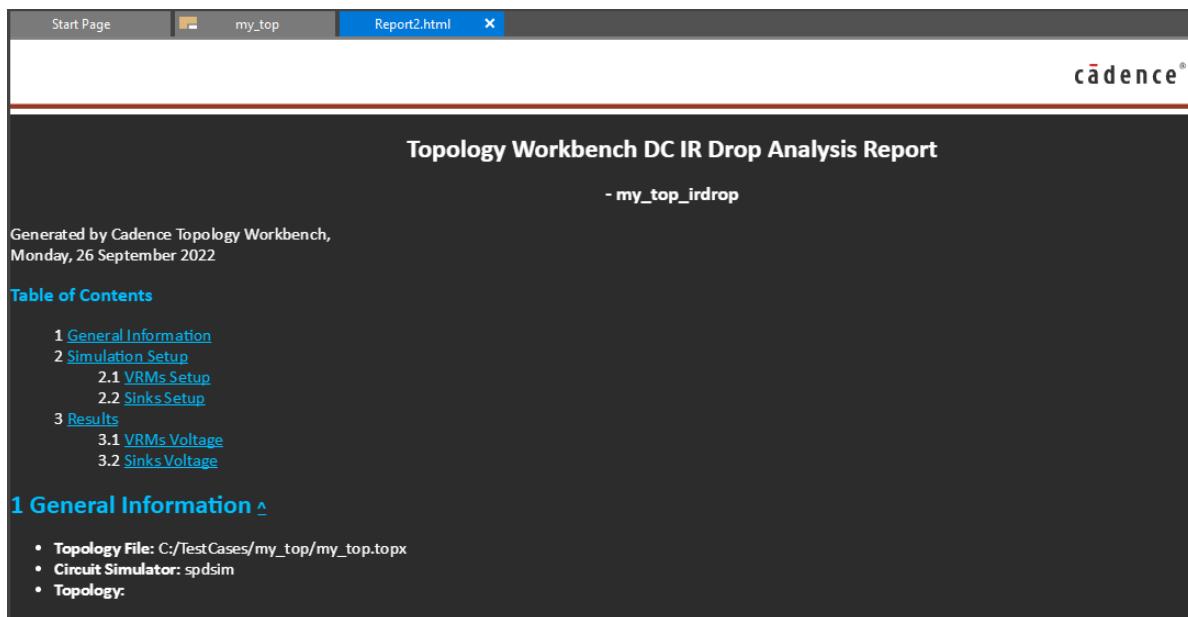
6. Similarly, repeat the set up on other tabs as per requirement.
7. Click *Generate Report* and specify custom information for the *Report Header* in the displayed dialog box. The default *Title* and *Sub-Title* given in the dialog box can be edited.



## Topology Workbench User Guide

### Using SystemPI Workflow

8. Click *Generate Report* given in the dialog box. A *Report#.html* tab opens with the analysis report printed neatly under headings such as *General Information*, *Simulation Setup*, and *Results*.



## Configuring the Blocks for SystemPI Workflows

For all SystemPI workflows, you can:

- Instantiate the required types of blocks on the canvas and connect them to form a wired topology. The blocks can be chosen from the Floating Toolbar.  
See Appendix A, “Choosing Blocks to Place on the Canvas.” for the complete range of blocks that can be used in PBA workflow.
- Edit the properties of a block in the *Component Properties* tab ( ) of the Edit Properties Panel as described in the Editing the Properties of a Component section.

To know more about configuring a few commonly used blocks in PBA workflow, see:

- S Parameter Block
- Subcircuit Block
- VRM Block
- Discrete Block

- [Via Block](#)
- [Sink Block](#)

## S Parameter Block

The S Parameter models describe the input-output relation between the ports (or terminals) in a block. Such models can be assigned to the *SnP* (S Parameter) blocks, which can be added to the topology from the floating toolbar.

For information about how to configure an S Parameter block, see [Assigning and Extracting S Parameter Files in Chapter 2, “Working with Topologies.”](#)

## Subcircuit Block

A *subckt* (subcircuit) block is a general purpose block that can contain an arbitrary SPICE subcircuit.

**Note:** You can set up the default pin locations for a SPICE subcircuit the same way as you can for an S Parameter block. For more information, see [Setting Up the Default Pin Location in Chapter 2, “Working with Topologies.”](#)

In the *Component Properties* tab of the *Edit Properties* panel for a subcircuit block, you can:

1. Assign a *Circuit File* of \*.sp or \*.ckt format.
  - a. Click *E* that is displayed when the pointer is placed in the cell adjacent to *Circuit File*. Alternatively, click *Load Circuit File*.
  - b. Browse and select the required file from the displayed dialog box.
  - c. Select the *Subcircuit* from the list that is populated based on the specified circuit file.
  - d. Click *View Subcircuit* to open the *Subcircuit Editor*. You can edit the subcircuit definition in this editor and then click *OK* to save the changes.

If you assign a circuit file (\*.ckt) of Touchstone or a more-compact Cadence Broadband Network Parameter (BNP) format, you can use the subcircuit block to create a PCB block. In this scenario, you can:

1. Assign a *Circuit File* of \*.ckt format.
2. Select or deselect the check box to *Remove DC Blocking Components*.

3. Select or deselect the check box to *Enforce Passivity*. When selected, passivity checks are run for the input S-element and passivity enforcement process is performed if passivity violations exist.
4. Select or deselect the check box to enable or disable *Layout Extraction*. For details, see [Appendix D, “Using Extracted Interconnect Models from Layout.”](#)
5. Click the *View S Parameter* button to view the waveforms for the *Network Parameters* in the *BNP Viewer* window.

## VRM Block

In the SystemPI workflow, you can parameterize the corner voltages of a Voltage Regulator Module (VRM) component including, Min, Typ, and Max VRM voltages, for fast, consistent simulation of the IBIS corner models.

In the *Component Properties* tab of the *Edit Properties* panel for a VRM block, you can:

1. Configure the associated *Power Net*.
  - a.Specify the *Net Name*.
  - b.Enter the (number) *# of Pins*.
  - c.Specify the *Pin Name* and *Pin Resistance*.
2. Configure the associated *Ground Net*.
  - a.Specify the *Net Name*.
  - b.Enter the (number) *# of Pins*.
  - c.Specify the *Pin Name* and *Pin Resistance*.

**Note:** In the extracted use models having VRM blocks, the connections of the VRM blocks are hidden by default. If you need to run non-ideal simulation for such use models, then before starting the simulation, right-click the canvas and click the *Display Unconnected Power Pin* option from the displayed shortcut menu.

## Discrete Block

By default, a discrete block represents a resistor. You can modify the block properties to represent other discrete components, such as capacitors and inductors.

# Topology Workbench User Guide

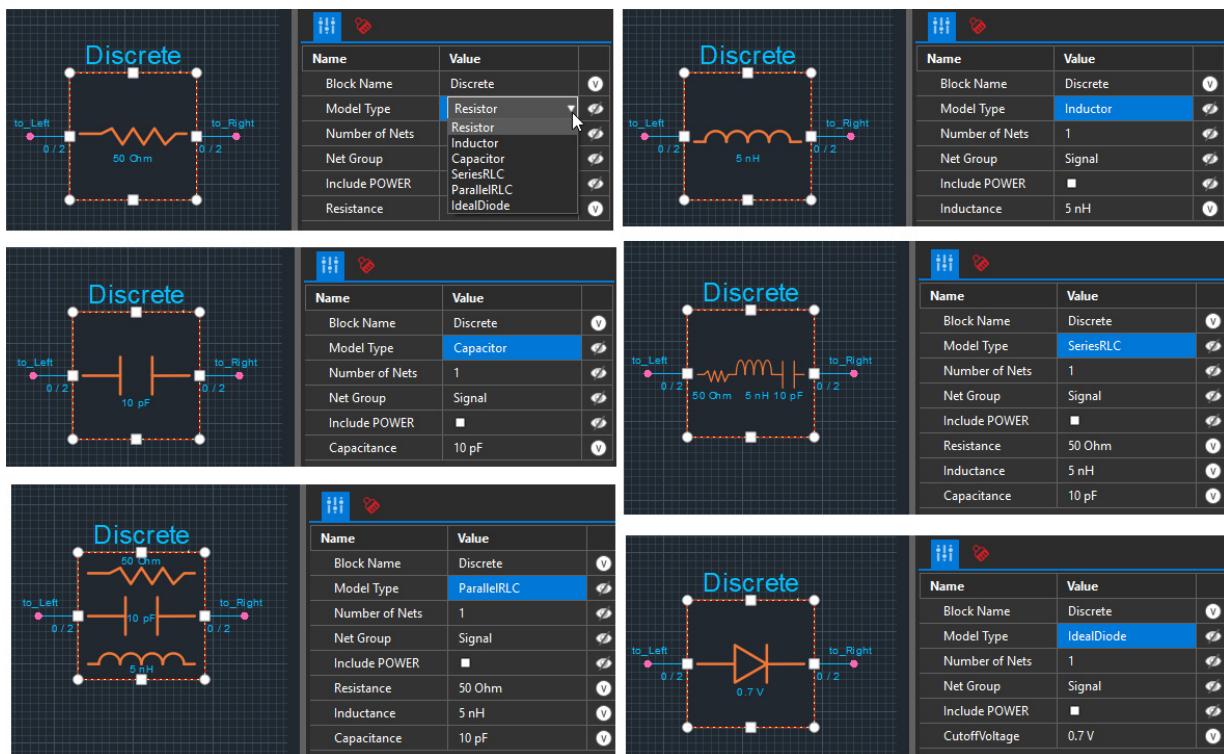
## Using SystemPI Workflow

After adding the block, in the *Component Properties* tab of the *Edit Properties* panel for a discrete block, you can:

1. Select the *Model Type* of the discrete block.

By default, the *Model Type* is set to *Resistor*. The other available options for choice are *Inductor*, *Capacitor*, *SeriesRLC*, *ParallelRC*, and *IdealDiode*.

As you change the selection in the *Model Type* list, the symbol within the discrete block placed on the canvas and the associated fields within the *Edit Properties* panel change, as shown below.



2. Modify the *Number of Nets* if you want more than one instance of the discrete model type to be included in the discrete block model. Else, by default, only one instance is

included. The corresponding changes that are made in subcircuit definition can be viewed in the *Subcircuit Editor* as shown below.

Properties Panel View		Subcircuit Editor View								
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Block Name</td> <td style="width: 85%;">Discrete</td> </tr> <tr> <td>Model Type</td> <td>IdealDiode</td> </tr> <tr> <td>Number of Nets</td> <td>1</td> </tr> <tr> <td>Net Group</td> <td>Signal</td> </tr> </table>	Block Name	Discrete	Model Type	IdealDiode	Number of Nets	1	Net Group	Signal	<pre style="font-family: monospace; background-color: #f0f0f0; padding: 5px;">** Signal * For a X_a a1 a2 one_IdealDiode IS='IS'  .MODEL IdealDiode D IS='IS'  .subckt one_IdealDiode in out d1 in out IdealDiode .ends one_IdealDiode</pre>	<p>Single instance of IdealDiode in the block model.</p>
Block Name	Discrete									
Model Type	IdealDiode									
Number of Nets	1									
Net Group	Signal									
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Block Name</td> <td style="width: 85%;">Discrete</td> </tr> <tr> <td>Model Type</td> <td>IdealDiode</td> </tr> <tr> <td>Number of Nets</td> <td>3</td> </tr> <tr> <td>Net Group</td> <td>Signal</td> </tr> </table>	Block Name	Discrete	Model Type	IdealDiode	Number of Nets	3	Net Group	Signal	<pre style="font-family: monospace; background-color: #f0f0f0; padding: 5px;">** Signals * For a X_a a1 a2 one_IdealDiode IS='IS'  * For b X_b b1 b2 one_IdealDiode IS='IS'  * For c X_c c1 c2 one_IdealDiode IS='IS'  .MODEL IdealDiode D IS='IS'  .subckt one_IdealDiode in out d1 in out IdealDiode .ends one_IdealDiode</pre>	<p>Three instances of IdealDiode in the block model.</p>
Block Name	Discrete									
Model Type	IdealDiode									
Number of Nets	3									
Net Group	Signal									

3. Select the *Net Group* from the list as *Signal* or *Power*.
4. Select the *Include POWER* check box to include non-ideal power effects during simulations.
5. Specify values greater than zero for resistance, inductance, and capacitance. All or one of these values is required based on the *Model Type* you select. Suffixes *m*, *u*, *n*, and *p* can be used to indicate milli( $10^{-3}$ ), micro( $10^{-6}$ ), nano( $10^{-9}$ ), and pico ( $10^{-12}$ ), respectively. For *IdealDiode* model type, you need to specify the cut-off voltage (*CutoffVoltage*).

## Via Block

A Via block is used for vertical layer transitions that are represented by SPICE subcircuits or S-parameters. In the *Component Properties* tab of the *Edit Properties* panel for a Via block, you can:

1. Assign a SPICE *Circuit File* of \*.sp or \*.ckt format.
  - a. Click *E* that is displayed when the pointer is placed in the cell adjacent to *Circuit File*.

- b.** Browse and select the required file from the displayed dialog box.
- 2.** Select the *Subcircuit* from the list that is populated based on the specified circuit file.
- 3.** Click *View Subcircuit* to open the *Subcircuit Editor*. You can edit the subcircuit definition in this editor and then click *OK* to save the changes.

For detailed information, refer to [Appendix B, “Using the Via Wizard.”](#)

## Sink Block

A Sink block is used to designate a consumer of power for IR drop analysis. In the *Component Properties* tab of the *Edit Properties* panel for a Sink block, you can:

- 1.** Define the *Current*.
- 2.** Configure the associated *Power Net*.
  - a.** Specify the *Net Name*.
  - b.** Enter the (number) *# of Pins*.
  - c.** Specify the *Pin Name*. The *Pin Current* is set to *on-the-fly*.
- 3.** Configure the associated *Ground Net*.
  - a.** Specify the *Net Name*.
  - b.** Enter the (number) *# of Pins*.
  - c.** Specify the *Pin Name*. The *Pin Current* is set to *on-the-fly*.
- 4.** Click *View Subcircuit* to open the *Subcircuit Editor* in read only mode.

# **Topology Workbench User Guide**

## Using SystemPI Workflow

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## Exporting Constraints from a Topology

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In Topology Workbench, you can derive constraint rules for a topology as an Electrical Constraint Set (ECSet), which applies to each net, and then export them to Constraint Manager. These constraint rules can be back-annotated to design tools, such as, Allegro, to derive the physical layout.

### ***Related Topics***

- [Introduction to Electrical Constraint Sets](#)
- [Setting Constraints in Topology Workbench](#)
  - [Setting the Wiring Constraint](#)
  - [Setting the Propagation Delay Constraint](#)
  - [Setting the Relative Propagation Delay Constraint](#)
  - [Setting the Impedance Constraint](#)
  - [Setting the Vias Constraint](#)
  - [Setting the Total Etch Length Constraint](#)
  - [Setting the Switch-Settle Constraint](#)
  - [Setting the Max Parallel Constraint](#)
  - [Setting the DiffPair Constraint](#)
- [Defining the MappingTag Parameter in Topology Workbench](#)

## Introduction to Electrical Constraint Sets

A constraint is a user-defined limit applied to an element in a design. In Topology Workbench, you define topology template constraints. Topology Workbench uses these constraint rules to drive both signal integrity and EMI analysis.

## Topology Workbench User Guide

### Exporting Constraints from a Topology

You can add user-defined constraints to a topology to store other supplementary constraints within a topology to later import into an electrical constraint set (ECSet) using Constraint Manager. You access these values from the design directly by the user or by other software systems.

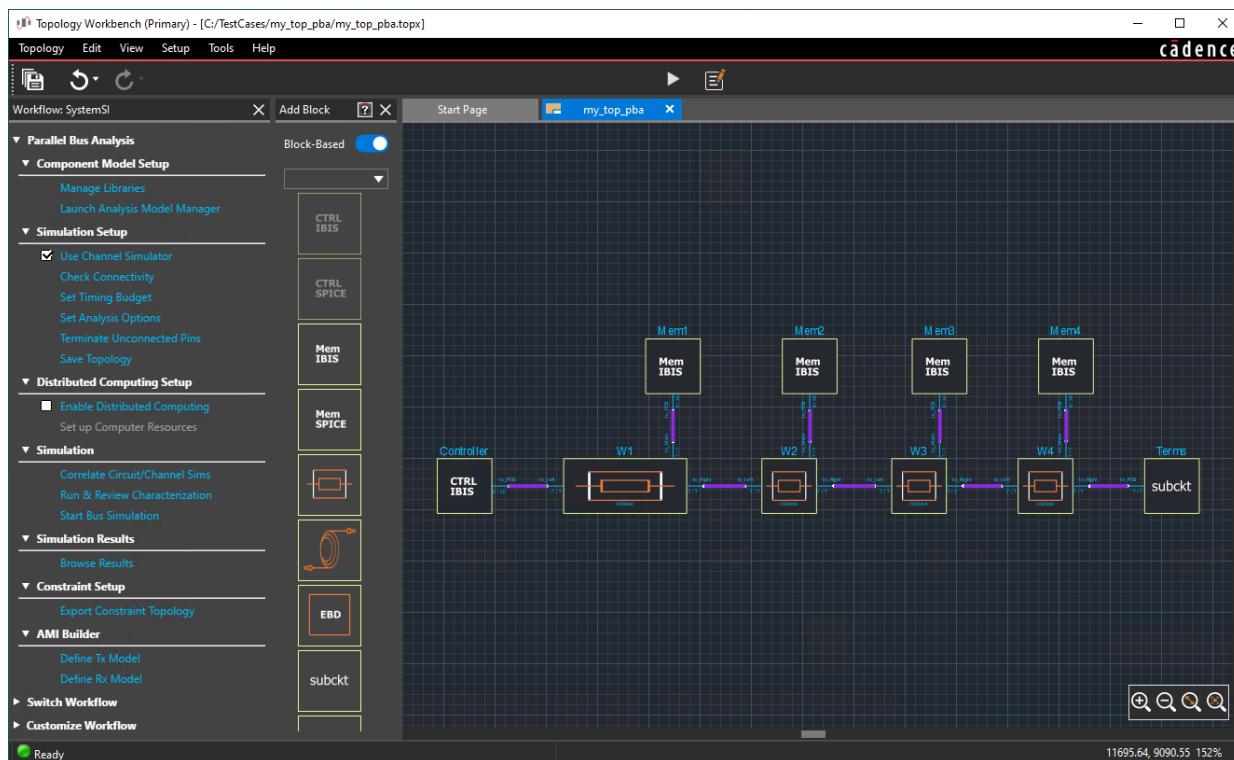
As with all other constraints, any bus, differential pair, Xnet or net of the assigned ECSet inherits user-defined constraints.

For more information on constraints, see the [\*Constraint Manager User Guide\*](#).

## Setting Constraints in Topology Workbench

To define constraints for a topology in Topology Workbench:

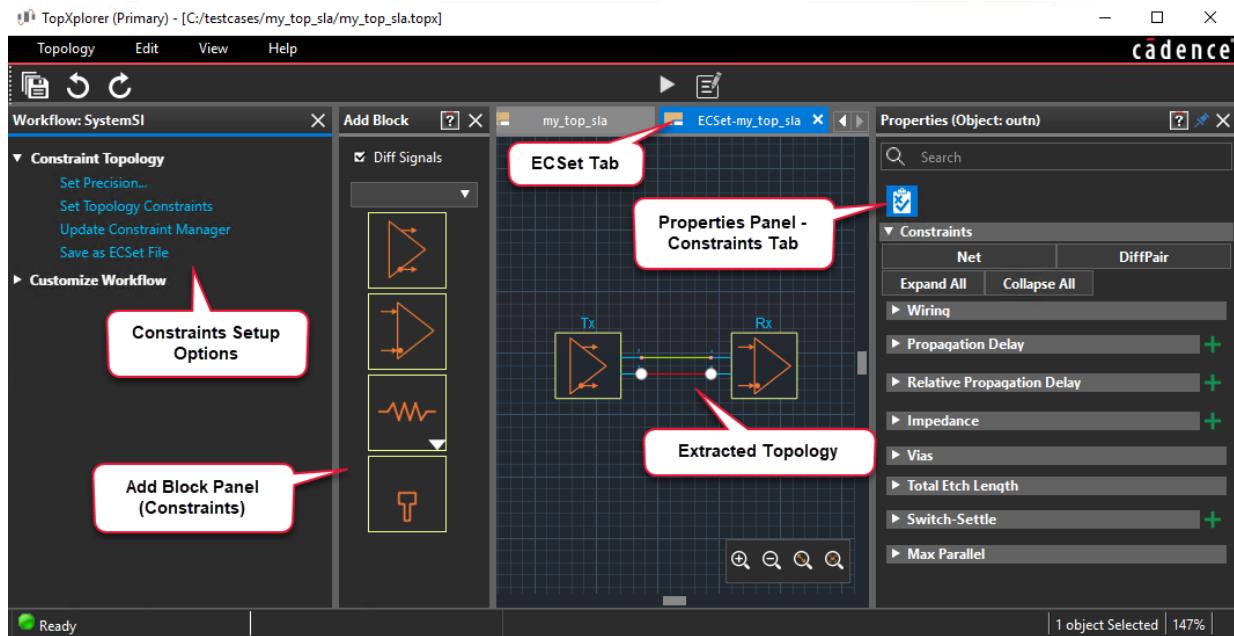
1. Open the topology to view the corresponding [Workflow Panel](#).



## Topology Workbench User Guide

### Exporting Constraints from a Topology

- Click *Export Constraint Topology* from the *Constraint Setup* schema. A new tab with a name of the format *ECSet-<TopologyName>* opens within the Topology Workbench window.

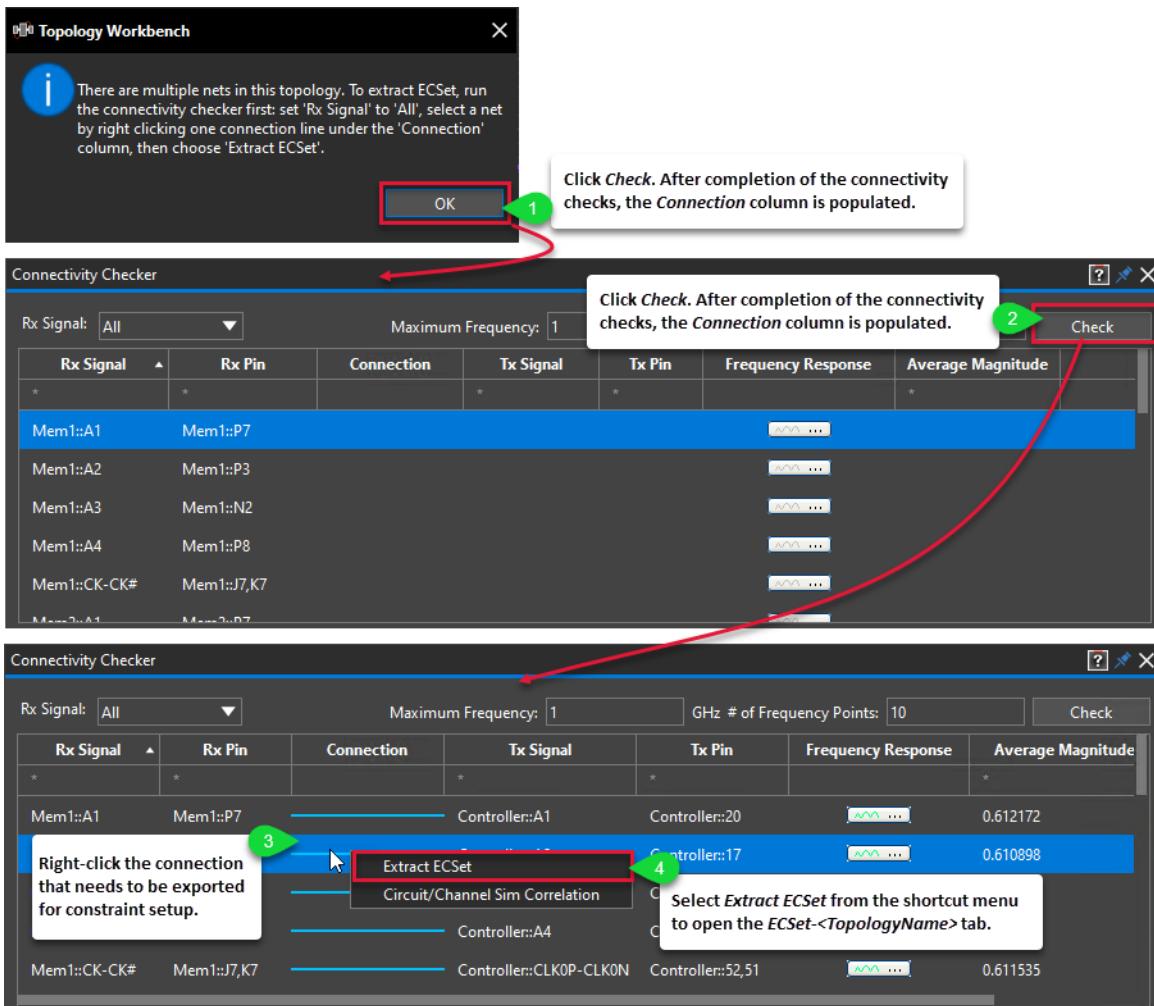


**Note:** If there are multiple nets in your topology, ensure that the *Check Connectivity* step is performed before exporting the constraint topology; otherwise a warning message is displayed. This scenario is essentially required in the Parallel Bus Analysis

# Topology Workbench User Guide

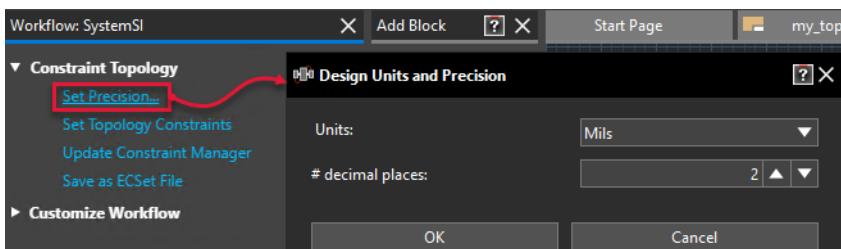
## Exporting Constraints from a Topology

(PBA) workflow.



- Click *Set Precision* in the *Workflow* panel displayed on the *ECSet-<TopologyName>* tab.

The *Design Units and Precision* dialog box opens to let you specify the *Units* and (number) *# of decimal places* to accept for setting the rules. Once done, click *OK* to save the definitions and close the dialog box.



4. Double-click the required connection on the canvas. The *Properties (Object : <Obj\_Name>)* panel opens.

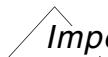
**Note:** When you export a topology from the canvas or a specific connection from the *Connectivity Checker* panel, the *Properties (Object :<Obj\_Name>)* panel is displayed by default. If this panel is already open, selecting the required connection populates the existing values in the schema for each constraint type. If no constraints have been defined yet, the blank fields are displayed for each constraint type.

5. Define the required constraint values in the *Edit Properties* panel. See the [Types of Constraints Available in Topology Workbench](#) below.

In modern bus design, it is common to have buses that have a similar purpose, yet have a slight difference in the number of pins in each net in the bus. Topology mapping mandates that the number of pins in a topology exactly match the number of pins in a net or Xnet. To relax this restriction, you can designate one or more pins in the topology as optional. In this way, the topology can successfully map to a net or an Xnet that may not have the same number of pins. To mark the pins on a selected component as optional, right-click the required block and click *Optional Pins* from the displayed shortcut menu. Alternatively, select a block in the schematic and run the `topxp::setOptionalPins` Tcl command in the Command Window panel.

**Note:** You cannot make vias, T-lines, T-points, traces, and termination networks optional.

6. Click *Update Constraint Manager* in the *Workflow* panel to write the modified constraint values back to the design database (Constraint Manager).

 **Important**

The *Update Constraint Manager* option works **only** when Topology Workbench is started from Allegro or Constraint Manager; otherwise, it does not work.

7. Click *Save as ECSet File* to save the defined constraints for reusing and applying to other components.

## Types of Constraints Available in Topology Workbench

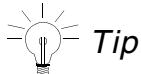
The *Edit Properties* panel provides you the options to define the following types of constraints:

<b>Net</b>	
<i>Wiring</i>	Defines topology scheduling parameters, physical ( <i>Stub Length</i> ) and electromagnetic interference (EMI) ( <i>Max Exposed Length</i> ) rules.  For more information, see <a href="#">Setting the Wiring Constraint</a> .
<i>Propagation Delay</i>	Defines the minimum and maximum delay in time or connection length restriction between any two pins on a net or between any pin and a T-point.  For more information, see <a href="#">Setting the Propagation Delay Constraint</a> .
<i>Relative Propagation Delay</i>	Defines connections that are part of a match group. You can specify relative propagation delays between nets and within a net, as well.  For more information, see <a href="#">Setting the Relative Propagation Delay Constraint</a> .
<i>Impedance</i>	Defines the baseline impedance value and allowable tolerance value above and below the baseline. An impedance constraint compares to the impedance of each cline segment of an extended net.  For more information, see <a href="#">Setting the Impedance Constraint</a> .
<i>Vias</i>	Defines the physical constraint <i>Max Via Count</i> .  For more information, see <a href="#">Setting the Vias Constraint</a> .
<i>Total Etch Length</i>	Defines the physical constraints <i>Minimum Etch Length</i> and <i>Maximum Etch Length</i> .  For more information, see <a href="#">Setting the Total Etch Length Constraint</a> .
<i>Switch-Settle</i>	Defines the switch and settle delay constraints between any driver - receiver pin pair. The current rules and a list of pins appear, as currently defined.  For more information, see <a href="#">Setting the Switch-Settle Constraint</a> .

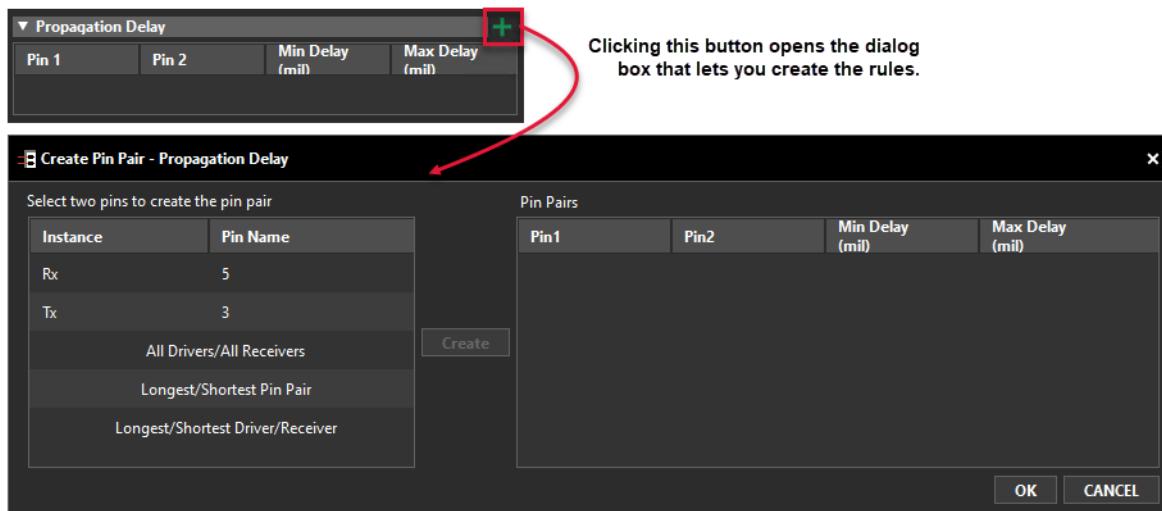
## Topology Workbench User Guide

### Exporting Constraints from a Topology

<b>Max Parallel</b>	Defines the maximum parallelism constraint between nets. This constraint shows the current coupled length and distance gap rules of the current template.  For more information, see <a href="#">Setting the Max Parallel Constraint</a> .
<b>DiffPair</b> (displayed when there are differential signals)	Assigns differential pair rules to differential pair objects in a board design. As a differential topology can contain two separate Xnets, Topology Workbench does not allow a single Xnet constraint definition between pins on different Xnets.  You can set the following rules for a DiffPair constraint:  <i>Members</i>  <i>DiffPair Constraint</i>  <i>Dynamic Phase</i>  <i>Coupling Parameters</i>



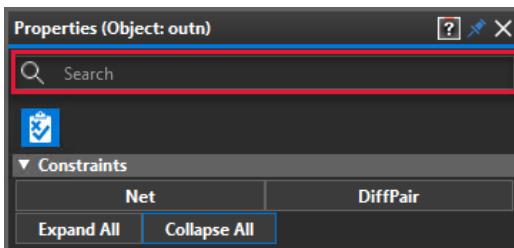
**Tip**  
For *Propagation Delay*, *Relative Propagation Delay*, *Impedance*, and *Switch-Settle* constraints, a button is displayed next to the constraint names. Click this button to open the dialog box where you can create pin pairs and define the constraint values as required.



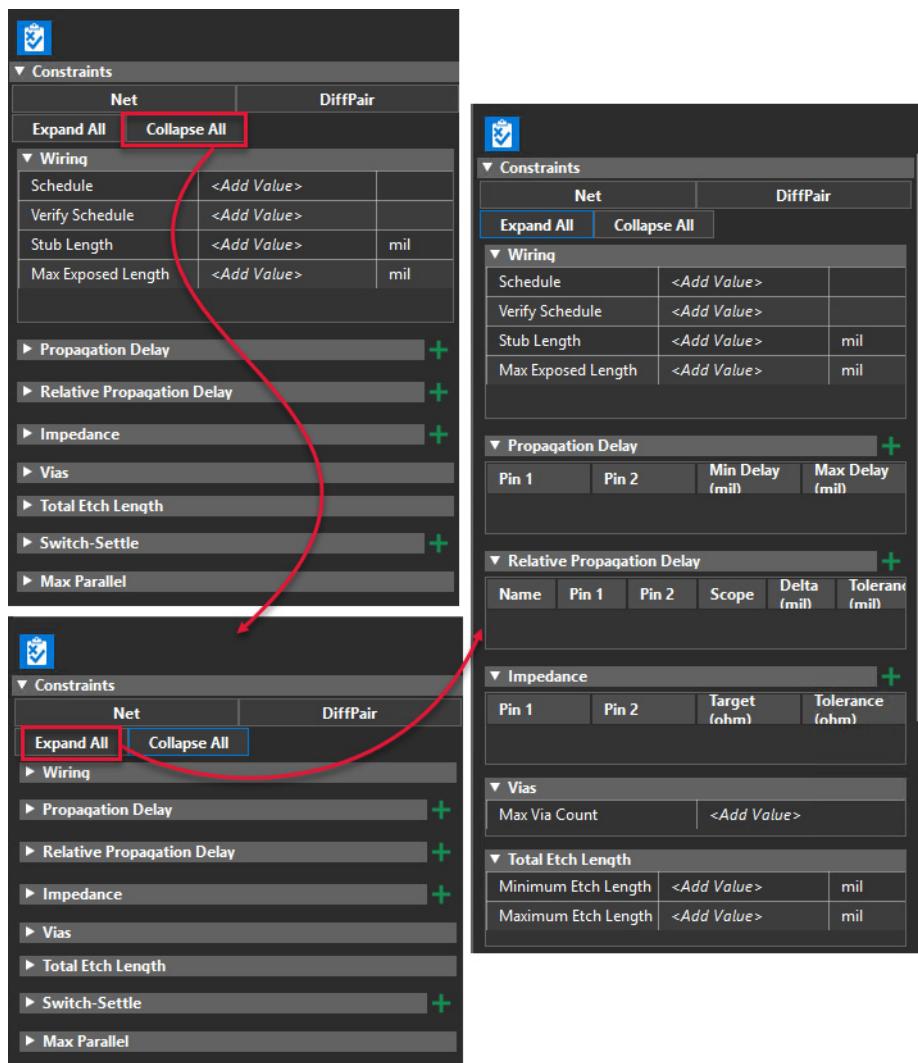
# Topology Workbench User Guide

## Exporting Constraints from a Topology

The *Search* text box in the *Properties (Object :<Obj\_Name>)* panel can be used to look for specific search strings.



Use *Expand All* or *Collapse All* to maximize or minimize all constraint schema with a single click as shown below.



## Setting the Wiring Constraint

Use the *Wiring* schema in the *Properties (Object :<Obj\_Name>)* panel to create and modify topology scheduling parameters and the available physical and EMI rules. These rules apply to the topology as a whole. They are not associated with specific topology elements.

To set a wiring constraint for a connection:

1. Click the *Wiring* schema. A table with the available constraint properties is displayed with editable fields.

▼ Wiring		
Schedule	<Add Value>	
Verify Schedule	<Add Value>	
Stub Length	<Add Value>	mil
Max Exposed Length	<Add Value>	mil

2. Select one of the pre-defined *Schedule* for the ECSet from the list. You have the following options in the list for choice:

- Minimum Spanning Tree*: Connects all of the pins together with minimum connection length. Any pin can connect to any number of other pins. This schedule starts at the primary driver, selects the closest pin to this driver, and connects it through a TLine. The search continues by selecting the next unscheduled pin that is closest to any of the scheduled pins and connecting it with a TLine to the closest scheduled pin. This continues until all pins are scheduled.
- Daisy-chain*: Connects the pins of the topology with minimum connection length, allowing each pin to connect to a maximum of two other pins. This schedule starts with the primary driver, selects the closest pin to this driver, and connects it with a TLine. The closest pin to the last pin scheduled is then selected and connected with a TLine. This continues until all of the pins are scheduled.
- Source-load Daisy-chain*: Connects similar to a daisy chain schedule except that all driver pins are scheduled first, followed by all receiver pins.
- Star*: Connects the driver pins in a daisy-chain pattern, then all of the receiver pins are connected to the last driver pin.
- Far-end Cluster*: Connects similar to a star schedule except that the last driver pin connects to a T-point, to which all of the receivers are connected.
- Template*: Connects according to a user-defined template schedule. You are required to interactively add and connect each T-line to form the custom net schedule.

- Clear*: No specified schedule.
3. Select the *Verify Schedule* value.
- Verify Schedule* is used to enable design rule checks (DRC) if a schedule has been set. Select one of the following from the drop-down list:
- |       |                   |
|-------|-------------------|
| Yes   | Enables DRC.      |
| No    | Disables DRC.     |
| Clear | No specified DRC. |
4. Enter the *Stub Length* for daisy chain routing.
- The daisy chain routing connects the pins of the topology with minimum connection length, allowing each pin to connect to a maximum of two other pins.
5. Enter the *Max Exposed Length*. This constraint property specifies the maximum length of interconnect allowed in a net that is not shielded by plane layers above and below.

▼ Wiring		
Schedule	Daisy-chain	
Verify Schedule	Yes	
Stub Length	10.00	mil
Max Exposed Length	25.00	mil

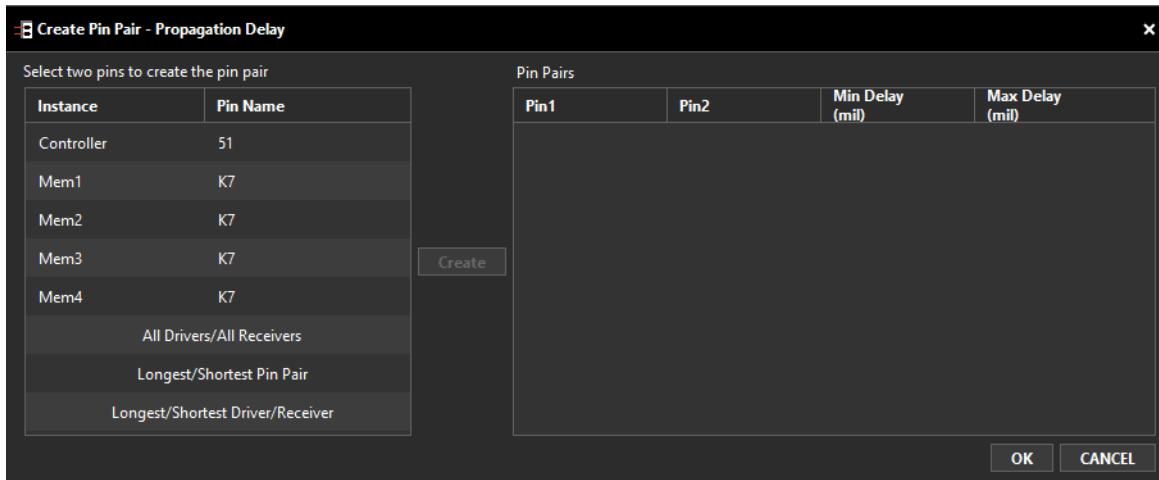
## Setting the Propagation Delay Constraint

With the *Propagation Delay* constraint, you can create and modify delay rules for pin, tee or pin-tee pairs. You can also create delay rules for all drivers and receivers, all driver and receiver pairs, and the longest and shortest Tlines. To set a *Propagation Delay* constraint for a connection, in the *Properties (Object: <Obj\_Name>)* panel:

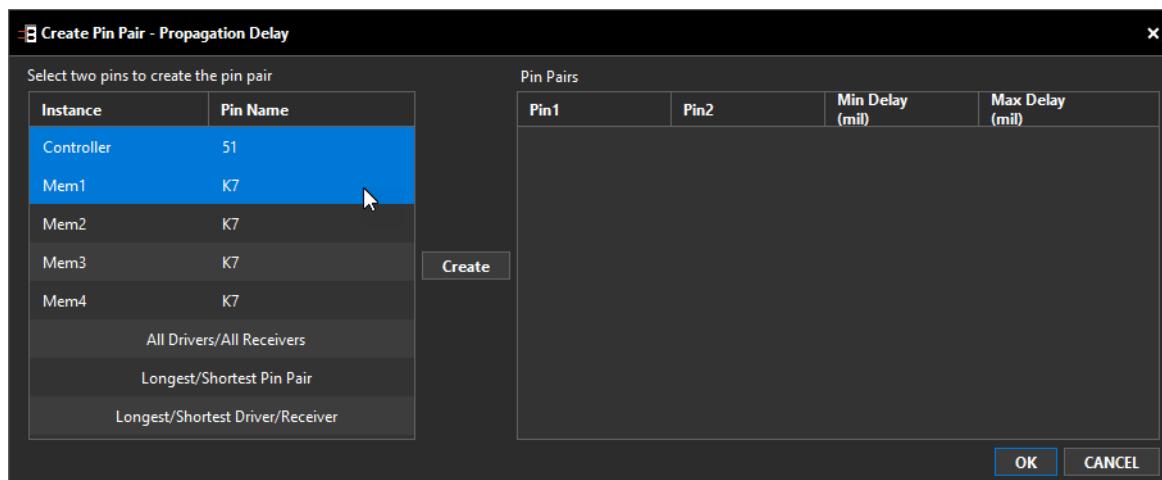
# Topology Workbench User Guide

## Exporting Constraints from a Topology

1. Click the button adjacent to the *Propagation Delay* schema. The *Create Pin Pair - Propagation Delay* dialog box opens as shown below.



2. Select two pins from the list in the left pane while keeping the `Ctrl` key pressed. The *Create* button is enabled as shown below.

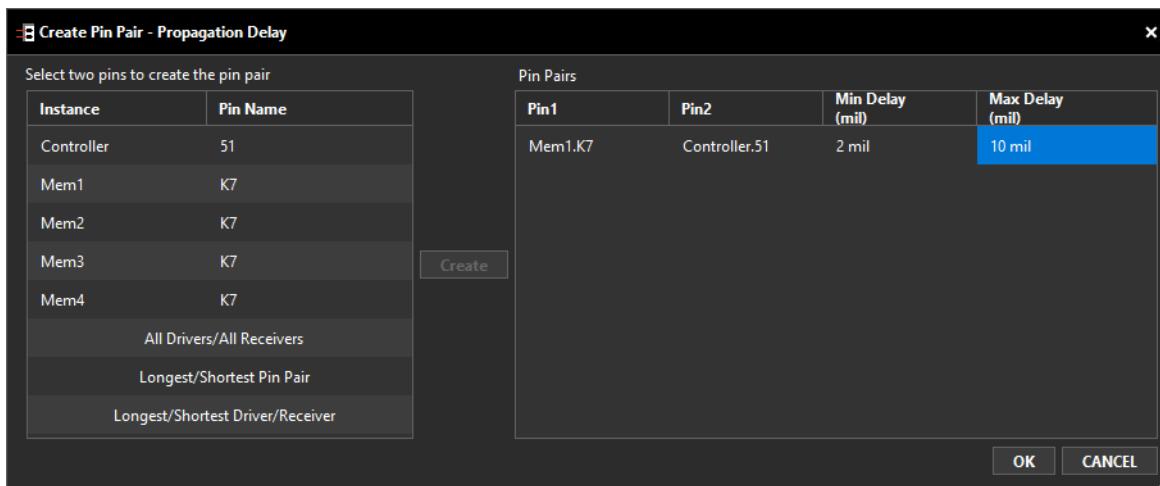


3. Click *Create*. A row of the selected pin pair is added to the *Pin Pairs* pane on right.

## Topology Workbench User Guide

### Exporting Constraints from a Topology

4. Add the *Min Delay* and *Max Delay* values in the corresponding cells of the table.

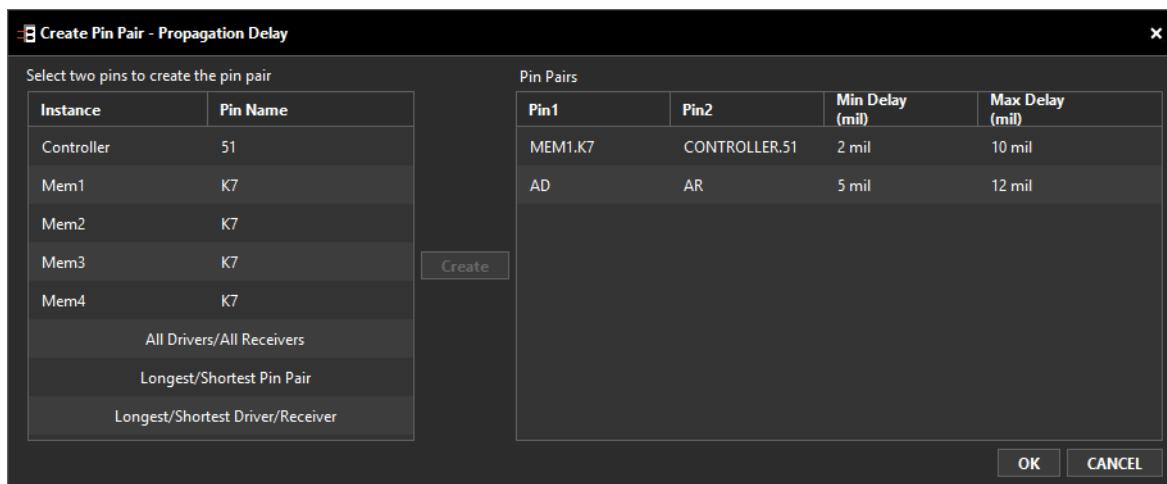


5. Create one of the following global constraints:

- All Drivers/All Receivers*
- Longest/Shortest Pin Pair*
- Longest/Shortest Driver/Receiver*

**Note:** When you click either of these global constraints in the left pane, the *Create* button is enabled provided you have not already set another global constraint.

6. Define the *Min Delay* and *Max Delay* for the global constraint in the *Pin Pairs* table.



## Topology Workbench User Guide

### Exporting Constraints from a Topology

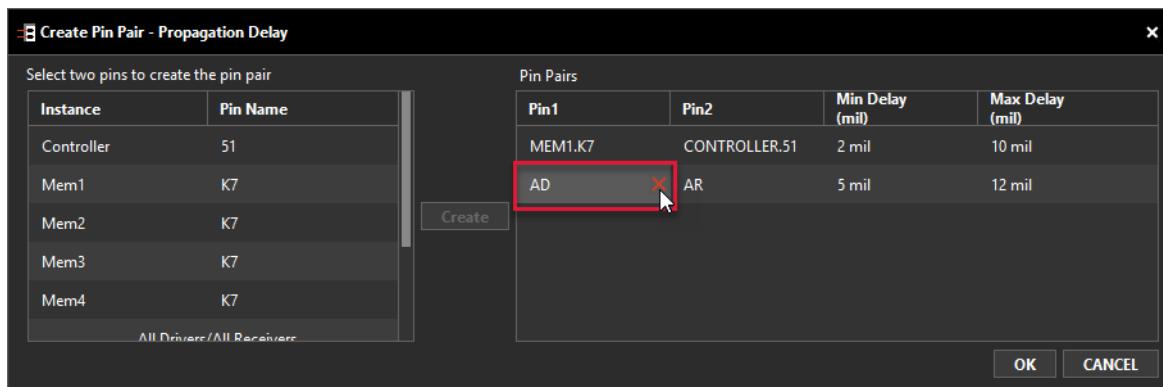
7. Click **OK** to save the changes you have made and close the dialog box. The table in the *Propagation Delay* schema is refreshed with the newly set or updated constraint values.

▼ Propagation Delay			
Pin 1	Pin 2	Min Delay (mil)	Max Delay (mil)
MEM1.K7	CONTRO...	2	10
AD	AR	5	12

## Deleting a Propagation Delay Constraint

If you want to remove a defined constraint:

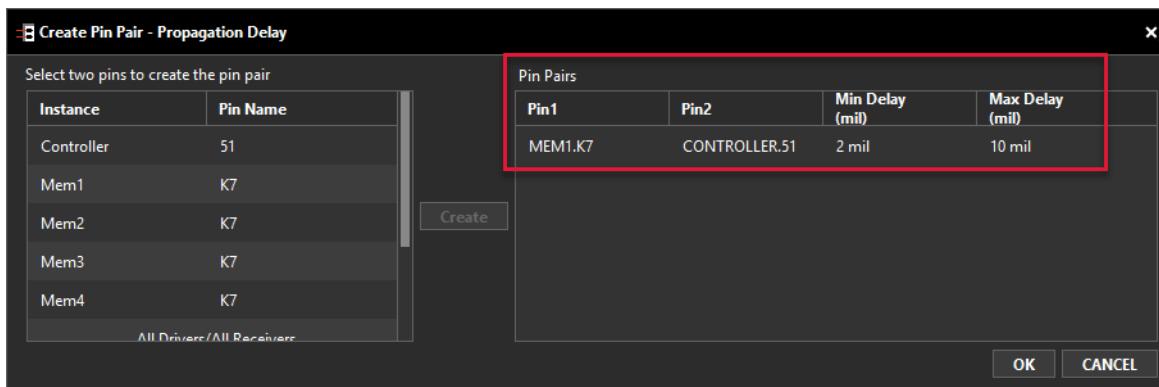
1. Click the  button adjacent to the *Propagation Delay* schema to open the *Create Pin Pair - Propagation Delay* dialog box.
2. Under the *Pin1* or *Pin2* column, place the pointer on a cell that represents the constraint you want to delete. A cross (X) symbol is displayed as shown below.



## Topology Workbench User Guide

### Exporting Constraints from a Topology

- Click the cross (*X*) to delete the constraint. The *Pin Pairs* table is refreshed.



- Click *OK* to save the change and close the dialog box. The table in the *Propagation Delay* schema is refreshed accordingly as shown below.

▼ Propagation Delay			
Pin 1	Pin 2	Min Delay (mil)	Max Delay (mil)
MEM1.K7	CONTRO...	2	10

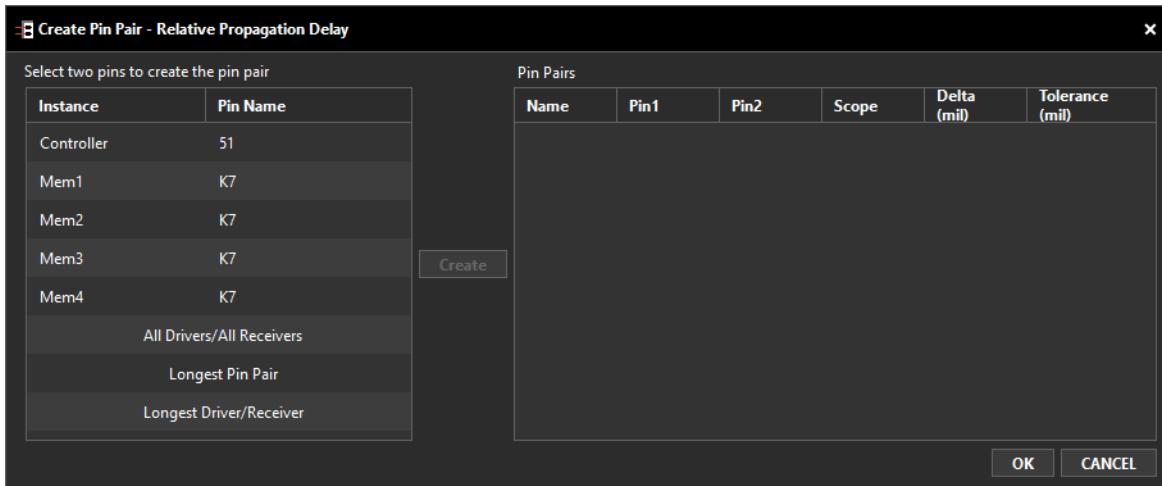
## Setting the Relative Propagation Delay Constraint

Use the *Relative Propagation Delay* constraint to assign matched interconnect delay constraint rules to pin, tee or pin-tee pairs. A matched delay constraint is two or more pin, tee or pin-tee pairs whose interconnect delay must be within a specified tolerance. You can assign matched delay rules to a single pair or to groups of pairs. To set a *Relative Propagation Delay* constraint for a connection, in the *Properties (Object: <Obj\_Name>)* panel:

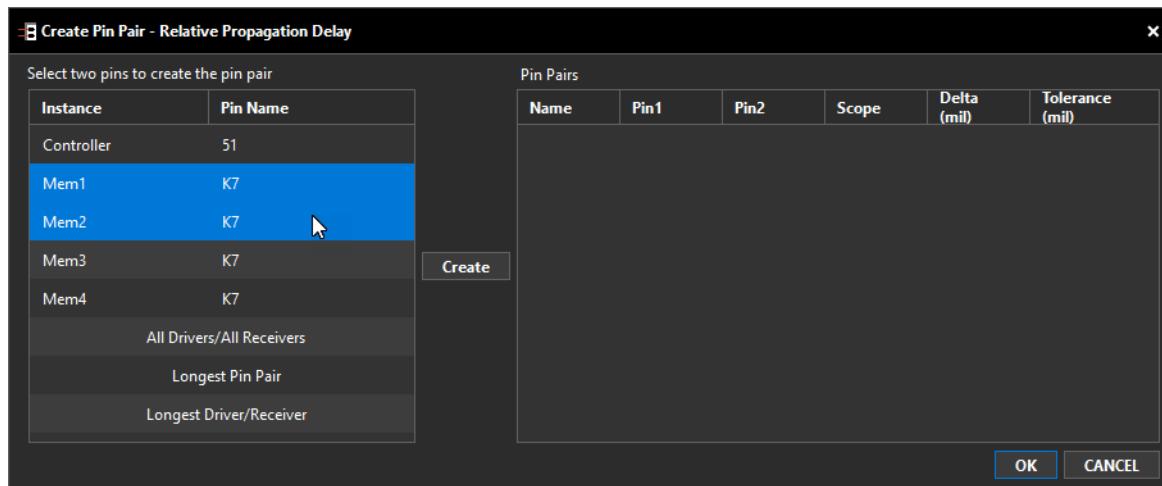
# Topology Workbench User Guide

## Exporting Constraints from a Topology

1. Click the  button adjacent to the *Relative Propagation Delay* schema. The *Create Pin Pair - Relative Propagation Delay* dialog box opens as shown below.



2. Select two pins from the list in the left pane while keeping the `Ctrl` key pressed. The *Create* button is enabled as shown below.



3. Click *Create*. A row of the selected pin pair is added to the *Pin Pairs* pane on right.
4. Modify the default *Name* (reference designators) for pins and T-points in the topology, if required.

**Note:** A default unique name of the format `<topology_name>_M<n>` is automatically assigned to each pin pair.

## Topology Workbench User Guide

### Exporting Constraints from a Topology

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5. Select the *Scope* of the pin pair to control how the members of the Group are validated. You can choose one from the list of following values that are displayed when a cell is clicked under the *Scope* column:

<i>Local</i>	Creates a single match group. Checking is done only between the two pin pairs of each net, and limited to within the net.  <i>Example:</i> Multiple nets with a single driver, two receivers, and a branch point where the length from the driver to each receiver must match, but no matching is needed to other nets.
<i>Global</i>	Creates a single match group, derived from net properties or an electrical constraint set (ECSet). The same match group can exist in multiple ECSets or properties, resulting in all objects ending up in the same match group. For hierarchical designs, use of the Global Scope in lower blocks creates a single merged match group at the top level.  <i>Example:</i> Multiple nets containing pin pairs that must match to each other across each net.
<i>Bus</i>	Creates match groups based on bus names (such as MG1_BUS1, MG1_BUS2, and so on). You can apply a single ECSet to all the nets at either the net or bus level. This group type reduces the number of ECSets required to constrain a design, as opposed to requiring a separate ECSet for each bus. A limitation of this scope type is that no other signals from outside the bus can be added to these match groups.  <i>Example:</i> Multiple nets organized in several buses. Pin pairs must match, but only to nets within the same bus. Typically, all nets share the same topology.

## Topology Workbench User Guide

### Exporting Constraints from a Topology

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**Class** Generates unique match groups for each class. Similar to Bus scope, Class scope also optimizes the number of topologies required to constraint a design. However, no other signal from outside the net class can be added to a match group with Class scope. Class scope has more flexibility than Bus scope because a class can include more signals than a bus, which is typically limited to vectored nets or nets that share a common topology. Unlike the Bus scope, the Class scope adds all the selected members, including bus members, to the match group created by the ECSet (with Class scope).

*Example:* When you need the functionality of a Bus scope and also need additional non-bus members in a match group, use the Class scope.

**Net Group** Generates unique match groups for each net group.

6. Specify the *Delta* value. It defines the allowable propagation delay/length delta for pin, tee or pin-tee pairs of the group. The delta is used to offset the pair(s) from a target pair.
7. Specify the *Tolerance* value for relaxing the relative/match requirements.

The default format for specifying a *Tolerance* is percentage. If you want to define an absolute tolerance, a value with the unit of measurement can be entered. For example, you can enter 0.1ns in the *Tolerance* field.

8. Create one of the following global constraints:

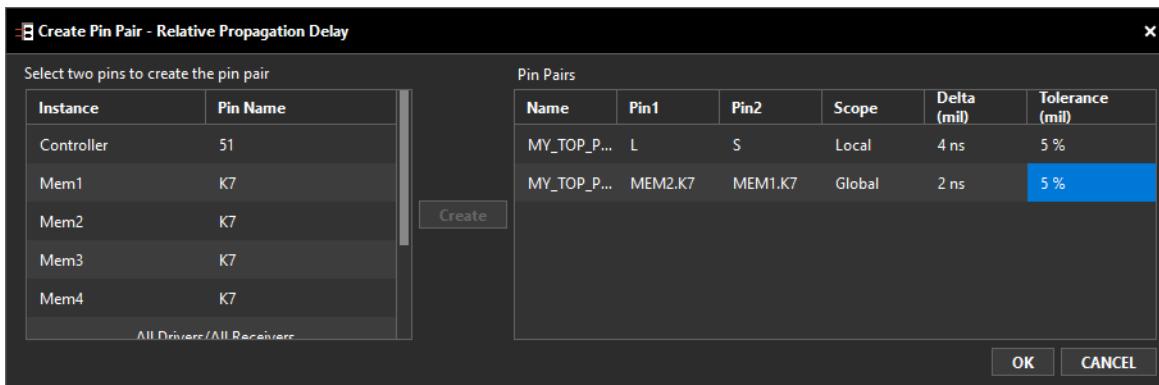
- All Drivers/All Receivers*
- Longest Pin Pair*
- Longest Driver/Receiver*

**Note:** When you click either of these global constraints in the left pane, the *Create* button is enabled provided you have not already set another global constraint.

## Topology Workbench User Guide

### Exporting Constraints from a Topology

9. Define the *Scope*, *Delta*, and *Tolerance* for the global constraint in the *Pin Pairs* table.



10. Click *OK* to save the changes you have made and close the dialog box. The table in the *Relative Propagation Delay* schema is refreshed with the newly set or updated constraint values.

▼ Relative Propagation Delay					
Name	Pin 1	Pin 2	Scope	Delta (mil)	Tolerance (mil)
MY_TOP_PBA_M2	L	S	Local	4 ns	5 %
MY_TOP_PBA_M1	MEM2.K7	MEM1.K7	Global	2 ns	5 %

## Deleting a Relative Propagation Delay Constraint

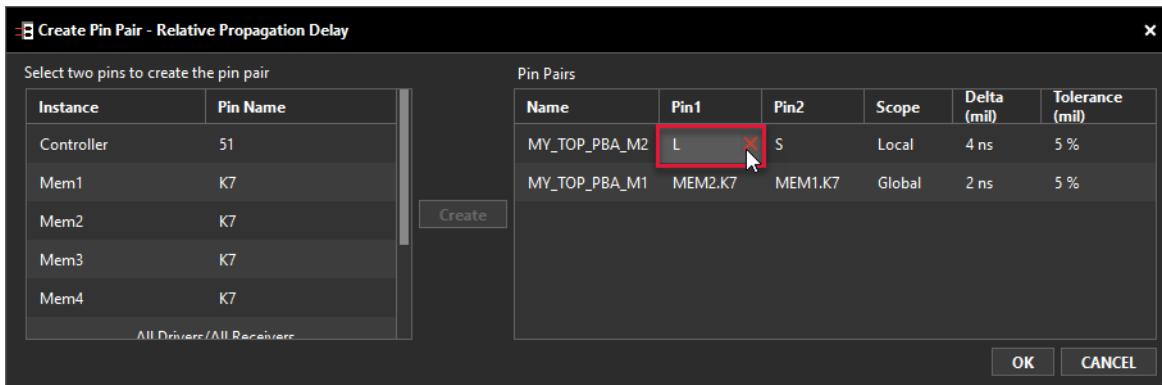
If you want to remove a defined constraint:

1. Click the button adjacent to *Relative Propagation Delay* to open the *Create Pin Pair - Relative Propagation Delay* dialog box.

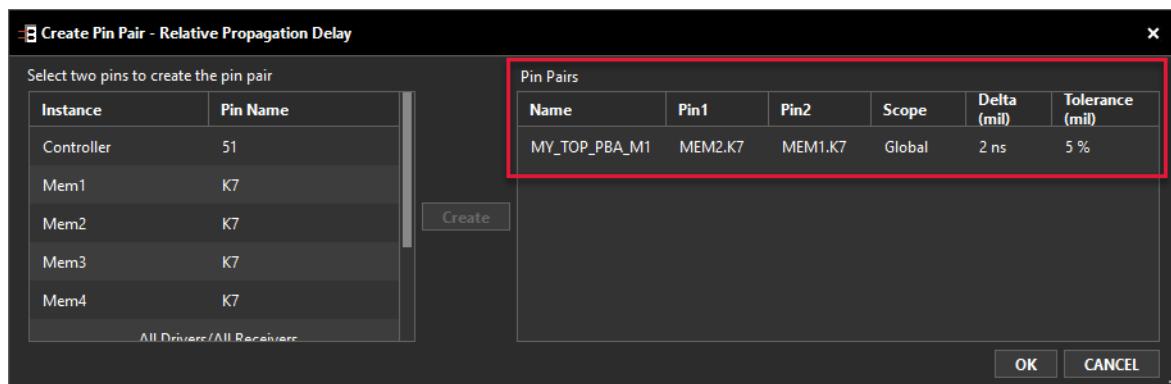
## Topology Workbench User Guide

### Exporting Constraints from a Topology

- Under the *Pin 1* or *Pin2* column, place the pointer on a cell that represents the constraint you want to delete. A cross (X) symbol is displayed as shown below.



- Click the cross (X) to delete the constraint. The *Pin Pairs* table is refreshed.



- Click *OK* to save the change and close the dialog box. The table in the *Propagation Delay* schema is refreshed accordingly as shown below.

Name	Pin 1	Pin 2	Scope	Delta (mil)	Tolerance (mil)
MY_TOP_PBA_M1	MEM2.K7	MEM1.K7	Global	2 ns	5 %

## Setting the Impedance Constraint

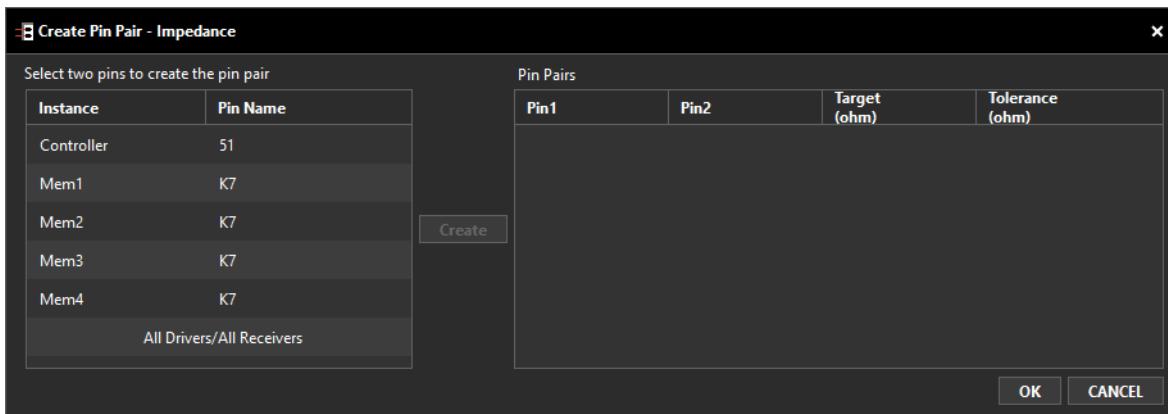
You can create and modify *Impedance* constraint for pin, tee or pin-tee pairs. You can also create delay rules that apply to all pin, tee or pin-tee pairs in the topology. The *Impedance* constraint specify a baseline impedance value and an allowable delta value above and below

## Topology Workbench User Guide

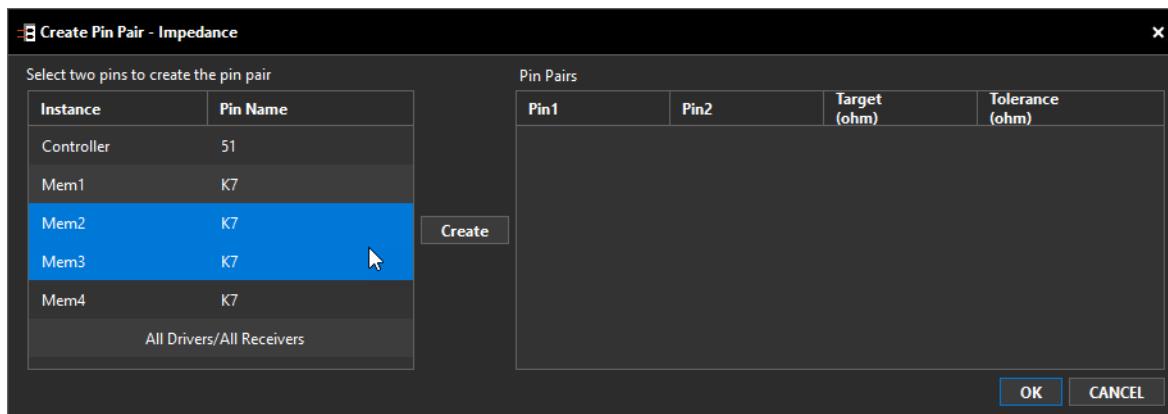
### Exporting Constraints from a Topology

the baseline. To set an *Impedance* constraint for a connection, in the *Properties (Object: <Obj\_Name>)* panel:

1. Click the button adjacent to the *Impedance* schema. The *Create Pin Pair - Impedance* dialog box opens as shown below.



2. Select two pins from the list in the left pane while keeping the `Ctrl` key pressed. The *Create* button is enabled as shown below.

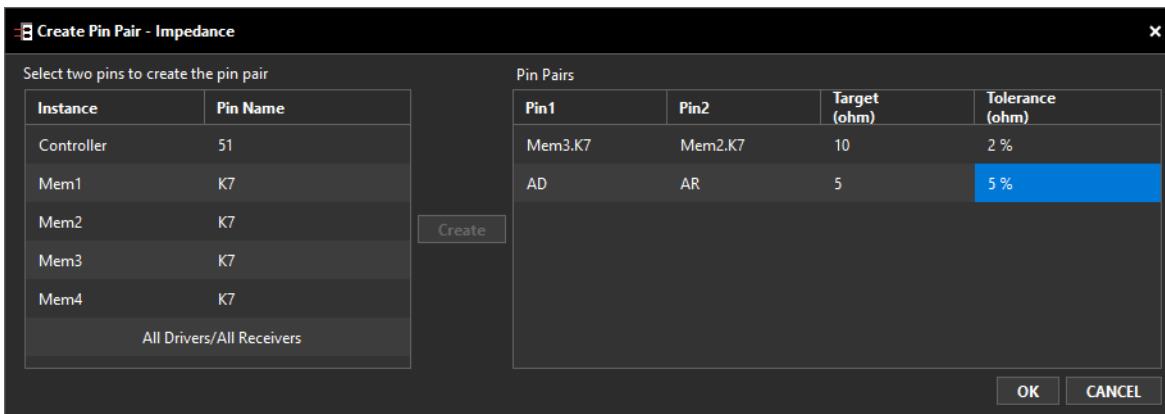


3. Click *Create*. A row of the selected pin pair is added to the *Pin Pair* pane on right.
4. Specify the impedance *Target* value. When you add the *Target* value, a default *Tolerance* percentage appears in the corresponding cell.

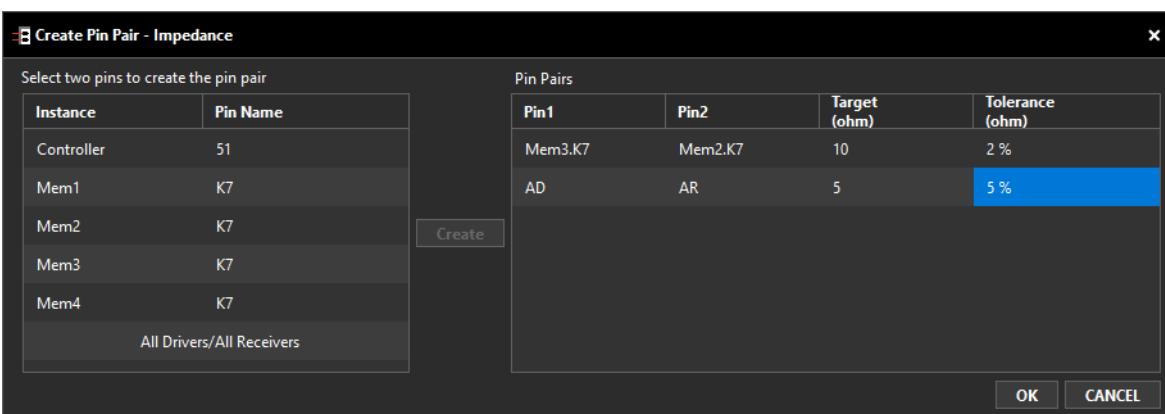
## Topology Workbench User Guide

### Exporting Constraints from a Topology

- Specify the impedance *Tolerance* value. Enter a delta value above and below the baseline impedance as a percentage.



- Create a *All Drivers/All Receivers* global constraint.
- Define the impedance *Target* and *Tolerance* for the global constraint in the *Pin Pairs* table.

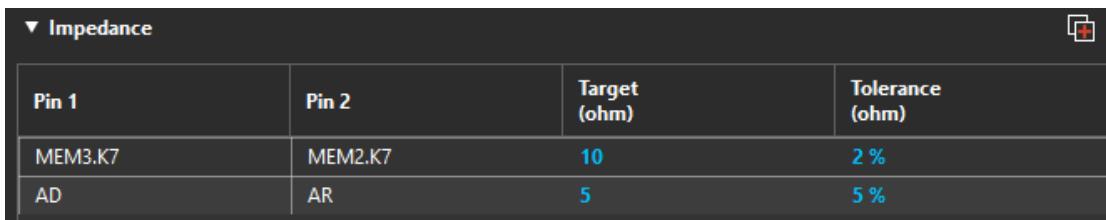


The default format for specifying a *Tolerance* is percentage. If you want to define an absolute tolerance, a value with the unit of measurement can be entered. For example, you can enter `0.1ns` in the *Tolerance* field.

## Topology Workbench User Guide

### Exporting Constraints from a Topology

- Click **OK** to save the changes you have made and close the dialog box. The table in the *Relative Propagation Delay* schema is refreshed with the newly set or updated constraint values.

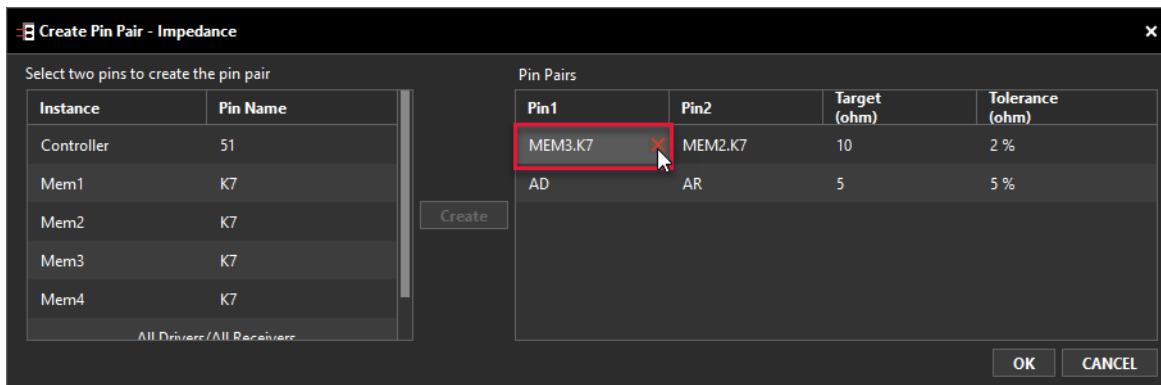


Pin 1	Pin 2	Target (ohm)	Tolerance (ohm)
MEM3.K7	MEM2.K7	10	2 %
AD	AR	5	5 %

## Deleting an Impedance Constraint

If you want to remove a defined constraint, open the

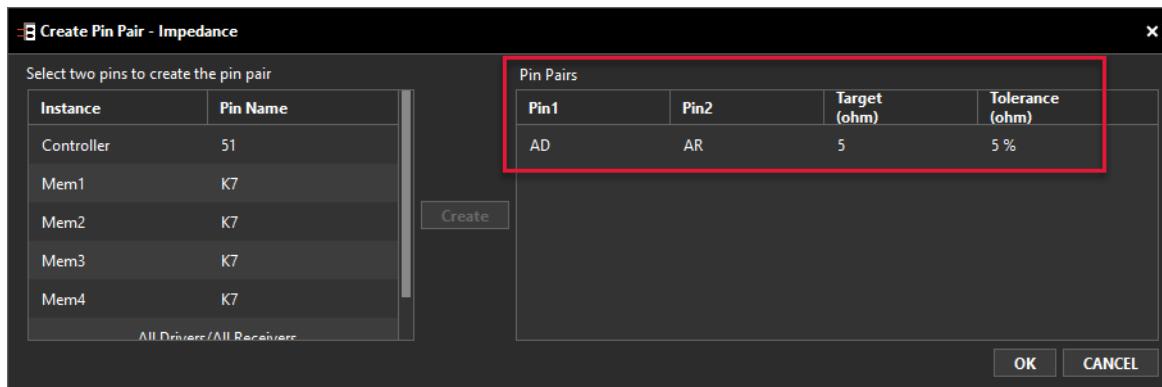
- Click the  button adjacent to *Impedance* to open the *Create Pin Pair - Impedance* dialog box.
- Under the *Pin 1* or *Pin2* column, place the pointer on a cell that represents the constraint you want to delete. A cross (X) symbol is displayed as shown below.



## Topology Workbench User Guide

### Exporting Constraints from a Topology

- Click the cross ( $X$ ) to delete the constraint. The *Pin Pairs* table is refreshed.



- Click *OK* to save the change and close the dialog box. The table in the *Impedance* schema is refreshed accordingly as shown below.

▼ Impedance			
Pin 1	Pin 2	Target (ohm)	Tolerance (ohm)
AD	AR	5	5 %

## Setting the Vias Constraint

To set the *Vias* constraint for a connection, in the *Properties (Object :<Obj\_Name>)* panel:

- Click the *Vias* schema. A table with the available constraint property is displayed with an editable field to add a value.

▼ Vias	
Max Via Count	<Add Value>

- Enter the *Max Via Count* to specify the maximum number of vias allowed in a net.

▼ Vias	
Max Via Count	10

## Setting the Total Etch Length Constraint

To set the *Total Etch Length* constraint for a connection, in the *Properties (Object : <Obj\_Name>)* panel:

1. Click the *Total Etch Length* schema. A table with the available constraint property is displayed with an editable field to add a value.

▼ Total Etch Length		
Minimum Etch Length	<Add Value>	mil
Maximum Etch Length	<Add Value>	mil

2. Enter the *Minimum Etch Length*.
3. Enter the *Maximum Etch Length*.

▼ Total Etch Length		
Minimum Etch Length	15.00	mil
Maximum Etch Length	25.00	mil

## Setting the Switch-Settle Constraint

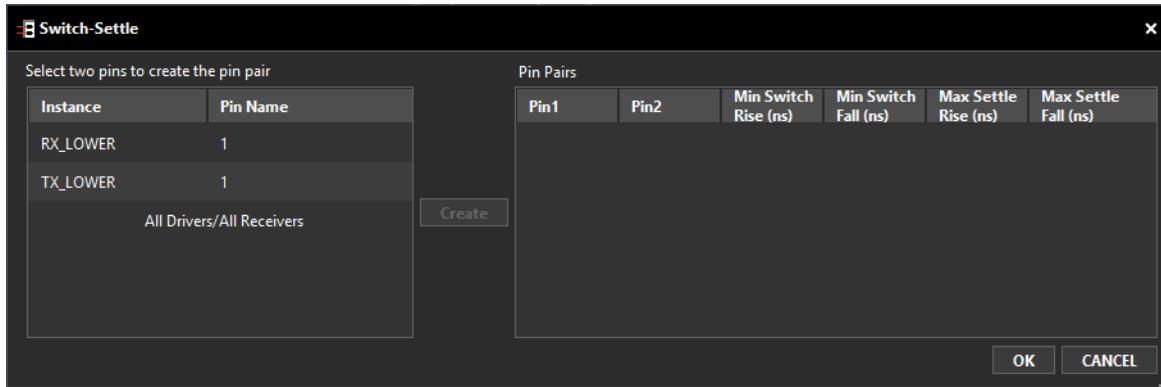
With the *Switch-Settle* constraint, you can create and modify switch and settle delay rules between driver and receiver pin pairs. You can also create switch and settle delay rules that apply to all driver and receiver pin pairs in the topology.

To set a *Switch-Settle* constraint for a connection, in the *Properties (Object: <Obj\_Name>)* panel:

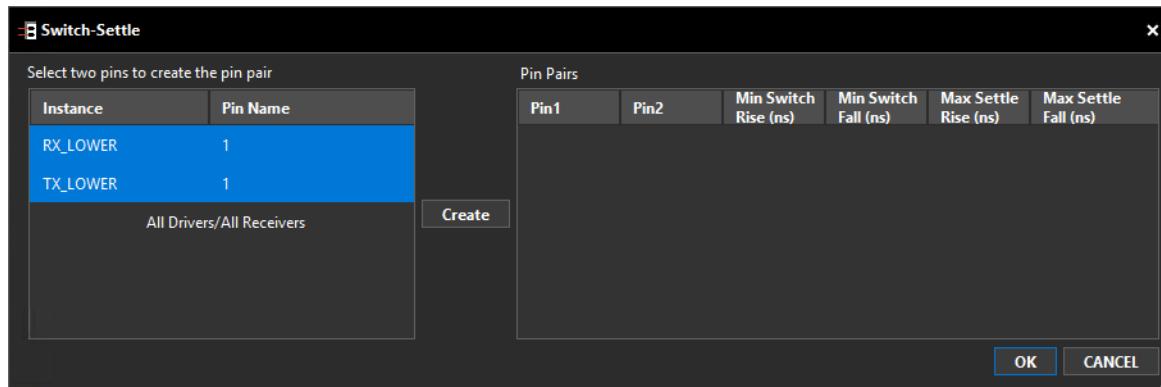
## Topology Workbench User Guide

### Exporting Constraints from a Topology

1. Click the button adjacent to the *Switch-Settle* schema. The *Switch-Settle* dialog box opens as shown below.



2. Select two pins from the list in the left pane while keeping the `Ctrl` key pressed. The *Create* button is enabled as shown below.



3. Click *Create*. A row of the selected pin pair is added to the *Pin Pairs* pane on the right.
4. Add the *Min Switch Rise (ns)*, *Min Switch Fall (ns)*, *Max Switch Rise (ns)*, and *Max Switch Fall (ns)* values in the corresponding cells of the table. These values define the minimum and maximum allowable rising and falling edges of the switch delays for the selected pin pairs.
5. Create a *All Drivers/All Receivers* global constraints:  
**Note:** When you click this global constraint, the *Create* button is enabled.
6. Define the *Min Switch Rise (ns)*, *Min Switch Fall (ns)*, *Max Switch Rise (ns)*, and *Max Switch Fall (ns)* values for the global constraint in the *Pin Pairs* table.
7. Click *OK* to save the changes you have made and close the dialog box. The table in the *Switch-Settle* schema is refreshed with the newly set or updated constraint values.

## Setting the Max Parallel Constraint

With the *Max Parallel* constraint, you can assign maximum parallel routing constraint rules to signals. A maximum of four length/gap pairs can be defined. Each pair defines a maximum parallel coupled length between the given net and any other net (assuming that the two nets are separated by an air gap which is less than or equal to the given gap distance value).

To set a *Max Parallel* constraint for a connection, in the *Properties (Object: <Obj\_Name>)* panel:

1. Enter a coupled length distance value in the cell under the *Length* column. This defines the allowable length for the selected signals to run in parallel.

▼ Max Parallel			
Rule#	Length	Gap	Unit
1			mil
2			mil
3			mil
4			mil

2. Enter a gap value in the cell under the *Gap* column. This defines the allowable gap between the selected signals running in parallel.
3. Repeat steps 1 - 2 to add additional rules till a maximum of four rules have been defined.

## Setting the DiffPair Constraint

With the *DiffPair* constraint, you can assign differential pair rules to differential pair objects in a board design. As a differential topology can contain two separate Xnets, Topology Workbench does not allow a single Xnet constraint definition between pins on different Xnets.

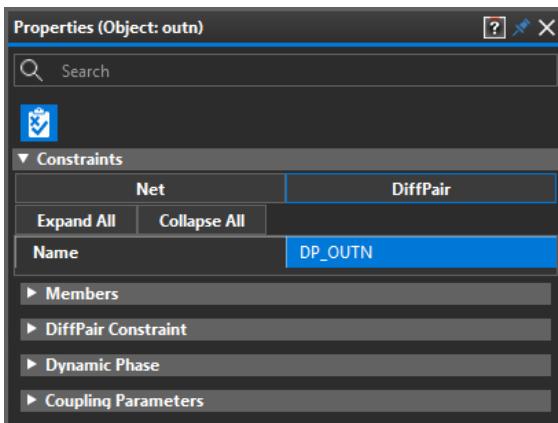
To set a *DiffPair* constraint for a connection, in the *Properties (Object: <Obj\_Name>)* panel:

1. Click the *DiffPair* tab to create and modify differential pair rules.

## Topology Workbench User Guide

### Exporting Constraints from a Topology

2. Enter a unique *Name* for the *DiffPair* constraint.



The *Type* and *Name* of the *Members* of a *DiffPair* constraint is displayed as shown below:

▼ Members	
Type	Name
Net	outn
Net	outp

3. Add the values for the *DiffPair Constraint*.

▼ DiffPair Constraint		
Max Uncoupled Length	<Add Value>	mil
Static Phase Tolerance	<Add Value>	mil
Min Line Spacing	<Add Value>	mil

The following parameters can be set:

- ❑ *Max Uncoupled Length*: Enter the maximum allowable uncoupled length.
- ❑ *Static Phase Tolerance*: Enter a tolerance value to specify a separation to which static phase matching is maintained.
- ❑ *Min Line Spacing*: Enter a value to constrain the distance between any two segments from each Xnet member of the differential pair. The value you enter must be less than or equal to the *separation*, minus the negative tolerance. The value must also be greater than or equal to the *Neck Gap* value.

## Topology Workbench User Guide

### Exporting Constraints from a Topology

#### 4. Add the values for the *Dynamic Phase*.

▼ Dynamic Phase		
Max Length	<Add Value>	mil
Tolerance	<Add Value>	mil

The following parameters can be set:

- Max Length*: Enter the maximum allowable length for the dynamic phase.
- Tolerance*: Enter a tolerance value for the dynamic phase.

#### 5. Add the values for the *Coupling Parameters*.

▼ Coupling Parameters		
Primary Gap	<Add Value>	mil
Primary Width	<Add Value>	mil
Neck Gap	<Add Value>	mil
Neck Width	<Add Value>	mil
(+) Tolerance	<Add Value>	mil
(-) Tolerance	<Add Value>	mil

The following parameters can be set:

- Primary Gap*: Enter a value for the ideal edge-to-edge spacing between the pair that should be maintained for the entire length of the pair. Values you set for *Neck Gap* override *Primary Gap* values in areas that need smaller gaps to get through dense components.
- Primary Width*: Enter a value for the minimum width of each member of the differential pair.
- Neck Gap*: Enter a value for the edge-to-edge spacing between a pair as it goes through tight areas full of component pins and vias. *Neck Gap* overrides any value in the *Primary Gap* when the differential pair's spacing collapses to or below the value of the *Neck Width*. Ensure that the neck gap does not go below any *Minimum line spacing* value you have set. You do not need to define a neck gap if you set *(-) Tolerance* with a value that accounts for the needed neck gap.
- Neck Width*: Enter a value for the width of each line in a differential pair as it goes through confined areas among densely placed components.
- (+) Tolerance*: Enter a *(+)* *Tolerance* value to define a band around the primary gap in which the lines of a pair can go beyond the primary gap value.

**Note:** The lines are considered coupled when they are within the band specified by the *(+)* *Tolerance* and outside the band specified by the *(-)* *Tolerance*.

- **(-) Tolerance:** Enter a **(-) Tolerance** value to define a band around the primary gap in which the lines of a pair can go closer than the primary gap value.

**Note:** The lines are considered coupled when they are within the band specified by the **(+) Tolerance** and outside the band specified by the **(-) Tolerance**.

## Defining the **MappingTag** Parameter in Topology Workbench

A pin parameter, *mappingTag*, is used to uniquely identify a pin. The topology file supports the *mappingTag* parameter that can be defined for all non-discrete nodes. When you extract a topology from Constraint Manager and then update it with an ECSet containing ambiguous nodes that are not tagged in Topology Workbench a warning appears.

Selecting *No* aborts the *Update Constraint Manager* command, and lets you set the *mappingTag* parameter for the ambiguous nodes. Else, Constraint Manager is updated with the existing (ambiguous) data.

To specify a value for the *mappingTag* parameter:

1. Double-click a block in the layout. The *Edit Properties* panel opens with the Attributes section.
2. Add the required property in the **<Add Property>** cell below the *mappingTag* parameter for a node. It should be a uniquely identifiable value.

▼ Attributes	
Name	Value
mappingTag	•
<Add Property>	

3. Specify a uniquely identifiable value in the resulting input box.



Before you *Update Constraint Manager* with the modified ECSet, ensure that the *Verify Schedule* field in the *Wiring* schema of the *Constraints* tab of the *Edit Properties* panel is set to *Clear*.

When the ECSet with the *mappingTag* values is applied to target nets in Constraint Manager, the *ECSet Apply* log is displayed with information about the changes.

## **Topology Workbench User Guide**

### Exporting Constraints from a Topology

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You then need to run *Audit* on the ECSet in Constraint Manager and assign the tags in the ECSet to the appropriate pins in the design in the *Review ECSet Mapping* dialog box.

For more information, see the [\*Mapping ECSets to Nets using Tags\*](#) in *Constraint Manager User Guide*.

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# Using Optimality with Topology Workbench

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The Optimality Intelligence System Explorer feature is available in the Topology Explorer, Serial Link Analysis (SLA), and Parallel Bus Analysis (PBA) workflows.

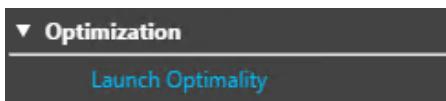
With growing complexity of modern electronic devices, realizing a system design concept into a high-performance product is an iterative, resource-intensive, and an expensive process. The Optimality Intelligence System Explorer uses an artificial intelligence (AI)-driven multidisciplinary analysis and optimization (MDAO) technology that enables you to optimize your design quickly and efficiently with no accuracy loss.

The Optimality Intelligence System Explorer requires you to specify the design parameters that you want to optimize and your optimization goal. During the optimization process, the Optimality Intelligence System Explorer creates additional surrogate models to optimize these parameters. The optimization stops when the goal is achieved and the result for each iteration is stored in a separate folder under the case folder.

**Note:** Before running parameter optimization, ensure that the design setup is complete, that is, all the parameters of the design are successfully imported into Clarity 3D Workbench along with the design, the frequency settings are specified, computer resources are set up, and the design is ready for simulation. It is recommended that you run a prevalidation check to ensure that your design is free of errors before performing the optimization.

To perform parameter optimization, perform the following steps:

1. Select *Launch Optimality* from the *Optimization* schema in the *Workflow* panel.

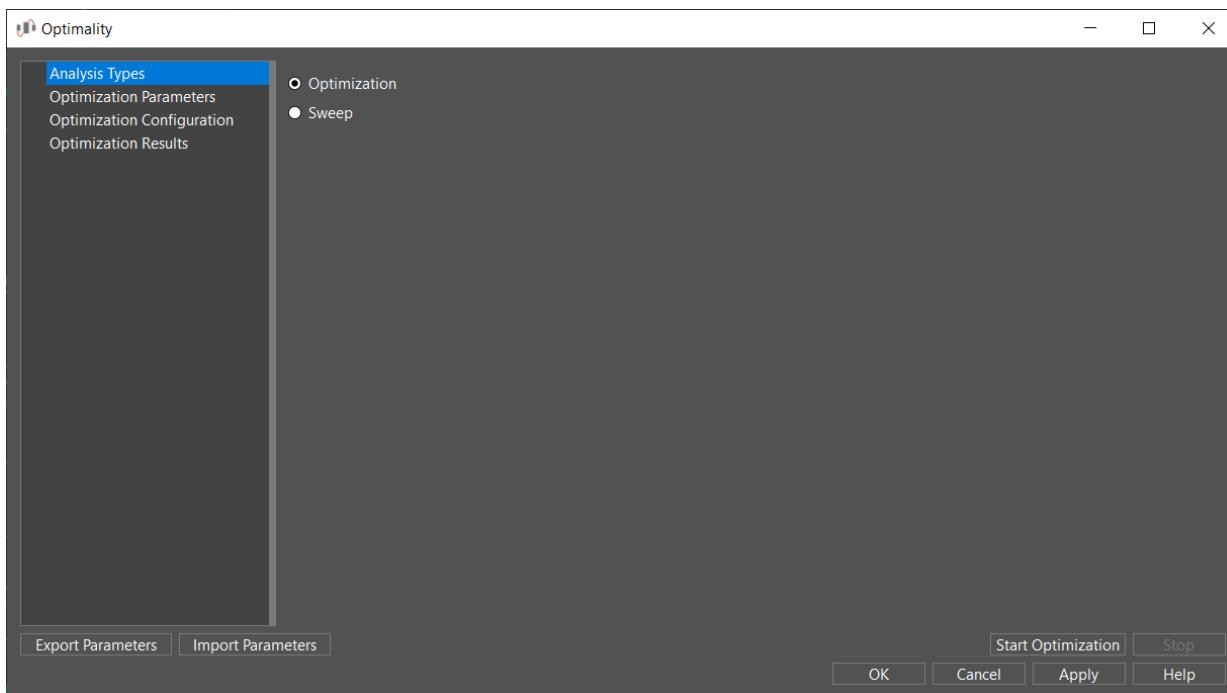


**Note:** Alternatively, run the `topxp::startOptimization -interconnect` Tcl command in the Command Window panel.

# Topology Workbench User Guide

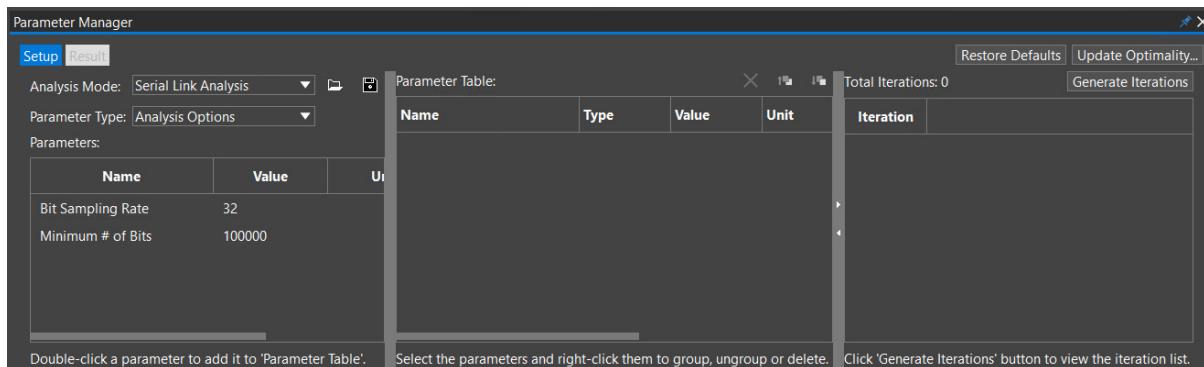
## Using Optimality with Topology Workbench

The Optimality window is displayed, as shown below.



The Optimality window contains two panes. The left pane enables you to choose the analysis types, the optimization parameters, optimization configuration, and optimization results. The right pane contains the options related to selection made on the left pane. Depending on the types of block in the topology, the default parameters are added automatically to the Optimality window.

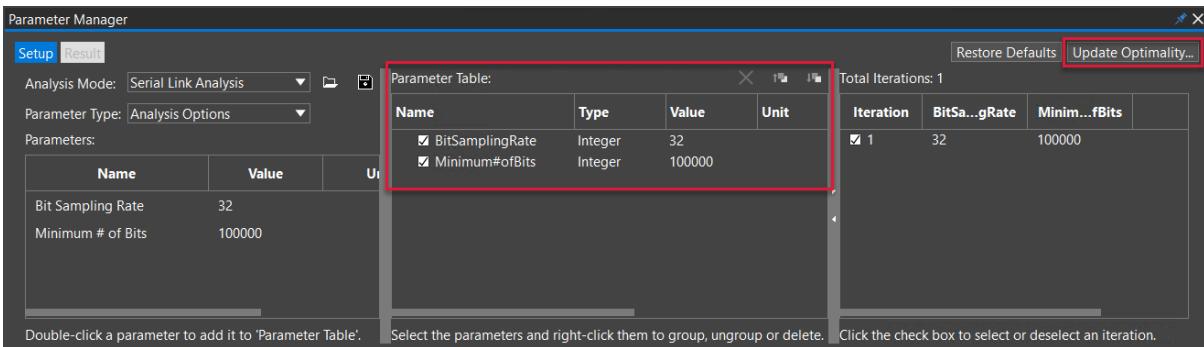
**Note:** If the parameter list is empty, a message is displayed. Clicking *OK* in the message box opens the Parameter Manager where you can define the optimization parameters.



## Topology Workbench User Guide

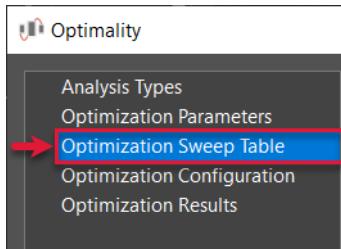
### Using Optimality with Topology Workbench

The interface and operational mechanics of the Parameter Manager are similar to the Sweep Manager. Once you have defined the required parameters, click the *Update Optimality* button that updates and opens the Optimality window.



2. Click *Analysis Types* in the left pane. The supported workflows are displayed in the right pane.

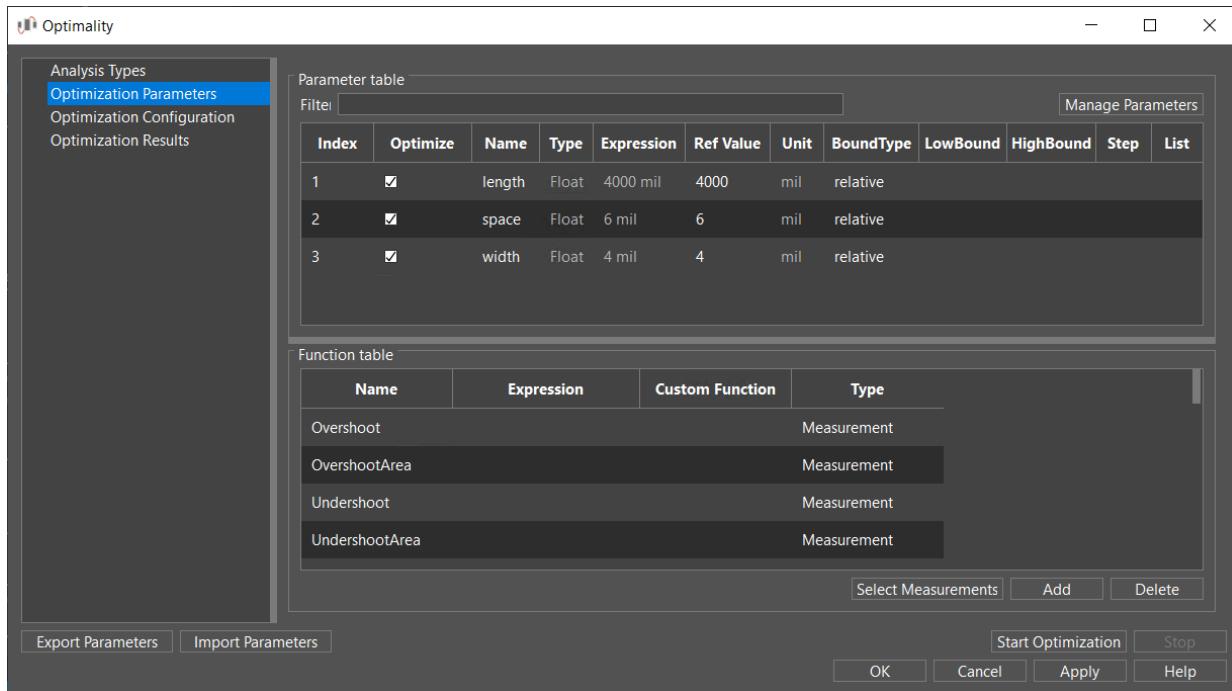
By default, the *Optimization* workflow is selected. You can select the *Sweep* workflow, if required. When you select the *Sweep* workflow, an additional option, *Optimization Sweep Table* is added in the left pane where you can configure the sweep table.



# Topology Workbench User Guide

## Using Optimality with Topology Workbench

3. Click *Optimization Parameters* on the left pane. The related options are displayed in the right pane, as shown below.



4. Select the parameters that you want to optimize in the *Optimize* column. For example, select the check boxes corresponding to the *length*, *space*, and *width* parameters.

The auto-calculated, non-editable optimization parameter values are displayed in the *Type*, *Expression*, *Ref Value*, and *Unit* columns. You can click the *Manage Parameters* button to open the Parameter Manager to add, delete, and redefine optimization parameters.

5. Select the parameter bound type from the *BoundType* column. By default, *relative* is selected.

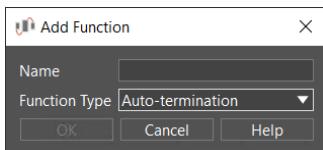
**Note:** This column is editable for length, space, and width parameters.

6. Specify the lower bound value in the *LowBound* column. For example, specify *0.9*. This will set the lower bound of the parameter to 90 percent of the reference value.
7. Specify the higher bound value in the *HighBound* column. For example, specify *1.1*. This will set the high bound of the parameter to 110 percent of the reference value.
8. Click *Add* below the *Function table*.

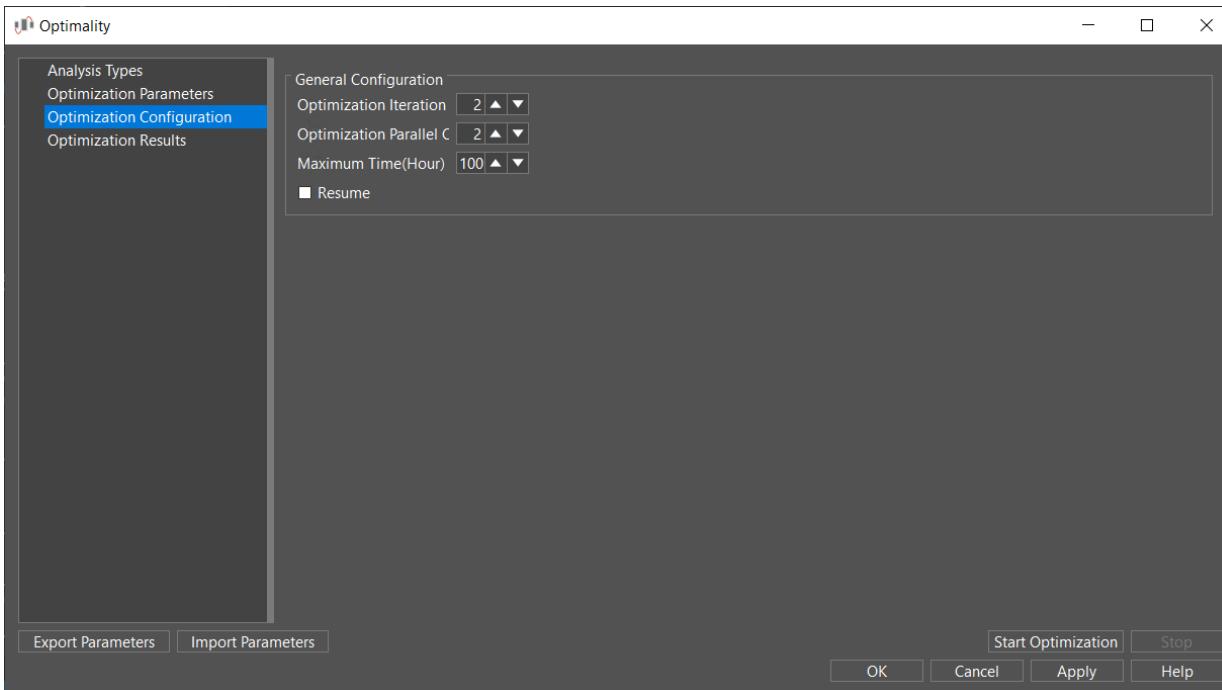
## Topology Workbench User Guide

### Using Optimality with Topology Workbench

The Add Function dialog box is displayed, as shown below.



9. Specify the name of the optimization function in the *Name* field. For example, specify *Obj*.
10. Select the *Function Type* from the drop-down list and click *OK*. You can select one from *Auto-termination*, *MidFunction*, and *Objective Function(goal)*.
11. Click *OK*. A row gets added to the *Function table* for the new function.  
For *Objective Function(goal)* function type, you can double-click and edit the cells under the *Name*, *Expression*, or *Custom Function* columns. Clicking a cell under the *Custom Function* column opens an editor where you enter the custom function.  
For *Auto-termination* and *MidFunction* function types, you can edit only the cells under the *Name* and *Expression* columns.
12. Click *Optimization Configuration* in the left pane. The configuration options are displayed in the right pane, as shown below.



## Topology Workbench User Guide

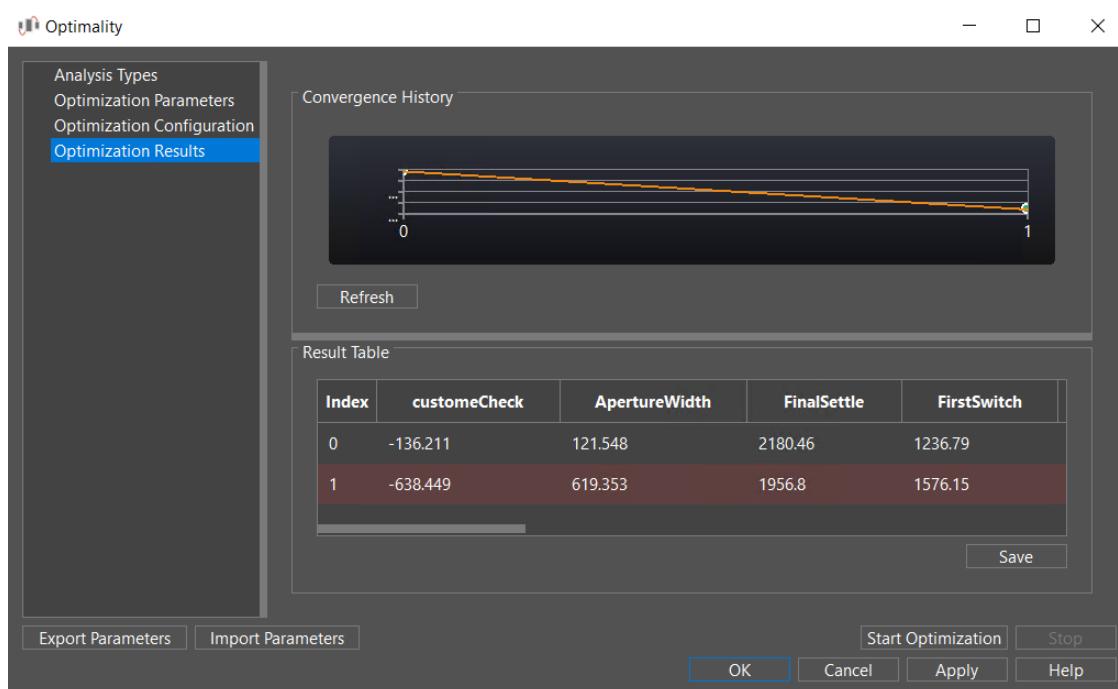
### Using Optimality with Topology Workbench

13. Select the maximum number of iterations to be performed from the *Optimization Iteration Count* spin box. For example, selecting 25 means that optimization will perform 25 iterations.
14. Select the number of parallel processes from the *Optimization Parallel Count* spin box.

**Note:** This number will depend upon the number of CPUs you specify in the Set up Computer Resources dialog box. For example, in the case of a local simulation run, if you specify 8 in the CPUs field, optimization will occupy  $8 \times 2 = 16$  CPUs for the simulation. Therefore, it is recommended that you select this number carefully and not overload the computer.

15. Select the maximum number of hours the optimization should run from the *Maximum Time(Hour)* spin box.
16. Click *Start Optimization*.

The optimization starts and the *Optimization Results* section of the Optimality window opens. The progress of the optimization is displayed in the progress bar. Once the optimization completes, the *Convergence History* is displayed. In addition, the *Result Table* shows results for each iteration in separate rows. The result that closely matches the goal is highlighted. The results for each iteration are also saved in separate folders in the design folder.

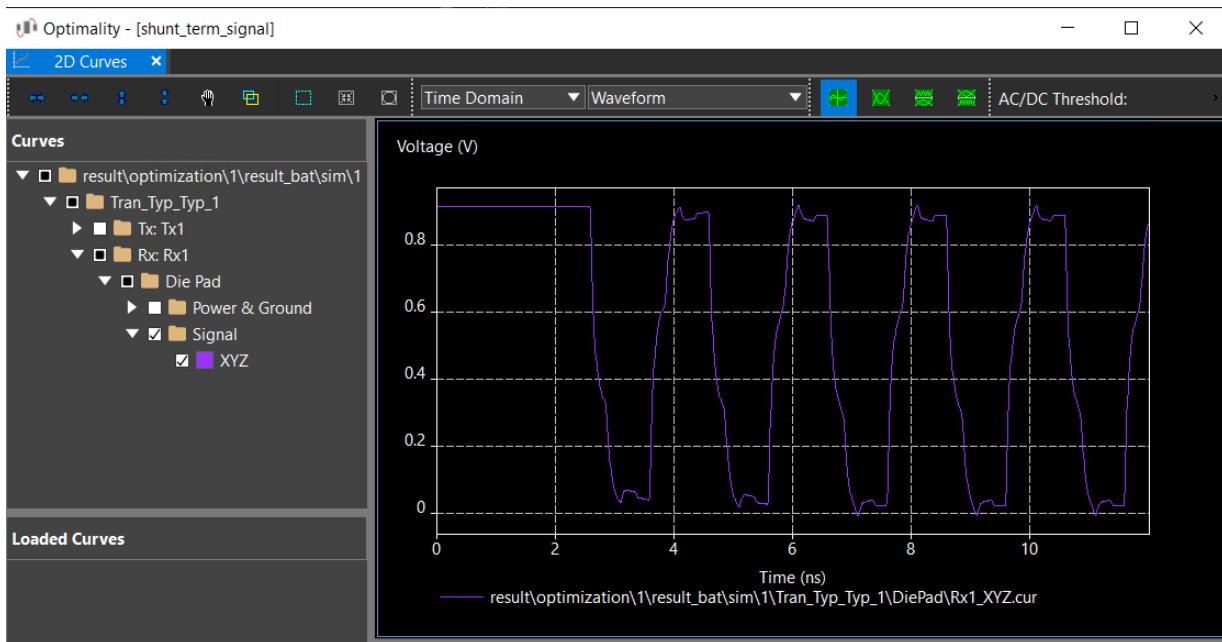


17. Right-click the required rows from the *Result Table* and click *Show Result*.

# Topology Workbench User Guide

## Using Optimality with Topology Workbench

The 2D Curves tab opens within the Optimality window for review.



### Related Topic

#### [Optimality Window](#)

## Optimality Window

The Optimality window contains the following sections:

- *Analysis Types* – Specifies the parameters that need to be optimized.
- *Optimization Parameters* – Specifies the optimization parameters and objective functions (goal).
- *Optimization Sweep Table* – Specifies the parameters for the sweep workflow.
- *Optimization Configuration* – Specifies the configuration setup for optimization.
- *Optimization Results* – Displays the results in a graphical or table format.

## Analysis Types

The *Analysis Types* section contains the following options:

Option	Description
<i>Optimization</i>	Selects the optimization workflow.
<i>Sweep</i>	Selects the sweep workflow.

## Optimization Parameters

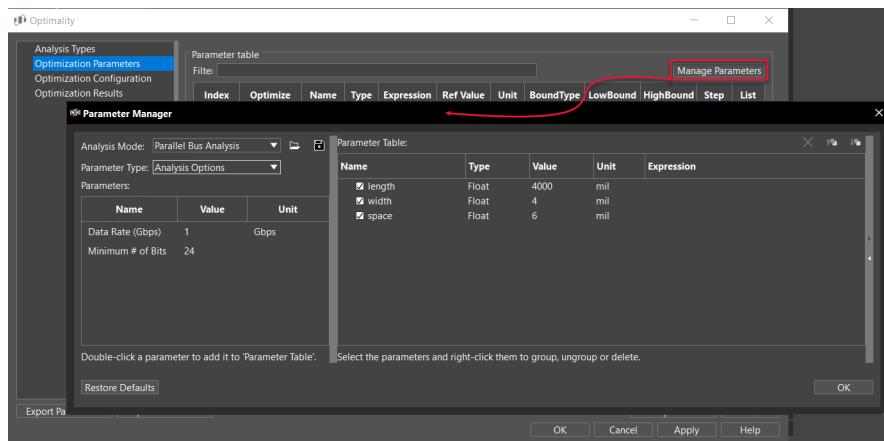
The Optimization Parameters section contains a *Parameter table* and a *Function table* with the following columns:

Option	Description
<b>Parameter Table</b>	
<i>Index</i>	Parameter index.
<i>Optimize</i>	Select the check box to optimize the corresponding parameter specified in the <i>Name</i> column.
<i>Name</i>	Name of the parameter to be optimized.
<i>Type</i>	Specifies the parameter type. For example: <i>Float</i> , <i>Integer</i> , <i>String</i> .
<i>Expression</i>	Specifies the parameter value. The value can be a math expression.
<i>Ref Value</i>	Specifies the original value of the parameter.
<i>Unit</i>	Specifies the unit of the parameter.
<i>BoundType</i>	Specifies the parameter bound type. Possible values are:  <i>relative</i> - Uses the values specified in the <i>LowBound</i> and <i>HighBound</i> column and multiplies it with the value specified in the <i>Ref Value</i> column.  <i>absolute</i> - Uses the values specified in the <i>LowBound</i> and <i>HighBound</i> columns directly.
<i>LowBound</i>	Specifies the lower parameter value for optimization.

# Topology Workbench User Guide

## Using Optimality with Topology Workbench

<i>HighBound</i>	Specifies the higher parameter value for optimization.
<i>Step</i>	Specifies the value by which the discrete parameter value should be stepped up. This column is enabled only when discrete is selected in the <i>Type</i> column.
<i>List</i>	Specifies the list.
<i>Manage Parameters</i>	Opens the Parameter Manager form when clicked. The displayed form lets you add, redefine, and delete parameters for optimization.



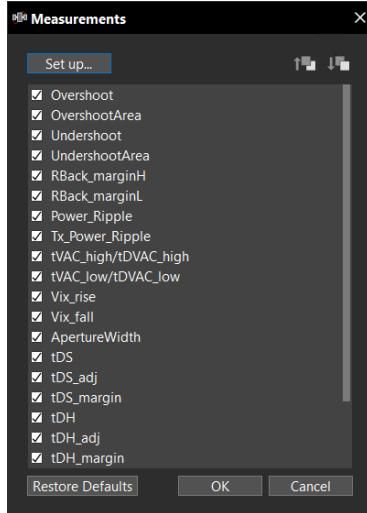
## Function Table

<i>Name</i>	Specifies the name of the optimization parameter.
<i>Expression</i>	Specifies the final objective function (goal). This option is enabled when <i>Function Type</i> is selected as <i>Auto-termination</i> , <i>MidFunction</i> , or <i>Objective Function(goal)</i> .
<i>Custom Function</i>	This option is similar to <i>Expression</i> . It enables you to define the final objective function as a python code.
	This option is enabled only when <i>Function Type</i> is selected as <i>Objective Function(goal)</i> . Clicking a cell under the <i>Custom Function</i> column opens an editor where you can enter the custom function.

## Topology Workbench User Guide

### Using Optimality with Topology Workbench

<b>Type</b>	Specifies the type of the function parameter. Possible values are:  <i>MidFunction</i> – Specifies a middle function expression that is used to simplify the final function expression.  <i>Objective Function(goal)</i> – Specifies the final optimization object function.  <i>Auto-termination</i> – Specifies the threshold setting. When the goal reaches the threshold value, optimization is stopped automatically.  <i>Measurement</i> – Specifies that the function is of measurement type.
<b>Select Measurements</b>	Opens the Measurements form when clicked. The displayed form displays a range of default measurements that are available in the supported workflows—Topology Explorer, SLA, and PBA workflow when the <i>Use Channel Simulator</i> check box is selected. You can select the measurements for which optimization is needed.

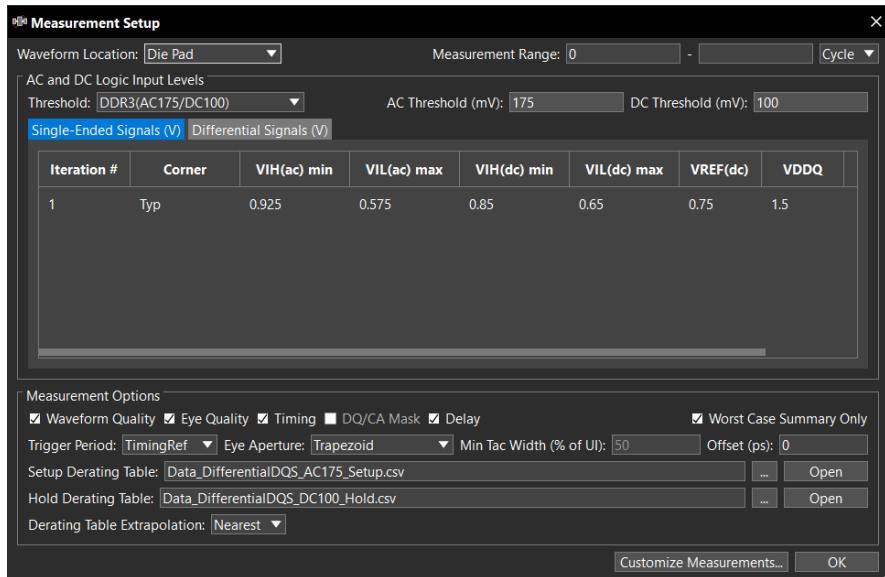


**Note:** In the SLA workflow, Optimality supports PAM4 interfaces. If you set *Signaling* for the stimulus pattern to *PAM4* in the Analysis Options panel, PAM4-specific measurements are displayed in the Measurements form.

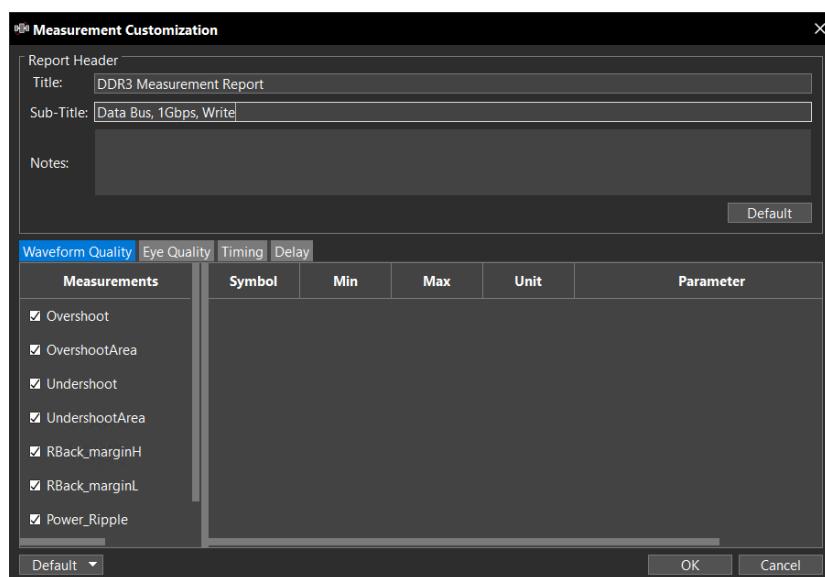
# Topology Workbench User Guide

## Using Optimality with Topology Workbench

Clicking the *Set up* button in the Measurements form opens the Measurement Setup form where you can specify the *Waveform Location, Measurement Range, AC and DC Logic Input Levels, and Measurement Options*.



To customize the measurement results such as Report Header, Waveform Quality, and Eye Quality, you can click the *Customize Measurements* button in the Measurement Setup form. This opens the Measurement Customization form as shown below.

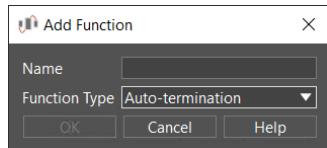


## Topology Workbench User Guide

### Using Optimality with Topology Workbench

#### Add

Opens the Add Function dialog box where you can specify the *Name* of the new optimization function and its *Function Type*.



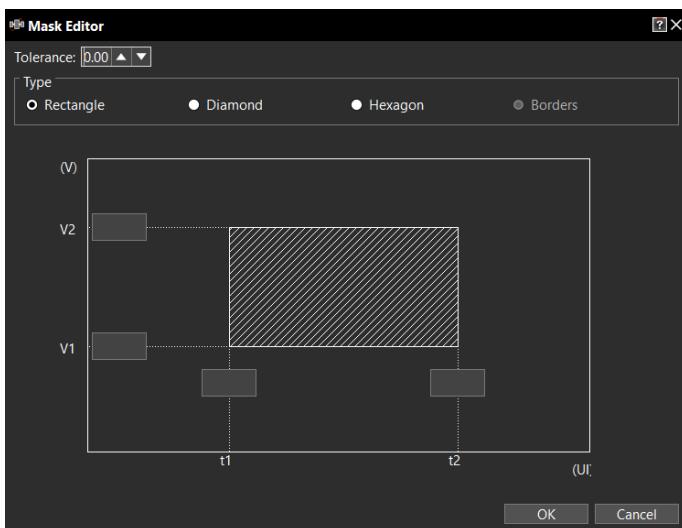
The *Function Type* list provides *Auto-termination*, *MidFunction*, and *Objective Function(goal)* as the valid values.

#### Delete

Deletes the functions selected in the *Function table*. To select multiple functions at a time, keep the `Ctrl` key pressed while clicking the functions that need to be deleted.

#### Set up Mask

Opens the Mask Editor form to let you define the eye mask as an objective function.



The defined eye mask is added as *EyeContourMask* of *Measurement* type in the *Function table*.

You can click the *Export Parameters* button to save the optimization parameters to a file with the name `<design_name>_Opt.param`. If the optimization parameter file exists, you can click *Import Parameters* to import the optimization parameters.

## Optimization Sweep Table

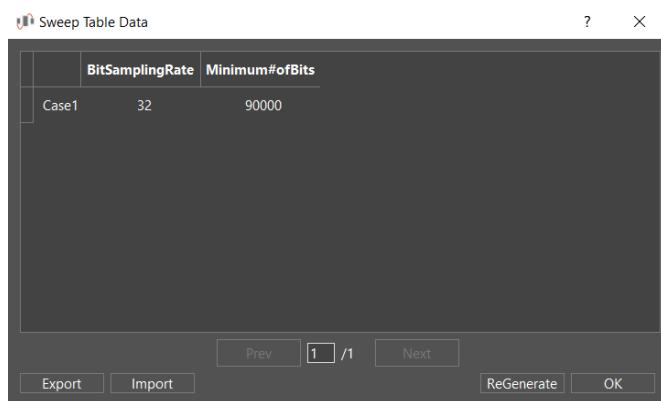
The Optimization Sweep Table section contains the following options:

Name	Description
<i>Index</i>	Specifies the parameter index.
<i>Name</i>	Specifies the parameter name.
<i>SweepType</i>	Specifies the sweep type. Possible values are <i>Count</i> and <i>Step</i> .
<i>SweepRefValue</i>	Specifies the original value of the sweep parameter.
<i>LowBound</i>	Specifies the lower sweep parameter value. This field is not editable. You can edit the value for this field in the Optimization Parameters table.
<i>HighBound</i>	Specifies the higher sweep parameter value. This field is not editable. You can edit the value for this field in the Optimization Parameters table.
<i>SweepStep</i>	Specifies the value by which the sweep parameter value should be stepped up. This column is enabled only when <i>Step</i> is selected in the <i>SweepType</i> column.
<i>SweepCount</i>	Specifies the count by which the sweep parameter value should be increased. This column is enabled only when <i>Count</i> is selected in the <i>SweepType</i> column.
<i>SweepArray</i>	Shows all the parameter values that are defined by LowBound, HighBound, Step and Count.

## Topology Workbench User Guide

### Using Optimality with Topology Workbench

**Sweep Table Preview** Displays the Sweep Table Data dialog box, as shown below.



You can add or delete cases in this table based on which the *LowBound* and *HighBound* values are modified automatically.

You can also click *Import* to import the sweep data from a CSV file or click *Export* to save the data to a CSV file.

## Optimization Configuration

The Optimization Configuration section contains the following options:

Name	Description
<i>Optimization/Sweep Iteration Count</i>	Specifies the total number of iterations for the optimization run. This option is disabled for the sweep workflow.
<i>Optimization/Sweep Parallel Count</i>	Specifies the number of parallel resources to use for optimization. Check the <i>Total CPU</i> and <i>Total Memory</i> values in the Set up Computer Resources dialog box for this setting. For the Sweep workflow, the number displays the number of cases specified in the Sweep Table Data dialog box.
<i>Maximum Time(Hour)</i>	Specifies the time for which optimization should run. Optimization stops automatically when the specified number of hours elapse.
<i>Resume</i>	Select this check box to start the optimization run from the point it stopped.

## Optimization Results

The result section displays the optimization result. It contains the following tabs:

Name	Description
<i>Convergence History</i>	<p>Displays the graph curve. It supports optimization for one or two objective functions. In case of one objective function, the X axis indicates the iteration index and the Y axis indicates the objective function value. In case of two objective functions, the X axis indicates the values of the first objective function and the Y axis indicates the values of the second objective function.</p> <p>The graph curve is auto-refreshed periodically, but you can click the <i>Refresh</i> button to refresh the graph curve on demand.</p>
<i>Result Table</i>	<p>Displays the objective function value and the parameters' value for each iteration in a table.</p> <p>You can click the <i>Save</i> button to save the results in a .csv file.</p>

**Topology Workbench User Guide**  
Using Optimality with Topology Workbench

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## A

# Choosing Blocks to Place on the Canvas

The floating toolbar in the Topology Workbench window lets you choose from the various types of blocks that are displayed depending on the active workflow. Blocks can be incorporated for single-ended or differential signals, and for connectivity method of wire-based or block-based.

This topic covers information about the supported blocks to assist you in making a choice.

**Note:** The display order of different types of blocks in the floating toolbar change in different projects. The most frequently used blocks are displayed first.

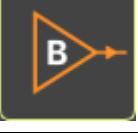
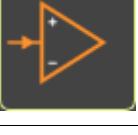
## Related Topics

- [Adding Blocks to the Canvas](#)
- [Connecting the Blocks on the Canvas](#)
- [Changing the Orientation of a Block](#)
- [Managing Connections Between Blocks and Signals](#)

Block Symbol	Block Name	Workflow	Description
<b>Differential Signals</b> (displayed when the <i>Diff Signals</i> check box is selected in the <i>Add Block</i> floating toolbar)			
	Transmitter (SPICE)	Topology Explorer, SLA	Use a Transmitter block to add a SPICE-based <b>driver</b> model that can be transistor-level or behavioral. You can add any number of transmitter blocks on the canvas.
	Transmitter (IBIS)	Topology Explorer, SLA	Use Transmitter (IBIS) block to add a driver represented by an <b>Output</b> model from an IBIS file.

## Topology Workbench User Guide

### Choosing Blocks to Place on the Canvas

Block Symbol	Block Name	Workflow	Description
	Receiver (SPICE)	Topology Explorer, SLA	Use a Receiver block to add a SPICE-based <b>receiver</b> model that can be transistor-level or behavioral. You can add any number of receiver blocks on the canvas.
	Receiver (IBIS)	Topology Explorer, SLA	Use Receiver (IBIS) block to add a driver represented by an <b>Input</b> model from an IBIS file.
<b>Block-Based Signals</b> (displayed when the <i>Block-Based</i> toggle button is selected in the <i>Settings</i> option of the floating toolbar)			
	Transmitter (SPICE)	Topology Explorer, SLA	This represents a single-ended transmitter block that adds a SPICE-based <b>driver</b> model of transistor-level or behavioral type.
	Transmitter (IBIS)	Topology Explorer, SLA	This represents a single-ended transmitter block that is based on an <b>Output</b> model from an IBIS file.
	Receiver (SPICE)	Topology Explorer, SLA	This represents a single-ended receiver block that adds a SPICE-based <b>receiver</b> model of transistor-level or behavioral type.
	Receiver (IBIS)	Topology Explorer, SLA	This represents a single-ended receiver block that is based on an <b>Input</b> model from an IBIS file.

## Topology Workbench User Guide

### Choosing Blocks to Place on the Canvas

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<b>Block Symbol</b>	<b>Block Name</b>	<b>Workflow</b>	<b>Description</b>
<b><i>Other Blocks</i></b>			
	I/O (IBIS)	Topology Explorer	<p>By default, an I/O block is treated as an equivalent of a receiver block. To change an it to a transmitter block, right-click the block and click <i>Make Transmitter</i> from the displayed shortcut menu.</p> <p><b>Note:</b> In a topology extracted from an Allegro tool, the existing I/O blocks retain their original properties and shape.</p>
	Controller IBIS	Topology Explorer, PBA	<p>Topology Workbench generates the multi-pin or block-based connections of a Controller block depending on the bus definition, pin mapping, and setup defined in the <i>Load IBIS</i> form. These definitions cannot be modified.</p> <p>When Explicit IO Power and Ground Terminals are utilized, ensure that all the powers and grounds of the Controller block are connected to do the non-ideal power bus simulation.</p> <p><b>Note:</b> You can add only one Controller block on the canvas. If a Controller or a Controller SPICE block has already been instantiated, the option in the floating toolbar is disabled.</p>
	Controller SPICE	Topology Explorer, PBA	<p>A Controller SPICE block enables an arbitrary SPICE subcircuit to be used as the Controller block in a Parallel Bus Analysis simulation.</p> <p><b>Note:</b> You can add only one Controller SPICE block on the canvas. If a Controller or a Controller SPICE block has already been instantiated, the option in the floating toolbar is disabled.</p>

## Topology Workbench User Guide

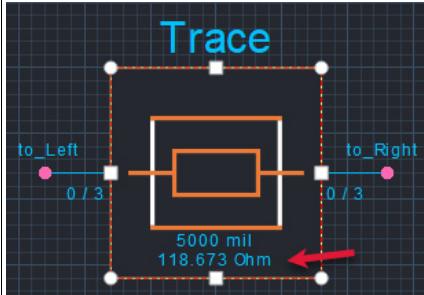
### Choosing Blocks to Place on the Canvas

Block Symbol	Block Name	Workflow	Description
	Memory IBIS	Topology Explorer, PBA	<p>Topology Workbench generates the multi-pin connections of a Memory block based on the bus definition, pin mapping, and setup defined in the <i>Load IBIS</i> form. These multi-pin connections cannot be modified.</p> <p>When Explicit IO Power and Ground Terminals are utilized, ensure that all the powers and grounds of the Controller block are connected to do the non-ideal power bus simulation.</p> <p><b>Note:</b> The Memory and Controller blocks cannot co-exist on a canvas. You can add only one out of these two in a topology. In addition, if you have already instantiated a Memory SPICE block, the Memory block option in the floating toolbar appears as disabled.</p>
	Memory SPICE	Topology Explorer, PBA	<p>A Memory SPICE block enables an arbitrary SPICE subcircuit to be used as the Memory block in a Parallel Bus Analysis simulation.</p> <p><b>Note:</b> If you have already instantiated a Memory block, the Memory SPICE block option in the floating toolbar appears as disabled.</p>

## Topology Workbench User Guide

### Choosing Blocks to Place on the Canvas

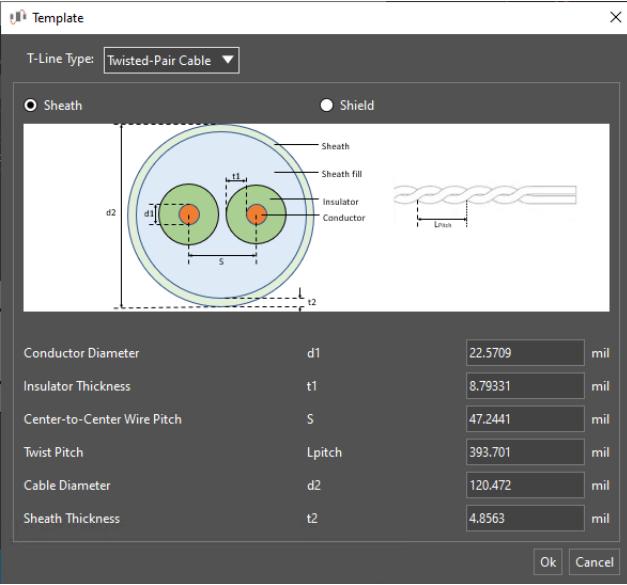
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Block Symbol	Block Name	Workflow	Description
	EBD (Electrical Board Description)	Topology Explorer, PBA	<p>While using Topology Workbench, you can import the EBD models that are as per the IBIS specification. EBD models are imported directly into Topology Workbench and automatically expanded out to include interconnect and referenced component blocks. EBD files are commonly used for modeling DIMMS.</p> <p><i>Important</i></p> <p>Topology Workbench does not support instantiating an EBD block along with a memory block.</p>
	Trace	Topology Explorer, SLA, PBA	<p>The Trace blocks are traces represented by W-Element SPICE syntax.</p> <p>Such blocks are convenient for pre-layout feasibility and trade-off analysis to derive wiring constraints.</p> <p>When a new Trace block is placed on the canvas, the block displays the corresponding single-ended or differential impedance value if there is only one value assigned to it. The impedance value is not shown in case of multiple traces.</p>  <p>For detailed information, refer to <a href="#">Appendix C, “Modeling Pre-Layout Transmission Lines.”</a></p>

## Topology Workbench User Guide

### Choosing Blocks to Place on the Canvas

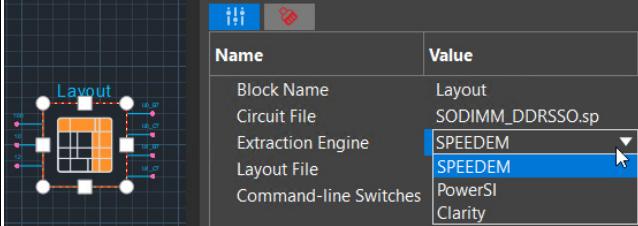
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Block Symbol	Block Name	Workflow	Description																								
	Cable	Topology Explorer, SLA, PBA	<p>The Cable modeler block lets you build twisted-pair cable and coaxial cable SPICE W-element models for simulation in complex topologies like CAN bus for automotive applications.</p> <p>To access the Twisted-Pair Cable or Coaxial Cable definition associated with a Cable modeler block, open the Cable Editor from the Edit Properties panel of the block. Clicking the <i>Input From Template</i> T-Line element from the menu of the Cable Editor opens the Template form where you can define the dimensions of the cable parameters as shown below:</p> <div>  <table border="1"> <tbody> <tr> <td>Conductor Diameter</td> <td>d1</td> <td>22.5709</td> <td>mil</td> </tr> <tr> <td>Insulator Thickness</td> <td>t1</td> <td>8.79331</td> <td>mil</td> </tr> <tr> <td>Center-to-Center Wire Pitch</td> <td>S</td> <td>47.2441</td> <td>mil</td> </tr> <tr> <td>Twist Pitch</td> <td>Lpitch</td> <td>393.701</td> <td>mil</td> </tr> <tr> <td>Cable Diameter</td> <td>d2</td> <td>120.472</td> <td>mil</td> </tr> <tr> <td>Sheath Thickness</td> <td>t2</td> <td>4.8563</td> <td>mil</td> </tr> </tbody> </table> </div> <p>Once the dimensions are specified, the electrical parameters can be defined to build the W-element model. In addition, the parameters can be added to be swept with the Sweep Manager for What-If analysis.</p> <p>After defining the dimensions and electrical parameters, you can select Generate W-Element Model from the Cable Editor to synthesize the model for simulation.</p>	Conductor Diameter	d1	22.5709	mil	Insulator Thickness	t1	8.79331	mil	Center-to-Center Wire Pitch	S	47.2441	mil	Twist Pitch	Lpitch	393.701	mil	Cable Diameter	d2	120.472	mil	Sheath Thickness	t2	4.8563	mil
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## Topology Workbench User Guide

### Choosing Blocks to Place on the Canvas

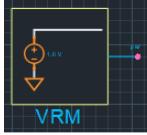
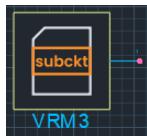
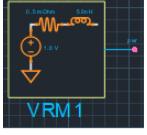
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Block Symbol	Block Name	Workflow	Description
	Layout	Topology Explorer, SLA, PBA, SystemPI (PDN Impedance and Power Ripple Analysis)	<p>The Layout blocks are used for extracting the SPICE database from the layout. You can load .brd, .mcm, and .sip files for layout block. The <i>Extraction Engine</i> list box in the <i>Edit Properties</i> panel lets you specify SPEEDEM, PowerSI, or Clarity engine for the extraction purpose, depending on the workflow in which the Layout block is used and the type of model that has been loaded. For example, when you load an existing S Parameter model by editing the <i>Circuit File</i> property, all available choices are listed for <i>Extraction Engine</i> as show below:</p> <div style="display: flex; align-items: center;">  <p>In Topology Workbench, when you open a legacy topology of .ssix or .top format that has a layout file assigned to a SPICE block, the Layout block is used instead of the SPICE block.</p> </div>
	Via	Topology Explorer, SLA, PBA, SystemPI (DC IR Drop Analysis, PDN Impedance and Power Ripple Analysis)	<p>Use a Via block for vertical layer transitions represented by SPICE subcircuits or S-parameters.</p> <p>For detailed information, refer to <a href="#">Appendix B, "Using the Via Wizard."</a></p>

## Topology Workbench User Guide

### Choosing Blocks to Place on the Canvas

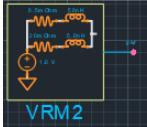
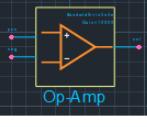
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Block Symbol	Block Name	Workflow	Description																																												
	VRM (Voltage Regulator Module)	Topology Explorer, SLA, PBA, SystemPI (DC IR Drop Analysis, PDN Impedance and Power Ripple Analysis)	<p>Use a VRM block to provide appropriate supply voltage. When you add a VRM block, a netlist file is created. This file uses a model with constant DC voltage having Typical, Minimum and Maximum corners.</p> <p>The following types of VRM blocks are available:</p> <ul style="list-style-type: none"> <li>■ <i>Ideal Supply (VDC) VRM</i>, which is a simple DC model.</li> </ul> <div style="display: flex; align-items: center;">  <table border="1"> <thead> <tr> <th>Name</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>Block Name</td> <td>VRM</td> </tr> <tr> <td>Nominal Voltage</td> <td>1.0 V</td> </tr> <tr> <td colspan="2">▼ Power Net</td> </tr> <tr> <td>Net Name</td> <td>PWR</td> </tr> <tr> <td># of Pins</td> <td>1</td> </tr> <tr> <td>Pin Name</td> <td>pwr</td> </tr> <tr> <td>Pin Resistance(Ohm)</td> <td>0</td> </tr> <tr> <td colspan="2">► Ground Net</td> </tr> </tbody> </table> </div> <ul style="list-style-type: none"> <li>■ <i>Subckt VRM</i>, which is a subcircuit model based on a user-supplied netlist model for a VRM model.</li> </ul> <div style="display: flex; align-items: center;">  <table border="1"> <thead> <tr> <th>Name</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>Block Name</td> <td>VRM3</td> </tr> <tr> <td>Circuit File</td> <td>vrm_Smith.sp</td> </tr> </tbody> </table> </div> <ul style="list-style-type: none"> <li>■ <i>RL VRM</i>, which is a 2-element model with a VDC source with a series resistor (R) and an inductor (L).</li> </ul> <div style="display: flex; align-items: center;">  <table border="1"> <thead> <tr> <th>Name</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>Block Name</td> <td>VRM1</td> </tr> <tr> <td>Nominal Voltage</td> <td>1.0 V</td> </tr> <tr> <td colspan="2">▼ Power Net</td> </tr> <tr> <td>Net Name</td> <td>PWR</td> </tr> <tr> <td># of Pins</td> <td>1</td> </tr> <tr> <td>Pin Name</td> <td>pwr</td> </tr> <tr> <td>R_VRM(Ohm)</td> <td>0.5m</td> </tr> <tr> <td>L_VRM(H)</td> <td>50n</td> </tr> <tr> <td colspan="2">► Ground Net</td> </tr> </tbody> </table> </div>	Name	Value	Block Name	VRM	Nominal Voltage	1.0 V	▼ Power Net		Net Name	PWR	# of Pins	1	Pin Name	pwr	Pin Resistance(Ohm)	0	► Ground Net		Name	Value	Block Name	VRM3	Circuit File	vrm_Smith.sp	Name	Value	Block Name	VRM1	Nominal Voltage	1.0 V	▼ Power Net		Net Name	PWR	# of Pins	1	Pin Name	pwr	R_VRM(Ohm)	0.5m	L_VRM(H)	50n	► Ground Net	
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► Ground Net																																															
Name	Value																																														
Block Name	VRM3																																														
Circuit File	vrm_Smith.sp																																														
Name	Value																																														
Block Name	VRM1																																														
Nominal Voltage	1.0 V																																														
▼ Power Net																																															
Net Name	PWR																																														
# of Pins	1																																														
Pin Name	pwr																																														
R_VRM(Ohm)	0.5m																																														
L_VRM(H)	50n																																														
► Ground Net																																															

## Topology Workbench User Guide

### Choosing Blocks to Place on the Canvas

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Block Symbol	Block Name	Workflow	Description																																														
			<ul style="list-style-type: none"> <li>■ <i>RL//RL VRM</i>, which is a 4-element model with a VDC source with a parallel combination of the series resistor and inductor as in the 2-element model.</li> </ul> <div style="display: flex; justify-content: space-between;"> <div style="flex: 1;">  <p><b>VRM2</b></p> </div> <div style="flex: 1;"> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Name</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>Block Name</td> <td>VRM2</td> </tr> <tr> <td>Nominal Voltage</td> <td>1.0 V</td> </tr> <tr> <td colspan="2">▼ Power Net</td> </tr> <tr> <td>Net Name</td> <td>PWR</td> </tr> <tr> <td># of Pins</td> <td>1</td> </tr> <tr> <td>Pin Name</td> <td>pwr</td> </tr> <tr> <td>R_VRM(Ohm)</td> <td>0.5m</td> </tr> <tr> <td>L_VRM(H)</td> <td>50n</td> </tr> <tr> <td>R_damp(Ohm)</td> <td>20m</td> </tr> <tr> <td>L_VRM/10(H)</td> <td>5.0n</td> </tr> <tr> <td colspan="2">► Ground Net</td> </tr> </tbody> </table> </div> </div> <p>In the Topology Explorer and SystemPI workflows, the following two operational amplifier (Op-Amp) blocks are also available to model voltage regulator modules (VRM) more accurately:</p> <ul style="list-style-type: none"> <li>■ <i>Ideal Op-Amp</i>, which is a model with a simple voltage-controlled voltage source (VCVS) with an input impedance resistor and output impedance resistor.</li> </ul> <div style="display: flex; justify-content: space-between;"> <div style="flex: 1;">  <p><b>Op-Amp</b></p> </div> <div style="flex: 1;"> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Name</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>Block Name</td> <td>Op-Amp</td> </tr> <tr> <td>Input Impedance</td> <td>1e7Ohm</td> </tr> <tr> <td>Gain</td> <td>10000</td> </tr> <tr> <td>Output Impedance</td> <td>0.1 Ohm</td> </tr> </tbody> </table> </div> </div> <ul style="list-style-type: none"> <li>■ <i>Bandwidth-Limited Op-Amp</i>, which is a model with an ideal op-amp with a bandwidth limit.</li> </ul> <div style="display: flex; justify-content: space-between;"> <div style="flex: 1;">  <p><b>Op-Amp1</b></p> </div> <div style="flex: 1;"> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Name</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>Block Name</td> <td>Op-Amp1</td> </tr> <tr> <td>Input Impedance</td> <td>2e6Ohm</td> </tr> <tr> <td>Gain</td> <td>2e5</td> </tr> <tr> <td>Bandwidth</td> <td>1e6Hz</td> </tr> <tr> <td>Output Impedance</td> <td>0.1 Ohm</td> </tr> </tbody> </table> </div> </div> <p><b>Note:</b> In SPICE format expressions, <code>M</code> is treated as <code>Milli</code> instead of <code>Mega</code>.</p>	Name	Value	Block Name	VRM2	Nominal Voltage	1.0 V	▼ Power Net		Net Name	PWR	# of Pins	1	Pin Name	pwr	R_VRM(Ohm)	0.5m	L_VRM(H)	50n	R_damp(Ohm)	20m	L_VRM/10(H)	5.0n	► Ground Net		Name	Value	Block Name	Op-Amp	Input Impedance	1e7Ohm	Gain	10000	Output Impedance	0.1 Ohm	Name	Value	Block Name	Op-Amp1	Input Impedance	2e6Ohm	Gain	2e5	Bandwidth	1e6Hz	Output Impedance	0.1 Ohm
Name	Value																																																
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## Topology Workbench User Guide

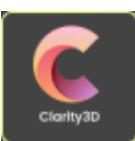
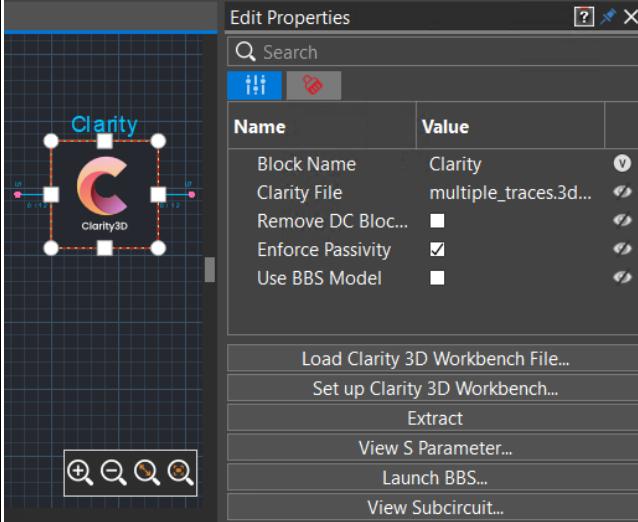
### Choosing Blocks to Place on the Canvas

Block Symbol	Block Name	Workflow	Description
	S Parameter	Topology Explorer, SLA, PBA, SystemPI (DC IR Drop Analysis, PDN Impedance Analysis, and Power Ripple Analysis)	<p>Place an S Parameter block on the canvas to add a general purpose block that can contain an S Parameter.</p> <p>When a Touchstone format model is loaded on an S Parameter block, the block displays multiple connection ports to enable making connections with multiple memory blocks.</p> <p>You can set up the default pin locations for a S Parameter block as described in the <a href="#">Setting Up the Default Pin Location</a> section of <a href="#">Chapter 2, “Working with Topologies.”</a></p> <p>See also the <a href="#">Assigning and Extracting S Parameter Files</a> section of <a href="#">Chapter 2, “Working with Topologies.”</a></p> <p> <b>Caution</b></p> <p><b><i>Editing of .sp file for the S Parameters is NOT recommended.</i></b></p>
	SPICE Subcircuit	Topology Explorer, SLA, PBA, SystemPI (DC IR Drop Analysis, PDN Impedance Analysis, and Power Ripple Analysis)	<p>This is a general purpose block that can contain an arbitrary SPICE subcircuit.</p> <p><b>Note:</b> You can set up the default pin locations for a SPICE subcircuit. The process is the same way as is described for an S Parameter block in the <a href="#">Setting Up the Default Pin Location</a> section of <a href="#">Chapter 2, “Working with Topologies.”</a></p>

## Topology Workbench User Guide

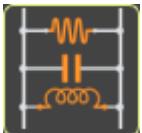
### Choosing Blocks to Place on the Canvas

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Block Symbol	Block Name	Workflow	Description
	Clarity3D	Topology Explorer, SLA, PBA, SystemPI (DC IR Drop Analysis, PDN Impedance and Power Ripple Analysis)	<p>Use to add Clarity3DWB component to edit the Clarity 3D Workbench properties from the Topology Workbench interface.</p>  <p>You can do the following from the Edit Properties panel for a Clarity3D block:</p> <ul style="list-style-type: none"> <li>■ Load Clarity 3D Workbench file of one of the following supported formats – .3dem, .spd, .brd, .mcm, and .sip.</li> <li>■ Set up the assigned Clarity model in Clarity 3D Workbench.</li> <li>■ Sweep Clarity 3D Workbench parameters using the Sweep Manager.</li> <li>■ Set up Clarity 3D Workbench parameters for optimization in Optimality.</li> </ul>

## Topology Workbench User Guide

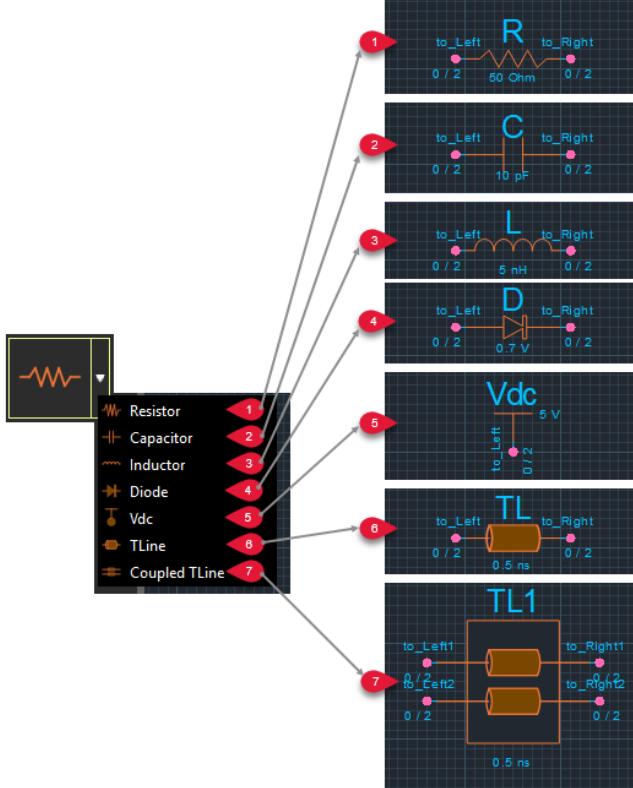
### Choosing Blocks to Place on the Canvas

Block Symbol	Block Name	Workflow	Description
	Discrete	Topology Explorer, SLA, PBA, SystemPI (DC IR Drop Analysis, PDN Impedance Analysis, and Power Ripple Analysis)	By default, the discrete block represents a resistor. You can modify the block properties to represent other discrete components, such as, capacitors and inductors.
	Terminator	Topology Explorer, SLA, PBA	Use this block to add terminations to the design. The supported termination types include <i>ShuntR</i> , <i>ShuntRC</i> , <i>SeriesR</i> , <i>Thevenin</i> , <i>DualClamp</i> , <i>HiClamp</i> , <i>LowClamp</i> , and <i>VoltageSource</i> .
	FDTD-D (Finite Difference Time Domain)	Topology Explorer, SLA, PBA	An FDTD-D block allows a physical layout to be specified for the SpeedEM engine in an "FDTD-direct" simulation.  <b>Note:</b> You can add only one FDTD-D block to the topology.  You can set up the default pin locations for a FDTD-D block as described in the <a href="#"><u>Setting Up the Default Pin Location</u></a> section of Chapter 2, "Working with Topologies."

## Topology Workbench User Guide

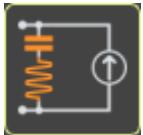
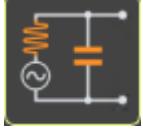
### Choosing Blocks to Place on the Canvas

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Block Symbol	Block Name	Workflow	Description
	<b>Ideal Elements</b>	Topology Explorer, SLA, PBA, SystemPI (DC IR Drop Analysis, PDN Impedance Analysis, and Power Ripple Analysis)	<p>You can use the ideal elements block to place Resistor, Capacitor, Inductor, Diode, Vdc, TLine, and Coupled TLine in the topology. Ideal elements of all types except Coupled TLine do not have borders. You cannot resize the ideal elements and their pins are fixed.</p> <div style="display: flex; align-items: center;">  <p><b>Note:</b> When you open a legacy SigXplorer topology in Topology Workbench, the discrete blocks are automatically replaced by ideal elements.</p> </div>

## Topology Workbench User Guide

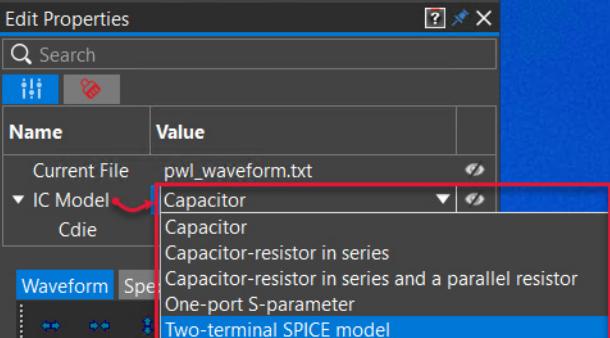
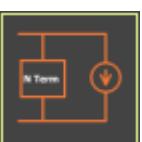
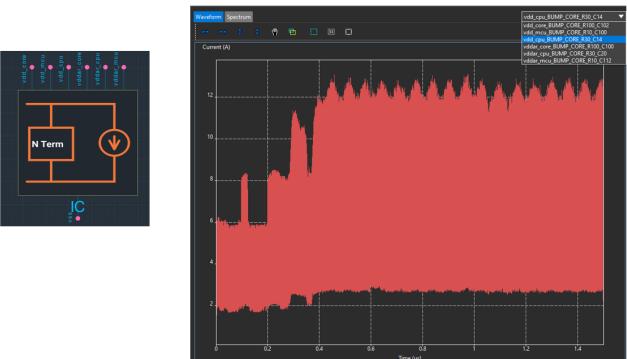
### Choosing Blocks to Place on the Canvas

Block Symbol	Block Name	Workflow	Description
	PI Current Source	Topology Explorer	<p>Current sources are useful for power integrity analysis. These enable excitation currents to be applied to a power distribution network (PDN) to observe voltage ripple in the time domain.</p> <p>By default, the current source block generates the Gaussian waveform. In the <i>Edit Properties</i> panel, you can specify the waveform shape and modify the parameter values to tweak the waveform shapes.</p>
	PI Voltage Source	Topology Explorer	<p>By default, the voltage source block generates the Gaussian waveform – similar to a current-source block. Using the <i>Edit Properties</i> panel, you can modify the default output by specifying a different waveform shape or by modifying the parameter values to tweak the waveform shapes.</p>
	Sink	SystemPI (DC IR Drop Analysis)	<p>Use the Sink block to designate a consumer of power for IR drop analysis.</p>

## Topology Workbench User Guide

### Choosing Blocks to Place on the Canvas

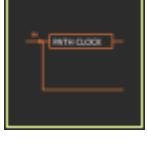
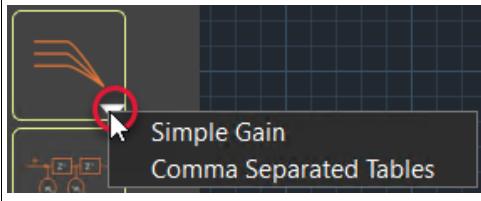
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Block Symbol	Block Name	Workflow	Description
	IC	SystemPI (PDN Impedance Analysis and Power Ripple Analysis)	<p>Use single or multiple IC blocks with alternating current (AC) sources to load PWL files and assign die models of the following types:</p> <ul style="list-style-type: none"> <li>■ Generic IC power models – Capacitor, Capacitor-resistor in series, Capacitor-resistor in series, two-terminal SPICE subcircuit model, one-port S Parameter</li> <li>■ Generic IC current models – Piecewise Linear (PWL)</li> </ul> <p>You can specify the IC block type in the <i>Edit Properties</i> panel.</p> 
	N-Terminal IC	SystemPI (PDN Impedance Analysis and Power Ripple Analysis)	<p>The N-Terminal IC block supports multi-terminal SPICE and Voltus models for IC blocks. It enables grid-based extractions. You can also view and edit the current profile for each terminal.</p> 

## Topology Workbench User Guide

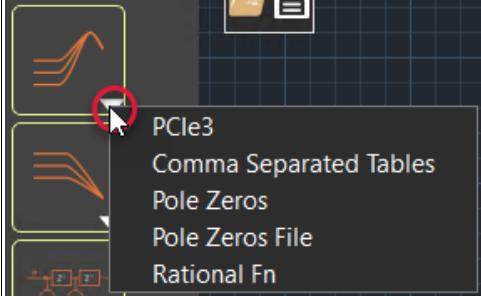
### Choosing Blocks to Place on the Canvas

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<b>Block Symbol</b>	<b>Block Name</b>	<b>Workflow</b>	<b>Description</b>
	GAIN	AMI Builder (Tx Model)	Use the GAIN block to model amplification in an IBIS-AMI model with AMI Builder.
	Custom	AMI Builder (Tx and Rx Models)	Use the Custom block to incorporate custom code in an IBIS-AMI model with AMI Builder
	FFE	AMI Builder (Tx and Rx Models)	Use the FFE block to model feed forward equalization in an IBIS-AMI model with AMI Builder.
	Path Clock	AMI Builder (Rx Model)	<p>Use the Path Clock block to model a separate clock path in an IBIS-AMI model with AMI Builder.</p> <p><b>Note:</b> Only one path clock can be added to a canvas.</p>
	AGC	AMI Builder (Rx Model)	<p>Use the AGC block to model automatic gain control (that is, variable gain amplification or VGA) in an IBIS-AMI model with AMI Builder.</p> <p>Topology Workbench provides support for the following types of AGC blocks—<i>Simple Gain</i> and <i>Comma Separate Tables</i>. To choose the type of AGC block you want to instantiate, click the drop-down list icon on the block and select the required option.</p>  <p>By default, a <i>Simple Gain</i> AGC block is selected for instantiation.</p>

## Topology Workbench User Guide

### Choosing Blocks to Place on the Canvas

Block Symbol	Block Name	Workflow	Description
	CTE	AMI Builder (Rx Model)	<p>Use the CTE block to model continuous time equalization in an IBIS-AMI model with AMI Builder.</p> <p>Topology Workbench provides support for the following types of CTE blocks—<i>PCIe3</i>, <i>Comma Separate Tables</i>, <i>Pole Zeros</i>, <i>Pole Zeros File</i>, and <i>Rational Fn</i>. To choose the type of CTE block you want to instantiate, click the drop-down list icon on the block and select the required option.</p>  <p>By default, a <i>PCIe3</i> CTE block is selected for instantiation.</p>

## **Topology Workbench User Guide**

### Choosing Blocks to Place on the Canvas

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## **Using the Via Wizard**

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To run the Via Wizard, ensure that:

- you have installed the Sigrity 2019 HF1 or later release in addition to the Allegro® 17.4-2019 QIR1 or later release.
- you have a Sigrity Aurora license or an Advanced SI license along with a Clarity license. For assistance, contact your Cadence Customer Support representative.

This section introduces the usage of the two types of Via Wizards to generate via models in pre-layout phase.

### **Related Topics**

- [Placing a Via Block](#)
- [Sigrity Via Wizard](#)
- [Aurora Via Wizard](#)

### **Placing a Via Block**

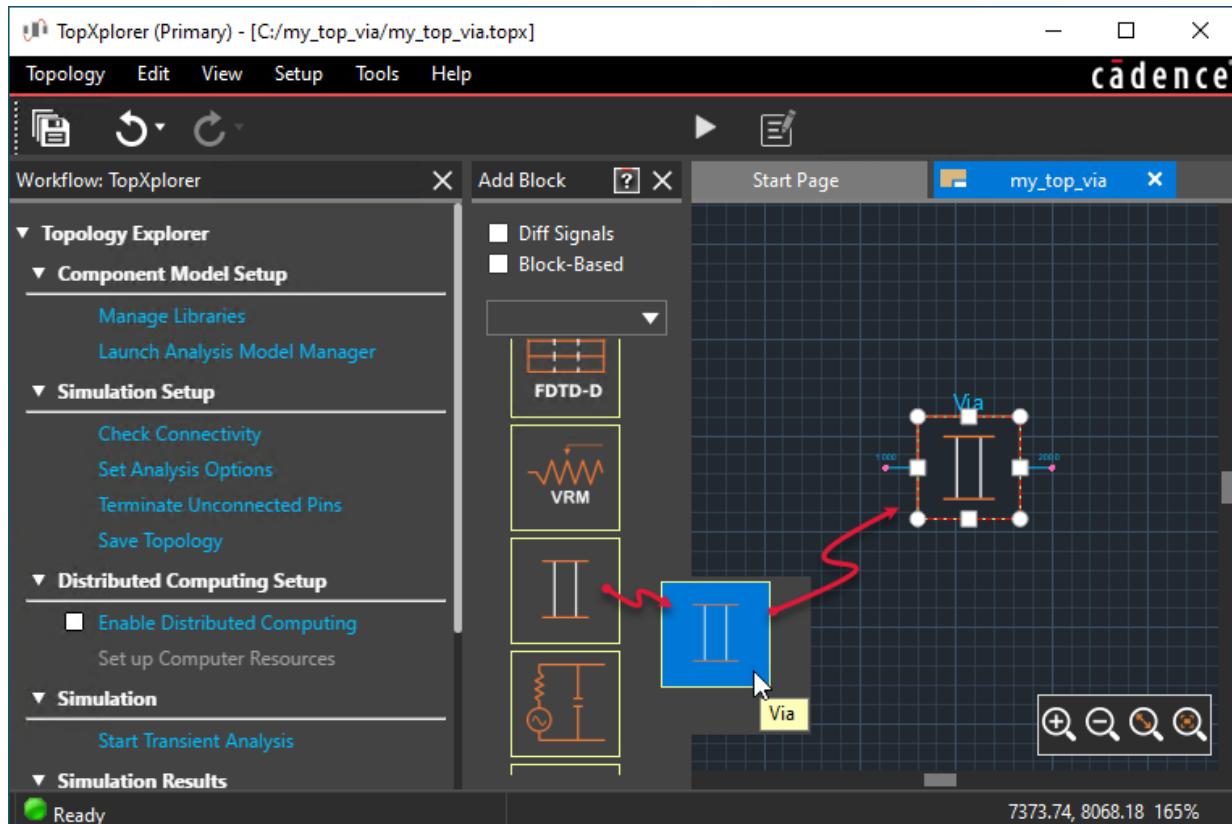
To place a Via block in Topology Workbench:

1. Click the Via block button in the [Floating Toolbar](#).

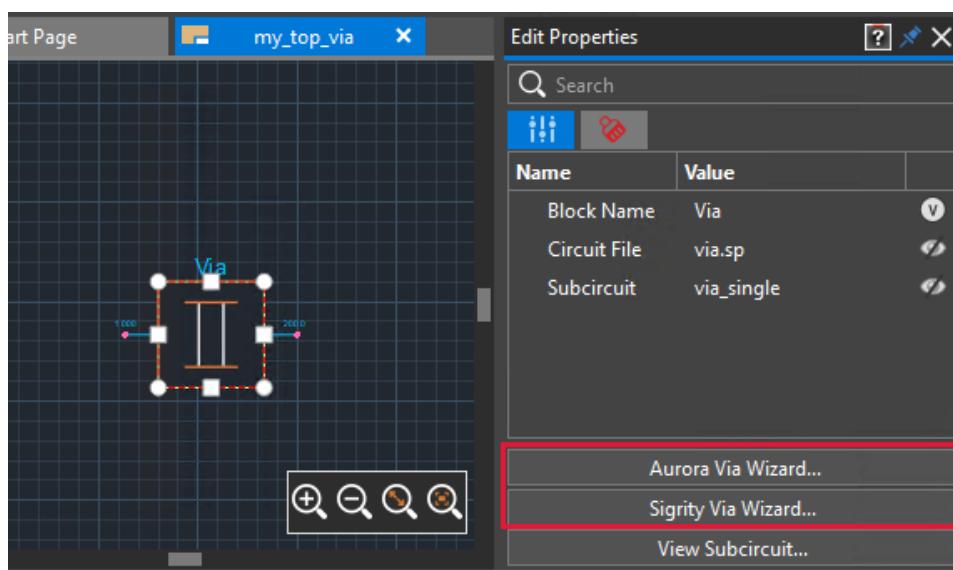
# Topology Workbench User Guide

## Using the Via Wizard

2. Drag the pointer to the canvas and click the canvas where the Via block needs to be placed.



3. Double-click the block to open the Edit Properties Panel and give it a unique name.



The *Edit Properties* panel for a via block lets you choose from the following two types of wizards to define parameters of a via structure and generate a via model:

- [Sigrity Via Wizard](#)
- [Aurora Via Wizard](#)

## Sigrity Via Wizard

This section introduces the usage of the Sigrity Via Wizard to generate coupled via models in pre-layout phase.

**Note:** When using a Sigrity 2019 HF<n> installation, pre-defined layout templates for the Sigrity Via Wizard can be found at the following location:

<SIGRITY\_INSTALL\_DIR>\share\library\template\SystemExplorer\ViaWizard\stackups

However, in Sigrity 2021, these pre-defined layout templates have been removed from the installation. You can alternatively access them from the following path in the Allegro 17.4-2019 installation:

<ALLEGRO\_INSTALL\_DIR>\share\topxp\ViaWizard\stackups

### **Related Topics**

- [Defining the Via Structure](#)
- [Generating the Via Model](#)

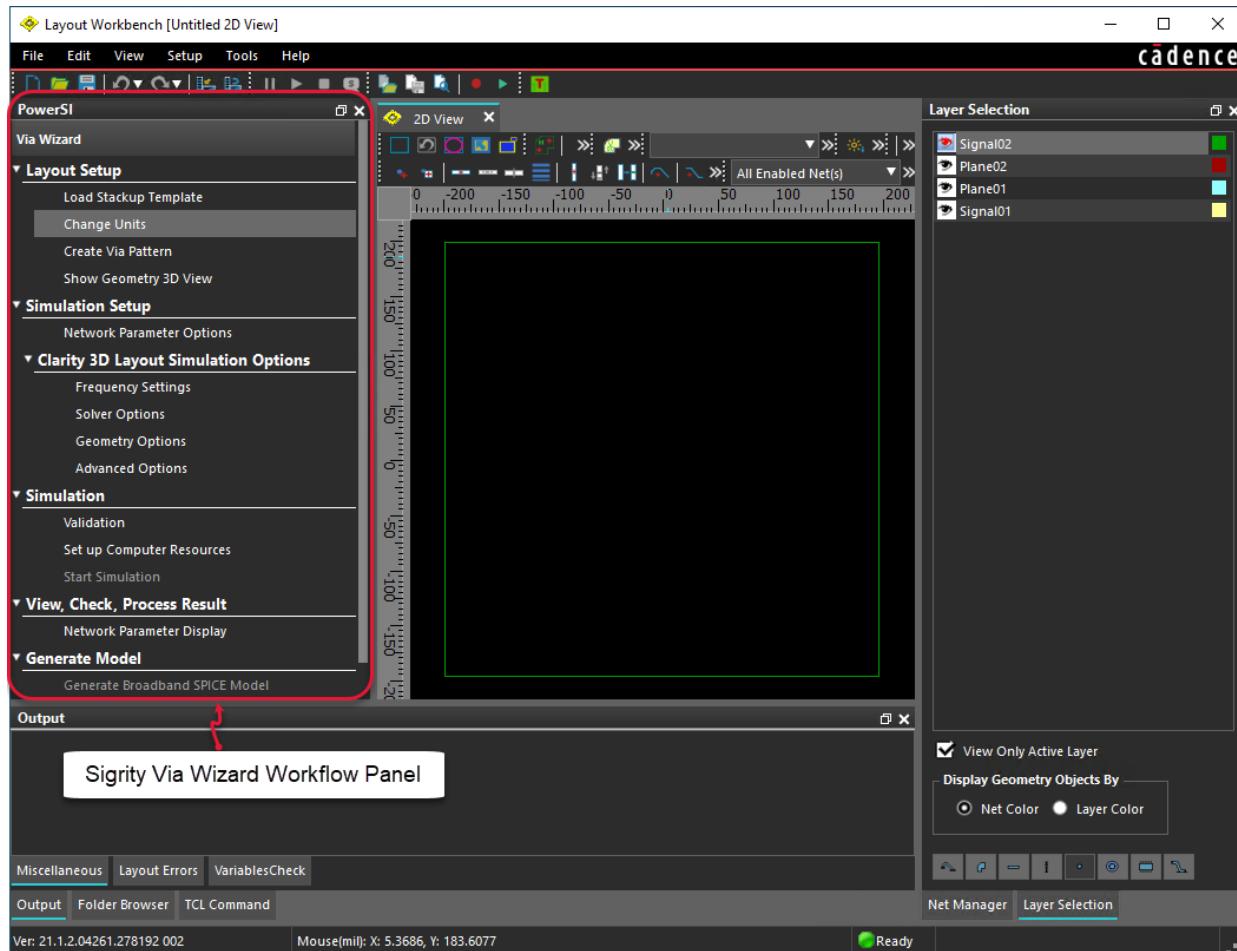
## Defining the Via Structure

To define a via structure using Sigrity Via Wizard:

# Topology Workbench User Guide

## Using the Via Wizard

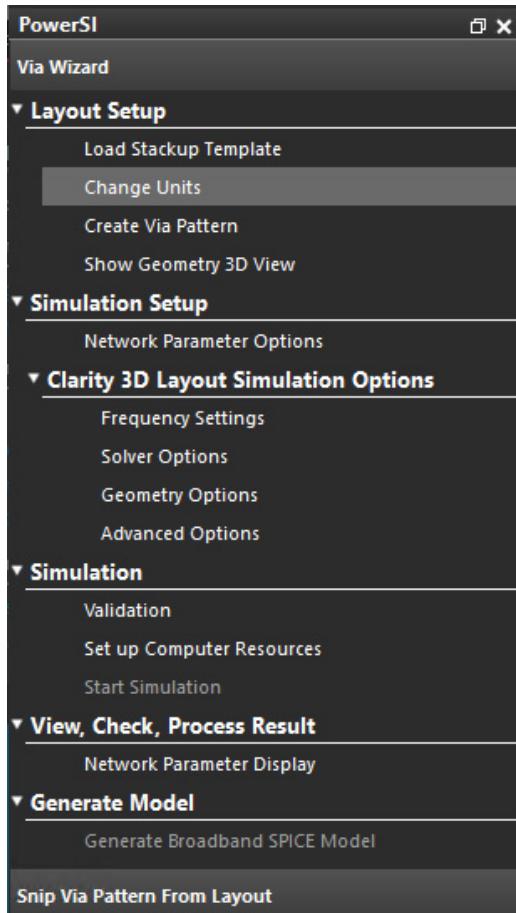
- Click the *Sigrity Via Wizard* button in the *Edit Properties* panel. The Layout Workbench window opens with the *Via Wizard* workflow panel displayed in it.



# Topology Workbench User Guide

## Using the Via Wizard

The *Sigrity Via Wizard* provides its own workflow to support the via modeling process.



The following sections provide a walk-through example of this process:

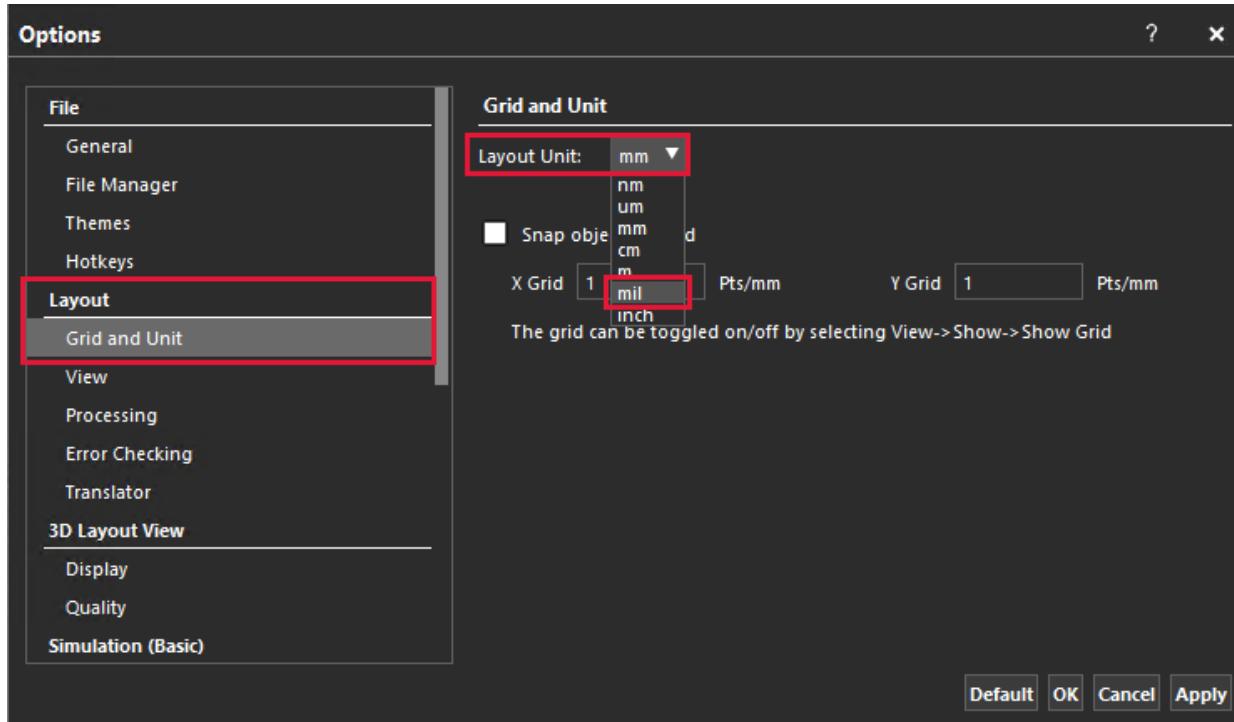
- [Changing the Units](#)
- [Defining the Stack-Up](#)
- [Defining the Pad Stack](#)
- [Defining the Options](#)
- [Defining the Via Pattern](#)
- [Reviewing the 3D Structure](#)

# Topology Workbench User Guide

## Using the Via Wizard

### Changing the Units

1. Click *Change Units* in the *Workflow* panel. The *Options* form opens with *Grid and Unit* selected in the *Layout* schema.
2. Choose *mil* for *Layout Unit*.



3. Click *OK* to save the change and close the *Options* form.

### Defining the Stack-Up

After you have loaded the required stack-up template:

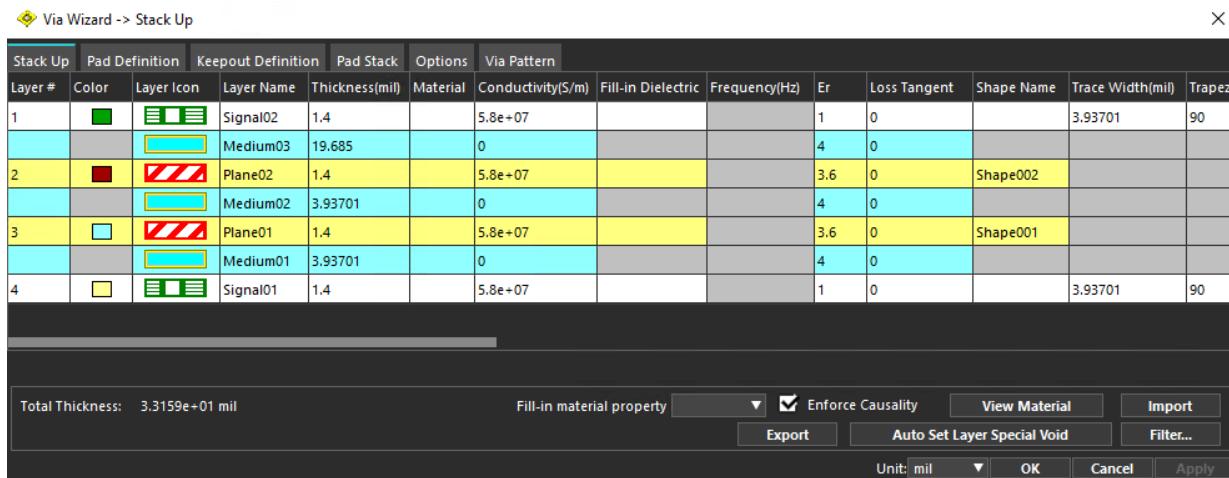
1. Click *Create Via Pattern* in the *Workflow* panel. The *Via Wizard -> Via Pattern* dialog box opens.

## Topology Workbench User Guide

### Using the Via Wizard

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2. Click the *Stack Up* tab. The dialog box's title changes to *Via Wizard -> Stack Up* and a table showing information related to stack-up layers is displayed.



Stack Up	Pad Definition		Keepout Definition		Pad Stack		Options		Via Pattern					
Layer #	Color	Layer Icon	Layer Name	Thickness(mil)	Material	Conductivity(S/m)	Fill-in Dielectric	Frequency(Hz)	Er	Loss Tangent	Shape Name	Trace Width(mil)	Trapez	
1	<span style="color: green;">█</span>		Signal02	1.4		5.8e+07			1	0		3.93701	90	
2	<span style="color: black;">█</span>		Medium03	19.685		0			4	0				
3	<span style="color: red;">█</span>		Plane02	1.4		5.8e+07			3.6	0	Shape002			
4	<span style="color: cyan;">█</span>		Medium02	3.93701		0			4	0				
5	<span style="color: cyan;">█</span>		Plane01	1.4		5.8e+07			3.6	0	Shape001			
6	<span style="color: yellow;">█</span>		Medium01	3.93701		0			4	0				
7	<span style="color: yellow;">█</span>		Signal01	1.4		5.8e+07			1	0		3.93701	90	

Total Thickness: 3.3159e+01 mil

Fill-in material property ▾  Enforce Causality      Unit: mil ▾

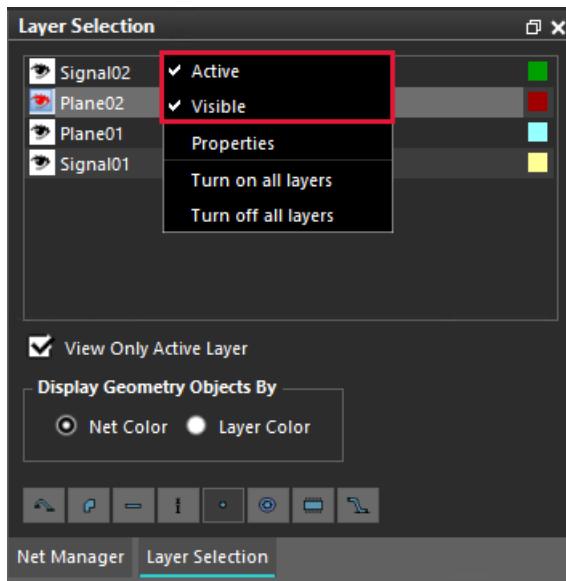
3. Edit the stack-up layers, thickness, and material properties as per your design requirements.
4. Click *OK* when finished with the stack-up definition. The *Via Wizard -> Stack Up* dialog box closes.

When you add plane layers to the stack-up, a shape is automatically added to that layer (for example, *Plane02* adds *Shape002* in the image above). The plane shapes need to be assigned to the GND net.

## Topology Workbench User Guide

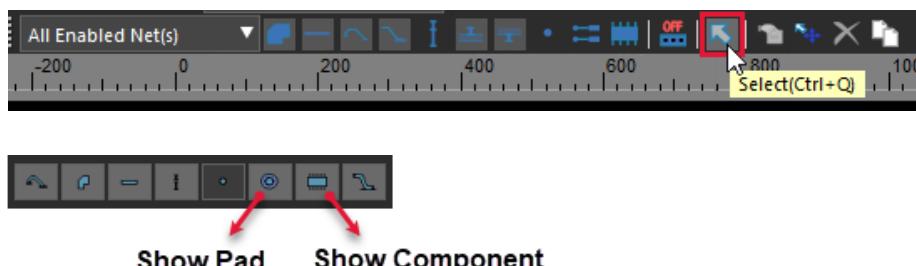
### Using the Via Wizard

5. Make each plane active and visible for review in the *Layer Selection* pane as shown below:



6. Select a plane in the *Layer Selection* pane. For example, assume that you select *Plane02*.

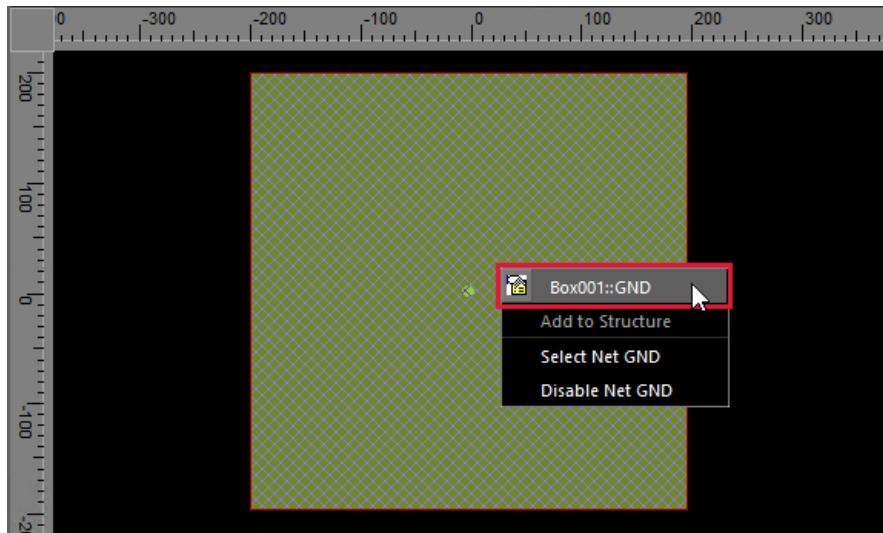
**Note:** Ensure that you have the *Select* option enabled in the toolbar, and the *Show Pad* and *Show Component* options enabled in the *Layer Selection* pane, as shown below:



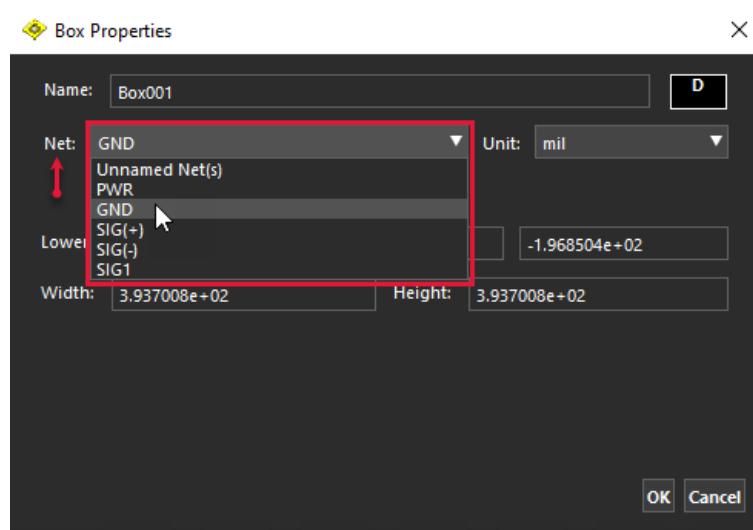
## Topology Workbench User Guide

### Using the Via Wizard

7. Right-click the shape on the canvas to verify the net assigned to the selected plane's shape.



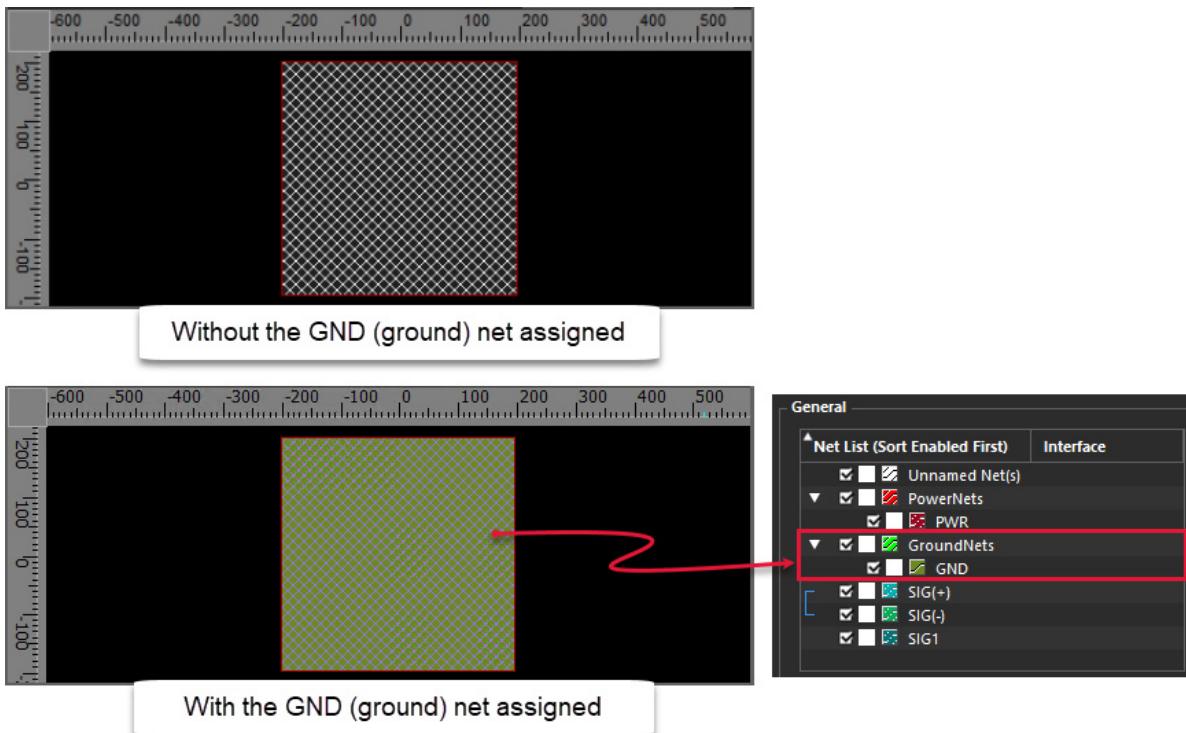
The `<shape_name>::<net_name>` option in the displayed shortcut menu indicates whether the shape has the GND net assigned to it. If it is not, then click `<shape_name>::<net_name>` option to open the *Box Properties* dialog box as shown below and reset the *Net* from the list to *GND*:



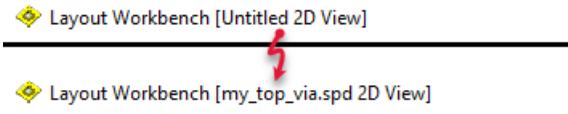
## Topology Workbench User Guide

### Using the Via Wizard

In the example given above, the GND net was already assigned. The following image also shows the difference you can notice in the shape when the GND net is not assigned.



8. Repeat this procedure as needed to assign all the plane shapes to the ground net, *GND*.
9. Choose *File – Save As* in the main menu and save the file to your working directory. The name of the saved file starts to display in the window title as shown below:



**Note:** You can additionally save the stack-up template to another location for future reuse using the same *File – Save As* method. The location can be in the standard location described earlier, or a local library. It is however recommended that you use similar naming conventions to facilitate stack-up selection for future projects.

For more information on stack-up editing, refer to the *PowerSI Getting Started Guide*.

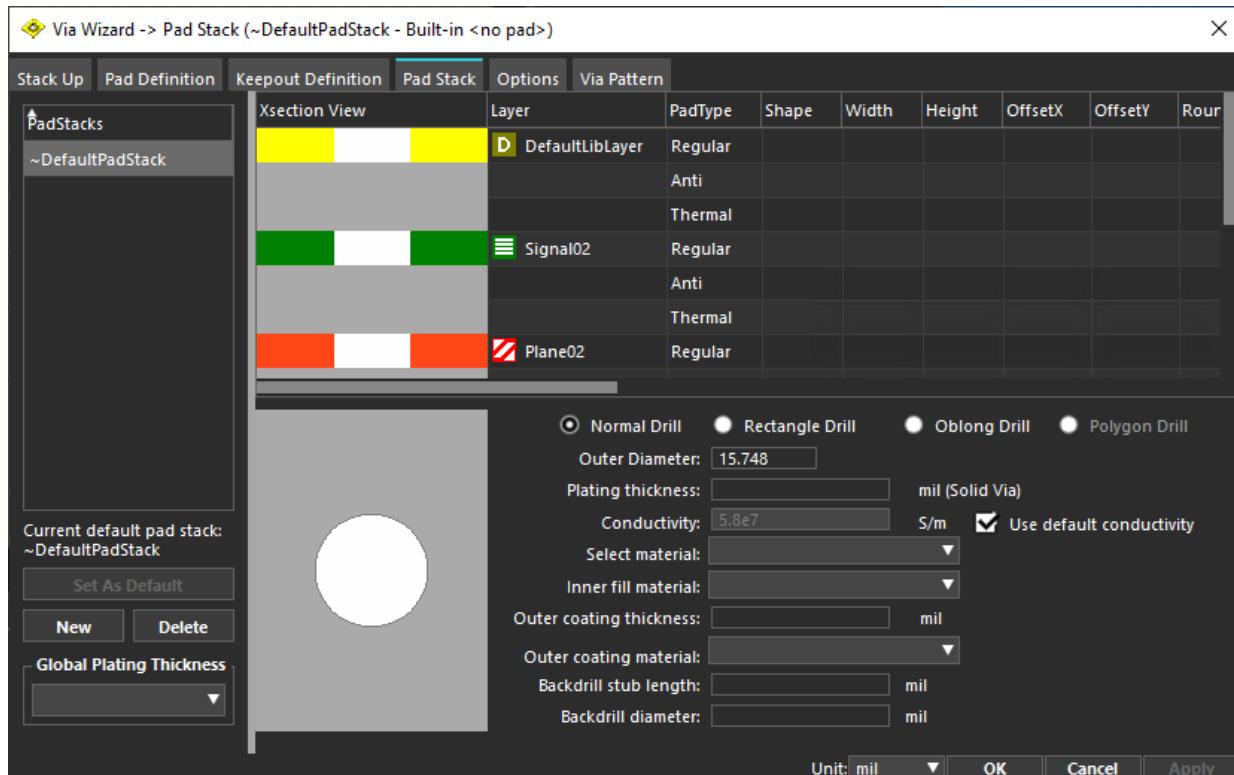
### Defining the Pad Stack

With the stack-up now in place, perform the following steps to define the pad stack:

# Topology Workbench User Guide

## Using the Via Wizard

1. Click *Create Via Pattern* in the *Workflow* panel.
2. Select the *Pad Stack* tab.



3. Review the default definitions of the pad stack.
4. Click *OK*.

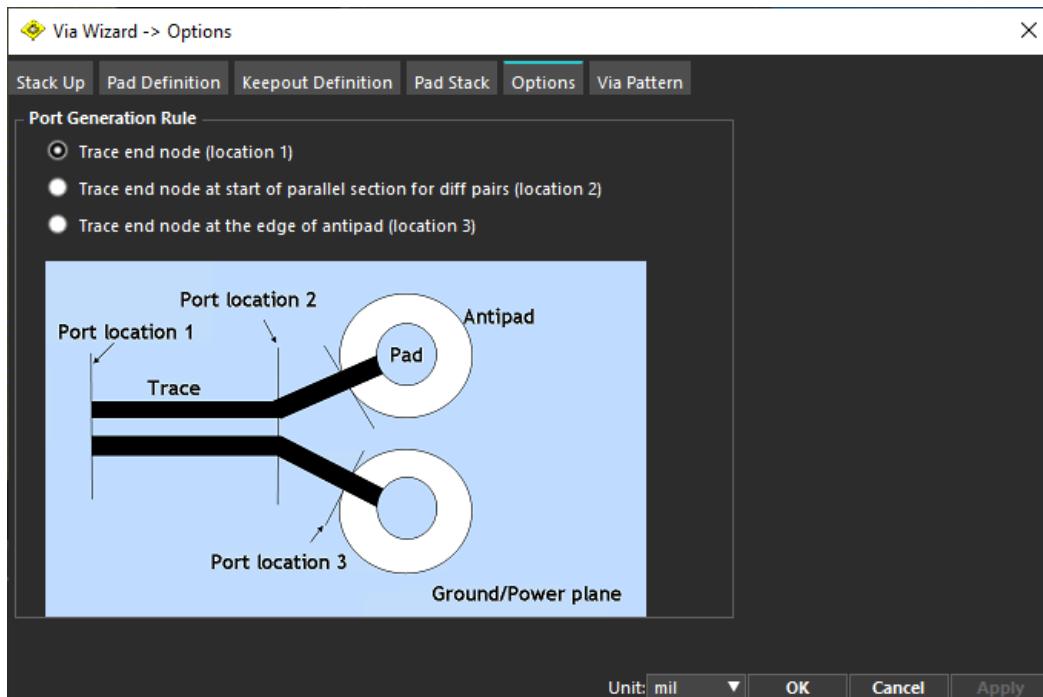
## Defining the Options

1. Click *Create Via Pattern* in the *Workflow* panel.
2. Click the *Options* tab.

## Topology Workbench User Guide

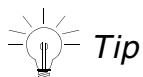
### Using the Via Wizard

3. Select *Trace end node (location 1)* as port generation rule.



4. Click *Apply*.

**Note:** The *Apply* button appears enabled when you select an option other than *Trace end node (location 1)*, which is selected by default.



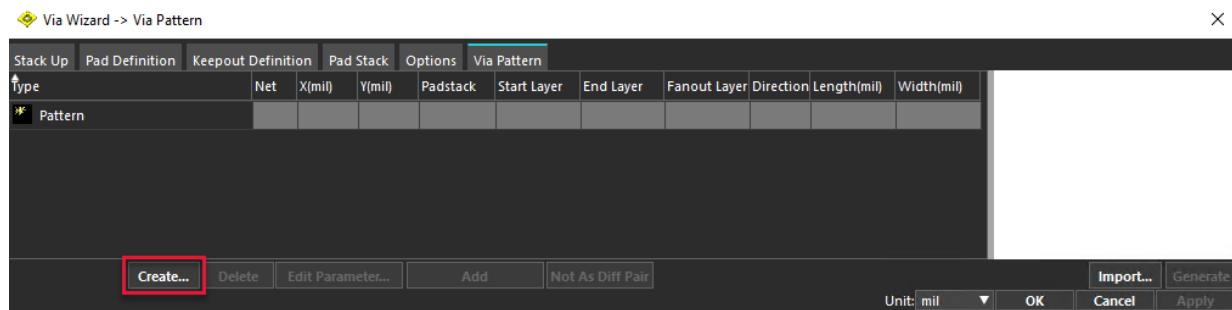
Do not close the *Via Wizard* dialog box. Proceed to the steps given in the next section.

# Topology Workbench User Guide

## Using the Via Wizard

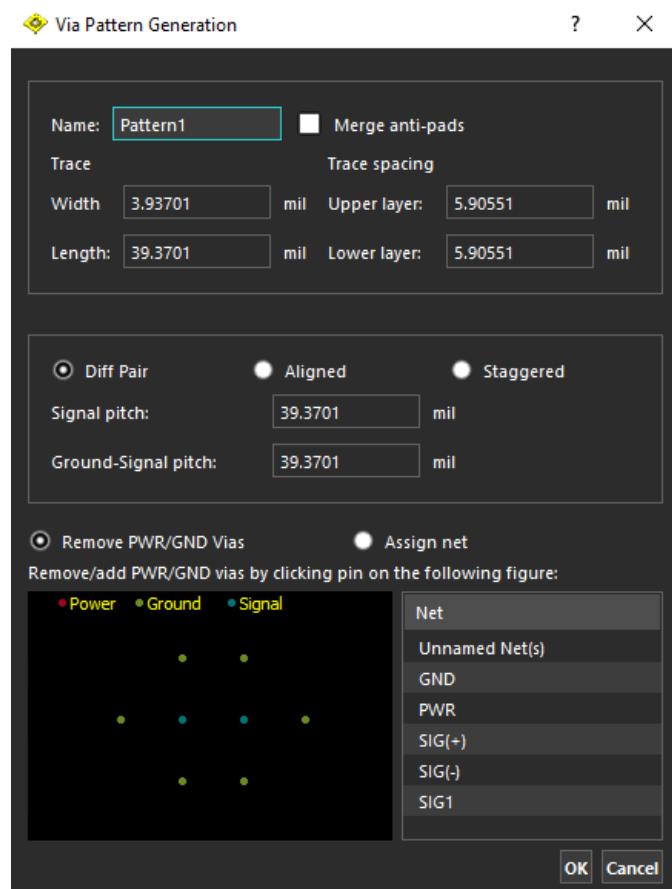
### Defining the Via Pattern

1. Click the *Via Pattern* tab.



This tab allows you to quickly create a pattern for multiple vias. For this example, create a common via pattern for a differential pair.

2. Click *Create*. The *Via Pattern Generation* dialog box opens.



3. Define a name for your via pattern.

## Topology Workbench User Guide

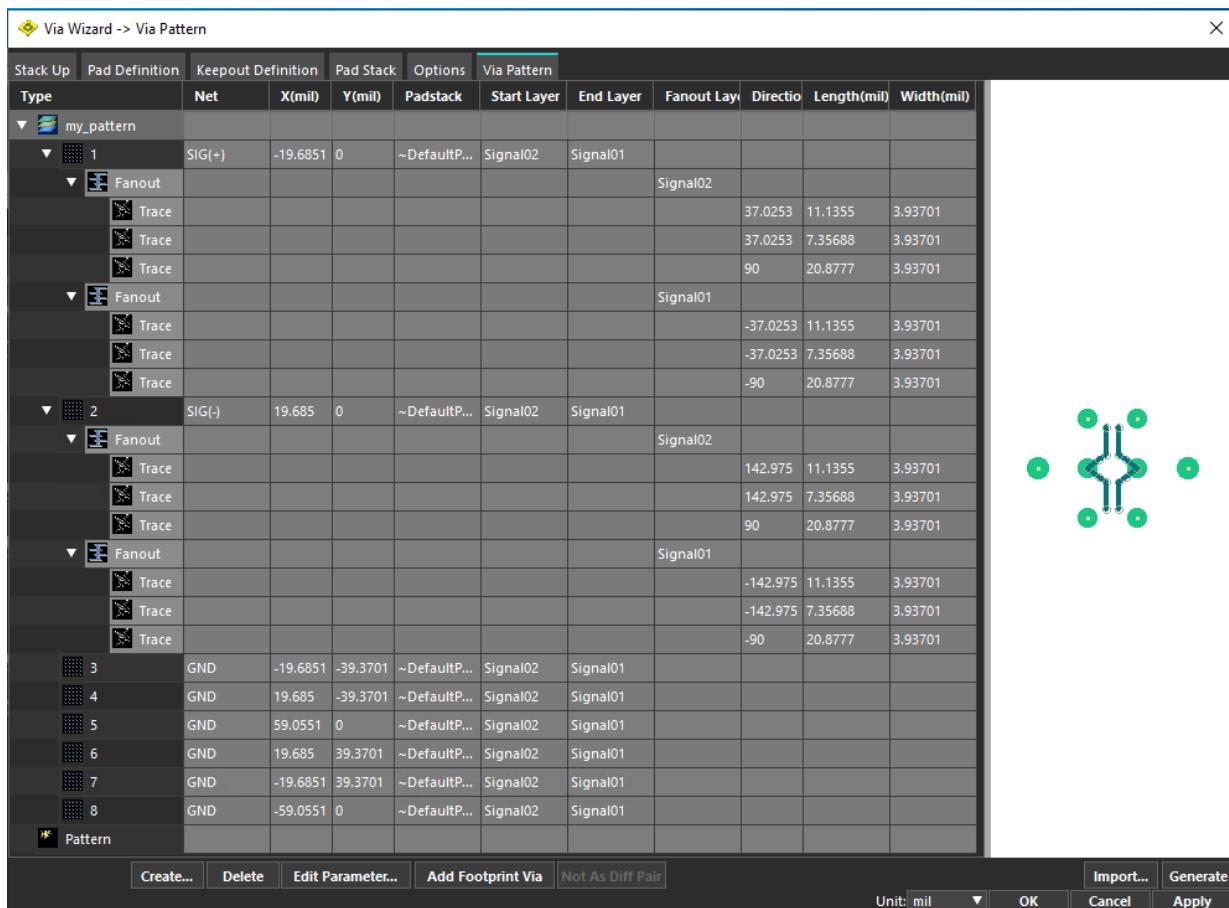
### Using the Via Wizard

4. Set the trace parameters and via-to-via pitch geometry as desired.

On selecting the *Diff Pair* configuration, a default pattern of 2 signals and 6 ground vias is created. *SIG(+)* and *SIG(-)* nets are automatically assigned to the signals, and *GND* is assigned to the surrounding vias. If required, you can change the default configuration by adding or removing the ground vias.

For example, if needed, you can click the two GND vias at the top and the two at the bottom of the diagram to remove them, and leave the left and right GND vias in place.

5. Click *OK* to save close the *Via Pattern Generation* dialog box.

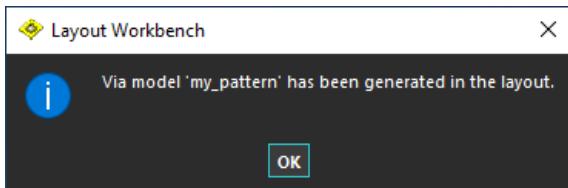


The via pattern is populated into the table as shown above, along with a “bird’s eye” preview of the structure in the right pane. Items in the spreadsheet can be edited to modify the structure.

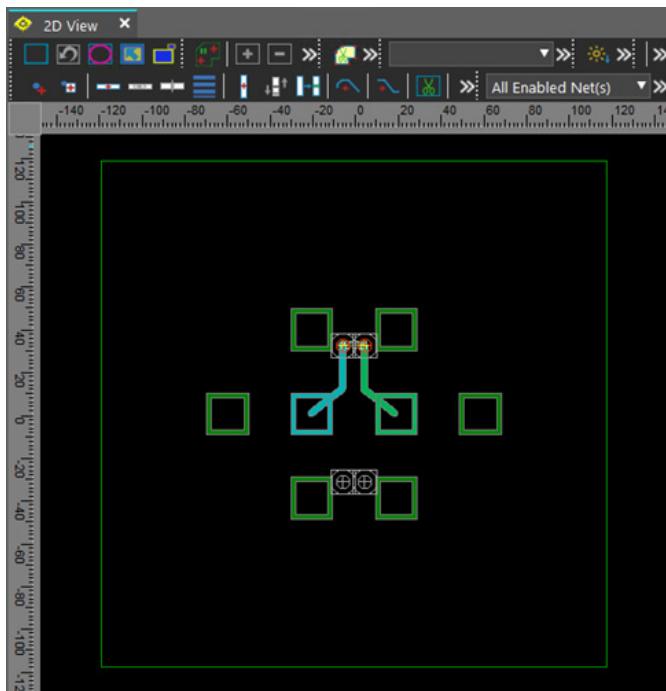
## Topology Workbench User Guide

### Using the Via Wizard

6. Click the *Generate* button to create the defined via pattern in the blank layout. On completion of the process, a message box is shown.



7. Click *OK* to close the message box.
8. Click *OK* to close the *Via Pattern* dialog box. The layout in the *2D View* tab is refreshed based on the pattern you generated as shown below:



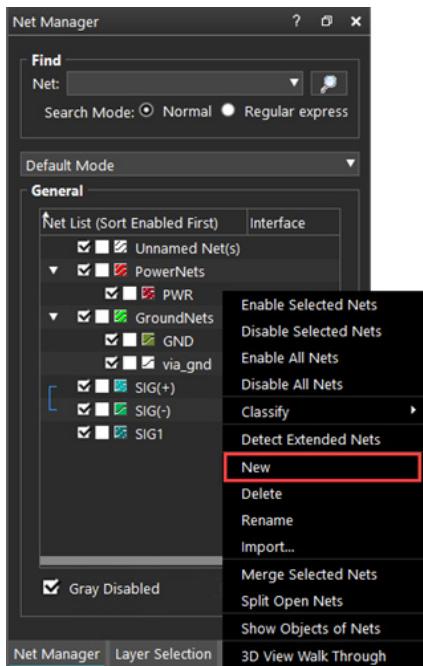
The example covered above is for the *Diff Pair* configuration. For the *Aligned* and *Staggered* patterns, you might want to define additional signals to use with the various vias. In this case, before generating the via pattern, perform the steps given below:

1. Click the *Net Manager* tab right pane of the main window.

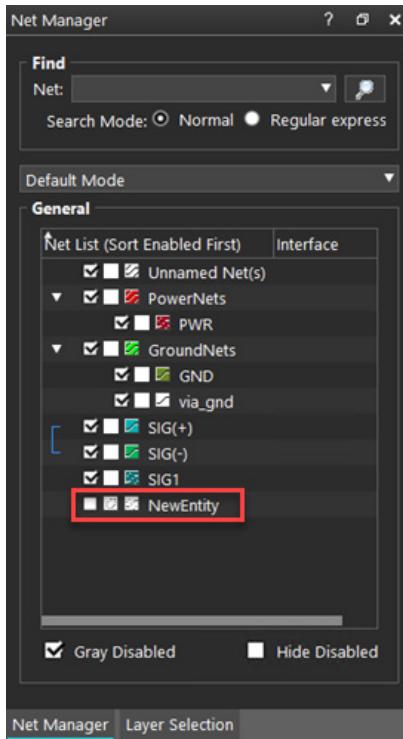
## Topology Workbench User Guide

### Using the Via Wizard

- Right-click anywhere in the *Net Manager* and select *New* from the displayed shortcut menu.



A new row, *NewEntity*, is added to the table in *General* section.



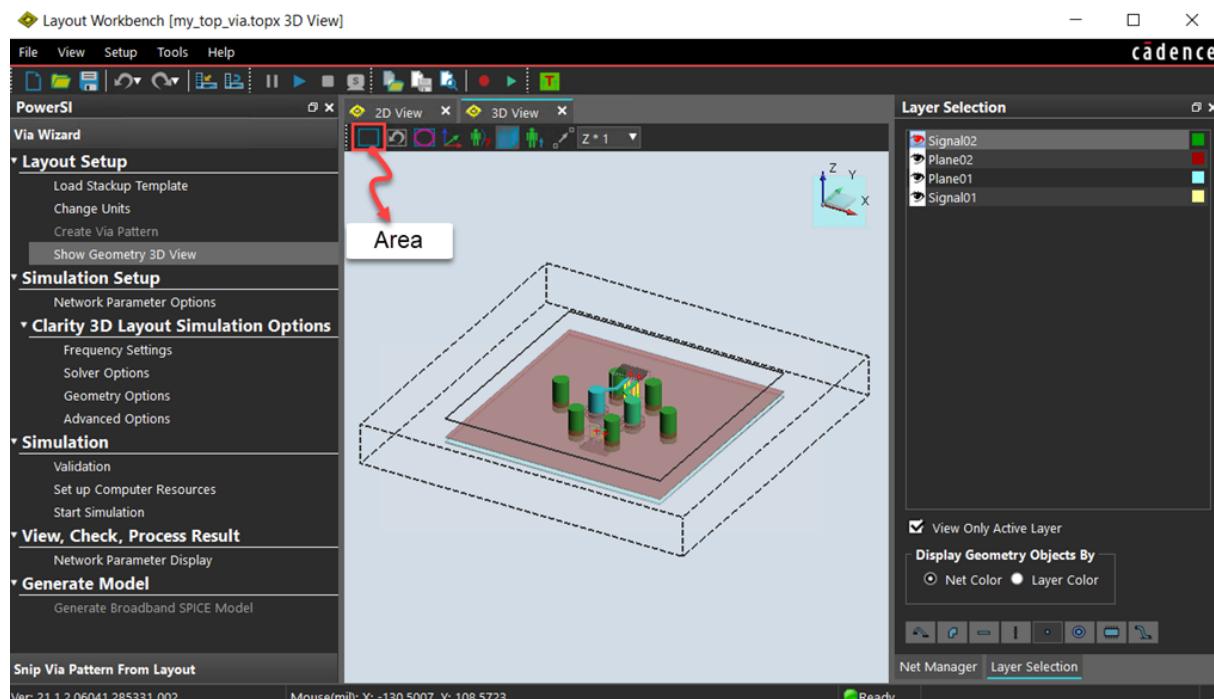
# Topology Workbench User Guide

## Using the Via Wizard

- Double-click the newly-created net (*NewEntity*) in the *Net Manager* and select *Rename* from the displayed shortcut menu, and give it the desired name.

### Reviewing the 3D Structure

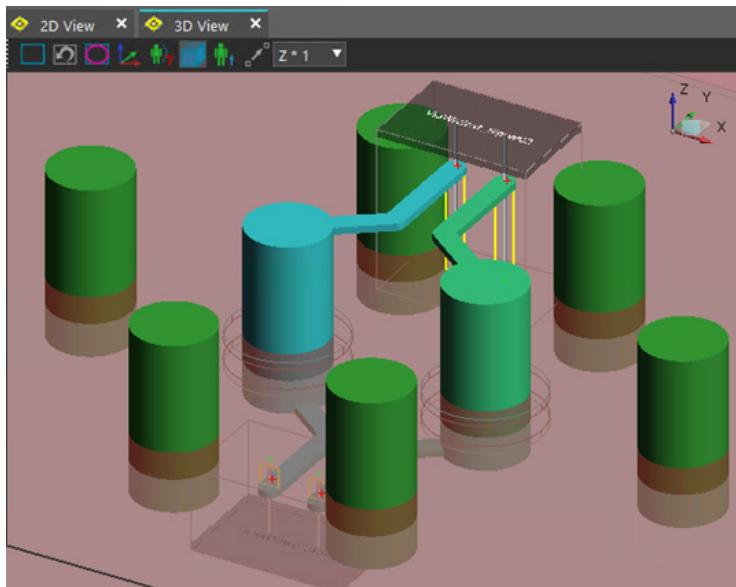
- Click *Show Geometry 3D View* in the *Workflow* panel.



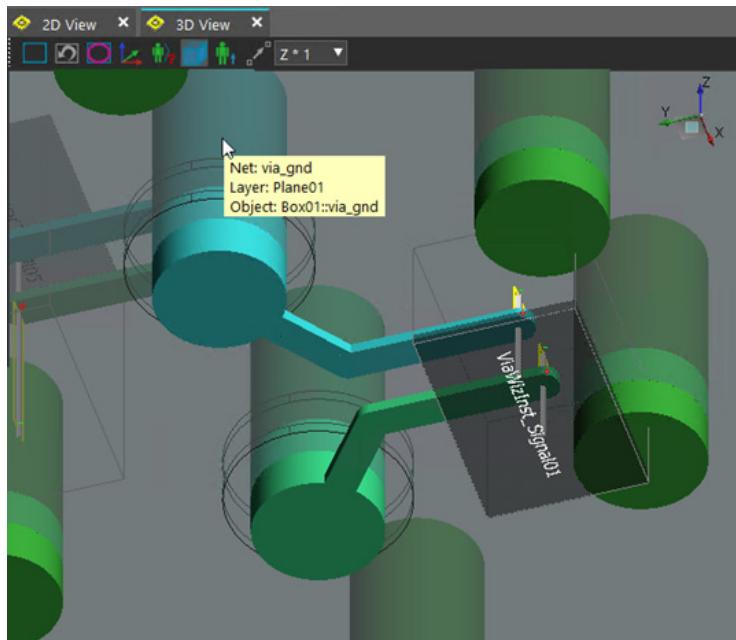
## Topology Workbench User Guide

### Using the Via Wizard

2. Click the *Area* option in the toolbar of the *3D View* tab, which opens, and click two points to zoom in. Click the *Area* icon again to disable the zoom mode.



3. Click the structure and move it around while keeping the pointer clicked to view the structure from all sides. Notice how the signals connect on the different layers. You can also zoom in or out by rotating the scroll wheel of the mouse. When you place the pointer on different parts of the structure, the annotated text is displayed about the object under the pointer.



# Topology Workbench User Guide

## Using the Via Wizard

**Note:** For the normal view, click the *2D View* tab.

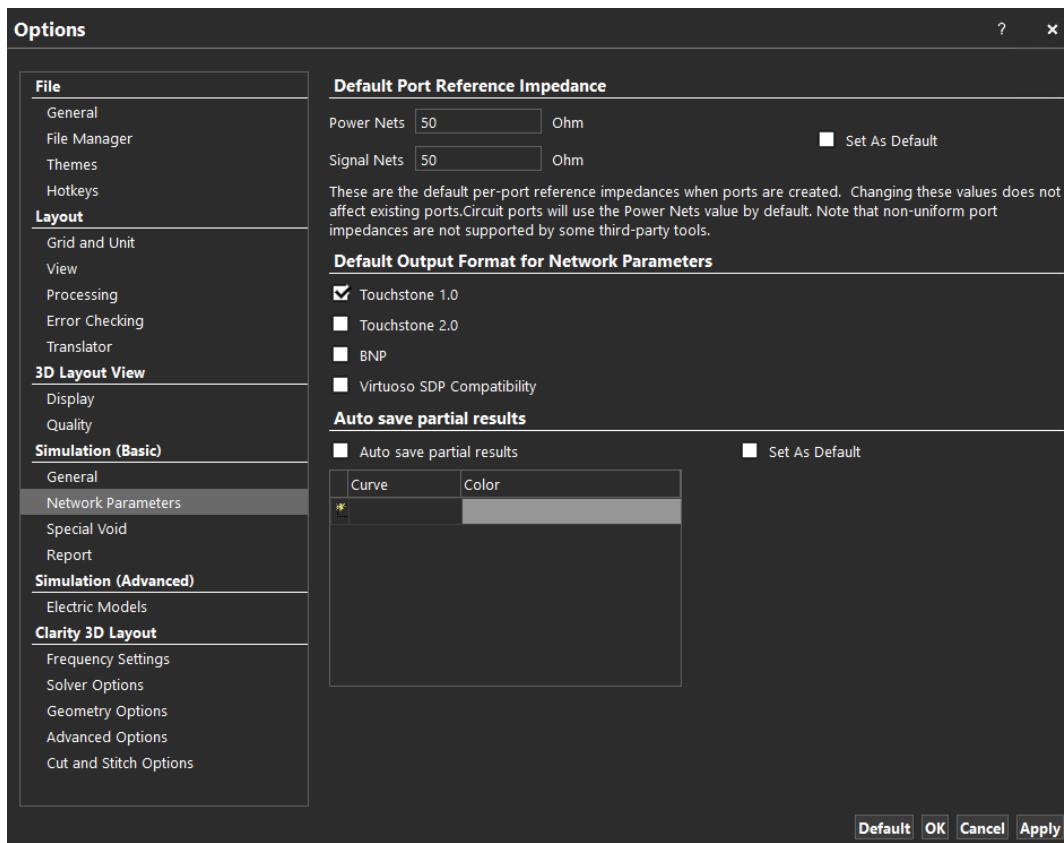
## Generating the Via Model

This process involves the following steps:

1. Setting the S-Parameter Model Format
2. Setting the Clarity 3D Layout Simulation Options
3. Setting the Resources for Simulation
4. Extracting the Model
5. Connecting the Via Block

## Setting the S-Parameter Model Format

1. Click *Network Parameter Options* in the *Workflow* panel. The *Options* form opens with *Network Parameters* selected in the *Simulation (Basic)* schema.



## Topology Workbench User Guide

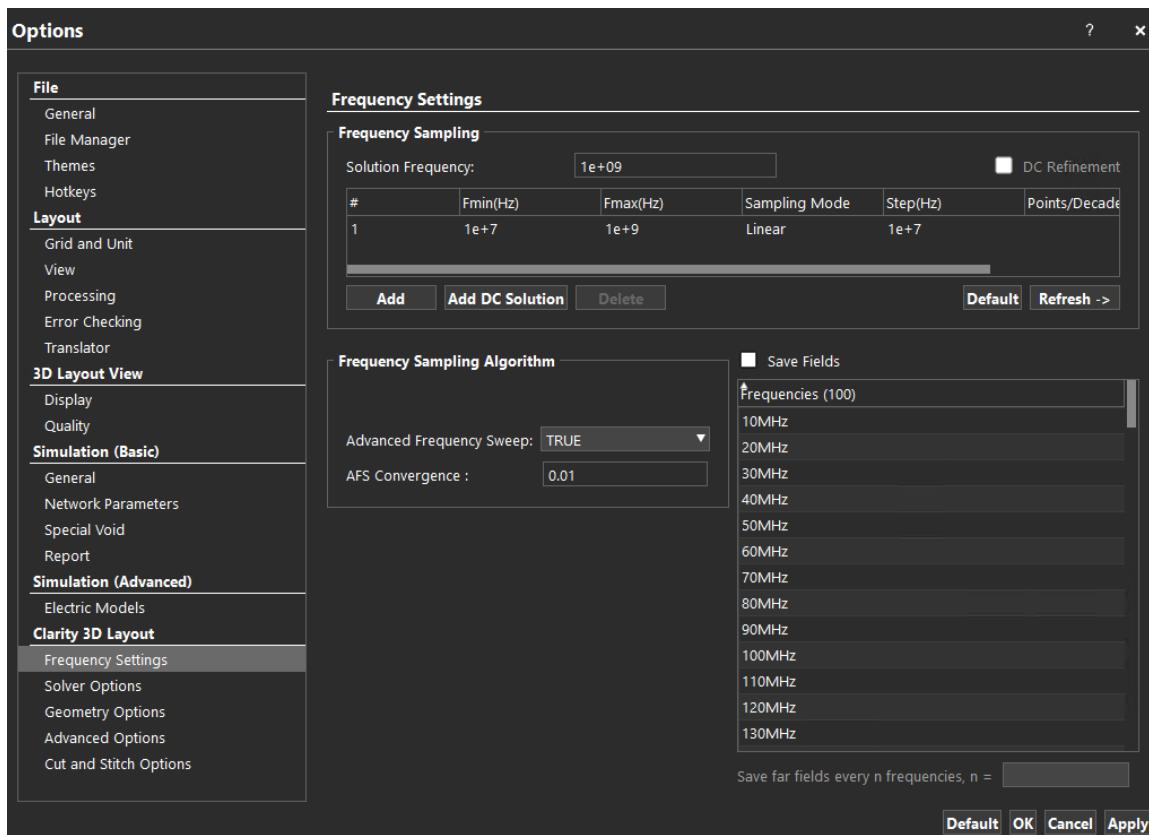
### Using the Via Wizard

2. Set the *Default Port Reference Impedance* for *Power Nets* and *Signal Nets*. You can choose to *Set As Default*.
3. Set the desired *Default Output Format for Network Parameters* to define the supported S Parameter model formats. For example, *Touchstone* is selected by default, and you can select *BNP* as well.

### Setting the Clarity 3D Layout Simulation Options

**Note:** The options covered in this section are used to control the Clarity 3D Layout field solution. Additional detail on these controls can be found in the *Clarity 3D Layout User Manual*. For the purpose of via model extraction for Topology Workbench, it is recommended that you retain the default settings.

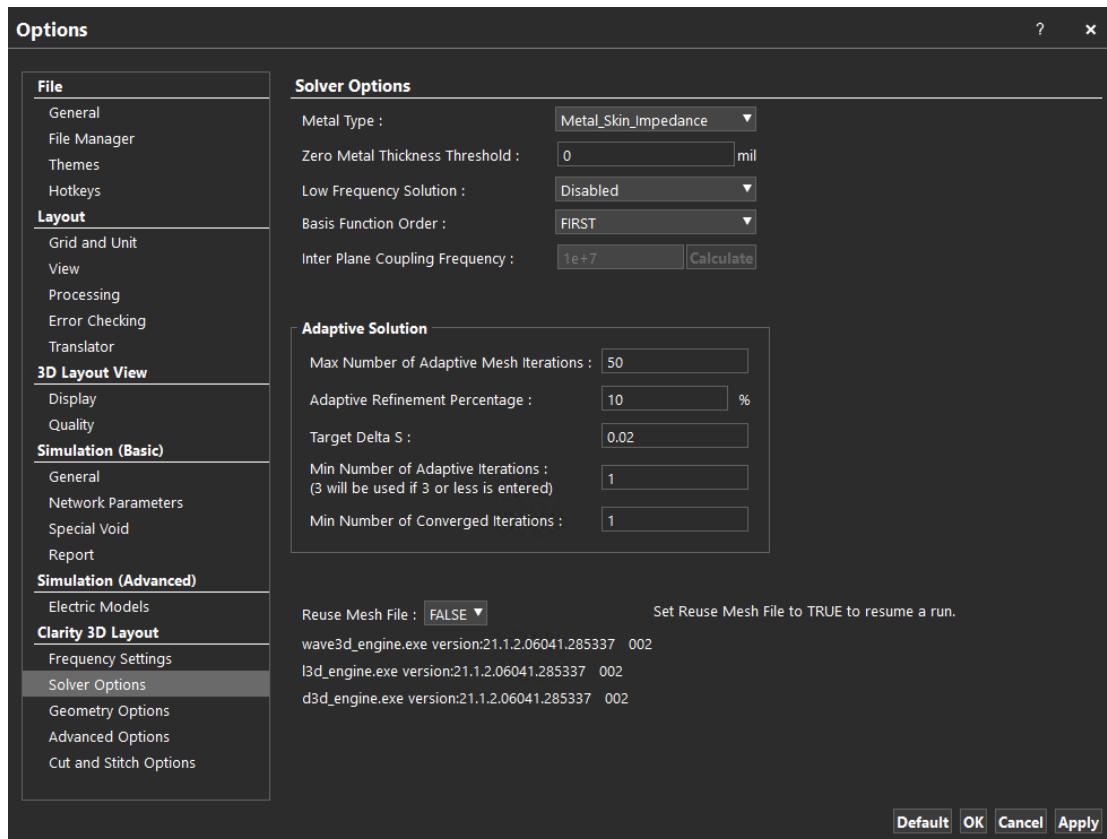
1. Click *Frequency Settings* in the *Workflow* panel. The *Options* form opens with *Frequency Settings* selected in the *Clarity 3D Layout* schema.



# Topology Workbench User Guide

## Using the Via Wizard

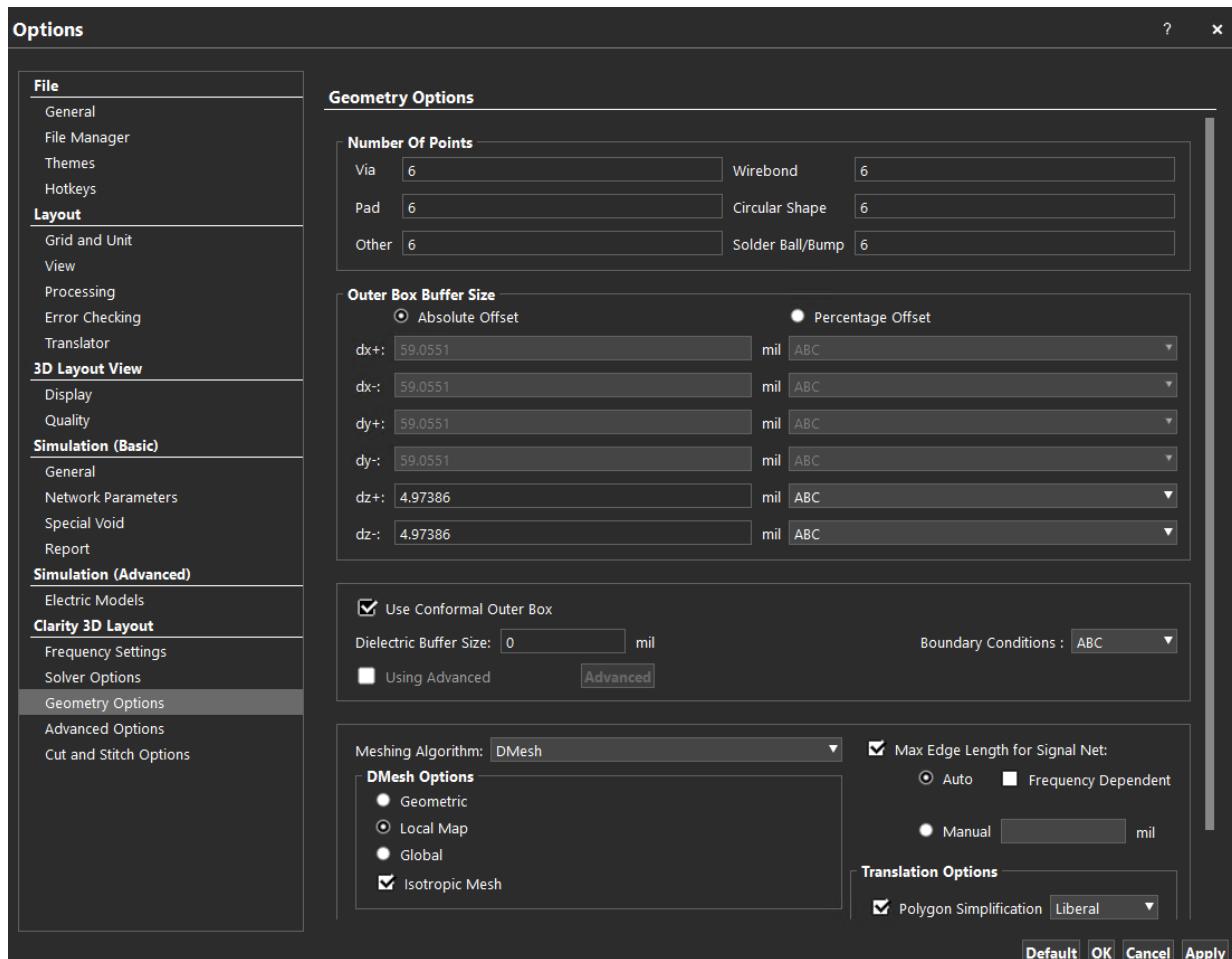
2. Click *Solver Options* to review the set parameters.



# Topology Workbench User Guide

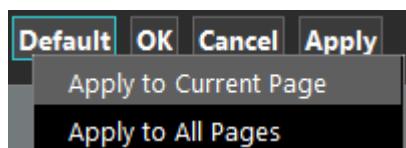
## Using the Via Wizard

3. Click *Geometry Options* to review the set parameters.



**Note:** In the *Geometry Options*, when *Use Conformal Outer Box* is selected and *Dielectric Buffer Size* is set to *0*, all planes are modeled as infinite because *ABC* is placed at the edges of the planes. This suppresses the plane modes that would otherwise exist due to the small plane size.

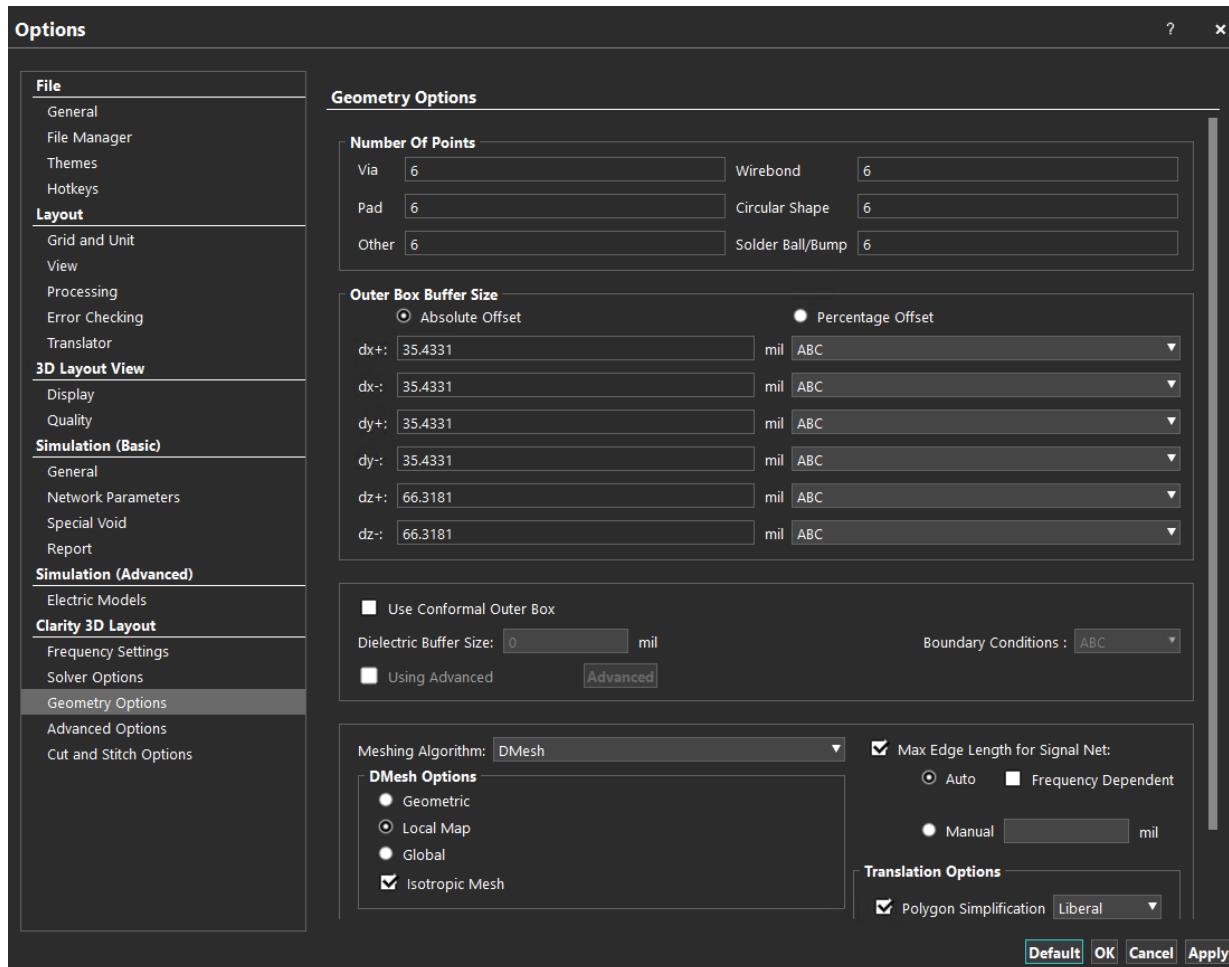
4. Click *Default*. When you are prompted to confirm whether to apply the change to the current page or all the pages, select *Apply to Current Page*.



# Topology Workbench User Guide

## Using the Via Wizard

The parameter definitions on the Geometry Options page show updated values as shown below:



- Click *OK* to save the settings.
- Click *File – Save* to save the .spd file before proceeding to the next step.

## Setting the Resources for Simulation

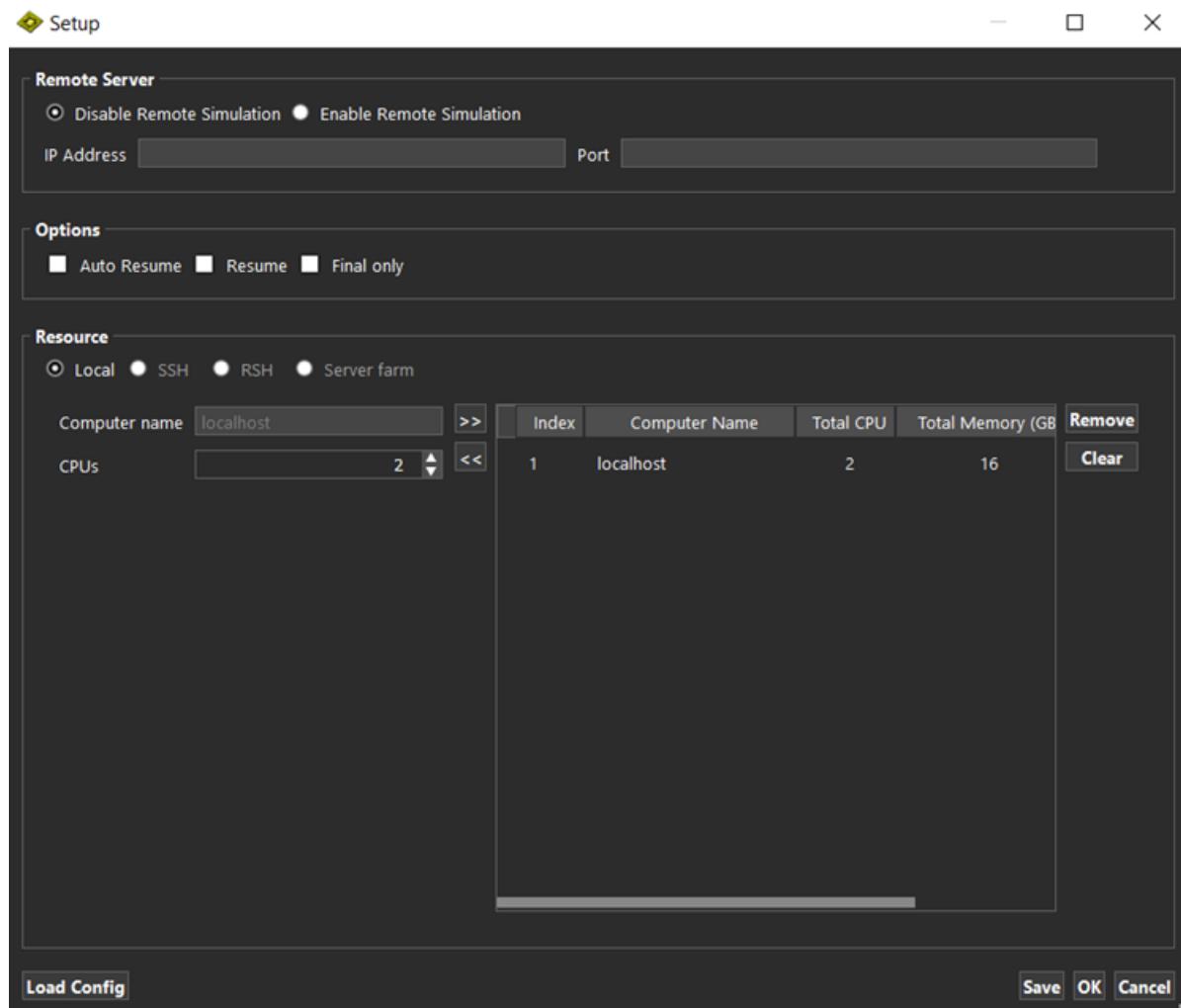
To set up the computer resources for a simulation run on a standalone Windows computer, perform the following steps:

- Click *Setup Computer Resources* in the *Workflow* panel. The *Setup* dialog box opens with *Disable Remote Simulation* selected in the *Remote Server* section and *Local* selected in the *Resource* section.

## Topology Workbench User Guide

### Using the Via Wizard

**Note:** The *Computer name* field is disabled and displays `localhost` as the name of the computer on which you are performing the simulation.



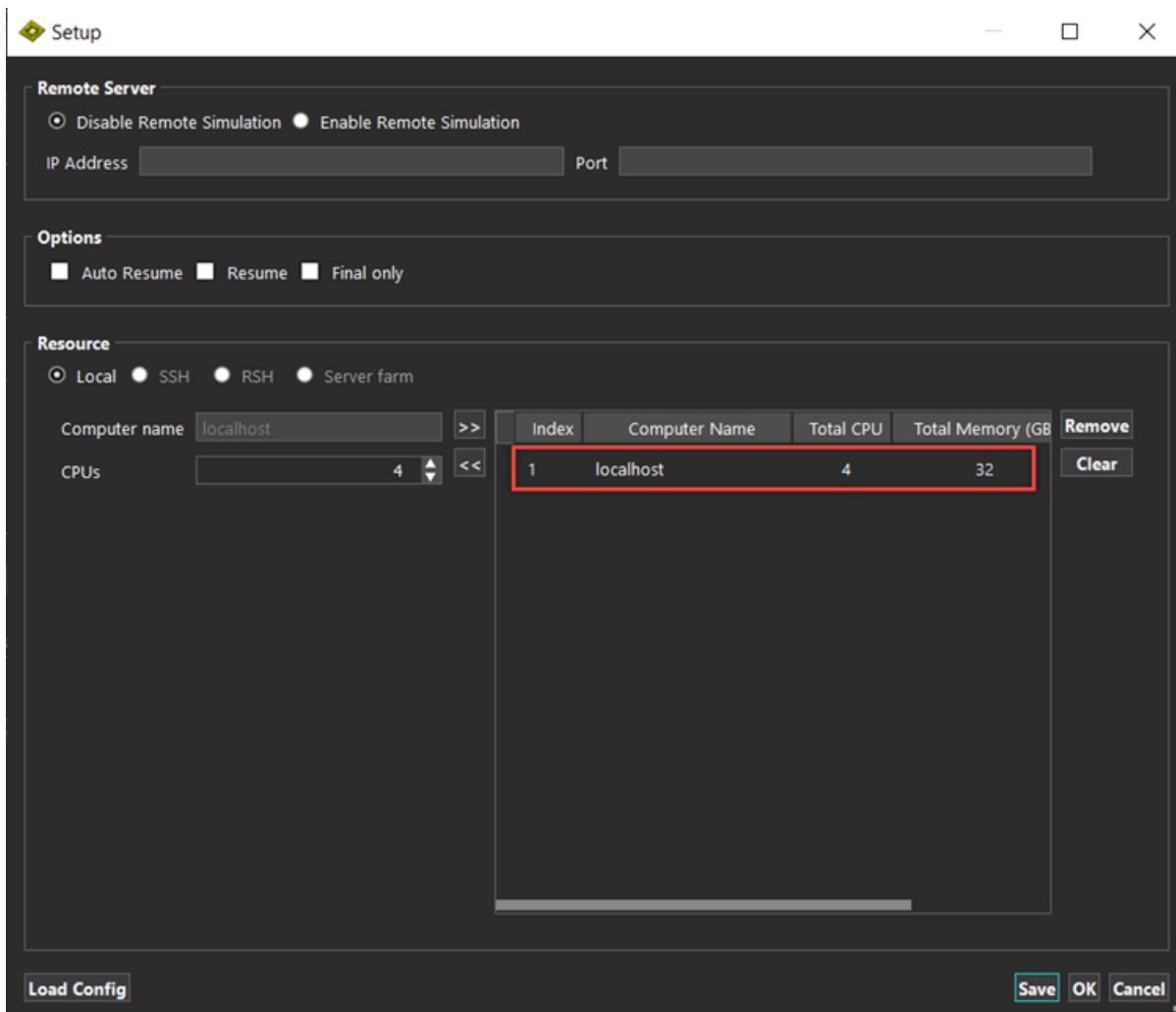
2. Specify 4 as the number of CPUs to use for the simulation in the *CPUs* field.

**Note:** The default value is 2 CPUs. You can change this value according to the need of the design.

## Topology Workbench User Guide

### Using the Via Wizard

3. Click the (**>>**) button to add the configuration to the right pane.



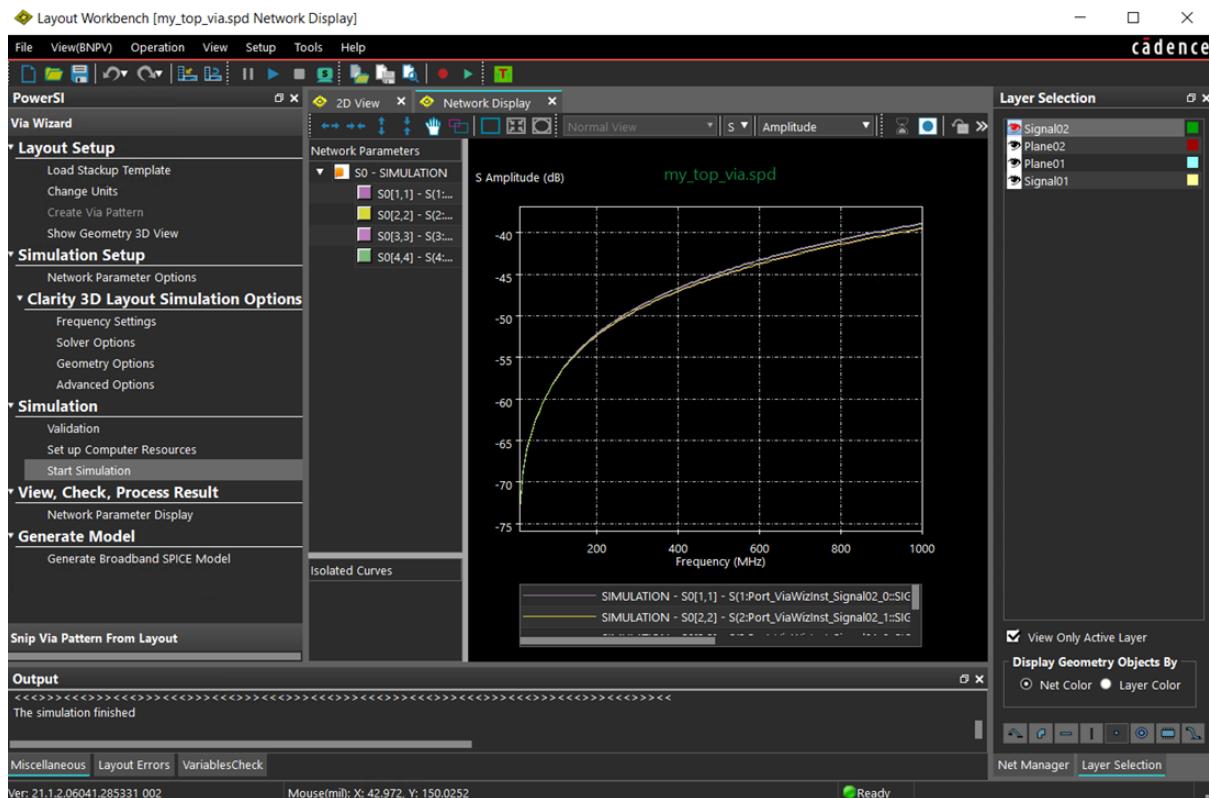
4. Click *Save* to save the configuration.
5. Click *OK* to exit the *Setup* dialog box.
6. Click *File – Save* to save the .spd file before proceeding to the simulation.

# Topology Workbench User Guide

## Using the Via Wizard

### Extracting the Model

1. Click *Start Simulation* in the *Workflow* panel. The progress messages are displayed in the *Output* pane.



2. Choose *File – Exit* from the Sigriy Suite window's menu after the extraction finishes and save the project if prompted before the exit.

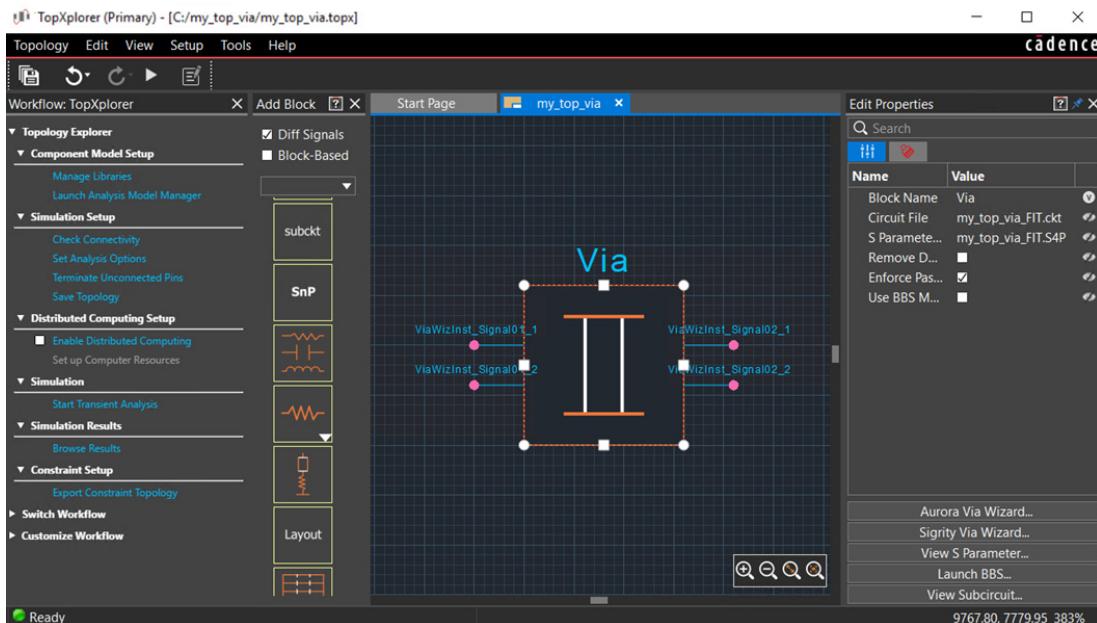
The Sigriy Suite window closes and the extracted via model is refreshed in Topology Workbench as shown below. The *Edit Properties* panel shows the name of the *Circuit*

# Topology Workbench User Guide

## Using the Via Wizard

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*File* and *Subcircuit* associated with the extracted via model. In addition, on the layout canvas, notice that the single-ended Via block now appears as a differential signal block.



### 3. Click *View Subcircuit* to open the *Subcircuit Editor*.

```

1 .SUBCKT my_top_via_FIT
2 +
3 +
4 +
5 +
6 +
7 +
8 +
9 +
10 *The following is the Cadence MCP(model connection protocol) Section
11 ****
12 *[MCP Begin]
13 *[MCP Ver] 1.1
14 *[MCP Source] Cadence Design Systems, Inc. Layout Workbench 21.1.2.06041.285331 002 6/7/2021
15 *
16 ****
17 *
18 *[REM]The following is the info for component connection ViaWizInst_Signal01
19 *[REM]*****
20 *[Connection] ViaWizInst_Signal01 ViaWiz 4
21 *[Power Nets]
22 *[Ground Nets]
23 *3 ViaWizInst_Signal01_3 via_gnd -0.0001250 -0.0008131
24 *4 ViaWizInst_Signal01_4 via_gnd 0.0001250 -0.0008131
25 *[Signal Nets]
26 *1 ViaWizInst_Signal01_1 SIG(+) -0.0001250 -0.0008131
27 *2 ViaWizInst_Signal01_2 SIG(-) 0.0001250 -0.0008131
28 *
29 *[REM]The following is the info for component connection ViaWizInst_Signal02
30 *[REM]*****
31 *[Connection] ViaWizInst_Signal02 ViaWiz 4
32 *[Power Nets]
33 *[Ground Nets]
34 *3 ViaWizInst_Signal02_3 via_gnd -0.0001250 0.0008131

```

## Topology Workbench User Guide

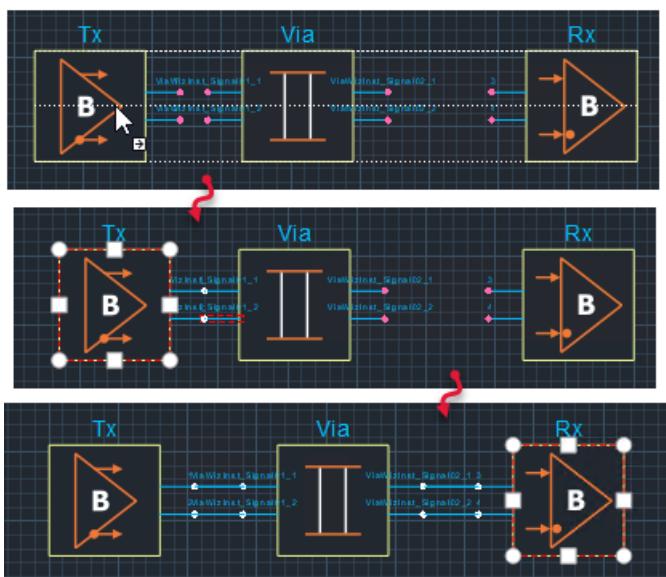
### Using the Via Wizard

4. Review the model definition and close the dialog box.

#### Connecting the Via Block

1. Connect the Via block with extracted model to the required blocks in the topology.

For example, the images below illustrate the Via block being connected to the transmitter IBIS (Tx) and receiver IBIS (Rx) blocks of differential configuration. Such type of blocks are available for use when you select the *Diff Signals* toggle button in the *Settings* option of the floating toolbar.



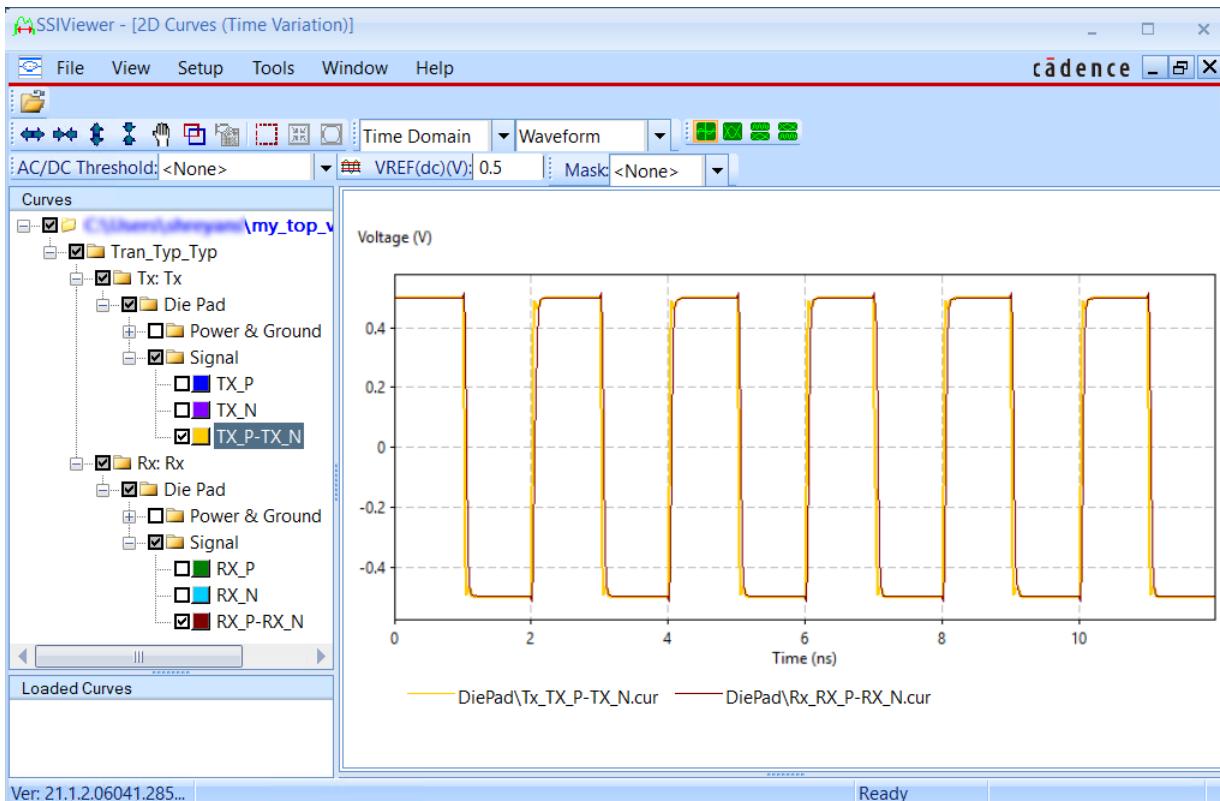
2. Check connectivity and define analysis options for the topology.
3. Simulate the topology.

On successful completion of the simulation run, the 2D Curves tab opens. You can select signals of the Via block that connect to the transmitter and receiver blocks, respectively.

## Topology Workbench User Guide

### Using the Via Wizard

This helps to review the simulation waveform results generated between these blocks as shown below.



## Aurora Via Wizard

This topic covers usage information about the Aurora Via Wizard that helps to generate via models in the pre-layout phase.

**Note:** You can use the pre-defined layout templates for the Aurora Via Wizard that can be found at the following location:

<ALLEGRO\_INSTALL\_DIR>\share\pcb\ida\viawiz\xsecion

### Related Topics

- [Defining the Via Structure](#)
- [Generating the Via Model](#)

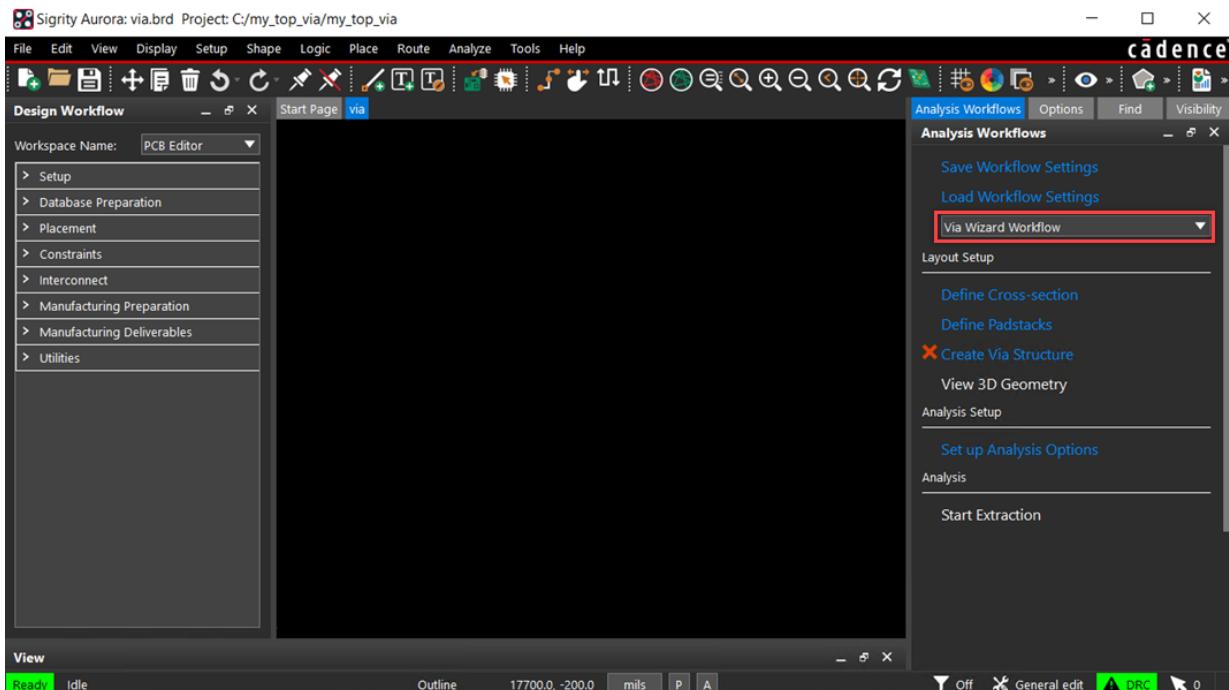
# Topology Workbench User Guide

## Using the Via Wizard

### Defining the Via Structure

To define a via structure using Aurora Via Wizard:

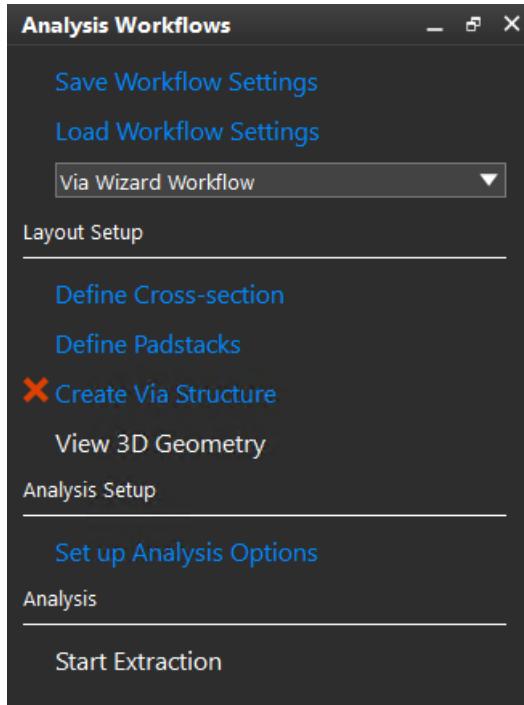
- Click the *Aurora Via Wizard* button in the *Edit Properties* panel. The Sigrity Aurora window opens with the *Via Wizard Workflow* option selected in it.



## Topology Workbench User Guide

### Using the Via Wizard

The *Aurora Via Wizard* provides its own workflow to support the via modeling process.

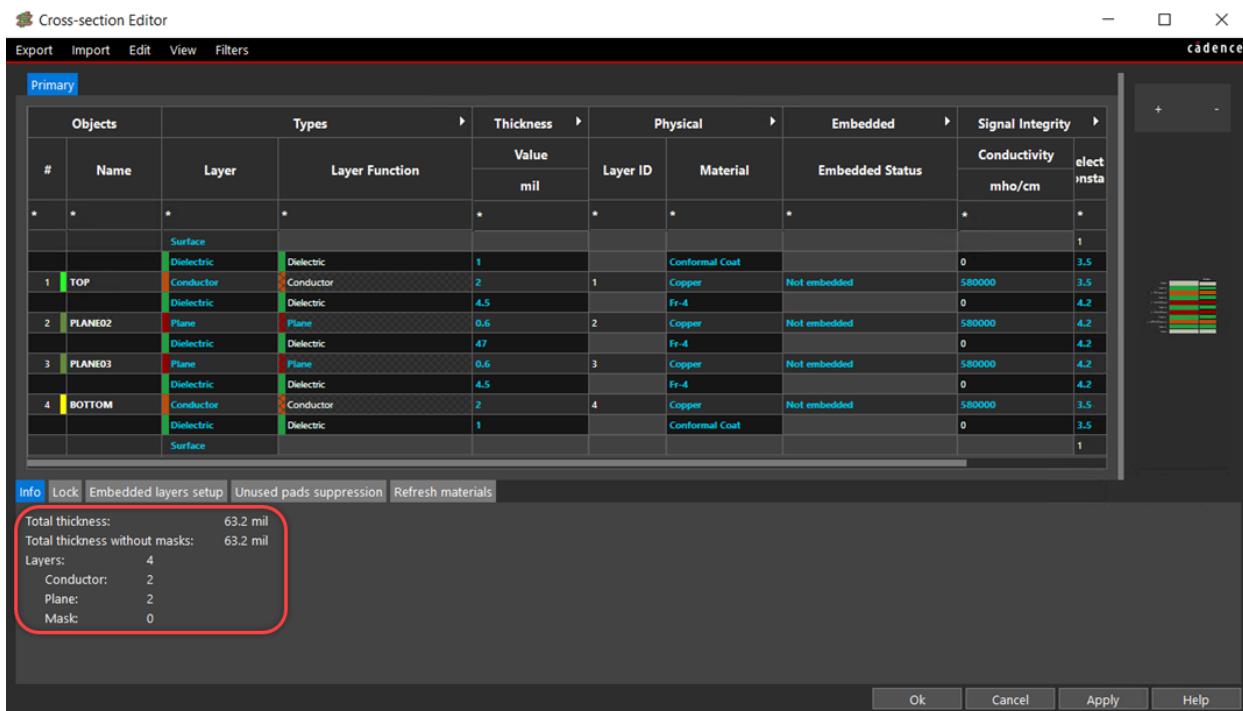


# Topology Workbench User Guide

## Using the Via Wizard

### Defining the Cross-Section

1. Click *Define Cross-section* in the *Analysis Workflows* panel. The *Cross-section Editor* window opens with the information of the layers displayed in the *Info* section.



2. Enter the stack-up layers, thickness, and material properties as per the design requirements.

**Note:** Add at least one **PLANE** layer and a **GND** shape on this layer to cover the entry and exit traces of a via structure, otherwise the port definition will fail.

3. Click **OK** when finished with the stack-up definition. The *Cross-section Editor* dialog box closes.

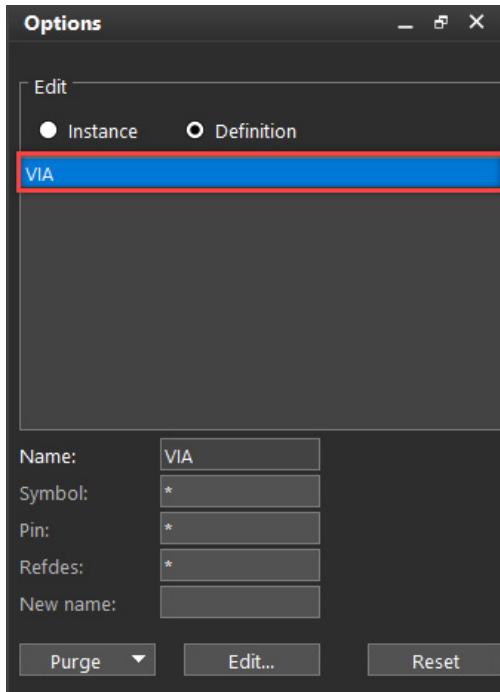
## Topology Workbench User Guide

### Using the Via Wizard

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#### Defining the Padstacks

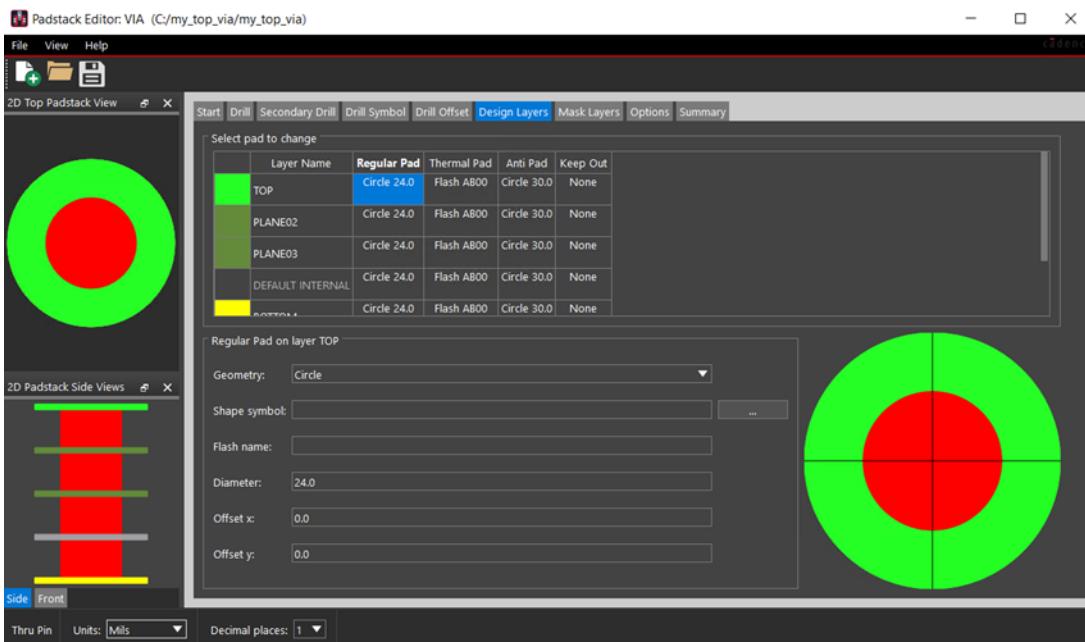
1. Click *Define Padstacks* in the *Analysis Workflows* panel. The *Options* panel opens with the pre-defined VIA selected in the *Edit* section.



## Topology Workbench User Guide

### Using the Via Wizard

2. Click *Edit* to edit the default definitions of the padstack according to the need of your design. The *Padstack Editor* window opens.



3. Close the *Padstack Editor* dialog box.

**Note:** If no padstack is defined in the design, you can select a padstack from library while creating a via structure.

### Creating a Via Structure

You can choose to create a differential pair or single-ended via structure as explained below:

- [Creating a Differential Pair Via Structure](#)
- [Creating a Single-Ended Via Structure](#)

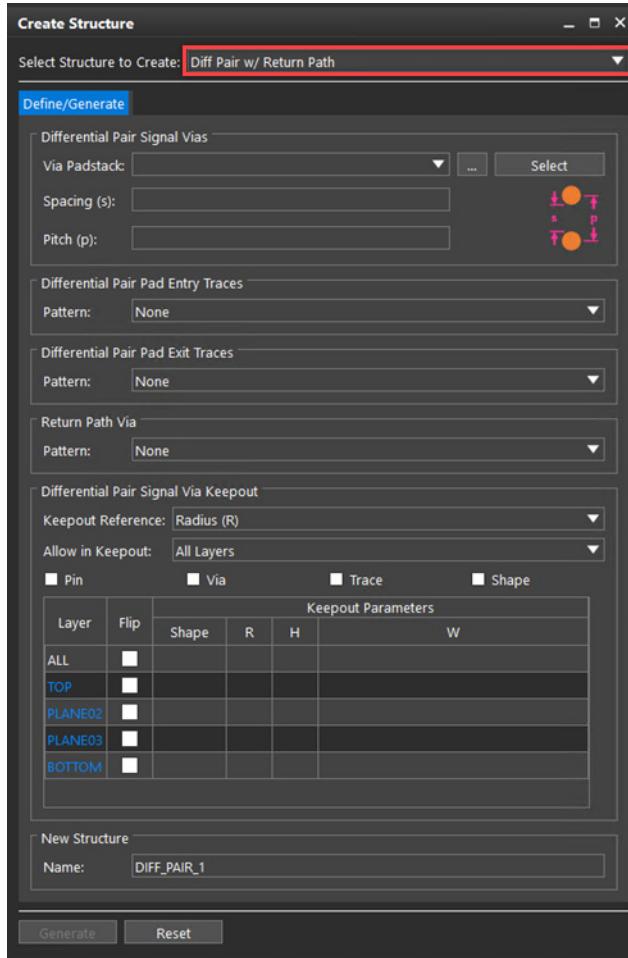
#### ***Creating a Differential Pair Via Structure***

1. Click *Create Via Structure* in the *Analysis Workflows* panel. The *Create Structure* dialog box opens.

## Topology Workbench User Guide

### Using the Via Wizard

- 2.** Choose *Diff Pair w/ Return Path* from the *Select Structure to Create* drop-down list.



- 3.** Input the desired values as per the requirements of your design.

**Note:** You can also choose to create a single-ended via structure. For more information, see [Creating a Single-Ended Via Structure](#).

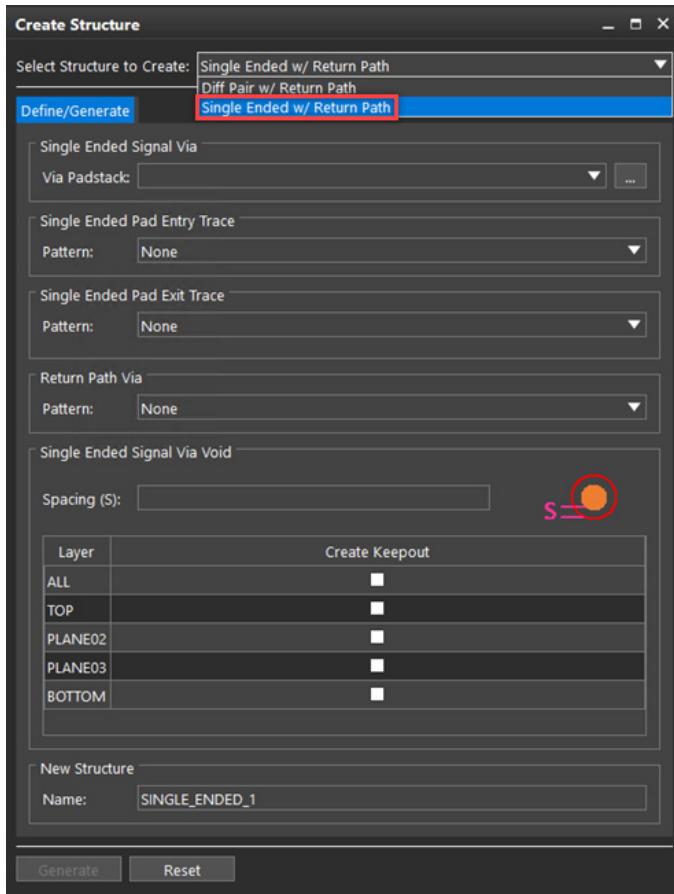
#### ***Creating a Single-Ended Via Structure***

- 1.** Click *Create Via Structure* in the *Analysis Workflows* panel. The *Create Structure* dialog box opens.

## Topology Workbench User Guide

### Using the Via Wizard

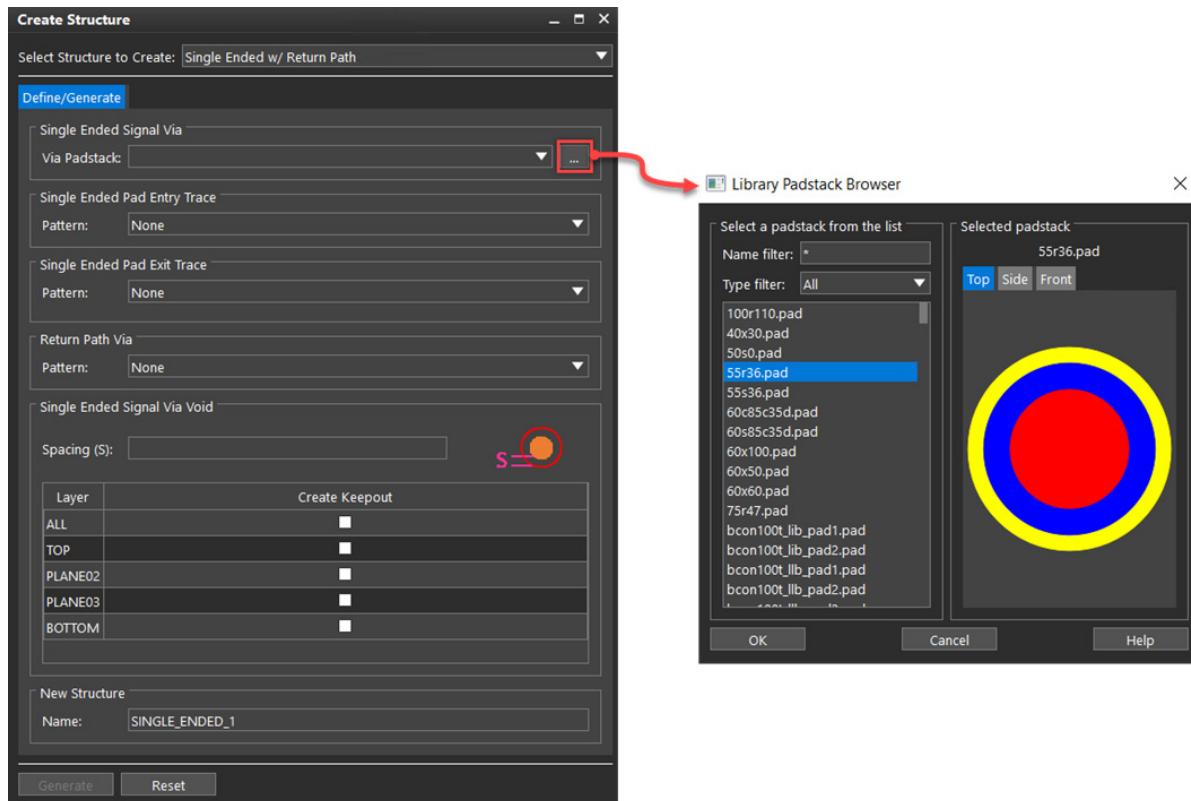
2. Choose *Single Ended w/Return Path* from the *Select Structure to Create* drop-down list.



## Topology Workbench User Guide

### Using the Via Wizard

3. Click the ( ...) button to browse through the padstack library. The *Library Padstack Browser* dialog box opens.



4. Choose 55r36.pad from the padstack list and click *OK*.

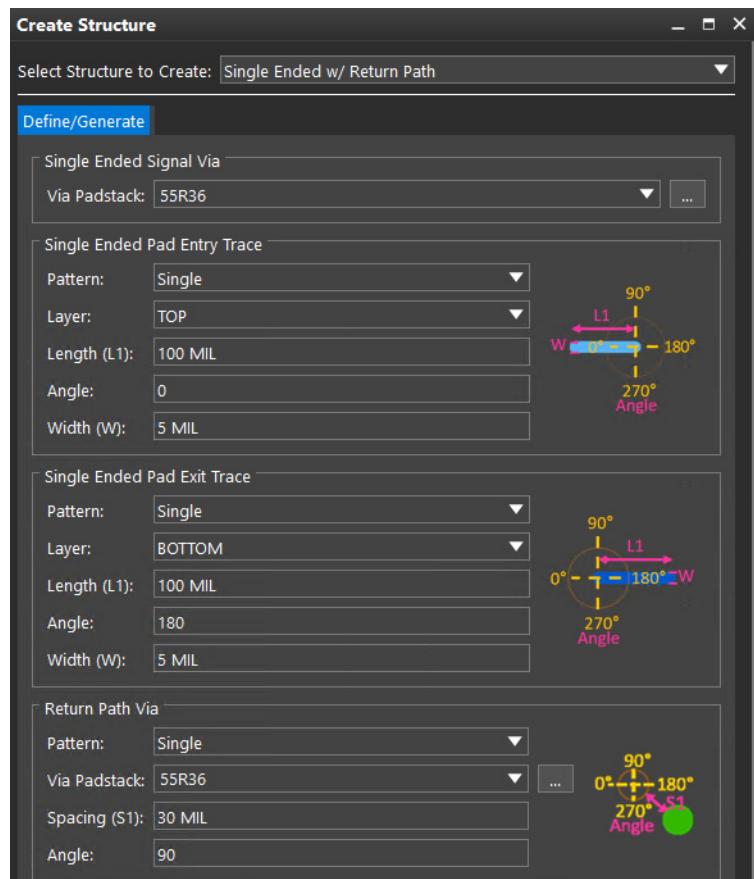
5. Input the following values:

- For the *Single Ended Pad Entry Trace* section:
  - Pattern:* Single
  - Layer:* TOP
  - Length (L1):* 100 MIL
  - Angle:* 0
  - Width (W):* 5 MIL
- For the *Single Ended Pad Exit Trace* section:
  - Pattern:* Single
  - Layer:* BOTTOM

# Topology Workbench User Guide

## Using the Via Wizard

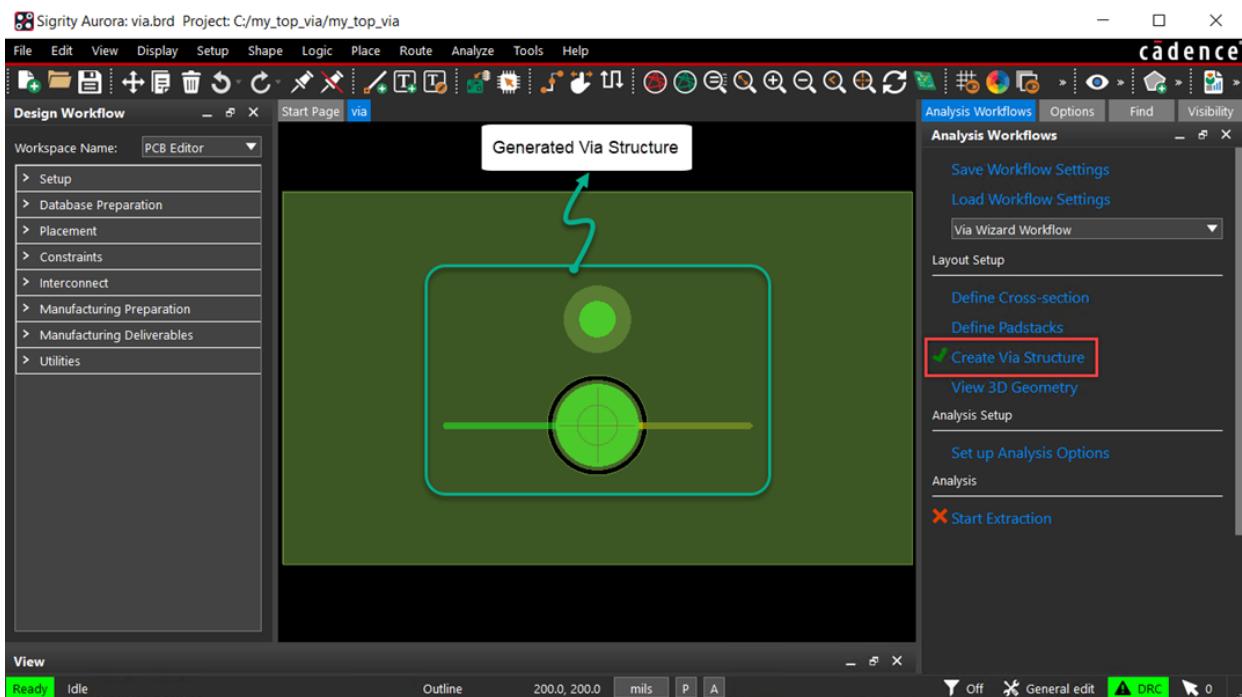
- *Length (L1)*: 100 MIL
- *Angle*: 180
- *Width (W)*: 5 MIL
- For the *Return Path Via* section:
  - *Pattern*: Single
  - *Via Padstack*: 55R36
  - *Spacing (S1)*: 30 MIL
  - *Angle*: 90



## Topology Workbench User Guide

### Using the Via Wizard

6. Click *Generate*. Notice that a green check mark now appears before *Create Via Structure*. This means that the via structure is generated on the canvas, as shown below:



**Note:** You can also choose to create a differential pair via structure. For more information, see [Creating a Differential Pair Via Structure](#).

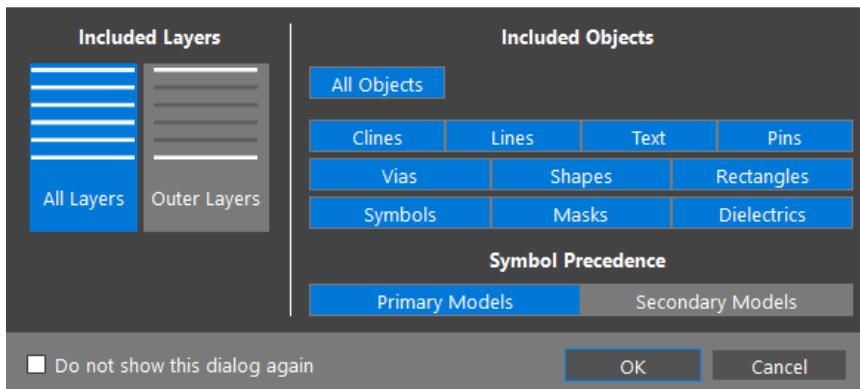
# Topology Workbench User Guide

## Using the Via Wizard

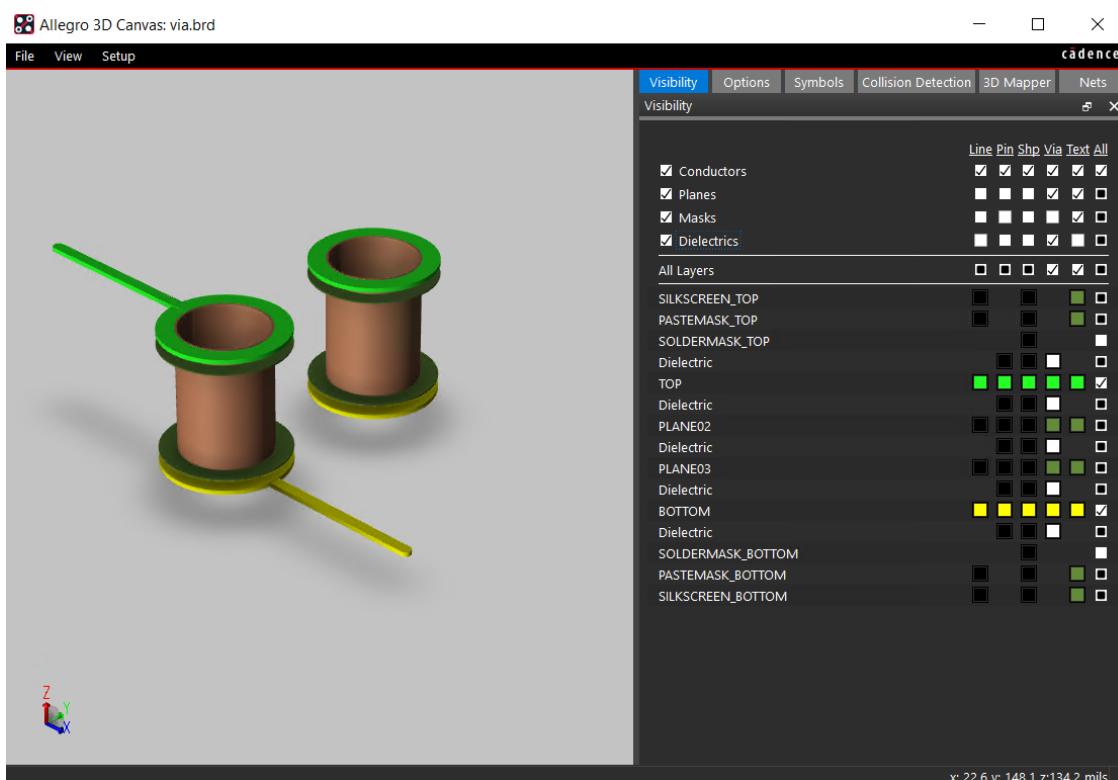
### Viewing the 3D Geometry

1. Click *View 3D Geometry* in the *Analysis Workflows* panel. The *3D Canvas Filter* dialog box opens.

3D Canvas Filter



2. Click *OK*. The *Allegro 3D Canvas* window opens. With the *Dielectrics* and *Conductors* options enabled for *Via*, you can visualize the via barrel, entry and exit traces, and the return path via, as shown below:



3. Close the *Allegro 3D Canvas* window.

## Generating the Via Model

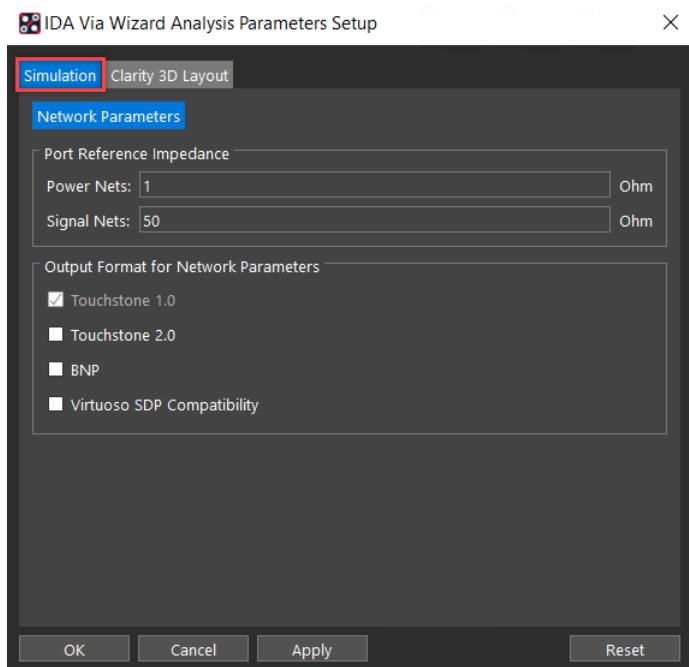
This process involves the following steps:

1. Setting Up Analysis Options
2. Extracting the Model
3. Connecting the Via Block

### Setting Up Analysis Options

To set up the frequency and network parameters, do the following:

1. Click *Set up Analysis Options* in the *Analysis Workflows* panel. The *IDA Via Wizard Analysis Parameters Setup* dialog box opens with the *Simulation* option selected in it.

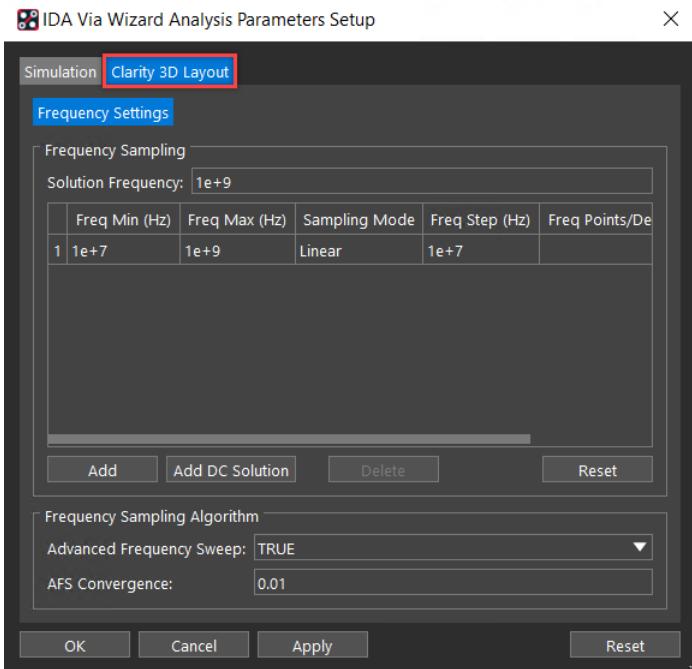


2. Edit the port reference impedance and specify the output format for the network parameters as per the requirements of your design.

## Topology Workbench User Guide

### Using the Via Wizard

3. Click *Clarity 3D Layout* to edit the frequency settings as per the requirements of your design.



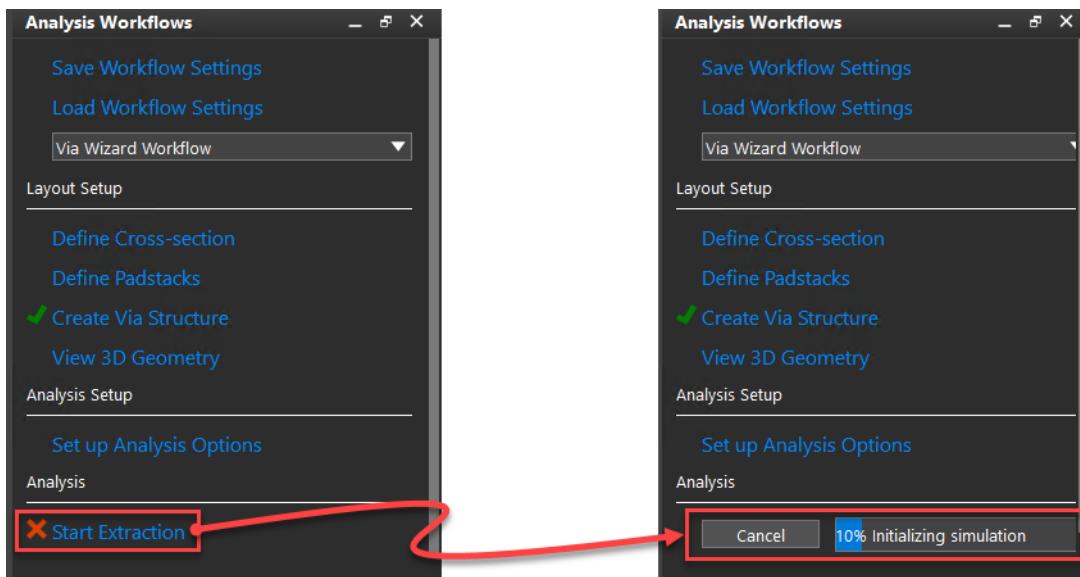
4. Click *OK* to close the dialog box.

# Topology Workbench User Guide

## Using the Via Wizard

### Extracting the Model

1. Click *Start extraction* to extract the S-Parameter for the via structure in the *Analysis Workflows* panel.



*Start Extraction* is enabled only when the current design is validated. A validated design must meet the following conditions:

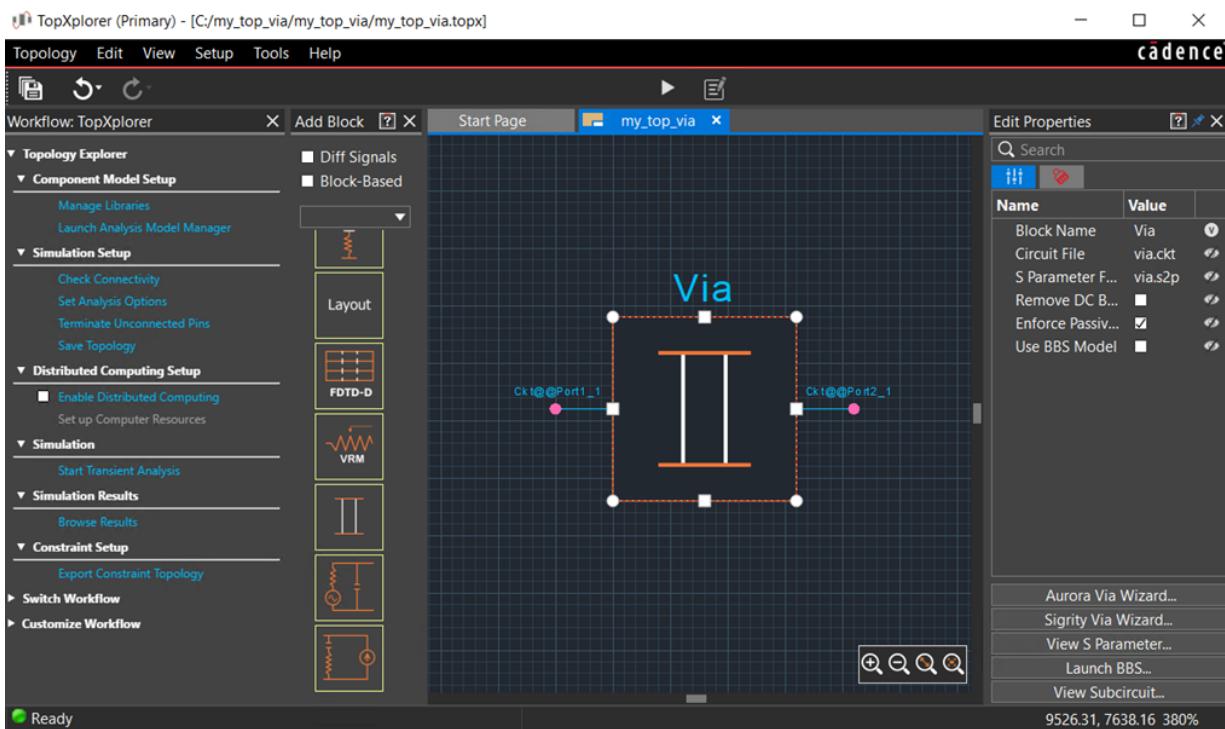
- Only one via structure is placed on the design canvas.
- If a single-ended via structure placed, one signal via and two traces are required.
- If a differential pair via structure placed, two signal vias and four traces are required.

On successful completion of the extraction, the Sigrity Aurora window closes automatically and the extracted via model is refreshed in the Topology Xplorer

# Topology Workbench User Guide

## Using the Via Wizard

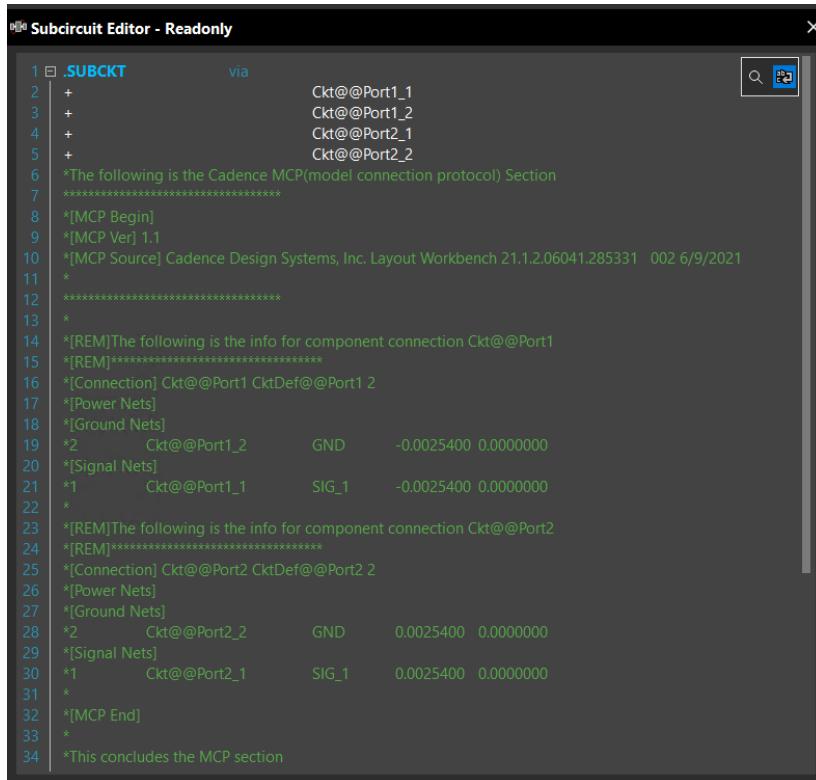
Workbench, as shown below. The *Edit Properties* panel shows the name of the *Circuit File* and *Subcircuit* associated with the extracted via model.



## Topology Workbench User Guide

### Using the Via Wizard

2. Click *View Subcircuit* to open the *Subcircuit Editor*.



The screenshot shows the 'Subcircuit Editor - Readonly' dialog box. The code content is as follows:

```
1 .SUBCKT      via
2 +           Ckt@@Port1_1
3 +           Ckt@@Port1_2
4 +           Ckt@@Port2_1
5 +           Ckt@@Port2_2
6 *The following is the Cadence MCP(model connection protocol) Section
7 ****
8 *[MCP Begin]
9 *[MCP Ver] 1.1
10 *[MCP Source] Cadence Design Systems, Inc. Layout Workbench 21.1.2.06041.285331 002 6/9/2021
11 *
12 ****
13 *
14 *[REM]The following is the info for component connection Ckt@@Port1
15 *[REM]*****
16 *[Connection] Ckt@@Port1 CktDef@@Port1 2
17 *[Power Nets]
18 *[Ground Nets]
19 *2       Ckt@@Port1_2      GND     -0.0025400 0.0000000
20 *[Signal Nets]
21 *1       Ckt@@Port1_1      SIG_1   -0.0025400 0.0000000
22 *
23 *[REM]The following is the info for component connection Ckt@@Port2
24 *[REM]*****
25 *[Connection] Ckt@@Port2 CktDef@@Port2 2
26 *[Power Nets]
27 *[Ground Nets]
28 *2       Ckt@@Port2_2      GND     0.0025400 0.0000000
29 *[Signal Nets]
30 *1       Ckt@@Port2_1      SIG_1   0.0025400 0.0000000
31 *
32 *[MCP End]
33 *
34 *This concludes the MCP section
```

3. Review the model definition and close the dialog box.

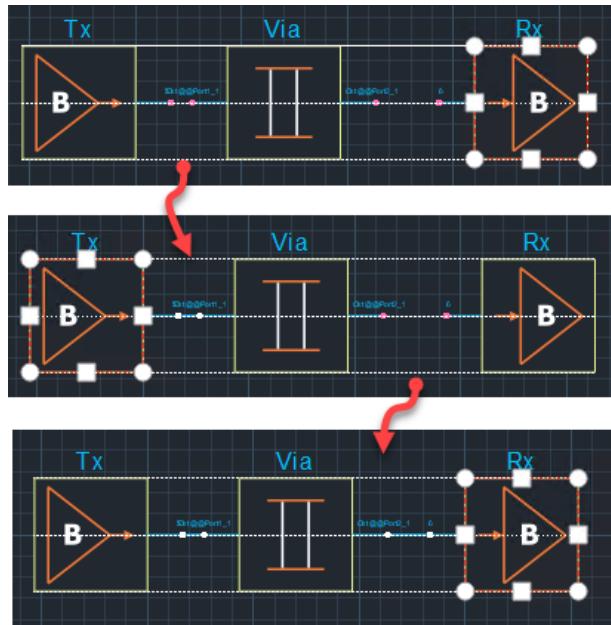
## Connecting the Via Block

1. Connect the Via block with extracted model to the required blocks in the topology.

## Topology Workbench User Guide

### Using the Via Wizard

For example, the images below illustrate the Via block being connected to the transmitter IBIS (Tx) and receiver IBIS (Rx) blocks of single-ended configuration.



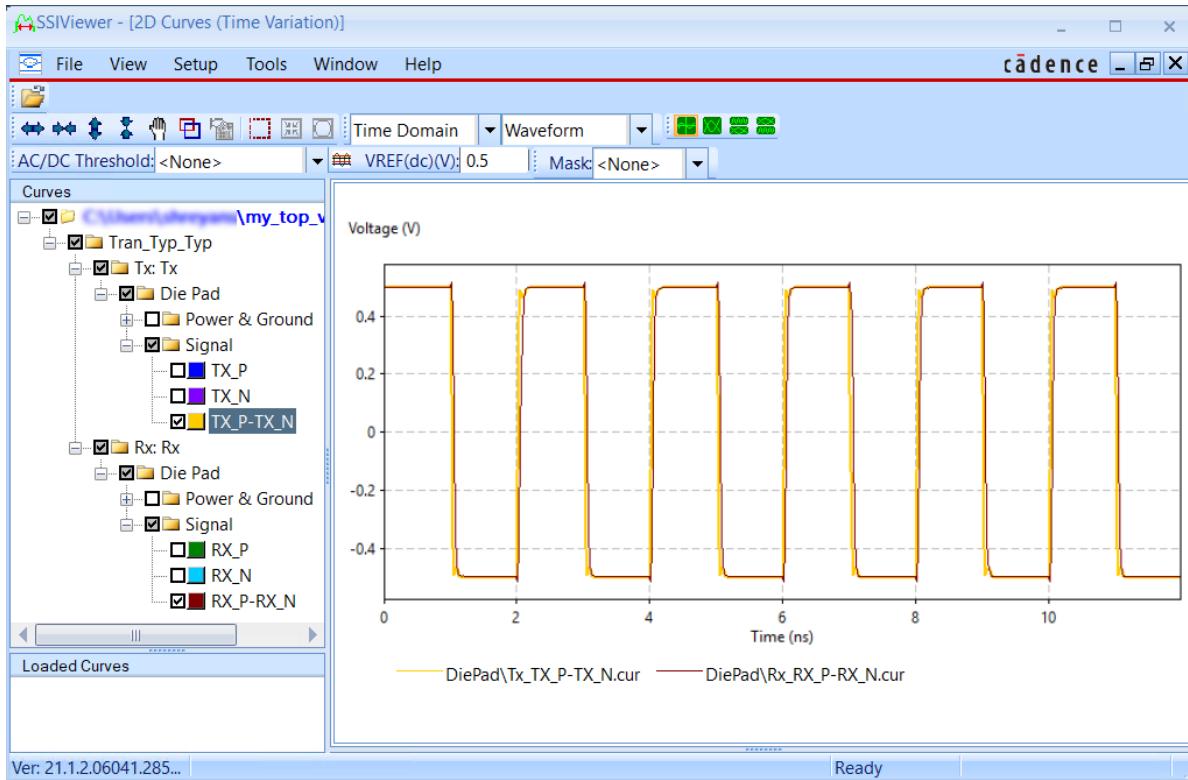
2. Check connectivity and define analysis options for the topology.
3. Simulate the topology.

On successful completion of the simulation run, the SSIViewer window opens. You can select signals of the Via block that connect to the transmitter and receiver blocks,

# Topology Workbench User Guide

## Using the Via Wizard

respectively. This helps to review the simulation waveform results generated between these blocks as shown below.



## **Topology Workbench User Guide**

### Using the Via Wizard

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# Modeling Pre-Layout Transmission Lines

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## *Important*

The pre-layout transmission line modeling feature is available in the Topology Explorer, Serial Link Analysis (SLA), and Parallel Bus Analysis (PBA) workflows.

Topology Workbench includes the pre-layout transmission line (TLine) modeling capability. This appendix covers the usage of this capability, with an example from the Topology Workbench – Topology Explorer workflow.

### **Related Topics**

- [Generating a TLine Model](#)
- [Connecting a TLine Block into the Topology](#)
- [Sweep Manager Support for Parameterized TLine Models](#)

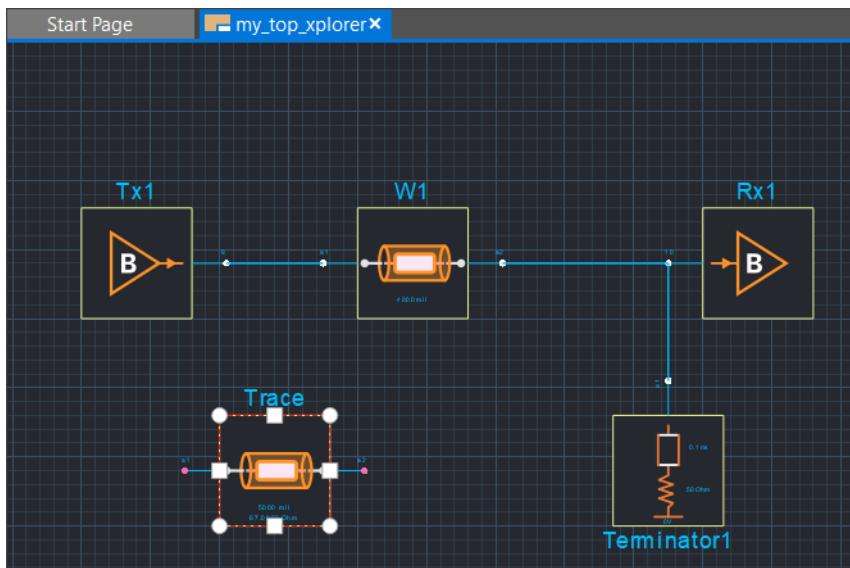
## Generating a TLine Model

For generating a TLine model, you need to perform the following tasks:

- [Placing a TLine Block](#)
- [Defining a Stack Up](#)
- [Specifying Surface Roughness](#)
- [Calculating TLine Parameters](#)
- [Generating a Model](#)

## Placing a TLine Block

In Topology Workbench, the TLines are represented using the Trace blocks. Such a block can be added from the Floating Toolbar as shown below:



Otherwise, you can open a default template-based SystemSI or Topology Explorer topology where TLine has been created already, such as, the *xtalk\_channel\_simple* template for the SLA workflow.

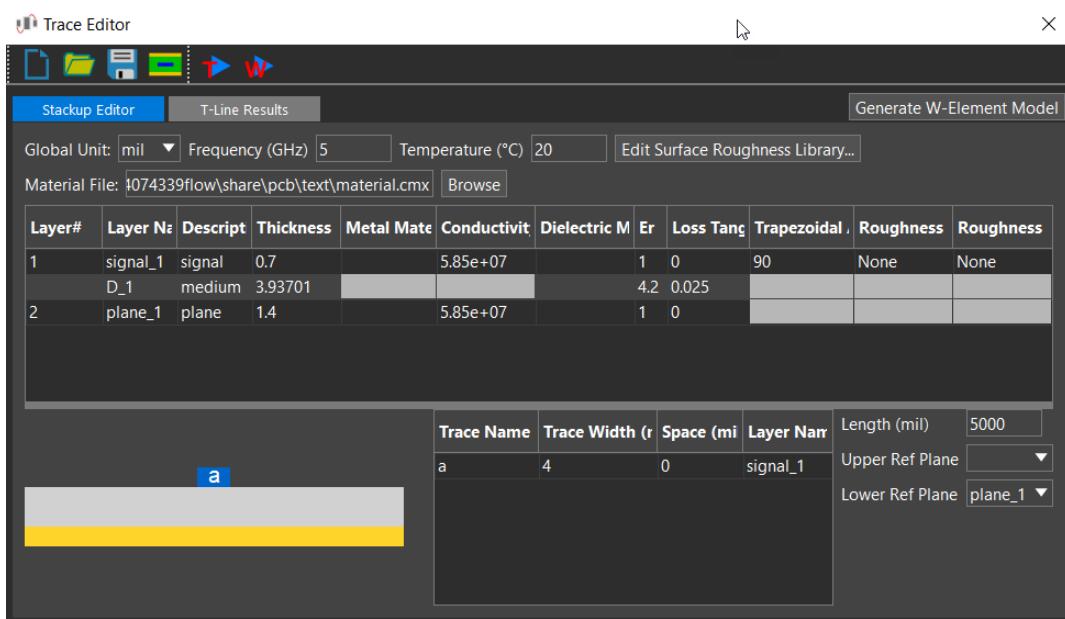
## Defining a Stack Up

1. Double-click the Trace block to open the corresponding properties in the Edit Properties Panel.
2. Click *Trace Editor*. The *Trace Editor* dialog box as shown below is displayed. The *Stackup Editor* tab is open by default.

# Topology Workbench User Guide

## Modeling Pre-Layout Transmission Lines

By default, the standard material file included in the installation, `material.cmx`, is selected. Ensure that the *Global Unit* is specified as `mil`.



**To utilize benefits of the Trace Editor shown above, ensure that you have installed the following two releases: Sigrity 2019 HF4 or a later version and OrCAD® and Allegro Release 17.4-2019 QIR2 or a later version.**

- Specify the *Frequency* and *Temperature* values.
- Modify the stack-up definition to change the dielectric Material for all conductor layers to FR42, as shown in the following figure.

Layer#	Layer Name	Description	Thickness	Metal Mate	Conductivity	Dielectric Material	Er	Loss Tang	Trapezoidal	Roughness	Roughness
1	signal_1	signal	0.7		5.85e+07		1	0	90	None	None
	D_1	medium	3.93701				4.2	0.025			
2	plane_1	plane	1.4		5.85e+07		1	0			

**Note:** The stack-up table above (and other table-based Topology Workbench forms) can be edited in a group. Select multiple rows in the table using the `Ctrl` or `Shift` key, and then click one of the column header cells. Edits made in the first selected row will then populate the other selected rows as well.

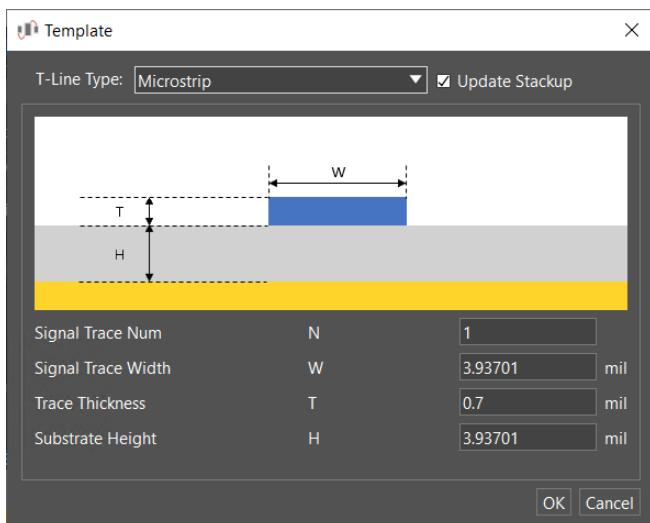
Optionally, you can choose to define the permittivity and loss tangent values directly instead of selecting a Dielectric Material from the library. If a Dielectric Material is selected and the Permittivity and/or Loss Tangent values are also defined, the explicit Permittivity and Loss

Tangent values will take precedence. Permittivity and Loss Tangent values can also be defined through parameters by clicking the *Edit Parameter* button, as described in the next section. This enables dielectric material properties to be swept using the Sweep Manager.

## Using Pre-Defined Template to Define a Stack Up

You can also use a pre-defined template. For this,

1. Click  in the toolbar of the *Trace Editor* dialog box. The *Template* dialog box opens as shown below:



2. Select one of the given *T-Line Types* from the list, that is, *Microstrip*, *Embedded Microstrip*, *Diff Coplanar Microstrip*, *Embedded Diff Coplanar Microstrip*, *Stripline*, *Diff Coplanar Stripline*, *Diff Broadside Coupled Stripline*, *Coplanar Waveguide*, and *Diff Coplanar Waveguide*.

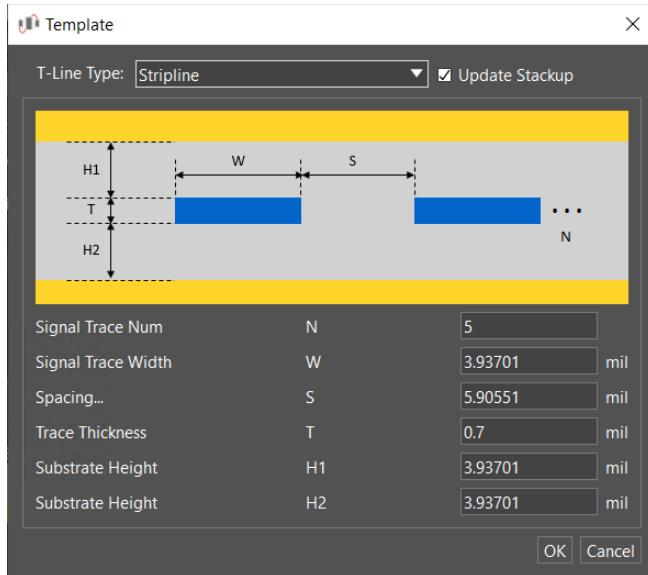
The graphical representation of the trace as per the selected TLine type is displayed to provide to you visual assistance.

3. Select the *Update Stackup* check box.

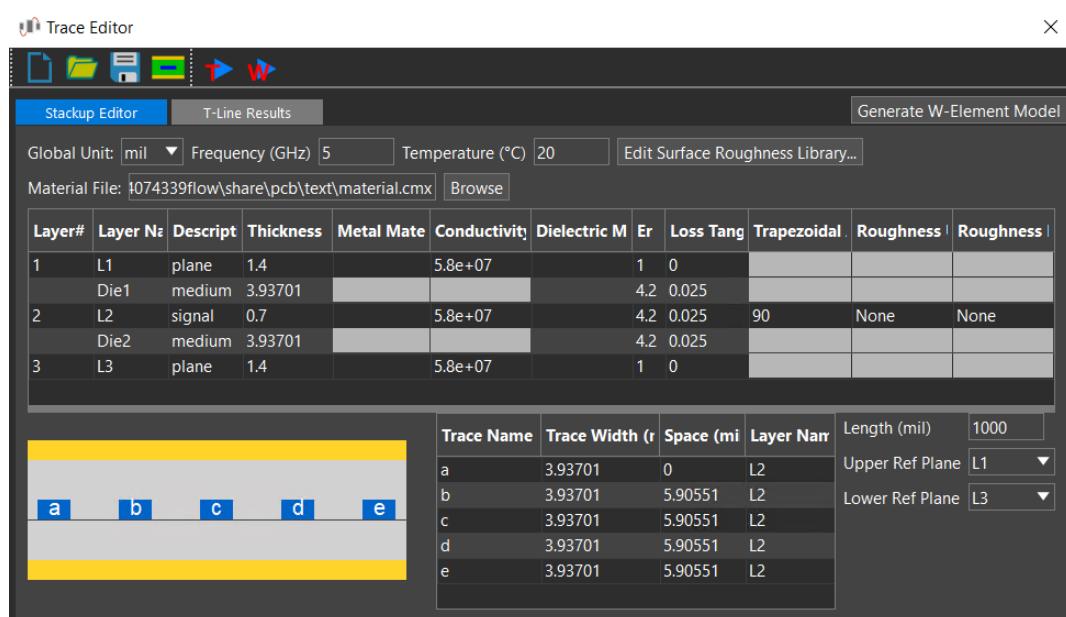
## Topology Workbench User Guide

### Modeling Pre-Layout Transmission Lines

4. Define the trace properties, such as, *Signal Trace Num*, *Signal Trace Width*, *Trace Thickness*, and *Substrate Height*.



5. Click *OK* to save the stackup settings. The *Template* dialog box closes and the *Trace Editor* shows the selected TLine pictorially along with the defined trace properties.



## Specifying Surface Roughness

Using the Trace Editor, you have the option to include surface roughness model of the conductor layers in the generated transmission line models. Separate roughness models can be defined for the upper and lower layers in the Roughness Upper and Roughness lower columns, respectively.

To specify a surface roughness model:

1. Click in the Roughness Upper (or Roughness Lower) column corresponding to the conductor layer. The cell changes to a list box that displays the available models.

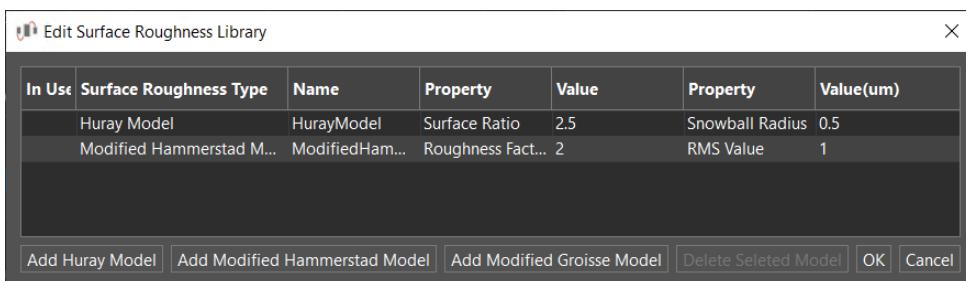
Layer#	Layer N#	Descript	Thickness	Metal Mate	Conductivity	Dielectric M	Er	Loss Tang	Trapezoidal	Roughness U	Roughness L
1	L1	plane	1.4	Die1	5.8e+07	4.2	1	0	90	None	None
2	L2	signal	0.7		5.8e+07		0.025				
3	L3	plane	1.4	Die2	3.93701	4.2	0.025	None	None	HurayModel	Mod...odel
					5.8e+07		0				

2. Select the model to be assigned to the layer.

All surface roughness models included in the Surface Roughness Library are listed in the drop-down list. To add surface roughness model to the library, perform the following steps.

1. Click *Edit Surface Roughness Library* in the *Trace Editor* dialog box.

The *Edit Surface Roughness Library* dialog box displays. Here you can add a Huray model and a Modified Hammerstad model for the layer.



2. Click *Add Huray Model*.

A row of Huray Model with default values is added to the table. You can modify the *Name*, and the values specified for *Surface Ratio* and *Snowball Radius*.

- The valid values for Surface Ratio are 0 and any value between 0 through 9.
- *Snowball Radius* can have any positive value. It is set to 0.5 times trace thickness by default.

**3. Click Add Modified Hammerstad Model.**

A row of Modified Hammerstad model with default values is added to the table. You can modify the *Name*, and the values specified for *Roughness Factor* and *RMS Value* for the model.

- For Roughness Factor, the valid values are 2, or any value greater than 2 and less than 10.
- RMS value can be 0 or any value less than 0.5 times the trace thickness.

Similarly, you can click *Add Modified Groisse Model* to add a row of the Modified Groisse model with default values.

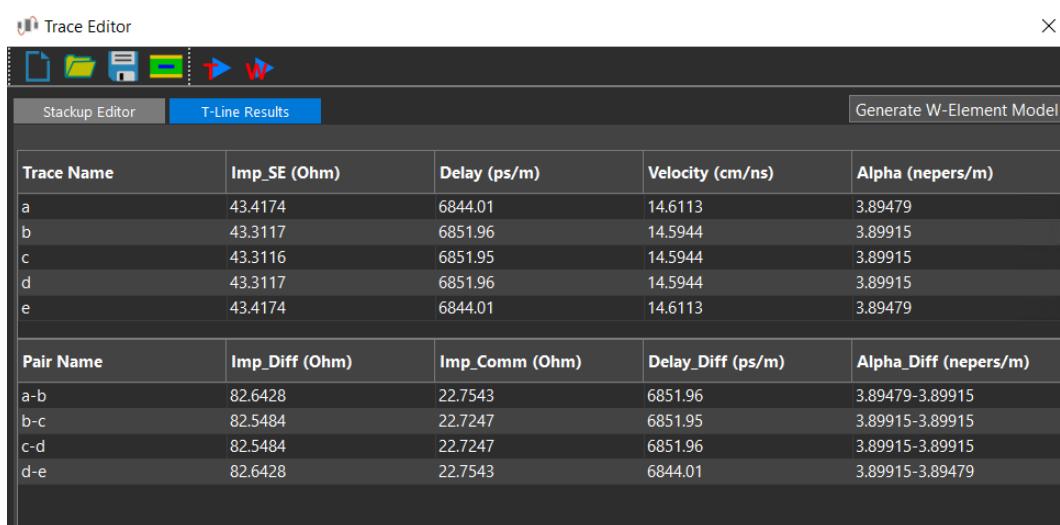
**4. Click *OK* after you have added all required models.**

The added models will now be available in the Roughness Upper and Roughness Lower drop-down list, for applying on layers.

**Note:** Before finalizing the model definitions, you can delete a model by selecting the corresponding row in the table and clicking the *Delete Selected Model* button.

## Calculating TLine Parameters

Once the definitions are completed, to calculate the TLine parameters, click  in the toolbar of the *Trace Editor* dialog box. The focus shifts from the *Stackup Editor* tab to the *T-Line Results* tab where a table of the calculated values is displayed. The table contains the *Trace Name*, *Imp\_SE (Ohm)*, *Imp\_Diff (Ohm)*, *Delay (ps/m)*, and the RLC values as shown below:



The screenshot shows the *Trace Editor* dialog box with the *T-Line Results* tab selected. The interface includes a toolbar with icons for file operations and a button to generate a W-Element Model. Below the tabs is a table with two sections: one for individual traces and one for pairs of traces.

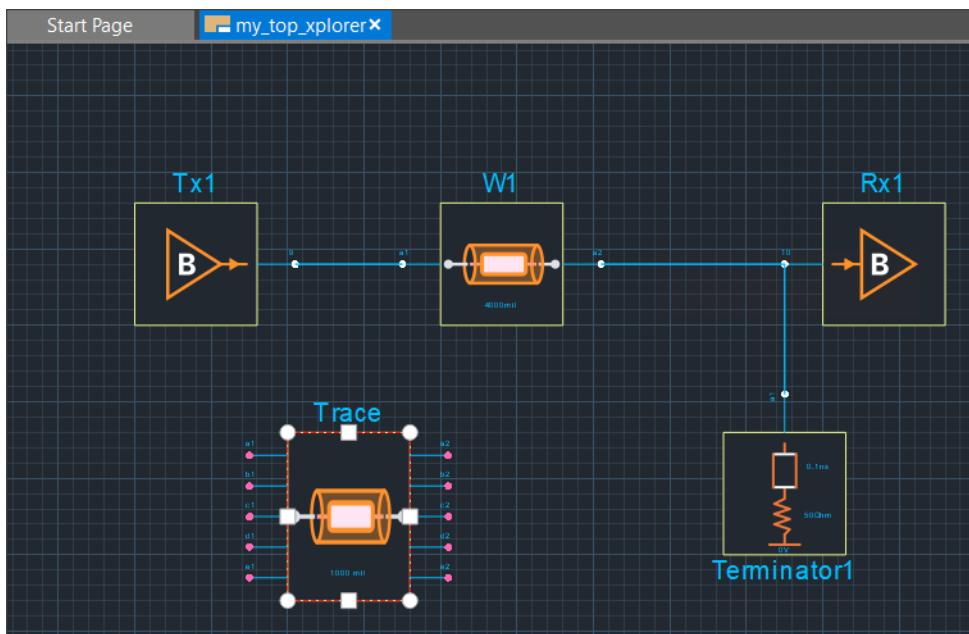
Trace Name	Imp_SE (Ohm)	Delay (ps/m)	Velocity (cm/ns)	Alpha (nepers/m)
a	43.4174	6844.01	14.6113	3.89479
b	43.3117	6851.96	14.5944	3.89915
c	43.3116	6851.95	14.5944	3.89915
d	43.3117	6851.96	14.5944	3.89915
e	43.4174	6844.01	14.6113	3.89479

Pair Name	Imp_Diff (Ohm)	Imp_Comm (Ohm)	Delay_Diff (ps/m)	Alpha_Diff (nepers/m)
a-b	82.6428	22.7543	6851.96	3.89479-3.89915
b-c	82.5484	22.7247	6851.95	3.89915-3.89915
c-d	82.5484	22.7247	6851.96	3.89915-3.89915
d-e	82.6428	22.7543	6844.01	3.89915-3.89479

## Generating a Model

To generate a model, in the *Trace Editor* dialog box, click  in the toolbar or the *Generate W-Element Model* button. It populates the model info in the *Edit Properties* panel. The Trace block on the canvas is updated with the model information.



## Connecting a TLine Block into the Topology

After you have generated the TLine model for the Trace block, you need to connect it to the other blocks. For information, see [Connecting the Blocks on the Canvas](#).

## Sweep Manager Support for Parameterized TLine Models

The TLine parameters that were set earlier can also be swept in the *Sweep Manager*.

To set the TLine sweep parameters and view the corresponding simulation results:

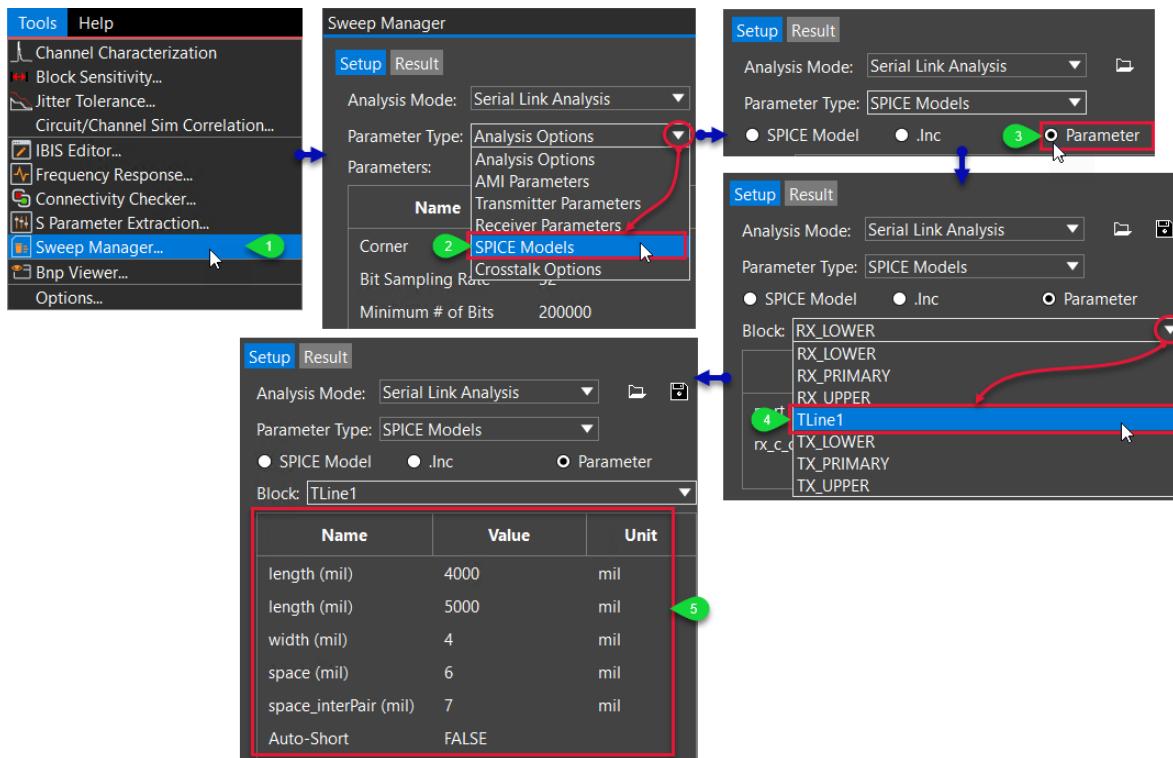
1. Click *Tools – Sweep Manager* from the menu bar. The *Sweep Manager* panel opens.
2. Select *Spice Models* from the *Sweep Type* list in the *Setup* tab.
3. Select *Parameter* from the displayed options.

## Topology Workbench User Guide

### Modeling Pre-Layout Transmission Lines

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4. Select *TLine* from the *Block* list. The table displays the defined TLine parameters, such as, length, width, and space.



5. Double-click the parameters that need to be added to the sweep list. The table listing the selected sweeps is updated accordingly.
6. Specify the *Min*, *Max*, and *Step*. The *Step Count* and *Total Iterations* are calculated automatically based on these three values. You can also optionally specify a *Value List*.
7. Click *Run Sweeps*. The simulation starts to run and the progress is displayed in the status bar. In addition, the *Result* tab of the *Sweep Manager* panel opens to display the results of the *Current* run.

**Note:** You can choose the parameters for which you want to see the results in the *Current* tab. For more information, see [Filtering the Sweep Simulation Results](#).

8. Click *Show Result* to open the SSIViewer to view the simulation results. For more information, see [Viewing the Sweep Simulation Results](#).

# **Topology Workbench User Guide**

## Modeling Pre-Layout Transmission Lines

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# Using Extracted Interconnect Models from Layout

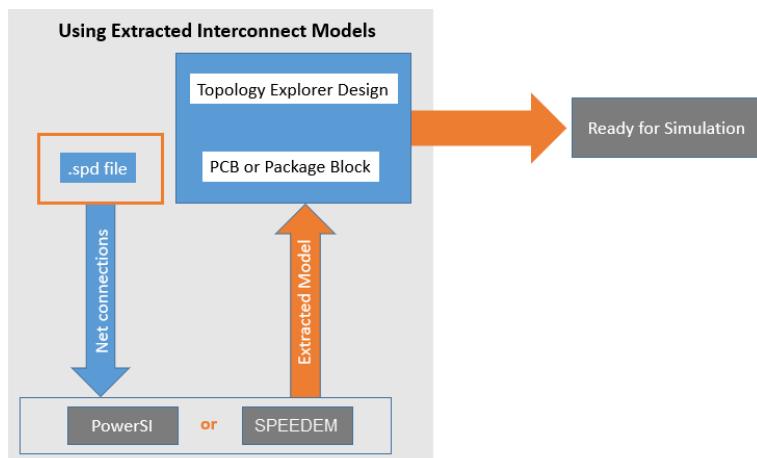
 *Important*

The physical layout extraction and simulation feature is available in Topology Explorer, SystemPI Serial Link Analysis (SLA), and Parallel Bus Analysis (PBA) modes.

The Layout Association functionality in Topology Workbench provides direct integration with Sigrity Clarity, PowerSI, and SPEEDEM Generator (SPDGEN), enabling automation in the extraction and model generation for blocks in the Topology Workbench topologies that are based on physical layout.

**Note:** For the purpose of understanding, this appendix explains extraction of model using SPEEDEM.

The following figure shows the flow of using extracted interconnect models from layout:

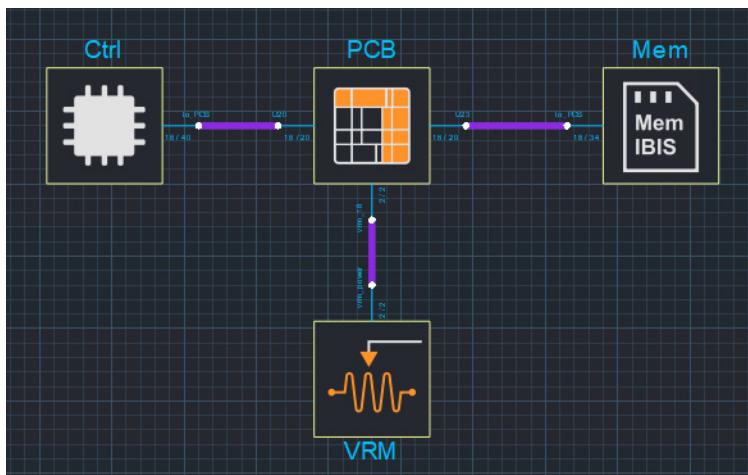


In the following sections, you can read about:

- [Extracting the Layout of a Model Using SPEEDEM](#)
- [Simulating Circuits with Direct FDTD-Based Approach](#)

## Extracting the Layout of a Model Using SPEEDEM

Consider a sample topology, as shown below, where initial connections have been made between the blocks including a *Controller*, *Memory*, *PCB*, and *VRM* component.



Assume that the *PCB* block has a physical layout (.spd file) and you would want to associate it to the corresponding block.

## Supported Types of Extraction

The level of extraction you select often depends on where you are in the design process.

Extraction	Description	When to Use
Level 1	Is the simplest type of extraction, where trace-trace and via-via coupling is excluded	If only some critical signals are routed, perform a Level 1 extraction, to focus on reflection, termination, and other topology-related issues.  Level 1 models are good choice when you need to get initial results in a short period of time.

## Topology Workbench User Guide

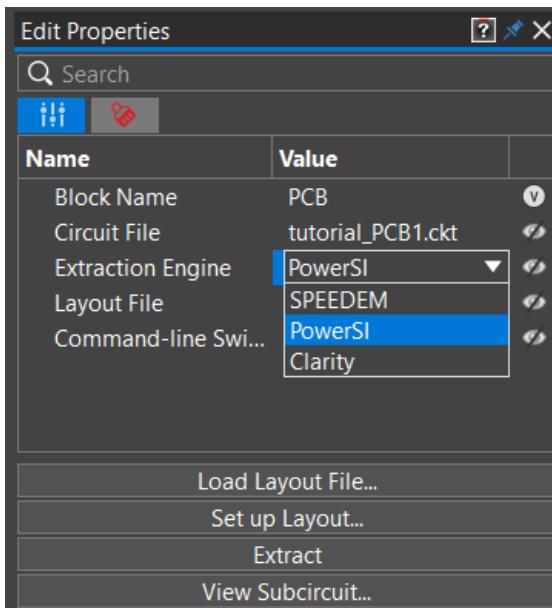
### Using Extracted Interconnect Models from Layout

Extraction	Description	When to Use
Level 2	Includes these couplings in the extracted model, so that crosstalk effects are included in the resulting simulation	If an entire critical bus is routed, a Level 2 extraction may be run, to include the effects of coupling on signal quality and timing.
Level 1 and 2 extractions with <i>SPEEDEM</i> both assume ideal power. This can save significant time, as the complex PDN, or power distribution network (for example: plane shapes and decoupling capacitors) is not extracted. These levels <b>do not</b> include non-ideal power effects. In the resulting models, the blocks have a SPICE subcircuit and MCP header.		

## Setting Up Layout Extraction

The following procedure walks you through the layout extraction tasks:

1. To associate a physical layout with the package block, double-click the *PCB* block. The Edit Properties Panel opens with the focus on the *Component Properties* tab (  ).



The following parameters related to layout extraction are displayed: *Extraction Engine*, *Layout File*, and *Command-line Switch*. The *Set up Layout* and *Extract* buttons are also displayed.

2. Select the *Extraction Engine* from the list. The following options are available to choose:

## Topology Workbench User Guide

### Using Extracted Interconnect Models from Layout

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- SPEEDEM**

Used for level 1 and Level 2 extraction explained in the [Supported Types of Extraction](#) section above.

- PowerSI**

Used for level 3 extraction.

- Clarity**

 **Important**

Topology Workbench checks out a PowerSI license for both *Set up Layout* and *Extract* unless you are using a license where Topology Workbench and PowerSI are included, such as, the Power-Aware SI option. The license check out rule also applies to Clarity extraction engine.

3. In the *Layout File* field, specify the layout file (.spd) to be associated with the PCB block.

**Note:** If the layout file is not specified in Topology Workbench, you can do so in the SPEEDEM, PowerSI, or Clarity window depending on the extraction engine you choose to use. Thereafter, make sure that the *Load Layout File* option in the *Model Extraction* workflow panel of the tool is clicked to load the layout file.

4. Click one of the following buttons in the Topology Workbench window's Edit Properties panel:

- Set up Layout***

The extraction engine selected in [step 2](#) is launched. The *Model Extraction* workflow opens in the Layout Workbench window for SPEEDEM, PowerSI, or Clarity based on the tool selected from the *Extraction Engine* list.

- Extract***

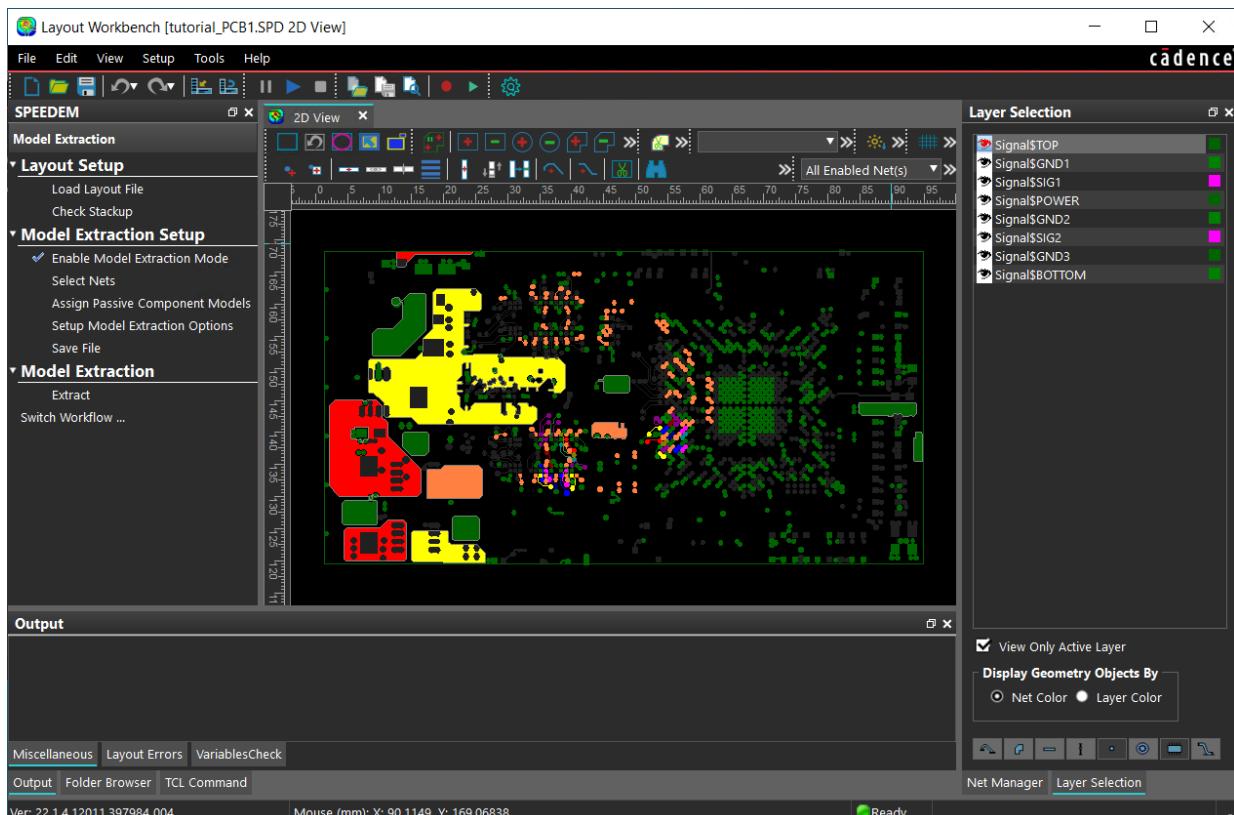
The extraction engine runs in a batch mode. After the extraction completes, the top-level SPICE model file is extracted and saved in the same location as the project file, along with four .sp files.

For understanding the process, select **SPEEDEM** and then click ***Set up Layout***.

# Topology Workbench User Guide

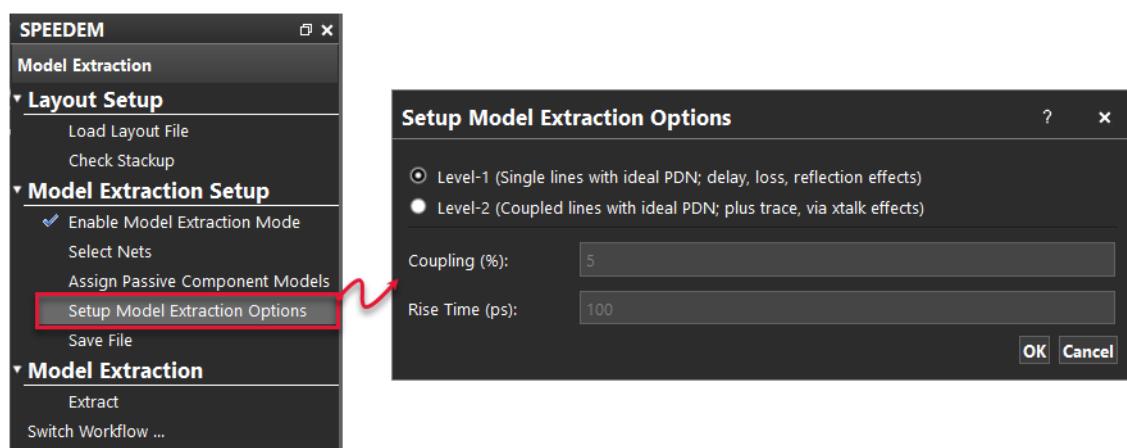
## Using Extracted Interconnect Models from Layout

5. Select an appropriate license in the *Choose License Suites* dialog box if prompted to do so. The design opens in the Layout Workbench window.



The workflow that appears walks you through the key setup tasks to control the extraction process.

6. Click *Setup Model Extraction Options* in the workflow.



# Topology Workbench User Guide

## Using Extracted Interconnect Models from Layout

- a. Select the level of extraction: *Level-1* or *Level-2*.

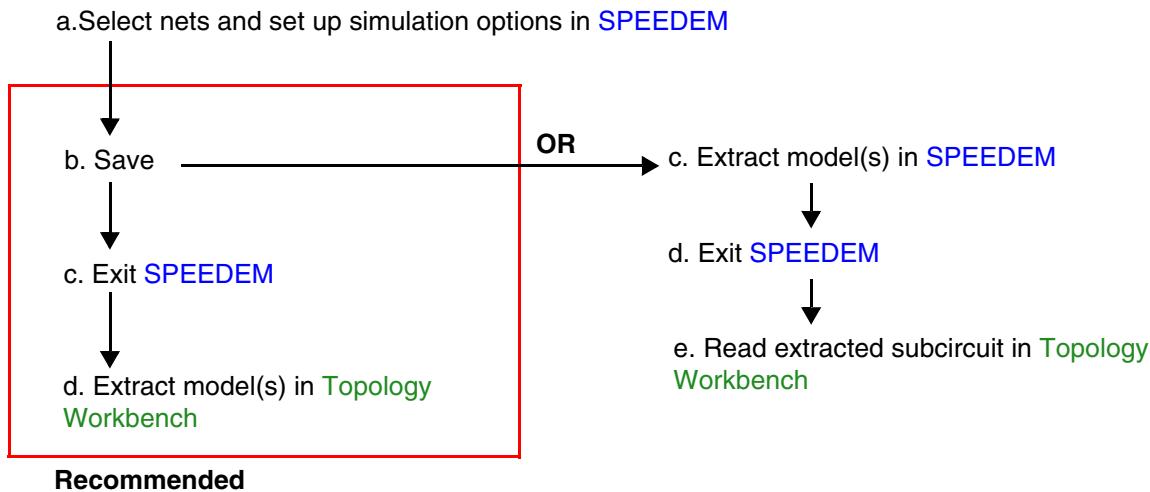
For *Level-1*, the *Coupling* and *Rise Time* fields cannot be edited. The extraction is done using the default values displayed in these read-only fields.

For *Level-2*, the *Coupling* and *Rise Time* fields are enabled and the default values are displayed. You can change the values as per your design requirements.

For information on how to use the SPEEDEM options, refer to the SPEEDEM documentation, particularly *Model Extraction Tutorial*.

- b. Click *OK*.

There are two ways to read the model extraction in the Topology Workbench <-> SPEEDEM workflow:



In this topic, the extraction has been shown in Topology Workbench.

Verify the stackup to ensure that it is correct, and if required, assign discrete models, such as terminating resistors, to be used with the signals of interest.

7. Save the .spd file and exit the extraction tool using the workflow.

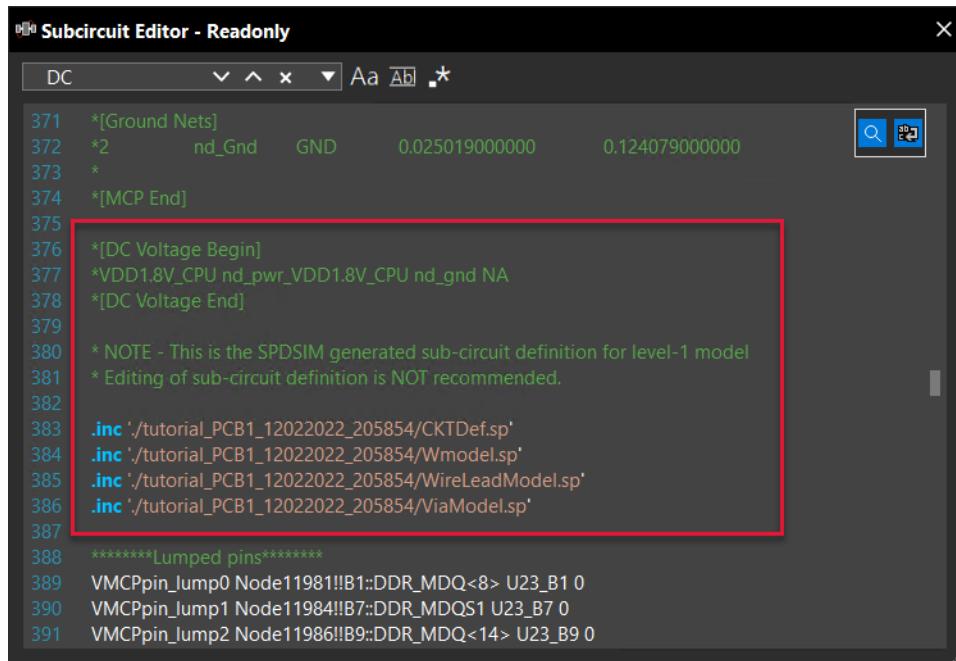
After the layout file is saved, it gets passed to Topology Workbench.

8. Click *Extract* in the *Edit Properties* panel of Topology Workbench.

# Topology Workbench User Guide

## Using Extracted Interconnect Models from Layout

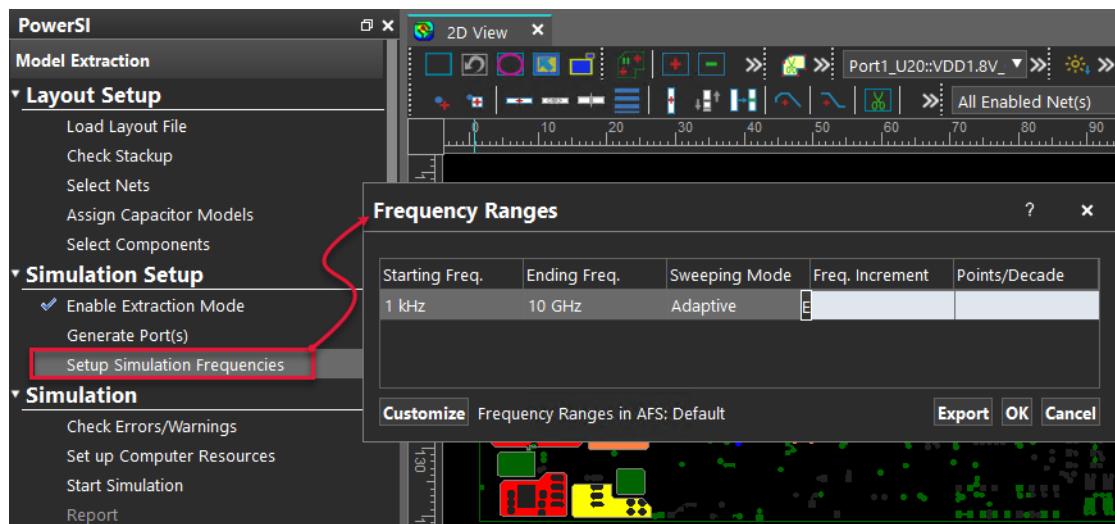
The extracted model for the block is now ready to be used in simulations. To view the updated subcircuit information, in the *Edit Properties* panel, click *View Subcircuit*. The *Subcircuit Editor* opens.



```
Subcircuit Editor - Readonly
DC  Aa Ab *
371 *[Ground Nets]
372 *2      nd_Gnd   GND      0.025019000000    0.124079000000
373 *
374 *[MCP End]
375
376 *[DC Voltage Begin]
377 *VDD1.8V_CPU nd_pwr_VDD1.8V_CPU nd_gnd NA
378 *[DC Voltage End]
379
380 * NOTE - This is the SPDSIM generated sub-circuit definition for level-1 model
381 * Editing of sub-circuit definition is NOT recommended.
382
383 .inc './tutorial_PCB1_12022022_205854/CKTDef.sp'
384 .inc './tutorial_PCB1_12022022_205854/Wmodel.sp'
385 .inc './tutorial_PCB1_12022022_205854/WireLeadModel.sp'
386 .inc './tutorial_PCB1_12022022_205854/ViaModel.sp'
387
388 *****Lumped pins*****
389 VMCPPin_Jump0 Node11981!!B1::DDR_MDQ<8> U23_B1 0
390 VMCPPin_Jump1 Node11984!!B7::DDR_MDQS1 U23_B7 0
391 VMCPPin_Jump2 Node11986!!B9::DDR_MDQ<14> U23_B9 0
```

The *DC Voltage* check box is selected automatically if a *[DC Voltage Begin]* section as shown above is generated.

**Note:** When you select *PowerSI* as the *Extraction Engine* and click *Set up Layout* in the *Edit Properties* panel of Topology Workbench, PowerSI opens in Layout Workbench. Thereafter, update the *Setup Simulation Frequencies* as shown below:



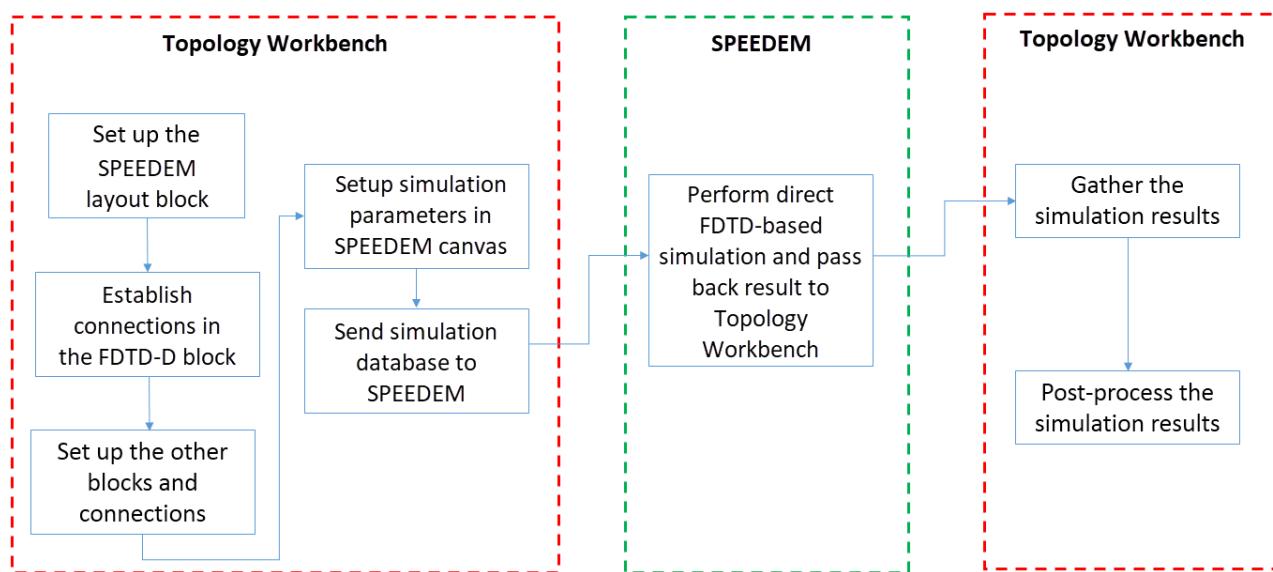
## Simulating Circuits with Direct FDTD-Based Approach

A model-based approach is used for transient simulation with Topology Workbench. However, there are challenges applying time domain simulation to large S-parameters with many ports. Stability and convergence challenges when encountered can often be overcome by applying Broadband SPICE to extract a micromodel. Alternatively, the unique "FDTD-direct" method employed by SPEEDEM can solve the physical layout directly, avoiding having to deal with very large S-parameters and the challenges associated with simulating them in the time domain. The FDTD-direct method has shown to be very robust for large physical structures such as wide DDR buses, and should be considered for large Level 3 layout association simulation challenges.



**An FDTD-D block is designed for non-ideal power only. Therefore, using an FDTD-D block is not recommended if you want to run the simulation in ideal power supply mode; use a SPICE block instead and extract level 1 or 2 model for simulation.**

Layout association simulation (Level 3) combines the advantages of both SPEEDEM and Topology Workbench.



The layout association simulation is supported for bus simulation in PBA, transient simulation in Topology Explorer, and characterization in SLA.

## **Before You Begin**

When using a SPEEDEM block, ensure that:

- The *Circuit Simulator* is set to *SPDSIM* in the *Analysis Options* panel – Circuit Simulation tab, which can be accessed by clicking *Set Analysis Options* in the *Workflow* panel.

**Note:** When SPDSIM is used for running the simulation, the options for specifying initial DC voltages for the circuit simulator are not supported.

- An SPD file is available for the model.

For detailed information on SPD files, see the SPEEDEM documentation.

## **Setting Up a SPEEDEM Link Block**

This section walks you through the steps of level 3 simulation in Topology Workbench:

1. Click the *FDTD-D* block in the floating toolbar.

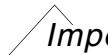
Only one *FDTD-D* block is allowed in a design. If there is already one *FDTD-D* block, the *FDTD-D* block gets disabled in the floating toolbar.

2. Double-click the *FDTD-D* block to open the *Edit Properties* panel. The following properties can be set:

- Block Name*
- Layout File* in the .spd format
- Layout Simulation (FDTD)* check box
- DC Voltage* check box

**Note:** The *DC Voltage* check box is available only when the *Layout Simulation (FDTD)* check box is not selected. When you perform level 1 or 2 extraction, Topology Workbench automatically finds all DC nets connected to the selected signal nets and includes them in the extracted SPICE model. When the *DC Voltage* check box is checked, the extracted voltages are listed. This is especially useful for address bus extraction.

3. Ensure the *Layout Simulation (FDTD)* check box is selected.

 *Important*

When this check box is selected, it means that layout simulation will be applied when you run the simulation. If not selected, model simulation will be run.

You can launch the SPEEDEM application or just extract the Level-1 or Level-2 model.

*Set up Layout*

Opens SPEEDEM to perform the simulation setup for layout association. An additional workflow is shown along with other default workflows. This workflow will not be shown if SPEEDEM is opened directly.

*Extract*

Topology Workbench calls SPEEDEM to extract the Level-1 or Level-2 model.

4. Ensure the *Enable Base Mode* option is selected.
5. Verify the stackup to ensure that it is correct.
6. If required, assign discrete models, such as terminating resistors, to be used with the signals of interest. Also, ensure that the required decoupling capacitors are assigned.
7. Click *Setup Options for Model Extraction* in the workflow.

**a.** Select the level of extraction: *Level-1* or *Level-2*.

For *Level-1*, the *Coupling* and *Rise Time* fields cannot be edited. The extraction is done using the default values displayed in these read-only fields.

For *Level-2*, the *Coupling* and *Rise Time* fields are enabled and the default values are displayed. You can change the values as per your design requirements.

For information on how to use the SPEEDEM options, refer to the SPEEDEM documentation, particularly *Model Extraction Tutorial*.

- b.** Click *OK*.
8. Click *Save File*.  
The *Speed Generator File Saving Option* dialog box is displayed.
  9. Specify the error checking options.
  10. Click *OK*.
  11. Exit SPEEDEM.
  12. Click *Extract* in the *Edit Properties* panel of Topology Workbench.

## **Topology Workbench User Guide**

### Using Extracted Interconnect Models from Layout

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You now have a power-aware simulation. You can make changes to the layout designs and perform “What-if” analysis. During simulation, the SPEEDEM hybrid solver and Finite Difference Time Domain (FDTD) engines work together to dynamically mesh and simulate the layout. This approach is well-suited to the large bus-level simulations commonly seen in DDR designs, where the inclusion of non-ideal power effects is required. Waveforms and outputs are displayed in Topology Workbench the same way as if they were produced from a model-based flow. Report generation and post-processing is done in Topology Workbench as usual.

**Topology Workbench User Guide**  
Using Extracted Interconnect Models from Layout

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# Using the Sweep Manager

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The *Sweep Manager* panel in Topology Workbench allows you to set up different values of key parameters, such as propagation delay value for DATA/STROBE signal nets and run sweep, that is, simulation corresponding to each value of a parameter. This provides an efficient feature in Topology Workbench to explore the effects of different values of a parameter on the signal integrity performance of the topology.

**Note:** The functionality extended using the *Sweep Manager* is available in the Topology Explorer, Serial Link Analysis (SLA), Parallel Bus Analysis (PBA), and SystemPI – PDN Impedance and Power Ripple Analysis workflows. However, to illustrate the use of the *Sweep Manager*, this appendix has used the interface from the SLA workflow. For some options, the available values are different, but the interface and working of the panel is essentially the same in the other Topology Workbench workflows.

## Related Topics

- [Accessing the Sweep Manager](#)
- [Setting Up the Sweep Manager](#)
- [Viewing the Sweep Simulation Results](#)
- [Exporting the Sweep Simulation Results](#)
- [Filtering the Sweep Simulation Results](#)
- [Other Sweep Features](#)

## Accessing the Sweep Manager

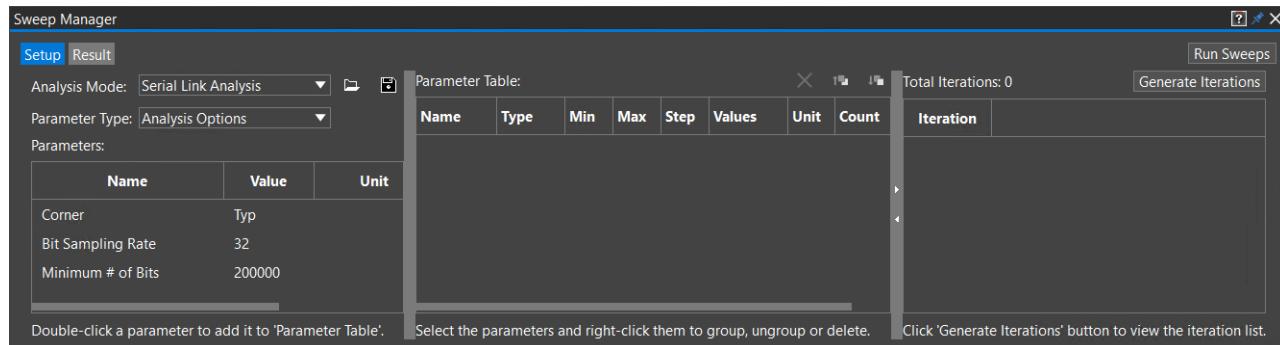
To open the *Sweep Manager* panel,

- Click *Tools – Sweep Manager* from the menu bar.

## Topology Workbench User Guide

### Using the Sweep Manager

The panel opens with the following tabs—*Setup* and *Result*.



## Setting Up the Sweep Manager

The *Setup* tab in the *Sweep Manager* panel is divided into the following sections:

- *Analysis Mode*, *Parameter Type*, and *Parameters* settings
- *Parameter Table*
- *Total Iterations*

To set up the sweeps:

1. Select the required *Analysis Mode*.

By default, this list displays the following values depending on the workflow:

Topology Explorer	<i>Transient Analysis</i>
Serial Link Analysis	<i>Serial Link Analysis</i>
Parallel Bus Analysis	<i>Parallel Bus Analysis</i>
SystemPI – PDN Impedance and Power Ripple Analysis	<i>Power Ripple, PDN Impedance</i>

2. Choose the relevant *Parameter Type*.

This list displays the following values depending on the workflow:

Topology Explorer	<i>Analysis Options, Transmitter Parameters, Receiver Parameters, SPICE Models</i>
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## Topology Workbench User Guide

### Using the Sweep Manager

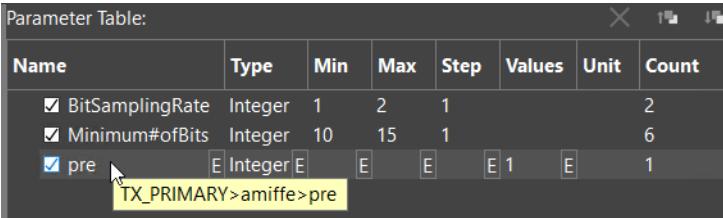
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Serial Link Analysis	<i>Analysis Options, AMI Parameters, Transmitter Parameters, Receiver Parameters, SPICE Models, Crosstalk Options</i>
Parallel Bus Analysis	<i>Analysis Options, Memory Parameters, Controller Parameters, SPICE Models</i>
SystemPI – PDN Impedance and Power Ripple Analysis	<i>Analysis Options, SnP Models, SPICE Models, What-If Decaps</i>

The *Parameter Table* is populated with the parameters corresponding to the selected *Parameter Type*. For example, in the SLA workflow, if you selected the *Parameter Type* as *Analysis Options*, the *Parameters* table displays the *Corner*, *Bit Sampling Rate*, and *Minimum # of Bits* values that you had set in the *Analysis Option* panel. On the contrary, in the PBA workflow, selecting the *Parameter Type* as *Analysis Options* populates the *Parameters* table with the *Corner*, *Data Rate (Gbps)*, *Minimum # of Bits*, and *Direction* values.

3. Double-click the required parameters from the *Parameters* table to add to the *Parameter Table* section.

**Note:** You can repeat step 2 and then step 3 to add sweep parameters of different types. The *Name* column of the *Parameter Table* section displays the name of the chosen sweep parameter. When you move the cursor on the name of a parameter, the tooltip shows concatenated information showing its type, the related block and signal names, and so on.



The screenshot shows the 'Parameter Table' dialog box with the following data:

Name	Type	Min	Max	Step	Values	Unit	Count
<input checked="" type="checkbox"/> BitSamplingRate	Integer	1	2	1			2
<input checked="" type="checkbox"/> Minimum#ofBits	Integer	10	15	1			6
<input checked="" type="checkbox"/> pre	Integer	E	E	E	E 1 E	E	1

A tooltip is visible at the bottom of the table, showing the concatenated information: TX\_PRIMARY>amiffe>pre.

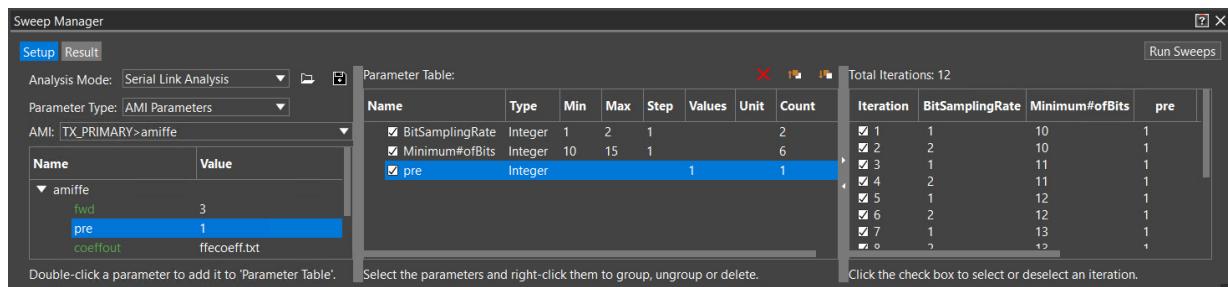
4. Specify the *Min*, *Max*, and *Step* values in the *Parameter Table* section.

The *Count* is calculated automatically based on the *Max* value.

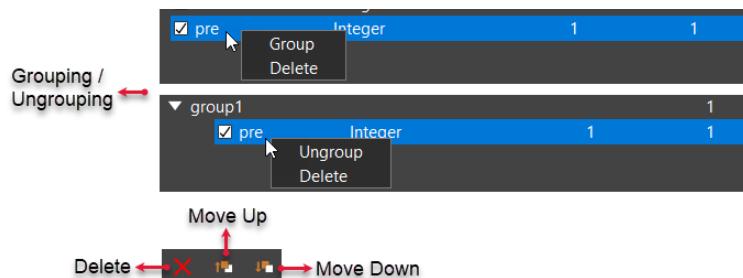
# Topology Workbench User Guide

## Using the Sweep Manager

After the required values for all sweep items have been added, the *Total Iterations* table is populated with a list of iterations that Topology Workbench calculates automatically based on the data entered in the *Parameter Table* section.



**Note:** When you right-click a parameter, a shortcut menu is displayed to let you group, ungroup, or delete sweep parameters. You can also reset the sweep sequence for the selected parameters.



5. Deselect the check boxes adjacent to the *Iterations* that should be excluded. By default, Sweep Manager adds all iterations for sweep simulation.
6. Click *Run Sweeps*. A confirmation message is displayed stating the number of iterations that would be required when sweep simulation is run on the topology.
7. Click *Yes* to continue.

The simulation run status is displayed in the status bar of the Topology Workbench window. In addition, the *Result – Current* tab of the *Sweep Manager* panel is opened where the simulation results are summarized in a tabular format.

The screenshot shows the 'Sweep Manager' window with the 'Result' tab selected. The 'Current' tab displays a table of simulation results for three iterations. The columns include Iteration, Folder, EyeContourHeight, EyeContourJitter, EyeContourNIN, COM, SNR, BER\_EyeHeight, BER\_EyeWidth, LogBER, Delay, IntraPairSkew, BitSamplingRate, and Minimum#ofBits. The results for iterations 1, 2, and 3 are listed, showing various performance metrics.

# **Topology Workbench User Guide**

## Using the Sweep Manager

If the sweep simulation run has failures, a message box is displayed to seek your confirmation for displaying the log file. When you click Yes, a new tab is displayed in the Topology Workbench window for a log of messages, as shown below:

You can repeat the steps described above to reset the sweep parameters and rerun the sweep simulation. The result summary on the *Result – Current* tab is updated automatically as per the current simulation run, while the results of the previous simulation run are moved to the *Result – History* tab as shown below.

Sweep Manager A															?		
Setup		Result															
Current		History													Show Result...	Select Measurements...	Export...
Iteration	Folder	EyeContourHeight	EyeContourJitter	EyeContourNIN	COM	SNR	BER_EyeHeight	BER_EyeWidth	LogBER	Delay	IntraPairSkew	BitSamplingRate	Minimum#ofBits	StimulusO			
	*	*	*	*	*	*	*	*	*	*	*	*	*	*			
<input checked="" type="checkbox"/> 1	result\5\Chan...	0	1	0.75	0	1			-12	5.74...	49.6212	2	8	0.9			
<input checked="" type="checkbox"/> 2	result\5\Chan...	0	1	0.83	0	1			-12	5.74...	49.6212	3	10	0.9			

Double-click an iteration to show the results.

Sweep Manager														
Setup		Result												
Current		History												
Iteration	Folder	EyeContourHeight	EyeContourJitter	EyeContourNJN	COM	SNR	BER_EyeHeight	BER_EyeWidth	LogBER	Delay	IntraPairSkew	BitSamplingRate	Minimum#ofBits	pre
■ 1	result\2\Chan...	0	1	0.75	0	1			-12	5.74...	49.6212	2	11	1
■ 1	result\4\Chan...	0	1	0.75	0	1			-12	5.74...	49.6212	2	8	
■ 2	result\4\Chan...	0	1	0.75	0	1			-12	5.74...	49.6212	2	9	
■ 3	result\4\Chan...	0	1	0.75	0	1			-12	5.74...	49.6212	2	10	

If you have set multiple Log BER values in the [Channel Simulation – Serial Link Analysis](#) tab of the *Analysis Options* panel, the sweep results are generated for each specified LBER

## Topology Workbench User Guide

### Using the Sweep Manager

value. The cells under the *LBER* column provide a list of the specified values, as shown below. Selecting a different value from the list box under the *LBER* column has an impact on the values displayed in the *BER\_Eye Height* and *BER\_Eye Width* columns.

**Note:** The *Channel Simulation* tab is displayed in the *Analysis Options* panel when you are using the SLA workflow or when the *Use Channel Simulator* check box is selected in the PBA workflow.

The screenshot shows two panels: 'Analysis Options' and 'Sweep Manager'.

**Analysis Options Panel:** This panel has tabs for 'Circuit Simulation' and 'Channel Simulation'. Under 'Channel Simulation', there are sections for 'Characterization' (Launch Delay 0 ns, Step Duration 30 ns, VMeas), 'Eye Distribution Method' (Time Domain Waveform selected), and 'BER\_Eyes' (checkbox checked, dropdown menu showing 'Time scale (eye width)', 'Voltage scale (eye height)', and 'Both time and voltage'). A range 'LBERs: -12 to -15' is also present. A red box highlights the 'Both time and voltage' checkbox and the LBER range input field.

**Sweep Manager Panel:** This panel has tabs for 'Setup' and 'Result'. The 'Result' tab is active, showing the 'Current' iteration table. The table includes columns: Iteration, Folder, Eye Contour Height (mV), Eye Contour Jitter (UI), Eye Contour NJN, COM (dB), BER\_Eye Height (mV), BER\_Eye Width (UI), LBER, Delay (ns), Intra-Pair Skew (ps), and Bits. The 'LBER' column for iteration 1 shows a dropdown menu with options: -12, -12, -13, -14, and -15. A red arrow points from the 'LBERs' input field in the Analysis Options panel to the dropdown menu in the Sweep Manager panel, indicating that the range specified in the Analysis Options is reflected in the LBER column of the Sweep Manager results table.

Iteration	Folder	Eye Contour Height (mV)	Eye Contour Jitter (UI)	Eye Contour NJN	COM (dB)	BER_Eye Height (mV)	BER_Eye Width (UI)	LBER	Delay (ns)	Intra-Pair Skew (ps)	Bits
1	result\3\Chan_Typ_Typ_1	113	0.67	0.93	5.49	57	0.21	-12	4.42682	5.9906	31
2	result\3\Chan_Typ_Typ_2	123	0.68	0.94	5.74	80	0.2	-12	4.42682	5.9906	32
3	result\3\Chan_Typ_Typ_3	112	0.66	0.94	5.40	58	0.19	-13	4.42682	5.9906	33
								-14			
								-15			

## Viewing the Sweep Simulation Results

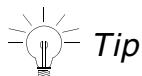
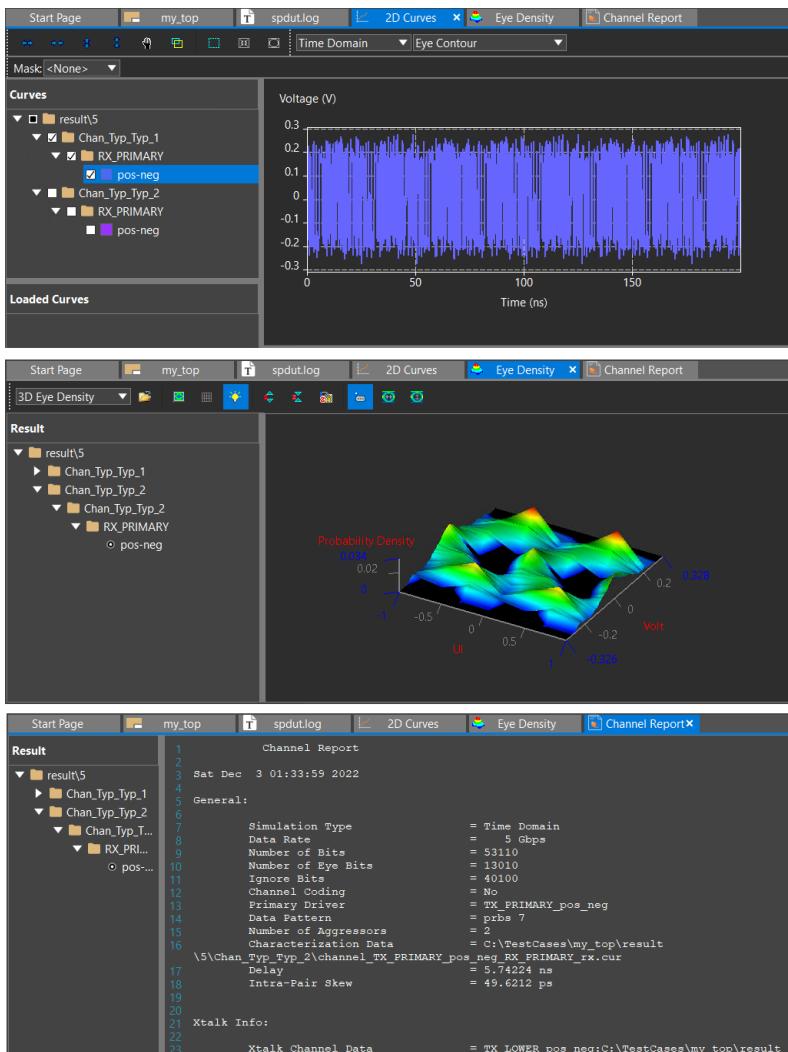
In the *Result – Current* tab, to view the sweep simulation results:

1. Select or deselect the check boxes adjacent to the iterations of interest.

## Topology Workbench User Guide

### Using the Sweep Manager

2. Click *Show Result*. The 2D Curves, Eye Density, and Channel Report tabs open in the Topology Workbench window.



Alternatively, double-click an iteration to view the corresponding simulation results.

## Exporting the Sweep Simulation Results

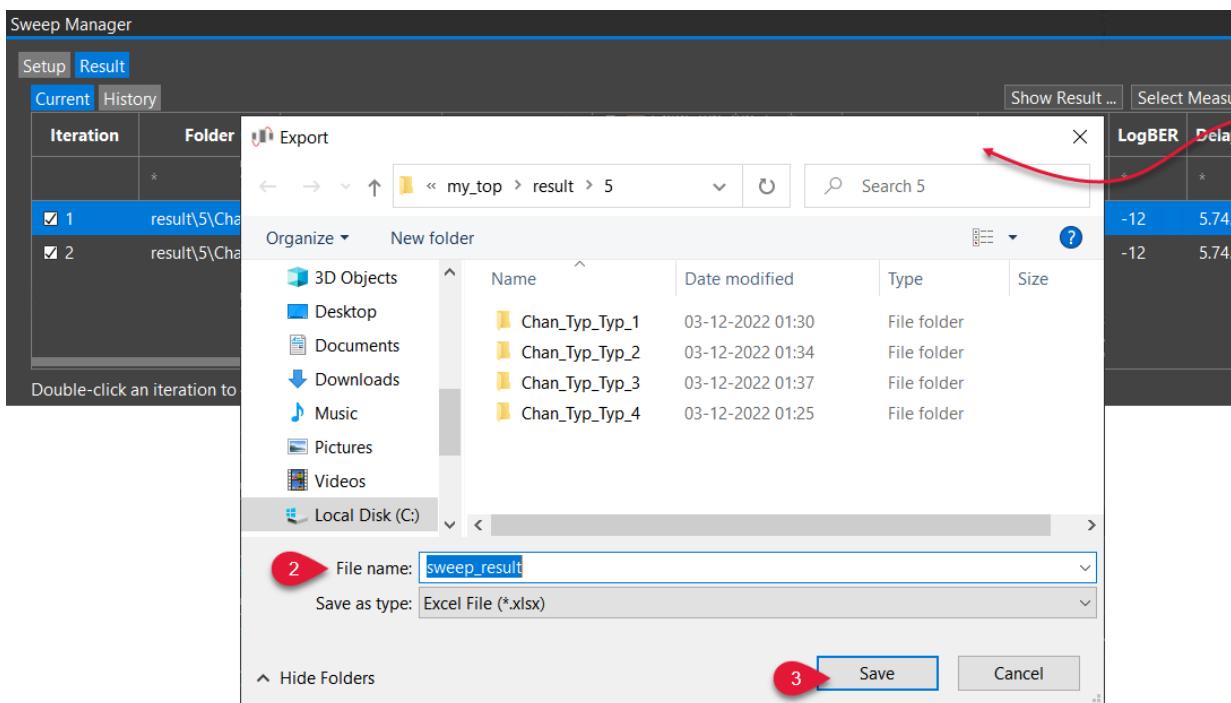
The *Current* and *History* sub-tabs in the *Result* tab have a button, *Export*, that lets you export the sweep simulation results to a Microsoft Excel file on Windows and a text file on Linux.

## Topology Workbench User Guide

### Using the Sweep Manager

For example, to export the sweep simulation results in Windows, perform the following steps:

1. Click *Export*. The *Export* dialog box opens with the current workspace selected by default.
2. Specify a *File name*. The default name for the file is *sweep\_result*.
3. Click *Save*.



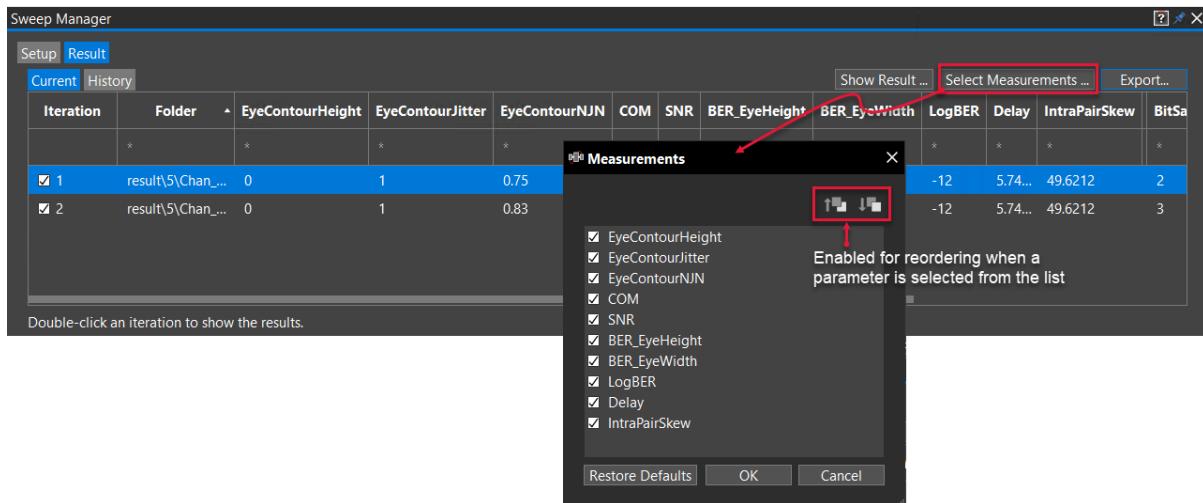
## Filtering the Sweep Simulation Results

To filter the parameters that should be displayed in the *Result* tab:

# Topology Workbench User Guide

## Using the Sweep Manager

1. Click *Select Measurements* on the *Result* tab in the *Sweep Manager* panel. The *Measurements* dialog box opens with a list of standard parameters. By default, all parameters are selected for display when you view the simulation results.



2. Deselect the check box adjacent to parameters that should not be displayed in the *Result* tab. You can select the check box again later, if needed.
3. Define the order in which the selected parameters should be displayed in the *Result* tab. For this, select the parameter that needs to be reordered and then click the activated up and down buttons as required.

For example, if you want to show *COM* as the first parameter and *EyeContourNJN* as the second, you can drag and drop the parameter names in the *Selected Parameters* list at the first and second spot as shown below.

4. Click *OK* to confirm the applied filters.

**Note:** Click *Restore Defaults* to undo the modifications done and restore the default settings.

The columns in the table displayed on the *Result – Current* tab adjust as per the applied changes as shown below.

Iteration	Folder	COM	EyeContourNJN	EyeContourHeight	SNR	EyeContourJitter	BER_EyeHeight	BER_EyeWidth	LogBER	Delay	IntraPairSkew	BitS
*	*	*	*	*	*	*	*	*	*	*	*	*
1	result\5\Chan...	0	0.75	0	1	1			-12	5.74...	49.6212	2
2	result\5\Chan...	0	0.83	0	1	1			-12	5.74...	49.6212	3

## Other Sweep Features

In addition to the features explained in the sections above, the *Sweep Manager* can group parameters and help select sweep models.

- [Grouping Sweep Parameters](#)
- [Defining SPICE Model Sweeps](#)

### Grouping Sweep Parameters

You can group two or more sweep parameters to reduce the number of iterations.

1. Select the rows that need to be grouped.
2. Right-click and choose *Group* from the shortcut menu.

The number of *Total Iterations* are accordingly recalculated and reduced.

For example, if originally, the iterations looked like following for *Data Rate* and *DCD* parameters:

Iteration	fwd	Data Rate (Gbps)	DCD (%)
1	2	5	0
2	3	5	0
3	2	8	0
4	3	8	0
5	2	5	1
6	3	5	1
7	2	8	1
8	3	8	1

After grouping the *Data Rate* and *DCD* parameters, the new iterations are:

Iteration	fwd	Data Rate (Gbps)	DCD (%)
1	2	5	0
2	3	5	0
3	2	8	1

## Topology Workbench User Guide

### Using the Sweep Manager

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4            3            8            1

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When combining two or more parameters in a group:

- The first value for each parameter in the group constitutes one combination.
- The second value for each parameter constitutes the second iteration.

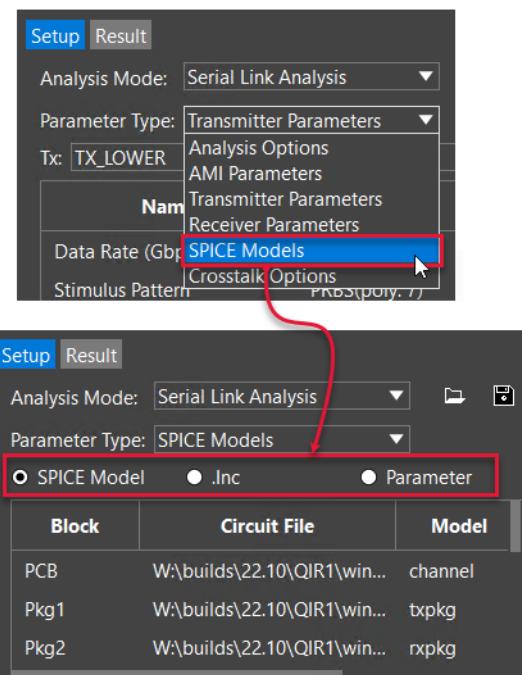


Within a group, the value in the *Step Count* column of each parameter must be identical; else, the *Total Iterations* of the group will be 0.

## Defining SPICE Model Sweeps

The *Sweep Manager* allows you to define the different types of SPICE models as described below.

1. Select *SPICE Models* from the *Parameter Type* list in the *Setup* tab.



2. Select one of the following options that are displayed:

- SPICE Model*

Lets you sweep multiple circuit files for a block. When this option is selected, all relevant block-wise circuit files are displayed in the table.

**Note:** Ensure that the MCP headers are common across the .sp files and that the connectivity inside each file is the same to maintain everything between \* [MCP Begin] and \* [MCP End].

For more information, see [Adding Iterations for a SPICE Model File](#).

*.Inc*

Lets you sweep multiple files that are included with a .include statement, such as seen in *conn1* and *conn2* blocks. When using *.Inc* sweep ensure that the sub-circuit name inside the specified .cir file or other circuit files all have the same name.

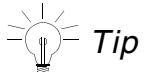
*Parameter*

Sweep the top-level parameters defined in a subcircuit, such as *c\_comp* for the *Tx1* block

## Adding Iterations for a SPICE Model File

The requirement for adding iterations for a SPICE model file arises when you set *Parameter Type* to *SPICE Models* and then select the *SPICE Model* option. Double-clicking the required rows from the tabular list of block-wise circuit files in leftmost table updates the *Parameter Table* section. However, to define a model file and then add iterations for it:

1. Click the new file button from the tool bar displayed above the *Sweep List* table. This opens the *Select Model* dialog box.



Alternatively, click *E* displayed in any of the cells for the *Sweep Element* for which the *Step Count* and *Total Iterations* need to be calculated.

2. Click the ... (*Browse*) button adjacent to the *File* field. It opens a dialog box to specify a SPICE model file.
3. Browse and select the required file using the dialog box.
4. Click *Open*. This closes the browse dialog box and refreshes the *File* field in the *Select Model* dialog box with the absolute path of the selected SPICE model file.
5. Click *OK* in the *Select Model* dialog box. This closes the dialog box and refreshes the *Sweep List* table. An additional row is added below the selected *Sweep Element* to display the absolute path of the associated SPICE model file. The calculated *Step Count* is also displayed.

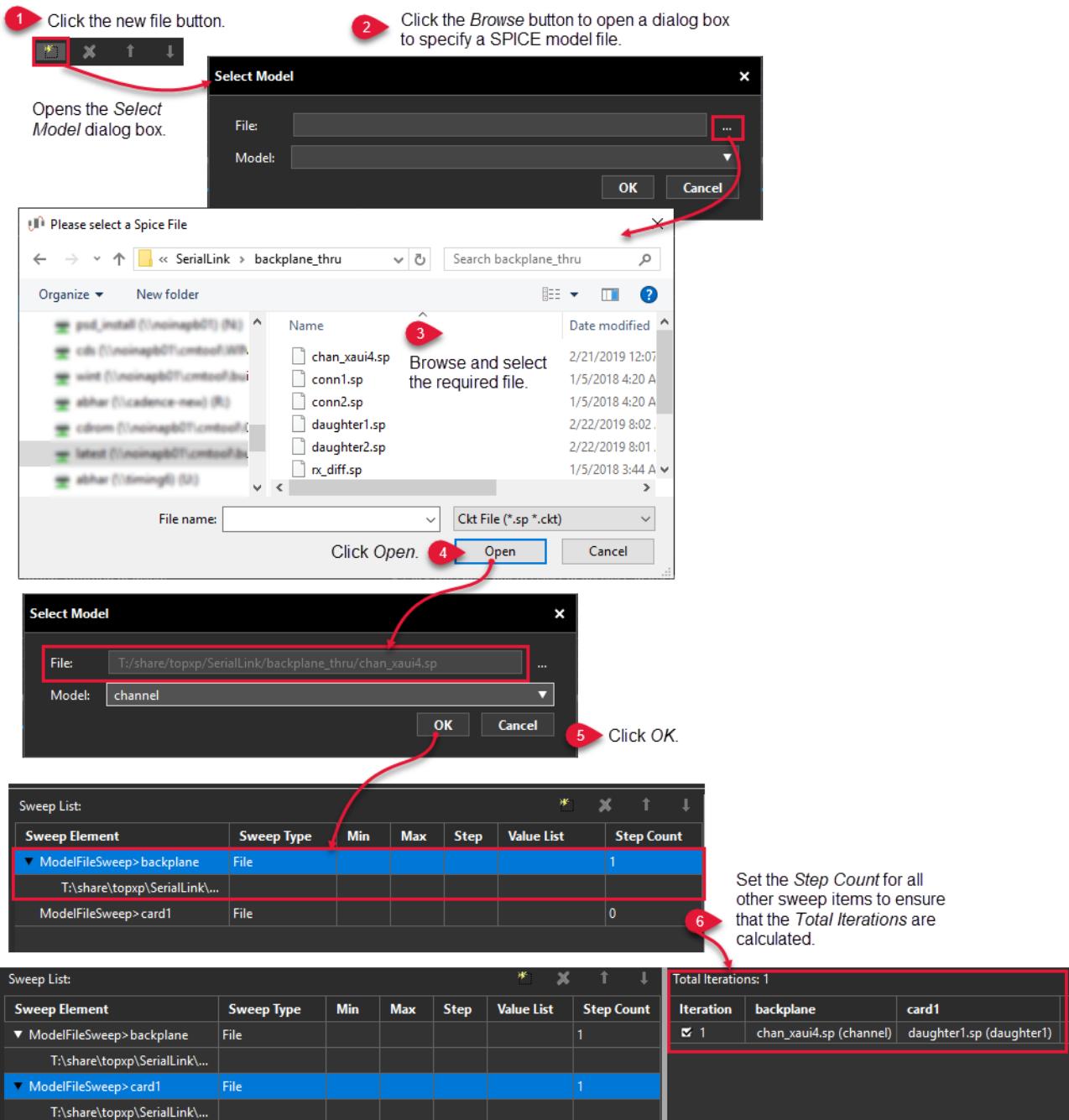
## Topology Workbench User Guide

### Using the Sweep Manager

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- 6.** Set the *Step Count* for all other sweep items. This is required to ensure that the *Total Iterations* are calculated and displayed in the rightmost table.

For an illustration of the steps given above, see the image below.



# **Topology Workbench User Guide**

## Using the Sweep Manager

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# Incorporating Crosstalk for Channel Analysis

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The crosstalk analysis feature is available in Serial Link Analysis workflow and in Parallel Bus Analysis when a channel simulator is used.

When multiple drivers and receivers are included in a topology, you can include crosstalk effects into Channel Analysis. With this type of multi-receiver topology, it is important that you identify the primary receiver.

Serial Link Analysis (SLA) and Parallel Bus Analysis (PBA) workflows support multiple crosstalk capabilities and provide corresponding analysis options to you. This appendix covers these options and facilitates you with information to select the desired approach for including crosstalk effects in your serial link and parallel bus analyses.

## **Related Topics**

- [Extraction-Based Crosstalk Topologies](#)
- [Selecting Crosstalk Stimuli](#)

## **Extraction-Based Crosstalk Topologies**

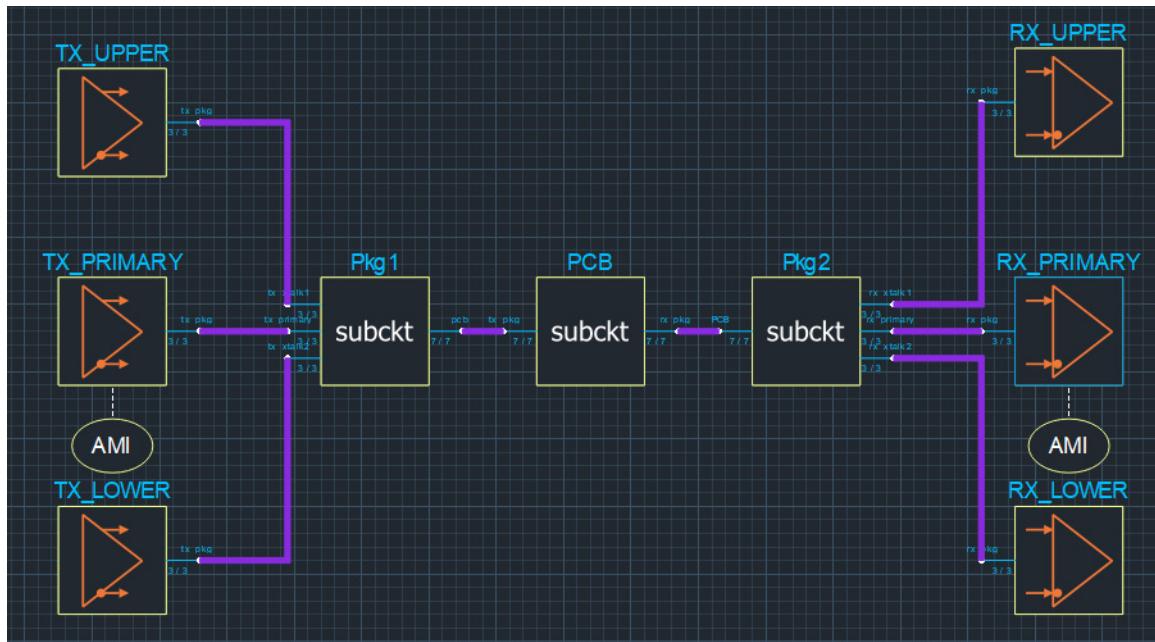
Extraction-based crosstalk topologies are built from interconnect circuits that are produced using extraction software, typically operating on a physical layout for a printed circuit board (PCB) or package. Extraction software, such as Sigrity PowerSI, allows you to place ports at the nodes of interest in the layout, and extract electrical circuits, generally in the form of S-Parameters or detailed SPICE subcircuits. There is usually no hard limit to the number of ports that can be defined for the extracted circuit. Therefore, it is straightforward to extract a

# Topology Workbench User Guide

## Incorporating Crosstalk for Channel Analysis

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*literal* circuit comprised of a through channel of interest coupled with a number of aggressor signals. An example of this kind of topology is shown below:



This design has three unique differential signals included in the topology, and three unique differential receivers; *RX\_UPPER*, *RX\_PRIMARY*, and *RX\_LOWER*. Here, the intended “through” channel of interest is *TX\_PRIMARY* > *RX\_PRIMARY*, while the other two differential pairs are intended as aggressor signals. These three differential pairs are coupled together on both, *Pkg1* and *Pkg2*, as well as in the *PCB* block. This represents the “literal” circuit as it exists in the package and PCB layouts.

You can specify the receiver of interest (primary receiver) for the purpose of channel analysis as following:

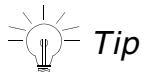
1. Choose *Check Connectivity* from the *Simulation Setup* schema in the Workflow panel. The *Connectivity Checker* panel opens.
2. Ensure that *Rx Signal* is set to *All*, or set it from the list.
3. Select a check box in the *Victim Rx* column to identify the corresponding *Rx Signal* as the primary receiver. There can be **only one** victim receiver (Rx).

Connectivity Checker							
Rx Signal:	All	Maximum Frequency:	1	GHz	# of Frequency Points:	10	Check
Rx Signal	Rx Pin	Connection	Tx Signal	Tx Pin	Frequency Response	Average Magnitude	Victim Rx
RX_LOWER::pos-neg	RX_LOWER::pos,neg				...		<input type="checkbox"/>
<b>RX_PRIMARY::pos-neg</b>	<b>RX_PRIMARY::pos,neg</b>				...		<b><input checked="" type="checkbox"/></b>
RX_UPPER::pos-neg	RX_UPPER::pos,neg				...		<input type="checkbox"/>

# Topology Workbench User Guide

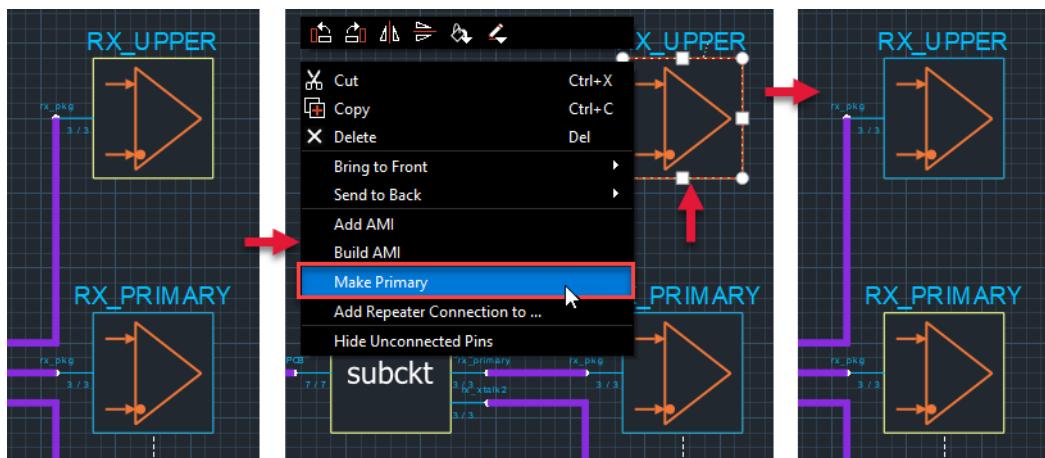
## Incorporating Crosstalk for Channel Analysis

The eye diagrams and other simulation results are generated for the receiver specified in this field.

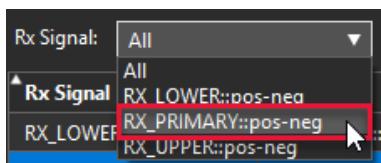


Alternatively, right-click the Rx block of interest and choose *Make Primary* from the displayed shortcut menu.

The boundary color of the primary receiver changes to blue as shown below.



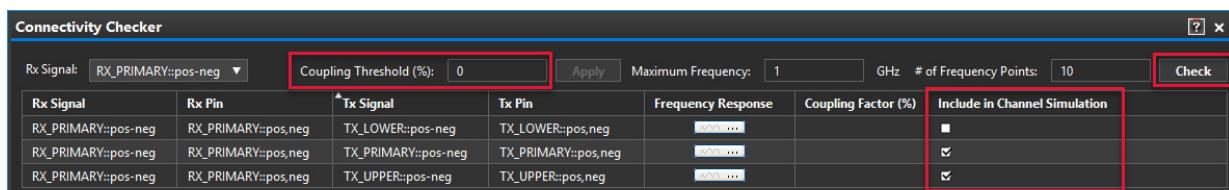
4. Select from the *Rx Signal* list the victim Rx chosen in step 3 as shown below.



The values corresponding to the selected Rx signal are displayed in the *Connectivity Checker* panel.

5. Specify the *Coupling Threshold* value, which is by default set to 0.

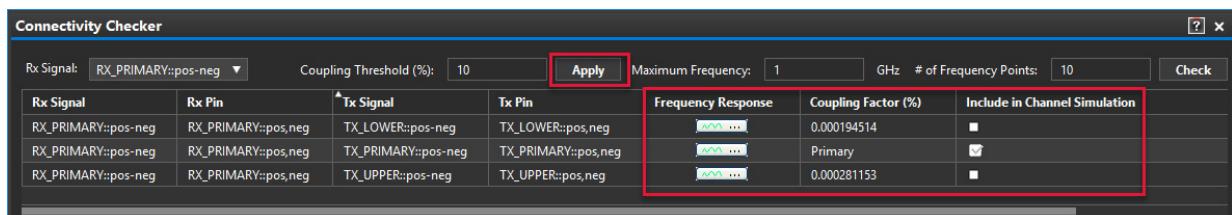
For a specified coupling threshold value, the tool automatically includes or excludes various aggressors in the channel simulation. This option is useful when you have multiple aggressors in your topology.



## 6. Click *Check*.

A fast frequency sweep analysis is performed from each transmitter to the selected primary receiver. Once the frequency sweep analysis is done, the *Coupling Factor (%)* column is populated with the coupling factor value for each transmitter. See also [Coupling Factor Calculation Formula](#) below.

Based on these values, the selections in the *Include in Channel Simulation* column can also get updated. If, for a transmitter, the value of the *Coupling Factor (%)* is smaller than the specified *Coupling Threshold* value, the check box in the *Include in Channel Simulation* column is not selected. If the coupling factor value is greater than the *Coupling Threshold* value, the corresponding check box is selected in the *Include in Channel Simulation* column.



## 7. Click *Apply*.

## 8. Click *Start Channel Simulation*.

When a channel analysis is run, a characterization or impulse response generation is run for each included transmitter to the primary receiver. For the topology shown earlier, three impulse responses are generated, all of which are combined together in the channel simulator to produce the combined waveforms at the primary receiver.

**Note:** To ignore the impact of an aggressor signal on channel simulation, in the *Include in Channel Simulation* column, clear the check box for the corresponding transmitter. If a particular Tx is not enabled or selected in the *Connectivity Checker* panel, it is completely ignored during simulation and its characterization is omitted from the command.txt file provided to the channel simulator (spdut).

## Coupling Factor Calculation Formula

The following formula is used for calculating the *Coupling Factor* values:

$$CF_k = \frac{P_k}{P_{max}}$$

$$P_k = \sqrt{\sum_{i=1}^N |V_{fi}|^2 / N}$$

$$P_{max} = \text{Max}(P_1, P_2, P_3, \dots, P_M)$$

$K = 1, 2, 3, \dots, M$

( $K^{\text{th}}$  transmitter connected to the receiver of interest)

$P_k$  is Average power delivered by  $K^{\text{th}}$  transmitter

$V_{fi}$  is Voltage at  $i^{\text{th}}$  frequency point;  $i = 1, 2, 3, \dots, N$

$N$  is total number of frequency points

For Primary Channels,  $CF_k = 1$  as  $P_k = P_{max}$

If a transmitter is not coupled with the receiver of interest,  $P_k$  is zero (0). Substituting this value in the *Coupling Factor* formula,  $CF_k$  is also calculated as zero (0).

## Selecting Crosstalk Stimuli

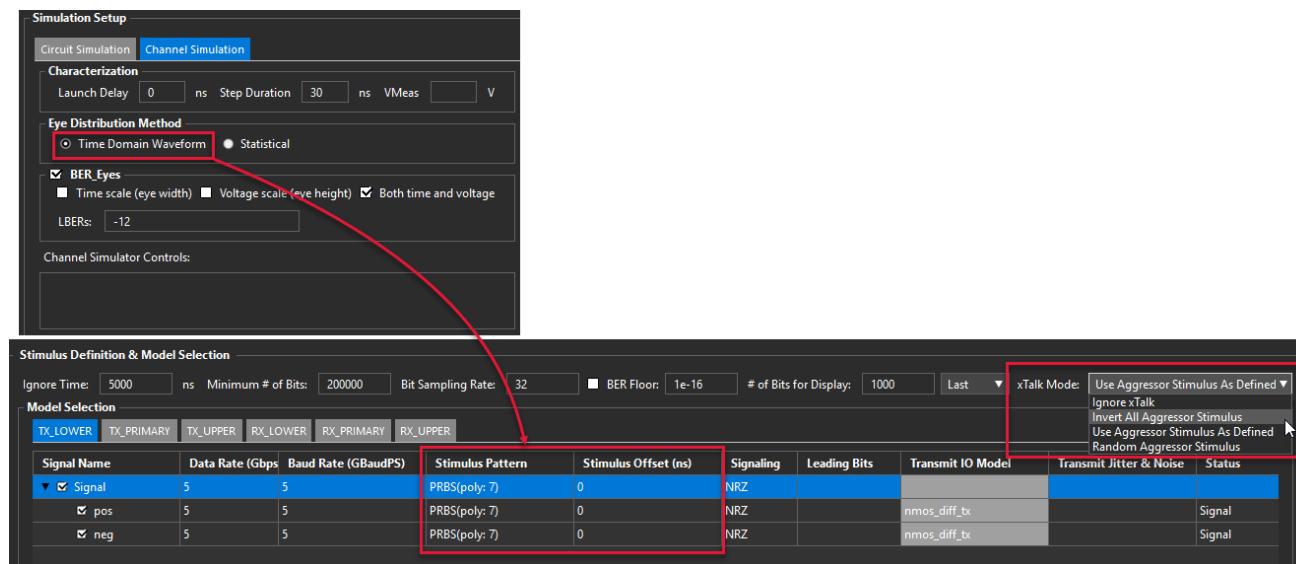
Once a coupled topology is built for Serial Link Analysis and the primary receiver has been identified, you have a number of choices as to how to handle the aggressor transmitters, which in turn provide you with significant flexibility as to the crosstalk analysis that can be performed. These choices are:

- Invert All Aggressor Stimulus
- Use Aggressor Stimulus As Defined
- Random Aggressor Stimulus
- Ignore xTalk

Of the four choices listed above, the first three choices relate to the time domain channel simulation of crosstalk.

## Setting a Stimulus for a Transmitter

When the time domain approach is opted for in the *Analysis Options* panel, each transmitter in a topology has its own unique stimulus settings that are defined in the *Stimulus Pattern* and *Stimulus Offset* columns.



## Xtalk Mode Settings

Before you run the crosstalk analysis, you need to set the *xTalk Mode* in the *Analysis Options* panel.

For the time domain channel analysis, you can selected one of the following options:

- Invert All Aggressor Stimulus

Selecting this option inverts the stimulus settings for the aggressor or crosstalk transmitters (that is, transmitters that are not connected directly to the primary receiver). This is meaningful when the identical stimulus has been set for all the transmitters in the topology, and the user wants the aggressors to have the opposite stimulus of the through channel.

- Use Aggressor Stimulus As Defined

When this option is selected, the stimulus on the crosstalk transmitters is left as it was defined, with no inversion.

- Random Aggressor Stimulus

This option is useful when the stimuli *Data Pattern* for the transmitters is set to PRBS or Random. This option ensures that a unique random seed is used for each transmitter.

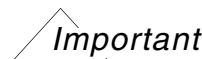
In a testbench with multiple Tx models, one pair of Tx and Rx is considered primary, while the others are defined as aggressors. The simulation of aggressor Tx models depends on the crosstalk setting. Suppose you chose *Ignore xTalk* from the *xTalk Mode* list box in the Analysis Options panel's *IO Models and Stimulus* tab. In that case, only the primary Tx model is simulated, and the crosstalk analysis is ignored. The waveform might show some voltage ripple caused by crosstalk from the primary Tx model onto the aggressor Tx models, but SystemSI ignores it. If other crosstalk options are selected from the *xTalk Mode* list box, each aggressor Tx model is simulated individually, and each waveform is recorded.

**Note:** Simulations of each Tx aggressor run one at a time, not simultaneously, resulting in multiple simulations when crosstalk is enabled. After simulating all the Tx aggressors, the primary Tx/Rx model is simulated, including the crosstalk from all aggressor Tx models, to provide the final eye at the primary Rx. The crosstalk options specify the type of data pattern for the aggressor Tx models.

**Topology Workbench User Guide**  
Incorporating Crosstalk for Channel Analysis

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# Setting Timing Parameters in Topology Workbench



Only Parallel Bus Analysis (PBA) workflow supports the timing parameter feature discussed in this appendix.

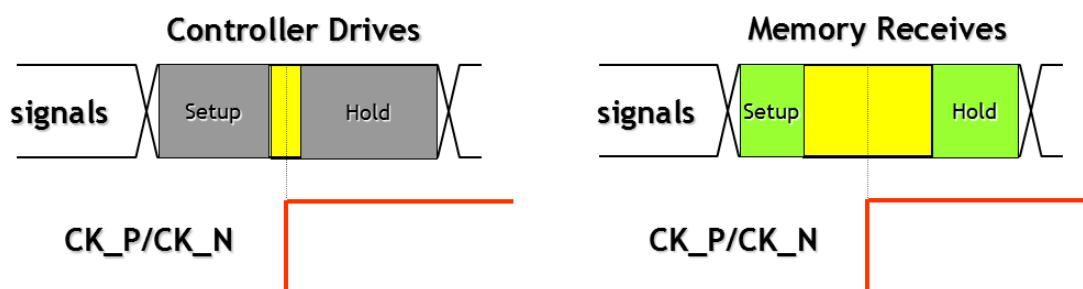
The [Setting Up Timing Specifications](#) section in [Chapter 7, “Using Parallel Bus Analysis Workflow”](#) explains the procedural information about how to set the timing parameters in the *Timing Budget* panel. The concepts covered in this appendix below familiarize you with the impact that these timing parameters have on different types of buses.

Timing affects the:

- Phase relationships at the transmitting component
- Phase requirements at the receiving component

The timing for memory is JEDEC-based and standardized; whereas, timing for controllers is more component specific.

## Setting AddCmd Timing Parameters



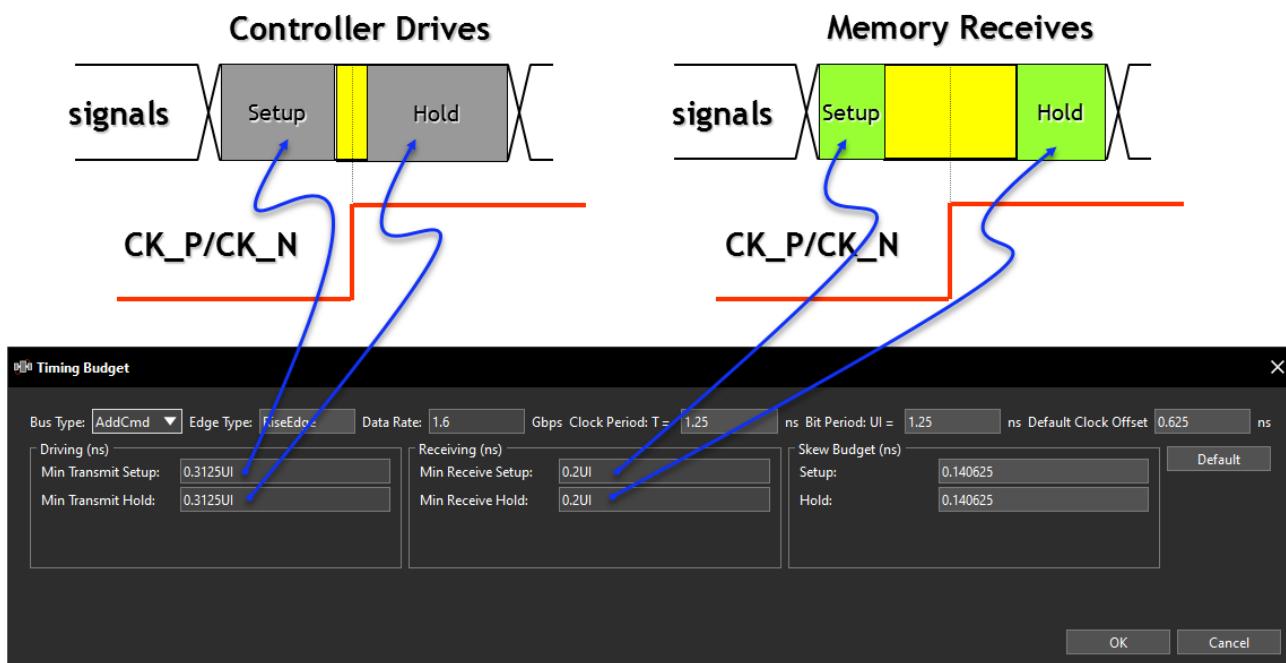
In this figure of AddCmd timing:

## Topology Workbench User Guide

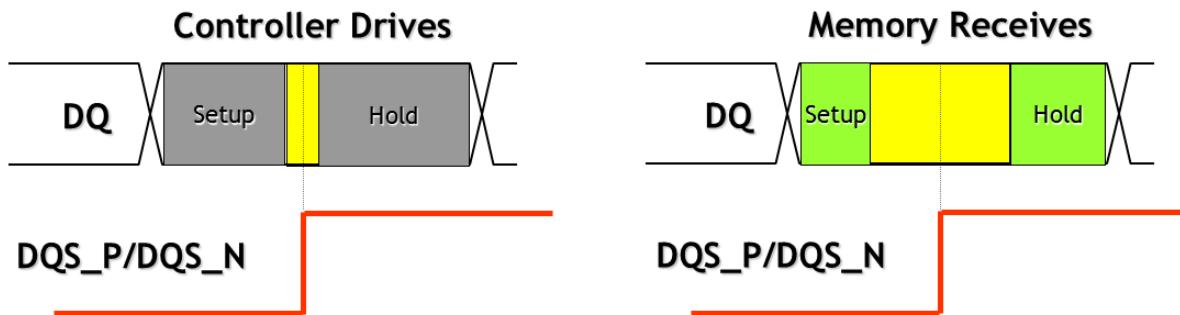
### Setting Timing Parameters in Topology Workbench

- AddCmd and Ctrl signals launched at t=0
- TimingRef is clock (CK)
- CK is launched about  $\frac{1}{2}$  clock period later to put rising edge in middle of eye diagram
- Setup and hold requirements must be met at receiver (memory)
- External termination is often used

The next figure shows you which UI elements correspond to which part of the timing.



## Setting Data (Write) Timing Parameters



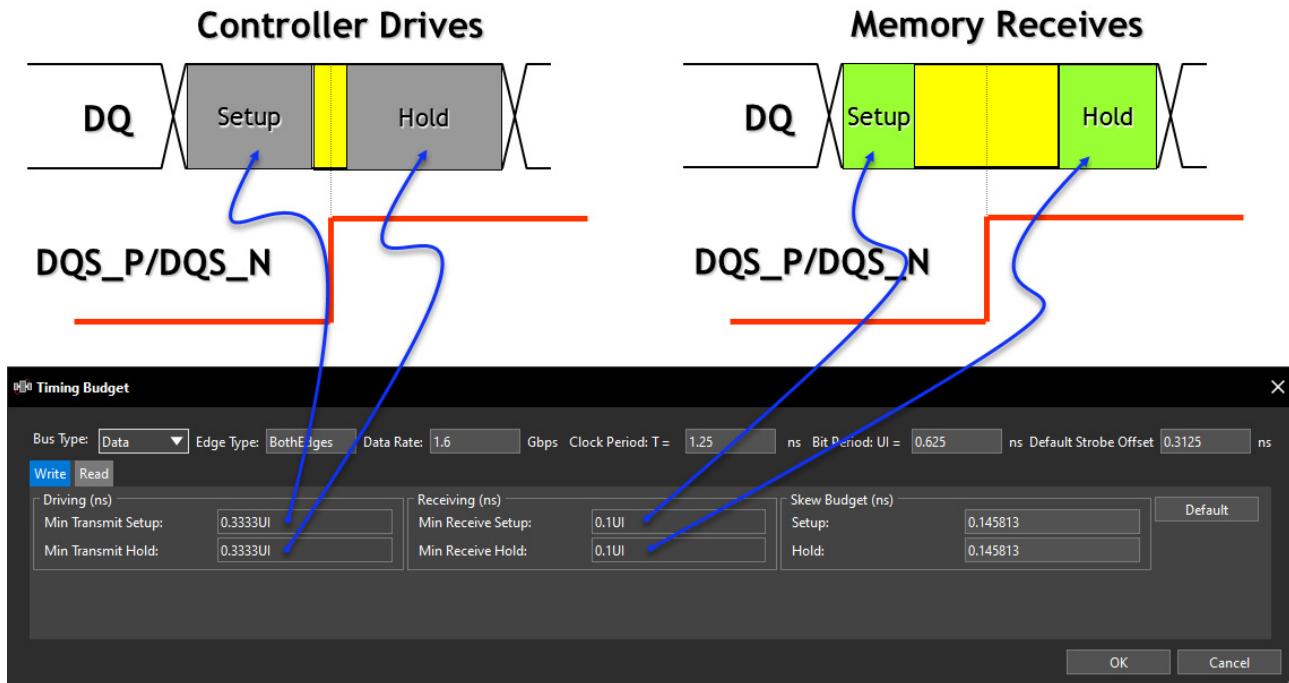
## Topology Workbench User Guide

### Setting Timing Parameters in Topology Workbench

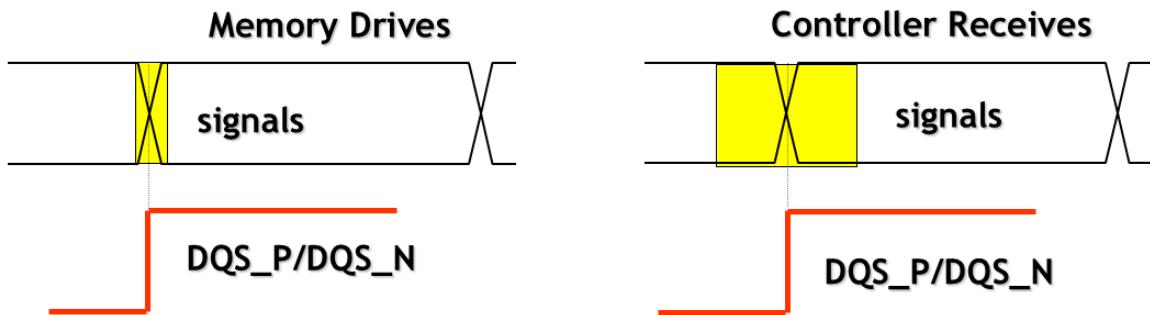
In this figure of Data (Write) timing:

- Data signals are launched at t=0
- Strobe is the TimingRef, unique to each byte of Data
- Strobe is launched about 1/4 clock period later to put rising and falling edges in middle of eye diagram
- Setup and hold requirements must be met at receiver (memory)
- On-die termination (ODT) is often used

The next figure shows you which UI elements correspond to this timing.



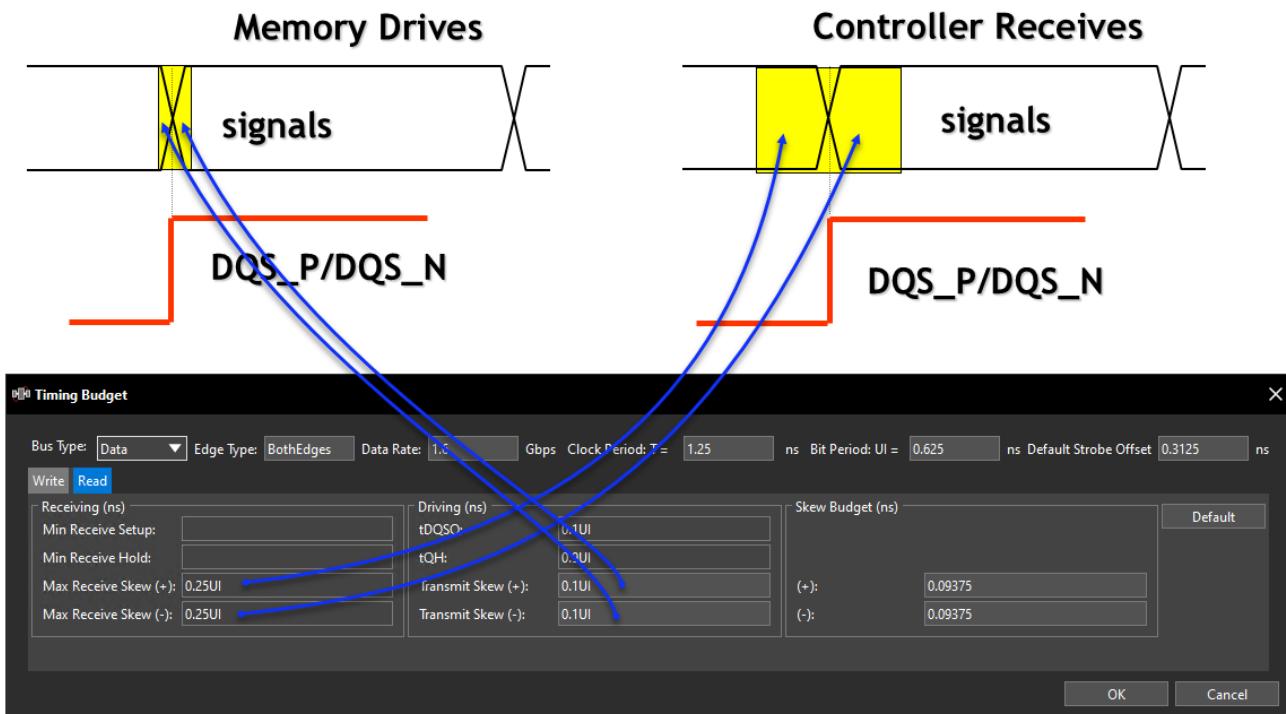
## Setting Data (Read) Timing Parameters



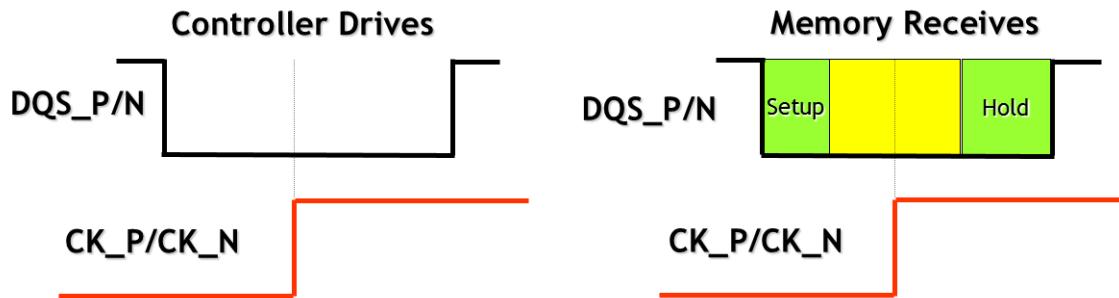
In this figure of Data (read) timing:

- Data and strobe signals are launched at  $t=0$ , essentially aligned
- Read Skew requirements must be met at receiver (controller)
- Quarter-cycle offset is added inside of Controller
- On-die termination (ODT) is often used

The next figure shows you which UI element corresponds to the timing.



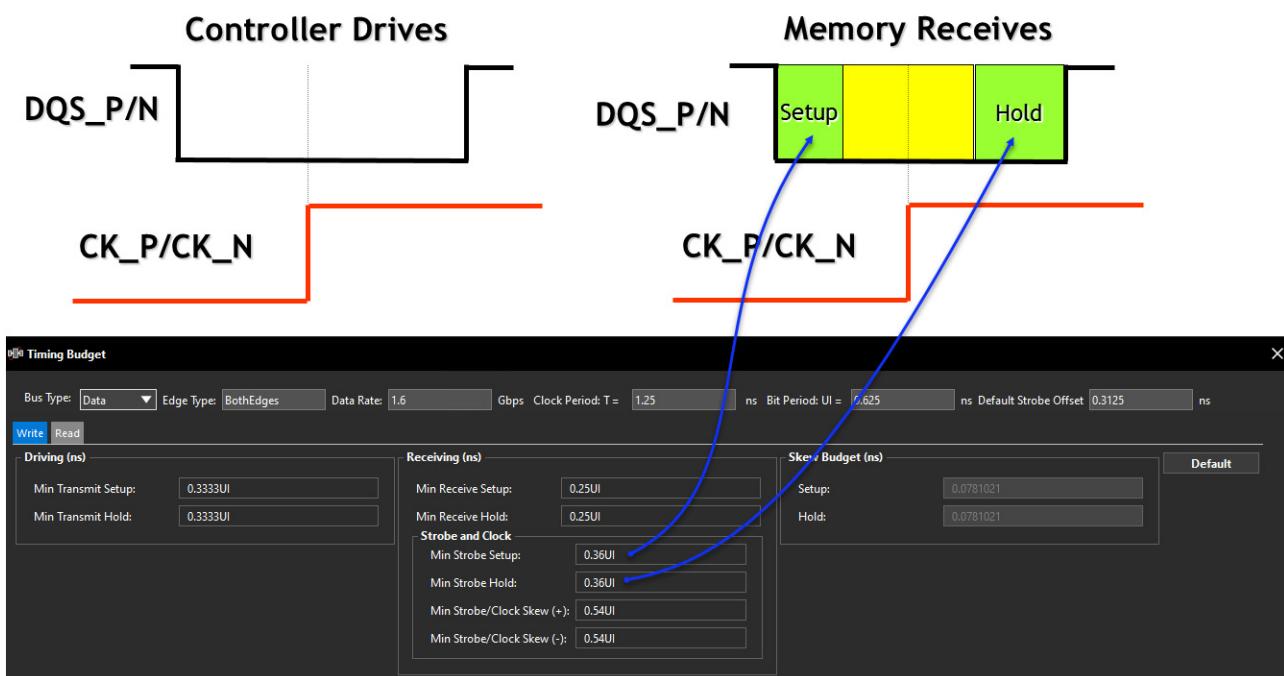
## Setting Strobe/Clock Timing Parameters



In this figure depicting the strobe/clock timing:

- Strobe is launched at  $t(0) + \frac{1}{4}$  clock period
- TimingRef is clock (CK)
- CK is launched at  $t(0) + \frac{1}{2}$  clock period
- Setup and hold requirements must be met at receiver (memory)

The following figure shows you which UI elements correspond to which part of the timing.



# **Topology Workbench User Guide**

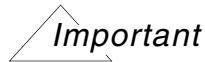
## Setting Timing Parameters in Topology Workbench

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# Reporting DDR Measurements

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Only the Parallel Bus Analysis (PBA) workflow supports the DDR measurement reports feature discussed in this appendix.

The PBA workflow supports extensive DDR data processing and compliance to specifications. The standard measurements and specifications from JEDEC standards are included, with user-friendly data presentation and parsing, for unprecedented troubleshooting, all combined with the implicit accuracy that comes with the unique simulation technology supported in Topology Workbench.

This appendix explores the DDR measurement reporting using examples.

## Preparing for DDR Measurement Reports

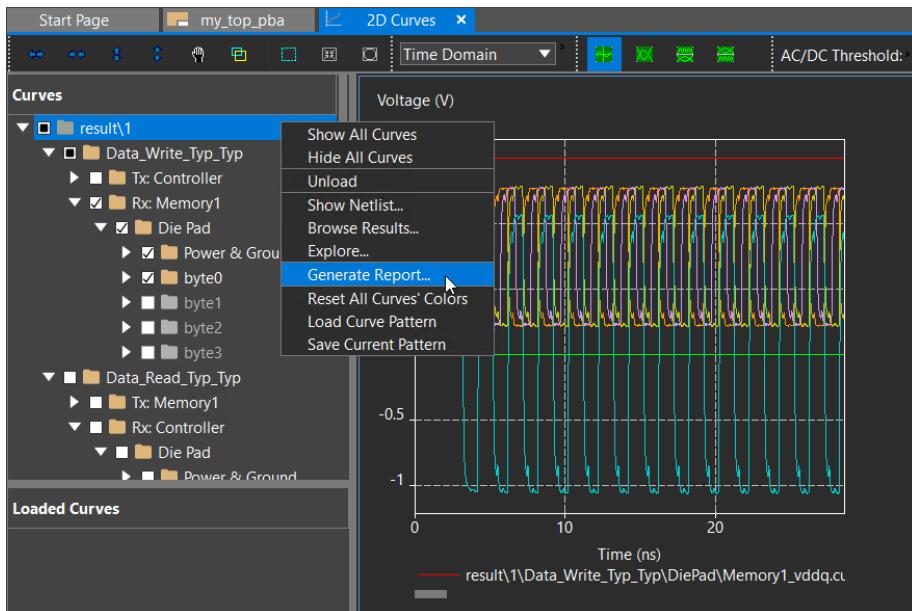
To start with DDR measurement reports,

1. Run the simulation for a topology in Topology Workbench. The simulation results open in the *2D Curve* tab.
2. Right-click a node in the hierarchy displayed in the *Curves* pane to display the shortcut menu. Depending on the node from where you choose to generate a report, the results shown in the report vary. For example:
  - When the topmost node that shows the path to simulation result directory is right-clicked, you can view the overall simulation results.
  - When a second-level node that indicates the type of simulation is right-clicked, you can view the results for that specific simulation type.

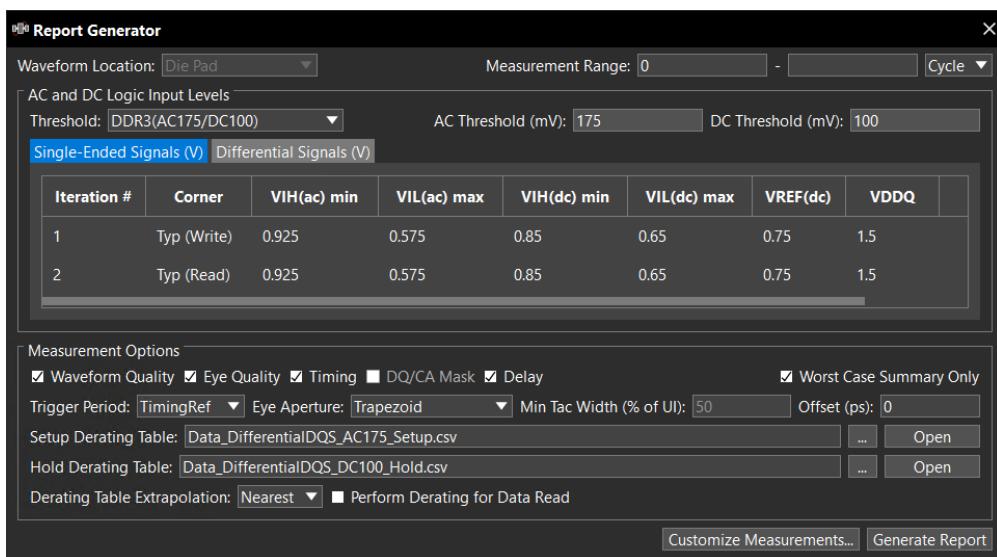
# Topology Workbench User Guide

## Reporting DDR Measurements

- When a third-level node that represents the simulated blocks is right-clicked, you can view the results for that specific block.



- Click *Generate Report* from the shortcut menu as shown above. The *Report Generator* dialog box opens.



## Topology Workbench User Guide

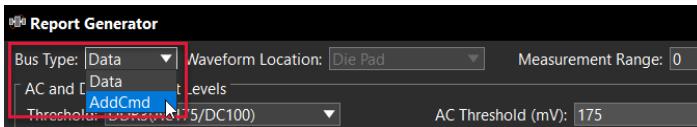
### Reporting DDR Measurements

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The *Report Generator* dialog box lets you set the following:

#### **Bus Type**

Select the bus type to generate the report.



**Note:** This list box is displayed only when the simulation was run for multiple bus types. The  $VREF(dc)$  and  $VDDQ(VDDA)$  values can be different for the different bus types.

#### **Waveform Location**

Displays whether the output waveform uses Die Pad or PKG Pin data.

#### **Measurement Range**

Specify the start and end measurement range, and choose the required unit of measurement from the list box. The following measurement units are supported: *ns* (nano seconds), *ps* (peco-seconds) and *Cycle*.

### ***Threshold***

Choose the *Threshold* from the list that includes JEDEC-specific AC and DC threshold levels for the following known standards:

- GDDR6(POD125, POD135)
- DDR5(4800-6400, 4400, 4000, 3600, 3200)
- DDR4(3200, 2933, 2666, 2400, 1600, 1866, 2133)
- DDR3(AC175/DC100, AC150/DC100, AC135/DC100, AC125/DC100)
- DDR2 (AC250/DC125, AC200/DC125)
- DDR1(AC310/DC150)
- LPDDR5(CK67-800MHz, WCK266-533MHz, WCK800-1600MHz, WCK1867-3200MHz)
- LPDDR4(4266, 3733, 3200, 2400, 2133, 1867, 1600)
- LPDDR4X-4266
- LPDDR3(AC150/DC100)
- LPDDR2(AC300/DC200, AC220/DC130)

**Note:** If you are running channel simulation in the PBA workflow, only DDR4, LPDDR4, and LPDDR4X threshold values can be selected.

If required, you can also use the *<User defined...>* option to add a custom threshold value. For related information, see [Adding a Custom Threshold Value](#).

## Topology Workbench User Guide

### Reporting DDR Measurements

#### **AC Threshold, DC Threshold, Single-Ended Signals, Differential Signals**

Selecting one of the predefined *Threshold* values updates the voltage values in the *Report Generator* dialog box. The voltage values include the *AC Threshold*, *DC Threshold*, and the single-ended typical corner values for low and high logic levels that are displayed in the *Single-Ended Signals* tab.

AC and DC Logic Input Levels								
Threshold:	DDR3(AC175/DC100)		AC Threshold (mV): 175		DC Threshold (mV): 100			
Single-Ended Signals (V) Differential Signals (V)								
Iteration #	Corner	VIH(ac) min	VIL(ac) max	VIH(dc) min	VIL(dc) max	VREF(dc)	VDDQ	
1	Typ (Write)	0.925	0.575	0.85	0.65	0.75	1.5	
2	Typ (Read)	0.925	0.575	0.85	0.65	0.75	1.5	

If required, you can modify the DC reference voltage value, *VREF(dc)*.

- To edit the default value, double-click the *VREF(dc)* value and enter the new value within the cell.

Single-Ended Signals (V) Differential Signals (V)								
Iteration #	Corner	VIH(ac) min	VIL(ac) max	VIH(dc) min	VIL(dc) max	VREF(dc)	VDDQ	
1	Typ (Write)	0.925	0.575	0.85	0.65	0.75	1.5	
2	Typ (Read)	0.925	0.575	0.85	0.65	0.75	1.5	

- To restore the default value, right-click and select *Default*.

Single-Ended Signals (V) Differential Signals (V)								
Iteration #	Corner	VIH(ac) min	VIL(ac) max	VIH(dc) min	VIL(dc) max	VREF(dc)	VDDQ	
1	Typ (Write)	1.075	0.725	1	0.8	0.9	1.5	
2	Typ (Read)	0.925	0.575	0.85	0.65	0.75	1.5	

The *Differential Signals* tab displays the differential corner values for the typical low and high logic levels.

### **Measurement Options**

Displays the following check boxes for selection: *Waveform Quality*, *Eye Quality*, *Timing*, *DQ/CA Mask*, *BER*, and *Delay*.

#### **Additional Points to Note**

- The *BER* measurement type is available only when the *Use Channel Simulator* check box is selected in the *Analysis Options* window.
- The *DQ/CA Mask* check box is enabled only when the following conditions are met; otherwise, it is unchecked and grayed out:
  - *Threshold* is set to *DDR4*, *DDR5*, *LPDDR4*, or *LPDDR4X*.
  - Simulation results have *Read* and *Write* data bus simulations.
- The *Eye Quality* and *Timing* check boxes are not available for channel analysis for *Write* data bus simulations.
- When *DDR4*, *DDR5*, *LPDDR4*, or *LPDDR4X* is selected from the *Threshold* list, the following measurement options are enabled by default: *Waveform Quality*, *Eye Quality*, *Timing*, *DQ/CA Mask*, and *Delay*. However, the following rules of mutual exclusivity define the availability of these check boxes for selection:
  - When the *Waveform Quality* and/or *Delay* check boxes are clicked, the *Eye Quality*, *Timing*, and *DQ/CA Mask* check boxes remain enabled.  

  - When the *DQ/CA Mask* check box is clicked, the *Eye Quality* and *Timing* check boxes are disabled.  

  - When the *Eye Quality* and/or *Timing* check boxes are clicked, the *DQ/CA Mask* check box is disabled.  


### **Trigger Period**

You can choose to specify the *Trigger Period* as *TimingRef* or *Same As UI*.

**Note:** This list box is enabled when the *Eye Quality* check box is selected.

### ***Eye Aperture***

Enables *ApertureWidth* measurement using one of the following methods:

- *Trapezoid* — Selected by default
- *Tac/Tdc Rectangles* — If selected, eye mask consists of two rectangular shapes:
  - *Tac*: Height of  $2 \times \text{VIH}(\text{ac})$  (from  $\text{VIL}(\text{ac})$  to  $\text{VIH}(\text{ac})$ ), with a width of  $\text{Tac}$ .
  - *Tdc*: The second rectangle is from  $(\text{VIL}(\text{dc})$  to  $\text{VIH}(\text{dc})$ ) and with width of  $\text{Tdc}$ .

The overall eye aperture width measurement is  $\text{Tac} + \text{Tdc}$ .

**Note:** This list box is enabled when the *Eye Quality* check box is selected.

### ***Min Tac Width***

Specify a positive number ranging from 0 to 100. The default is 50.

Like *Eye Aperture*, you can use *Min Tac Width* for *ApertureWidth* measurement. If the *Eye Aperture* is set to *Trapezoid*, the *Min Tac Width* field is disabled and the default value is used. It is enabled when you select *Tac/Tdc Rectangles* for *Eye Aperture*.

- If the ringback occurs after the *Tac* time point that is higher than *ViHDC*, it does not impact the eye-width measurement. Therefore, it is not a failure.
- If the ringback occurs within the *Tac* time point that can impact the receiver's switching, the first rectangle can be excluded from the eye-width measurement.

### ***Offset***

Specify the required offset value. By default, this field is set to 0.

### ***Setup Derating Table, Hold Derating Table, Derating Table Extrapolation***

These parameters are enabled when the *Timing* measurement option is selected.

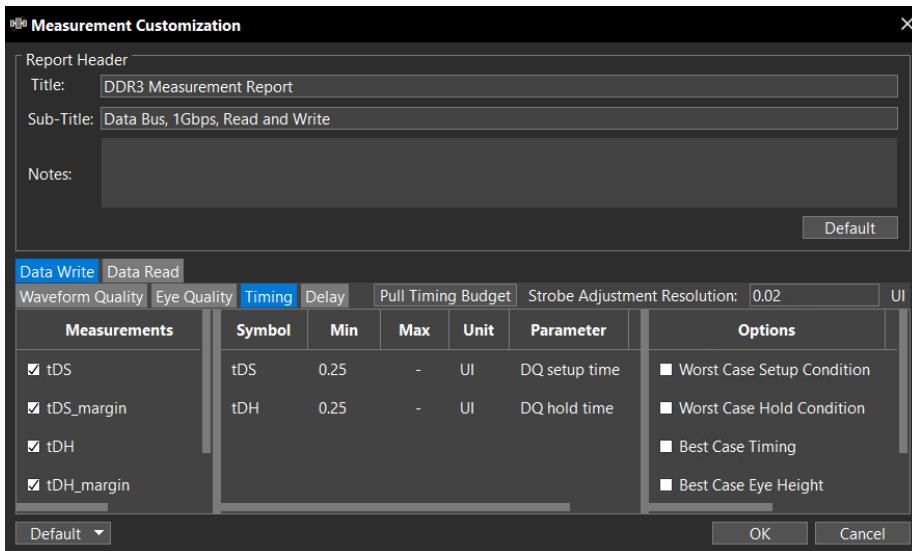
- Use the *Setup Derating Table* and *Hold Derating Table* fields to specify a derating table. When you click the corresponding ... button, multiple standard derating tables from public-domain sources are listed for selection.
- When Setup and Hold Derating Tables are specified, the *Derating Table Extrapolation* list is enabled to choose between *None* and *Nearest*.
- Select the *Perform Derating for Data Read* check box to perform derating for the *Read* data bus operations.

## Topology Workbench User Guide

### Reporting DDR Measurements

#### **Customize Measurements**

Click this button to open the *Measurement Customization* dialog box where you can customize the report header and specifications for the selected *Measurement Options*.



- The *Title* and *Sub-Title* in the HTML Header of the report can be changed as needed. The entries you add to the *Notes* field are appended to the report header.
- The *Data Write* and *Data Read* tabs are displayed based on the simulation directions you selected in the *Bus Simulation* tab of the Analysis Options panel.
- Under the simulation direction-specific tabs, sub-tabs are displayed for the *Measurement Options* you selected in the Report Generator dialog box. These sub-tabs contain the parameters for more granular customizations. A *Common* tab might be displayed for common parameters.

For example, if you selected the *Timing* measurement option in the *Report Generator* dialog box, the *Timing* tab is displayed in the *Measurement Customization* dialog box. On this tab, the *Pull Timing Budget* button is displayed to provide an option to use the *Timing Specifications* set for the simulation in the *Timing Budget* panel. In addition, you have the *Strobe Adjustment Resolution* field to specify a value that can be used for post-processing of *Data Bus* simulation results.
- To restore the default values, click the *Default* button. All customization are reversed.

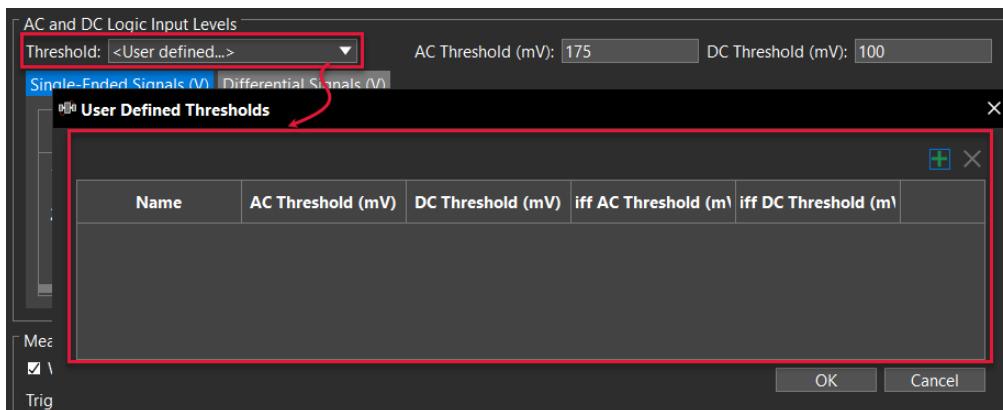
# Topology Workbench User Guide

## Reporting DDR Measurements

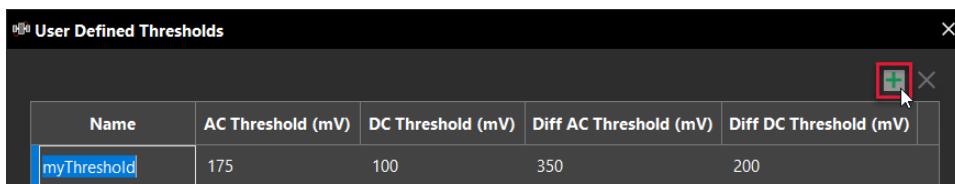
### Adding a Custom Threshold Value

To add a custom threshold value:

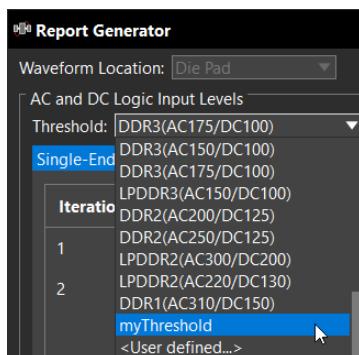
1. Select <User Defined...> from the *Threshold* list. The User Defined Threshold dialog box is displayed.



2. Click the + button given top-right corner of the table. A new row is added to the table where default values are populated under the *Name*, *AC Threshold (mV)*, *DC Threshold (mV)*, *Diff AC Threshold (mV)*, and *Diff DC Threshold (mV)* columns.



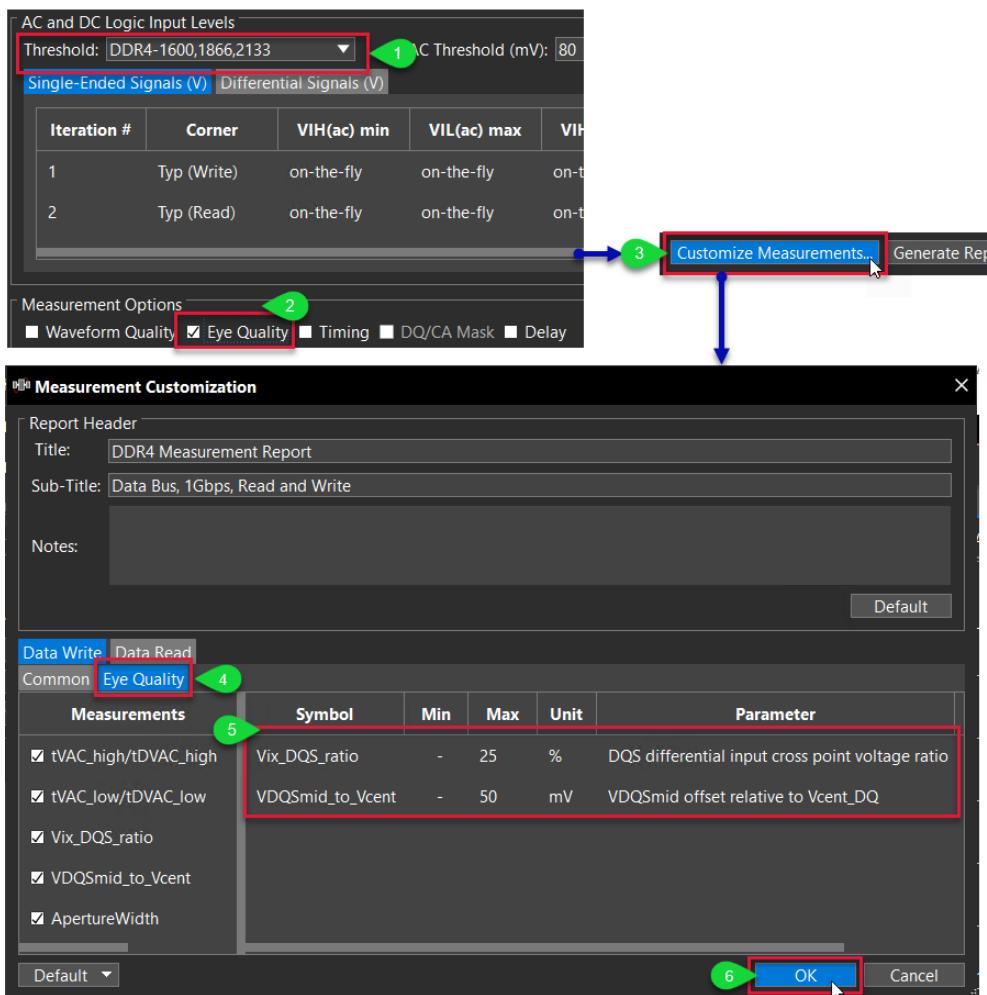
3. Edit the threshold values.
4. Click *OK* to save the definitions and close the User Defined Threshold dialog box. The *Threshold* list box in the *Report Generator* dialog box displays the name of the newly defined threshold.



## Calculating DQS Differential Input Voltage Values

To calculate DQS differential input voltage values, *Vix\_DQS\_Ratio* and *VDQSmid\_to\_Vcent*, as per the corresponding JEDEC standard:

1. Select a *DDR4* threshold from the *Threshold* list.
2. Select the *Eye Quality* check box.
3. Click the *Customize Measurements* button to display the corresponding dialog box.



4. Click the *Eye Quality* tab to view both the DQS differential input voltage
5. Edit the *Max* value as needed.
6. Click *OK*.

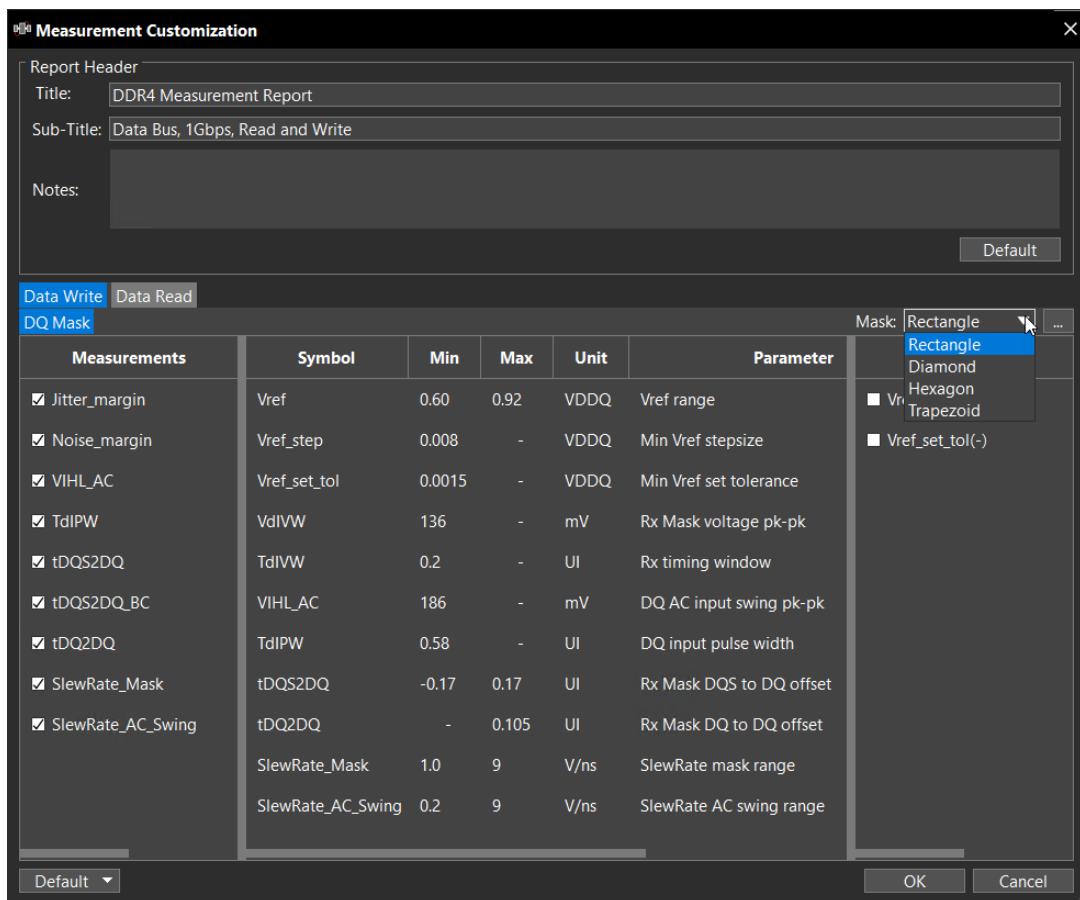
# Topology Workbench User Guide

## Reporting DDR Measurements

### Defining Custom Eye Mask for the DQ/CA Measurement Option

To perform PBA measurements on the interfaces of LPDDR4X, LPDDR4(Class-1), DDR5, and DDR4 at standard required data rates, you can define and select various eye masks in the shapes of rectangle, diamond, hexagon, and trapezoid.

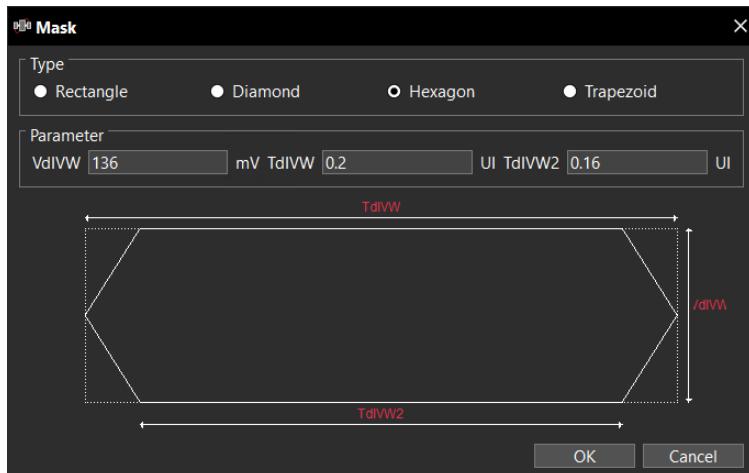
1. Select a *Threshold* from one of the following types of standards: DDR4, DDR5, LPDDR4(Class-1), or LPDDR4X.
2. Select the *DQ/CA Mask* check box from the *Measurement Options* section.
3. Click the *Customize Measurements* button to display the corresponding dialog box.



## Topology Workbench User Guide

### Reporting DDR Measurements

4. Select a *Mask* from the list and click the button with ellipsis (...). The *Mask* dialog box opens.



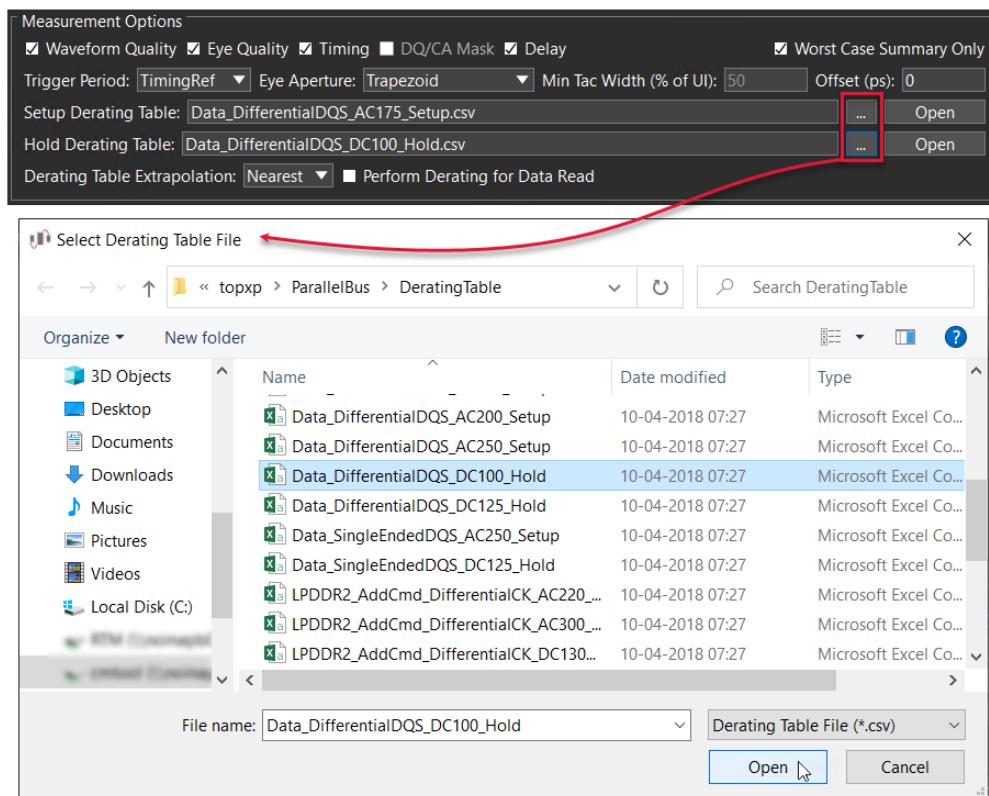
5. Change the mask *Type*, if required. The *Parameter* values and the diagrammatic representation change accordingly.
6. Edit the parameter values.
7. Click *OK*. The specified parameter values are updated in the *Min* column displayed on the *DQ Mask* tab.

## Setup and Hold Derating Tables

Topology Workbench includes standard derating tables from JEDEC for DDR2 and DDR3. These are delivered in CSV text format, and you can create custom tables too.

**Note:** The options to select a derating table are enabled when the *Timing* check box is selected.

When you click the ... (browse) buttons adjacent to the *Setup Derating Table* and *Hold Derating Table* fields, the *Select Derating Table File* dialog box opens to choose from the default derating table options given in the Topology Workbench installation.



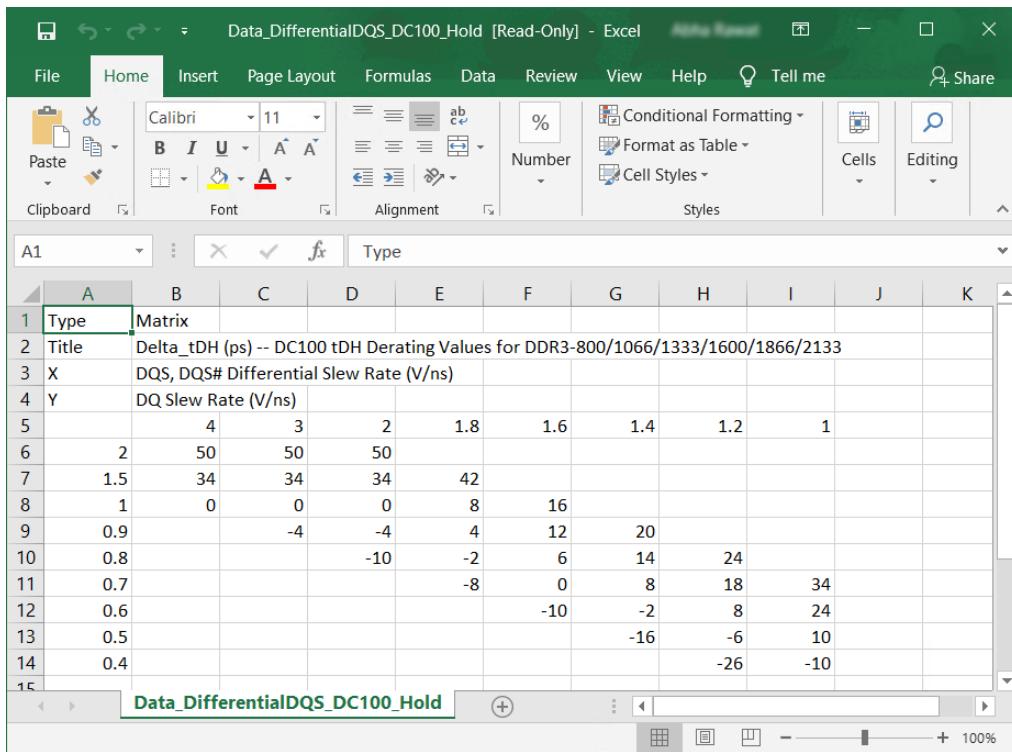
By default, the derating tables can be found in the installation directory at the following path:

<INSTALL\_DIR>\share\topxp\ParallelBus\DeratingTable

## Topology Workbench User Guide

### Reporting DDR Measurements

The derating table contains setup or hold scaling constants for specified slew rates. These tables are obtained from JEDEC for DDR2 and DDR3, and other public-domain sources, including device manufacturers. A typical derating table is shown below.



A screenshot of a Microsoft Excel spreadsheet titled "Data\_DifferentialDQS\_DC100\_Hold [Read-Only]". The spreadsheet contains a table with the following data:

Matrix										
1	Type	Delta_tDH (ps) -- DC100 tDH Derating Values for DDR3-800/1066/1333/1600/1866/2133								
2	Title	X DQS, DQS# Differential Slew Rate (V/ns)								
3	Y	DQ Slew Rate (V/ns)								
5		4	3	2	1.8	1.6	1.4	1.2	1	
6	2	50	50	50						
7	1.5	34	34	34	42					
8	1	0	0	0	8	16				
9	0.9		-4	-4	4	12	20			
10	0.8			-10	-2	6	14	24		
11	0.7				-8	0	8	18	34	
12	0.6					-10	-2	8	24	
13	0.5						-16	-6	10	
14	0.4							-26	-10	

## DDR<sub>x</sub> Threshold Application

The PBA workflow supports one threshold for DDR1, two for DDR2, and three thresholds for DDR3. Besides these, two thresholds for LPDDR2, and one for LPDDR3 are also supported.

If *LPDDR2(AC300/DC200)*, *LPDDR2(AC220/DC130)*, or *LPDDR3(AC150/DC100)* is selected, the AC and DC logic input levels for the Differential Signals is determined by the following formulas:

$$\begin{aligned}VIH_{diff}(ac) \min &= 2 * (VIH(ac) \ min - VIL(ac) \ max) \\VIL_{diff}(ac) \ max &= 2 * (VIL(ac) \ max - VIH(ac) \ min) \\VIH_{diff}(dc) \ min &= 2 * (VIH(dc) \ min - VREF(dc)) \\VIL_{diff}(dc) \ max &= 2 * (VIL(dc) \ min - VREF(dc))\end{aligned}$$

Otherwise, they are determined by the following:

$$\begin{aligned}VIH_{diff}(ac) \ min &= 2 * (VIH(ac) \ min - VIL(ac) \ max) \\VIL_{diff}(ac) \ max &= 2 * (VIL(ac) \ max - VIH(ac) \ min) \\VIH_{diff}(dc) \ min &= 0.2\end{aligned}$$

```
VILdiff(dc) max == 0.2
```

If the *TimingRef* is differential, the default derating table files are automatically loaded for LPDDR2 and LPDDR3 Setup derating and Hold derating.

## DDR4 Threshold Application

The PBA workflow supports one threshold for DDR4 interface, the *DDR4(AC100/DC75)*.

When *DDR4(AC100/DC75)* is selected, the AC and DC Logic Input Level for the Differential signals are determined using following equations.

```
VIHdiff(ac)min = 2 * (VIH(ac)min - VIL(ac)max)
```

```
VILdiff(ac)max = 2 * (VIL(ac)max - VIH(ac)min)
```

```
VIHdiff(dc)min = 0.15
```

```
VILdiff(dc)max = - 0.15
```

## LPDDR4 Threshold Application

If LPDDR4 threshold is selected, default VREF is on-the-fly. The AC and DC Logic Input Level are determined by the following equations.

### ***For the Single-Ended signals:***

```
VIH(ac) min = 0.5*VdIVM + VREF
```

```
VIL(ac) max = -0.5*VdIVM + VREF
```

```
VIH(dc) min = 0.5*VdIVM + VREF
```

```
VIL(dc) min = -0.5*VdIVM + VREF
```

If VREF is set to on-the-fly, it is calculated as:

```
VREF = Vcent_DQ (or Vcent_CA for Ctrl and AddCmd bus)
```

### ***For the Differential signals:***

```
VIHdiff(ac) min = VIH(ac) min - VIL(ac) max
```

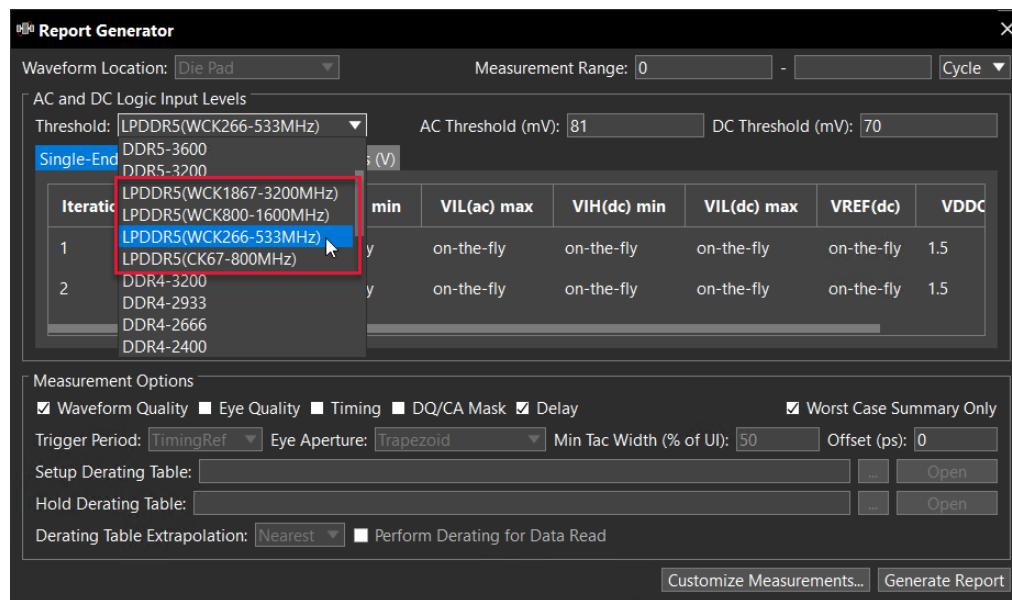
```
VILdiff(ac) max = VIL(ac) max - VIH(ac) min
```

```
VIHdiff(dc) min = VIH(dc) min - VIL(dc) max
```

```
VILdiff(dc) max = VIL(dc) max - VIH(dc) min
```

## LPDDR5 Threshold

JEDEC standard for fifth-generation Low Power Double Data Rate (LPDDR5) technology is supported by adding LPDDR5 interfaces to the postprocessing of measurements. The following LPDDR5 thresholds are available for choice: LPDDR5(CK67-800MHz), LPDDR5(WCK266-533MHz), LPDDR5(WCK800-1600MHz), and LPDDR5(WCK1867-3200MHz).



For eye budget, LPDDR5 requires hexagonal mask by default when *DQ/CA Mask* is selected. When *Eye Quality* is selected, LPDDR5 is measured by *Eye Aperture* instead of mask.

## Topology Workbench User Guide

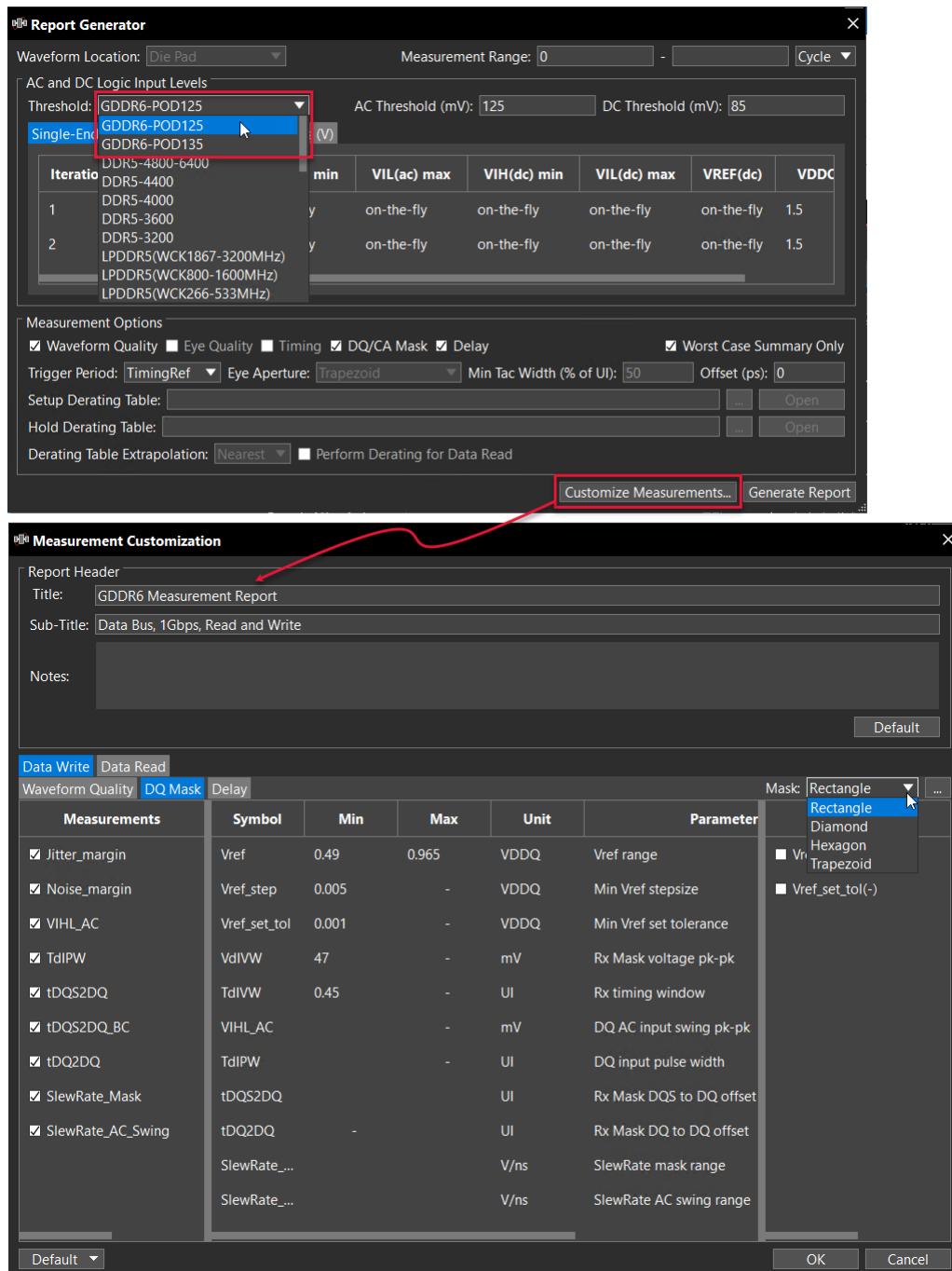
### Reporting DDR Measurements

When you customize the report for LPDDR5 threshold with *DQ/CA Mask* selected, the following customizations can be done:

Measurements	Symbol	Min	Max	Unit	Parameter	Mask	Options
<input checked="" type="checkbox"/> Jitter_margin	Vref	75	350	mV	Vref range	<input type="checkbox"/> Vref_set_tol(+)	
<input checked="" type="checkbox"/> Noise_margin	Vref_step	0.005	-	VDDQ	Min Vref stepsize	<input type="checkbox"/> Vref_set_tol(-)	
<input checked="" type="checkbox"/> VIHL_AC	Vref_set_tol	0.001	-	VDDQ	Min Vref set tolerance		
<input checked="" type="checkbox"/> TdIPW	VdIVW	140	-	mV	Rx Mask voltage pk-pk		
<input checked="" type="checkbox"/> TdIHL	TdIVW	0.35	-	UI	Rx timing window		
<input checked="" type="checkbox"/> tDQS2DQ	TdIVW2	0.18	-	UI	Rx Mask parameter		
<input checked="" type="checkbox"/> tDQS2DQ_BC	VIHL_AC	140	-	mV	DQ AC input swing pk-pk		
<input checked="" type="checkbox"/> tDQ2DQ	TdIPW	0.45	-	UI	DQ input pulse width		
<input checked="" type="checkbox"/> SlewRate_Mask	TdIHL	0.25	-	UI	DQ input pulse width above/below vDIVW		
<input checked="" type="checkbox"/> SlewRate_AC_Swing	tWCK2DQ	300	700	ps	Rx Mask WCK to DQ offset		
	tDQ2DQ	-	30	ps	Rx Mask DQ to DQ offset		
	SlewRate_Mask	1	7	V/ns	SlewRate mask range		
	SlewRate_AC_Swing	0.2	9	V/ns	SlewRate AC swing range		

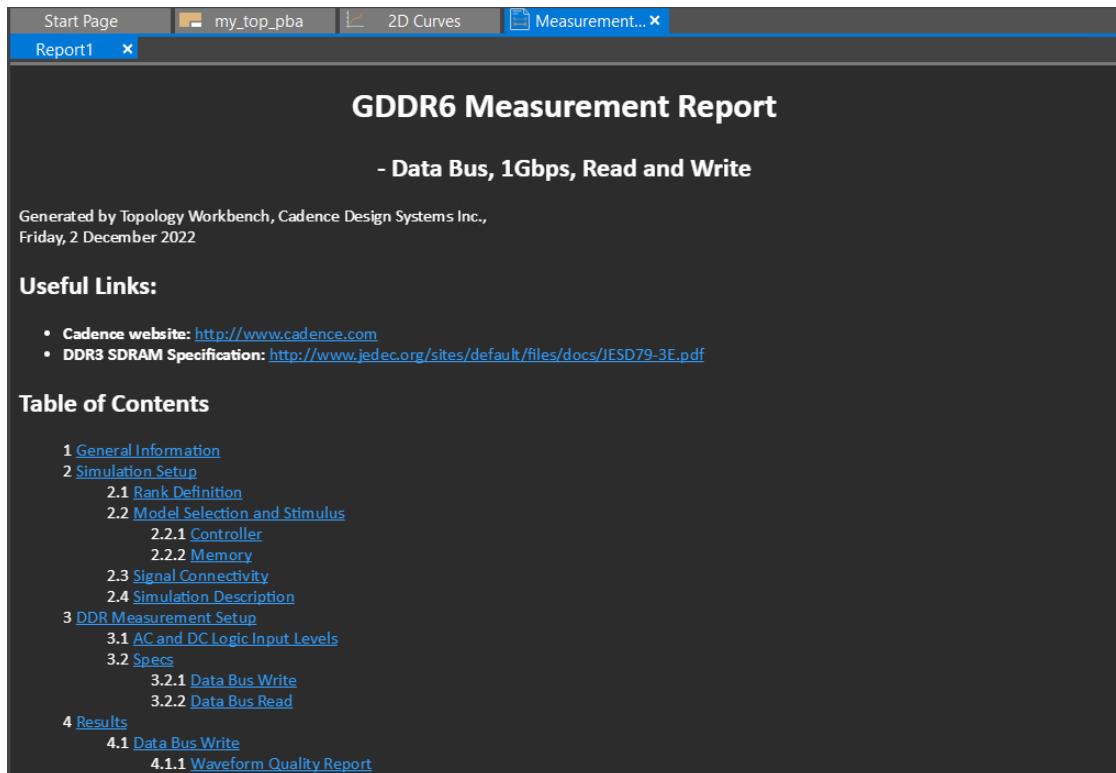
## GDDR6 Threshold

Automated JEDEC-based post-processing is supported in SystemSI for GDDR6 interfaces. The following GDDR6 thresholds are available for choice: GDDR6-POD125 and GDDR6-POD135.



## Generating the Report

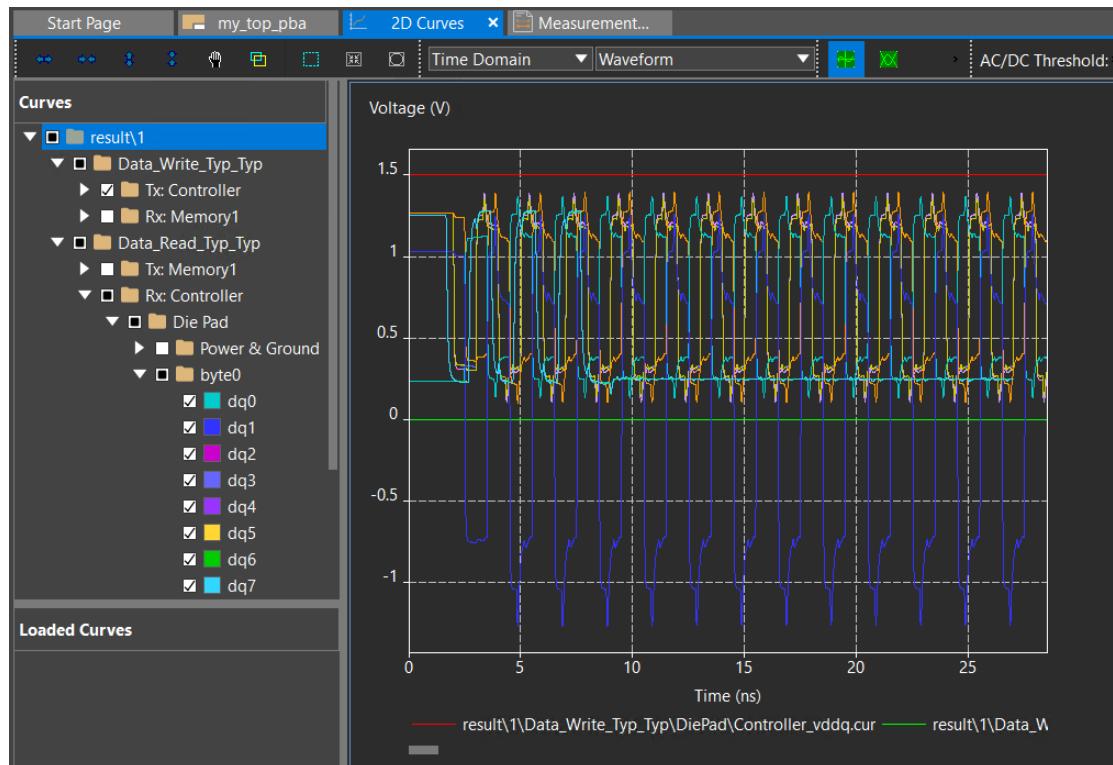
After specifying details of the DDR post-processing, click the *Generate Report* button in the Report Generator dialog box. The generator returns the report document in the *Measurement Report* tab.



## Topology Workbench User Guide

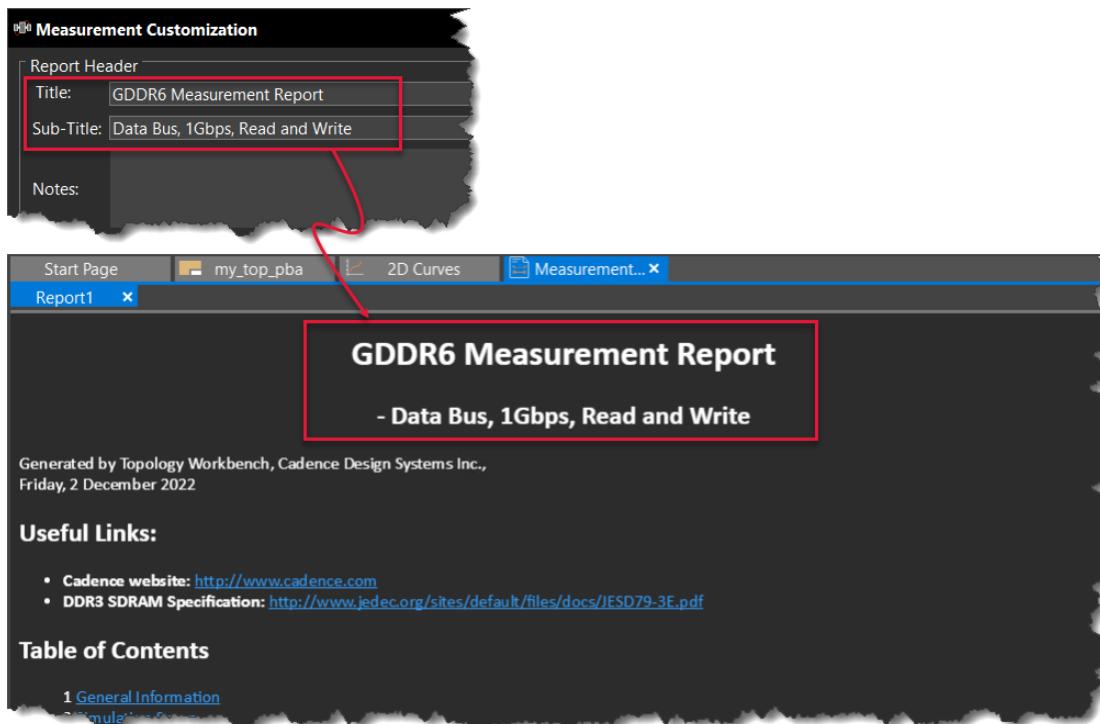
### Reporting DDR Measurements

In addition, in the *2D Curves* tab, you get several data analysis templates for viewing and analyzing the data.



## Contents of the Report

Each report has a header section that displays the *Title* and *Subtitle* of the report you entered in the *Measurement Customization* dialog box accessed from the *Report Generator* dialog box.



The other contents of the report include:

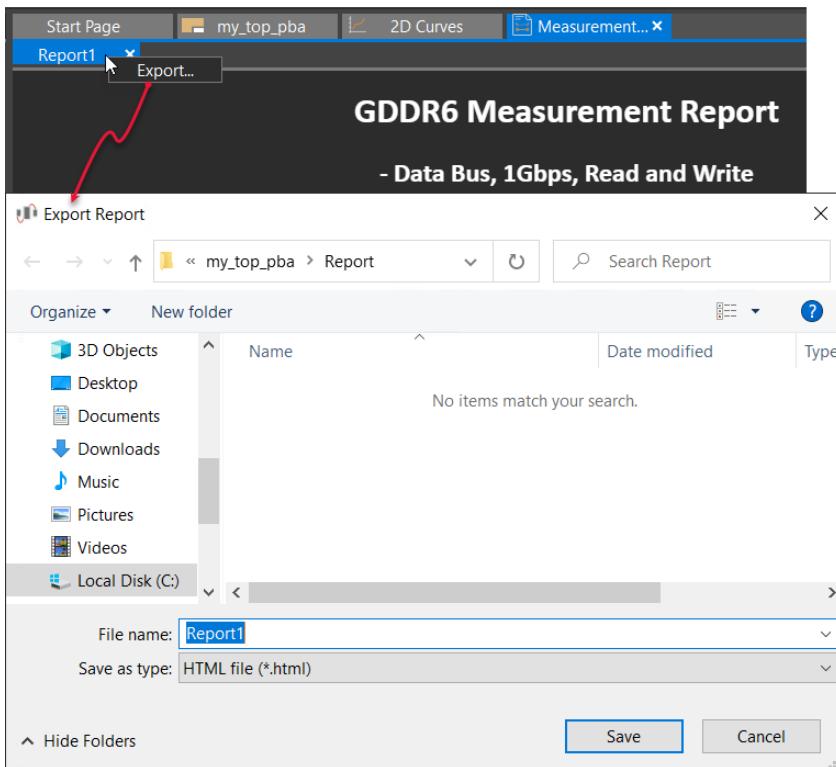
- Entries made in the *Notes* section
- The tool version and the date on which the report was generated
- Useful links to the Cadence website
- Link to the DDRx specification
- General information about the topology file, controller and memory IBIS files, circuit simulator used, and the topology layout
- Simulation setup details
- DDR measurement setup information
- Results for each selected measurement type

## Topology Workbench User Guide

### Reporting DDR Measurements

- Appendix covering the JEDEC DDR measurement definitions and description of abbreviations used in the report

You can also export the report as an HTML file. Right-click the report tab and click *Export* from the displayed shortcut menu. The Export Report dialog opens for you to assign a name to the report file, identify the path where the files should be saved, and then click *Save* to proceed.



# Topology Workbench User Guide

## Reporting DDR Measurements

## Table of Contents

The Table of Contents section provides jump list of links to the various sections in the report. To access a particular section of the report, click the appropriate link in the Table of Contents section.



# Topology Workbench User Guide

## Reporting DDR Measurements

To enable easy navigation, each section of the report has a hotlink next to the heading to go back to the Table of Contents.

Such blue icons across the report are hotlinks which when clicked, take you back to the Table of Contents section.

Iteration 1: C:\TestCases\my\_top\_pba\result\1\Data\_Write\_Typ\_Typ\DiePad

Measurement	Max O <sub>vershoot</sub> (mV)	Max O <sub>vershootArea</sub> (V·ns)	Max U <sub>ndershoot</sub> (mV)	Max U <sub>ndershootArea</sub> (V·ns)	Min R <sub>Back_margin</sub> (mV)	Min R <sub>Back_margin</sub> (mV)	Max Power Ripple (mV <sub>p-p</sub> )	Max Tx Power Ripple (mV <sub>p-p</sub> )
Worst Value					331.762	326.038	0	0
Bus Group					byte0	byte0	byte0	byte0
Rx Signal (Waveform)					dq2	dq2	vddq	vddq
Cycle					12	1		

Such blue icons across the report are hotlinks which when clicked, take you back to the Table of Contents section.

4.1.2 DQ Mask Report ▲

4.1.2.1 Worst Case Summary ▲

Iteration 1: C:\TestCases\my\_top\_pba\result\1\Data\_Write\_Typ\_Typ\DiePad

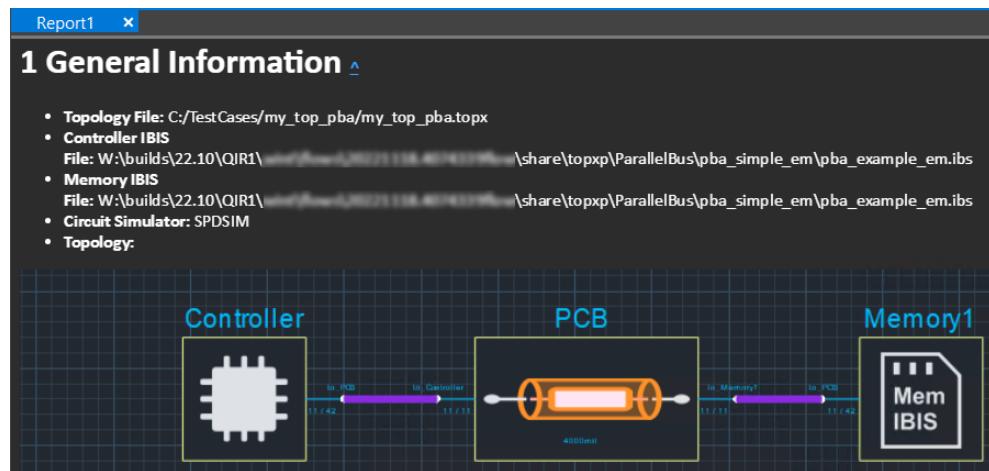
Measurement	DQ Compliance Mask	Min Jitter margin (ps)	Min Noise margin (mV)	Min VIHL_AC (mV)	Min tDIPW (ps)	Min tDQS2DQ (ps)	Max tDQS2DQ (ps)	Max  tDQS2DQ_BC (ps)	Max tDQ2DQ (ps)	Min SlewRate Mask (V/ns)	Max SlewRate Mask (V/ns)
Worst Value	Pass	271.008	387.537	1049.42	998.958	3.0224	4.22871	-0.603159	1.20632	8.07928	8.43688
Bus Group		byte0	byte0	byte0	byte0	byte0	byte0	byte0	byte0	byte0	byte0
Rx Signal		dq2	dq2	dq2	dq2	dq0	dq1	dq0	All cases	dq2	dq0

# Topology Workbench User Guide

## Reporting DDR Measurements

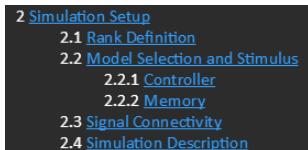
### Section 1 – General Information

This section includes information about the design files, including the names and locations of the IBIS models used in the simulation.



### Section 2 – Simulation Setup

The simulation information is listed, including simulator (HSPICE or SPDSIM), Power (Ideal or Non-ideal) Bus identification, the IBIS model selection and Stimulus for Controller and Memory, the Signal Connectivity, and simulation description.



If the WLO/ClkMeasDelay option was selected in the *Analysis Options* panel, the *Write Leveling Offset* section is added to the report. This section lists the delay values for each memory component, as calculated in the *Write Leveling Offset* dialog box.

For each controller and memory block, the report shows the OnDie Parasitics and Package parasitics model used, bus details, Stimulus Offset, and IO model used for each signal.

# Topology Workbench User Guide

## Reporting DDR Measurements

### Section 3 – DDR Measurement Setup

This section lists all the details specified in the *Report Generator* dialog box. These include the AC and DC logic levels, Specifications for each data bus, and selected Derating Tables for Setup and Hold measurements.

#### 3 DDR Measurement Setup [▲](#)

##### 3.1 AC and DC Logic Input Levels [▲](#)

###### Single-Ended Signals (V)

Iteration#	Receiver	Corner	VIH(ac) min	VIH(ac) max	VIH(dc) min	VIH(dc) max	Vcent_DQ	VDDQ
1	Memory1	Typ	0.875	0.625	0.835	0.665	0.75	1.5
2	Controller	Typ	0.8825	0.6325	0.8425	0.6725	0.7575	1.5

###### Differential Signals (V)

Iteration #	Corner	VIHdiff(ac) min	VIHdiff(ac) max	VIHdiff(dc) min	VIHdiff(dc) max
1	Typ	0.25	-0.25	0.17	-0.17
2	Typ	0.25	-0.25	0.17	-0.17

##### 3.2 Specs [▲](#)

###### 3.2.1 Data Bus Write [▲](#)

	Symbol	Min	Max	Unit	Parameter
DQ Mask	Vref	0.49	0.965	VDDQ	Vref range
	Vref_step	0.005	-	VDDQ	Min Vref stepsize
	Vref_set_tol	0.001	-	VDDQ	Min Vref set tolerance
	VdIVW	47	-	mV	Rx Mask voltage pk-pk
	TdIVW	0.45	-	UI	Rx timing window
	tDQS2DQ			UI	Rx Mask DQS to DQ offset
	tDQ2DQ	-		UI	Rx Mask DQ to DQ offset

# Topology Workbench User Guide

## Reporting DDR Measurements

### 3.3 Setup Derating Table ▲

The selected setup derating table file:

W:\builds\22.10\QIR1\share\topxp\ParallelBus\DeratingTable\Data\_SingleEndedDQS\_AC250\_Setup.

		Delta_tDS (ps) – AC250 tDS Derating Values for DDR2-400/533								
		DQS Single-ended Slew Rate (V/ns)								
		2.0 V/ns	1.5 V/ns	1.0 V/ns	0.9 V/ns	0.8 V/ns	0.7 V/ns	0.6 V/ns	0.5 V/ns	0.4 V/ns
DQ Slew Rate (V/ns)	2.0	188	167	125						
	1.5	146	125	83	81					
	1.0	63	42	0	-2	-7				
	0.9		31	-11	-13	-18	-29			
	0.8			-25	-27	-32	-43	-60		
	0.7				-45	-50	-61	-78	-108	
	0.6					-74	-85	-102	-132	-183
	0.5						-128	-145	-175	-226
	0.4							-210	-240	-291

Note: Derating Table Extrapolation: Nearest.

### 3.4 Hold Derating Table ▲

The selected hold derating table file:

W:\builds\22.10\QIR1\share\topxp\ParallelBus\DeratingTable\Data\_SingleEndedDQS\_DC125\_Hold.

		Delta_tDH (ps) – DC125 tDH Derating Values for DDR2-400/533								
		DQS Single-ended Slew Rate (V/ns)								
		2.0 V/ns	1.5 V/ns	1.0 V/ns	0.9 V/ns	0.8 V/ns	0.7 V/ns	0.6 V/ns	0.5 V/ns	0.4 V/ns

## Section 4 – Results

Results for each of the report data types that you selected in the *Report Generator* dialog box are listed in a tabular format.

4 Results
4.1 Data Bus Write
4.1.1 Waveform Quality Report
4.1.1.1 Worst Case Summary
4.1.2 Eye Quality Report
4.1.2.1 Worst Case Summary
4.1.3 Timing Report
4.1.3.1 Worst Case Summary
4.1.4 Delay Report
4.1.4.1 Worst Case Summary

# Topology Workbench User Guide

## Reporting DDR Measurements

### Waveform Quality Report

The Waveform Quality report includes maximum overshoot and undershoot voltage, Maximum Overshoot and Undershoot Area (voltage-time) and Ringback margin for low and high logic levels, for each simulation for each bus.

## 4 Results [▲](#)

### 4.1 Data Bus Write [▲](#)

#### 4.1.1 Waveform Quality Report [▲](#)

##### 4.1.1.1 Worst Case Summary [▲](#)

Measurement	Max Overshoot (mV)	Max OvershootArea (V·ns)	Max Undershoot (mV)	Max UndershootArea (V·ns)	Min RBack_marginH (mV)	Min RBack_marginL (mV)	Max Power_Ripple (mVp-p)	Max Tx_Power_Ripple (mVp-p)
Worst Value					367.762	350.038	0	0
Bus Group					byte0	byte0	byte0	byte0
Rx Signal (Waveform)					dq2	dq2	vddq	vddq
Cycle					12	1		

##### 4.1.1.2 Eye Quality Report [▲](#)

##### 4.1.2.1 Worst Case Summary [▲](#)

Measurement	Min tVAC_high/tVAC_high (ps)	Min tVAC_low/tVAC_low (ps)	Max Vix_DQS_ratio (%)	Max VDQSmid_to_Vcent (mV)	Min ApertureWidth (ps)	
Worst Value	985.155	980.564	0.394366	8.16958	981.705	980.486
Bus Group	byte0	byte0	byte0	byte0	byte0	byte0
Rx Signal (Waveform / Eye Diagram)	dq3	dq3	dqs0p-dqs0n	dqs0p-dqs0n	dq3	All Signals
Cycle	12	2	1			

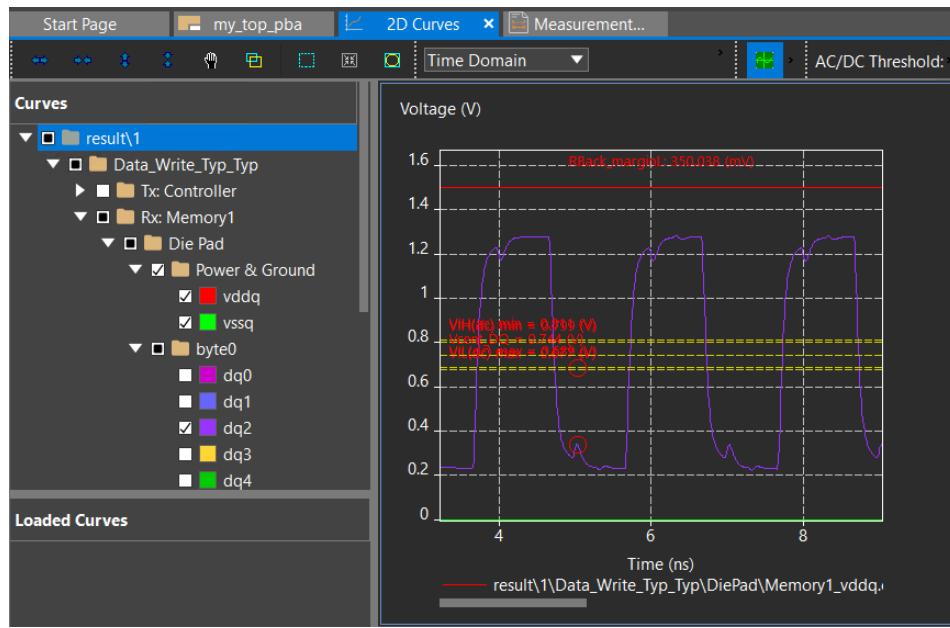
The worst-case values for each of these measurements for the bus are highlighted, and a worst case summary sheet is listed below. The worst case summary table also has p-p max column for Tx and Rx. To display the corresponding ripples in the Waveform Quality Report, ensure that you have run the frequency response simulation. As there is only one controller in each DDRx topology, maximum ripple at the controller side has only one value.

If the *Explicit Power and Ground Terminals* check box is selected in the *Load IBIS* dialog box of the Controller/Memory block, the Waveform Quality measurement uses the signal's own power and ground for the measurements of the Overshoot, OvershootArea, Undershoot, UndershootArea, and Power\_Ripple.

# Topology Workbench User Guide

## Reporting DDR Measurements

When you click a linked values that is highlighted in blue, the corresponding time-domain waveform opens in the *2D Curves* tab as is shown below for signal, *DQ2*. The waveform for the selected signal shows the low and high logic levels overlaid.



By clicking the column header link, the cycle-to-cycle variation for that value is plotted for the bus. For example, the Ringback margin (high) link opens the 2D Curve window that shows the Ringback margin at each cycle for every signal in the bus.

## Eye Quality Report

The Eye Quality report shows the summarized results in a tabular format. It includes the worst-case values, iterations, bus group and signals.

### 4.1.2 Eye Quality Report ▲

#### 4.1.2.1 Worst Case Summary ▲

Measurement	Min tVAC_high/tDVAC_high (ps)	Min tVAC_low/tDVAC_low (ps)	Max Vix_DQS_ratio (%)	Max VDQSmin_to_Vcent (mV)	Min ApertureWidth (ps)	
Worst Value	985.155	980.564	0.394366	8.16958	981.705	980.486
Bus Group	byte0	byte0	byte0	byte0	byte0	byte0
Rx Signal (Waveform/Eye Diagram)	dq3	dq3	dqs0p-dqs0n	dqs0p-dqs0n	dq3	All Signals
Cycle	12	2	1			

The Vix parameters in the eye quality metrics for DDR3 assume a differential clock signal. The measurement is not applicable for DDR2 systems with a single-ended strobe.

As with the Waveform Quality report, clicking the column heading for each measurement opens a 2D curve showing the cycle-to-cycle variation of that parameter.

Clicking the linked signal names given in the table opens the eye diagram for that signal, with the eye aperture plotted with the data on the plot.

## Timing Report

The timing report has a comprehensive tabular listing of JEDEC setup and hold measurements. Raw and slew-rate adjusted (derated) values are listed, with worst-case values highlighted in bold.

Out of Range are typically the undefined values in the derating tables:

- If you selected the *Derating Table Extrapolation* as *Nearest*, a note such as following is added below the derating table:

*Note: Derating Table Extrapolation: Nearest*

- If you selected the *Derating Table Extrapolation* as *None*, a note such as following is added below the derating table:

*Note: cell contents shaded in red are defined as ‘not supported’*

Clicking any of the column headers opens a cycle-to-cycle plot in the 2D Curve window, showing the variation of that parameter for each signal in the bus. This the raw tDS (Setup Time), with the tooltip showing the data for one of the DQ lines at the first cycle. Time periods where a data line does not have a transition will not have data for that cycle. Note that the “raw” prefix indicates that the measurement is taken directly from the raw waveforms that were produced.

Clicking a linked signal name in the table opens the time domain plot for that signal, with its clock/ strobe signal.

## Timing Report – Strobe and Clock

This report is available only for Data bus – Write simulations. If the Data bus has a clock signal defined and connected, the timing margin between the clock signal and the data strobe signal is measured and include in this report.

## Timing Report - Worst Case Condition

If worst case Timing Reference waveforms exist, the DDR report shows additional Timing Report tables for those cases. To generate data for these reports, Topology Workbench shifts the Timing Reference waveform according to the parameters set up in the *Timing Budget* panel, and re-measures all the report criteria. This enables the worst case timing margins to be determined from a single comprehensive time domain simulation run, saving significant simulation time. The shift applied to the Timing Reference signal is documented in each Worst Case report table, and the appropriate shifted waveforms appear when cross probed from these tables.

You can click any signals or parameter to open the 2D Curve or Criteria, and the shifted value of Timing reference is shown on the top of the sheet.

## DQ Mask Report

DQ Mask report is generated on Data Write simulations for DDR4 and LPDDR4 measurements only. DQ Mask report is generated when the Stimulus Offset values are set to the *Default* or *Ideal*, as well as for the user-defined Stimulus Offset values.

Parameters `Vcent_DQ`, `DQ Compliance Mask`, `Min Jitter_margin`, `Min Noise_margin`, and `Min VIHL_AC` are extracted from BER Eye curves. Other parameters in the report are measured from the Rx waveforms, while using the `Vcent_DQ` value extracted from the BER Eye curve.

## CA Mask Report

CA Mask report is generated on Ctrl and AddCmd simulations for LPDDR4 measurements.

## BER Report

BER Report is generated when you perform channel simulations for LPDDR4 and DDR4 buses.

The LBER value displayed in the report is same as the LBER value specified in the channel simulation tab of the *Analysis Options* dialog box.

Clinking a linked signal name displays the *BER\_Eye* diagram for the signal, in the 2D curves window.

Similarly, clicking the Min Eye Width and Min Eye Height values, displays the Bathtub and the Noise Bathtub graphs, respectively, for the signal.

If there are multiple BER Eye curves, pick ‘eye\_jnber’, ‘eye\_ber’ and then ‘eye\_nber’. First check for curves corresponding to 1e-16, if there is no 1e-16 curve, then pick the first curve.

## Delay Report

The Delay report includes Rx Signal and Tx Buffer Output information, MeasDelay, BufferDelay, InterconnectDelay, InterconnectSkew, StrobeInterconnectSkew, FirstSwitch, and FinalSettle. The worst-case values are highlighted in Bold, and a worst case summary sheet is listed in the following figure.

The *Stimulus Offset* column is populated for designs that have the *WLO/ClkMeasDelay* option is selected in the *Analysis Options* panel.

If the *WLO/ClkDelay* option is selected in the *Analysis Options* panel, the *Stimulus Offset* column includes the WLO values for controller block and ClkDelay values for memory block.

The delay measurements are defined as below:

- **BufferDelay**

The output buffer model used for signal integrity analysis is connected to the Tco test load and simulated. The delay is measured at the point where the output pin crosses Vmeas. The corresponding delay is then saved and used in flight time computations.

- **MeasDelay**

Measure delay(MeasDelay) is measured from time 0 in the simulation to when the receiver waveform crosses the Vmeas threshold.

- **InterconnectDelay**

InterconnectDelay is measured on the first cycle as follows:

`MeasDelay - BufferDelay`

This produces one value for each net.

- **InterconnectSkew**

InterconnectSkew is measured on each cycle as follows:

`InterconnectDelay_Signal - InterconnectDelay_TimingRef`

The max one of these gets reported in the Delay Report as *Max InterconnectSkew*.

- **StrobeInterconnectSkew**

StrobeInterconnectSkew is measured on each cycle as follows:

`InterconnectDelay_Strobe - InterconnectDelay_Clock`

## Topology Workbench User Guide

### Reporting DDR Measurements

The max one of these gets reported in the Delay Report as *Max StrobeInterconnectSkew*.

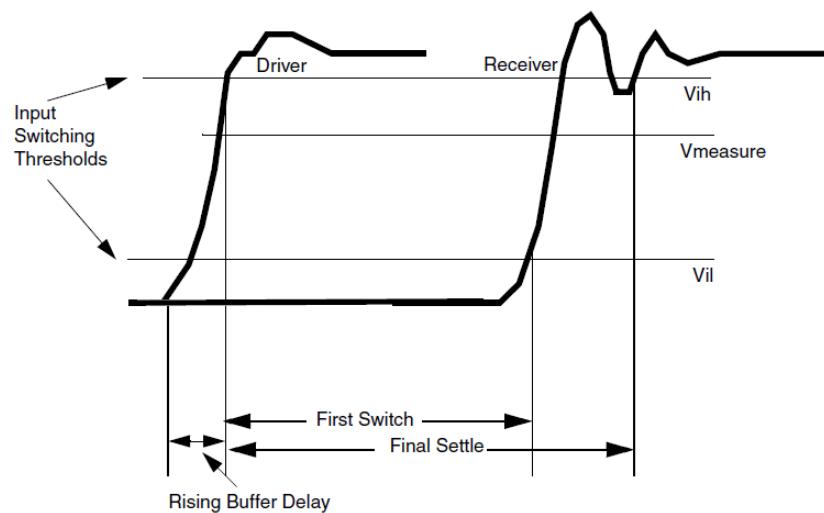
#### ■ FirstSwitch

This is determined by subtracting the associated buffer delay from a simulation measurement. For example, on a rising (falling) edge, the simulation measurement is from time zero to when the receiver first crosses its  $V_{ih}$  ( $V_{ih}$ ) DC logic threshold. The associated rising (falling) buffer delay of the driving IOCell is subtracted from this measurement value to produce the reported first switch delay.

#### ■ FinalSettle

This is determined by subtracting the associated buffer delay from a simulation measurement. For example, on a rising (falling) edge, the simulation measurement is from time zero to when the receiver crosses its  $V_{ih}$  ( $V_{ih}$ ) AC logic threshold the final time and settles into the high (low) logic state. The associated rising (falling) buffer delay of the driving IOCell is subtracted from this measurement value to produce the reported final settle delay.

The following diagram illustrates buffer delay, first switch delay, and final settle delay for a rising signal.



## Section 5 – Appendix

This section provides links to the *JEDEC DDR Measurement Definitions* and *Descriptions of Abbreviations* as shown below.

### 5 Appendix ^

#### 5.1 [JEDEC DDR Measurement Definitions](#) ^

#### 5.2 [Description of Abbreviations](#) ^

Clicking the *JEDEC DDR Measurement Definitions* link opens a new tab in the browser window. It contains links documents to the different specifications. These specifications documents explain each of the measurements included in the generated report.

The screenshot shows a web browser window with two tabs open: "DDR\_Measurement\_Definitions\_1" and "Description\_of\_Abbreviations". The main content area displays the "DDR Measurement Definitions" page. The title "DDR Measurement Definitions" is centered at the top. Below it, a section titled "Useful Links:" lists several URLs for various DDR SDRAM specifications. At the bottom of the page is a diagram illustrating signal overshoot and undershoot relative to supply voltages VDDQ and VSSQ.

**Useful Links:**

- Cadence website: <http://www.cadence.com>
- DDR1 SDRAM Specification: <http://www.jedec.org/sites/default/files/docs/JESD79F.pdf>
- DDR2 SDRAM Specification: <http://www.jedec.org/sites/default/files/docs/JESD79F-2F.pdf>
- DDR3 SDRAM Specification: <http://www.jedec.org/sites/default/files/docs/JESD79-3E.pdf>
- DDR4 SDRAM Specification: <http://www.jedec.org/sites/default/files/docs/JESD79-4.pdf>
- LPDDR2 SDRAM Specification: <http://www.jedec.org/standards-documents/docs/jesd209-2e>
- LPDDR3 SDRAM Specification: <http://www.jedec.org/standards-documents/docs/jesd209-3>
- LPDDR4 SDRAM Specification: <http://www.jedec.org/standards-documents/docs/jesd209-4>

**1 Overshoot**

The diagram illustrates a digital signal waveform between two horizontal lines labeled VDDQ (top) and VSSQ (bottom). The waveform rises from VSSQ to a peak and then falls back towards VSSQ. Two green shaded regions represent the excursion above and below the VDDQ and VSSQ levels. The upper green region is labeled "Overshoot Area" and the lower green region is labeled "Undershoot Area". Vertical double-headed arrows indicate the "Maximum Amplitude" for both the overshoot and undershoot areas.

# Topology Workbench User Guide

## Reporting DDR Measurements

Clicking the *Description of Abbreviation* link also opens a new tab in the browser window. It displays a table containing the abbreviations used in the report and their meanings.

ApertureWidth	Aperture Width of Eye Diagram
BufferDelay	Buffer Delay of the Tx IO Model
CA	Command, Bank, and Address Signal
CK	Command-Address Clock
ClockInterconnectSkew	Skew between Strobe and Clock
DDR	Double Data Rate
DDR SDRAM	Double Data Rate Synchronous Dynamic Random-Access Memory
DM	Write Data Mask Signal
DQ	Data Signal
DQS	Data Strobe Signal
FinalSettle	Final Settle Delay
FirstSwitch	First Switch Delay
IBIS	Input Output Buffer Information Specification
InterconnectDelay	MeasDelay - BufferDelay
InterconnectSkew	Interconnect Skew between the Signal and TimingRef
JEDEC	Joint Electron Devices Engineering Council
MeasDelay	Measured Delay at Rx crossing of Vmeas (per IBIS)
NA	Not Applicable
NMP	No Measurement Possible
OOR	Out of Range
Overshoot	Max Excursion of Signal over Power Rail
OvershootArea	Area of Overshoot Event in V-ns
Power_Binola	Back to Back Transistor Binola on Power Rail

## **Topology Workbench User Guide**

### Reporting DDR Measurements

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## Adding Channel Simulator Controls

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In the *Analysis Options* panel, the *Simulation Setup* section displays the *Channel Simulation* tab in the following scenarios:

- Serial Link Analysis (SLA) workflow, where channel simulators are supported automatically
- Parallel Bus Analysis (PBA) workflow, when the *Use Channel Simulator* check box is selected in the *Simulation Setup* schema of the *Workflow* panel

In addition to other settings, the *Channel Simulator Controls* text field in the *Channel Simulation* tab lets the expert users pass specific global controls to the channel simulator using the following syntax:

```
<command_name> <value(s)>
```

The specified controls are then reflected in the simulation results.

Some of the global controls that you can specify are used for:

- [Controlling the AMI Model](#)
- [Capturing User-Supplied Step Responses](#)
- [Probing All Eye Contours](#)
- [Changing ISI Only Eye Contour](#)
- [Saving Tx Bits as Output](#)
- [Controlling Output of Waveforms](#)

### Controlling the AMI Model

**Note:** You should avoid using these controls. Use them only if the AMI model is not IBIS compliant and not robust.

## useblkflt

<b>Syntax</b>	useblkflt <number>
<b>Description</b>	Controls the getwave size. The getwave blocks will be made of <number> bits.
<b>GUI Equivalent</b>	Select the <i>GetWave block size (in bits)</i> check box in the <a href="#">Channel Simulation</a> tab of the <i>Options</i> dialog box. The value specified in the corresponding text box specifies the block size in bits.

## ignoreamiclk

<b>Syntax</b>	ignoreamiclk
<b>Description</b>	Ignores the clock vector returned by the AMI model.
<b>GUI Equivalent</b>	Select the <i>Ignore clock ticks from AMI models</i> check box in the <a href="#">Channel Simulation</a> tab of the <i>Options</i> dialog box.

# Capturing User-Supplied Step Responses

## impfile

<b>Syntax</b>	impfile (<tx_id> <path_to_user_supplied_rx_step_response_file> (type step))
<b>Description</b>	In the syntax: <ul style="list-style-type: none"> <li>■ &lt;tx_id&gt; is the name of the Tx block. It should be the same name as that appears in the <code>command.txt</code> file</li> <li>■ &lt;user_supplied_rx_step_response_file&gt; is a two-column step response file. The first column is <i>time</i>, and the second column is the <i>step response</i>.</li> </ul>

## Probing All Eye Contours

### **probealleyes**

<b>Syntax</b>	probealleyes
<b>Description</b>	<p>Normally, the eye contour at the Rx output is an ISI only eye contour. You can also output ISI only eye contours at the following additional points: Tx input, Tx output (if the Tx has an AMI model and the model uses getwave), and Rx input.</p> <p>The files are in the standard tab-delimited ASCII format and are named as:</p> <ul style="list-style-type: none"> <li>■ eyectr_in.txt (Rx input)</li> <li>■ eyectr_tx.txt (Tx input and output only if Tx AMI model with getwave is available)</li> <li>■ eyectr_tx_in.txt</li> </ul>
<b>GUI Equivalent</b>	Select the <i>Probe All Eyes (Contours at Tx Input, Tx Output, and Rx Input)</i> check box in the <u>Channel Simulation</u> module of the <i>Options</i> dialog box.

## Changing ISI Only Eye Contour

By default, the eye contour is ISI only eye (as opposed to BER eye). You can modify the eye contour to a BER eye by using the following directives:

### **eyectr\_nber**

<b>Syntax</b>	eyectr_nber 1e-12
<b>Description</b>	The eye contour will now be 1e-12 nBER eye.

### **eyectr\_ber**

<b>Syntax</b>	eyectr_ber 1e-12
<b>Description</b>	The eye contour will now be 1e-12 BER eye.

## **eyectr\_jnber**

<b>Syntax</b>	eyectr_jnber 1e-12
<b>Description</b>	The eye contour will now be 1e-12 jnBER eye.

## **Adjusting Eye Contour Position**

### **peakshift**

<b>Syntax</b>	stat (peakshift x)
<b>Description</b>	Setting the value of x to 0, 1, or 2 for the peakshift channel simulator control adjusts the eye contour position.

## Saving Tx Bits as Output

### **output\_txbits**

<b>Syntax</b>	output_txbits
<b>Description</b>	To save Tx bits as output, use the <code>output_txbits</code> command. The Tx bits are stored in a two-column (time and voltage) ASCII file, <code>srcbit_&lt;tx_id&gt;.txt</code> .

## Controlling Output of Waveforms

### **wavecnt**

<b>Syntax</b>	<code>wavecnt [&lt;directive&gt;]</code>
<b>Description</b>	<p>By default, 1000 bits of waveforms are output to <code>waveform.txt</code>. This output is controlled by the <code>wavecnt</code> directive. You can modify the number of bits by passing these as a parameter. The command syntax in that case is <code>wavecnt &lt;#_bits&gt;</code> instead of just <code>wavecnt</code>.</p> <p>In addition to the Rx output, you can also continue on the theme of cheap probing by modifying <code>wavecnt</code> to output waveforms at Rx input, Tx input and Tx output by specifying these as parameters. The command is:</p> <pre>wavecnt (tx) (txin) (rxin)</pre> <p>The corresponding waveforms are available in the ASCII tab delimited files <code>chan2_tx.txt</code>, <code>chan2_tx_in.txt</code>, and <code>chan2_in.txt</code>, respectively.</p> <p><b>Note:</b> Tx input and output waveforms are available only if Tx has a <code>getwave</code> type of AMI model.</p>