

System Connectivity Manager Tutorial

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Preface

This chapter discusses the following:

- [Purpose of This Tutorial](#) on page 16
- [Audience](#) on page 16
- [How to Use This Tutorial](#) on page 17
- [Related Information](#) on page 22
- [Syntax Conventions](#) on page 22

Purpose of This Tutorial

This tutorial provides lessons, sample design files, and multimedia demonstrations to help new users learn how to use System Connectivity Manager.

The tutorial contains the following modules:

- [Module 1: Working with Projects](#) on page 21
- [Module 2: Working with Components and Connectivity](#) on page 53
- [Module 3: Working with Associated Components](#) on page 109
- [Module 4: Working with Properties](#) on page 137
- [Module 5: Working with Constraints](#) on page 161
- [Module 6: Creating a Hierarchical Design](#) on page 197
- [Module 7: Generating Document Schematic](#) on page 231
- [Module 8: Generating Reports](#) on page 253

Audience

This tutorial is designed to get you quickly started with System Connectivity Manager. This tutorial assumes that you are familiar with the development and design of electronic circuits at the system or board level. This tutorial also assumes a working knowledge of the following Cadence tools:

- Allegro Design Entry HDL
- Allegro Constraint Manager
- Allegro PCB Editor
- Allegro SigXplorer

Software Requirements

To perform all the exercises in this tutorial, you need the following Cadence tools:

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- System Connectivity Manager
- Allegro Design Entry HDL
- Allegro Constraint Manager
- Allegro PCB Editor
- Allegro SigXplorer

How to Use This Tutorial

The training is offered in three learning modes:

- Written lessons provide detailed procedures for performing basic operations.
- Multimedia presentations demonstrate the written procedures.
- Sample design files offer a starting point for practicing with the tools.

Depending on your personal learning style, you can use this tutorial in different ways:

- You might begin by reading through the written tutorial lessons. After completing each lesson, watch the multimedia demonstration to enhance your understanding of the procedures. Then, work through the procedures yourself using the sample design files with System Connectivity Manager.

Note: The exercises in this tutorial are built on a sample design and are progressive in nature. Follow the lessons in the sequence used in this tutorial. Skipping lessons might unsynchronize the design with the screenshots given in the tutorial.

- Another approach you can take is to watch the multimedia demonstrations first to gain a general understanding of how to work with the tools. Then, as you experiment with the sample files using System Connectivity Manager, you can refer to the written lessons to refresh your memory about procedures you saw in the demonstrations.

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The written lessons, demonstrations, and sample designs all work together to reinforce your learning experience. Use them in a way you find most conducive to learning.

Understanding the Sample Design Files

You can load the sample design files into System Connectivity Manager and begin working with them immediately. The lessons and multimedia demonstrations use these same design files to illustrate the procedures. You can work with the design files as you progress through the lessons.

Before you can use the sample design files, install the design files and set the required environment variables as described below.



All the steps described in this tutorial assume that the sample design files are installed into a `designs` folder on your `c :\` drive. If you install the sample design files at any other location, the file locations described in the tutorial steps and the file locations displayed in the screenshots in the tutorial will change accordingly.

Installing the Design Files

To use the design files, copy them to your system using the following instructions:

On Microsoft Windows

1. Create a directory in which you want to install the design files.
For this tutorial, we will refer to this directory as
`<your_work_area>`.

Note: For this tutorial `<your_work_area>` is set to the `c :\designs` folder. If you install the sample design files at any other location, the file locations described in the tutorial steps and the file locations displayed in the screenshots in the tutorial will change accordingly.

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2. Copy the `ade_tut_db.zip` file. It is located in the following directory:

`<install_dir>/doc/ade_tut/tutorial_examples`

to the `<your_work_area>` directory.

3. Unzip the `ade_tut_db.zip` file.

UNIX and Linux

1. For this tutorial, we will refer to this directory as `<your_work_area>`.
2. Copy the `ade_tut_db.t.Z` file. It is located in the following directory:

`<your_inst_dir>\doc\ade_tut\tutorial_examples`

to the `<your_work_area>` directory.

3. Uncompress and untar the `ade_tut_db.t.Z` file.

Note: For more information about the tutorial files, see [List of Sample Design Files](#) on page 284.

Setting Environment Variables

After installing the design files, you need to set the following environment variables on your system:

| Environment Variable | Description |
|----------------------|---|
| TUTORIAL_LIB | This environment variable should point to: <code><your_work_area>/reference/ref_lib</code> |

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| Environment Variable | Description |
|-------------------------|---|
| TDD_START_PROJ_LOCATION | <p>This environment variable should point to:</p> <p><i><your_work_area></i></p> <p>The TDD_START_PROJ_LOCATION environment variable specifies the default location in which all new projects will be created. For example, if you specify c:\designs as the value for the TDD_START_PROJ_LOCATION environment variable, and create a new project using the New Project Wizard in System Connectivity Manager, the project will be created in the c:\designs folder, unless you specify a different location for the project.</p> |

You must also set the PADPATH and PSMPATH Allegro environment variables by doing the following:

1. Type the following command in the Windows or UNIX command prompt:

enved

The User Preferences Editor dialog box appears.

Note: The enved utility is available only if you have Allegro PCB Editor set in your path.

2. In the *Categories* list, expand the *Paths* tab.
3. In the *Paths* list, click *Library*.
4. Click the *Value* button next to the padpath variable.

The padpath items dialog box appears.

5. Add the following path:

<your_work_area>/reference/pcb/symbols

6. Click *OK*.
7. Click the *Value* button next to the psmpath variable.

The psmpath items dialog box appears.

8. Add the following path:

<your_work_area>/reference/pcb/symbols

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9. Click *OK*.

10. Click *OK* to close the User Preferences dialog box.



The `enved` utility is available only if you have Allegro PCB Editor set in your path. If this utility is not present, then, for this tutorial, add the following lines in your `.cpm` file. This will ensure that when you add a component using Part Information Manager, the footprint information is also displayed.

```
START_ALLEGRO
psmpath '$TDD_START_PROJ_LOCATION/ade_tut_db/reference/
pcb/symbols'
padpath '$TDD_START_PROJ_LOCATION/reference/ade_tut_db/
pcb/symbols'
END_ALLEGRO
```

Understanding Multimedia Demonstrations

The multimedia demonstrations that accompany the tutorial lessons offer visual ways to grasp concepts and techniques that are described in the procedures. The demonstrations support and illustrate the procedures.

You can launch multimedia demonstrations in three ways:

- Click the hyperlink in the Multimedia Demonstration section in the beginning of a module or preceding the procedure for each lesson.
- Go to the section [List of Multimedia Demonstrations](#) on page 285 and click the hyperlink for the demo that you want to run.
- Open the System Connectivity Manager Start page and click the *DEMOS* tab. Then click the links in the *DEMOS* tab to view the demos.

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Getting the Flash Player

To view the multimedia demonstrations, you need to install the appropriate Adobe Flash Player on your system. Adobe Flash Player is free and is available for different operating systems at:

<http://www.adobe.com/shockwave/download/alternates/>

You can download the appropriate Adobe Flash Player for Windows, Solaris, and Linux operating systems.

Related Information

For more information about how to use System Connectivity Manager, see the following online manual, which can be accessed from the Cadence Program Group and from the Help menus of individual tools.

- *System Connectivity Manager User Guide*

Note: At the end of each lesson, you will find references to related sections of *System Connectivity Manager User Guide*.

Syntax Conventions

This list describes the syntax conventions used in this tutorial.

| | |
|-----------------|---|
| literal | Key words that you must enter literally. These keywords represent commands (functions, routines) or option names. |
| Courier font | Command line examples. |
| <i>UI</i> | Menus, labels, fields, or tabs in the user interface. |
| <i>variable</i> | Arguments for which you must substitute a value. |

Module 1: Working with Projects

Prerequisite

Install the sample design files and set the environment variables as described in [Understanding the Sample Design Files](#) on page 16.

Lessons

This module consists of the following lessons:

- [Overview](#) on page 24
- [Lesson 1-1: Starting System Connectivity Manager](#) on page 30
- [Lesson 1-2: Creating a Project](#) on page 31
- [Lesson 1-3: Setting Up the Project](#) on page 42
- [Lesson 1-4: Setting Up Libraries for the Project](#) on page 47

Multimedia Demonstration

 A Flash-based multimedia demonstration of this module, [Creating a Project in System Connectivity Manager](#), is available on Cadence Online Support.

Completion Time

1 hour for written lessons

8 minutes for multimedia demonstrations

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Module 1: Working with Projects

Prerequisite

Follow the instructions in [Understanding the Sample Design Files](#) on page 16 to install the sample design files and set the required environment variables.

Overview

The first task you perform in designing a PCB is to create a design project. A design project is the encapsulation of paths to libraries, part tables, tool settings, project-level settings, global settings and other related settings for designing a PCB to required specifications.

A design project consists of the following:

- Reference libraries
- Project libraries
- `cds.lib` file
- Project file (`.cpm` file)

The following sections provide more details about these components.

What are Libraries?

You begin the design process by creating a logic design using System Connectivity Manager or Allegro Design Entry HDL and then a board-level design that translates the logic design into a manufacturable entity. To accomplish this process, tools need a *software* representation of the various parts to be used in the design. The representations of these parts are organized into libraries.

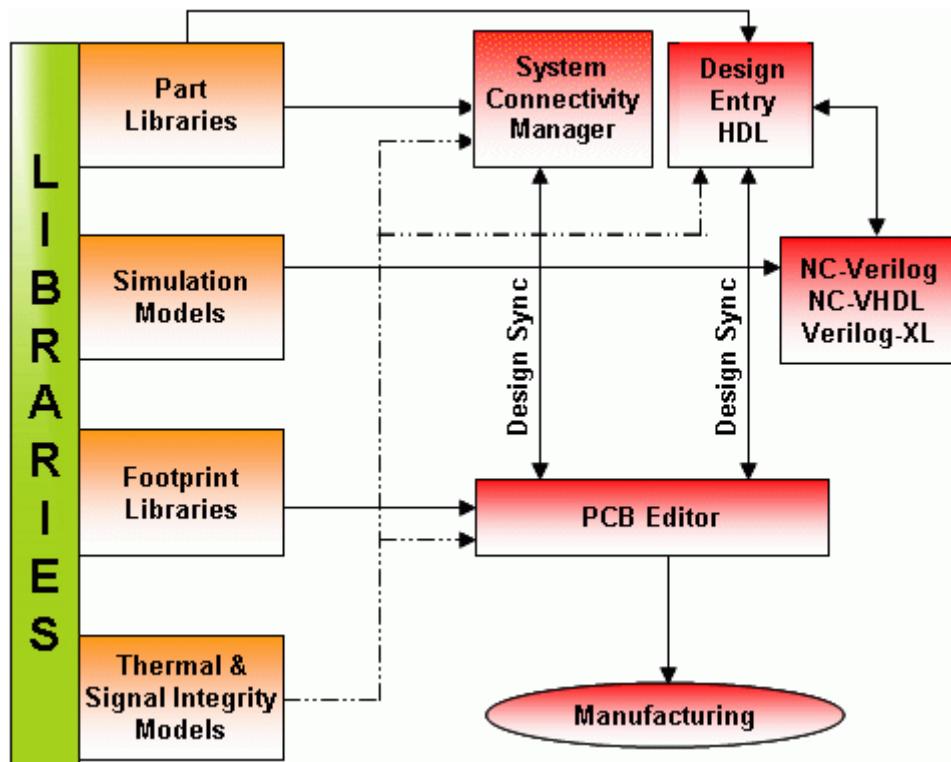
The different tools used in the various stages of the design flow, need different views or information about the same part. Some of these views are schematic, footprint, and simulation.

These views are organized into several libraries. For example, footprints of various parts are consolidated into a single layout library.

System Connectivity Manager Tutorial

Module 1: Working with Projects

The library organization for Cadence PCB design tools is as follows:



- Part libraries

These libraries contain views for design entry or schematic creation. The information contained in these views includes logical symbols (graphical representations of the part), pinouts, and packaging information.

- Footprint libraries

These libraries contain the footprints that correspond to the physical parts specified in part libraries. These libraries are required at the layout stage of the design flow.

- Simulation Libraries

These libraries model the behavior of the part in the Verilog or VHDL Hardware Description Languages. These libraries are required during the design verification phase.

System Connectivity Manager Tutorial

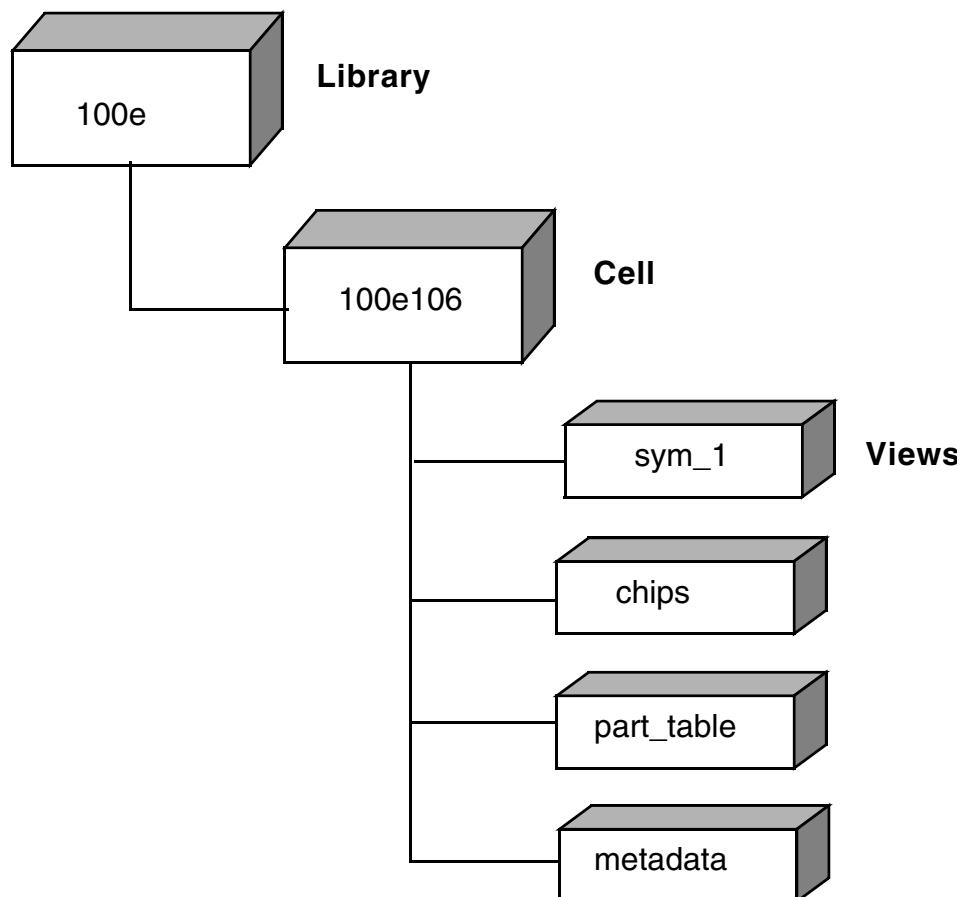
Module 1: Working with Projects

Reference Libraries

Cadence supplies a set of reference libraries that contain views of parts belonging to several logic families. The `lsttl` library is an example of a reference library. Reference libraries are usually stored in an area to which you do not have write permissions and are managed by a librarian. The Cadence reference libraries are located at `<your_inst_dir>/share/library`

The following figure illustrates the structure of a reference library.

Figure 4-1 Library Organization: Reference Libraries



System Connectivity Manager Tutorial

Module 1: Working with Projects

The following table describes each view within a part in a reference library.

| View Name | Description |
|------------|--|
| sym_1 | Contains the schematic symbol. When you add a part to a design, a reference to the symbol view is placed in the design only (not the actual part). |
| chips | Maps the logical part to the physical package (pinouts). You can also use this view to assign other physical properties (for example, input and output loading characteristics, and voltages). |
| part_table | Lets you add custom part properties to fit your company needs. For example, you can add a company part number, part description or any in-house or vendor information you require. |
| metadata | Contains version information for the part. |

Project Libraries

Project libraries (also known as local or design libraries) are used by designers at the project level. Project libraries contain parts customized for your project and the logical design you capture in System Connectivity Manager.

The libraries in which the designs you capture in System Connectivity Manager are stored are known as working libraries. By default, the directory for the working library for a project has the name `<projectname>_lib`. For example, if you create a project named `memory.cpm`, the working library for the project will be named `memory_lib`.

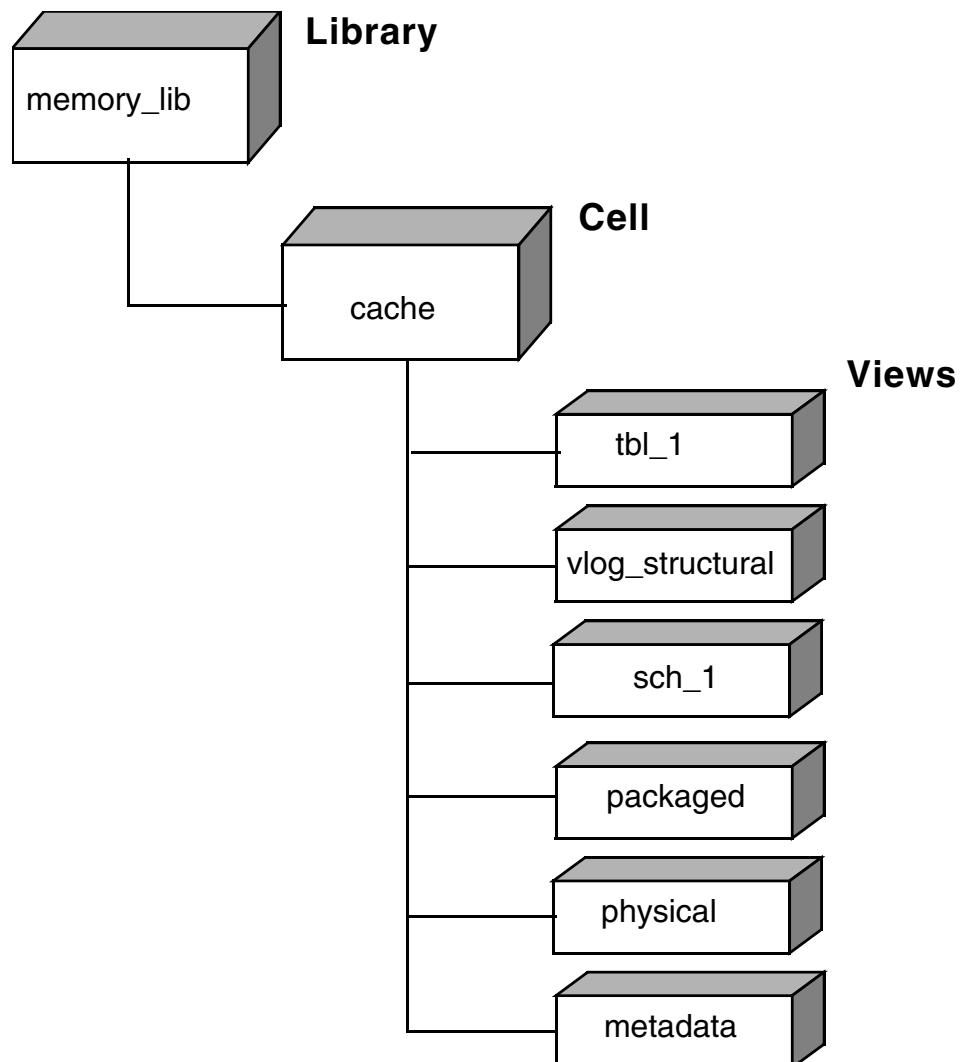
Each design is stored in a subdirectory within a working library. This subdirectory is known as a cell. A cell can represent the entire design or just a portion of the design (or hierarchy). Each cell or design contains subdirectories that represent different design phases (known as cell views).

[Figure 4-2 on page 28](#) illustrates the structure of a project library.

System Connectivity Manager Tutorial

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Figure 4-2 Library Organization: Project Libraries



The following table describes each view in a design library.

| View | Description |
|-----------------|---|
| tbl_1 | Contains the table based design. |
| sch_1 | Contains the schematics. |
| vlog_structural | Contains the Verilog description of the design. |
| packaged | Contains the results of packaging. |

System Connectivity Manager Tutorial

Module 1: Working with Projects

| View | Description |
|----------|--|
| physical | Contains the PCB layout. |
| metadata | Contains version information for the design. |

What is a `cds.lib` File?

System Connectivity Manager is a by-reference design editor. This means that System Connectivity Manager references all parts in the design from various libraries that reside in the reference or project area.

The `cds.lib` file is the library definition file that defines all the libraries used in your design and maps them to their physical locations. The contents of a typical `cds.lib` file is given below:

```
DEFINE 54alsttl ../../library/54alsttl
DEFINE 54fact ../../library/54fact
DEFINE tutorial_lib worklib
DEFINE local_lib local_lib
INCLUDE $CHDL_LIB_INST_DIR/share/cdssetup/cds.lib
```

For more information on the `cds.lib` file, see *Design Entry HDL Libraries Reference*.

What is a Project File?

When you create a new project, System Connectivity Manager creates a project file called `<projectname>.cpm` in the project directory. The `<projectname>.cpm` file includes the following setup information for your project:

- The name of the top-level design and the library in which it is located.
- The list of project libraries.
- The location of the temporary directory where tools generate intermediate data
- Setup directives for System Connectivity Manager, Design Entry HDL, PCB Editor, and any other tool launched from the project.

System Connectivity Manager Tutorial

Module 1: Working with Projects

Lesson 1-1: Starting System Connectivity Manager

Overview

In this lesson, you will learn to start System Connectivity Manager.

Procedure

1. To start System Connectivity Manager on Microsoft Windows, do one of the following:
 - ❑ From the Windows *Start* menu, choose *Programs – Cadence SPB 17.x – System Architect*.
(Launches System Connectivity Manager from Allegro System Architect.)
 - ❑ From the Windows *Start* menu, choose *Programs – Cadence SPB 17.x – SiP Digital Architect*.
 - ❑ From the Windows Start menu, choose *Run* to open the Run dialog box. Type `scm` and press *Enter*.
 - ❑ Type the following command in the Windows command prompt:
`scm`
2. From the Cadence Product Choices dialog box, select the appropriate license and click *OK*.

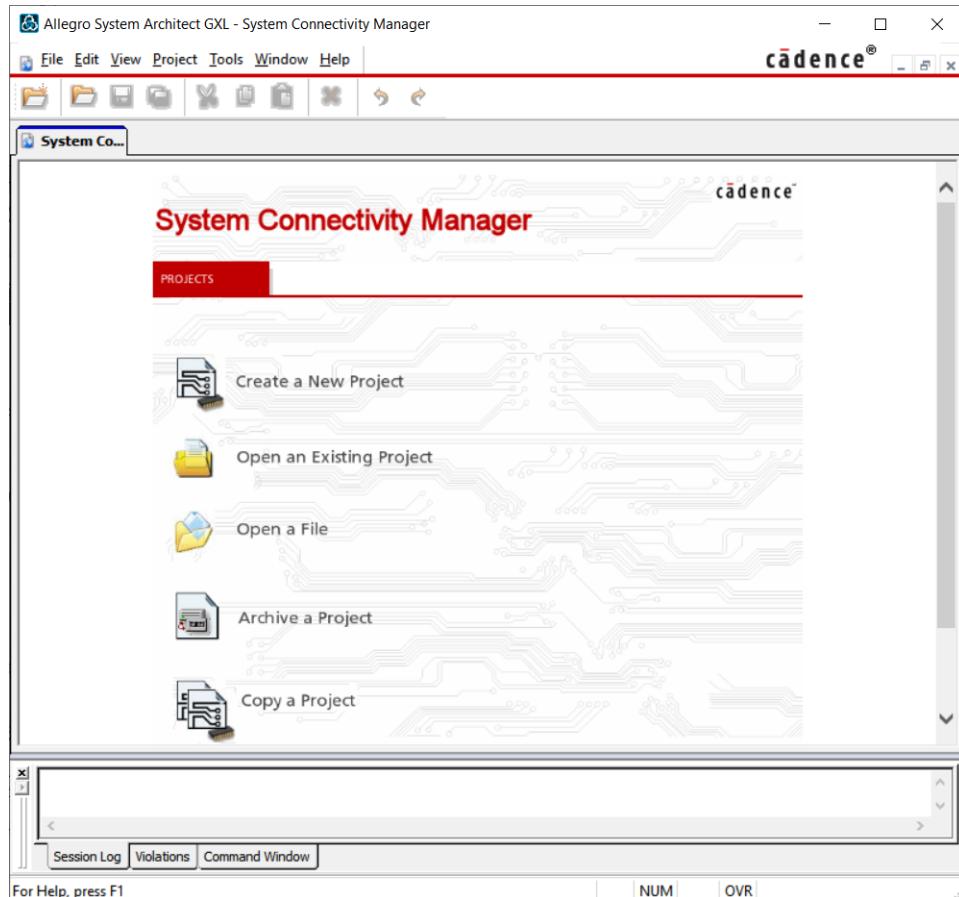
To start System Connectivity Manager on Unix or Linux

1. Open a terminal window and type the following command:
`scm`
2. From the Cadence Product Choices dialog box, select the appropriate license and click *OK*.

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Module 1: Working with Projects

The System Connectivity Manager Start Page appears.



Lesson 1-2: Creating a Project

Overview

In this lesson, you will learn to create a project in System Connectivity Manager.

Procedure

The New Project Wizard guides you through creating your project in System Connectivity Manager.

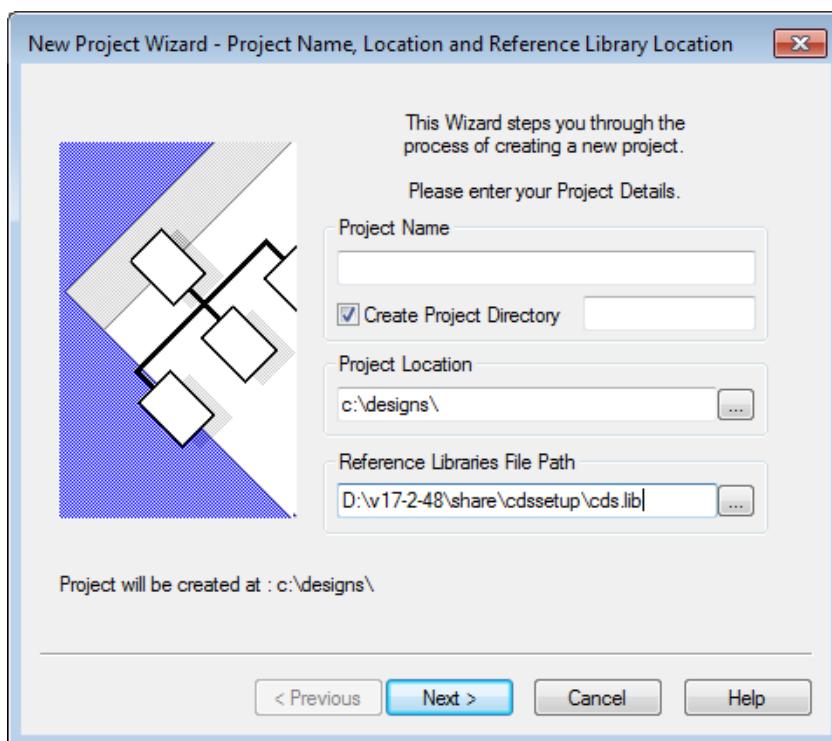
1. To access the New Project Wizard, do one of the following:

System Connectivity Manager Tutorial

Module 1: Working with Projects

- ❑ Click the *Create a New Project* icon in the System Connectivity Manager Start page.
- ❑ Choose *File – New – Project*.

The Project Name, Location and Reference Library Location page appears.



The default project location is displayed as `c:\designs\` because the `TDD_START_PROJ_LOCATION` environment variable is set to `c:\designs`. For more information on the `TDD_START_PROJ_LOCATION` environment variable, see [Understanding the Sample Design Files on page 16](#).

2. In the *Project Name* field, enter the project name as follows:

`tutorial`

The wizard will create a project file called `tutorial.cpm`.

Note: Use only lowercase letters, numbers and the underscore (`_`) character in project names.

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Module 1: Working with Projects

The project name is automatically added in the text box next to the *Create Project Directory* check box. This implies that the project files will be created in the `tutorial` folder.

Note: To ensure easy identification of projects, by default, System Connectivity Manager creates project files in a directory that has the same name as the name specified in the *Project Name* field.

If you want the project files to be created in a folder with a different name, select the *Create Project Directory* check box. In the text box next to it, specify the name of the folder in which the project files are to be created.

Although the default project location is specified as the value of the `TDD_START_PROJECT_LOCATION` environment variable, you can use the Browse button to specify a different location.

3. By default, the library definition file (`cds.lib`) in your Cadence installation directory is set as the reference library for the project. For this tutorial, we will use another reference library.

In the *Reference Libraries File Path* field, enter the reference library file path as:

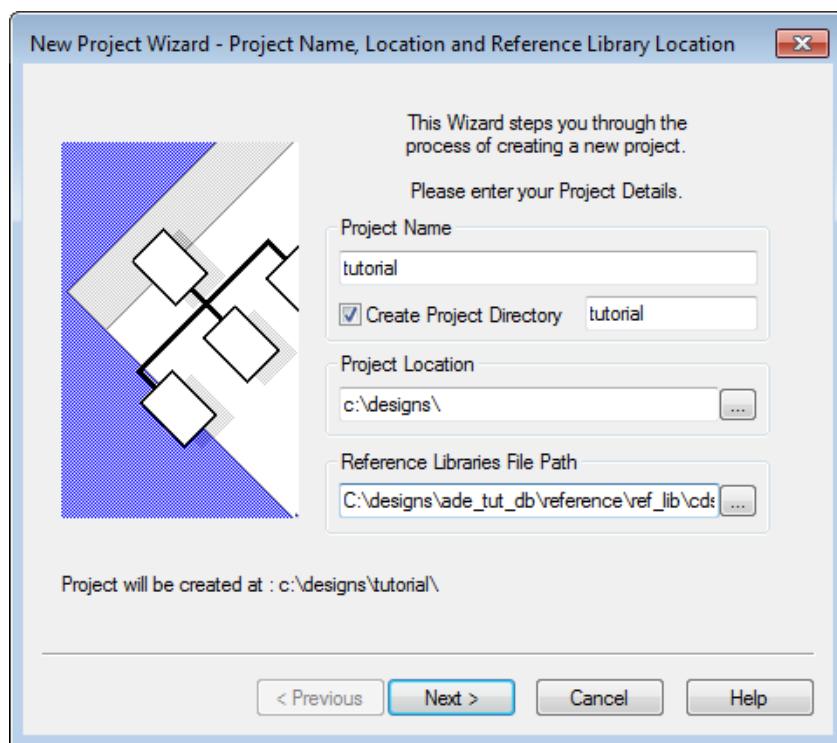
`<your_work_area>\reference\ref_lib\cds.lib`

Where `<your_work_area>` is the location where you have installed the sample design files for this tutorial.

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Module 1: Working with Projects

This `cds.lib` file defines the path to the part libraries you will use in this tutorial.

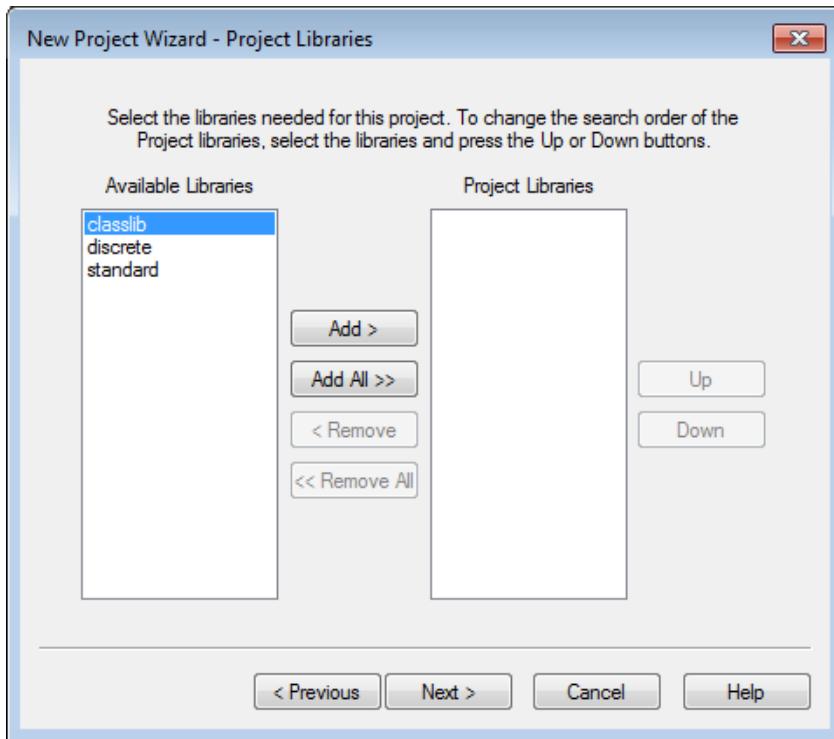


4. Click *Next*.

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Module 1: Working with Projects

The Project Libraries page appears.



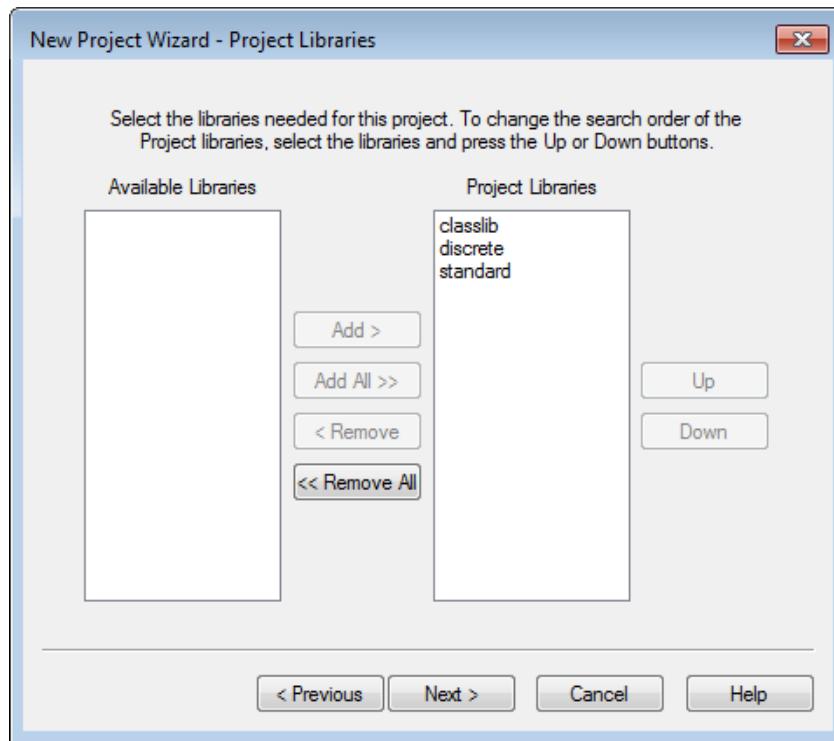
The reference libraries are displayed in the *Available Libraries* list. You can select the libraries you want to use in your project by adding them to the *Project Libraries* list. For this project, you will add all the libraries to the Project Libraries list.

Note: If you do not add a library now, you can add it later using the *Libraries* tab in the System Connectivity Manager Setup dialog. For more information, see [Lesson 1-4: Setting Up Libraries for the Project](#) on page 47.

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Module 1: Working with Projects

5. Click the *Add All* button to add the reference libraries in the *Project Libraries* list.

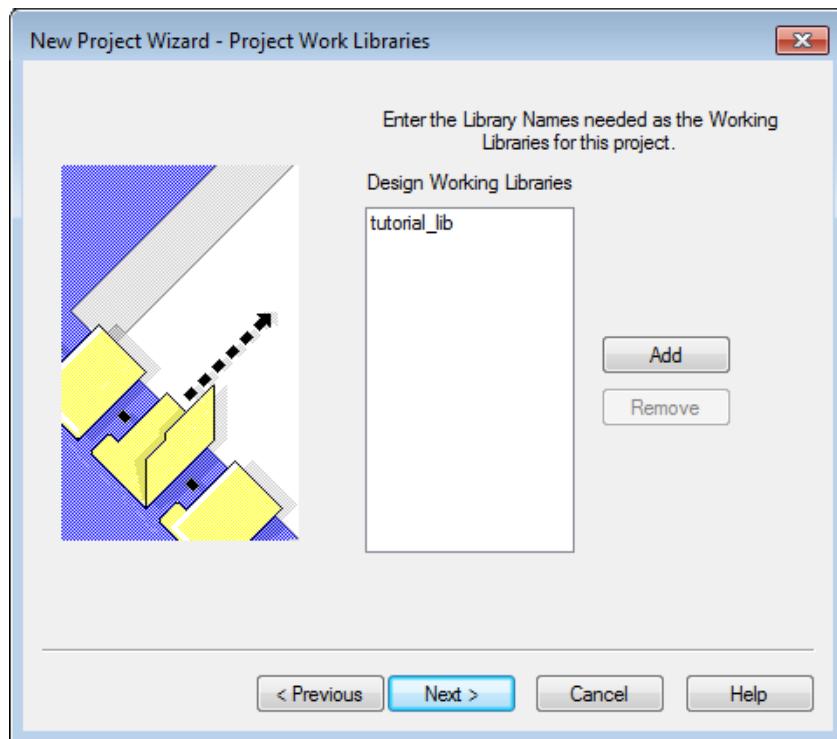


6. Click *Next*.

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The Project Work Libraries page appears.



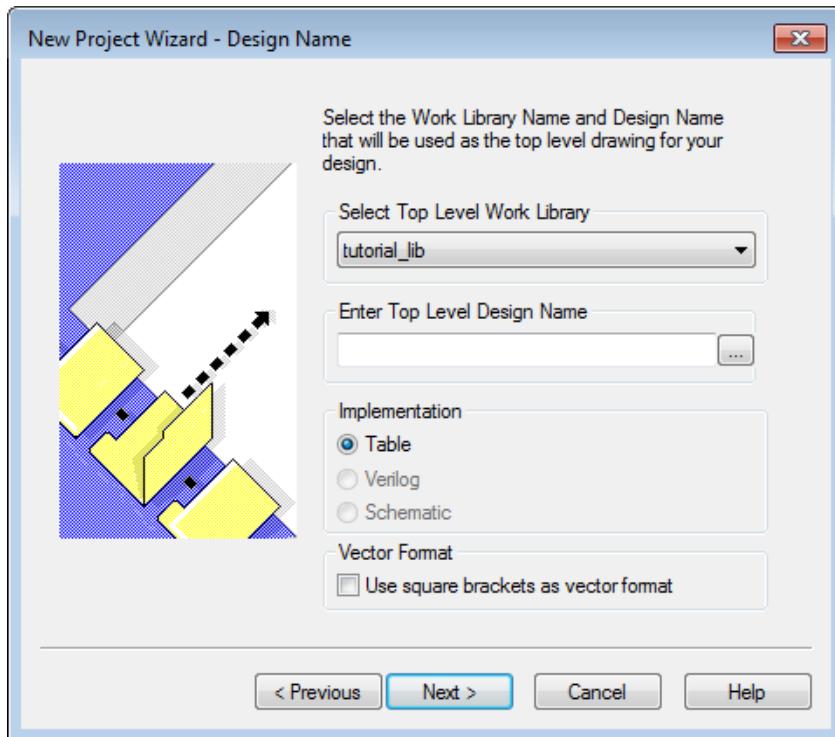
You can specify the working libraries in which the designs created by you will be stored. By default, the New Project Wizard creates a working library named `tutorial_lib` (`<projectname>_lib`). You can click the *Add* button to add more working libraries.

7. Click *Next*.

System Connectivity Manager Tutorial

Module 1: Working with Projects

The Design Name page appears.



Here, you can specify the name of the top-level or root design for the project and select the working library in which you want to create the top-level design.

8. In the *Enter Top Level Design Name* field, enter the top-level design name for the project as follows:

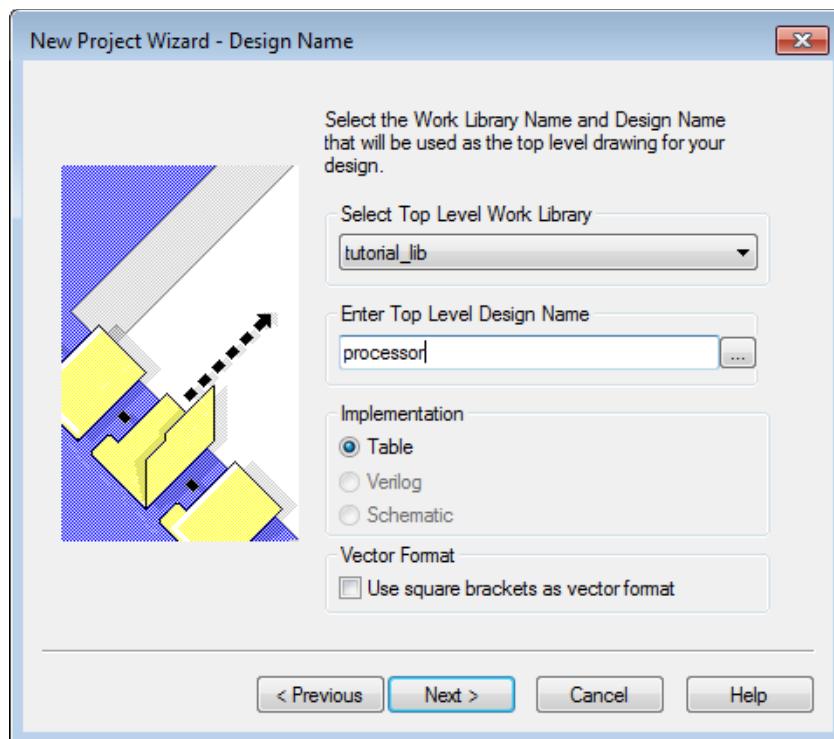
processor

Note: Use only lowercase letters, numbers and the underscore (_) character in design names.

System Connectivity Manager Tutorial

Module 1: Working with Projects

System Connectivity Manager lets you capture the top-level design using spreadsheets as indicated by the Table radio button in the Implementation box.

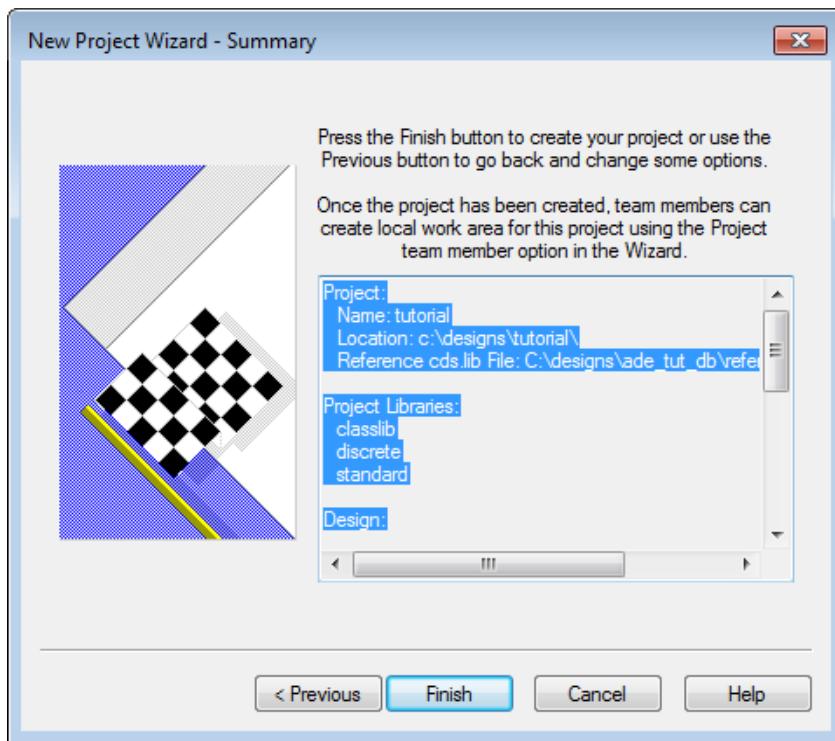


9. Click *Next*.

System Connectivity Manager Tutorial

Module 1: Working with Projects

The Summary page appears.



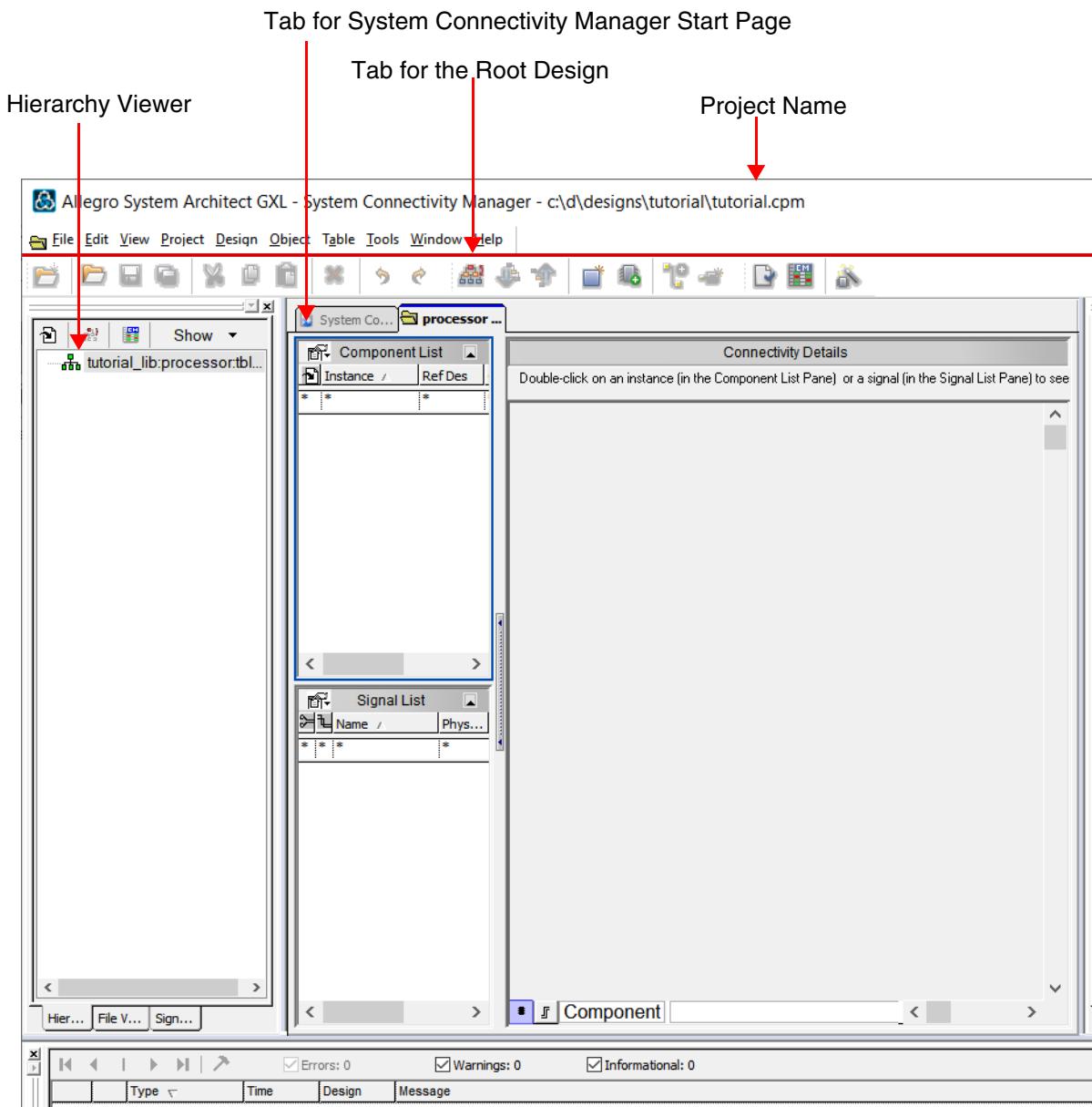
You can review the settings for the project. To modify the settings, you can click *Previous* to go back to a previous page.

10. Click *Finish* to create the project.

After the project is created, a message box reports successful project creation. Click *OK* in the box. The project is automatically opened in System Connectivity Manager.

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Module 1: Working with Projects



The project name and design name are displayed in the System Connectivity Manager title bar.

The Hierarchy Viewer displays the name of the top-level or root design in the `library:cell:view` format as:

..... tutorial_lib:processor:tbl_1

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Module 1: Working with Projects

Where `tutorial_lib` is the working library in which the `processor` design is saved and the `tbl_1` view indicates that the `processor` design is a spreadsheet-based design.

Note that System Connectivity Manager displays the `processor` design in a new tab. You can view the System Connectivity Manager Start page by clicking the tab for the System Connectivity Manager Start page.

You can use the Windows Explorer, UNIX, or Linux terminal window to view the contents of the `tutorial` project directory.

Summary

You now know how to create a project in System Connectivity Manager. You also learned the naming conventions for project names and design names.

For More Information

See the [Working with Projects](#) chapter of *System Connectivity Manager User Guide*.

Lesson 1-3: Setting Up the Project

Overview

After creating your project, you might want to change the default settings for your project. You can use the Setup dialog box to specify the settings for the project.

In this lesson, you will learn to include physical part table (`.ptf`) files for the project.

The Physical Part Table (`.ptf`) file stores the packaging properties for a part in the library. This file contains information about parts such as package types, manufacturers, part numbers and any custom properties. Each physical part must have an entry in the `.ptf` file in order to package properly. Part table files can be located in the `part_table` view of cells in a library or outside the library structure.

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Module 1: Working with Projects

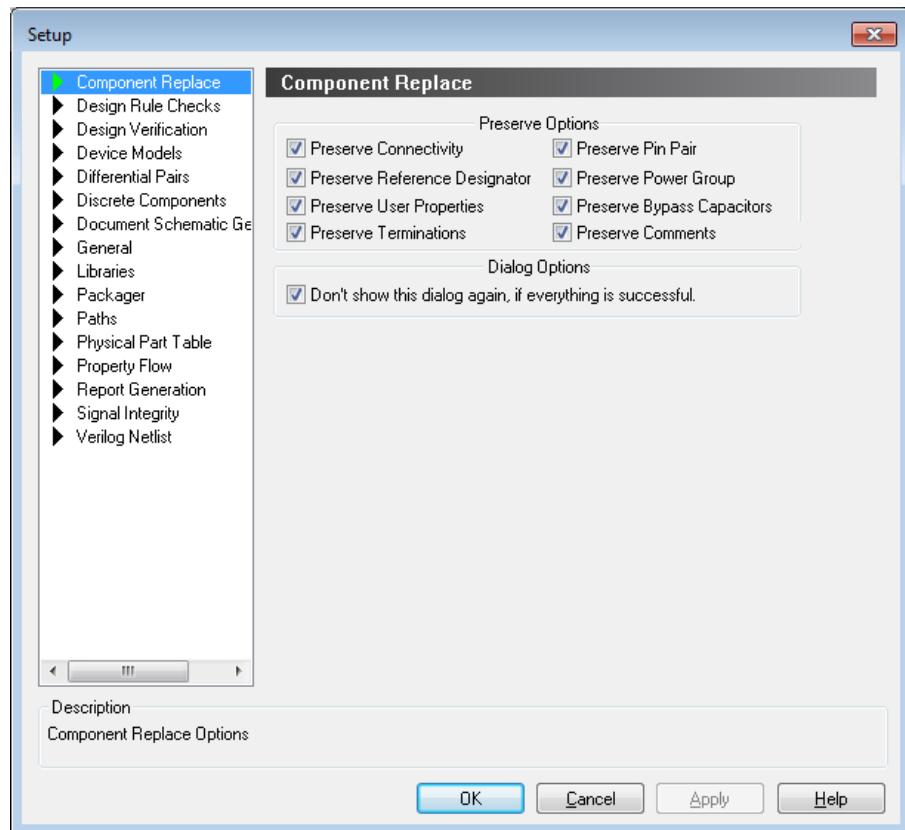
For more information on the structure of part libraries, see [Figure 4-1](#) on page 26.

To access the information contained in part table files, you must include them in your project. By default, the part table files located in the `part_table` view of cells in a library are included in your project. If a part table file is located outside the `part_table` view of cells in a library, you must include the file in your project.

Procedure

1. Choose *Project – Settings*.

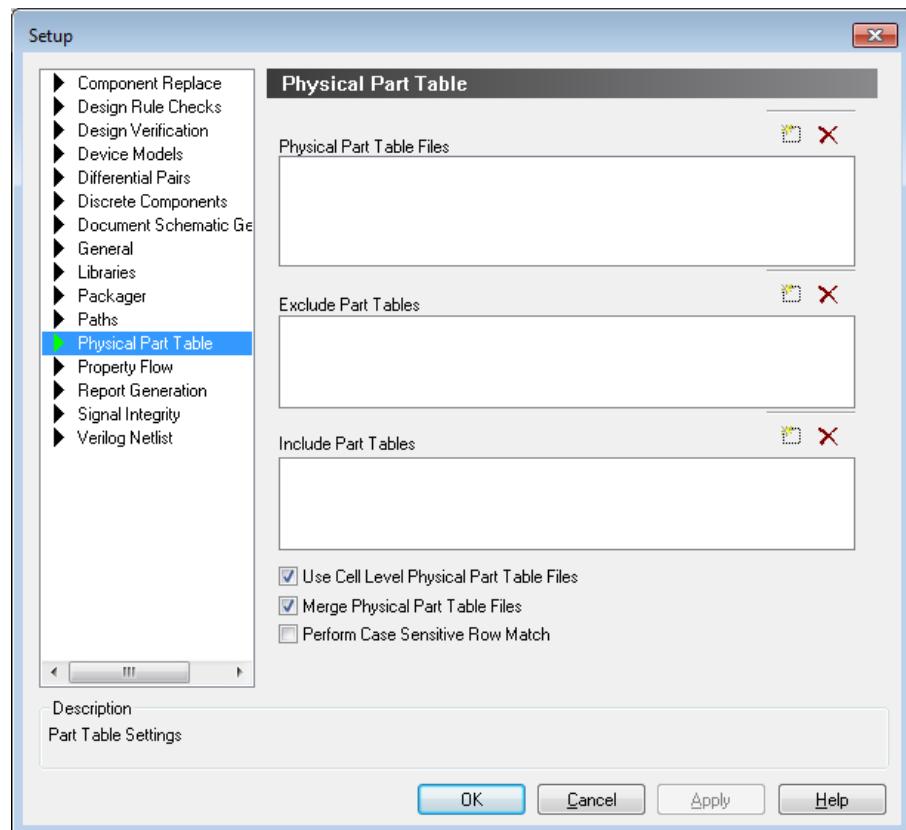
The Setup dialog box appears.



System Connectivity Manager Tutorial

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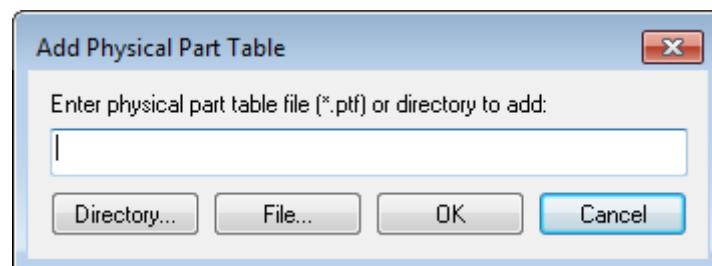
2. Click the *Physical Part Table* tab.



By default, the *Use Cell Level Physical Part Table Files* check box is selected. This indicates that the part table files that are located in the `part_table` view of cells, in the libraries added for your project, are automatically included in the project.

3. Click the add physical part table button () above the *Physical Part Table Files* list.

The Add Physical Part Table dialog box appears.



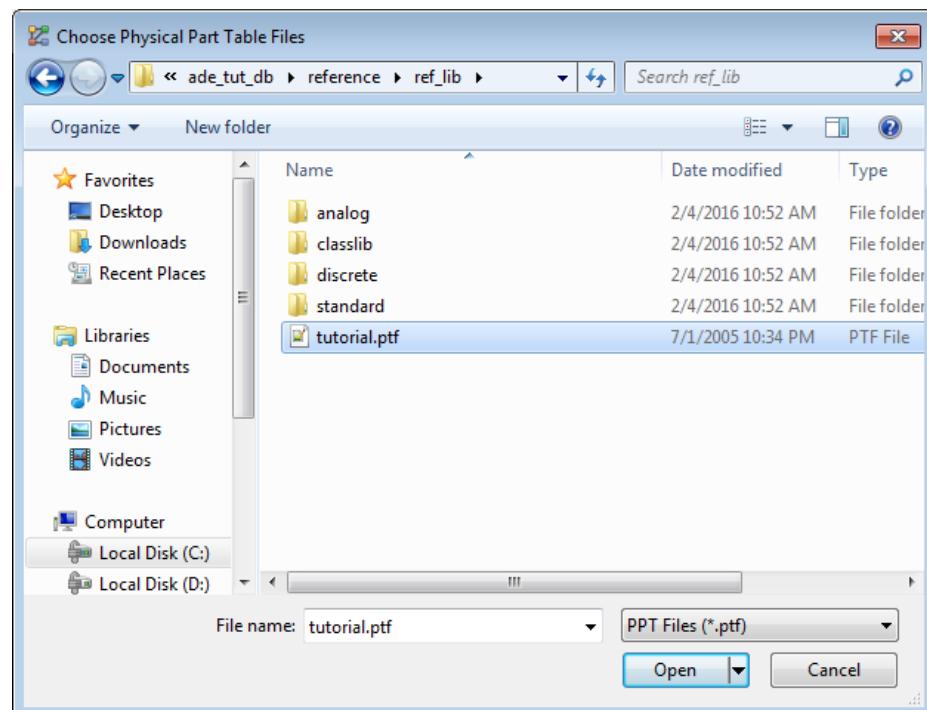
System Connectivity Manager Tutorial

Module 1: Working with Projects

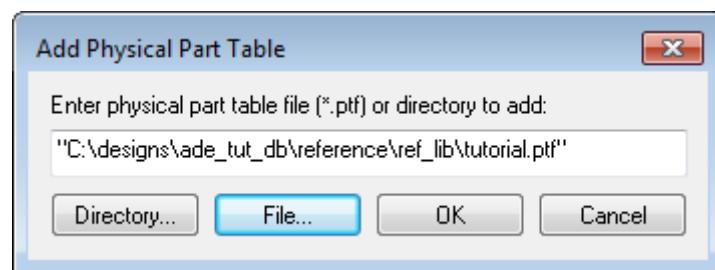
4. Click *File*.

The Choose Physical Part Table Files dialog box appears.

5. Select the `tutorial.ptf` file located at
`<your_work_area>\reference\ref_lib` and click *Open*.



6. The Add Physical Part Table dialog box displays the path to the `tutorial.ptf` file.

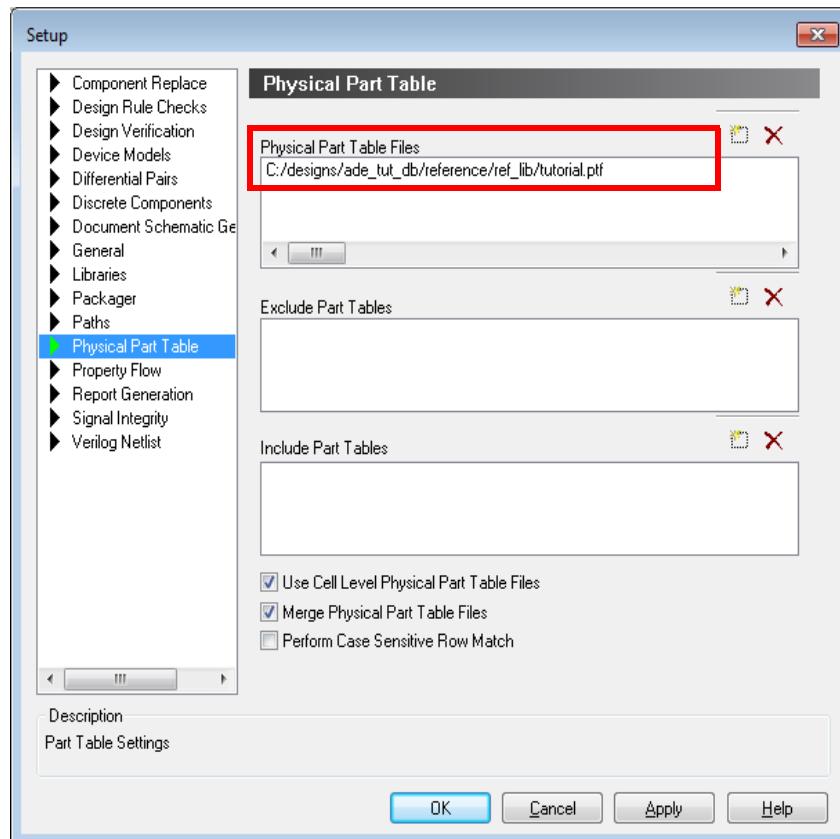


7. Click *OK*.

System Connectivity Manager Tutorial

Module 1: Working with Projects

The *Physical Part Table Files* list in the *Physical Part Table* tab displays the path to the `tutorial.ptf` file.



8. Repeat steps 3 to 7 to add the `mech.ptf` file located at:

`<your_work_area>\reference\cdssetup\`

to the *Physical Part Table Files* list.

The *Include Part Tables* list allows you to specify the part table files listed in the *Physical Part Table Files* list that should be used during packaging.

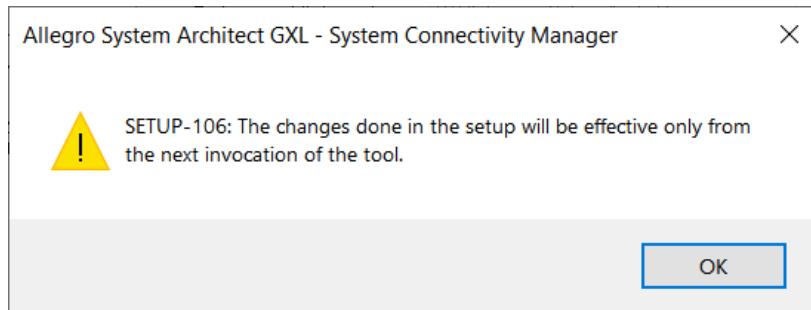
At this point of the tutorial, do not add any files to the *Include Part Tables* list.

9. Click *OK* to close the Setup dialog.

A message is displayed.

System Connectivity Manager Tutorial

Module 1: Working with Projects



10. Click *OK* to save the changes and close the Setup dialog box.

Summary

You now know how to open the Setup dialog box to specify the options for setting up your project. You also learned about physical part table files and how to include them in your project.

For More Information

For more information on physical part table (.ptf) files, see *Allegro Design Entry HDL Libraries Reference*.

Lesson 1-4: Setting Up Libraries for the Project

Overview

You can add only the parts existing in the libraries set up for your project. In this lesson, you will learn to set up libraries for the project.

Before you set up a library for your project, you must define the library in the `cds.lib` file for your project. In this lesson, you will include the library named `analog` in the `cds.lib` file for your project and then set up the library for your project.

System Connectivity Manager Tutorial

Module 1: Working with Projects

Procedure

1. Choose *File – Exit* to close System Connectivity Manager.
2. Open the `cds.lib` file located at
`<your_work_area>\tutorial` in a text editor.

The `cds.lib` file has the following entries:

```
DEFINE tutorial_lib ./tutorial_lib
INCLUDE <your_work_area>/reference/ref_lib/cds.lib
```

The first line defines the working library named `tutorial_lib` and the second line specifies the path to the reference `cds.lib` file located at:

```
<your_work_area>/reference/ref_lib
```

Use the `DEFINE` command to define a library. The library name is specified first, followed by the path to the library directory. The path can be absolute or relative to the location of the `cds.lib` file. Except for the path names, the `cds.lib` file is not case sensitive.

Use the `INCLUDE` command to load another library definition (`cds.lib`) file. For example, you can include a `cds.lib` file that defines a list of company-generated libraries, or you can include the `cds.lib` file being used in another project.

3. Add the following line in the `cds.lib` file:

```
DEFINE analog <your_work_area>/reference/ref_lib/analog
```

This syntax defines the analog library located at
`<your_work_area>/reference/ref_lib/` in the `cds.lib` file.

Note the following:

- ❑ Use lowercase library names only in the `cds.lib` file. Do not use mixed or uppercase names, or special characters except the underscore character.
- ❑ Use forward slashes in paths as they will work on Windows, UNIX and Linux platforms. Backward slashes and absolute paths will need to be modified if the project is transferred between Windows, UNIX and Linux platforms.

4. Start System Connectivity Manager.

System Connectivity Manager Tutorial

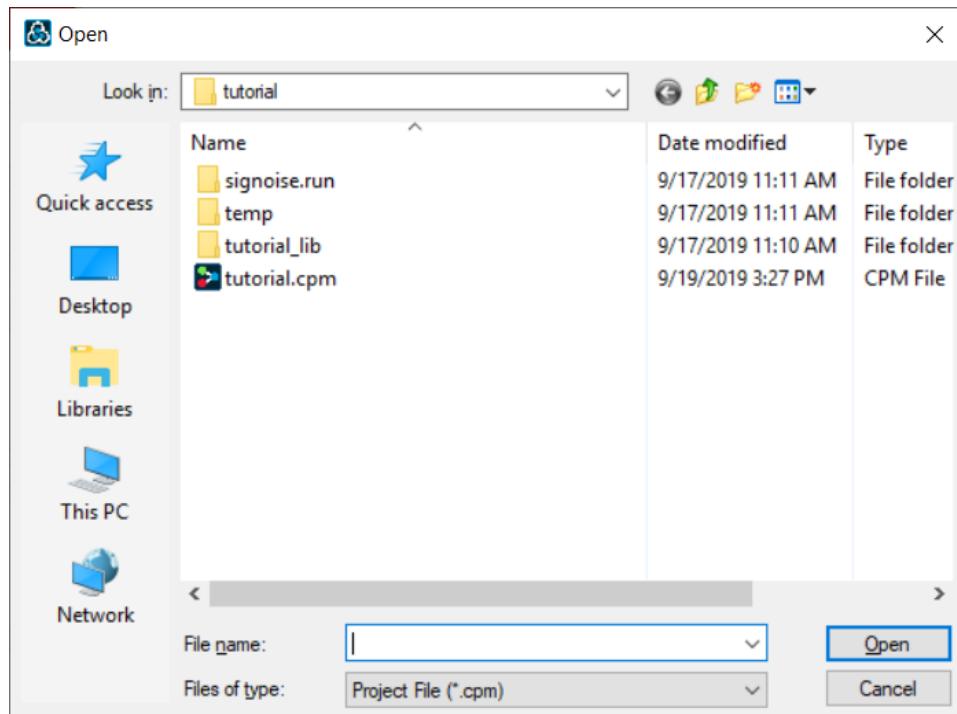
Module 1: Working with Projects

For more information on starting System Connectivity Manager, see [Lesson 1-1: Starting System Connectivity Manager](#) on page 30.

The System Connectivity Manager Start page appears.

5. Click the *Open an Existing Project* icon in the Start page.

The Open dialog box appears.



6. Select the `tutorial.cpm` file located at `<your_work_area>\tutorial\` and click *Open*.

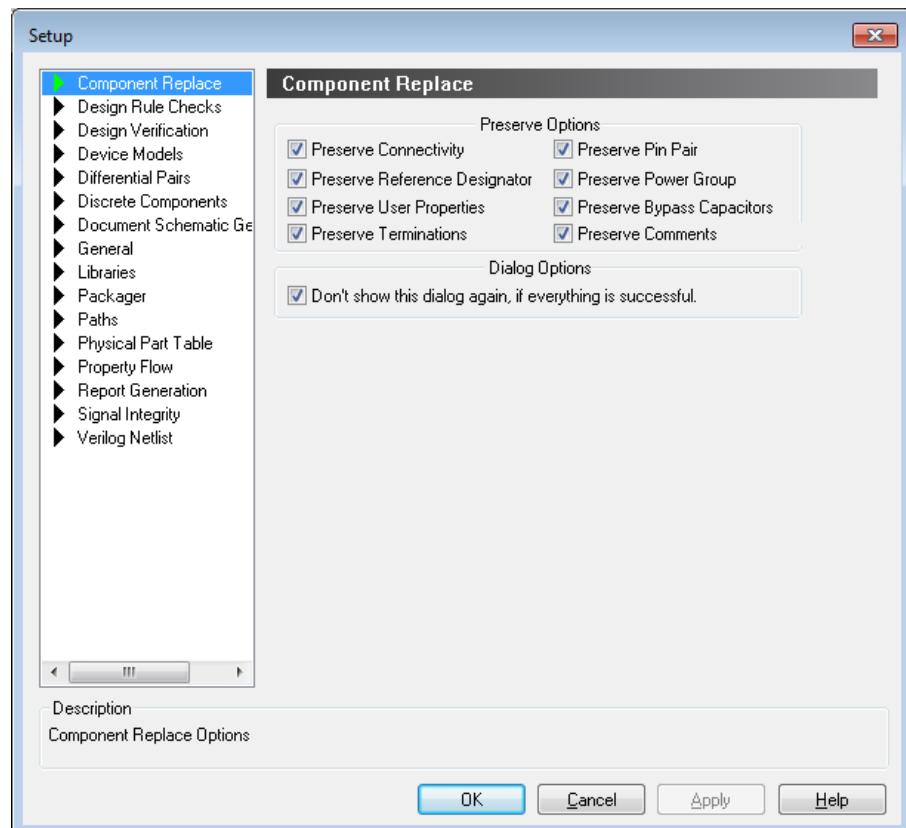
The project is opened in System Connectivity Manager.

7. Choose *Project – Settings*.

System Connectivity Manager Tutorial

Module 1: Working with Projects

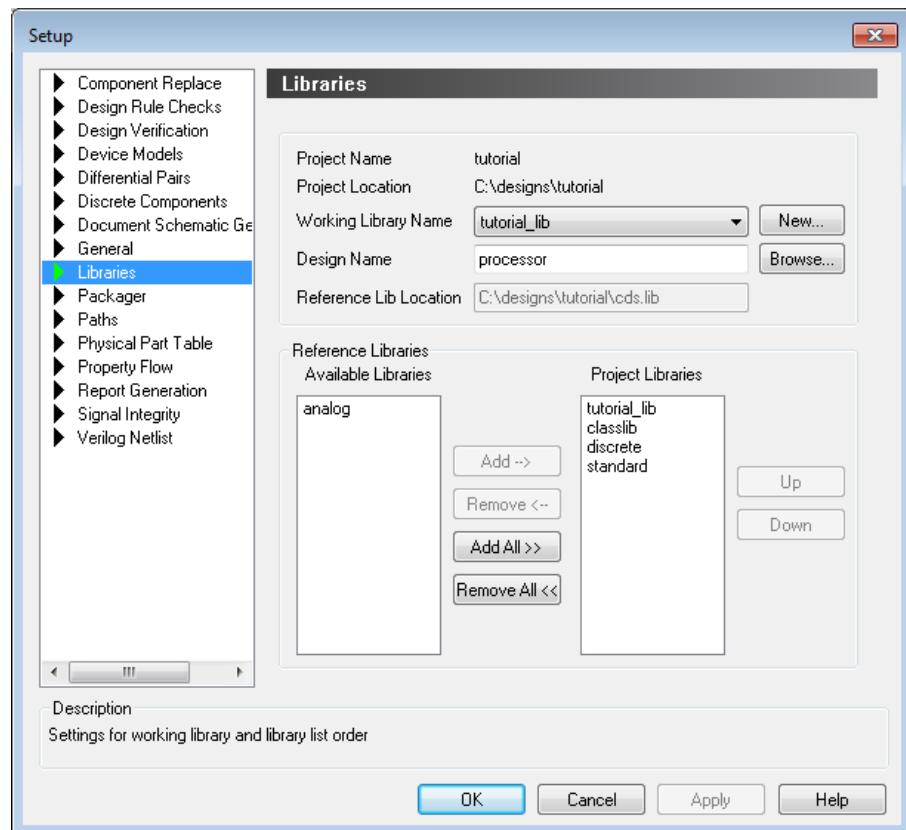
The Setup dialog box appears.



System Connectivity Manager Tutorial

Module 1: Working with Projects

8. Click the *Libraries* tab.

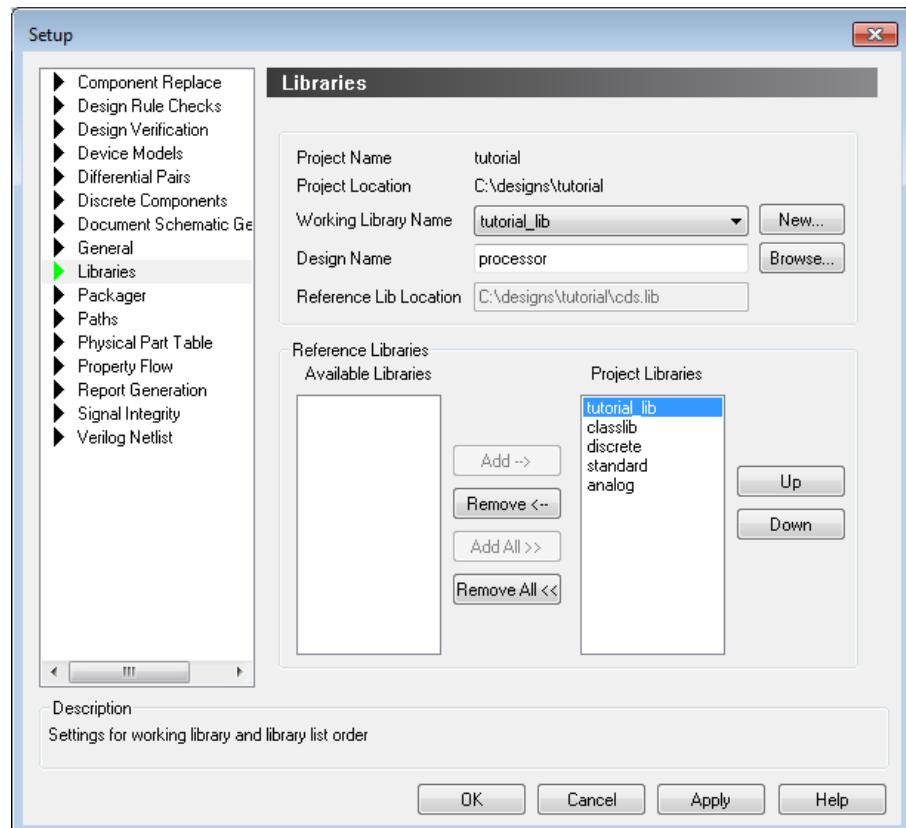


Note that the *analog* library is displayed in the *Available Libraries* list.

System Connectivity Manager Tutorial

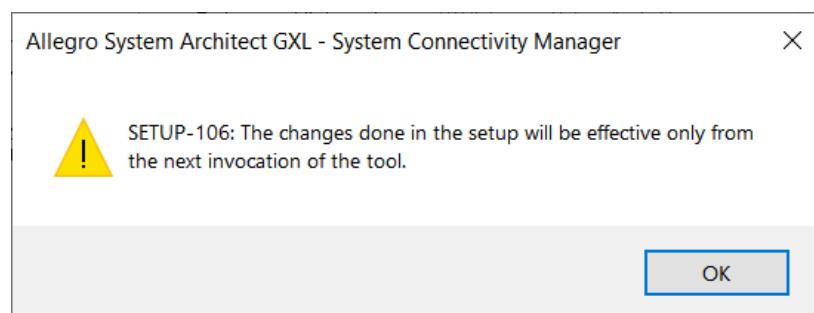
Module 1: Working with Projects

9. Select the analog library and click the *Add* button to add the analog library to the *Project Libraries* list.



10. Click *OK*.

The following message box appears:



Click *OK*.

11. Choose *File – Exit* to close System Connectivity Manager.

System Connectivity Manager Tutorial

Module 1: Working with Projects

12. Start System Connectivity Manager and open the project.

The `analog` library is now set up for the project.

Summary

You now know how to set up libraries for the project. You also learned the following:

- Syntax used in the `cds.lib` file
- How to exit System Connectivity Manager
- How to open a project in System Connectivity Manager

For More Information

For more information on the `cds.lib` file, see the [Allegro Design Entry HDL Libraries Reference](#).

System Connectivity Manager Tutorial

Module 1: Working with Projects

Module 2: Working with Components and Connectivity

Prerequisite

If you have completed all the lessons in [Module 1: Working with Projects](#), open the `tutorial.cpm` project located at
`<your_work_area>\modules\connectivity\tutorial` in System Connectivity Manager and perform the steps described in this module.

For more information, see [Understanding the Sample Design Files](#) on page 16.

Lessons

This module consists of the following lessons:

- [Overview](#) on page 56
- [Lesson 2-1: Adding Components](#) on page 56
- [Lesson 2-2: Adding Signals](#) on page 66
- [Lesson 2-3: Adding Differential Pairs](#) on page 75
- [Lesson 2-4: Capturing Connectivity](#) on page 79
- [Lesson 2-5: Viewing Connectivity in the Design](#) on page 99
- [Lesson 2-6: Adding Comments in the Design](#) on page 105

Multimedia Demonstration

 A Flash-based multimedia demonstration of this module, [Working with Components and Connectivity](#), is available on Cadence Online Support.

Completion Time

3 hours for written lessons

30 minutes for multimedia demonstrations

Overview

After you have created your project and specified the settings for your project, you can proceed with capturing the logic for your design.

One of the primary tasks in design capture involves adding components in the design and capturing the connectivity information for the design by connecting component pins to signals.

The following lessons tell you how to add components in the design and capture connectivity information.

Lesson 2-1: Adding Components

Overview

In this lesson, you will learn to add components in the design in System Connectivity Manager.

You use Part Information Manager to choose components from project libraries and add them in the design. The components added in the design are displayed in the Component List in System Connectivity Manager.

For more information on setting up libraries for your project, see [Lesson 1-4: Setting Up Libraries for the Project](#) on page 45.

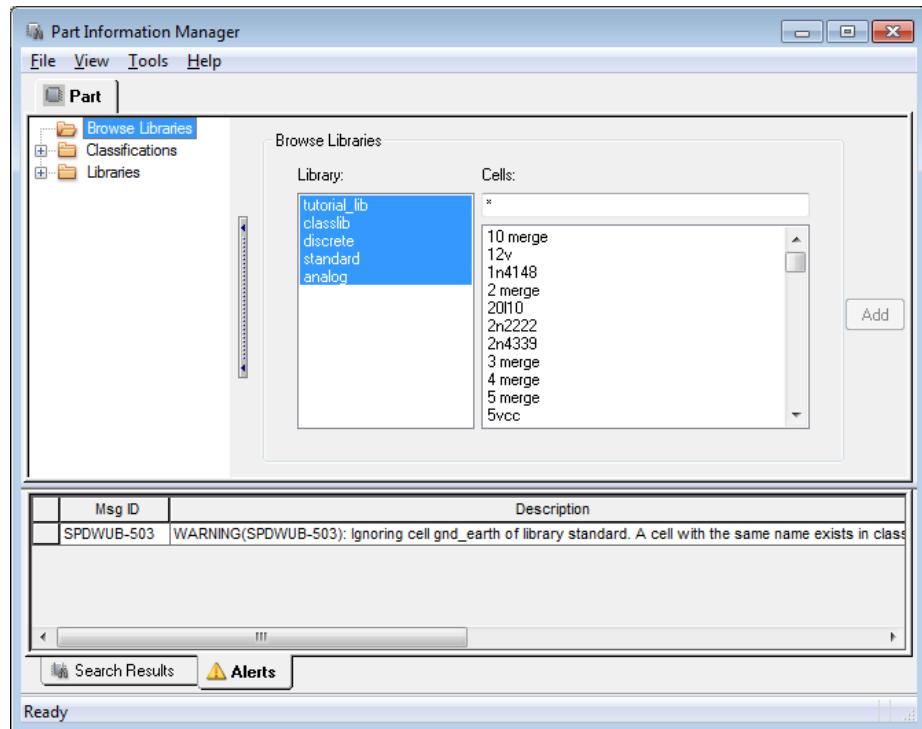
Procedure

1. To open Part Information Manager, do one of the following:
 - Choose *Design – Add Component*.
 - Click the *Add Component* toolbar button ().

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

Part Information Manager appears.

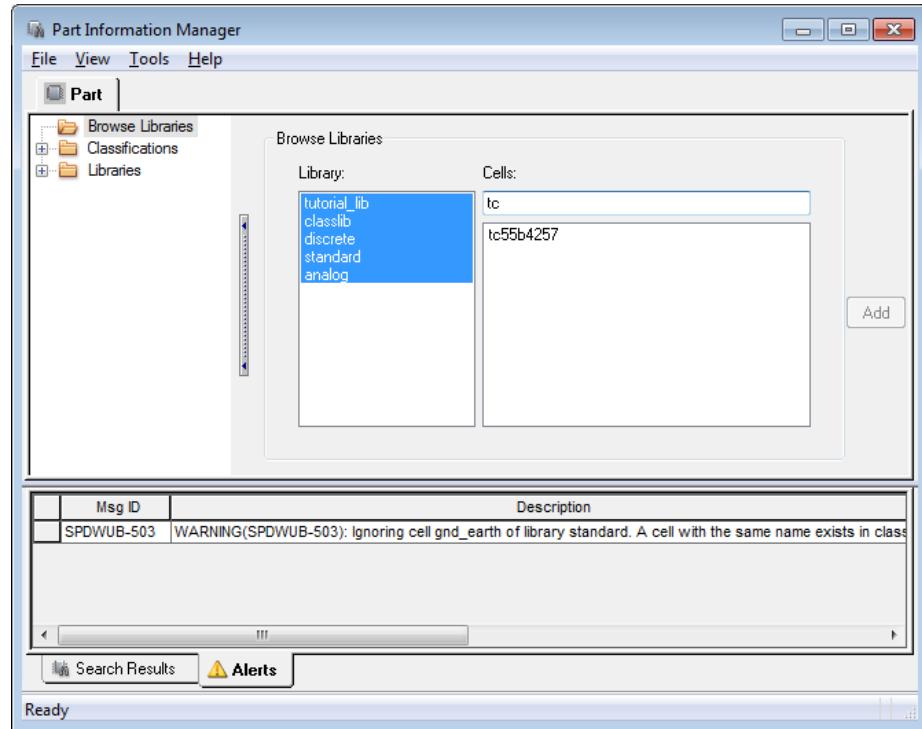


By default, all the libraries are selected and all the cells in the selected libraries are displayed in the *Cells* list. If you know the name of the component you want to add, type it partially in the text box or use wildcards. This will display all matching components in the *Cells* list.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

- Type `tc` in the Cells text box.



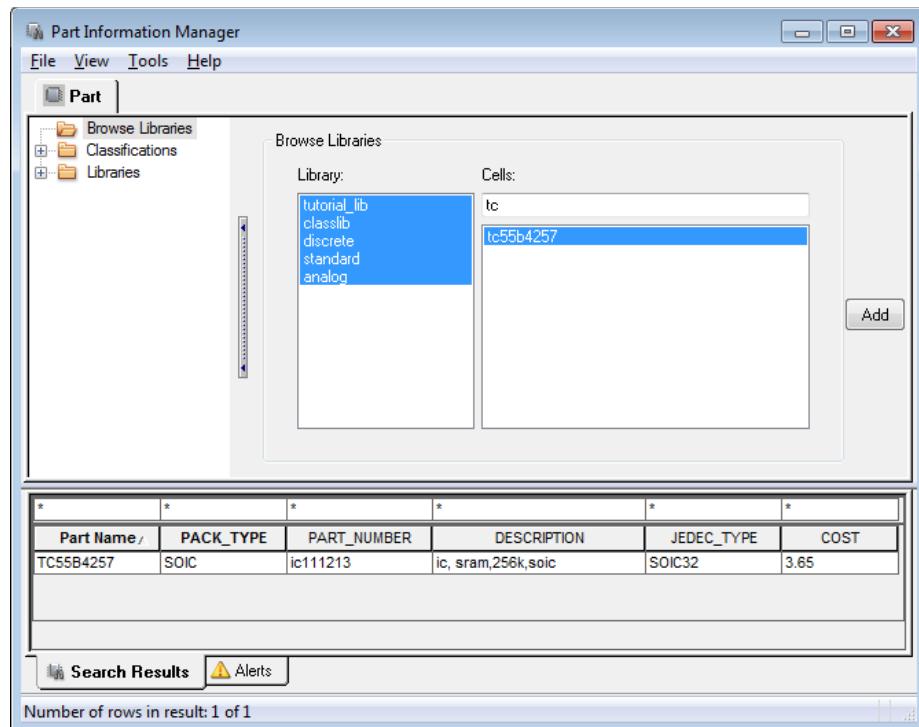
The memory component `tc55b4257` is displayed in the *Cells* list.

- Select the `tc55b4257` component in the *Cells* list.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

Figure 5-1



The part table rows available for the component are displayed in the *Search Results* pane.

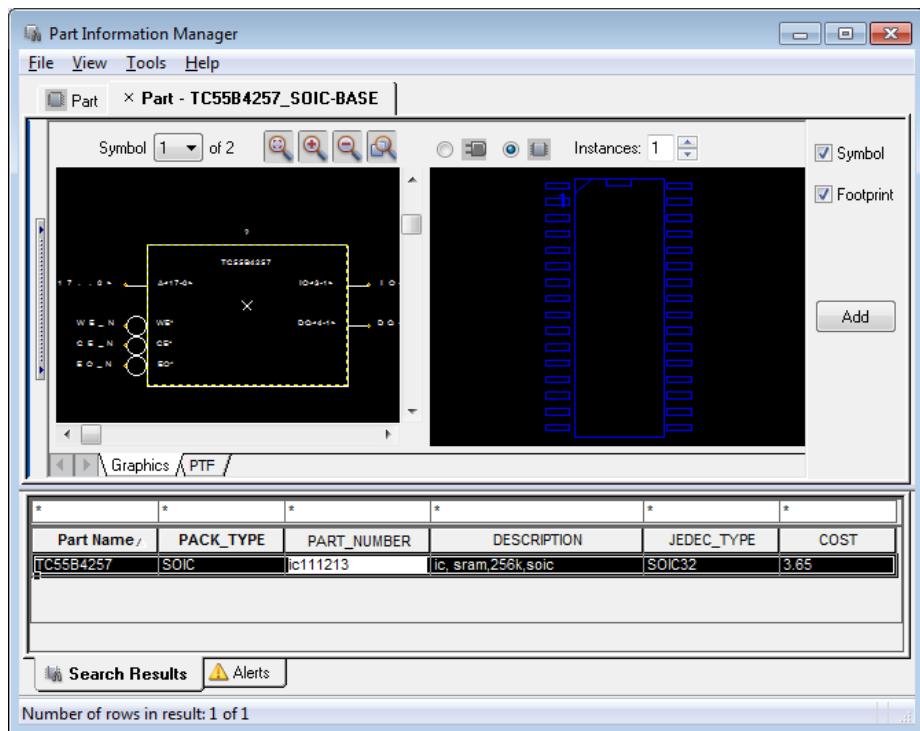
Note: If you place the mouse pointer on a component in the *Cells* list, the library in which the component exists is displayed as a tooltip. In the figure above (, the tooltip indicates that the `tc55b4257` component exists in the `classlib` library.

4. Select the physical part in the *Search Results* pane.

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Module 2: Working with Components and Connectivity

The component details are displayed in a new details tab named *Part TC55B4257_SOIC-BASE*.



The default symbol version for the component is displayed in the symbol viewer. The footprint for the component is displayed in the footprint viewer.

Note: If the footprint for the component is not displayed in the footprint viewer, check whether the `PADPATH` and `PSMPATH` Allegro environment variables are set. For more information, see [Setting Environment Variables](#) on page 17.

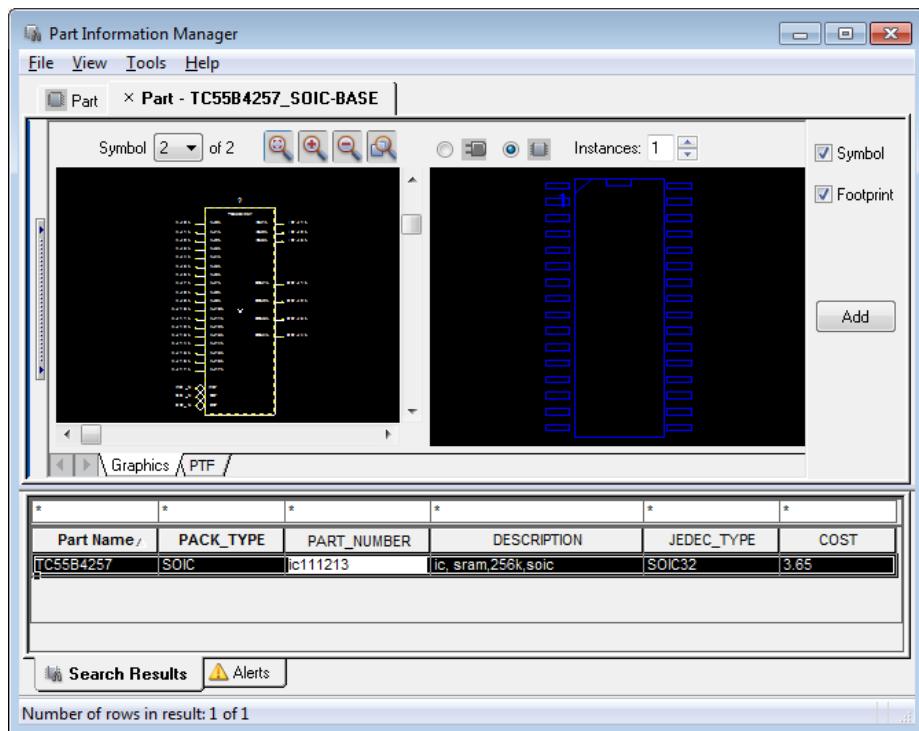
To view a different symbol version, select the version number from the Symbol drop-down list.



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Module 2: Working with Components and Connectivity

5. Select 2 from the Symbol drop-down list to view the second symbol version for the tc55b4257 component.



You can do one of the following:

- ❑ Click to instantiate the tc55b4257 component in the design by adding every symbol version of it. The number of symbols to be instantiated in the design, to make all component pins available, is equal to the number of symbol versions for the component.
- ❑ Click to add the tc55b4257 component as a package (one instance that represents the complete component).

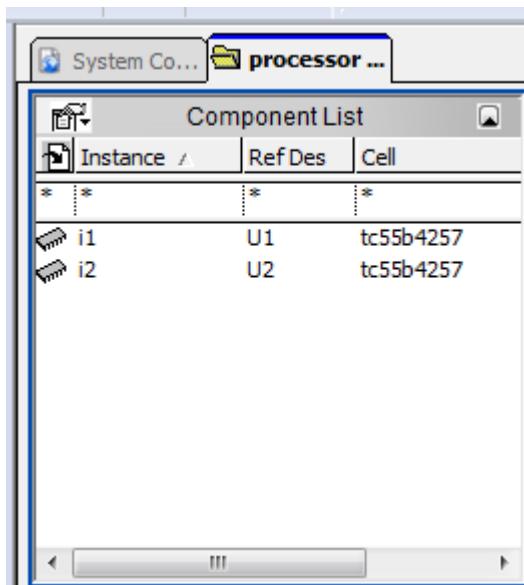
You will now add the tc55b4257 component as a package.

6. Click .
7. Type 2 in the *Instances* field.
8. Click the *Add* button.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

Two instances of the tc55b4257 component are added in the design and displayed in the Component List in System Connectivity Manager.



The screenshot shows a software interface titled "System Co... processor ...". A tab labeled "processor ..." is selected. Below it is a "Component List" window. The table has three columns: "Instance", "Ref Des", and "Cell". There are two rows of data:

| Instance | Ref Des | Cell |
|----------|---------|-----------|
| * | * | * |
| i1 | U1 | tc55b4257 |
| i2 | U2 | tc55b4257 |

The Component List lets you work with the components in the design. Each row in the Component List corresponds to a component in the current design.

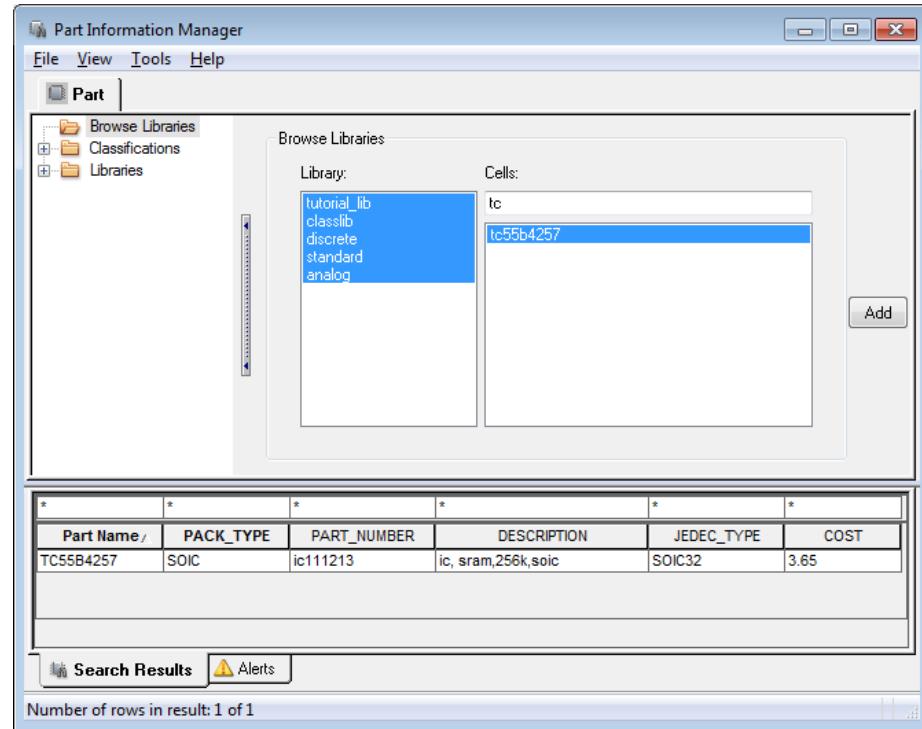
When you add a component in the design, System Connectivity Manager automatically packages the component and assigns a reference designator to the component. System Connectivity Manager also assigns an instance name to the component. In the figure above, note that the tc55b4257 components displayed in the Component List have been assigned the reference designators U1 and U2 and the instance names i1 and i2.

Note: You can modify the instance name and reference designator of the component.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

9. Click the *Part* tab in Part Information Manager.

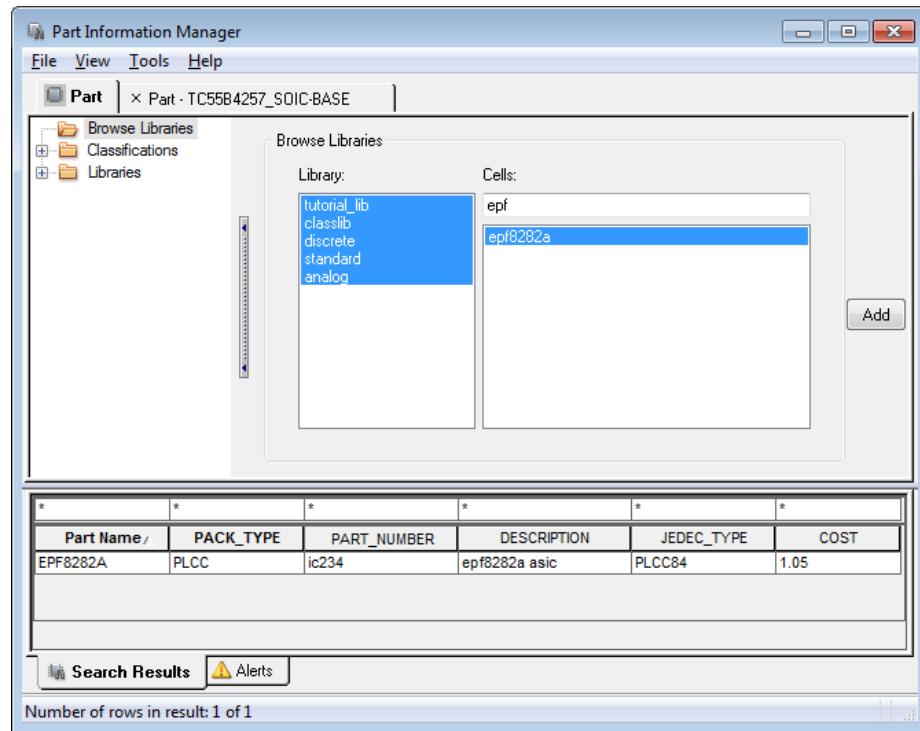


10. Type `epf` in the text box.

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Module 2: Working with Components and Connectivity

The FPGA component `epf8282a` is displayed in the *Cells* list.



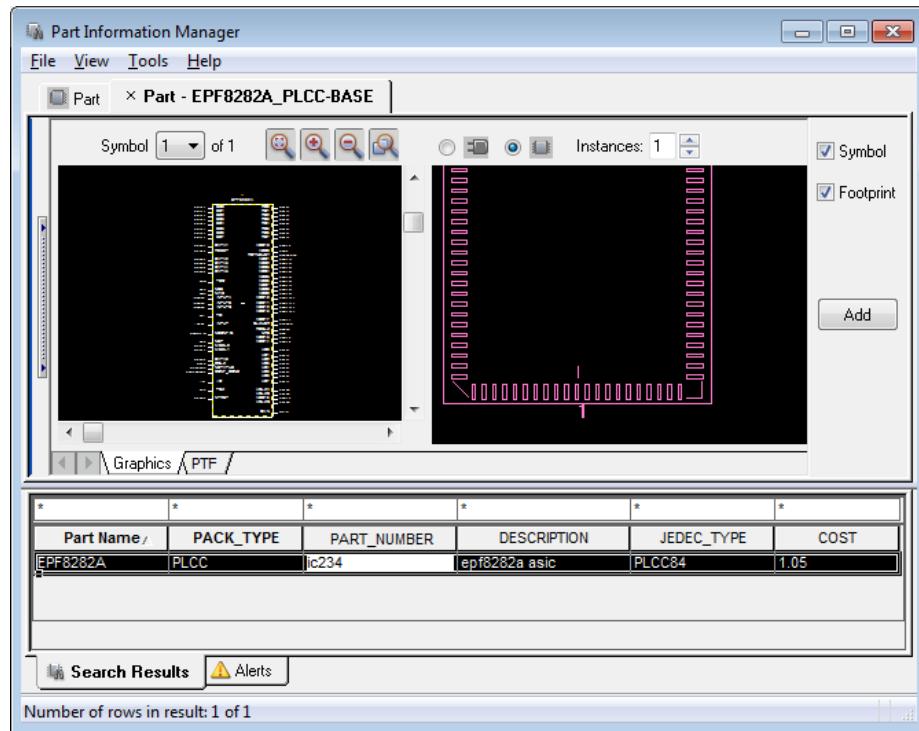
11. Select the `epf8282a` component in the *Cells* list.
12. Select the physical part in the *Search Results* pane.

The component details are displayed in a new tab named *Part EPF8282A_PLCC-BASE*.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

Enter 1 in the *Instances* field.



13. Click *Add*.

The epf8282a component is added in the design and displayed in the Component List.

14. Close Part Information Manager.

15. Choose *File – Save* to save the design.

Summary

You now know how to use Part Information Manager to add components in the design. You also learned the following:

- You can add a symbol version of the component or add the component as a package (one instance that represents the complete component).
- System Connectivity Manager automatically packages the components you add in your design and assigns a reference designator to the components.

For More Information

See the [Working with Components](#) chapter of *System Connectivity Manager User Guide*.

Lesson 2-2: Adding Signals

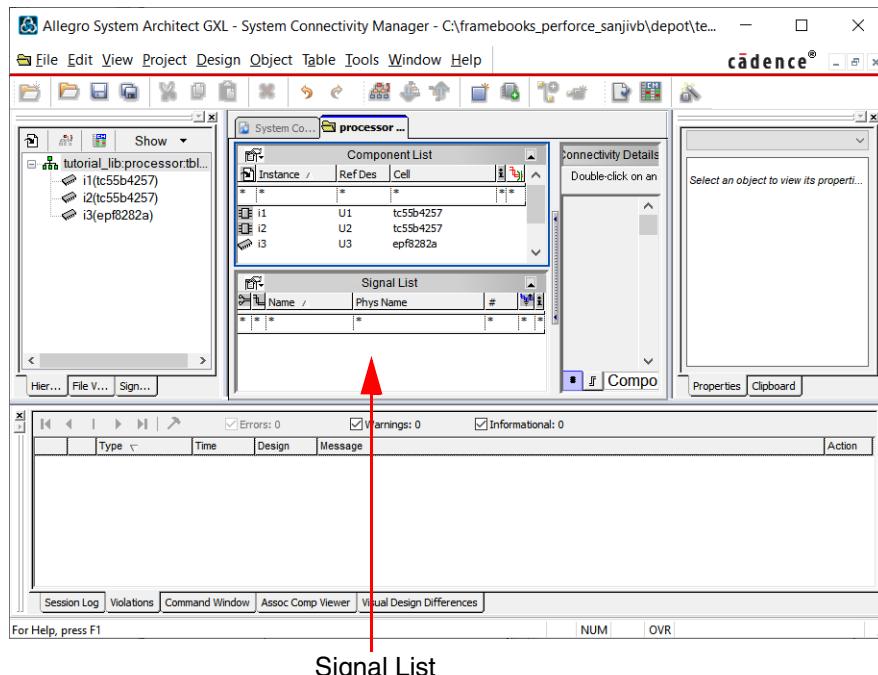
Overview

The Signal List in System Connectivity Manager lets you work with signals in the design.

In this lesson, you will learn to use the Signal List to add signals in the design.

Procedure

1. Click on the Signal List pane.

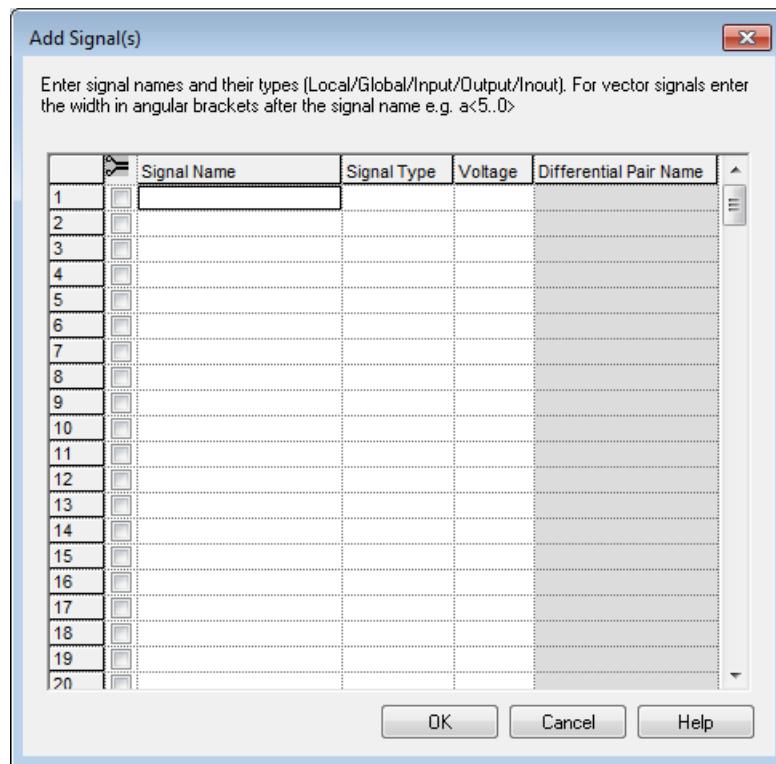


2. Choose *Design – Add Signal*.

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Module 2: Working with Components and Connectivity

The Add Signal(s) dialog box appears.



In this dialog box, you can specify the signal name, its scope and voltage. The scope of a signal can be LOCAL, GLOBAL, IN, OUT or INOUT.. Voltage is required to identify DC nets in the design.

DC nets are required for connecting to associated components (terminations, bypass capacitors and pullup/pulldown) in the design. For more information on working with associated components, see [Module 3: Working with Associated Components](#) on page 109.

3. In the *Signal Name* field, enter:

VCC

4. In the *Signal Type* field, select the scope of the VCC signal as *Global*.

Global signals are used to make sure that voltage signals with the same name in different blocks in a hierarchical design are connected together.

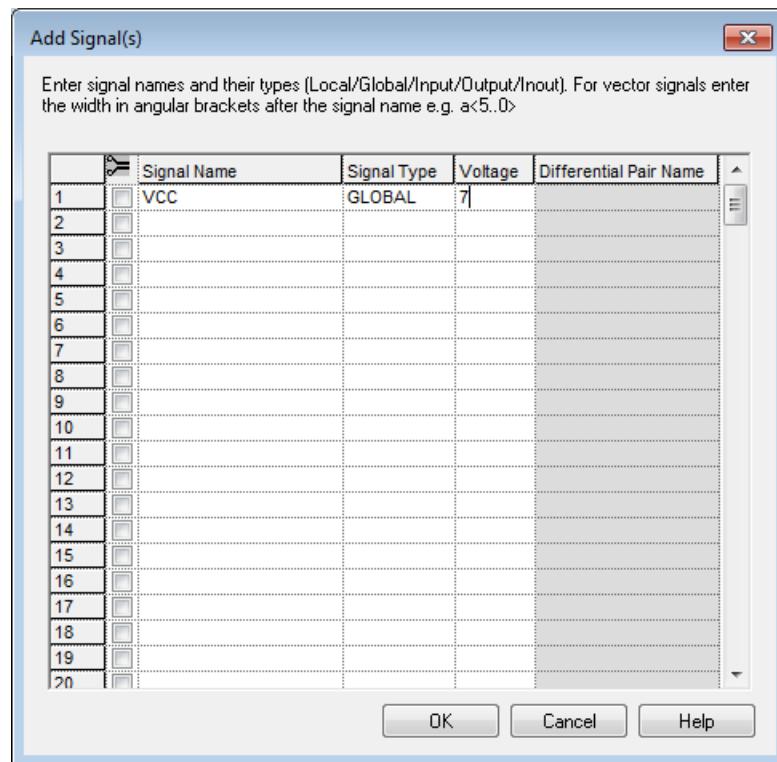
5. In the *Voltage* field, enter the voltage for the VCC signal as:

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

7

This completes the definition for the VCC signal.



Note: The default unit for voltage is Volts. If you want to specify the voltage in millivolts, say, 75 mV, enter the voltage as:

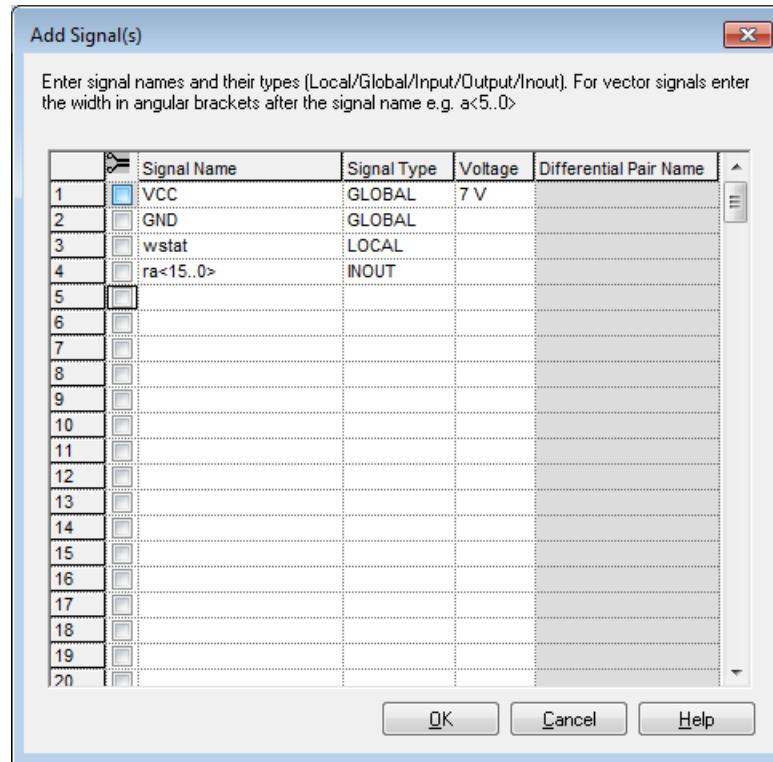
0.075

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Module 2: Working with Components and Connectivity

6. Define the following signals:

| Signal Name | Signal Type | Voltage |
|-------------|-------------|---------|
| GND | GLOBAL | 0 |
| wstat | LOCAL | |
| ra<15..0> | INOUT | |



The signal `wstat` is a **LOCAL** signal. A local signal is a signal that is unique to a design. Local signals that have the same name in different designs will not be connected.

The signal `ra<15..0>` is a vectored signal. A vectored signal name indicates multiple bits on the same signal. You must separate the vector or bit range with two periods (..) and enclose it in angle brackets (< >). The bit order is `<MSB..LSB>` where `MSB` is the most significant bit and `LSB` is the least significant bit of the signal.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

7. Click **OK** to add the signals in the design.
8. The signals are displayed in the Signal List. The icons in the *Type Icon* column in the Signal List indicate the scope of the signals.

| Name / | Phys Name | # | |
|---------------|-----------|---|--|
| ✉ G VCC | VCC | 0 | |
| ✉ G GND | GND | 0 | |
| ✉ L wstat | WSTAT | 0 | |
| ✉ I ra<15..0> | RA | 0 | |

For example, the  icon next to the VCC signal indicates that VCC is a global signal. The  icon next to the ra<15..0> signal indicates that ra<15..0> is an INOUT signal.

The Signal List lets you work with the signals in the design. It displays the list of signals in the design. Each row in the Signal List corresponds to a signal.

When you add a signal in the design, System Connectivity Manager automatically assigns a physical net name for the signal.

The *Conn* column in the Signal List displays the total number of component pins connected to each signal. The value 0 in the *Conn* column indicates that the signals are not connected to pins in the design. When you connect a signal to pins in the design, the value in the *Conn* column is automatically updated for the signal.

Note: You can modify the default column to view a different column.

9. You can also add signals by using the right-click option in the Signal List.

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Module 2: Working with Components and Connectivity

- a. Click in the Signal List.
- b. Right-click and select *Add Signal*.

The Add Signal(s) dialog is displayed.

- c. Enter the signal name as:

bnc1

- d. Click *OK*.

The bnc1 signal is added as a local signal in the Signal List.

| Name / | Phys Name | # |
|--------|-----------|---|
| VCC | VCC | 0 |
| GND | GND | 0 |
| WSTAT | WSTAT | 0 |
| RA | RA | 0 |
| bnc1 | BNC1 | 0 |

10. Another way to add signals in the design is to add pre-defined signals in the design.

You can use the *Design – Save Signals To File* command to export the signals (and their voltage values, if any) in a design to a signal (.sig) file. You can then load the signal file into another design using the *Design – Load Predefined Signals* command. This lets you quickly add signals (along with their voltage values, if any) in other designs.

- a. Choose *Design – Load Predefined Signals*.

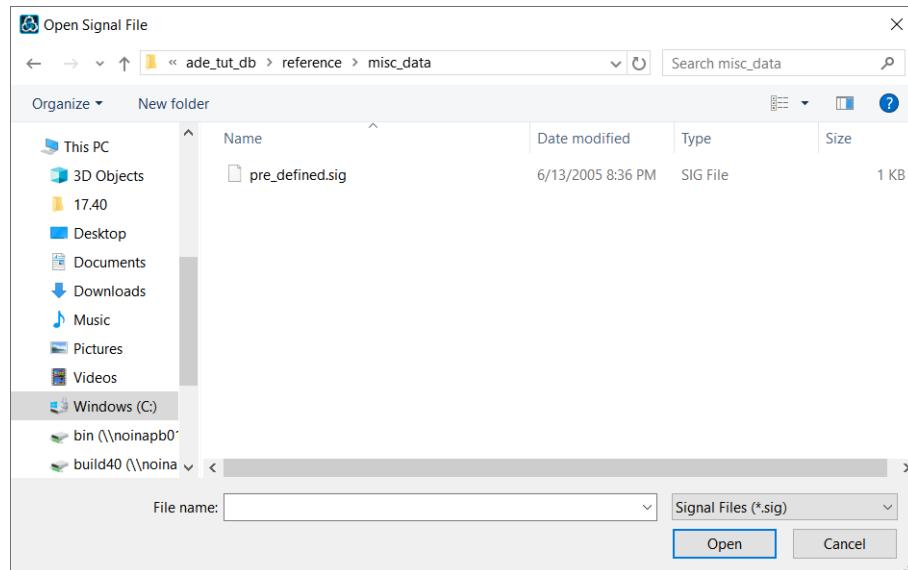
The Open Signal File dialog box appears.

- b. Select the `pre_defined.sig` located at:

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<your_work_area>\ade_tut_db\reference\misc_data



11. Click Open.

The following signals are automatically added in the Signal List.

brd
bwr
breset

| Name | Phys Name | # |
|-----------|-----------|---|
| VCC | VCC | 0 |
| GND | GND | 0 |
| wstat | WSTAT | 0 |
| ra<15..0> | RA | 0 |
| bnc1 | BNC1 | 0 |
| brd | BRD | 0 |
| bwr | BWR | 0 |
| breset | BRESET | 0 |

12. You can modify the signal name, the physical net name, the scope of the signal, and its voltage in the Signal List. You will now modify the scope of the `ra<15 .. 0>` signal from `INOUT` to `INPUT`.

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Module 2: Working with Components and Connectivity

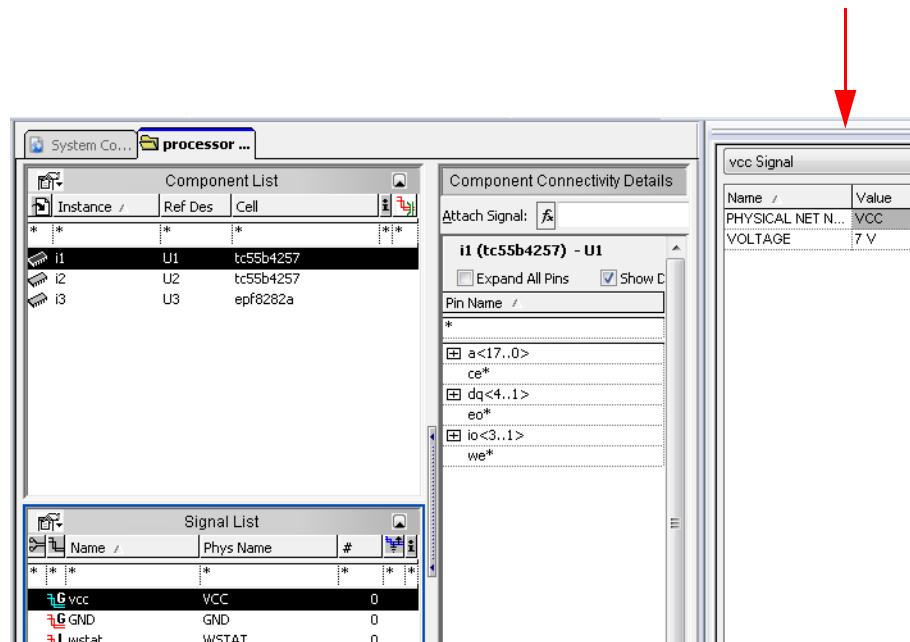
- a. Select the `ra<15..0>` signal in the Signal List.
- b. Choose *Object – Change – Signal Scope – Input*.

The scope of the `ra<15..0>` signal is displayed as  in the Type Icon column. This icon indicates an INPUT signal.

13. You will now change the voltage of the VCC signal from 7 V to 5 V.

- a. Select the VCC signal in the Signal List.
- b. Choose *View – Properties Window*.

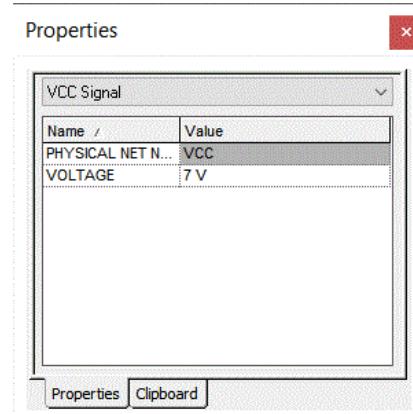
A new tab appears next to the Component Connectivity Details tab.



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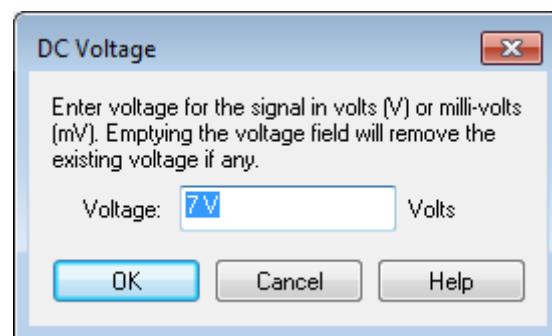
Module 2: Working with Components and Connectivity

It displays the property VOLTAGE with the value 7 V.



- c. Select the VOLTAGE property with the value 7 V.
- d. Choose *Object – Change – DC Voltage*.

The DC Voltage dialog box appears.



- e. Enter 5 in the Voltage field.
- f. Click *OK*.
- g. Click on the VCC signal in the Signal List.

The Properties tab now displays the value of the VOLTAGE property as 5 V.

14. Choose *File – Save* to save the design.

Summary

You now know how to add signals in the design using the Add Signal(s) dialog box and the Signal List. You also learned,

- how to load a predefined list of signals from a file.
- the syntax to be used when adding vectored signals.
- that System Connectivity Manager automatically assigns physical net names to the signals you add in the design.
- how to change the scope and voltage of signals.

For More Information

See the [Capturing Connectivity](#) chapter of *System Connectivity Manager User Guide*.

Lesson 2-3: Adding Differential Pairs

Overview

In the previous lessons, you learnt how to add components and signals to your design in System Connectivity Manager. In this lesson, you will learn how System Connectivity Manager can be used to identify and create user-defined differential pairs. You will also add differential pair signals to your design.

System Connectivity Manager uses a special icon () to indicate differential pairs in the Component Connectivity Details and Signal List panes.

The setup options provided in System Connectivity Manager are used to ensure that model-defined as well as user-defined differential pairs are listed in the Component Connectivity Details pane.

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Module 2: Working with Components and Connectivity

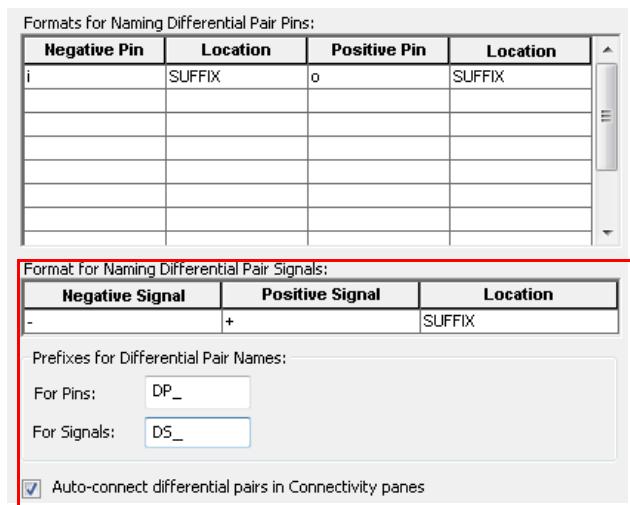
Procedure

Adding User-Defined Differential Pairs

1. Choose *Project – Settings*.
 2. Select *Differential Pairs*.
 3. In the *Format for Naming Differential Pair Pins* grid, specify the following:

| Negative Pin | Location | Positive Pin | Location |
|---------------------|-----------------|---------------------|-----------------|
| i | SUFFIX | o | SUFFIX |

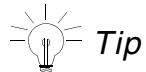
- To ensure that the name of the differential pair for pins starts with DP_, enter DP_ in the *Prefixes for Differential Pair Names For Pins* text box.
 - In the *Prefixes for Differential Pair Names For Signals* text box, enter DS_.



- ## 6. Click OK.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

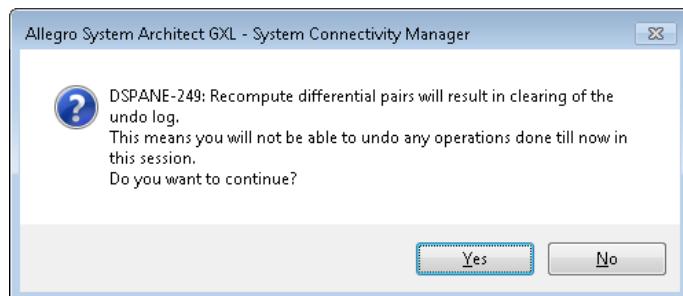


Tip

In case the differential pair pins on components used in your design use multiple naming formats, you should enter all the formats in the *Format for Naming Differential Pair Pins* grid. This will ensure that all the pins that satisfy a format are identified as a user-defined differential pair in the Component Connectivity Details pane.

7. Choose *File – Exit* to close System Connectivity Manager.
8. Start System Connectivity Manager and open the project.
9. In the Components List pane, select instance i3, that is, epf8282a.
10. Right-click and from the pop-up menu, choose *Recompute Differential Pairs*.

A message box appears with the information that the undo log will be cleared and that you will not be able to undo any previous action after this step. Click *Yes* in the box.



Pins that satisfy the criteria are listed as differential pairs in the Component Connectivity Details pane.

| Component Connectivity Details | | | | |
|--|---|--|--------|-------------|
| Attach Signal: <input type="text"/> | | | | |
| i3 (epf8282a) - U3 | | | | |
| <input type="checkbox"/> Expand All Pins | <input checked="" type="checkbox"/> Show Differential Pairs | <input checked="" type="checkbox"/> Show Vectors | | |
| Pin Name | Pin Number | Pin Type | Signal | Termination |
| * | * | * | * | * |
| DP_td | 27,73 | Input | | |
| + tdo | 27 | Input | | |
| - tdi | 73 | Input | | |
| + bd<7..0> | 18,19,20,21,22,2... | Input | | |
| data1 | 13 | Input | | |
| reset | 15 | Input | | |
| data2 | 9 | Input | | |



Differential pairs cannot be created using power pins, even if the power pins follow the naming format listed in the Format for Naming Differential Pair Pins grid.

Adding Differential Pair Signals

1. Click in the Signal List box.
2. Choose *Design – Add Signal*.

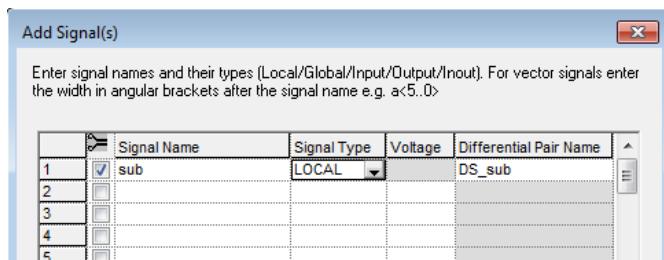
The Add Signal(s) dialog box appears.

3. Click the *Differential Pair* check box in the column headed by the icon: ().

The Differential Pair Name column is enabled.

4. Specify the signal name as `sub` and the type as `LOCAL`.

Note that the default name in the Differential Pair Name column, `DS_sub`, is generated using the prefix value specified by you in the setup dialog box for differential pair signals.



5. Click *OK*.

The differential pair is added to the design and is visible in the Signal List pane.

Summary

You now know how to add differential pair signals and user-defined differential pair of pins to your design. You also learnt how to use the

differential pair setup options to identify user-defined differential pairs.

For More Information

See the following:

- [Working with Differential Pairs](#) chapter of *System Connectivity Manager User Guide*.
- [Project Creation and Setup](#) chapter of *System Connectivity Manager User Guide*.

Lesson 2-4: Capturing Connectivity

Overview

The previous lessons showed you how to add components and signals in the design. In this lesson, you will learn how to capture the connectivity information for the design by connecting component pins to signals.

The Component Connectivity Details pane (CCP) in System Connectivity Manager provides a spreadsheet-based interface to quickly add pin-signal connectivity, apply terminations, pullups and pulldowns, and assign signal integrity models to component pins.

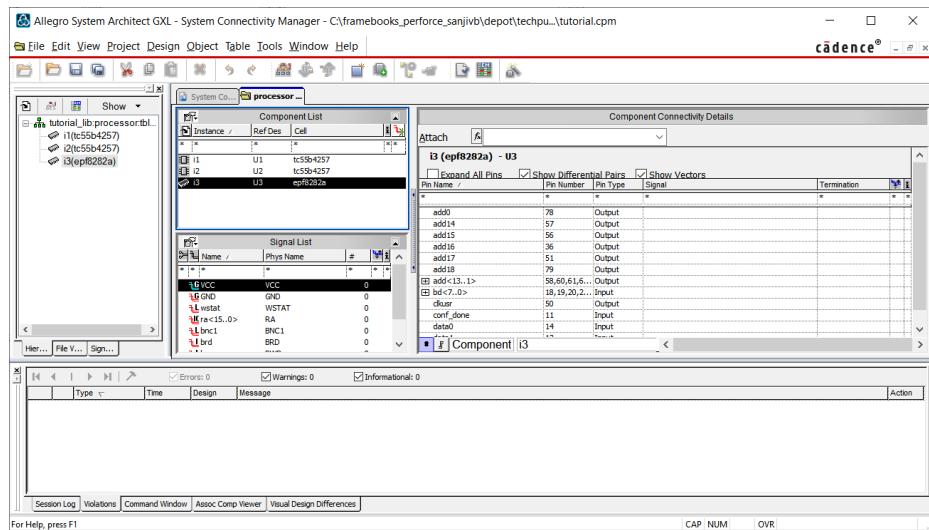
We will discuss different ways to quickly interconnect a design.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

Procedure

1. Click the `epf8282a` component in the Component List to display the Component Connectivity Details pane.



2. In the *Signal* cell next to the pin `data1`, type the signal name: `sel`

| Pin Name | Pin Number | Pin Type | Signal |
|------------|---------------|----------|--------|
| * | * | * | * |
| add0 | 78 | Output | |
| add14 | 57 | Output | |
| add15 | 56 | Output | |
| add16 | 36 | Output | |
| add17 | 51 | Output | |
| add18 | 79 | Output | |
| add<13..1> | 58,60,61,6... | Output | |
| bd<7..0> | 18,19,20,2... | Input | |
| clkusr | 50 | Output | |
| conf_done | 11 | Input | |
| data0 | 14 | Input | |
| data1 | 13 | Input | sel |
| data2 | 9 | Input | |
| data3 | 8 | Input | |

3. Press *Enter* or click in another cell.

The pin `data1` is connected to the signal `sel`.

Note that the signal `sel` is automatically added in the Signal List because a signal with the same name does not exist in the

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design. The *Conn* column in the Signal List indicates that the signal `sel` has one connection in the design.

| Name / | Phys Name | # | Conn |
|-----------|-----------|---|------|
| VCC | VCC | 0 | |
| GND | GND | 0 | |
| wstat | WSTAT | 0 | |
| ra<15..0> | RA | 0 | |
| bnc1 | BNC1 | 0 | |
| brd | BRD | 0 | |
| bwr | BWR | 0 | |
| breset | BRESET | 0 | |
| sel | SEL | 1 | |

4. In the Signal cell next to the pin `inputa`, type:

`brd`

| Pin Name / | Pin Number | Pin Type | Signal |
|------------|---------------|----------|--------|
| * | * | * | * |
| add0 | 78 | Output | |
| add14 | 57 | Output | |
| add15 | 56 | Output | |
| add16 | 36 | Output | |
| add17 | 51 | Output | |
| add18 | 79 | Output | |
| add<13..1> | 58,60,61,6... | Output | |
| bd<7..0> | 18,19,20,2... | Input | |
| clkusr | 50 | Output | |
| conf_done | 11 | Input | |
| data0 | 14 | Input | |
| data1 | 13 | Input | sel |
| data2 | 9 | Input | |
| data3 | 8 | Input | |
| data4 | 7 | Input | |
| data5 | 6 | Input | |
| dclk | 10 | Input | |
| gain | 28 | Output | |
| i/o | 16 | Input | |
| inputa | 55 | Input | brd |
| inputb | 54 | Input | |
| inputc | 12 | Input | |

The signal name auto completes to `brd`.

System Connectivity Manager auto completes signal names when you type them in the *Signal* column in the Component Connectivity Details pane.

5. Press *Enter* or click in another cell.

The pin `inputa` is connected to the signal `brd`.

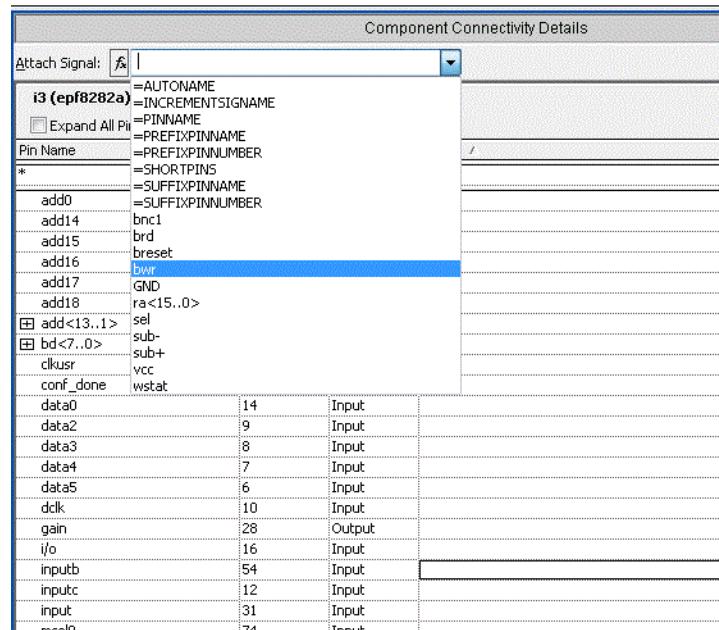
6. If you want to pick signal names from the Signal List in the design, you can select a pin in the Component Connectivity

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Module 2: Working with Components and Connectivity

Details pane or select the *Signal* cell next to a pin and then select a signal from the Attach Signal drop-down list.

- a. Click in the *Signal* cell next to the pin `inputb`.
- b. Click the *Attach Signal* drop-down list and choose the `bwr` signal.



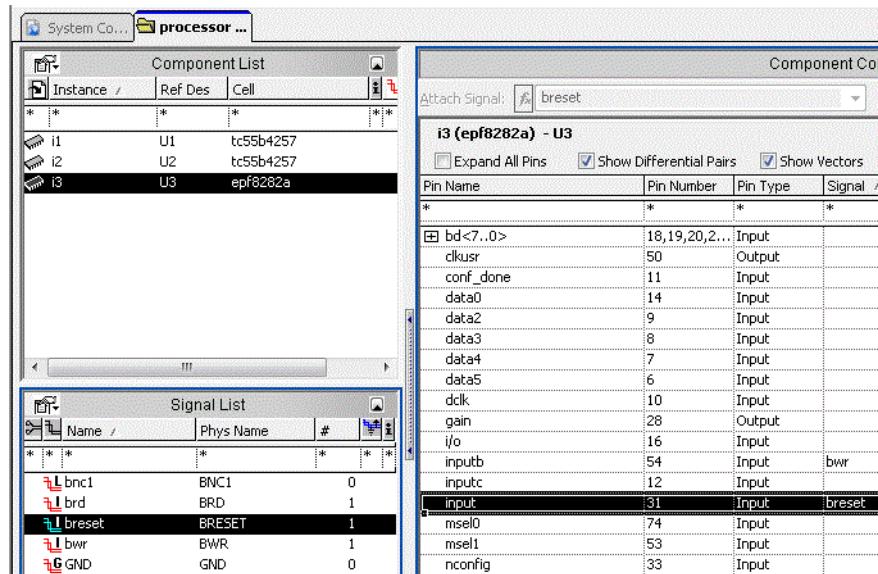
The pin `inputb` is connected to the `bwr` signal.

7. Another way to add connectivity is to select a signal in the Signal List and drag and drop the signal on a pin in the Component Connectivity Details pane.

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Module 2: Working with Components and Connectivity

- a. Select the breset signal in the Signal List.
- b. Keeping the left-mouse button pressed, drag and drop the signal on the pin `inputc` in the Component Connectivity Details pane.



The pin `inputc` is connected to the `breset` signal.

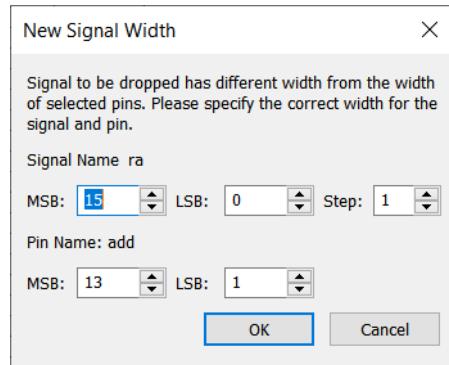
If you drag and drop a vectored signal that has a different width from the size of the pin, the New Signal Width dialog box appears. Specify the bits of the signal you want to connect to the pin.

- a. Select the `ra<15..0>` signal in the Signal List.
- b. Keeping the left-mouse button pressed, drag and drop the signal on the vector pin `add<13..1>` in the Component Connectivity Details pane.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

The New Signal Width dialog box appears.



- c. Specify the MSB (most significant bit) for the `ra<15..0>` signal as 12 and the LSB (least significant bit) for the signal as 0.

This indicates that the bits 0 to 12 of the `ra<15..0>` signal will be connected to the pin `add<13..1>`.

- d. Click *OK* to connect the pin to the signal.

Note: You can click the expand button () next to the `add<13..1>` pin or select the *Expand All Pins* check box to view the connectivity of each bit of the vector pin.

8. Another way to connect a pin to a signal is to enter the signal name in the *Signal* cell next to the pin.

Click in the *Signal* cell next to the pin `bd<7..0>` and type:

`rd<7..0>`

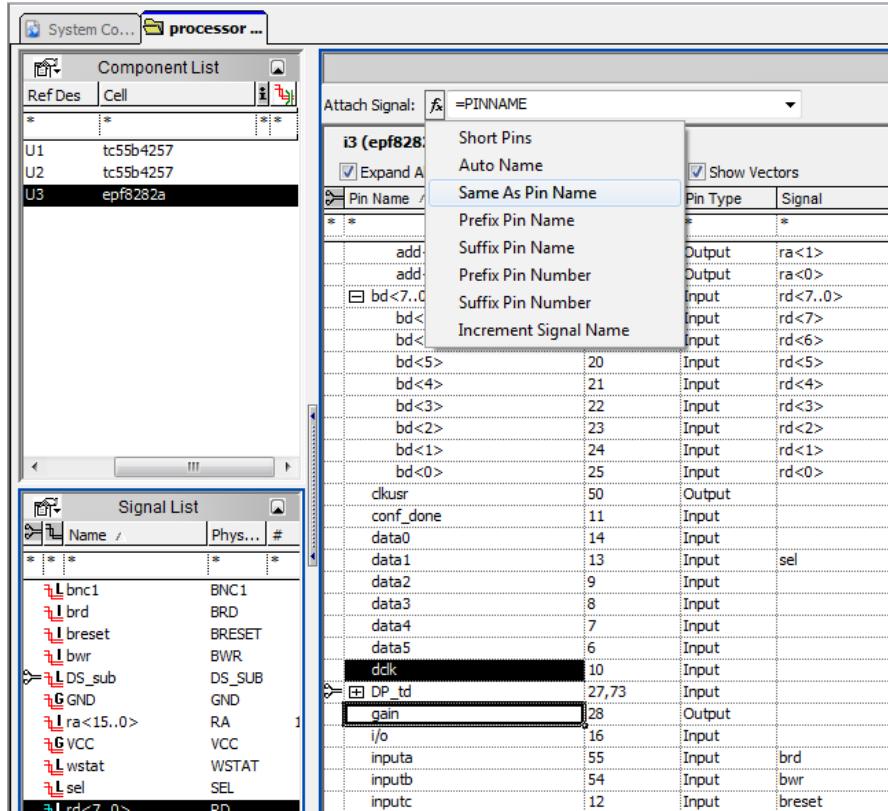
The pin `bd<7..0>` is connected to the signal `rd<7..0>`.

You can also use functions to automatically generate the signal names for pins.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

- a. Select the pins `dclk` and `gain` or select the *Signal* cells next to the pins.
- b. Click the *Function selector* button () and choose *Same as Pin Name* to generate signal names that have the same name as the pin names.



9. You can use filters to view only those pins on which you want to view or edit connectivity.

- a. Type `vd*` in the *Pin Name* column filter and press *Enter* to view only those pin names that start with the name `vd`.

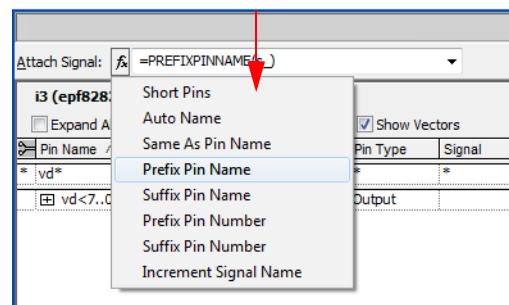
| Pin Name | Pin Number | Pin Type | Signal |
|----------|---------------|----------|--------|
| * vd* | * | * | * |
| vd<7..0> | 46,45,44,4... | Output | |

- b. Select the pin `vd<7..0>`.

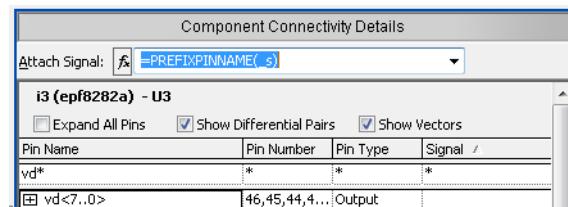
System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

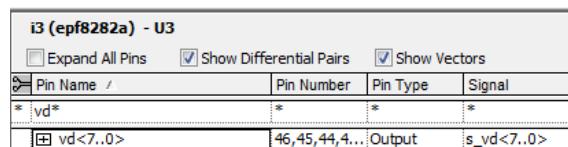
- c. Click the *Function selector* button () and choose *Prefix Pin Name*.



- d. Type the prefix as `s_` and press *Enter*.



The pin `vd<7..0>` is connected to the `s_vd<7..0>` signal.



- e. Type `*` in the *Pin Name* column filter and press *Enter* to view all the pins of the `epf8282a` component.

10. By default, vectored signals are displayed in the Signal List. Displaying the bits of a vectored signal in the Signal List lets you quickly connect bits of the vectored signal to component pins.

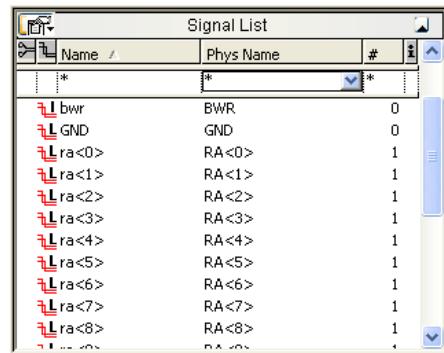
System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

- a. Click the Expand button in the Signal List and deselect *Show Buses*.



The bits of vectored signal $ra<15..0>$ are displayed in the Signal List.



- b. Select the bit $ra<13>$ in the Expanded Signal List.
- c. Keeping the left-mouse button pressed, drag and drop the signal on the pin $r_{dynbusy}$ in the Component Connectivity Details pane.

The pin $r_{dynbusy}$ is connected to the bit $ra<13>$ of the vectored signal $ra<15..0>$.

- d. Click and select *Show Buses*.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

The vectored signals in the design are now displayed in a non-expanded format.

| Name / | Phys Name | # |
|------------|-----------|----|
| breset | BRESET | 1 |
| bwr | BWR | 1 |
| GND | GND | 0 |
| ra<15..0> | RA | 14 |
| rd<7..0> | RD | 8 |
| s_vd<7..0> | S_VD | 8 |
| sel | SEL | 1 |
| sub+ | SUB+ | 0 |
| sub- | SUB- | 0 |
| Gvcc | VCC | 0 |
| wstat | WSTAT | 0 |

11. You can view and edit the connectivity for more than one component at the same time. This helps you quickly capture connectivity information on components that require similar connectivity.
 - a. Select the two instances of the `tc55b4257` component in the Component List.

| Pin Number | Signal |
|--------------------------|--------|
| * | * |
| 12,13,14,15,18,19,20,... | |
| 6 | |
| 26,23,10,7 | |
| 27 | |
| 17,16,1 | |
| 11 | |

- b. Choose *Object – Edit Connectivity*.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

A multiselect Component Connectivity Details pane for both the instances with one Pin Name column and two Signal columns is displayed.

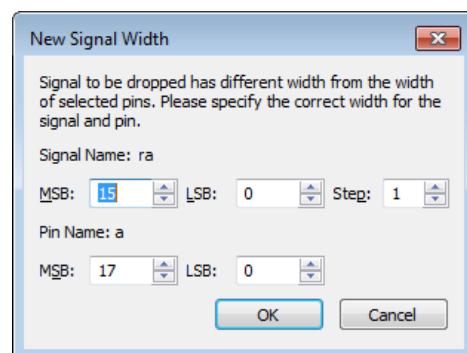
| Component Connectivity Details | | | |
|--|---------------------------------|---------------------|--------|
| Attach Signal: <input type="button" value="fx"/> | | | |
| i1 (tc55b4257) - U1 | | i2 (tc55b4257) - U2 | |
| Pin Name | Pin Number | Signal | Signal |
| * | * | * | * |
| <input checked="" type="checkbox"/> a<17..0> | 12, 13, 14, 15, 18, 19, 20, ... | | |
| <input checked="" type="checkbox"/> ce* | 6 | | |
| <input checked="" type="checkbox"/> dq<4..1> | 26, 23, 10, 7 | | |
| <input checked="" type="checkbox"/> eo* | 27 | | |
| <input checked="" type="checkbox"/> io<3..1> | 17, 16, 1 | | |
| <input checked="" type="checkbox"/> we* | 11 | | |

- c. Press the *Ctrl* key and click in the *Signal* cells next to the pin a<17..0>.

| Pin Name | Signal | Signal |
|--|--------|--------|
| * | * | * |
| <input checked="" type="checkbox"/> a<17..0> | | |
| ce* | | |
| dq<4..1> | | |
| eo* | | |
| io<3..1> | | |
| we* | | |

- d. Select the ra<15..0> signal in the Signal List.
e. Keeping the left-mouse button pressed, drag and drop the signal on the pin a<17..0> in the Component Connectivity Details pane.

The New Signal Width dialog box appears.

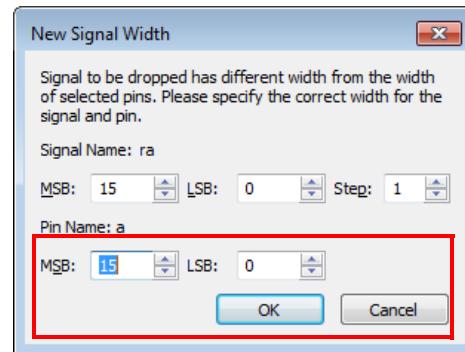


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Module 2: Working with Components and Connectivity

- f. Specify the MSB (most significant bit) for the pin $a<17..0>$ as 15.

This indicates that the $ra<15..0>$ signal will be connected to the bits 0 to 15 of the pin $a<17..0>$.



- g. Click *OK*.

The New Signal Width dialog box appears.

- h. Specify the MSB (most significant bit) for the pin $a<17..0>$ as 15.

- i. Click *OK*.

The pin $a<17..0>$ on both the instances of the component is connected to the $ra<15..0>$ signal.

| Component Connectivity Details | | |
|---|---------------|---|
| Attach Signal: <input type="text"/> ra<15..0> | | |
| i1 (tc55b4257) - U1 | | i2 (tc55b4257) - U2 |
| Pin Name | Pin Number | Signal |
| * | * | * |
| <input checked="" type="checkbox"/> a<17..0> | 12,13,14,1... | ,ra<15>,r... |
| ce* | 6 | |
| <input checked="" type="checkbox"/> dq<4..1> | 26,23,10,7 | ,ra<15>,ra<14>,ra<13>,ra<12>,ra<11>,... |
| eo* | 27 | |
| <input checked="" type="checkbox"/> io<3..1> | 17,16,1 | |
| we* | 11 | |

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Module 2: Working with Components and Connectivity

- j. Press the *Ctrl* key and click in the *Signal* cells next to the pin `dq<4..1>`.

| Pin Name | Pin Number | Signal | Signal |
|---|---------------|----------------------------------|---|
| * | * | * | * |
| <input checked="" type="checkbox"/> <code>a<17..0></code> | 12,13,14,1... | <code>,,ra<15>,r...</code> | <code>,,ra<15>,ra<14>,ra<13>,ra<12>,ra<11>,...</code> |
| <code>ce*</code> | 6 | | |
| <input checked="" type="checkbox"/> <code>dq<4..1></code> | 26,23,10,7 | | |
| <code>eo*</code> | 27 | | |
| <input checked="" type="checkbox"/> <code>io<3..1></code> | 17,16,1 | | |
| <code>we*</code> | 11 | | |

- k. Select the `rd<7..0>` signal in the Signal List.
- l. Keeping the left-mouse button pressed, drag and drop the signal on the pin `dq<4..1>` in the Component Connectivity Details pane.

The New Signal Width dialog box appears.

- m. Specify the MSB (most significant bit) for the `rd<7..0>` signal as 3.
- n. Click *OK*.

The New Signal Width dialog box appears.

- o. Specify the MSB (most significant bit) for the `rd<7..0>` signal as 3.
- p. Click *OK*.

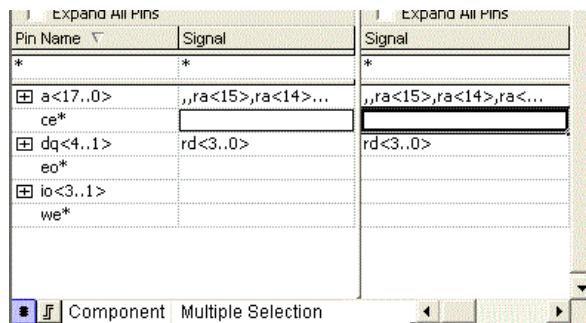
The pin `dq<4..1>` on both the instances of the component is connected to the `rd<3..0>` signal.

| Pin Name | Pin Number | Signal | Signal |
|---|---------------|----------------------------------|---|
| * | * | * | * |
| <input checked="" type="checkbox"/> <code>a<17..0></code> | 12,13,14,1... | <code>,,ra<15>,r...</code> | <code>,,ra<15>,ra<14>,ra<13>,ra<12>,ra<11>,...</code> |
| <code>ce*</code> | 6 | | |
| <input checked="" type="checkbox"/> <code>dq<4..1></code> | 26,23,10,7 | <code>rd<3..0></code> | <code>rd<3..0></code> |
| <code>eo*</code> | 27 | | |
| <input checked="" type="checkbox"/> <code>io<3..1></code> | 17,16,1 | | |
| <code>we*</code> | 11 | | |

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

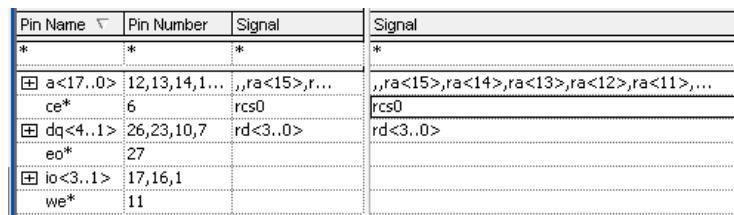
- q. Press the *Ctrl* key and click in the *Signal* cells next to the pin *ce**.



| Pin Name | Signal | Pin Name | Signal |
|--|--------------------|----------|------------------------|
| * | * | * | * |
| <input checked="" type="checkbox"/> a<17..0> | ,,ra<15>,ra<14>... | | ,,ra<15>,ra<14>,ra<... |
| <input checked="" type="checkbox"/> ce* | | | |
| <input checked="" type="checkbox"/> dq<4..1> | rd<3..0> | | rd<3..0> |
| <input checked="" type="checkbox"/> eo* | | | |
| <input checked="" type="checkbox"/> io<3..1> | | | |
| <input checked="" type="checkbox"/> we* | | | |

- r. Type *rcs0* and press *Enter*.

The pin *ce** on both the instances of the component is connected to the *rcs0* signal.

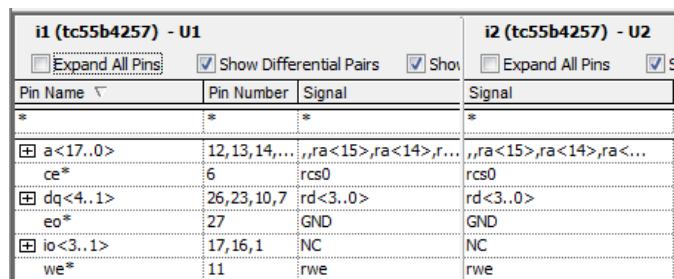


| Pin Name | Pin Number | Signal | Signal |
|--|---------------|---------------|--|
| * | * | * | * |
| <input checked="" type="checkbox"/> a<17..0> | 12,13,14,1... | ,,ra<15>,r... | ,,ra<15>,ra<14>,ra<13>,ra<12>,ra<11>,... |
| <input checked="" type="checkbox"/> ce* | 6 | rcs0 | rcs0 |
| <input checked="" type="checkbox"/> dq<4..1> | 26,23,10,7 | rd<3..0> | rd<3..0> |
| <input checked="" type="checkbox"/> eo* | 27 | | |
| <input checked="" type="checkbox"/> io<3..1> | 17,16,1 | | |
| <input checked="" type="checkbox"/> we* | 11 | | |

- s. Similarly connect:

- Pin *eo** to the GND signal.
- Pin *io<3..1>* to the NC signal.
- Pin *we** to the *rwe* signal.

The NC signal is used to indicate a pin that is intentionally unused. The NC signal name transfers to the board layout in Allegro PCB Editor as a dummy net that will not be routed.



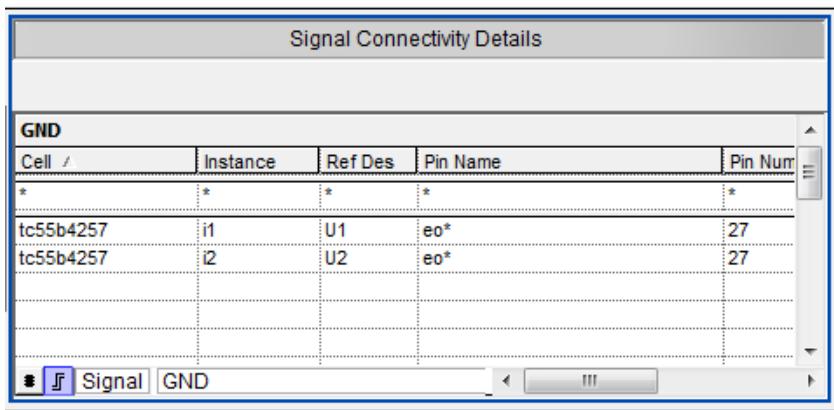
| i1 (tc55b4257) - U1 | | i2 (tc55b4257) - U2 | |
|--|---|--|--|
| <input type="checkbox"/> Expand All Pins | <input checked="" type="checkbox"/> Show Differential Pairs | <input checked="" type="checkbox"/> Show | <input type="checkbox"/> Expand All Pins |
| Pin Name | Pin Number | Signal | Signal |
| * | * | * | * |
| <input checked="" type="checkbox"/> a<17..0> | 12,13,14,... | ,,ra<15>,ra<14>,r... | ,,ra<15>,ra<14>,ra<... |
| <input checked="" type="checkbox"/> ce* | 6 | rcs0 | rcs0 |
| <input checked="" type="checkbox"/> dq<4..1> | 26,23,10,7 | rd<3..0> | rd<3..0> |
| <input checked="" type="checkbox"/> eo* | 27 | GND | GND |
| <input checked="" type="checkbox"/> io<3..1> | 17,16,1 | NC | NC |
| <input checked="" type="checkbox"/> we* | 11 | rwe | rwe |

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Module 2: Working with Components and Connectivity

12. Double-click on the GND signal in the Signal List.

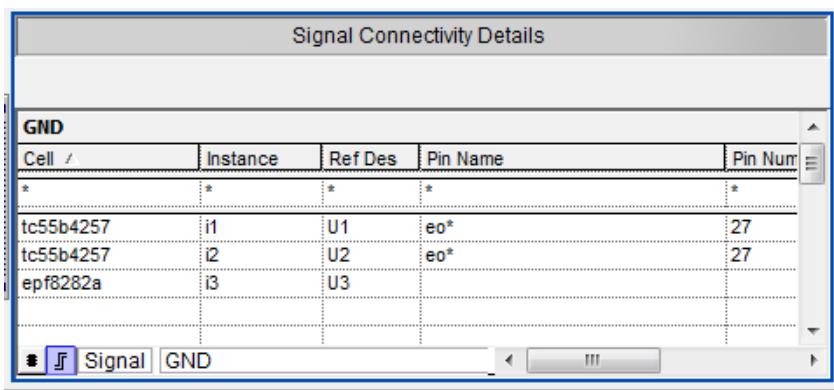
The connectivity information for the GND signal is displayed in the Signal Connectivity Details pane.



You can use the Signal Connectivity Details pane to quickly connect a signal to component pins.

- a. In the Component List, select the epf8282a component.
- b. Keeping the left-mouse button pressed, drag and drop the component in the Signal Connectivity Details pane.

A new row is added for the component.



- c. In the *Pin Name* column, click in the cell next to the epf8282a component.
- d. Type nsp or click the drop-down list to select the pin nsp.

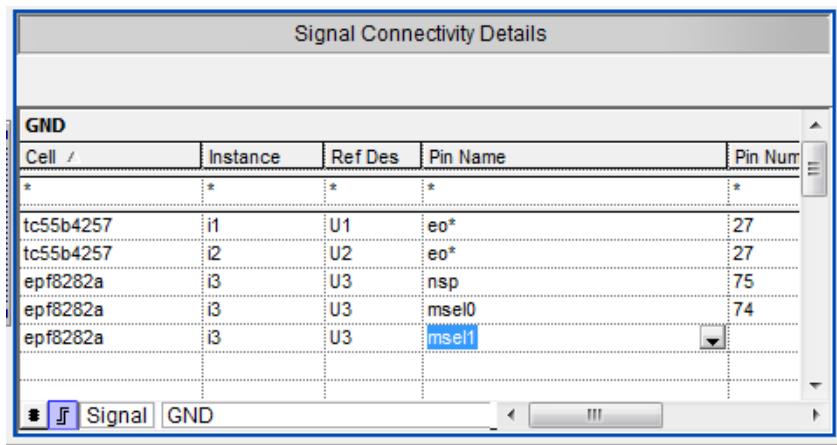
System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

- e. Click on any other cell in the Signal Connectivity Details pane.

The pin nsp is connected to the GND signal.

- f. Repeat steps a to d described above to connect the msel0 and msel1 pins of the epf8282a component to the GND signal.



The screenshot shows a software interface titled "Signal Connectivity Details". A table is displayed with the following data:

| GND | | | | |
|-----------|----------|---------|----------|---------|
| Cell / | Instance | Ref Des | Pin Name | Pin Num |
| * | * | * | * | * |
| tc55b4257 | i1 | U1 | eo* | 27 |
| tc55b4257 | i2 | U2 | eo* | 27 |
| epf8282a | i3 | U3 | nsp | 75 |
| epf8282a | i3 | U3 | msel0 | 74 |
| epf8282a | i3 | U3 | msel1 | |

At the bottom of the pane, there are buttons for "Signal" and "GND".

When you copy and paste a component in the Component List, its connectivity and property information are also copied. This feature lets you capture connectivity and property information on one instance of a component and quickly replicate the connectivity and property information on additional instances of the same component you want to use in your design.

- a. Double-click on the tc55b4257 component with the instance name i1 in the Component List.

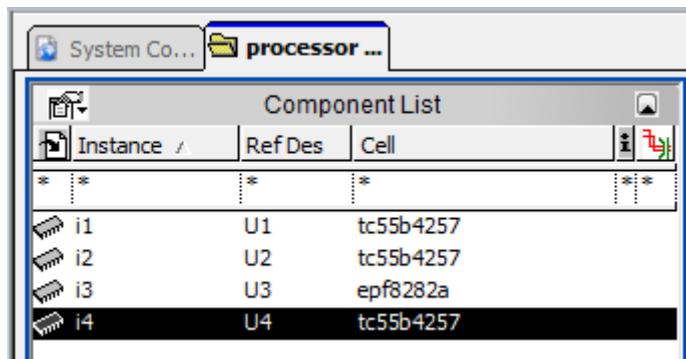
The connectivity for the component is displayed in the Component Connectivity Details pane.

- b. Choose *Edit – Copy* or press *Ctrl + C*.
c. Choose *Edit – Paste* or press *Ctrl + V*.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

A new instance of the `tc55b4257` component with the instance name `i4` is added in the Component List.



- d. Select instance `i4` of the `tc55b4257` component in the Component List.

The connectivity for the component is displayed in the Component Connectivity Details pane.

| i4 (tc55b4257) - U4 | | | |
|--|---|--|--------------------------------------|
| <input type="checkbox"/> Expand All Pins | <input checked="" type="checkbox"/> Show Differential Pairs | <input checked="" type="checkbox"/> Show Vectors | |
| Pin Name | Pin Number | Pin Type | Signal |
| * | * | * | * |
| <input checked="" type="checkbox"/> a<17..0> | 12,13,14,15... | Input | ,,ra<15>,ra<14>,ra<13>,ra<12>,ra<11> |
| <input checked="" type="checkbox"/> ce* | 6 | Input | rcs0 |
| <input checked="" type="checkbox"/> dq<4..1> | 26,23,10,7 | Inout | rd<3..0> |
| <input checked="" type="checkbox"/> eo* | 27 | Input | GND |
| <input checked="" type="checkbox"/> io<3..1> | 17,16,1 | Inout | NC |
| <input checked="" type="checkbox"/> we* | 11 | Input | rwe |

Note that the connectivity information on the component has also been copied.

The paste special feature in System Connectivity Manager lets you copy connectivity from one component and paste it on another component after making the required changes. Connect the pin `ce*` to the `rcs1` signal. To connect the pin, do the following:

- a. Add an instance of the `tc55b4257` component in the design.

For more information on adding components in the design, see [Lesson 2-1: Adding Components](#) on page 56.

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Module 2: Working with Components and Connectivity

- b.** Select instance `i1` of the `tc55b4257` component in the Component List.
- c.** In the Component Connectivity Details pane, select all the signals in the *Signal* column.

| Pin Name | Pin Number | Pin Type | Signal | Termination | ? | ? |
|----------|------------|-------------|--------|---------------|----|---|
| * | * | * | * | * | * | * |
| [+] | a<17..0> | 12,13,14... | Input | ,ra<15>,ra... | | |
| ce* | 6 | Input | | rcs0 | | |
| [+] | dq<4..1> | 26,23,10,7 | Inout | rd<3..0> | | |
| eo* | 27 | Input | | GND | | |
| [+] | io<3..1> | 17,16,1 | Inout | | NC | |
| we* | 11 | Input | | rwe | | |

- d.** Choose *Edit – Copy* or press *Ctrl + C* to copy the signal names.
- e.** Select instance `i5` (the instance you added in step **a** above) of the `tc55b4257` component.
- f.** Click in the first cell in the *Signal* column in the Component Connectivity Details pane.

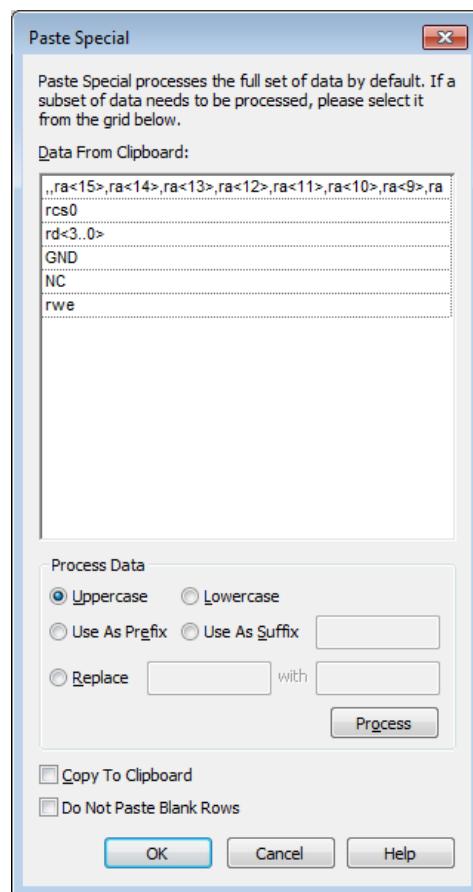
| Pin Name | Pin Number | Pin Type | Signal | Termination | ? | ? |
|----------|------------|-------------|--------|-------------|---|---|
| * | * | * | * | * | * | * |
| [+] | a<17..0> | 12,13,14... | Input | | | |
| ce* | 6 | Input | | | | |
| [+] | dq<4..1> | 26,23,10,7 | Inout | | | |
| eo* | 27 | Input | | | | |
| [+] | io<3..1> | 17,16,1 | Inout | | | |
| we* | 11 | Input | | | | |

- g.** Choose *Edit – Paste Special*.

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Module 2: Working with Components and Connectivity

The Paste Special dialog box appears.



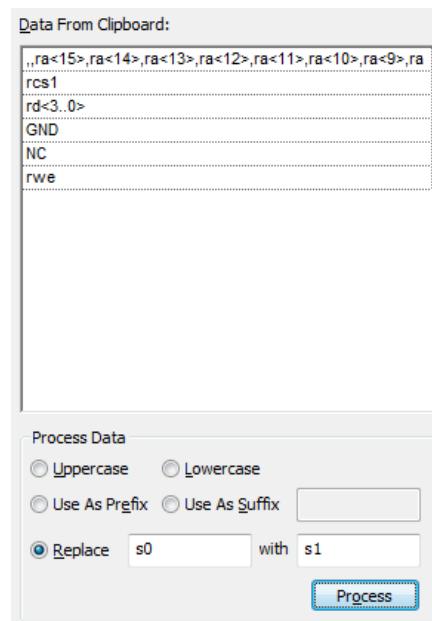
Here, you will replace the `rcs0` signal with `rcs1`.

- h.** Select the *Replace* option.
 - i.** Type `s0` in the first field and `s1` in the second field.
 - j.** Click the *Process* button.

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Module 2: Working with Components and Connectivity

k. The signal `rcs0` is changed to `rcs1`.

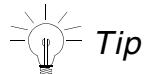


I. Click *OK*.

The modified connectivity information is pasted in the *Signal* column of the Component Connectivity Details pane.

| Component Connectivity Details | | | | |
|---|--------------|---|--|----------|
| Attach Signal: <input type="text" value="rwe"/> <input style="margin-left: 10px;" type="button" value="..."/> | | | | |
| i5 (tc55b4257) - U5 | | | | |
| Pin Name | Pin Number | Pin Type | Signal | Termi... |
| * | * | * | * | * |
| <input checked="" type="checkbox"/> <input type="checkbox"/> Expand All Pins | | <input checked="" type="checkbox"/> Show Differential Pairs | <input checked="" type="checkbox"/> Show Vectors | |
| a<17..0> | 12,13,14,... | Input | ,,ra<15>,r... | |
| ce* | 6 | Input | rcs1 | |
| dq<4..1> | 26,23,10,7 | Inout | rd<3..0> | |
| eo* | 27 | Input | GND | |
| io<3..1> | 17,16,1 | Inout | NC | |
| we* | 11 | Input | rwe | |

13. Choose *File – Save* to save the design.



Tip

You can also copy signal names from the Component Connectivity Details pane or from other applications, such as Microsoft Excel, and paste them in the *Signal* column in the Component Connectivity Details pane.

Summary

You now know how to use the Component Connectivity Details pane and the Signal Connectivity Details pane in System Connectivity Manager to quickly add connectivity information in the design. You also learned how to copy and paste connectivity information.

For More Information

See the [Capturing Connectivity](#) chapter of *System Connectivity Manager User Guide*.

Lesson 2-5: Viewing Connectivity in the Design

Overview

Having completed capturing design connectivity, you can now view how a particular signal moves across the components in the design and thus verify the connectivity.

In this lesson, you will learn to use the Matrix Connectivity View for viewing, adding, and modifying the signal connectivity.

In the Matrix Connectivity View, connectivity in the design is displayed in a matrix format. The rows in the matrix correspond to signal names and the columns correspond to the component instances. Each grid consists of the pin name to which a signal is connect.

Procedure

1. Choose *Table – Matrix View – Create*.
 2. In the Create Matrix View dialog box, select the Temporary View option.

Note: If *i5 – U5 (tc55b4257)* is in the Selected Objects list, select it and click the < Remove button to move it to the Available Objects list.
 3. Select the components to be added in the Matrix view.
 - a. Select instance *i1* of the *tc55b4257* component and instance *i3* of *epf8282a* from the Available Objects list.
 - b. Click the *Add* button.
 4. Select the signals to be added in the Matrix view. All the signals available in the design are listed in the Available Objects list in the Signals tab.
 - a. Click the *Signals* tab.
 - b. Select all signals from *ra<15>* to *ra<0>*.

Note: In the Available Objects list, all the buses in the design are flattened out and listed as individual bus bits.
 - c. Click *Add*.
5. Click OK.

The Matrix Connectivity View, Temp1 is created. Temp1 is the default name assigned to the first temporary view.

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Module 2: Working with Components and Connectivity

The view indicates that the signal `ra<15..0>` is not connected to any pin of component instance `i3`.

| Matrix Connectivity View - Temp1 | | | | |
|----------------------------------|---------------------------|--------------------------|------------|----------------------------|
| Signals | | Component i1 (U1) | | Component i3 |
| Name | Phys Name | Pin Name | Pin Number | Pin Name |
| * | * | * | * | * |
| <code>ra<15></code> | <code>RA<15></code> | <code>a<15></code> | 14 | |
| <code>ra<14></code> | <code>RA<14></code> | <code>a<14></code> | 15 | |
| <code>ra<13></code> | <code>RA<13></code> | <code>a<13></code> | 18 | <code>rdynbusy</code> |
| <code>ra<12></code> | <code>RA<12></code> | <code>a<12></code> | 19 | <code>add<13></code> |
| <code>ra<11></code> | <code>RA<11></code> | <code>a<11></code> | 20 | <code>add<12></code> |
| <code>ra<10></code> | <code>RA<10></code> | <code>a<10></code> | 21 | <code>add<11></code> |
| <code>ra<9></code> | <code>RA<9></code> | <code>a<9></code> | 22 | <code>add<10></code> |
| <code>ra<8></code> | <code>RA<8></code> | <code>a<8></code> | 28 | <code>add<9></code> |
| <code>ra<7></code> | <code>RA<7></code> | <code>a<7></code> | 29 | <code>add<8></code> |
| <code>ra<6></code> | <code>RA<6></code> | <code>a<6></code> | 30 | <code>add<7></code> |
| <code>ra<5></code> | <code>RA<5></code> | <code>a<5></code> | 31 | <code>add<6></code> |
| <code>ra<4></code> | <code>RA<4></code> | <code>a<4></code> | 32 | <code>add<5></code> |
| <code>ra<3></code> | <code>RA<3></code> | <code>a<3></code> | 2 | <code>add<4></code> |
| <code>ra<2></code> | <code>RA<2></code> | <code>a<2></code> | 3 | <code>add<3></code> |
| <code>ra<1></code> | <code>RA<1></code> | <code>a<1></code> | 4 | <code>add<2></code> |
| <code>ra<0></code> | <code>RA<0></code> | <code>a<0></code> | 5 | <code>add<1></code> |

Using Matrix Connectivity View, connect signals `ra<15>` and `ra<14>` to pins `add18` and `add14` respectively.

| Signal Name | Pin Name |
|---------------------------|--------------------|
| <code>ra<15></code> | <code>add18</code> |
| <code>ra<14></code> | <code>add14</code> |

To connect `ra<15>` to the `add18` pin of instance `i3`, do the following:

1. Click in the grid corresponding to signal `ra<15>` and component `i3`.

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Module 2: Working with Components and Connectivity

A down-arrow button appears.

| Matrix Connectivity View - Temp1 | | | | |
|----------------------------------|-----------|-------------------|----------|------------|
| Signals | | Component i3 (U3) | | |
| Name ▾ | Phys Name | Pin Number | Pin Name | Pin Number |
| * | * | * | * | * |
| ra<15> | RA<15> | 14 | | ▼ |
| ra<14> | RA<14> | 15 | | |
| ra<13> | RA<13> | 18 | rdynbusy | 77 |

2. Click the down-arrow button.
3. From the drop-down list, select add18 and press <Enter>. The pin number is filled in automatically.
4. Similarly, connect signal ra<14> and the add14 pin of instance i3 .

| Matrix Connectivity View - Temp1 | | | | |
|----------------------------------|-----------|-------------------|----------|------------|
| Signals | | Component i3 (U3) | | |
| Name ▾ | Phys Name | Pin Number | Pin Name | Pin Number |
| * | * | * | * | * |
| ra<15> | RA<15> | 14 | add18 | 79 |
| ra<14> | RA<14> | 15 | add14 | 57 |

System Connectivity Manager supports the modification of the Matrix Connectivity View by adding or removing signals and components from the view. You will now modify the Temp1 view by adding the bwr signal.

1. Choose *Table – Matrix View – Edit*.
- The Edit Matrix View dialog is displayed.
2. Select the *Signals* tab.
3. Select bwr from the Available Objects list and click *Add*.
4. Click *OK*, to update the Matrix Connectivity View.

The bwr signal is added to the view.

An alternate method for adding new signals to the matrix view is to drag and drop the signal from the Signal List Pane to the Matrix view.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

- a. Select `rwe` from the Signal List Pane.
- b. Keeping the left-mouse button pressed, drag and drop the signal on the Matrix Connectivity View pane.

The signal is added to the Matrix Connectivity View.

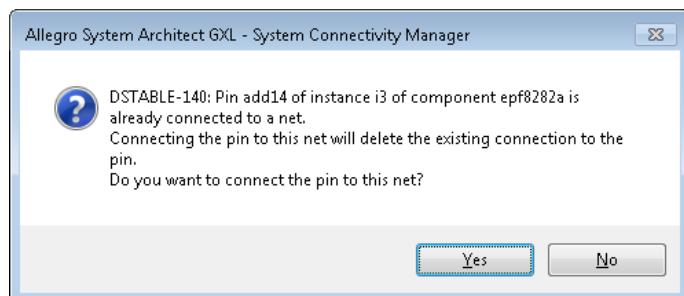
Similarly, you can add components to the Matrix Connectivity View pane.

Matrix Connectivity View can also be used to modify the existing connectivity by editing the signal to pin connection.

You will now modify the connectivity by connecting the `rwe` signal to the `add14` pin of instance `i3` of the component `epf8282a`.

1. Select the grid corresponding to the `rwe` signal and instance `i3`.
2. Click on the down-arrow button.
3. From the list of pin names, select `add14` and press *Enter*.

The following message appears.



4. Click `Yes` to modify the connections.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

The connectivity is updated. Note that the original connection of pin add14 to signal `ra<14>` is removed.

| Matrix Connectivity View - Temp1 | | | | |
|----------------------------------|-----------|-------------------|----------|------------|
| Signals | | Component i3 (U3) | | |
| Name | Phys Name | Pin Number | Pin Name | Pin Number |
| * | * | * | * | * |
| ra<15> | RA<15> | 14 | add18 | 79 |
| ra<14> | RA<14> | 15 | | |
| ra<13> | RA<13> | 18 | rdynbusy | 77 |
| ra<12> | RA<12> | 19 | add<13> | 58 |
| ra<11> | RA<11> | 20 | add<12> | 60 |
| ra<10> | RA<10> | 21 | add<11> | 61 |
| ra<9> | RA<9> | 22 | add<10> | 62 |
| ra<8> | RA<8> | 28 | add<9> | 63 |
| ra<7> | RA<7> | 29 | add<8> | 64 |
| ra<6> | RA<6> | 30 | add<7> | 65 |
| ra<5> | RA<5> | 31 | add<6> | 66 |
| ra<4> | RA<4> | 32 | add<5> | 67 |
| ra<3> | RA<3> | 2 | add<4> | 69 |
| ra<2> | RA<2> | 3 | add<3> | 70 |
| ra<1> | RA<1> | 4 | add<2> | 71 |
| ra<0> | RA<0> | 5 | add<1> | 76 |
| bwr | BWR | | inputb | 54 |
| rwe | RWE | 11 | add14 | 57 |

5. Connect the `ra<14>` signal to the `add0` pin.
 - a. Select the grid for signal `ra<14>` and component `i3`.
 - b. Click the down-arrow button to display all the pins of instance `i3`.
 - c. Select `add0` and press *Enter*.

The connectivity is updated.

6. Save the design.

The design is updated with the connectivity changes.

7. To close the temporary matrix view, choose *Table – Matrix View – Remove*.

Summary

You now know how to use the Matrix Connectivity View pane to quickly view the signal flow across components. You also learned

how to modify the connectivity information in the Matrix Connectivity View pane.

For More Information

See the following:

- [Capturing Connectivity](#) chapter of *System Connectivity Manager User Guide*.
-  A Flash-based multimedia demonstration of this module, [Using Matrix Connectivity View](#), is available on Cadence Online Support.

Lesson 2-6: Adding Comments in the Design

Overview

System Connectivity Manager allows you to add comments for components, signals and pins in the design. You can add comments for components in the Component List, for signals in the Signal List, and for pins in Component Connectivity Details pane.

The comments you add in the design can be displayed in reports and in the schematic generated for the design.

In this lesson, you will learn to add comments for components, signals and pins in the design.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

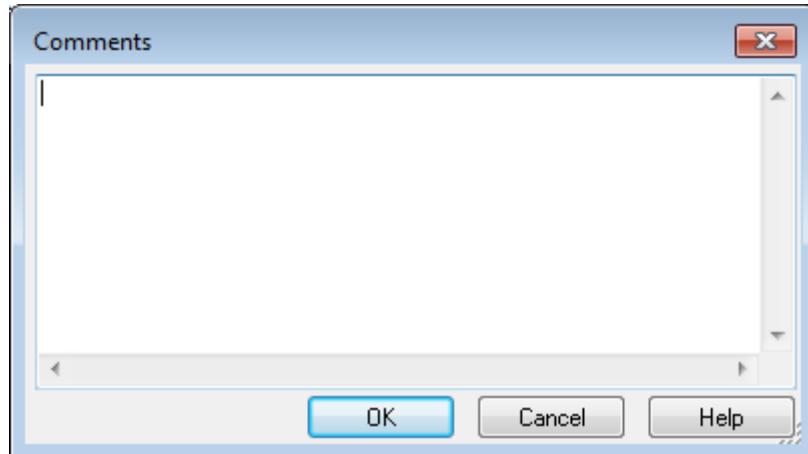
Procedure

1. In the Component List, select instance i1 of the tc55b4257 component.

| Instance / | Ref Des | Cell |
|------------|---------|-----------|
| * | * | * |
| i1 | U1 | tc55b4257 |
| i2 | U2 | tc55b4257 |
| i3 | U3 | epf8282a |
| i4 | U4 | tc55b4257 |
| i5 | U5 | tc55b4257 |

2. Choose *Object – Comments – Insert Comment*.

The Comments dialog box appears.



3. Enter the comment:

Add 4 bypass capacitors.

4. Click *OK*.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

An icon (ⓘ) in the Comments column (the column with the ⓘ icon) next to the component indicates that the comment has been added to the component.

| Component List | | | | |
|----------------|---------|-----------|----------|---------|
| Instance | Ref Des | Cell | Comments | Actions |
| * | * | * | * | * |
| i1 | U1 | tc55b4257 | ⓘ | |
| i2 | U2 | tc55b4257 | | |
| i4 | U4 | tc55b4257 | | |
| i5 | U5 | tc55b4257 | | |
| i3 | U3 | epf8282a | | |

5. Place the mouse pointer over the comment icon (ⓘ) next to the component.

A tooltip displays the comment added on the component. Note that tooltips displays the user name, date and time at which the comment was added, and the actual comment.

6. Select the signals `rccs0` and `rwe` in the Signal List.

| Signal List | | | | |
|--------------|-----------|----|------|---------|
| Name | Phys Name | # | Type | Actions |
| * | * | * | * | * |
| ra<15..0> | RA | 80 | | |
| rccs0 | RCS0 | 2 | | |
| rccs1 | RCS1 | 2 | | |
| rd<7..0> | RD | 24 | | |
| rwe | RWE | 5 | | |
| svd<7..0> | S_VD | 8 | | |
| sel | SEL | 1 | | |
| sub+ | SUB+ | 0 | | |
| sub- | SUB- | 0 | | |
| vcc | VCC | 0 | | |
| wstat | WSTAT | 0 | | |

7. Right-click and choose *Comments – Insert Comments*.

The Comments dialog box appears.

8. Enter the comment:

Pullup this signal.

9. Click **OK**.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

The comment icon () is displayed next to the signals in the Comments column in the Signal List.

| Name | Phys Name | # | Comments |
|---|-----------|----|---|
| * | * | * | * |
|   ra<15..0> | RA | 80 |  |
|   rcs0 | RCS0 | 2 |  |
|   rcs1 | RCS1 | 2 | |
|   rd<7..0> | RD | 24 | |
|   rwe | RWE | 5 |  |
|   s_vd<7..0> | S_VD | 8 | |
|   sel | SEL | 1 | |
|   sub+ | SUB+ | 0 | |
|   sub- | SUB- | 0 | |
|   vcc | VCC | 0 | |
|   wstat | WSTAT | 0 | |

10. Select the `i5` instance of `tc55b4257` in the Component List.
11. In the Component Connectivity Details pane, double-click in the Comments column (the column with the  icon) next to the pin `ce*`.

The Comments dialog box appears.

12. Enter the comment:

Apply shunt termination.

13. Click *OK*.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

The comment icon (ⓘ) icon is displayed next to the pin ce* in the Comments column in the Component Connectivity Details pane.

| Pin Name | Pin Number | Pin Type | Signal | Termination | Comments |
|--------------|-------------|----------|-------------|-------------|----------|
| * | * | * | * | * | * |
| [+] a<17..0> | 12,13,14... | Input | ,ra<15>,... | | |
| ce* | 6 | Input | rcs1 | | ⓘ |
| [+] dq<4..1> | 26,23,10,7 | Inout | rd<3..0> | | |
| eo* | 27 | Input | GND | | |
| [+] io<3..1> | 17,16,1 | Inout | NC | | |
| we* | 11 | Input | rwe | | |

14. Choose *File – Save* to save the design.

Summary

You now know how to add comments on components, signals and pins in the design. You also learned how to view the comments on objects in the design.

For More Information

See the [Working with Signals](#) chapter of *System Connectivity Manager User Guide*.

Exercise

Click on the epf8282a component in the Component List and capture the pin-signal connectivity on the component as shown below.

System Connectivity Manager Tutorial

Module 2: Working with Components and Connectivity

Note: Use the Signal List, Expanded Signal List, Component Connectivity Details pane and the Signal Connectivity Details pane to capture the connectivity information.

| i3 (epf8282a) - U3 | | | |
|--|---------------|----------|------------|
| <input type="checkbox"/> Expand All Pins | | | |
| Pin Name | Pin Number | Pin Type | Signal |
| * | * | * | * |
| add0 | 78 | Output | rwe |
| add14 | 57 | Output | ra<14> |
| add15 | 56 | Output | wstat |
| add16 | 36 | Output | |
| add17 | 51 | Output | rcs3 |
| add18 | 79 | Output | ra<15> |
| ⊕ add<13..1> | 58,60,61,6... | Output | ra<12..0> |
| ⊕ bd<7..0> | 18,19,20,2... | Input | rd<7..0> |
| clkusr | 50 | Output | rcs2 |
| conf_done | 11 | Input | ncs |
| data0 | 14 | Input | data |
| data1 | 13 | Input | sel |
| data2 | 9 | Input | ba<3> |
| data3 | 8 | Input | ba<2> |
| data4 | 7 | Input | ba<1> |
| data5 | 6 | Input | ba<0> |
| dclk | 10 | Input | dclk |
| gain | 28 | Output | gain |
| i/o | 16 | Input | |
| inputa | 55 | Input | brd |
| inputb | 54 | Input | bwr |
| inputc | 12 | Input | breset |
| input | 31 | Input | mclk |
| msel0 | 74 | Input | GND |
| msel1 | 53 | Input | GND |
| nconfig | 33 | Input | wait |
| ncs | 29 | Input | hs |
| trs | 48 | Output | rcs0 |
| nsp | 75 | Input | GND |
| nstatus | 32 | Input | oe |
| ntrst | 52 | Input | |
| nws | 30 | Input | fpga |
| ⊕ rd<7..0> | 4,3,2,1,84... | Output | rd<7..0> |
| rdclk | 49 | Output | rcs1 |
| rdynbusy | 77 | Output | ra<13> |
| reset | 15 | Input | reset |
| tck | 72 | Input | |
| tdi | 73 | Input | |
| tdo | 27 | Input | |
| vclkA | 34 | Output | vclkA |
| vclkB | 35 | Output | |
| vclkC | 37 | Output | vclkC |
| ⊕ vd<7..0> | 46,45,44,4... | Output | s_vd<7..0> |

Close System Connectivity Manager.

Module 3: Working with Associated Components

Prerequisite

If you have completed all the lessons in the previous modules, open the `tutorial.cpm` project located at

`<your_work_area>\modules\assoc_comp\tutorial` in System Connectivity Manager and perform the steps described in this module.

For more information, see [Understanding the Sample Design Files](#) on page 16.

Lessons

This module consists of the following lessons:

- [Overview](#) on page 112
- [Lesson 3-1: Applying Terminations](#) on page 112
- [Lesson 3-2: Adding Bypass Capacitors](#) on page 119
- [Lesson 3-3: Adding Pullups and Pulldowns](#) on page 126
- [Lesson 3-4: Using the Associated Component Viewer](#) on page 133

Multimedia Demonstration

 A Flash-based multimedia demonstration of this module, [Working with Associated Components](#), is available on Cadence Online Support.

Completion Time

1 hour for written lessons

11 minutes for multimedia demonstrations

Overview

Today's designs contain components, called associated components, that do not contribute to the logic of the design, but are a must for the correct functioning of the design. For example, bypass capacitors are needed for controlling power and ground bounce in the design. By definition, associated components are passive devices. System Connectivity Manager has classified associated components into three categories—terminations, bypass capacitors and pullup/pulldowns.

Traditional design entry tools do not capture the association between the parent object and the associated components. Wiring these components in the schematic is time consuming and error prone. Also, if you move or delete the parent object to which these associated components are attached in your schematic, you must ensure that the associated components are also moved or deleted.

The following lessons demonstrate how System Connectivity Manager allows you to quickly connect these devices to components and preserves their association with the components to which they are connected, making it easy to manage associated components in your design.

Lesson 3-1: Applying Terminations

Overview

Terminations are added to pins to ensure signal integrity. Terminations prevent the reflection of electrical signals occurring at the end of buses.

System Connectivity Manager supports applying standard terminations such as Series, Shunt, Thevenin and so on. The type of

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

termination you can add on a pin depends on the pin type of the pin, which is selected for termination.

In this lesson, you will learn to apply shunt terminations in the design.

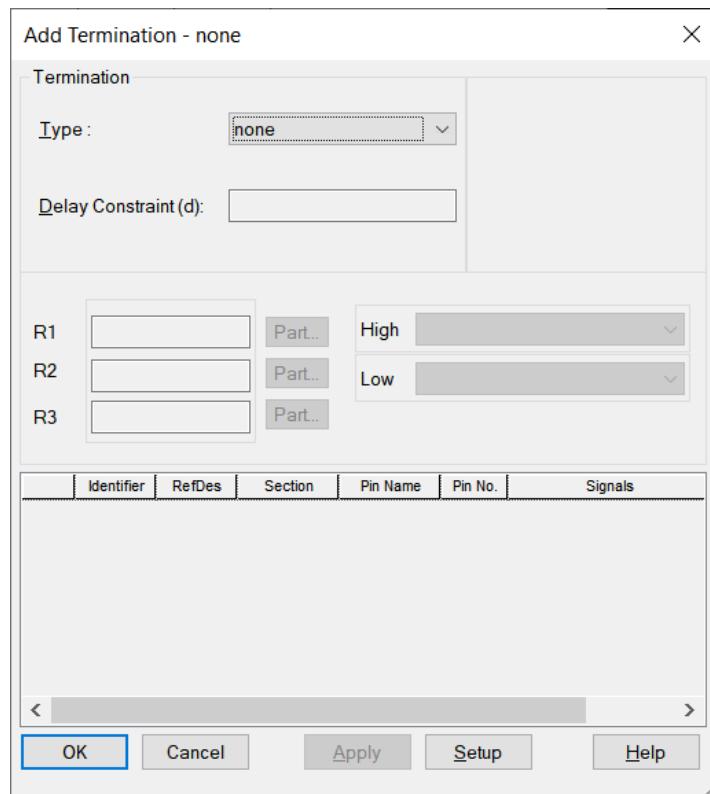
Procedure

1. In the Component List, select instance `i1` of the `tc55b4257` component.

The connectivity information for the component is displayed in the Component Connectivity Details pane.

2. Double-click on the *Termination* column next to the pin `ce*`.

The Add Termination dialog box appears.

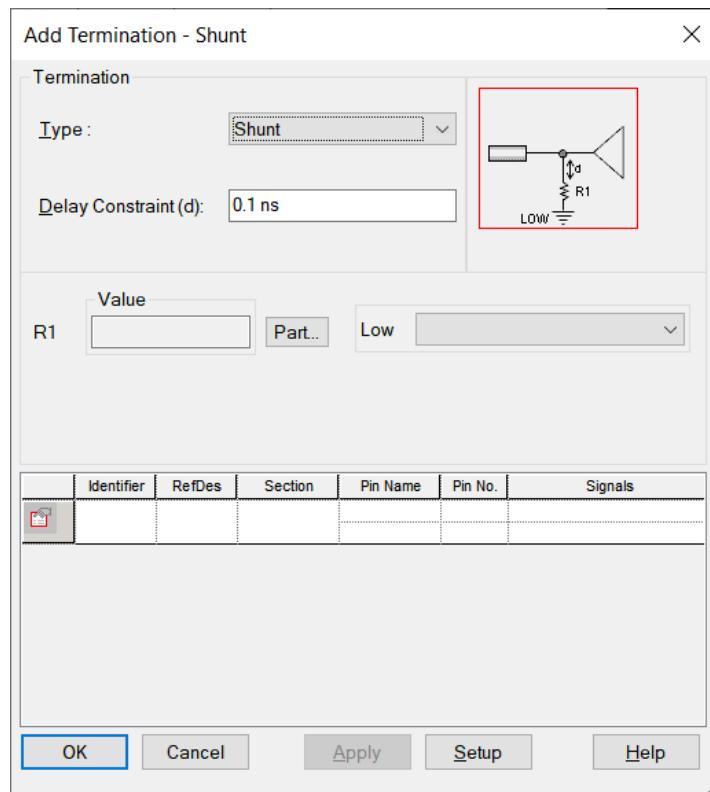


3. From the *Type* drop-down list, choose *Shunt* to add a shunt termination.

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

The Add Termination dialog box displays a graphical representation of the shunt termination scheme.



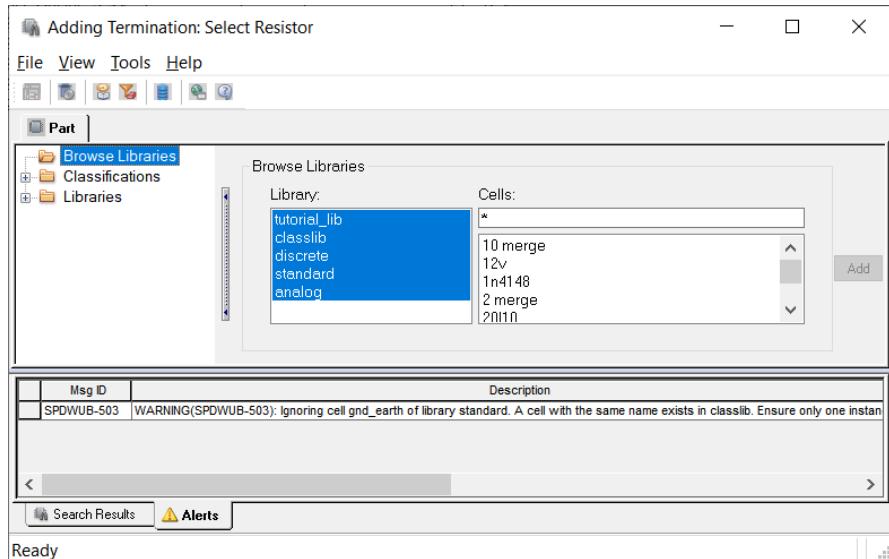
The default delay constraint is 0.1ns (nanoseconds). You can modify the delay value.

4. Click the *Part* button to select the resistor you want to use for the termination.

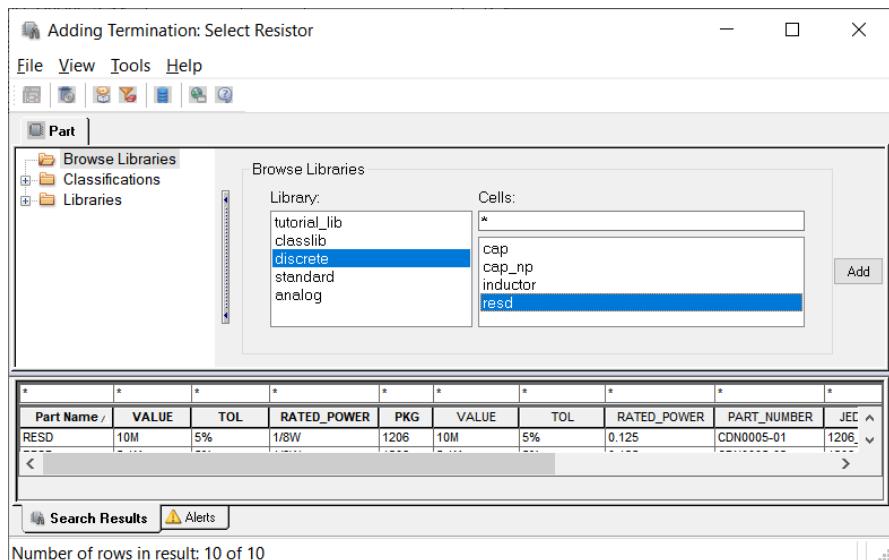
System Connectivity Manager Tutorial

Module 3: Working with Associated Components

The Adding Termination: Select Resistor dialog appears.



5. In the *Library* list, select the `discrete` library.
6. In the *Cells* list, select the `resd` component.



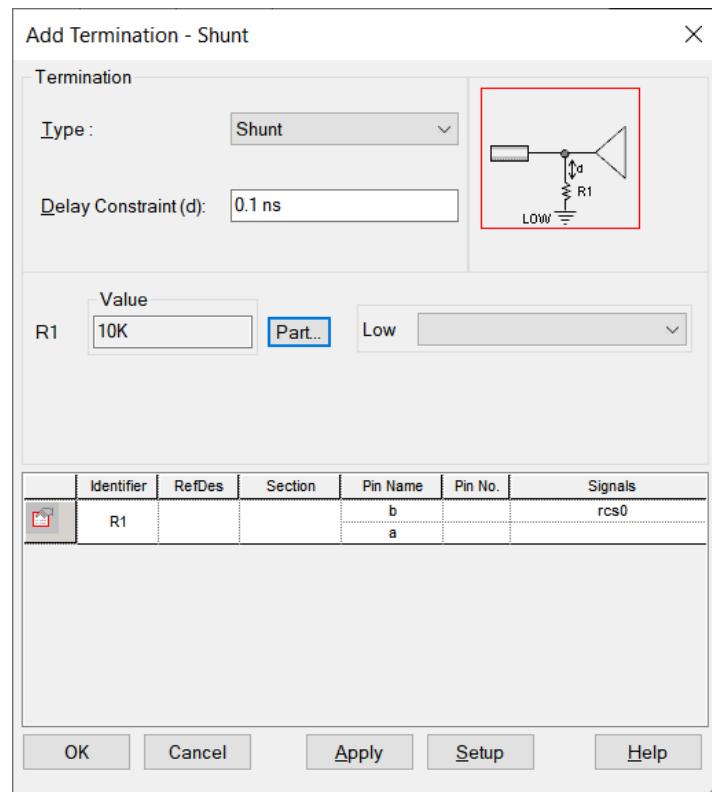
The part table rows for the resistor component are displayed in the *Search Results* pane.

7. In the *Search Results* pane, select the physical part with the value `10K`.
8. Click the *Add* button.

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Module 3: Working with Associated Components

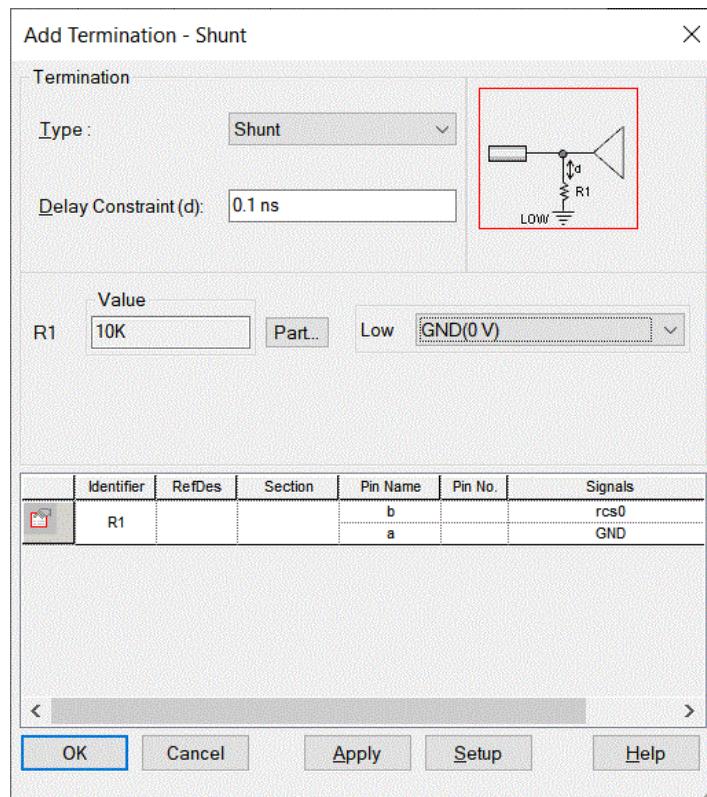
The value of the resistor is displayed in the *Value* field in the Add Termination dialog box.



System Connectivity Manager Tutorial

Module 3: Working with Associated Components

9. Click the *Low* drop-down list and select GND as the low signal.



10. Click *OK* to add the termination.

The termination type *Shunt* is displayed in the *Termination* column of the Component Connectivity Details pane.

| i1 (tc55b4257) - U1 | | | | | |
|--|---------------|---|---|--|---|
| <input type="checkbox"/> Expand All Pins | | <input checked="" type="checkbox"/> Show Differential Pairs | | <input checked="" type="checkbox"/> Show Vectors | |
| Pin Name | Pin Number | Pin Type | Signal | Termination / | |
| * | * | * | * | * | * |
| <input checked="" type="checkbox"/> a<17..0> | 12,13,14,1... | Input | ,,ra<15>,ra<14>,ra<13>,ra<12>,ra<11>... | | |
| <input checked="" type="checkbox"/> dq<4..1> | 26,23,10,7 | Inout | rd<3..0> | | |
| eo* | 27 | Input | GND | | |
| <input checked="" type="checkbox"/> io<3..1> | 17,16,1 | Inout | NC | | |
| we* | 11 | Input | rwe | | |
| ce* | 6 | Input | rcs0 | Shunt | |

If you place the mouse pointer over the termination, a tooltip displays the termination type, the resistor value and the voltage value of the signal.

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

You can copy the terminations added on a pin and paste it on another pin (on the same component or on another component) that supports the termination scheme.

11. Select the shunt termination added on the pin `ce*`.
12. Choose *Edit – Copy* or press *Ctrl + C*.
13. Click on the *Termination* column next to the pin `we*`.
14. Choose *Edit – Paste* or press *Ctrl + V*.

The termination is pasted on the pin `we*`.

| i1 (tc55b4257) - U1 | | | | | | |
|--|---|--|--|-------------|---|---|
| <input type="checkbox"/> Expand All Pins | <input checked="" type="checkbox"/> Show Differential Pairs | <input checked="" type="checkbox"/> Show Vectors | | | | |
| Pin Name | Pin Number | Pin Type | Signal | Termination | | |
| * | * | * | * | * | * | * |
| <input checked="" type="checkbox"/> a<17..0> | 12,13,14,1... | Input | ,ra<15>,ra<14>,ra<13>,ra<12>,ra<11>... | | | |
| <input checked="" type="checkbox"/> dq<4..1> | 26,23,10,7 | Inout | rd<3..0> | | | |
| <input checked="" type="checkbox"/> eo* | 27 | Input | GND | | | |
| <input checked="" type="checkbox"/> io<3..1> | 17,16,1 | Inout | NC | | | |
| <input checked="" type="checkbox"/> we* | 11 | Input | rwe | Shunt | | |
| <input checked="" type="checkbox"/> ce* | 6 | Input | rcs0 | Shunt | | |

The ability to copy and paste terminations lets you quickly apply terminations on pins in the design.

15. Choose *File – Save* to save the design.

Summary

You now know how to add a termination on a pin. You also learned how to copy and paste terminations.

Exercise

Add a series termination on the pin `add15` of the `epf8282a` component as shown below. For the termination, use the resistor component `resd` with the value `1K` from the discrete library.

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

Before adding a series termination, connect the `wstat` signal to the `ce*` pin.

| Component Connectivity Details | | | | | | |
|--|---|--|--------------------------|------------|----------|-----------|
| Attach Signal: <input type="text"/> =PINNAME | | | | | | |
| i3 (epf8282a) - U3 | | | | | | |
| <input type="checkbox"/> Expand All Pins | <input checked="" type="checkbox"/> Show Differential Pairs | <input checked="" type="checkbox"/> Show Vectors | Pin Name | Pin Number | Pin Type | Signal |
| * | * | * | * | * | * | * |
| | | | add0 | 78 | Output | ra<14> |
| | | | add14 | 57 | Output | rwe |
| | | | add15 | 56 | Output | wstat |
| | | | add16 | 36 | Output | |
| | | | add17 | 51 | Output | rcs3 |
| | | | add18 | 79 | Output | ra<15> |
| | | | ⊕ add<13..1> 58,60,61... | | Output | ra<12..0> |
| | | | ⊕ bd<7..0> 18,19,20... | | Input | rd<7..0> |
| | | | clkusr | 50 | Output | rcs2 |
| | | | conf_done | 11 | Input | ncs |
| | | | data0 | 14 | Input | data |
| | | | data1 | 13 | Input | sel |
| | | | data2 | 9 | Input | ba<3> |
| | | | data3 | 8 | Input | ba<2> |

For more information, see the [Working with Associated Components](#) chapter of *System Connectivity Manager User Guide*.

Lesson 3-2: Adding Bypass Capacitors

Overview

Bypass capacitors or decoupling capacitors are needed for controlling power and ground bounce in the design.

In this lesson, you will add four bypass capacitors to the memory component `tc55b4257`.

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

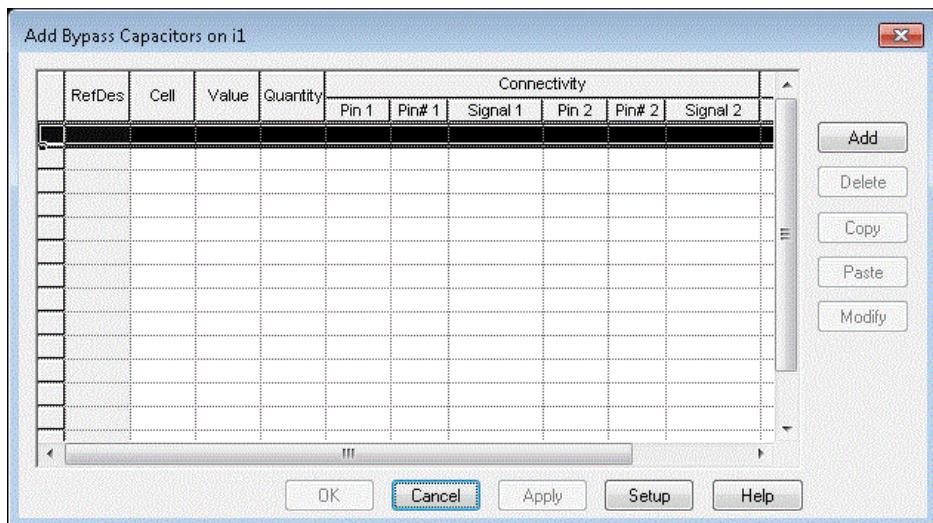
Procedure

1. In the Component List, select instance i1 of the tc55b4257 component.

| Component List | | | | | |
|----------------|---------|-----------|---|---|---|
| Instance | Ref Des | Cell | | | |
| * | * | * | * | * | * |
| i1 | U1 | tc55b4257 | | | |
| i2 | U2 | tc55b4257 | | | |
| i3 | U3 | epf8282a | | | |
| i4 | U4 | tc55b4257 | | | |
| i5 | U5 | tc55b4257 | | | |

2. Click the right-mouse button and choose *Add Bypass Capacitors* from the shortcut menu.

The Add Bypass Capacitors dialog box appears.



3. Click the *Add* button.

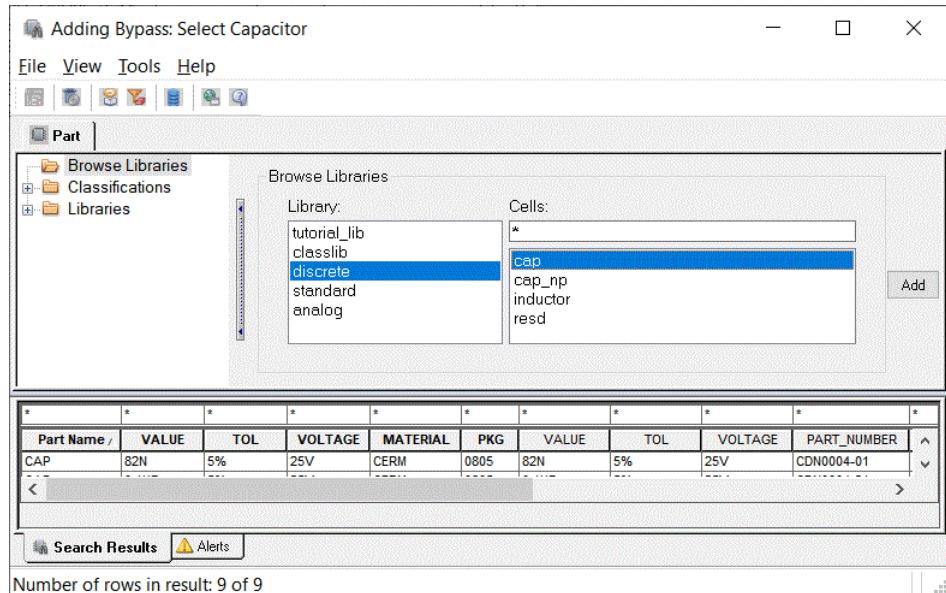
Part Information Manager appears.

4. In the *Library* list, select the *discrete library*.

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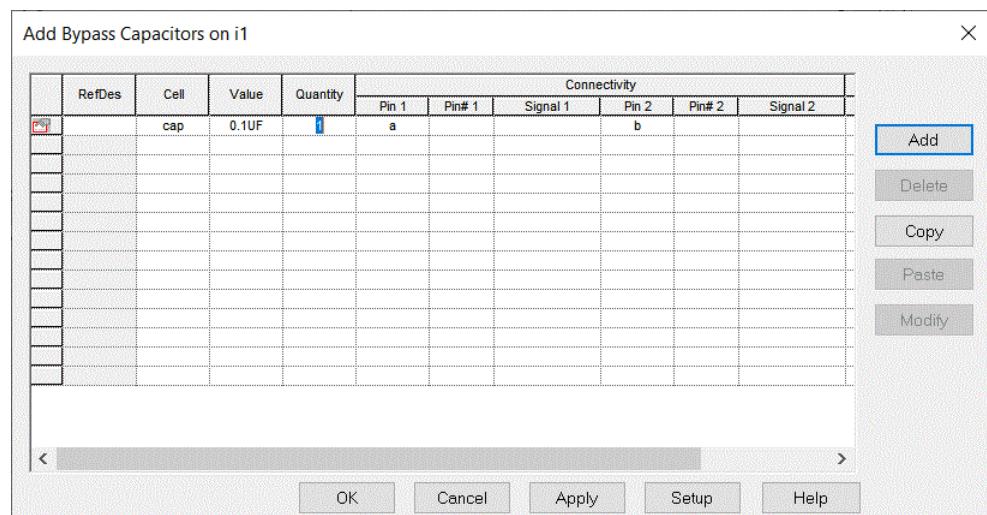
Module 3: Working with Associated Components

5. In the *Cells* list, select the *cap* component.



6. In the *Search Results* pane, select the physical part with the value *0.1UF*.
7. Click *Add*.

The capacitor component is displayed in the Add Bypass Capacitors dialog box.



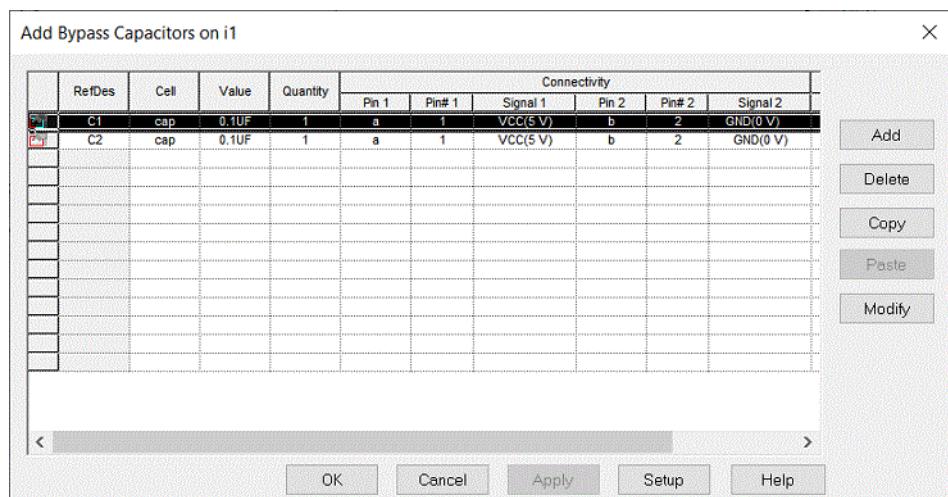
You will now add two bypass capacitors between the DC nets VCC and GND.

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

8. Change the quantity in the *Quantity* column to 2 and press *Enter*.
 9. From the *Signal 1* drop-down list, choose VCC.
 10. From the *Signal 2* drop-down list, choose GND.
 11. Click *Apply*.

Two bypass capacitors are added on the memory component.



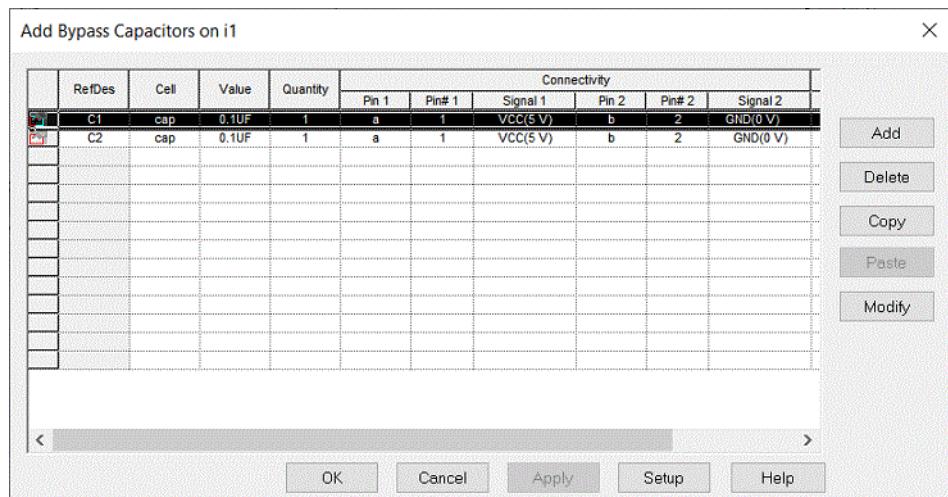
You will now add two more instances of the capacitor component cap with a capacitance value of 47UF as bypass capacitors between the same DC nets.

If you want to add more instances of the same capacitor between the same DC nets, but with different capacitance values, you can use the *Copy* and *Paste* buttons in the Add Bypass Capacitors dialog box to copy and paste capacitors, and then use the *Modify* button to modify the capacitance value on the pasted capacitors. This lets you quickly add bypass capacitors on components.

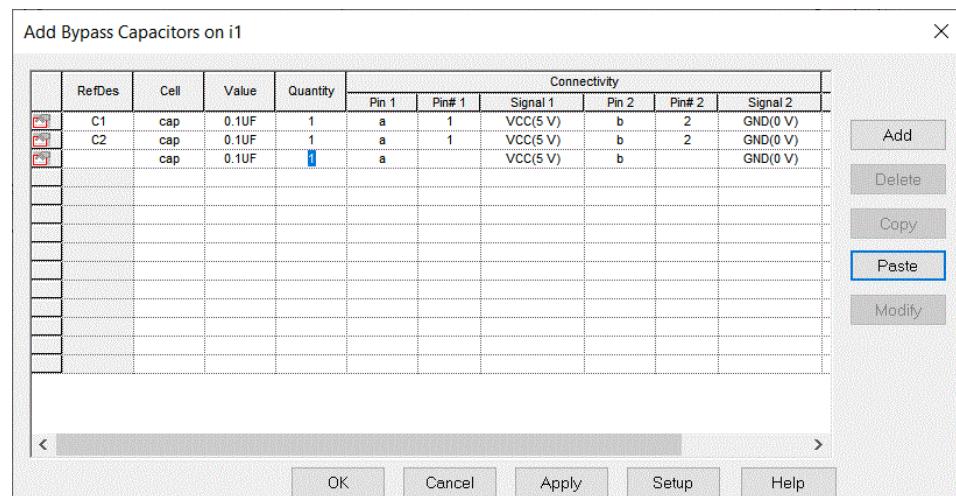
System Connectivity Manager Tutorial

Module 3: Working with Associated Components

12. Select the first capacitor displayed in the Add Bypass Capacitors dialog box.



13. Click the *Copy* button.
14. Select an empty row in the Add Bypass Capacitors dialog box and click the *Paste* button.



The capacitor is pasted in the Add Bypass Capacitors dialog box.

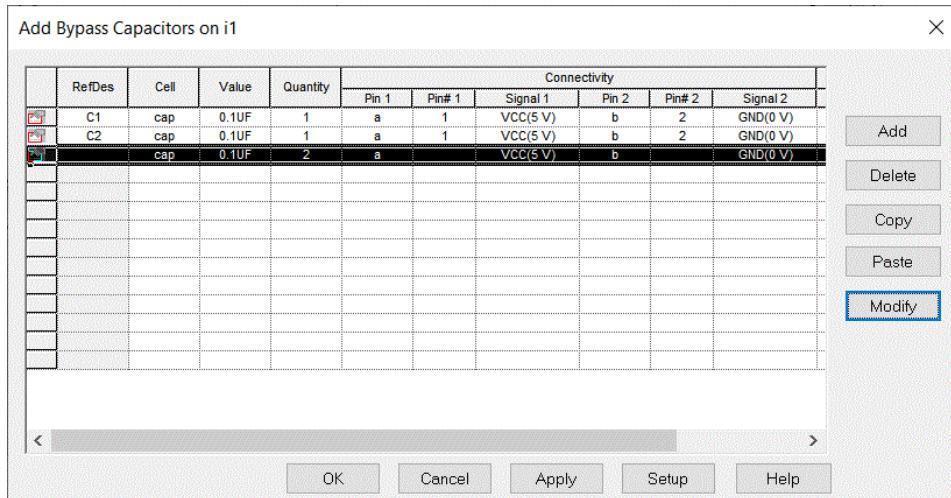
You will now add two capacitors with the value 47UF.

15. Change the quantity in the *Quantity* column to 2 and press *Enter*.

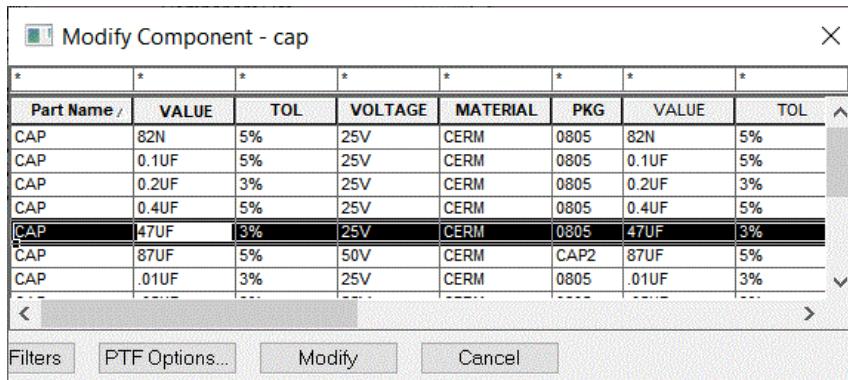
System Connectivity Manager Tutorial

Module 3: Working with Associated Components

16. Click on the third row and click the *Modify* button.



The Modify Component dialog box appears.



17. Select the part table row with the value 47UF and click the *Modify* button.

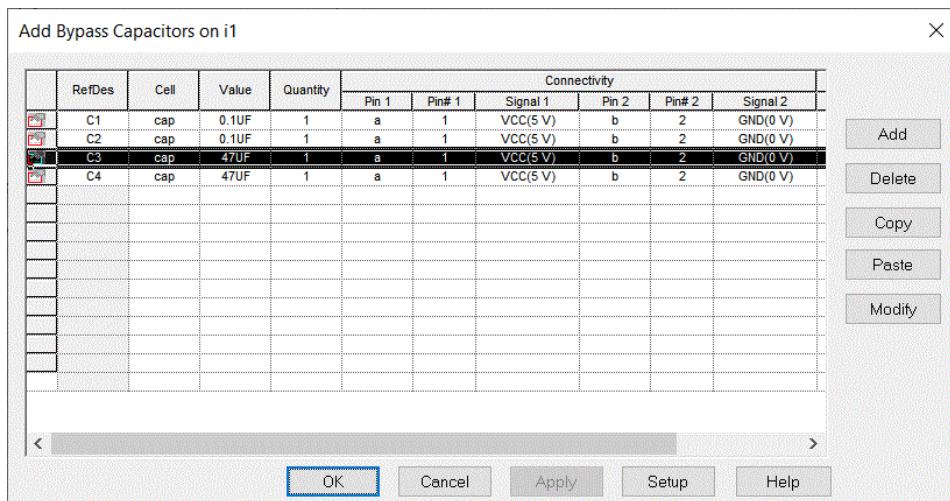
The value of the capacitor in the third row is changed to 47UF in the Add Bypass Capacitors dialog box.

18. Click the *Apply* button.

System Connectivity Manager Tutorial

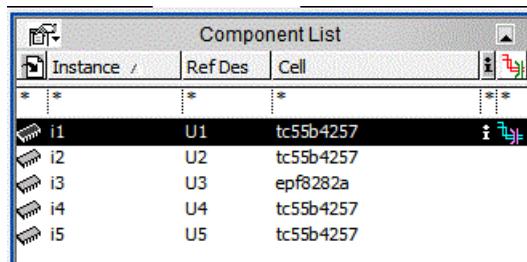
Module 3: Working with Associated Components

Two bypass capacitors with the value 47UF are added on the component.



19. Click **OK** to close the Add Bypass Capacitors dialog box.

The bypass capacitor icon () next to a component in the Component List indicates that bypass capacitors have been added to the component.



20. Choose **File – Save** to save the design.

Summary

You now know how to add bypass capacitors on a component. You also learned to:

- Copy and paste bypass capacitors
- Modify bypass capacitors
- Identify components in the design on which bypass capacitors are added

For More Information

See the [Working with Associated Components](#) chapter of *System Connectivity Manager User Guide*.

Lesson 3-3: Adding Pullups and Pulldowns

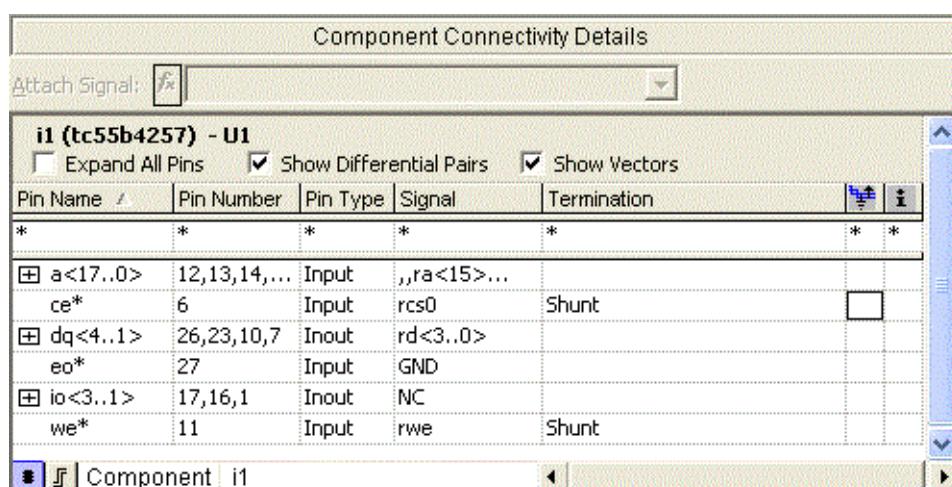
Overview

It is recommended to pullup or pulldown open pins of a component to reduce noise in the circuit.

In this lesson, you will learn how to add a pullup on a net.

Procedure

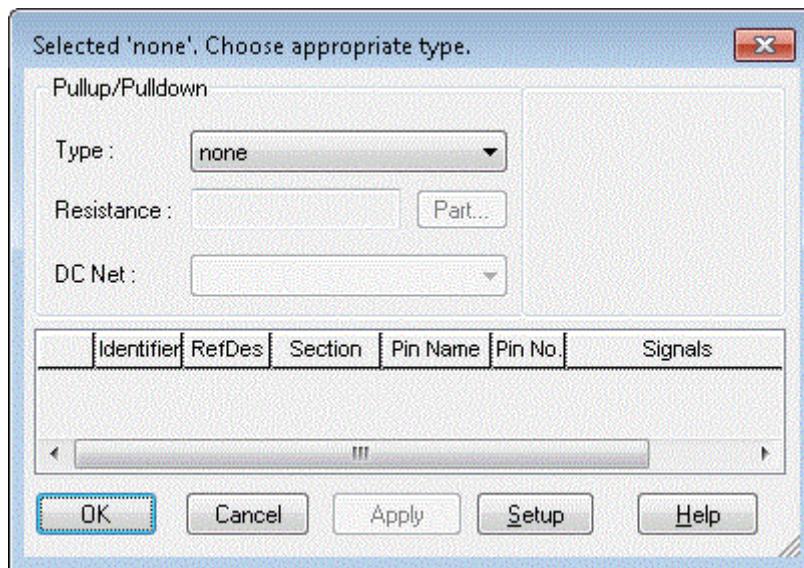
1. In the Component List, select instance `i1` of the `tc55b4257` component.
2. In the Component Connectivity Details pane, double-click in the Pullup/Pulldown column (the column with the  icon) next to the `ce*` pin.



System Connectivity Manager Tutorial

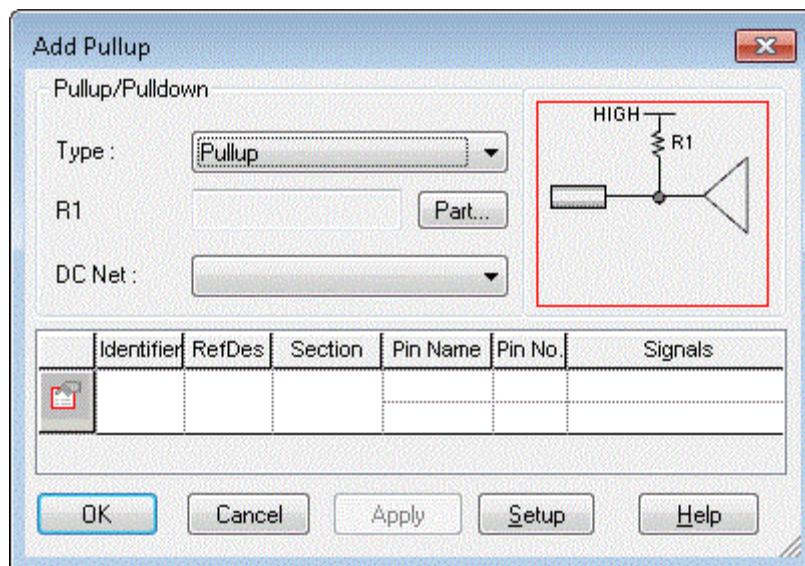
Module 3: Working with Associated Components

The Add Pullup/Pulldown dialog box appears.



3. From the Type drop-down list, choose *Pullup* to pullup the pin ce*.

The Add Pullup dialog box displays a graphical representation of the pullup scheme.



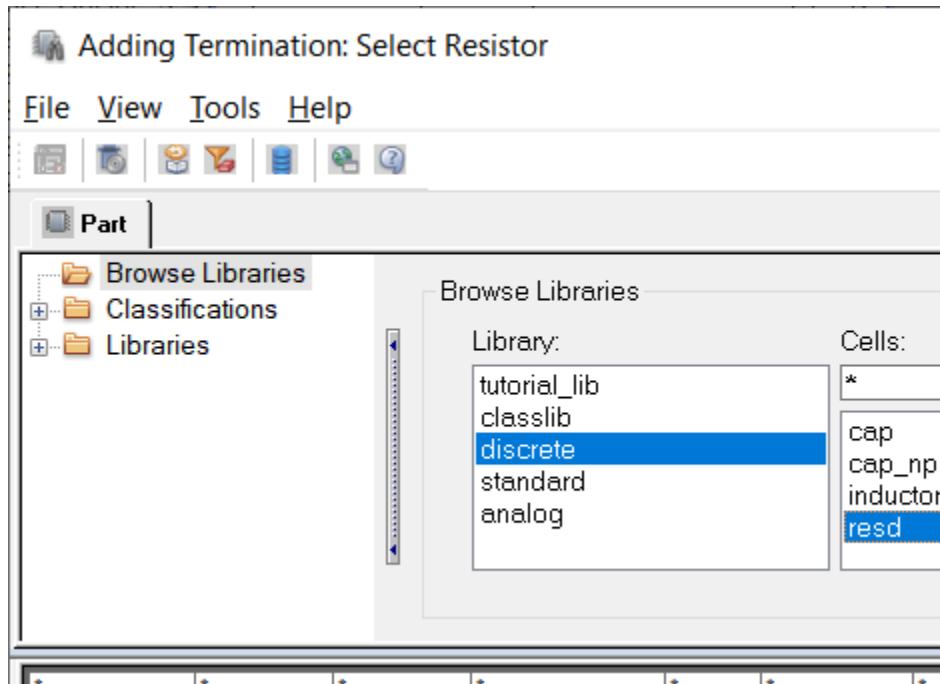
4. Click the *Part* button to select the resistor you want to use for the pullup.

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

Part Information Manager appears.

5. In the *Library* list, select the discrete library.
6. In the *Cells* list, select the `resd` component.



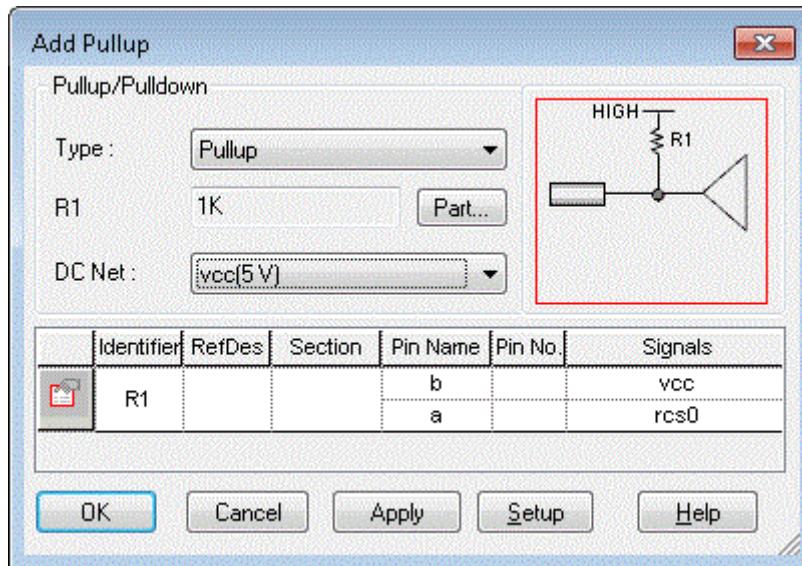
7. In the *Search Results* pane, select the physical part with the value `1K`.
8. Click the *Add* button.

The value of the resistor is displayed in the *R1* field in the Add Pullup dialog box.

System Connectivity Manager Tutorial

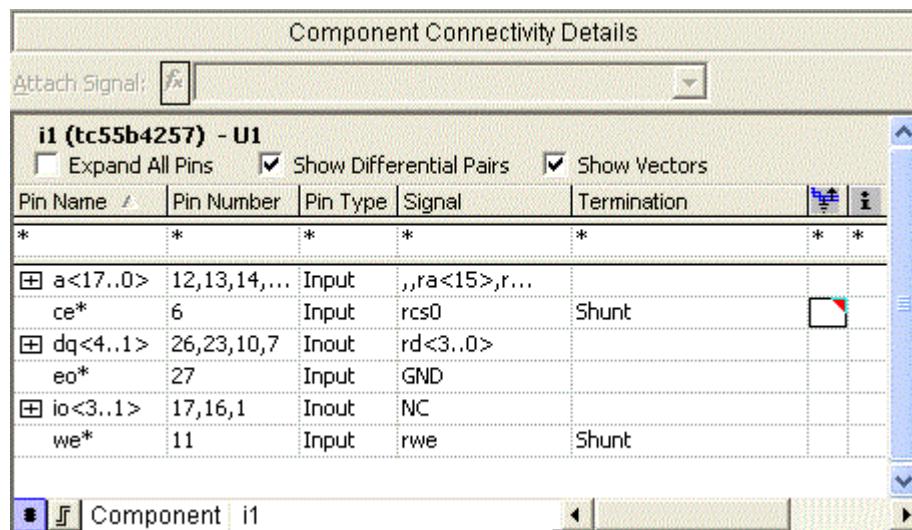
Module 3: Working with Associated Components

9. From the *DC Net* drop-down list, select the net VCC.



10. Click *OK* to add the pullup.

The red triangle at the top right of the cell in the Pullup/Pulldown column (the column with the icon) indicates that a pullup is attached to the net.

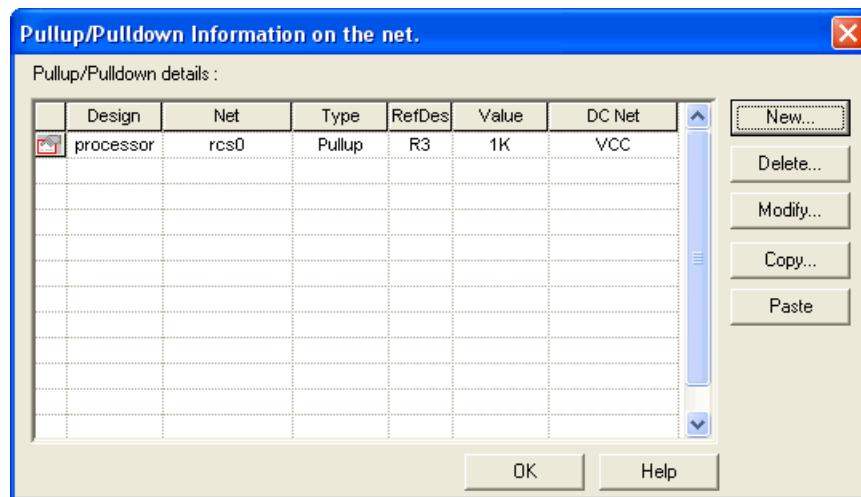


11. Double-click on the cell containing the pullup in the Pullup/Pulldown column.

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

The Pullup/Pulldown information on the net dialog box appears displaying the details of the pullup on the net.



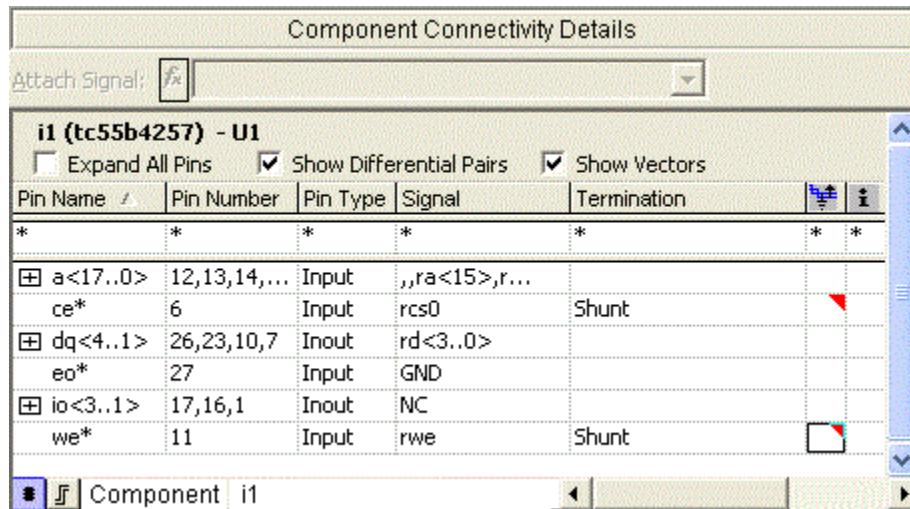
In this dialog box, you can add, copy/paste, modify and delete pull-ups and pulldowns on the net.

12. Click *OK* to close the Pullup/Pulldown information on the net dialog box.
13. You can copy pullups and pulldowns from one net and paste it on another net.
 - a. Click on the cell containing the pullup in the Pullup/Pulldown column (the column with the  icon).
 - b. Choose *Edit – Copy* or press *Ctrl + C*.
 - c. Click on Pullup/Pulldown column next to the `rwe` net.
 - d. Choose *Edit – Paste* or press *Ctrl + V*.

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

The pullup is pasted on the `rwe` net.



14. When you copy and paste a component in the Component List, its connectivity (pin-signal connectivity and the terminations, bypass capacitors and pullup/pulldowns), and property information are also pasted on the new instance of the component. This feature lets you capture connectivity and property information on one instance of a component and quickly replicate the connectivity and property information on additional instances of the same component you want to use in your design.
- In the Component List, select instance `i1` of the `tc55b4257` component.
 - Choose *Edit – Copy* or press *Ctrl + C*.
 - Choose *Edit – Paste* or press *Ctrl + V*.

A new instance of the `tc55b4257` component with the instance name `i6` is added in the Component List.

| Component List | | | |
|----------------|---------|-----------|---|
| Instance | Ref Des | Cell | |
| * | * | * | * |
| i1 | U1 | tc55b4257 | |
| i2 | U2 | tc55b4257 | |
| i3 | U3 | epf8282a | |
| i4 | U4 | tc55b4257 | |
| i5 | U5 | tc55b4257 | |
| i6 | U6 | tc55b4257 | |

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Module 3: Working with Associated Components

Note that the bypass capacitors on the original component has been copied and pasted on the new instance of the component.

- d. Select instance i6 of the tc55b4257 component in the Component List.

The connectivity for the component is displayed in the Component Connectivity Details pane.

The screenshot shows the 'Component Connectivity Details' dialog box. At the top, there is a search bar labeled 'Attach Signal:' with a magnifying glass icon. Below the search bar, there are three checkboxes: 'Expand All Pins' (unchecked), 'Show Differential Pairs' (checked), and 'Show Vectors' (checked). The main area is a table titled 'i6 (tc55b4257) - U6'. The table has columns: Pin Name, Pin Number, Pin Type, Signal, and Termination. The table contains the following data:

| Pin Name | Pin Number | Pin Type | Signal | Termination |
|--------------|-------------|----------|----------------|-------------|
| * | * | * | * | * |
| [+] a<17..0> | 12,13,14... | Input | ,,ra<15>,ra... | |
| ce* | 6 | Input | rcs0 | Shunt |
| [+] dq<4..1> | 26,23,10,7 | Inout | rd<3..0> | |
| eo* | 27 | Input | GND | |
| [+] io<3..1> | 17,16,1 | Inout | NC | |
| we* | 11 | Input | rwe | Shunt |

Note that the connectivity information (pin-signal connectivity and the terminations, bypass capacitors and pullup/pulldowns) on the original component has also been pasted on the new instance of the component.

15. Choose *File – Save* to save the design.

Summary

You now know how to add pullups on nets and how to copy a pullup added on a net and paste it on another net.

You also learned that when you copy and paste a component in the Component List, its connectivity information (pin-signal connectivity, terminations, bypass capacitors and pullup/pulldowns) is also pasted on the new instance of the component.

For More Information

See the [Working with Associated Components](#) chapter of *System Connectivity Manager User Guide*.

Lesson 3-4: Using the Associated Component Viewer

Overview

The individual discrete components attached to an object and the nets created as a result of adding terminations, bypass capacitors and pullup/pulldowns are displayed in the Associated Component Viewer and not in the Component List and the Signal List. This ensures that the design is not cluttered and keeps you focused on capturing the design's logic.

In this lesson, you will learn to view the associated components added on a component.

Procedure

1. Select instance `i1` of the `tc55b4257` component in the Component List.
2. Choose *View – Associated Components*.

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

The *Assoc Comp Viewer* tab (displayed in the bottom half of the System Connectivity Manager workspace) displays the details of the bypass capacitors on the component.

| Parent | RefDes | Value | Connectivity | |
|--------|--------|-------|--------------|--------------|
| | | | Pin | Physical Net |
| * | * | * | * | * |
| i1 | C1 | 0.1UF | 2 | GND |
| | | | 1 | VCC |
| i1 | C2 | 0.1UF | 2 | GND |
| | | | 1 | VCC |
| i1 | C3 | 47UF | 2 | GND |
| | | | 1 | VCC |
| i1 | C4 | 47UF | 2 | GND |
| | | | 1 | VCC |

Below the table:

Bypass Caps(4) Terminations(2) Pull-ups / Pull-downs(2)

Session Log Violations Assoc Comp Viewer Visual Design Differences

The Bypass Caps, Terminations and Pull-ups/Pull-downs tabs in the Assoc Comp Viewer display the number of terminations, bypass capacitors and pullup/pulldowns on the component.

3. Click on the Terminations and Pull-ups/Pull-downs tabs to view the details of the terminations and pullups and pulldowns added on the component.
4. In the Associated Component Viewer, you can modify the value of discrete components (resistors, capacitors, inductors and diodes) used in terminations, bypass capacitors and pullups and pulldowns

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

- a. Select instance i6 of the tc55b4257 component in the Component List.

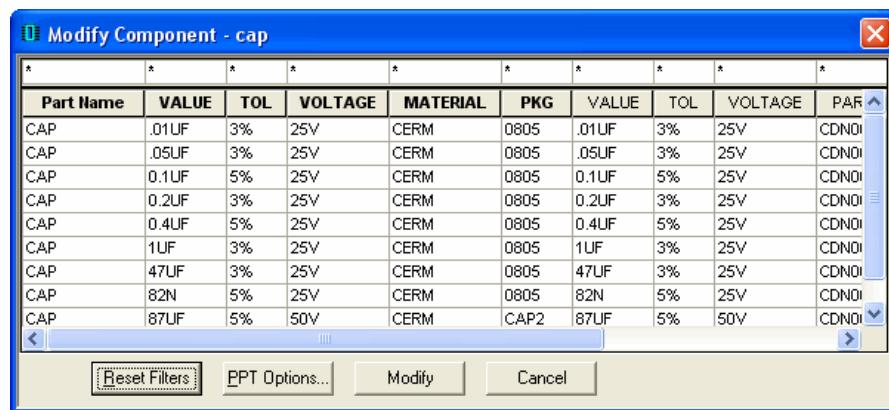
The *Assoc Comp Viewer* tab displays the details of the bypass capacitors on the component.

A screenshot of the 'Assoc Comp Viewer' tab in the System Connectivity Manager. The table shows the connections for component i6. The columns are Parent, RefDes, Value, Pin, and Physical Net. The rows show four capacitors (C5, C6, C7, C8) with values 0.1UF, 0.1UF, 47UF, and 47UF respectively, connected between pins 2 and 1 and GND and VCC. Below the table, there are tabs for Session Log, Violations, Assoc Comp Viewer (which is selected), and Visual Design Differences. A status bar at the bottom shows 'Bypass Caps(4)', 'Terminations(2)', and 'Pull-ups / Pull-downs(2)'.

| Parent | RefDes | Value | Connectivity | |
|--------|--------|-------|--------------|--------------|
| | | | Pin | Physical Net |
| * | * | * | * | * |
| i6 | C5 | 0.1UF | 2 | GND |
| | | | 1 | VCC |
| i6 | C6 | 0.1UF | 2 | GND |
| | | | 1 | VCC |
| i6 | C7 | 47UF | 2 | GND |
| | | | 1 | VCC |
| i6 | C8 | 47UF | 2 | GND |
| | | | 1 | VCC |

- b. Click on the capacitor with the reference designator C7.
c. Click the right-mouse button and choose *Modify Component*.

The Modify Component dialog box appears.



5. Select the part table row with the value .01uf and click the *Modify* button.

The value of the capacitor is changed to .01uf in the *Bypass Caps* tab of the Assoc Comp Viewer.

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

6. The discrete components (resistors, capacitors, diodes and inductors used in terminations, bypass capacitors and pullup/pulldowns) are directly associated with the objects on which you add the terminations, bypass capacitors or pullup/pulldowns. If you delete the object, the discrete components associated with the object are also automatically deleted. This makes it very easy for you to manage discrete components in your design.

- a. Select instance i6 of the tc55b4257 component in the Component List.

The *Assoc Comp Viewer* tab displays the details of the bypass capacitors on the component.

The screenshot shows a software interface for managing associated components. At the top, there's a toolbar with icons for Session Log, Violations, Assoc Comp Viewer (which is currently selected), and Visual Design Differences. Below the toolbar is a table titled 'Bypass Caps(4)'. The table has columns for Parent, RefDes, Value, Pin, and Physical Net. The data in the table is as follows:

| Parent | RefDes | Value | Connectivity | |
|--------|--------|-------|--------------|--------------|
| | | | Pin | Physical Net |
| * | * | * | * | * |
| i6 | C5 | 0.1UF | 2 | GND |
| | | | 1 | VCC |
| i6 | C6 | 0.1UF | 2 | GND |
| | | | 1 | VCC |
| i6 | C7 | .01UF | 2 | GND |
| | | | 1 | VCC |
| i6 | C8 | 47UF | 2 | GND |
| | | | 1 | VCC |

Below the table, there are navigation buttons for the viewer: back, forward, and search. The status bar at the bottom indicates 'Bypass Caps(4)', 'Terminations(2)', 'Pull-ups / Pull-downs(2)', and 'Session Log'.

- b. Right-click and select *Delete*.

The component and its associated discrete components are deleted from the design.

7. Choose *File – Save* to save the design.

Summary

You now know how to view the associated components added on components using the Associated Component Viewer. You also learned the following:

- How to modify the value of associated components

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Module 3: Working with Associated Components

- Deleting a component in the Component List deletes the associated components connected to it. This makes it easy to manage associated components in the design as you do not have to manually delete the associated components connected to a component when you delete the component in the design.

For more information

See the [Working with Associated Components](#) chapter of *System Connectivity Manager User Guide*.

System Connectivity Manager Tutorial

Module 3: Working with Associated Components

Module 4: Working with Properties

Prerequisite

If you have not completed all the lessons in the previous modules, you must open the `tutorial.cpm` project located at `<your_work_area>\modules\properties\tutorial` in System Connectivity Manager and perform the steps described in this module.

For more information, see [Understanding the Sample Design Files](#) on page 16.

Lessons

This module consists of the following lessons:

- [Overview](#) on page 139
- [Lesson 4-1: Working with Properties in the Properties Window in System Connectivity Manager](#) on page 140
- [Lesson 4-2: Working with Properties in Constraint Manager](#) on page 148
- [Lesson 4-3: Defining User Defined Properties](#) on page 156

Completion Time

1 hour for written lessons

Overview

Properties (also called attributes) are used to convey information about a design. Properties carry such information as the part number

System Connectivity Manager Tutorial

Module 4: Working with Properties

of a component, the voltage of a net and so on. Properties consist of a name and value. Some properties have a set of standard values that you can use; other properties support any value that you assign.

Properties added on components and nets in the design can also affect component placement and signal routing. This lets you specify physical layout requirements in the design capture stage itself.

System Connectivity Manager supports a predefined set of properties that you can add on design objects (components, nets or pins). You can also define custom (user-defined) properties and add them on design objects.

You can use the Properties window in System Connectivity Manager to work with properties on individual components, nets and pins in your design. You can also use Constraint Manager to capture and manage property information in your design. Constraint Manager provides a spreadsheet interface that helps you to quickly work with properties across your design.

In this module, you will learn to work with properties in System Connectivity Manager and in Constraint Manager.

Lesson 4-1: Working with Properties in the Properties Window in System Connectivity Manager

Overview

The Properties window in System Connectivity Manager allows you to work with properties on individual components, nets and pins in your design.

In this lesson, you will learn to work with properties in the Properties window in System Connectivity Manager.

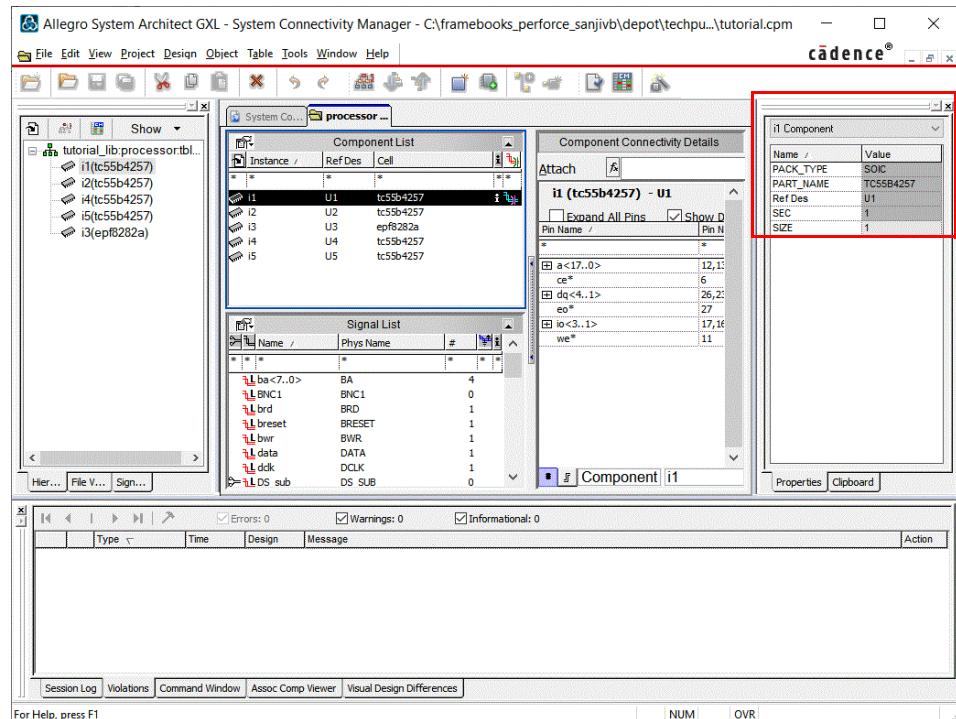
Procedure

1. Choose *View – Properties Window*.

System Connectivity Manager Tutorial

Module 4: Working with Properties

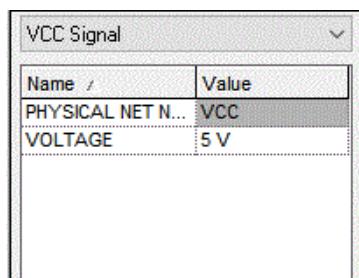
The Properties window appears on the right side of the System Connectivity Manager workspace.



The Properties window displays the properties on instance *i5* of the *tc55b4257* component because the instance is selected in the Component List. If not selected, you can click *i5* from the component list to select it.

2. Select the VCC signal in the Signal List.

The properties on the VCC signal are displayed in the Properties window.

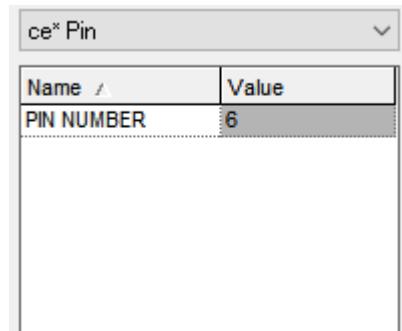


3. Select the ce* pin in the Component Connectivity Details pane.

System Connectivity Manager Tutorial

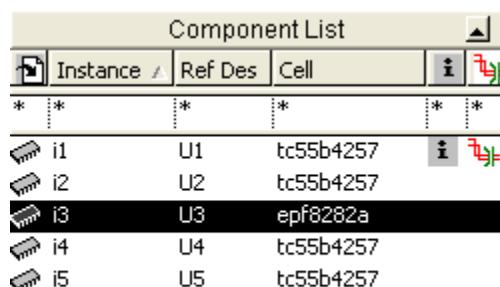
Module 4: Working with Properties

The properties on the `ce*` pin are displayed in the Properties window.



You will now add the `ROOM` property with the value `FPGA` on the `epf8282a` component. The `ROOM` property lets you control where parts are placed in the Allegro PCB Editor board.

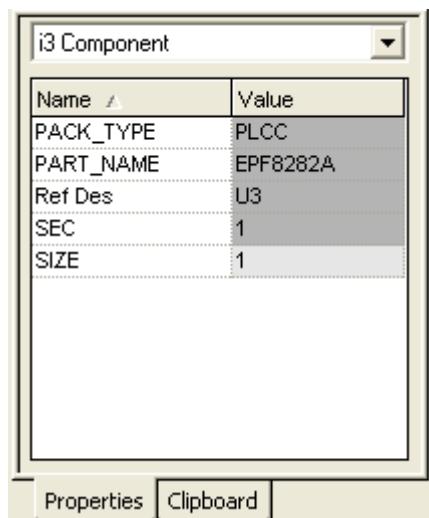
4. In the Component List, select the `epf8282a` component.



System Connectivity Manager Tutorial

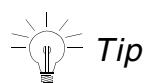
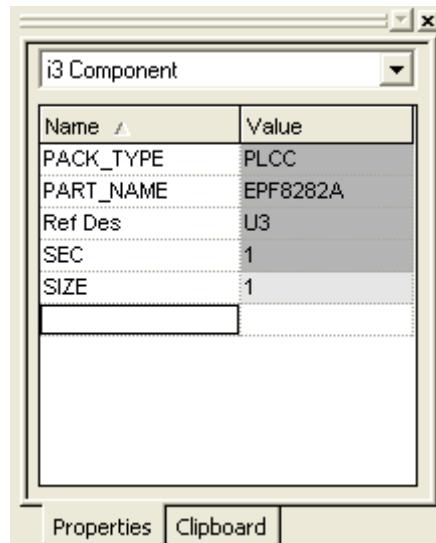
Module 4: Working with Properties

The properties on the component are displayed in the Properties window.



5. Click the right-mouse button in the Properties window and choose *Insert Property* from the shortcut menu.

A new row is added in the Properties window.

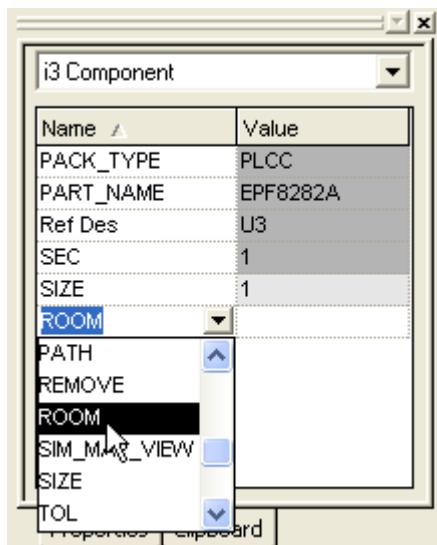


You can also press the *Insert* key to add a property.

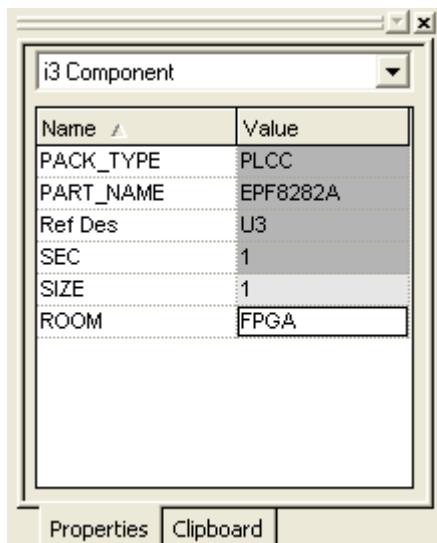
System Connectivity Manager Tutorial

Module 4: Working with Properties

6. Click in the *Name* column in the new row and choose ROOM from the drop-down list.



7. In the *Value* column, enter FPGA as the value for the ROOM property.



Similarly, you can select a signal in the Signal List or a pin in the Component Connectivity Details pane to display its properties in the Properties window and then add properties on the signal or pin.

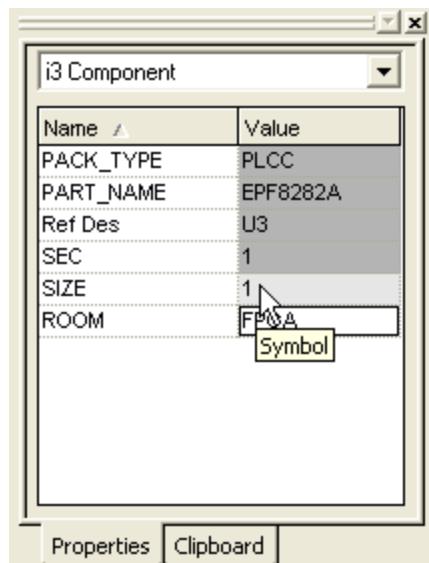
Note: You can copy property values from another component, signal or pin, or from another application such as Microsoft

System Connectivity Manager Tutorial

Module 4: Working with Properties

Excel, and paste it in the Properties window.

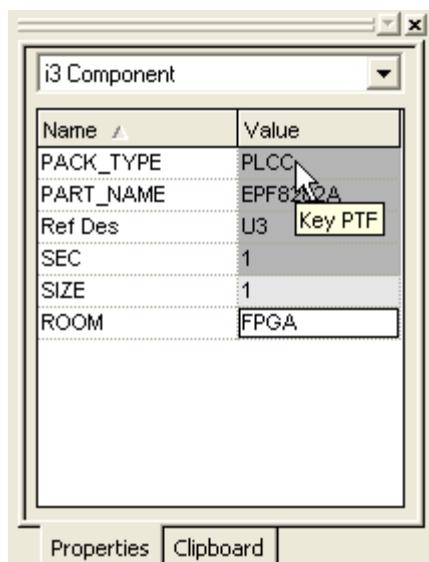
Note that the values for the PACK_TYPE, PART_NAME, Ref Des, SEC and SIZE properties are grayed out in the Properties window. You cannot modify the values for these properties because they are added on the symbol for the component, annotated from the physical part table, or are automatically assigned by System Connectivity Manager. If you place the mouse pointer over a property value, a tooltip appears displaying the origin of the property.



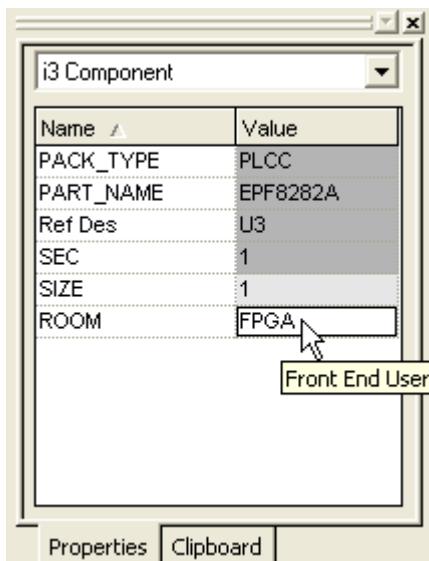
System Connectivity Manager Tutorial

Module 4: Working with Properties

In the figure above, the tooltip **Symbol** indicates that the **SIZE** property exists on the symbol for the **epf8282a** component.



In the figure above, the tooltip **Key PTF** indicates that the **PACK_TYPE** property is a key property that is annotated from the physical part table file. For more information on physical part table files, see [Lesson 1-3: Setting Up the Project](#) on page 40.

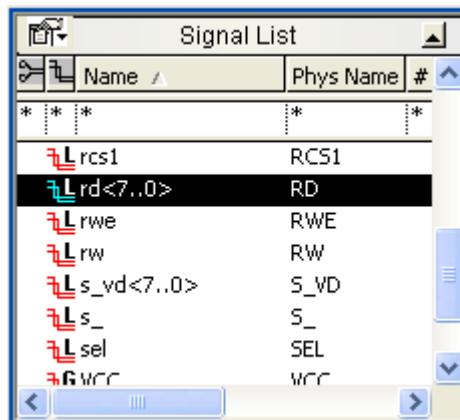


In the figure above, the tooltip **Front End User** indicates that you added the **ROOM** property in System Connectivity Manager.

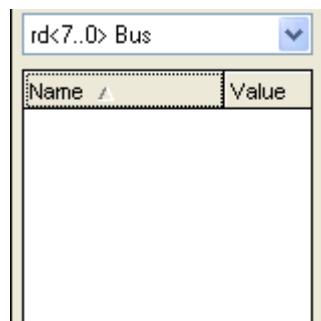
System Connectivity Manager Tutorial

Module 4: Working with Properties

8. In the Signal List, select the vectored signal (bus) `rd<7..0>`.

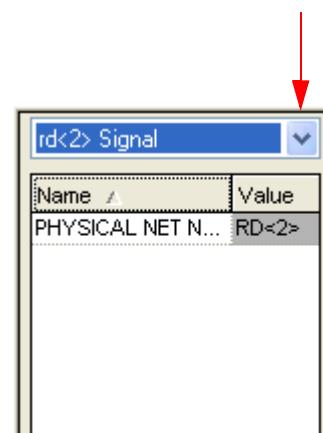


The Properties window appears as shown below.



Note: You cannot add properties on a vectored signal. You can only add properties on the bits of a vectored signal.

9. Click the drop-down list and select the bit `rd<2>`.



System Connectivity Manager Tutorial

Module 4: Working with Properties

The properties on the bit are displayed in the Properties window.
You can add properties on the bit.

Summary

You now know how to use the Properties window in System Connectivity Manager to view and add properties on components, signals and pins in the design.

For more information, see the [Working with Properties and Electrical Constraints](#) chapter of *System Connectivity Manager User Guide*.

Lesson 4-2: Working with Properties in Constraint Manager

Overview

Constraint Manager allows you to capture and manage property information in your design. Constraint Manager provides a spreadsheet interface that helps you to quickly work with properties across your design.

In this lesson, you will learn to work with properties in Constraint Manager.

Procedure

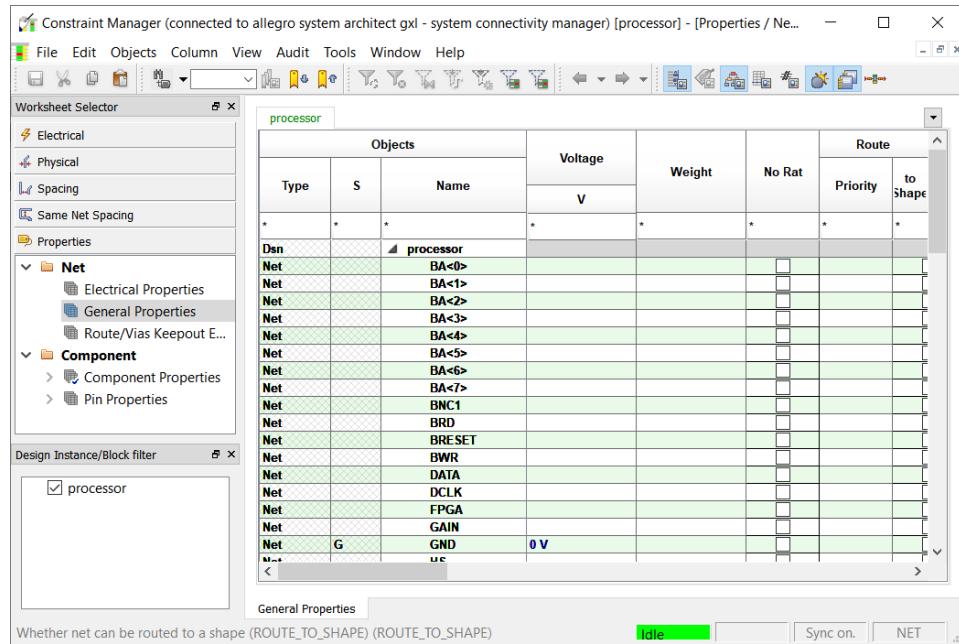
1. To open Constraint Manager from System Connectivity Manager, do one of the following:

- Click the *Edit Constraints and Properties* toolbar button ().
- Choose *Design – Edit Constraints*.

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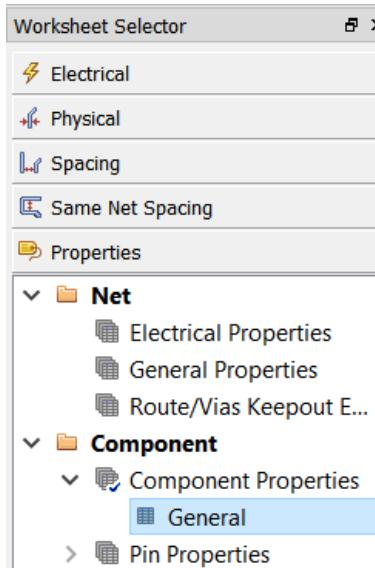
Module 4: Working with Properties

The Constraint Manager window appears.



The *General Properties* worksheet in the *Net* object folder lets you work with properties on nets in the design. Note that nets are displayed using physical net names in Constraint Manager.

The *General Properties* worksheet in the *Component* object folder lets you work with properties on components in the design.



System Connectivity Manager Tutorial

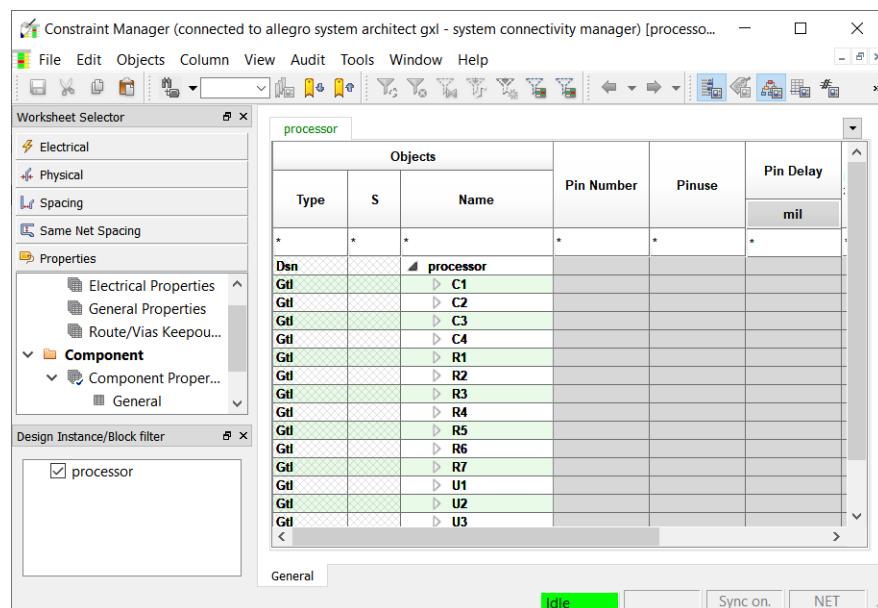
Module 4: Working with Properties

Note that the reference designators of components are displayed in Constraint Manager.

Note: To view the instance names of components, choose *Options* from the *View* menu in Constraint Manager, select the *Logical* option and click *Close*.

The changes you make to properties in System Connectivity Manager are displayed in Constraint Manager. Note that the ROOM property with the value FPGA you added on the epf8282a component using the Properties window in System Connectivity Manager is displayed in Constraint Manager. Similarly, the changes you make to properties in Constraint Manager are displayed in System Connectivity Manager.

The *Pin Properties* workbook in the *Component* object folder lets you work with properties on components pins.



The reference designators of components are displayed in the *Pin Properties* worksheet.

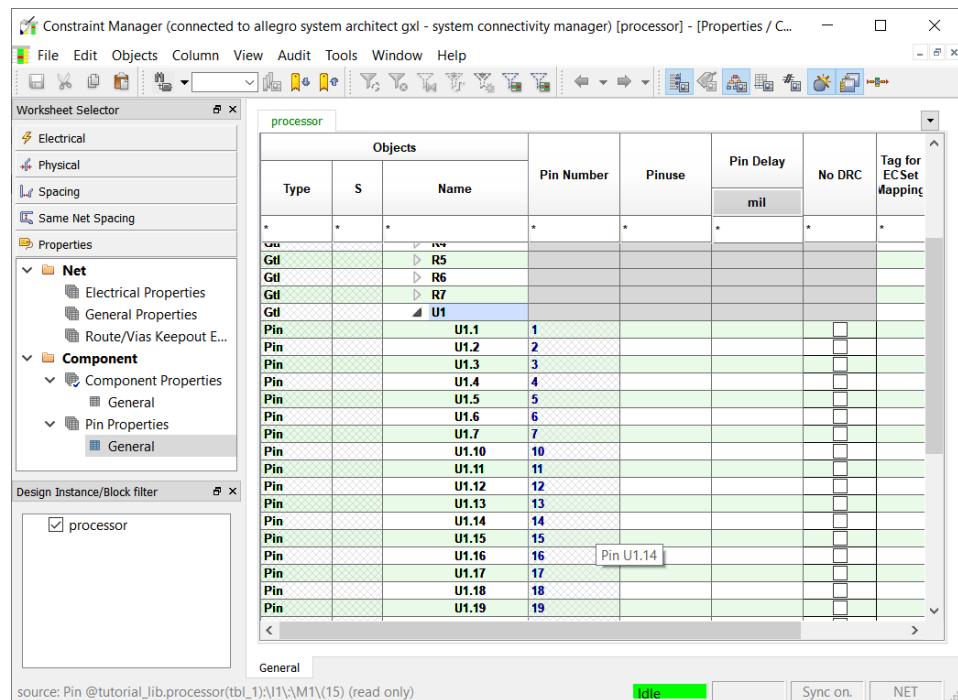
To view the pins of a component, click the expand icon (▶) next to the reference designator of the component.

2. Click the expand icon (▶) next to the reference designator U1.

System Connectivity Manager Tutorial

Module 4: Working with Properties

The pins on the component are displayed.



The screenshot shows the Constraint Manager interface with the title bar "Constraint Manager (connected to allegro system architect gxl - system connectivity manager) [processor] - [Properties / C...]" and various menu options like File, Edit, Objects, Column, View, Audit, Tools, Window, Help. On the left, there's a "Worksheet Selector" pane with sections for Electrical, Physical, Spacing, Same Net Spacing, and Properties. Under Properties, there are sections for Net (Electrical Properties, General Properties, Route/Vias Keepout E...), Component (Component Properties, General), and Pin Properties (General). A "Design Instance/Block filter" pane shows "processor" selected. The main area is a table titled "Objects" with columns: Type, S, Name, Pin Number, Pinuse, Pin Delay (with a dropdown set to mil), No DRC, and Tag for ECSet Mapping. The table lists pins for component U1, numbered 1 through 19. Pin U1.1 is highlighted with a yellow background. A tooltip "Pin U1.14" appears over Pin U1.16. The bottom status bar shows "source: Pin @tutorial_lib.processor(tbl_1)\U1\15 (read only)" and buttons for Idle, Sync on, and NET.

| Type | S | Name | Pin Number | Pinuse | Pin Delay | | No DRC | Tag for ECSet Mapping |
|-----------|---|-------|------------|-----------|-----------|----|--------|-----------------------|
| | | | | | mil | ns | | |
| Net | | R5 | | | | | | |
| Net | | R6 | | | | | | |
| Net | | R7 | | | | | | |
| Component | | U1 | | | | | | |
| Pin | | U1.1 | 1 | | | | | |
| Pin | | U1.2 | 2 | | | | | |
| Pin | | U1.3 | 3 | | | | | |
| Pin | | U1.4 | 4 | | | | | |
| Pin | | U1.5 | 5 | | | | | |
| Pin | | U1.6 | 6 | | | | | |
| Pin | | U1.7 | 7 | | | | | |
| Pin | | U1.10 | 10 | | | | | |
| Pin | | U1.11 | 11 | | | | | |
| Pin | | U1.12 | 12 | | | | | |
| Pin | | U1.13 | 13 | | | | | |
| Pin | | U1.14 | 14 | | | | | |
| Pin | | U1.15 | 15 | | | | | |
| Pin | | U1.16 | 16 | Pin U1.14 | | | | |
| Pin | | U1.17 | 17 | | | | | |
| Pin | | U1.18 | 18 | | | | | |
| Pin | | U1.19 | 19 | | | | | |

In the figure above, U1 . 1 indicates the pin with the number 1 on the component with the reference designator U1.

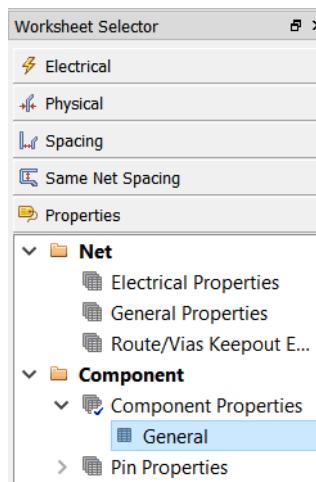
Note: To view the pin names, choose *Options* from the *View* menu in Constraint Manager, select the *Logical* option and click *Close*.

3. Now add properties on components in Constraint Manager.

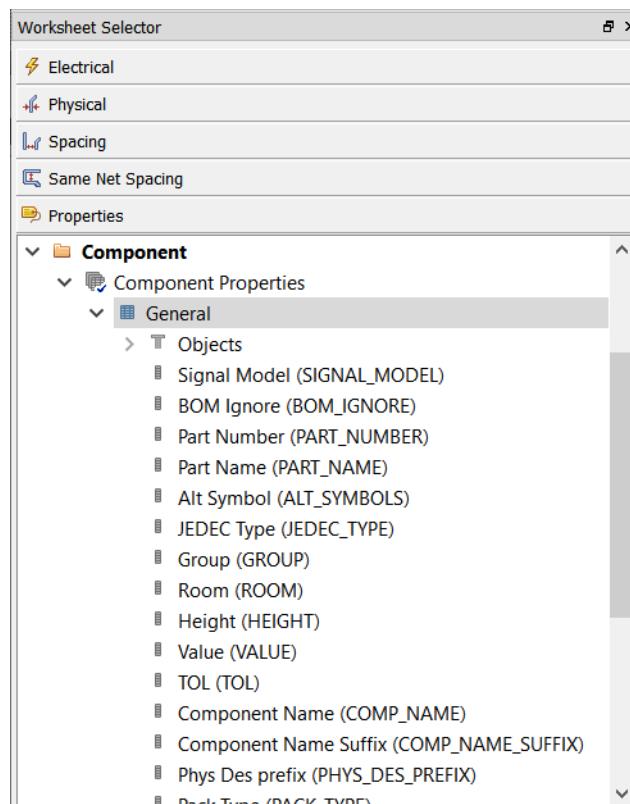
System Connectivity Manager Tutorial

Module 4: Working with Properties

a. Choose *Properties — Component — General*.



b. Right-click on *General* and choose *Customize Worksheets*. All visible columns are displayed under the General tree.



System Connectivity Manager Tutorial

Module 4: Working with Properties

- Click in the *Room* column next to the reference designator C1, press the *Shift* key, then click in the *Room* column next to the reference designator U2, to select the cells in the *Room* column as shown below.

| Objects | | | Signal Model | BOM Ignore | Part Number | Part Name | Alt Symbol | JEDEC Type | Group | Room |
|---------|---|-----------|--------------|------------|-------------|-----------|------------|------------|-------|------|
| Type | S | Name | | | | | | | | |
| * | * | * | | * | * | * | * | * | * | * |
| Dsn | | processor | | | | | | | | |
| Gtl | | C1 | | | | CAP | | | | |
| Gtl | | C2 | | | | CAP | | | | |
| Gtl | | C3 | | | | CAP | | | | |
| Gtl | | C4 | | | | CAP | | | | |
| Gtl | | R1 | DEFAULT... | | | RESD | | | | |
| Gtl | | R2 | DEFAULT... | | | RESD | | | | |
| Gtl | | R3 | | | | RESD | | | | |
| Gtl | | R4 | | | | RESD | | | | |
| Gtl | | R5 | DEFAULT... | | | RESD | | | | |
| Gtl | | R6 | | | | RESD | | | | |
| Gtl | | R7 | | | | RESD | | | | |
| Gtl | | U1 | | | | TC55B4257 | | | | |
| Gtl | | U2 | | | | TC55B4257 | | | | |
| Gtl | | U3 | | | | EPF8282A | | | | FPGA |
| Gtl | | U4 | | | | TC55B4257 | | | | |
| Gtl | | U5 | | | | TC55B4257 | | | | |

- Type MEMORY and press *Enter*.

The ROOM property with the value MEMORY is added on the selected components. The ROOM property lets you control where parts are placed in the Allegro PCB Editor board.

| Objects | | | Signal Model | BOM Ignore | Part Number | Part Name | Alt Symbol | JEDEC Type | Group | Room |
|---------|---|-----------|--------------|------------|-------------|-----------|------------|------------|-------|--------|
| Type | S | Name | | | | | | | | |
| * | * | * | | * | * | * | * | * | * | * |
| Dsn | | processor | | | | | | | | |
| Gtl | | C1 | | | | CAP | | | | MEMORY |
| Gtl | | C2 | | | | CAP | | | | MEMORY |
| Gtl | | C3 | | | | CAP | | | | MEMORY |
| Gtl | | C4 | | | | CAP | | | | MEMORY |
| Gtl | | R1 | DEFAULT... | | | RESD | | | | MEMORY |
| Gtl | | R2 | DEFAULT... | | | RESD | | | | MEMORY |
| Gtl | | R3 | | | | RESD | | | | MEMORY |
| Gtl | | R4 | | | | RESD | | | | MEMORY |
| Gtl | | R5 | DEFAULT... | | | RESD | | | | MEMORY |
| Gtl | | R6 | | | | RESD | | | | MEMORY |
| Gtl | | R7 | | | | RESD | | | | MEMORY |
| Gtl | | U1 | | | | TC55B4257 | | | | MEMORY |
| Gtl | | U2 | | | | TC55B4257 | | | | MEMORY |

- Add the ROOM property with the value MEMORY on the components with the reference designator U4 and U5.
- Switch to System Connectivity Manager.

System Connectivity Manager Tutorial

Module 4: Working with Properties

8. In the Component List, select instance i5 of the tc55b4257 component.

| Component List | | | | |
|----------------|----------|-----------|------|---|
| | Instance | Ref Des | Cell | |
| * | * | * | * | * |
| i1 | U1 | tc55b4257 | | |
| i2 | U2 | tc55b4257 | | |
| i3 | U3 | epf8282a | | |
| i4 | U4 | tc55b4257 | | |
| i5 | U5 | tc55b4257 | | |

The Properties window displays the ROOM property you added on the component instance in Constraint Manager.

| i5 Component | |
|--------------|-----------|
| Name | Value |
| PACK_TYPE | SOIC |
| PART_NAME | TC55B4257 |
| Ref Des | U5 |
| ROOM | MEMORY |
| SEC | 1 |
| SIZE | 1 |

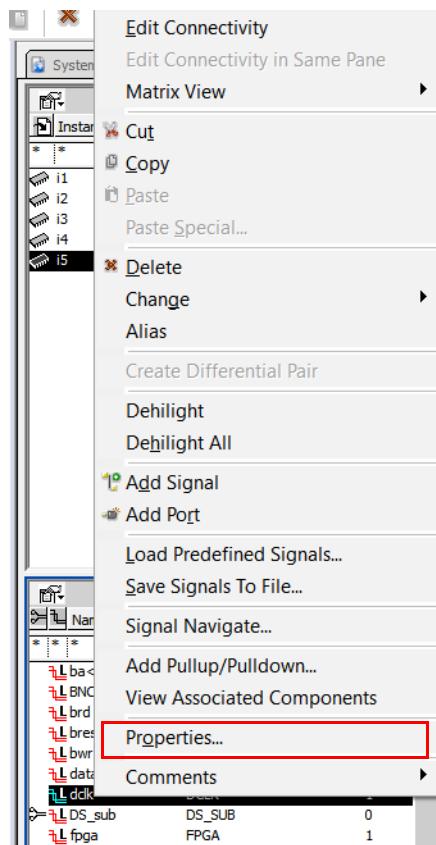
If you want to add a property on a specific component, net or pin in Constraint Manager, you can select the component, net or pin in System Connectivity Manager, click the right-mouse button and choose *Properties* to highlight the object in the corresponding property worksheet in Constraint Manager. Highlighting objects from System Connectivity Manager lets you quickly navigate to the required object in Constraint Manager. This is especially useful when working with properties in large designs where there are hundreds of components and nets in the design and when you are working with properties on pins of large pin-count devices.

9. Save the design.

System Connectivity Manager Tutorial

Module 4: Working with Properties

10. In the Signal List in System Connectivity Manager, right-click on the `dclk` signal and choose *Properties* from the shortcut menu.



The net DCLK is highlighted in the *General Properties* workbook in the *Net* object folder.

The screenshot shows the Constraint Manager workspace for the 'processor' component. The tree view on the left shows categories like Electrical, Physical, Spacing, Same Net Spacing, and Properties. Under Properties, the 'Net' object folder is expanded, showing sub-folders like Electrical Properties, General Properties, and Route/Vias Keepout Exception. The 'General Properties' folder is currently selected. The main table view on the right lists objects with columns for Type, S, Name, Voltage, and Weight. The 'DCLK' row is highlighted with a red box. Other rows include BA<0>, BA<1>, BA<2>, BA<3>, BA<4>, BA<5>, BA<6>, BA<7>, BNC1, BRD, BRESET, BWR, DATA, and FPGA.

| Type | S | Name | Voltage | Weight |
|------|---|-----------|---------|--------|
| | | | V | |
| Dsn | * | * | * | * |
| Net | | processor | BA<0> | |
| Net | | | BA<1> | |
| Net | | | BA<2> | |
| Net | | | BA<3> | |
| Net | | | BA<4> | |
| Net | | | BA<5> | |
| Net | | | BA<6> | |
| Net | | | BA<7> | |
| Net | | BNC1 | | |
| Net | | BRD | | |
| Net | | BRESET | | |
| Net | | BWR | | |
| Net | | DATA | | |
| Net | | DCLK | | |
| Net | | FPGA | | |

System Connectivity Manager Tutorial

Module 4: Working with Properties

This allows you to quickly add properties on specific components, nets and pins in the design.

Summary

You now know how to use Constraint Manager to work with properties on components, nets and pins in the design.

For more information, see the following:

- [Working with Properties chapter of System Connectivity Manager to Constraint Manager User Guide.](#)
- [Working with Properties and Electrical Constraints chapter of System Connectivity Manager User Guide.](#)

Lesson 4-3: Defining User Defined Properties

Overview

You can use an user defined property to capture a characteristic of an object. System Connectivity Manager and Constraint Manager do not perform any design rule checks or analysis on user defined properties; they facilitate communication of the design intent to down-stream tools in which you may want to manipulate the design objects associated with these properties.

System Connectivity Manager lets you define user defined properties. You can also define user defined properties in Constraint Manager.

In this lesson, you will learn to add a user defined property in System Connectivity Manager.

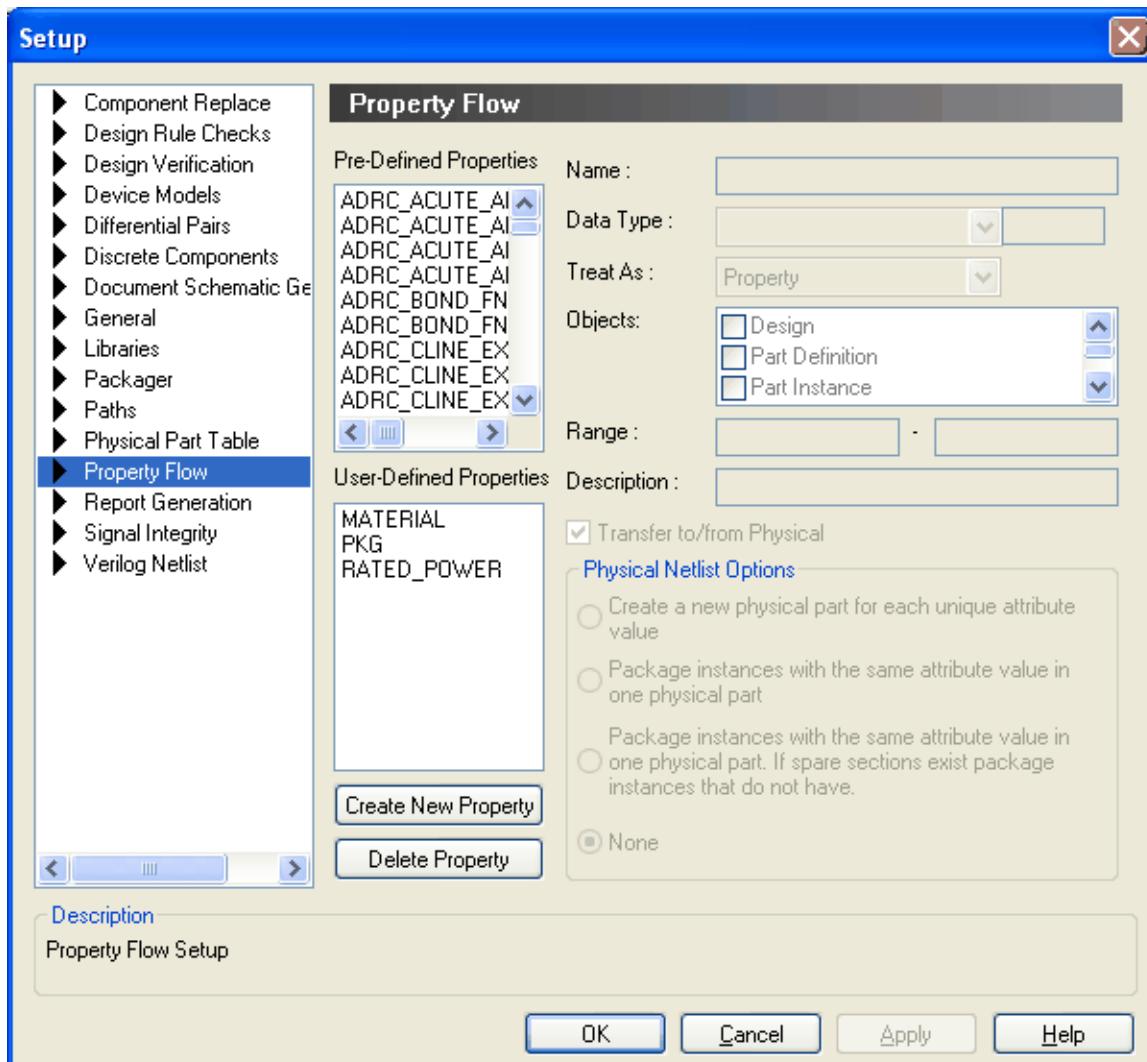
Procedure

1. In System Connectivity Manager, choose *Project – Settings*.
The Setup dialog box appears.

System Connectivity Manager Tutorial

Module 4: Working with Properties

2. Click the *Property Flow* tab.



The predefined set of properties supported by System Connectivity Manager are displayed in the *Pre-Defined Properties* list.

The user defined properties are displayed in the *User-Defined Properties* list.

3. Click the *Create New Property* button.
4. In the *Name* field, enter the property name as:
COST
5. Deselect all check boxes except Part Instance.

System Connectivity Manager Tutorial

Module 4: Working with Properties

As only the *Part Instance* check box is selected, you can add the COST property only on components in the design.

6. From the *Data Type* drop-down list, choose *String*.

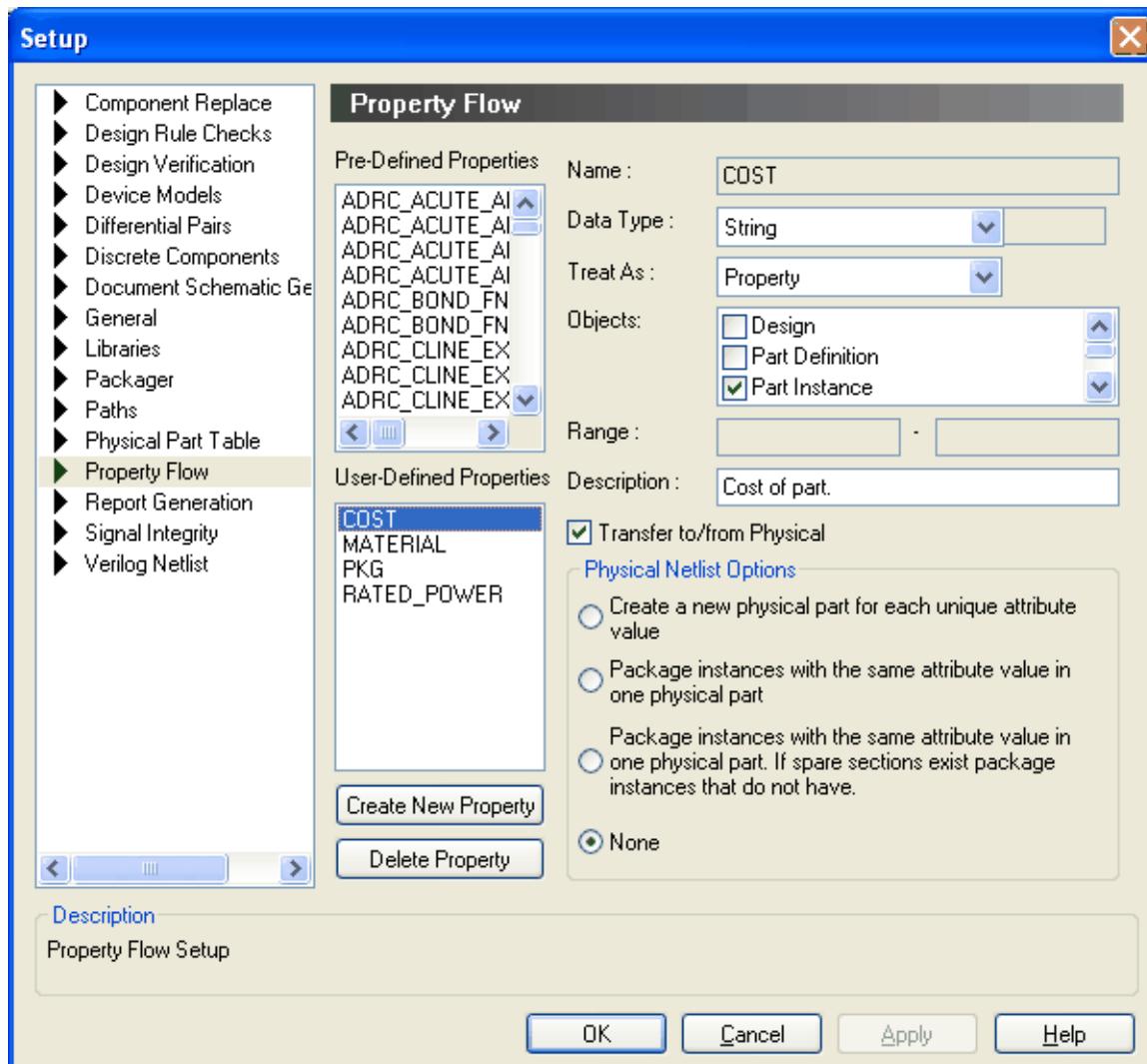
7. In the *Description* field, enter:

Cost of part.

8. Click *Apply*.

The COST property is displayed in the *User-Defined Properties* list.

9. Click on the COST property to view its definition.



System Connectivity Manager Tutorial

Module 4: Working with Properties

10. Click OK to close the Setup dialog box.

You will now add the COST property on the epf8282a component in the design.

11. In the Component List, select the epf8282a component.

| Component List | | | |
|----------------|---------|-----------|---|
| Instance | Ref Des | Cell | |
| * | * | * | * |
| i1 | U1 | tc55b4257 | |
| i2 | U2 | tc55b4257 | |
| i3 | U3 | epf8282a | |
| i4 | U4 | tc55b4257 | |
| i5 | U5 | tc55b4257 | |

12. Choose *View – Properties Window*.

The Properties window displays the properties on the epf8282a component.

| i3 Component | |
|--------------|----------|
| Name | Value |
| PACK_TYPE | PLCC |
| PART_NAME | EPF8282A |
| Ref Des | U3 |
| ROOM | FPGA |
| SEC | 1 |
| SIZE | 1 |

13. Click in the Properties window and press the *Insert* key.

A new row is added in the Properties window.

System Connectivity Manager Tutorial

Module 4: Working with Properties

14. Click in the *Name* column in the new row and choose MATERIAL from the drop-down list.

| i3 Component | |
|--------------|---------|
| Name | Value |
| SIZE | 1 |
| SEC | 1 |
| ROOM | FPGA |
| Ref Des | U3 |
| PART_NAME | EPF8282 |
| PACK_TYPE | PLCC |
| MATERIAL | |
| PACK_IGNORE | |
| PACK_SHORT | |
| PART_NUMBER | |
| PATH | |
| PKG | |

15. In the *Value* column, enter 3.25 as the value for the MATERIAL property.

| i3 Component | |
|--------------|---------|
| Name | Value |
| SIZE | 1 |
| SEC | 1 |
| ROOM | FPGA |
| Ref Des | U3 |
| PART_NAME | EPF8282 |
| PACK_TYPE | PLCC |
| MATERIAL | 3.25 |

Summary

You now know how to define user defined properties in System Connectivity Manager and add user defined properties on components, nets and pins in the design.

For more information, see the following:

- [Working with Properties and Electrical Constraints](#) chapter of *System Connectivity Manager User Guide* for details on working with user-defined properties in System Connectivity Manager.

System Connectivity Manager Tutorial

Module 4: Working with Properties

- Working with Properties chapter of the System Connectivity Manager to Constraint Manager User Guide for details on working with user-defined properties in Constraint Manager.

System Connectivity Manager Tutorial

Module 4: Working with Properties

Module 5: Working with Constraints

Prerequisite

If you have not completed all the lessons in the previous modules, you must open the `tutorial.cpm` project located at `<your_work_area>\modules\constraints\tutorial` in System Connectivity Manager and perform the steps described in this module.

For more information, see [Understanding the Sample Design Files](#) on page 16.

Lessons

This module consists of the following lessons:

- [Overview](#) on page 164
- [Lesson 5-1: Starting Constraint Manager from System Connectivity Manager](#) on page 164
- [Lesson 5-2: Assigning Constraints on a Net](#) on page 168
- [Lesson 5-3: Working with Electrical Constraint Sets](#) on page 173
- [Lesson 5-4: Assigning Signal Integrity Models](#) on page 181
- [Lesson 5-5: Applying Constraints from SigXplorer](#) on page 189
- [Lesson 5-6: Applying Physical and Spacing Constraints](#) on page 193

Completion Time

1 hour for written lessons

System Connectivity Manager Tutorial

Module 5: Working with Constraints

Overview

Allegro Constraint Manager is a workbook- and worksheet-based application used to manage high-speed constraints across all tools in the Cadence PCB and IC Package design flow.

You can use Constraint Manager with System Connectivity Manager to capture electrical constraint information early in the design cycle—right at the logic design stage.

Constraint Manager lets you define, view, and validate constraints at each step in the design flow, from design capture (in Allegro Design Entry HDL or System Connectivity Manager) to floorplanning (in Allegro PCB SI) to design realization (in Allegro PCB). You can also use Constraint Manager with SigXplorer to explore circuit topologies and derive electrical constraint sets which can include custom constraints, custom measurements, and custom stimulus.

In this module, you will learn to use Constraint Manager with System Connectivity Manager.

Lesson 5-1: Starting Constraint Manager from System Connectivity Manager

Overview

In this lesson, you will learn to start Constraint Manager from System Connectivity Manager.

Procedure

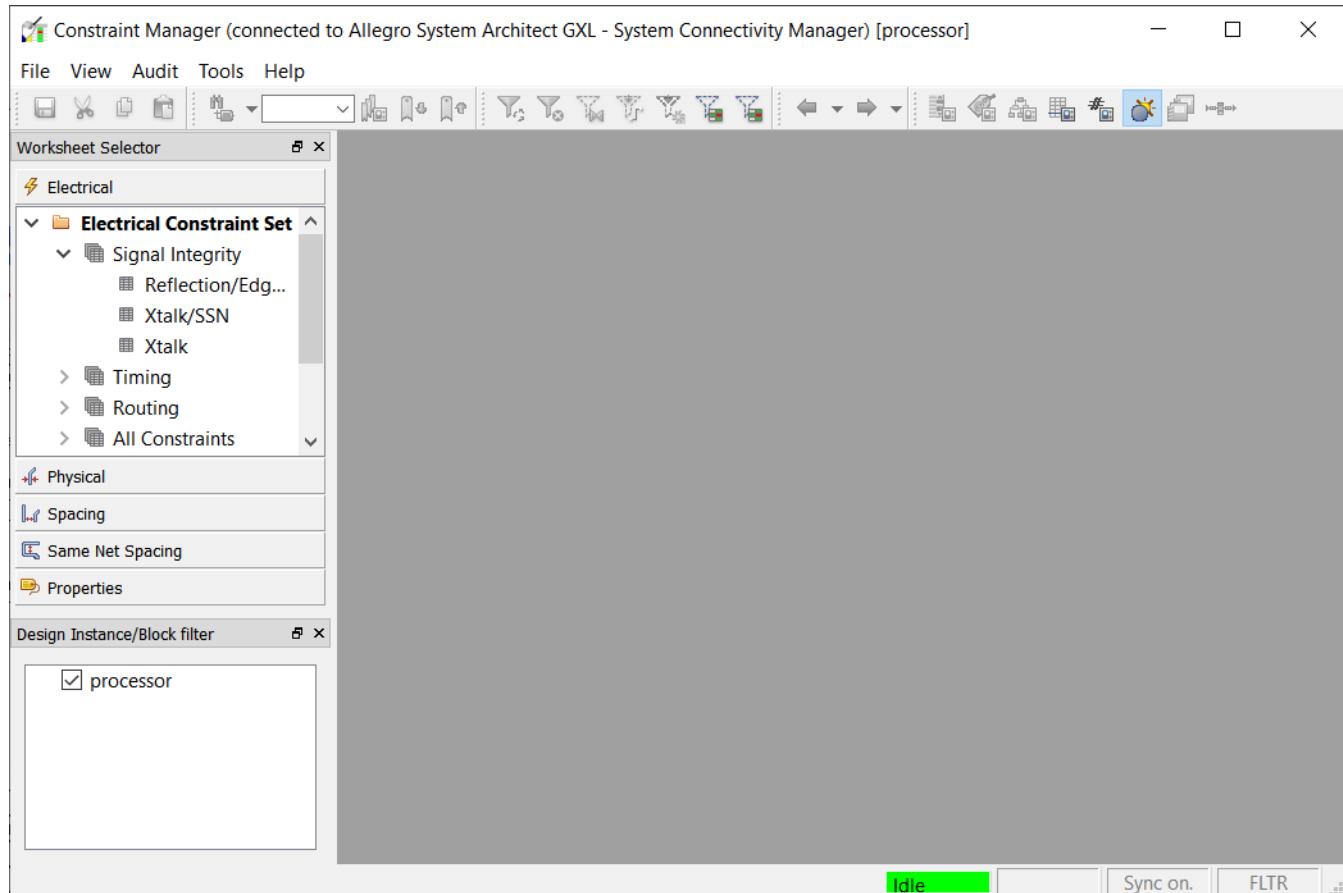
1. To start Constraint Manager, do one of the following:

- Click the  toolbar button.
- Choose *Design – Edit Constraints*.

System Connectivity Manager Tutorial

Module 5: Working with Constraints

The Constraint Manager window appears.



The Constraint Manager title bar displays (connected to Allegro System Architect). This indicates that Constraint Manager has been started from System Connectivity Manager.

Note: If you want to use Constraint Manager with System Connectivity Manager, you must start Constraint Manager only from System Connectivity Manager. If you start Constraint Manager from Allegro PCB Editor, you cannot use Constraint Manager to manage constraints in System Connectivity Manager.

The Constraint Manager user interface has two windows or panes. The left pane is the worksheet selector window. It lists constraints in the electrical, physical, and spacing domains. The net, component, and pin properties are listed in the Properties tab.

System Connectivity Manager Tutorial

Module 5: Working with Constraints

- The *Electrical Constraint Set* folder in the Electrical domain is used to create constraint rule sets. Think of this folder as a storage area of predefined constraint rules.
- The *Net* folder is used to assign individual constraint rules (or predefined rule sets) to nets. You can also attach constraint rules to pin pairs, buses, differential pairs, as so on.
- The worksheets in the Physical and Spacing domains is used to capture physical and spacing constraints. When Constraint Manager is invoked from System Connectivity Manager, you can only create new net classes in the physical and spacing domain, and specify nets to be included in these classes.

Note: Capturing physical and spacing constraints is supported when Constraint Manager is launched from Allegro PCB Editor.

- The worksheets in the Properties domain are used to assign properties on design components, such as nets, components, and pins.

System Connectivity Manager Tutorial

Module 5: Working with Constraints

The right pane is the worksheet editor window.

The screenshot shows the Allegro System Architect GXL - System Connectivity Manager software. The left pane is the 'Worksheet Selector' which contains a tree view of constraint sets and categories like Electrical, Net, Physical, Spacing, and Properties. A specific constraint set for 'processor' is selected. The right pane displays a detailed table for the 'processor' component, specifically for 'Single-line Impedance'. The table has columns for Type, S, Name, Referenced Electrical CSet, Target Ohm, Tolerance Ohm, Actual Ohm, and Margin Ohm. Numerous rows list various nets and their associated impedance values. At the bottom of the right pane, there are tabs for Wiring, Vias, Impedance, Min/Max Propagation Delays, Total Etch Length, Differential Pair, and Relative Propagation Delay. The 'Impedance' tab is currently selected. A status bar at the bottom indicates 'Idle'.

You can expand each folder in the left pane to view their associated workbooks. Each workbook contains one or more worksheets. The selected worksheet is displayed in the right pane. Each workbook deals with a particular category of design rules: Signal Integrity, Timing, and Routing. To attach routing rules to nets in the design, expand the *Net* folder, and edit the worksheets stored inside the *Routing* workbook.

System Connectivity Manager Tutorial

Module 5: Working with Constraints

Summary

You now know how to start Constraint Manager from System Connectivity Manager. You also learned about the folders, workbooks and worksheets in Constraint Manager.

For more information, see the following:

- [Allegro Constraint Manager Reference](#) for details on each worksheet in Constraint Manager.
- [Allegro Platform Constraint Reference](#) for details on each constraint in Constraint Manager.

Lesson 5-2: Assigning Constraints on a Net

Overview

While designing the schematic for your design, you might have several design constraints such as length and impedance on the critical nets in the design. These constraints might have been given to you by the Signal Integrity engineer. These translate to the length of critical nets and therefore to the propagation delay of the signals passing through them.

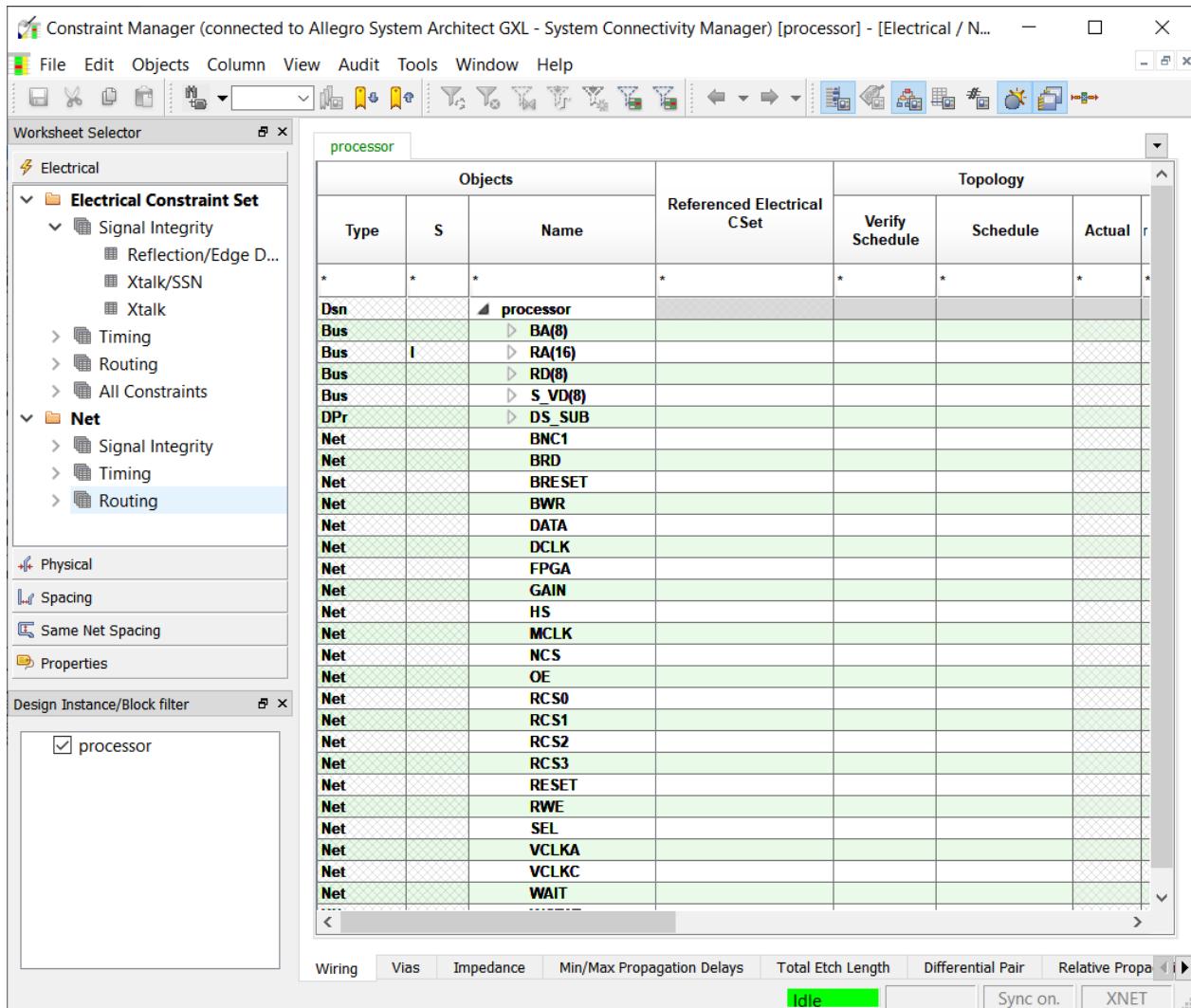
In this lesson, you will learn to set the minimum and maximum propagation delay constraint for a net.

System Connectivity Manager Tutorial

Module 5: Working with Constraints

Procedure

1. In the *Net* folder of the *Electrical* domain, double-click on the *Routing* workbook.



The worksheets in the *Routing* workbook are displayed. Note that nets are displayed using physical net names in Constraint Manager.

2. Click on the *Min/Max Propagation Delays* worksheet.

You will now set the minimum and maximum propagation delay constraint for the net named `rwe`. First, you will set the delay between all the drivers and receivers of net `rwe`. Then, for a

System Connectivity Manager Tutorial

Module 5: Working with Constraints

specific driver and receiver pair, we will set a different delay value.

You can locate the `rwe` net in the *Min/Max Propagation Delays* worksheet or select the net in the Signal List in System Connectivity Manager to highlight the net in the *Min/Max Propagation Delays* worksheet.

3. In the Signal List in System Connectivity Manager, select the `rwe` net.

Note that the net `rwe` has the physical net name `RWE`. This physical net name is displayed in Constraint Manager.

| | | |
|----------------|-------|----|
| ↳ L mdk | MCLK | 1 |
| ↳ L ncs | NCS | 1 |
| ↳ L NC | | 0 |
| ↳ L oe | OE | 1 |
| ↳ L ra<15..0> | RA | 80 |
| ↳ L rcs0 | RCS0 | 3 |
| ↳ L rcs1 | RCS1 | 3 |
| ↳ L rcs2 | RCS2 | 1 |
| ↳ L rcs3 | RCS3 | 1 |
| ↳ L rd<7..0> | RD | 32 |
| ↳ L reset | RESET | 1 |
| ↳ L rwe | RWE | 5 |
| ↳ L s_vd<7..0> | S_VD | 8 |
| ↳ L sel | SEL | 1 |
| ↳ G VCC | VCC | 0 |
| ↳ L vdka | VCLKA | 1 |
| ↳ L vdkc | VCLKC | 1 |
| ↳ L wait | WAIT | 1 |
| ↳ L wstat | WSTAT | 1 |

System Connectivity Manager Tutorial

Module 5: Working with Constraints

See that the net is highlighted in the *Min/Max Propagation Delays* worksheet in Constraint Manager.

| Type | S | Name | Referenced Electrical CSet | Pin Pairs | Pin Delay | |
|------|---|------------|----------------------------|---------------------------|-----------|-------|
| | | | | | Pin 1 | Pin 2 |
| FLTR | * | * | * | * | * | * |
| Net | | DCLK | | | | |
| Net | | FPGA | | | | |
| Net | | GAIN | | | | |
| Net | | HS | | | | |
| Net | | MCLK | | | | |
| Net | | NCS | | | | |
| Net | | OE | | | | |
| Net | | RCS0 | | | | |
| Net | | RCS1 | | | | |
| Net | | RCS2 | | | | |
| Net | | RCS3 | | | | |
| Net | | RESET | | | | |
| Net | | RWE | | | | |
| PPr | | U1.11:R2.2 | | | | |
| Net | | SEL | | | | |
| Net | | VCLKA | | | | |
| Net | | VCLKC | | | | |
| Net | | WAIT | | All Drivers/All Receivers | | |
| XNet | | WSTAT | | | | |

Highlighting nets from System Connectivity Manager lets you quickly navigate to the required net in the selected worksheet in Constraint Manager. This is especially useful in large designs where there are hundreds of nets in the design.

4. In the *Prop Delay* column, enter the minimum propagation delay for the net RWE as:

0.9

5. In the *Prop Delay* column, enter the maximum propagation delay for the net RWE as:

1.1

| | | | | |
|-----|---------|---------------------------|---------|---------|
| Net | RWE | All Drivers/All Receivers | 0.9 mil | 1.1 mil |
| Net | Net RWE | | | |

System Connectivity Manager Tutorial

Module 5: Working with Constraints

The default unit of value for the propagation delay constraint is ns (nanoseconds). This means that the signal on the net RWE must have a propagation delay of at least 0.9 ns before it reaches any destination, and that the signal must reach any destination within 1.1 ns after it is available on the net RCS0.

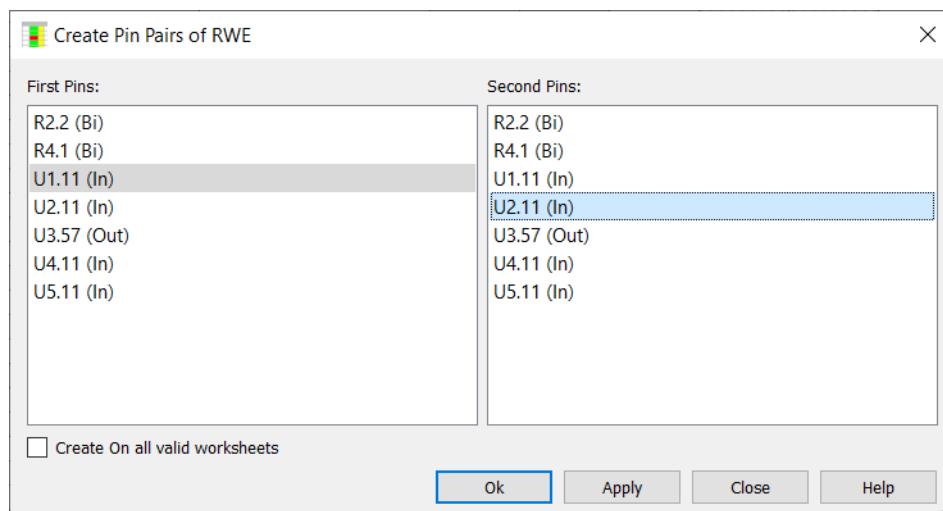
Note that in the *Pin Pairs* column, *All Drivers/All Receivers* gets selected automatically. This means that the propagation delay has been set between all the drivers and receivers of the signal on the net RWE.

6. Click net RWE and choose *Objects – Create – Pin Pair*.

The Create Pin Pairs of RCS0 for propagation delay dialog box appears. The *First Pins* column lists the driver pins connected to the net RWE. The *Second Pins* column list the receiver pins connected to the net RWE.

7. In the *First Pins* column, click U2 . 2.

8. In the *Second Pins* column, click U2 . 5.



9. Click *OK* to create the pin pair.

The pin pair U2 . 2 : U2 . 5 is displayed under the net RW in the Constraint Manager window.

| | | | | |
|----|-------------|---------------------------|---------|---------|
| at | RWE | All Drivers/All Receivers | 0.9 mil | 1.1 mil |
| Pr | U1.11:R2.2 | | 0.9 mil | 0.1 ns |
| Pr | U1.11:U2.11 | | 0.9 mil | 1.1 mil |
| st | SEL | | | |

System Connectivity Manager Tutorial

Module 5: Working with Constraints

The propagation delay constraint on the `RW` net is inherited by the pin pair. You can override the inherited constraint values.

10. Change the value in the *Min* column for the pin pair from `0.9 ns` to `0.8 ns`.
11. Change the value in the *Max* column for the pin pair from `1.1 ns` to `1.0 ns`.

Summary

You now know how to assign constraints on nets. You also learned to create a pin pair and override the constraint inherited by the pin pair from a net.

For more information, see the following:

- [System Connectivity Manager to Constraint Manager User Guide](#) for details on how to use Constraint Manager to capture constraints for a design created using System Connectivity Manager.
- [Allegro Constraint Manager User Guide](#) for details on using Constraint Manager.

Lesson 5-3: Working with Electrical Constraint Sets

Overview

You can identify the critical nets in your design and then identify constraints that are applicable to all of them. You can then define those constraints together in an ECSet and assign the ECSet on each of the critical nets. Thus, an ECSet can be used to define a generic set of rules applicable to a number of nets. If your design requirement changes at a later point in time, you can edit the constraints on the ECSet; all the nets referencing the ECSet shall inherit the changed ECSet automatically. Thus, using ECSets is a very efficient way of capturing constraints.

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Module 5: Working with Constraints

Another use of ECSets is in the case of design reuse. If you are reusing a design that has ECSets defined for its critical nets, you can import the ECSets into your new design; this saves a lot of rework.

The main advantages of an ECSet are:

- The ECSet can be assigned to many nets simultaneously.
- You can capture any or all electrical constraints in one ECSet.
- A change in a constraint in an ECSet is automatically inherited by the objects that reference the ECSet.
- You can override the constraints inherited from an ECSet.
- You can assign a different ECSet if the requirements change.

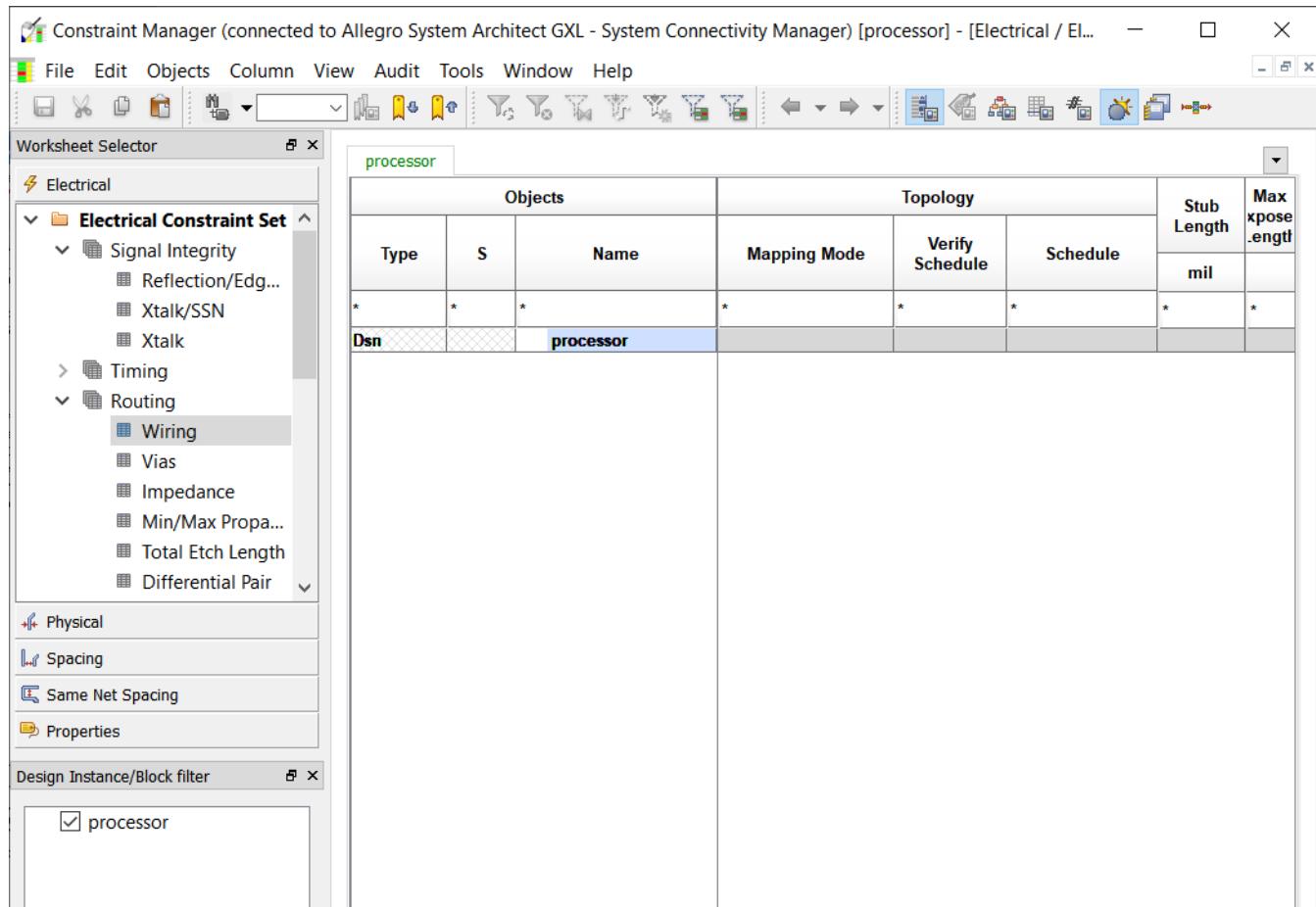
In this lesson, you will create an ECSet named `CRITICAL` and assign it on the bus `S_VD`. You will then override the constraints inherited from the ECSet on a bit of the bus.

System Connectivity Manager Tutorial

Module 5: Working with Constraints

Procedure

1. In the Constraint Manager window, click the *Routing* workbook in the *Electrical Constraint Set* folder.



2. Choose *Objects – Create – Electrical CSet*.

The Create Electrical CSet dialog box appears.

3. Enter the ECSet name as:

CRITICAL

4. Click *OK*.

5. In the *Objects* column, click on the sign next to the *processor* design.

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Module 5: Working with Constraints

The design expands to show the name of the new ECSet.

| processor | | | | | | | | |
|-----------|---|-----------|--------------|-----------------|----------|-------------|--------------------|--|
| Objects | | | Topology | | | Stub Length | Max Exposed Length | |
| Type | S | Name | Mapping Mode | Verify Schedule | Schedule | | | |
| * | * | * | * | * | * | * | * | |
| Dsn | | processor | | | | | | |
| ECS | | CRITICAL | | | | | | |

6. Click the *Wiring* worksheet in the *Routing* workbook in the *Electrical Constraint Set* folder.

You will now specify the wiring rules for the ECSet.

7. Do the following:

- a. Click in the *Verify Schedule* field, and select *Yes*.
- b. Click in the *Schedule* field, and select *Source-load Daisy-chain*.
- c. Click in the *Stub Length* field and enter 150.
- d. Click in the *Max Exposed Count* field and enter 4.
- e. Click in the *Max Parallel* field.

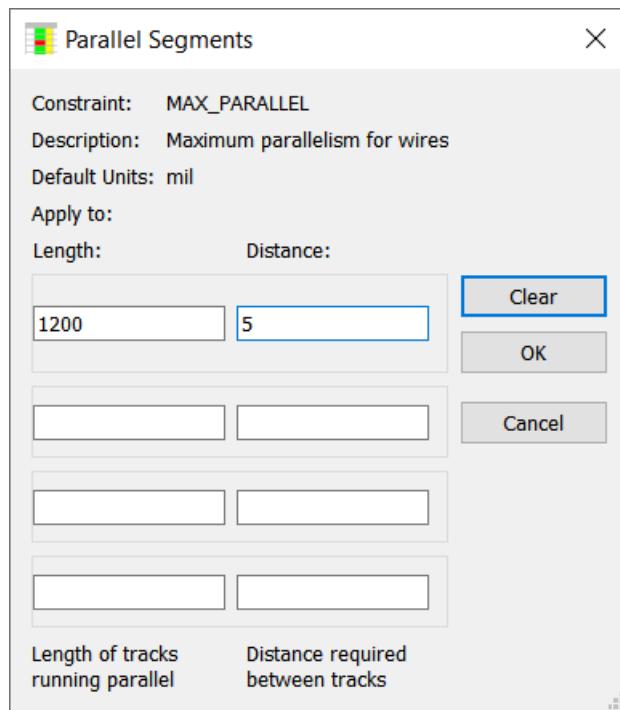
The Parallel Segments dialog box appears.

- f. Click in the first *Length* field and type 1200.

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Module 5: Working with Constraints

- g. Click in the *Distance* field next to the first *Length* field and type 5.



- h. Click OK.

The *Wiring* worksheet is modified as shown below:

| Objects | | | Topology | | | Stub Length | Max Exposed Length | Max Parallel | Layer Sets |
|---------|---|-----------|--------------|-----------------|-------------------|-------------|--------------------|--|------------|
| Type | S | Name | Mapping Mode | Verify Schedule | Schedule | | | | |
| * | * | * | * | * | * | * | * | * | * |
| Dsn | | processor | | | | | | | |
| ECS | | CRITICAL | | Yes | Source-load Da... | 150.00 | 4.00 | 0.00:0.00:0.00:0.00:0.00:0.00:1200.00:5.00 | |

8. Click the *Impedance* worksheet in the *Routing* workbook in the *Electrical Constraint Set* folder.

You will now specify the impedance rules for the ECSet.

9. Do the following:

- a. Click in the *Target* field and enter 65.
- b. Click in the *Tolerance* field and enter 5.

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Module 5: Working with Constraints

The *Impedance* worksheet appears as shown below:

| Objects | | | Single-line Impedance | |
|---------|---|-----------|-----------------------|-----------|
| Type | S | Name | Target | Tolerance |
| * | * | * | Ohm | Ohm |
| Dsn | | processor | * | * |
| ECS | | CRITICAL | 65 | 5 % |

10. Click the *Min/Max Propagation Delay* worksheet in the *Routing* workbook in the *Electrical Constraint Set* folder.

You will now specify the delay rules for the ECSet.

11. Do the following:

- a. Click in the *Min Delay* field and enter:

0 . 8

- b. In the *Max Delay* field, enter:

1 . 2

You used the *Routing* workbook in the *Electrical Constraint Set* folder to define the following rules:

- A source-load daisy chain schedule - a special routing sequence based on pin type.
- A stub length rule - 150 mils.
- A maximum vias per net rule - 4 maximum.
- A parallelism rule - two nets 5 mils apart cannot be adjacent more than 1200 mils.
- An impedance rule - 65 ohms.
- A Min/Max delay rule - the time taken for a signal to travel from the driver to the closest receiver must be at least 0.8 nanoseconds, and the time taken for the signal to travel to the furthest receiver not more than 1.2 nanoseconds.

These rules are stored in the ECSet named CRITICAL. You will now assign the ECSet named CRITICAL on the bus S_VD (8).

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Module 5: Working with Constraints

12. Click the *Wiring* worksheet in the *Routing* workbook in the *Net* folder.
13. Click on the Referenced Electrical CSet column next to the bus *S_VD(8)*.
The down-arrow button appears.
14. Click the drop-down list and choose *CRITICAL*.

| Objects | | | Referenced Electrical CSet |
|---------|---|-----------|----------------------------|
| Type | S | Name | |
| * | * | * | * |
| Dsn | | processor | |
| Bus | | BA(8) | |
| Bus | I | RA(16) | |
| Bus | | RD(8) | |
| Bus | | S_VD(8) | CRITICAL |
| DPr | | DS_SUB | |

The ECSets are assigned on the bus and the constraints on the ECSets are displayed on the bus.

15. Click on the sign next to the bus *S_VD*.

The constraints on the ECSets appear as inherited values on the bits of the bus *S_VD*.

| | | | | | | | | | |
|-----------|----------|-----|---------------------|--|--------|--|------|--|---------------------|
| ▲ S_VD(8) | CRITICAL | Yes | Source-load Dais... | | 150.00 | | 4.00 | | 0.00:0.00:0.00:0... |
| S_VD<0> | CRITICAL | Yes | Source-load Dais... | | 150.00 | | 4.00 | | 0.00:0.00:0.00:0... |
| S_VD<1> | CRITICAL | Yes | Source-load Dais... | | 150.00 | | 4.00 | | 0.00:0.00:0.00:0... |
| S_VD<2> | CRITICAL | Yes | Source-load Dais... | | 150.00 | | 4.00 | | 0.00:0.00:0.00:0... |
| S_VD<3> | CRITICAL | Yes | Source-load Dais... | | 150.00 | | 4.00 | | 0.00:0.00:0.00:0... |
| S_VD<4> | CRITICAL | Yes | Source-load Dais... | | 150.00 | | 4.00 | | 0.00:0.00:0.00:0... |
| S_VD<5> | CRITICAL | Yes | Source-load Dais... | | 150.00 | | 4.00 | | 0.00:0.00:0.00:0... |
| S_VD<6> | CRITICAL | Yes | Source-load Dais... | | 150.00 | | 4.00 | | 0.00:0.00:0.00:0... |
| S_VD<7> | CRITICAL | Yes | Source-load Dais... | | 150.00 | | 4.00 | | 0.00:0.00:0.00:0... |

This is because, constraints assigned on a bus are automatically inherited by the bits of the bus.

16. Click the *Impedance* worksheet in the *Routing* workbook in the *Net* folder.

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Module 5: Working with Constraints

17. Click in the *Target* field next to the bit S_VD<4> and enter 60.

| processor | | | | | |
|-----------|----------|----|-----|--|--|
| S_VD(8) | CRITICAL | 65 | 5 % | | |
| S_VD<7> | CRITICAL | 65 | 5 % | | |
| S_VD<6> | CRITICAL | 65 | 5 % | | |
| S_VD<5> | CRITICAL | 65 | 5 % | | |
| S_VD<4> | CRITICAL | 60 | 5 % | | |
| S_VD<3> | CRITICAL | 65 | 5 % | | |
| S_VD<2> | CRITICAL | 65 | 5 % | | |
| S_VD<1> | CRITICAL | 65 | 5 % | | |
| S_VD<0> | CRITICAL | 65 | 5 % | | |

The constraint values on the bit S_VD<4> appear in blue color because the constraints are overridden on the bit.

18. Close the Constraint Manager.

Summary

You now know how to use create an ECSet and assign it on a net. You also learned the following:

- Constraints assigned on an ECSet are automatically inherited by the objects on which the ECSet is assigned.
- Constraints assigned on a bus are automatically inherited by the bits of the bus.
- How to override an inherited constraint.

For More Information

See:

[Allegro Constraint Manager User Guide](#) for more information on working with ECSets.

System Connectivity Manager Tutorial

Module 5: Working with Constraints

Lesson 5-4: Assigning Signal Integrity Models

Overview

System Connectivity Manager lets you assign signal integrity (SI) models to components and pins in your design during the design capture phase. You can then use SigXplorer to perform topology exploration and analyze the nets in your design for signal integrity issues. This helps you correct signal integrity issues early in the design cycle.

You can manually assign existing signal models to components (such as IC devices) and pins. You can also automatically generate and assign signal models for all two-pin discrete components (resistors, capacitors, and inductors) in your design.

In this lesson, you will learn to assign a signal integrity model on a component and automatically generate models for the two pin discrete components (resistors, capacitors and inductors) in the design.

Multimedia Demonstration



A Flash-based multimedia demonstration of this module, [Assigning Signal Integrity Models in System Connectivity Manager](#), is available on Cadence Online Support.

Procedure

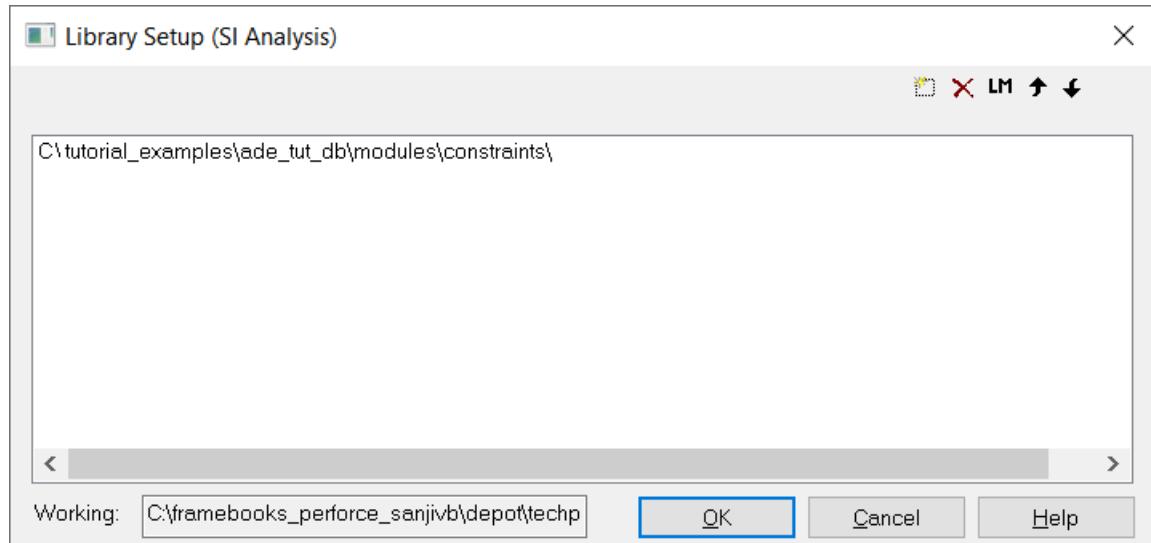
Before you can assign signal integrity models on components and pins, you must setup the signal integrity model libraries for your project.

1. In System Connectivity Manager, choose *Tools – Signal Integrity – SI Library Setup*.

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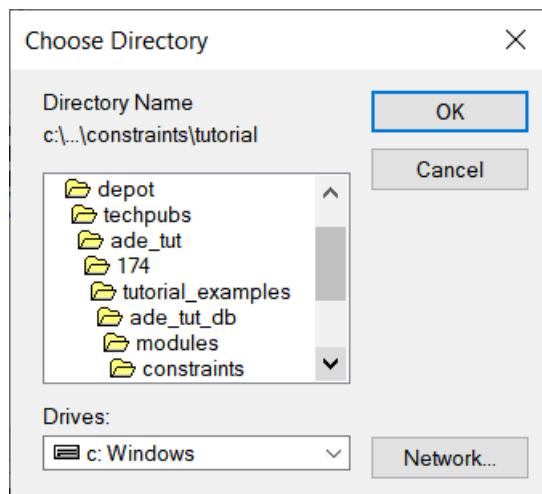
The Library Setup (SI Analysis) dialog box appears.



We will now setup a signal integrity model library named `tutorial.dml` for the project.

2. Click .

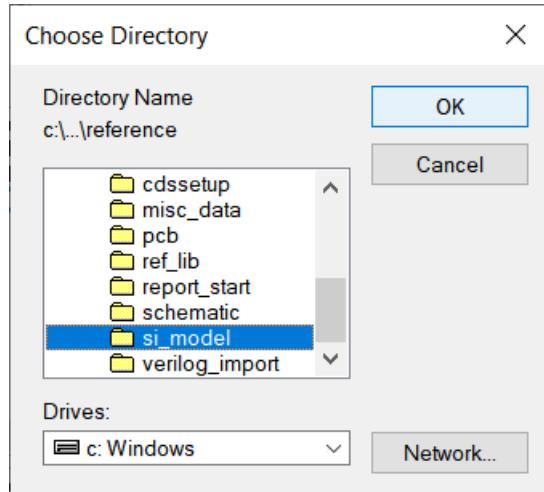
A dialog box appears.



3. Double-click *ade_tut - reference* and select *si_model*.

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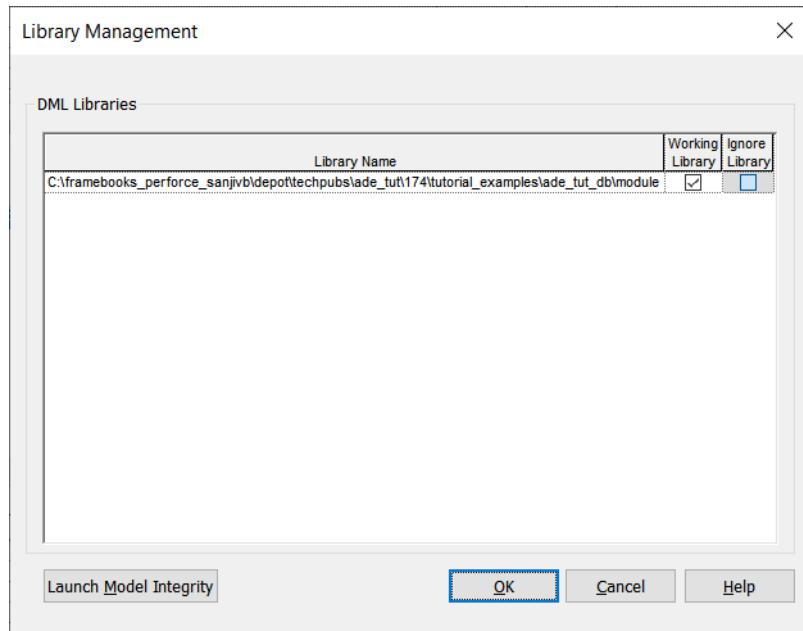
Module 5: Working with Constraints



4. Click **OK**.

The path is displayed in the Library Setup (SI Analysis) dialog box.

5. Click **LM**. to view the added .dml file.



6. Click **OK** to close the dialog box.

7. Add an instance of the ds901v031tm component, with PACK_TYPE as SOIC16, from the classlib library and close Part Information Manager.

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8. Connect the pins of the component as shown below.

| Component Connectivity Details | | | | | |
|--|----|---|--|--------|------|
| Attach | | Component Connectivity Details | | | |
| | | i7 (ds90lv031tm) - U6 | | | |
| <input type="checkbox"/> Expand All Pins | | <input checked="" type="checkbox"/> Show Differential Pairs | <input checked="" type="checkbox"/> Show Vectors | | |
| Pin Name | / | Pin Number | Pin Type | Signal | Terr |
| * | * | * | * | * | * |
| din1 | 1 | Input | | | |
| din2 | 7 | Input | | | |
| din3 | 9 | Input | | | |
| din4 | 15 | Input | wstat | | |
| dout1* | 3 | Output | vdka | | |
| dout1 | 2 | Output | vdkb | | |
| dout2* | 5 | Output | | | |
| dout2 | 6 | Output | | | |
| dout3* | 11 | Output | | | |
| dout3 | 10 | Output | | | |
| dout4* | 13 | Output | | | |
| dout4 | 14 | Output | | | |
| en* | 12 | Input | | | |
| en | 4 | Input | | | |

For more information on adding components in the design and connecting pins to signals, see [Module 2: Working with Components and Connectivity](#).

9. Save the design.

You will now assign a signal integrity model on the ds90lv031tm component and see how Constraint Manager creates a model-defined differential pair object when you assign the signal integrity model.

10. Select the ds90lv031tm component in the Component List.

| Component List | | | | | |
|----------------|---------|-------------|---|---|---|
| Instance | Ref Des | Cell | | | |
| * | * | * | * | * | * |
| i1 | U1 | tc55b4257 | | | |
| i2 | U2 | tc55b4257 | | | |
| i3 | U3 | epf8282a | | | |
| i4 | U4 | tc55b4257 | | | |
| i5 | U5 | tc55b4257 | | | |
| i6 | U6 | ds90lv031tm | | | |

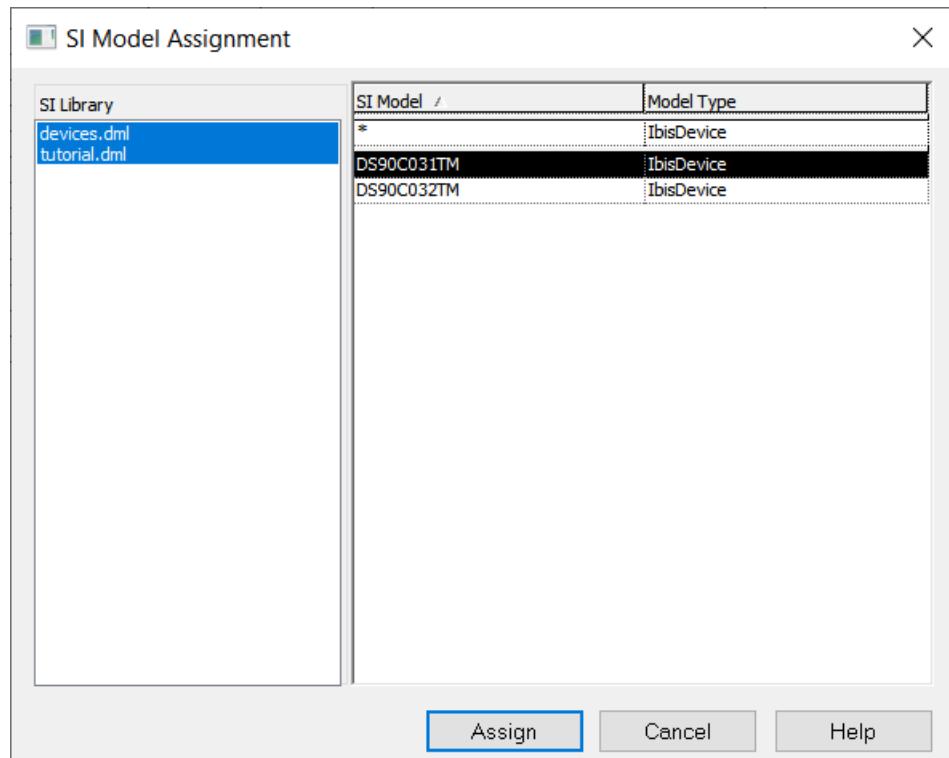
11. Choose Object – SI Models – Assign Model.

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The *SI Model Assignment* dialog box appears.

12. Select the IBIS Device model named DS90C031TM and click *Assign*.



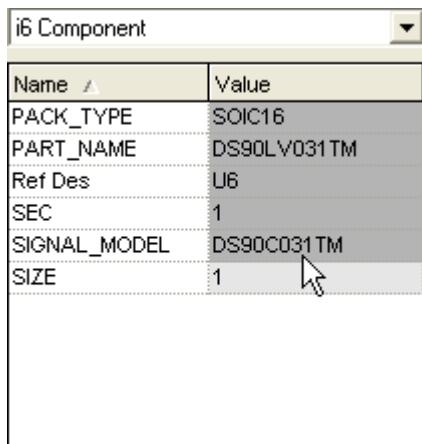
The Component Connectivity Details pane is modified to display the model-defined differential pairs.

| Pin Name | Pin Number | Pin Type | Signal |
|----------|------------|----------|---------|
| * | * | * | * |
| din1 | 1 | Input | |
| din2 | 7 | Input | |
| din3 | 9 | Input | |
| din4 | 15 | Input | wstat |
| DP_dout1 | 2,3 | Output | DP_VCLK |
| DP_dout2 | 6,5 | Output | |
| DP_dout3 | 10,11 | Output | |
| DP_dout4 | 14,13 | Output | |
| en* | 12 | Input | |
| en | 4 | Input | |

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The Properties window displays the SIGNAL_MODEL property with the value DS90C031TM.



This indicates that the signal integrity model DS90C031TM has been assigned on the ds90lv031tm component.

13. Click the toolbar button in System Connectivity Manager to open Constraint Manager.
14. Click the *Electrical Properties* worksheet in the *Signal Integrity* workbook in the *Net* folder.

A screenshot of the Constraint Manager interface. On the left, there's a tree view under the 'Electrical' category, with 'Net' expanded to show 'Signal Integrity', 'Timing', and 'Routing' sub-folders. Under 'Signal Integrity', 'Electrical Prop...' is selected. On the right, there's a table titled 'Objects' with columns 'Type', 'S', 'Name', and 'Referenced Electrical CSet'. The table lists various components and nets, including 'processor' (Type Dsn, S *), 'BA(8)', 'RA(16)', 'RD(8)', 'S_VD(8)', 'DP_VCLK' (Type DPr, S M, Referenced Electrical CSet CRITICAL), 'DS_SUB', 'BNC1', 'BRD', 'BRESET', 'BWR', 'DATA', 'DCLK', 'FPGA', and 'GAIN'. The 'DP_VCLK' row is highlighted.

Note that a model-defined differential pair named DP_VCLK with the member nets VCLKA and VCLKB has been automatically created in Constraint Manager.

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Module 5: Working with Constraints

System Connectivity Manager allows you to automatically generate and assign signal integrity models for all two-pin discrete components (resistors, capacitors, and inductors) in your design.

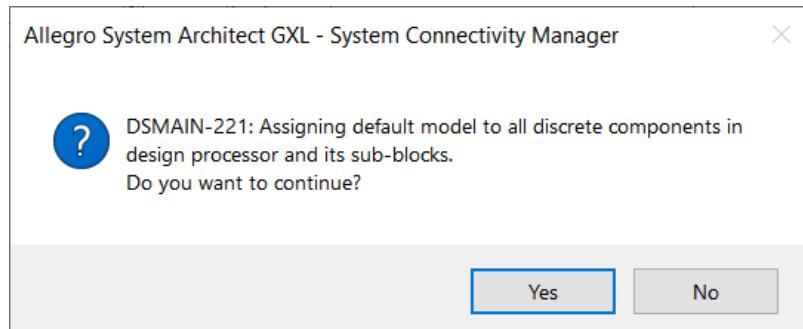
When you apply terminations in the design, signal integrity models are automatically assigned to the resistors and capacitors used in the termination. You can automatically generate and assign signal integrity models for all other two-pin discrete components such as resistors, capacitors, and inductors used in the design.

15. Close Constraint Manager.

You will now automatically generate and assign signal integrity models to all two-pin discrete components in the design.

16. Choose *Tools – Signal Integrity – Auto Assign Models*.

The following message box appears.

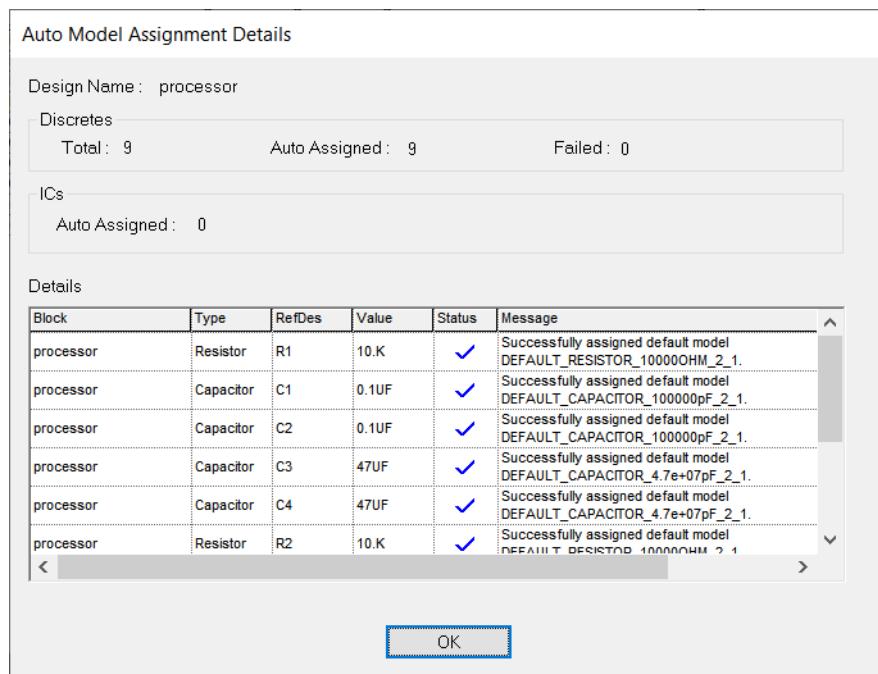


17. Click Yes.

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The Auto Model Assignment Details dialog box appears displaying the details of the model assignments made on two-pin discrete components in the design.



18. Click **OK** to close the dialog box.

Summary

You now know how to assign signal integrity models on components in System Connectivity Manager. You also learned how to automatically assign signal integrity models on two pin discrete components used in the design.

For More Information

See:

[Working with Signal Integrity Models](#) chapter of *System Connectivity Manager User Guide*.

Lesson 5-5: Applying Constraints from SigXplorer

Overview

You can use SigXplorer to analyze the high speed nets in your design for signal integrity issues and create a set of constraints for the nets. The topology file containing these constraints becomes an ECset. You can then apply the ECSet (topology file containing constraints) to nets in the design.

In this lesson, you will learn to extract a net into SigXplorer from Constraint Manager, set constraints in SigXplorer and then apply the topology containing the constraints on the net in Constraint Manager.

Procedure

1. Click the  toolbar button in System Connectivity Manager to open Constraint Manager.
2. Click the *Impedance* worksheet in the *Routing* workbook in the *Net* folder.

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3. Select the Xnet named WSTAT.

The screenshot shows the System Connectivity Manager interface. On the left is the 'Worksheet Selector' pane, which is currently set to 'Electrical'. Under the 'Net' category, 'Impedance' is selected. The main area displays a table titled 'processor' with columns for 'Objects', 'Referenced Electrical CSet', and 'Single-line Impedance'. The 'Single-line Impedance' section includes columns for Target (Ohm), Tolerance (Ohm), Actual (Ohm), and Margin (Ohm). The table lists various network objects like 'processor', 'BA(8)', 'RA(16)', 'RD(8)', and several 'S_VD' nets, each with a critical impedance value of 65 Ohms and a 5% margin.

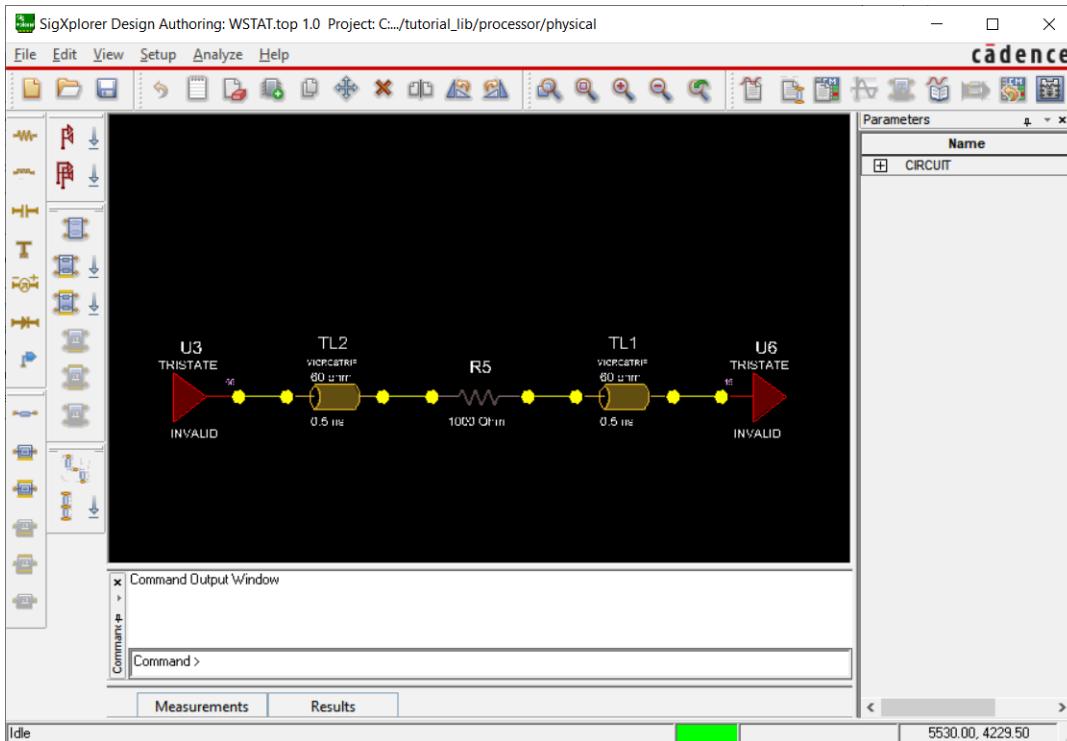
| Objects | | | Referenced Electrical CSet | Single-line Impedance | | | |
|---------|---|-----------|----------------------------|-----------------------|------------------|---------------|---------------|
| Type | S | Name | | Target Ohm | Tolerance Ohm | Actual Ohm | Margin Ohm |
| FLTR | * | * | | * | * | * | * |
| Dsn | | processor | | | | | |
| Bus | | BA(8) | | | | | |
| Bus | I | RA(16) | | | | | |
| Bus | | RD(8) | | | | | |
| Bus | | S_VD(8) | CRITICAL | 65 | 5 % | | |
| Net | | S_VD<0> | CRITICAL | 65 | 5 % | | |
| Net | | S_VD<1> | CRITICAL | 65 | 5 % | | |
| Net | | S_VD<2> | CRITICAL | 65 | 5 % | | |
| Net | | S_VD<3> | CRITICAL | 65 | 5 % | | |
| Net | | S_VD<4> | CRITICAL | 60 | 5 % | | |
| Net | | S_VD<5> | CRITICAL | 65 | 5 % | | |
| Net | | S_VD<6> | CRITICAL | 65 | 5 % | | |
| Net | | S_VD<7> | CRITICAL | 65 | 5 % | | |
| DPr | M | DP_VCLK | | | | | |
| Net | | VCLKA | | | | | |
| Net | | VCLKB | | | | | |
| DPr | | DS_SUB | | | | | |
| Net | | BNC1 | | | | | |
| Net | | BRD | | | | | |
| Net | | BRESET | | | | | |
| Net | | BWR | | | | | |

4. Choose Tools – SigXplorer.

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The topology for the net is displayed in SigXplorer.



5. Choose *Setup – Constraints*.

The Set Topology Constraints dialog box appears.

6. Click the *Impedance* tab.

7. In the *Pin/Tees* list, click on U3.56.

8. In the *Pin/Tees* list, click on U6.15.

9. In the *Target* field, enter 80.

10. In the *Tolerance* field, enter 5.

11. Click *Add*.

12. Click *OK* to save the changes and close the dialog box.

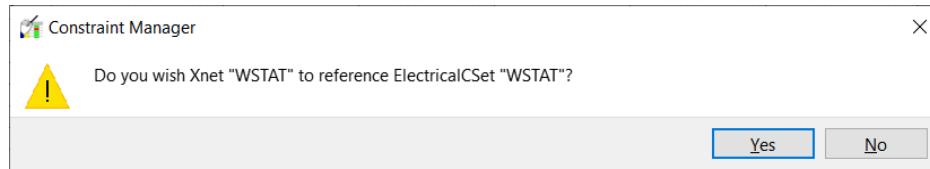
13. Choose *File – Update Constraint Manager*.

An ECSet named WSTAT with the constraints you added in SigXplorer is created.

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The following message box appears.



14. Click Yes.

The Electrical CSet Apply Information window appears.

15. Close Electrical CSet Apply Information window.

| RESET | | | | |
|-------------|-------|-------|-------|--|
| RWE | | | | |
| SEL | | | | |
| VCLKC | | | | |
| WAIT | | | | |
| WSTAT | | | | |
| U3.56:U6.15 | WSTAT | 80.00 | 5 ohm | |
| WSTAT | WSTAT | | | |
| X27^H1 | WSTAT | | | |

In the *Impedance* worksheet note that the ECSet WSTAT has been applied on the XNet WSTAT.

You can now assign the ECSet WSTAT on other XNets in Constraint Manager.

Summary

You now know how to extract a net into SigXplorer from Constraint Manager, set constraints in SigXplorer and then apply the topology containing the constraints on the net in Constraint Manager.

For More Information

See:

- [Topology Extraction in SigXplorer](#) chapter in the [System Connectivity Manager to Constraint Manager User Guide](#) for information on using SigXplorer with Constraint Manager when the later is launched from System Connectivity Manager.

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- [Allegro Constraint Manager User Guide](#) for more information on using SigXplorer with Constraint Manager.
- [Allegro PCB SI SigXplorer User Guide](#) for more information on using SigXplorer.

Lesson 5-6: Applying Physical and Spacing Constraints

Overview

System Connectivity Manager supports the addition of electrical as well as physical and spacing constraints to nets and related objects. You can use Constraint Manager connected to System Connectivity Manager to create, view, edit, and assign physical and spacing constraints to groups of nets or directly to nets in addition to electrical constraints. You also have the option to switch between edit and read-only modes for physical and spacing constraints in System Connectivity Manager.

In this lesson, you will learn to enable an existing project to support, and to specify Physical and Spacing constraints.

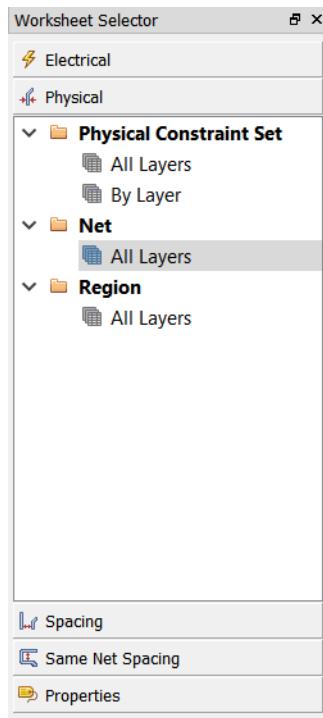
Procedure

1. Click the  toolbar button in System Connectivity Manager to open Constraint Manager.

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2. Click the *Physical — Net — All Layers*. Observe that the stack-up information is empty.



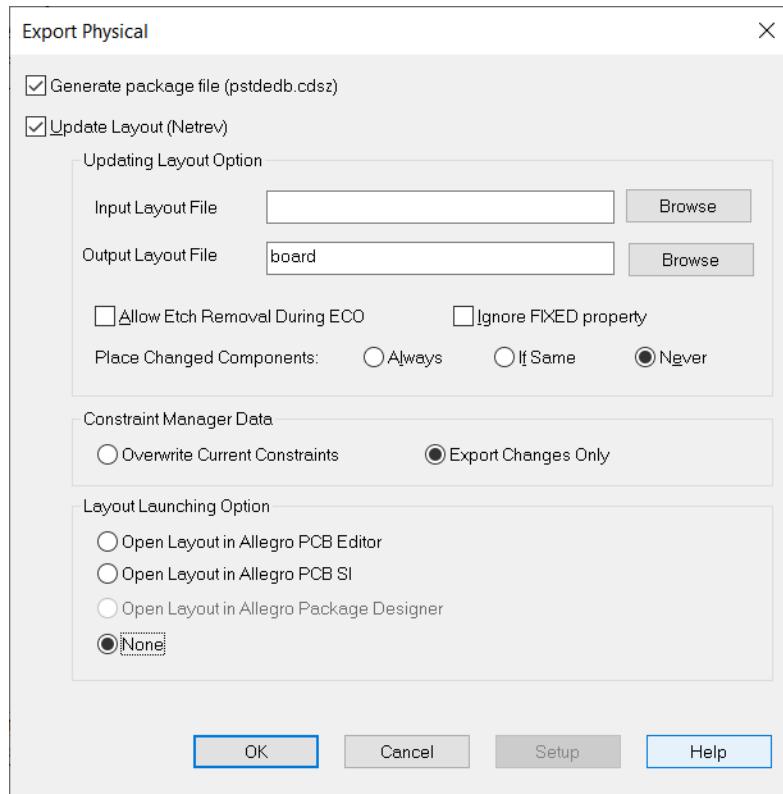
| Objects | | Referenced Physical CSet | Line Width | | |
|---------|---|--------------------------|------------|-----|-----|
| Type | S | | Name | Min | Max |
| | | | | mil | mil |
| FLTR | * | * | * | * | * |
| Dsn | | processor | | | |
| Bus | | BA(8) | | | |
| Bus | I | RA(16) | | | |
| Bus | | RD(8) | | | |
| Bus | | S_VD(8) | | | |
| Net | | S_VD<0> | | | |
| Net | | S_VD<1> | | | |
| Net | | S_VD<2> | | | |
| Net | | S_VD<3> | | | |
| Net | | S_VD<4> | | | |
| Net | | S_VD<5> | | | |
| Net | | S_VD<6> | | | |
| Net | | S_VD<7> | | | |
| DPr | M | DP_VCLK | | | |
| Net | | VCLKA | | | |
| Net | | VCLKB | | | |
| DPr | | DS_SUB | | | |
| Net | | BNC1 | | | |
| Net | | BRD | | | |
| Net | | BRESET | | | |
| Net | | BWR | | | |

3. In System Connectivity Manager, choose *Project — Export — PCB Board*. The *Export Physical* dialog box displays.

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Module 5: Working with Constraints

4. Specify the *Output Layout File* as *board.brd* and click *OK*.



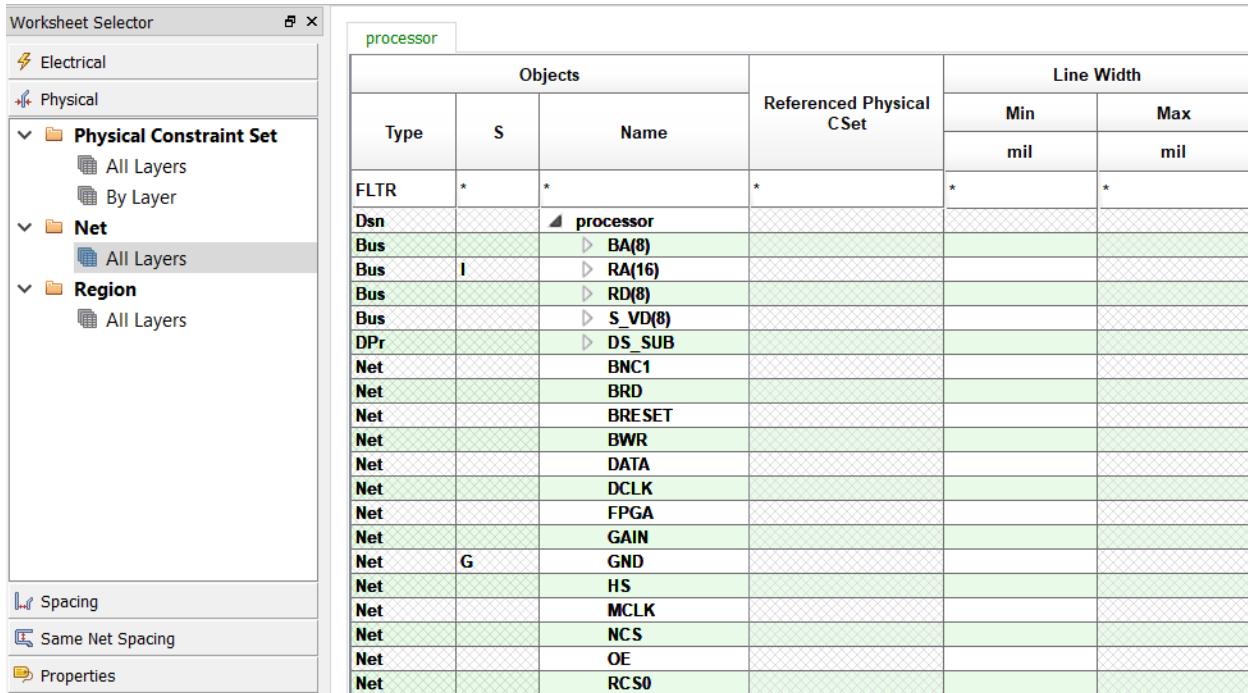
5. After we have exported the design to the board stack-up information is generated. To import this stack-up information we need to import the board file to the SCM design. Choose *Project — Import — Physical*. The Import Physical dialog box displays.
6. Click *Use Layout File* and click *OK*. The design differences are displayed in the Visual Design Differences window. Choose *Update All* to merge all the design changes.
7. Save the design and close System Connectivity Manager.
8. To make the physical and spacing constraints non-editable, we need to specify a directive in the .cpm file. Open the *tutorial.cpm* file using a text editor, and add the following lines:

```
START_CONSTRAINT_MGR  
EDIT_PHYSICAL_AND_SPACING_CONSTRAINTS 'OFF'  
END_CONSTRAINT_MGR
```
9. Launch System Connectivity Manager and reopen the project.

System Connectivity Manager Tutorial

Module 5: Working with Constraints

10. Click the  toolbar button in System Connectivity Manager to open Constraint Manager. The Physical and Spacing constraints are editable.



The screenshot shows the 'Worksheet Selector' on the left with 'Physical' selected. The main area is titled 'processor' and contains a table of objects. The table has columns for Type, S, Name, Referenced Physical CSet, and Line Width (Min and Max). Most values are marked with an asterisk (*), indicating they are editable. The table includes rows for various components like FLTR, Dsn, Bus, and Net, along with specific pins like BA(8), RA(16), RD(8), S_VD(8), DS_SUB, BNC1, BRD, BRESET, BWR, DATA, DCLK, FPGA, GAIN, GND, HS, MCLK, NCS, OE, and RCS0.

| Objects | | | Referenced Physical CSet | Line Width | |
|---------|---|-----------|--------------------------|------------|-----|
| Type | S | Name | | Min | Max |
| | | | | mil | mil |
| FLTR | * | * | * | * | * |
| Dsn | | processor | | | |
| Bus | | BA(8) | | | |
| Bus | I | RA(16) | | | |
| Bus | | RD(8) | | | |
| Bus | | S_VD(8) | | | |
| DPr | | DS_SUB | | | |
| Net | | BNC1 | | | |
| Net | | BRD | | | |
| Net | | BRESET | | | |
| Net | | BWR | | | |
| Net | | DATA | | | |
| Net | | DCLK | | | |
| Net | | FPGA | | | |
| Net | | GAIN | | | |
| Net | G | GND | | | |
| Net | | HS | | | |
| Net | | MCLK | | | |
| Net | | NCS | | | |
| Net | | OE | | | |
| Net | | RCS0 | | | |

11. You can now modify the Physical and Spacing constraints for the design. When you export the design to Physical, the modified Physical and Spacing constraints are transferred to the board.

Note: For new designs, that you make using this release of System Connectivity Manager the directive is set to 'ON' by default. To make the physical and spacing constraints non-editable, specify the directive to 'OFF' the .cpm file.

12. To set the directive to 'OFF' open the *tutorial.cpm* file using a text editor, and add the following lines:

```
START_CONSTRAINT_MGR  
EDIT_PHYSICAL_AND_SPACING_CONSTRAINTS 'OFF'  
END_CONSTRAINT_MANAGER
```

System Connectivity Manager Tutorial

Module 5: Working with Constraints

Summary

You now know how to enable and work with Physical and Spacing constraints in an SCM design.

For More Information

See:

- [Physical and Spacing Constraints](#) chapter in the [System Connectivity Manager to Constraint Manager User Guide](#) for information on using Physical and Spacing constraints.
- [Allegro Constraint Manager User Guide](#) for more information on using Constraint Manager.

System Connectivity Manager Tutorial

Module 5: Working with Constraints

Module 6: Creating a Hierarchical Design

Prerequisite

To work with the lessons in this module, open the `hier_design.cpm` project located at
`<your_work_area>\modules\hier_design\hier_design` in System Connectivity Manager.

For more information, see [Understanding the Sample Design Files](#) on page 16.

Lessons

This module consists of the following lessons:

- [Overview](#) on page 200
- [Lesson 6-1: Creating a Spreadsheet Block](#) on page 203
- [Lesson 6-2: Adding a Schematic Block in a Design](#) on page 208
- [Lesson 6-3: Importing Verilog Netlists](#) on page 213
- [Lesson 6-4: Setting Up Block Packaging Options](#) on page 215
- [Lesson 6-5: Editing Spreadsheet Blocks](#) on page 219
- [Lesson 6-6: Creating a Third-Level Hierarchical Design](#) on page 225
- [Lesson 6-7: Creating a Bottom-Up Hierarchical Design](#) on page 228

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

Multimedia Demonstration



A Flash-based multimedia demonstration of this module, [Working with Hierarchical Designs](#), is available on Cadence Online Support.

Completion Time

- 2 hours for written lessons
- 50 minutes for multimedia demonstrations

Overview

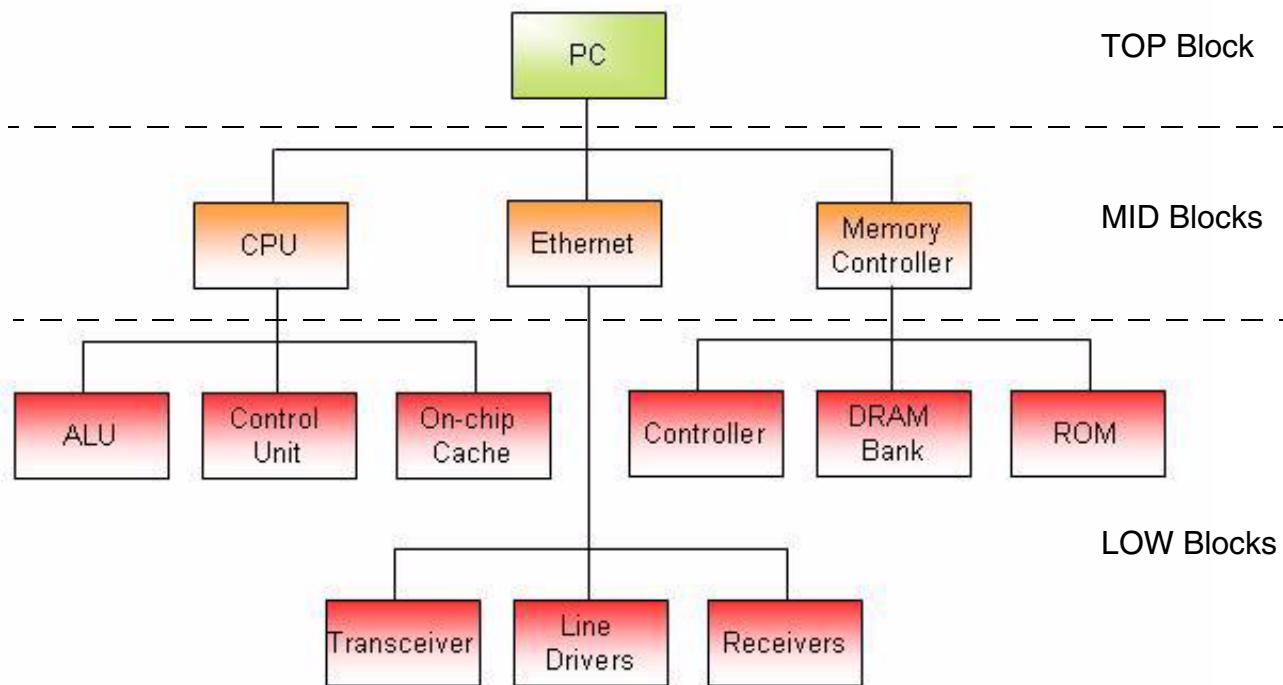
You can use a hierarchical design structure to divide a design into sub designs or blocks, where each block represents a logical function.

An example of a hierarchical design is shown below.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

Figure 9-1 Hierarchical Design Example



Notice that the design has a top-level block named `PC`. This block includes three sub-blocks, `CPU`, `Ethernet`, and `Memory Controller`. Each of these sub-blocks includes more lower-level blocks. In the hierarchical design example, the `CPU` block is divided into three sub-blocks named `ALU`, `Control Unit` and `On-chip Cache`.

To create a hierarchical design, you can use the top-down or bottom-up design methodology.

- **Top-Down Methodology**—In the top-down methodology, you first create the top-level design `PC`. Next, based on the logical partitioning of the design you create blocks for each logic function. In the case of the `PC` design, the top-level design will have three blocks: `CPU`, `Ethernet` and `Memory Controller`. After creating the top-level design with the necessary blocks, you can create the lower-level blocks.
- **Bottom-Up Methodology**—In the bottom-up methodology, you create a lower-level block first. For the design `PC`, you can first create the designs for the lowest level of hierarchy—`ROM`, `DRAM`

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

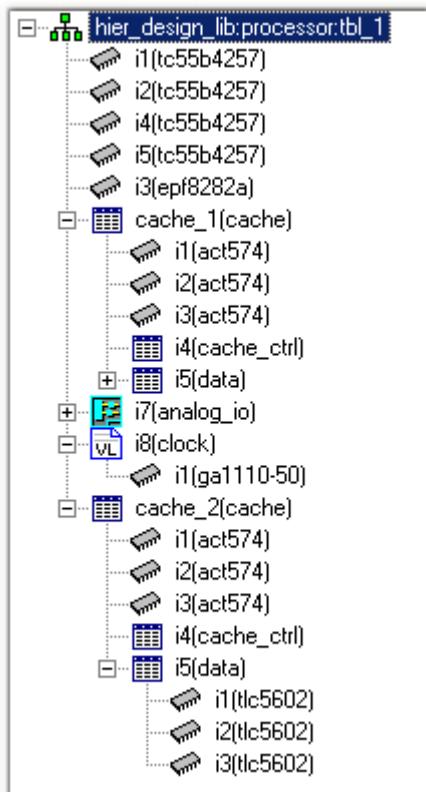
Bank, and Memory Controller. You can then create the higher level design Memory Controller. You can then repeat the process to create Ethernet and CPU blocks, and then create top-level design by integrating the Memory Controller, Ethernet and CPU blocks into the PC design.

While creating a hierarchical design, you can create blocks by:

- Creating them as stand-alone blocks that are part of a library.
- Instantiating them directly into the design. These blocks are integrated as sub-circuits in the hierarchical design.

System Connectivity Manager enables you to seamlessly create hierarchical designs using top-down and bottom-up design methodologies. You can have a combination of spreadsheet, Verilog and schematic blocks in your design. The use of multiple design blocks will allow you flexibility in capturing an electronic circuit. For example, you may prefer to use spreadsheet blocks to capture large pin-count devices and schematic blocks to capture analog designs.

In this module, you will create the following hierarchical block:



System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

You will start by creating design blocks. In the first three lessons of this module, you will create spreadsheet (`cache`), schematic (`analog_io`) and Verilog (`clock`) blocks. In the fourth and fifth lessons, you will learn to add components and set packaging options such that components in different blocks get unique reference designators. You will also learn the differences in editing properties or connectivity in the Context or Master modes. Finally, you will learn to create hierarchical designs by adding blocks within other blocks using both top-down and bottom-up methodologies.

Lesson 6-1: Creating a Spreadsheet Block

Overview

In this lesson, you will learn to create a spreadsheet block and instantiate it in an existing design.

You will create a spreadsheet block named `cache` and place it in the `hier_design_lib` library. This logical block (in spreadsheet format) will have the following input/output ports:

- Input ports—`vd<7..0>`, `gain`, `vclka`, and `vclkb`
- Output ports—`outa` and `outb`

Procedure

1. In the `hier_design.cpm` project, notice that the top-level design name or root design name is `processor`. The Hierarchy Viewer displays the root design.



The Hierarchy Viewer provides you a tree view of the complete design hierarchy and lets you quickly access all the blocks and components in your design.

You can use the Hierarchy Viewer to view the binding of any block.

You will now create a new spreadsheet block named `cache`.

2. Choose *Design – Create Block*.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

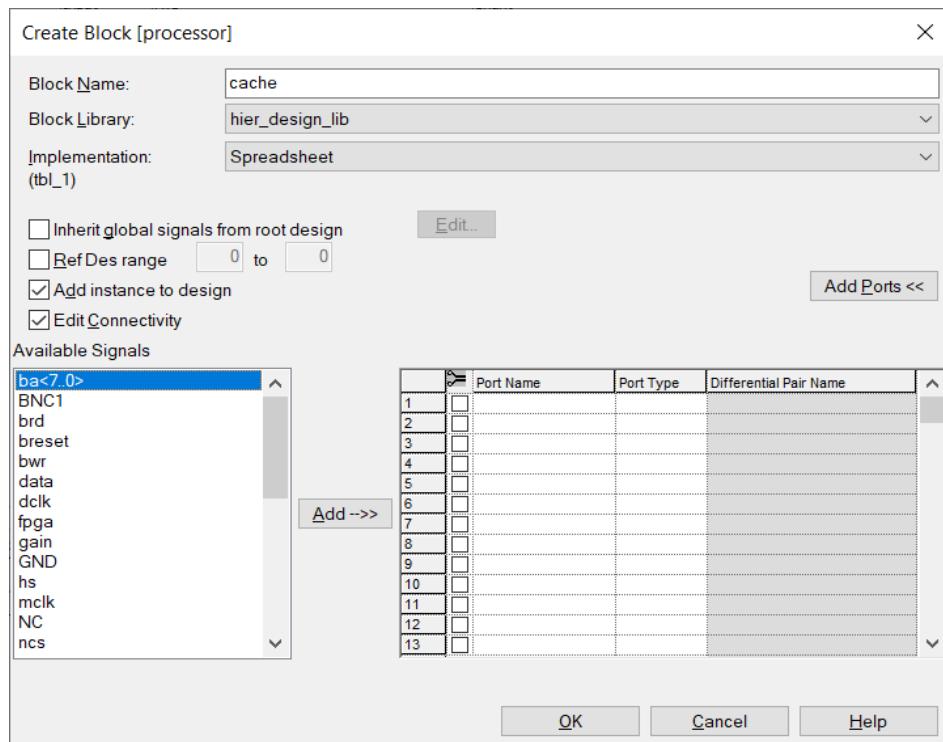
The Create Block dialog box appears. You use this dialog box to create blocks—Spreadsheet, Verilog or Schematic—in System Connectivity Manager.

3. Type `cache` in the *Block Name* field.

The *Block Library* field shows that the new block being created will be added in the `hier_design_lib` library. If required, you can change the library name.

4. Click the *Add Ports* button to display the port list.

The Create Block dialog box expands to display the port list.



You can assign port names and define the port type as IN, OUT, or INOUT.

5. To add an input port `vd<7..0>`, type `vd<7..0>` in the *Port Name* field and press Tab to move to the *Port Type* field.
6. IN is automatically populated in the *Port Type* drop-down list.
7. Repeat steps step 5 and step 6 to add the following input ports—`gain`, `vclka`, and `vclkb`.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

8. To add an output port `outa`, type `outa` in the *Port Name* field and choose `OUT` from the *Port Type* drop-down list.

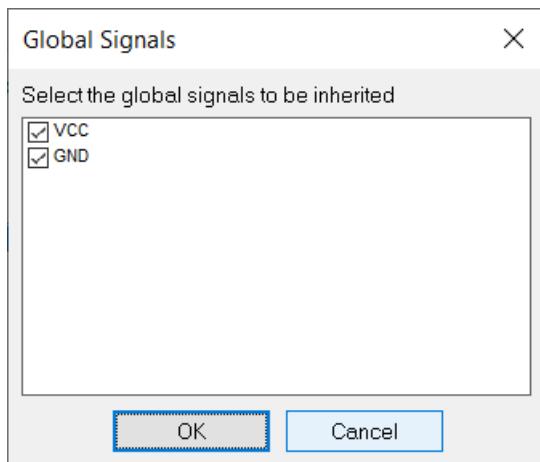
9. Repeat [step 8](#) to add another output port, `outb`.

You can inherit global signals available in the parent (processor) block in the current block.

10. Select the *Inherit global signals from root design* check box.

11. Click the *Edit* button.

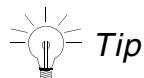
The Global Signals dialog box appears displaying the list of global signals that you can inherit from the processor block.



12. Without making any changes to the list, click *OK*.

13. Ensure that the *Add instance to design* check box is selected.

This will add an instance of the new block in the processor design.

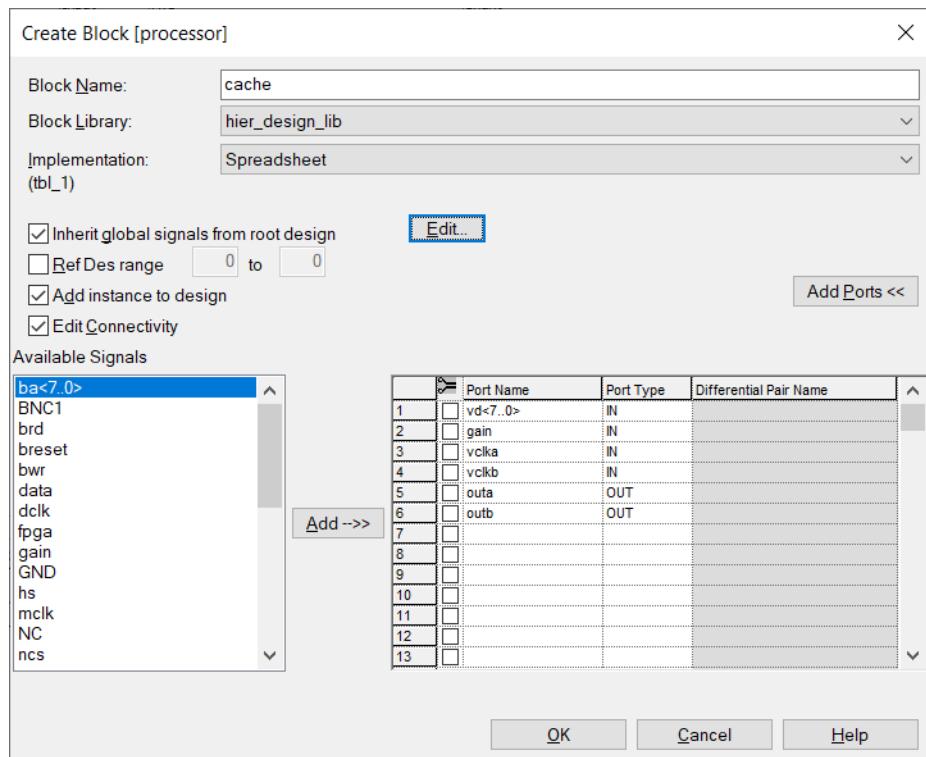


You can also add instances of blocks using Part Information Manager.

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Module 6: Creating a Hierarchical Design

At this point, the Create Block dialog box should display the following settings:



14. Click *OK* to store the `cache` block in the `hier_design_lib` library.

The `cache` block is stored in the `hier_design_lib` library. The Block Packaging Options dialog box appears.

15. Ensure that the *Use Optimized Packaging* option button is selected. This option will use optimized reference designators in context of the root block.

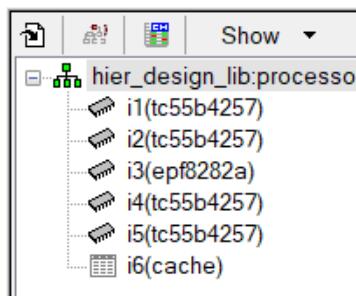
Note: The Block Packaging Options dialog box provides you a powerful mechanism of renaming reference designators and physical net names while integrating a block into any design. You can also alias a global signal in the block to a signal in the design in which you are adding the block. You will learn to use different block packaging options across this module.

16. Click *Apply*.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

A new block named `cache` is added in the Component List and the Hierarchy Viewer. The block is assigned the instance name `i6`. If required, you can change the instance name.



17. Double-click the `i6` instance of the `cache` block in the Hierarchy Viewer to open it.

The `cache` block appears. All signals in the `cache` block are displayed in the Signal List. This block does not contain any component. You will add components to the `cache` block and identify the advantages of different packaging options in [Lesson 6-4: Setting Up Block Packaging Options](#) on page 215.

18. Close the `cache` block by selecting *File–Close*.
19. Click *Yes* to save the changes.

Summary

In this lesson, you learned to create a spreadsheet block in an existing design.

For More Information

See:

[Working with Hierarchical Designs](#) chapter of *System Connectivity Manager User Guide*.

Lesson 6-2: Adding a Schematic Block in a Design

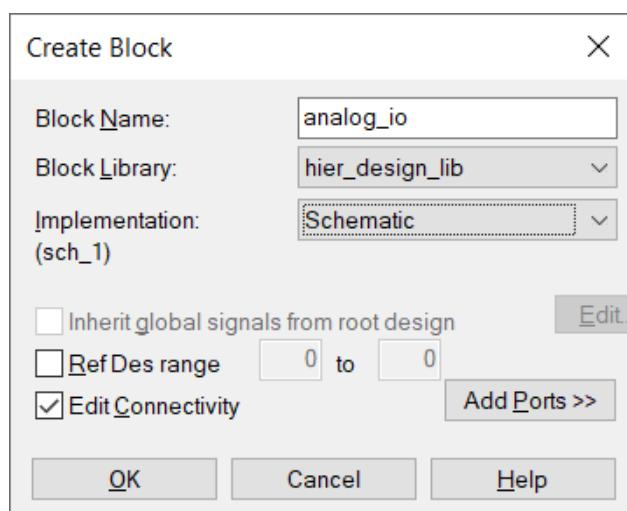
Overview

In this lesson, you will learn to add a schematic block in a spreadsheet design. You will first create a schematic block `analog_io` and then instantiate it in the design. Since creating a schematic in Design Entry HDL is beyond the scope of this tutorial, you will create the `analog_io` schematic block by copying parts from an existing schematic.

Procedure

1. Choose *Project – Create Block*.
The Create Block dialog box appears.
2. Specify the block name as `analog_io`.
3. From the *Implementation* drop-down list, choose *Schematic*.
4. Select the *Edit Connectivity* check box.

The Create Block dialog box should look like:



5. Click *OK*.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

The `analog_io` block opens in Design Entry HDL (instance 1).

You can create a new schematic here. Since creating a schematic in Design Entry HDL is beyond the scope of this tutorial, you will create the `analog_io` schematic block by copying an existing schematic. Also, CADENCE A SIZE PAGE is automatically added to the instance 1.

To copy an existing design, do the following:

- a. Open new instance (instance 2) of Allegro Design Entry HDL. In this instance, open the `analog_io.cpm` file located at `<your_work_area>/reference/schematic/analog_io`.
- b. Select *Group – Create – By Rectangle*.

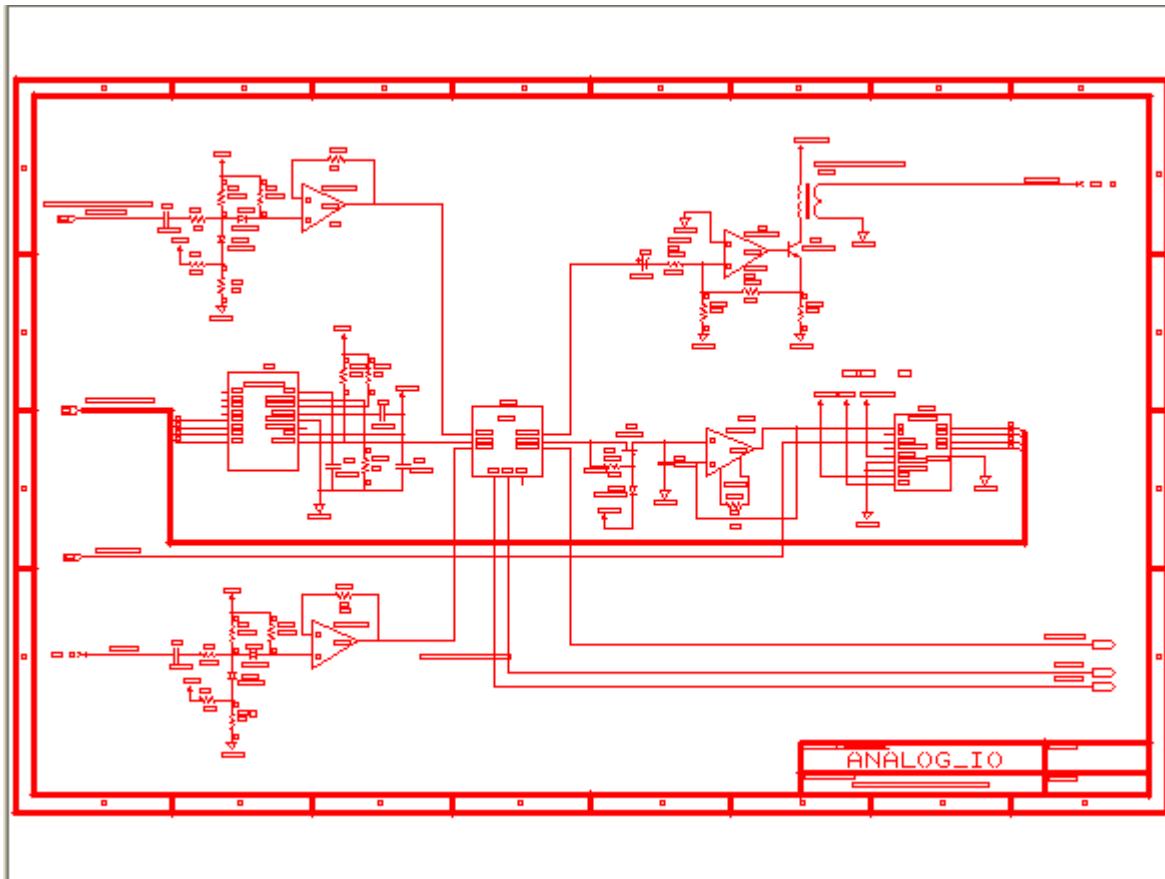
The cursor changes to a crosshair. The Design Entry HDL *Command Console* window displays the following message:

```
select A  
Using group "A"
```

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Module 6: Creating a Hierarchical Design

- c. Click once on the top-left of the page border on the canvas and drag the mouse to the bottom-right of the page border to create a selection box and click again.



All components and their connectivity, including the page border are selected. The Console window displays the message:

Group "A" contains:

82 bodies 730 properties 0 notes 163 wires
25 dots 0 images

- d. Select *Group – Copy All [A]*.

6. Select the instance 1 of Design Entry HDL that has been launched from System Connectivity Manager.
7. Right-click the border of CADENCE A SIZE PAGE and choose *Delete* from the pop-up menu.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

8. Select *Edit – Paste* to paste the contents of the group A created from schematic in instance 2 into instance 1 of Design Entry HDL.

9. Select *File – Save All* to save the schematic.

10. Click Yes.

11. Select *File – Exit* to close Design Entry HDL.

Similarly, close the other instance of Design Entry HDL as well.

12. In System Connectivity Manager, click the  *Add Component* tool button.

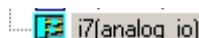
13. Select the `analog_io` cell in the `hier_design_lib` library.

14. Click the *Add* button and close Part Information Manager.

The Block Packaging Options dialog box appears.

15. Select the *Use Prefix* option button, enter `SCH` in the *Prefix* field and click *Apply*.

A new block `analog_io` is added in the Hierarchy Viewer and it also appears in the Component List. Notice that the icon placed next to the block represents block type as schematic as shown below.



16. Select *File – Save All* to save the design.

17. Double-click the `analog_io` block in the Hierarchy Viewer to open it in the Context mode.

The `analog_io` appears within the Spreadsheet Editor. Notice that all components are listed in the Component List and all

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

signals are listed in the Signal List. Also notice that the reference designator of each component is prefixed with SCH.

| Component List | | | |
|----------------|---------|--------|---|
| Instance | Ref Des | Cell | |
| * | * | * | * |
| page1_i1 | SCH_J8 | conn2 | |
| page1_i3 | SCH_R8 | resd | |
| page1_i4 | SCH_C2 | cap | |
| page1_i6 | SCH_R4 | resd | |
| page1_i7 | SCH_R3 | resd | |
| page1_i8 | SCH_CR2 | 1n4148 | |
| page1_i9 | SCH_R7 | resd | |
| page1_i10 | SCH_CR4 | 1n4148 | |
| page1_i11 | SCH_R10 | resd | |

Note: The schematic block opens in a read-only view in the Spreadsheet Editor. For more information about how to use read-only blocks of type schematic in System Connectivity Manager, see the *Working with Block Designs* chapter of the *Allegro Design Entry HDL User Guide*.

If required, you can modify the schematic block by launching Design Entry HDL either from System Connectivity Manager using *Project – Edit Block*, or from outside of SCM. Irrespective of how you make changes, if the spreadsheet design is open in System Connectivity Manager while the schematic block is updated, a warning message is displayed in the violations window to indicate that the schematic block has been modified. To update your spreadsheet design with these changes, click *Resolve*.

System Connectivity Manager also allows you to import schematic blocks as read-only blocks. In case such blocks are modified, you need to re-import the block using *Re-import Block* command.

Summary

In this lesson, you learned to add a schematic block in System Connectivity Manager.

For More Information

See:

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

Working with Hierarchical Designs chapter of *System Connectivity Manager User Guide*.

Working with Block Designs chapter of the *Allegro Design Entry HDL User Guide*.

Lesson 6-3: Importing Verilog Netlists

Overview

In this lesson, you will learn to import Verilog netlists in System Connectivity Manager.

Concept

You can import structural Verilog files into System Connectivity Manager. The modules in a Verilog file are imported as spreadsheet blocks. You can then add these blocks into your design. In this lesson, you will learn to import Verilog, create a block named `clock` along with the components and connectivity, and add this block into your design.

Note: The sample verilog file `clock.v` is included in the `<your work area>/reference/misc_data` directory.

Procedure

1. Choose *Project—Import — Verilog — Netlist*.

The Import Verilog dialog box appears.

2. Specify the file name and path of `clock.v` file. This file is located in the `<your work area>/reference/misc_data` directory.
3. From the Library Name drop-down list select `hier_design_lib`.
4. Click OK. A Finished Importing message box displays. The Visual Design Differences window displays a Module Difference.

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Module 6: Creating a Hierarchical Design

5. Click *Update* in the Visual Design Differences window. The Block is added to your design. To view this block, choose *Project—Change Root*, and then select *clock* and click *OK*.

Note: A directory named `clock` is created under the `hier_design_lib` directory.

6. To instantiate the block in your design, navigate back to the processor tab.

7. Click the  *Add Component* toolbar button.

8. Select the `clock` component from the `hier_design_lib` library and click *Add*.

9. In the Block Packaging Options dialog box, select *Use Optimized Packaging* and click *Apply*.

A new block `clock` is added in the Hierarchy Viewer and it also appears in the Component List.

10. Select the `clock` block in the Hierarchy Viewer.

11. Click the  *Descend* tool button.

A new tab for the `clock` block opens.

12. Choose *File—Save All* to save the changes in all blocks.

13. Choose *File—Close* to close the block.

Summary

In this lesson, you learned to import a verilog module as a spreadsheet block in System Connectivity Manager.

For More Information

See:

[Working with Hierarchical Designs](#) chapter of *System Connectivity Manager User Guide*.

Lesson 6-4: Setting Up Block Packaging Options

Overview

In this lesson, you will learn to add components in a hierarchical block. You will also use different packaging options to ensure that unique reference designators are assigned to different components or blocks.

Concept

You can use Part Information Manager to add components or blocks to any design.

When you add any block, the Block Packaging Options dialog box appears. In this dialog box, you can define a suffix, prefix, or reference designator range that can uniquely define the reference designators for the components in the block.

The use of these options help you:

- Avoid packaging errors by ensuring that the same reference designator is not assigned to packages in different blocks
- Easily identify the block in which a component having a specific reference designator exists.

This is helpful when you are debugging the design with respect to the board as you can trace back parts on the board to a specific block in the System Connectivity Manager.

For example, if you have a hierarchical design named `MEMORY` with the two blocks `ROM` and `CONTROLLER`, you can assign the suffix `ROM` to the reference designators of all components in the `ROM` block and the suffix `CNTR` to the reference designators of all the components in the `CONTROLLER` block. The reference designators of components in the `ROM` block will be `U1_ROM`, `U2_ROM`, and so on. The reference designators of components in the `CONTROLLER` block will be `U1_CNTR`, `U2_CNTR`, and so on. This unique identification of reference designators across blocks ensures that the same reference designator is not assigned to packages in different blocks.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

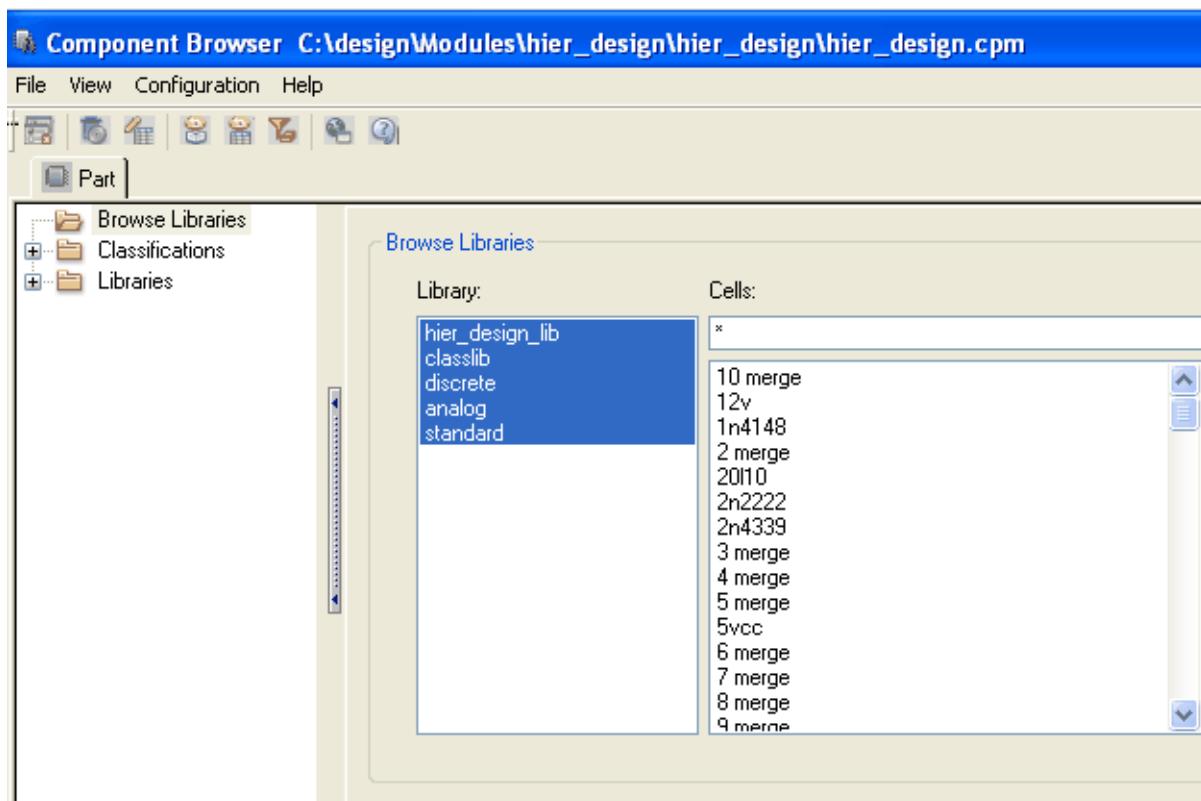
As a result, you can quickly debug a design with respect to the board layout by identifying the block in which a component having a specific reference designator exists.

Procedure

1. Select the `cache` block in the Hierarchy Viewer.
2. Click the *Descend* tool button ().
3. Click the *Add Component* tool button ().

Part Information Manager appears.

Select all available libraries. For this, click the `hier_design_lib` (first) library and then keeping the Shift key pressed, click the `standard` (last) library.



4. Type `act*` in the *Cells* field.

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Module 6: Creating a Hierarchical Design

5. Select the `act574` component.
6. Select the row with the part name `ACT574` and the part number `ic345`.
7. Type `3` in the *Instances* field to specify that you will add three instances of the `ACT574` part.
8. Click the *Add* button.

Notice that three instances of the `ACT574` component are added to the `cache` block and appears in the Component List and in the Hierarchy Viewer.

9. Close Part Information Manager.
10. Click *File–Save* to save the `cache` block.
11. Choose *File–Close* to close the `cache` block.

In [Lesson 6-1: Creating a Spreadsheet Block](#) on page 203, you added an instance of the `cache` block in the `processor` block.

You can now add another instance of the `cache` block with changed packaging options in the `processor` block. For example, you can define that reference designators for components in the new `cache` block should be any value between the range `30` and `51`. Such a definition of reference designators may help you identify components across multiple instances of the same block.

12. Switch to the `processor` design.
13. Click the *Add Component* tool button ().
14. Select the `cache` cell in the `hier_design_lib` library.
15. Click the *Add* button and close Part Information Manager.

The Block Packaging Options dialog box appears.

16. Select the *Use Ref. Des. Range* option button, enter `30` to `51` in the adjacent field, and click *Apply*.

A new instance of the `cache` block is added in the design.

17. Close Part Information Manager.
18. Double-click the new instance of the `cache` block in the Hierarchy Viewer to open its tab.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

The cache design opens. Notice that the three instances of the ACT574 part appear with the reference designators—U36, U37, and U38.

19. Close the tab for the cache block.

If you view the Hierarchy viewer, you will see a two-level hierarchical design with the processor design at root level. This design contains cache, analog_io and clock blocks. You have used the top-down methodology to create this design.

Notice that there are two instances of the cache block. Let's rename these instances as cache_1 and cache_2.

20. Select the i6 component from the Component List of the processor block.

21. Select *Object–Change–Name*.

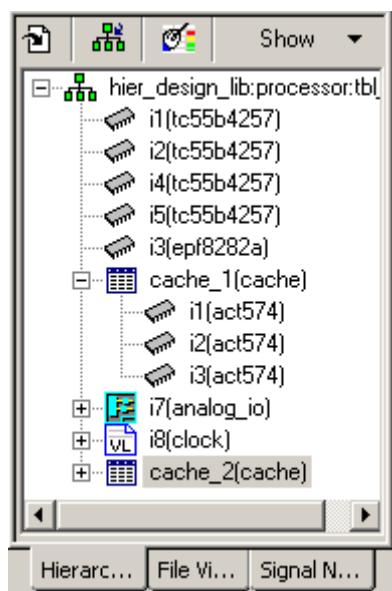
The instance name is selected and can be edited.



22. Type cache_1 and press Enter.

23. Repeat the above steps to rename the other instance of the cache block to cache_2.

The Hierarchy Viewer now displays the following design:



System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

Summary

In this lesson, you learned to add components to a block and change their packaging options.

For More Information

See:

[Working with Hierarchical Designs](#) chapter of *System Connectivity Manager User Guide*.

Lesson 6-5: Editing Spreadsheet Blocks

Overview

In this lesson, you will learn to edit blocks in master and context mode.

Concept

You can edit the blocks in your design in the master mode or in the context of the root design.

- Master mode—In this mode, the changes you make to a block are applied to all instances of the block in the design. The block edited in the master mode can be used as a stand-alone block.

The top-level or root design is always opened for editing in the master mode.

- Context mode—In this mode, the property and electrical constraint changes you make to a block are applied in context of the root design. However, the component and connectivity changes you make to the block are applied to all instances of the block in your design.

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Module 6: Creating a Hierarchical Design

Procedure

1. Open the `cache_1` block in the context mode. For this, double-click the `cache_1` block in the Hierarchy Viewer.

A new tab for the `cache` block opens. Notice that the titlebar displays the following text:

[In Context:`processor.cache_1`]

This indicates that the block with the block named `cache_1` is open in the context of the design named `processor`.

2. Select the `i1` instance in the Component List.
3. Connect the pins `D<0..7>` with the `VD<0..7> IN` port.
4. Connect the pins `CLK` with the `VCLKA IN` port.
5. Ground the `OE` pin. For this, connect the `OE` pin with the `GND` signal.

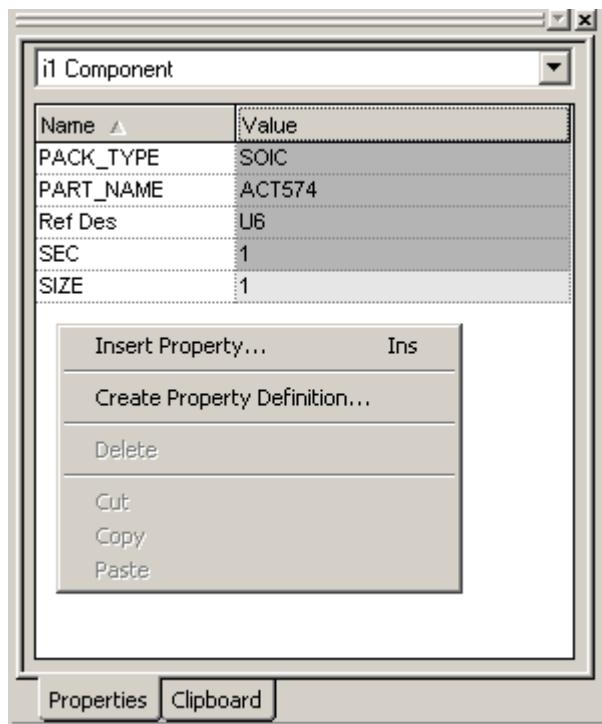
The connectivity changes are applied to the `cache` design. These changes will appear in all instances of the `cache` block.

6. Select *View–Properties Window* to open the Properties window.
7. Select the `i1` instance in the Component List.
8. Right-click in the Properties window to display the pop-up menu and select the *Insert Property* command.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

A new property row appears.



9. Specify the property name as `BOM_IGNORE` and the value as `TRUE` and press Enter.

A message box stating that the property changes to this (cache) block will be written to the property file of the master parent (processor) design appears.

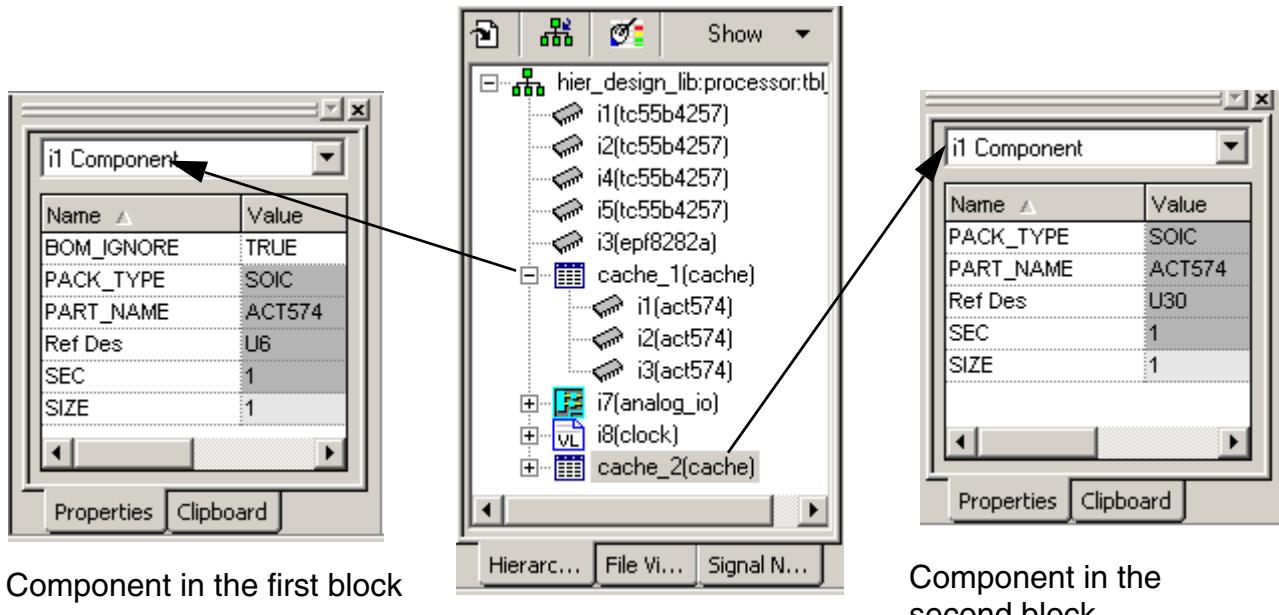


10. Click **OK**.
11. Select the `i1` component that has the `Ref Des` value `U30` in the `cache_2` block in the Hierarchy Viewer.

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Module 6: Creating a Hierarchical Design

Notice that the Properties Window refreshes.



Component in the first block

Component in the second block

Notice that the Properties window does not show the BOM_IGNORE property you added in the i1 component in the cache_1 block. The property changes made in the context mode are applied to the property file of the master parent (processor) design and not in the property file of the cache block. As a result, only the impacted cache block instance in the master design processor is changed.

12. Select the cache_2 block in the Hierarchy Viewer.

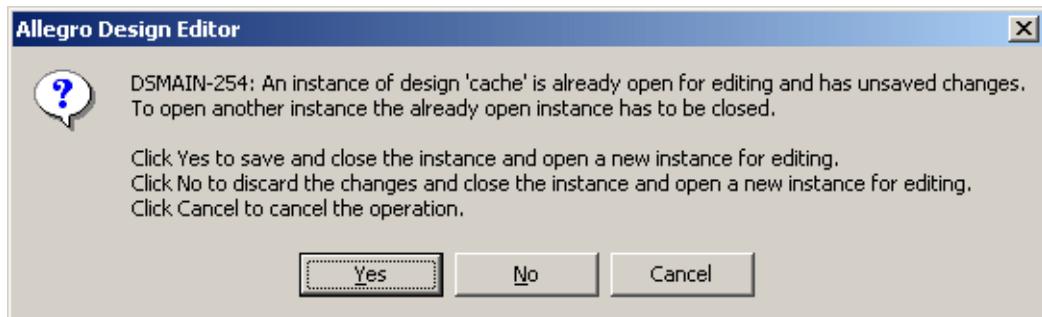
13. Click the Descend tool button.

A message box stating that you already have an instance (cache_1) open for editing appears. You are trying to open

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

another instance of the same design block. The message prompts you to save or discard the changes.



14. Click **Yes** to save the changes.

A tab for the `cache_2` block opens. Notice that the connectivity changes you made for the component with the instance name `i1` in the other instance of the `cache` block are available in the component with the instance name `i1` of the current block. If you make connectivity changes for any component in a block in the Context mode, then the changes are always made in context of the root design. As a result, these connectivity changes appear in all instances of the block under the root design.

15. Assign the `BOM_IGNORE` property with the value `TRUE` to the component with the instance name `i2`.
16. Click *OK* to close the message box.
17. Press `Ctrl+Shift+S` or select *File–Save All* to save changes to all blocks.

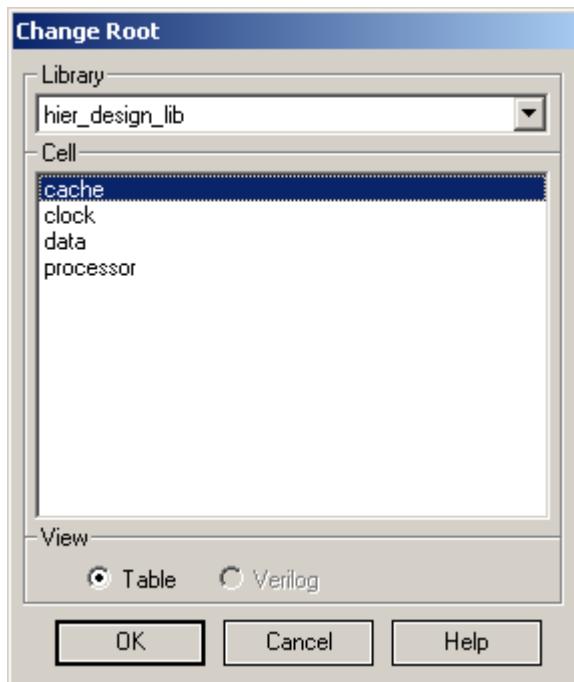
The `cache` block is saved, and the changes made to it will appear in context of the `processor` block. Changes in the `processor` design are also saved.

18. Select *Project–Change Root* for changing the root design for the project.

System Connectivity Manager Tutorial

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The Change Root dialog box appears.



19. Select the `cache` block and click *OK*.

Notice that the root design changes to `cache`.

hier_design_lib:cache:tbl_1

20. Select the `i1` component in the `cache` block.

Notice that the Properties window refreshes and it does not show the `BOM_IGNORE` property you added in the `i1` component in the `cache_1` block in the Context mode earlier. The reason stems from the fact that the property changes made in the context mode are applied to the property file of the master parent (`processor`) design and not `cache` block.

21. Select the component with the instance name `i3` and assign the `BOM_IGNORE` property with value `TRUE` on it.
22. Select *Project – Change Root* for changing the root design back to `processor`.

Note: If you get a message box to save unsaved designs, click `Yes`.

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Module 6: Creating a Hierarchical Design

The processor block appears as the root design.

23. Double-click the cache_1 block in the Hierarchy Viewer.

The cache block opens.

24. Select the i3 instance of the cache_1 block in the Hierarchy Viewer.

The BOM_IGNORE property is listed as an assigned property in the Properties window. The value assigned to this property is TRUE.

25. Similarly, check the properties of the i3 instance in the cache_2 block.

The BOM_IGNORE property with value TRUE is listed as an assigned property in the Property window for this instance too. Changes to properties made in master mode are available across all instances of the design.

Summary

In this lesson, you learned to edit blocks in master and context mode.

For More Information

See:

[Working with Hierarchical Designs](#) chapter of *System Connectivity Manager User Guide*.

Lesson 6-6: Creating a Third-Level Hierarchical Design

Overview

In this lesson, you will learn to create a block and add it in a mid-level design block.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

Procedure

1. Select *Project – Change Root* and change the root design back to cache.

Note: If you get a message box to save unsaved designs, click *Yes*.

2. Choose *Design–Create Block*.

The Create Block dialog box appears.

3. Type `cache_ctrl` in the *Block Name* field.

The *Block Library* field shows that the new block being created will be added in the `hier_design_lib`. Retain this setting.

4. Click the *Add Ports* button.

5. To add an input port `dq<7..0>`, type `dq<7..0>` in the *Port Name* field and press *Tab* to move the *Port Type* field.

6. Type `IN` or select it from the *Port Type* drop-down list.

7. Repeat steps step 5 and step 6 to add the input ports, `gain`, `vclk`, and `vref`, and an output port named `out`.

8. Select the *Add instance to design* check box to add an instance of the new block in the `cache` block.

9. Click *OK* to store the `cache_ctrl` cell in the `hier_design_lib` library.

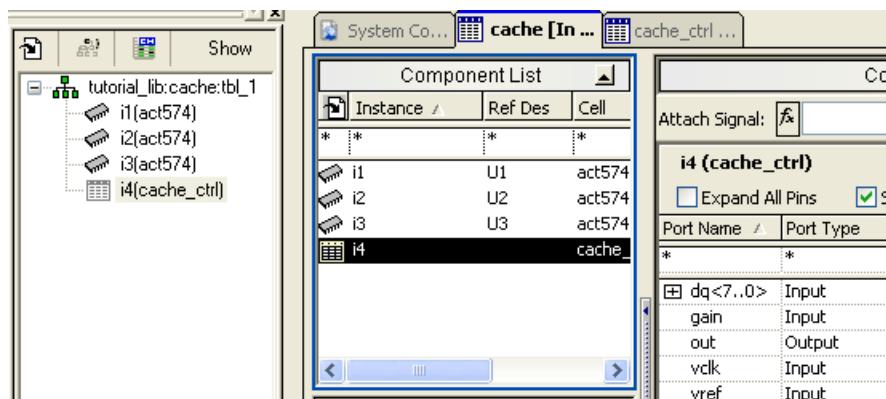
The Block Packaging Options dialog box appears.

10. Click *Apply* to accept the default packaging option.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

Notice that a new block named `cache_ctrl` appears as an instance in the Component List and also appears in the Hierarchy Viewer.



11. To save the design, choose *File – Save All*.
12. Select *Project–Change Root* for changing the root design back to `processor`.
The `processor` block appears as the root design.
13. Double-click the `cache_1` block.
The block expands and you can see the `cache_ctrl` block in it. You have a three level design hierarchy ready.
14. Select *File–Save All* to save the design.

Summary

In this lesson, you learned to create a three-level design hierarchy by creating a block and adding it in a mid-level design block. You have added this block using the top-down hierarchical design methodology.

For More Information

See:

[Working with Hierarchical Designs](#) chapter of *System Connectivity Manager User Guide*.

Lesson 6-7: Creating a Bottom-Up Hierarchical Design

Overview

In this lesson, you will learn to create a bottom-up hierarchical design.

Concept

In the bottom-up methodology, you create a lower-level standalone block first and add it to a library. After a block is finalized, it can be integrated into the root design.

In this procedure, you will add a lower level block `data` as a sub-block in the `cache` block.

Procedure

1. Select *Project–Change Root* and change the root design back to `cache`.
2. If you get a message box to save unsaved designs, click *Yes*.
3. Click the *Add Component* tool button ().
4. Select all libraries and type `data` in the *Cells* field.
5. Select the `data` cell.
6. Click the *Add* button.
The Block Packaging Options dialog box appears.
7. Select the *Use Ref. Des. Range* option button, type `40` to `49` in the adjacent field, and click *Apply*.
A new instance of the `data` block appears.
8. Close Part Information Manager.
9. Double-click the `data` cell in the Hierarchy Viewer, to open the tab for the new `data` block instance.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

Notice that the three instances of the tlc5602 part appear with the reference designators, U40, U41, and U42.

10. Close the data block.

You have created a hierarchical design by adding it bottom-up.

Next, you will learn how to mask global signals.

11. Scroll the Signal List of the cache block.

Notice that the signals VCC_D and GND_D appear in the Signal list of the cache block. These signals are global signals in the data block and are rippled up in the hierarchy.

12. Select the data block in the Component List.

13. Select *Object – Block Packaging Options*.

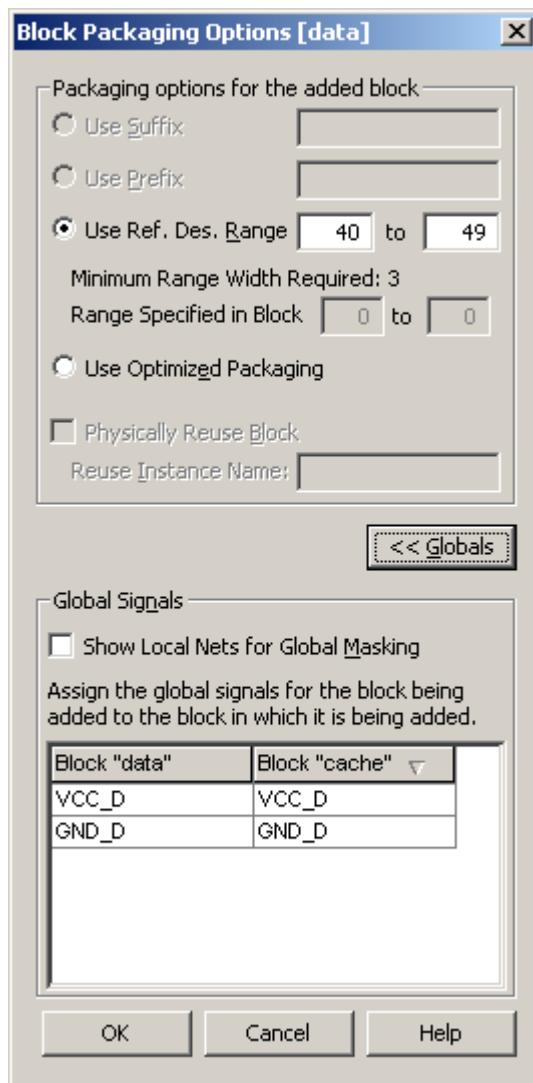
The Block Packaging Options dialog box appears.

14. Click the *Globals* button to display the *Global Signals* list.

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The Block Packaging Options dialog box expands to display the Global Signals list.



15. Alias the signal VCC_D in the data block with the signal VCC in the cache block. For this, select VCC in the cell in the same row as the VCC_D signal as shown below:

| Block "data" | Block "cache" |
|--------------|-------------------|
| VCC_D | VCC_D |
| GND_D | VCC GND VCC |

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Module 6: Creating a Hierarchical Design

16. Similarly, alias the signal `GND_D` in the `data` block with the signal `GND` in the `cache` block.
17. Click *Apply* to accept the changes in the Block Packaging Options dialog box.
Notice that the signals `VCC_D` and `GND_D` are removed from the Signal List. Instead, the signals they are aliased to—`VCC` and `GND`—appear in the list.
18. Select *Project—Change Root* and set the root design as processor.

Summary

In this lesson, you learned to create a hierarchical design following the bottom-up design methodology. You also learned to mask global signals.

For More Information

See:

[Working with Hierarchical Designs](#) chapter of *System Connectivity Manager User Guide*.

System Connectivity Manager Tutorial

Module 6: Creating a Hierarchical Design

Module 7: Generating Document Schematic

Prerequisite

If you have not completed all the lessons in [Module 6: Creating a Hierarchical Design](#), you must open the `hier_design.cpm` project located at
`<your_work_area>\modules\schgen\hier_design` in System Connectivity Manager and perform the steps described in this module.

For more information, see [Understanding the Sample Design Files](#) on page 16.

Lessons

This module consists of the following lessons:

- [Lesson 7-1: Setting the Project for Generating Document Schematic](#) on page 234
- [Lesson 7-2: Generating Document Schematic](#) on page 237
- [Lesson 7-3: Specifying Component Placement](#) on page 242
- [Lesson 7-4: Modifying Document Schematic](#) on page 245
- [Lesson 7-5: Regenerating Document Schematic](#) on page 248
- [Lesson 7-6: Exporting Design as a Schematic](#) on page 250

Multimedia Demonstration

 A Flash-based multimedia demonstration of this module, [Generating Document Schematic](#), is available on Cadence Online Support.

Completion Time

- 45 minutes for written lessons
- 15 minutes for multimedia demonstrations

Lesson 7-1: Setting the Project for Generating Document Schematic

Overview

System Connectivity Manager allows you to generate a schematic for your spreadsheet-based design. The generated schematic is strictly recommended for documentation purposes, and is therefore, referred to as document schematic. In this lesson, you will learn how to setup your design to successfully generate a document schematic.

Concept

Generating a document schematic is a useful feature supported by System Connectivity Manager. Using System Connectivity Manager, you can generate a flat schematic for your spreadsheet-based design.

To be able to generate a document schematic for your design, you first need to specify the options or the guidelines for generating the document schematic. For example, you need to specify the location of `cref.dat` to be used for generating the schematic pages. Similarly, you also need to specify if the schematic generation process should stop in case of errors or continue after reporting the problem as a warning.

Procedure

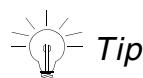
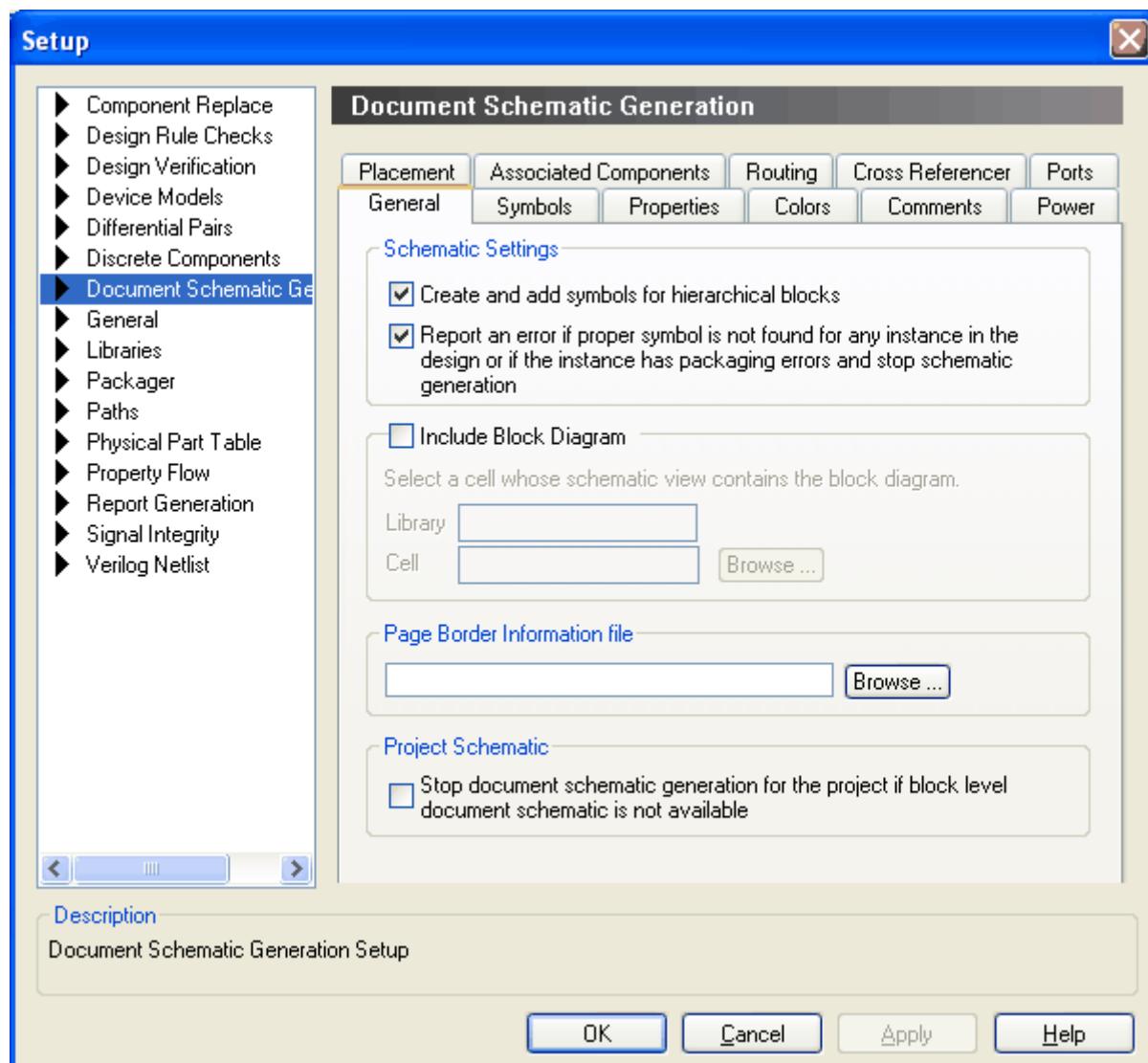
To specify the setup options, complete the following steps.

1. Choose *Project – Settings*.
2. From the list box, select *Document Schematic Generation*.

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Module 7: Generating Document Schematic

The Document Schematic Generation tab appears.



Tip
Setup options for generating document schematic can also be displayed by selecting *Project – Generate Schematic* and clicking the *Setup* button.

3. To ensure that the hierarchical blocks in the design are represented by a symbol, select the *Create and add symbol for hierarchical blocks* check box.

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Module 7: Generating Document Schematic

4. Specify the location of the `cref.dat` file to be used for generating the document schematic. Use the `cref.dat` file located at `<your_work_area>\reference\cdssetup`.

While generating document schematic, the page border information in the `cref.dat` file is used to compute the area available for drawing schematic.

5. You must add a page border to generate a document schematic. To add a page border, select the *Symbols* tab.
6. In the *Page Border* area, click *Browse* and specify the `lib:cell:view` from where the page border symbols are to be used or accept the default values.
7. To add offpage connectors to the generated document schematic, select the *Add Offpage Symbols* check box.
8. Specify the `lib:cell:view` from where the offpage symbols are to be used or accept the default values
9. Select the *Associated Components* tab.
10. Specify the maximum number of bypass capacitor that can be clubbed together in a rail in document schematic. Accept the default value of 100.
11. Click *OK*.

Summary

In this lesson, you learned to setup your design for generating document. You can specify options for adding symbols for blocks, running Cross Reference on the document schematic, and so on.

For More Information

See:

[Generating Document Schematic Setup](#) section in the *Dialog Box Description* chapter of *System Connectivity Manager User Guide*.

[Generating Document Schematic for a Design](#) chapter of *System Connectivity Manager User Guide*.

Lesson 7-2: Generating Document Schematic

Overview

In this lesson, you will learn to generate a document schematic.

Concept

System Connectivity Manager provides support for generating a schematic for a spreadsheet-based design. For a hierarchical design, first the document schematic is generated for all the blocks in the design. These are saved in `docsch_1` view for the block. The document schematic for the project is then generated using the document schematic for all the blocks instantiated in that project. The document schematic is saved in the `sch_1` view of the `<root block>_doc` folder in the library.

A document schematic is not generated for schematic blocks, that is, blocks created in Design Entry HDL, in the design. For these blocks, the schematic in the `sch_1` view is used as is in the project schematic.

Note: You can generate the schematic for a project from the command line. The command used is:

```
dsschgendocprog -proj <project_name>.cpm.
```

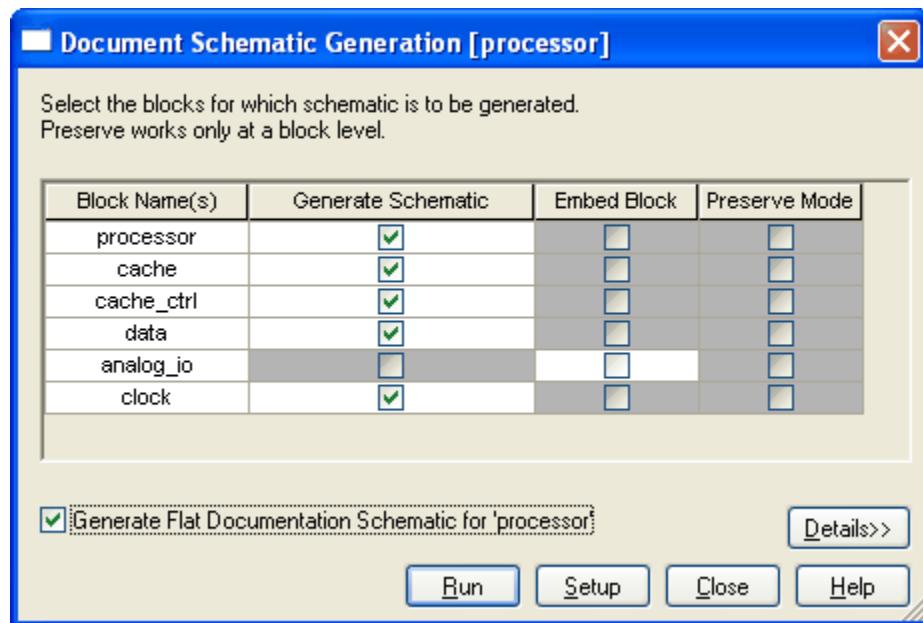
Procedure

1. Choose *Project – Generate Schematic*.

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Module 7: Generating Document Schematic

The Document Schematic Generation dialog box appears.



2. In the Generate Schematic column, select the check box corresponding to the block for which you want to generate the block schematic. Accept the default selection.

By default, all the blocks except that schematic block, `analog_io`, are selected. The *Generate Schematic* check box is not enabled for `analog_io`.

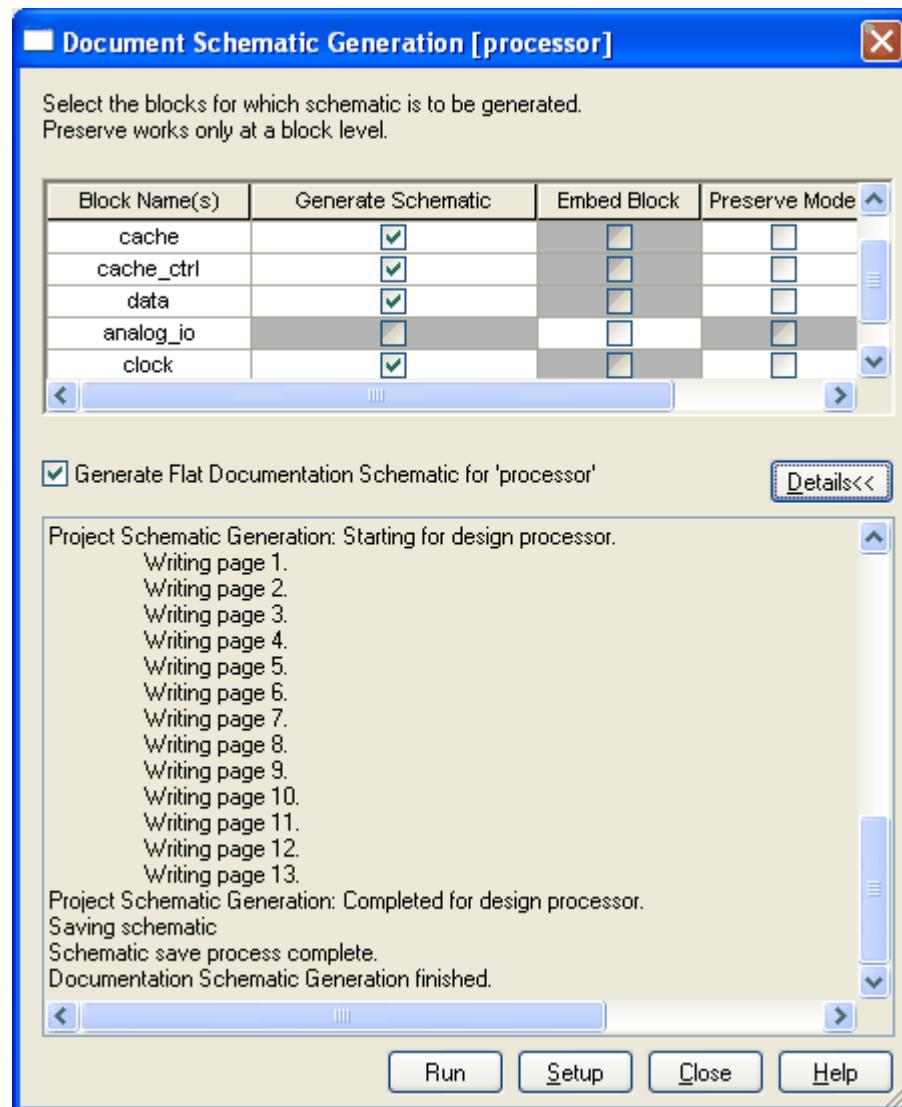
3. To create the document schematic for the project, select the *Generate Flat Documentation Schematic for 'processor'* check box. Click Run.

The schematic generation process starts.

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Module 7: Generating Document Schematic

4. To view the messages and warnings that are being generated, click the *Details* button.



5. Click *Close* to close Document Schematic Generation dialog box.

Viewing Block Schematic

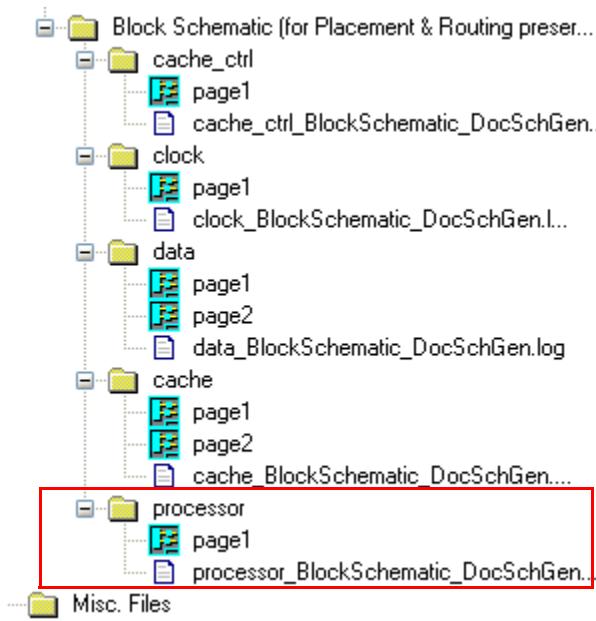
To view the block schematic for the processor block, perform the following steps:

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Module 7: Generating Document Schematic

1. In System Connectivity Manager, select the *File Viewer* tab.

As shown in the figure below, the pages in the block schematic for all the blocks are available in the Block Schematic folder located in the Output Files folder.



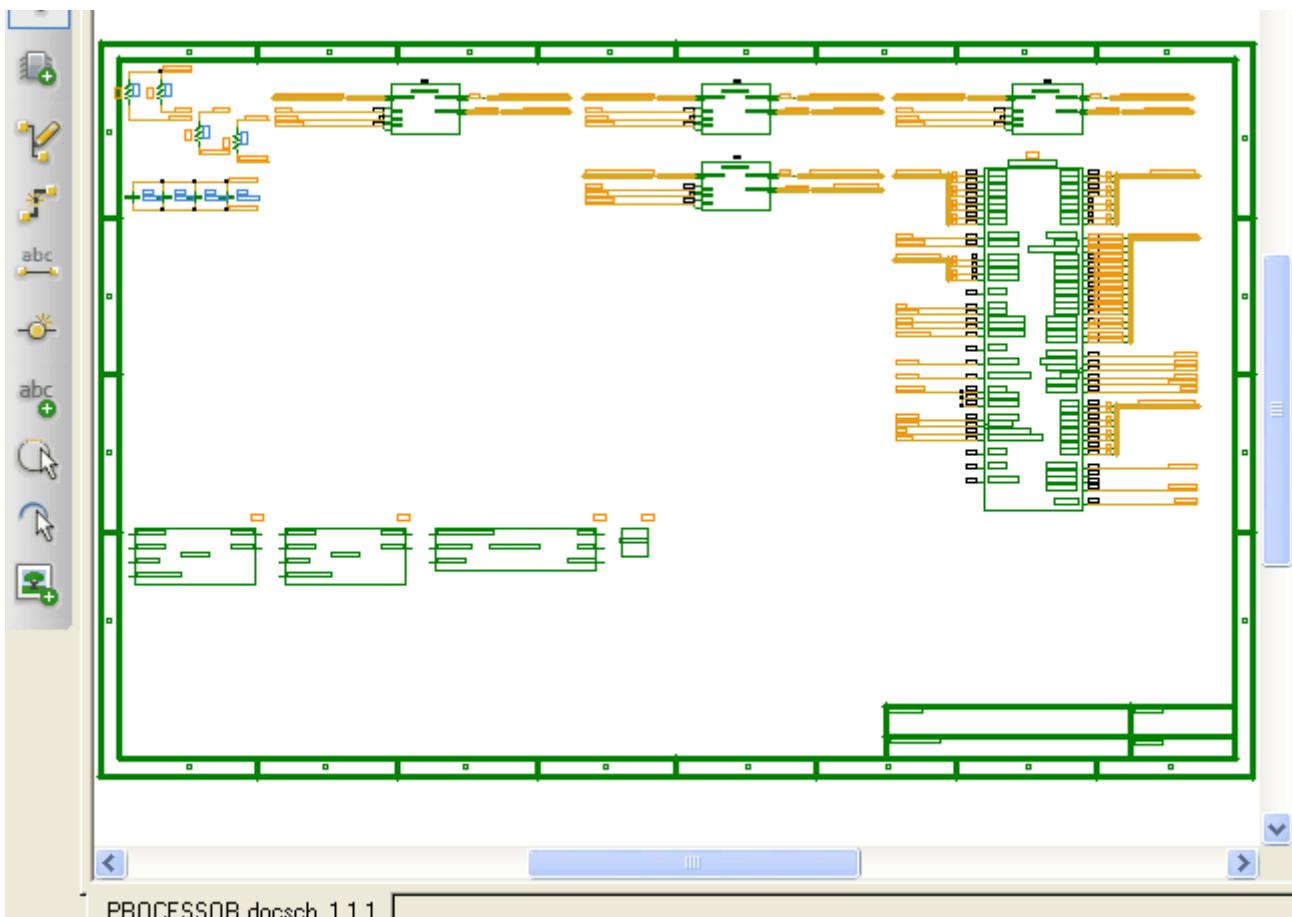
Note that the block schematic for the root design, `processor`, has only one page. This indicates that the project schematic is generated by concatenating the document schematic for all the block in the root design.

2. To open the document schematic for the processor block, right-click on `page1` below the `processor` folder.
3. From the pop-up menu, choose *Open schematic for preserve in Design Entry HDL*.

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Module 7: Generating Document Schematic

The block schematic for the `processor` block opens in Design Entry HDL.



Note that the schematic in page 1 of the block schematic, `PROCESSOR.DOC SCH_1.1.1`, is same as the schematic in the `PROCESSOR_DOC.SCH.1.1` page of the flat documentation schematic.

Summary

In this lesson, you learned to generate document schematic for your project and also for the blocks in your project.

For More Information

See:

Generating Document Schematic for a Design chapter of
System Connectivity Manager User Guide.

Lesson 7-3: Specifying Component Placement

Overview

In this lesson, you will learn to use the Placement tab to specify the component placement options for placing components on the generated document schematic.

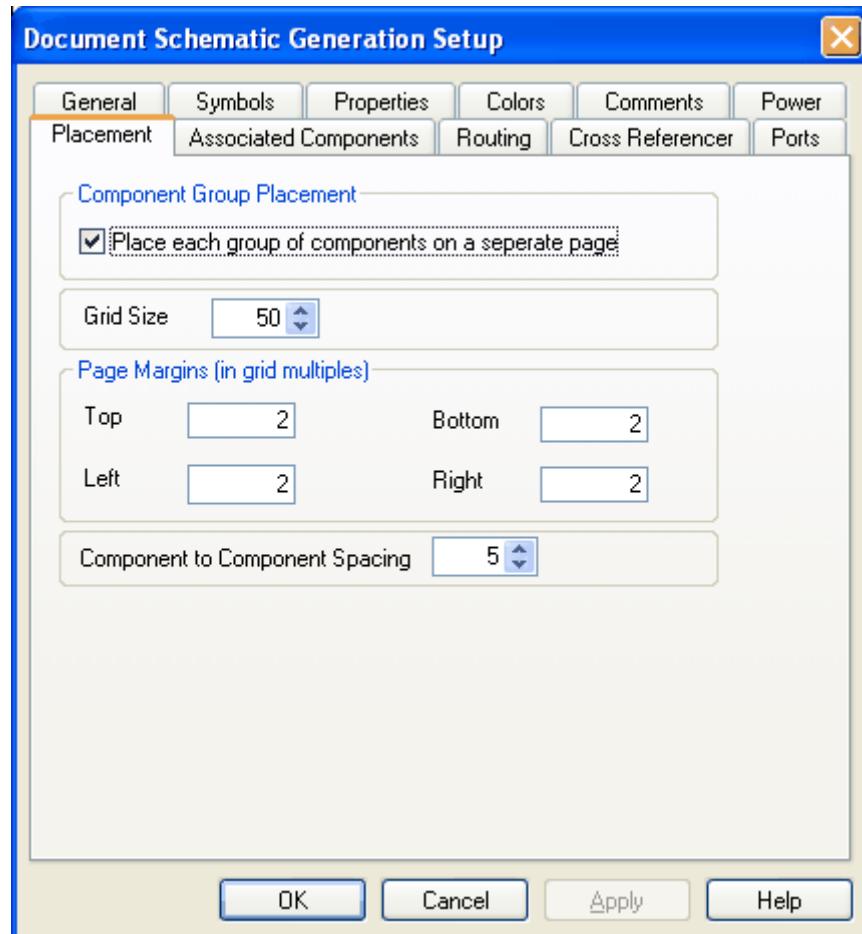
Procedure

1. Choose *Project – Generate Schematics*.
2. Click *setup*.
3. The Document Generation Setup box appears.
4. Select the Placement tab.
5. Select the *Place each group of components on a separate page* check box.
6. Specify the Grid size as 50.

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Module 7: Generating Document Schematic

7. Specify the other options as shown in the following figure:

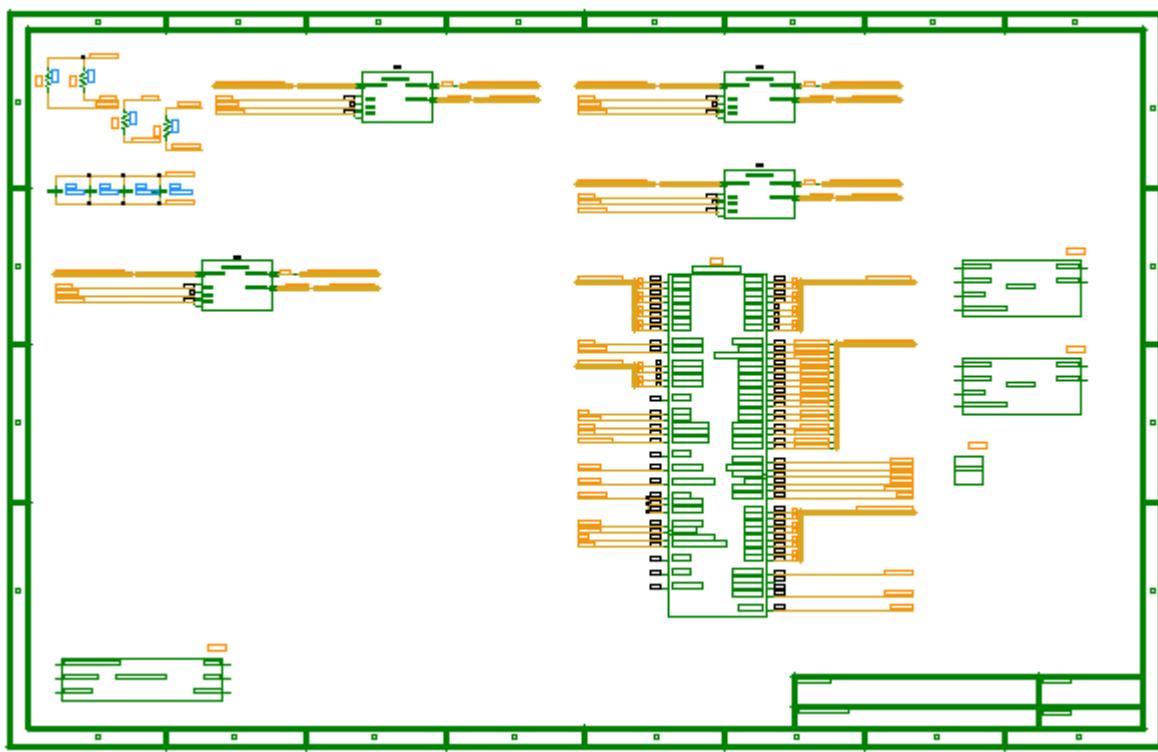


8. Click **Ok**.
9. To open the document schematic for the processor block, right-click on `page1` below the `processor` folder.
10. From the pop-up menu, choose *Open schematic for preserve in Design Entry HDL*.

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The block schematic for the `processor` block opens in Design Entry HDL.



Notice that the components are placed as per the specifications defined.

Summary

In this lesson, you learned to use the Placement tab to property specify the component placement options for placing components on the generated document schematic.

For More Information

See:

[Generating Document Schematic for a Design](#) chapter of [System Connectivity Manager User Guide](#).

Lesson 7-4: Modifying Document Schematic

Overview

In this lesson, you will learn to modify the document schematic to meet your requirements. You will learn about the modification that can be made to the schematic, such that the changes are preserved on regenerating the schematic. You might want to modify the document schematic to reduce the number of pages in the document schematic, or to modify the component placement by grouping a set of components together in a schematic.

Concept

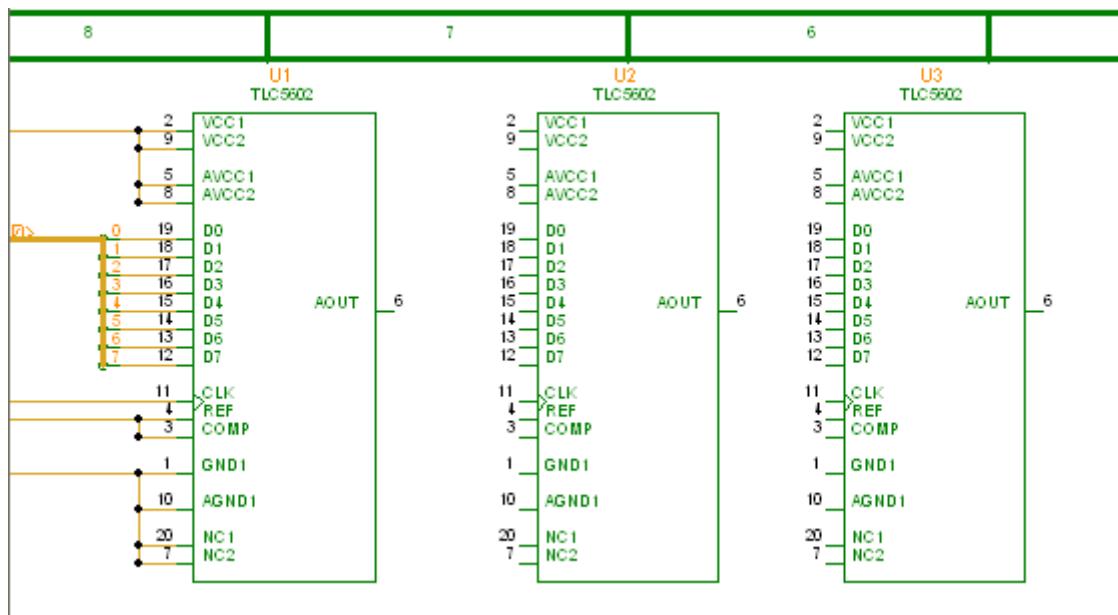
While modifying the document schematic, you need to ensure that all modifications are made to the block schematic in the `docsch_1` view. This is required because changes to the project schematic — saved in the `sch_1` view — cannot be preserved. You can modify the document schematic by making placement and routing modifications to the design. In this section, you will modify the schematic for the data block.

System Connectivity Manager Tutorial

Module 7: Generating Document Schematic

Procedure

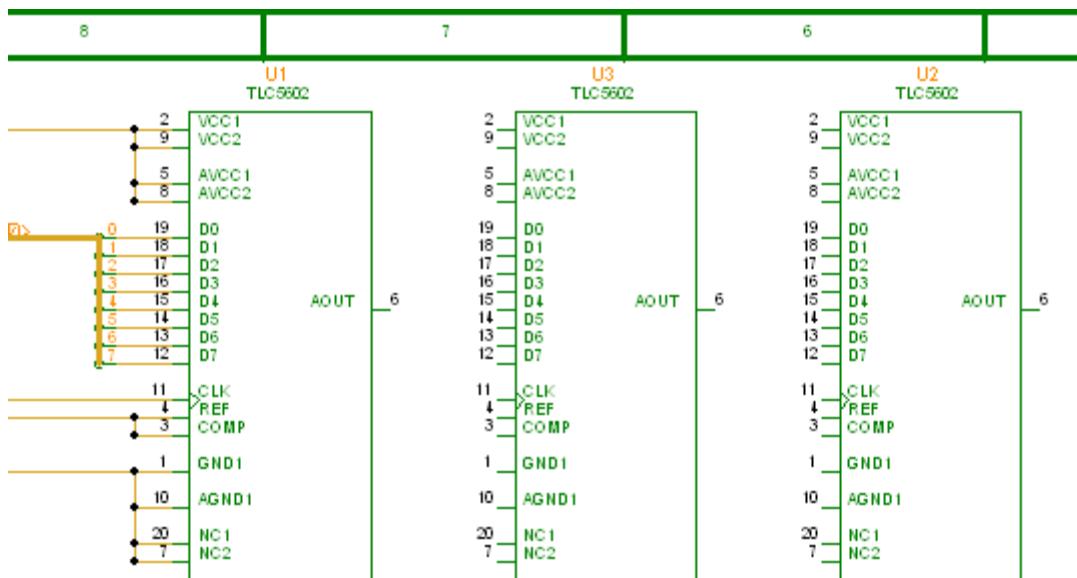
1. Open the document schematic for the data block in Design Entry HDL.



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Module 7: Generating Document Schematic

2. Modify the component placement, by swapping the placement of U2 and U3, as shown in the following figure:



3. Save the design in Design Entry HDL.

You will now modify the data block in System Connectivity Manager.

4. To make data as the root design, click
5. In the Change Root dialog box, select data and click OK.
6. Modify the connectivity by connecting the gnd1 and nc1 pins of instances i2 and i3 to the GND signal.
7. Save the design.
8. Make processor as the root design.

Lesson 7-5: Regenerating Document Schematic

Overview

In this lesson, you will learn to regenerate the document schematic such that the modifications made by you to the document schematic are not overridden. Only the modifications made to the block schematic can be preserved while regenerating the document schematic.

Procedure

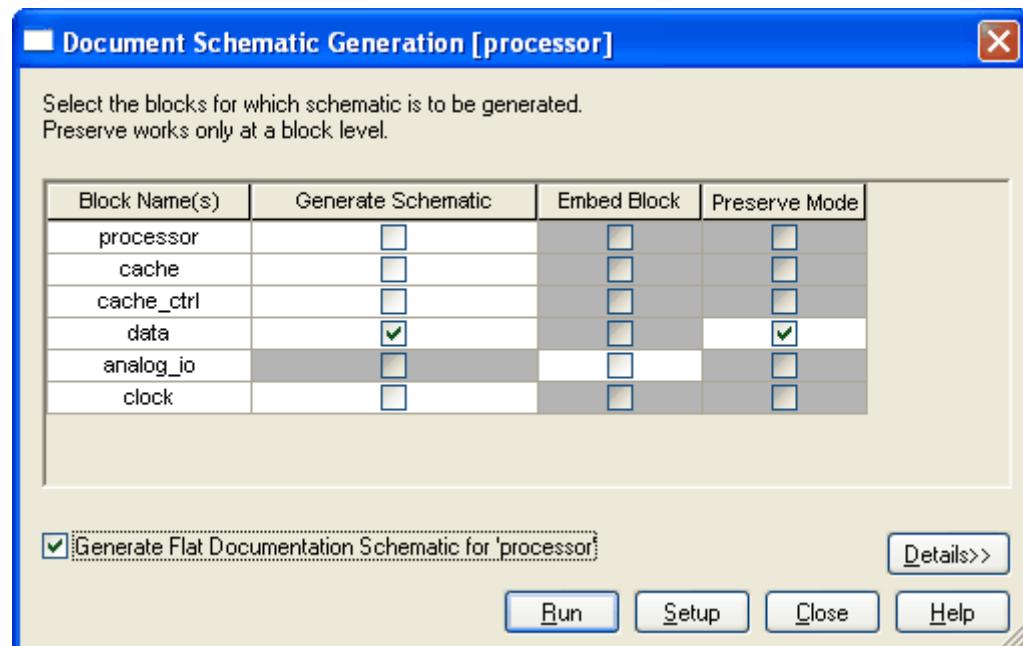
1. Choose *Project – Generate Schematics*.
2. In the Document Schematic Generation dialog box, select the *Generate Schematic* check box for the data block.
3. To preserve the placement changes made to the block schematic, select the *Preserve Mode* check box for the data block.

Note: Note that the *Preserve Mode* check box is enabled for all the non-schematic blocks in the design.

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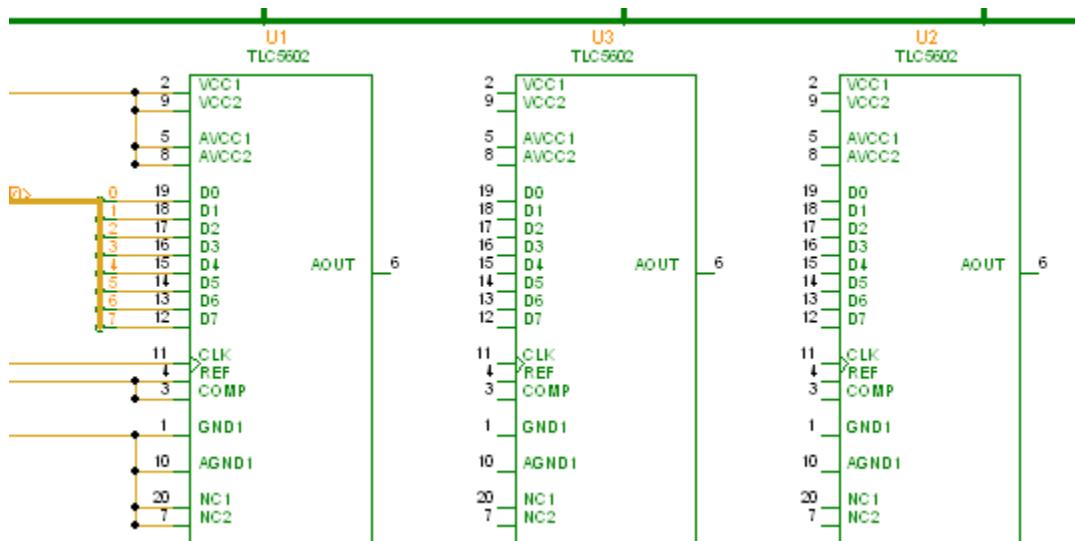
Module 7: Generating Document Schematic

4. Select the *Generate Flat Documentation Schematic for 'processor'* check box.



5. Click Run.

The generated document schematic opens in Design Entry HDL.



System Connectivity Manager Tutorial

Module 7: Generating Document Schematic

Note that the placement modifications made by you are preserved, and the schematic is also updated with the connectivity changes made in System Connectivity Manager.

Summary

In this lesson, you learned to regenerate the document schematic in the preserve mode, such that while the placement changes made to the schematic are saved, the schematic is also updated with the modifications in the spreadsheet-based design.

For More Information

See:

[*Generating Document Schematic for a Design*](#) chapter of [*System Connectivity Manager User Guide*](#).

Lesson 7-6: Exporting Design as a Schematic

Overview

In this lesson, you will learn to export your design as a schematic. You can open the exported schematic using Design Entry HDL to make modifications or continue with the same design. When you export the design as a schematic, a new Design Entry HDL project is created with schematic pages, libraries, and associated files. You also need to understand that the export schematic is a one way process.



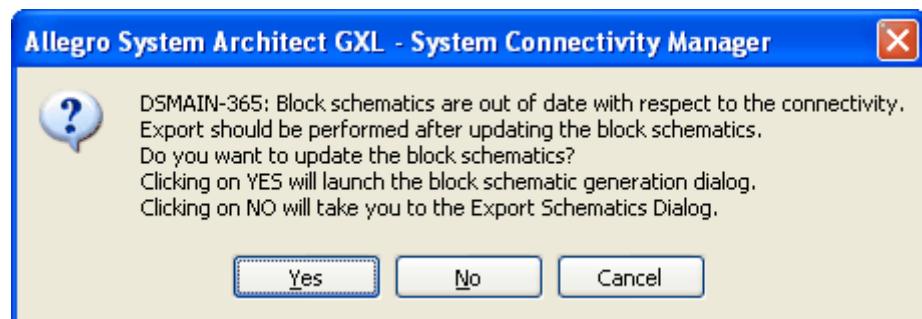
You cannot back-annotate any changes that you have made in the exported schematic to the spreadsheet-based design.

System Connectivity Manager Tutorial

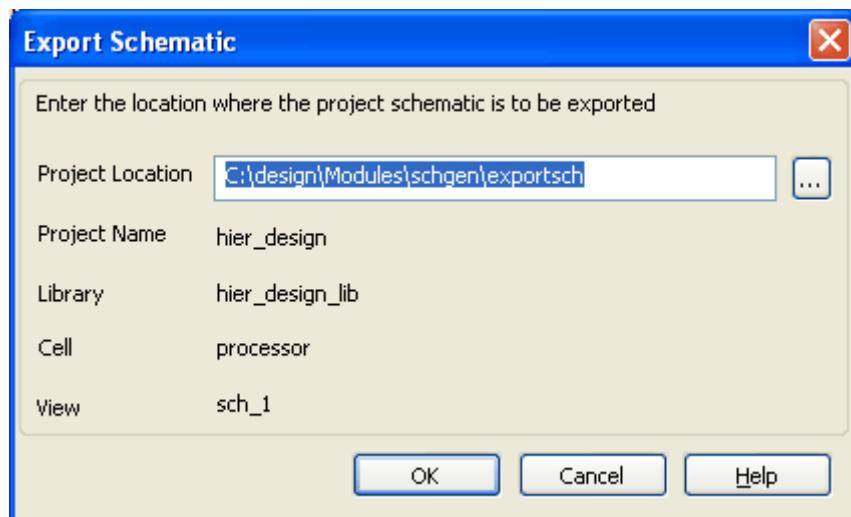
Module 7: Generating Document Schematic

Procedure

1. Choose *Project – Export-Schematics*.
2. If you have generated block schematics earlier, but they are out-of-date, a message displays. Click *Yes* to regenerate the block schematics or click *No* to use the existing block schematics.



3. The Export Schematic dialog box appears.



4. In the Project Location field, specify the directory to create the schematic project. by default the exported project is located in the exportsch directory located one level above the project folder.

The Project Name, Library, Cell, and View names are displayed for your reference.

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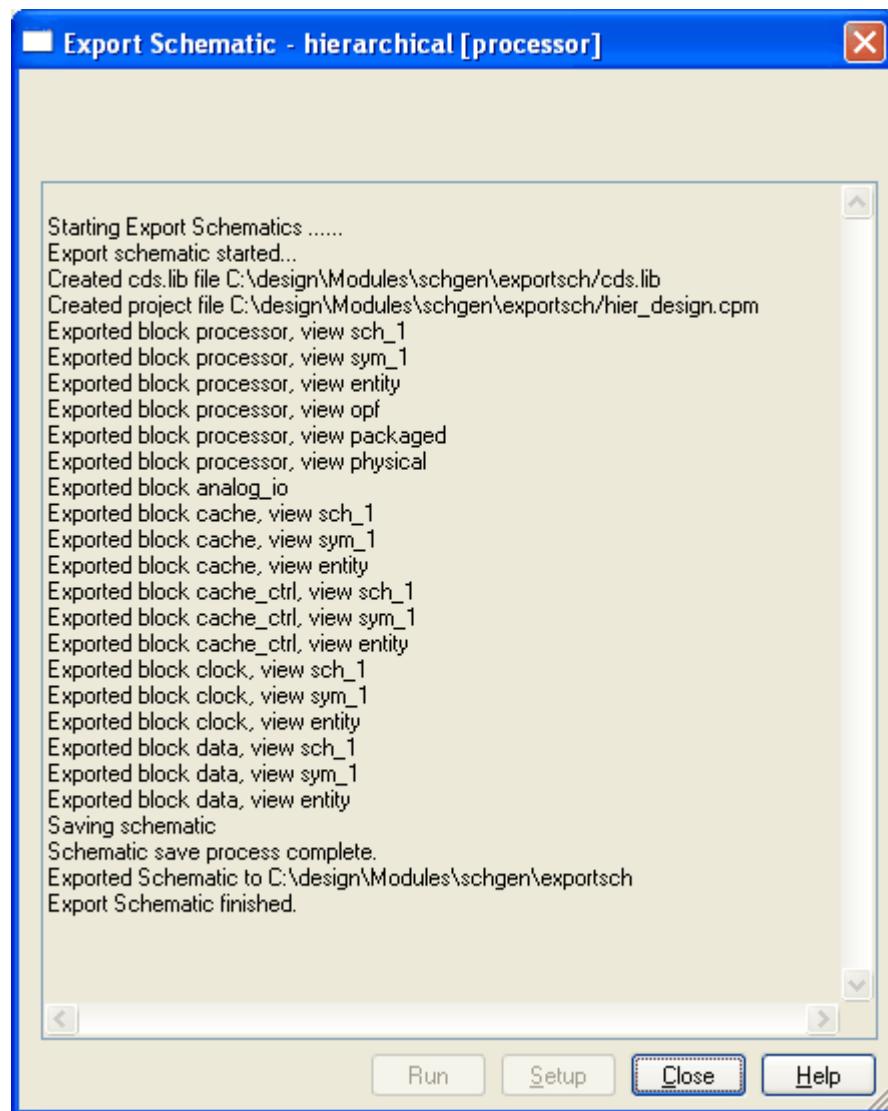
Module 7: Generating Document Schematic

5. Click *Ok* to Export the schematic. The Export Schematic dialog box displays the progress of the export process.

6. Click Close.

7. The exported schematic is saved in
C:\design\Modules\schgen\exportsch.

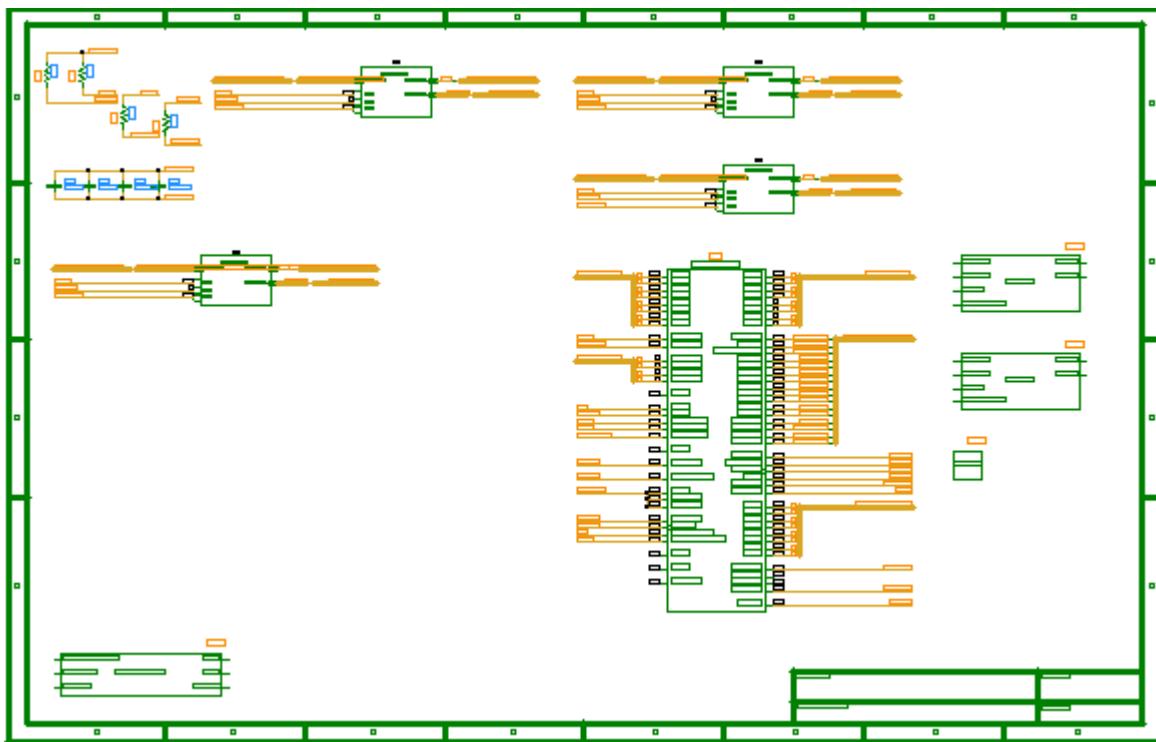
Note that the Project Name, Library, Cell, and View names are displayed for your reference.



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Module 7: Generating Document Schematic

8. Open the heir_design.cpm file in Design Entry HDL.



Summary

In this lesson, you learned to export your design as a schematic. You can open the exported schematic using Design Entry HDL to make modifications or continue with the same design.

For More Information

See:

Exporting Schematics for a Design chapter of *System Connectivity Manager User Guide*.

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Module 7: Generating Document Schematic

Module 8: Generating Reports

Prerequisite

If you have not completed all the lessons in [Module 6: Creating a Hierarchical Design](#), you must open the `hier_design.cpm` project located at
`<your_work_area>\modules\reports\hier_design` in System Connectivity Manager and perform the steps described in this module.

For more information, see [Understanding the Sample Design Files](#) on page 16.

Lessons

This module consists of the following lessons:

- [Lesson 8-1: Generating Standard Reports](#) on page 256
- [Lesson 8-2: Designing a Report Template](#) on page 261
- [Lesson 8-3: Customizing Existing Reports](#) on page 266
- [Lesson 8-4: Generating Block-Based Reports](#) on page 271
- [Lesson 8-5: Creating Cross-Tab Reports](#) on page 276
- [Lesson 8-6: Creating Custom Columns in Reports](#) on page 281

Multimedia Demonstration

 A Flash-based multimedia demonstration of this module, [Generating Reports Using System Connectivity Manager](#), is available on Cadence Online Support.

Completion Time

- 2 hours for written lessons

System Connectivity Manager Tutorial

Module 8: Generating Reports

- 45 minutes for multimedia demonstrations

Lesson 8-1: Generating Standard Reports

Overview

System Connectivity Manager has some default report templates that are shipped with the product. In this lesson, you will learn how to use these templates to generate reports and how to select the output format.

Concept

System Connectivity Manager provides powerful report design and generation features. You can even design report templates and then use the templates to generate reports for any design.

The Generate Report dialog box is used to generate reports in System Connectivity Manager. To create a report, you need a template file. You can select an existing report template to create a report, or customize the report template on the fly or create a new template and use it to generate the report. An example of a report template is BOM (Bill of Materials) report.

You can generate reports in the following formats:

- HTML
- CSV
- Text in Tabular Format
- Editable Report File Format, which is an intermediate report format provided by System Connectivity Manager. Using this editor, you can customize column sizes, have custom columns, change fonts of cells and add custom rows in a BOM report as required.

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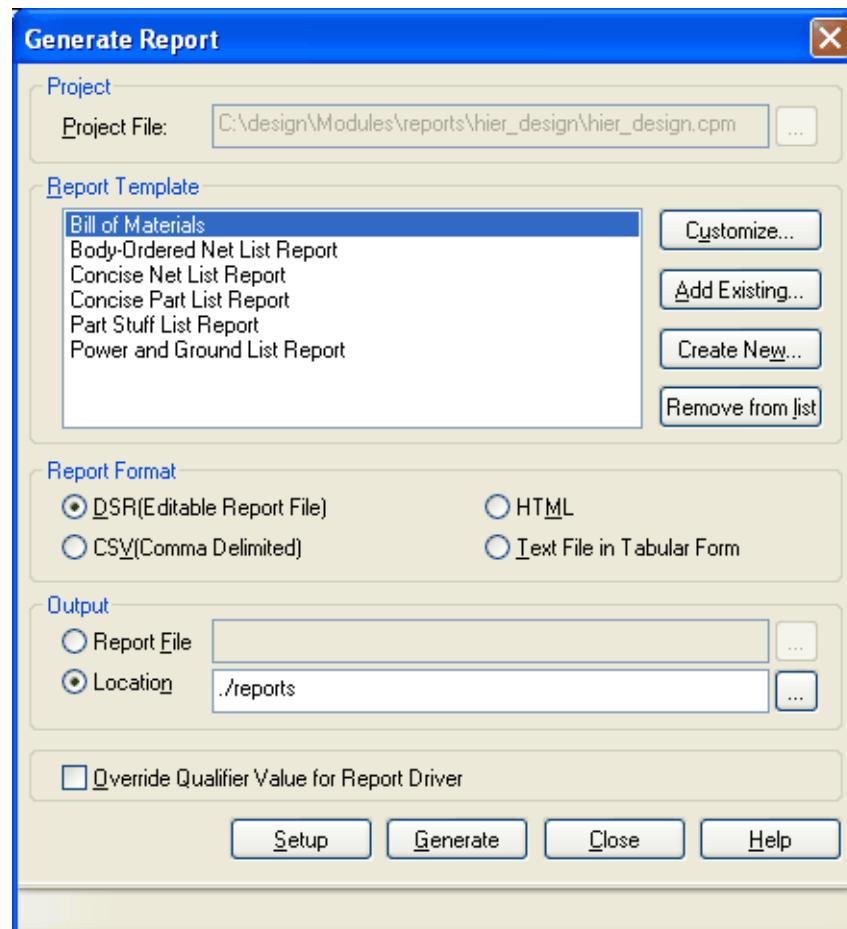
Procedure

Generating a Simple Report

1. Choose *Project – Reports – Generate Reports*.

Note: You can run the `dsreportgen -proj <project_name>.cpm` command from the command line.

The Generate Report dialog box appears.



Notice that the dialog box has the name of project already seeded in.

2. Select the *Bill of Materials* in the *Report Template* box.

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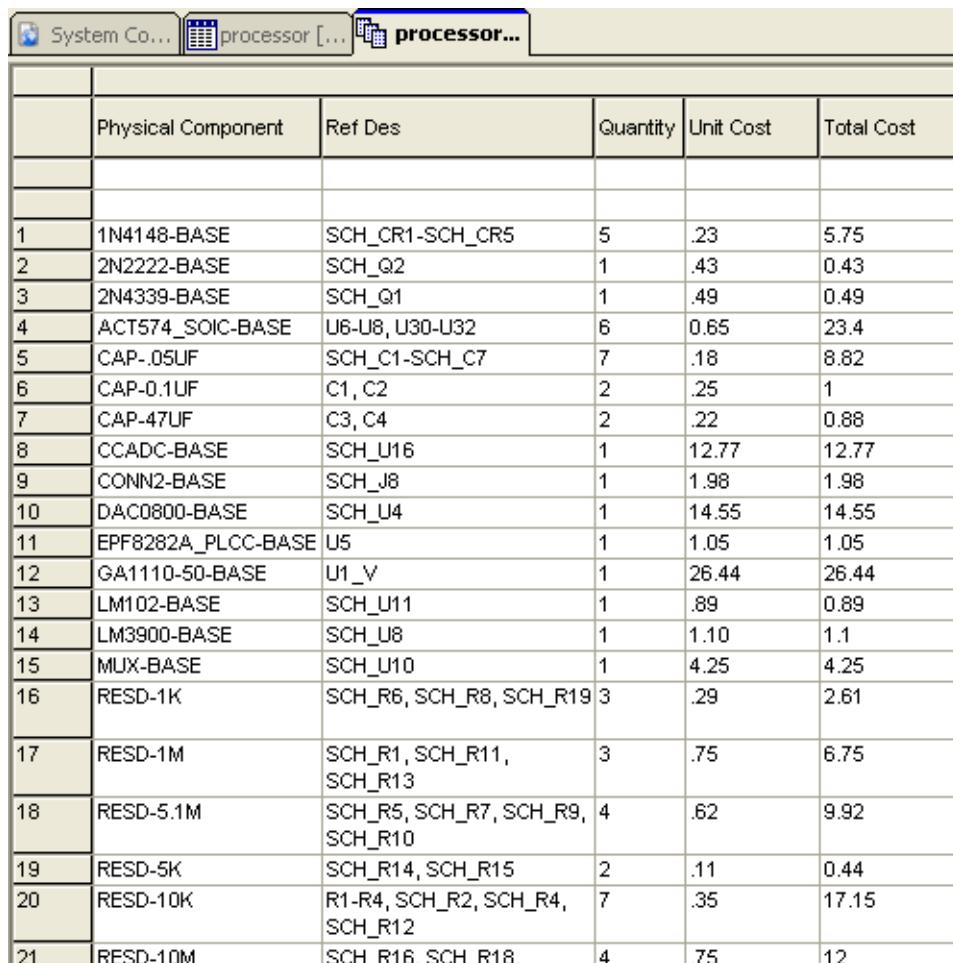
Module 8: Generating Reports

3. Select the *DSR (Editable Report File)* option button to specify the report format to be a custom editor within System Connectivity Manager.
4. Specify the output folder where the report will be located in the *Location* field.

Note: The default report location is the *reports* folder under the root design.

5. Click *Generate* to generate the report.

Notice that a new tabbed page appears titled *processor_Bill of Materials.dsr*.



The screenshot shows the System Connectivity Manager application window. At the top, there are three tabs: "System Co...", "processor [...]", and "processor...". The "processor..." tab is currently selected and highlighted in blue. Below the tabs is a large table representing a Bill of Materials (BOM) for a design named "processor". The table has columns for Physical Component, Ref Des, Quantity, Unit Cost, and Total Cost. The data is organized into 21 rows, each corresponding to a component listed with its reference designator and quantity. The total cost for all components is 12.00.

| | Physical Component | Ref Des | Quantity | Unit Cost | Total Cost |
|----|--------------------|---------------------------------|----------|-----------|------------|
| 1 | 1N4148-BASE | SCH_CR1-SCH_CR5 | 5 | .23 | 5.75 |
| 2 | 2N2222-BASE | SCH_Q2 | 1 | .43 | 0.43 |
| 3 | 2N4339-BASE | SCH_Q1 | 1 | .49 | 0.49 |
| 4 | ACT574_SOIC-BASE | U6-U8, U30-U32 | 6 | 0.65 | 23.4 |
| 5 | CAP-.05UF | SCH_C1-SCH_C7 | 7 | .18 | 8.82 |
| 6 | CAP-0.1UF | C1, C2 | 2 | .25 | 1 |
| 7 | CAP-47UF | C3, C4 | 2 | .22 | 0.88 |
| 8 | CCADC-BASE | SCH_U16 | 1 | 12.77 | 12.77 |
| 9 | CONN2-BASE | SCH_J8 | 1 | 1.98 | 1.98 |
| 10 | DAC0800-BASE | SCH_U4 | 1 | 14.55 | 14.55 |
| 11 | EPF8282A_PLCC-BASE | U5 | 1 | 1.05 | 1.05 |
| 12 | GA1110-50-BASE | U1_V | 1 | 26.44 | 26.44 |
| 13 | LM102-BASE | SCH_U11 | 1 | .89 | 0.89 |
| 14 | LM3900-BASE | SCH_U8 | 1 | 1.10 | 1.1 |
| 15 | MUX-BASE | SCH_U10 | 1 | 4.25 | 4.25 |
| 16 | RESD-1K | SCH_R6, SCH_R8, SCH_R19 | 3 | .29 | 2.61 |
| 17 | RESD-1M | SCH_R1, SCH_R11, SCH_R13 | 3 | .75 | 6.75 |
| 18 | RESD-5.1M | SCH_R5, SCH_R7, SCH_R9, SCH_R10 | 4 | .62 | 9.92 |
| 19 | RESD-5K | SCH_R14, SCH_R15 | 2 | .11 | 0.44 |
| 20 | RESD-10K | R1-R4, SCH_R2, SCH_R4, SCH_R12 | 7 | .35 | 17.15 |
| 21 | RESD-10M | SCH_R16, SCH_R18, | 4 | .75 | 12 |

Notice that the report has as many rows as the number of physical components in designs. There are five columns listing Physical Component, Ref Des, Quantity, Unit Cost and

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Total Cost. Depending upon the report template selected, the number of rows and columns displayed will change.

6. Select *File – Close* to close the tab for the BOM report.

Changing Report Formats

1. Choose *Project – Reports – Generate Reports*.
2. Select *HTML* in the *Report Format* box.
3. Click *Generate*.

Notice that a new tabbed page appears displaying the html report. This report is displayed in a tabbed page titled `processor_Bill of Materials.html` file.



| | Physical Component | Ref Des | Quantity | Unit Cost | Total Cost |
|----|--------------------|-------------------------|----------|-----------|------------|
| 1 | 1N4148-BASE | SCH_CR1-SCH_CR5 | 5 | .23 | 5.75 |
| 2 | 2N2222-BASE | SCH_Q2 | 1 | .43 | 0.43 |
| 3 | 2N4339-BASE | SCH_Q1 | 1 | .49 | 0.49 |
| 4 | ACT574_SOIC-BASE | U6-U8, U30-U32 | 6 | 0.65 | 23.4 |
| 5 | CAP-.05UF | SCH_C1-SCH_C7 | 7 | .18 | 8.82 |
| 6 | CAP-0.1UF | C1, C2 | 2 | .25 | 1 |
| 7 | CAP-47UF | C3, C4 | 2 | .22 | 0.88 |
| 8 | CCADC-BASE | SCH_U16 | 1 | 12.77 | 12.77 |
| 9 | CONN2-BASE | SCH_J8 | 1 | 1.98 | 1.98 |
| 10 | DAC0800-BASE | SCH_U4 | 1 | 14.55 | 14.55 |
| 11 | EPF8282A_PLCC-BASE | U5 | 1 | 1.05 | 1.05 |
| 12 | GA1110-50-BASE | U1_V | 1 | 26.44 | 26.44 |
| 13 | LM102-BASE | SCH_U11 | 1 | .89 | 0.89 |
| 14 | LM3900-BASE | SCH_U8 | 1 | 1.10 | 1.1 |
| 15 | MUX-BASE | SCH_U10 | 1 | 4.25 | 4.25 |
| 16 | RESD-1K | SCH_R8, SCH_R8, SCH_R19 | 3 | .29 | 2.61 |

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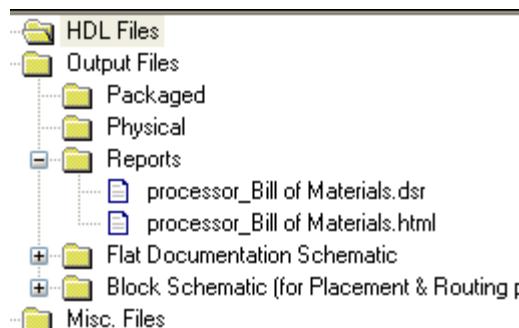
You can repeat the above steps to generate a CSV format report. The CSV report is displayed in a tabbed page titled processor_Bill of Materials.csv. You can open this file in Microsoft Excel.

4. Select *File – Close* to close the tab for the BOM report.

Viewing Reports from the File Viewer

1. Choose *View – File Viewer*.

The File Viewer appears. The File Viewer displays the files related to your design and lets you open the files from System Connectivity Manager.



2. Double-click processor_Bill of Materials.dsr.

The selected report opens in a new tab. The information displayed in this tab is same as one generated in [step 5 of Generating a Simple Report](#) section.

3. Select *File – Close* to close the tab for the BOM report.

Summary

In this lesson, you learned to create reports for your design. You can create a standard report in different file formats. You can format reports created in the .dsr format. You can add new columns or rows in generated reports.

For More Information

See:

[Creating Reports](#) chapter of *System Connectivity Manager User Guide*.

Lesson 8-2: Designing a Report Template

Overview

In this lesson, you will learn to create a report template and use it to generate reports.

Concept

System Connectivity Manager uses report template (.tpt) files to create reports. You can create a new report template file or customize an existing report template from the Generate Report dialog. A custom report allows you to define the order of keywords that will generate the query. You can change the view and sorting order, visibility, alignment, width, and other such characteristics in the report.

For this tutorial, you will create a new report template file.

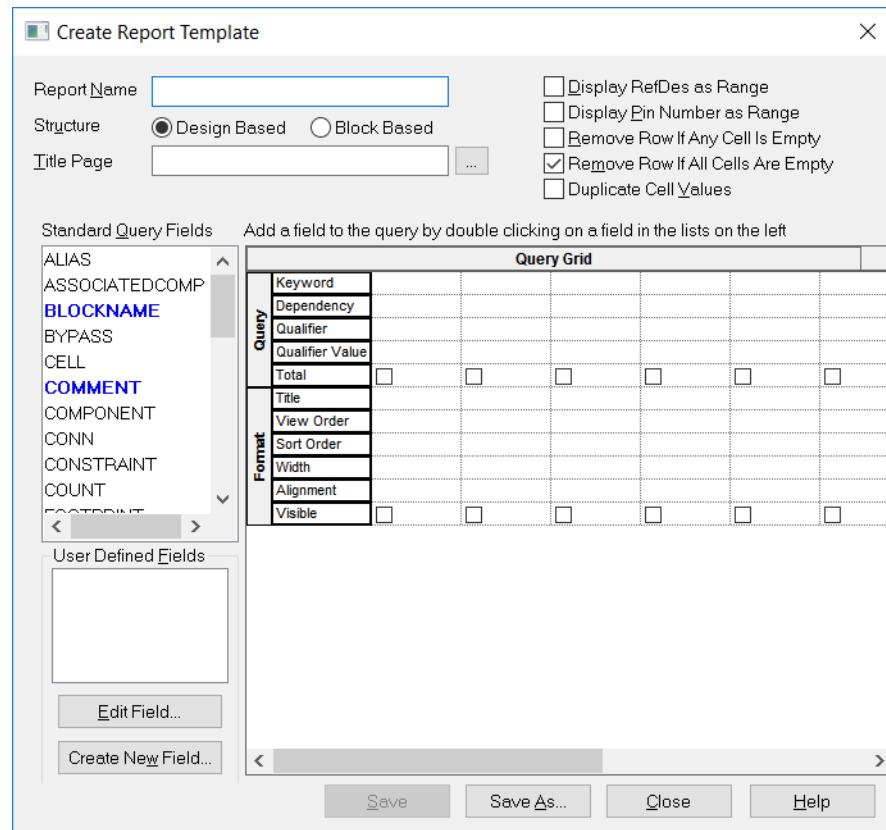
Procedure

1. Choose *Project – Reports – Generate Reports*.
The Generate Report dialog appears.
2. Click the *Create New* button.

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The Create Report Template dialog appears.



3. Type Associated Component Report in the *Report Name* field.
4. Select the *Design Based* option. Reports based on this template will be generated for the entire design.
You can also define a title for your report by selecting a text file that contains the title text for your report.
5. Browse to select the *Title.txt* file located at <your_work_area>/reference/report_start/ in the *Title Page* field.
6. Select the *Remove Row if Any Cell is Empty* check box. This deletes rows with empty cells in the report.
7. Clear the *Duplicate Cell Values* check box to ensure that duplicate values are listed only once in the report.

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Query Grid allows you to set up a template by defining the column headings for the report.

In the query grid, you can add query fields as keywords that can be used to generate data for the report. When you generate the report, the value of the keyword you entered as the title will be displayed as the column heading in the report. The order of keywords in this grid defines how the report will appear.

You can specify keywords in the *Keyword* row by:

- Selecting a cell and choosing a keyword from the drop-down list.
- Selecting and dragging a keyword to a cell from the *Query Fields* list.
- Typing the initials of the keyword in a cell.

8. Specify the keywords in the *Keyword* row as follows:

| Keyword | Cell Number | Tasks/Remarks |
|---------|-------------|--|
| REFDES | 1 | Change the title of this column to Component Reference Designator in the <i>Title</i> cell. |
| PINNUM | 2 | Notice that the <i>Dependency</i> field for the PINNUM column is automatically set as REFDES and the <i>Title</i> field is set as Pin Number. |
| | | When you add a keyword in the query grid, another keyword that you already added in the <i>Query Grid</i> grid is automatically set as the dependency for the keyword. If there are multiple keywords already set, SCM uses a pre-defined fixed order to calculate which keyword should be set as dependency. You can select another keyword as the dependency for PINNUM. |

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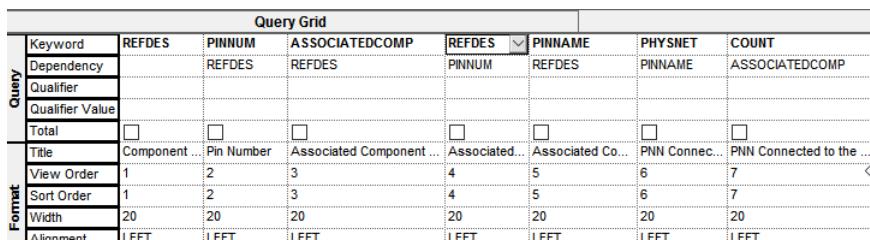
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| Keyword | Cell Number | Tasks/Remarks |
|-----------------|--------------------|--|
| ASSOCIATED COMP | 3 | Change the title of this column to Associated Component Type in the <i>Title</i> cell. |
| REFDES | 4 | Change the title of this column to Associated Component Reference Designator in the <i>Title</i> cell. |
| PINNAME | 5 | Change the title of this column to Associated Component Pin Name in the <i>Title</i> cell. |
| PHYSNET | 6 | Change the title of this column to PNN Connected to the Associated Component Pin in the <i>Title</i> cell. |

9. Specify COUNT in the seventh cell of the *Keyword* row and change the dependency to ASSOCIATEDCOMP.

10. Set the title to PNN Connected to the Associated Component Count in the *Title* cell for the COUNT column.

After adding all the keywords, the *Query Grid* is displayed as shown in the following figure:



The screenshot shows the 'Query Grid' interface with the following configuration:

- Query:** ASSOCCOMPREPORT.TPT
- Format:** Report
- Fields:**
 - Keyword: ASSOCIATEDCOMP
 - REFDES: REFDES
 - PINNUM: REFDES
 - ASSOCIATEDCOMP: ASSOCIATEDCOMP
 - REFDES: PINNUM
 - PINNAME: REFDES
 - PHYSNET: PINNAME
 - COUNT: ASSOCIATEDCOMP
- View Order:** 1, 2, 3, 4, 5, 6, 7
- Sort Order:** 1, 2, 3, 4, 5, 6, 7
- Width:** 20, 20, 20, 20, 20, 20, 20
- Alignment:** LEFT, LEFT, LEFT, LEFT, LEFT, LEFT, LEFT

11. Click the *Save As* button to save the report with a different name.

12. Enter AssocCompReport.tpt in the *File Name* field and click *Save*.

13. Click *Close*.

Notice that the Associated Component Report is selected in the *Report Template* box.

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If a report template is created but not listed in the *Report Template* box, use the *Existing* button to include the template file in the available report templates list.

14. Select the *DSR (Editable Report File)* option to specify the report format.
15. In the *Location* field, specify the output folder where you want the report to be created.
16. Click the *Generate* button.

The Associated Component Report is generated.

Notice that the name of the report is `processor_Associated Component Report.dsr` with following two-line text entry at top of the report:

XYZ Firm - ABC Department

```
# This is the header file that will be used as  
Title page in reports.
```

The report has seven columns. If you have components associated with other components, all seven columns show the value for those components. Otherwise, the component reference designator and pin numbers are listed.

| XYZ Firm - ABC Department | | | | | | |
|--------------------------------|------------|---------------------------|---|-------------------------------|---|---|
| Component Reference Designator | Pin Number | Associated Component Type | Associated Component Reference Designator | Associated Component Pin Name | Pin Connected to the Associated Component Pin | Pin Connected to the Associated Component Count |
| 1 | C1 | 1 | | C1 | a | VCC |
| 2 | | | | | b | GND |
| 3 | | | | C1 | a | VCC |
| 4 | | | | | b | GND |
| 5 | C2 | 1 | | C2 | a | VCC |
| 6 | | | | | b | GND |
| 7 | | | | C2 | a | VCC |
| 8 | | | | | b | GND |
| 9 | C3 | 1 | | C3 | a | VCC |
| 10 | | | | | b | GND |
| 11 | | | | C3 | a | VCC |
| 12 | | | | | b | GND |
| 13 | C4 | 1 | | C4 | a | VCC |
| 14 | | | | | b | GND |
| 15 | | | | C4 | a | VCC |
| 16 | | | | | b | GND |
| 17 | R1 | 1 | Pullup | R1 | a | GND |
| 18 | | | | | b | RC50 |
| 19 | | 2 | | R1 | a | GND |
| 20 | | | | | b | RC50 |
| 21 | R2 | 1 | Pullup | R2 | a | GND |
| 22 | | | | | b | RWE |
| 23 | | 2 | | R2 | a | GND |
| 24 | | | | | b | RWE |
| 25 | R3 | 1 | Pullup | R3 | a | RC50 |
| 26 | | | | | b | VCC |
| 27 | | 2 | | R3 | a | RC50 |
| 28 | | | | | b | VCC |
| 29 | R4 | 1 | Pullup | R4 | a | RWE |
| 30 | | | | | b | VCC |
| 31 | | 2 | | R4 | a | RWE |
| 32 | | | | | b | VCC |
| 33 | U1 | 1 | Bypass | U1 | a<0> | RA<0> |
| 34 | | | | | a<1> | RA<1> |
| 35 | | | | | a<2> | RA<2> |
| 36 | | | | | a<3> | RA<3> |
| 37 | | | | | a<5> | RA<5> |
| 38 | | | | | a<7> | RA<7> |

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Notice that duplicate component reference designators are listed only once. If you want the component reference designator to be repeated for each pin number, select the *Duplicate Cell Values* check box in the Create Report Template dialog and generate the report again.

Summary

In this lesson, you learned to create report templates and use them to generate reports for your design.

For More Information

See:

[Creating Reports](#) chapter of *System Connectivity Manager User Guide*.

Lesson 8-3: Customizing Existing Reports

Overview

In this lesson, you will learn to customize an existing report template and use it to generate reports. You may have standard report templates available for your firm, and may want to customize one of these report templates to quickly generate a report you need.

Concept

System Connectivity Manager uses report template (.tpt) files to create reports. You can open an existing report template and change its parameters or use it to create new report template.

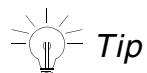
Procedure

Customizing Report Templates

1. Choose *Project – Reports – Generate Reports*.
2. Select *Bill of Materials* in the *Report Template* field.
3. Click the *Customize* button.

The Create Report template dialog box appears. Notice that the *Total* check box in the *Count* column is not selected. This is the reason why the BOM report generated in the [Generating a Simple Report](#) on page 257 is not very effective as the total number of components is not displayed. Let's modify the BOM template to show the count of components.

4. Select the *Total* check box for the *Count* column.
5. Type *BOM with Component Count* in the *Report Name* field.
6. Click *Save As* and save the report with the name *BOM_count.tpt*.



Tip

If you want to create a report template and want it to be available for use across your organization, you can save it in the location *<your_inst_dir>/share/cdssetup/tdd/custom_report_templates*.

7. Click *Close* to close the Create Report template dialog box.
8. Select the *BOM with Component Count* report in the *Report Template* box.
9. Click the *Generate* button to generate the report.

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The report is generated. Notice that the total component count is now displayed.

| | Physical Component | Ref Des | Quantity | Unit Cost | Total Cost |
|----|--------------------|------------------------------------|----------|-----------|------------|
| 1 | 1N4148-BASE | SCH_CR1-SCH_CR5 | 5 | .23 | 5.75 |
| 2 | 2N2222-BASE | SCH_Q2 | 1 | .43 | 0.43 |
| 3 | 2N4339-BASE | SCH_Q1 | 1 | .49 | 0.49 |
| 4 | ACT574_SOIC-BASE | U6-U8, U30-U32 | 6 | 0.65 | 23.4 |
| 5 | CAP-.05UF | SCH_C1-SCH_C7 | 7 | .18 | 8.82 |
| 6 | CAP-0.1UF | C1, C2 | 2 | .25 | 1 |
| 7 | CAP-47UF | C3, C4 | 2 | .22 | 0.88 |
| 8 | CCADC-BASE | SCH_U16 | 1 | 12.77 | 12.77 |
| 9 | CONN2-BASE | SCH_J8 | 1 | 1.98 | 1.98 |
| 10 | DAC0800-BASE | SCH_U4 | 1 | 14.55 | 14.55 |
| 11 | EPF8282A_PLCC-BA | U5 | 1 | 1.05 | 1.05 |
| 12 | GA1110-50-BASE | U1_V | 1 | 26.44 | 26.44 |
| 13 | LM102-BASE | SCH_U11 | 1 | .89 | 0.89 |
| 14 | LM3900-BASE | SCH_U8 | 1 | 1.10 | 1.1 |
| 15 | MUX-BASE | SCH_U10 | 1 | 4.25 | 4.25 |
| 16 | RESD-1K | SCH_R6, SCH_R8, SCH_R19 | 3 | .29 | 2.61 |
| 17 | RESD-1M | SCH_R1, SCH_R11, SCH_R13 | 3 | .75 | 6.75 |
| 18 | RESD-5.1M | SCH_R5, SCH_R7, SCH_R9, SCH_R10 | 4 | .62 | 9.92 |
| 19 | RESD-5K | SCH_R14, SCH_R15 | 2 | .11 | 0.44 |
| 20 | RESD-10K | R1-R4, SCH_R2, SCH_R4 SCH_R12 | 7 | .35 | 17.15 |

Customizing Report Templates to Show Specific Values

You can customize an existing report to display components or properties of specific values. In the following example, you will select the Concise_net_list.tpt template and customize it to display netlist for components with RefDes U1*.

1. Choose *Project – Reports – Generate Reports*.
2. Select *Concise Net List Report* in the *Report Template* field.
3. Click the *Customize* button.

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4. Type *Concise Net List Report for Components with RefDes Beginning with Letter U* in the *Report Name* field.
5. Select *Value* in the *Qualifier* cell of the *RefDes* column.
6. Enter *U1** as the value in the *Qualifier Value* field of the *RefDes* column.
7. Click *Save As* and save the template with name *Net_list_U_star.tpt*.
8. Click *Close* to close the Create Report template dialog box.
9. Select the Concise Net List for *U1** report in the *Report Template* box.
10. Click the *Generate* button to generate the report.

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The report is generated.

| Physical Net Name | Ref Des | Pin Number | Physical Component |
|-------------------|---------|------------|---------------------|
| N12V | | 6 | |
| N12V | | 7 | |
| NCS | | 11 | |
| OE | | 32 | |
| Q0_V | U1_V | 17 | GA1110-50-BASE |
| Q1_V | U1_V | 20 | GA1110-50-BASE |
| Q2_V | U1_V | 21 | GA1110-50-BASE |
| Q3_V | U1_V | 22 | GA1110-50-BASE |
| Q4_V | U1_V | 3 | GA1110-50-BASE |
| Q5_V | U1_V | 24 | GA1110-50-BASE |
| RA<0> | U1 | 5 | TC55B4257_SOIC-BASE |
| RA<0> | | 5 | |
| RA<0> | | 5 | |
| RA<0> | | 76 | |
| RA<1> | U1 | 4 | TC55B4257_SOIC-BASE |
| RA<1> | | 4 | |
| RA<1> | | 4 | |
| RA<1> | | 4 | |
| RA<1> | | 5 | |
| RA<1> | | 71 | |
| RA<2> | U1 | 3 | TC55B4257_SOIC-BASE |
| RA<2> | | 3 | |
| RA<2> | | 3 | |
| RA<2> | | 3 | |
| RA<2> | | 70 | |
| RA<3> | U1 | 2 | TC55B4257_SOIC-BASE |

Notice that the report lists the physical net names and pin numbers for the components with RefDes beginning with letters U1. If you scroll down the list, you will find over 200 components have reference designators starting with the letter U1.

Summary

In this lesson, you learned to customize an existing report template and use it to generate reports.

For More Information

See:

[Creating Reports](#) chapter of *System Connectivity Manager User Guide*.

Lesson 8-4: Generating Block-Based Reports

Overview

In this lesson, you will learn to generate reports for different blocks. These reports are sorted by blocks in a design.

Concept

System Connectivity Manager creates two types of reports—block-based report and design-based report. You have learned creating design-based reports, which report on components across the entire design. In this lesson, you will learn to create a template for block-based report and use it to generate reports sorted on basis of all blocks in the design.

Procedure

Creating the Template for Block-based Report

1. Choose *Project – Reports – Create Template*.
The Create Report Template dialog box appears.
2. Type *Block Based Net Report* to define the *Report Name*.
3. Select the *Block Based* option button to define that the report template should sort the report by blocks in the design.
4. Select the *Remove Row if Any Cell is Empty* check box to delete those rows in the report that have any cell as empty.
5. Clear the *Duplicate Cell Values* check box to ensure that duplicate values are not separately listed in the report.

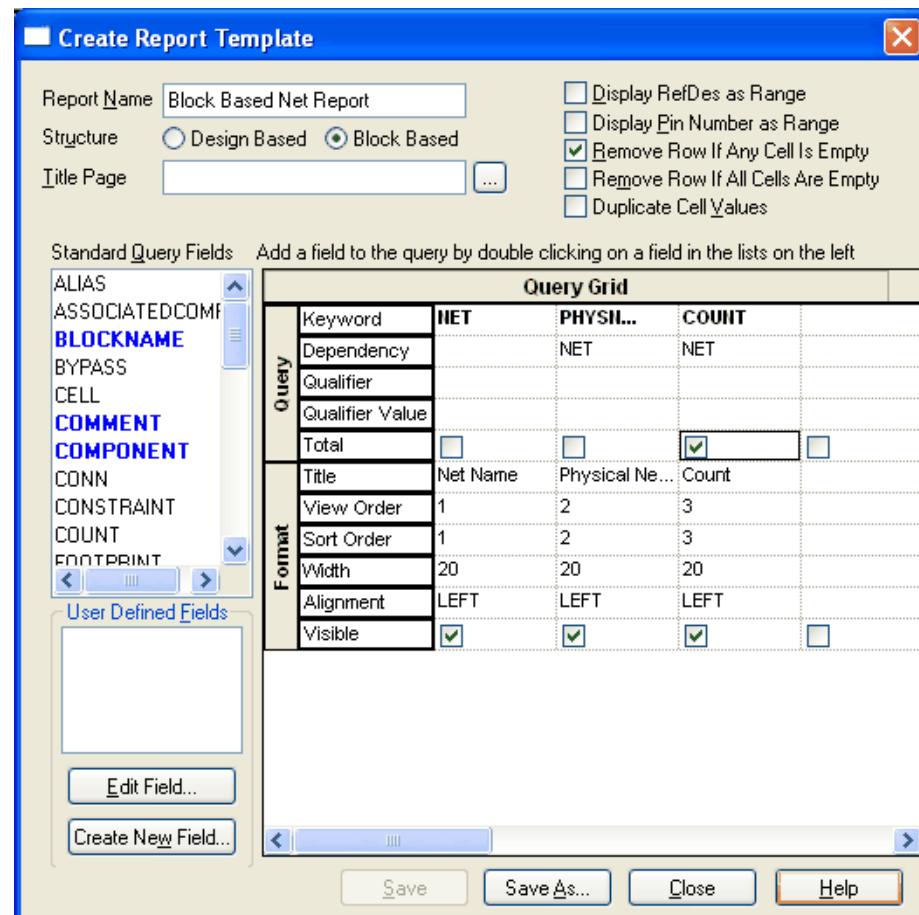
You can now define the query grid.

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6. Select first keyword as Net.
7. Notice that Net Name appears by default in the *Title* cell for the Net column.
8. Select second keyword as PHYSNET and specify its title as Physical Net Name.
Notice that the dependency of the PHYSNET column is set as NET.
9. Select third keyword as Count and select its *Total* field.

The Create Report template Dialog box should look like the figure shown below:



10. Click the Save As button.

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11. Select the `report_start/temp` directory and save the file with the name `BlockBasedNetReport.tpt`.
12. Click *Close* to close the Create Report template dialog box.

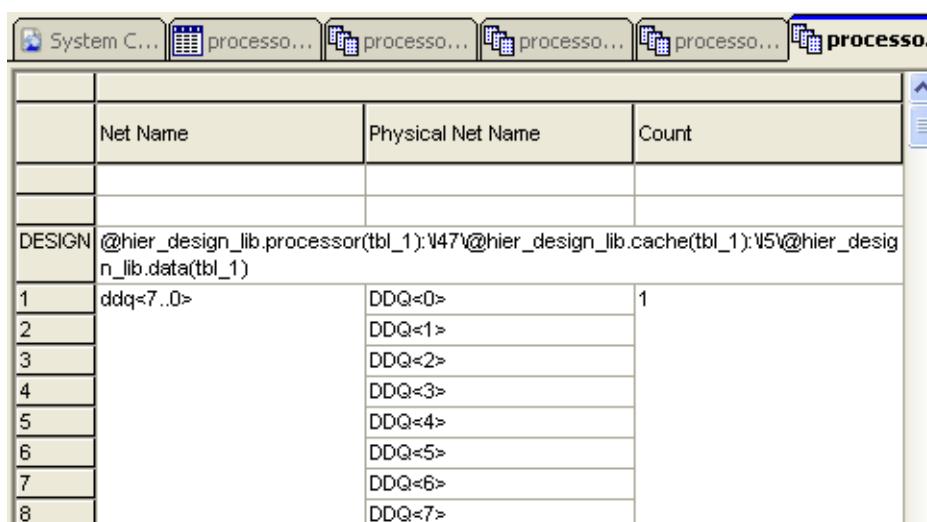
Generating the Report

1. Choose *Project – Reports – Generate Reports*.

You need to select the custom report you created. All reports created in the root directory automatically appear in the *Report Template* list. To get another report template not appearing in the default path, use the *Add Existing* button.

2. Click the *Add Existing* button.
 3. Open the `BlockBasedNetReport.tpt` report template from the `hier_design/temp` directory.
- Notice that the `Block Based Net Report` is selected in the *Report Template* box.
4. Select the *DSR(Editable Report File)* option button to specify the report format.
 5. Click the *Generate* button to generate the report.

The report lists nets available at different design levels, along with their physical net names and connection count of each net.



A screenshot of the System Connectivity Manager interface showing a report table. The table has columns for Net Name, Physical Net Name, and Count. The data is categorized by design level (DESIGN) and includes specific net names like ddq<7..0> and their corresponding physical net names and connection counts.

| | Net Name | Physical Net Name | Count |
|--------|---|-------------------|-------|
| | | | |
| | | | |
| DESIGN | @hier_design_lib.processor(tbl_1):\V47\V@hier_design_lib.cache(tbl_1):\V5\V@hier_design_lib.data(tbl_1) | | |
| 1 | ddq<7..0> | DDQ<0> | 1 |
| 2 | | DDQ<1> | |
| 3 | | DDQ<2> | |
| 4 | | DDQ<3> | |
| 5 | | DDQ<4> | |
| 6 | | DDQ<5> | |
| 7 | | DDQ<6> | |
| 8 | | DDQ<7> | |

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Module 8: Generating Reports

As you scroll down the list, you will see BOM information for different design blocks.

Editing the .dsr Report

You can edit the displayed report in multiple ways. In next few steps, you will learn few of these methods.

1. To change the order of columns, select a column and drag it to the place you wish. For example, try this.

- a. Click the *Net Name* column header to select it.

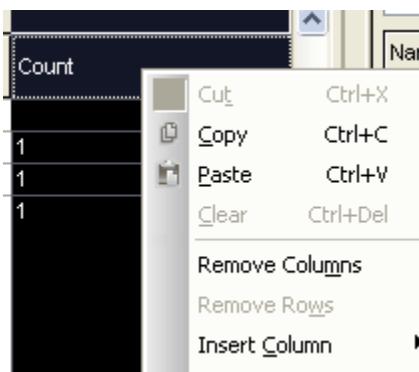
Keeping the left mouse button pressed, drag the column to the left. As you drag the column, notice that a rectangle appears indicating a drag operation. As you pass a column separator, a red line appears indicating the current position. Drop the *Net Name* column after the *Physical Net Name* column.

| | Net Name | Physical Net Name | Count |
|--------|-----------|-------------------|-----------|
| DESIGN | processor | | processor |
| 5 | 12v | 12V | 1 |
| 6 | agnd | AGND | 1 |
| 7 | ba<7..0> | BA<0> | 1 |

Note: You can drag and drop multiple rows or columns to change their display order.

2. To delete a column, for example the *Count* column:

- a. Select the *Count* column header and right-click to display the short-cut menu.
- b. Select the *Remove Columns* command.



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3. To quickly select a component, for example the component with the Ref Des U30:

- Select the signal with the net name dq<7..0> and the physical net name DQ<7>_1.
- Select *Edit – Highlight*.

The component with Ref Des U30 is highlighted in the design.

dq<7..0> DQ_1

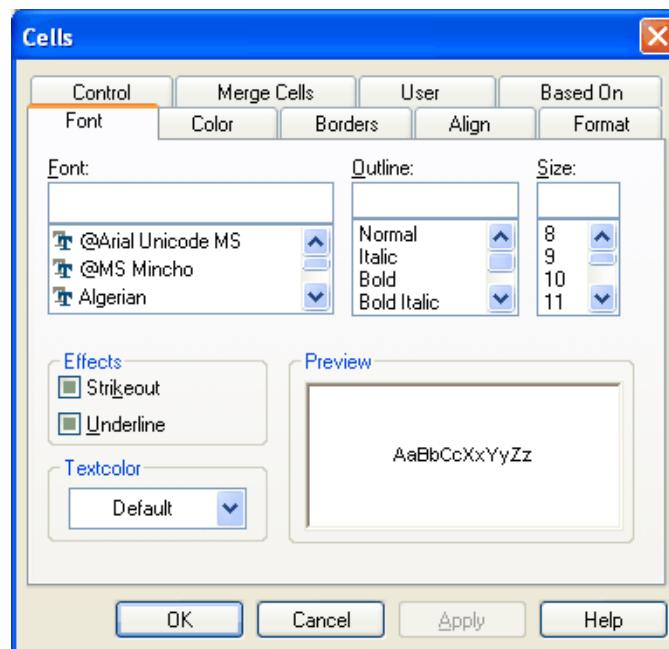
4. To quickly change the font and alignment; for example, to center align a row and apply bold style, select the cells that require alignment change, and choose:

- Format – Align – Center*.
- Format – Style – Bold*.

5. To change cell level format:

- Select the cell and choose *Format – Cells*.

The Cells dialog box appears.



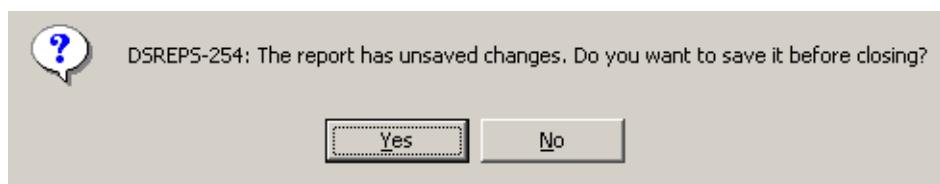
- To change a font, select a new font, outline or cell.

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- c. To change colors, select the *Color* tabbed page and select foreground or background color, shade and if required a 3-D effect. You can preview the selection before you apply it.
- d. Click *Ok* to accept the changes.
6. Close the report by selecting *File – Close*.

You may get the message that report has unsaved changes and whether you would wish to save those changes.



7. Click *Yes* to save the changes.

Summary

In this lesson, you learned to generate reports that are sorted with blocks. You also learned how to edit a .dsr report.

For More Information

See:

[Creating Reports](#) chapter of *System Connectivity Manager User Guide*.

Lesson 8-5: Creating Cross-Tab Reports

Overview

In this lesson, you will generate a cross tab report. A cross tab report can provide information such as details of which pin names of a given component instance is connected to which signal.

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Module 8: Generating Reports

Concept

You can enter the name of another keyword you have added in the query grid as the title for a keyword to generate a cross-tab report. The title should be entered as %keyword_name% where keyword_name is the name of another keyword in the query grid.

When you generate the report, the value of the keyword you entered as the title will be displayed as the column heading in the report. For example, if you enter %keyword_name% as the title for the keyword PINNUM, the reference designators of components in the design are displayed as column headings in the report and the pin numbers of a given reference designator appear in the column for the reference designator.

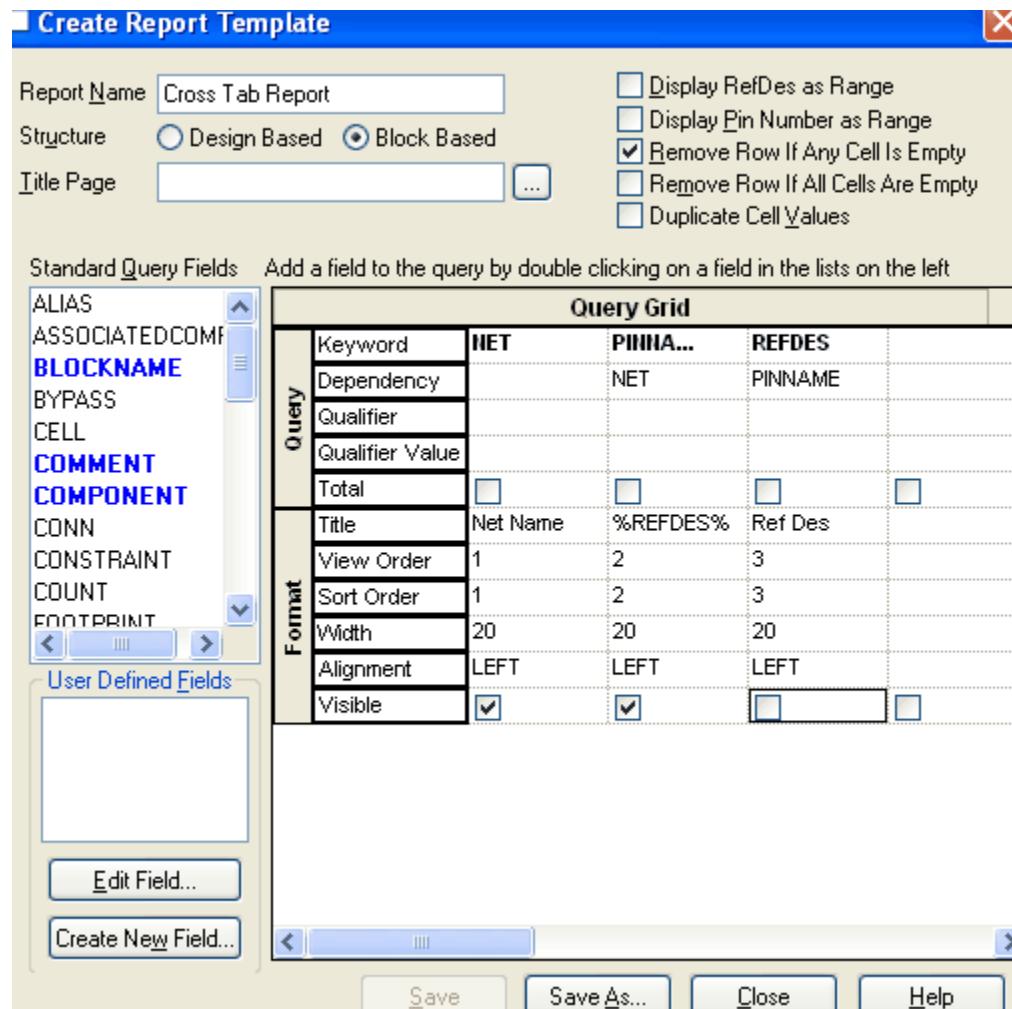
Procedure

1. Choose *Project – Reports – Create Template*.
2. Type Cross Tab Report to define the *Report Name*.
3. Select the *Block Based* option button to define that the report template should sort the report by blocks in the design.
4. Select the *Remove Row if Any Cell is Empty* check box to delete those rows in the report that have any cell as empty.
5. Clear the *Duplicate Cell Values* check box to ensure that duplicate values are not separately listed in the report.
6. Select first keyword as Net.
7. Type Net Name in the *Title* cell for the Net column.
8. Select second keyword as PINNAME.
Notice that the dependency for the PINNAME is automatically set as NET.
9. Select third keyword as REFDES.
10. Specify the title of the PINNAME column as %REFDES%.
11. Clear the *Visible* check box of the REFDES column.

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The Create Report Template Dialog box should look like the figure shown below:



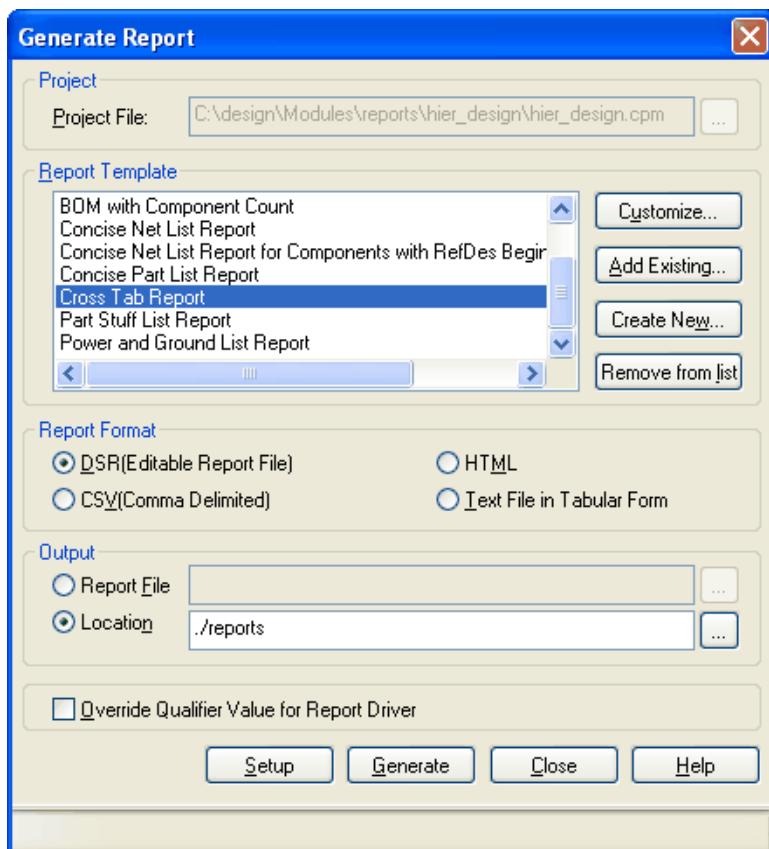
12. Click the *Save As* button and save the report with the name *CrossTabReport.tpt*.
13. Click the *Close* button to close the Create Template dialog box.

You have created the template file for generating a cross-tab report. You can now use this template to generate the cross-tab report.
14. Choose *Project – Reports – Generate Reports*.
15. Select the *Cross Tab Report* in the *Report Template* box.
16. Select the *DSR(Editable Report File)* option button to specify the report format.

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The Generate Report dialog box should have the following settings:



17. Click the *Generate* button to generate the report.

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Notice that the report lists all net names along with the pin names of components where they are connected. You can scroll down (and/or right) the report to see the details.

| | Net Name | SCH_C1 | SCH_C2 | SCH_C3 | SCH_C4 | SCH_C5 | SCH_C6 | SCH_C7 | SCH_1 |
|--------|---|--------|--------|--------|--------|--------|--------|--------|-------|
| 6 | | | | | | | | | |
| DESIGN | | | | | | | | | |
| DESIGN | @hier_design_lib.processor(tbl_1):V49v@hier_design_lib.analog_io(sch_1) | | | | | | | | |
| 7 | 12v | | | | | | | | |
| 8 | afd | | | | | | | | |
| 9 | afs | | | | | | | | |
| 10 | agnd | | | b | | b | | b | |
| 11 | | | | | | | | | |
| 12 | | | | | | | | | |
| 13 | audout | | | | | | | | |
| 14 | cclock | | | | | | | | |
| 15 | data<3..0> | | | | | | | | |
| 16 | micin | | a | | | | | | |
| 17 | mtorff | a | | | | | | | |
| 18 | n12v | | | b | | a | | | |
| 19 | rftum | | | | | | | | |

You can adjust the columns by dragging their borders for better display.

18. Close the report by selecting *File – Close*.
19. Click *No* to ignore the changes.

Summary

In this lesson, you learned to generate a cross tab report.

For More Information

See:

[Creating Reports](#) chapter of *System Connectivity Manager User Guide*.

Lesson 8-6: Creating Custom Columns in Reports

Overview

In this lesson, you will learn to create or edit user defined query fields that can be used in report templates.

Concept

A custom column is a user defined query field that can be used in report templates. For example, you can create columns with sub-columns.

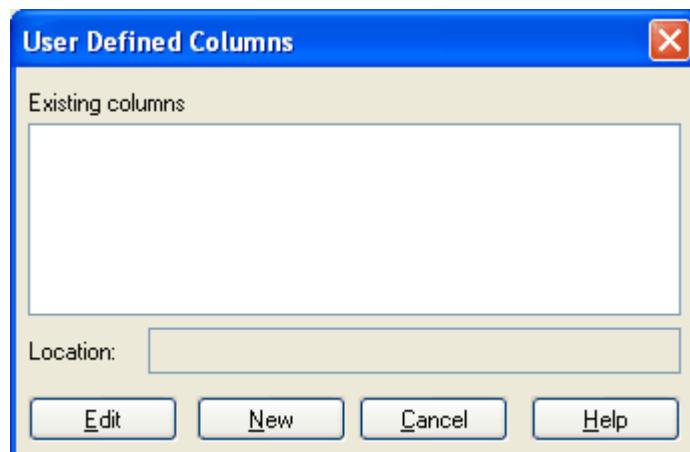
In this lesson, you will learn to create a column COMPONENT INFORMATION, which has two sub-columns—PIN NAME and REFDES.

Procedure

Creating a Custom Column

1. Choose *Project – Reports – Create Custom Column*.

The User Defined Columns dialog box appears.

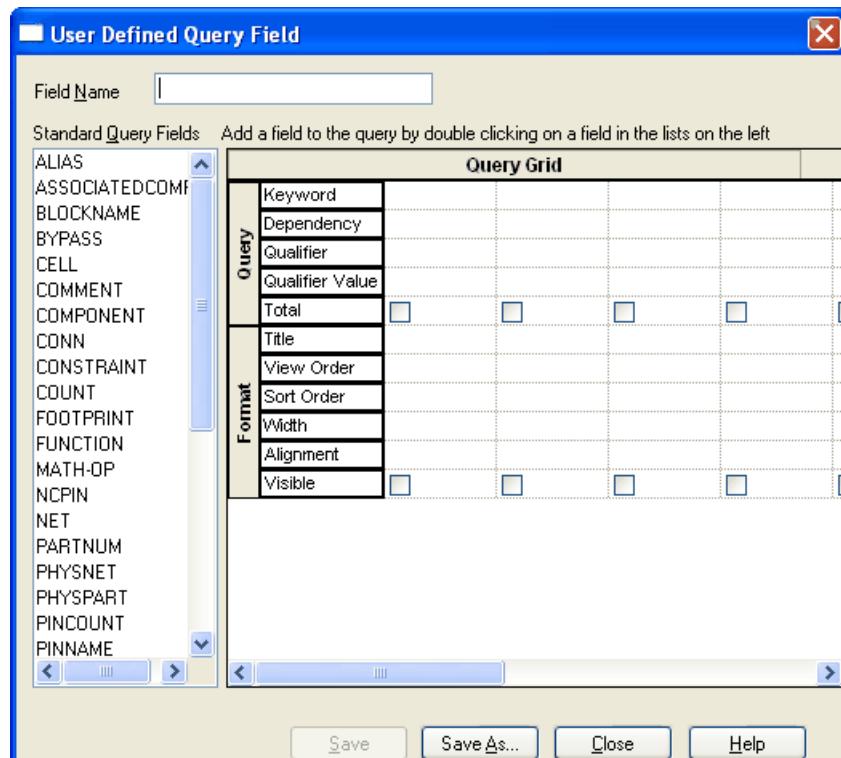


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Module 8: Generating Reports

2. Click *New*.

The User Defined Query Field dialog box appears.



Notice that the User Defined Query Field dialog box has a query grid similar to the query grid used in the Create Report Template dialog box

3. Type `COMPONENT_INFORMATION` as the field name.
4. Select the first keyword as `PINNAME`. To select the keyword, click in the first cell next to the *Keyword* cell and choose `PINNAME` from the list box.
5. Set the *Dependency* field for the `PINNAME` column to `PHYSNET`.
This dependency will display the names of pins connected to the nets in the design in the report
6. Select the second keyword as `REFDES`.

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Notice that the dependency is automatically set to `PINNAME` signifying that the report will display the reference designator of the components whose pins are connected to nets in the design.

7. Click the *Save As* button and save the report with the name `ComponentInfo.txt`.
8. Click the *Close* button to close the User Defined Query Field dialog box.
9. Click the *Cancel* button to stop making any more changes to the user-defined columns.

Associating a Custom Column in a Report Template

You will now add the custom column in a report template and generate a report.

1. Choose *Project – Reports – Create Template*.
2. Type `Connectivity Report` to define the *Report Name*.
3. Select the *Design Based* option button.
4. Select the first keyword as `PHYSNET`.
5. Select the second keyword as `COMPONENT_INFORMATION` by dragging the `COMPONENT_INFORMATION` keyword from the *User Defined Fields* to the cell next to the `PHYSNET` keyword.

Notice that the title `COMPONENT_INFORMATION` appears in the `COMPONENT_INFO` column.

6. Click the *Save As* button and save the report template with the name `Connectivity_report.tpt`.
7. Click the *Close* button.

Generating a Report Containing Custom Columns

1. Choose *Project – Reports – Generate Reports*.
2. Select *Connectivity Report* in the *Report Template* field.
3. Select the *DSR(Editable Report File)* option button to specify the report format.

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4. Specify the output folder where the report will be located in the *Location* field.

5. Click the *Generate* button to generate the report.

Notice that the generated report has a column titled COMPONENT INFORMATION, which has two sub-columns—Pin Name and Ref Des.

| | Physical Net Name | COMPONENT_INFORMATION | |
|----|-------------------|-----------------------|---------|
| | | Pin Name | Ref Des |
| 1 | 12V | a | SCH_R2 |
| 2 | | a | SCH_R4 |
| 3 | | a | SCH_R5 |
| 4 | | a | SCH_R7 |
| 5 | | a | SCH_R9 |
| 6 | | a | SCH_R10 |
| 7 | | a | SCH_R12 |
| 8 | | a | SCH_R15 |
| 9 | | v+ | SCH_U16 |
| 10 | AGND | b | SCH_C3 |
| 11 | | b | SCH_C5 |

Summary

In this lesson, you learned to create custom columns, associate them with a report template and then generate reports.

For More Information

See:

[Creating Reports](#) chapter of *System Connectivity Manager User Guide*.

References

This appendix discusses the following:

- [Learning More About System Connectivity Manager](#)
- [List of Sample Design Files](#)
- [List of Multimedia Demonstrations](#)

Learning More About System Connectivity Manager

Cadence Online Support®

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For additional information, go to:

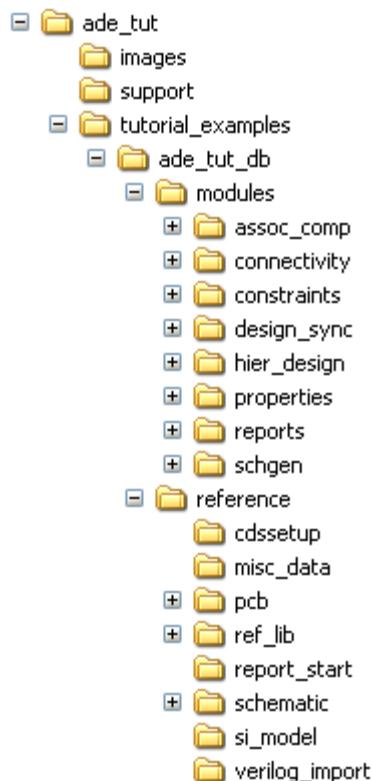
<http://www.cdnusers.org>

List of Sample Design Files

The zipped or tarred copy of the tutorial database is located in the directory:

```
<your_inst_dir>/doc/ade_tut/tutorial_examples/
```

After you have unzipped the `ade_tut_db.zip` file or untarred the `ade_tut_db.t.z` file, you will get the following directory structure.



The `modules` directory contains the design projects for each module in the tutorial. If you have not completed all the lessons in a previous module, you can open the project (`.cpm`) file for the current module and work through the lessons in the module.

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References

The reference directory contains the part and footprint libraries and other files used in the tutorial. The important folders in the reference directory are described below:

| Folder | Description |
|---------------|---|
| pcb | Contains the Allegro PCB footprint libraries. |
| ref_lib | Contains the part libraries and part table file used in designs in System Connectivity Manager. |
| schematic | Contains the schematic used in Lesson 6-2: Adding a Schematic Block in a Design of Module 6: Creating a Hierarchical Design . |
| si_model | Contains the signal integrity model library used in Lesson 5-4: Assigning Signal Integrity Models of Module 5: Working with Constraints . |

List of Multimedia Demonstrations

The following table lists the multimedia demonstration files that are available for System Connectivity Manager. Demonstrations that were created or updated before this release are available on Cadence Online Support.

Note: Not all lessons have accompanying multimedia demonstrations. Some lessons do not require visual demonstrations

| This demo ... | Shows how to ... | Available from.. |
|--|--|-------------------------|
| <u>Pin Swaps in the Back to Front Flow</u> | How to swap differential pairs in Allegro PCB and import the updated board file to System Connectivity Manager (Running Time: 6:00 min) | Cadence Online Support |
| <u>Generating Document Schematic</u> | How to generate a document schematic for a design created in System Connectivity Manager (Running Time: 15:00 min) | Cadence Online Support |

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References

| This demo ... | Shows how to ... | Available from.. |
|---|--|------------------------|
| <u>Creating a Project in System Connectivity Manager</u> | Create projects in System Connectivity Manager. (Running Time: 05:58 min) | Cadence Online Support |
| <u>Working with Components and Connectivity</u> | Add components and signals in the design and capture connectivity information. (Running Time: 30:00 min) | Cadence Online Support |
| <u>Using Matrix Connectivity</u> | Work with the matrix view to manage connectivity. (Running Time: 05:35 min) | Cadence Online Support |
| <u>Working with Associated Components</u> | Work with terminations, bypass capacitors and pullup/pulldowns in the design. (Running Time: 11:00 min) | Cadence Online Support |
| <u>Assigning Signal Integrity Models in System Connectivity Manager</u> | Assign a signal integrity model on a component and automatically generate models for the two pin discrete components (resistors, capacitors and inductors) in the design. (Running Time: 07:00 min) | Cadence Online Support |
| <u>Working with Hierarchical Designs</u> | Work with hierarchical designs in System Connectivity Manager. (Running Time: 48:46 min) | Cadence Online Support |
| <u>Generating Reports Using System Connectivity Manager</u> | Create report templates and generate reports in System Connectivity Manager. (Running Time: 45:00 min) | Cadence Online Support |