

Allegro X System Capture – Schematic Sign Off Tutorial

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Design Integrity Checks

After you have captured a schematic in Allegro X System Capture, you run various design integrity checks to detect common schematic design errors introduced while creating the design. These checks reduce design time, improve design quality, and help you verify and sign off the schematic.

To get the schematic ready for the PCB design phase, in addition to running design checks, you also need to perform tasks, such as adding schematic constraints, creating variants of a design, and generating a Bill of Materials (BOM).

To seamlessly run the design integrity checks, ensure that your system meets the following requirements:

- Allegro X System Capture installation – 23.10
- Minimum 8GB RAM and 500MB of free disk space

These are various design integrity checks to detect common errors introduced while creating the design, given as follows:

- Audit a Schematic
- Analyze Electrical Stress
- Set up Electrical Constraints and create ECSets
- Create a Design variant and modify variant data
- Generate and view a live BOM report

Related Topics

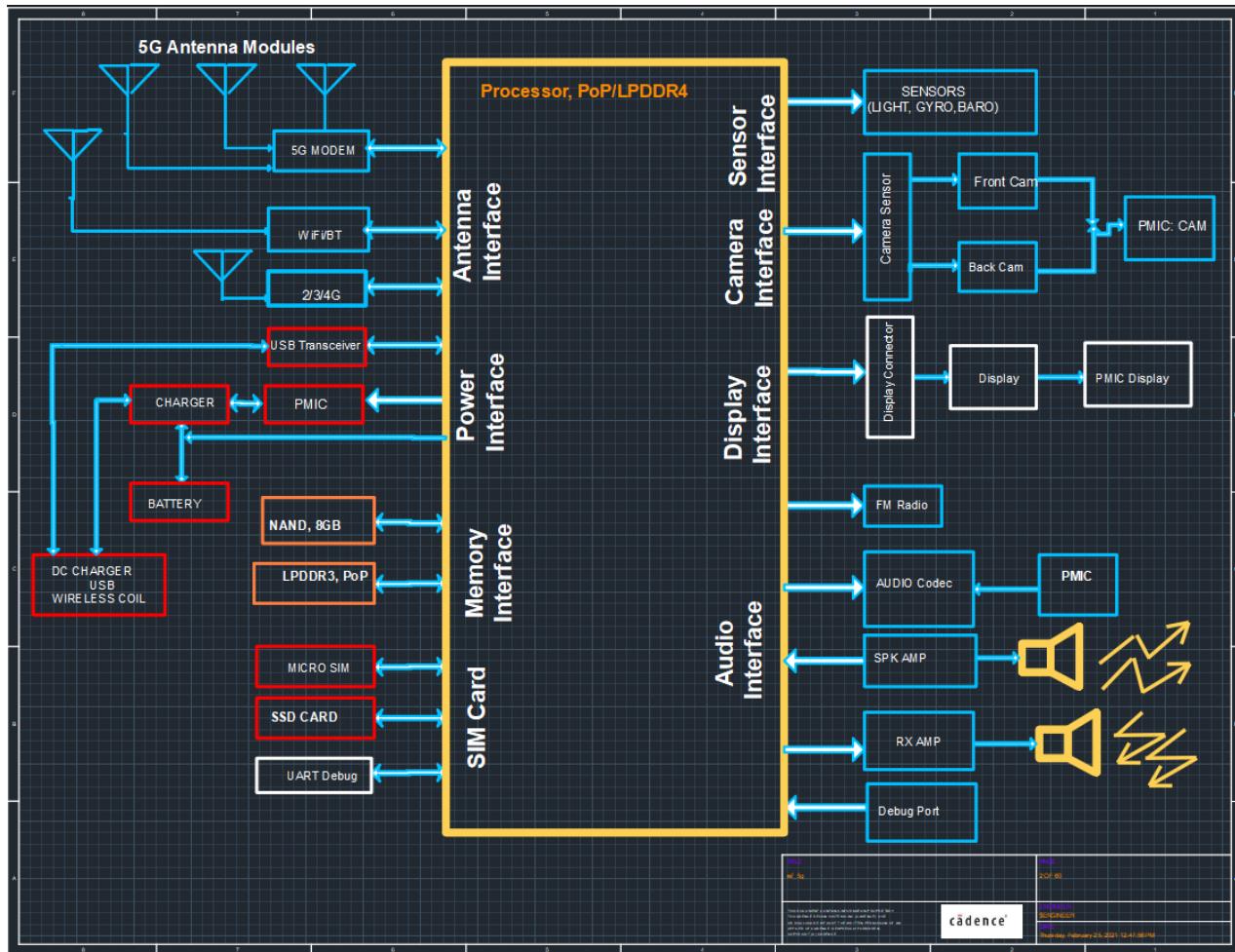
- [Accessing the Sample Design](#)

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Design Integrity Checks

Accessing the Sample Design

The sample design *reference_5G*, represents *Cadence 5G Phone reference PCB design schematic*. This design is used to showcase the various functionalities of System Capture.



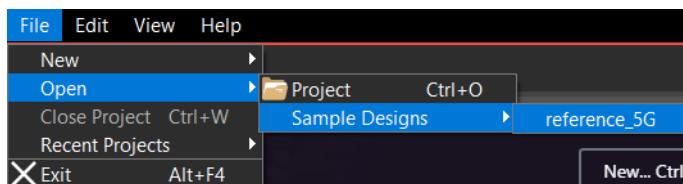
The sample design consists of various functions including Processor, Audio, Camera, Display, WLAN, Memory, 2G/3G/4G RF Blocks, and so on. The three 5G antenna modules illustrated in the previous image are excluded from the sample design.

To access the sample design, *reference_5G*, first launch Allegro X System Capture and follow these steps:

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Design Integrity Checks

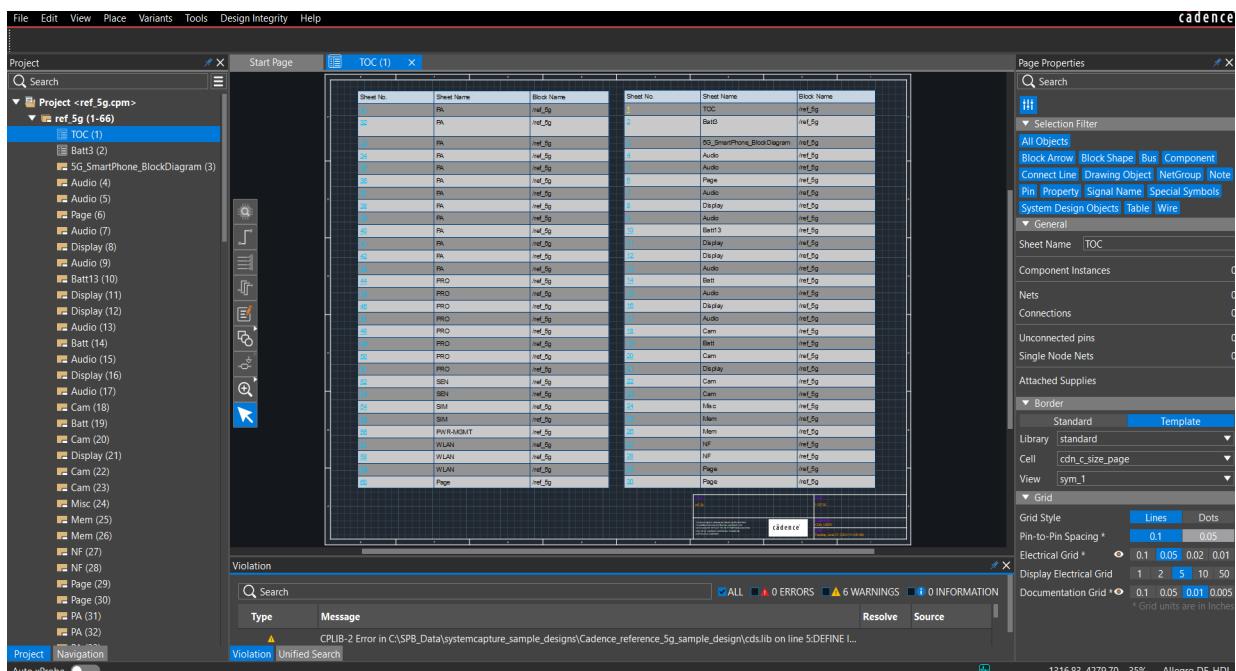
- From the *Start page*, choose *File – Open – Sample Designs – reference_5G*.



The sample design is downloaded to your system and a message is displayed informing about the location of the downloaded design. On subsequent launches, the design is opened from this location.

- Click *OK* to close the message box.

The sample design opens.



By default, the first page of the schematic opens. In this design, *Table of Contents* is added as the first page. The *Project Explorer* panel in the System Capture user interface lists all the pages of the design. Note that the page name is followed by the page number enclosed in parenthesis.

Related Topics

[User Interface of Allegro X System Capture](#)

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Design Integrity Checks

Setting Schematic Sign Off Options

To ensure that the integrity of the final schematic is maintained, System Capture provides you with the option to run sign off checks on the schematic design. In this section of the tutorial, you will use the *Audit Schematic* analysis option to identify and resolve any unintentional errors that may have been introduced while capturing the schematic design.

Another concern during the design phase is inadvertently using components with inaccurate ratings. Identifying such components without running simulations can be an arduous task. Running simulations requires models for components, which at times can be difficult to obtain, might require significant setup or a substantial run time. The *Analyze Electrical Stress* analysis option helps you identify overstressed components in a design without having to assign models or simulate the design. You can use the result dashboard to navigate to the overstressed component(s) and then resolve any underlying issues.

Auditing a Schematic

Auditing a schematic before simulating the design enables you to identify the failures and faults, navigate to them, and fix them in a short time.

To run checks and generate an audit report of the schematic, follow these steps:

1. Choose *Design Integrity – Audit Schematic*.

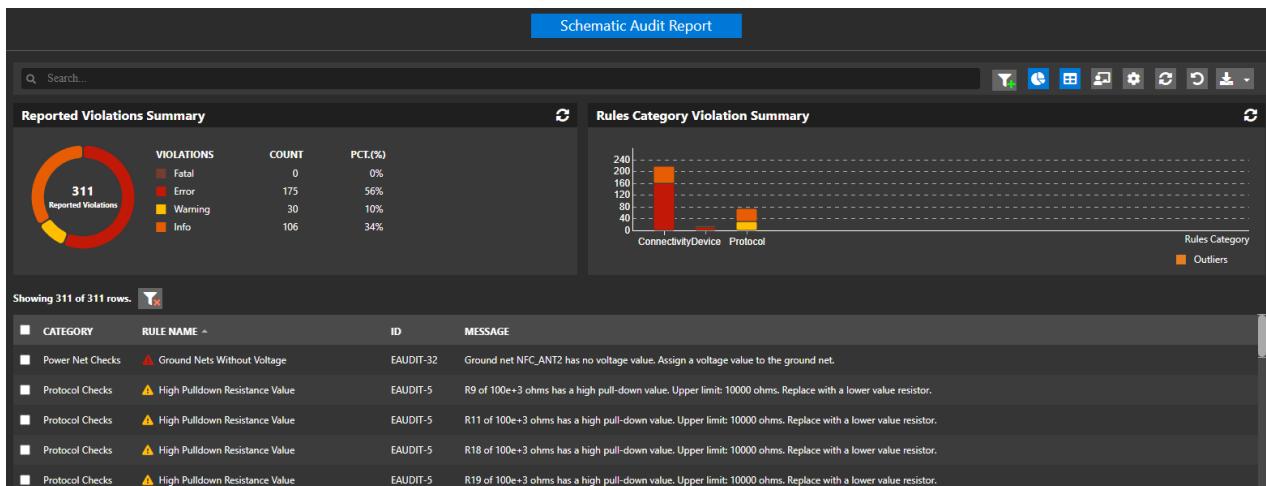
The basic checks run in the background and a detailed *Schematic Audit Report* is generated on completion. The user interface follows a distinct color coding for the four categories of violations, as illustrated in the following image:

- Fatal
- Error
- Warning

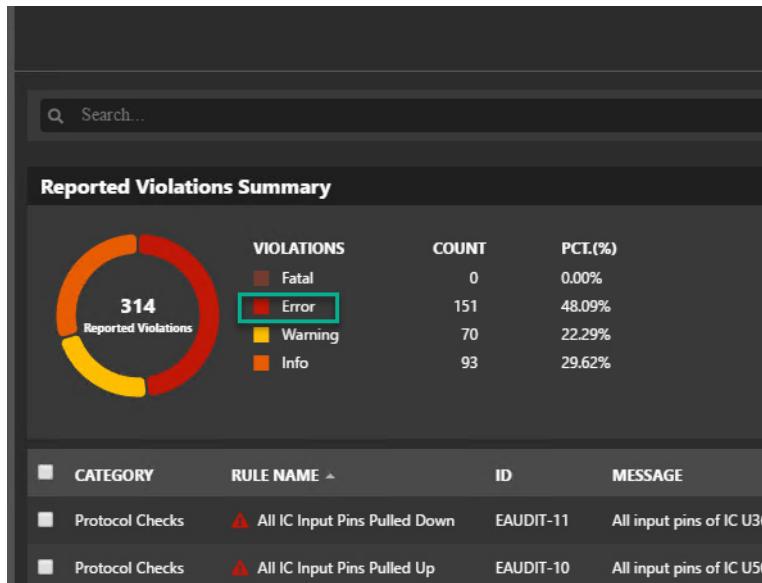
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Setting Schematic Sign Off Options

□ Info



2. To filter out violations in the Error category, click *Error* in the *VIOLATIONS* list of the Reported Violations Summary section.



The detailed violation summary of all the errors is displayed at the top of the message display section. As there are no Fatal category issues in this design, the Error violations appear at the top.

3. Scroll-down to the *Device Checks* category and select the first entry with the ID EAUDIT-22.

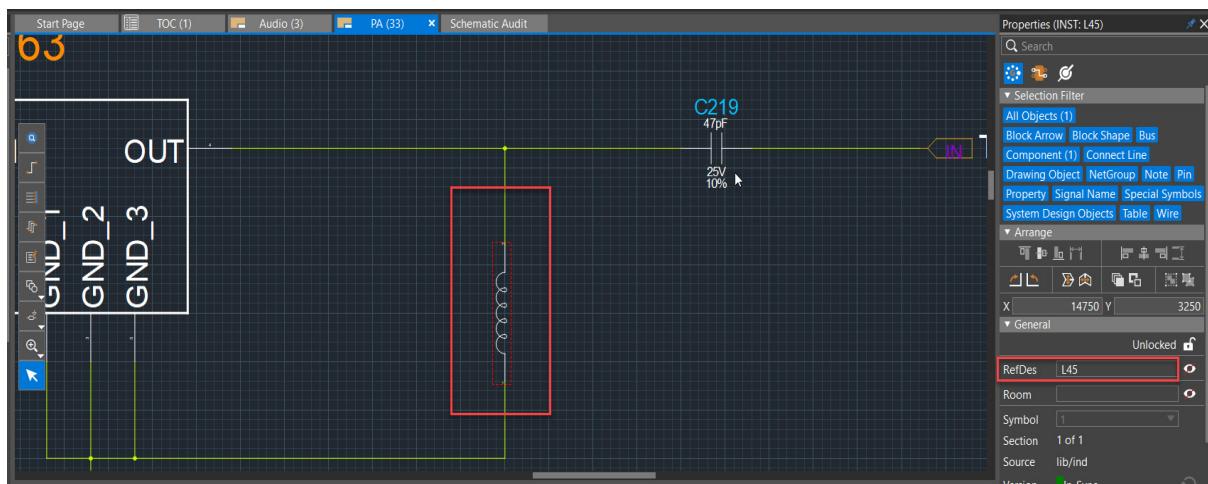
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Setting Schematic Sign Off Options

- Right-click the error message and choose *Highlight* to navigate to the location of the error on the schematic.

Showing 151 of 314 rows. 			
Category	Rule Name	ID	Message
Device Checks	Bypass capacitor voltage exceeds rated voltage	EAUDIT-59	DC voltage on bypass capacitor C275 exceeds its rated voltage. Ensure that the voltage on bypass capacitors is not more than their rated voltage.
Device Checks	Value Unavailable On R/L/C	EAUDIT-22	Inductor L45 has no assigned value. Assign a value to the part.
Device Checks	Value Unavailable On R/L/C	EAUDIT-22	Inductor L67 has no assigned value. Assign a value to the part.
Device Checks	Value Unavailable On R/L/C	EAUDIT-22	Inductor L68 has no assigned value. Assign a value to the part.

The page with the faulty component is opened in a new tab. As indicated in the first error message, Inductor *L45* on page *PA(33)* is highlighted in the following image:



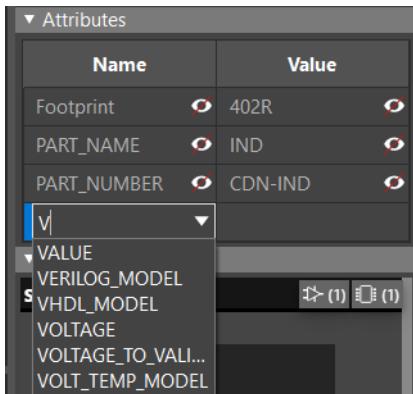
The violation message indicates a missing value on this Inductor. Let's manually specify this missing value.

- Click *<Add Property>* in the *Attributes* section of the *Properties* panel.

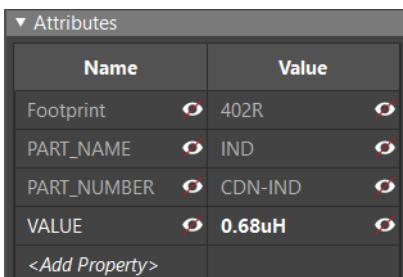
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Setting Schematic Sign Off Options

- Type *VALUE* or select *VALUE* from the drop-down list.



- In the corresponding *Value* column, specify *0.6uH* and press Tab.

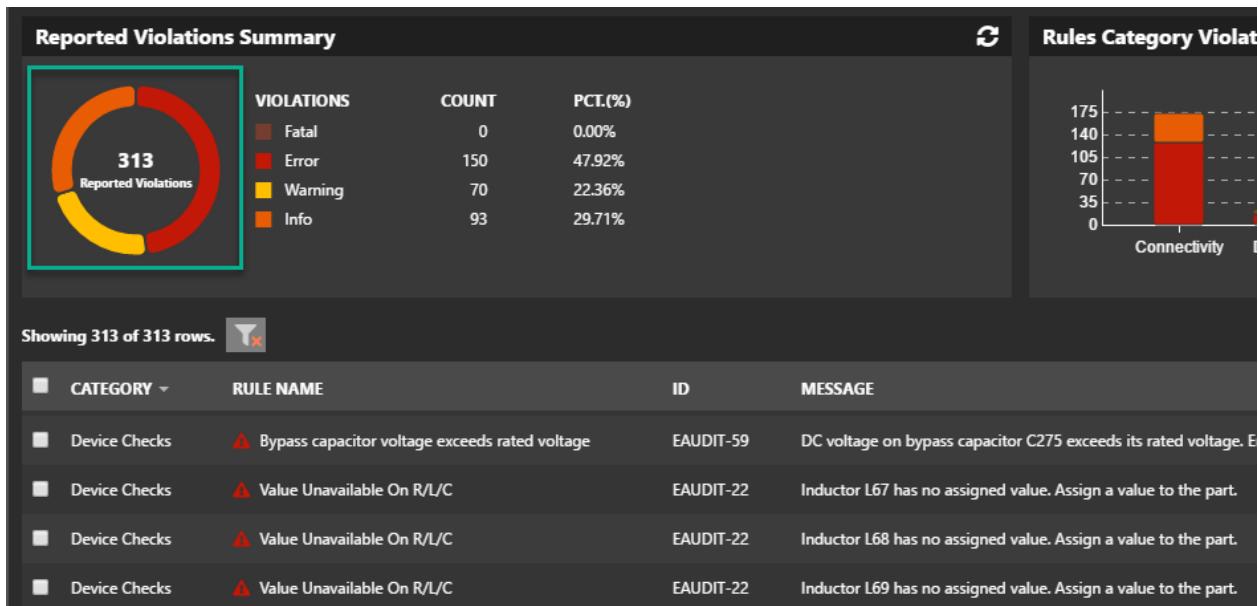


- Choose *File – Save All* or press the *Ctrl + S* key combination to save the design.
- Choose *Design Integrity – Audit Schematic* to run the audit checks once again.

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Setting Schematic Sign Off Options

The generated Schematic Audit report no longer shows the error corresponding to Inductor L45. Also notice that the number of reported violations has gone down by 1.



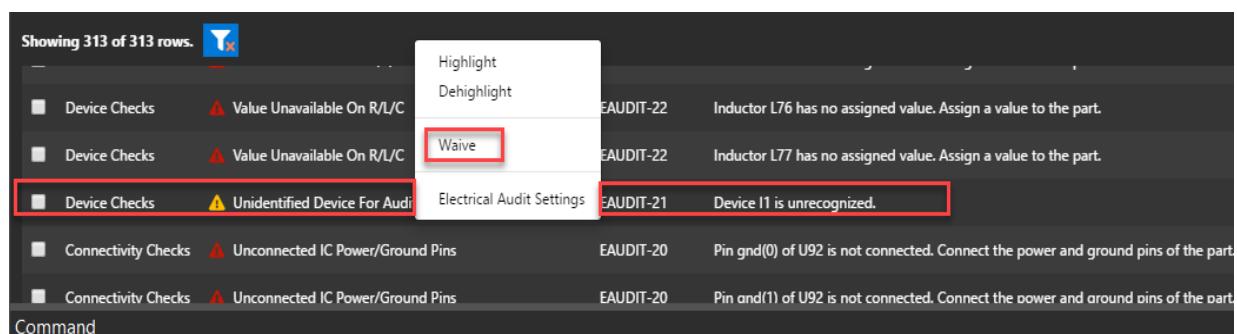
Similarly, you can view and resolve all the reported schematic errors.

Waiving off Rules

Schematic Audit Report displays all the design issues in the dashboard. However, if a check is not relevant for a device, you can waive it from the dashboard. Waived rules are not included in the subsequent runs of schematic audit checks.

To waive the check to report unknown devices, follow these steps:

1. Scroll down to the violation with the ID EAUDIT-21 in the *Device Checks* category.
2. Right-click the row and choose *Waive*.

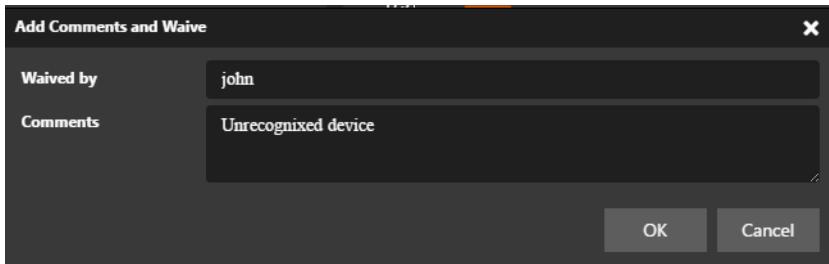


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Setting Schematic Sign Off Options

The *Add Comments and Waive* dialog box is displayed where you can leave notes on why the check is being waived.

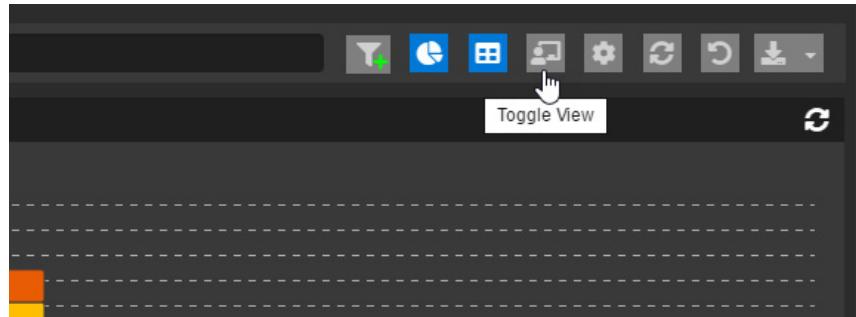
- Specify your name and a comment and click *OK*.



The violation is removed from the list.

Showing 312 of 312 rows. 				
Device Checks	 Value Unavailable On R/L/C	EAUDIT-22	Inductor L76 has no assigned value. Assign a value to the part.	
Device Checks	 Value Unavailable On R/L/C	EAUDIT-22	Inductor L77 has no assigned value. Assign a value to the part.	
Connectivity Checks	 Unconnected IC Power/Ground Pins	EAUDIT-20	Pin gnd(0) of U92 is not connected. Connect the power and ground pins of the part.	
Connectivity Checks	 Unconnected IC Power/Ground Pins	EAUDIT-20	Pin gnd(1) of U92 is not connected. Connect the power and ground pins of the part.	
Connectivity Checks	 Unconnected IC Power/Ground Pins	EAUDIT-20	Pin and(2) of U92 is not connected. Connect the power and ground pins of the part.	

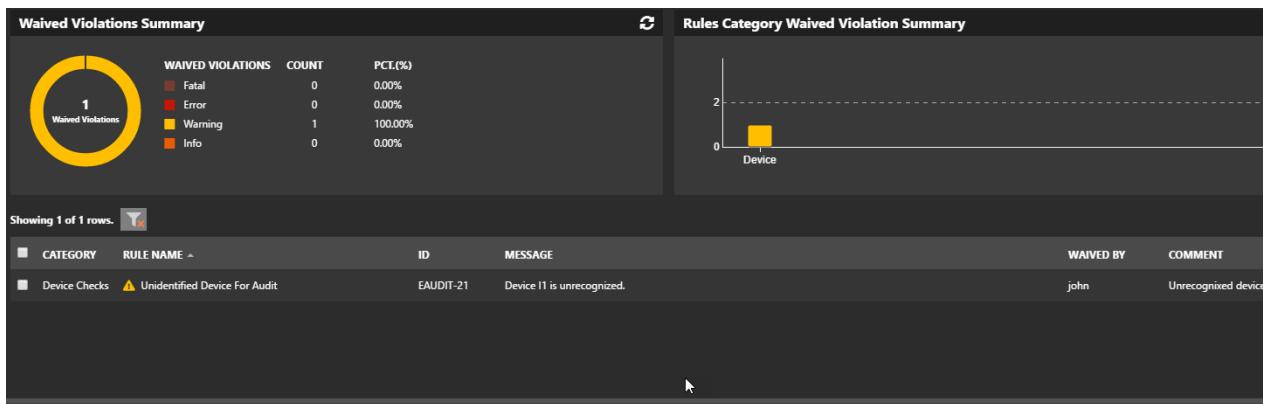
- Click the *Toggle View* icon to view the waived device in the pie chart.



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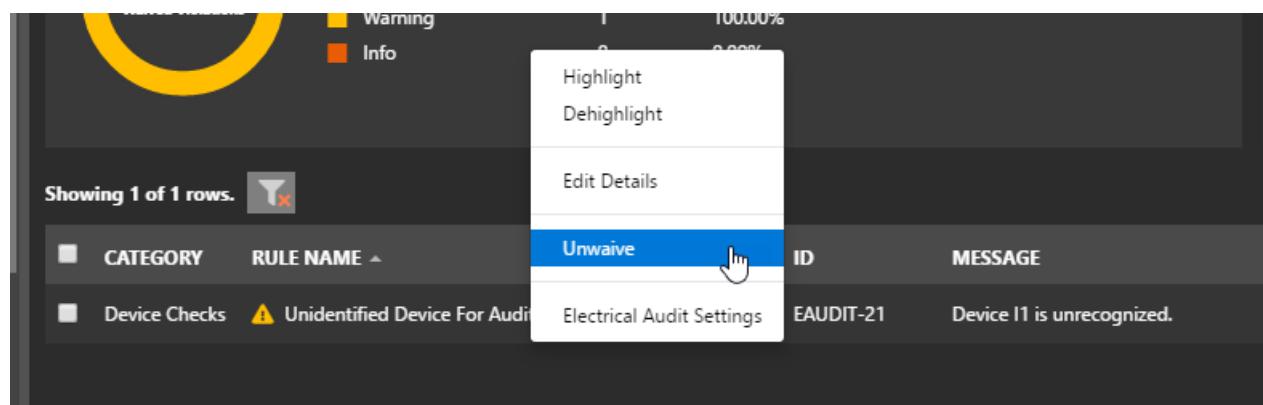
Setting Schematic Sign Off Options

The *Waived Violation Summary* report is displayed.



You can remove the violation from the list of waived violations at any time.

5. To remove the violation from the list, right-click the waived violation and choose *Unwaive*.



The violation is flagged again in the violations report.

The screenshot shows the 'Violations Summary' report. The row for 'Device Checks' (EAUDIT-21) is now highlighted with a red border, indicating it has been flagged again. The table below shows the violations:

CATEGORY	RULE NAME	ID	MESSAGE
Connectivity Checks	⚠️ Unconnected IC Power/Ground Pins	EAUDIT-20	Pin gnd(19) of U40 is not connected. Connect the power and ground pins.
Connectivity Checks	⚠️ Unconnected IC Power/Ground Pins	EAUDIT-20	Pin gnd(19) of U40 is not connected. Connect the power and ground pins.
Device Checks	⚠️ Unidentified Device For Audit	EAUDIT-21	Device I1 is unrecognized.
Device Checks	⚠️ Value Unavailable On R/L/C	EAUDIT-22	Inductor L67 has no assigned value. Assign a value to the part.
Device Checks	⚠️ Value Unavailable On R/L/C	EAUDIT-22	Inductor L68 has no assigned value. Assign a value to the part.

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Setting Schematic Sign Off Options

Analyzing Electrical Stress

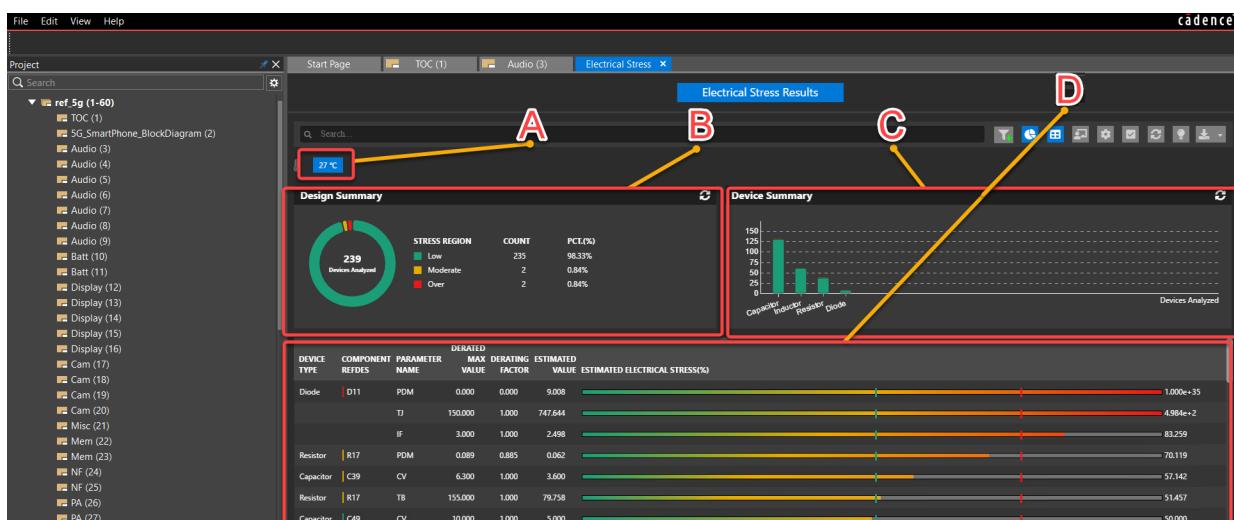
To check for overstressed components in the design, let's now run the Electrical Stress analysis on the sample design.

To analyze the electrical stress on the components, follow these steps:

1. Choose *Design Integrity – Analyze Electrical Stress*.

As the analysis runs in the background, progress messages are displayed continuously.

When the analysis completes, a detailed report is generated and displayed in a new tab, *Electrical Stress Results*. In the report, components in the overstressed region are indicated by a red bar along the component RefDes. The report includes information around the elements highlighted in the following image:



- ❑ *A – Ambient Temperature*
- ❑ *B – Design Summary* listing the total number of devices analyzed with the stress region
- ❑ *C – Device Summary* indicating the device types analyzed
- ❑ *D – Detailed list of all the overstressed devices*

Of the three reported issues, two pertain to the Diode, *D11*. This device is overstressed because of the following parameters:

- ❑ Power Dissipation (*PDM*)

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Setting Schematic Sign Off Options

- Junction Temperature (T_J)
- Forward Current (I_F)

DEVICE TYPE	COMPONENT REFDES	PARAMETER NAME	DERATED MAX VALUE	DERATING FACTOR	ESTIMATED VALUE	ESTIMATED ELECTRICAL STRESS(%)
Diode	D11	PDM	0.000	0.000	9.008	
		TJ	150.000	1.000	747.644	
		IF	3.000	1.000	2.498	
Resistor	R17	PDM	0.089	0.885	0.062	
Capacitor	C39	CV	6.300	1.000	3.600	
Resistor	R17	TB	155.000	1.000	79.758	
Capacitor	C49	CV	10.000	1.000	5.000	

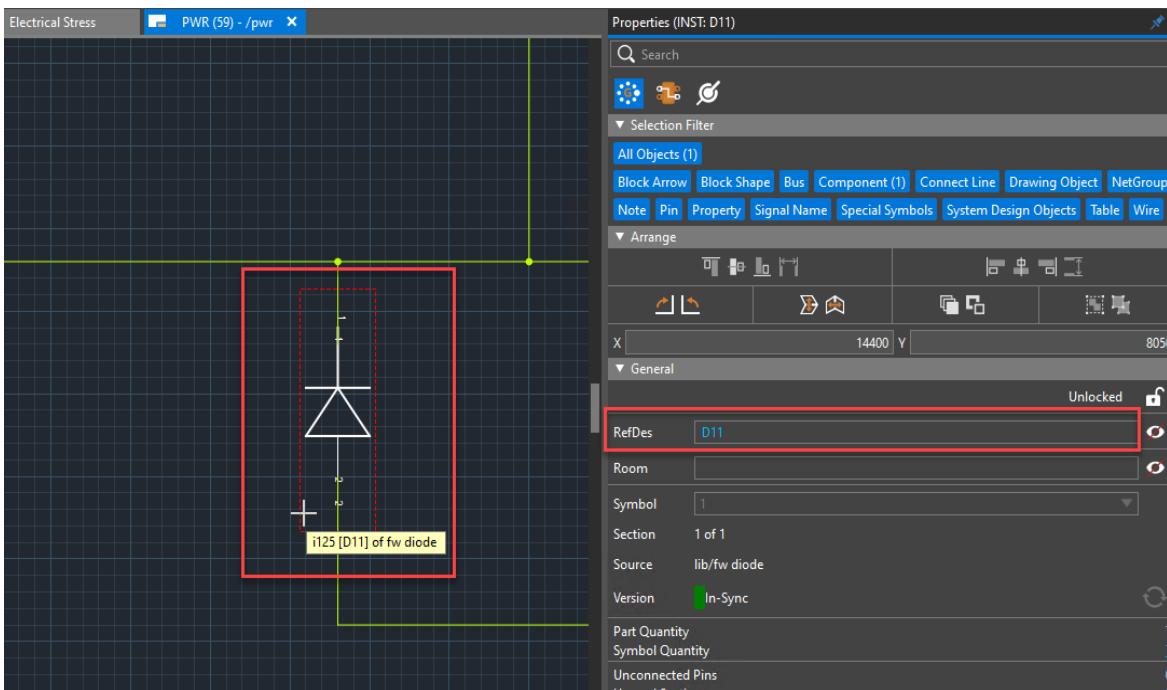
2. Right-click D_{11} and choose *Highlight Component* to locate the diode, D_{11} , in the design.

DEVICE TYPE	COMPONENT REFDES	PARAMETER NAME	DERATED MAX VALUE	DERATING FACTOR	ESTIMATED VALUE	ESTIMATED ELECTRICAL STRESS(%)
Capacitor	C10	TJ	0.0000	1.0000	1,626.9323	
Diode	D11	TJ	150.0000	1.0000	746.2255	
IC	U36	TJ	125.0000	1.0000	427.0280	

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Setting Schematic Sign Off Options

The corresponding schematic page opens in a new tab with *D11* highlighted on the canvas.



Some more tasks to perform for analysis of electrical stress are:

- [Managing Device Stress](#)
- [Running Incremental Analysis](#)
- [Configuring Custom Deration Settings](#)
- [Configuring Temperature Sweep](#)
- [Recognizing Unknown Devices](#)

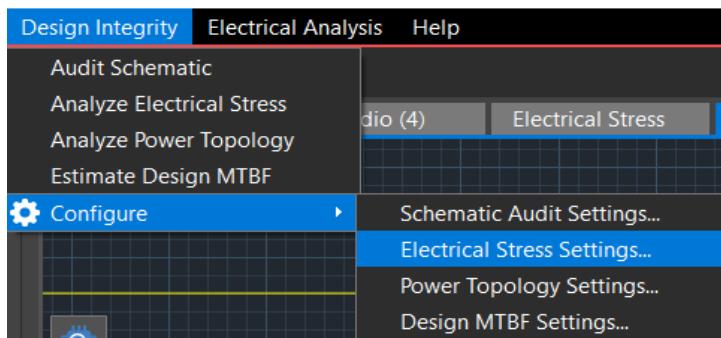
Managing Device Stress

You can modify the values of the reported parameters to reduce electrical stress on a device. To modify the parameter values for *D11*, follow these steps:

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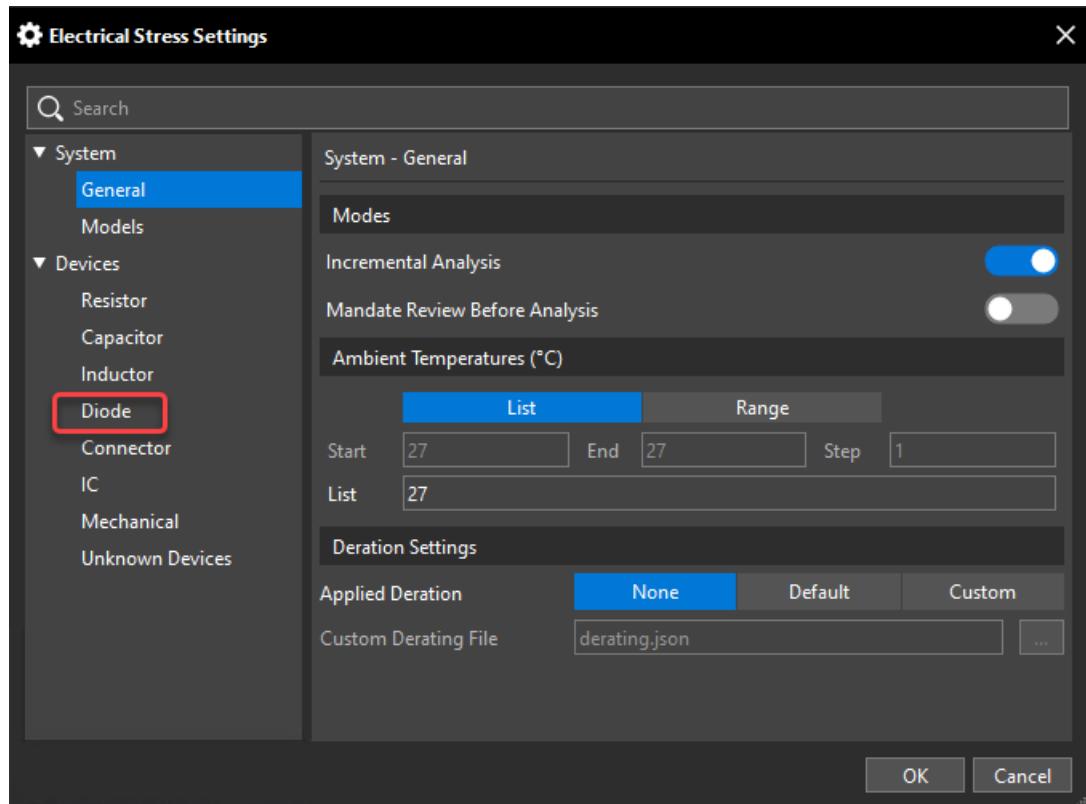
Setting Schematic Sign Off Options

1. Choose *Design Integrity – Configure – Electrical Stress Settings*.



The *Electrical Stress Settings* dialog box is displayed.

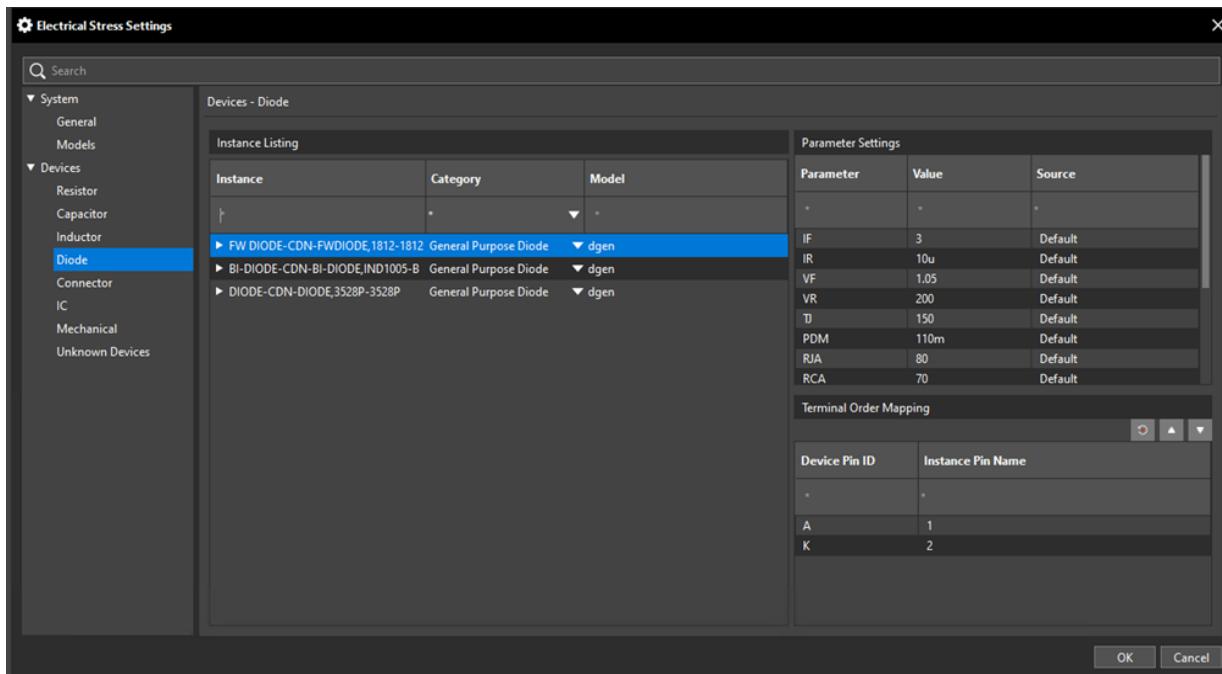
2. In the Devices section, select *Diode*.



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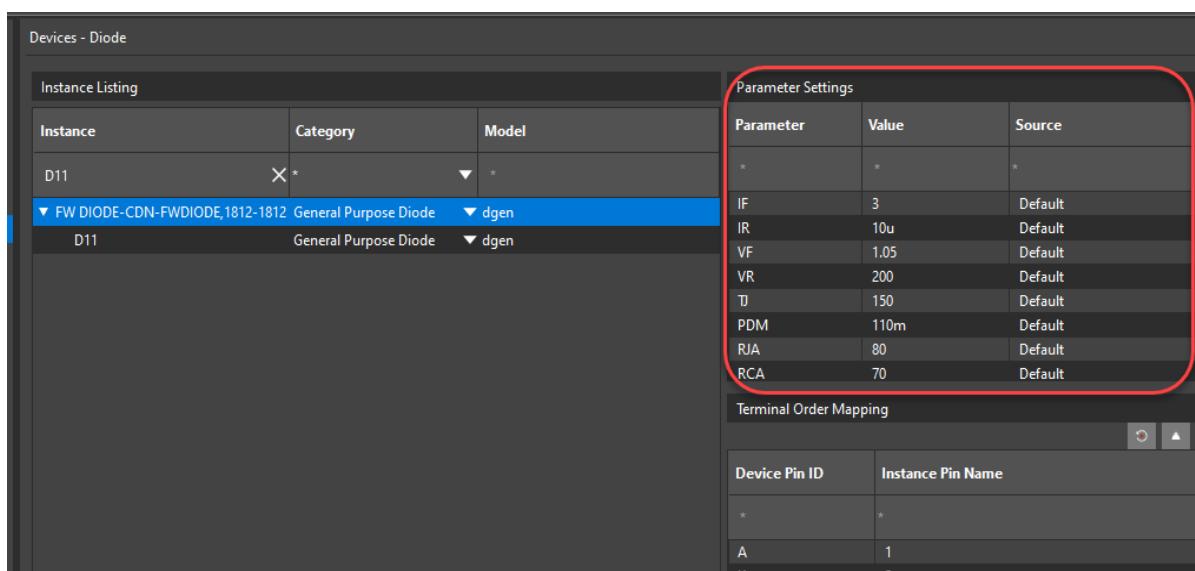
Setting Schematic Sign Off Options

All the diodes used in the design are listed along with the maximum operating values used for simulating each device.



3. To view the parameter values for the diode D_{11} , specify D_{11} in the *Instance* filter field.
4. Select D_{11} .

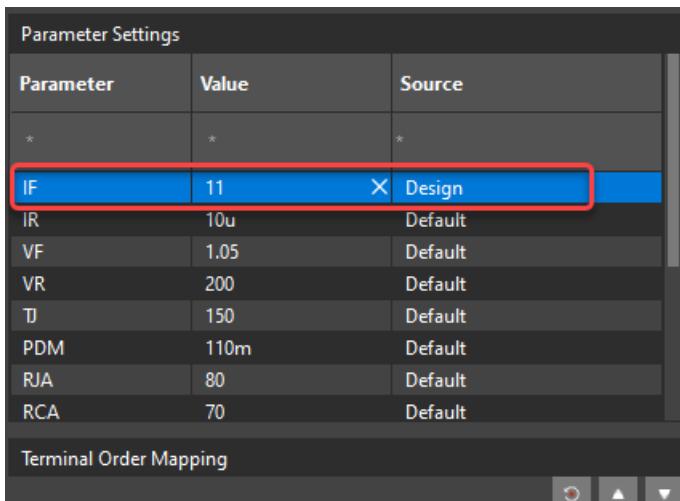
The parameter values are listed in the Parameter Settings section.



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Setting Schematic Sign Off Options

5. Change the value of the parameter *IF* from 3 to 11 and click *OK*.



6. Save the design.
7. Choose *Design Integrity – Analyze Electrical Stress* to verify that the issue is resolved after changing the parameter values.

DEVICE TYPE	COMPONENT REFDES	PARAMETER NAME	DERATED				ESTIMATED ELECTRICAL STRESS(%)
			MAX VALUE	DERATING FACTOR	ESTIMATED VALUE		
Diode	D11	PDM	0.000	0.000	9.008	<div style="width: 100%; background-color: green;"></div>	
		TJ	150.000	1.000	747.644	<div style="width: 100%; background-color: green;"></div>	
Resistor	R17	PDM	0.089	0.885	0.062	<div style="width: 100%; background-color: green;"></div>	
Capacitor	C39	CV	6.300	1.000	3.600	<div style="width: 100%; background-color: green;"></div>	
Resistor	R17	TB	155.000	1.000	79.758	<div style="width: 100%; background-color: green;"></div>	
Capacitor	C49	CV	10.000	1.000	5.000	<div style="width: 100%; background-color: green;"></div>	
Capacitor	C52	CV	10.000	1.000	4.966	<div style="width: 100%; background-color: green;"></div>	

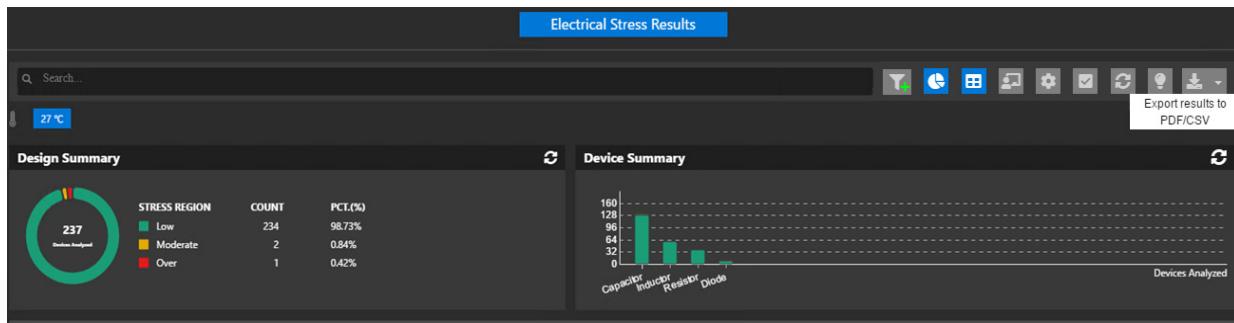
The newly generated report no longer lists the issue related to the *IF* parameter value. Similarly, you can resolve all the overstressed components by correcting the corresponding parameter values.

If required, you can export the analysis result and save it as a PDF or CSV file.

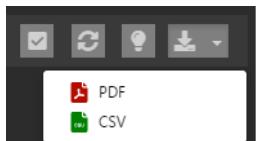
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Setting Schematic Sign Off Options

- Click the *Export results to PDF/CSV* icon to save the results in a CSV file.



- Choose CSV.



- Specify the name of the CSV file to be generated as *Stress Report* and click *Save*.

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Setting Schematic Sign Off Options

This Electrical Stress analysis report can be used as a sign off report.

Electrical Stress Results For Temperature 27 degC									
A1	B	C	D	E	F	G	H	I	J
1	Electrical Stress Results For Temperature 27 degC								
2									
3	Low Stress: Moderate Over Stress: Total Devices Analyzed								
4	234	2	1	237					
5									
6									
7	Device	Low Stress: Moderate Over Stress: Total Count							
8	Capacitor	129	1	0	130				
9	Diode	9	0	1	10				
10	Inductor	59	0	0	59				
11	Resistor	37	1	0	38				
12									
13									
14	Device	Component	Stress Category	Parameter	Parameter	Max Value	Derating Factor	Estimated Current	Estimated RMS (%)
15	Capacitor C1	Low	CI	Current	1	100	2.56E-07	2.56E-05	
16	Capacitor C1	Low	CV	Voltage	16	100	1.48E-05	9.28E-05	
17	Capacitor C2	Low	CI	Current	1	100	3.02E-10	3.02E-08	
18	Capacitor C2	Low	CV	Voltage	25	100	4.17E-06	1.67E-05	
19	Capacitor C3	Low	CI	Current	1	100	3.02E-10	3.02E-08	
20	Capacitor C3	Low	CV	Voltage	25	100	4.17E-06	1.67E-05	
21	Capacitor C4	Low	CI	Current	1	100	0.000437	0.043743	
22	Capacitor C4	Low	CV	Voltage	25	100	2.34825	9.39301	
23	Capacitor C5	Low	CI	Current	1	100	6.05E-10	6.05E-08	
24	Capacitor C5	Low	CV	Voltage	25	100	8.35E-06	3.34E-05	
25	Capacitor C6	Low	CI	Current	1	100	0.000437	0.043743	
26	Capacitor C6	Low	CV	Voltage	25	100	2.34825	9.39301	
27	Capacitor C7	Low	CI	Current	1	100	1.62E-18	0	
28	Capacitor C7	Low	CV	Voltage	25	100	0.000396	0.001584	
29	Capacitor C31	Low	CI	Current	1	100	0.001679	0.167875	
30	Capacitor C31	Low	CV	Voltage	6.3	100	0.000939	0.014902	
31	Capacitor C36	Low	CI	Current	1	100	0.025017	2.50165	
32	Capacitor C36	Low	CV	Voltage	10	100	0.142514	1.42514	
33	Capacitor C37	Low	CI	Current	1	100	0.025017	2.50165	
34	Capacitor C37	Low	CV	Voltage	10	100	0.142514	1.42514	
35	Capacitor C39	Moderate	CI	Current	1	100	4.87E-08	4.87E-06	
36	Capacitor C39	Moderate	CV	Voltage	6.3	100	3.59993	57.1417	
37	Capacitor C49	Low	CI	Current	1	100	7.12E-07	7.12E-05	
38	Capacitor C49	Low	CV	Voltage	10	100	5	50	

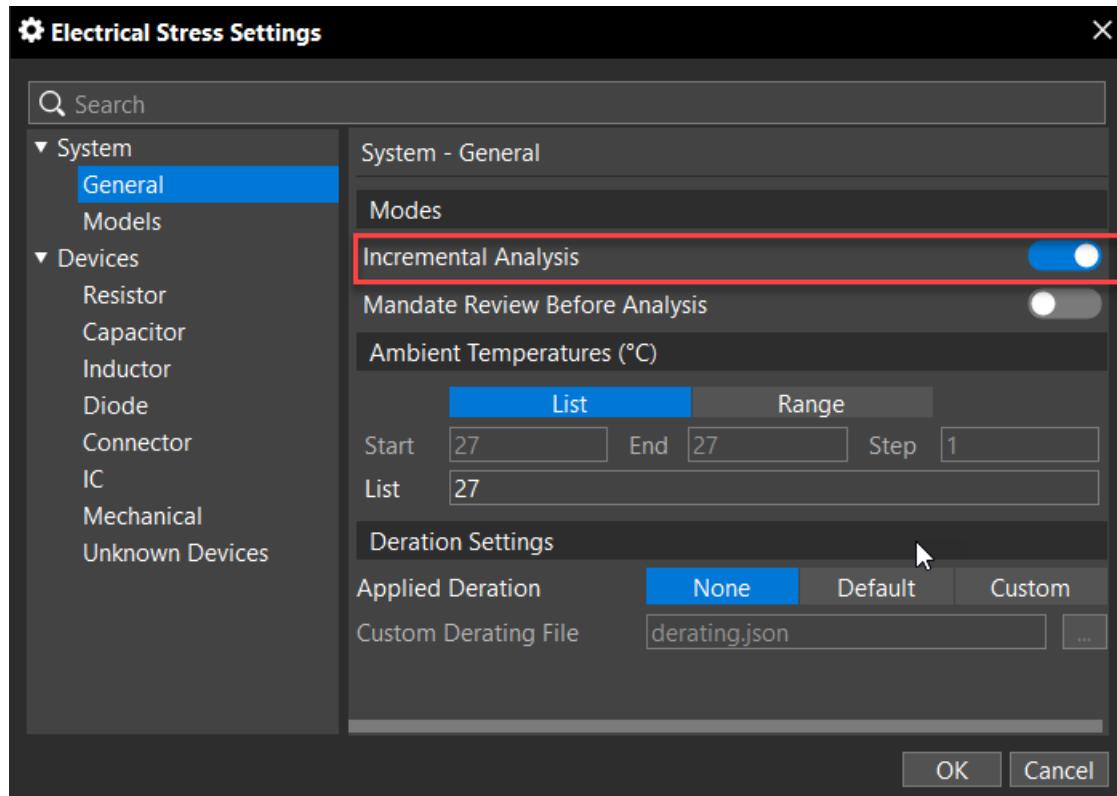
Running Incremental Analysis

To save analysis time, instead of simulating the entire design each time you run electrical stress analysis, you can simulate only the subcircuits that changed since the previous run of the analysis.

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

In the *Electrical Stress Settings* dialog box, ensure that the *Incremental Analysis* toggle is on.



When you run the analysis in the Incremental Analysis mode, information about unchanged subcircuits is fetched from the last run of the analysis. This significantly brings down the analysis time. The following image highlights the time taken to complete electrical stress

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

analysis in both the modes. Notice that the incremental mode (Incremental Stress Analysis) has taken less than half the time of the default mode (Complete Stress Analysis).

```
stimulus is applied on port AP44 of device 'U81' with the following values derived from these properties: V
maximum supply voltage of IC; VOL = 0 default value; TR = 10n default value; TF = 10n default value;
Stimulus is applied on port 13 of device 'U83' with the following values derived from these properties: VOH
supply voltage of IC; VOL = 0 default value; TR = 10n default value; TF = 10n default value;
Stimulus is applied on port 21 of device 'U83' with the following values derived from these properties: VOH
supply voltage of IC; VOL = 0 default value; TR = 10n default value; TF = 10n default value;
Stimulus is applied on port 1 of device 'U97' with the following values derived from these properties: VOH
= 0 default value; TR = 10n default value; TF = 10n default value;
'U2.4' 'U81.B24' 'U86.1'
Ignoring subcircuit177 for analysis as it has unspecified ports 'U2.4' 'U81.B24' 'U86.1' present in it.
Time taken to generate the simulation netlists is 8.538000 seconds.
Time taken to simulate the netlists is 48.803001 seconds.
Simulation of extracted subcircuits completed.
```

Complete Stress Analysis

```
Stimulus is applied on port AP44 of device 'U81' with the following values derived from these properties:
maximum supply voltage of IC; VOL = 0 default value; TR = 10n default value; TF = 10n default value;
Stimulus is applied on port 13 of device 'U83' with the following values derived from these properties:
supply voltage of IC; VOL = 0 default value; TR = 10n default value; TF = 10n default value;
Stimulus is applied on port 21 of device 'U83' with the following values derived from these properties:
supply voltage of IC; VOL = 0 default value; TR = 10n default value; TF = 10n default value;
Stimulus is applied on port 1 of device 'U97' with the following values derived from these properties:
= 0 default value; TR = 10n default value; TF = 10n default value;
'U2.4' 'U81.B24' 'U86.1'
Ignoring subcircuit177 for analysis as it has unspecified ports 'U2.4' 'U81.B24' 'U86.1' present in it.
Time taken to generate the simulation netlists is 8.332000 seconds.
Time taken to simulate the netlists is 22.540001 seconds.
Simulation of extracted subcircuits completed.
```

Incremental Stress Analysis

Configuring Custom Deration Settings

To decrease stress on components and obtain more accurate results, System Capture provides default and custom derating values on devices used in stress analysis.

To specify custom derating values, follow these steps:

1. Choose *Design integrity – Configure – Electrical Stress Settings*.
2. In the *Electrical Stress Setting* dialog box, choose *System – General – Deration Settings* to view the deration settings.

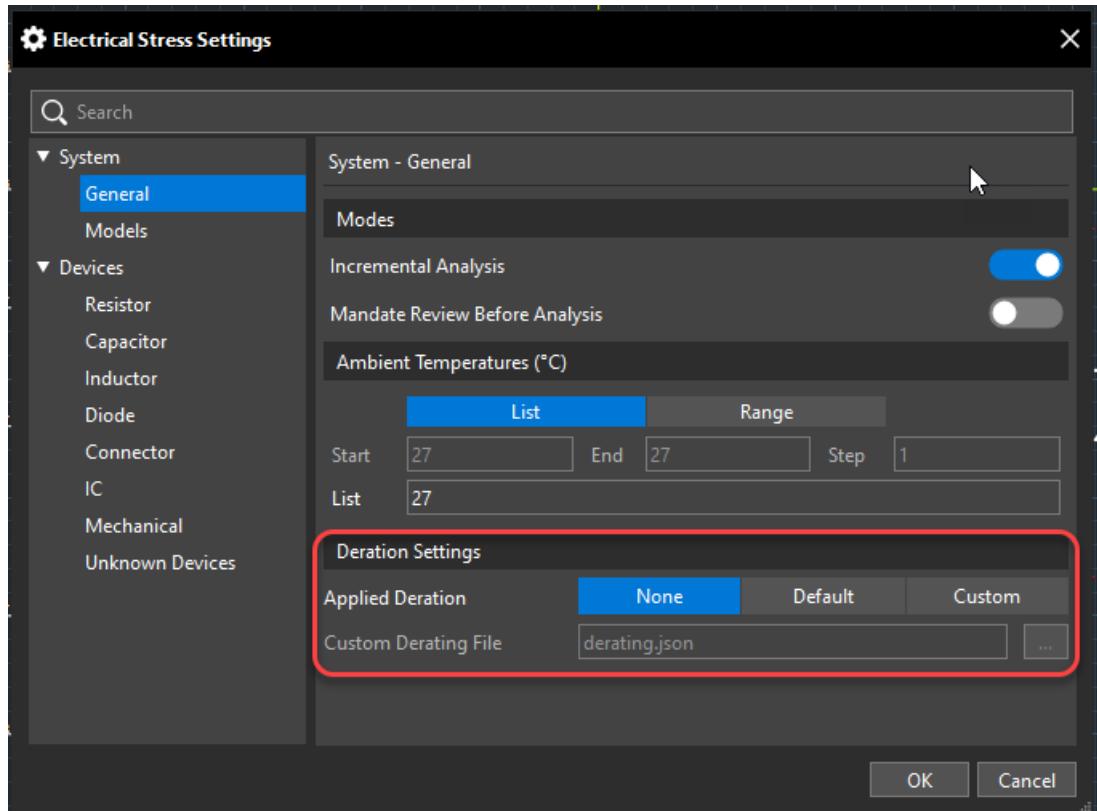
To run stress analysis, System Capture uses the following derating values of devices:

- None*: No Derations

Allegro X System Capture - Schematic Sign Off Tutorial

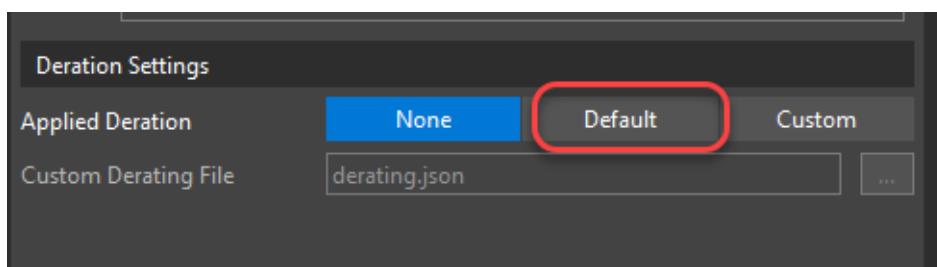
Setting Schematic Sign Off Options

- *Default:* Cadence Default Derations
- *Custom:* User-Defined Deration



3. Click *Default* in the Deration Settings section and click *OK* to specify Cadence default derating values.

The Cadence default derating values are stored at the following location:
SITE\cdssetup\sysr\config.xml.



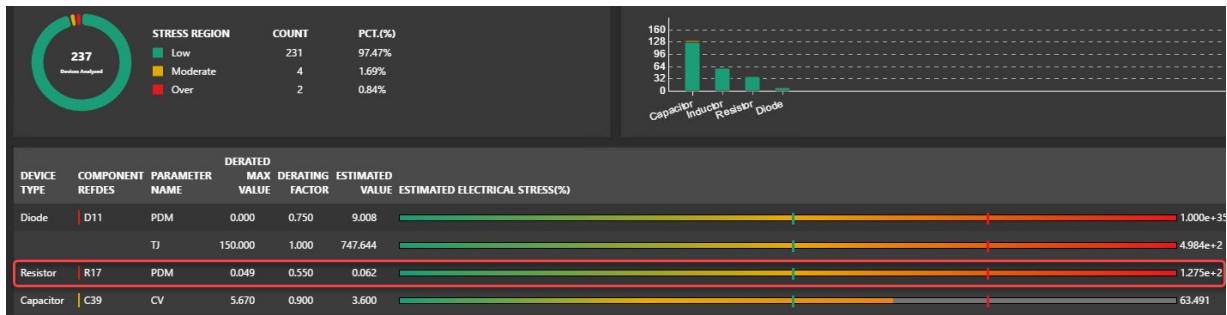
Let's run the stress analysis one more time.

4. Choose *Design integrity – Analyze Electrical Stress*.

Allegro X System Capture - Schematic Sign Off Tutorial

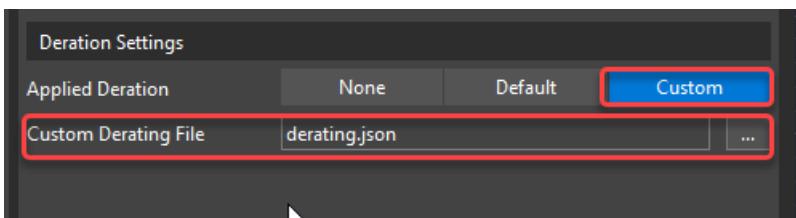
Setting Schematic Sign Off Options

The Electrical Stress Results tab shows some components falling in the overstressed region (red). The resistor, *R17* is one such component.



To resolve this issue, manually customize the derating value of the resistor, *R17*.

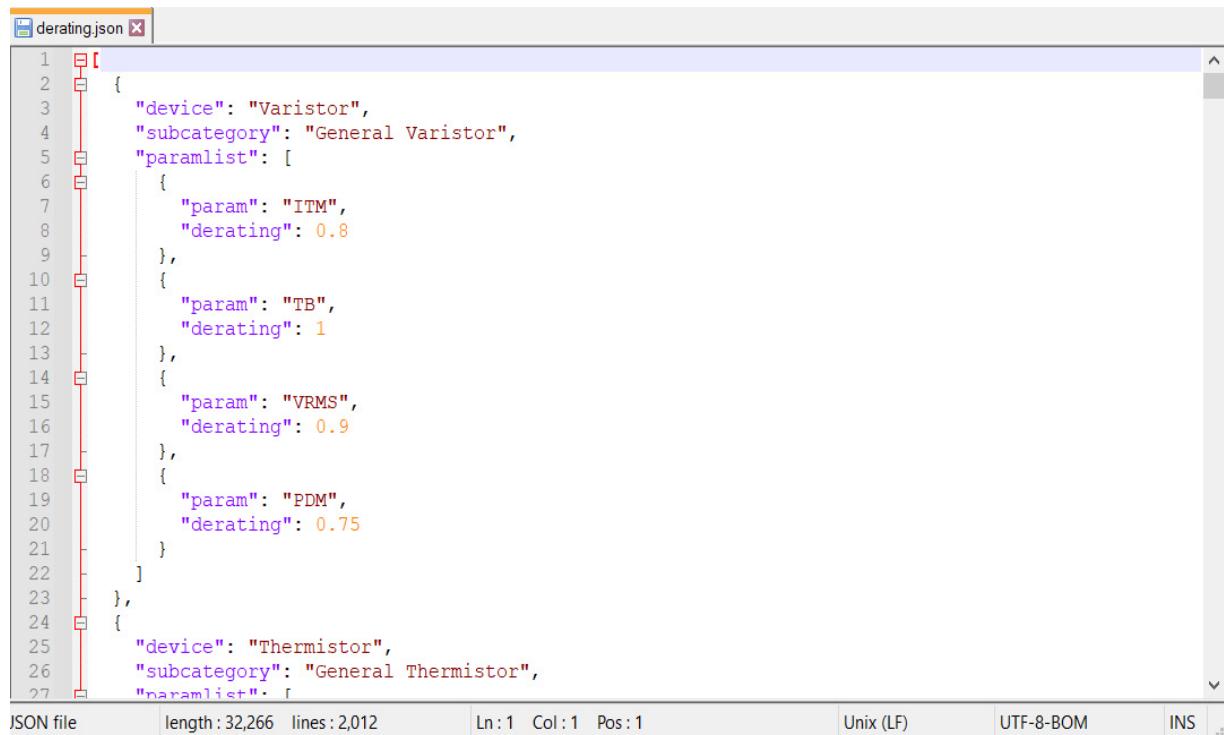
5. Open any sheet to enable the *Design Integrity* menu commands.
6. Choose *Design Integrity – Configure – Electrical Stress Settings*.
7. In the *Electrical Stress Settings* dialog box, click *Custom* under *System – General – Derating Settings*.
8. Click the ellipsis button (...) for the *Custom Derating File* field to locate the file named *derating.json*.



Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

9. Open derating.json with any text editor, preferably *Notepad++*.



The screenshot shows the Notepad++ text editor with the file "derating.json" open. The code is a JSON object defining device parameters and their derating values. The "paramlist" array contains five entries, each with a parameter name and its corresponding derating value.

```
1 [ {  
2   "device": "Varistor",  
3   "subcategory": "General Varistor",  
4   "paramlist": [  
5     {  
6       "param": "ITM",  
7       "derating": 0.8  
8     },  
9     {  
10      "param": "TB",  
11      "derating": 1  
12    },  
13    {  
14      "param": "VRMS",  
15      "derating": 0.9  
16    },  
17    {  
18      "param": "PDM",  
19      "derating": 0.75  
20    }  
21  ],  
22  {  
23    "device": "Thermistor",  
24    "subcategory": "General Thermistor",  
25    "paramlist": [  
26    ]  
27  }  
}
```

Below the code, the status bar displays: JSON file | length : 32,266 lines : 2,012 | Ln:1 Col:1 Pos:1 | Unix (LF) | UTF-8-BOM | INS | .

Search for a resistor with the *SMD_Thick* subcategory.

10. Press **CTRL + F** and search for *SMD_Thick*.

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

11. Change the derating value of *Power Dissipation (PDM)* from 0.55 to 1.

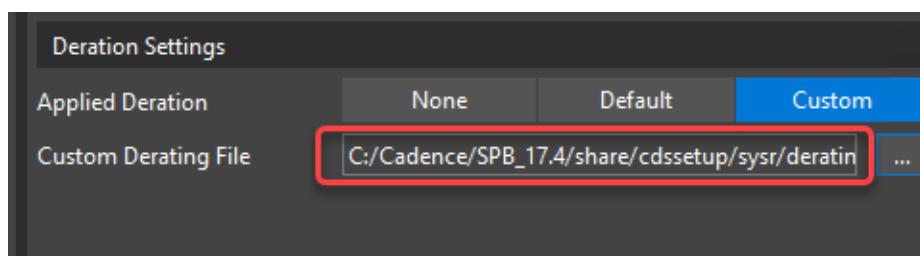


```
derating.json
88     "derating": 0.8
89   }
90   ],
91 },
92 {
93   "device": "Resistor",
94   "subcategory": "SMD_Thick",
95   "paramlist": [
96     {
97       "param": "PDM",
98       "derating": 1
99     },
100    {
101      "param": "TB",
102      "derating": 1
103    },
104    {
105      "param": "RV",
106      "derating": 0.8
107    }
108  ],
109 },
110 {
111   "device": "Resistor",
112   "subcategory": "SMD_Thin",
113   "paramlist": [
114     ...
115   ]
116 }
```

JSON file length : 32,263 lines : 2,012 Ln : 115 Col : 24 Pos : 1,833 Unix (LF) UTF-8-BOM INS

12. Save the changes and close the editor.

Notice that the path to the `derating.json` file is updated.



13. Click *OK* to save the changes made to the derating settings.

14. Analyze electrical stress again and check the results.

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

Notice that with the derating factor increased for *R17*, the estimated electrical stress for the device has reduced, and it is no longer in the overstressed devices zone (red).

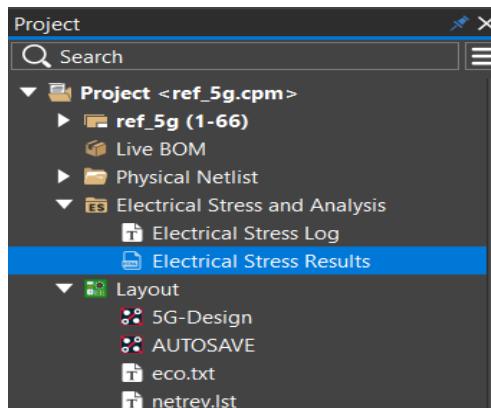
DEVICE TYPE	COMPONENT REFDES	PARAMETER NAME	DERATED MAX VALUE	DERATING FACTOR	ESTIMATED VALUE	ESTIMATED ELECTRICAL STRESS(%)
Diode	D11	PDM	0.000	0.750	9.008	1.000e+35
		TJ	150.000	1.000	747.644	4.984e+2
Resistor	R17	PDM	0.089	1.000	0.062	70.119
Capacitor	C39	CV	5.670	0.900	3.600	63.491
Capacitor	C49	CV	9.000	0.900	5.000	55.556
Capacitor	CS2	CV	9.000	0.900	4.966	55.176
Inductor	L79	LI	4.500	0.900	2.476	55.027

Configuring Temperature Sweep

The *Temperature Sweep* functionality lets you run *EOS (Electrical Overstress)* analysis at different temperature levels in one go.

To view the existing *Stress Analysis Report* of *ref_5G* design, follow these steps:

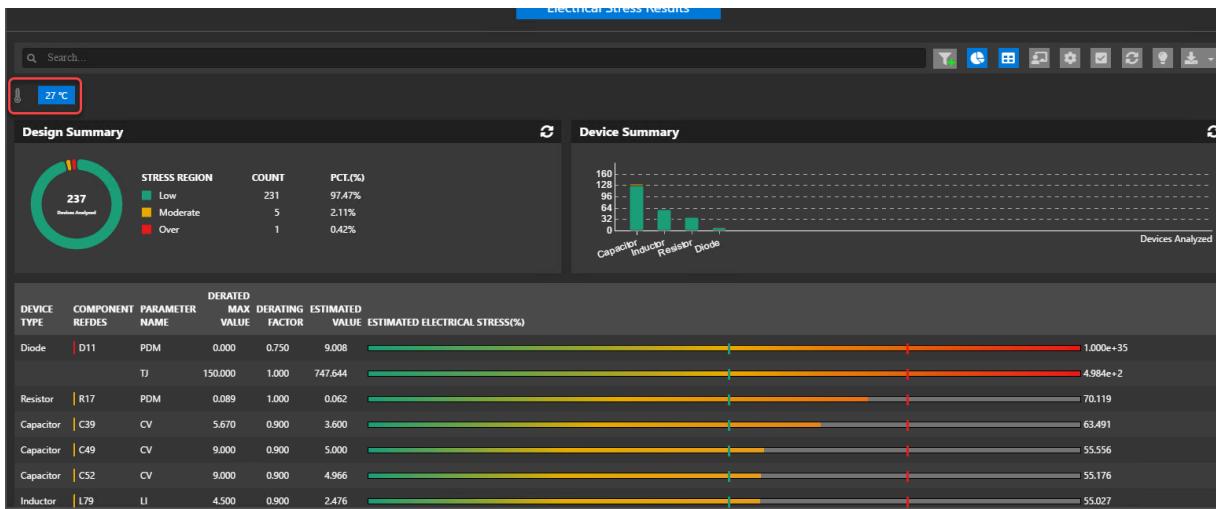
1. Select *Electrical Stress and Analysis – Electrical Stress Results*, in the *Project Explorer* panel.



Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

The *Electrical Stress Results* report is displayed. Notice that the default *Ambient Temperature* is set to 27°C.



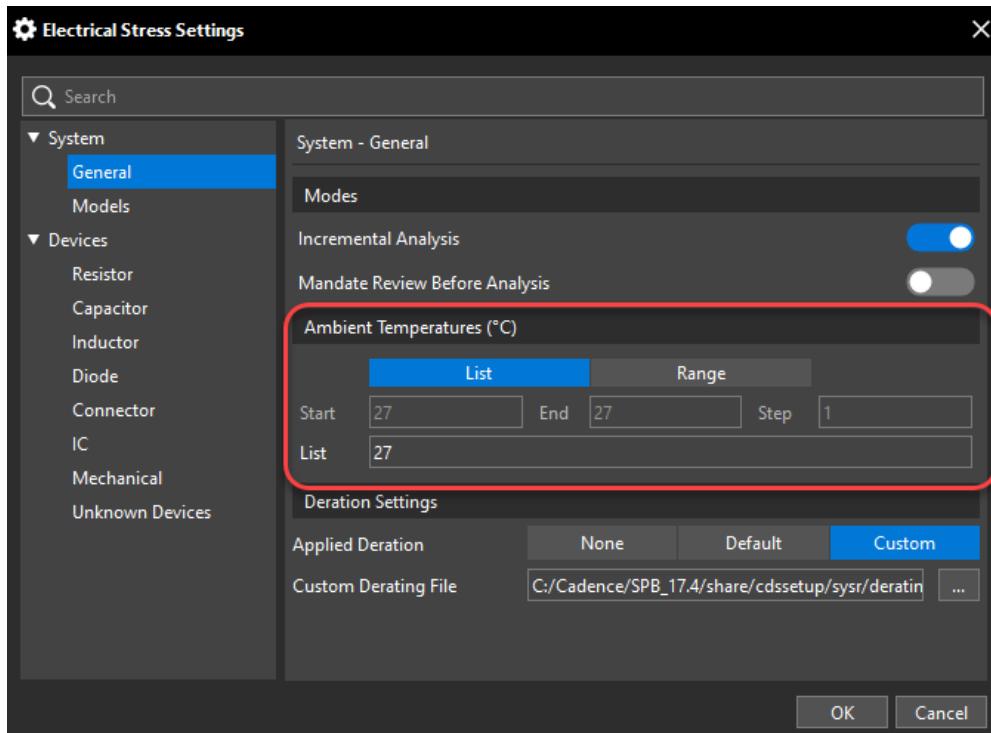
You can vary the temperature settings in the *Electrical Stress Settings* dialog box to analyze the electrical stress on devices at different temperatures.

2. Choose *Design Integrity – Configure – Electrical Stress Settings*.

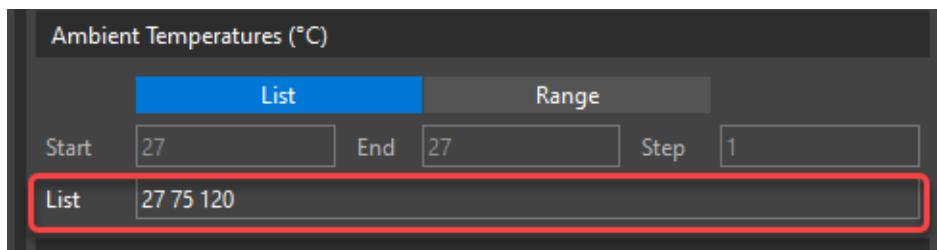
Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

In the Ambient Temperatures section, notice that the start and end default temperatures are set at 27 °C.



- Specify the following space-separated values in the *List* field:
27 75 120.

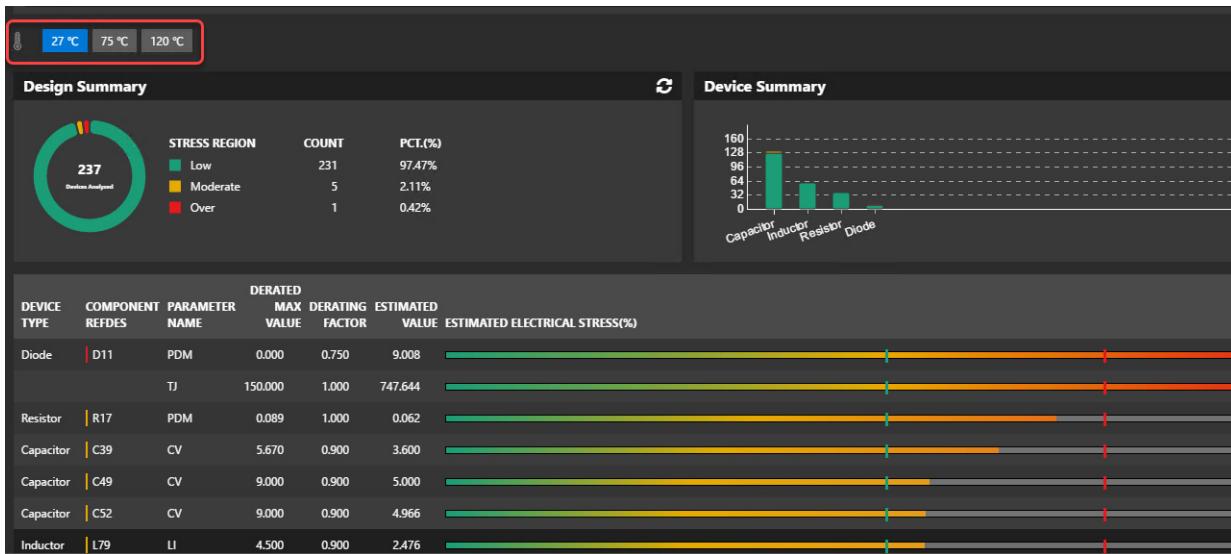


- Click *OK*.
- Choose *Design Integrity – Analyze Electrical Stress* to re-run Electrical Stress analysis.

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

After the completion of the analysis, the detailed *Electrical Stress Results* report for different temperature values is displayed.



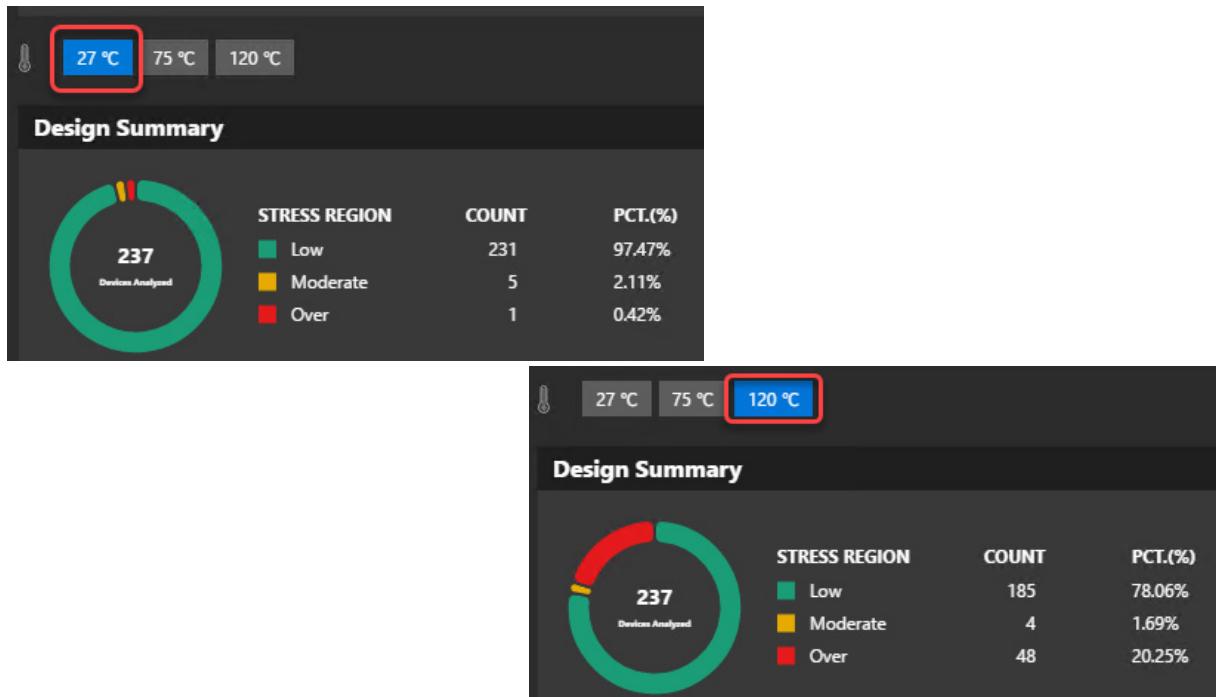
6. Click 120°C to display the *Electrical Stress Results* report for the temperature.



Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

Notice the difference between the reports for 27°C and 120°C in the *Design Summary* section of the *Electrical Stress Results* report.



You can navigate to the overstressed components and resolve the identified issues by editing the custom derating values and stress levels.

You can also compare the analysis results for other temperature values and save the results in a .csv file.

Recognizing Unknown Devices

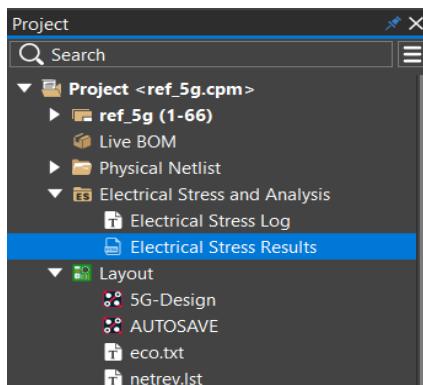
The devices used in a design are recognized by System Capture based on their classification. If a device is not identified, it is assigned to the *Unknown Device* category. While running Electrical Stress analysis, *Unknown Devices* are automatically skipped. However, they can be included in the analysis by manual recognition.

To locate and manually recognize *Unknown Devices* in the existing *Electrical Stress Results* report, follow these steps:

Allegro X System Capture - Schematic Sign Off Tutorial

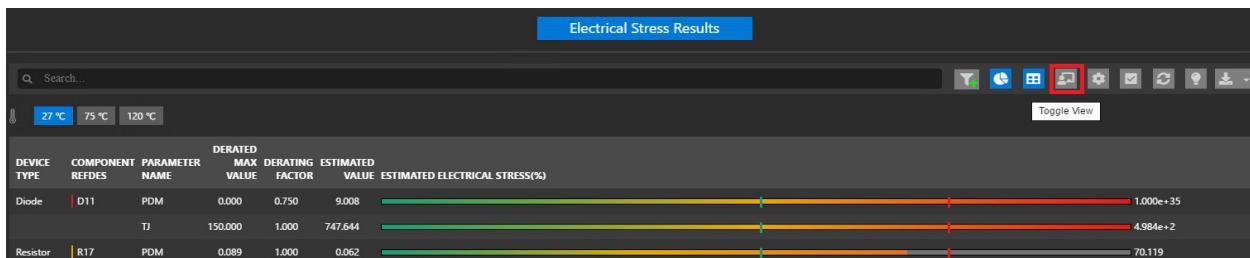
Setting Schematic Sign Off Options

1. Select *Electrical Stress and Analysis – Electrical Stress Results* in the *Project Explorer* panel to view the existing Stress Analysis Report.

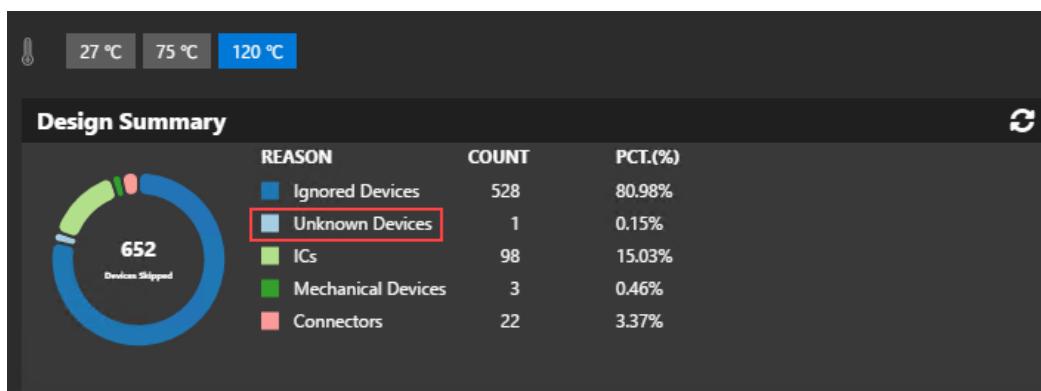


The *Electrical Stress Results* report is displayed.

2. Click the *Toggle View* icon to view the *Design Summary* of the skipped devices in the report.



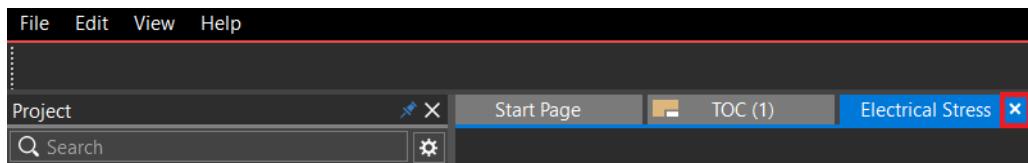
Notice that one device is listed as an unknown device indicating that it is not recognized by System Capture.



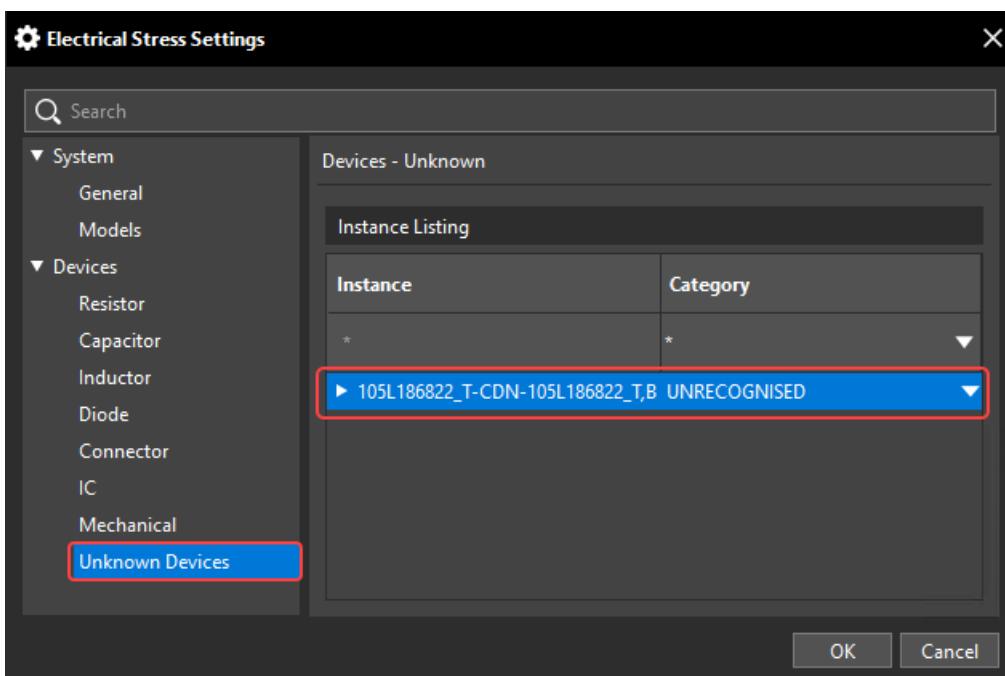
Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

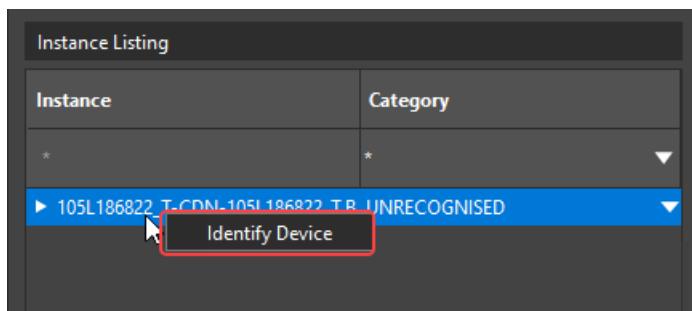
3. Close the *Electrical Stress* tab to manually identify or recognize the unknown device.



4. Choose *Design Integrity – Configure – Electrical Stress Settings*.
5. In the *Electrical Stress Settings* dialog box, click *Devices – Unknown Devices*.



6. Select the device, right-click in the instance column, and choose *Identify Device*.

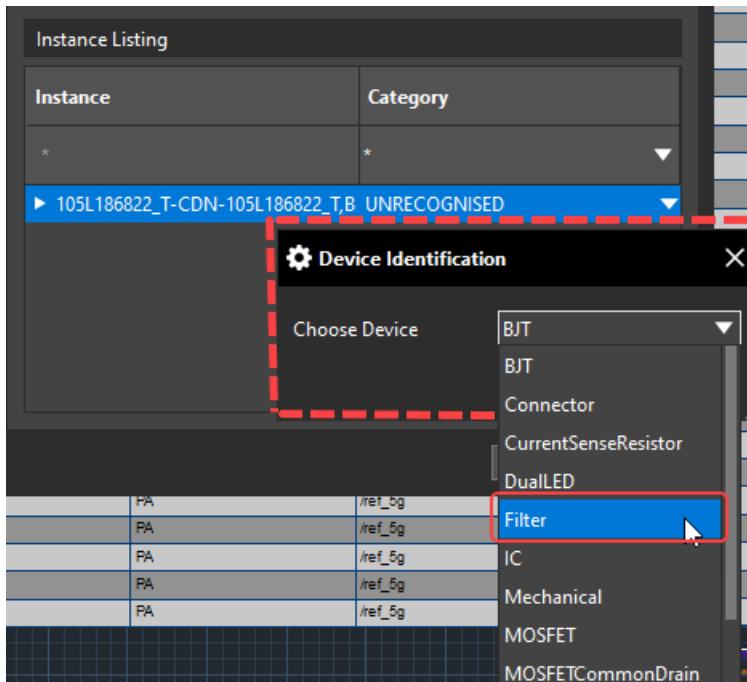


The *Device Identification* dialog box displays.

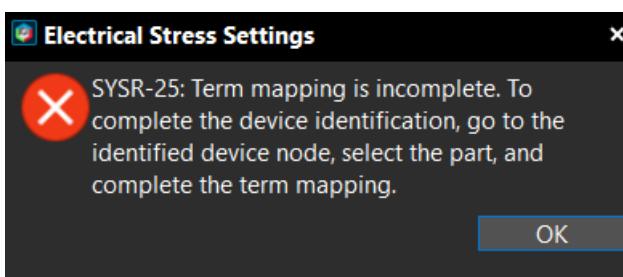
Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

7. In the *Device Identification* dialog box, select *Filter* from the *Choose Device* list and click *OK*.



System Capture prompts you to complete the term mapping for the recently recognized device.

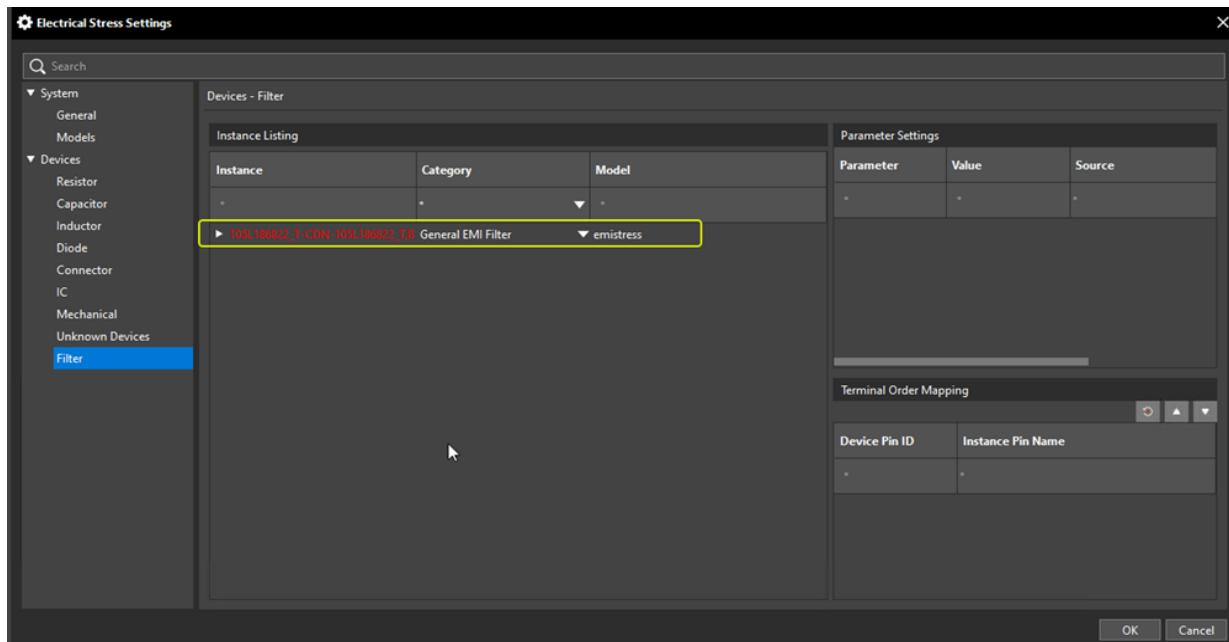


8. Click *OK*.
9. In the *Electrical Stress Settings* dialog box, click *Filter* in the Devices section.

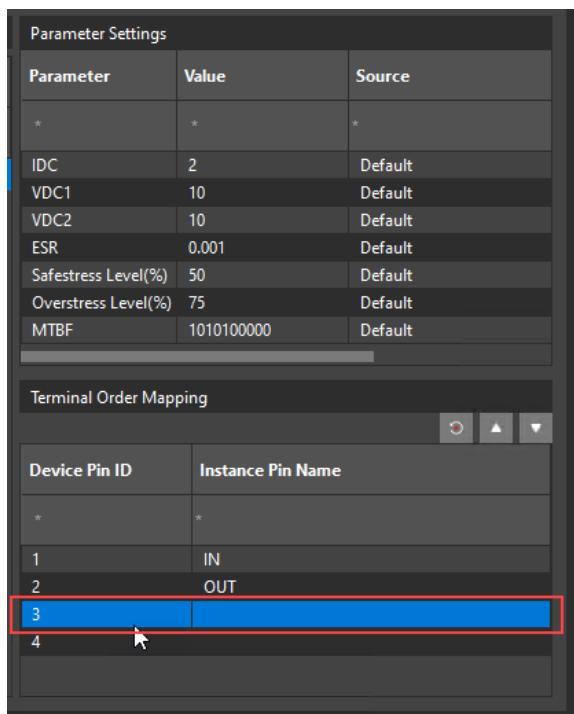
Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

The recently recognized device displays in red, signifying incomplete term mapping.



10. Select the device in the *Instance Listing* section.
11. In the *Terminal Order Mapping* section, select 3 in the *Device Pin ID* column.



Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

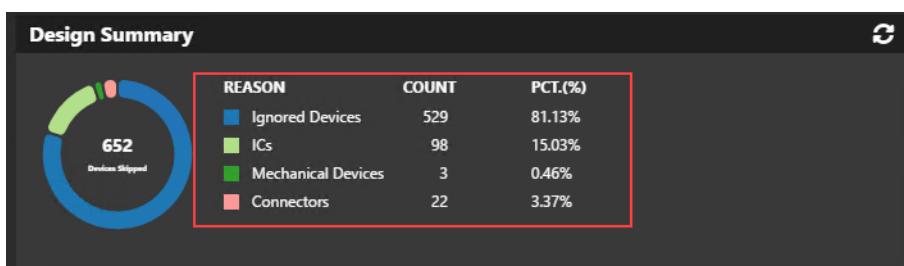
12. For the *Instance Pin Name* cell corresponding to pin 3, choose *GND_0* from the drop-down list.

Terminal Order Mapping	
Device Pin ID	Instance Pin Name
*	*
1	IN
2	OUT
3	GND_0
4	

13. Similarly, for the *Instance Pin Name* corresponding to pin 4, choose *GND_1* from the drop-down list and click *OK*.

Terminal Order Mapping	
Device Pin ID	Instance Pin Name
*	*
1	IN
2	OUT
3	GND_0
4	GND_1

14. Choose *File – Save All*.
15. Choose *Design Integrity – Electrical Stress Analysis*.
16. Click the *Toggle View* icon and view the Design Summary section of the *Electrical Stress Results* report.



Notice that there are no more *Unknown Devices* in the design.

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Schematic Sign Off Options

Setting Up Electrical Constraints

Electrical constraints govern the electrical behavior of a net or pin-pair in a design. The constraints captured in the design phase help meet the electrical criteria of the final physical board. Working with System Capture, you can define constraints in the docked Constraint Manager window or in the Constraint Manager application integrated with System Capture. You can also define common constraints together into an Electrical Constraints Set (ECSet) and assign them to nets. ECSets can be created in Constraint Manager and in Topology Workbench.

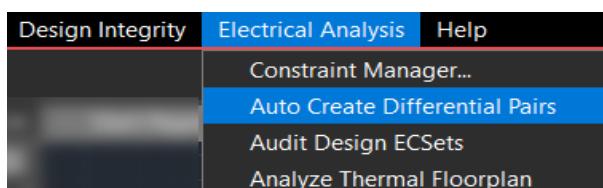
All the constraints, irrespective of where they are created, are displayed in both the docked Constraint Manager window as well as the Constraint Manager application.

Adding Constraints in Constraint Manager

The docked Constraint Manager window provides a quick snapshot of the constraints on the selected nets. You can also set up constraints at the net-level or DiffPair-level in the docked Constraint Manager window. In this section, you will define constraints on automatically-created differential pairs.

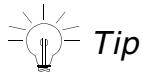
To add constraints to a differential pair, follow these steps:

1. Choose *Electrical Analysis – Auto Create Differential Pairs* to initiate the auto creation of differential pairs.



Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints



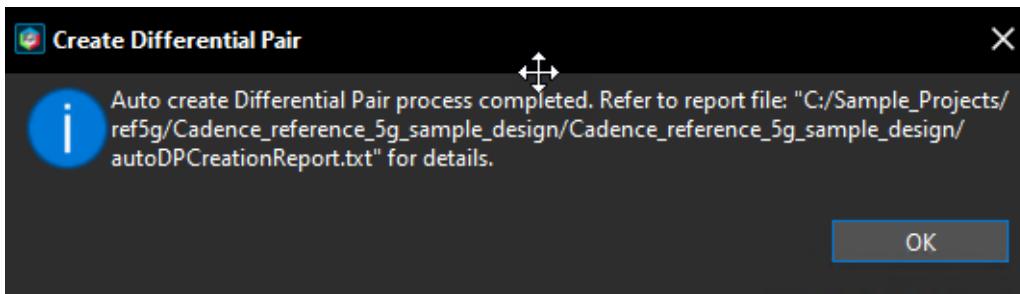
Tip

You can also run this operation from the *TCL Command Window* by typing the TCL command *cnsAutoCreateDiffPair*.

```
Command
Search
refreshDesignExplorer
PFM- hardware check OK
Tcl> selectObject 17230 17078
Tcl> launchPreferences
cps:contextCall SCH PAGE (updateUserPreferences -theme dark -schematicSheetTheme dark -schematicSheetBackgroundColor Light)
updateUserPreferences -theme dark -schematicSheetTheme dark -schematicSheetBackgroundColor Light
sdaStartPage::reloadStartPage
Tcl> cnsAutoCreateDiffPair

Command Session Log Violation Unified Search
```

2. A message pops up informing about the completion of the process and the location of the generated report file.

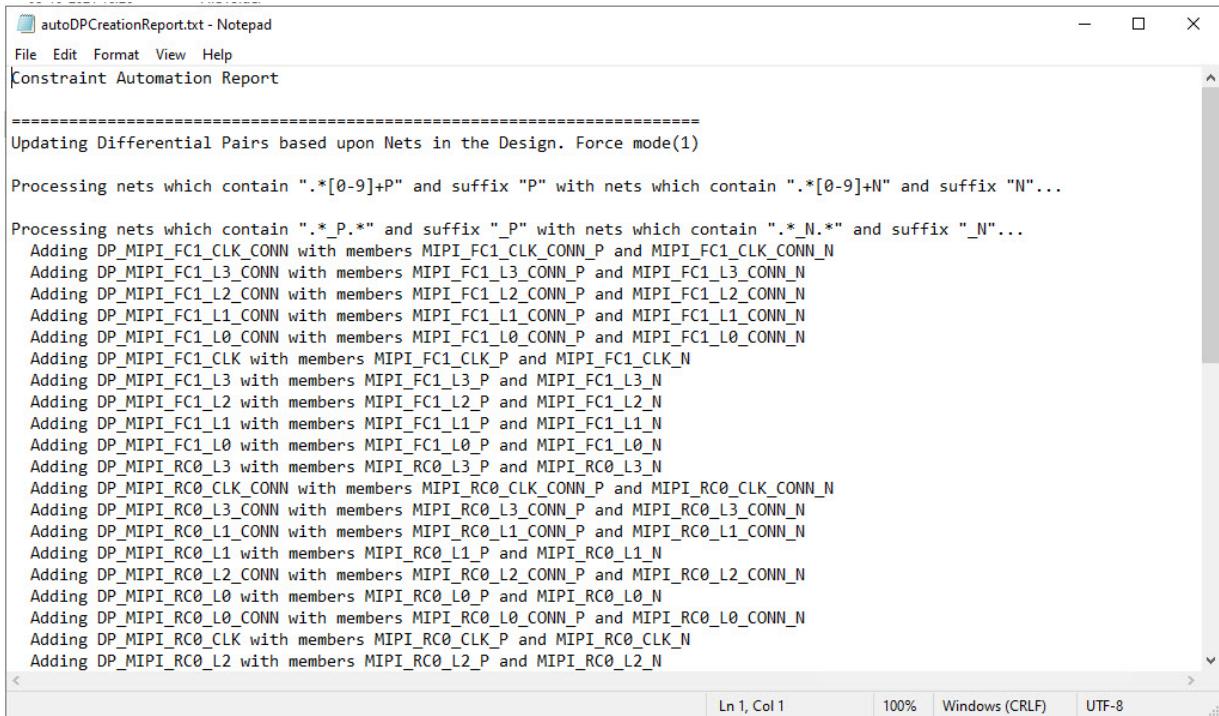


3. Click *OK*.

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints

The generated report file, `autoDPCreationReport.txt`, is stored in the design folder. To open the design folder, from the *Start page*, choose *File – Open Project Folder*.



```
autoDPCreationReport.txt - Notepad
File Edit Format View Help
Constraint Automation Report

=====
Updating Differential Pairs based upon Nets in the Design. Force mode(1)

Processing nets which contain ".*[0-9]+P" and suffix "P" with nets which contain ".*[0-9]+N" and suffix "N"...

Processing nets which contain ".*_P.*" and suffix "_P" with nets which contain ".*_N.*" and suffix "_N"...
    Adding DP_MIPI_FC1_CLK_CONN with members MIPI_FC1_CLK_CONN_P and MIPI_FC1_CLK_CONN_N
    Adding DP_MIPI_FC1_L3_CONN with members MIPI_FC1_L3_CONN_P and MIPI_FC1_L3_CONN_N
    Adding DP_MIPI_FC1_L2_CONN with members MIPI_FC1_L2_CONN_P and MIPI_FC1_L2_CONN_N
    Adding DP_MIPI_FC1_L1_CONN with members MIPI_FC1_L1_CONN_P and MIPI_FC1_L1_CONN_N
    Adding DP_MIPI_FC1_L0_CONN with members MIPI_FC1_L0_CONN_P and MIPI_FC1_L0_CONN_N
    Adding DP_MIPI_FC1_CLK with members MIPI_FC1_CLK_P and MIPI_FC1_CLK_N
    Adding DP_MIPI_FC1_L3 with members MIPI_FC1_L3_P and MIPI_FC1_L3_N
    Adding DP_MIPI_FC1_L2 with members MIPI_FC1_L2_P and MIPI_FC1_L2_N
    Adding DP_MIPI_FC1_L1 with members MIPI_FC1_L1_P and MIPI_FC1_L1_N
    Adding DP_MIPI_FC1_L0 with members MIPI_FC1_L0_P and MIPI_FC1_L0_N
    Adding DP_MIPI_RC0_L3 with members MIPI_RC0_L3_P and MIPI_RC0_L3_N
    Adding DP_MIPI_RC0_CLK_CONN with members MIPI_RC0_CLK_CONN_P and MIPI_RC0_CLK_CONN_N
    Adding DP_MIPI_RC0_L3_CONN with members MIPI_RC0_L3_CONN_P and MIPI_RC0_L3_CONN_N
    Adding DP_MIPI_RC0_L1_CONN with members MIPI_RC0_L1_CONN_P and MIPI_RC0_L1_CONN_N
    Adding DP_MIPI_RC0_L1 with members MIPI_RC0_L1_P and MIPI_RC0_L1_N
    Adding DP_MIPI_RC0_L2_CONN with members MIPI_RC0_L2_CONN_P and MIPI_RC0_L2_CONN_N
    Adding DP_MIPI_RC0_L0 with members MIPI_RC0_L0_P and MIPI_RC0_L0_N
    Adding DP_MIPI_RC0_L0_CONN with members MIPI_RC0_L0_CONN_P and MIPI_RC0_L0_CONN_N
    Adding DP_MIPI_RC0_CLK with members MIPI_RC0_CLK_P and MIPI_RC0_CLK_N
    Adding DP_MIPI_RC0_L2 with members MIPI_RC0_L2_P and MIPI_RC0_L2_N

Ln 1, Col 1 | 100% | Windows (CRLF) | UTF-8
```

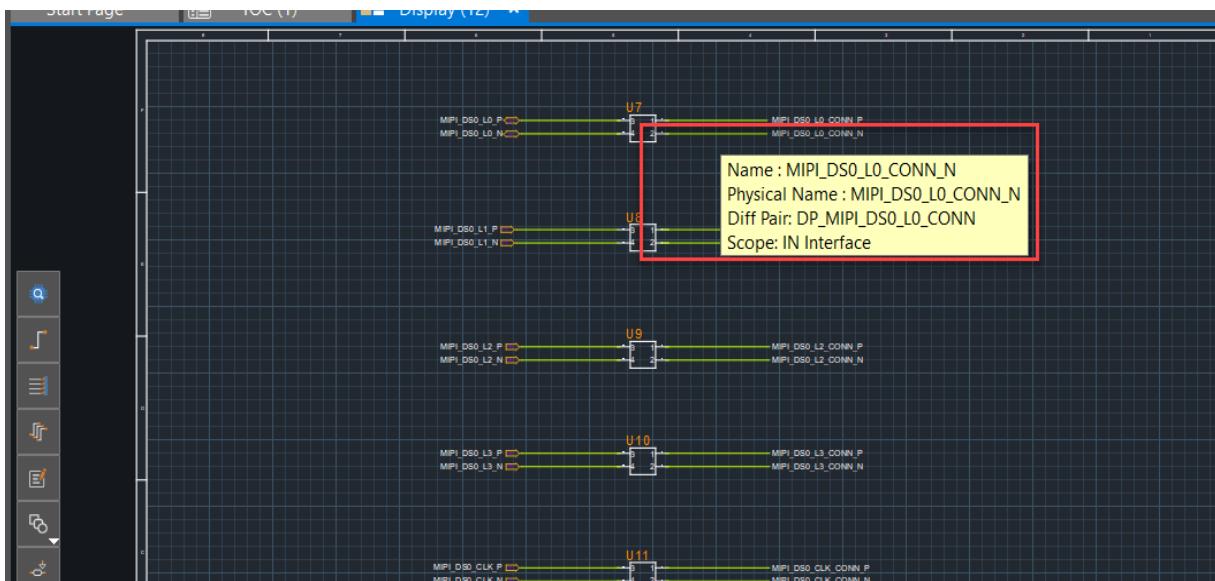
This file contains information on the pairs of nets which are made as differential pairs based on the default net name pattern in the configuration file, `acm_config.txt`.

4. Open any page of `ref_5G` design and hover the mouse pointer over the nets.

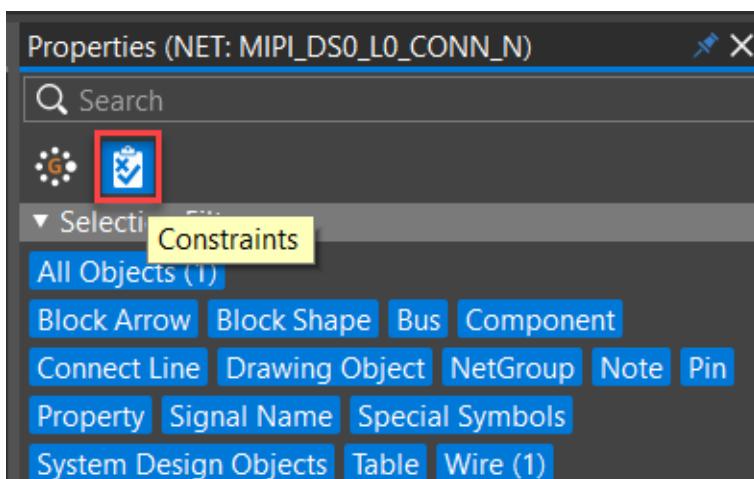
Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints

The tooltip reveals that the nets are now part of a differential pair. The differential pair name comprises a prefix, *DP_* and the common text part of the net names forming the rest of the name.



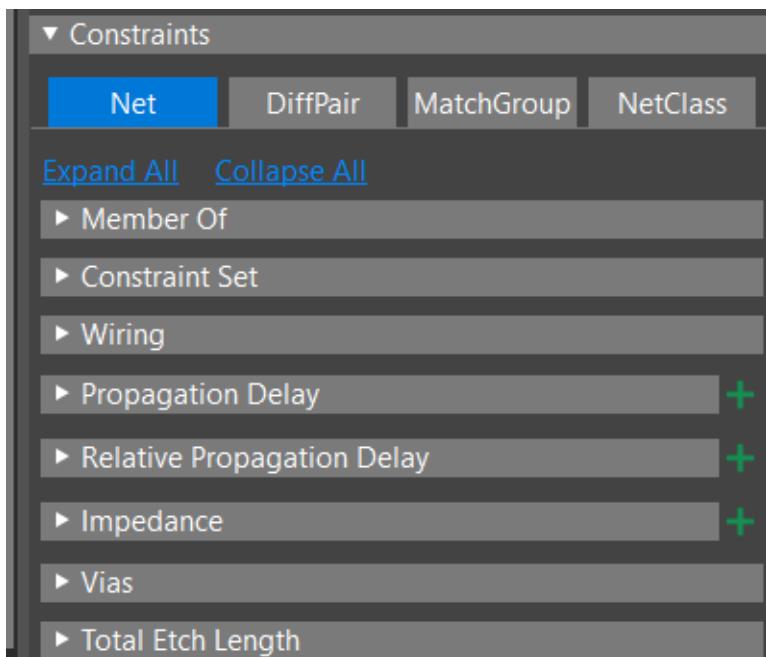
5. Navigate to the page, *Display(12)* of the design.
6. Click the net shown in the previous image.
7. Click the *Constraints* icon in the *Properties* panel.



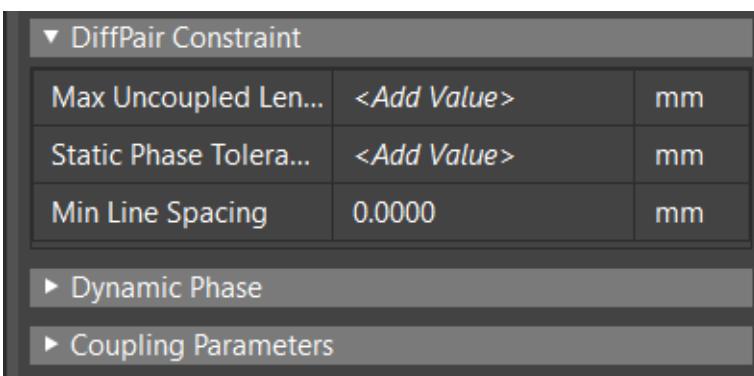
Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints

The docked Constraint Manager window is opened.



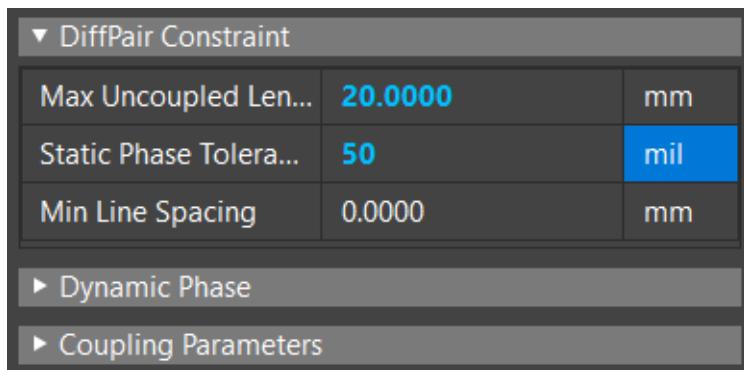
8. Click *DiffPair*.
9. Click *DiffPair Constraint*.



Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints

10. Specify the value for *Max Uncoupled Length* as 20 and *Static Phase Tolerance* as 50 mil.



These constraints will be visible on the differential pair in the Constraint Manager application as well.

Adding Constraints in Allegro Constraint Manager

To add constraints to net objects in Constraint Manager, follow these steps:

1. Choose *Electrical Analysis – Constraint Manager*.
2. In the *Worksheet Selector*, go to the *Electrical – Net – Routing – Differential Pair* spreadsheet.

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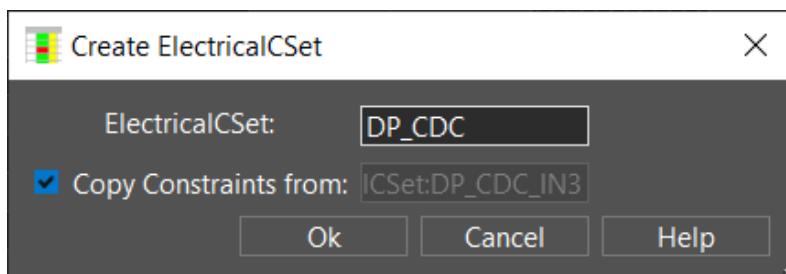
Setting Up Electrical Constraints

3. Navigate to the differential pair, DP_MIPI_DS0_L0_CONN.

Objects			Uncoupled Length					Static Phase
Type	S	Name	Length Ignored		Max	Actual	Margin	Tolerance
			mm	mm	mm	mm	mm	mm
*	*	*	*	*	*	*	*	*
Dsn		ref_5g						
Dsnl		► pwr (pwr)						
Bus		► GRFC8(1)						
Bus		► GRFC9(1)						
Bus		► N23(1)						
Bus		► N444						
Bus		► N464						
Bus		► N498						
Bus		► N660						
DPr		► DP_CDC_IN3						
DPr		► DP_ETDAC1						
DPr		► DP_MIPI_DS0_CLK						
DPr		► DP_MIPI_DS0_CLK_CONN						
DPr		► DP_MIPI_DS0_L0						
DPr		► DP_MIPI_DS0_L0_CONN		20.0000				50 mil
Net		► MIPI_DS0_L0_CONN_N		20.0000				50 mil
Net		► MIPI_DS0_L0_CONN_P		20.0000				50 mil
DPr		► DP_MIPI_DS0_L1						
DPr		► DP_MIPI_DS0_L1_CONN						

Notice that the constraints set in the docked Constraint Manager window are visible here. You will now create an ECSet and apply it on a differential pair.

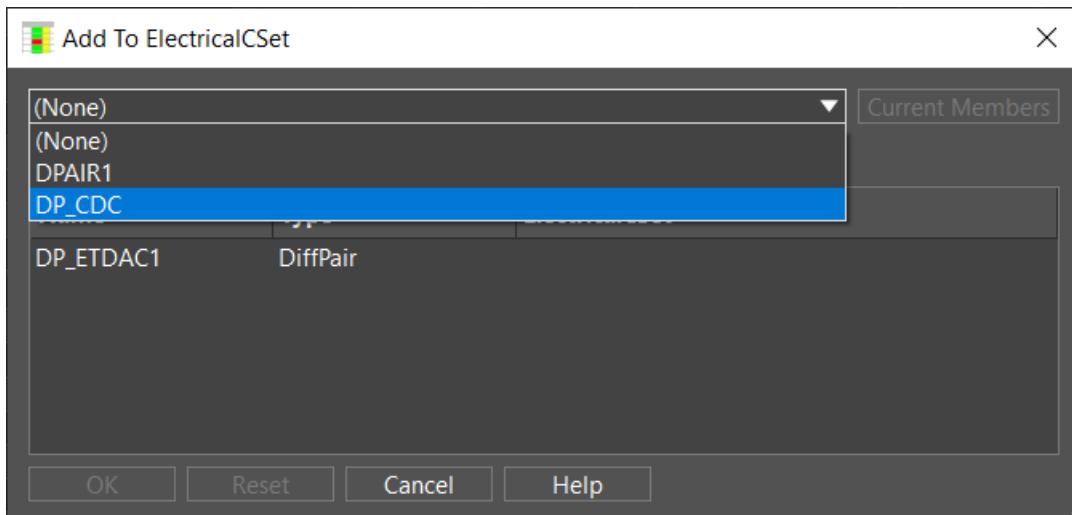
4. For differential pair, DP_CDC_IN3, specify the value for *Max Uncoupled Length* as 30 and *Static Phase Tolerance* as 70 mil.
5. Right-click DP_CDC_IN3 and choose *Create – ElectricalCSet*.
6. Specify *DP_CDC* as the name of the differential pair keeping the *Copy Constraints from* option enabled, and click *Ok*.



Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints

- Now right-click the differential pair, DP_ETDAC1 and choose *Constraint Set References*.



- Select DP_CDC from the list in the *Add To ElectricalCSet* dialog box and click *OK*.

The ECSet DP_CDC is applied to the differential pair, DP_ETDAC1 and it has inherited the constraint values for *Max Uncoupled Length* and *Static Phase Tolerance from the ECSet*.

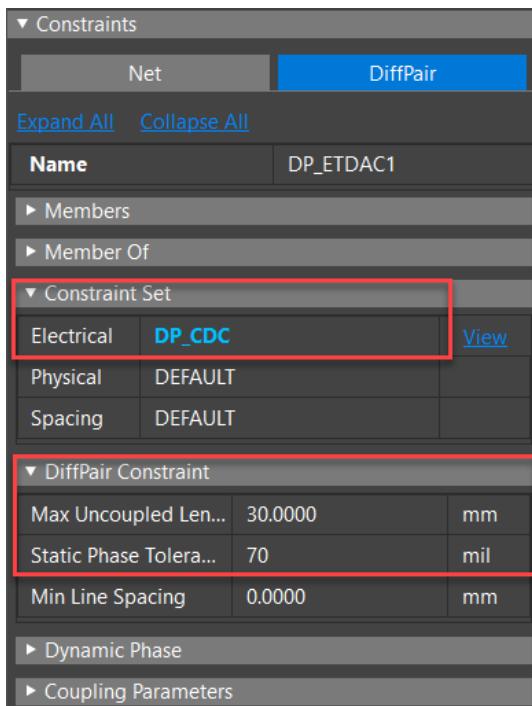
► DP_CDC_IN3					30.0000		70 mil
► DP_ETDAC1	DP_CDC				30.0000		70 mil
► DP_MIPI_DSO_CLK							
► DP_MIPI_DSO_CLK_CONN							

- Close Constraint Manager.
- In System Capture, search for DP_ETDAC1 in the schematic.
- Click the *Constraints* icon.

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints

Notice that the ECSet and the inherited constraint values are visible in the docked Constraint Manager window.



Creating ECSets in Topology Workbench

You can extract the extended nets or XNets in a design and view the topology in *Topology Workbench*. You can then define constraints in *Topology Workbench* as *ECSets* and apply the ECSets on net objects in Constraint Manager. The applied ECSets and constraints can be viewed in the docked Constraint Manager window in System Capture.

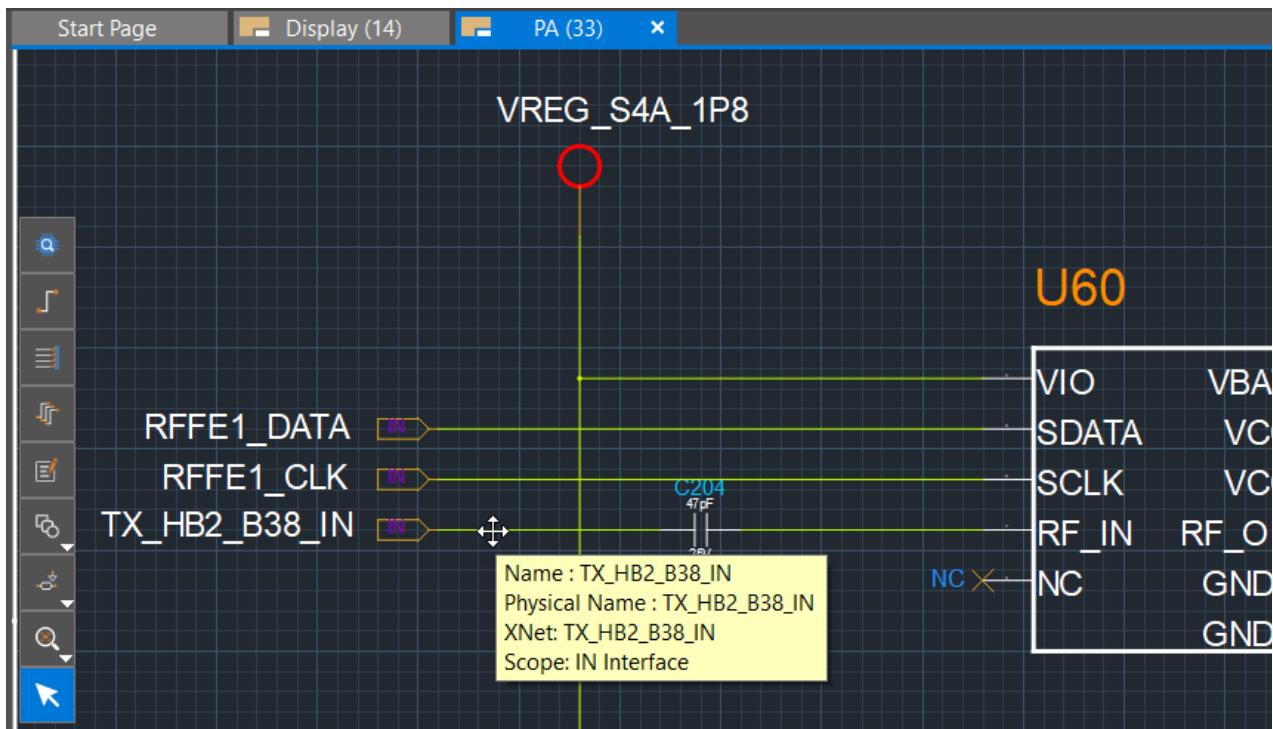
Extracting Topology in Topology Workbench

To extract a topology, follow these steps:

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints

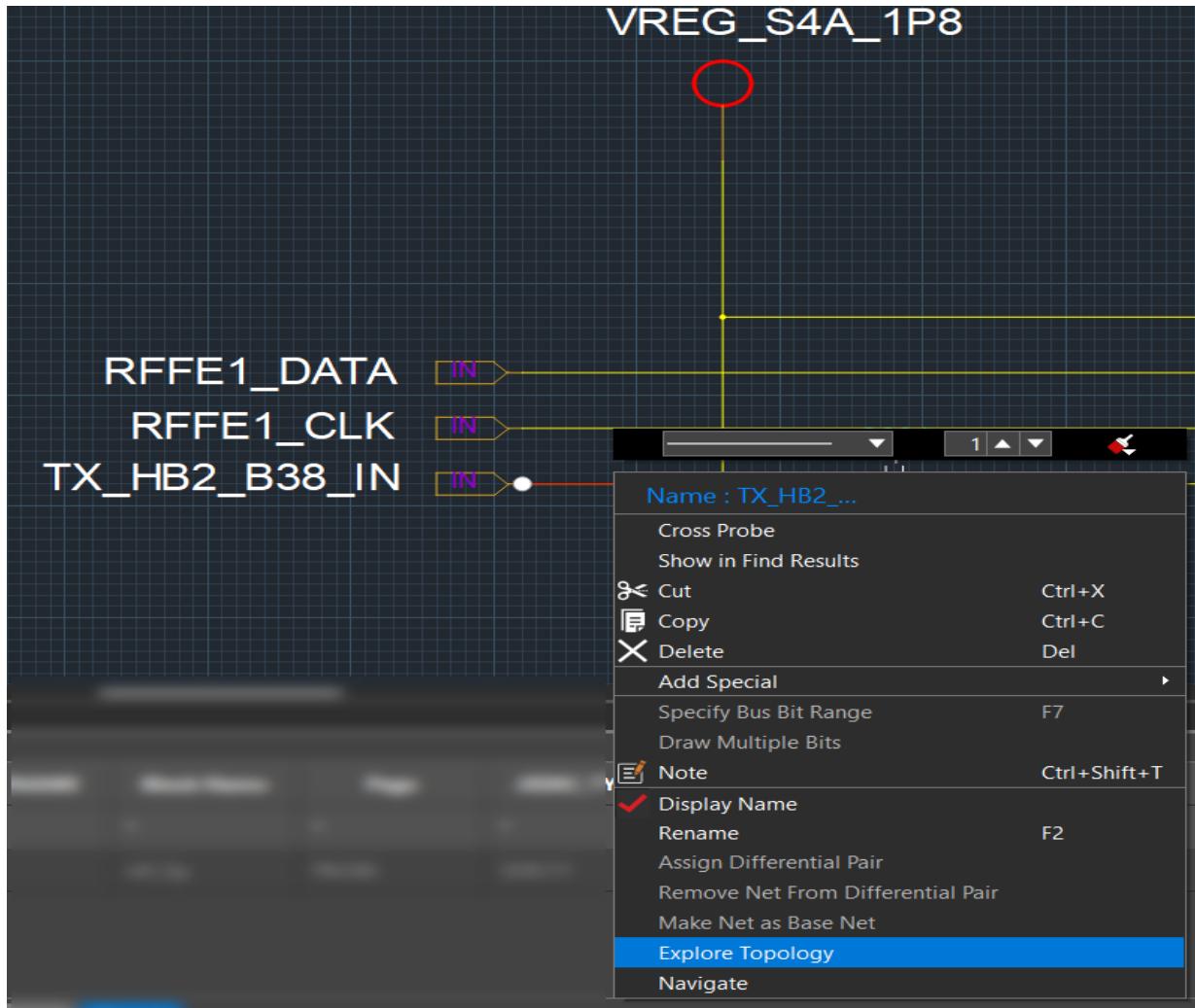
1. Navigate to page PA(33) and zoom in to the top left area and hover the mouse pointer over the net, TX_HB2_B38_IN as illustrated in the following image:



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Setting Up Electrical Constraints

- Right-click the wire and select *Explore Topology*.



The *Topology Workbench* window opens displaying the extracted net topology which can be used to define constraints.

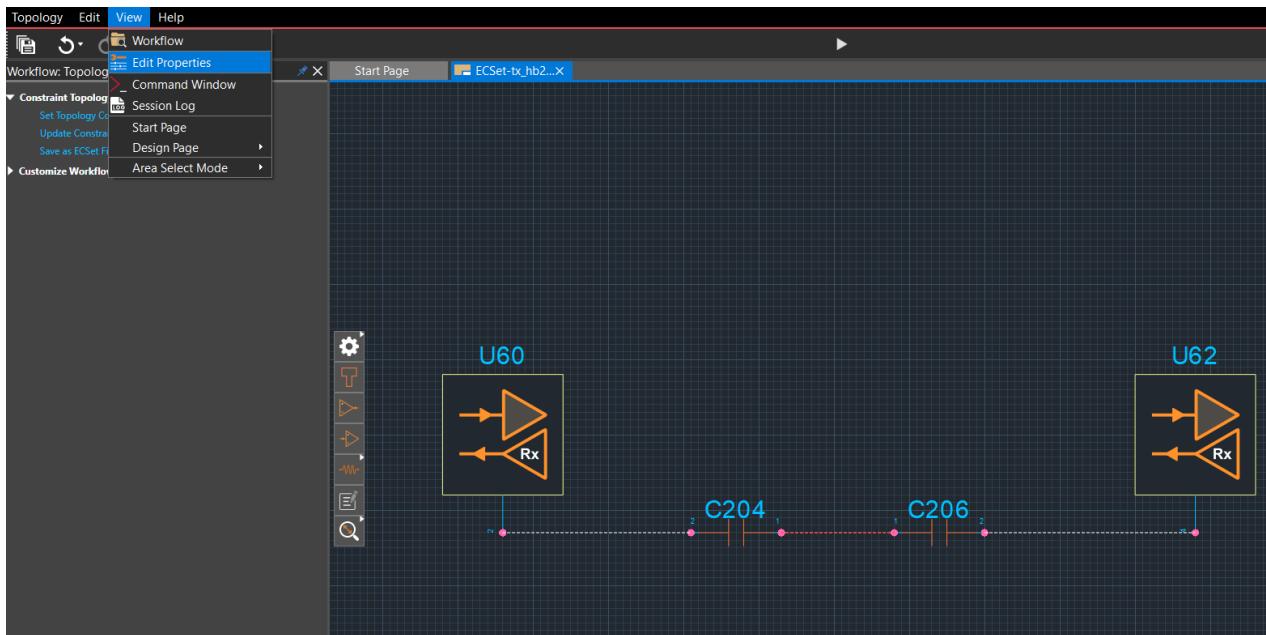
Defining Constraints in Topology Workbench

To define constraints on the extracted topology, follow these steps:

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Setting Up Electrical Constraints

1. Choose *View – Edit Properties*.

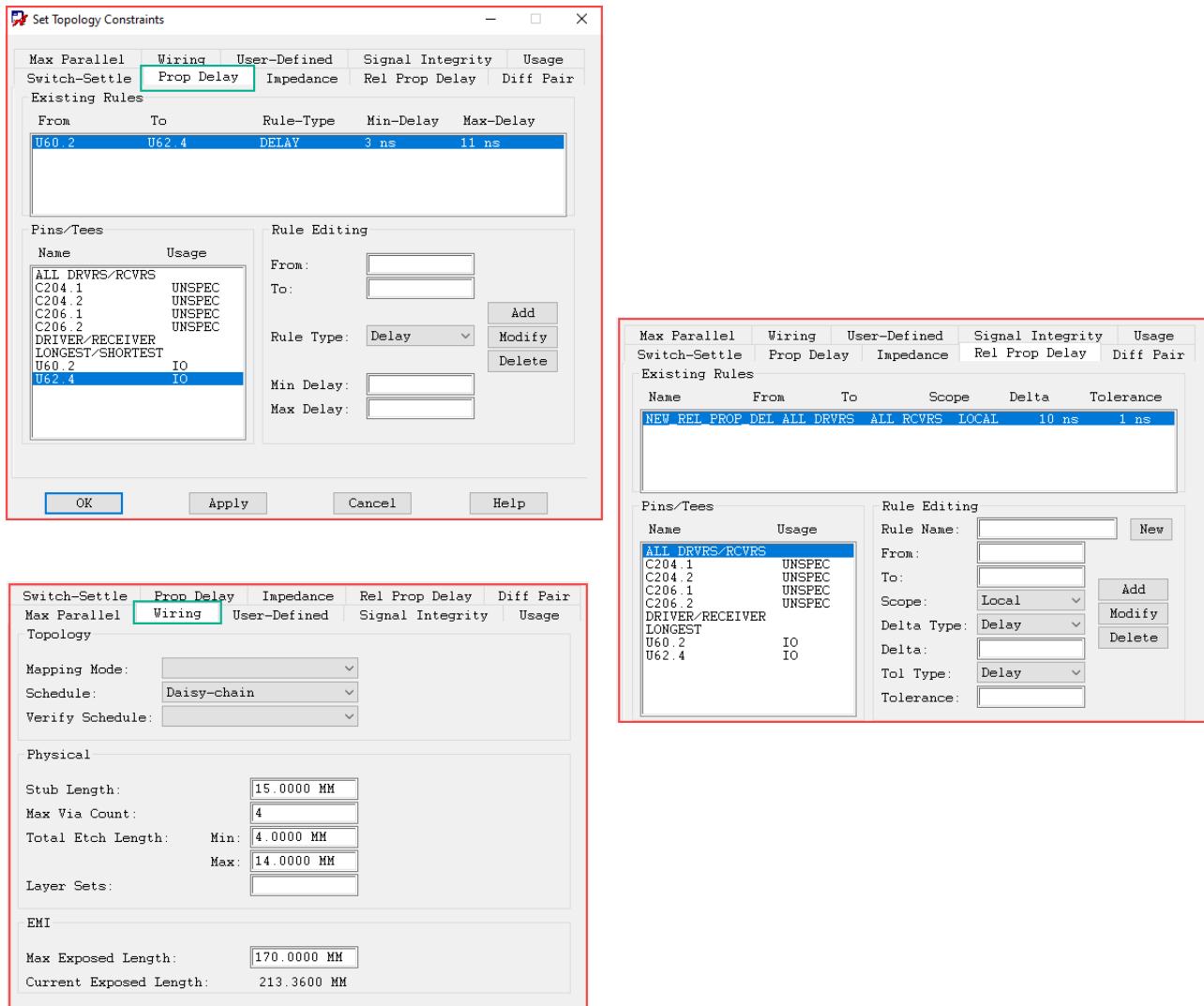


The *Properties* panel opens.

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints

- 2.** Change the values for *Propagation Delay*, *Relative Propagation Delay*, and *Wiring* in the respective tabs as illustrated in the following images.



- 3.** Choose *Constraint Topology – Update Constraint Manager*.

The Constraint Manager window opens. The information on applied ECSets is also displayed from a log file.

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints

- Click *Electrical Constraint Set* and traverse to the following spreadsheets to confirm that the ECSets created in *Topology Workbench* are propagated to Constraint Manager.

This screenshot shows the Allegro X Constraint Manager interface. The left sidebar under 'Electrical' routing includes 'Wiring', 'Vias', 'Impedance', 'Min/Max Propagation D...', 'Total Etch Length', 'Differential Pair', 'Relative Propagation Delay', and 'Return Path'. The 'Min/Max Propagation D...' item is highlighted with a red box. The main workspace displays a spreadsheet titled 'pwr ref_5g [R/W]'. The 'Objects' table has columns for Type, S, Name, Pin Pairs, Min Delay (mm), and Max Delay (mm). A row for 'ECSP' contains 'U60.2:U62.4' in the Pin Pairs column, with '3 ns' in the Min Delay and '11 ns' in the Max Delay.

Type	S	Name	Pin Pairs	Min Delay	Max Delay
				mm	mm
*	*	*	*	*	*
Dsn		ref_5g			
ECS		TX_HB2_B38_IN			
ECSP		U60.2:U62.4		3 ns	11 ns

This screenshot shows the Allegro X Constraint Manager interface. The left sidebar under 'Electrical' routing includes 'Wiring', 'Vias', 'Impedance', 'Min/Max Propagation D...', 'Total Etch Length', 'Differential Pair', 'Relative Propagation Delay', and 'Return Path'. The 'Relative Propagation Delay' item is highlighted with a red box. The main workspace displays a spreadsheet titled 'pwr ref_5g [R/W]'. The 'Objects' table has columns for Type, S, Name, Pin Pairs, Scope, and Delta:Tolerance (mm). A row for 'ECSP' contains 'NEW_REL_PROP_DEL' in the Pin Pairs column, with 'All Drivers/All Receivers' in the Scope and '10 ns:1 ns' in the Delta:Tolerance.

Type	S	Name	Pin Pairs	Scope	Delta:Tolerance
					mm
*	*	*	*	*	*
Dsn		ref_5g			
ECS		TX_HB2_B38_IN		All Drivers/All Receivers	10 ns:1 ns
ECSP		NEW_REL_PROP_DEL		Local	

This screenshot shows the Allegro X Constraint Manager interface. The left sidebar under 'Electrical' routing includes 'Wiring', 'Vias', 'Impedance', 'Min/Max Propagation D...', 'Total Etch Length', 'Differential Pair', 'Relative Propagation Delay', and 'Return Path'. The 'Wiring' item is highlighted with a blue box. The main workspace displays a spreadsheet titled 'pwr ref_5g [R/W]'. The 'Objects' table has columns for Type, S, Name, Verify Schedule, Schedule, Stub Length (mm), Max Exposed Length (mm), and Max Parallel. A row for 'ECSP' contains 'TX_HB2_B38_IN' in the Name column, with 'Daisy-chain' in the Verify Schedule, '15.0000' in the Stub Length, and '170.0000' in the Max Exposed Length.

Type	S	Name	Verify Schedule	Schedule	Stub Length	Max Exposed Length	Max Parallel
					mm	mm	
*	*	*	*	*	*	*	*
Dsn		ref_5g					
ECS		TX_HB2_B38_IN	Daisy-chain		15.0000	170.0000	
ECSP							

- Close *Constraint Manager*.

- Close *Topology Workbench*.

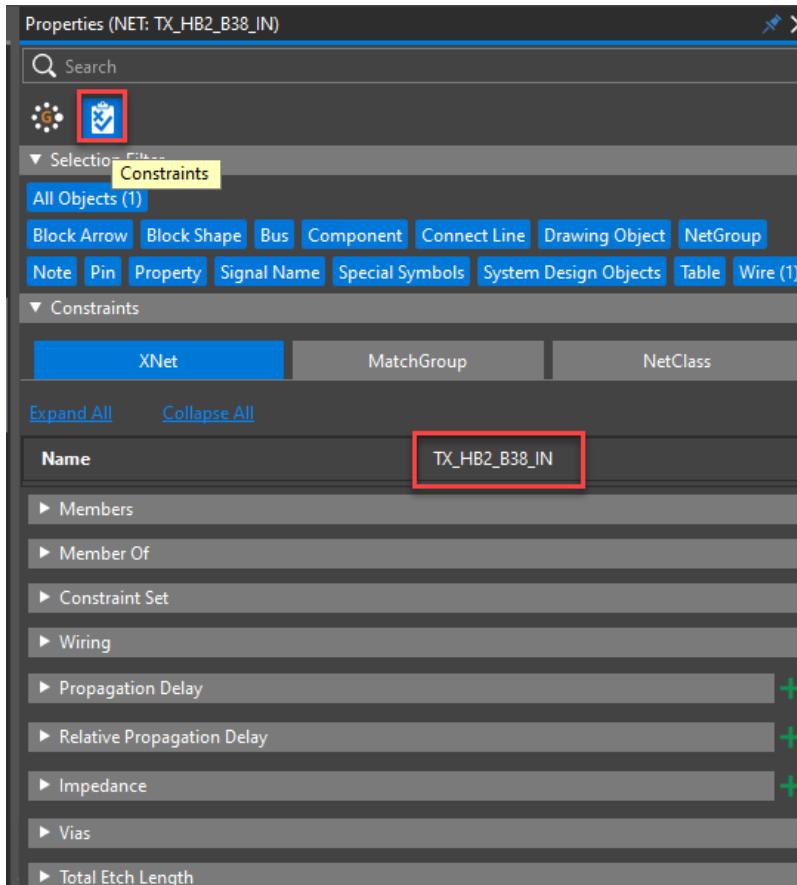
Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints

Viewing ECSets in Docked Constraint Manager

The applied constraints as well as the ECSets can also be viewed in the docked Constraint Manager window in System Capture.

1. In System Capture, ensure that the XNet *TX_HB2_B38_IN* is selected on the canvas.
2. In the *Properties* panel, click the *Constraints* icon and expand the Constraints list.



The docked Constraint Manager window is displayed for the selected XNet, *TX_HB2_B38_IN*.

3. Click *Expand All* to expand all the sections and view the constraints from the applied ECSet.

Allegro X System Capture - Schematic Sign Off Tutorial

Setting Up Electrical Constraints

The ECSet and all the constraint values from *Topology Workbench* are displayed.

The screenshot shows the ECSet configuration for a net named `_N48U`. The interface includes sections for Member Of, Constraint Set, Wiring, Propagation Delay, and Relative Propagation Delay. The wiring section is highlighted with a red border. The propagation delay section is also highlighted with a red border. The relative propagation delay section is also highlighted with a red border.

Member Of

Type	Parent Name
Electrical Class	<Add Value>
Physical Class	<Add Value>
Spacing Class	<Add Value>
Match Group	NEW_REL_PROP_DEL X

Constraint Set

Electrical	TX_HB2_B38_IN	View
Physical	DEFAULT	
Spacing	DEFAULT	

Wiring

Schedule	Daisy-chain
Verify Schedule	<Add Value>
Stub Length	15.0000 mm
Max Exposed Length	170.0000 mm

Propagation Delay

Pin 1	Pin 1 Delay ...	Pin 2	Pin 2 Delay ...	Min Delay ...	Max Delay ...
U60.2	0	U62.4	0	3 ns	11 ns

Relative Propagation Delay

Name	Pin 1	Pin 2	Scope	Delta (mm)	Tolerance (...)
NEW_REL_P...	AD	AR	Local	10 ns	1 ns

Managing Design Variants

Creating design variants is a critical step in the design cycle. A variant is an alteration or variation of the base PCB design. Almost all the electronics products have some variation, such as different RAM sizes or different supply voltages based on the geographical location. System Capture provides a robust solution to create and manage multiple variants of a design.

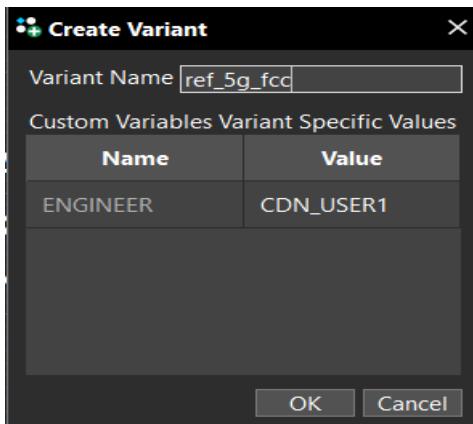
Creating a Design Variant

You need to create a Variant view of the base schematic, where you can modify the components and define the assembly variation for a specific customer, region, or any specific requirement.

To create a variant of the base design, follow these steps:

1. Choose *Variants – Create Variant*.
2. Click *Yes*, if prompted to save the design to continue.

The *Create Variant* dialog box is displayed.



3. Specify the name as *ref_5g_fcc* and click *OK*.

Allegro X System Capture - Schematic Sign Off Tutorial

Managing Design Variants

4. If prompted, click *Synchronize and Edit* to synchronize the variant database with the latest schematic changes.

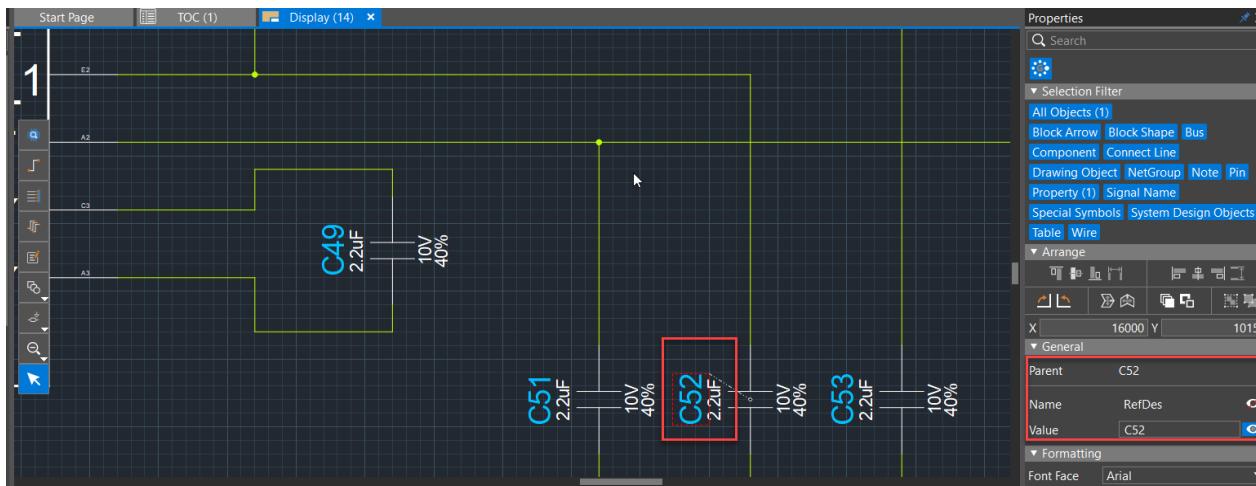
The tool switches to the Variant view for the variant, *REF_5G_FCC*, you just created. You can modify the variant data in this view.



Modifying Variant Data

After creating a variant, you can modify the part data for the variant. To do that, follow these steps:

1. Navigate to page *Display (14)* and select the capacitor C52.



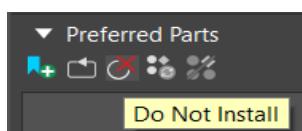
Allegro X System Capture - Schematic Sign Off Tutorial

Managing Design Variants

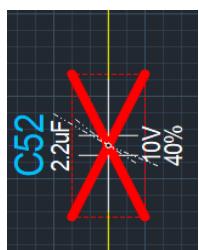
The *Variant Info* window opens on the right to display the properties of the selected component in the variant design.

Property	Base
CURRENT	CIMAX
DESCRIPTION	Capacitor X7R 50V 2.2n...
DIST	FLAT
HEIGHT	0.9mm
IC	UNDEF
Footprint	201C
KNEE	CBMAX
MANUFACTURER	AVX
MAX_TEMP	125
MDN	00000000000000000000000000000000

- Click the *Do Not Install* icon to skip including this capacitor in the variant.



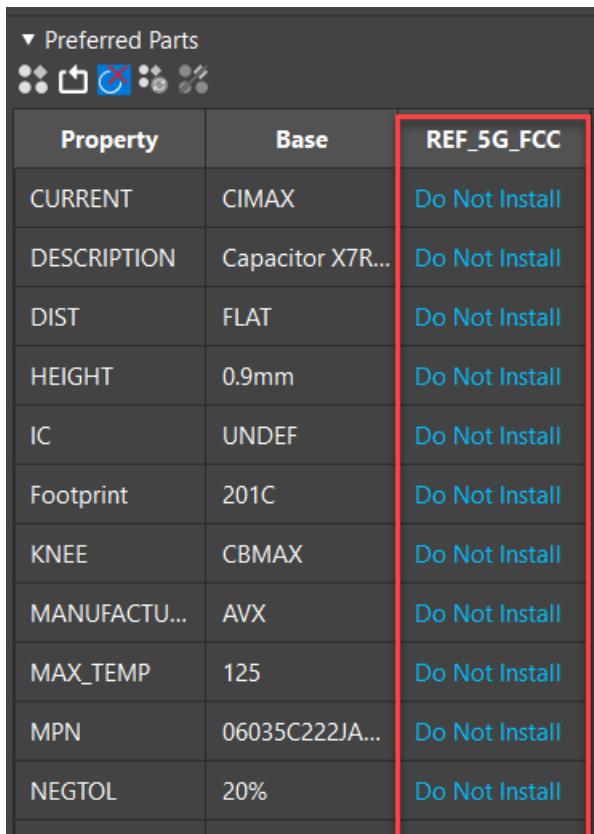
Notice that a cross mark appears across the component indicating that the selected capacitor is not to be included in the assembly for this variant.



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Managing Design Variants

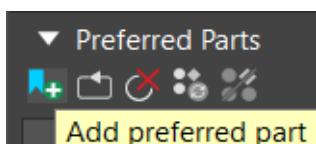
Also notice that a new column is added for the variant alongside the *Base* column for the component, showing its status as *Do Not Install*.



Property	Base	REF_5G_FCC
CURRENT	CIMAX	Do Not Install
DESCRIPTION	Capacitor X7R...	Do Not Install
DIST	FLAT	Do Not Install
HEIGHT	0.9mm	Do Not Install
IC	UNDEF	Do Not Install
Footprint	201C	Do Not Install
KNEE	CBMAX	Do Not Install
MANUFACTU...	AVX	Do Not Install
MAX_TEMP	125	Do Not Install
MPN	06035C222JA...	Do Not Install
NEG TOL	20%	Do Not Install

You will now replace a component in the base design with another component for use in this variant.

3. Navigate to the page, *Display(15)* and select the resistor, R15.
4. To specify the replacement part, click the *Add preferred part* icon.

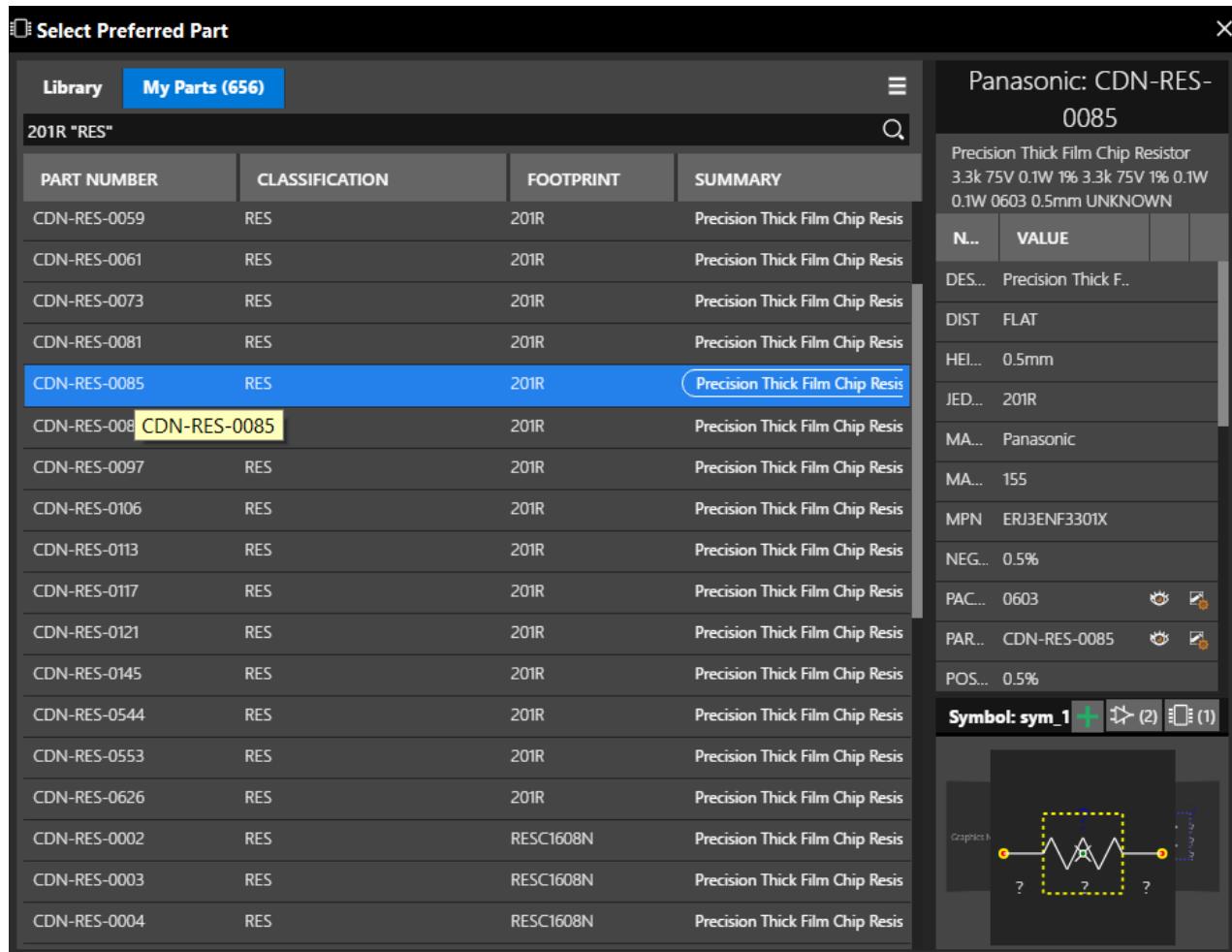


5. Click *Skip* if prompted to sign in to the providers libraries.

Allegro X System Capture - Schematic Sign Off Tutorial

Managing Design Variants

6. In the *Select Preferred Part* dialog box, search for a part that has the same or a compatible footprint, 201R in this case.



7. Right-click *CDN-RES-0085* and choose *Add*. Alternatively, you can double-click the component to add it.

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Managing Design Variants

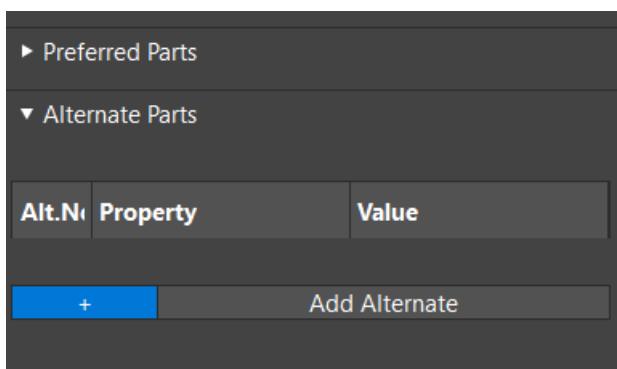
The component on the canvas is replaced with the preferred part for the variant. The properties of the preferred part are now displayed in the *Variant Info* window.



Property	Base	REF_5G_FCC
DESCRIPTION	Precision Thic...	Precision Thic...
DIST	FLAT	FLAT
HEIGHT	0.5mm	0.5mm
Footprint	201R	201R
MANUFACTU...	Panasonic	Panasonic
MAX_TEMP	155	155
MPN	ERJ3ENF0010X	ERJ3ENF3301X
NEG TOL	5%	0.5%
PACK_TYPE	0603	0603
PART_NUMBER	CDN-RES-0001	CDN-RES-0085
POSTOL	5%	0.5%

You can also add an alternate part for a variant. An alternate part is used when the preferred part is not available. If both are available, the preferred part gets priority over the alternate part.

- Click the + icon under the Alternate Parts section to add an alternate part.



- In the *Select Alternate Part* dialog box, double-click *CDN-RES-0081*.

Allegro X System Capture - Schematic Sign Off Tutorial

Managing Design Variants

The selected part is added to the list of alternate parts.

▼ Alternate Parts		
Alt.No	Property	Value
► 01	PART_NUMBER	CDN-RES-0081
+		Add Alternate

10. Choose *Variants – View – Off* to switch off the Variant view.
11. Create another variant and name it *ref_5g_fcc_a*.
12. Choose *Variants – View – Off*.

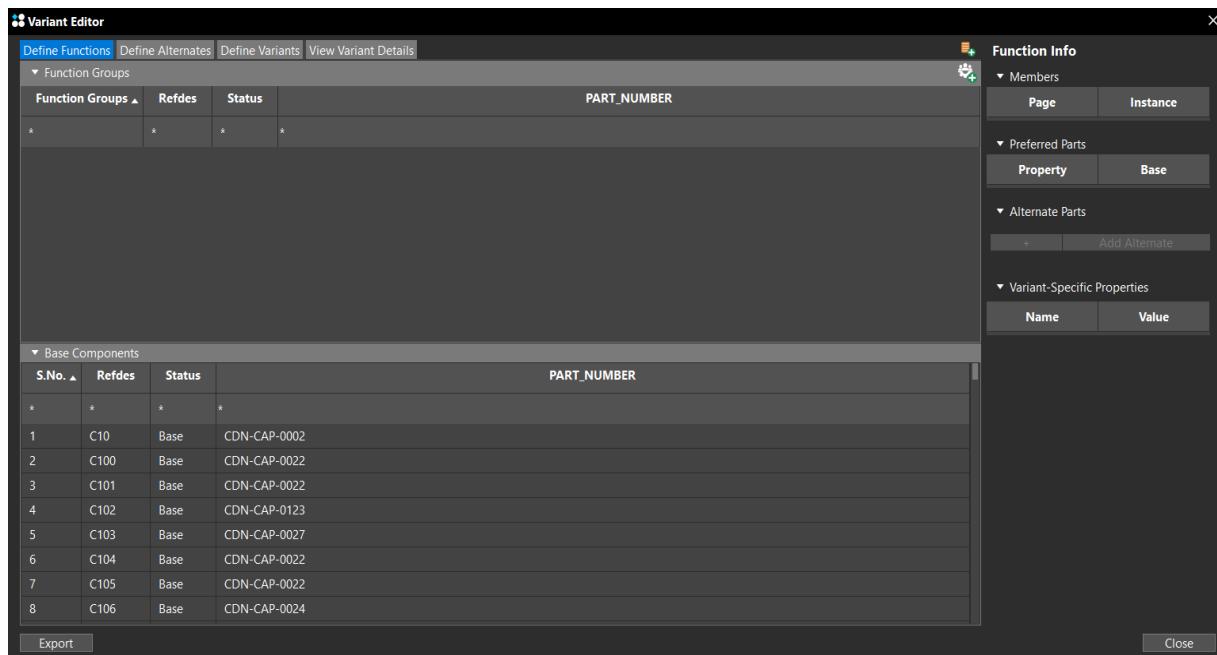
Managing Variants from Variant Editor

The *Variant Editor* window provides a single view to display information about all the objects and variants of a design. You can also perform operations, such as replacing parts with preferred parts, adding alternate parts, or marking components as *Do Not Install* in this interface.

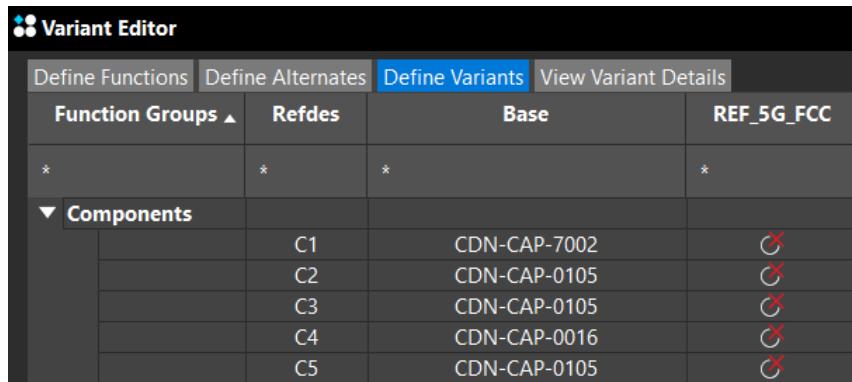
Allegro X System Capture - Schematic Sign Off Tutorial

Managing Design Variants

1. Choose *Variants – Variant Editor*.



2. Mark parts *C1* to *C5* as *Do Not Install* for the *REF_5G_FCC* variant, by choosing *Do Not Install* from the shortcut menu in the *REF_5G_FCC* column.



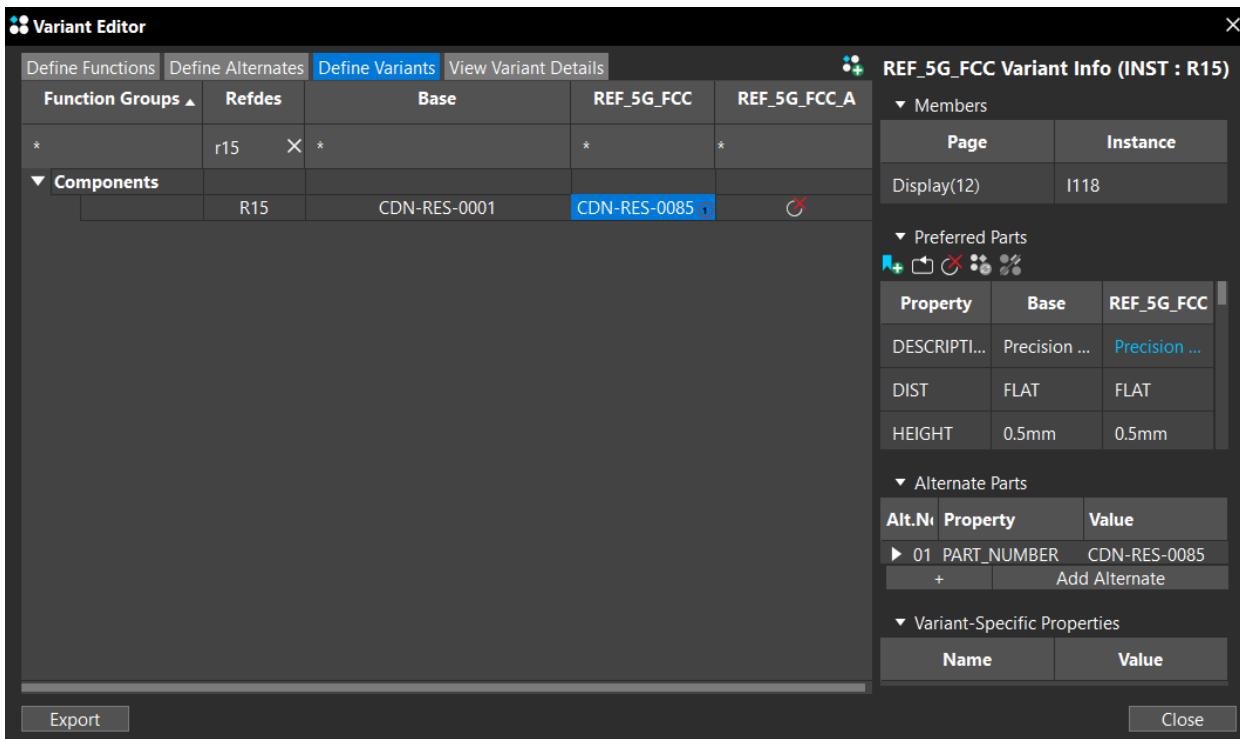
3. Next, search for the component, *R15*.

4. Click the corresponding part name under the variant, *REF_5G_FCC*.

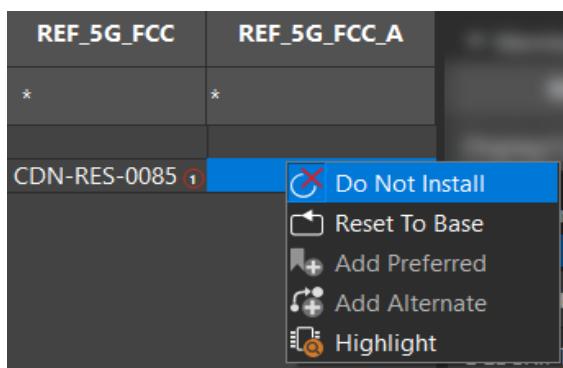
Allegro X System Capture - Schematic Sign Off Tutorial

Managing Design Variants

All the properties associated with the part are displayed in the *Properties* panel. The properties with changed values are displayed in blue to highlight the change. The alternate part information is also displayed.



5. Select this part under the variant, REF_5G_FCCA.
6. Right-click and choose *Do Not Install*.



This part will not be included in the variant, REF_5G_FCCA.

Exporting Variant Data

You can also export variant data into a .csv file. To export variant data, follow these steps:

1. In the *Variant Editor* window, click *View Variant Details* tab.
2. Click *Export*.
3. Specify *Var_Data* as the file name.
4. Click *Save* in the *Specify Export CSV File* dialog box.

The Variant Operations message box confirms the location of the file. The data for all the variants of the design is now exported into the .csv file.

5. Close the *Variant Editor* window and save the design.

Managing Bill of Materials

Generating the Bill of Materials (BOM) file is another crucial aspect of designing. A BOM report lists all the components used in a design along with the part numbers and the values of the properties of each component.

The *Live BOM* feature of System Capture presents a real-time view of the design BOM with minimal configuration. It also incorporates all the variants of the design so that you can quickly toggle between the Variants and the Base schematic BOM.

Generating a BOM Report

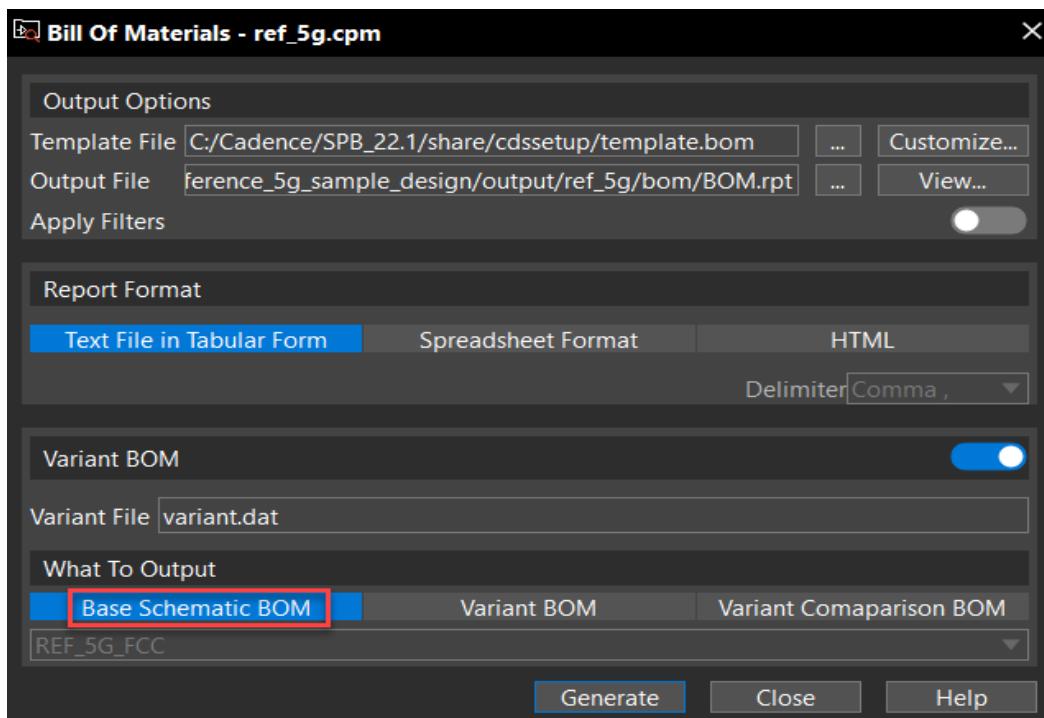
To generate a traditional BOM report in System Capture, follow these steps:

1. Choose *Tools – Generate BOM*.

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Managing Bill of Materials

The physical netlist is generated and the *Bill of Materials* dialog box is displayed for the design. You can configure the settings, such as choosing a specific template or the report format.



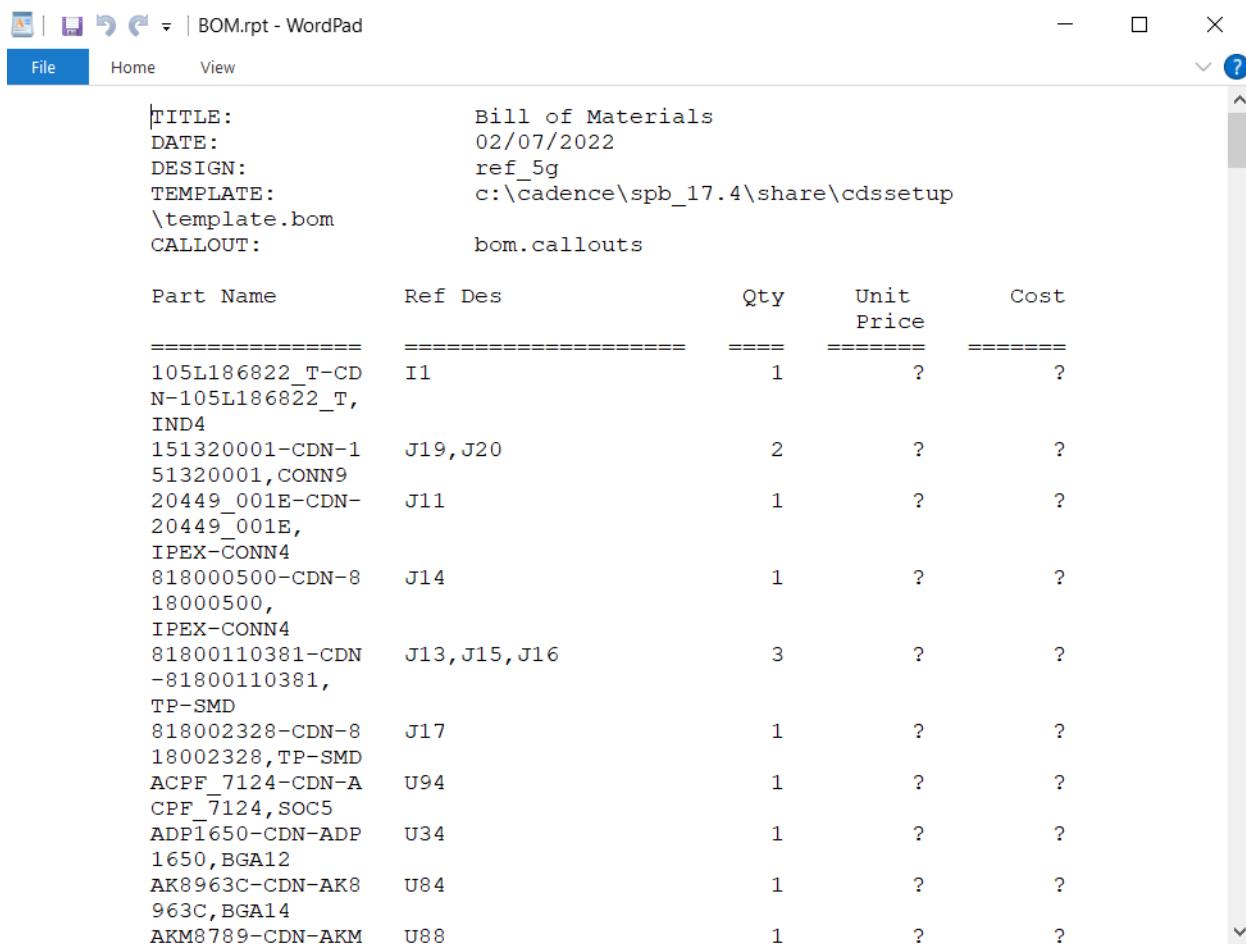
2. Click *Generate*.

By default, the BOM report for the base schematic is generated.

Allegro X System Capture - Schematic Sign Off Tutorial

Managing Bill of Materials

3. Click Yes to view the report.



The screenshot shows a Microsoft WordPad window titled "BOM.rpt - WordPad". The window contains a "Bill of Materials" report with the following details:

Header Information:

- TITLE: Bill of Materials
- DATE: 02/07/2022
- DESIGN: ref_5g
- TEMPLATE: c:\cadence\spb_17.4\share\cdssetup\template.bom
- CALLOUT: bom.callouts

Table Headers:

Part Name	Ref Des	Qty	Unit Price	Cost
-----------	---------	-----	------------	------

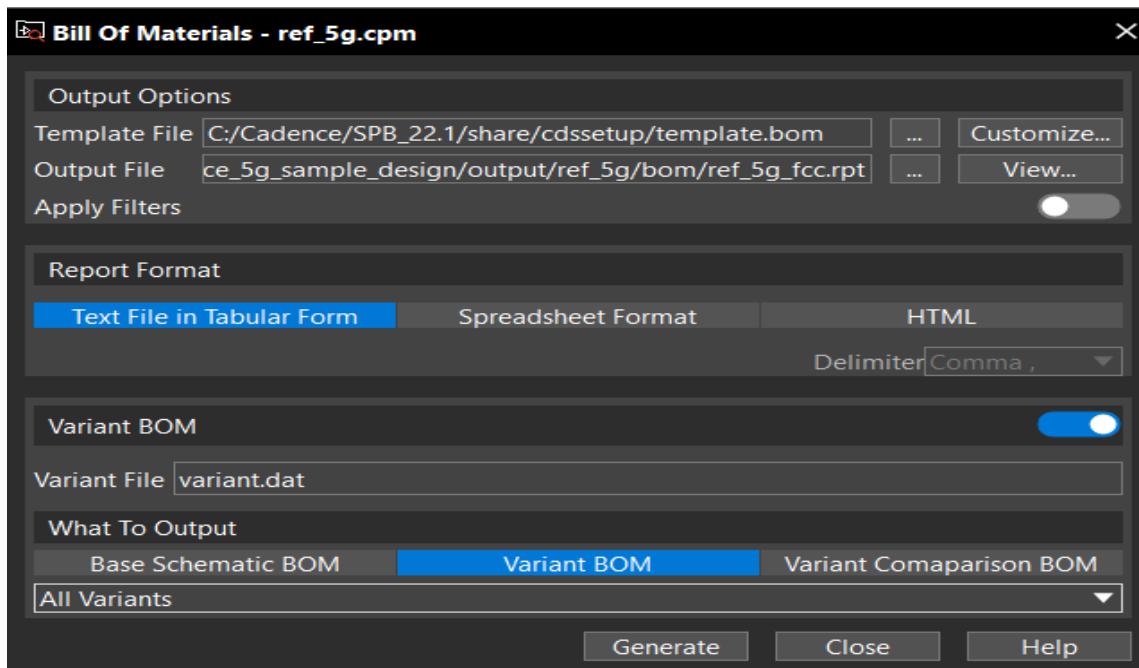
Table Data:

105L186822_T-CDN N-105L186822_T, IND4	J11	1	?	?
151320001-CDN-1 51320001,CONN9	J19,J20	2	?	?
20449_001E-CDN- 20449_001E, IPEX-CONN4	J11	1	?	?
818000500-CDN-8 18000500, IPEX-CONN4	J14	1	?	?
81800110381-CDN -81800110381, TP-SMD	J13,J15,J16	3	?	?
818002328-CDN-8 18002328,TP-SMD	J17	1	?	?
ACPF_7124-CDN-A CPF_7124,SOC5	U94	1	?	?
ADP1650-CDN-ADP 1650,BGA12	U34	1	?	?
AK8963C-CDN-AK8 963C,BGA14	U84	1	?	?
AKM8789-CDN-AKM	U88	1	?	?

Allegro X System Capture - Schematic Sign Off Tutorial

Managing Bill of Materials

Similarly, you can generate a report for a specific variant or for all the variants.

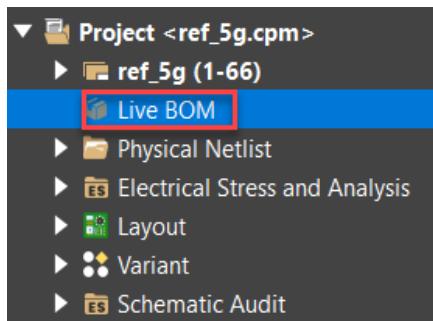


- Click *Close* to dismiss the *Bill of materials* dialog box.

Viewing Live BOM

To view Live BOM for a design, follow these steps:

- Open the *Project Explorer* panel and double-click *Live BOM*.



Live BOM for the design is displayed.

Note: If you do not see *Live BOM* in the *Project Explorer* panel, click the *Project*

Allegro X System Capture - Schematic Sign Off Tutorial

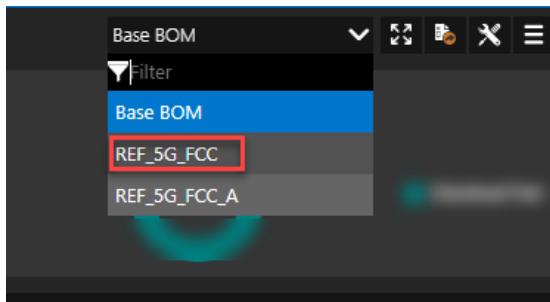
Managing Bill of Materials

Explorer Settings icon and choose *Live BOM* from the displayed list.

Live BOM								
155 UNIQUE PARTS			2 MPNs			PART STATUS		PART TYPE
892 PARTS			1 MANUFACTURERS					Electrical Part
<input type="text"/> Search								
T	S	PART NUMBER	QTY	UNUSED	REFDES	UNIT PRICE	VALUE	DESCRIPTION
		CDN-105L186822_T	1	0	J1		-	
		CDN-151320001	2	0	J19,J20			SIM SLOT CONNECTOR
		CDN-20449_001E	1	0	J11		-	
		CDN-818000500	1	0	J14		-	
		CDN-81800110381	3	0	J13,J15,J16		-	
		CDN-818002328	1	0	J17		-	
		CDN-ACPF_7124	1	0	U94			WLAN (2.4G)
		CDN-ADP1650	1	0	U34			LED FLASH
		CDN-AK8963C	1	0	U84			COMPASS SENSOR
		CDN-AKM8789	1	0	U88		-	
		CDN-ANT1400	1	0	J12			GPS ANTENNA

Live BOM displays the total number of parts and unique parts used in the design. Notice that this BOM is for the base schematic.

2. Switch to the Live BOM for the *REF_5G_FCC* variant from the drop-down list at the top-right corner.



Allegro X System Capture - Schematic Sign Off Tutorial

Managing Bill of Materials

The BOM for the selected variant is displayed. Notice that total number of parts and the number of unique parts has changed according to the variant REF_5G_FCC.

The screenshot shows the 'Live BOM' interface in Allegro X. At the top, there are four summary boxes: '154 UNIQUE PARTS' (highlighted with a red border), '3 MPNs', '2 MANUFACTURERS', and 'PART STATUS' (a donut chart with a small red segment). Below these is a 'PART TYPE' section with a teal circle icon and a legend for 'Electrical Part' and 'Preferred Part'. A search bar labeled 'Search' is followed by a table with columns: T, S, PART NUMBER, QTY, UNUSED, REFDES, UNIT PRICE, VALUE, and DESCRIPTION. The table lists ten parts, all of which are electrical components:

T	S	PART NUMBER	QTY	UNUSED	REFDES	UNIT PRICE	VALUE	DESCRIPTION
		CDN-105L186822_T	1	0	J11		-	
		CDN-151320001	2	0	J19,J20			SIM SLOT CONNECTOR
		CDN-20449_001E	1	0	J11		-	
		CDN-818000500	1	0	J14		-	
		CDN-81800110381	3	0	J13,J15,J16		-	
		CDN-818002328	1	0	J17		-	
		CDN-ACPF_7124	1	0	U94			WLAN (2.4G)
		CDN-ADP1650	1	0	U34			LED FLASH
		CDN-AK8963C	1	0	U84			COMPASS SENSOR
		CDN-AKM8789	1	0	U88		-	
		CDN-ANT1400	1	0	J12			GPS ANTENNA