cadence®

OrCAD® X Capture CIS Known Problems and Solutions, Release 23.1

Product Version 23.1
September 2023

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Contents

Known Problems and Solutions in OrCAD X Capture CIS Release 23.1

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This Known Problems and Solutions document describes important Cadence Change Requests (CCRs) for OrCAD X Capture CIS and tells you how to solve or work around these problems.

Important: Only known problems and solutions available at release time are available in this document.

CCMPR2874465: Node-based features, such as Symphony server and LiveDoc are not working for longer mapped hierarchy paths

Description: When accessing node-based applications, such as LiveDoc, Symphony server, and so on from a mapped hierarchy, if the number of characters in the fully qualified file name is greater than or equal to `260` characters or the directory name is greater than or equal to `248` characters, the following error occurs:

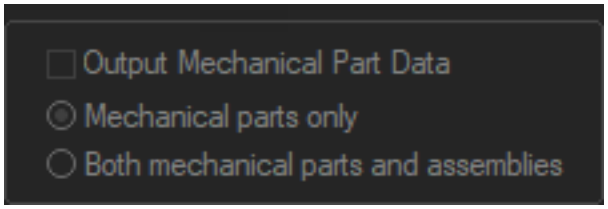
```
332: Error: EISDIR: illegal operation on a directory, lstat 'm:\'

OrNodeJSThread::ReportException532332:Error: EISDIR: illegal
operation on a directory, lstat 'm:\' throw err;
```

Workaround: Use the reduced hierarchy path for the applications to work.

CCMPR2830074: Mechanical part support in CIS BOM is missing in the OrCAD X Cloud flow

Description: The Mechanical parts section in the CIS BOM user interface is disabled in the OrCAD X Cloud flow. Therefore, mechanical parts are not included in the output BOM.

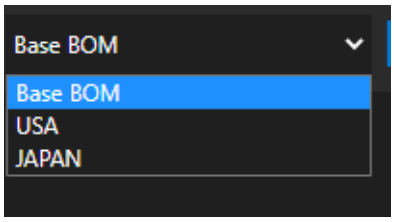


Solution: None.

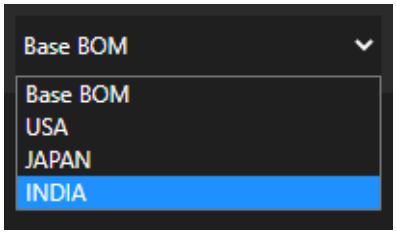
CCMPR2868425: With Live BOM tab opened, variant info is not loaded if variant of a dsn is created and saved (seen after reopening tab)

Description: If the *Live BOM* tab is opened and a new variant is added to the design from Part Manager, even after saving the design and refreshing the Live BOM data, the new variant name does not appear in the BOM selection list.

For example, if you add a new variant, *INDIA*, with the *Live BOM* tab already opened, the new variant does not show in the list of variants as illustrated in the following image:



Solution: Close the *Live BOM* tab and reopen it to view the updated BOM selection list. Also, before adding a new variant, ensure that the *Live BOM* tab is closed.



CCMPR2867694: Open a project, add it to workspace, and create new simulation profile, the Simulation Settings dialog box stops responding.

Description: The CCR is concerned with the following two issues:

Issue 1: If you add a local (non-Cloud workspace) project to the workspace using the *Add to Workspace* command and try to create a new simulation profile, the *Simulation Settings* dialog box stops responding to button actions, such as *OK* and *Cancel*. After you close the dialog box and try to run the simulation, the following netlisting related error messages are flagged:

```
INFO(ORNET-1041): Writing PSpice Flat Netlist .\

Cannot remove file .\

ERROR(ORNET-1163): Unable to create netlist file.
```

Issue 2: Capture stops responding if you run the *Save Project As* command in a new project to save the project to any location, and try to create a new simulation profile.

Solution: None.

Problem: Revision information is not available for a project, which is not stored directly under the *projects* folder in the workspace area.

Description: In the Cloud workspace, all the projects are created and stored in a flat structure under the *projects* folder. For example:

```
%HOME%\cdssetup\workspace\projects\benchproj
```

You can create a nested folder structure in (Windows) File Browser by creating a new folder in the *projects* folder and moving a project folder under the new folder. For example:

```
%HOME%\cdssetup\workspace\projects\new_project\benchproj
```

In OrCAD X Capture, the nested folder structure appears in the *File Manager* window and you can publish the project in the nested folder structure. However, the revision information is not retained for such projects.

Solution: To maintain the revision information for a project, ensure that the project is directly under the *projects* folder in the workspace area.

Related CCR: CCMPR2861382: New projects are always created in a flat structure under the projects folder.

Known Problems and Solutions in Older Capture CIS Releases

CCR 2701383: Right side panel of Unified CIS tab goes blank when a single MPN linked to a component is deleted.

Description: If you delete the only MPN linked to a component, the right pane displaying the properties of the selected component goes blank.

Solution: To view the properties of the component, select another component from the list and then click the previous component again.

CCR 2706786: On Japanese OS machines, there are issues in creating component or category when Japanese script characters are used in description or properties.

Description: When a component is created with Japanese script characters in its description or property name, each Japanese script character is replaced with the '?' character in the workspace. When placed on the schematic, the annotated properties also display the '?' characters. Similar issue exists while creating a category or linking an MPN to a selected component using Japanese script characters.

Solution: Currently, OrCAD X is not supported on Japanese OS.

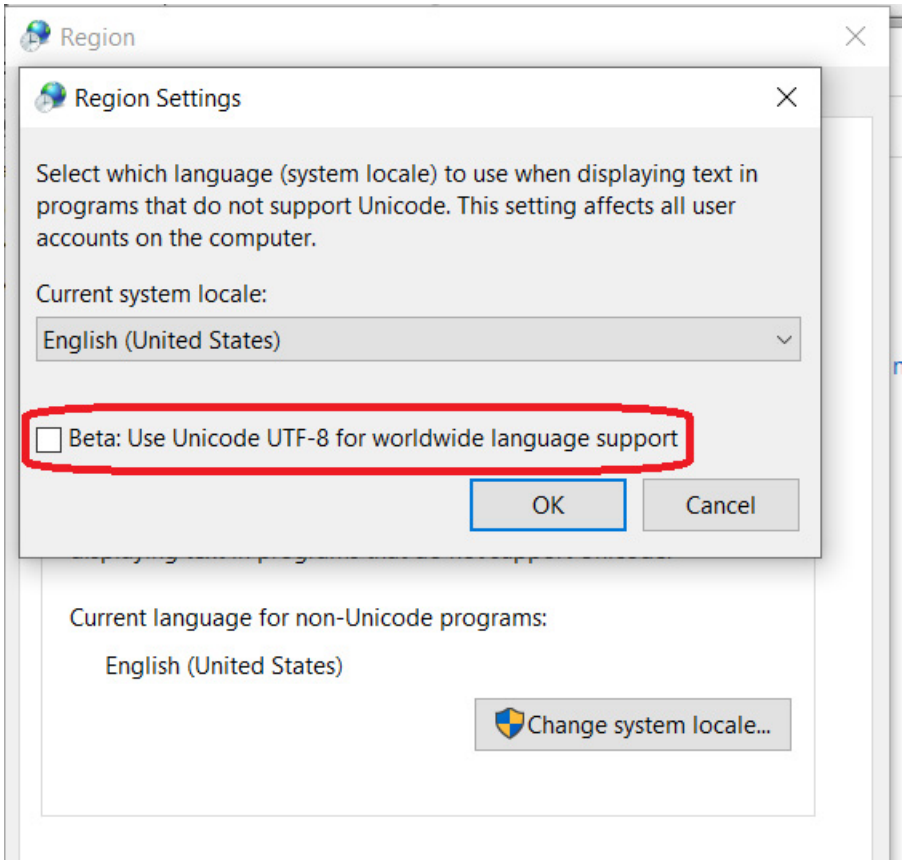
CCMPR02203550: Tcl HTML scripts slow

Description: A Tcl HTML script is slow in release 17.4-2019 of OrCAD Capture. The same script works smoothly and faster in release 17.2-2016.

Solution: Users working with European languages are experiencing the slowing of Tcl HTML scripts because of a bug in Windows.

For problem details, see the *discussion thread* on Microsoft site, and *here*.

Besides the resolutions listed at the Microsoft site, in some Windows 10 systems selecting *Beta: Use Unicode UTF-8 for worldwide language support* in *Region Settings* also helps resolve the issue.



It is recommended that you analyze any affect on other applications before selecting the option.

CCR 2148936: CIS configuration menu is not available on launching Capture CIS.

Description: Open Capture CIS and click the *Options* menu. The *CIS Configuration* menu option is not available.

Solution: Open any project. You can see this menu option in the *Options* menu when accessed from an active project.

CCMPR02131483: Design Sync fails with an error message in OrCAD Capture if components are deleted

Description: If you choose *PCB – Design Sync* in OrCAD Capture to backannotate a layout to the open schematic, the operation fails with an error message (ORCAD-36057) regarding the design name not matching if you deleted any components.

Solution: The backannotation process fails because the deletion of components is not supported in the Design Sync flow.

CCMPR02046845: XNet rename is not working with Allegro CIS license

Description: You cannot rename an XNet if you are using the Capture-Constraint Manager flow with the Allegro CIS license.

Solution: This feature is not supported yet.

CCR 1144603: Update-Refresh symbol from Libs menu does not update status for a deleted library part.

Description: If a library part used in the design is deleted from the library, then *Refresh Symbols From Libs* command will not update the library in the same session with the modified part list.

Solution: Re-launch Capture CIS.

CCR 604015: On closing Part Manager, design and Project Manager are closed.

Description: If Part manager is in docked stated and user closes by right-clicking and choosing *Close*, Project Manager and the open design are also closed.

Solution: Close Project Manager by clicking the Close button.

Allegro PCB Editor does not honor changed components in the assembly drawing variants.

Description: In Capture CIS, you can create variants such that some components of the base design

- do not appear in the variant (Part not Present)
- appear with changed values for some properties.

This information about variants can be exported to the variants.lst file for Allegro PCB Editor to view assembly drawings. Parts not present in a variant are handled properly in an Allegro PCB Editor assembly drawing. However, Allegro PCB Editor does not honor changed values of properties in the assembly drawing of a variant.

Solution: None.

CCR 19225: Components containing IEEE symbols are not visible in CIS explorer.

Description: During part creation, a user has access to a number of predefined graphical symbols. These symbols are grouped together as IEEE symbols and can be placed onto a library part using the Place IEEE Symbol command. If these symbols are used during part creation, any graphics added after the first symbol placement do not show up in the CIS part window in the CIS explorer. The actual part placed on the schematic contains the graphics as represented in the part library.

Solution: Edit the part in the library to remove the IEEE graphics symbol from the library part. Replace the symbol with other graphics elements, lines, polylines, rectangles, and so on.

CCMPR01949292: Update from SigXplorer prompts to update the topology in Allegro CM while SigXplorer was launched from Capture CM

Description: In a Constraint Manager-enabled design, when both Capture - Constraint Manager and Allegro Constraint Manager windows are open, and any update from SigXplorer (when launched from Capture-Constraint Manager interface) prompts to update the topology in Allegro Constraint Manager.

Solution: Open command prompt, set `CDS_SIS_SESSION_ID=<any_unique_number>`. For example, set `CDS_SIS_SESSION_ID=81970`. Next, launch PCB Editor from this command prompt and perform the required operation.

CCMPR01949268: Match Groups are not formed as per `Class` scope

Description: An ECSet has been created with `Class` scope and has been applied on a net class. The match group that is created does not honor the `Class` scope, and the net class name is not suffixed to the match group name.

Solution: This feature is not supported yet.

CCR 1147140: Support for reloading of hierarchical part

Description: Any modifications by the librarian in the schematic for hierarchical parts are not updated on choosing the *Reload Library Parts* option. Only the symbol for the hierarchical parts is updated.

Solution: Re-launch Capture to view the updated hierarchical parts.

CCR 1145501: Library Refresh: Capture does not reload library if added to the project in PM or if lock file exists of same owner

Description: When a library is opened or added to a project in Capture, a `.lck` file is created for that library. If the you replace this library on disk with an updated version, the updates are not read in the same session because the `.lck` file exists for you (owner).

Solution: Edit and save the original library in the same session using Capture. Once saved, the library is updated in the Place Part dialog.

No CCR: Connection is created between some objects during alignment or distribution

Description: Following objects may connect during alignment or distribution task when the *Drag Connected Object* option is *OFF*:

- Global
- OPC

- Ports
- Power/GND

Solution: None

CCR 943666: ENH: Flexibility to name a bus member in NetGroup as ?BUS[MSB..LSB]?

Description: Although `Bus[MSB..LSB]` is allowed resulting in the correct order for input pin of NetGroup block, the pin name and order is incorrect if autowire is done for entry pin or for NetGroup bus. Bus name is not taken into consideration resulting in flat NetGroup name members.

CCR 730224: Library gets upreved without any uprev message.

Description: Open a 16.2 library in 16.3 and perform the following operations:

1. Right-click the part and choose *Split part*. Save the part.

   Right-click the library (release 16.2) and choose either *New part from spreadsheet* or *New Symbol*.

   For the above operations, the 16.2 library is upgraded without displaying any message.

2. Open a 16.2 library in 16.3 and choose *Save As*. For the upgrade message, choose *Yes* and save it to another name. A backup of the new library is made instead of a backup of the original library.

Solution: When upgrading a library (`<library name>.olb`), Capture preserves the original copy of the library in the old database format. This file is saved with the name `<library name>_2_0_0.OBK` at the same location. You can rename this file as `<library name>.OLB` to retrieve the original library.

CCR 725742: Capture does not generate error and may allow you to create recursive design hierarchy tree.

Description: Capture may allow you to create a recursive design hierarchy tree if a schematic level operation is performed in the Project Manager window.

Solution: None.

CCR 724760: IREF generated for buses connected to OPCs.

Description: On a design, if the port is a bus and the bus bit is an off-page connector or the net name is the same as the bus bit, IREF is not generated.

If the off-page connector is a bus and the bit is an off-page connector or the net name is the same as the bus bit, IREF is not generated.

Solution: None

CCR 724738: Update/Replace cache not working properly on user-defined pin shapes.

Description: Choose any user-defined pin shape in the design cache and replace it with any other user shape. Changes are reflected in the schematic editor; pin shape changed to the new shape. On editing part, Capture still shows old pin shape and not the new shape.

If you close the part editor and update current or update cache without any change, pin shape is reverted to previous shape. Make some changes and then update, changes are not visible in part editor.

Cleanup cache will even remove the pin shape shown in part editor. But when you try to place same part from design cache still shows the old shape. Move the part or reopen design, changed pin shapes are not retained but reverted to the previous part.

Solution: If you do *Replace cache* on a user-defined pin shape say *A* with *B* in the design, all instances of the user-defined pin shape *A* are replaced by *B* in the design and Pin Shape property on the pins are updated to new pin shape value.

This property is an instance override. At any time, you want to revert to library level pin shape value, use *Delete property* in property editor to delete the instance override and the same will be reflected on the schematic.

However, if you do an *Edit part*, it will still show the part level user-defined shape and not the instance override that exists in the schematic. This is by design.

CCR 722555: Cannot dock command windows if Allow docking is not set.

Description: The command window is not docked if you set the *Allow docking* option and then deselect the option.

Solution: None

CCR 701056: Capture crashes due to old workspace data in registry.

Description: Capture crashes choosing *Place – Autowire – Connect to Bus*.

Solution: Remove the registry key `HKEY_CURRENT_USER\Software\OrCAD\CaptureWorkSpace\16.3.0` and then re-launch Capture.

CCR 700463: Pin shape issues.

Description:

- Replace a pin with a user-defined pin shape. The pin is not attached to the part boundary. There is no extra space between the shape and its bounding box.
- The pin shape created and the pin shape shown in part editor are different depending on the shape designed.

Solution: None

CCR 700407: Pin is removed if using IEEE symbols or picture in pin shapes.

Description: Create a pin shape using IEEE symbols or picture. Replace a pin with this shape, pin is removed. The pin name appears in the corner of the page. Update so that you can check on schematic. On schematic nothing can be seen and the pin is removed.

Solution: You cannot use IEEE symbols, text, or images when creating a pin shape.

CCR 687342: IREF not generated for external designs till page number is manually updated.

Description: Generating IREF for design with single hierarchical block that references an external design (design is in instance mode), causes a page number error. Using the *Annotate* command does not update the pages. Same behavior is observed for a design with hierarchical parts.

Solution: Before generating the IREF, update the pages manually.

CCR 425315: The Archive Project utility does not archive PSpice Advanced Analysis (AA) *opamp* models

Description: If you instantiate a part from the *OPA.OLB*, for example, *CA1458*, and create an archive; OrCAD Capture does not archive the model used by the part. The reason for this behavior is that the value of the *Implementation* property on the part is *awbca1458*, where as the library does not have this model. Instead the part contains models, like *awbca1458_1*, *awbca1458_2*, and *awbca1458_3*. Note that netlisting / simulation and Edit PSpice Model is successful and works by appending Implementation with the value of the property LAVEL to arrive at one of the above mentioned values.

Solution: None.

CCR 37520: Relative path should be added to place port macros.

Description: The *PORTIN.BAS* (Place Input Port) and *PORTOUT.BAS* (Place Output Port) macros shipped with Capture do not work because they have the wrong path set for *CAPSYM.OLB* library.

Solution: Open the `PORTIN.BAS` and `PORTOUT.BAS` files located in the `\tools\capture\macros\` directory in a text editor and correct the path for `CAPSYM.OLB` library.

CCR 31067: Need to run backannotation and update design twice if pin swapping and gate swapping is done for the same section in Allegro PCB Editor board.

Solution: If you have swap pin and gate for the same section in your Allegro PCB Editor board, run backannotation (and update your design) two times.

CCR 22098: DEVICE property in Capture version 9.2 and later.

Description: The `DEVICE` property that was used in previous releases, is used differently in Capture 9.2 and later. However, the existence of this property in your design library can cause problems with the Capture-Allegro PCB Editor interface.

Solution: In cases where your design library includes the `DEVICE` property (an anachronism from previous releases), you can avoid having to remove the property from each part in your library by employing the `IGNORE_PROP` property. To ignore the `DEVICE` property on a

complete design, define `IGNORE_PROP` as an environmental/system variable and assign it a value of *DEVICE*.

As with all environmental variables, `IGNORE_PROP` is specific to a system login. You must have administrative privileges to define `IGNORE_PROP` as a system variable. Also, you must restart Capture in order to read the new variable settings.

CCR 21123: Testbench should be invoked with VHDL editor.

Description: When you edit a simulation testbench from the NCVHDL Preroute (or Postroute) Simulation dialog box, the tool should open the testbench file with the VHDL editor, thereby highlighting VHDL keywords and other language features. However, the tool currently opens the file in the default text editor tool for the host system.

Solution: Generate the testbench file normally, include it in the project, and then open it from the project manager as a VHDL file. This will invoke the VHDL editor.

CCR 228624: Pads and wirelist netlists do not display visible Power pins connected to an external power.

Description: This problem arises when you make power pin visible for a component by checking *Power Pin Visible* in the Edit Properties dialog box and connect the pin. Now, when you create a netlist, the power pins do not appear in the netlist.

Solution: Before you create a netlist:

- Close the design file and reopen it.

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- Edit the part to make Power pins visible.

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- Drag the part slightly.

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