cadence™

Best Practices:
Working with Design True DFM

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Contents

Best Practices: DesignTrue DFM

Release 17.2-2016 of Allegro PCB Editor included new series of DRC checks focused on manufacturing, assembly, and test that run independent of the electrical and other physical checks performed in the design database. The DesignTrue DFM checks are global checks (meaning across the entire design outline) and purely focused on these three domains with no regards to constraint areas. As the rules are stackup based, it is possible to have different DesignTrue DFM rule CSets assigned to different stackup zones in a multi-stackup design, such as rigid-flex. The methodology is based on the fact that PCB Fabricators fabricate to minimums across an entire design in the traditional PCB fabrication processes.

Traditional Sign-off to Manufacturing

The sign-off flow in the more traditional processes where an OEM has no in-house DFM (Design for Manufacturing) checking tools may see delays in sign-off due to the time it takes for a manufacturer to run the DFM check, analyze the results, and return Technical Queries (TQs) for issues discovered. Once issues are resolved, the release process starts all over again.

For OEMs not having in-house DFM checking tools, there are common situations where at the end of the day, or week, the manufacturing data is extracted from the design and passed to the DFM tools to be run, results are waited upon, issues are resolved, and then the design process is continued. This cycle is performed several times during the design process, interrupting the design, hoping that when sent to fabrication all issues are resolved. Though fabricator may find issues, they are at least fewer. But design time has been extended due to the time it takes to generate manufacturing data for the DFM tool to validate.

DesignTrue DFM Impact to Manufacturing Sign-off

The DesignTrue DFM capabilities offer real-time checks during the design process. As soon as fabrication, assembly, or test issues are created, they are marked with DRC tags. The issues can then be resolved at the moment. The requirement of generating fabrication data, sending to another tool, and waiting for a report is no longer required. Because DesignTrue DFM is an on-line check, a much shorter time to manufacturing sign-off with fewer TQs can be achieved.

Before Beginning Use of DesignTrue DFM

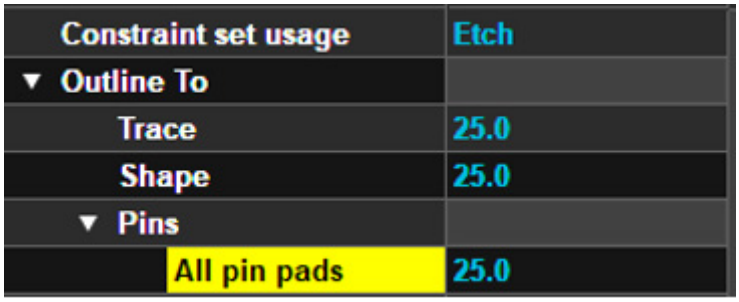
When a new feature is introduced, the first reaction is to find the most challenging PCB and throw everything at it. This may or may not prove anything, but when it comes to DesignTrue DFM, you will not really learn anything. The best approach is to understand what impacts the sign-off schedule and begin to focus on one or two areas. The best utilization of DesignTrue DFM is at the start of a new design, where the advantages of on-line checking can be realized.

Current Sign-off Process Review

A common answer to the question “What are your most common sign-off issues that delay release?” or “What are the most common TQs (Technical Queries) received from the fabricator?” is “I am not sure”. This is probably the hardest part of the process for many. Looking back at the release history of TQs for past designs may require cross-functional groups, or lead to the realization that this type of history has not been maintained.

Focusing to historical data from fabricators can identify common problem areas in PCB fabrication, assembly, and test. Start in one category, and find the top ten most common issues. Then focus on defining the DesignTrue DFM specifically for those issues. When the results are more positive focus on the next group of issues.

As an example, an OEM sees a trend with silkscreen (legend) over pads, silkscreen running over edge of the board outline, and traces too close to the edge of the PCB. By defining a series of DFM CSets, and applying the CSets to silkscreen layers and copper layers, these issues are now identified as part of the on-line checks, and the TQs for these issues are reduced or eliminated.



Name	SILKSCREEN
*	*
Constraint set usage	Non-Etch
▼ Pins	
All pin pads	4.0
Thru pin pad	4.0
SMD pin pad	4.0
Slot pad	4.0
Mechanical hole pad	4.0
Tooling hole pad	4.0
Mounting hole pad	4.0
▼ Vias	
All via pads	2.0
Thru via pad	2.0
BB via pad	2.0
Micro via pad	2.0

Creating DFM Rule Files

Spacing, width, and other fabrication concerns for PCB are driven by different factors including a PCB Fabricator's capabilities, product technology, product's intended use (IPC Design Classifications), materials, and most commonly, copper weight. Understanding these factors, and applying proper manufacturing rules in Allegro Constraint Manager can make a major difference in the accuracy, yield, and producibility of the PCB during the fabrication process.

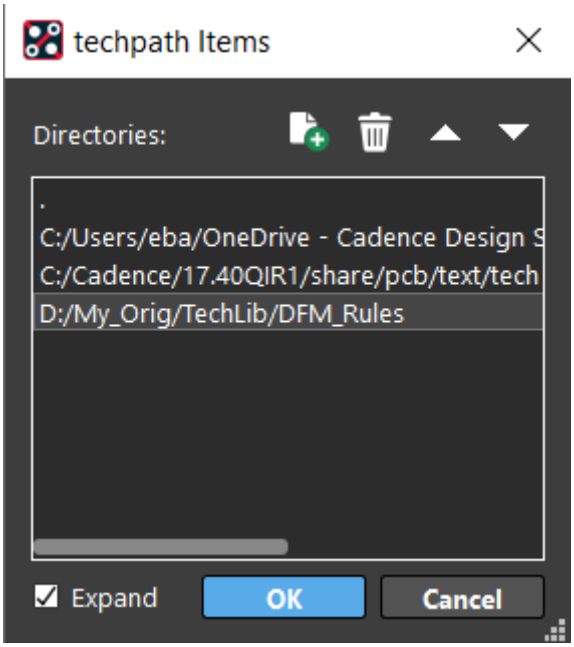
When defining the rule files, ensure a proper methodology is in place to import rules addressing the various criteria mentioned above without the need for multiple complex rule structures for every conceivable stackup configuration. Create rule sets that focus on a specific layer's copper weight, or application, such as mask or silk screen. A single PCB may have varying copper weights on individual layers requiring specific spacing, thickness, and width values for the different layers.

This section focuses on the methodology for defining rule files that may be used efficiently during the design process.

DesignTrue DFM Rule File Library

Rule File Locations

Create a library of DFM rules files to store and manage the various rules sets. Ensure that this directory is accessible by other Allegro users to import into their designs. Include the DFM directory as an entry in the Allegro PCB Editor `techpath` user preference setting.

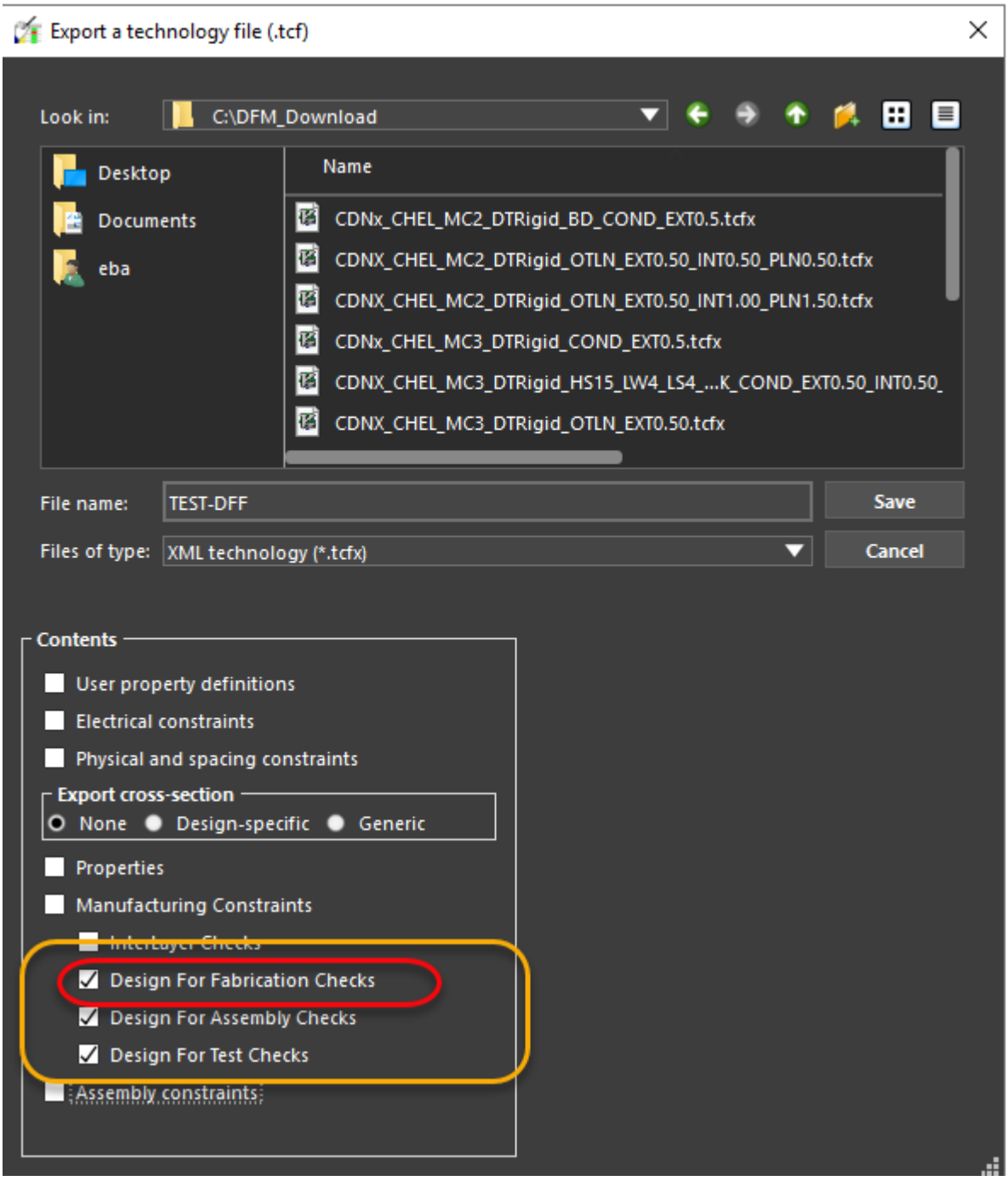


Defining the proper shared directory and breaking the DFM directory into subdirectories and further into rule categories to make rule selection easier may prove to be beneficial. Dividing a DFM rule into the major categories of rules sets, such as, Design for Fabrication (DFF), Design for Assembly (DFA), and Design for Test (DFT) helps in focusing on a specific type of DFM check. The technology files for each type would be stored in to the proper directory.

Rules Files and Naming

Export the rules files as technology files (`*.tcfx`). The Constraint Manager Export Technology file allows to export only the DFM type rules. When setting the options for exporting the rules to a technology file, verify that the *Export Cross-section* is set to *None*,

and only the *Manufacturing Constraints* for the specific rule type (for example, Design For Fabrication checks and or Design For Assembly checks) are set before running the export.



It is recommended to keep the DFM technology file name concise and meaningful to help understand what technology the file represents. The Appendix section describes details of file naming based on the DesignTrue DFM ecosystem web-based tool for rules request.

DesignTrue certified fabricators guided to a strict file naming convention that allows for automation for rule file selections for distribution to the end user of the rules. A strict Constraint Set naming convention is also included in the vendors rules sets to allow for import automation, such as through a DesignTrue Rules Wizard.

A recommended strict naming convention for Constraint Sets are highlighted in this section of this document so that automated/wizard tools can be applied to streamline the rule selection or assignment to a design.

Defining DFF Constraint Set Names

Design For Fabrication (DFF) rules do not require every category and combination to be defined within a single constraint set. Segmenting the rules into categories, such as layer use (silkscreen, solder mask, internal conductor, external, conductors, and so on) or conductor thickness (0.5 oz., 1.0 oz., and so on) provides easier configuration and application of rules to any design. Breaking the rule sets into several files by rule type, function, copper weight, and technology creates a more succinct and clearer choice of rules when it comes to applying the rules in a design. This document suggests a method for defining rules based on these principles.

Silkscreen Rules

In most cases typically only one or two silkscreen rules set may ever be applied in various designs. One set would be for rigid portions of a PCB, and another for flex. In the following example only two silkscreen rule sets would be required that could be imported in each design.

In Constraint Manager, only define a single silkscreen rule set without entering any values in any other DFF rules. Provide a constraint name that indicates the intended use of the rule set. In the following example, the silkscreen CSet is composed for a 4-character company identifier, a 4-character site code, the rule type (Silk), and the technology type (R - Rigid, F-Flex).

Constraint Name Examples

<Company Identifier>_<Site Code>_**silkscreen**_<technology type>

CDNS_BOST_Silk_R

CDNS_BOST_Silk_F

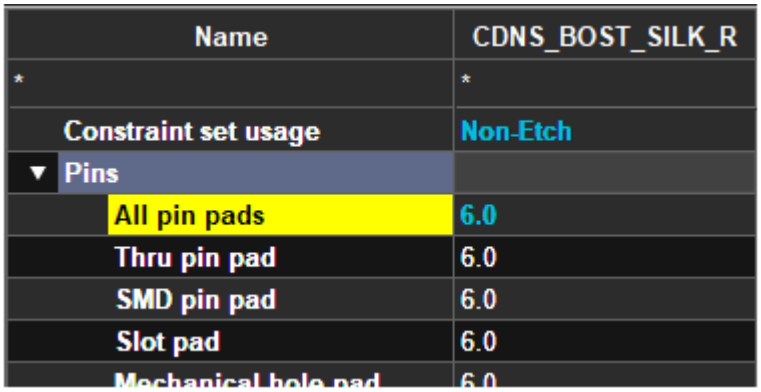
After the rules are defined for the first rule set, export that rule set into a technology file. Suggested file name structure for silkscreen rules would be:

```
<Company Identifier>_<Site Code>_<Manufacturing Class>_<Design
Technology>_SILK_

CDNS_BOST_MC2_DTRigid_SILK.tcfx

CDNS_BOST_MC2_DTFlex_SILK.tcfx
```

After the export is complete, create a new silkscreen rule set, with the constraint set name that represents the rule type and technology, and export the new rule set into another technology file.



The suggested name scheme for the silkscreen constraint set in the image above implies that the rule was defined by the company, from a specific site (for multi-site design groups), is a silkscreen rule set only, specifically for rigid designs. If a silkscreen rule set was imported from a fabricator the file name would contain the fabricator company name and site, along with the silkscreen and technology label. If both rules were imported, the design would have a choice of rule sets to apply if policy allowed.

Another example for independent rule sets is a rigid-flex design with multiple stackup definitions, with both the rigid and flex silkscreen rule sets imported into the design. The designer is able to assign the proper silkscreen rules to the corresponding rigid and flex stackups in the design.

Mask Rules

Mask rules may require a few different rule sets based on materials, manufacturing type, and technology. A mask rule set could be specified as a common rule set with options such as rules specific to a rigid PCB versus a flexible circuit and manufacturing class.

In Constraint Manager, only define a single mask rule set without entering any values in any other DFF rule. Provide a Constraint Set name that indicates the intended use of the rule set.

In the following example, the Mask CSet is composed for a 4-character company identifier, a 4-character site code, the rule type, a technology type, and surface layer if applicable.

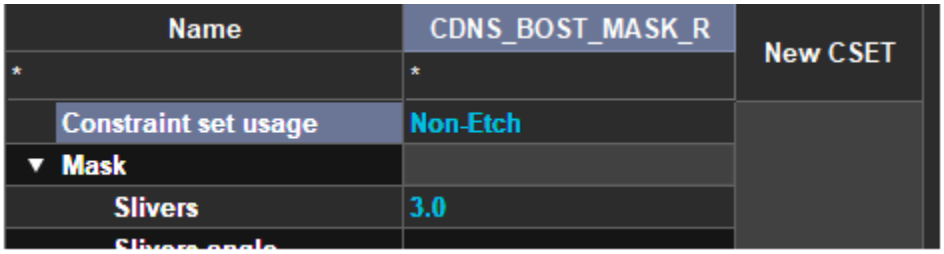
Constraint Name Examples

```
<Company Identifier>_<Site Code>_Mask_< technology type>

CDNS_BOST_Mask_R

CDNS_BOST_Mask_F
```

After the first rule set is defined, export that rule set into a technology file. After the export is complete, create a new mask rule set with the constraint set name that represents the rule type, technology, and other factors and export the new rule set into another technology file.



The suggested name scheme for the mask constraint set in the image above implies that the rule was defined by the company from a specific site (for multi-site design groups) is a soldermask rule set only, specifically for the top layer of a rigid design. If a mask rule set was imported from a fabricator the file name would contain the fabricator company name and site, along with the mask, technology label, and so on. If both rules were imported, the designer would have a choice of rule sets to apply if corporate policy allowed.

Another example for independent rule sets is a rigid-flex design with multiple stackup definitions, with both the rigid and flex mask rule sets imported into the design. The designer is able to assign the proper soldermask and coverlay rules to the design.

Outline Rules

Outline rules are applied to detect the clearances between board outline geometry and cutouts to conductor and non-conductor objects in the PCB design. These rules may vary depending on internal, external, and plane layers as well as copper layer weight. Heavier copper weights (for example, 3 ounce copper weight) may require more copper to edge clearance than lighter (0.5 ounce copper weight) copper layers. Internal layer rules may also differ between external layers and internal layers. In general, it is preferred that rules for outline checks be based on copper weights.

There are three constraint usage types for outline checks: etch, non-etch, and stackup. Each type should have an independent rule set. But if the rules are constant, they could be included into a single rule file. When defining outline rule set values, begin by creating a stackup use type for the combined outline to cutout checks under the "stackup" constraint usage type. It may only require one or two individual rule types based on flex or rigid designs. The Constraint Set name would consist of the company identifier, site code, identify as the stackup rules check with the design technology.

Stackup Constraint Name Examples

`<Company Identifier>_<Site Code>_**Stkp**_<technology type>`

`CDNS_BOST_Stkp_R`: This rule would apply to the outline to outline, outline to cutout and cutout to cutout checks for a rigid PCB.

`CDNS_BOST_Stkup_F`: This rule would apply to the outline to outline, outline to cutout and cutout to cutout checks for a flex PCB.

Continue to define outline to mask rules. The Constraint set naming would continue to follow the naming conventions of company identifier, site code, and an identify indicating the stackup mask rules types with the design technology.

Outline Mask constraint name examples

`<Company Identifier>_<Site Code>_**Mask**_<technology type>`

`CDNS_BOST_Mask_R`: This rule would apply to the outline to outline, outline to cutout and cutout to cutout checks for a rigid PCB.

`CDNS_BOST_Mask_F`: This rule would apply to the outline to outline, outline to cutout and cutout to cutout checks for a flex PCB.

Note: The constraint name appears to be a duplicate constraint name of the mask rules described under Mask Rules. Though the names are identical, the rule domain is different. The one specified in the outline context is independent of the Constraint Set defined in the Mask context.

Outline to copper checks should be separated into individual technology files and constraint names based on internal conductor layer, external conductor layer, plane layer, and copper weight. Outline rule name schemes would consist of company identifier, site code, layer type, copper weight, and design technology.

Outline copper constraint name examples

`<Company Identifier>_<Site Code>_<LayerType and copper weight>_<technology type>`

`CDNS_BOST_EXT0.5_R:` This rule would apply to outline to conductor, external 1/2 ounce copper layer for a rigid design PCB.

`CDNS_BOST_EXT0.5_F:` This rule would apply to outline to conductor, external 1/2 ounce copper layer for a flex design PCB

`CDNS_BOST_INT1.0_R`: This rule would apply to outline to conductor, internal 1 ounce copper layer for a rigid design PCB.

`CDNS_BOST_INT1.0_F`: This rule would apply to outline to conductor, internal 1 ounce copper layer for a flex design PCB.

`CDNS_BOST_PLN1.5_R`: This rule would apply to outline to conductor, plane 1 1/2 ounce copper layer for a rigid design PCB.

`CDNS_BOST_PLN1.5_F:` This rule would apply to outline to conductor, pane 1 1/2 ounce copper layer for a flex design PCB.

Annular Ring, Hole, Copper Spacing and Copper Feature Rules

The wide variety of rules for annular ring, hole, copper spacing, and copper features should all be defined using layer type and copper weight where applicable. When defining the constraint set rule names they should follow the convention of company identifier, site code, layer type, copper weight, and design technology. Each constraint name may be a duplicate name used in other checking domains, but each constraint set is maintained within the context of the DFF rule categories.

Examples of Annular Ring rules

`<Company Identifier>_<Site Code>_<LayerType and copper weight>_<technology type>`

`CDNS_BOST_EXT1.0_R:` This rule would apply to the annular ring rules for an external 1 ounce copper layer for a rigid PCB design.

`CDNS_BOST_INT1.0_R:` This rule would apply to the annular ring rules for an internal 1 ounce copper layer for a rigid PCB design.

`CDNS_BOST_PLN2.0_R:` This rule would apply to the annular ring rules for a conductor plane 1 ounce copper layer for a rigid PCB design.

`CDNS_BOST_Mask_R`: This rule would apply to the annular ring mask values for a rigid PC design.

Name	Constraint set usage	Missing mask	Pad to mask	P
		mil	mil	
*	*	*	*	*
Cdns_Bost_Mask_R	Non-Etch	On	1.0	
Cdns_Bost_Ext0.5_R	Etch			5.0
Cdns_Bost_Int1.0_R	Etch			5.0
Cdns_Bost_PIn2.0_R	Etch			5.0
<Create new>				

Examples of Holes Rules

`<Company Identifier>_<Site Code>_`**`Stkp`**`_<technology type>`

`CDNS_BOST_Stkp_R`: This rule would apply to hole rules for a rigid PCB design.

`CDNS_BOST_Stkp_F`: This rule would apply to hole rules for a flex PCB design.

Name	Constraint set usage	Via	Plated thr
*	*	*	*
<Create new>			
Cdns_Bost_Stkp_R	Stackup	8	8

Examples of Copper Feature Rules

`<Company Identifier>_<Site Code>_<LayerType and copper weight>_<technology type>`

`CDNS_BOST_EXT0.5_R`: This rule would apply to the copper feature rules for an external 1/2 ounce copper layer for a rigid PCB design.

`CDNS_BOST_INT1.0_R:` This rule would apply to the copper feature rules for an internal 1 ounce copper layer for a rigid PCB design.

`CDNS_BOST_PLN2.0 _R:` This rule would apply to the copper feature rules for 1 ½ ounce copper plane layer for a rigid PCB design.

Name	Constraint set usage	Minimum Line width mil
*	*	*
<Create new>		
Cdns_Bost_Pln2.0_R	Etch	8.0
Cdns_Bost_Int1.0_R	Etch	4.0
Cdns_Bost_Ext0.5_R	Etch	3.5

Examples of Copper Spacing Rules

`<Company Identifier>_<Site Code>_<LayerType and copper weight>_<technology type>`

`CDNS_BOST_EXT0.5_R:` This rule would apply to copper spacing rules for an external 1/2 ounce copper layer for a rigid PCB design.

`CDNS_BOST_INT1.0_R`: This rule would apply to copper spacing rules for an internal 1 ounce copper layer for a rigid PCB design.

`CDNS_BOST_PLN1.5_R:` This rule would apply to copper spacing rules for 1 ½ ounce copper plane layer for a rigid PCB design.

Name	Constraint set usage	Trace to	
		Trace	Sha
		mil	mi
*	*	*	*
<Create new>			
Cdns_Bost_Pln2.0_R	Etch	8.0	8.0
Cdns_Bost_Int1.0_R	Etch	4.0	4.0
Cdns_Bost_Ext0.5_R	Etch	3.5	3.5

`CDNS_BOST_Stkp_F`: This rule would apply to hole rules for a flex PCB design.

Begin by defining the CSet rule that indicates the intended use of the rule set. In the following example, outline and cutout stackup CSet name is composed of a 4-character company identifier, a 4-character site code, the rule type, the layer type, and technology type. Enter the values for the stackup usage ignoring all other values. Export the constraints into a technology file with a properly formatted or agreed upon file name structure. Once export is complete, define a new set of stackup rules and export those with properly formatted Constraint set and file names to make them distinguishable.

Stackup Constraint Name Examples

`<Company Identifier>_<Site Code>_<rule_type>_<technology type>`

`CDNS_BOST_Stackup_Rigid`: This rule would apply to the outline to outline, outline to cutout and cutout to cutout checks for a rigid PCB.

`CDNS_BOST_Stackup_Flex:` This rule would apply to the outline to outline, outline to cutout and cutout to cutout checks for a flex PCB.

Applying DesignTrue DFM Rule to a Design

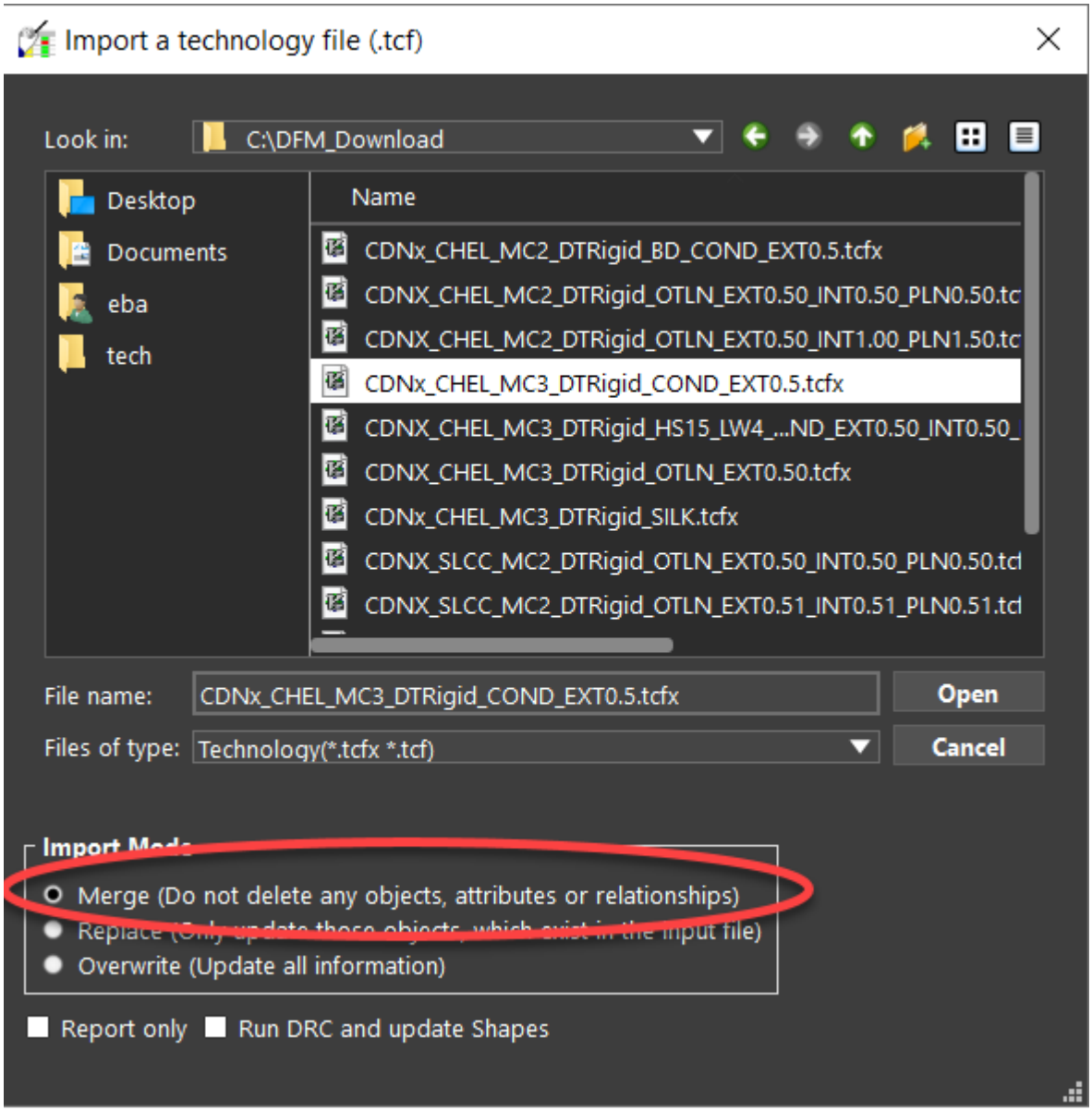
Proper DesignTrue DFM rule sets simplifies the applying of rules to a design. There are various options in using technology files, the first is those created by the user, the user can obtain rules through the DesignTrue DFM Web Portal, or by using the DesignTrue DFM Wizard.

Refer to *Cadence DesignTrue DFM Web Rules Rule Request Guide* for more details on requesting DesignTrue DFM rules from a fabricator.

Importing DFM Technology Files

Whether using customized technology file as defined in the previous sections, or by using the fabricator-supplied technology files received through use of the DesignTrue DFM Rules Request Web Portal, the import process follows the basic technology file import into Allegro Constraint Manager. To prevent unexpected results during the import of one or many

technology files, pay attention to the import settings. Be certain that only the *Merge* option is enabled.



Once all of the technology files are imported, they are ready to be assigned to the design layers.

Assigning DFM CSets

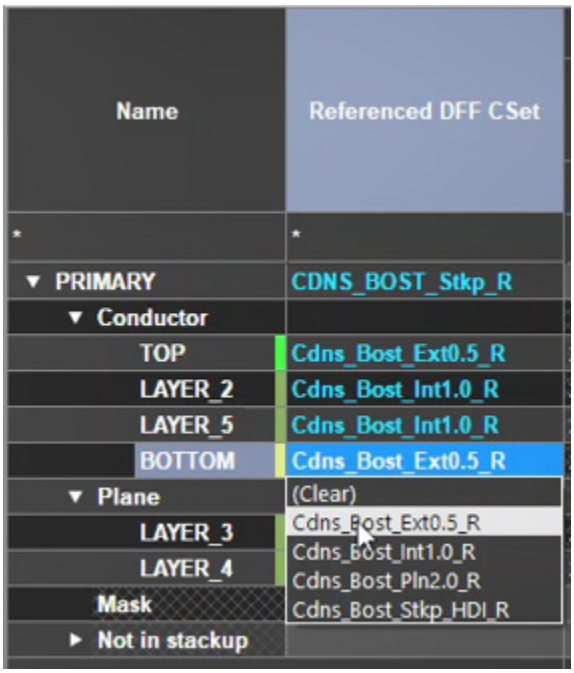
Before assigning DFM CSets to design layers, verify that a proper stackup definition has been created.

From the Manufacturing design worksheets, assign etch rules to the conductor layers. Know the coper thickness, and proper naming of the CSets, assign the CSets to the corresponding etch layer.

Figure 1-1 Stackup Definition Example

Objects		Types		Thickness
#	Name	Layer	Layer Function	Value mil
*	*	*	*	*
		Surface		
1	TOP	Conductor	Conductor	0.7
		Dielectric	Dielectric	8
2	LAYER_2	Conductor	Conductor	1.4
		Dielectric	Dielectric	8
3	LAYER_3	Plane	Plane	2.8
		Dielectric	Dielectric Core	8
4	LAYER_4	Plane	Plane	2.8
		Dielectric	Dielectric	8
5	LAYER_5	Conductor	Conductor	1.4
		Dielectric	Dielectric	8
6	BOTTOM	Conductor	Conductor	0.7
		Surface		

Figure 1-2 Assigning CSets to layers based on copper weight

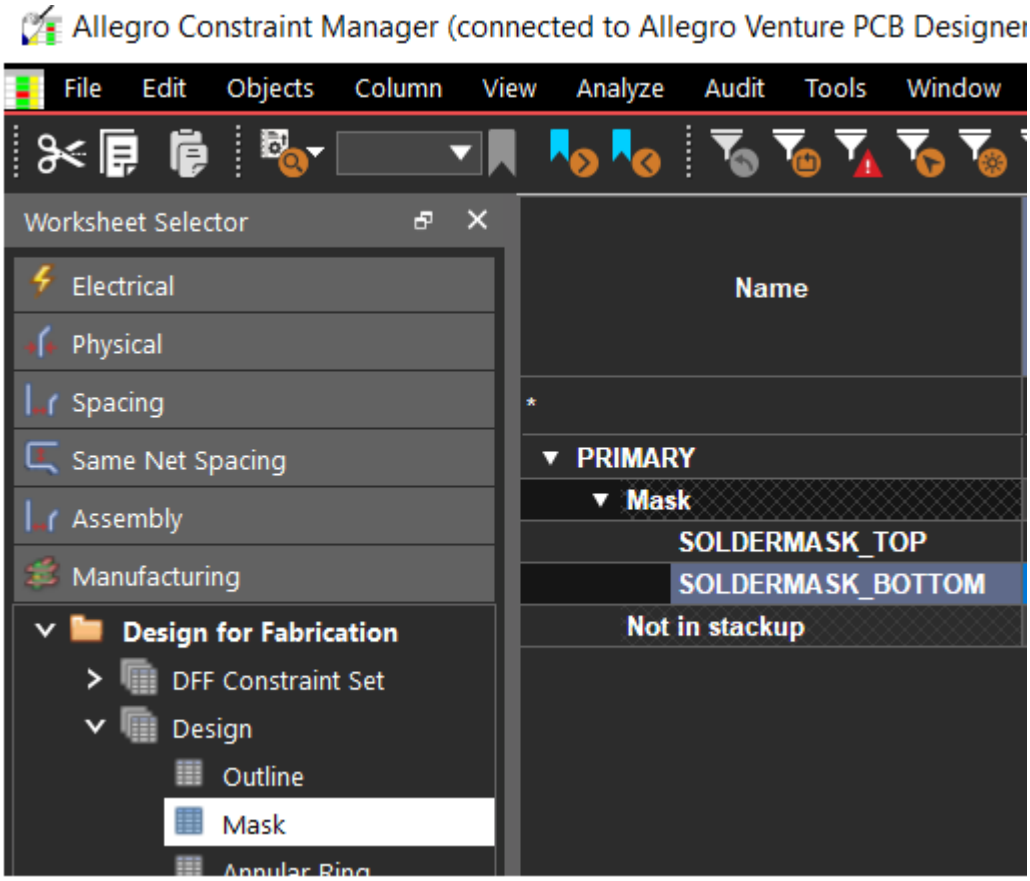


If the Soldermask (or Coverlay) is defined in the stackup definition, theses layer will appear in the CSet assignment for mask and annular ring checks.

Figure 1-3 Stackup with Soldermask Layers

#	Name	Layer	Layer Function	Value mil
*	*	*	*	*
		Surface		
	SOLDERMASK_TOP	Mask	Solder Mask	1.5
1	TOP	Conductor	Conductor	0.7
		Dielectric	Dielectric	8
2	LAYER_2	Conductor	Conductor	1.4
		Dielectric	Dielectric	8
3	LAYER_3	Plane	Plane	2.8
		Dielectric	Dielectric Core	8
4	LAYER_4	Plane	Plane	2.8
		Dielectric	Dielectric	8
5	LAYER_5	Conductor	Conductor	1.4
		Dielectric	Dielectric	8
6	BOTTOM	Conductor	Conductor	0.7
	SOLDERMASK_BOTTOM	Mask	Solder Mask	1.5
		Surface		

Figure 1-4 Mask Layer displayed when defined in Stack-up



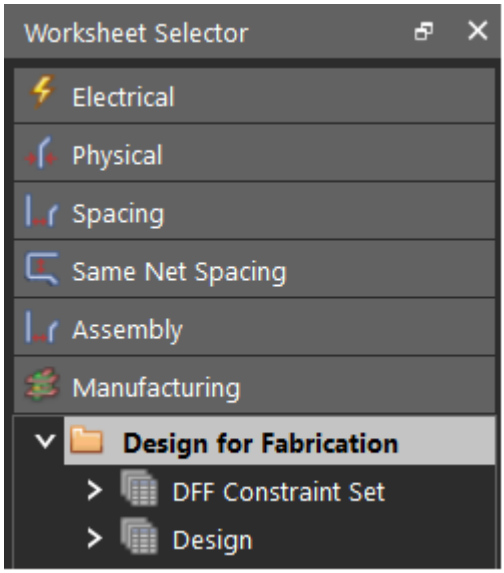
For layers not defined in the stackup, the layers that compose an artwork image layer can be defined in subclass groups using the tool provided in the *Not in stackup* entry.

Assigning Constraint Sets to Not in Stackup Layers

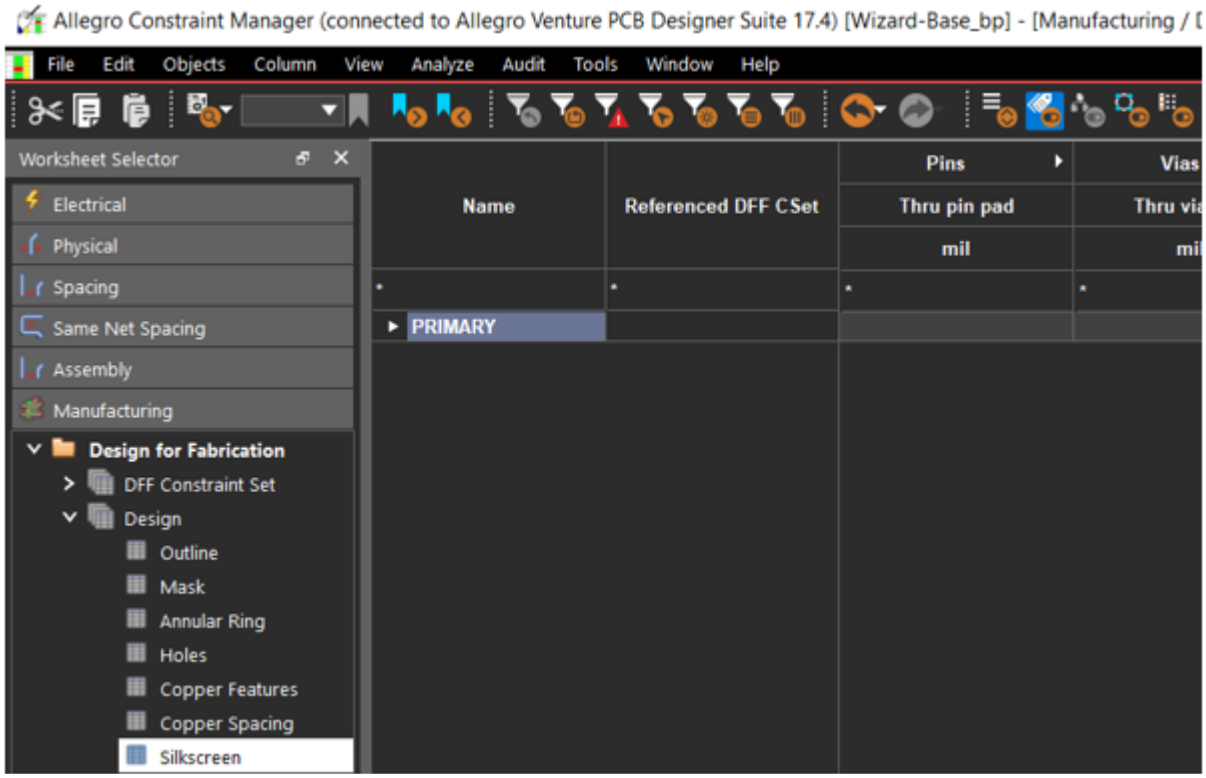
The following steps walk you through an example of assigning DFM CSets to a silkscreen layer, typically not defined in a stackup structure.

1. Start Allegro Constraint Manager. (*Setup – Constraints – Constraint Manager)*.

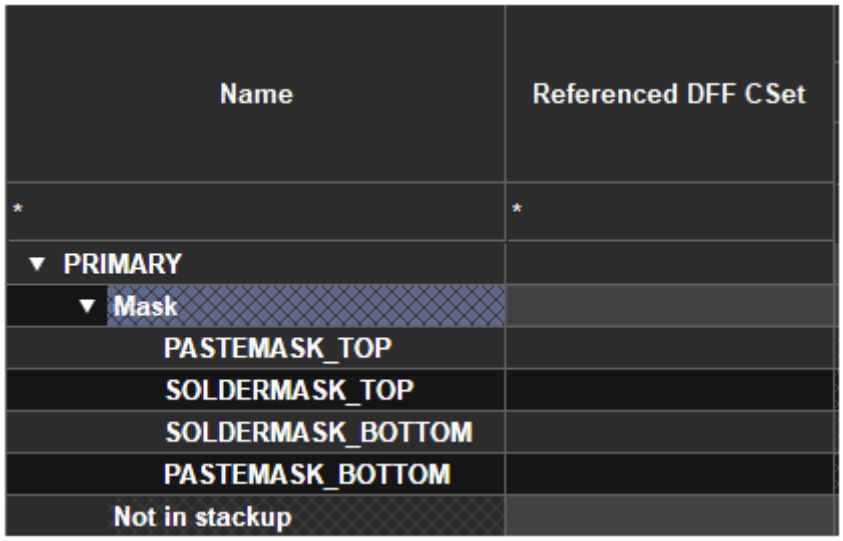
2. In Constraint Manager, select *Manufacturing* in *Worksheet Selector* to see the *Design for fabrication* constraint categories.



3. Expand *Design for Fabrication – Design – Silkscreen*.

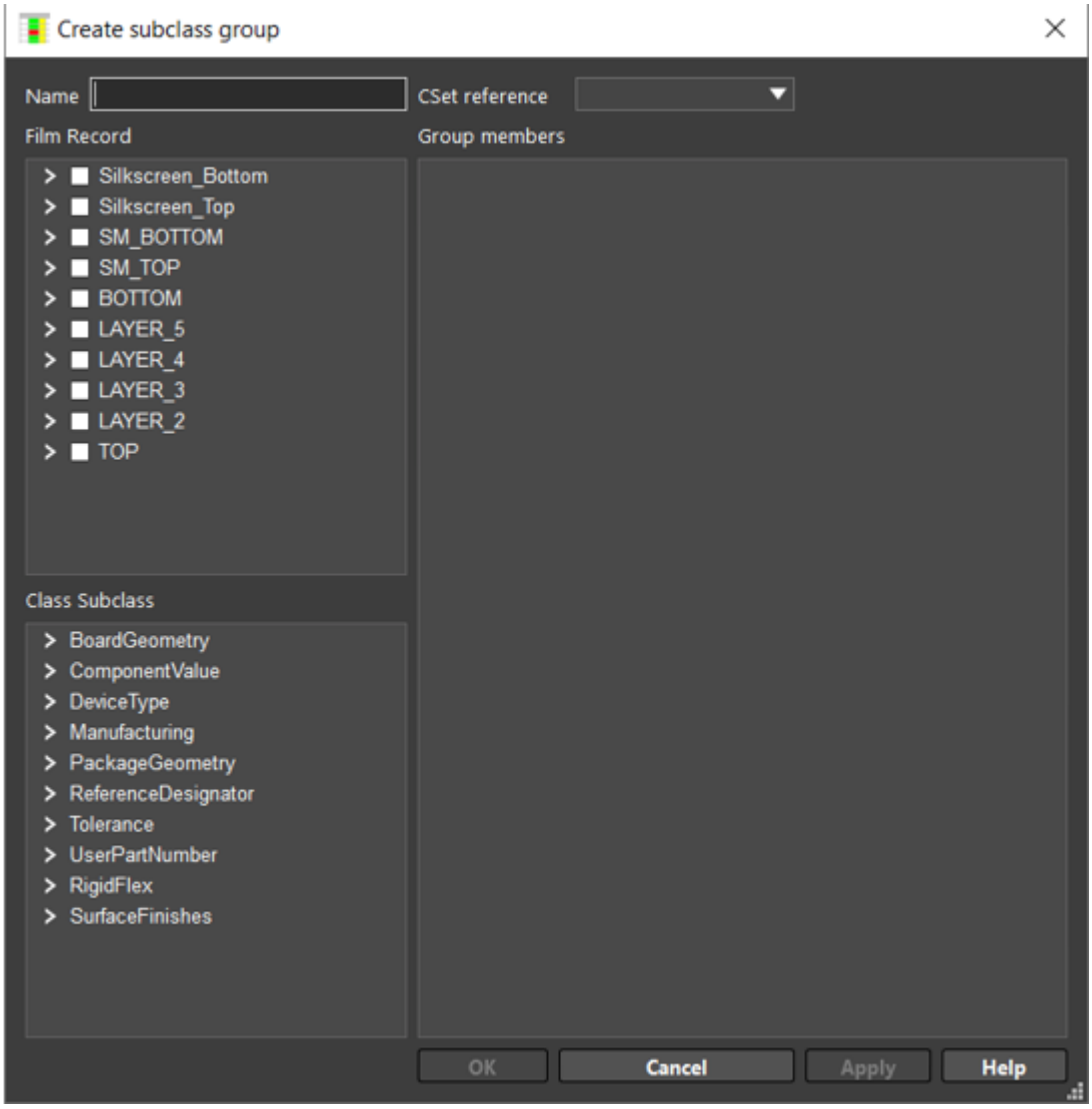


4. Expand the Primary stackup entries to display the non-etch layer names.



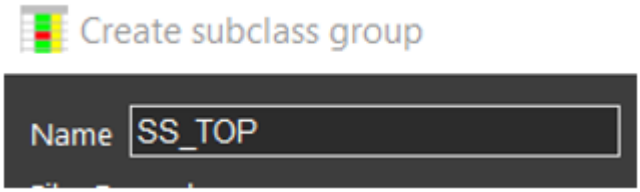
There are no silkscreen layers defined in the Primary stackup definition. Silkscreen layers can still be identified and the silkscreen Constraint Set can be associated to the silkscreen layers.

5. Right-click *Not in stackup* and choose *Add Subclass Group* from the popup menu.



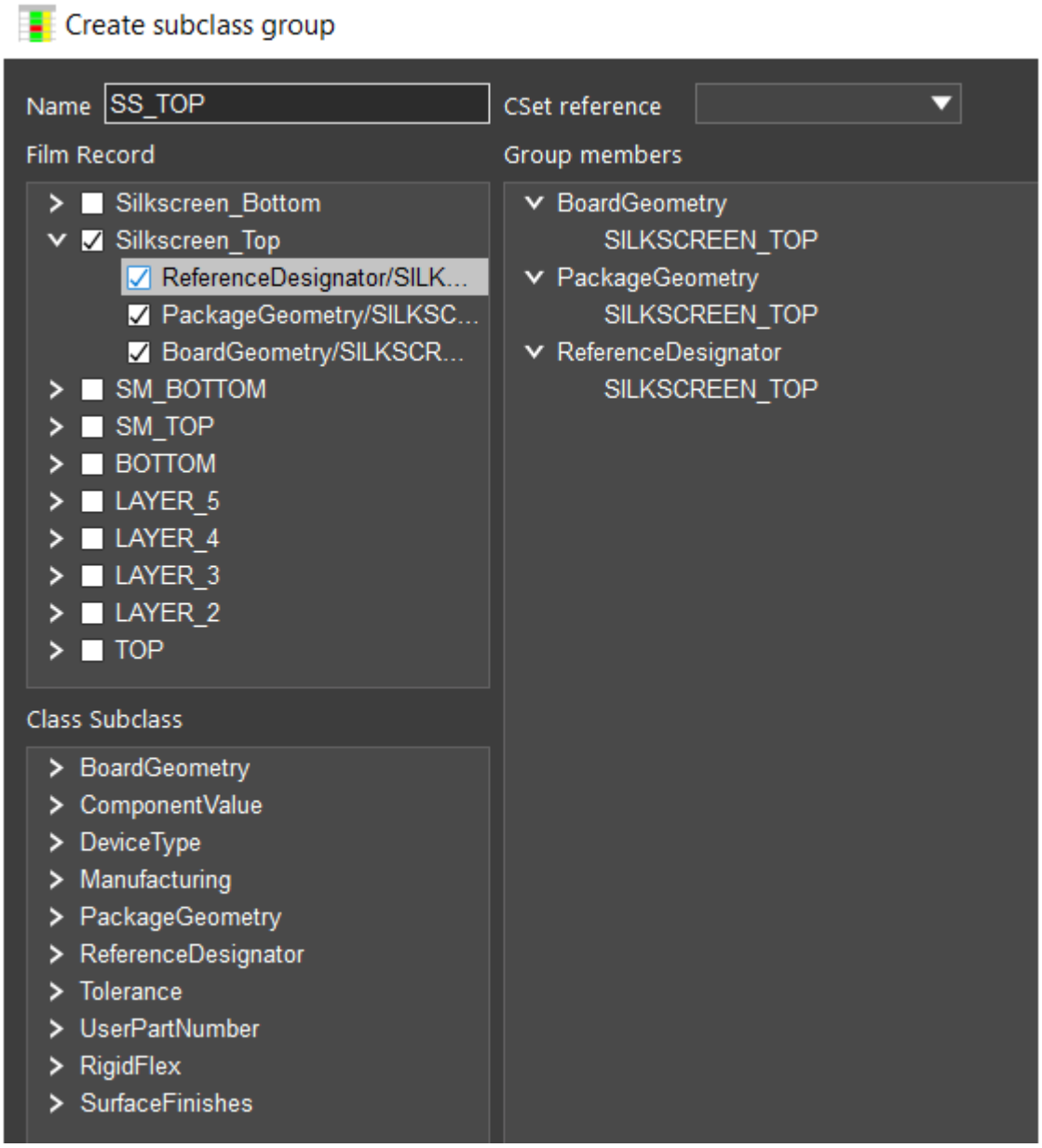
The Assign Subclasses form opens.

6. Enter the name `SS_TOP` in the *Name* field of the Assign SubClasses form.

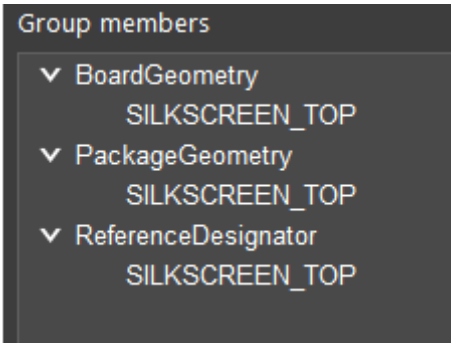


7. Select the subclasses that compose the silkscreen top layer:

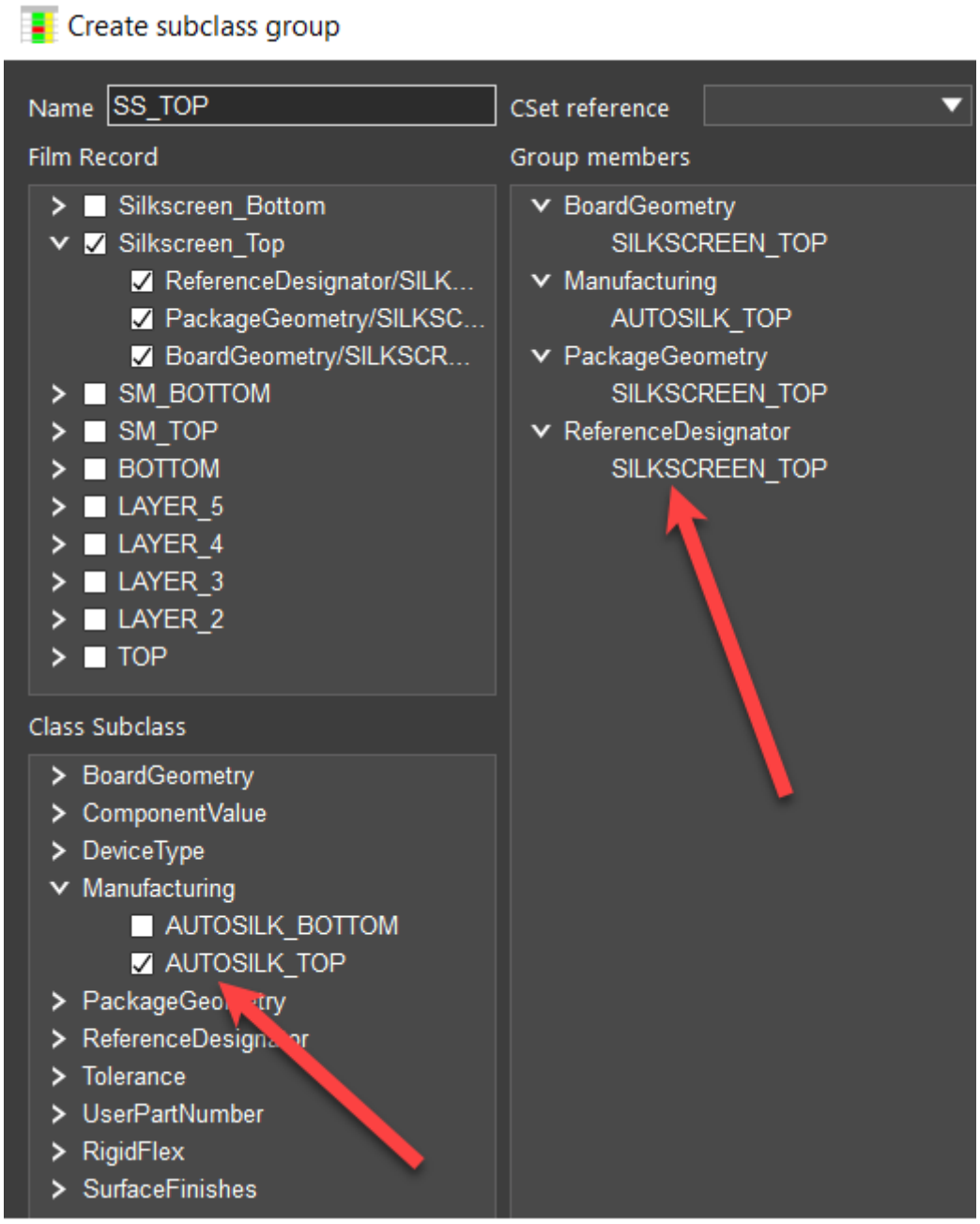
a. In the Create Subclass form, select the film record that defines the top silkscreen layers Board Geometry/SILKSCREEN_TOP.



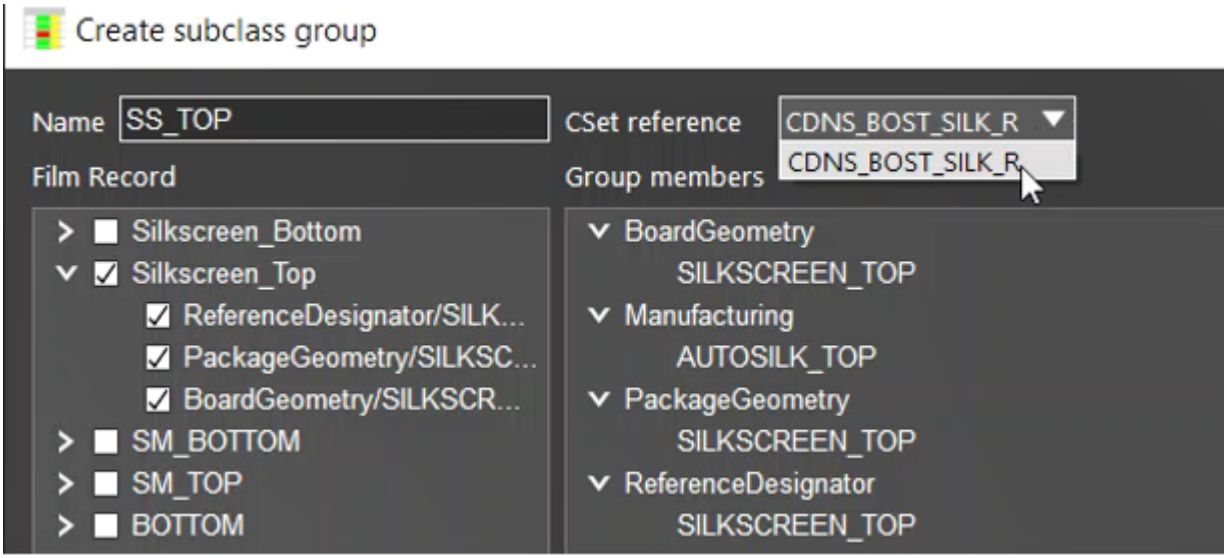
The layers that make up the top silkscreen defined in the film record are displayed in the Group Members list.



b. Include the Manufacturing AUTOSILK_TOP layer by selecting the subclass in the *Class Subclass* selection view. The *Group members* displays the addition of the AUTOSILK_TOP subclass.

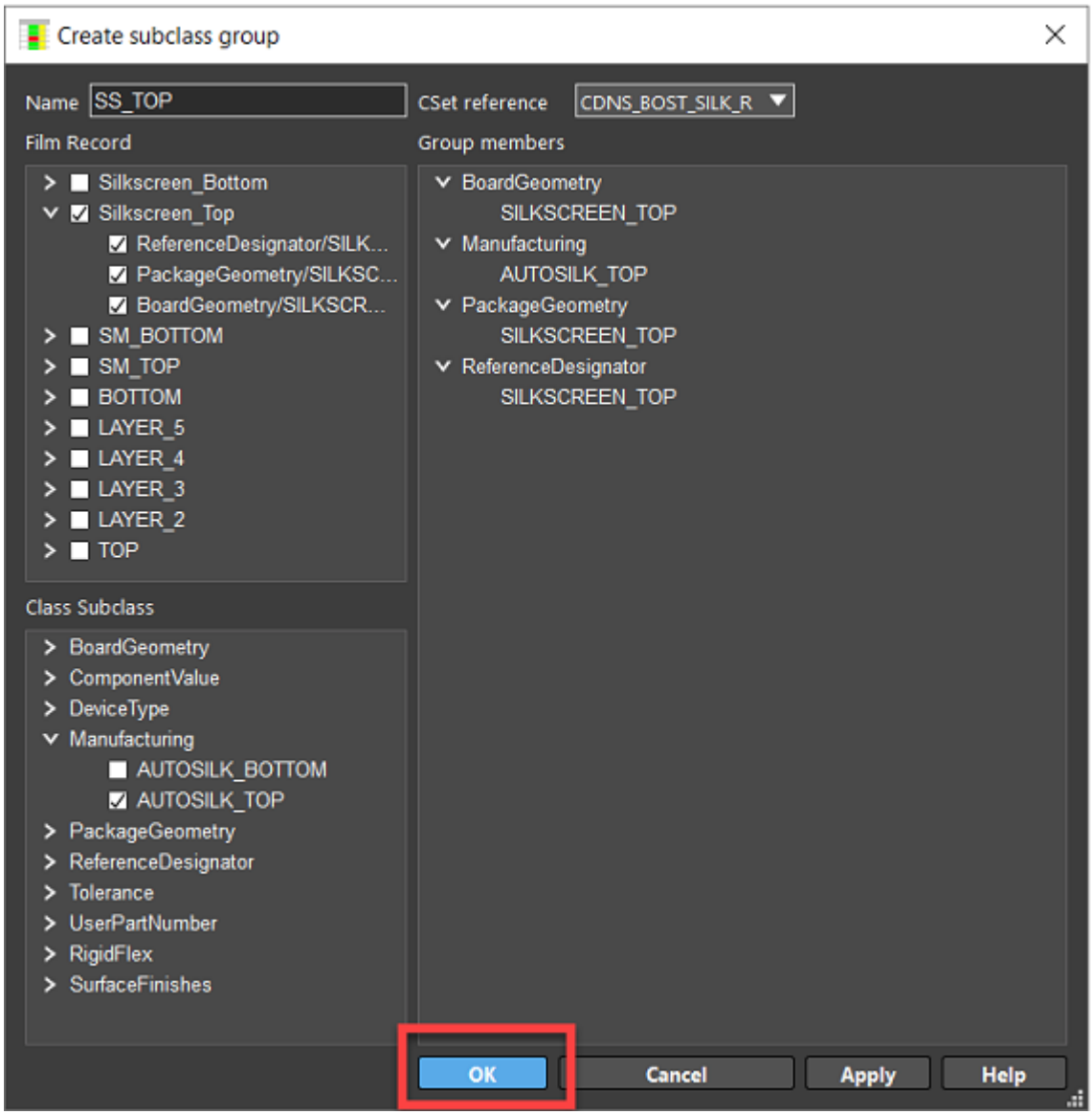


8. Using the pull-down menu in the CSet reference field, select the CSet `CDNS_BOST_SILK_R`.



The subclass layers that compose the Top Silkscreen layer have been identified as a common layer, and the Silkscreen Constraint Set is associated with that layer.

9. Click *OK* to instantiate the layers into the Constraint Set, and CSet assignment into Constraint Manager.



10. Expand *Not in stackup* to verify the new assignment.

Name	Referenced DFF CSet	Pins		
		Thru pin pad	SMD pin pad	
		mil	mil	
*	*	*	*	*
▼ PRIMARY				
▼ Mask				
PASTEMA...				
SOLDERM...				
SOLDERM...				
PASTEMA...				
▼ Not in stackup				
SS_TOP	CDNS_BOST_SILK_R	6.0	6.0	6.0

The CSet is now associated with the SS_TOP layers as defined in the Subclass Group listing.

11. Close Constraint Manager

Efficiently Applying DesignTrue DFM Rules During the Design Process

Having all of the DesignTrue DFM DFF required rules imported and assigned into the design, the layout process can begin. Verify that the rules to be applied are enabled before continuing to design.

Applying DFM Rules

One practical method for using the DesignTrue DFM checks is to enable the checks related to a particular phase of the design. When placing the design, turn on component to component, component to outline, pin to pin checks, and so on along with through hole and SMD Pin annular ring checks. Checking for via to pin or trace to pin checks do not necessarily apply during placement. As you move through the design process, include more DesignTrue DFM checks.

A

Understanding Fabricator Supplied Files Names

The Design Trues DFM ecosystem web tool provides a communication portal for designers to request DesignTrue DFM rules files directly from the PCB Fabricator. This web-based tool assists the PCB Fabricator in generating DFF technology files. One of the features of the tool is the naming of the technology file based on the criteria used to create the file. It is important to note that a PCB Fabricator may change the name of the file and ignore the default file name.

The default full file name for the DFF technology file contains several descriptors or fields. Each of the fields defines the criteria of the DFF rules. The following file name example displays all of the fields that can be applied to a single rule file.

Note: This example is not the preferred method of rule definition but displays the maximum capability.

`CDNS_BOST_MC2_DTRigid_HS24_LW4_LS4_BPP169_BPS75_MV_BD_EC_OTLN_MASK_SILK_COND_EXT0.5_INT1.0_PLN1.5.tcfx`

A more common use model would be where rules are broken into specific use cases with different rules for solder mask, silkscreen, external ½ oz. copper, internal 1 oz. copper, and so on. The following examples display the preferred file definition methodology.

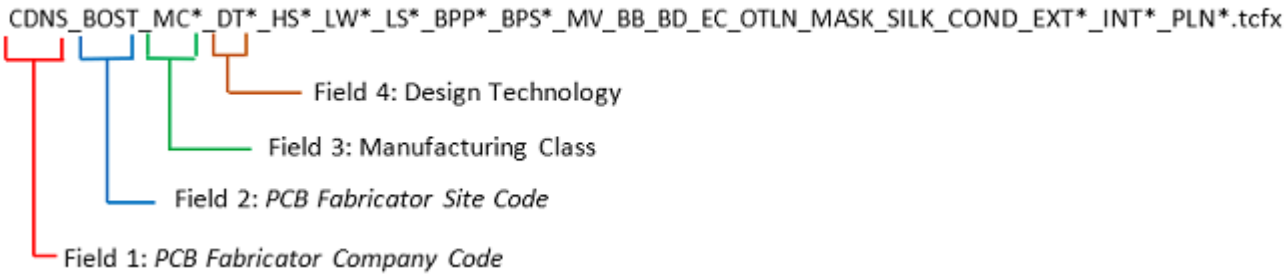
`CDNS_BOST_MC2_DTRigid_SILK.tcfx:` A rule file for a Class 2 rigid PCB silkscreen

`CDNS_BOST_MC2_DTRigid_OTLN_EXT0.5.tcfx:` A rule file for a Class 2 rigid PCB external ½ oz. copper layer board outline rules.

`CDNS_BOST_MC2_DTRigid_HS24_LW4_LS4_COND_EXT0.5.tcfx`: A rule file for a Class 2 Rigid PCB with 24 mil minimum holes size, 4 mil line width and spacing, ½ external copper layer.

File Name Structure

Each file name is divided into multiple groups or fields separated by an underscore (_). When this structure is used, the first four fields are consistent for every file name. The four fields are:



Field	Description	Values (*)	Remarks
1	A four-character PCB Fabricator company name code	Designates the name of the PCB Fabricator's name as defined by the Fabricator	
2	A four-character code that designates the for the PCB Fabricator's site	Designates the PCB Fabricator's site location name as defined by the Fabricator	
3	MC	Manufacturing Class	Designates the manufacturing class requirement specification. Based on IPC Class 2, Class 3, and so on, but other specifications may be used
4	DT	Design Technology	Designates the design technology applied in the design, such as a Rigid or Flex design, HDI, Radio Frequency (RF), and so on.

The remaining fields may or may not be used based on how the DesignTrue DFM DFF rules are created. The following table explains the various field definitions and values as they apply.

Field Code	Definition	Value	Remarks

HS	Finished hole size	Diameter of the finished hole	
LW	Line Width	Minimum line width	
LS	Line to Line spacing	Minimum line to line spacing	
BPP	BGA Pin Pitch	BGA pin center to center pin pitch spacing	
BPS	BGA Pin pad Size	The minimum BGA pin pad size	
MV	Micro Via		Micro or Laser via rule technology is applied
BB	Blind Buried Via		Blind buried via rule technology is applied
BD	Back Drill		Back drill rule technology is applied
EC	Embedded Component or Embedded Coin		Rules related to Embedded technology are applied for embedded components or embedded coins.
OTLN	Outline		Contains outline spacing rules
MASK			Contains mask and mask spacing rules
SILK			Contains silkscreen and silkscreen spacing rules
COND	Conductor		Rules for conductors are contained within the rules file
EXT	External conductor layer	Copper weight in ounces	External layer rules specific for defined copper weight
INT	Internal conductor layer	Copper weight in ounces	Internal layer rules specific for defined copper weight

PLN	Plane Layer	Copper weight in ounces	Plane layer rules specific for defined copper weight

An example of a rule file name for a rigid PCB ½ ounce external copper layer rule for a class 3 HDI design with 4 mils line/spacing and 24 mil minimum via holes size using blind buried vias would be:

```
CDNS_BOST_MC3_DTRigidHDI_HS24_LV4_LS4_BB_COND_EXT0.5.tcfx
```