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Topology Workbench: What's New in Release 23.1

Product Version 23.1
October 2023

Contents

Topology Workbench: What's New in 23.1

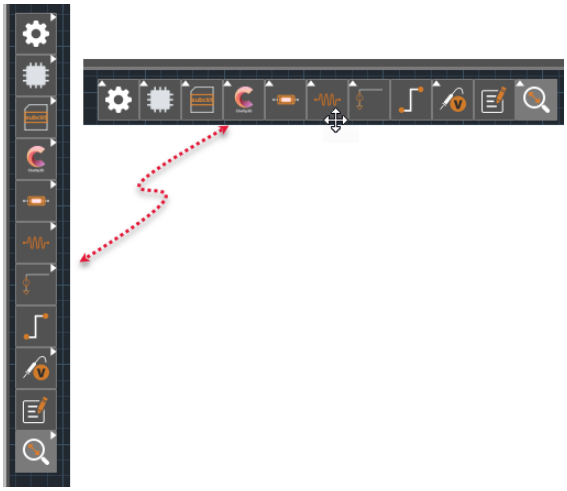
This document describes the new features and enhancements introduced in Cadence® Sigrity™ Topology Workbench in release 23.1.

For bug fixes and improvements in Allegro PCB SI in release 23.1, see *README_CCR.txt* in the *OrCAD/Allegro 23.1 (SPB231)* page at downloads.cadence.com.

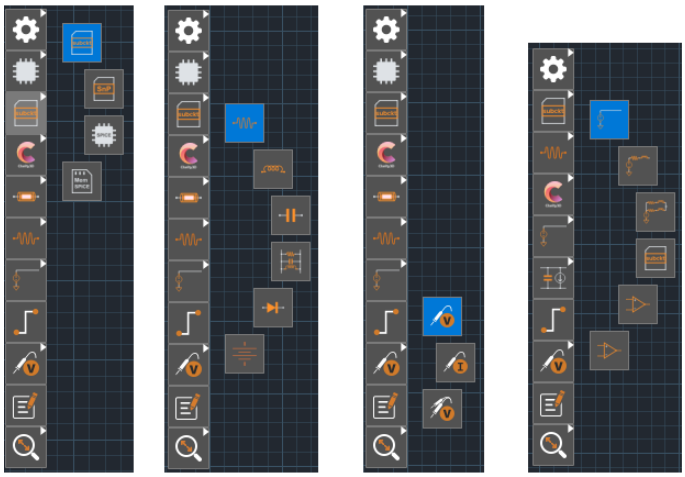
Common Updates

Floating Toolbar Replaces the Add Block Panel and Features New Block Icons

In this release, the Add Block panel has been removed. Instead, a new floating toolbar is available in the main application window with controls to help with various design operations on the canvas. It is by default aligned vertically and can be docked horizontally per convenience.



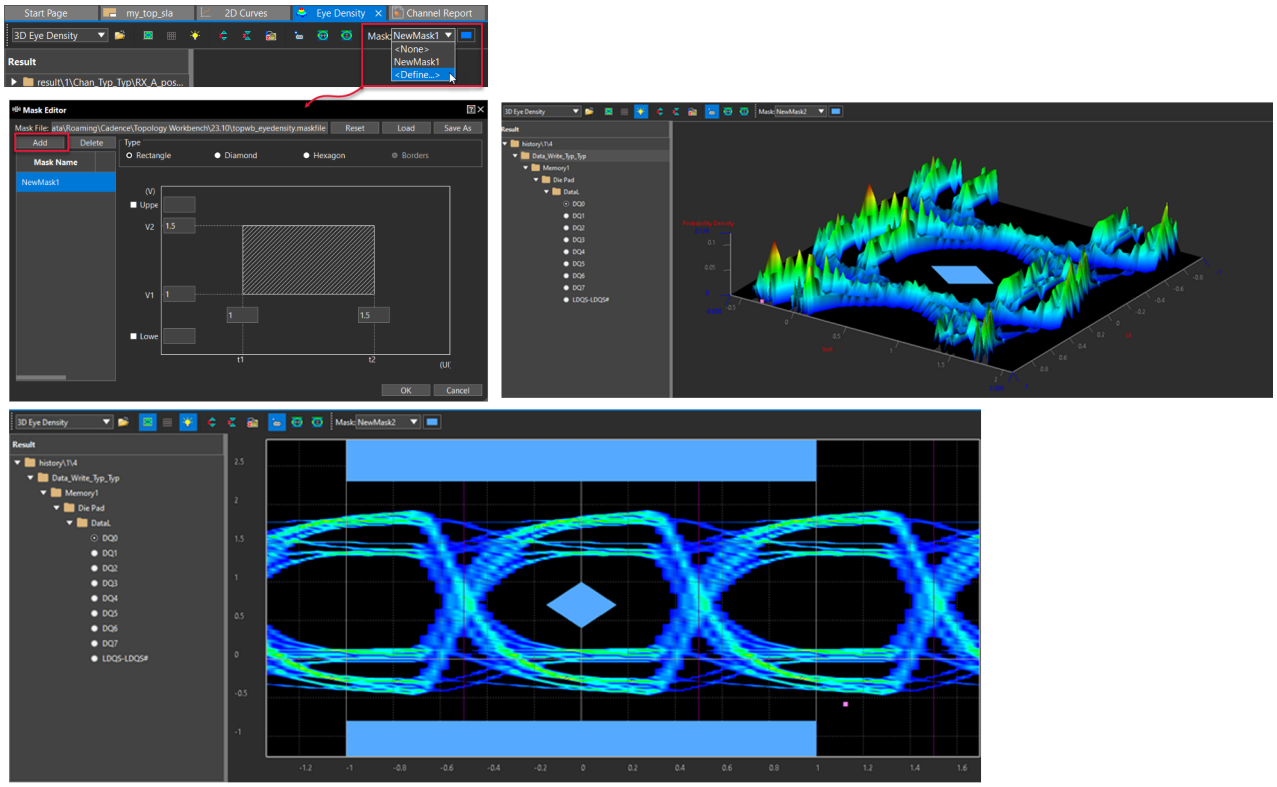
The floating toolbar features improved icons for placing blocks on the canvas. Only a subset of icons is visible at a time. To explore the additional blocks that can be added to the canvas, right-click any of the icons in the floating toolbar.



SystemSI Updates

Eye Mask Support Added to 3D Eye Density Plots

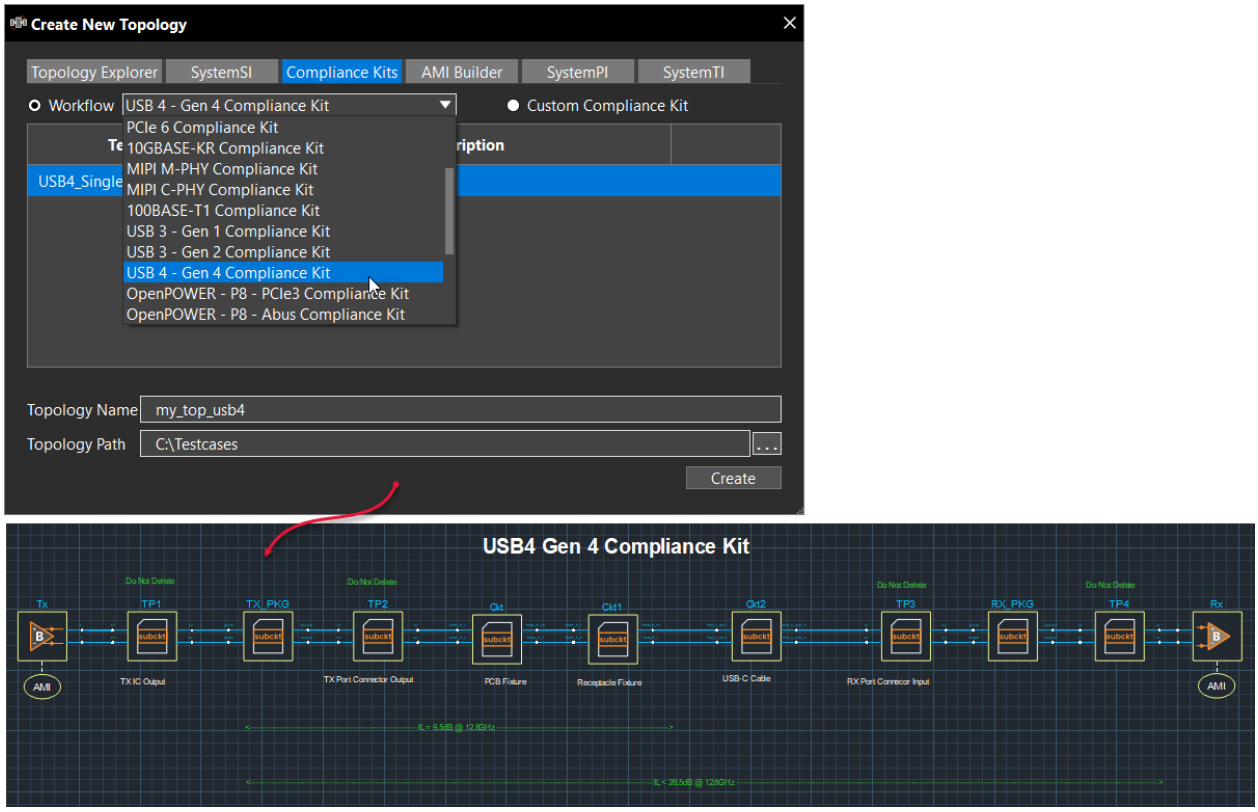
On completion of a channel simulation run in the Parallel Bus Analysis (PBA) or Serial Link Analysis (SLA) workflow, you can now define and apply eye mask values to the 3D plots in the Eye Density tab.



USB4 Gen 4 Compliance Kit Supported

The Compliance Kits workflow now supports USB 4 - Gen 4 Compliance Kit. With this enhancement, you can run PAM3 simulation at a defined Baud Rate for a single lane topology comprising Tx, Rx, Tx and Rx Port Connectors, PKG, Cable, and fixtures. Except for a few

components labeled as *Do Not Delete* in this sample topology, you can replace workspace items in the single-lane topology with your own design models.



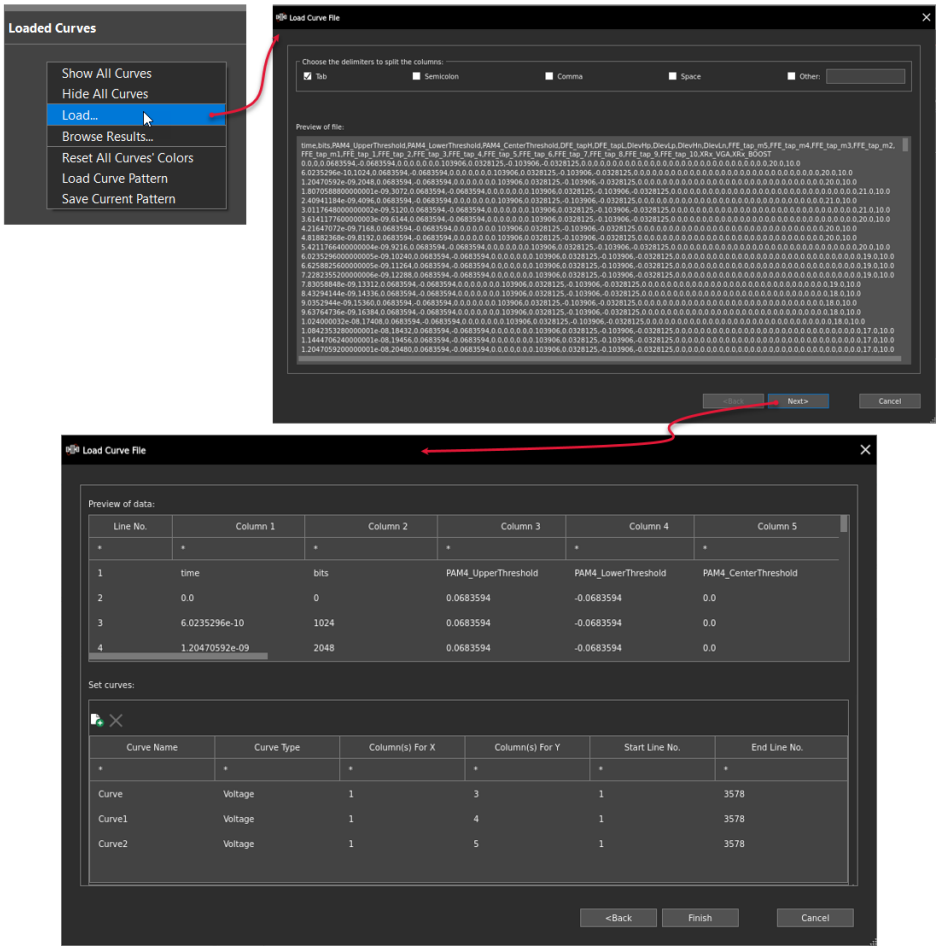
The related compliance items include the transmitter and receiver tests for parameters such as:

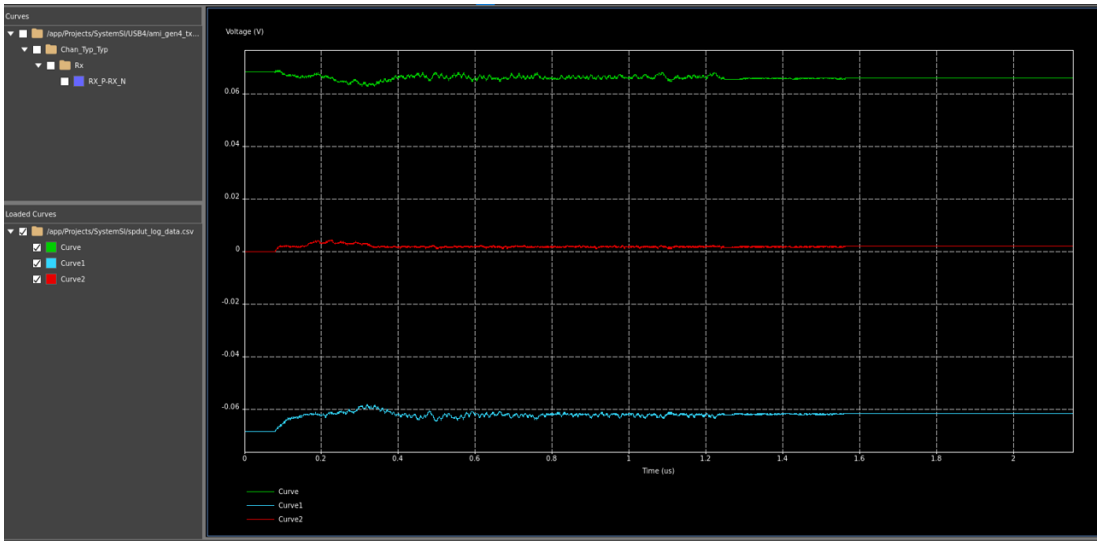
- Tx level, Tx differential return loss, and Tx signal to noise distortion ratio (SNDR) (Section 3.2.3.4)
- Rx end-to-end channel differential insertion loss, Rx differential return loss, and Rx tolerance test (Section 3.2.4.2)

A compliance report is generated on completion of the checks.

Import CSV Data into Waveform Display

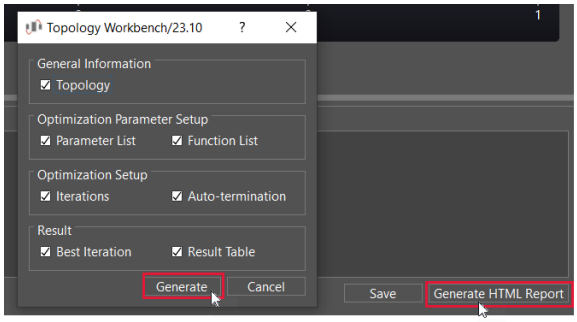
Some AMI models write data to a CSV file for post-processing and analysis. This data can now be imported and displayed in the 2D Curves tab with the simulation results.





Optimality Interface Enhanced to Generate a Report

In this release, the *Generate HTML Report* button has been added to the Optimality window for Topology Workbench. Clicking this button opens a dialog box where you can configure the contents of the report and generate the Topology Workbench Optimality Report.



2 Optimization Parameter Setup

2.1 Parameter List

Index	Optimize	Name	Type	Expression	Ref Value	Unit	BoundType	LowBound	HighBound	Step	Array
1	True	Trace_W	continous	1mm	1	mm	relative	1	2		
2	False	Trace_R	continous	2mm	2	mm	relative				

Return to Top

2.2 Function table

Name	Mode	Expression	Custom Function	Type	Indexi	Indexj	Target
obj		E12		Objective Function(goal)			
E12	single_end			Average	1	2	

4 Result

4.1 Best Iteration

Best Iteration: 5

Return to Top

4.2 Result Table

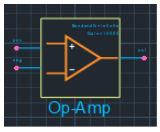
Index	obj	E12	Trace_W
0	0.999261	0.999261	1.23412
1	0.978154	0.978151	1.54421
2	0.951231	0.951231	1.1325
3	0.983121	0.983121	1.32489
4	0.977281	0.977281	1.525494
5	0.923211	0.923211	1.85421

SystemPI Updates

Support Added for New VRM Models

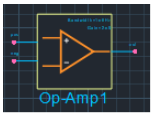
The following two operational amplifier (Op-Amp) blocks have been added to model voltage regulator modules (VRM) more accurately:

- *Ideal Op-Amp*, which is a model with a simple voltage-controlled voltage source (VCVS) with an input impedance resistor and output impedance resistor.



Name	Value
Block Name	Op-Amp
Input Impedance	1e7Ohm
Gain	10000
Output Impedance	0.1 Ohm

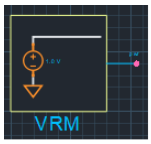
- *Bandwidth-Limited Op-Amp*, which is a model with an ideal op-amp with a bandwidth limit.



Name	Value
Block Name	Op-Amp1
Input Impedance	2e6Ohm
Gain	2e5
Bandwidth	1e6Hz
Output Impedance	0.1 Ohm

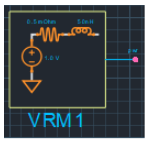
In addition, the following VRM blocks have been updated:

- *Ideal Supply (VDC) VRM*, which is a simple DC model.



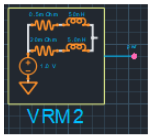
Name	Value
Block Name	VRM
Nominal Voltage	1.0 V
▼ Power Net	
Net Name	PWR
# of Pins	1
Pin Name	pwr
Pin Resistance(Ohm)	0
▶ Ground Net	

- *RL VRM*, which is a 2-element model with a VDC source with a series resistor (R) and an inductor (L).



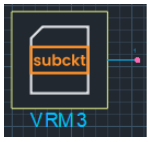
Name	Value
Block Name	VRM1
Nominal Voltage	1.0 V
▼ Power Net	
Net Name	PWR
# of Pins	1
Pin Name	pwr
R_VRM(Ohm)	0.5m
L_VRM(H)	50n
▶ Ground Net	

- *RL//RL VRM*, which is a 4-element model with a VDC source with a parallel combination of the series resistor and inductor as in the 2-element model.



Name	Value
Block Name	VRM2
Nominal Voltage	1.0 V
▼ Power Net	
Net Name	PWR
# of Pins	1
Pin Name	pwr
R_VRM(Ohm)	0.5m
L_VRM(H)	50n
R_damp(Ohm)	20m
L_VRM/10(H)	5.0n
▶ Ground Net	

- *Subckt VRM*, which is a subcircuit model based on a user-supplied netlist model for a VRM model.



Name	Value
Block Name	VRM3
Circuit File	vrm_Smith.sp