cadence®

Allegro X Layout Editor Environment Variables Reference

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Display Settings

3D

disable_3d_default_mask_layers	Set to stop showing 6 default mask layers (SILKSCREEN_TOP, PASTEMASK_TOP, SOLDERMASK_TOP, SOLDERMASK_BOTTOM, PASTEMASK_BOTTOM, SILKSCREEN_BOTTOM) in the board design if they are not defined in the stack-ups.
disable_3d_reference_geometry	Provide reference geometry to 3D canvas to save loading time. (::20%) and memory (::30%).
enable_3d_include_dfa_bound	Set to include both the Package Geometry/DFA_Bound class/subclass, and the Package Geometry/Place Bound class/subclass in the symbol shapes. Requires restart.
enable_3d_symbol_place_on_pastemask	Set to place symbols on the pastemask layer instead of the TOP and BOTTOM (or outermost) layers in 3D Canvas. Requires restart.
hide_unified_filter_dialog	Set to stop the 3D Canvas Unified Filter Dialog from being displayed.

Align Guides

align_guides	Set to show the "Alignment Guides" during move operations. Off by default. Variable name is align_guides.
align_guides_component_origin	Set to show the "Alignment Guides" when the Origins are aligned during move operations. On by default. Variable name is align_guides_component_origin.

align_guides_place_bound	Set to show the "Alignment Guides" when the place_bound extent of the components are aligned during move operations. Off by default. Variable name is align_guides_place_bound.
align_guides_ratsnest	Set to show the "Alignment Guides" when the ratsnests of the components are aligned during move operations. On by default. Variable name is align_guides_ratsnest.

Cursor

pcb_cursor	Choose a cursor type from infinite, cross (default), or octal. 'infinite' is two crossing lines, perpendicular by default, extending to the full display. Use pcb_cursor_angle to set the angle. 'octal' is four crossing lines, 45 degrees apart; the pcb_cursor_angle variable is not used.
pcb_cursor_angle	Specify the angle for the crossing lines of the infinite cursor (see pcb_cursor variable). Values are between 0 and 90. By default, infinite cross-hair is shown orthogonal.
pcb_cursor_color	If using the infinite cursor, specifies the RGB color value for the infinite cursor. By default, this is an off-white. Specify a value as three numbers, each 0-255, for the red, green, and blue values. An example string would be '255,255,255' for white or '255,0,0' for red.

Datatips

custom_datatip_remove_delay	Specify the duration after which a datatip should disappear. Value can be between 100 and 2000 milliseconds. By default, a datatip disappears 250 milliseconds after the cursor leaves an object. Value can be between 100 and 2000 milliseconds.
datatips_delay	Specify the delay after which datatip appears if the cursor remains in the same position. Value can be between 100 and 2000 milliseconds. Default is 250 milliseconds.

datatips_fixedpos	Set to display datatips above the command window. Can be set to be left, center, or right justified. By default, datatips appear next to the cursor.
disable_datatips	Set to disable context-sensitive datatips on hovering over data elements.
disable_hover_over	Set to disable dynamic highlighting and datatips that occur when you hover over elements in the display. Dynamic highlighting and datatips will still occur for application mode commands because they are needed for preselection preview.
focus_followmouse	Specify how window focus, hover-over highlighting, and datatip display should behave. Specify "allegro_derived" to enable highlighting and datatips when the canvas or sub-windows, such as Show Element, are in focus. Specify "anywhere" to enable highlighting and datatips regardless of focus. If not set, highlighting/datatips are enabled only when the canvas is in focus.

Element

etchlen_ignore_pinvia	By default, the etch length that is computed for show element and other commands will include via to via offset distances when a via or pin are directly connected. This makes this calculation agree with the delay calculations. Setting this variable will restore the older version of the calculation that excludes these offsets.
noshow_current_selections	Set to terminate any running command when show element is run. By default, if an interactive command is running, and there are some elements that currently are selected or highlighted (with temp highlight), running show element will result in a window displaying information for those elements while the other command remains active.

show_max_manhattan_pins	Set the threshold for maximum number of pins that a net can contain for which show element should display information. Value can be any number greater than 0. By default, show element does not display information when nets contain more than 50 pins for performance reasons. Not applicable for nets with NO_RAT property.
show_unique_pin_name	Set for show element to list the unique logical pin name in addition to the non-unique name. By default, only the non-unique name is shown.
showelement_autoavoid	Set to position the show element window to avoid the main window. By default, the previous location of the window is used on next open.
showelement_basearea	Specify the unit used by show element to display shape area. Choose 'traditional', which is the default, to report shape area in square inches if imperial or square centimeters if metric. Choose 'artwork' to report microns in square millimeters and everything else the same as traditional. Choose 'design' to report in current design units.
showelement_brief	Set to filter show element detail. Currently for shapes it filters boundary and void segments.
showelement_highspeed	Set for show element for nets to display in PCB SI format.
showelement_length_db_accuracy	Set to display length values for objects such as line segments with the same number of decimal places of accuracy as the design's accuracy. By default, this is display with an extra two places of accuracy.
showelement_xhatcharea	Set to report the actual area of cross-hatched shapes including cross-hatch lines. This calculation is time-consuming which is why it is not the default. By default, the cross-hatch lines are not considered when calculating the area.
showmeasure_altunits	Specify the units in which show measure displays measurements.

showmeasure_centerdist	If set, show measure additionally displays the center line distance (accounting for the line width) when lines, clines, or segments are selected.
showmeasure_layerrestore	Set for show measure to restore the active layer to the setting that existed at the start of the command. By default, a 'Done', leaves the active layer with its current setting.

General

display_backingstore	Set to store a copy of the screen in memory to avoid repainting when a form is closed or a window is moved. Supported only with X-windows (UNIX) and applies to drawing data, not forms. To set from the command line, type "backingstore".
display_mask_pads	Set to display pads on non-user-defined mask layers in addition to the first etch layer pad. By default, interactive commands, such as move and copy, display a pin or via's first defined visible etch layer regular pad. The first mask layer pad is only displayed if no etch layer pad is available.
display_no_auto_hide_boundary	Set to have the boundary layer remain visible unless manually toggled through the Display -> Color/Visibility form. By default, turning the visibility of an etch layer off through the options panel will automatically turn off the corresponding dynamic shape boundary layer.
display_no_pad_label_filter	By default, dynamic text labels on via and pin elements will be suppressed if they are below a given size threshold (and thus cannot be read). Enable this variable to continue to display the labels even at small size. The labels may be a means of determining what items are of a given type, not always a need to read the via span text label itself. This variable is independent of the size-based object filtering in the color192 form.

display_norepair	Specify elements for which to disable display repair. Options are rats or all. By default, display repair mode is enabled for all elements. For slower systems, setting this to "all" provides better performance but results in some graphics glitches. Leaving the variable unset results in the best display.
display_noskeletal_draw	Set to disable skeletal draw mode. Skeletal draw is used when very fast refresh of graphics is required such as dynamic zoom out mode.
display_raster_ops	Controls the use of raster operations to improve appearance of display features. The tradeoff is the use of additional system memory. Depending on your graphics hardware performance may be slow. For example, it greatly improves the look of the dynamic graphics. If set to "slow", features that require frequent use of the capability are not allowed to use it. The default is "on". In OpenGL this option may get turned off automatically if allegro display area is bigger than hardware supported storage mechanism. Making Allegro smaller should fix it.
display_refdes_subclass	Specify a subclass to display RefDes text on that subclass when a symbol is moved. If not set, or if text does not exist on the chosen subclass, priority of display will be assembly_top, assembly_embedded, assembly_bottom, silkscreen_top, silkscreen_bottom,display_top, display_embedded, display_bottom.

Highlight

disable_retain_custom_color	Set to specify the "Retain objects custom color" option in the dehighlight command to be Off by default.
display_nohighlight_priority	Set to ignore highlight and custom color display priority and display all elements based on layer priority only. It does not affect temporary highlighted elements. Environment variable name is display_nohighlight_priority.

display_nohilitefont	Set to display all highlighted elements with a solid highlight color. By default, highlighted elements are displayed with a combination of the highlight color and the element's original color (striped). OpenGL may not support striped highlighting at all zoom levels.
highlight_shape_net	Set to highlight the net associated with a selected shape.

Opengl

disable_gpu	Set to disable the GPU Plugin usage for Canvas rendering. If set, the default will be to use the regular OpenGL mode unless the disable_opengl is specified. If not set, then this becomes the default if your GPU is supported.
disable_opengl	Set to disable running in OpenGL mode.
disable_opengl_cache	Set to disable OpenGL performance boost in roam. Set this option if there are display artifacts while roaming. Caching makes heavy use of GPU resources. Your GPU capabilities dictate if caching should be disabled.
draw_etch_outline	Set along with the enhanced display option for connecting line end-caps to display wide lines with an outline.
gpu_delay_refresh_sg	This variable will delay the automatic refresh of the GPU Scene Graph when needed. The user will be informed with a message in the canvas and can refresh by using the redraw command of pressing F5.
old_grid_display	Set to enable the old grid display in OpenGL.
static_shapes_fill_solid	Set to disable fill pattern for static shapes. Static shapes fill the same as dynamic shapes.
viewer_useoglgraphics	Set to enable OpenGL in allegro_free_viewer. By default, the allegro_free_viewer disables OpenGL on Windows. Note the free viewer is an unsupported program, if any OpenGL issues are noted, discontinue use of this variable.

Roam

pcb_autoroam	Define the time interval, in milliseconds, between roam increments. If set to 1000, roam increments are 1 per second. Default value is 250 milliseconds.
roaminc	Define roam increments in pixels when using arrow keys to roam. For best performance set to multiples of 16. Minimum is 16 and maximum is 256 pixels. The default value is 96 pixels.

Seg_Over_Void

sov_active_only	Set for the Highlight SOV application to only consider the active layer instead of all layers.
sov_skip_plane_check	Set for the SOV application to skip check violation of partial/missing plane coverage.
sov_spacing	Specify a spacing parameter for the Highlight SOV application. A positive value indicates the minimum allowable spacing to an adjacent plane void. A negative value indicates allowable segment overlap onto an adjacent plane void.

shape_fill

display_shapefill	Specify the spacing in pixels for lines used to fill solid shapes and rectangles. Default is 4 pixels. This variable has no effect in OpenGL mode.
no_etch_shape_display	Set to NOT display etch shapes.
no_shape_fill	Disable filling solid shapes. If set shapes will drawn in skeletal mode (boundary only). Applies only to solid-filled shapes. Cross-hatched fill disable is via the no_shape_xhfill variable.
no_shape_fill_dyn_ood	Set to disable filling of dynamic shapes that are out of date. This variable can eliminate the need to move dynamic shapes off the design when disabling their fill mode.

no_shape_xhfill	Disable filling cross-hatched shapes. If set shapes will drawn in skeletal mode (boundary only). Applies only to cross-hatched shapes. Solid fill shape disable is via the no_shape_fill variable.
old_shape_fill_style	Set to fill shapes using old line fill style. By default, shapes are filled with a fill pattern bitmap. This variable has no effect in OpenGL mode.

Visual

display_custom_vis_layers	Set to control what layers are shown in the custom layers section of the visibility pane. By default, those layers added for the active design are shown. 'User' loads only active design's configured layers. 'Global' will load the layers set in all "CVCustomVisPaneLayers.xml" files in your pcbenv, ALLEGRO_SITE, and global env folders. 'Both' will load both active design and all global layers found. See <cdsroot>/share/pcb/examples directory for a starter file that can be copied into your environment and modified.
display_drcfill	Set to display DRC markers as "filled" butterflies.
display_dynamic_highlight	By default, when in an application mode, objects in the main canvas will highlight as you move your cursor over them. This shows the element that the datatip information is for, if datatips are enabled. It also shows what item will be selected if you click. This can lead to a strobe effect, most noticeable on large designs or when nets and shapes are enabled. To disable the auto highlighting, enable this variable. This has no impact on the datatip display ability or on the object which is selected.
display_etch_over_pad	Set to draw etch segments over pads on each layer. By default, pads are drawn over etch segments per layer. Environment variable name is display_etch_over_pad.
display_no_close_grids	Set to suppress grid display when zooming out reduces the ability to display grids at the spacing listed in the define grid form.
display_nocolor_dynamics	Set for the dynamic cursor buffer to draw the elements as white. When not set, the elements are drawn with their assigned color.

display_nodynamicarcwidth	Set, for performance reasons, to draw arcs and circles of one-pixel width when using interactive commands, such as move or copy. Unset to see correct width.
display_nolinewidth	Set to display all lines at a one-pixel width. This variable can increase performance at the expense of an accurate display. The default is lines at width. Note that dynamics drawing ignores this variable.
display_pinpair_connection	Set to mark differential pairs by drawing a line between associated pin pairs. This line is a visual indicator only. Note that this feature requires enabling Enhanced display mode "Diffpair drivers pins" in the Setup Design Parameters form.
display_readonly_intensity	Specify the display color intensity for disabled (readonly) database objects. By default, disabled objects are drawn at 40% intensity. Note that Shadow mode in Allegro does not affect disabled objects.
display_thintext	Set to restore release 13.5 behavior text spacing. Text is always drawn at one pixel width (ignores photoplot width).
old_style_flash_symbols	Set for Allegro layout editors to use non-WYSIWYG thermal flashes instead of WYSIWYG thermal flash symbols when creating new boards.
ratt_off_if_connected	Specify a value to control the visibility of Rat Ts that are fully connected (all of its ratsnests are connected). By default, a Rat T will remain visible when its ratnests are all connected. A value of "on" causes a fully connected Rat T to be invisible. A value of "unhighlighted" causes a fully connected Rat T to be invisible unless it is highlighted.

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Drawing Settings

Controls design access behavior typically at the global level.

allegro_long_name_size	Specify the maximum length of names in the design. Examples of long name types are (but not limited to); nets, padstacks, symbols, and function pins. The minimum value is 32 and the maximum is 255; the default is 255. The variable is only used when creating a new drawing. Existing designs have their name length managed in the Design tab of Design Parameters.
db_no_sector_retune_on_open	Set to stop retune sector map on opening.
db_no_sector_retune_on_save	Set to stop retune sector map on saving.
db_save_full_dbcheck	Specify how frequently full dbdoctor is run on saving a design. For example, a 2 means that a full dbdoctor will be run on every other save. By default, a quick design check is run on every save. Specifying this variable lengthens the time to save a design.
db_tier_nomsg	Set to stop the confirmation message when opening a design in a different product. You will still see a warning in the command area.
drawing_4mils	Set to allow a database in MILS to be set to an accuracy of 3 or 4 decimal places. By default, the maximum accuracy in MILS is 2. Using more than 2 decimal places of accuracy causes rounding issues when creating manufacturing data.
drawing_no_4mils_msg	Set to stop displaying a warning message in the drawing parameter form if accuracy is set to greater then 2 while using MILS.

filename_allow_brackets	Set to be able to open BRD, MCM, or SIP files that contain square brackets ([])or parenthesis (()) in filenames. Immediately save any file with these characters to a legal name. Setting this option is not recommended. Internet Explorer may add brackets to filenames if it detects that a download will overwrite an existing file.
legacy_character_set	Set to allow backslash () in net names, which is the pre-release 16.6 behavior.
multiboard_always	Set to automatically open a design link if one is currently associated with open design. By default, PCB Editor will not automatically open a system design link when a board is open while PCB SI will.
no_symbol_onsave	Set to stop creating a symbol file when saving a DRA file automatically. Create one manually using File-Create Symbol (create symbol). By default, on saving a DRA file, the symbol file is also created.
noconfirm_savedb	Set to overwrite databases without any warning messages while saving.
noconfirm_uprev	Set to stop displaying warning messages on opening drawings needing an uprev.
uprev_answer	Specify 'yes' to stop displaying the major release design uprev warning but to provide the default answer. Specify 'no' to stop opening designs from older releases using this method. Specifying 'no' disables the noconfirm_uprev environment variable.

New_design

allegro_new_accuracy	Specify accuracy for new board if design specific variable (for example, new_accuracy) is not specified.
allegro_new_units	Specify units for new board if design specific variable (for example, new_units) is not specified.

apd_new_accuracy	Specify accuracy for a new mcm if design specific variable (for example, new_accuracy) is not specified.
apd_new_units	Specify units for a new mcm if design specific variable (for example, new_units) is not specified.
cdnsip_new_accuracy	Specify accuracy for new SIP if design specific variable (for example, new_accuracy) is not specified.
cdnsip_new_units	Specify units for a new SIP if design specific variable (for example, new_units) is not specified.
new_accuracy	Specify accuracy for a new design if design specific variable (for example, allegro_new_accuracy) is not specified.
new_design_use_env_units	By default, when starting a new design in the layout editor, the units and accuracy are initialized from the previously-open design. Set this variable to override this behavior and use the values set at the environment level using the <toolname>_new_units and <toolname>_new_accuracy variables. If this variable is not set, or if the variables above are not set to values, then the last design's values will be used.
new_template_with_last_design	Set to restore pre-16.6 behavior for new designs to take their base characteristics (units, accuracy, and so on) from the previous design. Only the first design opened when starting the tool utilizes variables on that page or a new template design.
new_units	Specify the unit for new designs if design specific variable, such as allegro_new_units, is not specified.
padstack_editor_new_accuracy	Specify accuracy for a new padstack if design specific variable (for example, new_accuracy) is not specified.
padstack_editor_new_units	Specify units for a new padstack if design specific variable (for example, new_units) is not specified.

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DRC Settings

Delay

include_comp_delay	Set to include the delay of components in a path in a path delay when the path delay is computed to check propagation delay and relative propagation delay constraints. The delay of the component is determined from a transmission line (TL) statement in the ESpice model assigned to the component. If there is no assigned model or the assigned model contains no TL statement, no delay is included for the component.
include_terminators	Set to include the terminator length in the calculation ofdelay across an entire net. The standard check for delay across an entire net does not include terminators.
pre_12.0_delay_rule	Set to use the delay rule values as a length checker and the min and max delays to be a tolerance across the entire net as done in releases earlier than 12.0. By default, the checker checks the min delay value against the shortest pin pair, and the max delay value against the longest pin pair.
use_accurate_delay_calculation	Set for a more accurate modeling of power and ground shapes when computing impedance and delay. Instead of modeling the planes as perfect shields with no holes or cutouts, the actual outline of the shapes with all holes and cutouts are considered. The performance of the impedance, propagation delay and relative propagation delay constraint checks can be slowed when this more accurate calculator is used. Also, the Shield flag must be turned off on every plane layer.

DesignTrue

allow_acid_trap_on_thermal_spoke	This variable can be used to direct the tool to report acid trap violations on positive thermal spoke connections with a shape. By default those DRCs are not reported.

General

cns_threads	Limits number of DRC threads when drc_single_thread is disabled.Threads actually employed will not exceed system limitations.
cns_via_match_count_all	Set to do matched via count constraint check on partially connected nets.
drc_ignore_cline_end_filter	Restores pre-16.0 behavior with respect to cline endcap DRC when they end in a pad. In the current model, the endcap is ignored if it is smaller than the pad. In the old DRC model the cline endcap is always considered in DRC. This variable is NOT recommended since both etch editing and the auto-routers only use the new endcap model. The old model produces more DRCs.
drc_single_thread	Set to restrict drcupdate and dbdoctor to a single thread of execution on a multiple CPU system. This variable has no effect on a single CPU system. In pre-17.2 releases, this was called cns_single_thread.
dyn_phase_canvas_display	Set to display dynamic phase control delays as graphic text. Suggestion is to leave this option off except when debugging nets with difficult dynamic phase errors. Alternatively, you can set it as a teaching aid. When enabled, the display can become very busy with a large number of phase text errors from adjacent nets.
external_drc_reuse_layers	Set to reuse layer names for DRCs if you use a single source for sign-off violations. By default, APD DRCs are assigned to unique layer names under the MANUFACTURING class because external DRCs might come from multiple sources and represet different checking requirements.

same_net_traps	Set to check for small segment jogs. This spacing check is not intended for any angle data. It checks for this geometry at angles divisible by 45 degrees.
same_net_vias_shape_connect	Set to filter same-net vias sharing mutual shape connections.
wire_finger_same_profile	Set to restrict the wire-to-finger spacing constraint to fingers with wires of the same profile.

Schedule

sched_drc_output	If set, enables net schedule debugging on class Analysis, subclasses Anl_*connect. Run Show Element on a Net Schedule DRC to trigger.

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File_management Settings

script_nobuffer	By default, when a script file is being written, the output is buffered for improved performance. If the software crashes, or you need to see the script as it is being written, it may be empty until you stop recording. Set this variable to unbuffer the output and flush to the file on every new line. This ensures as many commands run as possible are present in the script if it is ended early.
temp_filename_prefix	Prefix used for temp files. By default, Allegro uses #T as the prefix. Some file systems and repositories do not allow specific characters in names. If yours does not allow #, set this variable. Recommend keeping this string short but identifiable. Requires restart to take effect. No characters not legal for file names permitted.

Autosave

autosave	Set to enable autosaving. Must be set/unset before starting the layout editor.
autosave_dbcheck	Set to run a quick database check before an autosave. Turned off by default to save time. Requires a restart.
autosave_name	Specify the base name for the autosave file. The default is AUTOSAVE. Do NOT provide a file extension. The layout editor will use the appropriate extension for the type of database under edit. Requires a restart.
autosave_time	Specify the autosave intervals. The default is 30 minutes. The minimum is 10 minutes and the maximum is 300 minutes. Requires a restart.

Journals

journal_nobuffer	Set for unbuffered output of journal files so that if a program crashes, more lines are written to the journal file. By default, the journal file has buffered output to improve performance when writing the file over a network.
journal_prefix	Specify the prefix for the journal file name. Three special prefix keys are available; "user" substitutes user's login, "host" substitutes system name, and "unique" creates a unique filename based upon host, user, and process id. Prefix must be a legal file name (no / or:).

Miscellaneous

allegro_nolocking	Set to disable advisory file locking (pre-16.5 behavior) so that file locks will not be created when you open designs, but you will be notified of locks created by other users. By default, Allegro programs create a lockfile when a design is opened. This allows other Allegro programs to sense that the design is in use.
directory_cache	Set to ignore fully qualified directories in Allegro PATH variables that do not exist. These directories when located remotely can have slow access. The bad_directories command lists these directories but requires you to use Allegro layout editors with features that use the PATH variables.
ecadmcad_status_update_interval	Specify the update interval of ECAD/MCAD status. The default is 1 minute. The minimum is 1 minute and the maximum is 30 minutes.
import_file_alarm_enable	Set for import file alarms. It must be set/unset before starting Allegro.
import_file_alarm_interval	Specify the import file alarm interval. The default is 10 minutes. The minimum is 1 minute and the maximum is 720 minutes.
temp	Specify the path to a location with free space to be used for temporary storage of data files. Most often, artwork requires more temporary space than the /tmp directory contains. By default, Allegro layout editors use the OS environment variable TEMP with a fallback to TMP.

Output_dir

ads_sdart	Specify the subdirectory to which artwork (Gerber), drill files and ipc2581 are written. Default is the same directory as the design.
ads_sdlog	Specify the subdirectory to which log files should be written.
ads_sdmcad	Specify the subdirectory to which IDF and IDX files are written. Default is the same directory as the design.
ads_sdplot	Specify the subdirectory to which plot files should be written.
ads_sdreport	Specify the subdirectory to which report files should be written.
dump_library_directory	Specify the export directory to be used by Export Libraries (dlib UI command). Default is the current directory. Location may be a relative or an absolute path. Command attempts to create the rightmost directory component if not present.

Pulse

allegro_pulse_enable	Set to enable the Pulse version control feature for the layout editor. When set, Pulse will automatically start on the next tool launch and is indicated by the Pulse icon in the system tray. Hover over the icon to check that its status is RUNNING - indicates that Pulse services are available. Once available, the Commit, Version Control, and Copy As entries under the File menu are enabled. Enabling Pulse increases memory consumption. The recommended minimum hardware required to run Pulse is 8GB of RAM and 4 CPU cores. Pulse is not available in the Allegro Artist or OrCAD PCB products.

Versioning

ads_autosaverevs	Specify the number of versions you want maintained for AUTOSAVE database files. Default is no versioning.
ads_boardrevs	Specify the number of versions you want maintained for Allegro layout files, (.brd) and symbol (.*sm). Default is one version.

ads_logrevs	Specify the number of versions you want maintained for Allegro layout editor log files.
ads_textrevs	Specify the number of versions you want maintained for Allegro layout editor files that are not .brd .*sm or .log.
ext_artwork	Specify the file extension used for artwork (film) files. Default is .art. Recommendation is to set this at the CDS_SITE level. Use caution before changing the extension to ensure all your post-processing tools can handle the new extension.
ext_drill	Specify file extension for ncdrill files. Default is .drl. Recommendation is to set this at the CDS_SITE level. Use caution before changing the extension to ensure all your post-processing tools can handle the new extension.
ext_script	Specify extension used for Allegro layout editor scripts. Default extension is .scr. Recommendation is to set this at the CDS_SITE level.

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IC_packaging Settings

3d_view_soldermask_default	Set to render soldermask layers in 3D Viewer by default. This will set 'Render solder masks' in the 3D Viewer Design Configuration form.
3dv_hatch_shapes_as_solid	Set to export cross-hatched shapes as solid filled shapes in 3D Viewer. By default, cross-hatched shapes are exported with all hatched voids intact causing the size of the 3Di database to grow, and the rendering performance to decrease for large designs.
allegro_component_alt_via_delay	Set to use a method similar to the 'Report' - 'Conductor Length Report' ('cond len report') command when generating delay reports for the placement of a package on PCB using the 'File' - 'Export' - 'Board Level Component' ('allegro_component') command. By default, via delay computation method is used.
allegro_component_seq_pin_names	Set to generate a pin name based on a unique sequential index instead of the pin number to ensure unique pin names when generating a component for placement on a PCB using the 'File' - 'Export' - 'Board Level Component' ("allegro_component") command. By default, the net name is combined with the pin number to generate unique pin names.
apd_verilog_include_voltage_nets	If set, Verilog files exported from APD or SiP using the verilog out command will include the power and ground nets. By default, only signal nets are included in the output. Power nets will be exported using supply1 while grounds nets will use supply0.

auto_assign_no_pinuse_warn	Set to disable the warning dialog shown the first time in a given tool session that you run the 'auto assign net' command and enable either the power/ground or pin reassignment allowed options.
auto_assign_no_schedule_update	Set to disable rescheduling by 'auto assign net' of impacted nets based upon the results of assignments. You can then keep the default scheduling pattern or apply your own custom scheduling.
degas_layer_types	Specify which layers in the cross-section should be considered to determine odd and even layers. The valid values are
die_replace_retain_nets	Set to assign package nets of the die being replaced to pins of the replacing component that do not have nets assigned. By default, when performing die replacements using any of the import commands such as die text in, def in, co-design die eco, and so on, if a pin in the new component has no net assigned and was not previously routed, it will remain on dummy net to abide by the configuration just imported.
display_pin_text_separator	Specify a character to be used to separate strings in a display pin text label that is composed of multiple values appended together with the append to existing label option. The default value is a space. Specify '_', '-', or other characters to meet downstream requirements.
dpn_dummy_net_string	Specify the net label for any objects not assigned to a real net when adding text labels with the "display pin text" command. For example, set this to "NC" and any dummy net pin, for a net label, will use "NC" instead of an empty string.

ground_net_regex	Specify a regular expression to categorize any net created in the design matching the regular expression as a ground net. This means the net will get a VOLTAGE and NO_RAT property, and will have its ratsnest schedule set to power and ground. You can modify these properties after creation, but allowing the tool to perform initial cataloguing improves performance on large designs. String supports * and ? for wildcard matching and | between wildcard strings.
icp_allow_adjacent_conductors	Set to enable adjacent conductor layers not separated by a dielectric layer. Any dielectric layers that are present in the manufactured part need to be in the cross-section for accurate extraction, 3D viewing, and so on. Objects on adjacent conductor layers do not automatically electrically connect together and a via must be used to establish inter-layer connections. By default, a dielectric must separate each pair of conductor layers in the cross-section of your design.
icp_chamfer_all_symbols	Set to create an orientation marker line in the form of an angled line in the bottom left corner when creating a BGA symbol, similar to the one created for Die Symbols.
icp_dbdoctor_on_component_edit	Set to scan the IC Packaging database for possible errors each time the editor is launched, to ensure no data is lost. The Die and BGA Editor environments allow editing of component and symbol instances and definitions for these objects directly within the owning database. These functions can unmask problems which may have been latent in your database before the tool is invoked.

icp_default_attach_wirebond	Set to import dies as wire bond and place them chip-up without mirroring when placed on cursor. By default, when a die is brought into the netlist, using commands such as Import Logic (netrev or netin) or Edit Parts, and no specific die attachment method is specified, die symbols will be defaulted as flip-chip dies and Place Manually will place them chip-down. The symbol brought in from the library will be mirrored when placed on the cursor.
icp_derive_assign_default_value	Set to configure the default settings for the 'derive assignment' option in commands such as the die and BGA text-in wizards. By default, the option is enabled. This preference enables you to change the default setting of the option on the forms. This may be overridden by the user when running the commands interactively.
icp_disable_cte_auto_update	Set to ignore CTE compensation setting of the die being replaced using any of the import commands such as die text in, def in, and so on. By default, if CTE compensation settings are defined and applied to the component, it will apply the same settings to the imported component.
icp_ic_class_not_die	Set to treat only components with a DIE_COMPONENT user-defined property as bare dies. For example, to list only these in the die-stack editor. The variable does not affect existing designs. Set this variable if you share libraries with a PCB design team. By default, the component class "IC" is reserved for flip-chip and wire-bond style bare die in the IC Packaging tool.
icp_layer_compare_default_operations	Specify the default boolean operations to use if none are specified for the batch layer comparison tool. This should be a list of operation names, separated by spaces. Accepted values are AND, OR, XOR, MANDNOTC, and CANDNOTM. If not set, default operations are AND, MANDNOTC, and CANDNOTM.

icp_netlist_spreadsheet_no_pg_nets	Set to suppress the writing of power and ground nets to spreadsheet files generated when using the "netlist spreadsheet" command.
icp_shrink_nosave_original_symdef	Set to prevent saving the original definition of an object when applying shrink to it. By default, the pre-shrink definition will be retained in the design. This is to allow you to move back to the original and see the die as it exists in the IC design space. However, this will increase the database size to store two versions of the definition.
icp_unique_outline_layer	Set to have each die's place bound shape automatically copied to a unique COMPONENT_GEOMETRY layer named after the die's reference designator. This allows for better visualization of the dies and easier export to manufacturing and documentation formats. By default, all die outlines in a package design are created on either the place bound top or bottom layer, depending on which side of the substrate the die attaches to. For stacked die designs, this can lead to multiple, overlapping die outlines which are hard to differentiate.
metal_usage_report_die_layers	Set to list non-substrate layers in metal usage reports in the IC Packaging tool. For example, for designs having package-level redistribution routing on one or more diestack layers. By default, the metal usage report shows only the substrate layers and soldermask top/bottom.
metal_usage_report_noarcs	Set to ignore arcs when generating the metal usage report to avoid inaccuracies for designs having very small arc segments. By default, the metal usage report generates the most accurate results possible, using the exact shape of objects in the design. In situations having very small arc segments, this can lead to rare occurrences of inaccurate results.

pad_repl_use_new_padlayer	Set to use the pad-layer of the replacement padstack when replacing padstacks involving die-layers. By default, the pad-layer of the padstack being replaced is retained.
pbar_outline_width	Specify the outline boundary width of plating bars. You must specify the value and its unit. By default, plating bars are created with an outline boundary line width matching the min line width on the top conductor layer of the design.
pbar_trace_no_fillet	Set to exclude plating bar traces from getting dynamically filleted. By default, plating bar traces are dynamically filleted.
power_net_regex	Specify a regular expression to categorize any net created in the design matching the regular expression as a power net. This means the net will get a VOLTAGE and NO_RAT property and will have its ratsnest schedule set to power and ground. You can modify these properties after creation, but allowing the tool to perform initial cataloging improves performance on large designs. String supports * and ? for wildcard matching and | between wildcard strings.
wirebond_report_include_pins	Set to include pins without any bond wires connected in the wire bond report.

Codesign

clm_default_min_die_pin_height	Specify the minimum die pin height. When adding or editing a die, the minimum size of the die pin is defined by the width and height of the pin.If a value is not set, a default value of 25 x 25 um is used.
clm_default_min_die_pin_width	Specify the minimum die pin width. When adding or editing a die, the minimum size of the die pin is defined by the width and height of the pin.If a value is not set, a default value of 25 x 25 um is used.

codesign_delay_drc_checks	Set to delay DRC checking of the co-design die in the co-design flow when this delay will be most noticeable. When adding or editing a co-design die, if your DRC constraint values are not properly configured, this could result in many DRC errors being flagged which may not be actual errors.
codesign_restore_pin_padstacks	Specify how pin padstacks are preserved after an edit of a codesign die has completed. Specify blank or "default" to use the existing pin padstack if the pin on the die has a pad within the package substrate. Specify "always" to preserve the pin padstack of the existing pin. Specify "never" to to load pin padstack from the CML file.
die_abstract_read_verbose	Set to see unknown XML tags and warnings when reading a die abstract, such as when developing your own abstract reader/writer.
sipiop_no_padstack_reuse	Set to create a new padstack definition for each cell definition.This will result in more padstacks in your database, but easier identification of the source cell and customization of the package-side padstack. By default, when adding a pin, padstack definitions in the database completely matching the pad size, shape, and layer characteristics for the pin's library cell definition are used.

Die_symbols

icp_disable_auto_symbol_lock	Set to disable automatic locking by the IC Packaging tool. By default, the IC Packaging tools maintain the locked property on all die symbols in the design, to prevent a user from inadvertently modifying them.
icpkg_unplace_comps_on_delete	Set to retain the logical component associated with a symbol instance (die or package) when the symbol is deleted. By default, logical component as well as the physical symbol are deleted.

Early_adopter

_dxf_out_merge_polygons	Set to enable an option on the DXF out GUI to merge all overlapping objects on each DXF layer prior to writing the data. For example, a cline routed to a pin is normally two objects in the output file. With this option enabled, they are combined into a single outline. Only available when writing DXF in revision 14 with block output for symbols and padstacks disabled. Available in all products which include the dxf in and out commands.
_stream_out_always_flatten_odd_rot	Set to flatten objects placed at odd angles, even if the flatten geometry option is disabled. When generating stream data for consumption by certain tools, most commonly IC-based tools, objects placed at a non 90-degree rotation need to be flattened.
_stream_out_merge_polygons	Set to enable the option on the stream out GUI to merge all overlapping objects on each stream layer prior to writing the data. For example, a cline routed to a pin is normally two objects in the stream file. With this option enabled, they are combined into a single outline. Only available when writing stream file with flatten geometry option. Available in all products which include the stream in and out commands.
cline_change_width_vias_beta	Set to enable the option to create vias at the dangling ends of clines when removing pieces of the clines. This will also add the "retain net on vias" flag on the owning nets. Combined, this option and the vias allow the dangling clines to retain their original net instead of reverting to not a net or being connected to a shape in the same region. Available in all products which include the cline change width command.
disable_tools_beta_functionality	Set to hide the "Unsupported Prototypes" Submenu in the "Tools" Menu. The commands available through the "Unsupported Prototypes" menu are of Beta quality and CCRs filed against them will not follow standard Cadence CCR policy. Internal environment variable name - disable_tool_beta_functionality.

dxf_out_derived_outlines	Set to generate unfilled objects to the specified DXF layer, when generating a dxf file with "dxf out" in Revision 14 and with filled pads or shapes enabled. An additional, derived layer (F_) is automatically created with the filled outline for those filled objects. This allows the person looking at the DXF to control whether the objects are shown as outlines or as solid shapes, without having to generate multiple files. Available to all products which include the dxf out command.
icp_crosshatch_void_fill_beta	Set to enable the "crosshatch void fill" command, which allows you to select a cross-hatched shape and add small shape overlays to fill any partial voids occurring in the hatching of that shape, such as near a corner or around a connected via or pin pad. This command is available from the 'Shape' - 'Cross-Hatch Void Fill' menu item.
icp_daisy_chain_beta	Set to enable the "daisy chain create" command (and add menu item under the Route menu on next tool restart). This "daisy chain create" command allows you to create simple daisy chain patterns of net assignments and routes for entire components, or sets of pins, specified. This is done by pairing neighboring pins together onto two-pin nets named based on the pin numbers and, if requested, adding a simple routing cline between the two pads.
icp_fillet_corners_beta	Set to enable the "fillet corners" command, which adds extra cline segments at bends in cline corners to improve manufacturability when cline tapers cannot be used.
icp_generate_rsf_beta	Set to enable the "generate rsf file" command line command that generates an RSF file from a source front-end netlist psdxprt.dat file for use with the "film res" command.
icp_layer_doc_beta	Set to enable the "layer doc" command that creates a graphic representing the cross-section and die stack ordering used to generate documentation for manufacturing.

icp_merge_shorted_nets_beta	Set to enable the "merge shorted nets command" that works similarly to the "rename net" command, except that it looks for all NET_SHORT properties in the database and, for those, merges the referenced nets into a single net object. At the end of this process, it removes the NET_SHORT properties. You are left with a database where all shorted nets are now single, large nets.
icp_mesh_pads_beta	Set, when using the unsupported prototype "mesh pads" tool, to draw the mesh openings on the screen (when the mesh pad layer itself is turned on in the color and visibility form). By default, these holes are not displayed for performance reasons. This is available when accessing a database containing mesh pad information.
icp_short_risk_report_beta	Set to enable the "short risk report" command, which identifies the BGA balls in a report for which there is a risk of the net shorting to neighboring nets. Some manufacturing groups request this report to improve test quality on the manufactured parts.
icp_soldermask_allow_pins	Set for the soldermask creation tool to allow selection of pins in addition to bond fingers and vias. The default for pins is disabled, and they must be turned on in the find filter to allow selection. This may be useful for generating openings for flip-chip bump arrays, discrete components, and certain other types of surface-mounted devices. Setting this variable enables pins for activation in the find filter the next time the command is run. Available to all products which include the bond finger soldermask command.
ncdrill_real_start_layer	Set to generate NC data with layer 1 being the first layer of the package substrate. By default, NC output data is based off layer 1, being the first layer in the design. In a design with two DIE / DIESTACK layers above the top substrate layer, NC output will have the top substrate layer as layer 3 by default. With this variable set, it will be layer 1. Changing this variable requires that you regenerate any existing drill and drill legend information for your designs.

packinteg_via_stack_align_beta	Set to enable an additional check in the Manufacturing category of the Package Design Integrity tool to look for stacks of vias where the via origins are not aligned. It is possible for this tool to correct the issue and align all the vias. Any misaligned vias will be moved to the same XY location as the top via in the stack, stretching clines to maintain connectivity.
shape_zigzag_beta	Set to enable the "shape zigzag" command if you have an SI Layout option license checked out. This command is a work in progress implementation for automatically adding bends to long edges of poured shapes to improve manufacturability and reliability. It is available from the 'SI Layout' - 'Shape Zig-Zag' command.
symed_codesign_convert_beta	Set to show "Change co-design level" pop-up option in the "Symbol Edit" app mode for a selected component. This option shows the current co-design status of the component and allow you to change to another available level based on your current product licensing.
symed_codesign_driver_place	Set to show pop-up options for placing unplaced drivers (when any exist) for a co-design die under edit, and to show the unplace driver command when a driver is directly selected. Available only in co-design IC packaging products which include the "Symbol Edit" application mode.
symed_ic_details	Set to show the "Show IC Details (View Only)" pop-up option in the Symbol Edit application mode. Depending on your additional settings, RDL routing, Drivers, and Shapes will be displayed as shapes on COMPONENT GEOMETRY layers. Choose the "Hide IC Details" on the same die component a second time to remove displayed items. Available in all IC Packaging tools which provide access to editing of distributed co-design die components.

symed_ic_details_drivers	Set to show a read-only view of the (placed) I/O drivers when the symed_ic_details_beta variable is enabled. Outside of the Die Editor command, the drivers will be shown on the COMPONENT GEOMETRY/DRIVERS layer, where you can get information about them, but any changes you make will not be preserved.
symed_ic_details_routing	Set to show a read-only view of the RDL routing when the symed_ic_details_beta variable is enabled. Routing will be created on COMPONENT GEOMETRY layers named _RDL, where is the layer of the RDL routing indicated in the die abstract. Click on a routing shape to see a property showing its IC net assignment.
symed_ic_details_shapes	Set to show a read-only view of the IC shape objects when the symed_ic_details_beta variable is enabled. Shapes will be created on COMPONENT GEOMETRY layers named _SHAPE, where is the layer of the shape indicated in the die abstract.
symed_rdl_on_pad_layer	Set, in conjunction with the "symed_rdl_display_beta" user preference, for the RDL routing shapes to be drawn on the selected die's pad layer instead of on the MANUFACTURING/RDL layer. Additionally, you can set this variable to a value of "CLINES" to experiment with seeing the RDL drawn as cline objects instead of as shape outlines.
symed_reusable_library_die_beta	Set to show the pop-up options in the symbol edit application mode for writing a library symbol. Three options for writing a library symbol are shown.
wb_tiered_sorting_beta	Set for the wire bond dynamic finger labeling algorithms to look for a user property, WB_PATH_TIER_INDEX, on each finger's associated guide path. This will be used in computing the sorted order for the fingers. All fingers are still sorted radially per the global configuration, except with the additional pre-sorting to group by tier index.
wirebond_dynamic_interposer	Set to add/manipulate bond fingers on a die stack layer when using the wire bonding commands. These fingers are designed to be converted into an interposer object when die stack construction and bonding are complete.

wirebond_label_add_missing_text	Set to add text label to fingers missing one based on the text settings found on other bond fingers in the design when dynamic bond finger labels are updated. This removes the extra step of using the display pin text command to create label text for each newly created bond finger.
wirebond_olp_beta	Set to enable the "olp export" command, which generates wire bonding manufacturing information for the active drawing. Information includes DXF files showing wires and fingers and XML files of profile definitions. A separate set of files is generated for the top and the bottom sides of the substrate, as these must be done separately by the bonding machine.
wirebond_rat_tees_beta	Set to enable the "wirebond rat tees" command. This command allows the you to add/delete rat tees at bond finger origins. These rat tees are moved during push and shove operations in the wirebond commands, and may provide a more accurate display of rat lines for signal nets of a wire bonded design.
wirebond_update_inst_beta	Set to enable the "wirebond update instances" command. This command allows you to refresh all instances of a wire bonded component based on the selected instance. It is available from the 'Route' - 'Wire Bond' - 'Update Instances' command or from the "Wire Bond Edit" application mode pop-up option with a reference component selected.

Manufacture

dxf_bond_finger_class	Set to control and export bond fingers using the BOND FINGER class. By default, bond finger objects in IC Packaging designs are exported to DXF as via objects using the "VIA CLASS" class.

dxf_suppress_wire_vias	Set to suppress connecting via objects when exporting bond wires to DXF from the IC packaging layout tool. By default, when a bond wire is exported to DXF, a via with the same diameter as the wire is placed at each end to connect the wire to the start and end items.
stream_drill_class	Set to enable a VIA_CONN class in the conversion file and its editor in stream out, where you can select layer pairs. Drills between these layers will be output on indicated stream layer. By default, via drill information is not written to stream files.
stream_in_no_shape_warnings	Set to suppress messages during stream in about self-intersecting boundary outlines. These outlines must be converted to positive shapes with voids in the Allegro tools. In most cases, the tool which generated the GDSII file will support creating non-intersecting boundaries and changing that setting will be most efficient. However, Allegro tools will correctly import these outlines after converting them to outlines with voids.
stream_out_hierarchy_relative_symbol	Set to stream out symbol instance relative to its definition. absolute_cells:Specifies that each symbol instance is a unique_cells and has absolute path. unique_cells:Specifies that each symbol instance is a unique cell in GDSII structure. template_cells: Specifies that symbol instance would be a unique cell only if the instance differs from its definition. By default, template_cells would be used.
stream_out_no_abs_rotation	Set to force stream out not to set absolute rotation flag in GDSII file. The absolute rotation flag might be reported as an error by signoff tools.

Package_integrity

packinteg_d2d_wire_count_all_pins	Set to count bond wires for both pins in a die to die bond. By default, a bond wire is only counted once with the die that it begins from (normally the higher die in the die stack).
packinteg_logic_include_drilled_pads	Set to include drilled pads in Logic category checks in package integrity. By default, the these package integrity checks only look for padstacks with no drill diameter defined.
packinteg_logic_nowarnings	Set to suppress generated warnings and info entries with all the package design integrity logic checks. Only errors will be reported.
packinteg_merge_segs_allow_drc	Set for the extra cline segments check in the package integrity tool to merge cline segments even if they might result in new DRCs. By default, it will not merge segments if the result will cause any new DRCs in the database.
packinteg_redundant_via_tol	Specify a tolerance distance (with units, if desired) within which vias will be considered redundant by the redundant padstacks check in the package integrity tool, which looks for unnecessary vias added to the design during its development. By default, only vias with identical origins are considered redundant.
packinteg_viapin_max_offset	Specify the maximum distance from the pin origin to the via origin before vias stop being snapped to the pin. By default, the via-pin alignment integrity check snaps all vias to the pin origin if the two are physically connected.
packinteg_voltage_nets_min_pins	Specify the pin count threshold to be considered high by the unidentified voltage nets check in the package integrity tool that looks for nets in the current drawing with a high pin count and possibly missing either VOLTAGE or RATSNEST_SCHEDULE properties. The default pin count threshold is 20 pins.

Reports

cond_length_report_2d_wires	Set to use 2-dimensional length of bond wires in the conductor length report. By default, the conductor length report uses the true 3-dimensional length of bond wires, based on the wire profile definition assigned to the wire.
cond_length_report_alt_plating	Set to compute plating trace length based on any cline connected to a plating bar for the conductor length report. By default, the conductor length report computes plating trace length based on the portion of clines which extend outside the package outline.
cond_length_report_alt_vias	Set for the conductor length report to consider the length of a via to be the difference between the bottom of the top pad layer and top of the bottom pad layer for the via, similar to other reports, such as delay report of the board-level component command. By default, the conductor length report adds the thickness of outer layers the first time they are used.

Symbol_editor

symbol_editor_hud_pin_use	Set to determine the use of a pin as power, ground, signal, or unassigned based on the specified pin use regardless of net assignment. By default, the heads up display of the symbol edit application mode uses the net assignment information of a pin to determine the use of a pin if a net is assigned and the specified pin use is only used for dummy net pins.
symed_allow_coincident_pins	Set to allow multiple pins with unique pin numbers to share the same locationin the symbol edit application mode. By default, the symbol edit application mode does not allow multiple pins to share the same coordinate.
symed_allow_locked_comp_edits	Set to allow editing of locked symbols in the symbol edit application mode. By default, symbols with the LOCKED property cannot be edited to prevent accidental modification of library symbols while still allowing the symbol to be edited (instead of used the FIXED property).

symed_allow_overlapping_drivers	Set to allow two overlapping drivers in a co-design die in the symbol edit application mode.
symed_dblclk_codesign_die_op	Specify the command to run when a co-design die component or symbol is double-clicked in the symbol edit application mode. Available option is 'toggle ic details'. By default, the pin is selected but you need to choose the action from the popup menu.
symed_dblclk_comp_op	Specify the command to run when a component or symbol is double-clicked in the symbol edit application mode. Available options are 'add pin', 'add grid', 'add keepout', 'edit text', and 'edit boundary'. By default, the pin is selected but you need to choose the action from the popup menu.
symed_dblclk_driver_op	Specify the command to run when a co-design die driver cell is double-clicked in the symbol edit application mode. Available options are 'align', 'move', and 'swap'. By default, the pin is selected but you need to choose the action from the popup menu.
symed_dblclk_grid_op	Specify the command to run when a pin placement grid rectangle is double-clicked in the symbol edit application mode. Available options are 'change pitch' and 'change numbering'. By default, the pin is selected but you need to choose the action from the popup menu.
symed_dblclk_pin_op	Specify the command to run when a pin is double-clicked in the symbol edit application mode. Available options are 'change', 'move', 'delete', 'swap', and 'copy'. By default, the pin is selected but you need to choose the action from the popup menu.

symed_disable_ic_net_dynamic_labels	Set for OpenGL dynamic text labels for a co-design die, when IC details are showing, to show the unprocessed temp net names in the database. Useful if you experience performance issues (you can also turn off the labels entirely through the Setup -> Drawing Options command). By default, OpenGL dynamic text labels show the IC net name for the IC footprint pins and driver pins.
symed_disable_snap_messages	Set to disable messages in the symbol edit application mode when a pin is placed at a location other than the point you specifically selected in the canvas. This happens because the pins are being snapped to a pin grid defined on the definition of the symbol under edit.
symed_drag_driver_op	Specify the command to run when a co-design die driver cell is dragged in the symbol edit application mode. Available option is 'move'. By default, the pin is selected but you need to choose the action from the popup menu.
symed_drag_pin_op	Specify the command to run when a pin is dragged in the symbol edit application mode. Available options are 'move' and 'copy'. By default, the pin is selected but you need to choose the action from the popup menu.
symed_pin_names_for_voltage_pins	Set to associate power and ground pins with pin names that you specify. By default, power and ground pins are not associated with pin names.
symed_refresh_padstacks	Set to ensure that the padstack definition of a pin matches the macro library data for the co-design die in refresh die abstract. By default, the symbol edit application mode maintains padstacks customized in the database.

symed_update_all_comp_inst_nets	Set to sync net assignment for corresponding pins of the pin being edited on all instances of the component in the symbol edit application mode. This is particularly useful when designing a redundant stacked memory module, where each instance should be identical to all others. By default, the net assignment for pins of the component instance actively being edited is updated.

Wirebond

wire_profile_ui_default_height	Specify the value for the sample wire start height of the bond wire 3D profile editor. If no units are specified in the value, the current drawing design units are used. Default is 200 um.
wire_profile_ui_default_length	Specify the sample wire length of the bond wire 3D profile editor. If no units are specified in the value, the current drawing design units are used. By default, the current drawing's maximum wire length constraint value is used.
wire_profile_ui_points_in_rows	Set for the bond wire 3D profile editor to reorient the grid on the form so that a point of the model is one row in the grid instead of one column. By default, the points of the model are displayed with one point in each column of the form's grid.
wirebond_auto_ring_pad_diameter	Specify the diameter of automatically generated padstacks for connections to power/ground rings (WB_TACKPOINT). If no units are specified in the value, the current drawing design units are used. By default, padstack will be created with the smallest diameter possible as the pad does not exist in the final design.

wirebond_center_ring_bonds	Set to run a post-process step to attempt to center power and ground wires between adjacent wires on both sides after doing wire bond movement operations, such as additions and movements, to improve manufacturability of the design. Setting this variable may cause a slight performance decrease during interactive wire bonding. Wire bond movement operations place power and ground ring bonds at minimum clearance to one adjacent wire bond.
wirebond_center_same_profile	Set to consider only wires with the same wire profile when centering bond wires between adjacent wires. The default behavior is to use the next wire bond found on any wire profile.
wirebond_cns_nodescription	Set to hide descriptions and images related to constraint behavior from the wire bond constraint settings window to reduce its size.
wirebond_deassign_on_wire_del	Set option primarily for feasibility flows to delete the last bond wire connected to a finger to deassign the net that was on the finger (and all items connected to it). This allows for an easy flow of wiring a pin to the finger, deleting the wire, and then wiring it to a pin on a different net. With each step, the connected BGA ball is kept up to date with the new net assignment.
wirebond_display_old_draw	Set to highlight only affected wire bonds during the push and shove operation. By default, all wire bonds are highlighted because the wire bond tool attempts to redraw all wire bonds on the same side of the die during a push and shove operation to minimize screen flickering.
wirebond_fast_draw_stubs	Set to only refresh routing stubs that are modified during push and shove operation. The clines are fully drawn again once the operation is complete. By default, for a move operation in the wire bond commands when the fingers are already routed on the package substrate, the routing stubs are updated along with the finger locations.

wirebond_finger_sort_wire_cross	Set this option in certain design scenarios that have many crossed wires but where you wish to maintain the current order of your bond fingers. When set, the system will attempt to retain your ordering so long as the wire crosses are legal (inside the cross distance constraint in Constraint Manager).
wirebond_highlight_single_net	Set to temp highlight the net currently being modified; for example, if in a high-density design with many guide paths, it can be difficult to tell what pin and ball the wire bond being worked on are associated with.
wirebond_hud_line_1	Choose the information displayed in the top (first) line of the HUD during wire bonding operations involving push and shove. Default is maximum wire length for all active wires.
wirebond_hud_line_2	Choose the information displayed in the middle (second) line of the HUD during wire bonding operations involving push and shove. Default is minimum wire length.
wirebond_hud_line_3	Choose the information displayed in the bottom (third) line of the HUD during wire bonding operations involving push and shove. Default is maximum wire angle.
wirebond_hud_update_frequency	Specify the frequency at which the wire bond HUD panel is updated with new information in updates per second. A higher value will update the HUD more frequently, but will cause the tool itself to operate more slowly, as more calculations must be performed. Range is 1-25 updates per second.
wirebond_ignore_disabled_cns	Set to NOT use disabled DRC checks to guide placement. Note that finger to finger and wire to wire spacing will always be used to ensure placement does not introduce unnecessary electrical shorts. By default, wire bond placement will attempt to satisfy wire to wire, finger to wire, and finger to finger DRC constraint values, whether these are currently enabled for online DRC checks or not.

wirebond_ignore_wire_profiles	Set to treat all wires as being the same profile for placement only. DRC computations, 3D views, and 3D analysis are unaffected by this setting. By default, wire bond placement will respect wire profiles when computing legal wire bond placements. As a result, if two wires use different profiles, they can cross within a set distance from the die or pin.
wirebond_label_old_sort	Set to label fingers by intersection of wire bond and die boundary when adding or moving bond fingers. By default, the fingers are labelled by finger location.
wirebond_merge_no_max_separation	Set to merge all fingers on a selected net for wire bond merge finger. By default, the wire bond merge finger capability will not merge fingers on the same net unless they are within 1.5 times the finger to finger spacing requirements. This reduces the burden to select the exact fingers for the merge.
wirebond_min_drc_default_bubble	Set for the min DRC wire bond tool use the current default bubble mode as in the wire bond settings command. The tool behaves more like the add and move commands, but may not resolve all DRCs if in "shove path" or "shove off" mode.By default, the adjust to min DRC wire bond tool runs in "shove all" mode to resolve as many DRCs as possible.
wirebond_multiwire_pins	Set to be able to select wired pins during a wire bond add operation to wire a single pin to multiple bond fingers. By default, the wire bond add tool does not allow you to add multiple pins to finger bond wires to the same pin. This allows for easier window select of sets of pins, as well as prevents you from inadvertently adding multiple wires.
wirebond_no_auto_ring_pad	Set for the wire bonding tools to use assigned padstacks for connections to the power/ground rings. By default, automatically generated will be used.

wirebond_no_load_die_stacks	Set to load only those items associated directly with the component owners when adding or moving bond fingers, ignoring other components in the stack. You can toggle this on or off from the quick utilities in the wire bond application mode. By default, all wire bonds associated with the components and die stack(s) owning any of the selected objects are loaded and available for push and shove. If you are designing a large die stack with many components, this may slow down the initialization of the tool.
wirebond_no_move_vias	Set to maintain connectivity to fingers by stretching clines instead of moving the vias connected to the end of single-segment routing stubs. By default, the wire bond tools move vias which are connected to the end of single-segment routing stubs, if there are no other clines connected to the via.
wirebond_no_show_hud	Set to stop showing the dynamic heads-up display (HUD) that is built into the wire bond toolset when manipulating your wire bond pattern. If you manually close the HUD panel, it will remain closed for the duration of the active tool session.
wirebond_nobond_dummy_pins	Set to stop bonding of dummy net pins. Dummy net pins will be treated as if NO_WIREBOND property is set for them and the pins will not be available for selection in add wire bond and they will not be legal destinations for connect bond wires. By default, the wire bonding tools allows bonding of dummy net pins, both to the substrate and to other die pads.
wirebond_pause_key	Specify a hotkey string for the pause option of the wire bond toolset. By default, the hotkey is Ctrl+F11.

wirebond_push_only_no_pull	Set to only push fingers which are in the direction of the reference wire bond's movement when performing a move operation in the wire bond commands in designs with many multi-wired bond fingers. By default, particularly in situations where one wire of a multi-wire finger crosses a single wire of a different, neighboring multi-wire finger, the tool tries to "pull" a finger that is on the other side of the reference wire bond in an attempt to satisfy constraints.
wirebond_same_symbol_die_pads	Set to add wire bonds between two die pins on the same symbol during a wire bond add operation. By default, you cannot add wire bonds between two die pins on the same symbol.
wirebond_samepath_diffprof_cross_ok	Set to treat two bond wires to be of the same profile for placement if the wires cross within a set distance from a die or a pin. DRC computations, 3D views, and 3D analysis are not affected by this setting. By default, wire bond placement uses the actual wire profiles when computing legal wire bond placements, EXCEPT when two wires go to fingers on the same path. Even if the two wires use different profiles and are normally allowed to cross within a set distance from the die or pin, that will not happen if they go to the same guide path.
wirebond_settings_key	Specify a hotkey string for the popup settings of the wire bond toolset. By default, the hotkey is Ctrl+F12.
wirebond_show_3d_length	Set to list the 3D wire length in addition to the 2D length for show element. The IC packaging database computes the exact 3D length of a bond wire based on the start and end points, the wire profile definition, and the height of the objects at both ends of the wire.
wirebond_show_angle_to_die	Set for show element to list the angle of the bond wire relative to the side of the die it originates from. If a wire is not connected to a die or interposer symbol at its start, the angle is shown as 0 degrees.

wirebond_simple_routing_channels	Set to space to minimum gap clearances for clines passing through routing channels. By default, bond fingers with routing channels defined between them use the finger gap calculations from the interactive routing commands to ensure that the interactive router can route the desired number of clines through the channels. This can leave overly conservative gaps when finger padstack definitions use pad shapes.
wirebond_sip_label_single_dies	Set to list the individual die components in the label configuration form instead of the owning die stack. By default, bond finger dynamic labels are applied at the die stack level, instead of the individual die level.
wirebond_snap_to_grid	By default, the wire bond placement engine does not snap to grids. This is because bond fingers, generally rotated at odd angles, may be more closely spaced if not snapped to grid. If this option is enabled, the reference finger will be snapped to grid on movement and addition. This will be adjusted to lie on the guide path if the grid does not align with the path placement (such as for arc paths).
wirebond_sort_finger	Set for the internal placement engine to sort wire bonds by finger location when adding or moving the wire bonds. By default, wire bonds are sorted by die pin location clockwise around the die.
wirebond_suppress_bondwire_drcs	Set for the online DRC system to report all bond wire to pin and finger violations, regardless of where along the length of the bond wire the violation occurs. By default, bond wire to pin and bond finger violations are suppressed by the tool unless the violation occurs over top of a pin/finger element on a different net. This is due to the 3D curvature of the bond wire through space.

wirebond_suppress_resort	Set to move wire bonds as they are sorted and not to update the sorting order based on the last placed wire bond during wire bond ADD or MOVE. This variable works best when all wire bonds being moved are on the same path. By default, sorting might be required to figure out the best wire bond to add or move as wire bond angles get farther away from the perpendicular and more than one tier of pins is involved. (See also wirebond_sort_finger).
wirebond_unwired_fingers_no_shove	Set to ignore unwired fingers during wire bond push and shove; for example, in designs where the unwired fingers are in fixed locations. By default, the wire bond tools push and shove both wired and unwired bond fingers.
wirebond_via_padst_only	Set to list only the padstacks in the available via padstack for use as bond fingers for wire bond commands. By default, the wire bond commands list all padstacks with a pad on the current bonding wire layer as available for use as a bond finger.

Wirebond_editor

wb_dblclk_comp_op	Specify the command to run when you double-click a component in the wire bond edit application mode. By default, you must choose the action from the popup menu.
wb_dblclk_finger_op	Specify the command to run when you double-click a bond finger in the wire bond edit application mode. By default, you must choose the action from the popup menu.
wb_dblclk_path_op	Specify the command to run when you double-click a bond finger guide path in the wire bond edit application mode. By default, you must choose the action from the popup menu.
wb_dblclk_pin_op	Specify the command to run when you double-click a pin or interposer finger in the wire bond edit application mode. By default, you must choose the action from the popup menu.

wb_dblclk_shape_op	Specify the command to run when you double-click a power/ground ring in the wire bond edit application mode. By default, you must choose the action from the popup menu.
wb_dblclk_wire_op	Specify the command to run when you double-click a bond wire in the wire bond edit application mode. By default, you must choose the action from the popup menu.
wb_drag_finger_op	Specify the command to run when you drag a bond finger in the wire bond edit application mode. By default, you must choose the action from the popup menu.
wb_drag_path_op	Specify the command to run when you drag a bond finger guide path in the wire bond edit application mode. By default, you must choose the action from the popup menu.
wb_drag_wire_op	Specify the command to run when you drag a bond wire in the wire bond edit application mode. By default, you must choose the action from the popup menu.

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Interactive Settings

addline_nomerge	Set to disble merging of lines whose end-points touch and that are on the same layer when running 'add line'.
copy_no_autopaste	Set to limit to one pick at a time while placing copied objects.By default, after copying objects, command enters the paste mode where you can pick, window/group select pads/clines, or find by query (paste to pins with GND net).
copy_no_autosnap	Set to snap picks to only the grid for the copy command. By default, the copy command auto-snaps clines and vias to aid connections.
dp_via_replace_with_struct	Set to enable diff pair mode in the "Replace Via with Structure" command. The diff pair mode allows the replacement of pairs of vias belonging to differential pair nets with a single, two-net structure. This is different from the single via mode, where each via is replaced by a separate instance of the selected structure. The diff pair mode will create derivative versions of the structure when placed at odd angle rotations where necessary to maintain expected spacing between the via elements in the structure. This is not supported by the replace, refresh, and redefine structure commands. To redefine these structures, first replace the structures with the original vias, redefine the structure, and then replace with the modified definition.
ripup_delete_first_segment	Set to delete only the first etch segment or delete segments until the remaining etch is outside a pin's when deleting a symbol and if etch ripup is ON. By default, all etches connected to the symbol's pins are deleted until the first non-cline/via etch object is encountered.

ripup_retain_bondwire	Set to retain wire bonds and bond fingers but delete subsequent etches when deleting a symbol. Set with DELETE_FIRST_SEGMENT to retain bond wires while deleting the first segment beyond the bond finger according to that preference's rules. By default, when a symbol is deleted and etch ripup is ON, all etch connected to the symbol's pins is deleted until the first non-cline/via etch object is encountered.
single_via_replace_default	Set to select single via replace mode by default when running replace padstack.
stacked_via_multi_split	Set to see buttons allowing splitting of all vias either above or below an identified layer pair. By default, splitting a stack of vias during a move, copy, delete, or slide will split a single selected via out from the stack, leaving all other vias in place.
stacked_via_off	Set to select individual vias in a stack. By default, move, spin, copy, delete and slide automatically select all vias in a stack rather than an individual via.
via_replace_with_struct_show_all	Set to show all structures in the "Replace Via with Structure" command. The default behavior is to show only those structures with either 1 or 2 net branches, depending on your current mode of single or diff pair replacement. When this is enabled, all structures will be shown in the pull-down list for selection for single item replacement.
via_struct_auto_lock	Set to add LOCKED property to each instance when placing via structure instances using the "add via structure" command. The LOCKED property prevents unintentional modifications to the placed instance, such as moving a via or changing the length of one of the via structure's clines. The property can be manually added or removed using the 'Edit' - 'Properties' command.
zone_no_trim_to_outline	Set to disable automatic trimming of the new zone boundary to the design outline when creating zones.

Clipboard

clip_altconnect	Set for Export Sub-Drawing to create a clipboard file that instructs Import Sub-drawing to lower the priority of shapes for connectivity purposes, that is, pins, vias, and clines have priority over shapes for connectivity assignment. This only applies if "Preserve nets of vias" is not checked. Clipboard files using this option are not compatible with releases older than 16.6. Should be used if utilizing sub-drawing to copy and paste via structures.
clip_filebrowser	Set for the 'clpcopy' command to use the file browser instead of the library path browser.

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Interfaces Settings

allegro_legacy_board_outline	Set to use the legacy layer 'BOARD GEOMETRY/OUTLINE' for board profile in IDF/IDX/IPC2581 export and import. By default, 'BOARD GEOMETRY/DESIGN_OUTLINE' and 'BOARD GEOMETRY/CUTOUT' are used.

DXF

dxf_incremental	Set to use incremental addition mode for dxf in. Default has dxf import replace the current design.
dxf_version	Specify DXF output version for command dxf out. Values can be 12 or 14.

IDF

idf_del_mcadowned_symbols_import	Set to delete all the MCAD-owned symbol without RefDes before importing a new IDF file.
idf_ignore_comp_height	Set for idf_out to ignore the component definition HEIGHT property and instead export the symbol definition height value.
idf_ignore_missing_refdes_placement	Set for idf import to ignore component placement instead of placing symbols without a RefDes if the RefDes cannot be found in the netlist.
idf_ignore_part_number	Set for idf_out to ignore the component definition PART_NUMBER property and instead export the component definition device type.
idf_layer_delineate	Specify a character to delineate between class and subclass names for idf export, if, for example, the default slash is illegal in your MCAD system.

idf_mech_refdes	Set for idf_out to output RefDes and part number for mechanical parts. This appears to violate the IDF standard in that mechanical parts should output NOREFDES.
idf_nodelete	Set to only import the .PLACEMENT and .NOTES sections of the IDF file using idf_in. All other sections of the IDF file will be ignored.
idf_place_bounds_bottom	Specify the subclass of the Package Geometry class that is used to calculate the component outline for the IDF Library file. Also specify IDF_PLACE_BOUNDS_TOP.
idf_place_bounds_top	Specify the subclass of the Package Geometry class that is used to calculate the component outline for the IDF Library file. Also specify IDF_PLACE_BOUNDS_BOTTOM.
idf_units_naming	Set for IDF to create padstacks and symbols using a unit string (), where units can be MM or MIL, and two decimal places of accuracy. For example, for a 1.10 mm hole a npin110mm.pad is created.By default, IDF creates padstacks and symbols using the hole diameter with 1 decimal place converted to MILS as the naming scheme (). For example, for a 1.10 mm hole a npin433.pad is created.

IDX

auto_set_object_ownership	Set to add electrical ownership to an object that does not already have ownership, and does not already have an IDX_ID on the first, and successive exports of Allegro data to IDX.

idx_enhanced_features	Set to export IDX enhanced features. These features are not supported by all MCAD software tools. Verify with your MCAD tool supplier if the MCAD software can support these features. The enhanced features are package pin 1 location, board height offset for components, component multiple outlines with different package heights, board thickness plus tolerance, user-defined layers including external copper, bi-directional exchange of user-defined shapes, and rectangle/square/oblong slots.
idx_export_compdef_attrs	Set to export all properties for component definition by idx_out.
idx_export_embedded_comp	Set to export embedded components using idx out. By default, embedded components are ignored in IDX export.
idx_export_first_mask_layer	Set to export the first mask layer located on the external side of the outermost copper layer on each side even if it is not intended to function as a soldermask layer.
idx_export_hatched_shapes	Set to export hatched shapes as is. By default, hatched shapes will be exported as solid shapes.
idx_export_layer_stackup	Set to export stackup information using idx_out. By default, layer stackup information is not exported for regular board.
idx_export_package_top_outline_only	By default, an overall bounding box is exported if both top and bottom place outlines are defined for package. Set to export top place outline only.
idx_export_pinhole_netname	Set to export the net name for the plated pin hole.
idx_hole_use_mapped_padstack	If set, 'idxHolePadstackMapping.txt' file will be considered when "Select All" is selected in IDX Flow Manager Import form.
idx_ignore_comp_height	Set to ignore the component definition HEIGHT property and instead export the symbol definition height value by idx_out.

idx_ignore_part_number	Set to ignore the component definition PART_NUMBER property and instead export the component definition device type by idx_out .
idx_place_bounds_bottom	Specify a subclass of the Package Geometry class to be used to calculate the component outline. Also specify IDX_PLACE_BOUNDS_TOP.
idx_place_bounds_top	Specify a subclass of the Package Geometry class to be used to calculate the component outline. Also specify IDX_PLACE_BOUNDS_BOTTOM.
idx_separated_board_cutout	Set to export cutouts as individual objects. By default, one single IDX object contains both design outline and cutouts. Before setting, ensure the MCAD tool supports this feature.
idx_units_naming	Set for IDX to create padstacks and symbols using a unit string (), where units can be MM or MIL, and two decimal places of accuracy. For example, for a 1.10 mm hole a npin110mm.pad is created.By default, IDX creates padstacks and symbols using the hole diameter with 1 decimal place converted to MILS as the naming scheme (). For example, for a 1.10 mm hole a npin433.pad is created.
idx_version	Specify the IDX output version for command idx_out. Values can be 2.0, 3.0 or 4.0. Default is 3.0.

IPC2581

ipc2581_compdef_all_attrs	Set for ipc2581_out to export all the component definition properties to BOM section.
ipc2581_enable_artwork_filename_affixes	Set for ipc2581_out to add prefix and suffix to the artwork film name as IPC2581 layer name.

ipc2581_enable_diff_thickness_mask_layers	Set for ipc2581_in to create separate mask layers for same mask layer which has different thicknesses in different zones, and for ipc2581_out to merge back to one single layer with varying thicknesses in different zones.
ipc2581_export_copper_layer_profile	Set for ipc2581_out to export copper layer profile for DFM check in rigid-flex designs for experimentation in IPC2581-B. They are always exported in IPC2581-C.
ipc2581_export_isolated_pin	If set, export the isolated non-plated pins of dummy nets in logical nets, physical nets.
ipc2581_export_user_specs	Set for ipc2581_out to export user-defined specs on logical nets, components, and design for experimentation in IPC2581-B. They are always exported in IPC2581-C.
ipc2581_export_xsection_drill_direction	Set for IPC2581_out to export drill directions defined in cross section editor.
ipc2581_filter_part_number	Set for ipc2581_out to not output part number from BOM items.
ipc2581_group_drills	Set for ipc2581_out to export drills into different groups by drill type (drill/slot/backdrill/counterdrill), layer pair, finished size, tool size, tolerances, plating status, and owner type (pin/via/pVia).
ipc2581_ignore_ood_check	Set for ipc2581_out to not check dynamic shape status and backdrill status to allow Allegro Documentation Editor tool to be opened without any restriction.
ipc2581_ignore_surface_layer	Set for ipc2581_out to not export surface layer in the stackup section.
ipc2581_output_square_hole_as_slot	Set for ipc2581_out to export square hole as slot.

ipc2581_rigid_flex_zone	Set for ipc2581_out to export multiple stackups and zones in rigid-flex design for experimentation in IPC2581-B. They are always exported in IPC2581-C.
ipc2581_stackup_core_group	Set to support manufacturing core group in layer stackup during ipc2581 export and import. by deafult, they are ignored.
ipc_add_no_place_bound_symbols	Set for ipc2581_out to export the symbols without PLACE_BOUND outline.
ipc_ignore_some_layer_specs	Set for ipc2581_out to not export the Conductivity for the dielectric layers, and the Dielectric Constant and Loss Tangent for the conductor layers.

PDF

pdf_apply_film_undefined_line_width	Set to apply the value of the "undefined line width" film parameter to all the objects with zero width.
pdf_bookmark_view_dest_no_fit	Set to NOT automatically zoom out to fit the page when a new page is selected using the bookmark tabs. Adjust to get a proper page view when a new page is open.
pdf_export_bondwire	Set to output an extra page for bondwires for chip-on-board designs.
pdf_filled_shape_transparency	Specify the transparency value for the filled shape and traces.
pdf_ignore_default_prefix_suffix	Set to NOT add default prefix and suffix strings in the output file name while exporting a pdf file.
pdf_minimum_print_line_width_scale	Set to scale the base minimum printed line width of 1.0 mil or 0.0254 mm, and then apply the resultant line width to all the objects with smaller line width.

pdf_netname_height_on_cline	Specify the height of net name as a percentage (0.0 1.0) of cline width. Default is .8 or eighty percent of the cline's width.
pdf_netname_height_on_pin	Specify the height of net name as a percentage (0.0 - 1.0) of the pin's small size. Default is .2 or twenty percent.
pdf_netname_on_cline	Set to display net names on clines.
pdf_netname_on_pin	Set to display net names on pins.
pdf_no_total_etch_length_on_net	Set to NOT display total etch length under Net Tree.
pdf_no_white_to_black_change	Set to retain white color geometries as white in PDF viewer. By default, the white color geometries will be changed to black to be seen in the PDF viewer.

plctxt

place_text_filename	Specify a name to override the default plctxt filename, place_txt.txt. Variable expansion is supported to use current values of other variables. To use the current design name, specify the value \$module The backslash (or single quotes around name and $) and $ are required in this mode.
place_text_version2	Set to use version 2 of place text file format. Set by default. The plctxt file format changes when version 2 is used. Plctxt in can consume either format.

STEP

copper_no_z_offset	set to export the external copper at the board level. By default, the external copper is exported above board level for display.

disable_new_3d_model_mapper_msg	Set to turn off the message dialog box for new 3D Canvas Model Mapper when opening existing Step Package Mapper.
step_3d_copper	Set to export external copper as 3D geometries. By default, the external copper will be exported as 2D geometries for smaller file size.
step_board_level_package_height	Set to export the design level package outlines and heights for all the components. Note that the STEP file will be much larger. By default, the package definition is exported only once and then referenced by the components, which results in a smaller and more efficient STEP file.
step_display_resistors_capacitors	Set to include the capacitors and resistors, which are ignored for performance improvement, during mapping mechanical assembly (enclosure, cage, bracket, and so on).
step_export_comp_part_number	Set to export the component part number as part of STEP object ID.
step_export_mixed_units	Set to keep original step units in STEP models in exported files. By default, mixed units are converted into a single unit in the exported STEP file.
step_export_rigid_flex_mask_layers	Set to export mask layers outside external copper layers in rigid-flex design for enclosure collision checking. Currently the hole details are ignored for better performance.
step_ignore_all_electrical_packages	Set to ignore all electrical packages for performance improvement during mapping of mechanical assembly (enclosure, cage, bracket, and so on).
step_map_sort_no_case	If set, the lists in the STEP package mapping tool will sort without regard to upper and lower case. If you have file names with mixed case strings, this will group these entries together. Default is a case-sensitive sort.

step_place_bounds_bottom	Specify a subclass of the Package Geometry class that is used to calculate the component outline. Also specify STEP_PLACE_BOUNDS_TOP.
step_place_bounds_top	Specify a subclass of the Package Geometry class that is used to calculate the component outline. Also specify STEP_PLACE_BOUNDS_BOTTOM.

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Logic Settings

allegro_max_signal_net_pins	Set the number of pins for which a net is automatically converted to a voltage net. When this threshold number of pins is reached, VOLTAGE, RATSNEST_SCHEDULE, and NO_RAT properties are added to the net. Set the value to 0 to disable this behavior and retain full manual control. Note that unidentified voltage nets can significantly degrade overall tool responsiveness.
dcnets_delete_norat	Set for the identify DC net command to delete NO_RAT property from nets getting the Power and Ground Schedule. Use to migrate legacy boards using NO_RAT scheduling.
edit_parts_expand_lists	Set for the edit parts command to display reference designator lists in an expanded format. Items are grouped together by default. For example, U1, U2, and U3 will be listed as U1-3. This format does not support dashes in designator names. If your design uses dashes, enable this variable to have full capabilities in the edit parts command.
logic_edit_enabled	Set to enable the 'net logic' command and the pop-up option 'Delete Component'. By default, this feature is disabled to prevent inadvertent changes to the logic.
netin_initial_directory	Specify the initial directory which import logic uses to store netlist files (Cadence or third-party). Used to initialize new designs. Ignored if editor is started from projmgr (uses the cpm file seeding).
netrev_forbid_precision	Set for netrev to NOT override board's precision during F2B flow.
netrev_missing_footprints	Set to report error for missing footprints instead of the default warning in netrev reports. Logic import will fail. Can also can bedriven via the '-e' command line switch to netrev batch.

netrev_no_footprint_warnings	Set to suppress warnings for missing footprints in netrev reports. This variable overrides the netrev_missing_footprints environment variable.
pcb_baf_pin_number	Set for backannotation to use the pin number and not the pin name for the "was" part of the PIN statement for preassigned and not yet assigned functions.
schematic_editor	Specify the schematic editor for a new drawing. Possible values are "capture" for Design Entry CIS (Capture) designs and "hdl-concept" for Design Entry HDL / System Capture designs.

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Manufacture Settings

Artwork

arc_oldvectorize	Set to use the old artwork vectorizing algorithm. Enables access to 'art_circvects' environment variable. New arc to vector algorithm automatically accommodates the wide range of units and accuracy present in modern designs. The old vectorizing algorithm will be removed in a future release.
art_arc_centercheck	Set to plot an arc only if the arc center is inside the photoplot outline. By default, GERBER 6X plots an arc even if the arc center is outside the photoplot outline. Certain CAM stations may have trouble with this model.
art_circvects	Specify the number of segments to vectorize a circle. If set, it overrides default artwork arc vectorization.By default, vectorization is based upon a combination of design units, accuracy and arc radius. Vector artwork (Gerber 6x or 4x) uses the specified value for all arcs. Raster artwork vectorization only applies to shape/void edges. If set, user supplied value is used if it would result in more vectorization then the calculated value. Starting 15.7, this setting is not used unless arc_oldvectorize is also set.
art_stripdirectoryname	Set to include only the design name in the comment section of the film. Normally, artwork in the comment section of the film file includes both the filename and the directory name.
artwork_allwarnings	Set to list all warnings in the "photoplot.log" log file .
artwork_arc_round_error	Set to display 'artwork arc to convert to line accuracy' WARNING messages as ERROR messages. By default, these are warnings.

artwork_filename_prefix	Specify a prefix to be added to the beginning of artwork file names. The global film filename prefix in the Art Control Form overrides this value.
artwork_filename_suffix	Specify a suffix to be added to the end of the artwork file names. The global film filename suffix in the Art Control Form overrides this value.
artwork_no_unit_warn	Set to disable popup warnings about artwork output rounding in the artwork user interface. Warnings are still issued to photoplot.log.
artwork_nophotoplot_warning	Set to issue INFO messages instead of WARNING messages if the photoplot window exceeds film size in artwork. The message will not be counted as a warning in the artwork summary.
artwork_undef_line_width	Specify a seed value for the "Undefined line width" parameter in the Artwork Control Form dialog when creating new films. The value is not applied to films that have been created prior to the value being set. The default value is 0 (zero). The number can be unitless, which maps to the design's units. If the value contains units it will be translated to the current design units (example 5 mils).
artwork_undefined_width_error	Set to mark 0 (zero) line widths in artwork films as ERROR messages when the undefined line width setting is also 0. This can be corrected by setting the 'Undefined line width' to a value for each film in the artwork dialog. By default, these are warnings.
film_nosort	Set to display film param artwork in an unsorted stackup order, similar to pre-14.2 releases. By default, film param artwork is sorted alphabetically. When this variable is set, film param artwork may appear in stackup order if you create the stackup before opening the film param dialog.
loadgerber_flash_size	Specify the size of flash triangle to be used when loading Gerber 4x or 6x and the target option is selected. Default value is C-point size (80 mils). Value can be a number; unit defaults to current design units. Value can also include a standard, length unit (MIL, MICRON, and so on).

Draft

draft_retain_class_subclass	Set for drafting commands to maintain current active layer.Default behavior is to switch to Board Geometry/Dimension layer when starting these commands.

Drilling

backdrill_enable_dynamic	Set to display the Dynamic Backdrill option under the Settings tab of the Backdrill Setup and Analysis dialog. If you enable the Dynamic Backdrill option, interactive editing commands will update backdrill information on pins and vias in real-time as the design is modified. Follow the standard backdrill process: Identify nets targeted for backdrill, configure backdrill and layer pairs, and then execute backdrill. You must rerun backdrill prior to manufacturing release to verify all relevant stubs have been removed.
backdrill_layer_pair_adjustment	Set for backdrill layer pairs to be adjusted by manufacturing stub length (Drill operation z tolerance).
backdrill_oversize_option	If set, the "Backdrill Setup and Analysis" form will provide options to disable canvas update of the Backdrill padstack geometries and keepouts in the path of the backdrill. Setting this variable is not recommended as it could lead to manufacturing issues when the design is backdrilled.
backdrill_skip_pairs_question	Set for Backdrill Pairs Question to be skipped if layer pairs are not initialized.
nc_customization_save_with_errors	Set to save NC drill customization with validation errors.
nc_drill_export_coordinate_format	Set to export the coordinate format in the header section of the drill and router files in an enhanced Excellon format. For example, "METRIC,TZ,000.00000".

nclegend_file	Specify the default filename convention for NC Drill Legend. By default, NC Drill Legend uses a name of default- where units is the current board units. The override name should contain only the filename not a PATH component.
nclegend_legacy_row_height	Set for NC drill legend table to keep the legacy row heights.
nclegend_supress_zero_tolerances	Set to supress NC drill legend table cell for zero tolerances +0.0/-0.0.
nctape_cam350	Set to suppress the ";DESIGN" comment line in Allegro drill files (.drl) because CAM350 software has a bug where it does not correctly process this line.
nctape_toolcodes_error	Set to change the missing toolcodes warning to an error. nctape will also exit with an error status instead of a warning.
preserve_via_backdrill_data	Set to keep backdrill data associated with Via during Slide and Move operations. This will maintain backdrill keepouts and Design for Fabrication backdrill checks without the need for repeated backdrill runs during etch editing activities. After updates are complete, a Backdrill run is required to validate backdrill data.

IPC_netlist

ipc356_027record_netname	Set to enable netname with continuation records (027) for ipc356. By default, ipc356 (rev A) continuation records (027) do not require the netname since the previous record has the name.
ipc356_mapped_atr_netshort	Set to use mapped net name in the NET_SHORT property for smaller string. By default, ipc356 exports NET_SHORT property from design.
ipc356_nomechpin_warnings	Set to suppress ipc356_out generated warnings when mechanical pins are defined without drill holes.

ipc356_truncate_large	Set for ipc356_out to truncate numbers exceeding the magnitude required by specification and generate warnings. By default, ipc356_out generates errors. Use this option only for debugging problematic coordinates and sizes and not for production.
ipc356_unique_netname	Set for ipc356_out to generate a unique net name for each dummy pin using the same methodology as dummy net pins with connections. By default, ipc356_out uses net name "N/C" for dummy net pins with no connections.

Plot

lp_abs_origin	Set for IPF import to use the origin contained within the IPF file. This helps alignment if you are using the design origin for placement. By default, load plot uses the lower left corner of the IPF file's bounding box as its placement origin.
noplotmargins	Set to disable plot margins on the printer. By default, printers provide a margin around a plot (typically 1 inch). Windows only.
plot_shape_bw_outline	Set to unfill shapes when plotting in the black and white mode to make items behind the shapes visible.
plot_shape_spacing	Specify the spacing for the lines created for shape fill in a plot. A high value plots shape fill with gaps but improves plotter speed.
plot_vectext_width	Specify, in conjunction with plot_vectorize_text, the default 'width' to appear with 'Vectorize text' under 'IPF setup' on the Plot Setup form. The width of the vectorized text is drawn at the value specified. Note that this will be overridden by a remembered .ini file plot_setup setting.
plot_vectorize_text	Set to enable 'Vectorize text' under 'IPF setup' on the Plot Setup form by default. When enabled, the .plt files generated by Allegro vectorizes text data into line segments. Note that this will be overridden by a remembered .ini file plot_setup setting.

Print

print_nt_extension	Speicfy the file print extension on Windows. Default is txt. An external program is is used to print text files; for example, Notepad for txt files or Word for doc files depending upon Print Windows file association settings in your system.

Reports

delay_report_max_signal_net_pins	Set for the IC Packaging net delay report to skip processing of nets with more pins than the value specified in the delay_report_max_signal_net_pins variable. Skipped nets are listed in the log file. By default, nets with more than 6 pins are skipped.
report_antennavia	Specify the set of vias NOT to be shown in the dangling report under the sub-section Antenna vias. 'voltage' suppresses vias on nets with the VOLTAGE property. 'testvia' suppresses testvias. 'thru' suppresses through hole vias. Choose a combination value to suppress more than one type of vias; for example, 'testvia thru' suppresses testvias and through hole vias.
report_noantennavia	Set to suppress the antenna via section of Dangling Report.
report_nopath	Set to strip the directory portion of the design name in certain reports. Default is to output the design name and directory name.
report_separator_pipe	Set to use pipe ('|') as the seperator in CSV reports. By default, comma is used.
testprep_rpt_netnames	Set to print net names on each line in the testprep report. By default, net is printed only on the first line if subsequent lines have the same net name.

Silkscreen

autosilk_disregard_solder_mask	Set for Autosilk to clear vias when the soldermask is not defined.

fst_ref_des	Specify the value for starting RefDes numbers for auto-rename.For example, if RefDes should start at C1000, set the value to the first RefDes number, 1000 in this case.

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Miscellaneous Settings

allegro_sort_separators	Set to compare strings between separator characters when using the 'jedec' or 'natural' string sorting styles. For example, comparing ABC-DEF to AB-CDEF would compare ABC to AB, then DEF to CDEF.
allegro_sort_style	Specify the sorting style of strings, such as in report outputs. 'default', which is the default style, sorts using a fast but simple routine. 'natural' sorts in the ascending order, puts 2 before 10. 'jedec' is similar to natural but sorts shorter strings before longer, B before AA. Requires restart.
clip_noclip_property	Set for the Export Sub-Drawing commands to create clipboard files without the CLIP_DRAWING property attached to objects.
cross_chart_all_stackups	Set to add all the stackup defintions to a cross-section chart or table even if they are not referenced in a rigid-flex design.
etch_length_pinpair_report_500+pins	Set to list nets with more than 500 pins in ETCH Length by Pin Pair Report.By default, the nets with 500+ pins are ignored.
report_comp_rotation_range_180	Set to specify the component rotation range from -180 to 180, including both the values. By default, the component rotation range is from 0 to 360, including both the values.

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Obsolete Settings

cns_noviasort	Set to restore release 13.6 no sorting behavior for the current via list in constraint dialog Physical Rule Set Values.
control_auto_raise	Specify the default tab in control panel. If a command had changed the tab, upon termination of the command, system reverts control panel to the default tab. If not set, tab is not changed at the end of a command.
copy_autopaste	Set to automatically invoke new Edit -> Paste command after selecting objects to copy using Edit -> Copy command.
database_compatibility_mode	Set to disable any new release feature that introduces a database schema change. When a design opened in compatibility is saved, it will be compatible with 17.2.
database_compatibility_new_design	Set along with database_compatibility_mode to open a new database in compatibility mode. Use this variable to run batch processes that open a new design.
drc_diff_pair_overide	Specify 0 (zero) to suppress line to line DRCs between two differential pair nets if the primary spacing is less than the line to line spacing for the etch layer. Use only while migrating designs with differential pairs from releases earlier than 15.0. In cases where the differential pair lines are routed diagonally, the actual spacing is fractionally higher or lower than the required spacing. Legal non-zero values are 100 (1 unit of accuracy) or 200 (2 units) for tolerancing.

drc_diff_pair_primary_separation_tolerance	Specify the minimum and maximum primary separation value for checking odd angle lines and differential pair line to line spacing while migrating legacy designs with differential pairs from releases earlier than 15.0.2. In pre-14.2 releases, set drc_diff_pair_primary_separation_tolerance = <min>:<max>. Both and are primary separation values with optional units ("10 MIL:20 MIL"). The 'max' value is added to the differential pair primary separation value when checking an odd angle line. The 'min' value is subtracted from the primary separation value when doing a line to line spacing check between differential pair lines.
drc_fillet_samenet	Enables more conservative same net checking with respect to fillets. With this variable set, more DRCs may be reported. The default is to not consider a fillet touching a pad to be a DRC even if an adjacent same net cline is below the line to line spacing value. This variable only applies to the pre 16.2 release cline-based fillets.
infinite_cursor_bug_nt	Set to eliminate graphics artifacts on screen in OpenGL with some GPUs or graphics drivers for the infinite cursor.
orcad_no_new_design_form	Set to suppress the new design basic configuration form when starting a new drawing in the OrCAD layout tools. The form presents you with the option to configure units and drawing size information, but may break existing scripts.

shape_void_cline_region	Set to void segments of a cline passing through constraint regions at its required clearance in each constraint region individually for dynamic shape voiding. By default, a cline will be voided to the most conservative (largest) spacing value of any constraint region it passes through. This variable is obsolete and has been replaced by the design level property DYN_SHAPE_VOID_CLINE_REGION. If this variable is set when opening a design without the design level property set, the property will be added. NOTE: Setting this variable may reduce performance slightly on very large designs.
xsection_modern	Set in pre-16.0 Allegro PCB to use the SI cross-section dialog.It can be slow on large layer count boards and disables the old xsection icon. Only supported in Expert and Performance. The old dialog is no longer supported.

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OS Settings

cdn_mail_unix	Specify an alternative interface for email in Unix/Linux. See /share/pcb/examples/configure/cdn_mail_unix directory for instructions on how to integrate an alternative email program to Allegro mail. This should only be used if you cannot use the default UNIX mail program. This override is not supported on Windows.
ntpserver	Specify the Network Time Protocol (NTP) server. The default server is 0.pool.ntp.org. NTP is currently an option used for design locking. To use an NTP server, you must be connected to the Internet and any firewall must be configured to allow port 123 to pass.

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Paths Settings

Config

accpath	Specify the search path to locate ACC projects.
aptpath	Specify the search path for aperture flash files (.bsm) when negative planes are present. This is obsolete if new-style flash designs are used.
artpath	Specify the search path for artwork aperture files (.txt).
clippath	Specify the search path for sub-drawing files (.clp).
dclpath	Click to specify search path for decoupling capacitor list files (.dcf).
dfaauditpath	Specify the search path for DFA Audit (.arl .rle).
dfacnspath	Click to specify search path for dfa constraints spreadsheet files (dfa).
idxfilterpath	Specify the search path for IDX object filter configuration file(.config).
idxpath	Specify the search path to locate IDX files(.idx).
ipc2581attrpath	Specify the search path for IPC2581 property configuration file(.atr).
ipc2581spec_path	Specify the search path for IPC2581 spec configuration file(.xml).
ldfpath	Click to specify search path for Library definition file (.ldf).
lstpath	Specify the search path to locate list files (.lst). Requires restart.
materialpath	Specify the search path to locate materials.dat (Allegro) or mcmmat.dat (APD) (.dat).
ncdpath	Specify the search path for NC Drill files (.txt).
pcell_lib_path	Click to specify search path for pcell component implementation (.il .ile).

prfeditpath	Specify the search paths for user preferences files.
scriptpath	Specify the search path for scripts.
textpath	Specify the search path for extracta command files (.txt).
tilepath	Click to specify search path for reusable die pin tiles (.til).
viewpath	Specify the search path for visibility schema files (.color).
wizard_template_path	Specify the search path for Allegro template databases. Used by the Template button in dialogs. If a template file named 'new_default.' (example, 'new_default.brd') exists,this file is used as the starting template if a template database is not explicitly specified.
xtalk_table_path	Specify the search path for crosstalk tables (.xtb).

Editor

formpath	Specify the search paths for forms.
menupath	Specify the search paths for menus.
workflowpath	Specify the search paths for Workflow files.

Library

allegro_http_library_source	Set the source for query and download process while updating the library data for Allegro Interactive and batch features.
devpath	Specify the search path for library devices (.txt).
iconpath	Search path for custom toolbar icon files.
interfacepath	Click to specify search path for Interface files (.idf).constraints spreadsheet files (dfa).
miscpath	Click to specify search path for miscellaneous file types. Supported types are dxf/idx conversion (.cnv) and find query (.qfnd).

modulepath	Click to specify search path for design reuse modules (.mdd).
padpath	Click to specify search path for library padstacks (.pad).
parampath	Click to specify search path for parameter files (.prm). These allow reuse of physical design data option settings like text, visibility and grid settings.
psmpath	Click to specify search path for library symbols (.psm .osm .bsm .ssm .fsm).
step_facet_path	Click to specify search path for STEP facet files (.xml).
step_mapping_path	Click to specify search path for STEP mapping files (.map) for device.
steppath	Click to specify search path for STEP files (.stp .step).
techpath	Click to specify search path for technology files (.tech).
topology_template_path	Click to specify search path for topology template files (.top).

MCM

wbpath	Search paths for wire bond pattern archive data files (.wbt). When importing wire bond patterns, this path is searched first for .wbt files previously exported from the tool.

SigNoise

signal_install_dir	Specify the path to standard SigNoise model libraries.
signal_optlib_dir	Specify the paths to optional SigNoise model libraries.
signoisepath	Specify the miscellaneous SigNoise file locations (.dat .wave .mod .ctl).
sigrity_eda_dir	Specify the path of the Sigrity installation.

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Placement Settings

Design_partition

allegro_email_address	Specify the value to be assigned by Design Partitioning to the Master Designer user field or the Active Partition user field. This variable should be used at sites where the user login name and email address are different.This variable should only be assigned in the user's env file, not in a site-wide env file.
partition_include_diestack	Set to include DIESTACK type layers and layers outside the substrate top and bottom when defining partitions for package designs in APD products. By default, only substrate layers are displayed.
partition_suppress_email	Set to suppress automatic email messages associated with Design Partition actions. You can temporarily enable email in Workflow Manager.

DFA

dfa_pause_level	Specify the pause level in manual placement command. If DFA DRC check is enabled, when a component reaches its minimal DFA spacing of another component, it pauses briefly so it can be placed as close as possible to the other component without a DFA DRC violation. Setting level to 0 disables this feature. A 3 gives the longest pause. Default level is 1.
display_nodfa_drc_marks	Set to display only dynamic spacing circles and not DRC markers for DFA violations during interactive placement.Default is to display both DRC markers and spacing circles.

General

disable_module_auto_lock	By default, the LOCKED property is added to each module instance created by place manual and place replicate. The LOCKED property prevents unintentional modifications to the placed module instance. Set this variable to disable automatic locking of module instances. The LOCKED property can be manually added to or removed from modules using the 'Edit' - 'Properties' command or in Placement Edit application mode using the €˜lock module €™ and €˜unlock module €™ commands.
disable_module_shape_convert	By default, modules that contain dynamic shapes will automatically convert shapes to static to maintain design intent when placed/applied in a design. Set this variable to disable shape conversion and to maintain dynamic shapes in the target design as defined in the module. This applies to both the Design Reuse and Place Replicate module flows.
display_norefdes	Set to not show RefDes for symbols in dynamic mode, which is the pre-release 15.2 behavior. By default, RefDes is shown when a symbol is being moved.
display_refdes_rats	Set to display a rat line from RefDes origin to a component's pin 1 in order to show component to RefDes relationship.
module_instance_no_rename	By default, nets and component reference designators of a placed module will have their names made unique by adding the module instance name as a prefix or suffix on the names. Set this variable to disable renaming of components, nets, or both. Note that disabling the renaming of component refdes strings will result in a second instances of the same module stealing the component from the previous instance.
modules_no_5x_support	Set to search for module files (.mdd) using only the MODULEPATH variable when the editor is started with a project file (.cpm). By default, when Allegro layout editors are started with a project file, modules are first searched in the sub-project physical design views under the active project hierarchy and then by the MODULEPATH variable.
no_dynamic_ratsnest	Set to disable display of dynamic ratsnest. This restores behavior where rats are shown as elastic rubber bands in dynamic mode. Currently dynamic ratsnest are shown only for Minimum Spanning Tree scheduled nets.

noswapripup	Set to NOT rip up etch during pin and function swaps. This does not apply to component swaps.
plc_rep_copy_attr	Set for the 'place replicate' commands to propagate pin attributes from the seed circuit.
plc_rep_show_matching_dialog	Set for the 'place replicate' commands to always display the component mapping dialog box. Normally, this window is only displayed if there is some ambiguity in component assignment and your inputs are needed.
plc_rep_suppress_warning	Set for the 'place replicate create' commands to set 'Continue' as default action and suppress the warning message.
preserve_symbol_textblocks	Set to preserve symbol block number when placing components. By default, the symbol text block size is matched with the board text block size when placing components. If a match is not found a new textblock is created until all text blocks are used.
swapcomp_acrossmodules	Set to allow inter-module swapping without confirmation. By default, 'swap components' displays a confirmation message when you swap across modules.

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Route Settings

Connect

acon_dest_sched_pinonly	Set to choose pins as the destination for user scheduled nets. By default, add connect picks up source and destination points as per the nearest endpoints, which may not be the ones specified in the user schedule.
acon_diag	Set for add connect to start routing from the dangling end of a non-orthogonal direction in the same direction as the existing segment before bending towards the cursor. By default, while in line lock 45 mode, add connect prefers to first route in an orthogonal direction before bending towards the cursor.
acon_diffpair_pad_connect	Specify the behavior for differential pair gathering at target terminals when the cursor is near the target terminal of the control trace. "center" is when the cursor is on the near-side of the terminal and midpoint gathering is performed. "old" is when the cursor is on the far-side of the terminal, the control trace is connected using line lock segments and the mate connects with automatic "Finish". "cursor or default" force midpoint gathering at the target terminals regardless of cursor position.
acon_disable_nullnet_route	Set to start routing only from pins connected to a net. By default, "add connect" allows routing to start from open space as well as from legal objects such as pins, vias, clines, shapes, rats, or rat Ts.
acon_no_impedance_width	Set for impedance rules to have no effect on the trace width in add connect. By default, add connect uses a trace width that satisfies the impedance requirement unless that width is less than the minimum allowable trace width.

acon_no_width_override_retain	Set to not retain user-defined width for the next command execution. By default, width value is retained for next command execution.
acon_offnet_snap	Specify the hug and snap behavior. By default, unless bubble is set to "Shove preferred", add connect will snap the endpoint of the new cline to the minimum drc distance from another net's cline if the cursor is near the other cline and that cline is on the active subclass. If the previous pick was also at the drc distance from the other cline, the new cline will hug to the other cline. You can totally disable this behavior by setting acon_offnet_snap to "off". You can turn off the hug part and only snap the endpoint by setting the variable to "endpoint".
acon_oldhlt	Specify whether to highlight only source and destination elements or the entire net for a connect. Set to "fromto" for add connect to highlight the source and destination elements instead of the entire net. This restores the behavior that existed before release 14.2. Set to "all" to highlight the entire net for all types of nets (14.2 behavior). By default, the entire net is highlighted unless the net is NO_RAT or POWER_AND_GROUND.
acon_restore_space_mode	Set to restore the space mode to the value that was active the last time add connect was run. By default, add connect sets the group route space mode to "Current Space" at the start of the command.
acon_route_on_active_subclass	Set for add connect to always begin a route on the active subclass. Otherwise, it may change the subclass to match an element that is findable at the starting pick.
allegro_dynam_timing	Specify "on" to enable dynamic timing feedback. Specify "off" to disable dynamic timing feedback. You can alias a function key to toggle feedback display using the settoggle command as follows: alias F2 "settoggle allegro_dynam_timing off on"

allegro_dynam_timing_fixedpos	Set to display dynamic timing feedback at a fixed location and not following the cursor. You will not be able to move the display. With this option, you also get multiple timing meters, one for each type of timing constraint that applies for the current edit.
allegro_etch_length_on	Set to display the pin to pin etch length information and the net length information while interactively routing by typing "etch length" on the command line while in add connect. If needed, set up an alias using a function key to activate add connect and etch length as follows: alias F2 "add connect;etch length"
bubble_no_display_invisible	Set to prevent elements on nonvisible subclasses from appearing in the etch editing dynamics when they are bubbled. By default, bubbled etch is displayed in the dynamics even if the element would not normally be displayed.
bubble_shove_bondpads	Set to bubble bondpad vias when via shoving is enabled. By default, bondpads are not shoved.
etchedit_ignore_dynamic_shapes	Set to ignore dynamic shapes while doing etch editing tasks like add connect and slide.
no_show_dynam_elec_errors	Set to stop showing errors for dynamic clines that are being edited or bubbled. By default, screen is dynamically updated with length errors when you move the cursor. Length errors in the dynamic clines are indicated by drawing a "centerline" on the etch in the DRC "Through All" color.
options_no_enhanced_padentry	Set to disable enhanced pad entry. By default, enhanced pad entry is enabled in new designs for the etch editing commands.

padentry_factor	Specify a percentage value to control gathering for traces exiting a round pin or via while concurrently routing more than one net, such as a differential pair. The purpose is to allow the traces to gather sooner. The value is used as a percentage to reduce the minimum clearance that the gathering code requires between the pin/via and the second segment of the cline exiting the pad. By default, it requires 100 percent of the applicable minimum segment to pin/via spacing constraint. A value of 75 causes the minimum space to be 75 percent of the constraint set value.
rats_factor	Specify a value to control the preference to select straight pin to pin horizontal and vertical ratsnest connections. The legal value is a range between 0.0 and 1.0. The default is .5. A value close to 0.0 specifies no preference to straightness, short manhattan length is the sole determining factor. A value close to 1.0 causes ratsnesting preference for straight connections, regardless of distance between the pins.
rv_single_thread	Set to stop route vision from multithreading.Set by default. If not set, route vision will use multithreading, the number of threads being equal to the number of cores in the system.
slide_no_snap	Set to disable the snap feature. By default, slide will snap to adjacent segments in order to make it easier to line up a track with the neighboring tracks.

Flow Plan

create_flow_45_snapping	Set to snap to 45 degrees for the Create Flow command.

Gloss

cbd_check	Set to perform a DRC check on the connections that have been changed during glossing.

enable_fixed_fillets	Set to display the 'Fix Teardrop' and 'Unfix Teardrop' options in the 'Route' menu to enable fixing and unfixing of fillets. If set, the missing fillet report will list any fixed fillets in your design. Commands and SKILL functions that modify the design will not remove or update fixed fillets. Requires restart.
fillet_pad_inside_shape	Set to generate fillets for clines entering pads covered by a shape. By default, a cline entering a pad that is itself already covered by a shape does not require a fillet. Instead, the shape provides the coverage that the fillet normally would, and the fillet is suppressed to avoid redundant objects in the database.
gloss_fatten_single_seg	Set to process each segment of a cline individually during line fattening. By default, if one segment of a cline cannot be fattened because new DRCs will result, no segments of that cline are modified.
gloss_pad_shape	Set for Allegro to consider the outline of a pad as a square or rectangle and enhance line entry into pads.

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Shapes Settings

General

enable_wysiwyg_move	By default, the move command defers dynamic shape updates until objects being moved are placed. Set this variable to update dynamic shapes when objects are selected and again when they are placed.
shape_add_filltype	Specify the initial shape type for adding shapes on ETCH. By default, this type is dynamic. Across use of adding shapes, type used for the last add shape is remembered.
shape_arcmode_nonsticky	Set to automatically change segment type to line after adding an arc for edit shape/void boundary commands. By default, the segment type remains an arc until the you manually change the value.
shape_conversion_msg_disabled	Set to suppress warning messages when converting shape type between dynamic and static shapes.
shape_drag_move	Set to enable dragging of a shape using mouse in the shape edit command.
shape_full_round_expand_rko	Set to enable expansion required to round corners of shapes and voids if acute angle trim control is set to full round. If you have route keepouts in your design, these do not normally require expansion beyond the keepout's outline, but in this mode, additional clearance is required to allow for the rounding of corners.

shape_in_rko_keep_shape_filled	Set to leave a filled etch piece in the design and show a DRC for a dynamic shape fully inside a route keepout area. By default, any dynamic shape fully inside of a route keepout area is deleted, leaving an empty shape with no etch pieces. These can be difficult to locate in the drawing for removal, requiring you to turn on boundary layer visibility and check the shape status report.
shape_local_temp	Set to use the operating system TEMP or TMP variable to store files during shape voiding. This improves performance if your design is located on a network file server. The temp directory on the system should have enough space for 8 Megabyte of storage.
shape_merge_props	Set for the shape merge command to also merge properties when merging two shapes. If the two shapes have duplicated properties, the property value on the first selected shape is maintained.
shape_no_ripupthermal	Set to change the default response for the static shape thermal rip-up question from Yes to No. This means that pressing Enter will not rip-up the thermals.
shape_noclip_rki	Set to stop clipping etch shapes when they cross route keepin (pre-15.5 functionality). By default, etch shape is clipped to the route keepin. Shapes added outside of the keepin are not clipped and generate DRCs.
shape_rki_autoclip	Set to preserve the original dynamic shape boundary and re-clip it to the route keepin during any dynamic shape update. This allows automatic update when a shape intersects the route keepin; shapes completely outside the route keepin are not affected. By default, dynamic shape boundaries are clipped to the route keepin. Caution: Using this variable may have performance implications.

Voiding

av_endcapstyle	Specify the geometry of void created around the end point of a cline for static shapes. Use to change void results when via/pin pad sizes are less than or equal to the line thickness. The default, a blank field, uses an octagon endcap. Setting this variable is not recommended.
av_inline	Specify the distance between pins during autovoid processing to determine if pins are voided as a group for static shapes. The distance must be greater than zero. The default is 100. Works only for horizontally and vertically aligned pins of the same size. To take advantage of this, set shape parameter to "inline voiding".
av_revoid_on_multi_select	Set to restore previous behavior when adding voids to static shapes. When set, if multiple objects are selected to be voided, the entire shape will be updated. Note that this may result in DRC errors in other areas of the shape not linked to the selected items if any constraints or settings have been modified.
av_squarecorners	Set to restore 16.6 behavior for square and rectangle pads where voids have square corners. Default is to round corners to the DRC spacing. Applies only to static shapes.
av_thermal_extend	Specify the extent of thermal relief clines generated during autovoid processing for static shapes, that is, how far into the shape thermals should extend. By default, thermals connect from a pin to 5 mils inside the shape. If shape area between pins is less than 5 mils, lowering the value to 2 or 3 creates more thermal connections.
dv_endcapstyle	Specify the geometry of void created around the end point of a cline for dynamic shapes. Avoid using this variable. First try oversizing the voids by a small value to address voiding issues.
legacypadsuppress	Set for static copper shapes to retain the pad to shape size even if pads are suppressed. Pads might be suppressed for some static copper shapes to enable legacy boards that used Gerber style pad suppression to maintain shape voiding when updated.
pad_drcplus	Specify a value that will be added to the DRC space set in shape parameters to increase the void size around pads for static shapes. Set this variable when autovoid generates DRC's for pin to shape spacing problems.

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Signal_analysis Settings

anl_min_void_area	Specify, in mils, the smallest void that should be considered in plane shapes, when non-ideal plane modeling is needed, that is, the "Shield" buttons are turned off in the stack-up description. The default value is "99", signifying that voids with an area less than 99x99 square mils will be ignored.
anl_show_coupled_trace	Set to get multi-trace model name, which can be used to get the coupled RLGC matrices. The 'Display' - 'Parasitic' command finds the crosstalk neighbors (within the geometry window) and shows the multi-trace model name.
avoid_matched_delay_calculations	Set to compute no delay for pin pairs with relative propagation delay constraints if the constraint is defined as length rather than delay. Since the field solver is used to compute delay values, this prevents the field solver from being run when the constraint is in length. For these cases the Delay column in the Constraint Manager Relative Propagation Delay worksheet will contain zeroes.
directconvolutionwithapproximation	Set to use an accelerated S parameter simulation algorithm, which will improve the time domain simulation performance of circuits containing S parameters.
enforce_structure_symmetry	Set for the BEM2D solver to use the nearest ground as lower ground for strip line cases. By default, BEM2D treats upper ground and lower ground differently methodology-wide so you see a minor difference numerically in C/L and the propagation delay.

enforce_welement_simulation	Set to model all cline segments as distributed elements. By default, cline segments shorter than the simulation timestep are modeled as lumped elements.
fix_all_t_points	Set to NOT move T-Points moved during topology assignment.
frequency_at_max_loss_tangent_in_ghz	Specify the frequency (in GHz) where the dielectric losses are maximum to control the non-linear dependency of the loss tangent to the signal frequency. The field solver uses this value to calculate the asymptotic behavior of the frequency-dependent G parameter. The default value is 1 GHz.
ignore_mapping_discrete_values	Set to match discretes by type (resistor, capacitor, or inductor) and not values when mapping an Electrical Cset topology to an XNet.
max_mappings_factor	Specify an integer multiplier to increase the number of mappings tried when mapping an Electrical CSet topology to an XNet. For example, a value of 10 means that the limit is increased by 10X. For very large topologies that have many pins or T-points this limit can cause a "no mapping found" error.
no_duplicate_model_checks	Set to NOT check Iml or Dml models with duplicate names.
no_pullup_diff_pairs	Set to NOT create a differential pair if one side of the differential pair only consists of a pin connected to a pullup or pulldown resistor.
num_new_iml_models_before_save	Define the number of new IML models that must be added to the IML working library before this library is saved to disk. The value must be an integer greater than zero. By default, this value is set to 50. For simulations that generate a large number of IML models, frequently writing the IML working library to disk can create a performance problem.

sig_mapfile_orgpath	Specify '1' to set the "Include ORIGINAL Model Path in Map File" option on the Signal Model Assignment form by default.
sig_pinuse_frozen	Set to NOT update pin use codes for components that is being assigned a package device model.By default, when a packaged device model is assigned to a component, the pin use codes are updated to match the type of buffer model that is assigned to each pin.
sigxp_allowoldrevs	Set to import newer SigXplorer topology to an earlier release of Constraint Manager. Any part of the topology that is not legal in the earlier release is ignored.

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SKILL Settings

skill_height	Specify the height of the TelSKILL input window on MS Windows. Value can be any number between 10 and 50. Default is 24.
skill_linebuffer	Specify the scrollbuffer lines for the TelSKILL input window on MS Windows. Value can be any number between 40 and 2500. Default is 250 lines.
skill_width	Specify the width of the TelSKILL input window on MS Windows. Value can be any number between 40 and 140. Default is 80.
telskill	Set to be able to enter SKILL information in xterm on Linux or an additional command window on Windows. Do not run Allegro layout editors in the background with this variable set on Linux.
telskill_nomsg	Set to direct only SKILL outputs to a TelSKILL window, if present. Other messages are shown in their intended message areas. This option does not apply if SKILL out (on Linux) is directed to the tty window.
telskill_notty	Set on Linux to create a separate TelSKILL window if the telskill environment variable is set.

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UI Settings

App_modes

appmode	Specify the initial tool application mode (none, generaledit, etchedit, placementedit, ifp, signalintegrity, or rfedit_appm). 'none' disables pre-selection. By default, the application mode that was in use on the previous invocation of the tool is used.

Browse

browser_nodircheck	Set to have the change directory checkbox in file browsers initially unset. By default, the main file browsers (say, File - Open) have the checkbox initially set while secondary file browsers (say, scripts) have it initially unset.
browser_nosticky	Set to open the current working directory when using the file browser. By default, file browser opens the last opened directory.
browser_type	Choose file and directory browser appearance. Replaces browser_win31 variable. Default (win2000) is a browser with the place bar. NT eliminates the place bar (15.x browser compatibility). The win31 setting uses an old two-pane Windows 3.1 browser. Unix currently does not support the place bar browser.
browser_win31	Applies to pre-16.0 releases. Set to use the older Windows 3.1 file browser. Use browser_type variable for post 15.x releases.
filemgr_unix	Specify a third-party file manager or change the default file manager appearance. Alternatively use the CDE file manager, dtfile. For example to use the CDE browser set: dtfile %s where the %s allows the substitution of the directory name. Applies to UNIX platforms for the filemgr command. Default is GNOME's nautilus.

filemgr_windows	Specify a third-party explorer or change the default explorer appearance. For example to enable an alternative two-pane explorer set: explorer /e,/root,%s or default explorer: explorer %s where the %s allows the substitution of the directory name. Applies only to Windows for the filemgr command. Default is explorer.
new_filedialog_disable	When set, replaces the Allegro file browser with the native system browser.
new_filedialog_fast_icons	When set, use simple icons in the default Allegro browser for improved browser performance.
nolast_directory	Set to open layout editors in the current working directory when started with no command-line arguments. By default, the editors use the last directory stored in ::/pcbenv/allegro.ini. This (with variable nolast_file) restores old 12.0 behavior. Requires restart.
nolast_file	Set to open Allegro editor in the current working directory when started with no command-line arguments. By default, the editors use the last directory stored in ::/pcbenv/allegro.ini. This (with variable nolast_file) restores old 12.0 behavior. Requires restart.
old_scriptbrowser	Set to use a file browser for replaying scripts instead of an Allegro data browser that supports SCRIPTPATH. This restores 13.6 behavior.
padlib_filebrowser	Set to use the file browser instead of a library path browser for the padeditlib command (Tools-Padstack-Modify Library Padstack)

Control_panel

addpin_default_space	Specify a seed value for spacing fields used by the add pin command in the Options pane. Value can be a number; units will default to current symbol units. Value can also include a length unit (MIL, MICRON, and so on.) where the value will be converted to the current symbol units.
color_lastgroup	Set to use the last displayed class to determine the initial display panel in the Color and Visibility dialog. By default, the Color and Visibility dialog uses the current active class in the options panel to determine the initial display panel.

color_nofilmrecord	Set to disable the display of artwork films in the view scheme control of the Visibility pane. By default, the view scheme control contains both artwork films and external user-defined view scheme files.
color_nosort	Set to disable sorting of subclasses in the tree control of the Color and Visibility dialog. By default, the subclasses for most classes in the tree control are sorted.
find_name_auto_clear	Set to edit or reuse the string for the next find-by-name query. Enable this variable to restore the default behavior prior to the 22.1 release, which clears the field automatically if a value matching the name is found.
find_nongui_reject	Specify the threshold value and behavior of the reject list that appears when a pick is rejected. By default, when you reject a pick and there are more than two elements in the reject buffer, a form shows the list of elements in the buffer. Specify an integer value to set the minimum buffer size for which the reject list appears. A value of "Always" disables the reject list form and the next item in the reject buffer is automatically selected.
find_reject_graphics	Specify the display behavior of an element selected in the reject list. You can specify the selected element to be blinked (Blink), highlighted (Highlight), or unchanged (Off). The default is Blink. Note that there could be performance issues with the highlighting of some elements. Requires restart.
vis_activelayer	Set and then choose the 'All' cell of a row in the Visibility Pane to set that row's Etch/Conductor to be the active layer. By default, the Visibility pane will not change the active layer.
wv_voltage_nets	Set to display all highlighted VOLTAGE net elements in the world view (pre-14.0 mode). By default, only displays pins of nets with the NO_RAT or VOLTAGE property. Default mode may improve interactive performance on boards with large number of clines on highlighted voltage nets.

Fonts

fontface	Specify the font name used in forms. Default is "Segoe UI" on Windows, and "DejaVu Sans" on Linux.

fontfixedface	Specify the fixed font name used in forms using fixed fonts. Default is "courier".
fontsize	Specify the font size used in forms. Default is 8.
fontweight	Specify the font weight used in forms. Values are between 0 and 99. Default is 50.

General

allegro_abortmsg	Specify your own message to be displayed if Allegro editors exit abruptly. Default message suggests downloading the latest HotFix and contacting customer support. For large sites, specify a common message for all users in the CDS_SITE env file; for example, stating your protocol and contacts.
allegro_allow_canvas_in_front	Set to allow the main canvas window to be in front of dialogs and forms. This is mainly useful when working on a smaller screen with limited resolution, or when you absolutely need to be able to see the entire canvas for making design decisions.
allegro_default_coordinates	Choose the default coordinate display. In the 'relative' mode, coordinate values are displayed relative to the previous pick. This may also be toggled by pressing the button in the lower status bar of the main window or with the xymode command.
allegro_history	Specify the command history length for both the Allegro command line and the TelSKILL development window. Default is 200. A value of 0 disables history.
allegro_lock_toolbars	Set to lock application toolbar icon strips to prevent accidental movement when the wrong area is clicked and dragged. Default is disabled, allowing for toolbar customization.
allegro_noabort_confirm	Set to suppress the confirmation message when Allegro editors exit abruptly. Include the variable in scripts that run Allegro editors in the unattended mode.

allegro_noghosting	Set if you experience problems on Vista or Windows 7 with Allegro showing a "Not Responding" message when running scripts or SKILL programs. On other Operating Systems this option is ignored.
allegro_savehist	Specify the number of last commands to be stored in a file, that is read into the history buffer next time the program is run. Controls if history buffers should be saved to /pcbenv on exit. Default is off.
allegro_theme	Sets the theme for Allegro and its associated applications. This changes the color palette only of the application itself. It does not change colors assigned to objects and layers in the design.
artist_use_orcad_menu	Set this preference to continue to use the OrCAD menu layout in Allegro PCB Artist when migrating from OrCAD PCB Designer.
cdsdoc_shownav	Set to open Cadence Help document browser, which lists all installed and configured documents, along with the help content. Default is to not show the document browser.
display_main_nosaved_geometry	Specify whether to save user sizing or positioning of the program's main window. Set to 'position' to save only window locations. Set to 'size' to save only window size. Set to 'both' to save neither position nor size. Use display_nosaved_geometry variable for secondary windows.
display_nosaved_geometry	Specify whether to save user sizing or positioning of windows. Set to 'position' to save only window locations. Set to 'size' to save only window sizing. If set to 'both', no window information is saved. This does not apply to the main window.
helpcmd_execute	Set to run a command instead of showing help when using 'helpcmd'.
left_right_dock_occupy_corners	Set to allow sub windows of left-right dockwidget type to occupy corners of the main window.
noabout	Set to suppress splash screen on startup.

Html

allegro_html	Set to use a HTML viewing for text windows. Set by default.
allegro_html_no_links	When opening files for HTML-based viewing, enable if your files have already been configured with cross-probing and other links embedded. This will disable the automatic link generation for coordinate values and similar text.
allegro_html_qt	Set to use a new modern HTML window. Set by default.
browser_text_size	Specify the default font size used in the HTML text browser windows. Note that, if this variable is set, you will not be able to use Control + Mouse Wheel to change the font size in the window once opened, as the text size has been explicitly configured. If unset, the HTML browser will use the font size defined by the fontsize variable, if set.
http_netscape	Set in UNIX to use an alternative HTML viewer. By default, Netscape is used. Alternative browser must support the netscape -remote and -openURL command-line arguments and netscape-remote X protocol. Allegro has been verified with Netscape 7 and Mozilla 1.4.
http_newwindow	Set in UNIX to open a new HTML window in the current virtual desktop By default, an existing Netscape window is reused even if it is in a different virtual desktop then the program.

Input

allegro_alt_alias	Set to allow the alt key to be used when defining alias definitions. The alias should use the @ character to represent ALT being held down when pressing the desired alphanumeric key. Function keys cannot be used in an alias. Menu shortcuts take precedent over alias.

allegro_html_link_set_pick	When clicking links from an HTML or text window, such as the show element display, a zoom center action is performed. This does NOT update the last pick for your active interactive command. Enable this variable to register the pick against the command for subsequent incremental pick actions.
allegro_no_autocomplete	Set to disable the auto-complete capability of the Allegro command line. This can be toggled on or off at any time during the running of the tool session. Most commonly, you would do this if you have many commands with similar names and want to make sure the tool does not auto complete and run a command other than your intended one.
allegro_no_text_auto_select	Set to disable the automatic pre-selection of text in a text edit of most Allegro UI windows. This overrides the behavior and instead will position the cursor in the text at the location clicked. Both methods are optimized for different use models. If you typically replace the entire string, auto select prevents keystrokes, but for editing strings, it may add key presses to get to the right position.
allegro_shift_alias	Set to allow the shift key to be used when defining alias definitions. The alias should use the ` character to represent SHIFT being held down when pressing the desired alphanumeric key. NOTE Enabling these aliases will mean that typing in the command line will require use of the CAPSLOCK key to enter upper case letters. Use with caution.
canvascommandmode	Set to change behavior back to 15.0 mode, where the Enter key is required when typing in commands. In the default mode, when cursor is in the graphics canvas and an alias is recognized, it is immediately run without the need of the Enter key. To have type-in command mode the cursor must be clicked in the console (TITO) area.
cmd_linebuffer	Specify the history length in the canvas/message area (TITO window). Default is 200 lines and may be set anywhere from 50 to 1000 lines. The environment variable, skill_linebuffer, provides the same control for the SKILL type-in window.
designhdl_pan	Set to pan or roam with mouse. By default, mouse location is fixed.

form_oldreturn	Set this variable to cause a carriage return to "tab" to the next field in forms. By default, a carriage return in a form is equivalent to clicking the default button.
no_dragpopup	Set to use strokes by just dragging with the right mouse button. With this option, you lose the ability to select popup menu items by doing a right mouse button drag. Instead, you have to click twice with the right mouse button, once to see the popup and a second time to select a popup item (works like the ValidUI based allegro_layout). By default, to use strokes you must hold down the Ctrl key when pressing the right mouse button.
no_shiftpopup	Set to get roam capability for Shift + right-click, say, for two-button mouse devices, such as notebooks. By default, the mouse Shift + right-click is used for pre-selection popup. Normal pre-selection without the Shift modifier will still function with this option.
unix_numlock	Set only on Linux if you see multiple characters echoed to the command area when you press the keypad. On certain Linux implementations, 'Numlock' setting might not be detected correctly on startup. This variable does not apply to Windows.

License

all_license_choices	Set to show all products supported by a program in the Product Choices dialog. By default, only the licenses you have in your license file are shown. When set, this can improve tool startup performance but you may see many more products in the choice dialog. Tip
allegro_license_caching	Set to cache license to improve tool startup performance. Do not use this option if you change license servers frequently. To reset license caching, check "Reset license cache" in the toolswap dialog.Set by default.

cds_ng_licenses	Set for the software to check for NG licenses. This allows access to some Cadence evaluation functionality if you have the require licenses. When enabled, it may cause tool startup slowness if you have multiple Cadence license servers in your CDS_LIC_FILE and one or more of these servers have a slow 'ping' response or high network packet drops.
license_nolegacy	Set to not list legacy product in the Change Editor dialog. This intended for CAD administrators to set for a site. By default, Change Editor lists all products available from the license server.

Padstack_editor

padstack_allow_connect_point_off_pad	Set to allow offsets for pads that would result in the drill hole being full, or partially, outside of the pad's definition. By default, this is not allowed and is an error. This variable is also aliased as CPT_OFF_PAD in past versions of the tool. That variable name may be removed in future versions of the tool.
padstack_allow_nonplated_thru	Set to allow non-plating to be selected for Thru Pin padstacks. By default, the Padstack Editor prevents non-plated hole plating for Thru Pin padstack usage to avoid connection issues made from multiple layers that require plating.
padstack_allow_null	Set to be able to define pad stacks containing only mask layers (pre-release 16.01 behavior).By default, pad stacks cannot be defined for no-etch (conductor) layers.
padstack_hole_outside	Set to display an error if multi-drill padstack drill array overlap the pad boundaries. By default, this is a warning. If made an error, you will not be able to save the pad stack.
padstack_mechanical_plated	Set to display an error if a mechanical hole is specified as plated but has no regular pads defined. If not set, this will be listed as a warning and save will still be permitted.

padstack_nowarning_display	Set to disable warning messages before file save in Padstack Editor for automatic pad stack creation.
padstack_nowarning_drill	Set to suppress the Padstack Editor warning when a drill hole is equal to or larger than the smallest pad size.

Remote

allegro_no_ownerdraw	Set to improve drop-down menu performance by disabling bitmaps shown in the menus. Requires restart.
roam_slowconnection	Set to improves roam control when using the middle mouse button to roam over high latency connections like VNC, Remote Desktop, or remote X WAN connection. Side effect of setting this variable is the cursor is not kept at its starting location. This option should not be used for running the software locally.

RF

use_floating_gui	Set to use floating GUI for RF autoplace and RF clearance commands.

Script

noconfirm	Set to disable prompts confirming certain actions. Use this variable only with scripts.
noconfirm_startup	Set to suppress confirmer windows on startup. These inform you of warnings or errors in the Allegro startup files. Messages suppressed with this option are not journaled.
noformscriptbutton	Set for scripts NOT to record add/reset button in forms. When set, print to script for a form containing add/reset buttons that can include add and reset as commands. Replay of the script updates values and then performs RESET.

script_keepformopen	Set to keep the script dialog open across script replay. Default is to close form during replay.
script_startup	Specify the script name used on startup. The program name is appended to the name provided (<program>_<name>), and filename is looked up using SCRIPTPATH. No warning is issued if script cannot be found. For more flexibility, use the "-s <script>" option when starting the program. Example: "script_startup = foo" results in looking for allegro_foo.scr when starting allegro and pad_designer_foo.scr with pad_designer.

Startpage

allegro_no_startpage	Set to disable Allegro start page.
allegro_startpage_alwaysshow	Set to always show start page on startup.

Title

Title variable strings are truncated to a maximum of 20 characters. Title bar space is at a premium when long project paths are present; recommend strings shorter than 20 be used.

title_allegro	Specify text to be appended to the title bar of PCB Editor.
title_allegro_viewer_plus	Specify text to be appended to the title bar of the allegro_viewer_plus program.
title_apd	Specify text to be appended to the title bar of APD.
title_cdnsip	Specify text to be appended to the title bar of the cdnsip program.
title_dir_length	Specify the length of the directory name in title bar before truncation. The minimum is 20 characters and the maximum is 120 characters. Default is 40 characters. Setting this field too long may hide other fields in the title bar.
title_sigxp	Specify text to be appended to the title bar of SigXplorer.

Undo

max_undo_memory	Specify the maximum memory (in MB) for storing undo history. Default is 20 MegaBytes. The range is 0 to 500.
undo_depth	Specify the maximum number of commands for Undo history. More undo history takes more memory. Default is 10 commands. The range is 0 to 100 commands. The actual number of commands in the undo buffer is dynamically determined based upon this value and the undo memory consumed to undo each command, the total of which must not exceed max_undo_memory.

Wizards

icp_bga_place_bounds	Set to create place bound or DFA bound shapes in the symbol definition for the BGA creation tools, such as BGA Text in and BGA Generator.
icp_die_in_center_pins_off	Set to not use the default die center, which is symbol origin, for the DIE format import (die in) command.
icp_text_wizard_all_rel_pins	Set to export all associated pins from a related component when exporting the related pins columns in a die or BGA text out file. By default, only one pin from the other related component (BGA if exporting a die, die for BGA) is listed to increase performance and reduce file size for large, high pin count devices.
icp_text_wizard_comment_char	Specify a character other than the default # to mark a comment line for the Die, BGA, and netlist text wizards to ignore during parsing.
icp_text_wizard_default_center_pins_off	Set to not use the default origin (symbol origin) used for centering the pins if no origin is specified in the text file being imported using die/BGA text in wizards.
icp_text_wizard_display_all_lines	By default, the text wizards in the APD tool display at most 1000 lines of information. With very high pin count components, the display of all the data slows the tool down with little benefit to the user. Set this variable to display all lines at the cost of reduced performance.

icp_text_wizard_old_extents_adjust	Set to offset extents by the symbol instance origin. The offset is used when importing a file into a database later.
icp_text_wizard_pinnum_in_name	Function pin names must be unique in the database. If non-unique names are found during text import, EXTRA<n> is added to each to make it unique. These numbers are added based on the order of pins in the file. Set this option to use the physical pin number to make the name unique instead.
noshow_new_design_wiz_intro	Set to NOT display the introduction page of the New Design Wizard.
noshow_tiling_gen_wiz_intro	Set to NOT display the introduction page of the Tiling Generator Wizard.
package_gen_allow_asymmetric	Set to generate full-matrix staggered pin patterns that have an even number of rows and/or columns when using die and BGA generators. By default, the die and BGA generators create symmetric patterns only requiring an odd number of rows and columns to create a full-matrix staggered pattern.
package_gen_start_staggered	Set to start with an empty top-left corner grid for a staggered pattern. By default, the die and BGA generators start a staggered pattern with the first pin being as close to the top-left corner as possible.

Xprobe

allegro_no_xprobe	Specify the cross-probing behavior with external tools. By default, inter-tool cross-probing is enabled. If set to 'yes' both input and output communications are disabled. If set to 'exceptProjectManager', cross probing is enabled if Allegro is started from Project Manager. When Allegro is run stand-alone cross-probing is disabled.
hilite_xnet_for_net	Set to highlight/dehighlight the XNet containing the net when the net is selected.

ignore_external_highlight	Set to ignore highlight (cross-probe) messages from simultaneously running, external instances of this program.
longmsg_noxprobe	Set to disable xy center functionality from text view windows such as show element and reports. By default, clicking on a text coordinate causes the main Allegro canvas to center on that coordinate.
unique_mps_session	Set to use a unique MPS session name for each Allegro instance preventing cross-probing to any layout unless the MPS session name is provided on the command line.
xprobe_send_select	Set to send out "highlighting/dehighlighting" the message when an object is selected/un-selected.

Zoom

buttonfactor	Specify the mouse wheel zooming adjustment. By default, uses a value of 1 which zooms by a factor of 2 for every click of the mouse wheel. If less sensitivity is needed, try 0.5 or 0.25 which will zoom by a factor of 1.5 and 1.25, respectively. Range is 0.1 to 5.
no_dynamic_zoom	Set to only zoom in and zoom out using the middle mouse key. By default, middle mouse click performs dynamic zoom which provides zoom in, zoom out, window fit, and zoom center operations.
no_zoom_to_object	Set to disable the automatic zoom in operation performed to enhance the display of highlighted objects.
wheel_zoom_center	Set to zoom based on the center of the screen using the mouse wheel. By default, zooming is based on current mouse location.

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Unsupported Settings

These variables control access functionality that is of Beta quality. The Beta features are present for customer feedback but they are NOT supported or documented. Once we are satisfied with the feature's quality and functionality, they will be promoted to a core feature.

allegro_startpage_path	Specify path for the local startpage HTML files. This variable is obsolete as of 17.4 release, but remains active in the 17.2 tools.
dbdoc_fixed_private	Set for DBdoctor to remove FIXED_PRIVATE properties left behind by partitioning application. Use only if unable to MOVE symbols or modules after importing partitions.
disable_unsupported_menus	Set to hide the "Unsupported Prototypes" submenus under all menus. Commands available through these submenus are of Beta quality and change requests filed against them do not follow standard Cadence CCR policy. Environment variable name is disable_unsupported_menus.
display_geometry_by_config	Specify whether to save user sizing or positioning of windows based on current display configuration. A new geometry files will be saved driven by the computer display settings and recalled when the same display configuration is used. This does not apply to the main window. ETCH class objects.
drc_multi_region_shapes	Set to evaluate shape-to-shape spacing uniquely in each region.
enable_command_window_history	Set to enable input history and autocomplete support in the command window. This variable is obsolete as of 17.4 release, but remains active in the 17.2 tools.
layout2allegro_unsupported	Set to access the Layout to Allegro translator. In the 17.x release stream, this is an unsupported capability and will be removed in a future base release.

legacy_diffpair_checks	Set to enable the legacy differential pair DRC check algorithm. DRC checks use pre-release 17.0 behavior.
mu_enable_cnseditmode	Set to enable Constraint Edit Mode in the Symphony Team Design environment. This allows a single client exclusive access to Constraint Manager for constraints entry while everyone continues their concurrent design work. An additional button "Enter CNS Edit Mode" will be added to the Connect Tab of the Symphony window pane.
odbpp_import_utility	Set to enable the Import ODB++ feature (odbpp in command) and add Import->ODB++ under the File menu on next tool restart. This feature allows user to import ODB++ compressed/archived file and convert to intelligent Allegro objects such as symbols, traces, vias, shapes, nets, etc on conductor layers to have a workable and editable database.
optimize_in_channel	Specify the channel size (air gap) between pins/vias for center cline segments after Auto Breakout. For example, if set to 50, cline segments will center between pins/vias less than or equal to 50 apart. A value of 0 turns off centering.
shape_layer_visibility_env	Set to see 'ship' column in the visibility tab to control the visibility of etch shapes. By layer, check to enable shape display and uncheck to suppress shape display. Shapes remain selectable and active while not visible. This can improve locating and viewing of traces on the same layer and relative to plane shapes on adjacent layers.
void_auto_oversize	Set to allow overriding of the oversize value in the shape parameters form. Due to database requirements that all locations and end points snap to a discrete grid point, shapes often need to oversize voids slightly in order to meet spacing values while also snapping to this grid. As a result, a small oversize is applied to the DRC constraint spacing value to achieve a DRC-free design.