cadence®

Allegro® X System Capture User Guide

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1

Allegro X System Capture

Allegro X System Capture offers a complete ecosystem for PCB design. System Capture offers scalable data management, ranging from individual designers to designers working in enterprises. From within System Capture you can:

- Create libraries and parts
- Create system-level designs
- Create block diagrams
- Capture design logic or intent
- Create symbols
- Generate layout files
- Use components from different applications and external data sources
- Reuse designs from other schematic-capture applications
- Use Tcl commands to complete common design tasks
- Store versions with data-driven design and integrated servers
- Analyze integrity

Tip

Before starting System Capture, ensure that your system meets the minimum *Hardware and software requirements* as listed in the installation documentation.

Related Topics

Hardware and software requirements

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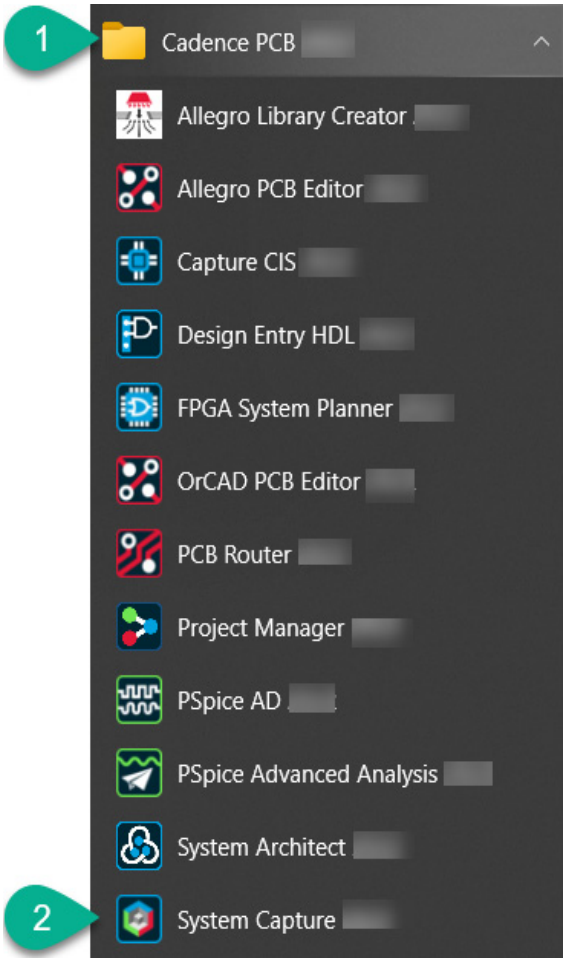
Launching System Capture

You can launch System Capture using the Windows menu or command line. To start System Capture:

1. Choose *Start – All Programs – Cadence PCB <release> – System Capture <release>.*



Or

Type *syscap* in a command window and press `Enter`.

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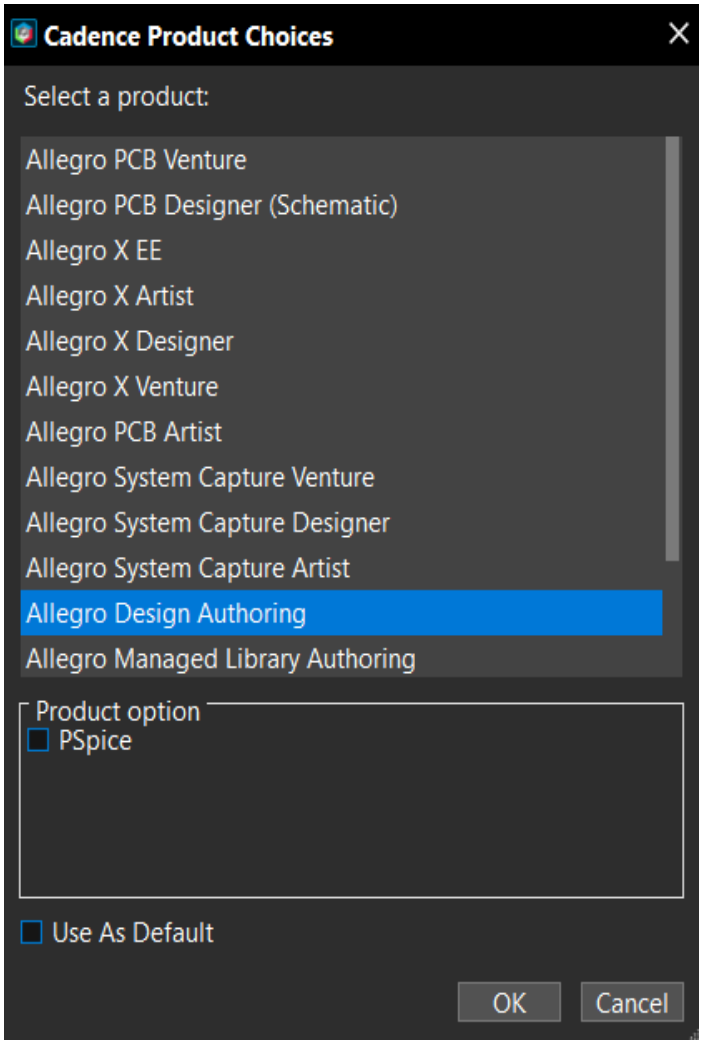
The *Cadence Product Choices* dialog box is displayed.



2. Choose a product license, such as *Allegro Design Authoring*.
3. Choose *Use As Default* to avoid having to choose a license at each launch.

   Choose *File – Change Product* to display the product choices dialog box and pick another license without restarting System Capture.

   Or,

   Choose *File – Reset Default License* or use the `cps::resetLicenseCache` Tcl command to choose a different license when System Capture restarts.
4. Click *OK*.

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System Capture is launched and the *Start Page* is displayed.

Related Topics

Creating a New Project

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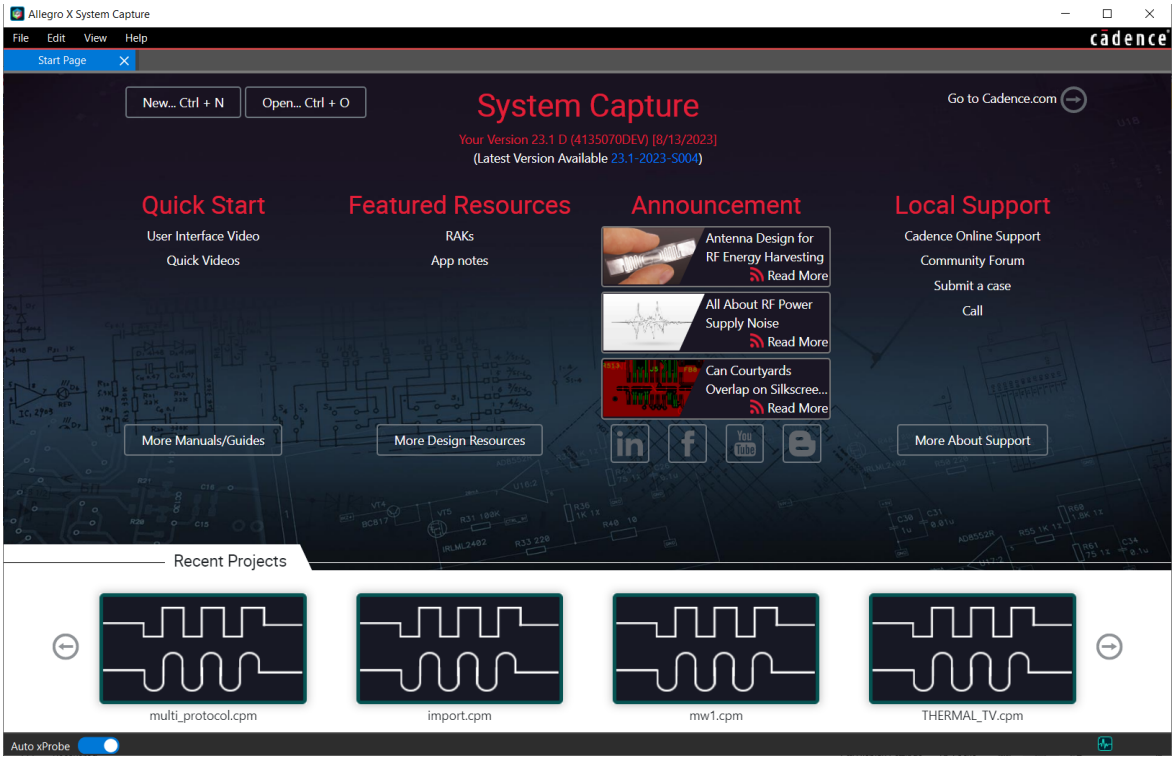
System Capture Start Page

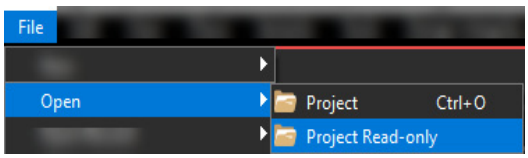
The *Start Page* is the default page displayed when you launch System Capture. You can see the version you are working with and if a newer version is available, a link to it is also displayed. The Start Page has links for training content, resources, announcements, and contacting Cadence support. From this page, you can also create new projects and access existing projects.



- *New* – Create a new project by providing basic details for a new project.
- *Open* – Browse and select an existing project.

  One instance of System Capture shows only one project. Opening multiple projects will open that many instances of System Capture. In case you try to open the same project more than once, you will be notified about an already open instance. This ensures no changes get overwritten or lost.

  - You can open projects in the read-only mode



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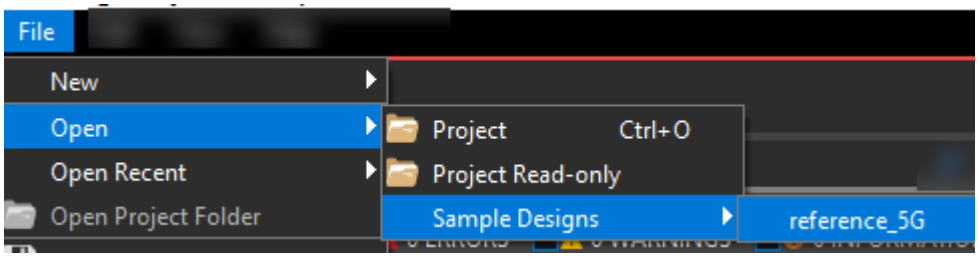
When an existing project is opened in the read-only mode, you see all schematic pages with a read-only watermark. You can only view parts of the design, such as components and constraints, without being able to make any changes.

Note: If you do not have write-access on project file you are opening, the project is automatically opened in the read-only mode.

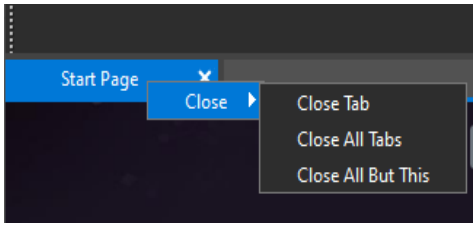
Or

- ❑ Open the sample project shipped along with System Capture.



- ■ *Recent Projects* – Open any of the recently accessed projects.

To close the *Start Page*, right-click the tab name and choose *Close – Close Tab*.



If you are working in a setup with multiple users, you see an additional option for creating projects based on templates.

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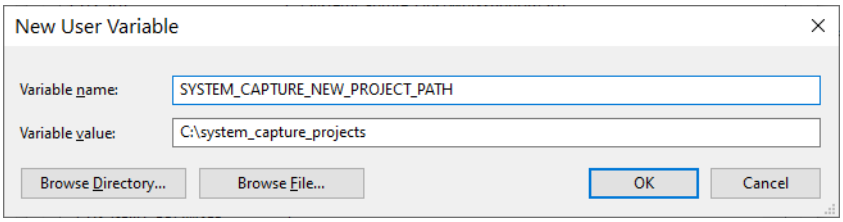
Creating a New Project

A project is the starting point of creating a design. Depending on where you are in project creation, it contains various files, such as board files, schematic files, and so on. System Capture offers many ways of working on a project, such as:

- One or more designers working on different aspects of a design.
- Existing designs being used to create versions or copies.
- Designs being created using other schematic capture applications that can be reused.

Prerequisite

- Before you create a project, you can set a default location for all new projects. To save all new projects at the same location, set a default location by creating a system variable called `SYSTEM_CAPTURE_NEW_PROJECT_PATH` and pointing it to a folder.



  Set this variable before starting System Capture as system variables are read only at start up.

- If you are working in a setup where only one library format is used, you can create an environment variable called `CDS_SYSCAP_NEWPROJ_LIBMODE` and set it to one of the following values:
  - `unified` or `libdb`
  - `DE-HDL` or `dehdl`
  - `capture`

To create a new project from the *Start Page*:

1. Click *New*.
2. Specify the project name, for example *Tutorial*.
3. Specify where to save the project.

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If the `SYSTEM_CAPTURE_NEW_PROJECT_PATH` variable is set, its location is auto-populated.

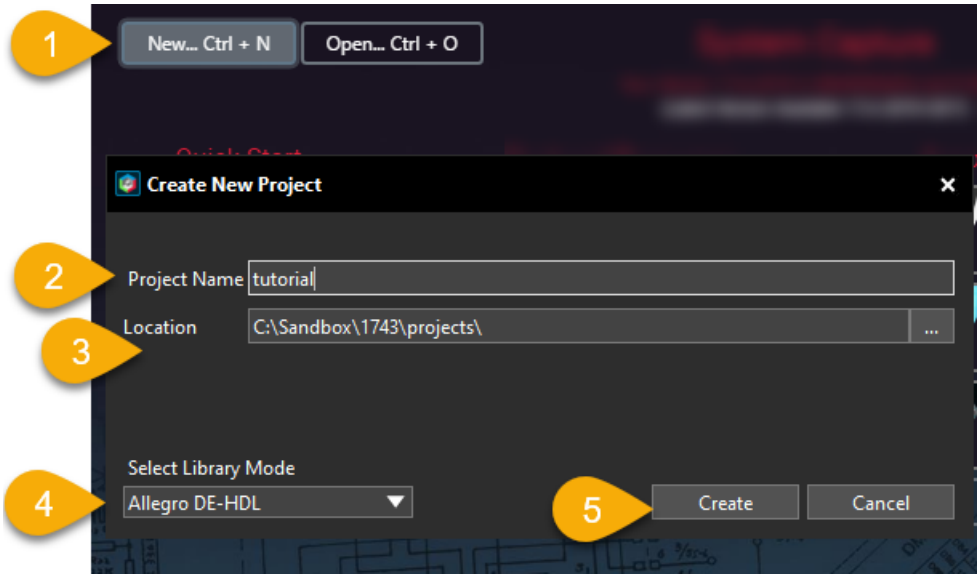
Important

The New Project dialog changes depending on whether you are connected to a remote server or not. In the example used here, System Capture is not connected to any remote server.

4. Choose the type of library this project will connect to.

A System Capture project can work with any of the following type of libraries:

- ❑ Allegro Unified
- ❑ Allegro DE-HDL
- ❑ OrCAD Capture



5. Click *Create*.

The project is created and the System Capture application opens with a blank page.

In addition to these library formats, a System Capture design has the ability to connect to the supported external data sources and download parts from there. This is explained in the *Unified Search User Guide*.

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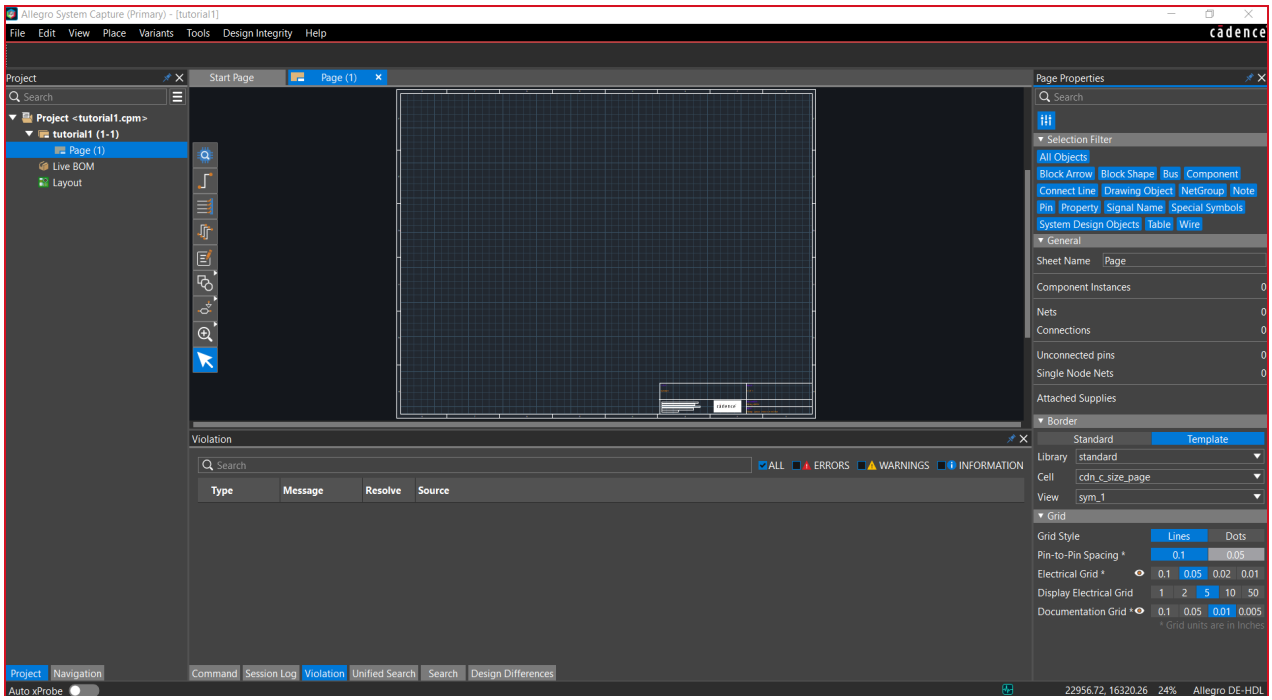
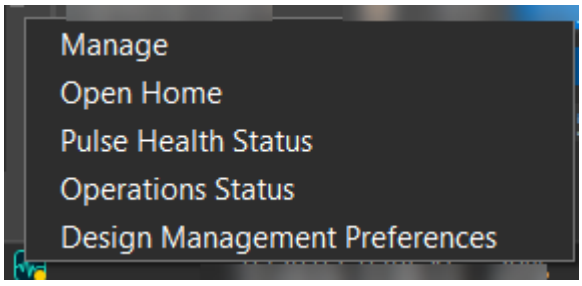
System Capture organizes schematic information in pages. Only one page of schematic information is displayed at a time. Other open windows are docked as tabbed pages.



When a project is open, you will notice an icon on the status bar. This is Pulse, which is used by System Capture internally to provide data management, library access, and *Unified Search* features to designers.

Right-click the Pulse icon on the status bar for more controls.



Pulse starts automatically and keeps running in the background. Only one instance of Pulse runs on a machine and Pulse stores design data either on the local machine or on a remote machine, depending on the settings done in Pulse Manager.

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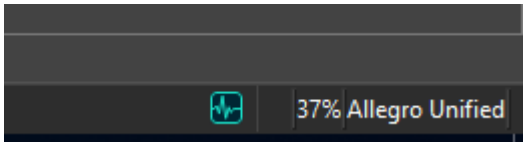
For the most part you do not need to perform any Pulse tasks, but at times, you might have to restart or shutdown the Pulse Manager. You are prompted to do so by messages from System Capture.

Pulse must be in the Running state when you start System Capture tasks. If not, the library access and version-control features remain disabled.

Important

To check the library mode of the project you are working on, check the bottom-right corner.



Related Topics

- System Maintenance in Single-Designer Environment
- User Interface of System Capture

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Creating a Project Based on an Existing Design

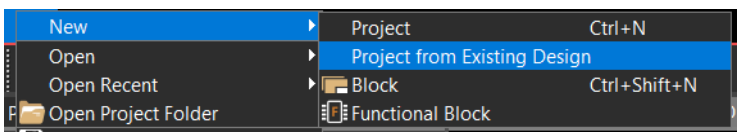
Building designs that reuse existing functionality is easier, and also saves time and effort. There are two ways in which you can reuse existing designs in System Capture:

- Reusing Designs Authored in Other Applications: To convert a DE-HDL or OrCAD Capture project into a System Capture project.
- Creating a Copy of a System Capture Design: To use a System Capture design as a starting point.

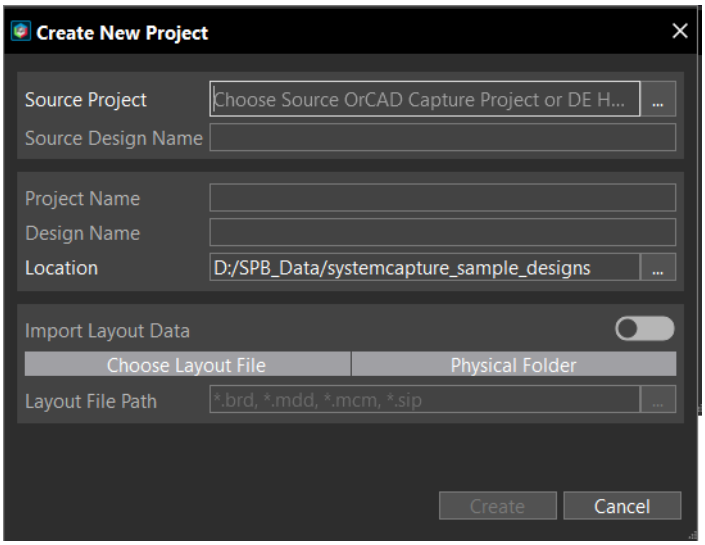
Reusing Designs Authored in Other Applications

When specifying a design created in another authoring application, such as DE-HDL or OrCAD Capture, System Capture gets configured to work with that type of design and library components. To reuse an existing design authored in another application:

1. Choose *File – New – Project from Existing Design*.



The *Create New Project* window opens.



2. Choose a DE-HDL design, OrCAD Capture design, or a project archive.

   When you select a design, the following fields are updated:

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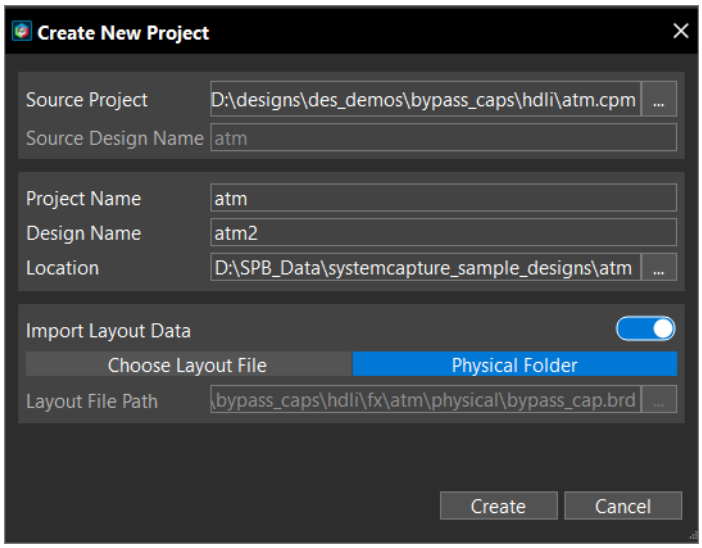
- *Project Name* based on the design chosen for both OrCAD Capture and DE-HDL designs.
- *Design name* based on the design chosen for only DE-HDL designs. This field remains blank and uneditable for OrCAD Capture designs.

3. Specify a new project name, if needed.

The *Location* field shows the default location.

4. Change the location, if needed.

For DE-HDL designs, you can import the physical layout files along with the schematics. If you choose a DE-HDL design, the *Import Layout Data option* gets enabled.



5. To import physical files, perform the next two steps:

a. Select *Import Layout Data*.

b. Choose *Physical Folder* to import the complete `Physical` folder in the DE-HDL project.

Or,

Click *Choose Layout File* and select a board file to import.

6. Click *Create*.

A new System Capture project opens, which is a copy of an existing DE-HDL or OrCAD Capture design.

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Caution

If you are creating a design based on designs created in other applications, post-processing checks and corrections are needed.

- For DE-HDL designs, refer to the *Migrating DE-HDL Designs to Allegro X System capture* guide.
- For OrCAD Capture designs, refer to the *Migrating OrCAD Capture Designs to Allegro X System Capture* guide.

Related Topics

- Migrating DE-HDL Designs to Allegro X System Capture
- Migrating OrCAD Capture Designs to Allegro X System Capture

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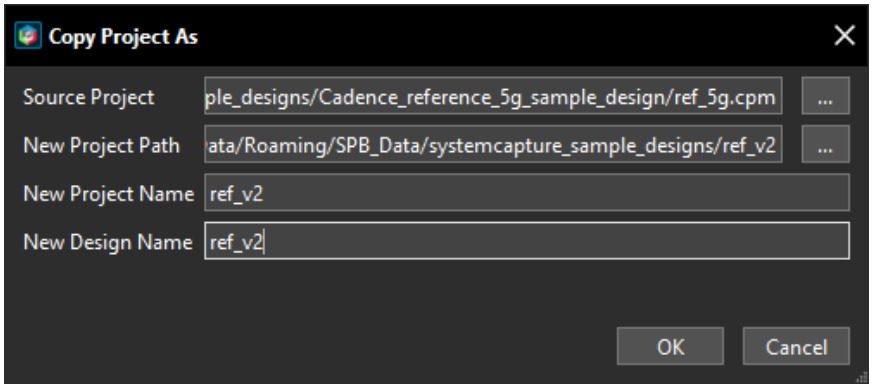
Creating a Copy of a System Capture Design

You can create a copy of a design using the Copy Project As functionality, which makes a new copy of the project with a new name and root design name. To create a copy of an open design, follow these steps:

1. Choose *File – Copy Project As.*

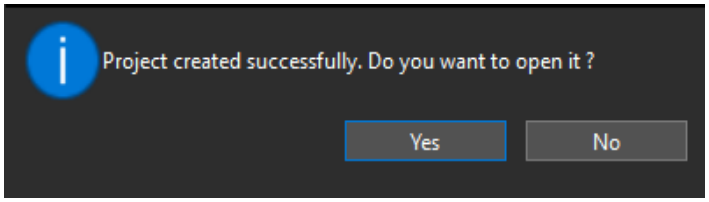
   The *Copy Project As* dialog box opens.



   The name of the project is shown as the *Source Project*. The new project details are added automatically. The location is the folder specified in the `SYSTEM_CAPTURE_NEW_PROJECT_PATH` variable. The same project name and design name are used for the copy, by default. The project name is the name of the cpm and the design name is the name for the root block in the copy.

2. Specify a different location for the new design.
3. Specify a name for the project and root design.
4. Click *OK*.

   The copying starts, and when it completes, a message displays.



5. Click *Yes* to open the newly created design.

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Important

By default, all the folders in the design get copied to the new project folder but the design information inside the folder is not modified. If you are working in a Pulse-managed environment or have used Flow Manager earlier to copy projects, set the following directives in the `CANVAS` section of the `site.cpm` file as needed:

- `rename_folders_on_copyproj` to rename files such as the board file
- `delete_folders_on_copyproj` to ensure extra files do not get copied to the new project

See *Allegro Front-End CPM Directive Reference Guide* for the details of these directives.

Related Topics

- rename_folders_on_copyproj
- delete_folders_on_copyproj

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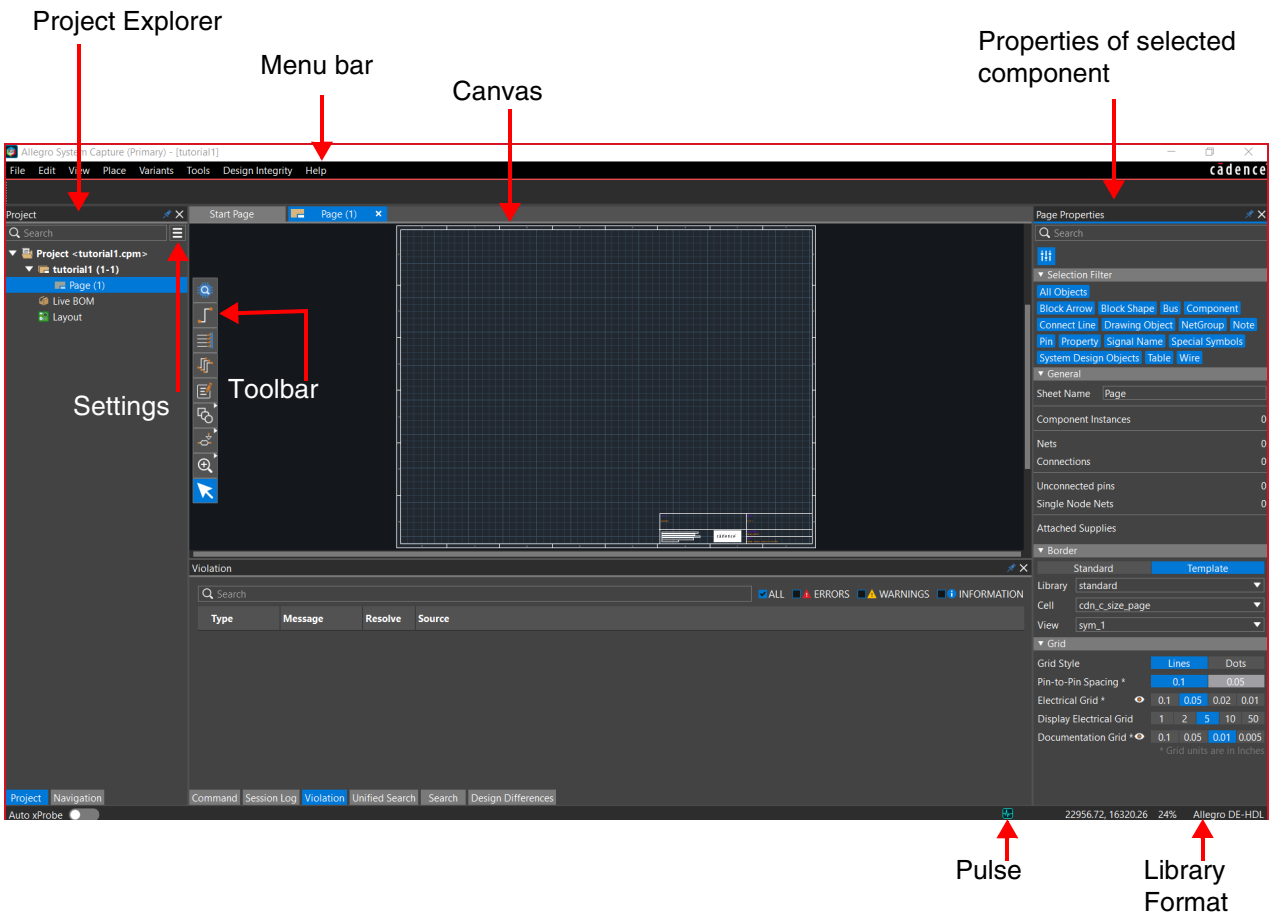
System Capture User Interface

The user interface (UI) of System Capture is easy to navigate and logically organized based on tasks that designers would perform. You can easily familiarize yourself with the options available by browsing the menus and windows. This section walks you through some of the main aspects of the UI. Once you understand the layout and how tasks are grouped, you can easily identify what all tasks can be accomplished and where do you go to control or modify any aspect of System Capture, for example, adding a library, changing the color theme, modifying colors and font for a symbol, and so on.

The schematic canvas is at the center of the main application window with room on the left and the right for additional dockable panels.



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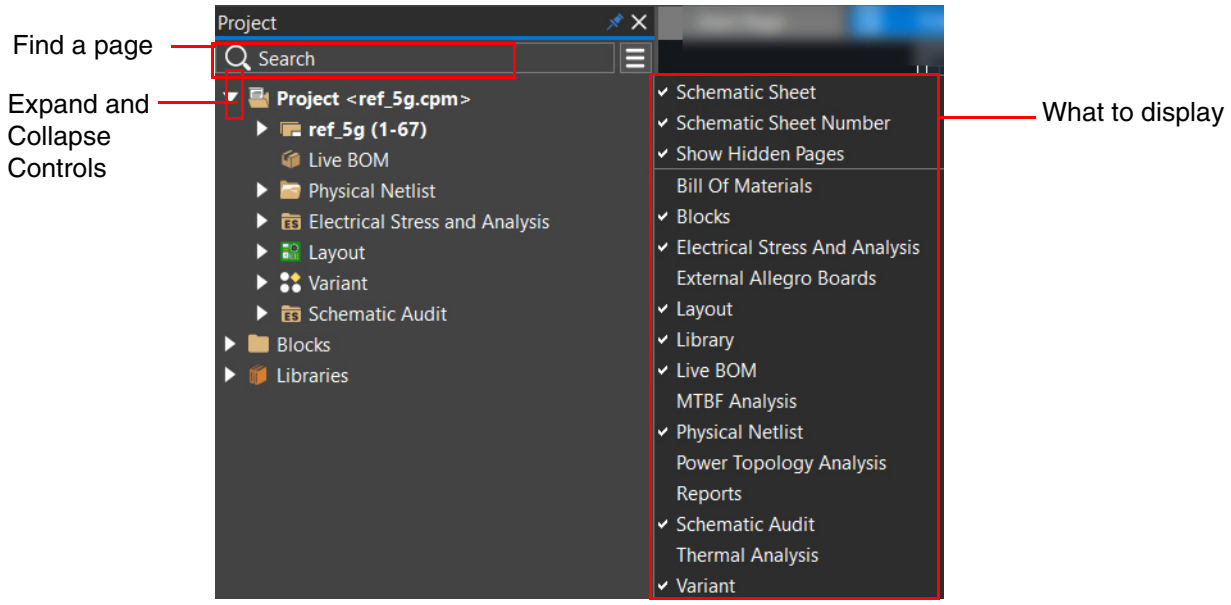
Project Explorer

The project you created is displayed with its contents as a single page. As you build the project, more content gets added to the *Project Explorer*. You can access all the components of the project, such as libraries, blocks, pages, symbols, layout files, design integrity audit results, and so on.



In this panel, you can use the:

- *Search* field to quickly locate a specific page or a block in the *Project Explorer*.
- Expand and Collapse buttons to selectively show or hide the details of the entire tree or its branches.
- *Hamburger* icon to choose what design elements you want to view in the tree.

  Apart from Schematic Sheet and Schematic sheet number, you can also display Physical Netlist, Layout, Bill of Materials, Variant, Library, Blocks, or External Allegro Boards.

You can also:

- Preview a schematic page

  Hover the mouse pointer on a schematic sheet. The thumbnail view is handy when you need to decide which sheet to open from a large number of sheets.
- Open a page

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Click any page in the Project Explorer to open the object in the appropriate editor. When you click a schematic sheet, it opens in the canvas.

Other page-related tasks are explained in the *Working with Schematic Pages* topic.

Related Topics

Working with Schematic Pages

Canvas

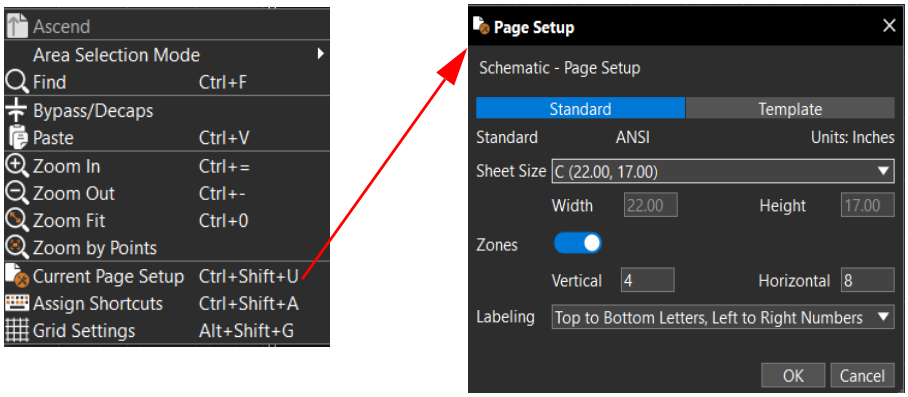
The area where the components are placed is called the canvas. The default basic settings for the page, such as grid setting and page border, are done in the project preferences.

- Page Border

  The page border can be changed for the current page or set as the default for the new pages in the project.

  - To change the border for the current page, right-click the canvas and choose *Current Page Setup*.

    This feature is useful when you need the first sheet of your schematic to have a border containing documentation of the project, which is different from the border on the rest of the sheets of the design.



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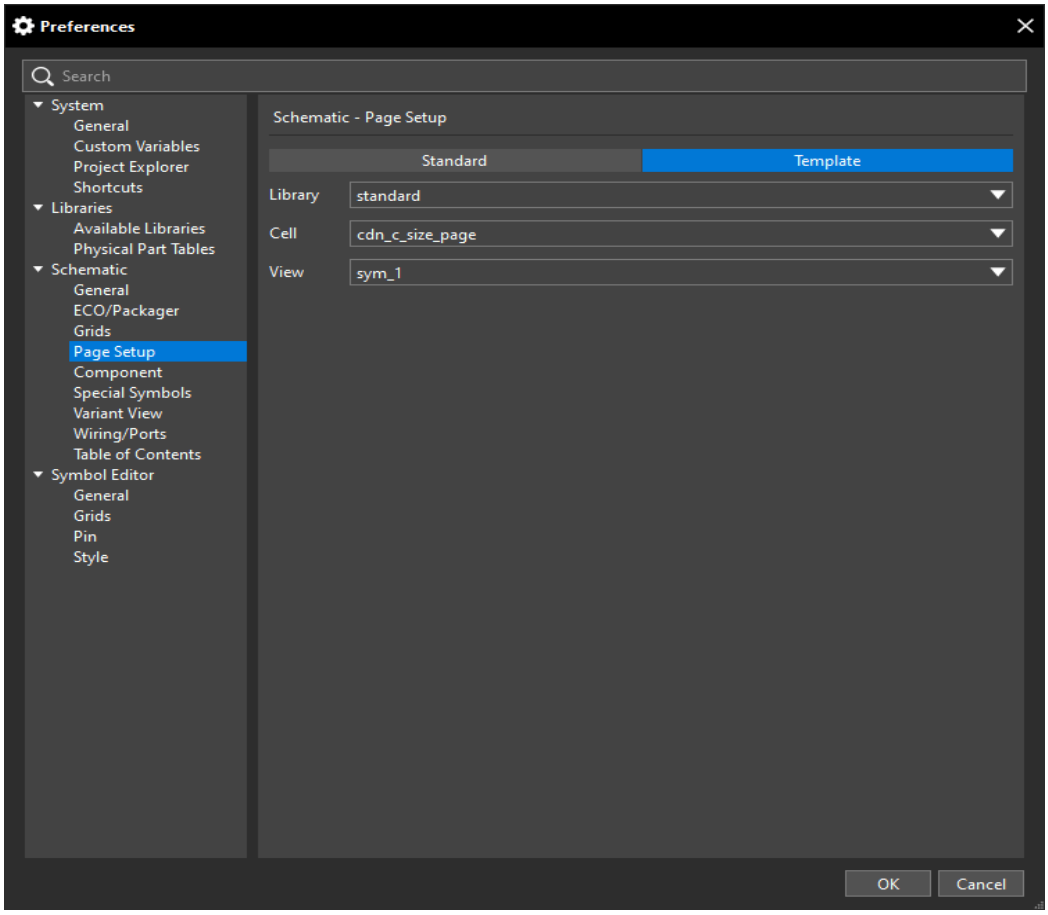
- To change the border for the project, modify the *Preferences – Schematic – Page Setup* page.



All the supported page sizes are displayed in this form. The page sizes A to E are displayed along with their dimensions. You can also specify a Custom page size.

Grid Settings

Similar to page borders, grids are an integral part of the schematic canvas. System Capture ensures that all the objects on the canvas are always placed on the grid to avoid any off-grid components in the design.

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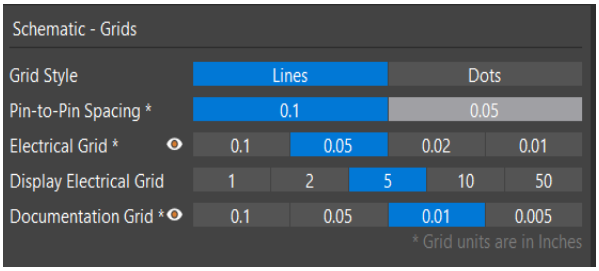
By default, the grid unit is inches. The basic unit of grids is *Pin-to-Pin Spacing*. After defining the *Pin-to-Pin Spacing* attribute, you can define the grids as its factor. The default unit is specified in the `site.cpm` file.



System Capture has two types of grids:

- Electrical Grid

  Used for placement of electrical objects on the canvas. Electrical objects include components and connecting wires–the objects that define the electrical connectivity of the design. Setting up a grid ensures that all the pins of the components are on the grid. If you try to add a part that does not have its pins on the grid, you are prompted to change the grid to a value which ensures that the component pins are on the grid.

Important

Electrical grids play a crucial role when adding components, sheets, or blocks from other designs. You can import design elements only from design that have the same or compatible electrical grid settings.

- Documentation Grid

  The display of documentation grid is optional. This grid is used for placing documentation objects on the canvas. The documentation objects include text, notes, drawing objects, and images. These objects do not contribute to the electrical connectivity of the design, but help in better documentation of the design. The documentation objects require a finer control for placement of objects, consequently, the Documentation Grid is set to a finer value than the Electrical Grid. If required, you can set the documentation grid to the same value as the electrical grid.

  You can also change the display options for the grids. You can choose to view the grid as Lines or Dots. Additionally, you can specify the distance at which you want to view the grid lines. This provides a cleaner view of the canvas.

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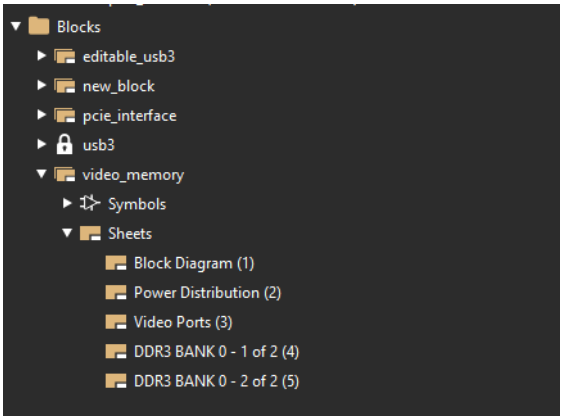
Toolbar

There is one floating toolbar in the main application window. By default, the toolbar is vertically aligned and can be docked per convenience.



Controls on this toolbar help with design operations on the canvas, such as placing a component, drawing a wire, bus, connect line, or a NetGroup. Some toolbar commands open a docking window or a panel that provides specific-information about the project. You can also add notes, auto shapes, special symbols, as well as control the zoom levels.

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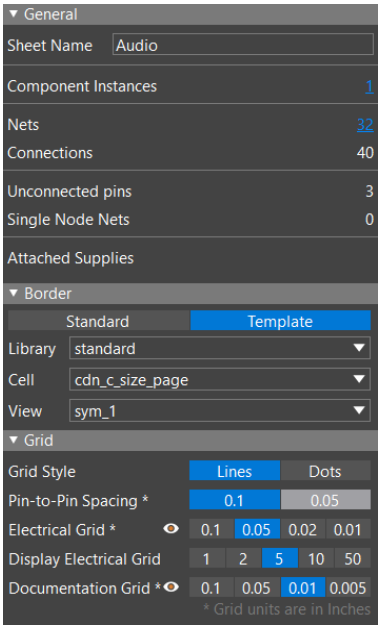
Properties Window

Shows the details of the currently selected components on the canvas. If nothing is selected or the canvas is empty, the design details are shown, such as:



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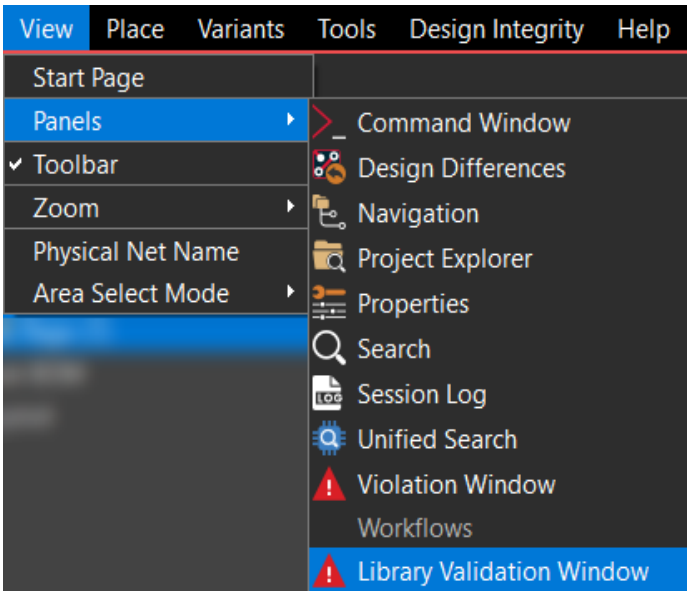
Display of System Capture Panels

When you launch System Capture, you see the windows and controls with default settings. By default, all windows retain their sizes and positions from the last session. The *View – Panels* menu has the controls for all the dockable windows.



From here you can launch the various windows available, such as Command Window, Properties, Project Explorer, Violation Window and so on.

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Unified Search

After a project is created, designers are ready to start placing components on the canvas.

To add components to your project, *Unified Search* is used, which you can start with the following menu command:

➡ *Place – Component*

Unified Search is an easy-to-use feature that supports free-text search across all configured libraries. With Unified Search, you can:

- Search and add parts from Cadence-supplied or custom libraries
- Search and add parts, symbols, footprints, and 3D images from Cadence-supported content providers — SamacSys and Ultra Librarian
- Add parts to the Live BOM

  You can directly search for and place a manufacturer part number based on electrical parameters as well as supply chain information, such as cost and availability.

In case you have been working with OrCAD Capture or DE-HDL, either as an individual designer or as part of a team, using the same libraries in System Capture is fully supported. Libraries are accessed using *Unified Search* through the Pulse infrastructure.

Related Topics

Unified Search User Guide

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Adding Components from External Sources

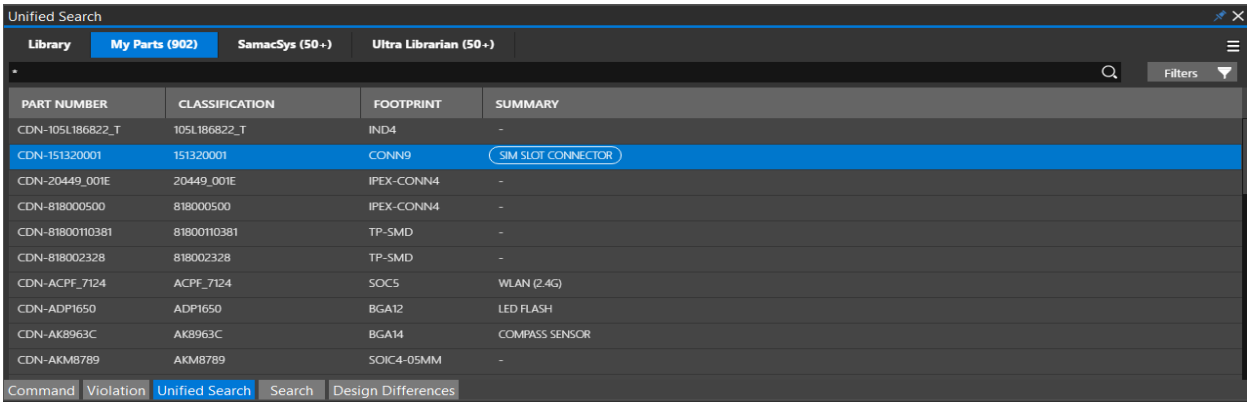
Using System Capture you can place components on the schematic from the Cadence-supported content providers, SamacSys, and Ultra Librarian.

Prerequisite

- A Cadence Support account is required.
- For Ultra Librarian parts, you also require an Ultra Librarian account.

To access components from external sources:

1. Launch *Unified Search*



2. Enter your user credentials.
3. Click *Sign in*.

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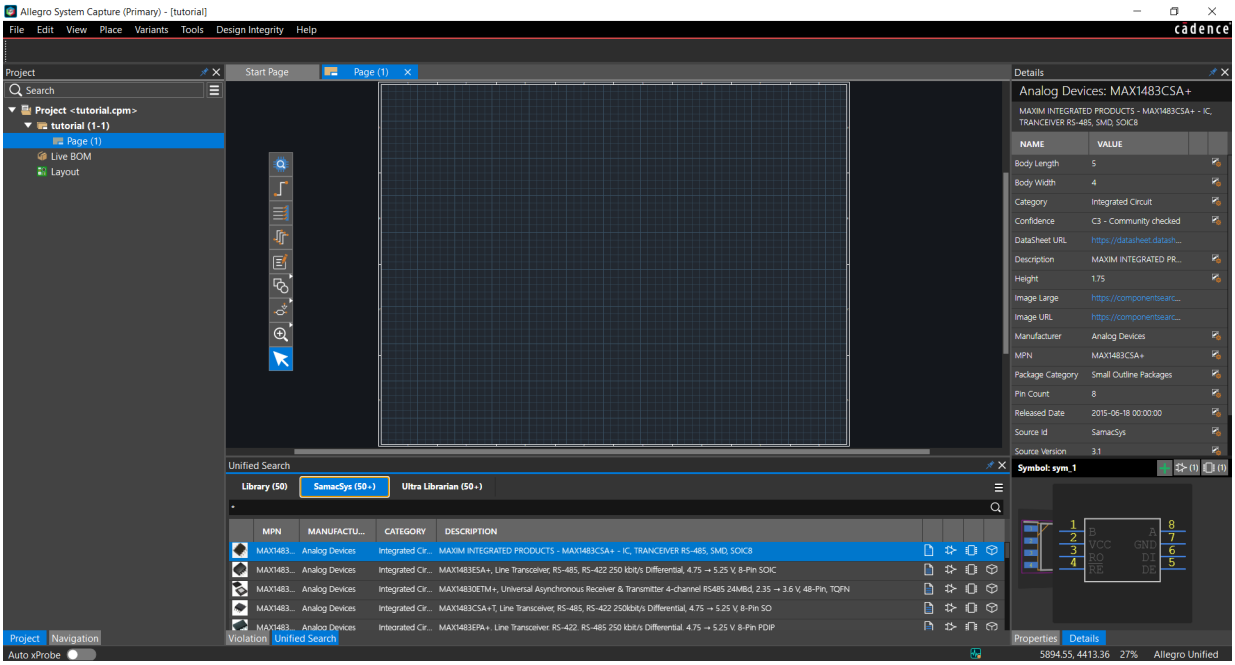
After signing in, parts from the selected external part provider are displayed.



Tip

If the *Sign in to Providers* dialog box does not appear and you see the *Library* pane, or you click the *Skip* button in the *Sign in to Providers* window, click the Global Navigation button in the *Unified Search* tab, and select the *Sign in* option.

Related Topics

- Unified Search User Guide
- Cadence Support Account

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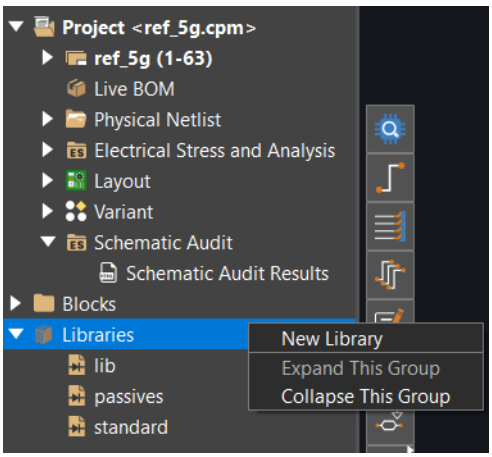
System Capture Libraries

System Capture provides a library called Unified Library. In addition to creating designs, you can also create parts, which get stored in the Unified Library.

Library-related tasks are accessible from the *Project Explorer.*



Related Topics

- Library Authoring and Editing in System Capture
- Project Explorer

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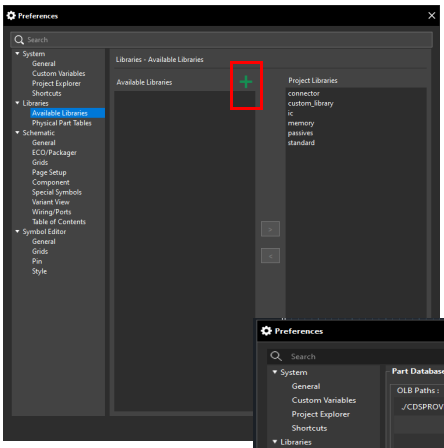
Adding Local Libraries to a Project

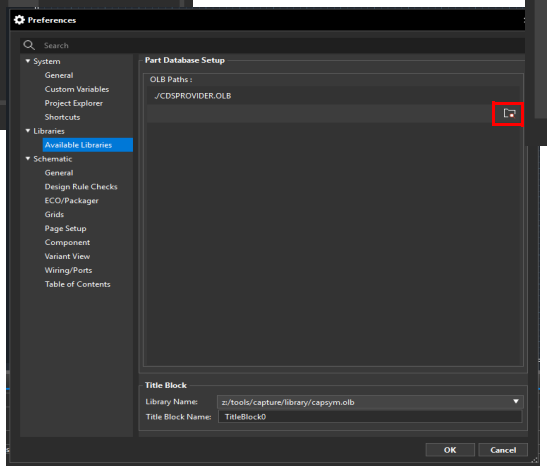
In System Capture, you can add the local libraries which have the parts that you need to your project. To do this, after opening a project:

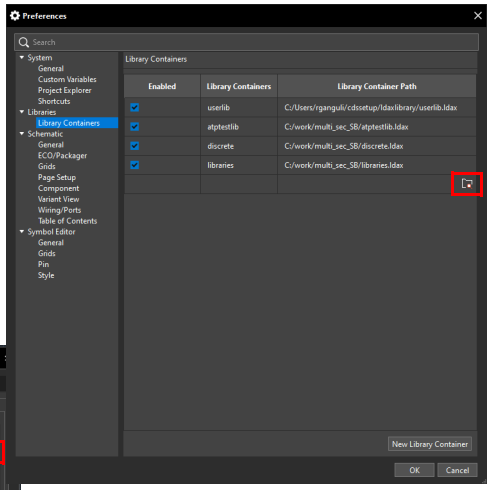
1. Choose *Edit – Preferences* to open the *Preferences* window.
2. Click *Available Libraries*.

   This tab changes depending on your project's library format.
3. Add local libraries.

DE-HDL Libraries







Allegro Unified Libraries

OrCAD Capture Libraries

- ❑ Click and choose any other locally available library for DE-HDL libraries.
- ❑ Click and choose any other locally available library for OrCAD Capture libraries or Allegro Unified libraries.

  To add multiple OrCAD Capture libraries, you can use `Ctrl+Click` or `Shift+Click` in the file explorer.

Note: Do not add the `capsym.olb` library as it is added to all OrCAD Capture-based

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projects by default.

4. Click *OK*.

Parts from the added libraries are now available in *Unified Search*.

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Working with Schematic Pages

When you create a project, a default schematic page is added and displayed. You can add or delete schematic pages depending on your requirement. As you work on the schematic design, the tasks that you perform are:

- Adding New Pages
- Creating Copies of a Page
- Renaming Pages
- Reordering Pages
- Hiding Pages
- Deleting Pages
- Importing Sheets from other Designs

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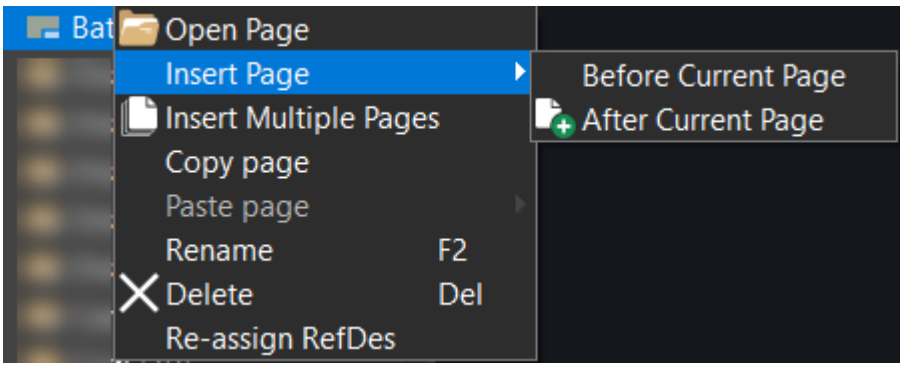
Adding New Pages

You can add one or more schematic pages in a project. You can do this by using the *Insert Page* command repeatedly or using the *Insert Multiple Pages* command and specifying the number of sheets to be inserted after the current sheet.

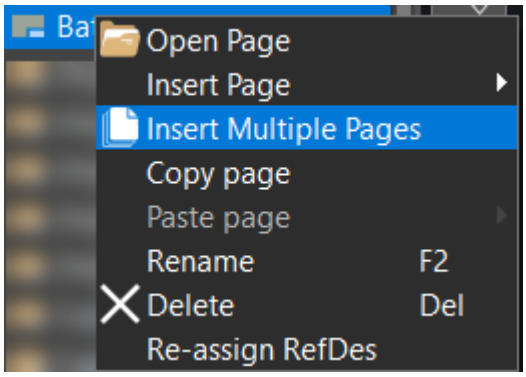
To add a page:

1. In the *Project Explorer*, right-click the first (default) sheet, and choose *Insert Page – After Current Page*.



   A new page is added after the current page. The name of the new page start with `Page<n>`, such as `Page(2)`, `Page(4)`. You can also add multiple pages in one go.

2. Right-click *a page* and choose *Insert Multiple Pages*.



3. Specify the number of pages to be added.

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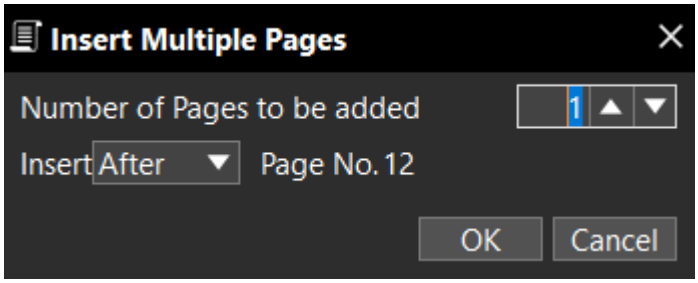
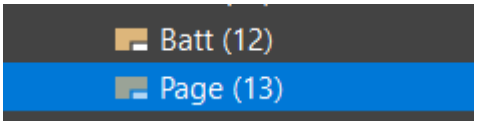
You can also specify if the pages are to be inserted before or after the selected page.



4. Click *OK*.

One new page is added after page(12):



You do not need to manually specify the sheet number after the page name. The sheet number is automatically suffixed to the page name.

Note: You cannot add multiple new pages before the first page if it is a TOC

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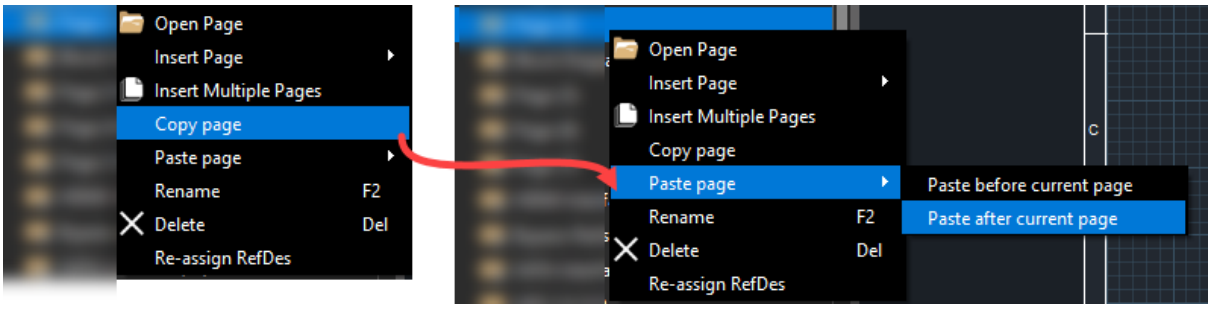
Creating Copies of a Page

You can also create copies of an existing page to reuse some part of the design. To do this, follow these steps:

1. Copy a page by right-clicking a page in the *Project Explorer* and choosing *Copy page*.
2. Paste the copied page by right-clicking a page and choosing *Paste page – Paste before* or *After current page*.

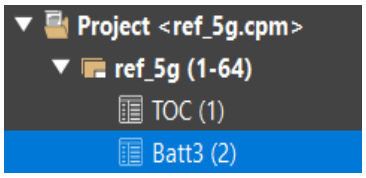


Renaming Pages

By default, a sheet is named as `Page<sheet_number>`. You can provide a meaningful name to the schematic page in the *Project Explorer*. Press `F2` or double-click the sheet name and enter a new name. Alternatively, you can right-click the sheet name and choose *Rename Page*. You can then specify the new sheet name in the dialog that opens. The newly-specified name is displayed in the *Project Explorer*.

To rename a page:

1. Right-click *page(1)* and choose *Rename* and type the new name or press `F2` and type the new name.
2. Specify a name for the page and press `Enter`.



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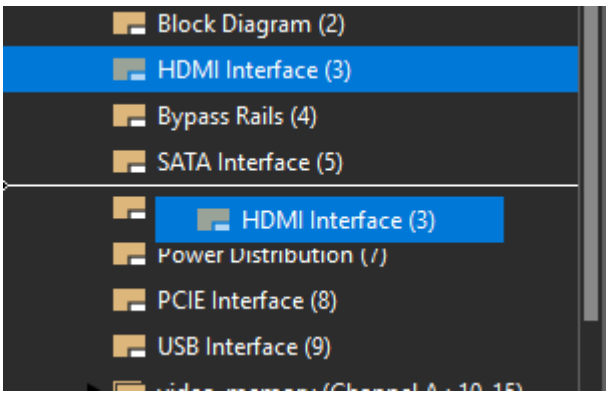
Reordering Pages

To change the sequence of pages in the *Project Explorer*, drag and move the schematic sheets to change the page order as required:



The page number in parenthesis next to the page name is automatically updated after reordering pages.

Hiding Pages

Pages without electrical data can be hidden from the design view. Printing the document and the design TOC also ignores the hidden pages.

Important

TOC pages and pages with connectivity cannot be hidden.

Prerequisite

- Set the following directives in the project cpm or site.cpm:
  - `START_CANVAS`
  - `PAGE_HIDE 'TRUE'`
  - `END_CANVAS`

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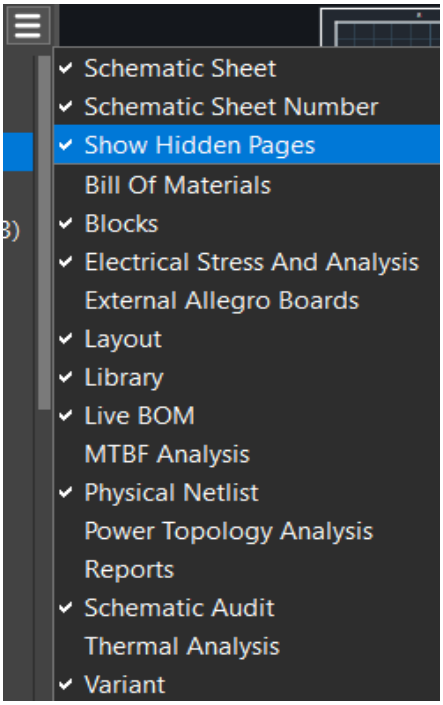
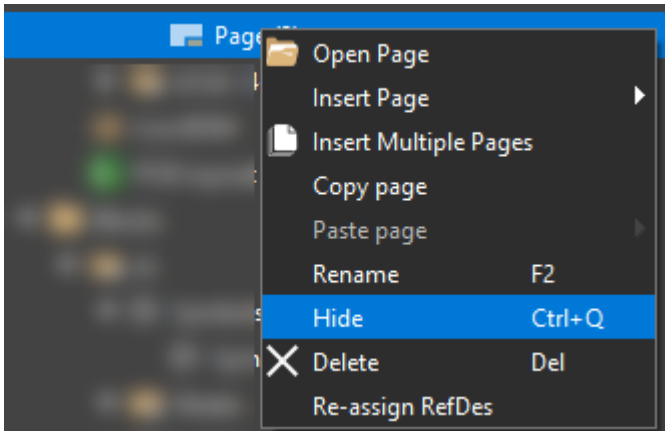
- Before hiding pages, set the *Project Explorer* display to show hidden pages. This helps to keep track of hidden pages and to show the hidden pages.



To hide a page, perform the following steps:

1. Right-click a page in *Project Explorer* and choose *Hide*.



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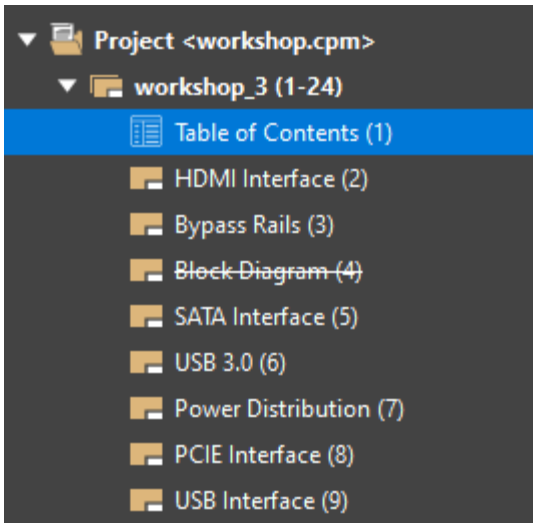
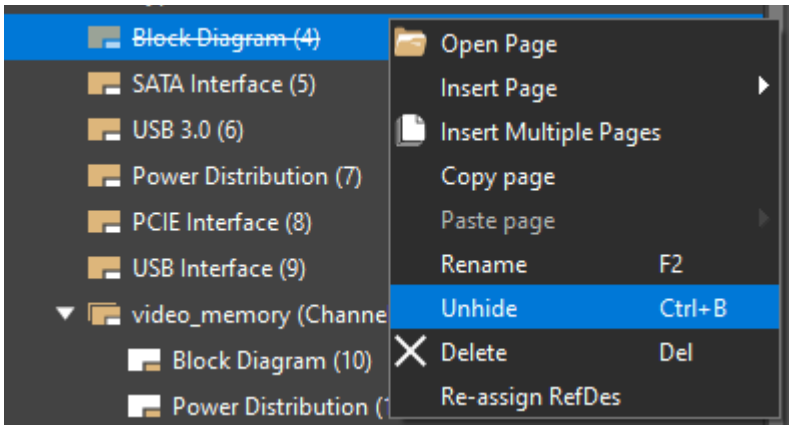
The page closes and the page name gets removed from the explorer. If the display of hidden pages is enabled, the entry for the page shows with a strikethrough in the *Project Explorer*.



Click the page to open it and see its contents.

2. To display a hidden page, right-click it in the *Project Explorer* and choose *Unhide*.



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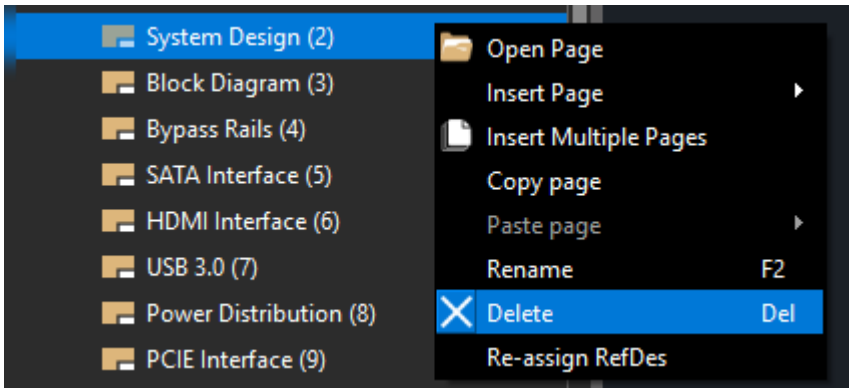
Deleting Pages

To delete the pages of a design, follow these steps:

1. Select a schematic page and press the `Delete` key.

   Alternatively, right-click a page and choose *Delete*.



   The selected page is deleted.

2. Choose *File – Save Project*.

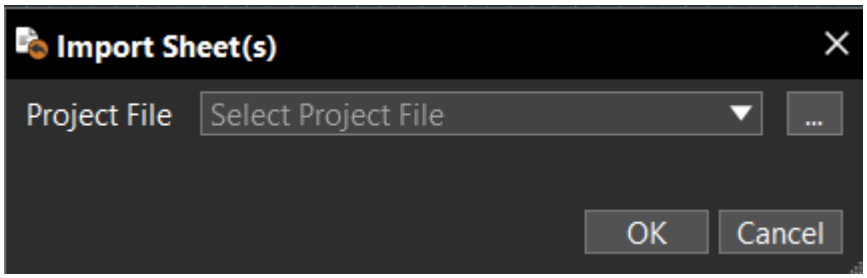
Importing Sheets from other Designs

You can import sheets from DE-HDL and System Capture designs.

To import a sheet:

1. Choose *File – Import – Sheet(s)*.

   The *Import Sheet(s)* dialog is displayed.



   You can choose a System Capture or DE-HDL project.

2. Browse to the folder where the source design is located.

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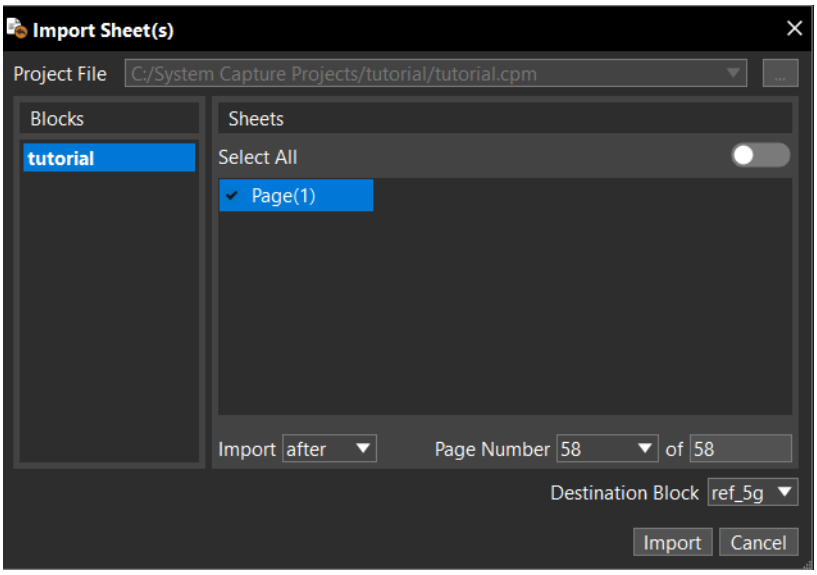
The project data is loaded.



3. Select the blocks and sheets.
4. Specify where to import and select the *Destination Block*.
5. Click the *Import* button to import the sheet.

   The sheet is imported along with all the packaging data.

   A confirmation message provides this information.
6. Close the confirmation message box.

Tip

A log file, `import_sheet.log`, having the changes is generated by the import process, at `<project>/temp/`.

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Impact on Design Elements When Replacing Sheets

When sheets are reimported into a design, the existing sheets get replaced. In most situations, the values from the source get replaced in the destination design. Refer to the following table to know what values and constraints are retained when sheets are replaced:

Design Element	Retained
Schematic	Source
Connectivity	Source
Instance	Source
Instance pin	Source
Instance properties	Source
Pin properties	Source
Pin-Net connectivity	Source
Nets	Source
Net properties	Source If a net exists on other pages of the destination design, properties deleted in source or added in destination would remain.
Voltage	Source In case of voltage values conflicting, the source voltage value wins. *Important* If a voltage is deleted in the source design, the value in the destination persists.
Base property (`MAKE_BASE`)	Source Source base value wins in conflicting cases. This property drives the PNN if it exists on the aliased net.
Constraints on nets or pins	Destination

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Design Element	Retained
Aliased nets	Constraints of the winning nets are retained. If the destination design has an alias of nets with constraints on it and aliasing is broken at the source, replace sheet restores the constraints only on the previous winning net. Remaining unaliased members lose constraints, if any.
Different voltages across blocks	The master property from lower block is retained. For example: ■ A sheet is imported for the lower-level block with a global power N1 with value +1_5V. This creates a global power net in the lower block. ■ Another power net N6 is generated in the root design that gets aliased to the net coming from the lower-level block. ■ If the voltage value on the N6 net is overridden by another value, for example 2V, and then the sheet is replaced again for the lower-level block, the overridden value of 2V is not preserved. The voltage value of +1_5V from the master net in lower-level block is retained. ■ Sheets from the lower-level block are imported again (replaced). ■ The master net N1 and its constraints are retained. ■ A new net N7 gets generated at the root level which gets aliased to N1 from the lower-level block. N7 is a new net and does not get the old overridden voltage value.

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Design Element	Retained
XNet changed in source design	Pin-pairs lost from XNet in the destination For example: ■ There is an XNet XNA in the source design and after importing the sheets, pin pairs are created on XNA in the destination design. ■ Now if XNA is split into two, creating XNets XNA and XNB in the source design and the sheet is imported again (a replace sheet operation), the XNet in the destination design also splits into two XNets XNA and XNB. ■ Pin pairs that were originally there in the destination are retained only for the connectivity that is still valid for the XNet XNA, since that is an existing xnet. ■ On the other hand, XNB is a new XNet and will not get any pin pairs.
Constraints	■ If the objects are still valid in the destination design, their constraints are preserved during replace sheet. Both, master and in context constraints of the object are retained. ■ All deleted objects and their constraints are removed during the replace sheet. ■ If a net is renamed, all the constraints captured on the net are lost.

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2

Building the Schematic

Creating a logical design involves the following design tasks:

- Adding Components to the Design
- Connecting Components
- Reassigning Reference Designators
- Using the Find and Modify Command

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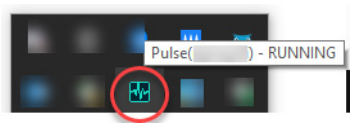
Adding Components to the Design

You can add the components from the libraries available to your project or the external data sources you are connected to. All these components are present in the *Unified Search* window.

Prerequisite

Before you start adding components, ensure that Pulse is in the Running state and there are no *Indexing in progress* messages in the Violation window. To check the status of Pulse, hover over the icon in the status bar.



To add or place a component:

1. Open the *Unified Search* window.

   Choose *View – Panels – Unified Search* or *Place – Component*. In the following image, you can see these parts:

   - Sources from where parts are available: These are:
     - The libraries available to the project
     - SamacSys
     - Ultra Librarian
   - Search: To search for components by entering their names.

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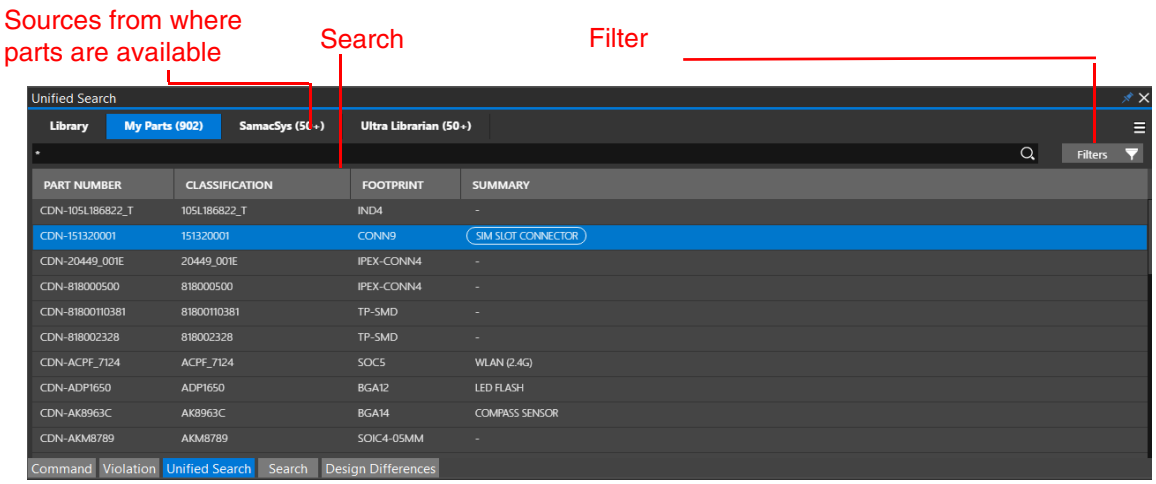
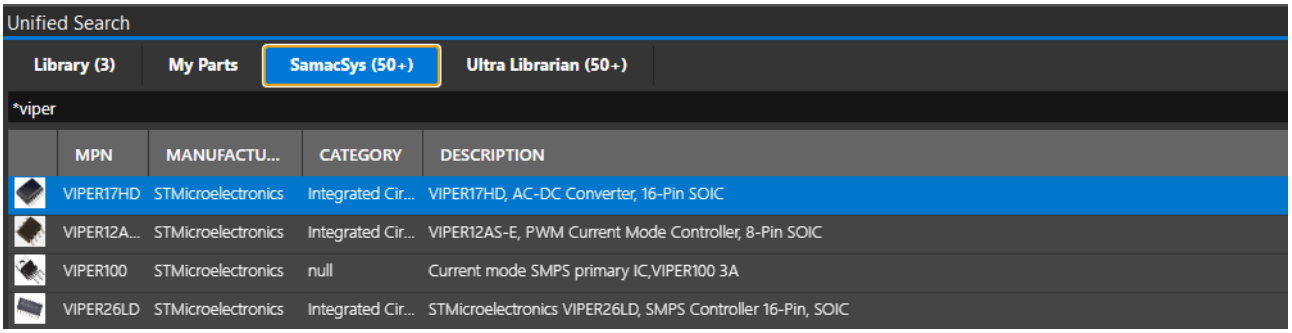
- Filter



Parts from each source are displayed in separate tabs.

2. Search for a part by entering a name in the search field.



Tip

You can choose to search parts only from a specific source, such as the libraries, by selecting the particular tab.

3. Click a row.

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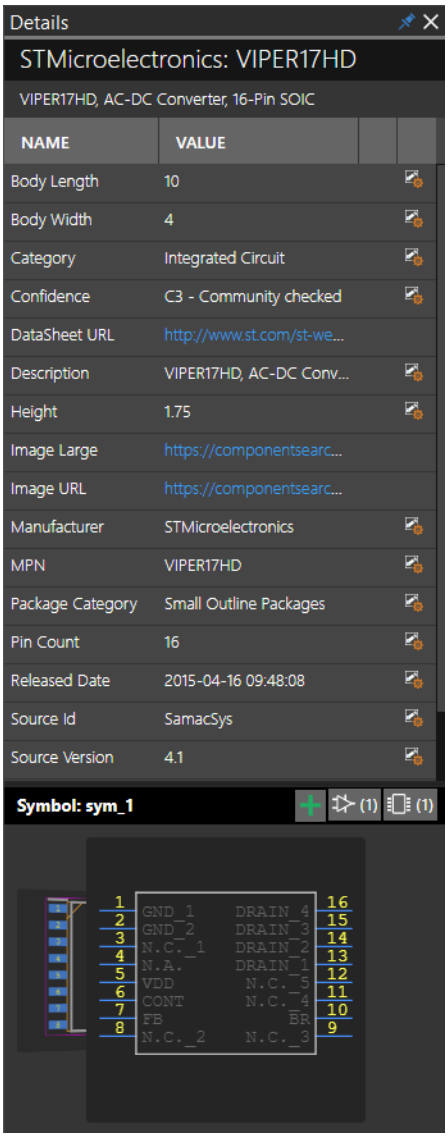
The details of the selected row are displayed in the *Part Details* window.



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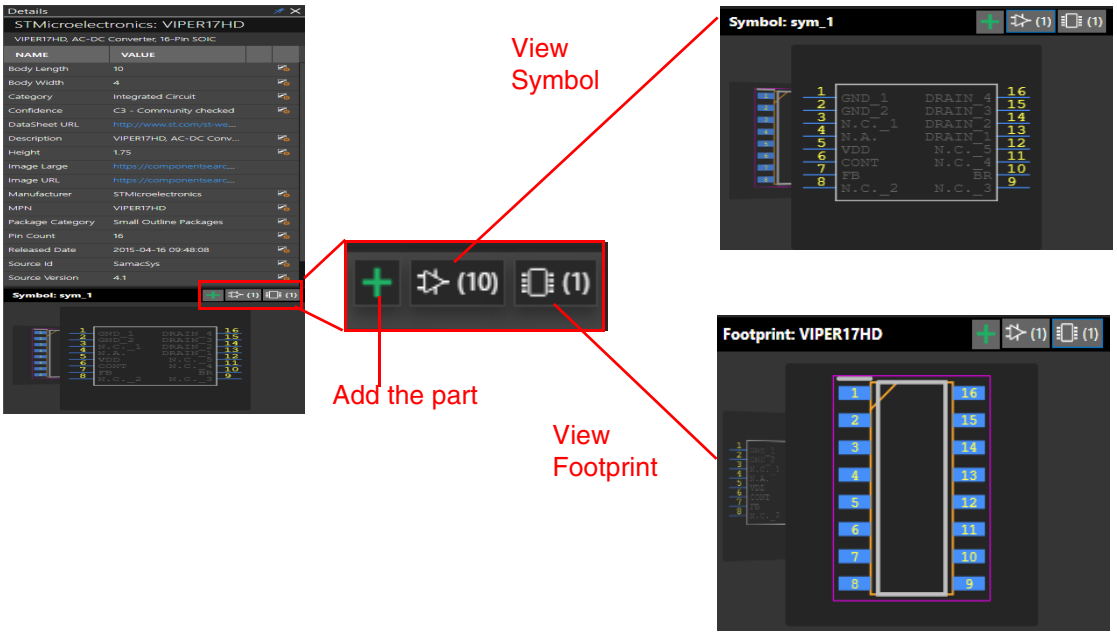
You can see the details of the selected part.



4. View the schematic and footprint models of the selected part.
5. Click *Place Part*.

   The symbol is attached to the cursor.
6. Click anywhere on the canvas to place the component on the canvas.

   After the component is placed, another instance of the component gets attached to the cursor for recursive addition.

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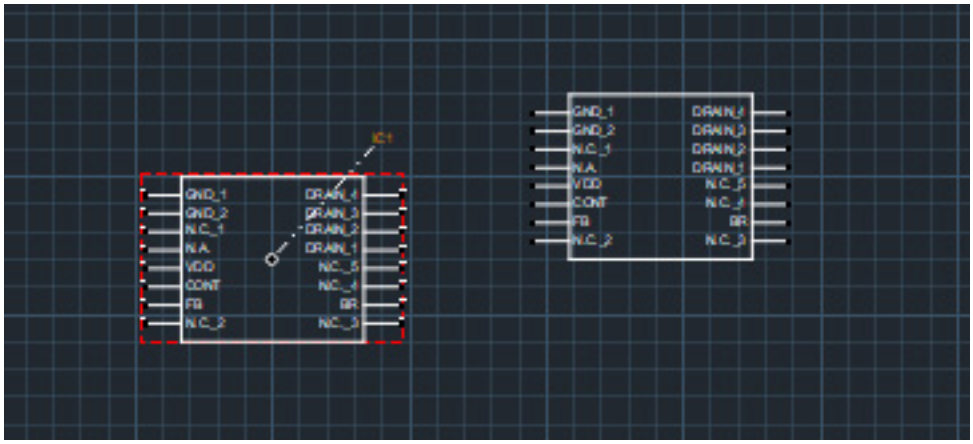
7. Right-click on the canvas and choose *Done* to complete the placement of the component.



After placing a component on the canvas, you can change the appearance of the component using the Formatting options available in the *Properties* window. The formatting operations are enabled when an object is selected on the canvas. These operations are also available when you right-click a component. To format the component, perform one of the following steps:

- Right-click a component to get a toolbar or the formatting bucket commands. Then using icons, rotate or mirror components. You can assign shortcut keys to each of these commands for quick usage.
- Select multiple components and quickly align and distribute them to create neat schematics. Similarly, you can flip a single object or a group of objects using the Mirror Vertical or Mirror Horizontal commands.

These quick commands reduce the need for manual accuracy required while placing components.

Related Topics

Connecting Components

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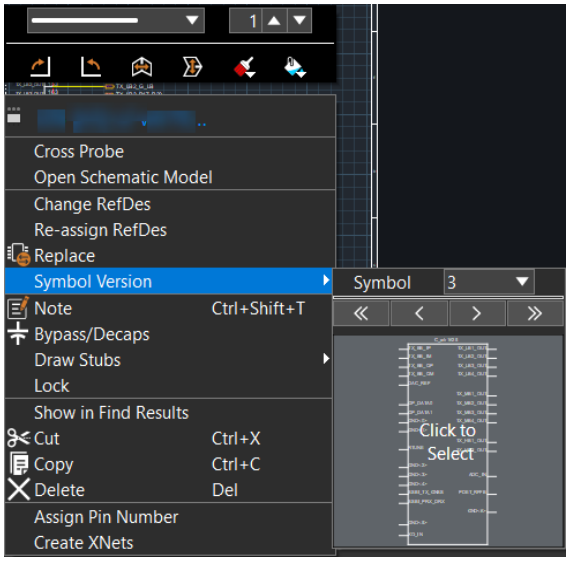
Changing the Symbol Version of a Placed Component

Many components have more than one symbols. To modify the symbol of the component, follow these steps:

1. Right-click the placed component and select *Symbol Version*.
2. Select a symbol and click the image.



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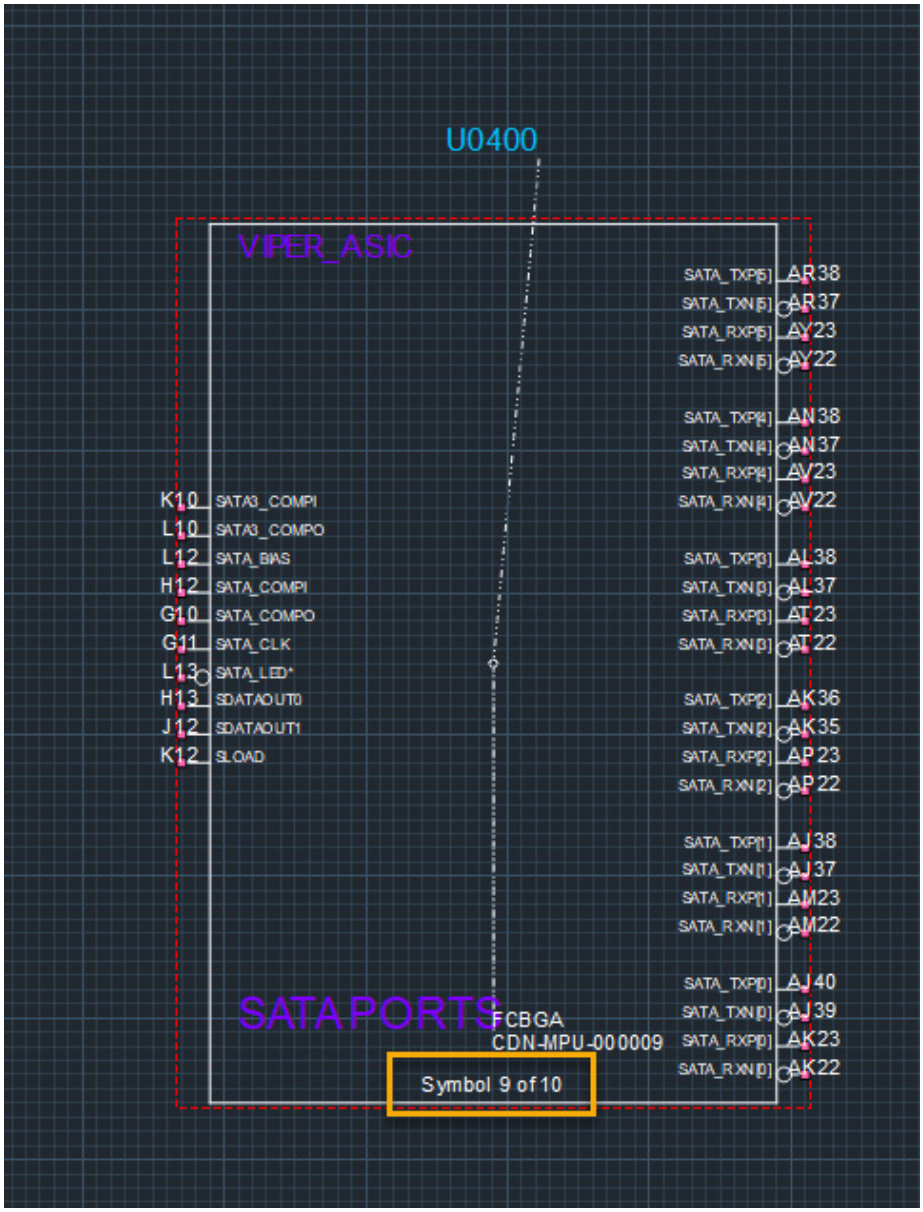
The version of the selected instance changes and the new symbol is placed on the schematic.



All the pins of the component show the unconnected pins indicator. When a net is connected to the pin, this indicator is removed from a pin.

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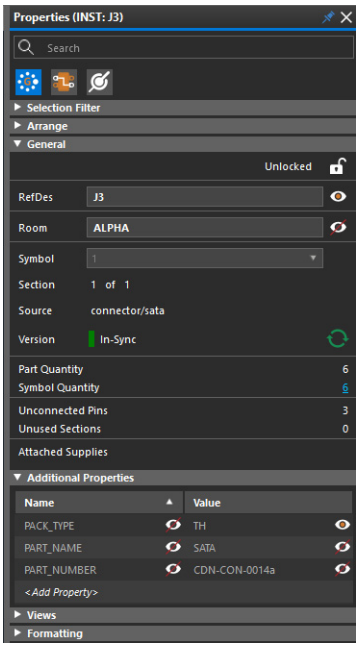
Modifying Display Properties of Selected Components

You can modify the display properties of a selected component, such as *RefDes*, *Line Width*, and so on in the *Properties* window. To do this, follow these steps:

1. Choose *View – Panels – Properties*.

   The *Properties* window opens. In the following figure you can see the *General* and *Additional* properties of the selected component.



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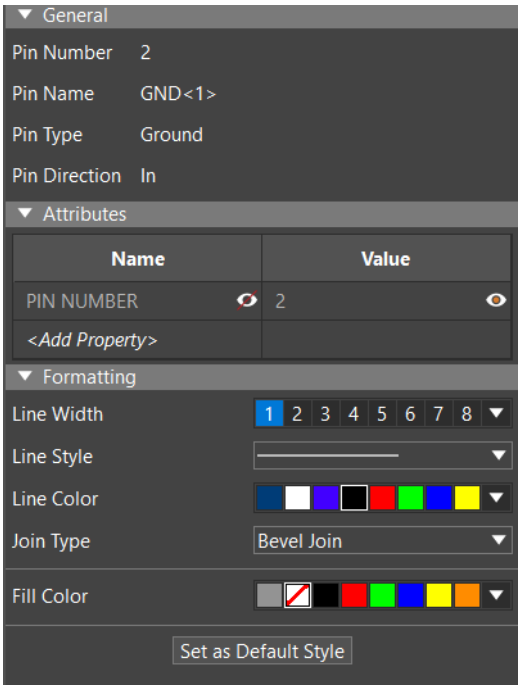
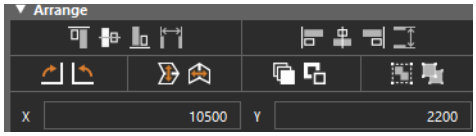
This window displays all the properties associated with the selected design object, which could be a component, special body, note, system block, or signal. As an example, clicking a pin shows the properties associated with the pin:



The property names are sorted alphabetically. For the placed component, you can see:

- Source
- Version status of the part in the design as compared to the source library

2. Modify the alignment of the component using the *Arrange* section.



3. Control the display of properties, such as RefDes, Room, and so on, from the *General* section.

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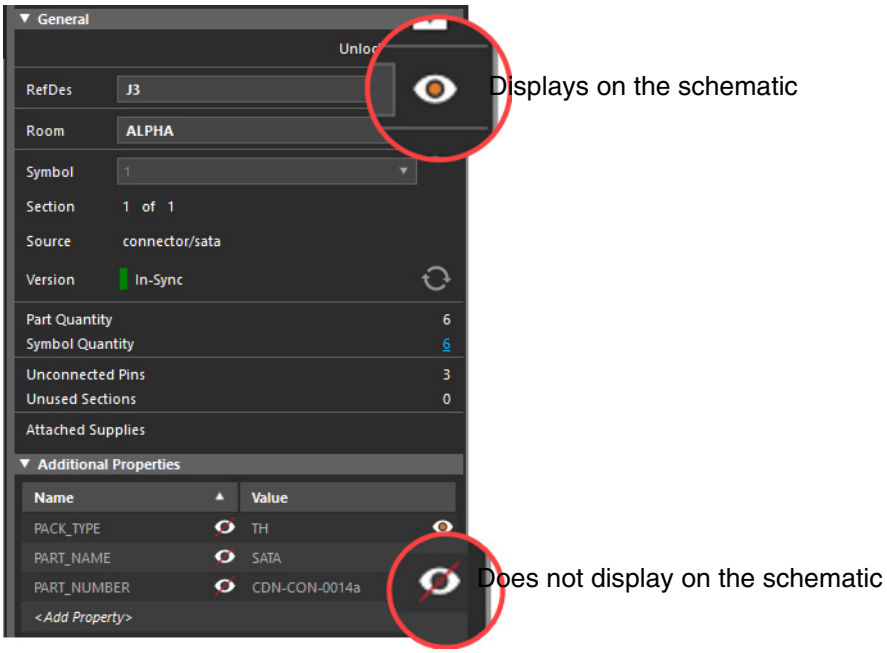
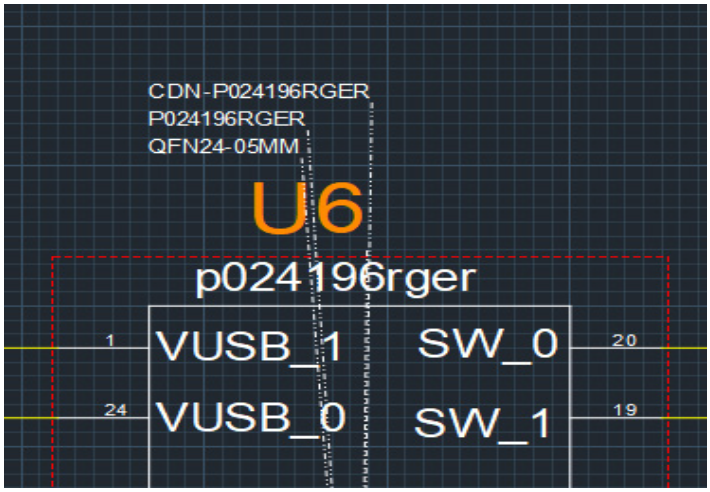
4. Click the eye icon to toggle the display.



When multiple properties are set to display, they are stacked on top-left of the component. If enough space is not available on the top-left, the properties are adjusted and displayed on the bottom-left, left, and right of the component.



5. Add properties, if needed.

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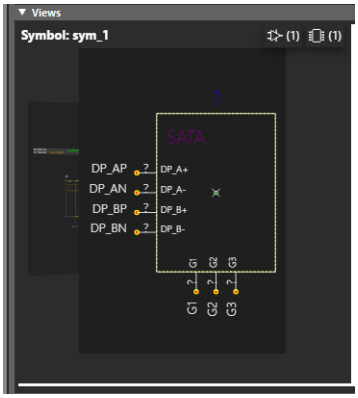
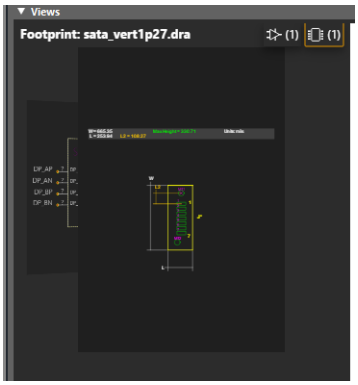
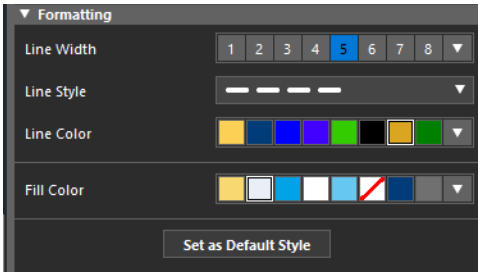
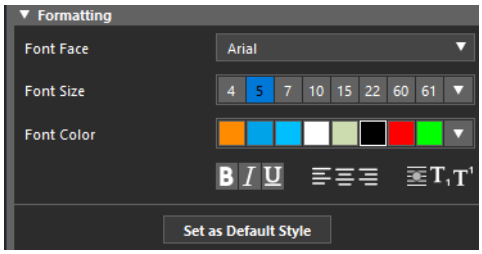
6. Check the symbol and footprint of the component in the *Views* section.





7. Change the formatting of the component or selected text.





You can set the default font and style for text and any text added after setting the default, follows the style that you specify.

Caution

System Capture does not support older, raster fonts, such as `Fixedsys`***. If you change the font size for these fonts, it will have no impact. These fonts get replaced by the system default font or the nearest matching 'Sans' font in different applications.***

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Adding Component Properties

You can add a new property, by specifying a name and a value to the property. When you select multiple components, the properties which are common to all the selected components

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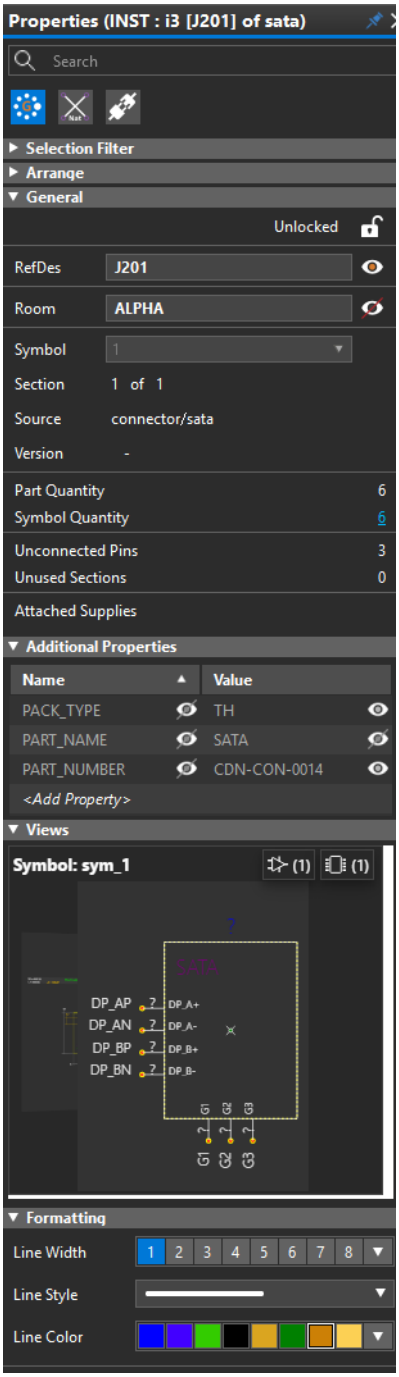
are displayed. The properties with inconsistent values are displayed with the text, `[ . . . ]`. You can compare the property values of all the selected components.



The properties on an object can be displayed on the schematic canvas. You can display the property *Name–Value* pair or the *Property Value*, or make it invisible.

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To add a property on multiple instances of a component:

1. Select the instances.

   The properties of a selected object are displayed in the *Properties* window, such as the name, value, and the visibility setting of a property. You can change the visibility setting of each property. The source of the components and number of instances of the selected component are also displayed.

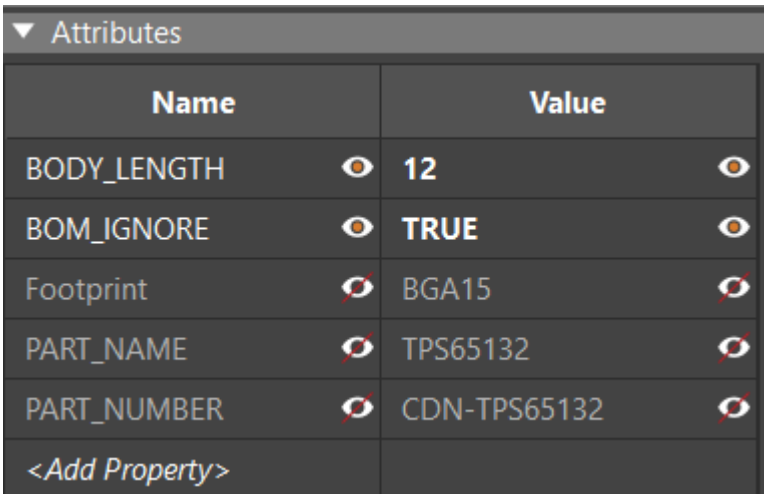
2. Open the *Properties* window to view properties of all the selected instances.

   All the properties that are common for the instances are displayed in the *Value* column. The RefDes property that is unique to each of the instances is displayed as `[...]`.

3. Click *<Add Property>* in the *Additional Properties* section to add a new property on all the selected instances.

4. Specify a property name and specify its value.

5. Press `Enter`.



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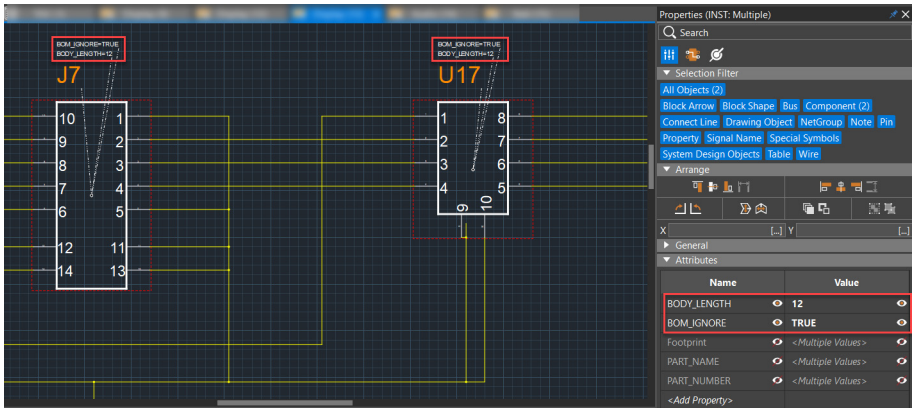
The new property is added to all the selected instances.You can view the property while viewing properties of individual instances also.



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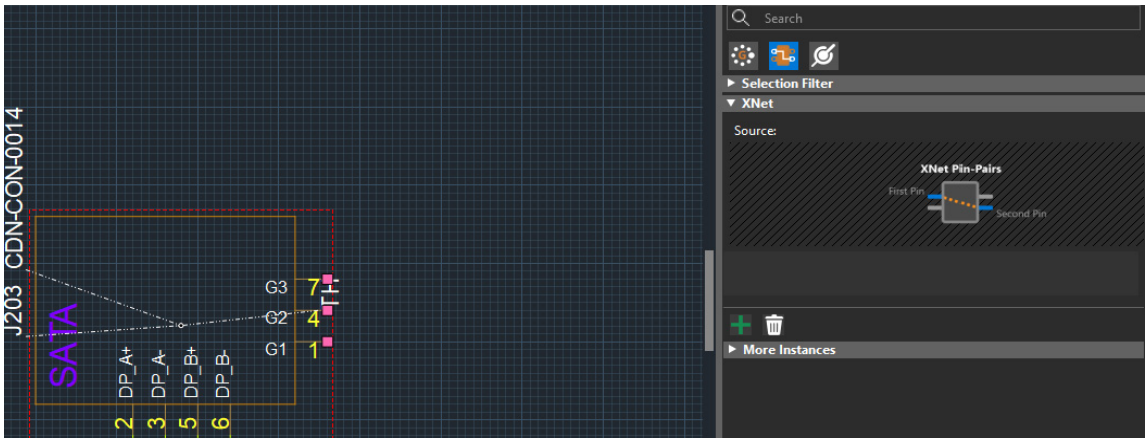
Adding XNet Pin Pairs for a Component

To create pin pairs for a net or XNet from the schematic, follow these steps:

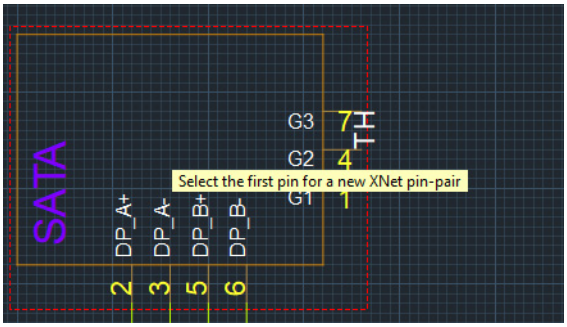
1. Select the component on the schematic.
2. Open the *XNet* tab in the *Properties* window.



A representative image is shown depicting two pins that are designated as a pin pair.

3. Click the *Create a new XNet pin-pair* icon.

   Move the cursor to the selected component. A tooltip prompts you to specify the two pins that will form an XNet pin-pair.



4. Click a pin.

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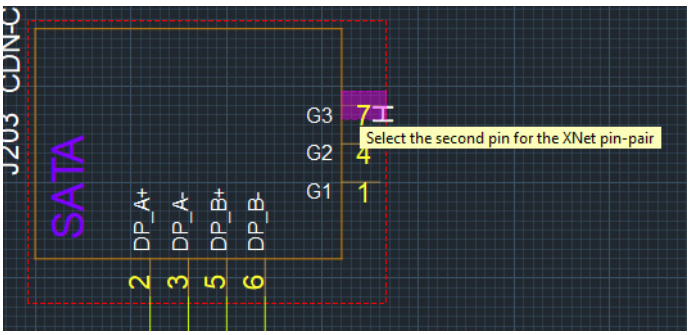
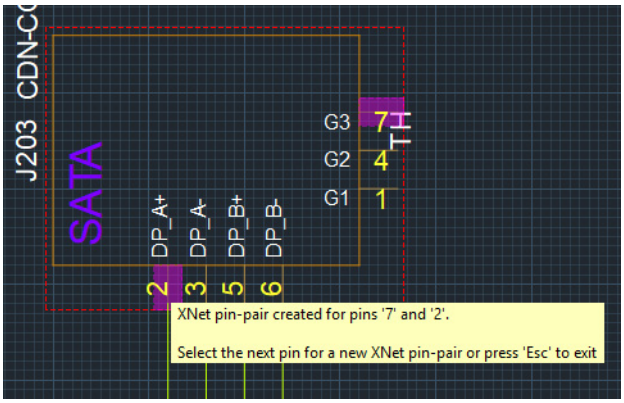
The selected pin is highlighted and the tooltip changes to prompt you to choose the second pin.

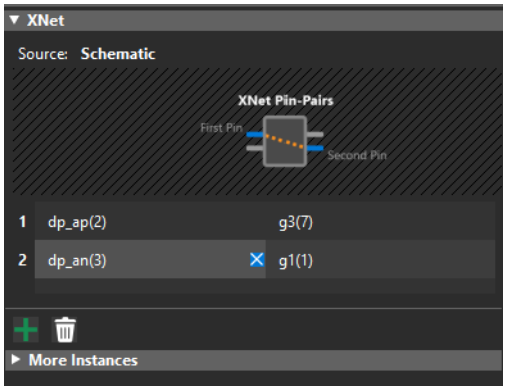


5. Click the second pin.

A confirmation message appears and now you can add more pin-pairs or exit.



The pin-pairs are also listed in the *Properties* window.



You can apply the same pin-pair definition to all the or a few of the other instances of the same component in the design.

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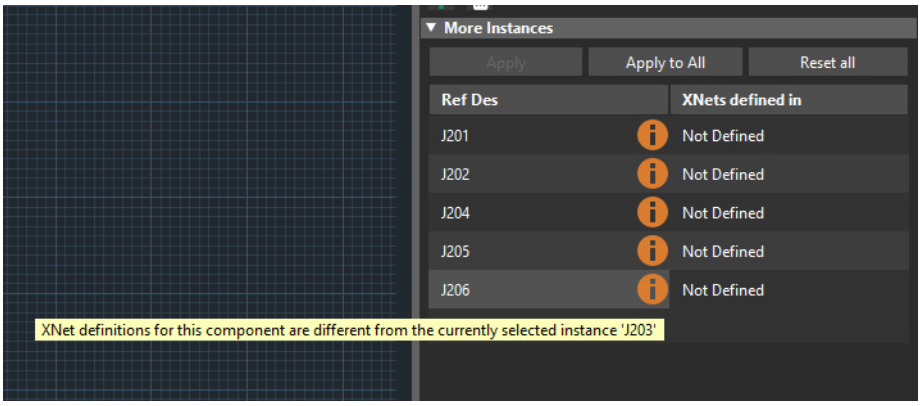
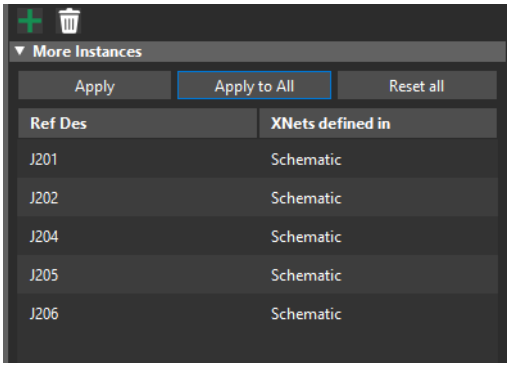
6. Expand *More Instances*.

All the other instances are listed. An icon depicts that the pin-pair definitions do not match the ones specified for the currently selected component.



7. Click *Apply to All* to apply the same pin-pair definition to all the components.



The information (i) icon gets removed and *Schematic* displays in the *XNets defined in* column.

Or

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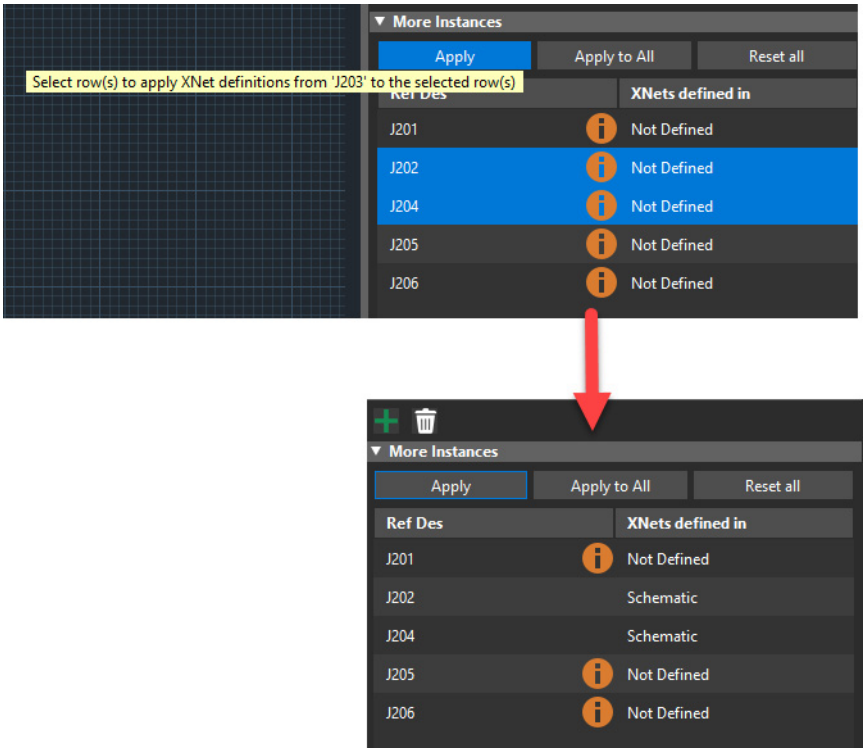
To change XNet pin-pair definitions for specific instances, select those instances and click *Apply* to change the XNet pin-pair definitions only for them.



8. Click *Reset* to discard the changes and set the XNet pin-pair definitions to the default values.

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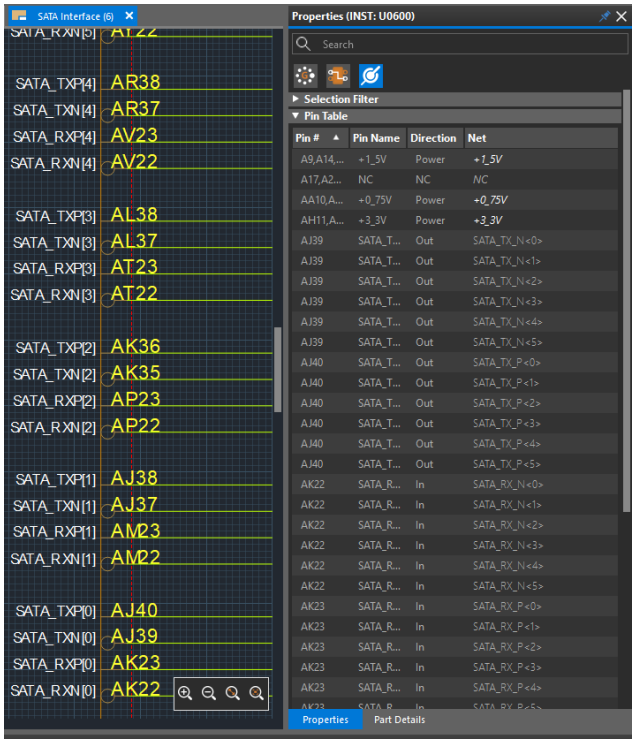
Changing Power Assignments from the Pin Table

The *Pin Table* tab of the Properties window displays the implicit power pins. You can specify or change the power assignments to those pins.

To assign power nets to power pins for a component, follow these steps:

1. Select the component on the schematic.
2. Open the *Pin Table* tab in the *Properties* window.



The pin groups, pins, pin names, directions, and connected nets are displayed.

- ❑ The non-editable nets are inactive.
- ❑ The lighter-colored nets in italics can be edited.
- ❑ The changed nets show in bold.

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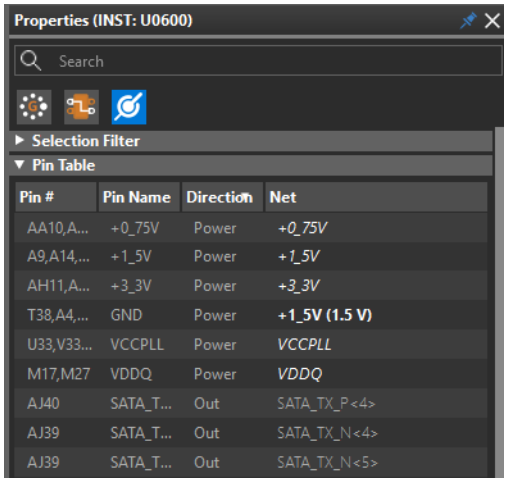
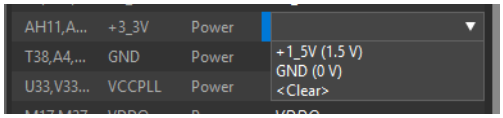
3. Sort the pins on the *Direction* column to bring the power pins to the top.



4. Click in the Net column.



5. Choose a different net to be assigned to the power pin.
6. To reset the assignment, choose *Clear* in the drop-down list.

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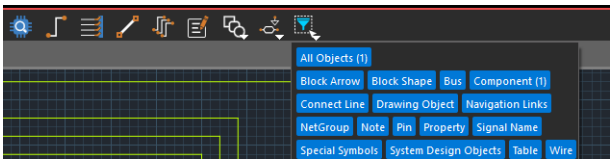
Controlling Object Selection on the Canvas

You can fine-tune a selection on the canvas to only specific types of schematic or block objects, such as signals, signal names, special symbols, components, blocks, and arrows. You can do this using the *Selection Filter* in the *Properties* panel. For example, you can choose *Component* so that only components are selected on the canvas when you mark a selected area and no signals or arrows are included in the selection.

To select only nets, perform the following steps:

1. Open the *Selection Filter* from the *Properties* panel.



2. Click options in the *Selection Filter* to deselect them. The corresponding types of objects get removed from the selection on the canvas.

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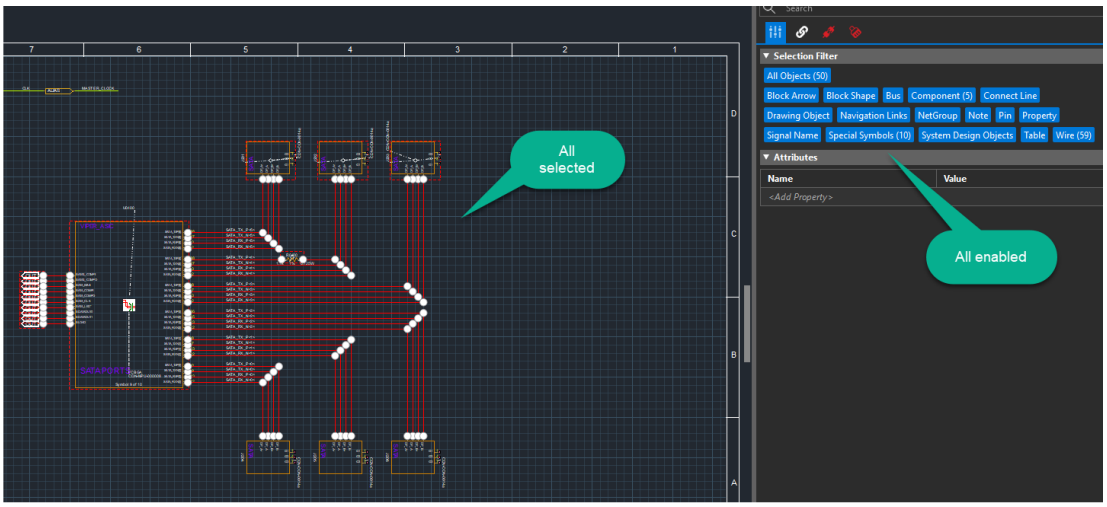
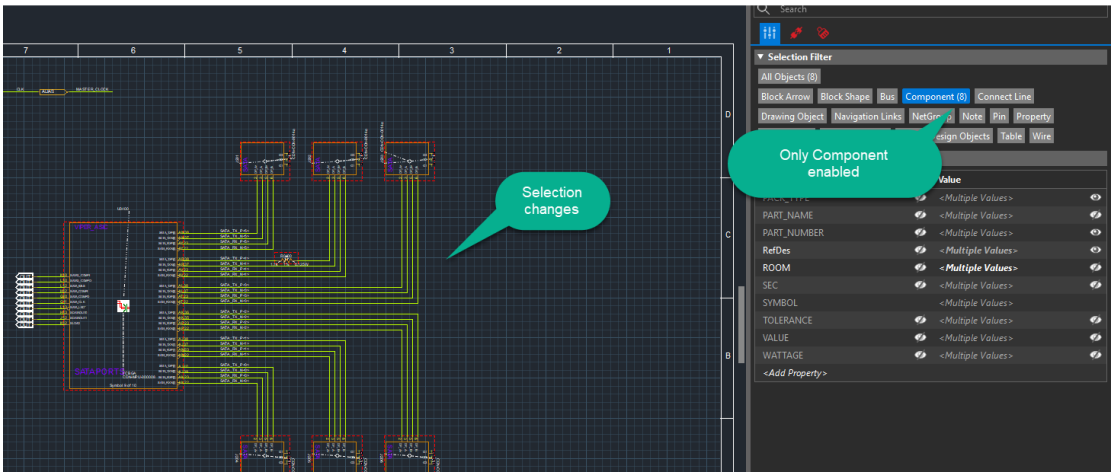
3. See the number of instances of each object type.





A red-dotted boundary appears on the selected components. Also, wires, netgroups, and buses are highlighted in red on selection.

Tip

To select objects enclosed within unfilled block shapes, click on the boundary of the shape.

Order of Selection

Selection Filter follows a hierarchy, which implies that if an object that is higher in the hierarchy is selected, objects under it are not selected. The hierarchical structure followed is:

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- Component > Component Property
- Component > Pin > Pin Property
- Component > Note linked to Component
- Wire > Signal Name
- Wire > Net Property
- Connect Line > Signal Name
- Connect Line > Net Property

For example, if you draw a selection box around all the wires, only the wires are selected and not their properties or names. Similarly, if a component is selected, the component pins, component properties, and pin properties are not selected.

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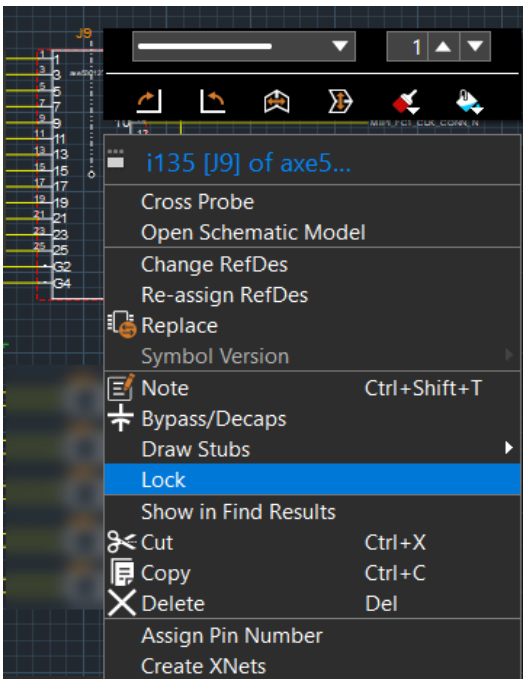
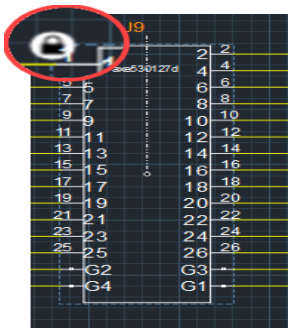
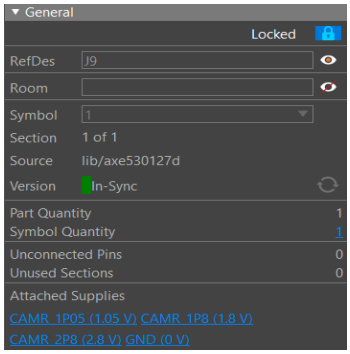
Disabling Component Modifications

For components critical to a design, you can lock their editing, formatting, and movement so that no changes are made to the components, even accidentally. To lock a component, follow these steps:

1. Right-click the component.
2. Choose *Lock*.







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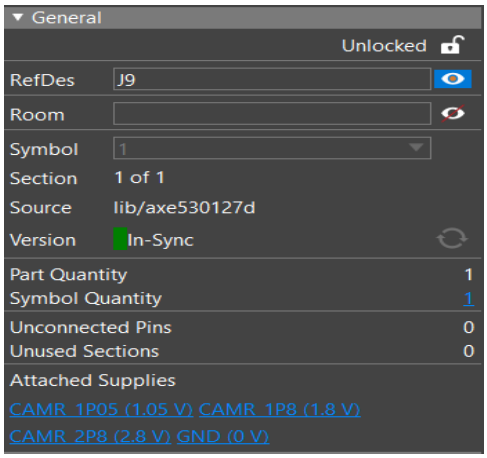
You can also lock a component from the *Properties* window.



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Connecting Components

Connectivity between components is established by drawing wires or buses between the pins of the components. System Capture provides intuitive use models for drawing wires and buses that require minimal steps. Establishing connectivity in a design comprises the following tasks:

- Drawing Wires
- Connecting Components with Wires
- Naming Wires
- Naming Multiple Nets Simultaneously
- Renaming Nets from the Property Window
- Modifying the Bus Width
- Wire Segments Selection Methods
- Ways to Align Wires
- Drawing Wire Stubs from Components
- Tapping Members from Buses
- Creating New Circuitry using Copies of Existing Nets
- Tapping out Multiple Bus bits from a Bus
- Changing Bit Numbers of Tapped Out Bus Bits

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Drawing Wires

You can draw wires or buses using the toolbar icon or by placing and moving components.

Using the Toolbar Icon

To add a wire using the toolbar:

1. Click the *Draw Wire* toolbar icon.

2. Click the canvas to start the wire.
3. Click again to create a junction and double-click to end the wire.
4. Specify a name for the wire.

Tip

Wires are drawn at 90 degrees by default. If you need to draw wires at 45 degrees, press the `Shift` key.

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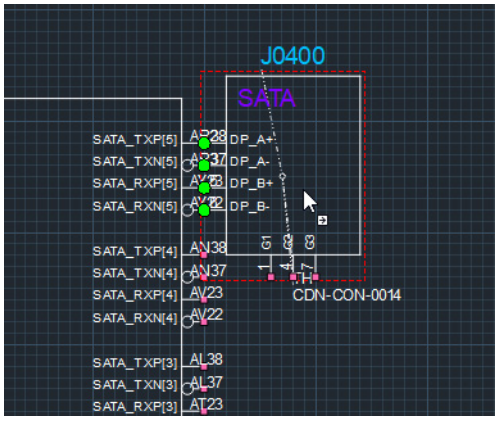
Connecting Components with Wires

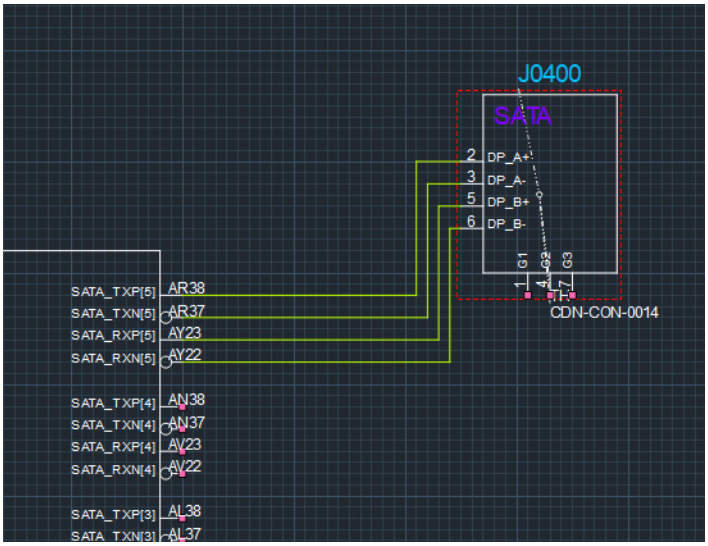
To connect the components in a design with wires:

1. Move the components in such a way that their pins overlap.

   When the pins are on top of each other, System Capture provides an indication by showing green dots at the junction points where the pins overlap. This indicates that dropping the component now will connect the overlapping pins of the component.



2. Drag one of the components away.



   Wires get drawn between the connector pins.

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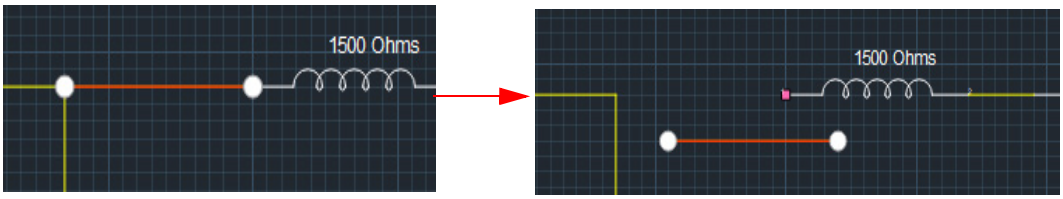
Disconnecting Wires from Component Pins

To disconnect a wire from a component pin, press `ALT` key while dragging the wire away from the pin or while resizing the wire.

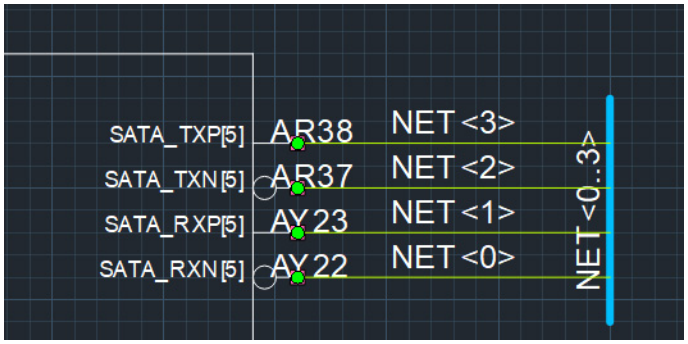
The pin-wire connection is removed and the wire is free to be connected elsewhere if required.



Alternative Methods to Draw Wires between Components

Here are some more ways to connect components using wires:

- Double-click a pin, drag the wire to another pin, and double-click the target pin, a wire is created between the two pins.
- Place a component. Add some wires on the canvas without connecting to the component. Copy the wires and move them to the pins, green connection dots appear to confirm that nets have connected to pins.
- When pasting wires or nets, visual cues help identify if the connection is complete or not. On hovering over pins, green dots mean connection is done.



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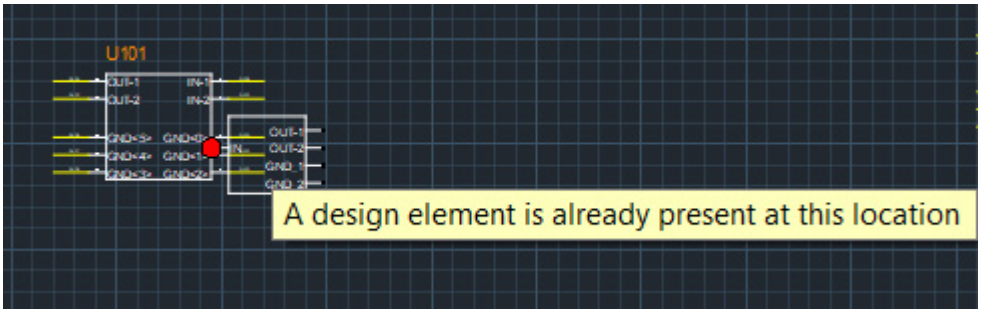
Red dots mean that no connection is possible at the current location. In such cases, a tool tip tells you the reason.



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Unsupported Characters in Net Names

The following characters are not allowed in net names:

backquote	‘
colon	:
pipe	|
comma	,
exclamation sign	!
semi-colon	;
tilde	~
square brackets	[and]
curly brackets	{ and }
back slash	\
forward slash	/
double quotes	“

Naming Wires

You have the option to name the wires in your design. In case you do not specify a name for a wire, System Capture gives it a unique, default name, called the system-defined name. You can rename the net later or continue with the default names and display them on the schematic.

To name a wire, follow these steps:

1. While you draw a wire, an edit box is displayed on the top-left corner of the canvas where you specify a name for the wire or bus.
2. Start typing the name without clicking in the edit box to get its focus.

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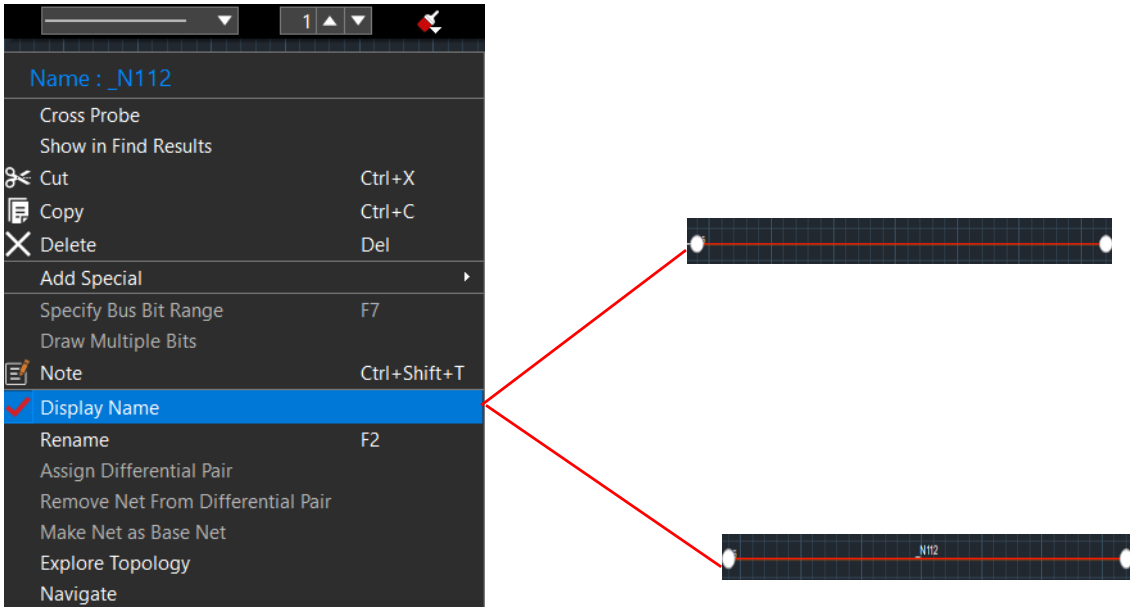
System-Defined Net Name

In case the name is not specified while drawing the wire or bus, System Capture assigns a name to it. This name starts with a prefix `_N` and has a unique number as the suffix. This name is not visible by default.



To make the net name visible, follow these steps:

1. Right-click the net.
2. Select *Display Name*.

Important

The *Voltage* property cannot be added to nets that do not have a name explicitly provided.

Related Topics

Naming Multiple Nets Simultaneously

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Renaming System-Defined Net Names

To change a system-assigned name, edit the net name by using one of these ways:

1. Right-click the net and choose *Rename*.
2. Double-click the net on the canvas.

Displaying System-Defined Net Names

When a new net is drawn, the system assigns a net name for it. By default, the system assigned net name is not displayed.

To display the system-assigned net names:

1. Choose *Edit – Preferences*.

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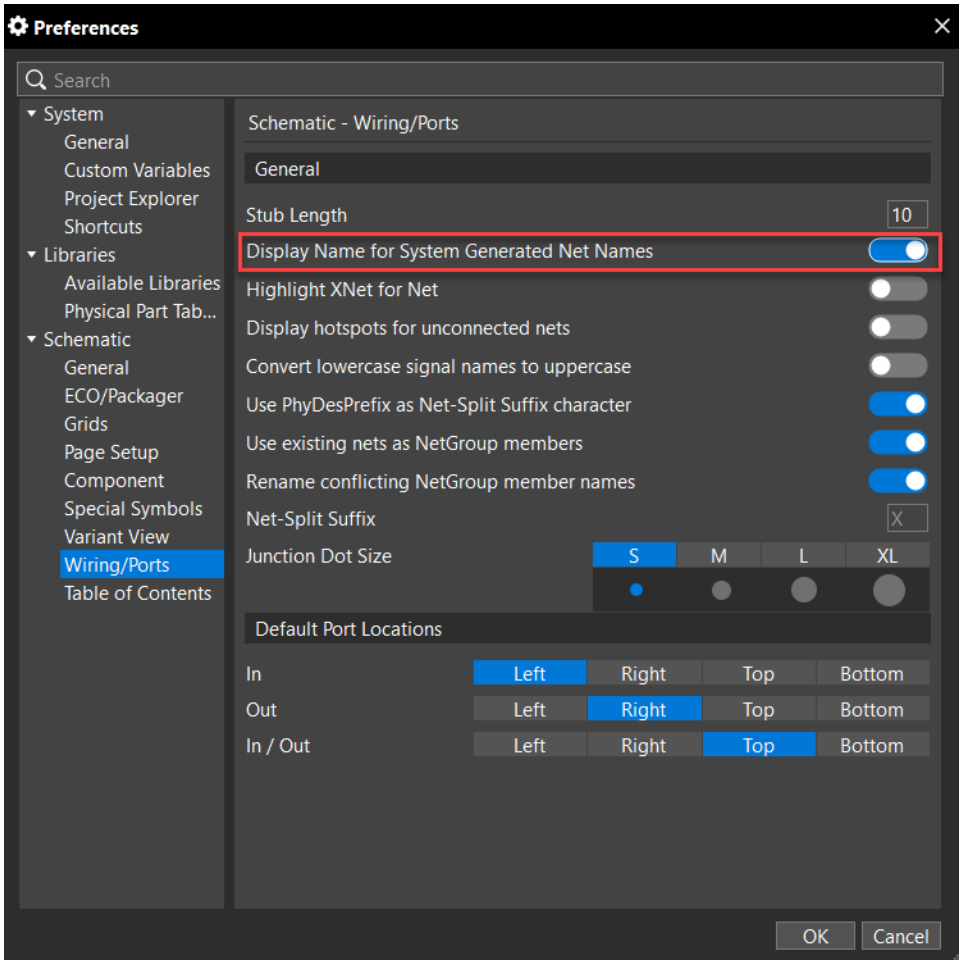
2. Open the *Schematic – Wiring/Ports* tab.



3. Enable *Display Name for System Generated Net Names* in the *General* section.

You can also name a net in any of these ways:

- Specify the net name on the canvas
- Specify the net name in the *Properties* window
- Select multiple nets and renaming them using the *Net Rename* dialog box
- Assign an existing net name to a segment

Displaying User-Defined Net Names

To display user-defined net name, follow these steps:

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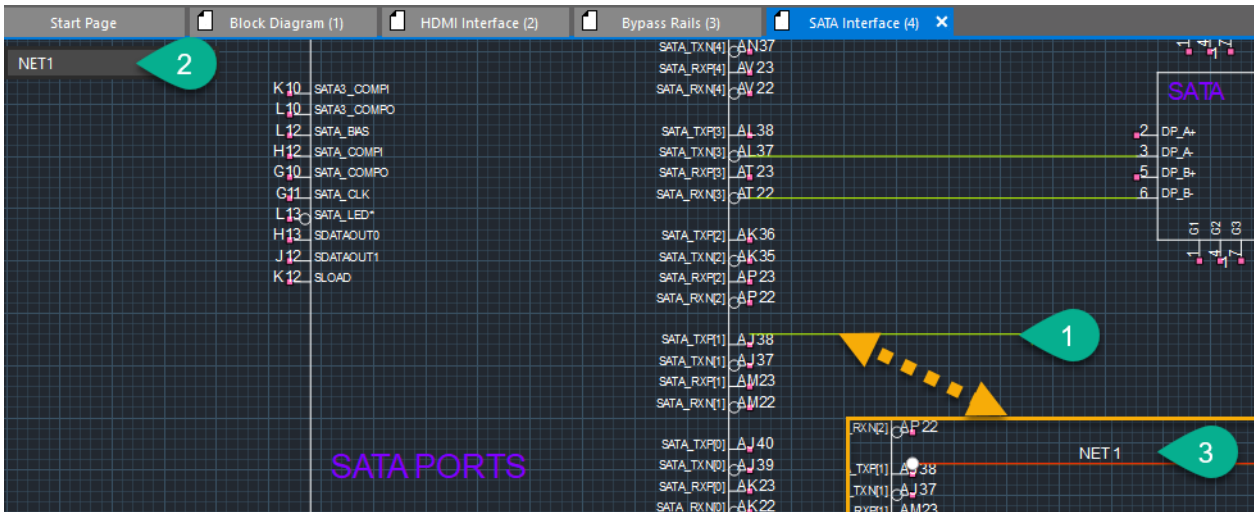
1. Start drawing a wire.
2. Name a wire while it is being drawn.

   Name specified on the wire becomes visible on the top-left of the canvas.
3. Double-click to end the wire.

   The user-defined wire name will be displayed.



Related Topics

Renaming Nets from the Property Window

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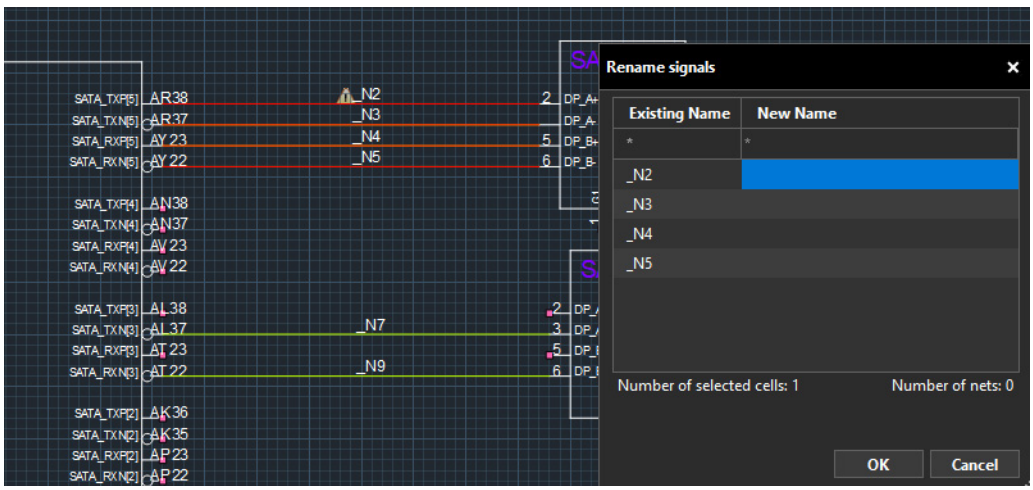
Naming Multiple Nets Simultaneously

To save time and effort, you can assign names to multiple nets in one go. To do this, follow these steps:

1. Select the nets that need to be renamed.
2. Press `F2` or right-click and choose *Rename.*

   The *Rename signals* dialog opens where the existing signal name is displayed.
3. Click a cell to specify the net name.

   A marker is displayed on the wire or the bus being named. You can also select multiple cells and rename them using data from an external source, such as a text file or spreadsheet.



Related Topics

- Naming Wires
- Renaming System-Defined Net Names

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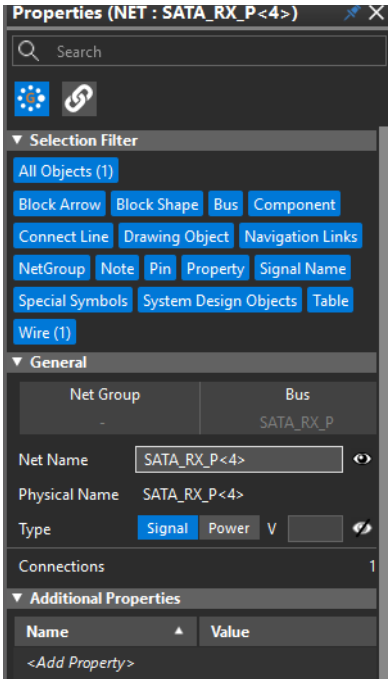
Renaming Nets from the Property Window

You can also rename a net in the *Property* window. To do this, follow these steps:

1. Open the *Properties* window.
2. Select a net.

   The properties of the net including its *Name* are displayed.
3. Modify the *Name* property to rename the selected net.



A drop-down list containing all the net names in the design is displayed and you can select a name from the list as the new net name. As you type in the letters for the name, the list gets filtered and you start seeing a smaller list of nets which match the pattern you enter. This ensures that the correct net names are specified for the nets.

Caution

When you rename a stub or a net that has constraints, the constraints are deleted when the net name changes. This is because System Capture internally treats it as a deletion and a new net addition.

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Related Topics

- Renaming System-Defined Net Names
- Naming Multiple Nets Simultaneously
- Naming Wires

Modifying the Bus Width

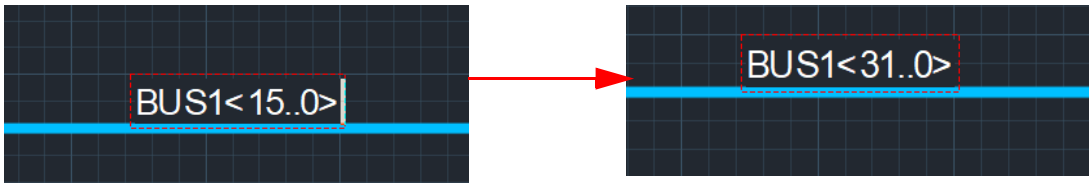
As you work with a design, you often need to increase or decrease the width of existing buses in the design.

Increasing the Bus Width

To increase the bus width, rename it and in the new name increase the bus bits. For example: *BUS1<15..0>* to *BUS1<31..0>*

1. Select the net whose width needs to be increased.
2. Press `F2`.
3. Type the new bus width

The bus bits increase.



Decreasing the Bus Width

To decrease the bus width:

1. Select the net whose width needs to be decreased.
2. Press `F2`.
3. Type the new bus width

   For example, *BUS2<31..0>* to *BUS2<15..0>*

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Related Topics

Changing Bit Numbers of Tapped Out Bus Bits

Wire Segments Selection Methods

A signal on a page can exist as a single wire segment, a set of connected wire segments, or disjoint wire segments connected to different components on the page. System Capture supports the following three different wire selection options to select the wire on a page.

- Clicking a wire selects the current wire segment only.
- Double-clicking a wire selects all the connected wire segments of the wire.
- Pressing the Ctrl key and then double-clicking a wire selects all the connected as well as disjoint wire segments on the page for that signal.

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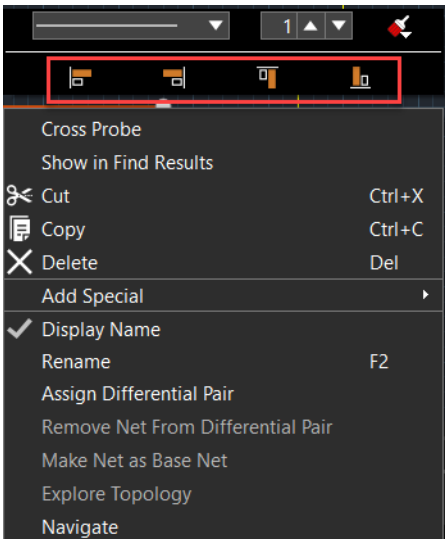
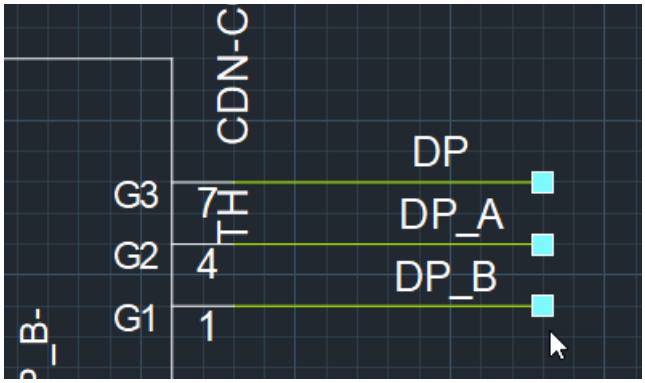
Ways to Align Wires

In System Capture, you can select wire stubs of different lengths and quickly align them to make them equal. The wires stubs of different lengths can be selected and aligned using any of the alignment commands – *Align Left*, *Align Right*, *Align Top*, or *Align Bottom*.



Based on the alignment command used, the wire segments are resized in that direction to align the edges of the wires.



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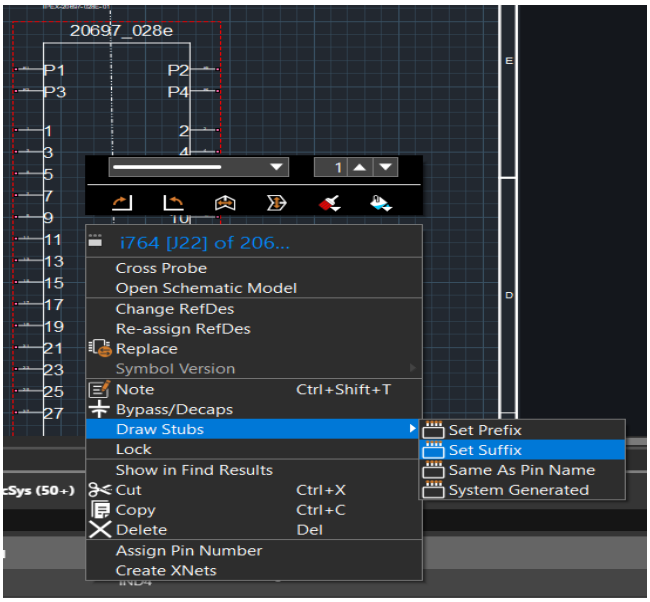
Drawing Wire Stubs from Components

System Capture provides an efficient method of drawing wires on all unconnected pins of a component. To do this, follow these steps:

1. Select a component.
2. Right-click and choose *Draw Stubs*.
3. Specify the naming convention. These can be:
   - ❑ Prefix
   - ❑ Suffix
   - ❑ Keep the names same the pin names
   - ❑ Use system-generated names



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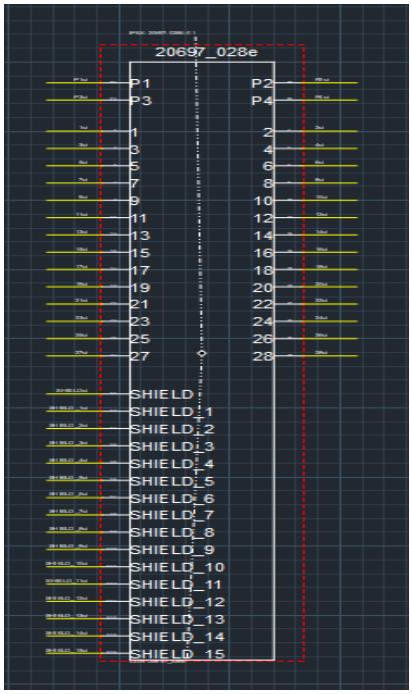
Stubs are drawn from all the pins of the component



These stubs are wires that can be quickly connected to other pins. When the components are connected and moved, the wires between the components are redrawn to ensure that there is no break in connectivity. When the components are moved, the wiring gets adjusted to display connectivity between components.

As with components, System Capture packages the nets as soon as they are added and automatically assigns Physical Net Names to the nets.

Related Topics

Tapping Members from Buses

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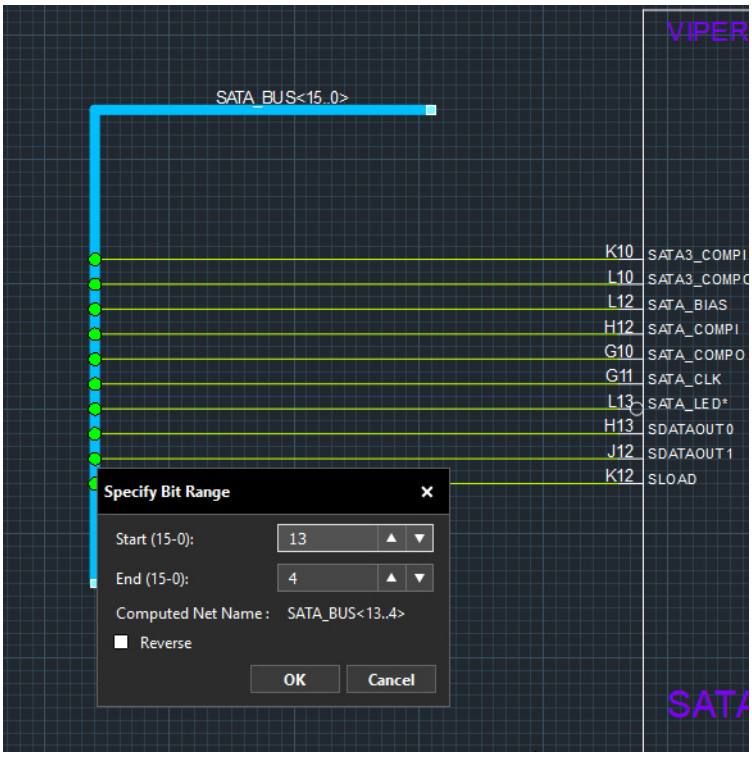
Connecting Multiple Pins to Wires Tapped from a Bus

System Capture provides a quick way to connect multiple pins to wires tapped from a bus.

To connect a bus to multiple pins:

1. Draw wire stubs on selected pins or all the pins of the component.
2. Select all the wire stubs and drag and drop them on the bus.

   The *Specify Bit Range* dialog opens and it automatically picks a suitable bus bit range.
3. Change the bit range if needed.



4. Click *OK*.

   The signals are named according to the name of the bus and the bit range specified. Tap bodies are placed for each tapped bits and the tapped bit number is displayed on the tap

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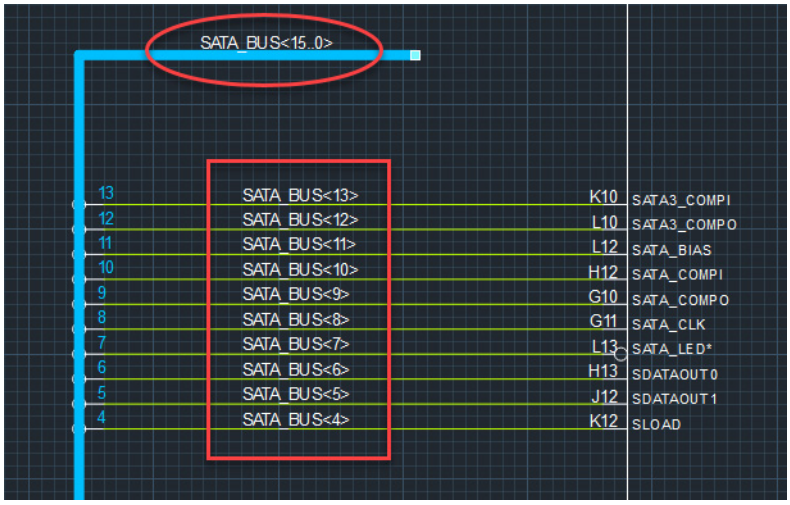
body. The visibility of the bus bit numbers can be controlled by right-clicking the bus and choosing *Display Bus Number(s)*.



Note: In case a named net is tapped out from the bus, the named net is aliased to the bus bit from which it was tapped.

Related Topics

- Tapping out Multiple Bus bits from a Bus
- Changing Bit Numbers of Tapped Out Bus Bits

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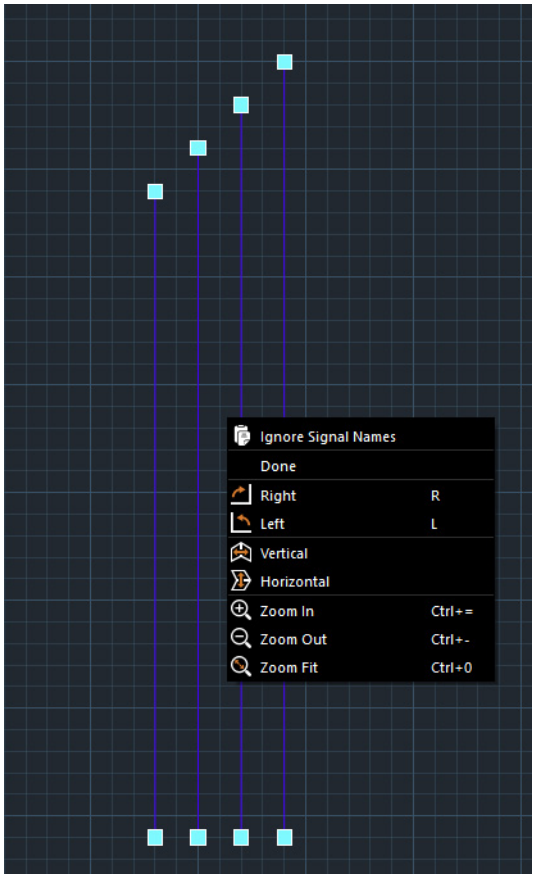
Creating New Circuitry using Copies of Existing Nets

When you copy and paste nets or wires, System Capture treats them as additional instances of the same nets. You can copy and paste wires without bringing their existing names to the newly made copies. These copies are given new system-generated names and are no longer associated with their source.

To create new circuitry:

1. Select the nets.
2. Right-click and choose *Copy.*
3. Move the cursor to another location.
4. Right-click and choose *Paste.*

   A copy of all the selected wires get attached to the cursor.
5. Right-click and choose *Ignore Signals* to make copies with new system-defined names.



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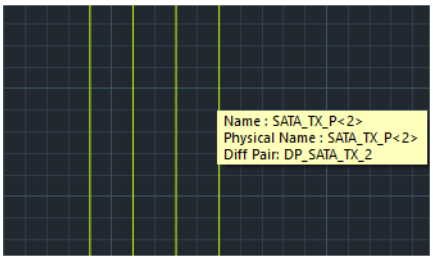
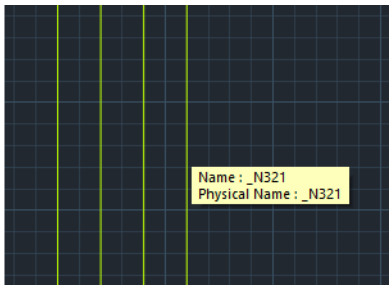
These copies will no longer have the name of the nets that were copied, as the following figure shows.



Right-click - Paste



Right-click - Paste - Ignore Names

Related Topics

Reassigning Reference Designators

Tapping Members from Buses

Some additional features, such as tapping members of the bus, are available for buses.

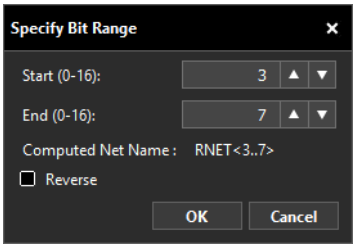
Important

You can only tap members of a bus that is named. This ensures that the bus and its width is correctly defined and when the members are tapped, the tapped wire is correctly named. The steps for drawing and naming wires and buses are similar.

To tap a member from the bus:

1. Click the bus where the bus bits will be tapped out.
2. Right-click and choose *Specify Bit Range*.

   The *Specify Bit Range* dialog box opens.



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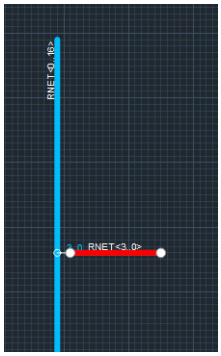
3. Specify the bits to tap out.
4. Click *OK*.

   The wire is tapped out from the bus and attached to the cursor for final placement.



Related Topics

Connecting Multiple Pins to Wires Tapped from a Bus

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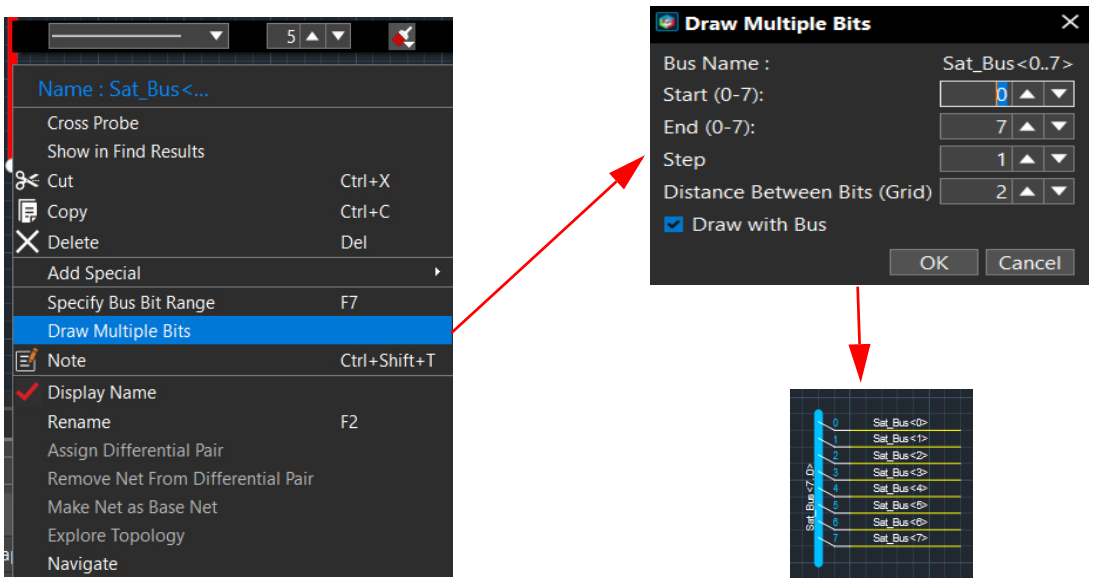
Tapping out Multiple Bus bits from a Bus

System Capture provides you the option of tapping out multiple bits from a bus.

1. Right-click a bus and choose *Draw Multiple Bits*.

   The *Draw Multiple Bits* dialog box opens.



2. Specify the following:

   - ❑ Bit number from where to start
   - ❑ Bit number to end
   - ❑ Step size

     The step size allows you to skip some bits in between. For example, tap out only even bit numbers or odd bit numbers. This command draws wire stubs with the name of the tapped out bus bit assigned to each of the wire stubs.

   - ❑ Distance between bits

     The wire stubs are spaced based on the distance in grid units as specified in the dialog box.

     If the Electrical Grid is set to ½ of the pin-to-pin spacing in your project, use 2 grids as the distance between the wire stubs.

   - ❑ Draw with Bus

     The bits are drawn with the bus.

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The wire stubs are attached to the cursor and you can place them on any side of the bus. The bus tap symbols are automatically attached to the wire stubs and the multiple bus bits are tapped out.

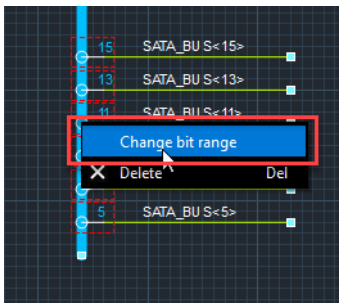
Related Topics

Tapping Members from Buses

Changing Bit Numbers of Tapped Out Bus Bits

You can change the tapped bus bit numbers for multiple bus taps in a single operation. Changing the bus bit numbers as per your requirement makes the schematic cleaner and reduces duplicacy.

1. Right-click the tapped bus bits to be modified and choose *Change bit range*.



The *Change bit number* dialog box opens. The signal names along with currently tapped out bus bit number are displayed.

2. Specify a new bit number.

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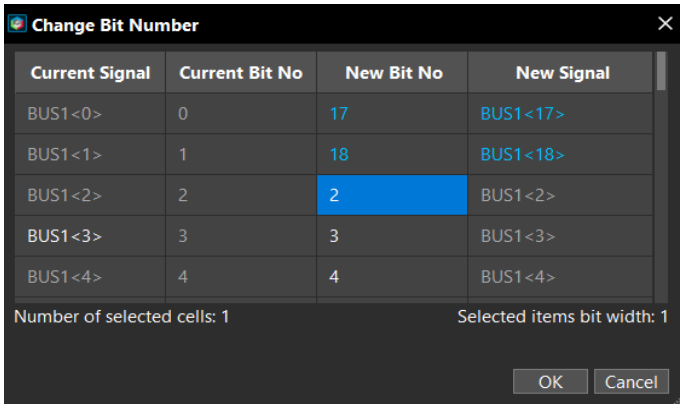
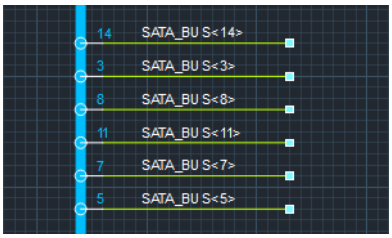
The new signal name is automatically computed. The modified bit number and the modified signal name are shown in blue to indicate that they have changed information.



3. Click *OK*.

The tapped out bus bits get updated and you see the new bit numbers being displayed on the tap symbols. The tapped out bus bit names are also updated on each of the bits. Unchanged bus bits continue to show the existing values.



When renaming the bus or tapped bus-bits, remember the following.

- You can rename any of the bus taps to have a different name from the parent bus.
- When you rename the bus, all the tapped out bus bits get renamed.

Important

If any of the tapped out bits have a different name, you cannot rename the bus using Rename. You need to use the *Find and Replace* command.

Related Topics

- Tapping out Multiple Bus bits from a Bus
- Tapping Members from Buses

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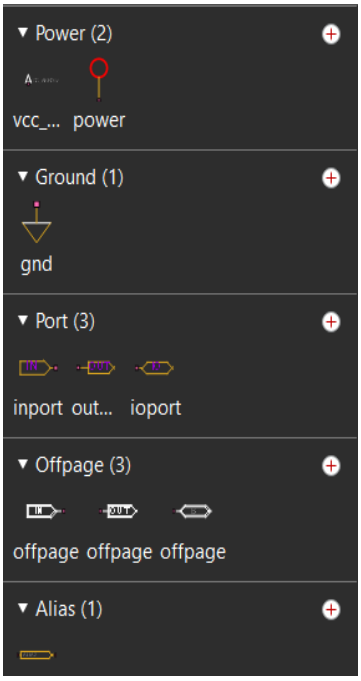
Alias body and Synonym Body

Nets in a design get aliased when they are connected across levels of hierarchy or while tapping them out of a Bus object. You can also alias nets selectively using the *Alias* body or the *Synonym* body. You can add the Alias body or the Synonym body from the Special Symbols Alias section. Place the Alias body on the canvas and use it to alias the nets.



Two nets can be aliased by placing the Alias body or Synonym body between them. When the *Physical Net Name* of the nets are displayed, both the nets show the same Physical Net Name.

Related Topics

Show Winning Nets with Overlays

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Aliasing Nets

Any number of nets can be aliased by placing the Alias body or the Synonym body between the nets. The winning base net name is decided using the lexicographical order of naming. If required, you can also select a different net name as the winning net name.

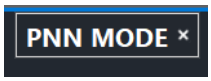
To alias two or more nets:

1. Draw three wires on the schematic canvas and give them different names. As an example, *CLOCK*, *RESET,* and *MASTER*, respectively.
2. Open the Special Symbols bucket and from the Alias section, select the Alias body and place it between the nets *CLOCK* and *RESET*.
3. Place another Alias body between the nets *RESET* and *MASTER*.
4. Extend the nets to join them as illustrated in the following image:

   The three nets are now aliased.

5. To view the Physical Net Names of these nets, choose *View – Physical Net Names*.

   The Physical Net Names of the nets are now displayed. Also, at the top-right corner of the canvas, the following information is displayed indicating that the PNN Mode is on:



   All the three nets have the same Physical Net Name, CLOCK, which is the winning base net name in this case, as lexicographically it is the first of the three nets.

6. Choose *View – Physical Net Names* to hide the Physical Net Names.

   You can also turn it off by clicking on the cross on the PNN Mode notification.

   You can select a different net as the winning base net.

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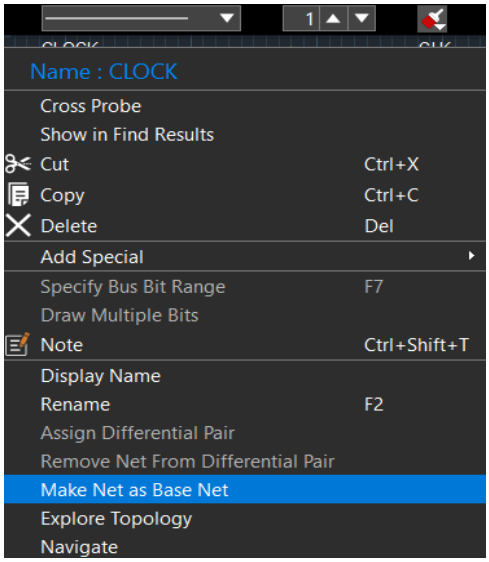
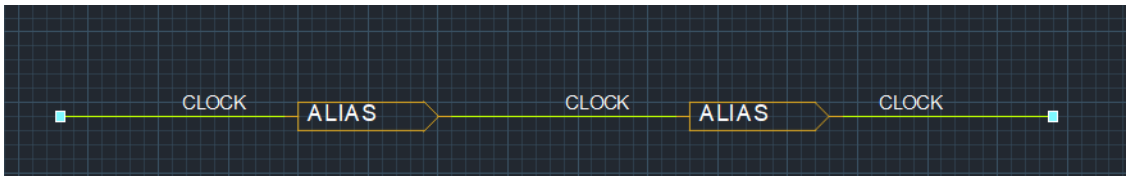
7. Right-click the net *CLOCK* and choose *Make Net As Base Net*.



8. Choose *View – Physical Net Names* to view the new Physical Net Names assigned to the nets.



9. Hide the Physical Net Names.

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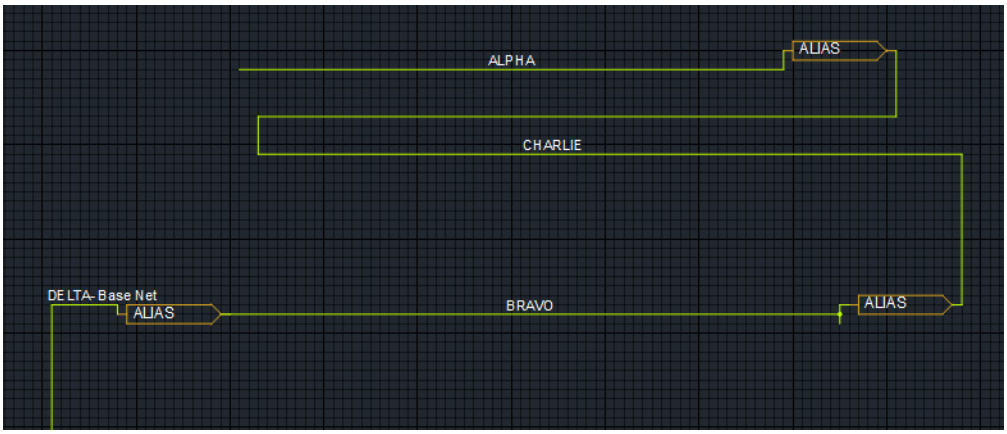
Show Winning Nets with Overlays

When multiple nets are aliased, the winning net name is used as the physical name. You can configure System Capture to show the winning or base net on the canvas. For example, in the following image, the net `DELTA` is the base net. The suffix you see next to the net name is called a text overlay and can be customized.



To configure this behavior, set the following directives in the `CANVAS` section of the `site` or *`project`* cpm file:

Directive	Value	Description
`BASE_NET_OVERLAY`	`ON`	Enables the feature
`EXPLICIT_BASE_NET_IDENTIFIER`	*`<text>`*	The text to be shown as the suffix for the base net. In the example, this is set to `' - Base Net'`

Related Topics

Allegro Front-End CPM Directive Reference Guide

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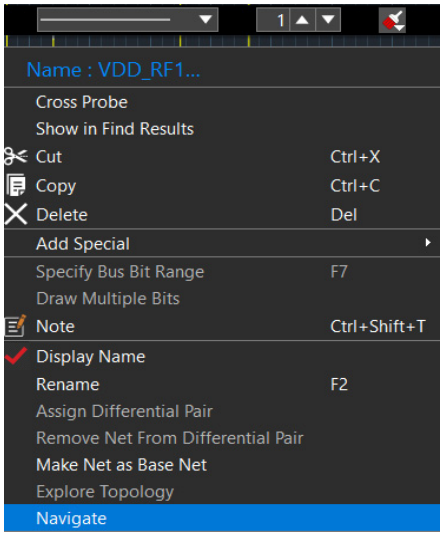
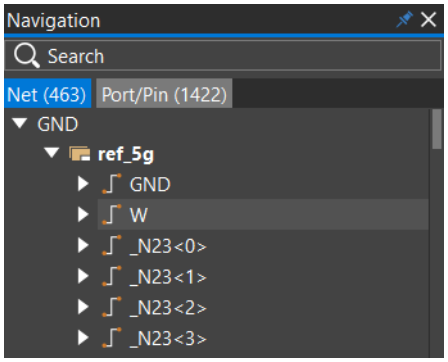
Navigation of a Signal in the Design

Signal navigation provides a quick way to navigate all the occurrences of a net throughout the project hierarchy.

System Capture provides a quick and robust way to navigate to the designs for nets and components in a design from the *Navigation* tab in the *Project Explorer* window can be used for this. To do this, follow these steps:

1. Select a wire segment on the schematic canvas
2. Right-click and choose *Navigate.*





The *Navigation* tab opens.This tab is populated with the list of all the locations in the design where this net exists. Each row in the Navigation tab is a hyperlink.

3. Click a row.

   The corresponding page opens, zooms and highlights the net.

4. Clicking a different net on the canvas.

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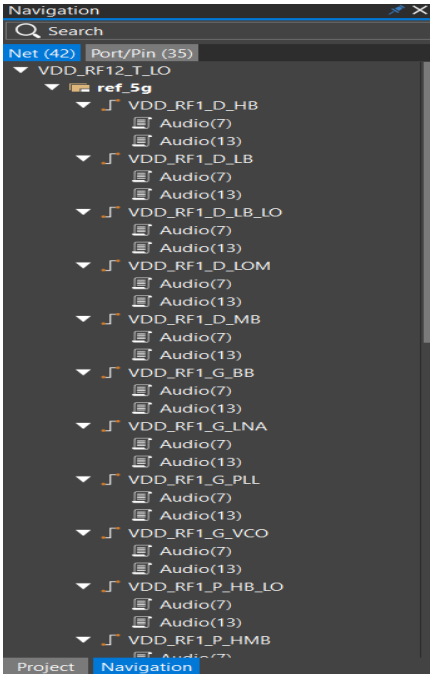
The Navigation tab is updated with the information corresponding to that net.



Related Topics

- Using the Find and Modify Command
- Adding Bypass Capacitor Rails

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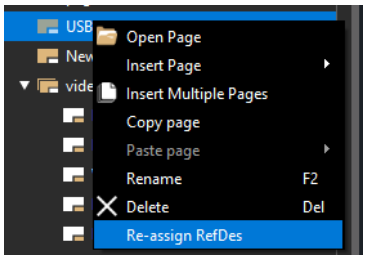
Reassigning Reference Designators

When reusing a schematic sheet from another design, you can preserve the source packaging of the schematic sheet. This implies that the packaging information inherited from the source design is retained in the destination design. At any stage, if you want the packaging of the page to follow the same RefDes pattern as defined in the current design, you can repackage the instances on the schematic sheet. Repackaging reassigns the RefDes on the schematic sheet based on the defined RefDes pattern.

To repackage component instances on a schematic sheet:

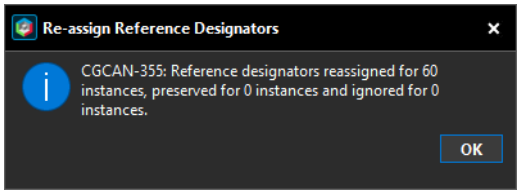
1. Open the *Project Explorer* and select the schematic sheet.
2. Right-click and choose the *Re-assign RefDes* command.



3. Click *Yes* in the message box.

   The packaging information of the schematic sheet is updated and a summary dialog box is displayed providing the information about the changes done.

4. Click *OK* to close the dialog.



Related Topics

Changing Reference Designators from Search Results

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Adding Bypass Capacitor Rails

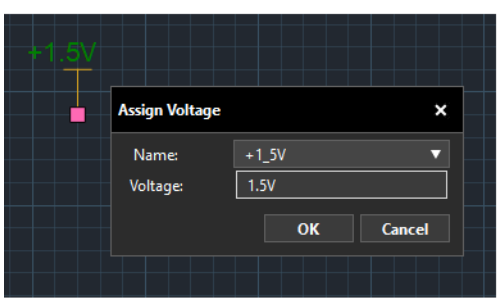
Bypass Capacitors are required in a design to maintain its Power Integrity (PI). These capacitors are connected between the Power and Ground pins of a device to address the power requirements of the device. The number of capacitors placed is usually determined by the information in the data sheet or by the rule of thumb developed over time.

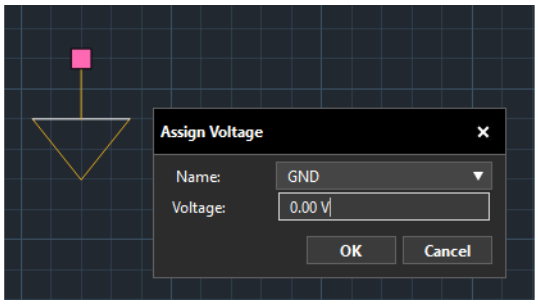
You can define the requirements for a bypass capacitor rail and generate a rail to be placed on the schematic sheet. The generated rail can be resized to fit the available space on the schematic sheet.

To add a bypass capacitor rail:

1. Add power symbols to the design and specify voltage as `1.5 V` and `GND`.
2. Add a ground symbol and specify voltage as `0V`.

   Adding these ensures that power nets are available for connections to Bypass Capacitors.





3. Right-click on the canvas and choose *Bypass/Decaps*.

   The *Add Bypass Capacitors* dialog box opens.
4. Click the button next to *Select Capacitor*.

   The *Add Capacitor for Bypass* dialog box opens.
5. Specify the search criteria, for example, `10uF`.
6. Double-click the row to select the component.

   The part is selected in the *Add Bypass Capacitors* dialog box.
7. Select the pin connections.
8. Assign net names to the pins, for example:
   - Pin B – `GND`

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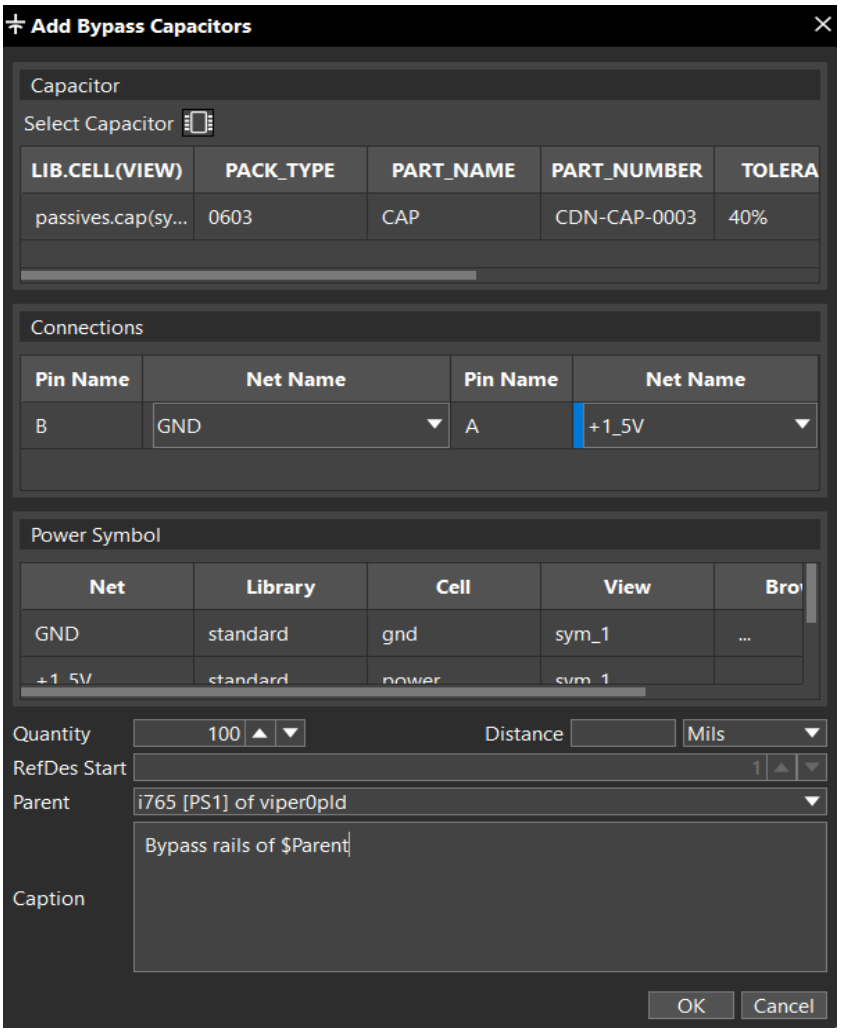
- Pin A – `1.5V`

9. Specify the values for Quantity and Caption, for example:

- Quantity – `100`
- Caption – `Bypass rails of $Parent`



As the `REF_DES_PATTERN CPM` directive is already defined, the *RefDes Start* field is disabled in this dialog. The capacitors in the rail will be assigned RefDes based on the `REF_DES_PATTERN`.

10. Click *OK*.

The rail is attached to the cursor for placement.

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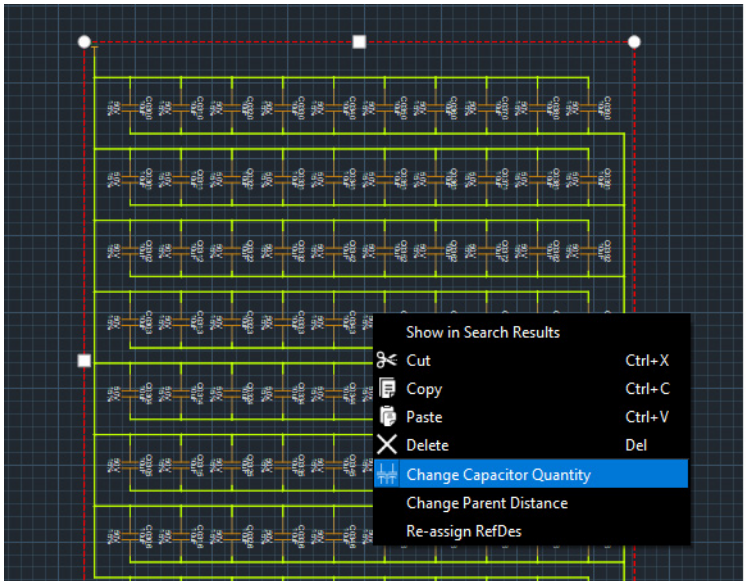
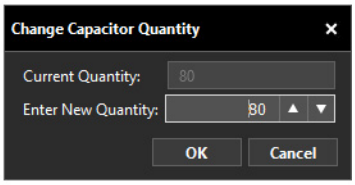
11. Place the rail of bypass capacitors on a page.

12. Right-click the bypass rail and choose *Change Capacitor Quantity*.

The *Change Capacitor Quantity* dialog opens.





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The current quantity of capacitors is displayed which you can change.

13. Specify the new quantity value and click *OK*.

The bypass rail is updated with the new count of capacitors.

You can resize the rail to create room for more components. The number of capacitors in the bypass rails can be modified at a later stage also. The number of capacitors can be increased or decreased, and the bypass rail is modified to match the new number of capacitors.

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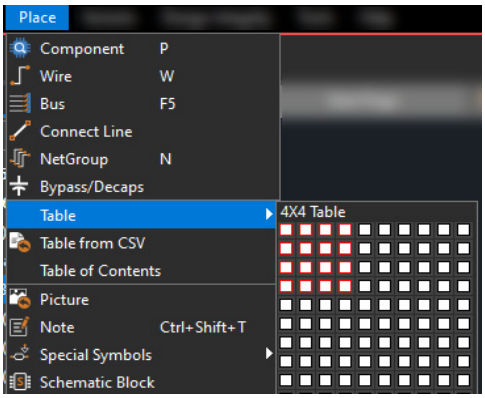
Adding Tables to the Design

You can add tables on schematic pages for documentation purposes, such as displaying pin numbers for buses or vector pins, displaying pin numbers of implicit power pins, and so on.

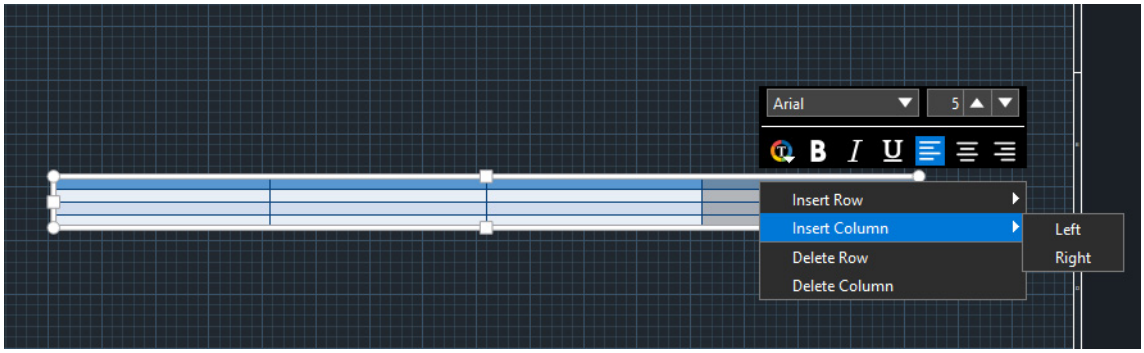
To add a table, follow these steps:

1. Choose *Place – Table*.
2. Specify the number of rows and columns.



A table image is attached to the cursor.

3. Click the canvas to place the table.
4. Add or remove rows and columns as required.



5. The height of each row and the width of each column of the table is adjustable.

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Importing a CSV file as a Table

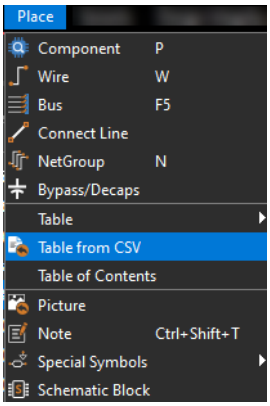
You can add a table using a Comma Separated Values (CSV) file.

Caution

.csv files with Byte Order Marker (BOM) characters in the beginning cannot be imported. In case you have trouble importing data from a .csv file, open it in a text editor and ensure the BOM character is not there.

To import a CSV file, follow these steps:

1. Choose *Place – Table from CSV*.



2. Choose a CSV file.

   The CSV can have a maximum of 20 rows and 20 columns. If the file has more rows or columns than this, it cannot be imported and System Capture reports an error.

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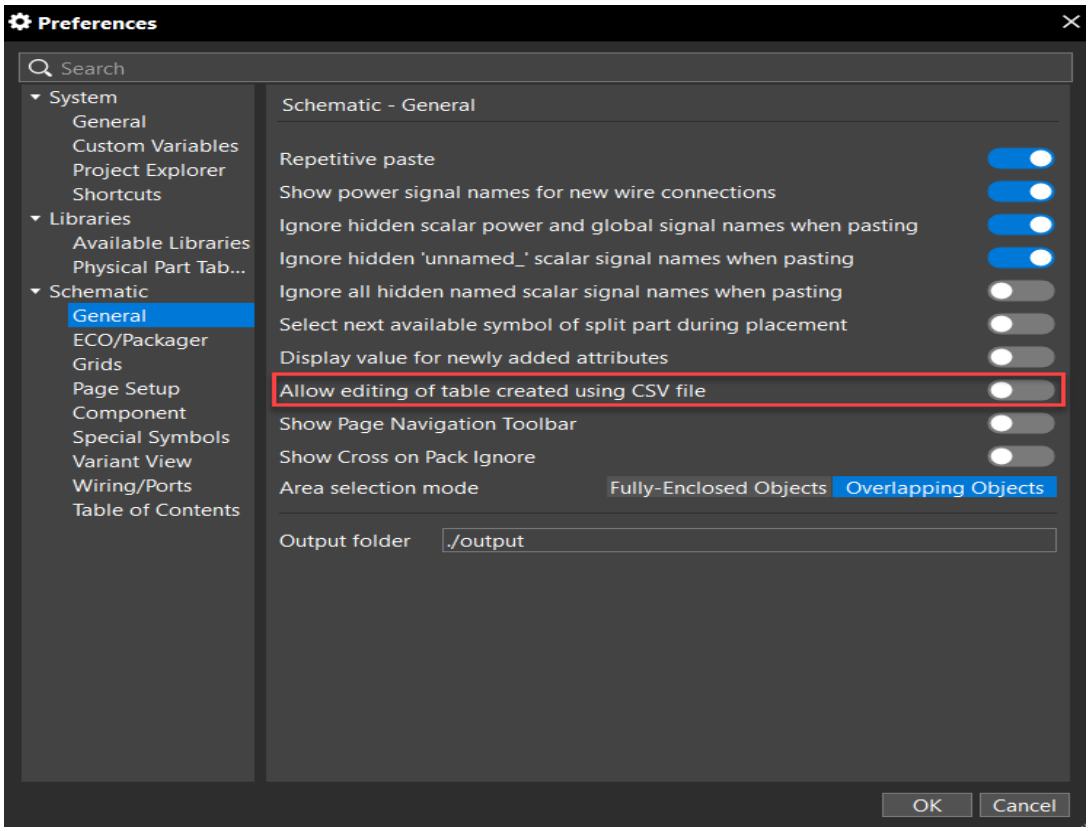
3. Control the editing of the imported table by setting the following option.



Related Topic

Adding Tables to the Design

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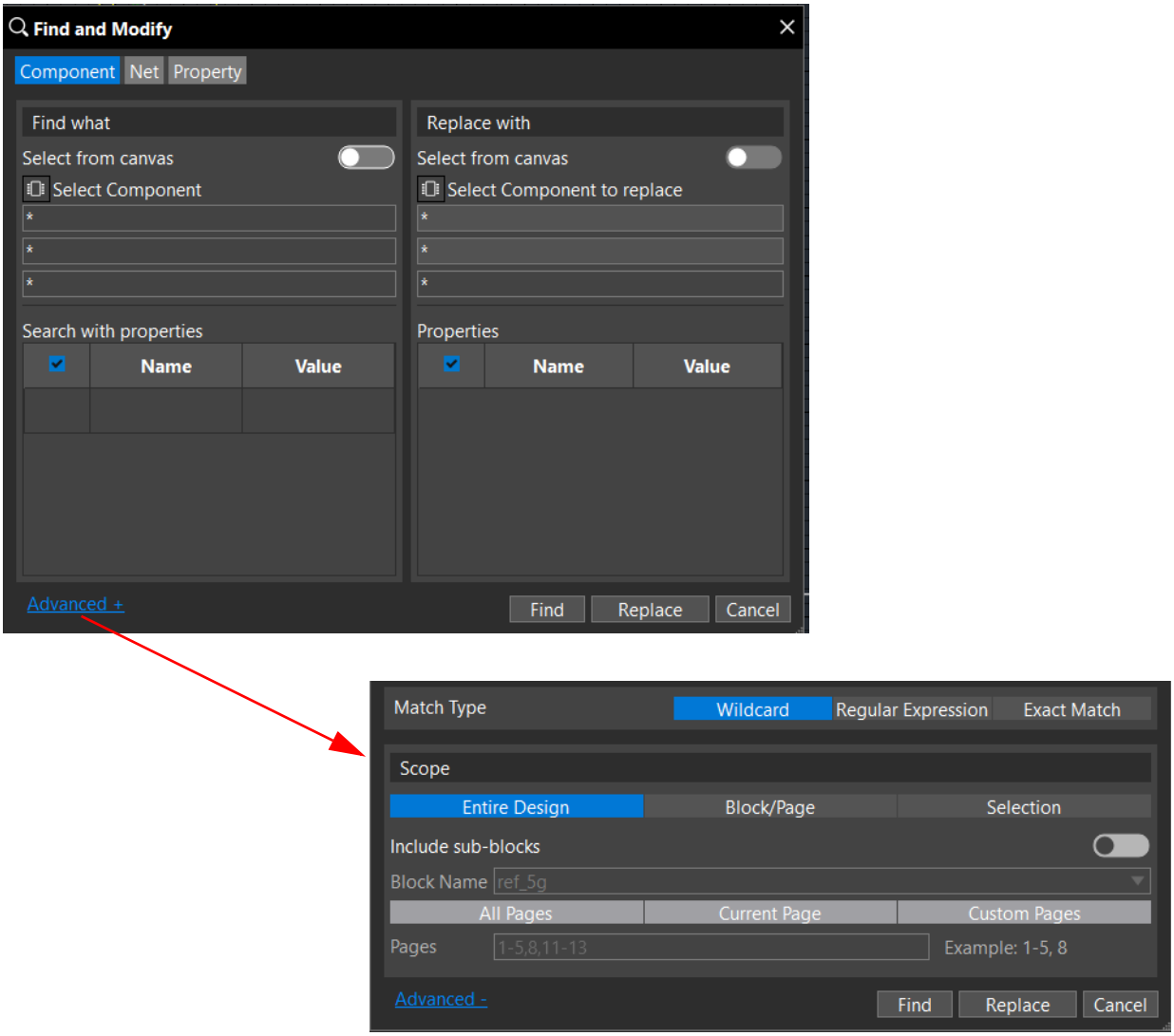
Using the Find and Modify Command

In addition to quickly locating a component or net, the System Capture *Find* command helps in various other tasks.

1. Choose *Edit – Find and Replace*.

   The *Find and Modify* dialog is displayed.



   This dialog has three tabs: Component, Net, and Property. The options in the tabs are relevant to the type of object you are searching. You can also use *Advanced* options to fine-tune your search. For example, you can:

   - ❑ Search for exact matches or use wildcards and regular expressions.

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- Search for properties.

  Note: A property is shown on the object on which it was entered. Inherited properties are shown in Search and Property window.

- Restrict the parts of the design where you want to search
  - Blocks and sub-blocks

    When you have a page in a sub-block open and choose *Block/Page*, the block name changes to the parent block of the currently open page. This indicates that the scope of the search operation will be restricted to that block.

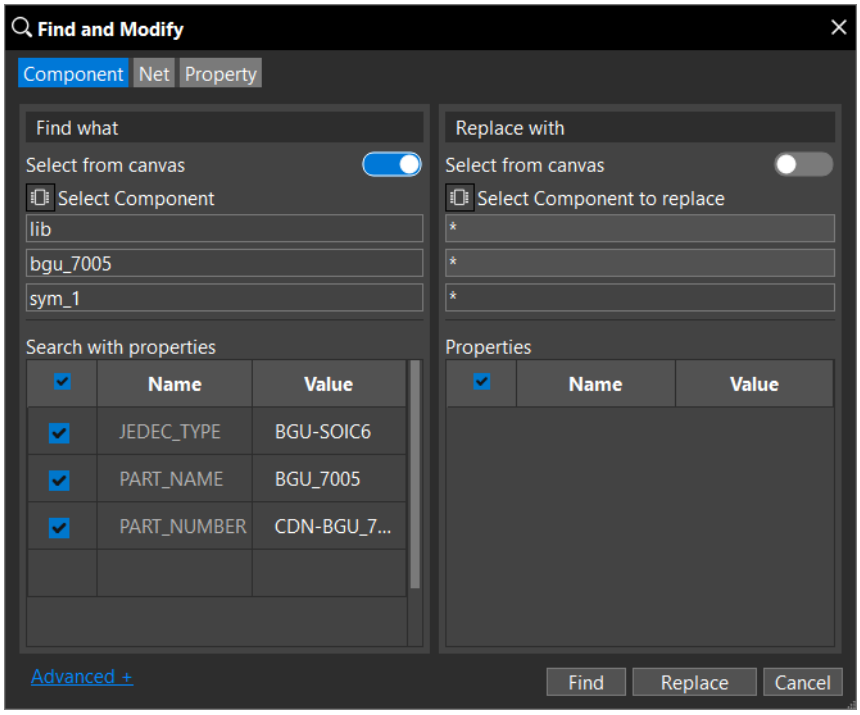
  - Page ranges

2. In the *Find what* section of the Component tab, specify the search criteria.

You can either select an instance on the canvas to auto fill the criteria, or manually specify the name of the instance.

3. Select the *Select from canvas* option and then click any instance of a component on the schematic.

The fields of the dialog are automatically populated with the attributes of the selected instance. On the canvas, the selected component gets a red-dotted boundary around it.



4. Click *Find* to search for all the instances matching the specified criteria.

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The results are displayed at the bottom of the application window.

Search

ref_5g (905) | ref_5g:Special Symbols (1758) | pwr:Special Symbols (195) | ref_5g:Auto Shapes (30) | pwr (124)

	REFDES	CELL NAME	Block Name	Page	JEDEC_TYPE	PACK_TYPE	PART_NAME	PART_NUMBER	SEC
	*	*	*	*	*	*	*	*	*
1		pwr	ref_5g						
2	U54	z1404	ref_5g	PA(32)	QFN10		Z1404	CDN-Z1404	1
3	U57	z1401	ref_5g	PA(32)	SOC5		Z1401	CDN-Z1401	1
4	Y2	y601	pwr	PWR(3)	CRY4		Y601	CDN-Y601	1
5	Y3	y500	ref_5g	WLAN(54)	CRY4		Y500	CDN-Y500	1
6	Y1	y1	ref_5g	NF(26)	CRY4		Y1	CDN-Y1	1
7	J1	xm-27-xp-119	ref_5g	Audio(5)	TP-SMD		XM-27-XP-119	CDN-XM-27-X...	1
8	J2	xm-27-xp-119	ref_5g	Audio(5)	TP-SMD		XM-27-XP-119	CDN-XM-27-X...	1
9	J21	xf2u_0415_3a	ref_5g	SIM(50)	CONN6-SMD		XF2U_0415_3A	CDN-XF2U_04...	1

The *Search* window displays all instances of component searched along with all the properties. You can sort and filter the data on any column of this dialog. You can double-click any row in this form to select the corresponding object on the canvas.You can also select one or more instances from this list.

Other tasks that can be done using the *Find and Modify* dialog box:

- Property Management
- Changing Reference Designators from Search Results
- External Editing of Find Results
- Reporting Search Results

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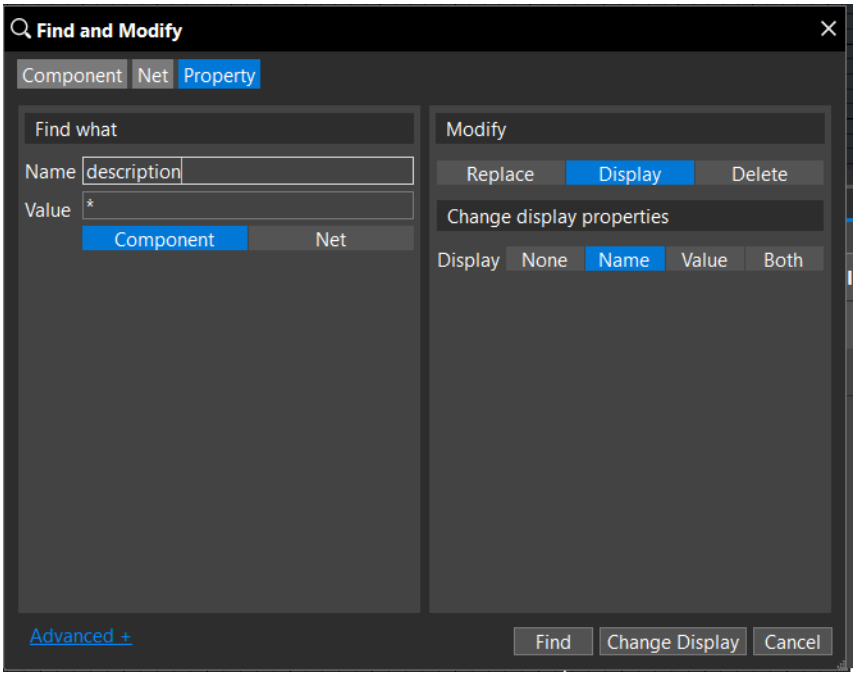
Property Management

In addition to changing the properties, you can also:

- Control the display of properties for components and nets



This is useful when a property is applied to multiple components or nets and you need to change the display settings for the name and values across the design.

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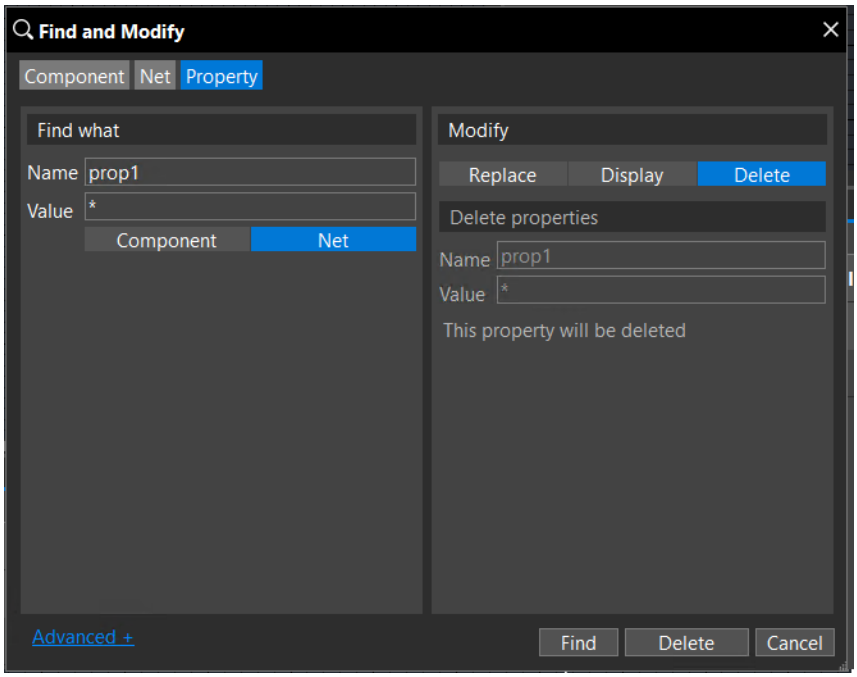
- Delete properties on components or nets as a batch operation.

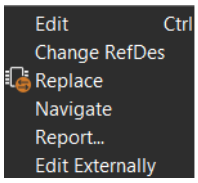


You can search for and delete any user-defined property that is applied to nets or components in the design. If you try to delete any system-defined property, you get an message that informs you that deleting reserved properties is not supported.

Changing Reference Designators from Search Results

To change reference designators from *Search Results*, follow these steps:

1. Select all the instances listed in the form.
2. Right-click the instances and choose *Change RefDes*.



The *Change RefDes* dialog box lists all the selected instances. The *Current RefDes* column displays the currently assigned RefDes of the instance. You can change this value in the *New RefDes* column.

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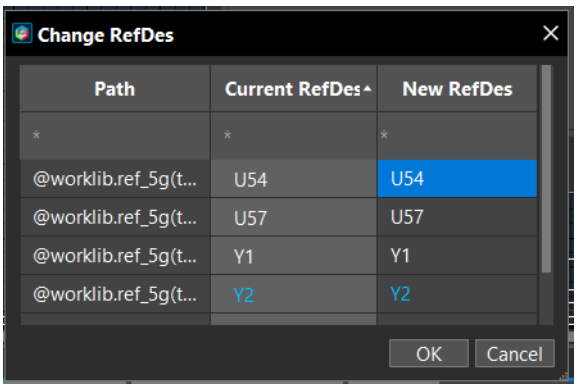
3. Change the RefDes of the instances.

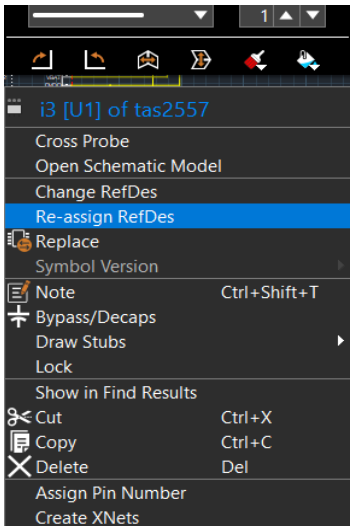


4. Click *OK* to confirm the changes.

   The RefDes of all the instances is changed. You can now see the updated RefDes on the schematic.

   The change in RefDes makes the RefDes of the components out-of-sync with the RefDes Pattern defined at the site level in the `site.cpm` file. System Capture provides an easy mechanism to repackage instances of a design, so that the default RefDes can be reassigned to the instances based on the RefDes Pattern. To do this, follow these steps:

5. Right-click the currently selected instances or on the block.



6. Choose *Re-assign RefDes*.

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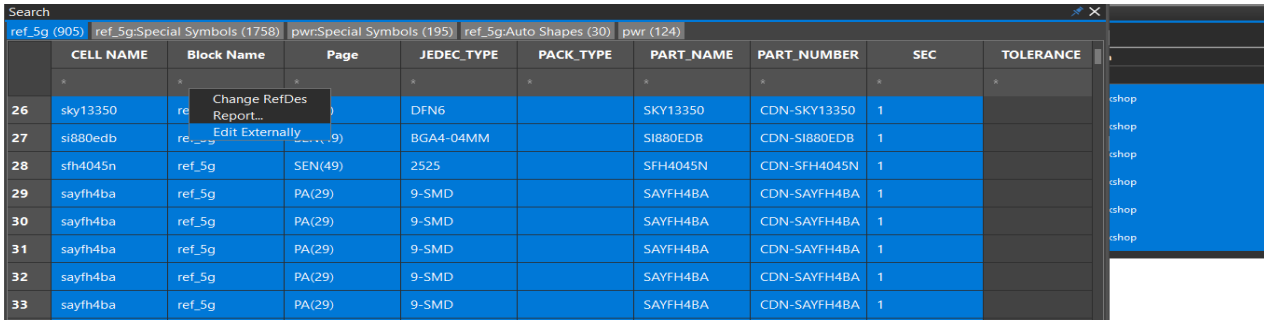
External Editing of Find Results

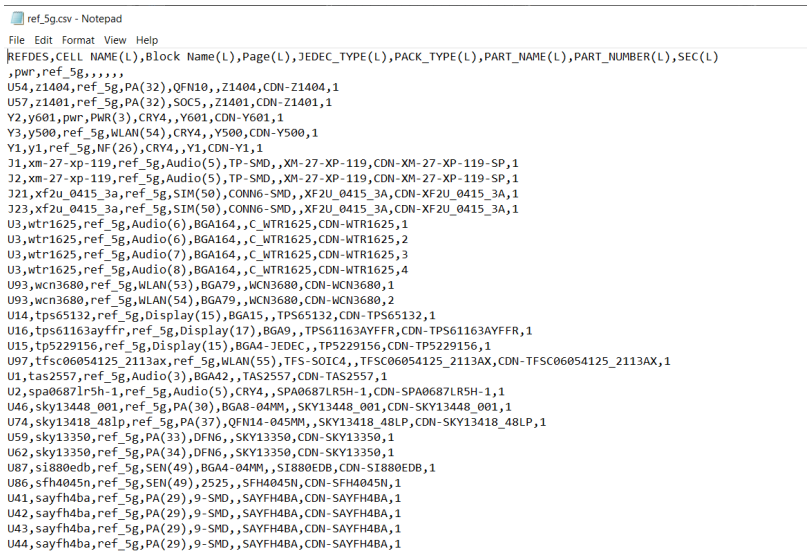
Another way to change the reference designators is by externally editing them. To do this, follow these steps:

1. Use *Find and Replace* to find all the components that need changes in the design.
2. The results are displayed in the *Search* window at the bottom of the application window.
3. Select all instances in the form.
4. Right-click and choose *Edit Externally*.



	CELL NAME	Block Name	Page	JEDEC_TYPE	PACK_TYPE	PART_NAME	PART_NUMBER	SEC	TOLERANCE
	*	*	*	*	*	*	*	*	*
26	sky13350	re		DFN6		SKY13350	CDN-SKY13350	1	
27	si880edb	re	9)	BGA4-04MM		SI880EDB	CDN-SI880EDB	1	
28	sfh4045n	ref_5g	SEN(49)	2525		SFH4045N	CDN-SFH4045N	1	
29	sayfh4ba	ref_5g	PA(29)	9-SMD		SAYFH4BA	CDN-SAYFH4BA	1	
30	sayfh4ba	ref_5g	PA(29)	9-SMD		SAYFH4BA	CDN-SAYFH4BA	1	
31	sayfh4ba	ref_5g	PA(29)	9-SMD		SAYFH4BA	CDN-SAYFH4BA	1	
32	sayfh4ba	ref_5g	PA(29)	9-SMD		SAYFH4BA	CDN-SAYFH4BA	1	
33	sayfh4ba	ref_5g	PA(29)	9-SMD		SAYFH4BA	CDN-SAYFH4BA	1	

The tool opens an external editor. The default editor for Windows is Notepad. To change the editor, use the `text_editor` directive.




```
REFDES,CELL NAME(L),Block Name(L),Page(L),JEDEC_TYPE(L),PACK_TYPE(L),PART_NAME(L),PART_NUMBER(L),SEC(L)
,pwr,ref_5g,,,,,,
U54,z1404,ref_5g,PA(32),QFN10,,Z1404,CDN-Z1404,1
U57,z1401,ref_5g,PA(32),SOC5,,Z1401,CDN-Z1401,1
Y2,y601,pwr,PWR(3),CRY4,,Y601,CDN-Y601,1
Y3,y500,ref_5g,WLAN(54),CRY4,,Y500,CDN-Y500,1
Y1,y1,ref_5g,NF(26),CRY4,,Y1,CDN-Y1,1
J1,xm-27-xp-119,ref_5g,Audio(5),TP-SMD,,XM-27-XP-119,CDN-XM-27-XP-119-SP,1
J2,xm-27-xp-119,ref_5g,Audio(5),TP-SMD,,XM-27-XP-119,CDN-XM-27-XP-119-SP,1
J21,xf2u_0415_3a,ref_5g,SIM(50),CONN6-SMD,,XF2U_0415_3A,CDN-XF2U_0415_3A,1
J23,xf2u_0415_3a,ref_5g,SIM(50),CONN6-SMD,,XF2U_0415_3A,CDN-XF2U_0415_3A,1
U3,wtr1625,ref_5g,Audio(6),BGA164,,C_WTR1625,CDN-WTR1625,1
U3,wtr1625,ref_5g,Audio(6),BGA164,,C_WTR1625,CDN-WTR1625,2
U3,wtr1625,ref_5g,Audio(7),BGA164,,C_WTR1625,CDN-WTR1625,3
U3,wtr1625,ref_5g,Audio(8),BGA164,,C_WTR1625,CDN-WTR1625,4
U93,wcn3680,ref_5g,WLAN(53),BGA79,,WCN3680,CDN-WCN3680,1
U93,wcn3680,ref_5g,WLAN(54),BGA79,,WCN3680,CDN-WCN3680,2
U14,tps65132,ref_5g,Display(15),BGA15,,TPS65132,CDN-TPS65132,1
U16,tps61163ayffr,ref_5g,Display(17),BGA9,,TPS61163AYFFR,CDN-TPS61163AYFFR,1
U15,tp5229156,ref_5g,Display(15),BGA4-JEDEC,,TP5229156,CDN-TP5229156,1
U97,tfsc06054125_2113ax,ref_5g,WLAN(55),TFS-SOIC4,,TFSC06054125_2113AX,CDN-TFSC06054125_2113AX,1
U1,tas2557,ref_5g,Audio(3),BGA42,,TAS2557,CDN-TAS2557,1
U2,spa0687lr5h-1,ref_5g,Audio(5),CRY4,,SPA0687LR5H-1,CDN-SPA0687LR5H-1,1
U46,sky13448_001,ref_5g,PA(30),BGA8-04MM,,SKY13448_001,CDN-SKY13448_001,1
U74,sky13418_48lp,ref_5g,PA(37),QFN14-045MM,,SKY13418_48LP,CDN-SKY13418_48LP,1
U59,sky13350,ref_5g,PA(33),DFN6,,SKY13350,CDN-SKY13350,1
U62,sky13350,ref_5g,PA(34),DFN6,,SKY13350,CDN-SKY13350,1
U87,si880edb,ref_5g,SEN(49),BGA4-04MM,,SI880EDB,CDN-SI880EDB,1
U86,sfh4045n,ref_5g,SEN(49),2525,,SFH4045N,CDN-SFH4045N,1
U41,sayfh4ba,ref_5g,PA(29),9-SMD,,SAYFH4BA,CDN-SAYFH4BA,1
U42,sayfh4ba,ref_5g,PA(29),9-SMD,,SAYFH4BA,CDN-SAYFH4BA,1
U43,sayfh4ba,ref_5g,PA(29),9-SMD,,SAYFH4BA,CDN-SAYFH4BA,1
U44,sayfh4ba,ref_5g,PA(29),9-SMD,,SAYFH4BA,CDN-SAYFH4BA,1
```

5. You can make changes in this files, for example, change the value of *ROOM* property to `BETA`.
6. Save the file and close the editor.

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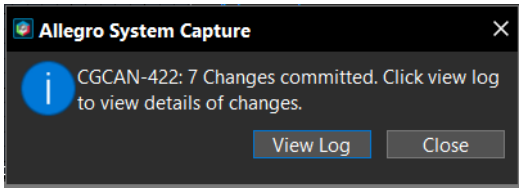
In System Capture, you are prompted to view the changes.

7. Click *View Log* to review the changes you have made.



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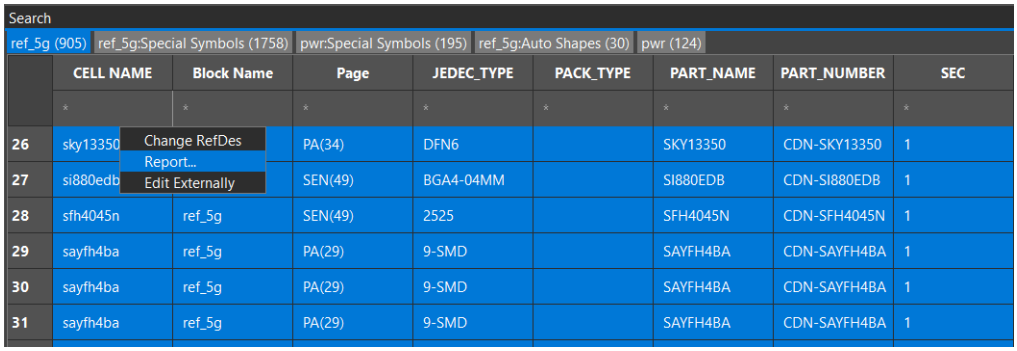
Reporting Search Results

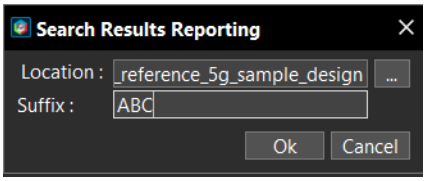
To generate a report for your search results, follow these steps:

1. Select all the columns in the *Search* window.
2. Right-click and choose *Report*.



	CELL NAME	Block Name	Page	JEDEC_TYPE	PACK_TYPE	PART_NAME	PART_NUMBER	SEC
	*	*	*	*	*	*	*	*
26	sky13350		PA(34)	DFN6		SKY13350	CDN-SKY13350	1
27	si880edb		SEN(49)	BGA4-04MM		SI880EDB	CDN-SI880EDB	1
28	sfh4045n	ref_5g	SEN(49)	2525		SFH4045N	CDN-SFH4045N	1
29	sayfh4ba	ref_5g	PA(29)	9-SMD		SAYFH4BA	CDN-SAYFH4BA	1
30	sayfh4ba	ref_5g	PA(29)	9-SMD		SAYFH4BA	CDN-SAYFH4BA	1
31	sayfh4ba	ref_5g	PA(29)	9-SMD		SAYFH4BA	CDN-SAYFH4BA	1

3. Specify the location and suffix for the report.



4. Click *OK*.
5. Open the Project folder to view the file.

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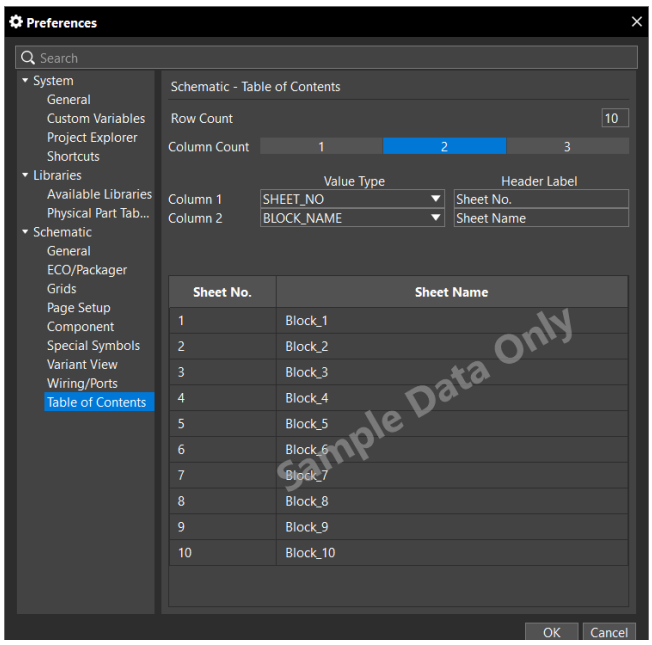
Adding a Table of Contents

System Capture can automatically generate Table of Contents (TOC) for a design. A *Table of Contents* is treated as a separate section of the design that follows a different page-numbering scheme compared to the design pages.

The TOC displays data for the complete design hierarchy. All the blocks instantiated in the design are displayed in the TOC.

To add a table of contents:

1. Choose *Edit – Preferences*.
2. The *Preferences* window opens.
3. Choose *Schematic – Table of Contents.*



4. Specify the row count.

   This is the number of rows on a page.

5. Specify the column count.

   This is the number of columns on a page.

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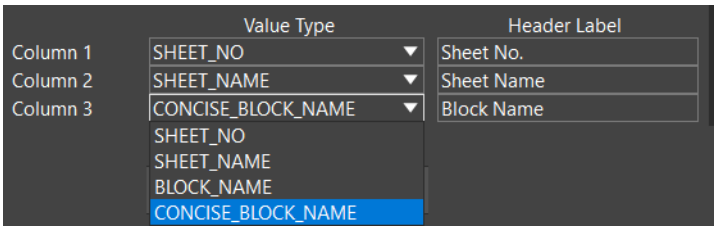
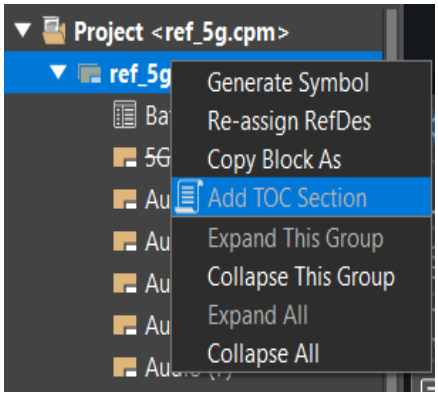
6. Specify the content for the columns.



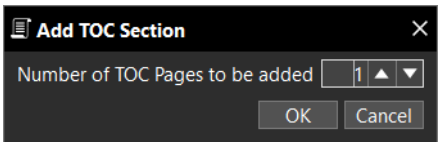
The header for the column is populated automatically.

7. Click *OK* to close the *Preferences* window.
8. Right-click the block in *Project Explorer* and choose *Add TOC Section*.



The Add TOC Section dialog is displayed.

9. Specify the number of pages to be added for the TOC.
10. Retain the default value of 1.



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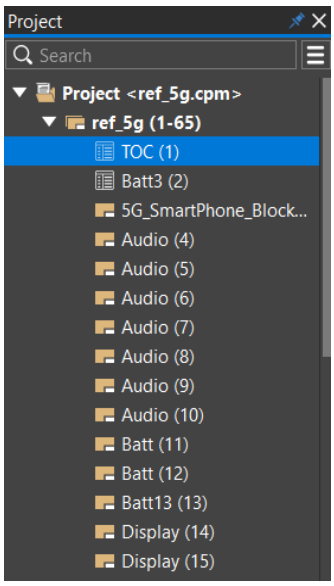
This inserts one new page in the root design. Note that the numbering of this page is (1). Also, the page numbering of the other pages of the design changes accordingly. Rename the newly added page to *Table of Contents*.



11. Choose the *Place – Table of Contents* menu command.

The Table of Contents symbol is attached to the cursor.

12. Place the symbol on the schematic sheet.

13. Select the cells and change the font size for better readability, if required.

Sheet No.	Sheet Name	Block Name
1	Page	/sld_bu1
2	Page	/sld_bu1
3	page	/dcu004
3	page	/dcu004
5	page	/sld_bu1/dcu004(dcu004)
6	page	/sld_bu1/dcu004(dcu0041)

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After the symbol is placed, the TOC is populated based on the schematic data.

- The first column of the table shows the Sheet Number. These sheet numbers are hyperlinks and navigate to the schematic sheet.
- The next column contains the Name of the Sheet.
- The last column contains the name of the block containing the sheet.

If all the pages in the design do not fit into a single table, place more Table of Contents symbols on the schematic sheet.

Adding Hyperlinks

Hyperlinks provide an easy way to navigate in System Capture. All text objects, such as x and y, notes as well as properties can be made hyperlinks. The target of a hyperlink can be:

- A web page

  The web page is opened in the default web browser.

- A file

  The file is opened in the default program associated with the file type.

- Location in the project

  The target of a hyperlink can also be a schematic page in the project. You can also configure the hyperlink to a zone on a schematic sheet in the project. This displays the specified schematic sheet and zooms into the specified zone on the schematic sheet.

- An email address

  You can also configure an email address as a target of a hyperlink. On clicking the hyperlink, the default mail client configured in the system is used and an email message is created for the specified email id.

The hyperlinked text is visible on the schematic with hyperlink formatting— underlined and colored blue. When you hover the mouse pointer over the text, a tooltip appears with details of the hyperlink. `Ctrl`+click the hyperlink to navigate to the target location.

In a *Table of Contents*, the entries in the *Sheet Number* column are automatically hyperlinked to display the corresponding page of the design. In case of a hierarchical design, the occurrence of the block is auto-resolved and the relevant sheet is opened.

To add a hyperlink to text:

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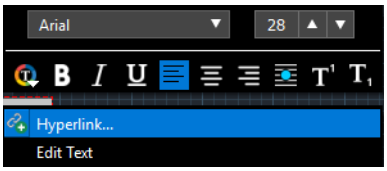
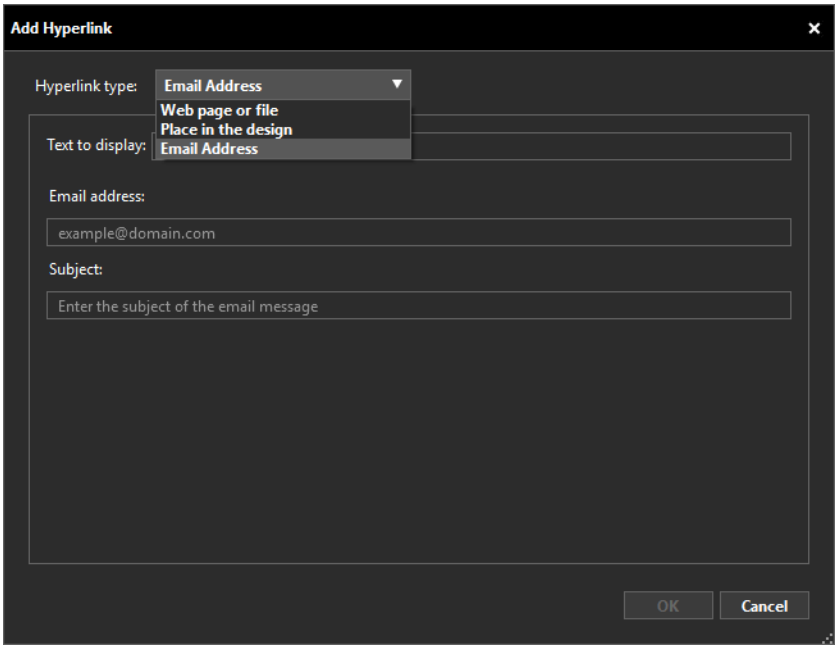
1. Select the text.
2. Right-click and choose *Hyperlink*.



The *Add Hyperlink* dialog box opens.



3. Choose the type of hyperlink.

   The *Text to display* field shows the currently selected text. If required, the text can be modified.

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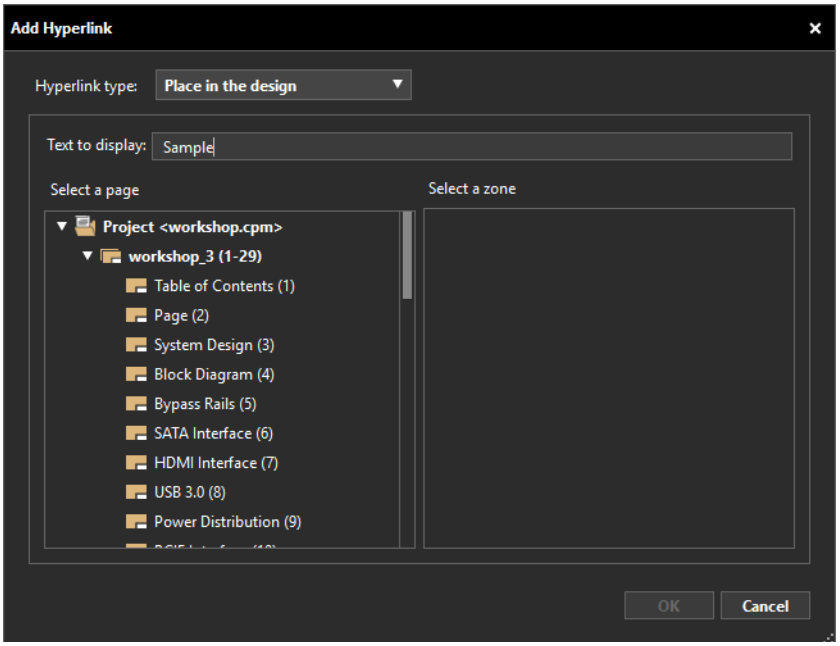
4. Choose *Place in the design* in *Hyperlink type*.

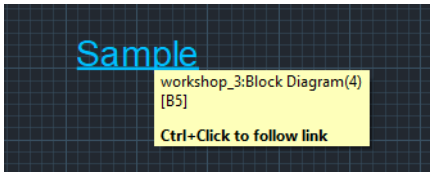


   a. Select the schematic sheet

   b. Select the zone.

5. Click *OK* to associate the hyperlink to the selected text.

6. Move the mouse pointer over the text to display the tooltip showing the target of the hyperlink.



Similarly, hyperlinks can be created for websites, files, or email addresses.

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3

NetGroups and PortGroups

NetGroups are used to group net objects and provide a faster way of connecting them to components across schematic pages. Different types of net objects, such as nets, buses, and NetGroups, can be members of a NetGroup. A NetGroup is treated as a single entity.

A NetGroup is a completely heterogeneous collection of nets. Unlike a bus, which is homogeneous collection of nets (scalar or vector), a NetGroup provides a greater flexibility in grouping nets together.

NetGroups can be of two types:

- Single-level NetGroups

  NetGroups that have nets and buses as members are called single-level NetGroups.

- Nested NetGroups

  NetGroups that have other NetGroups as members are called nested NetGroups.

Important

The nets in a NetGroup can be a scalar, vector, or a combination of both. However, a net can belong to only one group at a time.

PortGroups are used in hierarchical designs to replicate the lower-level NetGroup structure, on a higher-level block. A PortGroup is an interface port on a hierarchical symbol that corresponds to a NetGroup used in the lower-level schematic. Using PortGroups, connections to NetGroups members can be created at a higher level of hierarchy, thus further speeding up the task of capturing connectivity.

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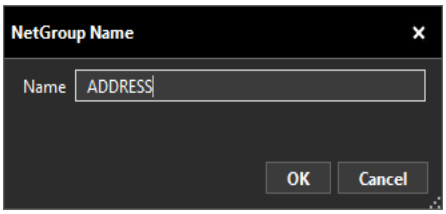
Creating a NetGroup

You need to create a NetGroup to add member objects to it, like existing nets or NetGroups. To add a NetGroup, follow these steps:

1. Click the icon for drawing NetGroups on the toolbar.

2. Click the canvas to mark the starting point.
3. To specify the NetGroup name when drawing it, type the name in the box on the top-left of the canvas.
4. Double-click to mark the end of the NetGroup.
5. Specify a name for the NetGroup, if not specified already.

   A NetGroup cannot have a system-generated name. Only user-defined names are supported.



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The name gets assigned to the NetGroup and is visible on the NetGroup segment.

At any point, you can rename the NetGroup by right-clicking it and choosing *Rename NetGroup*.

Related Topics

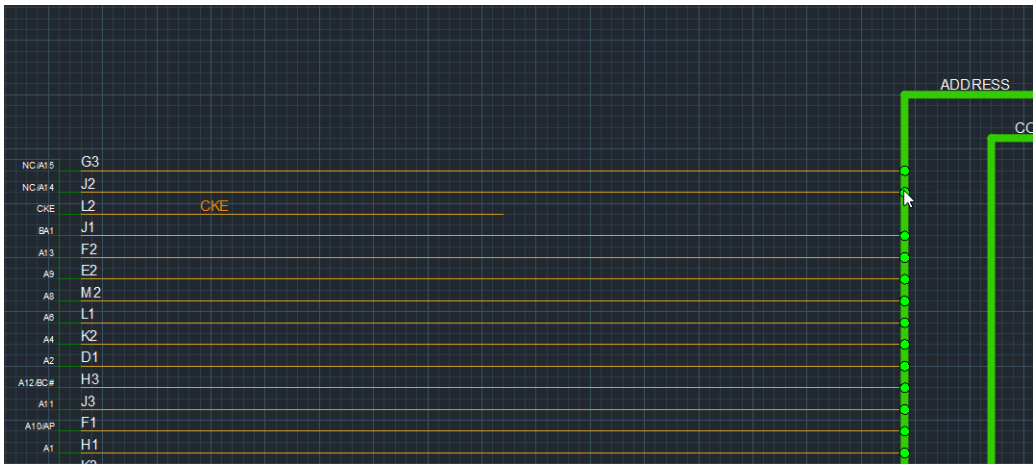
- Tapping Members from NetGroups
- Controlling NetGroup Names Usage
- Renaming NetGroups and Members

Adding Member Objects to NetGroups

To add new members to a NetGroup as they are created, drop them on a NetGroup. To add existing nets or NetGroups to a NetGroup:

1. Select all the net objects that you want to add.
2. Drag the nets using their end points.

   As the dragged nets touch the NetGroup, green dots are displayed signaling that these nets can be added as members of the NetGroup.



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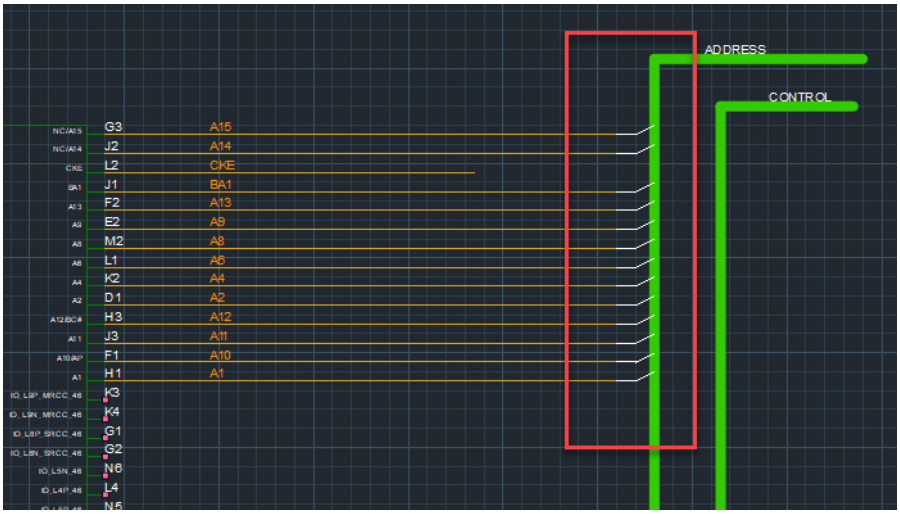
3. Drop the nets on the NetGroup.



When you drop the nets on the NetGroup, tap symbols are placed on the NetGroup and each net gets added as a member of the NetGroup.

Related Topics

- Controlling NetGroup Names Usage
- Renaming NetGroups and Members

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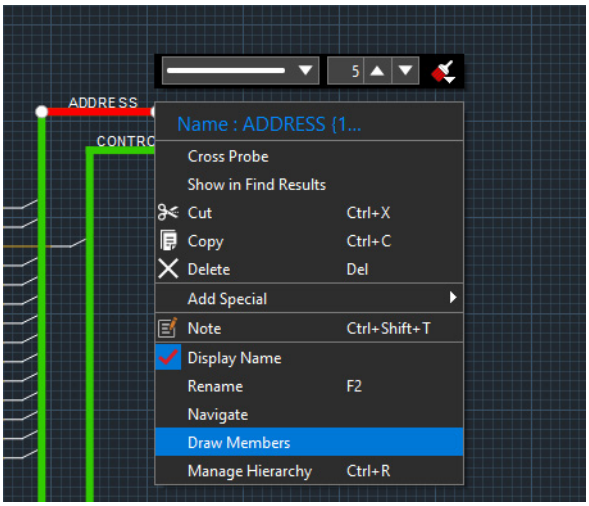
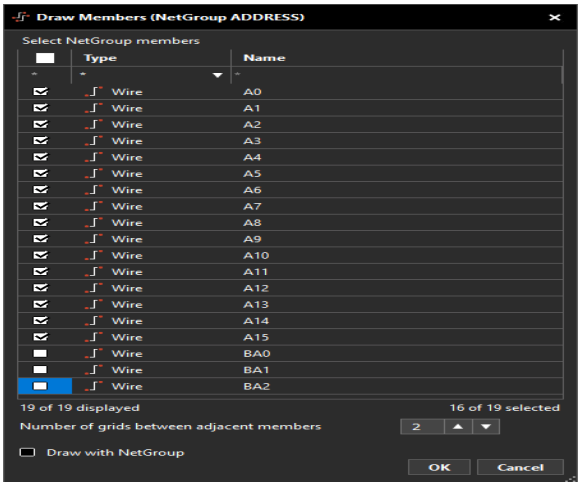
Tapping Members from NetGroups

To connect a NetGroup to components, you need to tap-out wires from the NetGroup and connect them to the component pins or wires. To tap-out members from the NetGroup:

1. Right-click a NetGroup and choose *Draw Members*.



The *Draw Members (NetGroup <name>)* dialog box opens.



A list of the members of the NetGroup is shown.

2. Select the check boxes for nets to tap out.

   This can be quickly done by checking the check box in the header for selecting all the bits.

   Notice at the bottom of the dialog, the number of selected bits is displayed.

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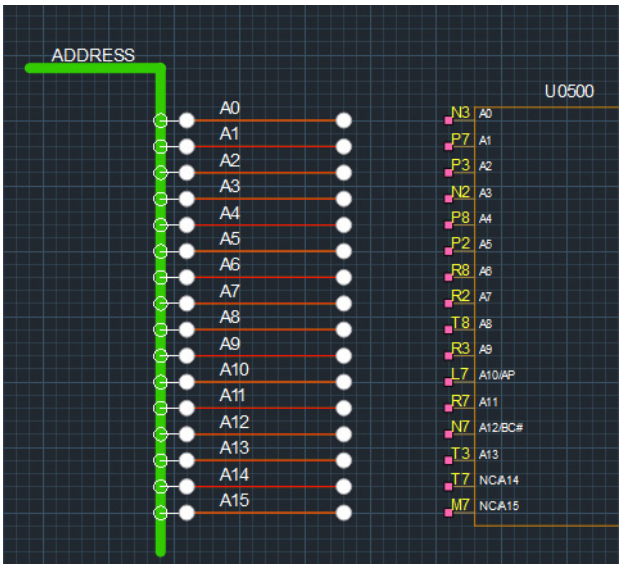
3. Click *OK*.

   This attaches the selected nets to the cursor.

4. Move them so that the left ends overlap the NetGroup and the wires are aligned to the pins of the component.

   As the wires overlap the NetGroup, green dots show that connections can be established.



5. Drop the wires and notice that the wire segments are now tapped-out from the NetGroup. Also, each of the wires is named based on the selected member of the NetGroup.

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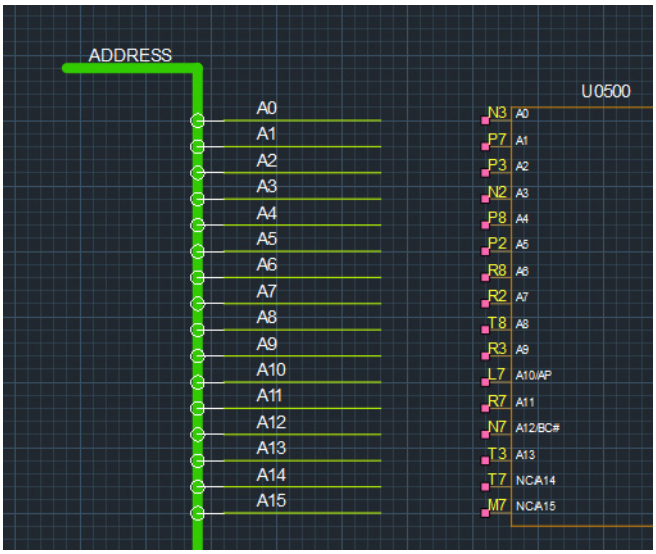
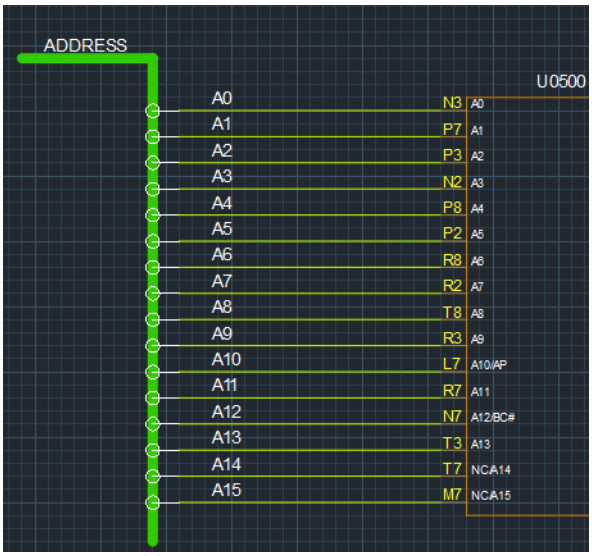
6. Select all the tapped-out wires and drag and drop them on component pins.





Connections are created between the pins and the wire segments from the NetGroup's members.

Related Topics

- Creating a NetGroup
- Controlling NetGroup Names Usage

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Renaming NetGroups and Members

There are two ways in which NetGroups and members can be renamed:

- Using Find and Replace
- Using the Rename NetGroup Command

Using Find and Replace

The *Find and Replace* command enables you to rename all instances of NetGroups or members at once. To rename using the *Find and Replace* command, follow these steps:

1. Choose *Edit – Find and Replace*.
2. Specify the Netgroup to rename.
3. Specify a new name of the NetGroup.
4. Click *Advanced*.
5. Ensure the *Scope* is *Entire Design*.

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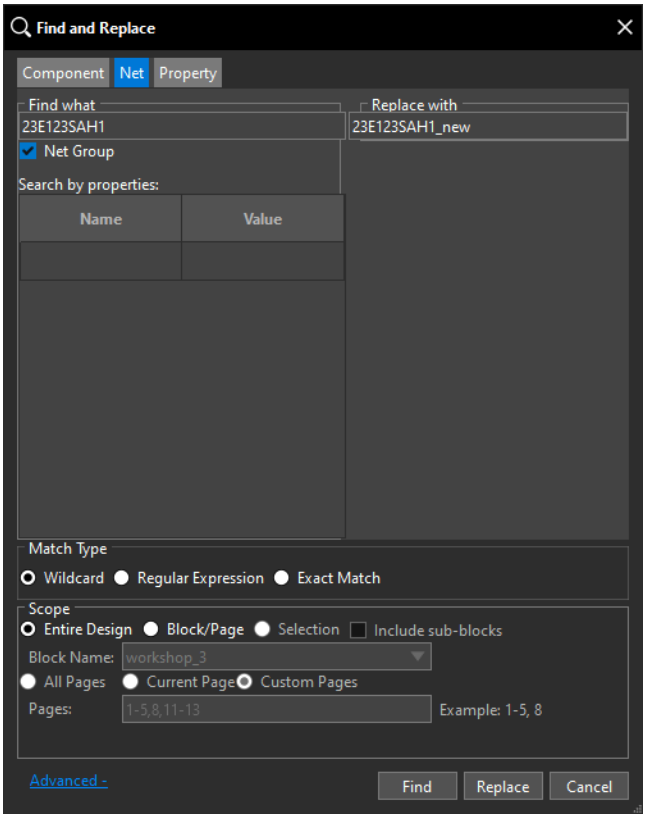
6. Click *Replace*.



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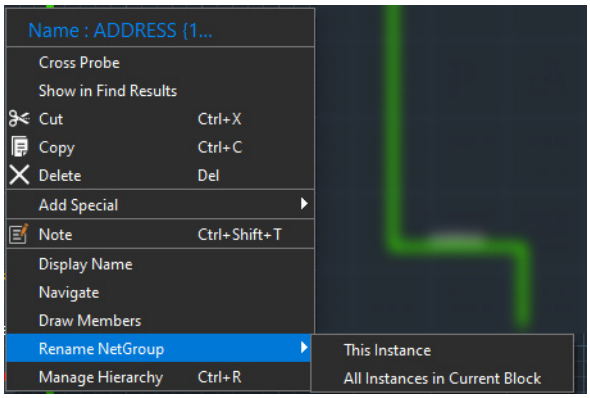
Using the Rename NetGroup Command

Using the *Rename NetGroup* command, you can rename a NetGroup or its member's particular instance or all their instances in a block. To rename a NetGroup and its members using the *Rename NetGroup* command, follow these steps:

1. Right-click the NetGroup and choose *Rename NetGroup*.



   Two options with self-explanatory names are available. If multiple instances of the same NetGroup exist in the block, you can rename just the selected NetGroup instance or make the same changes to all instances of the selected NetGroup in the block.

   If there are no other instances of the selected NetGroup, only the *All Instances in Current Block* option is available.

2. Choose *This Instance*.

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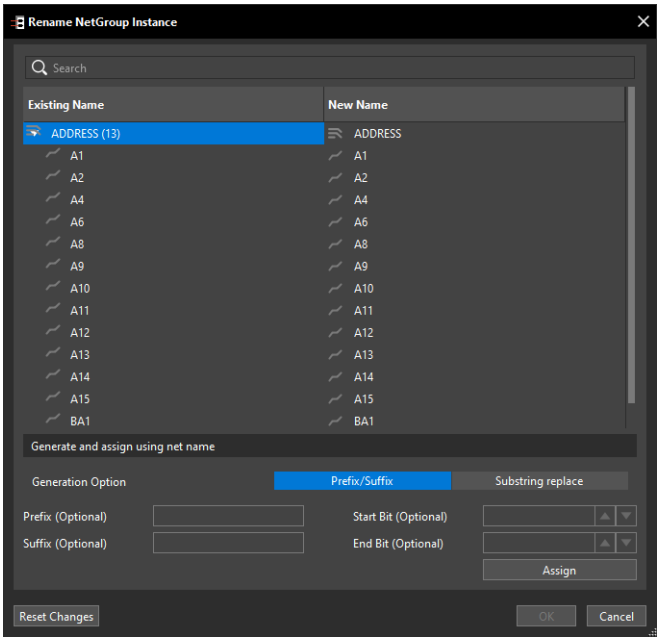
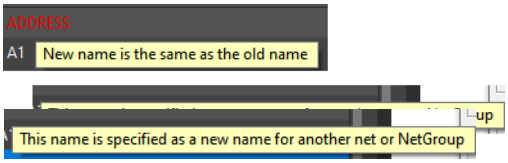
The *Rename NetGroup* Instance dialog box opens.



3. Select the rows that need to be renamed.
4. Specify a new name for the NetGroup and its members using any of the following ways:
   - ❑ Typing in the new name in the *New Name* column
   - ❑ Specify the Prefix/Suffix options
   - ❑ Use the Substring replace options
5. Click *Assign* to apply the prefix, suffix, or string replacements.

   If any change cannot be made, the text turns red and you can see a tooltip that explains what has gone wrong. For example:



When renaming a NetGroup or its members System Capture runs multiple checks, such as:

- ❑ The new name cannot be used for the type of object selected. For example, a name in scalar format for a bus or reverse.

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- ❑ The new name is already in use.
- ❑ The new name has unsupported characters.
- ❑ The base name for all the bits of a bus must be identical.
- ❑ The start and end bits cannot be changed.
- ❑ The width of a bus cannot be changed.
- ❑ New name is the same as the old name.

6. Correct the errors flagged by the red text.

After the errors are removed, the changed names show in bold. This helps to easily identify the changes.

7. Click *Reset Changes* if you need to revert to the original.

8. Click *OK* to apply the changes.

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Adding PortGroups to Designs

PortGroups are used in hierarchical designs to replicate the lower-level NetGroup structure, on a higher-level block. A PortGroup is an interface port on a hierarchical symbol that corresponds to a NetGroup used in the lower-level schematic. Using PortGroups, connections to NetGroups members can be created at a higher level of hierarchy, speeding up the task of capturing connectivity.

In other words, a PortGroup is a special type of port/pin on the block symbol through which all members of the NetGroup are available to the higher level of hierarchy.

The main tasks when working with PortGroups are:

1. Create a new block and add components and connectivity.

   This is explained in the Creating a New Block section.
2. Create PortGroups.
3. Generate the symbol for the block.
4. Place the block symbol on a higher level.
5. Add connectivity to the PortGroup on the higher block.
6. Modify the members of the PortGroup
7. Modify the structure of a NetGroup.

Related Topics

- Creating a New Block
- Adding PortGroup Connectivity

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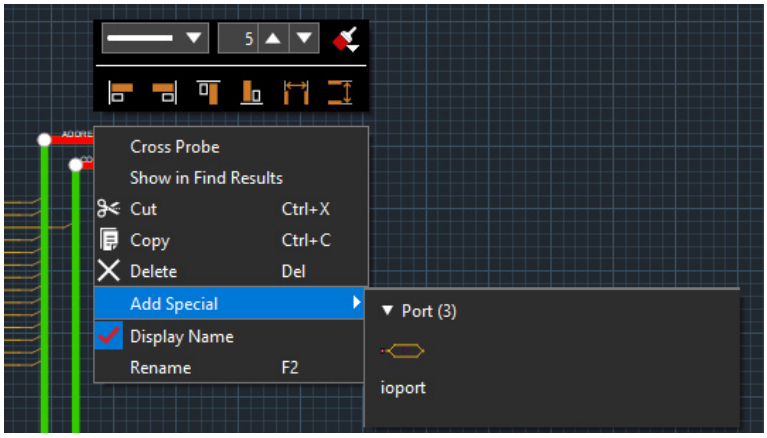
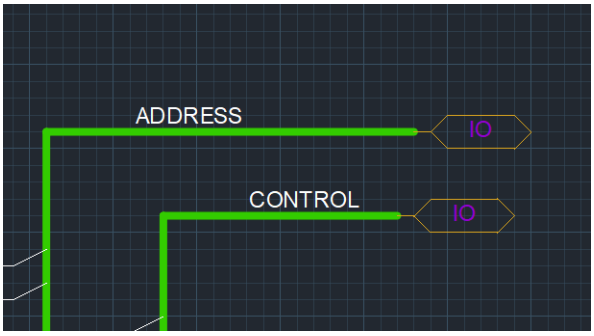
Creating a PortGroup

To create PortGroups for existing NetGroups and updating the block symbol with the PortGroups, follow these steps:

1. Select the NetGroups.
2. Right-click and choose *Add Special – ioport*.



The symbol for IOPORT gets attached to the selected NetGroups. These NetGroups have now been identified as interface objects and would become PortGroups on the block symbol.



Now update the block symbol to generate the PortGroups on the block symbol.

3. In the *Project Explorer*, select the block.

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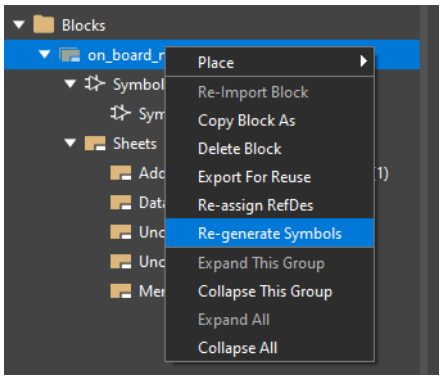
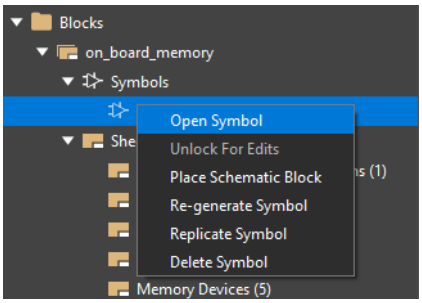
4. Right-click and choose *Regenerate Symbol* to refresh the block symbol with the new interface definitions.



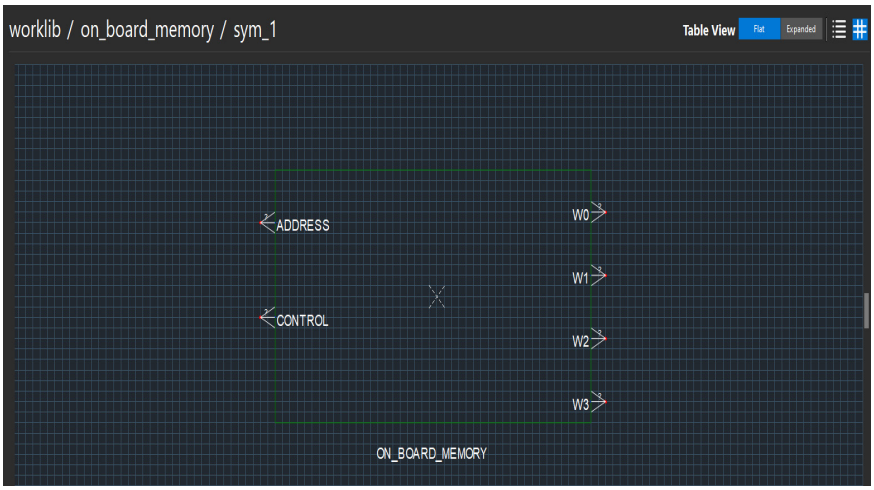
The block symbol would be updated and the new PortGroups are added to it.

5. In the *Project Explorer*, select *Symbol 1*.

6. Right-click and choose *Open Symbol* to open the block symbol in Symbol Editor.



Symbol Editor opens as a new window displaying the newly added PortGroups placed on the symbol.



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7. Edit the symbol, if needed.
8. Save the changes made to the symbol.
9. Close the symbol tab.

The block symbol has now been updated and all the PortGroups are now available on the block symbol for connections.

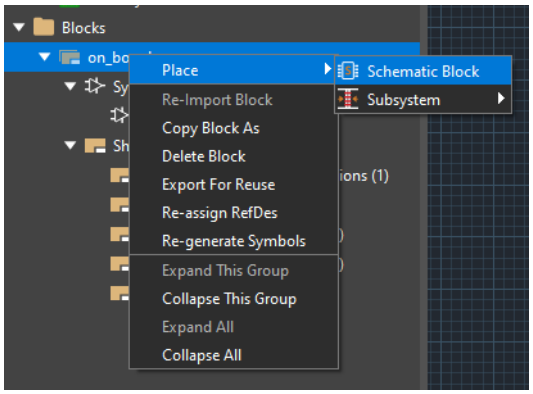
The next step is to place this symbol on a higher-level page.

Adding PortGroup Connectivity

PortGroups can be connected only to NetGroups. The structure of the NetGroup can be different from the PortGroup. You can connect the member nets of a NetGroup manually or go with the default connections that System Capture builds.

To instantiate the block in the top-level design and make connections to the PortGroups, follow these steps:

1. Open a page in the top-level design.
2. Right-click the block to be instantiated and choose *Place – Schematic Block*.



The block symbol attaches to the cursor.

3. Click the schematic sheet to place it.

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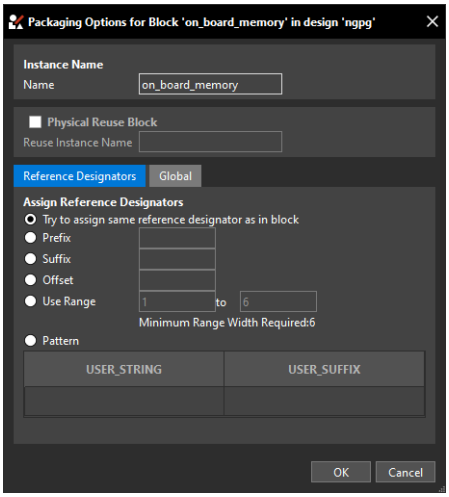
The *Packaging Options* dialog box opens.

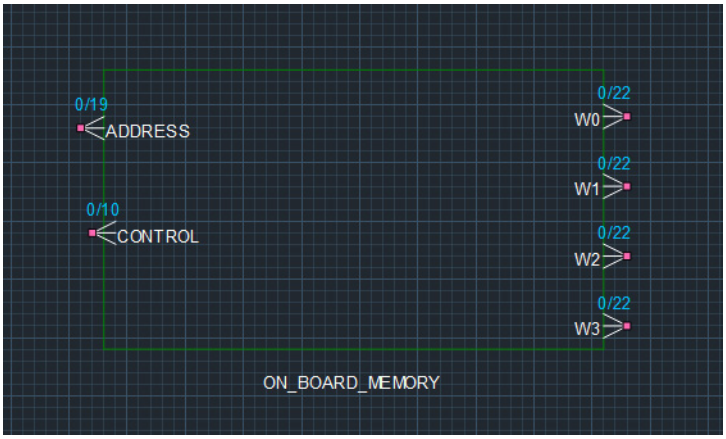


Make changes if needed, or continue with the defaults.

4. Click *OK*.

5. Press `Esc` to exit the block placement mode.

   The schematic block symbol is now placed on the schematic.



All the PortGroups from the block are unconnected and the number of connections and total members of the PortGroup are displayed. For example, PortGroup ADDRESS has 19 members, CONTROL has 10 members, and so on.

The next step is to add connectivity. You can create NetGroups, add existing NetGroups, or use the *Draw Stubs* option.

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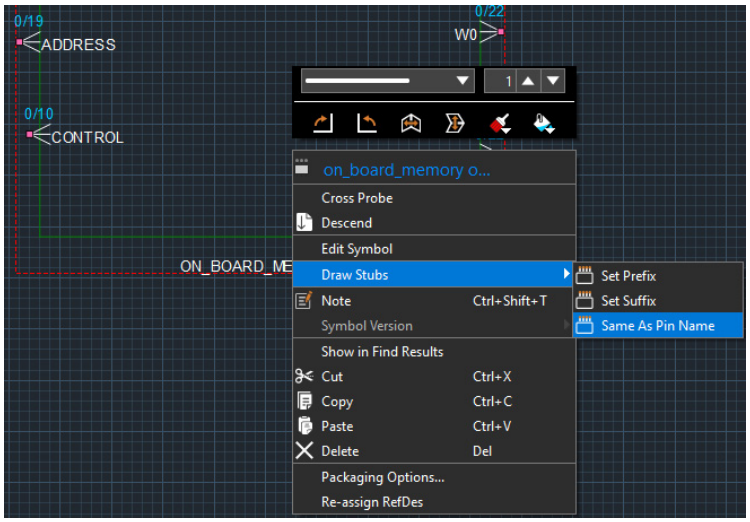
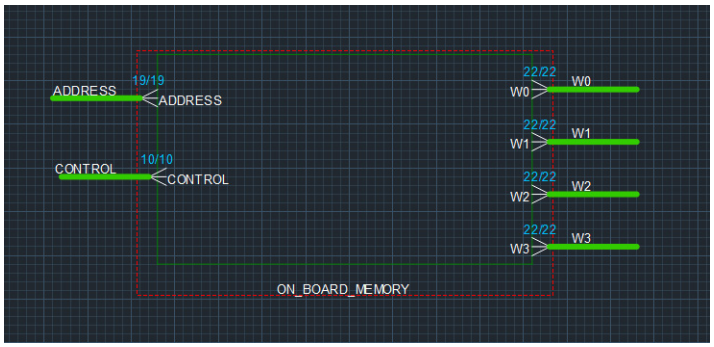
Adding NetGroups with Default Members

In this section, the *Draw Stubs* option is used.

1. Right-click the block and choose *Draw Stubs*.



2. Choose *Same as Pin Name*.



The following changes happen at this time:

- ❑ NetGroups are added with the same name as the PortGroup names.
- ❑ The connectivity has changed. All the PortGroups are completely connected.

You can view the members of the newly created NetGroups.

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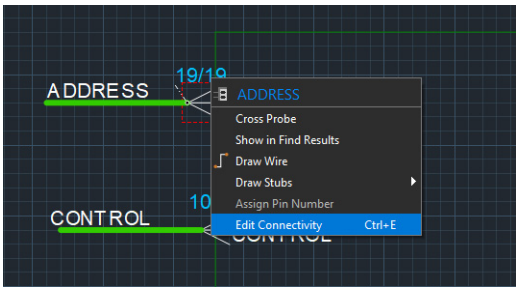
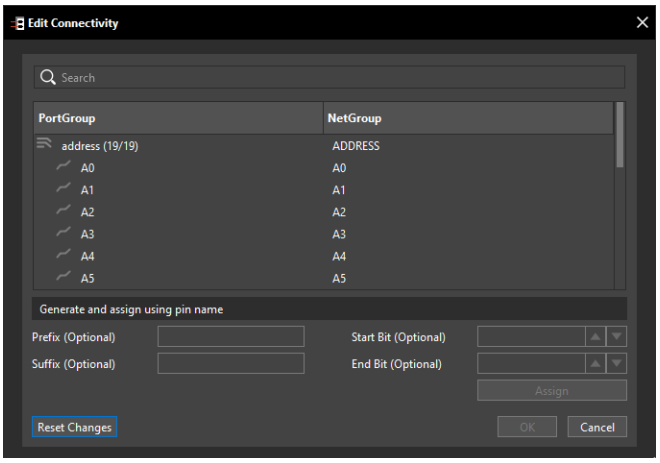
3. Right-click the PortGroup and choose *Edit Connectivity*.



The *Edit Connectivity* dialog box opens. The members of the NetGroups have been connected to the PortGroup members on the basis of their names.



In this dialog box, you can:

- Change the connectivity.

  Membership might also change when connectivity changes.

- The net name shows in bold for the changed entries.

- Connect PortGroup members with existing NetGroup members.

- Using Prefix, Suffix, or Substring replace, connections are setup for PortGroup members with existing NetGroup members or by creating new members.

- Delete the connection between the PortGroup pin and NetGroup member.

  Choose *Clear* in the drop-down list.

- Change the names of the connected nets.

  Set the prefix or suffix and click *Assign*.

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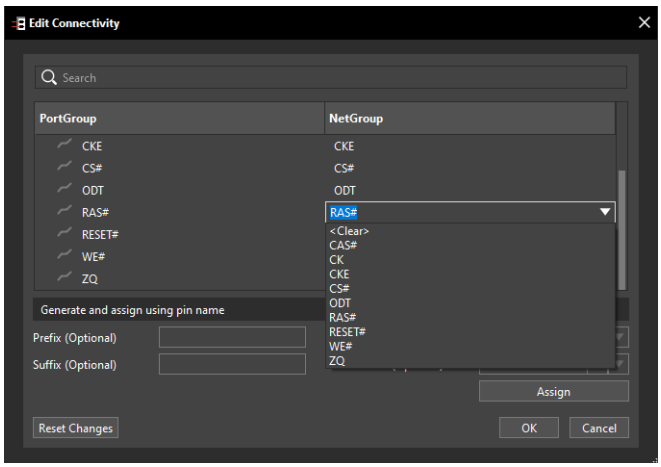
Note: When any change is made to the name of a NetGroup or bus, all its members automatically get the same changes.

- ❑ Change the bits connected for a bus.

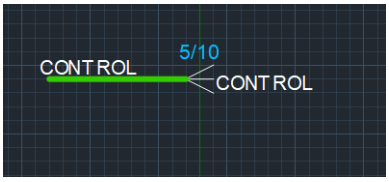
  Choose the start and end bits and click *Assign*.

- ❑ Reset any changes made.



4. Click *OK* to close the dialog box.

You can make the required changes and the status of the connections is updated on the schematic.



This completes the automatic NetGroup addition.

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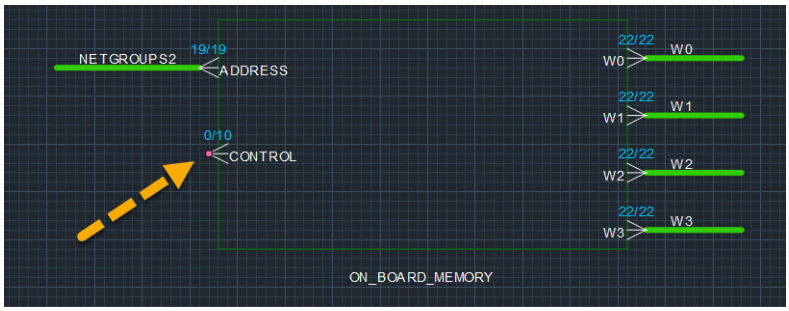
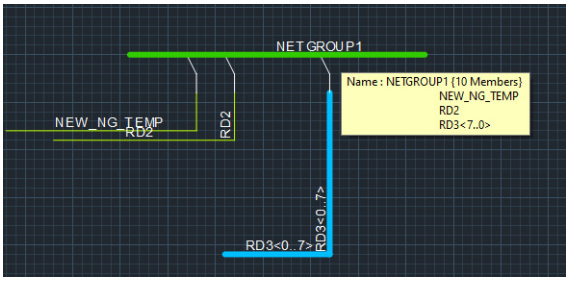
Adding Custom Membership

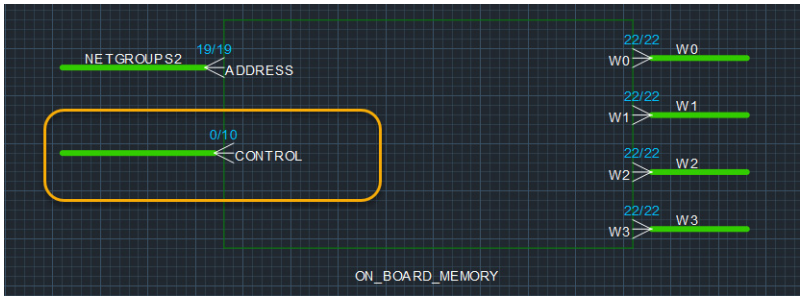
You can also build the connectivity for a PortGroup. In this section, an existing NetGroup will be attached to a PortGroup. And the connectivity between PortGroup pins and NetGroup members will be specified.



1. Connect an existing NetGroup, for example `NetGroup1` with the following structure.



2. Draw a NetGroup from the PortGroup and name it `NetGroup1`.



There are no connections at this time because the names of the NetGroup members do not match the PortGroup members. The next step is to add connectivity between pin and nets.

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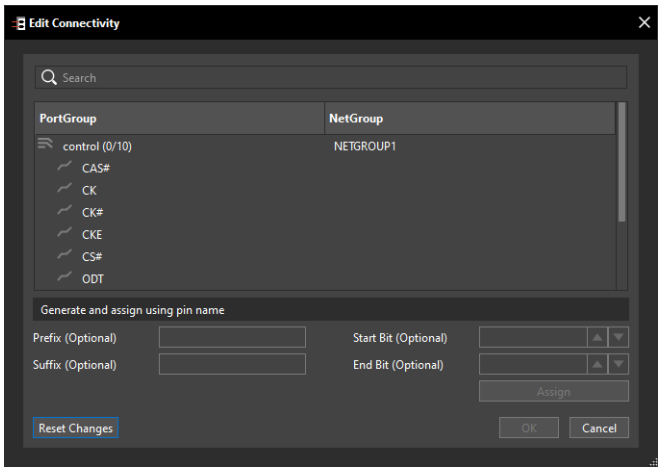
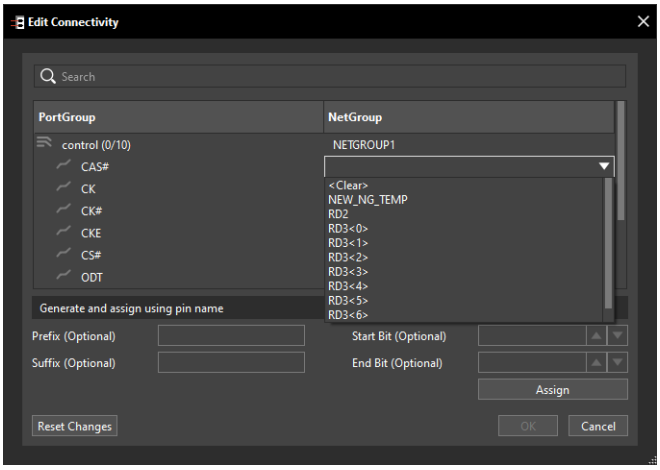
3. Right-click the PortGroup and choose Edit Connectivity.



4. Click in the NetGroup column for a PortGroup row.
5. Select the net to connect to the PortGroup pin.



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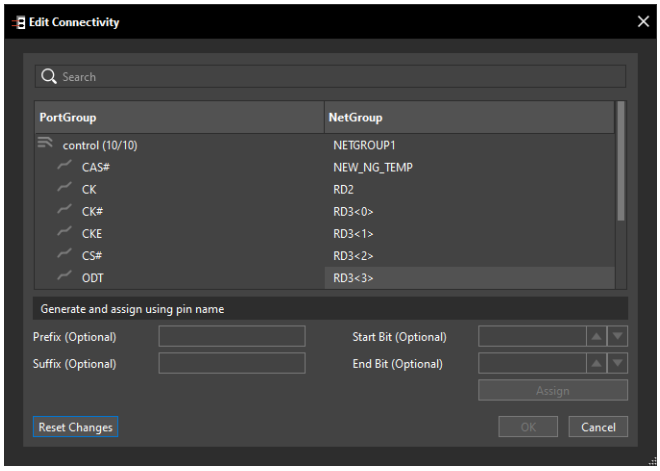
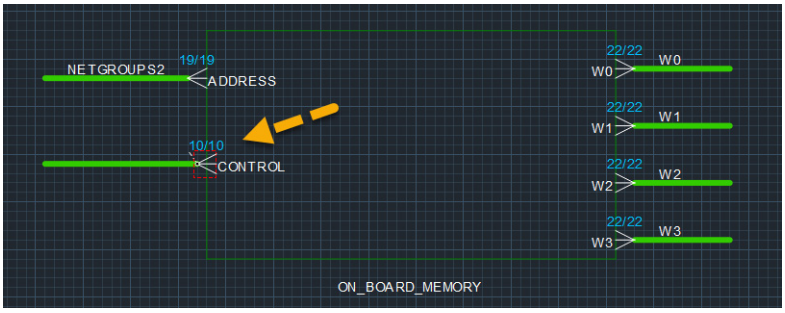
6. Repeat for all the pins.



7. Click OK.

   The connections are updated.



This completes the custom addition of NetGroups and members.

Related Topics

Adding PortGroups to Designs

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Modifying the Structure of NetGroups Connected to PortGroups

The structure of NetGroups connected to PortGroups can be modified at any time.

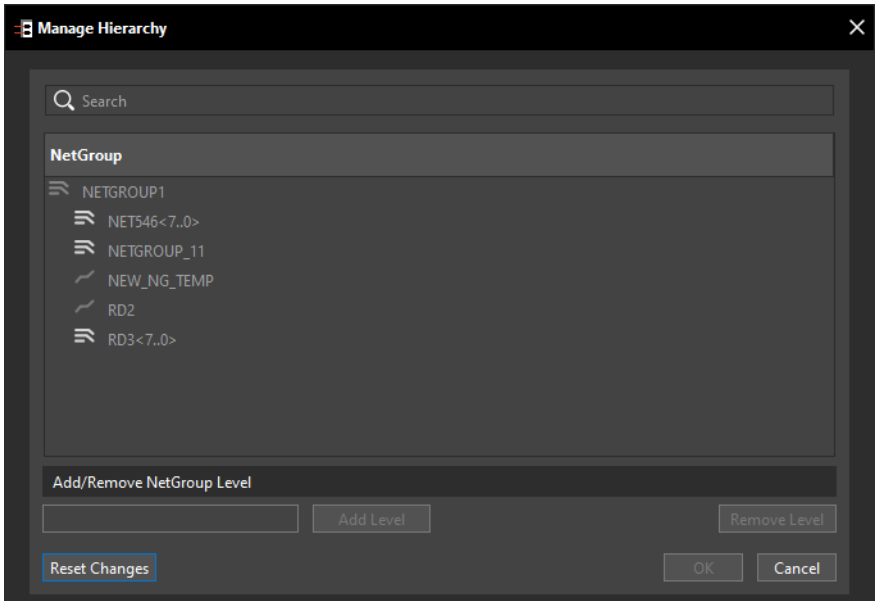
Note: The structure or membership of tapped out NetGroup members cannot be modified

To add or remove members of a NetGroup:

1. Right-click a NetGroup and choose *Manage Hierarchy*.

   The *Manage Hierarchy* dialog box opens. All the members of the NetGroup are listed.

   You can see NetGroups, vector nets (buses), and scalar nets.



   You can add and remove NetGroups.

2. To add a new NetGroup:

   a. Type a name for a new NetGroup.

   b. Click *Add Level*.

   c. Move a net to the newly added level by dragging and dropping.

   Note: If no net is placed under this NetGroup, it will not be saved.

   d. Click *OK*.

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3. To remove a NetGroup:

e. Click the *NetGroup*.

f. Click *Remove Level*.

When removing levels, the following points need to be considered:

- Only non-tapped out NetGroups can be deleted.
- Members that cannot be moved are shown disabled, for example gray in the dark theme.
- Members that can be moved or dragged are visually easy to identify. For example, shown in white in the dark theme.
- When a level is deleted, all its members move up to its parent level.
- Members of any NetGroup level can be moved to another member NetGroup.

g. Click *OK*.

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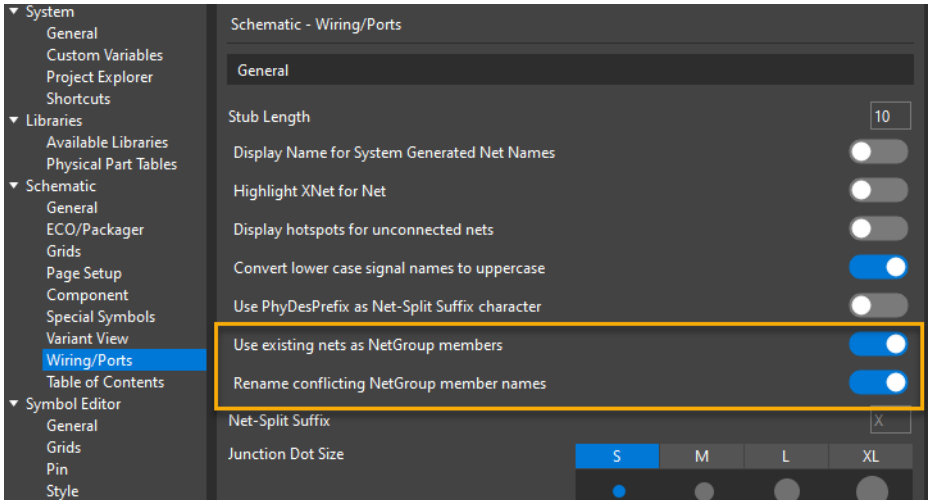
Controlling NetGroup Names Usage

The *Preferences* dialog has the following controls for NetGroups. Both the controls are selected by default. It is recommended that you continue with these default settings.



- *Use existing nets as NetGroup members*
- *Rename conflicting NetGroup member names*

When new NetGroups are added to a design by commands, such as using *Import Sheet*, copy pasting, making changes in the *Edit Connectivity* dialog box and so on, you can control how System Capture manages new members or new NetGroups.

If these controls are disabled, you might see name changes for nets and when the renaming option is disabled, many commands might fail.

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4

Constraints

A constraint is a user-defined requirement applied to a net or pin-pair in a design. The Allegro platform supports the following types of constraints:

- Electrical Constraints

  An electrical constraint is a rule that characterizes and constrains the electrical behavior of a net. Impedance and propagation delay are examples of electrical constraints.

- Physical Constraints

  A physical constraint is a rule that characterizes and constrains the physical instantiation of a net. Minimum line width and minimum neck width are examples of physical constraints that apply to the connect lines (clines) of a net.

- Spacing Constraints

  A spacing constraint is a rule that specifies the spacing between two physical objects. These objects may be the physical instantiation of the same net or different nets. Line-to-line spacing is an example of a spacing constraint that applies between two connect lines (clines).

- Design Constraints

  A design constraint is a rule that applies to the entire physical design. These constraints are independent of the electrical circuit. Soldermask alignment and testpoint spacing are examples of design constraints.

A collection of constraints is called a Constraint Set (CSet). A CSet is a named, reusable collection of constraint values.

For more information on constraints, see the *Constraint Manager User Guide*.

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Defining Constraints in System Capture

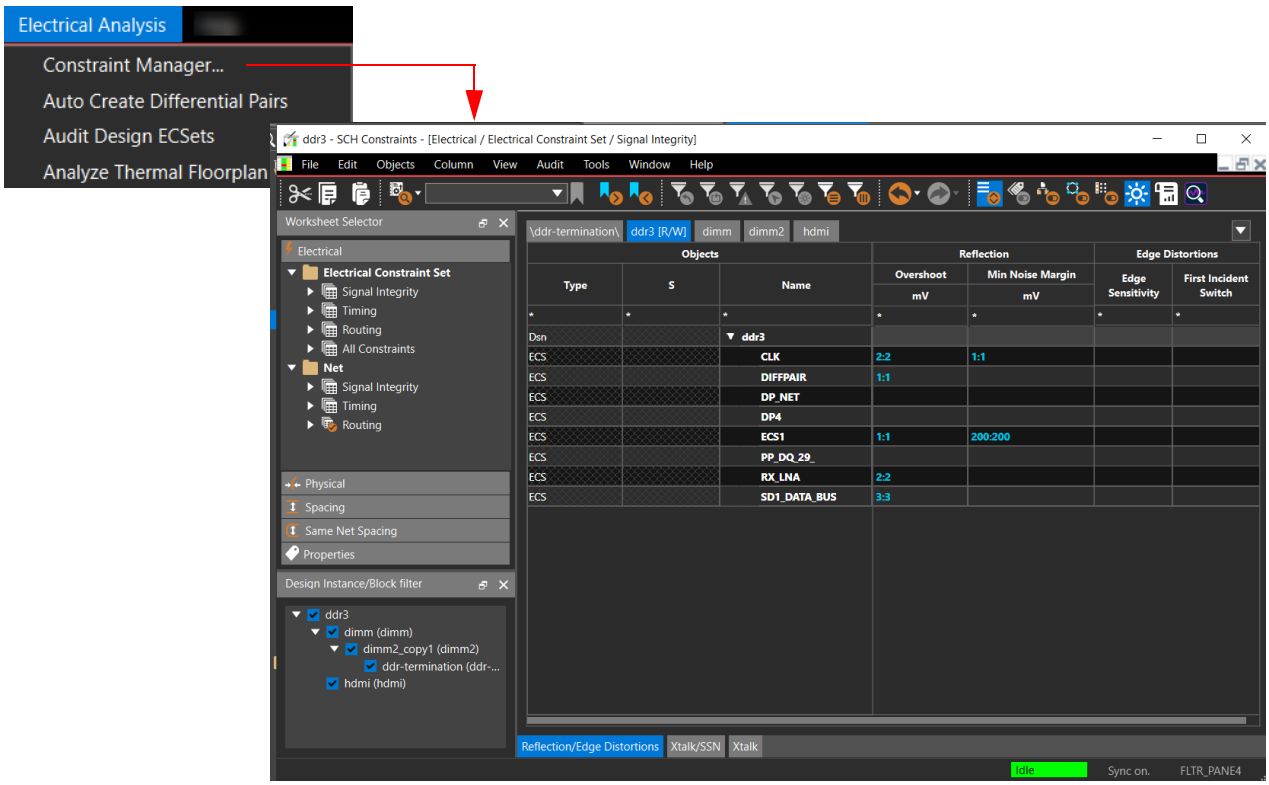
When creating a schematic design, only the electrical CSets are available. the physical and spacing constraints are set during layout.

Electrical constraints (ECs) govern the electrical behavior of a net or pin-pair in a design. For example, you can capture a constraint to define the maximum voltage overshoot tolerated by a net and capture the minimum first switch delay for a driver-receiver pin-pair in your design.

When creating a design schematic in System Capture, designers can add constraints in any of the following:

- Constraint Manager

  Capture and manage electrical constraints as you implement logic. Constraint Manager is integrated with System Capture. As a result, the changes made to constraints in Constraint Manager are displayed in System Capture, and the changes that you make to constraints in System Capture are displayed in Constraint Manager. Launch Constraint Manager from the *Electrical Analysis* menu.



- Properties Window

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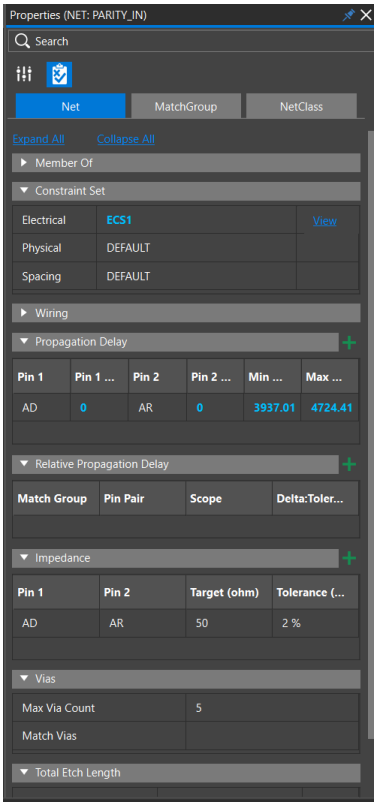
In addition, System Capture offers designers the ability to set up constraints at the net-level or DiffPair-level using the Properties window. The constraints tab is also called the Docked Constraint Manager.



The basic difference between working with Constraint Manager, the application, and the constraints in the *Property* window is the scope and the sequence. If the net elements are on the same page of the schematic, you can use the docked Constraint Manager, whereas if you are setting up constraints for nets and XNets that are not on the same page, you can use the spreadsheet-based Constraint Manager.

- Topology Workbench

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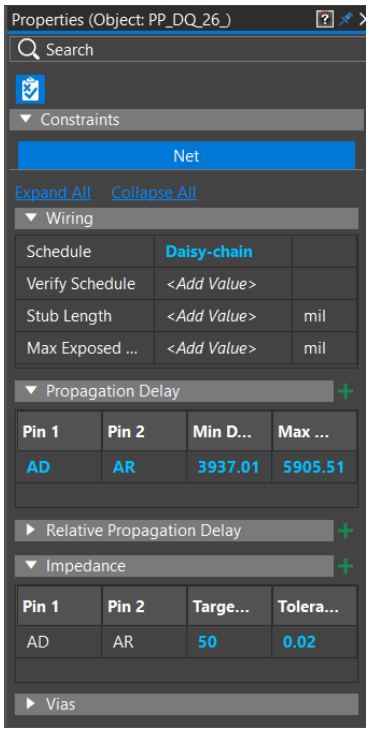
You can view the topology of a net in Topology Workbench, where you can derive constraint rules for the topology as an Electrical Constraint Set (ECSet) which applies to each net, and then update them in System Capture and Constraint Manager.



Regardless of where you set the constraints, they are immediately displayed in both the docked Constraint Manager panel in the Properties window as well as the Constraint Manager application.

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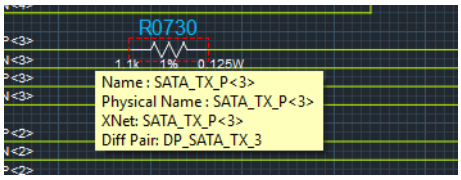
Creating an XNet

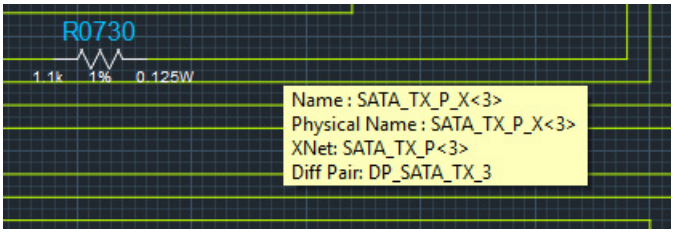
An XNet (eXtended net) is a connection between drivers and receivers. An XNet includes all the drivers and receivers connected to each other plus any discrete components that are connected to the XNet.

To create an XNet:

1. Go to any net.
2. Add a resistor component.
3. Place the resistor on the wire.
4. View the tooltip on the net that the XNet has been created.



5. You can check both sides of the resistor and notice that the same net name is there and the wire has a suffix `_x`, for example *`SATA_TX_P_X<4>`*.
6. View the tooltip of this net and observe that this is also part of the same XNet SATA_TX_P<3>.



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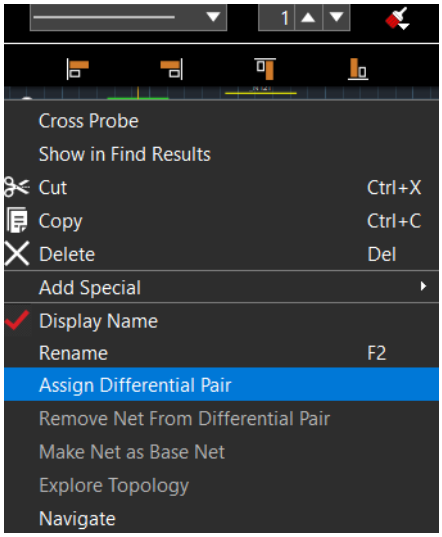
Creating Differential Pairs

A differential pair represents a pair of flat nets that are routed in a way such that the signals passing through them are opposite in sign with respect to the same reference. This ensures that any electromagnetic noise in the circuit is canceled out.

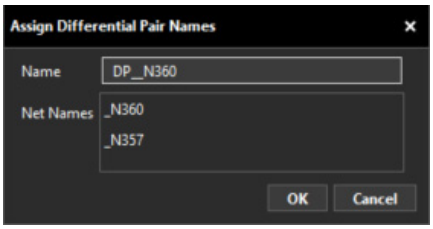
You can create differential pair signal using two scalar signals or two vector signals with same signal width. To create a differential pair:

1. Select two signals to be added as member nets of the differential pair on the canvas.
2. Right-click and choose *Assign Differential Pair*.



The *Assign Differential Pair Names* dialog box opens. The default name is shown.

3. Specify a new name, if needed.



4. Click *OK*.

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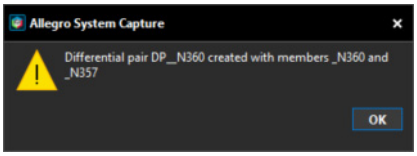
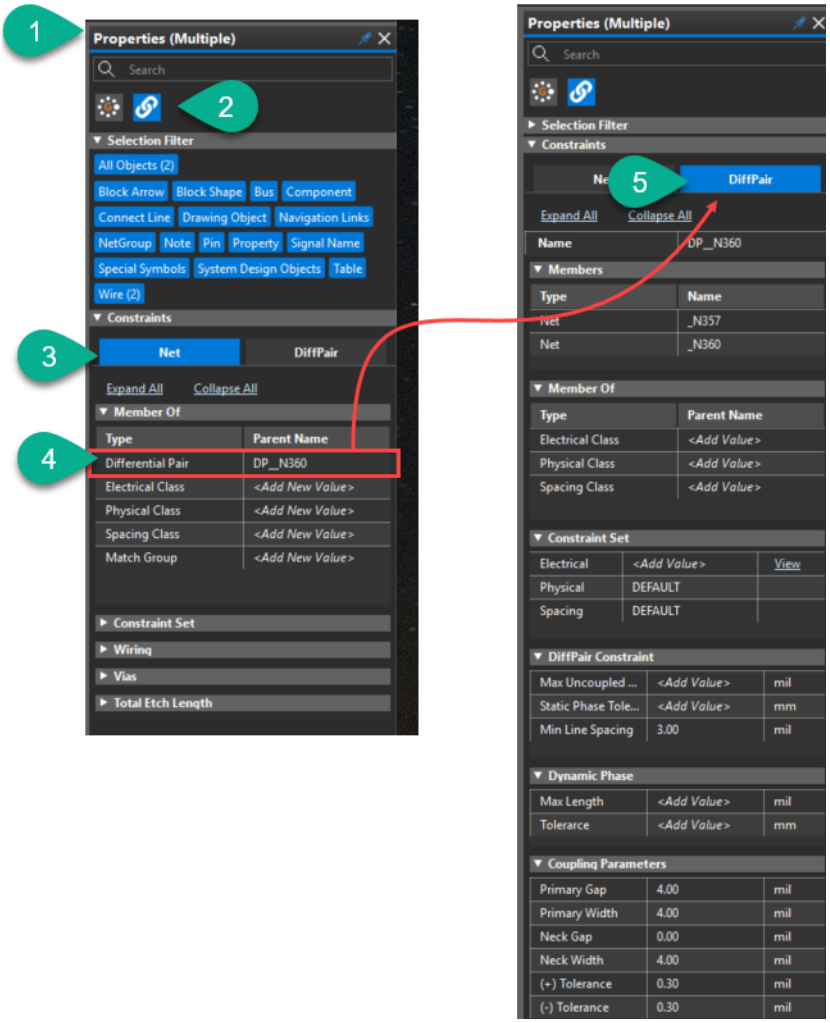
A confirmation message appears.



5. Click *OK*.

When the nets are added to a differential pair, the *Diff Pair* tab shows up in the *Constraints* tab of the *Properties* window.



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Tip

To create differential pair using a scalar net and one bit of a vector net, first display the individual bits of a bus, and then create a differential pair. To display the individual bits of a vector signal, right-click and choose *Draw Multiple Bits*.

Names for Differential Pair Signals

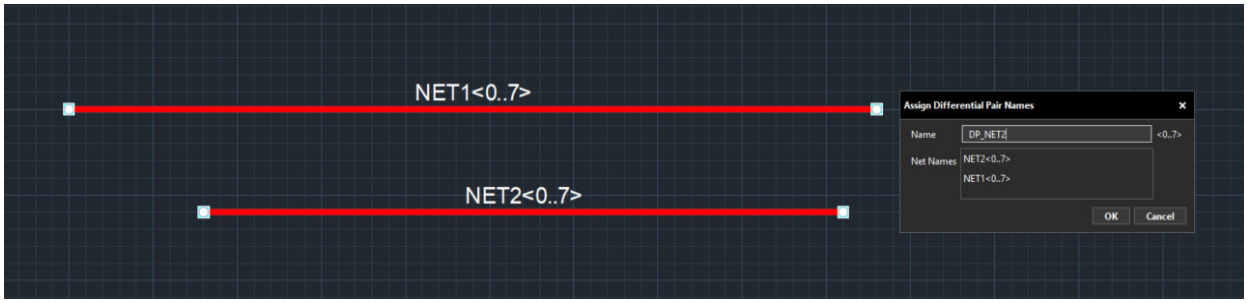
The differential pair name is generated by concatenating the prefix value specified in the Differential Pairs tab of the Setup dialog box and the common string (if any) in the member net names.

The convention used for naming differential pairs is `[prefix_specified_in_setup]<common_string_in_member_net_name>`. If prefix value is not specified in the setup, only the second part is used to name the differential pair signals.

Differential Pairs for Vectored Signals

System Capture supports creating differential pairs with two vector signals with same signal width. To create a differential pair from existing vectored signals:

1. Select the two vector nets.
2. Right-click and choose *Assign Differential Pair.*
3. Click *OK*.



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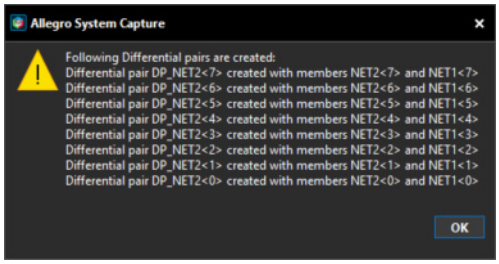
The confirmation message shows the differential pairs that are created.



Important

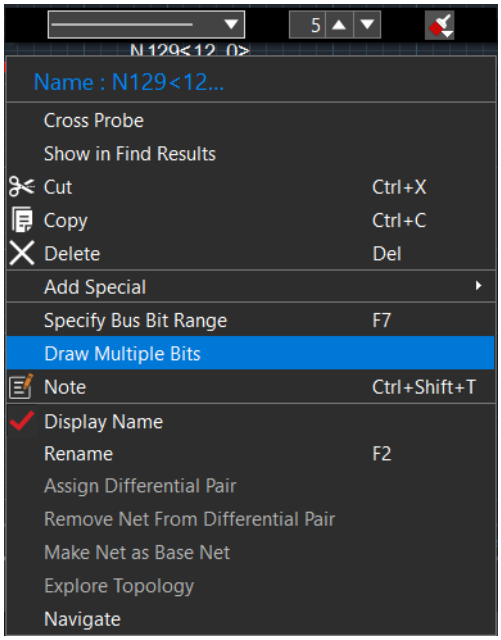
Note the bit numbers are matching in the pairs.

Differential Pairs for Bits of Vectored Signals

You can also create differential pairs of the individual bits of a vector net or two different vector nets.

1. Display the individual bits of the vector bus.

   a. Right-click the vector net and choose *Draw Multiple Bits*.



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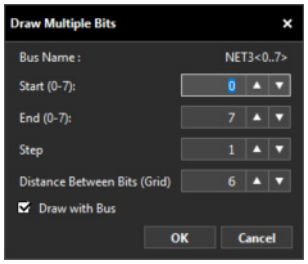
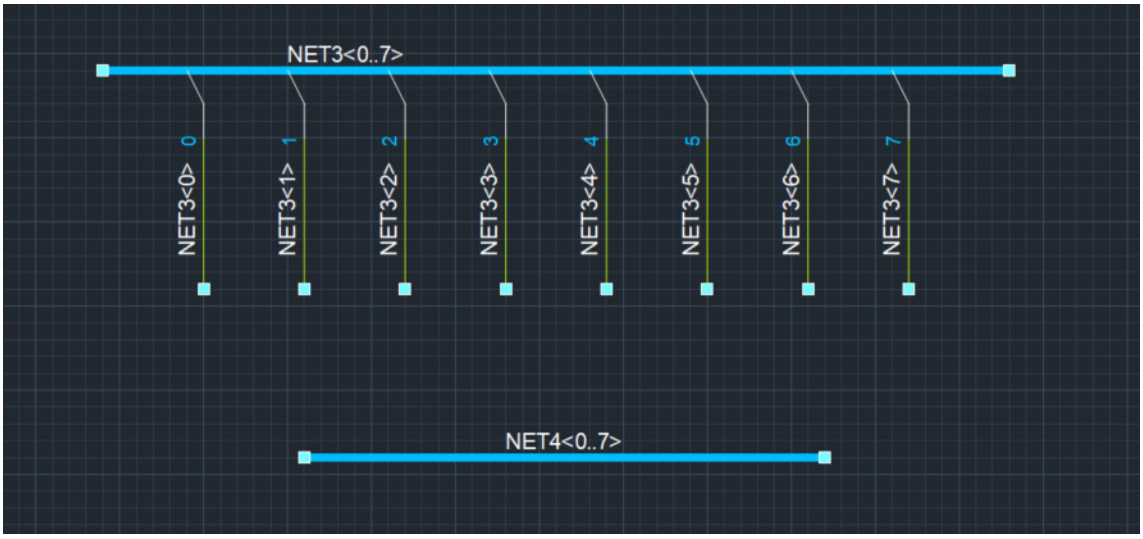
The *Draw Multiple Bits* dialog box appears.



b. Click *OK*.

The bus with individual bits is attached to the cursor. Place it where needed.



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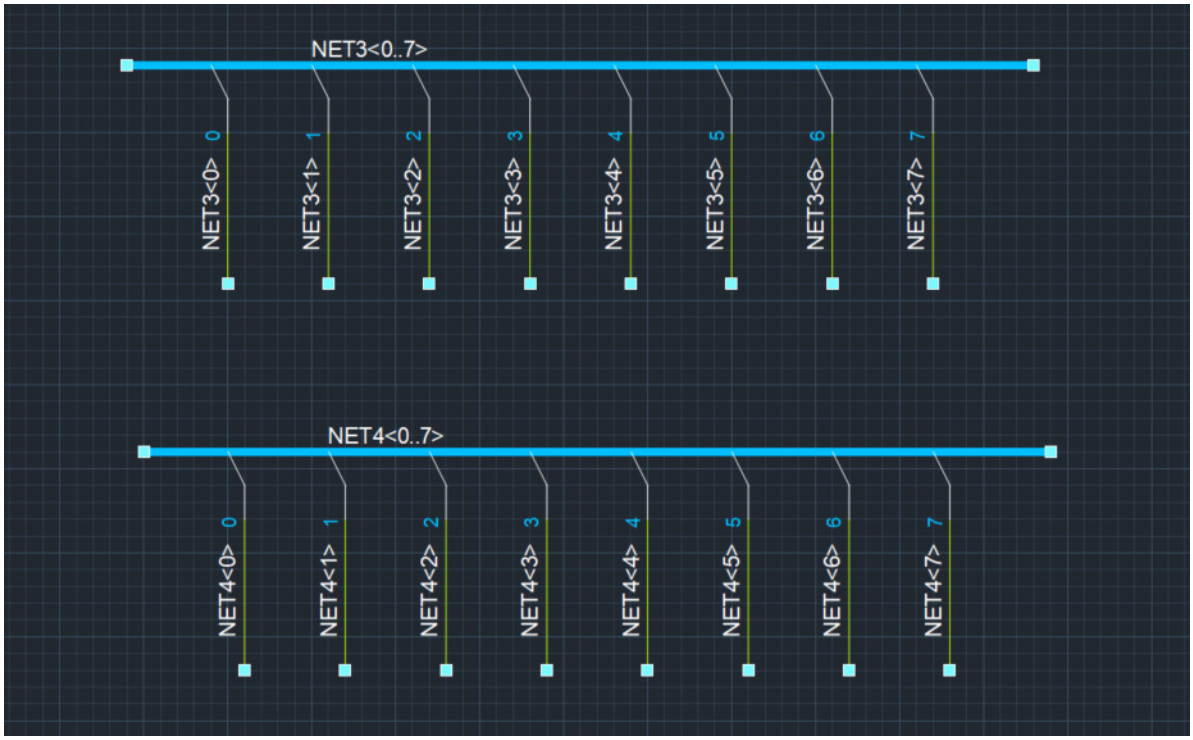
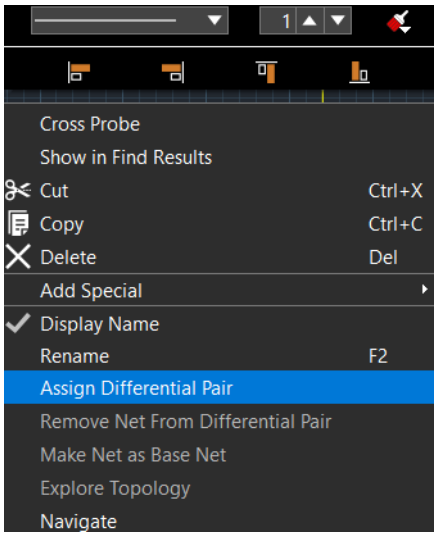
2. Repeat this for the second vector bus.



3. Select one bit from both the vector signal bits.
4. Right-click and choose *Assign Differential Pair*.



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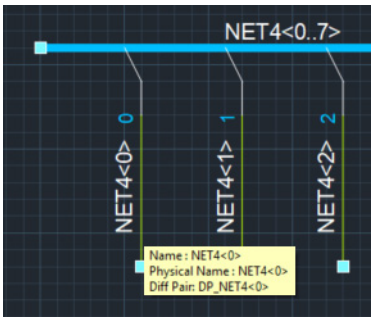
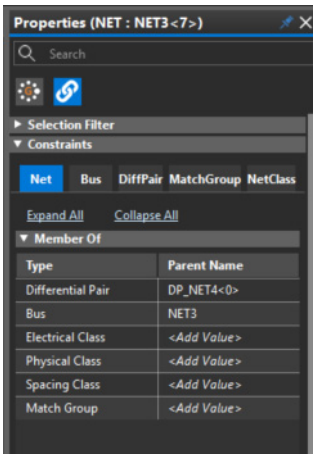
5. Change the differential pair name if needed.

6. Click *OK*.

   The diff pair information is visible in the *Properties* window and also in the tool tip if you hover the mouse cursor over the bit.





Renaming Differential Pairs

In System Capture, you can rename the logical as well as the physical name of a differential pair signal. To change the name of a differential pair signal, perform the following steps.

1. Select any member of a differential pair, such as a bit, vector net, or scalar net.
2. Open the *Properties* window.
3. Open the *Constraints* - *Diff Pair* tab

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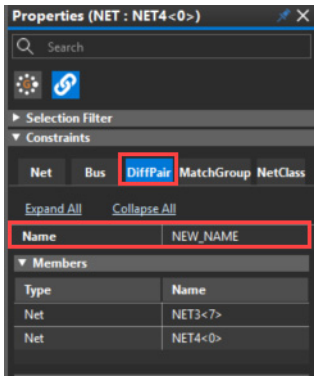
4. In the *Name* field, type in the new name.

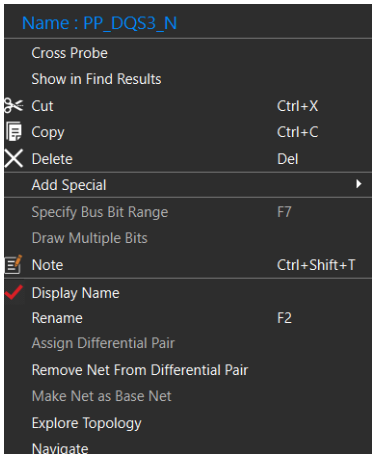


This changed name gets updated in all locations immediately.

Deleting Differential Pairs

When you remove a signal from a differential pair, the other signal is also removed and the differential pair gets deleted. To remove a signal or delete a differential pair:

1. Right-click any member signal of a Differential Pair, such as a scalar net, vector net, or bit of a vector net and choose *Remove Net from Differential Pair*.



A message confirms that the differential Pair has been deleted.

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Automatic Differential Pairs Creation

The naming convention for nets that form a Differential Pair often follow a pre-defined pattern. Looking at the name of the net name, you can guess if it is part of a differential pair, and whether it is the Inverting or Non-inverting leg of the differential pair: Here are some commonly used patterns for naming nets of a differential pairs:

Suffix	_P	_N
Suffix	P	N
Suffix	_L	_H
Suffix	+	-
Prefix	+	-

In System Capture, you can define the patterns to be used to identify nets for forming a differential pair in a configuration file. This configuration file is stored in the SITE area.

The common text in the net names is used for naming a differential pair. A prefix in the differential pair name can also be defined in the configuration file, which is added to the differential pair name.

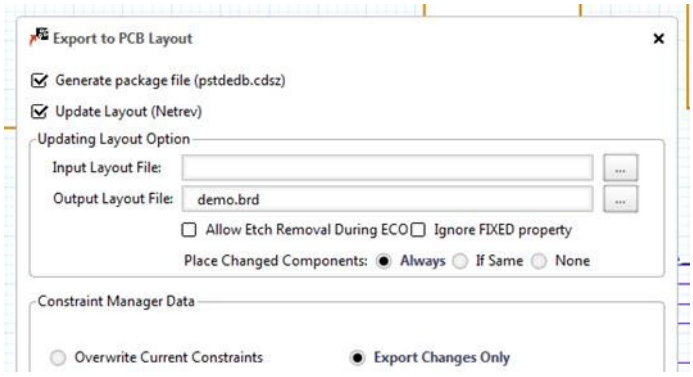
For example, in <CDS_SITE>/cdssetup/canvas/resources/syscap:

- `utils.tcl`

  Contains the required Tcl commands.

- `acm_config.txt`

  Contains the setup instructions for differential pairs.



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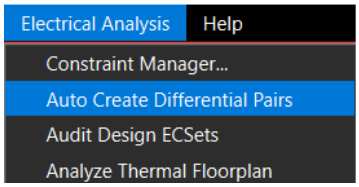
➡ To create differential pairs based on names, use the *Electrical Analysis – Auto Create Differential Pair* command.



Or

Enter the `cnsAutoCreateDiffPair` command in the *Command* window.

The return value of this function is displayed. A value of 0 indicates that there is no error. The tool also generates a report of the operation and it is stored in the design folder as `autoDPCreationReport.txt`.

autoDPCreationReport.txt

```
Constraint Automation Report

=========================================================================
Updating Differential Pairs based upon Nets in the Design. Force mode(1)

Processing nets which contain ".*[0-9]+P" and suffix "P" with nets which contain
".*[0-9]+N" and suffix "N"...

Processing nets which contain ".*_P.*" and suffix "_P" with nets which contain ".*_N.*
and suffix "_N"...
  Using existing DP_SATA_RX_5 for members SATA_RX_P<5> and SATA_RX_N<5>
  Using existing DP_SATA_RX_4 for members SATA_RX_P<4> and SATA_RX_N<4>
  Using existing DP_SATA_RX_3 for members SATA_RX_P<3> and SATA_RX_N<3>
  Using existing DP_SATA_RX_2 for members SATA_RX_P<2> and SATA_RX_N<2>
  Using existing DP_SATA_RX_1 for members SATA_RX_P<1> and SATA_RX_N<1>
  Using existing DP_SATA_RX_0 for members SATA_RX_P<0> and SATA_RX_N<0>
  Using existing DP_SATA_TX_5 for members SATA_TX_P<5> and SATA_TX_N<5>
  Using existing DP_SATA_TX_4 for members SATA_TX_P<4> and SATA_TX_N<4>
  Using existing DP_SATA_TX_3 for members SATA_TX_P<3> and SATA_TX_N<3>
  Using existing DP_SATA_TX_2 for members SATA_TX_P<2> and SATA_TX_N<2>
  Using existing DP_SATA_TX_1 for members SATA_TX_P<1> and SATA_TX_N<1>
  Using existing DP_SATA_TX_0 for members SATA_TX_P<0> and SATA_TX_N<0>

Processing nets which contain ".*[0-9]+P" and suffix "P" with nets which contain
```

To confirm that the nets are now part of a differential pair, check the tooltip displayed on a net. In the following image, the differential pair name comprises a prefix of DP_ and the common

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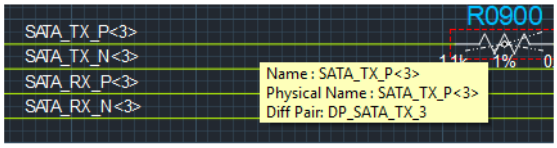
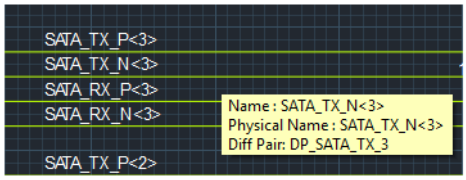
part of the net names making the rest of the name. The same differential pair name is visible on the Inverting as well as the non-Inverting leg of the differential pair.





Related Topics

cnsAutoCreateDiffPair

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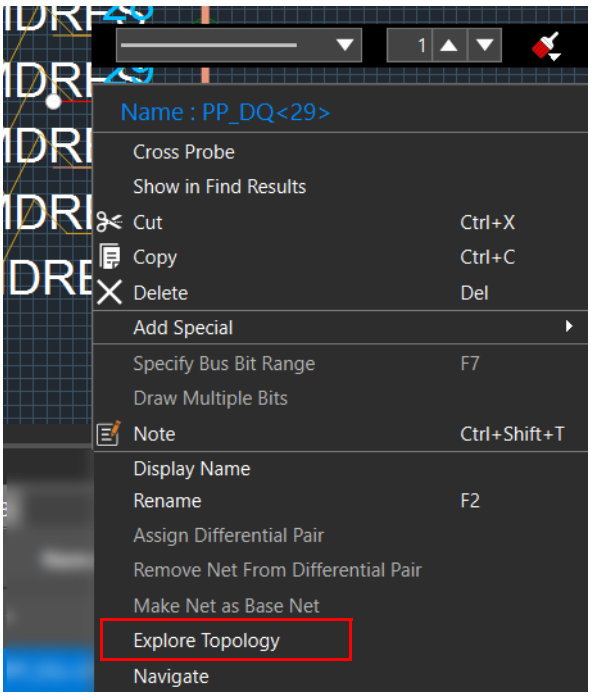
Extracting Topology in Topology Workbench

You can extract the net objects in a design and view their topology in Allegro Topology Workbench.

To extract a topology of a net, follow these steps:

1. Right-click a net and choose *Explore Topology*.



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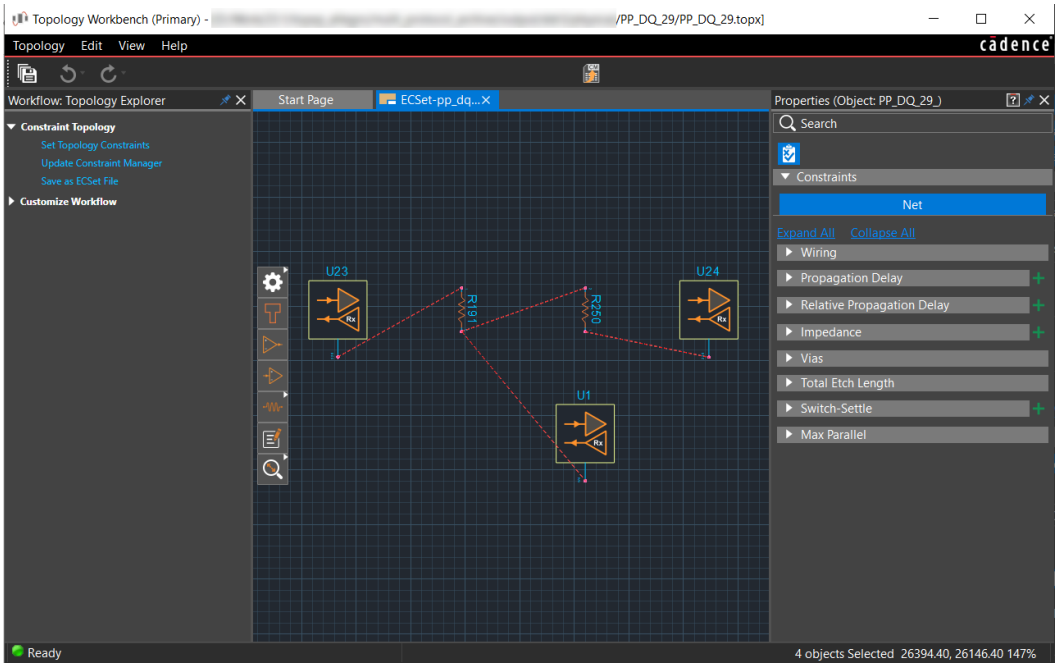
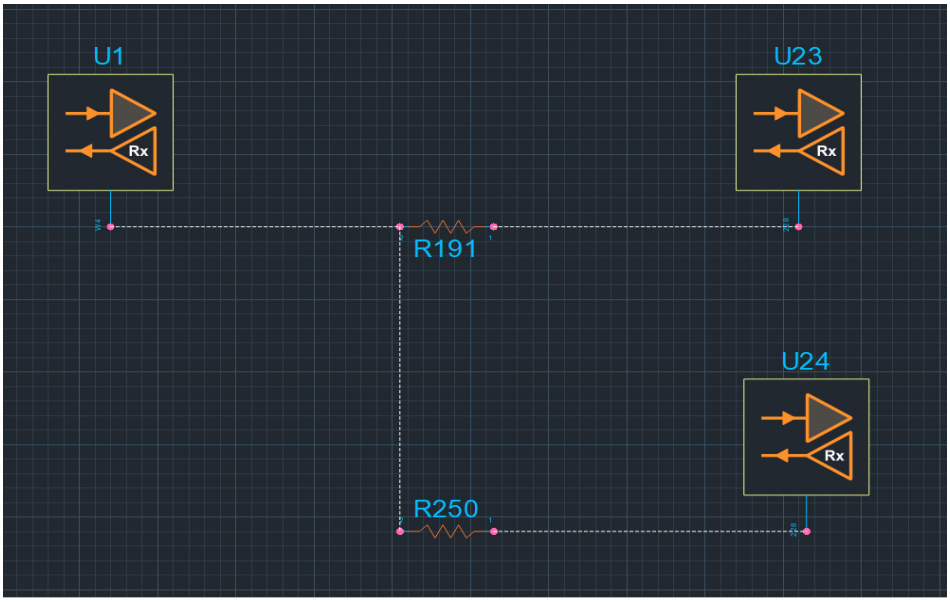
Topology Workbench opens.



The ECset view of the net is displayed with ratsnest-based connectivity.

2. Rearrange the topology as shown in the following image.



3. Select one of the segments.

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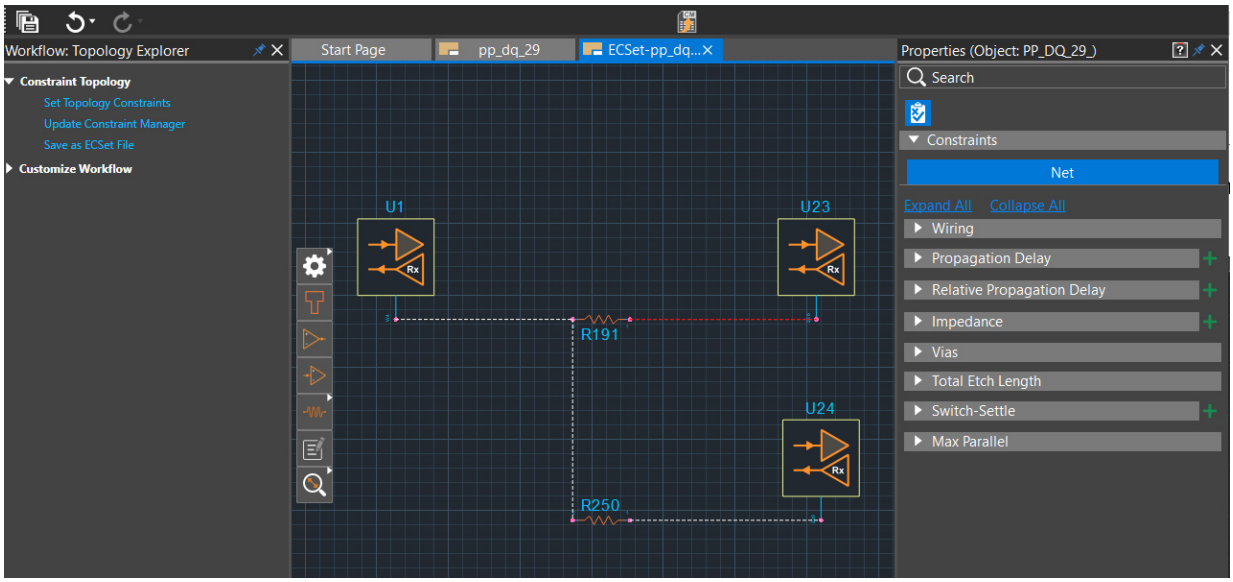
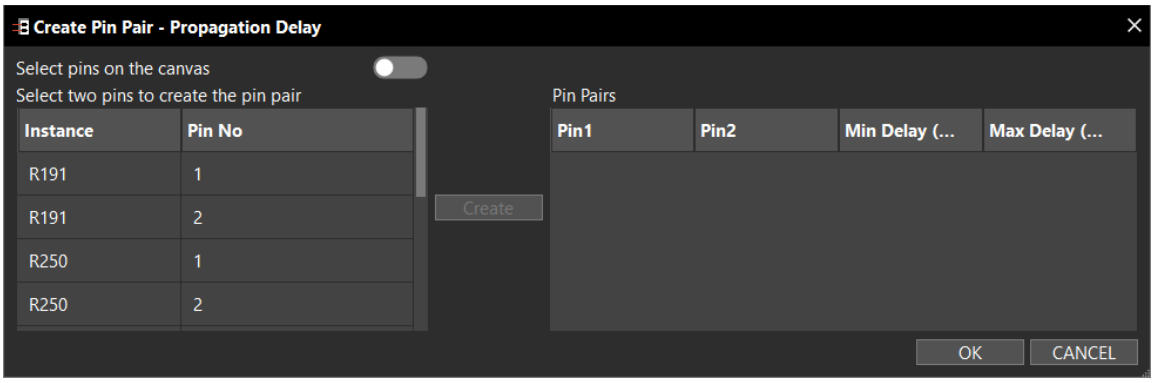
The *Properties* panel displays on the right and the constraints are visible.



4. Select the + icon next to *Propagation Delay* tab.

The *Create Pin Pair-Propagation Delay* window opens.



5. Scroll to the end of the pins list.

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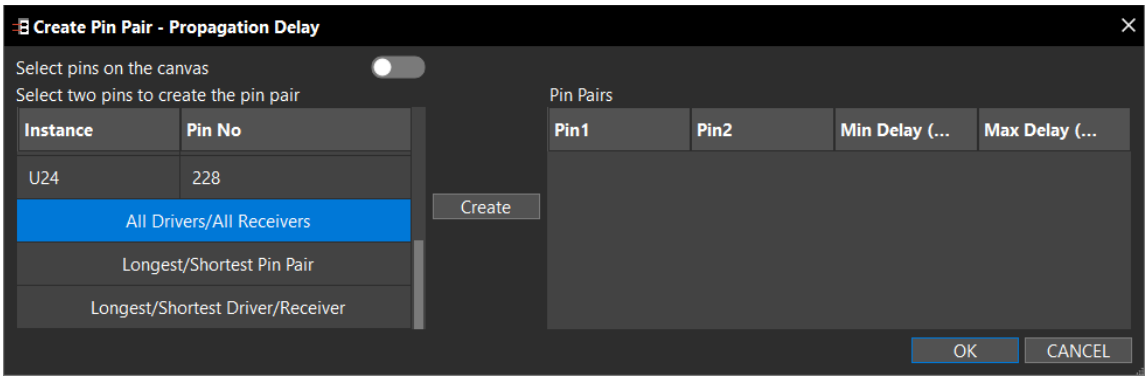
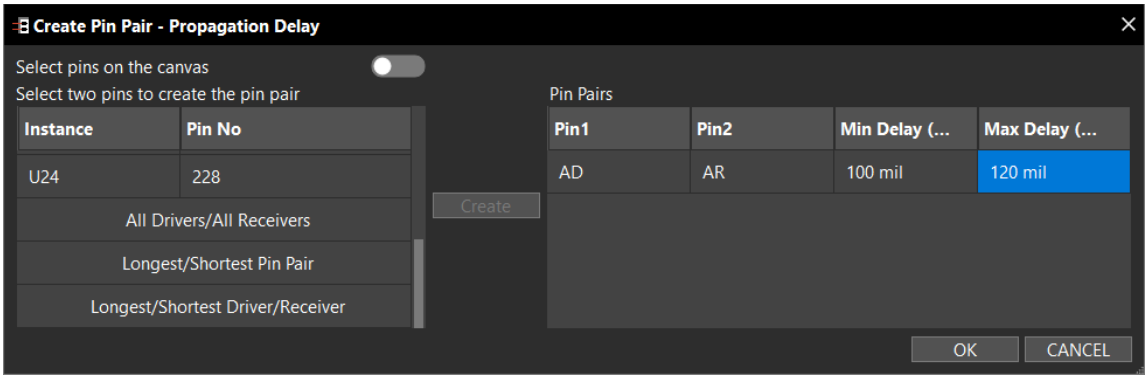
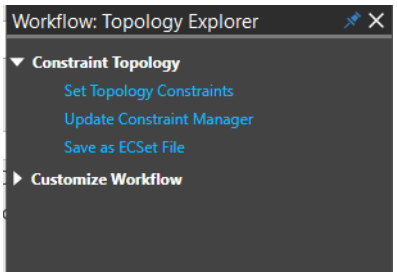
6. Select *All drivers and All receivers*.



7. Click *Create*.
8. Define the *Min Delay* as 100 and *Max Value* as 120.



9. Click *OK*.
10. Save the topology.
11. Click *Update Constraint Manager* in the *Workflow* panel.



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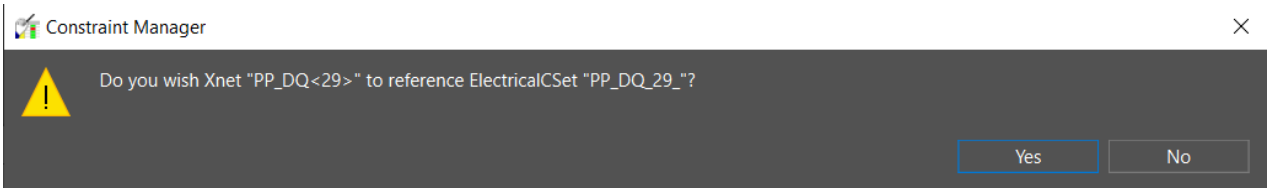
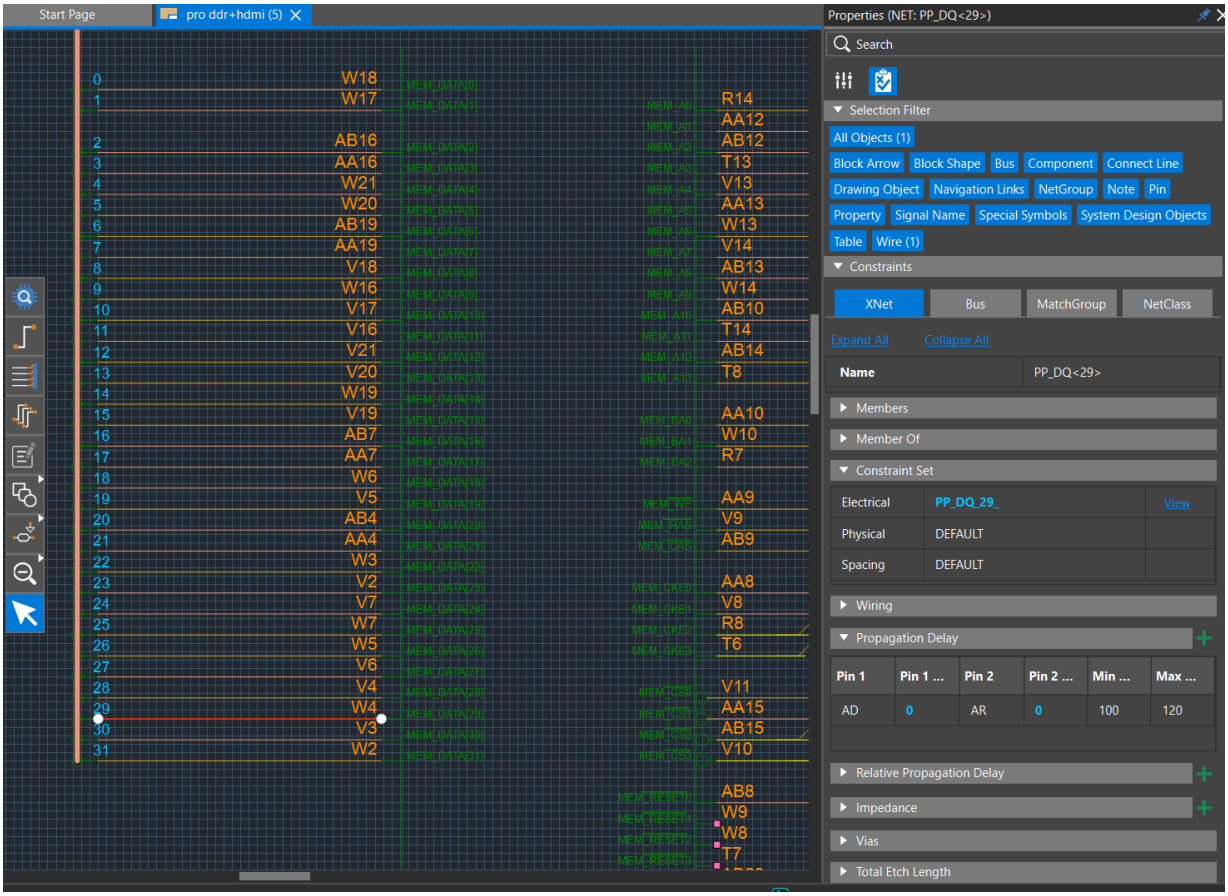
Constraint Manager asks for confirmation.



12. Click *Yes*.
13. Close Topology Workbench.
14. Select the net in System Capture.
15. Open docked Constraint Manager.
16. Expand Constraints.
17. Expand Propagation Delay.



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Observe the following:

- An ECSet has been created with the same name as the net.
- Propagation delay values that were specified in Topology Workbench are applied.

Changes in constraints can also be made in Constraint Manager and they are immediately applied in System Capture.

Related Topics

- Allegro Constraint Manager Reference
- Topology Workbench User Guide
- Exporting Constraints from a Topology

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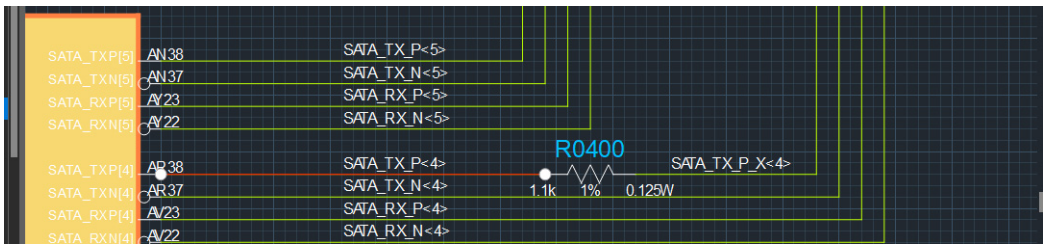
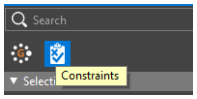
Setting Constraints in Docked Constraint Manager

To define constraints in Docked Constraint Manager:

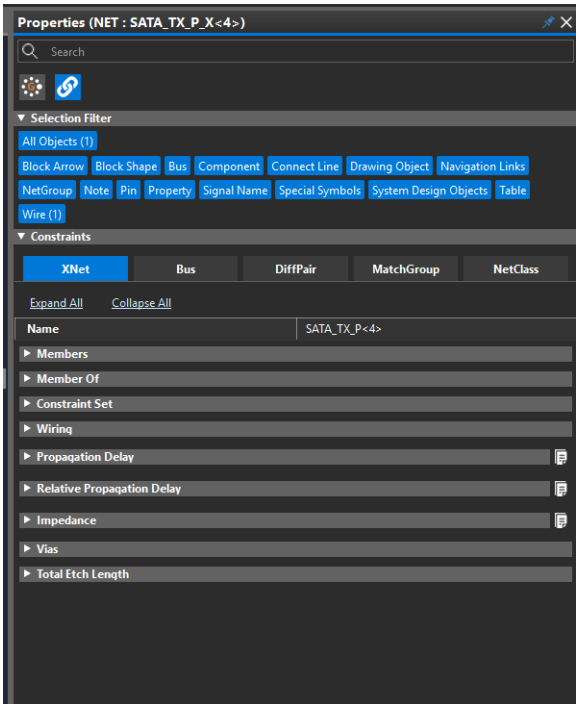
1. Select an XNet.



2. In the *Properties* window, click the *Constraints* icon.



The Constraints information is displayed. By default the nodes are collapsed and the information for the selected XNet is displayed as tabs.



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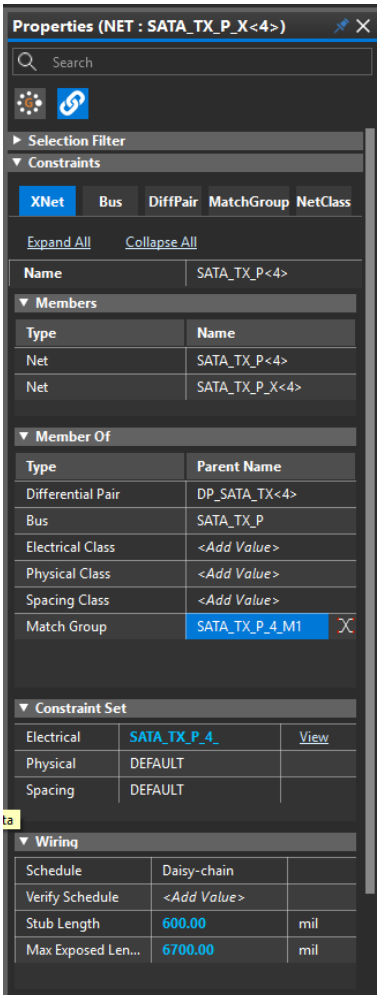
You can view the members of the XNet along with the Buses, Classes, and Match Groups to which this XNet belongs. The applied Constraint Sets are visible in the *Constraint Set* section.

All the constraints that are available on the XNet by the application of the ECSet are displayed. Observe that these values are the same as specified in Topology Workbench.

The Bus and DiffPair tabs show when the selected net is a part of a bus or Diff Pair. The MatchGroup and NetClass tabs gets populated when there are changes made in Constriant Manager or SigXplorer.

3. Click *Expand All* in the *XNet* tab.



Here you can see a summary of the XNet in the *Member Of* node and the types of constraints applied. In this image, the XNet is a part of a:

- Differential Pair called *DP_SATA_TX_4*

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- Bus called *SATA_TX_P*
- Electrical constraint *SATA_TX_P_4* is applied to this net.

From the *XNet* tab of the *Properties* panel, you can define the following types of electrical constraints:

- Wiring
- Propagation Delay
- Relative Propagation Delay
- Impedance
- Vias
- Total Etch Length

From the *Diff Pair* tab of the *Properties* panel, you can define the following types of electrical constraints to the XNet:

- DiffPair Constraint
- Dynamic Phase
- Coupling Parameters

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Assigning Wiring Constraints

Wiring constraints define topology scheduling parameters, physical (*Stub Length*) and electromagnetic interference (EMI) (*Max Exposed Length*) rules.

Use the *Wiring* schema in the *Properties (Object :<Obj_Name>)* panel to create and modify topology scheduling parameters and the available physical and EMI rules. These rules apply to the topology as a whole. They are not associated with specific topology elements.

To set a wiring constraint for a connection:

1. Expand the *Wiring* node.

   A table with the available constraint properties is displayed with editable fields.

Important

The unit is `mil` in docked Constraint Manager by default. If you open the Constraint Manager spreadsheet editor, you will notice that the unit is `ns` there and also changes in the docked constraint manager. This change remains only for the session.

2. Specify the *Schedule.*

   Select one of the pre-defined schedules for the ECSet from the drop-down list.

   - Minimum Spanning Tree: Connects all of the pins together with minimum connection length. Any pin can connect to any number of other pins. This schedule starts at the primary driver, selects the closest pin to this driver, and connects it through a TLine. The search continues by selecting the next unscheduled pin that is closest to any of the scheduled pins and connecting it with a TLine to the closest scheduled pin. This continues until all pins are scheduled.

   - Daisychain: Connects the pins of the topology with minimum connection length, allowing each pin to connect to a maximum of two other pins. This schedule starts with the primary driver, selects the closest pin to this driver, and connects it with a TLine. The closest pin to the last pin scheduled is then selected and connected with a TLine. This continues until all of the pins are scheduled.

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- Source-load Daisy-chain: Connects similar to a daisy chain schedule except that all driver pins are scheduled first, followed by all receiver pins.
- Star: Connects the driver pins in a daisy-chain pattern, then all of the receiver pins are connected to the last driver pin.
- Far-end Cluster: Connects similar to a star schedule except that the last driver pin connects to a T-point, to which all of the receivers are connected.
- (Clear): No specified schedule

3. Select the *Verify Schedule* value.

Verify Schedule is used to enable design rule checks (DRC) if a schedule has been set. Select one of the following from the drop-down list:

Yes	Enables DRC.
No	Disables DRC.
Clear	No specified DRC.

4. Enter the *Stub Length* for daisy chain routing.

The daisy chain routing connects the pins of the topology with minimum connection length, allowing each pin to connect to a maximum of two other pins.

5. Enter the *Max Exposed Length*.

This constraint property specifies the maximum length of interconnect allowed in a net that is not shielded by plane layers above and below.

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Setting the Propagation Delay Constraint

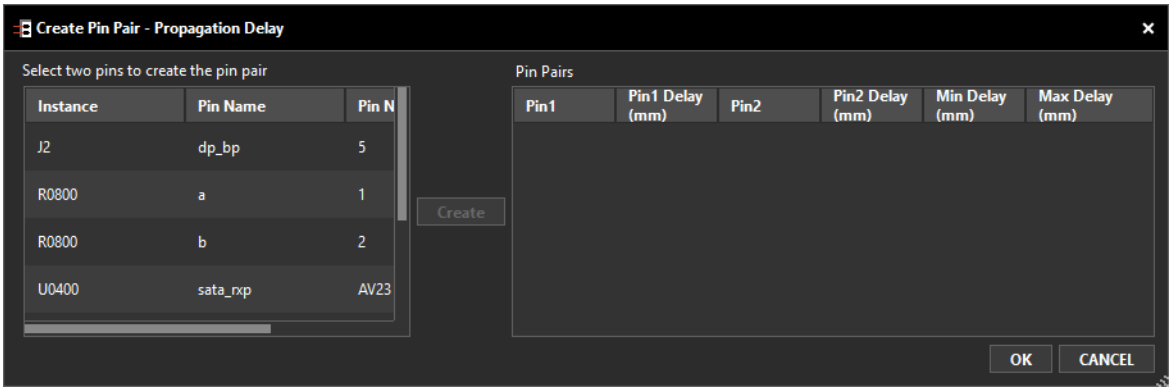
Propagation delay defines the minimum and maximum delay in time or connection length restriction between any two pins on a net or between any pin and a T-point.

With the *Propagation Delay* constraint, you can create and modify delay rules for pin, tee or pin-tee pairs. You can also create delay rules for all drivers and receivers, all driver and receiver pairs, and the longest and shortest Tlines.

To set a *Propagation Delay* constraint for a connection, in the *Properties (Object: <Obj_Name>)* panel:

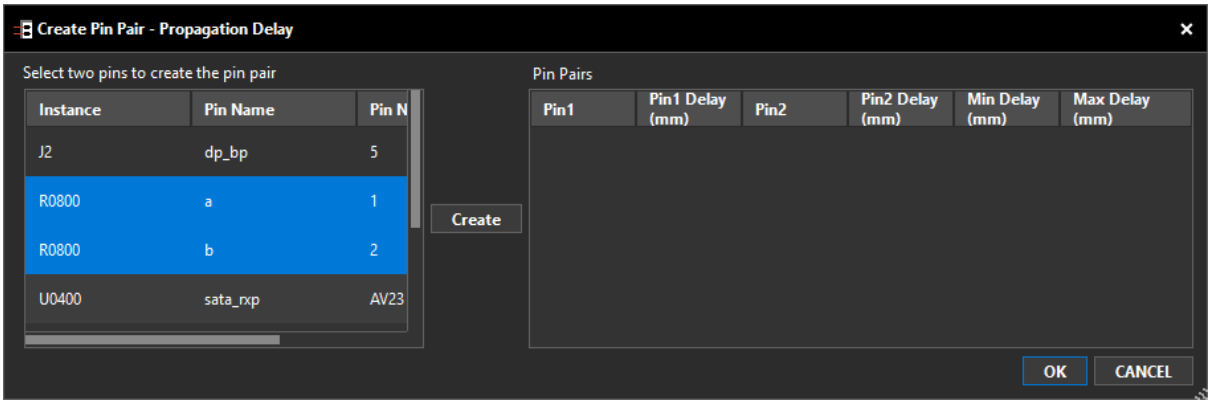
1. Click the button next to *Propagation Delay*.

   The *Create Pin Pair - Propagation Delay* dialog box opens.



2. Select two pins from the list in the left pane while keeping the `Ctrl` key pressed.

   The *Create* button is enabled.



3. Click *Create*.

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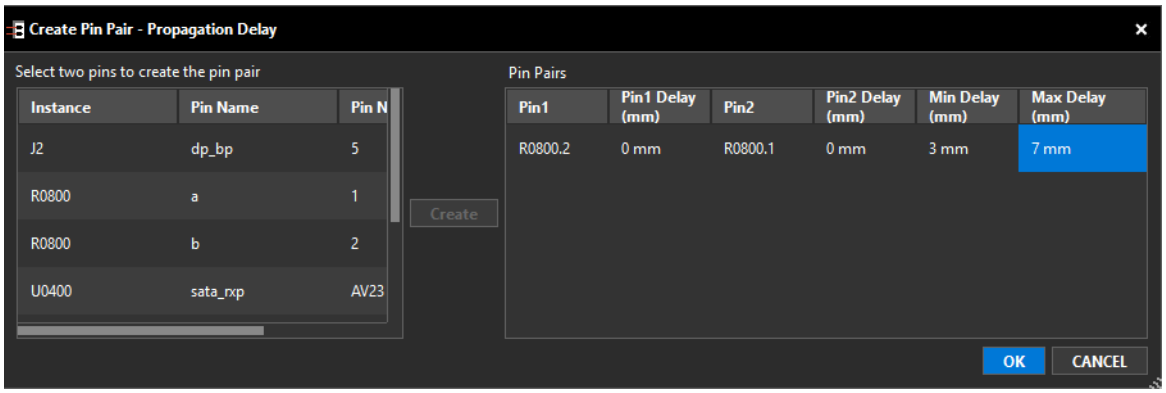
A row of the selected pin pair is added to the *Pin Pairs* pane on right.

4. Add the *Min Delay* and *Max Delay* values in the corresponding cells of the table.

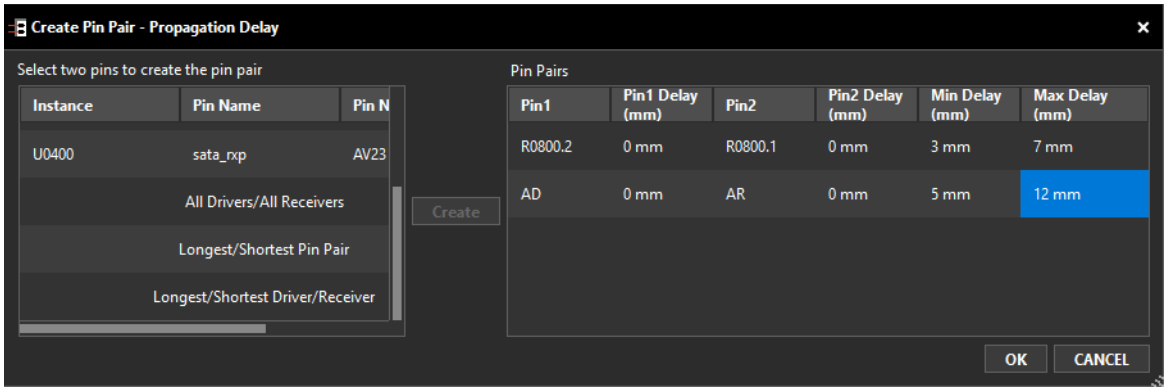


5. Create one of the following global constraints:

- ❑ *All Drivers/All Receivers*
- ❑ *Longest/Shortest Pin Pair*
- ❑ *Longest/Shortest Driver/Receiver*

Note: When you click either of these global constraints in the left pane, the *Create* button is enabled provided you have not already set another global constraint.

6. Define the *Min Delay* and *Max Delay* for the global constraint in the *Pin Pairs* table.



7. Click *OK*.

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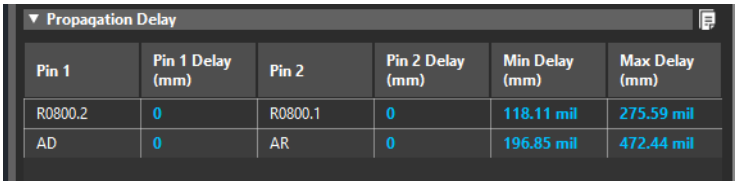
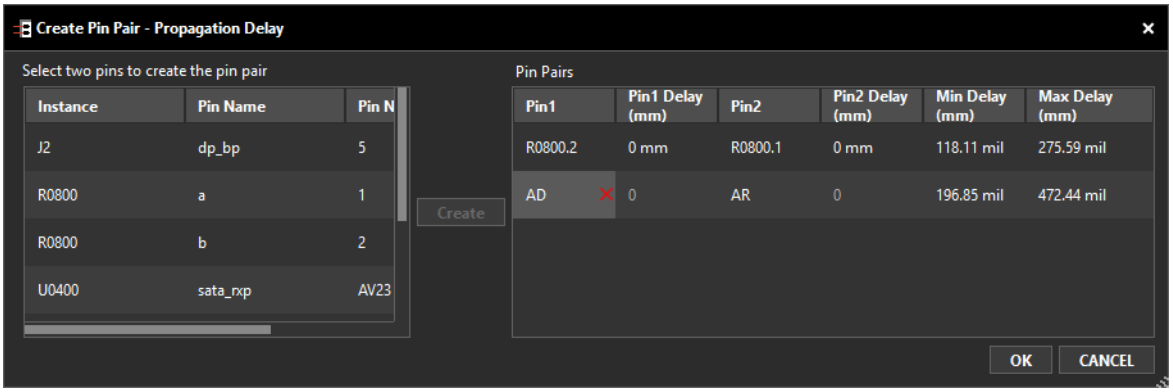
The table in the *Propagation Delay* node shows the changes made.



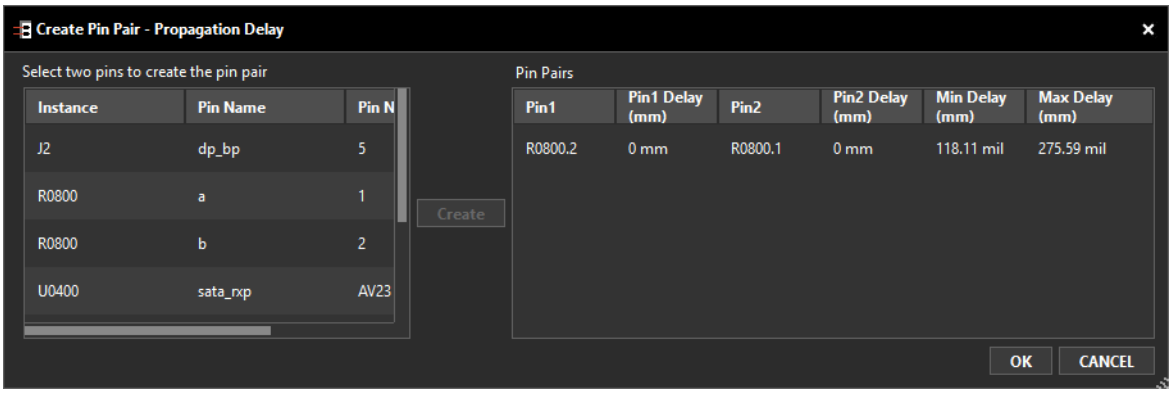
Deleting a Propagation Delay Constraint

If you want to remove a defined constraint:

1. Click the button adjacent to the *Propagation Delay* schema to open the *Create Pin Pair - Propagation Delay* dialog box.
2. Under the *Pin1* or *Pin2* column, place the pointer on a cell that represents the constraint you want to delete. A cross (*X*) symbol is displayed.



3. Click the cross (*X*) to delete the constraint. The *Pin Pairs* table is refreshed.



4. Click *OK*.

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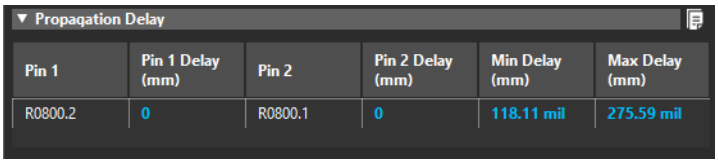
The *Propagation Delay* table is updated.



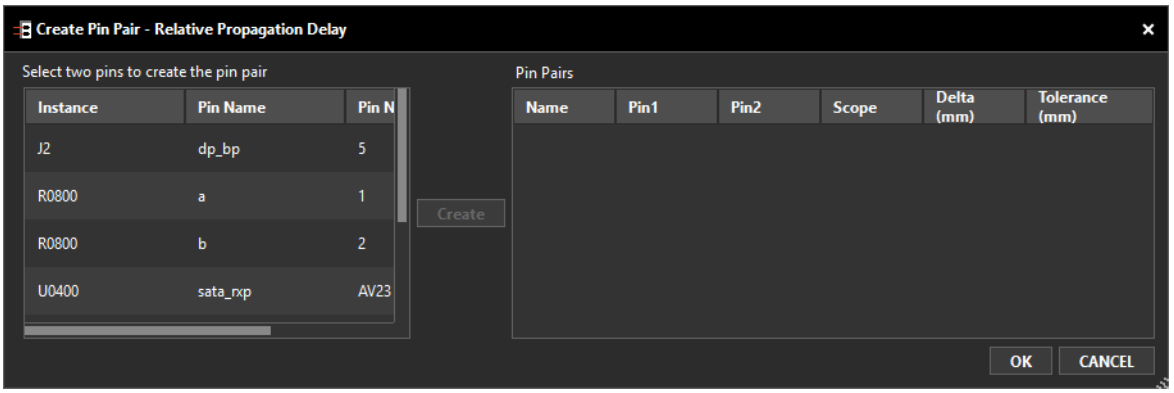
Assigning Relative Propagation Delay Constraints

Relative propagation delay defines connections that are part of a match group. You can specify relative propagation delays between nets and within a net, as well.

Use the *Relative Propagation Delay* constraint to assign matched interconnect delay constraint rules to pin, tee or pin-tee pairs. A matched delay constraint is two or more pin, tee or pin-tee pairs whose interconnect delay must be within a specified tolerance. You can assign matched delay rules to a single pair or to groups of pairs. To set a *Relative Propagation Delay* constraint for a connection, in the *Properties (Object: <Obj_Name>)* panel:

1. Click the button next to *Relative Propagation Delay*.

   The *Create Pin Pair - Relative Propagation Delay* dialog box opens.



2. Select two pins from the list in the left pane while keeping the `Ctrl` key pressed.

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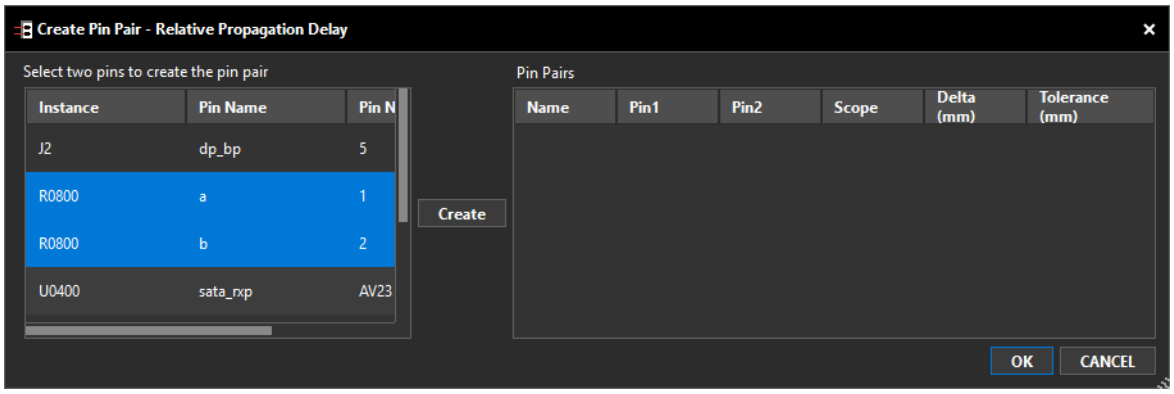
The *Create* button is enabled.



3. Click *Create*.

A row of the selected pin pair is added to the *Pin Pairs* pane on the right.

4. Modify the default *Name* (reference designators) for pins and T-points in the topology, if required.

Note: A default unique name of the format *<topology_name>_M<n>* is automatically assigned to each pin pair.

5. Select the *Scope* of the pin pair to control how the members of the Group are validated.

You can choose one from the list of following values that are displayed when a cell is clicked under the *Scope* column:

Local — Creates a single match group. Checking is done only between the two pin pairs of each net, and limited to within the net.

Example: Multiple nets with a single driver, two receivers, and a branch point where the length from the driver to each receiver must match, but no matching is needed to other nets.

Global — Creates a single match group, derived from net properties or an electrical constraint set (ECSet). The same match group can exist in multiple ECSets or properties, resulting in all objects ending up in the same match group. For hierarchical designs, use of the Global Scope in lower blocks creates a single merged match group at the top level.

Example: Multiple nets containing pin pairs that must match to each other across each net.

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Bus Creates match groups based on bus names (such as MG1_BUS1, MG1_BUS2, and so on). You can apply a single ECSet to all the nets at either the net or bus level. This group type reduces the number of ECSets required to constrain a design, as opposed to requiring a separate ECSet for each bus. A limitation of this scope type is that no other signals from outside the bus can be added to these match groups.

Example: Multiple nets organized in several buses. Pin pairs must match, but only to nets within the same bus. Typically, all nets share the same topology.

Class Generates unique match groups for each class. Similar to Bus scope, Class scope also optimizes the number of topologies required to constraint a design. However, no other signal from outside the net class can be added to a match group with Class scope. Class scope has more flexibility than Bus scope because a class can include more signals than a bus, which is typically limited to vectored nets or nets that share a common topology. Unlike the Bus scope, the Class scope adds all the selected members, including bus members, to the match group created by the ECSet (with Class scope).

Example: When you need the functionality of a Bus scope and also need additional non-bus members in a match group, use the Class scope.

Net Group Generates unique match groups for each net group.

6. Specify the *Delta* value. It defines the allowable propagation delay/length delta for pin, tee or pin-tee pairs of the group. The delta is used to offset the pair(s) from a target pair.

7. Specify the *Tolerance* value for relaxing the relative/match requirements.

   The default format for specifying a *Tolerance* is percentage. If you want to define an absolute tolerance, a value with the unit of measurement can be entered. For example, you can enter `0.1ns` in the *Tolerance* field.

8. Create one of the following global constraints:

   - *All Drivers/All Receivers*
   - *Longest Pin Pair*
   - *Longest Driver/Receiver*

   Note: When you click either of these global constraints in the left pane, the *Create*

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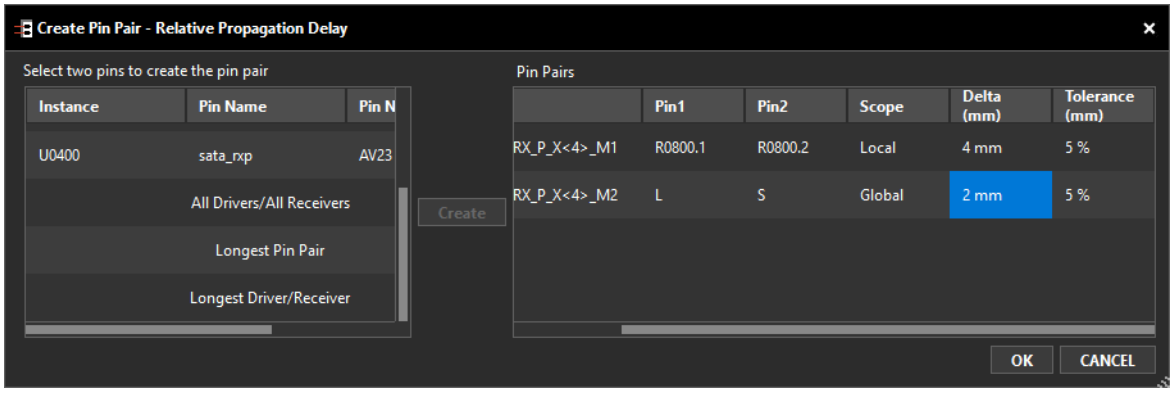
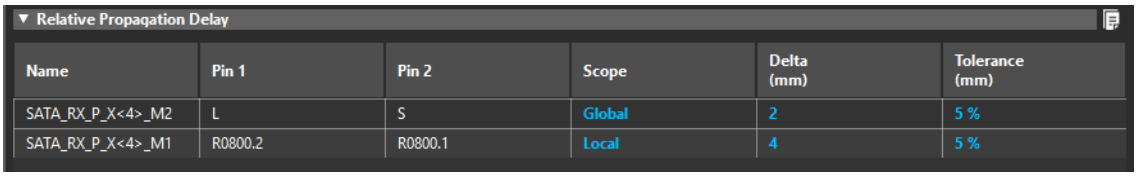
button is enabled provided you have not already set another global constraint.

9. Define the *Scope*, *Delta*, and *Tolerance* for the global constraint in the *Pin Pairs* table.



10. Click *OK*.

The *Relative Propagation Delay* schema table is refreshed.



Deleting a Relative Propagation Delay Constraint

To remove a defined constraint:

1. Click the button next to *Relative Propagation Delay.*

The *Create Pin Pair - Relative Propagation Delay* dialog box opens.

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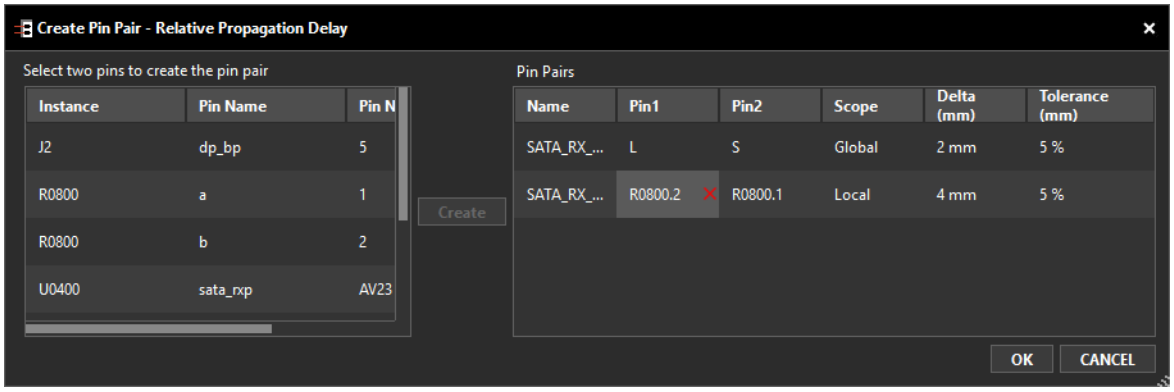
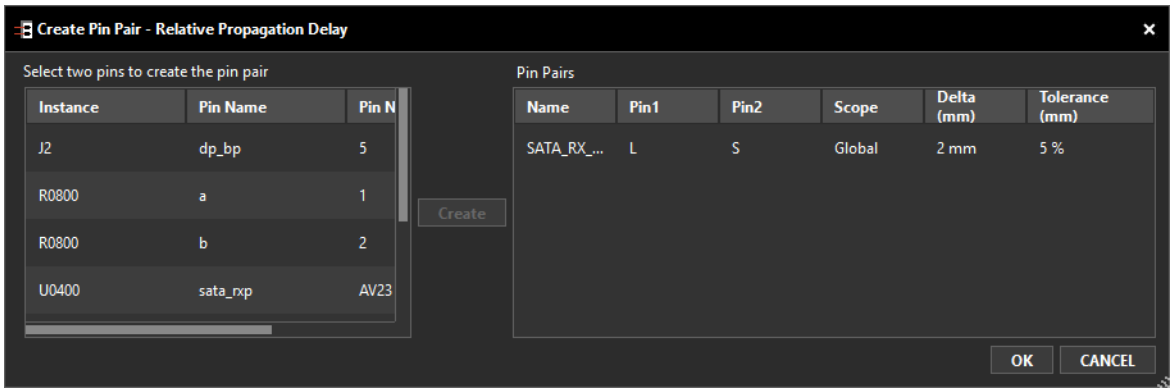
2. Under the *Pin1* or *Pin2* column, place the pointer on a cell that represents the constraint you want to delete. A cross (*X*) symbol is displayed.

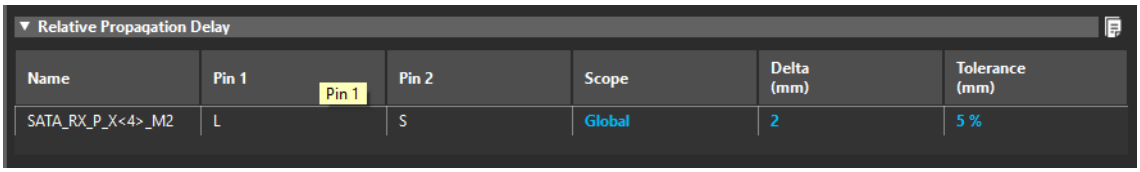


3. Click the cross (*X*) to delete the constraint. The *Pin Pairs* table is refreshed.



4. Click *OK*.

   The *Propagation Delay* table is updated.



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Assigning Impedance Constraints

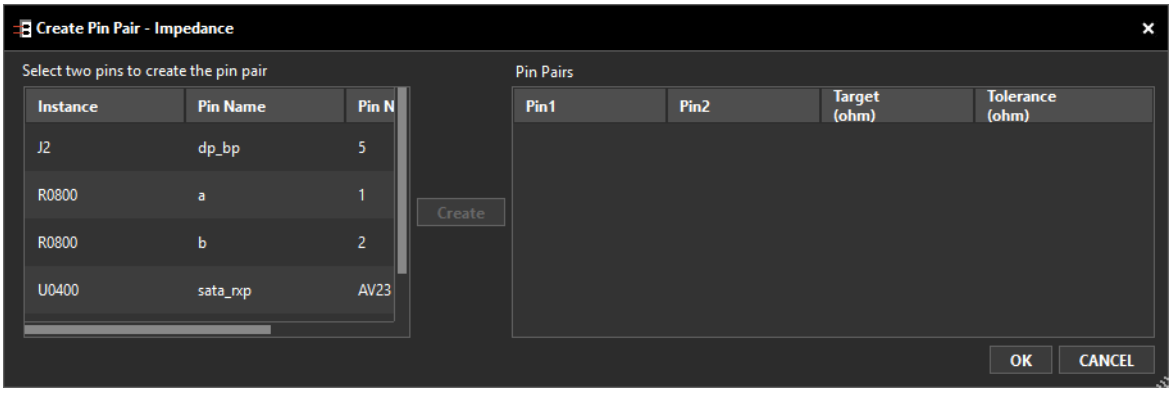
Impedance constraints define the baseline impedance value and tolerance values allowed above and below the baseline. An impedance constraint compares the impedance of each cline segment of an extended net.

You can create and modify *Impedance* constraint for pin, tee, or pin-tee pairs. You can also create delay rules that apply to all pin, tee, or pin-tee pairs in the topology. The *Impedance* constraint specifies a baseline impedance value and an allowed delta value above and below the baseline.

To set an *Impedance* constraint for a connection:

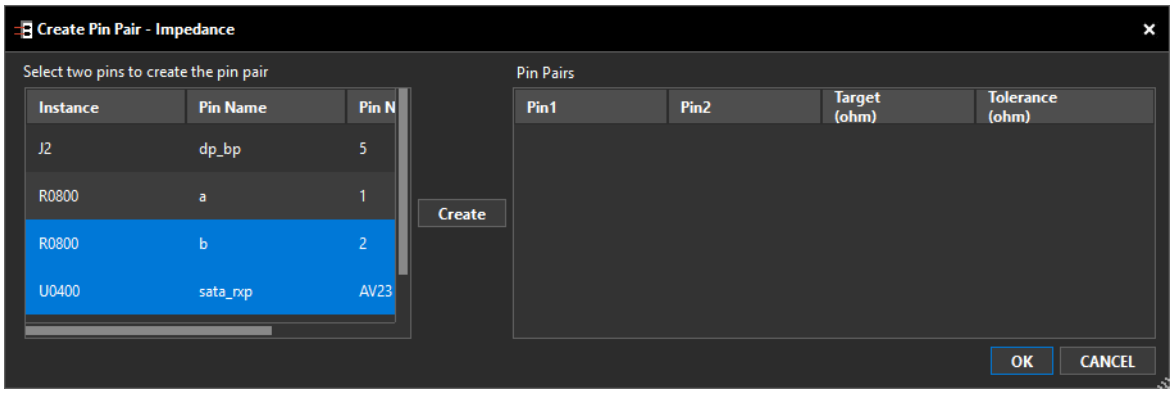
1. Click the button next to *Impedance*.

   The *Create Pin Pair - Impedance* dialog box opens.



2. Select two pins from the list in the left pane while keeping the `Ctrl` key pressed.

   The *Create* button is enabled.



3. Click *Create*.

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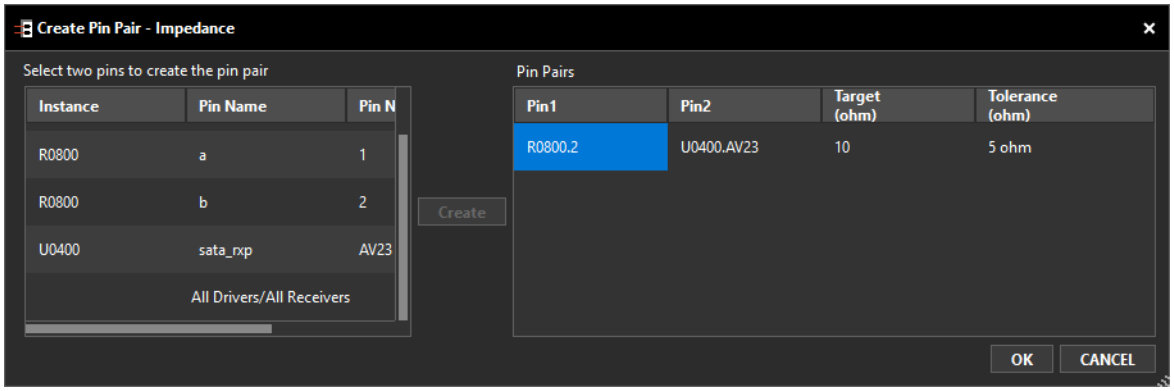
A row of the selected pin pair is added to the *Pin Pair* pane on right.

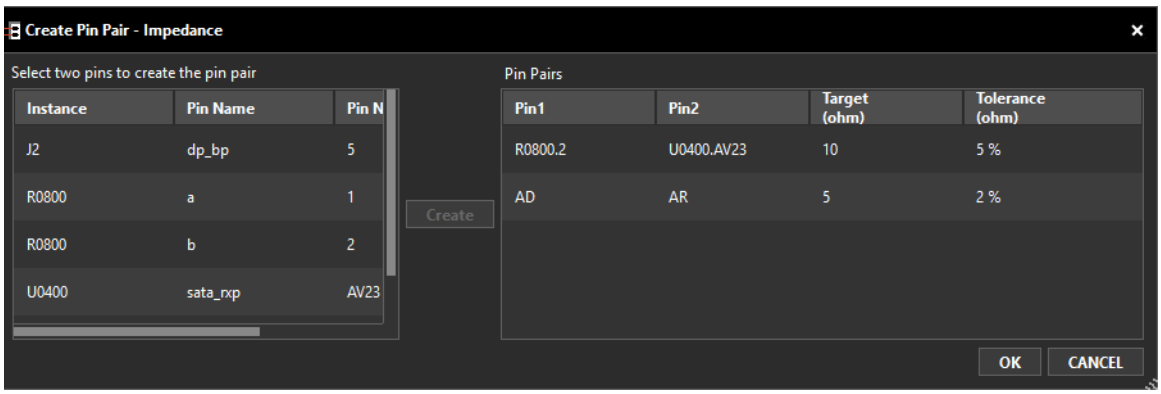
4. Specify the impedance *Target* value. When you add the *Target* value, a default *Tolerance* percentage appears in the corresponding cell.

5. Specify the impedance *Tolerance* value. Enter a delta value above and below the baseline impedance as a percentage.



6. Create a *All Drivers/All Receivers* global constraint.

7. Define the impedance *Target* and *Tolerance* for the global constraint in the *Pin Pairs* table.



The default format for specifying a *Tolerance* is percentage. If you want to define an absolute tolerance, a value with the unit of measurement can be entered. For example, you can enter `0.1ns` in the *Tolerance* field.

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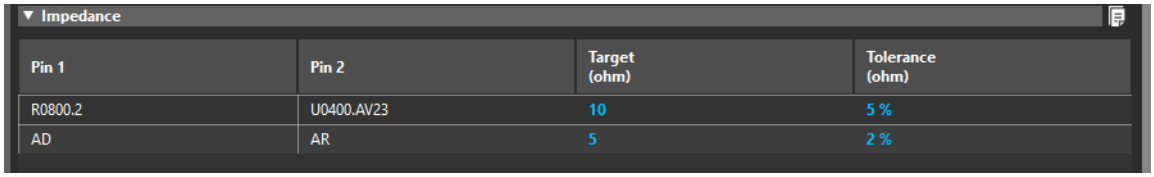
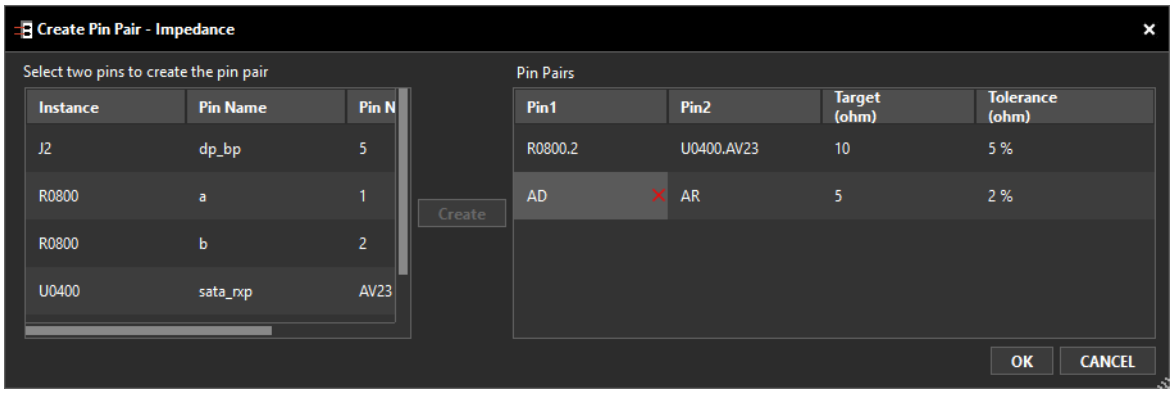
8. Click *OK* to save the changes you have made and close the dialog box. The table in the *Relative Propagation Delay* schema is refreshed with the newly set or updated constraint values.



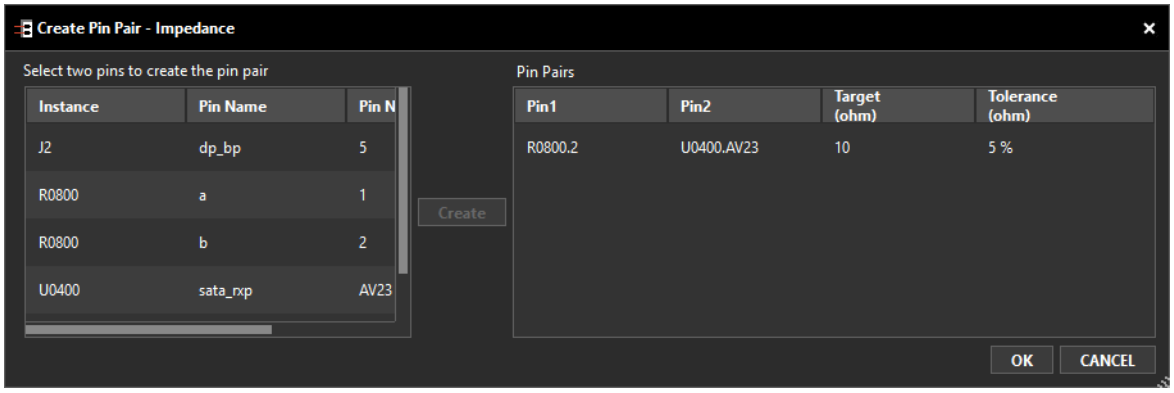
Deleting an Impedance Constraint

If you want to remove a defined constraint, open the

1. Click the button next to *Impedance* to open the *Create Pin Pair - Impedance* dialog box.
2. Under the *Pin1* or *Pin2* column, place the pointer on a cell that represents the constraint you want to delete. A cross (*X*) symbol is displayed.



3. Click the cross (*X*) to delete the constraint. The *Pin Pairs* table is refreshed.



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4. Click *OK* to save the change and close the dialog box.

   The *Impedance* table is updated.

Pin 1	Pin 2	Target (ohm)	Tolerance (ohm)
R0800.2	U0400.AV23	10	5 %

Assigning Vias Constraints

Via constraints define the physical constraint Max Via Count.

To set the *Vias* constraint for a connection:

1. Click *Vias* in the *Constraints* tab of the *Properties* window.

   A table with the available constraint property is displayed with an editable field to add a value.

Vias	
Max Via Count	*<Add Value>*
Match Vias	

2. Enter the *Max Via Count* to specify the maximum number of vias allowed in a net.

Vias	
Max Via Count	15
Match Vias	

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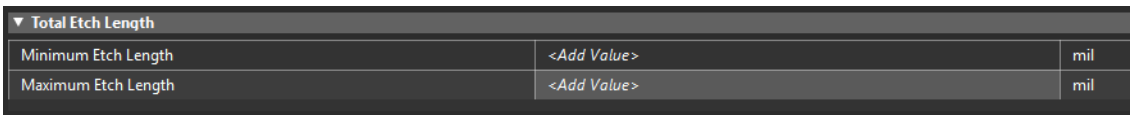
Assigning Total Etch Length Constraints

Total etch length defines the physical constraints *Minimum Etch Length* and *Maximum Etch Length*.

To set the *Total Etch Length* constraint for a connection:

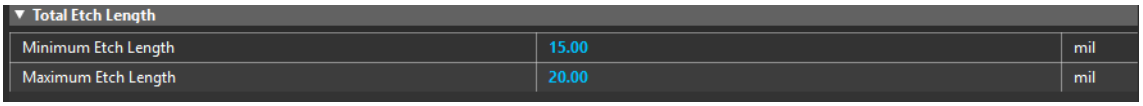
1. Expand the *Total Etch Length* node.

   A table with the available constraint property is displayed with an editable field to add a value.



Total Etch Length		
Minimum Etch Length	<Add Value>	mil
Maximum Etch Length	<Add Value>	mil

2. Enter the *Minimum Etch Length*.
3. Enter the *Maximum Etch Length*.



Total Etch Length		
Minimum Etch Length	15.00	mil
Maximum Etch Length	20.00	mil

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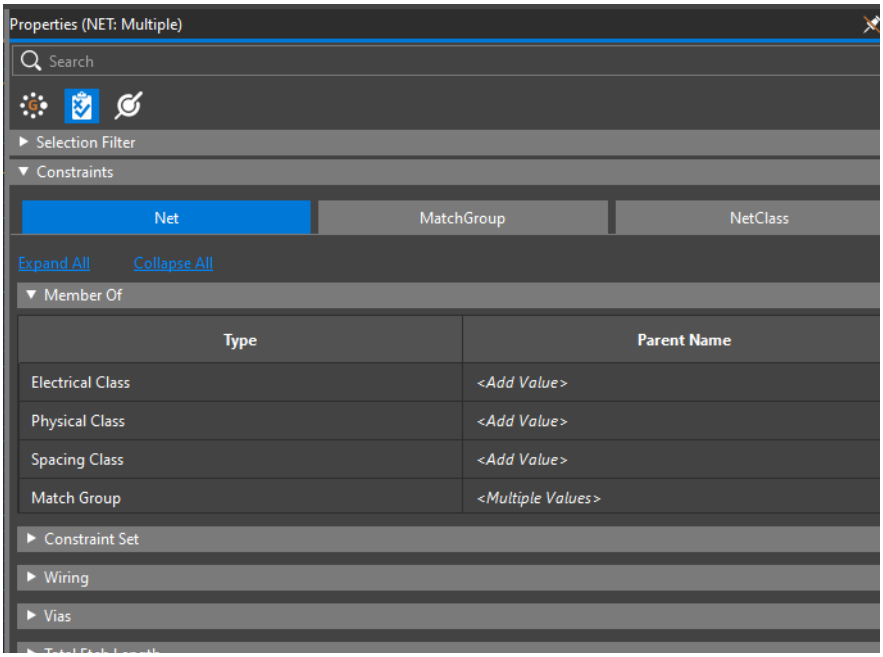
Adding Nets to a Match Group

A Match Group is a collection of nets, Xnets, or pin pairs that must all match (in delay or length) or be relative to a specific target within the group. Match Groups are resolved down to specific pin pairs. To add multiple nets to a Match Group:

1. Select the nets on the canvas.
2. Open the *Constraints* tab in the *Properties* window.



3. Specify a Match Group name in the *Member Of* panel.

   The *MatchGroup* tab appears.

4. Open the *MatchGroup* tab.

   A Match Group is a collection of nets, XNets, or pin pairs which must all match (in delay or length) or be relative to a specific target within the group.

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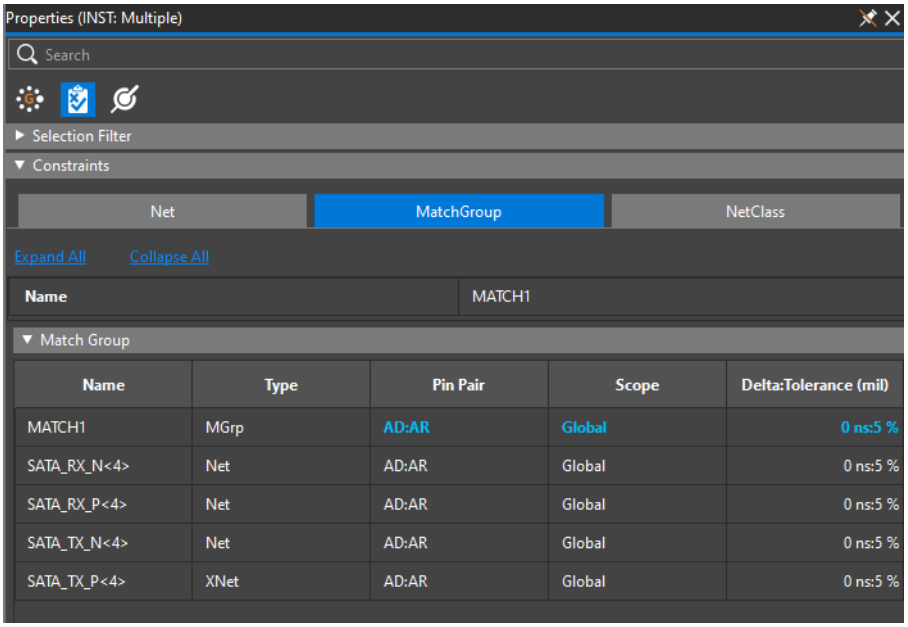
5. Make the changes needed.



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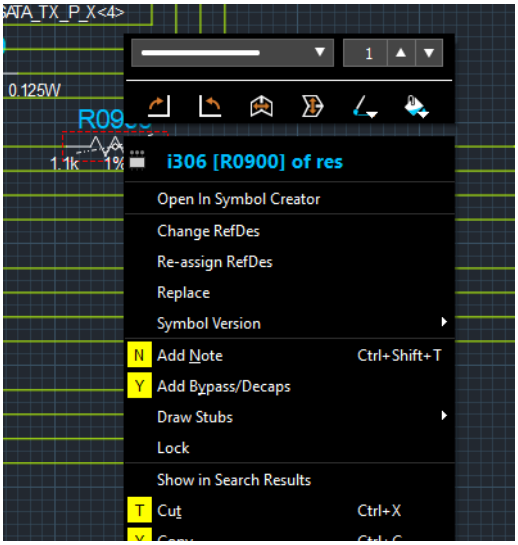
Removing XNets from a Device

The XNET_PINS property is defined as part of library definition for the Resistor component. Therefore, as soon as a resistor component is added, an XNet is generated between the nets that it is connecting. In case the creation of XNet is not needed across the device, you can add a property, NO_XNET_CONNECTION with the value as 1, on the device. This ensures that the XNet is not created across the device. In case the XNet is required across the device, this property can be removed and the XNet regenerated.

You can also remove an XNet by right-clicking the device and choosing *Remove from XNet*.



This command adds the `NO_XNET_CONNECTION` property with the value as `1` on the device. With this property set, an XNet can no longer be created for the design. In case the XNet is desired back, use the Include in XNet command from the right-click pop-up menu. This removes the property and the XNet is regenerated.

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Reusing Constraints from External Sources

Instead of manually setting up constraints, designers can reuse constraints by:

- Importing Pin Delay Values
- Importing ECSets
- Importing a Technology File

Importing Pin Delay Values

Pin Delay values are available in the form of a text file, which you can import directly into System Capture. The same Pin Delay file format as generated from PCB Editor is supported in System Capture. A sample Pin Delay file is shown in the following image:

U1.csv

```
PIN DELAY

REFDES     U1
DEVICE     SOIC16

  1,1.00 MIL
  10,1.00 MIL
  11,1.00 MIL
  12,1.00 MIL
  13,1.00 MIL
  14,1.00 MIL
  15,1.00 MIL
  16,1.00 MIL
  2,1.00 MIL
  3,1.00 MIL
  4,1.00 MIL
  5,1.00 MIL
  6,1.00 MIL
  7,0.00 MIL
  8,1.00 MIL
  9,1.00 MIL
```

A file can contain Pin Delay data for one component instance at a time. The first column of the file contains the Pin Number and the second column contains the Pin Delay value.

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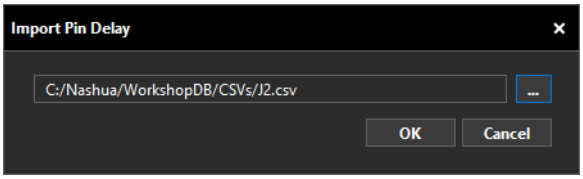
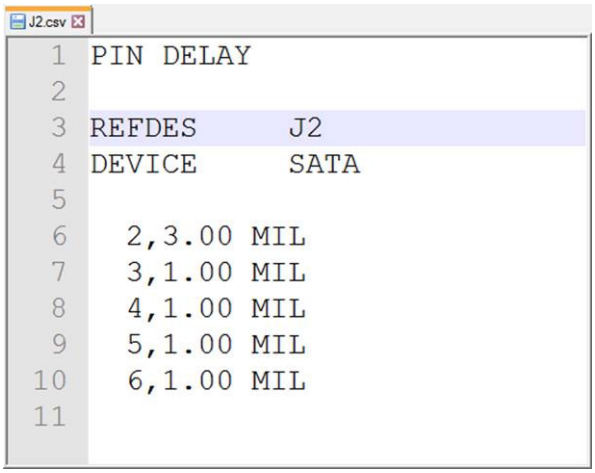
1. Choose *File – Import – Pin Delay*.

   The Import Pin Delay dialog is displayed.

2. Browse and select the Pin Delay file and click *OK*.



   The content of the selected Pin Delay file as illustrated in the following screenshot is imported to the design:



3. View the imported Pin Delay data in the *Properties* form in the *Constraints* section.

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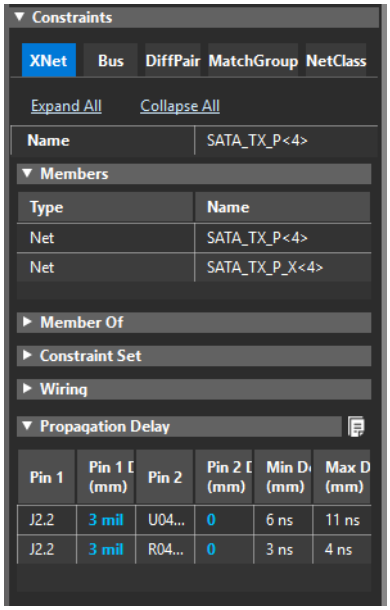
The Propagation Delay constraint shows the newly imported value of delay for pin J2.2 as 3 mil as imported from the Pin Delay file.



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Importing ECSets

The Electrical Constraint Set (ECSet) definition is stored in a Topology file with a `.top` extension. The topology file contains the scheduling as well as the definition of the ECSet. System Capture supports importing a technology file so that the pre-defined ECSets can be imported and applied where required. You can import one or more files at a time.

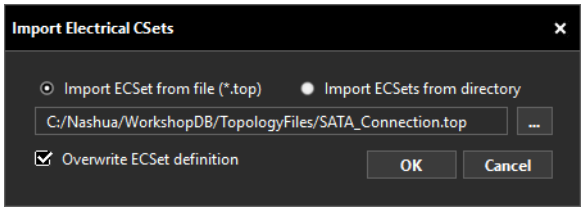
1. Choose the *File – Import – Electrical CSets* menu command.

   The Import Electrical CSets dialog is displayed. You can choose to import a single Electrical CSet or import all the Electrical CSets from a directory.

2. Retain the default option *Import ECSet from file (*.top)*.

3. Browse and select the ECSet file.

4. Select the *Overwrite ECSet definition* check box and click *OK*.



   The topology file is imported and the ECSet is available for application in the *Docked Constraints Manager*.

5. Select the net on the canvas and open the Constraints.

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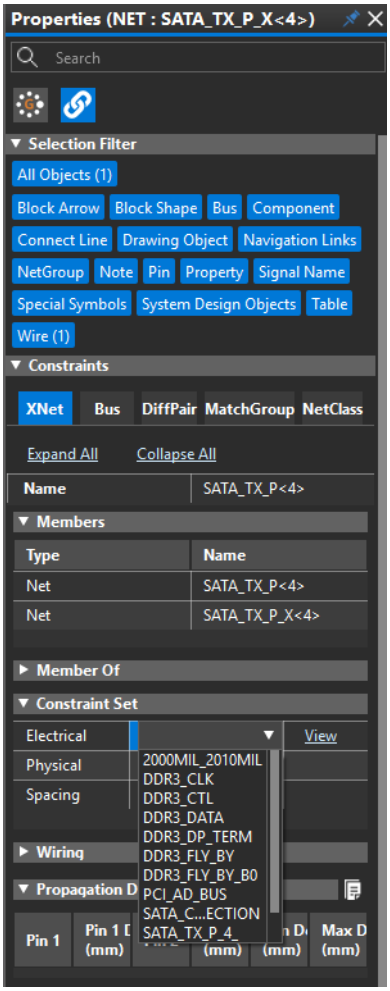
In the Constraint Set section, on expanding the Constraint Set - Electrical list, all the available ECSets are visible including the newly imported value.



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Importing a Technology File

Both the technology and the parameter files are essential components in the process of leveraging re-usable design information during the database creation stage of the design flow. Technology files are used to specify cross-section, drawing, and constraint settings into the database while parameter files are used to specify settings for global and application-based functions.

System Capture supports importing technology files so that the pre-defined Physical and Spacing Constraints Sets can be imported and made available for application.

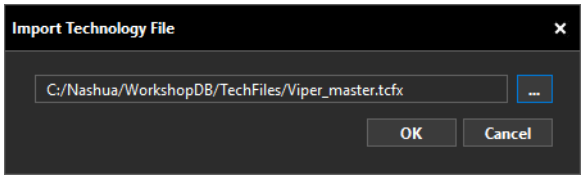
To import a technology file:

1. Choose the *File – Import – Technology File* menu command.

   The Import Technology File dialog is displayed.

2. Browse and select the Technology file.

3. Click *OK* to import the technology file.



   The technology file data is imported and the Physical Constraint Sets (PCSets) and Spacing Constraint Sets (SCSets) are now available for application in the Docked Constraints Manager.

4. Select the net on the canvas and open the Constraints in the Properties form.

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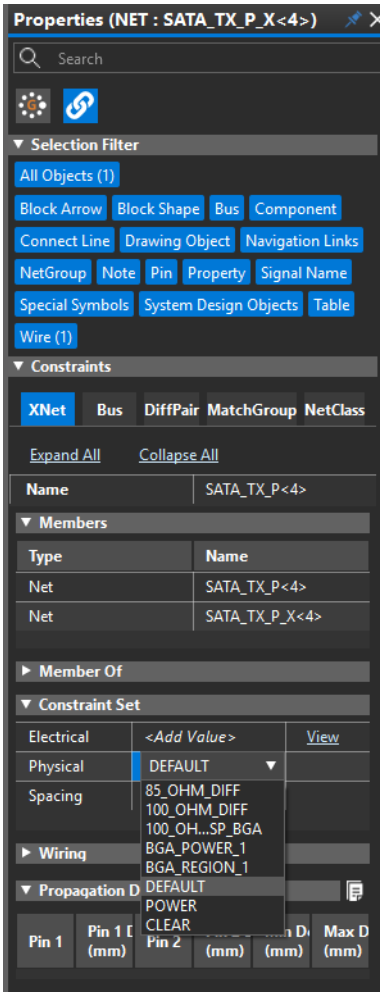
In the Constraint Set section, the DEFAULT Physical CSet and DEFAULT Spacing CSet are applied on the net. Also, all the available Constraint Sets are visible in the drop-down list. You can select and apply any of the Constraint Sets from this list.



Related Topics

Allegro Constraint Manager Reference

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5

Generating Output

This module covers how different outputs can be generated from System Capture. The following topics are covered in this module:

- Accessing Live BOM
- Using Bill of Materials
- Print and Generate PDFs of a Design
- Generating Reports

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Accessing Live BOM

You need a report popularly called the Bill of Materials (BOM) to help you place an order for the required components. A BOM report lists all the components used in a design along with the part numbers and values of the different properties of each component. You can specify the properties to be displayed in a BOM report.

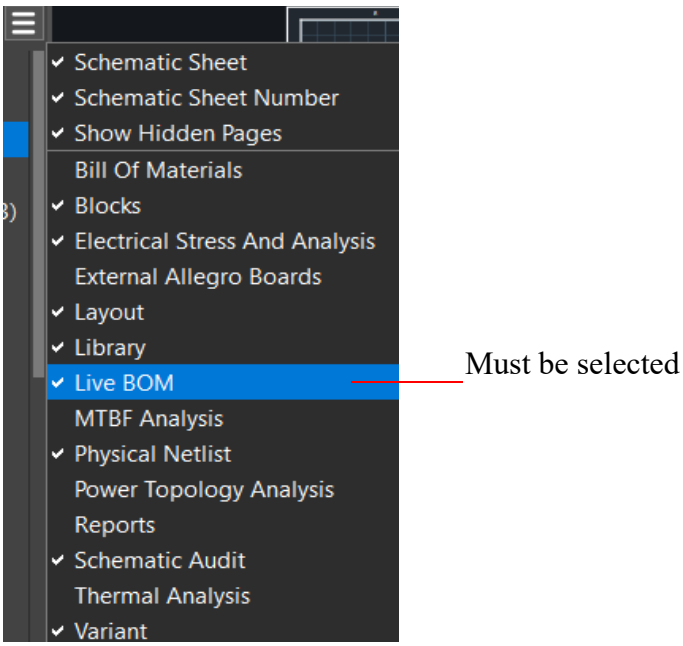
Live BOM presents an always up-to-date view of the design BOM with minimal configuration required. Live BOM is updated when you:

- Use *Place Part* and save the project.
- Use *Add To BOM* from Unified Search in or from the *Library* section in the *Search* tab of the Web dashboard
- Modify the quantity of a component in the *Live BOM* tab in System Capture or *BOM* tab in the Web dashboard

From System Capture, you can access *Live BOM* from the *Project Explorer.*

To view *Live BOM* for a design, do the following:

1. Open the Project Explorer Settings.
2. Ensure the *Live BOM* option is enabled.



3. Click the *Live BOM* entry in the *Project Explorer*.

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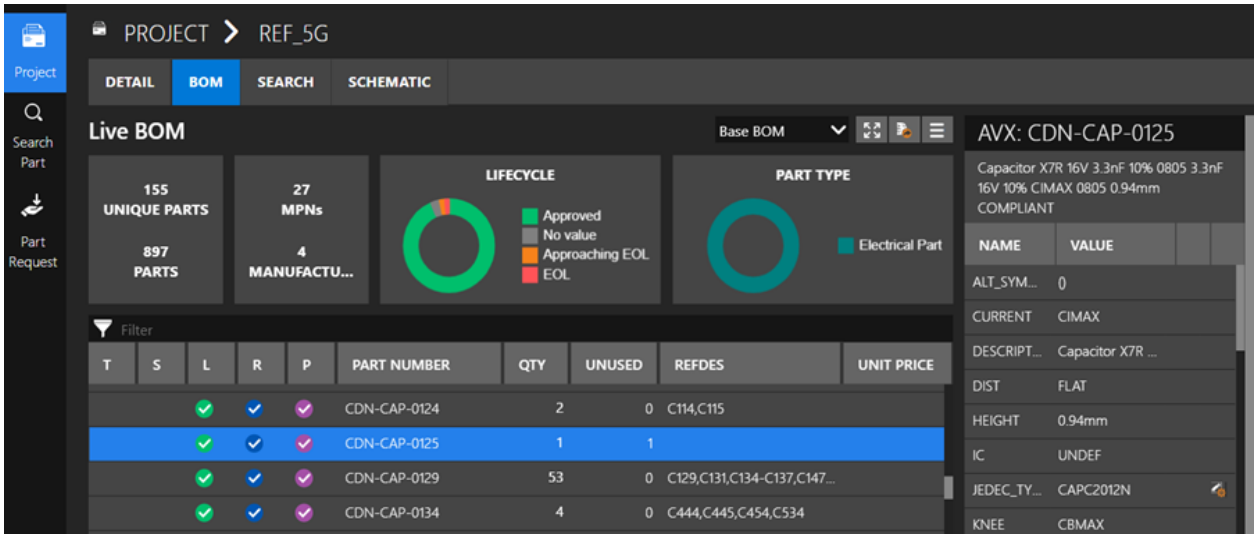
The *Live BOM* tab opens.

From the Web dashboard, you can view the BOM data using the following URLs:

- For projects connected to Design Entry HDL libraries:

  `<pulse_server_URL>/projects`



- For projects connected to OrCAD Capture libraries:

  `<pulse_server_URL>/projects?subtool=orcad`

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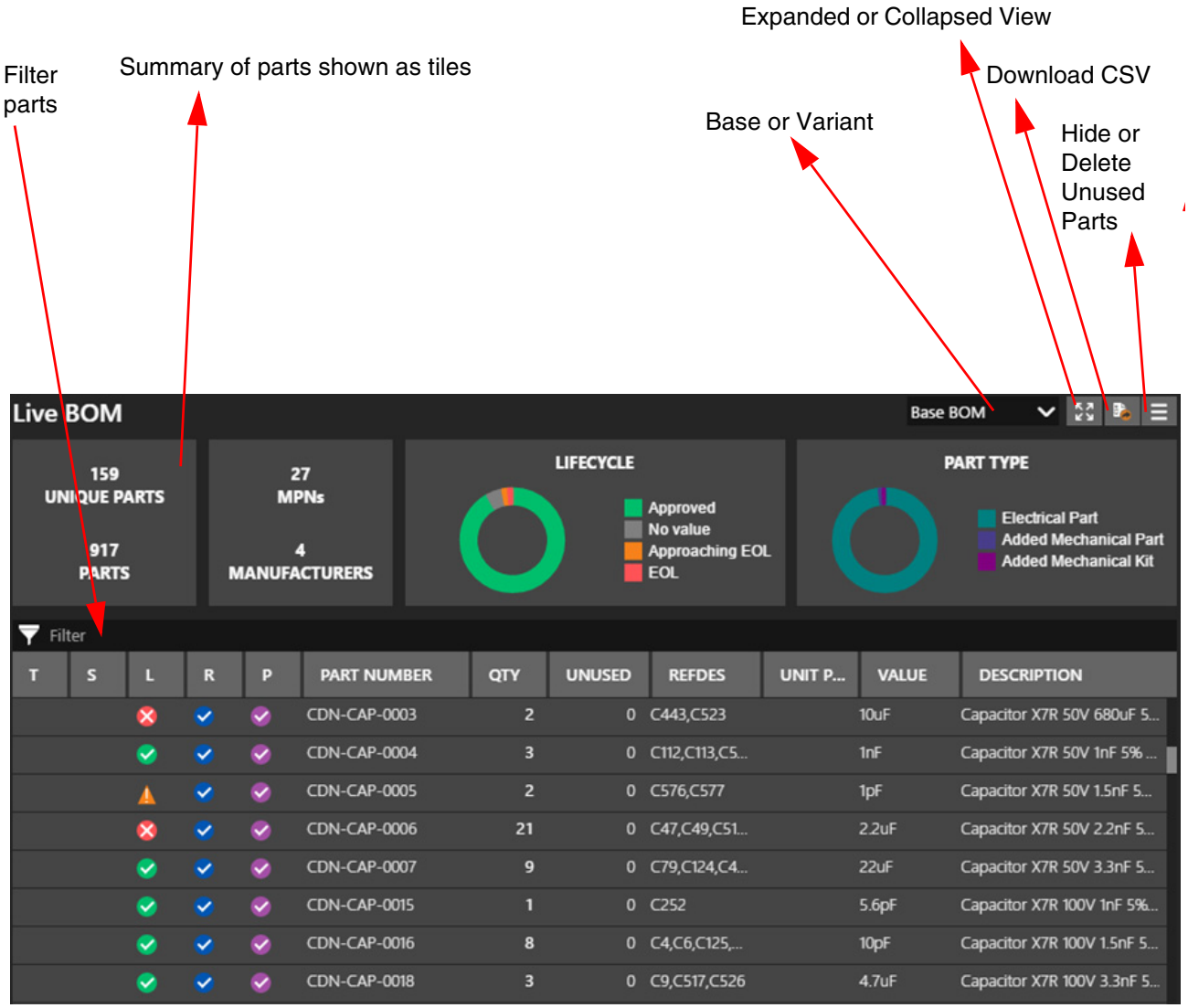
Live BOM Interface



In the *Live BOM* tab, you can:

- View various tiles that provide a summary view of the BOM. This summary contains the following information:
  - Number of unique parts and total parts
  - How many different manufacturers you have in the BOM and how many Manufacturer Part Numbers (MPNs) are there from the unique parts.

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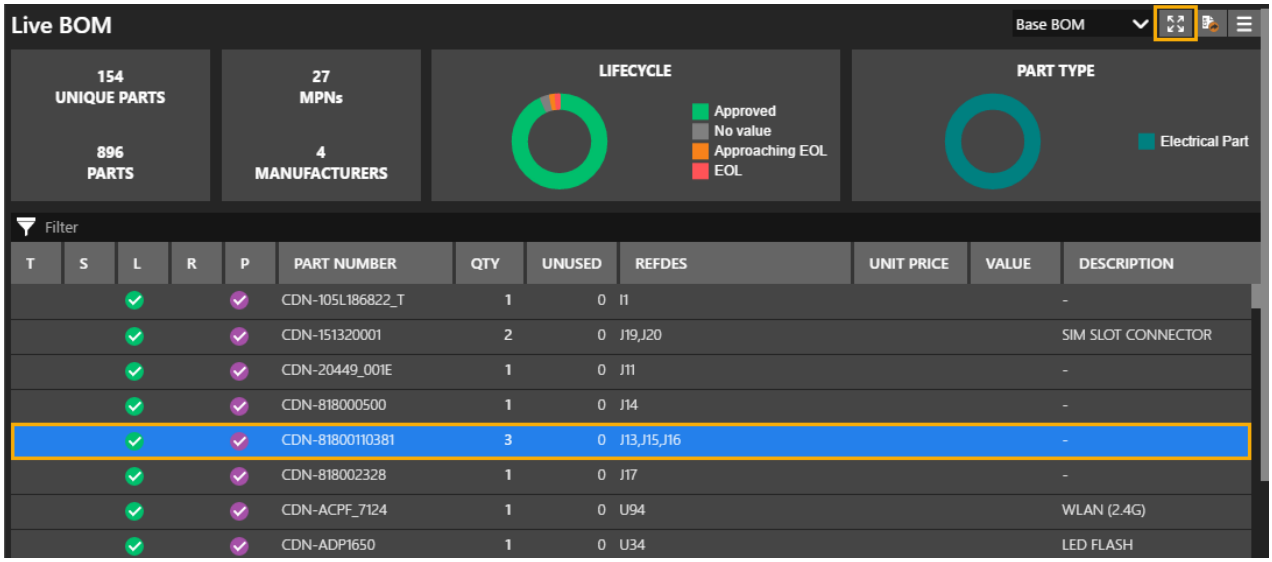
- Lifecycle: Out of the unique parts how many parts have a lifecycle status assigned to them. Some of the values for the status are shown in the figure, such as Approved, No value, Approaching EOL, and EOL. Their distribution is represented in the form of a chart.

  Note: The third column *L* shows the lifecycle status of the part and this rule is configured by the administrator. The contents of this rule are displayed as the third tile in the summary section.

  In the individual mode, the third tile will represent the part status.

- Part Type: Out of the unique parts how many parts are electrical parts, mechanical parts, and mechanical kits. Their distribution is represented in the form of a chart.

- Filter the results and also sort the information using the column headers.
- See the summary for each part in the *Collapsed* view, for example the highlighted row shows that there are 3 instances of that component. The *REFDES* is shown as a list or range.



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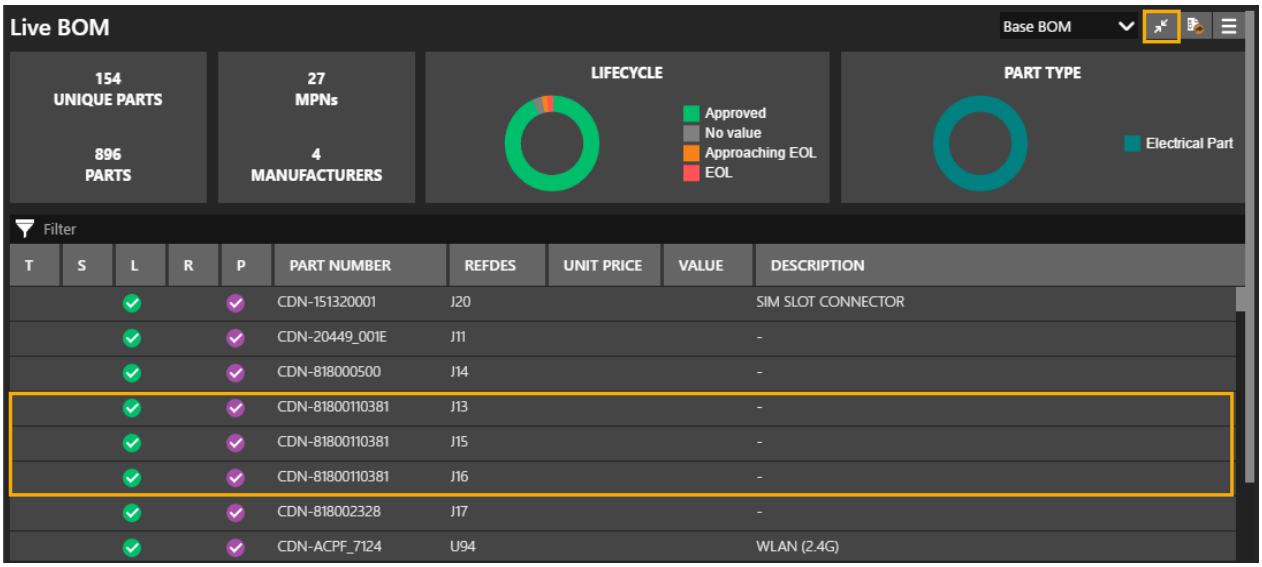
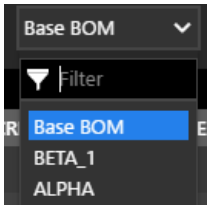
In the *Expanded* mode, each instance is shown as a separate row.



- View the BOM for the base design as well as its variants.



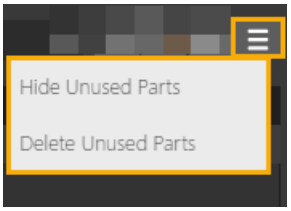
- Download a CSV of the BOM

  The current view of Live BOM is downloaded, whether view is expanded or collapsed, or you have selected base or variant.

- Using the Configure Properties dialog box, you can the columns displayed and also modify the display name of the headers.

  Note: The configure option is only with users with the administrator role in central server setup.

- Hide or delete unused parts



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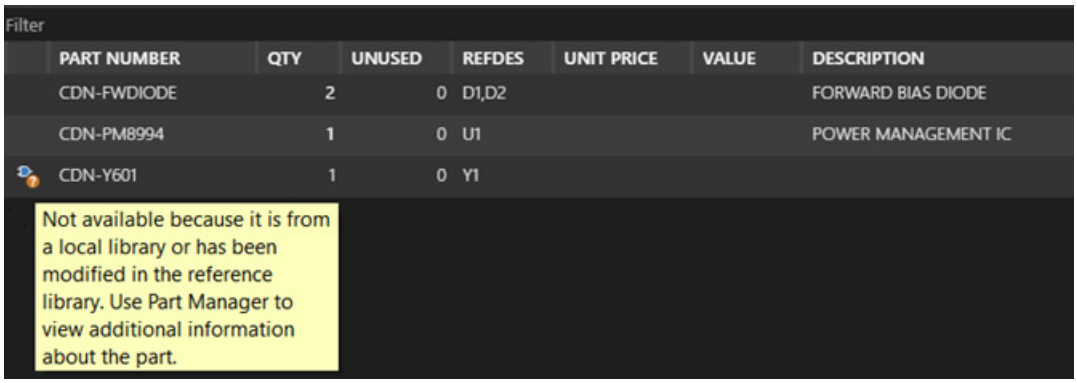
In the Live BOM tab

- In case of mechanical parts, their linked parts' Ref Des is repeated.
- Designers can add mechanical parts, mechanical kits, and electrical parts to *Live BOM*. The quantity of these added parts can be deleted or modified only from *Live BOM*.
- Any changes done to the parts is indicated in the *Live BOM* tab with an icon. To view and update the design with such changes, you need to use Part Manager.



- Mechanical kits and parts quantities are displayed differently if they are connected to electrical parts.
  - Manually added mechanical kits from Unified Search, only show kit names and quantity, such as 1 or 2.
  - When multiple electrical parts have the same linked mechanical kits, the expanded list is repeated.

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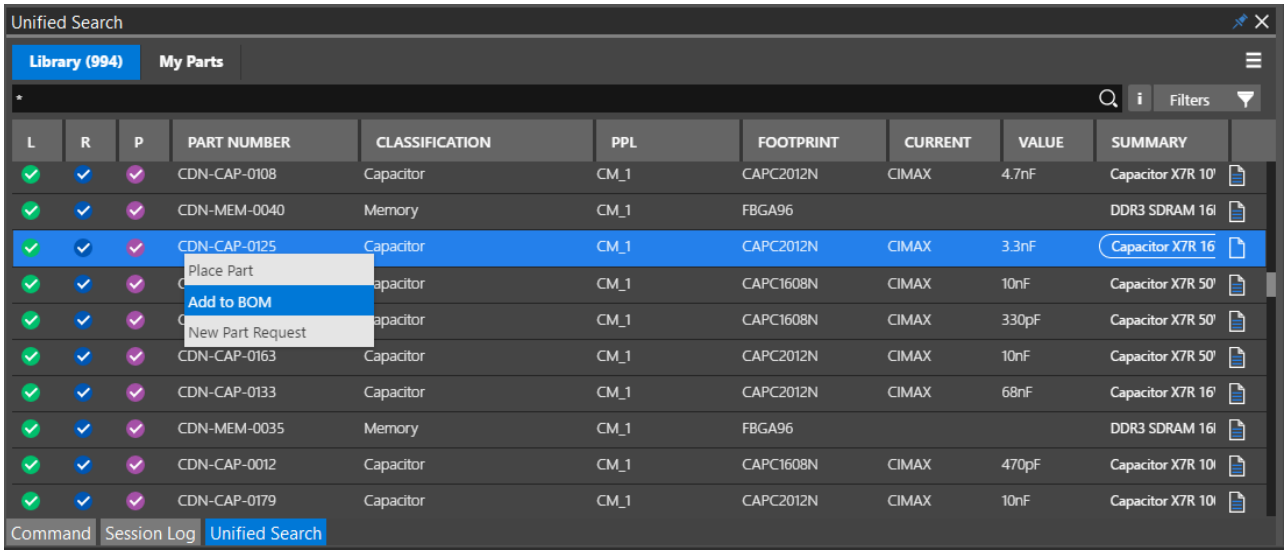
Adding Parts to Live BOM

You may need to create a preliminary BOM before starting with the schematic. You may also want to build a placement queue of parts that is needed when creating the schematic.

This concept is similar to the shopping cart concept used in other schematic tools, such as Design Entry HDL.

To create a BOM, from the *Library* pane in the *Unified Search* tab or from *SEARCH* tab in the dashboard, select a part row, and right-click to select *Add To BOM*.



Related Topics

Accessing Live BOM

Using Add to BOM

- Select a component in the *Library* pane of Unified Search:

  On using *Add To BOM*, the changes are reflected in the *Live BOM* tab in System Capture and in the *BOM* tab of the Web dashboard immediately.

- Select a component in the *Library* pane of Unified Search or in the *Live BOM* tab:

  On using *Place Part*, the changes are updated in the *Live BOM* tab of System Capture on saving the project and in the Web dashboard on using the *Commit* operation.

- Select a component in the *Live BOM* tab of System Capture:

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On modifying its quantity under the *QTY* column, the changes are seen in the *BOM* tab of the dashboard immediately.

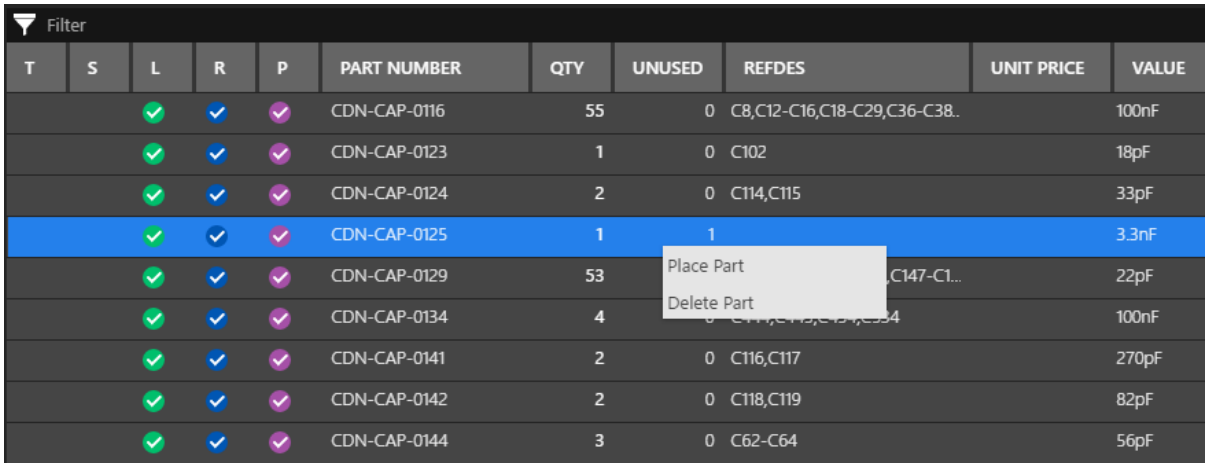
Important

The *Add To BOM* and quantity (*QTY)* changes in Live BOM are not under version control. That is, the unplaced (*UNUSED*) parts will be available in *Live BOM* when you load an older version of the design in System Capture.

Operations from Live BOM in System Capture

You can perform the following tasks from the *Live BOM* tab in System Capture:

- Place a part
- Delete an unused part



- Cross-probe to a placed part instance

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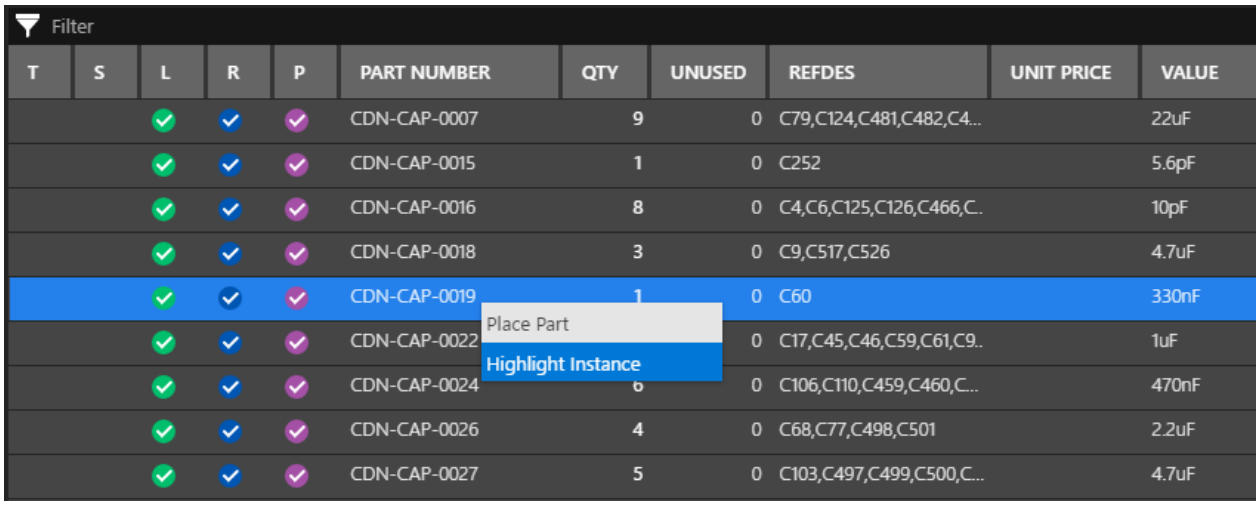
To highlight a placed part on the schematic, either double-click the part instance or right-click and select *Highlight Instance*.



Related Topics

- Accessing Live BOM
- Live BOM Interface

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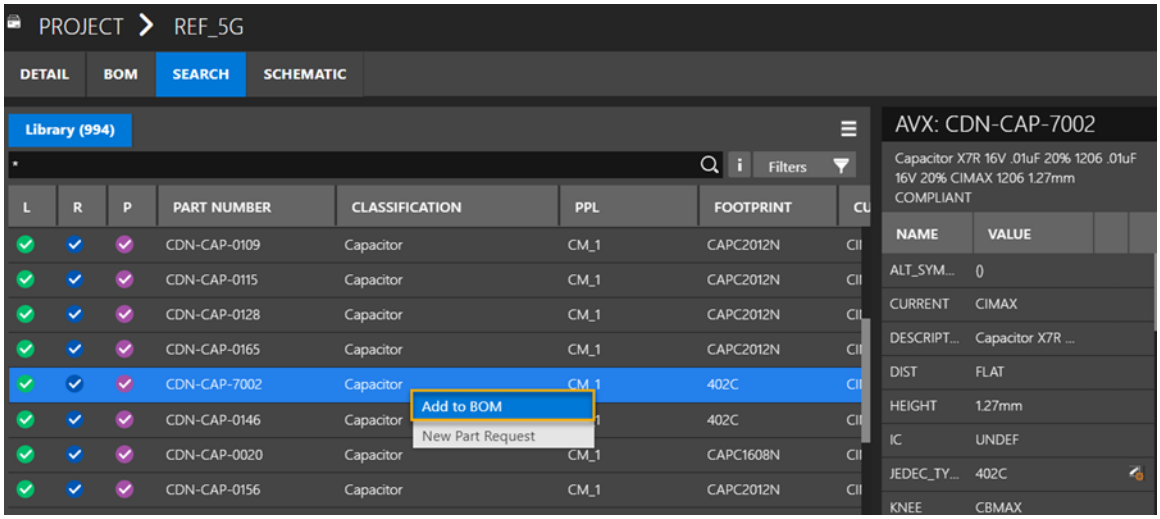
Viewing Live BOM in Web Dashboard

When you modify *BOM* in the Web dashboard, the changes are seen in *Live BOM* tab in System Capture immediately.

To see how changes are reflected from dashboard to System Capture, do the following.

1. From the *Library* section in the Search tab of the Web dashboard, select a component.
2. Right-click and select *Add To BOM*.



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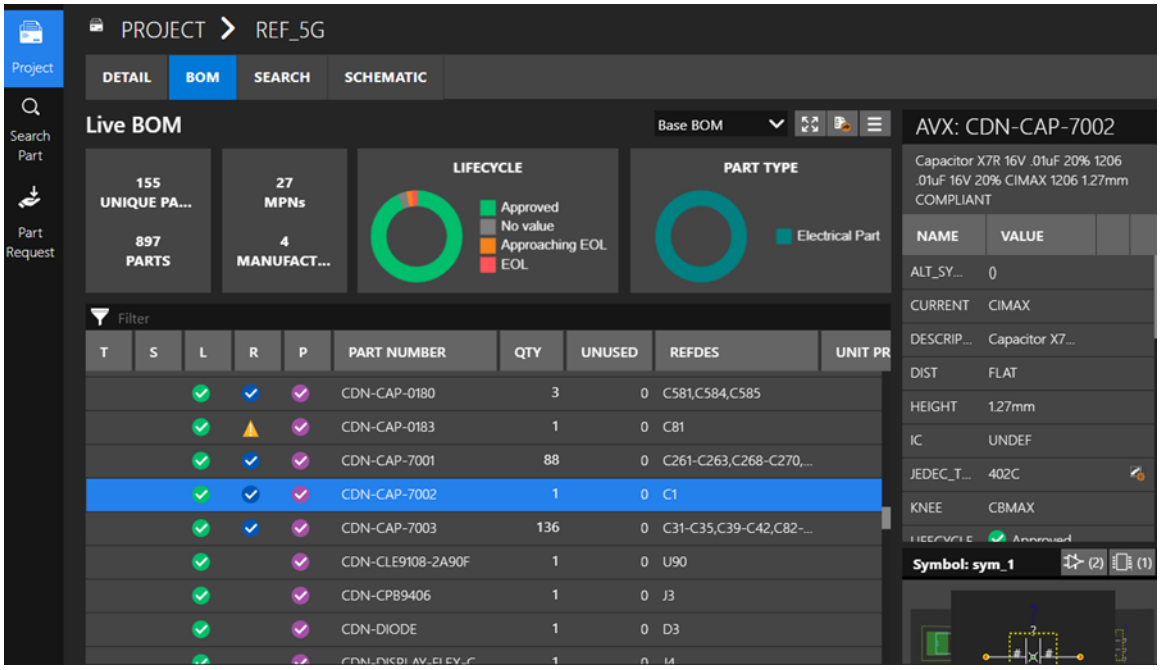
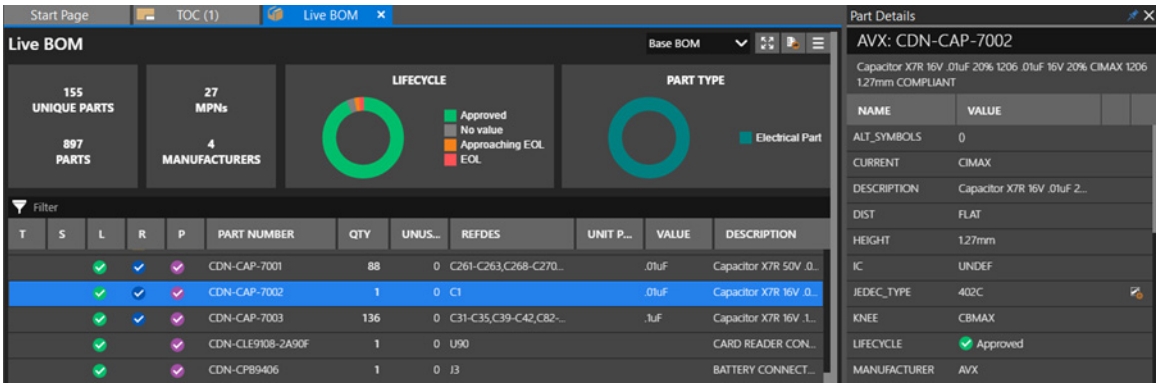
The changes are seen in the *BOM* tab in Web dashboard and in the *Live BOM* tab in System Capture simultaneously.





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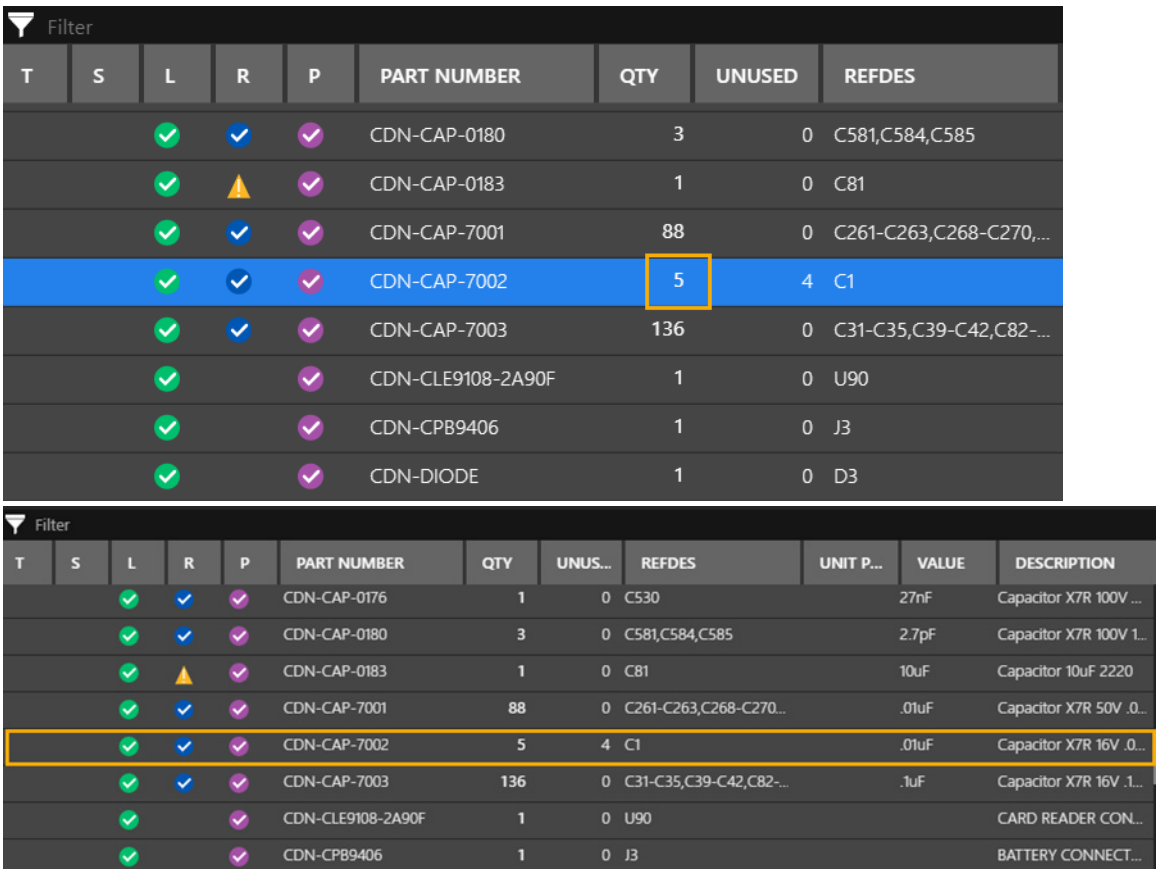
Similarly, if you modify the *QTY* value in the dashboard, you can see the changes in System Capture simultaneously.



Filter

T	S	L	R	P	PART NUMBER	QTY	UNUSED	REFDES
					CDN-CAP-0180	3	0	C581,C584,C585
					CDN-CAP-0183	1	0	C81
					CDN-CAP-7001	88	0	C261-C263,C268-C270,...
					CDN-CAP-7002	5	4	C1
					CDN-CAP-7003	136	0	C31-C35,C39-C42,C82-...
					CDN-CLE9108-2A90F	1	0	U90
					CDN-CPB9406	1	0	J3
					CDN-DIODE	1	0	D3

Filter

T	S	L	R	P	PART NUMBER	QTY	UNUS...	REFDES	UNIT P...	VALUE	DESCRIPTION
					CDN-CAP-0176	1	0	C530		27nF	Capacitor X7R 100V ...
					CDN-CAP-0180	3	0	C581,C584,C585		2.7pF	Capacitor X7R 100V 1...
					CDN-CAP-0183	1	0	C81		10uF	Capacitor 10uF 2220
					CDN-CAP-7001	88	0	C261-C263,C268-C270...		.01uF	Capacitor X7R 50V .0...
					CDN-CAP-7002	5	4	C1		.01uF	Capacitor X7R 16V .0...
					CDN-CAP-7003	136	0	C31-C35,C39-C42,C82-...		.1uF	Capacitor X7R 16V .1...
					CDN-CLE9108-2A90F	1	0	U90			CARD READER CON...
					CDN-CPB9406	1	0	J3			BATTERY CONNECT...

Tip

You can control which parts to exclude from the Live BOM by adding Attribute Name and Value pairs to `search.config`. For example, BODY_TYPE = COMMENTS. For steps to download and upload the `search.config` file, see *Using Custom Configuration File*.

Related Topics

- Adding Parts to Live BOM
- Using Custom Configuration File

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Using Bill of Materials

Three report formats are supported by Bill of Materials:

- Base Schematic BOM

  Report is created with the name `BOM.rpt` by default.

- Variant BOM

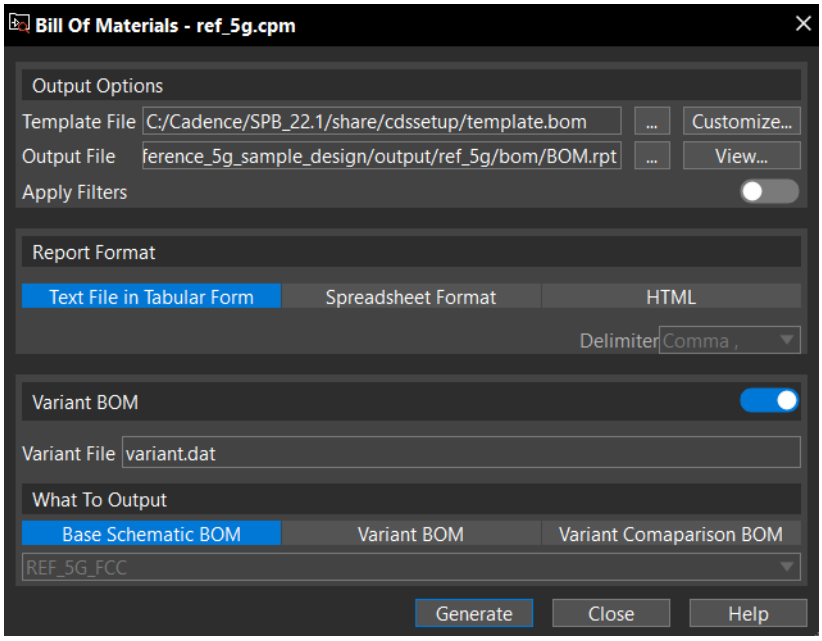
  Report is created with the name of variant, such as `alpha.rpt`.

- Variant Comparison BOM

  Report is created with the name `ComparisionBOM.rpt` by default.

➡ To generate a BOM report, choose *Tools – Generate BOM*.

The Bill of Materials dialog is displayed. This is where you specify the details of the type of report you want and the template to be used to generate the report.



You can customize the information and format of the BOM report using the *Customize* option.

The Bill of Materials tool uses the information in the netlist files to generate BOM reports. The reports are placed in a folder with the name BOM at the same level as the project file. The

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report lists all the components in the design along with their properties. The properties displayed in the report are determined by the BOM template file.

```
TITLE:                  Bill of Materials
DATE:                   09/24/2019
DESIGN:                 workshop_3
TEMPLATE:               c:/cadence/spb_17.4/share/cdssetup/template.bom
CALLOUT:                bom.callouts

 Ref     Part Number    ALPHA        BETA         COPY-ALPHA        GAMMA
 Des
======   ============   ==========   =========    ===============   ==========
 J201    CDN-CON-0014   -            DNI          DNI               -
         A
 J202    CDN-CON-0014   DNI          -            DNI               -
         A
 J203    CDN-CON-0014   -            DNI          DNI               -
         A
 J204    CDN-CON-0014   DNI          -            DNI               -
         A
 J205    CDN-CON-0014   -            DNI          DNI               -
         A
 J206    CDN-CON-0014   DNI          -            DNI               -
         A
R0600    CDN-RES-0290   CDN-CAP-01   CDN-CAP-0    CDN-CAP-0154      -
                        54           154

Common Components List :
 Ref     Part Number
 Des
======   ============
C0200    CDN-CAP-0185
C0201    CDN-CAP-0185
C0202    CDN-CAP-0185
C0203    CDN-CAP-0185
C0204    CDN-CAP-0185
C0205    CDN-CAP-0185
C0206    CDN-CAP-0182
```

In addition to the Variant BOM, you can also create a Variant Comparison BOM report, which provides a part number-based comparison between the components of the base schematic

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and all the variants. This report lists the DNI components in individual variants, and all the common components across the base schematic and the variants.

```
TITLE:                  Bill of Materials
DATE:                   08/17/2018
DESIGN:                 root
TEMPLATE:               d:\cadence\spb_17.2\share\cdssetup\template.bom
CALLOUT:                bom.callouts

 Ref      Part Number    ALPHA        BETA         TEST
 Des
======    ============   ==========   =========    =========
J0400     CDN-CON-0014   DNI          DNI          -
J0401     CDN-CON-0014   -            DNI          -
J0402     CDN-CON-0014   -            DNI          -
J0403     CDN-CON-0014   -            DNI          -
J0404     CDN-CON-0014   -            DNI          -
J0405     CDN-CON-0014   -            DNI          -

Common Components List :
 Ref      Part Number
 Des
======    ============
C0206     CDN-CAP-0185
C0207     CDN-CAP-0185
C0208     CDN-CAP-0185
C0218     CDN-CAP-0185
C0219     CDN-CAP-0185
C0220     CDN-CAP-0185
C0227     CDN-CAP-0182
C0228     CDN-CAP-0182
C0229     CDN-CAP-0182
C0230     CDN-CAP-0184
C0231     CDN-CAP-0184
C0232     CDN-CAP-0184
C0233     CDN-CAP-0185
C0234     CDN-CAP-0185
C0235     CDN-CAP-0185
```

Related Topics

- Accessing Live BOM
- Using Add to BOM

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Print and Generate PDFs of a Design

System Capture provides the standard plotting and printing functionality. You can print your design, save as a basic PDF file, PDF/A or a Smart PDF.

Smart PDFs usually load faster as they are smaller in size compared to traditional PDFs. You can explore the available print options when creating a PDF, such as how to:

- Password protect the PDF with the *Encrypt PDF* option.
- Allow or block printing the PDF.
- Specify what changes are allowed in the PDF, such as commenting, page manipulations, and so on.
- Control copying of text and other objects.
- Grant access to screen reading devices.

When using PDF format, you can face challenges with files stored for a long time, such as the fonts no longer being available on the systems. In such cases you can face problems in reading the text or in opening the PDF.

PDF/A format, which is available with the Allegro Design Publisher License is more suitable for long-term archiving. Fonts used are embedded in the PDF/A, and are independent of the OS. However, PDF/A does not support:

- Encryption
- Annotation
- Insertion of audio and video content
- External content references, such as hyperlinks
- File attachments

You can also choose to generate a Color or a Black and White PDF for your project.

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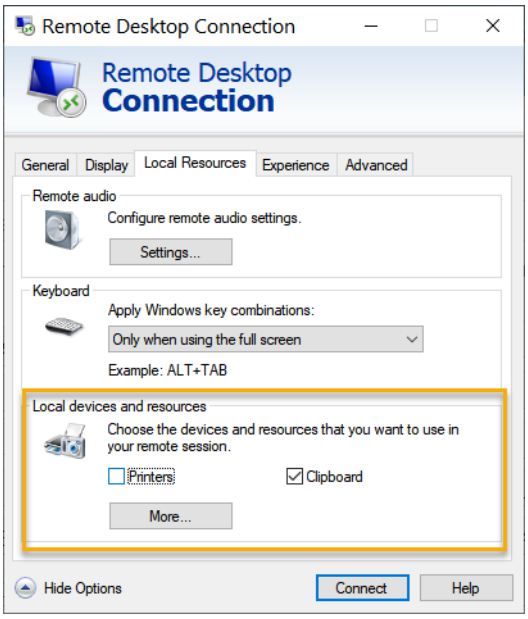
Prerequisites

- In case you are working on a Remote Desktop, ensure the *Printers* check box is ***not*** selected in the *Local devices and resources* section of the *Local Resources* tab. If this is missed, there is a possibility of System Capture behaving erratically when printing.



- When working on non-local displays, such as xvfb (X virtual framebuffer), make sure that the resolution matches the display resolution for correct PDF output.

Creating a PDF

To generate a PDF or print a design:

1. Select *File – Print*.

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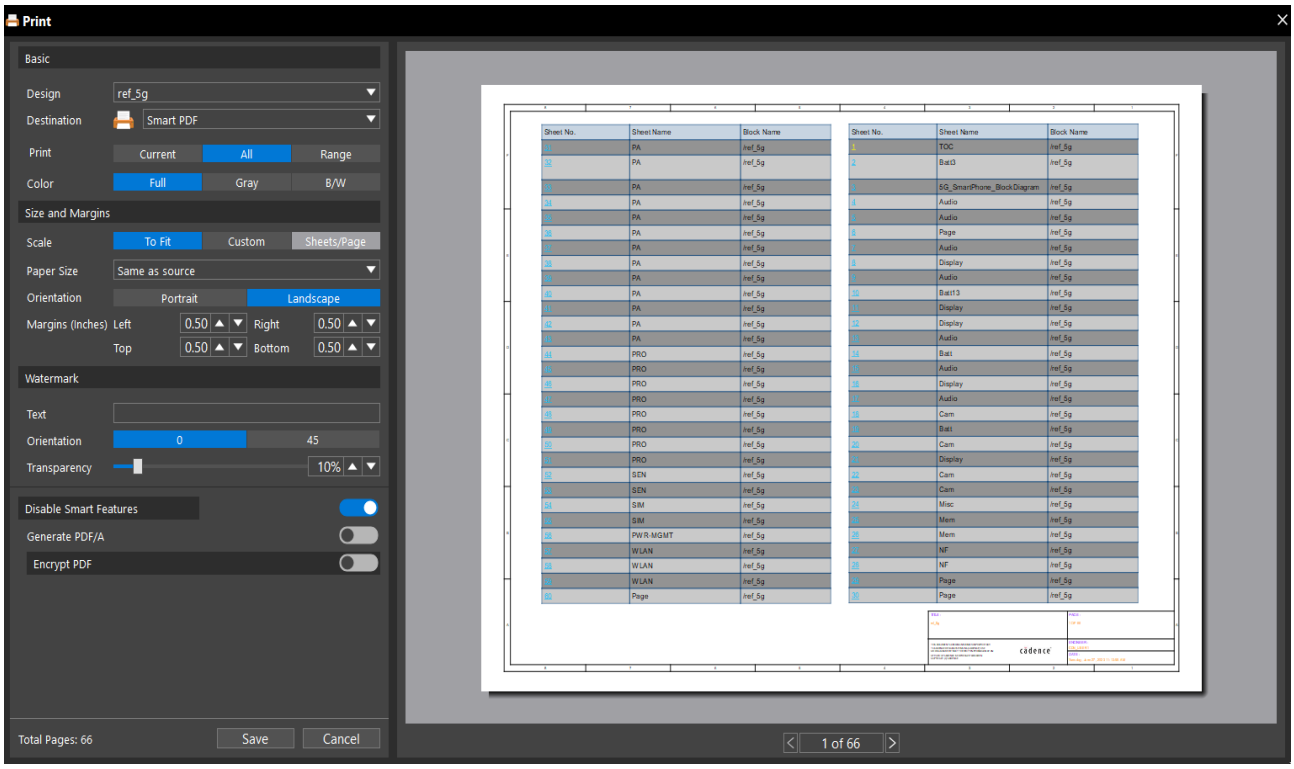
2. Choose *Smart PDF* as the destination.



You have the option to *Disable Smart Features*.

3. If required, enable *Generate PDF/A*.

Smart features must remain enabled for *Generate PDF/A* and *Encrypt PDF* functionalities.

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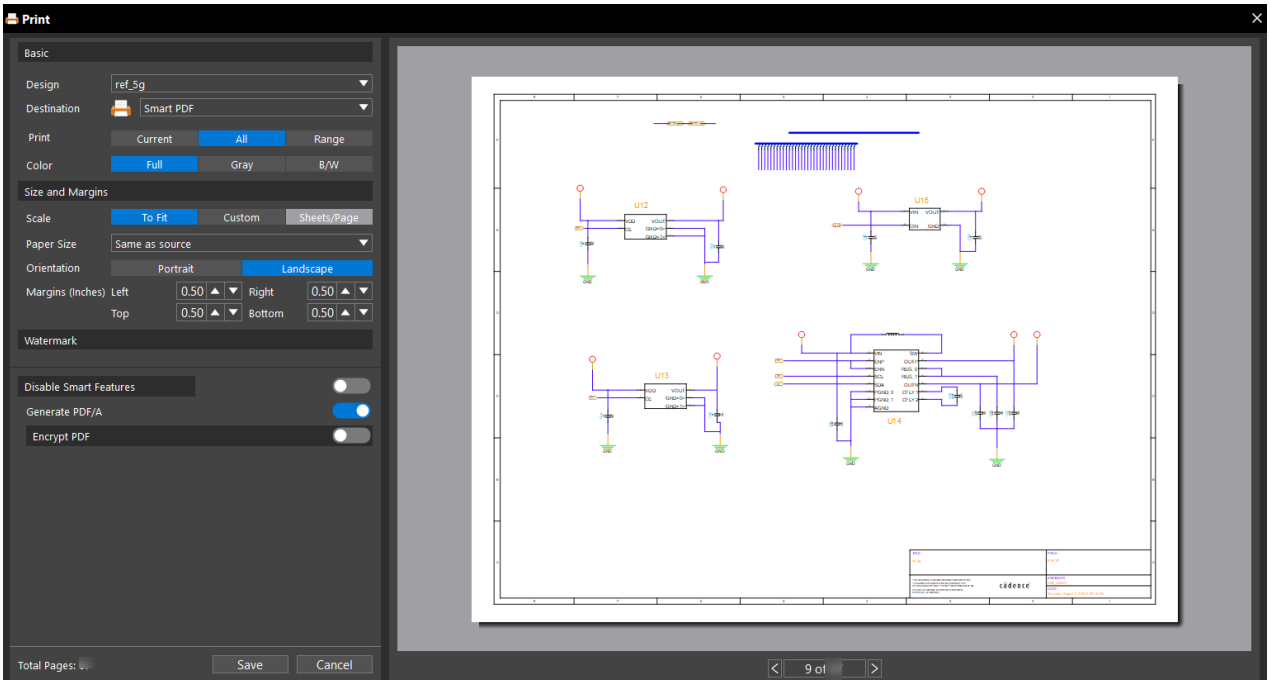
4. Make other changes in configuration, as necessary.



5. Click *Save*.
6. Specify the file location and file name.
7. Click *Save*.

Controlling the Blocks to Print

By default all the blocks and pages in a design are printed on printing the design. If you want to restrict the printing of certain blocks, follow these steps before opening the design:

1. Enable the `PRINT_EXCLUSION` directive in the `site.cpm` or *`design`* file.

   ```
   PRINT_EXCLUSION 'true'
   ```

2. Save and close the cpm file.
3. Open the design in which you want to restrict the printing of blocks.

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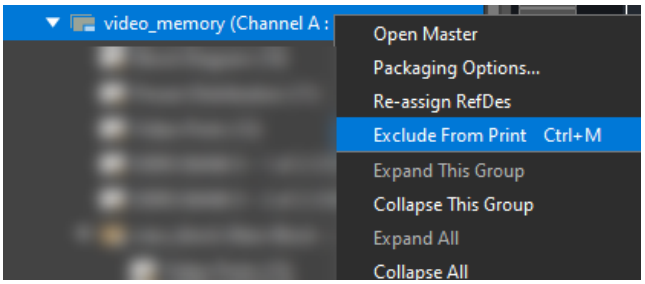
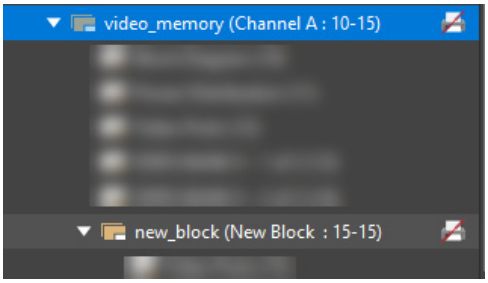
4. Right-click a block and choose *Exclude From Print*.

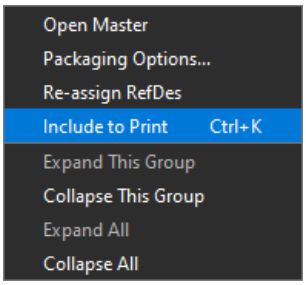


An icon shows up next to the block and its sub-blocks.



When this design is now printed, this block is excluded.

➡ To include an excluded block back in the printing, right-click the block and choose *Include to Print*.



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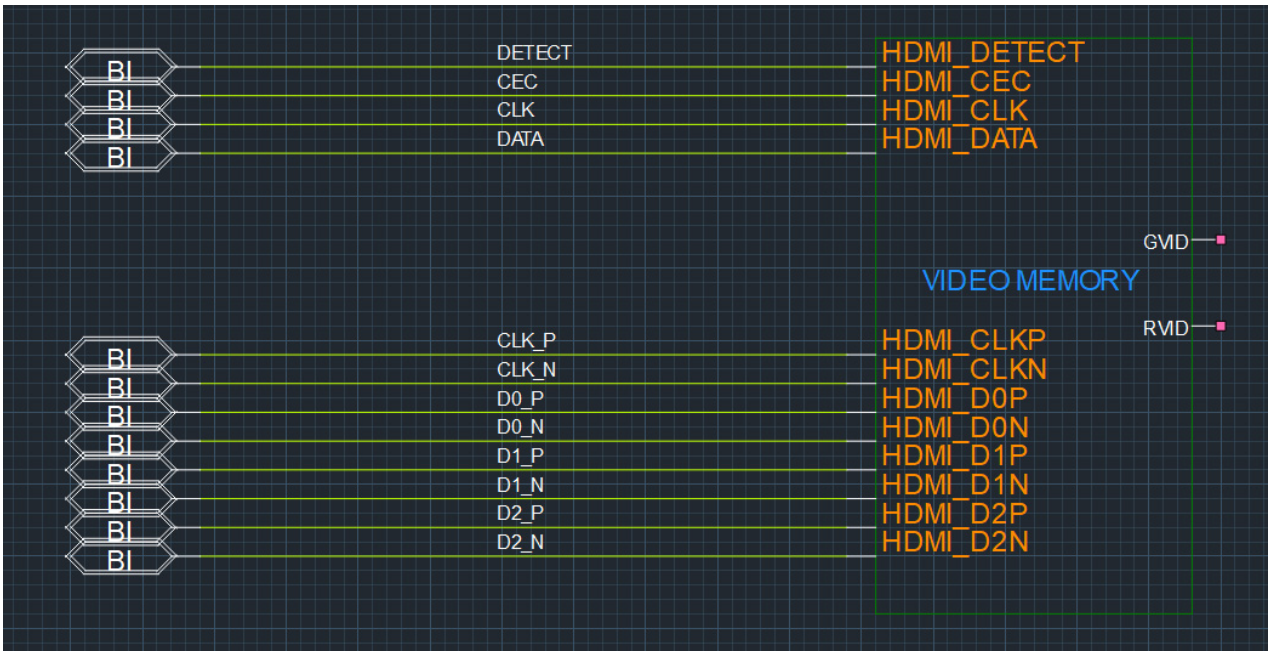
Navigation Links in PDFs

Allegro X System Capture provides navigation capabilities within the application using the Navigation Window. But when the schematics created in System Capture are published as PDF or plotted on paper, a different solution comes handy. Navigation links acts as an aid for tracing signals across the design while not in System Capture.

All signals connected to OffPage/Port symbols are used for generation of navigation links. In case you need to trace a net using navigation links, you need to connect an OffPage or Port symbol to the net. A net connected to OffPage/Port symbol has navigation links for all the other locations where the net with same name exists with OffPage/Port symbols.

Each navigation link contains two parts, Page Number and Zone information. The navigation links are hyperlinked for quick navigation. These links can be traversed in System Capture as well as in generated Smart PDF file. While taking a plot of the schematic, these navigation links are visible, and user can manually follow them.



The zone information for the schematic sheet is read from Cross Reference Data File. The location of this file can be configured using a Project (`cpm`) file directive.

System Capture automatically places navigation links on the OffPage/Port symbols. The OffPage / Port symbols can also be pre-configured with placeholders for the navigation links.

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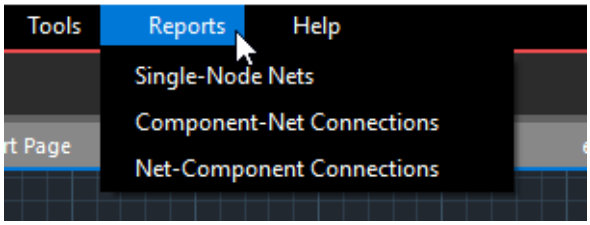
Related Topics

Block Differences in Report

Generating Reports

System Capture provides support for generation of commonly used reports. These reports are available through the Reports menu.

➡ To print a report, choose *Reports – <Report_type>* to generate the required report.



The reports are generated in the same folder as the project file. The generated reports are formatted as text files which can be easily parsed. The following data is included in the reports:

- Component-based Netlist Report
  - RefDes.PinNum, Net Name
- Unnamed Nets Report
  - Net Name, Block Name, Page Number
- Single Node Nets Report
  - Net Name, Block Name, Part Name, Page Number
- Net-based Netlist Report
  - Net Name, RefDes.PinNum

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Block Differences in Report

A command-line utility is available that compares logical connectivity between two designs, or two versions of the same design, and generates a list of netlist differences. The report classifies differences as:

- Connectivity objects
- Properties compared

Syntax

```
logicalDesignCompare
   -dstproj <Destination Project Path>
   -srcproj <Source Project Path >
   -report <Differences Report Path>
   [-block <Block Name>]
   [-mode id | name | RefDes]
   [-log <logfilepath>]
```

The differences reported are based on any one of the following modes:

- ID

  Compares revisions of a design. ID-based difference is useful when there are logical differences in a design, for example, renamed or replaced net names

- Name

  Compares the designs based on logical names of connectivity objects, such as nets, components, and pins.

- RefDes

  Compares two designs based on the physical name of the connectivity objects, such as reference designator of components, physical net name of nets, and so on.

  Name and Ref Des difference is used to compare designs when they are imported from other applications into System Capture. This helps to check whether Ref Des were preserved or modified.

The following are **not** reported:

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- Non-electrical objects and constraints are **not** compared.
- NetGroup modifications are not reported, such as rename or membership changes.
- Attribute changes are not reported for added components.

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6

Schematic and Layout Information Transfer

The schematic to layout journey happens in two directions:

- Schematic to layout

  This is also called the front-to-back flow. In this mode, a logical design created in System Capture gets translated into a physical design ready for layout in PCB Editor. To run the front-to-back mode, run the *File – Export to Layout* command.

  Tip

  To update design changes in an existing physical design, you can use subsequent Export to Layout runs.

  To import the design into the PCB Editor environment, you can also use the PCB Editor *Import Logic* feature.

  When transferring a logic design to physical design in System Capture, the packaging step is eliminated. Only the `*.pst` files are generated to synchronize with PCB Editor.

  Exporting Logical Design to Physical Design has the steps for this flow.

- Layout to schematic

  This is also called the back-to-front flow. Changes made in the layout file in PCB Editor are brought back to the schematic to ensure both remain updated.

  To run the back-to-front mode, run the *File – Import – Layout* command.

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Exporting Logical Design to Physical Design

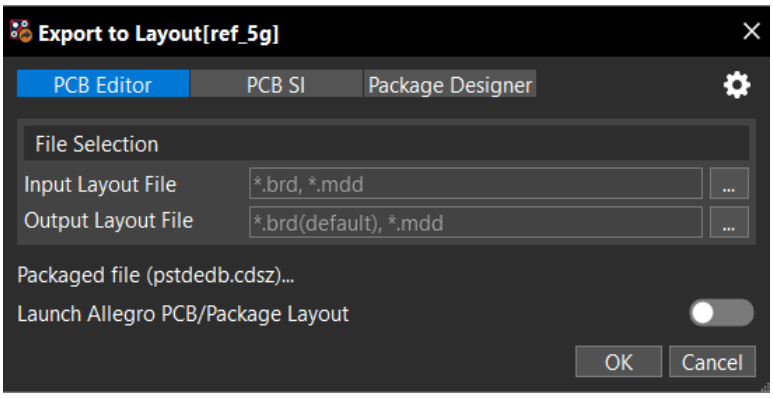
After a schematic design is complete and design rules checks have been done, the design is ready to be translated from a schematic into a physical design. Packaging involves converting a logical design into a physical layout and vice versa. An internal utility called Packager-XL acts as an interface between the schematic and the board. This utility:

- Translates the schematic into a physical design
- Brings back the changes made in the board file to the schematic
- Updates the changes made in the schematic after initial packaging to the board

To transfer a System Capture schematic to Allegro PCB Editor board:

1. Choose *File – Export to Layout*.

   The *Export to Layout* dialog box opens.



   The dialog box contains similar tabs for PCB Editor, PCB SI, and Package Designer. Choose the application to export the layout to.

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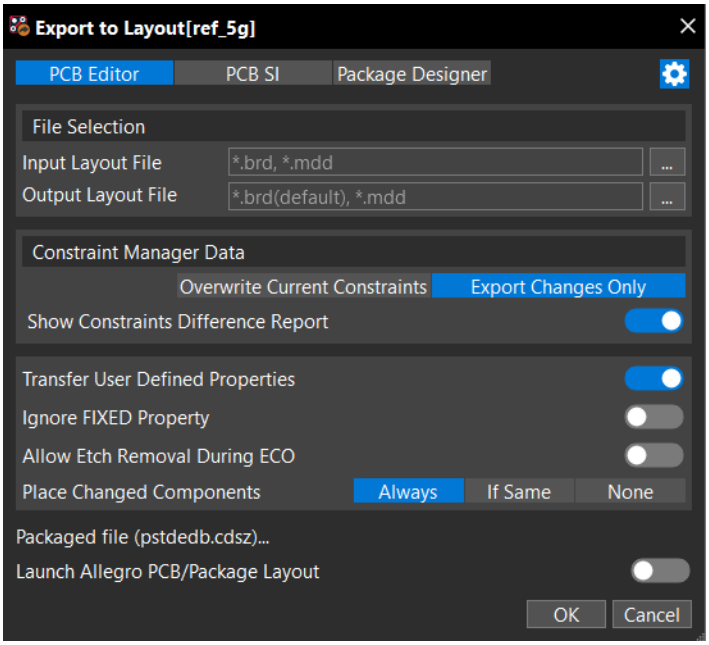
2. Click the gear icon on top-right.



3. Specify the *Input Layout File*, if needed.

   The input board file or previous board file (*.brd, physical view), which is a base (template) file on top of which the logical schematic data is placed to create the output board file.

4. Specify the *Output Layout File*, if needed.

   The output board file (*.brd) or the same board file that is created when the logic data is loaded onto the input board file.

5. Specify how to manage the *Constraint Manager Data*.

   - *Overwrite current constraints*

     All existing electrical constraint information in the Output Board file get overwritten with the electrical constraint information currently available in the schematic.

   - *Export changes only*

     Only the electrical constraints that have changed in the schematic since the last export get exported and overwrite the constraints in the Output Board File.

   - *Show Constraint Difference Report*

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Enables you to compare two constraint databases to view the constraint differences in a report viewer. The report lists the objects which have changed since the last update.

For more information, see *Generating and Viewing Constraints Differences* in Allegro Constraint Manager User Guide.

6. Specify if the `FIXED` property should be ignored.

Select the *Ignore FIXED property* option to indicate that components with FIXED property set as TRUE can also be moved or deleted.

7. Decide if *Allow Etch removal during ECO* should be selected.

If a pin is removed from a net because of an engineering change order (ECO), use this option to specify that the etch be ripped up from a removed pin to the closest T connection or pin.

Important

Do not select this option if you want PCB Editor to rip up the etch interactively.

8. Specify what to do with the components that have changed.

The *Place Changed Components* controls you what to do when the new design logic is loaded into the PCB Editor or SI layout. An ECO (engineering change order) can result in a reference designator being assigned to a different type of device in the schematic than the device used in the PCB Editor layout.

- If the part has not changed, it maintains its location in the PCB Editor layout.
- If the part has changed, you can select one of the following options:
  - *Always*

    Specifies that PCB Editor must replace all components in the layout with the new components according to their reference designators. *Always* is the default option. The new component is placed at the same x y location and rotation as the old part.
  - *If Same*

    Specifies that PCB Editor must replace all components in the layout with the new components, but only if the replacement component matches the package symbol, value, and tolerance of the component in the layout. If the package

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symbol has changed, the old part is removed from the layout, and the changed part is added to the PCB Editor database (unplaced part).

- *None*

  Specifies that PCB Editor should not replace the components in the layout with new components from the packager. You must make the changes interactively.

9. Specify the application to open the layout file in, if any from the following:

- Allegro PCB Editor is the default option
- Allegro PCB SI
- Allegro Package Designer

10. Click *OK*.

This schematic is transferred into a board file with the name you specified and opened in PCB Editor. Select the license as Allegro PCB Design with the High Speed Option. If this is not available, then use any other license available to access Allegro PCB Editor.

You can now make changes to the layout, such as change part placements, change RefDes values, and modify constraints. You can also check how *Cross-Probing between Schematic and Board* works.

This completes the front to back flow when a schematic design is exported to the board layout. See *Updating the Schematic with Changes made in PCB Editor* for details of the back-to-front flow where constraints, stackup, and other design information from the board gets brought back to the schematic.

Related Topics

Updating the Schematic with Changes made in PCB Editor

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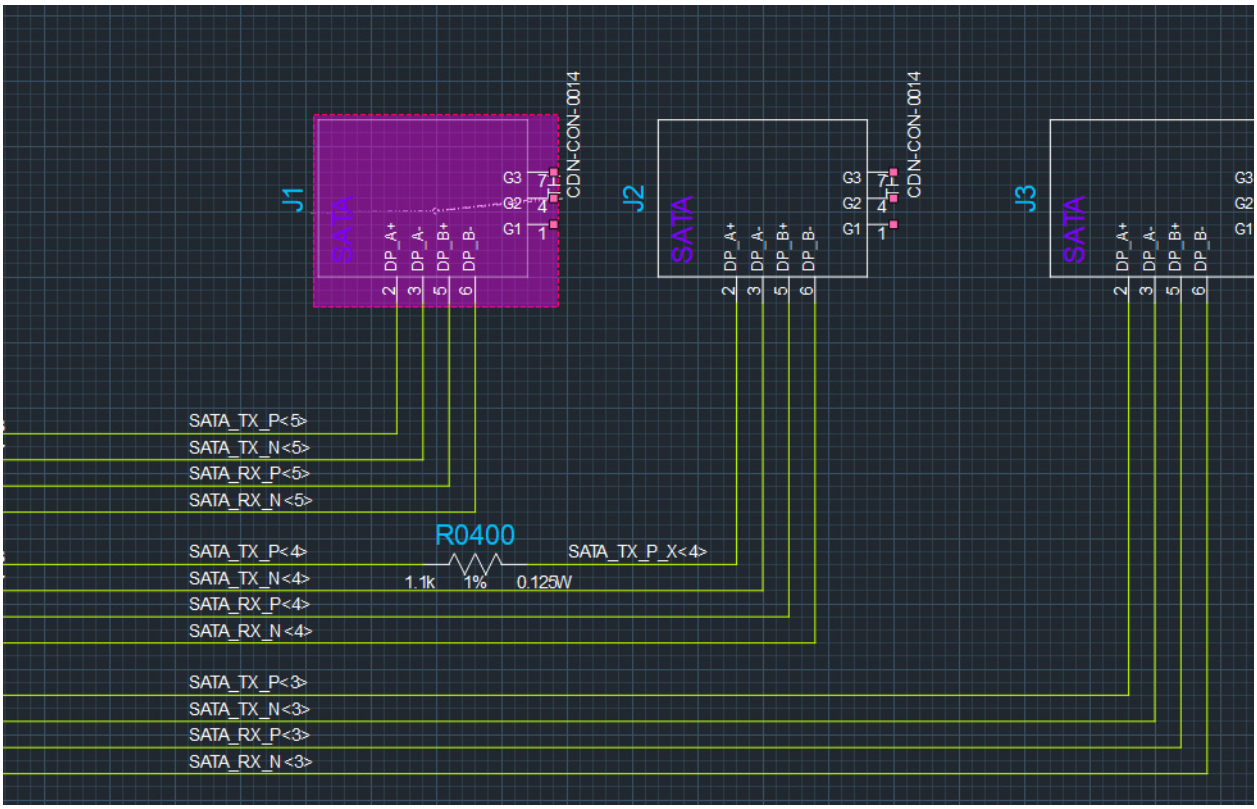
Cross-Probing between Schematic and Board

Once a schematic design is complete and is translated to a physical design in PCB Editor, you can cross-probe between the schematic and the board. System Capture and PCB Editor communicate with each other using an internal messaging system that helps in cross-probing between the two applications. Cross-probing means any component selected in one application, automatically gets highlighted in the other.

To cross-probe between System Capture and PCB Editor:

1. In PCB Editor, choose *Display – Highlight* to enable the cross-probing mode.
2. When this mode is enabled, select an instance, such as `J1` on the canvas.

   The corresponding instance is highlighted in System Capture.



3. In the same manner, in System Capture, select an instance.

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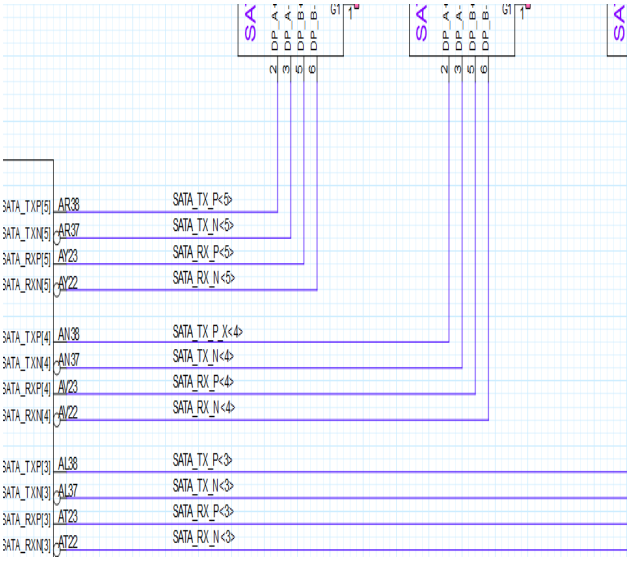
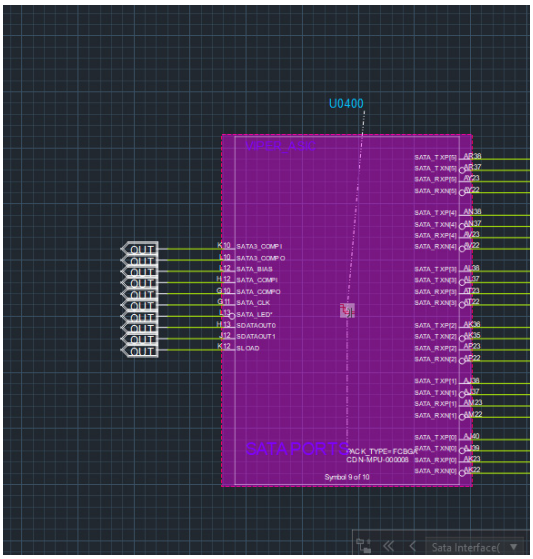
The instance gets highlighted in PCB Editor.





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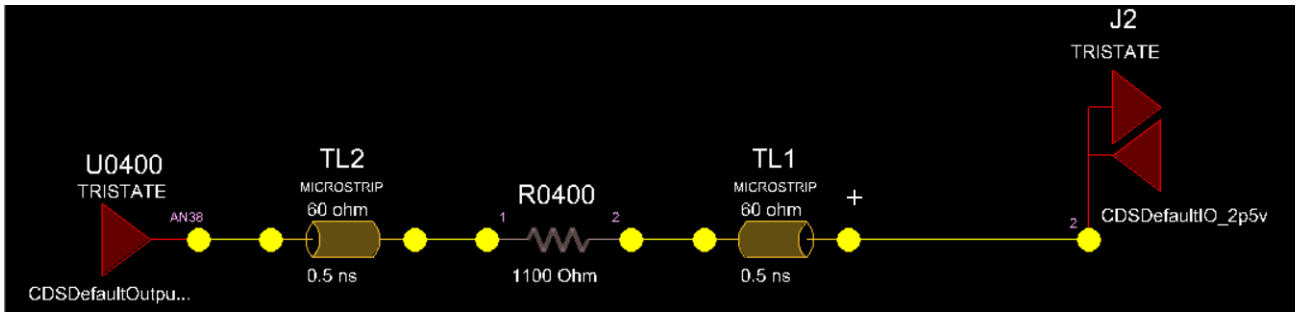
Updating the Schematic with Changes made in PCB Editor

You can also import data from the layout to bring the information around the layer stackup along with Physical and Spacing Constraints Sets (PCSets and SCSets). With this information available, you can apply Physical and Spacing Constraints in addition to the Electrical Constraints in the schematic design. The back to front flow checks the flow of constraints from the layout to the schematic and displays them in the *Constraint Difference Report* window, where you can view the changes in the database.

Any changes in the design done in the layout can be synchronized with the schematic. These changes can be to RefDes, Properties, Pin Swaps, Section Swaps, constraints, and so on. Layer stack-up definition along with Constraint Set definition for Physical and Spacing domains can also be synchronized with the schematic.



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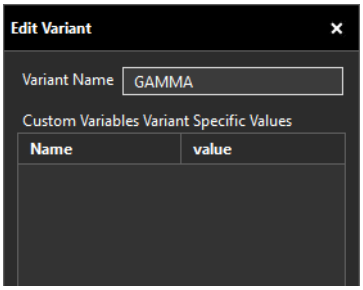
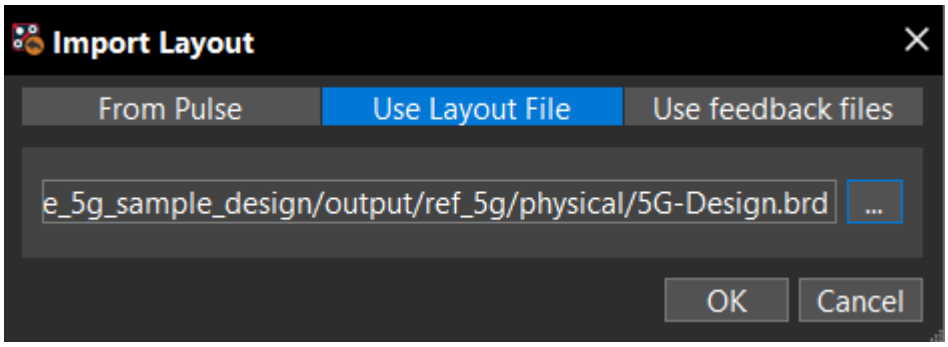
You can decide whether to accept the changes and update the schematic database. This is done in the Schematic-Board Differences window.



To update the schematic with layout changes:

1. Choose *File – Import – Layout*.

   The *Import from Layout* dialog is displayed. The last used board file is already selected in the *Use Layout File* field.



2. Click *OK* to import the changes from the board file.

   The changes from the board file are imported and displayed at the following locations:

   - Schematic-Board Differences window
   - Constraints Difference Report

3. Close the *Constraints Difference Report.*

   The schematic- board differences window shows the changes in:

   - RefDes

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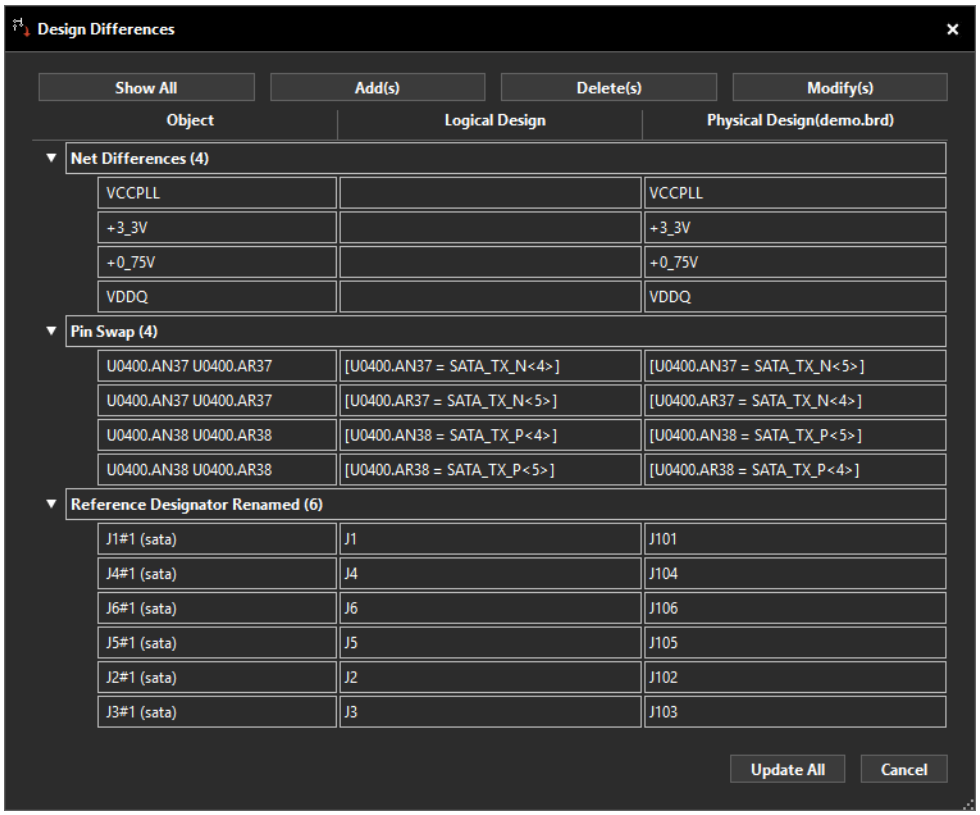
- Pin Swaps



4. Click the *Update All* button in the Design Differences window to update all the changes from the layout.

Important

If you import the layout files generated for a design after making a copy of the System Capture design with a different root design name, even if the schematic logic is the same, you will get many design differences.

Update Constraints Mode

When the layout file is synchronized with the schematic using *File – Import – Layout*, the *Design Differences* window is populated with the changes. The constraints updates work in the overwrite mode, that is constraints from the layout overwrite the schematic ones are not retained. In case you need the constraints to be imported in the changes only mode, set the following directive:

```
START_CANVAS
```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```
B2F_OVERWRITE_CONSTRAINTS 'OFF'

END_CANVAS
```

Changes-Only Mode

When constraints are transferred between the schematic and layout, checks are in place to ensure the values set in the layout (back-end) are not lost. The translation process uses a three-way comparison to move the user-specified constraints from front-to-back or back-to-front. The three places are:

- System Capture (front-end)
- Internal storage (last sync state/data)
- Allegro layout (back-end)

To understand this better, let's consider an example.

Front-to-Back Flow

1. `MIN_LINE_WIDTH` is set to 1 in System Capture

   The Export Physical command is used. The values are set as:

   - `MIN_LINE_WIDTH` = 1 in the internal storage
   - `MIN_LINE_WIDTH` = 1 in the Allegro layout design
2. `MIN_LINE_WIDTH` is changed to 2 in Allegro
3. `MIN_LINE_WIDTH` is changed to 3 in System Capture
4. Export physical is run again.

   The following values are set:

   - `MIN_LINE_WIDTH` = 3 in the internal storage
   - `MIN_LINE_WIDTH` = 3 in the Allegro layout design

Let's now see how the reverse works.

Back-to-Front Flow

1. `MIN_LINE_WIDTH` is changed to 4 in the Allegro layout design.

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2. The Import PCB Layout command is used.

   `MIN_LINE_WIDTH` is changed to 4 in System Capture

   The internal last sync state also saves `MIN_LINE_WIDTH` as 4.

Related Topics

Cross-Probing between Schematic and Board

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7

Creating Hierarchical Designs

A PCB schematic design can be one of the following two types:

- Flat Design

  In a flat design, all parts on the drawing come from libraries and are one-to-one logical representations of the physical parts. The entire interconnecting wiring within the design is entered pin-to-pin.

  Flat designs are best suited for small designs that do not have sophisticated bus requirements and do not reuse portions of circuitry. Also, if the design must be completely backannotated with pin and physical location numbers, a flat drawing is required.

- Hierarchical Design

  A hierarchical design is recommended for developing complex designs that can be organized into modules. This method is useful when the same circuit functions needs to be reused and for teamwork assignments.

  Hierarchical designs reduce the amount of data entry and interconnections required by the design, thereby reducing the chance for error.

In a hierarchical design, block symbols are created for each of the blocks representing the block. Each block symbol contains pins that are the interfaces to the block. These block symbols can be instantiated and interconnected in the design to capture design intent. A hierarchical design can have any number of levels. System Capture does not have any limitation on the number of hierarchical levels. All the connectivity and constraints captured in the block are reused in the design. When working with hierarchical designs, the following tasks are commonly performed:

- Importing a Block
- Instantiating a Block
- Viewing the Design Hierarchy
- Editing a Block

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- Adding Multiple Levels of Hierarchy
- Resolving Interface Connectivity Changes
- Creating a New Block
- Re-importing Blocks
- Reusing a Design

Importing a Block

Designs created in DE-HDL or System Capture can be imported and used in System Capture. AWR Microwave Office (AWR MWO) designs can also be imported into a System Capture design by using a unified library representation of the AWR MWO design.

All the data that is part of the source block including Sheet Titles, Packaging Information, Constraints, Block Symbol, and Variant data is also imported with the block. All this data can be reused in the target design.

If the source block does not have a Symbol view present, a schematic symbol for the block is generated. This schematic symbol is available in System Capture for instantiating the block.

Prerequisites

- As System Capture supports the *DML-independent* flow, it is important that the designs to be imported are *DML independent,* and have the same state of operation as the current design. This implies that the *XNet creation mode* is the same.
- Before you import a block in System Capture, ensure that the libraries in the source design are available to the target design.

Important

In case a block being imported contains more blocks inside it, **all** the blocks are imported along with the main block. In case any block already exists in the target design, the block is not re-imported.

To import a block:

1. Choose *File – Import – Block(s)*.

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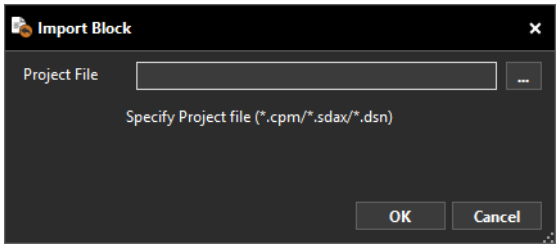
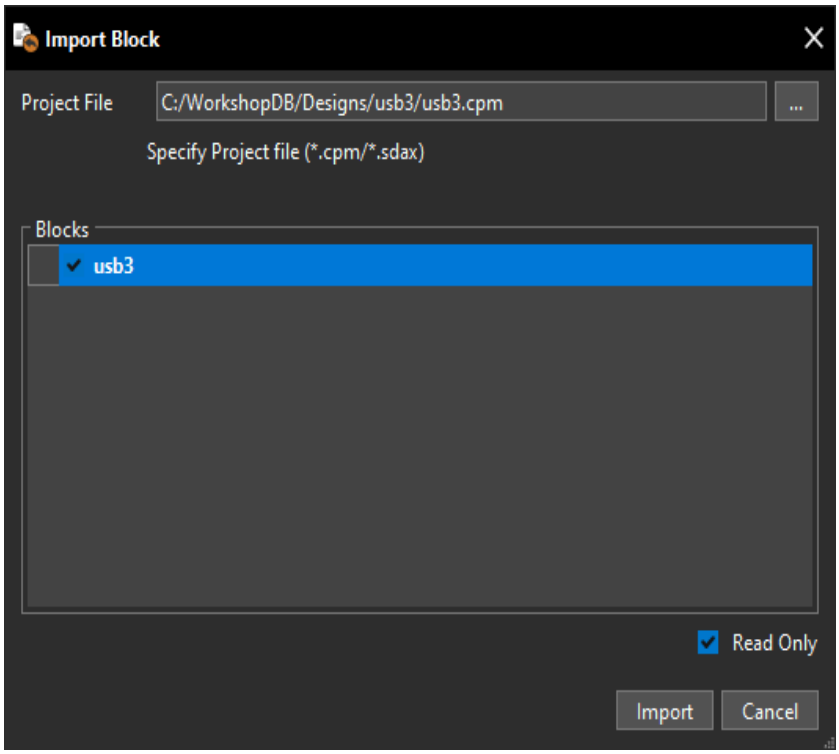
The *Import Block* dialog is displayed.



2. Browse to the project file you want to import. The project types supported are listed.

   After the project is selected, all the blocks of the project are listed.

3. Select the block to import.



   By default, the Read Only option is selected. Clear this option to ensure the block can be edited in this design.

4. Click *Import*.

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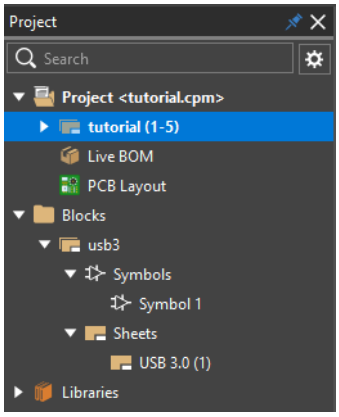
The block is imported and displayed in the *Project Explorer*.



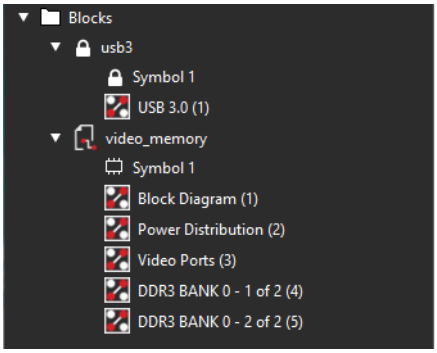
If the block is successfully imported without any errors and warning, the symbol for the block is attached to the cursor and is ready to be placed.

Tip

The log file is generated in `<project>/temp/import_block.log`. If needed, you can check the changes made by the import process.

Important

When you import a System Capture block, you can import the block as a non-editable block or an editable one. Select the *Read Only* check box to ensure no chances are made in the target design.



A lock icon shows for the newly added block and its symbol. You can unlock the symbol and edit it without making changes to the rest of the block.

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Related Topics

- Instantiating a Block
- Importing RF Design in Allegro System Capture

Instantiating a Block

After the block is imported, you can instantiate it in the design. On adding a block instance to the design, you are prompted to set the packaging options for the block in the *Packaging Options for Block* dialog.

In this dialog, you can provide a name to the block instance for easy identification. You can also decide how the instances from this block are to be packaged with respect to the top-level design. There are multiple options that the tool provides:

- *Optimized*
- *Prefix*
- *Suffix*
- *Offset*
- *Pattern*
- *Range*

These options cover all possible ways to configure the RefDes for a block. Apart from this, you can configure how the *Global Signals* from the block appear in the top-level design. You can use the global signals from the block as it is, or alias them to signals in the top-level design to control the scope of these signals.

To instantiate a block:

1. Right-click the block in *Project Explorer* and choose *Place – Schematic Block* from the pop-up menu.

   The block is attached to the mouse pointer.

2. Click the page where you want to instantiate the block on the page.
3. Click anywhere on the page to place the block symbol.

   The *Packaging Options for Block* dialog pops up.

4. Change the name of the block instance.

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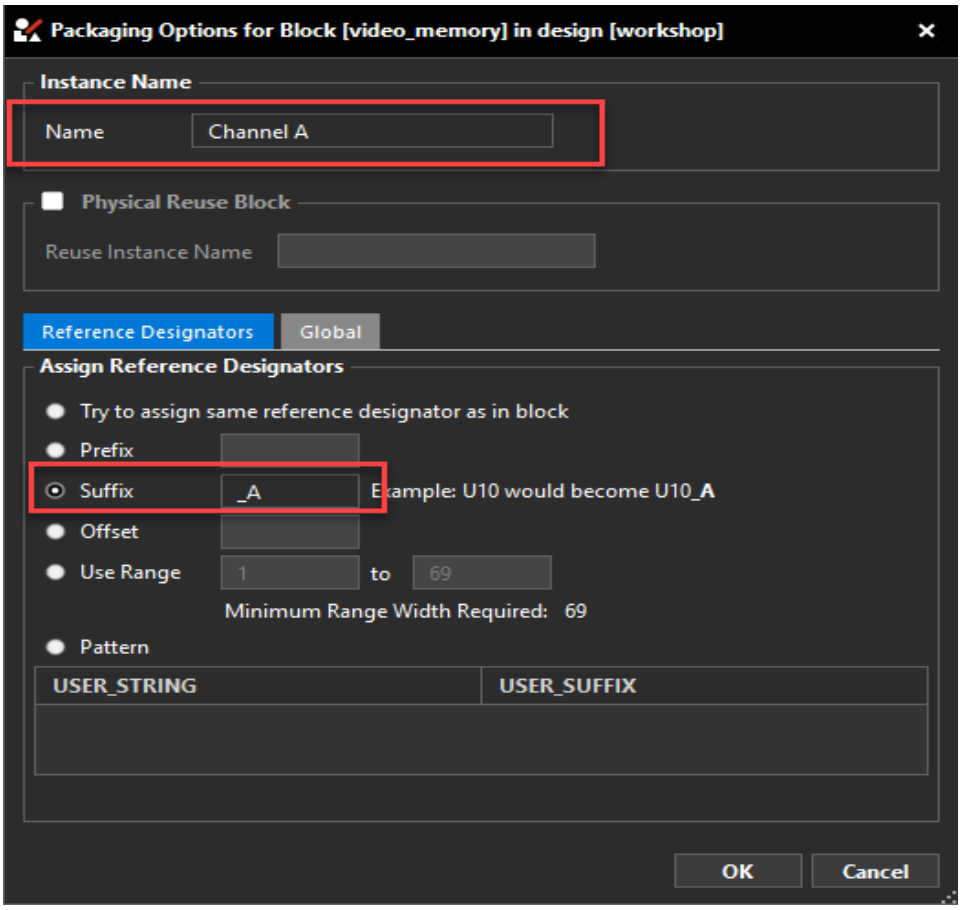
For example, from `video_memory to` *Channel A*.

5. Select the *Suffix* option and assign a suffix for instances of this block.

   For example, suffix of `_A` to the RefDes from the block.



6. Click *OK* to place the block on the schematic sheet.

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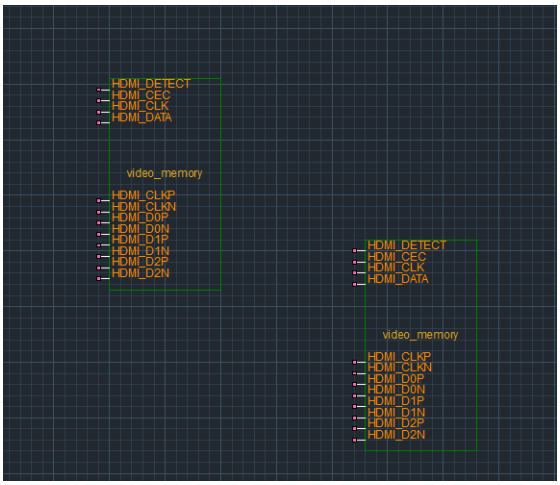
Another instance of the block is now attached to the cursor for placement.



7. Place another instance of the block and specify the following attributes in the Packaging Options for Block dialog:

- ❑ Bock instance name: *Channel B*

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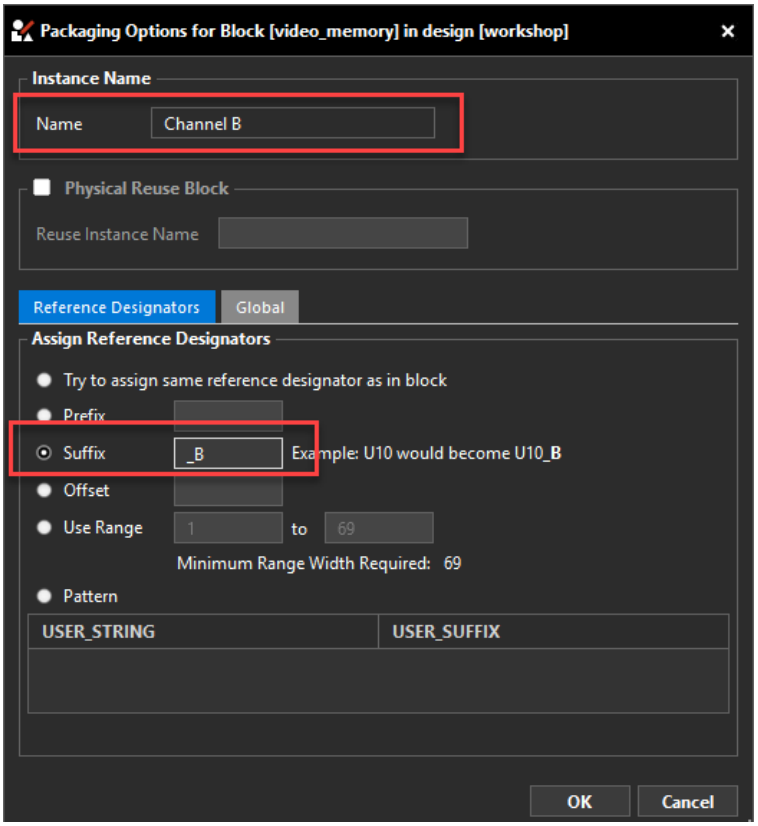
- Reference designator suffix: `_B`



8. Click *OK*.
9. Right-click and choose *Done* to complete the placement of the block symbols.

The prefix or suffix applied to a block also gets applied to the physical net names for nets or buses in the instance.

Related Topics

Viewing the Design Hierarchy

Viewing the Design Hierarchy

The Project explorer shows the blocks instantiated in the design along with their block instance names. When you click any block name, the sheets of that block are shown in a window where the view can be either a thumbnail or a list view. You can open a schematic sheet in the context of the root level design.

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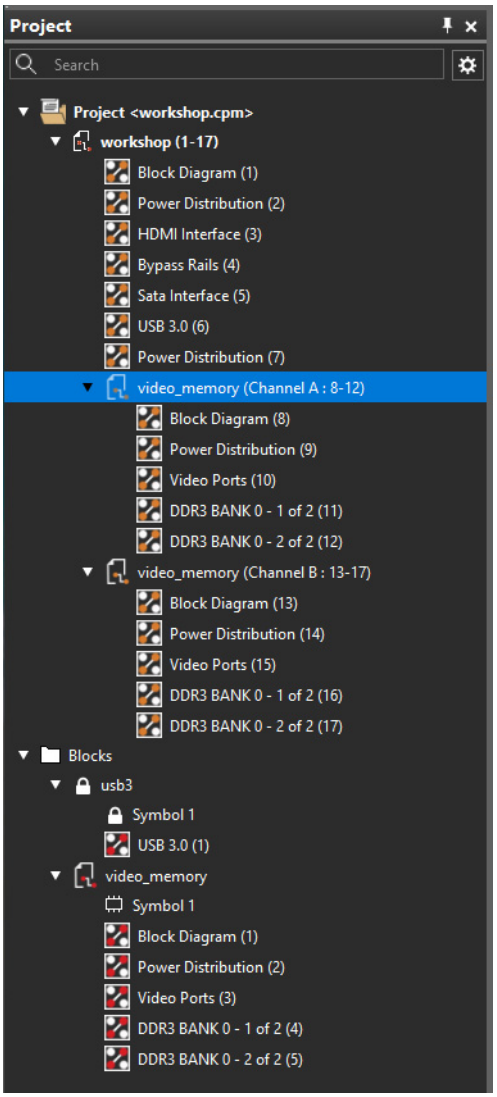
1. View the design hierarchy.

.



The imported blocks are displayed, and all the sheets of the block instances can be seen.

2. In the block *video_memory(Channel A)*, click the schematic sheet *Video Ports(10)* to open it.

3. Zoom in to view the reference designator of the *VIPER_ASIC* component.

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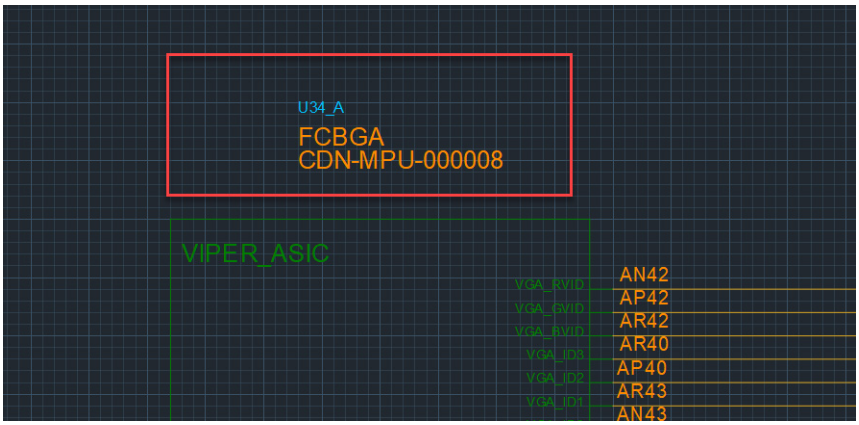
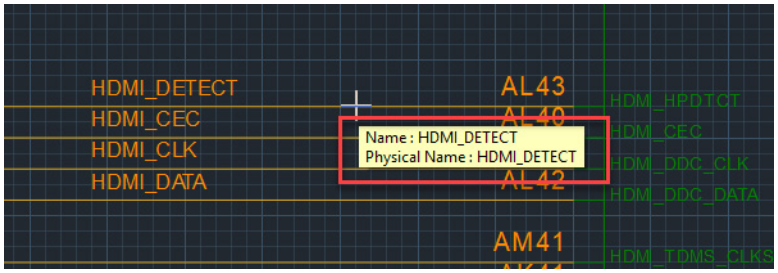
It has a suffix of *_A* attached to it, which was specified while defining Packaging Options for the block instance. As this property is modified at the occurrence level, it is displayed in Blue, which is different from the default color for displaying a property.



The physical net names of the signals have the same suffix attached to them.



4. Back in the HDMI Interface sheet of the root design, add the *HDMI* connector component, and connect it to the instance of video_memory block with name Channel A.

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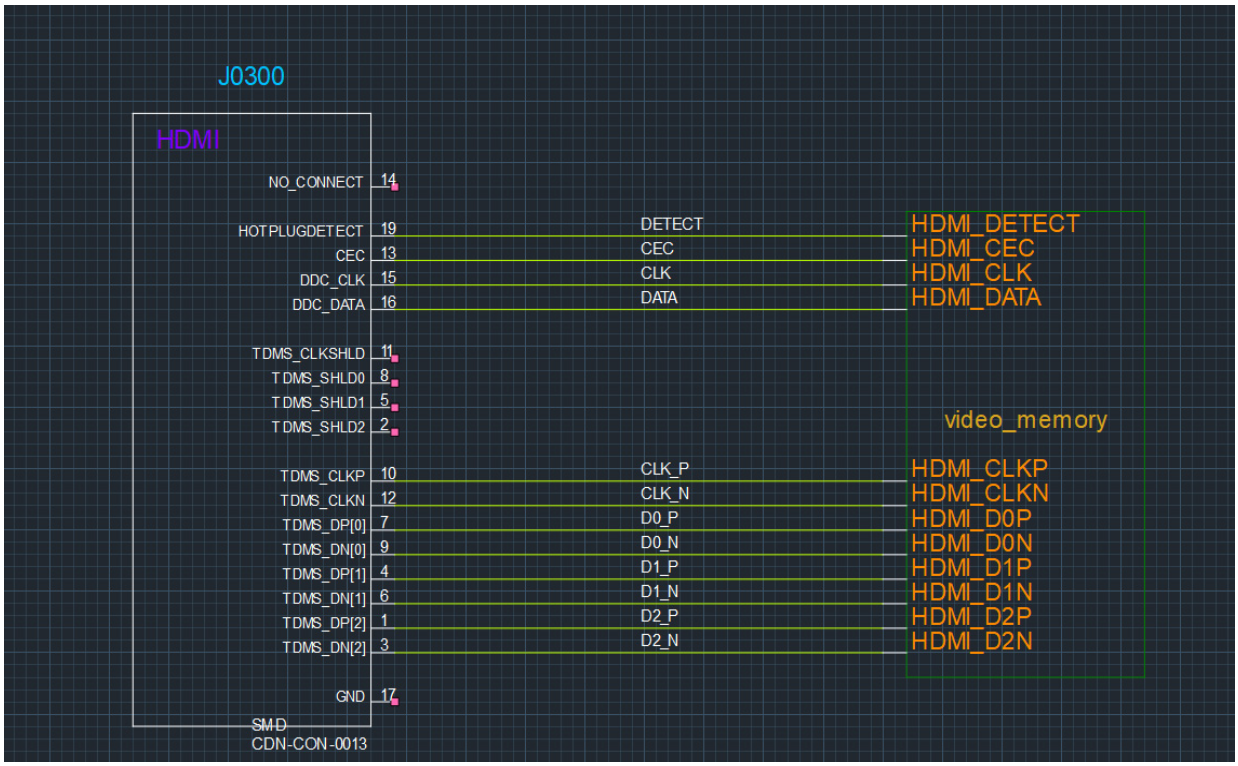
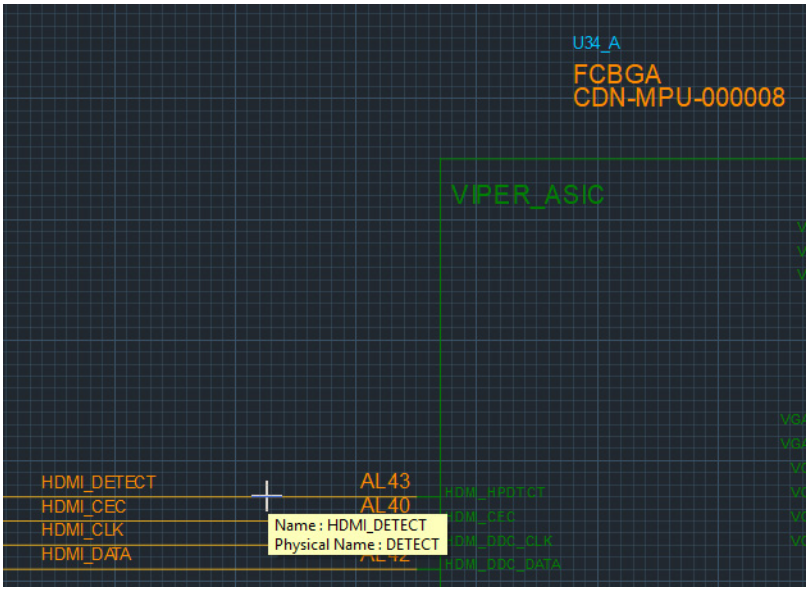
5. Assign names to signals as illustrated in the following screenshot.



6. In the Hierarchy viewer, click the *Video Ports(3)* sheet for the video_memory (Channel A**)** block, check the physical net names:



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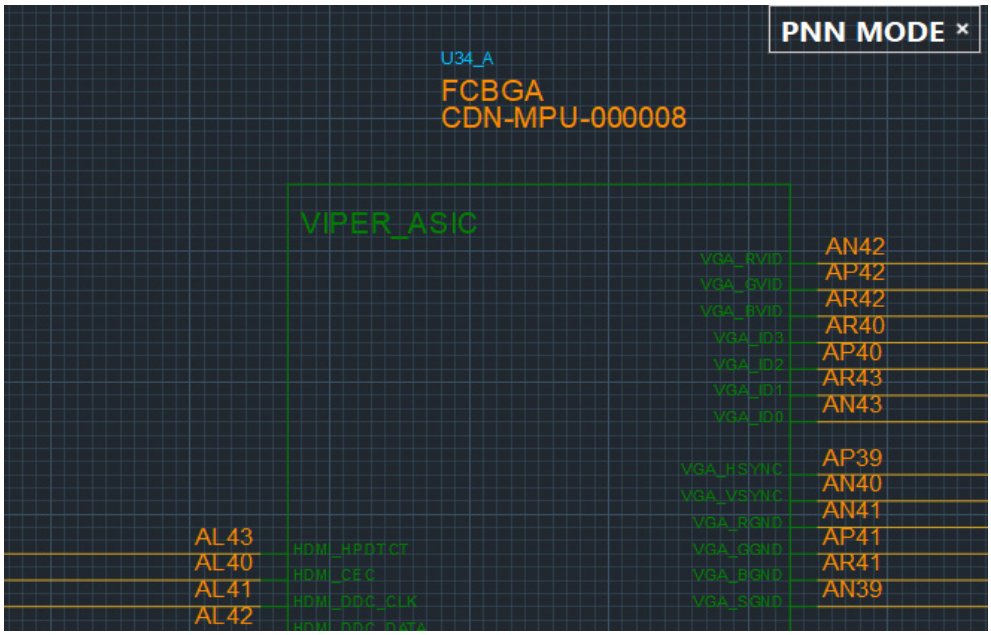
You can also choose the *View – Physical Net Names* menu command to view the Physical Net Names on the nets. This command gets you into the *PNN mode* where by the Physical Net Names for all the nets in the design are displayed instead of the Logical Net Names. Also, on the top-right corner of the schematic sheet appears the *PNN Mode* visual indicator. You can click the close (x) mark on the indicator to get out of the PNN mode.



Reordering Blocks

You can modify the order of blocks under same hierarchy. The changed order applies to PDFs created or print outs. The order of pages in the *Project Explorer* pane defines how pages are numbered. Hierarchical design blocks can have multiple instances and they get listed in order they get added. By default, schematic sheets of the top-level design are always placed first and after that sheets from block instances are configured. Any changes made are immediately reflected in the:

- Project Explorer
- TOC
- Print Preview
- PDF generated
- Page Tab
- Page numbers

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- Navigation links
- Custom Variables

Caution

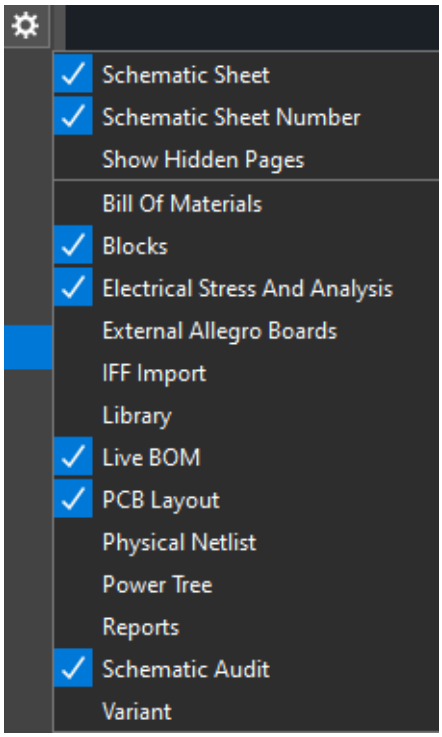
The changes made in block order cannot be undone or redone.?

Prerequisites

- Set the following directive in the project cpm or `site.cpm`:

```
START_CANVAS
MODULE_ORDERING 'TRUE'
END_CANVAS
```

- Ensure blocks and pages are displayed in *Project Explorer*



To change the sequence of blocks, perform these tasks in the Project Explorer.

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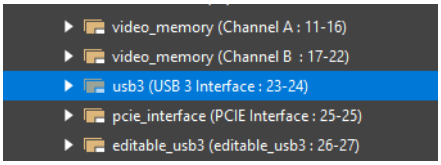
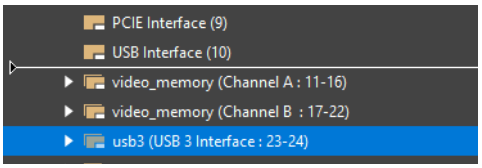
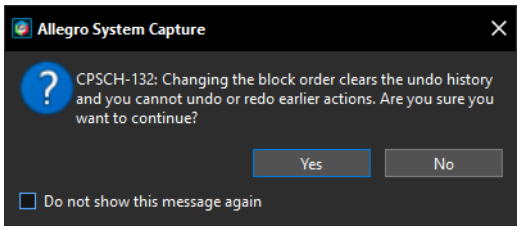
1. Click the block.



2. Drag and drop to the required location.

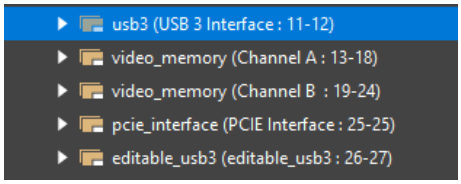


A reminder shows that these changes cannot be undone.



3. Click *Yes* and choose the check box to disable this messages.

   The block moves to the new location and the page numbers change to reflect the new location. For example, usb3 has moved up the design in the images and the page numbers have changed from 23-34 to 11-12.



Related Topics

Adding Multiple Levels of Hierarchy

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Editing a Block

The schematic sheets for a block can be opened in two modes for editing:

- Master Mode
- Occurrence or In-Context Mode

You can perform various operations on the blocks you instantiated in the design at these two levels.

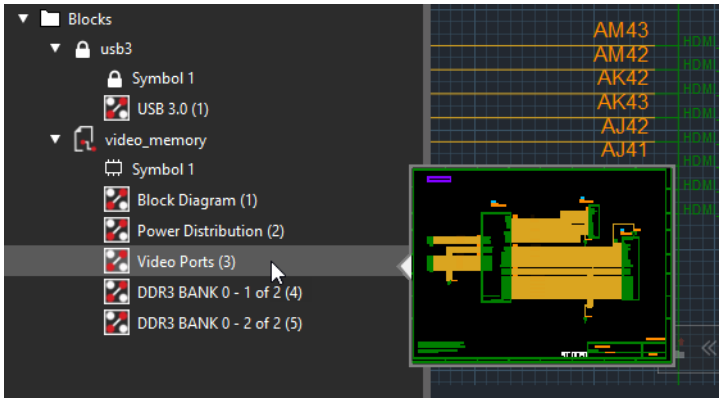
Master Mode Operations

You can open the schematic sheets of a block in the *master mode* from the *Project Explorer* where each block and its contents are listed. Any change made to the schematic sheet in the master mode is available on the schematic sheet in all occurrences or instances of the block. Change in connectivity and visibility or formatting of objects are all master mode operations, and these changes are visible on all instances of the schematic sheet.

Note: Even if the master mode operations are attempted in the occurrence mode or the in-context mode, they are treated as master mode changes and are available on all instances of the schematic sheet.

To edit the design in the master mode:

1. In the *Project Explorer*, click the *Video Ports* sheet for the `video_memory` block. This opens the schematic sheet for editing.



2. Click the component with reference designator `U34` and add a property *VALIDITY* with the value as *VALIDATED*.

3. Change the Visibility of this newly added property to *Name & Value* so that it is visible on the canvas.

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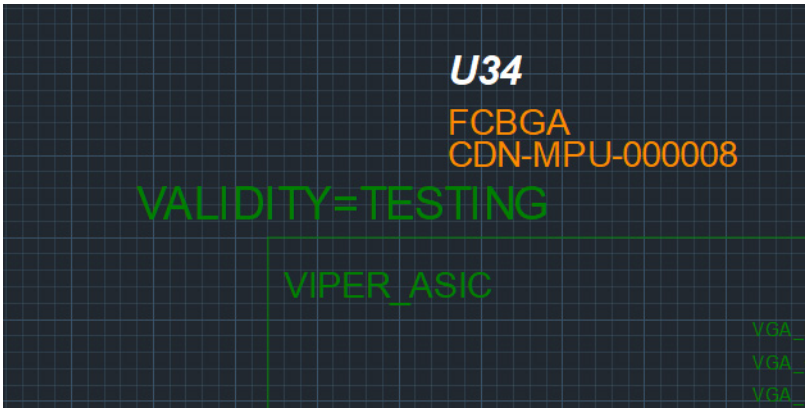
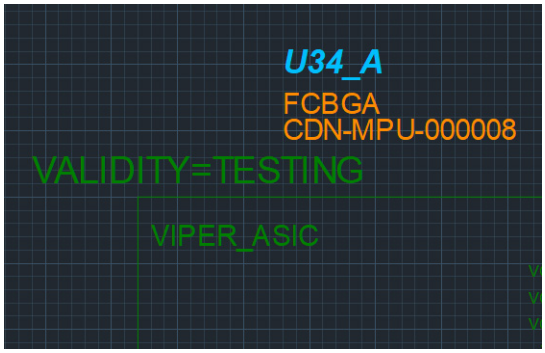
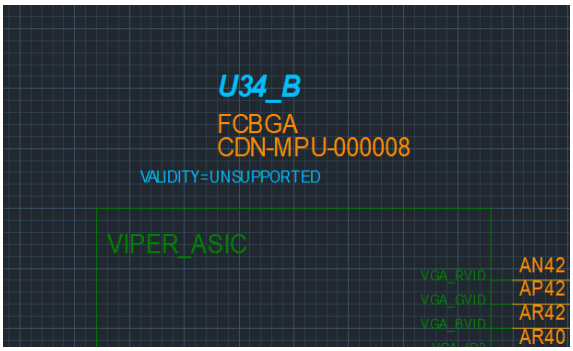
4. Move the text towards the top of the component.



Both instances of the block reflect the change made to the block in the master mode.





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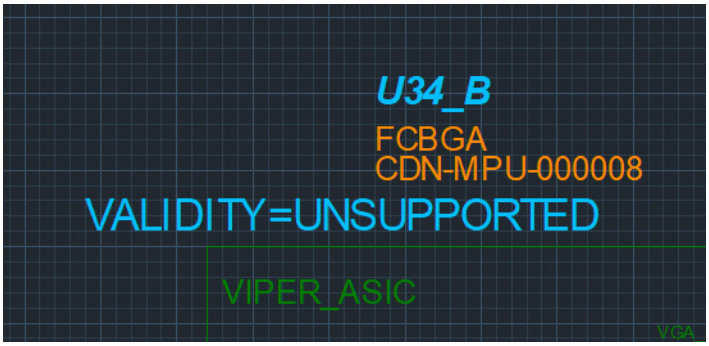
Occurrence Mode Operations

Schematic sheets of a block are opened in the *occurrence mode* from the *Project Explorer* where each block instance along with its contents is listed. The only change that can be done in the context of the root design is the change in properties. The in-context changes are stored as part of the root-level design and are done for a specific instance of the block. The in-context changes are not visible in other instances of the block as these changes are done only on opening the schematic sheet specific to a block instance. The property value that is the same in master and occurrence is displayed in the same color, but if the property has been modified in the occurrence mode, it appears in a different color indicating that it is an occurrence property.

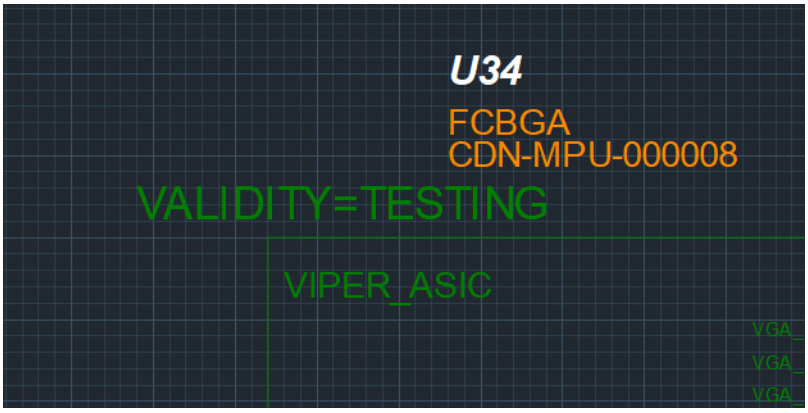
To edit the design in the occurrence mode:

1. Open the sheet for the block instance *Channel B* and change the value of the *VALIDITY* property from *VALIDATED* to *UNSUPPORTED*.

   With this change the property is now displayed in a different color.



2. Open the *Video Ports* sheet for the `video_memory` block, and change the value of the VALIDITY property to *TESTING*.



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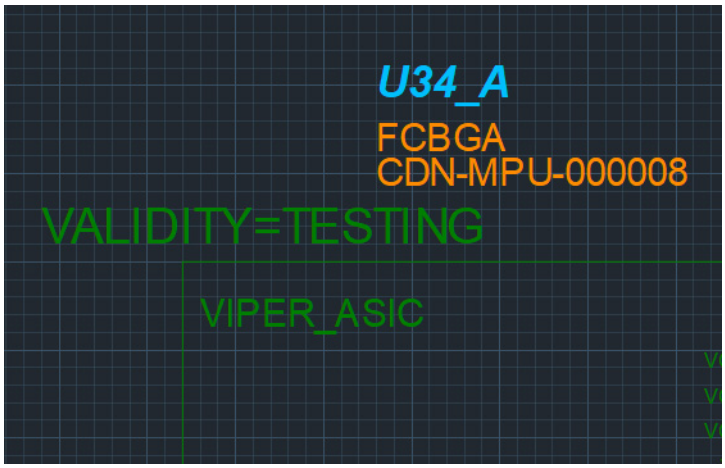
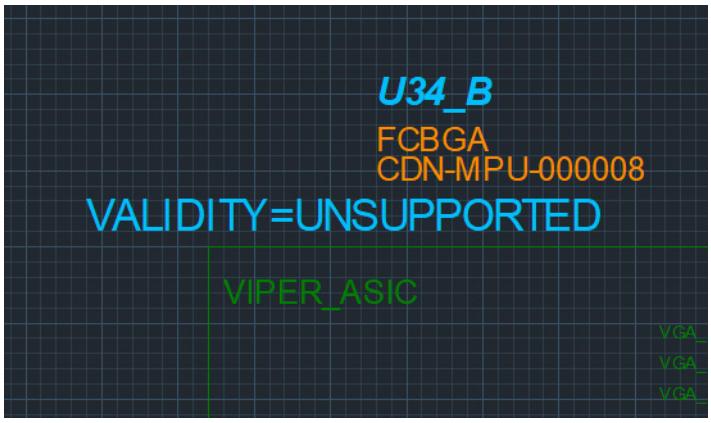
The value of the VALIDITY property is changed for block instance, *Channel A*.



While the block instance *Channel B* remains unchanged.



3. Delete the VALIDITY property on this instance.

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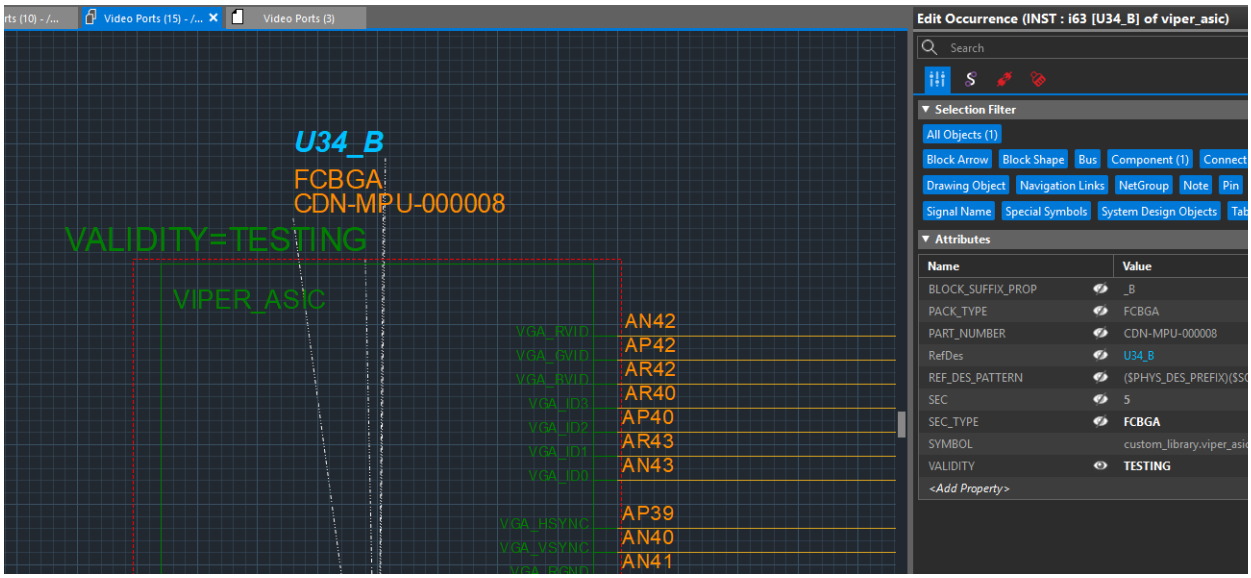
As soon as the VALIDITY property with the value change in the occurrence mode is deleted, the VALIDITY property from the master mode starts to show up on this block instance.



Related Topics

- Adding Multiple Levels of Hierarchy
- Resolving Interface Connectivity Changes

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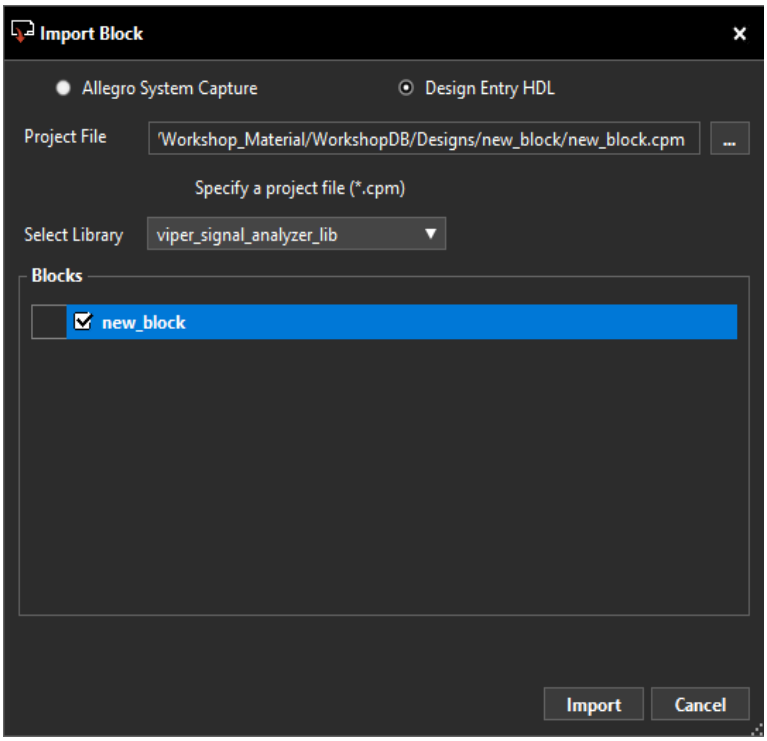
Adding Multiple Levels of Hierarchy

System Capture supports multiple levels of hierarchy. There is no limit on the number of levels of hierarchy. The packaging options specified at the time of adding the block are honored at each level of hierarchy. The final RefDes that you get is a completely resolved RefDes for the part.

To add blocks to a design:

1. Import another block, *new_block*, from the design named, *new_block.cpm*.



The new_block has been imported and is now part of the working library. It needs to be added to the video_memory block.

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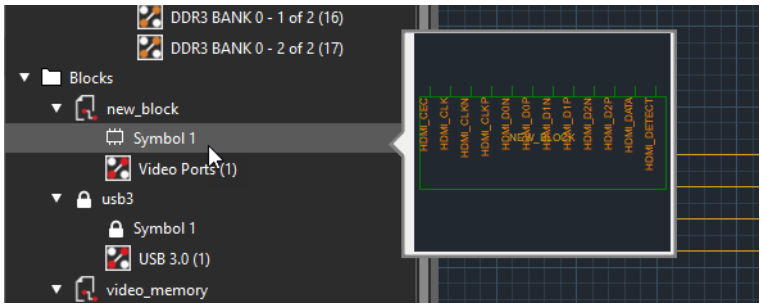
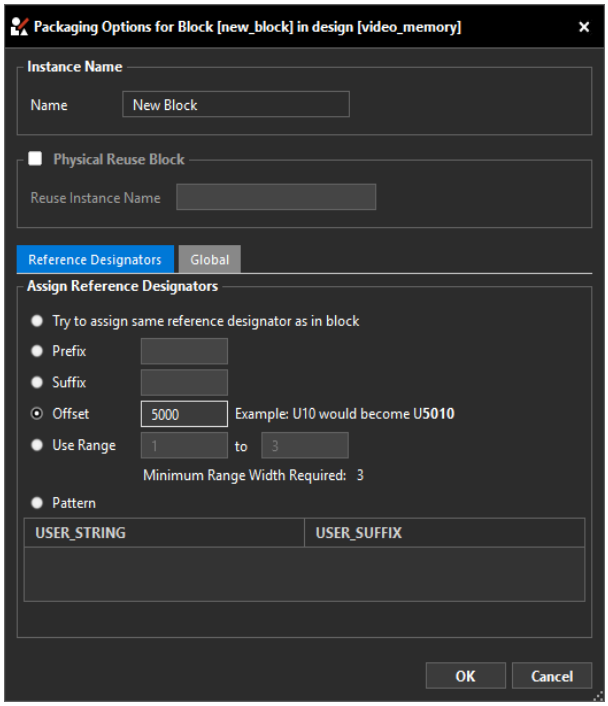
2. Instantiate the block.



3. Click anywhere on the *Video Memory* page of `Channel B` to place the block.

   The *Packaging Options for Block* dialog opens.

4. Specify the block *Instance Name* as *New Block* and the *Offset* as *5000*.



   All the RefDes from the block will have 5000 added to it to create RefDes at this level of hierarchy.

5. Click *OK*.

   The instance is added to the schematic sheet.

6. Right-click and choose the *Done* command to get out of the block add mode.

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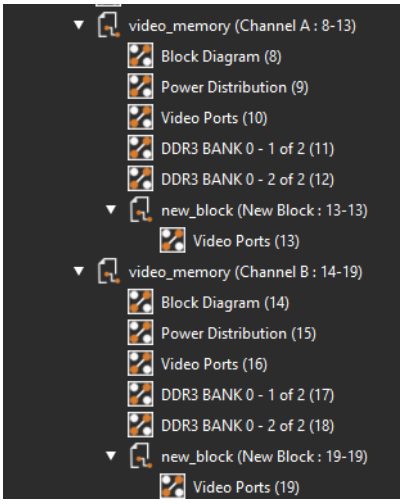
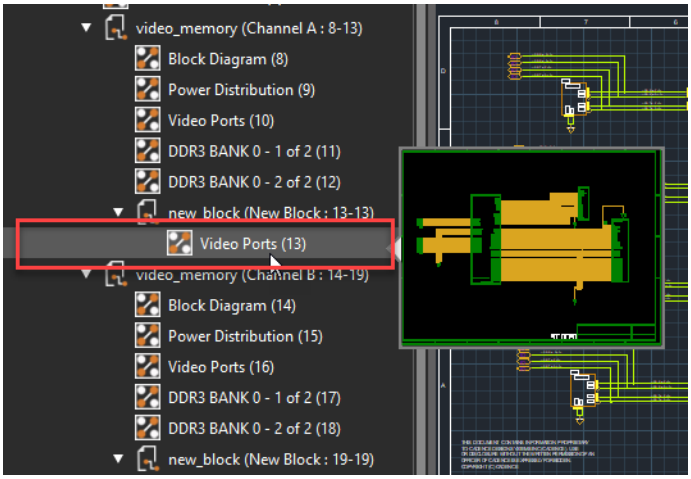
In the Hierarchy viewer, the **new_block** instance is added to both the instances of the **video_memory** block.



7. Open the schematic sheet for the newly added block, NEW BLOCK under the Channel A of video_memory block.



8. Zoom in to view the reference designator of the component.

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Observe that first the offset of 5000 is added to the RefDes from the new_block, and on the resultant value, a suffix of _A has been applied.

Related Topics

- Viewing the Design Hierarchy
- Working with Hierarchical-Split Symbols

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Resolving Interface Connectivity Changes

Any change in the interface definition of a block is treated as a master mode change and is applicable to all the instances of the block.

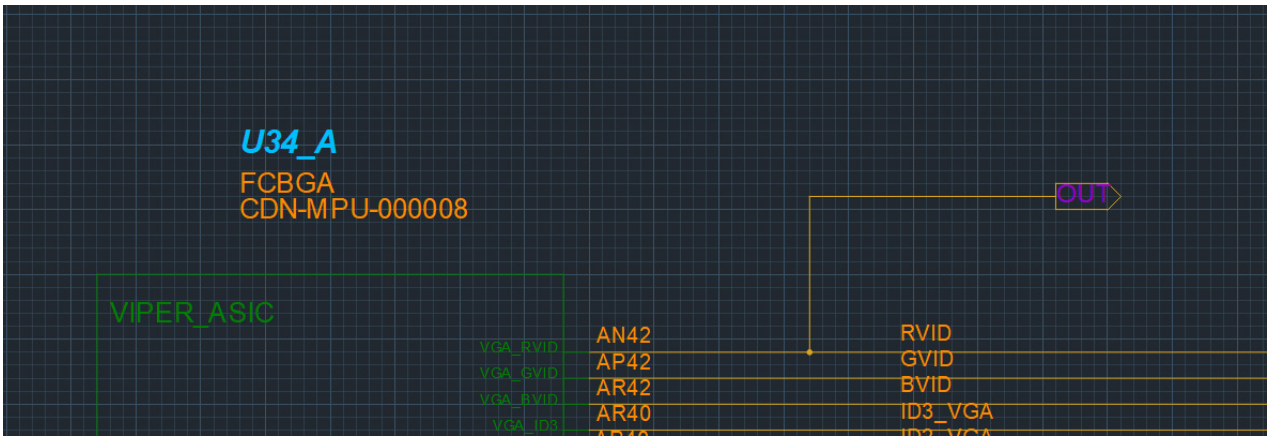
Important

Regardless of whether you have opened the schematic sheet in the master or occurrence mode, interface changes are treated as master changes.

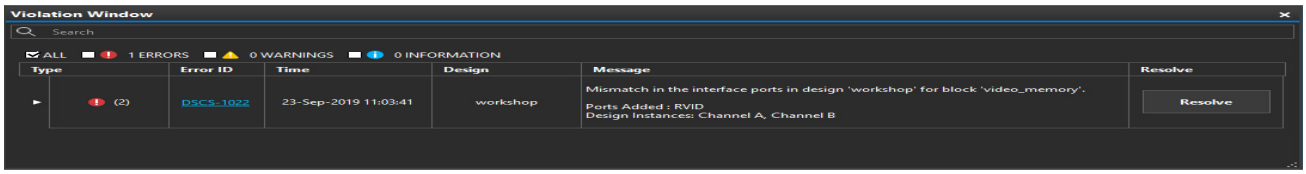
For example, in the *video_memory* block, add new interfaces by drawing wires and adding port symbols to the wires to define interface ports.

1. In the *Video Ports* schematic sheet for *Channel A*, make some interface changes as illustrated in the following screenshot:

   Add an Out port from the Special Symbols panel to *RVID*.



   The moment a change is made in the interface or an interface mismatch is detected between the contents of a block instance and the block symbol, a violation message is generated in the Violation Window.



2. Add another port as illustrated in the following screenshot:

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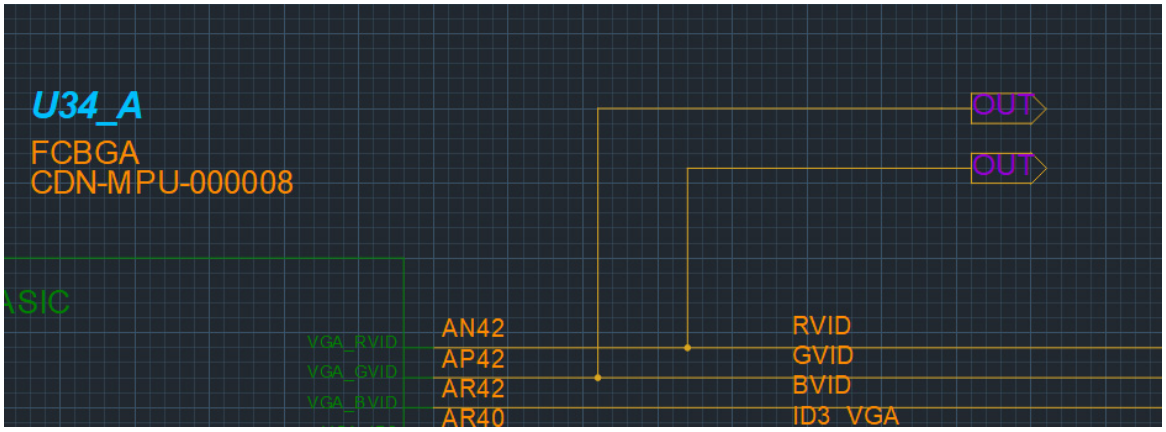
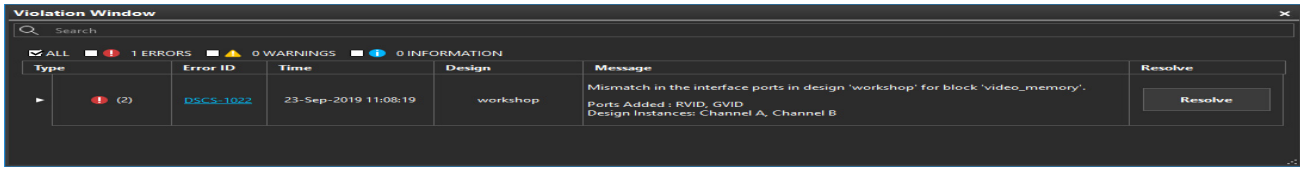


The interface mismatch results in an updated violation message:

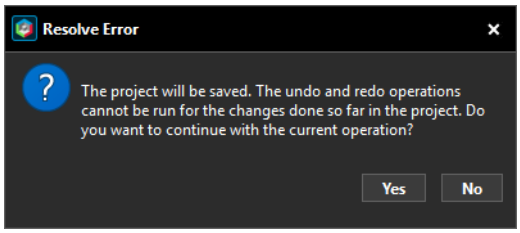


You can resolve the violations by clicking the *Resolve* button in the Violation Window. To resolve the reported violations, the block symbol has to match the schematic data.

Note: In case only ports are deleted from the block, the tool deletes the extra ports from the block symbol and updates all the instances of the block.

3. Click *Resolve*.

   A message might remind you that the design needs to saved.



4. Click *Yes* in the confirmation message box, if prompted.

   System Capture updates the block symbol and the two ports that have been added appear on the block symbol. The block symbol is validated against the schematic again.

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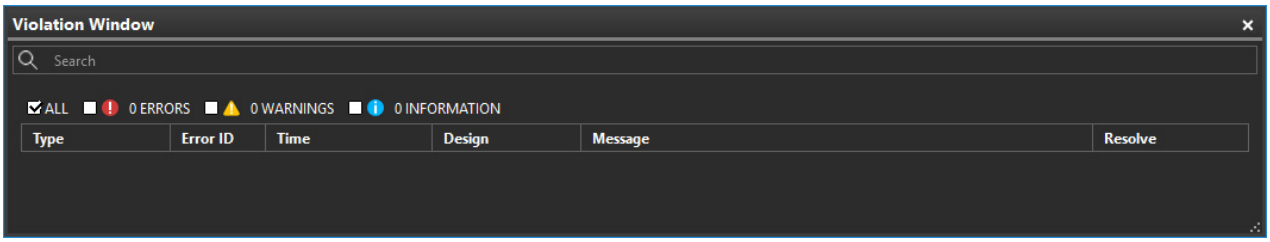
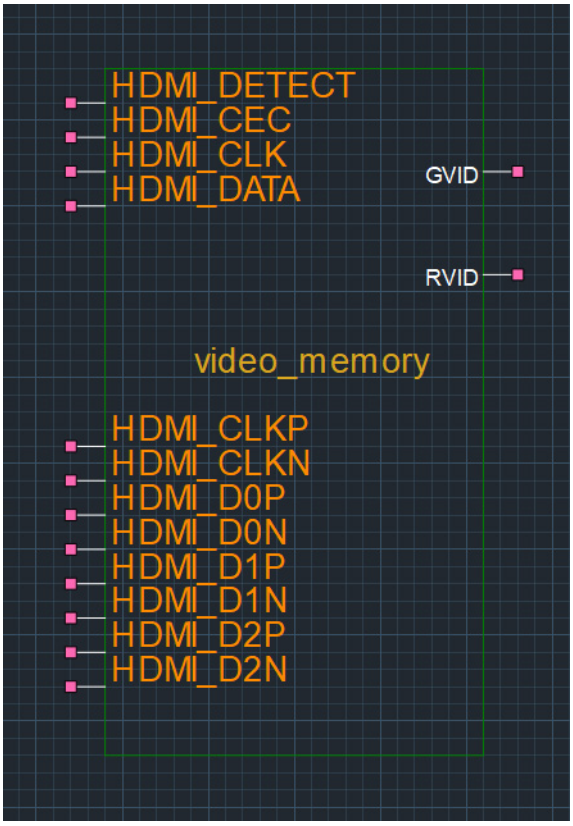
If all the mismatches are resolved, the violation message is removed from the *Violation* Window.



The block is updated.



You can edit the block symbol and move the ports to desired position on the symbol.

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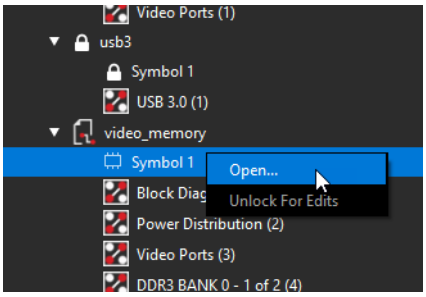
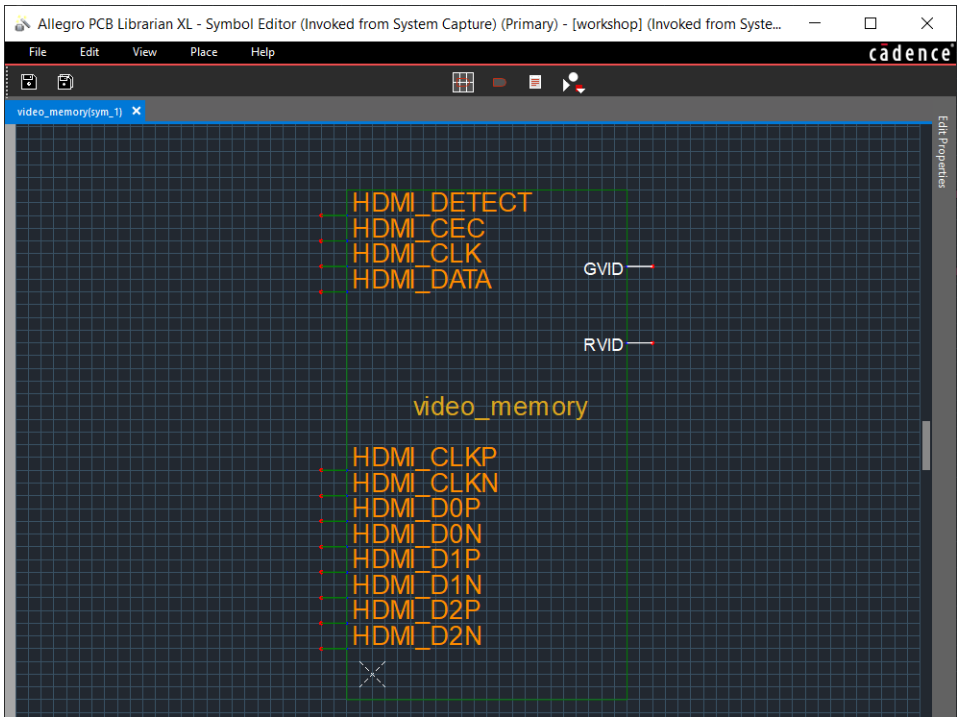
5. In the *Project Explorer*, right-click *Symbol 1* under the *video_memory* block and choose *Open*.



Allegro PCB Librarian XL – Symbol Editor launches and displays the *video_memory* block symbol.

The newly added pins appear on the edge of the block symbol.



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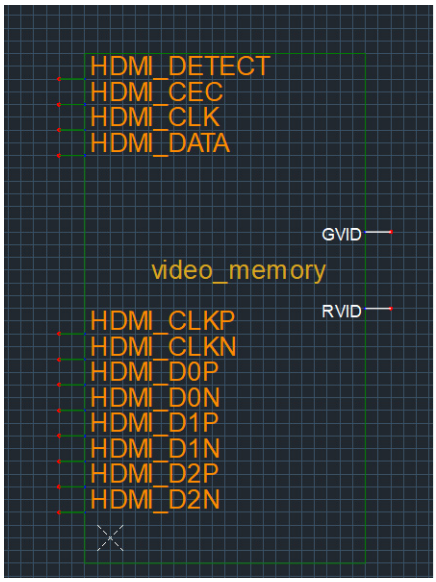
6. Move the newly added pins and place them at the desired location.



You can select any text on the symbol and change it by double-clicking on it and editing it right there (in-place editing). You can change the color and size of the text using the right-click pop-up menu.

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7. Change the video_memory text as illustrated in the following screenshot:

8. Choose *File – Save* and then close *Symbol Editor*.

When you save the symbol, the block symbol is validated against the schematic again.

The block symbol is updated in all the instances on the schematic. This ensures that the change in the port location does not lead to any change in the connectivity of the design.

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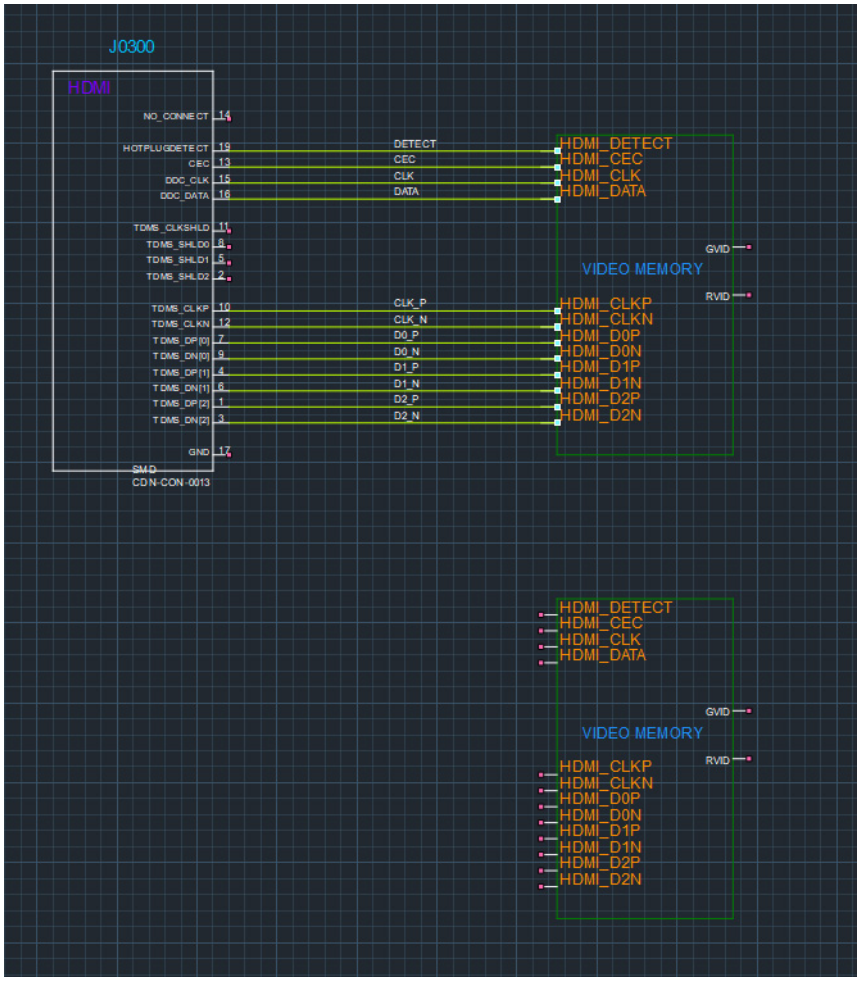
If required, the wires are redrawn to the new pin location to ensure that the connectivity is maintained.



Related Topics

Editing a Block

Creating a New Block

You can create a new *hierarchical block* in System Capture. A newly created block is a blank block with a single schematic sheet in it. The block symbol for the new block is also generated. This is just a rectangular symbol without any interface ports.

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You can open the schematic sheet of the new block and add connectivity to it. Any interfaces to be exposed can be defined by adding *Interface Ports* to the nets.

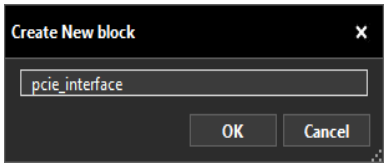
When the connectivity of the block is complete and the block is added to the design, any interface mismatch between the block and its symbol are reported in Violation Window. The *Resolve* button in Violation Window lets you resolve the interface mismatches and provides you the ability to update the symbol. After the symbol is updated, it can be saved and the new symbol is automatically refreshed on the schematic canvas.

To create a new block:

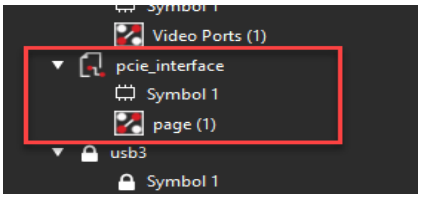
1. Choose the *File – New – New Block* menu command to create a new block.

   The *Create New block* dialog is displayed.

2. Specify the new block name as *pcie_interface.*
3. Click *OK*.



   A new block named *pcie_interface* is created and is available in the *Project Explorer*.



   Note that the block has one schematic sheet and the symbol for the block is available.

4. Rename the page(1) of the block as *PCIE Interface*.
5. Open the page for editing connectivity.
6. On this page, capture the PCI Interface performing the following steps:

   a. Add one instance of *symbol 10 to symbol 3* of component *custom_pcie8* available in the library named *connector*.

   b. Ensure that the RefDes is visible for each of the instances.

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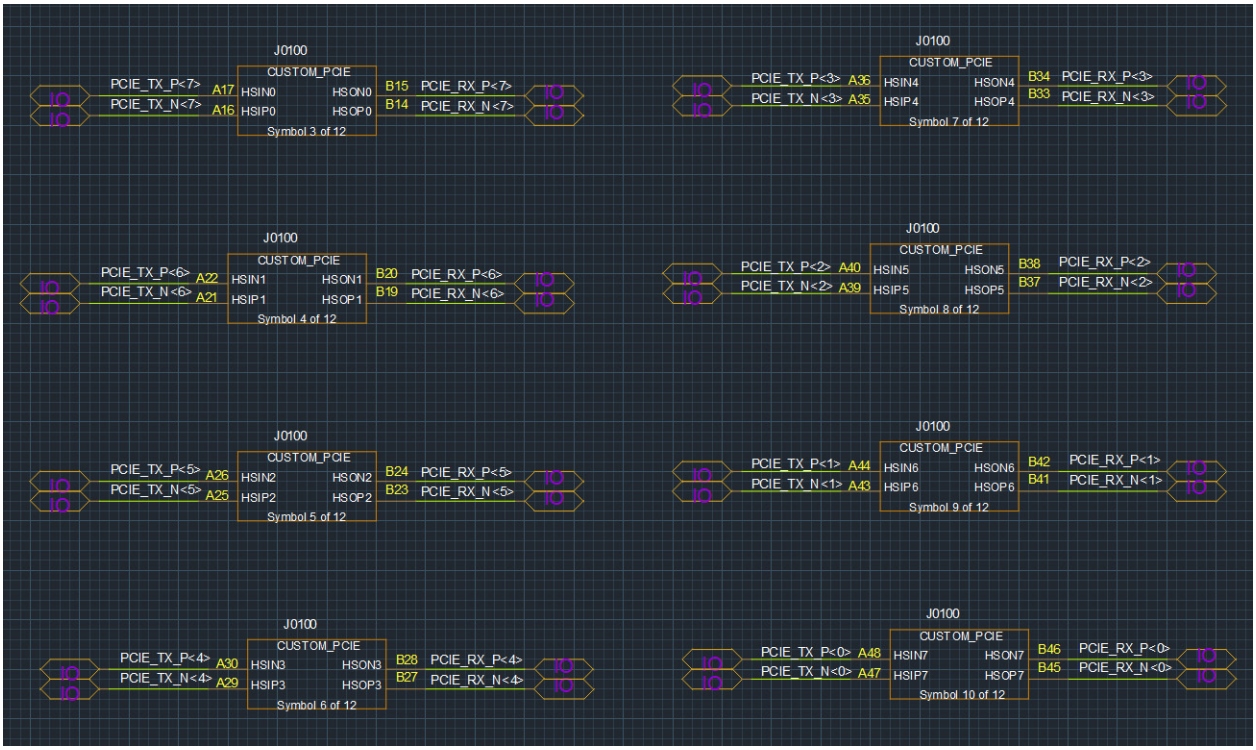
c. Draw wire stubs for each of the components and name the signals on the left side as *PCIE_TX_P<n>* and *PCIE_TX_N<n>*, and those on the right side as *PCIE_RX_P<n>* and *PCIE_RX_N<n>*, where <n> decrements from <7> to <0>.

You can use the `PCIE_NetName.txt` file present in the *`WorkshopDB/NetNameFiles`* folder.

d. After the signals are captured, connect IO Ports on each of them.



7. Save the project.

Since new interfaces have been added to the block, we should refresh the block symbol.

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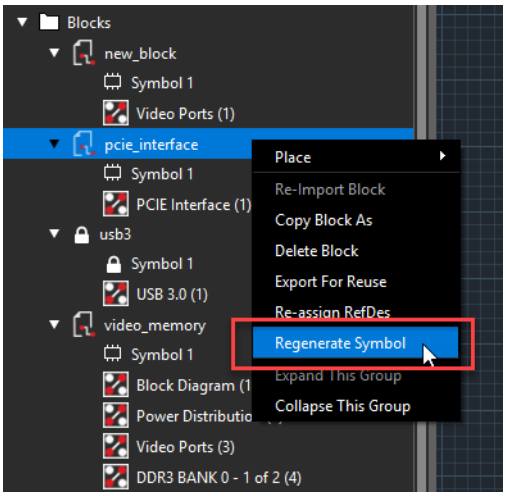
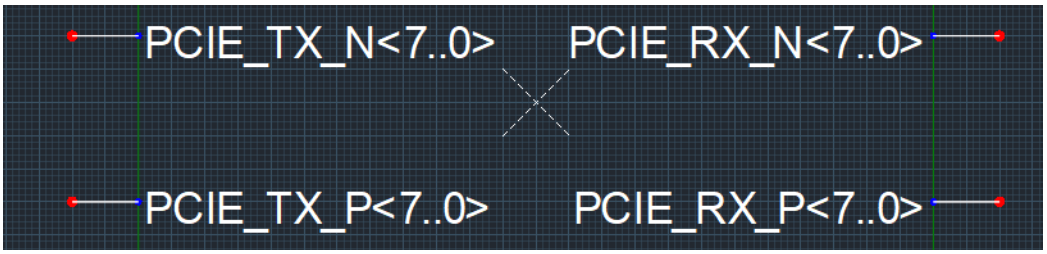
8. In the *Project Explorer*, right-click the block *pcie_interface* and select the *Regenerate Symbol* command.



The block symbol has now been refreshed and new ports have been added.

9. Open the block symbol for the *pcie_interface* and edit it to make it look like the following screenshot.



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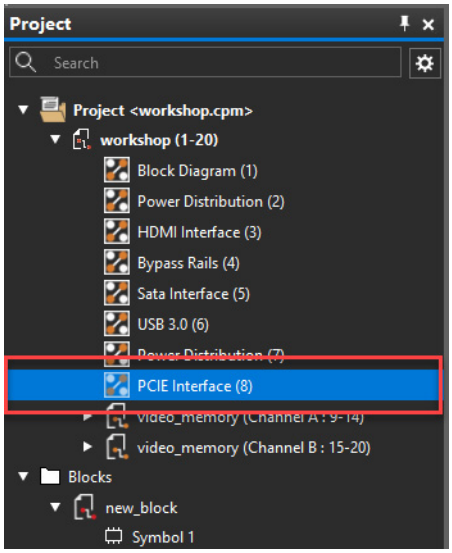
10. Insert a new schematic sheet at the end for the PCIE Interface sheet, and name it as *PCIE Interface*.



11. Add the block symbol of the *pcie_interface* block on this newly added schematic sheet.

The Packaging Options dialog is displayed.

12. Specify the *Instance Name* as *PCIE Interface*.

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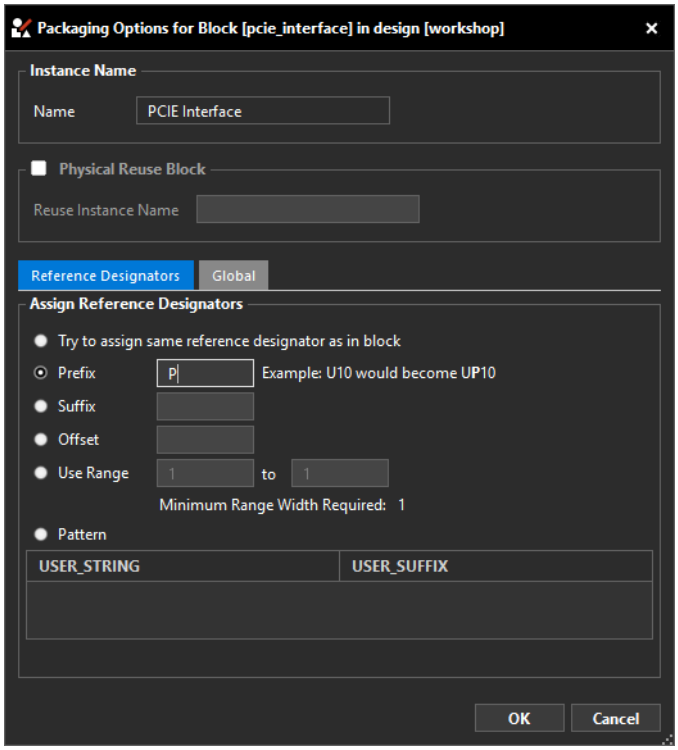
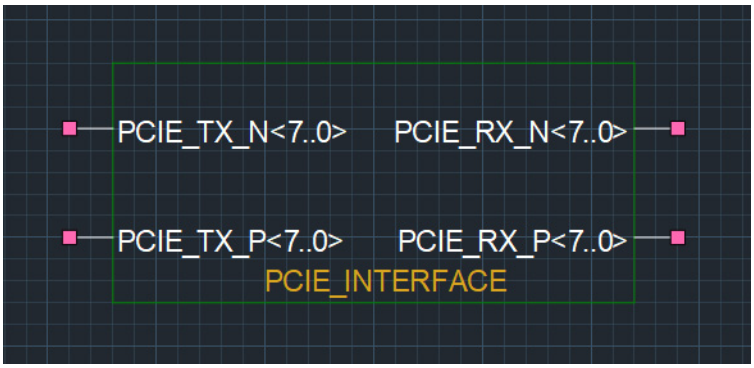
13. For RefDes, select the *Prefix* option and specify the prefix as `P`.



14. The block is added to the design.

The *PCIE_INTERFACE* schematic symbol placed on the schematic sheet.



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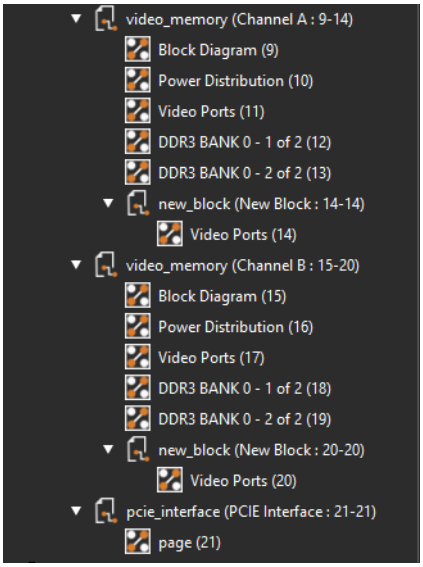
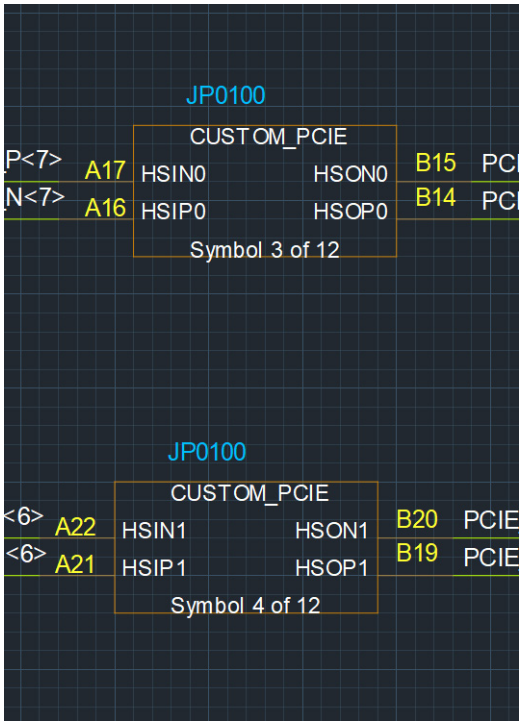
15. The *Project Explorer* is updated and shows the new block.



16. Descend into the instance of the PCIE Interface and view the modified RefDes of the instances present inside the block.

The prefix `P` added to the RefDes of each of the instances.



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Related Topics

Instantiating a Block

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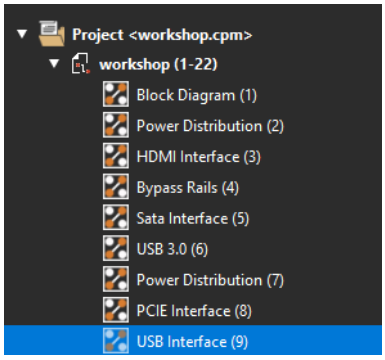
Re-importing Blocks

Blocks that are imported as read-only, can be updated to bring in the changes made in the source design since their addition into the current design. To update read-only blocks, use the re-import block option. In this section, first a block is added and then changes re-imported.

1. Add a new schematic sheet for the USB Interface, and name it *USB Interface*.



2. Add the block symbol for the *usb3* block on this newly added schematic sheet.

   The Packaging Options dialog is displayed.

3. Specify the instance name as *USB 3 Interface*.
4. Select the *Use Range* option.

   A minimum range of `16` is suggested as the total number of components in the block are 16.

5. Specify the range as *`501`* to *`600`*.

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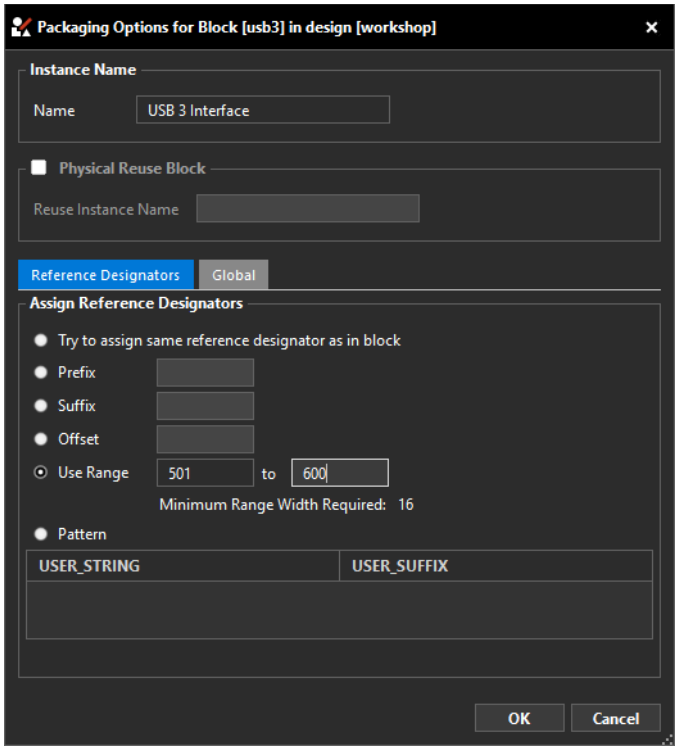
This means that the components of this block will have RefDes from `501` to `600`.



6. Click *OK*.

   The block is added to the design.

7. Right-click and choose *Done* to complete the process of instantiating the block.

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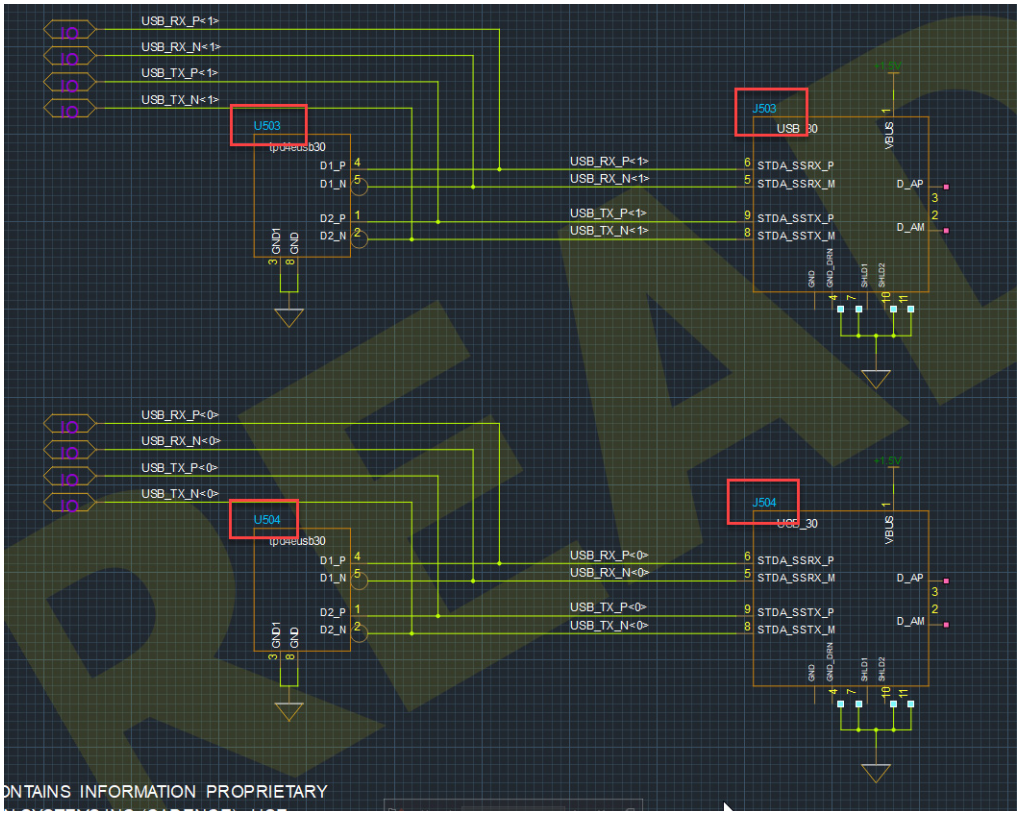
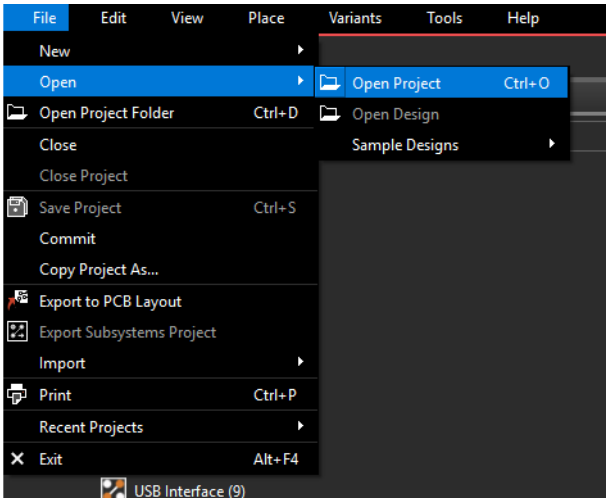
8. Descend into the block and view the RefDes assignment based on the Range specified.



Open the source block that was imported and check. This can be done directly from System Capture using the *File – Open – Open Project.*



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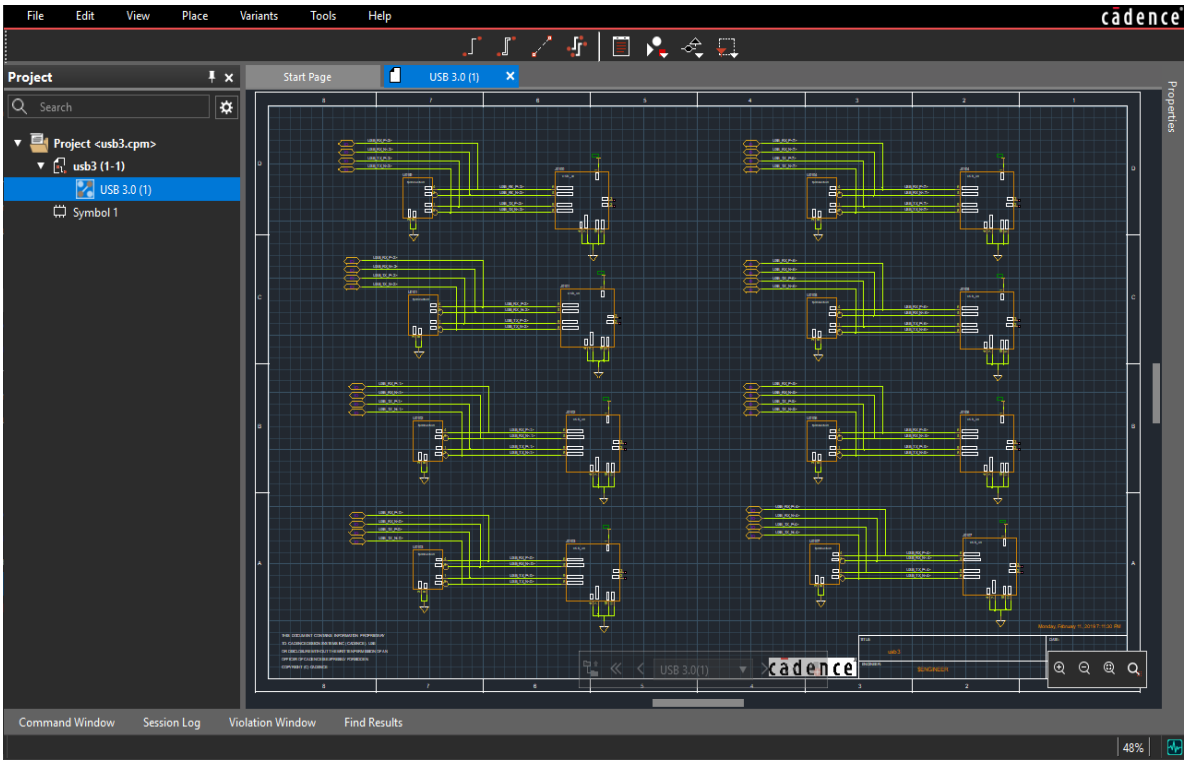
Browse to the project.A new System Capture window opens with the selected project. It is the same block, which was imported in an earlier step.



9. Close this session.
10. Choose *File – Open – Open Project* to open another project.

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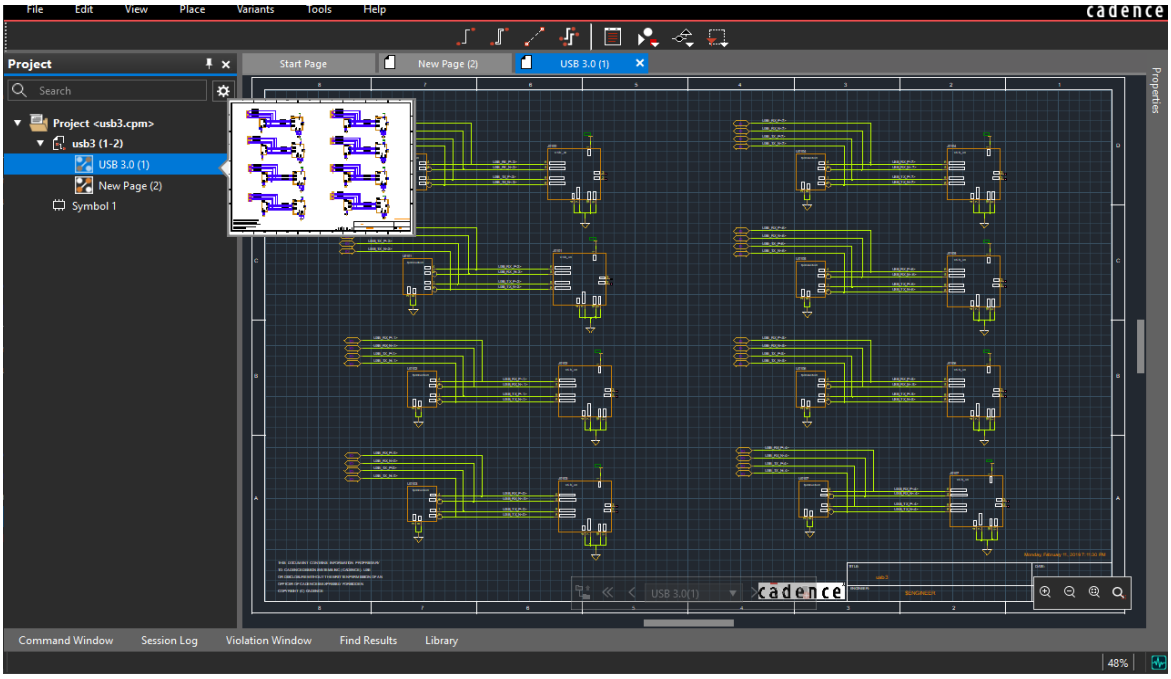
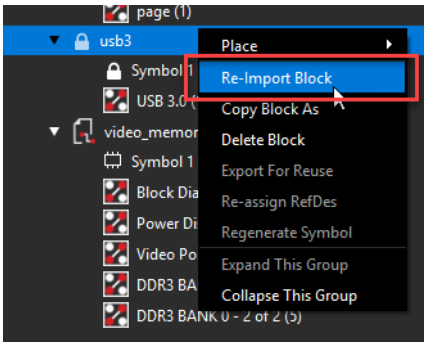
This is a modified version of the same block. This design contains two pages.



11. Close the session.

12. Go back in the first session of System Capture where the workshop design is open.

13. In the *Project Explorer*, select a block, right-click and choose *Re-Import Block*.



14. The *Re-Import Block* dialog opens with the path from where the block was originally imported.

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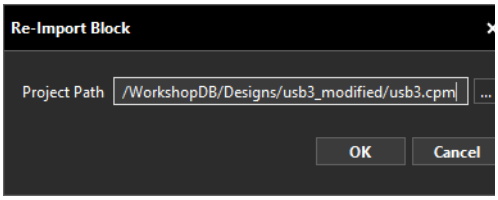
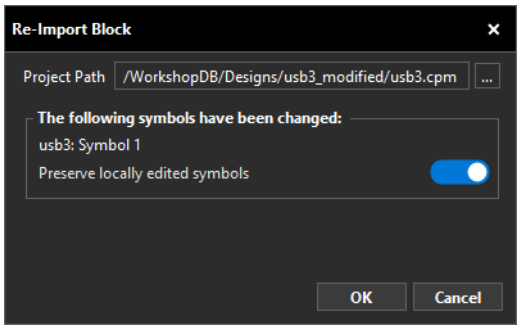
15. Click the browse button and select another project.

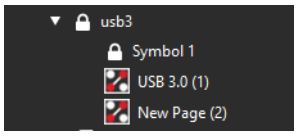


In case changes are made to the block's symbol, you are informed that the changes can get overwritten. You can retain the changed symbol or overwrite it.

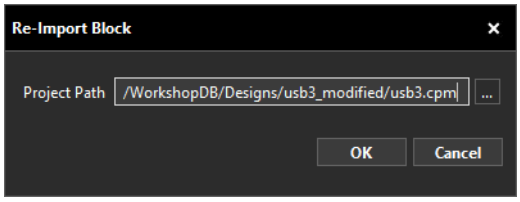


16. Click *OK* to re-import the block.

The block is re-imported and the *Project Explorer* is updated to display the newly added sheets of the block.



As the interfaces from the updated block have changed (change in the width of the ports), you can see that the instantiated block symbol is also updated to display the updated interface.



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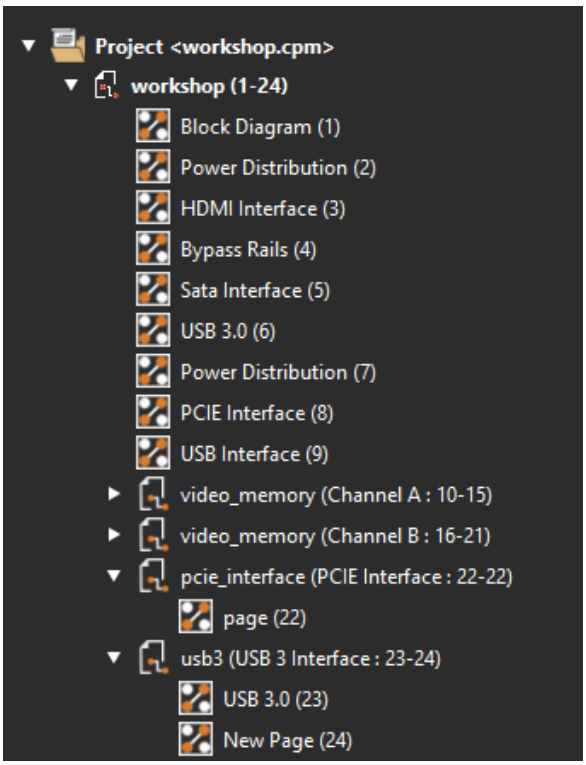
The Hierarchy viewer is also updated to display the newly added sheets in the re-imported block.



Related Topics

- Editing a Block
- Importing a Block

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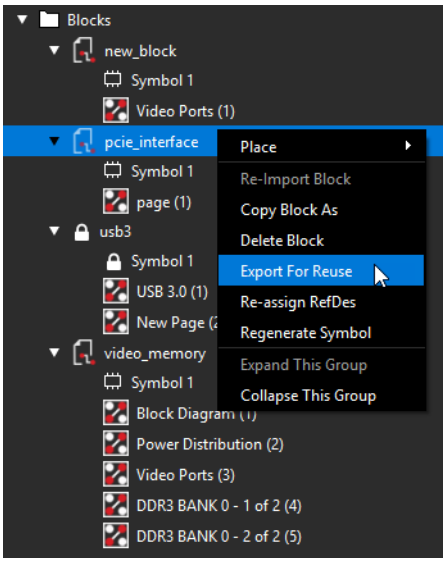
Reusing a Design

System Capture supports reusing of designs. Hierarchical blocks can be reused both logically as well as physically. Generating the packaging files for a block prepares the block for *logical reuse*. System Capture provides an easy way to generate packaging files without the need to make the block as root design. In Project right-click the block and choose *Export for Reuse*.



This displays the *Export to PCB Layout* form where you generate the packaging files for the block and, if required, netlist it to a board file. Netlisting the block to a board file enables the creation of the module (.mdd) file for the block, which is used in the *physical reuse* of the block. There are no other settings required for physical reuse.

When these packaging files are available and the block is instantiated, you can choose to reuse the block for logical reuse or physical reuse. The default option is logical reuse. When a block instance is selected for physical reuse, a unique Reuse Instance Name is assigned to it. The tool suggests a unique name that you can retain, or modify to another value.

In this section, we will reuse multiple instances of the *PCIE_INTERFACE* block. Each of the block instances will be enabled for *Physical Reuse*. We will also netlist this block to PCB Editor and view each of the block instances identified as modules.

To reuse a block:

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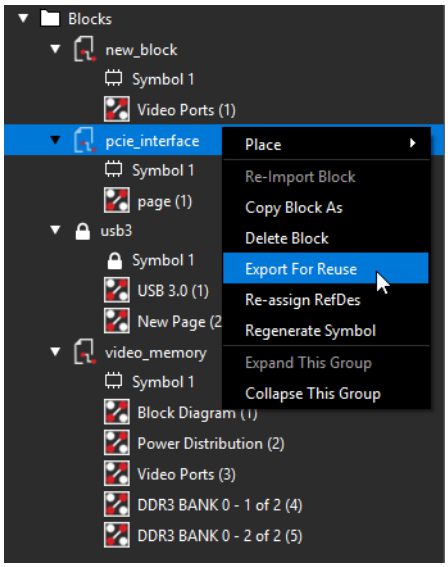
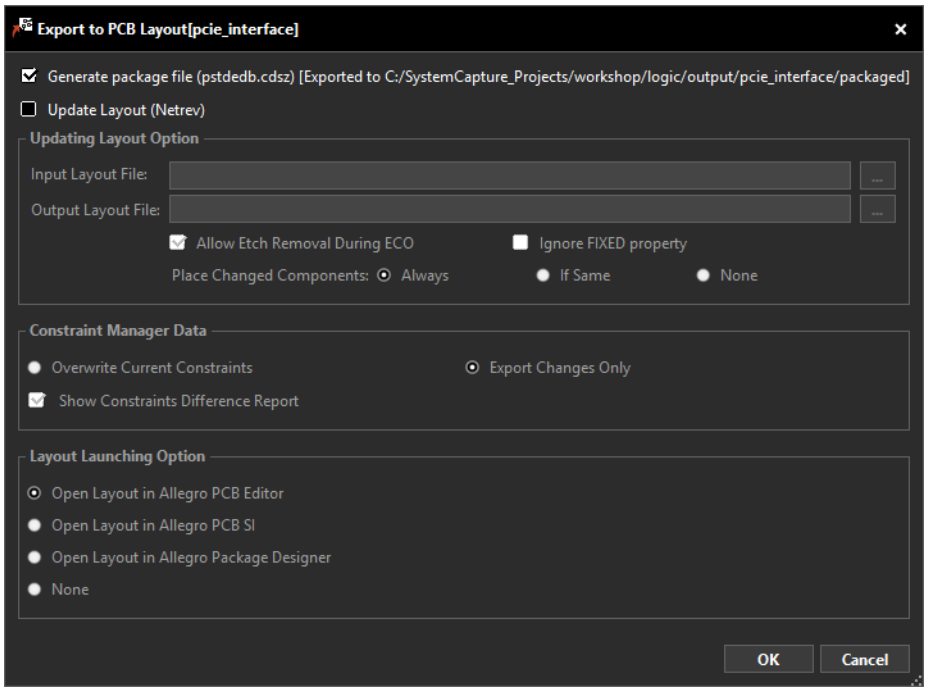
1. Open the *PCIE Interface* page, and delete the *pcie_interface* block instantiated on it.
2. In the *Project Explorer*, right-click the *pcie_interface* block and select *Export for Reuse*.



The *Export Physical* dialog box for the block *pcie_interface* is displayed.



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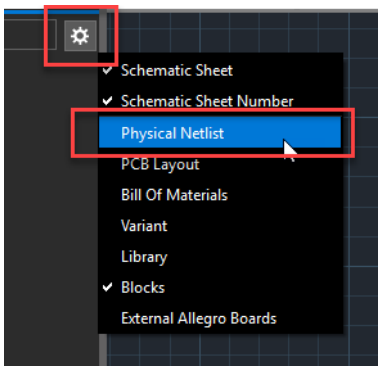
Use this dialog to generate the packaging files for the selected block. You can also select and generate a board file for the block from this form.

You can select a .mdd file directly as the *Input board file*. When you do that you can update the logic and layout, and save the updated module directly.

After the packaging files are generated, from the hamburger icon in *Project Explorer*, select Physical Netlist to view the files.



You can click a file to open the file and view its contents.

The block is now ready for reuse. We will now add a few instances of the block and enable them for physical reuse.

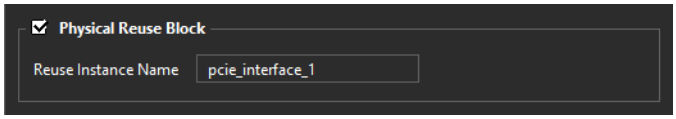
3. Add an instance of the *pcie_interface* block on the page *PCIE Interface*.

   As soon as the block is placed on the schematic sheet, the Block Packaging Options dialog is displayed.

4. Specify the *Instance Name* as *PCIE Interface*.

5. Select the *Physical Reuse Block* check box to enable this block for physical reuse.

   This enables the *Reuse Instance Name* edit box. This field is automatically populated with a unique value for this design. If required, you can change the value.



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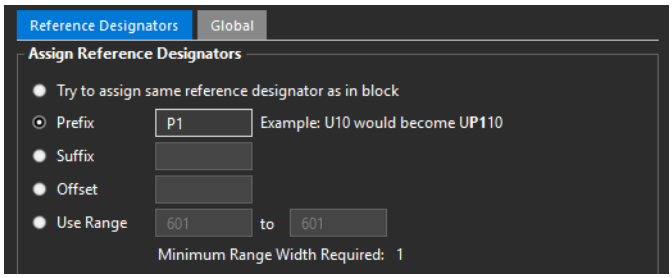
6. Select the *Prefix* option and specify the prefix as *P1*.

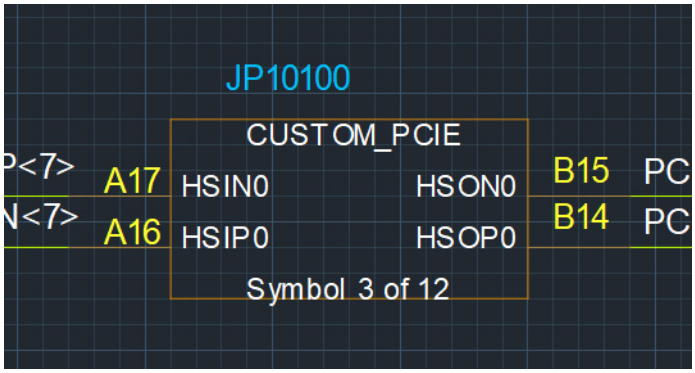


All the settings are complete.

7. Click *OK* and complete the block instance add function.

   The block is placed on the canvas and the next block instance is attached to the cursor. Get out of the block add mode.

8. Descend into the block to check that the RefDes assigned now has a prefix of P attached.



Now the netlist to will be exported to PCB Editor to check how the reuse block is transferred to PCB Editor.

9. Save the project.

10. Choose *File – Export to Layout* to export netlist of the design.

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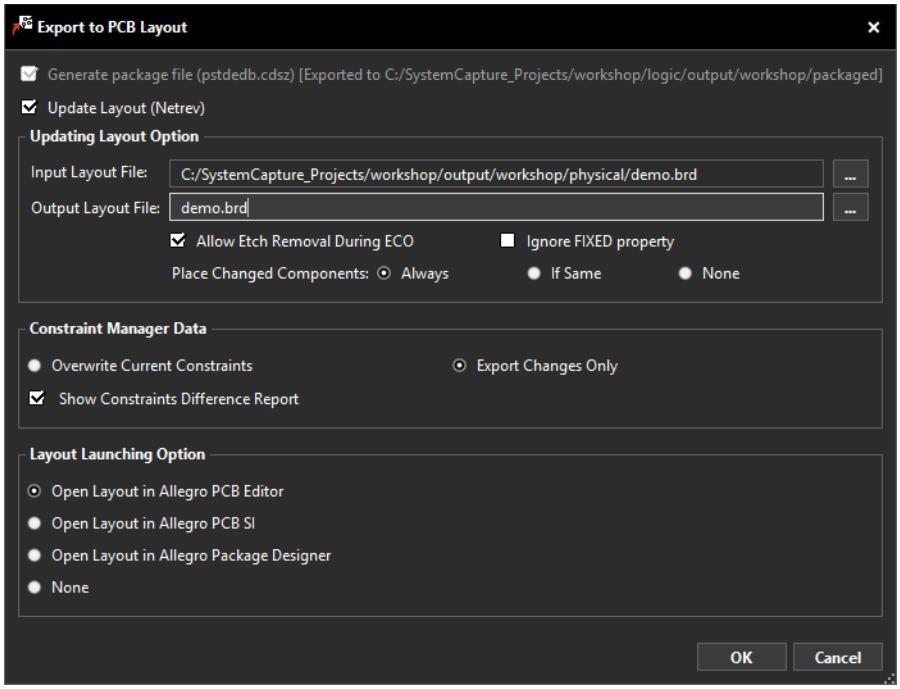
The *Export to Layout* dialog opens.



11. Ensure that the *Generate package file* check box is selected.

Note that the *Input Layout File* is set to the last board file that was generated. You can select a .brd or a .mdd file.

12. Specify the *Output Layout File* as `demo.brd` as we need to update the same file with the new netlist.

13. Ensure that the *Open Layout in Allegro PCB Editor* option is selected.

The netlist is exported and the board file is updated with the new changes. PCB Editor is launched with the updated board file. The already placed components are still placed on the layout canvas.

14. In PCB Editor, choose *Place – Manually* to open the Placement dialog.

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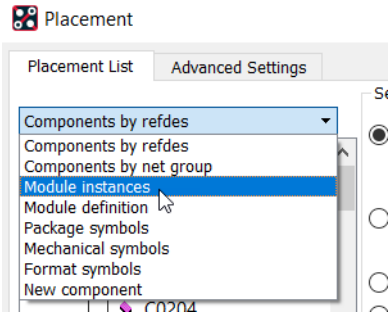
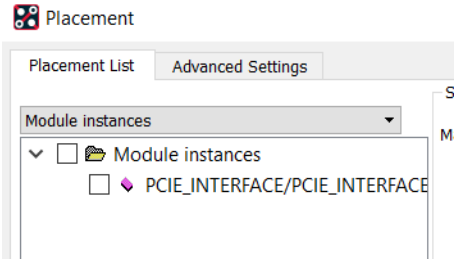
15. From the drop-down list, change the selection to *Module instances*.



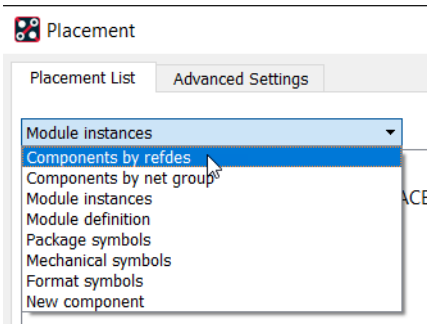
This changes the view and displays only the module instances found in the design. The design just contains one block, which has been marked for physical reuse. Therefore, only a single entry is available here. By hovering the mouse pointer over the name of the module instance, you can view the name of the reuse block as well as the Reuse Instance Name provided to the block for easy identification of the reuse instance.



If a module (`.mdd`) file for the reuse block is available, and you select the reuse instance, you can place it on the layout canvas.

16. Change the selection back to *Components by refdes*.

This again shows all the RefDes which are yet to be placed on the layout canvas.



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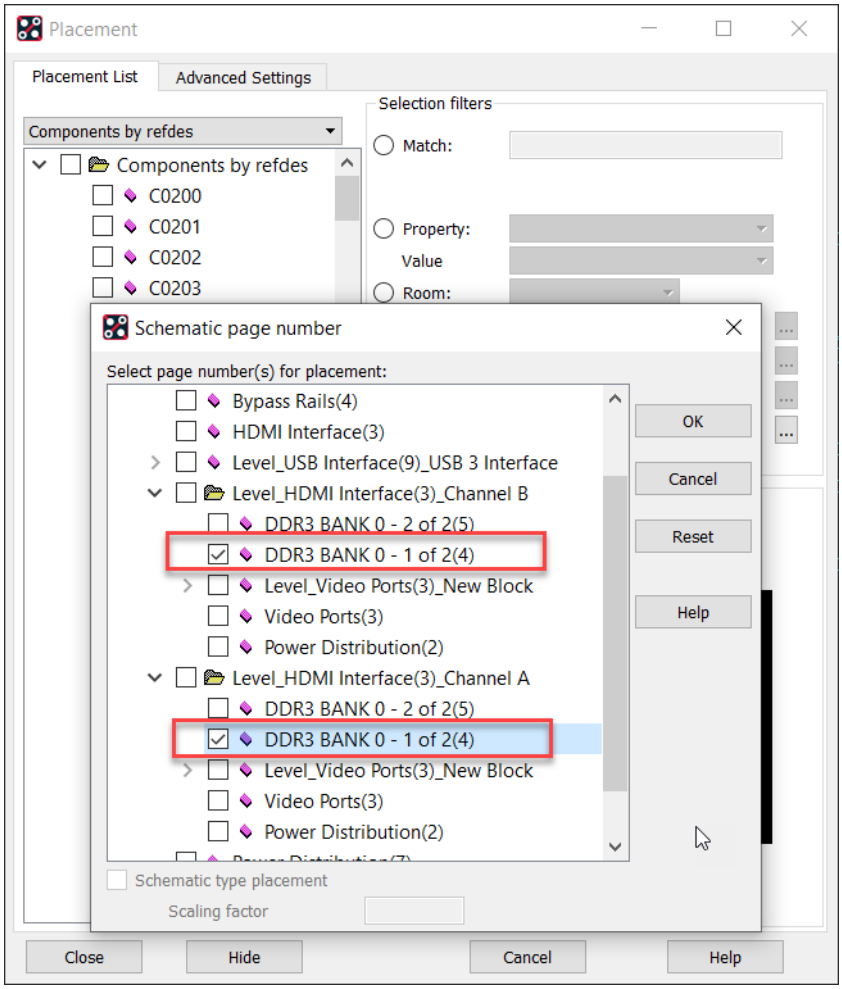
In the *Placement* dialog, `Selection filters` can be used to filter data from the RefDes list.

17. Select the option for *Schematic page number*.

This enables the ellipsis (browse) button next to it.

18. Click the ellipsis.

A dialog lists all the schematic pages where components are still unplaced.



19. Select one or more pages from the list to filter the components present on the selected pages only.

20. Select the page *DDR3 BANK 0 – 1 of 2* from Channel A & channel B.

21. Click the *OK* button.

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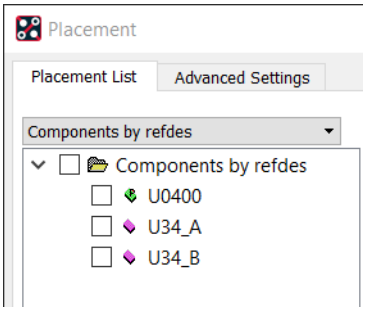
This updates the RefDes list and show instances from the selected pages only.



22. In the *Selection filters*, reset the filter by selecting the *Match* option.

23. Back in System Capture, open the schematic page for *USB 3 Interface*.

24. On this page, select the instance of the *USB3* block.

25. Go back to PCB Editor and scroll down in the Placement dialog.

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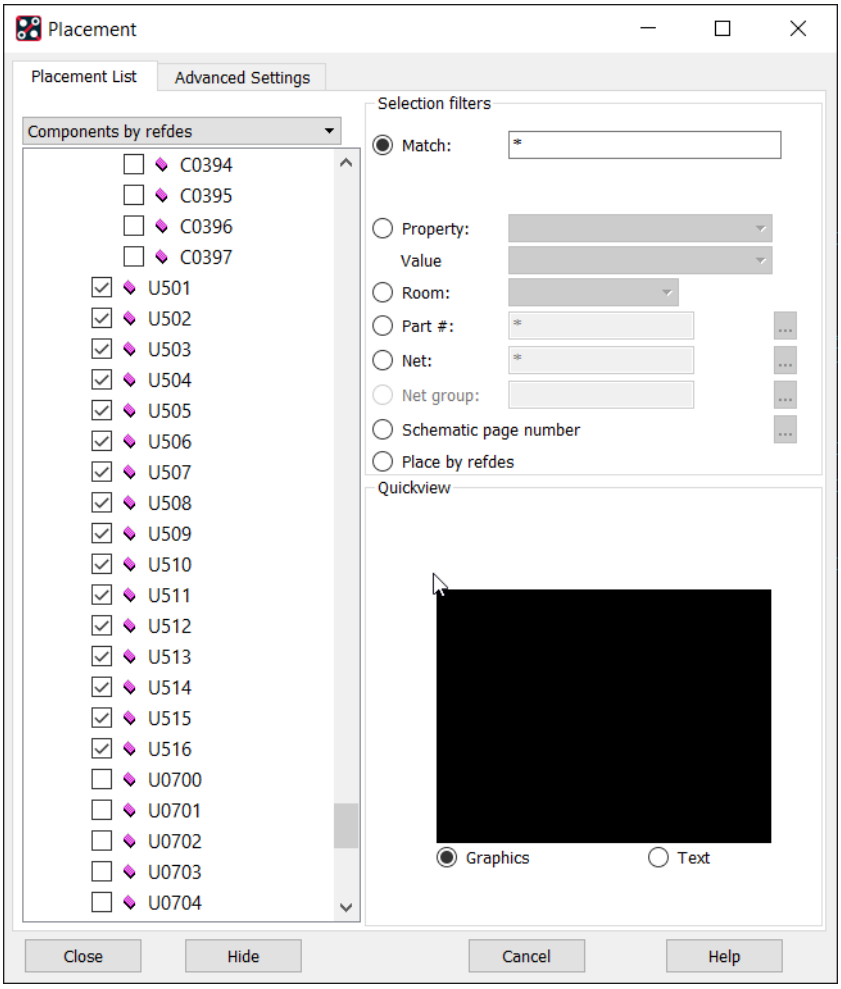
All the instances of the USB3 block (instances with RefDes starting from 500) have been selected for placement.



Selecting a block instance symbol in schematic, selects all the instances of the block for placement.

Save the PCB Editor database and close all the windows and exit PCB Editor.

Related Topics

- Re-importing Blocks
- Editing a Block

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Working with Hierarchical-Split Symbols

Hierarchical block symbols that have a high pin count can become difficult to manage as these symbols cannot be placed within the standard page border. Large symbols can also take up most of the space on page and the connections between blocks cannot be displayed on same page. To overcome this problem, large hierarchical block symbols are split into multiple split symbols.

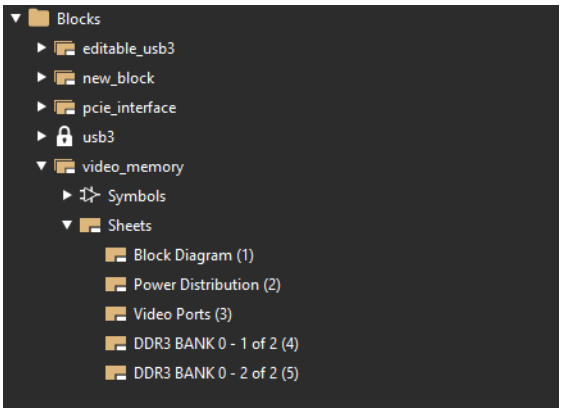
Instead of generating one difficult-to-manage large symbol, the ports of the hierarchical block are distributed across multiple symbols. This support for hierarchical-split symbols (HSS) reduces the size of the block symbol. Additionally, the ports can be logically categorized and placed on different symbols to create symbols that can be placed across schematic sheets, especially near the circuitry to which they are connected.

Creating a Hierarchical-Split Symbol

To split a symbol, follow these steps:

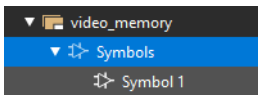
1. Navigate to the *Blocks* node in the *Project Explorer.*
2. Expand any of the blocks.

   You will notice an entry called *Symbols.*



3. Click *Symbols.*

   By default, there is one symbol always present under the *Symbols* entry.



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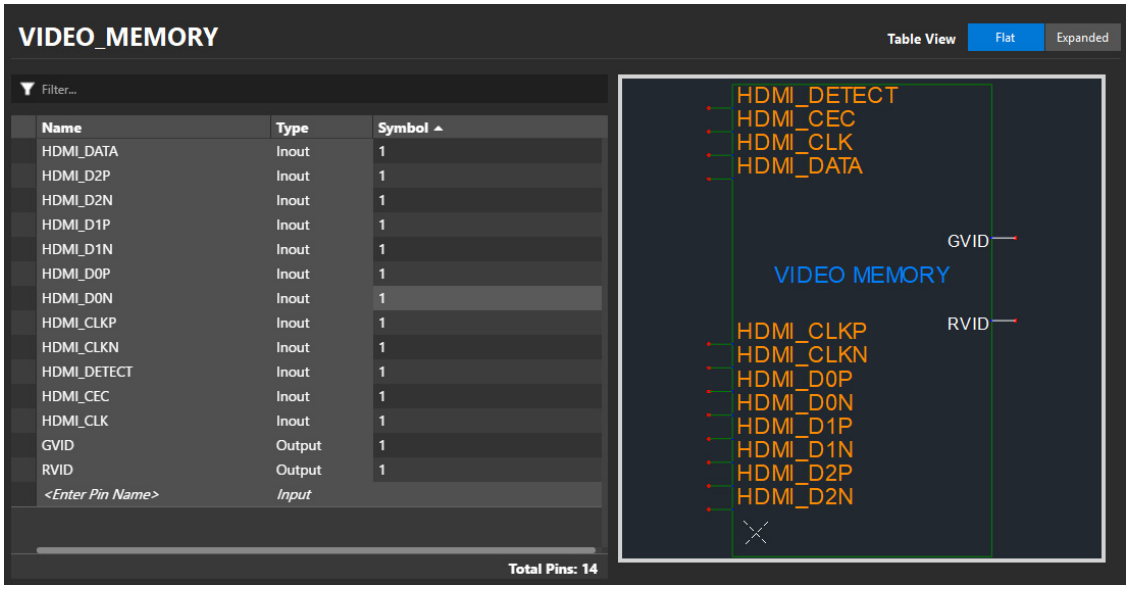
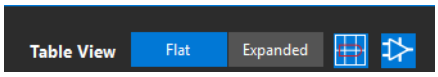
4. Click the *Symbol1* entry.



All the pins in the block are listed in a table along with their type. You can see the symbol where these pins are assigned.

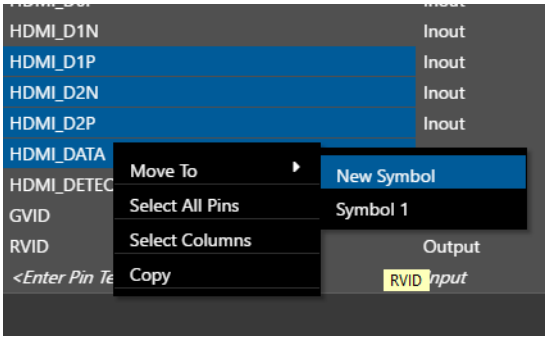
You can also see the placement of the pins in a diagram.

To toggle the display of the table and diagram, click the following icons.



5. Sort the pins as needed.

6. Select the pins that you want to move to another symbol.



7. Right-click the pins and choose *Move To – New Symbol*.

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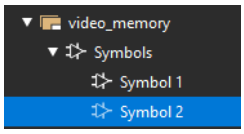
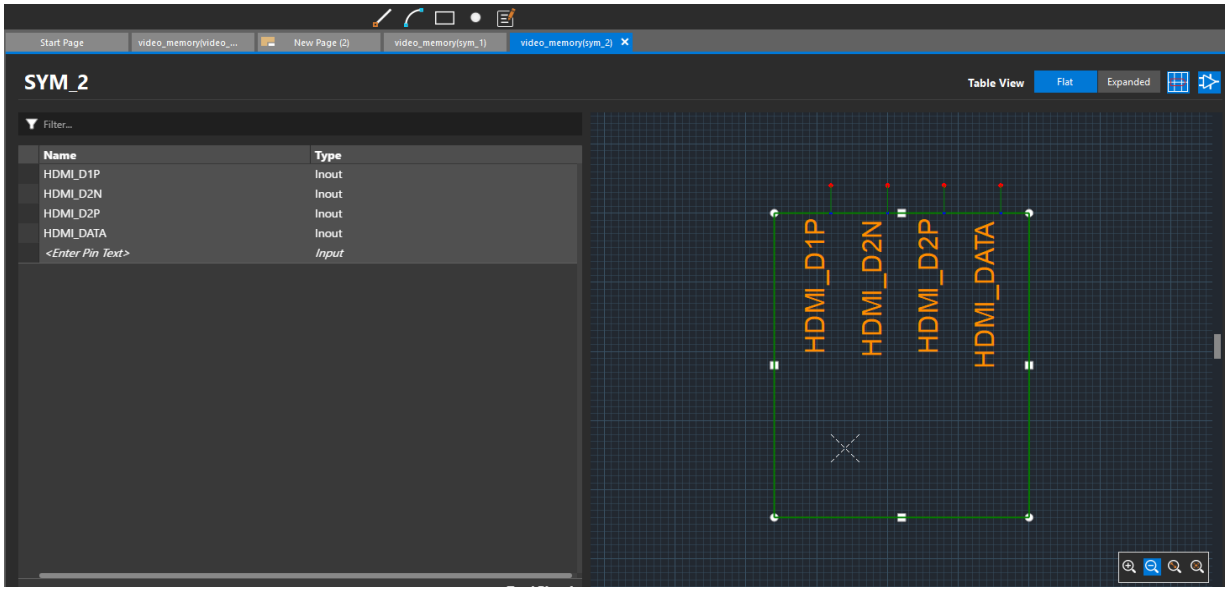
A new entry for *Symbol2* gets immediately added under *Symbols*. This is the default name and cannot be edited.



8. Click *Symbol2.*

   The pins that were moved to this new symbol are displayed, both in the table and as an image.



9. Edit the pins and names if required.

10. Similarly, create more symbols.

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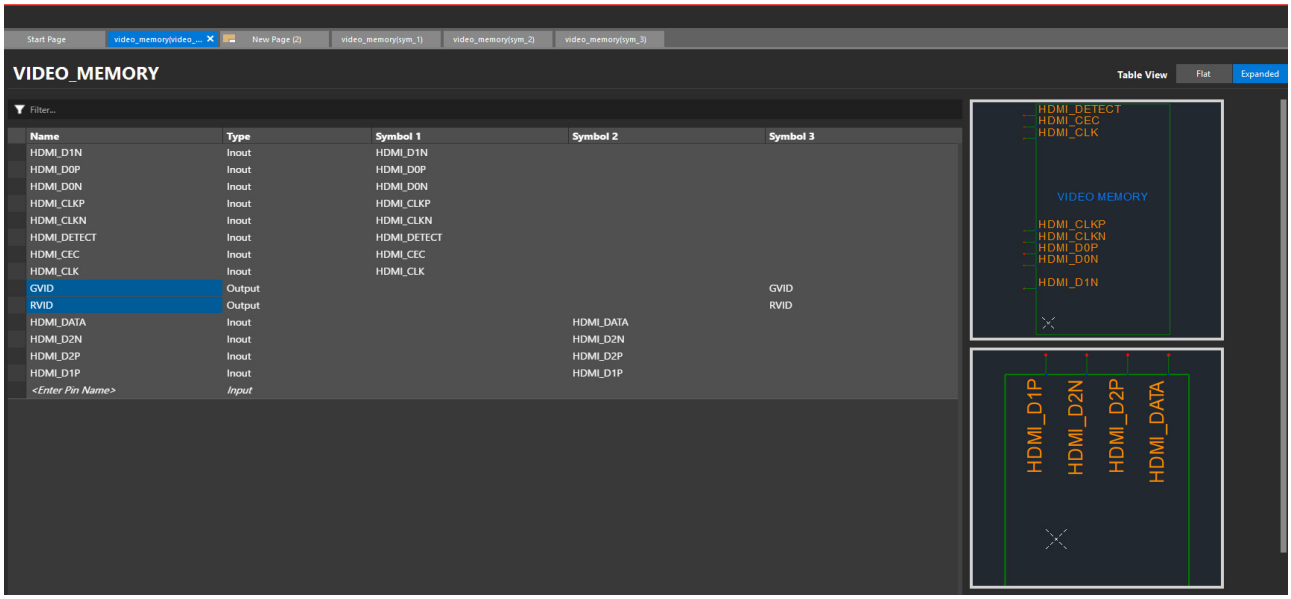
11. Click *Symbols.*



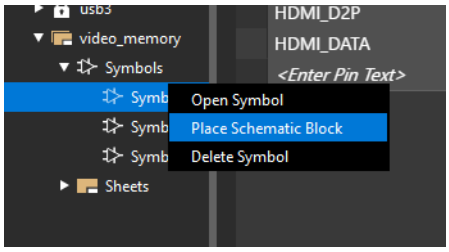
All the pins are displayed along with the symbols that they are in. You can also see the graphics for each symbol.

This completes the splitting of a symbol into multiple symbols. You can also change the symbols the pins are moved to later. All that you need to do is select the pins and choose the symbol in the *Move To* command.

Placing the Symbol

To place the symbol, follow these steps:

1. Right-click the symbol to be placed and choose *Place Schematic Block*.



2. Navigate to a place where the split symbol is to be placed.

An icon for the symbol is attached to the cursor.

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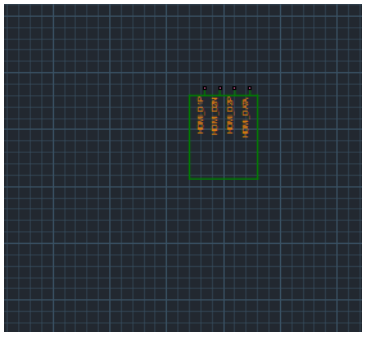
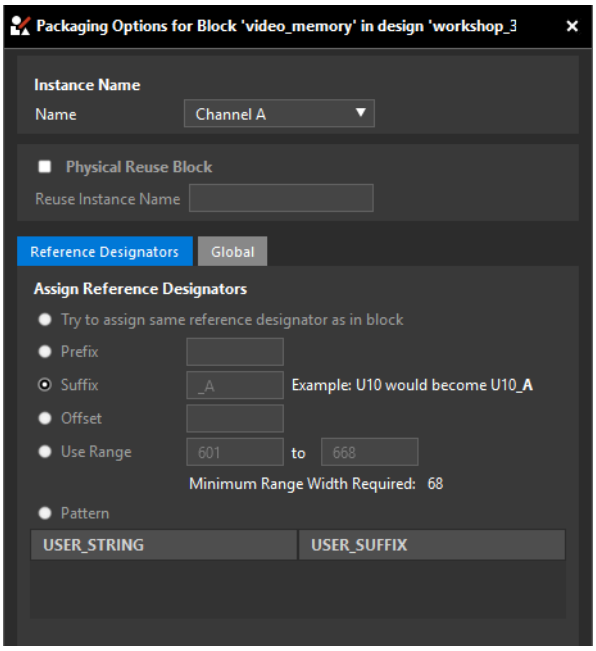
3. Click anywhere on the canvas.



The symbol is placed and the *Packaging Options* dialog box is opened.



4. Specify a name for the instance.

You can choose a preexisting name from the drop-down list or enter a new name.

5. Click *OK*.

You will notice a message in the Violation window that the other split symbols have not yet been placed.

Important

Place all symbols of the HSS part to ensure no errors are displayed when changing NetGroup members.

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Merging Split Symbols

To merge symbols, you need to remove all the symbols that have been created from the default *Symbol1*.

1. Ensure the split symbol is not instantiated.
2. Right-click the *Symbol<n>* entry and choose *Delete Symbol*.
3. Confirm that you want to delete, if prompted.

When you delete the symbol<n> the pins that were moved to this symbol are moved back to *Symbol1*.

Managing Connectivity Changes

- In case there are symbol vs schematic mismatches, System Capture reports that when a page is opened.
- If the net width is increased, the extra bits need to be assigned again to any symbol of the split symbol.

Related Topics

- Viewing the Design Hierarchy

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8

Managing Variants in System Capture

This module covers how System Capture supports creation and management of Variants of a design. The following topics are covered in this module:

- Creating Design Variants
- Changing Variant Name and Custom Variable Values
- Deleting Variants
- Variant Editor

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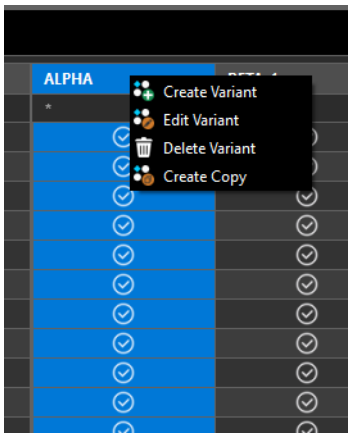
Creating Design Variants

System Capture supports creation and management of design variants on schematic sheets. You can create multiple variants of a base design and modify the components in the base schematic for use in the variants.

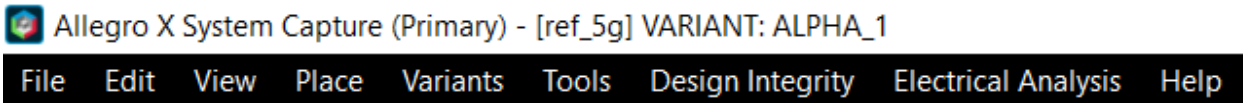
1. Choose the *Variants – Create Variant* command to create a new variant for the design.
2. Specify the name of the variant.

   If there are no custom variables defined for the design, the lower part of the form does not display anything. This is where you can specify the variant-specific Custom Variable values.



3. Click *OK*.

   The variant is created. System Capture switches to the *Variant* view where the variant data is edited. The title bar indicates that the variant view is being displayed.



No design editing features are available so that the schematic remains the same in the variant. Icons for editing the schematic are hidden in the variant view. The *Properties*

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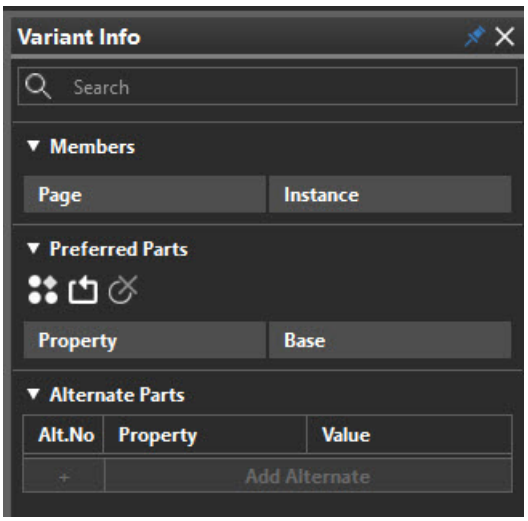
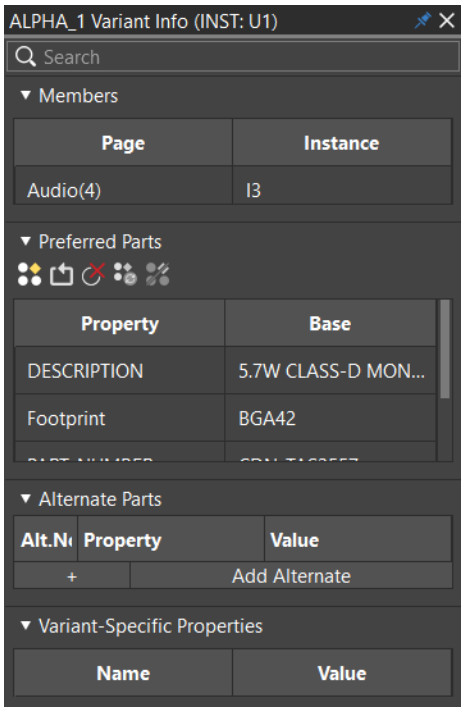
window is replaced by the *Variant Info window,* that displays the variant information for the selected object.



4. Select one of the components on the canvas.

   The details of the selected object are displayed in Variant Info. All the key properties of the part are visible under the Base column.



5. Specify if the part should not be installed.

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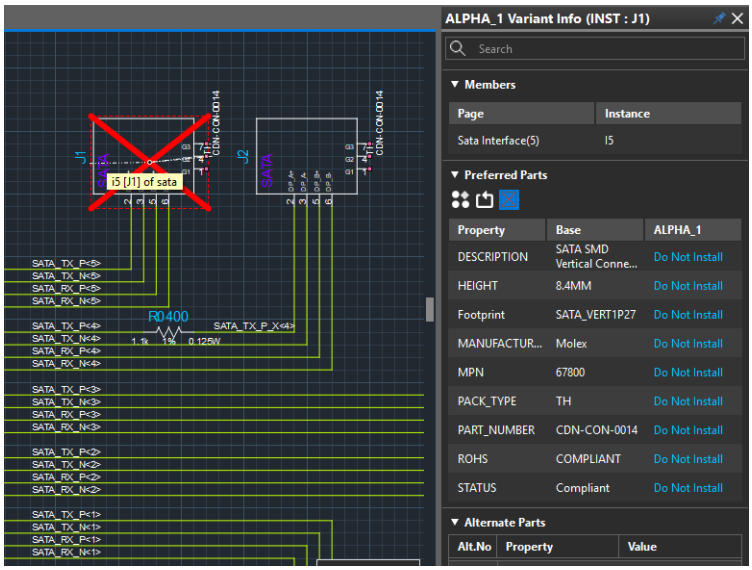
a. Click the *DNI* button in the *Preferred Parts* section of the *Variant Info* form.

On marking the component instance as DNI, a cross mark appears across the component instance on the canvas.

The Variant Info window changes to display a new column for the properties specific to the variant, `ALPHA`, and shows the status of the component as `Do Not Install` for this variant.



b. Customize the color and line width of the cross placed on DNI components:

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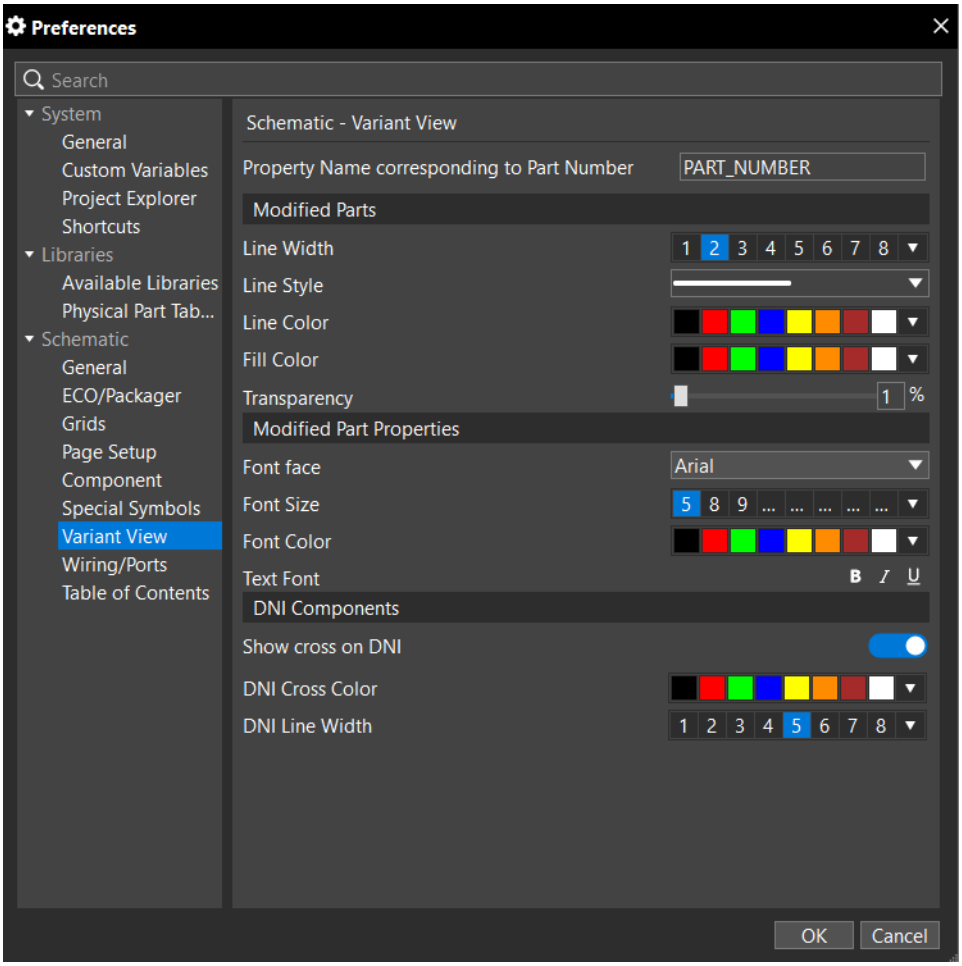
c. Choose *Edit – Preferences – Schematic – Variant View*.



d. Change as required.

e. Click *OK*.

6. Replace a part with another part by following these steps:

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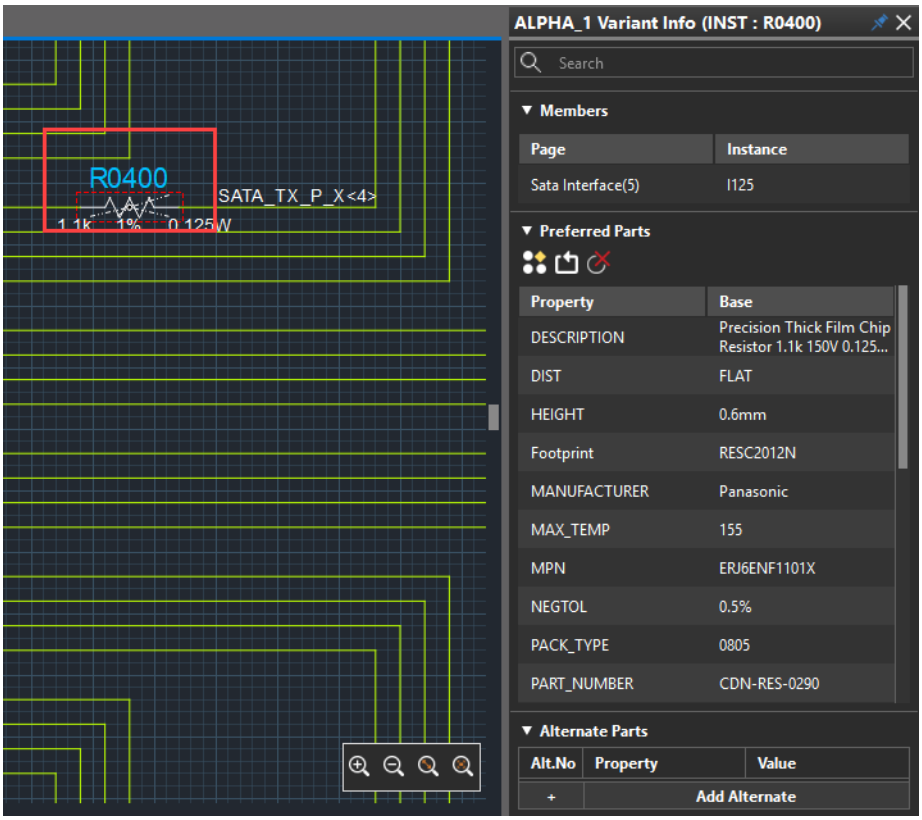
a. Select a component on the schematic.

The *Variant Info* form is populated with the properties of the selected part.



b. To replace this, click *Add Preferred Part*.

You can change a part with a preferred part only if the new part has the same or a compatible footprint. A compatible footprint can be defined in the `cjedectype.txt` file which is placed in the SITE area. All the compatible footprints are listed in the file in different sections which are separated using a semi-colon (;).

c. Log in to external sources or click *Skip* to use parts from the libraries.

The *Select Preferred Part* dialog is displayed.

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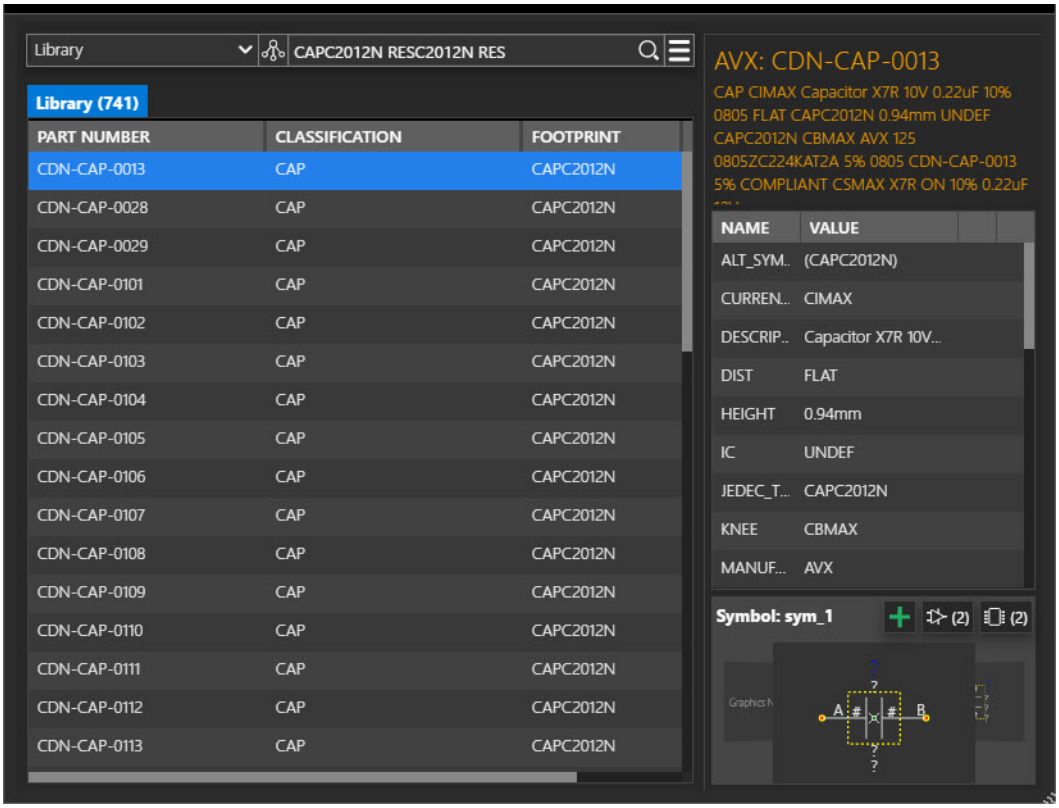
The search criteria for compatible footprints is already applied and relevant results are displayed. This ensures that the selected preferred part has a compatible footprint.



7. Specify the replacement.
8. Double-click to select the component as a preferred part.

   The component on the canvas is replaced with the selected part:

   - The formatting of the component changes to show that it has been changed in the variant.
   - The properties of the newly selected part are now displayed in the *Variant Info* form.

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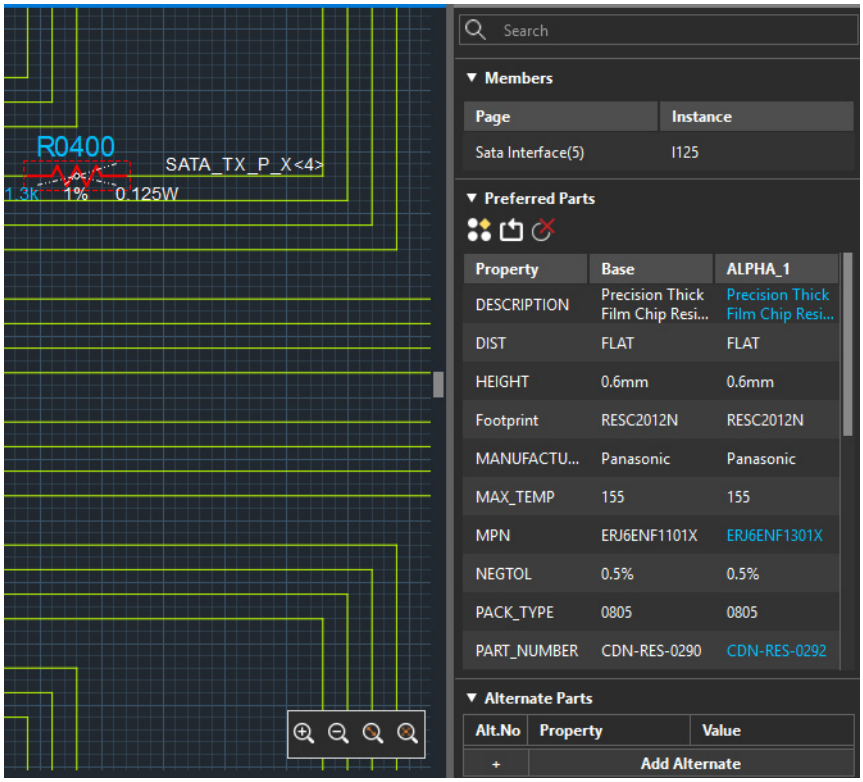
- The properties that have changed display in a different color, both in the *Variant Info* form as well as the schematic.



9. Choose *Variants – View – Off* to switch back to the base schematic view.

Related Topics

Deleting Variants

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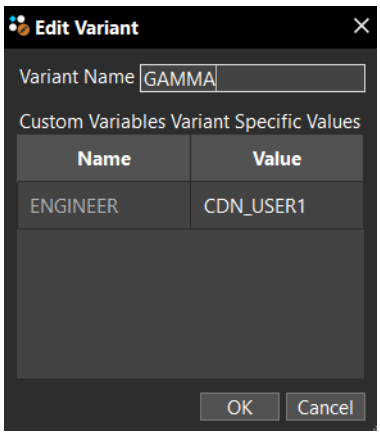
Changing Variant Name and Custom Variable Values

To modify the name of a variant:

1. Choose *Variants – Edit Variant – <Variant Name>*.

   The *Edit Variant* dialog opens.

2. Specify a new name.
3. Change custom variables if defined in the design.



4. Click *OK*.

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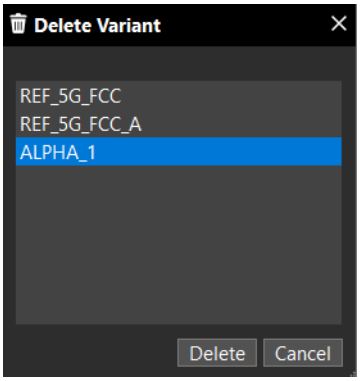
Deleting Variants

To delete variants:

1. Choose *Variants – Delete Variant*.

   The Delete Variant dialog opens and lists all the variants.

2. Select one or more variants from this dialog to delete the variants.



3. Click *Delete*.

   When a variant is deleted, all the changes done in the variant are lost.

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Programmable Parts for Variants

Important

Available only when connected to a Remote Pulse Server.

If you are working in an enterprise mode, that is multiple designers are connected to the same server where all designs and libraries are located, you can replace components in a variant to a part code or part number that is not present in the project libraries. This works as a placeholder for the component. This is in addition to being able to choose an alternate preferred part.

Setting Up the Programmable Parts Feature

Prerequisite

To enable the feature, set the following directives in the `START_VARIANT` section of the *`project`* or `site cpm` file:

Directive	Value	Description
`VAR_REPLACE_BY_PROP`	`ON`	Enables the feature
`VAR_REPLACE_PROP`	*`<Property name>`*	Specifies which property can be changed

Adding Programmable Parts to Variants

To replace a component with a placeholder part, follow these steps:

1. Ensure that the Remote Server address is provided in Pulse and you have successfully logged in.
2. Open the design that has variants or create variants for an open design.

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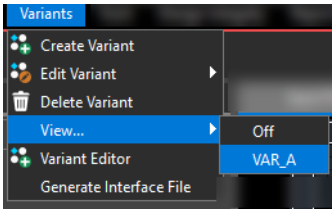
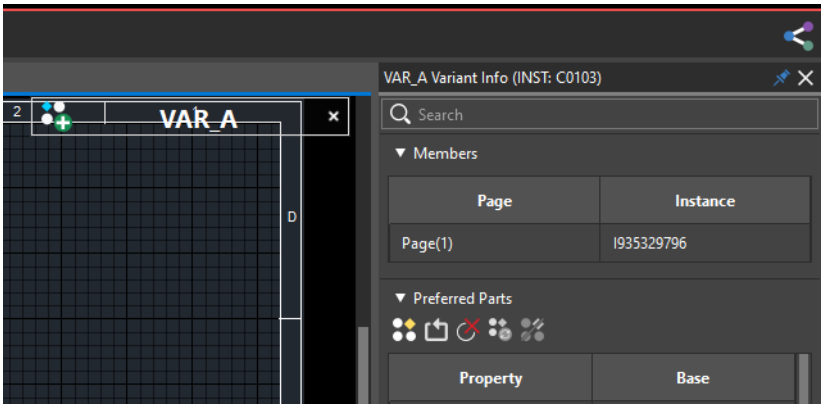
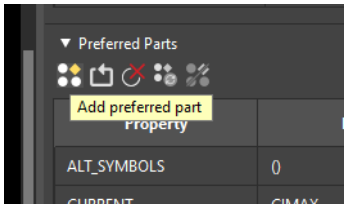
3. Choose *Variants – View –* `<variant name>` to open the variant where you want to replace a part with a placeholder.



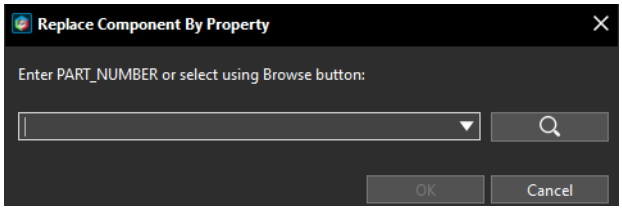
The variant opens and the name is displayed on the canvas and the *Properties* window changes.



4. Choose the component to be replaced.
5. Click *Add preferred part.*



The *Replace Component By Property* dialog box is displayed.



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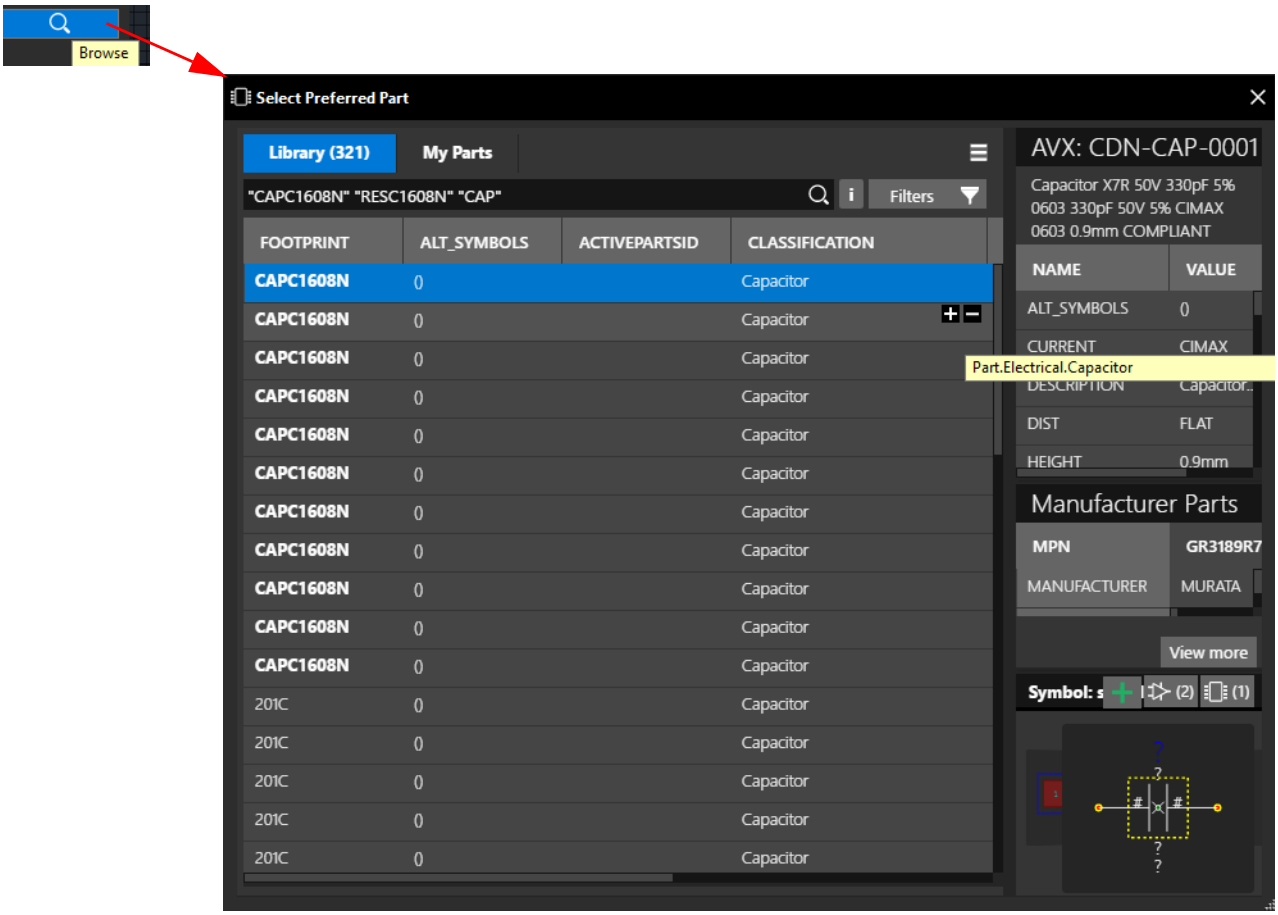
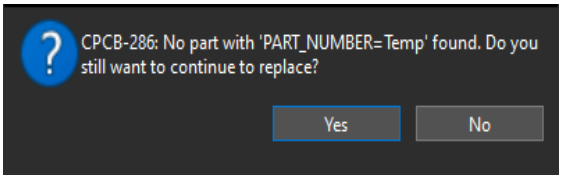
6. Enter a name for the replacement part or click Browse to open the Select Preferred Part dialog box.

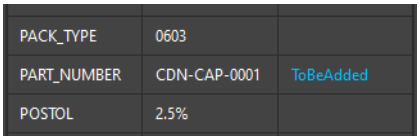


If you enter a part name that does not exist, you get the following message:



7. Click *Yes* to continue.

The part number for the component gets changed to the text you added.



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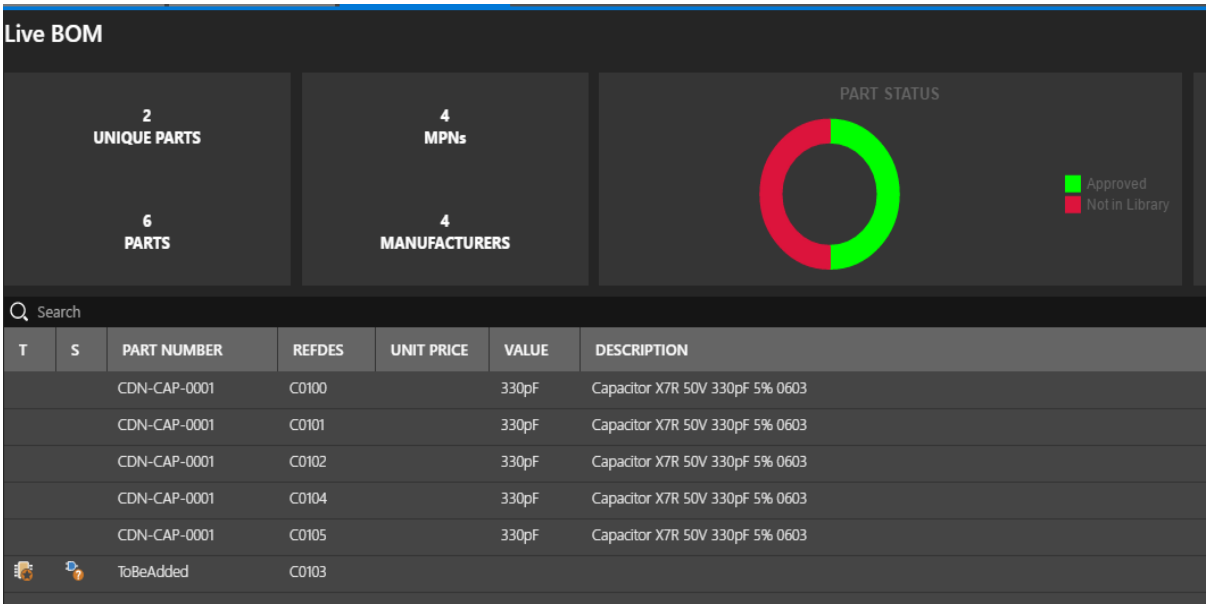
After you save design, the Live BOM component list for the variant gets updated.



You can use this feature even with the *Variant Editor*.

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Variant Editor

System Capture also provides spreadsheet-based variant editing capability. The Variant Spreadsheet Editor provides a single view for displaying information about all the function groups, alternates, and the variants of a design. Function groups are a set of components that form a feature or a logical function in multiple variants. Alternates are used to replace the preferred value of the component.

Using Variant Editor, you can:

- Create a new variant
- Create a copy of an existing variant
- Edit variant information, such as name and Custom Variables
- Delete a variant
- Create function groups
- Add components to the function groups
- Define alternate components
- Add function groups and alternates to different variants of a design
- View details of each variant
- Import DE HDL design with functions and alternate parts
- Configure user-defined properties in the Variant Editor

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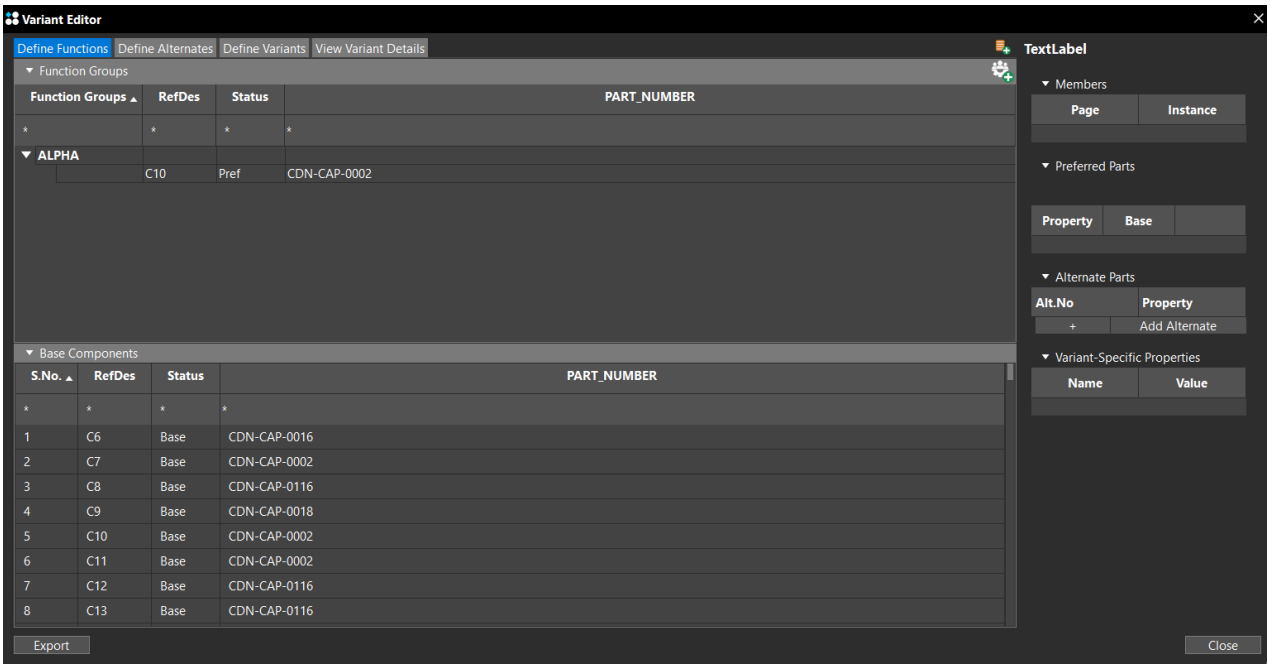
All basic operations of spreadsheet, such as column resizing, sorting, filtering, and so on are supported.



Each of the instances for a variant can be:

- Same as Base, shown with a check mark
- Do Not Install (DNI), shown with a cross
- New preferred value

  On selecting the cell, all the properties associated with the part are displayed in the Properties Window. The properties with changed values are displayed in blue to highlight the change.

You can select one or more of these cells and operate on them through the right-click menu or using buttons in Property Window.

- Select Preferred Part
- Reset to Base
- Mark as DNI (Do Not Install)

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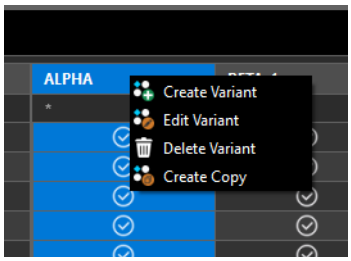
- Add Alternates



You can select and copy data from one or more cells and paste on other cells to replicate the variant information. Variant columns can be copied and pasted for replicating the complete variant. After making changes in Variant Editor, you can switch to the schematic view to view the changes applied.

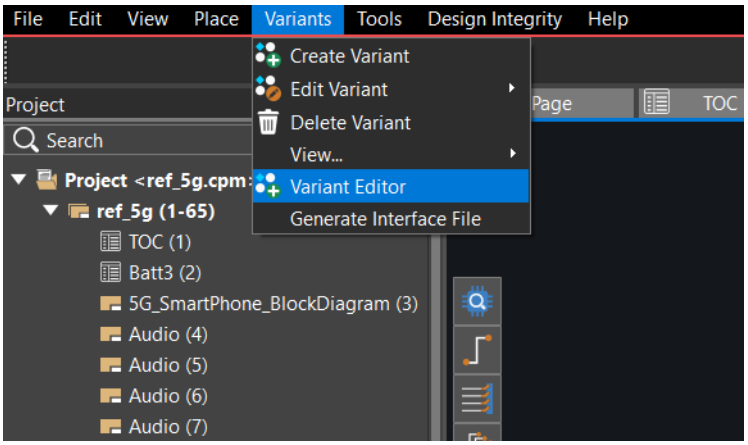
Defining Functions in Variant Editor

If you need to add a set of components that form a feature or a logical function in multiple variants, you can create a function. Later, you can exclude or include the function from the variant as a whole, which means, you either add all the components defined in the function to the variant, or add none of those components in the variant.

Create a function if you need a set of components in the base schematic to be included in any variant as a group. When you create a function, you can either include all the components in the function in the variant or include none of them in the variant. Functions can contain alternate groups and components that have been assigned alternate values

To create a function from the Variant Editor:

1. Choose *Variants – Variant Editor*.



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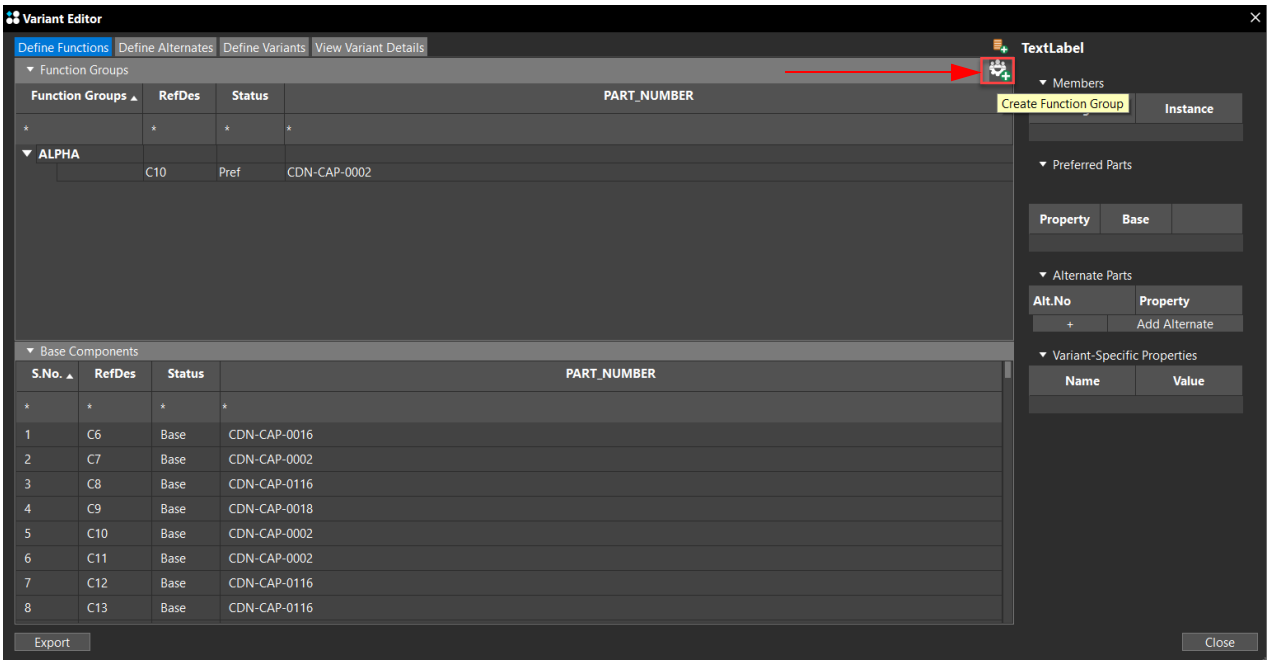
The *Variant Editor* dialog box opens. It contains four tabs to define functions, alternates, variants, and view variant details. *Define Functions* tab opens by default. In this tab, you can define function groups and add components to function groups.

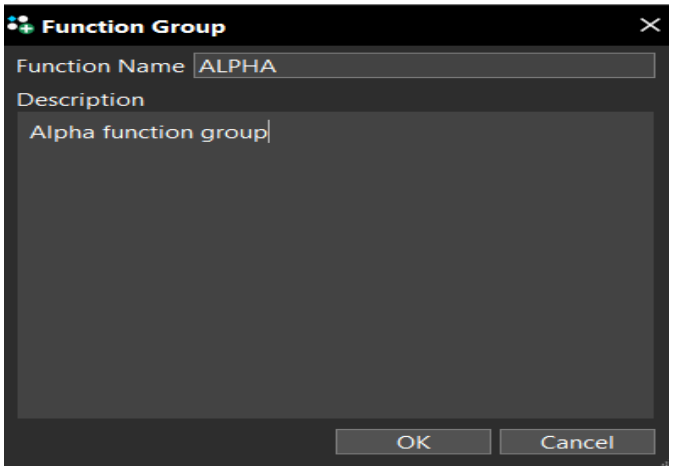
2. Click the + icon on top-right of the *Function Groups* section.



The *Create a Function Group* dialog box opens.

3. Enter a name and optionally, description for the function group, for example, `Alpha`.

4. Optionally, add a *Description* for the function group.



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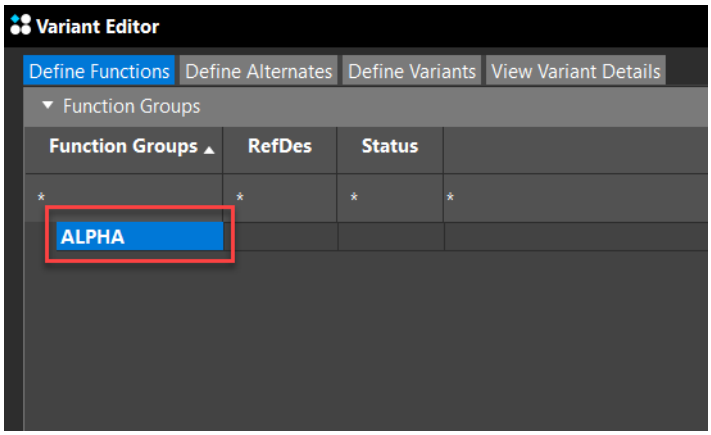
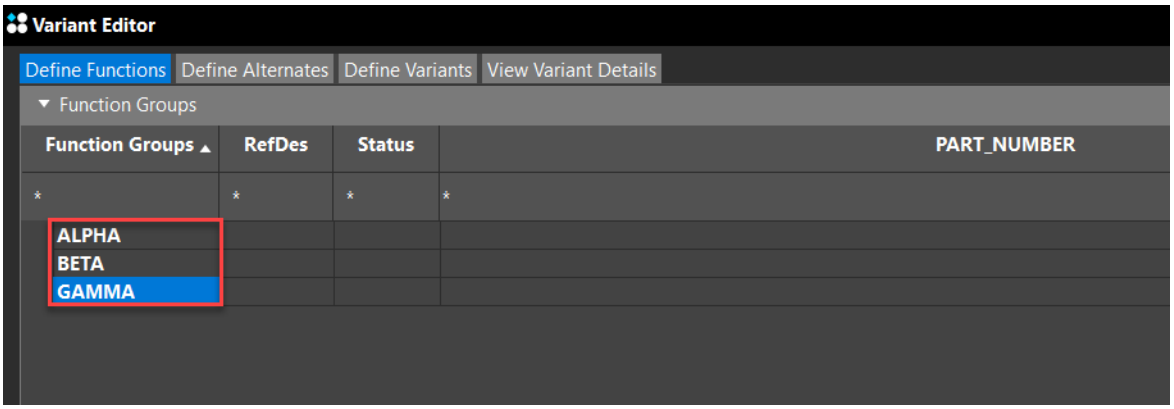
5. Click *OK*.

   The function group gets added to the *Function Group* section.



6. Repeat the steps to create a function group to create two more function groups named `Beta` and `Gamma`, respectively.



Each added function will be displayed in the *Define Variants* tab of the *Symbol Editor* with the respective components. By default, the function will not be added to any of the variants.

Add Components to the Function in Variant Editor

You can add components to the function groups in the *Define Functions* tab of the *Variant Editor*. To search components with particular values of properties, add those properties as columns. To do this, follow these steps:

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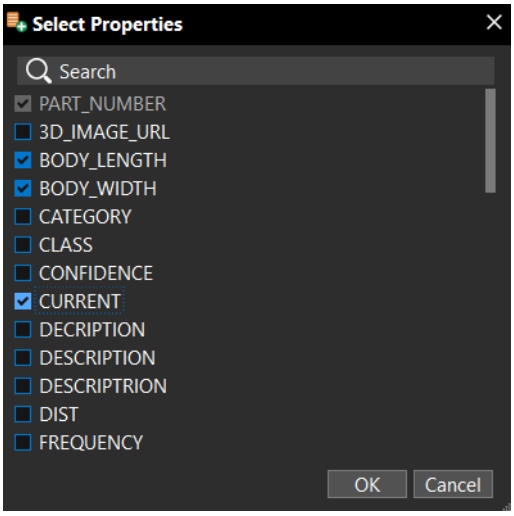
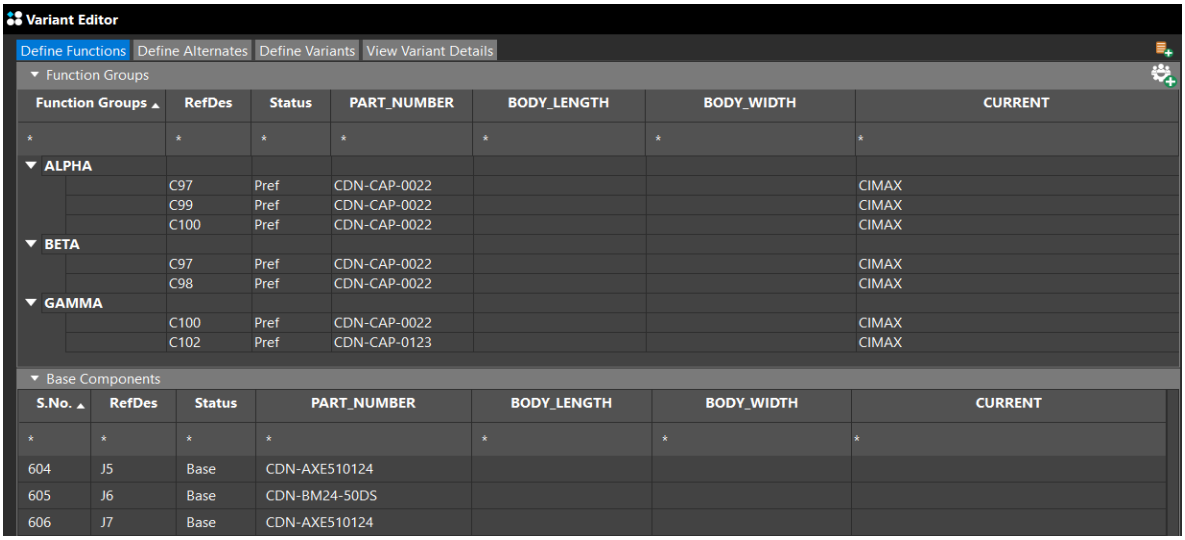
1. Click *Choose property columns to display* icon from the top-right.

2. Select properties to be displayed as columns.



3. Click *OK*.

   All tabs of the *Variant Editor* will be updated with these columns.



Note: In case *PART_NUMBER* property is named differently in your library, you can

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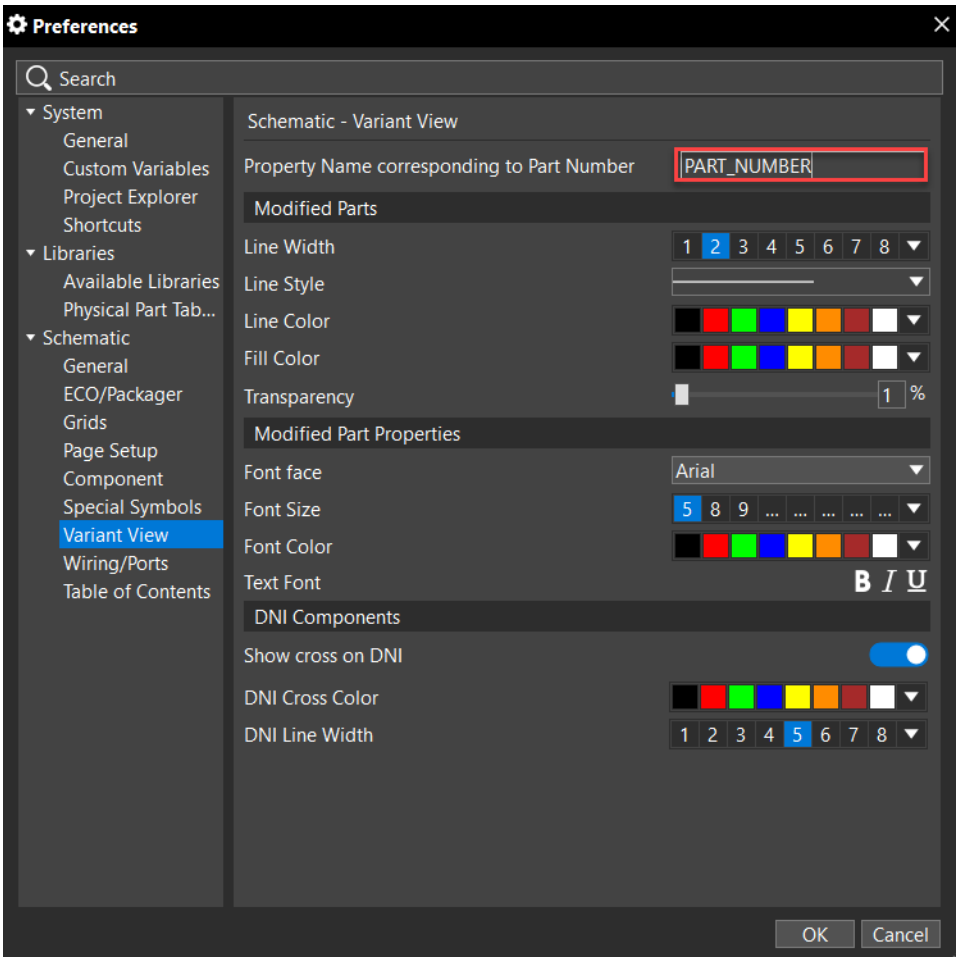
customize it in *Edit – Preferences – Variant View.*



To add components to the function in *Variant Editor*, follow these steps:

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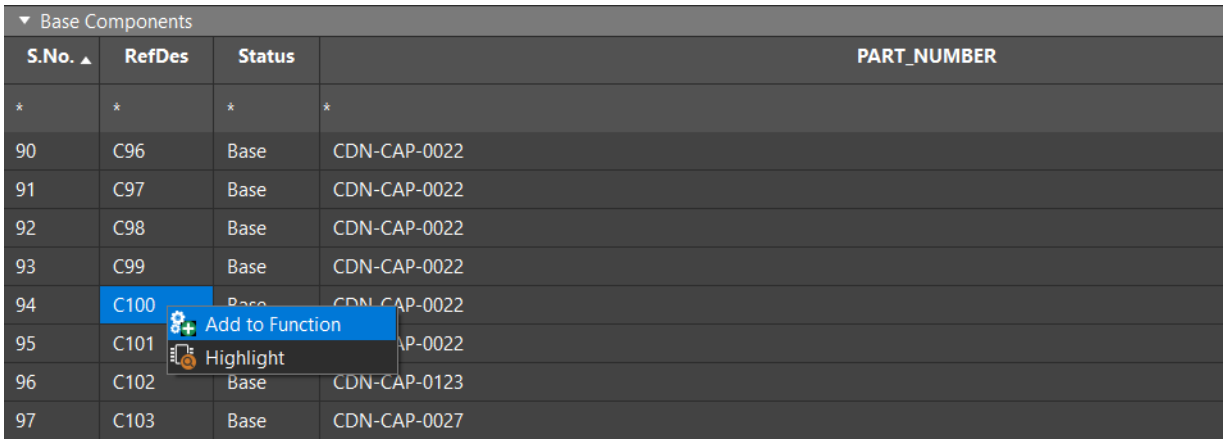
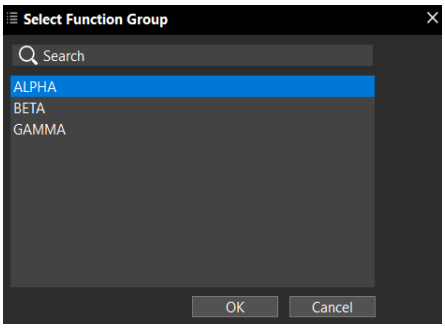
4. Right-click any component in the *Base Components* list and select *Add to Function*.



A dialog box listing the different function groups opens.

5. Select the function group to add the base component to.



6. Click *OK*.

The newly added component will now display in the *Function Group* section.

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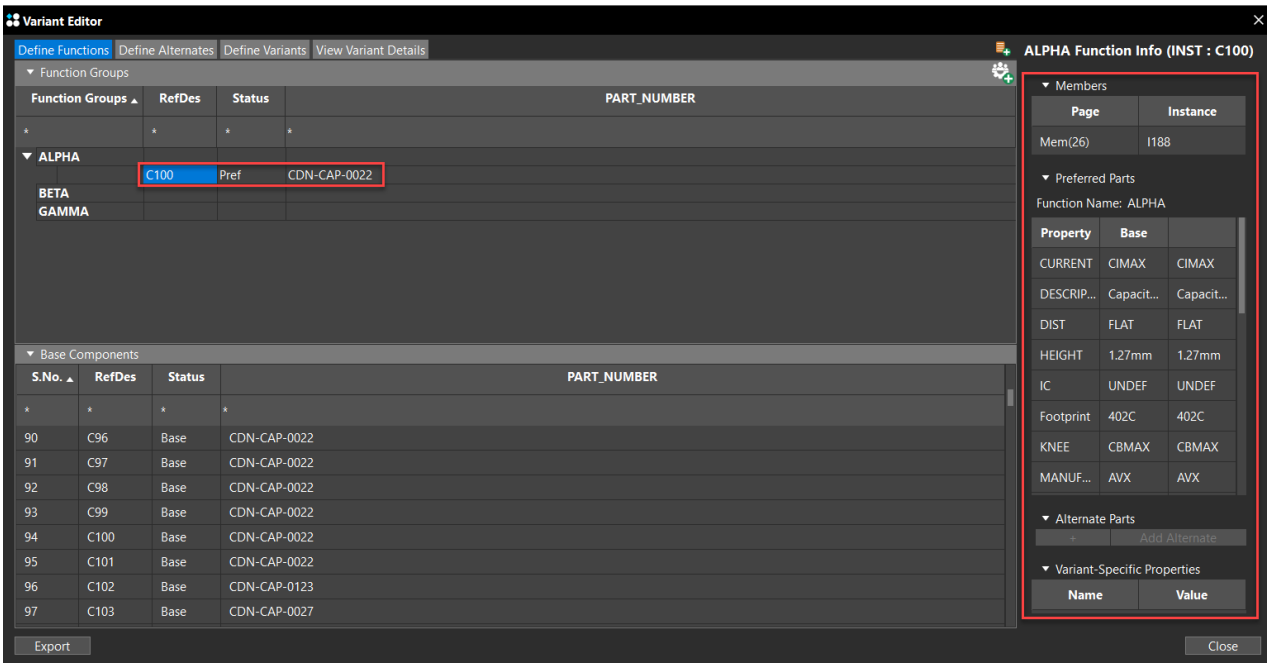
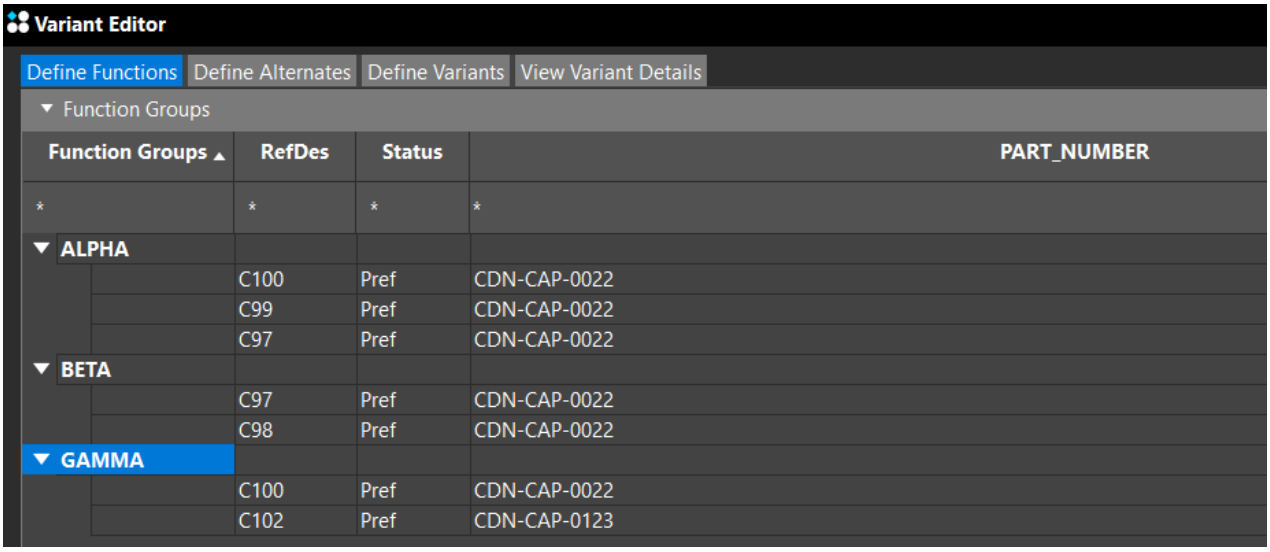
7. Click the component within the function group.



Clicking on any component in the *Base Components* or *Function Groups* section will display the base or variant specific properties for that component. It also displays the instance name of that component.

8. Add two more components to the `Alpha` function group and two each to `Beta` and `Gamma` function groups.



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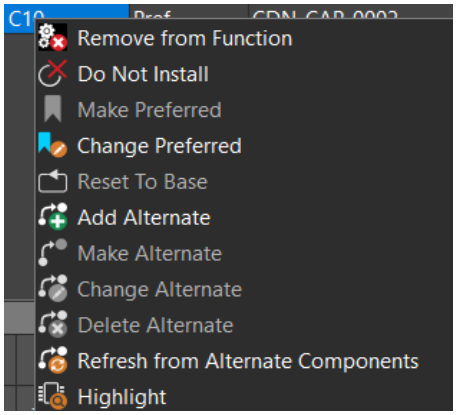
9. Click *OK*.

The component is added to the selected function and displayed in the table.

You can also select multiple components to add to the function group together by pressing the `Shift` key. Each added function will be displayed in the *Define Variants* tab of the *Variant Editor* with the respective components. By default, the function will not be added to any of the variants.

10. Right-click on any component in the *Function Groups* section.



You can perform the following operations on the part:

- *Remove from Function*: Removes the part from the function
- *Do Not Install*: The part will not be installed in the function. Will display a DNI icon on the part.
- *Make Preferred*: Active in the right-click menu of an alternate component. On clicking, the part will become the preferred part. This will be inactive in case it is a preferred part.
- *Change Preferred*: Active in the right-click menu of a preferred part. Will display a pop up menu to select a new preferred part.
- *Reset To Base*: Resets the component to the base schematic value.
- *Add Alternate*: Additionally, you can define up to 99 alternate values.
- *Make Alternate*: By default, the value of the component on the base schematic is considered the preferred value. You can change this value.
- *Delete Alternate*: To delete the alternate part. Active only for alternate parts.
- *Change Alternate*: To change alternate part. Active only for alternate parts.

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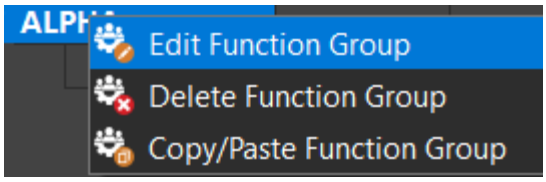
11. Right-click any function group.



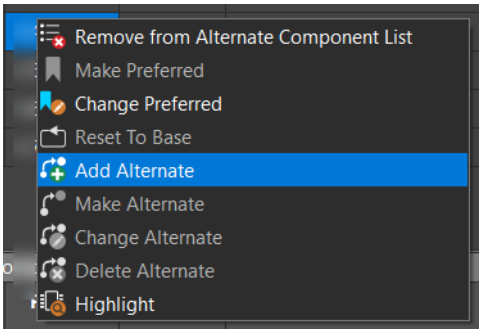
A pop-up menu containing the operations you can perform on function groups opens. They are:

- *Edit Function Group*: To edit the name or description of the function group
- *Delete Function Group:* To delete a function group
- *Copy/Paste Function Group:* To copy and paste a function group

12. Right-click any component in the Variant Editor and click *Highlight* to cross-probe. This takes you to the component in the schematic.

13. Select any component in the schematic. This highlights the component in the *Variant Editor*.

14. From *Define Alternates* tab, right-click a component and select *Add Alternate.*



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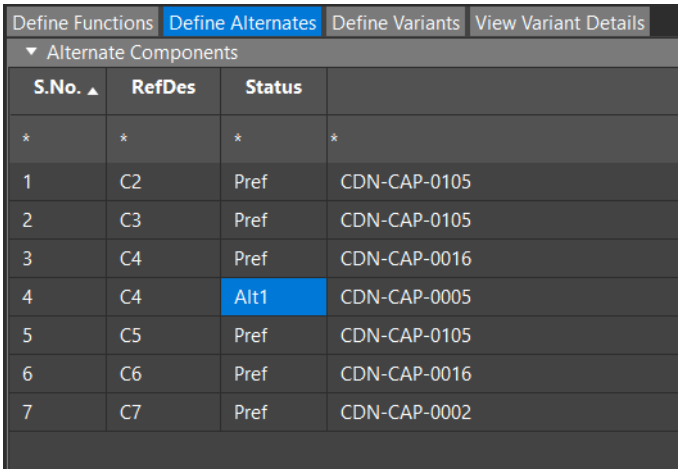
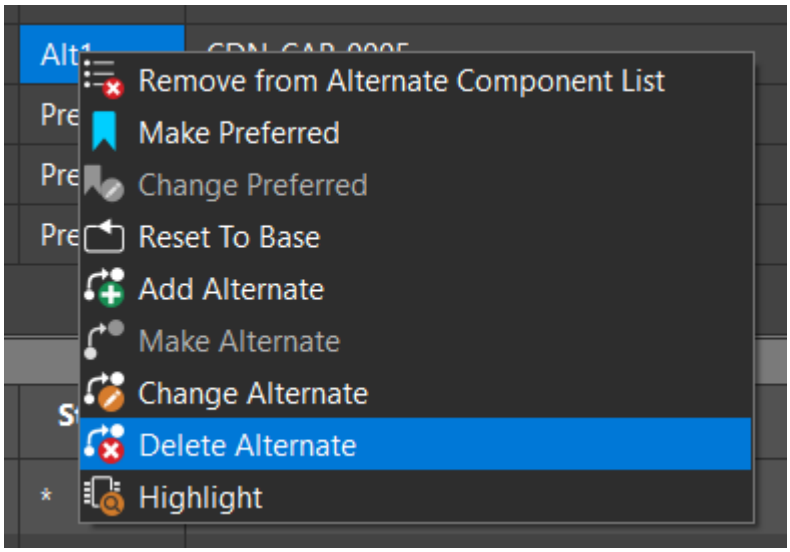
The alternate is added.



15. Right-click the alternate component and click *Delete Alternate*. The alternate is deleted.



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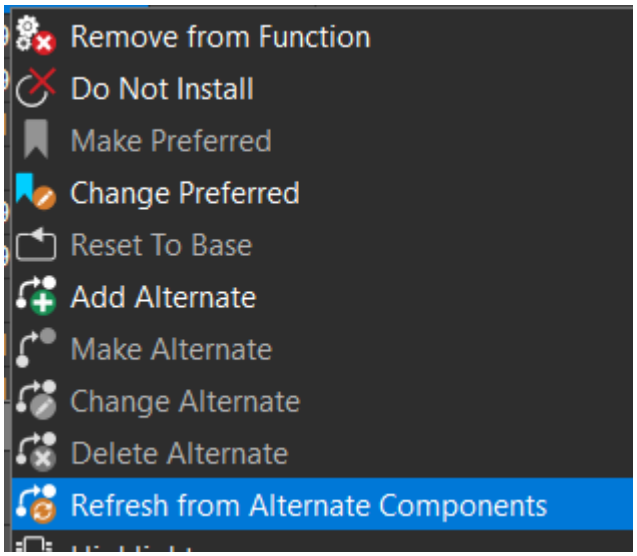
16. To verify this in the *Define Functions* tab, right-click the component, and click *Refresh from Alternate Components*.



The deleted alternate will be removed from the list.

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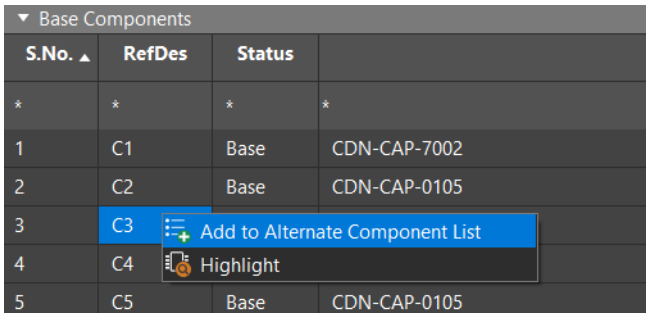
Defining Alternates in the Variant Editor

By default, the value of a component on the base schematic is the preferred value. However, you are not limited to using this value. You can change the preferred value and define up to 99 alternate values for the component.

Any of these alternate values can be used to replace the preferred value of the component. When you define an alternate value for a component, you can select only those values that have the same footprint.

To define alternates from the *Define Alternates* tab of the *Variant Editor*:

1. Choose *Variants – Variant Editor*.
2. Click *Define Alternates*.
3. Right-click a component from the *Base Components* list and select Add to *Alternate Component List*.



The component will be removed from the Base Components section and added to the Alternate Components section on top.

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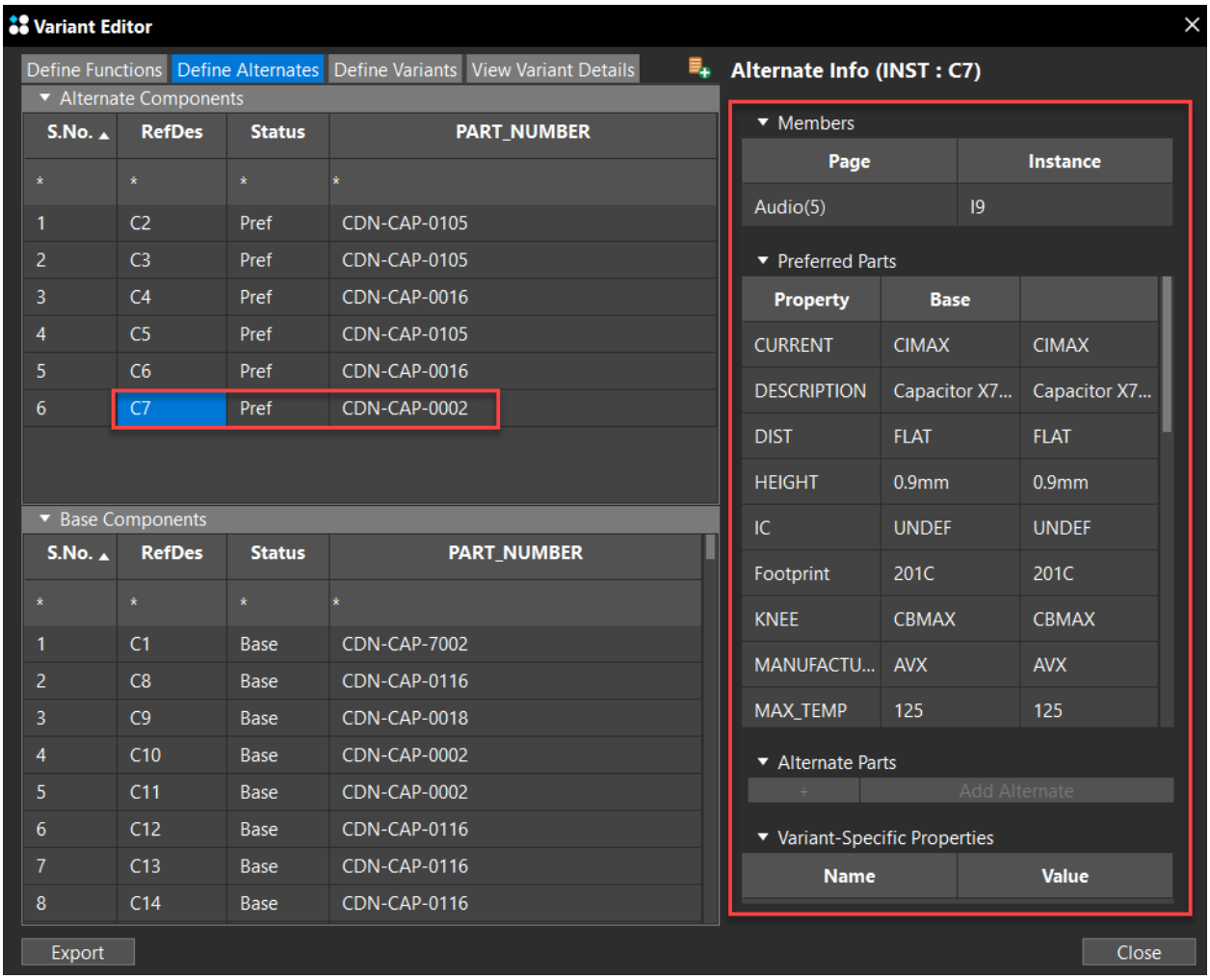
4. Click on any component in the *Alternate Components* section.



Properties for this alternate part will be displayed in the right-hand side panel.

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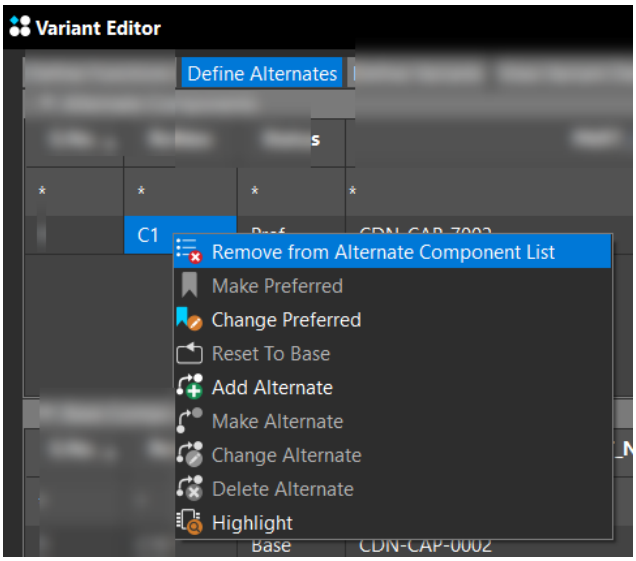
5. Right-click an alternate component in the *Alternate Components* section.



A pop-up menu having the following options opens up:

- *Remove from Alternate Component List*
- *Make Preferred*: This will be active for alternate components. Makes the alternate component as the preferred component.
- *Change Preferred:* This active for preferred components. Changes the preferred part.
- *Reset To Base:* Resets the component to the base schematic value.
- *Add Alternate:* Adds an alternate component.
- *Make Alternate:* Makes a preferred component as the alternate component.
- *Change Alternate:* Changes the alternate component.
- *Delete Alternate:* Deletes an alternate component.

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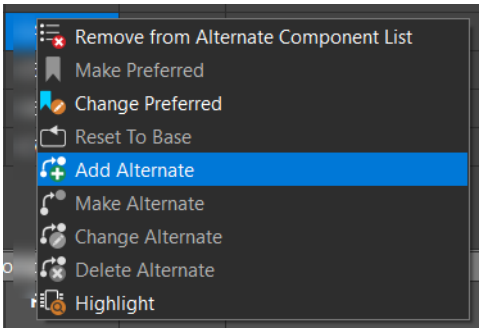
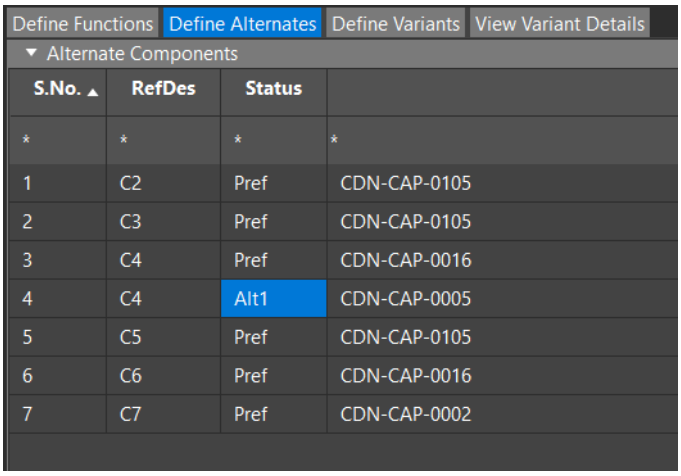
6. Select *Add Alternate.*



7. Search for a component with matching footprint.
8. Double-click the component.

   The alternate is added.



S.No.	RefDes	Status	
*	*	*	*
1	C2	Pref	CDN-CAP-0105
2	C3	Pref	CDN-CAP-0105
3	C4	Pref	CDN-CAP-0016
4	C4	Alt1	CDN-CAP-0005
5	C5	Pref	CDN-CAP-0105
6	C6	Pref	CDN-CAP-0016
7	C7	Pref	CDN-CAP-0002

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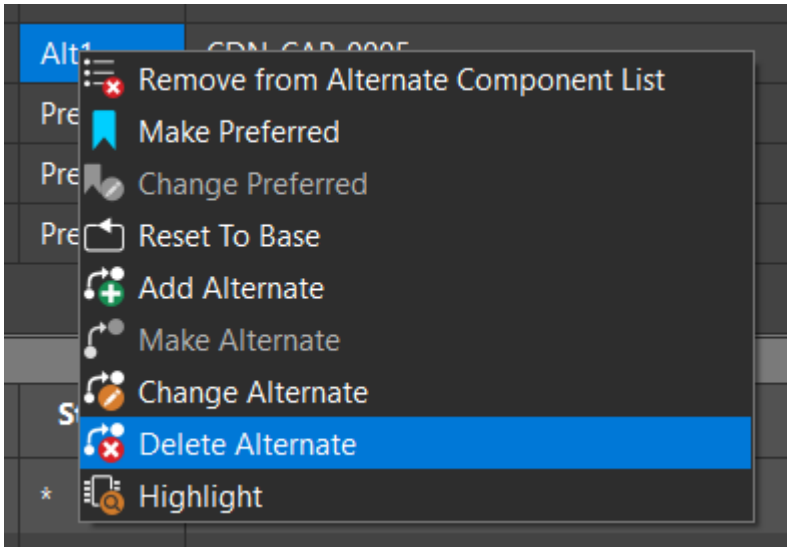
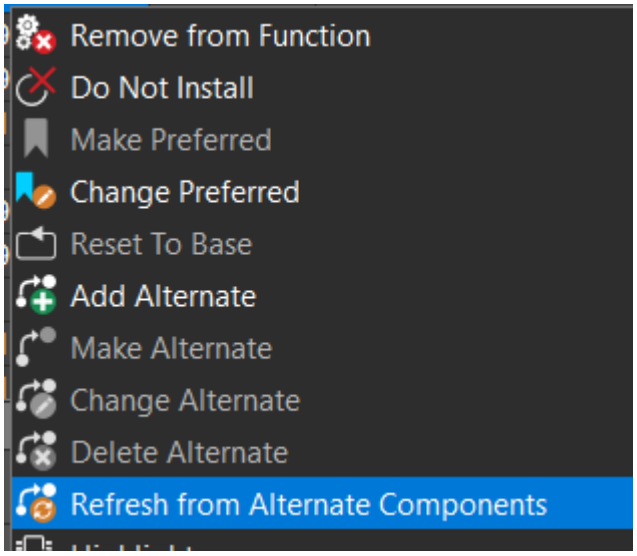
9. Right-click the alternate component and click *Delete Alternate*. The alternate is deleted.



10. To verify this in the *Define Functions* tab, right-click the component, and click *Refresh from Alternate Components*.



The deleted alternate will be removed from the list.

11. Click *Remove From Alternate Component List.*

The component is now deleted from the alternate components.

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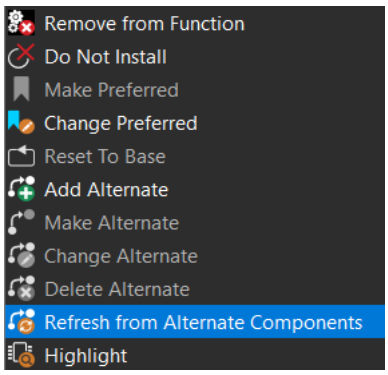
12. To verify this in *Define Functions* tab, right-click the component in function and select *Refresh from Alternate Components*.



This will update the component list to reflect that the alternate component has been removed.

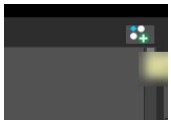
Defining Variants from the Variant Editor

Designers often need designs that differ from each other in minor ways. For example, designs may need to be customized for targeted market segments, destination countries, or feature sets. These differences are often small and are made of incremental changes on the base design. For example, you might need two designs, USA and India, that have only one difference, which is in the resistance value of one resistor. However, creating these differences is often difficult. You can end up repeating the whole design cycle for each design.

Using the *Define Variant* tab in *Variant Editor* you can create and manage designs that are different from each other by minor differences (these designs are also called variants). All you have to do is to create the base design in System Capture and then define the variant component in the Cadence tool called Variant Editor. In the example of the USA and India designs, first create the base design, say USA, and then define the changed resistor in the India design.Without resorting to complex editing of text files, you can define variant components, generate Bill of Materials (BOM) reports, annotate special designators to any components, annotate variant data, and merge variant databases using Variant Editor.

To create a variant from the Variant Editor:

1. Click the + icon from top-right of the *Define Variants* tab.



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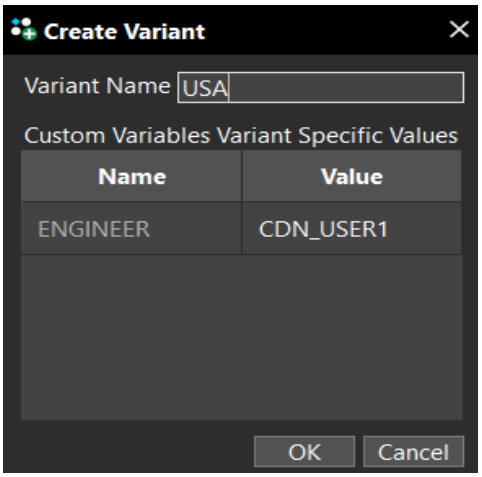
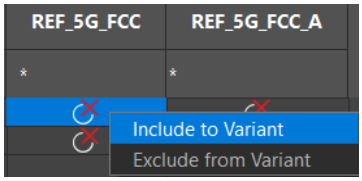
2. Enter the new variant name.



3. Click *OK*.

To add functions to variants using *Variant Editor*:

1. Right-click the variant column cell in the function row.
2. Select *Include to Variant*.



3. To exclude from variant, right-click the same cell and select *Exclude from Variant*.

   Note: In the *Define Variants* tab, variant related operations cannot be done for parts that are part of function groups.

For components, the following operations can be performed from the Define Variants tab of the Variant Editor:

- *Do Not Install*: To remove from the variant
- *Reset To Base*: To reset to base components list and remove from the variant
- *Add Preferred*: To add preferred parts

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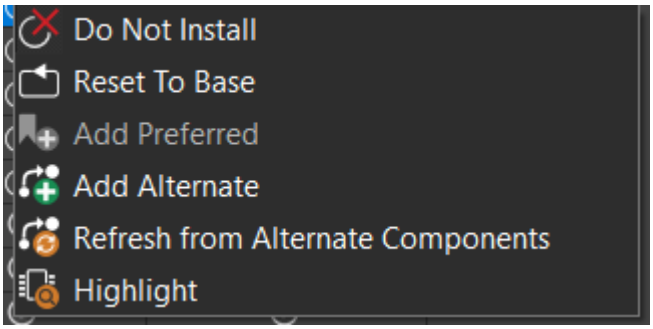
- *Add Alternate*: To add alternate parts



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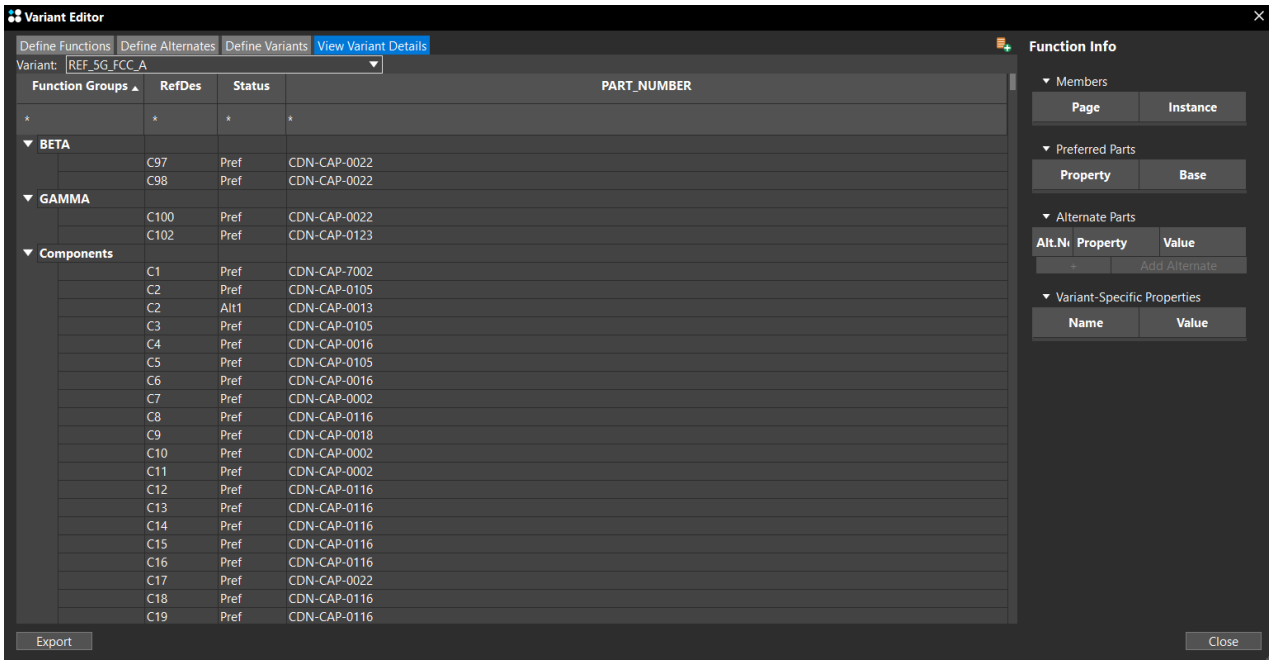
Viewing Variant Details in Variant Editor

To view variant details from the *Variant Editor*, click *View Variant Details* tab.

Select the variant you need to view the details for from the drop down menu. A list of components in that Variant will be displayed. You can also view the function groups included in that variant. Moreover, you can verify the preferred parts and alternate parts in the variant info panel on the right.

To export data of a selected Variant into a `.csv` file:

1. Click the *Export* button at the bottom-left corner of the *Variant Editor*.



2. Enter the name of the file as `Variant_data` and click *Save*.

   The data for a selected variant of the design is now exported into a `.csv` file.

3. Close *Variant Editor* and double-click the `.csv` file to open it.

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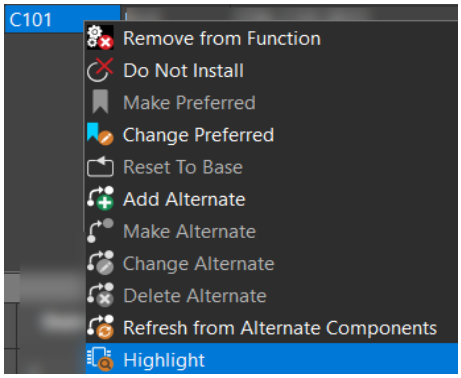
Cross-Probing

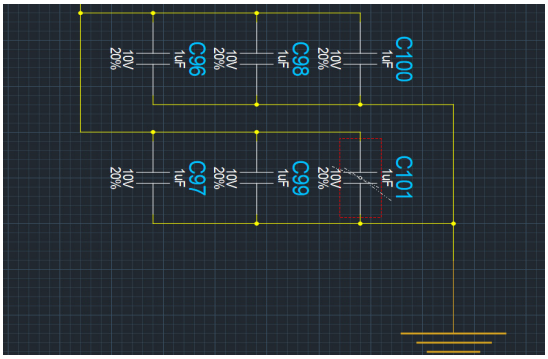
Apart from defining functions, alternates, variants from the *Variant Editor*, you can cross-probe the component from the *Variant Editor* to Schematic and vice-versa to view the component placement and location on schematic.

To cross-probe the component from the *Variant Editor* to Schematic, follow these steps:

1. From the *Define Functions* tab, right-click any component and select *Highlight*.



You can do this from any tab of the *Variant Editor*. The component gets cross-probed to the schematic.



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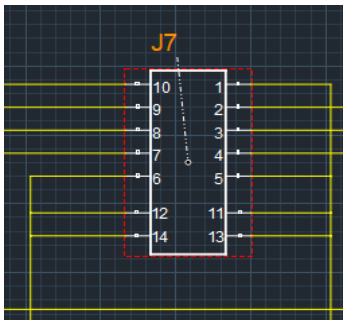
2. Search and select J(7) on the canvas.



Notice that on selecting the component on canvas, it gets highlighted in the *Variant Editor* on the last active tab.

Base Components

S.No.	RefDes	Status	PART_NUMBER
*	*	*	*
604	J5	Base	CDN-AXE510124
605	J6	Base	CDN-BM24-50DS
606	J7	Base	CDN-AXE510124
607	J8	Base	CDN-AXE534127D
608	J9	Base	CDN-AXE530127D
609	J10	Base	CDN-AXE114124
610	J11	Base	CDN-20449_001E
611	J12	Base	CDN-ANT1400

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9

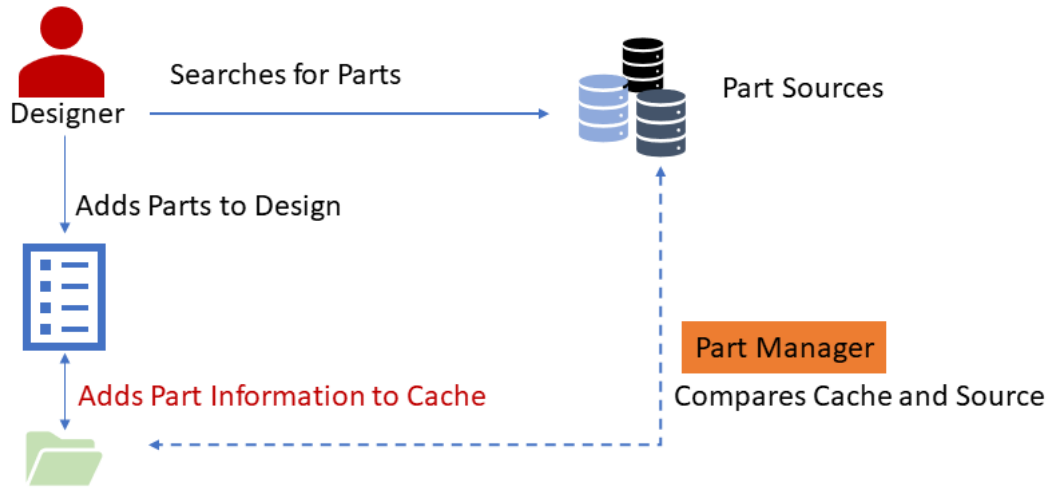
Synchronizing Designs and Libraries with Part Manager

Designers search for parts in libraries or external sources with *Unified Search* and add them to their designs. Information about the parts, such as symbols, are stored in a local project cache and all the properties are stored with the design instances.

Part Manager Overview

The reference libraries are often updated with the part changes and modifications in the values of properties. These changes in the reference libraries need to be passed on to the designs. Part Manager compares the parts in the design with their sources and synchronizes design data with the reference library.

Here is a pictorial overview:



When Part Manager is run on a design that was created in an earlier version of System Capture, a few internal properties are also added to the part instance. These internal

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properties establish a link between the part instance in the design with its source in the reference library.

You can annotate all the properties on the schematic or a selected set of properties by using the `ANNOTATE_ALL_PROPS` directive. In case only a selected set of properties is annotated, the rest of the properties are retrieved from the reference libraries at the time of generating a netlist. The internal properties are used for identifying the relevant information from the source libraries.

Since the properties are no longer part of the design cache, multiple users can simultaneously work on a design and add parts without getting causing a conflict of part properties in the design cache. This also makes working on a design independent of the source of reference library. That is, regardless of the library sources, DE-HDL, OrCAD Capture, or external part providers, the System Capture behavior and use models remain the same. All the properties from the source are annotated on the part instance in the schematic.

Understanding Part Status

When Part Manager compares the parts in the design with their sources, it identifies the following scenarios and categorizes them:

Scenario	Part Status
A match exists in the reference library for the part in the design and parts in the design are same as that in reference library.	*In Sync*
A match is found in the reference library for the part in the design, but it has some changes. Part Manager can automatically synchronize these changes in the design.	*Auto Sync*
No match was found in the reference library for the part in the design. You need to manually select a part from the reference library and synchronize the part.	*Manual Sync*

Note: If you are working a design that was created from a DE-HDL design and was set up for uppercase input such that library properties are annotated in uppercase, while the part definition (PTF) has properties in mixed case, these properties get flagged as not-in-sync because Part Manager does case-sensitive comparison.

In case the parts in the design are not synchronized with their source, you can either update the design and the cache with the latest data from the reference library, or continue with the cached parts.

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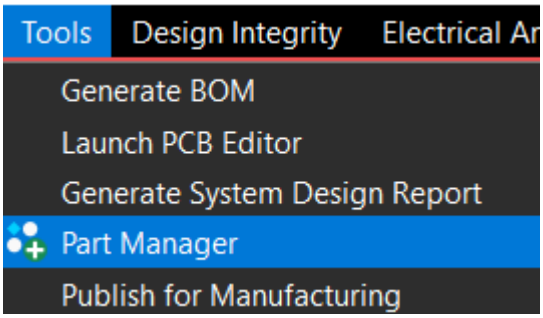
Running Part Manager

Running Part Manager is critical before the netlist is generated for translating the schematic design to layout files to ensure the part information in the design is correct and latest.

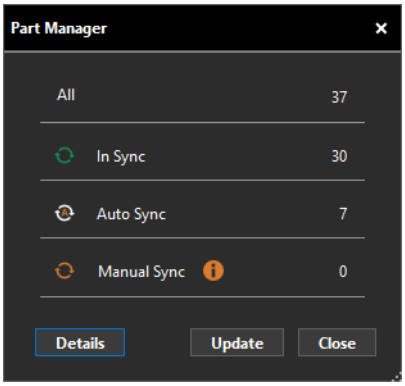
Caution

If a design has manual sync errors, it cannot be exported to layout.

1. Open a design.
2. Choose *Tools – Part Manager*.



The design is compared with the reference libraries using the Part Manager utility. And a summary is displayed.



If all the parts in the design are in-sync, the summary dialog displays with just the *Close* button. In case there are some out-of-sync parts in a design, the *Details* and *Update* buttons are also available on the dialog.

Note: Part Manager does not compare the visibility settings of properties of parts.

3. Click *Details*.

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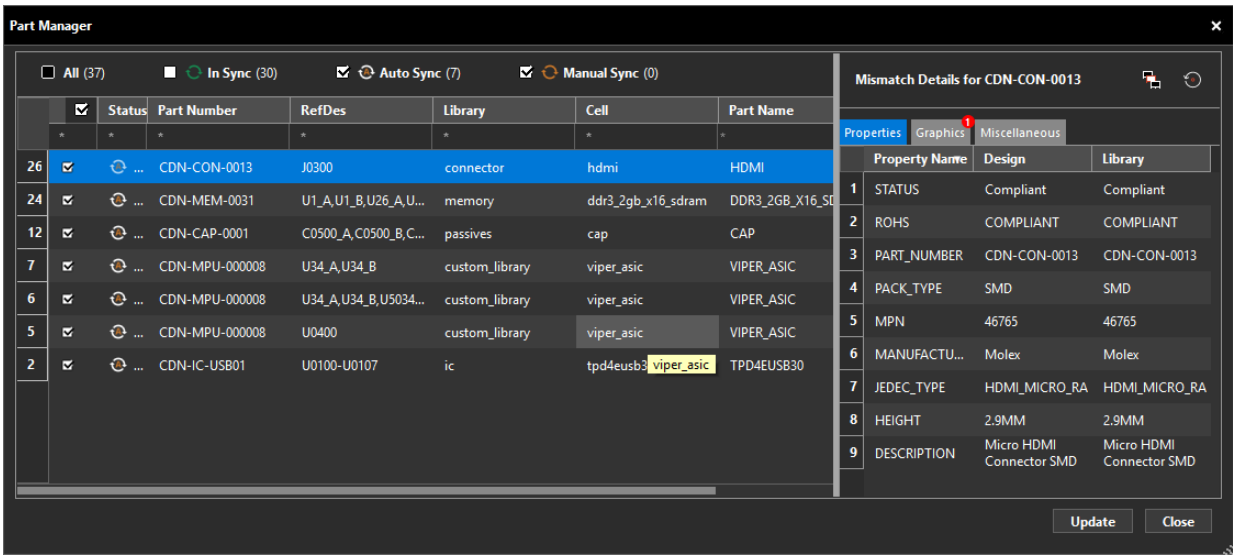
This opens the detailed *Part Manager* dialog.



4. Select the categories you want to include in the right table.

For example, *Auto Sync* and *Manual Sync*.

5. Review each row of the table.

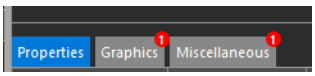
a. Select the update check box for each row

- In Sync – The check box is unchecked and disabled
- Auto Sync – The check box enabled and checked indicating that the part is ready to be updated.
- Manual Sync – The check box is unchecked and disabled. When manually resolved, the check box is enabled and checked, indicating that the part is now ready to be updated**.**

b. Review the details of the selected part in the right pane.

In the right pane, the details are categorized in three columns, *Properties*, *Graphics*, and *Miscellaneous*:

- Number of differences (if any) in each category is displayed as a superscript in red on the tab header



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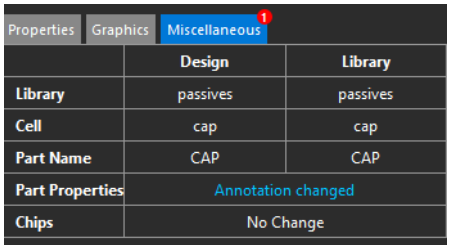
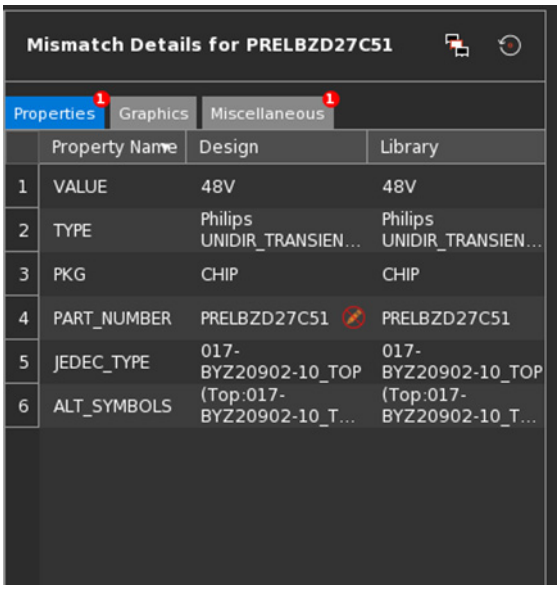
- Annotation changes are reported in the *Miscellaneous* tab.



- The property type is reported.



For read-only properties (key properties), an icon indicates that it cannot be edited.

6. Select a different part to synchronize.
7. Reset to discard any changes.
8. Click *Update* to synchronize all the parts, which were selected for synchronization.

   Part Manager updates the design data with the data from the reference library, and makes the data consistent for the selected parts. The *Part Manager* window is updated and reflects the result of synchronization.

Important

If the *Update* command fails, check if the libraries have incorrect values or unsupported property names.

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9. Click *Close*.

Impact of Design Tasks on Part Status

When adding parts, blocks, sheets, or copying pages from other designs, remember the following to avoid any potential problems:

When you	What happens	You need to
Import an editable (read-write) block	Its parts come in as is System Capture does not read its part table information, only the properties in the schematic are read into the destination.	Run Part Manager to sync the parts from the imported block with the reference libraries of the destination design.
Import a read-only block	Its parts come in as in	Reimport the block whenever the source design is updated because Part Manager cannot update the parts in a read-only block. This is also why you cannot select parts from read-only blocks for updating in Part Manager.
Add a new part	An instance gets placed with the latest part properties ***without any change*** in already placed instances of the same part	Run Part Manager Multiple rows would show for the same part. The newest instance would be in-sync and the older ones might need to be synchronized.

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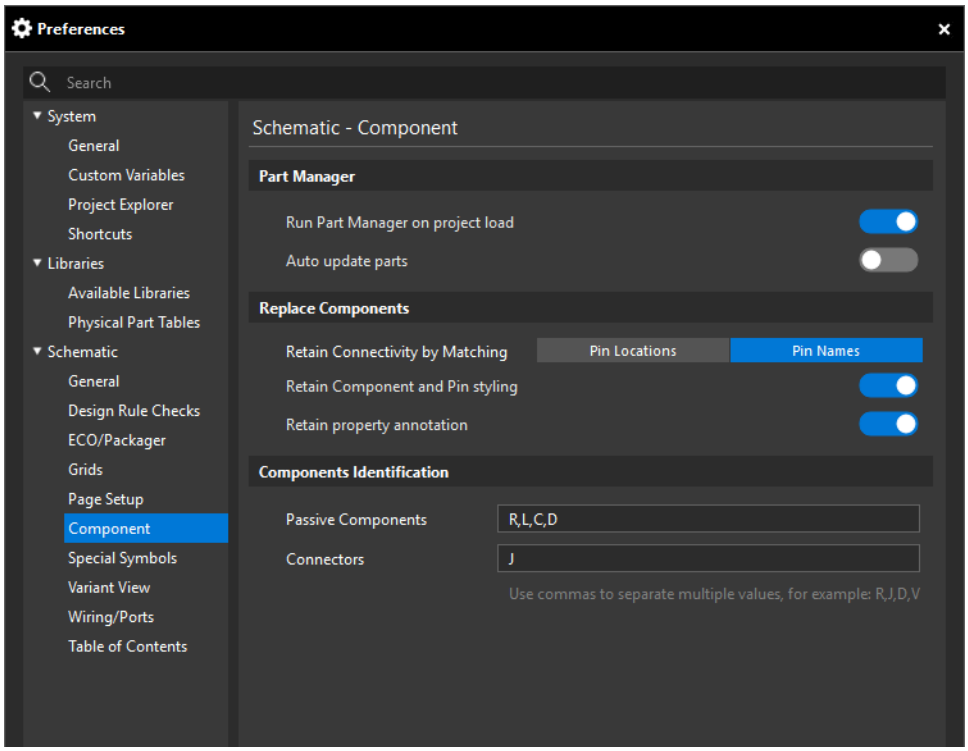
When you	What happens	You need to
Paste components or pages from another design	All library properties get associated just as if the component were added	Run Part Manager to ensure the newly added parts are in sync with the destination libraries If the component being added does not match any row in the reference library, additional properties do not get added. In such a case, a manual update would be required in Part Manager.

Running Part Manager at Design Load

You can configure System Capture to run Part Manager when a design is opened.

1. Choose *Edit – Preferences*
2. Choose the *Schematic – Component*
3. Enable *Run Part Manager on project load* in the *Component* tab of *Preferences.*



A tooltip informs you that the changes will come into effect in the next launch.

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4. Restart System Capture.

Part Manager will be launched when any design is now opened.

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10

Integrated Layout

System Capture is an integrated design environment where you can work on nearly every aspect of the design process without switching to another external application, such as creating parts, libraries, schematics, adding parts, and so on. This environment also includes the ability to view, create, and modify layout files. You can view a layout file that is created when you export a schematic to physical layout, using the *Export to Layout* command, create new board files, open existing board files that are not related to the currently open design, and even create a board file for the schematic design without having to specify the large number of initial settings.

Important

To perform the tasks described in this section, select any of the following licenses:

- `Allegro X EE`
- `Allegro X Designer`
- `Allegro X Designer Plus`

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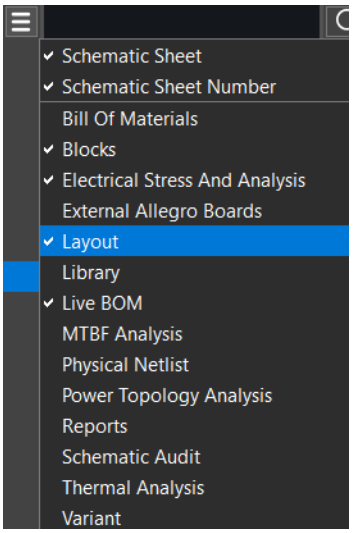
Board Files in System Capture

System Capture comes with a basic layout viewer that enables designers to check the schematic and layout files simultaneously. While the complete range of layout tasks is available in applications such as PCB Editor, the benefit of in-tool layout abilities is that an additional application does not need to be launched or learned. You are in the same application and depending on the file you open, the window tabs and available options change. Having layout abilities and basic floorplanning features enables schematic designers to take better decisions during the initial design phase.

To work with a layout file in System Capture, perform these tasks:

1. Open a design.
2. Ensure *Layout* is displayed in the project explorer.

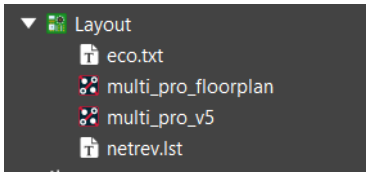
   You might need to change the *Project Explorer Settings*.



3. Locate the board file in the project.

   If you need to generate the physical file, follow the instructions in the Exporting Logical Design to Physical Design section.

4. Navigate to `<project name>` – *Layout.*



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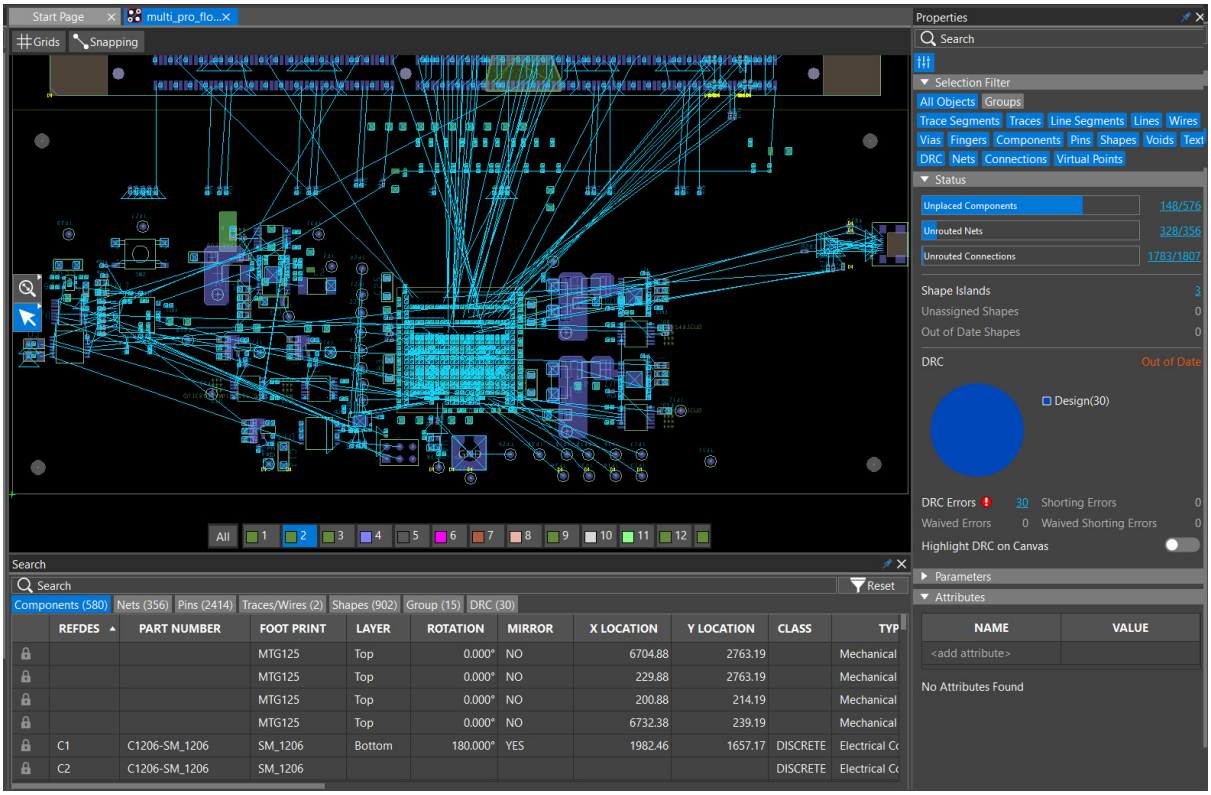
5. Double-click the `<board file name>`.

   The board file opens in a new tab.



Related Topics

Exporting Logical Design to Physical Design

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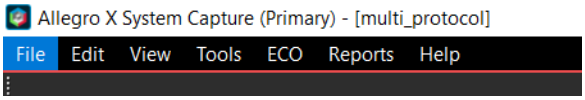
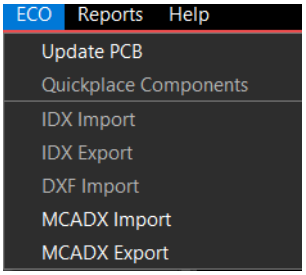
Layout Tasks Available From System Capture

When a board file is opened, the System Capture UI changes to display layout-related information and perform tasks on board files. Here is an overview of differences:

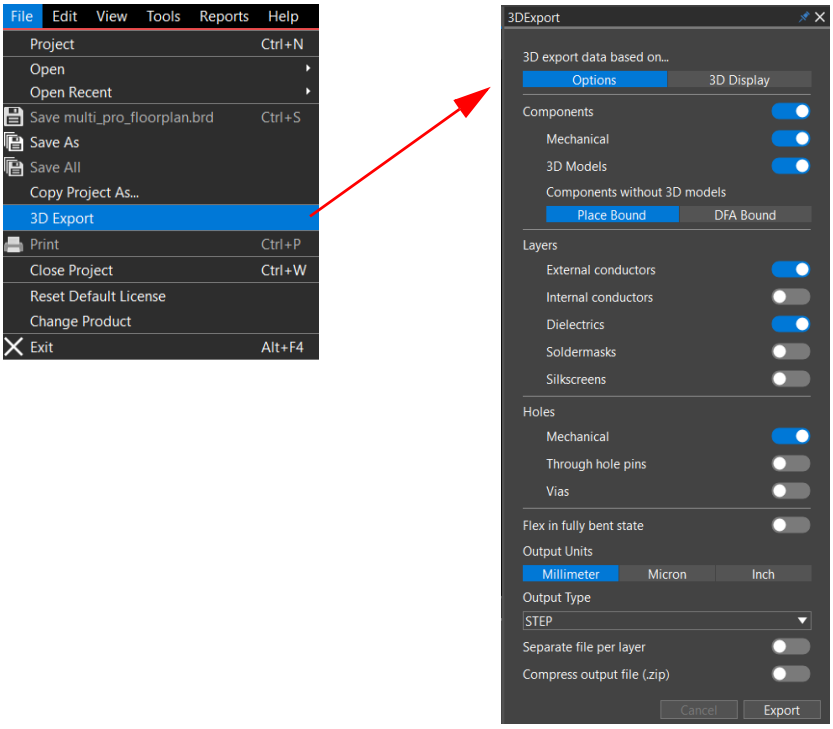
- The menu options change.



- A new *ECO menu* is available.



- A new option *3D Export* is added to the *File* menu.



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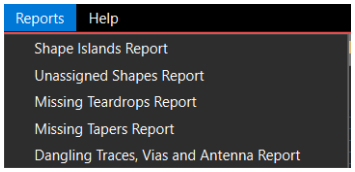
- Reports menu is added.



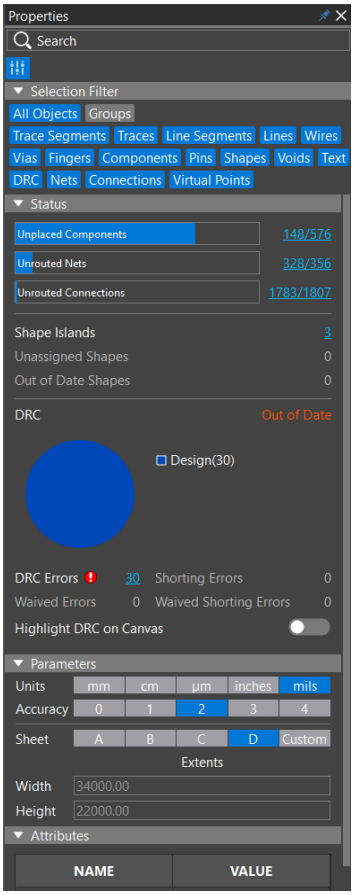
- Two icons display to the left of the canvas.

Zoom Fit

Select

Right-click the *Zoom Fit* icon for other viewing options.

- The *Properties* window shows details of the board file.



- *Viewing* control available on the top-right of the screen

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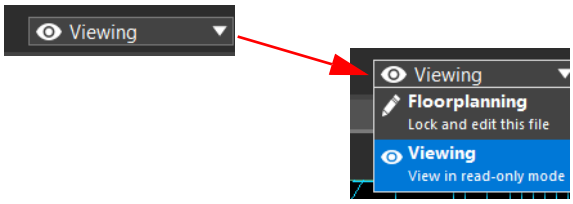
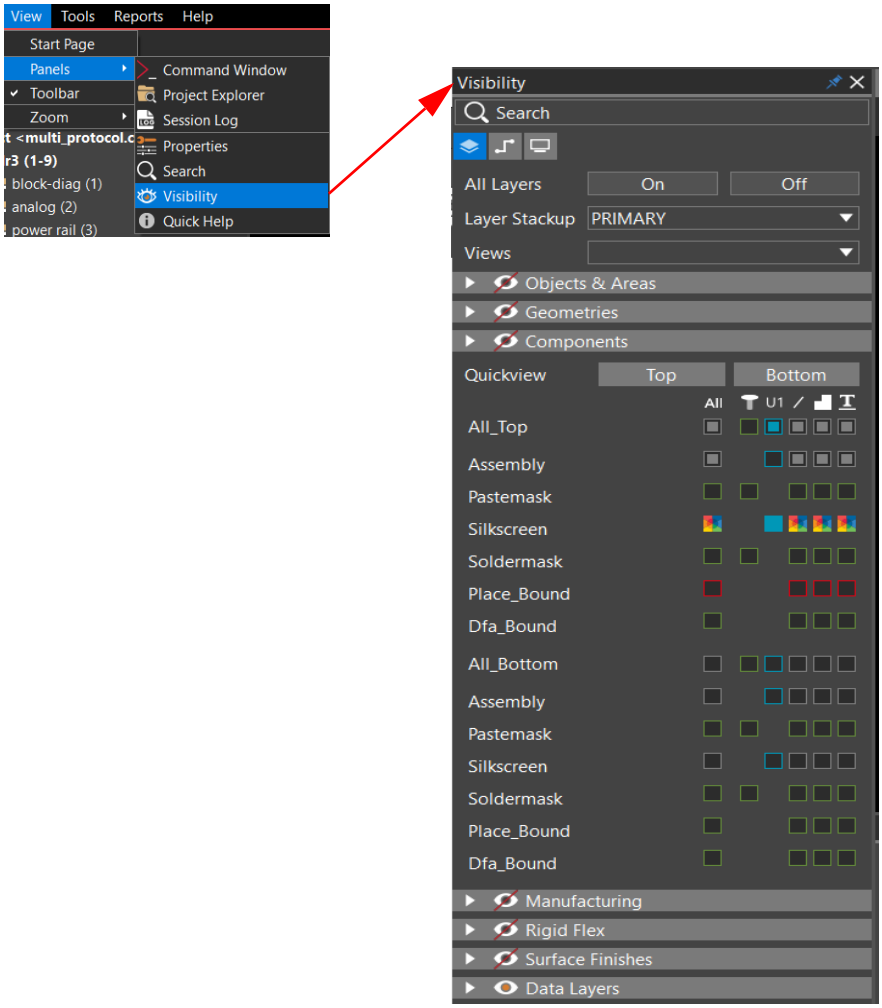
By default the board file is in the *Viewing* mode



You can switch to the floorplanning mode to make routing changes or populate a blank board file with the logic in the schematic pages.

See *Creating a Board File Using Default Settings* for details.

- A *Visibility* tab is available



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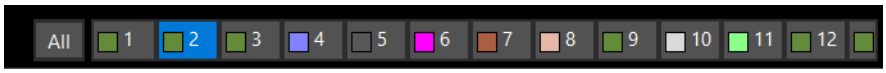
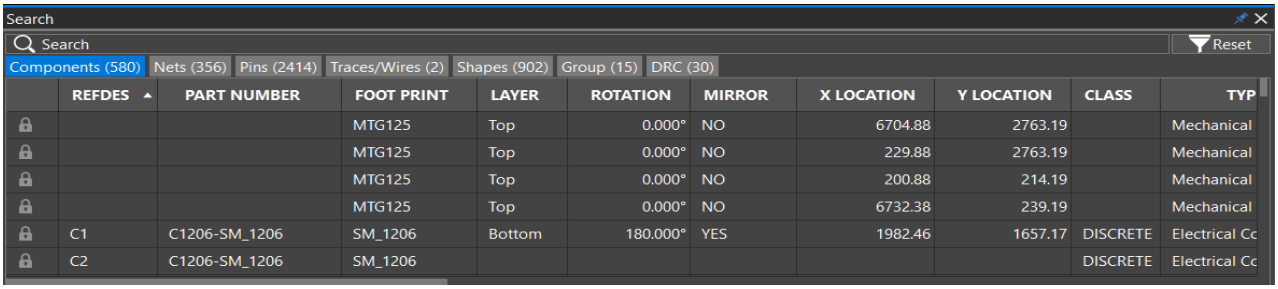
- Controls for displaying layers are available.



  - A *Search* window where you can see a list of all the design elements, such as components, nets, pins, traces, shapes, groups, and so on.



REFDES	PART NUMBER	FOOT PRINT	LAYER	ROTATION	MIRROR	X LOCATION	Y LOCATION	CLASS	TYP
		MTG125	Top	0.000°	NO	6704.88	2763.19		Mechanical
		MTG125	Top	0.000°	NO	229.88	2763.19		Mechanical
		MTG125	Top	0.000°	NO	200.88	214.19		Mechanical
		MTG125	Top	0.000°	NO	6732.38	239.19		Mechanical
C1	C1206-SM_1206	SM_1206	Bottom	180.000°	YES	1982.46	1657.17	DISCRETE	Electrical Cc
C2	C1206-SM_1206	SM_1206						DISCRETE	Electrical Cc

Related Topics

- 3D Export
- Markup
- Quickplace Components
- Generating Reports

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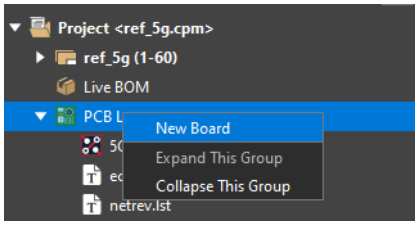
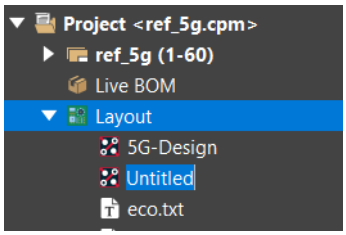
Creating a Board File Using Default Settings

To create a board file that is stored within the project, follow these steps:

1. Right-click *Layout* in *Project Explorer*.
2. Choose *New Board*.

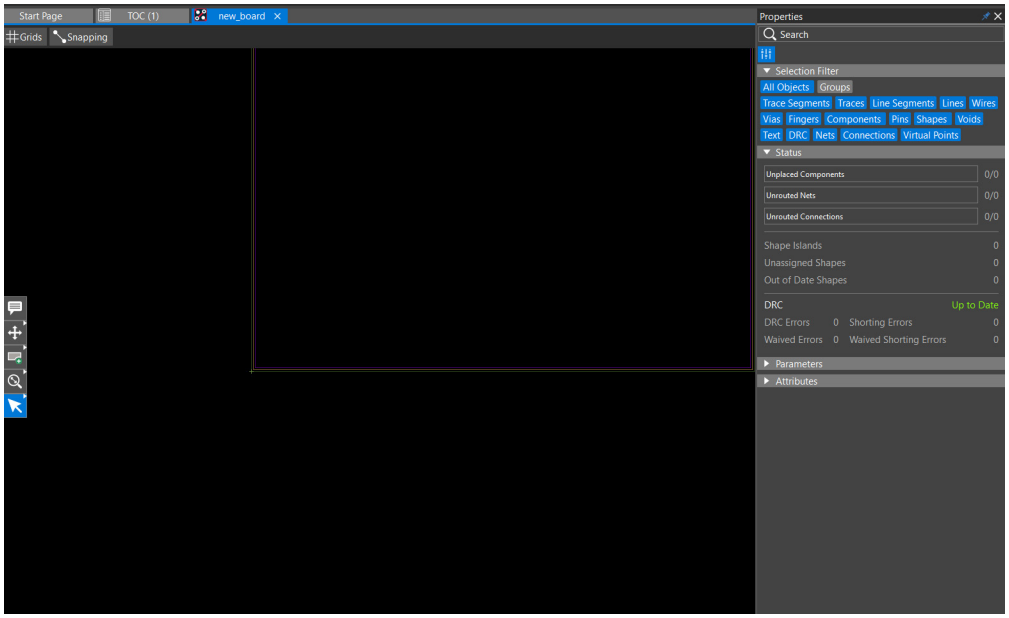


A new entry gets added labeled *Untitled*.



3. Specify a name and press `Enter`.

   The new board opens in a tab.



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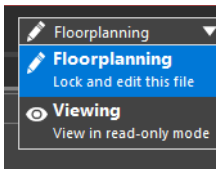
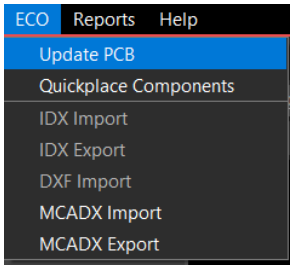
4. Change the mode to *Floorplanning*.



The *Floorplanning* feature this is available only with the *following* licenses:

- ❑ `Allegro X EE`
- ❑ `Allegro X Designer`
- ❑ `Allegro X Designer Plus`

5. Choose *ECO – Update PCB.*



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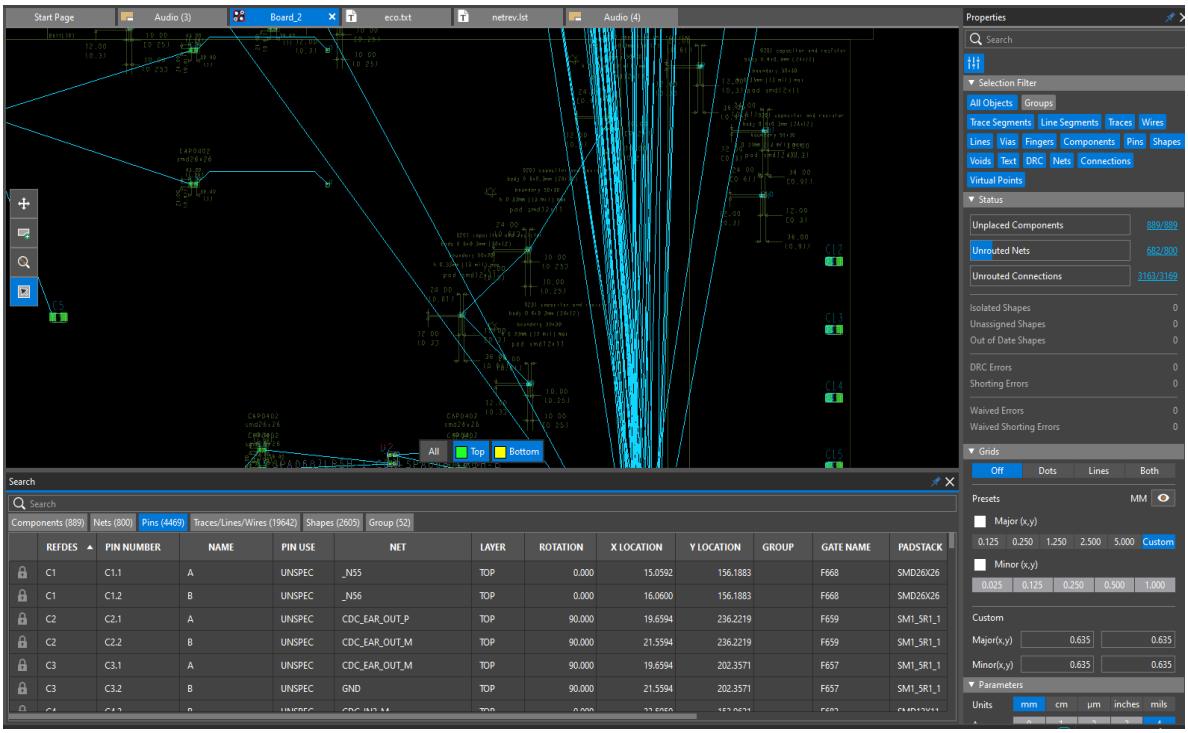
The logic specified in the schematic is translated and a partially routed board file is ready. The *Search* window is populated with all the design elements.



Some of the tasks you can perform are:

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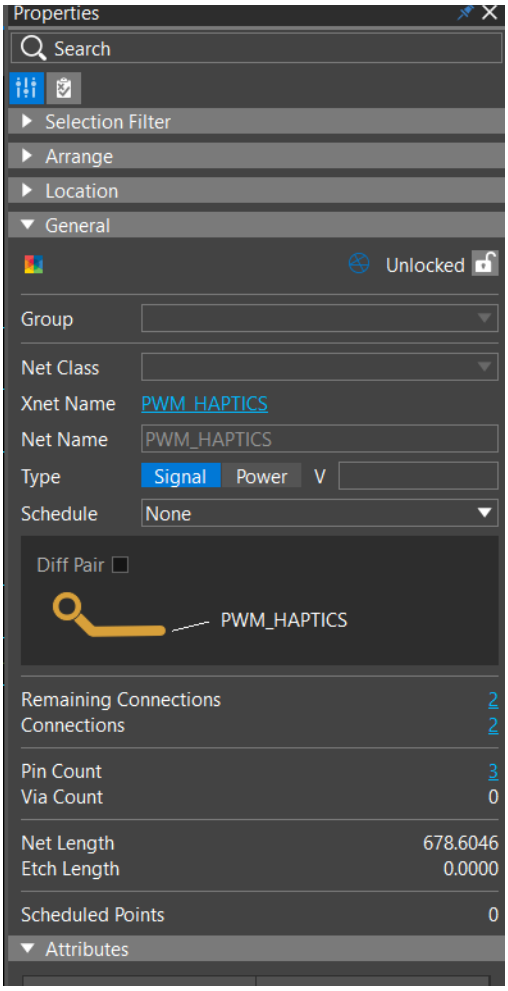
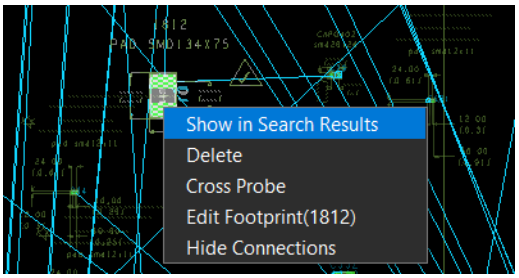
- Click any element on the canvas to look at its details in the *Properties* window.



- Right-click any element on the canvas and perform the actions shown in the following image.



The *Edit Footprint* command launches a different application, such as OrCAD X Presto.

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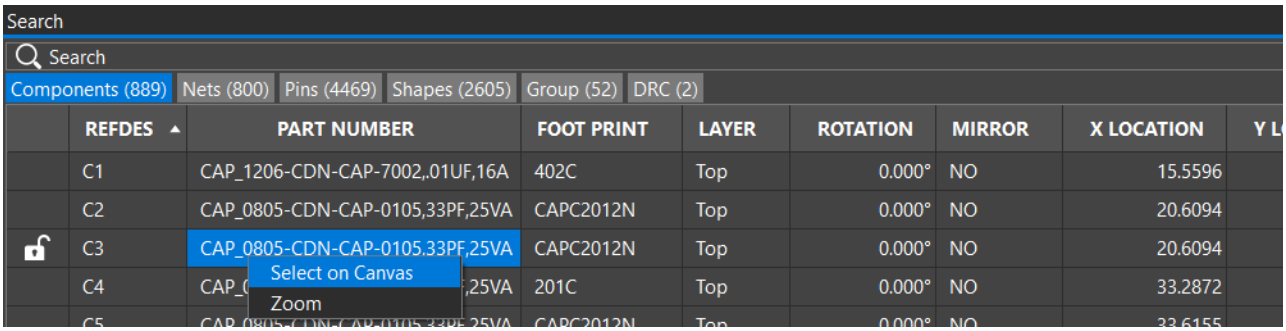
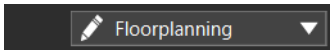
- Right-click any row in the Search results to select the design element on the canvas or zoom to the selected part.



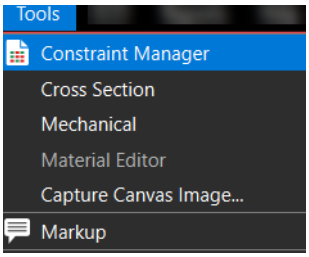
You can also double-click a row to display to the selected part.

- Launch Constraint Manager and extract topology.

Ensure you are in the *Floorplanning* mode.



a. Choose *Tools – Constraint Manager*.



Constraint Manager opens in a new window.

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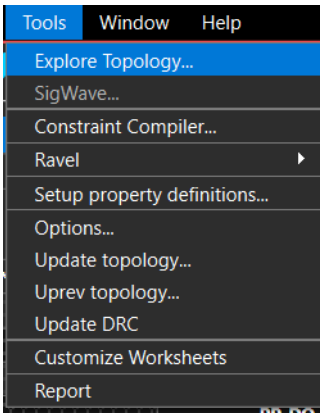
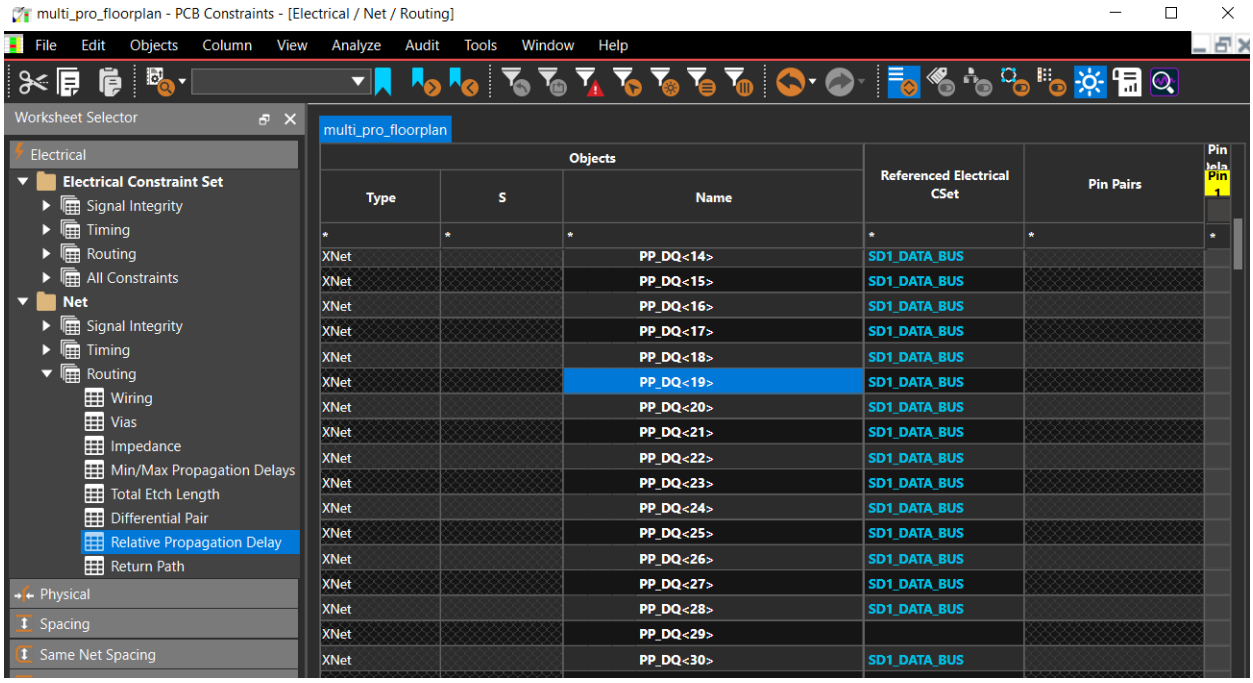
b. Launch Topology Workbench from the *Tools* menu.



Or,

Navigate to the sheet and object that you want to further investigate.



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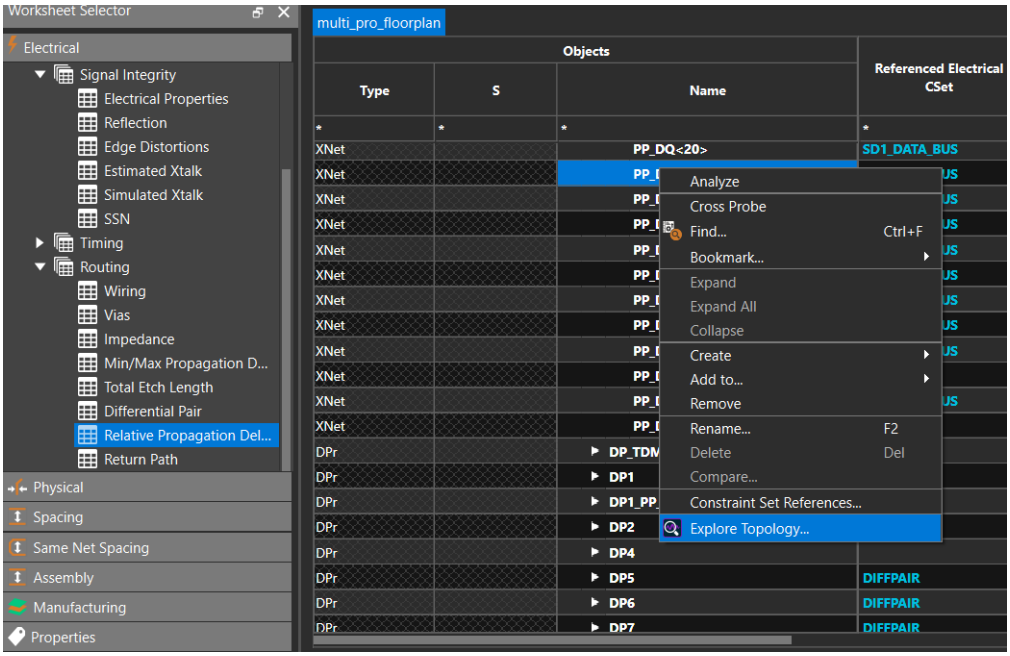
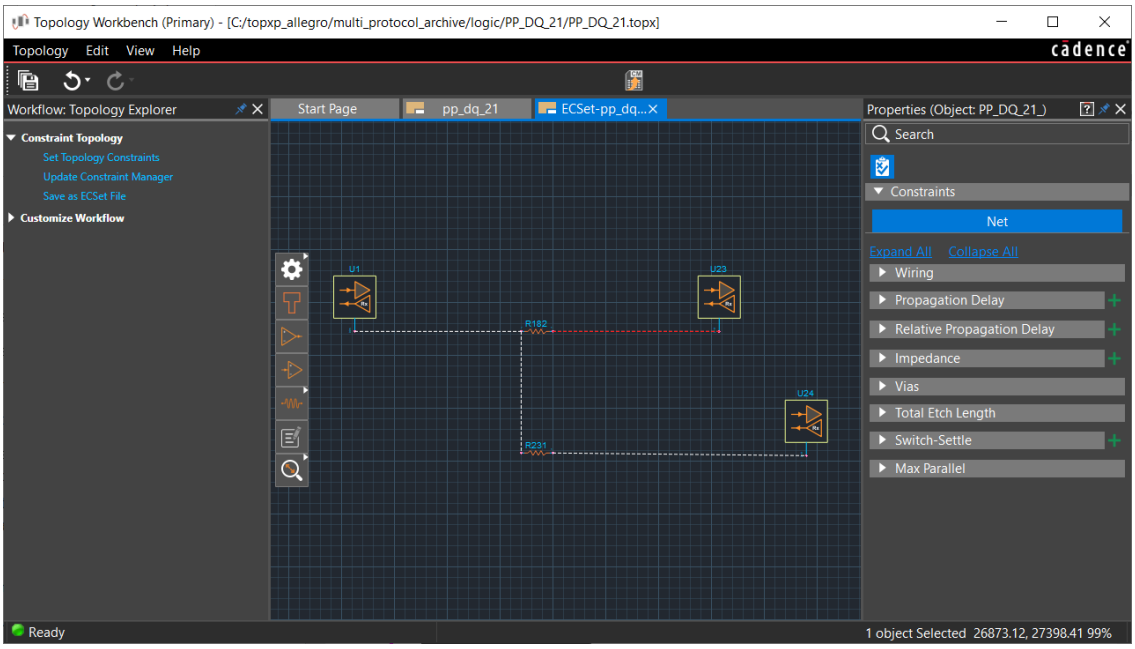
c. Right-click and choose *Explore Topology*.



Topology Workbench opens in a new window.



You can see and set the ECSet constraints here.

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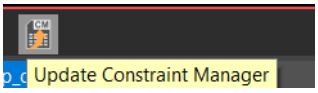
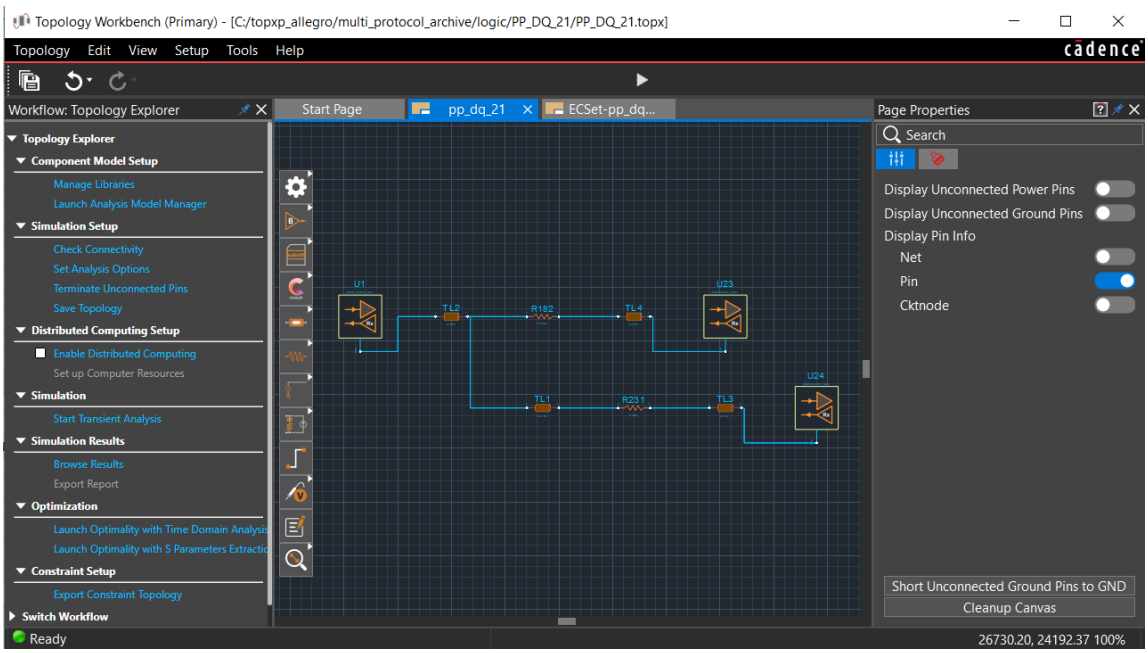
d. Click *Update Constraint Manager* in the Workflow panel or the icon.



You can also run simulation if the required applications are available and setup.



Related Topics

- Using Topology Explorer Workflow
- Workflow Panel
- Setting Constraints in Topology Workbench

Locating Design Parts Across Tabs

You can cross probe any element in a tab or from Search results to everywhere it is located in the design or even its entry in Constraint Manager. System Capture supports the following modes of cross-probing.

- Automatic cross-probing across all applications open from the instance of System Capture
- Explicit cross-probing the selected element

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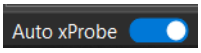
Tip

This feature is useful when working with multiple monitors. Dock the tab to a different workspace. On a single monitor, you need to move and resize the tabs to get the full benefit of this feature.

Automatic Cross-Probing

Automatic cross-probing can get resource-intensive when a large selection is made. Because every instance of every selected part is located and its tab page opened.

See the Auto xProbe control at the left of the status bar. This is a toggle control that gets applied to all the tabs in an instance. That is, if you enable or disable it on one tab, it gets applied to all.



When enabled, any selection on a tab, will also select the component in the other tabs.

Explicit Cross-Probing

If automatic cross-probing is enabled, even an accidental click or choosing a large selection, can prevent you from moving ahead with your tasks until all the instances are selected and relevant tabs opened. To avoid this, disable Auto xProbe and right-click a component and choose Cross Probe. This is available from the layout tab, schematic pages, and Constraint Manager.

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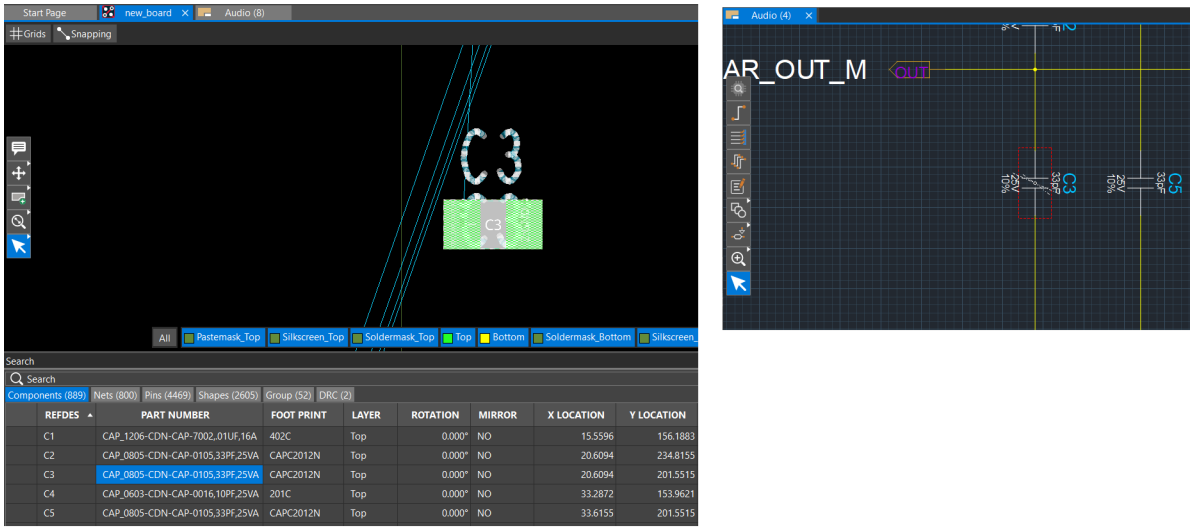

REFDES	PART NUMBER	FOOT PRINT	LAYER	ROTATION	MIRROR	X LOCATION	Y LOCATION
C1	CAP_1206-CDN-CAP-7002,,01UF,16A	402C	Top	0.000°	NO	15.5596	156.1883
C2	CAP_0805-CDN-CAP-0105,33PF,25VA	CAPC2012N	Top	0.000°	NO	20.6094	234.8155
C3	CAP_0805-CDN-CAP-0105,33PF,25VA	CAPC2012N	Top	0.000°	NO	20.6094	201.5515
C4	CAP_0603-CDN-CAP-0016,10PF,25VA	201C	Top	0.000°	NO	33.2872	153.9621
C5	CAP_0805-CDN-CAP-0105,33PF,25VA	CAPC2012N	Top	0.000°	NO	33.6155	201.5515

In this image, component C3 is selected in the Search results, displayed on the board and also shown in the schematic design.

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11

Creating Block Diagrams

A block or system diagram is used for architectural and documentation purposes. You can capture the top-level schematic design depicted by blocks and their connections. This diagram represents how the design is organized.

Creating a system diagram to depict a design or drawing a process flow diagram in System Capture is a simple activity. All you need to do is draw block shapes on the canvas, use block arrows to show connection between blocks, and the system design is ready.

The following topics are covered in this module:

- Adding Auto Shapes
- Naming a Block
- Connecting Blocks using Arrows
- Block Diagram Elements
- Grouping Block Elements

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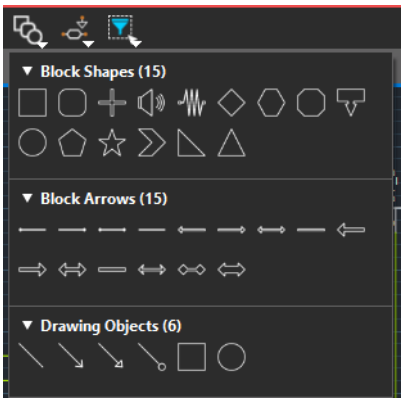
Adding Auto Shapes

A typical block diagram consists of different shapes and connecting lines, and helps you graphically represent the system and the relationships in the process. The *Auto Shapes* bucket on the left pane of the System Capture application window provides all the blocks and arrows you can use to create a system design.

To display the Auto Shapes available, click the Auto Shapes icon



To create a system diagram, place blocks on the canvas and draw connections between them using arrows and other drawing objects.

To place a block:

1. Choose a rectangle

   As soon as you click a shape, it is attached to the cursor. Objects are added on the canvas in the continuous add mode. You can draw as many instances as you want on the canvas.

2. Draw a rectangle on the canvas and then draw more shapes as needed.

   For example:

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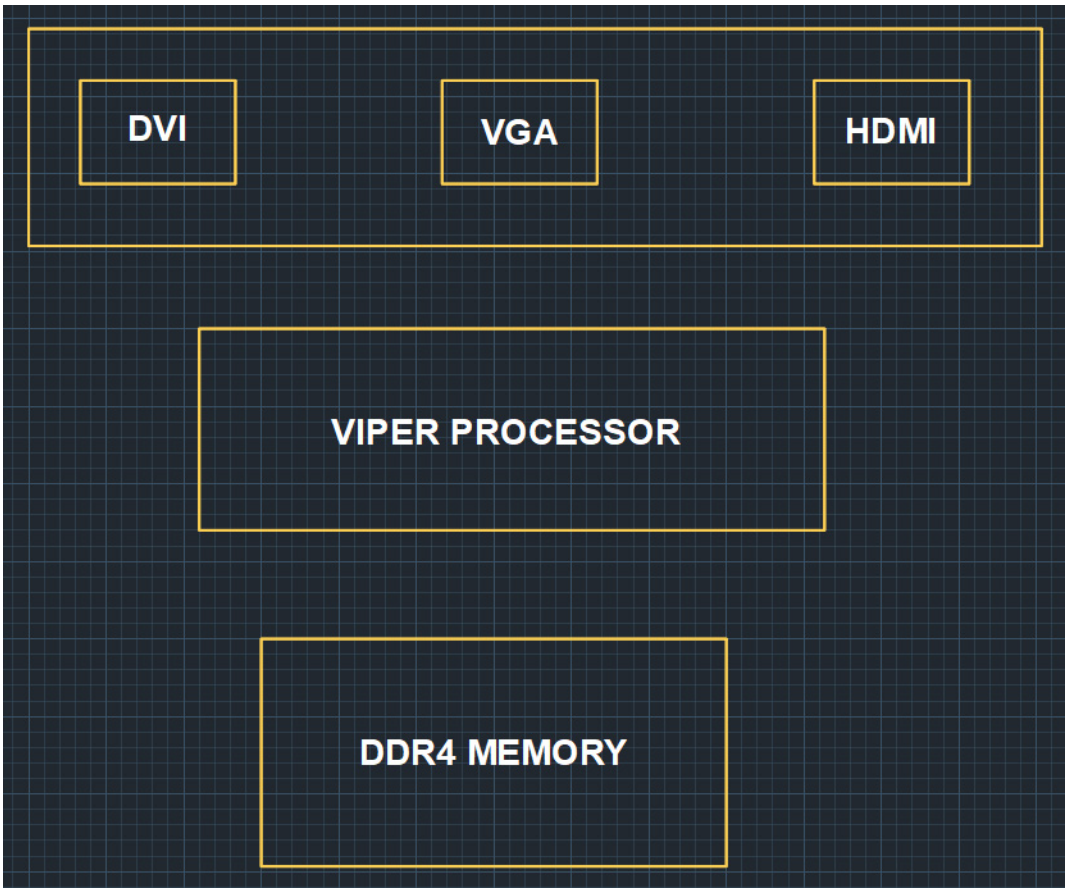

3. Press the `Esc` key or choose *Done* from the right-click pop-up menu to end the operation.

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Naming a Block

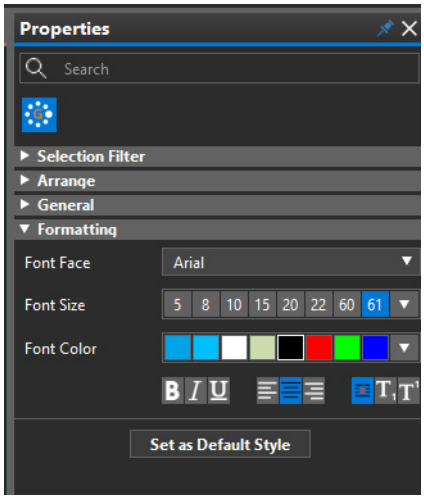
You can name the blocks you added to the canvas.

To name a block:

1. Double-click the first square block and type a name.

   You may want to change the size of the text to improve readability:

2. Click the Format icon
3. Select the text and change the Font size and style to *25* and *Bold*, respectively.



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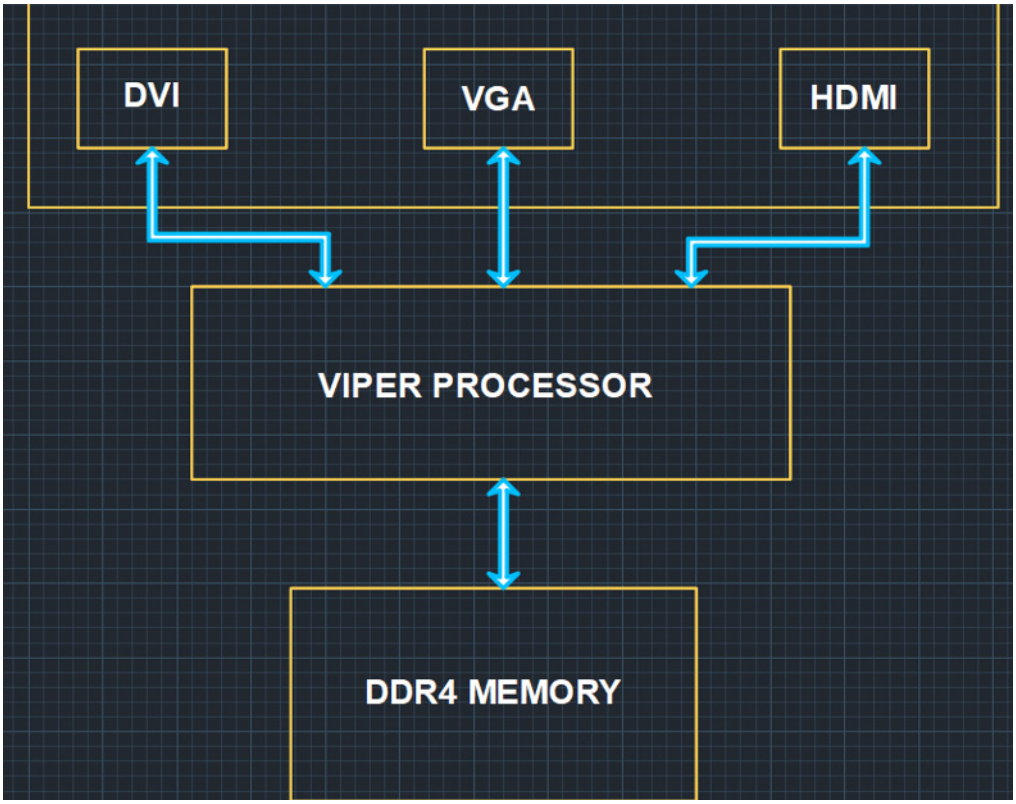
Connecting Blocks using Arrows

Use arrows to connect various blocks.

To connect blocks using arrows:

1. Choose the *Arrow Pointed* arrow from the Block Arrows bucket.
2. Click the starting point.
3. Click at every point where you want to create a junction and finally click the edge of the block to be connected.
4. Draw more connections as required.

   For example:



5. Double-click after you are done drawing each arrow.
6. Press the Esc key to complete the operation.

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Block Diagram Elements

In addition to blocks and arrows, you can add drawing objects from the Drawing Object bucket, and notes and images to the design.

Adding Images

To add an Image:

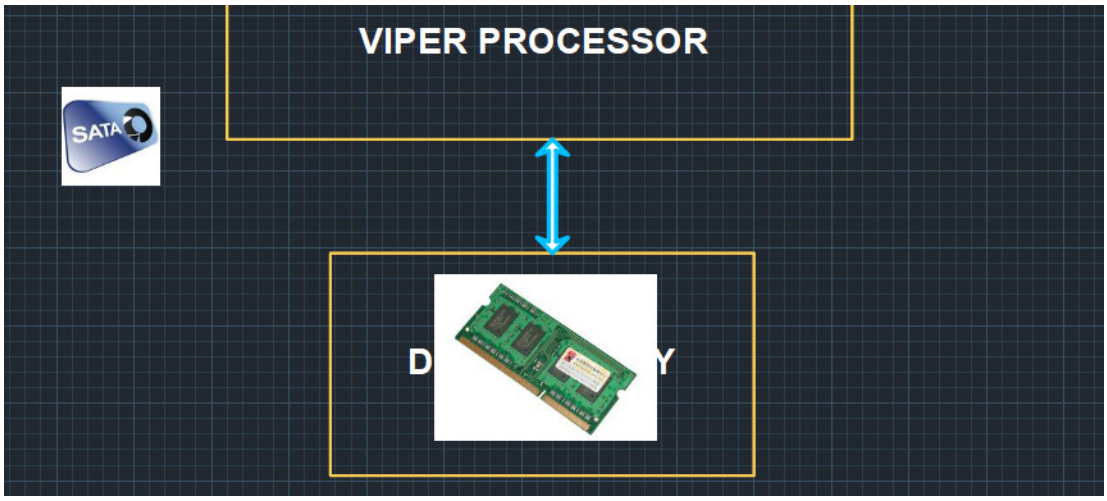
1. Choose the *Place – Picture* menu.
2. Choose an image and click *Open*.

Caution

In case you are working with the SVG format, note that System Capture has a technical limitation and only supports images compliant with the standards specified at https://www.w3.org/TR/SVGTiny12/. Non-compliant SVGs might not render correctly.

3. Place the image.
4. Repeat as required.

   For example:



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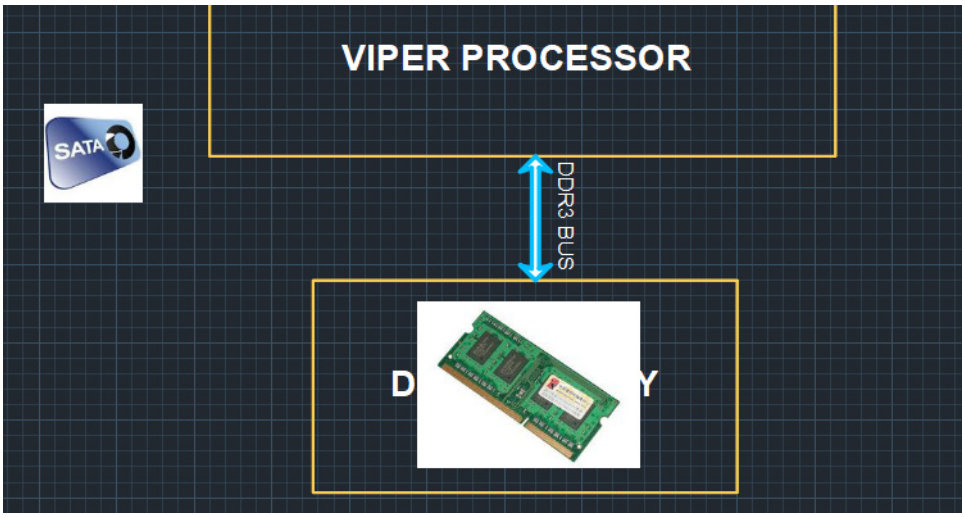
Adding Notes

To add a note:

1. Click the *Add Note* icon.
2. Click anywhere on the canvas to place the note.
3. Type *the text* and click outside the note.
4. Rotate the note to align it as required



The note object can take inputs in any international language. You can try to add the note in international language by selecting the font to an international language or by switching keyboard to an international language.

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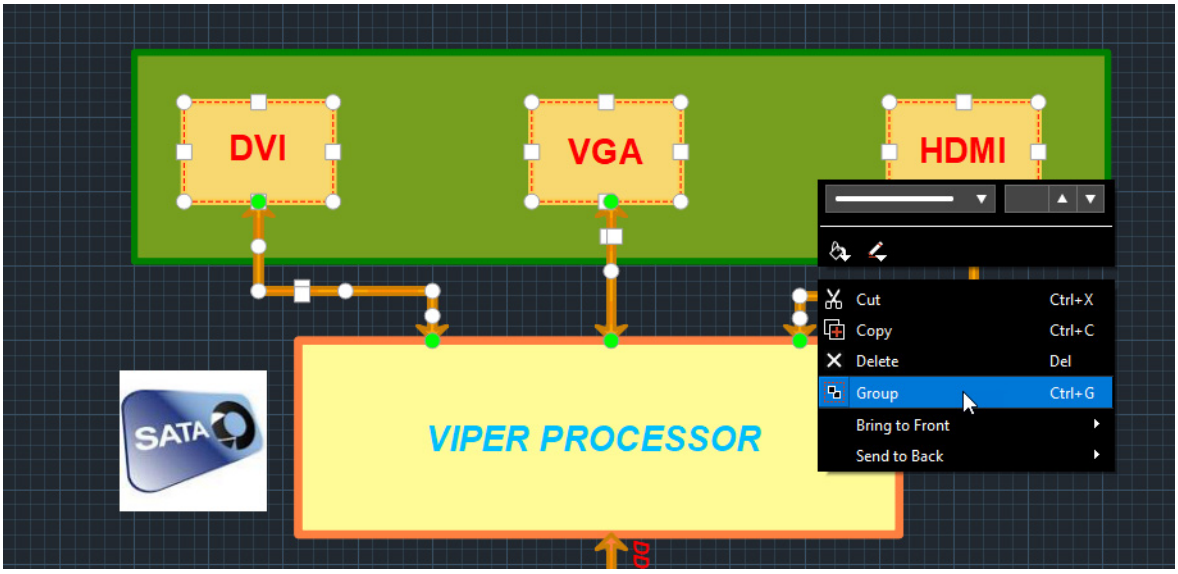
Grouping Block Elements

You can create groups of elements for easy manipulation on the canvas.

To group block elements:

1. Select two or more blocks.
2. Right-click and choose *Group* from the pop-up menu.



The selected elements are grouped together.

Related Topics

https://www.w3.org/TR/SVGTiny12/

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A

Glossary

attribute

Information that System Capture lets you attach to objects (components, wires/nets, and pins) in a schematic. Attribute information is passed to other design programs for processing. An attribute consists of a name-value pair. Attributes are also called properties.

backannotate

The process of updating a System Capture schematic with information on new parts, connectivity, and properties from the layout file tools. Usually, you backannotate the design after the design has been processed by a physical design system.

block

A hierarchical representation of a logical collection that can be reused in a schematic.

body

The symbolic representation of a component or design block. This is also called symbol.

BODY drawing (symbol)

The symbolic representation of a library component that you add to your design. This drawing defines the shape, pins, and general properties of the library component.

bus tap

Tapping a subset of signals from a bus.

C-tap body

The default bus tap provided in the System Capture standard library.

category

Refers to a group of components arranged hierarchically.

cds.lib

A file containing a list of libraries available to a site or a project.

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cell

Software representation of a component. Consider a cell to be a collection of views that describe an individual building block of a chip or a system.

chips.prt

A file containing physical information about a component.

component

Refers to the logical characteristics of a library part.

component instance

The placement of a component one or more times on a schematic.

configuration

A collection of views that control how a design is compiled and simulated.

constant signal

A signal that has a numeric name. For example, a signal named `123`.

See also, non-constant signal

constraint

A restriction on the physical implementation of a design object.

cross-probe

The process of identifying corresponding parts, packages, and signals in the System Capture schematic and PCB Editor.

design

A schematic drawing created in System Capture.

DRC

Design Rule Check

entity

The view of a cell that contains the definition, including port (pin) definitions, for the current drawing (cell). Several checks are made to ensure that entity declarations, symbols, and schematics are in agreement.

expand

To build a complete design including all levels of the hierarchy based on views specified in the current expansion configuration.

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flat design

A design in which all parts of the drawing come from System Capture or user-defined libraries and are one-to-one logical representations of the physical parts. All of the interconnecting wiring within the design is entered pin-to-pin. Best suited for small designs that do not have sophisticated bus requirements or reuse portions of circuitry.

grid

Defines where wires and pins meet in the schematic. System Capture supports two grid types. hard property

Properties that you add to the schematic to specify packaging assignments. Hard properties are included in the connectivity files and thus also in the Verilog/VHDL netlist. They differ from soft properties, which are essentially documentation properties on the schematic and are not included in the netlist.

hierarchical design

A design that is organized into blocks to reuse many of the same circuit functions and isolate portions of the design for teamwork assignments. Using a block design lets you refer to a collection of logic without having to include the logic in the drawing. Hierarchical blocks simplify a drawing. This is also called block design.

injected property

A property that appears to the right of a PPT format definition or part row. Packager-XL passes these properties to Allegro in the physical netlist, - for example, company-specific part numbers, costs, or package types.

interface signal

A signal property (\I) assigned to pins in block diagrams to indicate an interface signal from a higher level drawing. In a flat design, this is a signal in the schematic that corresponds to a pin in the symbol drawing.

key property

A property that appears to the left of a PPT format definition or part row. Packager-XL uses these properties to uniquely identify the physical part to use from the various table entries. For example, a resistor part table may use VALUE or TOLERANCE to select a specific physical part.

library

A collection of components from which you can select a component to place in a schematic.

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library properties

Librarian-generated properties on symbols, chips, and in the Physical Part Table (PPT). Only the librarian can modify library properties.

marker

An error, warning, or information item that indicates a rule violation in your schematic.

net

A set of pins that are electrically connected.

netlist

An ASCII text file that describes the electrical connectivity (wires/nets and components) of a drawing.

non-constant signal

A signal that has an alphabetical or alphanumeric name. For example, `ADDRESS`, `DATA1`, `1CLOCK` and so on.

See also constant signal

orthogonal

Bent to route around objects in a schematic. This is an alternative to direct (diagonal) placement.

package

(noun) In VHDL, a collection of types, constants, subprograms, and so on, usually intended to implement some particular service or to isolate a group of related items.

(verb) The process of translating a logical netlist into a physical netlist. Design Synchronization takes a logical representation of a schematic and applies the physical attributes necessary to allow physical layout.

page

Refers to a page in a design. If the amount of logic required to define a design does not fit on a single page, the drawing might extend to more than one page.

part

Refers to the physical symbol derived from the logical representation of a component or design block.

PDF/A

Refers to the ISO-Standardized version of the Portable Document Format (PDF) specialized for use in the archiving and long-term preservation of electronic documents.

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physical

Refers to the physical properties associated with a library component.

Physical Part Table (PPT)

Used to map logical parts in the schematic to physical parts for a layout.

pin

Conductors that protrude from packages. Pins allow the component to be connected logically to wires and other components in the logical design.

placeholder property

A temporary property assigned to the symbol drawing of a part. These properties serve as substitutes for part properties that will be assigned later in the schematic design. Placeholder properties let you predefine the location and text size of part properties through the part symbol drawing.

placeholder value

Substitutes a real property value. It is indicated with a **?** value.

primitive

The symbol name in the chips.prt file.

project

The work area for a design, including all the views of the design, links to libraries, and setup information such as Physical Part Table, configuration, and expansion directives. Separate directories exist for each design project.

property

A logical characteristic of a design object. It is information that System Capture lets you attach to objects (components, nets, and pins) in a schematic. Property information is passed to other design programs for processing. A property consists of a name-value pair. Properties are also called attributes.

ratsnest line

In a design drawing, a line that shows a logical connection between two pins, connect lines, or vias. Elements connected by the same ratsnest line are part of the same net. The ratsnest shows the circuit logic and, for ECL circuits, the order in which pins are to be connected.

reference designator

The designator, or identification code, for a component.

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reference library

A library containing cells that describe common components potentially used in many designs.

root drawing

The top-level drawing in your design. This is the drawing that System Capture opens by default when you start an editing session.

scalar signal

A signal having a single bit.

schematic

The standard type of drawing created with System Capture to represent the logic of components or design blocks that make up a circuit. The symbolic drawing is generated in a physical layout tool. A schematic can contain library components and design blocks that represent other schematics.

schematic properties

Modifiable properties that are defined when editing the schematic.

scope

You can assign one of three different scopes to a signal:

INTERFACE	Used on signals you want to access from a higher level of a hierarchy. Represented by \I.
GLOBAL	Used on signals that you need to access on all levels of hierarchy. Represented by \G.
LOCAL	Indicates that the signal is recognized only at its own level. No special characters are required because the local scope is the default.

section

Refers to a physical section on a logical component. Pin numbers are different in different sections of the component. You can section a component either before or after you package the design.

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signal

Wire connections between components that support communication of dynamic data between components. Signals having the same name are interpreted as one signal; this is how signals are connected across multiple pages of a drawing.

signal bits

Signals can have a single bit (scalar signals) or multiple bits (vectored signals). The bit portion of the signal name is called the bit subscript and gives the bit information. Bit subscripts are enclosed in angle brackets, for example, <3..0>.

soft property

Properties that can change from one backannotation to the next. Soft properties are documentation properties on the schematic and are not included in the netlist. They differ from hard properties, which are included in the connectivity files and thus also in the Verilog/VHDL netlist.

structured design

Uses bus signals and memory and register depth. A structured design minimizes the number of interconnections and parts on the schematic.

swap

To exchange the locations of two logically identical pins within a function. This minimizes the average ratsnest crossings in a layout.

symbol

The symbolic representation of a library component that you add to your design. This drawing defines the shape, pins, and general properties of the library component.

symbol properties

Librarian-generated properties defined on a component through its symbol description and not by editing the schematic.

system properties

Non-modifiable schematic properties that System Capture adds.

tap body

Cadence-supplied taps found in the standard library: C-tap, tap.body, bustap.body, msbtap.body, and lsbtap.body.

text

Includes text can be signal names, properties, and notes.

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user-defined net

A net with a signal name on it. This is in contrast with an unnamed net, for which the user did not specify a net name and System Capture specifies the net name.

vectored signal

A signal having multiple bits.

version

Different graphical but functionally equivalent representations of a component, all of which refer to the same logic drawing. If the version is not specified, System Capture assumes the version to be1.

VHDL

VHSIC Hardware Description Language.

view

Designs are represented by these views in System Capture: schematic (or logic), symbol (or body), VHDL, and Verilog.

visibility

Refers to the amount of property or pin information displayed on a schematic.

wire

An electrical connection. A single wire can be an entire net, or, where there are many connections, a wire can be a segment of a net. This is also called signal.

wire orientation

Bent to route around objects in a schematic versus direct (diagonal).

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B

Preferences Window

How to open the Preferences window?

Choose *Edit – Preferences* to open this window.

Many default values for Allegro X System Capture controls are defined in this window. Some of them have corresponding directives that can be set before starting a session or in the `site.cpm`, if required.

The *Preferences* window contains the following sections:

- System
- Libraries
- Schematic
- Symbol Editor

System

The *System* preferences section is divided into four categories:

- General
- Custom Variables
- Project Explorer
- Shortcuts

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General

The following table lists the *General* preferences and their descriptions:

Section	Field	Description
Auto Recovery		Controls if the designs open in System Capture are auto-saved and are available on the subsequent launch, in case the session closes unexpectedly.
	Generate auto-recovery data	Enables saving the recovery data for designs and session.
	Interval (in minutes)	Sets the frequency of backing up the data, if the auto-recovery option is enabled.
Canvas		Includes the controls to fine-tune the display of the schematic canvas.
	Auto Pan	Adjusts the display to keep a part of the canvas in focus.
	Show Guidelines	Displays an alignment guide (dotted line) to show alignment with the nearest object of the same type when placing blocks and instances on the schematic.
	Show Grid Location	Shows the grid location of the cursor in the status bar.
Style	*Application Theme*	Sets the color theme, *Dark* or *Light*, for the current session of System Capture for all the menus and windows except the canvas background and canvas, which are controlled by the next two options.
	Schematic Sheet Theme	Sets the color scheme of the canvas.
	Canvas Background Color	Sets the color for the blank area that surrounds the canvas.
	Grid Lines	Sets the color of the grid lines on the canvas.

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Section	Field	Description
Other	*Recent Project List Count*	Sets the number of recently opened projects as displayed in the *File – Open Recent* menu command.
	Open Projects in Read Only	Enables opening of the project in the read-only mode.

Custom Variables

You can define custom variables to be placed on a schematic, in the *Custom Variables* tab. These variables make the plots of cross-referenced schematics illustrative and easy to use. For example, `CDN_DESIGN_NAME` = *`ref_5g`* indicates that the name of the design in this project is *ref_5g*.

The following table lists the fields in the *Custom Variables* tab:

Field	Description
Name	Displays the name of the custom variable.
Value	Displays the value of the custom variable.
<Add Custom Var>	Add new variables here.

Project Explorer

You can choose the entries to be displayed in *Project Explorer*.

The following table lists the entries in *Project Explorer* and their descriptions:

Field	Description
Blocks	Blocks added to the design.
Schematic Sheet	Names of the Sheets in the design.
Schematic Sheet number	Page numbers of the schematic sheets.
Variants	Variants of the design.
Live BOM	Live Bill of Materials of the project.

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Field	Description
Bill Of Material	Bill of Materials containing details, such as Part Name, Ref Des, Quantity, and so on.
Physical Netlist	Contains the physical netlist files.
Layout	Contains the exported board files.
External Allegro Boards	Contains the imported Allegro boards.
Library	Libraries available in the current project.
Electrical Stress And Analysis	Electrical stress log and results obtained after analyzing electrical stress.
Schematic Audit	Schematic audit results obtained after auditing the schematic.
Single-click to open an item	Controls the click action to select an entry in the explorer. By default, a double-click opens the selected entry.
Show Hidden Pages	Displays the hidden pages in the *Project Explorer* with a strikethrough.

Shortcuts

Many keyboard shortcuts are assigned to commands by default. You can also specify custom keyboard shortcuts for various commands.

The following table lists the fields in the *Shortcut* tab, which displays various commands and their keyboard shortcuts:

Field	Description
Command	Displays the operation that the shortcut will perform.
Keyboard Shortcut	Displays the keys to be pressed to trigger the command.

Libraries

The contents of the *Libraries* tab depend on the library selected during project creation. There are three libraries: *Allegro DE-HDL*, *Allegro Unified*, and *OrCAD Capture*. Let us take the example of a *DE-HDL* Library project.

For a *DE-HDL* library project, the project libraries and part table files (PTFs) are displayed.

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- Available Libraries
- Physical Part Table

Available Libraries

Shows the libraries available to the project and the ones already added. You can add any of the available libraries to the project and remove libraries from the project.

The following table lists the *Available Libraries* preferences and their descriptions:

Field	Description
Available Libraries	Displays the available libraries which can be added to the project. To add a library, click the + icon.
Project Libraries	Lists all the libraries added to the site. More libraries can be added using the *Available Libraries* field.

Physical Part Table

The following table lists the *Physical Part Table* preferences and their descriptions:

Field	Description
File/Folder Path	Select the folder where the part table files reside.
Type	States if a single physical part table file or a folder containing multiple files is selected.
Use Cell Level Physical Part Table Files	Reads cell-level part table files (PTFs), and not the ones specified at the global-level, that is, in the `ppt` directive of the `START_GLOBAL` section.
Merge Physical Part Table Files	Merges cell-level PTFs and global-level PTFs, if they exist at both the levels.
Perform Case Sensitive Row Match	Unified Search does not display parts where attribute values are in different cases in cell and part table file.

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Schematic

This section controls the behavior of user actions and System Capture responses. The controls are grouped as follows:

- General
- ECO/Packager
- Grids
- Page Setup
- Component
- Special Symbols
- Variant View
- Wiring/Ports
- Table of Contents

General

The following table lists the *General* preferences and their descriptions:

Field	Description
Repetitive Paste	Attaches the selected part or component to the cursor for multiple paste operations until the user presses `Esc`. Enabled by default.
Show power signal names for new wire connections	Controls if the signal names on wires are added or displayed automatically when the wires are connected to power sources in various scenarios. Enabled by default

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Field	Description
Ignore hidden scalar power and global signal names when pasting	When wires are copied and pasted without the attached power source, this option controls if the power signal names get transfered along or not. Enabled by default
Ignore hidden 'unnamed_' scalar signal names when pasting	Controls the transfer of the hidden 'unnamed_*' signal names when a selection is pasted. Enabled by default
Ignore all hidden named scalar signal names when pasting	Controls the transfer of all the hidden signal names when a selection is pasted. Unselected by default
Select next available symbol of split part during placement	Attaches the next available symbol to the cursor when a split part is selected for placement.
Display values for newly added attributes	Displays the newly-added attributes.
Allow editing of table created using CSV file	Enables editing of tables added from CSV files. Such tables cannot be edited by default.
Show Page Navigation Toolbar	Shows a toolbar at the bottom-center of the canvas to help switch or add pages.
Show Cross on Pack Ignore	Shows a Do Not Install (DNI) cross on components that have the `PACK_IGNORE='True'` property set.
Area selection mode	Helps you fine-tune how the parts get selected when the components and circuitry is selected on the canvas. The options are: ■ Fully-enclosed objects ■ Overlapping Objects (default)

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Field	Description
Output folder	Displays the folder where all the generated files are stored. This is set to `./output` by default.

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ECO/Packager

The following table lists the *ECO/Packager* preferences and their descriptions:

Section	Field	Description
RefDes Pattern		The reference designator (RefDes) assigned to the components in a design are controlled by the values set in this section.
	RefDes Numbering Characters	Displays the character format for the RefDes applied to components. The options are: ■ *Numeric (default)* ■ *Alpha-numeric* ■ *Unit-numeric* **Note:** Unit-numeric implies that the unit character is assigned from the 0-9 range, while all other places are assigned from the A-Z, or 0-9 range.
	Starting Digit	Controls if RefDes starts with 0 or 1 (default).
	Fixed RefDes Length	Controls the length of RefDes. The fixed length can be set to *Off* or a value of *3* through *8*. If unselected, any length is accepted.
	Include Page Number	Controls if the page number is included in RefDes. Enabled by default.
	Fixed Page Number Length	Controls the length of the page number. Options are: ■ No fixed length ■ Two digits (default) ■ Three digits

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Defaults		*This section lists the additional controls for RefDes and describes how they are managed.*
	Restart Numbering on Each Page	Enables the reference designator numbering to be restarted for every page.
	Reuse Reference Designator's Numbers	Enables reassignment of previously-assigned reference designators, if not assigned to any other instance.
	Auto-resolve RefDes Conflicts	Enables System Capture to correct any RefDes conflict. For example, if two components are named `R1`, the second one is changed to an unassigned value.
	Check parts sync status when generating layout netlist	Checks if there are any parts for which a unique part definition is not found. If yes, the layout netlist is not generated.
	Default Reference Designator Prefix	Displays the starting letter of RefDes. Set to `U` by default.
	Reference Designator Max Length	Displays the maximum length of any assigned RefDes. Set to `31` by default.
	Physical Part Name Max Length	Displays the maximum length of any part name. Set to `31` by default.
	Physical Net Name Max Length	Displays the maximum length of any net name. Set to `31` by default.

Grids

Similar to page borders, grids are an important part of the schematic canvas. System Capture ensures that all the objects on the canvas are always placed on the grid to avoid any off-grid components in the design. The display settings for the grid on the schematic design canvas are listed in the *Grids* tab. By default, the unit for these settings is inches. You can change this to millimeters by modifying the `GRID_UNIT_MEASURE` directive of the `site.cpm` file.

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The following table lists the *Grids* preferences and their descriptions:

Field	Description
Grid Style	Choose the display option for the grids. You can view the grid as *Lines* or *Dots*.
Pin-to-Pin Spacing	Displays the space between two adjacent pins of a component. By default, the grid unit is *inches*.
Electrical Grid	Controls the electrical grid on which electrical objects, such as components and wires are placed and aligned. All the placed electrical components snap to this grid. If you change the *Electrical Grid* value, System Capture checks for off grid components based on the new value. If off grid components are present, System Capture flags a message that the value cannot be changed due to the presence of off-grid components. Else, the value is successfully changed. The eye icon controls if the electrical grid is visible.
Display Electrical Grid	Select the value to multiply with the *Electrical Grid* value to display the electrical grid accordingly.
Documentation Grid	Controls the documentation grid. Documentation objects, such as text, notes, drawing objects, and images do not contribute to the electrical connectivity of the design, but help in better documentation of the design. Documentation objects require a finer control for placement of objects, consequently, the *Documentation Grid* is set to a finer value than the *Electrical Grid* value. If required, you can set the *Documentation Grid* value to the same value as the *Electrical Grid*. Display of the documentation grid is optional. Use the eye icon to show or hide the documentation grid.

Page Setup

The page border can be changed for the current page or set as the default for all the new pages in the project. This feature is useful when you need the first sheet of your schematic to have a border containing documentation of the project, which is different from the border on the rest of the sheets of the design.

Page Setup consists of two tabs: *Standard* and *Template*.

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In the *Standard* tab, select the *Sheet Size* and the *Zone* attributes, as explained in the following table:

Field	Description
Sheet Size	Select the required sheet size from the list.
Zones	Divides the canvas into vertical and horizontal zones. Optionally, you can modify the number of vertical and horizontal zones.
Labeling	Select any one option for labeling the vertical and horizontal zones. You can choose letters or numbers for labeling the zones from top to bottom or left to right.

In the *Template* tab, select the *Library*, *Cell*, and *View* from which the page border information is fetched.

Component

Component preferences let you modify settings related to Part Manager, replacing components, changing the symbol version, and component identification.

The following table lists the *Component* preferences and their descriptions:

Field	Description
Part Manager	This section is used to control the Part Manager settings.
Run Part Manager on project load	Run the Part Manager when a design is opened in System Capture.
Auto update parts	Updates Part Manager on project load to synchronize the attribute value in library and design, if this option is enabled.
Allow import or paste even if component cells do not match	When enabled, a symbol mismatch in the current design and the design from where the symbol is copied does not stop paste or import process.
Allow page border updates for read-only pages	Applies any change in page border in any cell, to only read-only pages.

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Field	Description
Replace Components	Controls the settings for replacing components.
Retain connectivity by matching	Retains connectivity by *Pin Locations* or *Pin Names,* when replacing components.
Retain component and pin styling	Retains component and pin location of the previous component, when replacing components.
Retain property annotation	Retains the library property annotations when replacing or updating a part from Part Manager without refreshing the symbol properties from library.
Retain signal names and voltage values for power symbols	Retains the signal names and voltage values for power symbols when they are added to the schematic.
Symbol Version Change	Controls changes in symbol version attributes.
Retain annotations when replacing versions of same symbol	Retains attribute annotations on a symbol, even when the symbol version is changed.
Components Identification	Controls the letters of the alphabet with which various component names start.
Passive Components	By default, the passive components, such as resistors, inductors, and capacitors, begin with the letters, `R, L, C`, respectively.
Connectors	By default, connector names start with the letter `J`.

Special Symbols

Used to control special symbols. Select the *Library*, *Cell*, and *View* for a given category. By default, the symbol is added to the panel, and is available for placement.

The following table lists the *Special Symbol* preferences and their descriptions:

Field	Description
Ports	Defines the location from which port symbols are fetched.

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Field	Description
In	Controls the library, cell, and view for inport.
Out	Controls the library, cell, and view for outport.
In/Out	Controls the library, cell, and view for in/out port.
Off Page Connectors	Defines the library, cell, and view for various ports of off page connectors.
In	Controls the library, cell, and view for inport of off page connector.
Out	Controls the library, cell, and view for outport of off page connector.
In/Out	Controls the library, cell, and view for in/out port of off page connector.
Taps	Defines the location of the special symbols used for tapping.
Default Tap	Controls the library, cell, and view for tapping symbol, when tapping by default.
90 Degrees Tap	Controls the library, cell, and view for tapping symbol, when tapping at *90 degrees*.
180 Degrees Tap	Controls the library, cell, and view for tapping symbol, when tapping at *180 degrees*.
270 Degrees Tap	Controls the library, cell, and view for tapping symbol, when tapping at *270 degrees*.

Variant View

Used to set attributes related to the variant view to help you recognize the modified parts in a variant.

The following table lists the *Variant View* preferences and their descriptions:

Field	Description
Property Name corresponding to Part Number	Displays the attribute from which the part number is fetched.
Modified Parts	Sets the variant part properties to identify what was changed.
Line Width	Sets the width of the line to use when working with variants.

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Field	Description
Line Style	Sets the line style to use when working with variants.
Line Color	Sets the line color to use when working with variants.
Fill Color	Sets the color for filling the symbol modified in a variant.
Transparency	Sets the transparency level in percentage of the filling color for the modified component in a variant.
Modified Part Properties	This section lists the properties of the modified part in a variant.
Font Face	Controls the font for the modified part of a variant.
Font Size	Controls the font size for the modified part of a variant.
Font Color	Sets the font color for the modified part of a variant.
Text Font	Controls the formatting, such as, Bold, Italics, or Underline for the variant text.
DNI Components	This section lists the attributes of the DNI Components in a variant.
Show cross on DNI	Controls whether a cross is shown on the DNI component.
DNI Cross Color	Sets the color of the DNI cross for a variant.
DNI Line Width	Sets the line width of the DNI cross for a variant.

Wiring/Ports

Used to control the settings related to stub length, display name for net names, highlighting Xnets, and more for the *Wiring/Ports* controls. The following table lists the *Wiring/Ports* preferences and their descriptions:

Field	Description
General	Controls the general settings for Wiring/Ports, such as stub length, display name, and so on.
Stub Length	Sets the default length of the stub added to the components.

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Field	Description
Display Name for System Generated Net Names	Enables you to display the system-assigned net names. When a new net is drawn, the system assigns a net name for it. By default, this name is not displayed.
Highlight XNet for Net	Enables you to highlight Xnets with discretes, such as R,L, and C when the net is highlighted.
Display hotspots for unconnected nets	Displays an indicator or hotspot on the nets which are not connected.
Convert lower case signal names to uppercase	Automatically converts lowercase signal names to uppercase.
Use PhyDesPrefix as Net-Split Suffix Character	Attaches the prefix of PhyDes as a suffix for net name when a discrete component is placed on a wire. When unselected, the value of Net-Split Suffix is used by default.
Use existing nets as NetGroup members	Selected by default, which is the recommended setting. When new NetGroups are added to a design by importing sheets, copying, or by making changes in the *Edit Connectivity* dialog box, you can control if System Capture uses existing nets as NetGroup members.
Rename conflicting NetGroup member names	Selected by default. When new NetGroups are added to a design by importing sheets, copying, or by making changes in the *Edit Connectivity* dialog box, you can control if System Capture uses existing nets as NetGroup members. When this option is unselected, some copy or paste commands might not perform the desired operations.
Net-Split Suffix	The suffix to be used when a discrete component, such as a Resistor, Inductor, or Capacitor is placed on a wire.
Junction Dot Size	Sets the dot size of the junction between components and wires.
Default Port Locations	Controls the placement of ports, such as *In*, *Out*, and *In/Out*.
In	The default location of the inport, for hierarchical designs, and when creating symbols.

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Field	Description
Out	The default location of the outport, for hierarchical designs, and when creating symbols.
In/Out	The default location of the ioport, for hierarchical designs, and when creating symbols.

Table of Contents

Used to set the attributes of *Table of Contents*. The following table lists the *Table of Content* preferences and their descriptions:

Field	Description
Row Count	Controls the number of rows required in the TOC.
Column Count	Controls the number of columns required in the TOC.
Value Type	Sets the value type which needs to be populated in this column.
Header Label	Controls the header label or column name here.

Symbol Editor

Choose *Open Schematic Model* in the shortcut menu of any component on the schematic to view the *Symbol Editor* tab in the *Preferences* window. *Symbol Editor* preferences can be grouped as follows:

- General
- Grids
- Pins
- Style

General

The following table lists the *General* preferences of the *Symbol Editor* and their descriptions:

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Field	Description
Classification Explorer	Displays the list of parts in a library based on the assigned categories.
Show packageable symbols only	Displays the minimum symbols required to package a schematic in the library explorer. Symbol replicas are not shown when enabled.
Use space as column separator when pasting	Divides the data with spaces in separate columns, when copying it from a text file to the symbol table.

Grids

This controls the settings related to the grid style, pin-to-pin spacing, electrical grid and so on, for editing a symbol. The following table lists the *Grid* preferences of the *Symbol Editor* and their descriptions:

Field	Description
Grid Style	Controls the display option for the grids displayed when editing a symbol. You can view the grid as *Lines* or *Dots*.
Pin-to-Pin spacing	Displays the space between two adjacent pins of a component when editing a symbol. By default, the grid unit is *Inches*. After defining the Pin-to-Pin Spacing attribute, you can define the grids as its factor.
Electrical Grid	Controls the electrical grid on which electrical objects, such as components and wires get placed and aligned. All the placed electrical components snap to this grid. If a user changes the *Electrical Grid* value for *Symbol Editor*, System Capture checks off-grid components as per the new value and changes the value if there are none. In case off-grid components exist, System Capture informs the user that the value cannot be changed.
Display Electrical Grid	Sets the value to be multiplied with the *Electrical Grid* value and displays the electrical grid when editing a symbol, accordingly.

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Field	Description
Documentation Grid	Controls the documentation grid when editing a symbol. Documentation objects, such as text, notes, drawing objects, and images do not contribute to the electrical connectivity of the design, but help in better documentation of the design. The documentation objects require a finer control for placement of objects, consequently, the *Documentation Grid* is set to a finer value than the *Electrical Grid*. If required, you can set the *Documentation Grid* to the same value as the *Electrical Grid*. The display of documentation grid is optional.

Pins

This section controls the default pin settings, such as placement location of different pin types on the symbol outline, pin shape, size, pitch, and assertion shape for pins when editing a symbol. The following table lists the *Pins* preferences of the *Symbol Editor* and their descriptions:

Field	Description
Side and Shape	Controls the side the pin will be displayed on, and the shape of the pin for all the listed symbols.
Attributes	Controls the attributes of the pin.
Pin Size	Controls the length of the pin.
Pin Pinch	Controls the distance required between two pins.
Assertion Shape	Controls the shape of the pin.

Style

Set the symbol graphics, pin attributes, and text attributes for editing a symbol in this section. The following table lists the *Style* preferences of the *Symbol Editor* and their descriptions:

Field	Description
Graphics	Controls the outline and the attributes of the drawing objects when editing a symbol.

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Field	Description
Outline	Controls the width, style, and color of the outline around the symbol.
Drawing Object	Controls the line width, style, and color of the drawing object.
Pin	Controls the various pin attributes.
Pin Shape	Controls the shape attributes of the pin, such as the width, style, and color.
Pin Text	Controls the text font, size, and color of the pin text.
Pin Property	Controls the text font, size, and color of the pin property.
Pin Number	Controls the text font, size, and color of the pin number.
Text	Controls the text attributes for notes and properties.
Note	Controls the font, size, and color of the added notes.
Prop	Controls the font, size, and color of the properties.

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Bill of Materials

The first dialog box that is displayed when you run the BOM tool is *Bill of Materials*. This dialog box is divided in three main sections:

1. *Output Options*
2. *Report Format Options*
3. *Variant BOM Options*

The following table describes these sections:

Fields	Description
Template File	Enter the path to the template file in this field. Alternatively, you can use the browse (...) button to browse to the file. You can enter the full path or the relative path. If you specify the full path, Bill of Materials searches for the template file in that path. If you specify the relative path, Bill of Materials (BOM) searches for the template file relative to the bom view of the current project. Therefore, if your template file is present in the BOM view, specify only the file name; otherwise, specify the complete path to the template file. If the template file is not found in the specified path, an error message is displayed. When the *Bill of Materials* dialog box is displayed for the first time, the Template File field is filled with the template file path in the following order: (1) the last saved template file in the project file; (2) the bom view of the current project; and (3) the locations as specified in the setup.loc file.

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Customize	Launches the Customize Template dialog box. The information specified in the template file is used to fill the initial entries in the different tabs. After customizing the values, you can save the template file (with the same name or with a new name) and use it for future runs.
Output File	Enter the path of the output file that contains the BOM report in this field. By default, the value of the Output File field is picked from the project (.cpm) file. If the project file does not have information specified about the output file, the Output File field displays the BOM.rpt file in the bom view of the design as the default output filename. Depending on the report format type you choose and whether you are generating the BOM report for the base schematic or a variant, the name of the file in the Output File field automatically changes. For example, if you are generating a variant BOM report for INDIA variant in HTML format, the name of the file will be INDIA.html. If you specify an output file but do not specify its path, the Bill of Materials tool saves the output file in the bom view of the project. If you specify the full path of the output file, Bill of Materials saves the output file in your specified path.
View	Choose this button to view the BOM report (as defined in the Output File field) in the default viewer. The viewer will be a text viewer if the output file is in the text or spreadsheet format, or an HTML viewer if the output file is in the HTML format.
Apply Filters	Choose this check box if you want to define conditions on any property. To define a condition, use the Filters button in the Customize Template - Part Specifications tab. The project file stores information about whether you have applied filters in the last run. If you have applied filters, the Apply Filters check box appears selected in subsequent runs.
Text File in Tabular Form	Choose this button to create the output file in the ASCII text format.

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Spreadsheet Format	Choose this button to create the output file in the spreadsheet format, which can be imported in an application such as MS Excel. If you choose the Spreadsheet Format button, you can also select the delimiter in the Delimiter drop down. The default delimiter is comma (,). You can also use semicolon, colon, space, dot, tab, or hash as the delimiter.
HTML	Choose this button to create the output file in the HTML format. The file is stored in a tabular format as defined by the settings in the template file.
Variant BOM	By default, the options in this group box are not active. However, you can turn on the Variant BOM toggle to display the different options for generating the BOM reports. When you turn on the Variant BOM toggle.
Variant File	Check accuracy. Enter the name of the variant database file. You can use the browse button to browse to the file. Alternatively, you can type the path to the file. You can specify absolute path or relative path from the project directory. If you specify relative path, dot (.) is taken as the project directory and not the working directory. To generate a BOM report for a variant, you must have the variant database file (variant.dat), which is generated by using Variant Editor. If you do not specify the report format, the format is picked from the project file. If the report format is not specified in the project file, the BOM report is generated in the text format.
What to Output	Choose the type of the BOM report to be created by clicking on one of the following three options.
Base Schematic BOM	Choose this button to generate the normal BOM report for the base schematic with no variant information. The report generated contains the listing of all the components used in the base schematic. All the property values including the part number correspond to the values chosen in the base schematic.

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Variant BOM	Choose this button to generate the variant BOM report. This report contains the listing of all the components used in a particular variant. All the property values including the part number correspond to the values selected in the particular variant. When you choose the Variant BOM button, the drop down becomes available for selection. You can choose the variant for which you want to create the BOM report. You can also choose the All Variants option. This will generate variant BOM reports for all the variants. For example, if there are three variants: INDIA, USA, and EUROPE and you choose the All Variants option, Bill of Materials will generate the following BOM reports in the bom view of the project: INDIA.rpt, USA.rpt, and EUROPE.rpt. If you want to customize the template file for variant specific options, use Customize - Variant Settings.
Variant Comparison BOM	Choose this button to generate a number-based comparison between the components of the base schematic and all the variants. While generating the comparison BOM report, only the preferred values of the components and alternate groups are considered.
Generate	Choose this button to generate the BOM report.
Close	Choose this button to close the Bill of Materials dialog box.
Help	Choose this button to display Help about the BOM dialog box.

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Customize Template - Report Parameters

The Customize Template dialog box can be opened by clicking the *Customize* button in the *Bill of Materials* dialog box. The default tab displayed is *Report Parameters*. This dialog box is divided into five main sections:

- *Report Header*
- *Row Column Separator*
- *RefDes*
- *Callouts*
- *Miscellaneous*

The following table describes there sections:

Report Header	The Report Header grid box displays the header properties and their values. You can enter new properties or delete the existing properties in this grid box. Notice that a check box precedes each header property. If you clear the check box, the property is not displayed in the BOM report. By default, the Report Header list has five properties.
Title	Specifies a title to appear in the BOM report. The default value of the title is Bill of Materials. You can edit this value. If you want to blank the value of the title then type: TITLE = "".
Date	Specifies the current date as obtained from your system's clock to appear in the BOM report. If you click in the *Value* column of the *Date* property, a drop down displays. From this drop down, you can choose any of the available date formats. If the check box to the left of the *Date* property is checked, the current date is included in the BOM report. A value unchecked omits the date entry in the report.
Design	Specifies the name of the design to appear in the BOM report. You cannot edit this option, as the design name is picked up from the project file.
Template	Specifies the name of the BOM template to appear in the BOM report.

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Callout	Specifies the name of the callout file to appear in the BOM report. The default template file stores the callout file name value as `bom.callout`. Besides these properties, which are selected by default, there are 5 optional properties that you can select and include in the Report Header, which are: ■ Product ■ Version ■ Description ■ Project Path ■ Variant You can drag and drop these properties to move them up and down. To remove any property, click the cross icon on its Header Property. To add a new property, click the *Header Property* column on a new row and select the property from the drop down.
Product	Displays the default name is Bill of Materials.
Version	Displays the product version number.
Description	If you are generating a variant comparison BOM, *Bill of Materials* displays Part Number based Comparison BOM as description. For Base schematic BOM, *Bill of Materials* displays the description as Base schematic BOM. If you have defined a description for variant and are generating a variant BOM report, the description is listed in this row.
Project Path	Displays the path to the project file.
Variant	Displays the name of the variant. The *Variant* property will be visible only when you are generating variant reports.
Column Separator	Enter the character to be used to separate columns in the BOM report. The value of the column separator character in the default template is a space (" ").
Row Separator	Enter the character to be used to separate rows in the BOM report. The value of the row separator character in the default template is a null character ("").

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Header Separator	Enter the character to be used to separate the header row from the part rows. The value of the header separator character in the default template is an equal sign ("=").
	Note: The row and column separators will work only if you are displaying the report in a tabular format such as an ASCII file. If you set a value for the row separator or the column separator, and set the report format as *Spreadsheet Format* or *HTML*, the values for the row separator and the column separator are overwritten by standard values. The Spreadsheet report will be separated by the Delimiter defined in the *Bill of Materials* dialog box. The HTML report will be displayed in a standard table format with grid-lines creating a matrix structure.
Column Pad	Enter the character that appears on both sides of the column separator character. The value of the column pad character in the default template is a space (" ").
Unique	Select this to list each reference designator for a part on a separate row.
Ranges	Select the *Ranges* check box to indicate that ranges, such as U1-U5, can be used for reference designators. The default template file has the *Ranges* check box as selected. When the *Ranges* check box is not selected, the *Separator* and *Minimum Members* in Range fields become inactive.
Separator	Enter the character you want to use as range separator for reference designators. The default value of the range separator in the default template file is dash (-). You can change this default value and specify a different character. For example, if you have four consecutive reference designators U1, U2, U3, and U4, and if you have specified colon (:) as the range separator, the BOM report will display the range as U1:U4.
Minimum Members	Sets the minimum number of members in a range. The default template file defines the value of the minimum number of members in a range as 3. You cannot define a number less than 3 or greater than 1024 as the *Minimum Members in Range* value.
Title	Defines the title that will be used as the header in the Callouts section of the report. The title value in the default template file is Callouts.

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File	Defines the name of the callout file to be used. The value of the callouts file in the default template file is `<your_inst_dir>/share/cdssetup/bom.callouts`. You can change the filename by specifying the new path in the *File* field or by using the browse (...) button.
Edit	Choose this button to open the Callouts Editor dialog box where you can change the quantity of each part, or add or delete mechanical parts. If no callout file is specified, the default callout file `<cds_inst_dir>/share/cdssetup/bom.callouts` is opened for editing.
Intersperse Associated Mechanical Parts	Choose this toggle to list the mechanical parts next to the physical parts to which they are associated. If the *Intersperse Associated Mechanical Parts* toggle is not selected, the associated mechanical parts are listed in the Callouts section of the BOM report. The default template file defines that the *Intersperse Associated Mechanical Parts* toggle is selected by default.
Header File	Defines the name of the file that contains the header to be used in the BOM report. This file is appended to the standard header as specified in the Report Header section of the *Customize Template* dialog box. The contents of the Header file are included whenever the header is printed. The default template file defines the value of the *Header File* field as "" (null string). The header file must be an ASCII text file.
Page Length	Defines the number of lines per page. By default, the column headers and page numbers are printed at the top of each page. By default, the BOM report is of a single page. By using the *Page Length* field, you can divide the report into multiple pages, where the length of each page is defined by the value in the *Page Length* field. Each of these pages will display the column header and the page number. You can also print the report header at the top of each page. For this, choose the *Print Header at Top of Each Page* toggle. You cannot set the value in the *Page Length* field below 20 because that will display too less information/ page. If you set any number below 20, when you save the file, the page length value will automatically revert to 20.

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Print Header at Top of Each Page	When you change the value in the *Page Length* field, the *Print Header at Top of Each Page* toggle becomes active. If you choose this check box, the header information will be printed at the top of every page. If you choose *Spreadsheet Format* or *HTML* as the format for the BOM report, the report will be displayed in a single page. The values in the *Page Length* field and the *Print Header at Top of Each Page* toggle will be ignored.
Print Column Header	By default, the *Print Column Header* toggle is selected signifying that BOM report will contain a column header that lists the names of properties displayed in the report. To remove the display of the column header, clear the selection from the *Print Column Header* toggle. The *Header Separator* will be displayed in the BOM report only if you are printing the column header.
Save	Saves the changes in the template file as defined in the *Template File* field of the *Bill of Materials* dialog box.
Save As	Saves the changes in the template file with another name. This will display the *Save BOM Template As* dialog box, where you can specify the new path to the BOM template file.
Close	Closes the dialog box

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Customize Template - Physical Part Specifications

The Physical Part Specifications tab in the Customize Template dialog box allows you to specify the properties that need to be extracted from the schematic and how to format the extracted information in the BOM report. This dialog box is divided in two main sections:

- *Report Columns group box*
- *Sorting group box*

The following table describes these sections:

Report Columns	This group box allows you to determine which schematic properties need to be displayed as columns in the BOM report.
Property	This column specifies the properties that will be displayed in the BOM report. All the properties used in the schematic design and some BOM related properties (BOM_PART, BOM_INST, and BOM_QUANTITY) are listed in the *Property* column. There is a check box to the left of each property. If you choose the check box corresponding to any property, the property appears as a column in the BOM report. If the check box corresponding to any property is not selected, that property is not displayed in the BOM report. The first property listed in the Report Columns grid box is treated as the key property and it is used to sort the BOM report. By default, the first property in the Report Columns grid box is BOM_PART. This property represents the primitive name used for the part in the pstchip.dat file. The BOM report is, therefore, sorted on the BOM_PART property. To make another property as the key property, move it to the first row in the Property column. However when you change the key property, ensure that all components to be listed in the BOM report must have some non-null value against that property. See Packager-XL Reference in cdsdoc for more information about properties.

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Mech	Mech is a short-form of Mechanical. If you choose the *Mech* check box for any property row, that property is extracted in the callouts (mechanical parts) table. You must have at least one property with the Mech check box selected. If you try to deselect all Mech check boxes then an error message appears stating that you must select at least one column.
Title	Defines the column title. A default title is provided for all properties. The title for the special BOM related properties is available in the default template file. For example, the BOM_PART, BOM_INST, and BOM_QUANTITY properties have Part Name, Ref Des, and Qty as the title. The title for all properties that are obtained from the netlist files is the same as the property name. You can edit the title for any property.
Width	Defines the number of characters that will be used as the width for the column. If an entry is longer than the column width, it continues in the next line. Therefore, the report always appears in a tabular structure. To change the value in the Width cell, click in the cell and either enter the new value or use the spin box to choose the new value. The maximum width that you can define is 1023 characters while the default width is obtained from the template file. Two columns are separated by a space (or any other character specified in the Column Pad and Column Separator fields in the tab). It is advisable to set the column width to allow the maximum possible property value. If the column width is less than the property value, the BOM report will be cluttered.
Justification	Specifies whether the column text will be left justified, right justified, center justified, or not justified (none). To choose a value for Justification, click in the cell. A list box appears with four values: Left, Right, Center, and None. You can choose any of these values.
Total	Choose the check box to specify that the column total for the selected property must be displayed in the BOM report. This total is displayed at the end of the report.
Subtotal	Choose the check box to specify that the value displayed for the column is a product of the property value and the BOM_QUANTITY for that row.

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Quote

When you generate the BOM report as a spreadsheet, select the Quote check box to ensure that the property value is enclosed in double quotes if the value has a delimiter.

For example, if you are using a semi colon (:) as the delimiter and have a property such as D:E, the property value will be displayed as “D:E” when the Quote check box is selected.

The Quote option is also useful if you have a property value with the following format: xxx-xx-xx, say PART-NUMBER = 9011-05-11.

In such cases, the spreadsheet program modifies the format and changes the data type to date and displays the data as 5/11/9011.

When you select the Quote check box, the BOM utility adds a leading space and ensures that the spreadsheet program does not modify the data type.

The Quote option is also useful if the property value has a space in it. Without the quote option, the value might be split in the output report file.

You can also use the -forcequotes argument as “bomhdl -proj *.cpm –forcequotes” in the command line for column values. If you use this argument, quotes are added to all column values regardless of the Quote check box selection.

Missing Value

Enter a string value that will be displayed if a property is missing for a component. The default value is “?”. You can change this value.

The columns in the BOM report will appear in the order specified in the grid rows. To reorder report columns, you need drag and drop the columns and change the order of the grid rows.

An associated mechanical part does not inherit PTF properties from the parent electrical part. The property columns in the BOM report are therefore based on this field. In case no customization is done, the default value is used.

Serial Number

Turn on this toggle to assign a serial number to all the parts displayed in the BOM report.

Start

This field becomes active when the *Serial Number* toggle is selected. You can change the starting serial number to one of your choice by using the arrow buttons.

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Filters	Choose this button to launch the Part Filters dialog box. This dialog box allows you to include specific parts from the BOM report by defining the conditions on part names and properties.
Style	Determines the sorting style. The sorting style in the default template file is alphabetic. You can change this style to alphanumeric. If you have three parts with reference designators U1, U2, and U11, then, in the alphabetic sorting style, the result will be U1, U11, and U2 while in the alphanumeric sorting style, the result will be U1, U11, and U2.
Order	Determines the sorting order. The sorting style in the default template file is ascending. You can change this style to descending.

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Customize Template - Variant Settings

The *Variant Settings* tab in the *Customize Template* dialog box allows you to customize the variant section in the template file. This tab will display only if you are generating variant BOM reports (that is, you have selected the Variant BOM button in the *Bill of Materials* dialog box). This dialog box is organized in two group boxes:

- *Alternates group box*
- *Miscellaneous group box*

The following table describes these sections:

Alternates	This group box allows you to define three types of reports based on the inclusion or exclusion of information about alternates.
Exclude	Choose the *Exclude* button to generate a variant report that does not include alternates. The report lists only the preferred value of components. When a function is excluded from a variant, the components which are part of the function are DNI for that variant. While generating a variant BOM, you can show DNI components by selecting the *Include DNI Components List* option. This will show all the components of the excluded function (DNI and non-DNI) as DNI.

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Include

Choose the *Include* button to generate a variant report that contains information about all preferred and alternate values of components. By default, all DNI components are displayed as separate list at the bottom of the report.

When you choose the *Include* button, the *Duplicate SNo. For Same Reference Designator* toggle and *Alternate Limit check* field are displayed.

By default, the BOM report does not repeat the serial number for the same reference designator in case of alternate values. If you want to display the reference designators for alternate values, choose the *Duplicate SNo. For Same Reference Designator* toggle. You can choose this toggle only if refdes is the key property in the *Physical Part Specifications* tab.

The default limit for the number of alternates that will display in the BOM report is 99. You can reset this limit to any number between 0 and 99 by typing the new number in the *Alternate Limit* field.

Delta Only

Choose the *Delta Only* button to generate a variant report that lists the differences between the variant and the base schematic. All the alternate values of components for the variant appear as DNI in this report.

Miscellaneous

This group box allows you to customize the formatting of the BOM report. You can specify whether DNI components be displayed in the report. You can also specify your own designators to specify the status of different components.

Include DNI Components

If you want the variant report to contain the list of DNI components, choose the *Include DNI Components* toggle. This will display the list of DNI components but not their property values.

When the *Include DNI Components* toggle is selected, the *Show Values For DNI Components* toggle displays. Choose this toggle to display the property values for DNI components.

Status

This group box contains five fields, which you can use to customize the information in the BOM report.

Preferred

Enter the value that you want to use to designate the preferred status in the BOM report. By default, the value is *Pref*.

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Alternate	Enter the value that you want to use to designate the alternate status in the BOM report. By default, the value is *Alt*. For the first alternate, this value is *Alt1* and for the second alternate this value is *Alt2*. For example, if you specify `ABC` as the alternate value, the first alternate will be assigned the status `ABC1` and the second alternate will be assigned the status `ABC2`.
DNI	Enter the value you want to use to designate the DNI status in the BOM report. By default, the value is DNI. You cannot have a blank value in the *Preferred*, *Alternate*, or *DNI* fields.
Values Different From Base	The value in this field is displayed next to a component when it has a value, which is not the same as the value in the base schematic. The default template file uses * to represent component values different from the value in the base schematic. You can change this value.
Value Same as Base	The value in this field is displayed in comparison BOM reports when the preferred value of a components is same as the base schematic values. The default template file uses a blank space to represent the component values that are same as the base schematic values. You can change this value.

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Report Parameters - Callouts Editor

The *Callouts Editor* dialog box displays all the mechanical parts, all the properties corresponding to them, and their quantity. The information about the callout properties is picked from the template file or the callouts file that you can specify using the Callouts - *Title* field in the *Customize* Template dialog box.

You can use the *Callouts Editor* dialog box to add or remove mechanical parts. You can even modify the quantity for each mechanical part. To edit the BOM_QUANTITY property, choose that cell and enter the new value. The changed value will be effective only when you choose the *Save* button.

Callouts are displayed as the last section in a BOM report. This section lists the serial number and the values of those properties the *MECH* check box for which are selected in the *Customize Template - Physical Part Specifications* tab. If you want to display values for any property in the *Callouts* section of the BOM report, select the *MECH* check box corresponding to that property in the *Customize Template - Physical Part Specifications* tab. Ensure that you have at least one *MECH* check box selected for any property to display its value in the BOM report.

The *Callouts Editor* dialog box contains the following buttons:

Add Part	Choose this button to display the Mechanical Part browser from where you can add more mechanical parts. You can choose the PPT rows in the Mechanical Part browser to add to the `callouts` file. The default quantity of the part is 1. If you need to change this value, you can later edit it. You can even assign a non-integer value to the part. **Note:** To include mechanical parts in the ptf files, ensure that they are assigned the `CLASS=MECH` property. BOM-HDL will list only those components from ptf files (as mechanical parts) that are assigned the `CLASS=MECH` property. You can add these parts using the Add Parts button.
Remove Parts	Choose this button to remove the mechanical parts from the list. To remove a mechanical part, first choose it and then click the *Remove Parts* button.
Save	Choose this button to save the changes to the *callout* file.
Close	Choose this button to close the *Callouts Editor* dialog box and return to the place from where you opened the dialog box.

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Report Parameters - Callouts Editor - Physical Part Filter

When you choose the *Add Part* button to add a mechanical part in the *Callouts Editor* dialog box, the *Physical Part Filter* dialog box displays. This dialog box is used to include mechanical parts from the Physical Part Table (PPT) files. The *Physical Part Filter* dialog box contains the following fields:

Part Names	The Part Names box displays the part names. When you choose any part name, all the available PPT rows for that part are displayed in the Property List.
Property List	The Property List displays all physical property names from left to right in the order you specify in the Property Options dialog box. The Filter field on the top of each column heading allows you to filter physical property values based on the string you enter. For example, if you have ten rows appearing in the Physical Part Filter dialog box and you want to filter out and use only those physical parts with part numbers starting with 1, enter 1* in the Filter field and press enter. The Physical Part Filter dialog box displays only those physical part table rows with part number starting with 1.
Use Case Sensitive Filtering	Choose the Use Case Sensitive Filtering check box to use case sensitive filtering of physical properties from a PPT. For example, consider that the PPT for the selected part has two rows and the values for the JEDEC_TYPE property are C123 and c123. If you choose case sensitive filtering, type C* in the filter, and press Enter. The Physical Part Filter dialog box will display only that row, which has C123 as the value for the JEDEC_TYPE property.
Reset Filters	Choose this button to reset all applied filters to default values. By default, no filter is applied for any property.
Options	Choose this button to display the Property Options dialog box. The Property Options dialog box allows you to define the settings for annotating physical properties on the schematic.

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Part Specifications - Part Filter

The *Bill of Materials* dialog box supports the following filter options:

Filter Details	This group box allows you to choose a property and define a condition. All parts that match this condition are listed in the BOM report.
Property Name	The Property list box displays the list of component properties. You can choose a property to define a condition on it.
Condition	The Condition list box displays a list of conditions that you can use to filter parts. The conditions available are: ■ Is Equal To ■ Is Greater Than ■ Is Less Than ■ Is Not Equal to ■ Is Greater Than Equal to ■ Is Less than Equal to ■ Like - This condition applies for wildcard entries
Value	You define the value of the property in this field.
To Selected Filter	Choose this button to add the condition to the selected filter in the filter list. The new condition will be added to the selected filter with an AND condition.
Add Filter Name	Choose this button to add the filter as a new filter to the list of filters.
Filter List	This group box displays the filter list where all the defined filters are displayed.

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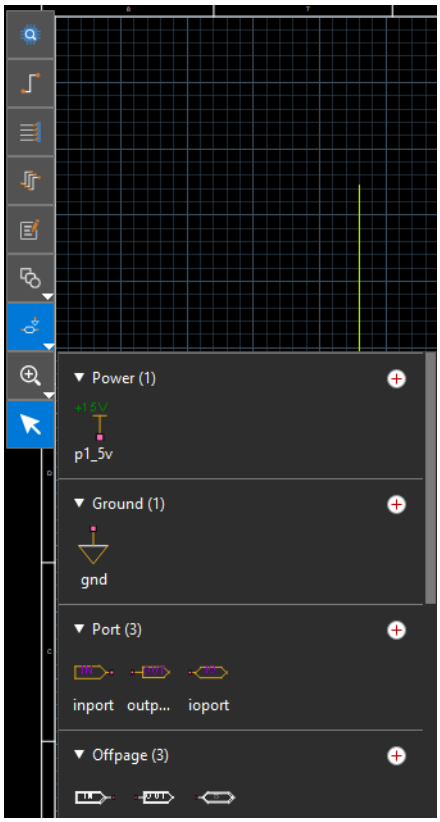
D

Using Special Symbols

There are many components used in the design that are not packaged. These components provide logic to the design and are important for the working of the design. Some examples of such objects are Power Symbols, Ground Symbols, Ports, Off-page bodies, Alias symbols, and so on. You can access the Special Symbols from the floating toolbar. You can select and add special symbols directly to your design from this bucket.



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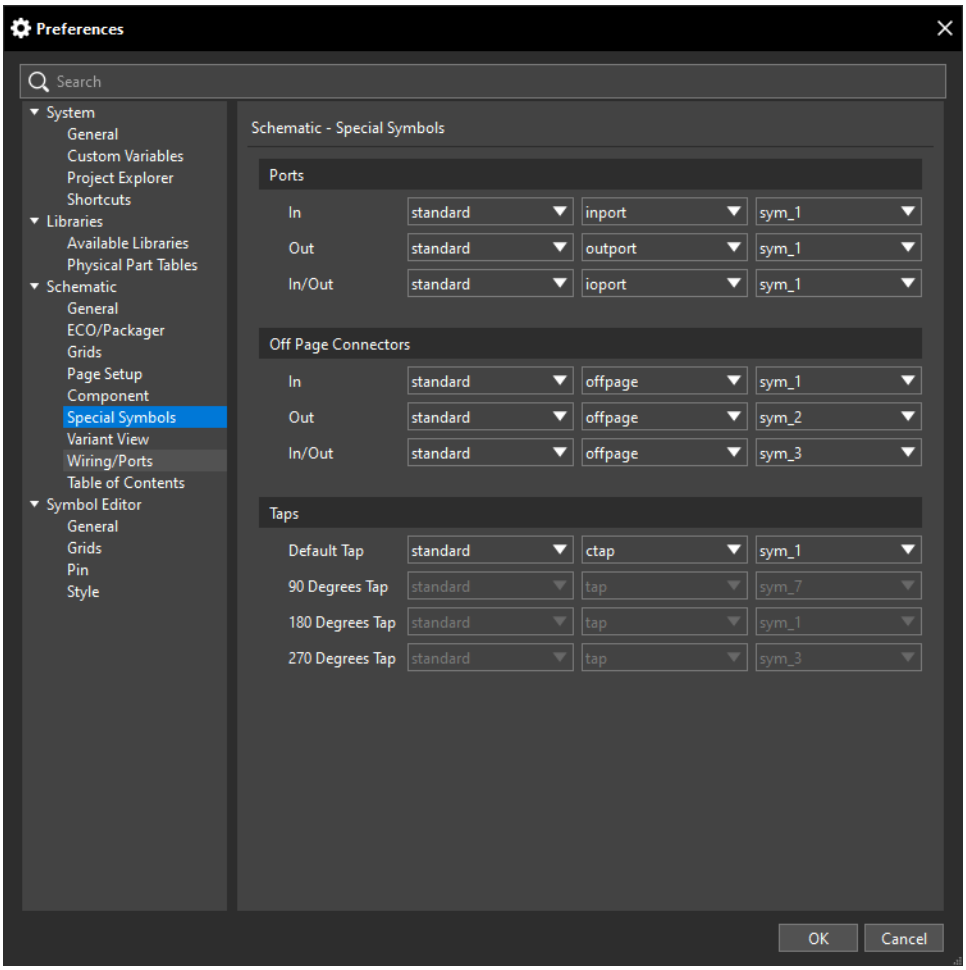
Special Symbols Available to Design

The special symbols available to you depend on the configuration done. You can also configure this from the *Preferences* window.



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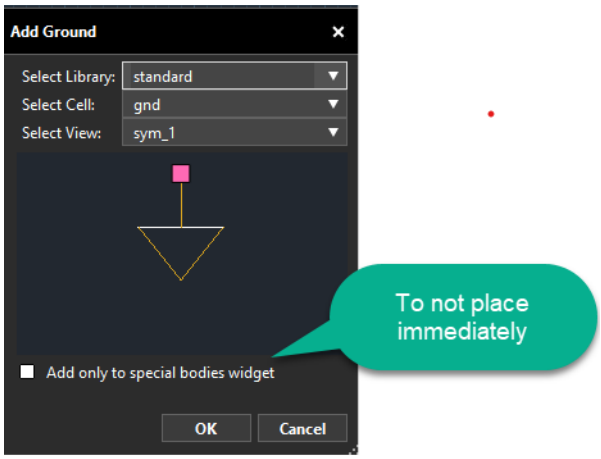
Adding Special Symbols to the Panel

To add a new symbol:

1. Open the *Special Symbols* panel.
2. Click the ⊕ button in any of the required category.

   A dialog box opens.
3. Select the library, cell, and view.



   By default, the symbol gets added to the panel as well as gets available for placing.
4. To add the symbol **only** to the panel and not place it immediately, choose *Add only to special bodies widget*.
5. Click *OK*.

Adding Special Symbols to Components

To add special symbols, perform these steps:

1. Right-click a component and choose *Draw Stubs – Same as Pin Name*.

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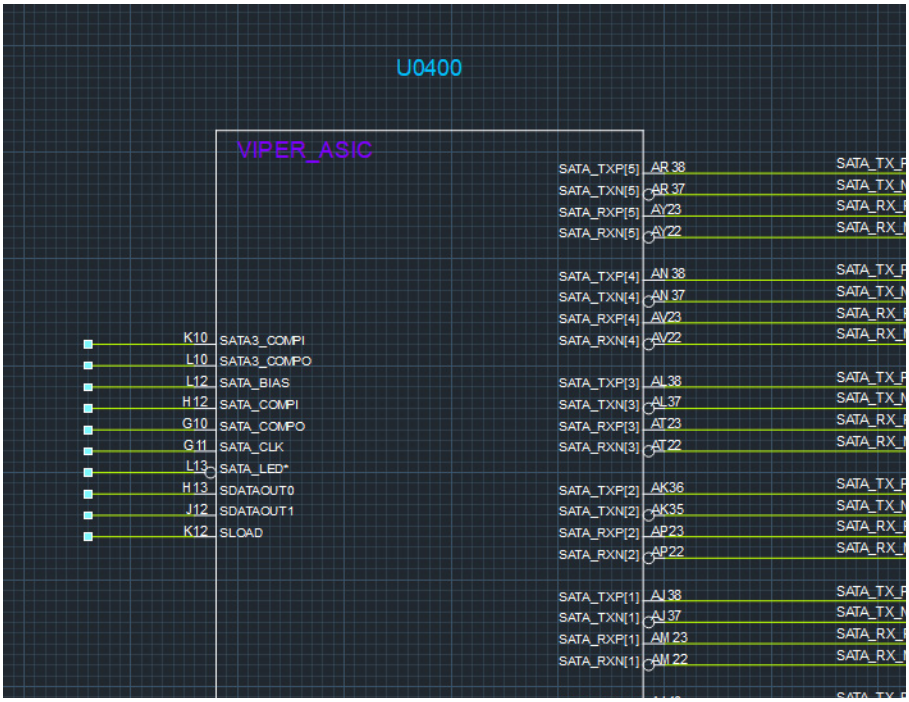
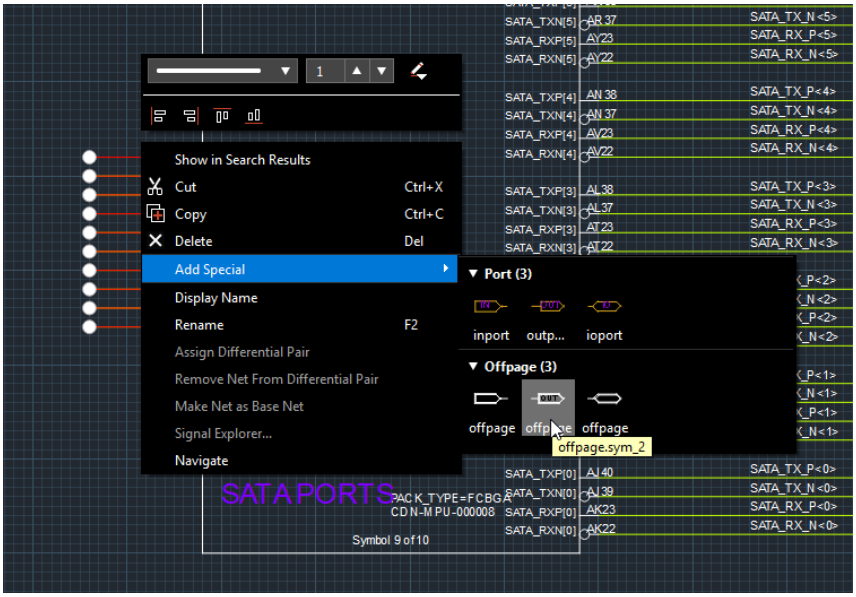
Wire stubs are drawn on all the unconnected pins present on the left side of the symbol.



2. Select the wire stubs.
3. Right-click and choose *Add Special – Offpage – OUT*.



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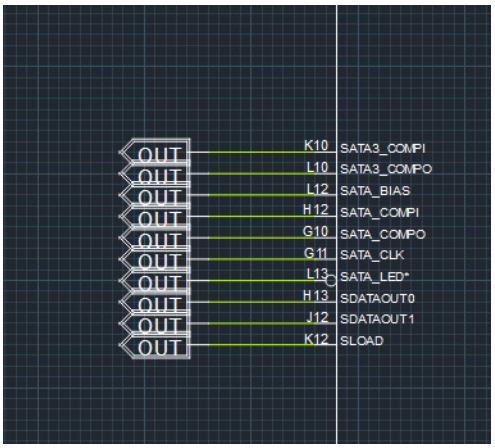
The *OUT* offpage symbol is added to all the selected nets.



Special Symbols Available

Special symbols can be easily configured at the SITE area using directives in the site.cpm file. The configured special symbols are available in the Special Symbols bucket.

The following directives in the site.cpm file help in configuring the special symbols:

```
POWER_SYMBOLS '+1_5V!1.5V:standard:p1_5v:sym_1' 'GND!0V:standard:gnd:sym_1'

INPORT 'standard.inport:sym_1'

OUTPORT 'standard.outport:sym_1'

IOPORT 'standard.ioport:sym_1'

OFFPAGE_INPUT 'standard.offpage:sym_1'

OFFPAGE_OUTPUT 'standard.offpage:sym_2'

OFFPAGE_IO 'standard.offpage:sym_3'

ALIASBODY 'standard.alias:sym_1'

NO_CONNECT 'standard.nc:sym_1' 'standard.nc:sym_2' 'standard.nc:sym_3'
     'standard.nc:sym_4'
```

Tip

You can also directly attach special bodies, such as ports and off-page connectors, to wires and buses using the *Add Special* command after right-clicking a wire or a bus on the canvas.

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Specifying Multiple Power Symbols

In case you need to define multiple power symbols and it is inconvenient to define it in one line, you can split them across lines and use backslash (\) at the end of each line. For example:

```
POWER_SYMBOLS \

    'GENERIC!TBD:standard_atdm:generic:sym_1 \

    'VCC!+5V:standard_atdm:vcc:sym_1' \

    'VCSAUV!+5V:standard_atdm:vcsauv:sym_1' \

    'VSS!0V:standard_atdm:vss:sym_1'
```

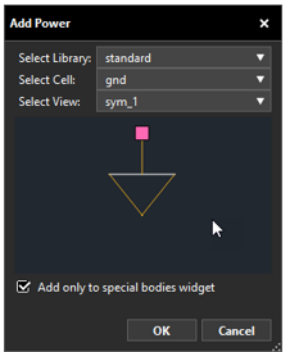
Tip

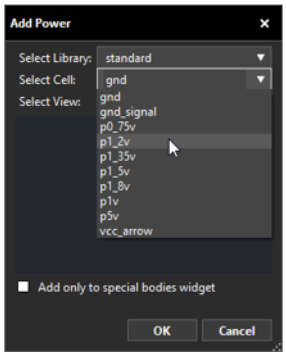
System Capture recognizes `GROUND` also as `GND`

Special symbols, such as Ports and Off-page Connectors can be directly attached to one or more wires or buses from the *Add Special* command in the right-click pop-up menu on the canvas. This provides a quick way of adding the special symbols to the design.

You can also configure Special Symbols bucket while working on the design. This can be done by clicking the button in the Special Symbols bucket. The button is available in all the categories in the bucket. This button opens a dialog where you can select the special symbol to add to the Special Symbols bucket. You first select the library followed by the cell in that library, and finally the symbol version to be used.

The dialog filters the cell data to show only those cells which appear in the selected category. As an example, if you are adding a Power or Ground symbol, the tool filters the cell data to display only the symbols in the Power or Ground category.





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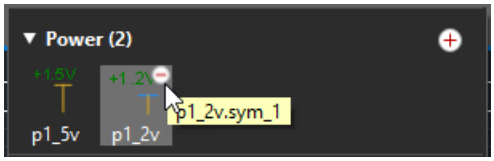
After the selection is made, the symbol is added to the Special Symbols bucket and is ready for use in the design.

The directives in the project (cpm) file are also updated to reflect the new addition in the special symbols.

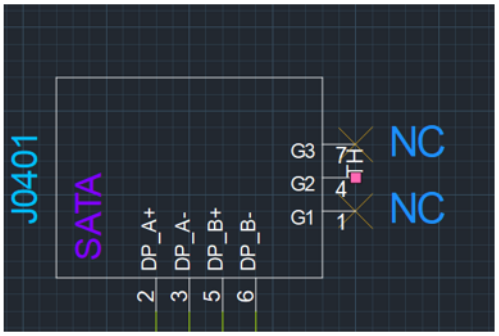
```
POWER_SYMBOLS '+1_5V!1.5V:standard:p1_5v:sym_1' 'GND!0V:standard:gnd:sym_1'
     'standard:p1_35v:sym_1'
```

After you have configured all the special symbols in your project, you can transfer this information from the project (cpm) file to the site.cpm file to utilize it across all the designs using this site.

The configured special symbol(s) can be removed from the Special Symbols bucket. When you hover over a special symbol, a button shows up on the symbol. This button can be used for removing the symbol from the Special Symbols bucket.



No-connect symbol is a special body that is added to the pins which are explicitly left unconnected. Adding this symbol, suppresses DRCs reported for such pins.



The *Selection Filter* has an entry for Special Symbols. This enables you to select only the special symbols, such as offpages, ports, tap bodies, and so on. This ensures that the special symbols do not get selected which selecting component instances.

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Properties of Special Symbols

The following table lists how System Capture recognizes special symbols. This is important when importing designs or creating new projects based on existing designs that were authored in other applications, such as OrCAD Capture or Design Entry HDL (DE-HDL).

Type of symbol	Mandatory Requirements
Power or Ground	■ One-pin component ■ Component has any ***one*** of the following properties applied with value set to `signal_name` ❑ `HDL_POWER = signal name` ❑ `VHDL_POWER = signal name` **Note:** If signal name is `NC`, the component is treated as a no connect symbol. See NC Component Or ■ Pin has `SIG_NAME` property with any of these values ❍ *<sig_name>***\g** ❍ **!***<sig_name>* ❍ **/***<sig_name>*
NC Component	This is a special use of power or group symbol where the value of signal name is `NC`. ■ One-pin component ■ Component has any ***one*** of the following properties applied with value set to `NC` ❑ `HDL_POWER = NC` ❑ `VHDL_POWER = NC` Or ■ Pin has `SIG_NAME` property with any of the following values: ❍ `NC` ❍ `NC\g`

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Type of symbol	Mandatory Requirements
Bus Tap	■ Two-pin component ■ One pin must have the `BN` property ■ Component has any ***one*** of the following properties with value set to `TRUE`: ❑ `HDL_TAP` ❑ `HDL_BITTAP` ❑ `HDL_MSBTAP` ❑ `HDL_LSBTAP` ❑ `VHDL_SLICE`
Alias or Synonym	■ Two-pin component ■ Component has any ***one*** of the following properties with value set to `TRUE`: ❑ `VHDL_ALIAS` ❑ `HDL_REPLICATE` With the size property assigned. Or ■ Component has ***all*** the following properties: ❑ `BODY_TYPE=PLUMBING` ❑ `HDL_TAP =true` ❑ `NEEDS_NO_SIZE = true`
Port	Any of the following pin properties are set to `in, out`, or `inout`: ■ `VHDL_PORT` ■ `HDL_PORT`

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Type of symbol	Mandatory Requirements

Offpage	A component is treated as offpage, if `OFFPAGE= true`
	Note: This is overridden by Port. That is, if a symbol has:
	`offpage = True`
	`HDL_PORT = in, out, or inout`
	The component is not treated as an offpage but as a port.

Page Border	A component is treated as page border, if `PAGE_BORDER=true`
Merge Body	Any one of the following set to true. ■ `HDL_CONCAT=true` ■ `VHDL_CONCAT=true` *Caution* ***Is read from incoming designs being imported but not supported in System Capture***
Comment Body	Any one of the following: ■ `COMMENT_BODY=true` ■ `BODY_TYPE=COMMENT` ■ `TOC_SYMBOL==true` This applies only to incoming designs and `OFFPAGE` must not be `true`

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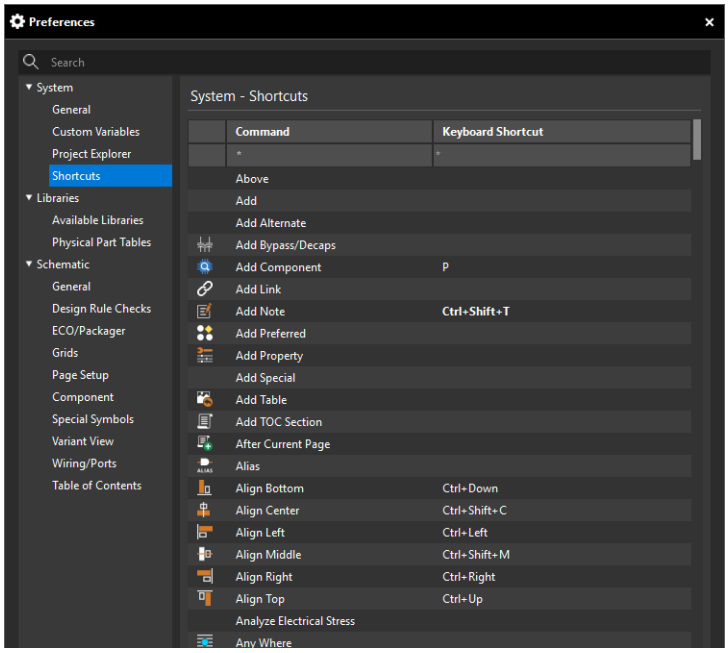
E

Assigning Keyboard Shortcuts

Keyboard shortcuts facilitate faster interaction with an application. System Capture provides support for keyboard shortcuts for all the commands that the tool supports. Shortcuts for some of the commands are preset at the installation level. You can also define your own set of shortcuts and store them at either the SITE level or at the user level.

You can view the currently assigned list of shortcuts and also specify the new shortcuts in the Keyboards Shortcut form accessible from the *Edit – Preferences – System – Shortcuts* menu. This form is also available from the Assign Shortcut command in the right-click pop-up menu on the canvas.



To define a shortcut key to a command or change a preset shortcut:

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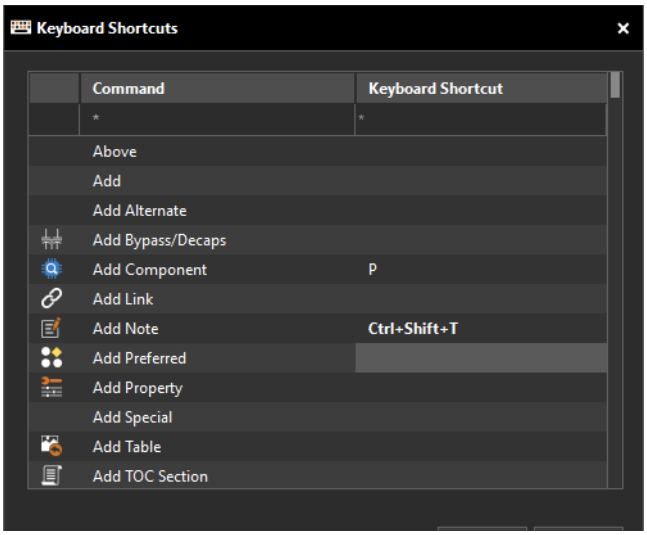
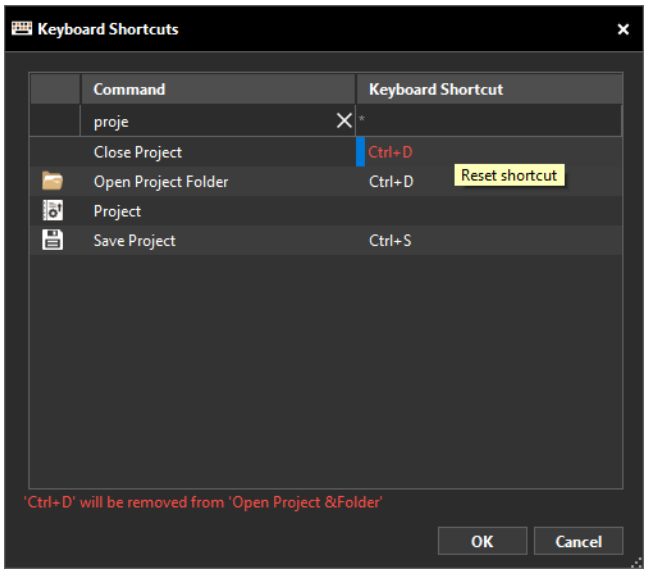
1. Right-click the canvas and choose *Assign Shortcuts*.



2. Press the desired key combination to set the shortcut.

   You can create combinations with the `Ctrl`, `Shift`, and `Alt` keys. If you change an existing shortcut, it is displayed in bold to indicate that it as an overridden value. Also, when you move the mouse cursor to the cell, a button appears in the cell which allows you to reset the shortcut to its original value.



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Tip

The default shortcuts which you modify are stored in the `cpUserShortcuts.txt` file located at *$HOME/cdssetup/canvas/resources*. This file is an incremental file and stores only those shortcuts which are not the same as the default.

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