

Design Integrity and Analysis in Allegro® X System Capture

Product Version 23.1

September 2023

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System Capture Audit and Analyses

Allegro X System Capture includes schematic audits and various analyses you can run on a System Capture design. This helps to create reliable and robust PCBs that shorten time-to-market and improve the design process. Design Integrity and analyses detect schematic design errors based on component parameters and rules. This ensures the correctness of a circuit in terms of component usage, values, polarity, and so on.

You can analyze Allegro X System Capture, OrCAD X Capture, and Design Entry HDL designs. The reliability analysis:

- Audits a schematic for adherence to design principles
- Analyzes electrical stress, MTBF, Power Topology and Thermal Floorplan
- Modifies the required default component parameters

Design Analyses

Allegro X System Capture supports the following types of analyses:

Analysis	Description
<u>Electrical Stress Analysis</u>	Examines electrical stress in complex PCBs. It increases reliability by providing a sufficient margin compared to the allowable stress limits. Electrical Stress Analysis can be run on the entire System Capture design or the subcircuits that have changed since the last analysis.
<u>MTBF Analysis</u>	Estimates the performance and safety of electrical, mechanical and electro-mechanical parts.
<u>Power Topology Analysis</u>	Validates the power distribution across the devices selected for the design.

Design Integrity and Analysis in Allegro X System Capture

System Capture Audit and Analyses

Analysis	Description
<u>Thermal Analysis with Celsius Thermal Solver</u>	Estimates stress of schematic components based on the thermal map. It helps in better placement of components early in the design cycle.

Rule Severity at Site Level

By default, audit and electrical stress settings are saved in the `project.cpm` file. If you want a team of designers to follow the same audit and electrical stress settings, it is recommended that you use a `site.cpm` file instead of `project.cpm`.

To run rules and define the severity of a rule at a site level, it is recommended that you set the rule severity in a project using the *Schematic Audit Settings* dialog box.

To ensure that the values are correctly set for the rules you want to run at the site level, copy the AUDIT* directives from the RELIABILITY section in the `project.cpm` file to the `site.cpm` file.

Related Topics

- [CPM Files](#)
- [Design Integrity CPM Directives](#)

Schematic Audit

With the growing complexity of embedded systems employed in safety critical applications, manual inspection of a schematic might not be sufficient to identify all possible issues. The design audit feature of the Design Integrity capability integrated with Allegro X System Capture includes schematic audit capabilities to ensure the quality and reliability of a design.

There are 40 default, predefined rules that are used for auditing a schematic. The following design components are excluded from the analysis:

- Connectors
- Mechanical parts
- Multi-pin discretes, operational amplifiers (op-amps)

Configuring Schematic Audit Settings

The Design Integrity solution provides you with options to modify the default setup values for schematic auditing analysis.

You can customize the predefined severity level of a rule as fatal, an error, warning, or information. For example, there is a list of predefined rules based on which a design is analyzed for violations.

Design Integrity also displays a list of potential power and ground nets in your design, which you should ideally review and configure to ensure effective audit analysis.

You can do the following to customize the level of a schematic audit:

- Configure design rules in the *Schematic Audit Settings* dialog box to modify the severity of a problem, such as fatal, error, warning, or information. Be aware that the severity can only be modified for rules available per the license.
- Modify the default upper and lower limits of pull-up and pull-down resistors for detection during analysis. For example, the default lower and upper limits for pull-up and pull-down resistors are 1000 and 10000 ohms and you can modify them.

Design Integrity and Analysis in Allegro X System Capture

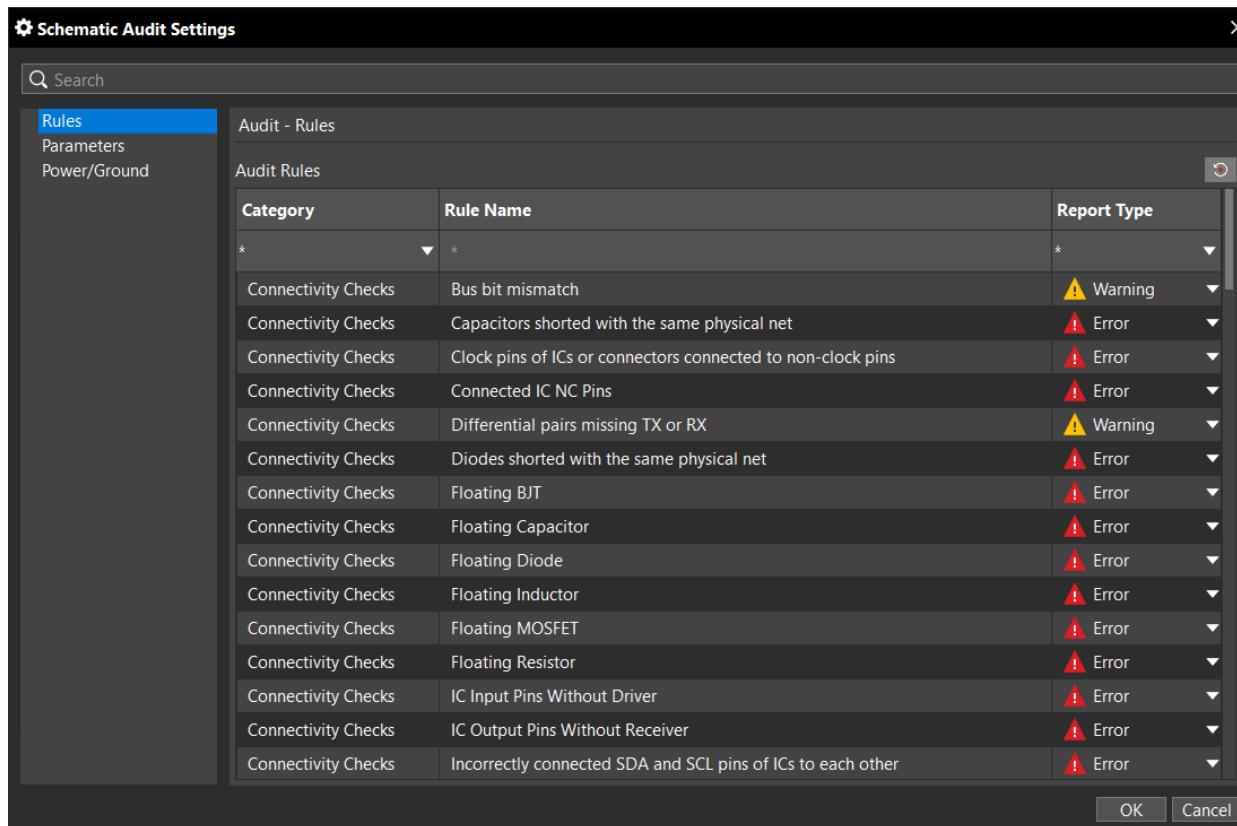
Schematic Audit

- Waive a device or audit check from the dashboard itself. Waived rules are not run the next time you run a schematic audit.

To customize audit schematic settings, do the following:

- Choose *Configure — Schematic Audit Settings* from the *Design Integrity* menu.

The *Schematic Audit Settings* dialog box is displayed.



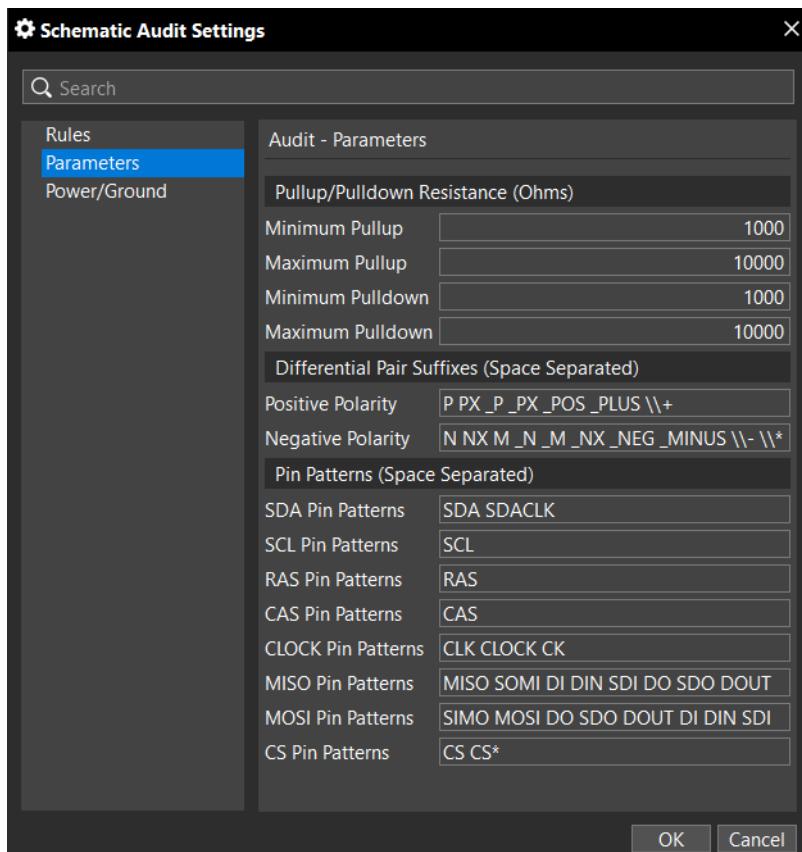
The Schematic Audit Settings dialog box is displayed. There are three tabs in the *Schematic Audit Settings* dialog box.

- In the *Rules* tab, specify which rules should be run during analysis and define the severity of a rule as fatal, an error, warning, or information message.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit

3. In the *Parameters* tab, modify the minimum and maximum positive integer values for pull-up and pull-down resistors.

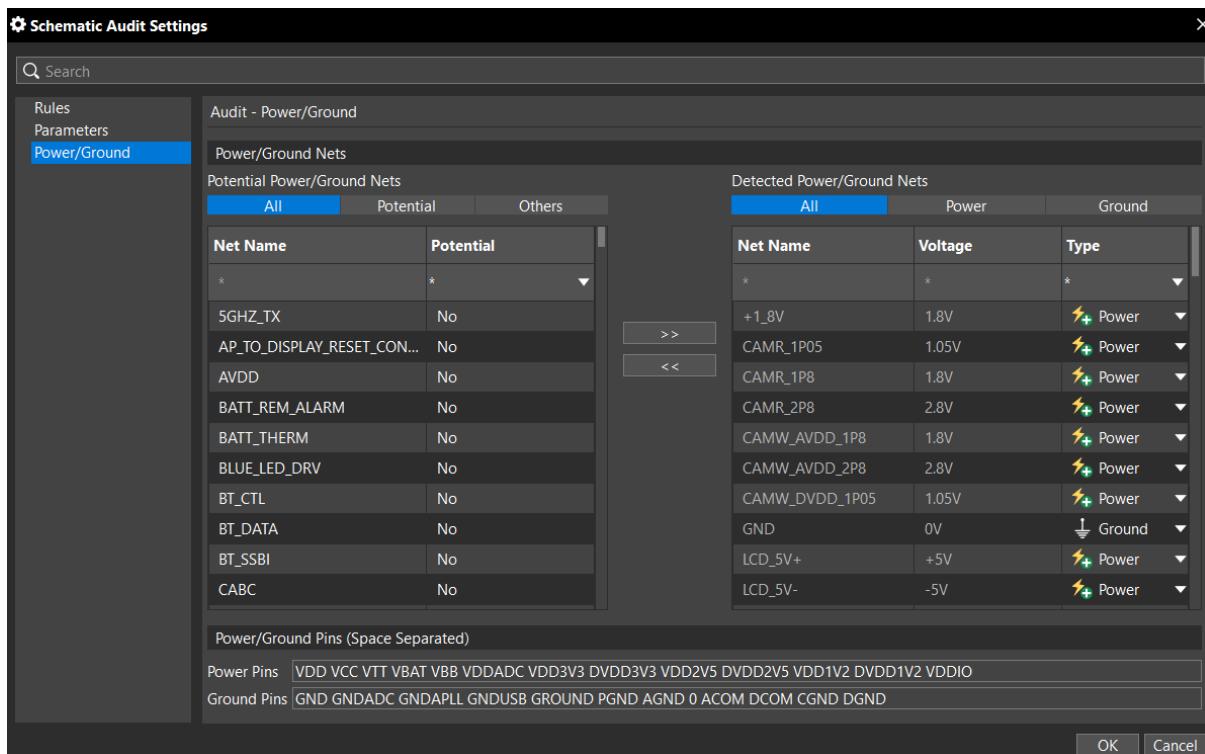


By default, Design Integrity provides the most commonly used differential pair patterns. You can also add new patterns as a space-separated list. This enables Design Integrity to recognize and run schematic audit rules for the differential pairs in the design.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit

4. In the *Power/Ground* tab, define power and ground nets by moving the required nets from the left to the right pane.



Design Integrity defines power or ground nets as follows:

- ❑ Nets with VOLTAGE properties are automatically recognized as power nets. Power or ground nets with voltage properties automatically appear in the Detected Power/Ground Nets pane on the right.
- ❑ Nets where the names suggest power nets but which do not have any assigned VOLTAGE property, are flagged as potential power nets in the *Schematic Audit Settings* dialog box. Power or ground nets with no voltage property are listed in the left pane as potential power or ground nets.

5. Add voltage properties for the power and ground nets in your design.

Related Topics

- [Rule Severity at Site Level](#)
- [Waiving Checks from Report Dashboard](#)

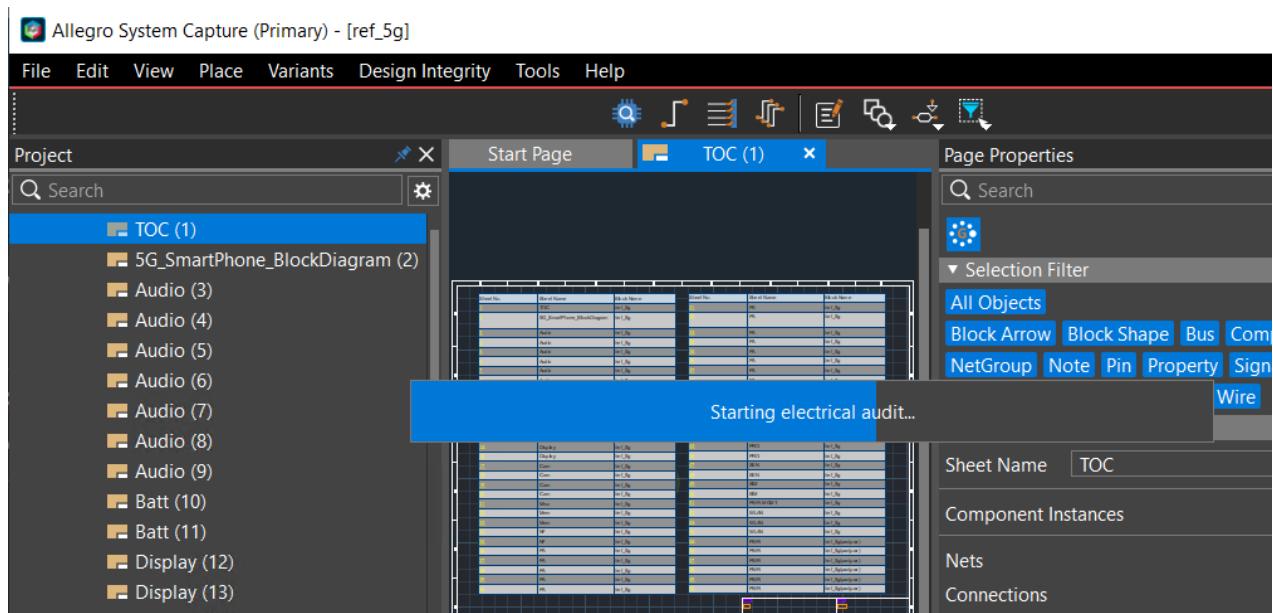
Auditing a Schematic

Design components excluded from the analysis are flagged by the audit rules. They are also listed in the electrical stress log file as unrecognized devices.

To detect design errors in your schematic, do the following in Allegro X System Capture:

1. Save the design.
2. Choose *Design Integrity — Audit Schematic*.

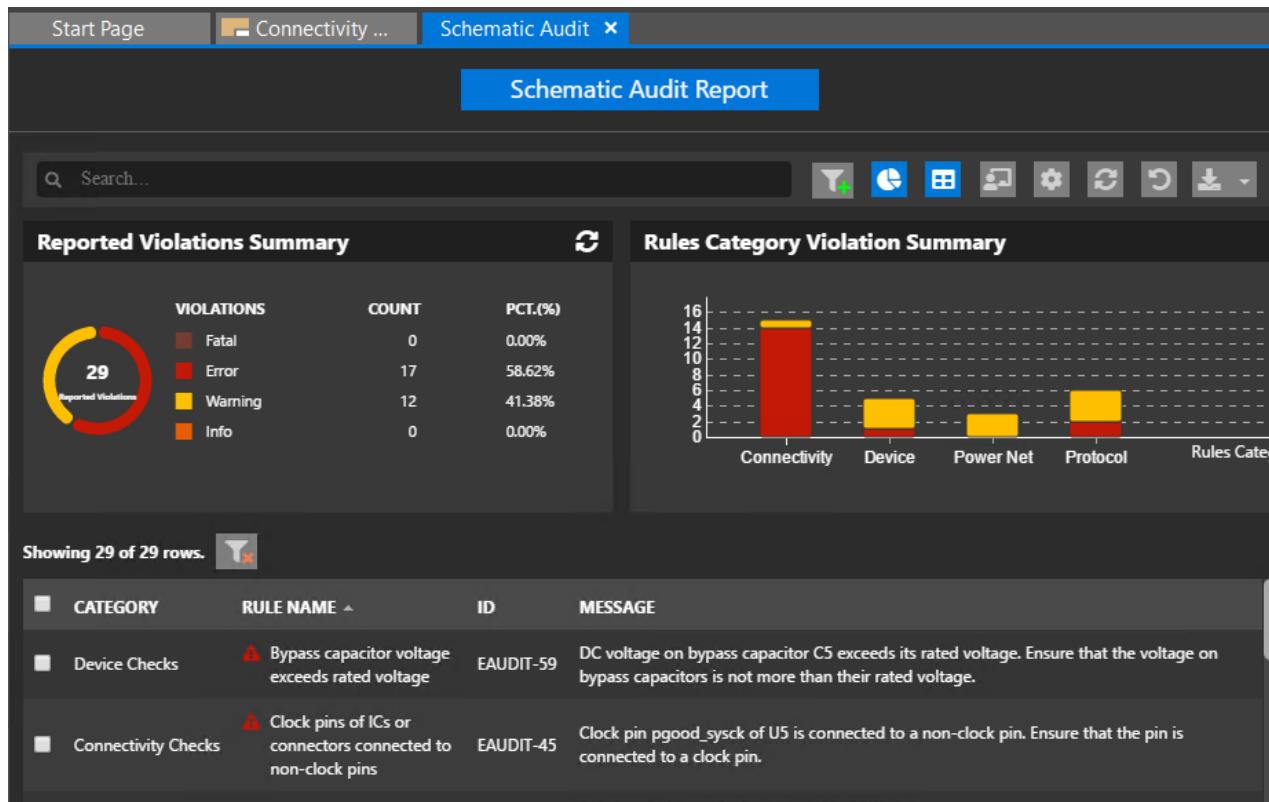
Design Integrity starts the schematic audit.



Design Integrity and Analysis in Allegro X System Capture

Schematic Audit

After the audit is completed, all the issues in the design are presented in a dashboard and are marked as fatal, errors, warnings, or information depending on predefined rules.



Related Topics

- [Schematic Audit Rules](#)
- [Configuring Schematic Audit Settings](#)

Analyzing the Results

From *Schematic Audit Report*, you can navigate to the location where the error is flagged in the schematic and resolve the issue.

Design Integrity and Analysis in Allegro X System Capture

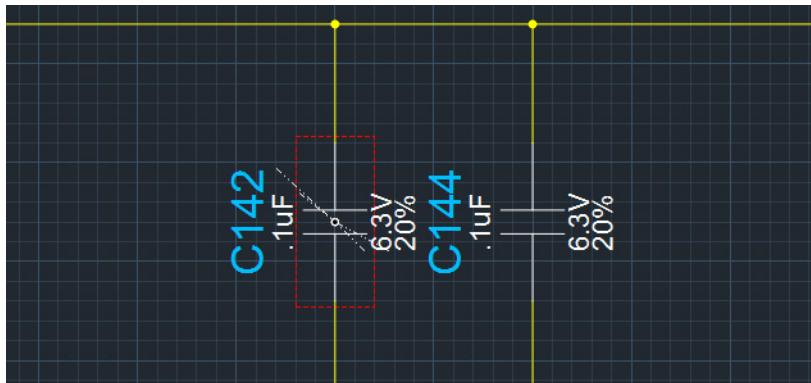
Schematic Audit

- To navigate to the location of an error, right-click the required component row in the stress report and select *Highlight Component*.

Showing 304 of 304 rows.		
CATEGORY	RULE NAME	ID
Connectivity Checks	⚠ Bus bit mismatch	EAUDIT-58
Device Checks	⚠ Bypass capacitor voltage exceeds rated voltage	EAUDIT-59
Device Checks	⚠ Bypass capacitor voltage exceeds rated voltage	EAUDIT-59

A context menu is open over the third row, showing options: Highlight, Dehighlight, Waive, and Electrical Audit Settings.

The component is highlighted in the schematic design.



Audit the schematic again after resolving the issues.

Waiving Checks from Report Dashboard

You can waive a device and or audit check from the schematic audit and electrical stress report dashboard. Waived rules are not run the next time you run a schematic audit. For example, you can choose to waive ignored and unknown devices.

To waive a check, do the following in Allegro X System Capture:

- In the violations summary report, select a row with the device to be waived.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit

- Right-click and select *Waive*.

The screenshot shows the Schematic Audit Report interface. At the top, there are tabs for 'Start Page', 'Connectivity ...', and 'Schematic Audit'. The 'Schematic Audit' tab is active. Below the tabs is a blue header bar with the text 'Schematic Audit Report'. Underneath is a search bar with placeholder text 'Search...' and a set of icons for filtering and exporting data.

Reported Violations Summary:

VIOLATIONS	COUNT	PCT. (%)
Fatal	0	0.00%
Error	17	58.62%
Warning	12	41.38%
Info	0	0.00%

Rules Category Violation Summary:

A bar chart titled 'Rules Category Violation Summary' showing the count of violations for different categories. The categories on the x-axis are Connectivity, Device, Power Net, and Protocol. The y-axis represents the count from 0 to 16. The bars show approximately 16 for Connectivity, 4 for Device, 2 for Power Net, and 4 for Protocol.

Violations List:

CATEGORY	RULE NAME	ID	MESSAGE
Device Checks	Bypass capacitor voltage exceeds rated voltage	EAUDIT-59	DC voltage on bypass cap... Electrical Audit Settings stage. Ensure that the voltage on bypass capacitors is not more than their rated voltage.
Connectivity Checks	Clock pins of ICs or connectors connected to non-clock pins	EAUDIT-45	Clock pin pgood_sysck of U5 is connected to a non-clock pin. Ensure that the pin is connected to a clock pin.

Showing 29 of 29 rows.

A context menu is open over the first violation in the list, showing options: 'Highlight', 'Dehighlight', and 'Waive'. The 'Waive' option is highlighted in blue.

- Specify a reason for waiving the violation.

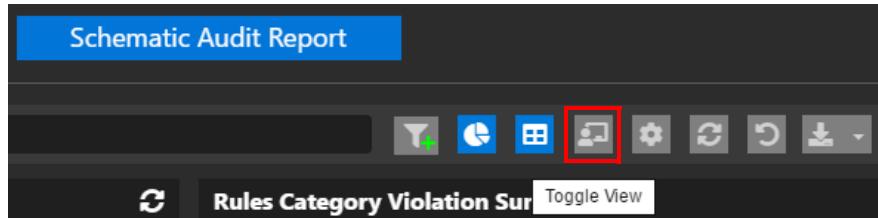
The name of the user who waived the violation is displayed by default.

The dialog box is titled 'Add Comments and Waive'. It has two main sections: 'Waived by' and 'Comments'. The 'Waived by' section contains a text input field with the value 'pvccon'. The 'Comments' section is a large text area that is currently empty. At the bottom right are 'OK' and 'Cancel' buttons.

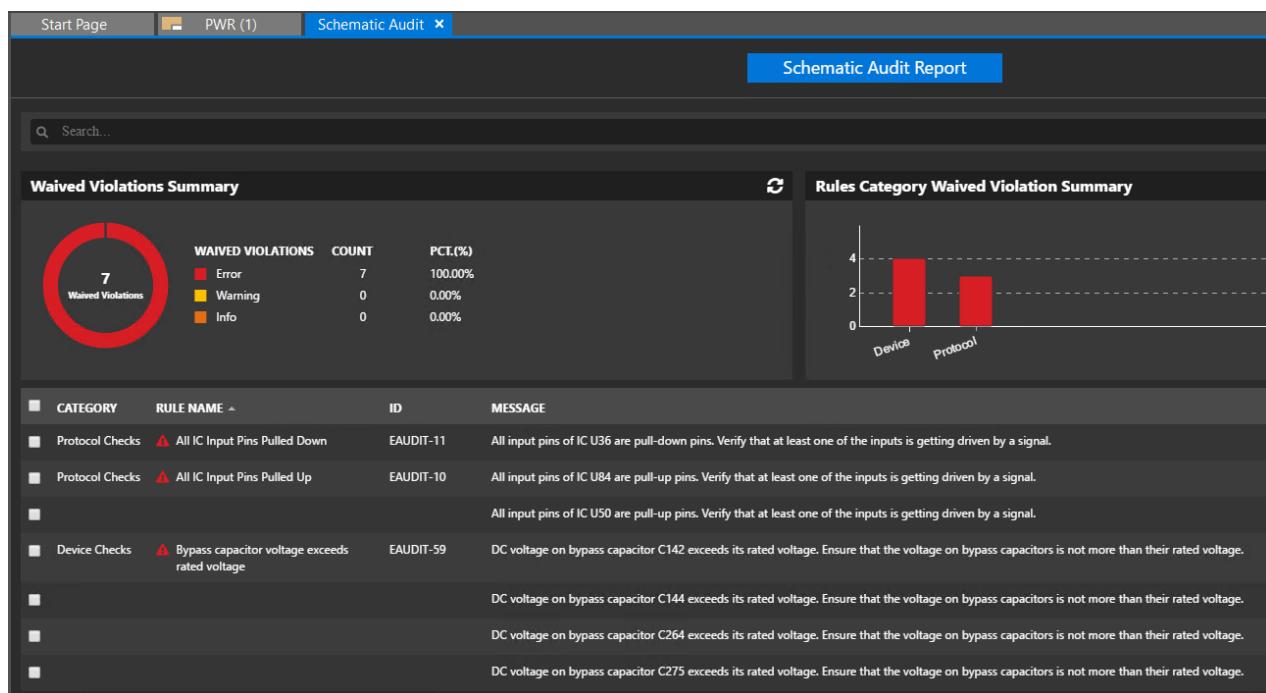
Design Integrity and Analysis in Allegro X System Capture

Schematic Audit

4. To view waived devices in the pie chart, click the *Toggle View* button in the report:



All the waived devices are listed in the *Waived Violations Summary* report.



Click **Ctrl + S** or choose *File — Save Project* to save the changes.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit

Electrical Stress Analysis

Electrical overstress (EOS) is a common cause of failure of an electronic device. An EOS failure can be caused by the failure of another device in a circuit, the misapplication of a device in a circuit, or the external application of excessive power to a device.

The Design Integrity solution uses an efficient way to analyze electrical stress in a complex PCB by splitting the PCB circuit. The electrical stress of components is calculated by partitioning the design into multiple subcircuits.

During electrical stress analysis, the available information for the library part as well as the user-defined properties for design instances are read and electrical performance parameters are calculated. These parameters include power dissipation, voltage, and current for mixed signal, analog, digital, and RF components, including DC/DC power supplies.

Component stress is checked against their maximum and derated ratings at the operating temperature. The actual power dissipated in each component is automatically calculated during the analysis, and the results are presented in a stress report.

By accounting for component variability and generating electrical stress derating reports, Design Integrity determines the circuit performance under a worst-case scenario.

Configuring Electrical Stress Settings

The Design Integrity solution provides you with options to modify the default setup values for electrical stress analysis.

It also displays a list of potential power and ground nets in your design, which you should ideally review and configure to ensure effective stress analysis. You can also modify the default upper and lower operating ratings of design components, such as resistors, capacitors, ICs, and connectors.

If user-defined property values for devices are not found in a design, Design Integrity assumes the default values during stress analysis. For example, properties such as the maximum voltage rating, power dissipation, or the maximum temperature for thermistors.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

To make the analysis results more accurate, the following steps are recommended:

- Review the classified devices in your design, and their properties, through *Configure — Electrical Stress Settings*.
- Ensure that all power and ground nets have a voltage property. This ensures that:
 - All bypass capacitors are stressed per the actual design.
 - Schematic audit scans these kinds of nets when running the stress analysis.

This step is particularly important for designs that have been imported into Allegro X System Capture from OrCAD X Capture or Design Entry HDL, where voltages were not defined for power or ground nets.

- Check the log file for devices that have been ignored because discrete RLC components do not have properly defined values. These devices are not recognized.
Note: A property REL_IGNORE=TRUE is used to ignore any devices from being used for Stress Analysis.
- Review and update the properties for all the devices in the *Electrical Stress Settings* dialog box by doing the following:
 - Ensure that the absolute maximum ratings are defined for discrete parts such as:
 - Capacitors (voltage rating)
 - Resistors (power and temperature rating)
 - MOSFETs, bipolar junction transistors (VDS, ID, and so on)

Note: Terminal voltages specified across a zero-ohm resistor cannot be different in a design.

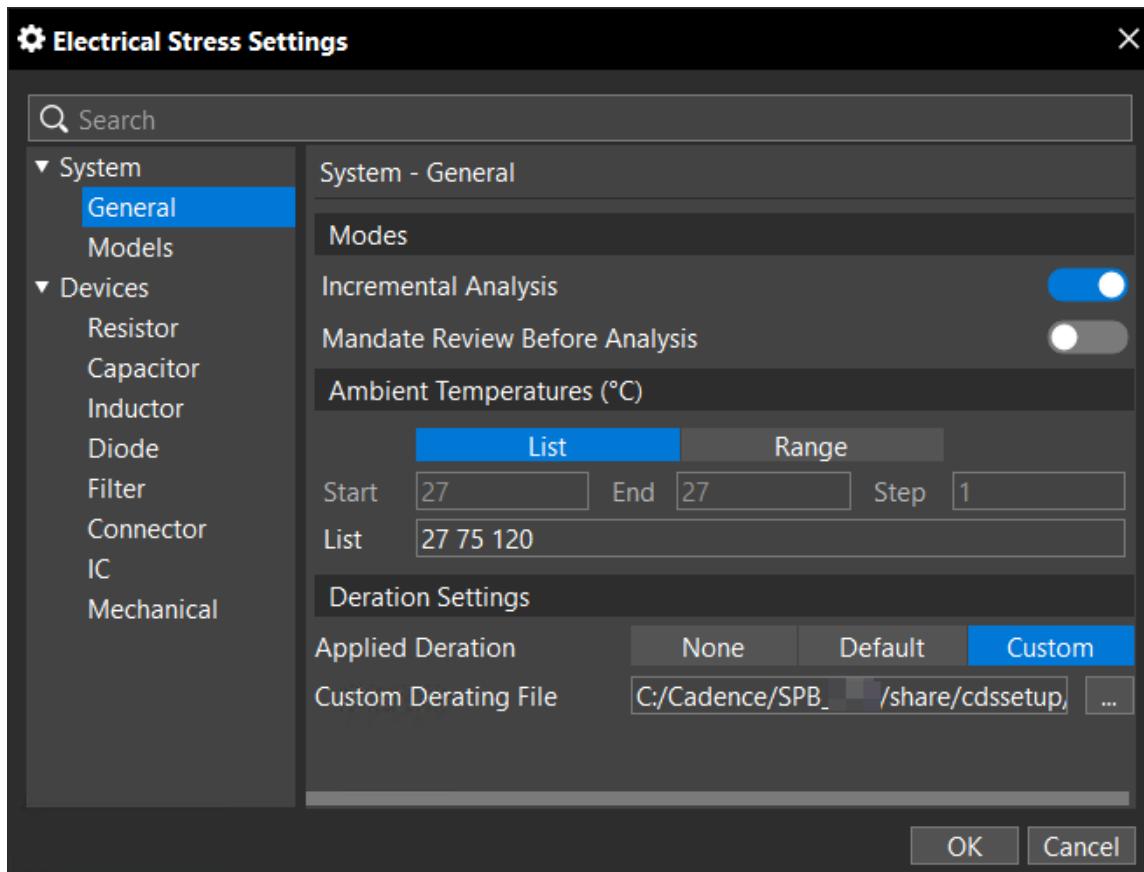
Be aware that the default temperature used for analysis is 27 degrees Celsius. This value cannot be modified.

- To access the *Electrical Stress Settings* dialog box for electrical stress configuration, select *Configure — Electrical Stress Settings* from the *Design Integrity* menu.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

Design Integrity generates a list of the electronic components in the design and the nodes they are connected to, and displays the dialog box.



The following tasks can be done to configure electric stress settings:

- [Modes of Analysis](#)
- [Defining Ambient Temperatures](#)
- [Specifying Derating Values for Device Parameters](#)
- [Modifying Device Categories and Parameters](#)
- [Mapping Terminal Order](#)
- [Modifying Device Sub-Type](#)
- [Overriding Default IC Pin Stimulus](#)

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

Modes of Analysis

Electrical Stress Analysis supports two modes of analysis:

- Device Sign-off Before Analysis. See [Signing Off Devices Before Analysis](#)
- Incremental Analyses. See [Running an Incremental Analysis](#)

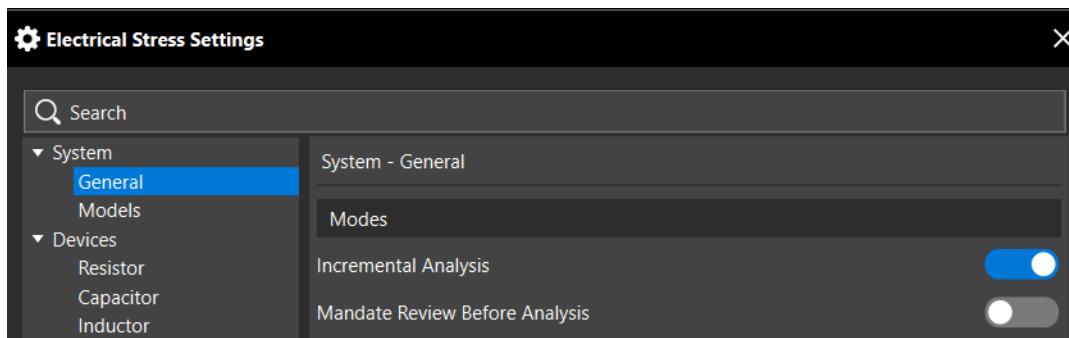
These two modes are supported with any of the following licenses:

- Allegro System Capture Designer
- Allegro PCB Venture
- Allegro System Capture Venture
- Allegro Enterprise System Design Authoring
- Allegro Enterprise Authoring Solution

You can review and sign off device parameter values before the analysis is run using the *Mandate Review Before Analysis* option in the *Electrical Stress Settings* dialog box.

When selected, this option highlights devices that have one or more parameters with default values, and enforces a sign-off of the device before proceeding with stress analysis.

To save time and improve performance, you can choose to simulate only those subcircuits that have changed since the last analysis instead of the entire design. When this option is selected, subcircuits that are unchanged since the last run are fetched from the last analysis run.



Defining Ambient Temperatures

The default derated setting for the operating temperature is 27 °C. Depending on the datasheets for the devices you work with, you can specify additional operating temperatures.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

You can specify a space-separated list of integers, such as 27 32 35 -25 -20 or a range, such as 27 to 32, -30 to -10. During stress analysis, the temperature values are analyzed against the minimum operating temperature (TMIN) value for each component.

To specify additional temperature values for a device, do the following:

1. Navigate to the *System - General* tab in the *Electrical Stress Settings* dialog box.
2. Do one of the following in the *Ambient Temperatures (°Celsius)* pane:
 - Select *List* to specify a space-separated list of temperatures.
 - Select *Range* to specify a range of values separated by a dash.

When additional temperature values are specified, the electrical stress analysis report displays the performance of the device for all the specified temperatures.

Specifying Derating Values for Device Parameters

In addition to the operating temperature of a device, you can specify derating values for all the other parameters of a device.

To specify device parameters, do the following:

1. Navigate to the *System - General* tab in the *Electrical Stress Settings* dialog box.
2. Under Deration Settings, select and specify the required options for derating values:
 - None* - no derating values are considered during the electrical stress analysis of the devices in the design
 - Default* - uses the default derating values for all the parameters of a device.
 - Custom* - you can specify custom derating values, which must be provided in a JSON file. Specify the custom derating JSON file in this field and place the file in <installation directory>\share\cdssetup\sysr.

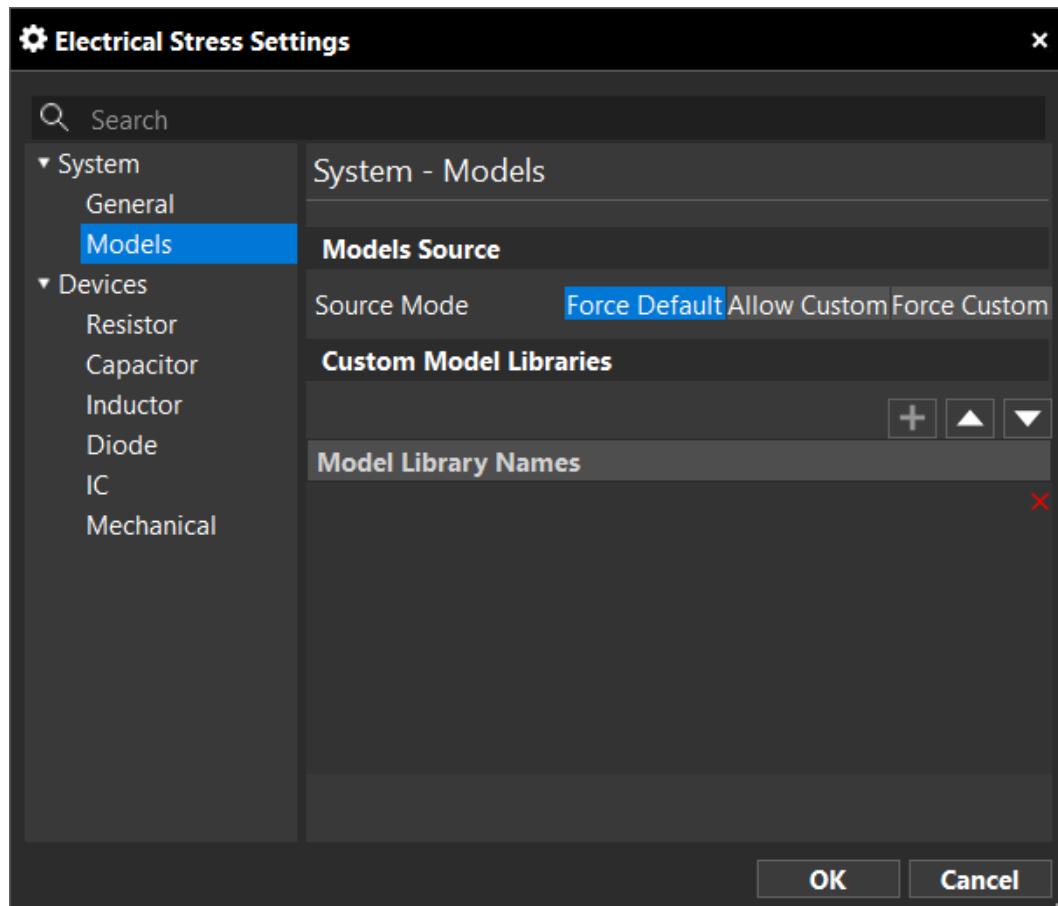
Customizing Device Simulation Models

To customize the device simulation models, do the following:

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

- Navigate to the *System - Models* tab in the *Electrical Stress Settings* dialog box.



There are three options available for Source Mode:

- *Force Default* – This option uses the default models in Design Integrity. If you do not work with custom models, continue with this option. If you want to check the default model, view the device category and model under *Electrical Stress Settings - System - Devices*.
- *Allow Custom* - This option uses custom models, if available. Else, the default models are used.
- *Force Custom* – With this option, the device is skipped during electrical stress analysis if no custom models are specified.

If you choose *Allow Custom* or *Force Custom*, click the plus icon under Custom Model Libraries and provide the path to the PSpice model library (.lib).

If you specify multiple model libraries, you can define the priority order of these libraries using the up and down arrows. This is useful if there are models with the same name in more than one library.

Modifying Device Categories and Parameters

The Design Integrity solution recognizes devices by their reference designator patterns, number of pins, and pin name patterns. Based on these, Design Integrity classifies a device into categories or might not recognize it at all. In such cases, you might need to modify the device categories.

Design Integrity also assumes the default value for all parameters but the default values are generalized. For example, if a design using a resistor of 1 ohm, its power handling capability might not be the same as the default value in Design Integrity. In such cases, you might want to update or modify the parameters per the device datasheet.

Component types in a design are listed in the *Electrical Stress Settings - System - Devices* tab.

To modify device categories or parameters, do the following:

1. Right-click a device and select *Identify Device*.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

- 2.** Select the device category from the drop-down list. For example, change the device category from a resistor to a capacitor.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

The screenshots illustrate the process of identifying a resistor instance in the system:

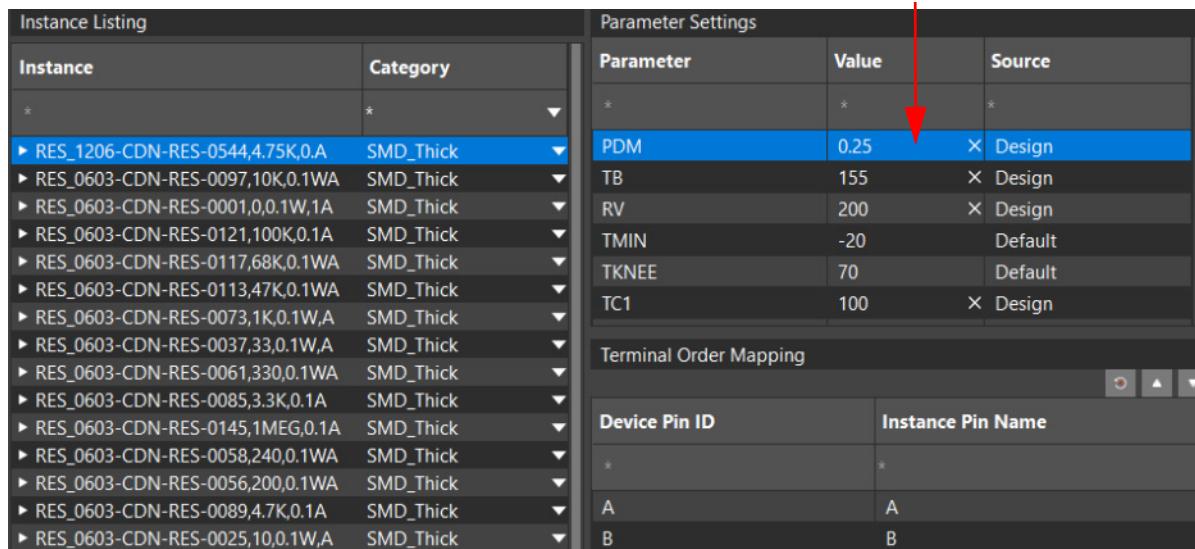
- Screenshot 1:** Shows the "Devices - Resistor" list with an instance named "Identify Device" selected. A red box highlights this instance.
- Screenshot 2:** A "Device Identification" dialog box is open over the list. It contains a dropdown menu set to "Bead". A red box highlights the dialog, and a red arrow points from the "Identify Device" instance in the list to the "Device Identification" dialog.
- Screenshot 3:** The "Devices - Resistor" list now shows the "Identify Device" instance with its category changed to "Bead". The "Parameter Settings" and "Terminal Order Mapping" sections are also visible on the right.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

3. To modify device parameter values, click in the *Value* field for a particular parameter.

You can modify root and instance-level values.



Instance Listing		Parameter Settings		
Instance	Category	Parameter	Value	Source
*	*	*	*	*
► RES_1206-CDN-RES-0544,4.75K,0.A	SMD_Thick	PDM	0.25	X Design
► RES_0603-CDN-RES-0097,10K,0.1WA	SMD_Thick	TB	155	X Design
► RES_0603-CDN-RES-0001,0,0.1W,1A	SMD_Thick	RV	200	X Design
► RES_0603-CDN-RES-0121,100K,0.1A	SMD_Thick	TMIN	-20	Default
► RES_0603-CDN-RES-0117,68K,0.1WA	SMD_Thick	TKNEE	70	Default
► RES_0603-CDN-RES-0113,47K,0.1WA	SMD_Thick	TC1	100	X Design
► RES_0603-CDN-RES-0073,1K,0.1W,A	SMD_Thick			
► RES_0603-CDN-RES-0037,33,0.1W,A	SMD_Thick			
► RES_0603-CDN-RES-0061,330,0.1WA	SMD_Thick			
► RES_0603-CDN-RES-0085,3.3K,0.1A	SMD_Thick			
► RES_0603-CDN-RES-0145,1MEG,0.1A	SMD_Thick			
► RES_0603-CDN-RES-0058,240,0.1WA	SMD_Thick			
► RES_0603-CDN-RES-0056,200,0.1WA	SMD_Thick			
► RES_0603-CDN-RES-0089,4.7K,0.1A	SMD_Thick			
► RES_0603-CDN-RES-0025,10,0.1W,A	SMD_Thick			

Terminal Order Mapping

Device Pin ID	Instance Pin Name
*	*
A	A
B	B

Hover over the operating parameters to view tool tips for a brief description of each abbreviation. The data in these parameters, such as the power dissipation or maximum temperature that a resistor can withstand, is derived from the device manufacturer or part datasheet. The updated values are then used for stress analysis.

Mapping Terminal Order

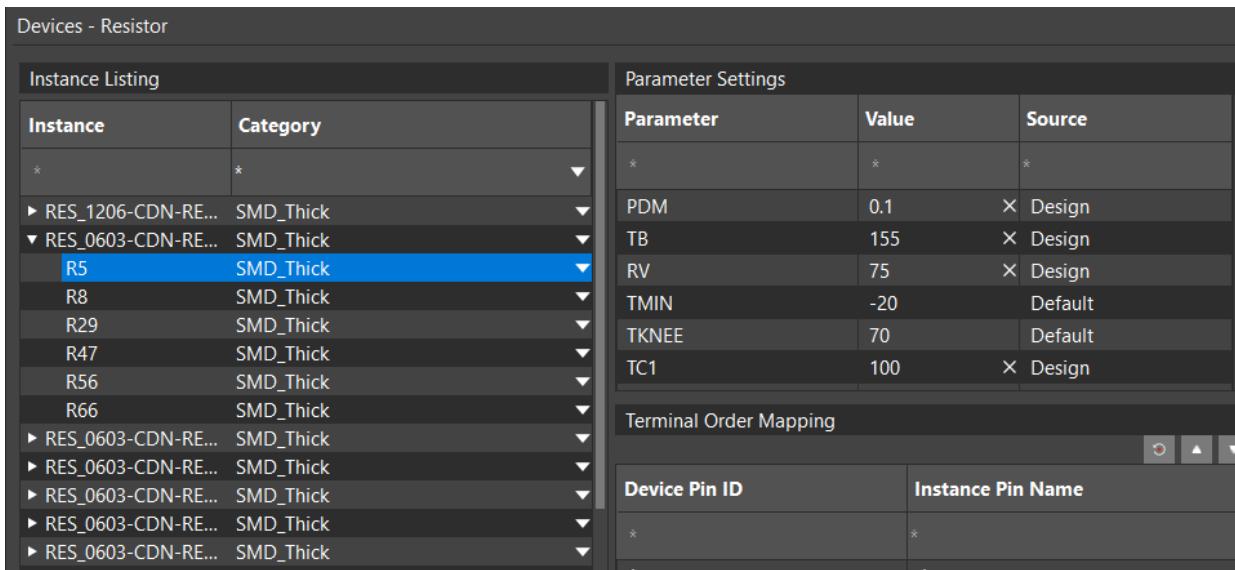
You can map the device pins versus the pins actually used for a device in the design. For example, instance R4 of a resistor has A and B pins. You can define that the cathode maps to A, and anode maps to B, or vice versa.

To map the terminal order, do the following:

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

1. In the *Electrical Stress Settings* dialog box, choose the desired device type in the *Devices* tab.



2. Restore the default pin mapping if needed and use the up and down arrows to map the term order in a custom model.

For example, a component DEMO has pin names A1 and B1.

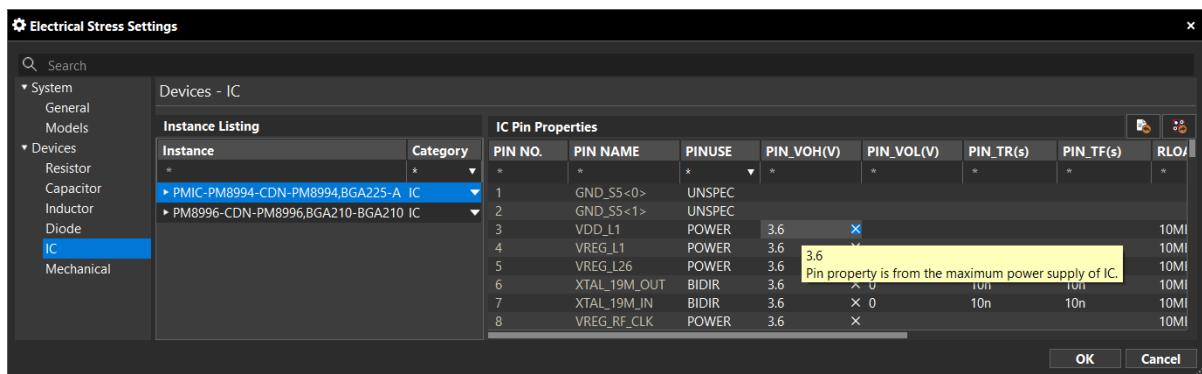
A = A1, which is the mapping of pin ID A with the actual pin, A1, on the instance. Similarly, B = B1 pin ID B is mapped to the actual pin on the instance B1.

However, say a custom model is attached to the component, and it has .SUBCKT a b where a and b are terminals of the model. Since a is specified first, the first row in the Term Order table maps to a and the second row maps to b. The final result would be: a=A=A1 and b=B=B1.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

For interface devices, such as connectors or ICs, you can view all the properties required for stress analysis and their values. The source of these values is indicated in the tool tips when you hover over the field.

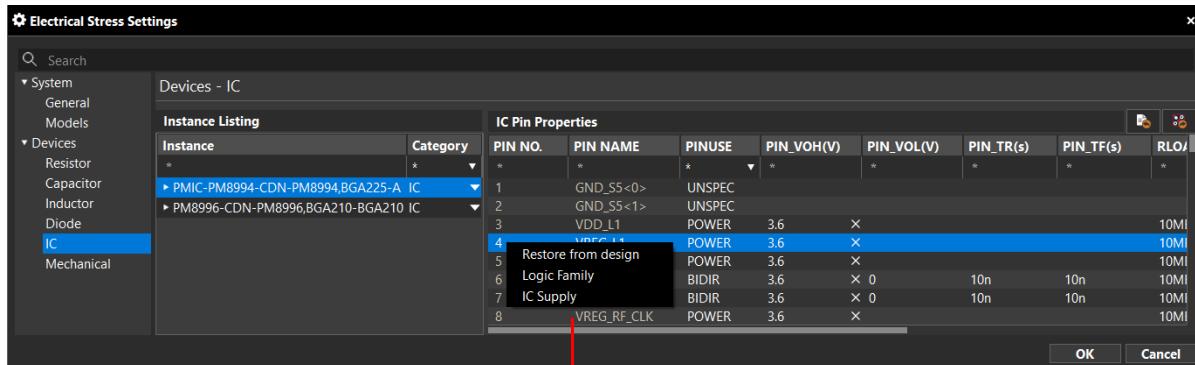


3. If required, you can modify the source by right-clicking on the pin property row and:
 - restoring the pin property from the design
 - selecting from the list of default logic families

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

- choosing the property source from the IC supply list



IC Pin Properties				
PIN NO.	PIN NAME	PINUSE	PIN_VOH(V)	
*	*	*	*	
1	GND_S5<0>	UNSPEC		
2	GND_S5<1>	UNSPEC		
3	VDD_L1	POWER	3.6	X
4	Restore from design	POWER	3.6	X
5	Logic Family	POWER	3.6	X
6	IC Supply	BIDIR	3.6	X
7		BIDIR	3.6	X
8	VREG_RF_CLK	POWER	3.6	X

You can import or export the pin properties of a device, if needed.

Mechanical Pin Properties							
PIN NAME	PINUSE	PIN_VOH(V)	PIN_VOL(V)	PIN_TR(s)	PIN_TF(s)	RLOAD(Ohm)	PIN
*	*	*	*	*	*	*	*
HOT1	BIDIR	3.3	0	10n	10n	10MEG	<<(
GND	UNSPEC						
HOT2	BIDIR	3.3	0	10n	10n	10MEG	<<(
SENSOR	BIDIR	3.3	0	10n	10n	10MEG	<<(

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

Modifying Device Sub-Type

Design Integrity automatically tries to identify the subtype of an instance based on the library properties. If the information cannot be obtained from the library, Design Integrity assigns a default sub-type to a device category to proceed with the electrical stress analysis.

However, you can change the device sub-type of a device category. For example, you can change the category of a capacitor to the following available options:

The screenshot shows the 'Electrical Stress Settings' window with the 'Devices - Capacitor' tab selected. On the left, a sidebar lists categories: System, General, Models, Devices, Resistor, **Capacitor**, Inductor, Diode, IC, and Mechanical. The 'Capacitor' category is highlighted. The main area has three sections: 'Instance Listing', 'Parameter Settings', and 'Terminal Order Mapping'. The 'Instance Listing' section contains a table with columns 'Instance' and 'Category'. The first row shows 'CAP_0603-CDN-CAP-0007,3.3NF,50A' under 'Category' with a dropdown menu open, showing options: 'Ceramic General Purpose', 'Tantalum General Purpose', and 'Aluminium Electrolytic General Purpose'. A red box highlights this dropdown. The 'Parameter Settings' section lists parameters like CV, CI, and MTBF with their values. The 'Terminal Order Mapping' section maps device pins to instance pins.

Instance	Category
CAP_0603-CDN-CAP-0007,3.3NF,50A	Ceramic General Purpose
CAP_0603-CDN-CAP-0006,2.2NF,50A	Ceramic General Purpose
CAP_0805-CDN-CAP-0173,1NF,100VA	Tantalum General Purpose
CAP_0805-CDN-CAP-0162,6.8NF,50A	Aluminium Electrolytic General Purpose
CAP_1206-CDN-CAP-0027,47NF,200A	Ceramic General Purpose
CAP_1206-CDN-CAP-0026,330NF,25A	Ceramic General Purpose
CAP_0805-CDN-CAP-0158,1.5NF,50A	Ceramic General Purpose
CAP_0805-CDN-CAP-0104,1NF,10V,A	Ceramic General Purpose
CAP_0805-CDN-CAP-0169,100NF,50A	Ceramic General Purpose
CAP_1206-CDN-CAP-0024,470NF,16A	Ceramic General Purpose
CAP_0805-CDN-CAP-0116,100NF,10A	Ceramic General Purpose
CAP_0805-CDN-CAP-0164,15NF,50VA	Ceramic General Purpose
CAP_0603-CDN-CAP-0003,680PF,50A	Ceramic General Purpose
CAP_0603-CDN-CAP-0018,3.3NF,10A	Ceramic General Purpose
CAP_1206-CDN-CAP-0022,1UF,16V,A	Ceramic General Purpose
CAP_0805-CDN-CAP-0174,1.5NF,10A	Ceramic General Purpose
CAP_0805-CDN-CAP-0134,100NF,16A	Ceramic General Purpose
CAP_0402-CDN-CAP-0034,2.2UF,6,A	Ceramic General Purpose
CAP_0805-CDN-CAP-0176,3.3NF,10A	Ceramic General Purpose
CAP_0603-CDN-CAP-0016,1.5NF,10A	Ceramic General Purpose
CAP_0805-CDN-CAP-0166,33NF,50VA	Ceramic General Purpose

Overriding Default IC Pin Stimulus

Design Integrity uses the PINTYPE or PINUSE properties on pins to determine the stimulus or load pins. It also uses the PIN_VOH and RLOAD properties for determining the stimulus and load to be applied on driver or receiver pins.

If a part library does not have IC pin voltage-level properties, default values are assigned to IC pins, particularly output and bidirectional.

Design Integrity and Analysis in Allegro X System Capture

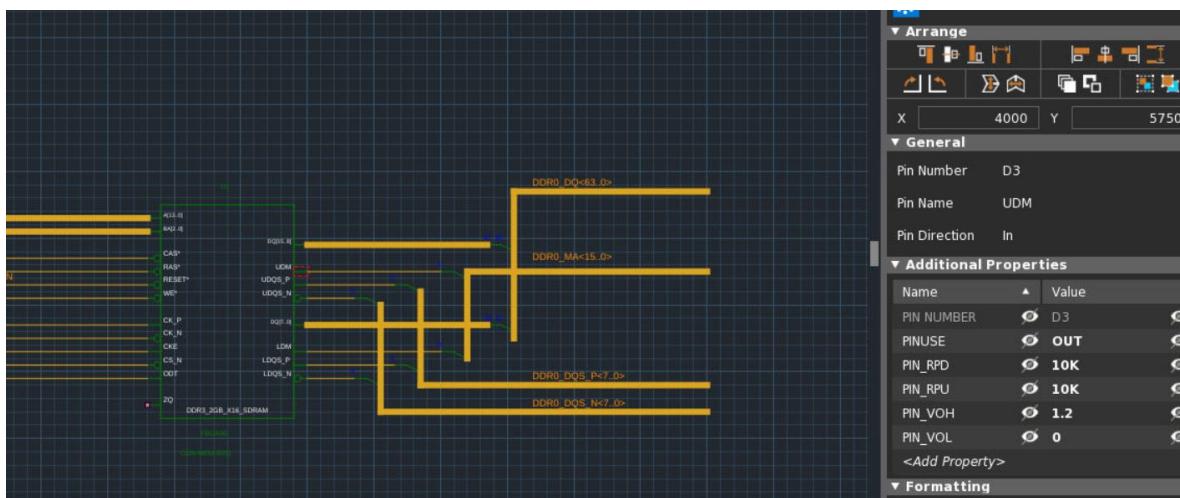
Electrical Stress Analysis

For worst-case analysis, pin voltages default to the maximum power supply of an IC, which results in worst-case estimates.

To override these automatically applied voltage values, do the following:

1. Assign properties on schematic instance pins.

You can define pin properties by selecting the required pin on the schematic and adding the required properties to the properties editor dialog box.



2. Include the relevant properties as part of the part library.

Supported pin properties in Design Integrity are as follows:

Pin Properties	Description
PINUSE	Pin type
PIN_VOH	VOH or high logic level
PIN_VOL	VOL or low logic level
PIN_TR	Pin rise time
PIN_TF	Pin fall time
PIN_RPD	Internal pull-down
PIN_RPU	Internal Pull-up
RLOAD	Receiver/input pins

Related Topics

- [Device Identification and Pin Detection](#)
- [Rule Severity at Site Level](#)
- [Waiving Checks from Report Dashboard](#)

Signing Off Devices Before Analysis

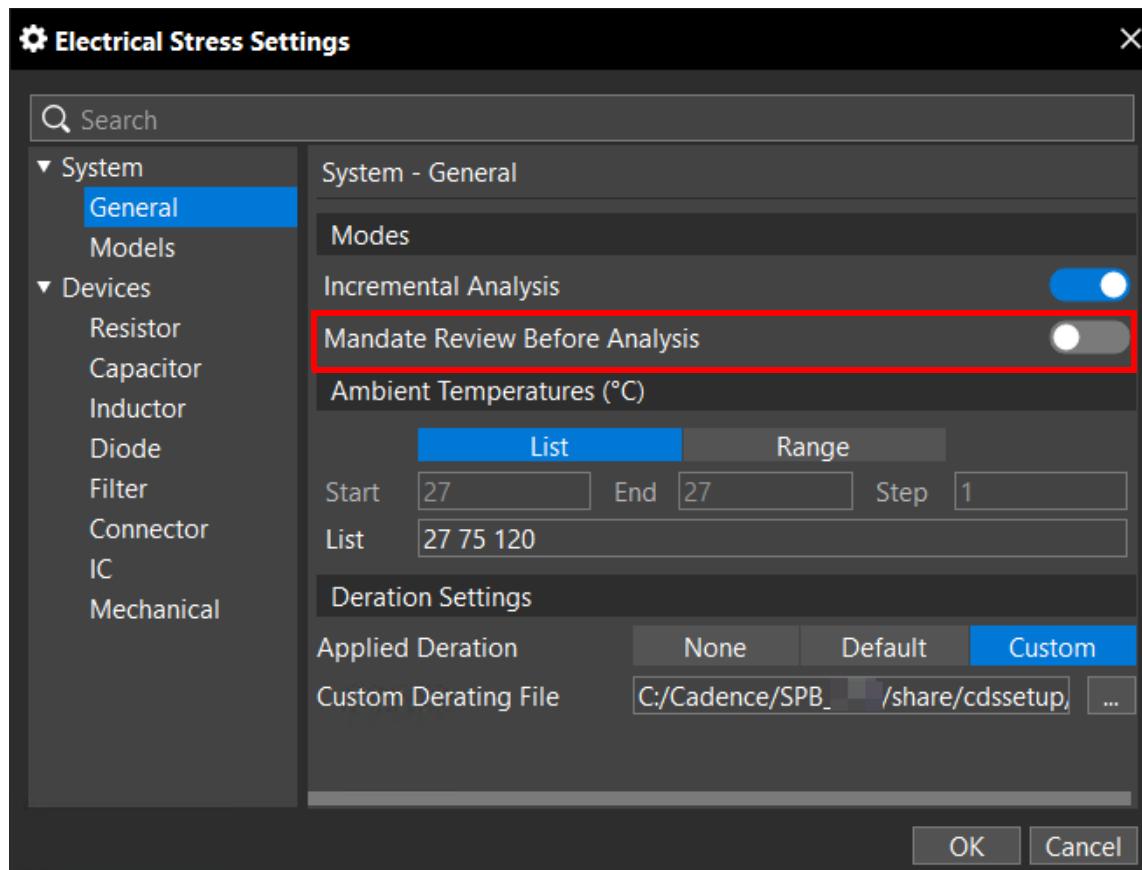
You can choose to manually review and sign off device parameter values before the analysis is run using the *Mandate Review Before Analysis* option in the *Electrical Stress Settings* dialog box. When selected, this option highlights devices that have one or more parameters with default values, and enforces a sign-off of the device before proceeding with stress analysis. This option is available only with specific licenses.

To enforce a review of the device parameter values before analysis, do the following:

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

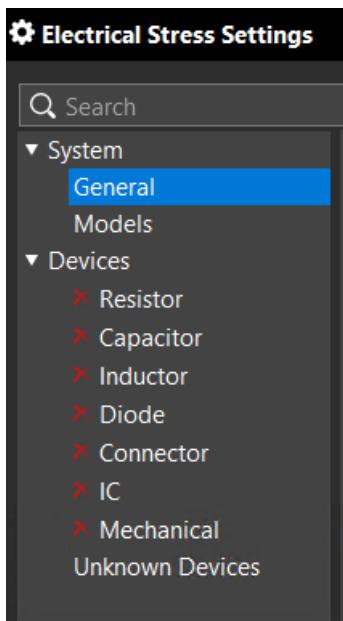
1. In the *System – General* tab of the *Electrical Stress Settings* dialog box, toggle the *Mandate Review Before Analysis* button.



Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

An X sign is displayed on some of the devices in the tree in the left pane. This indicates that these device categories need to be reviewed.



- Click the devices that require a parameter value review. For example, select the Capacitor device.

The screenshot shows the 'Electrical Stress Settings' window with the 'Capacitor' device selected in the tree view. The main panel displays the 'Devices - Capacitor' details. It includes an 'Instance Listing' table and a 'Parameter Settings' table. The 'Parameter Settings' table lists parameters like CV, CI, TKNEE, TJ, ESR, and PDM, many of which have red 'X' icons indicating they are not signed off. The 'Terminal Order Mapping' section shows mappings for Device Pin ID and Instance Pin Name.

Parameter	Value	Source
CV	16	X Design
CI	1.0	Default
TKNEE	85	Default
TJ	125	X Design
ESR	0.001	Default
PDM	0.1	Default

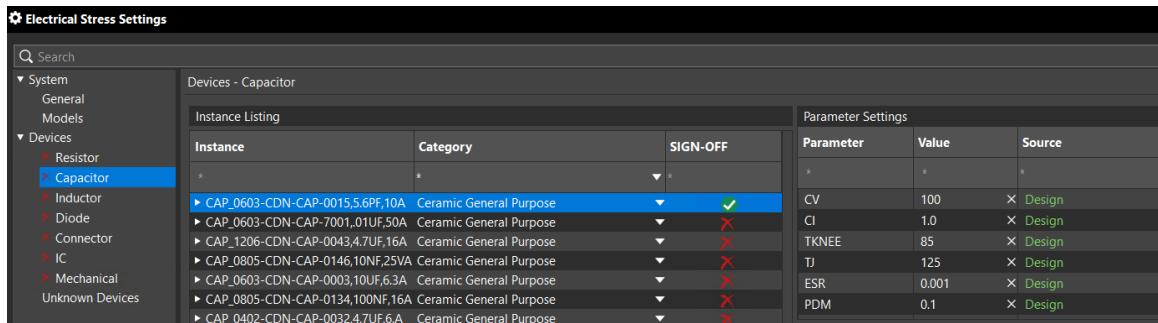
The cross sign indicates that those parts are not signed off because one or more parameters are using default values.

- To sign off a device, double-click the cross sign in the SIGN-OFF column.

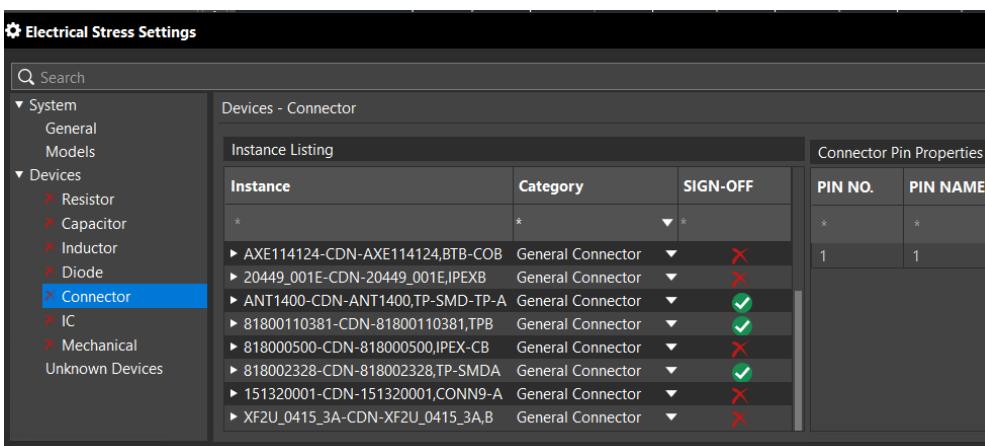
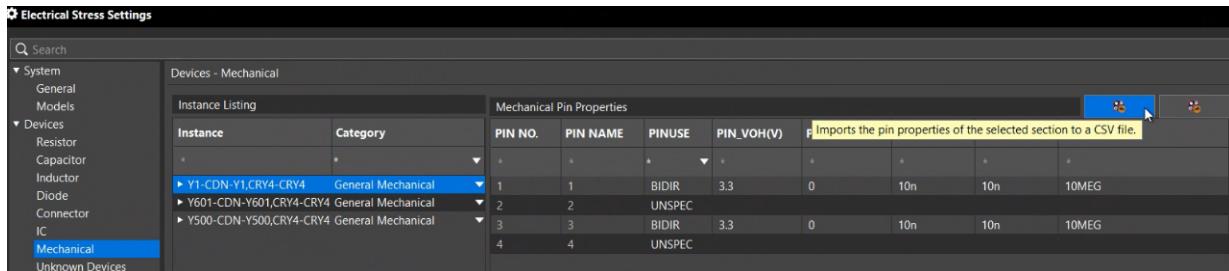
Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

The sign is changed to a check mark and the default values are saved for the design. The device is now explicitly signed off. A check mark indicates that all the parameters are being read either from the library or from the design. In such cases, the devices are auto-signed off.



For ICs and connectors, importing the pin properties through a .CSV file automatically signs off the parts. You can import the properties using the icons on the top right.



- Click **OK** to close the *Electrical Stress Settings* dialog box.

Related Topics

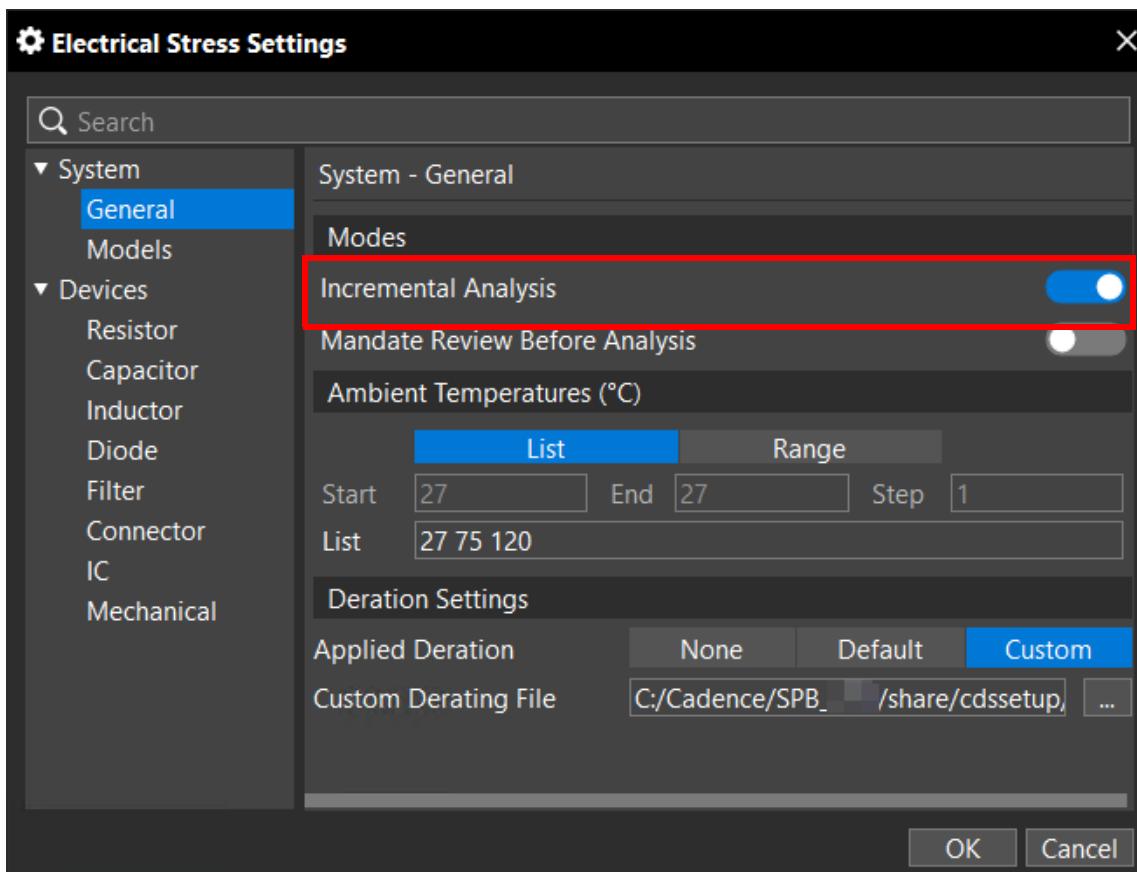
- [Device Identification and Pin Detection](#)
- [Modes of Analysis](#)

Running an Incremental Analysis

To save time and improve performance, you can choose to simulate only the subcircuits that have changed since the last analysis instead of the entire design. When this option is selected, subcircuits that are unchanged since the last run are fetched from the last analysis run. This option is available only with specific licenses.

To run an incremental analysis, do the following:

1. In the *System – General* tab of the *Electrical Stress Settings* dialog box, toggle the *Incremental Analysis* button.



2. Click **OK**.

Related Topics

- [Rule Severity at Site Level](#)
- [Waiving Checks from Report Dashboard](#)

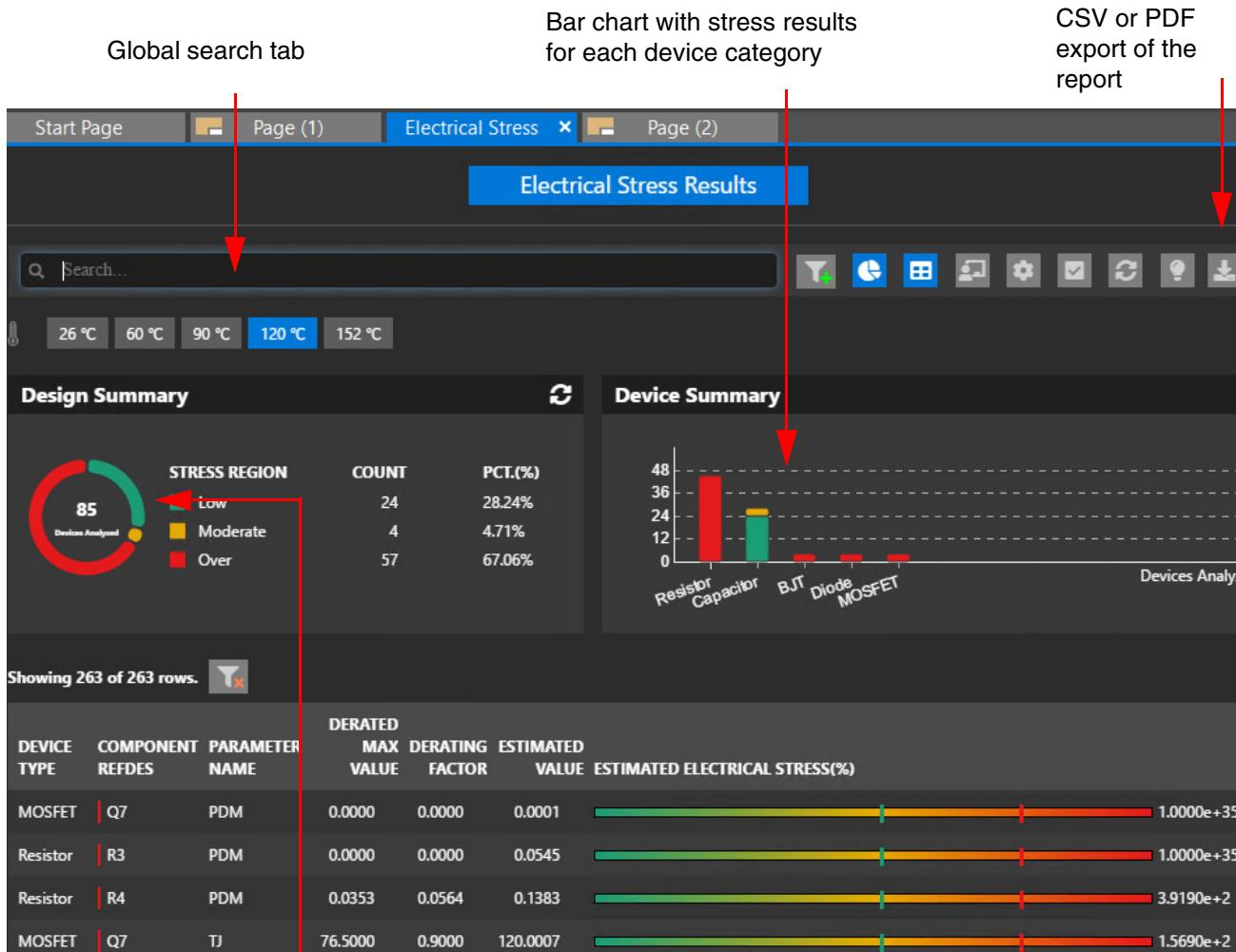
Analyzing Electrical Stress

- To analyze the electrical stress of a design, select *Design Integrity — Analyze Electrical Stress*.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

Design Integrity analyzes the design and presents the result in an easy-to-read report.



Stress results summary. You can reset the parameters applied to the chart.

Examining Electrical Stress Results

You can view the electrical stress report after you run the analysis and view the results of previously run analysis from the project explorer window. You can also toggle between a tabular and graphical display, filter, and export the results.

- [Viewing Electrical Stress Report](#)
- [Sharing Electrical Stress Analysis Results](#)

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

■ Searching for Components and Parameters in Electrical Stress Report

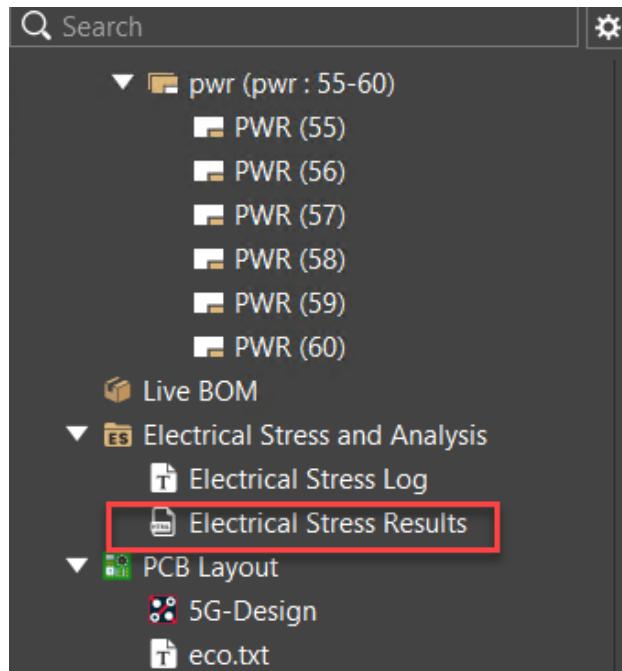
Viewing Electrical Stress Report

The electrical stress report categorizes components in three stress regions based on the stress analysis:

- Over: Includes overstressed components
- Moderate: Includes moderately stressed components
- Low: Includes safely stressed components

Note: The definition of stress can vary across organizations. You can define the stress level for individual device categories. For example, for each resistor, you can define a different stress level based on your company-specific derating standards. This can be done in the *Electrical Stress Settings* dialog box accessed from *Design Integrity - Configure - Electrical Stress Settings*.

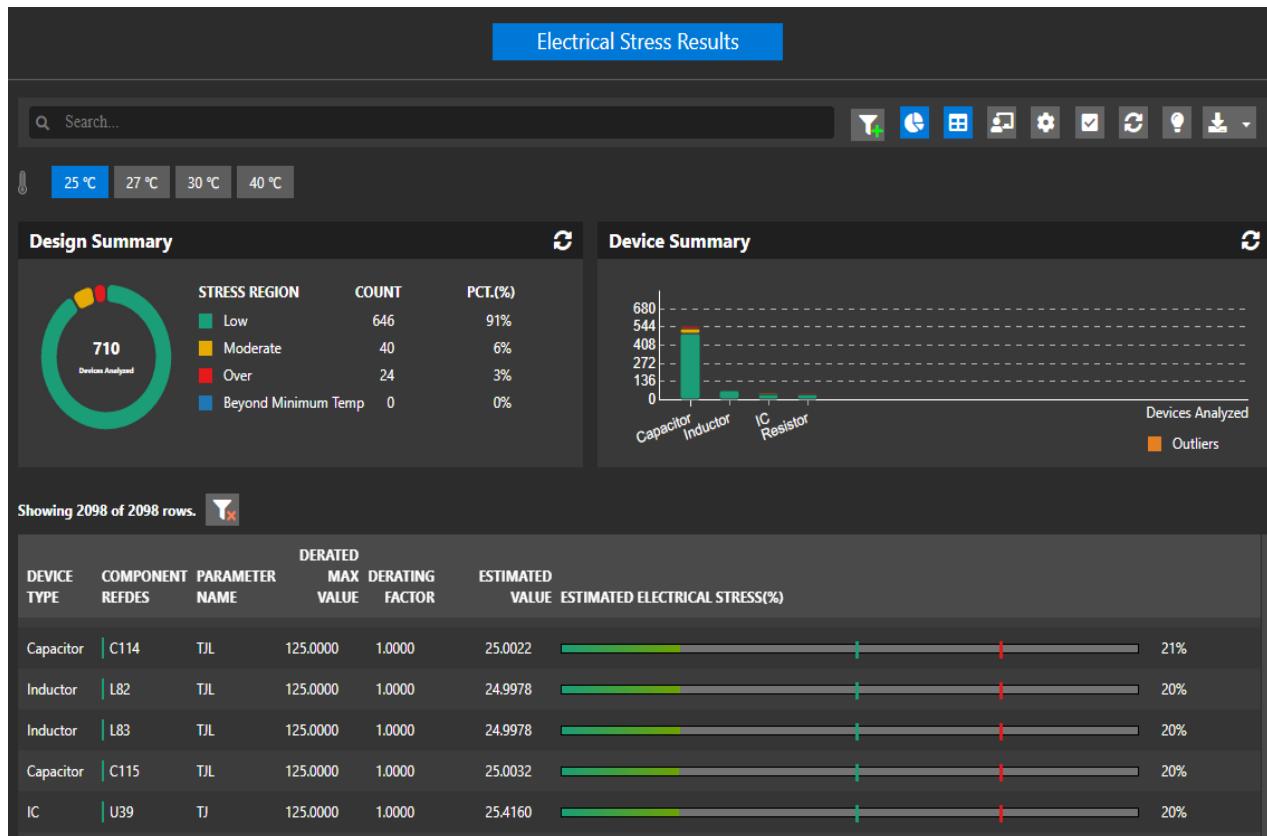
You can access the results of previously run analysis from the Project viewer. To view a report, double-click the analysis results HTML file in the Project viewer.



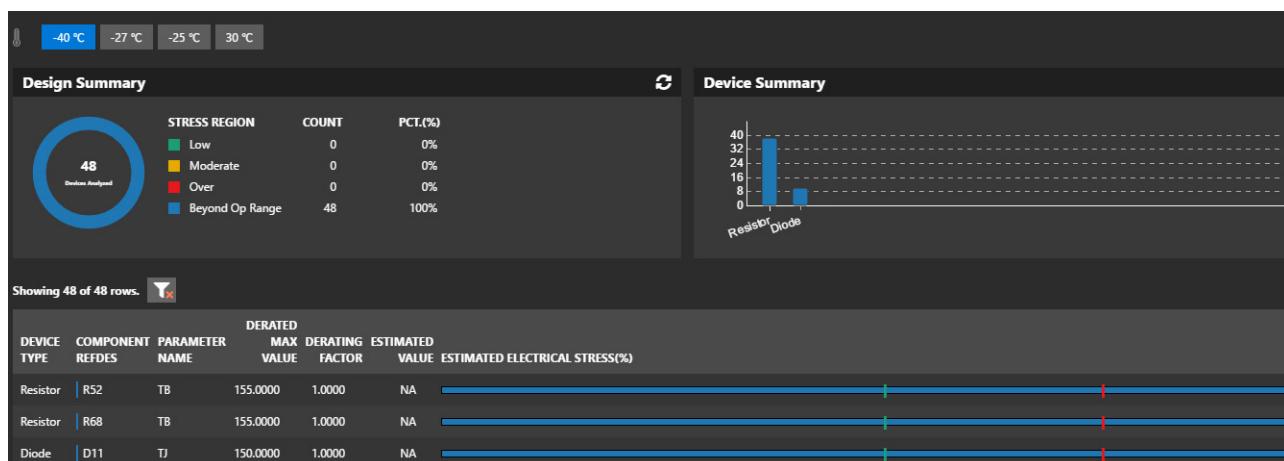
Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

The stress report is loaded and displayed to the right of the Project viewer.



When you run electrical stress analysis at an ambient temperature less than the minimum operating temperature (TMIN), the *Electrical Stress Results* dashboard displays a blue bar as illustrated in the following image:



Design Integrity and Analysis in Allegro X System Capture

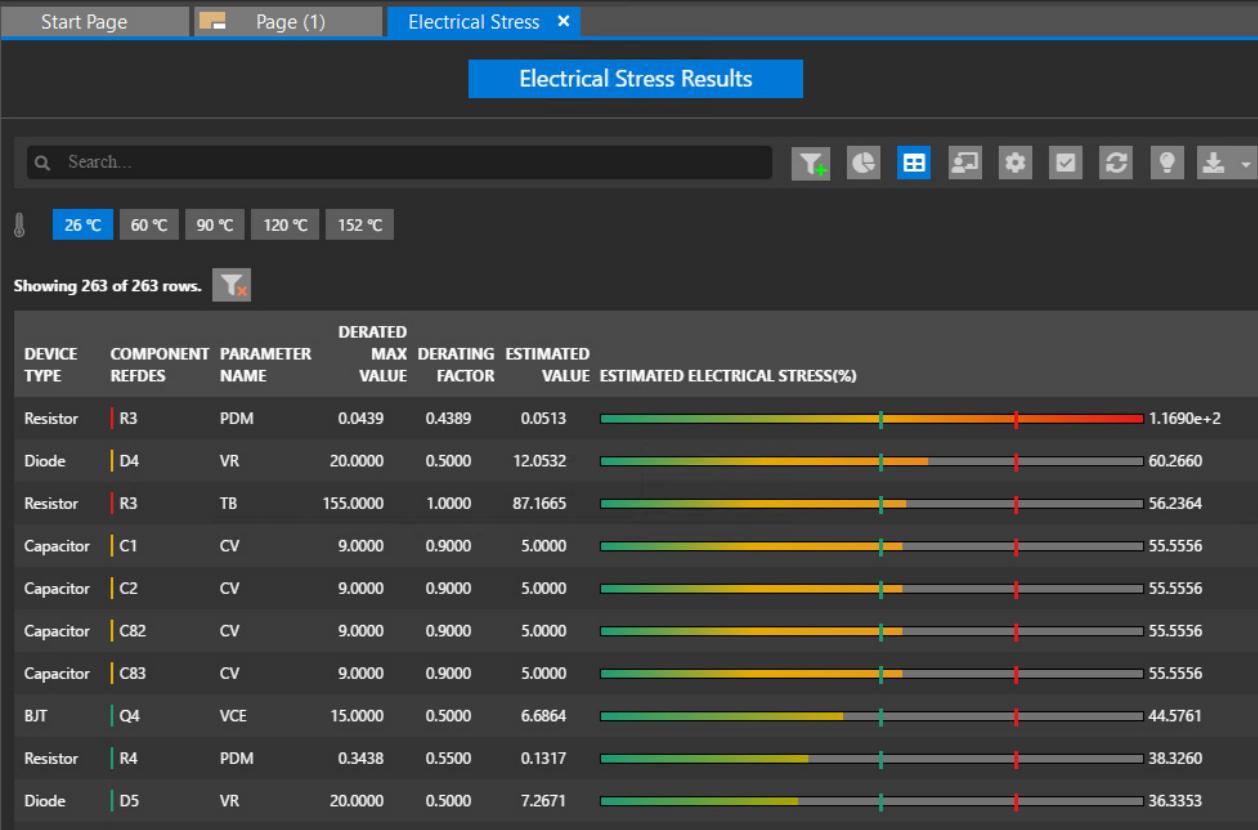
Electrical Stress Analysis

This indicates that the device is not included in the stress analysis because it is operating below TMIN.

Toggling Views in Electrical Stress Report

To toggle between the tabular and graphic view, do the following:

1. Click the *Toggle Charts Visibility* icon () to view a tabular display of the analysis results.
- A table is displayed.



The screenshot shows the 'Electrical Stress' tab in the Allegro X System Capture interface. The main title is 'Electrical Stress Results'. Below the title is a toolbar with various icons for search, filters, and export. A temperature selection bar shows values from 26 °C to 152 °C. The table displays 263 rows of data, with the first few rows shown below:

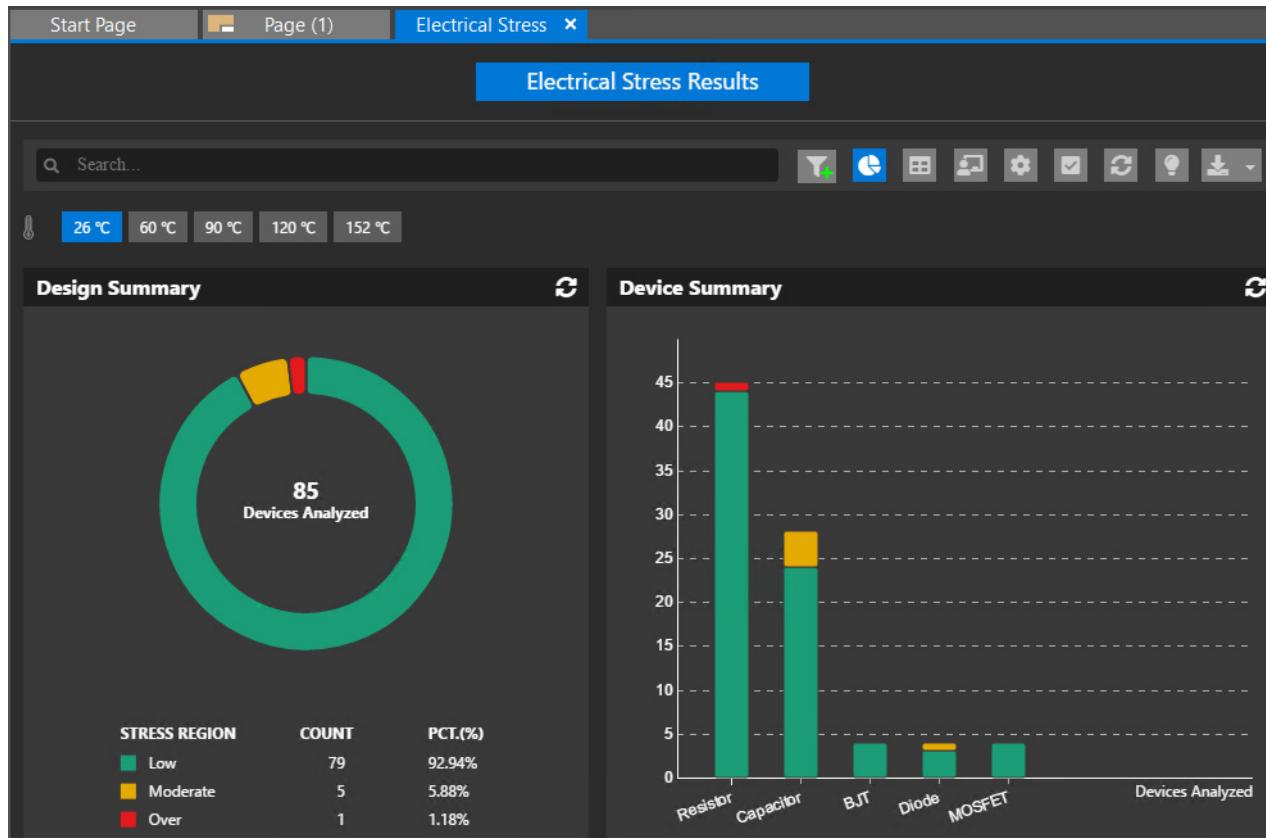
DEVICE TYPE	COMPONENT REFDES	PARAMETER NAME	DERATED			ESTIMATED ELECTRICAL STRESS(%)
			MAX VALUE	DERATING FACTOR	ESTIMATED VALUE	
Resistor	R3	PDM	0.0439	0.4389	0.0513	1.1690e+2
Diode	D4	VR	20.0000	0.5000	12.0532	60.2660
Resistor	R3	TB	155.0000	1.0000	87.1665	56.2364
Capacitor	C1	CV	9.0000	0.9000	5.0000	55.5556
Capacitor	C2	CV	9.0000	0.9000	5.0000	55.5556
Capacitor	C82	CV	9.0000	0.9000	5.0000	55.5556
Capacitor	C83	CV	9.0000	0.9000	5.0000	55.5556
BJT	Q4	VCE	15.0000	0.5000	6.6864	44.5761
Resistor	R4	PDM	0.3438	0.5500	0.1317	38.3260
Diode	D5	VR	20.0000	0.5000	7.2671	36.3353

2. Click the *Toggle Table Visibility* icon () to view a graphical display of the analysis results.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

A graphical view of the analysis results is displayed.



Sharing Electrical Stress Analysis Results

You can share the results of electrical stress analysis with other design team members so that they do not have to re-analyze the design.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

- To share the results, click the *Export Results to PDF/CSV* icon.



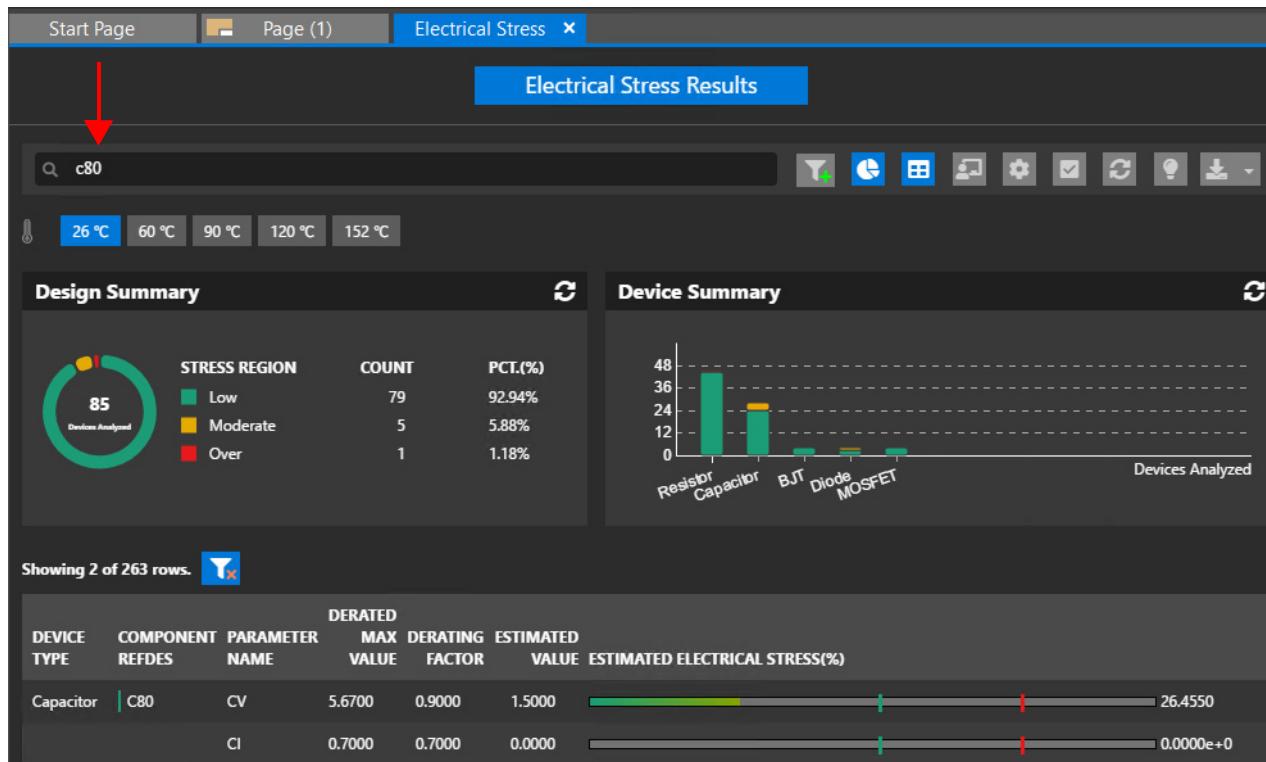
Searching for Components and Parameters in Electrical Stress Report

- To search for components and parameters, you can do the following:

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

- Filter the stress report by specifying names in the global search bar to display specific parameters or components. For example, specify C80 in the search bar to display the C80 component in the report.

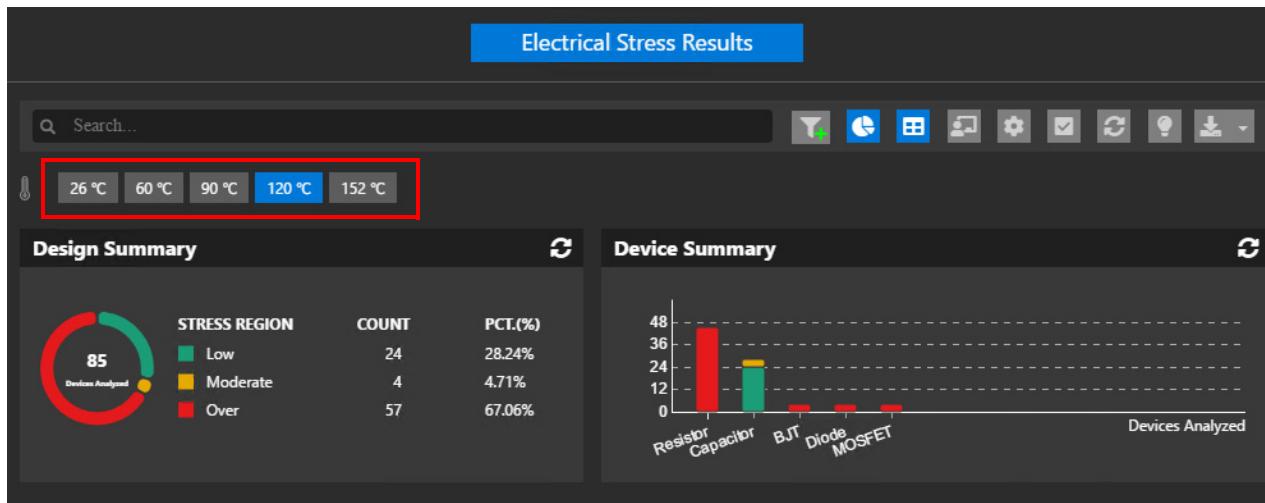
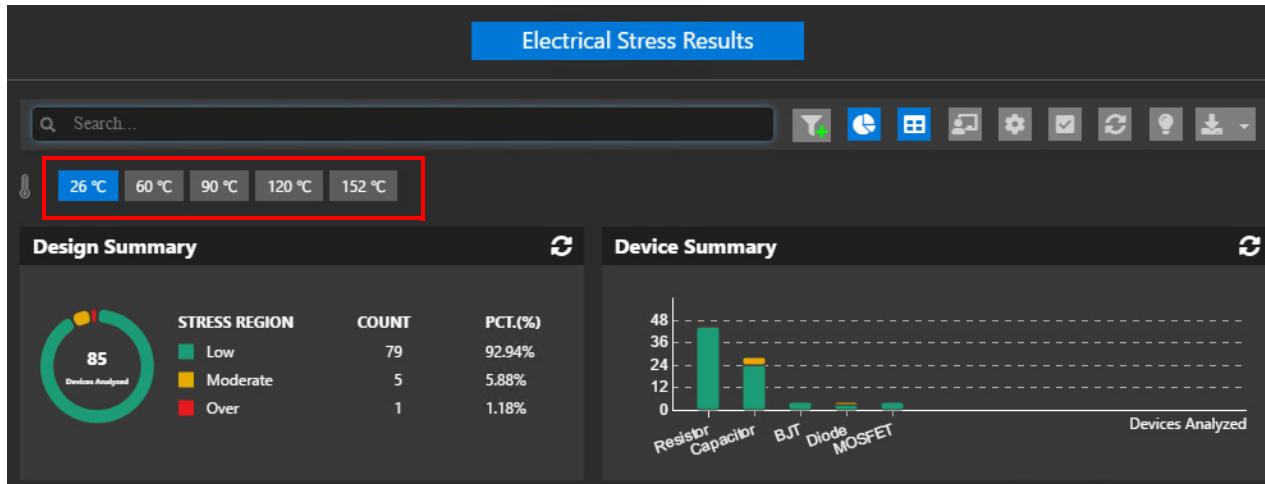


- Filter the stress report to search for specific parameters or components, such as PDM or capacitors, by clicking on the required column headers in the tabular list.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

- If multiple temperatures are specified for the analysis of a device, you can view the stress results analysis for each temperature, provided you have the required license for the temperature sweep feature.



Related Topics

- [Device Identification and Pin Detection](#)
- [Reference Designator Prefixes or Patterns to Recognize Devices](#)

Resolving Reported Errors After Electrical Stress Analysis

From the stress report, you can quickly navigate to the location where the error is flagged in the schematic and resolve the issue.

- To navigate to the location of an error, right-click the required component row in the stress report and select *Highlight Component*.

The screenshot shows the Allegro X System Capture software interface for Electrical Stress Analysis. The top navigation bar includes 'Start Page', 'Page (1)', and 'Electrical Stress'. The main window is titled 'Electrical Stress Results' and displays a search bar with 'c80', temperature settings (26 °C, 60 °C, 90 °C, 120 °C, 152 °C), and two summary sections: 'Design Summary' and 'Device Summary'.

Design Summary: Shows a circular progress bar with 85 devices analyzed, a stress region distribution table, and a bar chart of device types vs. stress level.

STRESS REGION	COUNT	PCT. (%)
Low	24	28.24%
Moderate	4	4.71%
Over	57	67.06%

Device Summary: A bar chart showing the count of devices for different component types: Resistor, Capacitor, BJT, Diode, and MOSFET. The Y-axis ranges from 0 to 48.

Component Type	Count
Resistor	48
Capacitor	24
BJT	4
Diode	4
MOSFET	4

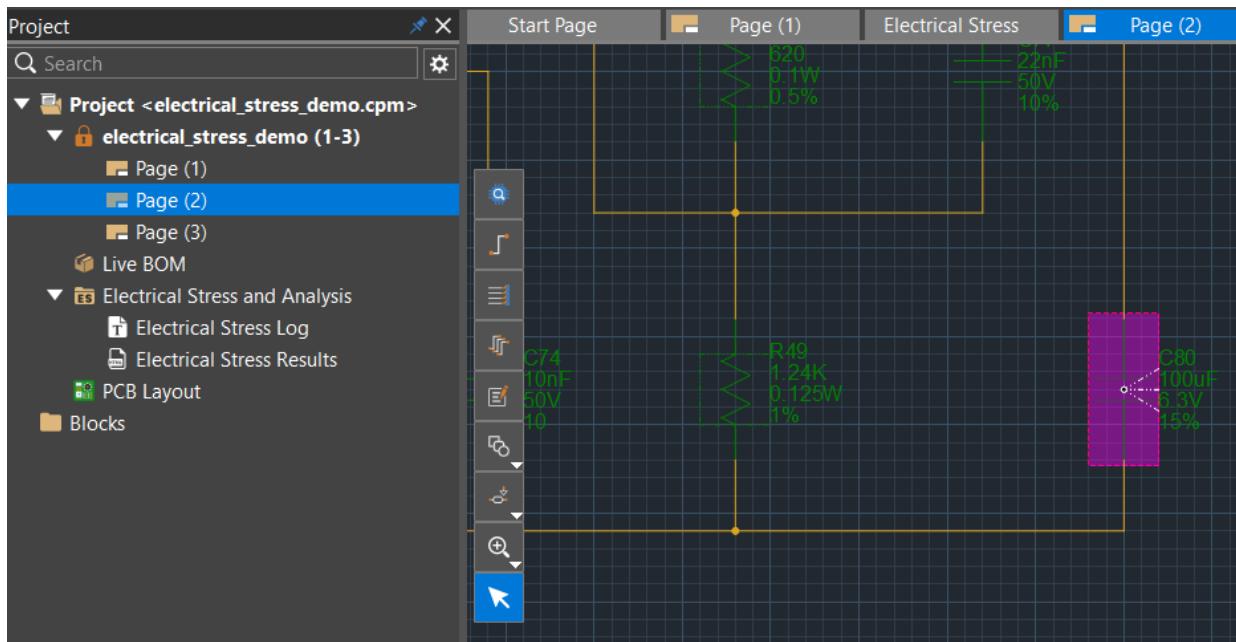
Context Menu: A context menu is open over a table row for a capacitor component. It includes options: 'Highlight Component', 'Dehighlight Component', 'Highlight Subcircuit', 'Dehighlight Subcircuit', and 'Electrical Stress Settings'.

DEVICE TYPE	COMPONENT REFDES	PARAMETER NAME	DERATED MAX VALUE	DERATING FACTOR	ESTIMATED VALUE	ESTIMA
Capacitor	C80	CV	5.6700	0.9000	1.5000	
		CI	0.7000	0.7000	0.0000	

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

Design Integrity highlights the relevant component in the design.

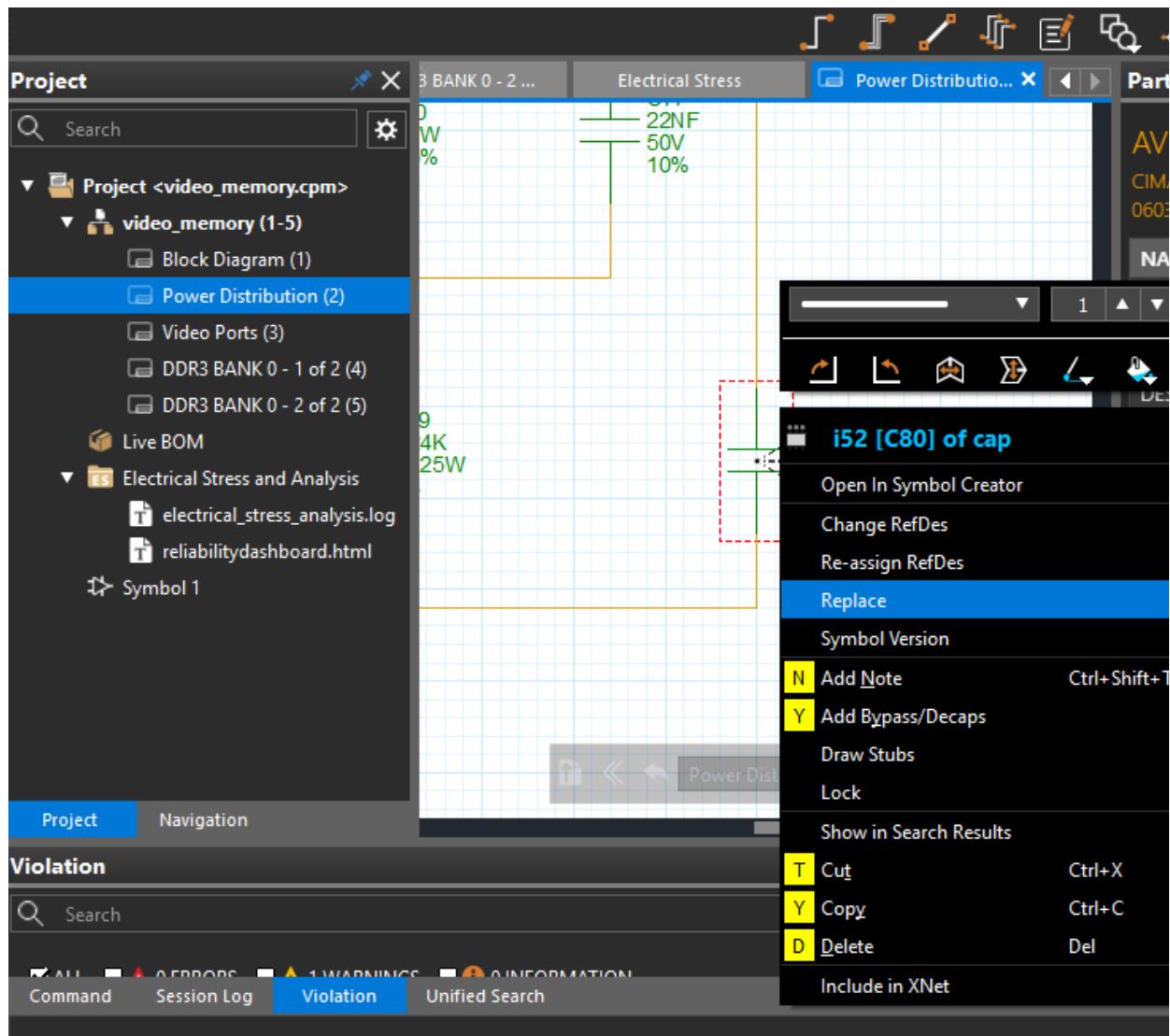


To resolve an issue reported by Design Integrity after an electrical stress analysis, do the following:

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

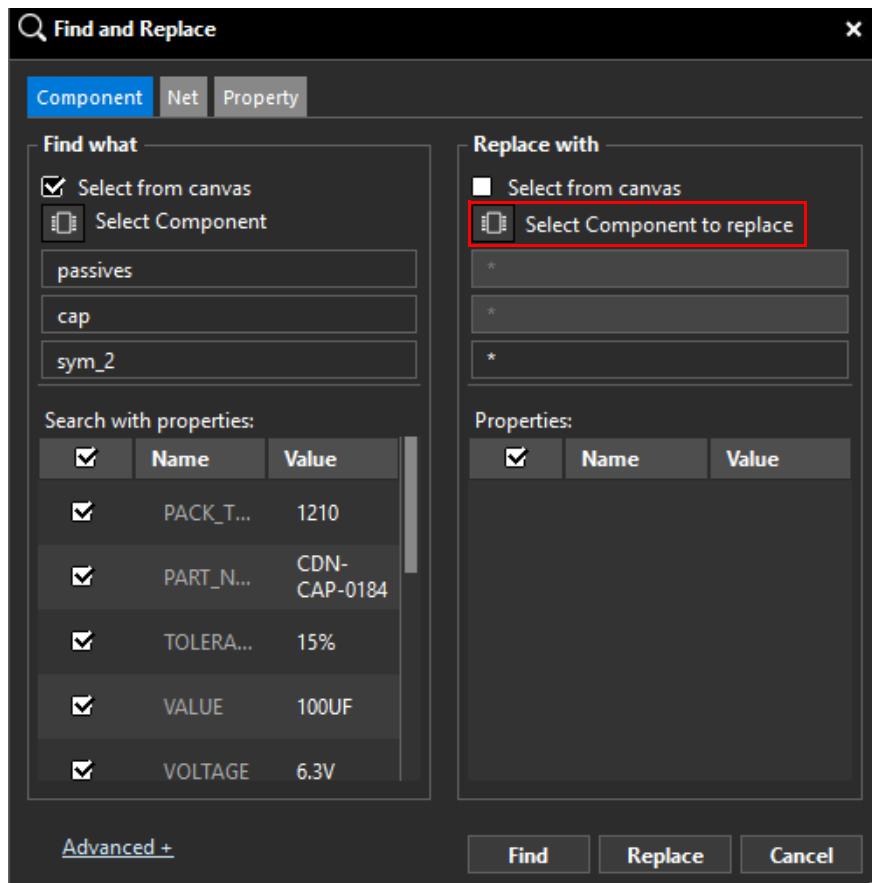
1. To replace a component that appears in the report, right-click the component in the design and select *Replace*. For example, replace C80 with a 4V part from the library.



Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

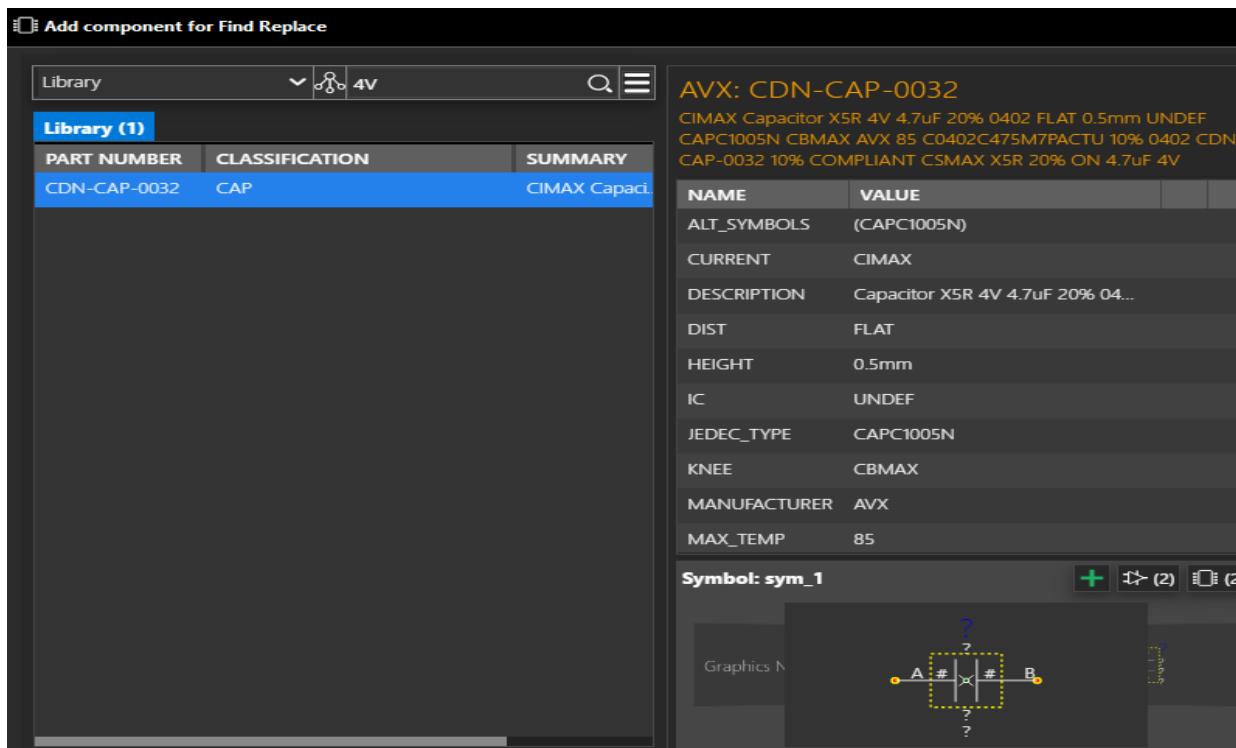
2. In the Find and Replace dialog that is displayed, click the *Select component to replace* icon.



Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

- In the Add component for Find Replace dialog, search for the required part. For example, search for a 4V part.

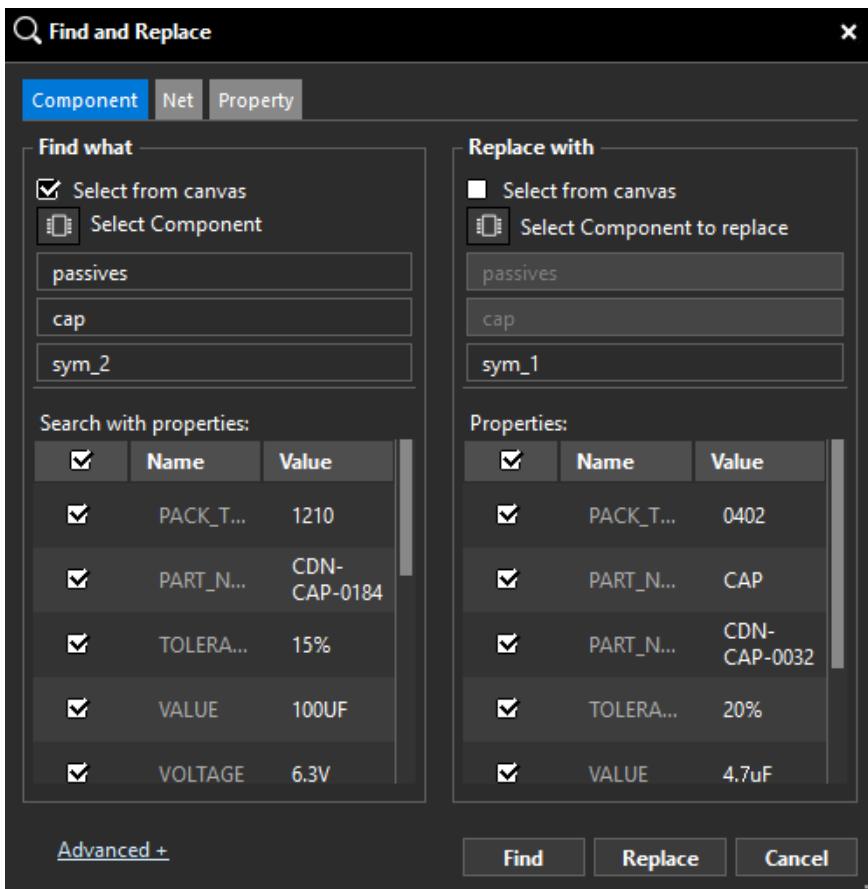


- Double-click the required part in the library.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

The selected part is displayed in the Find and Replace right portion of the form for comparison with the existing part.

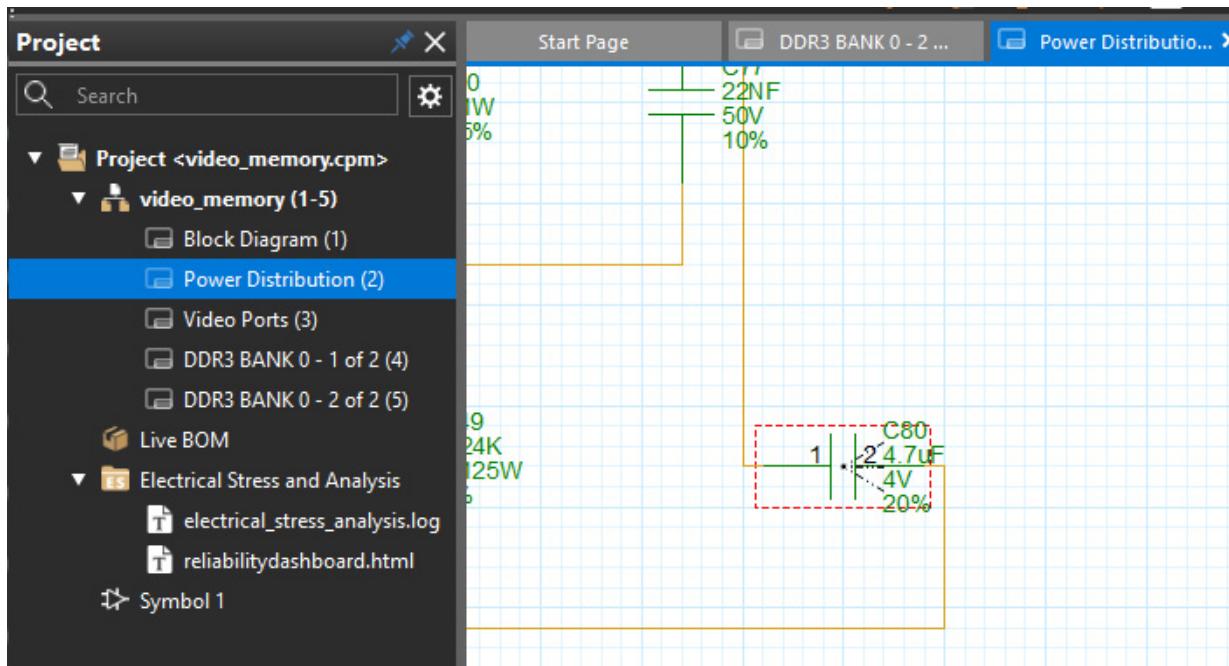


5. Click *Replace*.

Design Integrity and Analysis in Allegro X System Capture

Electrical Stress Analysis

You are prompted that the changes cannot be undone. For example, if you continue with the replacement, the original 6.3v part is replaced with the selected 4V part.



6. Choose *Design Integrity — Analyze Electrical Stress* to re-run the stress analysis.

Related Topics

- [Configuring Electrical Stress Settings](#)
- [Analyzing Electrical Stress](#)

MTBF Analysis

Mean Time Between Failures (MTBF) is an attribute of durability that estimates the performance and safety of electrical, mechanical and electro-mechanical parts. Temperature, power dissipation, quality, and stress are some factors that can affect the MTBF of a device.

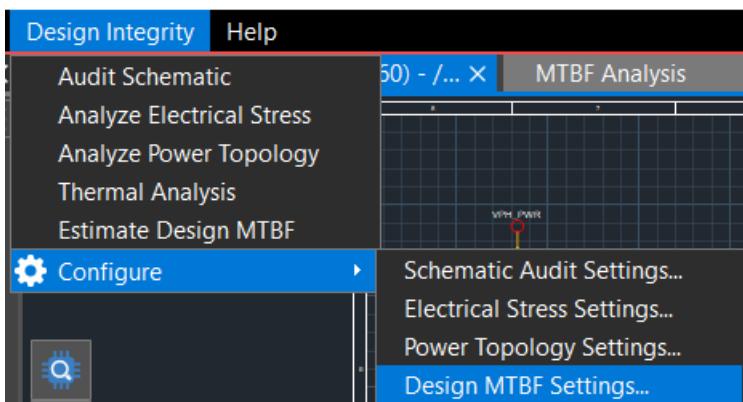
The Design Integrity solution of Allegro X System Capture provides an efficient way to analyze the MTBF of complex PCB designs.

Configuring Design MTBF Settings

MTBF settings is classified into *System* settings and *Device* settings. If the property values are not defined for the devices, default values are used in MTBF analysis.

For more accurate MTBF analysis results, you can configure the MTBF settings in the following ways:

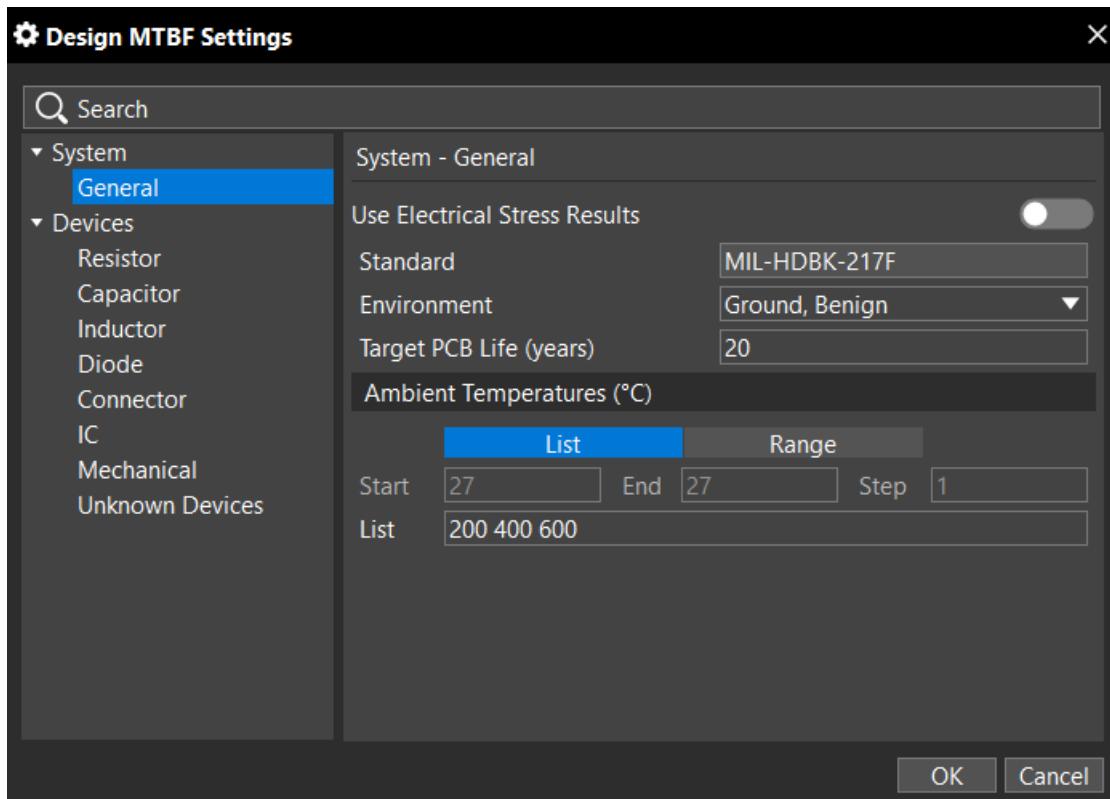
1. Access the *Design MTBF Settings* dialog box by choosing *Configure — Design MTBF Settings* from the *Design Integrity* menu.



Design Integrity and Analysis in Allegro X System Capture

MTBF Analysis

The *Design MTBF Settings* dialog box is displayed.



2. To calculate MTBF results based on the electrical stress data generated in the last run, enable the *Use Electrical Stress Results* option under *General* settings.

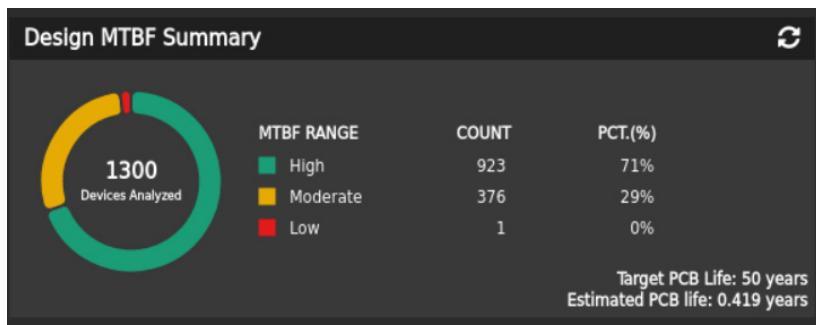
The *Standard* field shows MIL-HDBK 217F, a currently implemented reliability standard for design life estimation.

3. Select an environment based on which MTBF is calculated for a design. The default environment set for the MTBF calculation is *Ground, Benign*.
4. In the *Target PCB Life (years)* field, configure the life expectancy of the PCB design.
 - ❑ If the MTBF of a component is less than or equal to twice the target PCB life, the device is highly likely to fail and is categorized as *Low* in the *MTBF Results* dashboard.
 - ❑ If the MTBF of a component is over ten times the target PCB life, the device is highly likely to pass and is categorized as *High* in the *MTBF Results* dashboard.

Design Integrity and Analysis in Allegro X System Capture

MTBF Analysis

- The remaining devices come under the *Moderate* category.



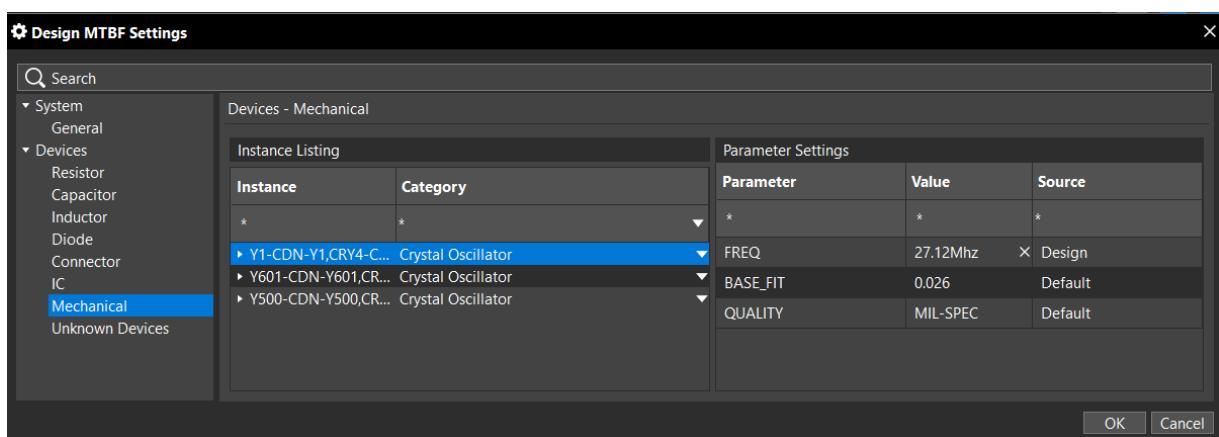
Note: The MTBF failure or success is computed based on the actual life compared to the target life.

- If you don't want to use the same temperatures used for Electrical Stress Analysis, configure either a list or a range of *Ambient Temperatures* for MTBF analysis.

Under *Device* settings, each device has different operating parameters for which the default values are defined. The MTBF parameters are listed under the *Parameter Settings* table of the *Design MTBF Settings* dialog box.

- Select a device, such as a capacitor or a diode, and modify the value if required.

The *Source* of the parameters can be *Default*, *Design*, or *Stress*.



- Click *OK* to close the *Design MTBF Settings* dialog box.

Related Topics

- [Property Alias](#)

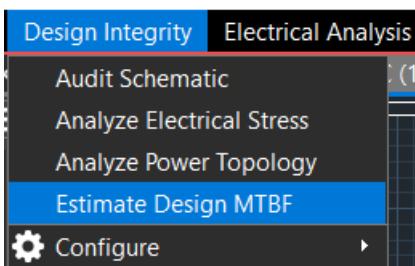
Running MTBF Analysis

You can run MTBF analysis on a design in the following ways:

- If *Use Electrical Stress Results* is enabled, MTBF analysis is run based on the settings used for the last electrical stress analysis.
- If *Use Electrical Stress Results* is disabled, ambient temperatures configured from *Design MTBF Settings* will be used.

To run MTBF analysis using data configured from *Design MTBF Settings*, do the following:

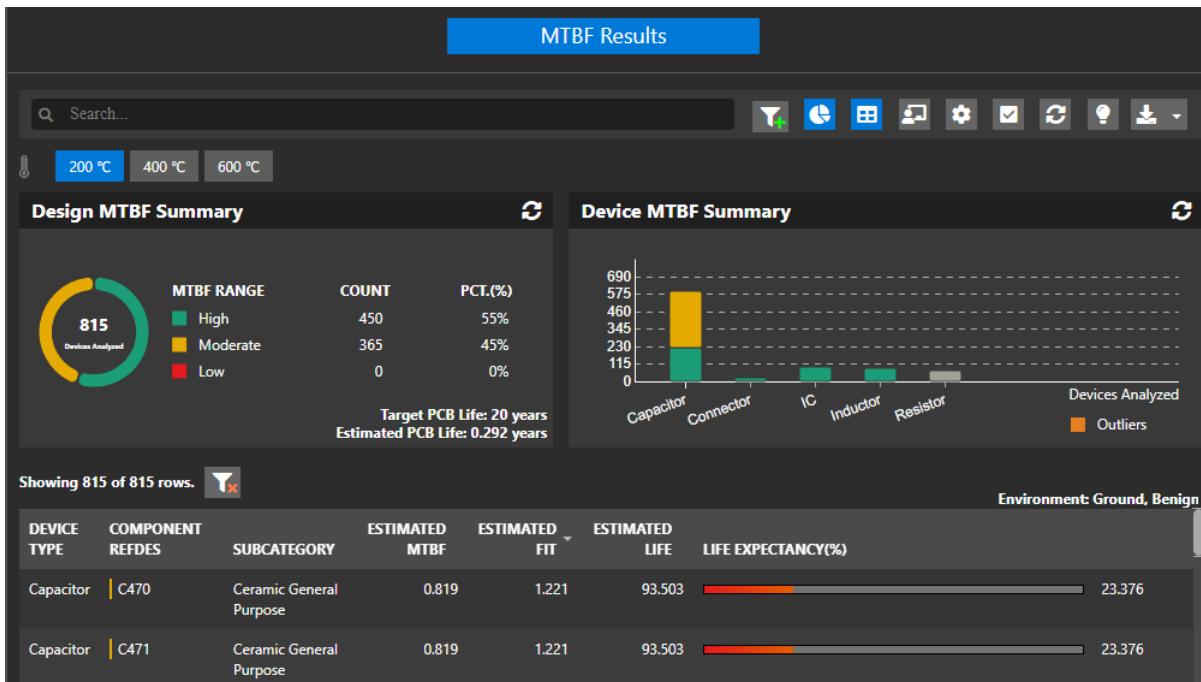
1. Launch Allegro X System Capture with any of the following licenses:
 - Allegro X Designer
 - Allegro X Designer Plus
 - Allegro X Venture
2. Open a design in Allegro X System Capture.
3. Click *Estimate Design MTBF* in the *Design Integrity* menu to run the analysis.



Design Integrity and Analysis in Allegro X System Capture

MTBF Analysis

The analysis result is displayed in the *MTBF Results* dashboard.



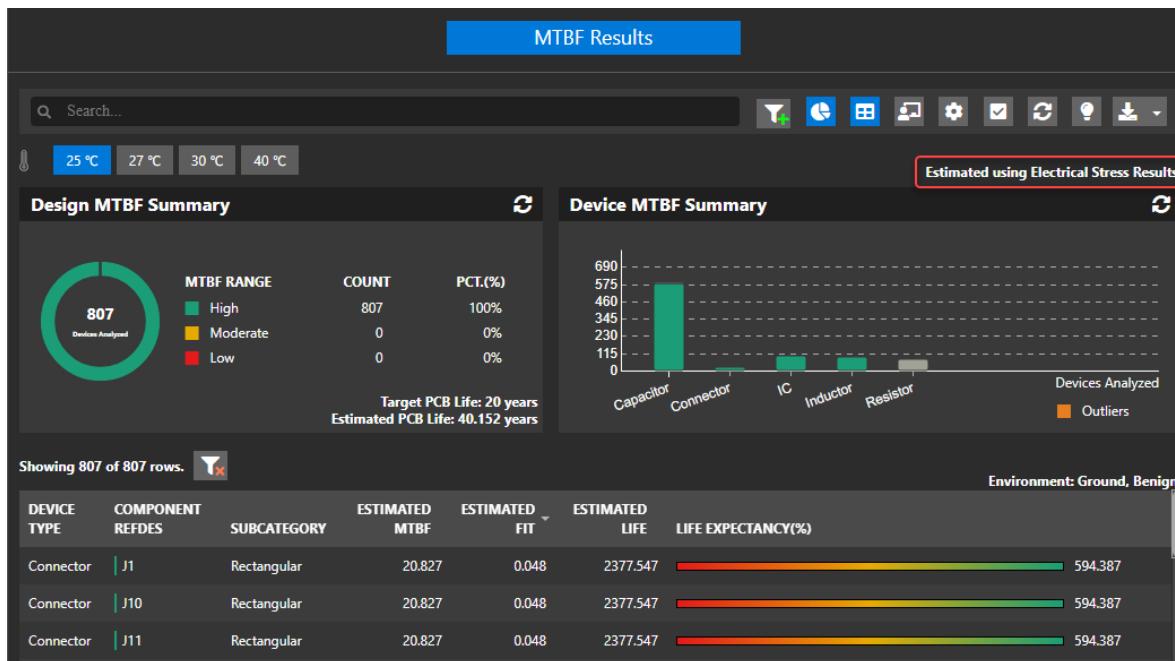
To calculate MTBF results based on the electrical stress data generated in the last run, do the following:

1. In the *Design Integrity* menu, select *Configure — Design MTBF Settings*.
2. In the *Design MTBF Settings* dialog box, under *General* settings, enable the *Use Electrical Stress Results* option.
3. Click *OK* and re-run the MTBF analysis on the design.

Design Integrity and Analysis in Allegro X System Capture

MTBF Analysis

The MTBF results are displayed in the dashboard with the text *Estimated using Electrical Stress Results*.



MTBF Results Calculation

The MTBF dashboard generates data based on the *Use Electrical Stress Results* option configured from the *Design MTBF Settings* dialog box.

The MTBF analysis results are calculated either:

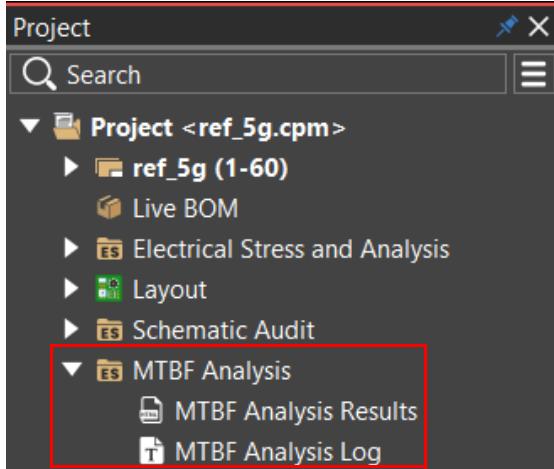
- Using data configured from *Design MTBF Settings*
- Using electrical stress result data generated from the last run

Note: The currently implemented standard does not support MTBF analysis for negative temperature values.

MTBF analysis results and logs can also be accessed from the *Project Explorer* panel.

Design Integrity and Analysis in Allegro X System Capture

MTBF Analysis

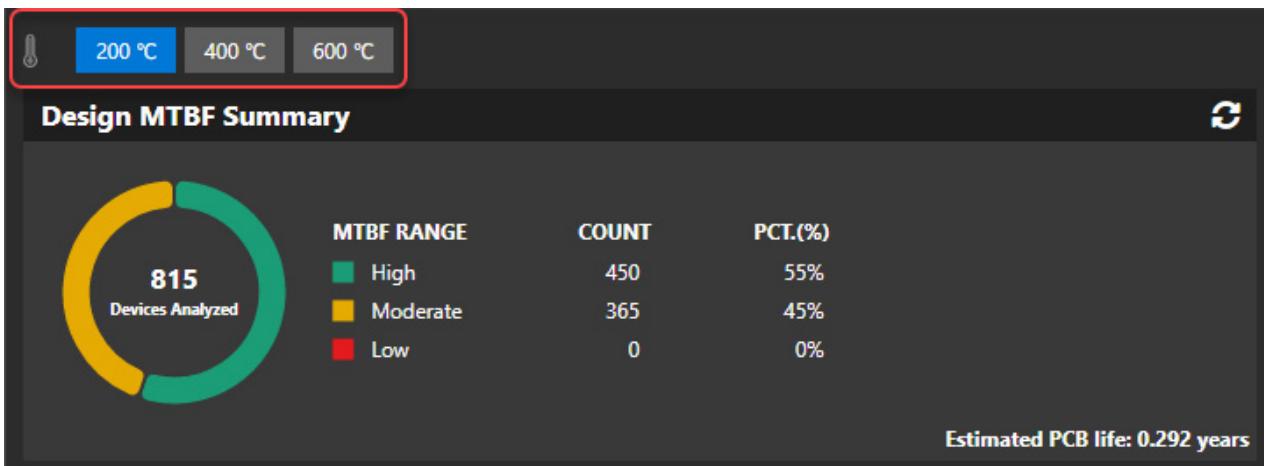


MTBF dashboard displays the results of the mean time between failures of the design. It includes the following:

- Temperature Tabs
- Search and Toolbar Options

Temperature Tabs

The ambient temperatures used for MTBF calculation are listed at the top left corner of the *MTBF Results* dashboard. You can switch between the tabs to check the results generated at different temperatures.



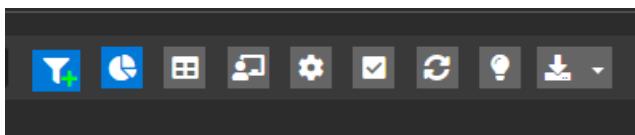
Design Integrity and Analysis in Allegro X System Capture

MTBF Analysis

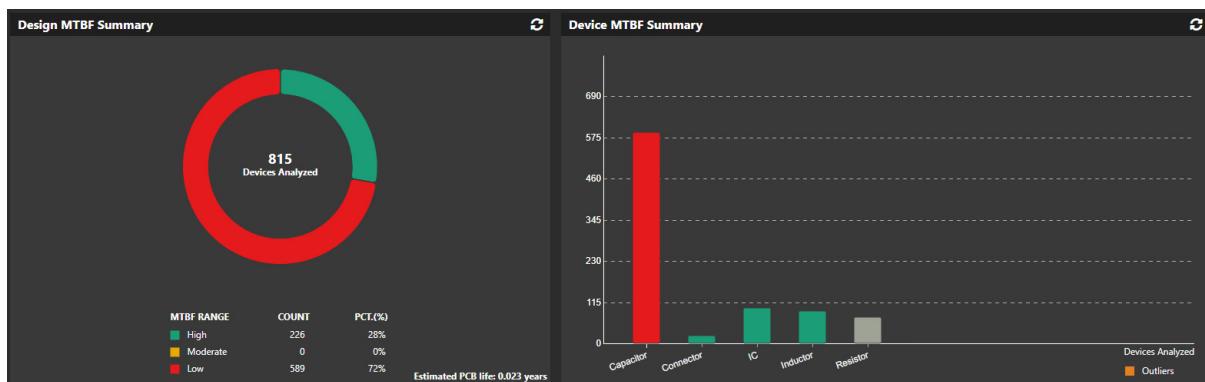
Search and Toolbar Options

The toolbar provides the following options on the MTBF dashboard:

- A filter option to search for any device type, device sub-category, and, so on.



- *Toggle Charts Visibility* to view the summary of your design in doughnut and bar chart form.



- *Toggle Table Visibility* to view the summary of your design in a tabular form.

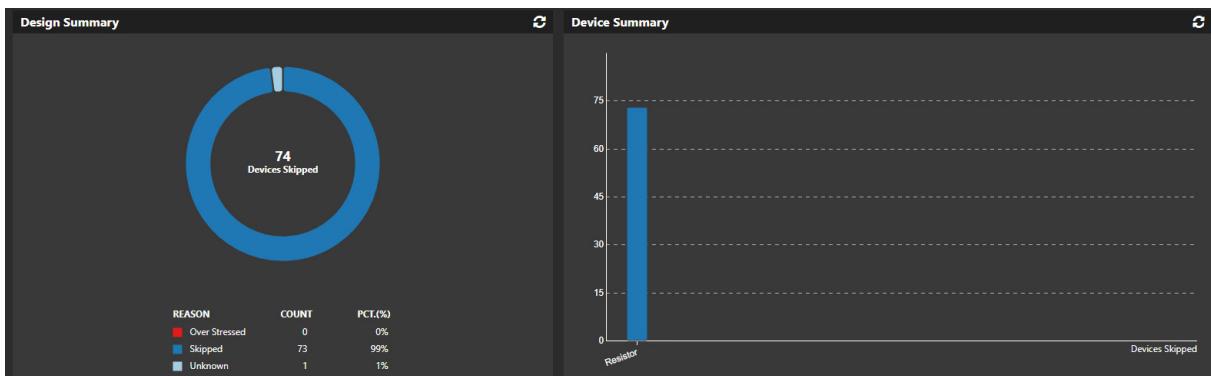
A table showing details for 815 components. The columns include: DEVICE TYPE, COMPONENT REFDES, SUBCATEGORY, ESTIMATED MTBF, ESTIMATED FIT, ESTIMATED LIFE, and LIFE EXPECTANCY(%). All entries for Capacitors have an estimated MTBF of 0.064, an estimated fit of 15.666, and an estimated life of 7.287 years.

DEVICE TYPE	COMPONENT REFDES	SUBCATEGORY	ESTIMATED MTBF	ESTIMATED FIT	ESTIMATED LIFE	LIFE EXPECTANCY(%)
Capacitor	C470	Ceramic General Purpose	0.064	15.666	7.287	<div style="width: 100px; height: 10px; background-color: red;"></div>
Capacitor	C471	Ceramic General Purpose	0.064	15.666	7.287	<div style="width: 100px; height: 10px; background-color: red;"></div>
Capacitor	C472	Ceramic General Purpose	0.064	15.666	7.287	<div style="width: 100px; height: 10px; background-color: red;"></div>
Capacitor	C479	Ceramic General Purpose	0.064	15.666	7.287	<div style="width: 100px; height: 10px; background-color: red;"></div>

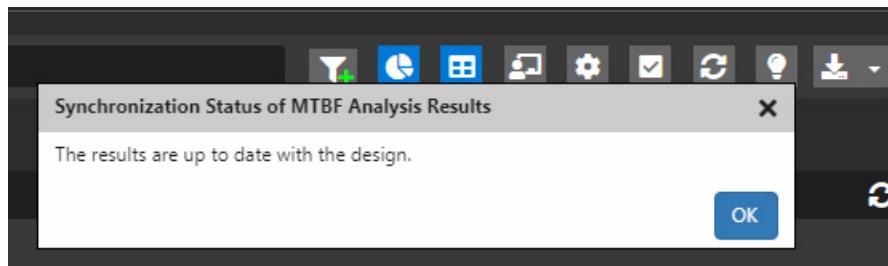
Design Integrity and Analysis in Allegro X System Capture

MTBF Analysis

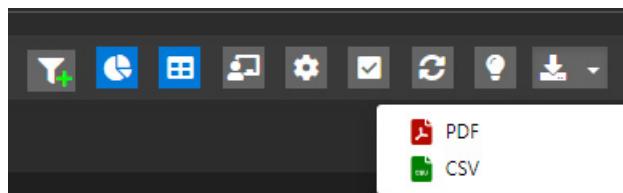
- *Toggle View* to view the summary of the successfully analyzed devices and the devices that are skipped.



- *MTBF Settings* option to launch *Design MTBF Settings* dialog box directly from the dashboard.
- Option to check whether the report is synchronized with the design data.



- Option to re-run MTBF analysis directly from the dashboard.
- Option to download MTBF reports as PDF or CSV file.



Related Topics

- [Configuring Design MTBF Settings](#)
- [Running MTBF Analysis](#)

Design Integrity and Analysis in Allegro X System Capture

MTBF Analysis

Resolving Reported Errors After MTBF Analysis

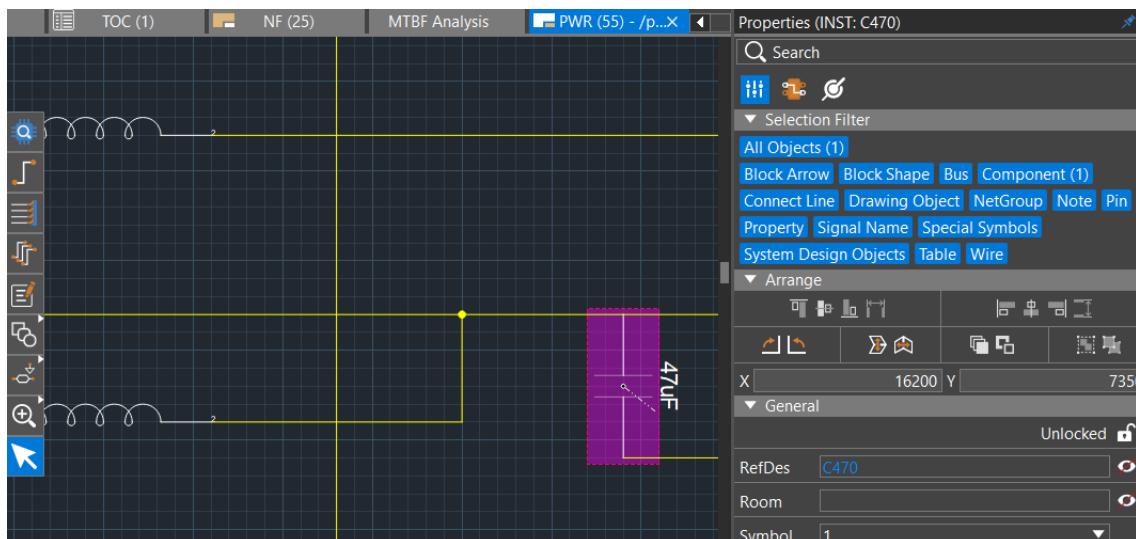
From the MTBF analysis report, you can navigate to the location where the error is flagged in the schematic and resolve the issue.

Do the following:

1. To navigate to the location of an error, right-click the required component row in the MTBF report and select *Highlight Component*.

DEVICE TYPE	COMPONENT REFDES	SUBCATEGORY	ESTIMATED MTBF	ESTIMATED FIT	ESTIMATED LIFE	LIFE EXPECTANCY(%)
Capacitor	C470	Ceramic General Purpose	0.819	1.221	93.503	23.376
Capacitor	C471	Ceramic General Purpose	0.819	1.221	93.503	23.376
Capacitor	C472	Ceramic General Purpose	0.819	1.221	93.503	23.376
Capacitor	C479	Ceramic General Purpose	0.819	1.221	93.503	23.376

The component is highlighted in the schematic.



2. To resolve an issue reported in MTBF analysis, modify the parameter values or change the component, as required.

After resolving the issue, re-run the MTBF analysis.

Design Integrity and Analysis in Allegro X System Capture

MTBF Analysis

Related Topics

- [Configuring Design MTBF Settings](#)
- [Running MTBF Analysis](#)

Design Integrity and Analysis in Allegro X System Capture

MTBF Analysis

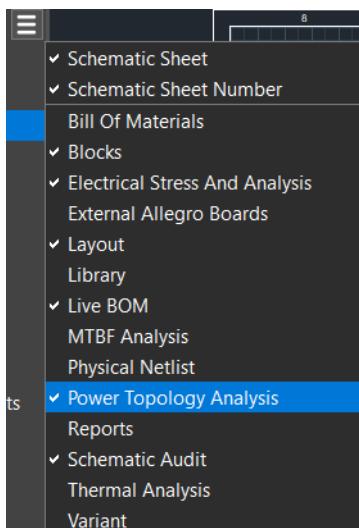
Power Topology Analysis

In Allegro X System Capture, Power Topology analysis sets up a power distribution network on the schematic that can be used to estimate DC power consumption by the components in a PCB design.

Power Topology is created at the schematic level which enables you to verify all the components in your design at an early stage of your project. You can run Power Topology analysis on the schematic data and validate the power distribution across the devices selected for the design.

You can analyze the results that are displayed on the dashboard and modify the design if required. After that, you can re-run the analysis to update the Power Topology and verify it again.

- To view the Power Topology node, select *Power Topology* in *Project Explorer Settings*.



Prerequisites for Power Topology Analysis

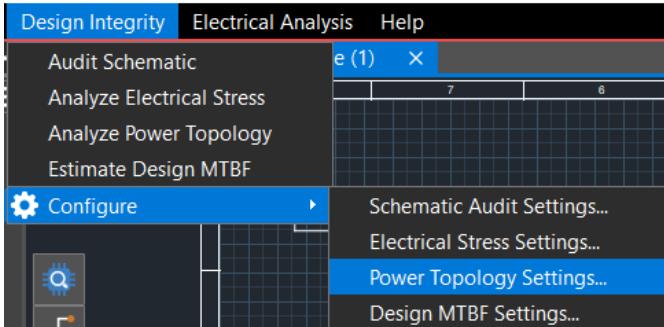
In Allegro X System Capture, Power Topology analysis is available with any of the following licenses:

- Allegro X Designer
- Allegro X Designer Plus
- Allegro X Venture

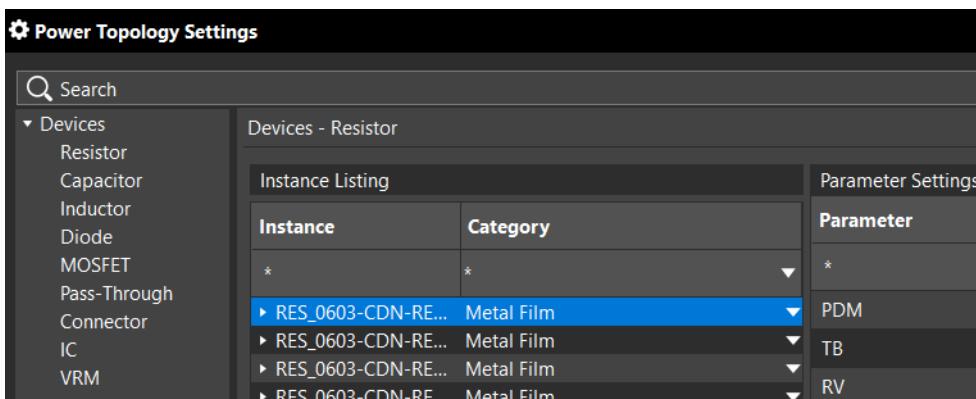
Configuring Power Topology Settings

Power Topology Settings consists of *Device Settings*. To configure the Power Topology settings, do the following:

1. Access the *Power Topology Settings* dialog box by choosing *Configure — Power Topology Settings* from the *Design Integrity* menu.



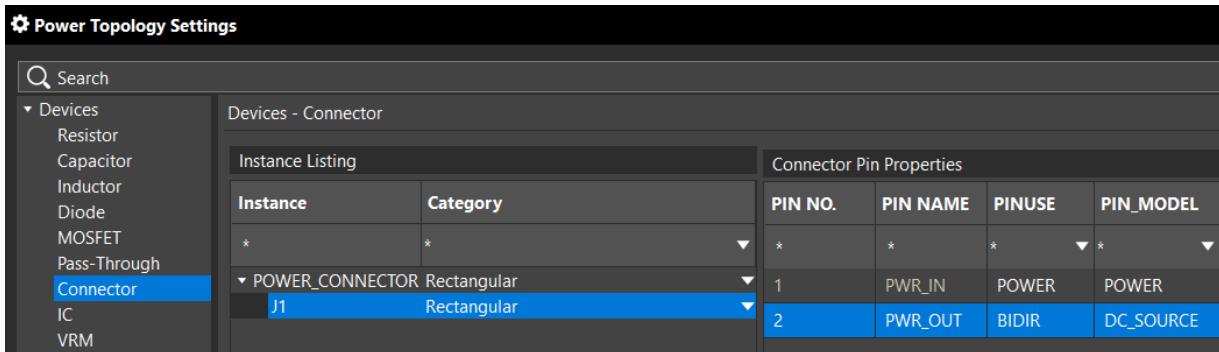
The *Power Topology Settings* dialog box is displayed. System Capture categorizes all the instances of your design under the *Devices* list.



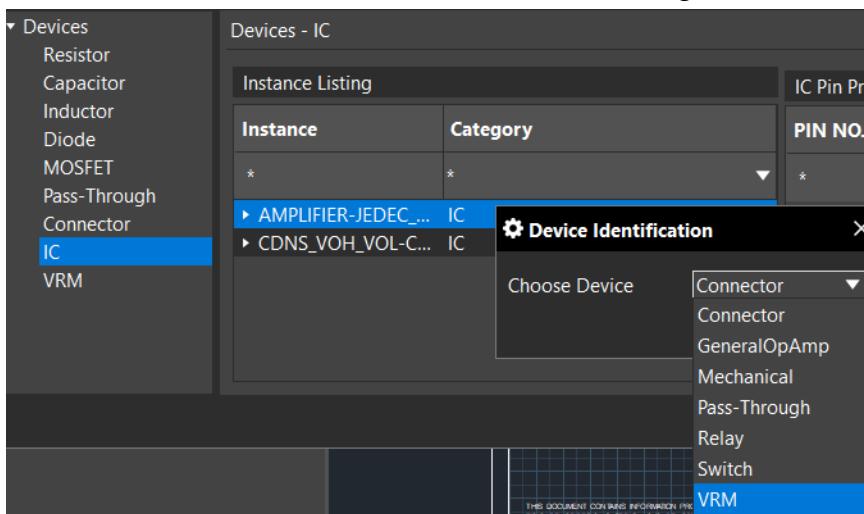
Design Integrity and Analysis in Allegro X System Capture

Power Topology Analysis

2. Identify a connector pin as a DC source. For this, set the PINUSE to OUT or BIDIR and set the PIN_MODEL to DC_SOURCE.



3. Identify a device, IC as VRM. To do this, right-click an instance of the selected IC and choose VRM in the *Device Identification* dialog box.



Design Integrity and Analysis in Allegro X System Capture

Power Topology Analysis

4. After identifying an IC as a VRM for a device instance, you need to configure VRM_IN and VRM_OUT pins under the device, VRM. Select the pin instance and change the PIN_MODEL to VRM_IN and VRM_OUT.

The screenshot shows two windows from the Allegro X System Capture interface. The left window is a sidebar titled 'Devices' with categories like Resistor, Capacitor, Inductor, Diode, MOSFET, Pass-Through, Connector, IC, and VRM. The 'VRM' category is selected and highlighted in blue. The right window is titled 'Devices - VRM' and contains an 'Instance Listing' table. It shows instances TPS76201DBVT, ST1L04, and AMPLIFIER-JEDEC_TYPE, all categorized as VRM. Below this is the 'VRM Pin Properties' dialog, which lists five pins (1-5) with columns for PIN NO., PIN NAME, PINUSE, and PIN_MODEL. The PIN_MODEL column for pin 1 (VIN) is set to 'VRM_IN' and for pin 5 (VOUT) is set to 'VRM OUT'. Both of these entries are highlighted with red boxes.

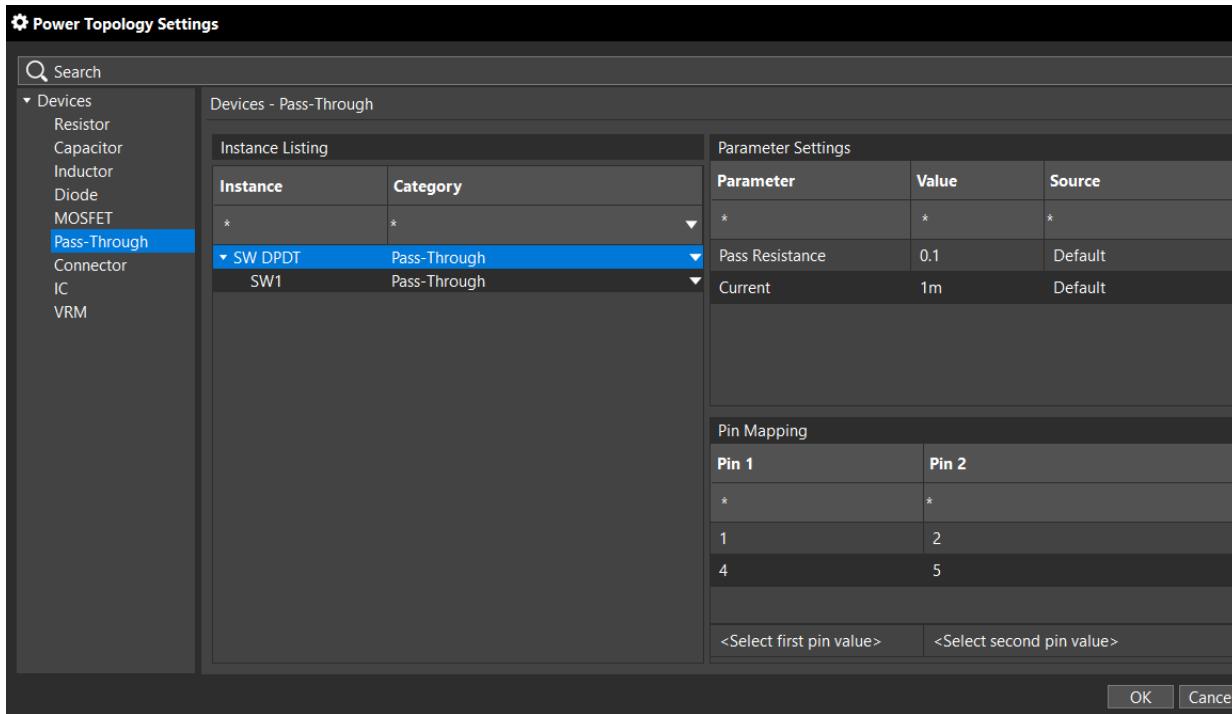
PIN NO.	PIN NAME	PINUSE	PIN_MODEL
*	*	*	*
1	VIN	IN	VRM_IN
2	NC	UNSPEC	SINK
3	GND	GROUND	GROUND
4	ADJ	IN	SINK
5	VOUT	OUT	VRM OUT

Note: To display the pins in the Power Topology, all the SINK pins of ICs must have their PINUSE set to POWER.

Design Integrity and Analysis in Allegro X System Capture

Power Topology Analysis

5. To identify a device as *Pass-through*, define the parameters and pin mapping of the instances.



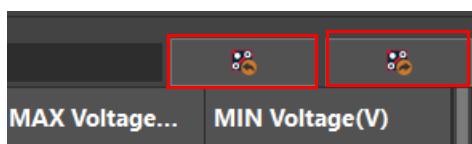
6. Click *OK* to close the *Power Topology Settings* dialog box.

Importing and Exporting Pin Properties

You can also import pin properties of the selected section into a CSV file. Also, the pin properties can be exported to a CSV file.

To import or export pin properties, do the following:

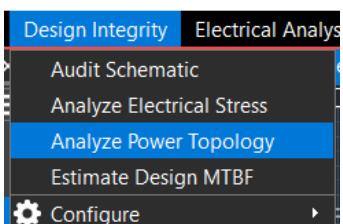
1. Select *Configure — Power Topology Settings* from the *Design Integrity* menu.
2. Choose *Power Topology Settings*.
3. In the *Power Topology Settings* dialog box, select a section and click the import or export icon on the top-right corner.



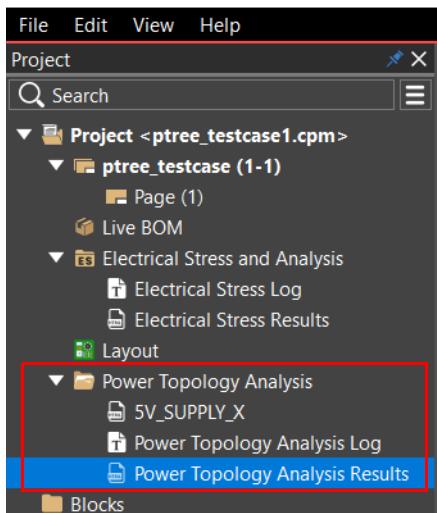
Running Power Topology Analysis

To run the Power Topology analysis using the data configure from *Power Topology Settings* dialog box, do the following:

1. Launch Allegro X System Capture with any of the following licenses:
 - Allegro X Designer
 - Allegro X Designer Plus
 - Allegro X Venture
2. Click *Analyze Power Topology* in the *Design Integrity* menu to run the analysis.



The analysis is running in the background. After the process is completed, the log and results are accessed from the Project Explorer panel.



Power Topology Results Analysis

Power Topology analysis results are displayed in the following ways:

- Analysis in a Graphical View

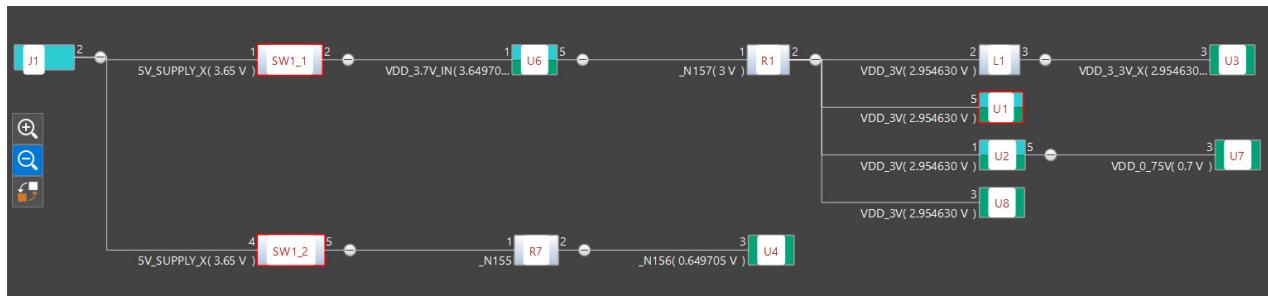
Design Integrity and Analysis in Allegro X System Capture

Power Topology Analysis

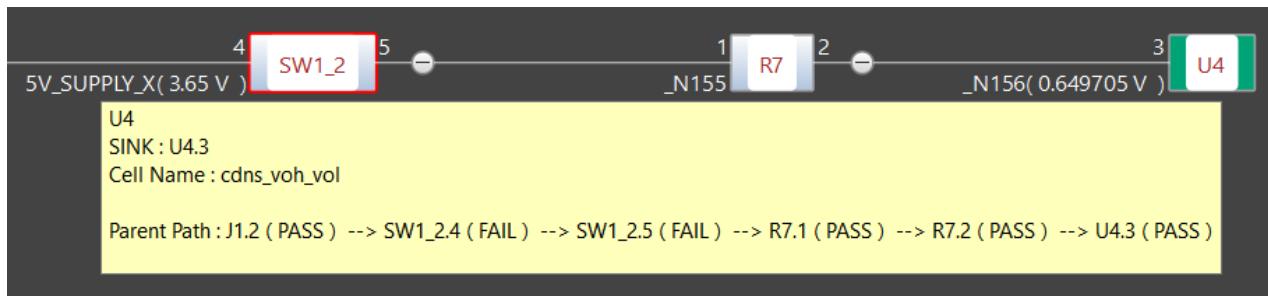
- Analysis in a Hierarchical View
- Dashboard Analysis

Graphical View

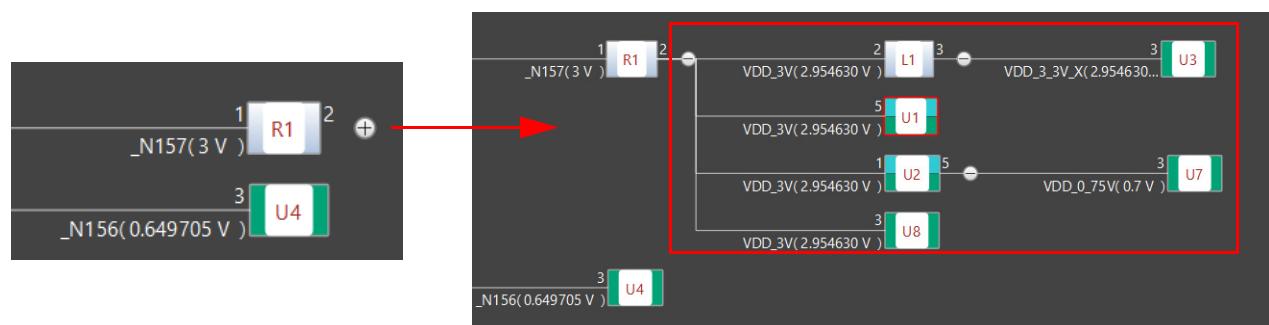
The graphical view of Power Topology shows a pictorial representation of DC Power flow through the entire circuit. You can view a tree of DC sources, VRMs, passive devices and ICs in a different color coding scheme.



Hover over a block to see the parent path of the power rail with a status, pass or fail for each component.



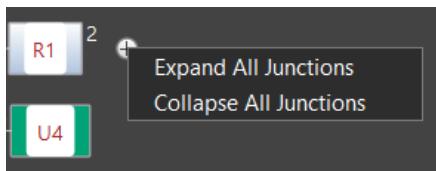
You can expand a node to see the components associated with a part.



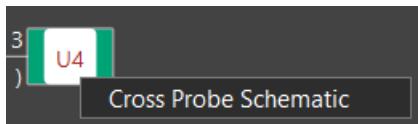
Design Integrity and Analysis in Allegro X System Capture

Power Topology Analysis

You can right-click a node to expand or collapse a power block.



- You can right-click a block and select *Cross Probe Schematic* to highlight a pin of the respective component in the schematic design.

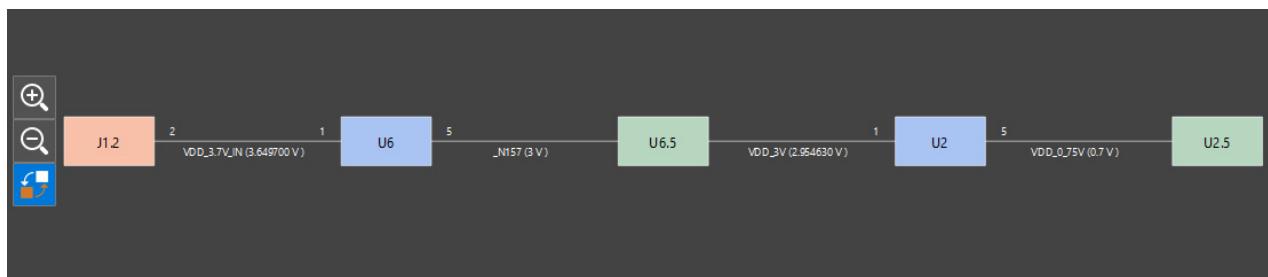


Hierarchical View

In the floating toolbar, you can click the following icon to switch to the hierarchical view:



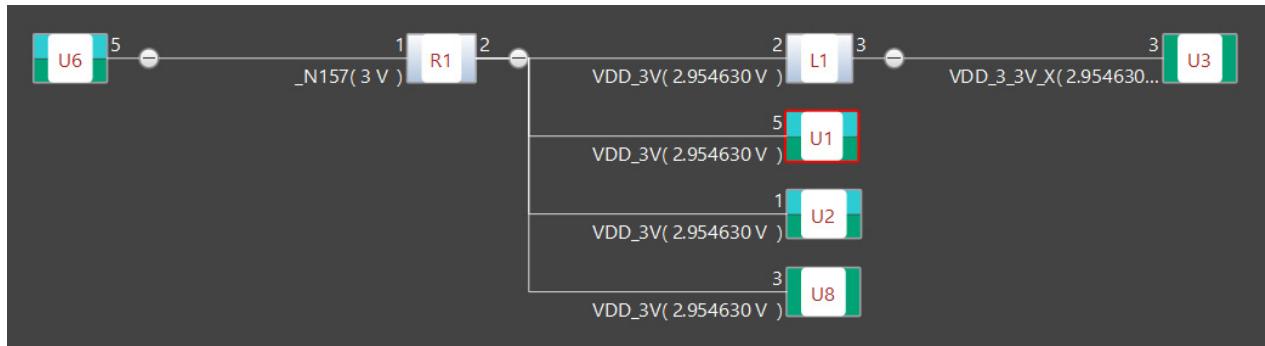
It is a simplified view to Power Topology graph that clubs the connectivity across all the VRMs.



Design Integrity and Analysis in Allegro X System Capture

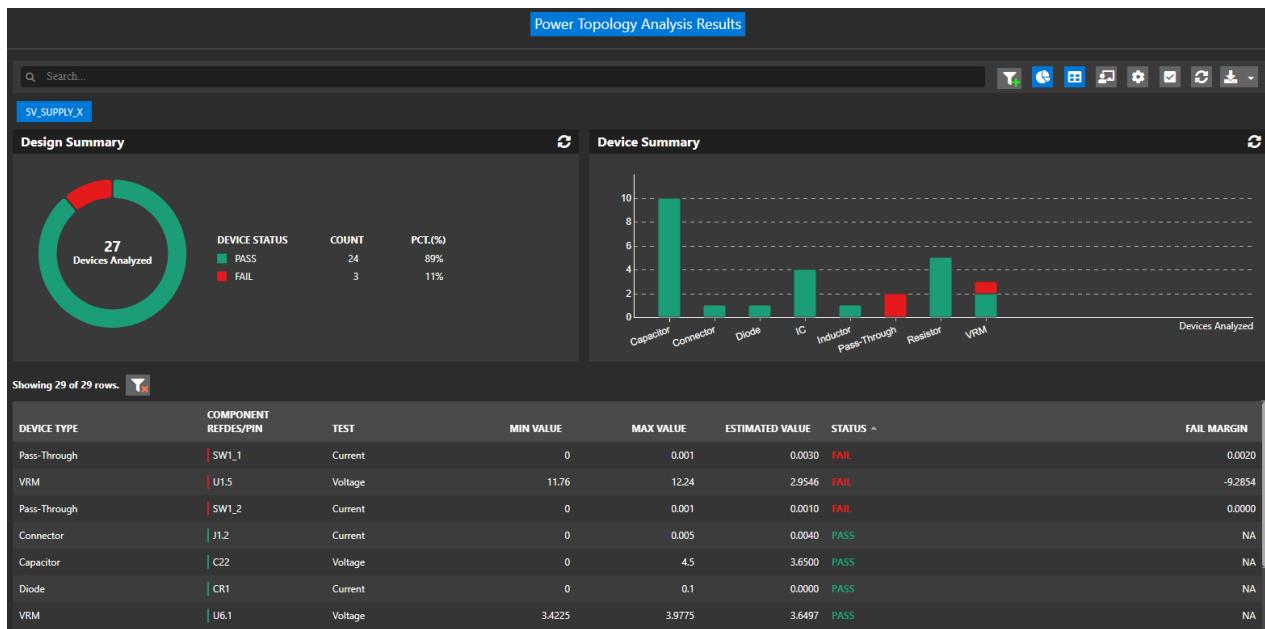
Power Topology Analysis

You can double click the VRM pin block to view the connected VRM branches.



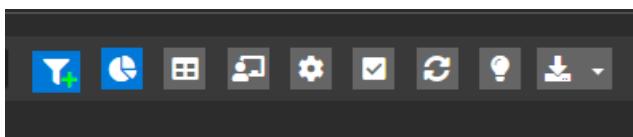
Dashboard Analysis

Power Topology Analysis Results dashboard shows the success or failure status of the component available in the design.



The dashboard analysis provides the following menu options:

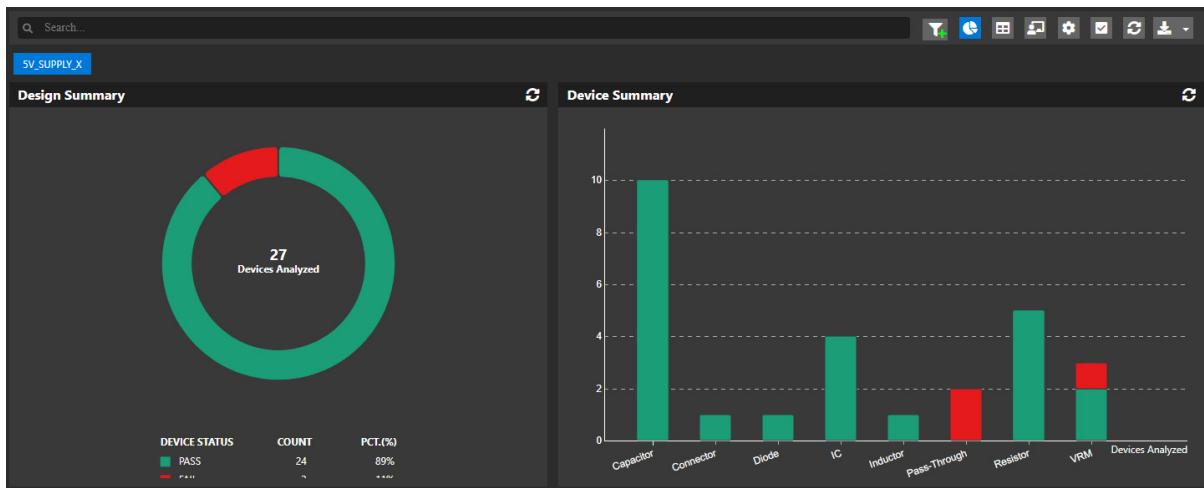
- A filter option to search for any device type, device sub-category, and, so on.



Design Integrity and Analysis in Allegro X System Capture

Power Topology Analysis

- *Toggle Charts Visibility* to view the summary of your design in doughnut and bar chart form.

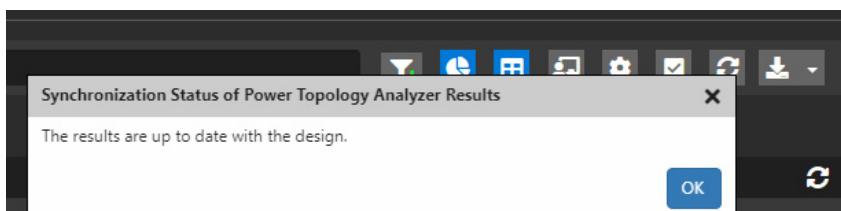


- *Toggle Table Visibility* to view the summary of your design in a tabular form.

The screenshot shows a table of analyzed device data. The columns are: DEVICE TYPE, COMPONENT REFDES/PIN, TEST, MIN VALUE, MAX VALUE, ESTIMATED VALUE, STATUS, and FAIL MARGIN. The data rows are:

DEVICE TYPE	COMPONENT REFDES/PIN	TEST	MIN VALUE	MAX VALUE	ESTIMATED VALUE	STATUS	FAIL MARGIN
Pass-Through	SW1_1	Current	0	0.001	0.0030	FAIL	0.0020
VRM	U1.5	Voltage	11.76	12.24	2.9546	FAIL	-9.2854
Pass-Through	SW1_2	Current	0	0.001	0.0010	FAIL	0.0000
Connector	J1.2	Current	0	0.005	0.0040	PASS	NA
Capacitor	C22	Voltage	0	4.5	3.6500	PASS	NA
Diode	CR1	Current	0	0.1	0.0000	PASS	NA

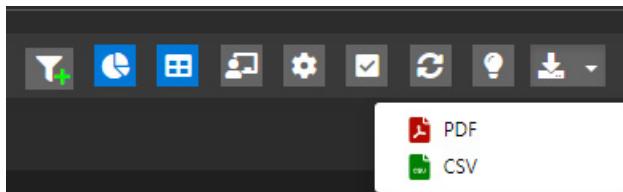
- *Toggle View* to view the summary of the successfully analyzed devices and the devices that are skipped in the Power Topology analysis.
- *Power Topology Settings* option to launch *Power Topology Settings* dialog box directly from the dashboard.
- Check whether the report is in sync with the design data.



Design Integrity and Analysis in Allegro X System Capture

Power Topology Analysis

- Option to re-run Power Topology analysis directly from the dashboard.
- Option to download Power Topology reports as PDF or CSV file.



Resolving Reported Errors After Power Topology Analysis

From the Power Topology analysis report, you can navigate to the location where the error is flagged in the schematic and resolve the issue.

Do the following:

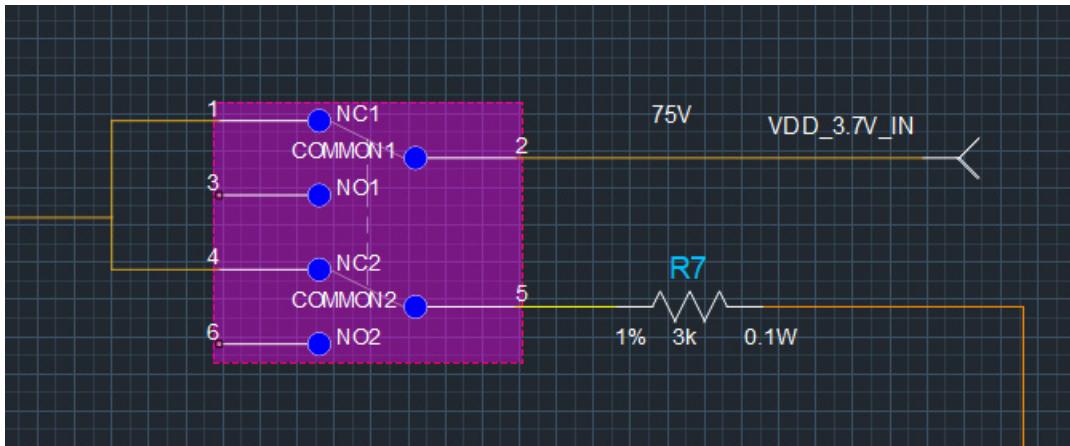
1. To navigate to the location of an error, right-click the required component row in the Power Topology report and select *Highlight in Schematic*.

Pass-Through	SW1_2	Current	Highlight in Schematic
Connector	J1.2	Current	Dehighlight in Schematic
Capacitor	C22	Voltage	Highlight in Topology
Diode	CR1	Current	Power Topology Settings
VRM	U6.1	Voltage	

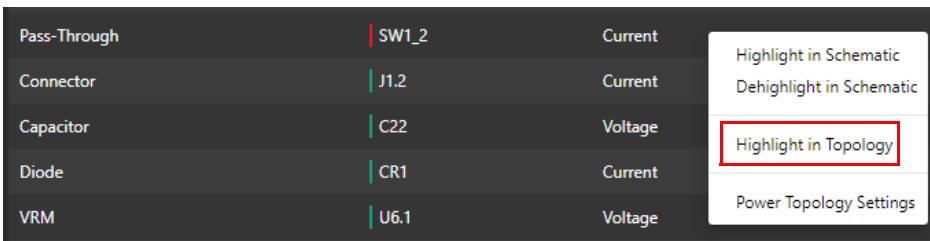
Design Integrity and Analysis in Allegro X System Capture

Power Topology Analysis

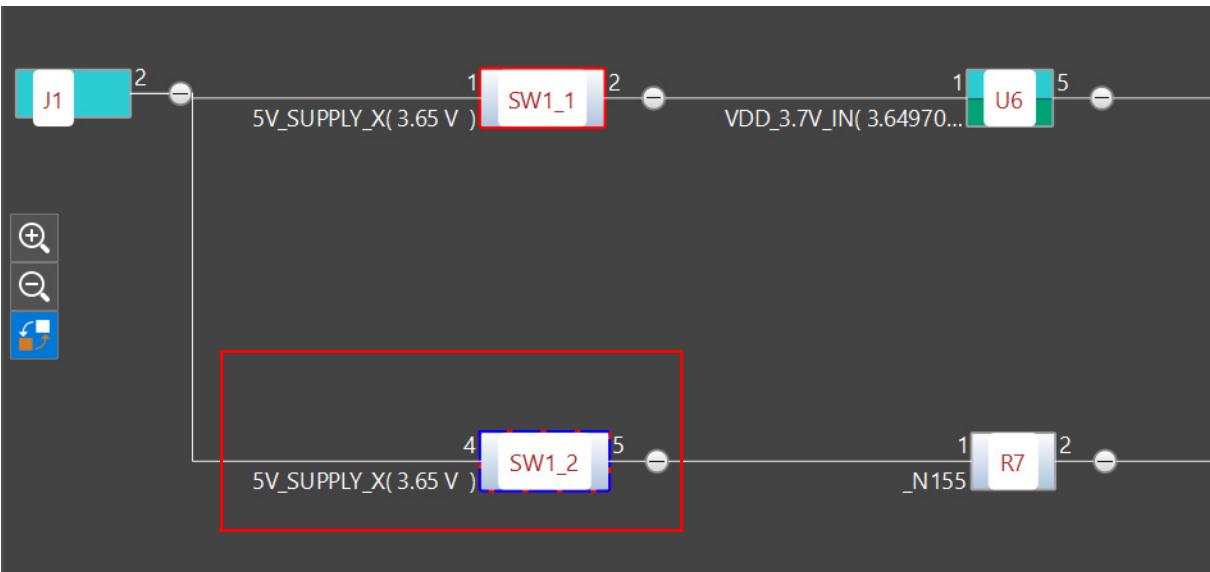
The component is highlighted in the schematic.



2. To highlight a component in the design topology, select *Highlight in Topology*.



The component is highlighted in the design Topology.



Design Integrity and Analysis in Allegro X System Capture

Power Topology Analysis

3. Modify the parameter values or change the component, as required.

After resolving the issue, re-run the Power Topology analysis.

Related Topics

- [Configuring Power Topology Settings](#)
- [Running Power Topology Analysis](#)

Design Integrity and Analysis in Allegro X System Capture

Power Topology Analysis

Thermal Analysis with Celsius Thermal Solver

Allegro X provides a unified framework where you can create schematics, do layout floor planning, and even estimate the PCB design life. Access to Celsius Thermal Solver is integrated from both the schematic and the layout floor plan. Thermal analysis helps in better placement of components early in the design cycle. Designers can estimate stress of schematic components based on the thermal map. All these help in taking circuit and BOM decisions at schematic stage based on thermal estimations. Some benefits of the integrated thermal analysis are:

- As designers try to fit components into a floorplan, the thermal status of the design enables them to take better schematic decisions.
- Thermal estimation can be done even before routing a design. This helps optimize the floorplan of the board early in the design process.
- The final detailed thermal analysis can be used to sign-off the board before it is sent for fabrication.

Prerequisites for Running Thermal Analysis

Before starting the analysis, ensure that the following are available:

- Electrical stress analysis results

To run the Electrical Analysis, choose *Design Integrity – Analyze Electrical Stress*.

For information on what all this analysis checks and how to configure it, see [Electrical Stress Analysis](#).

- Compatible Sigrity installation

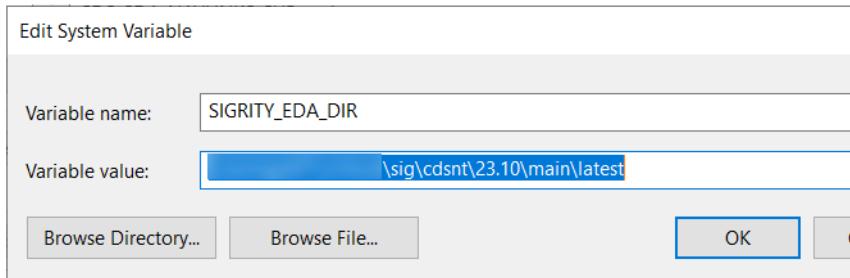
Celsius Thermal Solver is shipped separately. The path to the compatible Sigrity release, such as Sigrity 23.1 for Allegro System Capture 23.1, is set as an environment variable.

`SIGRITY_EDA_DIR = <path to Celsius executable file>`

Design Integrity and Analysis in Allegro X System Capture

Thermal Analysis with Celsius Thermal Solver

For example:



To identify which Sigriy release is compatible with the Allegro applications installed, refer to the *README.pdf* available on downloads.cadence.com. For example, for release 22.1 Hotfix 005, here is what you would find.

Hotfix	
Release Name	OrCAD/Allegro 22.1 [SPB221]
Release Date	23-Jun-2023
Release Version	SPB:Hotfix:22.10.005~wint
Release Number	SPB22.10.005
Media	 Download Media 1 of 1 zip format, Size: 3935792491 (3,753.46 MB)
Operating System	WINDOWS Windows 10 (64B) WINDOWS 11 WINDOWS 2016 Server WINDOWS 2019 Server
Documentation	README-Release_Notes.pdf README-checksums.md5 README.pdf README_CCR.txt README_kitlist.wint.txt

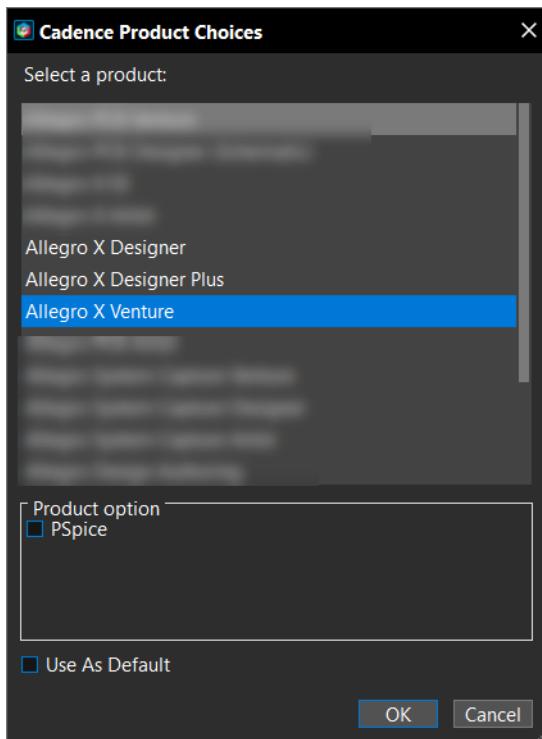
Supported Sigriy and Systems Analysis (SIGRITY/SY)
For users of Sigriy™ Aurora, SystemSI, 2022.1 HF3
SystemPI, Allegro® Sigriy™ PI, Allegro®
Sigriy™ SI, and APD-XtractIM and
Topology Explorer

- Any of the licenses that enable thermal analysis:
 - ❑ Allegro X Designer
 - ❑ Allegro X Designer Plus

Design Integrity and Analysis in Allegro X System Capture

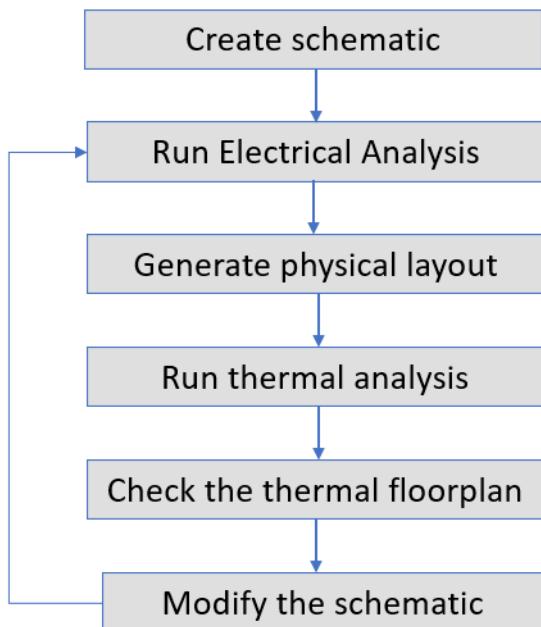
Thermal Analysis with Celsius Thermal Solver

□ Allegro X Venture



Generating the Thermal Floorplan for a Design

The following flowchart shows the steps involved in performing a thermal analysis on a design:



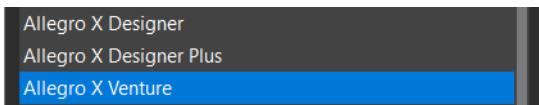
To generate the thermal floorplan of a design, follow these steps:

1. Start System Capture.

The *Cadence Product Choices* dialog box displays.

2. Choose one of the following licenses:

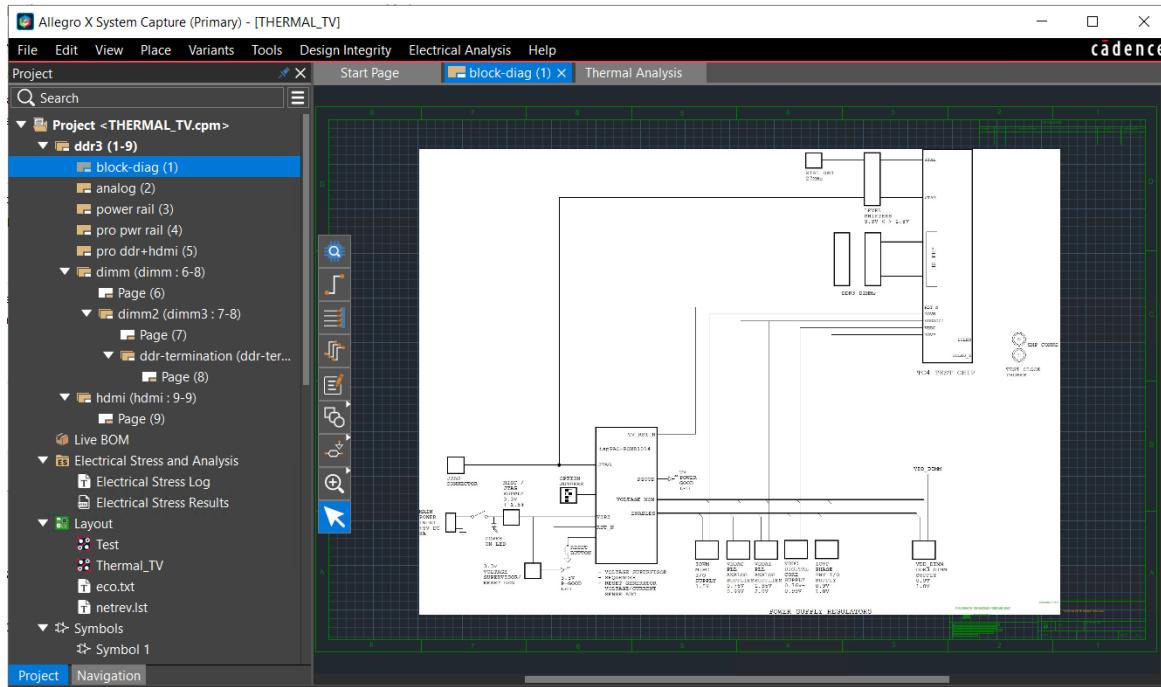
- Allegro X Designer
- Allegro X Designer Plus
- Allegro X Venture



Design Integrity and Analysis in Allegro X System Capture

Thermal Analysis with Celsius Thermal Solver

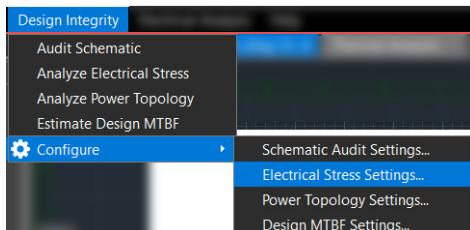
3. Open a design.



The electrical stress data is required for generating the thermal floorplan. If you have the latest stress analysis report, skip to [step 6](#), else continue to the next step.

4. Run the Electrical Stress Analysis.

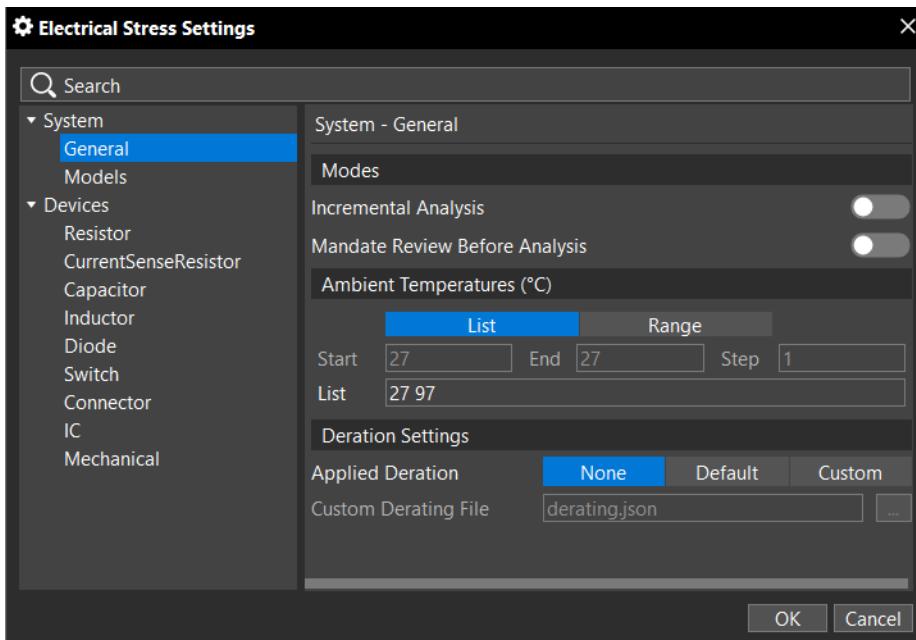
a. Choose *Design Integrity – Configure – Electrical Stress Settings*.



Design Integrity and Analysis in Allegro X System Capture

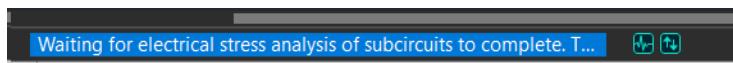
Thermal Analysis with Celsius Thermal Solver

The design is saved and the *Electrical Stress Settings* dialog box opens.



- b. Set the *Ambient Temperature – List* value as 27 97.
- c. Click *OK*.
- d. Choose *Design Integrity – Analyze Electrical Stress* to start the electrical stress analysis.

You are prompted to save the design before proceeding.

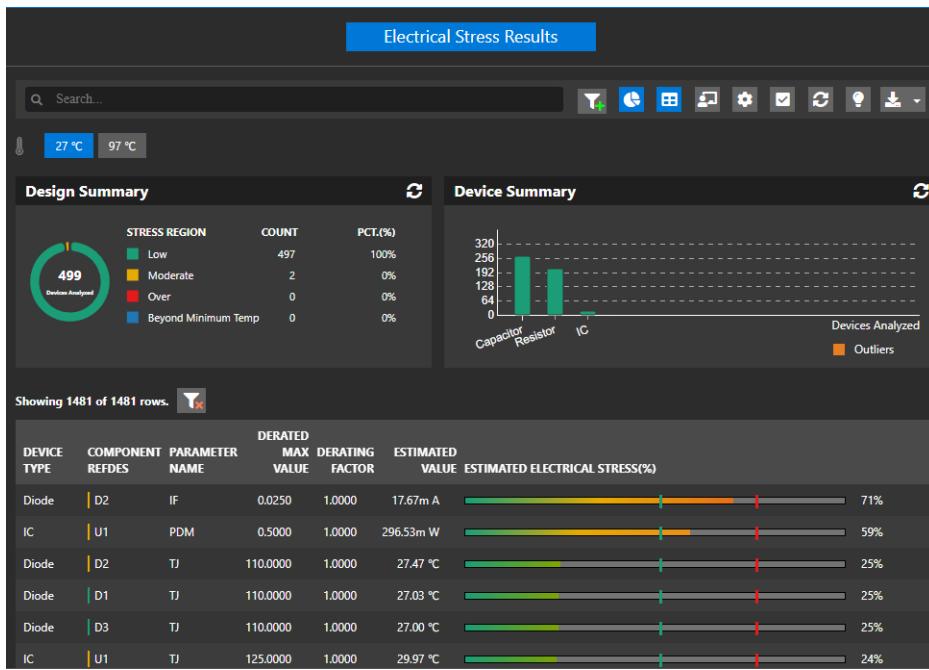


- e. Click *Yes*.

Design Integrity and Analysis in Allegro X System Capture

Thermal Analysis with Celsius Thermal Solver

The *Electrical Stress Results* dashboard opens.

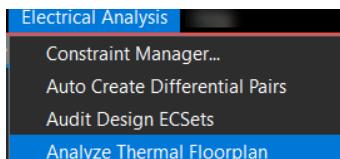


The required stress information is now available and the thermal floorplan can be generated.

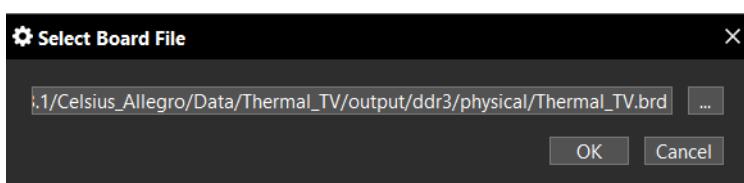
5. Switch back to the schematic page.

The *Electrical Analysis* menu is not available on dashboard pages.

6. Choose *Electrical Analysis – Analyze Thermal Floorplan*.



You are prompted to choose a board file.



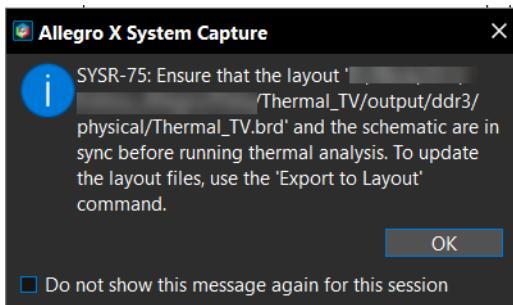
7. Choose the design board file.

Design Integrity and Analysis in Allegro X System Capture

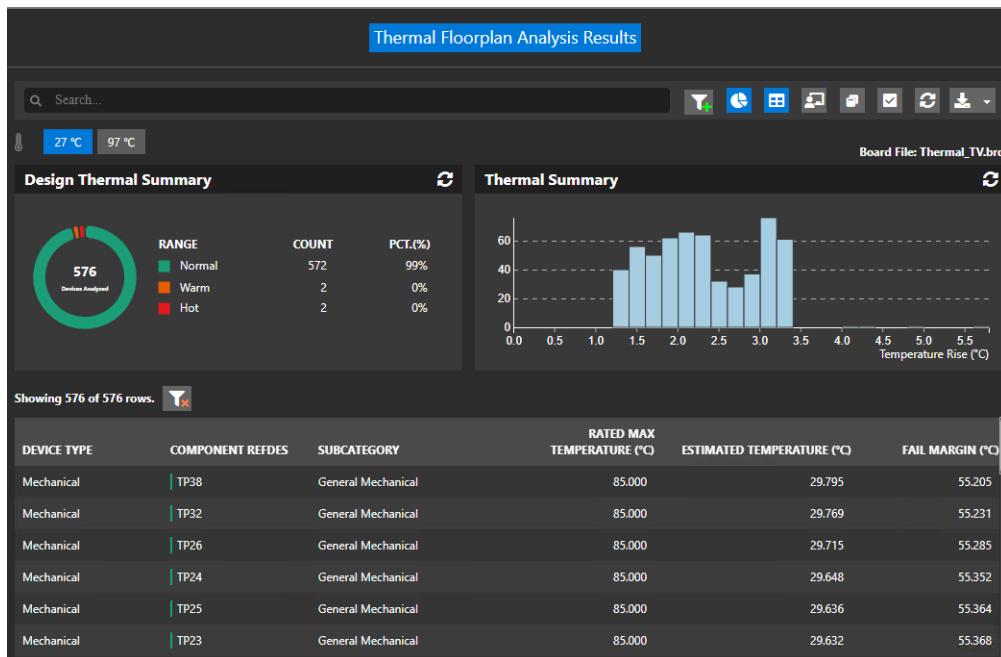
Thermal Analysis with Celsius Thermal Solver

8. Click OK.

A message prompts you to ensure that the board and the schematic are in sync.



The *Thermal Floorplan Analysis Results* dashboard opens.



By default, the dashboard shows charts and a table. The values entered in step b are shown as tabs, that is, 27 degrees and 97 degrees C.

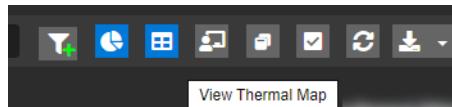
You can identify hot components on the PCB as shown in the doughnut chart, explore the impact of temperature rise, and so on.

To control what is displayed, click the icons available on the top-right.

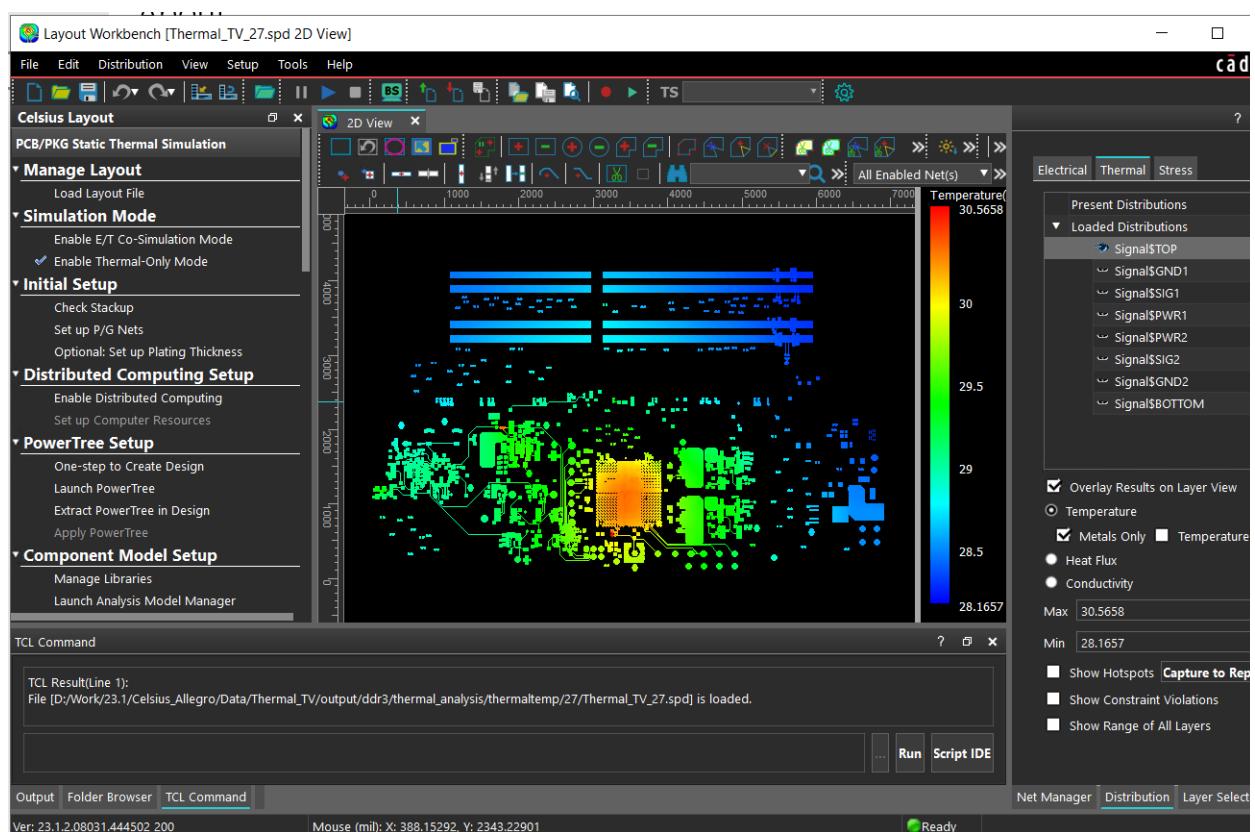
Design Integrity and Analysis in Allegro X System Capture

Thermal Analysis with Celsius Thermal Solver

9. Click *View Thermal Map* to view the thermal floorplan.



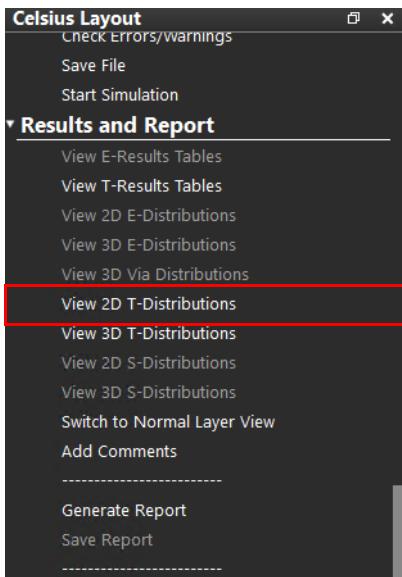
The *Layout Workbench* opens.



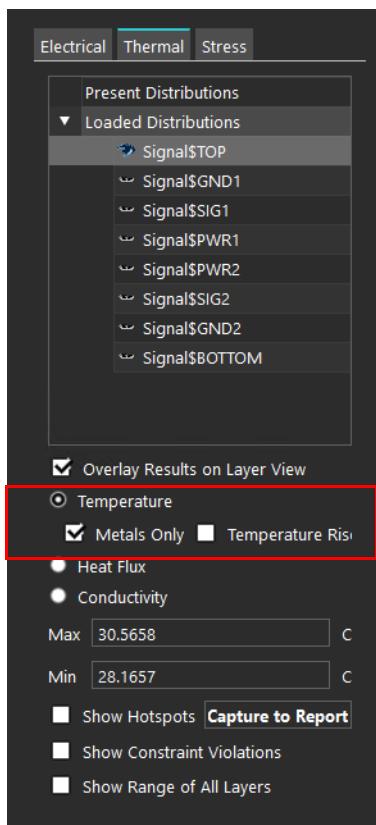
Design Integrity and Analysis in Allegro X System Capture

Thermal Analysis with Celsius Thermal Solver

10. Choose *Results and Report – View 2D T-Distributions* in the Celcius Layout panel on the left.



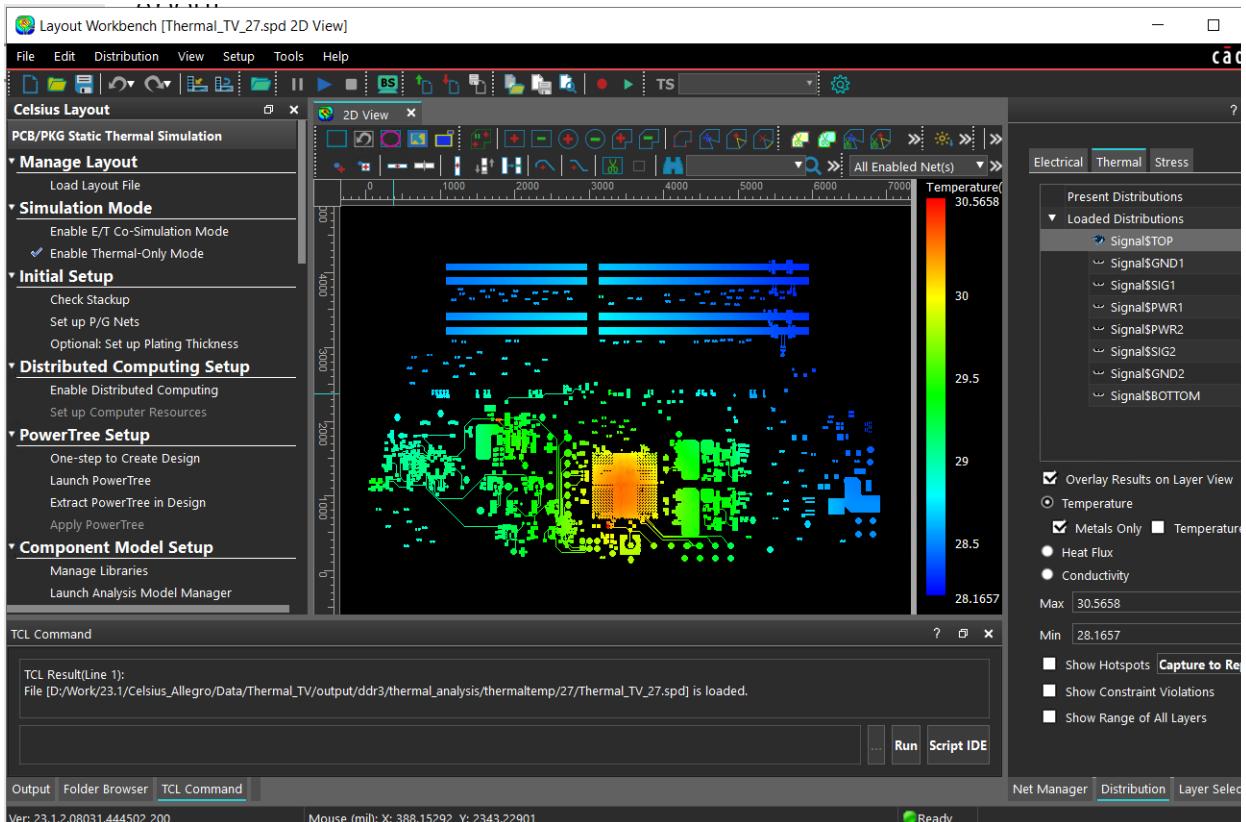
11. Choose *Metals Only* and clear *Temperature Rise*.



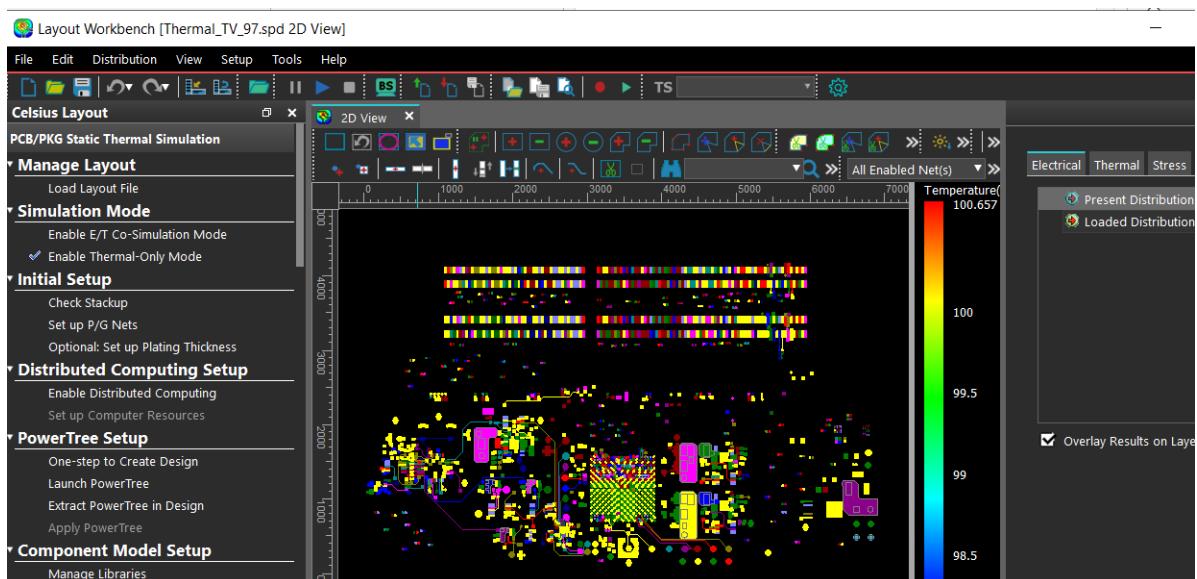
Design Integrity and Analysis in Allegro X System Capture

Thermal Analysis with Celsius Thermal Solver

The thermal map is loaded.



Similarly, you can view the thermal map for the design at 97 degrees C.



Design Integrity and Analysis in Allegro X System Capture

Thermal Analysis with Celsius Thermal Solver

Based on the thermal map, you can adjust the schematic and change the component placement.

Related Topics

- [Electrical Stress Analysis](#)
- [Analyzing Electrical Stress](#)

Schematic Audit Rules

There are a number of predefined rules used for auditing a schematic. This following table provides information about the list of rules for auditing a schematic:

Audit Rules Available With Artist and Designer Licenses

Audit Rule	Check Performed by the Rule
Missing footprint	Reports physical part instances with no associated footprints.
All Input Pins of IC Pulled Down	If all the input pins of an IC are connected to a pull-down resistor, the IC is flagged.
All Input Pins of IC Pulled Up	If all the input pins of an IC are connected to a pull-up resistor, the IC is flagged.
Asymmetrical Functions Missing	If you have a part with more than one section, this rule reports unused or non-instantiated sections in the design.
Connected IC NC Pins	NC pin detection: IC pin names starting with NC but not followed by a letter NC pins are checked for whether any net is connected to them. If found, NC pins are reported.
Differential pair net polarity mismatch	Patterns for nets/pins with positive polarity and negative polarity are defined in the 'Parameters' tab of Schematic Audit Settings dialog. Based on the name, the polarity of the nets/pins is decided and nets are checked for whether they are connected to IC pins with same polarities. If the polarity on nets and IC pins do not match, it is flagged.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule
Differential pair pins polarity mismatch	<p>Patterns for nets/pins with positive polarity and negative polarity are defined in the 'Parameters' tab of the Schematic Audit Settings dialog.</p> <p>Based on the name, the polarity of the pins is decided and pins are checked for whether they are connected to the pins of different ICs with the same polarity through differential pairs. If polarities of pins of different ICs connected through a differential pair do not match, it is flagged.</p>
Floating BJT	Reports BJTs with unconnected pins.
Floating Capacitors	Reports a capacitor if any of its pins is not connected to a net.
Floating Diodes	Reports a diode if any of its pins is not connected to a net.
Floating Inductors	Reports an inductor if any of its pins is not connected to a net.
Floating MOSFETs	Reports a MOSFET if any of its pins is not connected to a net.
Floating Resistors	Reports a resistor if any of its pins is not connected to a net.
Ground Net Without Voltage	Reports ground nets without voltage values.
Ground Nets With Non-Zero Voltage	Ground nets are checked for '0 V' as the voltage value. Ground nets with non-zero voltage value are flagged.
Grounded IC Output Pins	Reports IC output pins connected to ground.
High Pull-Down Values	<p>The maximum acceptable value for pull-down resistors is defined in the 'Parameters' tab of the Schematic Audit Settings dialog.</p> <p>The rule checks the value of pull-down resistors and if the resistor value is greater than the maximum value, it is flagged.</p> <p>Resistor values are accepted only with the following units: m, u, n, p, K, M, g, G, T)</p>

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule
High Pull-Up Values	<p>The maximum acceptable value for pull-up resistors is defined in the 'Parameters' tab of the Schematic Audit Settings dialog.</p> <p>The rule checks the value of pull-up resistors and if the resistor value is greater than the maximum value, it is flagged.</p> <p>Resistor values are accepted only with the following units: m, u, n, p, K, M, g, G, T</p>
IC Input Pins Without Driver	<p>Following are the drivers for IC input pins:</p> <ul style="list-style-type: none">■ IC input pins directly connected to POWER nets/ground nets■ IC input pins directly connected to POWER pins/ground pins■ IC input pins are connected to a pull-up/pull-down resistors■ IC input pins are driven by output/bidirectional pins of ICs (directly or through XNets)■ IC input pins are connected to MOSFETs/BJTs (directly or through XNets) <p>This rule checks for drivers if they are pulled-up or pulled-down through resistors. Discretes used for pulling up/down are not considered.</p>

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule
IC Output Pin Without Receiver	<p>Following are the receivers for IC output pins:</p> <ul style="list-style-type: none">■ IC output pins directly connected to POWER nets/ ground nets■ IC input pins directly connected to POWER pins/ ground pins■ IC output pins connected to pull-up/pull-down resistors■ IC output pins connected to input/bidirectional pins of ICs (directly or through XNets)■ IC input pins connected to MOSFETs/BJTs (directly or through XNets) <p>This rule also flags the IC output pins connected to voltage sources/ ground/nets with voltage property through series components (inductor and capacitor).</p>
IC Output Pin Without VOH/VOL	<p>This rule checks for VOH/VOL values through properties on connected output pins of ICs. If any or both of the VOH and VOL values are missing on output pins, this rule flags it.</p>
IC Power and Ground Pins Without Voltage	<p>Reports power and ground pins for ICs whose nets do not have voltages.</p>
Low Pull-Down Values	<p>The minimum acceptable values for pull-down resistors are defined in the 'Parameters' tab of the Schematic Audit Settings dialog.</p> <p>The rule checks the value of pull-down resistors and if it is less than the defined minimum value, it is flagged.</p> <p>Resistor values are accepted only with the following units: m, u, n, p, K, M, g, G, T</p>

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule
Low Pull-Up Values	<p>The minimum acceptable values for pull-down resistors are defined in the 'Parameters' tab of the Schematic Audit Settings dialog.</p> <p>The rule checks the value of pull-up resistors and if it is less than the defined minimum value, it is flagged.</p> <p>Resistor values are accepted only with the following units: m, u, n, p, K, M, g, G, T</p>
Missing Bypass Capacitor	<p>The rule checks for bypass capacitors on:</p> <ul style="list-style-type: none">■ Nets connecting to power pins of ICs■ Power nets <p>Nets without bypass capacitors are flagged.</p> <p>Bypass capacitors through series components (XNets) are not considered as bypass capacitors for power nets.</p>
Missing power nets	Reports power nets not placed on schematic
Power Net With 0V	Power nets are checked for non-zero voltage values. Power nets with '0 V' voltage values are flagged.
Power Net Without Voltage	Power nets and nets connected to power pins are checked for voltage values. Nets with no voltage values are flagged. Signal nets connected to power pins of ICs are excluded.
Single Connection nets	Reports single-node nets.
Unconnected Differential pair member nets, either or both	Reports differential pair nets whose members are unconnected
Unconnected Differential Pair Nets	Nets defined as differential pairs and left unconnected in the design are reported as unconnected differential pair nets.
Unconnected IC Input Pins	Input pins of IC are checked for whether any net is connected to them. The rule flags unconnected pins.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule
Unconnected IC Power and Ground Pins	Power and ground pins of ICs are checked for whether any net is connected to them. The rule flags unconnected pins.
Unconnected Nets	Unconnected nets in the design are flagged.
Unconnected Pins	Reports pins not connected to any net
Unconnected power pins	Reports power pins not connected to any net
Unrecognized Device for Audit	Reports unidentified devices. The rule checks for formats/valid reference designators, pin names, and the number of pins for device identification.
Value Unavailable on RLC	Reports resistors, inductors, or capacitors with missing values.
Inductor shorted with the same physical net	Reports inductors with more than one pin connected to the same physical net.
Incorrectly connected power pin, ground pin	Reports power pins and ground pins that are incorrectly connected.

Audit Rules Available With Designer, Venture, and Enterprise Licenses

The following rules, used for auditing a schematic, are only available with these licenses:

- Allegro System Capture Designer
- Allegro PCB Venture
- Allegro System Capture Venture
- Allegro Enterprise System Design Authoring
- Allegro Enterprise Authoring Solution

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule	Configuration Settings/Rule Check Patterns
Bus bit mismatch	Reports bus bits with indexes not matching the index of connected pins.	<p>The rule checks for index numbers in pin names of ICs connected to bus bit nets.</p> <p>If index numbers of bus bit nets and pin names of ICs do not match, the rule flags it.</p>
Bypass capacitor voltage exceeds rated voltage	Reports bypass capacitors whose DC voltage exceeds their rated voltage.	<p>Examples of a correct format:</p> <ul style="list-style-type: none"> ■ io<1> --> Pin1 ■ io<2> --> A2_3 <p>Examples that this rule flags:</p> <ul style="list-style-type: none"> ■ io<3> --> GPIO10 ■ io<4> --> V40
Capacitors shorted with the same physical net	Reports capacitors that have more than one pin connected to the same physical net.	<p>If a power net has a voltage value greater than the rated voltage of the bypass capacitor (read through voltage property) connected to it, this rule flags the bypass capacitor.</p> <p>Bypass capacitor detection: A capacitor connected to voltage at one end and a ground net at the other end.</p>
Clock pins of ICs not connected to same set of ICs or connectors as MISO and MOSI pins	Reports Clock pins of ICs that are not connected to same set of ICs or connectors as MISO and MOSI pins.	NA

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule	Configuration Settings/Rule Check Patterns
Clock pins of ICs or connectors connected to non-clock pins	Reports clock pins of ICs or connectors connected to non-clock pins of ICs or connectors.	Clock pins of ICs or connectors are identified and if these clock pin are connected to non-clock pins of ICs or connectors, they are flagged by the rule. The rule excludes clock pins connected to nets with voltages.
Differential pair member nets with multiple transmitters	Reports differential pair member nets that are connected to more than one transmitter pin.	When considering the connection to a connector, some generic pin names are excluded. For example: pin names starting with a letter followed by a digit, pin names starting with <code>IO</code> and followed by a digit and only digits.
Differential pair members not connected to same ICs	Reports differential pairs whose positive and negative members are not connected to same set of ICs or connectors	If a differential pair net is connected to multiple ICs and any of the member nets of a differential pair are connected to multiple TX pins, this rule flags the member net.
		TX pin detection is done when a pin name has <code>tx</code> in it.
		If nets of a differential pair are connected to ICs with different reference designators, the differential pair is flagged as Differential pair not connected to the same ICs .

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule	Configuration Settings/Rule Check Patterns
Differential pairs missing TX or RX	Reports differential pairs with missing TX or RX pairs.	<p>The rule identifies TX and RX differential pairs based on differential pair name patterns.</p> <p>A differential pair with a name ending with <code>TX</code> is considered a transmitter, while a differential pair with a name ending with <code>RX</code> is considered a receiver differential pair.</p>
		<p>For example: <code>SATA_TX</code> is a transmitter differential pair and <code>SATA_RX</code> is a receiver differential pair.</p>
		<p>Differential pair <code>SATA_TX</code> will have <code>SATA_TXP</code> and <code>SATA_TN</code> as its member nets. Differential pair <code>SATA_RX</code> will have <code>SATA_RXP</code>, and <code>SATA_RXN</code> as its member nets.</p>
Diodes shorted with the same physical net	Reports diodes that have more than one pin connected to the same physical net.	<p>This rule, which considers differential pairs which are already in the design, flags TX or RX differential pairs if the corresponding RX or TX pair is missing in the design.</p>
Fiducials not present	Reports if fiducials are not in the design	<p>The rule checks net names connected to both pins of a diode. If the physical net names are the same, the diode is flagged.</p>
Fiducials present is less than the minimum specified limit	Reports if the number of fiducials in the design is lower than the minimum specified limit	<p>NA</p>

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule	Configuration Settings/Rule Check Patterns
Holes not present	Reports if holes are not in the design	NA
Inductors shorted with the same physical net	Reports inductors that have more than one pin connected to the same physical net.	The rule checks for nets connected to both pins of an inductor. If the physical net names are the same, the inductor is flagged.
Invalid net name	Reports if net name has invalid characters in it	NA
Low-voltage class net having incorrect voltage	Reports nets of low-voltage class having voltage greater than threshold voltage	NA
MISO and MOSI pins of ICs incorrectly connected to non-MISO or non-MOSI pins	Reports MISO and MOSI pins of ICs incorrectly connected to non-MISO or non-MOSI pins	NA
MISO and MOSI pins of ICs not connected to the same set of ICs or connectors	Reports MISO and MOSI pins of ICs not connected to same set of ICs or connectors	NA
Missing resistors at BJT base	Reports BJTs that do not have resistors connected to the base pins.	If a resistor is missing at the base of a BJT, or if a net connected to a BJT base has voltage, the base pin of the BJT is flagged.
Nets connected through discretes belonging to different net classes	Reports nets connected through discretes R,L,C that belong to different net classes	NA

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule	Configuration Settings/Rule Check Patterns
Nets connected to SCL pins missing a pull-up	Reports SCL pins of ICs that are missing a pull-up.	If a pull-up resistor is missing on SCL pins of IC, the rule flags it. Up to 17.4-2019 hotfix 019, only a single pull-up resistor is considered. Resistors in a series that make a pull-up are not identified as pull-ups for that particular net/pin of an IC.
Nets connected to SDA pins missing a pull-up	Reports SDA pins of ICs that are missing a pull-up.	If a pull-up resistor is missing on SDA pins of an IC, the rule flags it. Up to 17.4-2019 hotfix 019, only a single pull-up resistor is considered. Resistors in series that make a pull-up are not identified as pull-ups for that particular net/pin of an IC.
Nets not connected to off-page port	Reports nets that are on multiple pages but are not connected to an off-page port	NA
Nets with missing voltage, zero voltage, non-zero voltage based on net name	Reports nets, based on the net names, with missing voltage, zero voltage, non-zero voltage.	Nets with certain patterns in their names, such as [POWER, VDD, VCC, VBB, VTT, VBAT, VIN, V(digit), (digit)P(digit)] are checked for missing voltages or zero voltage. Nets with patterns in the name, such as [GROUND, GND] are checked for missing voltage or non-zero voltage.
Nets with pull-up and pull-down resistors	Reports nets with pull-up and pull-down resistors connected to them.	The rule flags nets with pull-up and pull-down resistors connected to them.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule	Configuration Settings/Rule Check Patterns
Open collector output pin missing a pull-up	Reports open collector output pins that are connected but are missing a pull-up resistor.	The rule checks for pull-up resistors on OC/OCA pins of ICs. If missing, the rule flags the resistor. Pull-up resistors through series components (XNets) are not considered as pull-up resistors.
Parallel Inductors	Reports inductors parallel to each other.	The rule flags inductors parallel to each other.
Parallel Resistors	Reports resistors parallel to each other.	The rule flags resistors parallel to each other.
RAS and CAS pins of IC incorrectly connected	Reports RAS pins of ICs incorrectly connected to CAS pins and vice versa.	CAS and RAS pin patterns are predefined as CPM directives in the project CPM file. No user input required. CAS and RAS pins of ICs are identified based on pin patterns.
RAS and CAS pins of ICs incorrectly connected to non-RAS or non-CAS pins	Reports RAS and CAS pins of ICs incorrectly connected to non-RAS or non-CAS pins.	If CAS pins are connected to RAS pins or vice versa, this rule flags the pins. CAS and RAS pins connected to non-CAS and non-RAS pins are not flagged.
RAS and CAS pins of ICs not connected to the same set of ICs or connectors	Reports RAS and CAS pins of ICs not connected to same set of ICs or connectors.	This rule flags the RAS and CAS pins of ICs that are incorrectly connected to non-RAS or non-CAS pins. This rule flags the RAS and CAS pins of ICs that are not connected to the same set of ICs or connectors.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule	Configuration Settings/Rule Check Patterns
RefDes visibility	Reports invisible reference designators for components for a specified reference designator pattern	NA
Resistors shorted with the same physical net	Reports resistors that have more than one pin connected to the same physical net.	The rule checks net names connected to both pins of a resistor. If physical net names are the same, the resistor is flagged.
Same group power pins connected to nets with different voltage values	Reports power pins of the same group but connected to nets with different voltage values.	<p>Power pins of an IC are considered grouped if the names of power pins are the same, but end with different digits.</p> <p>For example, power pins of IC with names VDD1, VDD2, VDD3, VDD4 are considered as belonging to a group.</p> <p>Design Integrity reports a group of power pins if the nets connecting to pins have different voltage values.</p>
SDA and SCL pin of IC incorrectly connected	Reports SDA pins of ICs incorrectly connected to SCL pins and vice-versa.	<p>If an SDA pin of an IC is connected to an SCL pin of an IC, the SDA pin is flagged.</p> <p>Similarly, if an SCL pin of an IC is found to be connected to an SDA pin of an IC, the SCL pin is flagged.</p>
		This rule does not cover SDA pins connected to any non-SDA pins, or SCL pins connected to non-SCL pins.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule	Configuration Settings/Rule Check Patterns
SDA and SCL pins of ICs incorrectly connected to non-SDA or non-SCL pins	Reports SDA and SCL pins of ICs incorrectly connected to non-SDA or non-SCL pins.	The rule flags SDA and SCL pins of ICs that are incorrectly connected to non-SDA or non-SCL pins.
SDA and SCL pins of ICs not connected to the same set of ICs or connectors	Reports SDA and SCL pins of ICs not connected to the same set of ICs or connectors.	The rule flags SDA and SCL pins of ICs that are not connected to the same set of ICs or connectors.
Single-connection differential pair nets	Reports single-connection floating differential pair nets.	Differential pairs that have nets connected only at one end are flagged as single-connection differential pair nets.
System-generated net name	Reports nets that have system-generated net names.	<p>System-generated nets are nets that have names with the following format: '_N%' ('%' being any numerical value).</p> <p>This rule flags all system-generated nets.</p> <p>Even with extra characters added to system-generated net names, such as _N1a or _N1_A, the nets are still considered system-generated nets.</p>
Testpads not connected to a net having user-defined name	Reports if testpads are not connected to a net having user-defined name	NA
Testpads not present	Reports if testpads are not in the design	NA
Unconnected Chip Select pins of ICs when MISO or MOSI pins are connected	Reports Chip Select pins of ICs that are unconnected, but MISO and MOSI pins are connected	NA

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule	Configuration Settings/Rule Check Patterns
Unconnected Clock pins of ICs when MISO or MOSI pins are connected	Reports Clock pins of ICs that are unconnected, but MISO and MOSI pins are connected	NA
Unconnected MISO and MOSI pins of ICs	Reports MISO and MOSI pins of an IC when either MISO or MOSI pin of an IC is connected, but not both	NA
Unconnected RAS and CAS pins of ICs	Reports RAS and CAS pins of an IC when either RAS or CAS pin of an IC is connected, but not both.	NA
Unconnected SDA and SCL pins of ICs	Reports SDA and SCL pins of an IC when either SDA or SCL pin of an IC is connected, but not both.	NA
Voltage net missing net class	Reports nets with voltages missing net class	NA

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rule	Check Performed by the Rule	Configuration Settings/Rule Check Patterns
Voltage on capacitor is not per pin polarity	Reports capacitors when voltage on capacitor pins is not per pin polarity.	<p>Voltages are read on the nets that connect to the positive and negative pins of the capacitor.</p> <p>If the voltage on nets connecting to the positive pin is lower than that of the negative pin, the capacitor is reported.</p> <p>Capacitor pin polarity detection:</p> <ul style="list-style-type: none">■ The value of PIN_POLARITY is checked for the capacitor pin in the chips.prt file.■ The property PIN_POLARITY is read on the capacitor pin from the chips.prt file.■ If PIN_POLARITY='POS', the pin of the capacitor is treated as positive.■ If PIN_POLARITY='NEG', the pin of the capacitor is treated as negative. <p>CPM directives for specifying polarity keywords for this rule are as follows:</p> <ul style="list-style-type: none">■ POLAR_CAP_NEG_PIN 'NEG'■ POLAR_CAP_POS_PIN 'POS'

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Audit Rules Available for CPM Directives

The following rules, used for the CPM directives for auditing a schematic, are only available with these licenses:

- Allegro PCB Venture
- Allegro Enterprise Authoring Solution
- Allegro Venture System Design Authoring
- Allegro System Capture Venture
- Allegro Enterprise System Design Authoring
- Allegro X EE
- Allegro System Capture Designer
- Allegro Enterprise PCB Designer Suite
- Allegro PCB Designer (Schematic)

Audit Rule	Description	Directive	Identification
Fiducials not present	Reports if fiducials are not present	FIDUCIAL_FOOTPRINT_NAME_PATTERN	If the FIDUCIAL_FOOTPRINT_NAME_PATTERN pattern is not found in JEDEC_TYPE and the BOM_IGNORE property is found, the part is considered fiducial.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Fiducials present is less than the minimum specified limit	Reports if number of fiducials are present is less than the minimum specified limit	FIDUCIAL_FOOTPRINT_NAME_PATTERN ERN FIDUCIAL_MIN_NUMBER	If the FIDUCIAL_FOOTPRINT_NAME_PATTERN pattern is not found in JEDEC_TYPE and the BOM_IGNORE property is found, the part is considered fiducial. The number of fiducials present should be less than FIDUCIAL_MIN_NUMBER.
Holes not present	Reports if holes are not present	HOLE_FOOTPRINT_NAME_PATTERN	If the HOLE_FOOTPRINT_NAME_PATTERN pattern is found in JEDEC_TYPE and BOM_IGNORE property is found, the part is considered as a hole.
Testpads not present	Reports if testpads are not present	TESTPAD_FOOTPRINT_NAME_PATT ERN	If the TESTPAD_FOOTPRINT_NAME_PATTERN pattern is found in JEDEC_TYPE and the BOM_IGNORE property is found, the part is considered a testpad.
Testpads not connected to a net having user-defined name	Reports if testpads are not connected to a net having user-defined name	TESTPAD_FOOTPRINT_NAME_PATT ERN	If the net connected to the testpad is a generated net, a violation is flagged.
RefDes visibility	Reports invisible refdes for components for specified refdes pattern	REFDES_PREFIX_VISIBILITY_CHECK	Flags violation if refdes are not visible on canvas for parts whose refdes match the pattern specified by REFDES_PREFIX_VISIBILITY_CHECK.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Invalid net name	Reports if net name has invalid characters in it	ILLEGAL_NET_NAME_ME_CHAR	Flags violation if the logical net name has invalid characters specified by ILLEGAL_NET_NAME_CHAR.
Voltage net missing net class	Reports nets with voltages missing net class	NA	Flags violation if the voltage net present in the design does not have a net class (physical, spacing, or electrical) assigned to it.
Low-voltage class net having incorrect voltage	Reports nets of low-voltage class having voltage greater than threshold voltage	LOWVOLTAGE_CLASS_PATTERN LOWVOLTAGE_THRESHOLD	For each physical net, get net class list {P:S:E}, if any of net class names {Physical, Spacing, Electrical} has LOWVOLTAGE_CLASS_PATTERN and if the voltage on the net is greater than LOWVOLTAGE_THRESHOLD, the net is reported.
Nets connected through discretes belonging to different net classes	Reports nets connected through discretes R,L,C that belong to different net classes	NA	Physical, spacing, and electrical class on both sides of the discretes should be the same; otherwise, the net is reported.

Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Unconnected MISO and MOSI pins of ICs	Reports MISO and MOSI pins of an IC when either MISO or MOSI pin of an IC is connected, but not both	MISO_PIN_PATTE RN MOSI_PIN_PATTE RN MISO_NET_PATTE RN MOSI_NET_PATTE RN	For an IC, scan all the pins. If the pin is a MISO pin, identified by a pattern specified in MISO_PIN_PATTERN, it generates the expected pin name of the MOSI pin. Check if the pin name exists on that IC. If yes, get the physical pin for the expected MOSI pin. Check if the MISO pin has a MISO connection using MISO_NET_PATTERN and if the MOSI pin has a MOSI connection using MOSI_NET_PATTERN. Report if exactly one pin is unconnected. Identification of MOSI pins: <ul style="list-style-type: none">- Check if the pin is a MOSI pin, identified by MOSI_PIN_PATTERN- Match the name of the net connected to the MOSI pin with MOSI_NET_PATTERN. Identification of MISO connection: <ul style="list-style-type: none">- Check if the pin is a MISO pin, identified by MISO_PIN_PATTERN- Match the name of the net connected to the MISO pin with MISO_NET_PATTERN.
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Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

MISO and MOSI pins of ICs not connected to the same set of ICs or connectors	Reports MISO and MOSI pins of ICs not connected to same set of ICs or connectors	MISO_PIN_PATTE RN MOSI_PIN_PATTE RN MISO_NET_PATTE RN MOSI_NET_PATTE RN	For an IC, scan all the pins. If the pin is a MISO pin, identified by a pattern specified in MISO_PIN_PATTERN, get the net connected to the MISO pin and its XNET members. Generate the expected pin name of the MOSI pin. Check if the pin name exists on that IC; if yes, get the physical pin for the expected MOSI pin. Check if the MISO pin has an MISO connection using MISO_NET_PATTERN and if the MOSI pin has a MOSI connection using MOSI_NET_PATTERN. Find the ICs, and connectors connected to MOSI and MISO pin's net. Report if there is a mismatch in the connected ICs and connectors. Identification of MOSI pins: <ul style="list-style-type: none">- Check if the pin is a MOSI pin, identified by MOSI_PIN_PATTERN- Match the name of the net connected to the MOSI pin with MOSI_NET_PATTERN. Identification of MISO connection: <ul style="list-style-type: none">- Check if the pin is a MISO pin, identified by MISO_PIN_PATTERN- Match the name of the net connected to the MISO pin with
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Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

MISO and MOSI pins of ICs incorrectly connected to non-MISO or non-MOSI pins	Reports MISO and MOSI pins of ICs incorrectly connected to non-MISO or non-MOSI pins	MISO_PIN_PATTE RN MOSI_PIN_PATTE RN MISO_NET_PATTE RN MOSI_NET_PATTE RN	Scan all the pins of an IC, and identify MISO or MOSI pins. Check the pins for MISO or MOSI connection using MISO_NET_PATTERN and MOSI_NET_PATTERN. If the connection is found, find the net connected to the pin. Find the XNET and all the member nets of the XNET. For each member net, check if the net connects to a pin that belongs to an IC. If yes, report if the pin cannot be identified as an MISO or MOSI pin. Identification of MOSI pins: <ul style="list-style-type: none">- Check if the pin is a MOSI pin, identified by MOSI_PIN_PATTERN- Match the name of the net connected to the MOSI pin with MOSI_NET_PATTERN. Identification of MISO connection: <ul style="list-style-type: none">- Check if the pin is a MISO pin, identified by MISO_PIN_PATTERN- Match the name of the net connected to the MISO pin with MISO_NET_PATTERN.
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Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Unconnected clock pins of ICs when MISO or MOSI pins are connected	Reports clock pins of ICs that are unconnected, but MISO and MOSI pins are connected.	MISO_PIN_PATTE RN MOSI_PIN_PATTE RN MISO_NET_PATTE RN MOSI_NET_PATTE RN CLOCK_PIN_PATT ERN	For an IC, scan all the pins. If the pin can be identified as MISO, generate the expected MOSI and Clock pin names. Check if the expected pin names exist on that IC. If yes, get the physical pin for the expected MOSI and Clock pin. Check the pins for MISO/MOSI connection using MISO_NET_PATTERN and MOSI_NET_PATTERN. If MOSI MISO are both connected or if exactly one is connected and the clock pin is left unconnected, flag a violation. Identification of MOSI pins: <ul style="list-style-type: none">- Check if the pin is a MOSI pin, identified by MOSI_PIN_PATTERN- Match the name of the net connected to the MOSI pin with MOSI_NET_PATTERN. Identification of MISO connection: <ul style="list-style-type: none">- Check if the pin is a MISO pin, identified by MISO_PIN_PATTERN- Match the name of the net connected to the MISO pin with MISO_NET_PATTERN.
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Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Clock pins of ICs not connected to same set of ICs or connectors as MISO and MOSI pins.	Reports clock pins of ICs that are not connected to same set of ICs or connectors as MISO and MOSI pins.	MISO_PIN_PATTE RN MOSI_PIN_PATTE RN MISO_NET_PATTE RN MOSI_NET_PATTE RN CLOCK_PIN_PATT ERN	For an IC, scan all the pins. If the pin is a MISO pin, identified by a pattern specified in MISO_PIN_PATTERN, get the net connected to the MISO pin and its XNET members. Generate the expected pin name of the MOSI and Clock pin. Check if the pins exist on that IC; if yes, get the physical pin for the expected MOSI and clock pin. Check if the MISO pin has a MISO connection using MISO_NET_PATTERN and if the MOSI pin has a MOSI connection using MOSI_NET_PATTERN. Find the ICs, and connectors connected to the MOSI, Clock, and MISO pin's net. Report if there is a mismatch in the connected ICs and connectors. Identification of MOSI pins: <ul style="list-style-type: none">- Check if the pin is a MOSI pin, identified by MOSI_PIN_PATTERN- Match the name of the net connected to the MOSI pin with MOSI_NET_PATTERN. Identification of MISO connection: <ul style="list-style-type: none">- Check if the pin is a MISO pin, identified by MISO_PIN_PATTERN- Match the name of the net connected to the
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Design Integrity and Analysis in Allegro X System Capture

Schematic Audit Rules

Unconnected chip select pins of ICs when MISO or MOSI pins are connected	Reports Chip Select pins of ICs that are unconnected, but MISO and MOSI pins are connected	MISO_PIN_PATTE RN MOSI_PIN_PATTE RN MISO_NET_PATTE RN MOSI_NET_PATTE RN CS_PIN_PATTERN	For an IC, scan all the pins. If the pin can be identified as MISO, generate the expected pin names of the MOSI and CS pin. Check if the expected pin names exist on that IC. If yes, get the physical pin for the expected MOSI and CS pin. Check the pins for MISO/MOSI connection using MISO_NET_PATTERN and MOSI_NET_PATTERN. If MOSI and MISO are connected or if exactly one is connected and the CS pin is left unconnected, flag a violation. Identification of MOSI pins: <ul style="list-style-type: none">- Check if the pin is a MOSI pin, identified by MOSI_PIN_PATTERN- Match the name of the net connected to the MOSI pin with MOSI_NET_PATTERN. Identification of MISO connection: <ul style="list-style-type: none">- Check if the pin is a MISO pin, identified by MISO_PIN_PATTERN- Match the name of the net connected to the MISO pin with MISO_NET_PATTERN.
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Design Integrity and Analysis in Allegro X System Capture

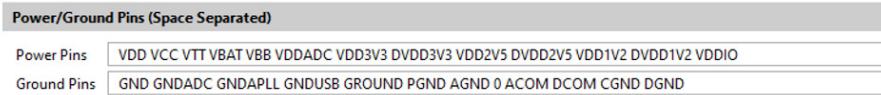
Schematic Audit Rules

Related Topics

- [Configuring Schematic Audit Settings](#)
- [Design Analyses](#)
- [Design Integrity CPM Directives](#)

Device Identification and Pin Detection

This following table provides information about device identification and pin detection:

Identification/Detection	Basis of Identification/Detection				
Device identification	The component type is identified based on the reference designator format, number of pins, and pin names.				
Power pin, ground pin detection	Based on the pin name as defined in the Schematic Audit Settings dialog or based on pins defined as power/ground pins in <code>chips.prt</code>				
 <p>Power/Ground Pins (Space Separated)</p> <table border="1"><tr><td>Power Pins</td><td>VDD VCC VTT VBAT VBB VDDADC VDD3V3 DVDD3V3 VDD2V5 DVDD2V5 VDD1V2 DVDD1V2 VDDIO</td></tr><tr><td>Ground Pins</td><td>GND GNDADC GNDAPLL GNDUSB GROUND PGND AGND 0 ACOM DCOM CGND DGND</td></tr></table>		Power Pins	VDD VCC VTT VBAT VBB VDDADC VDD3V3 DVDD3V3 VDD2V5 DVDD2V5 VDD1V2 DVDD1V2 VDDIO	Ground Pins	GND GNDADC GNDAPLL GNDUSB GROUND PGND AGND 0 ACOM DCOM CGND DGND
Power Pins	VDD VCC VTT VBAT VBB VDDADC VDD3V3 DVDD3V3 VDD2V5 DVDD2V5 VDD1V2 DVDD1V2 VDDIO				
Ground Pins	GND GNDADC GNDAPLL GNDUSB GROUND PGND AGND 0 ACOM DCOM CGND DGND				
Ground net identification	Nets with zero-voltage values are defined as ground nets in the Schematic Audit Settings dialog.				
	User configurable				
Power net identification	Nets with zero-voltage values are defined as power nets in the Schematic Audit Settings dialog.				
	User configurable				
Clock pin detection	<code>CLOCK_PIN_PATTERN</code> in pin name				
SDA pin detection	<code>SDA_PIN_PATTERN</code> in pin name				
SCL pin detection	<code>SCL_PIN_PATTERN</code> in pin name				
RAS pin detection	<code>RAS_PIN_PATTERN</code> in pin name				
CAS pin detection	<code>CAS_PIN_PATTERN</code> in pin name				

Design Integrity and Analysis in Allegro X System Capture

Device Identification and Pin Detection

Related Topics

- [Configuring Electrical Stress Settings](#)
- [Design Analyses](#)

Pattern Matching

This section provides information about the property alias for design parameters, reference designator prefixes or patterns that you might need to know.

Design Integrity and Analysis in Allegro X System Capture
 Pattern Matching

Property Alias

Parameter	Type	Property Alias	Unit	Description
AGD	AREA	AGDIGATE-DRAIN AREAIIG-D AREA	square-m	GATE-DRAIN OVERLAP AREA
ALPHA	Voltage	ALPHASATURATION VOLTAGE		SATURATION VOLTAGE PARAMETER
AREA	AREA	AREA		AREAAA
AT	Attenuation	ATATTENUATION		ATTENUATION
BETA	TRANSCONDUCTANCE	BETAITRANSCONDU CTANCE		TRANSCONDUCTANCE PARAMETER
BF		BFIHFEIGAINIBETA		IDEAL MAXIMUM FORWARD BETA
BV	Voltage	BVIREVERSE BREAKDOWN VOLTAGE		REVERSE BREAKDOWN VOLTAGE
BVF		BVFIAVALANCHE UNIFORMITY FACTOR		AVALANCHE UNIFORMITY FACTOR
C	Capacitance	CICAPACITANCE		CAPACITANCE
CGD	Capacitance	CGDIGATE-DRAIN JUNCTION CAPACITANCEIIG-D JUNCTION CAPACITANCE		ZERO-BIAS GATE-DRAIN JUNCTION CAPACITANCE
CGDO	Capacitance	CGDOIIGATE-DRAIN CAPACITANCEIIG-S CAPACITANCE		GATE-DRAIN OVERLAP CAPACITANCE PER METER CHANNEL WIDTH
CGS	Capacitance	CGSIGATE-SOURCE JUNCTION CAPACITANCEIIG-S JUNCTION CAPACITANCE		ZERO-BIAS GATE-SOURCE JUNCTION CAPACITANCE
CGSO	Capacitance	CGSOIIGATE- SOURCE CAPACITANCEIIG-S CAPACITANCE		GATE-SOURCE OVERLAP CAPACITANCE PER METER CHANNEL WIDTH
CI	Current	Current	A	Maximum ripple current supported by the capacitor

Design Integrity and Analysis in Allegro X System Capture

Pattern Matching

Parameter	Type	Property Alias	Unit	Description
CJO	Capacitance	CJOIZERO-BIAS JUNCTION CAPACITANCE		ZERO-BIAS JUNCTION CAPACITANCE
COXD	Capacitance	COXD		GATE-DRAIN OVERLAP OXIDE CAPACITANCE
CTR	Current	CTRICURRENT TRANSFER RATION		CURRENT TRANSFER RATIO
CV	Voltage	Voltage\VOLTIMAX_VOLTAGE\ERATED_VOLTAGE_MAXIMUM	V	Maximum voltage rating supported by the capacitor
FREQ	Frequency	FREQ\FREQUENCY	Hertz	FREQUENCY
GAMMA	Voltage	GAMMAIBULK THRESHOLD PARAMETER		BULK THRESHOLD PARAMETER
IA	Current	IA	A	Maximum SCR anode current that a device can withstand
IB	Current	IB	A	Maximum base current that a device can withstand
IB_NPN	Current	IB	A	Maximum base current that a NPN BJT can withstand
IB_PNP	Current	IB	A	Maximum base current that a PNP BJT can withstand
IBV	Current	IBVICURRENT AT BREAKDOWN VOLTAGE		CURRENT AT BREAKDOWN VOLTAGE
IC	Current	IC\CONTINUOUS_CURRENT	A	Maximum collector current that a device can withstand
IC_NPN	Current	IC	A	Maximum collector current that a NPN BJT can withstand
IC_PNP	Current	IC	A	Maximum collector current that a PNP BJT can withstand
ID	Current	ID\CONTINUOUS_CURRENT	A	Maximum drain current that a device can withstand

Design Integrity and Analysis in Allegro X System Capture

Pattern Matching

Parameter	Type	Property Alias	Unit	Description
ID_NMOS	Current	ID	A	Maximum drain current that a N-Channel MOS can withstand
ID_PMOs	Current	ID	A	Maximum drain current that a P-Channel MOS can withstand
IF	Current	IFCONTINUOUS_CURRENT	A	Maximum forward current that a device can withstand
IFD	Current	IF	A	Maximum forward current that a diode can withstand
IG	Current	IG	A	Maximum gate current that a device can withstand
IG_NMOS	Current	IG	A	Maximum gate current that a N-Channel MOS can withstand
IG_PMOs	Current	IG	A	Maximum gate current that a P-Channel MOS can withstand
IMINUS	Current	IMINUS	A	Maximum inverting input current that a device can withstand
IOUT	Current	IOUT	A	Maximum output current that a device can withstand
IPLUS	Current	IPLUS	A	Maximum non-inverting input current that a device can withstand
IRMX	Current	IR	A	Maximum reverse current that a device can withstand
IS	Current	ISISATURATION_CURRENT		SATURATION CURRENT
ITM	Current	ITM	A	Maximum peak single pulse transient current that a device can withstand
IV	Voltage	IV	V	Maximum voltage that a current source can withstand
KF		KFFLICKER NOISE COEFFICIENT		FLICKER NOISE COEFFICIENT

Design Integrity and Analysis in Allegro X System Capture

Pattern Matching

Parameter	Type	Property Alias	Unit	Description
KP	TRANSCONDUCTANCE	KPITRANSCONDUCTANCE		TRANSCONDUCTANCE PARAMETER
L	Inductance	LIINDUCTANCE		INDUCTANCE
LAMBDA	1/Voltage	LAMBDACHANNEL-LENGTH MODULATION		CHANNEL-LENGTH MODULATION
LEVEL		LEVEL		SPICE MODEL LEVEL
LI	Current	Current	A	Maximum current rating that an inductor can withstand
LIDC	Current	Current	A	Maximum DC current rating that an inductor can withstand
LV	Voltage	VoltageMAX_VOLTAGE	V	Maximum voltage rating that an inductor can withstand
N		NIIDEALITY FACTOR		IDEALITY FACTOR
NF	Current	NFIFORWARD CURRENT EMISSION COEFFICIENT		FORWARD CURRENT EMISSION COEFFICIENT
PB	Voltage	PBIBULK JUNCTION POTENTIAL		BULK JUNCTION POTENTIAL
PDM	Power	PowerMAX_WATTAGE	W	Maximum power dissipation supported by the device
PDM_NMOS	Power	Power	W	Maximum power dissipation supported by N-Channel MOS
PDM_PMOS	Power	Power	W	Maximum power dissipation supported by P-Channel MOS
PDML	Power	Power	W	Maximum power loss supported by a device
PHI	Voltage	PHISURFACE POTENTIAL		SURFACE POTENTIAL

Design Integrity and Analysis in Allegro X System Capture

Pattern Matching

Parameter	Type	Property Alias	Unit	Description
RCA	Thermal Resistance	RCA	°C/W	Maximum thermal resistance (Case-To-Ambient) supported by the device
RCOIL	Resistance	RCOILICOIL RESISTANCE		RELAY COIL RESISTANCE
RCONTACT	Resistance	RCONTACTICONTACT RESISTANCE		RELAY CONTACT RESISTANCE
RD	Resistance	DIRSERISeries resistance Parasitic resistance Ohmic resistance		DRAIN SERIES RESISTANCE
RDC	Resistance	RDCIDCRIRSERISeries resistance Parasitic resistance Ohmic resistance		
RJA	Thermal Resistance	RJA	°C/W	Maximum thermal resistance (Junction-To-Ambient) supported by the device
RJC	Thermal Resistance	RJC	C	Maximum thermal resistance (Junction-To-Case) supported by the device
RJB	Thermal Resistance	RJB		
RS	Resistance	SIRSERISeries resistance Parasitic resistance Ohmic resistance		SOURCE SERIES RESISTANCE
RV	Voltage	Voltage MAX_VOLTA GE RATED_VOLTAGE_MAXIMUM	V	Maximum voltage rating supported by the device
SBINT	Current	SBINT	A	Maximum secondary breakdown intercept that a device can withstand
TAU	TIME	TAUIAMBIOPOLAR RECOMBINATION LIFETIME	s	AMBIOPOLAR RECOMBINATION LIFETIME

Design Integrity and Analysis in Allegro X System Capture

Pattern Matching

Parameter	Type	Property Alias	Unit	Description
TB	Temperature	TJIMAX_TEMP	C	Maximum temperature that a resistor can withstand
TBRK	Temperature	TJ	C	Maximum breakdown temperature that a device can withstand
TJ	Temperature	TJ	C	Maximum junction temperature supported by the device
TMAX	Temperature	TJIMAX_TEMP	C	Maximum temperature supported by the device
VAC	Voltage	VAC	V	Maximum anode-to-cathode voltage that a device can withstand
VAF	Voltage	VAFIEARLYVOLTAGE	V	FORWARD EARLY VOLTAGE
VCB	Voltage	VCB	V	Maximum collector-to-base voltage that a device can withstand
VCB_NPN	Voltage	VCB	V	Maximum collector-to-base voltage that a NPN BJT can withstand
VCB_PNP	Voltage	VCB	V	Maximum collector-to-base voltage that a PNP BJT can withstand
VCBO	Voltage	VCBO	V	Maximum collector-to-base voltage with open emitter that a BJT can withstand
VCE	Voltage	VCEIMAX_VOLTAGE	V	Maximum collector-to-emitter voltage that a device can withstand
VCE_NPN	Voltage	VCE	V	Maximum collector-to-emitter voltage that a NPN BJT can withstand
VCE_PNP	Voltage	VCE	V	Maximum collector-to-emitter voltage that a PNP BJT can withstand

Design Integrity and Analysis in Allegro X System Capture

Pattern Matching

Parameter	Type	Property Alias	Unit	Description
VCEO	Voltage	VCEO	V	Maximum collector-to-emitter voltage with open base that a BJT can withstand
VCG	Voltage	VCG	V	Maximum collector-to-gate voltage that a device can withstand
VD	Voltage	VD	V	Maximum forward voltage that a device can withstand
VDG	Voltage	VDG	V	Maximum drain-to-gate voltage that a device can withstand
VDG_NMOS	Voltage	VDG	V	Maximum drain-to-gate voltage that a N-Channel MOS can withstand
VDG_PMO	Voltage	VDG	V	Maximum drain-to-gate voltage that a P-Channel MOS can withstand
VDIFF	Voltage	VDIFF	V	Maximum differential input voltage that a device can withstand
VDS	Voltage	VDSIMAX_VOLTAGE VOLTAGE	V	Maximum drain-to-source voltage that a device can withstand
VEB	Voltage	VEB VBE_GS	V	Maximum emitter-to-base voltage that a device can withstand
VEB_NPN	Voltage	VEB	V	Maximum emitter-to-base voltage that a NPN BJT can withstand
VEB_PNP	Voltage	VEB	V	Maximum emitter-to-base voltage that a PNP BJT can withstand
VEBO	Voltage	VEB	V	Maximum emitter-to-base voltage with open collector that a device can withstand

Design Integrity and Analysis in Allegro X System Capture

Pattern Matching

Parameter	Type	Property Alias	Unit	Description
VECO	Voltage	VEC	V	Maximum emitter-to-collector voltage with open base that a device can withstand
VGEF	Voltage	VGEF	V	Maximum forward gate-to-emitter voltage that a device can withstand
VGER	Voltage	VGER	V	Maximum reverse gate-to-emitter voltage that a device can withstand
VGS	Voltage	VGS	V	Maximum gate-to-source voltage that a device can withstand
VGSF	Voltage	VGSF	V	Maximum forward gate-to-source voltage that a device can withstand
VGSF_NMOS	Voltage	VGSF	V	Maximum forward gate-to-source voltage that a N-Channel MOS can withstand
VGSF_PMOS	Voltage	VGSF	V	Maximum forward gate-to-source voltage that a P-Channel MOS can withstand
VGSR	Voltage	VGSR	V	Maximum reverse gate-to-source voltage that a device can withstand
VGSR_NMOS	Voltage	VGSR	V	Maximum reverse voltage that a N-Channel MOS can withstand
VGSR_PMOS	Voltage	VGSR	V	Maximum reverse voltage that a P-Channel MOS can withstand
VI	Current	VI	A	Maximum current that a voltage source can withstand
VINMAX	Voltage	VIN_MAX	V	Maximum input voltage that a device can withstand

Design Integrity and Analysis in Allegro X System Capture

Pattern Matching

Parameter	Type	Property Alias	Unit	Description
VPMAX	Voltage	VIN_MAX	V	Maximum input voltage (non-inverting) that a device can withstand
VPMIN	Voltage	VIN_MIN	V	Minimum input voltage (non-inverting) that a device can withstand
VR	Voltage	VRIMAX_VOLTAGE REVERSE_VOLTAGE	V	Maximum reverse voltage that a device can withstand
VSD	Voltage	VSDIMAX_VOLTAGE VOLTAGE	V	Maximum source-to-drain voltage that a device can withstand
VSMAX	Voltage	VCC_MAX	V	Maximum supply voltage that a device can withstand
VSMIN	Voltage	VCC_MIN	V	Minimum supply voltage that a device can withstand
VT	Voltage	VTITHRESHOLD_VOLTAGE		THRESHOLD VOLTAGE
VTD	Voltage	VTDIGATE-DRAIN_OVERLAP_DEPLETION_THRESHOLD DIG-D_OVERLAP_DEPLETION_THRESHOLD		GATE-DRAIN OVERLAP DEPLETION THRESHOLD
VTO	Voltage	VTOITHRESHOLD_VOLTAGE	V	THRESHOLD VOLTAGE
WB	WIDTH	WBIWIDTH	m	Metallurgical base width

Related Topics

- [Configuring Schematic Audit Settings](#)
- [Design Analyses](#)

Design Integrity and Analysis in Allegro X System Capture
Pattern Matching

Reference Designator Prefixes or Patterns to Recognize Devices

Device Type	Reference Designator Prefixes/Patterns
Varistor	"RV.*"
Thermistor	"RT.* NTC.* PTC.*"
Resistor	"R[^TV].*"
Current Sense Resistor	"R[^TV].*"
Capacitor	"C[^R]+.*"
Inductor	"L.*"
Bead	"FB.* E.*"
Diode	"D.* CR.* V.* OP.* LED.*"
Bidirectional TVS Diode	"D.* CR.*"
Dual Schottky Diodes in Series	"D.*"
Dual Diodes Common Cathode	"D.*"
Dual Diodes Common Anode	"D.*"
Dual Diodes in Single Configuration	"D.*"
RGB LED Diode	"D.*"
Dual LED Diode	"DS.* DLED.*"
Rail Clamp Diode (TVS diode array for ESD protection)	"CR.*"
MOSFET	"M.* Q.* N.*"
MOSFETCommonDrain	"M.* Q.* N.*"
BJT	"Q.*"
JFET	"Q.*"
Optocoupler	"Q.*"
Fuse	"F[^BL].*"
Connector	"J.* P.* CN.* HDR.*"
IGBT	"Q.* Z.*"
Thyristor	"D.* X.* Q.*"
Triac	"X.* Q.*"

Design Integrity and Analysis in Allegro X System Capture

Pattern Matching

Device Type	Reference Designator Prefixes/Patterns
Filter	"FL.* C.*"
Relay	"K.* REL.* RLY.*"
Transformer	"TX.* TR.* T.* XMER.*"
Jumper	"W.* JP.*"
General Opamp	"U.* OP.*"
Switch	"S[^PKEP].* SW.* "
IC	"U.* IC.* VR.*"
Mechanical device	"TP.* BP.* SP.* SEP.* SK.* TPOL.* TPAD.* MP.* Y.* G.* XTAL.* FD.* FID.* MH.* ZT.* ZH.* BS.* SP.* SV.* VV.* X.* LB.* FM.* H.* E.* A.*"

Related Topics

- [Configuring Electrical Stress Settings](#)
- [Design Analyses](#)

Term Order Matching Patterns

Bead	pin_id="A" mandatory="yes" matching patterns="A.* P_1 P1 P \+ PLUS IO1 1" pin_id="B" mandatory="yes" matching patterns="B.* Y.* P_2 P2 NIMI-IMINUS IO2 2"
BidirectionalTVS (Bidirectional TVS Diode)	pin_id="A1" mandatory="yes" matching patterns="ANODE1 AN1 P_1 P1 P1_1 AC1.* A1 1 IO1" pin_id="A2" mandatory="yes" matching patterns="ANODE2 AN1 P_2 P2 P1_2 AC2.* A2 2 IO2"

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Pattern Matching

BJT	<p>pin_id="C" mandatory="yes" matching patterns="C C.[0-9]. COLLECTOR 3"</p> <p>pin_id="B" mandatory="yes" matching patterns="B B.[0-9]. BASE 1"</p> <p>pin_id="E" mandatory="yes" matching patterns="E E.[0-9]. EMITTER 2"</p> <p>pin_id="S" mandatory="no" matching patterns="SUB SUBSTRATE BULK 4"</p>
Capacitor	<p>pin_id="A" mandatory="yes" matching patterns="A.* P_1 P1 P \+ PLUS O1 C1.* 1"</p> <p>pin_id="Y" mandatory="yes" matching patterns="B.* P_2 P2 NI- MINUS O2 C2.* Y.* K.* 2"</p> <p>pin_id="C" mandatory="no" matching patterns="C GND P_3 P3 C3.* 3"</p>
CurrentSenseResistor	<p>pin_id="I" mandatory="yes" matching patterns="I 1"</p> <p>pin_id="V" mandatory="yes" matching patterns="V IS1"</p> <p>pin_id="I1" mandatory="yes" matching patterns="I1 2"</p> <p>pin_id="V1" mandatory="yes" matching patterns="V1 IS2"</p>
Diode	<p>pin_id="A" mandatory="yes" matching patterns="ANODE AN P_1 P1 P1_1 \+ PLUS AC1.* A 1 O1 A[1-9]"</p> <p>pin_id="K" mandatory="yes" matching patterns="C.* K.* CATHODE CAT P_2 P2 P1_2 Y - MINUS AC2.* B 2 O2 C[1-9]"</p>
DualDiodeCommonAnode:	<p>pin_id="A" mandatory="yes" matching patterns="ANODE AN A GND 3"</p> <p>pin_id="K1" mandatory="yes" matching patterns="CATHODE1 CAT1 C1 K1 AC1 2"</p> <p>pin_id="K2" mandatory="yes" matching patterns="CATHODE2 CAT2 C2 C K2 AC2 1"</p>

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Pattern Matching

DualDiodeCommonCathode	<p>pin_id="A1" mandatory="yes" matching patterns="ANODE1 AN1 A1"</p> <p>pin_id="A2" mandatory="yes" matching patterns="ANODE2 AN2 A2"</p> <p>pin_id="K" mandatory="yes" matching patterns="CATHODE CATICICCIK"</p>
DualDiodeSeries	<p>pin_id="A" mandatory="yes" matching patterns="ANODE ANIA"</p> <p>pin_id="K" mandatory="yes" matching patterns="CATHODE CATICIK"</p> <p>pin_id="KA" mandatory="yes" matching patterns="KAIKICA AC"</p>
DualDiodeSingleConfig (Schottky Diodes in Single Configuration)	<p>pin_id="A" mandatory="yes" matching patterns="ANODE ANIA"</p> <p>pin_id="K" mandatory="yes" matching patterns="CATHODE CATICIK"</p> <p>pin_id="NC" mandatory="yes" matching patterns="NC CA AC"</p>
DualLED (Dual LED Diode)	<p>pin_id="A1" mandatory="yes" matching patterns="ANODE1 AN1 A1 A"</p> <p>pin_id="K1" mandatory="yes" matching patterns="CATHODE1 CAT1 C1 K1 CIK"</p> <p>pin_id="A2" mandatory="yes" matching patterns="ANODE2 AN2 A2"</p> <p>pin_id="K2" mandatory="yes" matching patterns="CATHODE2 CAT2 C2 K2"</p>
Filter	<p>pin_id="1" mandatory="yes" matching patterns="A.* P_1 P1 P \+ PLUSIC1.* I1 IN IRF1"</p> <p>pin_id="2" mandatory="yes" matching patterns="B.* P_2 P2 NI- IM MINUSIC2.* Y.* K.* I2 OUTIRF2"</p> <p>pin_id="3" mandatory="yes" matching patterns="C GND GND1 G1 P_3 P3 C3.* I3"</p> <p>pin_id="4" mandatory="no" matching patterns="D GND2 G2 P_4 P4 C4.* I4"</p>

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Pattern Matching

Fuse	pin_id="A" mandatory="yes" matching patterns="A.* P.* \+ PLUS IO1 1" pin_id="B" mandatory="yes" matching patterns="B.* N.* \- MINUS IO2 2"
GeneralOpAmp	pin_id="INV" mandatory="yes" matching patterns="INVERTING.* INV MINUS \- INN IN \- VINN" pin_id="NINV" mandatory="yes" matching patterns="NONINVERTING.* NON \- INVERTING.* IN INV PLUS \+ INP IN \+ VIN \+ VNP" pin_id="V+" mandatory="yes" matching patterns="V\+ VCC VPOS" pin_id="V-" mandatory="yes" matching patterns="V\ - VEE VNEG" pin_id="OUT" mandatory="yes" matching patterns="OUTPUT OUTIO" pin_id="OS1" mandatory="no" matching patterns="OS1 OFFSETNULL1 OFFSET_NULL1" pin_id="OS2" mandatory="no" matching patterns="OS2 OFFSETNULL2 OFFSET_NULL2"
IGBT	pin_id="C" mandatory="yes" matching patterns="C COLLECTOR 3" pin_id="G" mandatory="yes" matching patterns="G GATE 1" pin_id="E" mandatory="yes" matching patterns="E EMITTER 2"
Inductor	pin_id="A" mandatory="yes" matching patterns="A.* P_1 P1 P \+ PLUS IO1 1" pin_id="B" mandatory="yes" matching patterns="B.* Y.* P_2 P2 IN MI \- MINUS IO2 2"
JFET	pin_id="D" mandatory="yes" matching patterns="D DRAIN 1" pin_id="G" mandatory="yes" matching patterns="G GATE 2" pin_id="S" mandatory="yes" matching patterns="S SOURCE 3"
Jumper	pin_id="A" mandatory="yes" matching patterns="A.* P.* \+ PLUS 1" pin_id="B" mandatory="yes" matching patterns="B.* N.* \- MINUS 2"

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Pattern Matching

MOSFET	pin_id="D" mandatory="yes" matching patterns="D DRAIN 2" pin_id="G" mandatory="yes" matching patterns="G GATE 1" pin_id="S" mandatory="yes" matching patterns="S SOURCE 3" pin_id="B" mandatory="no" matching patterns="SUB SUBSTRATE BULK 4"
MOSFETCommonDrain (Power PMOS and MNOS)	pin_id="D1" mandatory="yes" matching patterns="D1 DRAIN1 1" pin_id="D2" mandatory="yes" matching patterns="D2 DRAIN2 2" pin_id="D3" mandatory="no" matching patterns="D5 DRAIN5 5" pin_id="D4" mandatory="no" matching patterns="D6 DRAIN6 6" pin_id="G" mandatory="yes" matching patterns="G GATE 3" pin_id="S" mandatory="yes" matching patterns="S SOURCE 4"
Optocoupler	pin_id="A" mandatory="yes" matching patterns="A DIODE + PLUS 1" pin_id="K" mandatory="yes" matching patterns="K Y B CATHODE - MINUS 2" pin_id="E" mandatory="yes" matching patterns="E A EMITTER 3" pin_id="C" mandatory="yes" matching patterns="C COLLECTOR 3"
RailClampDiode	pin_id="IO1" mandatory="yes" matching patterns="IO1 1" pin_id="IO2" mandatory="yes" matching patterns="IO2 6" pin_id="IO3" mandatory="yes" matching patterns="IO3 3" pin_id="IO4" mandatory="yes" matching patterns="IO4 4" pin_id="VSS" mandatory="yes" matching patterns="VSS VI5" pin_id="GND" mandatory="yes" matching patterns="GND GI2"

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Pattern Matching

Relay	pin_id="A" mandatory="yes" matching patterns="A.* 1" pin_id="B" mandatory="yes" matching patterns="B.* 2" pin_id="NC" mandatory="yes" matching patterns="NC.* 3" pin_id="NO" mandatory="yes" matching patterns="NO.* 4" pin_id="COM" mandatory="no" matching patterns="COM.* 5"
Resistor	pin_id="A" mandatory="yes" matching patterns="A.* P_1 P1 P \+ PLUS 1 IO1" pin_id="B" mandatory="yes" matching patterns="B.* Y.* P_2 P2 NI- MINUS 2 IO2"
RGBLED (RGB LED Diode)	pin_id="A" mandatory="yes" matching patterns="ANODE COMMON\ ANODE COMMON_ANODE COMMON.* CA ACIA" pin_id="R" mandatory="yes" matching patterns="CATHODE1 RED\ sCATHODE RED_CATHODE RED.* RCIR" pin_id="G" mandatory="yes" matching patterns="CATHODE2 GREEN\ sCATHODE GREEN_CATHODE GREEN.* GCIG" pin_id="B" mandatory="yes" matching patterns="CATHODE3 BLUE\ sCATHODE BLUE_CATHODE BLUE.* BCIB"
Thermistor	pin_id="A" mandatory="yes" matching patterns="A.* P.* \+ PLUS IO1 1" pin_id="B" mandatory="yes" matching patterns="B.* N.* I- MINUS IO2 2"
Thyristor	pin_id="A" mandatory="yes" matching patterns="A.* ANODE AN \+ PLUS AC1.* 1" pin_id="K" mandatory="yes" matching patterns="C.* CATHODE CAT Y K1 I- MINUS AC2.* 2" pin_id="G" mandatory="yes" matching patterns="G.* GATE GT 3"

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Pattern Matching

Transformer	pin_id="1" mandatory="yes" matching patterns="P1.*IP_1.*IA1.*I1" pin_id="2" mandatory="yes" matching patterns="P2.*IP_2.*IA2.*I2" pin_id="3" mandatory="yes" matching patterns="P3.*IP_3.*IA3.*I3" pin_id="4" mandatory="yes" matching patterns="P4.*IP_4.*IA4.*I4" pin_id="5" mandatory="no" matching patterns="P5.*IP_5.*IS1.*IA5.*I5" pin_id="6" mandatory="no" matching patterns="P6.*IP_6.*IS2.*IA6.*I6"
Triac	pin_id="A" mandatory="yes" matching patterns="A.*IANODE ANI\+ PLUSIAC1.*I1 MT1" pin_id="K" mandatory="yes" matching patterns="C.*ICATHODE CAT YIIK1 -MINUSIAC2.*I2 MT2" pin_id="G" mandatory="no" matching patterns="G.*IGATE GT 3"
Varistor	pin_id="A" mandatory="yes" matching patterns="A.*IANODE ANI\+ PLUSIAC1.*I1" pin_id="K" mandatory="yes" matching patterns="C.*ICATHODE CAT YIIK1 -MINUSIAC2.*I2"

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