cadence®

Allegro®
Constraint Manager with Design Entry HDL Tutorial

Product Version 23.1
September 2023

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Contents

1

Introduction to the Tutorial

The Allegro Constraint Manager with Design Entry HDL tutorial describes the different types of electrical constraints you can capture in Constraint Manager. You learn to capture them in Constraint Manager and keep them synchronized in Design Entry HDL. The tutorial also highlights the tight integration between Constraint Manager, Design Entry HDL, and PCB Editor. You set constraints while creating the schematic in Design Entry HDL and then propagate them to the board in PCB Editor through Constraint Manager.

A constraint is a user-defined restriction applied to an object when it is routed and placed on the board. An electrical constraint (EC) restricts the electrical behavior of an object on the printed circuit board. For example, you can specify that a net can have a maximum propagation delay of 2 ns for a circuit to function properly.

The tutorial focuses on the following procedures:

- Capturing ECs in Constraint Manager
- Performing Engineering Change Orders (ECOs) in Design Entry HDL and Constraint Manager
- Propagating ECs back and forth between Design Entry HDL and PCB Editor

Audience

This tutorial is designed for first-time users of Constraint Manager from Design Entry HDL. If you are a schematic designer, you might want to capture ECs while implementing the logic of your design. Constraint Manager, when connected to Design Entry HDL, helps you capture these constraints and ensures that the properties in Design Entry HDL are synchronized with their corresponding electrical constraints in Constraint Manager, and conversely.

Prerequisites

It is assumed that you are familiar with Design Entry HDL and PCB Editor but not with Constraint Manager. The scope of this tutorial does not include details of various modes and

properties in Design Entry HDL or PCB Editor but will cover Constraint Manager procedures in detail.

Note: To learn about Design Entry HDL or PCB Editor, see the *Allegro Design Entry HDL User Guide* and the *Allegro X PCB and Package User Guide: Getting Started with Physical Design*.

Tip

You can watch the multimedia demonstrations about the Design Entry HDL - Constraint Manager flow to quickly understand the main features of the flow on the *SPB Video Library Page* on Cadence Online Support.

Advantages of Using Constraint Manager with Design Entry HDL

In Design Entry HDL, you used the Attributes dialog box to set restrictions in the form of properties on objects. A property is captured as a name-value pair. This requires you to be familiar with the syntax of properties. No syntax checking is performed while a property is being added and a property with incorrect syntax is not added to an object. As a result, multiple rounds are sometimes required to add one property.

Constraint Manager is a spreadsheet-based application with an easy-to-use interface for entering constraints, which are equivalent to Design Entry HDL properties. Constraint Manager checks the syntax of a constraint while it is being added, thus simplifying your task.

Another advantage of using Constraint Manager is that it allows you to create generic constraints that you can apply to multiple nets or Xnets at the same time. At a later point in time, if your design requirements change, you can edit the generic rule. The updated rule will be automatically applied to the nets or Xnets that refer to the rule.

Using the Tutorial

To use the Allegro Constraint Manager with Design Entry HDL tutorial, you need the following tools and Tutorial Database:

- Allegro Project Manager
- Design Entry HDL
- Constraint Manager

- Signal Explorer
- PCB Editor

Tutorial Database

To run the tutorial, you need to unzip the design files and copy them to your local machine. The design files contain the schematics and the other files required to perform the procedures explained in this tutorial.

Before using the tutorial, ensure that you do the following:

- Unzip the file <*your_inst_dir*>/doc/conCM_tut/tutorial_examples/project.zip on Windows NT, and save it locally to your work area.

  Ensure that the work area is a local directory for which you have write permissions.
- For the commands specified in the tutorial, you need to replace your work area with the name of the local directory in which you have copied the samples.
- Ensure that you unset the `CDS_SITE` environment variable on your computer if it is set.
- Ensure that the CONCEPT_INST_DIR variable points to the directory where you install the PCB tools.

Understanding the Tutorial Database Structure

The design database consists of the following directories and files:

Directory/File	Purpose
worklib	This is the project directory that contains all the schematics in the design; `ps0` is the top-level schematic.
lib	This directory contains all the libraries that have been used in creating the design.
part_tables	This directory contains the part table files for components instantiated in the design.
temp	This directory contains the temporary files that are created when you run various tools.

Directory/File	Purpose
cds.lib	This file defines the libraries that tools read to identify the libraries they can use. This file maps user library names to physical directory paths.
project.cpm	This is the Design Entry HDL project file.

Summary

The Allegro Constraint Manager with Design Entry HDL tutorial should be used by schematic designers who want to capture high-speed constraints while implementing the logic of the design. Constraint Manager lets you set constraints in a convenient, faster, and error-free manner.

What's Next

In the next chapter, Setting Routing Constraints on Nets, you will use Constraint Manager with Design Entry HDL for setting routing constraints. You will set the propagation delay constraint for a net, create pin-pairs, differential pairs and matched groups, and set constraints on them. You will also learn to view nets in canonical and physical formats in Constraint Manager.

Recommended Reading

For more information about the Constraint Manager tool, refer to *Allegro Constraint Manager User Guide* and *Allegro Design Entry HDL - Constraint Manager User Guide*. For information about how high-speed constraints are handled in the PCB flow, refer to *Allegro X PCB Design Flows.*

2

Setting Routing Constraints on Nets

Objectives

To learn how to set routing constraints on nets in your design using Constraint Manager and view the constraints in Design Entry HDL.

At the end of the lesson, you will be able to,

- navigate to a net.
- create a differential pair.
- set constraints on a differential pair.
- view a constraint in Design Entry HDL.
- create a pin-pair.
- create a match group.
- set the minimum and maximum delay for a net.
- set the delay for a net relative to another net.

Nature of Chapter

Skill (includes concepts and practice)

Estimated Completion Time

1.5 hours

Starting Design Entry HDL

Task Overview

You will start Project Manager and open the `project.cpm` file in it. Then you will start Design Entry HDL and view the schematic in it.

Steps

1. To open Project Manager, do one of the following:

   - Launch *Project Manager* from *Start – Cadence PCB 2023 – Project Manager 2023*.

   The Cadence Product Choices dialog box is displayed.

   Note: If you have set the default suite previously, the Design Entry HDL window opens automatically and you can skip step 2.

2. Select *Allegro Design Authoring.*

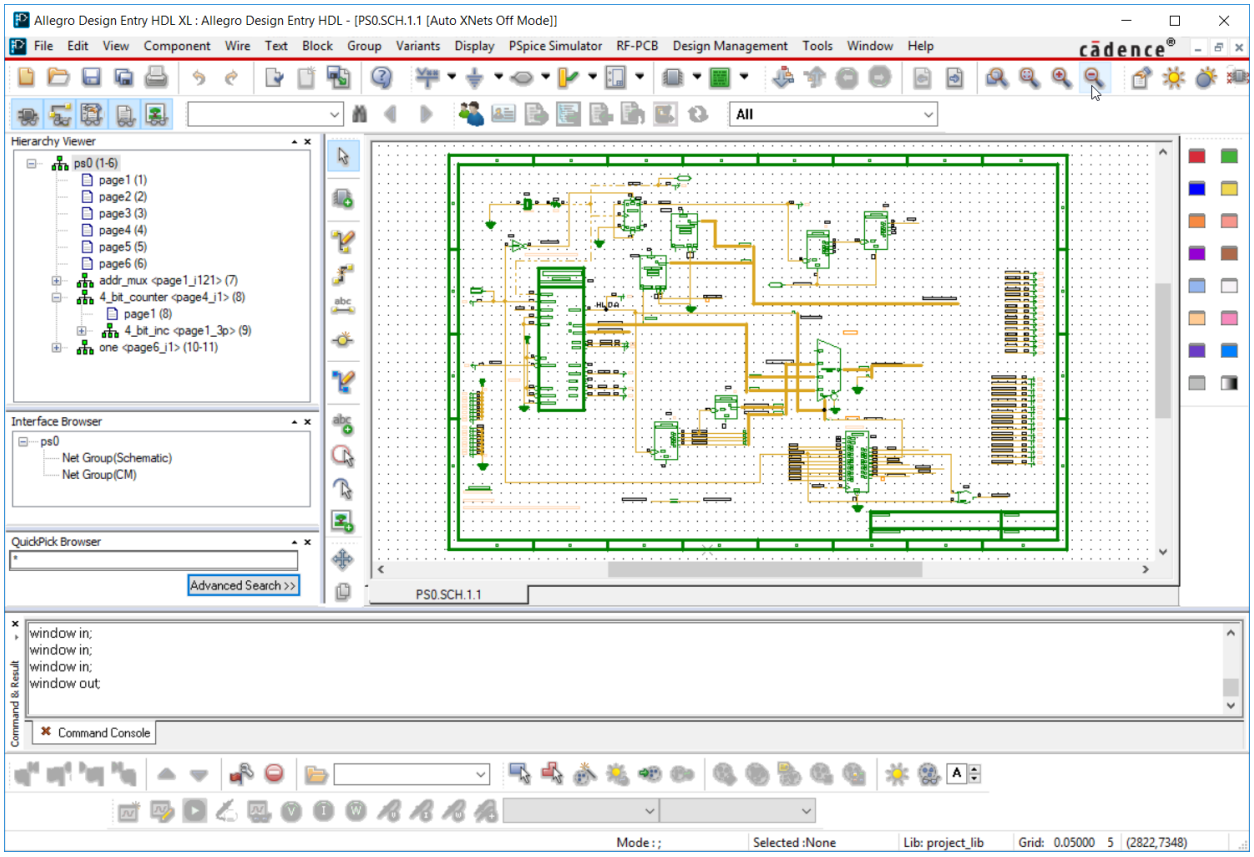
   The *Allegro Design Authoring: Allegro Project Manager* window appears.

3. Click *Open Project*.

4. Locate and open the `project.cpm` project file from your tutorial example directory.

5. Click the *Design Entry* button.

The Design Entry HDL window opens showing the schematic for `project.cpm` as follows:



Starting Constraint Manager

Task Overview

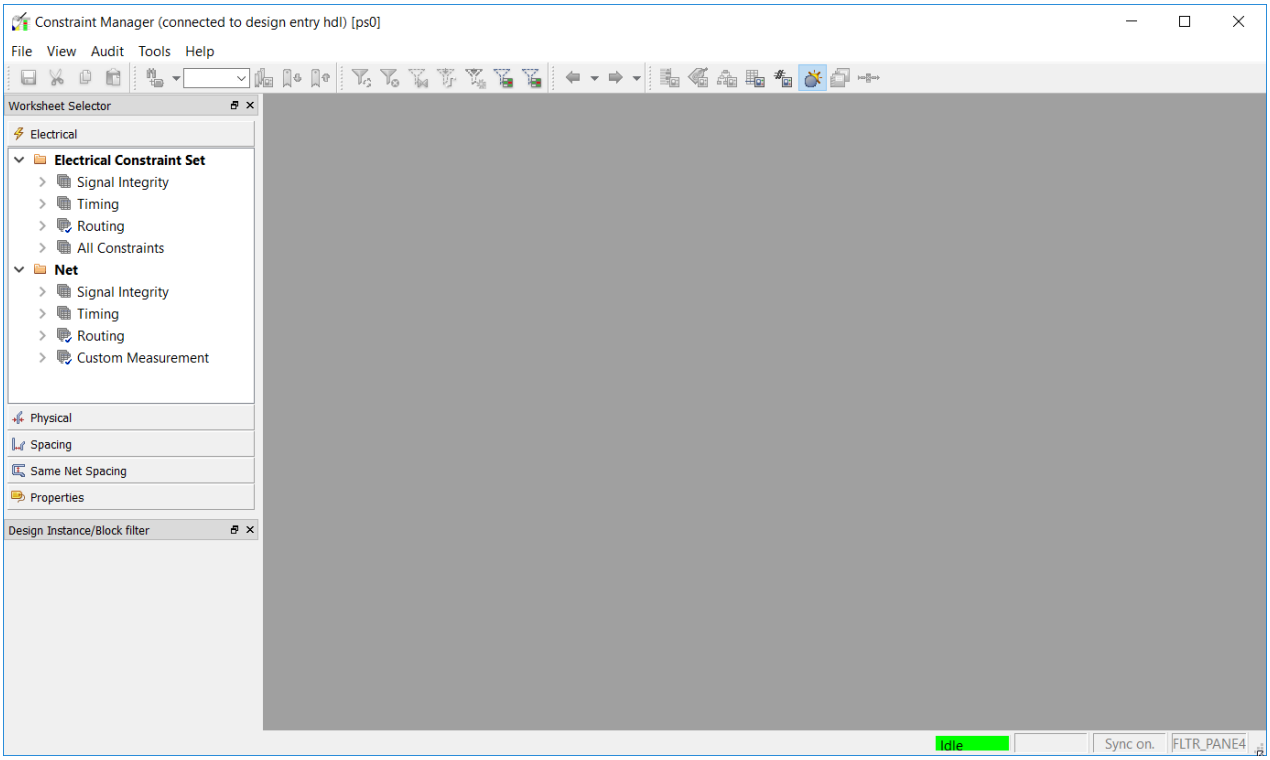
You will start Constraint Manager from Design Entry HDL and capture constraints on some nets in the schematic.

Steps

1. In Design Entry HDL, choose *Tools – Constraints – Edit*.

   The Constraint Manager window is displayed over the Design Entry HDL window. If the Constraint Manager window does not appear on top by itself, press *Ctrl + TAB* and

select Allegro Constraint Manager or click Allegro Constraint Manager in the taskbar to bring the window forward.



Note: The title bar of the Constraint Manager window shows that Constraint Manager is launched from Allegro Design Entry HDL.

For details on the Constraint Manager user interface, refer to *Constraint Manager User Interface* in the *Introduction to Constraint Manager* chapter in *Allegro Design Entry HDL - Constraint Manager User Guide*.

Video

Now watch this multimedia demonstration, *Starting Constraint Manager*, on Cadence Online Support.

Setting Constraints on Nets

In the Design Entry HDL-Constraint Manager flow, constraints are stored at a single location — the Constraint Manager database. To store a constraint or a property in the schematic, you need to add the `synch_props.cfg` property to a configuration file. This configuration file controls the synchronization of constraints between Design Entry HDL and Constraint Manager. The constraints listed in this file are considered as sync constraints and can be written on to the schematic. All the other constraints are considered non-sync and are pushed to Constraint Manager using the `Synchronize` utility.

Note: The `Synchronize` utility also facilitates migration of all pre-15.7 designs to the current design.

For more information on synchronization of constraints between Design Entry HDL and Constraint Manager, see the Synchronizing Constraints chapter of the *Allegro Design Entry HDL - Constraint Manager User Guide.*

Accessing the Differential Pair Worksheet

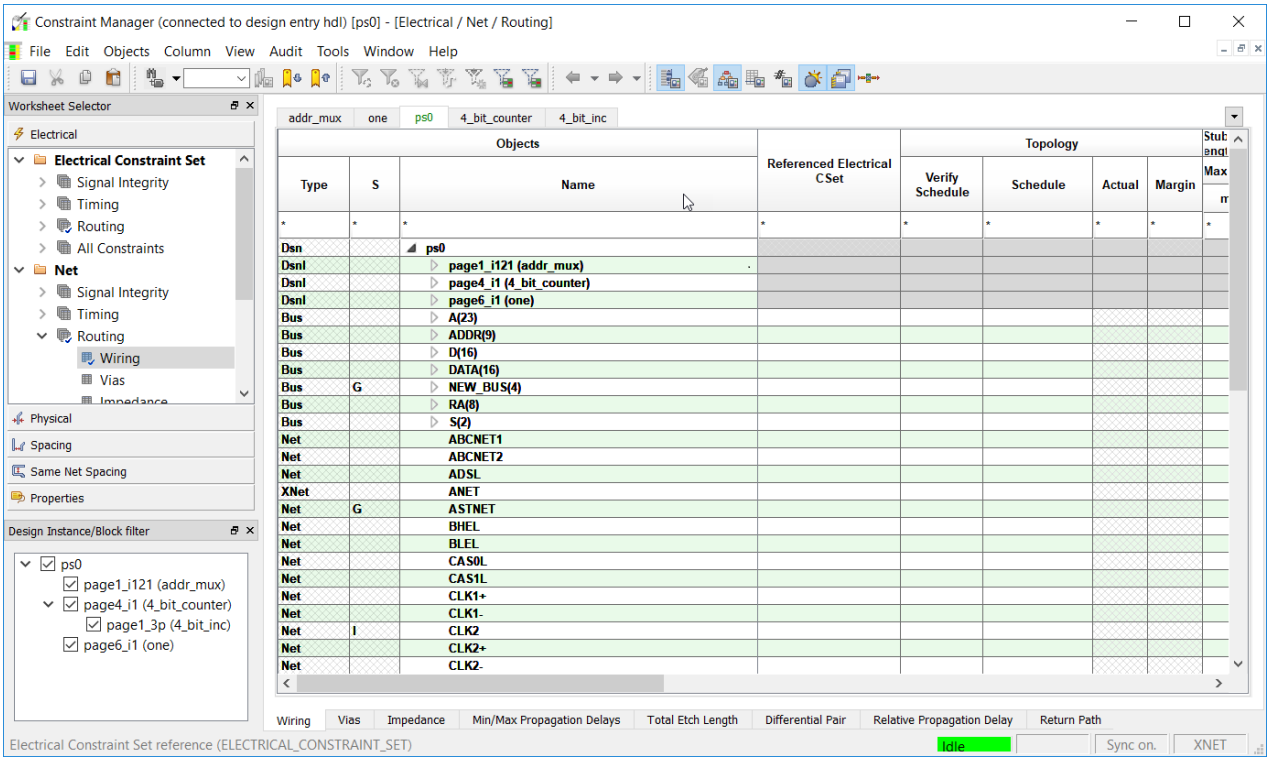
Task Overview

You will set a `DIFFERENTIAL PAIR` constraint on the `SIG1A` and `SIG1B` nets. This constraint is in the Differential Pair worksheet in the `Net` workbook.

Steps

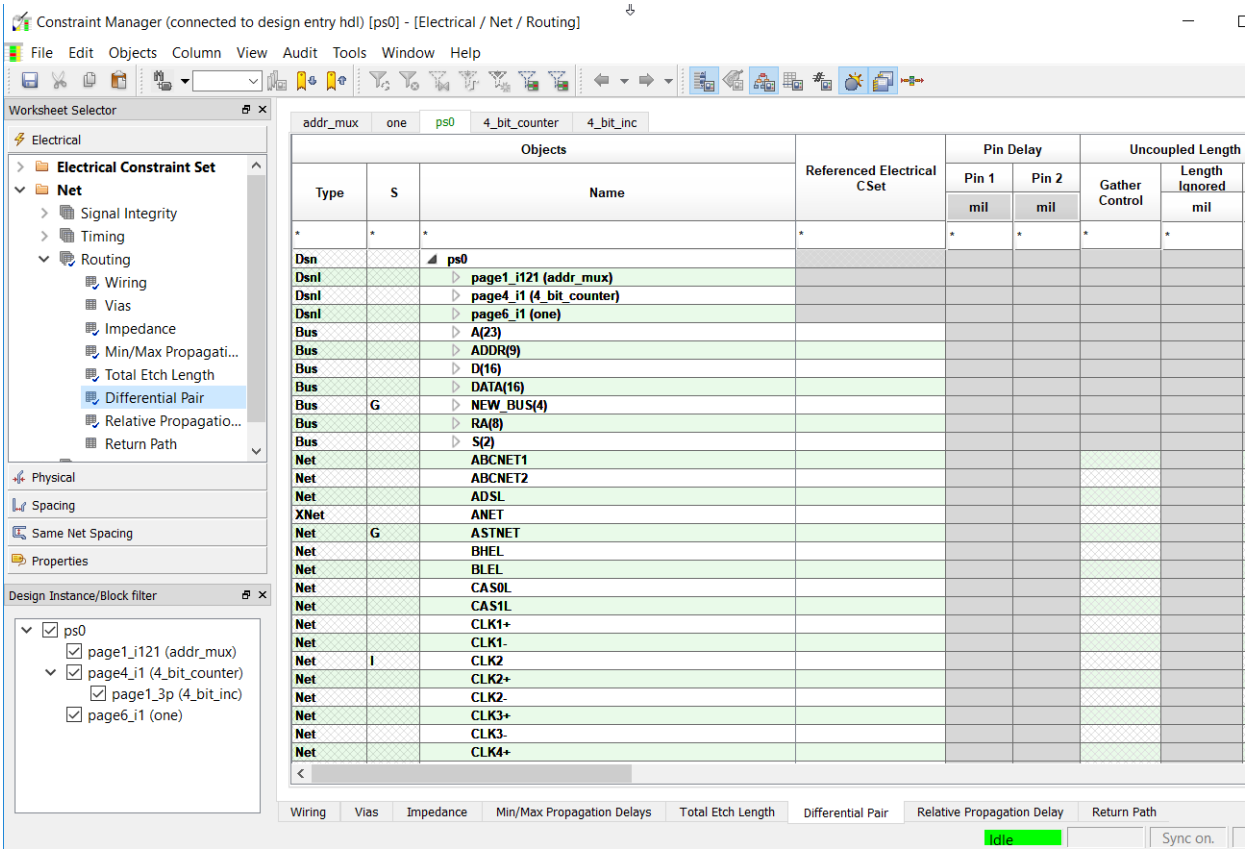
1. Select the *Net* workbook in the *Electrical* domain and click *Routing*.

The routing worksheet appears.



Note: The *Wiring, Vias, Impedance, Min/Max Propagation Delays, Total Etch Length, Differential Pair,* and *Relative Propagation Delay* tabs in this workbook.

2. Click the *Differential Pair* worksheet.



You can see that the nets are listed in their physical format in upper case. This is the default format of display in Constraint Manager if your design is packaged. If the design is not packaged, the nets are displayed in small case.

Navigating to a Net

When Constraint Manager is launched from Design Entry HDL, you can click an object in Design Entry HDL and it is highlighted in Constraint Manager. However, if you select an object in Constraint Manager and want it to be highlighted in Design Entry HDL, you need to right-click the object in Constraint Manager and choose *Select* from the pop-up menu.

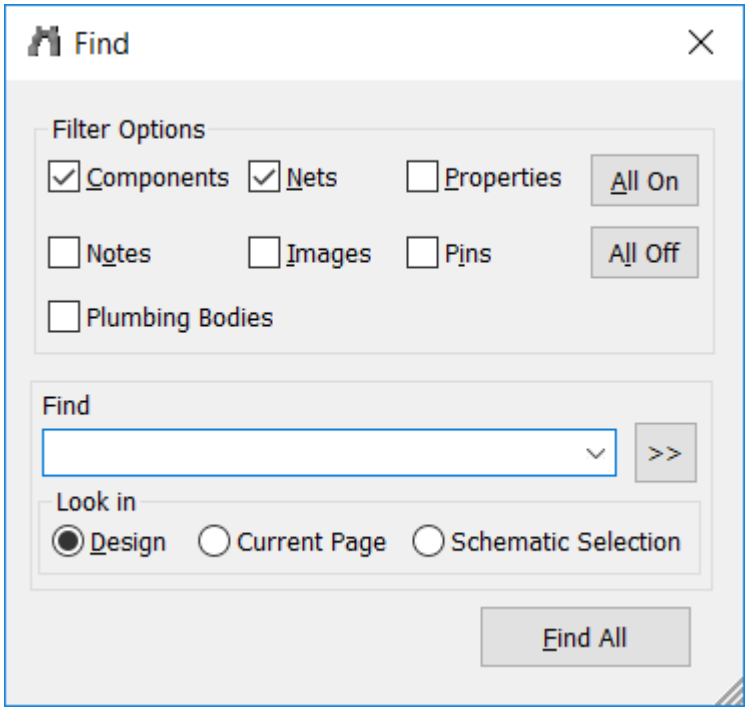
Task Overview

You will locate the `SIG1A` net in Design Entry HDL and highlight it. It will be automatically selected in Constraint Manager.

Steps

1. In Design Entry HDL, click *Search options* from the *Search Toolbar.*

   The *Find* dialog box appears.

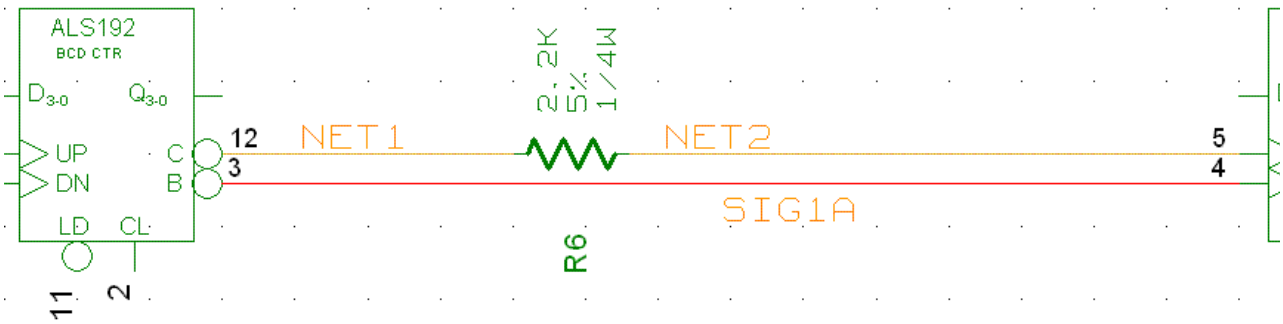


2. Enter the net name as `SIG1A` in the *Find* field. Ensure that the *Nets* checkbox is selected.
3. Click *Find All*.

   The instance of the `SIG1A` net is displayed in the Search *Results* window.
4. Double-click the highlighted result in the *Search Result* window.

   The net is selected in the Design Entry HDL.
5. Close the Find dialog box.

6. Click the `SIG1A` net on the canvas.



7. Click the Constraint Manager window.

The `SIG1A` net is selected.

Objects			Referenced Electrical CSet
Type	S	Name	
*	*	*	*
Net		CLK4-	
Net	I	CLRCNT	
Net		CLR_CNT	
Net		M_IO	
Net		NET1	
Net		NET2	
Net		NET3	
Net		NET4	
Net	G	ONE_GLB	
Net		PCLK	
Net		RASL	
Net		RDYL	
Net		REF	
Net	I	RESET	
Net		RESETL	
Net		ROMOEL	
Net		SIG1A	
Net		SIG1B	

Setting the Differential Pair Constraints on Nets

You can set constraints on nets in Constraint Manager. For example, you can create a Differential Pair for nets and set constraints on the differential pair so that the *Auto Router* routes them accordingly.

Creating a Differential Pair

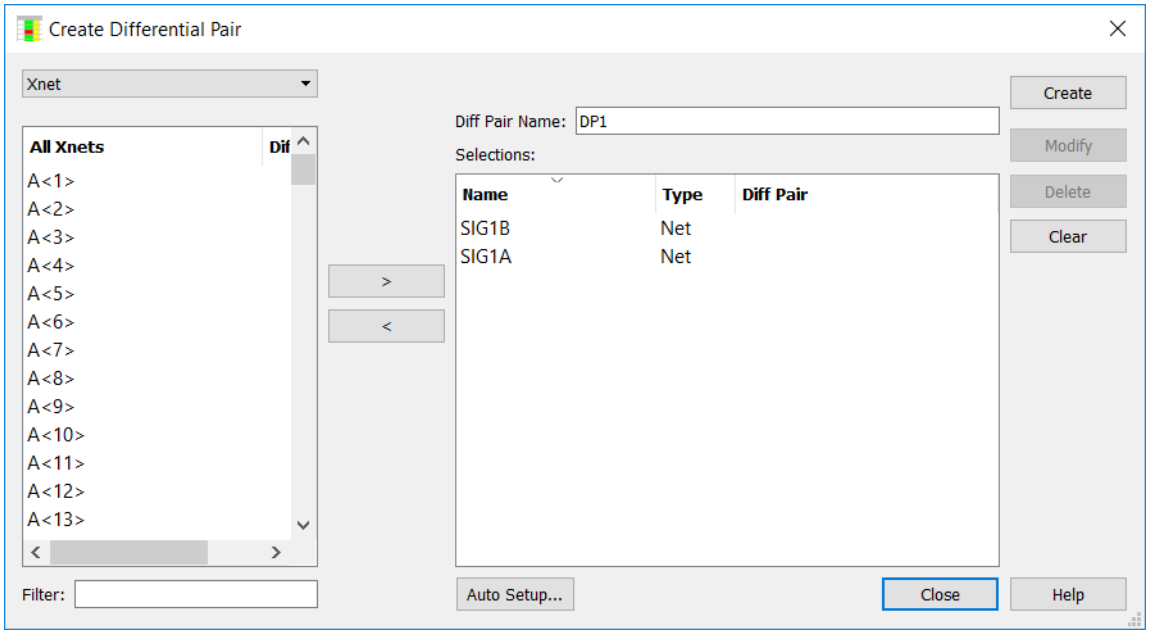
Task Overview

You will now create a differential pair with the `SIG1A` and `SIG1B` nets. Later, you will propagate the `DIFFERENTIAL_PAIR` property to the schematic canvas.

Steps

1. Select the *Net* workbook under *Electrical* domain.
2. Select the *Differential Pair* spreadsheet under *Routing* worksheet.
3. Select the `SIG1A` and `SIG1B` nets simultaneously.
4. Choose *Objects – Create – Differential Pair* from the Constraint Manager menu or right-click and choose *Create – Differential Pair* from the pop-up menu.

The *Create Differential Pair* dialog appears.

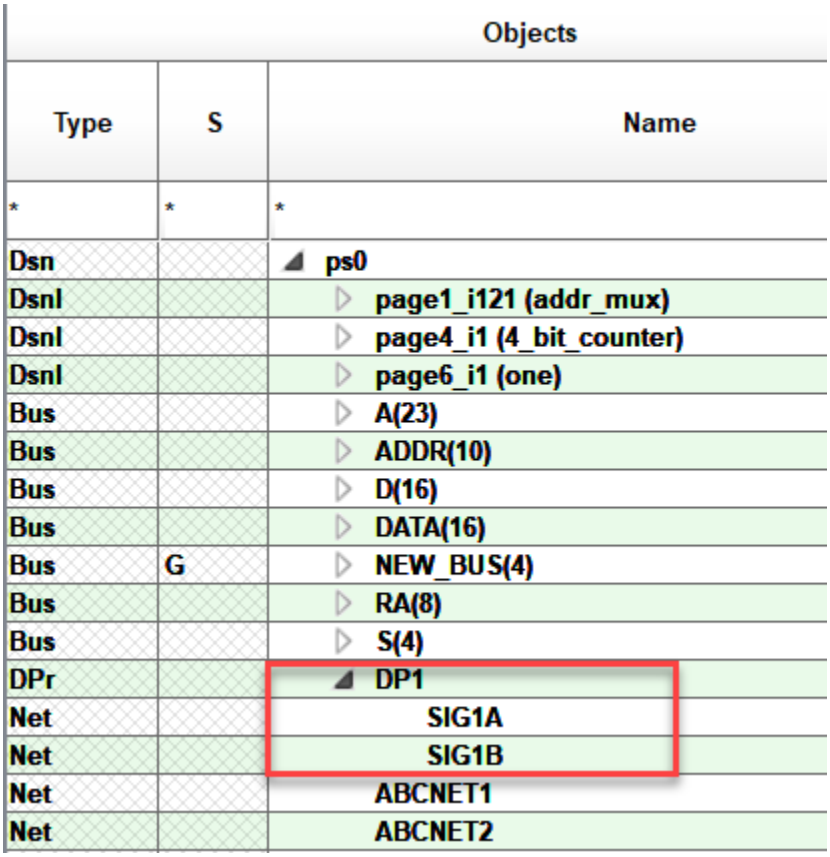


It contains the `SIG1A` and `SIG1B` nets in the *Selections* section indicating that these nets are members of the differential pair. A default name `DP1` appears in the *Diff Pair Name* field.

Note: If the nets forming a differential pair are of the form `A+` and `A-`, the name of the differential pair is set to `A`. For other pairs of nets, the name of the differential pair is of the form `DP`*`n`*.

5. Click *Create*.
6. Click *Close* to close the *Create Differential Pair* dialog.

The differential pair is created with the default name of DP1.



7. To change the default name, right-click *DP1* in the *Name* column and choose *Rename* or press `F2`.

   The *Rename Diff Pair* dialog box appears.

8. Type *DP1_SIG* in the *New Diff Pair Name* field and click *Ok*.

   The differential pair name is changed.

9. Choose *File – Save* to save the constraints in the Constraint Manager database.

   The Differential Pair constraint is mapped to the `DIFFERENTIAL_PAIR` property in Design Entry HDL.

10. Choose *File – Exit* to close Constraint Manager.

Video

Now watch this multimedia demonstration, *Creating Differential Pairs,* on Cadence Online Support.

Important

Before you move on to the next exercise, it is strongly recommended that you read the Synchronizing Constraints chapter of the *Allegro Design Entry HDL - Constraint Manager User Guide*.

Viewing the Constraint on the Schematic

The constraint that you added in Constraint Manager is added as an electrical constraint property in the occurrence property file of the design. For example, the `DIFFERENTIAL PAIR` constraint maps to the `DIFFERENTIAL_PAIR` electrical constraint property. For all mappings between constraints and properties, refer to Appendix F, "Property Mapping" of the *Allegro Design Entry HDL - Constraint Manager User Guide*.

The constraint will not be automatically visible on the schematic sheet. To view the constraint on the schematic, make the corresponding electrical constraint property visible using the *Attributes* dialog box in Design Entry HDL.

The `DIFFERENTIAL_PAIR` constraint is a sync constraint. Therefore, it can be written on to the schematic canvas.

Note: To learn how to write non-sync constraints on the schematic canvas, refer to the Synchronizing Constraints chapter of the *Allegro Design Entry HDL - Constraint Manager User Guide.*

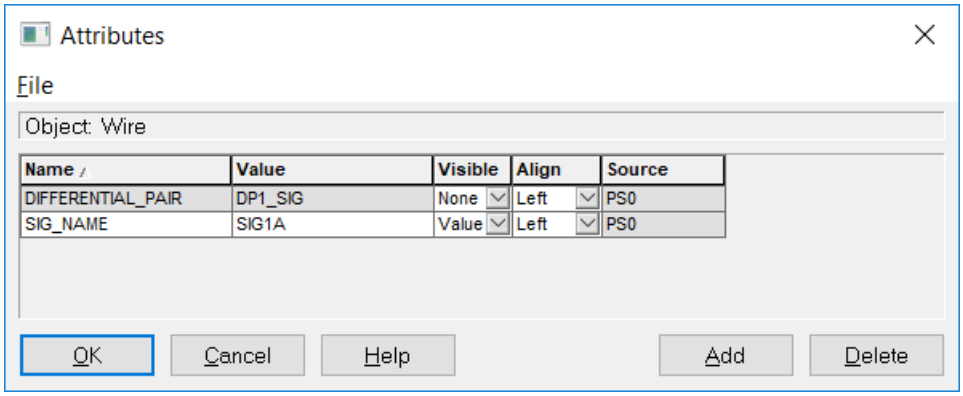
Task Overview

The `DIFFERENTIAL PAIR` constraint maps to the `DIFFERENTIAL_PAIR` property of Design Entry HDL. You will now make the `DIFFERENTIAL_PAIR` property visible on the Design Entry HDL. Then you will propagate the `DIFFERENTIAL_PAIR` property to the schematic.

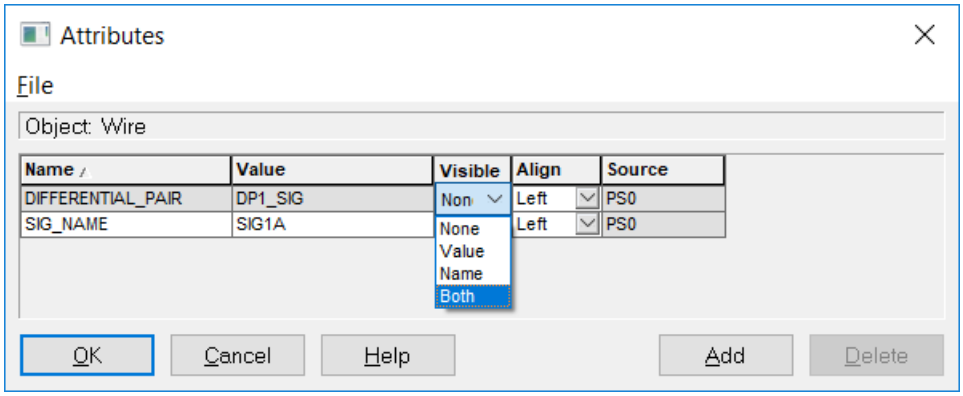
Steps

1. Click the Design Entry HDL window.
2. Choose *Text – Attributes*.
3. Click the `SIG1A` net.

The *Attributes* dialog box appears. You can see the DIFFERENTIAL_PAIR property. The visibility property is set to *None* in the Attributes dialog box.



4. Set the visibility of DIFFERENTIAL_PAIR to *Both* as shown below.



Note: You can select *Name* or *Value* to make only the property name or the property value visible.

5. Click *OK*.

   The *Attributes* dialog box closes.

6. Zoom into the portion of the schematic where the SIG1A net is placed.

7. Similarly, make the `DIFFERENTIAL_PAIR` property visible for `SIG1B`.
8. Choose *File – Save*.

Important

Every time you change the visibility of a property name in the schematic, you must launch and close Constraint Manager to synchronize the changes between the schematic and Constraint Manager.

Video

Now watch this multimedia demonstration, *Viewing Electrical Constraints*, on Cadence Online Support.

Setting Constraints on a Differential Pair

Task Overview

You will set constraints on the `DP1_SIG` differential pair. These constraints will be inherited by the `SIG1A` and `SIG1B` member nets automatically.

Note: Differential pair constraints in the *Differential Pair* worksheet can be applied only to differential pairs and not to individual members of the differential pair.

Steps

1. Launch Constraint Manager.
2. Select the *Net* workbook under *Electrical* domain.
3. Select the *Differential Pair* spreadsheet under *Routing* worksheet.
4. Select the `DP1_SIG` differential pair.
5. In the *Uncoupled Length* column:
   a. Select the value of *Gather Control* as *Ignore*.

      The value of *Gather Control* determines whether to ignore or to include the uncoupled length that occurs before the etch gathers at the pins.

   b. Set the value of *Max* as `200`.

This sets the maximum amount of uncoupled length to `200 mil`, where `mil` is the default unit.

6. In the *Min Line Spacing* column,

   a. Set the value of *Min* as `6 mil`.

      This sets the minimum etch to etch spacing for the differential pair to 6 mil. If this value is not set, the default net spacing rule is used.

7. In the *Coupling Parameters* column,

   a. Set the value of Primary Gap as `8 mil`.

      This sets the optimal distance between the pair of nets in the differential pair to 8 mil.

   b. Set the value of *Prim. Width* as `6 mil`.

      This sets the line width for the differential pair to 6 mil.

   c. Set the value of *Neck Gap* as `6 mil`.

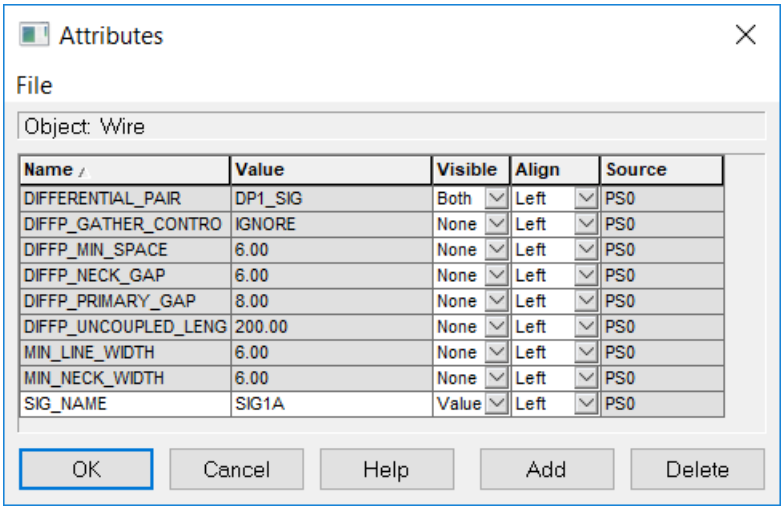
      This sets the allowed distance between the two nets of the differential pair if the etch needs to neck-down to get through the pins.

   d. Set the value of *Neck Width* as `6 mil`.

      This sets the allowed line width for the differential pair if the etch needs to neck-down to get through the pins.

8. Choose *File – Save* to save the constraint in the Constraint Manager database.

9. In Design Entry HDL, access the *Attributes* dialog box for `SIG1A`.
   Note that all the constraints that you specified in Constraint Manager appear in Design Entry HDL.



Setting Values for Propagation Delay

While designing the schematic for your design, you might have several design constraints such as length and impedance on the critical nets in the design. These constraints might have been given to you by the Signal Integrity engineer. These translate to the length of critical nets and therefore to the propagation delay of the signals passing through them.

Depending on the requirement, the Signal Integrity engineer might give you the maximum and minimum allowed length of critical nets. You can accordingly set the maximum and minimum propagation delays of those nets.

It is possible that for a certain critical net, you might have to set the constraint on all its driver and receiver ends or specific pin pairs. In the following section, you will learn how to set the constraint for the entire net and also for a specific driver-receiver pair.

Task Overview

You will set the maximum and minimum values for propagation delay on the `RESET` net. First, you will set the delay between all the drivers and receivers of the `RESET` net. Then, for a specific driver and receiver pair, you will set a different value for the propagation delay.

Steps

1. In Constraint Manager, select the *Min/Max Propagation Delays* spreadsheet under the *Routing* worksheet of *Net* workbook.
2. In Design Entry HDL, locate the `RESET` net using the *Find* dialog.
3. Click the `RESET` net on the schematic.

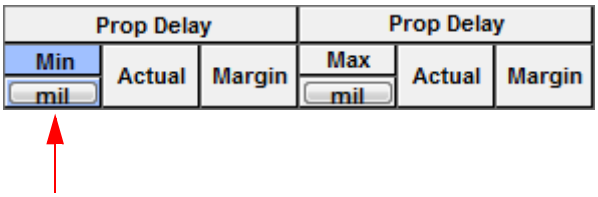
   The `RESET` net is highlighted in Constraint Manager.

Important

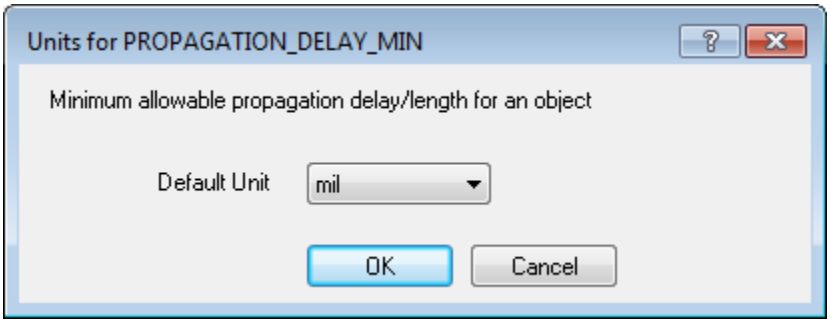
In Constraint Manager version 17.0 onwards, the default unit is `mil`. For the purpose of this tutorial, we will use the `ns` unit.

4. For the `RESET` net, do the following:

   a. In the *Prop Delay Min* column, click the *mil* button.



   The *Units for PROPAGATION_DELAY_MIN* dialog box appears.



   b. Select *ns* from the *Default Unit* drop-down list and click *OK*.

   c. Type a *Min* value of `0.9`.

   This means that the signal on the `RESET` net must have a propagation delay of at least `0.9 ns` before it reaches any destination.

   Note: Note that in the Pin Pairs column, All Drivers/All Receivers is selected

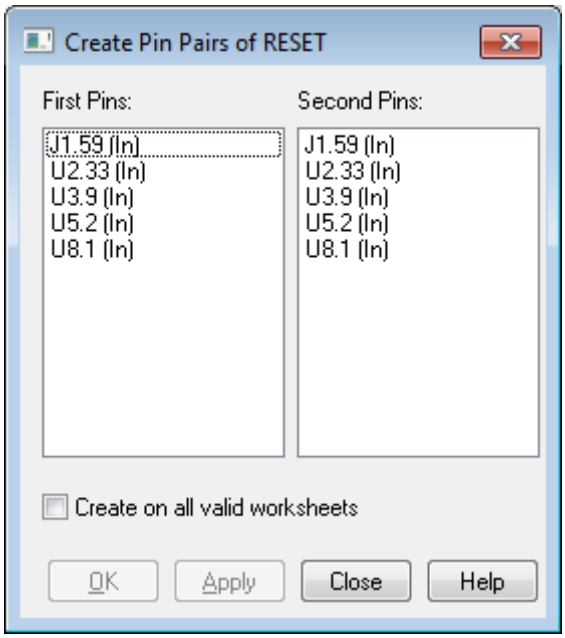
automatically. This means that the propagation delay has been set between all the drivers and receivers of the RESET net.

d. In the *Prop Delay Max* column, change the default measurement unit to ns and type the *Max* value as 1.1.

This means that the signal on the net RESET must reach any destination within 1.1 ns after it is available on the RESET net.

5. Click the RESET net and choose *Objects – Create – PinPair* from the Constraint Manager menu or right-click on the RESET net and choose *Create – Pin Pair* from the pop-up menu.

The *Create Pin Pairs* dialog box appears. The *First Pins* and *Second Pins* columns list the pins for RESET net.



6. In the *First Pins* column, click *J1.59*.

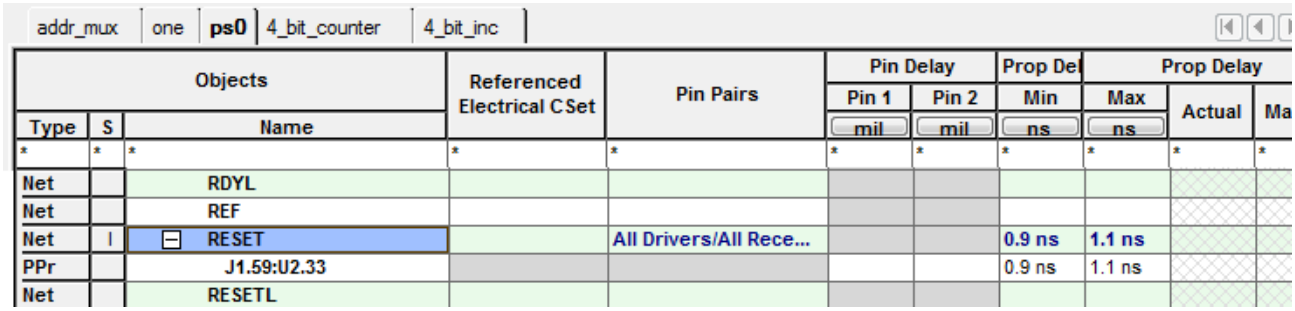
7. In the *Second Pins* column, click *U2.33*.

8. Select the *Create on all valid worksheets* check box.

9. Click *OK*.

Click *OK* in the information message box that appears.

Pin pair `J1.59:U2.33` is created and is visible under the `RESET` net in Constraint Manager.

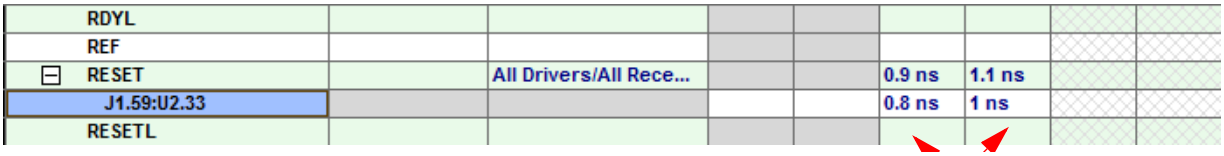


Note: The values in the *Min* and *Max* columns for the pin-pair are inherited from the existing constraint on the `RESET` net.

10. For the `J1.59:U2.33` pin pair, change the value in the *Min* column from `0.9 ns` to `0.8 ns`.

11. Also, change the value in the *Max* column from `1.1 ns` to `1.0 ns`.

    The worksheet appears as shown below:



12. Choose *File – Save* to save the constraints in the Constraint Manager database.

13. Choose *File – Exit* to exit from Constraint Manager.

14. Choose *File – Save* in Design Entry HDL.

Video

Now watch this multimedia demonstration, *Creating Pin Pairs*, on Cadence Online Support.

Setting the Propagation Delay Relative to Another Net

You can set the propagation delay of a net or pin pair relative to the propagation delay of another net. All these nets and pin pairs can then be grouped together to form a match group. The group is characterized by a target pin pair/net, a delta value, and a tolerance value. For details on match groups, refer to the Working with Objects chapter of the *Allegro Constraint Manager User Guide.*

Task Overview

You will now set the propagation delay for the `D<0>` target net and create a matched group for it. Then, you will add nets `D<14>` and `D<15>` to the matched group and set their propagation delay relative to the `D<0>` net.

Steps

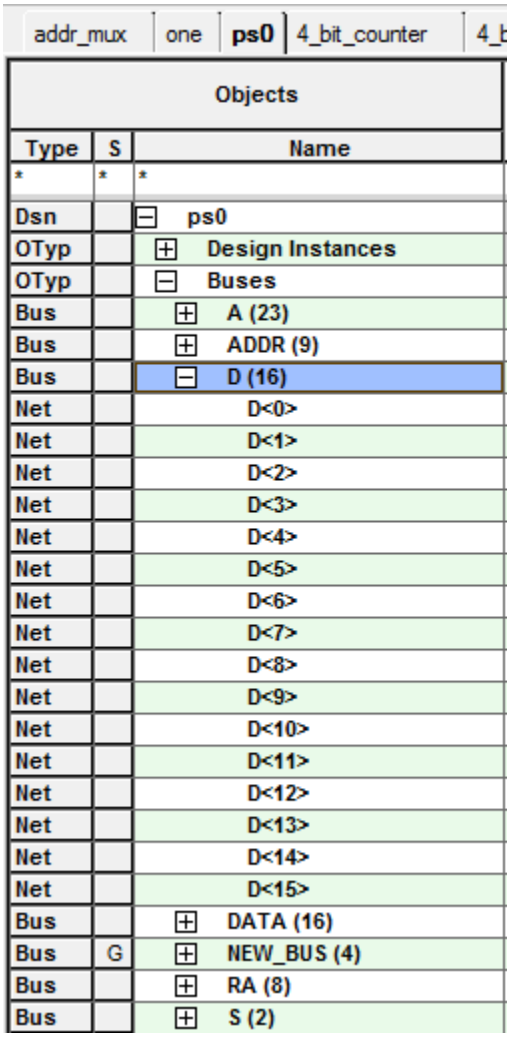
You need to perform the following tasks to complete this activity:

1. Setting the Minimum and Maximum Propagation Delay for the Target Net
2. Creating a Matched Group
3. Adding Nets to a Matched Group
4. Setting Relative Propagation Delay values for Nets

Setting the Minimum and Maximum Propagation Delay for the Target Net

1. Open Constraint Manager by choosing *Tools – Constraints – Edit* in Design Entry HDL.
2. In the *Min/Max Propagation Delays* worksheet, expand the `D(16)` bus.

The bits in bus `D (16)` are displayed.



3. In the *Prop Delay Min* column, for bit `D<0>`, type the value `1.0`; In the *Prop Delay Max* column, type `1.2`.

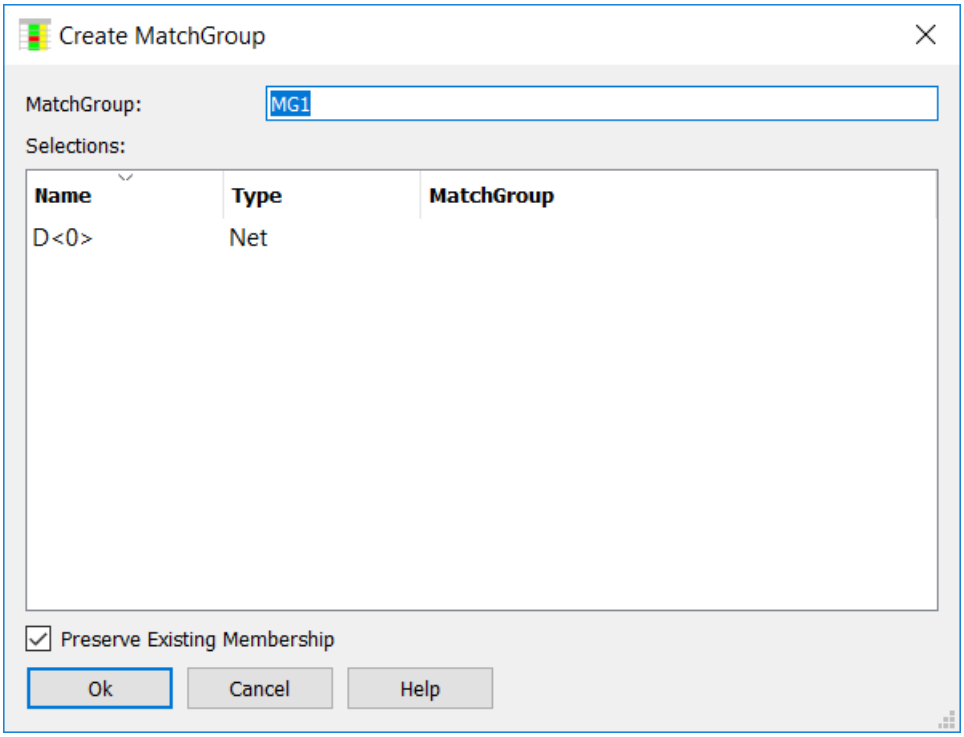
Creating a Matched Group

1. Click *Relative Propagation Delay* spreadsheet in the *Routing* worksheet.

   The *Relative Propagation Delay* worksheet appears in the right pane.

2. Click the `D<0>` bit and choose *Objects – Create – Match Group* from the menu or right-click on the `D<0>` bit and choose *Create – Match Group* from the pop-up menu.

The *Create MatchGroup* dialog box appears.

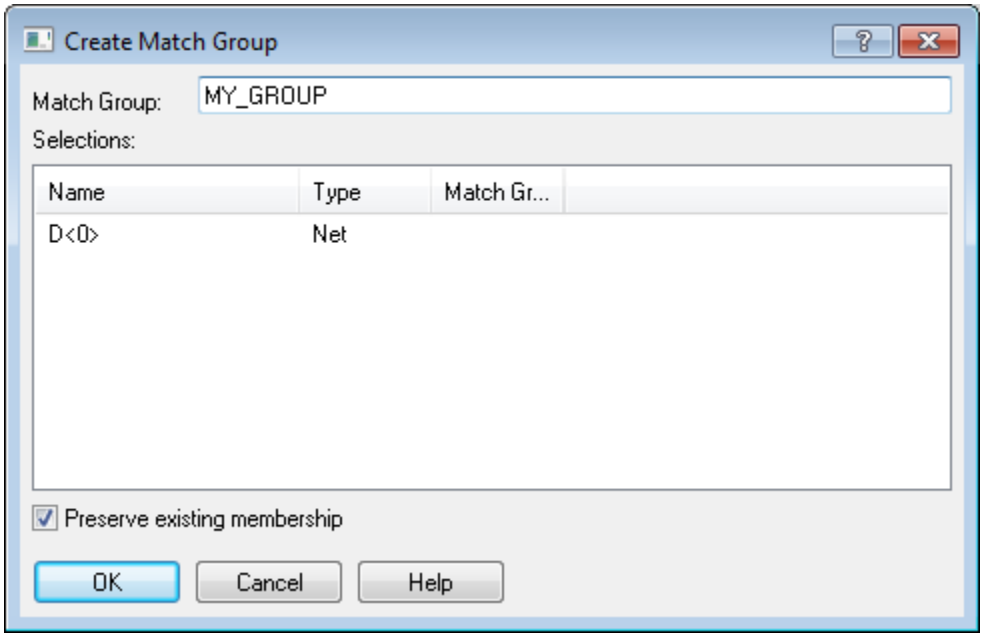


It contains the bit `D<0>` in the *Selections* list indicating that this net will be a member of the match group.

Tip

You can also create an empty match group at the design level using the menu option *Objects – Create – Match Group* first and add the members of the group later.

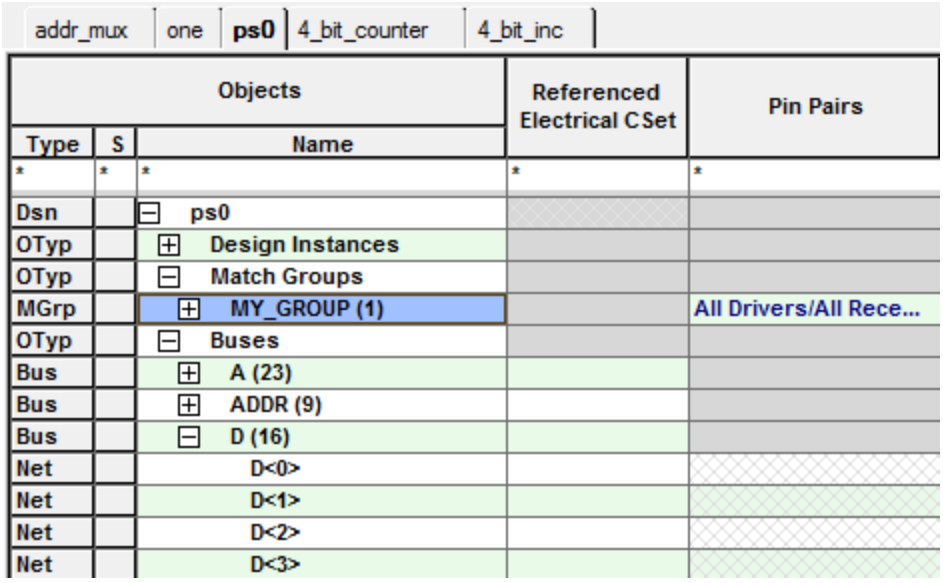
3. Specify the name of the match group as `MY_GROUP` in the *Match Group* field.



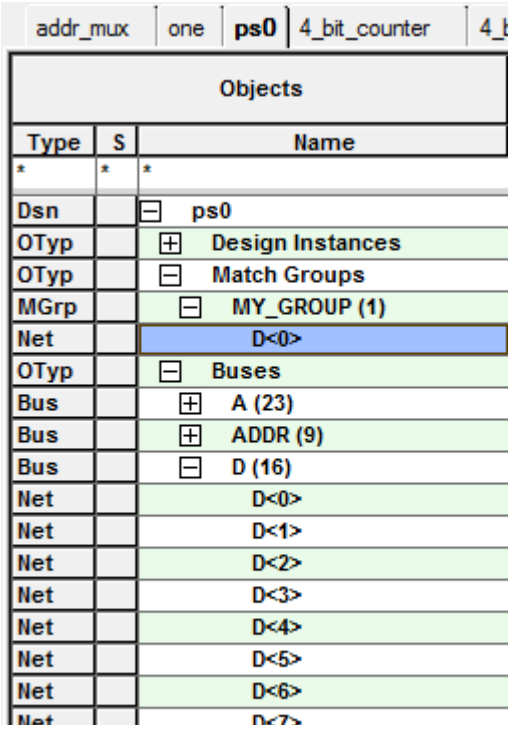
4. Click *OK*.

   The Match Group is created and the *Create Match Group* dialog box closes.

5. Scroll up the list of nets to see the entry *MY_GROUP* under the *ps0* design in the worksheet.



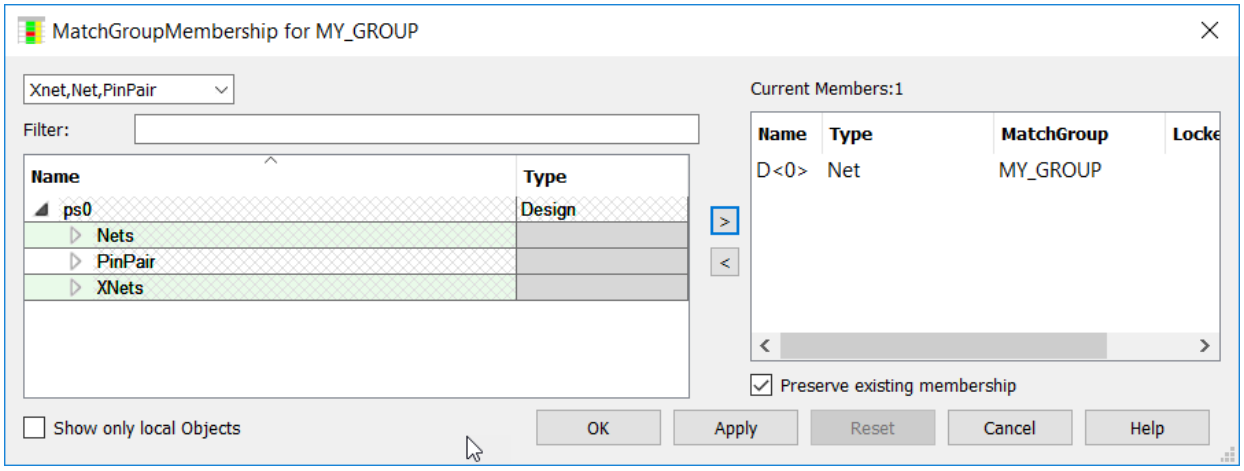
Note: The net D<0> appears under MY_GROUP indicating that it is a member of the group.



Adding Nets to a Matched Group

1. Right-click *MY_GROUP* and choose *Match Group members* from the pop-up menu.

   The *MatchGroupMembership* dialog box appears with the D<0> net as a member.



2. In *Name* column under the *Filter* section, expand *Nets* and click D<14>.

3. Click > to move the selected D<14> net to the *Current Members* list.
4. Similarly, move the net D<15> to the *Current Members* list.

   Now, the three nets—D<0>, D<14>, and D<15>–are members of the match group MY_GROUP.
5. Click *OK*.

   The *MatchGroupMembership* dialog box closes and the D<0>, D<14>, and D<15> nets appear under MY_GROUP in the *Relative Propagation Delay* worksheet.

Note that the *Scope* and *Delta:Tolerance* fields are automatically filled in with default values.

Objects			Referenced Electrical CSet	Pin Pairs	Pin Delay		Scope	Relati
					Pin 1	Pin 2		Delta:Tolerance
Type	S	Name			mil	mil		ns
*	*	*	*	*	*	*	*	*
Dsn		ps0						
OTyp		Design Instances						
OTyp		Match Groups						
MGrp		MY_GROUP (3)		All Drivers/All Rece...			Global	0 ns:5 %
Net		D<0>		All Drivers/All Receivers			Global	0 ns:5 %
Net		D<14>		All Drivers/All Receivers			Global	0 ns:5 %
Net		D<15>		All Drivers/All Receivers			Global	0 ns:5 %
OTyp		Buses						
Bus		A (23)						
Bus		ADDR (9)						
Bus		D (16)						
Net		D<0>						
Net		D<1>						
Net		D<2>						

Setting Relative Propagation Delay values for Nets

1. For the D<0> net, note the following:

   a. In the *Scope* column, *Global* is selected by default.

   b. In the *Delta:Tolerance* field, the value is automatically set to *0 ns:5%*.

      The delta value zero for the D<0> net makes Constraint Manager select this net as the target net. The minimum and maximum propagation delay values for the D<14> and D<15> nets are set relative to that of net D<0>.

      The default unit for delta is ns and for tolerance is percentage. You can specify tolerance in ns too. For the purpose of this tutorial, you will retain the default measurement units for both, delta, and tolerance.
2. For the D<14> net, do the following:

c. In the *Pin Pairs* column, select *Longest Pin Pair* from the drop-down box.

A constraint that is set on the longest pin pair of a net is most stringent. If this constraint is met by the longest pin pair, it is ensured that the constraint will be met by all the other pin-pairs of the net also.

d. In the *Delta:Tolerance* field, specify the value as `0.3 ns:5%`.

This means that the travel time for the signal on net `D<14>` must be `0.3 ns` more than that for the signal on net `D<0>` within a tolerance of `+/- 5%`.

3. For the `D<15>` net, do the following:

e. In the *Delta:Tolerance* field, specify the value as `-0.03 ns:0.06 ns`.

This means that the travel time for the signal on net `D<15>` must be `0.03ns` less than that for the signal on net `D<0>` within a tolerance of `+/- 0.06ns`.

4. Choose *File – Save* to save the constraints.

Note: The *Relative Propagation Delay* constraint maps to the `RELATIVE_PROPAGATION_DELAY` property in Design Entry HDL.

Summary

You learned to create driver-receiver pin pairs and differential pairs for nets and set some DRC-based constraints on them. You also learned to cross-probe between Design Entry HDL and Constraint Manager.

What's Next

In the next chapter, Setting Timing and Signal Integrity Constraints on Nets, you will set some timing and signal integrity constraints on critical nets. These are constraints that you would get after simulating the design. You will also view these constraints on the schematic.

Recommended Reading

For more information about how pin-pair and differential pair constraints are handled in Design Entry HDL, see *Allegro Design Entry HDL - Constraint Manager User Guide*.

3

Setting Timing and Signal Integrity Constraints on Nets

Objectives

To learn how to set timing and signal integrity constraints on nets in your design using Constraint Manager and view those constraints on the schematic in Design Entry HDL.

At the end of the lesson, you will be able to:

- set the switch and settle time for a signal.
- control the electrical properties of a signal.
- set the maximum overshoot of a signal.
- set the noise margin for a signal.

Nature of Chapter

Skill (includes concepts and practice)

Estimated Completion Time

30 minutes

Setting Timing Constraints

You will now learn how to set the following timing constraints on nets in your design:

- Settle time
- Switch time

Controlling the Settle and Switch Time of a Signal

Task Overview

You will navigate to the `RESETL` net and add settle and switch time constraints to it. Then, you will save the constraints and view the corresponding properties on the schematic.

Steps

1. Accessing the Switch and Settle Delay Worksheet
2. Navigating to a Net
3. Setting Values for Min First Switch and Max Final Settle
4. Viewing the Constraint on the Schematic

Accessing the Switch and Settle Delay Worksheet

1. In the *Net* workbook under the *Electrical* domain, click *Timing*.

   The *Timing* worksheet appears. All the nets and the buses in the `ps0` design are listed in the worksheet in the right pane. Note the *Switch/Settle Delays* and *Setup/Hold* tabs in this workbook.

2. Click *Switch/Settle Delays* worksheet.
3. Size the worksheet to occupy the full window.

Navigating to a Net

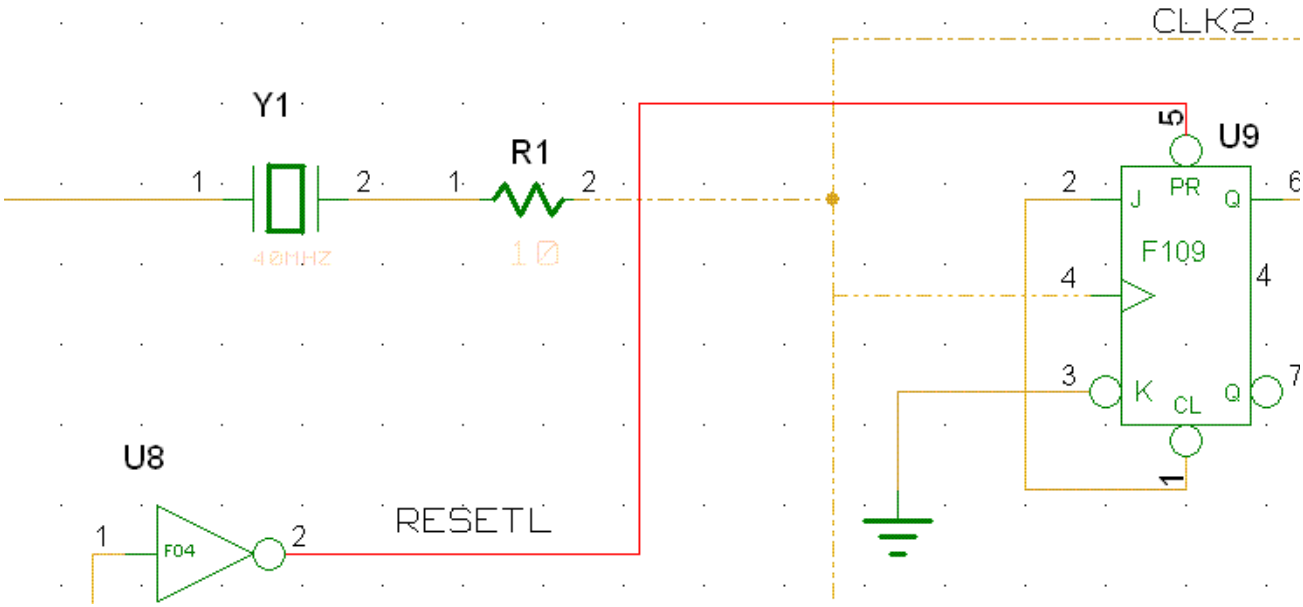
Task Overview

You will select the `RESETL` net in Constraint Manager and it will be selected in Design Entry HDL.

Steps

1. Right-click the `RESETL` net and choose *Select* from the pop-up menu.

   In the Design Entry HDL window, an entry for *@project_lib.ps0(sch_1):page1_resetl* appears in the Global Navigate window and the net is also selected on the schematic.



Note: You can also navigate to a net using the *Find* option.

Setting Values for Min First Switch and Max Final Settle

Steps

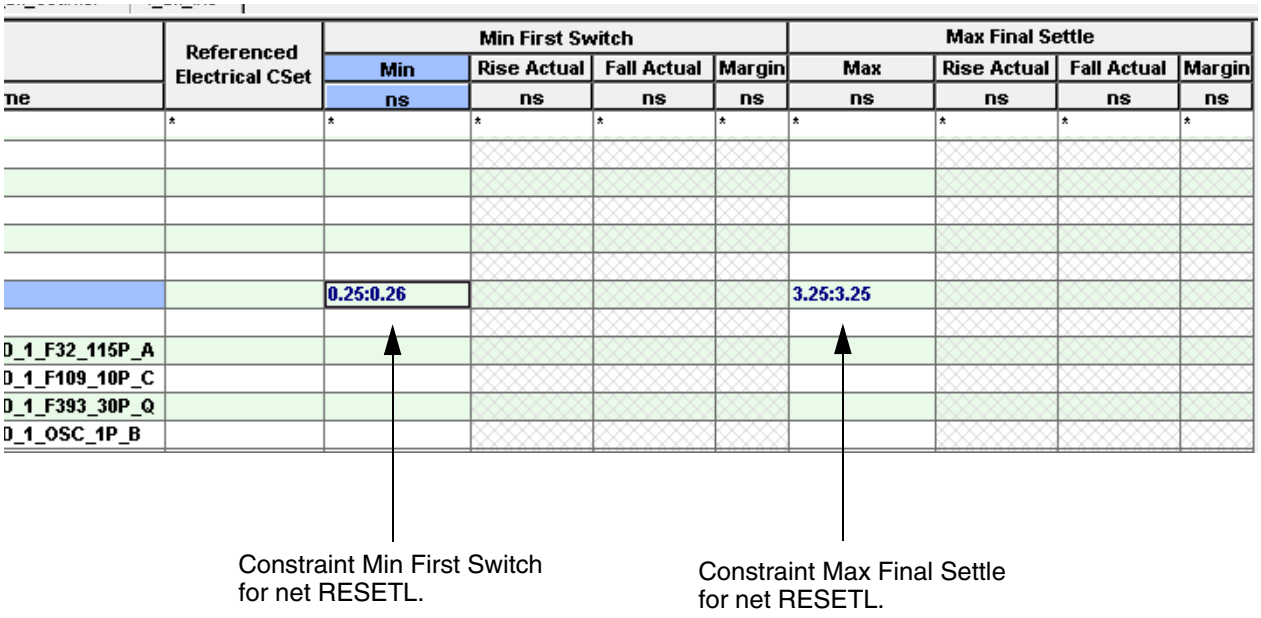
1. In Constraint Manager, under the *Min First Switch* column, set the *Min* value as `0.25:0.26` for RESETL net.

This sets the value for the rising edge of the signal on the `RESETL` net as `0.25 ns` and the falling edge as `0.26 ns`. The default unit for min first switch is `ns`.

2. In the *Max Final Settle* column, set the *Max* value as `3.25:3.25` for the `RESETL` net.

   This sets the value for maximum final settle delay for the rising edge and the falling edge of the `RESETL` net as `3.25 ns`. The default unit for max final settle is `ns`.

   The Constraint Manager worksheet now appears as follows:



ne	Referenced Electrical CSet	Min First Switch				Max Final Settle			
		Min	Rise Actual	Fall Actual	Margin	Max	Rise Actual	Fall Actual	Margin
		ns	ns	ns	ns	ns	ns	ns	ns
	*	*	*	*	*	*	*	*	*
		0.25:0.26				3.25:3.25			
D_1_F32_115P_A									
D_1_F109_10P_C									
D_1_F393_30P_Q									
D_1_OSC_1P_B									

3. Choose *File – Save* to save the constraints in the Constraint Manager database.

Viewing the Constraint on the Schematic

The *Min First Switch* constraint is mapped to the `MIN_FIRST_SWITCH` property in Design Entry HDL and the *Max Final Settle* constraint is mapped to the `MAX_FINAL_SETTLE` property.

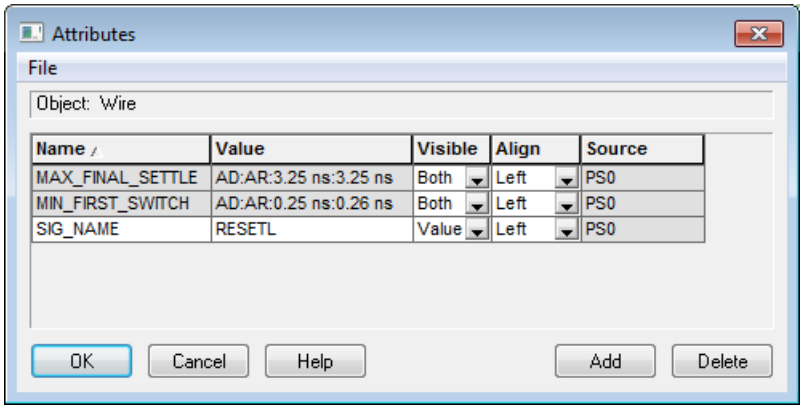
Task Overview

You will now make the `MIN_FIRST_SWITCH` and `MAX_FINAL_SETTLE` properties on the `RESETL` net visible in Design Entry HDL.

Steps

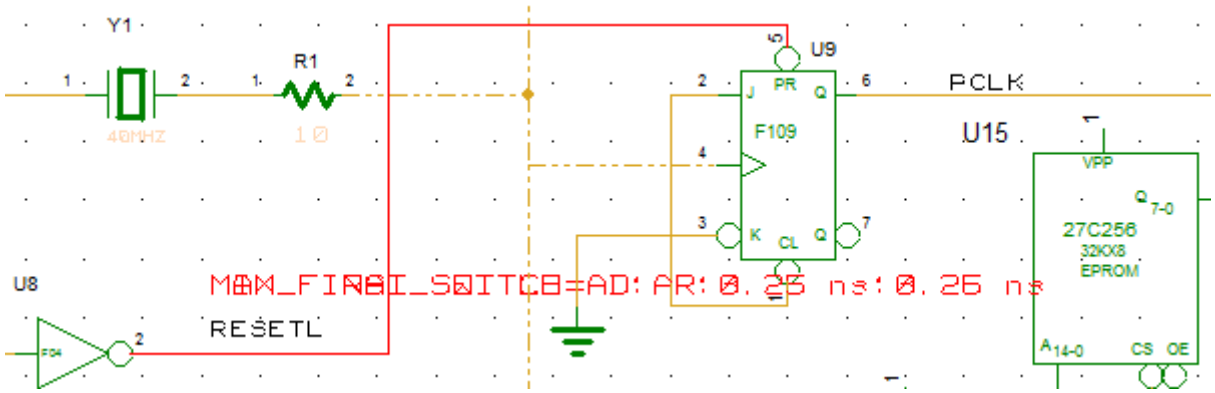
1. Click the Design Entry HDL window.
2. Choose *Text – Attributes*.
3. Click the `RESETL` net.

   The Attributes dialog box appears. You can see the `MIN_FIRST_SWITCH` and `MAX_FINAL_SETTLE` properties with visibility set to *None* in the *Attributes* dialog box.
4. Set the visibility of `MIN_FIRST_SWITCH` and `MAX_FINAL_SETTLE` to *Both*.



5. Click *OK*.
6. Click *File – Save*.

   The constraints appear as shown below:



Note: If you had closed Constraint Manager earlier, remember to launch and close it again to synchronize the changes between the schematic and Constraint Manager.

Setting Signal Integrity Constraints

You will now learn how to set the following constraints on nets in your design:

- Electrical Properties
- Reflection constraints, maximum Overshoot and Noise Margin

Setting the Electrical Properties of a Signal

Task Overview

You will set electrical properties constraints for the `CLK` net. Then, you will save the constraints and view the corresponding properties on the schematic.

Steps

1. Open Constraint Manager.
2. In the *Net* worksheet under *Electrical* domain, click *Signal Integrity*.

   The *Signal Integrity* worksheet appears. All the nets and the buses in the `ps0` design are listed in the worksheet in the right pane. Note the *Electrical Properties, Reflection, Edge Distortions, Estimated XTalk, Simulated XTalk* and *SSN* tabs in this worksheet.
3. In the *Electrical Properties* worksheet, click the *CLK* net as shown below:

addr_mux | one | **ps0** | 4_bit_counter | 4_bit_inc

Objects			Referenced Electrical CSet	Frequency	Period	Duty Cycle	Jitter	Cycle to Measure
Type	S	Name		MHz	ns	%	ps	
*	*	*	*	*	*	*	*	*
Dsn		⊟ ps0						
OTyp		⊟ Design Instances						
Dsnl		⊞ page1_i121 (addr_mux)						
Dsnl		⊟ page4_i1 (4_bit_counter)						
Dsnl		⊞ page1_3p (4_bit_inc)						
Net	I	CIN						
Net	I	CLK						
Net		UNNAMED_1_4BITINC_3P_DOUT						
Net		UNNAMED_1_4BITINC_3P_DOUT						
Net		UNNAMED_1_4BITINC_3P_DOUT						
Net		UNNAMED_1_4BITINC_3P_DOUT						
Dsnl		⊞ page6_i1 (one)						
OTyp		⊞ Buses						
OTyp		⊞ Diff Pairs						
OTyp		⊞ XNets/Nets						

4. In the *Frequency* column, set the value as `66` for `CLK` net. The unit for frequency is set to MHz.

   The values of *Period, Duty Cycle, Jitter,* and *Cycle to Measure* are set automatically.

5. The default value of Duty Cycle is 50%. Set the value as 60%.

6. The default value of Jitter is 0. Set the value as 20. The default unit for jitter is `ps`.

7. The default value of *Cycle to Measure* is 1. Set the value as `2`.

8. Choose *File – Save* to save the constraints in the Constraint Manager database.

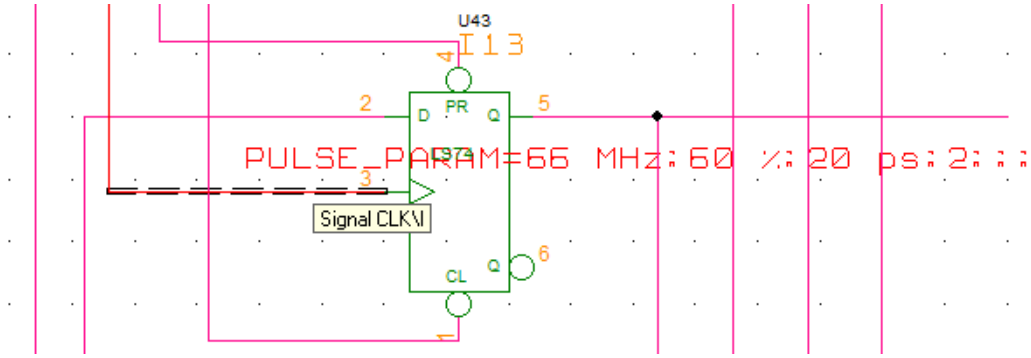
   The frequency, period, jitter, duty cycle and cycle to measure constraints are mapped to the `PULSE_PARAM` property in Design Entry HDL.

9. Right-click on the `CLK` net and choose *Select* from the pop-up menu.

10. In Design Entry HDL, choose *Text – Attributes* and then click the `CLK` net.

11. In the *Attributes* dialog box, set the visibility of `PULSE_PARAM` to *Both* and then click *OK*.

    The `PULSE_PARAM` property appears as follows:



Setting Reflection Constraints for a Signal

Task Overview

You will set Reflection constraints for the `CLK` net. Then, you will save the constraints and view the corresponding properties on the schematic.

Steps

1. In Constraint Manager, click the *Net* worksheet under *Electrical* domain and then click *Signal Integrity*.
2. Select the *Reflection* tab.
3. Size the worksheet to occupy the full window.
4. Set the Max Overshoot for `CLK` to `5100:-610`. The default unit for max overshoot is `mV`.

   This sets the value of maximum overshoot for the rising edge of net `CLK` to 5100mV and the value of maximum overshoot for the falling edge of net `CLK` to 610mV.

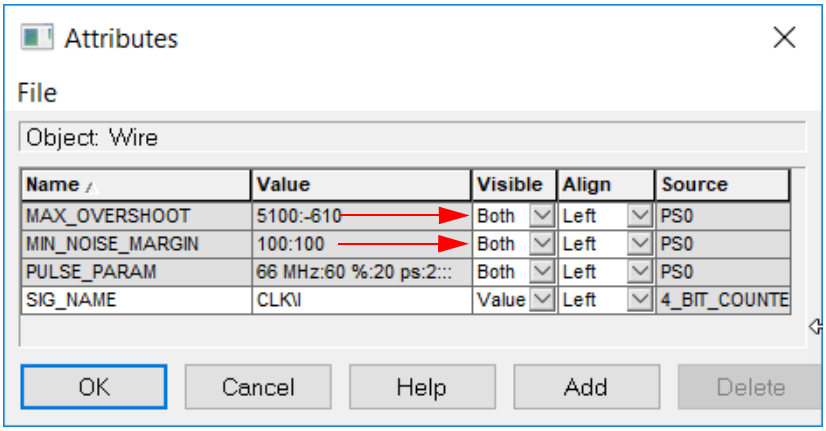
   The values for *High Actual*, *Low Actual*, and *Margin* are set at the time of analysis in Allegro SI/PCB Editor. You cannot set them in Constraint Manager connected with Design Entry HDL.
5. Set the Min Noise Margin for `CLK` to `100:100`. The default unit for min noise margin is `mV`.

   This sets the value of the minimum noise margin for the rising and falling edges of net `CLK` to `100 mV`.

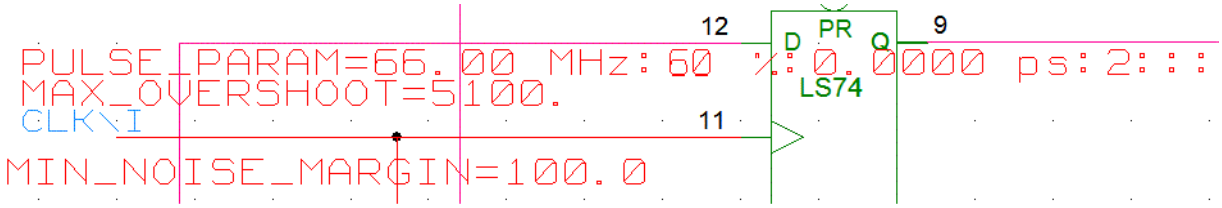
   The values for *High Actual*, *Low Actual*, and *Margin* are set at the time of analysis in Allegro SI/PCB Editor. You cannot set them in Constraint Manager connected with Design Entry HDL.
6. Choose *File – Save* to save the constraints in the Constraint Manager database.

   The maximum overshoot constraint in Constraint Manager maps to the `MAX_OVERSHOOT` property in Design Entry HDL and the minimum noise margin maps to `MIN_NOISE_MARGIN`.
7. Click the Design Entry HDL window.

8. In Design Entry HDL, set the visibility of `MAX_OVERSHOOT` and `MIN_NOISE_MARGIN` to *Both*.



The `MAX_OVERSHOOT` and `MIN_NOISE_MARGIN` properties are now visible on the schematic.



9. Click *File – Save*.

Note: If Constraint Manager was closed, remember to launch and close it to synchronize the changes between the schematic and Constraint Manager.

Summary

You learned to set some simulation-based constraints on nets in Constraint Manager. You also learned the correspondence between those constraints and properties in Design Entry HDL, and made the properties visible on the canvas.

What's Next

In the next chapter, Working with Electrical Constraint Sets, you will learn to group constraints into an electrical constraint set (ECSet) and apply them to several critical nets at the same

time. You will also see how an ECSet appears in Design Entry HDL and how to change some constraints that are part of an ECSet.

Recommended Reading

For information about all the timing and signal integrity constraints that you can set in Constraint Manager, see the Allegro Constraint Manager User Guide.

4

Working with Electrical Constraint Sets

Objectives

To learn how to create an Electrical Constraint Set (ECSet) and apply it to nets and buses in your design using Constraint Manager.

At the end of the lesson, you will be able to,

- decide when to use an ECSet.
- create an ECSet.
- assign an ECSet to a net.
- override values of constraints in an ECSet.
- view an ECSet in Design Entry HDL.

Nature of Chapter

Skill (includes concepts and practice)

Estimated Completion Time

40 minutes

Overview

You can identify critical nets in your design and identify constraints that are applicable to all these critical nets. You can define these constraints together into an ECSet and apply them to each critical net. This way, an ECSet can be used to define a generic set of rules applicable to a number of nets. If your design requirement changes at a later point in time, you can edit your constraint; all the nets referencing the ECSet inherit the changed ECSet automatically. Thus, using ECSets is a very efficient way of capturing constraints in Constraint Manager.

You can also use ECSets for setting pin pair constraints on the bits of a large bus. You can set the pin pair constraints on one bit of the bus and create an ECSet. Then, you can make the bits of the bus reference this ECSet. Constraint Manager will automatically create the corresponding pin pairs for the bits and make them visible in Constraint Manager.

The main advantages of an ECSet are:

- One ECSet can be applied to many nets simultaneously.
- Capture any or all electrical constraints in one ECSet.
- A change in a constraint in an ECSet is automatically inherited by the objects that reference the ECSet.
- Override the constraints defined in an ECSet.
- Import ECSets to your new design when reusing a design.
- Use ECSets for setting pin pair constraints on the bits of a large bus.

Take the example of the `DATA` bus. First, you will create an ECSet in Constraint Manager and then attach this ECSet to a bit and make a few other bits of the bus reference this ECSet. Finally, you will override the default values of constraints for some bits of the `DATA` bus.

Creating an ECSet

Task Overview

You will create an ECSet with the following constraints on bit `DATA<1>` of the `DATA` bus in Constraint Manager:

- Max overshoot
- Min noise margin

- Min first switch
- Max final settle
- Impedance

Steps

1. Launch Constraint Manager.
2. Select the *Electrical Constraint Set* workbook under the *Electrical* domain and then click *All Constraints*.
3. Select `ps0`.
4. Choose *Objects – Create – Electrical CSet*.

   The *Create Electrical CSet* dialog box appears.
5. Specify the name for the Electrical CSet as `DATA<1>`.
6. Click *OK*.
7. Click *Signal Integrity/Timing/Routing* workbook under the *All Constraints* worksheet.
8. Click `DATA<1>` under `ps0`.
9. In the *Reflection* column:
   a. Set the value of *Overshoot* as `5000:-600`.
   b. Set the value of *Min Noise Margin* as `20:22`.
10. In the *Switch/Settle Delays* column:
    a. Set the value of *Min First Switch* as `2:3`.
    b. Set the value of *Max Final Settle* as `5:6`.
11. In the *Single-line Impedance* column:
    a. Set the value of *Target* as `70`.

       The value of *Tolerance* is automatically set as `2%`.
12. Choose *File – Save*.

This completes the creation of the `DATA<1>` ECSet.

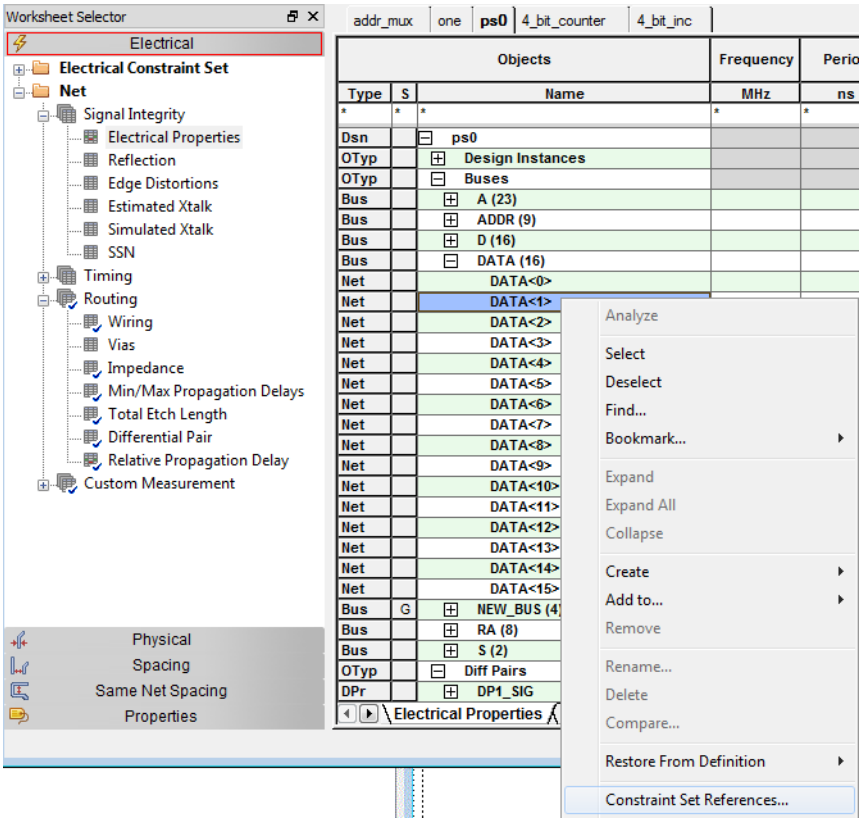
Assigning an ECSet to a Net

Task Overview

You will first attach the DATA<1> ECSet to the DATA<1> net. Later, you will assign the same ECSet to DATA<15>, DATA<14>, DATA<13>, and DATA<12> of bus DATA so that the constraints in DATA<1> are applied to them.

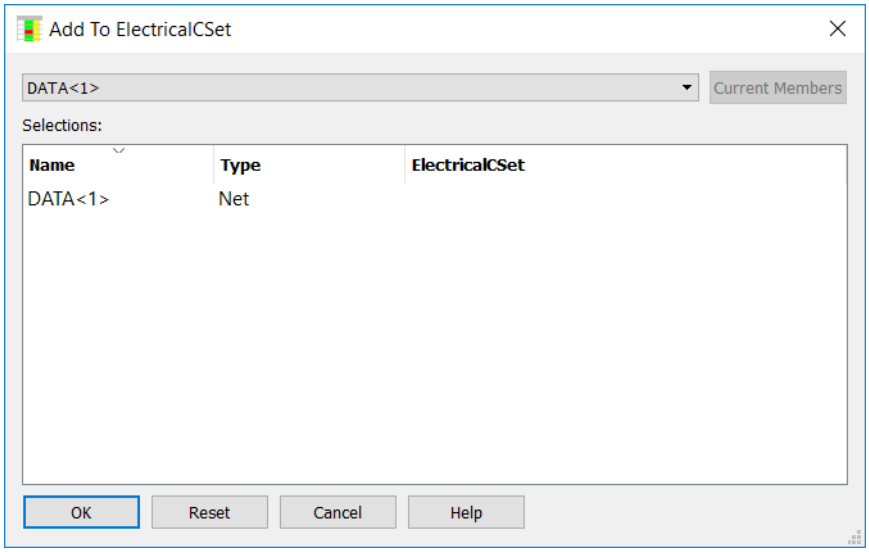
Steps

1. In the *Net* workbook, select *Reflection* under the *Signal Integrity* worksheet.
2. Click the DATA<1> bit of bus DATA(16) and choose *Objects – Constraint Set References* from the Constraint Manager menu or right-click DATA<1> to bring up the pop-up menu and choose *Constraint Set References*.



The *Add to Electrical CSet* dialog box appears.

3. Select DATA<1> from the *Current Members* drop-down list.



4. Click *OK*.
   View the reflection constraints on bit DATA<1> of the DATA bus and the inherited *Switch/Settle Delays* and *Impedance* constraints on bit DATA<1>.

Objects			Referenced Electrical CSet	Overshoot				
				Max	High Actual	Low Actual	Margin	Min
Type	S	Name		mV	mV	mV	mV	mV
*	*	*	*	*	*	*	*	*
Dsn		⊟ ps0						
OTyp		⊞ Design Instances						
OTyp		⊟ Buses						
Bus		⊞ A (23)						
Bus		⊞ ADDR (9)						
Bus		⊞ D (16)						
Bus		⊟ DATA (16)						
Net		DATA<0>						
Net		DATA<1>	DATA<1>	5000:-600				20:22

5. Assign the DATA<1> ECSet to the DATA<13>, DATA<14>, and DATA<15> bits of the DATA bus:

   a. Drag and select the cells for the DATA<13>, DATA<14>, and DATA<15> bits under the *Referenced Electrical CSet* column.

b. From the drop-down menu, choose the DATA<1> ECSet.
The DATA<1> ECSet is automatically assigned to the DATA<13>, DATA<14>, and DATA<15> bits.

Objects			Referenced Electrical CSet	Overshoot				
				Max	High Actual	Low Actual	Margin	Min
Type	S	Name		mV	mV	mV	mV	mV
*	*	*	*	*	*	*	*	*
Net		DATA<13>	DATA<1>	5000:-600				20:22
Net		DATA<14>	DATA<1>	5000:-600				20:22
Net		DATA<15>	DATA<1>	5000:-600				20:22
Bus	G	⊞ NEW_BUS (4)						
Bus		⊞ RA (8)						

Tip

You can also select multiple nets at the same time by keeping the *Ctrl* key pressed and clicking the nets. Then you can open the *Electrical CSet References* dialog box and assign the ECSet to all of them at the same time.

Note: If you apply an ECSet on the bus instead of individual bits of the bus, the ECSet is assigned to all the bits of the bus.

6. Choose *File – Save* to save the constraints in the Constraint Manager database.

Video

Now watch this multimedia demonstration, *Creating ECSets*, on Cadence Online Support.

Overriding Default Values of Constraints in an ECSet

Once a net has inherited constraints from an ECSet with their default values, you can override the values of some of the constraints for a net if your design has such a requirement.

Task Overview

Change the values of the Impedance and Min First Switch constraints for bit DATA<15> of the DATA bus.

Steps

1. In the *Net* workbook under the *Electrical* domain, select *Impedance* under the *Routing* worksheet.
2. In the *Target* column for bit DATA<15> of the DATA bus, change the inherited value of 70 Ohm to 74 Ohm.
3. Select *Switch/Settle Delays* under the *Timing* worksheet.
4. In the *Min First Switch* column for bit DATA<15> of the DATA bus, change the value of *Min* from 2:3 ns to 0.5:0.6 ns.
5. Choose *File – Save* to save the constraints.
6. Choose *File – Exit*.

Viewing an ECSet on the Schematic

An ECSet in Constraint Manager maps to the ELECTRICAL_CONSTRAINT_SET property in Design Entry HDL. Like other properties, this is also a read-only property in Design Entry HDL.

Task Overview

You will view the properties of the DATA<15> bit of bus DATA in Design Entry HDL.

Steps

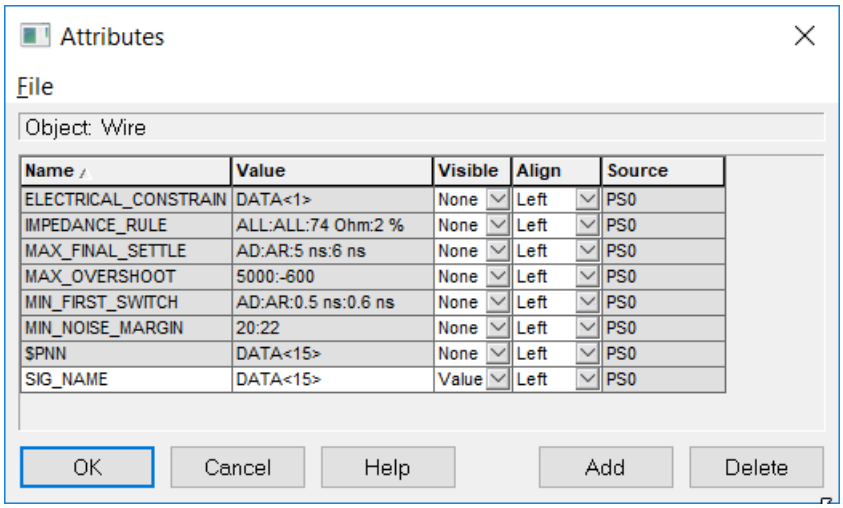
1. In the Design Entry HDL window, locate bus bit DATA<15> in the design.
2. Choose *Text – Attributes*.
3. Click the DATA bus.

   The *Attributes* dialog box appears.

   You can see the IMPEDANCE_RULE, MIN_FIRST_SWITCH, and ELECTRICAL_CONSTRAINT_SET properties.

Important

The `IMPEDANCE_RULE` and `MIN_FIRST_SWITCH` properties appear separately because they have values different from the constraints in the ECSet `A<1>`.



4. Click *Cancel*.

   The *Attributes* dialog box closes.

Summary

You learned to set constraints on a net in Constraint Manager to form an ECSet. You also learned to make a net reference an ECSet, and then override some constraints in the ECSet.

What's Next

In the next chapter, Working with Xnets, you will create an Xnet in Design Entry HDL, view it in Constraint Manager, generate electrical constraints on the Xnet in SigXplorer, and apply the constraints to other Xnets in Constraint Manager.

Recommended Reading

For more information about electrical constraint sets, see the *Allegro Design Entry HDL - Constraint Manager User Guide* and the Allegro Constraint Manager User Guide.

5

Working with Xnets

Objectives

To learn how to create an extended net (Xnet) in Design Entry HDL, view it in Constraint Manager, generate electrical constraints on the Xnet in SigXplorer, and apply the constraint rules to other Xnets in Constraint Manager.

At the end of the lesson, you will be able to,

- create an Xnet.
- create a model-defined differential pair.
- view an Xnet in Constraint Manager.
- generate an electrical constraint on the Xnet in SigXplorer.
- apply an ECSet on one Xnet to other Xnets in Constraint Manager.
- rename an Xnet.

Nature of Chapter

Skill (includes concepts and practice)

Estimated Completion Time

30 minutes

Overview

When the path of a net traverses a discrete device (resistor, inductor, or capacitor), each net segment is represented by an individual net entity in the board database. Constraint Manager, however, interprets these net segments as a contiguous extended net (Xnet). Xnet creation is based on the presence of the `SIGNAL_MODEL` property on the discrete components. This means that to qualify as an Xnet, the discrete component separating the net into segments must have a valid signal model assigned to it. Design Entry HDL includes Signal Integrity analysis features that support creation of Xnets and model-defined differential pairs through the assignment of valid signal models to various devices.

You assign a signal model to components in Design Entry HDL using the *Model Assignment (SI Analysis)* window. The *Model Assignment (SI Analysis)* window provides an easy way of assigning signal models to multiple components and pins in Design Entry HDL.

When you launch Constraint Manager, it reads the signal models assigned to various components including discretes. Constraint Manager interprets the net, separated by the discrete with a valid signal model, as an Xnet. You can create electrical constraints on the Xnet in Constraint Manager as well as in SigXplorer. You can also apply these constraints to other Xnets in Constraint Manager.

Take the example of the `NET1` net divided by the `R6` discrete. You will assign a valid signal model to the discrete device, `R6`, and to an IC device, `U19`, to create a model-defined differential pair. Then view the Xnet and model-defined differential pair in Constraint Manager. Later, you will launch SigXplorer on the Xnet and set electrical constraints on it in SigXplorer. Consequently, an ECSet will be formed in Constraint Manager. You will then make another Xnet reference this ECSet.

Note: Before you start this exercise, it is recommended that you read the Creating Xnets and Differential Pairs by Assigning Signal Models chapter of *Allegro Design Entry HDL - Constraint Manager User Guide* to learn about the signal integrity features supported by Design Entry HDL in the Constraint Manager flow.

Creating an Xnet in Design Entry HDL

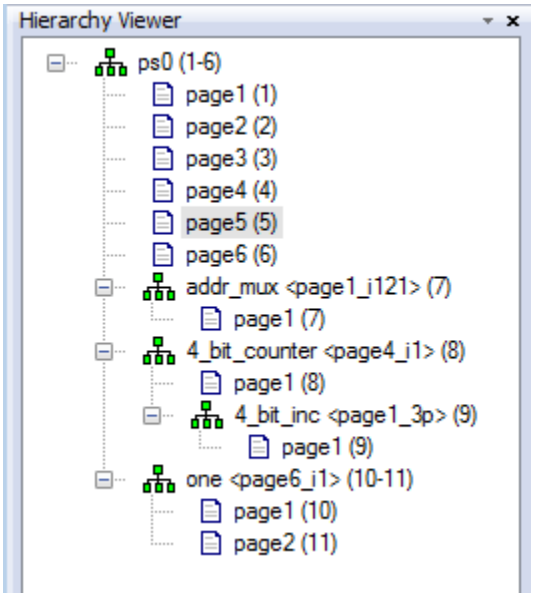
Task Overview

You will create an Xnet by assigning a signal model to the `R6` discrete.

Steps

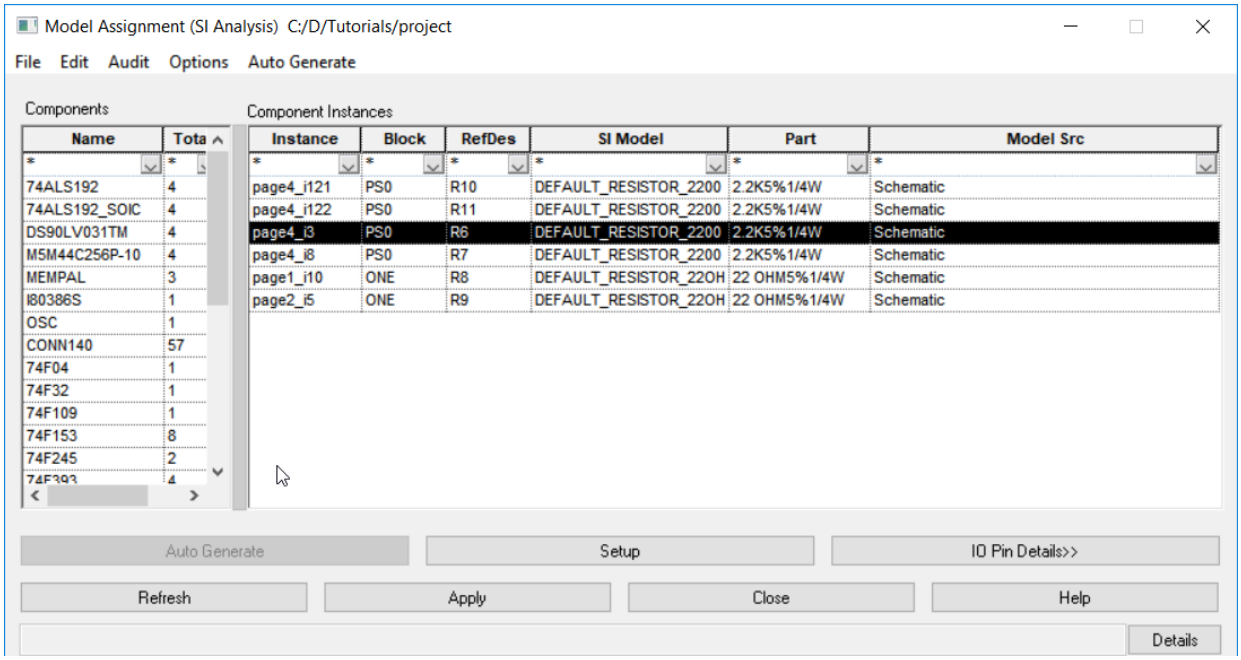
To create an Xnet for the current design, do the following:

1. In Design Entry HDL, navigate to page 5 `(PS0.SCH.1.5)`.



2. Zoom in appropriately to display the schematic drawing clearly.
3. Choose *Tools – Model Assignment*.
4. Minimize the *Model Assignment (SI Analysis)* window.
5. Search for the `R6` resistor instance on the schematic.
6. Right-click the `R6` resistor instance and choose *Highlight on Current Page* in the *Search Result* window.
7. Restore the *Model Assignment (SI Analysis)* window.

The entry for `R6` is selected in the Component Instances pane of the *Model Assignment (SI Analysis)* window.



8. Click *RES* in the *Name* column of the *Components* section.
9. Click the *Auto Generate* button.
10. Click the *Apply* button.

    An appropriate signal model is assigned to `R6`. The `NET1` net will now be interpreted as an Xnet by Constraint Manager.

11. Minimize the *Model Assignment (SI Analysis)* window.
12. Choose *File – Save* to save the drawing.

Creating a Model-Defined Differential Pair in Design Entry HDL

Task Overview

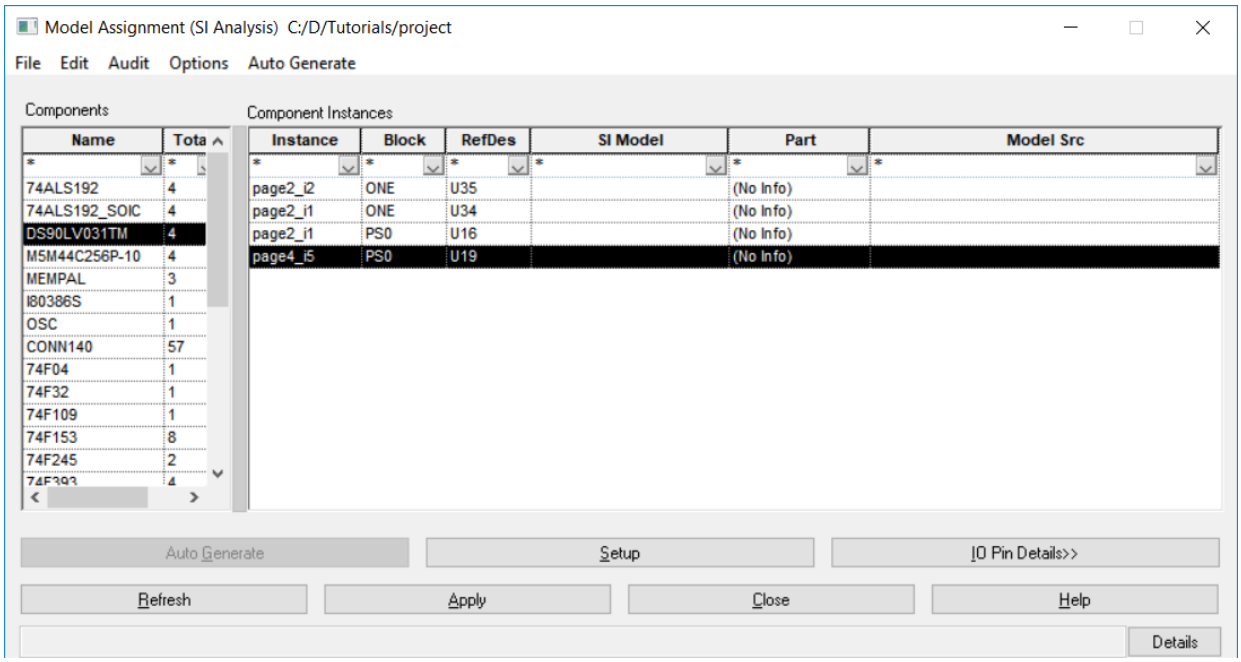
You will set up a path to the device model library, `start.dml`, and assign a model, `DS90LV031TM`, to the component `U19` to create a model-defined differential pair.

Steps

1. Locate the *U19* component instance in the *Model Assignment (SI Analysis)* window by doing the following:

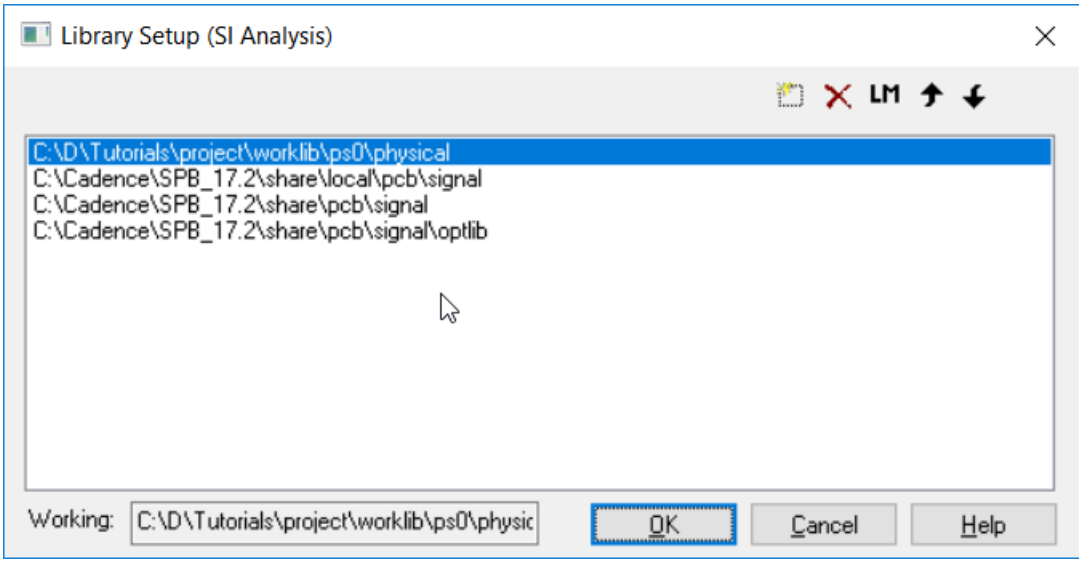
   a. Select `DS90LV031TM` in the Components list on the left pane.

   b. In the Components Instances list on the right pane, click the instance with RefDes *U19*.



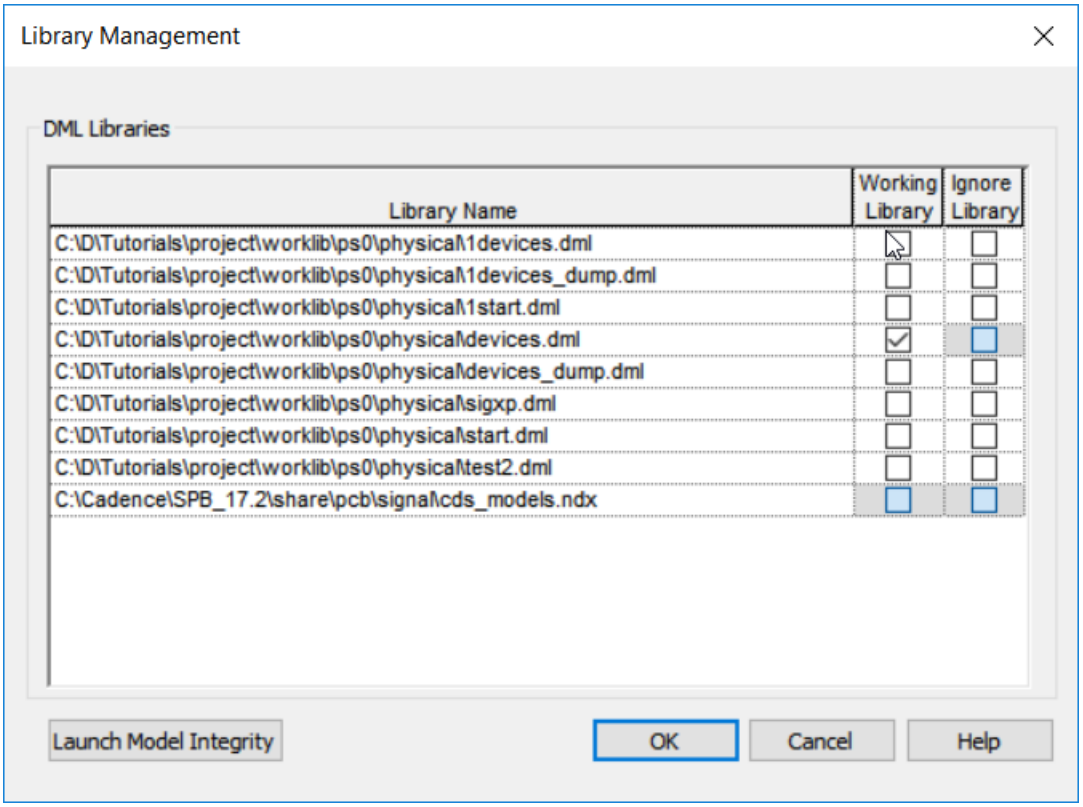
2. Click the *Setup* button.

The *Library Setup (SI Analysis)* dialog appears.



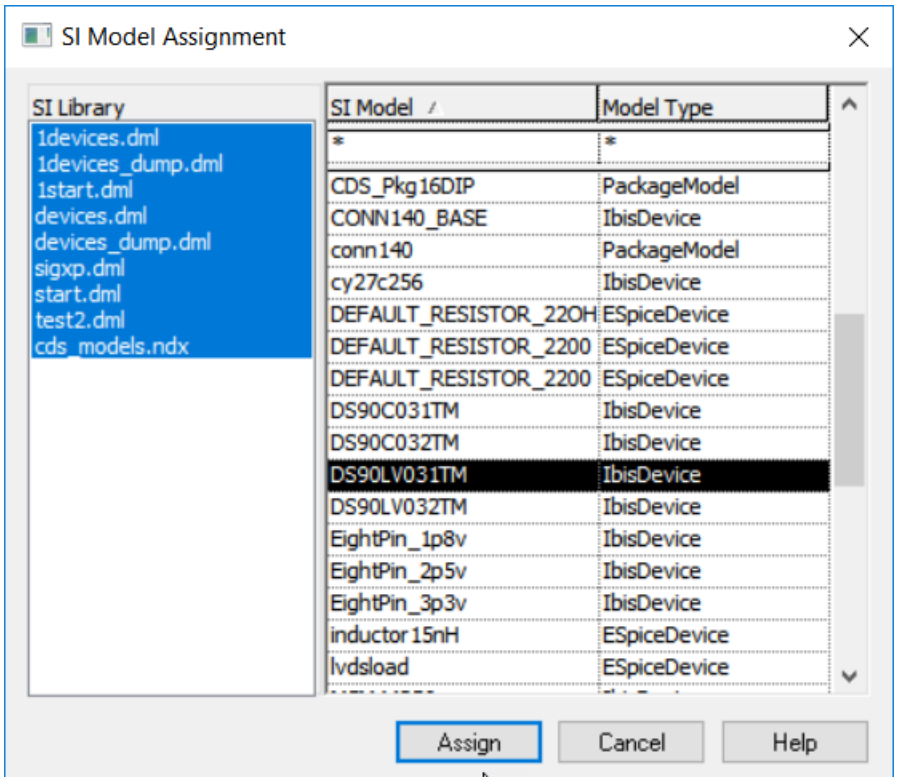
3. Click the *Launch Library Management* button.

The *Library Management* dialog appears with devices.dml already selected.



4. Select the check box under the *Working Library* column for `start.dml`. This removes the selection of the `devices.dml` check box.
5. Click *OK*.
6. Click *OK* in the *Library Setup (SI Analysis)* dialog.
7. In the *Model Assignment (SI Analysis)* window, right-click on *U19* and select *Assign SI Model* from the pop-up menu.

   The *SI Model Assignment* window is displayed.
8. Browse to the signal model *DS90LV031TM* in the *SI Model* column.



If the required model is not available, add the device model library `ps0/physical/start.dml` by doing the following:

a. Click *Cancel* on the *SI Model Assignment* window.

b. Click the *Setup* button on the Model Assignment (SI Analysis) window.

c. Click the *Add a New library* button ( ).

d. Double-click *one* under the worklib folder.

e. Double-click *physical*.

f. Click *OK*.

g. Click *OK*.

h. Open the *SI Model Assignment* window again and assign the *DS90LV031TM* signal model.

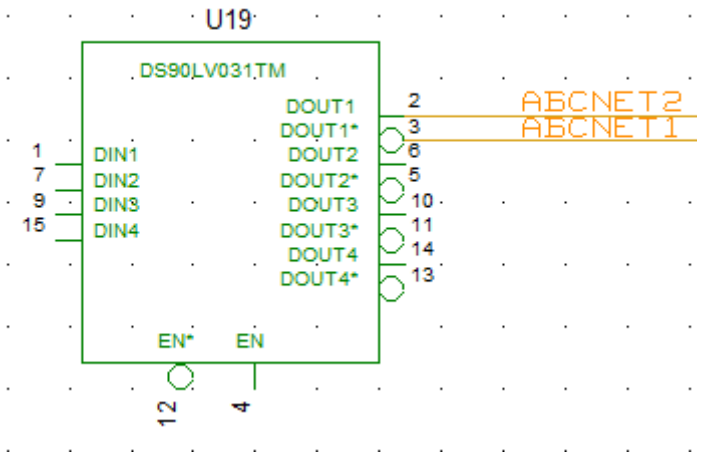
9. Click the *Assign* button.

10. Click the *Apply* button.

11. Click the *Close* button to close the *Model Assignment (SI Analysis)* window.

12. Zoom in again to display the schematic drawing clearly.

The `ABCNET1` and `ABCNET2` nets will now be interpreted as a model-defined differential pair by Constraint Manager.



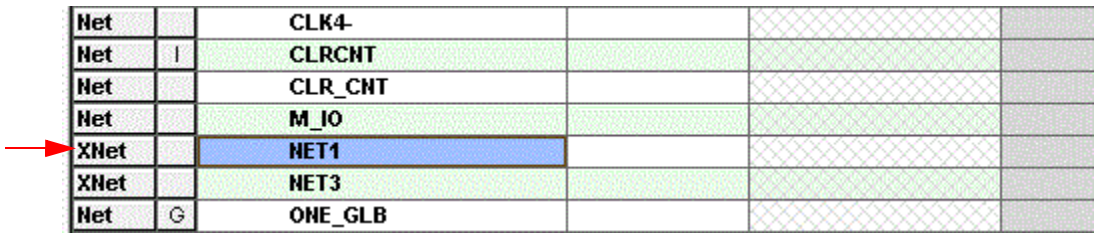
Viewing an Xnet in Constraint Manager

Task Overview

You will view the Xnet and model-defined differential pair you created in the previous exercise in Constraint Manager.

Steps

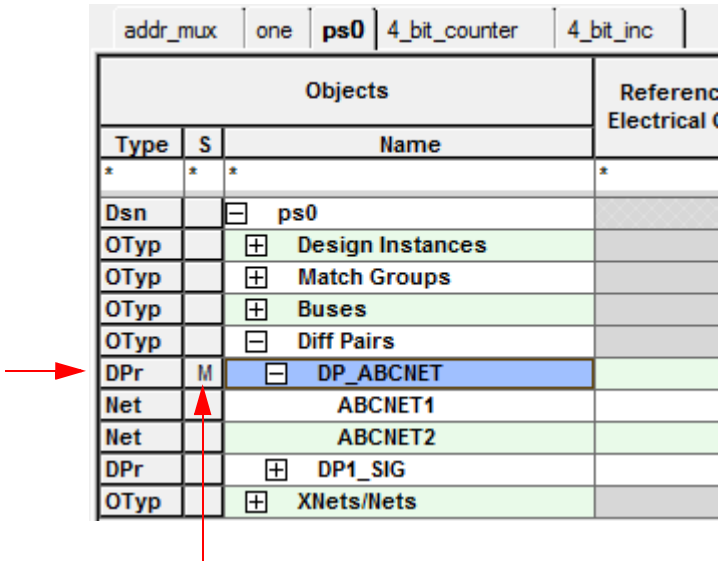
1. Open Constraint Manager from Design Entry HDL by choosing *Tools – Constraints – Edit*.
2. Click *Relative Propagation Delay* under *Routing* in the *Net* workbook.
3. Scroll down and note that the *Type* column for the `NET1` net is now showing the value *XNet* indicating that it is an xnet.



4. Similarly, the value in the *Type* column for the new model-defined differential pair `DP_ABCNET` shows *DPr* indicating that it is a differential pair. The M indicates that this is a model-defined differential pair.

   Note: Constraint Manager reads the nets `ABCNET1` and `ABCNET2` as a differential pair

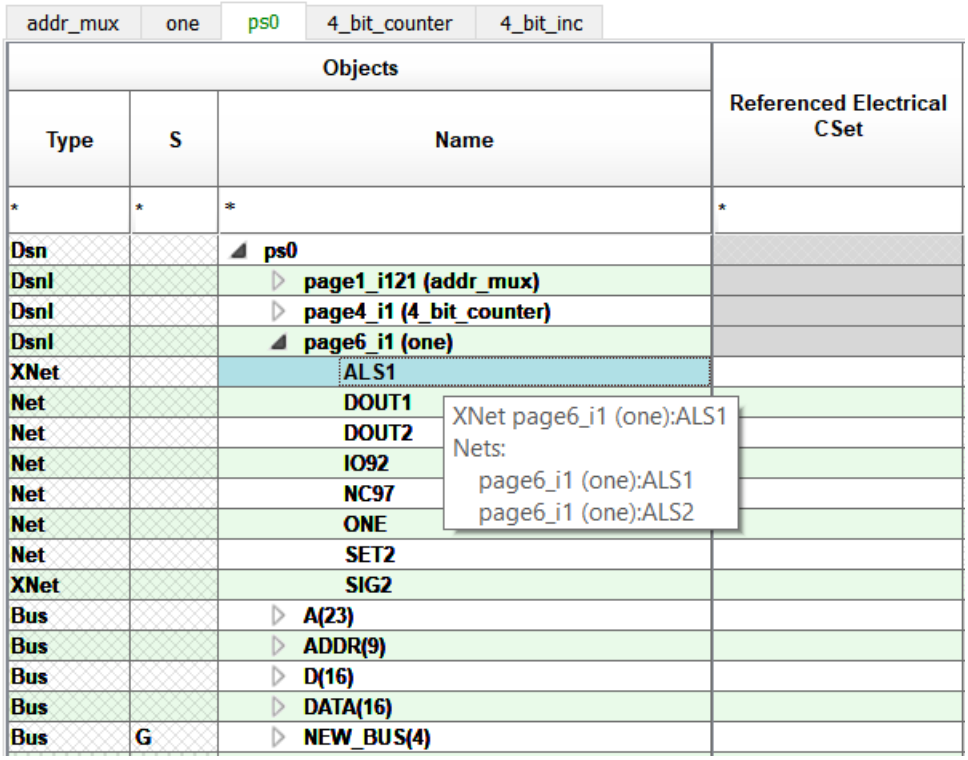
and adds a `DPr_` prefix to the differential pair name.



Xnets in a Lower-Level Block

If you have an Xnet in a lower-level block instantiated in a top-level design, the tooltip appearing on the Xnet shows the entire path to the Xnet. For example, in the following figure,

the tooltip on the `ALS1` Xnet, under the lower-level block `one`, appears as: `XNet page6_i1 (one):ALS1`.



Differential Pairs in a Lower-Level Block

Similarly, for a differential pair in a lower-level block instantiated in a top-level design, the tooltip for the differential pair shows the entire path to the differential pair.

Generating an Electrical Constraint on an Xnet in SigXplorer

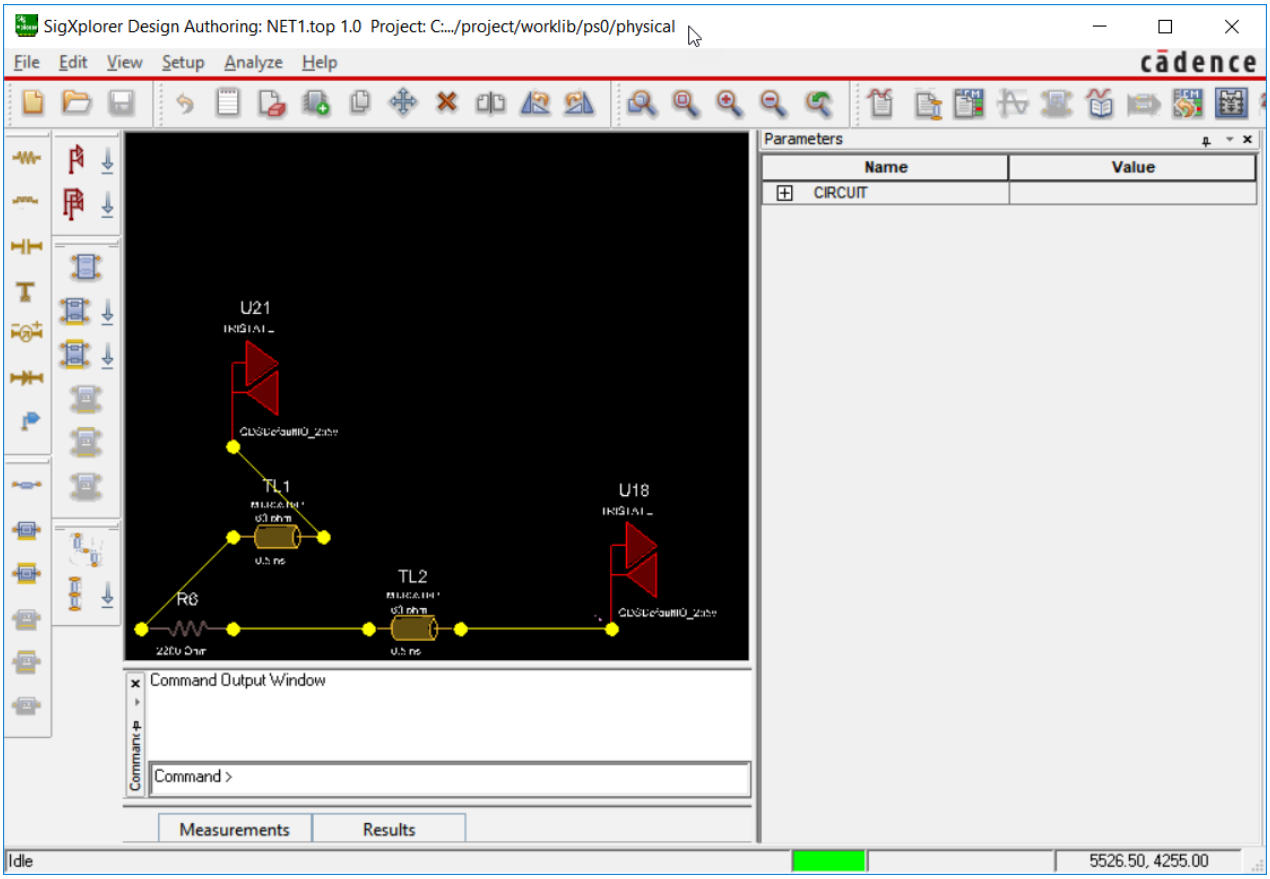
Task Overview

You will generate an electrical constraint for the Xnet you created in a previous exercise in SigXplorer.

Steps

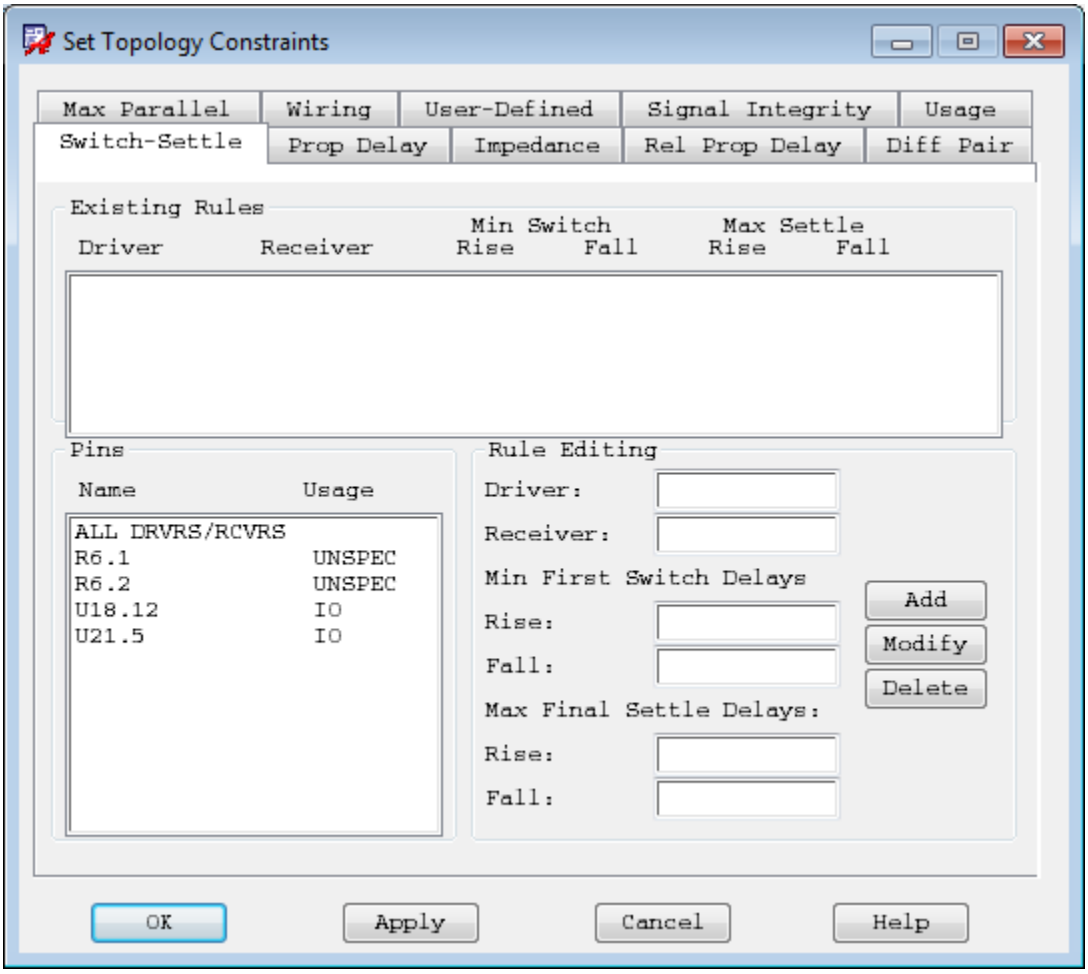
1. Select the *Relative Propagation Delay* worksheet under *Net* workbook of *Electrical* domain.
2. Right-click the `NET1` Xnet and select *SigXplorer* from the pop-up menu.
3.

SigXplorer launches displaying the topology of the `NET1` Xnet.



4. Choose *Setup – Constraints* from the main menu of SigXplorer to generate constraint rules for the `NET1` Xnet.

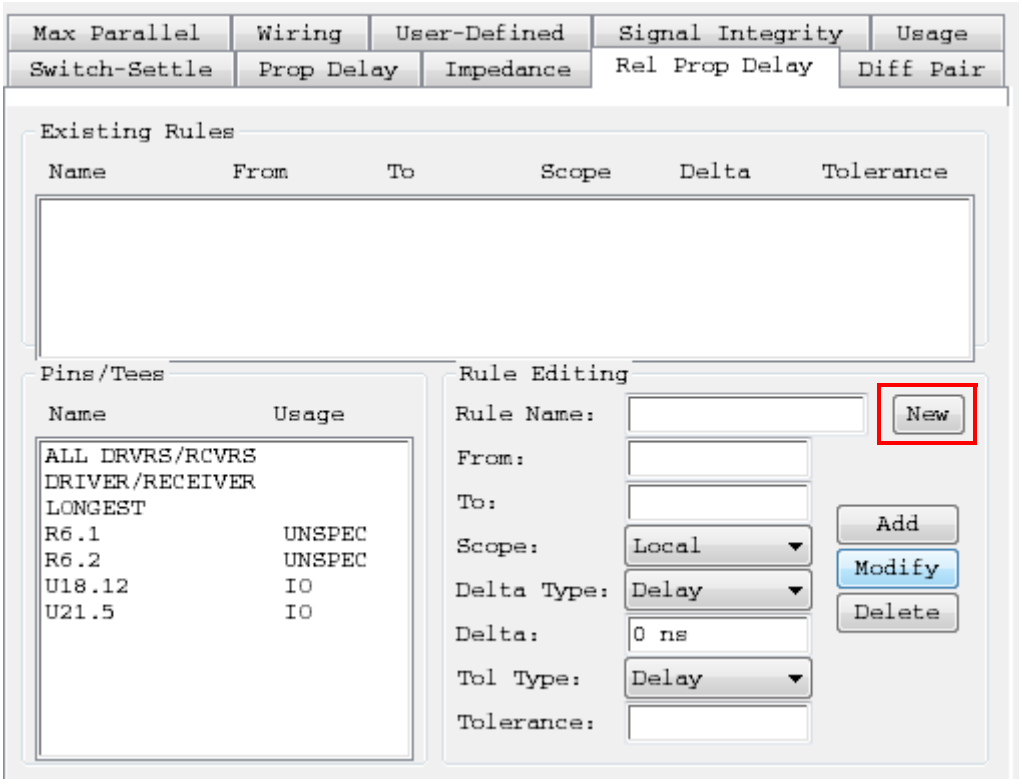
The *Set Topology Constraints* window appears.



5. Click the *Rel Prop Delay* tab.

For Relative Propagation Delay, you specify both `Delta` and `Tolerance` values, and select a `Target`. The `Target` may be implicit or explicit; each pin pair is compared to the `Target` pin pair by the specified `Delta` and within the specified `Tolerance`.

6. Click *New*.



Note that when you click *New*, the *Rule Name* field is automatically filled in with the base name of the topology and a suffix `M1`. Here, it is named as `NET1_M1` after the Xnet, `NET1`. If you add a second rule, the suffix will automatically increment by `1`.

7. Click the entry for *U18.12* in the Pins/Tees section.

   The *From* field is filled in with the appropriate value in the *Rule Editing* section.

8. Click the entry for *U21.5* in the *Pins/Tees* section.

   The *To* field is filled in with the appropriate value in the *Rule Editing* section.

9. Retain the default scope in the *Scope* field.

   Scope controls the validation of the match group. There are three scope options that you can specify:

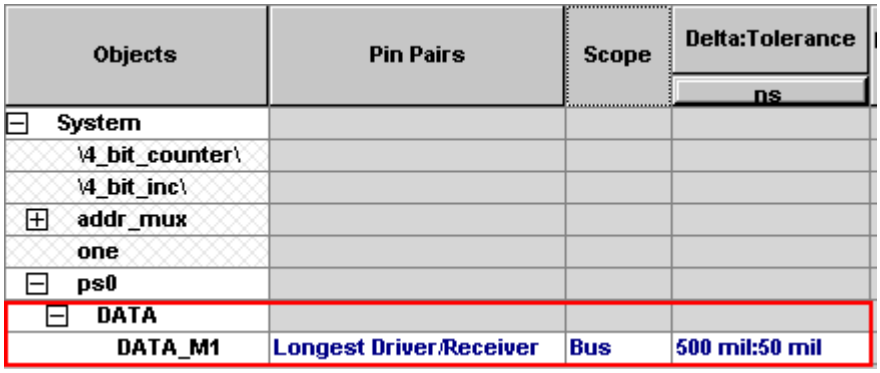
   Local - Validates only pin pairs within each net (or Xnet) against other pin pairs in the same net (or Xnet) for each member of the match group.

   Global - Validates all pin pairs against all other pin pairs in the match group.

Bus - Validates all pin pairs within the same bus and within the same match group by creating a unique match group name for each bus with a scope of Global. A Bus scope optimizes the number of topologies required to constraint a design.

A Bus scope reduces the number of topologies (ECSets) required to constrain a design. A Bus scope is useful in flat designs and replicated blocks where buses (groups of signals) are replicated and the same ECSet needs to be applied to these buses. In the absence of the Bus scope, to constrain these buses, you would require multiple identical ECSets that only differ by the match group name.

When you apply an ECSet to a bus, each bus inherits constraints from the ECSet. For each bus referencing an ECSet, a unique match group is created, where each bus member can be matched to the other member nets. The match group is created with a name derived from the ECSet name and the name of the bus to which the net belongs. In case of a non-bus member, Constraint Manager retains the original name of the match group. In the example shown in the figure below, note the ECSet definition of the `DATA_M1` ECSet.



- If the `DATA_M1` ECSet is assigned to a net in the bus `DATA`, the net will be added to the match group `DATA_M1_DATA`.
- If the net belongs to another bus, let's say `ADDR`, a new match group is created, `DATA_M1_ADDR`.

- If the ECSet is applied to a non-bus member, the net is added to the `DATA_M1` match group. All the other non-bus members referencing this ECSet will be added to this match group.

Objects	Referenced Electrical CSet	Pin Pairs	Pin Del Pin mil	Pin Del Pin mil	Scope	Relat Delta:Tolerance ns
ps0						
\4_bit_counter\ <page4_i1>						
one <page6_i1>						
addr_mux <page1_i121>						
DATA_M1_DATA						
DATA<0>	DATA	Longest Driver...			Global	500 MILS:50 MILS
DATA_M1_ADDR						
ADDR<0>	DATA	Longest Driver...			Global	500 MILS:50 MILS
DATA_M1						
CLK2	DATA	Longest Driver...			Global	500 MILS:50 MILS
net1	DATA	Longest Driver...			Global	500 MILS:50 MILS

Important

In the figure above, note that the match groups appear under the lower-level blocks to which the bus or the nets belong.

Note: You must specify a bus scope for a match group within an ECSet in either the *ECSet* folder or in SigXplorer. You can then apply the ECSet to a bus or a net in the Relative Propagation Delay worksheet. Although you define the bus scope at the *ECSet* level, when the ECSet is applied to a bus member at the *Net* level, the Scope column indicates *Global*.

10. Retain the default value, `0`, in the *Delta* field.

Delta is the value added to, or subtracted from, the routed length of the target net. Constraint Manager uses the Delta to determine the required length of the pin pair before applying the Tolerance.

If the Delta is unspecified, the pin pair must match all other pin pairs in the match group (within the Tolerance). A design rule violation results when the difference is greater than the Tolerance.

11. Type *6* in the *Tolerance* field.

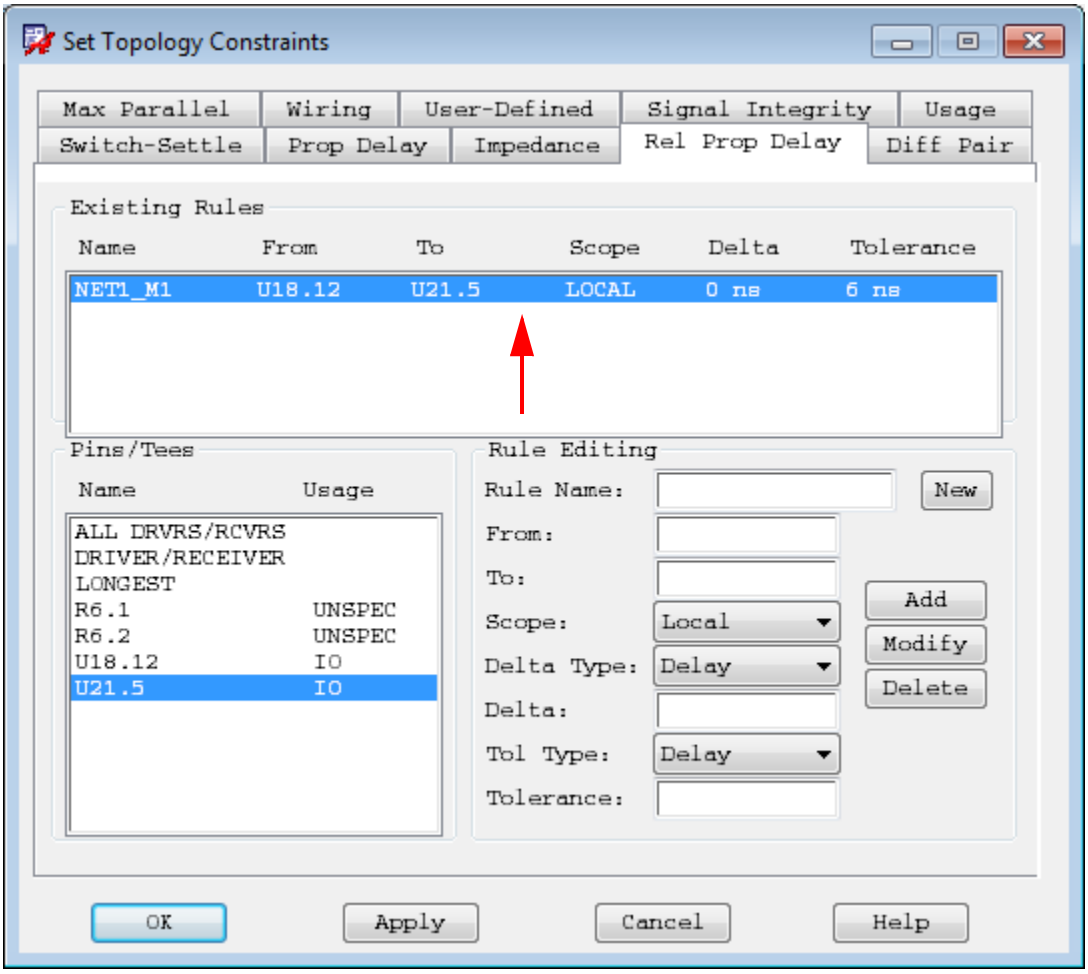
Tolerance is the allowable skew when matching member pin pairs. You specify Tolerance as either length, delay, or a percentage.

If you define only a *Tolerance* value for a member pin pair or for the matched group, the member is compared to every other pin pair within the specified *Tolerance*.

If you define a *Delta* value for a member, the member is matched to the target, plus or minus the *Delta* and within the specified *Tolerance*.

12. Click the *Add* button.

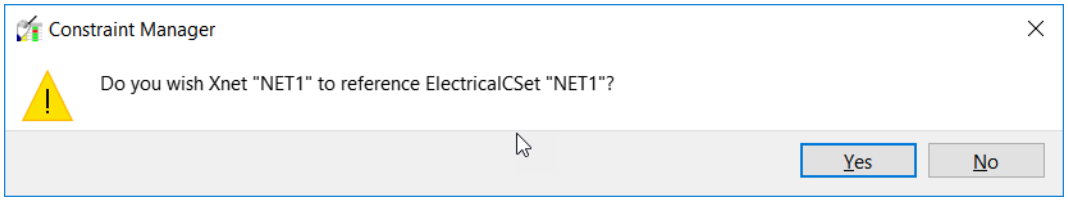
The relative propagation delay constraint that you created is added in the *Existing Rules* section.



13. Click *OK*.

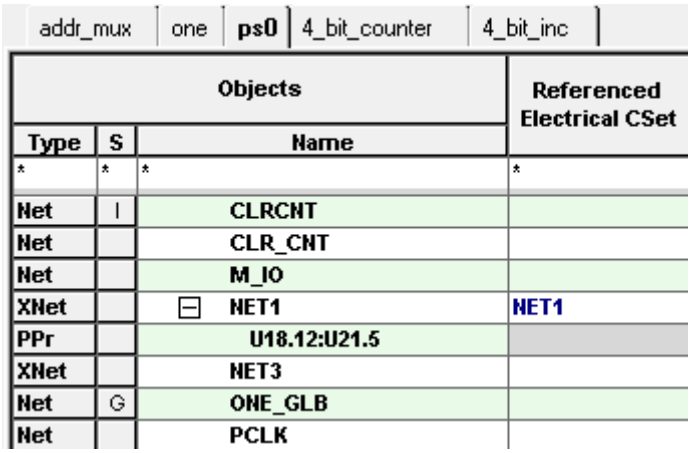
14. Choose *File – Update Constraint Manager* to create a new ECSet—`NET1`—in Constraint Manager for the electrical constraints that you have set on the `NET1` Xnet in SigXplorer.

A confirmation message is displayed.

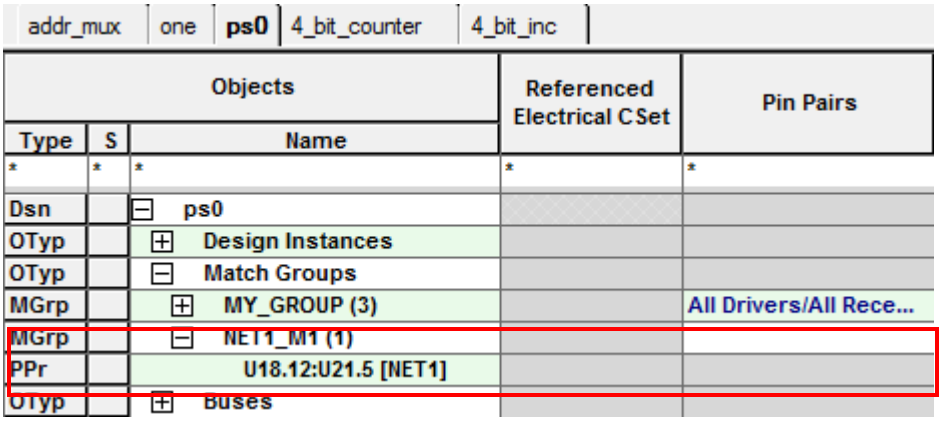


15. Click *Yes*.

Note that the ECSet has been applied to the NET1 Xnet and that the pin-pair constraint you defined has been applied to NET1.



Also note that the ECSet-generated, matched group `NET1_M1` is created.



16. In the SigXplorer window, choose *File – Exit*.

A message box pops up prompting you to save NET1.top. You can choose *Yes* or *No*. Either choice will not affect the steps that follow in the tutorial.

You generated an electrical constraint on an Xnet in SigXplorer and applied it to the Xnet in Constraint Manager.

Applying an ECSet on an Xnet to Other Xnets in Constraint Manager

Task Overview

You will apply the `NET1` ECSet to the `NET3` Xnet in Constraint Manager.

Steps

1. Right-click the entry for the `BHEL` Xnet in Constraint Manager and select *Constraint Set References* from the pop-up menu.

   The *Add to ElectricalCSet* dialog box appears.

2. Select *NET1* from the drop-down list.
3. Click *OK*.

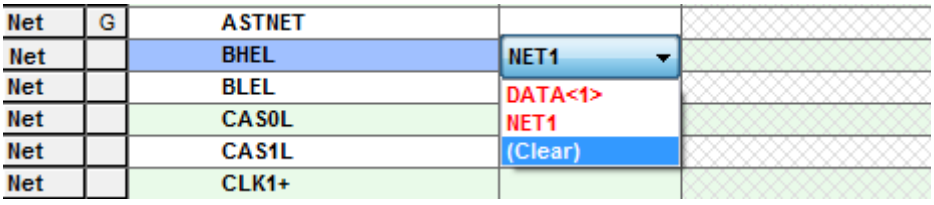
The ECSet is applied and appears in blue in the Referenced Electrical CSet column indicating that the ECSet is applied correctly.

Objects			Referenced Electrical CSet
Type	S	Name	
*	*	*	*
Dsn		ps0	
OTyp		Design Instances	
Dsnl		page1_i121 (addr_mux)	
Dsnl		page4_i1 (4_bit_counter)	
Dsnl		page6_i1 (one)	
OTyp		Match Groups	
MGrp		MY_GROUP (3)	
MGrp		NET1_M1 (2)	
PPr		U18.12:U21.5 [NET1]	
PPr		U22.12:U23.5 [NET3]	
OTyp		Buses	
OTyp		Diff Pairs	
DPr	M	DP_ABCNET	
DPr		DP1_SIG	
OTyp		XNets/Nets	
Net		ADSL	
XNet		ANET	
Net	G	ASTNET	
Net		BHEL	NET1
Net		BLEL	

The ECSet name appears in red in the Referenced Electrical CSet column indicating that an error occurred while applying the ECSet to the net.

Important

Before you move ahead, remove the `NET1` ECSet associated with the net `BHEL`. If you do not remove the ECSet from the `BHEL` net, the sections that follow in this tutorial will not work as documented. To remove an ECSet from a net/Xnet, select *(clear)* from the drop-down list in the Electrical CSet Reference dialog box.



4. Choose *File – Save*.

Video

Now watch this *multimedia demonstration* on creating Xnets and model-defined differential pairs, generating ECSets on Xnets in SigXplorer, and applying the ECSets to other Xnets in Constraint Manager.

Renaming an Xnet

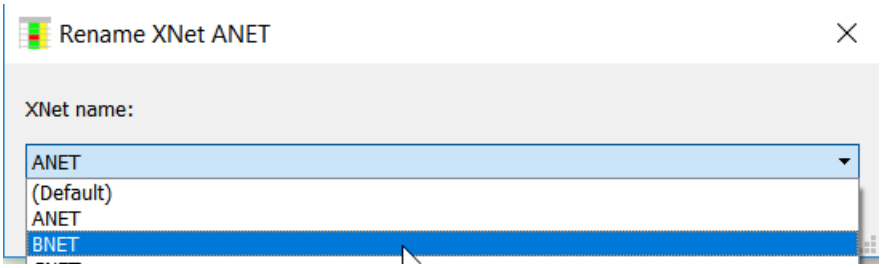
In Constraint Manager, by default, the Xnet name is taken from the lowest alphabetical name of the member nets. However, you can also rename the Xnet to any of its members in Constraint Manager.

Task Overview

You will now rename `ANET`, which comprises nets `ANET`, `BNET`, and `CNET`.

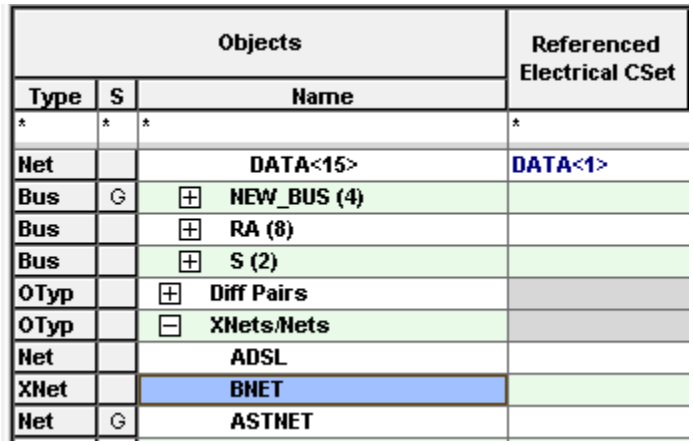
Steps

1. Right-click the entry for the *ANET* Xnet in the *Relative Propagation Delay* worksheet.
2. Choose *Rename* from the pop-up menu.
3. Select *BNET* from the Xnet name drop-down list.



4. Click *OK*.

The name of the Xnet changes to BNET.



Objects			Referenced Electrical CSet
Type	S	Name	
*	*	*	*
Net		DATA<15>	DATA<1>
Bus	G	⊞ NEW_BUS (4)	
Bus		⊞ RA (8)	
Bus		⊞ S (2)	
OTyp		⊞ Diff Pairs	
OTyp		⊟ XNets/Nets	
Net		ADSL	
XNet		BNET	
Net	G	ASTNET	

Note: If at any point in time you want to go back to the default Xnet name, repeat steps 1 and 2. Select *(ANET)* from the Xnet name drop-down list. Click *OK*. The Xnet name changes back to ANET, which in this case is the default name.

5. For this tutorial, rename the net back to ANET.
6. Choose *File – Save*.

Summary

You learned to create an Xnet in Design Entry HDL, view it in Constraint Manager, generate electrical constraints on the Xnet in SigXplorer, and apply the constraints to other Xnets in Constraint Manager. You also learned how to rename an Xnet in Constraint Manager.

What's Next

In the next chapter, Performing ECOs in Design Entry HDL/Constraint Manager, you will make changes to constraints existing on the schematic. You will make changes both in Constraint Manager and Design Entry HDL. The two tools are synchronized when you save the changes.

Recommended Reading

For more information about Xnet creation, see the *Working with Signal Integrity Analysis Features* chapter of the Allegro Design Entry HDL - Constraint Manager User Guide and the Allegro Constraint Manager User Guide.

6

Performing ECOs in Design Entry HDL/ Constraint Manager

Objectives

To learn how to perform Engineering Change Orders (ECOs) in schematic objects and constraints on objects while keeping the constraints and the corresponding electrical properties synchronized

At the end of the lesson, you will be able to

- capture a constraint on an unpackaged net.
- modify a constraint in Constraint Manager.
- delete a constraint in Design Entry HDL.
- create a constraint in Design Entry HDL.
- delete a constraint in Constraint Manager.

Nature of Chapter

Skill (includes concepts and practice)

Estimated Completion Time

40 minutes

Overview

You can make changes in constraints and their corresponding electrical properties after you have added them once and have exited the corresponding tools. Design Entry HDL and Constraint Manager are synchronized when the electrical constraints and schematic are saved in Constraint Manager and Design Entry HDL.

Adding a Net in the Schematic

You can capture a constraint on an unpackaged object in a schematic. At a later point in time, when you package the design, the constraint is retained in the schematic.

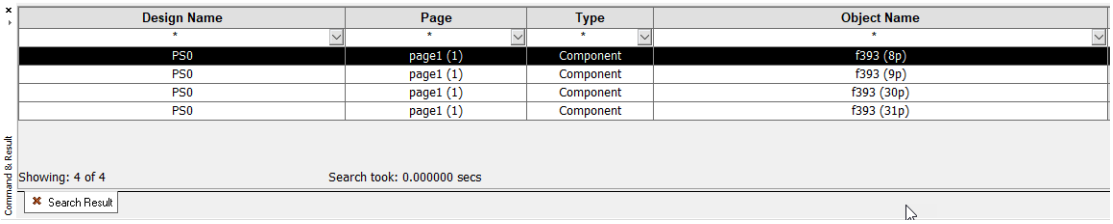
Task Overview

You will add a net, `MY_NET`, between pin `Q0` of `BINARY CTR F393` and pin `I11` of `20R8`. Then you will add an impedance constraint on it. Lastly, you will package your design and view the constraint in Constraint Manager.

Steps

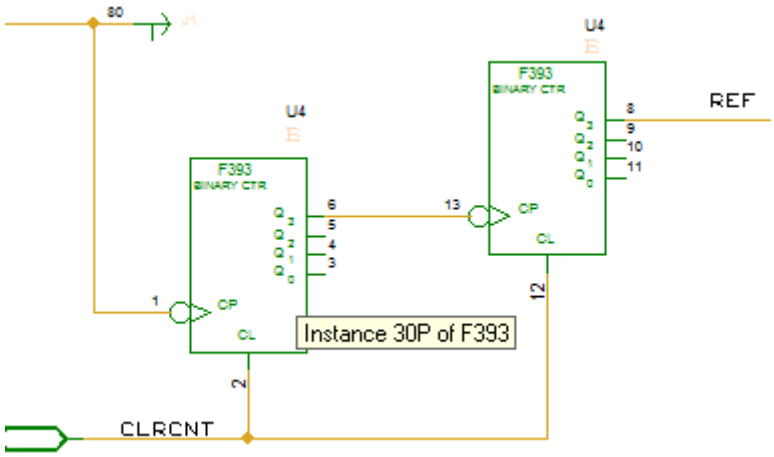
1. In Design Entry HDL, search for the `F393` component using the *Find* dialog.

   The instances of the `F393` component are displayed in the *Search Results* window.



2. Double-click the `f393 (30p)` instance in the *Search Results* window.

The selected instance is zoomed-in on the canvas.

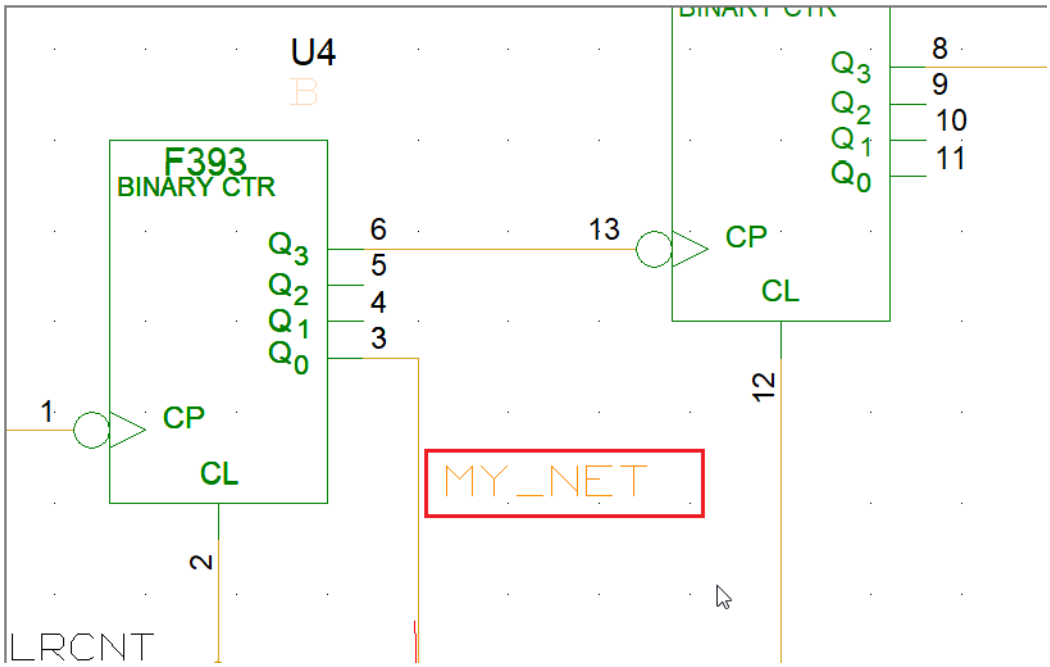


3. Choose *Wire – Route*.
4. Click once on the `Q0` pin of the`30P` instance of `BINARY CTR F393` and again on the `I11` pin of the `24P` instance of `20R8`.

   Pins `Q0` and `24P` are connected.
5. Choose *Wire – Signal Name*.

   The *Signal Name* dialog box appears.
6. Enter the name `MY_NET` in the *Signal Names* field and click the net that you have just added.

7. Close the Signal Name dialog box.



8. Choose *File – Save* to save the newly-added net in the schematic database.
9. Choose *Tools – Constraints – Edit*.
10. Select *Impedance* under *Routing* in the *Net* worksheet of the *Electrical* domain.

    Note that `my_net` appears in lower case while all the other nets appear in upper case. This is because the design has not been packaged after the addition of the `my_net` net.

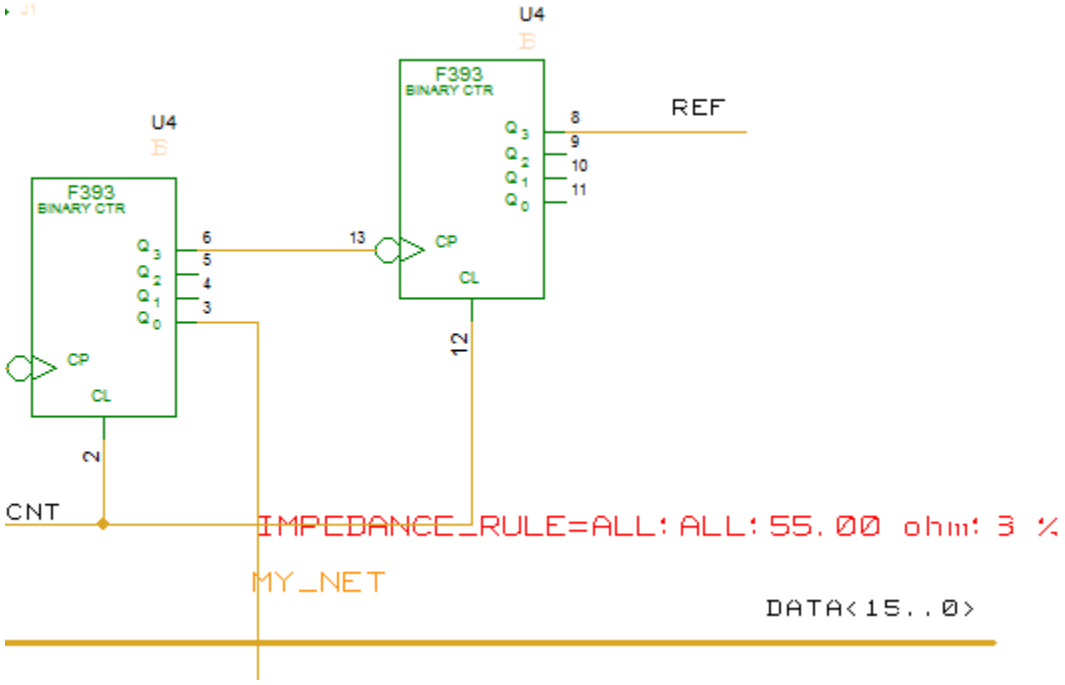
Objects			Referenced Electrical CSet	Sir Target Ohm
Type	S	Name		
*	*	*	*	*
Net		RESETL		
Net		ROMOEL		
Net		UNNAMED_1_F32_115P_A		
Net		UNNAMED_1_F109_10P_C		
Net		UNNAMED_1_F393_30P_Q		
Net		UNNAMED_1_OSC_1P_B		
Net		WEL		
Net		W_R		
Net		my_net		

11. Set the *Single-line Impedance Target* value as `55 Ohm` and *Tolerance* value as `3%` for `my_net`.

12. Choose *File – Save*.

13. Close Constraint Manager.

14. Switch to the Design Entry HDL window and make the `IMPEDANCE_RULE` property visible.



15. Choose *File – Save*.

16. Ensure that the `PADPATH` and `PSMPATH` environment variables are set so that Allegro PCB Editor can access the symbols used in this tutorial. If you need to set these environment variables, first close DE-HDL and to check whether the variables are set, do the following:

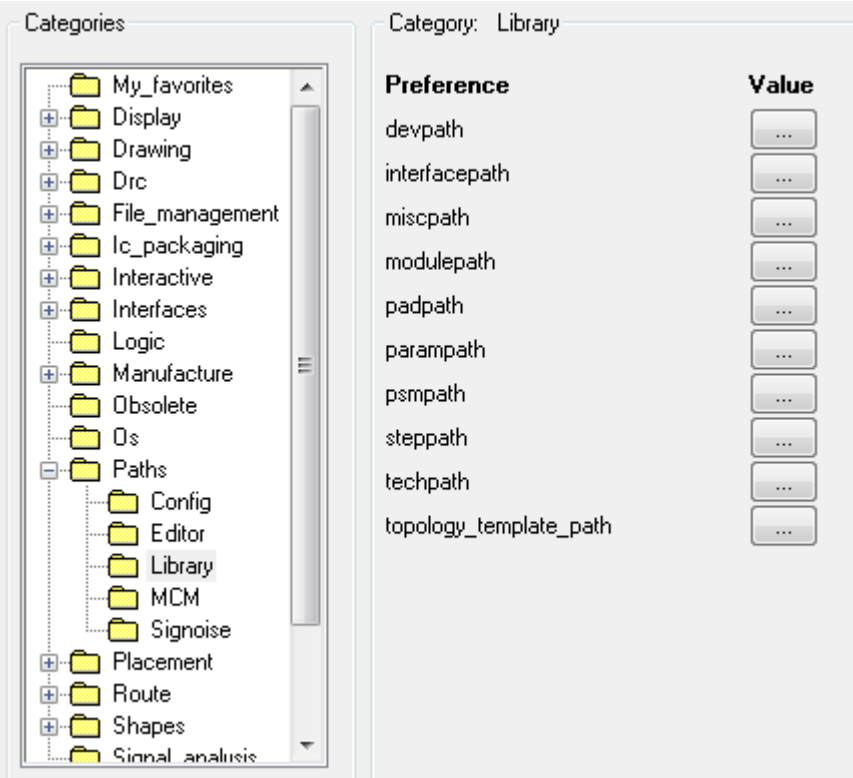
a. Click the Project Manager window.

b. Click the *Setup* button in Project Manager.

c. Select the *Tools* tab in the *Project Setup* dialog.

d. Click the *Setup* button next to PCB Editor in the *Tools* tab.

e. In the *User Preferences Editor* dialog, select *Paths – Library* in the *Categories* list.



f. Click the *Value (...)* button next to *padpath*.

If the path to your symbols directory does not exist, click the *New (Insert)* button ( ) and specify the path. The symbols used in this tutorial are in `<your_proj_dir>/worklib/ps0/physical/symbols`.

Click *OK*.

g. Repeat step *f* for *psmpath*.

h. Click *OK* in the *User Preferences Editor* dialog.

i. Click *OK* in the *Project Setup* dialog.

j. Launch Design Entry HDL from Project Manager.

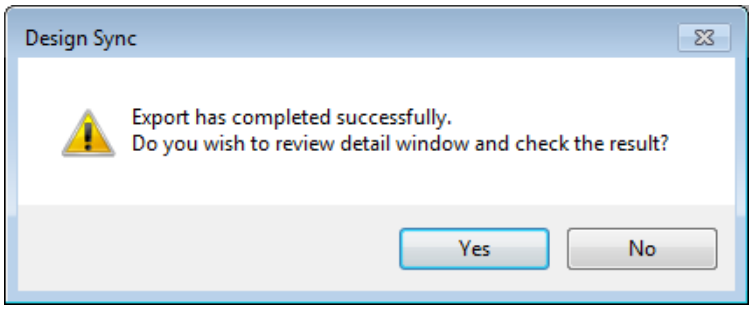
17. Choose *File – Export Physical*.

The *Export Physical* dialog appears.

18. Click *OK*.

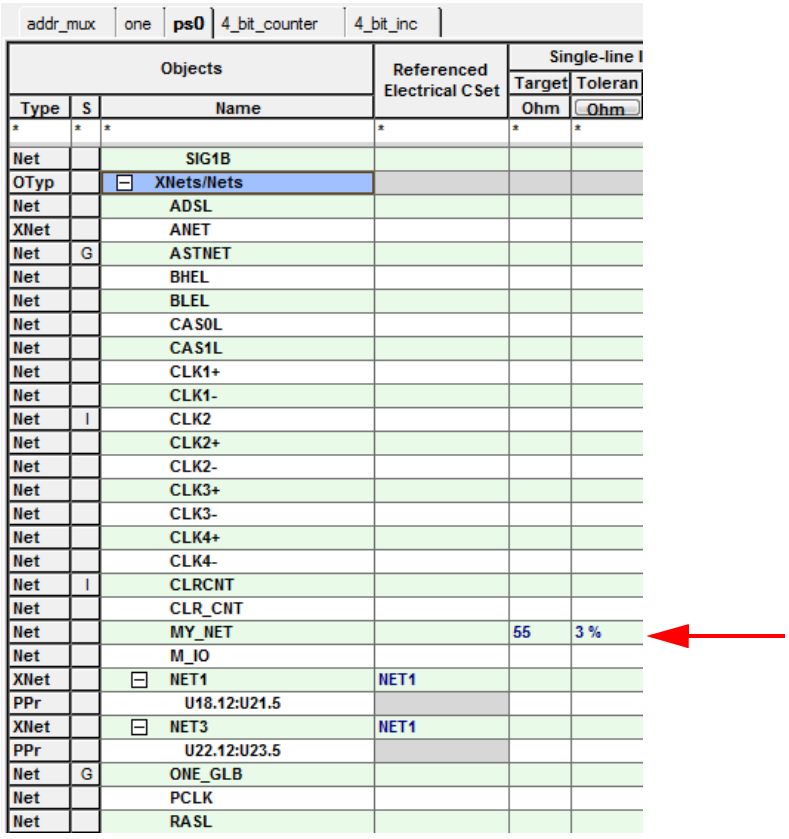
A Progress box displays the progress of the export and a confirmation message id displayed prompting you to review the details and check the result.

19. Click *No*.



20. Choose *Tools – Constraints – Edit* to launch Constraint Manager.

You can now see the net `MY_NET` in uppercase along with the impedance constraint as shown:



21. Close Constraint Manager.

Deleting a Constraint in Design Entry HDL

Deleting a constraint in Design Entry HDL requires exiting Constraint Manager to delete properties in the schematic. If Constraint Manager is running simultaneously with Design Entry HDL, the *Values* column is grayed (disabled) in the *Attributes* dialog box in Design Entry HDL.

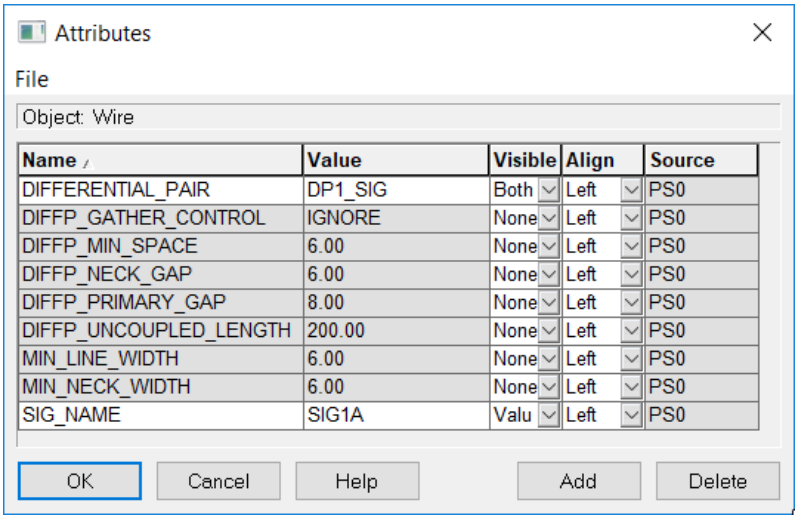
Task Overview

You will delete the `DIFFERENTIAL_PAIR` property for the `SIG1A` and `SIG1B` nets in Design Entry HDL and check that the property is deleted in Constraint Manager.

Steps

1. Click the Design Entry HDL window.
2. Locate the `SIG1A` net using the *Search option* on the search toolbar.
3. Choose *Text – Attributes* and click the `SIG1A` net.

   The *Attributes* dialog box appears. Except for the *Source* column, all the other columns are editable for the `DIFFERENTIAL_PAIR` property.



4. Select the `DIFFERENTIAL_PAIR` property row.
5. Click the *Delete* button.
6. Click *OK*.

Similarly, delete the `DIFFERENTIAL_PAIR` property for SIG1B net.

7. Choose *File – Save* to save the changes to the SIG1A and SIG1B nets.

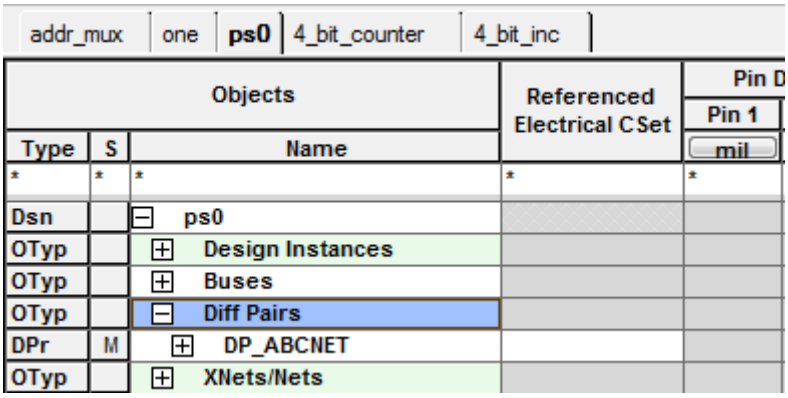
   A netlisting warning is displayed and prompts you to view the warning. Click *No*.

   The warning is that the DIFFERENTIAL_PAIR property value DP1_SIG has been applied to only one net when it should be applied to two nets.

   Ignore the warning.

8. Choose *Tools – Constraints – Edit* to open Constraint Manager.

   The Constraint Manager window appears. In the Net worksheet, click *Routing* then *Differential Pair*. Note that the DP1_SIG differential pair has been deleted in Constraint Manager as well.



Creating a Constraint in Design Entry HDL

You will now create a differential pair with the SIG1A and SIG1B nets. Then you will view the DIFFERENTIAL_PAIR property in Constraint Manager.

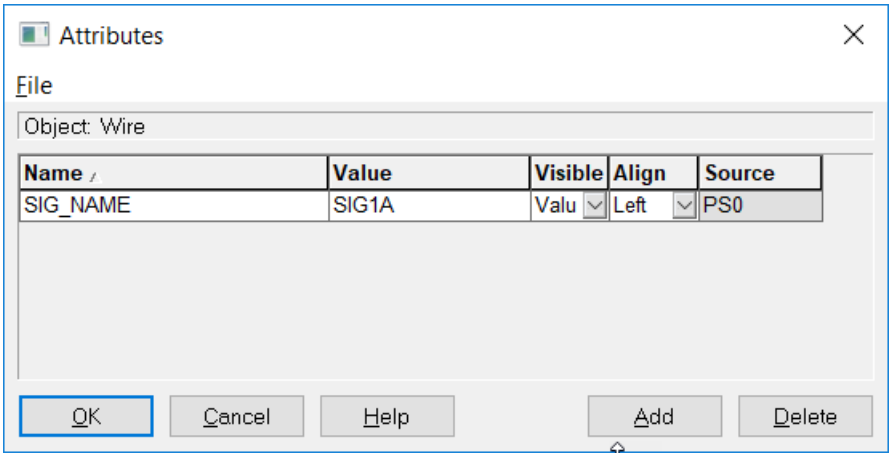
Task Overview

You will create a differential pair constraint for the `SIG1A` and `SIG1B` nets in Design Entry HDL and view it in Constraint Manager.

Steps

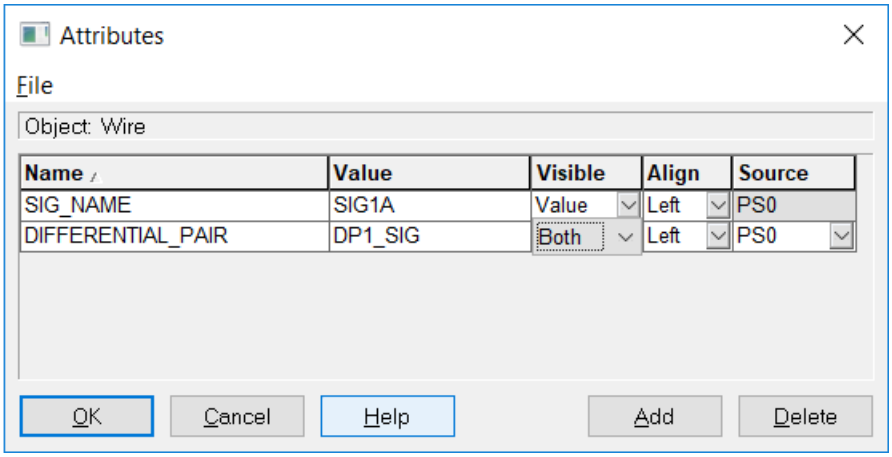
1. Close Constraint Manager.
2. In Design Entry HDL, search for the SIG1A net.
3. Choose *Text – Attributes* and click the SIG1A net.

   The *Attributes* dialog box appears. You can see that the SIG1A net has no DIFFERENTIAL_PAIR property.



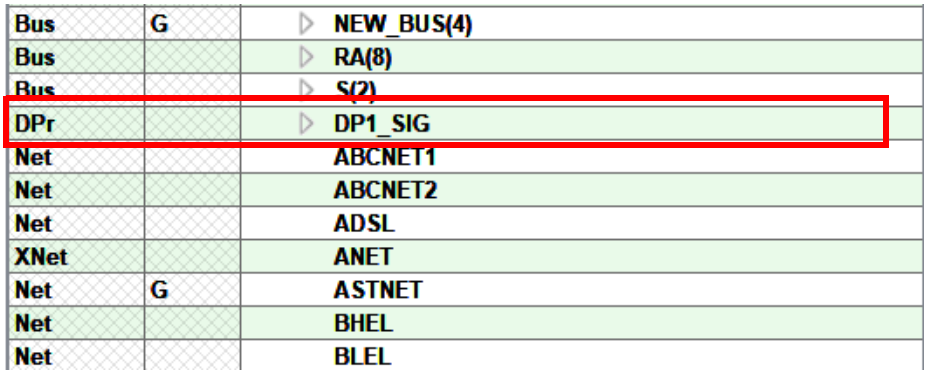
4. Click the *Add* button.
5. Select `Differential Pair` in the *Name* drop-down list.
6. In the *Value* column, type `DP1_SIG`.

7. Select *Both* in the *Visible* column drop-down list.



8. Click *OK*.
9. Repeat steps 2 to 9 for the SIG1B net.
10. Choose *File – Save* to save the new constraints.
11. Open Constraint Manager.
12. In the Net worksheet, click *Routing* then *Differential Pair*.

    The constraint just created in Design Entry HDL is visible in Constraint Manager.



Deleting a Constraint in Constraint Manager

In the preceding sections, we deleted a constraint in Design Entry HDL. You can also delete an electrical constraint in Constraint Manager; the corresponding electrical property is deleted from the schematic.

Task Overview

You will delete the Electrical Properties constraint for the `CLK` net in Constraint Manager and view the change on the schematic.

Steps

1. In Constraint Manager, in the *Net* workbook, select *Signal Integrity*.
2. Select the *Electrical Properties* tab in this workbook.
3. Scroll down to the constraints for the lower-level `CLK` net.

Type	S	Name	Referenced Electrical CSet	Frequency	Period	Duty Cycle	Jitter	Cycle to Measure
				MHz	ns	%	ps	
*	*	*	*	*	*	*	*	*
Dsn		ps0						
Dsnl		page1_i121 (addr_mux)						
Dsnl		page4_i1 (4_bit_counter)						
Dsnl		page1_3p (4_bit_inc)						
Net	I	CIN						
Net	I	CLK		66	15.1515	60	20	2
Dsnl		page6_i1 (one)						
Bus		A(23)						
Bus		ADDR(9)						

4. Delete the existing value in the *Frequency* column for CLK.

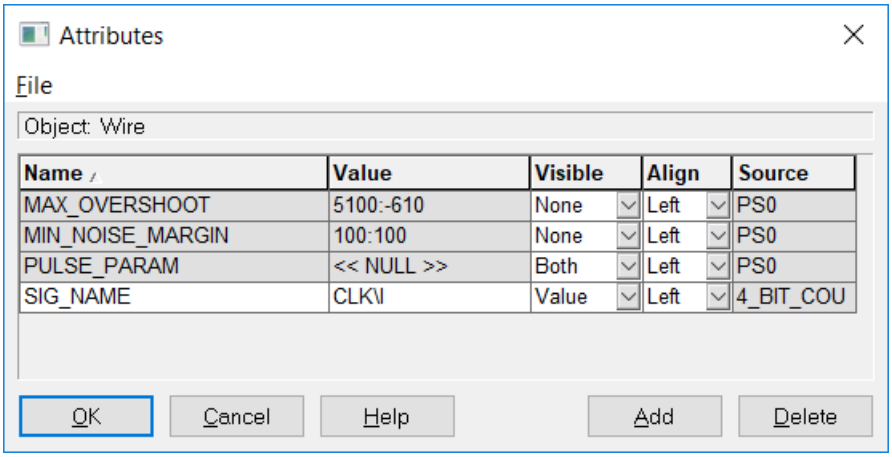
   The values for the constraints *Period*, *Duty Cycle*, *Jitter,* and *Cycle to Measure* are deleted automatically.

5. Choose *File – Save*.

   Constraint Manager updates the design and the property is deleted from the schematic as well.

6. Click the Design Entry HDL window.
7. Locate the `CLK` net.

8. Open the *Attributes* dialog for the CLK net and note that the value of `PULSE_PARAM` is deleted but the property name still exists in the *Attributes* dialog box.



Summary

You have now seen the tight integration between Design Entry HDL and Constraint Manager. You learned to make changes to constraints in Constraint Manager and Design Entry HDL separately and saw that the two tools are synchronized when you save changes.

What's Next

In the next chapter, Synchronizing Constraints Between Schematic and Board, you will learn to propagate constraints on the schematic to the board. You will also learn to propagate the constraints on the board back to the schematic so that the board and the schematic are synchronized.

Recommended Reading

For more information about the integration between Design Entry HDL and Constraint Manager, see the Allegro Design Entry HDL - Constraint Manager User Guide.

7

Synchronizing Constraints Between Schematic and Board

Objectives

To learn how to synchronize electrical constraints captured on the schematic with those captured on the board and vice versa

At the end of the lesson, you will be able to:

- Propagate electrical constraints on the schematic to the corresponding board.
- Propagate electrical constraints on a board to the corresponding schematic.
- Overwrite electrical constraints in the schematic onto those on the board and vice versa.
- Propagate only changed electrical constraints from the schematic to the board and vice versa.

Nature of Chapter

Skill (includes concepts and practice)

Estimated Completion Time

1 hour 10 minutes

Exporting Constraints from Design Entry HDL

After you have created your schematic and added all the constraints relevant during logic implementation, you can transfer the logic to a PCB Editor board. When you create the board, the electrical constraints are also transferred to objects on the board.

Task Overview

You will package your design and create a board file for your design. The board file will contain all the constraints that you have added in the schematic.

Steps

1. Choose *File – Save* in Design Entry HDL.
2. Choose *File – Export Physical*.

   The *Export Physical* dialog appears.
3. Ensure that the *Package Design* check box is selected.
4. Select the *Repackage* option under *Package Option* section.

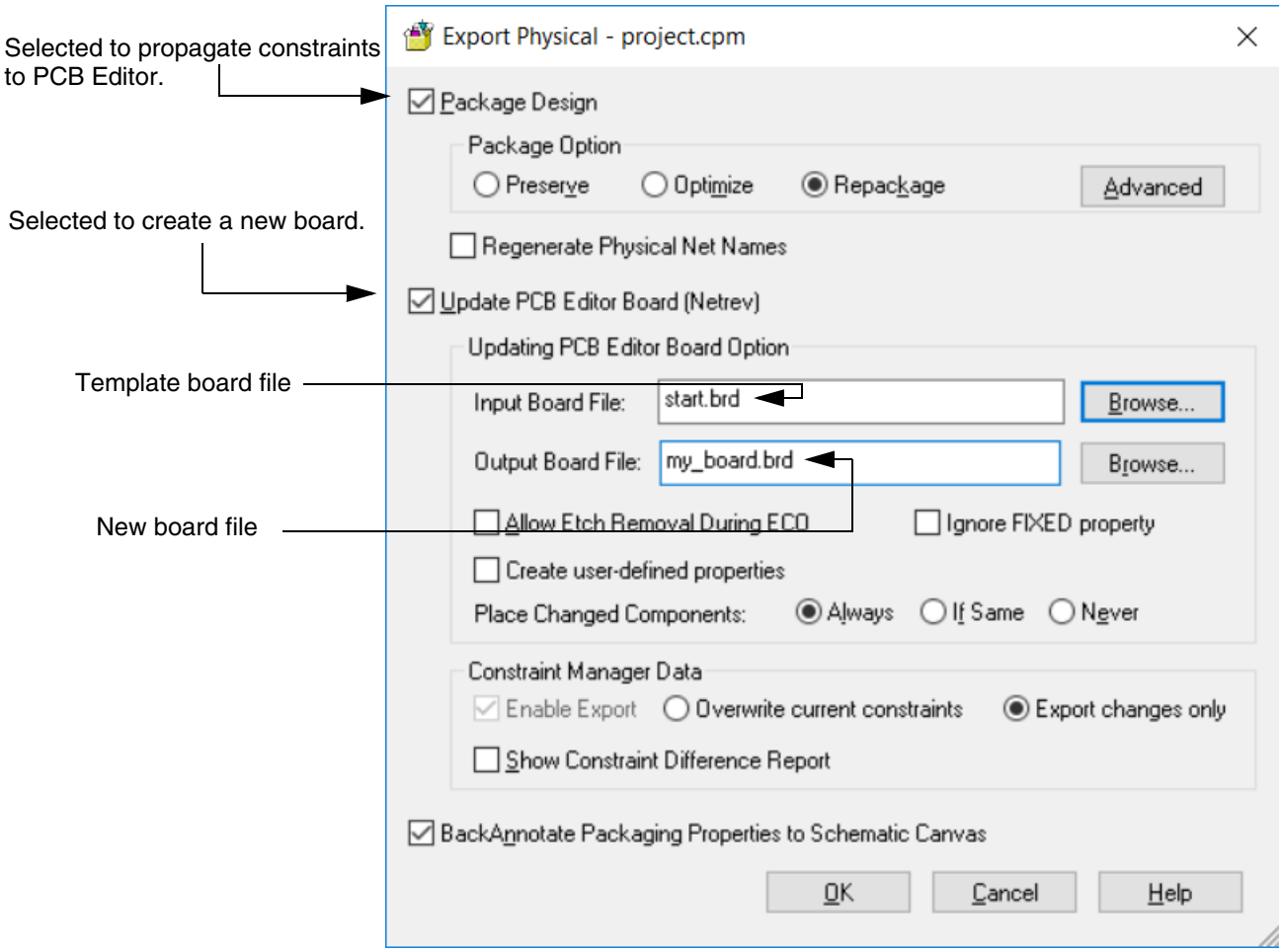
Important

You must package the design when you add new constraints in your design so that they are propagated to the corresponding board.

5. Select the *Update PCB Editor Board (Netrev)* check box.

   The *Input Board File* option contains `start.brd`. This is the input template file for the board that will be created for your design. Ensure that the `start.brd` file is from `worklib\ps0\physical`.

6. Enter `my_board.brd` as the *Output Board File* field.



Note: The *BackAnnotate Package Properties to Schematic Canvas* check box is selected by default. Electrical constraints are automatically backannotated when you run Export Physical.

7. Click *OK*.

   The *Export Physical* dialog closes and the *Progress* window appears. After the packaging is done and the board is created, a *Design Sync* warning box may appear prompting you to view the `netrev.lst` file.

8. Click *No*.

   The *Design Sync* message box closes. Packaging continues then a message box appears prompting you to review the details and check the result.

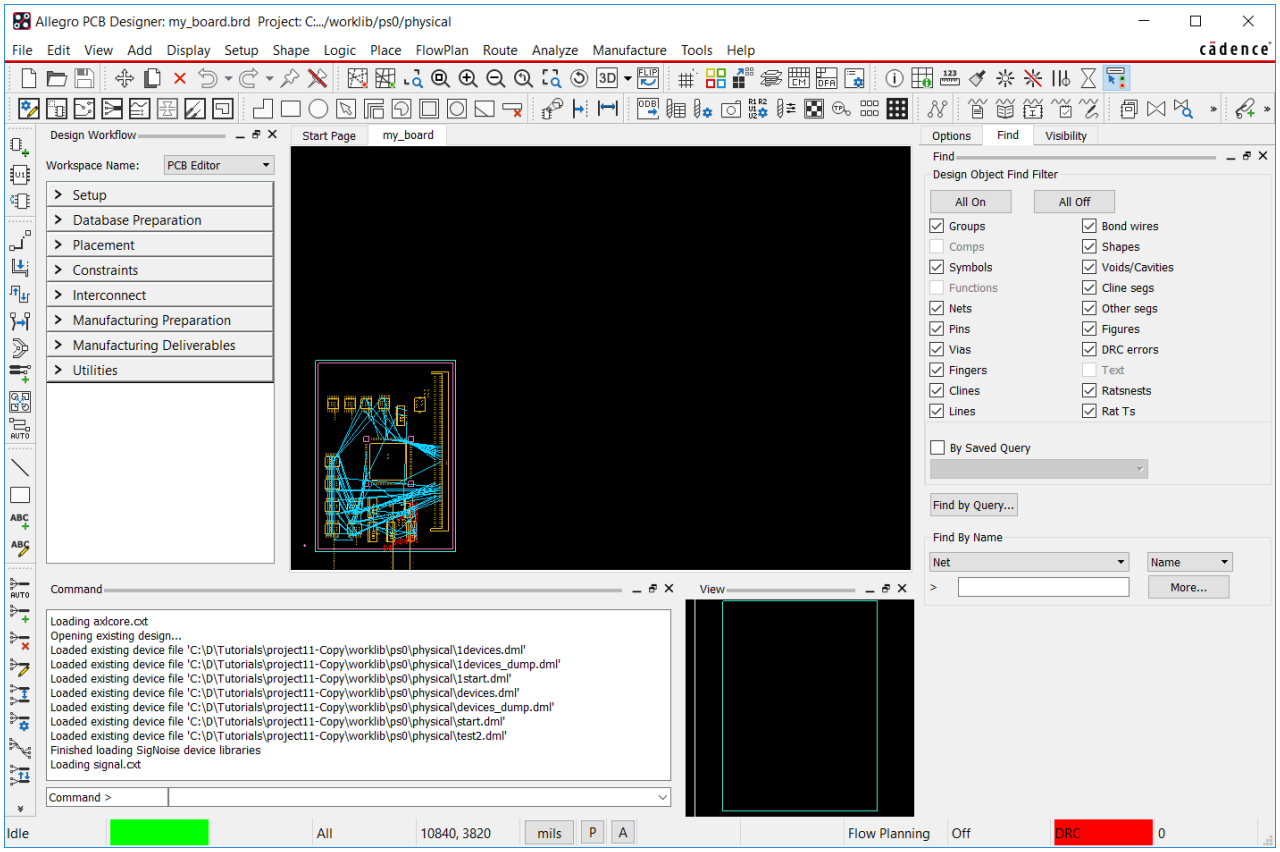
9. Click *No*.

Starting Allegro PCB Editor

Steps

1. Click the *Layout* icon in Project Manager.

   The PCB Editor window opens with the `my_board.brd` board file.



Viewing and Adding Constraints in PCB Editor

The Constraint Manager tool is integrated with Design Entry HDL as well as with PCB Editor. The layout engineer can view the constraints captured on the schematic in PCB Editor by opening Constraint Manager from it. In addition to viewing the constraints captured on schematic, the layout engineer can also:

- Capture constraints relevant to placement and routing of objects on the board.
- Update the constraints captured in the schematic in case the constraints are not in line with the way nets are routed on the board.
- Analyze the values of various constraints.
- Export the results of the analysis, which can then be viewed by the schematic engineer in Constraint Manager connected to Design Entry HDL to see if there are any violations in the constraints set by the engineer.

Task Overview

You will launch Constraint Manager from PCB Editor and then view the Differential Pair constraint on the `SIG1A` and `SIG1B` nets, and edit the differential pair constraint. You will also analyze the constraints and export the results.

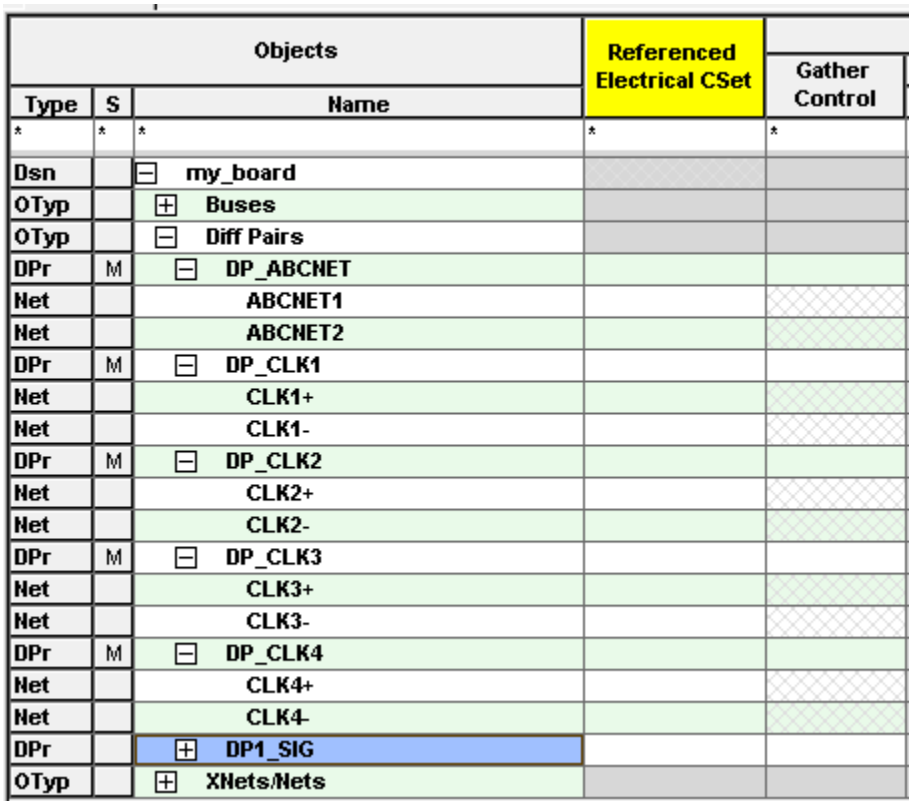
Steps

1. Choose *Setup – Constraints – Constraint Manager* in PCB Editor.

   The Constraint Manager window is displayed.

2. In the worksheet selector, ensure that the *Electrical* tab is selected.
3. In the *Net* workbook, click *Routing* and then click the *Differential Pair* worksheet.

The constraints that you had captured on the nets in Constraint Manager connected to Design Entry HDL were propagated to the PCB Editor database when you packaged the design and created the board using *Export Physical*.



Objects			Referenced Electrical CSet	Gather Control
Type	S	Name		
*	*	*	*	*
Dsn		my_board		
OTyp		Buses		
OTyp		Diff Pairs		
DPr	M	DP_ABCNET		
Net		ABCNET1		
Net		ABCNET2		
DPr	M	DP_CLK1		
Net		CLK1+		
Net		CLK1-		
DPr	M	DP_CLK2		
Net		CLK2+		
Net		CLK2-		
DPr	M	DP_CLK3		
Net		CLK3+		
Net		CLK3-		
DPr	M	DP_CLK4		
Net		CLK4+		
Net		CLK4-		
DPr		DP1_SIG		
OTyp		XNets/Nets		

4. Expand the `DP1_SIG` differential pair.
5. Right-click the `DP1_SIG` differential pair and choose Rename from the pop-up menu.

   The *Rename Diff Pair* dialog box appears.
6. Enter `DP1_REN_PCB` in the *New Diff Pair Name* field.

Important

You may want to change the values of constraints captured in Design Entry HDL in PCB Editor after doing an analysis on the nets on the board.

7. Click the PCB Editor window.
8. Choose *File – Save*.

   PCB Editor prompts you to overwrite the `my_board.brd` file.
9. Click *Yes*.

PCB Editor saves the changes in its database.

10. In the PCB Editor main window, choose *File – Exit*.

    Allegro Constraint Manager also closes.

Importing Constraints in Design Entry HDL

The constraints that you have added on the board need to be propagated to the schematic. This is required to keep the logic in the schematic and the physical design synchronized with each other. The propagation of physical design information to the schematic can be done through the import process in Design Entry HDL.

Task Overview

You will open the Import Physical dialog from Design Entry HDL and import the physical design information from the `my_board.brd` file to your schematic design.

Steps

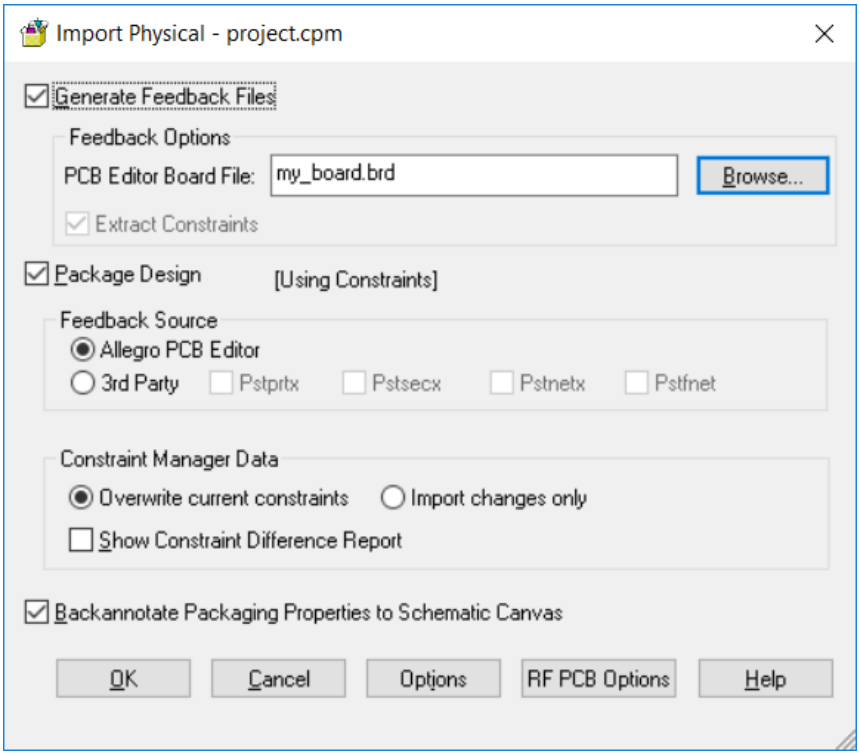
1. Choose *File – Import Physical* in Design Entry HDL.

   The *Import Physical* dialog appears.

2. Select the *Generate Feedback Files* check box.

   Note: Ensure that the *PCB Editor Board File* field is pointing to the `my_board.brd` board file. This is the file from which the electrical constraints will be read.

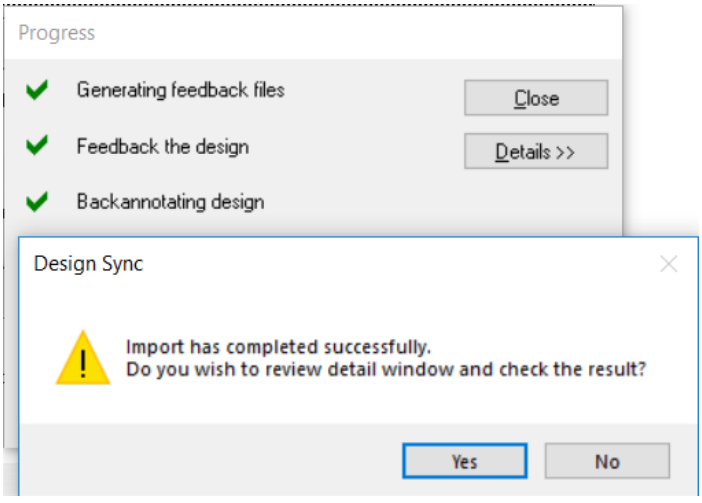
3. Select *Overwrite current constraints* in the *Constraint Manager Data* section.



Note: The *Backannotate Packaging Properties to Schematic Canvas* check box is selected by default.

4. Click *OK*.

The *Progress* window appears. When the import process completes, the *Design Sync* message box appears.



5. Click *No*.

   The *Design Sync* message box closes.

6. Close Design Entry HDL.

 Video

Now watch the *Synchronizing Changes between Schematic and Board* multimedia demonstration.

Summary

You looked at how to propagate electrical constraints from the schematic to the board and conversely. This ensures that constraints in Design Entry HDL and PCB Editor are synchronized.

What's Next

In the next chapter, Handling Lower-Level Constraints, you will learn to generate electrical constraints on a lower-level block, view lower-level constraints in the context of a top-level design, and modify lower-level constraints in the context of a top-level design.

Recommended Reading

For more information, see the Electrical Constraints chapter of the *Allegro Design Entry HDL - Constraint Manager User Guide*.

8

Handling Lower-Level Constraints

Objectives

At the end of the lesson, you will be able to:

- Generate an ECSet on a lower-level block.
- View lower-level constraints in the context of a top-level design.
- Modify lower-level constraints in the context of a top-level design.
- Restore a constraint from its definition.

Nature of Chapter

Skill (includes concepts and practice)

Estimated Completion Time

20 minutes

Overview

The Design Entry HDL-Constraint Manager flow includes support for handling constraints in lower-level blocks in hierarchical designs. You can capture constraints in a schematic block and later pull the constraints into the top-level design by instantiating the schematic block in the top-level design.

We will take the example of a schematic block, **one**, which is instantiated in the top-level design, **ps0**. You will first set **one** as the root design and generate an ECSet on a net in it. Then, you will view the constraints on **one** in the context of the top-level design, **ps0**. Later, you will modify the lower-level constraints in ps0 and finally view the effect of the modification on the original definition in the schematic block, **one**.

Generating an ECSet on a Block

Task Overview

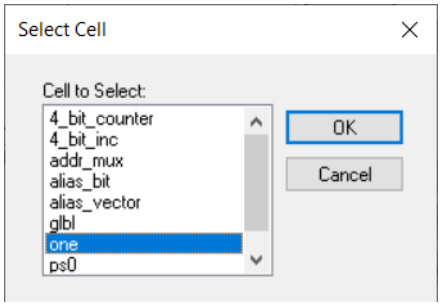
You will generate an ECSet on the `ALS1` Xnet of `one` block.

Steps

1. In Project Manager, click *Setup*.

   Project Setup dialog box is displayed.

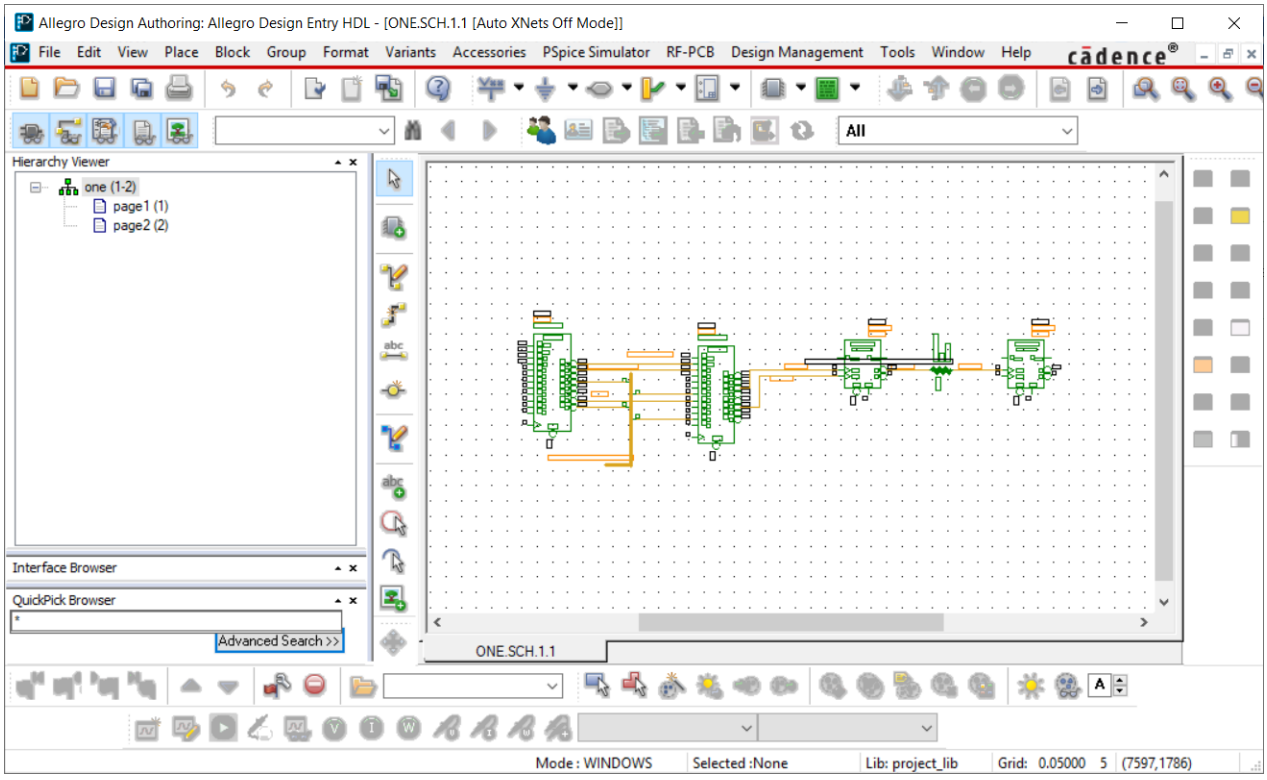
2. In the *Global* tab, click the *Browse* button for the *Design Name* field.
3. Select *one* from the *Cell to Select* list in the *Select Cell* dialog box.



4. Click *OK*.
5. Click *OK* to close the *Project Setup* dialog.

6. In Project Manager, click *Design Entry*.

   The Design Entry HDL main window opens with *one* as the root design.



7. Choose *Tools – Constraints – Edit*.

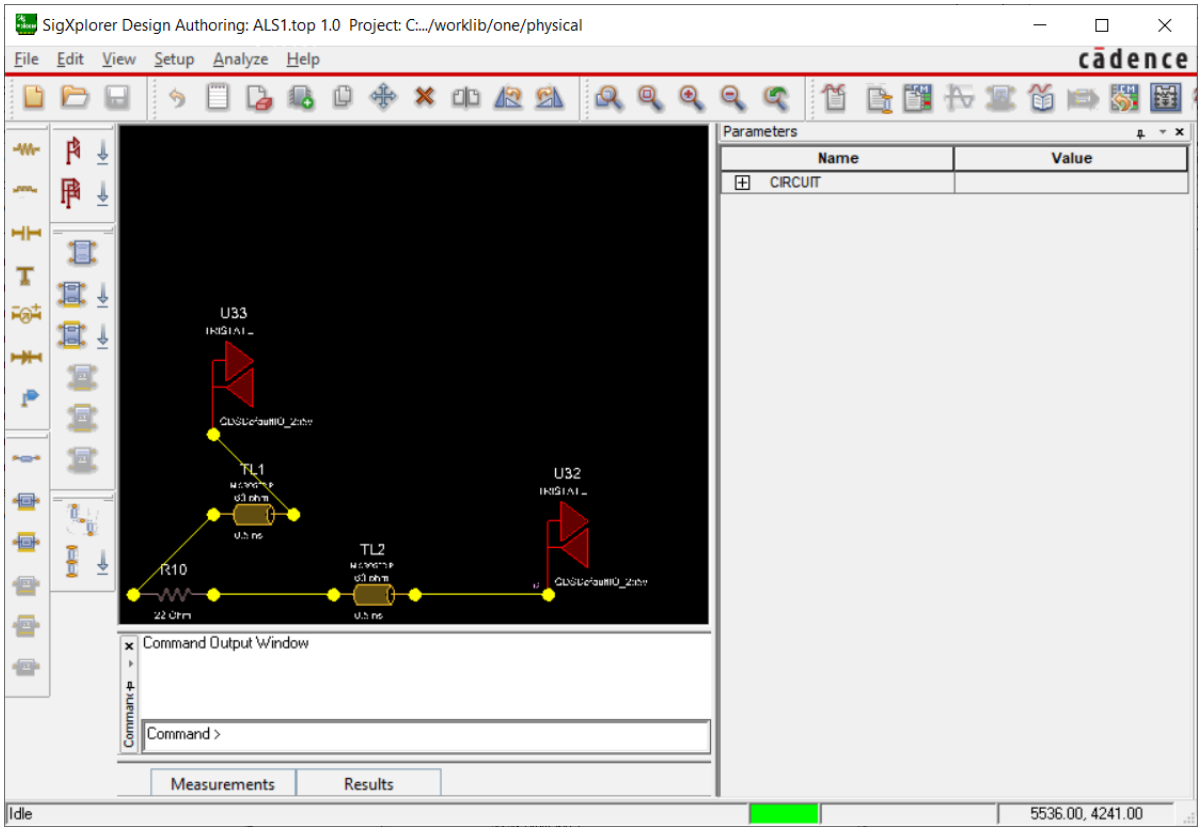
   Constraint Manager appears.

8. Select *Routing* under the *Net* workbook in the *Electrical* domain.

9. Select *Relative Propagation Delay* and expand the *XNets/Nets* tree.

10. Right-click *ALS1 and* choose *SigXplorer* from the pop-up menu.

SigXplorer Design Authoring opens.



11. Choose *Setup – Constraints*.

Set Topology Constraints dialog appears.

12. Click the *Rel Prop Delay* tab.

13. Click *New*.

The *Rule Name* field is filled in with the name `ALS1_M1`. A matched group with this name will be created in Constraint Manager.

14. Click *U32.12* in the *Pins/Tees* section.

The *From* field in the *Rule Editing* section is populated with the pin name `U32.12`.

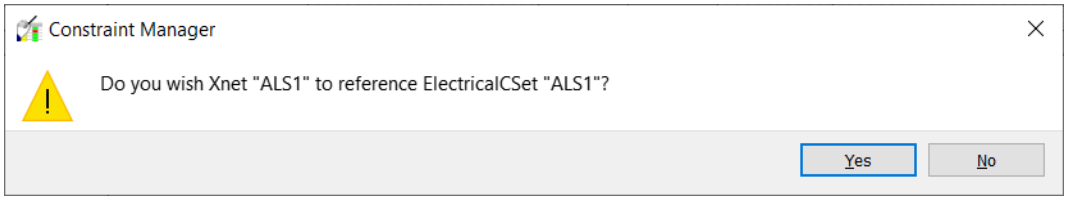
15. Click *U33.5* in the *Pins/Tees* section.

The *To* field in the *Rule Editing* section is populated with the pin name `U33.5`. A pin-pair of the From and To pins will be created in Constraint Manager.

16. Type *6* in the *Tolerance* field.

17. Click *Add*.
18. Click the *Prop Delay* tab to specify the Min/Max Propagation Delay rule.
19. Click *U32.12*.
20. Click *U33.5*.
21. Type *1* in the *Min Delay* field.
22. Type *3* in the *Max Delay* field.
23. Click *Add*.
24. Click *OK* to close the *Set Topology Constraints* dialog.
25. Choose *File – Update* Constraint Manager.

    A message box appears.



26. Click *Yes* to continue.

    Electrical CSet Apply Information window appears.

    The ECSet-created matched group you just created is displayed in the Constraint Manager spreadsheet. The ECSet `ALS1` is also applied to the *ALS1*X net.

Objects			Referenced Electrical CSet	Pin Pairs	Pin Delay		Scope	Delta:Tolerance
Type	S	Name			Pin 1	Pin 2		
					mil	mil		mil
*	*	*	*	*	*	*	*	*
Dsn		one						
MGrp		ALS1_M1(1)						
PPr		U33.5:U32.12 [A...					Local	0 ns:6 ns
Bus	G	NEW_BUS(4)						
XNet		ALS1	ALS1					
PPr		U33.5:U32.12						
Net	G	ASTNET						
Net		DOUT1						
Net		DOUT2						
Net		IO92						
Net		NC97						
Net		ONE						
Net	G	ONE_GLB						
Net		SET2						
XNet		SIG2						

27. Choose *File – Save* in Constraint Manager.

28. Close Constraint Manager.

29. Close SigXplorer.

Click *Yes* if prompted to save `ALS1.top`.

30. Close Design Entry HDL.

You have generated an ECSet on an Xnet in a schematic block.

Viewing Lower-Level Constraints in a Top-level Design

Task Overview

You will view the lower-level constraints in the context of the top-level design, **ps0**, in which the lower-level block is instantiated.

Steps

1. In Project Manager, click *Setup*.

2. Click the *Browse* button for the *Design Name* field in the *Global* tab.

3. Select *ps0* from the *Cell to Select* list of the *Select Cell* dialog box.

4. Click *OK*.

5. Click *OK* to close the *Project Setup* dialog.

6. Click *Design Entry*.

The Design Entry HDL main window opens with `ps0` as the root design.

7. Choose *Tools – Constraints – Edit*.

8. Click *Routing* in the *Net* workbook of the *Electrical* domain.

9. Click the *Relative Propagation Delay* sheet.

Constraint Manager displays the match group `ALS1_M1` under the top-level design `ps0`.

Objects			al	Pin Pairs	Pin Delay		Scope	De
Type	S	Name			Pin 1 mil	Pin 2 mil		
FLTR	*	*		*	*	*	*	*
Dsn		ps0						
MGrp		ALS1_M1(1)						
PPr		U33.5:U32.12 [ALS1]					Local	0 ns:6 ns
MGrp		MY_GROUP(3)		Longest Pin Pair			Global	0 ns:5 %
MGrp		M1(1)						
Net	I	CLRCNT		All Drivers/All Receivers			Local	0 ns:5 %
Bus		A(23)						
Bus		ADDR(10)						
Bus		D(16)						
Bus		DATA(16)						
Bus	I	I3(8)						
Bus	G	NEW_BUS(4)						
Bus		PAGE1_DOUT(8)						

10. Expand *Design Instances* then *page6_i1_(one)*.

Note that the ECSet `ALS1` appears in the Referenced Electrical CSet column of the `ALS1` Xnet.

Objects			al	Pin Pairs	Pin Delay	
Type	S	Name			Pin 1 mil	Pin 2 mil
FLTR	*	*		*	*	*
Dsn		ps0				
MGrp		ALS1_M1(1)				
PPr		U33.5:U32.12 [ALS1]				
MGrp		MY_GROUP(3)		Longest Pin Pair		
MGrp		M1(1)				
Net	I	CLRCNT		All Drivers/All Receivers		
Bus		A(23)				
Bus		ADDR(10)				
Bus		D(16)				
Bus		DATA(16)				
Bus	I	I3(8)				
Bus	G	NEW_BUS(4)				
Bus		PAGE1_DOUT(8)				
Bus		RA(8)				
Bus		S(4)				
DPr		DP1_REN_PCB				
Net		ABCNET1				
Net		ABCNET2				
Net		ADSI				
XNet		ALS1				
PPr		U33.5:U32.12				
XNet		ANET				
Net	G	ASTNET				

You just saw how lower-level constraints appear in a top-level design.

Modifying Lower-Level Constraints in a Top-level Design

Task Overview

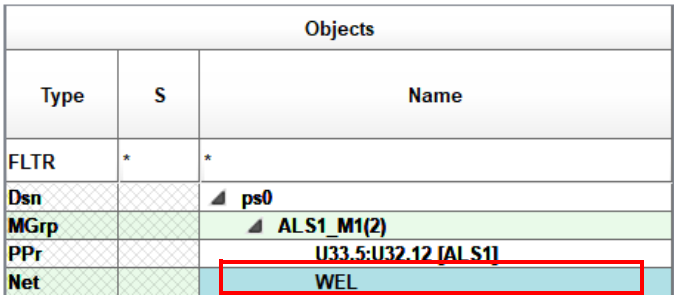
You will now modify constraints defined on the lower-level block, `one`, in the top-level design `ps0`.

Steps

1. In Constraint Manager, under *Net - Routing - Relative Propagation Delay*, scroll down to the *WEL* net under the top-level design.
2. Right-click on the *WEL* net and choose *Add to – Match Group* from the pop-up menu.

   Add To MatchGroup dialog box is displayed.
3. Select *ALS1_M1* from the matched group drop-down list.
4. Click *OK*.

   The net `WEL` is added to the `ALS1_M1` matched group.



5. Change the *Relative Delay Delta:Tolerance* value of the pin-pair to `2ns:8ns`.
6. Choose *File – Save*.
7. Close Constraint Manager.
8. Close Design Entry HDL.

You have modified lower-level constraints on the `ALS1` Xnet. You will now see the effect of this change in the *one* schematic block.

1. In Project Manager, click *Setup*.
2. In the *Global* tabbed page, click the *Browse* button for the *Design Name* field.

3. Select *one* from the *Cell to Select* list in the *Select Cell* dialog box.
4. Click *OK*.
5. Click *OK* to close the *Project Setup* dialog.
6. In Project Manager, click *Design Entry*.

   Design Entry HDL window appears.
7. Choose *Tools – Constraints – Edit*.
8. Select *Routing* under the *Net* workbook in the *Electrical* domain.
9. Select *Relative Propagation Delay* and expand the matched group `ALS1_M1`.

   The changes you made in the top-level design have not propagated to the lower-level block.

Objects			Referenced Electrical CSet	Pin Pairs	Pin Delay		Scope
Type	S	Name			Pin 1	Pin 2	
					mil	mil	
*	*	*	*	*	*	*	*
Dsn		one					
MGrp		ALS1_M1(1)					
PPr		U33.5:U32.12 [ALS1]					Local
Bus	G	NEW_BUS(4)					
XNet		ALS1	ALS1				
Net	G	ASTNET					

10. Close the Constraint Manager window.
11. Close the Design Entry HDL window.

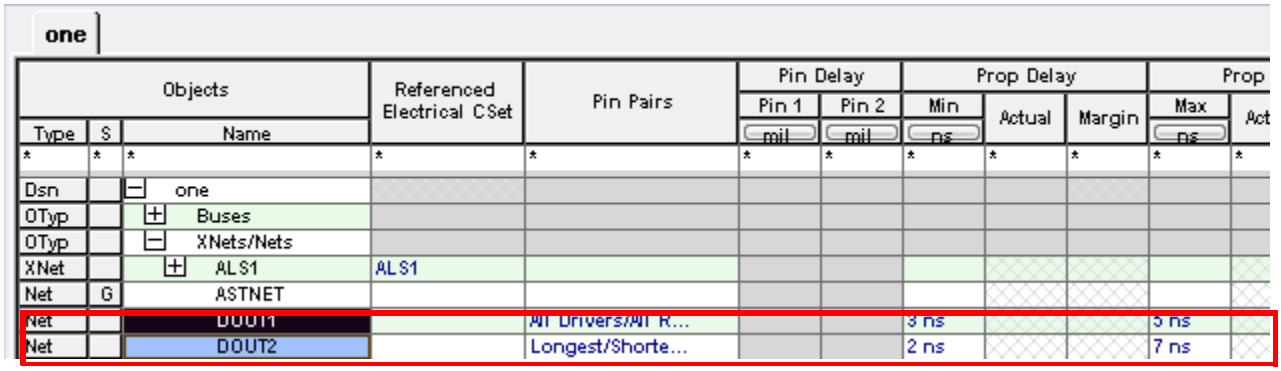
Video

Now watch the *Support for Lower-Level Constraints* multimedia demonstration.

Restoring a Constraint from its Definition

Task Overview

You will now restore the `Min/Max Propagation Delay` constraints overridden in the top-level design, `ps0`, from the lower-level block, `one`. The `Min/Max Propagation Delay` constraints defined on the `DOUT1` and `DOUT2` nets in the lower-level block, `one`, are as follows:



You will first override these in the context of the top-level design, `ps0`, and then restore them from their original definition in `one`.

For information on restoring constraints, see the *Restoring Constraints from Definition* chapter of the *Allegro Design Entry HDL - Constraint Manager User Guide*.

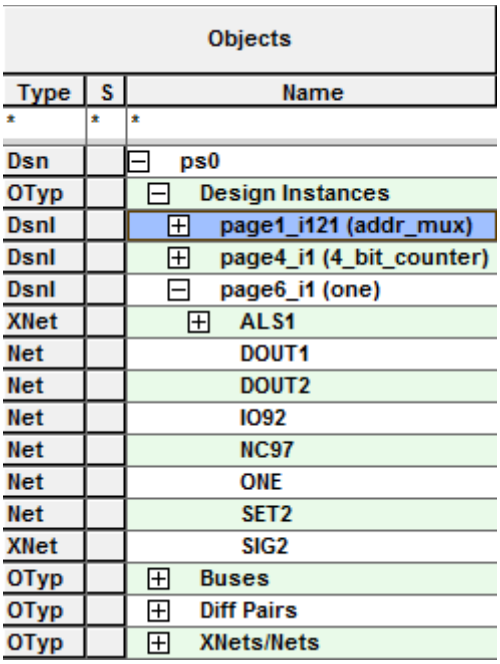
Steps

1. Change the root design to `ps0` in Project Manager by doing the following:

   To do this, perform the step 1 to step 5 of the Generating an ECSet on a Block on page 110 section.

2. In Design Entry HDL, choose *Tools – Constraints – Edit*.

3. In Constraint Manager, under *Net - Routing - Min/Max Propagation Delays*, scroll down to the `DOUT1` and `DOUT2` nets, under design instance `one` in the top-level design, `ps0`.



4. Modify the constraint definition for `Min/Max Propagation Delay` as follows:

   a. For net `DOUT1`, change the value of *Pin Pairs* to *Longest/Shortest Pin Pair*, and change the value of *Min Prop Delay* to `5 ns` and the *Max Prop Delay* to `7 ns`.

   b. For net `DOUT2`, change the value of *Min Prop Delay* to `3 ns`.

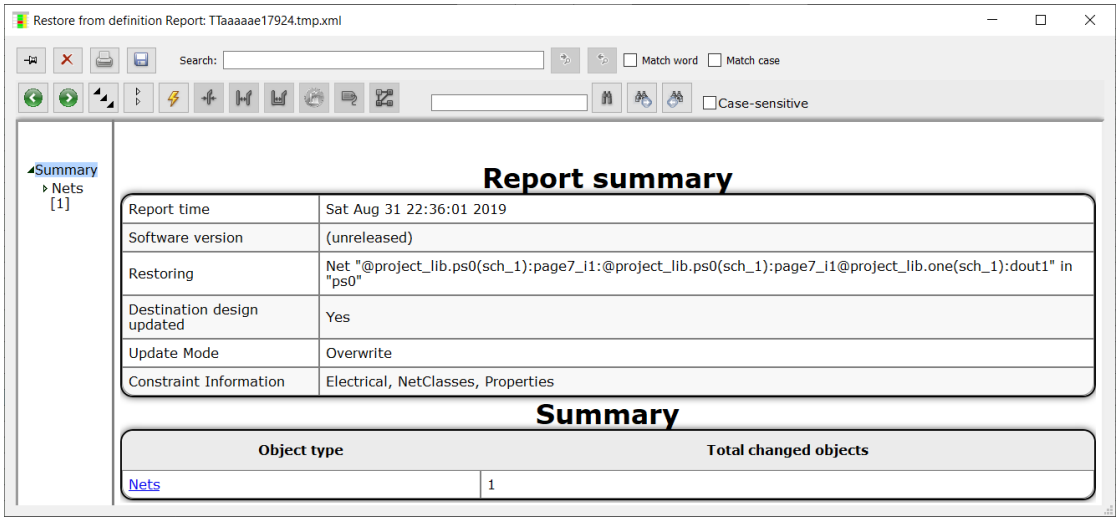
   Note that the constraints on `DOUT1` *and* `DOUT2` appear in bold blue color indicating that the constraints have been overridden.

Objects			Referenced Electrical CSet	Pin Pairs	Pin Delay		Prop Delay			
Type	S	Name			Pin 1	Pin 2	Min	Actual	Margin	Max
					mil	mil	mil			mil
*	*	*	*	*	*	*	*	*	*	*
Dsn		one								
Bus	G	NEW_BUS(4)								
XNet		ALS1	ALS1							
Net	G	ASTNET								
Net		DOUT1		Longest/Shortest Pin Pair			5 ns			7 ns
Net		DOUT2		Longest/Shortest Pin Pair			7 ns			7 ns
Net		IO92								

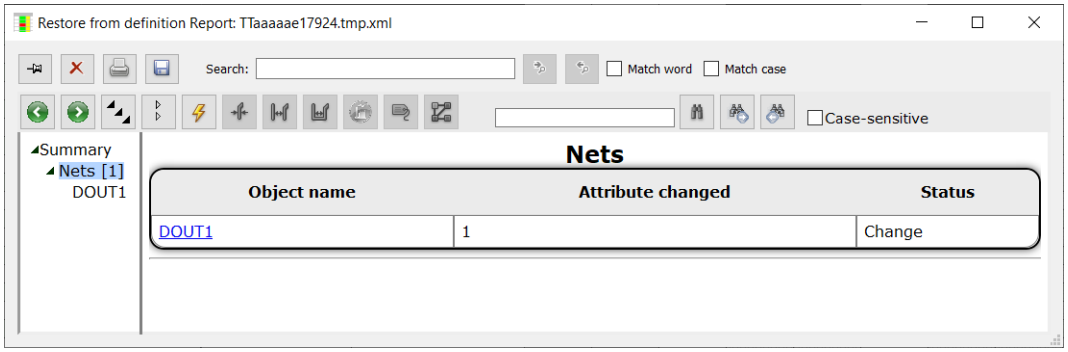
You will now restore the `Min/Max Propagation Delay` constraint from its definition in the lower-level block, `one`.

5. Right-click `DOUT1`, and choose *Restore From Definition – Restore and Report* from the pop-up menu.

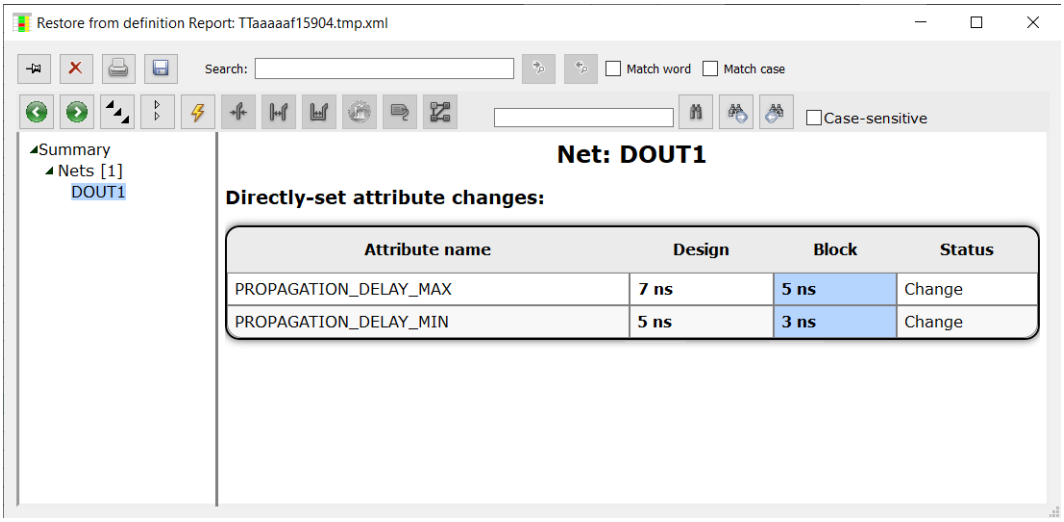
   The *Restore from definition Report* window shows the summary of the changes made to restore the `Min/Max Propagation Delay` constraints on the `DOUT1` net.



6. Click *Nets* to see a detailed report.



7. Click *DOUT1*.



8. Repeat step 5 for net `DOUT2`.

   The `Min/Max Propagation Delay` constraints on `DOUT2` are also restored.

9. Choose *File – Save*.
10. Close Constraint Manager.
11. Close Design Entry HDL.

Summary

In this lesson, you learned how to generate electrical constraints on a lower-level block, view lower-level constraints in a top-level design, and modify lower-level constraints in the context of a top-level design. You also learned that changes made to lower-level constraints in the context of a top-level design are not propagated to the lower-level blocks. Finally, you learned how to restore a constraint from its definition in a lower-level block.

What's Next

In the next chapter, Working with Net Classes, you will learn to create and edit a net class in Constraint Manager.

Recommended Reading

For more information about lower-level constraints, see the Constraints in Hierarchical Designs chapter of the *Allegro Design Entry HDL - Constraint Manager User Guide*.

9

Working with Net Classes

Objectives

To learn how to use net classes in Constraint Manager.

At the end of the lesson, you will be able to:

- identify types of classes.
- create a net class.
- edit a net class membership.
- create a net class-class in Constraint Manager connected to PCB Editor.

Nature of Chapter

Skill (includes concepts and practice)

Estimated Completion Time

20 minutes

Overview

Constraint Manager provides support for the capture of constraints using classes. A net class is created by grouping objects with common features and similar constraints. Using classes allows you to quickly apply similar constraints on all the objects in the same class using CSets.

There are three types of classes in Constraint Manager:

- Electrical classes
- Physical classes
- Spacing classes

You can apply ECSets to electrical classes in Constraint Manager launched from Design Entry HDL. Net classes created for electrical constraints are considered local classes. Physical and spacing net classes are considered global classes.

Creating a Net Class

Task Overview

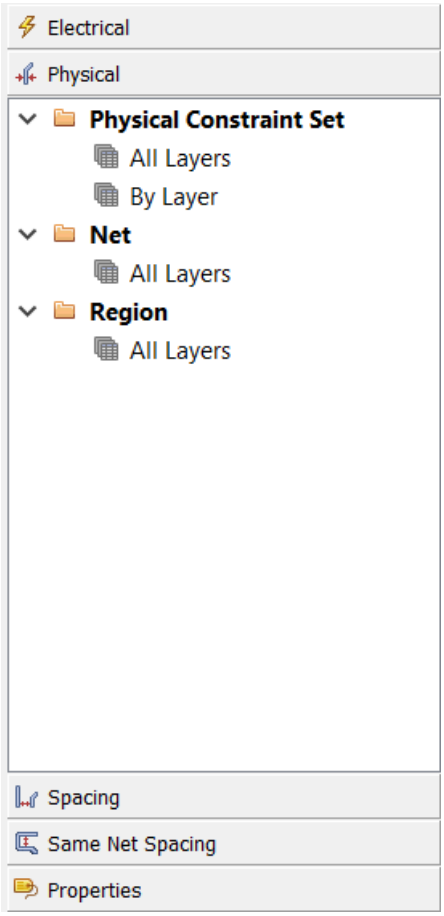
When Constraint Manager is opened from Design Entry HDL, you can only add or modify the membership of physical and spacing net classes. In this exercise, you will create a physical net class.

Steps

To create a new physical net class in Constraint Manager, do the following:

1. Click *Design Entry* in Project Manager.
2. In Design Entry HDL, choose *Tools – Constraints – Edit*.

3. In the worksheet selector, select the *Physical* tab.



4. Click *All Layers* under *Net*.

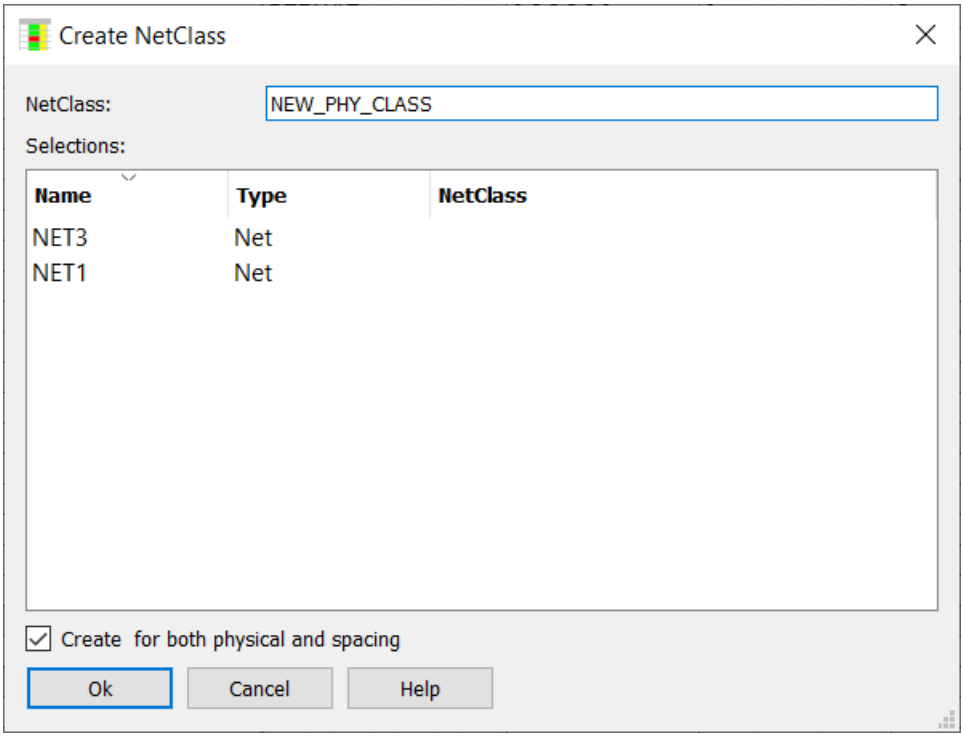
5. Select `NET1` and `NET3`.

Objects			Referenced Physical CSet	Line V
Type	S	Name		Min
				mil
*	*	*	*	*
Bus		RA(8)	DEFAULT	9:5:5:5:5:9
Bus		S(4)	DEFAULT	9:5:5:5:5:9
DPr		DP1_REN_PCB	DEFAULT	9:5:5:5:5:9
Net		ABCNET1	DEFAULT	9:5:5:5:5:9
Net		ABCNET2	DEFAULT	9:5:5:5:5:9
Net		ADSL	DEFAULT	9:5:5:5:5:9
XNet		ANET	DEFAULT	9:5:5:5:5:9
Net	G	ASTNET	DEFAULT	9:5:5:5:5:9
Net		BHEL	DEFAULT	9:5:5:5:5:9
Net		BLEL	DEFAULT	9:5:5:5:5:9
Net		CAS0L	DEFAULT	9:5:5:5:5:9
Net		CAS1L	DEFAULT	9:5:5:5:5:9
Net		CLK1+	DEFAULT	9:5:5:5:5:9
Net		CLK1-	DEFAULT	9:5:5:5:5:9
Net	I	CLK2	DEFAULT	9:5:5:5:5:9
Net		CLK2+	DEFAULT	9:5:5:5:5:9
Net		CLK2-	DEFAULT	9:5:5:5:5:9
Net		CLK3+	DEFAULT	9:5:5:5:5:9
Net		CLK3-	DEFAULT	9:5:5:5:5:9
Net		CLK4+	DEFAULT	9:5:5:5:5:9
Net		CLK4-	DEFAULT	9:5:5:5:5:9
Net	I	CLRCNT	DEFAULT	9:5:5:5:5:9
Net		CLR_CNT	DEFAULT	9:5:5:5:5:9
Net		M_IO	DEFAULT	9:5:5:5:5:9
Net		NET1	DEFAULT	9:5:5:5:5:9
Net		NET2	DEFAULT	9:5:5:5:5:9
Net		NET3	DEFAULT	9:5:5:5:5:9
Net		NET4	DEFAULT	9:5:5:5:5:9
Net	G	ONE_GLB	DEFAULT	9:5:5:5:5:9
Net		PCLK	DEFAULT	9:5:5:5:5:9
Net		RASL	DEFAULT	9:5:5:5:5:9
Net		RDYL	DEFAULT	9:5:5:5:5:9

Net NET3

6. Right-click on the two selected nets and choose *Create – Class*.

7. In the Create Net Class dialog box, specify the name of the net class as `NEW_PHY_CLASS`.



Note: The *Create for both physical and spacing* box is checked by default. This indicates that a class will be created in both, the *Physical*, and the *Spacing* domains. If you want to create a physical or a spacing class only, uncheck this option. The resulting class will be physical or spacing depending on the tab from which you launched the Create Net Class dialog box. In this exercise, we have launched the dialog box from the *Physical* worksheet. Since the check box is selected, a corresponding *Spacing* class will also be created.

8. Click *OK*.

A new net physical and spacing class is created.

Objects			Referenced Physical CSet
Type	S	Name	
*	*	*	*
Dsn		ps0	DEFAULT
Dsnl		page1_i121 (addr_mux)	
Dsnl		page4_i1 (4_bit_counter)	
Dsnl		page6_i1 (one)	
NCls		NEW_PHY_CLASS(2)	DEFAULT
Net		NET1	DEFAULT
Net		NET3	DEFAULT
Bus		A(23)	DEFAULT
Bus		ADDR(10)	DEFAULT

9. Choose *File – Save*.
10. Close the Constraint Manager window.
11. Close the Design Entry HDL window.

For more details, see the *Constraint Manager Reference* guide.

Creating a Net Class in a Hierarchical Block

Task Overview

You will now add a new net class in the hierarchical block, `one`, and then view it in the context of the top-level design, `ps0`.

Steps

1. Change the root design from `ps0` to `one` in the Project Setup dialog of Project Manager.
2. Launch Design Entry HDL.
3. Launch Constraint Manager.
4. In Constraint Manager, select the *Physical* tab.
5. Click *All Layers* under *Net*.
6. Select the `ALS1` and `SIG2` nets.

7. Right-click on the selected nets and choose *Create – Class*.
8. In the Create Net Class dialog box, specify the name of the net class as `NEW_ONE_PHY_CLASS`.
9. Leave the *Create for both physical and spacing* check box selected.
10. Click *OK*.

Objects			Referenced Physical CSet	Line Width	
Type	S	Name		Min	Max
				mil	mil
*	*	*	*	*	*
Dsn		one			
NCls		NEW_ONE_PHY_CL...			
XNet		ALS1			
XNet		SIG2			
Bus	G	NEW_BUS(4)			
Net	G	ASTNET			
Net		DOUT1			
Net		DOUT2			
Net		IO92			
Net		NC97			
Net		ONE			
Net	G	ONE_GLB			
Net		SET2			

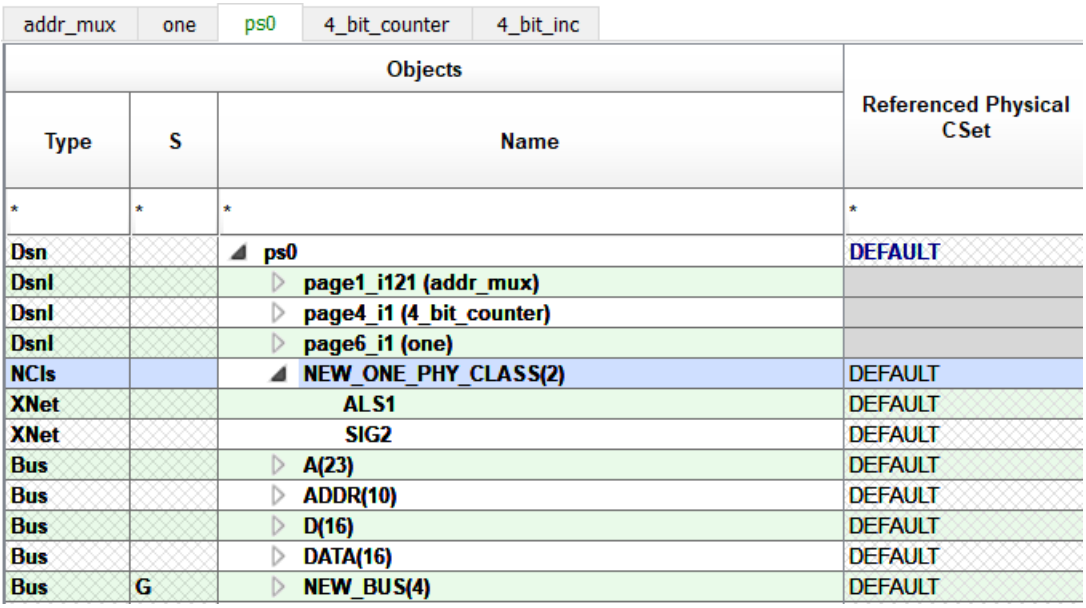
A new net class is created in `one`.

11. Choose *File – Save*.
12. Close the Constraint Manager window.
13. Close the Design Entry HDL window.

Let's now open the top-level design and view the net class.

1. Change the root design from `one` to `ps0` in the Project Setup dialog of Project Manager.
2. Launch Design Entry HDL.
3. Open Constraint Manager.

4. In the Physical tab, click *Net - All Layers*.



   The `NEW_ONE_PHY_CLASS` appears under the top-level design.

5. Close the Constraint Manager window.
6. Close the Design Entry HDL window.

Viewing a Net Class in Constraint Manager Connected to PCB Editor

Task Overview

You will now view a net class created in Constraint Manager connected to Design Entry HDL in Constraint Manager connected to Allegro PCB Editor.

Steps

1. In Project Manager, choose *Tools – Design Sync – Export Physical*.
2. In the *Export Physical* dialog, ensure that the *Update PCB Editor Board (Netrev)* check box is selected.
3. Change the name of the *Output Board File* field to `my_new.brd`.

4. In the *Constraint Manager Data* section, select the *Overwrite current constraints* option.
5. Click *OK*.

   The Progress window appears displaying the progress of the export.
6. Close *No* in the *Design Sync* window that appears prompting you to check the result.

   Note: Warnings may be reported when it prompts you to review the result. For the purpose of this tutorial, you can ignore the warnings.
7. Click *Layout* in Project Manager.

   A message appears saying that license does not include the ability to run the program.
8. Click *OK*.

   Cadence product choices window appears.
9. Select *Allegro PCB Designer* from the *Select a Product* list and click *OK*.

   The Allegro PCB Editor windows appears.
10. Click the Constraint Manager button () to launch Constraint Manager.

    The Constraint Manager window appears.
11. Click the *Physical* tab.
12. Select the *All Layers* worksheet under the *Net* workbook.

    Note that both the net classes created in Constraint Manager connected to Design Entry HDL are visible here.

my_new

Objects			Referenced Physical CSet
Type	S	Name	
*	*	*	*
Dsn		my_new	DEFAULT
NCls		NEW_ONE_PHY_CLASS(2)	DEFAULT
NCls		NEW_PHY_CLASS(2)	DEFAULT
Bus		A(23)	DEFAULT
Bus		ADDR(8)	DEFAULT
Bus		D(16)	DEFAULT

Creating a Net Class-Class in Constraint Manager Connected to PCB Editor

Task Overview

A net class-class lets you define an intra-class spacing relationship among members within a net class, or an inter-class spacing relationship among objects in different net classes. You will create a net class-class in this exercise. You will note that though you can view a net class-class created in Constraint Manager connected to PCB Editor in Constraint Manager connected to Design Entry HDL, you cannot create a net class-class from Design Entry HDL.

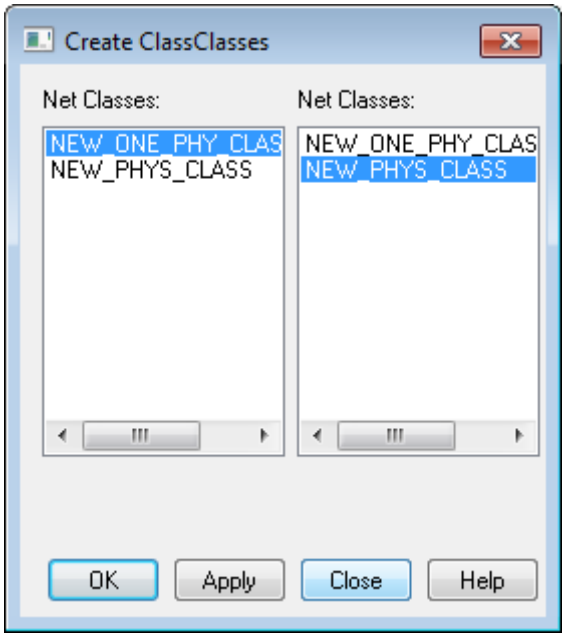
Note: A net class-class applies to the spacing domain.

For more information on the net class-class constraint object, see the Constraints Objects in Hierarchy chapter in *Analysis Modes Constraints Reference guide*.

To create a net class-class constraint object, do the following:

1. In Constraint Manager connected to PCB Editor, select the *Spacing* tab.
2. Select *Net Class-Class – All Layers*.
3. Select the `NEW_PHY_CLASS` class.
4. Do one of the following:
   - Choose *Objects – Create – Class-Class*.
   - Right-click and choose *Create – Class-Class* from the pop-up menu.

5. Specify the class-to-class relationship as shown:



6. Click *OK*.

   Constraint Manager adds a new net class-class, which is indicated by the letters ‘CCIs’ in the *Type* column.

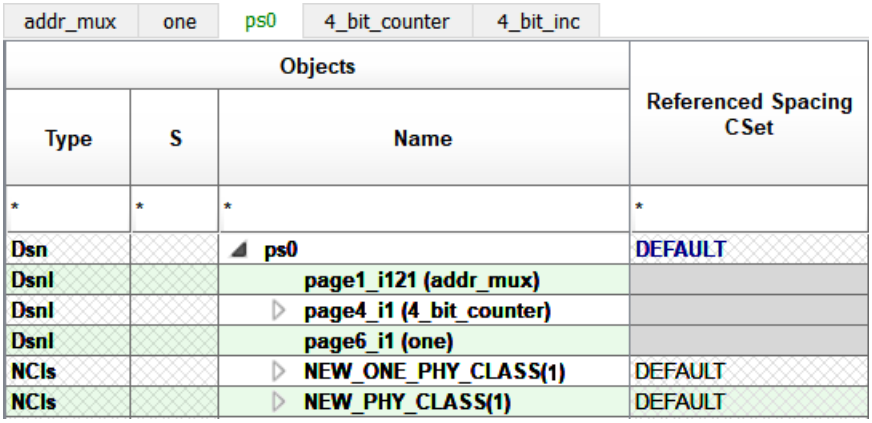
my_new

Objects			Referenced Spacing CSet
Type	S	Name	
*	*	*	*
Dsn		my_new	DEFAULT
NCIs		NEW_ONE_PHY_CLASS(3)	DEFAULT
CCIs		NEW_PHY_CLASS	
NCIs		NEW_PHY_CLASS(1)	DEFAULT
CCIs		NEW_ONE_PHY_CLASS	

7. In PCB Editor, choose *File – Save*.
8. Click *Yes* to overwrite the board file.
9. Choose *File – Exit*.
10. Open Design Entry HDL and choose *File – Import – Import Physical*.

11. Click *OK*.
12. Click *No* when prompted to view the results.
13. Launch Constraint Manager from Design Entry HDL.
14. Click the *Spacing* tab.
15. Click *All Layers* under *Net Class-Class*.

    Note that the net class-class you created is visible in Constraint Manager connected to Design Entry HDL in read-only mode.



What's Next

In the next chapter, Working with Physical and Spacing Constraints, you will learn how to capture and edit physical and spacing constraints in Constraint Manager.

Recommended Reading

For more information about net classes, see the Working with Classes section of the *Allegro Design Entry HDL - Constraint Manager User Guide*.

10

Working with Physical and Spacing Constraints

Objectives

To learn how to work with physical and spacing constraints in Constraint Manager.

At the end of the lesson, you will be able to capture physical and spacing constraints.

Nature of Chapter

Skill (includes concepts and practice)

Estimated Completion Time

20minutes

Overview

Physical and spacing constraints impact the physical layout of a PCB board and are therefore usually captured and modified during the layout design stage by layout engineers. However, stackup information and some physical and spacing constraints are finalized during the design capture stage itself. For example, physical constraints, such as minimum line width and maximum line width, that have an impact on the manufacturing as well as the functioning of the design are finalized during the design capture stage. Such constraints are specified at the design stage and can then be modified while creating the physical layout. Similarly, information such as layers to be used by signal groups and trace proximity, is also decided at the design stage.

Note: It is strongly recommended that you read the *Physical and Spacing Constraints* chapter of the *Allegro Design Entry HDL - Constraint Manager User Guide* before you proceed with this exercise.

Viewing and Capturing Physical/Spacing Constraints

Constraint Manager launched from Design Entry HDL can be used to view, capture, or edit physical and spacing constraints. By default, only those constraints that impact the functioning of the design are displayed in Constraint Manager connected to Design Entry HDL.

Constraint Manager connected to Design Entry HDL allows you to easily capture Physical and Spacing constraints.

Viewing Physical and Spacing Constraints in the Read-Only Mode

Task Overview

Physical and spacing constraints are visible in the read-only mode. In this mode, constraint information is updated only in the back to front flow. You need to add the *EDIT PHYSICAL SPACING CONSTRAINTS* directive to switch to the Edit mode to capture physical and spacing constraints.

Steps

To view physical and spacing constraints in Constraint Manager, do the following:

1. In the Project Manager window, click *Layout* to launch PCB Editor.

   An message is displayed saying that the license you have chosen does not include the ability to run this program.

2. Click *OK*.

   Cadence 23.1 Allegro Product Choices window is displayed.

3. Select *Allegro PCB Designer* and click *OK*.

   Allegro PCB Editor window is displayed.

4. Choose *Setup – Constraints – Spacing*.

   Constraint Manager window is displayed with the Spacing domain open.

5. Select *Net – All Layers.*

6. Double-click on the *Line to* column header to see the Line to Line constraint column.

my_new

Objects			Referenced Spacing CSet	Line To	Thru Pin To	SMD Pin To
Type	S	Name		All	All	All
				mil	mil	mil
*	*	*	*	*	*	*
Dsn		my_new	DEFAULT	5	5	5
NCls		NEW_ONE_PHY_CLASS(3)	DEFAULT	5	5	5
NCls		NEW_PHY_CLASS(1)	DEFAULT	5	5	5
NCls		NEW_PHY_CLASS1(2)	DEFAULT	5	5	5
Bus		A(23)	DEFAULT	5	5	5
Net		A<1>	DEFAULT	5	5	5
Net		A<2>	DEFAULT	5	5	5
Net		A<3>	DEFAULT	5	5	5
Net		A<4>	DEFAULT	5	5	5
Net		A<5>	DEFAULT	5	5	5
Net		A<6>	DEFAULT	5	5	5
Net		A<7>	DEFAULT	5	5	5

7. Change the value of the Line To Line constraint for the net class `NEW_PHY_CLASS` to *25*.

my_new

Objects			Referenced Spacing CSet	All	Line	Thru Pin
Type	S	Name		mil	mil	mil
*	*	*	*	*	*	*
Dsn		my_new	DEFAULT	5	5	5
NCls		NEW_ONE_PHY_CLASS(3)	DEFAULT	5	5	5
NCls		NEW_PHY_CLASS(1)	DEFAULT	5	5	5
NCls		NEW_PHY_CLASS1(2)	DEFAULT	5	25	5
Net		NET1	DEFAULT	5	25	5
Net		NET3	DEFAULT	5	25	5
Bus		A(23)	DEFAULT	5	5	5

8. In PCB Editor, choose *File – Save*.
9. Click *Yes* to overwrite the board file.
10. Choose *File – Exit*.
11. In Project Manager, click *Design Entry*.
12. Choose *File – Import – Import Physical*.
13. Click *OK*.
14. Click *No* to close the *Design Sync* message box.
15. Launch Constraint Manager from Design Enty HDL.

16. Choose *All Layers* under the *Net* folder in the Spacing workbook.

    The updated value of the *Line To Line* constraint for the net class, `NEW_PHY_CLASS`, is propagated to Constraint Manager connected to Design Entry HDL. Note that the stackup information is also available. However, you cannot make any changes to the physical and spacing constraints at this stage.

addr_mux | one | ps0 | 4_bit_counter | 4_bit_inc

Objects			Referenced Spacing CSet	All	Line	Thru Pin
Type	S	Name		mil	mil	mil
FLTR	*	*	*	*	*	*
Dsn		ps0	DEFAULT	5	5	5
NCls		NEW_ONE_PHY_CLASS(3)	DEFAULT	5	5	5
NCls		NEW_PHY_CLASS(1)	DEFAULT	5	5	5
NCls		NEW_PHY_CLASS1(2)	DEFAULT	***	25	5
Net		NET1	DEFAULT	***	25	5
Net		NET3	DEFAULT	***	25	5
Bus		A(23)	DEFAULT	5	5	5
Bus		ADDR(10)	DEFAULT	5	5	5
Bus		D(16)	DEFAULT	5	5	5
Bus		DATA(16)	DEFAULT	5	5	5
Bus	I	I3(8)	DEFAULT	5	5	5

17. Close Constraint Manager.
18. Close the Design Entry HDL window.

Editing Physical and Spacing Constraints in Constraint Manager connected to Design Entry HDL

Task Overview

In order to capture or modify physical and spacing constraints, you need to specify a directive in the CPM file. When you set this directive to ON, the Edit mode for physical and spacing constraints is activated and constraint information is shared in the front-to-back flow as well as in the back-to-front flow.

1. Open *project.cpm* file in a text editor.
2. Add the following directive in the `START_CONSTRAINT_MGR` section:

   ```
   EDIT_PHYSICAL_SPACING_CONSTRAINTS 'ON'
   ```

3. Save the file.
4. In Project Manager, click *Design Entry*.

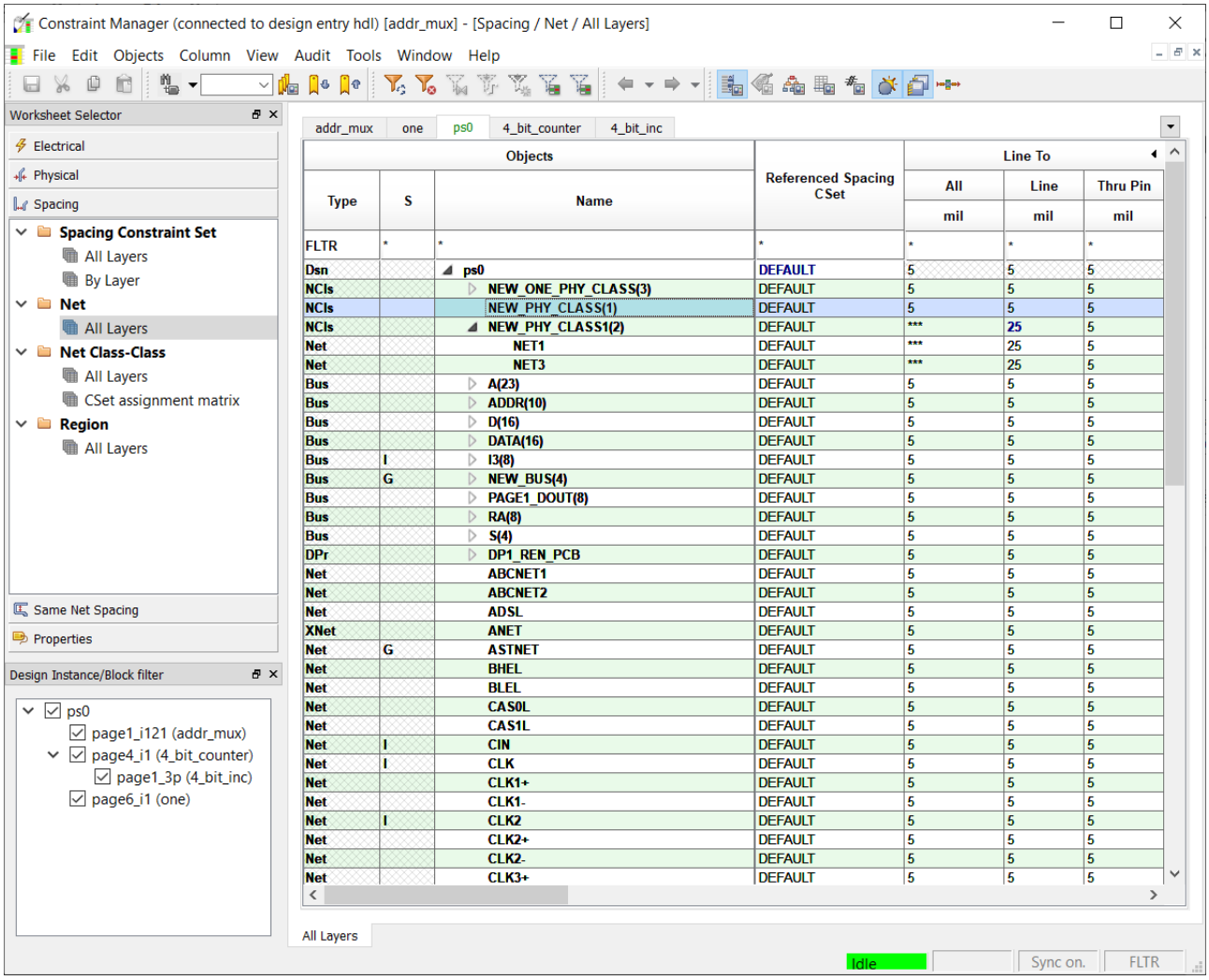
5. In Design Entry HDL, choose *File – Import – Import Physical*.

   Note: Ensure that the *Import changes only* option is selected under *Constraint Manager Data* when you run Import Physical.

6. Click *OK*.

7. Click *No* to close the *Design Sync* message box.

8. Launch Constraint Manager.



Note that the physical and spacing constraints are now editable.

9. Click *All Layers* under *Net Class-Class*

addr_mux | one | ps0 | 4_bit_counter | 4_bit_inc

Objects			Referenced Spacing CSet	Line To	
Type	S	Name		All	Line
				mil	mil
FLTR	*	*	*	*	*
Dsn		ps0	DEFAULT	5	5
NCls		NEW_ONE_PHY_CLASS(3)	DEFAULT	5	5
NCls		NEW_PHY_CLASS(1)	DEFAULT	5	5
NCls		NEW_PHY_CLASS1(2)	DEFAULT	***	25

Note that even the net class-class constraints are editable now.

10. Choose *All Layers* under the *Net* folder in the *Physical* domain.
11. Change the following constraints for the `NEW_PHY_CLASS` class:
    a. Max Line Width to *9*.
    b. Min Neck Width to *2*.
    c. Max Neck Width to *7*.
    d. Min Line Spacing to *3*.

addr_mux | one | ps0 | 4_bit_counter | 4_bit_inc

Objects			Width	Neck		Static Phase Tolerance		
Type	S	Name	Max	Min Width	Max Length		Referenced Intra-DP Spacing CSet	Min Line Spacing
			mil	mil	mil	mil		mil
FLTR	*	*	*	*	*	*	*	*
Dsn		ps0	0	5	0			0
NCls		NEW_ONE_PHY_CLASS(3)	0	5	0			0
NCls		NEW_PHY_CLASS1(2)	9	2	7			3
Net		NET1	9	2	7			3
Net		NET3	9	2	7			3
Bus		A(23)	0	5	0			
Bus		ADDR(10)	0	5	0			

12. Choose *File – Save*.
13. In Design Entry HDL, choose *File – Export – Export Physical*.
14. Click *OK*.
15. Click *No* to close the *Design Sync* message box.
16. In the Project Manager window, click *Layout* to launch PCB Editor.

An message is displayed saying that the license you have chosen does not include the ability to run this program.

17. Click *OK*.

Cadence 23.1 Allegro Product Choices window is displayed.

18. Select *Allegro PCB Designer* and click *OK*.

Allegro PCB Editor window is displayed.

19. Choose *Setup – Constraints – Physical*.

20. Click *All Layers* under the *Net* domain.

my_new

Objects			Width	Neck		Static Phase Tolerance	Dynamic Phase			Differe
Type	S	Name	Max	Min Width	Max Length		Max Length	Tolerance	Referenced Intra-DP Spacing CSet	Min Line Spacing
			mil	mil	mil	mil	mil	mil		mil
*	*	*	*	*	*	*	*	*	*	*
Dsn		my_new	0	5	0					0
NCls		NEW_ONE_PHY_CLASS(3)	0	5	0					0
NCls		NEW_PHY_CLASS1(2)	9	2	7					3
Net		NET1	9	2	7					3
Net		NET3	9	2	7					3
Bus		A(23)	0	5	0					
Net		A<1>	0	5	0					0
Net		A<2>	0	5	0					0

Note that the physical constraints are updated with the changes you made.

21. Close Constraint Manager.

22. In PCB Editor, choose *File – Exit*.

Click *Yes* when prompted to save the changes to the board file.

23. Close the Design Entry HDL window.

24. Close Project Manager.

A

Glossary

Overshoot

Overshoot is the maximum voltage swing above the input voltage. It specifies the acceptable voltage limits of logic families.

Noise Margin

Noise margin is the voltage difference between the maximum voltage dip and the active high threshold or between the maximum voltage dip and the active low threshold.

Jitter

Jitter is the deviation in pulse width of a clock cycle, keeping the clock cycle same.

Sensitive Edge

Sensitive edge signals are those that drive receivers by their edge thresholds. A typical example of a sensitive edge signal is a clock signal.

First Incident Switch

First incident switching is the switching voltage of sufficient amplitude at the initial rise of a signal which is sufficient to drive receivers.

Propagation Delay

Propagation delay is the summation of all calculated transmission line delays along the shortest path between two points. The default unit for propagation delay is ns.

Settle Time

Settle time is the time required for a ringing signal to stabilize to within a specified range of the final value.

Minimum First Switch Time

Specifies the maximum transmission line wire delay plus distortions differing from the nominal driver rise-or-fall time seen in the receiver rise-or-fall.

Duty Cycle

The portion of the time the pulse stimuli is held in the high state as a fraction of the entire pulse period. A value of 0.5 represents equal high and low portions of the cycle period.

Simultaneous Switching Noise

When a number of drivers switch simultaneously in a digital system, a sudden change in current occurs through the power and ground connections to the die. Because of the parasitic inductance that exists in this path, any current change produces a temporary fluctuation in the power and ground voltages as seen by the die. This is typically referred to as Simultaneous Switching Noise (SSN), or Ground Bounce. Simultaneous switching noise can cause noise at the output of non-switching drivers. This noise will then propagate to loads on the net and potentially cause false switching.

Impedance

Impedance is the ratio of input voltage to input current for a transmission line (Z0 = V/I). When a source sends a signal down a line, this is the impedance it must drive. The Source will not see a change in its loading Impedance until 2*TD, where TD is the delay of the line.

Reflection

A reflection on a transmission line is an echo. A portion of the signal power (voltage and current) transmitted down the line goes into the load, and a portion is reflected. Reflections are prevented if the load and the line have the same impedance.

Setup Time

The time for which a digital signal A must be stable and unchanging prior to another digital signal of interest B.

Setup time is most often associated with activity of digital signals immediately before a clock event when these signals must be stable and ready as necessary inputs to clocked circuits, especially latches.

Hold Time

The time for which a digital signal A must be stable and unchanging following the change of another digital signal of interest B.

This parameter is very important with synchronous state machines employing feedback logic that can change as a result of the clock.

Clock Skew

Clock skew is the difference in arrival time between clock and data at a logic gate.

Differential Pair

A differential pair represents a pair of nets or Xnets that will be routed in a way that the signals passing through them are opposite in sign with respect to the same reference. This ensures that any electromagnetic noise in the circuit is cancelled out.

Pin-Pair

A pin-pair represents a pair of logically connected pins, often a driver-receiver connection. Pin-pairs may not be directly connected but they must be on the same net or Xnet. A pin-pair for a net connecting component 1 and component 2 is represented as follows:

```
reference designator of component 1.pin number : reference designator of component
     2.pin number
```

You can specify a pin-pair explicitly, or it can be derived based on the length of the physical net between the pins forming the pin-pair. The length of the net is determined when the board for the schematic is placed and routed in PCB Editor. Accordingly, the pin-pairs are categorized as follows:

- **longest/shortest pin-pair**

Out of all the possible pairs of pins that a net connects, the longest pin-pair is the one between whose pins the length of the connecting net is maximum. Similarly, the shortest pin-pair is the one between whose pins the length of the connecting net is minimum.

- **longest/shortest driver-receiver**

  Out of all the pairs of pins for a net where one pin outputs the signal (driver) on the net and the other takes input (receiver), the longest driver-receiver is the one between whose pins the length of the connecting net is maximum. Similarly, the shortest driver-receiver is the one between whose pins the length of the connecting net is minimum.

- **all driver-receiver pin-pairs**

  This refers to all possible pairs of pins for a net such that one pin outputs the signal (driver) on the net and the other takes input (receiver).

Electrical Constraint Set

An electrical constraint set (ECSet) is a collection of constraints and their default values. An ECSet reflects a particular design requirement. You can capture any or all electrical constraints in an ECSet.

ECSets reside in the Electrical Constraint Set object folder. You can create ECSets for signal integrity, timing, and routing constraints.

Primary Gap

Indicates the ideal edge-to-edge spacing between the pair of nets in the differential pair that should be maintained for the entire length of the pair.

Index

L

M

N

O

P

R

S

V