Product Version 23.1 September 2023 © 2023 Cadence Design Systems, Inc. All rights reserved.

Portions © Apache Software Foundation, Sun Microsystems, Free Software Foundation, Inc., Regents of the University of California, Massachusetts Institute of Technology, University of Florida. Used by permission. Printed in the United States of America.

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

Product PSpice contains technology licensed from, and copyrighted by: Apache Software Foundation, 1901 Munsey Drive Forest Hill, MD 21050, USA © 2000-2005, Apache Software Foundation. Sun Microsystems, 4150 Network Circle, Santa Clara, CA 95054 USA © 1994-2007, Sun Microsystems, Inc. Free Software Foundation, 59 Temple Place, Suite 330, Boston, MA 02111-1307 USA © 1989, 1991, Free Software Foundation, Inc. Regents of the University of California, Sun Microsystems, Inc., Scriptics Corporation, © 2001, Regents of the University of California. Daniel Stenberg, © 1996 - 2006, Daniel Stenberg. UMFPACK © 2005, Timothy A. Davis, University of Florida, (davis@cise.ulf.edu). Ken Martin, Will Schroeder, Bill Lorensen © 1993-2002, Ken Martin, Will Schroeder, Bill Lorensen. Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, Massachusetts, USA © 2003, the Board of Trustees of Massachusetts Institute of Technology. vtkQt, © 2000-2005, Matthias Koenig. All rights reserved.

Trademarks: Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522. Open SystemC, Open SystemC Initiative, OSCI, SystemC, and SystemC Initiative are trademarks or registered trademarks of Open SystemC Initiative, Inc. in the United States and other countries and are used with permission.

All other trademarks are the property of their respective holders.

Restricted Permission: This publication is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this publication, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this publication subject to the following conditions:

- 1. The publication may be used only in accordance with a written agreement between Cadence and its customer.
- 2. The publication may not be modified in any way.
- 3. Any authorized copy of the publication or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
- 4. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

Disclaimer: Information in this publication is subject to change without notice and does not represent a commitment on the part of Cadence. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information. Cadence is committed to using respectful language in our code and communications. We are also active in the removal and/or replacement of inappropriate language from existing content. This product documentation may however contain material that is no longer considered appropriate but still reflects long-standing industry terminology. Such content will be addressed at a time when the related software can be updated without end-user impact.

Restricted Rights: Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227-14 and DFAR252.227-7013 et seg. or its successor.

Contents

Knowr	n Problems and Solutions in PSpice	5
	CCMPR02146101: Default font size in the Model Text window is very large	5
	CCR 1534735: Mathworks Matlab crashes randomly in the PSpice-SLPS flow	5
	CCR 19462: Cannot use relative tolerances on parameters used for DEV	
		6
	CCR 22481: Part names with spaces in the name result in	_
	"Error in Open Alias" when simulating	
	CCR 32270: Model reads information from another model with the same name and	
		6
	CCR 152246: Error in displaying plot, if the simulation profile name includes any special character.	7
Know	n Problems and Solutions in Capture-PSpice Flow	•
IXIIOWI	CCR 332772: Issue with the Markers flow in hierarchical designs in OrCAD Capture	
	8	
Knowi	n Problems and Solutions in Design Entry HDL-PSpice Flow	9
	CCR 892748: Simulation failure because sub-parameters are not passed if	
	·	9
	CCR 243620: Bias display settings from previous releases are not available in the	
	SPB 15.5.1 release	9
	CCR 270644: PSpice name does not appear for listed parts in the View Probe dialog	_
		9
	CCR 273518: AA Models to be supported for model association	0
	CCR 107997: Inconsistency between toolbar settings and the bias point values	_
	displayed on the schematic	
	CCR 94690: Issue in the bias display with hierarchical designs.	
	CCR 13789: Default values and sign mismatch between Input and Output load current values in PSpice library parts	<u>nt</u> 0
	•	
	CCR 8522: K and ABM parts do not have the REFDES property	
	CCR 8624: PSpice netlisting fails if @ <variable> used in parameter values 1</variable>	1
	CCR 13996: SUBPARAM part does not support passing parameters to subcircuits 12	
	CCR 8524: DE-HDL does not delete probes placed on a deleted node or part 1	2
		2
	^^# DEGN ONGUE IO HOURS HE SHIDIGION DIONE NAME	_

CCR 14022: PSpice does not display trace for a probe placed on a bus in Concept
<u>HDL</u> 12
CCR 19131: Coax models in the TLINE library do not netlist from DE-HDL 13
CCR 23415: Unable to view PSpice netlist from DE-HDL
CCR 32518: Smoke Analysis: Need to change device name in <design_name>.prp file</design_name>
to match part name if you edit smoke information in parts with multiple implementation
properties

This Known Problems and Solutions document describes important Cadence Change Requests (CCRs) for PSpice and PSpice Simulator¹ and tells you how to solve or work around these problems. For information about CCRs that are fixed for this release, see PSpice Product Notes.

Important: Only known problems and solutions application at the time of this release are listed in this document.

Known Problems and Solutions in PSpice

This section lists the known problems in PSpice and tells you how to solve or work around these problems.

CCMPR02146101: Default font size in the Model Text window is very large

Description: In Model Editor, the default font size of the model definition displayed in the Model Text window is very large.

Solution: Use CTRL+ mouse scroll to zoom out or zoom in the text size.

CCR 1534735: Mathworks Matlab crashes randomly in the PSpice-SLPS flow

Description: When you run a design in the PSpice-SLPS flow, Mathworks[©] Matlab may crash without any error message.

Solution: Ensure that the Matlab's current working directory has all the PSpice-SLPS flow designs.

Depending on the license and installation, either PSpice or PSpice Simulator is installed.

PSpice Known Problems and Solutions

CCR 19462: Cannot use relative tolerances on parameters used for DEV in Monte Carlo analysis

Description: When running a Monte Carlo (.MC) analysis, a DEV tolerance that is a parameter (for example, DEV={ATOL}) will work only if it is an absolute tolerance.

Solution: If using Capture, Design Entry HDL, or Schematics for design entry, you can create an expression for DEV that multiplies that value by the relative tolerance divided by 100. For example, given a relative tolerance RTOL%, if the property being toleranced is VALUE, set DEV={VALUE*RTOL/100}.

CCR 22481: Part names with spaces in the name result in "Error in Open Alias" when simulating

Description: If a part reference contains a space (e.g., MY PART), then the simulation fails to run. The PSpice window shows the error: "Error in Open Alias."

Solution: Use an underscore (_) instead of a space in the part reference.

CCR 32270: Model reads information from another model with the same name and having the _<integer> suffix

Description: If there are two models, say UA741 and UA741_2, the model UA741 might read simulation and smoke information from the model UA741_2. This results in Model Editor displaying the wrong simulation and smoke information for the UA741 model, and in incorrect simulation results when you run the simulation in PSpice and Advanced Analysis.

Solution:

- Ensure that you do not create a model with a _<integer> suffix in its name when another model with the same name exists. For example, if a model with the name UA741 exists, do not create another model with the name UA741_1, UA741_2, and so on.
- Make sure that you do not create a model with the same name when another model with the same name and a _<integer> suffix exists. For example, do not create a model with the name UA741 when another model with the name UA741_1, UA741_2, and so on exists.

Note: The _<integer> suffix is reserved for level support in OPAMP model creation.

PSpice Known Problems and Solutions

CCR 152246: Error in displaying plot, if the simulation profile name includes any special character.

Description: If the simulation profile name includes a special character, an error is encountered while displaying plot. For example, if the simulation profile name is trans`.sim and you are trying to plot measurement vs. measurement, the following error message appears:

"One or more required header items are missing from csdf file. Error trying reading data file. The data file is empty. Analysis failed."

Solution: Avoid special characters in the simulation profile, design, and schematic names.

PSpice Known Problems and Solutions

Known Problems and Solutions in Capture-PSpice Flow

This section lists important Cadence Change Requests (CCRs) when using Capture with PSpice and tells you how to solve or work around these problems.

CCR 332772: Issue with the Markers flow in hierarchical designs in OrCAD Capture

Description: When you have two or more current markers in a design and delete the markers from the Probe window, you can enable only one marker in OrCAD Capture.

Solution:

To solve the issue, do the following:

- 1. In CAPTURE, choose *PSpice Markers List.* De-select and then select the markers to enable all the markers.
- 2. Select any one of the markers and rotate it. Now you are able to select the other marker as well.
- 3. Select markers on one of the descend down schematic page to enable markers on this page, close down the other schematic, and reopen it. You are able to place all markers on it.

PSpice Known Problems and Solutions

Known Problems and Solutions in Design Entry HDL- PSpice Flow

This section lists the important Cadence Change Requests (CCRs) when using Design Entry HDL with PSpice and tells you how to solve or work around these problems.

CCR 892748: Simulation failure because sub-parameters are not passed if Verilog Decs is used

Description: If Verilog_Decs is used to pass parameters to lower-level blocks in a hierarchical design, the parameters are not initialized in the subcircuit when you create a netlist. As a result, simulation fails.

Solution: Use VHDL_Decs to pass parameters to lower-level blocks.

CCR 243620: Bias display settings from previous releases are not available in the SPB 15.5.1 release

Description: If you open a DE-HDL design that was created in a previous release and saved with bias display options turned on, in the SPB 15.5.1 release, you will find that the bias display settings are either turned off or are grayed out.

Solution: Reconfigure the bias display settings. From the *PSpice Simulator* menu in Design Entry HDL, choose *Bias Display*. Select the appropriate submenu to configure the desired bias display settings. Save the updated design. Saving the design ensures that the bias display settings are saved in the project file for future use.

CCR 270644: PSpice name does not appear for listed parts in the View Probe dialog

Description: If you attach PSpice probe symbols to the ground symbol from the pspice_elem library or the ground (0) symbol from the Source library, the PSpice names for the parts will not be visible in the View Probes dialog. Only the Design Entry HDL names are displayed.

Solution: None

PSpice Known Problems and Solutions

CCR 273518: AA Models to be supported for model association.

Description: In the SPB 15.51 release, you cannot use the Model Import Wizard, launched using the Associate Model command from the PSpice Simulator menu, to associate parametrized PSpice models to a part in DE-HDL.

Solution: None

CCR 107997: Inconsistency between toolbar settings and the bias point values displayed on the schematic

Description: At times when you open a previously saved design in DE-HDL, there might be an inconsistency in the bias point values displayed and the status of the toolbar buttons used to enable the display of bias point values. For example, it may so happen that the bias voltages are displayed even if the toolbar button for enabling the display of bias point voltages is not selected. Or, bias point values might not be displayed even if the toolbar buttons are selected. This happens because displayed bias point values are saved as a part of the design whereas toolbar settings are global and do not change when you close a design and open another.

Solution: First de-select all the tool buttons used to enable the display of bias point values, and then select the required toolbar buttons again.

CCR 94690: Issue in the bias display with hierarchical designs.

Description: In hierarchical designs with reusable blocks, the bias point voltage is not displayed.

Solution: To view the bias point voltages in a hierarchical design with reusable blocks, select the net for which you want to view the bias point voltage and display the Attributes dialog box. The bias point voltage will be displayed as the value of the \$BIASVOLTAGE property in the Attributes dialog box.

CCR 13789: Default values and sign mismatch between Input and Output load current values in PSpice library parts

Description: The chips.prt files for all PSpice library parts have the following problem:

- The INPUT_LOAD and OUTPUT_LOAD values have the same sign.
- Default values have been assigned for INPUT_LOAD and OUTPUT_LOAD.

PSpice Known Problems and Solutions

This results in errors if, in a design, Electrical Rule Checks are run to check loading violations for interface signals (which are digital in nature).

Solution: Edit the chips.prt file for such parts as illustrated in the following example:

```
pin
'A':
    INPUT_LOAD='(-0.010000,0.010000)';
    PIN_NUMBER='(1,3,5,9,11,13)';
'-Y':
    OUTPUT_LOAD='(-1.000000,1.000000)';
    PIN_NUMBER='(2,4,6,8,10,12)';
end pin;
```

In this example OUTPUT_LOAD value has to be changed to '(1.000000, -1.000000)' to represent the sink current as +ve and source current as -ve.

Also note that default values have been assigned to INPUT_LOAD and OUTPUT_LOAD. Refer to the data sheet for the part and assign correct values for INPUT_LOAD and OUTPUT_LOAD.

CCR 8522: K and ABM parts do not have the REFDES property

Description: The K parts (for example, k502t300_3e2a) in the MAGNETIC part library and all parts in the ABM library do not have the REFDES property.

Solution: Add the REFDES property to these parts as described in the "Coupling of Inductors using REFDES property" section in PSpice User Guide.

CCR 8624: PSpice netlisting fails if @<variable> used in parameter values

Description: If a parameter value has a variable name starting with @, PSpice netlisting fails. For example, if a resistor placed on a design has the value {@rval} or @rval, PSpice netlisting fails.

Solution: Do not use a parameter value with the variable name starting with @.

PSpice Known Problems and Solutions

CCR 13996: SUBPARAM part does not support passing parameters to subcircuits

Description: The SUBPARAM part in the SPECIAL library does not support passing parameters to subcircuits.

Solution: Use the VHDL_DECS part in the STANDARD library to pass parameters to subcircuits. For more information, see the "*Passing parameters to subcircuits*" section of *PSpice User's Guide*.

CCR 8524: DE-HDL does not delete probes placed on a deleted node or part

Description: In DE-HDL, place a probe on a node or part. Now delete the node or part. In the Probes dialog box you will see that the corresponding probe for the deleted node or part is not deleted.

Solution: Open the Probes dialog box and manually delete the probes.

CCR 13480: Unable to modify the simulation profile name

Description:

- 1. From the PSpice menu in DE-HDL, choose *Edit Simulation Profile*.
- 2. Click on the General tab in the Simulation Settings dialog box.
- **3.** Change the name of the simulation profile in the Profile name field, and click OK.

The name of the simulation profile does not change in the PSpice toolbar.

Solution: None

CCR 14022: PSpice does not display trace for a probe placed on a bus in Concept HDL

Description: In DE-HDL, place a probe on a bus, say, DATA<3..0>. When you simulate the design, the trace for the probe placed on the bus is not displayed in PSpice Probe.

Solution: Do the following:

1. From PSpice Trace menu, choose *Add Trace*.

PSpice Known Problems and Solutions

The Add Traces dialog box appears.

- **2.** From the Functions and Macros list, select Digital Operators and Functions.
- **3.** Click the { } entry.
- **4.** In the Simulation Output Variables list, click the digital signals for the bus in the sequence you want.

Note: For a DATA bus <3..0>, the signals displayed in the Simulation Output Variables list will be DATA_OP_3_CP_, DATA_OP_2_CP_, DATA_OP_1_CP_, and DATA_OP_0_CP_.

CCR 19131: Coax models in the TLINE library do not netlist from DE-HDL

Description: An attempt to generate a DE-HDL netlist for a coax model in the TLINE library fails with "ERROR: Invalid device type specified in PSpiceTemplate." This happens because the first character in the PSpiceTemplate is not recognized by the DE-HDL-PSpice netlister.

Solution: There are two different models that can be selected by the coax symbols:

1. A lossy tline .MODEL statement (T statement) that models frequency-dependent loss. Modify the PSpiceTemplate as illustrated:

```
T^@REFDES %A+ %A- %B+ %B-@MODEL ?LEN/LEN=@LEN/
```

2. A .SUBCKT statement (X statement) that models fixed-frequency loss. Modify the PSpiceTemplate as illustrated:

X^@REFDES %A+ %A- %B+ %B- @MODEL ?FRQ/PARAMS: FRQ=@FRQ/ ?LEN/LEN=@LEN/

CCR 23415: Unable to view PSpice netlist from DE-HDL

Description: When you choose *View Netlist* from the PSpice menu in DE-HDL, the following error message is displayed and you are unable to view the PSpice netlist:

No error message for error code = 3

Solution: This error message appears because write.exe (the executable for WordPad) could not be located in the system path. Ensure that write.exe is in the system path.

Product Version 23.1

All Rights Reserved.

PSpice Known Problems and Solutions

CCR 32518: Smoke Analysis: Need to change device name in design_name.prp file to match part name if you edit smoke information in parts with multiple implementation properties

Scenario1: Model with multiple implementation properties

Description: If you edit the model for a part (with multiple implementation properties) placed in your design and change its smoke parameters, you must change the device name in the <design_name>.prp file to match the name of the part.

To change the device name in the $< design_name > . prp$ file, do the following:

- **1.** From the Text menu in DE-HDL, choose *Attributes*.
- **2.** Click the part whose smoke information you edited.

The Attributes dialog box appears.

- **3.** Note the value of the IMPLEMENTATION property.
- 4. Click OK to close the Attributes dialog box.
- **5.** Open the <design_name>.prp file located in the project directory in a text editor.
- **6.** Use the Find command in the text editor to find the device name that is the same as the value of the IMPLEMENTATION property on the part.
- 7. Change the device name to match the name of the part.
- **8.** Save the changes in the text editor.

Note: If the device name in the $< design_name>.prp$ file is not the same as the name of the part, the modified smoke information will not be used for smoke analysis. Instead, the smoke information from the part library will be used for smoke analysis.

Scenario2: Model with multiple-level support

Description: If you edit the model for a part (with level support) placed in your design and change its smoke parameters, you must change the device name in the <design_name>.prp file to awb<part_name>.

For example, suppose you edited the smoke information of the AD101A part in the OPA library and that part has the LEVEL property set to 3. The device name in the <design_name>.prp file will be written as AWBAD101A_3 (where 3 is the value of the LEVEL property on the part). You must change the device name in the <design_name>.prp file to AWBAD101A.

PSpice Known Problems and Solutions

Note: If you do not change the device name in the <design_name>.prp file as described above, the modified smoke information will not be used for smoke analysis. Instead, the smoke information from the part library will be used for smoke analysis.