

System Connectivity Manager User Guide

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System Connectivity Manager User Guide

Preface

About This User Guide

System Connectivity Manager User Guide explains how to use the System Connectivity Manager design capture environment.

System Connectivity Manager is available with following licenses.

- Allegro Design Authoring
- Cadence SiP Digital Architect GXL
- Cadence SiP Digital Architect XL

SiP Digital Architect license provides support for the co-design using SCM.

Audience

This user guide assumes that you are familiar with the development and design of electronic circuits at the system or board level. This user guide also assumes a working knowledge of the following Cadence tools:

- Allegro Design Entry HDL
- Allegro Constraint Manager
- Cadence SiP Layout
- Allegro PCB Editor
- Allegro SigXplorer

Finding Information in This User Guide

This user guide covers the following chapters:

See...	For Information About...
<u>Chapter 1, “System Connectivity Manager: Introduction”</u>	Introduces System Connectivity Manager and describes the important features of System Connectivity Manager. The co-design concept, how it is supported in SCM, and the problems that can be addressed by using co-design concept have also been touched upon in this chapter.
<u>Chapter 2, “Getting Started with System Connectivity Manager”</u>	Describes the System Connectivity Manager user interface and how to perform basic tasks like starting System Connectivity Manager, creating and opening projects and so on.
<u>Chapter 3, “Project Creation and Setup”</u>	Describes how to create and setup design projects.
<u>Chapter 4, “Working with Components”</u>	Describes how common design tasks, such as adding a component, modifying instance name and reference designators, are performed in System Connectivity Manager.
<u>Chapter 5, “Working with Signals”</u>	Describes how to perform common tasks related to design nets, such as adding a signal, aliasing nets, renaming a signal and so on.
<u>Chapter 6, “Capturing Connectivity”</u>	Describes how to use the spreadsheet based interface of System Connectivity Manager to capture connectivity in your design.
<u>Chapter 7, “Working with Differential Pairs”</u>	Describes how differential pairs are supported in System Connectivity Manager.

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See...

For Information About...

[Chapter 8, “Navigating the Design and Viewing Files”](#)

Describes how to use the Hierarchy Viewer and Signal Navigate windows in System Connectivity Manager to navigate the design, and how to view the files related to the design in the File Viewer in System Connectivity Manager.

[Chapter 9, “Using the Physical View”](#)

Describes how to use the Physical View in System Connectivity Manager.

The Physical View in System Connectivity Manager provides a physical netlist view of the design as it appears in your board layout.

[Chapter 10, “Working with Properties and Electrical Constraints”](#)

Describes how to work with properties using the Properties window in System Connectivity Manager and using the property worksheets in Allegro Constraint Manager.

This chapter also describes how to work with electrical constraints in your design using Allegro Constraint Manager.

[Chapter 11, “Working with Associated Components”](#)

Describes how to work with terminations, bypass capacitors and pull-ups/pull-downs in your design.

[Chapter 12, “Working with Signal Integrity Models”](#)

Describes how to assign signal integrity (SI) models to components and pins in your design.

You need to assign SI models before you can use SigXplorer to perform topology exploration and analyze the nets in your design for signal integrity issues.

[Chapter 13, “Working with Hierarchical Designs”](#)

Describes the procedures for working with blocks to create hierarchical designs in System Connectivity Manager.

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Preface

See...	For Information About...
<u>Chapter 14, “Netlisting the Design for Simulation.”</u>	Describes how to generate structural Verilog netlists for all the blocks in the design. You can then use the Verilog netlist to simulate the design using the Cadence Verilog XL and NC Verilog simulators, or third-party Verilog simulators.
<u>Chapter 15, “Team Design”</u>	Describes how you can use System Connectivity Manager to create hierarchical designs in a team design environment, in which a team of designers work on a design.
<u>Chapter 16, “Designing System-in-Package”</u>	Describes how you can use System Connectivity Manager for SiP design tasks.
<u>Chapter 17, “Design Reuse”</u>	Describes the process of creating standalone reusable physical blocks and using them in different designs.
<u>Chapter 18, “Transferring the Logical Design to a Board and Design Synchronization”</u>	Describes the tasks you need to perform to transfer the logical design in System Connectivity Manager to the Allegro PCB board for physical layout and keep the design in System Connectivity Manager and the board in synch.
<u>Chapter 19, “Running Design Rule Checks”</u>	Describes how to run design rule checks (DRCs) to identify connectivity and other errors in the design.
<u>Chapter 20, “Creating Reports”</u>	Describes how to design report templates and then use the templates to generate reports for designs.
<u>Chapter 21, “Generating Document Schematic for a Design”</u>	Describes how to generate a schematic of the design for documentation purposes.
<u>Chapter 22, “Exporting Schematics for a Design.”</u>	Describes how to export a design as a schematic.
<u>Chapter 23, “Creating Parts from External Data Files”</u>	Describes how you can create parts from .csv files and place-and-route data for FPGAs, and add the parts in your design.
<u>Chapter 24, “Archiving Projects”</u>	Describes how to archive your project.

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Preface

See...	For Information About...
Chapter 25, “Customizing System Connectivity Manager”	Describes how you can customize the menus, toolbars and the spreadsheet editor in System Connectivity Manager.
Appendix A, “Dialog Box Descriptions”	Describes the dialog boxes in System Connectivity Manager.

Related Documentation

You can also refer the following documentation to know more about related tools and methodologies:

If you want to know...	Read
How to get quickly started with System Connectivity Manager	System Connectivity Manager Tutorial
How to use Design Entry HDL to enter schematics	Allegro Design Entry HDL User Guide
More about Allegro Design Entry HDL digital libraries	Allegro Design Entry HDL Libraries Reference
More about how to use Allegro Constraint Manager to manage electrical constraint information in your design	Allegro Constraint Manager User Guide Allegro Constraint Manager Reference
More about properties supported by Cadence PCB design software	Allegro Platform Properties Reference
More about how to create and use physical layouts	Allegro PCB Editor documentation

If you want to know... Read

More about using
SigXplorer to analyze
the high speed nets in
your design for signal
integrity issues and
create a set of
constraints for the nets.

[Allegro PCB SI SigXplorer User Guide](#)

Typographic and Syntax Conventions

This list describes the syntax conventions used for this user guide:

literal	Nonitalic words indicate keywords that you must enter literally. These keywords represent command (function, routine) or option names.
<i>argument</i>	Words in italics indicate user-defined arguments for which you must substitute a name or a value.
	Vertical bars (OR-bars) separate possible choices for a single argument. They take precedence over any other character.
[]	Brackets denote optional arguments. When used with OR-bars, they enclose a list of choices. You can choose one argument from the list.
{ }	Braces are used with OR-bars and enclose a list of choices. You must choose one argument from the list.

System Connectivity Manager: Introduction

In today's board-level digital designs historical schematic capture techniques are not as efficient as they once were. The designs today are increasing in complexity, but decreasing in the number of components on the board. To reduce the number of components on a board, large pin-count devices are being used extensively. As these large pin-count devices cannot be placed on a single schematic page, designers spend great amounts of time to split these devices into multiple symbols based on functionality and place each symbol on separate schematic pages. A natural effect of this is the increased complexity of the logical interconnect on the PCB.

Most of the schematics today that represent these complex designs do not have room to draw connecting wire segments between logical pins so the design is entirely connect-by-name. This coupled with the fact that very few of the symbol's graphics indicate any logical meaning makes today's designs very ineffective in documenting the design intent. It is clear that designs dominated by large pin-count devices require a more efficient way of capturing the interconnect.

System Connectivity Manager is the next generation PCB design capture tool that helps you tackle your PCB design capture challenges.

What is System Connectivity Manager?

System Connectivity Manager is a new design capture environment that provides logic designers the flexibility of capturing their designs in multiple ways. While Allegro Design Entry HDL offered schematic based design capture environment, System Connectivity Manager allows you to capture your design using spreadsheets, schematic and Verilog HDL.

The spreadsheet-based design capture environment in System Connectivity Manager allows you to quickly capture connectivity information in the design. Spreadsheet-based design is very effective for capturing designs with large pin count components and backplanes.

Designing Systems Using System Connectivity Manager

Besides providing users with multiple ways of capturing their designs, SCM can also be described as the tool that captures and maintains the association of the implemented functions and the communication interfaces between these functions. While working with SCM, a system is defined as a set of functions, which when put together perform a particular task. These functions communicate with each-other through a set of interfaces that are implemented as wires carrying signals from one function to another.

The ability of SCM to manage communication interfaces between these functions makes it a useful tool to implement partitioning of system design. Defining system partitions is one of the primary tasks in the system design cycle. Partitioning consists of dividing a system into different functional groups and then targeting an implementation for each group. This is important design task because partitioning of the system hardware or software directly impacts the cost of the system. After the system is partitioned into groups, sub-systems or components, the physical implementation of the system in each partition is finalized. Each partition or group can map to a separate physical implementation. The possible physical implementation could be ASICs, FPGAs, custom ICs, or even off-the-shelf components.

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System Connectivity Manager: Introduction

The partitioning process and its results on a system design are shown in [Figure 1-1](#) on page 35.

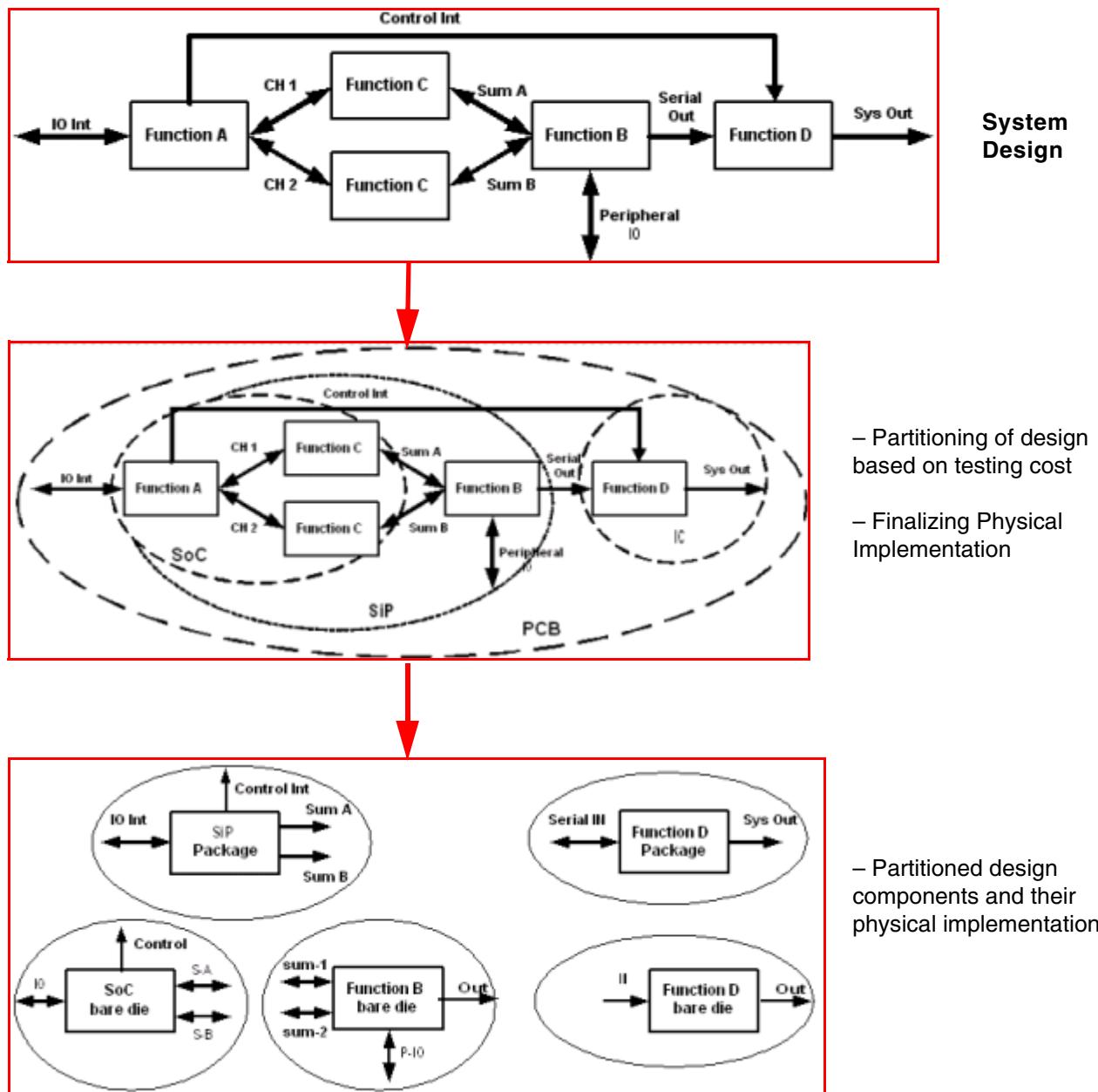


Figure 1-1 Partitioning System Design

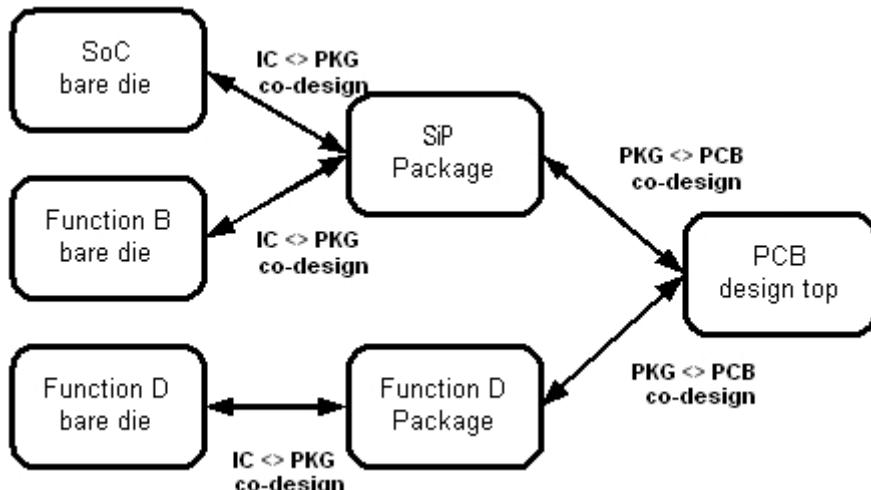
Co-Design Objects in SCM

After you have partitioned your system, depending on the physical implementation, it may happen that one or more functional groups have to be designed in one fabric and implemented in another. As shown in [Figure 1-1](#) on page 35, Function D is to be designed as a bare die and packaged before it is instantiated on a PCB. The functionality of the Function D will be implemented during the bare die design, whereas the interface information required to integrate this die with the rest of the system is taken care during package design.

To implement such real-life scenarios in the design cycle, SCM provides support for co-design objects. Co-design objects are objects that are designed in one fabric and implemented in another.

Using co-design objects in SCM allows you to concurrently modify different aspects of the object in separate implementation fabrics and synchronize the information as and when required. the logical design and the connectivity of a co-design block is captured in SCM where as the physical implementation of the co-design object is designed simultaneously in SiP Layout or PCB Editor. For example, a package whose pin number to signal assignments are defined during PCB design and also during the package design, is a co-design object.

The figure below shows the implementation of the system shown in [Figure 1-1](#) on page 35, in terms of co-design objects. The bare die for Function D can be implemented as a co-design IC in the IC design tool. The package for this die can again be implemented as a co-design object in Cadence IO Planner.



To know more about designing System-in-Package using System Connectivity Manager, see [Chapter 16, “Designing System-in-Package.”](#)

Advantages of Using Co-Design Objects

Concurrent designing, implemented in SCM using co-design objects, has many advantages over traditional design methodology, which uses a sequential approach.

- Using co-design methodology to design your system allows you to work in a distributed design environment across domains and across technologies.
- Using co-design objects enhances productivity and leads to better designs. This is because different teams can simultaneously work on their modules and common information is synced from time to time. For example, by using a co-design die, you can test your logical design by simulating the signals even if the physical implementation is not known.
- While specifying the connectivity between the logical and the physical implementations of a co-design object, you can introduce new signals, such as power and ground signals that are must for the physical implementation, but do not have a major impact on the logical design.
- In SCM, co-design objects are modeled in such a way that the physical and logical implementation of co-design blocks is separate. This feature allows you to map one logical signal to multiple physical pins.
- As interface information about a component is available early in the cycle, iterations related to component placement and orientation on a PCB can be completed early in the cycle. This shortens the development life cycle.
- SCM provides support for synchronizing design differences any time during the design cycle.
- Early interaction between the teams sharing the data, minimizes the possibility of redesigning the system towards the end of the design cycle. This shortens the development life cycle and reduces the cost. The time-to-market is also reduced.

System Connectivity Manager Features

Besides providing support for the co-design objects and spreadsheet editor, there are various other features in SCM that can be used to capture the connectivity of a complex and huge system in a fast and simple manner. Using SCM, logic designers have the flexibility of capturing their designs in multiple ways. Unlike schematic-based design capture environment, SCM allows you to capture your design using spreadsheets, schematic and Verilog HDL.

- The spreadsheet-based design capture environment in System Connectivity Manager allows you to quickly capture connectivity information in the design. Spreadsheet-based

System Connectivity Manager User Guide

System Connectivity Manager: Introduction

design is very effective for capturing designs with large pin count components and backplanes.

- System Connectivity Manager also provides a Verilog design environment that integrates the power of spreadsheets with a language sensitive Verilog editor to enable you to quickly capture your design in Verilog HDL.

You can also import existing Verilog files into your design. When you import a Verilog file, SCM parses the file for errors and creates blocks for the modules in the Verilog file. You can then add the blocks in your design edit them using the Verilog Design Editor.

Besides the capability to capture designs using spreadsheets, schematics and Verilog HDL, System Connectivity Manager has the following features:

- Intuitive User Interface
- Capturing Connectivity
- Easy Property and Electrical Constraint Management
- Online Packaging
- Easy Management of Associated Components
- Support for Assigning Signal Integrity Models
- Easier Management of Hierarchical Designs
- Support for Functional Verification of the Design
- Support for Generating Reports
- Support for Generating Schematics for Documentation Purposes
- Design Debugging with Design Rule Checks (DRCs) and the Physical View

Intuitive User Interface

System Connectivity Manager provides a highly customizable and intuitive user interface with features like multi-select connectivity, drag-drop, copy/paste, multiple undo-redo, error highlighting, find/replace, global find/replace and design comments.

For a detailed description of the System Connectivity Manager user interface, see [Chapter 2, “Getting Started with System Connectivity Manager.”](#)

Spreadsheet-based Design Capture

The spreadsheet-based design capture environment in System Connectivity Manager allows you to quickly capture connectivity information in the design.

For more information on using the spreadsheet-based design capture environment in System Connectivity Manager, see [Chapter 6, “Capturing Connectivity.”](#)

Easy Property and Electrical Constraint Management

System Connectivity Manager lets you use the Constraint Manager tool to capture and manage property and electrical constraint information across your design. Constraint Manager provides a spreadsheet interface that helps you to quickly work with properties and electrical constraints across your design.

You can also use the *Properties* window in System Connectivity Manager to work with properties on individual components, nets and pins in your design.

For more information on working with properties and electrical constraints, see [Chapter 10, “Working with Properties and Electrical Constraints.”](#)

Online Packaging

Unlike Allegro Design Entry HDL where you have to package a saved design to assign reference designators, physical net names and packages, System Connectivity Manager performs online packaging to automatically assign reference designators, physical net names and packages.

Easy Management of Associated Components

Today’s designs have a large number of discrete components such as terminations, bypass capacitors and pullup/pulldowns connected to components in the design.

System Connectivity Manager allows you to quickly add these discrete components in the design. System Connectivity Manager preserves the association between these discrete components and the component to which they are connected. If you move or delete the component to which these discrete components are connected, the associated discrete components are also moved or deleted. This makes it easy to manage associated components in the design.

For more information, see [Chapter 11, “Working with Associated Components.”](#)

Support for Assigning Signal Integrity Models

System Connectivity Manager lets you assign signal integrity (SI) models to components and pins in your design during the design capture phase. You can then use SigXplorer to perform topology exploration and analyze the nets in your design for signal integrity issues. This helps you correct signal integrity issues early in the design cycle.

For more information, see [Chapter 12, “Working with Signal Integrity Models.”](#)

Easier Management of Hierarchical Designs

System Connectivity Manager lets you quickly create and manage hierarchical designs using top-down and bottom-up design methodologies. You can have a combination of spreadsheet, Verilog and schematic blocks in your hierarchical design.

For more information on working with hierarchical designs, see [Chapter 13, “Working with Hierarchical Designs.”](#)

Support for Functional Verification of the Design

System Connectivity Manager provides support for generating verilog netlist of your design. You can perform the functional verification of your design by simulating the generated netlist in any verilog simulator.

For more information on how to generate the simulation netlist for your design, see [Chapter 14, “Netlisting the Design for Simulation.”](#)

Support for Generating Reports

System Connectivity Manager provides powerful report design and generation features. You can design report templates and then use the templates to generate reports for any design.

For more information, see [Chapter 20, “Creating Reports.”](#)

Support for Generating Schematics for Documentation Purposes

If you captured your design using spreadsheets or Verilog HDL, you might want to generate a schematic of the design for documentation purposes. System Connectivity Manager allows you to generate a document schematic of your design.

Note: The document schematic is only meant for documentation purposes. You can do placement and routing changes, add notes, and plot the document schematic. You cannot cross reference, package, or add constraints in the document schematic.

For more information, see [Chapter 21, “Generating Document Schematic for a Design.”](#)

Design Debugging with Design Rule Checks (DRCs) and the Physical View

System Connectivity Manager lets you run design rule checks (DRCs) to identify connectivity and other errors in the design. System Connectivity Manager provides a standard set of DRCs. System Connectivity Manager also lets you write your own custom DRCs in Tcl language and run the custom DRCs from System Connectivity Manager. For more information on running DRCs, see [Chapter 19, “Running Design Rule Checks.”](#)

The Physical View in System Connectivity Manager provides a physical netlist view of the design as it appears in your board layout. You can use the physical view to debug the design with respect to the board layout and verify whether you have assigned the correct signal integrity (SI) models on components and pins, and assign SI models, if required. For more information on using the Physical View in System Connectivity Manager, see [Chapter 9, “Using the Physical View.”](#)

System Connectivity Manager User Guide

System Connectivity Manager: Introduction

Getting Started with System Connectivity Manager

This chapter describes the following sections:

- [Starting System Connectivity Manager](#) on page 44
- [System Connectivity Manager Start Page](#) on page 45
- [System Connectivity Manager User Interface](#) on page 48
 - [Component List](#) on page 50
 - [Signal List](#) on page 52
 - [Component Connectivity Details Pane](#) on page 56
 - [Signal Connectivity Details Pane](#) on page 64
 - [Matrix Connectivity View Pane](#) on page 68
 - [Menu Bar](#) on page 68
 - [Tabs](#) on page 69
 - [Toolbars](#) on page 70
 - [Status Bar](#) on page 73
 - [Hierarchy Viewer](#) on page 73
 - [File Viewer](#) on page 74
 - [Properties Window](#) on page 75
 - [Signal Navigate](#) on page 76
 - [Session Log Window](#) on page 77
 - [Violations Window](#) on page 78
- [Sorting the Data in System Connectivity Manager](#) on page 78

- [Filtering the Display of Information in System Connectivity Manager](#) on page 79

Starting System Connectivity Manager

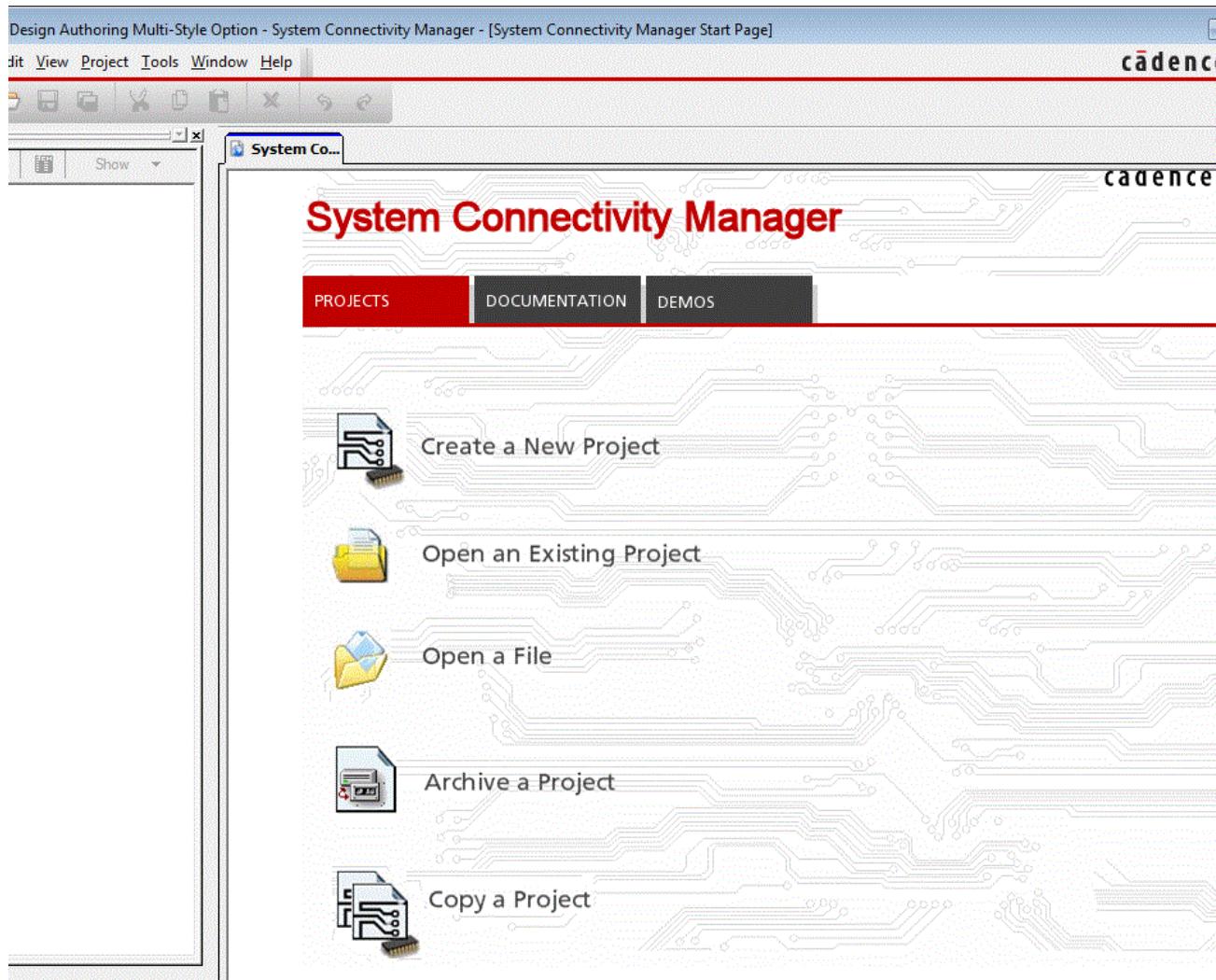
To start System Connectivity Manager

- To start System Connectivity Manager on Microsoft Windows, do one of the following:
 - From the Windows *Start* menu, choose *Programs – Allegro SPB – System Connectivity Manager*.
 - From the Windows Start menu, choose *Run* to open the Run dialog box. Type `scm` and press *Enter*.
 - Type the following command in the Windows command prompt:
`scm`
- To start System Connectivity Manager on Unix or Linux, open a terminal window and type the following command:
`scm`

System Connectivity Manager User Guide

Getting Started with System Connectivity Manager

The System Connectivity Manager start page appears.



System Connectivity Manager Start Page

The System Connectivity Manager start page appears when you do one of the following:

- Start System Connectivity Manager.
- Click the tab for the start page in the System Connectivity Manager workspace.
- Choose *Help – Display Start Page*.

You can use the System Connectivity Manager start page to do the following:

- [Create a New Project](#)
- [Open an Existing Project](#)
- [Open a File](#)
- [Archive a Project](#)
- [Copy a Project](#)
- [Access System Connectivity Manager Documentation](#)
- [View System Connectivity Manager Multimedia Demonstrations](#)

Create a New Project

To create a new project

Do one of the following:

- Click the *Create a New Project* icon in the Start Page.
- Choose *File New – Project*.

The New Project Wizard window appears.

For more information on creating projects in System Connectivity Manager, see [Chapter 3, “Project Creation and Setup.”](#)

Open an Existing Project

To open an existing project

1. Do one of the following:

- Click the *Open an Existing Project* icon in the Start Page.
- Choose *File – Open Project*.

The Open dialog box appears.

2. Select the project file (.cpm) and click *Open*.

The project is opened in System Connectivity Manager.

Open a File

To open a file

1. Do one of the following:

- Click the *Open a File* icon in the Start Page.
- Choose *File – Open – File*.
- Click  on the toolbar.

The Open dialog box appears.

2. Select the file you want to open and click *Open*.

The file is opened in a new tab in System Connectivity Manager.

You can open the following files in System Connectivity Manager:

- HTML files (.html)
- Verilog Files (.v)
- System Connectivity Manager Report Files (.dsr)

Archive a Project

To archive a project

1. Do one of the following:

- Click the *Archive a Project* icon in the Start Page.
- Choose *Project – Archive Project*.

The System Connectivity Manager Archiver window appears.

For more information on archiving projects, see [Chapter 24, “Archiving Projects.”](#)

Copy a Project

To copy a project

1. Do one of the following:

- Click the *Copy a Project* icon in the Start Page.
- Choose *Project – Copy Project*.

The System Connectivity Manager Copy Project window appears.

Access System Connectivity Manager Documentation

To access System Connectivity Manager documentation

1. Click the *DOCUMENTATION* tab in the Start Page.

The list of user and reference document for System Connectivity Manager are listed in the page.

2. Click on a document name to view the document.

View System Connectivity Manager Multimedia Demonstrations

1. Click the *DEMOS* tab in the Start Page.

The multimedia demonstrations for important features in System Connectivity Manager are listed in the page.

2. Click on a link for a demo to view the demo.

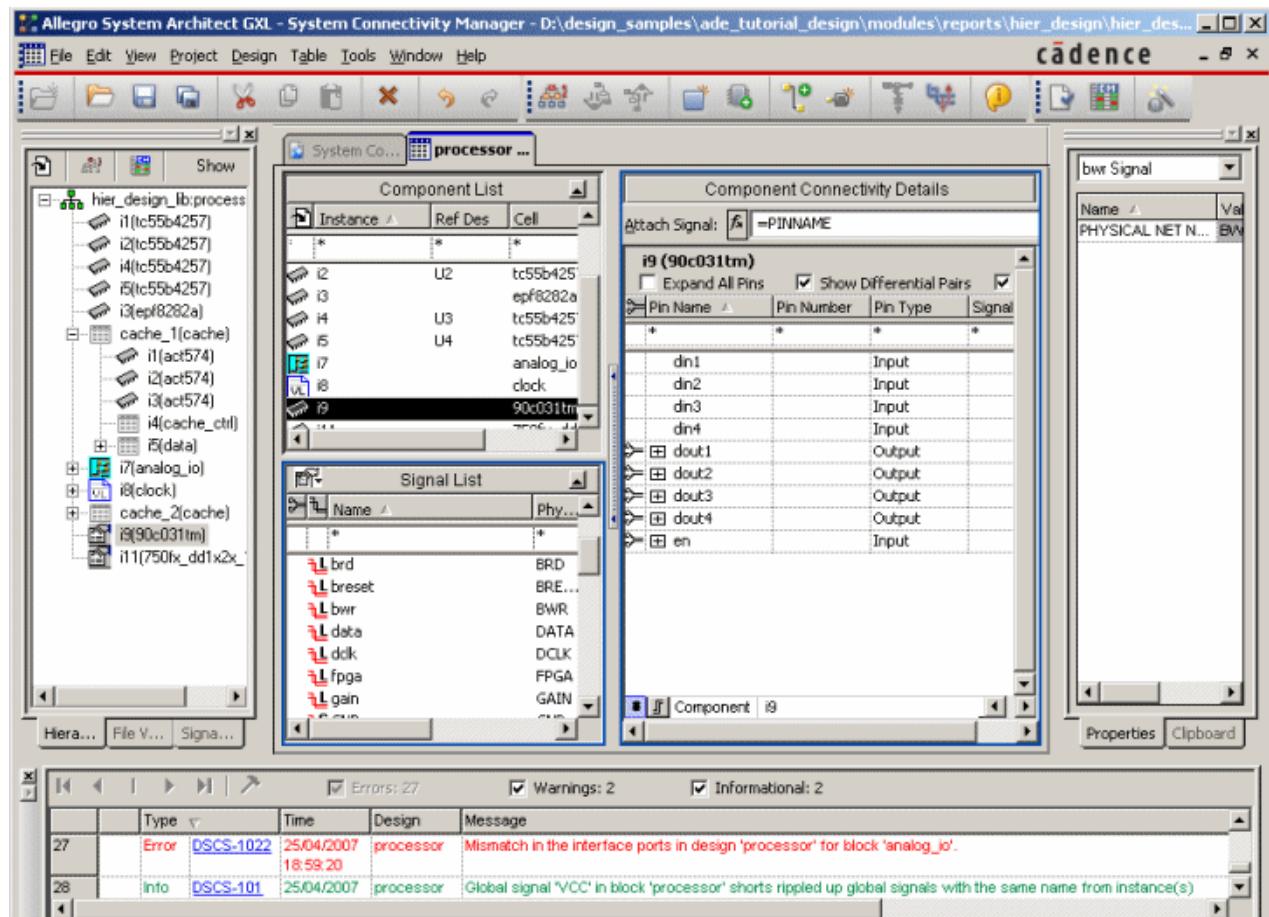
System Connectivity Manager User Interface

When you open a project in System Connectivity Manager, the System Connectivity Manager workspace appears.

System Connectivity Manager User Guide

Getting Started with System Connectivity Manager

Figure 2-1 System Connectivity Manager Workspace



At the center of System Connectivity Manager workspace lies the Spreadsheet Editor. You can use the Spreadsheet Editor to view or modify the information about components and blocks and their connectivity information.

The Spreadsheet Editor is the heart of System Connectivity Manager. You can use the spreadsheet editor to quickly manage components and blocks and the connectivity information for the components and blocks in the design.

The spreadsheet editor has the following four components:

- Component List
- Signal List
- Component Connectivity Details Pane
- Signal Connectivity Details Pane

Component List

You can use the Component List to work with the components and blocks in the design. Each row in the Component List corresponds to a component or block in the current block or design.

Figure 2-2 Component List

Instance	Ref Des	Cell			
*	*	*	*	*	*
i1		clock			
i2		mem_blk			
i3		analog_io			
i9		processor			
i18	U6	mcm			
i19	U7	irf7317			
i26	U15	pa0785			

The Component List displays the following information:



Displays the type of the component or block.

The following icons are used to display the type of a component or block:



Component added as Symbol



Component added as Package



Spreadsheet block



Schematic block



Verilog block

System Connectivity Manager User Guide

Getting Started with System Connectivity Manager

Name	Displays the instance name of the component or block. The first component you add in a design is assigned the instance name <code>i1</code> , the second component you add is assigned the instance name <code>i2</code> , and so on. You can modify the instance name as described in Modifying Component Instance Names on page 128.
Ref Des	Displays the reference designator of the component. You can modify the reference designator as described in Modifying Component Reference Designators on page 130.
Cell	Displays the component name.
	Indicates whether a comment is added for the component or block. The  icon next to a component or block indicates that a comment exists for the component or block. For more information on working with comments in the design, see Working with Comments on page 167.
	Indicates whether bypass capacitors have been added on the component. The  icon next to a component indicates that bypass capacitors have been added on the component. For more information on adding bypass capacitors, see Adding Bypass Capacitors on page 296.
Unconnected Pins	Displays the number of pins of the component that are not connected to signals. Note: The <i>Unconnected Pins</i> column is not displayed by default in the Component List. For more information on displaying the <i>Unconnected Pins</i> column, see Hiding/Showing Columns on page 650.
Filter	The filter row lets you use the wildcard characters * and ? and regular expressions to filter the display of information in the Component List. For more information on filtering the display of information in the panes in System Connectivity Manager, see Filtering the Display of Information in System Connectivity Manager on page 79.

For more information on working with components in the design, see the procedures described in [Working with Components](#) on page 107.

If you double-click on a component or block in the Component List, the connectivity information for the component or block is displayed in the [Component Connectivity Details](#) pane.

Signal List

You can use the Signal List to work with the signals in the design. The Signal List displays the list of signals in the current block or design and the global signals from the blocks added in the current block or design. Each row in the Signal List corresponds to a signal in the current design or block.

Figure 2-3 Signal List

The screenshot shows the Signal List pane with the following data:

Name	Phys Name	#
*	*	*
ADDRESS[7..0]	ADDRESS	3
GND	GND	0
IOCLK1	IOCLK1	0
IOCLK2	IOCLK2	0
IOCLK3	IOCLK3	0
IOCLK4	IOCLK4	0
VCC	VCC	0
DS_SUB	DS_SUB	0

The Signal List displays the following information:

Differential Pair

Displays whether the signal listed in the signal list pane is a differential pair signal.

The icon in the first column of the Signal List pane indicates that the signal is a differential pair.

System Connectivity Manager User Guide

Getting Started with System Connectivity Manager

Type Icon	<p>Displays the scope of the signal.</p> <p>The following icons are used to indicate the scope of the signal:</p> <ul style="list-style-type: none"> Input signal Output signal Inout signal Global signal Local signal <p>A local signal is a signal that is unique to a design. Local signals that have the same name in different designs will not be connected.</p> <p>Note: If you want local nets to be shorted at the top level, define the nets in the blocks as interface nets and then connect them explicitly, or define the nets in the blocks as global nets. When defined as global nets, the nets are implicitly connected.</p> <p>Global signals are used to make sure that the same voltage signals in different blocks are connected together. For more information on working with global signals, see About Global Signals in Hierarchical Designs on page 374.</p> <p>I/O signals are interface signals that talk to other blocks (or designs). For more information on working with ports or interface signals, see Working with Ports of a Block on page 369.</p> <p>You can modify the signal type as described in Modifying the Scope of a Signal on page 165.</p>
Name	<p>Displays the logical name of the signal.</p> <p>You can modify the logical name of a signal as described in Modifying the Logical Name of a Signal on page 165.</p>

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Getting Started with System Connectivity Manager

Phys Name	Displays the physical net name for the signal. For more information on how physical net names are assigned to signals, see How Physical Net Names are Assigned to Signals in Hierarchical Designs on page 381. You can modify the physical net name of a signal as described in Modifying the Physical Net Name of a Signal on page 166.
Conn	Displays the total number of pins connected to the signal. The default value is 0. When you connect the signal to more pins, the value in the <i>Conn</i> column is automatically updated.
 Filter	Indicates whether a comment is added for the signal. The  icon next to a signal indicates that a comment exists for the signal. For more information on working with comments in the design, see Working with Comments on page 167.

Show Buses

Use this option to display vectored signals in the Signal List pane in a collapsed format, as buses, or in the expanded format, as individual bits. By default, this command is selected, thus enabling vectored signals to be displayed as buses in the Signal List pane.

To display the individual bits of the vectored signals in the Signal List pane, deselect this option using one of the following methods.

- Right-click on the Signal List pane header and deselect *Show Buses*.
- Select the  button in the Signal List pane header and deselect *Show Buses*.

Displaying the bits of a vectored signal lets you connect bits of a vectored signal to pins using the Component Connectivity Details pane or the Signal Connectivity Details pane. For more information on using the Signal List with signals displayed in the expanded format, see [Viewing Bits of a Vector Signal in Signal List Pane](#) on page 149.

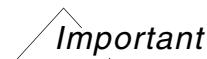
Show Differential Pairs

Use this option to display either the differential pairs or member nets of the differential pair in the Signal List Pane. By default, this option is selected, thus displaying differential pairs.

To display member nets of a differential pair perform one of the following steps.

- Right-click on the Signal List pane header and deselect *Show Differential Pair*.
- Select the  button in the Signal List pane header and deselect *Show Differential Pair*.

Instead of differential pair names, individual net names are displayed in the Signal List pane.



When you deselect the *Show Differential Pairs* option, the Differential Pair column disappears.

System Connectivity Manager User Guide

Getting Started with System Connectivity Manager

For more information on using the Signal List, see the procedures described in [Working with Signals](#) on page 143. When you double-click on a signal in the Signal List, the connectivity information for the signal is displayed in the [Signal Connectivity Details](#) pane.

Component Connectivity Details Pane

The Component Connectivity Details pane displays the connectivity information for the component or block you selected in the [Component List](#).

You can use the Component Connectivity Details pane to capture the connectivity information for the components and blocks in the design. The Component Connectivity Details pane lets you quickly connect component pins to signals, apply terminations, add pullups and pulldowns, assign signal integrity models, and add comments on component pins.

To display the Component Connectivity Details pane

Do one of the following:

- Double-click a component in the Component List
- Do the following:
 - a. Click  in the Component Connectivity Details pane or the Signal Connectivity Details pane to display the list of components in the design.
 - b. Click a component.

The connectivity information for the component is displayed in the Component Connectivity Details pane.

System Connectivity Manager User Guide

Getting Started with System Connectivity Manager

Figure 2-4 Component Connectivity Details Pane

Component Connectivity Details					
Attach Signal: <input type="button" value="fx"/>					
i2 (epf8282a) - U2					
<input type="checkbox"/> Expand All Pins	<input checked="" type="checkbox"/> Show Differential Pairs	<input checked="" type="checkbox"/> Show Vectors			
Pin Name	Pin Number	Pin Type	Signal	Termination	
*	*	*	*	*	
add18	79	Output			
[+] add[13..1]	58,60,61,62,63,6...	Output			
[+] bd[7..0]	18,19,20,21,22,2...	Input	ADDRESS[7..0]		
clkusr	50	Output	signal_0		
conf_done	11	Input	signal_1		
data2	9	Input	data2		
data3	8	Input	data3		
data4	7	Input	data4		
data5	6	Input	data5		
dclk	10	Input	dclk		
[+] DP_data	13,14	Input	D5_data	DPSeries	
[+] DP_msel	53,74	Input			
gain	28	Output			
i/o	16	Input	pc_web		
inputa	55	Input			
inputb	54	Input			

The fields in the Component Connectivity Details pane are described below:

Attach Signal Button

The button lets you use functions to automatically generate the signal names for the selected pins in the Component Connectivity Details pane.

For more information on using the button, see [Using the Attach Signal Button](#) on page 187.

Attach Signal Drop-Down List

The Attach Signal drop-down lets you do the following:

- Use functions to automatically generate signal names for pins.
- Connect a signal existing in the current design to the selected pins in the Component Connectivity Details pane.

For more information on using the Attach Signal drop-down list, see [Using the Attach Signal Drop-Down List](#) on page 196.

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- Component Displays the instance name, cell name and reference designator of the component.
For example, in the above figure:
 - i18 is the instance name of the component.
 - mcm is the cell name of the component.
 - MCM1 is the reference designator of the component.
- Expand All Pins By default, all the vector and differential pair pins are displayed in non-expanded mode in the Component Connectivity Details pane.
 - Select this check box if you want to expand all the vector and differential pair pins of the component to display the bits of the vector pins in the Component Connectivity Details pane. In this case, both the vector and the differential pins, along with the individual bits are displayed in the Component Connectivity Details pane.

<input checked="" type="checkbox"/> Expand All Pins	<input checked="" type="checkbox"/> Show Differential Pairs	<input checked="" type="checkbox"/> Show Vectors	
Pin Name	Pin Number	Pin Type	Signal
*	*	*	*
db	Y5,U7	Input	
dbg	Y5	Input	
dbb	U7	Input	
tstclk	W13,Y13	Input	
l2_tstclk	W13	Input	
l1_tstclk	Y13	Input	
a<31..0>	E5,B3,A3,...	Inout	
a<31>	E5	Inout	
a<30>	B3	Inout	
a<29>	A3	Inout	

If this check box is selected, the polarity of each pin of the

differential pair is also displayed in the Component Connectivity Details pane.

- Clear this check box if you want to display all the vector and differential pair pins of the component in non-expanded mode in the Component Connectivity Details pane.

<input type="checkbox"/> Expand All Pins	<input checked="" type="checkbox"/> Show Differential Pairs	<input checked="" type="checkbox"/> Show Vectors	
Pin Name	Pin Number	Pin Type	Signal
*	*	*	*
 db	Y5,U7	Input	
 tstclk	W13,Y13	Input	
 a<31..0>	E5,B3,A3,...	Inout	
aack	A8	Input	
abb	Y6	Inout	
 ap<3..0>	B8,A13,D1...	Inout	
artry	W7	Inout	
bg	W4	Inout	

Show Differential Pairs

By default, this check box is selected and differential pairs are displayed in the Component Connectivity Details pane.

<input type="checkbox"/> Expand All Pins	<input checked="" type="checkbox"/> Show Differential Pairs	<input type="checkbox"/> Show Vectors	
Pin Name	Pin Number	Pin Type	Signal
*	*	*	*
din1	1	Input	
din2	7	Input	
din3	9	Input	
din4	15	Input	
 dout1	2,3	Output	
 dout2	6,5	Output	
 dout3	10,11	Output	
 dout4	14,13	Output	
 en	12,4	Input	

- Clear this check box if instead of differential pairs, you want to display the individual pins of the differential pair in the Component Connectivity Details pane.
- Select this check box if you want to display the differential pairs instead of individual pins in the Component Connectivity Details pane.

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Getting Started with System Connectivity Manager

Show Vectors

By default, all the vector pins are displayed in non-expanded mode in the Component Connectivity Details pane.

- Clear this check box if you want that instead of vector pins, individual bits of a vector pin of the component are displayed in the Component Connectivity Details pane.

<input type="checkbox"/> Expand All Pins	<input type="checkbox"/> Show Differential Pairs	<input type="checkbox"/> Show Vectors	
Pin Name	Pin Number	Pin Type	Signal
*	*	*	*
a<0>	5	Input	ra<0>
a<1>	4	Input	ra<1>
a<2>	3	Input	ra<2>
a<3>	2	Input	ra<3>
a<4>	32	Input	ra<4>
a<5>	31	Input	ra<5>
a<6>	30	Input	ra<6>
a<7>	29	Input	ra<7>
...

- Select this check box if you want to display the vector pins of the component in the Component Connectivity Details pane.

<input type="checkbox"/> Expand All Pins	<input type="checkbox"/> Show Differential Pairs	<input checked="" type="checkbox"/> Show Vectors	
Pin Name	Pin Number	Pin Type	Signal
*	*	*	*
+ a<17..0>	12,13,14,1...	Input	,,ra<15>,r
ce*	6	Input	rcs0
+ dq<4..1>	26,23,10,7	Inout	rd<3..0>
eo*	27	Input	GND
+ io<3..1>	17,16,1	Inout	NC
we*	11	Input	rwe
...

For more information on working with vector pins in the Component Connectivity Details pane, see [Working with Connectivity on Vector Pins in the Component Connectivity Details Pane](#) on page 186.

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Functions The *Functions* drop-down list appears if you are viewing the connectivity information for a component that has more than one function.

In the *Functions* drop-down list:

- Select *All* to view the pins of all the sections in the package.
- Select the section number to view only the pins for the section in the package. This lets you focus on editing the connectivity information on the pins for the section in the package.

Filter The filter row lets you use the wildcard characters * and ? and regular expressions to filter the display of information in the Component Connectivity Details pane.

You can filter the display of information in the Component Connectivity Details pane if you want to view or edit the connectivity information on a specific set of pins. This lets you focus on editing the connectivity information on a specific set of pins and is especially useful when you are editing the connectivity information on a large pin-count device.

For more information on filtering the display of information in the panes in System Connectivity Manager, see [Filtering the Display of Information in System Connectivity Manager](#) on page 79.



Click this icon to display the list of components in the current design, as shown below.

Name	RefDes	Cell
i1	U14	mcm
i2	U4	mcm
i4	U18	irf7317

You can select a component in this list to display its connectivity information in the Component Connectivity Details pane.



Click this icon to display the list of signals in the current design, as shown below.

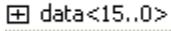
Name	Phys Name
afd	AFD_1
afs	AFS_1
cclock	CCLOCK_1_1
iord	IORD_1_1
iowr	IOWR_1_1
mrd	MRD_1
mready	MREADY_1
mwr	MWR_1
reset	RESET_1_1
rfd	RFD_1
rfs	RFS_1
sclock	SCLOCK_1_1
sel	SEL_1
set1	SET1_1
set2	SFT2_1

You can select a signal in this list to display its connectivity information in the Signal Connectivity Details pane. For more information on using the Signal Connectivity Details pane, see [Signal Connectivity Details Pane](#) on page 64.



Tip
To view row numbers in the Component Connectivity Details pane, choose *Tools — Options — Spreadsheet Editor* and select *Show Row Numbers in connectivity panes*.

Each row in the Component Connectivity Details pane displays the following connectivity information for a pin of the component.

Pin Name	Displays the logical pin names of the component. By default, vector pins are shown in non-expanded mode. For example, the vector pin <code>data<15..0></code> is displayed as:  <ul style="list-style-type: none">■ To display the bits of the vector pin, click  next to the vector pin name to display each bit of the vector pin in a separate row.■ To collapse the bits of the vector pin, click  next to the vector pin name■ To display the bits of all vector pins of the component, select the <i>Expand All Pins</i> check box in the Component Connectivity Details pane.■ To collapse the bits of all vector pins of the component, clear the <i>Expand All Pins</i> check box in the Component Connectivity Details pane. For more information on working with vector pins in the Component Connectivity Details pane, see Working with Connectivity on Vector Pins in the Component Connectivity Details Pane on page 186.
Pin Number	Displays the physical pin numbers of the pins of the component. The pin numbers of a vector pin are separated by commas.
Pin Type	Displays the pin type of pins of the component.
Signal	Displays the names of signals connected to pins of the component. For more information on connecting signals to pins in the Component Connectivity Details pane, see Signal Connectivity Details Pane on page 64.

Termination	Indicates the type of termination applied on the pins of the component. For more information on applying terminations, see Adding a Termination on page 285.
	Indicates that a pullup or pulldown is added on the pin. Pullups appear as a red triangle on top-right side of cell and pulldowns appear as a triangle on bottom-left side of cell. For more information on the icons that are displayed for pullups and pulldowns, see Pullup-Pulldown Icons on page 309. For more information on adding pullups and pulldowns, see Adding a Pullup or Pulldown on page 303.
	Indicates whether a comment is added for the pin. The comment icon () next to a pin indicates that a comment exists for the pin. For more information on working with comments in the design, see Working with Comments on page 167.

Signal Connectivity Details Pane

The Signal Connectivity Details pane displays the connectivity information for the signal you selected in the [Signal List](#).

You can use the Signal Connectivity Details pane to quickly connect a signal to component pins, apply terminations to pins, and assign signal integrity models.

To display the Signal Connectivity Details pane

Do one of the following:

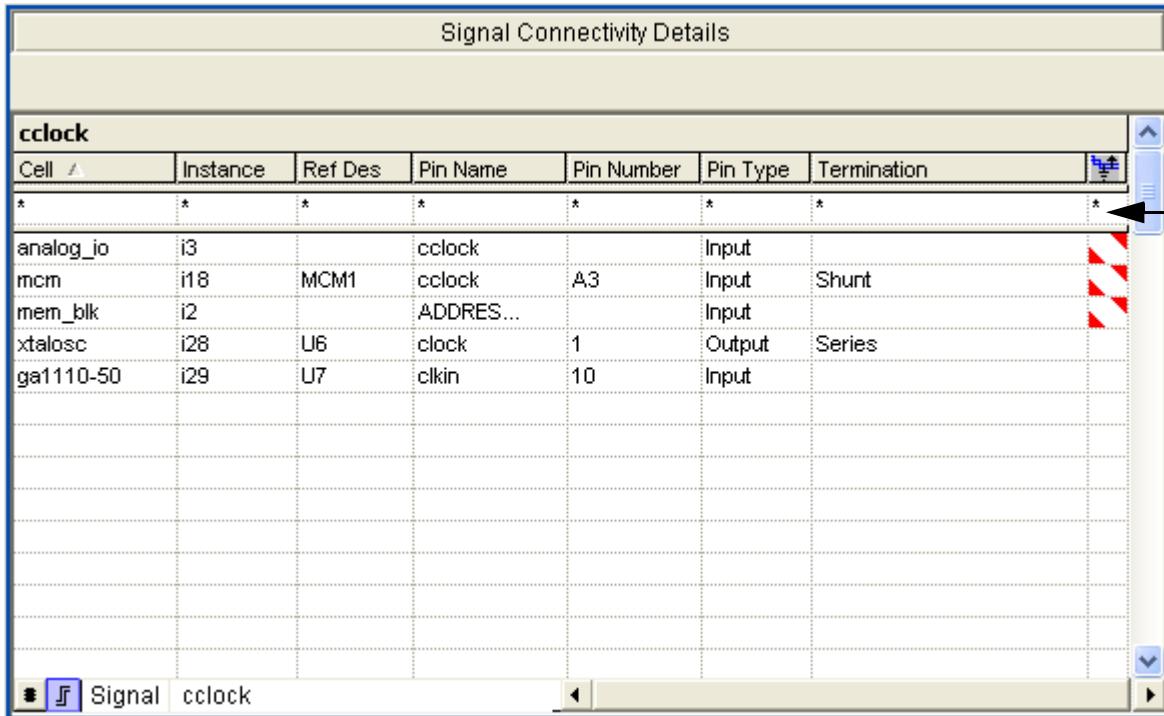
- Double-click a signal in the Signal List.
- Do the following:
 - a. Click  in the Component Connectivity Details pane or the Signal Connectivity Details pane to display the list of signals in the design.
 - b. Click a signal.

The connectivity information for the signal is displayed in the Signal Connectivity Details pane.

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Figure 2-5 Signal Connectivity Details Pane



Signal Connectivity Details							
cclock							
Cell	Instance	Ref Des	Pin Name	Pin Number	Pin Type	Termination	
*	*	*	*	*	*	*	*
analog_io	i3		cclock		Input		
mcm	i18	MCM1	cclock	A3	Input	Shunt	
mem_blk	i2		ADDRES...		Input		
xtalosc	i28	U6	clock	1	Output	Series	
ga1110-50	i29	U7	clkin	10	Input		

Each row in the Signal Connectivity Details pane displays the following connectivity information for a component pin that is connected to the signal.

Start Bit	Displays the start bit of the vectored signal that is connected to the pin of the component. This <i>Start Bit</i> column is displayed only if you are viewing the connectivity information for a vectored signal in the Signal Connectivity Details pane.
End Bit	Displays the end bit of the vectored signal that is connected to the pin of the component. This <i>End Bit</i> column is displayed only if you are viewing the connectivity information for a vectored signal in the Signal Connectivity Details pane.
Cell	Displays the name of the component whose pin is connected to the signal.
Instance	Displays the instance name of the component whose pin is connected to the signal.

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Ref Des	Displays the reference designator of the component whose pin is connected to the signal.
Pin Name	Displays the pin name of the pin that is connected to the signal.
Pin Number	Displays the pin numbers of the pin that is connected to the signal.
Pin Type	Displays the pin type of the pin that is connected to the signal.
Termination	Indicates the type of termination applied on the pin of the component. For more information on applying terminations, see Adding a Termination on page 285.
	Indicates that a pullup or pulldown is added on the pin of the component. Pullups appear as a red triangle on top-right side of cell and pulldowns appear as a triangle on bottom-left side of cell. For more information on the icons that are displayed for pullups and pulldowns, see Pullup-Pulldown Icons on page 309.
Note:	You can only view pullups and pulldowns in the Signal Connectivity Details pane. Use the Component Connectivity Details pane to work with pullups and pulldowns in the design. For more information on working with pullups and pulldowns, see Pullups and Pulldowns on page 303.
Filter	The filter row lets you use the wildcard characters * and ? and regular expressions to filter the display of information in the Signal Connectivity Details pane. For more information on filtering the display of information in the panes in System Connectivity Manager, see Filtering the Display of Information in System Connectivity Manager on page 79.

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The icons in the Signal Connectivity Details pane are described below:



Click this icon to display the list of components in the current design, as shown below.

Name	RefDes	Cell
i1	U14	mcm
i2	U4	mcm
i4	U18	irf7317

You can select a component in this list to display its connectivity information in the Component Connectivity Details pane.



Click this icon to display the list of signals in the current design, as shown below.

Name	Phys Name
afd	AFD_1
afs	AFS_1
cclock	CCLK_1_1
iord	IORD_1_1
iowr	IOWR_1_1
mrd	MRD_1
mready	MREADY_1
mwr	MWR_1
reset	RESET_1_1
rfd	RFD_1
rfs	RFS_1
sclock	SCLK_1_1
sel	SEL_1
set1	SET1_1
set2	SFT2_1

You can select a signal in this list to display its connectivity information in the Signal Connectivity Details pane.

Note: When Constraint manager is launched from SCM, and you select a row, the corresponding object is highlighted in the Signal List Pane in SCM. To dehighlight the object, you can use the right-click menu, and select the dehighlight option.

Matrix Connectivity View Pane

Besides the Signal Connectivity pane and Component connectivity pane, connectivity information can also be viewed in the Matrix view.

The Matrix Connectivity View pane displays the connectivity information for all the signals and components selected by you. The connectivity information is displayed in form of a matrix. Signal name form the rows of the matrix and the package or the component name constitute the columns of the matrix.

The Matrix View shows data in form of a spreadsheet where each signal can be connected to multiple pins of one or more components.

For more information on using the Matrix Connectivity View pane, see [Using Matrix Connectivity View Pane to Capture Connectivity](#) on page 204.

Menu Bar

The menu bar in System Connectivity Manager has the following menus.

Figure 2-6 Menu Bar



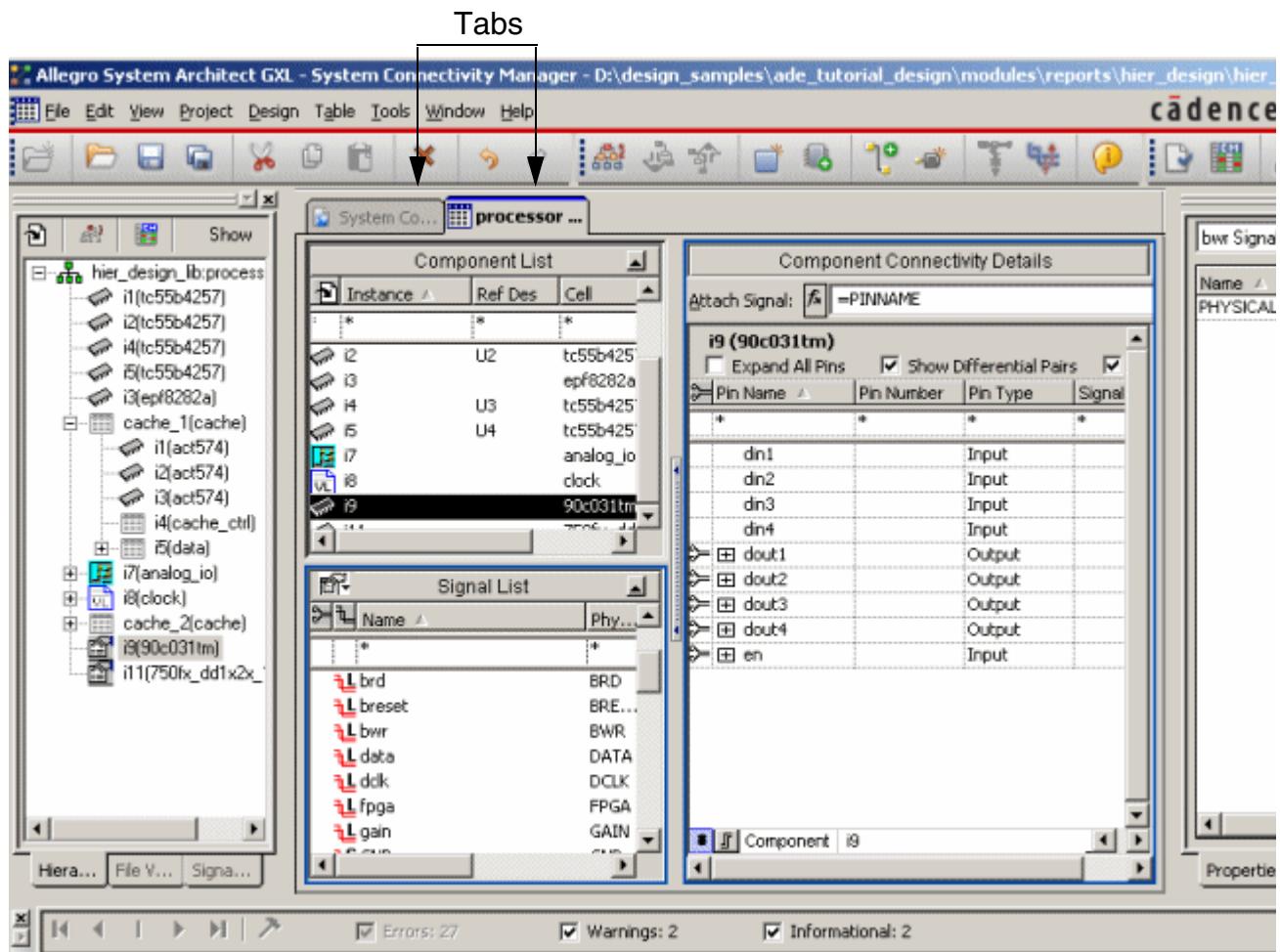
- File
- Edit
- View
- Project
- Design
- Table
- Tools
- Windows
- Help

For more information on customizing menus, see [Customizing Menus in System Connectivity Manager](#) on page 636 and [Customizing System Connectivity Manager Tools](#) on page 652.

Tabs

The files or blocks you open in System Connectivity Manager are displayed in different tabs.

Figure 2-7 System Connectivity Manager Workspace



To switch between different tabs

- Click on the tab you want to open.
- Press *Ctrl + Tab* key.

To close the current tab

- Choose *File – Close*.

Toolbars

System Connectivity Manager has the following three toolbars:

- [File Toolbar](#)
- [Design Toolbar](#)
- [Tools Toolbar](#)

File Toolbar



Descriptions for the buttons in the *File* toolbar are as follows:

Icon	Name	Description
	New Project	Create a new project. Equivalent to <i>File – New – Project</i> .
	Open	Opens an existing file. Equivalent to <i>File – Open – File</i> .
	Open Project Directory	Allows you to navigate to the project directory and search for project files in the packaged or physical folders, or to find any .zip files.
	Save	Saves the current block. Equivalent to <i>File – Save</i> .
	Save All	Saves all the open blocks. Equivalent to <i>File – Save All</i> .
	Cut	Removes the selected object and places it on the clipboard. Equivalent to <i>Edit – Cut</i> .
	Copy	Copies the selected object to the Clipboard. Equivalent to <i>Edit – Copy</i> .

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Icon	Name	Description
	Paste	Pastes the contents of the Clipboard at the cursor. Equivalent to <i>Edit – Paste</i> .
	Delete	Deletes the object selected in the design. Equivalent to <i>Edit – Delete</i> .
	Undo	Undoes the last command performed. Equivalent to <i>Edit – Undo</i> .
	Redo	Redoes the last command performed. Equivalent to <i>Edit – Redo</i> .

Design Toolbar



The buttons in the *Design* toolbar are described below.

Icon	Name	
	Change Root Design	Opens the Change Root dialog box. You can use this dialog box to change the root design of a hierarchical design. For more information, see Change Root on page 696. Equivalent to <i>Project – Change Root</i> .
	Descend Block	Opens the block you selected in the Component List for editing in context mode. Equivalent to <i>Design – Descend</i> .
	Ascend Block	Ascends the design hierarchy by opening the parent block for the current block. Equivalent to <i>Design – Ascend</i> .

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Icon	Name	
	Create New Block	Opens the Create Block dialog box. You can use this dialog box to create blocks in a hierarchical design. For more information on creating blocks, see Creating Blocks on page 339. Equivalent to <i>Design – Create Block</i> .
	Add Component	Opens Part Information Manager. You can use Part Information Manager to add components and blocks in your design. Equivalent to <i>Design – Add Component</i> .
	Add Signal	Opens the Add Signal(s) dialog box. You can use this dialog box to add signals in the current block or design. Equivalent to <i>Design – Add Signal</i> .
	Add Port	Opens the Add Port(s) dialog box. You can use this dialog box to add interface ports for the current block or design. Equivalent to <i>Design – Add Port</i> .
	Add Termination	Opens the Add Termination dialog box. You can use this dialog box to apply terminations to high speed nets in your design. Equivalent to <i>Object – Associate Components – Add Termination</i> .
	Add Pullup Pulldown	Opens the Add Pullup or Add Pulldown dialog box. You can use this dialog box to pullup or pulldown resistors to the design signals. Equivalent to <i>Object – Associate Components –Add Pullup/Pulldown</i> .
	Insert Comment	Opens the Comments dialog box. You can use this dialog box to add or edit comments for the selected object. Equivalent to <i>Object – Comments – Insert Comment</i>

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Tools Toolbar



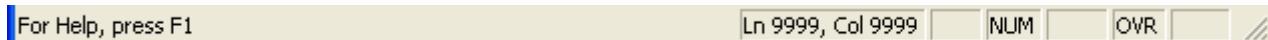
Icon	Name	Description
	Design Rules Check	Checks for design rules violations in the design. Equivalent to <i>Project – Design Rules Check</i> .
	Edit Constraints and Properties	Opens Constraint Manager. You can use Constraint Manager to capture properties and electrical constraints in the design. Equivalent to <i>Design – Edit Constraints</i> .
	Launch Part Developer	Increases the indentation of the selected line. Equivalent to <i>Tools – Allegro Part Developer</i> .

For more information on customizing toolbars, see [Customizing Toolbars in System Connectivity Manager](#) on page 647.

Status Bar

The status bar located at the bottom of the System Connectivity Manager window displays the status of operations you are performing in System Connectivity Manager. When you hover the cursor on a menu or on a toolbar button, the status bar displays a brief description of the menu or toolbar button.

Figure 2-8 Status Bar



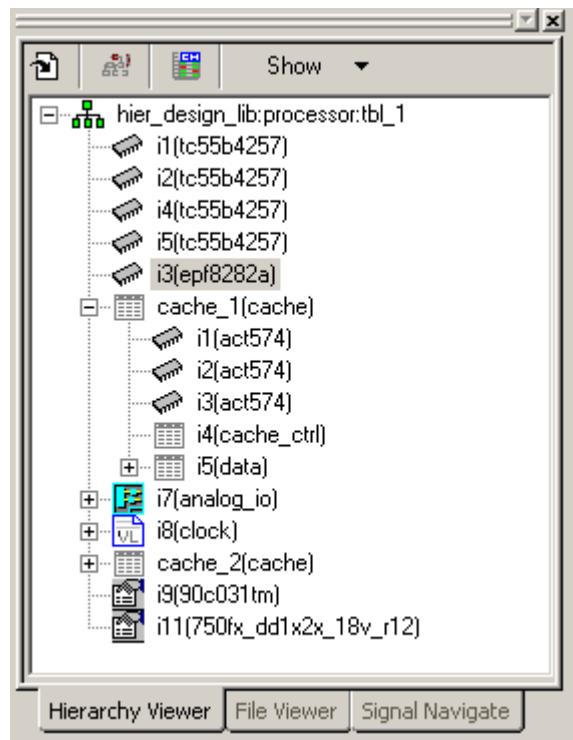
Hierarchy Viewer

The Hierarchy Viewer provides you a tree view of the complete design hierarchy and lets you quickly access all the blocks and components in your design.

To open Hierarchy Viewer, do one of the following:

- Choose *View – Hierarchy Viewer*.
- Press *Ctrl + Alt + H*.

Figure 2-9 Hierarchy Viewer



Note: For more information on using the Hierarchy Viewer, see [Using Hierarchy Viewer](#) on page 222.

File Viewer

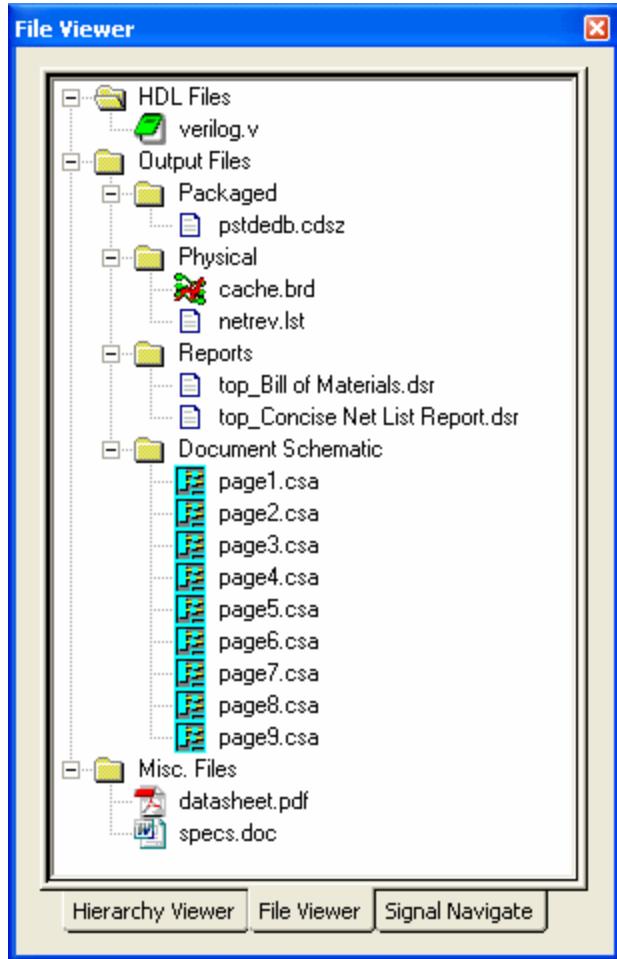
The File Viewer displays the files related to your design and lets you open the files from System Connectivity Manager. For example, you can double-click on the board file to open it in Allegro PCB Editor.

You can also add any other file that you want to refer to when working in the design. For example, you can add the design specifications document for your design in the File Viewer so that you can easily access it when you are working in the design.

To open File Viewer, do one of the following:

- Choose *View – File Viewer*.
- Press *Ctrl + Alt + F*

Figure 2-10 File Viewer



Note: For more information on using the File Viewer, see [Using the File Viewer](#) on page 230.

Properties Window

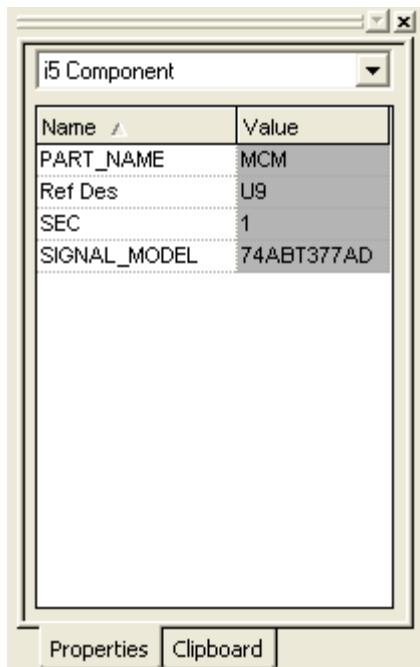
You can use the Properties window to work with properties on individual components, nets and pins in your design.

To open the Properties window, do one of the following:

- Choose *View – Properties Window*.

- Press *Ctrl + Alt + P*.

Figure 2-11 Properties Window



For more information on using the Properties window, see [Using System Connectivity Manager to Manage Properties](#) on page 253.

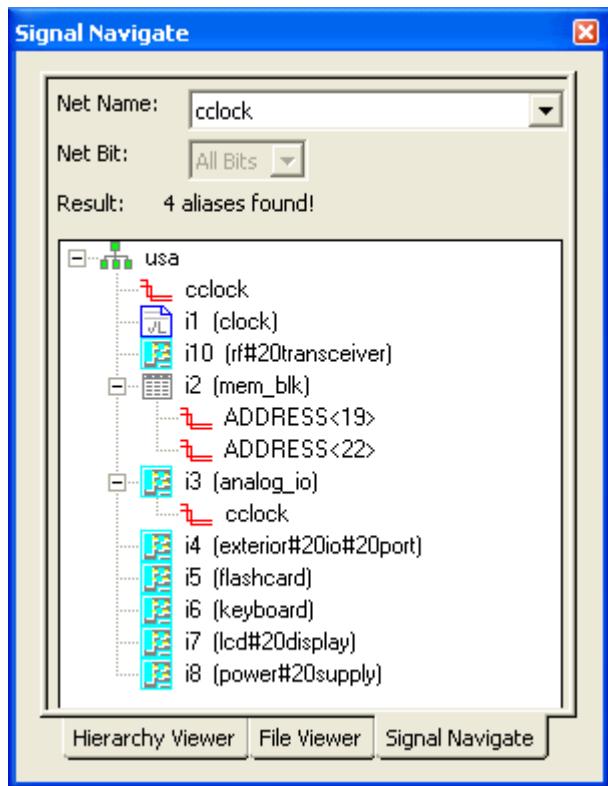
Signal Navigate

The Signal Navigate window lets you quickly view the aliases for a signal at all levels of a hierarchical design and navigate the signal to view its connectivity.

To open the Signal Navigate window, do one of the following:

- Choose *View – Signal Navigator*.
- Select a signal in the Signal List, right-click and choose *Signal Navigate*.
- Press *Ctrl + Alt + N*.

Figure 2-12 Signal Navigate Window



Note: For more information on using the Signal Navigate window, see [Using Signal Navigate](#) on page 226.

Session Log Window

The Session Log window displays the details of the current session. These details include the information about opened design files and packaged designs.

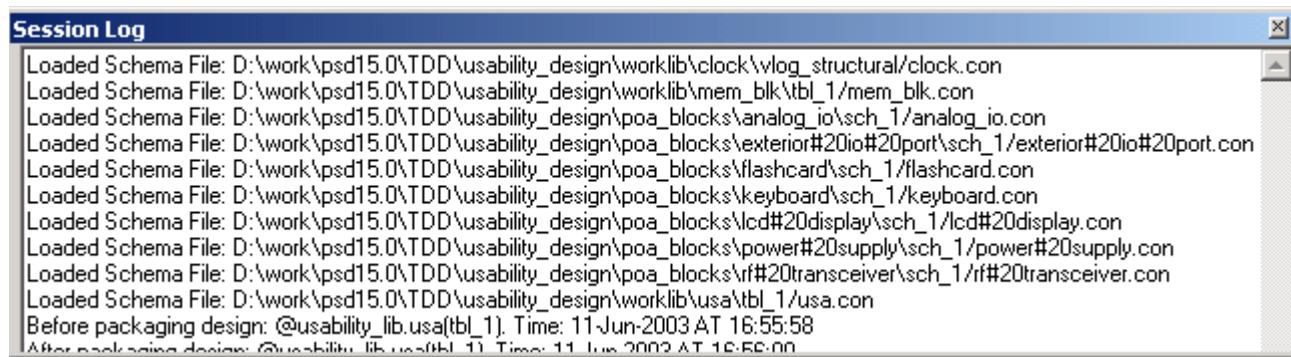
To open the Session Log, do one of the following:

- Choose *View – Session Log*.
- Press *Ctrl + Alt + L*.

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Figure 2-13 Session Log Window



Violations Window

The Violations window displays the error, warning, and informational messages that occur while working in System Connectivity Manager. To highlight the object causing the error, warning or informational message, double-click on the row for the message.

To open the Violations window, do one of the following:

- Choose *View – Violations*.
- Press *Ctrl + Alt + V*.

Figure 2-14 Violations Window

Violations					
	Type	Time	Design	Message	Action
43	Info	DSCS-101 20/06/2005 13:17:20	usa	Global signal 'lnf2v' in block 'usa' shorts rippled up global signals with the same name from instance(s) '13'.	Resolve
44	Info	DSCS-101 20/06/2005 13:17:20	usa	Global signal 'gnd' in block 'usa' shorts rippled up global signals with the same name from instance(s) '12,32'.	Resolve
45	Error	DSCS-2000 20/06/2005 13:17:20	usa	*ERROR: Unable to find Ibis Device model p14uf that is assigned to component @usability_llb.usa(tbl_1)@poa_blocks.analog_io(sch_1) page1_1p.	Resolve
46	Error	DSCS-2000 20/06/2005 13:17:20	usa	*ERROR: Unable to find Ibis Device model p14uf that is assigned to component @usability_llb.usa(tbl_1)@poa_blocks.analog_io(sch_1) page1_2p.	Resolve

For more information on using the Violations window, see [Violations](#).

Sorting the Data in System Connectivity Manager

You can sort the data displayed in a column in the Component List, Signal List, Component Connectivity Details pane, Signal Connectivity Details pane, Physical Part List, Physical Net List, Physical Part Connectivity Details pane, and the Physical Net Connectivity Details pane.

To sort data in a column

1. Do one of the following:

- Click on a column heading name.
- Click on a pane in the spreadsheet editor and choose *View – Sort By – <column_name>*.

By default, the data is sorted in alphanumeric order. For example, in alphanumeric sorting, the reference designators in the Component List will be sorted in the following order:

U1, U2, U3, U10, U11, U20, U21...

To alphabetically sort the data in a pane, click on the pane in the spreadsheet editor and choose *View – Sort By – Sort As Alpha*. For example, in alphabetic sorting, the reference designators in the Component List will be sorted in the following order:

U1, U10, U11, U2, U20, U21, U3...

Filtering the Display of Information in System Connectivity Manager

System Connectivity Manager provides a filter row that lets you use wildcard characters and regular expressions to filter the display of information in the following panes:

- Component List
- Signal List
- Component Connectivity Details pane
- Signal Connectivity Details pane
- Physical Part List
- Physical Net List
- Physical Part Connectivity Details pane
- Physical Net Connectivity Details pane

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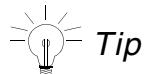
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Figure 2-15 Filter row in Component Connectivity Details pane

The screenshot shows the 'Component Connectivity Details' pane for a component named 'i2 (epf8282a) - U2'. At the top, there are three checkboxes: 'Expand All Pins' (unchecked), 'Show Differential Pairs' (checked), and 'Show Vectors' (checked). Below the checkboxes is a table with columns: Pin Name, Pin Number, Pin Type, Signal, and Termination. A horizontal row of asterisks (*) serves as a filter bar. An arrow points from the word 'Filter' to the right side of this bar. The table lists various pins with their details. For example, pin 'add18' is an output pin number 79. The status bar at the bottom shows the text 'Component i2'.

Component Connectivity Details				
i2 (epf8282a) - U2				
<input type="checkbox"/> Expand All Pins	<input checked="" type="checkbox"/> Show Differential Pairs	<input checked="" type="checkbox"/> Show Vectors		
Pin Name	Pin Number	Pin Type	Signal	Termination
*	*	*	*	*
add18	79	Output		
add[13..1]	58,60,61,62,63,6...	Output		
bd[7..0]	18,19,20,21,22,2...	Input	ADDRESS[7..0]	
clkusr	50	Output	signal_0	
conf_done	11	Input	signal_1	
data2	9	Input	data2	
data3	8	Input	data3	
data4	7	Input	data4	
data5	6	Input	data5	
dclk	10	Input	dclk	
DP_data	13,14	Input	DS_data	DPSeries
DP_msel	53,74	Input		
gain	28	Output		
i/o	16	Input	pc_web	
inputa	55	Input		
inputb	54	Input		

Filtering the display of information lets you focus on working on a specific set of objects in the design. For example, you can filter the display of information in the Component Connectivity Details pane to display a specific set of pins. This lets you focus on editing the connectivity information on a specific set of pins. This is especially useful when you are editing the connectivity information on a large pin-count device.



Tip
The status bar displays the filtering mechanism in use: wildcards or regular expressions.

Using Wildcard Characters

You can use the wildcard characters * and ? to filter the display of information.

Wildcard Character	Description
*	An asterisk matches any number of characters.
?	The question mark matches any single character.

Examples

- a* Displays data starting with the character a.
- *a Displays all data ending with the character a.
- *<* Displays vector pins or signals.
For example, if you enter *<* in the filter field for the *Name* column in the Signal List, only vectored signals are displayed in the Signal List.
- c?k Displays data like clk, crk, cdk, and so on.

Using Regular Expressions

Regular expressions are a concise and flexible notation for filtering patterns of text. Regular expressions are made up of normal characters and metacharacters.

To switch on regular expressions in filters select *Options — General — Use Regular Expressions in Filters*.

Normal Characters in Regular Expressions

Normal characters include upper and lower case letters and digits—A to Z, a to z, and 0 to 9 and all characters except \ ! ! *

For example, if you enter a in the filter field for the *Pin Name* column in the Component Connectivity Details pane, only pins having the name a are displayed in the Component Connectivity Details pane.

Metacharacters in Regular Expressions

The metacharacters used in regular expressions have special meanings and are described below.

Metacharacter	Description
\	<p>A backslash (\) followed by any metacharacter matches the literal character itself. That is, the backslash escapes the metacharacter.</p> <p>For example, * is used to match the asterisk sign * rather than zero or more occurrences of the character immediately preceding.</p> <p>Examples</p> <ul style="list-style-type: none">■ Use * \ * to display only pin names ending with *.■ Use a * \ * to display only pin names starting with a and ending with *.
	<p>Matches the conditions on the left side and the right side of the pipe character.</p> <p>For example, the regular expression a* c* matches strings starting with a and c.</p>
!	<p>Excludes the characters following the ! character.</p> <p>For example, the regular expression ! a* excludes all strings starting with a. The regular expression ! a* b* excludes all strings starting with a and b.</p>

Project Creation and Setup

This chapter describes the following sections:

- [Creating Design Projects](#) on page 84
- [Files Created for Your New Project](#) on page 91
- [Project Files](#) on page 94
- [The cds.lib File](#) on page 100
- [Setting Up the Project](#) on page 101
- [Setting Up the Vector Notation for a Project](#) on page 102
- [Setting Differential Pair Naming Convention](#) on page 103
- [Setting Up Libraries for a Project](#) on page 105
- [Setting Up Physical Part Table Files for a Project](#) on page 106

Creating Design Projects

The New Project Wizard guides you through creating your project in System Connectivity Manager. You can use the New Project Wizard to create a new design project, or to create a project from a structured Verilog file.

For more information, see the following topics:

- [Creating a New Design Project](#) on page 84
- [Creating a Project from a Verilog File](#) on page 87

Creating a New Design Project

To create a new design project

1. Do one of the following:

- Click the *Create a New Project* icon in the System Connectivity Manager start page.
- Choose *File – New – Project*.

The *Project Name, Location and Reference Library Location* page appears.

2. In the *Project Name* field, type your project name.

Note: Use lowercase letters, numbers and the underscore (_) character in library names. Using mixed-case library names, might cause problems when you move your design across platforms.

3. By default, System Connectivity Manager creates the project files in a directory with the name same as the name specified by you in the Project Name field. If required, you can specify a different folder name in the text box next to the *Create Project Directory* check box.

4. In the *Project Location* field, type the path to the directory in which you want to create the project, or click the browse button to select the directory in which you want to create the project.

Note: To create project files in the folder specified by the *Project Location* field, clear the *Create Project Directory* check box.

Note: If you want to create the project in a directory that does not exist in the path, add the name for the new directory to the path (for example: \cpu). The New Project Wizard will create the folder in the path.

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Note: You can set the TDD_START_PROJ_LOCATION environment variable to specify the default location in which all new design projects will be created. For example, if you specify c:\designs as the value for the TDD_START_PROJ_LOCATION environment variable, the path c:\designs will be displayed by default in the *Project Location* field.

Note: Run a tcl script on SCM launch by using the

```
-tclfile option scm -tclfile <path to tcl file>
```

This command line argument will launch scm and then run the tcl file contents within SCM. For Example, if your tcl file has the following commands

```
openProject test.cpm addSignal [list GND global '0 v']
```

Then scm will open the project test.cpm and also add a global GND signal with 0 V voltage to the design.

Note:

5. Specify the name and path to the cds.lib file containing the path to the reference libraries in your installation.

The default reference library cds.lib file is located at
<install_dir>\share\cdssetup\

6. Click *Next*.

The *Project Libraries* page appears with the list of libraries available for your project libraries.

7. Select the libraries for your project by placing them in the *Project Libraries* list.

- To add a library to the *Project Libraries* list, select the library in the *Available Libraries* list and then click *Add*.
- To add more than one library to the *Project Libraries* list, press *Ctrl* and select the libraries. Then, click *Add*.
- To add all the libraries in the *Available Libraries* list, click *Add All*.
- To remove a library from the *Project Libraries* list, select the library and then click *Remove*.
- To remove more than one library from the *Project Libraries* list, press *Ctrl* and select the libraries. Then, click *Remove*.
- To remove all the libraries from the *Project Libraries* list, click *Remove All*.

8. Choose the search order for your project libraries. The order in which libraries are listed in the *Project Libraries* list determines their search order.

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- To move a library one level up, select the library and then click Up.
- To move a library one level down, select the library and then click Down.

9. Click *Next*.

The *Project Work Libraries* dialog box appears.

10. Specify the working libraries for the project. These are the libraries in which System Connectivity Manager maintains the libraries specific to your project.

By default, the New Project Wizard creates a working library named <projectname>_lib. This <projectname>_lib library is displayed in the *Design Working Libraries* list. If you created the project in a new directory or in a directory that does not contain a cds.lib file, a cds.lib file is automatically created in the project directory. The cds.lib file contains an entry for the <projectname>_lib library.

- Click *Add*, specify a library name in the *Enter the Working Library Name* dialog box and click *OK*, to add a working library for the project.

Note: Use lowercase letters, numbers and the underscore (_) character in library names. Using mixed-case library names, might cause problems when you move your design across platforms.

- Select a library and click *Remove* to remove the library.

11. Click *Next*.

The *Design Name* page appears.

To create a new design

- a. In the *Select Work Library Name* drop-down list, choose the library in which you want to create the top-level design.
- b. In the *Enter Top Level Design Name* field, type a name for the top-level design for the project.

Note: Use lowercase letters, numbers and the underscore (_) character in library names. Using mixed-case library names, might cause problems when you move your design across platforms.

To select an existing design

- a. In the *Select Work Library Name* drop-down list, choose the library that contains the top-level design for your project.
- b. Click the browse button, select a design from the *Existing Design Names* list, and then click *OK*.

12. Select the implementation type for the top-level design. The default option is Table and it creates a Spreadsheet-based design.

13. Click *Next*.

The *Summary* page displays your project specifications.

14. Do one of the following.

- To create the project, click *Finish*.
- To change the project options, click *Previous* and edit the information you entered in each page. When you finish, click *Next* until the *Summary* page appears. Click *Finish* to create the project.

Creating a Project from a Verilog File

System Connectivity Manager lets you create a project from a structured Verilog HDL file. When you create a project from a structured Verilog HDL file, blocks are created in the library for every module in the Verilog file.

To create a project from a Verilog file

1. Choose *File – New – Project From Verilog File*.

The *Project Name, Location and Reference Library Location* page appears.

2. In the *Project Name* field, type your project name.

Note: Use lowercase letters, numbers and the underscore (_) character in library names. Using mixed-case library names, might cause problems when you move your design across platforms.

3. In the *Project Location* field, type the path to the directory in which you want to create the project, or click the browse button to select the directory in which you want to create the project.

Note: If you want to create the project in a directory that does not exist in the path, add the name for the new directory to the path (for example: \cpu). The New Project Wizard will create the folder in the path.

Note: You can set the TDD_START_PROJ_LOCATION environment variable to specify the default location in which all new design projects will be created. For example, if you specify c :\designs as the value for the TDD_START_PROJ_LOCATION environment variable, the path c :\designs will be displayed by default in the *Project Location* field.

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4. Specify the name and path to the `cds.lib` file containing the path to the reference libraries in your installation.

The default reference library `cds.lib` file is located at
`<install_dir>\share\cdssetup\`

5. Click *Next*.

The *Project Libraries* page appears with the list of libraries available for your project libraries.

6. Select the libraries for your project by placing them in the *Project Libraries* list.

- To add a library to the *Project Libraries* list, select the library in the *Available Libraries* list and then click *Add*.
- To add more than one library to the *Project Libraries* list, press *Ctrl* and select the libraries. Then, click *Add*.
- To add all the libraries in the *Available Libraries* list, click *Add All*.
- To remove a library from the *Project Libraries* list, select the library and then click *Remove*.
- To remove more than one library from the *Project Libraries* list, press *Ctrl* and select the libraries. Then, click *Remove*.
- To remove all the libraries from the *Project Libraries* list, click *Remove All*.

7. Choose the search order for your project libraries. The order in which libraries are listed in the *Project Libraries* list determines their search order.

- To move a library one level up, select the library and then click *Up*.
- To move a library one level down, select the library and then click *Down*.

8. Click *Next*.

The *Project Work Libraries* dialog box appears.

9. Specify the working libraries for the project. These are the libraries in which System Connectivity Manager maintains the libraries specific to your project.

By default, the New Project Wizard creates a working library named `<projectname>.lib`. This `<projectname>.lib` library is displayed in the *Design Working Libraries* list. If you created the project in a new directory or in a directory that does not contain a `cds.lib` file, a `cds.lib` file is automatically created in the project directory. The `cds.lib` file contains an entry for the `<projectname>.lib` library.

- Click *Add*, specify a library name in the *Enter the Working Library Name* dialog box and click *OK*, to add a working library for the project.

Note: Use lowercase letters, numbers and the underscore (_) character in library names. Using mixed-case library names, might cause problems when you move your design across platforms.

- Select a library and click *Remove* to remove the library.

10. Click *Next*.

The *Verilog Import Details* page appears.

- 11.** Specify the name and path to the Verilog file you want to import, or click the browse button to select the Verilog file.
- 12.** In the *Select Top Level Work Library* drop-down list, select the name of the working library in which you want to create blocks for the modules in the Verilog file.

Blocks are created in the library for every module in the Verilog file. For example, if you import the following Verilog file, two blocks named `Top` and `Mid` are created in the library.

Contents of Verilog File

```
module Top ( x, y, carry_out, sum, carry_in);  
    input x, y;  
    output sum, carry_in, carry_out;  
endmodule  
  
module Mid ( x,y,carry,sum);  
    input x, y;  
    output sum, carry;  
endmodule
```

- 13.** In the *Select Top Level Design* drop-down list, select the name of the module in the Verilog file that you want to use as the top-level design for the project.
- 14.** Select the *Use Instance Names as Ref. Des.* check box if you want to use the instance names for components in the Verilog file as reference designators.

For example, if you select this check box and import the following Verilog file, the reference designator assigned for the resistors will be `I1`, `I2`, `I3` and the reference designator for the capacitor will be `I4`.

Contents of Verilog File

```
module res (in, out);  
    input in;  
    output out;
```

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```
    wire w1,w2;
    resistor i1 (in ,w1);
    resistor i2 (w2 ,out);
    resistor i3 (in ,out);
    capacitor i4 (in ,out);
endmodule
```

If you do not select this check box, the reference designators R1, R2 and R3 are assigned to the resistors and the reference designator C1 is assigned to the capacitor.

15. Select the *Map Cells/Port Names* check box if you want to map cell names and port names.

System Connectivity Manager lets you use a map file to map component names in the Verilog file to cell (component) names in the libraries added for your project. You can also use the map file to map the port names of a component in the Verilog file to the port names of the cell (component) in a library.

16. Specify the name and path to the map file you want to use to map component names in the Verilog file to cell names and port names in the Verilog files to port names of the cell.

For example, if you import the following Verilog file

Contents of Verilog File

```
module example ();
    wire a,b,c;
    and_gate i1 (in1 (a),
                  in2 (b),
                  out1 (c));
endmodule
```

and select the following map file,

Contents of Map File

```
(  
("and_gate" "ls00"  
(ports  
    ("in1" "a")  
    ("in2" "b")  
    ("out1" "\y* ")  
)  
)  
)
```

the following happens when you import the Verilog file:

- A block named `example` is created in the selected library

- The component `and_gate` gets mapped to the cell (component) `ls00` in the libraries added for the project.
- The port `in1` of the component `and_gate` gets mapped to port `a` of the `ls00` cell.
- The port `in2` in the component `and_gate` gets mapped to port `b` of the `ls00` cell.
- The port `out1` in the component `and_gate` gets mapped to port `y*` of the `ls00` cell.

17. Click *Next*.

The *Summary* page displays your project specifications.

18. Do one of the following.

- To create the project, click *Finish*.
- To change the project options, click *Previous* and edit the information you entered in each page. When you finish, click *Next* until the *Summary* page appears. Click *Finish* to create the project.

The project is opened in System Connectivity Manager. System Connectivity Manager sets the module you select as the top-level design as the root design for the project. The top-level design will be in Verilog format.

Files Created for Your New Project

When you create a new project, System Connectivity Manager creates the following:

■ A project file (`<projectname>.cpm`).

The project file contains all the setup information you have specified for the project. For more information on project files, see [Project Files](#).

■ A `cds.lib` file

The `cds.lib` file determines the list of available libraries from which you can choose the project libraries for your project. It contains the logical names of libraries and their physical locations.

For more information on the `cds.lib` file, see [The cds.lib File](#) on page 100.

■ A `<project_name>.lib` directory.

The `<project_name>.lib` directory is the contains the designs you capture in System Connectivity Manager.

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Each design is stored in a subdirectory within the `<project_name>.lib` directory. This subdirectory is known as a cell. A cell can represent the entire design or just a portion of the design (or hierarchy). Each cell or design contains subdirectories that represent different design phases (known as cell views). The library-cell-view structure of the `<project_name>.lib` directory is shown in [Figure 3-1](#) on page 93.

- **A `devices.dml` file**

The `devices.dml` file is the default working signal integrity (SI) device model library for the project. The SI models you create, or the default SI models generated by System Connectivity Manager for two-pin discrete devices are stored in this file, unless you have specified another file as the working SI model library for the project. For more information on the `devices.dml` file, see [Chapter 12, “Working with Signal Integrity Models.”](#)

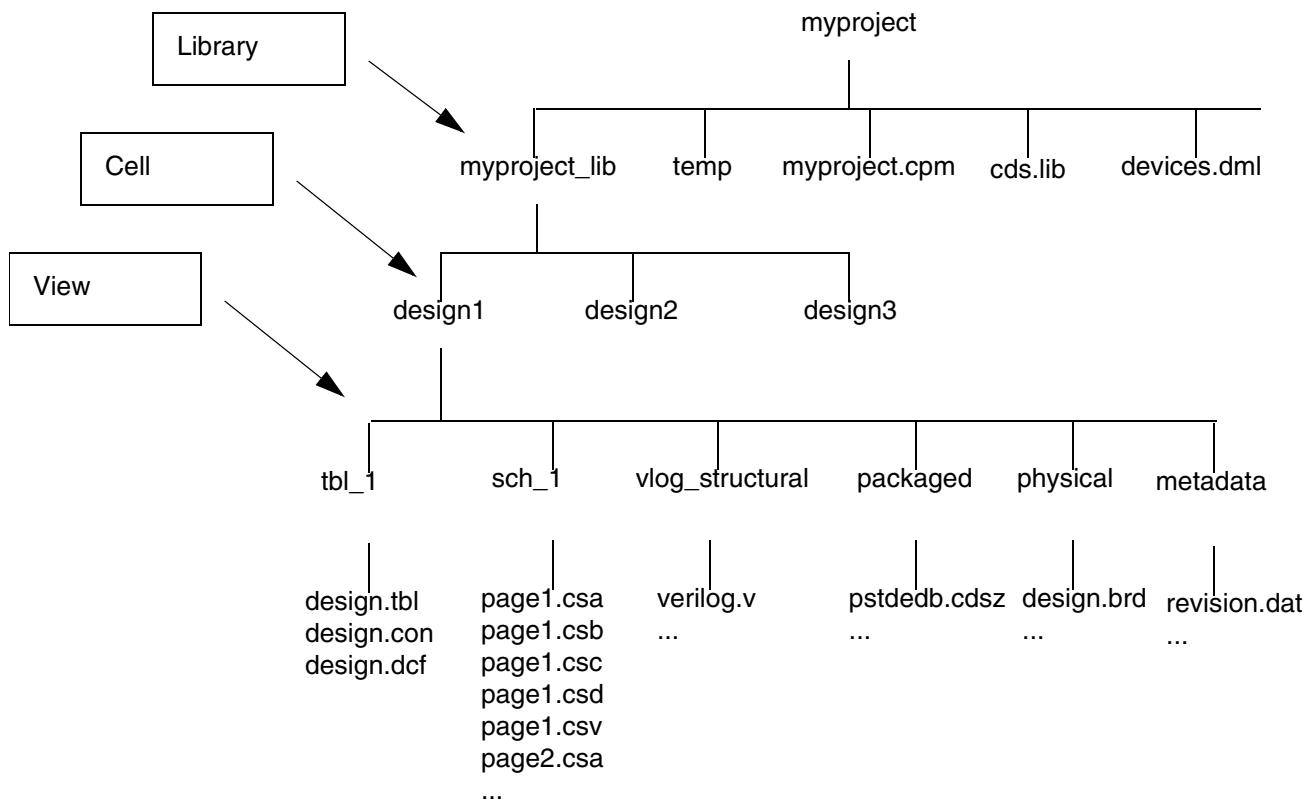
- **An application temp directory (`temp`)**

Temporary files created by Cadence applications are placed in the `temp` directory. You can delete the contents of this directory. You can also specify your own application temp directory in the [Paths](#) tab of the [Setup](#) dialog box.

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Figure 3-1 Project Structure



The following table describes each view in a design library.

View	Description
tbl_1	Contains the table based design.
sch_1	Contains the schematics.
vlog_structural	Contains the Verilog description of the design.
entity	Contains an HDL description of the cell (known as a module). This view is present only if the cell contains a symbol view that is used in a hierarchical design.
packaged	Contains the results of packaging.
physical	Contains the PCB layout.
metadata	Contains version information for the design.

Project Files

System Connectivity Manager manages all the information about a project—such as its libraries, physical part table files, packaging options, and so on—through project files.

There is a hierarchy of files followed by System Connectivity Manager while looking for directives set for a project:

- Local Project Files—named `<project>.cpm`
- Site Project File—named `site.cpm`
- Installation Project File—named `cds.cpm`

Note: The setup directives you specify (that is, the directives in the `<projectname>.cpm` file) always have precedence over the `site.cpm` directives, which in turn have precedence over the `cds.cpm` directives. When you open a project, System Connectivity Manager gets the setup directives you specified for that project from the `<projectname>.cpm` file and the default values for other directives from the `site.cpm` file. If they are not defined in the `site.cpm` file, System Connectivity Manager obtains the default values from the `cds.cpm` file.

Local Project Files

When you create a new project, System Connectivity Manager creates a project file called `<projectname>.cpm` in the project directory. The `<projectname>.cpm` file includes the following setup information for your project:

- The name of the top-level design and the library in which it is located.
- The list of project libraries.
- The location of the temporary directory where tools generate intermediate data
- Setup directives for System Connectivity Manager, Design Entry HDL, PCB Editor, and any other tool launched from the project.

The default setup information is maintained in an installation project file (`cds.cpm`) shipped by Cadence. The defaults in the `cds.cpm` file apply to all your projects. If you want to change these defaults, create a site project file (`site.cpm`) for your site.

When you open a project, System Connectivity Manager gets the setup directives you specified for that project from the `<projectname>.cpm` file and the defaults for the other directives from the `site.cpm` and `cds.cpm` files. Your setup directives always have precedence over the `site.cpm` directives, which in turn have precedence over the `cds.cpm` directives.

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Project File (.cpm) example

```
{ Machine generated file created by SPI }
{ Last modified was 19:33:15 Sunday, June 19, 2005 }
{ NOTE: Do not modify the contents of this file. If this is regenerated by }
{       SPI, your modifications will be overwritten. }

START_GLOBAL
design_name 'processor'
design_library 'tutorial lib'
library 'tutorial lib' 'classlib' 'discrete' 'standard'
temp_dir './temp'
ref_cdslib_path 'c:/designs/reference/ref_lib/cds.lib'
cpm_version '15.1'
session_name 'Project4701'
END_GLOBAL

START_ECSET_MODELS
retain_existing_xnets_and_diffpairs 'NO'
END_ECSET_MODELS

START_DESIGNSTUDIO
cap 'discrete.cap.VALUE'
gen_pstfiles 'TRUE'
update_allegroboard 'TRUE'
overwrite_constraints 'OFF'
etch_removal 'NO'
ignore_fixed 'NO'
replace_symbol '2'
launch_option '3'
last_board_file 'test.brd'
res 'discrete.res.VALUE'
END_DESIGNSTUDIO
```

Site Project File

You create the site project file, called `site.cpm`, in the `<your_inst_dir>/share/local/cdssetup/projmgr` directory when you want to specify default setup options for all the projects at your site. The directives in this file have precedence over the installation project file (`cds.cpm`) and the local project file (`<projectname>.cpm`) has precedence over the `site.cpm` file.

You can customize the default settings for all your projects by creating the `site.cpm` file. To create a `site.cpm` file, either use a copy of an existing project file, or create a dummy project and use its project file to define your site settings.

To create a site project file for all the projects at your site

1. Create a project in System Connectivity Manager.

For more information on creating a project, see [Creating a New Design Project](#) on page 84.

2. Choose *Project – Settings*.

The Setup dialog box appears.

3. In each tab of the Setup dialog box, specify the default setup information you want for all projects. For information about the setup options, click the *Help* button in the dialog box.

4. Click *OK* to close the Setup dialog box.

5. Exit System Connectivity Manager.

6. Copy the `<project_name>.cpm` file from the project directory to `<your_inst_dir>/share/local/cdssetup/projmgr`, where `<your_inst_dir>` is the directory in which you have installed Cadence tools.

7. In the `<your_inst_dir>/share/local/cdssetup/projmgr` directory, rename `<project_name>.cpm` to `site.cpm`.

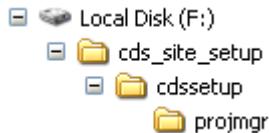
Creating a Custom Site Environment

The site.cpm File

If you do not place the `site.cpm` file in the `<your_inst_dir>/share/local/cdssetup/projmgr` directory, you must set a `CDS_SITE = <location>` environment variable that specifies the location of the site project file. The site location must have the following directory structure:

`cdssetup/projmgr/site.cpm`

For example, if you want to set your `CDS_SITE = f:\cds_site_setup`, you must create the following directory structure and place the `site.cpm` file in the `projmgr` directory:



If you have customized any of the following files and want the changed version to be available for all projects at your site, copy them to the location mentioned in the table below. This will

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ensure that the customized information is available even when you install a newer version of Cadence SPB software.

Files and Descriptions	Location	File Used By
cds.lib (lists libraries used in the project)	\$CDS_SITE/cdssetup	System Connectivity Manager Design Entry HDL
*.tpt files (customized report templates that you want to make available all users)	Copy from <your_install_dir>\share\cdssetup\tdd\custom_templates\ to \$CDS_SITE\cdssetup\tdd\custom_templates\	System Connectivity Manager
*.tcl files containing the procedures for custom DRCs tclIndex (Tcl index file for the .tcl files containing the procedures for custom DRCs) custom_drc.txt (file required for displaying custom DRCs in the in the <u>Design Rule Checks</u> tab of the <u>Setup</u> dialog box in System Connectivity Manager) (files related to custom DRCs)	Copy from <your_install_dir>\share\cdssetup\tdd\custom_rules\ to \$CDS_SITE\cdssetup\tdd\custom_rules\	System Connectivity Manager
bom.callouts (mechanical parts to be added in the BOM reports)	Copy from <your_inst_dir>/share/cdssetup/ to \$CDS_SITE/cdssetup/	Design Entry HDL
cdsinfo.tag (project-specific information, including the name of the data management system, if any, used in the project)	Copy from <your_inst_dir>/share/cdssetup/ to \$CDS_SITE/cdssetup/	Design Entry HDL

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Files and Descriptions	Location	File Used By
cdsprop.paf (information about properties)	Copy from <your_inst_dir>/share/cdssetup/ to \$CDS_SITE/cdssetup/	Design Entry HDL
cdsprop.tmf (information about text macros)	Copy from <your_inst_dir>/share/cdssetup/ to \$CDS_SITE/cdssetup/	Design Entry HDL
cjedectype.txt (compatible JEDEC types in the Variant Editor tool)	Copy from <your_inst_dir>/share/cdssetup/ to \$CDS_SITE/cdssetup/	Variant Editor
propflow.txt (the default property flow setup in Packager Setup)	Copy from <your_inst_dir>/share/cdssetup/ to \$CDS_SITE/cdssetup/	Design Entry HDL
template.bom (the default template for BOM reports)	Copy from <your_inst_dir>/share/cdssetup/ to \$CDS_SITE/cdssetup/	Design Entry HDL
xilfam.dat (mapping information between a Xilinx family and a specific library and architecture)	Copy from <your_inst_dir>/share/cdssetup/ to \$CDS_SITE/cdssetup/	System Connectivity Manager Design Entry HDL
xmodules.dat (modules that have to be excluded for cross-referencing and plotting)	Copy from <your_inst_dir>/share/cdssetup/ to \$CDS_SITE/cdssetup/	Design Entry HDL
concepthdl_key.txt (Design Entry HDL shortcut keys)	Copy from <your_inst_dir>/share/cdssetup/concept/ to \$CDS_SITE/cdssetup/concept/	Design Entry HDL
concepthdl_menu.txt (Design Entry HDL menus)	Copy from <your_inst_dir>/share/cdssetup/concept/ to \$CDS_SITE/cdssetup/concept/	Design Entry HDL

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Files and Descriptions	Location	File Used By
template.tsg (information related to the graphical attributes of the symbols and additional pin and symbol properties)	Copy from <your_inst_dir>/share/cdssetup/concept/genview/ to \$CDS_SITE/cdssetup/concept/genview/	Design Entry HDL
cref.dat (template options of CRefer)	Copy from <your_inst_dir>/share/cdssetup/creferhdl/to \$CDS_SITE/cdssetup/creferhdl/	Design Entry HDL
allegro.ilinit (SKILL initialization file) Note: Copy the file as allegro.ilinit only if same initialization file is to be used by all programs. If the customization is for one program, copy example.ilinit as <programName>.ilinit	Copy <your_inst_dir>/share/local pcb/skill/example.ilinit to \$CDS_SITE/pcb/text/allegro.ilinit	Allegro PCB
cuimenus folder (updated PCB Editor menus)	Copy from <your_inst_dir>/share/pcb/text/ to \$CDS_SITE/pcb/text/	Allegro PCB
env (paths to PCB Editor libraries and other site settings for PCB Editor)	Copy from <your_inst_dir>/pcb/text/ to \$CDS_SITE/pcb/text/	Allegro PCB
forms folder (all forms called from Allegro SKILL code)	Copy from <your_inst_dir>/share/pcb/text/ to \$CDS_SITE/pcb/text/	Allegro PCB
nclegend folder (PCB Editor templates from NCDRIII legend)	Copy from <your_inst_dir>/share/pcb/text/ to \$CDS_SITE/pcb/text/	Allegro PCB
skill folder (custom Allegro SKILL code)	Place at \$CDS_SITE/pcb/text/	Allegro PCB

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Files and Descriptions	Location	File Used By
views folder (Allegro extract command files)	Copy from <your_inst_dir>/share pcb/text/ to \$CDS_SITE pcb/text/	Allegro PCB

Note: The `cdsprop.txt` file need not be copied as you should not be modifying this file.

Installation Project File

The installation project file, called `cds.cpm`, is shipped by Cadence and is in the `<your_inst_dir>/share/cdssetup/projmgr` directory. The `cds.cpm` file contains default setup directives for all projects and tools. System Connectivity Manager obtains defaults from this file for setup options that are not defined in the `<projectname>.cpm` or `site.cpm` files. Do not modify this file. If you want to change the defaults for a set of projects, create a site project file (`site.cpm`).

The `cds.lib` File

System Connectivity Manager is a by-reference design editor. This means that System Connectivity Manager references all parts in the design from various libraries that reside at the reference or project area.

The `cds.lib` file is the library definition file that defines all the libraries used in your design and maps them to their physical locations. The contents of a typical `cds.lib` file is given below:

```
DEFINE 54alsttl ../../library/54alsttl
DEFINE 54fact ../../library/54fact
DEFINE tutorial_lib worklib
DEFINE local_lib local_lib
INCLUDE $CHDL_LIB_INST_DIR/share/cdssetup/cds.lib
```

- The `DEFINE` command defines a library. The library name is specified first, followed by the path to the library directory. The path can be absolute or relative to the location of the `cds.lib` file. Except for the path names, the `cds.lib` file is not case sensitive.

For example, the syntax:

```
DEFINE analog c:/designs/reference/ref_lib/analog
```

defines the `analog` library located at `c:/designs/reference/ref_lib/` in the `cds.lib` file.

- The `INCLUDE` command loads another library definition (`cds.lib`) file that defines the libraries you want to setup for your project. For example, you can include a `cds.lib` file that defines a list of company-generated libraries, or you can include the `cds.lib` file being used in another project.

For example, the syntax:

```
INCLUDE c:/designs/reference/ref_lib/cds.lib
```

includes all the libraries defined in the `cds.lib` file located at `c:/designs/reference/ref_lib/` in the `cds.lib` file for the current project.

Note the following:

- Use lowercase library names only in the `cds.lib` file. Do not use mixed or uppercase names, or special characters except the underscore character.
- Use forward slashes in paths as they will work on Windows, UNIX and Linux platforms. Backward slashes and absolute paths will need to be modified if the project is transferred between Windows, UNIX and Linux platforms.

For more information on the `cds.lib` file, see the *Design Entry HDL Libraries Reference*.

Setting Up the Project

To setup the options for the project

1. Choose *Project – Settings*.

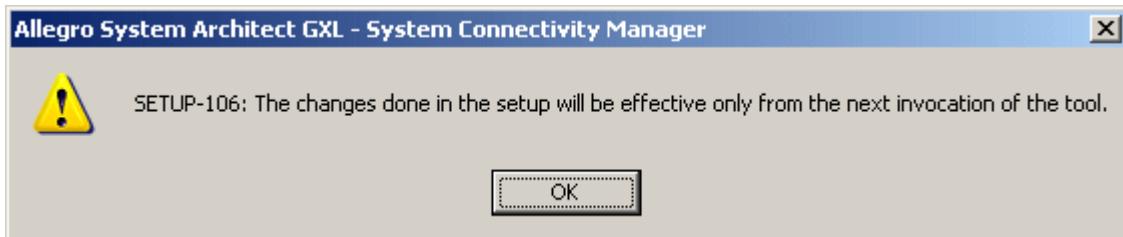
The Setup dialog box appears.

2. In each tab of the Setup dialog box, specify the setup options for the project.

For information about the setup options in each tab of the Setup dialog box, see [Setup](#).

3. Click *OK* to save the changes and close the Setup dialog box.

The following message box appears if a change in a tab in the Setup dialog box will be effective only if you reopen the project in System Connectivity Manager.



If the above message box appears, do the following:

- a. Exit System Connectivity Manager.
- b. Reopen the project in System Connectivity Manager.

Setting Up the Vector Notation for a Project

In System Connectivity Manager, for naming vector pins and signals, you can either use the angle (<>) brackets or the square ([]) brackets. By default, angle brackets are used for naming vectors.

To change the vector notation for a project, complete the following steps.

1. Choose *Project – Settings*.
2. Select *General*.
3. In the Show Vector Using group box,
 - select the [] option, to use square brackets as the vector notation.
 - select <> to use angle brackets as the vector notation.
4. Click OK.

Note: These settings are not reflected in the current session of System Connectivity Manager. For this, exit System Connectivity Manager and launch System Connectivity Manager again.



Changing the vector notation does not change the physical net names for the existing nets.

When you change the vector notation for a project, the signal names and the pin names of a vector signal or a vector pin are modified to use the specified vector notation. However, there is no change in the physical net name of an existing net. For example, if a design has vector signal $a<3..1>$, the individual bits $a<3>$, $a<2>$, and $a<1>$ have physical net names as $A<3>$, $A<2>$, and $A<1>$, respectively. If you now change the vector notation such that square brackets are used to represent vectors, the signal names will change to $A[3]$, $A[2]$, and $A[1]$, respectively. However, the physical net names for these signals will still remain $A<3>$, $A<2>$, and $A<1>$.

Name	Phys Name
*	*
ba<0>	BA<0>
ba<1>	BA<1>
ba<2>	BA<2>
ba<3>	BA<3>
ba<4>	BA<4>
ba<5>	BA<5>
ba<6>	BA<6>
ba<7>	BA<7>
BNC1	BNC1

Signal names and physical net names with $<>$ as the vector notation

Name	Phys Name
*	*
ba[0]	BA<0>
ba[1]	BA<1>
ba[2]	BA<2>
ba[3]	BA<3>
ba[4]	BA<4>
ba[5]	BA<5>
ba[6]	BA<6>
ba[7]	BA<7>

Signal names and physical net names when vector notation changed to []

Setting Differential Pair Naming Convention

In System Connectivity Manager, you can modify the setup options to ensure that the component pins names in a particular format are identified as differential pair pins. Similarly, you can also create differential pair signals using two scalar signals or two vector signal of the same width. In both the cases, the names for the differential pairs are auto-generated by System Connectivity Manager. However, you can use the setup options to specify the prefix values that want to be used for differential pair pins and differential pair signals.

To specify the differential pair setup options, complete the following steps.

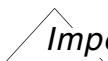
1. Choose *Project – Settings*.
2. In the Setup Dialog box, select *Differential Pairs*.
3. In the Differential Pairs page, specify the formats used for naming differential pair pins in the Formats for Naming Differential Pair Pins grid.

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- a. In the Negative Pin column, specify the characters used for naming the negative pin in the differential pair.
- b. In the Location column specify whether the characters mentioned in Negative Pin column are added as prefixes or suffixes to the pin name.
- c. In the Positive Pin column, specify the characters used for naming the positive pin in the differential pair.
- d. In the Location column specify whether the characters mentioned in the Positive Pin column are added as prefixes or suffixes to the pin name.

For example, to ensure that the component pins add_LOW and add_HIGH are treated as differential pair pins, enter _LOW in the Negative Pin column, _HIGH in the Positive Pin column, and in the Location column, select SUFFIX from the Location drop-down list for both pins. This will ensure that any two pins with the same name and _LOW and _HIGH as suffixes are displayed as differential pair pins in Component Connectivity Details pane.



Important
Regardless of the pin naming formats specified in the setup, you cannot create differential pairs using power pins.

4. Similarly, you can also specify the naming convention used for naming differential pair signals in the Differential Pair Signals Syntax.

Note: The signal naming convention specified here is used for naming member nets of a differential pair created in SCM.

5. In the Prefix section, specify the text that is to be prefixed while generating the names for differential pair of pins and differential pair of signals.

The prefix specified for the differential pair signals is used in the following situations.

- While adding differential pair signals to a design using the Add Signal dialog box.
- While creating a differential pair by using existing signals in the Signal List pane.

6. Click *OK* to save your settings and to close the Setup dialog box.

Setting Up Libraries for a Project

To setup libraries for a project

1. Choose *Project – Settings*.

The Setup dialog box appears.

2. Select the *Libraries* tab.

If the library you want to use is not listed in the *Available Libraries* list or the *Project Libraries* list, do the following:

- a. Open the `cds.lib` file located in your project directory in a text editor.
- b. Add the definition for the library you want to use for your project.

For more information on adding a definition for a library in the `cds.lib` file, see [The `cds.lib` File](#) on page 100.

- c. Exit System Connectivity Manager.
- d. Reopen the project in System Connectivity Manager.
- e. Choose *Project – Settings*.

The Setup dialog box appears.

- f. Select the *Libraries* tab.

The new libraries that were defined or included in the `cds.lib` file for the project are displayed in the *Available Libraries* list.

3. Modify the *Project Libraries* list.

- To add a library, select the library in the *Available Libraries* list and click *Add*.
- To add all the libraries in the *Available Libraries* list, click *Add All*.
- To remove a library, select the library in the *Project Libraries* list and click *Remove*.
- To remove all the libraries in the *Project Libraries* list, click *Remove All*.

Note: You can only add components from the libraries that are listed in the *Project Libraries* list.

4. Choose the search order for the project libraries. The order in which the libraries are listed in the *Project Libraries* list determines their search order.

- To move a library one level up, select the library and then click *Up*.
 - To move a library one level down, select the library and then click *Down*.
5. Click *OK*.

The following message box appears.



6. Exit System Connectivity Manager.
7. Reopen the project in System Connectivity Manager.

Setting Up Physical Part Table Files for a Project

The Physical Part Table (.ptf) file stores the packaging properties for a part in the library. This file contains information about parts such as package types, manufacturers, part numbers and any custom properties. Each physical part must have an entry in the .ptf file in order to package properly. Part table files can be located in the `part_table` view of cells in a library or outside the library structure.

To access the information contained in part table files, you must include them in your project. By default, the part table files located in the `part_table` view of cells in a library are included in your project. If a part table file is located outside the `part_table` view of cells in a library, you must include the file in your project.

You can add either .ptf files directly or directories that contain .ptf files. For example, if the `lsttl` directory contains the `lsttl.ptf` file, you can add either the complete path to the `lsttl.ptf` file or just the path to the `lsttl` directory. When you add a directory, all the .ptf files in that directory are added to the project. You can then exclude some of the .ptf files if you do not want them in the project.

To setup Physical Part Table files for a project

1. Open the project.
2. Choose *Project – Settings*.

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The Setup dialog box appears.

3. Select the *Physical Part Table* tab.
4. To add cell-level .ptf files to your project, select the *Use Cell-Level Physical Part Table Files* check box. All the .ptf files contained in the part_table view of the cells will be read by System Connectivity Manager.
5. To add other Physical Part Table files,
 - a. Under *Physical Part Table Files*, click *Add*.
The *Add Physical Part Table* dialog box appears.
 - b. Type the name and the path of the .ptf file or the directory containing the .ptf files. To add more than one path, separate each path with a space.
—or—
To add a file, click *File* and select the .ptf file in the *Choose Physical Part Table Files* dialog box. (To select more than one file, select the first one, then press *CTRL* and select the others.)
To add a directory, click *Directory* and select a directory in the *Choose Directory* dialog box.
 - c. Click *OK*.
6. To exclude any unwanted .ptf files contained in the directories you have added, do one of the following:
 - Under *Exclude Part Tables*, click *Add* and enter the name and path of the .ptf file you want to exclude from your project. Repeat this step for all the files you want to exclude.
 - Under *Include Part Tables*, click *Add* and enter the name and path of the .ptf file you want to include in your project. Repeat this step for all the files you want to include.
 - To remove a Physical Part Table file or directory, select the file and click *Remove*.
 - Select the *Merge Physical Part Table Files* check box to merge the information in all included Physical Part Table files.
 - Select the *Perform Case Sensitive Row Match* check box to perform a case-sensitive match of key properties for a part in the physical part table files.
7. Click *Apply* to save your changes, or *OK* to save your changes and close the Setup dialog box.

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Project Creation and Setup

Working with Components

The chapter describes the procedures for working with components in the design. The topics covered in this chapter are:

- [Adding Components](#) on page 109
- [Modifying Components](#) on page 111
- [Replacing Components](#) on page 112
- [Copying and Pasting Components](#) on page 129
- [Modifying Component Instance Names](#) on page 130
- [Modifying Component Reference Designators](#) on page 132
- [Working with Power Pins and NC Pins of Components](#) on page 133
- [Swapping Pins Across Functions of a Component](#) on page 142
- [Deleting Components](#) on page 143

Adding Components

You can use Part Information Manager to add components in your design. For more information on using Part Information Manager, see *Part Information Manager User Guide*.

Note the following:

- You can add components from the libraries that are listed in the *Project Libraries* list in the [Libraries](#) tab of the [Setup](#) dialog box. For more information on setting up libraries for your project, see [Setting Up Libraries for a Project](#) on page 103.
- You can also access part information from the Allegro EDM component server. This allows you access to a richer set of data and an accessible-from-anywhere database of components. To identify the Allegro EDM component server of Part Information Manager,

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Working with Components

in the START_COMPBROWSER section of the site.cpm or project.cpm, specify the following two directives:

- Online_Mode 'TRUE'
- server_url <server_URL>

where server_url points to the Allegro EDM database. For example, `http://edmserver:9999`.

To access symbols, the cds.lib file in your design project should point to the Allegro EDM server libraries, and the PPT directive in the Global section of the .cpm file should point to the server PTF to access parts.

Local cells/blocks other than those in the design library are not available in the Allegro EDM mode. To access cells and blocks from your local libraries, you can switch to the offline mode by selecting *File — Switch to Offline* or by clicking the Switch to Offline button () in Allegro EDM Part Information Manager.

For more details about the Allegro EDM and standard (offline) modes, see the Part Information Manager Modes section of *Part Information Manager User Guide*.

- Do not add components with mixed or uppercase names, or components whose names have special characters except the underscore character.
- Do not add components whose symbol or physical part table (.ptf) file has properties with null (empty) values. Such components will not be packaged in System Connectivity Manager. If you add such components in the design, packaging errors are reported in the Violations window for the components.
- It is recommended that you add split parts as a package.

To add a component

1. Do one of the following:

- Choose *Design – Add Component*.
- Click  on the toolbar.

Part Information Manager appears.

2. Search for the component you want to add.

For information on how to search for components, see *Part Information Manager User Guide*.

3. In the *Search Results* pane, click the row corresponding to the physical part you want to add.

The symbol and footprint for the component are displayed in the *<Part Name>* tab.

4. Do one of the following:

- Select the  option if you want to add a symbol version of the component and select the version of the symbol you want to add in the version drop-down list.

Note: The number of instances comprising the component is equal to the number of symbol versions for the component.

- Select the  option if you want to add the component as a package (an instance that represents the complete component).

5. In the *Instances* field, enter the number of instances of the component you want to add in the design.

6. To add the component, do one of the following:

- Click the *Add* button.
- Double-click on the component in the *Search Results* pane.
- Select the component in the *Search Results* pane, right-click and choose *Add to Design* from the pop-up menu.

The component is added in the design and displayed in the Component List. For more information on using the Component List, see [Component List](#) on page 48.

Note: By default you cannot add chips view if a part has multiple primitives in chips.prt. You need to set the following environment variable to add parts that have multiple primitives in chips prt:

```
DS_SPECIAL_CONNECTOR_SUPPORT = TRUE.
```

Modifying Components

You can modify a component to modify its physical properties.

To modify a component

1. Select the component whose physical properties you want to modify in the Component List and choose *Object – Modify Component*.

The Modify Component dialog box appears.

Note: To select more than one instance of the same component, press the *Shift* or *Ctrl* key and click on the components you want to modify. You can only select multiple instances of the same component and modify them at the same time. You cannot select two different components and modify them at the same time.

2. Select the desired row of physical properties to attach to the component you want to modify.
3. Click *Modify*.

Replacing Components

You can replace components in your design with other components. System Connectivity Manager lets you:

- Replace a component in your design with another component.
For more information, see [Replacing a Component with another Component](#) on page 112.
- Replace all the instances of a component in your design with another component using Global Replace.
For more information, see [Replacing all instances of components in the design with other components using Global Replace](#) on page 122.



Undo operations are not supported after you have replaced a component.

Note: You cannot replace a hierarchical block in your design with another hierarchical block or component. For more information on working with hierarchical blocks, see [Chapter 13, “Working with Hierarchical Designs.”](#)

Replacing a Component with another Component

To replace a component in the design with another component

1. Setup the options for replacing components in the [Component Replace](#) tab of the [Setup](#) dialog box.

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Working with Components

2. In the Component List, select the component you want to replace and choose *Object – Replace Component*.

Part Information Manager appears. For more information on using Part Information Manager, see *Part Information Manager User Guide*.

Note: To select more than one instance of the same component in the Component List, press the *Shift* or *Ctrl* key and click on the components you want to replace. You can only select multiple instances of the same component and replace them at the same time. You cannot select two different components and replace them at the same time. For example, you can replace two instances of the `ls04` component at the same time. However, you cannot replace an instance of the `ls01` component and another instance of the `ls04` component at the same time.

3. Search for the component you want to use to replace the component in the design.

For information on how to search for components, see *Part Information Manager User Guide*.

4. In the *Search Results* pane, click the row corresponding to the physical part you want to use to replace the component in the design.

The symbol and footprint for the component are displayed in the *<Part Name>* tab.

5. Do one of the following:

- In the version drop-down list select a symbol version of the component and select the  option, if you want to replace the component in the design with that symbol version of the new component.

For example, if you want to replace the component in the design with the symbol version 3 of the new component, select 3 in the version drop-down list and select the  option.

- Select the  option if you want to add the component as a package (an instance that represents the complete component) to replace the component in the design.

6. To replace the component, do one of the following:

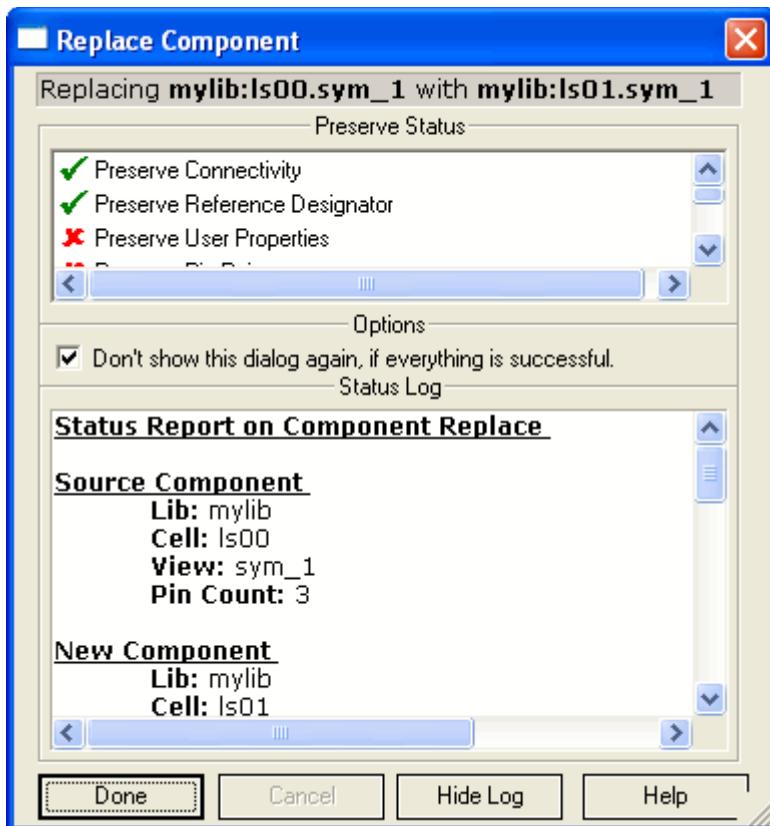
- Click the *Replace* button.
- In the *Search Results* pane, double-click the row corresponding to the physical part you want to use to replace the component in the design.
- In the *Search Results* pane, select the row corresponding to the physical part you want to use to replace the component in the design, right-click and choose *Replace* from the pop-up menu.

7. Click *Replace*.

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Working with Components

- If there is no mismatch in the pin names and pin numbers of the existing component (the component existing in the design) and the target component (the new component), the Replace Component dialog box appears displaying whether the component replace preserve options you selected in the Component Replace tab of the Setup dialog box will be honored when you replace the component. Click *Done* to replace the component.



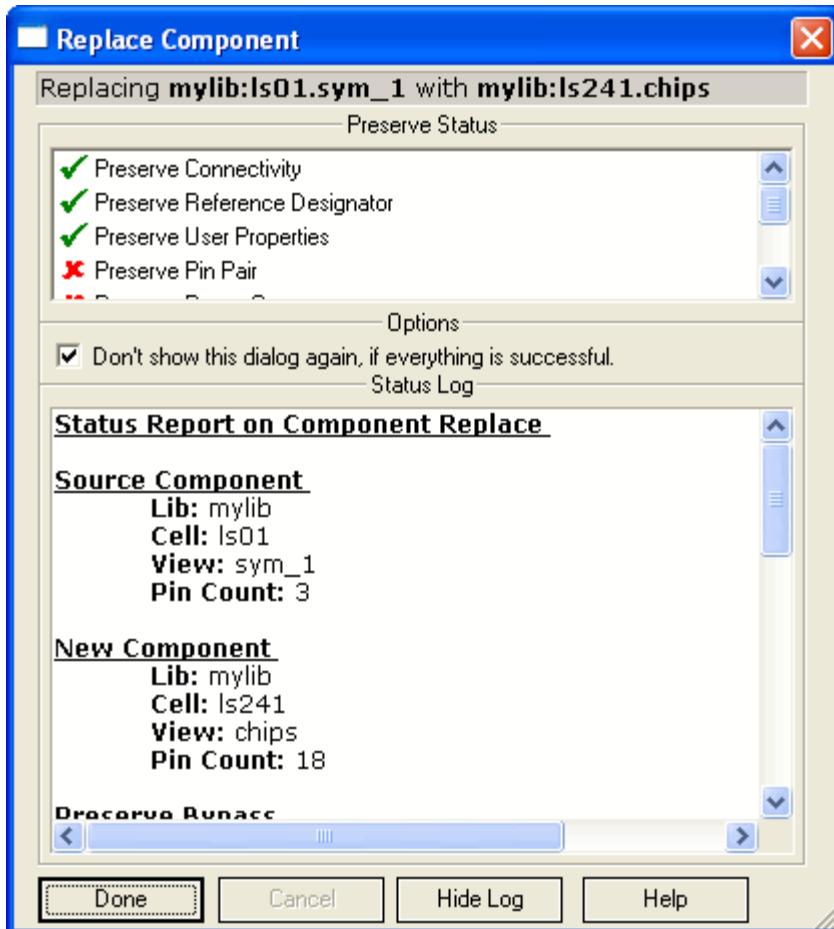
- If there is a mismatch in the pin names or pin numbers of the existing component (the component existing in the design) and the target component (the new component), the Component Replace dialog box appears.
 - Resolve the connectivity and property differences between the existing component and the target component in the Component Replace dialog box.
For more information on using the Component Replace dialog box, see [Using the Component Replace Dialog Box](#) on page 115.
 - Click *Replace*.

Note: To cancel the replace operation, click *Cancel*.

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The Replace Component dialog box appears displaying whether the component replace preserve options you selected in the Component Replace tab of the Setup dialog box will be honored when you replace the component.



8. Click *Done* to close the Replace Component dialog box.

Using the Component Replace Dialog Box

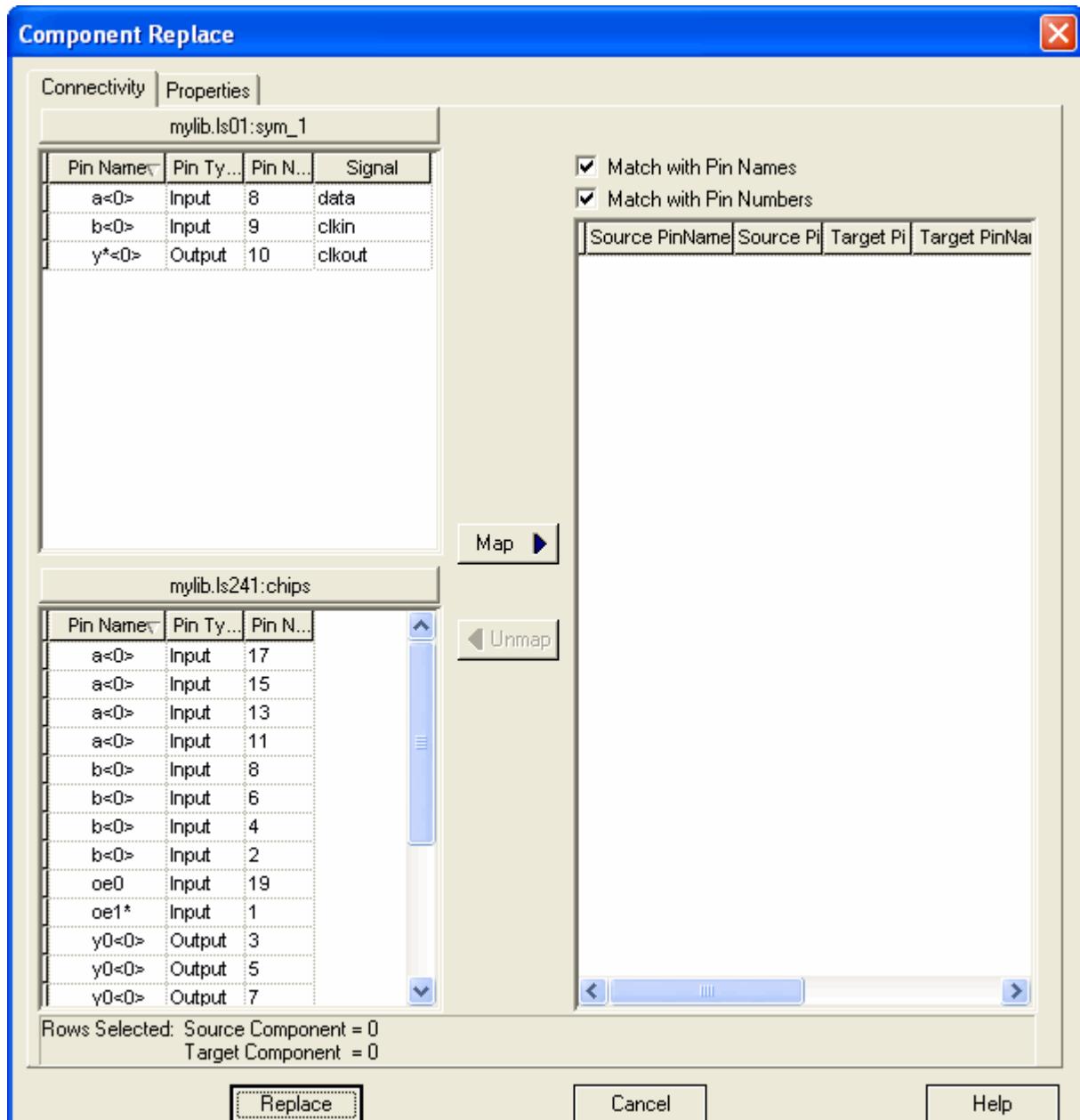
The Component Replace dialog box appears when you are replacing a component in the design with another component, if there is a mismatch in the pin names or pin numbers of the existing component (the component existing in the design) and the target component (the new component).

This dialog box lets you resolve the connectivity and property differences between the existing component and the target component.

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Working with Components

1. In the Connectivity tab, resolve the connectivity differences between the existing component and the target component.



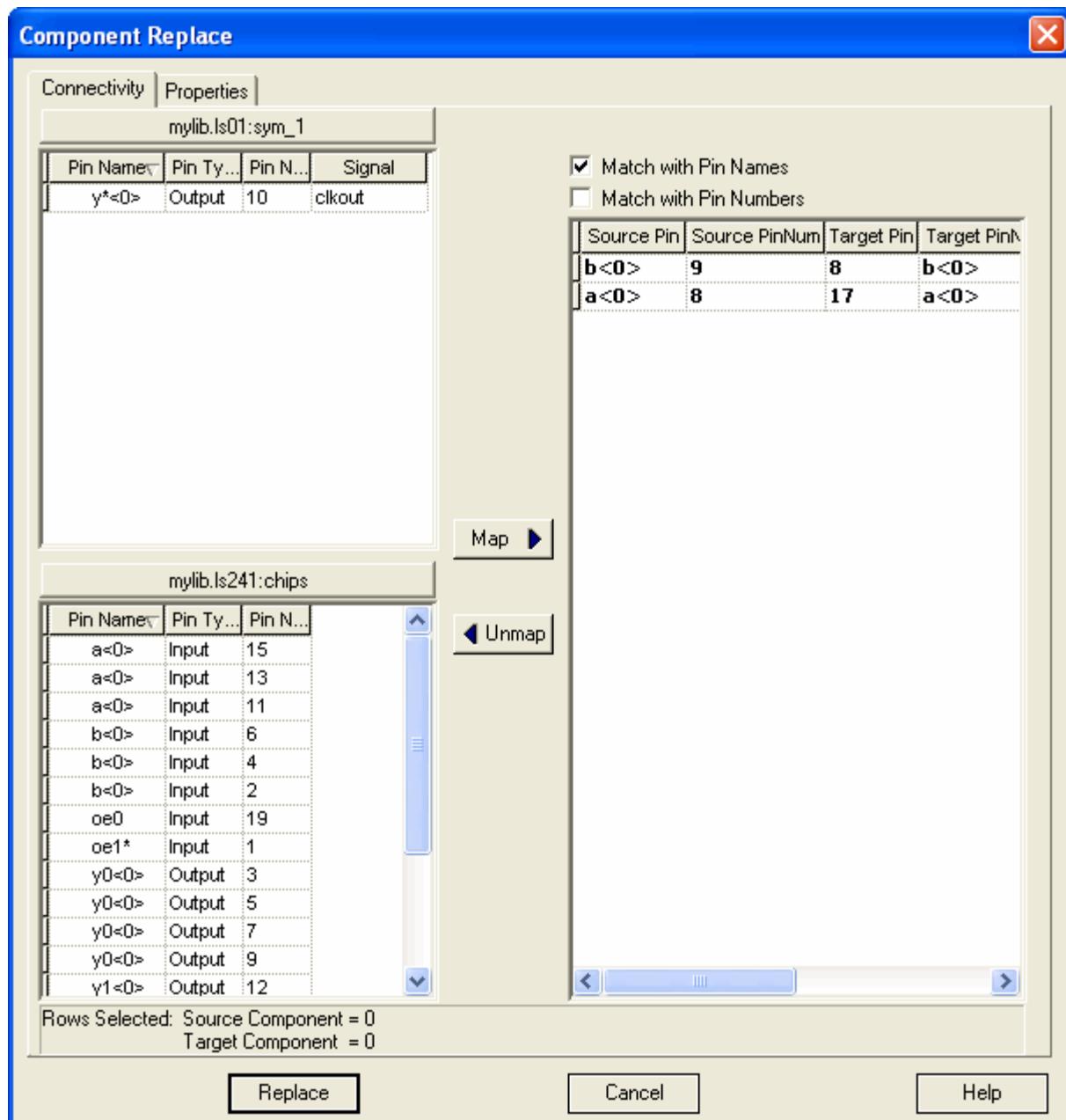
In the above figure, both the *Match with Pin Names* and *Match with Pin Numbers* check boxes are selected. This means that a signal that is connected to a pin on the existing component will be automatically connected to a pin on the target component if the target component has a pin with the same name and number. For example, in the above figure, pin a<0> with the pin number 8 on the existing component is connected to

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Working with Components

the signal data. This signal will get automatically connected to a pin on the target component that has the pin name $a<0>$ and the pin number 8.

- If only the *Match with Pin Names* check box is selected, connectivity will be automatically matched based on pin names. This means that a signal that is connected to a pin on the existing component will be automatically connected to a pin on the target component, if the target component has a pin with the same name.

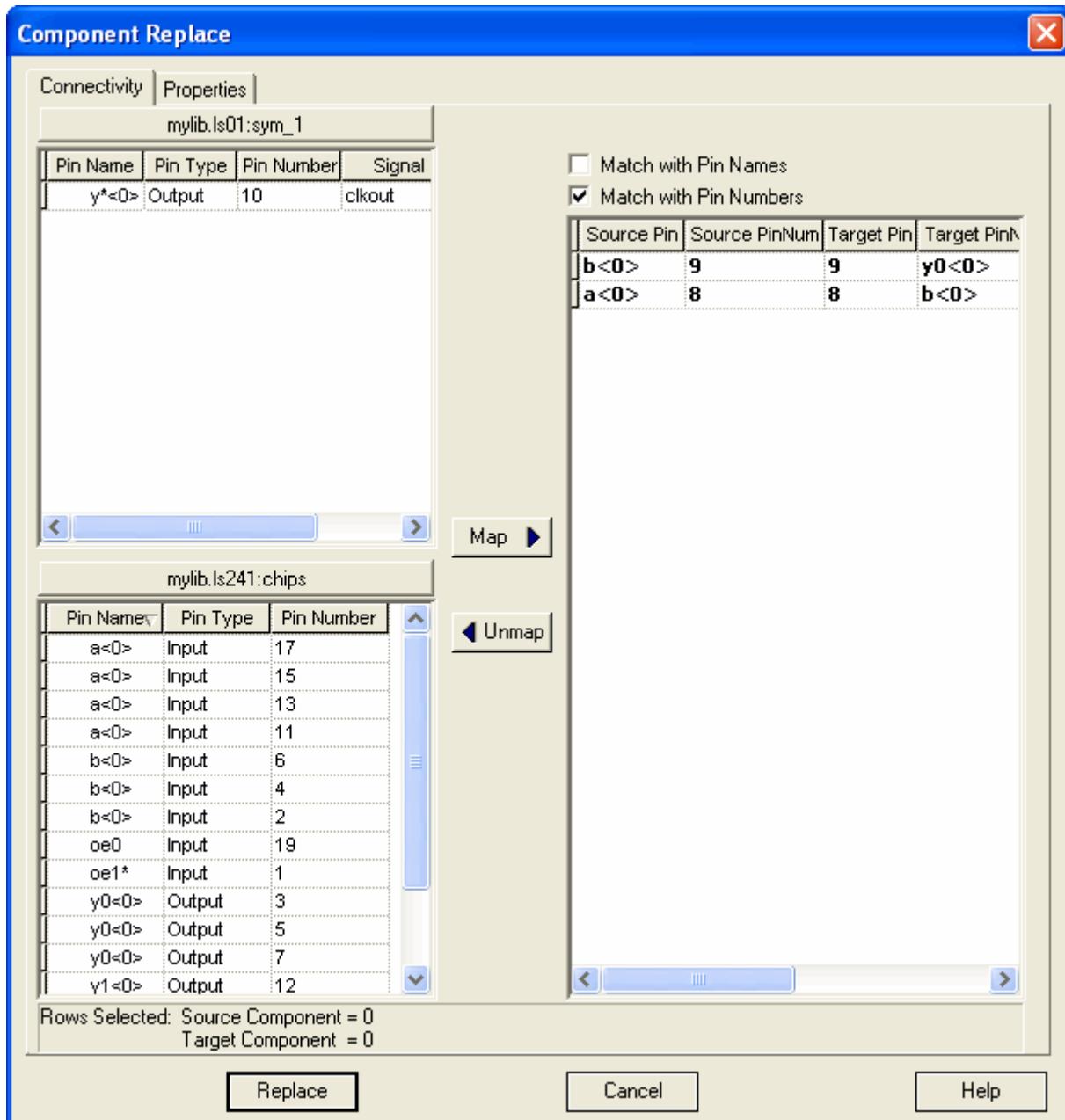


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Working with Components

In the above figure, the signals connected to the pins $a<0>$ and $b<0>$ on the existing component are automatically connected to the pins $a<0>$ and $b<0>$ on the target component.

- If only the *Match with Pin Numbers* check box is selected, connectivity will be matched based on pin numbers. This means that a signal that is connected to a pin on the existing component will be automatically connected to a pin on the target component, if the target component has a pin with the same number.



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In the above figure, the signals connected to the pins with the numbers 8 and 9 on the existing component are automatically connected to the pins with the numbers 8 and 9 on the target component.

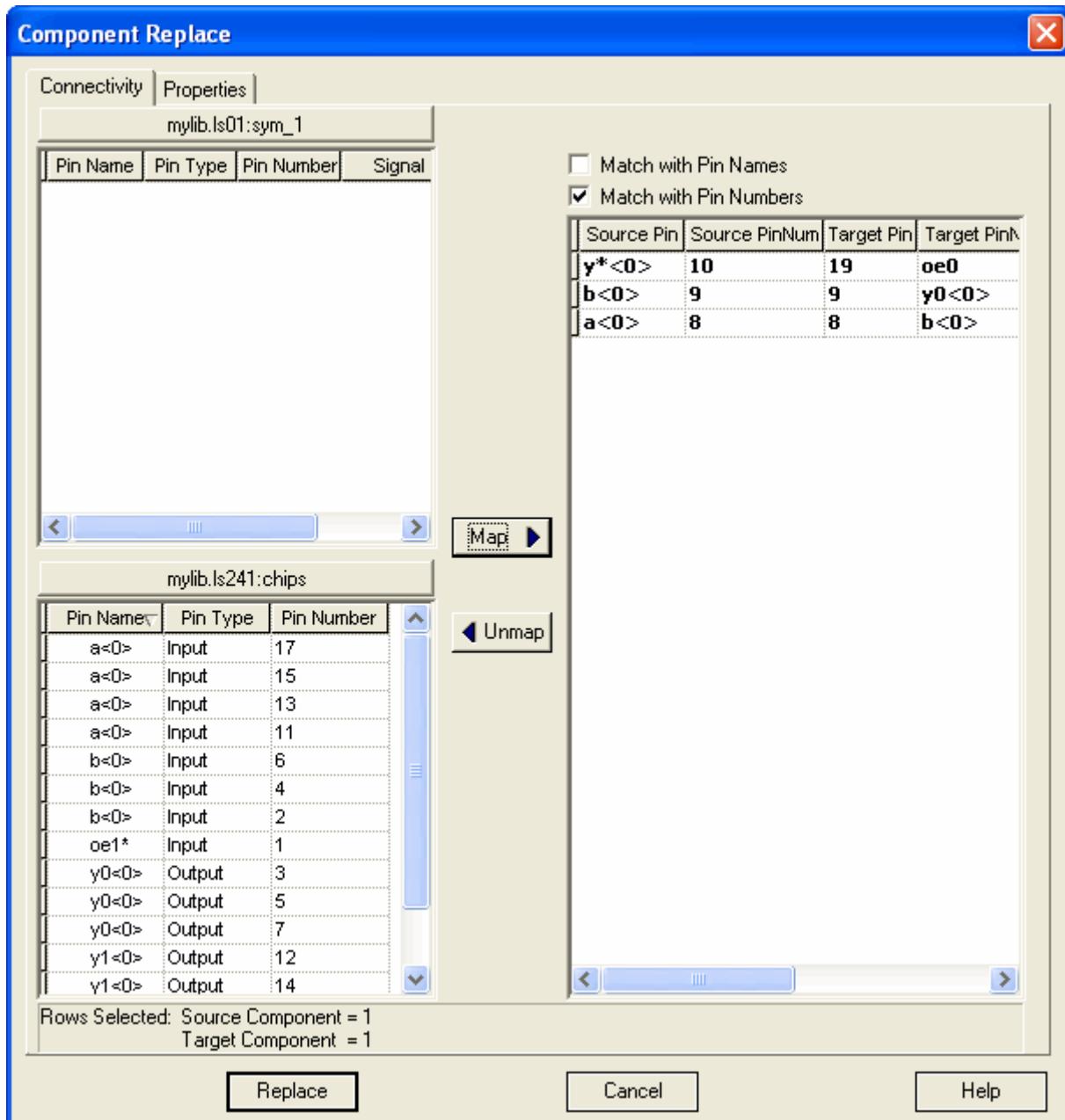
You can also manually resolve the connectivity differences between the existing component and the target component by doing the following:

- a. Select a pin on the existing component that is connected to a signal.
- b. Select the pin on the target component to which you want the signal to be connected when the existing component is replaced with the target component.
- c. Click the *Map* button.

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In the figure below, the pin $y^*<0>$ on the existing component is mapped to the pin $oe0$ on the target component.

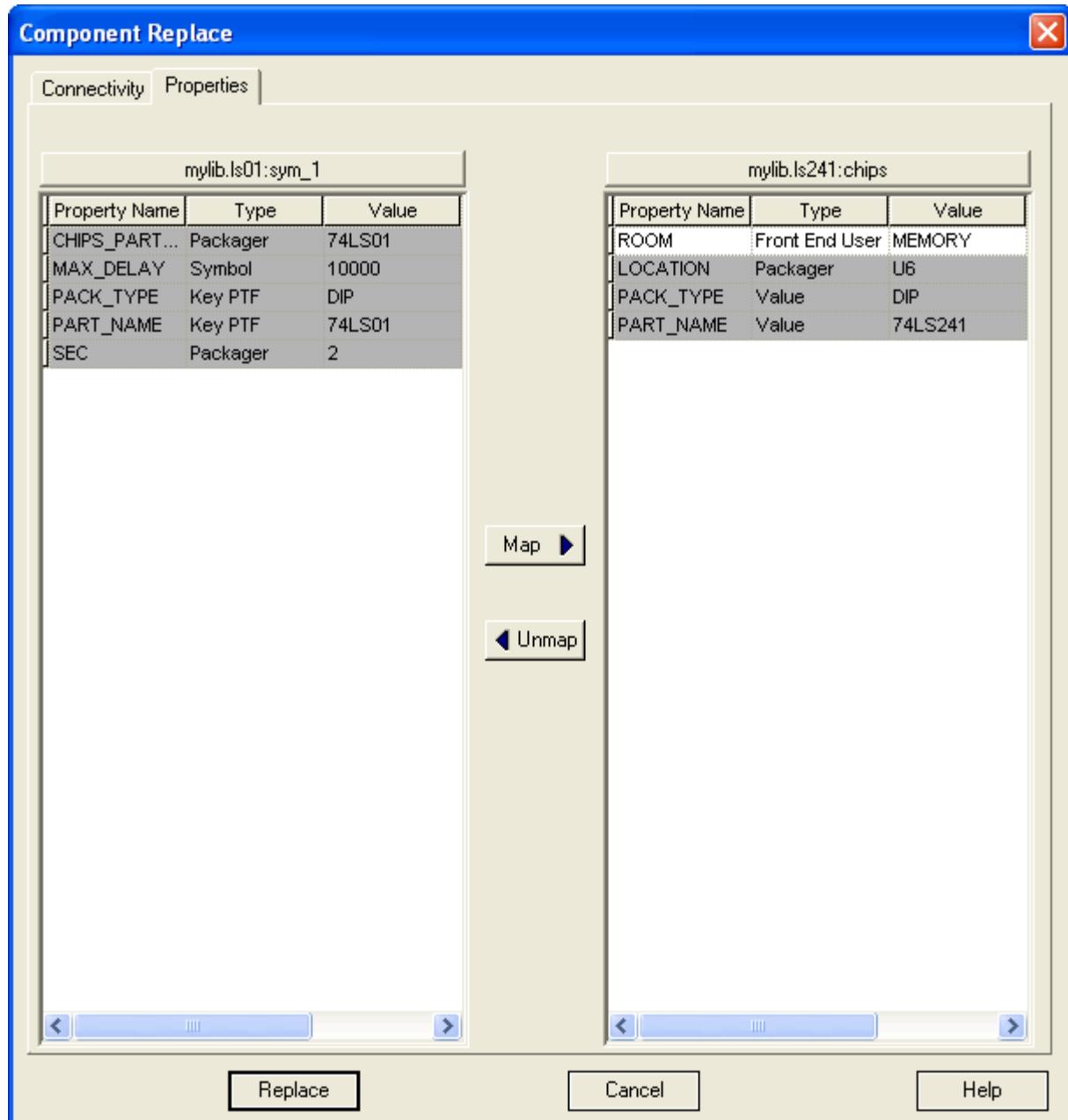


Note: To unmap the pins that were manually or automatically mapped, select the pin in the list on the right side and click the *Unmap* button.

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2. Click the Properties tab to resolve the user property (a property added by you on components in System Connectivity Manager) differences between the existing component and the target component.



The properties on the existing component are displayed on the left side. The properties on the target component are displayed on the right side. In the above figure, the user property `ROOM` added on the existing component (`ls01`) is automatically added on the

target component (ls241) because the *Preserve User Properties* check box in the Component Replace tab of the Setup dialog box is selected.

To add a user property from the existing component to the target component, do the following:

- a. Select the user property on the existing component.
- b. Click the *Map* button.

Note: If you do not want to add a user property on the target component, select the user property on the target component and click the *Unmap* button.

Replacing all instances of components in the design with other components using Global Replace

You can use the Global Replace dialog box to replace all instances of a component in your design with another component.

Note the following:

- Global Replace will replace components in all the spreadsheet and Verilog blocks in a hierarchical design. However, Global Replace will not replace components in schematic blocks and components in read-only blocks. To replace components in schematic blocks, open the block in Design Entry HDL and perform Global Replace in Design Entry HDL. For more information on working with read-only blocks, see Working with Read-Only Blocks in your Design on page 380.
- You cannot use the Global Replace dialog box to replace associated components such as terminations, bypass capacitors, and pullups and pulldowns in the design. You must manually modify the associated components in the design. For more information on working with associated components, see Chapter 11, “Working with Associated Components.”



Exercise caution when performing global replace because global replace impacts the connectivity and property information on component instances across all levels of a hierarchical design.

To replace all instances of a component in the design with another component

1. Setup the options for replacing components in the Component Replace tab of the Setup dialog box.

2. Choose *Project – Global Replace*.

The Global Replace dialog box appears.

3. Select the Components tab.

4. Specify the name of the library, cell, and view of the component you want to replace.

- a.** In the *Library* field, enter the name of the library in which the component exists.
- b.** In the *Cell* field, enter the name of the component you want to replace in the design.
For example, enter `1s04` to replace all instances of the component `1s04` in your design.
- c.** In the *View* field, enter the name of the view.
 - Enter the name of the view for a symbol version if you want to replace only those instances of the component that are instantiated using that symbol version of the component.
For example, enter `sym_1`, if you want to replace only those instances of the component that are instantiated using symbol version 1 of the component.
 - Enter `chips` to replace only those instances of the component that are added as a package (an instance that represents the complete component) in the design.

You can also use Part Information Manager to specify the name of the library, cell, and view of the component you want to replace by doing the following:

- a.** Click the *Select* button.

Part Information Manager appears.

- b.** In the *Library* list, select the library in which the component you want to replace exists.
- c.** In the *Cells* list, select the component you want to replace.
- d.** In the *Search Results* pane, click the row corresponding to the physical part you want to replace.

The symbol and footprint for the component are displayed in the *Part <Name>* tab.

- e.** Do one of the following:

- In the version drop-down list select a symbol version of the component and select the  option, if you want to replace only instances of the component that are instantiated using that symbol version of the component.

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For example, if you want to replace only the instances of the component that are instantiated using symbol version 3 of the component, select 3 in the version drop-down list and select the  option.

- Select the  option if you want to replace only instances of the component that are added as a package in the design.

f. Click *Replace*.

The name of the library, cell, and view of the component you want to replace are displayed in the Global Replace dialog box.

5. Select the component you want to use to replace the component in the design by doing the following:

a. Click the *Select* button.

Part Information Manager appears.

- b. In the *Library* list, select the library in which the component you want to use to replace the component in the design exists.**
- c. In the *Cells* list, select the component you want to use to replace the component in the design.**
- d. In the *Search Results* pane, click the row corresponding to the physical part you want to use when replacing the component.**

The symbol and footprint for the component are displayed in the *Part <Name>* tab.

e. Do one of the following:

- In the version drop-down list select a symbol version of the component and select the  option, if you want to replace the component in the design with that symbol version of the new component.

For example, if you want to replace the component in the design with the symbol version 3 of the new component, select 3 in the version drop-down list and select the  option.

- Select the  option if you want to replace the component in the design with a package version of the new component.

f. Click *Replace*.

The name of the library, cell, and view of the component you want to use to replace the component in the design are displayed in the Global Replace dialog box.

6. Select the *Show Advanced Options* check box if you want to:

- Replace only instances of a component that have specific properties.
 - Add properties on the component that replaces the component in the design.
- a. In the *Search with Properties* list, specify the name and value of the properties you want to be searched.

In the *Property Name* column, click on a row and select a property from the drop-down list or enter the property name. Enter the value of the property in the *Property Value* column.

You can use the * (asterisk) and ? wildcard characters to perform the search.

To add rows, click . To delete a row, select the row and click .

- b. In the *Add these Properties* list, specify the name and value of the properties you want to add on the component that replaces the component in the design.

In the *Property Name* column, click on a row and select a property from the drop-down list or enter the property name. Enter the value of the property in the *Property Value* column.

Note: If you specify a property that already exists on instances of the component in the design that you are going to replace, the property value on the instances will be preserved on the new instances if the *Preserve User Properties* check box in the Component Replace tab of the Setup dialog box is selected. For example, if the instances of a component in the design have the property `ROOM` with the value `CPU` and you specify the `ROOM` property with the value `MEMORY` in the *Add these Properties* list, after you perform global replace, the new instances will continue to have the property `ROOM` with the value `CPU`, if the *Preserve User Properties* check box in the Component Replace tab of the Setup dialog box is selected.

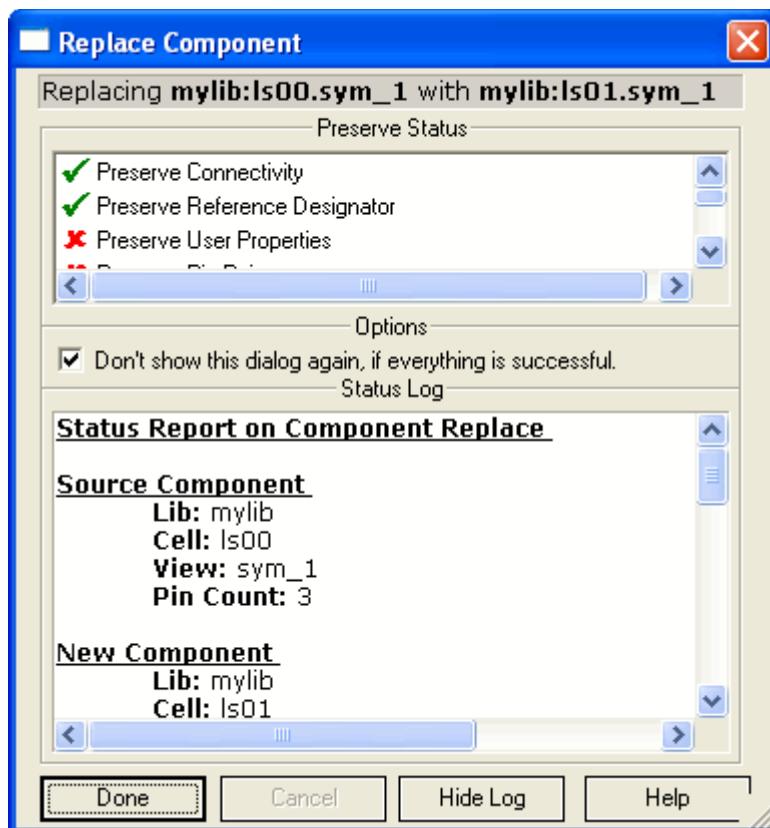
Important

Ensure that the *Preserve User Properties* check box in the Component Replace tab of the Setup dialog box is selected before performing global replace for components in the design. If the *Preserve User Properties* check box is not selected, the user properties (properties you added on the component in System Connectivity Manager) on the instances of the component you are replacing will not be copied over to the new instances of the component.

To add rows, click . To delete a row, select the row and click .

7. Click *Replace*.

- ❑ If there is no mismatch in the pin names and pin numbers of the existing component (the component existing in the design) and the target component (the new component), the Replace Component dialog box appears displaying whether the component replace preserve options you selected in the Component Replace tab of the Setup dialog box will be honored when you replace the components. Click *Done* to replace the component.



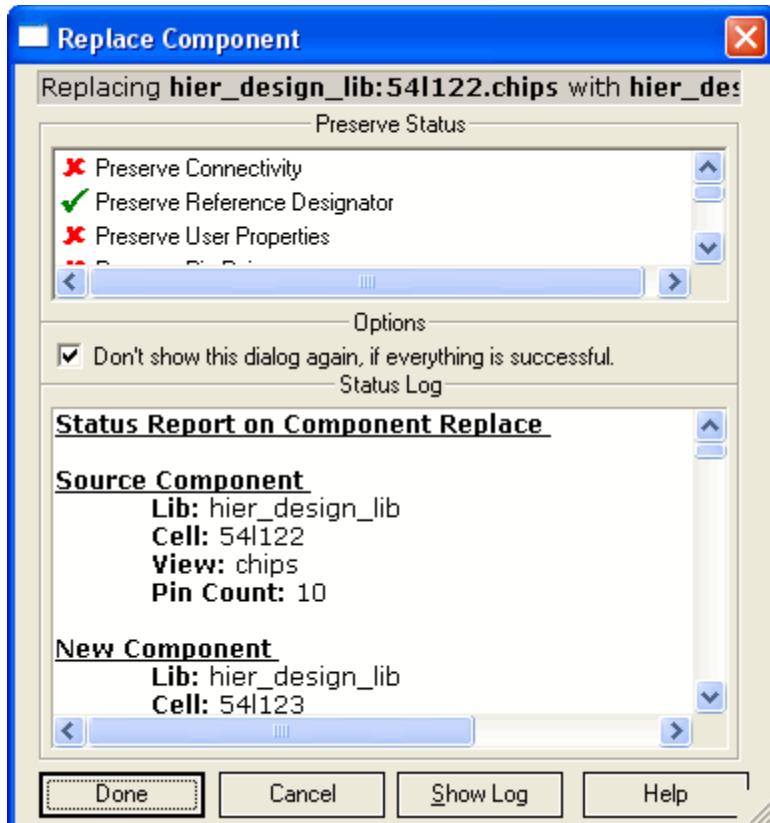
- ❑ If there is a mismatch in the pin names or pin numbers of the existing component (the component existing in the design) and the target component (the new component), the Component Replace dialog box appears.
 - a. Resolve the connectivity and property differences between the existing component and the target component in the Component Replace dialog box.
For more information on using the Component Replace dialog box, see [Using the Component Replace Dialog Box](#) on page 115.
 - b. Click *Replace*.

Note: To cancel the replace operation, click *Cancel*.

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Working with Components

The Replace Component dialog box appears displaying whether the component replace preserve options you selected in the Component Replace tab of the Setup dialog box will be honored when you replace the component.

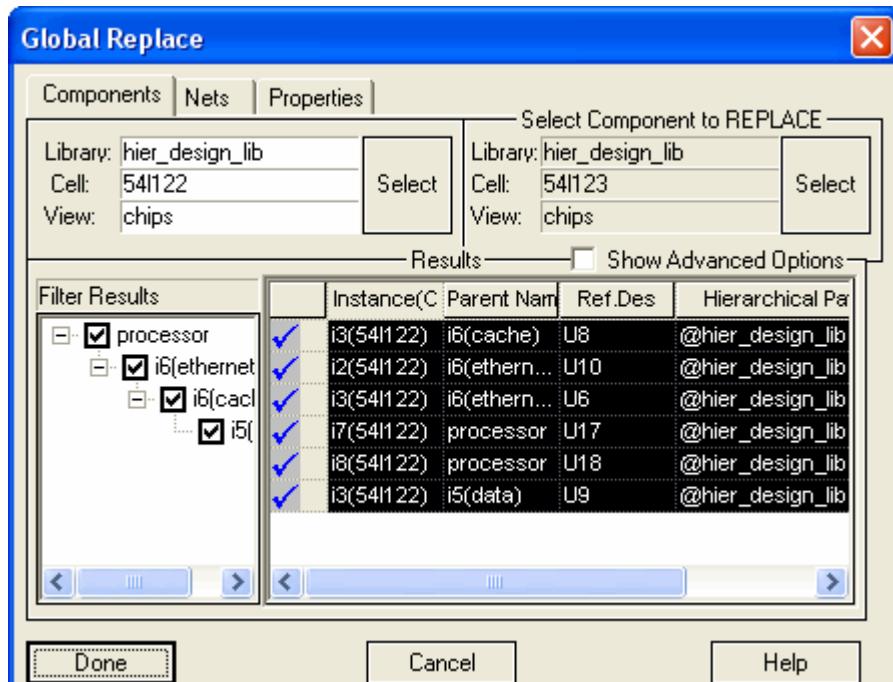


8. Click Done to close the Replace Component dialog box.

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Working with Components

The Global Replace dialog box displays the instances of the component that have been replaced in the design.



The ✓ icon indicates that instances of the component have been replaced successfully.

9. In the *Filter Results* box:

- ❑ Clear the check box next to a block name if you want to do not want to view the search results for that block.
- ❑ Select the check box next to a block name if you want to view the search results for that block.

10. To highlight a component instance that has been replaced, select the row for the instance in the *Results* list, right-click and choose *Highlight*.

The component instance is highlighted in the design.

11. Click *Done* to close the Global Replace dialog box.

Copying and Pasting Components

You can quickly add components in the design by copying a component in the Component List and pasting it. You can also copy components from another block or design and paste it in the current block or design.

When you copy and paste a component, its connectivity and property information, and the comments and bypass capacitors added on the component are also copied. This lets you add connectivity and property information on one instance of a component and copy and paste it to quickly add another instance of the component with the same connectivity and property information, thus avoiding the need to add connectivity and property information for each instance of the component in the design.

Note: When you copy and paste a component (whose pins have series terminations added on them) from one block to another block, the default signal integrity models are not automatically assigned to the resistors used in the terminations. Choose *Tools – Signal Integrity – Auto Assign Discrete Models* to automatically assign the default ESpiceDevice models for the resistor components.

For more information on copying and pasting blocks, see [Copying and Pasting Blocks](#) on page 362.

Copying Components

1. Select a component or a group of components.
2. Press *Ctrl + C* or choose *Edit – Copy*.

Pasting Components

1. Click in the Component List.
2. Choose *Edit – Paste* or press *Ctrl + V*.

Note: When you copy a component from another design and paste it in the current design, System Connectivity Manager preserves the reference designator of the component, if the same reference designator is already not being used in the current design.

Using Paste Special to Paste Components

You can use the *Paste Special* command when you paste a component in the Component List if you want to specify whether you want the connectivity information, property information

and the comments and bypass capacitors added on the original instance of the component to be pasted on the new instance of the component.

1. Click in the Component List.
2. Choose *Edit – Paste Special*.

The Paste Special dialog box appears.



Note: The *Paste Special* command will work only if you have data copied to the Clipboard using the Copy or Cut commands.

3. Select the *With Properties* check box if you want the properties on the original component to be pasted.
4. Select the *With Connectivity* if you want the connectivity information and the bypass capacitors added on the original component to be pasted.
5. Select the *With Comments* check box if you want the comments on the original component to be pasted.
6. Click *OK*.

Modifying Component Instance Names

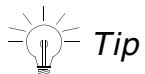
The components you add in System Connectivity Manager are automatically assigned instance names like *i1*, *i2*, and so on. The instance names are displayed in the *Name* column in the Component List.

To modify the instance name for a single component

1. Select the component in the Component List.
2. Choose *Object – Change – Name*.

The instance name is highlighted.

3. Enter the new instance name.



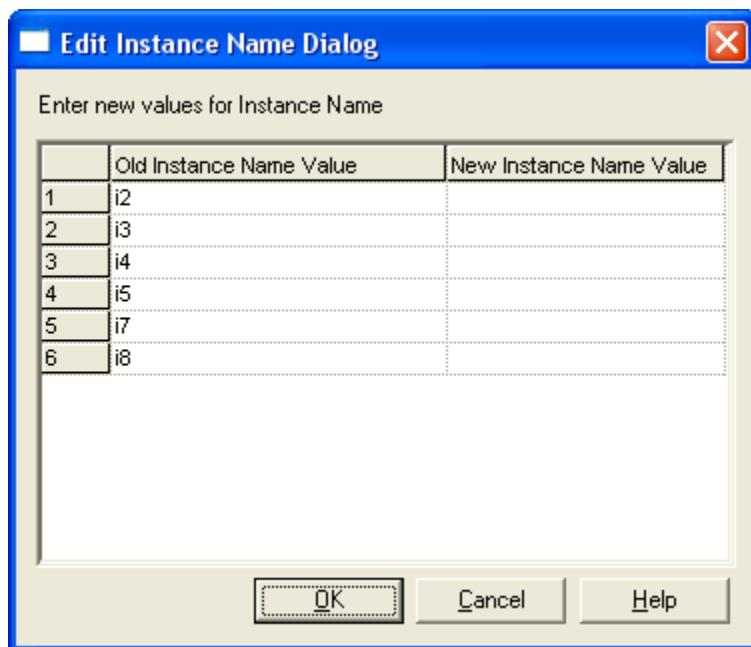
Tip

You can also click on the instance name of a component, press the *F2* key, and then modify the instance name.

To modify the instance names of multiple components simultaneously

1. Select the components whose instance names you want to change in the Component List.
2. Choose *Object – Change – Name*.

The Edit Instance Name Dialog dialog box appears.



3. Enter the new instance name in the *New Instance Name Value* column.

You can also copy instance names from another application such as Microsoft Excel and paste them in the *New Instance Name Value* column.

4. Click *OK*.

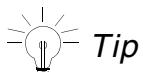
Modifying Component Reference Designators

The components you add in System Connectivity Manager are automatically assigned reference designators. The reference designators of components are displayed in the *Ref Des* column in the Component List.

You can modify the reference designators of components. If you have modified the reference designator of a component, you can reset the reference designator value to a tool assigned reference designator value.

To modify the reference designator for a single component

1. Select the component in the Component List.
 2. Choose *Object – Change – Ref Des – User Assigned*.
- The reference designator value for the component is highlighted.
3. Enter the new reference designator value.



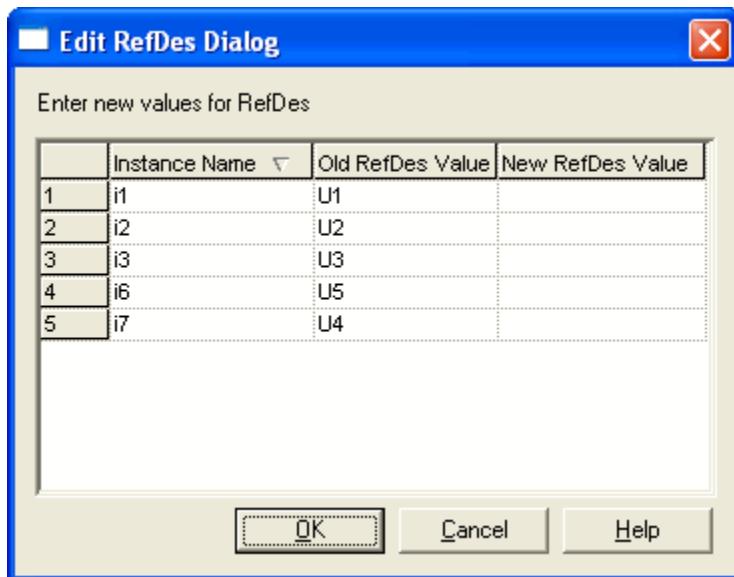
Tip

You can also click on the reference designator value for a component, press the *F2* key, and then modify the reference designator value.

To modify the reference designator of multiple components simultaneously

1. Select the components whose reference designators you want to change in the Component List.
2. Choose *Object – Change – Ref Des – User Assigned*.

The Edit RefDes Dialog dialog box appears.



3. Enter the new reference designator value in the *New RefDes Value* column.
You can also copy reference designator values from another application such as Microsoft Excel and paste them in the *New RefDes Value* column.
4. Click *OK*.

To reset the reference designator value to a tool assigned reference designator value

1. Select the component in the Component List.
2. Right-click and choose *Change – Ref Des – Tool Assigned*.

System Connectivity Manager automatically assigns a new reference designator for the component.

Working with Power Pins and NC Pins of Components

You can specify the power pins of a component using the `POWER_PINS` and `POWER_GROUP` properties. Not Connected (NC) pins can be specified using the `NC_PINS` property. Power and NC pins are unconnected pins that exist on a physical part but that are not shown on the symbol.

`POWER_PINS`, `POWER_GROUP`, and `NC_PINS` properties can be used in the following places:

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Working with Components

- In the `chips.prt` file for a component
- In the physical part table file (`.ptf`) for a component
- On the symbol for a component

Note: You cannot add `POWER_PINS`, `POWER_GROUP`, `MERGE_POWER_PINS`, `NC_PINS` and `MERGE_NC_PINS` properties in System Connectivity Manager. For more information on these properties, see the *Allegro Platform Properties Reference*.

Note: If you want to intentionally leave certain signal pins unconnected, see [Working with Unconnected Pins](#) on page 202.

If you want to check for NC pins in your design, you can use the following:

- The `phys_unconnected_pins` Rules Checker rule, which checks for unconnected pins on each packaged body in your design
- The *Edit – Component – Unconnected Pins* menu in DE-HDL
- Set `SHOW_UNCONNECTED_PIN ON` console command to show unconnected pins in DE-HDL
- The `dsreportgen` command to generate a report of all NC pins in your design. See [Using the dsreportgen Command](#) on page 550 for details.

You can use the Assign Power dialog box to change the assignment of power and NC pins of a component. The Assign Power dialog box lets you:

- Assign a new power supply to power pins by assigning global signals in your design to the pins.
- Assign an NC pin as a power pin by specifying a power supply for the NC pin.
- Assign a power pin as an NC pin.

System Connectivity Manager User Guide

Working with Components

You can view implicit power pins in the Component Connectivity pane. The option to view implicit power pins is in the *Project — Settings — General* tab. The option is off by default.



System Connectivity Manager User Guide

Working with Components

When the Show Power Pins option is enabled, power pins are visible in the Component Connectivity Details pane. Power nets attached to the power pins of a component are visible in the Signal List pane.

Pin Name	Pin Number	Pin Type	Signal
*	*	*	*
dqm1	71	Input	
dqm2	28	Input	
dqm3	59	Input	
GND	44,58,72,8...	Power	GND
GND	44	Power	GND
GND	58	Power	GND
GND	72	Power	GND
GND	86	Power	GND
GND	6	Power	GND
GND	12	Power	GND
GND	32	Power	GND
GND	38	Power	GND
GND	46	Power	GND
GND	52	Power	GND
GND	78	Power	GND
GND	84	Power	GND
NC	14,30,57,6...	NC	NC
NC	14	NC	NC
NC	30	NC	NC
NC	57	NC	NC
NC	69	NC	NC
NC	70	NC	NC
NC	73	NC	NC
P3V3	1,15,29,43...	Power	P3V3
P3V3	1	Power	P3V3
P3V3	15	Power	P3V3

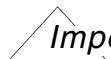
You can connect any type of signal to power pins. The connection count is updated automatically and the signal names are italicized in the Signal List pane. Once established, the connection count can be modified, but not deleted. The modified connection will appear in normal font and is not italicized.

If the nets are not available and are added in the Signal List pane, check the voltage. Add voltage to the nets before connecting power pins. If there is no voltage, you will get an error. To resolve the error, you need to add voltage to the net.

Power pin connections are passed to the physical design using the POWER_PIN and POWER_GROUP properties.

A power pin connected to an individual pin remains a single power pin, but when connected to a parent row, it acquires the properties of a power group.

When a new component is enabled with the power pin option, design differences in the Visual Design Differences pane are eliminated when transferring the physical design from the PCB Editor layout database to the Design Entry HDL schematic design (Import Physical).

 **Important**

It is recommended that you enable the *Show Power Pins in Connectivity Pane* option before you start creating any new design. If you enable the option *Show Power Pins in Connectivity Pane* while you are in the midst of creating a design, the signal count and net names that are already present will not get updated. Only nets for new components that are added after the option is enabled are displayed in the Signal List pane.

To access the Assign Power dialog box

1. In the Component List select the component whose power and NC pin assignments you want to change.

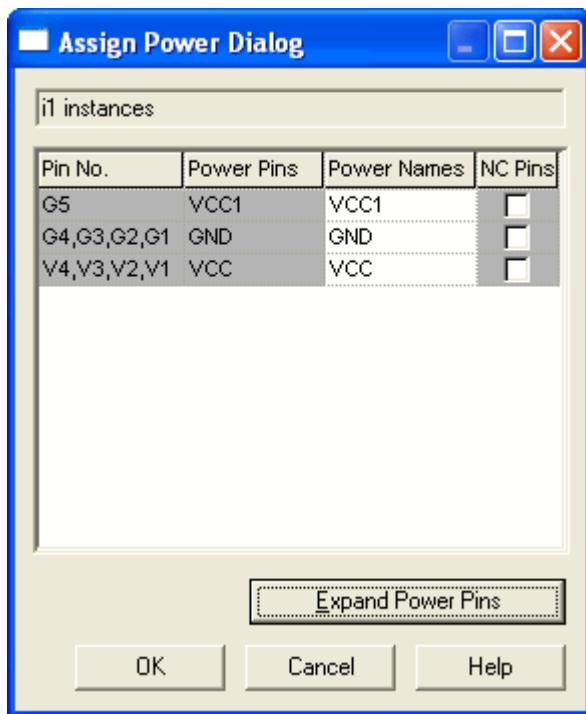
Note: To change the power and NC pin assignments of more than one instance of the component at the same time, select the instances of the component in the Component List.

2. Choose *Object – Assign Power*.

System Connectivity Manager User Guide

Working with Components

The Assign Power dialog box appears.

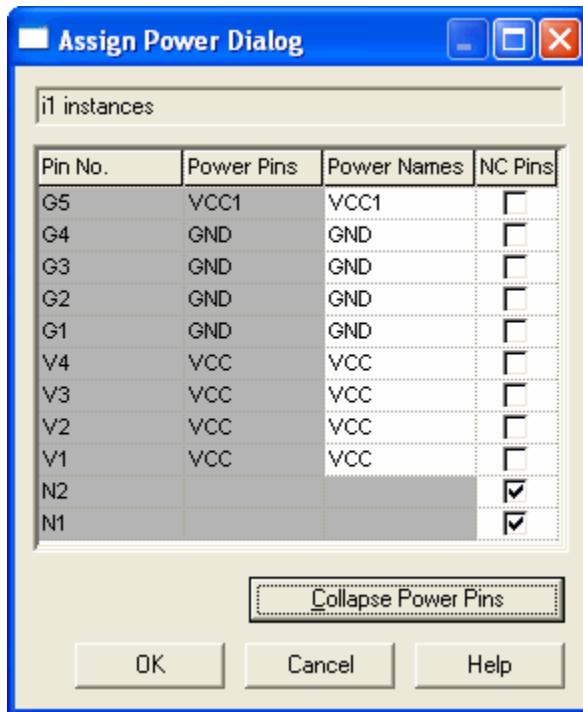


The Assign Power dialog box displays the power pins on the component. In the above figure, the power pin G5 is connected to the power supply VCC1 and the power pins G1, G2, G3, and G4 are connected to the power supply GND.

System Connectivity Manager User Guide

Working with Components

3. To view the power supply connected to each power pin and to display the NC pins on the component, click the *Expand Power Pins* button.



In the above figure, the *NC Pins* check box next to the pins N1 and N2 are selected. This indicates that the pins are NC pins.

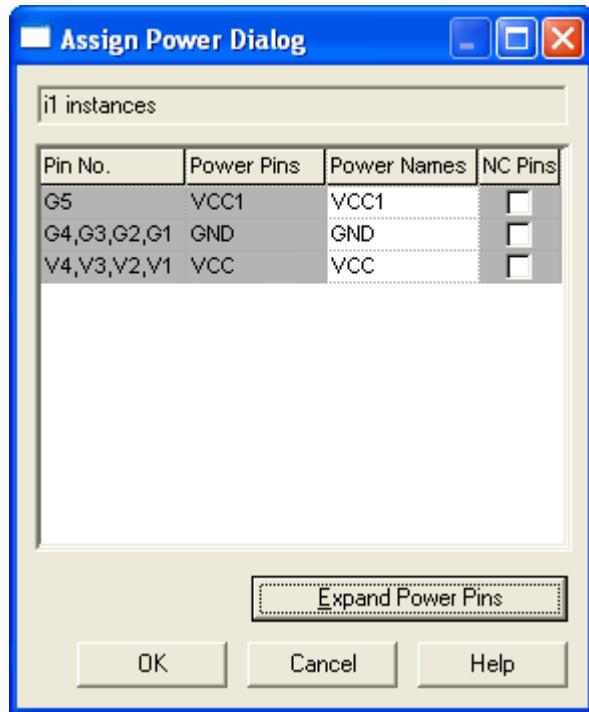
To assign a new power supply to power pins

Click in the *Power Names* cell next to a power pin and select another global signal in the drop-down list.

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Working with Components

If more than one power pin is connected to the same power supply, the new power supply is assigned to all the power pins. For example, in the following figure, the power supply GND is connected to the pins G1, G2, G3, and G4.

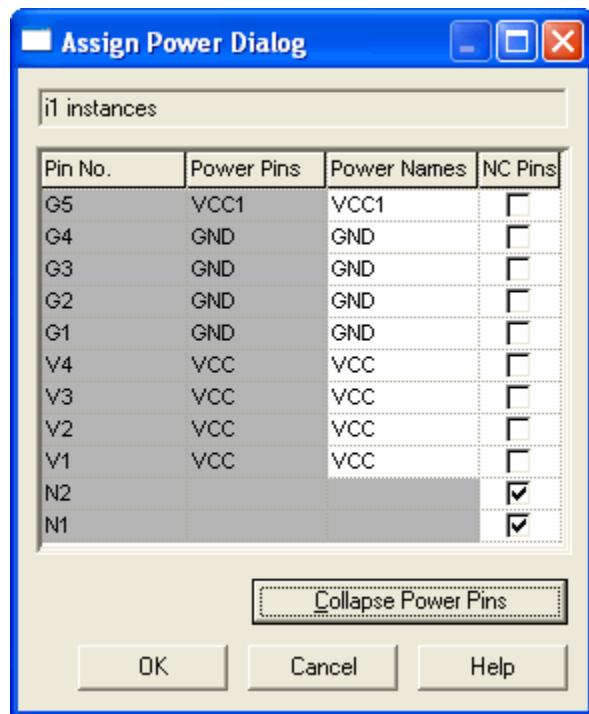


If you now select a global signal named GROUND in the *Power Names* cell next to the pins, all the pins are connected to the new power supply named GROUND.

System Connectivity Manager User Guide

Working with Components

If you want to assign a new power supply to each pin, click the *Expand Power Pins* button to display the power pins in expanded format as shown below:



You can now assign a new power supply for each of the pins. To do this, click in the *Power Names* cell next to a pin and choose a global signal from the drop-down list.

To assign an NC pin as a power pin

1. Click the *Expand Power Pins* button to display the NC pins on the component.
2. Clear the check box next to the NC pin.
3. Click in the *Power Names* cell next to the NC pin and select a global signal in the drop-down list.

To assign a power pin as an NC pin

1. Select the *NC Pins* check box next to the power pin.

Controlling the Overwriting of POWER_PINS Properties

It can happen that you are capturing your logical design and creating the parts being used in the design in parallel. While capturing the design, you can use the Assign Power dialog box to do the following:

- Assign a new power supply to power pins by assigning global signals in your design to the pins.
- Assign an NC pin as a power pin by specifying a power supply for the NC pin
- Assign a power pin as an NC pin.

Performing these operations overrides the power pin assignments defined using the POWER_PINS properties in the `chips.prt` file or the physical part table (`.ptf`) file or the symbol. If you want to retain the power pin assignments in the `chips.prt` file or the physical part table (`.ptf`) file or the symbol, set the following directive in the `<projectname>.cpm` file for your project, or the `site.cpm` file.

```
ALLOW_POWER_PINS 'OFF'
```

By default, the `ALLOW_POWER_PINS` directive is set to `ON`. If it is set to `OFF`, you cannot make any changes in the *Assign Power* dialog box.

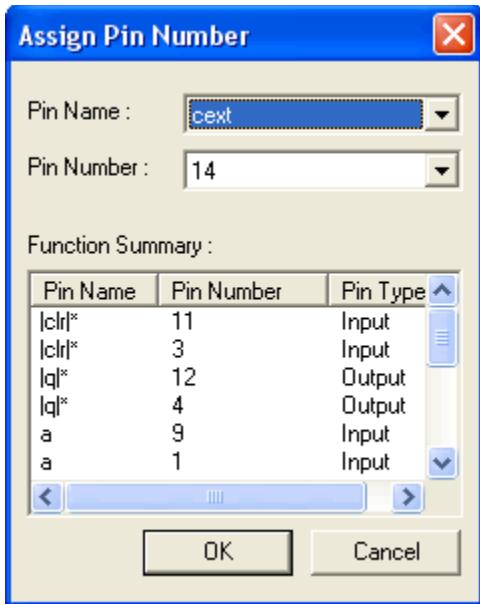
Swapping Pins Across Functions of a Component

You can exchange the location of two pins across two functions in a multi-function component by swapping the two pins. Swapping pins across functions lets you minimize the average net length when you route the board in Allegro PCB Editor.

To swap pins across functions of a component

1. Select the pin name or pin number of the pin in the Component Connectivity Details pane.
For more information on using the Component Connectivity Details pane, see [Component Connectivity Details Pane](#) on page 54.
2. Right-click and choose *Assign Pin Number* then do one of the following:
 - ❑ Choose the pin number of the pin with which you want to swap the selected pin.
 - ❑ Choose *More* if you want to swap any other pin of the component.

If you choose *More*, the Assign Pin Number dialog box appears.



- a. In the *Pin Name* drop-down list, select the pin you want to swap with the pin in another function.
 - b. In the Pin Number drop-down list, select the pin number of the pin with which you want to swap the selected pin.
3. Click *OK*.

Deleting Components

To delete components

- To delete a component or a group of components, select them in the Component List and do one of the following:
 - Choose *Edit – Delete*.
 - Press the *Delete* key.

Working with Blocks

For more information on working with hierarchical blocks, see [Chapter 13, “Working with Hierarchical Designs.”](#)

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Working with Components

Working with Signals

This section describes the following procedures for working with signals in System Connectivity Manager:

- [Signal Naming Conventions](#) on page 146
- [Adding Signals to a Design](#) on page 147
- [Viewing Bits of a Vector Signal in Signal List Pane](#) on page 151
- [Aliasing Nets](#) on page 152
- [Copying and Pasting Signals](#) on page 160
- [Using Paste Special to Paste Signals](#) on page 160
- [Swapping Signals](#) on page 166
- [Deleting Signals](#) on page 167
- [Modifying the Scope of a Signal](#) on page 167
- [Modifying the Logical Name of a Signal](#) on page 167
- [Modifying the Physical Net Name of a Signal](#) on page 168
- [Specifying the Voltage for Signals](#) on page 159
- [Copying and Pasting Signals](#) on page 160
- [Using Paste Special to Paste Signals](#) on page 160
- [Navigating a Signal](#) on page 169
- [Working with Comments](#) on page 169

Signal Naming Conventions

Signal names must follow the following naming conventions:

- Names cannot be VHDL and Verilog keywords.
- For vectored signals, do not add the bit range as part of the name. Separate the vector or bit range with two periods (..) and enclose it in angle (<>) or square ([]) brackets. The bit order is <MSB..LSB> where MSB is the most significant bit and LSB is the least significant bit of the signal. For example, a<12..4> is a valid vectored signal, while a(12..4) is a scalar signal.
- System Connectivity Manager is not case-sensitive. System Connectivity Manager treats two names that differ only in uppercase or lowercase as the same name.
- Signal names can have greater than 31 characters, but the physical net names will be truncated to 31 characters.
- NC signal cannot be added as a vectored signal. For example, you cannot add a signal named NC<7..0> or NC[6..0].

The following characters must not be used in signal names:

Single quotation mark (')

double quotation marks (")

exclamation mark (!)

forward slash (/)

Backward slash (\)

ampersand (&)

back tick (`)

colon (:)

<

Adding Signals to a Design

This section describes the various ways in which you can add signals in System Connectivity Manager.

Adding a signal

1. Click on the Signal List pane.
2. Press the *Insert* key to add a new row in the Signal List.
3. Type the name of the new signal in the *Name* column and press *Enter*.

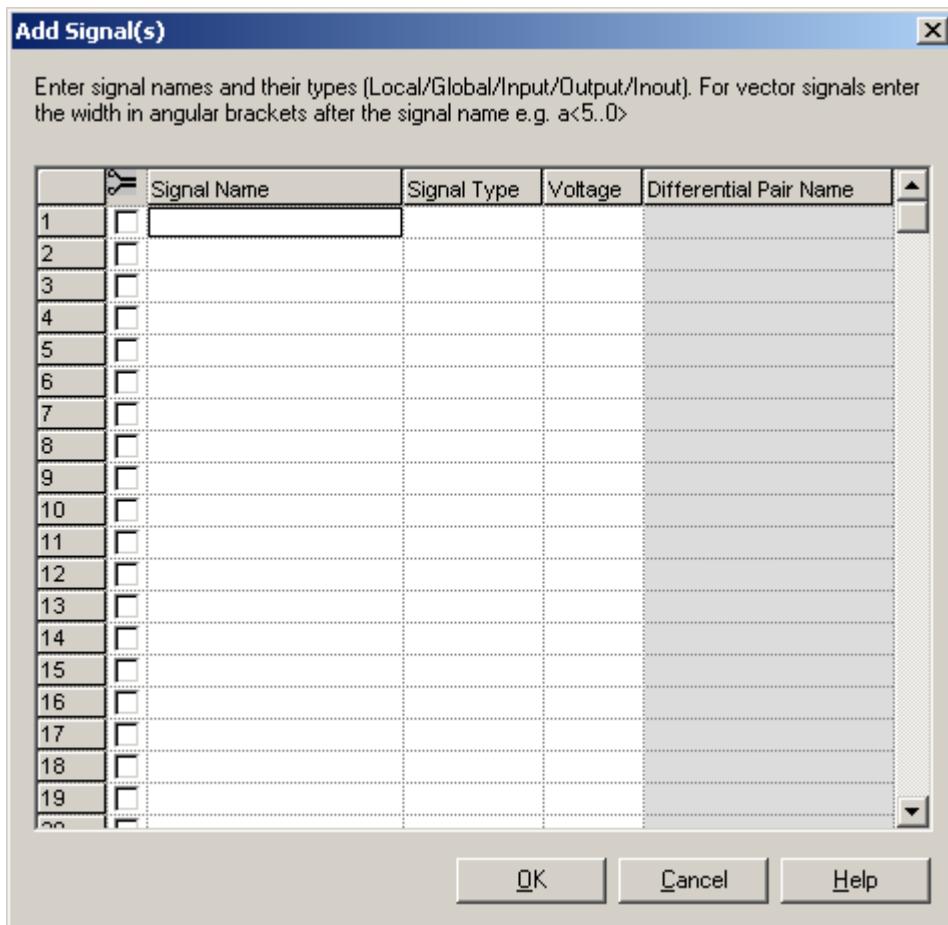
Adding multiple signals

1. Click on the Signal List pane.
2. Choose *Design – Add Signal*.

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Working with Signals

The Add Signal(s) dialog box appears.



3. Enter the name of the signal in the *Signal Name* field.

Note: Signal names must follow the naming conventions described in [Signal Naming Conventions](#) on page 146.

4. Specify the scope of the signal as LOCAL, GLOBAL, IN, OUT, or INOUT in the *Signal Type* list.
5. If you want to define the signal as a power net, enter the voltage for the signal in the *Voltage* field.

Note: The default unit for voltage is Volts. To specify the voltage in millivolts, say, 75 Mv, enter the voltage as:

0.075

Note: All voltage values are rounded off to three significant digits to the right of the decimal, and stored as Volts.

6. Click OK.

The new signals are displayed in the Signal List.

Adding signals from a file

You can save the list of signals used in one design to a file, and then add signals from that file to the current design. This lets you quickly add signals in a design.

To save the list of signals used in a design to a file:

- 1. Open the design or block from which you want to save the list of signals to a file.**
- 2. In the Signal List, select the signals you want to save to a file.**
- 3. Choose *Design – Save Signals To File*.**

The Save File As dialog box appears.

- 4. Enter the name of the file in the *File name* field and click *Save*.**

By default, the file is saved with the `.sig` extension.



Only the signals highlighted in the Signal List are exported to the `.sig` file.

To add signals from the file you created using the above procedure, do the following:

- 1. Open the design or block in which you want to add the signals from the file.**
- 2. Choose *Design – Load Predefined Signals*.**

The Open Signal File dialog box appears.

- 3. Select the file containing the list of signals you want to add and click *Open*.**

The signals defined in the file are added in the Signal List.

Syntax of .sig File

The `.sig` file has the following syntax:

```
(  
("<signal_name>" "<signal_type>" "<voltage_value>" "<LSB>" "<MSB>")  
)
```

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Working with Signals

Where:

signal_name	Is the name of the signal you want to add.
	Note: Signal name is case-sensitive.
signal_type	Is the type of the signal you want to add. The signal type can be one of the following: <ul style="list-style-type: none">■ Global■ Input■ Output■ Inout■ Local
voltage_value	Is the voltage value of the signal. Specify the voltage value in Volts if you want to define the signal as a power net. For example, if you want to specify the voltage as 5 V, enter "5.000 V". To specify the voltage as 75 Mv, enter "0.075 V". If you do not want to define the signal as a power net, specify the voltage as "". For example, if you want to define an input signal named DATA without a voltage value, use the following syntax: (("DATA" "Input" "" "-1" "-1"))
LSB	Is the least significant bit for a vectored signal. For scalar signals this is set to -1.

MSB

Is the most significant bit for a vectored signal.

For example, if you want to define a output vectored signal named ADDRESS<7..0>, use the following syntax:

```
(  
("ADDRESS" "Output" "" "7" "0")  
)
```

Where 7 is the LSB and 0 is the MSB for the signal.

If you want to declare a scalar signal, specify the LSB and MSB as "-1". For example, to declare an input scalar signal named CBDATA, use the following syntax:

```
(  
("CBDATA" "Input" "" "-1" "-1")  
)
```

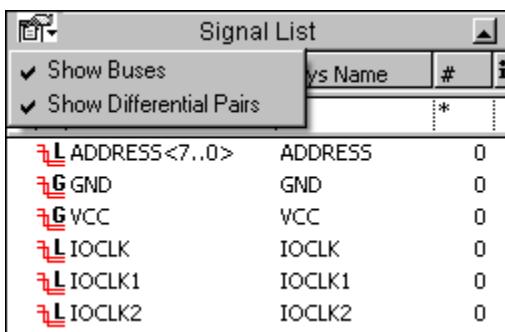
Viewing Bits of a Vector Signal in Signal List Pane

By default, vectored signals are displayed in the Signal List. If you want to connect bits of a vectored signal to pins using the Component Connectivity Details pane or the Signal Connectivity Details pane, System Connectivity Manager provides you with the options to expand the vector signals such that only the bits of vector signals are displayed in the Signal List.

Displaying Bits of Vector Signals

To display the bits of a vector signal, complete one of the following steps.

- Right-click on the Signal List pane header and deselect *Show Buses*.
- Select the  button in the Signal List pane as header and deselect *Show Buses*.



The screenshot shows the Signal List pane with the following configuration:

- Header buttons:
- Checkboxes:
 - Show Buses
 - Show Differential Pairs
- Table headers:

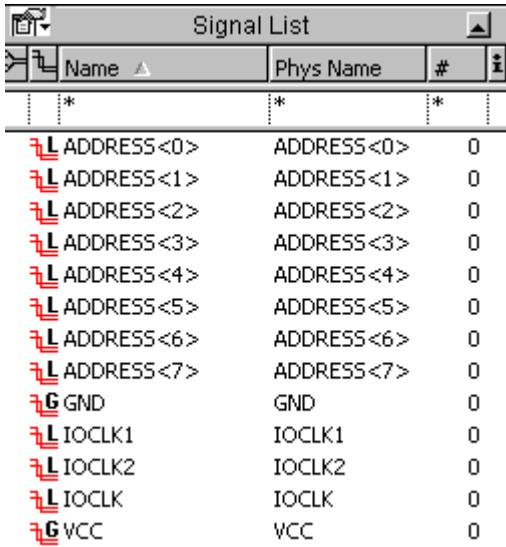
sys Name	#	
----------	---	--
- Table data:

ADDRESS<7..0>	ADDRESS	0
GND	GND	0
VCC	VCC	0
IOCLK	IOCLK	0
IOCLK1	IOCLK1	0
IOCLK2	IOCLK2	0

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Working with Signals

The bits of the vectored signal ADDRESS<7..0> are now displayed in the Signal List as shown below:



Name	Phys Name	#
*	*	*
L ADDRESS<0>	ADDRESS<0>	0
L ADDRESS<1>	ADDRESS<1>	0
L ADDRESS<2>	ADDRESS<2>	0
L ADDRESS<3>	ADDRESS<3>	0
L ADDRESS<4>	ADDRESS<4>	0
L ADDRESS<5>	ADDRESS<5>	0
L ADDRESS<6>	ADDRESS<6>	0
L ADDRESS<7>	ADDRESS<7>	0
GND	GND	0
IOCLK1	IOCLK1	0
IOCLK2	IOCLK2	0
IOCLK	IOCLK	0
VCC	VCC	0

To view the unexpanded vectored signals, again right-click on the Signal List pane header and select *Show Buses*.

Aliasing Nets

The following procedures describe how you can alias nets in your design:

- [Aliasing Two Scalar Nets](#)
- [Aliasing Two Vectored Nets](#)
- [Aliasing a Net to Multiple Nets Simultaneously](#)
- [Declaring an Aliased Net as the Base Net](#)
- [Removing an Alias](#)

Aliasing Two Scalar Nets

- Select two nets in the Signal List, then choose *Object – Alias*.

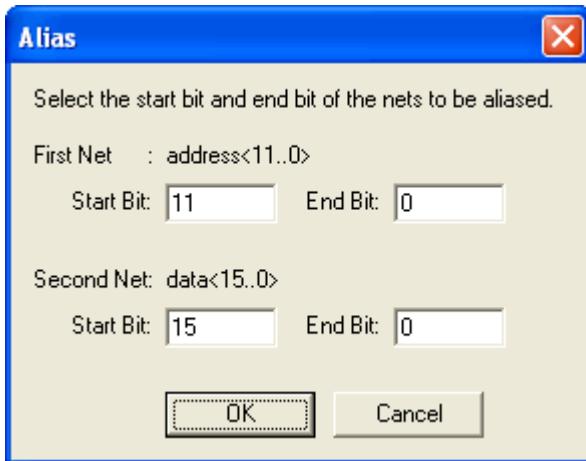
Aliasing Two Vectored Nets

1. Select two vectored nets in the Signal List, then choose the *Object – Alias*.

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Working with Signals

If both the vectored nets have same the width, they get aliased. If they have different width, the Alias dialog box appears.

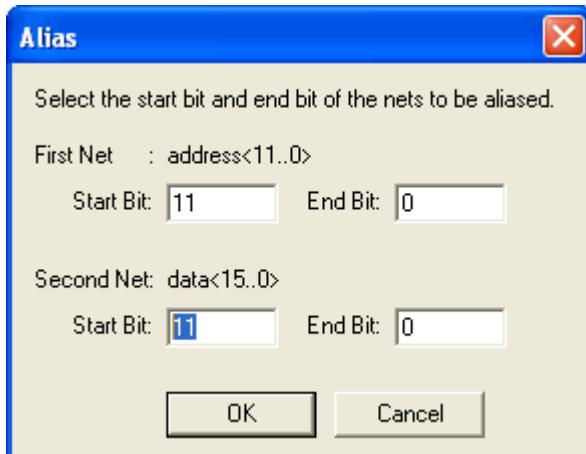


In the above example, the Alias dialog box appears because of the mismatch in the width of the vectored net `address<11..0>` being aliased to the vectored net `data<15..0>`.

Note: If the two vectored nets are already aliased, the Edit Alias dialog box appears instead of the Alias dialog box. For more information on using the Edit Alias dialog box, see [Aliasing a Net to Multiple Nets Simultaneously](#) on page 154.

2. Enter the start and end bit of the nets to be aliased (ensuring that the width you specify is same for both the nets).

For example to alias the net `address<11..0>` with the bit range `<11..0>` of the `data<15..0>` net, enter the start bit for the `data<15..0>` net, as shown below:



3. Click **OK**.

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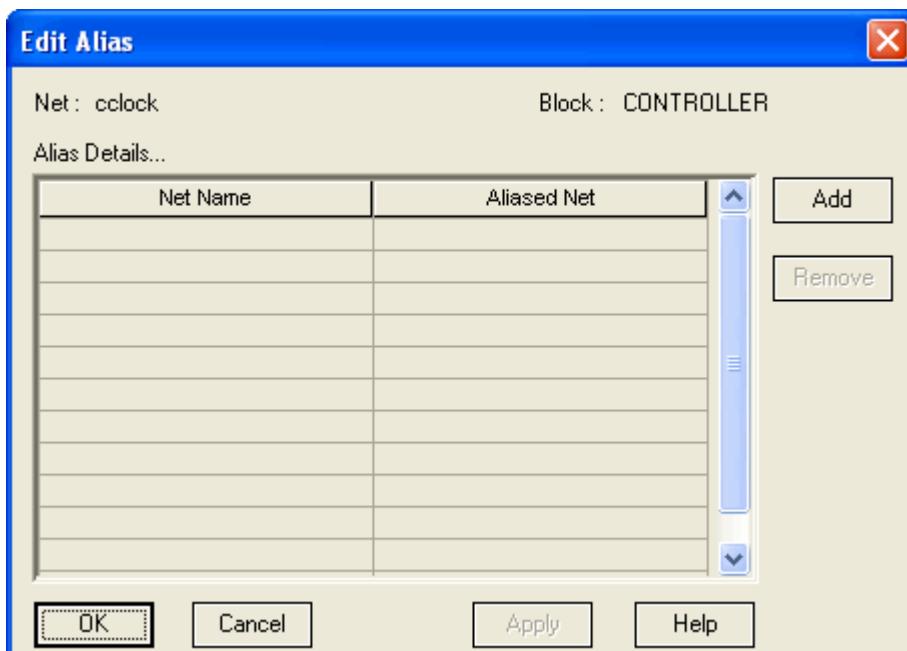
Working with Signals

The two vectored nets are aliased.

Aliasing a Net to Multiple Nets Simultaneously

1. Select the net in the Signal List, right-click and choose *Alias*.

The Edit Alias dialog box appears.

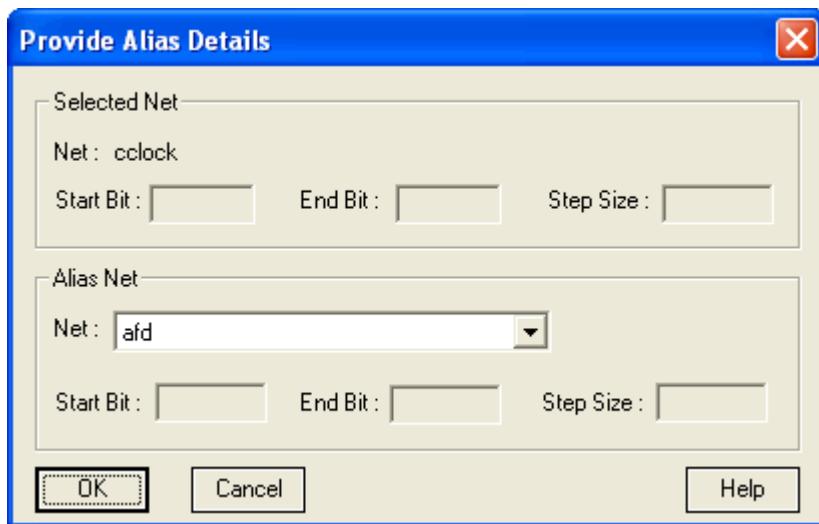


2. To add an alias, click the *Add* button.

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Working with Signals

The Provide Alias Details dialog box appears.



The *Selected Net* box displays the properties of the existing net. If the net is a vectored net, the start bit, end bit and step size of the net are displayed. For more information on using step size in vectored nets, see [Using Step Size to Connect or Alias Vectored Signals on page 185](#)

3. To alias the net, select the net to be aliased in the *Net* drop-down list.

If you select a vectored net as alias, the start bit, end bit and step size of the net are displayed.

4. Click *OK* to alias the nets and close the Provide Alias Details dialog box.

The new alias is displayed in the Edit Alias dialog box.

5. Repeat steps 2 to 4 to add more aliases.

6. Click *OK* to close the Edit Alias dialog box.

Declaring an Aliased Net as the Base Net

When two nets are aliased, System Connectivity Manager selects one of the net names as the base net or the master net by following the rules for choosing the base net. For more information on the rules for choosing the base net, see [Rules for Choosing the Base Net on page 158](#).

System Connectivity Manager assigns the physical net name of the base net to both the aliased nets. For example, if you alias two nets named `data` and `reset`, System Connectivity Manager assigns the physical net name, say `DATA` to both the nets because the `data` net is

System Connectivity Manager User Guide

Working with Signals

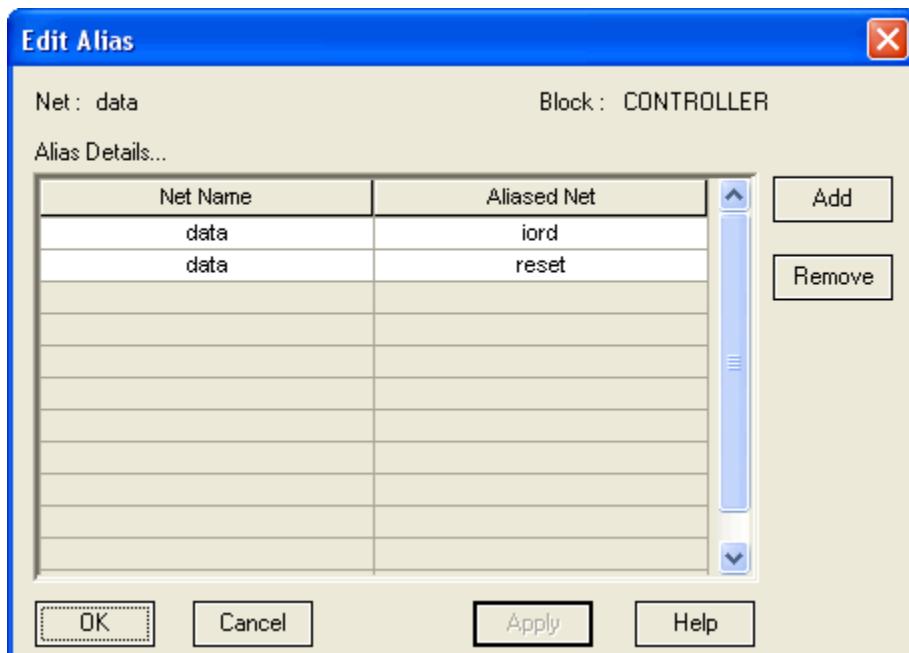
the base net according to the rules for choosing the base net. The name of the base net becomes the name of corresponding physical net in the board in Allegro PCB Editor. In the above example, the physical net DATA in the board corresponds to the aliased nets data and reset in the design in System Connectivity Manager.

You may want the name of a particular aliased net to be passed to Allegro PCB Editor as the physical net name for the aliased nets even if the net is not the base net by default. You can do this by declaring the aliased net as a base net in System Connectivity Manager. For example, when you alias the nets `data` and `reset`, the `data` net becomes the base net by default. You can override this by declaring the `reset` net as the base net.

To declare an aliased net as the base net

1. Select the data net or the reset net in the Signal List.
 2. Right-click and choose *Alias*.

The Edit Alias dialog box appears.

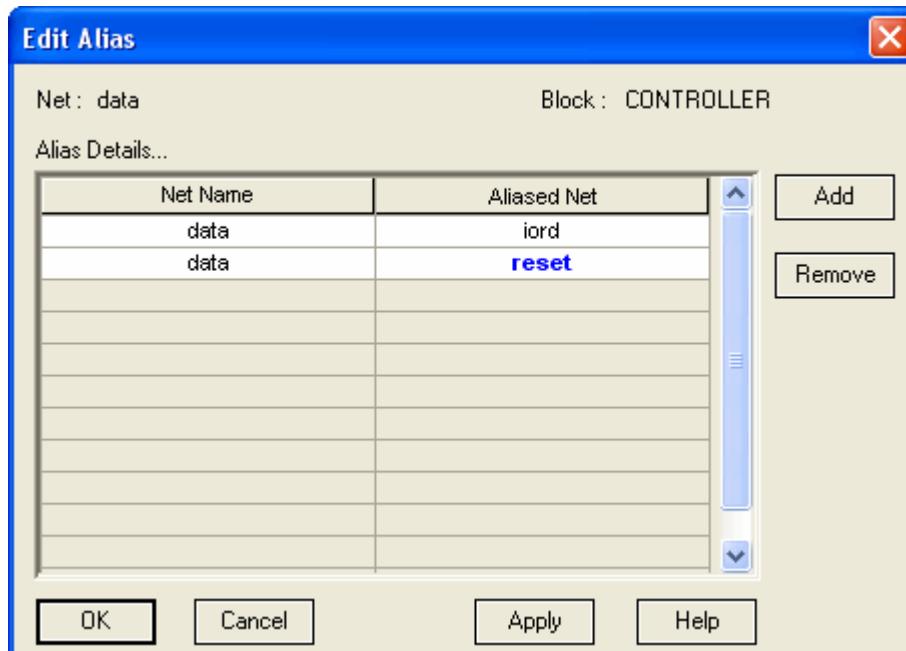


3. Select the reset net, right-click, and choose *Make Base*.

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Working with Signals

The `reset` net is displayed in blue color indicating that it has been declared as the base net.



Note: To remove the base net declaration, select the `reset` net, right-click and choose *Clear Base*.

4. Click *OK*.

The next time you open the Edit Alias dialog box, the base net is displayed in bold letters in black color.

Note: If you declare more than one net as the base net in the Edit Alias dialog box, System Connectivity Manager applies the rules for choosing the base net to identify the winning base net. For more information on the rules for choosing the base net, see [Rules for Choosing the Base Net](#) on page 158.

Note the following:

- The base net inherits all the properties that exist on the nets aliased to it. A property you add on a base net also applies to the nets aliased to it.
- If the same property exists on the base net and an aliased net, the value of the property on the base net will be used.
- If the same property exists on the base net and an aliased net, and you change the value of the property on any of the aliased nets, the change is reflected on both the aliased nets.

Rules for Choosing the Base Net

The rules for selecting a base net are listed below, in the order in which System Connectivity Manager applies them. If System Connectivity Manager cannot select the base net name from the first rule, the next rule is applied, and so on.

1. Select the net that is declared as the base net.
2. Select a constant net over a non-constant net.

For example, if a constant net 123 is aliased to a non-constant net `CLOCK`, the constant net will be the base net.

3. Select the lower bit number of two nets with the same name (for example, `X<0>` is selected over `X<3>`).
4. Select a user-assigned net name over an unnamed net.
For example, if a net `CLOCK` is aliased to an unnamed net, the net `CLOCK` will be treated as the base net.
5. Select a scalar net over a vectored net.
6. Select the net that is lexicographically smaller (for example, `CLK` is selected over `CLOCK`).

Removing an Alias

You can remove the aliasing of nets in the Signal List or in the Edit Alias dialog box.

To remove the aliasing of nets in the Signal List:

1. In the Signal List select two nets that are aliased.
2. Choose *Object – Remove Alias*.

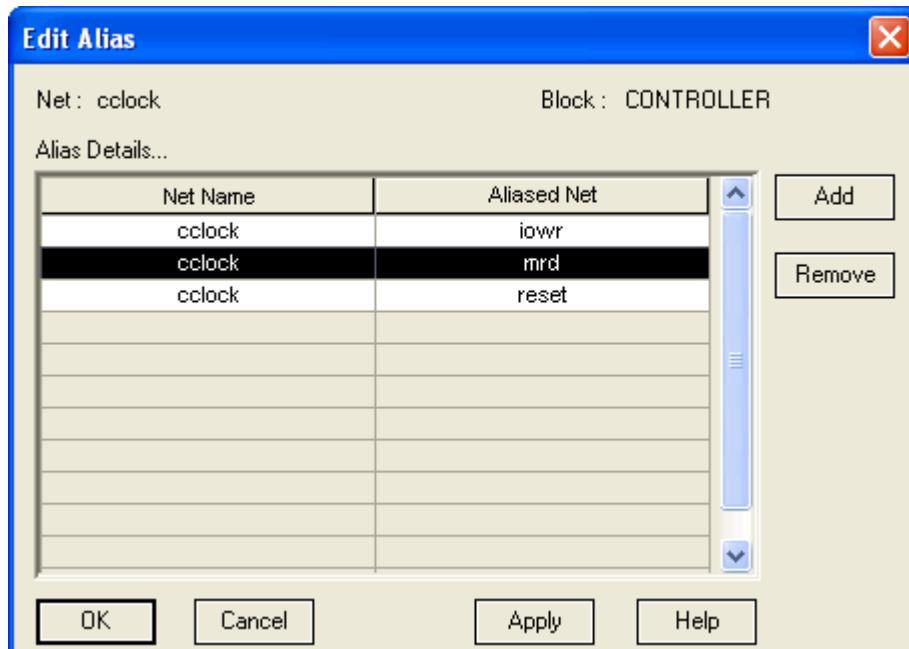
To remove the aliasing of nets in the Edit Alias dialog box:

1. In the Signal List select the net whose aliases you want to remove.
2. Right-click and choose *Alias*.

System Connectivity Manager User Guide

Working with Signals

The Edit Alias dialog box appears displaying the list of nets aliased to the net.



3. Select the row for the aliased net you want to remove and click the *Remove* button.
4. Click *OK*.

Specifying the Voltage for Signals

To specify the voltage value for a single signal

1. Select the signal in the Signal List.
2. Choose *Object – Change – DC Voltage*.
The DC Voltage dialog box appears.
3. Specify the voltage value for the signal and click *OK*.

To specify the voltage value for multiple signals simultaneously

1. Select the signals for which you want to specify voltage values in the Signal List.
2. Choose *Object – Change – DC Voltage*.
The Edit Signal Voltage dialog box appears.

3. Specify the voltage value in the *Voltage* column.

You can also copy voltage values from another application such as Microsoft Excel and paste them in the *Voltage* column.

4. Click *OK*.

Copying and Pasting Signals

Copying Signals

1. Select a signal or a group of signals in the Signal List.
2. Choose *Edit – Copy* or press *Ctrl + C*.

Pasting Signals in the Signal List

1. Click in the Signal List.
2. Choose *Edit – Paste* or press *Ctrl + V*.

When you paste a signal in the Signal List, the name of the new signal will be in the format:

`Copy_1_of_<signal_name>`

For example, if you copy a signal named `VCC` and paste it in the Signal List, the new signal name will be `Copy_1_of_VCC`.

Note: When you paste a signal in the Signal List, all the properties and pullups and pulldowns added on the original signal are also copied to the new signal.

Note: If you paste the signal in another design that does not use a signal with the same name, the signal will be pasted with the same name as the original signal.

Using Paste Special to Paste Signals

You can use the *Paste Special* command to paste signal names in the Signal List and in the Component Connectivity Details pane.

Using Paste Special in the Signal List

1. Choose *Edit – Paste Special*.

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Working with Signals

The Paste Special dialog box appears.



Note: The Paste Special command will work only if you have data copied to the Clipboard using the Copy or Cut commands.

2. Select the With Properties check box if you want the properties on the signal to be copied.
3. Select the With Comments check box if you want the comments to be copied.
4. Click *OK*.

A new signal with the name *Copy_1_of_<signal_name>* appears in the Signal List.

Using Paste Special in the Component Connectivity Details Pane

You can use paste special in the Component Connectivity Details pane to modify the data you copied and then paste the modified information in the *Signal* column in the Component Connectivity Details pane.

For example, if two components need similar pin-signal connectivity, but with a few changes, add the pin-signal connectivity on the first component, copy the signals from the Component Connectivity Details pane for the first component and use paste special to paste it on the second component after making the required changes.

You can also copy signal names from the Signal List or from another application such as Microsoft Excel, and use paste special to paste the information on a component after making the required changes.

To use paste special in the Component Connectivity Details pane

1. In the Component List, select the component on which you want to paste the signals you copied from the Component Connectivity Details pane for another component or from another application such as Microsoft Excel.

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Working with Signals

2. Click on the *Signal* cell starting from which you want to paste the signal names.

Component Connectivity Details							
Attach Signal: <input type="button" value="fx"/>							
i27 (mcm) - U7							
<input type="checkbox"/> Expand All Pins							
Pin Name	Pin Number	Pin Type	Signal ▾	Termination			
*	*	*	*	*	*	*	*
[+] address<11..0>	B6,B7,B8...	Output					
afd	A9	Input					
afs	A8	Input					
cclock	A3	Input					
[+] data<15..0>	H2,H1,G1...	Output					
iord	A5	Input					
iowr	A6	Input					
mrd	J6	Input					
mready	A2	Input					
mwr	J5	Input					
reset	A4	Input					
rfd	J3	Input					
rfs	J2	Input					
sclock	A7	Input					
sel	A1	Output					
set1	H8	Output					
set2	H3	Output					
set	H9	Output					

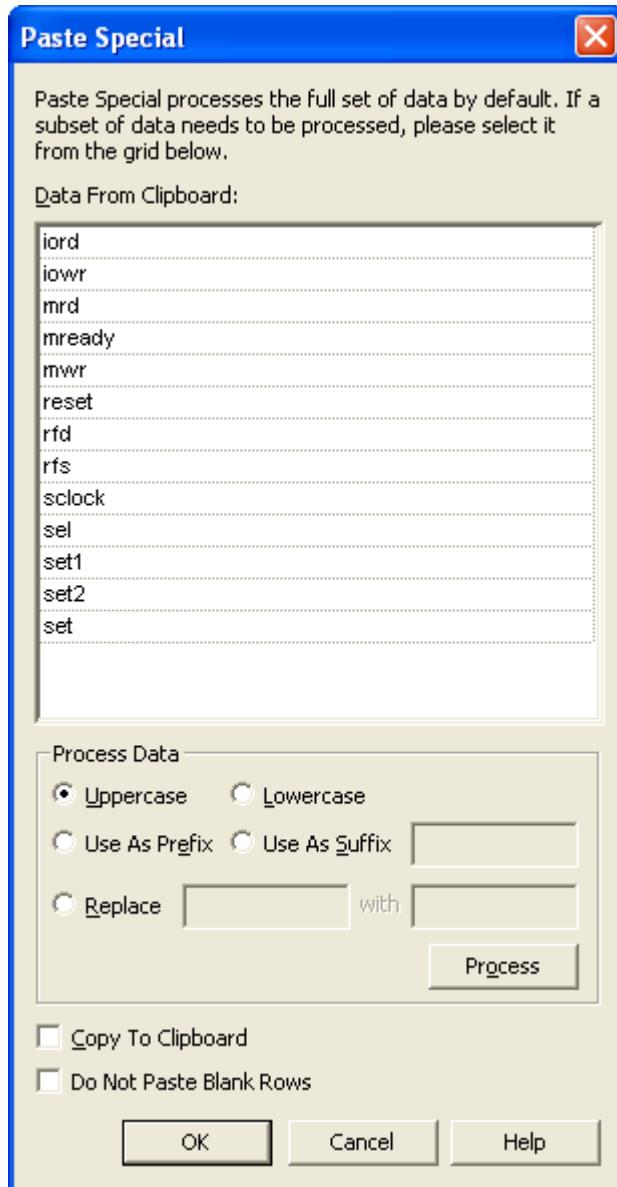
For example, in the above figure the *Signal* cell next to the `iord` pin is selected. The signal names will be pasted starting from this cell.

3. Choose *Edit – Paste Special*.

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Working with Signals

The Paste Special dialog box appears displaying the list of signals you copied.



You can now modify the signal names using the options for processing the data in the Paste Special dialog box.

4. By default, all the signal names will be modified when you use an option for processing the data. To modify only a subset of the signal names, use the *Ctrl* and *Shift* keys to select only the signal names you want to be modified in the *Data From Clipboard* list.

Note the following:

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Working with Signals

- If you do not want to paste a signal name on the component, select the signal name in the *Data From Clipboard* list and press the *Delete* key to delete the signal name.
- To modify a signal name manually, do one of the following:
 - Select the signal name in the *Data From Clipboard* list and type the new signal name.
 - Double-click on the signal name and modify the signal name.
 - Select the signal name and press the *F2* key. The signal name becomes editable. You can now modify the signal name.

5. Select the option for processing the data.

The usage of each option is described in the following table.

Select	To
Upper Case	Change the data to all uppercase letters. For example, the signal name <code>clock</code> is changed to <code>CLOCK</code> .
Lower Case	Change the data to all lowercase letters. For example, the signal name <code>DATA</code> is changed to <code>data</code> .
Use As Prefix	Add the specified prefix to the data. Select this option and enter the prefix you want to use in the text box next to the <i>Use as Suffix</i> option. For example, if the prefix is <code>mcm_</code> the signal name <code>reset</code> changes to <code>mcm_reset</code> .
Use As Suffix	Add the specified suffix to the data. Select this option and enter the suffix you want to use in the text box next to the <i>Use as Suffix</i> option. For example, if the suffix is <code>_mcm</code> the signal name <code>reset</code> changes to <code>reset_mcm</code> .
Replace	Replace a string with another string.

6. Click *Process* to process the data.

Note: If you have selected some signal names in the *Data From Clipboard* list, only

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Working with Signals

the selected signal names will be modified when you click the *Process* button. If you later want to use another option for modifying all the signal names, you need to clear the selection in the *Data From Clipboard* list. To clear the selection in the *Data From Clipboard* list, click anywhere outside the *Data From Clipboard* list.

7. Select the *Copy to Clipboard* check box if you want to copy the modified data to the clipboard.
8. Select the *Do Not Paste Blank Rows* check box if you do not want blank rows in the Paste Special dialog box to be pasted.
9. Click *OK*.

The modified signal names are pasted in the *Signal* column in the Component Connectivity Details pane.

The screenshot shows the 'Component Connectivity Details' dialog box. At the top, there is a search bar labeled 'Attach Signal:' with a magnifying glass icon. Below it, the component name 'i27 (mcm) - MCM2' is displayed, along with a checkbox for 'Expand All Pins'. The main area is a table with columns: Pin Name, Pin Number, Pin Type, Signal, and Termination. The 'Signal' column contains modified signal names starting from the 'iord' pin. The table has 20 rows, each representing a pin. The last row, corresponding to the 'iord' pin, has a highlighted background.

Pin Name	Pin Number	Pin Type	Signal	Termination		
*	*	*	*	*	*	*
+ address...	B6,B7,B8...	Output				
afd	A9	Input				
afs	A8	Input				
cclock	A3	Input				
+ data<1...	H2,H1,G...	Output				
iord	A5	Input	mcm_jord			
iowr	A6	Input	mcm_iowr			
mrd	J6	Input	mcm_mrd			
mready	A2	Input	mcm_mready			
mwr	J5	Input	mcm_mwr			
reset	A4	Input	mcm_reset			
rfd	J3	Input	mcm_rfd			
rfs	J2	Input	mcm_rfs			
sclock	A7	Input	mcm_sclock			
sel	A1	Output	mcm_sel			
set1	H8	Output	mcm_set1			
set2	H3	Output	mcm_set2			
set	H9	Output	mcm_set			

In the above figure, the signals have been pasted starting from the *Signal* cell next to the *iord* pin you selected in step 2 above.

Swapping Signals

You can exchange signals connected to pins by swapping the two signals. Swapping signals lets you minimize the average ratsnest crossings when you route the board in Allegro PCB Editor.

Swapping signals gains more significance for BGAs and similar components where the Pin Name and the Pin Number are same.

Swap Signals is supported for any signal connected to scalar or single-bit vector pin.

Note: Swap Signals is not supported for:

- Vector or differential pair signals
- If swapped signals are connected to pins with different parent differential pair pins which have terminations attached.
- If scalar or single-bit vector pin is connected to a multi-bit vector pin.
- Signals connected to pins that have different PIN_GROUP values.

To swap signals

1. Select the two signals to swap in the Component Connectivity Details pane.

Click to select the first signal and Control+Click to select the second signal.

For more information on using the Component Connectivity Details pane, see [Component Connectivity Details Pane](#) on page 54.

2. Right-click and choose *Swap Signals*.

Deleting Signals

To delete a signal from your design, perform the following steps.

1. Select a signal or a group of signals in the Signal List.
2. Press the *Delete* key.

Note the following:

- You cannot delete a signal that is connected to components in the design. If you want to delete a signal that is connected to a component, you must first delete the connection and then delete the signal.
- You cannot delete a bit of a signal in the Expanded Signal List.
- You cannot delete a global signal that is rippled up from a lower level block.

Modifying the Scope of a Signal

You can have signals with the scope LOCAL, GLOBAL, IN, OUT, or INOUT in your design.

To modify the scope of a signal

1. Select the signal in the Signal List.
2. Choose *Object – Change – Signal Scope*, then choose the new scope for the signal.

Note: If you want to change the scope of signals in a block in a hierarchical design, set the block as the root design and then change the scope of the signals in the block. For more information on setting a block as the root design, see [Setting the Root Design](#) on page 372. You cannot modify the scope of a signal when you are editing a block in master or context mode. For more information on editing blocks, see [Editing a Hierarchical Design](#) on page 356.

Modifying the Logical Name of a Signal

To modify the logical name of a signal

1. Select the signal in the Signal List.
2. Choose *Object – Change – Name*.

The *Name* field becomes editable.

3. Type the new name for the signal and press *Enter*.



Tip

You can also click on the logical name of a signal, press the *F2* key, and then modify the signal name.

Modifying the Physical Net Name of a Signal

System Connectivity Manager automatically generates a physical net name for all the signals added to a design. The physical net name corresponding to a signal is listed in the *Phys Name* column in the Signal List pane.

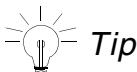
If required, you can modify the physical net names of signals.

Changing Physical Net Name

To modify the physical net name of a signal, complete the following steps.

1. Select the signal in the Signal List.
 2. Choose *Object – Change – Phys Name*.
- The *Phys Name* field becomes editable.
3. Type the new physical net name for the signal and press *Enter*.

Note: You cannot modify the physical net name of signals in the Expanded Signal List. For more information on using the Expanded Signal List, see [Viewing Bits of a Vector Signal in Signal List Pane](#) on page 151.



Tip

You can also click on the physical net name of a signal, press the *F2* key, and then modify the physical net name.

Regenerating Physical Net Name

In some designs, because of change in the vector notation used, the physical net names generated for signals in the design may not be in sync with the signal names.

- To modify the physical net names as per the naming convention used for naming signals, choose *Project – Regenerate Physical Net Names*.

The physical net names of signals are regenerated based on signal names.



Regenerate Physical Net Name command regenerates the physical net names that are auto-generated. User-specified physical net names are not modified.

Navigating a Signal

In complex hierarchical designs, a large number of signals may be aliased to each other in the same block or across different blocks. This makes it difficult to quickly identify the aliases of a signal and view their connectivity for debugging purposes.

You can use the Signal Navigate window to quickly view the aliases for a signal at all levels of a hierarchical design and navigate the signal to view its connectivity. For more information on using the Signal Navigate window, see [Using Signal Navigate](#) on page 226.

Working with Comments

The following procedures describe how you can use comments in your design.

- [Adding Comments](#) on page 169
- [Editing Comments](#) on page 170
- [Deleting Comments](#) on page 170

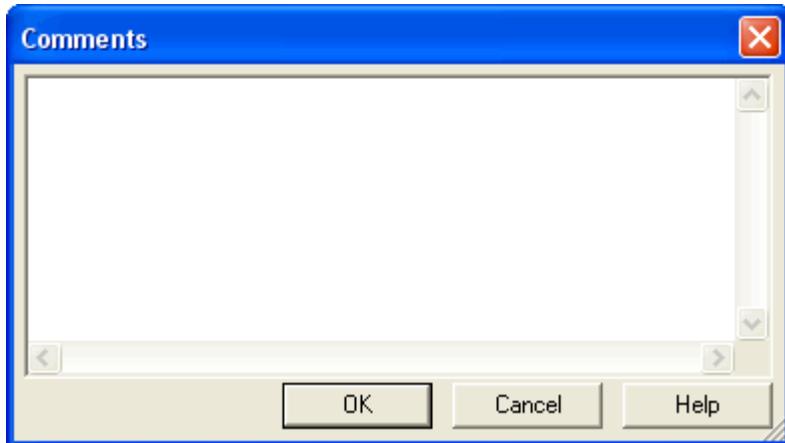
Adding Comments

You can add a comment to a component in the Component List, to a signal in the Signal List, or to a pin in Component Connectivity Details pane.

To add a comment

1. Select the component, signal or pin to which you want to add
2. Choose *Object – Comments – Insert Comment*.

The Comments dialog box appears.



3. Enter the comments and click *OK*.

The comment icon () next to a component, signal or pin indicates that a comment exists for the component, net or pin.

Viewing Comments

The comment icon () next to a component, signal or pin indicates that a comment exists for the component, net or pin.

To view the comment, hover the cursor on the comment icon () next to a component, signal or pin. The comment is displayed as a tooltip.

Editing Comments

To edit a comment:

1. Choose *Object – Comments – Edit Comment*.

The Comments dialog box appears with the existing comment selected.

2. Enter the new comments and click *OK*.

Deleting Comments

To delete a comment:

1. Select the row containing the comment.

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2. Choose *Object – Comments – Delete Comment.*

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Capturing Connectivity

For more information on using the Component Connectivity Details pane, see the following sections:

- [Capturing Pin-Net Connectivity for a Component](#) on page 174
- [Capturing Pin-Net Connectivity for Multiple Components](#) on page 177
- [Modifying Connectivity Simultaneously in Same Pane](#) on page 183
- [Connecting Component Pins to Vectored Signals](#) on page 185
- [Working with Connectivity on Vector Pins in the Component Connectivity Details Pane](#) on page 188
- [Using the Attach Signal Button to Capture Connectivity](#) on page 189
- [Deleting Pin-Signal Connectivity in the Component Connectivity Details Pane](#) on page 199
- [Assigning SI Models](#) on page 323 for information on assigning signal models to component pins.
- [Working with Unconnected Pins](#) on page 204

Capturing Pin-Net Connectivity for a Component

The Component Connectivity Details pane allows you to quickly connect signals to pins of components. The different ways in which you can connect signals to pins in the Component Connectivity Details pane are described below.

Note: For information on working with connectivity on vector pins, see [Working with Connectivity on Vector Pins in the Component Connectivity Details Pane](#) on page 188.

- Type the signal name in the *Signal* cell next to the pin and press *Enter*.

If the first few characters of the signal name you type match the name of an existing signal in the design, System Connectivity Manager automatically fills in the remaining characters for you. You can turn on or off automatic completion of signal names using the *Enable Auto Complete for Signal Names* check box in the [Spreadsheet Editor](#) tab of the [Setup](#) dialog box.

To connect the same signal to multiple pins, select the *Signal* cells next to the pins, type the signal name, then press *Enter*.

Note: If a signal with the same name does not exist in the current design, the signal is automatically added in the Signal List.

- Select a signal in the Signal List and drag and drop it on the *Signal* cell next to the pin.

To connect the same signal to multiple pins, do the following:

- a. Select the *Signal* cell next to the pins.
- b. Select the signal in the Signal List and drag and drop it on the Component Connectivity Details pane.

- Click in the *Signal* cell next to the pin, select the signal name from the drop-down list that displays all the available signals in the design, and press *Enter*.

To connect the same signal to multiple pins, select the *Signal* cells next to the pins, select the signal name from the drop-down list, and press *Enter*.

You can enable or disable the display of the drop-down list in the cells in the *Signal* column using the *Show Signal Combo Box in CCP signal column* check box in the [Spreadsheet Editor](#) tab of the [Setup](#) dialog box.

Note: By default, the *Show Signal Combo Box in CCP signal column* check box in the [Spreadsheet Editor](#) tab of the [Setup](#) dialog box is not selected.

- Click in the *Signal* cell next to the pin, press *Alt + Down Arrow* and select the signal name from the drop-down list that displays all the available signals in the design, then press *Enter*.

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Capturing Connectivity

To connect the same signal to multiple pins, select the *Signal* cells next to the pins, press *Alt + Down Arrow* and select the signal name from the drop-down list, then press *Enter*.

- Click in the *Signal* cell next to the pin and use the *Attach Signal* button  or the *Attach Signal* drop-down list.

For more information on using the *Attach Signal* button, see [Using the Attach Signal Button to Capture Connectivity](#) on page 189.

- Copy a pin name and paste it in the *Signal* cell next to the pin. You can do this if you want to connect the pin to a signal that has the same name as the pin name.

To connect multiple pins to signals that have the same name as the pin name of each of the selected pins, do the following:

- a. Select the pin names as shown below, and choose *Edit – Copy* to copy the pin names.

Pin Name	Pin Number	Pin Type	Signal ▾
*	*	*	*
a	1	Input	
a	9	Input	
b	2	Input	
b	10	Input	
cext	14	Input	
cext	6	Input	
q	13	Output	
q	5	Output	
rext/cext	15	Input	
rext/cext	7	Input	
clr *	3	Input	
clr *	11	Input	
q *	4	Output	
q *	12	Output	

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Capturing Connectivity

- b.** Click in the *Signal* cell next to the first pin you selected, as shown below, and choose *Edit – Paste*.

Pin Name	Pin Number	Pin Type	Signal ▾
*	*	*	*
a	1	Input	
a	9	Input	
b	2	Input	
b	10	Input	
cext	14	Input	
cext	6	Input	
q	13	Output	
q	5	Output	
rext/cext	15	Input	
rext/cext	7	Input	
clr *	3	Input	
clr *	11	Input	
q *	4	Output	
q *	12	Output	

- Copy a signal from the Signal List or the *Signal* column in the Component Connectivity Details pane and paste it in the *Signal* cell next to the pin.

- To connect the same signal to multiple pins, copy the signal from the Signal List or the *Signal* column in the Component Connectivity Details pane, select the *Signal* cell next to the pins, then choose *Edit – Paste*.
- To connect different signals to different pins, copy the signals from the Signal List or the *Signal* column in the Component Connectivity Details pane, select the *Signal* cell next to the pins, then choose *Edit – Paste*.

Note: Ensure that the number of signals you copied from the Signal List and the number of pins you selected in the Component Connectivity Details pane are the same.

- Paste connectivity information from another component by doing the following:

- a.** In the Component List, click on the component from which you want to copy the connectivity information.

The connectivity information for the component is displayed in the Component Connectivity Details pane.

- b.** Copy the required signals from the *Signal* column in the Component Connectivity Details pane.
- c.** In the Component List, click on the component on which you want to paste the connectivity information.

The connectivity information for the component is displayed in the Component Connectivity Details pane.

- d. Select the *Signal* cell next to the first pin from which you want to paste the signals.
- e. Paste the information.

Note: You can also use the *Paste Special* command to modify the names of the signals you copied and then paste the signals. For more information on using the *Paste Special* command, see [Using Paste Special in the Component Connectivity Details Pane](#) on page 159.

- Paste the signal names from another application such as Microsoft Excel.

Note: When pasting signals names in the *Signal* column in the Component Connectivity Details pane, you can choose *Edit – Paste Special* to modify the signal names you copied before pasting them. For more information on using Paste Special, see [Using Paste Special in the Component Connectivity Details Pane](#) on page 159.

Note: If you enter or paste a signal name that does not exist in the current design in the *Signal* column of the Component Connectivity Details pane, the signal name is automatically added in the Signal List for the current design.



Tip
You can also add connectivity using multiple connectivity panes. By combining multi-select operation in multiple connectivity panes, you can make fast connectivity assignments. For example, you can add some connectivity to a group of components. Next, you can add the same connectivity to a subset of pins of a component.

Capturing Pin-Net Connectivity for Multiple Components

You can use the Component Connectivity Details pane to edit the pin-signal connectivity information of multiple components in different panes within the Component Connectivity Details pane at the same time. This allows you to quickly capture connectivity information on components that require similar connectivity.

Modifying Connectivity Simultaneously in Different Panes

To open the Component Connectivity Details pane to simultaneously edit pin-signal connectivity of multiple components in different panes at the same time, perform the following steps.

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Capturing Connectivity

1. Select the components in the Component List.

2. Do one of the following:

- Press *Enter*.
- Choose *Object – Edit Connectivity*.

The Pin Name and Signal columns for the selected components are displayed in different panes within the Component Connectivity Details pane as shown below:

Figure 6-1 Component Connectivity Details Pane: Different Panes for Multiple Instances of Same Component

The screenshot shows the 'Component Connectivity Details' pane with two separate sections for component instances:

- i2 (epf8282a) - U2**: This section contains a table with 'Pin Name' and 'Signal' columns. It lists various pins: add[13..1], add[13], add[10], add[7], add[4], add[3], bd[7..0], clkusr, conf_done, data2, data3, data4, data5, ddk, DP_data, DP_msel, gain, i/o, inputa, inputb, inputc, input, nconfig, ncs. The 'Signal' column for data2 is highlighted.
- i8 (epf8282a) - U7**: This section also contains a table with 'Pin Name' and 'Signal' columns. It lists: ADDRESS[7..0], data2, data3, data4, data5, ddk, DS_data, pc_web.

At the bottom left of the pane, there are buttons for 'Component' and 'Multiple Selection'.

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Capturing Connectivity

In the above figure, the *Pin Name* column is displayed only once because you have selected two instances of the same component `epf8282a` in the Component List. As both the instances have the same pin names, the *Pin Name* column is displayed only once in the Component Connectivity Details pane.

If you select different components in the Component List, the Pin Name column is displayed for each component in the Component Connectivity Details pane as shown below:

Figure 6-2 Component Connectivity Details Pane: Different Panes for Multiple Instances of Different Components

Component Connectivity Details	
<input type="text"/> Attach Signal: <input type="button" value="fx"/> =PINNAME	
i1 (idf_cspu_877) - U1 Functions: All	<input type="checkbox"/> Expand All Pins <input checked="" type="checkbox"/> Show Differential Pairs <input checked="" type="checkbox"/> Show
Pin Name	Signal
*	*
+ DP_ck	DP_ck
+ DP_fbin	DP_fbin
+ DP_fbout	DP_fbout
+ DP_y0	DP_y0
+ DP_y1	DP_y1
+ DP_y2	DP_y2
+ DP_y3	DP_y3
+ DP_y4	DP_y4
+ DP_y5	DP_y5
+ DP_y6	DP_y6
+ DP_y7	DP_y7
+ DP_y8	DP_y8
+ DP_y9	DP_y9
+ nc[7..0]	nc
oe	oe
os	os

Component Connectivity Details	
<input type="text"/> Attach Signal: <input type="button" value="fx"/> =PINNAME	
i2 (epf8282a) - U2 Functions: All	<input type="checkbox"/> Expand All Pins <input checked="" type="checkbox"/> Show Differential Pairs <input checked="" type="checkbox"/> Show
Pin Name	Signal
*	*
+ bd[7..0]	ADDRESS[7..0]
clkusr	
conf_done	
data2	data2
data3	data3
data4	data4
data5	data5
dclk	dclk
+ DP_data	DS_data
+ DP_msel	
gain	
i/o	pc_web
inputa	
inputb	
inputc	
input	
nconfig	
ncs	
nrs	
nsp	
nstatus	
nrst	
nws	

In the above figure, the Component Connectivity Details pane displays the Pin Name column for each component because you selected different components (`idf_cspu_877` and `epf8282a`) in the Component List.

To edit the pin-signal connectivity of multiple components in different panes at the same time

The different ways in which you can connect signals to pins when you are editing the pin-signal connectivity of multiple components at the same time in different panes within the Component Connectivity Details pane are described below.

Note: You can use the *Ctrl* key to select multiple pin names of each component, or to select the *Signal* cells next to pins of each component, when you are editing the pin-signal connectivity of multiple components at the same time in the Component Connectivity Details pane.

Note: For information on working with connectivity on vector pins, see [Working with Connectivity on Vector Pins in the Component Connectivity Details Pane](#) on page 188.

- To connect the same signal to pins of multiple components, do one of the following:
 - Select the *Signal* cells next to the pins of each component, type the signal name and press *Enter*.

If the first few characters of the signal name you type match the name of an existing signal in the design, System Connectivity Manager automatically fills in the remaining characters for you. You can turn on or off automatic completion of signal names using the *Enable Auto Complete for Signal Names* check box in the [Spreadsheet Editor](#) tab of the [Setup](#) dialog box.

Note: If a signal with the same name does not exist in the current design, the signal is automatically added in the Signal List.

- Select the *Signal* cells next to the pins of each component, select the signal in the Signal List and drag and drop it on the Component Connectivity Details pane.
- Select the *Signal* cells next to the pins of each component, select the signal name from the drop-down list, then press *Enter*.

You can enable or disable the display of the drop-down list in the cells in the *Signal* column using the *Show Signal Combo Box in CCP signal column* check box in the [Spreadsheet Editor](#) tab of the [Setup](#) dialog box.

Note: By default, the *Show Signal Combo Box in CCP signal column* check box in the [Spreadsheet Editor](#) tab of the [Setup](#) dialog box is not selected.

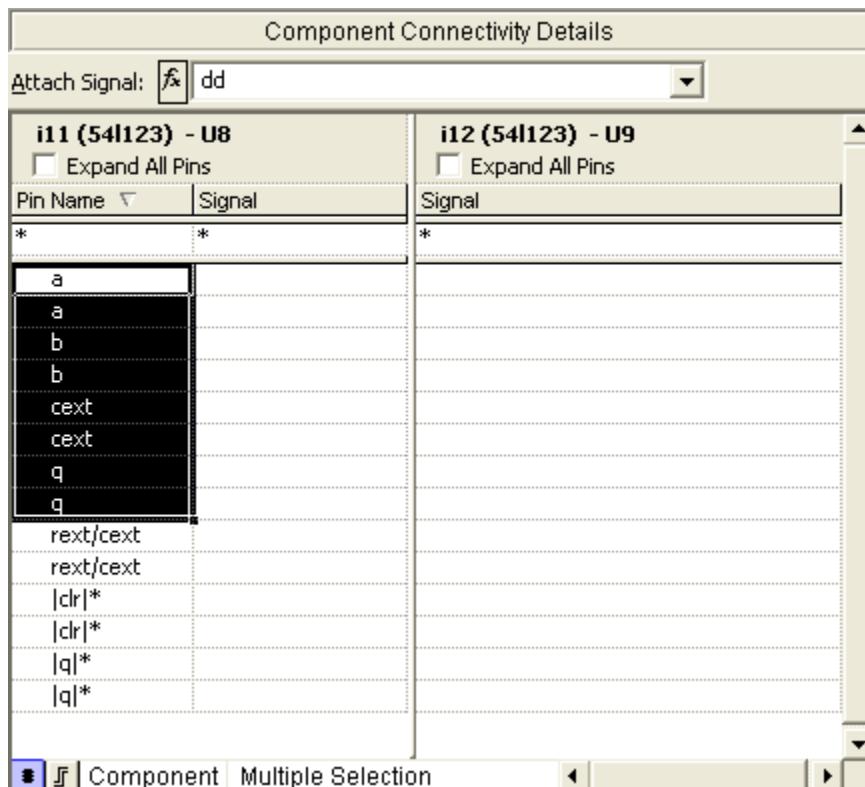
- Select the *Signal* cells next to the pins of each component, press *Alt + Down Arrow* and select the signal name from the drop-down list, then press *Enter*.
- Select the *Signal* cells next to the pins of each component and select the signal name from the *Attach Signal* drop-down list.

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For more information on using the *Attach Signal* drop-down list, see [Using the Attach Signal Button to Capture Connectivity](#) on page 189.

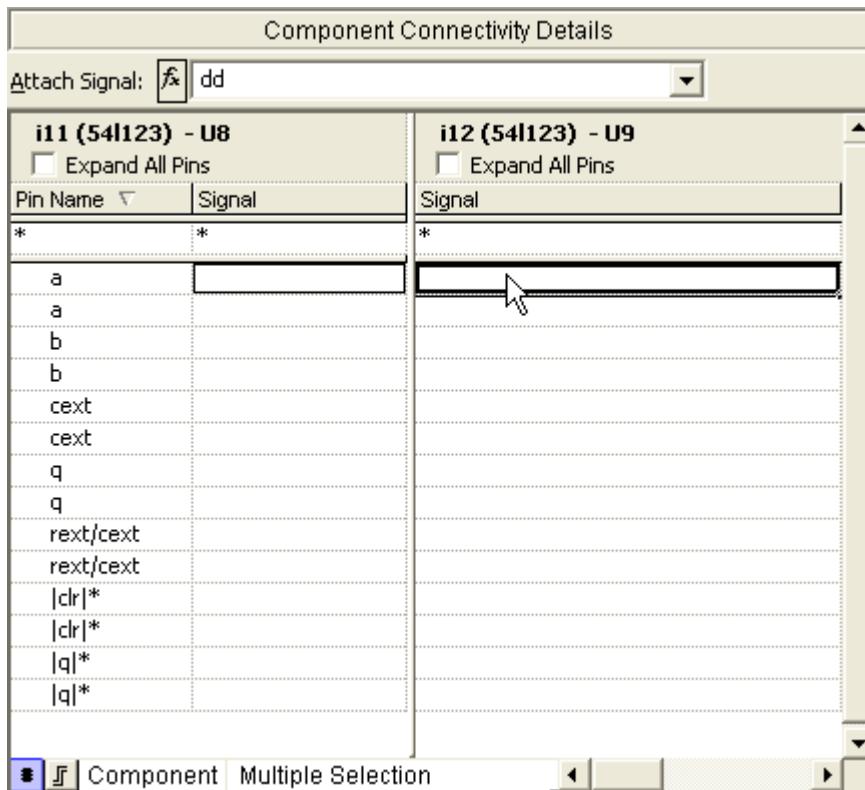
- ❑ Copy the signal from the Signal List or in the *Signal* column in the Component Connectivity Details pane, select the *Signal* cell next to the pins of each component, then choose *Edit – Paste*.
 - Click in the *Signal* cell next to the pins of each component and use the *Attach Signal* button.
- For more information on using the *Attach Signal* button, see [Using the Attach Signal Button to Capture Connectivity](#) on page 189.
- To connect multiple pins of each component instance to signals that have the same name as the pin name of each of the selected pins, do the following:
 - a. Select the pin names as shown below, and choose *Edit – Copy* to copy the pin names.



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- b. Press the *Ctrl* key, and for each component instance, click in the *Signal* cell next to the first pin you selected, as shown below, and choose *Edit – Paste*.



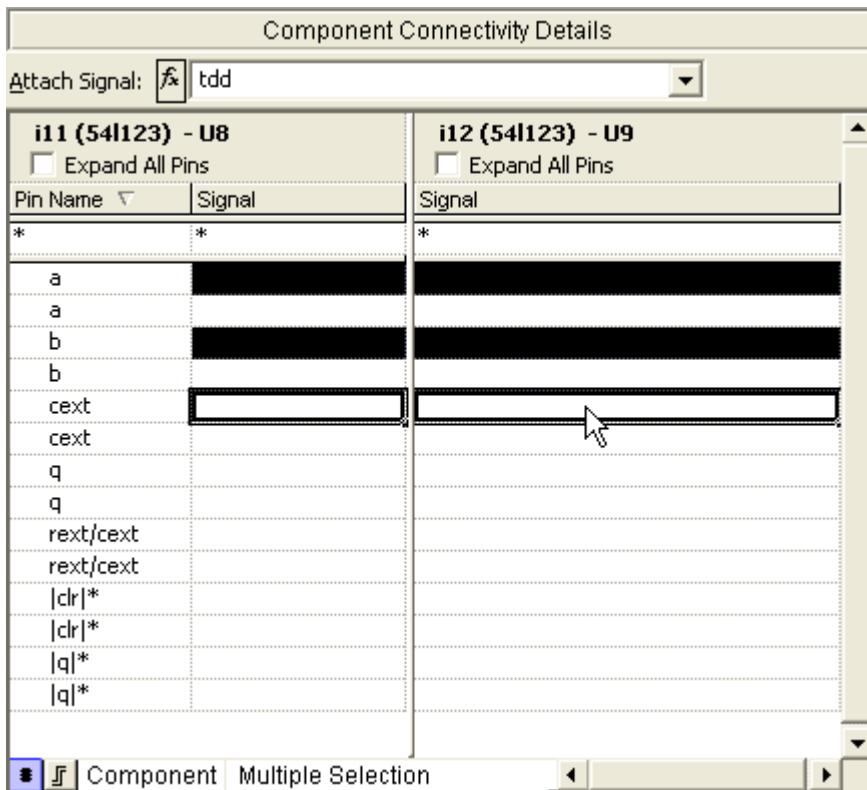
- To connect different signals to different pins of each component, copy the signals from the Signal List or the *Signal* column in the Component Connectivity Details pane, select the *Signal* cell next to the pins of each component, then choose *Edit – Paste*.

Note: Ensure that the number of signals you copied in the Signal List and the number of pins you selected in the Component Connectivity Details pane for each component are the same. For example, if you have copied three signals from the Signal List, you must

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select the *Signal* cells next to only three pins of each component as shown below.



- Paste the signal names from another application such as Microsoft Excel.

Note: When pasting signals names in the *Signal* column in the Component Connectivity Details pane, you can choose *Edit – Paste Special* to modify the signal names you copied before pasting them. For more information on using Paste Special, see [Using Paste Special in the Component Connectivity Details Pane](#) on page 159.

Note: If you enter or paste a signal name that does not exist in the current design in the *Signal* column of the Component Connectivity Details pane, the signal name is automatically added in the Signal List for the current design.

Modifying Connectivity Simultaneously in Same Pane

You can use the Component Connectivity Details pane to edit the connectivity information of multiple components in the same pane in the Component Connectivity Details pane at the same time. This allows you to quickly edit the connectivity information for a group of components at the same time.

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To open the Component Connectivity Details pane to edit connectivity information of multiple components in the same pane at the same time, complete the following step.

1. Select the components in the Component List.
2. Choose *Object – Edit Connectivity in Same Pane*.

The connectivity information for the selected components are displayed in the same pane within the Component Connectivity Details pane as shown below:

Figure 6-3 Component Connectivity Details Pane: Same Pane for Multiple Components

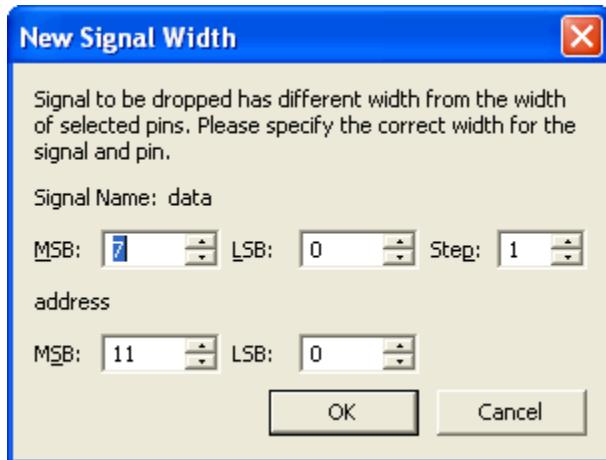
The screenshot shows the 'Component Connectivity Details' pane with the title bar 'Component Connectivity Details'. Below it is a dropdown menu labeled 'Attach Signal: f =AUTONAME'. A section titled 'Multiple Instances' contains a checkbox 'Expand All Pins'. The main area is a table with columns: Instance, Ref Des, Pin Name, Pin Number, Pin Type, Signal, Termination, and two icons. The table lists various pins for instances i2 and i3. For instance i2, pins include address<11..0>, afd, afs, cclock, d1_7, d1_8, d2_5, d2_6, data<15..0>, g1, g2, iord, iowr, mrd, mready, mwr, reset, rfd, rfs, and s1. For instance i3, pins include 7, 8, 5, 6, 2, 4, A5, A6, J6, A2, J5, A4, J3, J2, and 1. The table has scroll bars on the right and bottom. At the bottom, there are tabs for 'Component' and 'Multiple Selection'.

Instance	Ref Des	Pin Name	Pin Number	Pin Type	Signal	Termination		
*	*	*	*	*	*	*	*	*
i2	U4	address<11..0>	B6,B7,B8...	Output				
i2	U4	afd	A9	Input				
i2	U4	afs	A8	Input				
i2	U4	cclock	A3	Input				
i3	U18	d1_7	7	Inout				
i3	U18	d1_8	8	Inout				
i3	U18	d2_5	5	Inout				
i3	U18	d2_6	6	Inout				
i2	U4	data<15..0>	H2,H1,G...	Output				
i3	U18	g1	2	Inout				
i3	U18	g2	4	Inout				
i2	U4	iord	A5	Input				
i2	U4	iowr	A6	Input				
i2	U4	mrd	J6	Input				
i2	U4	mready	A2	Input				
i2	U4	mwr	J5	Input				
i2	U4	reset	A4	Input				
i2	U4	rfd	J3	Input				
i2	U4	rfs	J2	Input				
i3	U18	s1	1	Inout				

In the above figure, the connectivity information of instances i2 and i3 in the design are displayed in the same pane in the Component Connectivity Details pane. This lets you modify the pin-signal connectivity, apply terminations, add pullups and pulldowns, assign signal integrity models, and add comments for pins of multiple components at the same time.

Connecting Component Pins to Vectored Signals

If the width of a signal does not match the width of the pin to which you are connecting the signal, the New Signal Width dialog box appears. For example, if you connect a signal `data<7..0>` to a pin `address<11..0>`, the New Signal Width dialog box appears as shown below:



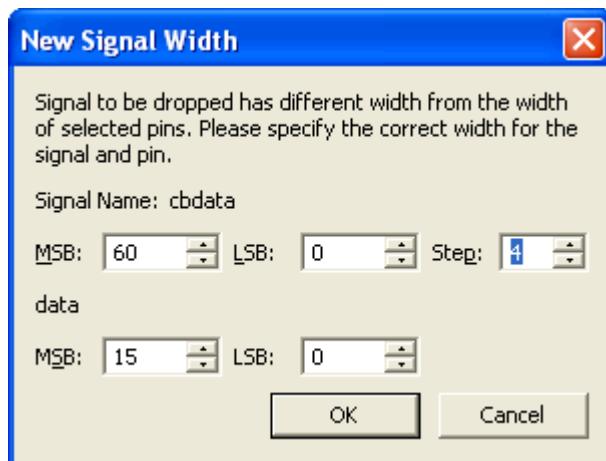
The following examples describe how to use the New Signal Width dialog box.

- To connect the signal `data<7..0>` to the bits `address<7..0>` of the pin, enter 7 in the *MSB* field for the pin and click *OK*.
- To connect the signal `data<7..0>` to the bits `address<11..4>` of the pin, enter 11 in the *MSB* field for the pin, enter 4 in the *LSB* field for the pin and click *OK*.
- To connect the signal `data<3..0>` to the bits `address<3..0>` of the pin, enter 3 in the *MSB* fields for the signal and the pin, enter 0 in the *LSB* fields for the signal pin and click *OK*.
- To change the width of the signal `data<7..0>` to `data<11..0>`, enter 11 in the *MSB* field for the signal and click *OK*. The signal is automatically renamed to `data<11..0>` in the Signal List pane and connected to the pin `address<11..0>`.

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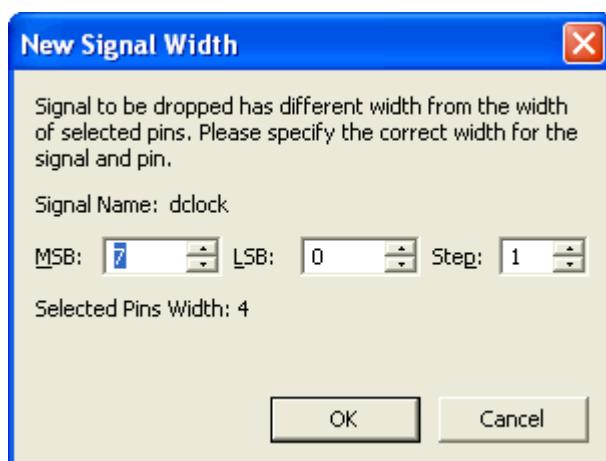
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- To connect the signal `cbdata<60..0>` with the step size 4 to a pin `data<15..0>`, enter the step size as 4 in the New Signal Width dialog box, as shown below:



Note: You can also enter the signal name `cbdata<60..0:4>` in the *Signal* cell next to the pin `data<15..0>` in the Component Connectivity Details pane to use the step size 4 to connect the signal to the pin. For more information on using step size in signal names, see [Using Step Size to Connect or Alias Vectored Signals](#).

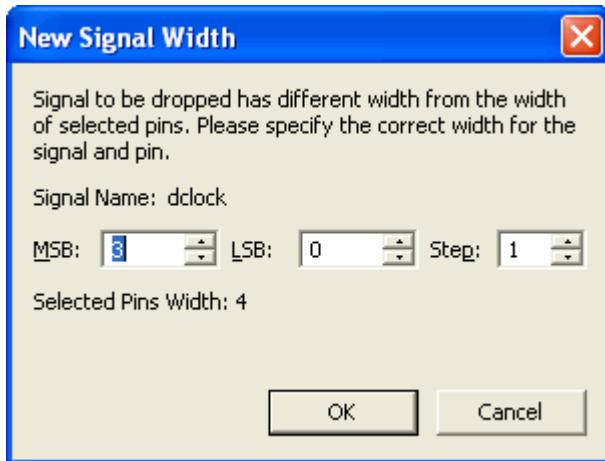
- If you select multiple pins in the Component Connectivity Details pane and enter the name of a vectored signal in the *Signal* column in the Component Connectivity Details pane or select the vectored signal in the Signal List and drag and drop it on the Component Connectivity Details pane, the New Signal Width dialog box appears as shown below:



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In the above figure the vectored signal `dclock<7..0>` has the width 8 and the pins selected in the Component Connectivity Details pane have the total width of 4. To connect the signal to the pin, change the MSB of the signal to 3 as shown below:



Using Step Size to Connect or Alias Vectored Signals

You use bit subscripts to specify the number of bits that a signal represents and to identify the bits when you connect a signal to a pin in the Component Connectivity Details pane or when you alias two vectored signals.

Syntax

```
<bit1..bit2:step>  
<bit1:bit2:step>
```

The syntax specifies a sub-range of bits beginning with bit1 or bit2, whichever is the LSB, and including every bit that is step bits apart up to bit1. The step value is usually a positive integer. Use a negative integer to reverse the bit order. A step value of 1 is equivalent to no step value.

Examples

Subscript	Result
<code><31..0:2></code>	30 28 26 ... 6 4 2 0
<code><11..0:4></code>	8 4 0

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Subscript	Result
<9:1:3>	7 4 1
<0..31:-1>	31 30 29 ... 3 2 1 0
<15..0:20>	0
<0..6:-2>	0 2 4 6
<0..7:-2>	0 2 4 6

For example DATA<60..0:4> or DATA<60:0:4> results in the bits

DATA[60], DATA[56], DATA[52], DATA[48], DATA[44], DATA[40], DATA[36], DATA[32], DATA[28], DATA[24], DATA[20], DATA[16], DATA[12], DATA[8], DATA[4], DATA[0].

Working with Connectivity on Vector Pins in the Component Connectivity Details Pane

- If you connect a scalar signal to a vector pin, all the bits of the vector pin are connected to the scalar signal. For example, if you connect a scalar signal CLOCK to a vector pin CCLOCK<7..0>, all the bits of the vector pin are connected to the signal CLOCK.
- If the bits of a vector pin are connected to different signals, the signals connected to the bits are separated by commas and displayed in the *Signal* field next to the vector pin, as shown below:

Pin Name /	Pin Number	Pin Type	Signal
*	*	*	*
⊕ address<11..0>	B6,B7,B8,...	Output	address<11..0>
afd	A9	Input	afd
afs	A8	Input	afs
cclock	A3	Input	cclock
⊕ data<15..0>	H2,H1,G1...	Output	addr,rdf,rdd,cbdata,cbdata,...

If the above figure, the bits of the vector pin data<15..0> are connected to different signals. The signal names are separated by commas. To view the connections to each bit of the vector pin, do one of the following:

- Expand the vector pin by clicking the ⊕ icon next to the vector pin name.

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- Hover the cursor on the *Signal* field next to the vector pin. A tooltip displays the connectivity of the bits of the vector pin as shown below.

Pin Name	Pin Number	Pin Type	Signal	Te
*	*	*	*	*
+ address<11..0>	B6,B7,B8,...	Output	address<11..0>	
afd	A9	Input	afd	
afs	A8	Input	afs	
cclock	A3	Input	cclock	
+ data<15..0>	H2,H1,G1...	Output	addr,rdf,rdd,cbdata,cbdata,...	
iord	A5	Input	iord	
iowr	A6	Input	iowr	
mrd	J6	Input	mrd	
mready	A2	Input	mread	
mwr	J5	Input	mwr	
reset	A4	Input	reset	
rfd	J3	Input	rfd	
rfs	J2	Input	rfs	
sclock	A7	Input	sclock	
sel	A1	Output	sel	
set1	H8	Output	set1	
set2	H3	Output	set2	
set	H9	Output	set	

Connection Details
data<15>;addr
data<14>;rdf
data<13>;rdd
data<12>;cbdata
data<11>;cbdata
data<10>;cbdata
data<9>;cbdata
data<8>;cbdata
data<7>;cbdata
data<6>;cbdata
data<5>;cbdata
data<4>;cbdata
data<3>;cbdata
data<2>;cbdata
data<1>;cbdata
data<0>;cbdata

In the above figure, the tooltip displays the names of signals connected to each bit of the vector pin `data<15..0>`.

Using the Attach Signal Button to Capture Connectivity

This section describes the procedures for using the Attach Signal button and drop-down list in the Component Connectivity Details pane.

- [Using the Attach Signal Button](#)
- [Using the Attach Signal Drop-Down List](#)

Using the Attach Signal Button

The button lets you use functions to automatically generate the signal names for the selected pins in the Component Connectivity Details pane.

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To use functions to automatically generate signal names for pins in the Component Connectivity Details pane:

1. Do one of the following:

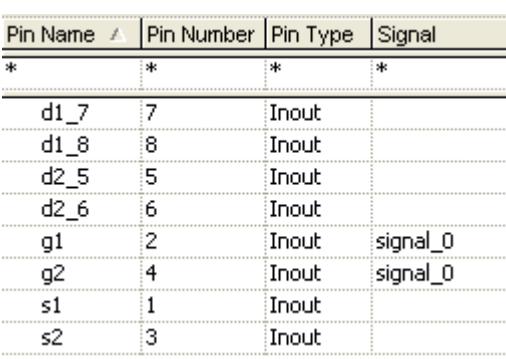
- Select the pin name of the pins for which you want to automatically generate signal names.
- Select the *Signal* cell next to the pins for which you want to automatically generate signal names.

2. Click  and choose the function you want to use to automatically generate signal names for the selected pins.

Note: If a selected pin is already connected to a signal, choosing a function will overwrite the signal connected to the pin.

The following table describes the functions you can choose when you click  and the equivalent functions you can select in the *Attach Signal* drop-down list.

Table 6-1 Functions for Automatically Generating Signal Names

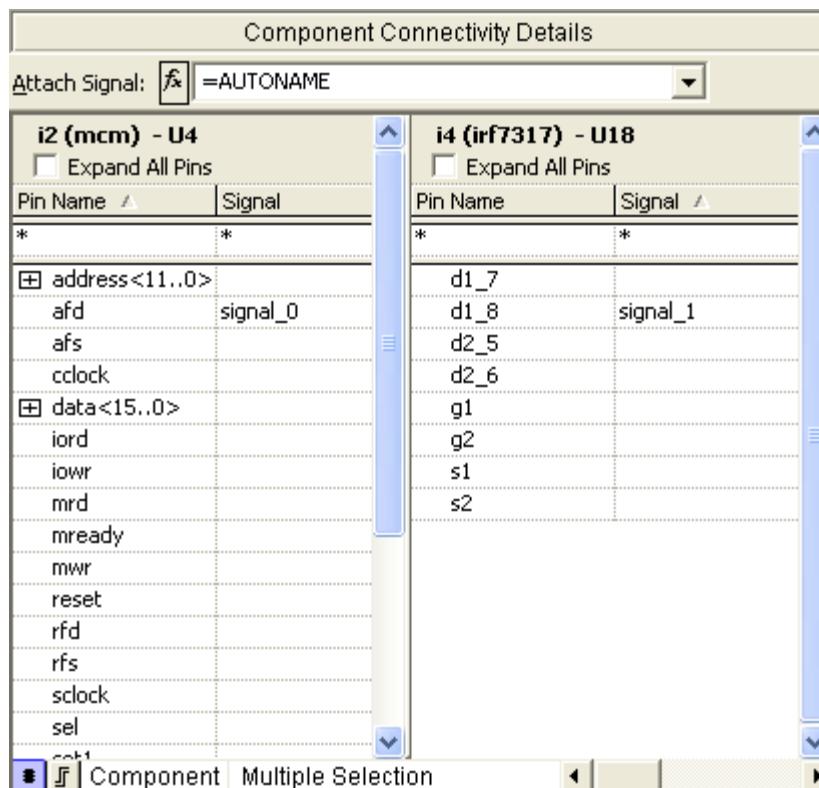
Function	Description																																								
Short Pins	Shorts the selected pins by connecting them to a signal with the same name. In Attach Signal drop-down list, select:																																								
=SHORTPINS	 <table border="1"><thead><tr><th>Pin Name</th><th>Pin Number</th><th>Pin Type</th><th>Signal</th></tr></thead><tbody><tr><td>*</td><td>*</td><td>*</td><td>*</td></tr><tr><td>d1_7</td><td>7</td><td>Inout</td><td></td></tr><tr><td>d1_8</td><td>8</td><td>Inout</td><td></td></tr><tr><td>d2_5</td><td>5</td><td>Inout</td><td></td></tr><tr><td>d2_6</td><td>6</td><td>Inout</td><td></td></tr><tr><td>g1</td><td>2</td><td>Inout</td><td>signal_0</td></tr><tr><td>g2</td><td>4</td><td>Inout</td><td>signal_0</td></tr><tr><td>s1</td><td>1</td><td>Inout</td><td></td></tr><tr><td>s2</td><td>3</td><td>Inout</td><td></td></tr></tbody></table>	Pin Name	Pin Number	Pin Type	Signal	*	*	*	*	d1_7	7	Inout		d1_8	8	Inout		d2_5	5	Inout		d2_6	6	Inout		g1	2	Inout	signal_0	g2	4	Inout	signal_0	s1	1	Inout		s2	3	Inout	
Pin Name	Pin Number	Pin Type	Signal																																						
*	*	*	*																																						
d1_7	7	Inout																																							
d1_8	8	Inout																																							
d2_5	5	Inout																																							
d2_6	6	Inout																																							
g1	2	Inout	signal_0																																						
g2	4	Inout	signal_0																																						
s1	1	Inout																																							
s2	3	Inout																																							

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Table 6-1 Functions for Automatically Generating Signal Names, *continued*

Function	Description
Auto Name	Automatically assigns signal names to the selected pins. The signals are named <code>signal_0</code> , <code>signal_1</code> , and so on.
In Attach Signal drop-down list, select:	Note the following: <ul style="list-style-type: none"> ■ If you are editing pin-signal connectivity of multiple components in different panes at the same time and use the <i>Auto Name</i> function for two pins selected across different panes, different signals are assigned to the selected pins, as shown below.
=AUTONAME	



For example, in the above figure, the `af0` pin of the `mcm` component is connected to the signal named `signal_0` and the `d1_8` pin of the `irf7317` component is connected to the signal named `signal_1`.

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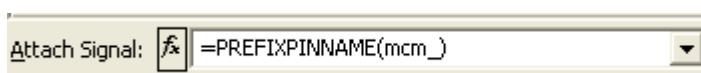
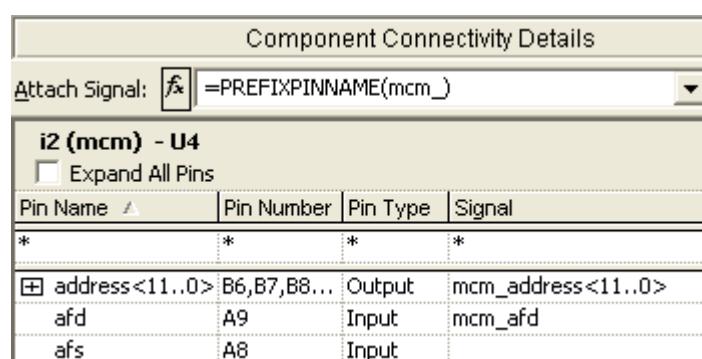
Table 6-1 Functions for Automatically Generating Signal Names, *continued*

Function	Description
Same As Pin Name	Automatically connects the selected pin to a signal that has the same name as the pin name of the pin.
In Attach Signal drop-down list, select: =PINNAME	For example, if the pin name is <code>data<15..0></code> , the signal <code>data<15..0></code> is automatically connected to it.

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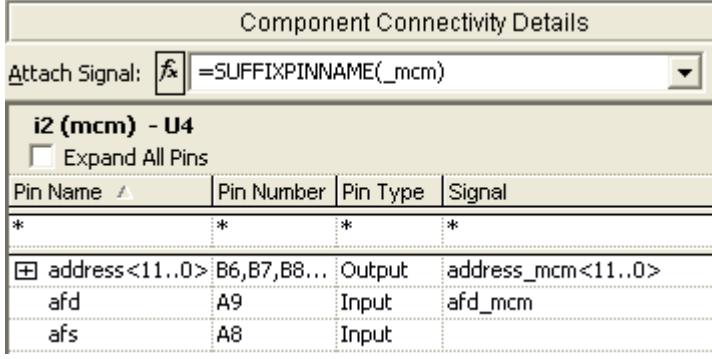
Table 6-1 Functions for Automatically Generating Signal Names, *continued*

Function	Description
Prefix Pin Name In Attach Signal drop-down list, select: =PREFIXPINNAME(<string>)	<p>Automatically connects the selected pin to a signal that has the same name as the pin name of the pin and with the specified prefix.</p> <p>1. When you choose the <i>Prefix Pin Name</i> function, the <i>Attach Signal</i> drop-down list appears as shown below.</p>  <p>2. Replace <i><string></i> with the prefix you want to use for the signals. For example, in the following figure, <i>mcm_</i> is specified as the prefix.</p>  <p>3. Press <i>Enter</i>.</p> <p>The pins are automatically connected to signals that have the same name as the pin names of the pins and with the prefix you specified in the <i>Attach Signal</i> drop-down list.</p>  <p>In the above example, the pin <i>address<11..0></i> is connected to a signal name <i>mcm_address<11..0></i>, where <i>mcm_</i> is the prefix you specified in the <i>Attach Signal</i> drop-down list and <i>address<11..0></i> is the pin name of the pin.</p>

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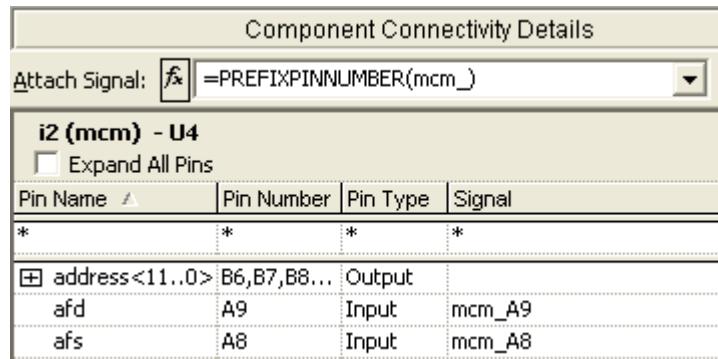
Table 6-1 Functions for Automatically Generating Signal Names, *continued*

Function	Description																				
Suffix Pin Name In Attach Signal drop-down list, select: =SUFFIXPINNAME(<string>)	Automatically connects the selected pin to a signal that has the same name as the pin name of the pin and with the specified suffix. <ol style="list-style-type: none"> When you choose the <i>Suffix Pin Name</i> function, the <i>Attach Signal</i> drop-down list appears as shown below.  <ol style="list-style-type: none"> Replace <string> with the suffix you want to use for the signals. Press <i>Enter</i>. <p>The pins are automatically connected to signals that have the same name as the pin names of the pins and with the suffix you specified in the <i>Attach Signal</i> drop-down list.</p>  <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">Pin Name</th> <th style="text-align: left;">Pin Number</th> <th style="text-align: left;">Pin Type</th> <th style="text-align: left;">Signal</th> </tr> </thead> <tbody> <tr> <td>*</td> <td>*</td> <td>*</td> <td>*</td> </tr> <tr> <td>[+] address<11..0></td> <td>B6,B7,B8...</td> <td>Output</td> <td>address_mcm<11..0></td> </tr> <tr> <td>afd</td> <td>A9</td> <td>Input</td> <td>afd_mcm</td> </tr> <tr> <td>afs</td> <td>A8</td> <td>Input</td> <td></td> </tr> </tbody> </table> <p>In the above example, the pin <code>address<11..0></code> is connected to a signal name <code>address_mcm<11..0></code>, where <code>_mcm</code> is the suffix you specified in the <i>Attach Signal</i> drop-down list and <code>address<11..0></code> is the pin name of the pin.</p>	Pin Name	Pin Number	Pin Type	Signal	*	*	*	*	[+] address<11..0>	B6,B7,B8...	Output	address_mcm<11..0>	afd	A9	Input	afd_mcm	afs	A8	Input	
Pin Name	Pin Number	Pin Type	Signal																		
*	*	*	*																		
[+] address<11..0>	B6,B7,B8...	Output	address_mcm<11..0>																		
afd	A9	Input	afd_mcm																		
afs	A8	Input																			

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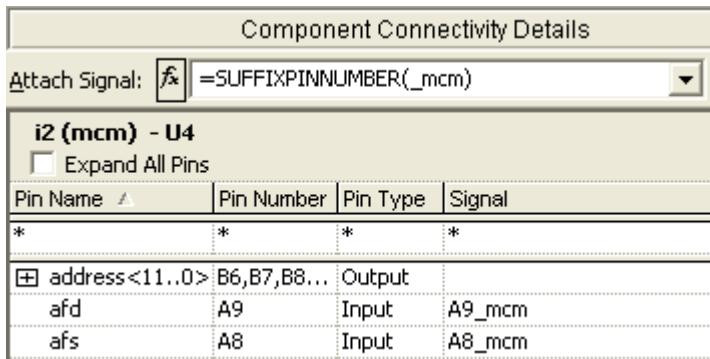
Table 6-1 Functions for Automatically Generating Signal Names, *continued*

Function	Description
Prefix Pin Number In Attach Signal drop-down list, select: =PREFIXPINNUMBER(<string>)	<p>Automatically connects the selected pin to a signal that has the same name as the pin number of the pin and with the specified prefix.</p> <p>1. When you choose the <i>Prefix Pin Number</i> function, the <i>Attach Signal</i> drop-down list appears as shown below.</p>  <p>2. Replace <string> with the prefix you want to use for the signals.</p> <p>3. Press <i>Enter</i>.</p> <p>The pins are automatically connected to signals that have the same name as the pin numbers of the pins and with the prefix you specified in the <i>Attach Signal</i> drop-down list.</p>  <p>In the above example, the pin <code>afd</code> is connected to a signal name <code>mcm_A9</code>, where <code>mcm_</code> is the prefix you specified in the <i>Attach Signal</i> drop-down list and <code>A9</code> is the pin number of the pin.</p>

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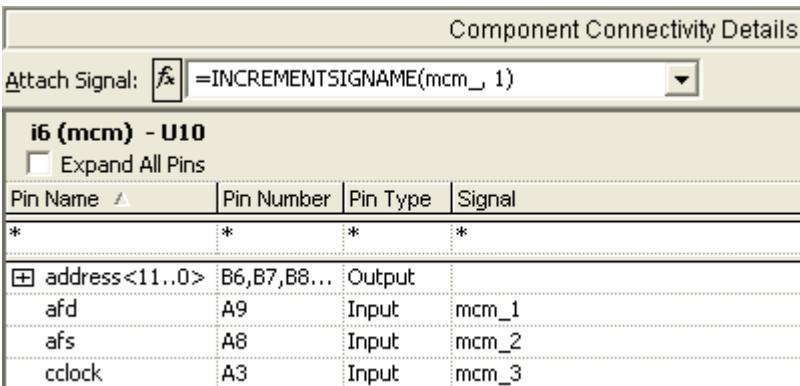
Table 6-1 Functions for Automatically Generating Signal Names, *continued*

Function	Description																				
Suffix Pin Number In Attach Signal drop-down list, select: =SUFFIXPINNUMBER(<string>)	<p>Automatically connects the selected pin to a signal that has the same name as the pin name of the pin and with the specified suffix.</p> <p>1. When you choose the <i>Suffix Pin Number</i> function, the <i>Attach Signal</i> drop-down list appears as shown below.</p>  <p>2. Replace <string> with the suffix you want to use for the signals.</p> <p>3. Press <i>Enter</i>.</p> <p>The pins are automatically connected to signals that have the same name as the pin numbers of the pins and with the suffix you specified in the <i>Attach Signal</i> drop-down list.</p>  <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">Pin Name</th> <th style="text-align: left;">Pin Number</th> <th style="text-align: left;">Pin Type</th> <th style="text-align: left;">Signal</th> </tr> </thead> <tbody> <tr> <td>*</td> <td>*</td> <td>*</td> <td>*</td> </tr> <tr> <td>address<11..0></td> <td>B6,B7,B8...</td> <td>Output</td> <td></td> </tr> <tr> <td>afd</td> <td>A9</td> <td>Input</td> <td>A9_mcm</td> </tr> <tr> <td>afs</td> <td>A8</td> <td>Input</td> <td>A8_mcm</td> </tr> </tbody> </table> <p>In the above example, the pin afd is connected to a signal name A9_mcm, where _mcm is the suffix you specified in the <i>Attach Signal</i> drop-down list and A9 is the pin number of the pin.</p>	Pin Name	Pin Number	Pin Type	Signal	*	*	*	*	address<11..0>	B6,B7,B8...	Output		afd	A9	Input	A9_mcm	afs	A8	Input	A8_mcm
Pin Name	Pin Number	Pin Type	Signal																		
*	*	*	*																		
address<11..0>	B6,B7,B8...	Output																			
afd	A9	Input	A9_mcm																		
afs	A8	Input	A8_mcm																		

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Table 6-1 Functions for Automatically Generating Signal Names, *continued*

Function	Description																								
Increment Signal Name In Attach Signal drop-down list, select: =INCREMENTSIGNAME(<signal, start_num>)	<p>Automatically connects the selected pins to the specified signal name that increments from the starting number you specify.</p> <ol style="list-style-type: none"> When you choose the <i>Increment Signal Name</i> function, the <i>Attach Signal</i> drop-down list appears as shown below.  <ol style="list-style-type: none"> Replace <code>signal</code> with the name of the signal you want to use. Replace <code>start_num</code> with the number starting from which you want to increment the signal name. Press <i>Enter</i>. <p>The pins are automatically connected to signals that have the signal name that increments from the starting number you specified in the <i>Attach Signal</i> drop-down list.</p>  <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">Pin Name</th> <th style="text-align: left;">Pin Number</th> <th style="text-align: left;">Pin Type</th> <th style="text-align: left;">Signal</th> </tr> </thead> <tbody> <tr> <td>*</td> <td>*</td> <td>*</td> <td>*</td> </tr> <tr> <td>address<11..0></td> <td>B6,B7,B8...</td> <td>Output</td> <td></td> </tr> <tr> <td>afd</td> <td>A9</td> <td>Input</td> <td>mcm_1</td> </tr> <tr> <td>afs</td> <td>A8</td> <td>Input</td> <td>mcm_2</td> </tr> <tr> <td>cclock</td> <td>A3</td> <td>Input</td> <td>mcm_3</td> </tr> </tbody> </table>	Pin Name	Pin Number	Pin Type	Signal	*	*	*	*	address<11..0>	B6,B7,B8...	Output		afd	A9	Input	mcm_1	afs	A8	Input	mcm_2	cclock	A3	Input	mcm_3
Pin Name	Pin Number	Pin Type	Signal																						
*	*	*	*																						
address<11..0>	B6,B7,B8...	Output																							
afd	A9	Input	mcm_1																						
afs	A8	Input	mcm_2																						
cclock	A3	Input	mcm_3																						

In the above example, the pin `afd` is connected to signal `mcm_1`, pin `afs` is connected signal `mcm_2`, and pin `cclock` is connected to signal `mcm_3` because you specified `mcm_` as the signal name and `1` as the starting number in the *Attach Signal* drop-down list.

Using the Attach Signal Drop-Down List

The Attach Signal drop-down list lets you do the following:

- Connect a signal existing in the current design to the selected pins in the Component Connectivity Details pane.
- Use functions to automatically generate signal names for pins.

Note: If a selected pin is already connected to a signal, using a function will overwrite the signal connected to the pin.

To connect a signal to the selected pins in the Component Connectivity Details pane:

1. Do one of the following:
 - Select the pin name of the pins to which you want to connect the signal.
 - Select the *Signal cell* next to the pins to which you want to connect the signal.
2. Select the signal name from the *Attach Signal* drop-down list.

To use functions to automatically generate signal names for pins in the Component Connectivity Details pane:

1. Do one of the following:
 - Select the pin name of the pins for which you want to automatically generate signal names.
 - Select the *Signal cell* next to the pins for which you want to automatically generate signal names.
2. In the *Attach Signal* drop-down list, select the function you want to use to automatically generate signal names for the selected pins.

For more information on the functions you can select in the *Attach Signal* drop-down list, see [Table 6-1](#) on page 190.

Note: If a selected pin is already connected to a signal, choosing a function will overwrite the signal connected to the pin.

Deleting Pin-Signal Connectivity in the Component Connectivity Details Pane

To delete the pin-signal connectivity in the Component Connectivity Details pane

- Select the *Signal* cells next to the pins for which you want to delete the pin-signal connectivity and press the *Delete* key.

Capturing Signal Connectivity

The Signal Connectivity Details pane displays the connectivity information for a signal in the design. The Signal Connectivity Details pane also allows you to quickly connect a signal to component pins, apply terminations, and assign signal integrity models.

For more information on using the Signal Connectivity Details pane, see the following sections:

- [Capturing Connectivity for a Single Signal](#) on page 200
- [Capturing Connectivity Information for Multiple Signals](#) on page 201
- [Capturing Connectivity Information for a Vectored Signal](#) on page 202
- [Editing the Connectivity Information for a Bit of a Vectored Signal](#) on page 203
- [Modifying Pin-Signal Connectivity in the Signal Connectivity Details Pane](#) on page 204
- [Deleting Pin-Signal Connectivity in the Signal Connectivity Details Pane](#) on page 204
- [Working with Unconnected Pins](#) on page 204

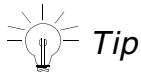
Capturing Connectivity for a Single Signal

To edit the connectivity information for a single signal, complete the following steps.

1. Double-click on the signal in the Signal List.

The connectivity information for the signal is displayed in the Signal Connectivity Details pane.

2. In the *Cell* drop-down list, select the name of the component whose pin you want to connect to the signal.
3. In the *Instance* drop-down list, select the instance name of the component whose pin you want to connect to the signal.
4. In the *Ref Des* drop-down list, select the reference designator of the component whose pin you want to connect to the signal.



Tip

You can also select components in the Component List and drag and drop the components in the Signal Connectivity Details pane to display the component name, instance name and reference designator of the component in the Signal Connectivity Details pane. You can then perform step 5 below.

5. Do one of the following:

- In the *Pin Name* drop-down list, select the pin name of the pin you want to connect to the signal.
- In the *Pin Number* drop-down list, select the pin number of the pin you want to connect to the signal.

The pin of the component is connected to the signal.

Capturing Connectivity Information for Multiple Signals

System Connectivity Manager allows you to simultaneously capture the connectivity of multiple signals using Signal Connectivity Details pane. The steps to be performed to edit the connectivity information for multiple signals at the same time, are as follows.

1. Select the signals in the Signal List.

2. Choose *Object – Edit Connectivity in Same Pane*.

The connectivity information for both the signals is displayed in the Signal Connectivity Details pane.

3. In the Signal Name drop-down list, select the name of the signal you want to connect to the pin of a component.

4. In the *Cell* drop-down list, select the name of the component whose pin you want to connect to the signal.

5. In the *Instance* drop-down list, select the instance name of the component whose pin you want to connect to the signal.

6. In the *Ref Des* drop-down list, select the reference designator of the component whose pin you want to connect to the signal.



Tip

You can also select components in the Component List and drag and drop the components in the Signal Connectivity Details pane to display the component name, instance name and reference designator of the component in the Signal Connectivity Details pane. You can then perform step 7 below.

7. Do one of the following:

- In the *Pin Name* drop-down list, select the pin name of the pin you want to connect to the signal.
- In the *Pin Number* drop-down list, select the pin number of the pin you want to connect to the signal.

The pin of the component is connected to the signal.

Capturing Connectivity Information for a Vectored Signal

To edit the connectivity information for a vectored signal, display the existing connectivity of the signal in the Signal Connectivity Details pane by double-clicking on the vectored signal in the Signal List.

1. In the *Start Bit* drop-down list select the start bit of the signal you want to connect to the pin.
2. In the *End Bit* drop-down list select the end bit of the signal you want to connect to the pin.

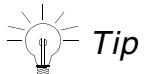
Note the following:

- Ensure that there is no mismatch in the width of the signal you specify in the *Start Bit* and *End Bit* fields, and in the width of the pin you want to connect to a signal.
- You can connect a bit of a vectored signal to a bit of a vector pin. However, you cannot connect a range of bits of a vectored signal to a range of bits of a vector pin.

For example, to connect the bit `ADDR<0>` of a vectored signal `ADDR<15..0>` to the bit `DATA<0>` of the vector pin `DATA<7..0>`, enter 0 in the *Start Bit* and *End Bit* fields and then select the bit `DATA<0>` of the vector pin `DATA<7..0>` in the *Pin Name* drop-down list. However, you cannot connect `ADDR<3..0>` to `DATA<3..0>` by entering 3 in the *Start Bit* and 0 in the *End Bit* field and then entering `DATA<3..0>` in the *Pin Name* field.

3. In the *Cell* drop-down list, select the name of the component whose pin you want to connect to the signal.

4. In the *Instance* drop-down list, select the instance name of the component whose pin you want to connect to the signal.
5. In the *Ref Des* drop-down list, select the reference designator of the component whose pin you want to connect to the signal.



Tip

You can also select components in the Component List and drag and drop the components in the Signal Connectivity Details pane to display the component name, instance name and reference designator of the component in the Signal Connectivity Details pane. You can then perform step 6 below.

6. Do one of the following:
 - In the *Pin Name* drop-down list, select the pin name of the pin you want to connect to the signal.
 - In the *Pin Number* drop-down list, select the pin number of the pin you want to connect to the signal.

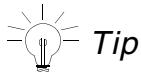
The pin of the component is connected to the signal.

Editing the Connectivity Information for a Bit of a Vectored Signal

1. Click on the *Expanded Signal List* button in the Signal List to display the Expanded Signal List.

For more information on using the Expanded Signal List, see [Viewing Bits of a Vector Signal in Signal List Pane](#) on page 149.
2. Double-click on the bit of the vectored signal in the Signal List.

The connectivity information for the bit of the vectored signal is displayed in the Signal Connectivity Details pane.
3. In the *End Bit* drop-down list select the end bit of the signal you want to connect to the pin.
4. In the *Cell* drop-down list, select the name of the component whose pin you want to connect to the signal.
5. In the *Instance* drop-down list, select the instance name of the component whose pin you want to connect to the signal.
6. In the *Ref Des* drop-down list, select the reference designator of the component whose pin you want to connect to the signal.



Tip

You can also select components in the Component List and drag and drop the components in the Signal Connectivity Details pane to display the component name, instance name and reference designator of the component in the Signal Connectivity Details pane. You can then perform step 7 below.

7. Do one of the following:

- In the *Pin Name* drop-down list, select the pin name of the pin you want to connect to the signal.
- In the *Pin Number* drop-down list, select the pin number of the pin you want to connect to the signal.

The pin of the component is connected to the signal.

Modifying Pin-Signal Connectivity in the Signal Connectivity Details Pane

You can modify the pin-signal connectivity of a component by connecting the signal to another pin of the component.

Do one of the following:

- Select a different pin name in the *Pin Name* drop-down list.
- Select a different pin number in the *Pin Number* drop-down list.

Deleting Pin-Signal Connectivity in the Signal Connectivity Details Pane

To delete the pin-signal connectivity in the Signal Connectivity Details pane

Click on the row for the component for which you want to delete the pin-signal connectivity, and press the *Delete* key.

Working with Unconnected Pins

In System Connectivity Manager, you can assign a power pin as a not connected (NC) pin, or assign an NC pin as a power pin by specifying a power supply for the NC pin. See [Working with Power Pins and NC Pins of Components](#) for details on this.

You can also intentionally leave certain signal pins unconnected for various reasons, such as:

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Capturing Connectivity

- You might not need to use all the PCIe ports on a processor for which you want an NC symbol on the net.
- A die will not fit into a package with the appropriate number of pins, and you use a larger, standard package. This results in unused pins.
- Adjacent pins are too close together to meet high voltage spacing requirements, so you want an NC pin between them.

To mark a signal pin as a not connected (NC) pin, create a signal named NC and connect the pin that you want to leave unconnected to this signal. This will identify it as an NC pin.

Important

Like GND, an NC signal is a special name. As a result, do not use prefixes or suffixes with the name. The only supported name is NC for such signals.

Pins connected to NC signals will not be flagged during the Unconnected Pins Design Rule Check (DRC).

To create an NC signal in System Connectivity Manager, do the following:

1. Choose one of the following options:
 - Select *Design — Add Signal*.
 - In the Signal List pane, right-click and select *Add Signal*.
 - In the Signal List pane, press the *Insert* key.
2. Specify the Signal Name as NC.
3. Select the Signal Type as *Local*.

A local signal is a signal that is unique to a design. Local signals that have the same name in different designs will not be connected.
4. Connect the NC signal to the pins that you want to deliberately leave unconnected.

Using Matrix Connectivity View Pane to Capture Connectivity

The Matrix Connectivity View pane displays the connectivity information for the selected signals and components in a matrix format. You can use this view to connect a signal to the pins of one or more design components. Using the Matrix Connectivity view, you can validate the signal flow through the components.

Creating a Matrix Connectivity View

Do the steps listed below.

1. From the *Table* menu, choose *Matrix View - Create*.
2. In the Create Matrix View dialog box, select the option to specify whether the matrix view being created is a temporary view or permanent view.
3. In the Components tab select the components to be added to the matrix view.
4. Use the Signals tab to specify the signals to be added to the matrix view.
5. Click OK.

The Matrix Connectivity View appears with signal names appearing in the first column and components added in step 3 constitute the other columns of the matrix. Signal names, added in step 4 appear as rows. The number of rows in the matrix depends on whether the signals are connected to component pins or not.

To open an existing Matrix Connectivity View

1. From the *Table* menu, choose *Matrix View - Open*.

All the Matrix Connectivity views that are available for the design as listed in the Open sub menu.

2. Select the required view.

Modifying the Matrix Connectivity View

After you have created the Matrix Connectivity View, you can modify it by adding or removing objects from the view.

1. From the *Table* menu, choose *Matrix View - Edit*.

The Edit Matrix View dialog box appears, with the list of objects available and the objects to be added.

2. To modify the view, add or delete the objects in the component or signals pane as per the requirement.
3. Click OK, to update the view with the modifications.

Note: If required, you can customize the information displayed in the Matrix Connectivity View. To know how to customize the view, see [Customizing the Spreadsheet Editor](#) on page 650.

Deleting a Matrix Connectivity View

To delete the matrix Connectivity view that is currently open, do the following.

- From the *Table* menu, choose *Matrix View – Remove*.

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Capturing Connectivity

Working with Differential Pairs

Working with Differential Pair of Pins

While working on your design in System Connectivity Manager you can use the Show Differential Pairs check box in the Component Connectivity Detail pane to display the differential pair pins as differential pairs instead of individual pins. When you select this check box, differential pair of pins are listed in the Component Connectivity Detail pane.

System Connectivity Manager supports following types of differential pairs:

- Model-Defined Differential Pairs
- Library-Defined Differential Pairs
- User-Defined Differential Pairs

Model-Defined Differential Pairs

These differential pairs are created when you assign signal integrity model to a component. For information on how to assign models to a component, see Chapter 12, “Working with Signal Integrity Models.”

Note: After you have created a model-defined differential pair, any modifications made to the model, does not automatically impact the differential pair. To view the impact of the changes, reassign the model or open the design in the session of System Connectivity Manager.

Library-Defined Differential Pairs

While capturing a design in SCM, you may have components that have pins marked as differential pair pins. Signals connected to these pins automatically form differential pairs. These are called library-defined differential pairs. In library-defined differential pairs, the positive and negative pins of the differential pair are identified using the DIFF_PAIR_PINS_POS and DIFF_PAIR_PINS_NEG properties, respectively.

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Working with Differential Pairs

Pins that have the same value of the DIFF_PAIR_PINS_POS and DIFF_PAIR_PINS_NEG properties, form a differential pair. The name of a library-defined differential pair is the same as the value assigned to the DIFF_PAIR_PINS_POS and DIFF_PAIR_PINS_NEG properties.

The following figure shows a section of the `chip.prt` file for a component with library-defined differential pair. The figure also shows the differential pair that is created when this part is instantiated in a design in SCM.

Entries in the `chip.prt` file for pins of a library-defined differential pair

```
'B1_N':
  PIN_NUMBER='(49)';
  PIN_TYPE='ANALOG';
  NO_LOAD_CHECK='Both';
  NO_IO_CHECK='Both';
  NO_ASSERT_CHECK='TRUE';
  NO_DIR_CHECK='TRUE';
  ALLOW_CONNECT='TRUE';
  DIFF_PAIR_PINS_NEG='DP_B1_';

'B1_P':
  PIN_NUMBER='(53)';
  PIN_TYPE='ANALOG';
  NO_LOAD_CHECK='Both';
  NO_IO_CHECK='Both';
  NO_ASSERT_CHECK='TRUE';
  NO_DIR_CHECK='TRUE';
  ALLOW_CONNECT='TRUE';
  DIFF_PAIR_PINS_POS='DP_B1_';
```

☒	DP_B1_	53,49	Inout
⊕	b1_p	53	Inout
⊖	b1_n	49	Inout
☒	DP_B2_	54,50	Inout

Library-defined differential pair in SCM

Figure 7-1 Library-defined differential pair

Note: For information on how to create parts with library-defined differential pairs, see *Part Developer User Guide*.

User-Defined Differential Pairs

If you have components that use a particular naming scheme to name differential pair pins on the component, you can ensure that these pins are displayed as differential pairs in the Component Connectivity Details pane.

For example, if a component has two pins, `add+` and `add-`, the setup options can be modified to ensure that these pins are displayed in Component Connectivity Details pane as a differential pair of pins. The name for this differential pair of pins is generated based on the

setup options specified by you. If you expand this differential pair, add+ and add- are displayed as pins in the differential pair.

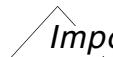
Differential-Pair Precedence

In a design, model-defined differential pairs have precedence over library-defined differential pairs, which in turn have higher precedence than user-defined differential pairs.

This implies that if a component has library-defined differential pairs, user-defined differential pairs will not be created even if the component satisfies the criteria for creating user-defined differential pairs, specified in the Differential Pair page of the Setup dialog box.

Consider a project in which all components pins that have _LOW and _HIGH as suffixes should form a differential pair. If you now instantiate a component that has library-defined differential pairs and also has a set of pins that satisfy the above criteria, then only library-defined differential pairs will be honored for the component.

Similarly, model-defined differential pairs created by assigning signal integrity model to a component, will override the library-defined or user-defined differential pairs on that component. Creating a model-defined differential pair may break an existing library-defined differential pair, but it does not impact the existing connectivity and constraints defined for the component.



Important
Model-defined and library-defined differential pairs cannot be modified by users.

To identify whether a differential pair is a model-defined, a library-defined, or a user-defined differential pair, hover the cursor on the differential pair icon in the Component Connectivity Details pane. The tooltip displays the type of the differential pair of pins.



For information on capturing differential pair connectivity, see Working with Differential Pair Signals on page 214

Displaying Differential Pairs in Component Connectivity Details Pane

To ensure that the differential pins on a design component are displayed as differential pairs in Component Connectivity Details pane, perform the following steps.

1. In the Differential Pairs page of the Setup dialog box, modify the setup information to specify the pin name formats to be identified as differential pairs.
To know how to specify the naming convention in Setup, see Setting Differential Pair Naming Convention on page 101.
2. In the same dialog box, you also need to specify the prefix value to be used while generating a name for the differential pair of pins.
3. Click *OK* to save the modifications.
4. In the Component Connectivity Details pane, ensure that the Show Differential Pairs check box is selected.

If you now instantiate a component in your design, differential pairs are created for the pins that have pin names as per the format specified in the step 1.



Regardless of the pin naming formats specified in the setup, you cannot create differential pairs using power pins.

In case you modify the setup options for the differential pair in the middle of the design process, to update the user-defined differential pair based on the latest setup options, complete the following steps.

- a. Right-click on the Component List pane.
- b. From the pop-up menu, choose *Recompute Differential Pairs*.

The display in the Component Connectivity Details pane is updated to show pins as differential pairs.

Note that while generating names differential pairs for pins, the default naming convention used is [prefix_specified_in_setup]<common_string_in_pin_name>.



The Recompute Differential Pairs option recomputes differential pairs based on the latest setup options. Based on the modifications made in the setup options, this may result in the creation or deletion of new differential pairs.

By default, the differential pair pins are displayed in the Component Connectivity Details pane in non-expanded mode. To view the individual pins in the differential pair, select the *Expand All Pins* check box in the Component Connectivity Details pane.

i6 (90c031tm) - U6			
<input type="checkbox"/> Expand All Pins			
	Pin Name	Pin Number	Pin Type
:	*	*	*
	din1	1	Input
	din2	7	Input
	din3	9	Input
	din4	15	Input
☒	DP_dout1	3,2	Output
☒	DP_dout2	6,5	Output
☒	DP_dout3	11,10	Output
☒	DP_dout4	14,13	Output

Differential Pair Pins

☒	DP_dout1	2,3	Output
⊕	dout1+	2	Output
⊖	dout1-	3	Output
☒	DP_dout2	6,5	Output
⊕	dout2+	6	Output
⊖	dout2-	5	Output
☒	DP_dout3	10,11	Output
⊕	dout3+	10	Output
⊖	dout3-	11	Output
☒	DP_dout4	14,13	Output
⊕	dout4+	14	Output
⊖	dout4-	13	Output

Expanded Differential Pair Pins

In the expanded view, along with individual pins, the polarity of each differential pair pin is also displayed in the Component Connectivity Details pane.

Deleting User-Defined Differential Pair of Pins

You can remove user-defined differential pair of pins displayed in the Component Connectivity Details pane. However, removing model-defined differential pairs is not supported in System Connectivity Manager.

To delete a user-defined differential pair of pins you need to perform the following step.

- In CCP, right-click on the differential pair to be deleted, and from the pop-up menu, choose *Remove Differential Pair*.

Working with Differential Pair Signals

System Connectivity Manager provides support for adding user-defined differential pair signals to your project.

- [Adding Differential Pair Signals in System Connectivity Manager](#)
- [Creating Differential Pairs from Existing Signals](#)
- [Differential Pairs for Vectored Signals](#)
- [Renaming Differential Pairs](#)
- [Deleting Differential Pair Signals](#)
- [Capturing Differential Pair Connectivity](#)

Adding Differential Pair Signals in System Connectivity Manager

You can add a differential pair signal using the Add Signal(s) dialog box.

1. Choose *Design – Add Signal*.

Alternatively, right-click on the Signal List pane and choose *Add Signal*.

2. In the Add Signal(s) dialog box, specify the details listed below.

- a. To add a differential pair signal, select the differential pair check box .

Note: Selecting the check box enables the Differential Pair Name field.

- b. In the Signal Name column, specify the name of the differential pair member net.

Note: Names of the member nets are generated by applying the [Format for Naming Differential Pair Signals](#) to the value specified by you in the Signal Name column.

- c. Specify the Signal Type as LOCAL, GLOBAL, IN, OUT, or INOUT.

Note that the Differential Pair Name column is automatically populated by the differential pair name, created using the signal name specified in [step b](#) and the differential pair signal prefix value specified in the [Setup](#) dialog box. You can either accept the default name or can specify a different name for the differential pair.



If you have not specified the signal naming convention in the Setup dialog box, member net names are generated by suffixing + and - to the signal name.

3. Click OK.

The differential pair signals are added to the design. Differential pairs are listed in the Signal List pane and are identified by the differential pair icon ().

Note: If you place your cursor on the differential pair in the SLP, member nets are displayed as tooltips.

Example

Create differential pair signals with the following specifications:

- The positive and negative signals of the differential pair are to be indicated by suffixes, `_pos` and `_neg`, respectively.
- Differential pair signal names should start with the prefix, `DFS_`
- Verify the setup by creating a differential pair with member nets as `a_pos` and `a_neg`.

To ensure that the differential pair signals that you add to your design follow the above specifications, perform the steps listed below.

1. Choose *Project – Settings – Differential Pairs* to open the dialog box with differential pair setup options.

2. In the *Format for Naming Differential Pair Signals* grid, enter `_neg` and `_pos` in the Negative Signal and Positive Signal columns, respectively.

Ensure that SUFFIX is specified as Location. This will ensure that `_pos` or `_neg` are added as suffixes while generating the member net names.

3. In the *Prefixes For Differential Pair Names For Signals* text box, enter `DFS_`

4. Click *OK* to save the settings.

5. Open the Add Signal(s) dialog box using one of the methods listed below.

- Choose *Design – Add Signal(s)*.
- Right-click on the Signal List pane and choose *Add Signal(s)*.

6. In the Add Signal(s) dialog box, select the differential pair check box indicated the following icon .

7. In the Signal Name column, specify the member net name as `a`.

8. Click *OK*.

The differential pair DFS_a is listed in the Signal List pane.

Note: You cannot change the scope of a differential pair signal to Global in the Signal List Pane.

Creating Differential Pairs from Existing Signals

You can create differential pair signal using two scalar signals or two vector signals with same signal width.

1. In SLP, select the signals to be added as member nets of the differential pair.
2. Right-click and from the pop-up menu, choose *Create Differential Pair*.

A differential pair is created.

To create differential pair using a scalar net and one bit of a vector net, first display the individual bits of a bus, and then create a differential pair using the steps listed above. To display the individual bits of a vector signal in the Signal List pane, complete one of the steps listed below.

- Click  in the Signal List pane header and deselect *Show Buses*.
- Right-click on the Signal List pane header and deselect *Show Buses*.

Names for Differential Pair Signals

The differential pair name is generated by concatenating the prefix value specified in the *Differential Pairs* tab of the Setup dialog box and the common string (if any) in the member net names.

The convention used for naming differential pairs is

[prefix_specified_in_setup]<common_string_in_member_net_name>.
If prefix value is not specified in the setup, only the second part is used to name the differential pair signals.

Example

The prefix for naming differential pairs for signals is specified as DFS_. If you create a differential pair using existing signals, d_s and d_z as member nets, the differential pair created is DFS_d. In the same design, if you now want to create differential pair for signals d and d_1, the differential pair will be named as DFS_1_d.

Important

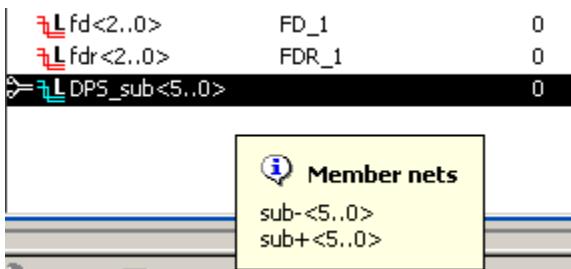
If you use the function “same as pin-name” to name the signals, SCM creates a differential pair name similar to the differential pair pin-name. The differential-pair prefix defined in the setup is not valid as you are defining the name explicitly.

Differential Pairs for Vectored Signals

System Connectivity Manager supports differential pairs created using two vector signals with same signal width. You can add differential pairs for vectored signals using one of the following methods.

■ Using Add Signal(s) dialog box.

To add a vectored differential pair signal, the value specified in the Signal Name column should be a vectored signals.



■ Using existing vectored signals

To create a differential pair from existing vectored signals, ensure that the vectored signals have same signal width.

Displaying Differential Pair Signals

Using the options provided in SCM, you can either display the individual member nets of a differential pair or can display the differential pairs in the Signal List pane. By default, differential pairs are displayed in the Signal List pane.

To display member nets of a differential pair signal in the Signal List pane, perform the following steps:

1. Select the  button in the Signal List pane header.

Alternatively, you can right-click on the header of the Signal List pane.

2. From the pop-up menu, deselect *Show Differential Pairs*.

Individual member nets are displayed in SLP.

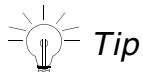
Note: In case of vectored differential pair signals, instead of scalar nets, two buses will be listed as member nets.

Renaming Differential Pairs

SCM provides support for renaming differential pair signals from the *Signals List pane*. In System Connectivity Manager, you can rename the logical as well as the physical name of a differential pair signal.

To change the name of a differential pair signal, perform the following steps.

1. In the Signal List pane, right-click on the differential pair name.
2. To change the logical name, choose *Change – Name*.



To change the physical name, choose *Change – Phys Name*.

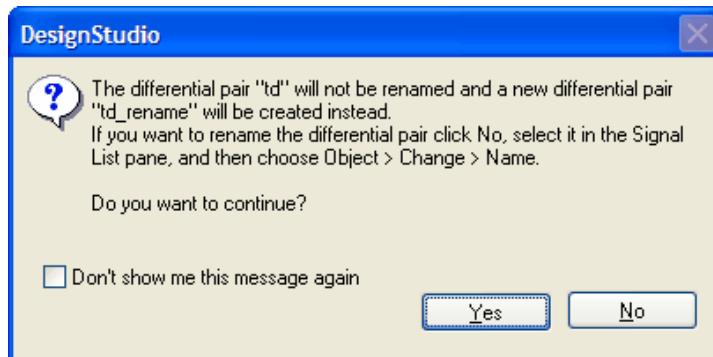
3. Specify the new name and press the Enter key.

Alternatively, you can select the differential pair in the Signal List pane, press the F2 key, or choose *Object — Change* from the menu, and modify the differential pair name.



Important

You cannot rename a differential pair from the Component Connectivity Details pane. A warning message displays that the differential pair will not be renamed and a new differential pair will be created instead.



System Connectivity Manager User Guide

Working with Differential Pairs

Differential pairs can also be renamed using the Constraint Manager. Changes made to the differential pair name in the Constraint Manager are reflected in System Connectivity Manager. For information on renaming differential pairs in Constraint Manager, see [System Connectivity Manager To Constraint Manager User Guide](#).



Important

In case of hierarchical designs that have single-or multiple instances of blocks with differential pair signals, renaming the logical name of a differential pair signal in System Connectivity Manager, will cause the physical name to be updated, only if the physical name is auto-generated by the tool. In case, you have modified the physical name of a differential pair either in System Connectivity Manager or in Constraint Manager, it is not synced up with logical name automatically.



Tip

Renaming of vectored differential pairs is not supported.

Deleting Differential Pair Signals

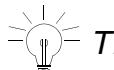
Using SCM, you can delete user-defined differential pairs. Model-defined differential pairs cannot be deleted.

To delete a user-defined differential pair:

1. Right-click on the differential pair to be deleted.
2. From the pop-up menu, choose *Delete*.

The differential pair gets deleted, and the member nets are listed as individual nets. Note that deleting a user-defined differential pair does not delete the member nets from the design. Only the differential pair signal is deleted.

The *Delete* command is not enabled if the differential pair signal has connectivity. In such cases, you first need to delete the differential pair connectivity — the member net and pin connectivity can be retained — and then delete the differential pair.



Tip

Deleting a differential pair signal without modifying the connectivity of member nets is supported in Constraint Manager.

Capturing Differential Pair Connectivity

Using SCM, you can easily capture connectivity between a differential pair signal and differential pair pin.

- To connect a differential pair signal to a differential pair pin, drag the differential pair signal from Signal List pane and drop it on the differential pair pin in Component List pane. The member net with a positive polarity is connected to the pin with positive polarity, and the other member net is connected to the pin with negative polarity.

Note: When you specify connectivity in System Connectivity Manager, internal design rule checks are run to ensure that the differential pair pin and the member net of a differential pair signal connected to it have same polarity. For example, positive pin of a differential pair must always be connected to the positive member of the differential pair signal.

- In Component Connectivity pane, you can also specify connectivity of a differential pair pin to a differential pair signal by typing the name of the differential pair signal in the Signal Name column corresponding to the differential pair pin.
- If you connect individual pins of a differential pair pin to two scalar signals, a new differential pair signal is created using scalar signals as member nets. The differential pair name is generated using the prefix value specified in the Differential Pair Setup page.
- If you connect member nets of a differential pair signal to two pins that are not differential pair pins, the member nets are listed as normal nets in the Component Connectivity Details pane.
- While capturing connectivity in the Component Connectivity Details pane, if you use the *Same as Pin Name* option on a differential pair object, the name of the differential pair signal that gets created is the same as the name of the differential pair object. In this case, the prefix value specified in the Differential Pair Setup page, for differential pair of

System Connectivity Manager User Guide

Working with Differential Pairs

signals, is ignored. However, the member nets of the new differential pair follow the format specified in the setup.

Y	DP_y2	D1,C1	Output	
Y	DP_y3	J1,K1	Output	
Y	DP_y4	K3,K2	Output	DP_y4
Y	DP_y5	A5,A4	Output	
Y	DP_y6	A6,B6	Output	
Y	DP_y7	D6,C6	Output	

Differential pair signal that does not use the prefix specified in the setup.

Y	DP_y4	K3,K2	Output	DP_y4
⊕	y4_p	K3	Output	y4+
⊖	y4*	K2	Output	y4-

Member nets names are generated using the format specified in setup and do not match the pin names

Figure 7-2 Same as Pin Name command used on differential pair object

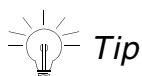
When you use the *Same As Pin Name* command to generate member nets, the name of the differential pair signal is generated as shown in the figure below.

Y	DP_y4	K3,K2	Output	DP_y4
Y	DP_y5	A5,A4	Output	DS_y5
⊕	y5_p	A5	Output	y5_p
⊖	y5*	A4	Output	y5*

Name of the differential pair signal is generated using the prefix value specified in setup

Member nets names match the pin names.
(Format specified in the setup for differential pair signals is ignored)

Figure 7-3 Same as Pin Name command used on differential pair pins

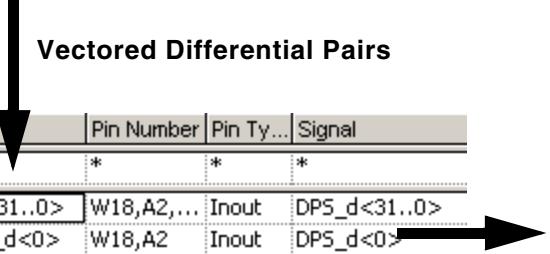


While using the *Same as Pin Name* command to capture differential pair connectivity, if you want the differential pair signal names to be generated based on component pins, it is recommended that you first clear the *Show Differential Pairs* check box to display only the component pins in the Component Connectivity Detail pane, and then use the *Same as Pin Name* command.

System Connectivity Manager User Guide

Working with Differential Pairs

- Drag a vectored differential pair signal from SLP and drop it on the vectored differential pair pin of same width. The individual bits of the members nets of the differential pair signal are connected to the component pins as shown in the figure below.



Vectorized Differential Pairs

Pin Name	Pin Number	Pin Type	Signal	Term
*	*	*	*	*
☒ DPP_d<31..0>	W18,A2,T17,A1,...	Inout	DPS_d<31..0>	

Pin-net connections

Pin Name	Pin Number	Pin Ty...	Signal
*	*	*	*
☒ DPP_d<31..0>	W18,A2,...	Inout	DPS_d<31..0>
☒ DPP_d<0>	W18,A2	Inout	DPS_d<0>
☒ DPP_d<1>	T17,A1	Inout	DPS_d<1>
☒ DPP_d<2>	Y20,C2	Inout	DPS_d<2>
☒ DPP_d<3>	Y19,E4	Inout	DPS_d<3>
☒ DPP_d<4>	W20,C1	Inout	DPS_d<4>
☒ DPP_d<5>	V19,E2	Inout	DPS_d<5>
☒ DPP_d<6>	U19,D2	Inout	DPS_d<6>
☒ DPP_d<7>	T16,E1	Inout	DPS_d<7>
☒ DPP_d<8>	T19,D1	Inout	DPS_d<8>
☒ DPP_d<9>	U20,F1	Inout	DPS_d<9>
☒ DPP_d<10>	Y20,G2	Inout	DPS_d<10>
☒ DPP_d<11>	R19,F2	Inout	DPS_d<11>
☒ DPP_d<12>	N17,H2	Inout	DPS_d<12>
☒ DPP_d<13>	P17,H4	Inout	DPS_d<13>
☒ DPP_d<14>	R20,G1	Inout	DPS_d<14>
☒ DPP_d<15>	P20,K2	Inout	DPS_d<15>
☒ DPP_d<16>	N20,J2	Inout	DPS_d<16>

Pin Name	Pin Number	Pin Ty...	Signal
*	*	*	*
☒ DPP_d<31..0>	W18,A2,...	Inout	DPS_d<31..0>
☒ DPP_d<0>	W18,A2	Inout	DPS_d<0>
⊕ d_h<0>	W18	Inout	add<0>
⊖ d_l<0>	A2	Inout	bad<2>
☒ DPP_d<1>	T17,A1	Inout	DPS_d<1>
⊕ d_h<1>	T17	Inout	add<1>
⊖ d_l<1>	A1	Inout	bad<3>
☒ DPP_d<2>	Y20,C2	Inout	DPS_d<2>
⊕ d_h<2>	Y20	Inout	add<2>
⊖ d_l<2>	C2	Inout	bad<4>
☒ DPP_d<3>	Y19,E4	Inout	DPS_d<3>
⊕ d_h<3>	Y19	Inout	add<3>
⊖ d_l<3>	E4	Inout	bad<5>
☒ DPP_d<4>	W20,C1	Inout	DPS_d<4>
⊕ d_h<4>	W20	Inout	add<4>
⊖ d_l<4>	C1	Inout	bad<6>
☒ DPP_d<5>	V19,E2	Inout	DPS_d<5>
⊕ d_h<5>	V19	Inout	add<5>

- While capturing the connectivity of a differential pair pin, if you enter a non-existent differential pair name, the differential pair is created in the signal list pane.
- With the *Auto-connect differential pairs in the Connectivity panes* option in the Differential Pairs setup dialog box selected, if you connect one member net of a differential pair signal to a differential pair pin, the second member net of the differential pair is automatically connected to the unconnected differential pair pin.

Navigating the Design and Viewing Files

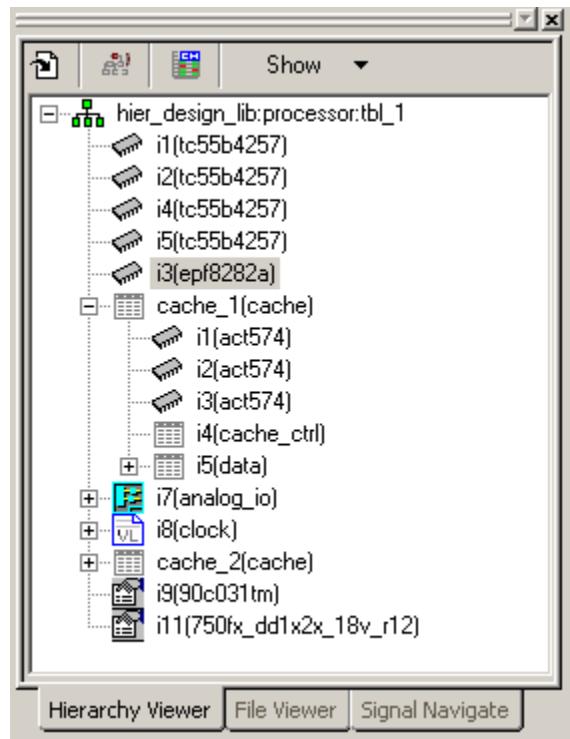
This chapter describes how you can use the Hierarchy Viewer and Signal Navigate windows to navigate the design and view the files related to the design in the File Viewer.

For more information, see the following sections:

- [Using Hierarchy Viewer](#) on page 224
- [Using Signal Navigate](#) on page 228
- [Using the File Viewer](#) on page 232

Using Hierarchy Viewer

The Hierarchy Viewer provides you a tree view of the complete design hierarchy and lets you quickly access all the blocks and components in your design.



Opening Hierarchy Viewer

To open Hierarchy Viewer, do one of the following:

- Choose *View – Hierarchy Viewer*.
- Click the *Hierarchy Viewer* tab.
- Press *Ctrl + Alt + H*.

The Hierarchy Viewer appears.

Opening a Block for Editing

To open a block for editing, do one of the following:

- Double-click on the block.
- Select the block and click .

The block is highlighted in the Component List and opened for editing in context mode. For more information on editing blocks, see [Editing a Hierarchical Design](#) on page 356.

Viewing the Connectivity of a Component Instance

To view the connectivity of a component

- Double-click on the component in the Hierarchy Viewer.

The block in which the component exists is opened for editing in context mode and the connectivity information for the component is displayed in the Component Connectivity Details pane.

Editing Properties and Constraints

To edit properties and electrical constraints using Constraint Manager

- Click .

Constraint Manager appears. You can view, add or modify properties and electrical constraints in Constraint Manager.

Note: For more information on working with properties and electrical constraints in Constraint Manager, see [Chapter 10, “Working with Properties and Electrical Constraints.”](#)

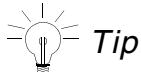
Setting a Block as the Root Design

To set a block as the root design

1. Click  on the toolbar.

The Change Root dialog box appears.

2. Click the *Library* drop-down list and select the library that contains the block you want to set as the root design.
3. Select the block from the *Cell* list and click *OK*.



You can also select a block in the *Hierarchy Viewer*, right-click and choose *Set as ROOT* to set the block as the root design.

For more information on setting a block as the root design, see [Setting the Root Design](#) on page 372.

Creating Blocks

To create a block using the Hierarchy Viewer, right-click and choose *Create Block*. The Create Block dialog box appears.

Note: For more information on creating blocks, see [Creating Blocks](#) on page 339.

Editing the Ports of a Block

To edit the ports or interface signals of a block using the Hierarchy Viewer, right-click and choose *Edit Block Interface*. The Edit Block Interface dialog box appears.

Note: For more information about editing the ports of a block, see [Editing the Ports of a Block](#) on page 370.

Showing and Hiding Components in the Hierarchy Viewer

- To display all the components in the design, choose *Show – Primitives*.
- To hide all the components in the design, choose *Show – Primitives*.

Expanding and Collapsing the Display in the Hierarchy Viewer

To expand the contents of a block

Do one of the following:

- Click next to the block.

- Select the block and choose *Show – Expand*.

To expand the contents of the entire design

- Choose *Show – Expand All*.

To collapse the contents of a block

Do one of the following:

- Click ⊞ next to the block.
- Select the block and choose *Show – Collapse*.

To collapse the contents of the entire design

- Choose *Show – Collapse All*.

Refreshing the Hierarchy in the Hierarchy Viewer

To refresh or rebuild the hierarchy, right-click and choose *Rebuild Hierarchy*.

The tree structure in the Hierarchy Viewer is updated with any changes in the components and blocks in the design.

Using Signal Navigate

In complex hierarchical designs, a large number of signals may be aliased to each other in the same block or across different blocks. This makes it difficult to quickly identify the aliases of a signal and view their connectivity for debugging purposes.

The Signal Navigate window lets you quickly view the aliases for a signal at all levels of a hierarchical design and navigate the signal to view its connectivity.

For more information on working with hierarchical designs, see [Chapter 13, “Working with Hierarchical Designs.”](#)

Using Signal Navigate

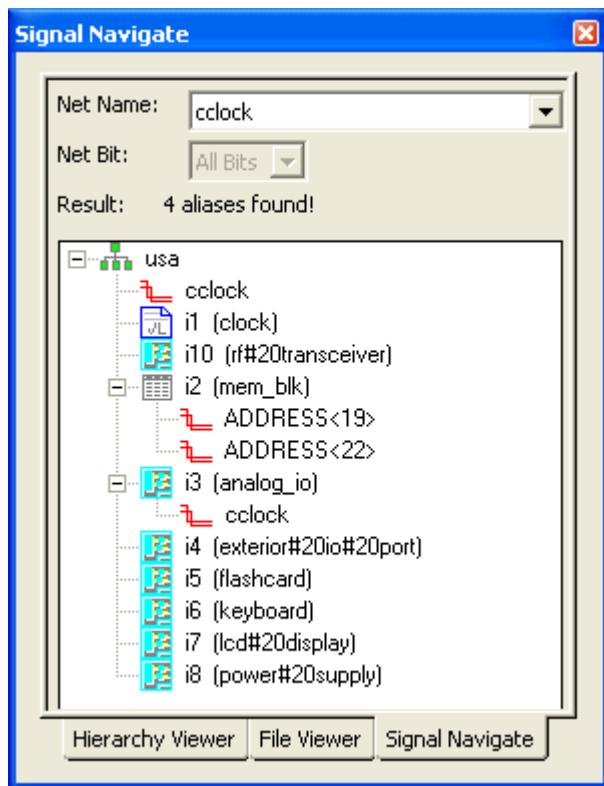
To use Signal Navigate

1. Do one of the following:

- Choose *View – Signal Navigate*.
- Select a signal in the Signal List, right-click and choose *Signal Navigate*.
- Click the *Signal Navigate* tab.
- Press *Ctrl + Alt + N*

The Signal Navigate window appears.

Figure 8-1 Signal Navigate Window



2. You can select a signal in one of the following ways:

- Select a signal in the Signal List.
- Select a signal from the *Net Name* drop-down list.

The *Net Name* drop-down list displays the last nine signals you selected in the Signal List.

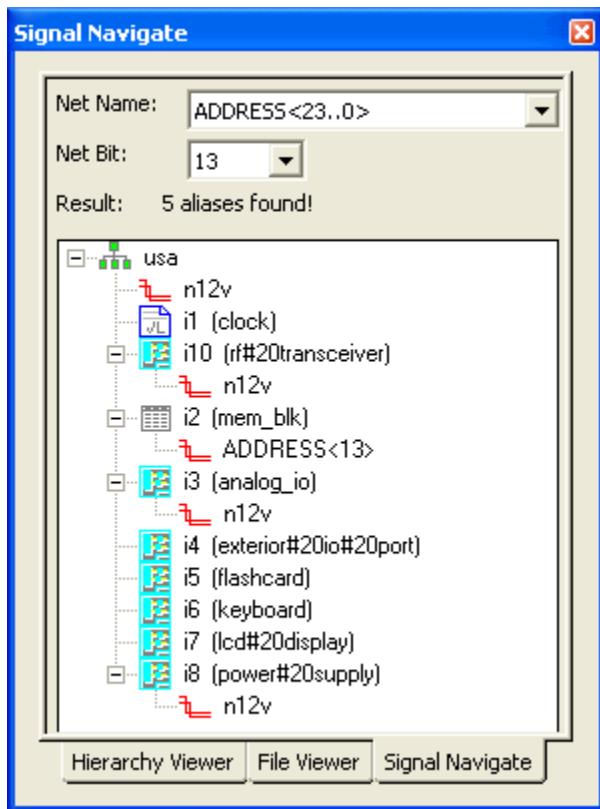
The Signal Navigate window displays the aliases for the signal at all levels of the design. For example, in Figure 8-1, the Signal Navigate window indicates that the signal `cclock` is aliased to the signals `ADDRESS<19>` and `ADDRESS<22>` in the `mem_blk` block and to another signal `cclock` in the `analog_io` block.

Note: If you have selected a vectored signal, by default, the Signal Navigate window displays the aliases for all the bits of the vectored signal. If you have aliased different bits of the vectored signal to different signals, you can view the aliases for a bit of the vectored signal by selecting the bit in the *Net Bit* drop-down list. This helps you in quickly identifying the signals aliased to a bit of a vectored signal.

For example, the following figure displays the signals aliased to the thirteenth bit of the vectored signal `ADDRESS<23..0>`.

System Connectivity Manager User Guide

Navigating the Design and Viewing Files

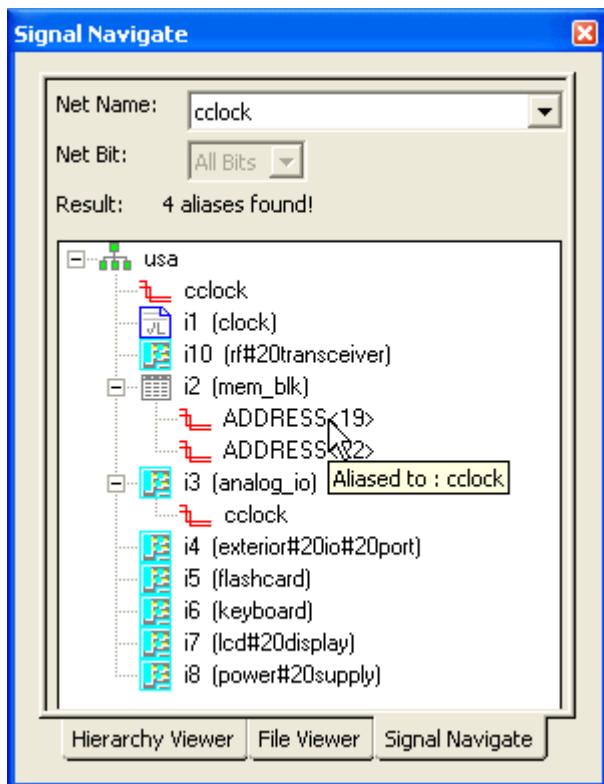


Note: To view the alias for a signal, hover your cursor over it. The alias for the signal is

System Connectivity Manager User Guide

Navigating the Design and Viewing Files

displayed as a tooltip as shown in the figure below.



3. To navigate to a signal, select it in the Signal Navigate window.

The connectivity information for the selected signal is displayed in the Signal Connectivity Details pane.

Note: If the selected signal is in a block you have not opened for editing, System Connectivity Manager automatically opens the block for editing in the context mode. For more information on editing blocks, see [Editing a Hierarchical Design](#) on page 356.

Using the File Viewer

The File Viewer displays the files related to your design and lets you open the files from System Connectivity Manager. For example, you can double-click on the board file to open it in Allegro PCB Editor.

You can also add any other file that you want to refer to when working in the design. For example, you can add the design specifications document for your design in the File Viewer so that you can easily access it when you are working in the design.

Opening File Viewer

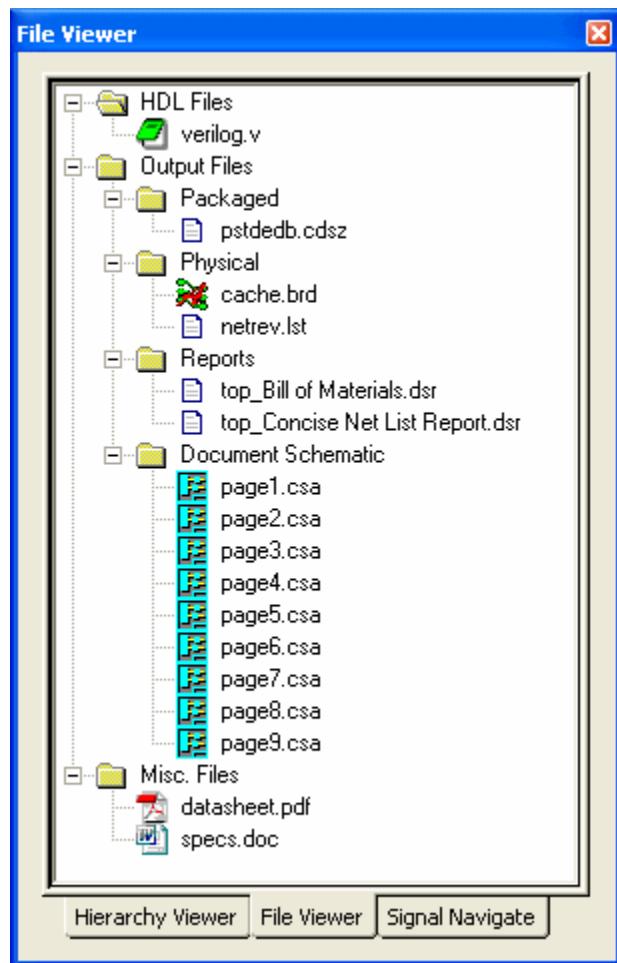
To open File Viewer, do one of the following:

- Choose *View – File Viewer*.
- Click the *File Viewer* tab.
- Press *Ctrl + Alt + F*

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Navigating the Design and Viewing Files

The File Viewer appears.



The contents of the folders in the File Viewer are described below:

Folder Name	Folder Contents
HDL Files	Contains the Verilog files used in the design.
Output	Contains the output files for the design such as packaging files, board (.brd) files, reports, and the pages in the document schematic generated for the design.
Packaged	Contains the packaging files for the design.

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Navigating the Design and Viewing Files

Folder Name	Folder Contents
Physical	Contains the board layout related files for the design. Double-click on a board (.brd) file to open it in Allegro PCB Editor.
Reports	Contains the reports generated for the design. Double-click on a report to view the report in System Connectivity Manager.
Document Schematic	Contains the pages for the document schematic generated for your design. Double-click on a schematic page to open it in Design Entry HDL.
Misc. Files	Contains any other file you added in the File Viewer. For more information on adding files in the File Viewer, see Adding New Files on page 234. Double-click on a file to open it in its associated program.

Working with Files in the Hierarchy Viewer

You can use the File Viewer to add, open and remove files, and view the properties of a file. For more information, see the following sections:

[Adding New Files](#) on page 234

[Opening Files](#) on page 235

[Removing Files](#) on page 235

[Displaying File Properties](#) on page 235

Adding New Files

1. Select the folder in which you want to add a file, right-click and choose *Add File*.

The *Open* dialog box appears.

2. Select the file and click *Open*.

The file is added in the folder.

Opening Files

To open a file, do one of the following:

- Double-click on the file.
- Select the file, right-click and choose *View File*.

The file is opened in its associated program. For example, if you open a board file, it is opened in Allegro PCB Editor. If you open a PDF file, it is opened in Adobe Acrobat.

Removing Files

1. To remove a file, do one of the following:
 - Select the file and press the *Delete* key.
 - Select the file, right-click and choose *Remove File*.

Displaying File Properties

To display the properties of any file in the File Viewer:

1. Select the file.
2. Right-click and choose *Properties*.

The Properties dialog box appears displaying the properties of the file.

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Navigating the Design and Viewing Files

Using the Physical View

This chapter contains the following sections describing the physical view in System Connectivity Manager.

- [Overview](#) on page 238
- [Accessing the Physical View](#) on page 238
- [Understanding the Physical View User Interface](#) on page 239
- [Working in the Physical View](#) on page 248

Overview

The physical view is a physical netlist view of the design as it appears in your board layout. It displays all the physical components and nets in the design, including the associated components used for terminations, pullups, pulldowns, or bypass capacitors. You can use the physical view to:

- Debug the design with respect to the board layout.

As the physical view displays the same information as in the board layout in Allegro PCB Editor, you can quickly compare the board layout with the physical view for debugging purposes.

- Verify whether you have assigned the correct signal integrity (SI) models on components and pins, and assign SI models, if required.

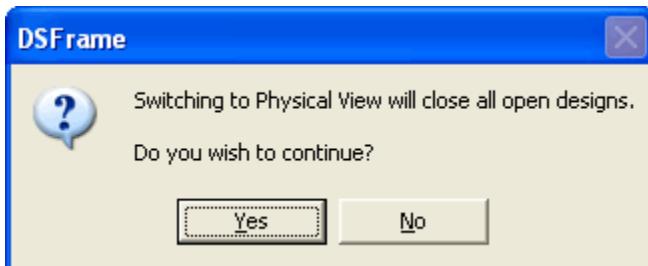
For more information on assigning SI models, see [Assigning SI Models on page 323](#).

Accessing the Physical View

To access the physical view, do the following:

1. Choose *View – Physical View*.

If the logical view of the design is already open, the following message is displayed:



2. Click *Yes* to switch to the physical view.

A tab for the root (top-level) design opens. This tab displays all the components and signals that exist in the root design and all its lower-level blocks.

Note: To open the physical view of a lower-level block, open the block for editing in master mode, click the tab for the block, and choose *View – Physical View*. The physical view of the block displays all the components and signals that exist in the block and its lower-level blocks. For more information on editing blocks in master mode, see [Editing a Hierarchical Design on page 356](#).

System Connectivity Manager User Guide

Using the Physical View

System Connectivity Manager's title bar indicates that you are now in the physical view. For example, if you switch to the physical view when you are editing a design named ROM, the System Connectivity Manager title bar displays:

[ROM [In Phys]]

Note the following:

- System Connectivity Manager will save the unsaved changes before switching between the logical and physical view.
- System Connectivity Manager displays only one view at a time. When the physical view opens, the logical view closes and vice versa.

Understanding the Physical View User Interface

The physical view has the following four components:

- Physical Part List
- Physical Net List
- Physical Part Connectivity Details Pane
- Physical Net Connectivity Details Pane

Physical Part List

The Physical Part List displays the details of all components that go in the board. These components include all components displayed in the logical view and all associated components used for terminations, pullups, pulldowns, or bypass capacitors.

System Connectivity Manager User Guide

Using the Physical View

Physical Part List			
Ref Des	Foot Print	Physical Name	SI Model
*	*	*	*
R3	1206_T	RESD-1K	DEFAULT_RESISTOR_1000OHM_2_1
R4	1206_T	RESD-10K	DEFAULT_RESISTOR_10000OHM_2_1
R6	1206_T	RESD-1K	DEFAULT_RESISTOR_1000OHM_2_1
U1	SOIC32	TC55B4257_SOIC-BASE	
U2	SOIC32	TC55B4257_SOIC-BASE	
U3	PLCC84	EPF8282A_PLCC-BASE	
U4	SOIC32	TC55B4257_SOIC-BASE	
U5	SOIC32	TC55B4257_SOIC-BASE	
U6	SOIC16	DS90LV031TM_SOIC16	DS90C031TM

Filter

The Physical Part List displays the following information for each component:

- | | |
|---------------|--|
| Ref Des | Displays the reference designator of components. |
| Footprint | Displays the name of the footprint for the components. |
| Physical Name | Displays the physical part name of components. |
| SI Model | Displays the name of the signal integrity (SI) model assigned to components.

For more information on assigning SI models to components, see Assigning SI Models to Components and Pins on page 250.

For more information on removing SI models assigned to components, see Removing a Model Assignment on page 334. |
| Filter | The filter row lets you use the wildcard characters * and ? and regular expressions to filter the display of information in the Physical Part List.

For more information on filtering the display of information in the panes in System Connectivity Manager, see Filtering the Display of Information in System Connectivity Manager on page 77. |

Physical Net List

The Physical Net List displays the details of nets attached to components in the design.

Physical Net List		
T..	Phys Name	Conn
*	*	*
G	1.V	5
G	12V	17
L	ADDRESS7	4
L	ADDRESS<0>_1	0
L	ADDRESS<1>_1	0
L	ADDRESS<2>_1	0
L	ADDRESS<3>_1	0

Filter

The Physical Net List displays the following information for each net:

Type Displays the signal type of a net. The following icons are used to indicate the signal type:

 Input signal

 Output signal

 Inout signal

 Global signal

 Local signal

Phys Name Displays the physical net name of a net.

Conn Displays the number of pins connected to a net.

Filter The filter row lets you use the wildcard characters * and ? and regular expressions to filter the display of information in the Physical Net List.

For more information on filtering the display of information in the panes in System Connectivity Manager, see [Filtering the Display of Information in System Connectivity Manager](#) on page 77.

Note the following:

- If you have aliased nets in a design, the Physical Net List displays:

System Connectivity Manager User Guide

Using the Physical View

- ❑ The physical net name for the base net.

For more information on base nets, see [Declaring an Aliased Net as the Base Net](#) on page 153.

- ❑ Connections equal to the sum of connections for the base net and the nets aliased to it.

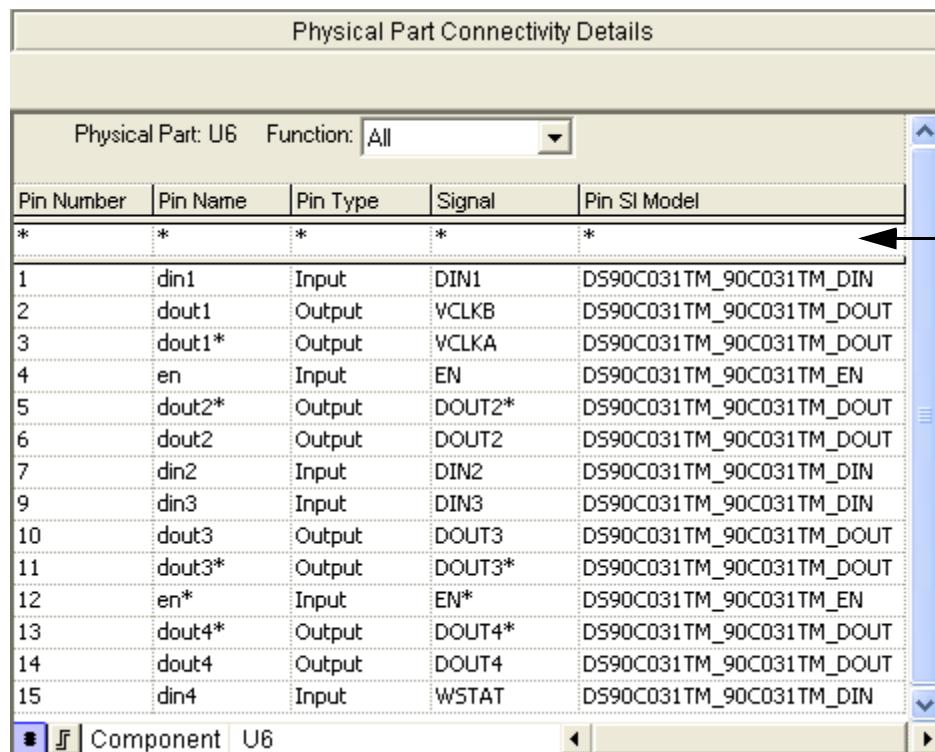
For example, if you have a signal `RESET_CPU` with four connections aliased to another signal `RESET_CPU1` that has three connections, the Physical Net List displays seven connections for the base net `RESET_CPU`.

- For global signals that run across multiple levels of a design, the Physical Net List displays the number of connections equal to the sum of connections that the global signal has at each level of the design hierarchy.

Consider you have a hierarchical design of three levels, with a `TOP` design containing a `MID` design and the `MID` design containing the `LOW` design. Assume there is a global signal `VCC` and there are six connections of `VCC` in `TOP`, seven connections of `VCC` in `MID`, and three connections of `VCC` in `LOW`, then the Physical Net List will show the `VCC` signal with 15 connections.

Physical Part Connectivity Details Pane

If you select a component in the Physical Part List, the Physical Part Connectivity Details pane appears showing the connectivity information for the selected component.



The screenshot shows the 'Physical Part Connectivity Details' pane. At the top, it displays 'Physical Part: U6' and a 'Function:' dropdown set to 'All'. Below is a table with columns: Pin Number, Pin Name, Pin Type, Signal, and Pin SI Model. The table lists 15 pins for component U6, including various inputs (din1, dout1, en, din2, din3, din4) and outputs (dout1*, dout2*, dout2, dout3, dout3*, dout4*, dout4). The 'Function:' dropdown is highlighted with a black arrow and labeled 'Filter'.

Pin Number	Pin Name	Pin Type	Signal	Pin SI Model
*	*	*	*	*
1	din1	Input	DIN1	DS90C031TM_90C031TM_DIN
2	dout1	Output	VCLKB	DS90C031TM_90C031TM_DOUT
3	dout1*	Output	VCLKA	DS90C031TM_90C031TM_DOUT
4	en	Input	EN	DS90C031TM_90C031TM_EN
5	dout2*	Output	DOUT2*	DS90C031TM_90C031TM_DOUT
6	dout2	Output	DOUT2	DS90C031TM_90C031TM_DOUT
7	din2	Input	DIN2	DS90C031TM_90C031TM_DIN
9	din3	Input	DIN3	DS90C031TM_90C031TM_DIN
10	dout3	Output	DOUT3	DS90C031TM_90C031TM_DOUT
11	dout3*	Output	DOUT3*	DS90C031TM_90C031TM_DOUT
12	en*	Input	EN*	DS90C031TM_90C031TM_EN
13	dout4*	Output	DOUT4*	DS90C031TM_90C031TM_DOUT
14	dout4	Output	DOUT4	DS90C031TM_90C031TM_DOUT
15	din4	Input	WSTAT	DS90C031TM_90C031TM_DIN

Component U6

The Physical Part Connectivity Details pane displays the following information:

Function

The *Functions* drop-down list appears if you are viewing the connectivity information for a component that has more than one function.

In the *Functions* drop-down list:

- Select *All* to view the pins of all the sections in the package.
- Select the section number to view only the pins for the section in the package. This lets you focus on editing the connectivity information on the pins for the section in the package.

Pin Number

Displays the pin number.

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Using the Physical View

Pin Name	Displays the pin name.
Pin Type	Displays the pin type.
Signal	Displays the name of the signal connected to the pin.
Pin SI Model	Displays the name of the signal integrity (SI) model assigned to the pin. For more information on assigning SI models to pins, see Assigning SI Models to Components and Pins on page 250. For more information on removing SI models assigned to pins, see Removing a Model Assignment on page 334.
Filter	The filter row lets you use the wildcard characters * and ? and regular expressions to filter the display of information in the Physical Part Connectivity Details pane. For more information on filtering the display of information in the panes in System Connectivity Manager, see Filtering the Display of Information in System Connectivity Manager on page 77.
	Click this icon to display the list of components in the design, as shown below.

Name	RefDes	Cell
U1	TC55B4257_SOIC-BASE	
U2	TC55B4257_SOIC-BASE	
U4	TC55B4257_SOIC-BASE	
U5	TC55B4257_SOIC-BASE	
U3	EPF8282A_PLCC-BASE	
U6	DS90LV031TM_SOIC16	
R1	RESD-10K	
R2	RESD-10K	
R4	RESD-10K	
R3	RESD-1K	
R6	RESD-1K	
C1	CAP-0.1UF	
C2	CAP-0.1UF	
C3	CAP-47UF	
C4	CAP-47UF	

You can select a component in this list to display its connectivity information in the Physical Part Connectivity Details pane.

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Using the Physical View



Click this icon to display the list of signals in the design, as shown below.

Name	Phys Name
VCC	
GND	
WSTAT	
RA<0>	
RA<1>	
RA<2>	
RA<3>	
RA<4>	
RA<5>	
RA<6>	
RA<7>	
RA<8>	
RA<9>	
RA<10>	
RA<11>	

You can select a signal in this list to display its connectivity information in the Physical Net Connectivity Details pane. For more information on using the Physical Net Connectivity Details pane, see [Physical Net Connectivity Details Pane](#) on page 245.

You can select a pin in the Physical Part Connectivity Details pane and edit connectivity for the pin in the logical view. For more information, see [Making Connectivity Changes in the Physical View](#) on page 249.

Physical Net Connectivity Details Pane

You can view the connectivity of a physical net in the Physical Net Connectivity Details pane. To do this, do one of the following:

- Double-click on a net in the Physical Net List pane.

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Using the Physical View

- Select a net in the Physical Net List pane and choose *Design – View Connectivity*.

Physical Net Connectivity Details				
GND				
Ref Des	Pin Name	Pin Number	Pin Type	Pin SI Model
*	*	*	*	*
C1	b	2	Inout	DefaultBIModel
C2	b	2	Inout	DefaultBIModel
C3	b	2	Inout	DefaultBIModel
C4	b	2	Inout	DefaultBIModel
R1	a	1	Inout	DefaultBIModel
R2	a	1	Inout	DefaultBIModel
U1	eo*	27	Input	
U2	eo*	27	Input	
U3	nsp	75	Input	
U3	msel0	74	Input	
U3	msel1	53	Input	
U4	eo*	27	Input	
U5	eo*	27	Input	

Filter

The Physical Net Connectivity Details pane displays the following information:

Ref Des	Displays the reference designator of the component whose pin is connected to the net.
Pin Name	Displays the name of the pin connected to the net.
Pin Number	Displays the number of the pin connected to the net.
Pin Type	Displays the pin type of the pin connected to the net.
Signal	Displays the name of the signal connected to the pin.
SI Model	Displays the name of the signal integrity (SI) model assigned to the pin. For more information on assigning SI models to pins, see Assigning SI Models to Components and Pins on page 250.

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Using the Physical View

Filter

The filter row lets you use the wildcard characters * and ? and regular expressions to filter the display of information in the Physical Net Connectivity Details pane.

For more information on filtering the display of information in the panes in System Connectivity Manager, see [Filtering the Display of Information in System Connectivity Manager](#) on page 77.



Click this icon to display the list of components in the design, as shown below.

Name	RefDes	Cell
U1		TC55B4257_SOIC-BASE
U2		TC55B4257_SOIC-BASE
U4		TC55B4257_SOIC-BASE
U5		TC55B4257_SOIC-BASE
U3		EPF8282A_PLCC-BASE
U6		DS90LV031TM_SOIC16
R1		RESD-10K
R2		RESD-10K
R4		RESD-10K
R3		RESD-1K
R6		RESD-1K
C1		CAP-0.1UF
C2		CAP-0.1UF
C3		CAP-47UF
C4		CAP-47UF

You can select a component in this list to display its connectivity information in the Physical Part Connectivity Details pane. For more information on using the Physical Part Connectivity Details pane, see [Physical Part Connectivity Details Pane](#) on page 243.

System Connectivity Manager User Guide

Using the Physical View



Click this icon to display the list of signals in the design, as shown below.

Name	Phys Name
VCC	
GND	
WSTAT	
RA<0>	
RA<1>	
RA<2>	
RA<3>	
RA<4>	
RA<5>	
RA<6>	
RA<7>	
RA<8>	
RA<9>	
RA<10>	
RA<11>	

You can select a signal in this list to display its connectivity information in the Physical Net Connectivity Details pane.

You can select a pin in the Physical Net Connectivity Details pane and edit connectivity for the pin in the logical view. For more information, see [Making Connectivity Changes in the Physical View](#) on page 249.

Working in the Physical View

This section describes the following procedures for working in the physical view:

- [Making Connectivity Changes in the Physical View](#) on page 249
- [Working with Properties and Electrical Constraints](#) on page 249
- [Assigning SI Models to Components and Pins](#) on page 250
- [Excluding and Including Blocks](#) on page 250
- [Changing Reference Designators](#) on page 251
- [Changing Physical Net Names](#) on page 251

Making Connectivity Changes in the Physical View

You cannot make connectivity changes in the physical view. However, System Connectivity Manager allows you to select a pin in the Physical Part Connectivity Details or the Physical Net Connectivity Details pane and edit the connectivity for the pin in the logical view.

Note: You cannot select the pin of an associated component (component used in terminations, bypass capacitors and pullups or pulldowns) and edit its connectivity in the logical view.

To make connectivity changes in the physical view

1. Select the pin in the Physical Part Connectivity Details or the Physical Net Connectivity Details pane.
2. Right-click and choose *Edit Logical Pin* from the shortcut menu.

System Connectivity Manager switches to the logical view. The pin is selected in the Component Connectivity Details pane.

Note: If you select a pin of a component that exists in a sub-block in the design, the sub-block is opened for editing in the context mode. For more information on editing a block in the context mode, see [Editing a Hierarchical Design](#) on page 356.

3. Make the required connectivity changes.

For more information on using the Component Connectivity Details pane to make connectivity changes, see [Component Connectivity Details Pane](#) on page 54.

4. Switch back to the physical view, if required.

Working with Properties and Electrical Constraints

For more information on working with properties and electrical constraints, see [Chapter 10, “Working with Properties and Electrical Constraints.”](#)

Note: The Properties window (choose *View – Properties Window*) in the physical view displays only the properties on component instances. User properties and component definition properties (properties defined in the physical part table files (.ptf) files) are not displayed in the Properties window.

Assigning SI Models to Components and Pins

For more information on assigning SI models to components and pins in the physical view, see [Assigning SI Models](#) on page 323.

Excluding and Including Blocks

When you are debugging a design in the physical view, you might want to limit the view to only the blocks where errors are reported. System Connectivity Manager lets you do this by including or excluding blocks from the physical view. When you exclude a block from the physical view, the components and nets in the excluded block are not displayed in the physical view.

Note: If an interface net is connected to components in a block that you excluded, the Physical Net Connectivity Details pane does not display the connectivity of the interface net in the excluded block.

To exclude or include blocks in the physical view:

- Choose *Design – Filter Blocks*.

The *Physical View Block Selection* dialog box appears and displays the hierarchy of the blocks in the design.

- To include blocks, do one of the following:
 - Select the check box next to a block to include the block.
 - If a block is not already included, right-click on the block then choose:
 - *Include* to include the block.
 - *Include All Occurrences* to include all occurrences of the block.
 - Click *Include All* to include all the blocks.
- To exclude blocks, do one of the following:
 - Clear the check box next to a block to exclude the block.
 - If a block is not already excluded, right-click on the block then choose:
 - *Exclude*, to exclude the block
 - *Exclude All Occurrences*, to exclude all occurrences of the block
 - Click *Exclude All*, to exclude all the blocks.

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If you include or exclude a top-level block, all the blocks under it will also be automatically included or excluded.

Note: If you have excluded blocks from the physical view, the status bar displays the text *FLTR* as shown below.



Changing Reference Designators

To change the reference designator for a component:

1. Select the component in the Physical Part List.
2. Choose *Object – Change – Ref Des.*

The reference designator of the component is selected.

3. Enter the new reference designator.

Changing Physical Net Names

To change the physical net name of a net:

1. Select the net in the Physical Net List.
2. Choose *Object – Change – Phys Name.*

The physical name of the net is selected.

3. Enter the new physical net name.

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Using the Physical View

Working with Properties and Electrical Constraints

This chapter describes the following sections:

- [About Properties](#) on page 254
- [Predefined and User-Defined Properties](#) on page 254
- [Working with Properties](#) on page 255
- [About Electrical Constraints](#) on page 274
- [Working with Electrical Constraints](#) on page 274
- [Cross Probing between System Connectivity Manager and Constraint Manager](#) on page 275
- [System Connectivity Manager to Allegro PCB Editor Property Flow](#) on page 276

About Properties

Properties (also called attributes) are used to convey information about a design. Properties carry such information as the part number of a component, the voltage of a net and so on. Properties consist of a name and value. Some properties have a set of standard values that you can use; other properties support any value that you assign.

Note the following when working with properties:

- The maximum permissible length for a property name is 31 characters and that for a property value is 255 characters.
- You can use only the following characters in property names:
 - Uppercase letters A to Z
 - Lowercase letters a to z
 - Numbers 1 to 9
 - - (hyphen)
 - _ (underscore)
- Do not start property names with the letters CDS_. The letters CDS_ is reserved for system generated properties.
- You must not assign a string value to a property that has the integer data type.
- Property value should not be null (empty). System Connectivity Manager does not allow you to add properties with null value.

Note: If a property on the symbol or physical part table (.ptf) file of a component has a null value, the component will not be packaged, and packaging errors are displayed in the Violations window.

Predefined and User-Defined Properties

System Connectivity Manager supports a predefined set of properties that you can add on design objects (component, net or pin).

You can also add user-defined properties to capture a characteristic of a design object. You can define new user-defined properties in System Connectivity Manager or in Constraint Manager. System Connectivity Manager and Constraint Manager do not perform any design rule checks or analysis on user-defined properties; they facilitate communication of the

design intent to down-stream tools in which you may want to manipulate the design objects associated with these properties.

Working with Properties

You can assign properties to design components, using one of the following methods.

- Using System Connectivity Manager

You can use the Properties window in System Connectivity Manager to work with properties on individual components, nets and pins in your design. For more information, see [Using System Connectivity Manager to Manage Properties](#) on page 255.

- Using Constraint Manager

You can also use Constraint Manager to capture and manage property information across your design. Constraint Manager provides a spreadsheet interface that helps you to quickly work with properties across your design. The changes you make to properties in Constraint Manager are displayed in System Connectivity Manager. Similarly, the changes that you make to properties in System Connectivity Manager are displayed in Constraint Manager. For more information, see [Using Constraint Manager to Manage Properties](#) on page 274.

Using System Connectivity Manager to Manage Properties

You can use the *Properties* window in System Connectivity Manager to work with properties on individual components, nets and pins in your design.

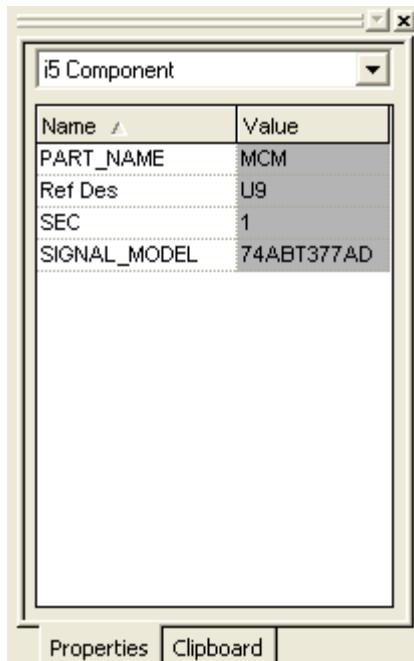
The following sections describe how you can work with properties in System Connectivity Manager:

- [Adding Properties in System Connectivity Manager](#) on page 256
- [Finding Properties in a Design](#) on page 258
- [Replacing Properties in the Design](#) on page 259
- [Deleting Properties in System Connectivity Manager](#) on page 262
- [Sorting Properties in System Connectivity Manager](#) on page 262
- [Viewing the Origin of a Property in System Connectivity Manager](#) on page 262

- [Working with User-Defined Properties in System Connectivity Manager on page 263](#)

Adding Properties in System Connectivity Manager

1. Choose *View – Properties Window* to display the Properties window.



2. Select the object (component, net or pin) on which you want to add properties.

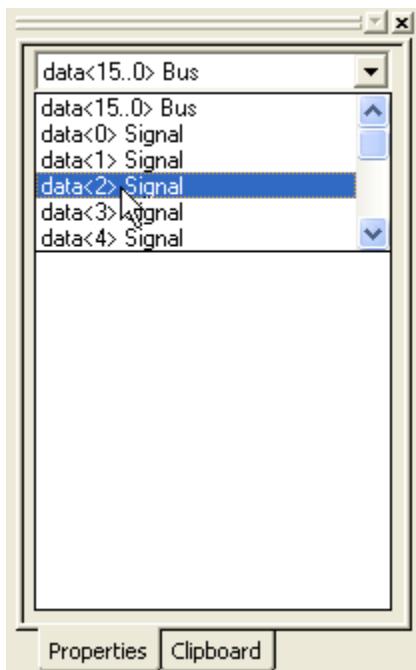
The object name and the properties on the object are displayed in the *Properties* window.

Note the following:

- If you select a bus (vectored net), you cannot add properties on the bus. You can add properties only on the bits of the bus.

To add properties on a bit of a bus, select the bit from the drop-down list. For example, if you select a bus named DATA<15 .. 0>, the Properties window displays

DATA<15..0> Bus. Click the drop-down list to select the bit on which you want to add properties.



- If you select a vector pin, you can add properties on the vector pin and on the bits of the vector pin. A property you specify on a vector pin applies to all the bits of the vector pin. A property you specify on a bit of a vector pin overrides the same property you specify on the vector pin.

To add properties on a bit of a vector pin, select the bit from the drop-down list. For example, if you select a vector pin named CLOCK<7..0>, the Properties window displays CLOCK<7..0> Pin. Click the drop-down list to select the bit on which you want to add properties.

3. Click in the *Properties* window and press the *Insert* key or right-click and choose *Insert Property*.

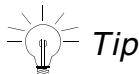
An empty row appears in the *Properties* window.

4. To add a property, click the *Name* drop-down list to select the property.

The *Name* drop-down list displays the list of predefined properties supported in System Connectivity Manager and the user-defined properties you defined in System Connectivity Manager or in Constraint Manager.

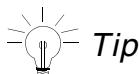
Note: You can define user-defined properties. For more information, see [Working with User-Defined Properties in System Connectivity Manager](#) on page 263.

5. Enter the value of the property in the *Value* field next to the property.



Tip

You can use the Expanded Signal List to select a bit of a bus in the Expanded Signal List to view and edit the properties on the bit.



Tip

You can click on a bit of a vector pin in the Component Connectivity Details pane to view and edit the properties on the bit.

Finding Properties in a Design

You can use the Global Find dialog box to find all the objects (components, nets or pins) in the design on which a property exists. You can then highlight an object on which the property exists in the design.

1. Choose *Project – Global Find*.

The Global Find dialog box appears.

2. Select the *Properties* option.

3. In the *Name* field, do one of the following:

- Enter the name of the property you want to search.
- Use the * and ? wildcard characters to specify the property name.

For example, to find any property with the value CPU, enter * in the *Name* field and enter CPU in the *Value* field.

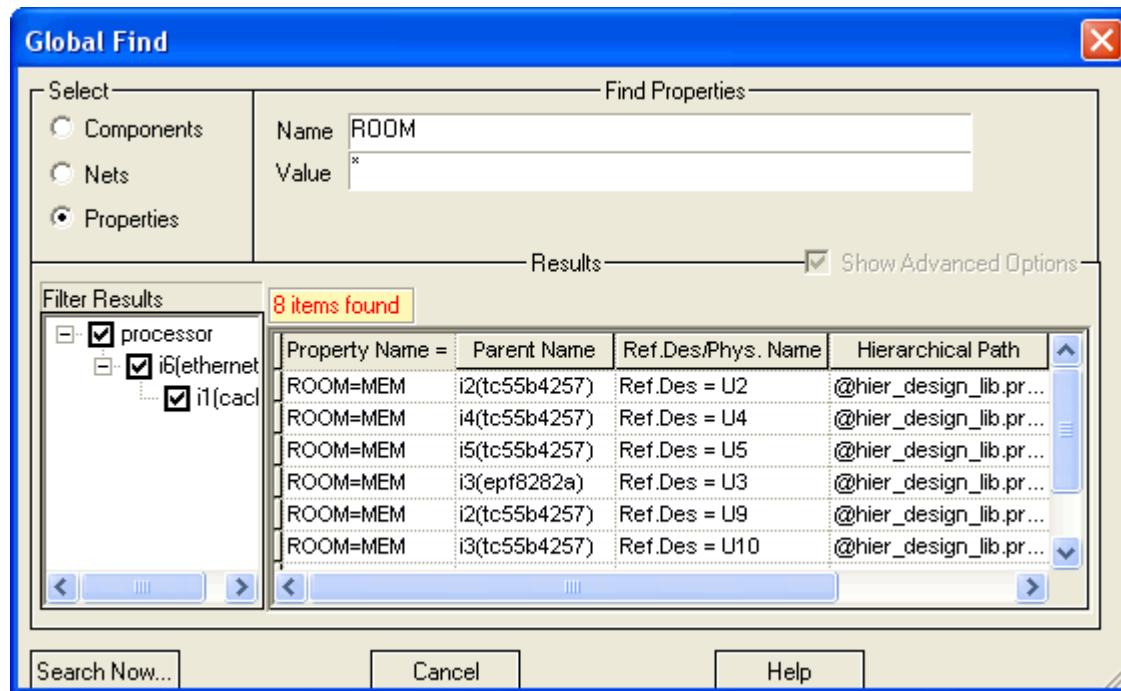
4. In the *Value* field, do one of the following:

- Enter the value of the property if you want to find only the properties having the specific value.
- Use the * and ? wildcard characters to specify the property value.

For example, to find the property named ROOM with any value, enter ROOM in the *Name* field and enter * in the *Value* field.

5. Click *Search Now*.

The objects (components, nets or pins) on which the property exists are displayed in the *Results* list.



6. In the *Filter Results* box:

- Clear the check box next to a block name if you want to do not want to view the search results for that block.
- Select the check box next to a block name if you want to view the search results for that block.

7. To highlight an object (component, net or pin) on which the property exists, select the row for the object in the *Results* list, right-click and choose *Highlight*.

The object is highlighted in the design.

Replacing Properties in the Design

You can use the Global Replace dialog box to find and replace properties across all blocks in a design.

Note: Global Replace will replace properties in all the spreadsheet and Verilog blocks in a hierarchical design. However, Global Replace will not replace properties in schematic blocks and in read-only blocks. To replace properties in schematic blocks, open the block in Design

Entry HDL and perform Global Replace in Design Entry HDL. For more information on working with read-only blocks, see [Working with Read-Only Blocks in your Design](#) on page 380.



Exercise caution when performing global replace because global replace impacts property information across all levels of a hierarchical design.

1. Choose Project – Global Replace.

The Global Replace dialog box appears.

2. Select the Properties tab.

3. In the *Name* field, enter the name of the property you want to replace.

4. In the *Value* field, do one of the following

- Enter the value of the property if you want to replace only the properties having the specific value.
- Enter an * (asterisk) to replace properties having the specified property name with any value.

5. In the *Select Property to REPLACE* group box, do the following.

- a. In the *Name* field, enter the name of the property you want to use to replace the original property.**
- b. In the *Value* field, enter the value for the new property.**

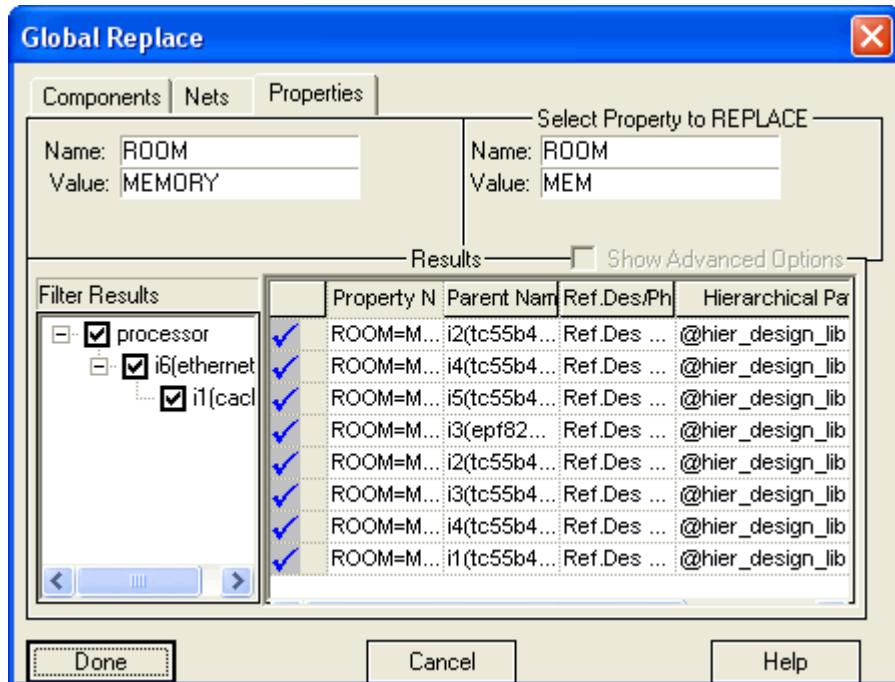
Note: If you want to modify only the value of a specific property, enter the same property name in the *Name* field and enter the new property value in the *Value* field.

6. Click *Replace*.

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Working with Properties and Electrical Constraints

The Global Replace dialog box displays the objects (components, nets, or pins) on which the property has been replaced in the design.



The ✓ icon indicates that the properties on an object have been replaced successfully.

7. In the *Filter Results* box:

- ❑ Clear the check box next to a block name if you want to do not want to view the search results for that block.
- ❑ Select the check box next to a block name if you want to view the search results for that block.

8. To highlight an object (component, net or pin) on which the property has been replaced, select the row for the object in the *Results* list, right-click and choose *Highlight*.

The object is highlighted in the design.

9. Click *Done* to close the Global Replace dialog box.

Deleting Properties in System Connectivity Manager

1. Choose *View – Properties Window* to display the *Properties* window.
2. Select the object (component, net or pin) on which you want to delete properties.

The object name and the properties on the object are displayed in the *Properties* window.

Note: To delete a property from a bit of a bus (vectored net), select the bit from the drop-down list.

3. Select the property you want to delete and press the *Delete* key.

Note: You can also cut, copy and paste property values.

Note: You cannot paste property names in the Properties window.

Sorting Properties in System Connectivity Manager

To sort the properties on an object,

- Click on the *Name* or *Value* column heading in the *Properties* window.

The column is sorted in the ascending or descending order.

Viewing the Origin of a Property in System Connectivity Manager

When you move the cursor on a property name or value in the Properties window, a tooltip appears displaying the origin of the property.

Origin of Property	Description
Symbol	Property, which the component instance inherited from its symbol. If a property on the symbol is modified in System Connectivity Manager, then its origin will become <code>Symbol+Front End User</code> .
Front End User	A property added or any other property whose value is changed by the user in System Connectivity Manager.

Origin of Property	Description
Back End User	A property added or any other property whose value is changed in Allegro PCB Editor or Allegro PCB SI. These properties will be added in System Connectivity Manager when you run <i>Import Physical</i> to update the logical design in System Connectivity Manager with the changes made in the board in Allegro PCB Editor or Allegro PCB SI.
Packager	A property whose value is assigned when the design is packaged.
Key PTF	Property, which was annotated from the part table key property section.
Injected PTF	Property, which was annotated from the part table injected property section.

Working with User-Defined Properties in System Connectivity Manager

System Connectivity Manager lets you define user-defined properties. You can use an user-defined property to capture a characteristic of an object.

You can also define user-defined properties in Constraint Manager. For more information, see the [Working with Properties in Constraint Manager](#) chapter of [System Connectivity Manager to Constraint Manager User Guide](#).

The following topics provide information on working with user-defined properties:

- [Defining User-Defined Properties in System Connectivity Manager](#) on page 263
- [Modifying the Definition of User-Defined Properties](#) on page 273
- [Deleting User-Defined Properties in System Connectivity Manager](#) on page 273

Defining User-Defined Properties in System Connectivity Manager

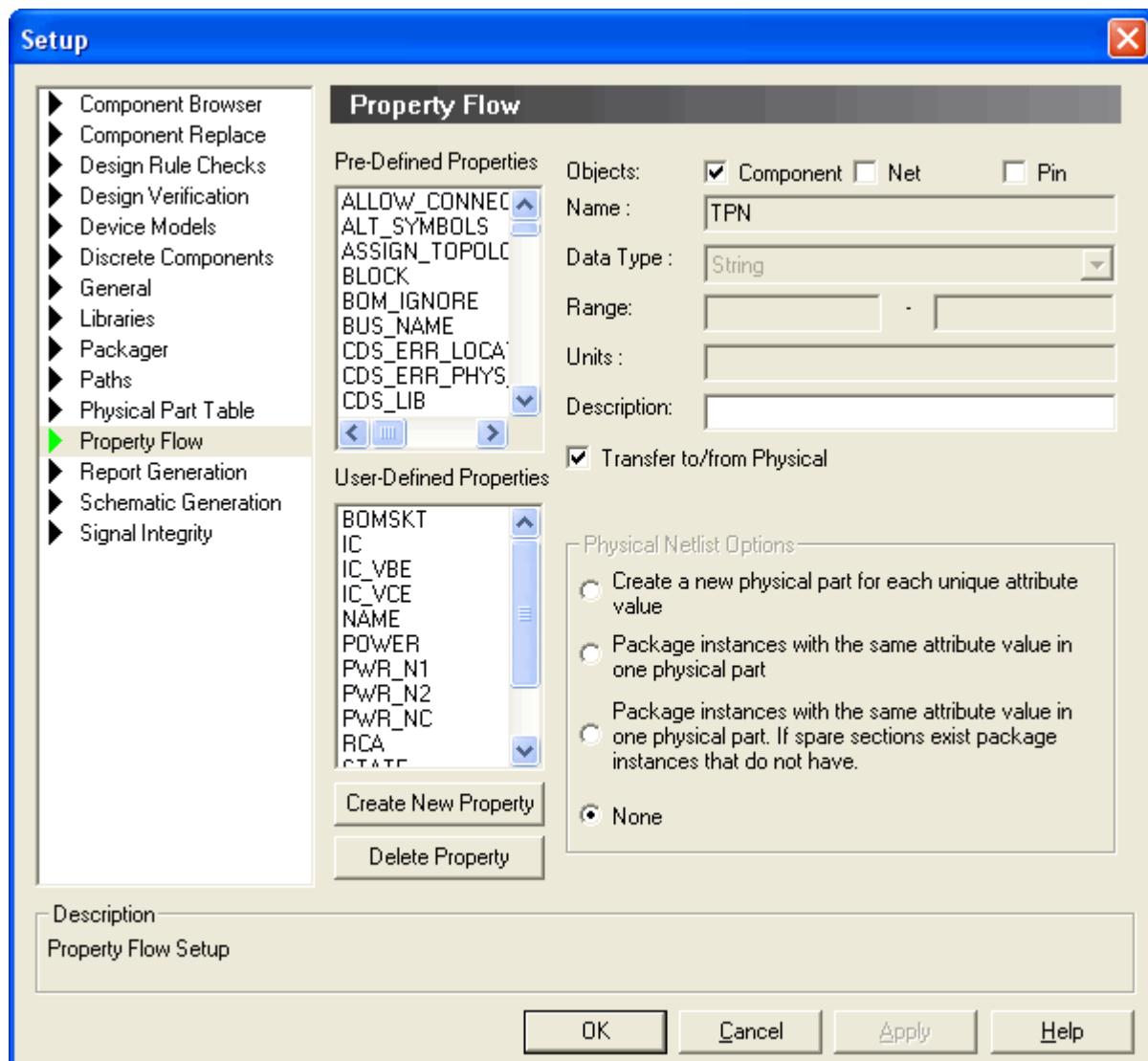
You can add user-defined properties using the Property Flow tab in the Setup dialog box or by using the Create Attribute Definition dialog box that appears when you right-click in the Properties window and choose *Create Property Definition*.

Using the Property Flow tab for defining user-defined properties

1. In System Connectivity Manager, choose *Project – Settings*.

The Setup dialog box appears.

2. Click the Property Flow tab.



3. Click the *Create New Property* button.
4. Specify the property name.
5. Choose the data type for the property.

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Working with Properties and Electrical Constraints

6. Select the check box next to the objects on which you want to be able to add the property.

Select	If
Design Instance	You want to be able to add the property on blocks.
Part Instance	You want to be able to add the property on components.
Gate Instance	You want to be able to add the property on gate components.
Pin	You want to be able to add the property on pins.
Net	You want to be able to add the property on nets.
Bus	You want to be able to add the property on vectored signals.

7. Specify the range of values that are acceptable for the property.

When you enter a property value, System Connectivity Manager displays an error message if the value is not within the specified range.

8. Enter a description for the property.
9. Select the *Transfer to/from Physical* check box if you want the property to be transferred between System Connectivity Manager and Allegro PCB Editor along with the netlist when you run *Export Physical*.

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Working with Properties and Electrical Constraints

10. If you have selected the *Component* check box in [step 6](#), specify the physical netlist options for the property.

Select

Create a new physical part for each unique property value

If

You want a new physical part to be created for each instance of a component that has the property with a unique property value.

Note: If instances of a component have the property with the same value, System Connectivity Manager packages the instances together. However, instances that do not have the property will not be packaged together with instances having the same property value for the property.

Example

If you select this option for a property named MYPROP and if you have an instance of a 74LS00 in your design with the property, MYPROP=ALT1, and another instance of 74LS00 with the property, MYPROP=ALT2, the following two physical parts are created:

- 74LS00-ALT1
- 74LS00-ALT2

If both instances of 74LS00 have the MYPROP=ALT1 property, System Connectivity Manager packages them as a single physical part named 74LS00-ALT1.

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Working with Properties and Electrical Constraints

Select

Package instances with the same property value in one physical part

If

You want component instances with the same property value for the property to be packaged together in one physical part.

Note: System Connectivity Manager does not package together instances that have different values for the same property. Further, instances that do not have a property value will not be packaged together with instances that have the same property value for the property.

Example

If you select this option for a property named MYPROP and if you have two instances of the 74LS00 component in your design with the property, MYPROP=ALT1, System Connectivity Manager packages them as a single physical part named 74LS00-ALT1.

Select	If
Package instances with the same property value in one physical part. If spare sections exist package sections that do not have.	You want component instances with the same property value for the property to be packaged together in one physical part. However, if spare sections are available, instances without the property will also be packaged together. Note: System Connectivity Manager does not package together instances that have different values for the same property. Example If you select this option for a property named MYPROP and if you have four instances of the 74LS00 component with the: <ul style="list-style-type: none">■ Instance i1 having the MYPROP=ALT1 property■ Instance i2 having the MYPROP=ALT2 property■ Instance i3 having the MYPROP=ALT1 property, and■ Instance i4 not having the MYPROP property, then System Connectivity Manager packages instances i1 and i3 together because they have the same property value. The 74LS00 component has four sections. As there are two spare sections in the package, System Connectivity Manager includes the instance i4 also in the same package because i4 does not have the MYPROP property.
None	You do not want to specify any physical netlist options for the property.

11. Click *Apply* or *OK*.

The user-defined property is created. You can now add the property on objects in the design.

Using the Properties window for defining user-defined properties

1. Choose *View – Properties Window* to display the Properties window.
2. Do one of the following:

- ❑ Click in the Properties window and press the *Insert* key or right-click and choose *Insert Property*. An empty row appears in the Properties window. Enter the name of the property in the *Name* column and press *Enter*.
- ❑ Right-click and choose *Create Property Definition*.

The Create Attribute Definition dialog box appears.

3. Specify the property name.
4. Choose the data type for the property.
5. Select the check box next to the objects on which you want to be able to add the property.

Select	If
Design Instance	You want to be able to add the property on blocks.
Part Instance	You want to be able to add the property on components.
Gate Instance	You want to be able to add the property on gate components.
Pin	You want to be able to add the property on pins.
Net	You want to be able to add the property on nets.
Bus	You want to be able to add the property on vectored signals.

6. Specify the range of values that are acceptable for the property.

When you enter a property value, System Connectivity Manager displays an error message if the value is not within the specified range.

7. Enter a description for the property.
8. Select the *Transfer to/from Physical* check box if you want the property to be transferred between System Connectivity Manager and Allegro PCB Editor along with the netlist when you run *Export Physical*.

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Working with Properties and Electrical Constraints

9. If you have selected the *Component* check box in [step 5](#), click the *Netlist Options* button and specify the physical netlist options for the component property.

Select

Create a new physical part for each unique attribute value

If

You want a new physical part to be created for each instance of a component that has the property with a unique property value.

Note: If instances of a component have the property with the same value, System Connectivity Manager packages the instances together. However, instances that do not have the property will not be packaged together with instances having the same property value for the property.

Example

If you select this option for a property named MYPROP and if you have an instance of a 74LS00 in your design with the property, MYPROP=ALT1, and another instance of 74LS00 with the property, MYPROP=ALT2, the following two physical parts are created:

- 74LS00-ALT1
- 74LS00-ALT2

If both instances of 74LS00 have the MYPROP=ALT1 property, System Connectivity Manager packages them as a single physical part named 74LS00-ALT1.

System Connectivity Manager User Guide

Working with Properties and Electrical Constraints

Select

Package instances with the same attribute value in one physical part

If

You want component instances having the same property value for the property to be packaged together in one physical part.

Note: System Connectivity Manager does not package together instances that have different values for the same property. Further, instances that do not have the property will not be packaged together with instances that have the same property value for the property.

Example

If you select this option for a property named MYPROP and if you have two instances of the 74LS00 component in your design with the property, MYPROP=ALT1, System Connectivity Manager packages them as a single physical part named 74LS00-ALT1.

Select	If
Package instances with the same attribute value in one physical part. If spare sections exist package sections that do not have.	You want component instances having the same property value for the property to be packaged together in one physical part. However, if spare sections are available, instances without the property will also be packaged together. Note: System Connectivity Manager does not package together any instances that have different values for the same property.
None	Example If you select this option for a property named MYPROP and if you have four instances of the 74LS00 component with the: <ul style="list-style-type: none">■ Instance i1 having the MYPROP=ALT1 property■ Instance i2 having the MYPROP=ALT2 property■ Instance i3 having the MYPROP=ALT1 property, and■ Instance i4 not having the MYPROP property, then System Connectivity Manager packages instances i1 and i3 together because they have the same property value. The 74LS00 component has four sections. As there are two spare sections in the package, System Connectivity Manager includes the instance i4 also in the same package because i4 does not have the MYPROP property.

10. Click *Apply* or *OK*.

The user-defined property is created. You can now add the property on objects in the design.

Modifying the Definition of User-Defined Properties

System Connectivity Manager provides support for modifying the definition of a user-defined property. To modify the definition for a user-defined property, complete the following steps/

1. In System Connectivity Manager, choose *Project – Settings*.
The Setup dialog box appears.
2. Click the Property Flow tab.
3. Select the property you want to modify in the *User-Defined Properties* list.
4. Modify the definition for the user-defined property and click *Apply* or *OK*.



Important
You cannot modify the definition of predefined properties.

Deleting User-Defined Properties in System Connectivity Manager

Note: You cannot delete the definition of predefined properties.



If you delete the definition of a user-defined property, the property is deleted from all the objects in the design on which it exists. You cannot undo deletion of the definition of user-defined properties.

To delete the definition of a user-defined property, complete the following steps.

1. In System Connectivity Manager, choose *Project – Settings*.
The Setup dialog box appears.
2. Click the Property Flow tab.
3. Select the property you want to delete in the *User-Defined Properties* list.
4. Click *Delete Property*.

The property is deleted from all the objects in the design on which it exists.

Using Constraint Manager to Manage Properties

For more information on using Constraint Manager to manage properties, see the [Working with Properties in Constraint Manager](#) chapter of [System Connectivity Manager to Constraint Manager User Guide](#).

About Electrical Constraints

A constraint is a user-defined requirement applied to an object in a design. Electrical constraints (ECs) govern the electrical behavior of an object in a design. For example, you can capture a constraint to define the maximum voltage overshoot tolerated by a net and capture the minimum first switch delay for a driver-receiver pin-pair in your design.

Working with Electrical Constraints

System Connectivity Manager lets you use the Allegro Constraint Manager tool to capture and manage high-speed electrical constraints information in your design.

Allegro Constraint Manager lets you define, view, and validate constraints at each step in the design flow, from design capture (in System Connectivity Manager and Design Entry HDL) to floorplanning (in Allegro PCB SI) to design realization (in Allegro PCB). You can also use Constraint Manager with SigXplorer to explore circuit topologies and derive electrical constraint sets which can include custom constraints, custom measurements, and custom stimulus.

Note the following when you are using Constraint Manager with SigXplorer:

- You cannot apply a topology that has low clamp, high clamp or dual clamp terminations in Constraint Manager started from System Connectivity Manager.
- You cannot apply a topology that has terminations when you are editing a block in context mode. The following message is displayed in the log file when you apply the topology in Constraint Manager.

Adding termination in context mode is not supported.

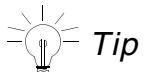
Using Constraint Manager to Capture Electrical Constraints

To start Constraint Manager, do one of the following:

- Choose *Design – Edit Constraints*.

- Click  on the toolbar.

The Constraint Manager window appears. The Constraint Manager title bar displays (connected to System Connectivity Manager). This indicates that Constraint Manager has been started from System Connectivity Manager.



Tip

You can perform cross probing from System Connectivity Manager to Constraint Manager to quickly locate objects on which you want to capture constraints in Constraint Manager. For more information, see [To perform cross probing from System Connectivity Manager to Constraint Manager](#) on page 275.

Cross Probing between System Connectivity Manager and Constraint Manager

You can perform cross probing between System Connectivity Manager and Constraint Manager to highlight components, nets and pins. This lets you quickly locate objects on which you want to add properties or constraints.

To perform cross probing from System Connectivity Manager to Constraint Manager

Do one of the following:

- In System Connectivity Manager, select a block, net, component or pin and choose *Object – Properties* or *Design – Edit Constraints*.
Switch to Constraint Manager. The selected block, net, component or pin is highlighted in Constraint Manager.
- If you have already started Constraint Manager from System Connectivity Manager, double-click on a block, net, component or pin in System Connectivity Manager.
Switch to Constraint Manager. The selected block, net, component or pin is highlighted in Constraint Manager.

To perform cross probing from Constraint Manager to System Connectivity Manager

- In Constraint Manager, select a net, component, pin or Xnet and choose *Objects – Select*.

Switch to System Connectivity Manager. The object (net, component, pin or the member nets of the Xnet) is highlighted in System Connectivity Manager.

Note: You cannot select a pin-pair, differential pair, match group or ECSet in Constraint Manager and highlight it in System Connectivity Manager.

To select multiple nets, components, pins or Xnets in Constraint Manager and highlight all of them together in System Connectivity Manager, do the following:

1. In Constraint Manager, select multiple objects (components, nets, pins or Xnets) by doing one of the following:
 - Press *Ctrl* and click to select individual objects in no particular order.
 - Press *Shift* and click to select a range of objects.
2. Choose *Objects – Select*.

Switch to System Connectivity Manager. The objects (nets, components, pins or the member nets of the Xnets) are highlighted in System Connectivity Manager.



Tip

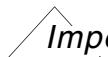
To dehighlight an object (component, pin, net or Xnet) in System Connectivity Manager, select the highlighted object in System Connectivity Manager and choose *Design – Dehighlight* in System Connectivity Manager. To dehighlight all the objects highlighted in System Connectivity Manager, choose *Design – Dehighlight All* in System Connectivity Manager.

System Connectivity Manager to Allegro PCB Editor Property Flow

All the predefined properties you add in System Connectivity Manager that are set up as transferable between System Connectivity Manager and the board are automatically passed to the board when you run *Export Physical* to update the board with the changes in System Connectivity Manager. Similarly, when you run *Import Physical* to update the design in System Connectivity Manager with the changes in the board, all the predefined properties that are set up as transferable between System Connectivity Manager and the board are automatically passed from the board to the logical design in System Connectivity Manager. For more information on *Export Physical* and *Import Physical*, see [Chapter 18, “Transferring the Logical Design to a Board and Design Synchronization.”](#)

However, before you run *Export Physical*, you must setup the options for transferring user-defined properties between System Connectivity Manager and Allegro PCB Editor.

1. In System Connectivity Manager, choose *Project – Settings*.
The Setup dialog box appears.
2. Click the Property Flow tab.
3. Select a property in the *User-Defined Properties* list.
4. Select the *Transfer to/from Physical* check box if you want the property to be transferred between System Connectivity Manager and Allegro PCB Editor when you run *Export Physical* or *Import Physical*.
5. Repeat Steps 3 and 4 for each user-defined property.
6. Click *OK* to save the changes.

 **Important**

For this update of System Connectivity Manager, when you run *Import Physical* to update the design in System Connectivity Manager with the changes in the board, the user-defined properties you setup as transferable between System Connectivity Manager and PCB Editor are not passed automatically from the board to the design in System Connectivity Manager. To push the user-defined properties from the board to System Connectivity Manager, you must define the user-defined properties in a px1BA.txt file located in the physical view of the root (top-level) design for the project.

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Working with Properties and Electrical Constraints

Working with Associated Components

This chapter describes the following sections:

- [Overview](#) on page 280
- [Terminations](#) on page 280
- [Bypass Capacitors](#) on page 298
- [Pullups and Pulldowns](#) on page 305
- [Setting Up Discrete Components](#) on page 315

Overview

Today's designs contain components, called associated components, that do not contribute to the logic of the design, but are a must for the correct functioning of the design. For example, bypass capacitors are needed for controlling power and ground bounce in the design. By definition, associated components are mostly passive devices. System Connectivity Manager classifies associated components into three categories— terminations, bypass capacitors and pullup/pulldowns.

Traditional design entry tools do not capture the association between the parent object and the associated components. This makes design entry time consuming and error prone. For example, if you move or delete the parent object to which these passive devices are attached in your schematic, you must ensure that the passive devices are also moved or deleted.

System Connectivity Manager automates the tedious task of working with associated components in your design.

In this chapter, you will learn to apply terminations, bypass capacitors and pullups or pulldowns in your design. For more information, see the following topics:

- [Terminations](#) on page 280
- [Bypass Capacitors](#) on page 298
- [Pullups and Pulldowns](#) on page 305

Terminations

Terminations are a group of components, typically resistors or diodes, added to pins or buses to prevent the reflection of electrical signals occurring at the end of buses.

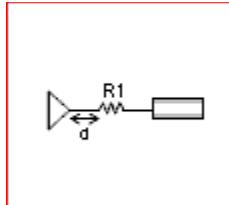
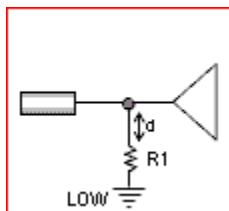
System Connectivity Manager provides you a convenient way to apply terminations. You can quickly apply a termination at the bus-level and System Connectivity Manager automatically applies it to all bits, thereby saving time and effort. You can also apply terminations to specific bits of a bus or scalar pins using multi-select or copy-paste features.

The individual components making the termination are not displayed in the Component List and new nets generated as a result of applying the termination are not displayed in the Signal List. This feature ensures that the Component List and the Signal List remain uncluttered.

Termination types

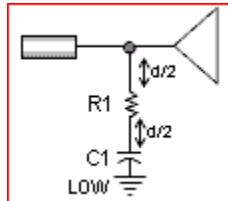
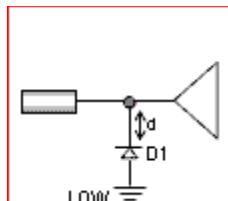
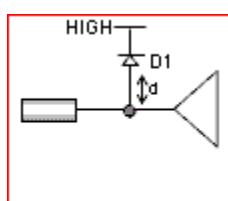
System Connectivity Manager supports seven standard termination types. You can add a standard termination by looking at its pin type.

The following table explains the different termination types, their configurations and the pin types to which they can be connected.

Termination type and usage	... has this configuration	... looks like	... is connected to the following pin types
Series Series termination is power efficient. It effectively dampens ringing and overshoot.	One resistor connected in series		output or inout
Shunt Shunt termination gives the best speed performance for an interconnection and allows the use of distributed loads. However, the required power consumption makes it unsuitable for CMOS.	One resistor		input or inout

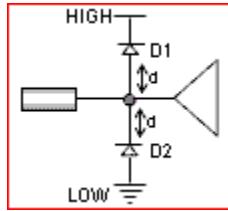
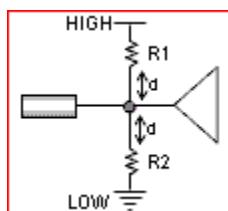
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Working with Associated Components

Termination type and usage	... has this configuration	... looks like	... is connected to the following pin types
Shunt RC	One resistor, one capacitor		input or inout
Shunt RC termination dampens signal transients. It differs from shunt termination because the capacitor blocks any DC current path and helps reduce power consumption.			
GNDClampDiode	One diode connected to a low voltage (ground diode)		input or inout
This method of termination, commonly used for DRAMs, dampens the signal overshoot at a level of -1V using a Schottky diode. It does not provide immunity to crosstalk and noise at high edge rates.			
PowerClampDiode	One diode connected to a high voltage (power diode)		input or inout
This method of termination is similar to the GNDClampDiode termination, but dampens the signal			

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Working with Associated Components

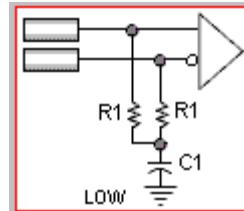
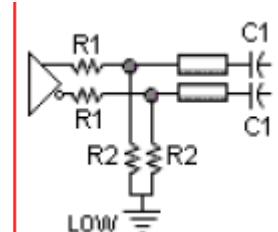
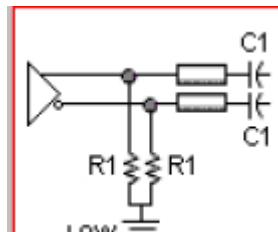
Termination type and usage	... has this configuration	... looks like	... is connected to the following pin types
DualClampDiode This method of termination is similar to the GNDClampDiode termination, but uses two diodes to dampen the signal overshoot to both -1V and +1V.	One diode connected to a low voltage another connected to a high voltage		input or inout
Thevenin This method of termination uses two components (resistors) to provide effective termination for incident wave switching while not degrading VOL and VOH as much as the parallel termination. Virtually free of duty cycle effects and suitable in both high and low frequency buses.	Two resistors, one connected to a low voltage and another connected to a high voltage		input or inout

You can create custom terminations. You can also use discrete components, such as diodes, resistors, or capacitors, to create a custom termination. For example, you can use one resistor and one diode in parallel to create a termination scheme.

Terminations on Differential Pairs

System Connectivity Manager supports adding terminations to the differential pair pins. [Table 11-1 on page 284](#) lists the terminations than can be added to differential pair pins. These terminations cannot be applied to individual pins. To know about the pin-terminations, see [Terminations on page 280](#).

Table 11-1 Differential Pair Terminations

Termination type and usage	... has this configuration	... looks like
AC Bias	Two parallel resistors connected in series with capacitor	
ACCT1 (AC-Coupled Transmission Lines)	AC-coupling is recommended for clock applications with 50% duty cycle. For optimal performance, the ESR (Effective Series Resistance) and the inductance of the capacitors should be low at the targeted frequency. Series resistors R1, are optional, and should be used in circuits with overshoots and undershoots to prevent ringing.	
ACCT2 (AC-Coupled Transmission Lines)	Same as ACCT1, but without option series resistors used to stop ringing.	

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Working with Associated Components

Table 11-1 Differential Pair Terminations, *continued*

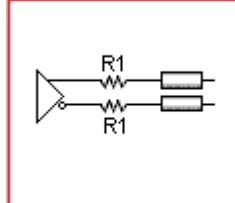
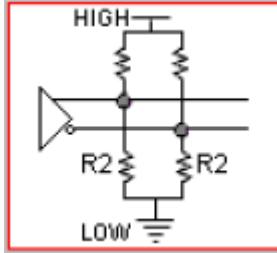
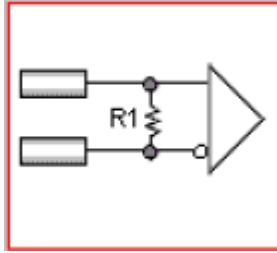
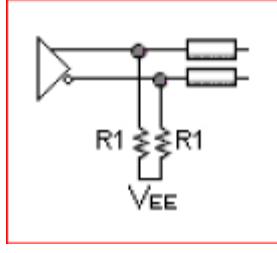
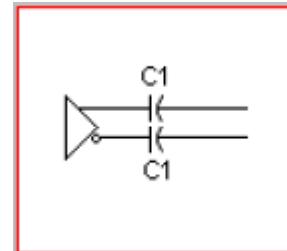
Termination type and usage	... has this configuration ... looks like
DPSeries Minimizes power dissipation	One resistor in series
	
DPThevenin	
	
LVDS (Low Voltage Differential Signal)	A termination resistor is used between the signals at the receiving device
The resistor value should match the differential load impedance of the bus	
Parallel	
Used for high-speed designs	

Table 11-1 Differential Pair Terminations, continued

Termination type and usage	... has this configuration ... looks like
SeriesCap	Capacitor in series each differential pair pin



Note: Unlike pin terminations, all differential pair terminations can be applied to all pin types.

The details about the differential pair terminations attached to differential pair pins is visible in the Associate Components window.

Working with Differential Pair Terminations

While working with differential pair terminations in System Connectivity Manager, you should take care of the following.

- If the differential pair with an associated differential pair termination, is broken, the termination is also lost and cannot be retrieved using undo or redo commands. Differential pair terminations are also lost when you use *Recompute Differential Pair* command to recreate user-defined differential pairs based on the current setup options, or when an existing model-defined differential pair is recreated because a different model was assigned to the component. In both these case, it might happen that the differential pair name remains the same, but because the differential pair were broken and then recreated, therefore, any terminations applied on the pins of the differential pair are lost.
- Differential pair terminations cannot be applied on a differential pair, if the pins of a differential pair terminal have terminations applied on them. To apply termination to a differential pair, ensure that individual pins of the differential pair do not have terminations applied on them.
- Design components that constitute a differential pair are treated as regular design components in physical layout tools, such as Allegro PCB Editor. As a result, any changes to these components in the front to back and back-to-front flow are reported in the Visual Design Differences pane as component or connectivity changes and not as termination changes.

Example

Consider a design in System Connectivity Manager, that is sync with its physical layout in Allegro PCB Editor. Modify the design by deleting a differential pair termination. If you now run the back-to-front flow, and update the logical design with all the changes, the design components, that were originally a part of the termination will get added as regular components and not as terminations.

Adding Termination Flow

To add any termination, you need to perform the following steps:

1. Ensure that the pin on which you want to add termination has a signal connected to it.
 2. Based on the pin type, decide which termination type you want to apply.
- Note:** You cannot apply terminations on Unspec pins, pins connected to DC nets and pins connected to the NC signal.
3. (Optional) Define termination setup by associating discrete components that would be used as default when defining terminations. For details, see [Defining Default Discrete Components](#) on page 315.
 4. Use the Add Termination dialog box to add a termination. For details, see [Adding a Termination](#) on page 287.
 5. Define ground or power signals with appropriate voltage property. For details, see [Adding a signal](#) on page 145.

Adding a Termination

You can add a standard termination in System Connectivity Manager using the Component Connectivity Details pane or the Signal Connectivity Details pane.

1. Do one of the following:

- In the Component List select the component on whose pins you want to add the termination.

The connectivity information for the component is displayed in the Component Connectivity Details pane.

- In the Signal List, double-click on the signal that is connected to the component pin on which you want to add the termination.

The list of pins to which the signal is connected is displayed in the Signal Connectivity Details pane.

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Working with Associated Components

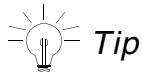
Note: You can define new power signals using the Add Signal dialog box. For details, see [Adding a signal](#) on page 145.

2. Select the row for the pin in the Component Connectivity Details pane or Signal Connectivity Details pane.
3. Do one of the following:
 - Choose *Object – Associate Components – Add Termination*.
 - Double-click on the Termination column for that pin.
 - Choose *Add Termination* from right-click menu.

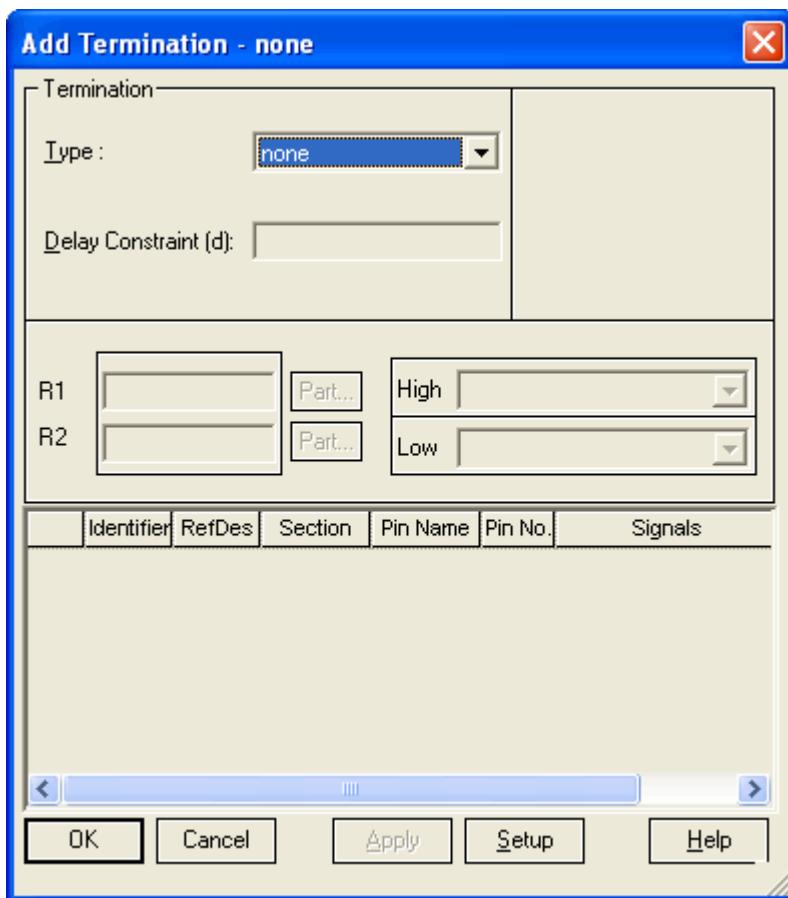
The Add Termination dialog box appears.

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Working with Associated Components



To add terminations on more than one pin at the same time, select the pins in the Component Connectivity Details pane or Signal Connectivity Details pane and choose *Object – Associate Components – Add Termination*.



4. The *Termination Type* list displays the available termination types for the selected pin type. Select the appropriate type.
5. The default delay constraint is 0.1ns. You can specify a new value.

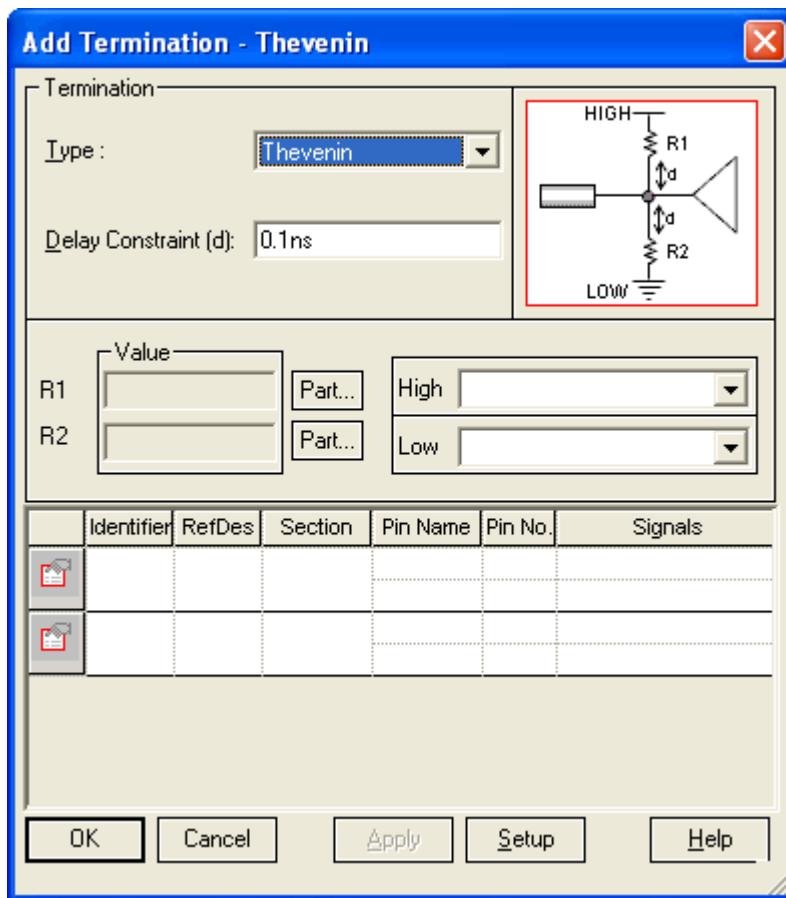
Note: Constraint Manager uses the *Delay Constraint* value to create a Propagation Delay constraint with matching value.

6. Based on the termination type you select, the Add Termination dialog box displays different fields corresponding to the discrete components used for creating the termination.

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Working with Associated Components

The following screen displays the fields that appear when you are adding a thevenin termination.



The Thevenin termination includes two resistors.

7. (Optional) You can define the default library components for resistors, capacitors and diodes in the Discrete Component Setup dialog box. For this, select the *Setup* button and make changes in the Discrete Component Setup dialog box.

Note: For more information about defining the setup of discrete components, see [Defining Default Discrete Components](#) on page 315.

8. Click the *Part* button to select each component (resistor, capacitor, or diode) making the termination.

The Adding Termination: Select Resistor dialog box appears.

Note: For more information about adding components using Part Information Manager, see [Adding Components](#) on page 107.

9. Select the component and select the part table row corresponding to the value.

10. Click *Add*.

The component value is displayed in the Add Termination dialog box.

Note: If you select a component that does not have a valid configuration, a warning message appears. You may select a new component or retain your existing selection. For more information on defining a valid capacitor component, see [Defining Valid Discrete Components](#) on page 317.

11. Select the appropriate power signals in the *High* and *Low* list boxes.

12. If you want to make changes to reference designator value or other properties for the added termination, click the *Apply* button.

Note: The *Apply* button is not available if you are adding terminations to multiple pins at the same time.

13. To change the reference designator value, select the existing value and enter a new value in the *Refdes* field.

14. Click *OK*.

The termination is applied to the selected pin in System Connectivity Manager. The type of termination is displayed in the *Termination* column in the Component Connectivity Details pane and Signal Connectivity Details pane.



Tip
If you have applied a termination to one pin, you can quickly copy it and paste it to other pins. You can also delete the termination using context sensitive menu commands.

Note: If you add a termination to a vector pin, it gets applied to all individual pins. You can individually apply another termination to a bit of a vector pin. Terminations applied to a bit of a vector pin win over the terminations applied to vector pin.

Viewing Termination Values

To view the key values for resistors, capacitors or diodes used in terminations, hover the cursor over the termination cell next to a pin in the Component Connectivity Details pane or

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Working with Associated Components

Signal Connectivity Details pane. The key values are displayed as a tooltip as shown in the figure below:

The screenshot shows the 'Component Connectivity Details' window. At the top, there is a search bar labeled 'Attach Signal:' with a dropdown menu set to '=PINNAME'. Below the search bar, the text 'Component: i8 (cy7c170) Ref Des: U5' is displayed. The main area is a table titled 'Pin Name' with columns for Pin Number, Pin Type, Signal, and Termination. A tooltip is visible over the 'Termination' column for pin 13, which is currently set to 'Shunt'. The tooltip content is 'SHUNT R=2.7K/VOLTAGE=0 V'. The table rows include:

Pin Name	Pin Number	Pin Type	Signal	Termination
*	*	*	*	*
a<11..0>	8,7,6,5,4,...	Input	a<11..0>	
io<0>	13	Inout	io<0>	Shunt
io<0>	14	Inout	io<0>	
io<0>	15	Inout	io<0>	
io<0>	16	Inout	io<0>	
ks*	9	Input	ks*	
oe*	10	Input	oe*	
we*	12	Input	we*	

Modifying a Termination

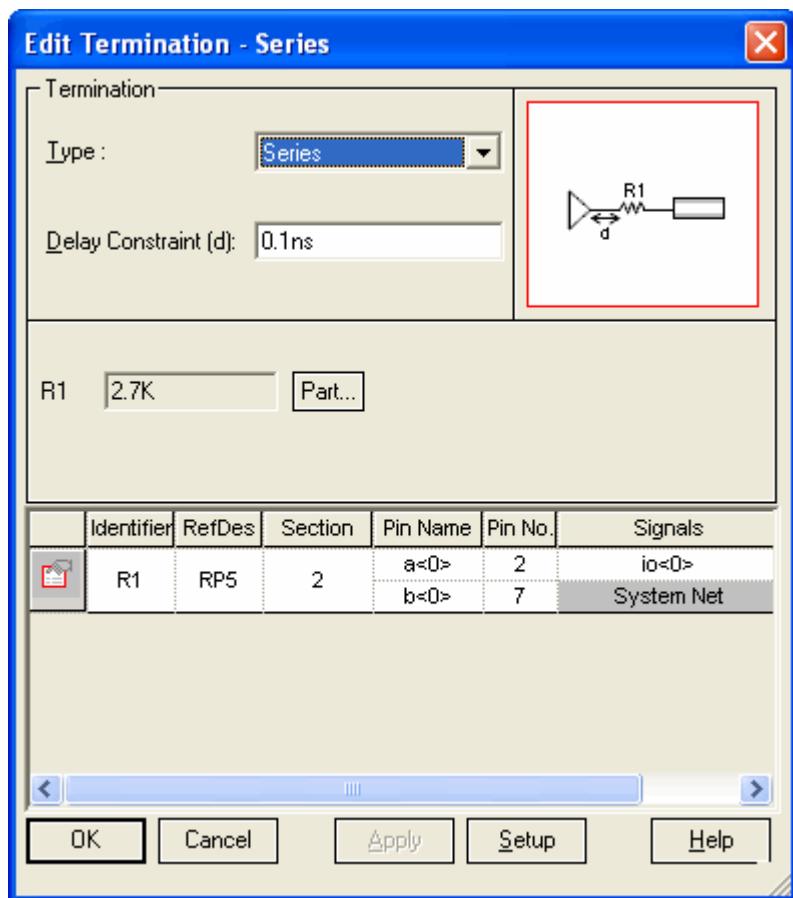
To modify a termination

- Select the termination in the Termination column and choose *Design – Edit Termination*.

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The Edit Termination dialog box appears.



Make the required changes and click *OK*.

Viewing and Modifying Properties for Termination Components

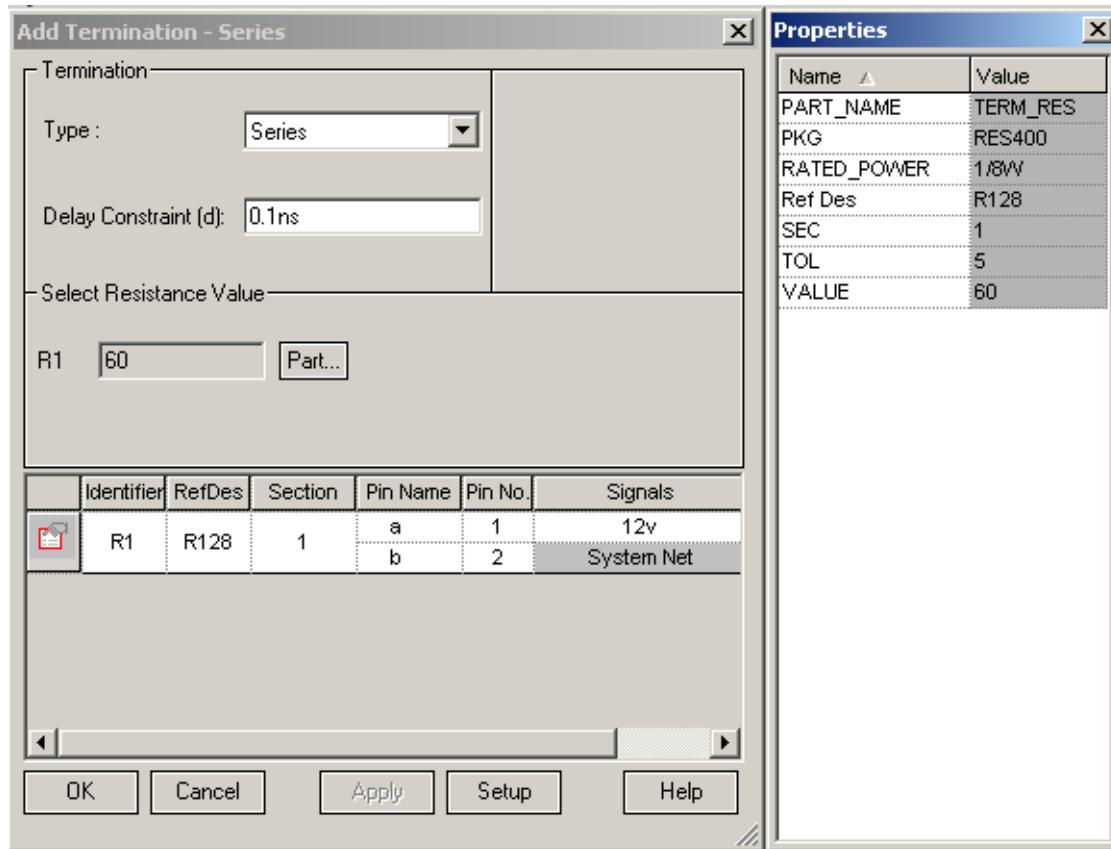
1. Select the termination in the Termination column and choose *Design – Edit Termination*.

The Edit Termination dialog box appears.

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2. Click  next to a component to display the Properties window.



3. Click *OK*.

Performing Common Operations on Terminations

You can perform the following common operations on terminations:

- **Copy**—Select any termination and click *Copy* in the context sensitive menu.
The property and connectivity information for the selected termination is copied to the Clipboard.
Note: You cannot copy a termination from a driver pin to a receiver pin or vice versa.
- **Cut**—Select any termination and click *Cut* in the context sensitive menu.
The property and connectivity information for the selected termination is copied to the Clipboard. The termination is also removed.
- **Paste**—Select any termination and click *Paste* in the context sensitive menu.

The property and connectivity information for the selected termination in the Clipboard is copied to the selected net.

- **Delete**—Select any termination and click *Delete* in the context sensitive menu.
- **Change Properties**—Select any termination and click *Properties* in the context sensitive menu.
Constraint Manager opens and you can change the desired properties.
- **Multi-select**—You can select terminations applied to multiple signals and then cut, copy or paste them across other signals.
- **Change component associated with terminations**—You can quickly change the component associated as resistor, capacitor or diode for a termination. For this, select *Edit Termination* in the context sensitive menu. This displays the Add Termination dialog box where you can change the associated components.

Deleting a Termination

To delete a termination

1. Select the termination in the Termination column and do one of the following:
 - Press the *Delete* key.
 - Choose *Design – Edit Termination*.

The Edit Termination dialog box appears. Choose *None* in the *Termination Type* drop-down list and click *OK*.

Termination Example 1

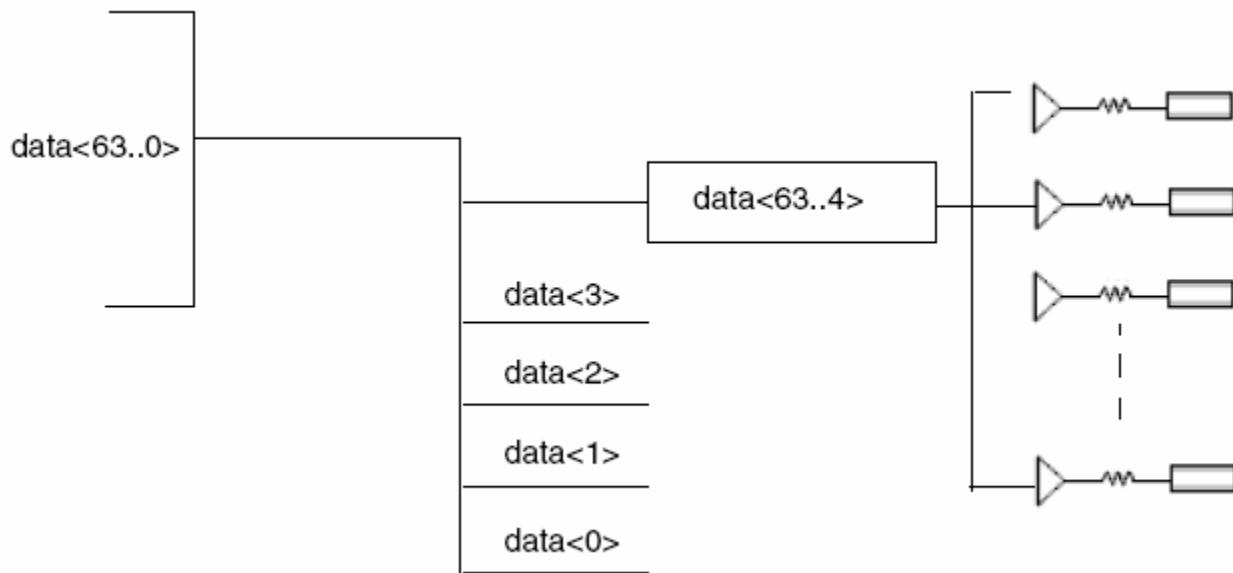
You may need to attach a series termination to a signal. For example, you may have a signal AD with series termination attached.



To add a series termination to the above signal, select the component row corresponding to the `AD` signal in the Signal Connectivity Pane. Next, add the termination. For details, see [Adding a Termination](#) on page 287.

Termination Example 2

You may need to attach series termination to data buses. For example, you may have a data bus `data<63..0>` with series terminations attached to the bits `data<63..4>`.

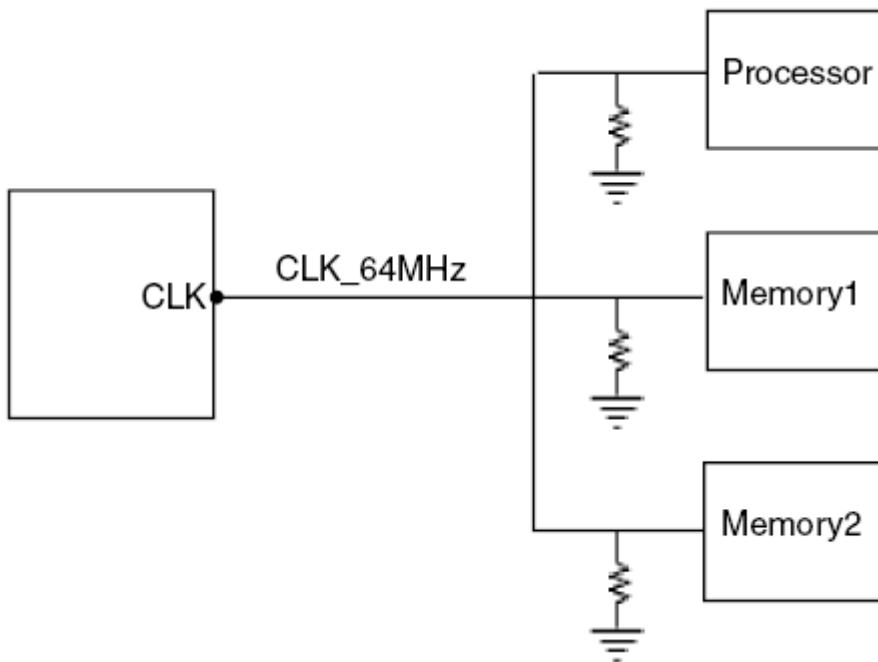


To create terminations for such a bus, you can:

- Select all bits between `data<63>` and `data<4>` in the Component Connectivity Details pane and apply terminations. To select all bits, first select the first bit (`data<63>`), and hold the Shift key and select the last bit (`data<4>`).
- Create a bus `data<63..4>` and then apply terminations at the bus level.

Termination Example 3

You may need to attach shunt terminations to a signal moving out from a clock and feeding different chips such as processors and memory.



To quickly apply such terminations, perform the following steps:

1. Click the `CLK_64MHz` signal to open the Signal Connectivity Details pane.
2. Select the rows corresponding to the cells (`Processor`, `Memory1` and `Memory2`).
3. Select *Add Termination* from the context sensitive menu.
4. Apply the appropriate shunt termination.

The selected shunt termination is added to all 3 blocks—`Processor`, `Memory1` and `Memory2`.

Bypass Capacitors

In high-speed environments, the instantaneous current generated with the rising and falling edges of the outputs causes the power plane to generate noise. Hence one of the key tasks in minimizing the variation of effective power plane and ground bounce, is to provide enough bypass capacitors near power pins to maintain power supply voltage. Bypass capacitors act as a local power storage for the device to which they are associated.

System Connectivity Manager lets you quickly add the bypass capacitors you want to associate with the power pins of a component.

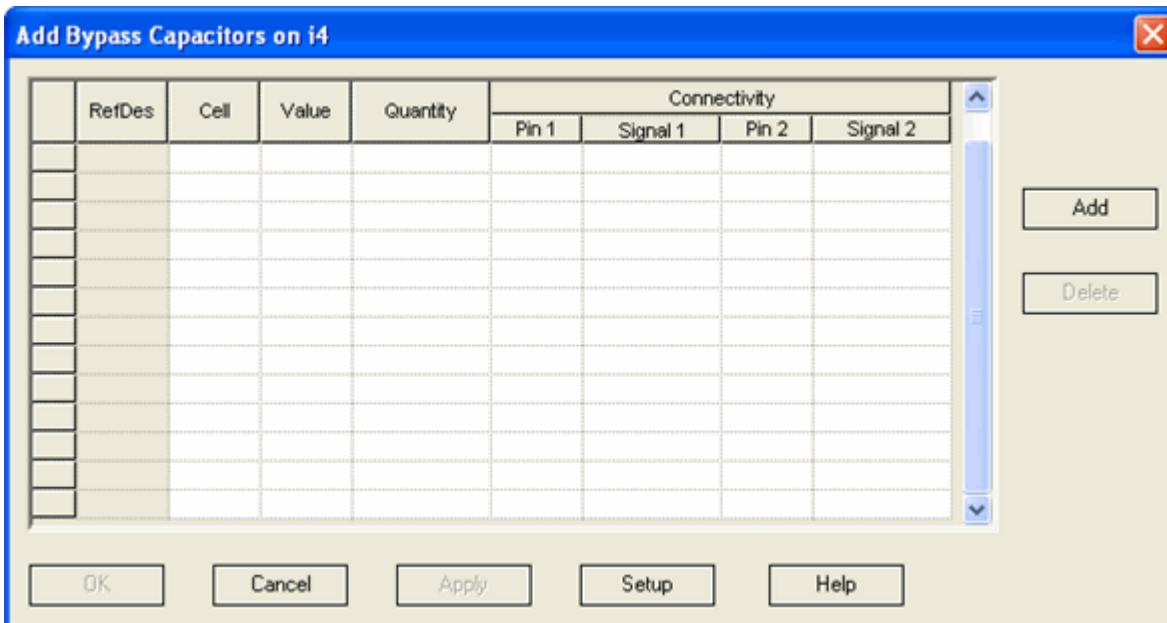
Adding Bypass Capacitors

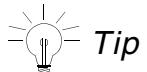
Before you add bypass capacitors, ensure that DC nets (nets with the VOLTAGE property) exist in your design.

To add a bypass capacitor to a component

1. Select the component in the Component List.
2. Right-click and choose *Add Bypass Capacitors*.

The Add Bypass Capacitors dialog box appears.





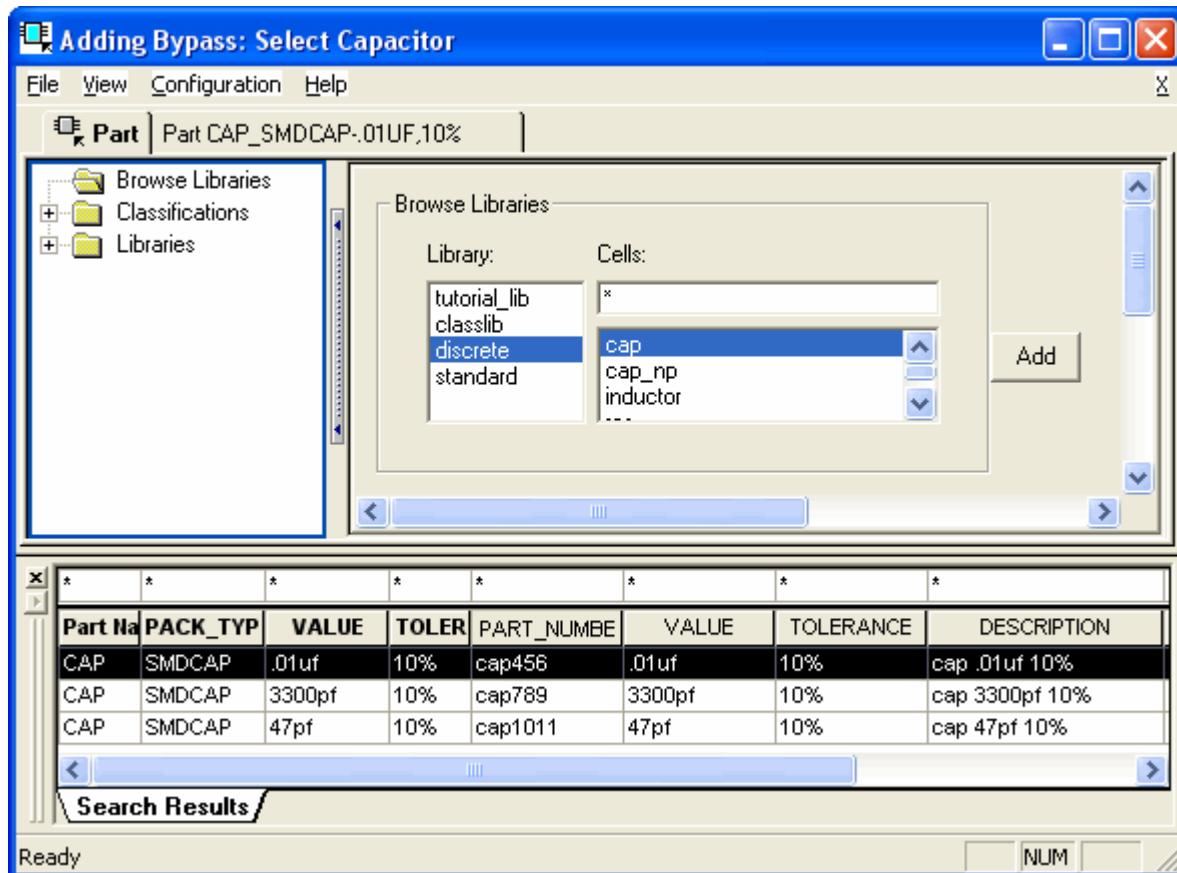
Tip

To specify the capacitor component that should be used by default when adding bypass capacitors, click the *Setup* button and select the capacitor component that you want to be used by default when adding bypass capacitors. For information on how to do this, see [Defining Default Discrete Components](#) on page 315.

3. Click the *Add* button.

The Adding Bypass: Select Capacitor dialog box appears.

4. In the *Cells* list, select the capacitor component you want to add.
5. In the *Search Results* pane, select the part table row that specifies the capacitance value you want to use.



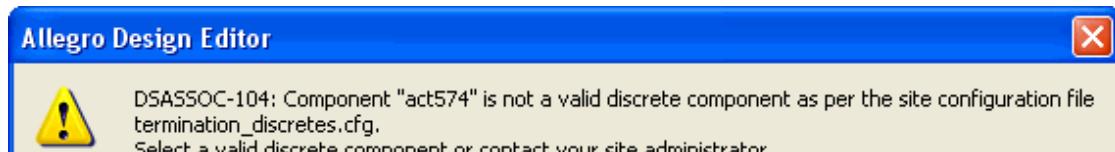
6. Click *Add*.

The capacitor is added in the Add Bypass Capacitor dialog box.

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Note: If you select a component that is not a valid capacitor component, the following error message appears:



Select another component that is a valid capacitor component. For more information on knowing whether a component is a valid capacitor component and defining valid capacitor components, see the following topics:

- [Requirements for Discrete Components](#) on page 319
- [Defining Valid Discrete Components](#) on page 317.

7. To add multiple instances of the bypass capacitor to the selected component, enter a new value in the *Quantity* field.

For example, to add four instances of the bypass capacitor to the component, enter 4 in the *Quantity* field.

8. Connect the pins of the capacitor to signals.

- a. Click the *Signal1* field and select a signal from the drop-down list.
- b. Click the *Signal2* field and select a signal from the drop-down list.

9. To apply the changes and package the added bypass capacitors, click *Apply*.

System Connectivity Manager automatically packages the bypass capacitors you added in the Add Bypass Capacitors dialog box and assigns reference designators to the bypass capacitors. If you modified the quantity in the *Quantity* field, as many rows appear as the number you entered in the *Quantity* field. For example, if you entered 4 in the *Quantity* field next to a bypass capacitor, four instances of the bypass capacitor are displayed (in four separate rows) in the Add Bypass Capacitors dialog box.

Note: Once a bypass capacitor is packaged, you cannot modify the quantity in the *Quantity* field. If you want to add more instances of a bypass capacitor that is packaged, copy and paste the bypass capacitor. For more information on copying and pasting bypass capacitors, see [Copying and Pasting Bypass Capacitors](#) on page 302.

10. You can add more bypass capacitors, if required, by performing steps 3 to 9.

11. Click *OK* to close the Add Bypass Capacitors dialog box.

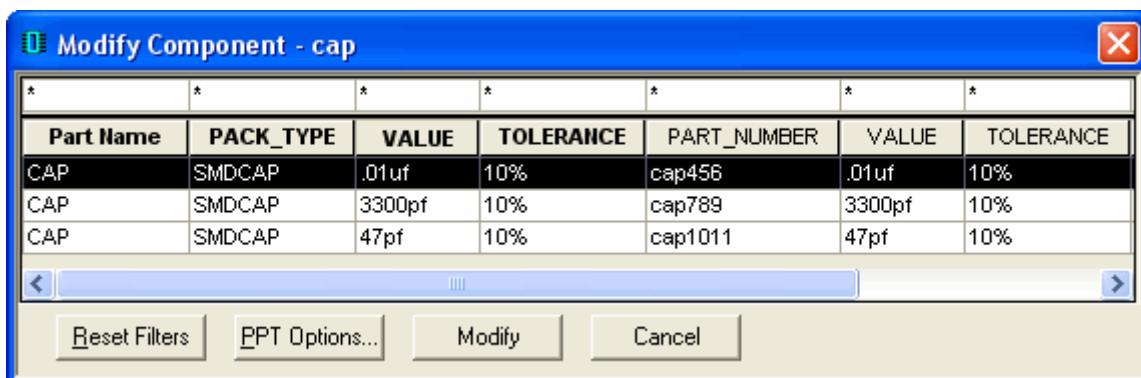
The  icon next to a component in the Component List indicates that bypass capacitors have been added on the component.

Modifying Bypass Capacitors

You can modify the connectivity and the capacitance value of bypass capacitors.

1. In the Component List, select the component on which the bypass capacitor is added.
 2. Right-click and choose *Edit Bypass Capacitors*.
- The Add Bypass Capacitors dialog box appears.
3. Modify the connectivity of the bypass capacitors as required.
 4. To modify the capacitance value of bypass capacitors, do the following:
 - a. Select the row for the bypass capacitor whose capacitance value you want to modify.
 - b. Click the *Modify* button.

The Modify Component dialog box appears.



- c. Select the part table row that specifies the capacitance value you want to use.
- d. Click the *Modify* button.

The new capacitance value is displayed in the Add Bypass Capacitors dialog box.

Viewing and Modifying Properties on Bypass Capacitors

1. In the Component List, select the component on which the bypass capacitor is added.
 2. Right-click and choose *Edit Bypass Capacitors*.
- The Add Bypass Capacitors dialog box appears.
3. Click  next to a bypass capacitor to display the Properties window.

Here you can add, modify or delete properties on the bypass capacitor. For more information on using the Properties window, see [Using System Connectivity Manager to Manage Properties](#) on page 253.

Copying and Pasting Bypass Capacitors

When you copy and paste a component, the bypass capacitors added on the component are also retained on the new instance of the component.

You can also copy specific bypass capacitors added on a component and paste them on the same component or on another component. This lets you quickly add bypass capacitors on components.

To copy and paste bypass capacitors

1. In the Component List, select the component on which the bypass capacitor is added.
2. Right-click and choose *Edit Bypass Capacitors*.

The Add Bypass Capacitors dialog box appears.

3. Select the row for the bypass capacitor you want to copy.

To select multiple rows, press the *Shift* or *Ctrl* key and click the rows you want to copy.

4. Click *Copy*.

To paste the bypass capacitors on the same component

- a. Click on an empty row in the Add Bypass Capacitors dialog box and click *Paste*.

Note: You cannot paste more than one instance of a row for a bypass capacitor you copied using the *Copy* button. For example, if you copy a row for a bypass capacitor, select more than one empty row in the Add Bypass Capacitors dialog box and click *Paste*, only one row is pasted.

- b. To add multiple instances of the pasted bypass capacitor to the selected component, enter a new value in the *Quantity* field.

For example, to add four instances of the pasted bypass capacitor to the component, enter *4* in the *Quantity* field.

- c. To apply the changes and package the pasted bypass capacitors, click *Apply*.

System Connectivity Manager automatically packages the bypass capacitors you pasted in the Add Bypass Capacitors dialog box and assigns reference designators

to the bypass capacitors. If you modified the quantity in the *Quantity* field, as many rows appear as the number you entered in the *Quantity* field. For example, if you entered 4 in the *Quantity* field next to a bypass capacitor, four instances of the bypass capacitor are displayed (in four separate rows) in the Add Bypass Capacitors dialog box.

Note: Once a bypass capacitor is packaged, you cannot modify the quantity in the *Quantity* field. If you want to add more instances of a bypass capacitor that is packaged, copy and paste the bypass capacitor.

- d. Click *OK*.

To paste the bypass capacitors on another component

- a. Click *OK* to close the Add Bypass Capacitors dialog box.
- b. In the Component List, select the component on which you want to paste the bypass capacitors.
- c. Right-click and choose *Add Bypass Capacitors*.

The Add Bypass Capacitors dialog box appears.

- a. Click on an empty row in the Add Bypass Capacitors dialog box and click *Paste*.

Note: You cannot paste more than one instance of a row for a bypass capacitor you copied using the *Copy* button. For example, if you copy a row for a bypass capacitor, select more than one empty row in the Add Bypass Capacitors dialog box and click *Paste*, only one row is pasted.

- b. To add multiple instances of the pasted bypass capacitor to the selected component, enter a new value in the *Quantity* field.

For example, to add four instances of the pasted bypass capacitor to the component, enter 4 in the *Quantity* field.

- c. Click *OK*.

Deleting Bypass Capacitors

1. In the Component List, select the component on which the bypass capacitor is added.
2. Right-click and choose *Edit Bypass Capacitors*.

The Add Bypass Capacitors dialog box appears.

3. Select the row for the bypass capacitor you want to delete.

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To select multiple rows, press the *Shift* or *Ctrl* key and click the rows you want to delete.

4. Click *Delete*.
5. Click *OK*.

Viewing Bypass Capacitors on Components

You can view the bypass capacitors on a component in the Add Bypass Capacitors dialog box or the Associated Component Viewer.

To view bypass capacitors using the Add Bypass Capacitors dialog box

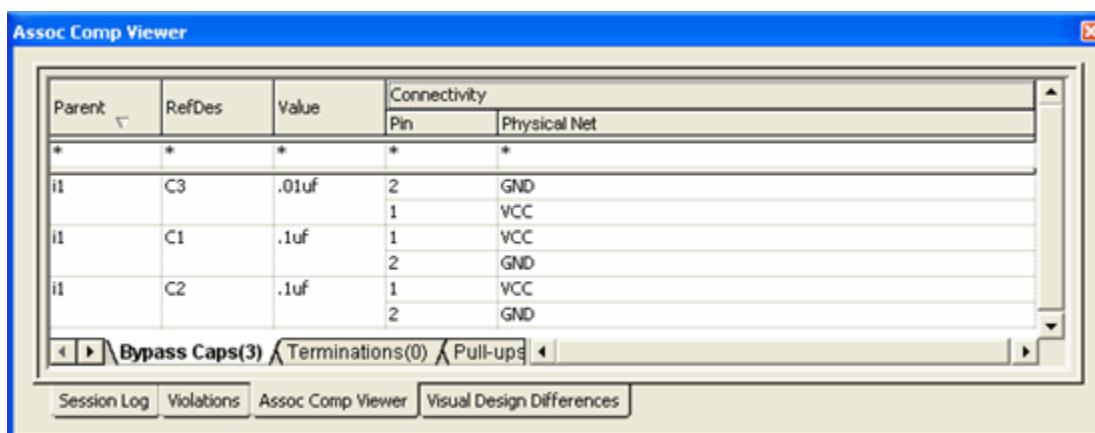
1. In the Component List, select the component on which the bypass capacitor is added.
2. Right-click and choose *Edit Bypass Capacitors*.

The Add Bypass Capacitors dialog box appears.

To view bypass capacitors using the Associated Component Viewer

1. In the Component List, select the component on which the bypass capacitor is added.
2. Choose *View – Associated Components*.

The bypass capacitors added on the component are displayed in the *Bypass Caps* tab of the Assoc Comp Viewer window.



Pullups and Pulldowns

Pullups and pulldowns are used to reduce noise in the circuit.

The following sections describe how you can work with pullups and pulldowns in your design.

- [Adding a Pullup or Pulldown](#) on page 305
- [Adding Pullup or Pulldown to Multiple Pins](#) on page 308
- [Viewing and Editing Pullup or Pulldown Information](#) on page 312

Adding a Pullup or Pulldown

Note: Before you add a pullup or pulldown, ensure that DC nets (nets with the VOLTAGE property) exist in your design.

Note: You can specify the resistor component that should be used by default when adding pullups or pulldowns. This helps you quickly select the resistor when you add pullups or pulldowns in your design. For information on how to do this, see [Defining Default Discrete Components](#) on page 315.

To add a pullup or pulldown

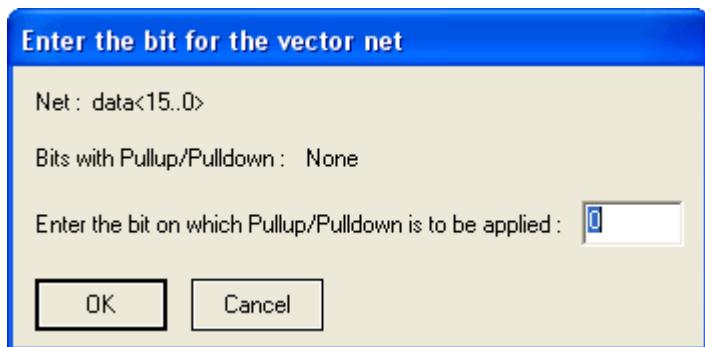
1. Click on any cell in the *Pullup/Pulldown* column (the column with the  symbol) in the *Component Connectivity Details* pane or select a signal in the *Signal List* pane
2. Choose *Object – Associate Components – Add Pullup/Pulldown*.

Alternatively, you can also double-click any cell in the *Pullup/Pulldown* column (the column with the  symbol) in the *Component Connectivity Details* pane. If the pin is not connected to any signal, System Connectivity Manager connects the pin to a new signal named `signal_n` (where `n` is a number). For example, if the pin is not connected to a signal, System Connectivity Manager connects the pin to a new signal named `signal_1`.

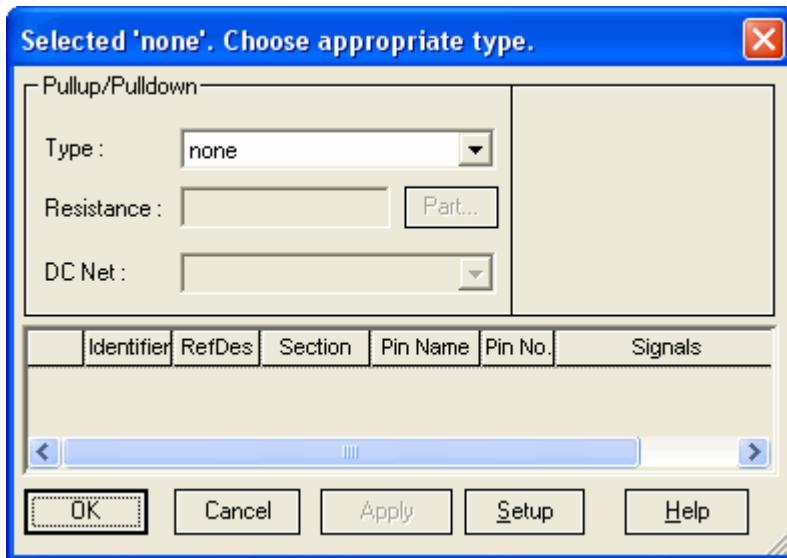
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3. (If the selected signal is a vectored signal) Enter the bit on which you want to add the pullup or pulldown in the *Enter the bit for the vector net* dialog box and click *OK*.



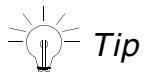
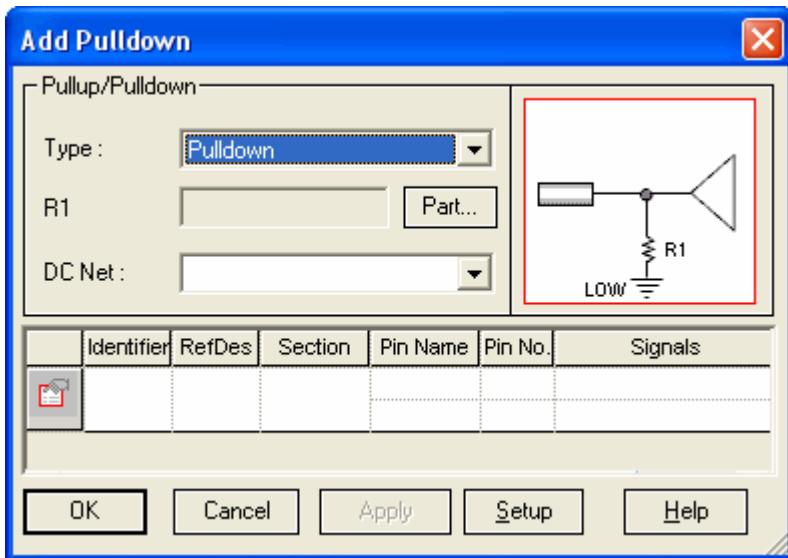
4. Choose *Pullup* or *Pulldown* from the *Type* drop-down list in the *Select 'none'. Choose appropriate type* dialog box.



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Based on your selection, the dialog box title and the image representing the circuit for the selection (pullup or pulldown) in the Add Pullup/Pulldown dialog box changes.



Tip
To specify the resistor component that should be used by default when adding pullups or pulldowns, click the *Setup* button and select the resistor component that you want to be used by default when adding pullups or pulldowns. For information on how to do this, see [Defining Default Discrete Components](#) on page 315.

5. Click the *Part* button to select the resistor component you want to use for the pullup or pulldown.

The Adding Termination: Select Resistor dialog box appears.

6. Select the resistor component and click *Add*.
7. Select the DC net you want to use for the pullup or pulldown from the *DC Net* drop-down list.

Note that the grid below is filled with the information regarding the resistor. You can enter a reference designator value for the resistor in the *RefDes* column or click the *Apply* button to let System Connectivity Manager automatically assign the reference designator value.

8. Click *OK*.

The pullup or pulldown is added and an icon representing the pullup or pulldown is displayed in the Pullup/Pulldown column. For more information, see [Pullup-Pulldown Icons](#) on page 311.

Adding Pullup or Pulldown to Multiple Pins

You can add pullups or pulldowns to multiple pins at the same time. This lets you quickly capture pullup or pulldown information in the design.

Note: Before you add a pullup or pulldown, ensure that DC (or power) nets exist in your design.

Note: You can specify the resistor component that should be used by default when adding pullups or pulldowns. This helps you quickly select the resistor when you add pullups or pulldowns in your design. For information on how to do this, see [Defining Default Discrete Components](#) on page 315.

To add a pullup or pulldown to multiple pins

1. Open the Component Connectivity Details pane.
2. Select the cell in the Pullup/Pulldown column (the column with the  symbol) next to each pin on which you want to add a pullup or pulldown.
3. Choose *Object – Associate Components – Add Pullup/Pulldown*.
 - If only one of the selected pins is not connected to any signal, System Connectivity Manager connects the pin to a new signal named `signal_n` (where `n` is a number). For example, System Connectivity Manager connects the unconnected pin to a new signal named `signal_1`.
 - If two or more selected pins are not connected to any signal, System Connectivity Manager displays the following message:



- Click **Yes** to wire the unconnected pins to the same signal. System Connectivity Manager connects the pins to a new signal named `signal_n` (where `n` is a

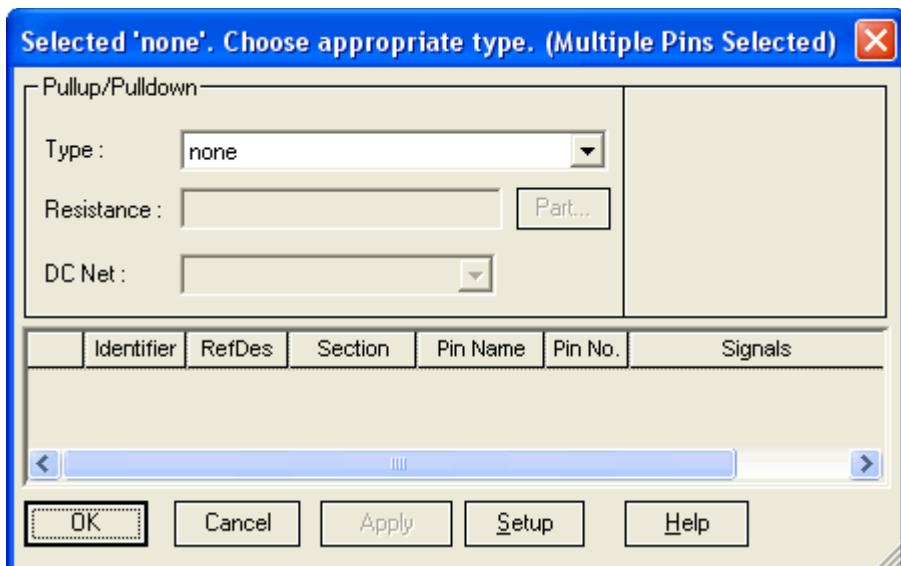
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number). For example, System Connectivity Manager connects the pins to a new signal named `signal_1`.

- Click *No* to wire the unconnected pins to different signals. System Connectivity Manager connects the pins to new signals named `signal_n` (where *n* is a number). For example, System Connectivity Manager if there are three unconnected pins, System Connectivity Manager connects the first pin to `signal_1`, the second pin to `signal_2` and the third pin to `signal_3`.
- Click *Cancel* to cancel the process of adding the pullup or pulldown.

The Add Pullup/Pulldown dialog box appears. The text (*Multiple Pins Selected*) in the dialog box title indicates that you have selected multiple pins for adding a pullup or pulldown.



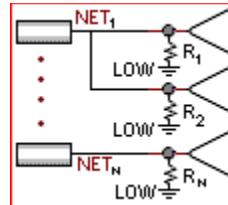
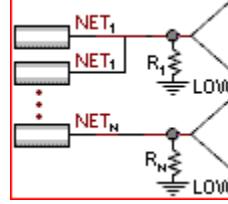
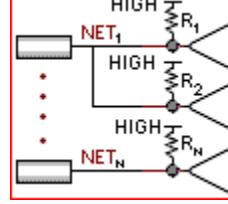
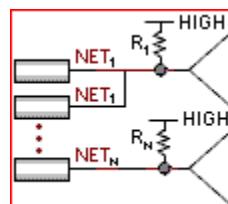
4. Click the *Type* drop-down list to choose the type of pullup or pulldown you want to add to the pins.

Based on your selection, the dialog box title and the image representing the circuit for the selection in the Add Pullup/Pulldown dialog box changes.

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Table 11-2 Choices for adding Pullup/Pulldown to multiple pins

Choose	To	Sample Circuit
Pulldown For Each Connection	<p>Add a separate pulldown for pins connected to the same signal.</p> <p>For example, if you are adding a pulldown on two pins connected to the same signal NET1, each connection is separately pulled down as shown in the sample circuit.</p>	
Pulldown For Each Unique Net	<p>Add a common pulldown for pins connected to the same signal.</p> <p>For example, if you are adding a pulldown on two pins connected to the same signal NET1, a common pulldown is added as shown in the sample circuit.</p>	
Pullup For Each Connection	<p>Add a separate pullup for pins connected to the same signal.</p> <p>For example, if you are adding a pullup on two pins connected to the same signal NET1, each connection is separately pulled up as shown in the sample circuit.</p>	
Pullup For Each Unique Net	<p>Add a common pullup for pins connected to the same signal.</p> <p>For example, if you are adding a pullup on two pins connected to the same signal NET1, a common pullup is added as shown in the sample circuit.</p>	

5. Click the *Part* button to select the resistor component you want to use for the pullup or pulldown.

The Adding Termination: Select Resistor dialog box appears.

6. Select the resistor component and click *Add*.

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7. Select the DC net you want to use for the pullup or pulldown from the *DC Net* drop-down list.

Note that the grid below is filled with the information regarding the resistor. You can enter a reference designator value for the resistor in the *RefDes* column, or click the *Apply* button to let System Connectivity Manager automatically assign the reference designator value.

8. Click *OK*.

The pullup or pulldown is added and an icon representing the pullup or pulldown is displayed in the Pullup/Pulldown column next to each selected pin. For more information, see [Pullup-Pulldown Icons](#) on page 311.

Pullup-Pulldown Icons

The following table describes the icons used for pullups and pulldowns in the Pullup/Pulldown column (the column with the following symbol: ) in the Component Connectivity Details and Signal Connectivity Details panes.

Icon	Description
None	The selected net does not have any pullup or pulldown associated with it.
Red triangle at top-right	There is one or more pullup attached directly to the net. The aliases, however, do not have any pullup or pulldowns.
Red triangle at bottom-left	There is one or more pulldown attached directly to the net. The aliases, however, do not have any pullup or pulldowns.
Gray triangle at top-right	One or more aliases of the selected net has one or more pullups attached to it. The selected net, however, does not have any pullup or pulldown directly attached to it.
Gray triangle at bottom-left	One or more aliases of the selected net has one or more pulldowns attached to it. The selected net, however, does not have any pullup or pulldown directly attached to it.
Two red triangles, at top-right and bottom-left	The selected net has one or more pullups and one or more pulldowns attached to it. The aliases of the selected net may also have pullups or pulldowns attached.
Two gray triangles, at top-right and bottom-left	The selected net does not have any pullup or pulldown attached to it. The aliases of the selected net has one or more pullups or pulldowns attached.

Icon	Description
Red triangle at top-right and gray triangle at bottom-left	The selected net has a pullup attached and the aliases of that net have one or more pulldowns attached.
Gray triangle at top-right and red triangle at bottom-left	The selected net has a pulldown attached and the aliases of that net have one or more pullups attached.

Viewing and Editing Pullup or Pulldown Information

You can have multiple pullups and pulldowns attached to a net. Using the Pullup/Pulldown Information on the net dialog box, you can quickly:

- View existing pullups and pulldowns on a net and the aliases of that net.
- Add pullups and pulldowns to the selected net.
- Modify existing pullups and pulldowns on a net.
- Delete existing pullups or pulldowns on a net.
- View and modify properties on the resistor component used for the pullup or pulldown.

To view or modify pullups or pulldowns

1. Click on any cell in the *Pullup/Pulldown* column (the column with the  symbol) in the *Component Connectivity Details* pane or select a signal in the *Signal List* pane
2. Choose *Object – Associate Components – Edit Pullup/Pulldown*.

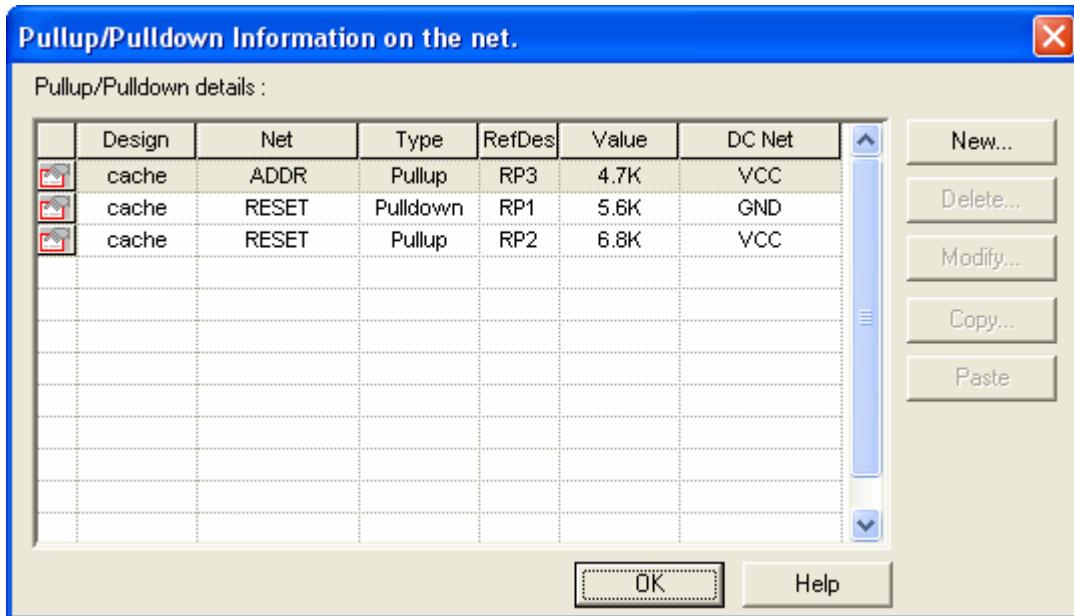
Alternatively, you can also double-click any cell in the *Pullup/Pulldown* column (the column with the  symbol) in the *Component Connectivity Details* pane.

The *Pullup/Pulldown Information on the net*. dialog box appears and displays the list of pullups and pulldowns on the selected net and the nets aliased to the selected net. The pullup or pulldown on aliased nets are displayed in gray color. For example the pullup

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on the net ADDR is displayed in gray color in the above figure because the net ADDR is aliased to the net RESET.



3. You can now edit the pullup or pulldown information.

- ❑ To add a new pullup or pulldown, click the *New* button.

For more information, see [Adding a Pullup or Pulldown](#) on page 305.

- ❑ To delete a pullup or pulldown, select the pullup or pulldown from the *Pullup/Pulldown details* list and click the *Delete* button.
- ❑ To edit the information for a pullup or pulldown, select the pullup or pulldown from the *Pullup/Pulldown details* list and click the *Modify* button.

The Edit Pullup/Pulldown dialog box appears displaying the information for the selected pullup or pulldown. You can now make the following changes:

- Change the type by selecting *Pullup* or *Pulldown* in the *Type* drop-down list.
- Change the associated resistor by clicking the *Part* button and selecting a new resistor in the Adding Termination: Select Resistor dialog box appears.
- Change the DC net for the pullup or pulldown by selecting a DC net from the *DC Net* drop-down list.
- Change the reference designator value for the resistor by clicking in the *RefDes* field and modifying the reference designator value.

- To view or modify the properties on the resistor component used for the pullup or pulldown, click  next to a bypass capacitor to display the Properties window.

Here you can view, add, modify or delete properties on the bypass capacitor. For more information on using the Properties window, see [Using System Connectivity Manager to Manage Properties](#) on page 253.

4. Click *OK*.

Copying and Pasting Pullups and Pulldowns

When you copy and paste a component, the pullups and pulldowns added on the signals connected to the pins of the component are also retained on the new instance of the component.

You can also copy specific pullups or pulldowns added on a signal and paste them on the same signal or on another signal. This lets you quickly add pullups and pulldowns on signals.

To copy pullups and pulldowns

1. Click the cell in the *Pullup/Pulldown* column (the column with the  symbol) in the *Component Connectivity Details* pane or select a signal in the *Signal List* pane
2. Choose *Object – Associate Components – Edit Pullup/Pulldown*.

Alternatively, you can also double-click any cell in the *Pullup/Pulldown* column (the column with the  symbol) in the *Component Connectivity Details* pane.

The *Pullup/Pulldown Information on the net* dialog box appears.

3. Select the row for the pullup or pulldown you want to copy.

To select multiple rows, press the *Shift* or *Ctrl* key and click the rows you want to copy.

4. Click *Copy*.

To paste pullups or pulldowns on the same signal

1. Click on an empty row in the *Pullup/Pulldown Information on the net* dialog box and click the *Paste* button.
2. Click *OK*.

To paste the pullups or pulldowns on another signal

Note: You can paste pullups or pulldowns on another signal only if that signal or a signal aliased to that signal already has a pullup or pulldown added to it.

1. Click *OK* to close the Pullup/Pulldown Information on the net dialog box.
2. Click the cell in the *Pullup/Pulldown* column (the column with the  symbol) in the *Component Connectivity Details* pane or select a signal in the *Signal List* pane
3. Choose *Object – Associate Components – Edit Pullup/Pulldown*.

Alternatively, you can also double-click any cell in the *Pullup/Pulldown* column (the column with the  symbol) in the *Component Connectivity Details* pane.

The *Pullup/Pulldown Information on the net* dialog box appears.

4. Click an empty row in the *Pullup/Pulldown Information on the net* dialog box dialog box and click the *Paste* button.
5. Click *OK*.

Setting Up Discrete Components

Defining Default Discrete Components

You can use the Discrete Component Setup dialog box to define the discrete components (resistors, capacitors, diodes and inductors) that appear as the default selection when you apply terminations, bypass capacitors, pullups or pulldowns in your design. This helps you quickly select the discrete components while applying terminations, bypass capacitors, pullups or pulldowns in your design.

For example, when you click the *Part* button in the Add Pullup/Pulldown dialog box to select the resistor to be used for a pullup, the resistor defined in the Discrete Component Setup dialog box is selected by default in Part Information Manager.

To define the default discrete components:

1. Choose *Project – Settings* and click the *Discrete Components* tab.

The Discrete Component Setup dialog box appears.

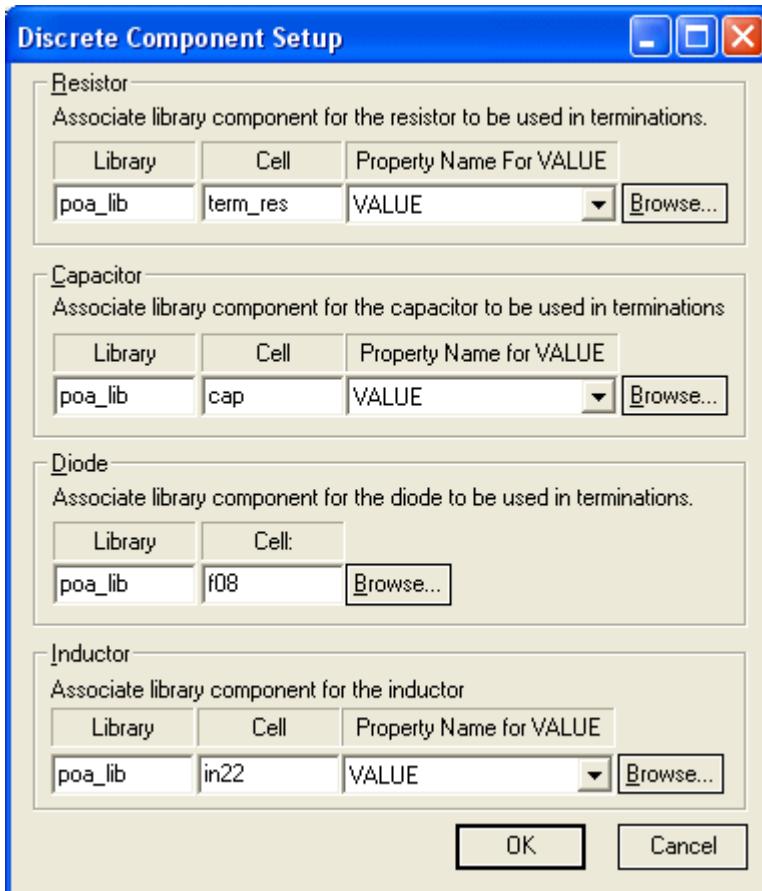
Note: The Discrete Component Setup dialog box also appears if you click the *Setup* button in the following dialog boxes:

- Add Termination dialog box

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Working with Associated Components

- Add Pullup/Pulldown dialog box
- Add Bypass Capacitor dialog box



2. Click *Browse* in the *Resistor* group box and select a resistor in Part Information Manager.
3. Select the property to use for displaying the value of the selected resistor. The default property is *VALUE*. You can choose another property for displaying the value of the resistor from the *Property Name for VALUE* drop-down list.
4. Click *Browse* in the *Capacitor* group box and select a capacitor in Part Information Manager.
5. Select the property to use for displaying the value of the selected capacitor. The default property is *VALUE*. You can choose another property for displaying the value of the capacitor from the *Property Name for VALUE* drop-down list.
6. Click *Browse* in the *Diode* group box and select a diode in Part Information Manager.

7. Click *Browse* in the *Inductor* group box and select an inductor in Part Information Manager.
8. Select the property to use for displaying the value of the selected inductor. The default property is *VALUE*. You can choose another property for displaying the value of the inductor from the *Property Name for VALUE* drop-down list.
9. Click *OK*.

Defining Valid Discrete Components

System Connectivity Manager uses a configuration file named `termination_discretes.cfg` file to ensure that only valid discrete components (resistors, capacitors, inductors and diodes) are used for adding terminations, bypass capacitors, and pullups or pulldowns in your design.

When you define the default discrete components (see [Defining Default Discrete Components](#) on page 315) for your project, or select a discrete component to be used for adding terminations, bypass capacitors, pullups or pulldowns in your design, System Connectivity Manager reads the `termination_discretes.cfg` file and displays the following message if the component is not valid:

```
<component_name> does not seem to be a valid component as per configuration  
(termination_discretes.cfg). Do you still want to add it?
```

For example, you have to select a resistor when you add a pullup in your design. Instead, if you select a capacitor or any other component, System Connectivity Manager displays the above message.

Location of `termination_discretes.cfg` File

The default `termination_discretes.cfg` file is located at:

```
<your_inst_dir>/share/cdssetup/tdd/
```

You can customize the `termination_discretes.cfg` file and place it in any of the default search locations specified in the `setup.loc` file located at `<your_inst_dir>/share/cdssetup/`. System Connectivity Manager searches for the file in the order specified in the `setup.loc` file. The search terminates when the first `termination_discretes.cfg` file is found. For example, if the file exists in your project directory and at `<your_inst_dir>/share/cdssetup/tdd`, System Connectivity Manager uses the file located in your project directory.

Syntax of `termination_discretes.cfg` File

```

(
  (
    ("RES"             ← Discrete component ID: RES for resistor,
      ("PHYS_DES_PREFIX" ("R" "RP")) )           CAP for Capacitor, DIODE for diode, IND for
                                                inductor and IO for connectors
    )
    ("CAP"
      ("PHYS_DES_PREFIX" ("C")) )               Property values
    )
    ("DIODE"
      ("PHYS_DES_PREFIX" ("CR")) )              Property name
    )
    )
    ("IND"
      ("PHYS_DES_PREFIX" ("L")) )              )
    )
    ("IO"
      ("PHYS_DES_PREFIX" ("X" "E" "A" "CU" "S" "VV" "B" "D" "W" "F" "TP")) )
    )
  )
)

```

System Connectivity Manager checks if the value of the `PHYS_DES_PREFIX` property on the selected discrete component matches the value specified in the `termination_discretes.cfg` file. If there is any mismatch, System Connectivity Manager displays an invalid component selection message. For example, if the `PHYS_DES_PREFIX` property on a selected resistor has any value other than `R` or `RP`, System Connectivity Manager displays the invalid component selection message.

Note: If you do not want a property specified in the `termination_discretes.cfg` file to be checked by System Connectivity Manager, specify the value of the property as `NULL` (represented by “ ”). For example, if you do not want the `CLASS` property to be checked, specify the property in the `termination_discretes.cfg` file as:

```
("CLASS" "")
```

You can edit the `termination_discretes.cfg` file to specify the properties that should be checked for declaring a discrete component as valid. For example, if you want to define resistors having the `PHYS_DES_PREFIX` property values `R` or `RP`, and having the `CLASS` property with the value `DISCRETE`, as valid resistors, modify the `termination_discretes.cfg` file as shown below:

```
(
```

```
(  
  ("RES"  
    ("PHYS_DES_PREFIX" ("R" "RP"))  
    ("CLASS" ("DISCRETE"))  
  )  
  ("CAP"  
    ("PHYS_DES_PREFIX" ("C"))  
  )  
  ("DIODE"  
    ("PHYS_DES_PREFIX" ("CR"))  
  )  
  ("IND"  
    ("PHYS_DES_PREFIX" ("L"))  
  )  
  ("IO"  
    ("PHYS_DES_PREFIX" ("X" "E" "A" "CU" "S" "VV" "B" "D" "W" "F" "TP"))  
  )  
)  
)
```

Requirements for Discrete Components

Before you use a discrete component in your design, ensure that it complies with the following requirements:

- The component must have the `VALUE` or `VAL` property, or the property defining the value that you specified in the Discrete Components tab of the Setup dialog box or the Discrete Component Setup dialog box.

The `VALUE` or `VAL` property, or the property defining the value that you specified must be defined in the physical part table (`.ptf`) file for the component.

Note: If the `VALUE` or `VAL` property or the property defining the value that you specified is defined as an injected property in the physical part table (`.ptf`) file, you must annotate the property on the component when you add the component. If you do not do this, a model will not be assigned to the component when you run the *Auto Assign Models* command to automatically assign models for discrete components.

For example, to annotate the `VALUE` or `VAL` property when you add the component, do the following:

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Working with Associated Components

- a. Select the component in Part Information Manager.
- b. In the *Search Results* pane, click the row corresponding to the physical part you want to add.

- c. Right-click and choose *Property Options*.

The Property Options dialog box appears.

- d. Click in the *Annotate* field next to the `VALUE` or `VAL` property and choose *Value* or *Both* in the drop-down list.
- e. Click *OK* to close the Property Options dialog box.
- f. Click *Add* to add the component.

For more information on using Part Information Manager, see *Component Browser User Guide*.

Note: If the `VALUE` or `VAL` property on the component has the value 0, System Connectivity Manager assigns the following value to the property on the component when you run the *Auto Assign Models* command to automatically assign models to discrete components in the design.

Resistor 0.001 Ohm

Capacitor 0.001 pF

Inductor 0.001 nH

- The components must have an associated physical part table (`.ptf`) file.
- The properties specified in the `termination_discretes.cfg` file must exist in the `chips.prt` file for the components.

For example, the `termination_discretes.cfg` file located at `<your_inst_dir>/share/cdssetup/tdd/` specifies the `PHYS_DES_PREFIX` property with the value `R` or `RP` for resistors. This indicates that valid resistor components must have the `PHYS_DES_PREFIX` property with the value `R` or `RP` in their respective `chips.prt` files.

Working with Signal Integrity Models

This chapter describes the following sections:

- [Overview](#) on page 322
- [Setting Up SI Model Libraries](#) on page 322
- [Assigning SI Models](#) on page 325
- [Setting Up Signal Models in Component Libraries](#) on page 330
- [Automatically Assigning Models for Discrete Devices and ICs](#) on page 332
- [Viewing the Names of Assigned Models](#) on page 335
- [Removing a Model Assignment](#) on page 336
- [Model Assignment Checks](#) on page 336

Overview

System Connectivity Manager lets you assign signal integrity (SI) models to components and pins in your design during the design capture phase. You can then use SigXplorer to perform topology exploration and analyze the nets in your design for signal integrity issues. This helps you correct signal integrity issues early in the design cycle.

You can manually assign existing signal models to components (such as IC devices) and pins. You can also automatically generate and assign signal models for all two-pin discrete components (resistors, capacitors, and inductors) in your design.

The different types of signal models you can assign include:

- IBISDevice (Input/Output Buffer Information Specification) models to ICs and connectors.
Note: You cannot assign IBISDevice models to discretes.
- Package models to connectors.
- ESpiceDevice models to discrete devices such as resistors, capacitors, inductors and diodes.
- IOCell models and programmable buffer models to component pins.

You can also launch the Model Integrity tool from System Connectivity Manager to create and edit models. Model Integrity is a high-speed design tool that enables you to easily manage the integrity of the model data required for high-speed circuit simulations. For more information on Model Integrity, see the *Model Integrity User Guide*.

Setting Up SI Model Libraries

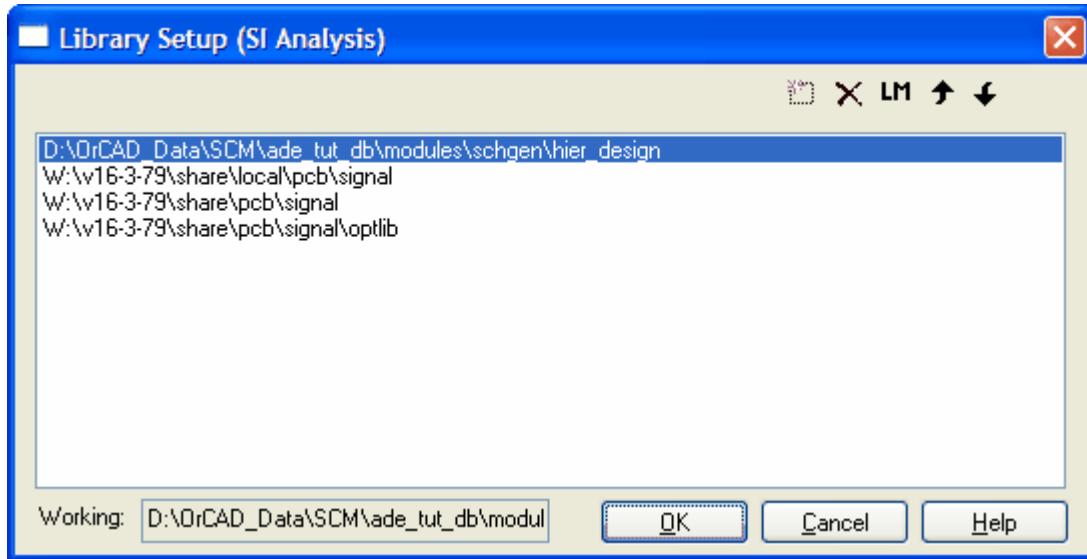
To setup SI model libraries for your project, do the following:

1. Do one of the following:
 - Choose *Project – Settings*.
The *Setup* dialog box appears. Click *Signal Integrity*.
 - Choose *Tools – Signal Integrity – SI Library Setup*.

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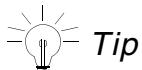
Working with Signal Integrity Models

The Library Setup (SI Analysis) dialog box appears.



You can use the Library Setup (SI Analysis) dialog box to do the following:

- Add an existing device model library to the library search list. For more information, see [Adding Model Library Directory](#) on page 324.
- Reorder libraries in the library search list. For more information, see [Changing the Library Search Order](#) on page 324.
- Specify the working device model library; the library to which the models you create will be added. For more information, see [Setting the Working Library](#) on page 324.
- Launch the Model Integrity tool to create and edit models. For more information, see [Editing Libraries](#) on page 325.
- Remove libraries from the library search list. For more information, see [Removing Libraries](#) on page 325.



Tip
You can also use the SIGNAL_DEVLIBS environment variable to specify the SI model libraries for your project. For example, if you set the SIGNAL_DEVLIBS environment variable as shown below, the new.dml and std.dml model libraries will be automatically listed in the Library Setup (SI Analysis) dialog box.

```
set SIGNAL_DEVLIBS c:\simodels\new.dml c:\simodels\std.dml
```

Adding Model Library Directory

1. Click .

The *Local Directory* dialog box appears.

2. Navigate to the directory that contains signal integrity device model library (.DML) or device model library index (.NDX) files.
3. Click OK. The path to the library directory is added in the list box.

Note: Ensure that there are no spaces in the name of the .DML or .NDX files

Changing the Library Search Order

The order in which the libraries are listed in the Library Setup dialog box determines their search order. Libraries are searched starting at the top of the list. If a model is included in two or more libraries, you can change the search order to determine which library SigXplorer searches first. SigXplorer uses the first model found in the search order.

- To move a library (.DML) or index (.NDX) file one level up, select the file and click .
- To move a library (.DML) or index (.NDX) file one level down, select the library or index file and click .

Setting the Working Library

A working library is the library to which the models you create or the default models generated by System Connectivity Manager for two-pin discrete devices will be added.

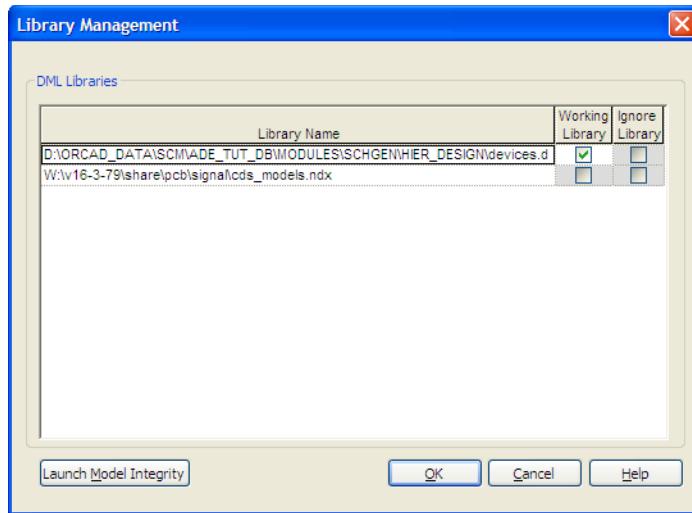
Note: When you create a project, System Connectivity Manager creates a default device model library named `devices.dml` in the project directory and sets it as the working library. You can change it using the Library Manager dialog box.

To set the working library:

1. Click  to launch the Library Manager.

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Working with Signal Integrity Models



2. Check the Working Library check box next to the library to set as the working library.
3. Click OK to save the settings and close the Library Management dialog box.

Editing Libraries

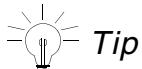
You can launch the Model Integrity tool from the *Library Management* dialog box to create and edit models in a library. To edit a library, select the library (.DML) file and click *Launch Model Integrity*. The library is opened for editing in the Model Integrity tool.

Removing Libraries

- In the Library Management dialog box, select a device model library (.DML) or index (.NDX) file and check the *Ignore Library* box.
- To remove the library directory, in the Library Setup (SI Analysis) dialog box, click .

Assigning SI Models

System Connectivity Manager lets you assign signal integrity (SI) models to components and pins in your design.



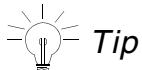
You can also specify the model setup for components in component libraries. When System Connectivity Manager finds that a component instance does not have a SI model assigned to it, it checks to see if the component has a SIGNAL_MODEL property on its device definition. For more information, [Setting Up Signal Models in Component Libraries](#) on page 330.

Note: Before assigning SI models to components and pins, you must setup the SI model libraries as described in [Setting Up SI Model Libraries](#) on page 322.

To assign SI models to components

1. Select a component in the *Component List* (in the logical view) or in the *Physical Part List* (in the physical view) and choose *Object – SI Models – Assign Model*.

The *SI Model Assignment* dialog box appears.

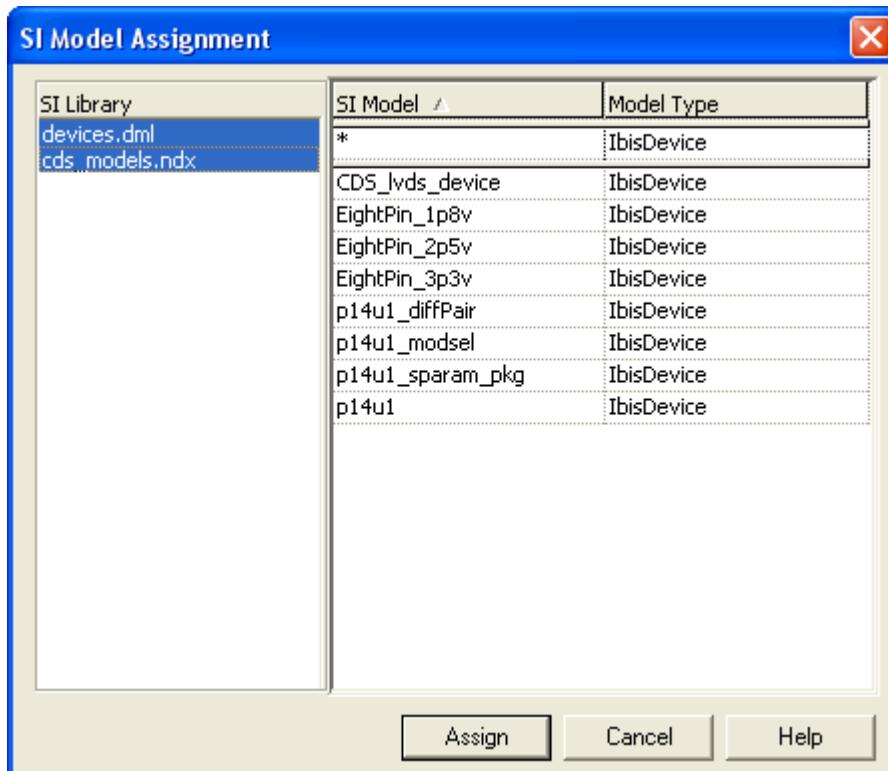


To assign the same model to more than one component, select the required components and then choose *Object – SI Models – Assign Model*.

System Connectivity Manager User Guide

Working with Signal Integrity Models

For more information on logical and physical views in System Connectivity Manager, see [Chapter 9, “Using the Physical View.”](#)



- To display only the models in a specific library, select the library in the *SI Library* list. If you select more than one library in the *SI Library* list, all the models in the selected libraries are displayed.
- To display only the models of a specific type, choose the model type in the *Model Type* drop-down list and press *Enter*.

You can select * in the *Model Type* drop-down list, enter a search string using the wildcard characters * and ?, and then press *Enter* to display only the models that belong to that model type.

- To search for models by name, select * in the *SI Model* drop-down list, enter a search string using the wildcard characters * and ?, and then press *Enter* to display only the models that meet the search criteria.

2. Select the model you want to assign and click *OK*.

System Connectivity Manager adds the SIGNAL_MODEL property on the component.

Note: You cannot add, modify or delete the SIGNAL_MODEL property on a component using the Properties window in System Connectivity Manager or using the Component

General Properties workbook in Constraint Manager.

- ❑ To add the SIGNAL_MODEL property on a component, you must assign a model to the component using the SI Model Assignment dialog box, as described above.
- ❑ To modify the SIGNAL_MODEL property on a component, you must assign a different model to the component using the SI Model Assignment dialog box, as described above.
- ❑ To delete the SIGNAL_MODEL property on a component, you must remove the model assignment as described in [Removing a Model Assignment](#) on page 336.

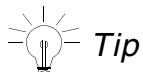
For more information on working with properties using the Properties window and Constraint Manager, see [Chapter 10, “Working with Properties and Electrical Constraints.”](#)

To assign models to pins

1. Do one of the following:

- ❑ Select a pin in the *Component Connectivity Details* pane (in the logical view), *Signal Connectivity Details* pane (in the logical view) or in the *Physical Part Connectivity Details* pane (in the physical view) and choose *Object – SI Models – Assign Model*.
- ❑ Double-click in the *Pin SI Model* cell next to a pin in the *Physical Part Connectivity Details* pane (in the physical view).

The *SI Model Assignment* dialog box appears.

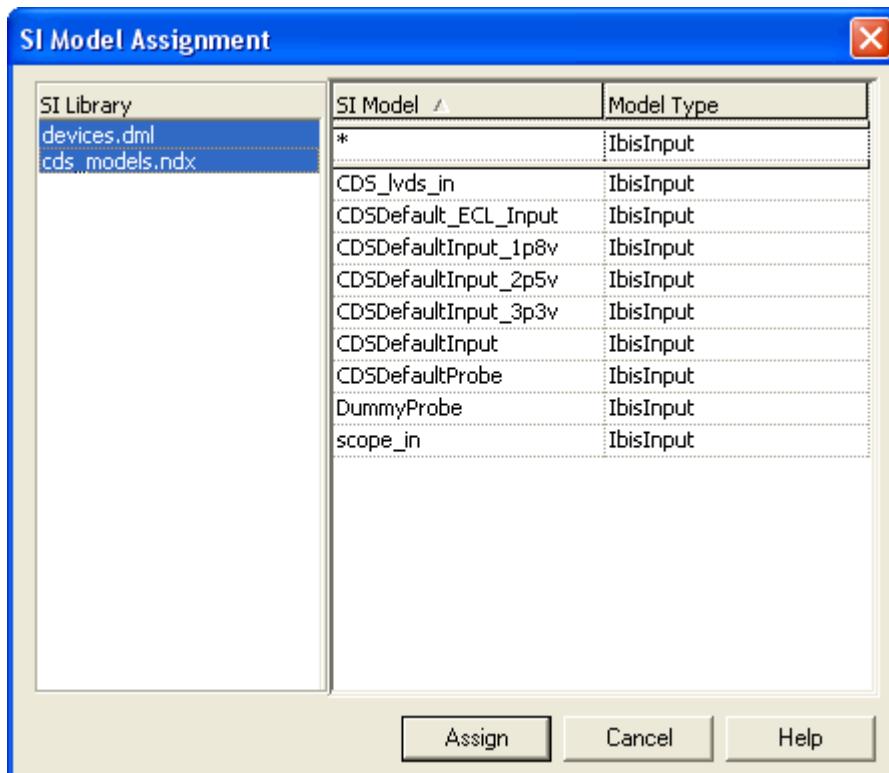


To assign the same model to more than one pin, select the required pins and then choose *Object – SI Models – Assign Model*. Ensure that the selected pins have the same pin type.

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Working with Signal Integrity Models

For more information on the logical and physical views in System Connectivity Manager, see [Chapter 9, “Using the Physical View.”](#)



- To display only the models in a specific library, select the library in the *SI Library* list. If you select more than one library in the *SI Library* list, all the models in the selected libraries are displayed.
- To display only the models of a specific type, choose the model type in the *Model Type* drop-down list and press *Enter*.

You can select * in the *Model Type* drop-down list, enter a search string using the wildcard characters * and ?, and then press *Enter* to display only the models that belong to that model type.

- To search for models by name, select * in the *SI Model* drop-down list, enter a search string using the wildcard characters * and ?, and then press *Enter* to display only the models that meet the search criteria.
2. Select the model you want to assign and click *OK*.

System Connectivity Manager adds the PIN_SIGNAL_MODEL property on the pin.

Note: You cannot add, modify or delete the PIN_SIGNAL_MODEL property on a pin using the Properties window in System Connectivity Manager or using the Component

General Properties workbook in Constraint Manager.

- ❑ To add the PIN_SIGNAL_MODEL property on a pin, you must assign a model to the pin using the SI Model Assignment dialog box, as described above.
- ❑ To modify the PIN_SIGNAL_MODEL property on a pin, you must assign a different model to the pin using the SI Model Assignment dialog box, as described above.
- ❑ To delete the PIN_SIGNAL_MODEL property on a pin, you must remove the model assignment as described in [Removing a Model Assignment](#) on page 336.

For more information on working with properties using the Properties window and Constraint Manager, see [Chapter 10, “Working with Properties and Electrical Constraints.”](#)

Setting Up Signal Models in Component Libraries

If you do not want to manually or automatically assign signal models to a component in System Connectivity Manager, you can specify the signal model for the component by using the following properties in the device definition.

Property	Description
SIGNAL_MODEL	<p>Add the SIGNAL_MODEL property in one of the following files to specify the signal model for a component:</p> <ul style="list-style-type: none">■ <code>chips.prt</code> file for the component■ Physical part table (<code>.ptf</code>) file for the component <p>The value of the SIGNAL_MODEL property must be the name of an IBISDevice or ESpiceDevice model.</p> <p>Note: The model you assign on a component in System Connectivity Manager (using the procedure described in Assigning SI Models on page 325) overrides the models, if any, in the device definition (<code>chips.prt</code> file, <code>.ptf</code> file, <code>phys_prt.dat</code> file, or PCB Editor device file).</p>

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Working with Signal Integrity Models

Property	Description
DEFAULT_SIGNAL_MODEL	<p>The DEFAULT_SIGNAL_MODEL property is used to specify a model name for the device before the actual model is developed.</p> <p>Add this property in one of the following files:</p> <ul style="list-style-type: none">■ chips.prt file for the component■ Physical part table (.ptf) file for the component <p>Note: System Connectivity Manager reports an error when a component with a SIGNAL_MODEL property does not have an associated model. However, with the DEFAULT_MODEL_NAME property attached to a component, System Connectivity Manager does not report an error when a model is not yet available.</p>
VOLT_TEMP_MODEL	<p>The VOLT_TEMP_MODEL property, attached to a pin, specifies the name of the voltage temperature model for the pin.</p> <p>Add this property in one of the following files:</p> <ul style="list-style-type: none">■ chips.prt file for the component■ Physical part table (.ptf) file for the component
DEFAULT_MODEL_NAME	<p>You can use the DEFAULT_MODEL_NAME property as a placeholder for a to-be-procured library of models or for implementing model names based on your internal model naming conventions.</p> <p>Add this property in one of the following files:</p> <ul style="list-style-type: none">■ chips.prt file for the component■ Physical part table (.ptf) file for the component

System Connectivity Manager uses the following precedence to determine which model gets assigned to a device:

1. An instance-specific SIGNAL_MODEL assignment made using the SI Model Assignment dialog box (using the procedure described in [Assigning SI Models](#) on page 325).
2. A SIGNAL_MODEL property on the device definition (component's physical part table file or chips.prt file).

3. A VOLT_TEMP_MODEL property on the device definition (component's physical part table file or `chips.prt` file).
4. A DEFAULT_SIGNAL_MODEL property on the device definition (component's physical part table file or `chips.prt` file).

If the same property exists in the `chips.prt` file and in the part table file (`.ptf`), the property in the `.ptf` file wins.

Automatically Assigning Models for Discrete Devices and ICs

System Connectivity Manager lets you automatically generate and assign ESpiceDevice models for all two-pin discrete devices (resistors, capacitors, and inductors) in your design.

System Connectivity Manager also lets you automatically assign IBISDevice models to ICs in your design if the SI model libraries you have setup for your project contain an IBISDevice model that has the same name as the value of the PART_NAME property for an IC. For example, the 74ls00 component has the part name `74LS00`. If you have an IBISDevice model named `74LS00` in the SI model libraries setup for your project, the model will be automatically assigned to the 74ls00 component when you add the component in the design.



While working on your design, if you modify the model library and make the default model for an instance available in the design, the model is not automatically assigned to the existing instances in the design. Default model assignment happens only for the new instances in the design.

For more information on setting up SI model libraries for your project, see [Setting Up SI Model Libraries](#) on page 322.

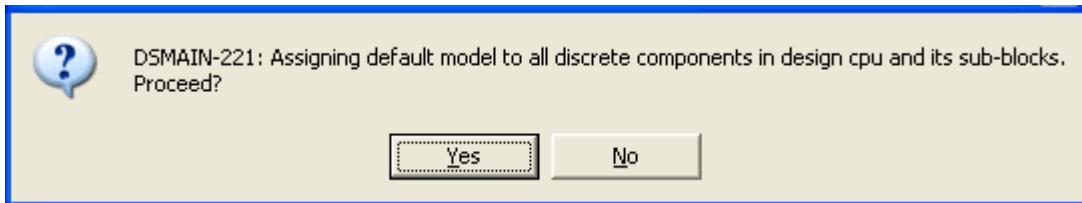
To automatically assign models to ICs, and generate and assign models for discrete devices

1. Setup the SI model libraries for the ICs used in your design as described in [Setting Up SI Model Libraries](#) on page 322.
2. Set the device library in which you want the models generated by System Connectivity Manager for the discrete devices, as the working library. For more information on setting a library as the working library, see [Setting the Working Library](#) on page 324.
3. Choose *Tools – Signal Integrity – Auto Assign Discrete Models*.

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Working with Signal Integrity Models

If you are working on a design named `cpu`, the following message appears:



4. Click Yes.

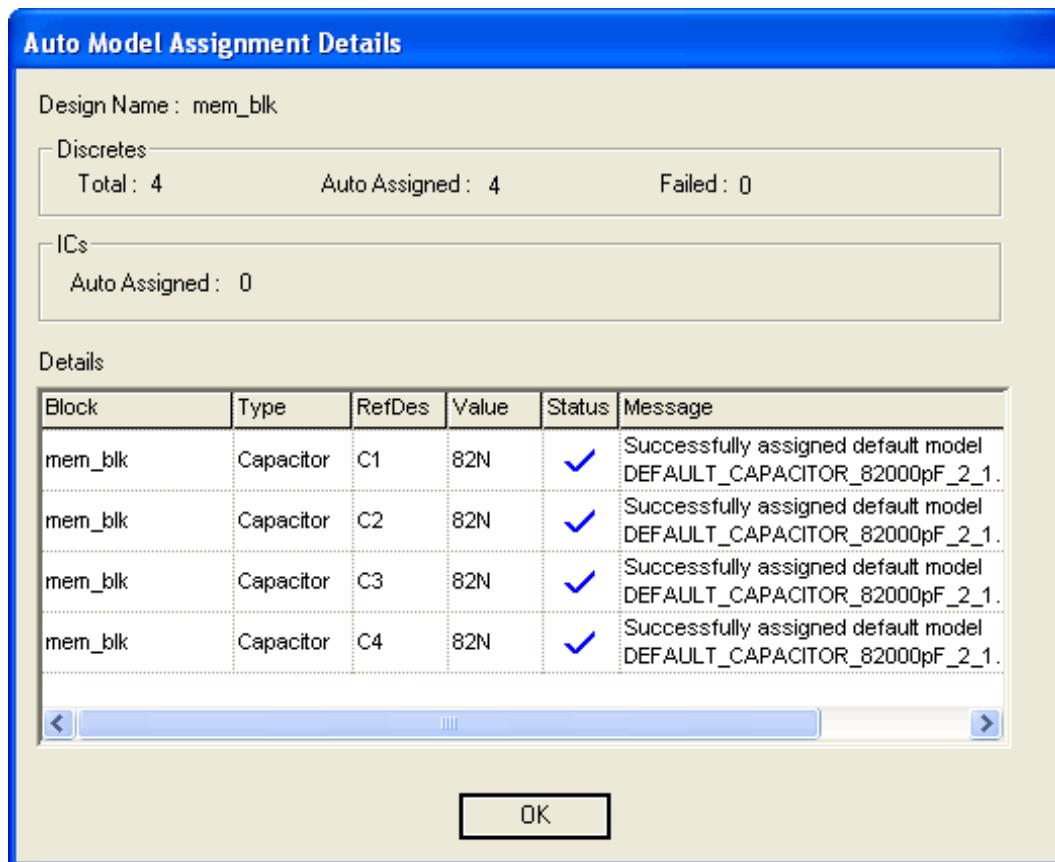
System Connectivity Manager does the following:

- ❑ Automatically assigns default models to all the discrete devices in the design and its sub-blocks for which no models have been previously assigned manually (using the procedure described in [Assigning SI Models](#) on page 325) or automatically. If a default model was already assigned to a discrete device, System Connectivity Manager checks for the existence of the default model in the model libraries. If the default model is not found in the SI model libraries setup for use with System Connectivity Manager (see [Setting Up SI Model Libraries](#) on page 322), System Connectivity Manager regenerates the default model for the device.
- ❑ Automatically assigns IBISDevice models to ICs in your design if the SI model libraries you have setup for your project contain an IBISDevice model that has the same name as the value of the `PART_NAME` property for an IC.

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The Auto Model Assignment Details dialog box appears.



The Auto Model Assignment Details dialog box displays the following information:

- Number of discrete devices found in the design
- Number of discrete devices on which System Connectivity Manager has automatically assigned models
- Number of discrete devices on which System Connectivity Manager could not automatically assign models.
- Number of ICs on which System Connectivity Manager has automatically assigned models.
- Status* column in the *Auto Model Assignment Summary* dialog box displays whether a model was assigned to a discrete device or not.

You can also open the `autoassign.log` file in the project directory to see the model assignment details.

Viewing the Names of Assigned Models

To view the names of models assigned to components in the logical view

- Select a component in the Component List and choose *View – Properties* to display the Properties window.

The value of the SIGNAL_MODEL property displayed in the Properties window is the name of the model assigned to the component.

To view the names of models assigned to pins in the logical view

1. Select a component in the Component List to display its pins in the Component Connectivity Details pane.
2. Select a pin in the Component Connectivity Details pane and choose *View – Properties* to display the Properties window.
3. The value of the PIN_SIGNAL_MODEL property displayed in the Properties window is the name of the model assigned to the pin.

To view the names of models assigned to components in the physical view

The *SI Model* column in the Physical Part List displays the models assigned to components in the design.

To view the names of models assigned to pins in the physical view

- Click on a component in the Physical Part List to display its pins in the Physical Part Connectivity Details pane.

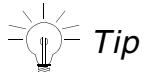
The *SI Model* column in the Physical Part Connectivity Details pane displays the models assigned to the component's pins.

For more information on the logical and physical views in System Connectivity Manager, see [Chapter 9, “Using the Physical View.”](#)

Removing a Model Assignment

To remove the model assigned to a component

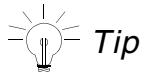
- Select the component in the *Component List* (in the logical view) or in the *Physical Part List* (in the physical view), and choose *Object – SI Models – Remove Model*.



To remove models assigned to more than one component, select the required components and then choose *Object – SI Models – Remove Model*.

To remove the model assigned to a pin

- Select the pin in the *Component Connectivity Details* pane (in the logical view) or in the *Physical Part Connectivity Details* pane (in the physical view), and choose *Object – SI Models – Remove Model*.



To remove models assigned to more than one pin, select the required pins and then choose *Object – SI Models – Remove Model*.

For more information on logical and physical views in System Connectivity Manager, see [Chapter 9, “Using the Physical View.”](#)

Model Assignment Checks

System Connectivity Manager performs the following checks for model assignments:

- If the model assigned to a component is not found in the model libraries setup for the project, errors are displayed in the Violations window.

This check is performed when you:

- Open the design in System Connectivity Manager.
- Add a component that has a signal model assigned to it using the SIGNAL_MODEL property.
- Assign a model to a component.

For more information on assigning models, see [Assigning SI Models on page 325](#).

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- ❑ Remove the library that contains a model assigned to a component from the list of model libraries setup for use with System Connectivity Manager.

For information on setting up model libraries for the project, see [Setting Up SI Model Libraries](#) on page 322.

- If there is a mismatch between the pin numbers or pin types of a component and the pin numbers or pin types of the model assigned to the component, errors are displayed in the Violations window. This check is performed when you assign a model to a component.

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Working with Signal Integrity Models

Working with Hierarchical Designs

This chapter contains the following sections that describe the procedures for working with blocks to create hierarchical designs in System Connectivity Manager.

- [Overview](#) on page 340
- [Creating Blocks](#) on page 341
- [Creating Sub-Projects for Blocks](#) on page 345
- [Adding Blocks from a Library](#) on page 345
- [Importing Blocks from Another Project](#) on page 346
- [Adding or Importing Design Entry HDL Blocks in System Connectivity Manager](#) on page 348
- [Adding or Importing Verilog files as Spreadsheet Blocks](#) on page 351
- [Creating a Hierarchical Design](#) on page 355
- [Editing a Hierarchical Design](#) on page 358
- [Working with Blocks](#) on page 361
- [Working with Ports of a Block](#) on page 371
- [Navigating a Hierarchical Design](#) on page 373
- [Setting the Root Design](#) on page 374
- [About Global Signals in Hierarchical Designs](#) on page 376
- [Working with Read-Only Blocks in your Design](#) on page 382

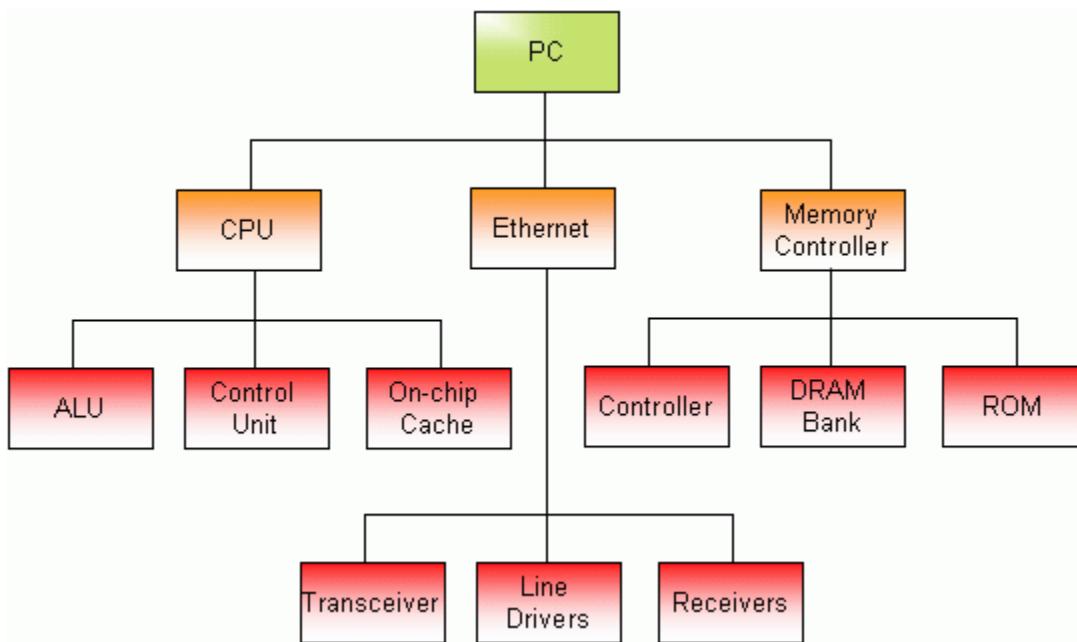
Overview

Blocks provide a mechanism for creating and storing functional blocks of circuitry. You can use a hierarchical design structure to divide a design into blocks or sub designs, where each block represents a logical function. Each of the blocks can further be divided into sub blocks.

In the hierarchical design example shown below, you have a hierarchical design called PC that contains the blocks CPU, Ethernet, and Memory Controller. The block CPU is further divided into three sub-blocks named ALU, Control Unit and On-chip Cache.

The top-level design in a hierarchical design is also called the root design. In the hierarchical design example shown below, the top-level design PC is the root design.

Figure 13-1 Hierarchical Design Example



The hierarchical design method is typically followed for large and complex designs.

System Connectivity Manager lets you easily create hierarchical designs using top-down and bottom-up design methodologies. You can have a combination of spreadsheet, Verilog and schematic blocks in your hierarchical design. For more information on the methodologies for creating hierarchical designs, see [Creating a Hierarchical Design](#) on page 355.

- For information on working on hierarchical designs in a team design environment, see [Chapter 15, “Team Design.”](#)

- For information on creating and using reusable blocks in your design, see [Chapter 17, “Design Reuse.”](#)

Creating Blocks

You can create blocks in the following two ways:

- Create a stand alone block and add it in a library. You can then add the block in your design. For this, choose *Project – Create Block*.
- Create a block and add it in your design. The block will be integrated as a sub-circuit in the hierarchical design. To create and instantiate the block, choose *Design – Create Block*.

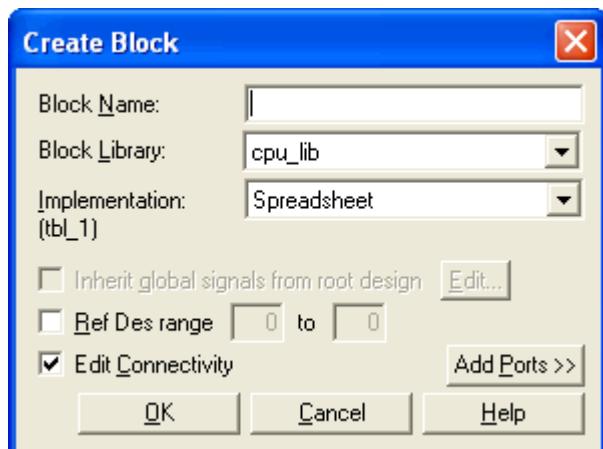
Creating a Standalone Block in a Library

This method of creating blocks is useful when you are creating a hierarchical design using bottom-up design methodology. The block is saved in a library and can later be instantiated in the design.

To create a stand alone block in a library

1. Choose *Project – Create Block*.

The Create Block dialog box appears.



2. Enter the name of the block in the *Block Name* field.

Note: Use only letters (a to z), numbers (0 to 9) and the underscore character (_) in

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block names. Do not use any other special character in block names.

3. Select the library in which you want to create the block in the *Block Library* field.
4. Select the implementation type of the block. You can create a block of type Spreadsheet, Verilog or Schematic.

The default implementation is Spreadsheet type.

5. Select the *Ref Des range* check box if you want to specify the range of reference designators to be used for components in the block.

For example, if you specify the reference designator range 1 to 100 for a block named ROM, the reference designators of components in the ROM block will start from, say, U1 and go up to U100. You cannot have a component with the reference designator U105 in the ROM block.

6. Click *Add Ports* to display the port list where you can define the ports or interface signals for the block.

- a. Enter the port name in the *Port Name* column.

Note: You can also paste the port names from other applications such as Microsoft Excel.

- b. Select the port type for each port as `IN`, `OUT`, or `INOUT` in the *Port Type* column.

Note: To specify the same port type for more than one port, select the port type field next to the ports and then select the port type from the drop-down list.

Note: While defining ports, you can right-click to use commands from the context sensitive menu. These commands help you add and delete ports, modify the port type and cut, copy or paste port information.

7. Select the *Edit Connectivity* check box if you want to add connectivity information for the block.

8. Click *OK* to create the block.

If you selected the *Edit Connectivity* check box, the new block is opened in:

- Spreadsheet Editor if you are creating a block of type Spreadsheet. The ports for the block are displayed in the Signal List.
- Verilog Design Editor if you are creating a block of type Verilog. The ports for the block are displayed in the Signal List.
- Allegro Design Entry HDL if you are creating a block of type Schematic.

You can now add connectivity information for the block.

The new block you created exists in a library and is still not part of your design. You can add it in your design using Part Information Manager.

Note: If you have created a block of type Schematic, you need to exit System Connectivity Manager and reopen the project in which you want to add the schematic block.

Creating a Block and Adding it in the Current Design

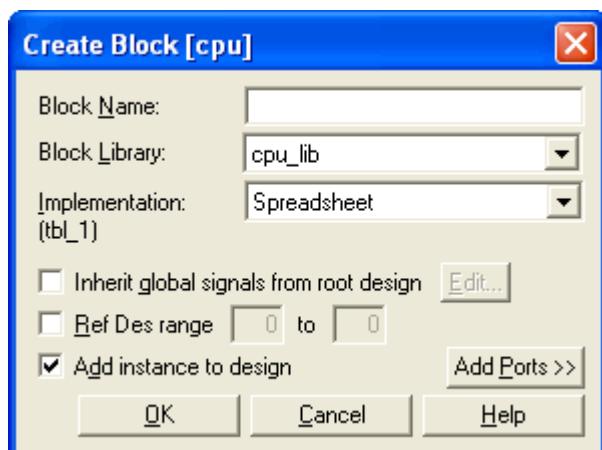
This approach is useful when you are creating a hierarchical design using top-down design methodology. The block is created and instantiated in the current design in a flow.

To create a block and add it in the current design

1. Do one of the following:

- Choose *Design – Create Block*.
- Click  on the toolbar.

The *Create Block [<design name>]* dialog box appears, where *<design name>* is the name of the design under which the block will be added. For example, if you create a block named *alu* when you are editing a block named *cpu*, the *alu* block will be added in the *cpu* block. For more information on editing blocks, see [Editing a Hierarchical Design](#) on page 358.



2. Enter the name of the block in the *Block Name* field.
3. Select the library in which you want to create the block in the *Block Library* field.

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4. Select the implementation type of the block. You can create a block of type Spreadsheet, Verilog or Schematic.

The default implementation is Spreadsheet type.

5. Select the *Inherit global signals from root design* check box if you want all the global signals in the top-level or root design and the parent blocks to be automatically added in the new block.

- a. Click *Edit* if you want to select the list of global signals that have to be inherited in the new block.

The Global Signals dialog box appears displaying the list of global signals in the root design and the parent blocks.

- b. Clear the check box next to the global signals that you do not want to be inherited in the new block, and click *OK*.

For more information on working with global signals in hierarchical designs, see [About Global Signals in Hierarchical Designs](#) on page 376.

6. Select the *Ref Des range* check box if you want to specify the beginning and ending numbers for the reference designators of components in the block.
7. Click *Add Ports* to define the ports or interface signals for the block. You can add signals from the root design or add new signals to define the ports for the block.

- a. The *Available Signals* list displays the list of signals from the parent design. Select the signals you want to use as ports for the block using *Ctrl* or *Shift* keys and then click *Add*. The selected signals appear in the Port Name list.

or

Enter the port names in the *Port Name* column.

Note: You can also paste the port names from other applications such as Microsoft Excel.

- b. Select the port type for each port as `IN`, `OUT`, or `INOUT` in the *Port Type* column.

Note: To specify the same port type for more than one port, select the port type field next to the ports and then select the port type from the drop-down list.

Note: While defining ports, you can right-click to use commands from the context sensitive menu. These commands help you add and delete ports, modify the port type and cut, copy or paste port information.

8. Select the *Add instance to design* check box to add an instance of the new block in the selected design.

Note: If you do not select this check box, an instance of the block will not be added to the current design by default. You can add it later using Component Browser. For more information, see [Adding Blocks from a Library](#) on page 345.

9. Click *OK*.

The [Block Packaging Options](#) dialog box appears. This dialog box allows you to specify how you want the block to be packaged in context of the design in which it is being added.

10. Specify the block packaging options and click *OK* to create the block.

You can now edit the block to add connectivity information for the block. For more information on editing blocks, see [Editing a Hierarchical Design](#) on page 358.

Creating Sub-Projects for Blocks

When you are creating a hierarchical design in a team design environment, each designer in the design team has to create a project for the blocks assigned to him.

This requires that the projects created by every designer must have the same settings. For example, all the projects must have the same packaging options, use the same list of component libraries, signal integrity model libraries, physical part table files, and so on.

System Connectivity Manager lets you specify the project settings in the project containing the top-level or root design for the hierarchical design and then create sub-projects for each block in the hierarchical design. The sub-projects will have the same project settings as that of the project containing the top-level design. For more information on creating sub-projects for blocks, see [Creating Sub-Projects](#) on page 394.

After the blocks in the sub-projects are finalized, the blocks can be imported into the project containing the top-level or root design for the hierarchical design. For more information on importing blocks, see [Importing a Block](#) on page 395.

Adding Blocks from a Library

You can add spreadsheet, schematic, and Verilog type blocks from the libraries added for your project. For information on adding Design Entry HDL designs as schematic blocks in System Connectivity Manager, see [Adding or Importing Design Entry HDL Blocks in System Connectivity Manager](#) on page 348.

Cadence recommends that you set the design in which want to add a block as the root design and then add the block. For more on setting the root design for the project, see [Setting the Root Design](#) on page 374.

Note: You cannot add a block that is currently set as the root design for the project.

To add blocks from a library to your design

1. Do one of the following:

- Choose *Design – Add Component*.
- Click  on the toolbar.

Part Information Manager appears.

2. Click *Browse Libraries*.

3. Select the library in which the block exists in the *Library* list.

4. Select the block in the *Cells* list.

5. Click *Add*.

The Block Packaging Options dialog box appears.

For more information on specifying the packaging options for a block, see [Block Packaging Options](#) on page 687.

6. Specify the packaging options for the block and click *OK*.

System Connectivity Manager automatically packages the block and adds it in the design.

7. Click *Close* to close Part Information Manager.

Importing Blocks from Another Project

System Connectivity Manager allows you to import a block from another project (.cpm) file or from the cds.lib file of another project into your current design. You can import a block as a read-only block or as a read-write block into your design.

For more information on importing blocks, see [Importing a Block](#) on page 395.

Adding Spreadsheet and Verilog Blocks from Another Project

You can add spreadsheets and Verilog blocks that exist in another project into the current project in System Connectivity Manager.

1. If the project in which you want to add the spreadsheet or Verilog block is open in System Connectivity Manager, close the project by exiting System Connectivity Manager.
2. Define the library containing the spreadsheet or Verilog block and the libraries used by the block in the `cds.lib` file for the project in System Connectivity Manager, or include the `cds.lib` file for the project in which the block exists in the `cds.lib` file for the project in which you want to add the block.

For example, if the spreadsheet or Verilog block exists in a library named `memory_lib` and uses the `part`, `array`, `memory`, `discrete` and `standard` located at `c:\memory_design`, define the libraries by adding the following entries in the `cds.lib` file for the project in which you want to add the block:

```
DEFINE memory_lib c:\memory_design\memory_lib
DEFINE array c:\memory_design\array
DEFINE memory c:\memory_design\memory
DEFINE standard c:\memory_design\standard
DEFINE discrete c:\memory_design\discrete
```

OR

Include the `cds.lib` file for the project containing the spreadsheet or Verilog block by adding the following entry in the `cds.lib` file for the project in which you want to add the block:

```
INCLUDE c:\memory_design\cds.lib
```

For more information on the `cds.lib` file, see [The cds.lib File](#) on page 98.

3. Open the project in which you want to add the spreadsheet or Verilog block in System Connectivity Manager.
4. If the components in the block you are adding refer to library level physical part table (`.ptf`) files, ensure that the library level `.ptf` files are setup for your project in System Connectivity Manager. For more information on setting up library level `.ptf` files for your project, see [Setting Up Physical Part Table Files for a Project](#) on page 104.
5. If you have assigned signal integrity (SI) models to components, pins and nets in the block you are adding, ensure that SI libraries containing the models are setup for your project in System Connectivity Manager. For more information on setting up SI model

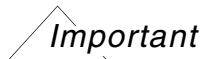
libraries in System Connectivity Manager, see [Setting Up SI Model Libraries](#) on page 320.

6. Add the block in the project.

For information on adding blocks in System Connectivity Manager, see [Adding Blocks from a Library](#) on page 345.

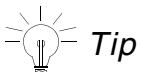
Adding or Importing Design Entry HDL Blocks in System Connectivity Manager

You can add or import the schematic blocks existing in another project into the current project in System Connectivity Manager.



Before you add or import a Design Entry HDL block as a block in SCM, do the following:

- 1.** If the project in which you want to add or import the schematic block is open in SCM, close the project by exiting System Connectivity Manager.
- 2.** Open the project containing the schematic block in Design Entry HDL version 15.5 or later.
- 3.** If you have used Constraint Manager to capture electrical constraints in your Design Entry HDL design, or if you have used electrical constraint or DIFFERENTIAL_PAIR properties in your Design Entry HDL design, do the following:
 - a.** Choose *Tools - Constraints - Edit* to open Constraint Manager.
 - b.** Choose *File - Save* in Constraint Manager or Design Entry HDL.
 - c.** Close Constraint Manager.
- 4.** Choose *File - Save Hierarchy* in Design Entry HDL.
- 5.** Exit Design Entry HDL.



If you have not used Constraint Manager to capture electrical constraints in your Design Entry HDL design, you can use the following command for preparing the Design Entry HDL block for use in System Connectivity Manager instead of performing Steps 2 to 5 described below:

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```
netassembler -proj <project_name>.cpm -mode tdd
```

For example, if the Design Entry HDL design exists in a project named controller.cpm, change to the project directory and run the following command:

```
netassembler -proj controller.cpm -mode tdd
```



If you keep the *Retain diff pair//xnet* option ON while creating the Design Entry HDL project that contains library-defined differential pairs, it is recommended that you synchronize the project with Allegro before you add the block to SCM.

If you do not synchronize the project with Allegro, XNets and differential pairs are not created in *Constraint Manager connected to Design Entry HDL*, but are created in *Constraint Manager connected to System Connectivity Manager*. This difference can lead to confusion in the design cycle.

Alternatively, you can create a Design Entry HDL project with the *Retain diff pair/ xnets* option OFF, and library-defined differential pairs are displayed in Constraint Manager connected to both SCM and DEHDL.

6. Define the library containing the Design Entry HDL block and the libraries used by the Design Entry HDL design in the `cds.lib` file for the project in System Connectivity Manager, or include the `cds.lib` file for the project in which the Design Entry HDL block exists in the `cds.lib` file for the project in System Connectivity Manager.

For example, if the Design Entry HDL block exists in a library named `memory_lib` and uses the part libraries, `array`, `memory`, `discrete` and `standard` located at `c:\memory_design`, define the libraries by adding the following entries in the `cds.lib` file for the project in System Connectivity Manager:

```
DEFINE memory_lib c:\memory_design\memory_lib  
DEFINE array c:\memory_design\array  
DEFINE memory c:\memory_design\memory  
DEFINE standard c:\memory_design\standard  
DEFINE discrete c:\memory_design\discrete
```

OR

Include the `cds.lib` file for the project containing the Design Entry HDL block by adding the following entry in the `cds.lib` file for the project in System Connectivity Manager:

```
INCLUDE c:\memory_design\cds.lib
```

For more information on the `cds.lib` file, see [The cds.lib File](#) on page 98.

7. Open the project in which you want to add or import the schematic block in System Connectivity Manager.

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8. If the components in the block you are adding refer to library level physical part table (.ptf) files, ensure that the library level .ptf files are setup for your project in System Connectivity Manager. For more information on setting up library level .ptf files for your project, see [Setting Up Physical Part Table Files for a Project](#) on page 104.
9. If you have assigned signal integrity (SI) models to components, pins and nets in the block you are adding or importing, ensure that SI libraries containing the models are setup for your project in System Connectivity Manager. For more information on setting up SI model libraries in System Connectivity Manager, see [Setting Up SI Model Libraries](#) on page 320.
10. Ensure that \g and \i are used as suffixes for identifying global signals and interface signals, respectively. This is important if the schematic in Design Entry HDL is created by importing design data from some other schematic tool.

You can now add or import the Design Entry HDL block as a schematic block in System Connectivity Manager.

- For information on adding blocks in System Connectivity Manager, see [Adding Blocks from a Library](#) on page 345.
- For information on importing blocks in System Connectivity Manager, see [Importing a Block](#) on page 395.

Important

To successfully import a DE-HDL schematic block in System Connectivity Manager, it is required that the constraints in the schematic are synchronized with the Constraint Manager.

You cannot import a DE-HDL schematic that has constraints defined only in schematic sheets, and does not have a constraints view. To import such a schematic, you need to synchronize constraints in DE-HDL and Constraint Manager. To know more about synchronizing constraints, see *Allegro Design Entry HDL Constraint Manager Flow Guide*.

Note the following after you have added or imported the Design Entry HDL block as a schematic block in System Connectivity Manager:

- If your schematic block has two or more symbols with a common pin (a pin with the same name and number across multiple sections) and if the common pin on only one of the symbols is connected to a signal, Design Entry HDL packages such symbols together into the same package. However, System Connectivity Manager cannot package such symbols into the same package and reports packaging errors for such symbols in the schematic block.

- If the logical net name of a net in the schematic block has more than 31 characters, System Connectivity Manager renames the physical net name of the net such that the physical net name has only 31 characters.
- Unnamed nets in your schematic block are renamed in System Connectivity Manager. For example, an unnamed net in the schematic with the name `UN1ALS192$I1$C` is named as `unnamed_1_als192_i1_c` in System Connectivity Manager.

Editing the imported block in Design Entry HDL

If the schematic imported as a block in System Connectivity Manager is to be modified in Design Entry HDL, you need to ensure the following:

1. Synchronize the schematic with the constraints in the Constraint Manager.
 - a. Choose *Tools – Constraints – Edit* to open Constraint Manager.
 - b. Choose *File – Save* in Constraint Manager or Design Entry HDL.
 - c. Close Constraint Manager.
2. Refresh the Design Entry HDL block in System Connectivity Manager.
 - a. Open the spreadsheet design.
 - b. Click Resolve.

Adding or Importing Verilog files as Spreadsheet Blocks

System Connectivity Manager lets you import structural Verilog HDL files into your design. When you import a Verilog file, System Connectivity Manager parses the file for errors and creates blocks for the modules in the Verilog file. You can then add the blocks in your design.

System Connectivity Manager creates spreadsheet blocks for the modules in the Verilog file.



Properties defined in the Verilog file are not imported.

Note: If the Verilog file (created in Design Entry HDL) you are importing in System Connectivity Manager has unconnected signals like `open_p1$1`, rename all the unconnected signals named `open_p*${}` to `NC` before importing the Verilog file. If you do not rename such unconnected signals to `NC`, the import process will fail.

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When importing Verilog files, System Connectivity Manager lets you use a map file to map component names in the Verilog file to cell (component) names in the libraries added for your project. You can also use the map file to map the port names of a component in the Verilog file to the port names of the cell (component) in a library.

To import a Verilog file:

1. Choose *Project – Import –Verilog – Netlist*

The Import Verilog dialog box appears.

2. Specify the name and path to the Verilog file you want to import, or click the browse button to select the Verilog file.
3. Specify the name of the library in which you want to create blocks for the modules in the Verilog file.

By default, the blocks will be created in the working library (the library that contains the current root design (top-level design) for the project).

Blocks are created in the library for every module in the Verilog file. For example, if you import the following Verilog file, two blocks named `Top` and `Mid` are created in the library.

Contents of Verilog File

```
module Top ( x, y, carry_out, sum, carry_in);
    input x, y;
    output sum, carry_in, carry_out;
endmodule

module Mid ( x,y,carry,sum);
    input x, y;
    output sum, carry;
endmodule
```

4. Select the *Use Instance Names as Reference Designator* check box if you want to use the instance names for components in the Verilog file as reference designators.

For example, if you select this check box and import the following Verilog file, the reference designator assigned for the resistors will be `I1`, `I2`, `I3` and the reference designator for the capacitor will be `I4`.

Contents of Verilog File

```
module res (in, out);
    input in;
    output out;
    wire w1,w2;
```

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```
resistor i1 (.a(in) ,.b(w1));  
endmodule
```

If you do not select this check box, the reference designators R1, R2 and R3 are assigned to the resistors and the reference designator C1 is assigned to the capacitor.

5. Select the *Import Interfaces Only* check box if you want to the information related to the IO ports to be added in System Connectivity Manager.
6. Selecting the *Import Interfaces Only* check box enables the Module Name drop-down list box and the *Get* button.

In the Module Name drop-down list box, you specify the name of the module in the verilog file that is to be imported.

For example, if you select the *Import Interfaces Only* check box and try to import the interfaces shown in Verilog file listed below, enter the *Module Name* as `res`.

Contents of Verilog File

```
module res (in, out);  
    input in;  
    output out;  
    wire w1,w2;  
    resistor i1 (.a(in) ,.b(w1));  
endmodule
```

After a successful import, the `in` and `out` ports will be included in the signal list pane.

7. To populate the Module Name drop-down list, click *Get*.
8. From the Module Name drop-down list, select the module to be imported in the design.
9. Select the *Map Cells/Port Names* check box if you want to map cell names and port names.

System Connectivity Manager lets you use a map file to map component names in the Verilog file to cell (component) names in the libraries added for your project. You can also use the map file to map the port names of a component in the Verilog file to the port names of the cell (component) in a library.

10. Specify the name and path to the map file you want to use to map component names in the Verilog file to cell names and port names in the Verilog files to port names of the cell.

For example, if you import the following Verilog file

Contents of Verilog File

```
module example ();  
    wire a,b,c;
```

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```
and_gate i1 (in1 (a),  
             in2 (b),  
             out1 (c));  
endmodule
```

and select the following map file,

Contents of Map File

```
(  
("and_gate" "ls00"  
(ports  
  ("in1" "a")  
  ("in2" "b")  
  ("out1" "\y* "))  
)  
)
```

the following happens when you import the Verilog file:

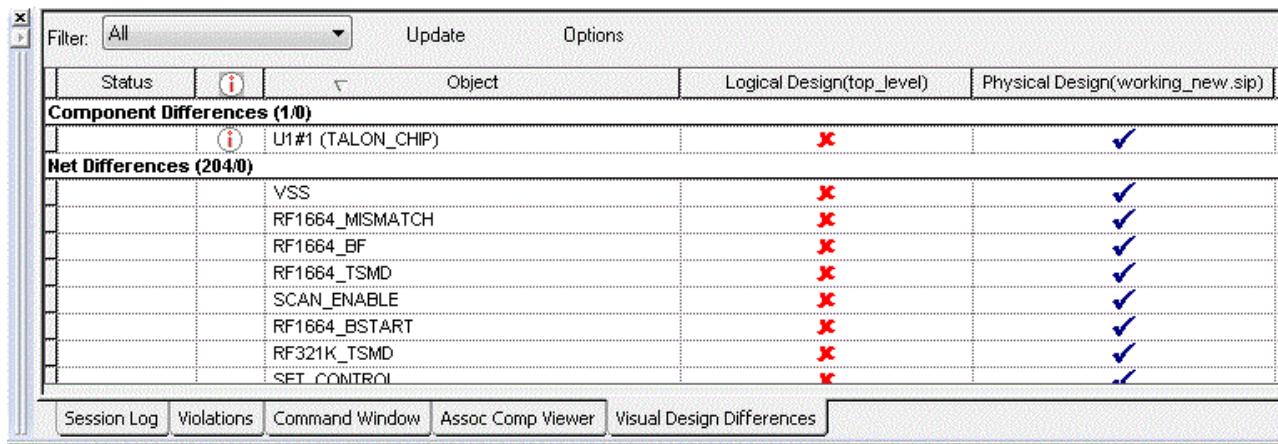
- A block named `example` is created in the selected library
- The component `and_gate` gets mapped to the cell (component) `ls00` in the libraries added for the project.
- The port `in1` of the component `and_gate` gets mapped to port `a` of the `ls00` cell.
- The port `in2` in the component `and_gate` gets mapped to port `b` of the `ls00` cell.
- The port `out1` in the component `and_gate` gets mapped to port `y*` of the `ls00` cell.

11. Click *OK* to import the verilog file.

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The Visual Design Differences pane displays differences between the design and the verilog file.



12. Choose *Update — All* to update the changes.



Verilog will not be imported if:

- ❑ There is a mismatch between the number of pins or pin names between the component in the SCM design and the component in the verilog design.
- ❑ There is a mismatch between the name of a components in the SCM design and a module in the verilog file. The names are case-sensitive, to ensure correct case before importing.
- ❑ Any referenced modules are not present in the library.

Creating a Hierarchical Design

The hierarchical design method is typically followed for large and complex designs. These designs are divided into individual blocks where each block represents a logical function.

To create a hierarchical design in System Connectivity Manager, you can use either of the following methods:

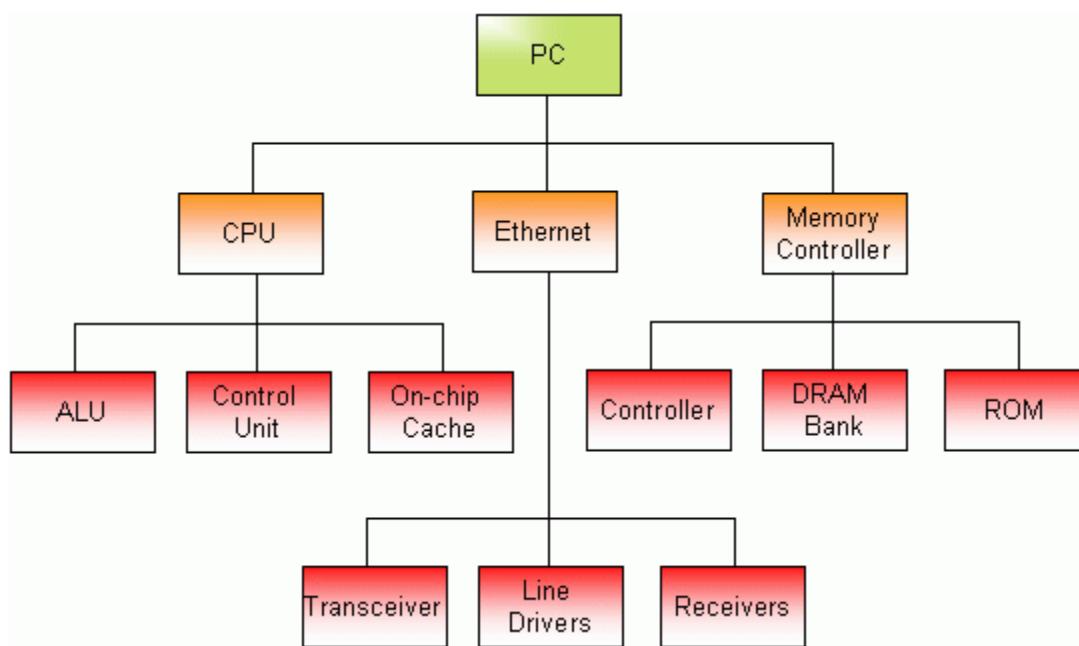
- Top Down method
- Bottom Up method

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Let us take the example of the hierarchical design shown in Figure 13-2 to understand the methods for creating a hierarchical design.

Figure 13-2 Example of a Hierarchical Design



Top Down Method

In the Top Down method, you first create the top-level design (PC in this case). In the top-level design you can add blocks that represent individual modules. In the case of the PC design, the top-level design will have three blocks:

- CPU
- Ethernet
- Memory Controller

After creating the top-level design with the necessary blocks, you create the lower-level blocks. For example, for the block CPU, create the three sub-blocks named:

- ALU
- Control Unit
- On-chip Cache

To create the hierarchical design using the top down method

1. Choose *View - Hierarchy Viewer*.

The Hierarchy Viewer appears.

2. In the Hierarchy Viewer, double-click the top-level design PC.

3. Create the blocks named CPU, Ethernet and Memory Controller.

For more information on creating blocks, see [Creating a Block and Adding it in the Current Design](#) on page 343.

4. In the Hierarchy Viewer, double-click the CPU block to open the CPU block for editing.

5. Create the blocks ALU, Control Unit and On-chip Cache and add them to the ETHERNET block by following the procedure described in [Creating a Block and Adding it in the Current Design](#) on page 343.

You can complete the design PC by creating blocks for all levels of the design.

Bottom Up Method

In the Bottom Up method, you create a lower-level block first. For the design Ethernet, you can first create the blocks for Transceiver, Line Drivers, and Receivers. You then create the higher level block Ethernet and add the blocks Transceiver, Line Drivers, and Receivers under it. Finally you add the Ethernet block in the PC design.

To create the hierarchical design using the bottom up method

1. Create the blocks Transceiver, Line Drivers, and Receivers by following the procedure described in [Creating a Standalone Block in a Library](#) on page 341.
2. Create the block named Ethernet by following the procedure described in [Creating a Standalone Block in a Library](#) on page 341.
3. Add the blocks Transceiver, Line Drivers, and Receivers in the Ethernet block by following the procedure described in [Adding Blocks from a Library](#) on page 345.
4. Add the Ethernet block in the PC design by following the procedure described in [Adding Blocks from a Library](#) on page 345.

Advantages of Hierarchical Designs

Hierarchical designs have the following advantages:

- The top-level data flow in the design is easy to understand. The design stays compact.
- Part properties that control packaging or part placement, and electrical constraints defining the electrical design rules can be assigned at the block level.
- You can replicate blocks easily. Changes within a block are replicated to all instances of the block in your design.
- You can debug each block separately.
- You can use hierarchy to facilitate a team design approach, when separate engineering teams are working within their respective blocks. For information on working on hierarchical designs in a team design environment, see [Chapter 15, “Team Design.”](#)
- Blocks can be associated with PCB layout blocks for design reuse. For information on creating and using reusable blocks in your design, see [Chapter 17, “Design Reuse.”](#)

Editing a Hierarchical Design

You can edit the blocks in your design in the master mode or in context of the root design.

Master mode

In this mode, the changes you make to a block are applied to all instances of the block in the design.

Note: The top-level or root design is always opened for editing in master mode.

For more information, see [Editing a Block in Master Mode](#) on page 359.

Context mode	<p>In this mode, the property and electrical constraint changes you make to a block are written in the property file of the root design. In other words, the property and electrical constraint changes you make to a block are visible in the block only when you open the block for editing in context of the root design.</p> <p>For example, add a block named <code>CACHE</code> in a root design named <code>MEMORY</code>. Open the <code>CACHE</code> block for editing in context mode and make some property changes. If you now edit the <code>CACHE</code> block in master mode or set the <code>CACHE</code> block as the root design, the property changes you made in the <code>CACHE</code> block when editing it in context of the root design <code>MEMORY</code> will not be visible in the <code>CACHE</code> block.</p> <p>Note: In the context mode, the component and connectivity changes you make to the block are applied to all instances of the block in your design.</p> <p>For more information, see Editing a Block in Context of the Root Design on page 360.</p>
--------------	--

Though you can edit blocks in master and context mode, Cadence recommends that you set the block in which you want to make component or connectivity changes as the root design and then make the required changes. For more information on setting a block as the root design, see [Setting the Root Design](#) on page 374.

Note: If you have added more than one instance of a block in a design, the errors, if any, in the block will be reported for each instance of the block in the Violations window. For example, if you have added four instances of a block in a design, errors in the block will be reported four times in the Violations window. Cadence recommends that you edit the block in master mode and correct the error. When you correct the error in master mode, all the four errors are resolved in one go. If you edit the block in context mode to correct the error, only the error related to the instance of the block will get resolved.

Editing a Block in Master Mode

To edit a block in master mode

1. Do one of the following:
 - Choose *Project - Edit Block*.
 - Choose *File - Open - Block*.

The *Edit Block* dialog box appears.

2. Click the *Library* drop-down list and select the library that contains the block you want to edit in master mode.
3. Select the block from the *Cell* list and click *OK*.

If the block you are editing is of spreadsheet or Verilog type, System Connectivity Manager opens a new tab for editing the block in master mode. System Connectivity Manager's title bar displays the mode in which you have opened a block for editing. For example, if you open a block named `mem_blk` in master mode, the title bar displays:

[mem_blk [In Master]]

If the block you are editing is of schematic type, the block is opened for editing in Design Entry HDL. When you save the schematic block in Design Entry HDL, the following warning message is displayed in the Violations window in System Connectivity Manager:

Schematic block `<block_name>` has been modified in Allegro Design Entry HDL.

Click the *Resolve* button in the Violations window to reload the schematic block in System Connectivity Manager.

Editing a Block in Context of the Root Design

To edit a block in context of the root design

- Do one of the following:
 - Choose *View - Hierarchy Viewer*.
The *Hierarchy Viewer* appears.
Double-click on the block.
 - Select the block in the *Component List* and do one of the following:
 - Choose *Design - Descend*.
 - Click  on the toolbar.

System Connectivity Manager opens a new tab for editing the block in context of the root design.

Note: When you open a block of type schematic in context mode, the schematic block is opened in the spreadsheet view in System Connectivity Manager (and not in Design Entry

HDL) in read-only or view mode. You cannot make any changes to the schematic block you are editing in context mode.

System Connectivity Manager's title bar displays the mode in which you have opened a block for editing. For example, if you open a block named ROM in context of a root design named mem_blk, the title bar displays:

[ROM [In Context: mem_blk.i1]]

This means that the block ROM with the instance name i1 is being edited in context of the root design mem_blk.

Working with Blocks

This section describes the following procedures for working with blocks.

- [Modifying the Packaging Options for a Block](#) on page 361
- [Editing the Reference Designator Range of a Block](#) on page 362
- [Navigating Signals in a Hierarchical Design](#) on page 363
- [Copying and Pasting Blocks](#) on page 364
- [Saving a Copy of a Block](#) on page 365
- [Importing Blocks](#) on page 366
- [Deleting Blocks](#) on page 366
- [Adding Multiple Instances of a Logical Block in a Design](#) on page 366
- [Specifying Packaging Options for Multiple Blocks](#) on page 367

Modifying the Packaging Options for a Block

To modify the packaging options for a block

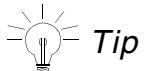
1. Select the block in the Component List.
2. Choose *Object - Block Packaging Options*.

The *Block Packaging Options* dialog box appears.

For more information on specifying the packaging options for a block, see [Block Packaging Options](#) on page 687.

3. Specify the packaging options for the block and click *OK*.

Note: Modifying Block Packaging Options applies to connectivity objects only. It does not modify constraint objects such as user-defined differential pairs, match groups and so on.



To control the reference designators for components in blocks, it is recommended to use the reference designator range, reference designator prefix or reference designator suffix packaging options for the blocks in the design. These options help you:

- Avoid packaging errors by ensuring that the same reference designator is not assigned to packages in different blocks.
- Easily identify the block in which a component having a specific reference designator exists. This is helpful when you are debugging the design with respect to the board as you can trace back parts on the board to a specific block in System Connectivity Manager.

Editing the Reference Designator Range of a Block

When you create a block or add it in the design, you can specify the unique reference designator range you want to use to control the reference designator values of components in the block. For example, if you specify the reference designator range 1 to 100 for a block named ROM and the reference designator range 201 to 300 for a block named CACHE, the reference designators of components in the ROM block will start from say, U1 and go up to U100. You cannot have a component with the reference designator U105 in the ROM block.

You can edit the reference designator range to modify the existing range, or to specify the reference designator range:

- If there are conflicts in the reference designator range of blocks in the design, or if no reference designator range is specified for blocks in the design and packaging errors occur because of conflict in reference designator values in the design.

For example, if a block named ROM with the reference designator range 1 to 50 has a component with the reference designator U25, and another block named CONTROL with no reference designator range has a component with the reference designator range U25 System Connectivity Manager reports packaging errors because of conflict in reference designator blocks. To avoid packaging errors in the future, you can rename the reference

designator for the component in the CONTROL block to, say, U101 and specify the reference designator range 101 to 200 for the CONTROL block.

- If the specified reference designator range is not sufficient for a block, or if you want to reduce the reference designator range for the block.

For example, if you have specified a reference designator range 1 to 50 for a block, the block can support only reference designators from, say, U1 to U50. If you want to assign a reference designator, say U55 in the block, you need to increase the reference designator range for the block to, say, 1 to 100.

You can also remove the reference designator range if you do not want to use a reference designator range for a block.

To edit the reference designator range of a block

1. Open the block for which you want to edit or remove the reference designator range.
For more information on editing blocks, see [Editing a Hierarchical Design](#) on page 358.
2. Choose *Design - Edit Block Refdes Range*.

The Edit Design Ref Des Range dialog box appears.

- To specify a new reference designator range, select the *Ref Des Range* option and enter the range.

Note: Ensure that the new reference designator range has the minimum range width displayed in the dialog box. For example, if the block has 12 components, the minimum range width required will be 12. This means that you must specify a reference designator range that has a width of 12, say 101 to 112 in the Use Ref. Des. Range field.

- To remove the reference designator range specified for the block, select the *Remove Ref Des Range* option.

3. Click *OK*.

Navigating Signals in a Hierarchical Design

In complex hierarchical designs, a large number of signals may be aliased to each other in the same block or across different blocks. This makes it difficult to quickly identify the aliases of a signal and view their connectivity for debugging purposes.

You can use the Signal Navigate window to quickly view the aliases for a signal at all levels of a hierarchical design and navigate the signal to view its connectivity. For more information on using the Signal Navigate window, see [Using Signal Navigate](#) on page 226.

Copying and Pasting Blocks

You can copy a block and paste it in the same parent design or in another block.

When you copy and paste a block, its connectivity and property information, and the comments added on the block are also copied. This lets you add connectivity and property information on one instance of a block and copy and paste it to quickly add another instance of the block with the same connectivity and property information, thus avoiding the need to add connectivity and property information for each instance of the block in the design.

To copy a block

1. Select the block in the Component List.
2. Choose *Edit - Copy* or press *Ctrl + C*.

To paste a block

1. Open the block in which you want to paste the block.
2. Click in the Component List.
3. Choose *Edit - Paste* or press *Ctrl + V*.

The [Block Packaging Options](#) dialog box appears. This dialog box allows you to specify how you want the block to be packaged in context of the design in which it is being added.

4. Specify the block packaging options and click *OK* to paste the block.

Using Paste Special to Paste Blocks

You can use the *Paste Special* command when you paste a block in the Component List if you want to specify whether you want the connectivity information, property information and the comments on the original instance of the block to be pasted on the new instance of the block.

1. Click in the Component List.
2. Choose *Edit - Paste Special*.

The Paste Special dialog box appears.



Note: The *Paste Special* command will work only if you have data copied to the Clipboard using the Copy or Cut commands.

3. Select the *With Properties* check box if you want the properties on the original block to be pasted.
4. Select the *With Connectivity* if you want the connectivity information on the original block to be pasted.

The connectivity information including its pin-signal connectivity, and the terminations, bypass capacitors and pullups and pulldowns added on the original component are pasted.

5. Select the *With Comments* check box if you want the comments on the original block to be pasted.
6. Click *OK*.

The Block Packaging Options dialog box appears. This dialog box allows you to specify how you want the block to be packaged in context of the design in which it is being added.

7. Specify the block packaging options and click *OK* to paste the block.

Saving a Copy of a Block

You may want to save a copy of a block and modify it to suit your requirements. System Connectivity Manager lets you save a copy of a block or type spreadsheet or Verilog that you are editing in the master mode. For more information on editing blocks, see Editing a Hierarchical Design on page 358.

Note: You cannot save a copy of a block of type schematic.

To save a copy of a block

1. Open the block for editing in the master mode.

For more information, see [Editing a Block in Master Mode](#) on page 359.

2. Choose *File – Save As*.

The Block Save As dialog box appears.

3. Enter the name for the copy of the block in the *Block Name* field.
4. Select the library in which you want to save the new block.
5. Click *OK*.

Importing Blocks

You can import a block from another project (.cpm) file or from another `cds.lib` file into your current design. For more information on importing blocks, see [Importing a Block](#) on page 395.

Deleting Blocks

To delete a block

- Select the block in the Component List and press the *Delete* key.

Note: When you delete a block, it is only deleted from the design. The block is not deleted from the library in which it exists. You can later add the block in your design by performing the steps described in [Adding Blocks from a Library](#) on page 345.

Adding Multiple Instances of a Logical Block in a Design

If required, you can simultaneously add multiple instances of a block to a design and also package them. The steps required for adding multiple instances of a block from a library to your design are listed below.

1. To add blocks, launch Part Information Manager using one of the following steps:
 - Choose *Design – Add Component*.
 - Click  on the toolbar.
- Part Information Manager appears.

2. Click *Browse Libraries*.
3. Select the library in which the block exists in the *Library* list.
4. Select the block from the *Cells* list.
5. In the Search Results pane, click on the message, *No parts found, click here to view the details of component*.

Part details are displayed in a new tab.

6. In the *Instances* spin box, specify the number of instances of the block to be added to the design. For adding multiple instances of the block, the number specified should be greater than 1.
7. Click *Add*.

The Block Packaging Options dialog box appears.

Note: In this step, you specify the packaging options for all instances of the block. Depending on the selected packaging option, you can provide your inputs for individual instances or for all instances simultaneously. For more information on specifying the packaging options, see [Specifying Packaging Options for Multiple Blocks](#) on page 367.

8. Specify the packaging options for the block and click the *Apply* or *Apply All* button.

System Connectivity Manager automatically packages the block and adds it to the design.

Note: Depending on the packaging options selected by you, either *Apply* or *Apply All* button will be activated. To know more about when each button is activated, see [Block Packaging Options](#) on page 687.

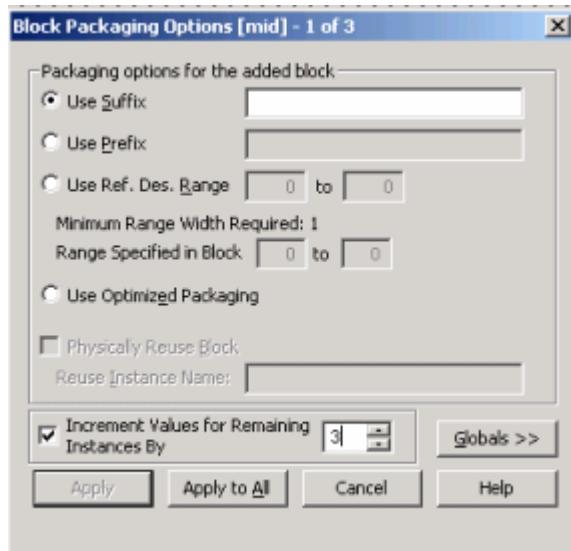
9. Click *Close* to close Part Information Manager.

Specifying Packaging Options for Multiple Blocks

When you simultaneously instantiate multiple instances of a block in a design, the information entered by you in the Block Packaging Options dialog box, is applicable to all the instances. The packaging options available are:

- [Use Suffix](#)
- [Use Prefix](#)
- [Use Ref. Des. Range](#)

□ Use Optimized Packaging



Note: The procedures used for implementing the *Use Suffix* and *Use Prefix* packaging options are similar. The *Use Suffix* option is used to specify suffixes to be used for reference designators. Whereas the *Use Prefix* option is used if you want to specify prefixes to be used for reference designators.

Use Suffix

While generating reference designators, you can use a number, a letter, or an alphanumeric string as the suffix. When you select the *Use Suffix* option, you can either specify the suffix for each instance one-by-one or can select an option using which incremental suffixes are generated for reference designators for all instances of the block.

Specifying individual suffixes

1. In the *Use Suffix* text box, specify the suffix to be used.
2. Click *Apply*.

Note: The *Apply* button is enabled only if the *Increment Values for remaining Instances By* check box is clear.

3. The Block Packaging Options dialog box reappears for the next instance. By default, the suffix value is incremented by 1. You can either accept the default value or enter a different suffix value and click *Apply*.

The Block Packaging Options dialog box closes after you have entered the suffixes for all the instances of the logical block to be added to the design.

Using Incremental Values for Suffixes

1. In the *Use Suffix* text box, specify the suffix to be used.
 2. Select the *Increment Values for remaining Instances By* check box.
 3. In the corresponding spin box, enter the value by which each suffix should be incremented.
- Note:** The *Increment Values for remaining Instances By* check box and the corresponding spin box are activated only if you select *Use Suffix* or *Use Prefix* as the packaging options.
4. Click *Apply All*.

Calculating incremental suffix values

The value of the reference designator depends on the incremental value and whether the suffix or prefix entered by you is a numeral, a letter, or an alphanumeric value. The guidelines used for calculating suffix or prefix values are listed below:

1. If you specify a numeric value as the suffix, the numeric value is incremented by the value specified in the *Increment Values for remaining Instances By* spin box, to generate the consecutive suffix.

For example, if you specify the suffix value as 5 and the incremental value as 3, the suffixes used in the reference designators are 5, 8, 11, 14, and so on.
2. If you specify a letter as the suffix, the letters are incremented until the last letter, Z, and then the number of letters in the suffix is incremented by 1.

For example, if the suffix is Z and incremental value is 1, the suffixes used in reference designators are Z, AA, AB, AC and so on.
3. In case alphanumeric strings are used as suffixes, the incremented value depends on whether the string ends with a numeral or a letter. For suffix strings ending with a numeral, only the numeral part of the string is incremented.

For example, if AX8 is the suffix value to be incremented by 3, the suffixes used in the reference designators are AX8, AX11, AX14, and so on.
4. For alphanumeric suffix strings ending with a letter, only the letters are incremented.

For example, if A8C is the suffix value to be incremented by 3, the suffixes used in the reference designators are A8C, A8F, A8I, and so on.

5. For suffixes ending with special characters, numbers are appended and incremented.

For example, if a_ is the suffix value to be incremented by 2, the suffixes used in the reference designators are a_1, a_3, a_5, and so on.

Note: Asterisk (*), percent (%), and hash (#) are invalid suffix characters and should not be used.



These guidelines are valid for calculating incremental prefix values as well.

Use Prefix

Select this option if you want to specify prefixes to be used for reference designators. You can use a number, a letter, or an alphanumeric string as the prefix.

This option works similar to the *Use Suffix* option. To know more about how to use this packaging option, see the section on [Use Suffix](#) on page 368.

Use Ref. Des. Range

When you select the *Use Reference Designator Range* option, a range of values is assigned to the component as reference designators.

For example, if you specify the range as 5 to 7, the reference designators assigned to the first instance are 5, 6, and 7, the range assigned to next instance is 8 to 10, and so on.



If a design has duplicate reference designators, a packaging error is generated.

Note: The *Increment Values for remaining Instances By* check box is disabled if the *Use Reference Designator Range* option is selected.

Use Optimized Packaging

If this option is selected, all instances of the hierarchical block are packaged in the optimized mode. This implies that the reference designators of components in the block are preserved.

The *Increment Values for remaining Instances By* check box is disabled if the *Use Optimized Packaging* option is selected.

Working with Ports of a Block

The following sections describe how you can add and edit the ports or interface signals for a block.

- [Adding a Port](#) on page 371
- [Editing the Ports of a Block](#) on page 372

Adding a Port

To add a port

1. Set the block in which you want to add ports as the root design for the project.
For more information on setting a block as the root design, see [Setting the Root Design](#) on page 374.
2. Choose *Design – Add Port*.
The Add Port dialog box appears.
3. Enter the port name in the *Port Name* column.
Note: You can also paste the port names from other applications such as Microsoft Excel.
4. Select the port type for each port as `IN`, `OUT`, or `INOUT` in the *Port Type* column.
Note: To specify the same port type for more than one port, select the port type field next to the ports and then select the port type from the drop-down list.
Note: While defining ports, you can right-click to use commands from the context sensitive menu. These commands help you add and delete ports, modify the port type and cut, copy or paste port information.
5. Enter the voltage for the port in the *Voltage* column, if required.
6. Click *OK*.

The new ports are displayed in the Signal List.

Note: If you add a port in a block, the addition is automatically reflected in the design in which you have added the block.

Editing the Ports of a Block

To edit the ports of a block

1. Set the block in which you want to edit ports as the root design for the project.

For more information on setting a block as the root design, see [Setting the Root Design](#) on page 374.

2. Choose *Design – Edit Block Interface*.

The Edit Block Interface dialog box appears.

3. Select the *Ports* tab to edit the ports of the block. You can do the following in the ports tab:

- To add a new port, enter the port name in an empty row in the *New Port Name* column and select the port type in the *Port Type* column.
- To delete a port, select the row for the port by clicking the number next to the row, then press *Delete*.
- To modify the port name, enter the new name in the *New Port Name* field.
- To modify the port type, select a new port type in the *Port Type* column.

4. Click *OK*.

Note the following:

- If you delete a port, rename the port or change the port type of a port when you are editing a block in the master or context mode, the changes are automatically reflected in the design in which you have added the block.

For example, assume that a block named `CACHE` that has a port named `DATA` with the port type `IN` is added in a design named `MEMORY`. The `DATA` port is connected to the signal `CBDATA` in the `MEMORY` design.

- If you delete the `DATA` port when you are editing the `CACHE` block in master or context mode, the port and its connection to the `CBDATA` signal is also automatically deleted from the `MEMORY` design.

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- If you rename the `DATA` port to `ADDRESS` when you are editing the `CACHE` block in the master or context mode, the port name is automatically updated in the `MEMORY` design and the port `ADDRESS` is connected to the `CBDATA` signal.
 - If you change the port type of the `DATA` port to `OUT` when you are editing the `CACHE` block in master or context mode, the port type is automatically updated in the `MEMORY` design and the port remains connected to the `CBDATA` signal.
- If you set a block as the root design and delete a port, rename the port or change the port type of a port, and then set a design in which you have added the block as the root design, System Connectivity Manager reports the following error message in the *Violations* window:

Mismatch in interface ports in design <*design_name*> for block <*block_name*>.

Click *Resolve* in the *Violations* window to automatically update the port list of the block in the design with the changes you made to the ports in the block.

For example, assume that a block named `CACHE` that has a port named `DATA` with the port type `IN` is added in a design named `MEMORY`. The `DATA` port is connected to the signal `CBDATA` in the `MEMORY` design.

If you set the `CACHE` block as the root design and delete the port, rename the port or change the port type of the `DATA` port and then set the `MEMORY` design as the root design, System Connectivity Manager reports the above error message in the *Violations* window.

- If you delete a port that is connected to a signal and then undo the deletion, the deletion of the port will be undone, but the connection will not be undone.

For example, assume that a block named `CACHE` that has a port named `DATA` with the port type `IN` is added in a design named `MEMORY`. The `DATA` port is connected to the signal `CBDATA` in the `MEMORY` design.

If you delete the `DATA` port when you are editing the `CACHE` block, the port and its connection to the `CBDATA` signal is also automatically deleted from the `MEMORY` design. If you now undo the deletion, the `DATA` port is displayed on the `CACHE` block in the `MEMORY` design but the deletion of its connection to the `CBDATA` signal will not be undone.

Navigating a Hierarchical Design

You can use the *Descend* and *Ascend* commands to navigate through a hierarchical design.

Descending to a Lower-Level Block

Do one of the following:

- Choose *View – Hierarchy Viewer*.

The *Hierarchy Viewer* appears. Do one of the following:

- Double-click on the block.
 - Select the block and choose *Design – Descend*, or click  on the toolbar.
- Select the block in the *Component List* and do one of the following:
 - Choose *Design – Descend*.
 - Click  on the toolbar.

System Connectivity Manager opens a new tab for editing the lower-level block in the context of the root design. For more information on editing a design in the context of the root design, see [Editing a Hierarchical Design](#) on page 358.

Ascending to a Higher Level Block

- Select the tab for the lower-level block and do one of the following:
 - Choose *Design – Ascend*.
 - Click  on the toolbar.

System Connectivity Manager opens the tab for the higher level block

Setting the Root Design

When you create a project in System Connectivity Manager, you specify the name of the top-level design for the project. This top-level design becomes the root design for the project.

In a hierarchical design, you will have a number of blocks and sub blocks. If you are working on a specific block in the design, you may not want to work with the rest of the design (because it has some connectivity or packaging errors) or you may want to focus on completing the logic for the block and package or simulate it before proceeding with the rest of the blocks in the design. You can do this by setting the block in which you want to work as the root design. System Connectivity Manager displays only the block and the blocks under it.

To set a block as the root design, do the following:

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1. Select one of the following:

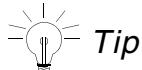
- Project – Change Root.*
- View – Hierarchy Viewer.*

The Hierarchy Viewer appears. Click  on the toolbar.

The Change Root dialog box appears.

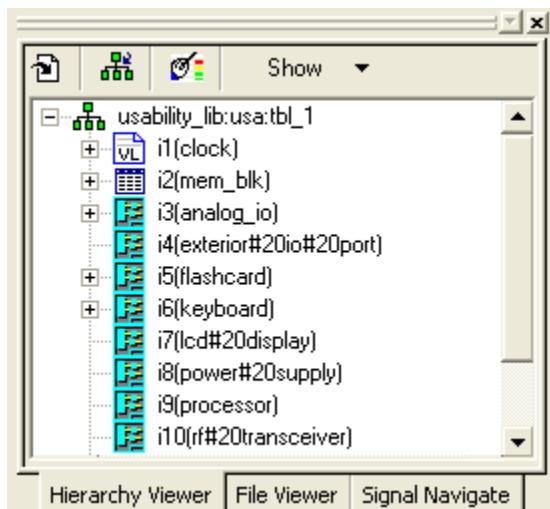
2. Click the *Library* drop-down list and select the library that contains the block you want to set as the root design.
3. Select the block from the *Cell* list and click *OK*.

System Connectivity Manager displays only the block and the blocks under it.

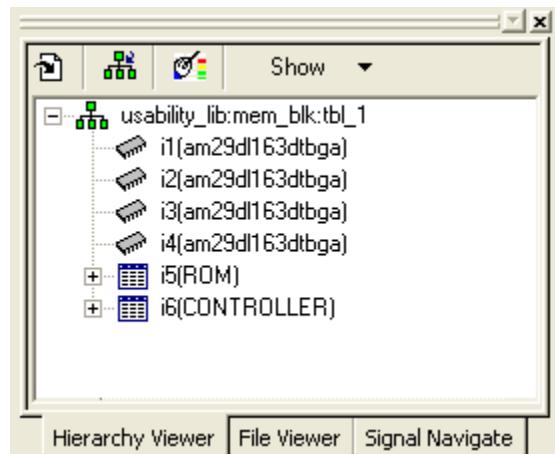


You can also select a block in the *Hierarchy Viewer*, right-click and choose *Set as ROOT* to set the block as the root design.

For example, the following figure shows a hierarchical design with the root design named *usa*. In the Hierarchy Viewer, the root design is indicated by the following icon: .

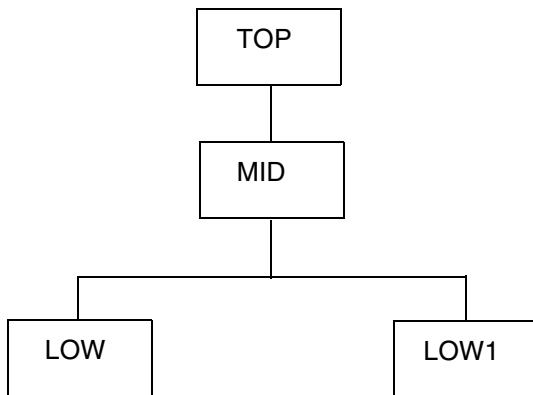


If you set the `mem_blk` block as the root design, System Connectivity Manager displays only the `mem_blk` block and the blocks under it, as shown in the following figure.



About Global Signals in Hierarchical Designs

This section describes how global signals are handled in hierarchical designs. We will use the example of a hierarchical design shown in the figure below to understand how global signals are handled in hierarchical designs.



- A global signal added in a lower-level block and its properties are pushed to the upper level blocks in a hierarchical design. For example, if you add a global signal VCC in the block LOW, the global signal and its properties are displayed in the MID and the TOP block also.
- If a global signal VCC is added in TOP block, the signal will not be visible in the lower level blocks MID, LOW and LOW1.

- If a global signal VCC exists in the block MID and you add a global signal VCC in the block LOW, the two global signals get aliased, and a global signal VCC appears in the TOP block also.
- If a local or interface signal VCC exists in the block MID and you add a global signal VCC in the block LOW, the two signals are not aliased. The scope of the global signal VCC will be limited to the block LOW.
- If a global signal VCC in the blocks TOP or MID is not connected to any pin and you delete a global signal named VCC in the block LOW, the global signal gets deleted from the LOW, MID and TOP blocks.
- If a global signal VCC in the block MID is connected to a pin and you delete a global signal named VCC in the block LOW, the global signal gets deleted only from the LOW block. The signal VCC is retained in MID as a global signal with its connectivity.

Note: It is recommended that you rename global signals only in System Connectivity Manager and not in the board in Allegro PCB Editor.

Selecting the Global Signals to be Inherited by a Block

When you create a block using the procedure described in [Creating a Block and Adding it in the Current Design](#) on page 343, you can select the global signals to be inherited in the block from the root design or the parent blocks.

Later, if you add new global signals in the root design or in the parent blocks, you can select the new global signals to be inherited in the block. You can also specify that a global signal that was previously being inherited in the block should no longer be inherited.

To select the global signals to be inherited by a block

1. Open the block for which you want to select the global signals to be inherited.

For more information on opening a block for editing in System Connectivity Manager, see [Editing a Hierarchical Design](#) on page 358.

2. Choose *Design – Edit Block Interface*.

The Edit Block Interface dialog box appears.

3. Select the Globals tab to select the global signals you want the block to inherit from the root design or the parent blocks.
 - Clear the check box next to the global signals that you want to be inherited in the block.

- Clear the check box next to the global signals that you do not want to be inherited in the block.
4. Click *OK*.

Aliasing and Masking Global Signals in Hierarchical Designs

By default, the global signals in a lower-level block in the design are inherited by the higher level blocks in the design. For example, assume that you have a block named `CPU` with a global signal named `VCC` and a local signal named `RESET` and another block named `CONTROLLER` with a global signal named `CON_VCC`. If you add the `CONTROLLER` block in the `CPU` block, the global signal `CON_VCC` is inherited by the `CPU` block (and displayed in the Signal List for the `CPU` block) and by all the blocks above the `CPU` block.

You may want to do one of the following:

- Alias the global signal `CON_VCC` to the global signal `VCC`.
- Mask the global signal `CON_VCC` by aliasing it to the local signal `RESET` if you do not want the `CON_VCC` signal to be inherited by the `CPU` block and any block above the `CPU` block.

To alias the global signal

To alias the global signal `CON_VCC` that is inherited by the `CPU` block to the global signal `VCC` in the `CPU` block, do the following:

1. Select the block in the Component List.
2. Choose *Object – Block Packaging Options*.
The *Block Packaging Options* dialog box appears.
3. Click *Globals*.

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4. Alias the CON_VCC signal in the CONTROLLER block to the global signal named VCC by clicking in the *Block "cpu"* column next to the signal CON_VCC and selecting the VCC signal from the drop-down list, as shown below.



Note: If the *Show Local Nets for Global Masking* check box is not selected, only global signals in the CPU block will be displayed in the *Block "cpu"* column.

Note: You cannot alias a vectored global signal to a vectored global signal that has a different width. For example, you cannot alias a vectored global signal DATA<3..0> to another vectored global signal CBDATA<7..0>.

5. Click *OK*.

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The CON_VCC signal will not be displayed in the Signal List for the CPU block and the VCC signal will be pushed up to the higher level blocks in the design.

To mask the global signal

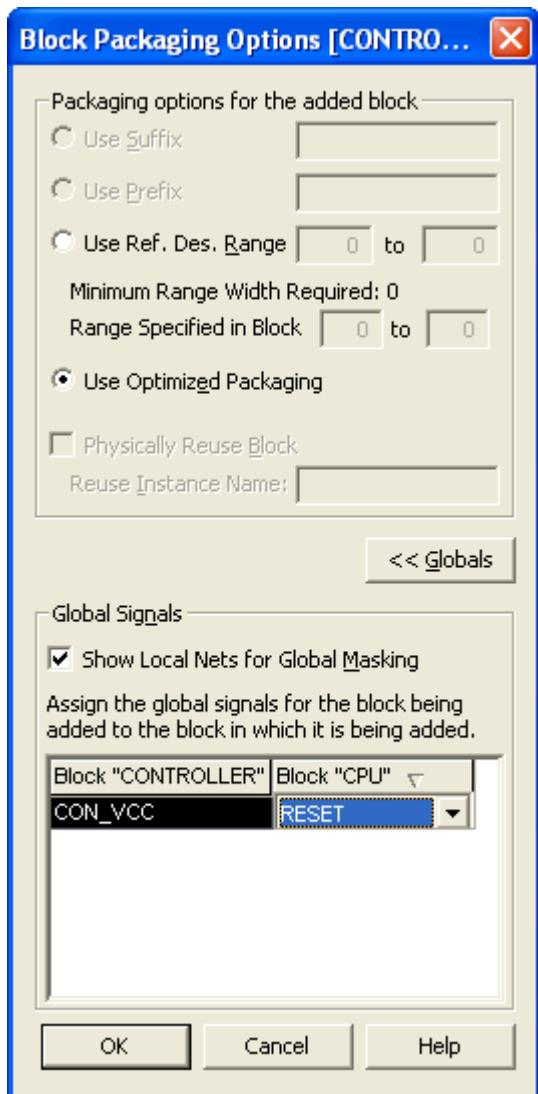
To mask the global signal CON_VCC from being inherited by the higher level blocks in the design, alias the CON_VCC signal in the CONTROLLER block to the local signal, say RESET, in the CPU block, by doing the following:

1. Select the block in the Component List.
 2. Choose *Object – Block Packaging Options*.
- The *Block Packaging Options* dialog box appears.
3. Click *Globals*.
 4. Select the *Use Local Nets for Global Masking* check box to display all the local and global signals in the CPU block.

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5. Click in the *Block "cpu"* column next to the signal CON_VCC and select the RESET signal from the drop-down list, as shown below.



Note: You cannot mask a vectored global signal with a vectored local signal that has a different width. For example, you cannot mask a vectored global signal DATA<3 .. 0> with a vectored local signal CBDATA<7 .. 0>. Also, you cannot mask a bit of a vectored global signal with a local signal or a bit of a vectored local signal.

6. Click *OK*.

The CON_VCC signal will not be displayed in the Signal List for the CPU block nor will it be inherited by the higher level blocks in the design.

Working with Read-Only Blocks in your Design

A read-only block is a block in which you do not have write permissions.

This section describes how you can use read-only blocks of type Spreadsheet and Verilog in System Connectivity Manager. For more information on how to use read-only blocks of type Schematic in System Connectivity Manager, see the *Working with Block Designs* chapter of the *Allegro Design Entry HDL User Guide*.

Using Read-Only Blocks

You can use read-only blocks in your design by doing one of the following:

- Adding the read-only block in the design.
For more information, see the following sections:
 - ❑ [Adding Spreadsheet and Verilog Blocks from Another Project](#) on page 347
 - ❑ [Adding or Importing Design Entry HDL Blocks in System Connectivity Manager](#) on page 348
- Importing a block as a read-only block. When you import a block as a read-only block, the block is copied into the working library for the current project and read-only permissions are set for the cell for the block. For more information on importing a block as a read-only block, see [Importing a Block](#) on page 395.

Editing Read-Only Blocks

When you open a read-only block for editing in context mode, you can only make property and electrical constraint changes in the read-only block. You cannot make any connectivity changes when you are editing a read-only block in context mode. For more information on editing a block in context mode, see [Editing a Block in Context of the Root Design](#) on page 360.

You might want to make connectivity and property changes to a read-only block, save the block with a different name and then add the new block in your design. To do this, do the following:

1. Open the read-only block for editing in master mode, or set the read-only block as the root design for your project.

For more information on editing a block in master mode, see [Editing a Block in Master Mode](#) on page 359. For more information on setting a block as the root design for your project, see [Setting the Root Design](#) on page 374.

2. Make the required connectivity and property changes in the block.

3. Choose *File – Save*.

The Block Save As dialog box appears.

4. Enter a new name for the block in the *Block Name* field.
5. Select the library in which you want to save the block in the *Block Library* drop-down list.
6. Click *OK*.

You can now add the modified block in your design.

Note: The modified block will have write permissions. So you can make both connectivity and property changes in the block.

Working with Read-Only Blocks

- If errors are displayed in the Violations window for an instance of a read-only block you have added or imported into your design, you cannot correct the errors because you do not have write permissions on the block. In such cases, the owner of the read-only block has to correct the errors in the block. Once the errors are corrected by the owner of the read-only block, do the following:
 - ❑ If the read-only block was added in your design, reopen the project in System Connectivity Manager.
 - ❑ If the read-only block was imported into your design, re-import the block in your design. For more information on re-importing read-only blocks, see [Reimporting a Read-Only Block](#) on page 403.
- When you perform Global Replace to replace components, nets or properties in your design, the components, nets or properties in the read-only blocks used in your design will not be replaced.

How Physical Net Names are Assigned to Signals in Hierarchical Designs

- The physical net names of bits of a vectored signal in System Connectivity Manager, say, `data<3..0>` have the following syntax:

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```
data<0>_1  
data<1>_1  
data<2>_1  
data<3>_1
```

Note: This is different from the physical net names of bits of a vectored signal in Design Entry HDL, where the bits of a vectored signal, say, `data<3..0>` have the following syntax:

```
data_1<0>  
data_1<1>  
data_1<2>  
data_1<3>
```

- When you add more than one instance of a block in a design (by selecting the *Use Optimized Packaging* option in the Block Packaging Options dialog box), System Connectivity Manager suffixes the characters `_n` to the physical net names of signals in the additional instances of the block.

For example, if you have a signal named `DATA` in a block named `CACHE` and you add two instances of the `CACHE` block in another block named `MEMORY`, the physical net name of the `DATA` signal in the first instance of the `CACHE` block will be, say `DATA` and the physical net name of the `DATA` signal in the second instance of the `CACHE` block will be `DATA_1`.

In other words, System Connectivity Manager suffixes the characters `_n` (where `n` is a number) to the signal in the second instance of the block to ensure that there is no conflict in physical net names of signals in lower-level blocks. If you now add another instance of a `CACHE` block in the `MEMORY` block, System Connectivity Manager assigns the physical net name `DATA_2` to the `DATA` signal in the third instance of the block.

Netlisting the Design for Simulation

System Connectivity Manager allows you to generate the structural Verilog netlist for all the blocks in the design. You can then use the Verilog netlist to simulate the design using the Cadence Verilog XL and NC Verilog simulators, or third-party Verilog simulators.

Generating the Verilog Netlist for Simulating the Design

Before you generate the Verilog netlist, do the following:

1. Specify the options for generating the netlist.

For more information, see [Specifying Options for Generating the Netlist](#) on page 386.

2. By default, a pullup resistor component is replaced with a `pullup` in the Verilog netlist and a pulldown resistor component is replaced with a `pulldown` in the Verilog netlist. For example, a pullup resistor connected to a signal named `reset` is written in the Verilog netlist as:

```
pullup (reset);
```

If you want any pullup or pulldown resistor component to be replaced by an open in the Verilog netlist, add the `REMOVE=EXCLUDE` property on the pullup or pulldown resistor by doing the following:

- a. Choose *View - Properties* to display the Properties window.
- b. Choose *View – Associated Components* to display the Assoc Comp Viewer.
- c. Click the Pullups/Pulldowns tab in the Assoc Comp Viewer.
- d. Click on the row for the pullup or pulldown resistor you want to be replaced by an open in the Verilog netlist.

The Properties window displays the properties of the selected resistor.

- e. Add the `REMOVE=EXCLUDE` property in the Properties window.

For more information on adding properties, see [Adding Properties in System Connectivity Manager](#) on page 254.

Specifying Options for Generating the Netlist

To Specify the Options for Generating Netlist

1. Choose *Project – Settings*.

The Settings dialog box appears.

2. Select the Verilog NetList page.
3. Specify the options for generating the Verilog netlist.
4. Click *OK*.

Generating the Verilog Netlist

For the SiP design, you can generate both, the logical and the physical, verilog netlist for the design.

To Generate Physical Netlist

- Choose *Project – Generate Verilog Netlist – Physical*.

Note: You can also run the `sipsimnetlister` command to generate the Verilog netlist from the command prompt. For more information on the `sipsimnetlister` command, see [The sipsimnetlister Command](#).

When you generate a flat verilog netlist, a single netlist file, is generated in the `sim_tbl_1` view of the root design. However, if the *Single File Netlist* check box in the Verilog NetList page of the Setup dialog box is selected, then the netlist file named `<root_design>.v` is generated and saved in the root design folder.

Note: Physical netlist is not generated in case your design has errors, such as reference designator conflicts. However, in case there is a conflict in physical net names, the verilog netlist is generated using canonical names.

To Generate Logical Netlist

- Choose *Project – Generate Verilog Netlist – Logical*.

A verilog.v file is created in the sim_tbl_1 view of each spreadsheet block in the design.

While generating the logical netlist, if the *Single File Netlist* check box in the Verilog NetList page of the Setup dialog box is selected, then along with the individual netlists for each block, a single verilog netlist is created for the root design. This netlist is named as <root_design>.v and is saved in the root design folder.

The sipsimnetlister Command

The sipsimnetlister command allows you to generate the Verilog netlist from the command prompt.

The usage for the sipsimnetlister command is:

```
sipsimnetlister -proj <project_file> [-physical] [-createconfig]
```

Where:

-proj <project_file> Specifies the path and project file (.cpm) name of the project for which you want to generate the Verilog netlist.

Example:

```
-proj c:\network_switch\network_switch.cpm
```

Note: You can use absolute and relative paths to specify the path to the project file.

-physical

This is a optional variable.
When specified it generates flat (physical) netlist for the design.

-createconfig

Generates the cfg_verilog configuration view for the root design for the project.

Viewing Verilog Netlist

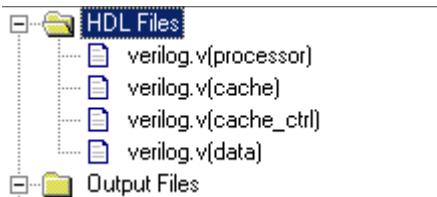
To view the Verilog netlist

1. Choose *View – File Viewer*.
2. Expand the *HDL Files* folder.

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Netlisting the Design for Simulation

The `verilog.v` file for all the spreadsheet blocks in the design is listed as shown in the figure given below.



3. To view the file, double-click on the filename.

The selected `verilog.v` file opens in a new tab.

Note: If you generate the physical netlist of the design after generating the logical netlist, then in the File Viewer, The new file for the root design will be displayed along with the verilog files generated for individual blocks in the previous run.

In the File Viewer, placeholder for a verilog file is created as soon as the netlisting process starts. As a result, if the netlist process fails, or if you try to view the verilog file before netlisting is complete, an error message appears stating that the file does not exist.

Netlisting for Non-Spreadsheet Blocks in a Design

Schematic blocks

System Connectivity Manager does not support generating the Verilog netlist for schematic blocks in the design. When you choose *Project – Generate Verilog Netlist* in System Connectivity Manager, System Connectivity Manager does not generate the Verilog netlist for the schematic blocks in the design.

To generate the Verilog netlist for each schematic block in the design complete the following:

1. Set the schematic block as the root design for the project.

For more information on setting a block as the root design, see [Setting the Root Design](#) on page 372.

2. Exit System Connectivity Manager.

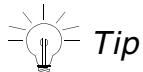
3. Use the Design Entry HDL Digital Simulation Interface to generate the Verilog netlist for the design.

For more information on using the Design Entry HDL Digital Simulation Interface, see the [Allegro Design Entry HDL Digital Simulation User Guide](#).

The Verilog netlist file for a schematic block is located in the `run` directory that you specify when creating the Verilog netlist for schematic block.

Verilog blocks

Generate Netlist does not generate netlist for the verilog blocks. This is because, the Verilog netlist file for a Verilog block is located in the `vlog_structural` view of the block.



Tip

The netlist information for schematic and Verilog blocks are not included when the Single File Netlist check box is selected. When the *Single File Netlist* check box in the Verilog Netlist setup is selected, the single file netlist named `verilog.v` created in the `sim_tb1_1` view of the root design for the hierarchical design does not include the netlist information for the schematic and Verilog blocks in the design. Use the `include` directive to include the Verilog files for the schematic and Verilog blocks in the design.

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Netlisting the Design for Simulation

Team Design

This chapter describes the following sections:

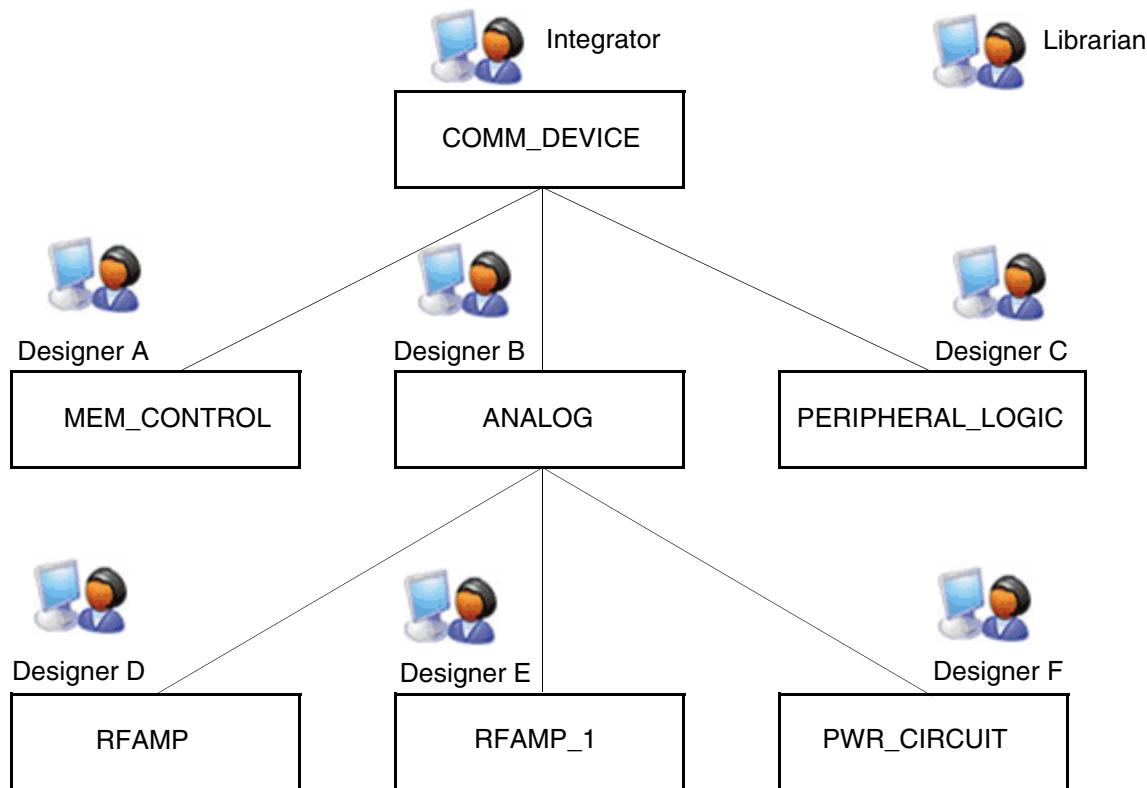
- [Overview](#) on page 392
- [Team Design Methodology](#) on page 394
- [Recommendations for Working in a Team Design Environment](#) on page 395
- [Creating Sub-Projects](#) on page 396
- [Importing a Block](#) on page 397
- [Baselining a Design](#) on page 401
- [Notifying the Design Team When a Block is Baseline](#) on page 403
- [Reimporting a Read-Only Block](#) on page 405
- [Updating the Source Location of a Read-Only Block](#) on page 405
- [Updating Components Modified by the Librarian](#) on page 406
- [Viewing the Version History of Blocks and Components](#) on page 411

Overview

With an increase in the complexity of designs and the need to reduce design cycle time, hierarchical design is becoming the preferred design approach. In the hierarchical design approach, a design is divided into sub designs or blocks, where each block represents a logical function. For more information on working with hierarchical designs, see [Chapter 13, “Working with Hierarchical Designs.”](#)

This chapter describes how you can use System Connectivity Manager to create hierarchical designs in a team design environment, in which a team of designers work on a design. Each designer may be working on one or more blocks of the hierarchical design.

Figure 15-1 Hierarchical Design Using a Team Design Approach



In the above example of a hierarchical design `COMM_DEVICE`, teams of designers work on different blocks of the design. The Librarian creates the components for the design. The Integrator (a team leader or a designated person) integrates all the blocks into the top-level design (`COMM_DEVICE`) for testing the design during the design cycle, and for signing off on the design after all the designers working on the blocks have completed their work.

During the design cycle, the components used in the design might be modified by the Librarian. The designers need to be notified when a component is modified and be able to update all the instances of the component used in the design with the modified version, on a need basis.

A designer may want to copy over a block being developed by another designer and modify it to suit his requirements. For example, in the hierarchical design `COMM_DEVICE` shown in [Figure 15-1](#) on page 392, Designer E may want to copy the `RFAMP` block being developed by Designer D and modify it to create the `RFAMP_1` block.

The Integrator may want to take a snapshot of the blocks at various points of time and integrate them into the top-level design during the testing or signoff phases of the design cycle. To achieve this, the Integrator needs to be notified when a block integrated into the top-level design is modified so that he can use the latest snapshot of the block during the testing or signoff phases.

System Connectivity Manager provides the following features to enable teams of designers to create hierarchical designs.

- Creating sub projects

For more information, see [creating Sub-Projects](#) on page 396.

- Importing blocks

For more information, see [Importing a Block](#) on page 397.

- Baselining blocks that are modified

For more information, see [Baselining a Design](#) on page 401.

- Notifying designers when a block used in a design is baselined and allowing them to update the block used in the design with the baselined block.

For more information, see the following sections:

- ❑ [Notifying the Design Team When a Block is Baselined](#) on page 403
- ❑ [Reimporting a Read-Only Block](#) on page 405
- ❑ [Updating the Source Location of a Read-Only Block](#) on page 405
- ❑ [Viewing the Version History of Blocks and Components](#) on page 411

- Notifying designers when a component used in the design is modified by the Librarian and allowing them to update all the instances of the component used in the design with the modified version.

For more information, see the following sections:

- [Updating Components Modified by the Librarian](#) on page 406
- [Viewing the Version History of Blocks and Components](#) on page 411

Team Design Methodology

Developing a hierarchical design in a team design environment involves the following steps:

1. Integrator creates a project for the top-level design and specifies the project settings that he wants to be used for the hierarchical design.
2. Integrator creates sub-projects for each block in the hierarchical design. This ensures that the project for the hierarchical design and the project for each block used in the hierarchical design have the same settings.
For more information on creating sub-projects, see [Creating Sub-Projects](#) on page 396.
3. Designers use the sub-projects to work on the blocks assigned to them.
4. Integrator imports the blocks being developed by the designers as read-only blocks into the project for the top-level design for the hierarchical design.

Note: Other designers may also import a block as a read-only block in to the design they are working on.

Note: The integrator or other designers may also import a block as a read-write block if they want to copy a block from another design and modify it to suit the requirements of their current design.

For more information on importing blocks, see [Importing a Block](#) on page 397.

5. Designers baseline the blocks they are working on, when they want to notify the integrator or other designers who have imported the blocks into their design as read-only blocks that changes have been made in the source block for the read-only block. For more information on baselining blocks, see [Baselining a Design](#) on page 401.

The integrator or other designers who have imported the blocks into their design as read-only blocks reimport the blocks when System Connectivity Manager reports that the version of the source block for a read-only block has changed. For more information on specifying the options for notifying the design team when a block is baselined, see [Notifying the Design Team When a Block is Baseline](#)d on page 403. For more information on reimporting read-only blocks, see [Reimporting a Read-Only Block](#) on page 405.

6. When the Librarian modifies the components used in the hierarchical design, he baselines the components in Part Developer. System Connectivity Manager reports the list of components used in the design that have changed and allows designers to update

all instances of the components used in their design with the latest version of the components.

For more information on updating components modified by the Librarian, see [Updating Components Modified by the Librarian](#) on page 406.

Recommendations for Working in a Team Design Environment

Cadence recommends the following when you are working in a team design environment:

- To control the reference designators for components in blocks, it is recommended to use the reference designator range, reference designator prefix or reference designator suffix packaging options for the blocks in the design. These options help you:
 - Avoid packaging errors by ensuring that the same reference designator is not assigned to packages in different blocks.
 - Easily identify the block in which a component having a specific reference designator exists. This is helpful when you are debugging the design with respect to the board as you can trace back parts on the board to a specific block in System Connectivity Manager.

To use the reference designator range, prefix, or suffix packaging options, see [Modifying the Packaging Options for a Block](#) on page 359, and [Editing the Reference Designator Range of a Block](#) on page 360.



The reference designator range, prefix, or suffix values must be unique across all the blocks used in the design. Any conflict in the reference designator range, prefix, or suffix values across blocks in the design will result in packaging errors because of conflict in reference designator values in the design.

- Use environment variables instead of absolute paths to specify the path to libraries in the `cds.lib` file for your project. Using environment variables ensures that the `cds.lib` file for your project points to the correct library path and avoids the need to edit the `cds.lib` file if the location of the libraries change.

For example, if you import a block in your design, you need to specify the path to the libraries used in the source block in the `cds.lib` file of the project in which you have imported the block. If the designer of the source block has used absolute paths like:

```
DEFINE array f:\designs\rf_designs\rflibs\array
```

and you include the `cds.lib` file of the source project in the `cds.lib` file of the project in which you have imported the block, the `cds.lib` file of the target project will point to the wrong path for the `array` library. Using environment variables in the `cds.lib` file for the project containing the source block will ensure that the `cds.lib` file of the target project points to the correct path for the `array` library.

For example, the designer for the source block can set the environment variable `RFLIBS` to point to `f:\designs\rf_designs\rflibs` and then use the environment variable in the `cds.lib` file for the project containing the source block as shown below:

```
DEFINE array $RFLIBS\array
```

You can then include the `cds.lib` file of the source project in the `cds.lib` file of the project in which you have imported the block and set the environment variable `RFLIBS` to point to `f:\designs\rf_designs\rflibs`. If the location of the `array` library changes, you need to only set the environment variable `RFLIBS` to point to the new location.

Creating Sub-Projects

When you are creating a hierarchical design in a team design environment, each designer in the design team has to create a project for the blocks assigned to him.

This requires that the projects created by every designer must have the same settings. For example, all the projects must have the same packaging options, use the same list of component libraries, signal integrity model libraries, physical part table files, and so on.

System Connectivity Manager lets you specify the project settings in the project containing the top-level or root design for the hierarchical design and then create sub-projects for each block in the hierarchical design. The sub-projects will have the same project settings as that of the project containing the top-level design. The settings in the sub-projects can further be modified as required.

For example, in the hierarchical design `COMM_DEVICE` shown in [Figure 15-1](#) on page 392, the Integrator (a team leader or a designated person) can create a project for the top-level design `COMM_DEVICE` and specify the project settings that he wants to be used for the hierarchical design. He can then create sub-projects for the `MEM_CONTROL`, `ANALOG`, `PERIPHERAL_LOGIC`, `RF_AMP`, `RFAMP_1` and `PWR_CIRCUIT` blocks so that the sub-projects use the same settings as the project for the top-level design `COMM_DEVICE`. The designers can use the sub-projects to work on the blocks assigned to them.

After the blocks in the sub-projects are finalized, the blocks can be imported into the project containing the top-level or root design for the hierarchical design. For more information on importing blocks, see [Importing a Block](#) on page 397.

To create a sub-project

1. Open the project containing the top-level or root design for the hierarchical design.
2. Specify the project settings that you want to use for the hierarchical design.
3. Choose *Project – Create Sub-Project*.

The Create Sub-Project dialog box appears.

4. Enter the name of the block for which you want to create the sub-project in the *Block Name* field.
5. Enter the name of the library in which you want the block to be created in the sub-project in the *Block Library* field.

This library will be set as the working library for the sub-project.

6. Select the implementation type of the block. You can create a block of type Spreadsheet, Verilog or Schematic.

The default implementation is Spreadsheet type.

7. Enter the name for the sub-project in the *Project Name* field.
8. In the *Project Location* field, type the path to the directory in which you want to create the sub-project, or click the browse button to select the directory in which you want to create the sub-project.

9. Click *Add Ports* to display the port list in which you can define the ports or interface signals for the block.

- a. Enter the port name in the *Port Name* column.

- b. Select the port type as `IN`, `OUT`, or `INOUT` in the *Port Type* column.

10. Click *OK* to create the sub-project.

Importing a Block

System Connectivity Manager allows you to import a block from another project (`.cpm`) file or from the `cds.lib` file of another project into your current design. You can import a block as a read-only block or as a read-write block into your design.

When you import a block, the cell for the block is copied into the working library for the current project. You can then add the block in your design. For more information on adding blocks in your design, see [Adding Blocks from a Library](#) on page 343.

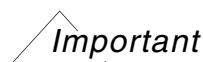
Importing as a Read-Only Block

You can import a block as a read-only block if you want to have a snapshot of the block in your design and want to be notified when changes are made to the source block.

When changes are made to the source block, the owner of the source block baselines the block. For more information on baselining a block, see [Baselining a Design](#) on page 401.

When the source block is baselined, System Connectivity Manager reports that the version of the source block has changed. You can then choose to reimport the read-only block if you want to use the latest version of the block in your design.

When you import a block as a read-only block, the block is copied into the working library for the current project and read-only permissions are set for the cell for the block.



Cadence recommends that you do not modify the read-only permissions set for the cell for a block you have imported as a read-only block in your design.

For more information on working with read-only blocks in your design, see [Working with Read-Only Blocks in your Design](#) on page 380.

Importing as a Read-Write Block

You can import a block as a read-write block if you want to copy a block from another design and modify it to suit the requirements of your current design. For example, in the hierarchical design `COMM_DEVICE` shown in [Figure 15-1](#) on page 392, Designer E can import the `RFAMP` block as a read-write block, make the required changes and then choose *File - Save As* to save the `RFAMP` block as `RFAMP_1`.

When you import a block as a read-write block, the block is copied into the working library for the current project and read-write permissions are set for the cell for the block. Any changes you make to the block will be written to the block.

Note: When you import a block as a read-write block, you break the link between the source block and the read-write block. As a result, when the source block is baselined, System Connectivity Manager will not report that the version of the source block has changed.

Before you import a block, do the following

1. If the project in which you are importing the block is open in System Connectivity Manager, close the project by exiting System Connectivity Manager.
2. Define the part libraries you have used in the source block in the `cds.lib` file for the project in which you are importing the block, or include the `cds.lib` file for the project

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in which the block exists in the `cds.lib` file for the project in which you are importing the block.

For example, if the source block uses the part libraries, `array`, `memory`, `discrete` and `standard` located at `c:\memory_design`, define the libraries by adding the following entries in the `cds.lib` file for the project in which you are importing the block:

```
DEFINE array c:\memory_design\array
DEFINE memory c:\memory_design\memory
DEFINE standard c:\memory_design\standard
DEFINE discrete c:\memory_design\discrete
```

OR

Include the `cds.lib` file for the project containing the source block by adding the following entry in the `cds.lib` file for the project in which you are importing the block in System Connectivity Manager:

```
INCLUDE c:\memory_design\cds.lib
```

For more information on the `cds.lib` file, see [The cds.lib File](#) on page 98.

3. Open the project in which you are importing the block in System Connectivity Manager.
4. If the components in the block you are adding refer to library level physical part table (`.ptf`) files, ensure that the library level `.ptf` files are setup for your project in System Connectivity Manager before you import the block. For more information on setting up library level `.ptf` files for your project, see [Setting Up Physical Part Table Files for a Project](#) on page 104.
5. If you have assigned signal integrity (SI) models to components, pins and nets in the block you are importing, ensure that SI libraries containing the models are setup for your project in System Connectivity Manager before you import the block. For more information on setting up SI model libraries in System Connectivity Manager, see [Setting Up SI Model Libraries](#) on page 320.
6. If you are importing a schematic block you created in Allegro Design Entry HDL, perform the steps described in [Adding or Importing Design Entry HDL Blocks in System Connectivity Manager](#) on page 346.

To import a block

1. Open the project in which you are importing the block in System Connectivity Manager.
 2. Choose *File – Import Block*.
- The Import Block: Step 1 dialog box appears.
3. Do one of the following:

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- Select the *Using Project File (*.cpm)* option if you want to import the block from another project (.cpm) file, then enter the name and path to the .cpm file for the project in the *Location* field, or click the browse button to select the .cpm file.

Note: You cannot import a block from the .cpm file for the current project.

- Select the *Using Library File (cds.lib)* option if you want to import the block from the cds.lib file of another project, then enter the name and path to the cds.lib file in the *Location* field, or click the browse button to select the cds.lib file.

4. Click *Next*.

The Import Block: Step 2 dialog box appears.

5. Select the block you want to import.

6. Select the view of the block you want to import.

You can import a spreadsheet view (tbl_1, tbl2 and so on), a schematic view (sch_1, sch_2 and so on), or a Verilog view (vlog_structural) of the block.

7. Do one of the following:

- Select *Read-Only* if you want to import the block as a read-only block.

For more information on read-only blocks, see [Importing as a Read-Only Block](#) on page 398.

- Select *Read-Write* if you want to import the block as a read-write block.

For more information on read-write blocks, see [Importing as a Read-Write Block](#) on page 398.

8. Click *Next*.

The Import Block: Step 3 dialog box appears displaying the details of the block selected for import.

9. Review the messages displayed in the dialog box.

Note the following:

- If a block with the same name is used in the design, the block cannot be imported.
- If a block with the same name exists in the working library for the current project but is not used in the design, System Connectivity Manager will overwrite the existing block with the imported block.

- When you import a block, all its sub-blocks are also imported into your design unless another block with the same name as the sub-block of the block you are importing is already being used in the design.

For example, if you import a block named ANALOG that has a sub-block named RFAMP, the RFAMP sub-block will not be imported along with the ANALOG block if another block named RFAMP is already being used in the design.

10. Click *Finish*.

The imported block is copied to the working library for the current project. You can now add the block in your design.

To add the imported block in your design

1. Do one of the following:

- Choose *Design – Add Component*.
- Click  on the toolbar.

Part Information Manager appears.

2. Click *Browse Libraries*.

3. Select the working library for the project in the *Library* list.

Note: If the imported block is not displayed in the *Cells* list, right-click in the *Library* list and choose *Refresh Lib* to display the imported block in the *Cells* list.

4. Select the block in the *Cells* list and click *Add*.

The Block Packaging Options dialog box appears.

For more information on specifying the packaging options for a block, see [Block Packaging Options](#) on page 687.

5. Specify the packaging options for the block and click *OK*.

System Connectivity Manager automatically packages the block and adds it in the design.

Baselining a Design

In a team design environment, the designer or integrator who has imported a block being developed by another designer as a read-only block needs to be notified when changes are made to the source block so that he can reimport the latest version of the block into his

design. For more information on importing as a read-only block, see [Importing a Block](#) on page 397.

To achieve this, the designer who is working on the source block needs to baseline the block when he wants to notify other designers that the source block has changed. When the source block is baselined, System Connectivity Manager notifies the designers who have imported the block as a read-only block into their designs so that they can reimport the latest version of the block into their design.

Note the following:

- You can baseline a design that is in a modified state. You cannot baseline a design that is already in a baselined state.
A design is said to be in a modified state if it was never baselined, or was modified after the last time you baselined it.
- You cannot baseline a read-only block used in your design.
- If you want to baseline the schematic blocks in your design, ensure that the GENERATE_SCH_METADATA directive in the `cds.cpm` file located at:
`<your_install_dir>\share\cdssetup\projmgr`
is set as shown below:

`GENERATE_SCH_METADATA 'ON'`

To baseline a design

1. Choose *File – Save All* to save all the changes in the design and its sub-blocks.
2. Choose *Design – Baseline Design*.

The Baseline Design dialog box appears displaying the current version of the design.

3. Do one of the following:

- Select the Major option if you want to baseline the design as a major version.

For example, if the current version number is 2 . 0, baselining the design as a major version will bump up the version number to 3 . 0.

You can baseline the design as a major version if you want to notify other designers that significant changes have been made in the design.

- Select the Minor option if you want to baseline the design as a minor version.

For example, if the current version number is 2 . 0, baselining the design as a minor version will bump up the version number to 2 . 1.

You can baseline the design as a minor version if you want to notify other designers that minor changes have been made in the design.

- ❑ Select the Custom option if you want to use a custom version number to baseline the design and enter the version number in the *This design will be baselined as Version* field.

For example, if the current version number of the block is 2 . 0, the next major version will be 3 . 0. However, if you want to specify the next major version as 4 . 0, select the Custom option and enter 4 . 0 in the *This design will be baselined as Version* field.

4. Select the *Use the above information to baseline all sub-blocks* check box if you want to baseline all the sub-blocks in the current design. For more information on how the version number of a sub-block changes, see [How Version Numbers of Sub-Blocks Change When You Baseline a Design](#) on page 687.

Note the following:

- ❑ A sub-block that is in a modified state will be baselined when the top-level design is baselined. However, a sub-block that is already in a baselined state will not be baselined again when the top-level design is baselined.

A sub-block is said to be in a modified state if it was never baselined, or was modified after the last time you baselined it.

- ❑ A sub-block that is a read-only block will not be baselined when the top-level design is baselined.

5. Enter the comments for baselining the design.

6. Click *OK*.

Notifying the Design Team When a Block is Baselined

System Connectivity Manager supports notifying the designer who has imported a block as a read-only block of changes in the source block, when the source block is baselined. You can specify that the designer who has imported a block as a read-only block is notified in one of the following ways:

- When he opens the design containing the read-only block in System Connectivity Manager

- At specific time intervals
- When he runs the *Project – Validate Revisions* command

To specify the options for notifying the design team when a block is baselined

1. Open the design in which a block is imported as a read-only block.
2. Choose *Project – Settings*.
The Setup dialog box appears.
3. Click the Design Verification tab and do one of the following:
 - Select the *Run whenever a design is loaded* check box if you want System Connectivity Manager to report differences in the version of a read-only block imported into your design and the version of its source block when you open the design in System Connectivity Manager.
 - Select the *Run at fixed intervals* check box and select the time interval from the drop-down list, if you want System Connectivity Manager to check at the specified time interval whether the version of the read-only block is the same as the version of its source block and report differences, if any.

When System Connectivity Manager finds differences in the version of a read-only block imported into your design and the version of its source block, the following warning message is displayed in the Violations window:

Local version of block <block_name> is X.X.X. New version X.X.X is available at source.

For example, the warning message:

Local version of block rfamp is 1.2.0. New version 2.0.0 is available at source.

indicates that the block named `rfamp` that you have imported as a read-only block into your design has a version 1.2.0 in the current design and a version 2.0.0 in its source design.

The Hierarchy Viewer also displays the following icons next to the name of the block when System Connectivity Manager finds differences in the version of a read-only block imported into your design and the version of its source block.



This icon indicates that the version of the spreadsheet block has changed in its source location.



This icon indicates that the version of the schematic block has changed in its source location.



This icon indicates that the version of the Verilog block has changed in its source location.

You need to reimport the read-only block into your design if you want to access the latest changes in the block. For more information see, [Reimporting a Read-Only Block](#).

Reimporting a Read-Only Block

When System Connectivity Manager reports differences in the version of a read-only block imported into your design and the version of its source block, you need to reimport the read-only block into your design if you want to access the latest changes in the block.

To reimport a read-only block you have imported into your design

- Select the read-only block in the Hierarchy Viewer, right-click and choose *Re-import Block*.

Updating the Source Location of a Read-Only Block

The designer who is working on the block you have imported into your design as a read-only block might move the design containing the source block for the read-only block to a new location. If the location of the source block for a read-only block changes, Hierarchy Viewer displays the icon next to the name of the block, when you do one of the following:

- Open the design in which you have imported the read-only block in System Connectivity Manager.
- Select the Run at fixed intervals check box in the Design Verification tab of the Setup dialog box.

You can specify the new location for the source block for the read-only block by doing the following:

1. Select the read-only block in the Hierarchy Viewer, right-click and choose *Update Block Source*.

The Update Block Location dialog box appears.

2. Select the new location for the source block for the read-only block by doing one of the following:

- Select the *Using Project File (*.cpm)* option if you want to specify the location of the source block from another project (.cpm) file, then enter the name and path to the .cpm file for the other project in the *Location* field or click the browse button to select the .cpm file.
- Select the *Using Library File (cds.lib)* option if you want to specify the location of the source block from another cds.lib file, then enter the name and path to the cds.lib file in the *Location* field or click the browse button to select the cds.lib file.

3. Clock OK.

The location of the source block for the read-only block is set to the new location.

Updating Components Modified by the Librarian

During the design cycle, the components used in the design might be modified by the Librarian. The designers need to be notified when a component is modified and be able to update all the instances of the component used in the design with the modified version, on a need basis.

The Part Developer tool allows the Librarian to baseline components that are modified. For more information on baselining components in Part Developer, see the *Part Logging and Versioning* chapter of the *Part Developer User Guide*.

If a component used in a design is modified by the Librarian, pin mismatch packaging errors are displayed in the Violations window when you open the design in System Connectivity Manager, if there is any mismatch between the pins of a component in the design and the pins defined in the chips.prt file of the component. Click the *Resolve* button in the Violations window to update such components.

Note the following:

- The Violations window reports errors for every instance of the component that has pin mismatch packaging errors. However, when you click the *Resolve* button next to the error for one instance, all the instances of the component that exist in the block in which the instance exists are updated. If the error is reported for an instance of the same

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component in another block, you must click the *Resolve* button next to the error reported for the instance in that block to update all instances of the component in that block.

For example, if pin mismatch packaging errors are reported for instances `i1` and `i8` of the `ls04` component in the `memory` block and for instances `i33` and `i36` of the `ls04` component in the `cache` block, do the following:

- Click the *Resolve* button next to the error reported for instance `i1` or `i8` to update both the instances in the `memory` block.
- Click the *Resolve* button next to the error reported for instance `i33` or `i36` to update both the instances in the `cache` block.
- You cannot use the Violations window to automatically update associated components such as terminations, bypass capacitors, and pullups and pulldowns that have pin mismatch packaging errors. You must manually modify the associated components in the design. For more information on working with associated components, see [Chapter 11, “Working with Associated Components.”](#)
- If you do not resolve the pin mismatch packaging errors in the Violations window, the components that have pin mismatch errors are displayed in the Cell Revision Manager dialog box. You can update the components using the Cell Revision Manager dialog box. For more information, see [Using the Cell Revision Manager to Update Modified Components in the Design](#) on page 408.
- The Violations window does not report changes that are automatically resolved by the tool. For example, consider a design that instantiates a component with pin names `add1` and `add2`. The corresponding pin numbers are 1 and 2, respectively. Now edit the component in Part Developer and swap pins such that pin `add1` now maps to pin number 2 and pin `add2` maps to pin number 1. If you now open the design that instantiates the modified component, no message is displayed but the details in the Component Connectivity Details are updated.

If changes are made to the symbol or properties of a component, System Connectivity Manager displays the Cell Revision Manager dialog box when you choose *Project – Validate Revisions* in SCM. You must use the Cell Revision Manager dialog box to update all the instances of the component used in the design with the latest version of the component.

Note the following:

- Not updating all the instances of a component with its latest version can result in packaging errors in the design.
- You cannot use the Cell Revision Manager dialog box to automatically update associated components such as terminations, bypass capacitors, and pullups and pulldowns in the design. You must manually modify the associated components in the design. For more

information on working with associated components, see [Chapter 11, “Working with Associated Components.”](#)

- You cannot update modified components in the schematic and read-only blocks used in your design.
 - Open the schematic block in Design Entry HDL by editing the schematic block in master mode and update the modified components using the Component Revision Manager in Design Entry HDL. For more information on editing blocks in master mode, see [Editing a Hierarchical Design](#) on page 356.
 - Request the owner of the read-only block to update the modified components in the block and then reimport the read-only block into your design. For more information on reimporting read-only blocks, see [Reimporting a Read-Only Block](#) on page 405.

Using the Cell Revision Manager to Update Modified Components in the Design

1. Before updating components, you must setup the options for replacing components in the [Component Replace](#) tab of the [Setup](#) dialog box. This is because, when you update a modified component in the design, System Connectivity Manager replaces all the instances of the component used in the design with the latest version of the component.
2. Choose *Project – Validate Revisions*.

SCM displays the Cell Revision Manager dialog box if it finds any differences between the version of a component used in the design and the version of the component in the component library. The Cell Revision Manager displays the list of components used in the design that have been baselined by the Librarian.

To view the list of instances of a component in the design, select a component and click the *Details* button.

3. Select the *Update* check box next to a component to update all the instances of the component used in the design with the latest version of the component.

Note: You can only update all the instances of the component used in the design with the latest version of the component. You cannot update specific instances of a component used in the design with the latest version of the component.

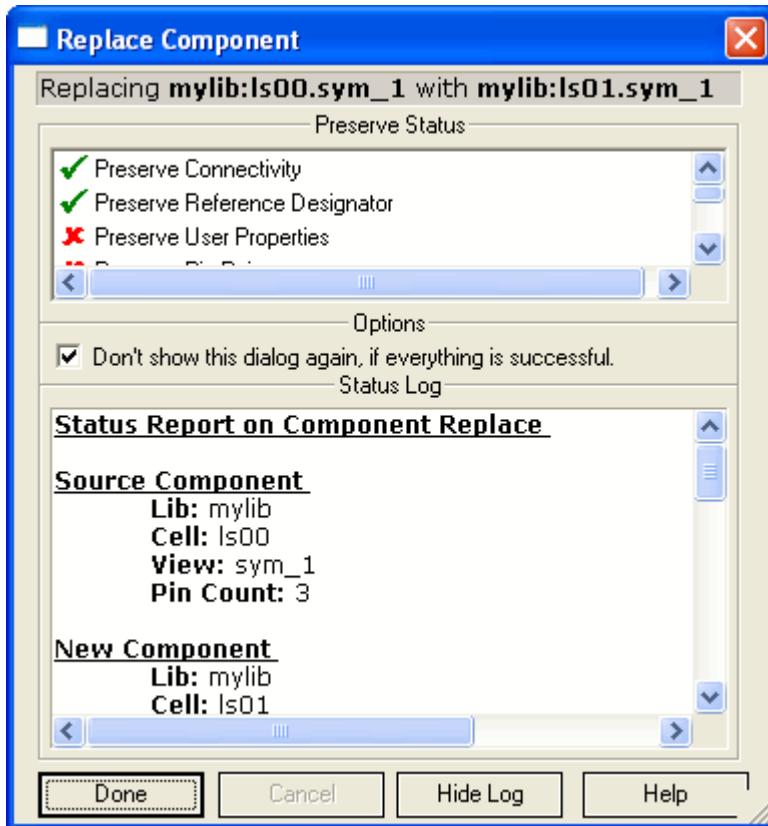
4. Click *OK*.

- If there is no mismatch in the pin names and pin numbers of the version of the component in the design and baselined component, the [Replace Component](#) dialog box appears displaying whether the component replace preserve options you

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selected in the Component Replace tab of the Setup dialog box will be honored when you update the component. Click *Done* to replace the component.



- If there is a mismatch in the pin names or pin numbers of the version of the component in the design and baselined component, the Component Replace dialog box appears.
 - a. Resolve the connectivity and property differences between the version of the component in the design and the baselined component.

For more information on using the Component Replace dialog box, see [Using the Component Replace Dialog Box](#) on page 113.

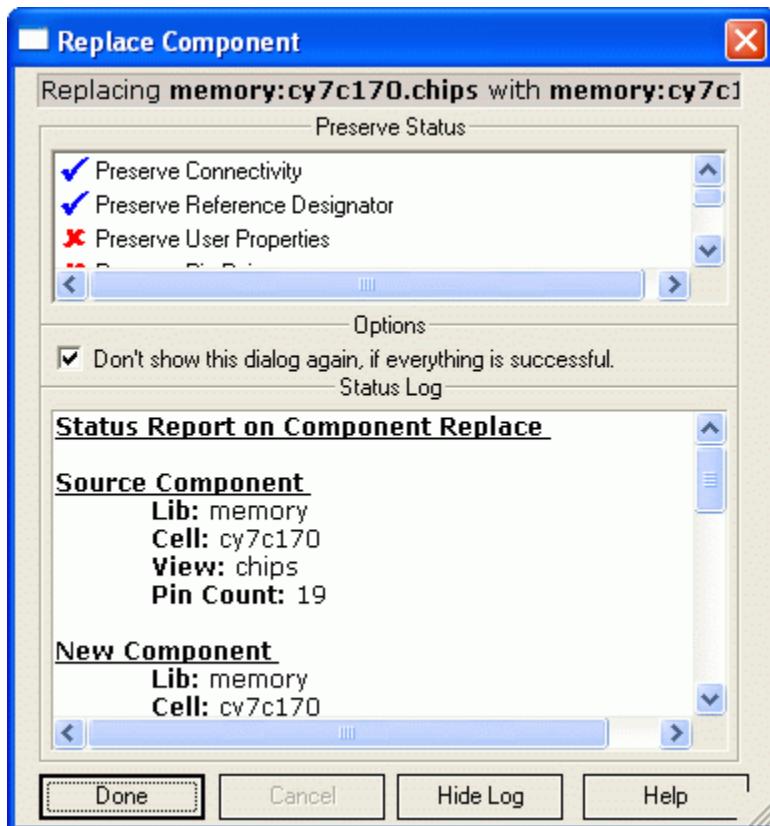
- b. Click *Replace* to update all the instances of the component used in the design with the latest version of the component.

Note: Click *Cancel* if you do not want to update all the instances of the component used in the design with the latest version of the component.

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The Replace Component dialog box appears. This dialog box displays whether the component replace preserve options you selected in the Component Replace tab of the Setup dialog box will be honored when you replace the component.



- c. Click *Done*.

Note the following:

- The Component Replace dialog box appears once for each modified component you are updating in the design. So you must perform step a to step c for each modified component you are updating in the design. For example, if you selected the Update check box next to two components in the Cell Revision Manager dialog box, the Component Replace dialog box appears twice.
- If you have added a component as a symbol and also as a package, the Component Replace dialog box appears once for updating the instances of the component added as a symbol and once for updating the instances of the component added as a package. For more information on adding components in the design, see Adding Components on page 107.

- The pins of the target component will not be displayed in the Component Replace dialog box if the primitive is deleted from the `chips.prt` file or if the part table row for the primitive is modified in the physical part table file (`.ppt`) for the component.

Viewing the Version History of Blocks and Components

You can view the version history of blocks and components used in your design.

To view the version history of the current block

- Choose *Design – Version History*.

The Revision History dialog box appears displaying the version history of the current block.

To view the version history of any block

1. Select the block in the Hierarchy Viewer or the Component List.
2. Right-click and choose *Version History*.

The Revision History dialog box appears displaying the version history of the selected block.

To view the version history of a component

1. Select the component in the Hierarchy Viewer or the Component List.
2. Right-click and choose *Version History*.

The Revision History dialog box appears displaying the version history of the selected component.

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Designing System-in-Package



The contents of this chapter are valid if you are using System Connectivity Manager, with one of the following licenses.

- SIP Digital Architect GXL
- SIP Digital Architect XL

Overview

Design challenges, such as increase in design complexity, reduction in cycle time, and reduction in the physical size of high functionality systems have led to an increase in the use of System-in-Packages. A System-in-Package (SiP) is a system design fabric that enables you to add multiple dies in a single package. Using System Connectivity Manager, you can design SiPs by adding standard dies as well as co-design dies. System Connectivity Manager also provides support for adding RF or analog dies to a SiP.

An important feature of the Cadence SiP solution is that it provides support for concurrent designing. This is implemented in form of co-design objects. Co-design objects are the dies that are under development. These objects are simultaneously designed in one fabric and implemented in another. In the Cadence Digital SiP flow, the logical design and the connectivity of a co-design object is captured in System Connectivity Manager, where as the physical implementation of the co-design die is simultaneously designed in SiP Layout and IO/Planner.

The Digital SiP solution provided by Cadence, uses System Connectivity Manager as a tool to capture connectivity between different components of the system, quickly and efficiently. SCM also provides designers with the capability of importing Verilog netlists for the bare dies, which are an important part of any System-in-Package (SiP).

While designing a System-in-Package, System Connectivity Manager is used in the following scenarios.

- During the SiP design process, to capture interconnectivity between the components of SiP
- While designing a PCB that instantiates the SiP package as a component on the actual board.
- For capturing the logical design of a SiP
- For adding associated components

This chapter focuses only on the flows and design tasks that are performed in SCM during the SiP design process. For a complete overview of the SiP solutions provided by Cadence, it is recommended that prior to reading this chapter, you go through the book, [Cadence SiP Design Solution Overview](#).

Co-Designing Using Cadence Tools

System Connectivity Manager features, such as the ability to capture designs as spreadsheets, schematic, and Verilog blocks, and the support provided for co-design objects, make it an ideal tool for capturing designs in a distributed design environment. As System Connectivity Manager has the required infrastructure to support development of designs across domains and across technologies, it is the one of the main products in the Cadence SiP Digital Architect flow.

The SiP Digital Architect flow provided by Cadence focuses on the design challenges of integrating multiple, large, high pin count chips onto a single substrate. This flow targets the major challenges of System-in-Package (SiP) in terms of connectivity definition and management, physical concept prototyping of the SiP floorplan, including multi-chip die stacks, and die I/O planning to optimize and minimize substrate connectivity routing and signal integrity challenges.

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An example of how Cadence products can be used to implement co-design flow is shown in the figure given below. The task-level details of a co-design flow are covered later in the book.

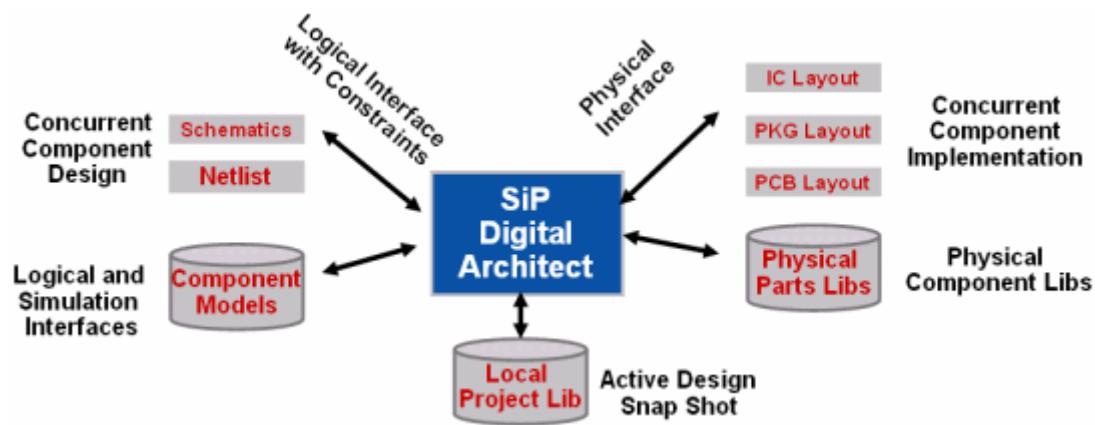


Figure 16-1 Co-Designing across Cadence products

Introduction to SiP Design Flows

Cadence Design Systems uses concurrent design and co-design methodology to define the SiP design flows. The SiP design flows that use System Connectivity Manager as a tool to capture system connectivity are listed below.

- [SiP Physical Co-Design Flow](#)
- [SiP Logical Co-Design Flow](#)
- [PCB-Driven SiP Co-Design Flow](#)

These flows are useful when you are designing a PCB, that instantiates a SiP, which is still being developed. The SiP in turn, is a package that may have single or multiple dies. In case the SiP has multiple dies, some of the dies will be standard dies that are already in the production, while some dies can be co-design dies, that are still being designed and can therefore, influence the package design.

SiP design flows supported by Cadence are based on the assumption that SiP design process involves concurrent design efforts between a PCB user, the SiP (or IC-PKG co-design) user, and an Encounter user as depicted in [Figure 16-2](#) on page 416.

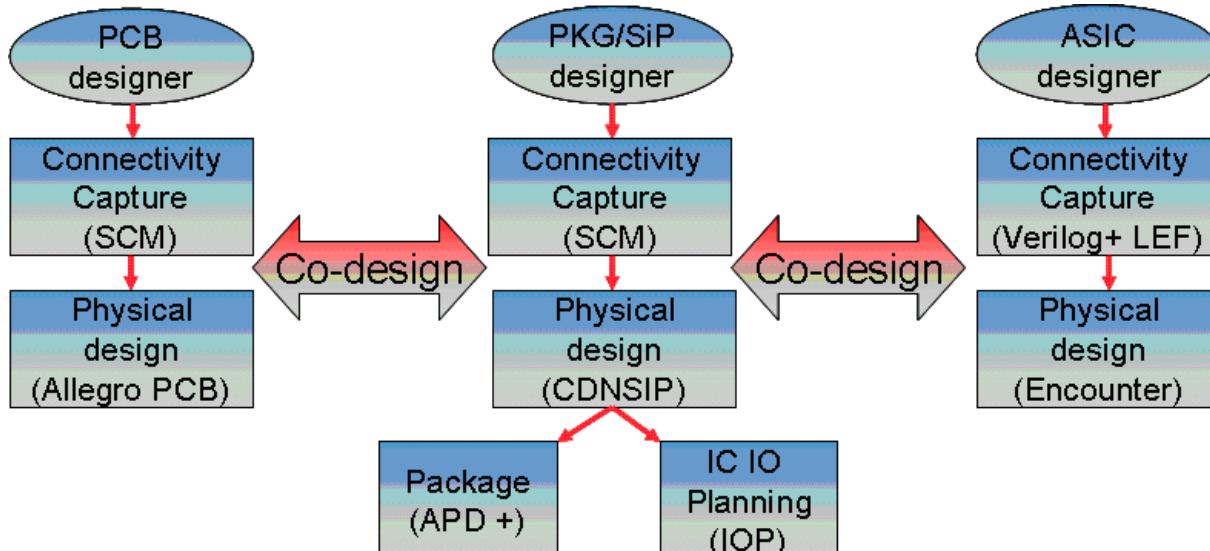


Figure 16-2 Concurrent designing

SiP Physical Co-Design Flow

This is an IC — PKG — PCB co-design flow. In this flow, the physical co-design object, based on the IC abstract generated using Encounter platform, is added to the design in SiP Layout.

When to use

In case of SiP Physical Co-Design flow, the co-design die is instantiated in the SiP Layout and System Connectivity Manager is used to define the connectivity between the dies instantiated in SiP. If required, the connectivity between the bare co-design die and the SiP package can also be captured using System Connectivity Manager. This is an IC driven flow, where the physical information about the co-design die is generated in Encounter, and then exported to package.

Table 16-1 Design Tasks in Physical Co-Design Flow

Steps	Tasks/Actions	Comments
Step 1: Create a project in System Connectivity Manager.	<ol style="list-style-type: none">1. Choose <i>File – New – Project</i>.2. If required, add standard die components to the SiP design.	This step is required to ensure that at any point in the flow, the logical design in SCM can easily be updated with all the modifications made to the physical SiP design in SiP Layout. For details on how to create a project in System Connectivity Manager, see Creating Design Projects on page 82.
Step 2 Generate a board file for the project.	<ol style="list-style-type: none">1. Choose <i>Project – Export Physical – SiP Package</i>.	A .sip file is generated.

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Table 16-1 Design Tasks in Physical Co-Design Flow, *continued*

Steps	Tasks/Actions	Comments
Step 3	<p>Open the .sip file in SiP Layout.</p> <p>To Launch SiP Layout:</p> <ul style="list-style-type: none"> ■ On Windows, choose <i>Start – Programs – Cadence SPB 17.x –SiP</i> ■ From the command line, type <code>cdnsip &</code> and press Enter. 	
Step 4	<p>Add components to the SiP Design.</p> <p>Add design components, including bare dies.</p> <ul style="list-style-type: none"> ■ If the standard DIE data is in text format, choose <i>Add – Standard DIE – DIE Text-In Wizard</i>. 	<p>The actual design tasks start here. Depending on format in which the DIE data is available, different commands are used to add an instance of the bare DIE or a co-design DIE.</p> <p>For more information on procedures used for creating a co-design die, see the section on add codesign die in <u>Allegro PCB and Package Physical Layout Command Reference: A Commands</u></p>
Step 5	<p>Add a co-design die to the design</p> <ol style="list-style-type: none"> 1. Setup LEF libraries. 2. To add a co-design DIE, choose <i>Add – Co-Design Die</i>. 	<p>The data for the co-design die, which is still being designed by an IC designer, can either be a LEF/DEF format or can be a OA database file. In both the situations, the LEF libraries must be set up before a co-design die is added.</p>

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Table 16-1 Design Tasks in Physical Co-Design Flow, *continued*

Steps	Tasks/Actions	Comments
Step 6	<p>Specify bump patterns for the co-design die in I/O Planner.</p> <p>IO placement steps including the generation of the bump pattern for flip-chip.</p> <p>Using I/O Planner, you can specify:</p> <ul style="list-style-type: none"> <input type="checkbox"/> bump matrix <input type="checkbox"/> I/O pad ring/ array through connectivity assignment <input type="checkbox"/> I/O placement <input type="checkbox"/> redistribution layer (RDL) routing. 	<p>The Cadence I/O Planner (IOP) is an IC layout tool that is launched automatically when you create or edit a co-design die. Using this tool, you can actively plan the die down to the I/O buffer level, concurrently with the package design in which it will be placed.</p> <p>For detailed information on the Cadence I/O Planner, see <u>Cadence® I/O Planner: Application Note</u> (available at <code><install_dir>/doc/IOPlanner/IOPlanner.pdf</code>).</p>
Step 7	Place the co-design die in SiP Layout	You can also refer to the First Encounter documentation.
Step 8	Save the design without modifying the connectivity and exit SiP Layout	<p>For detailed information, see the chapter on <i>Generating Co-Design Die (APD XL)</i> in the <i>Allegro Package Designer User Guide: Placing the Elements</i>.</p> <p>1. Choose <i>File – Save</i></p> <p>2. Choose <i>File – Exit</i></p> <p>If you are using SCM to capture connectivity, it is recommended that initial connectivity must be captured in SCM.</p>

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Table 16-1 Design Tasks in Physical Co-Design Flow, *continued*

Steps	Tasks/Actions	Comments
Step 9	Update the logical design with the changes in the SiP Layout.	<ol style="list-style-type: none"> 1. Choose <i>Project – Import Physical</i> to view the modifications. 2. Update the design will all or selected changes.
Step 10	Capture connectivity between dies in SCM	
Step 11	Add user-defined power and ground ports to the co-design die.	<p>This is an optional step in the SiP design process.</p> <p>For detailed procedure, see <u>Adding User-Defined Pins on a Co-Design Die</u> on page 437.</p>
Step 12	Synchronize the physical design with the changes in the logical design	Choose <i>Project – Export Physical</i> .
Step 13	Capture the connectivity of the dies to the SiP Package	Though the connectivity of a bare die to the SiP Package is usually captured in SiP Layout, if required this connectivity can also be captured in System Connectivity Manager.

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Table 16-1 Design Tasks in Physical Co-Design Flow, *continued*

Steps	Tasks/Actions	Comments
Step 14 Design modifications	If required, make changes to the design in SiP Layout or in I/O Planner.	<p>After making any modification make to the plan of the co-design die in IO Planner, you should update the package and then exit IOP. This ensures that the co-design die in SiP Layout is also updated.</p> <p>Note: Using IO Planner, you can add or delete physical pins to the co-design dies. However, adding or deleting IC pins (logical pins) is not recommended. This is because modifying logical pins in IO Planner causes the Verilog file for the co-design die in SCM to go out of sync with the Verilog file in SiP Layout and IO Planner. You can only move the existing IC pins in IO Planner.</p> <p>Using Import Physical command from SCM, updates the logical SiP design with the changes made in IOP.</p>
Step 16 Synchronize the logical design with the changes in the physical design	In SCM, choose <i>Project – Import Physical</i> .	Based on the modifications made to the logical or the physical design, <u>Step 12</u> and <u>Step 16</u> might have to be repeated multiple times before the SiP design is finalized.

SiP Logical Co-Design Flow

In this flow, the complete logical design for SiP is captured in System Connectivity Manager.

When to use

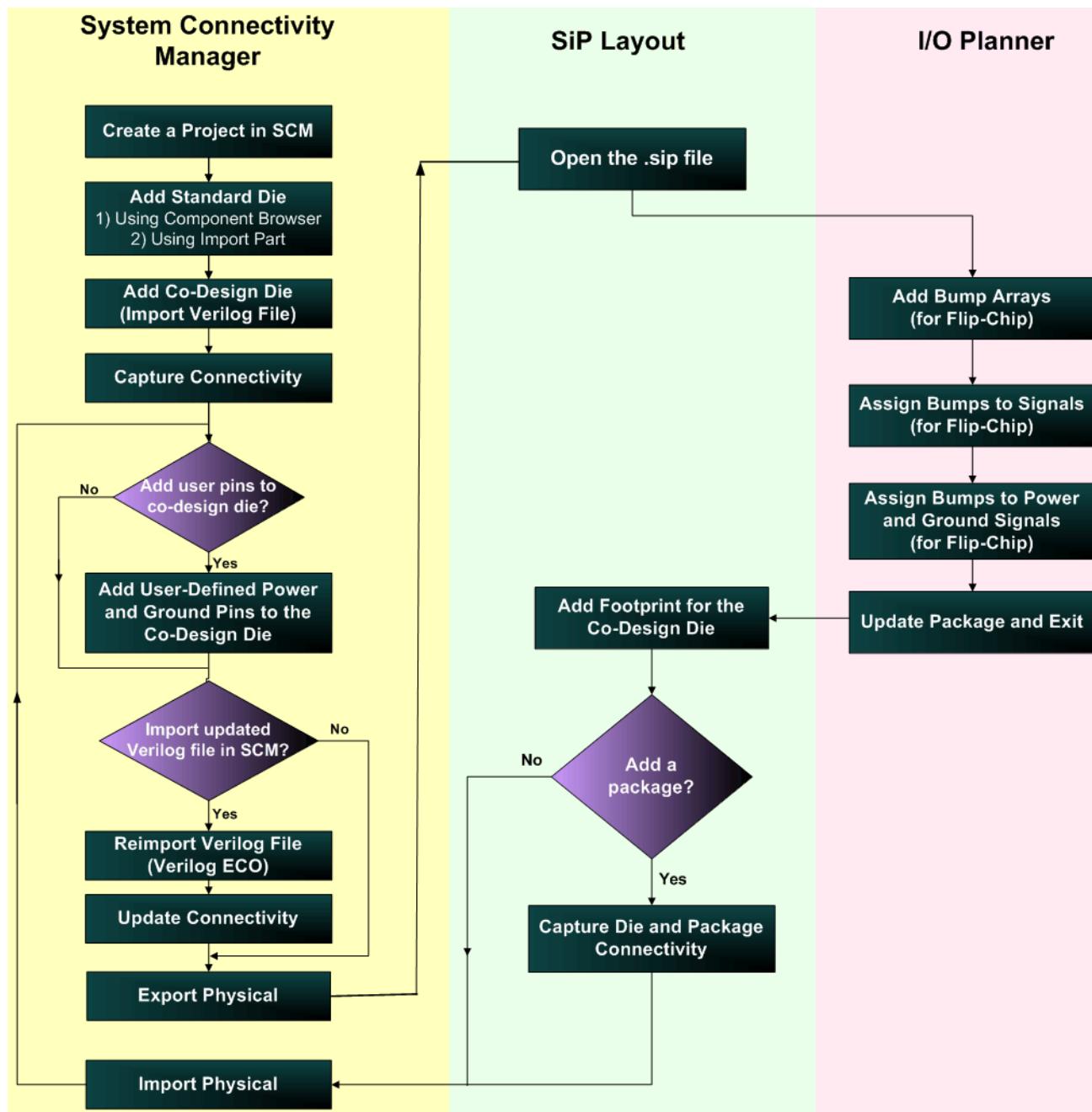
In this flow, the complete logical design of a SiP — including the co-design object and the connectivity — is first captured in System Connectivity Manager. After initial connectivity is specified, the design data is sent to SiP Layout and IO/Planner for package designing. This flow uses the logical ECO capabilities of SCM. Therefore, changes in the Verilog netlist used for creating the co-design die, can be imported in SCM as Verilog ECOs.

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Table 16-2 on page 424 lists the steps that are to be performed if you use System Connectivity Manager as the tool for capturing the logical SiP design.

Figure 16-3 SiP Logical Co-Design Flow with Verilog ECO



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Table 16-2 Design Tasks in SiP Logical Co-Design Flow

Step	Tasks/Actions	Comments
Step 1	Create a project in System Connectivity Manager	For information on how to create projects in SCM, see Creating Design Projects on page 82.
Step 2	Create a table block in SCM for the SiP	This is a Cadence recommended best practise.
		The advantage of this approach is that it is easier to export the interface data of the SiP to the PCB Designer, who is using this SiP as a component in the PCB.
		For example, in the figure shown below, the hierarchical block, <code>siplogic</code> , should be used to capture the SiP design.
		
Step 3	Add standard die	Use Component Browser to add standard dies from the libraries included in the project.
		For details on how to instantiate components, see Working with Components on page 107.

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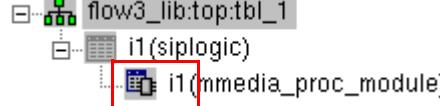
Table 16-2 Design Tasks in SiP Logical Co-Design Flow, *continued*

Step	Tasks/Actions	Comments
Step 4	<p>Import die data in SCM</p> <p>To create a part by importing die text:</p> <ol style="list-style-type: none">1. Choose <i>File – Import Part</i>.2. In the Import and Export wizard, choose <i>Import Die Text</i> and follow the instructions in the subsequent pages of the wizard. <p>To create a part by importing footprint data:</p> <ol style="list-style-type: none">1. Choose <i>File – Import Part</i>.2. In the Import and Export wizard, choose <i>Import Allegro Footprint</i> and follow the instructions in the subsequent pages of the wizard. <p>Using Component Browser, add an instance of the table block — representing the die — to the design.</p>	<p>SCM provides support for importing die data captured in the text format. To instantiate standard dies in SCM, you can create a part either by importing the footprint data or by importing the die text file. Any modifications to the die text data or the footprint data can also be incorporated by importing changes as ECOs.</p> <p>For more information, see the <u>Chapter 23, “Creating Parts from External Data Files.”</u></p>

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Table 16-2 Design Tasks in SiP Logical Co-Design Flow, *continued*

Step	Tasks/Actions	Comments
Step 5 Create co-design die	<ol style="list-style-type: none"> 1. Choose <i>Project – Import – Verilog – Netlist</i>. 2. After the specified Verilog module is imported as a table block, use Component Browser to add an instance of the table block to the design. 3. In the Hierarchy Viewer, right-click on the table block representing the co-design die. 4. Choose <i>Mark As Co-Design</i> 	<p>A co-design die is a die that is still being developed. This implies that there is a possibility that the die interface may change during the SiP design process.</p> <p>For information on importing a verilog file as a table block, see Importing a Verilog File in System Connectivity Manager on page 436.</p> <p>When you mark a table block as a co-design block, the icon associated with the block changes, and the block is also assigned a reference designator value.</p> 

For step-by-step information on creating a co-design die in SCM, see [Creating a Co-Design Block](#) on page 437.

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Table 16-2 Design Tasks in SiP Logical Co-Design Flow, *continued*

Step	Tasks/Actions	Comments
Step 6	<p>Add user-defined ports to the co-design die</p> <ol style="list-style-type: none"> 1. In the Component List pane, right-click on the co-design die. 2. Choose <i>Edit User Pins</i> 	<p>This is an optional step in design process, and need not be performed in all scenarios.</p> <p>In a design environment, this step is required if you want to add power and ground pins to the co-design die.</p> <p>To know more about adding user-defined pins, see the section on Adding User-Defined Pins on a Co-Design Die on page 437.</p>
Step 7	<p>Capture connectivity</p> <ol style="list-style-type: none"> 1. Capture connectivity between the dies instantiated in the design. 2. If required, add associated components. 	<p>To know about capturing design connectivity, see Chapter 6, “Capturing Connectivity.”</p>
Step 8	<p>Importing Changes in the Verilog File</p> <p>Choose <i>Project – Import – Verilog – ECO</i>.</p>	<p>To know how to add associated components, see the chapter on Chapter 11, “Working with Associated Components.”</p> <p>This is an optional step in the design flow and is required only if the Verilog file that was imported in SCM in Step 5 gets modified.</p>
Step 9	<p>Create a physical layout for the SiP</p> <p>Choose <i>Project – Export Physical – SiP Package</i>.</p>	<p>The changes are imported as Verilog ECO.</p> <p>Ensure that the <i>Update Layout (Netrev)</i> check box is selected in the Export Physical dialog box.</p>

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Table 16-2 Design Tasks in SiP Logical Co-Design Flow, *continued*

Step	Tasks/Actions	Comments
Step 10 Open the physical layout in SiP Layout	To launch SiP Layout: <ul style="list-style-type: none">■ In Windows, choose <i>Start – Programs – Cadence SPB 17.x – SiP</i>■ From command line, type <code>cdnsip &</code> and press Enter.	
Step 11 Generate footprint for the co-design DIE	Choose <i>Edit – Co-Design Die</i>	To instantiate a co-design die in SiP Layout, you first generate the package data. The packaging information for a bare die is generated using Cadence IO Planner.

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Table 16-2 Design Tasks in SiP Logical Co-Design Flow, *continued*

Step	Tasks/Actions	Comments
Step 12 Modify the co-design die in IO Planner	<p>Tasks performed in the IO Planner are:</p> <ul style="list-style-type: none"> ■ Bump Array Creation ■ Bump Assignment ■ RDL Routing ■ Manual Wire Editing <p>Choose <i>File – Update Package</i> and exit IO Planner.</p>	<p>In this step, you assign bump matrix to all the logical pins in the co-design die.</p> <p>Note: Using IO Planner, you can add or delete physical pins to the co-design dies. However, adding or deleting IC pins (logical pins) is not supported. You can only move the existing IC pins in IO Planner. This is because modifying logical pins in IO Planner causes the Verilog file for the co-design die in SCM to go out of sync with the Verilog file in SiP Layout and IO Planner.</p>
Step 13 Update the design in SiP Layout		<p>This adds the footprint information of the co-design die to SiP Layout.</p> <p>For detailed information on the Cadence I/O Planner, see <u>Cadence® I/O Planner: Application Note</u> (available at <install_dir>/doc/IOPlanner/IOPlanner.pdf).</p> <p>You can also refer to the First Encounter documentation.</p>

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Table 16-2 Design Tasks in SiP Logical Co-Design Flow, *continued*

Step	Tasks/Actions	Comments
Step 14 Update the design in SCM with the changes in the SiP Layout.	<ol style="list-style-type: none"> 1. Choose <i>Project – Import Physical</i> to view the modifications. 2. Update the design will all or selected changes. 	<p>This step is must because the pin numbers of the co-design die change as a result of Step 12.</p> <p>The modified pin numbers are displayed in SCM as shown in Figure 16-4.</p>

Figure 16-4

	Pin Name ▲	Pin Number	Pin Type	PINUSE	Signal
	VDD VSS*	*	*	*	*
475		VDD	BUMP_266_5_10,BUMP...	Input	oooooooooooo,V
618		VSS	BUMP_272_11_10,BUM...	Input	VSS
619	VSS	BUMP_272_11_10	Input	GROUND	VSS
620	VSS	BUMP_273_12_10	Input	GROUND	VSS
621	VSS	BUMP_274_13_10	Input	GROUND	VSS
622	VSS	BUMP_275_14_10	Input	GROUND	VSS
623	VSS	BUMP_276_15_10	Input	GROUND	VSS

Note that power and ground pins — multiple pins with same pin name — are concatenated together and are displayed as a single entry in CCP in collapsed format. To view the individual pins, expand the pins by clicking on the button.

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Table 16-2 Design Tasks in SiP Logical Co-Design Flow, continued

Step	Tasks/Actions	Comments
Step 15 Design modification	<p>After the logical and physical SiP designs are synchronized, there might be changes made to the logical design in SCM. These changes are mainly because of the following reasons.</p> <ul style="list-style-type: none"> ■ Verilog ECO Choose <i>Project – Import – Verilog – ECO</i>. ■ Changes in the pin definition of the co-design die. (Changes in the Edit User Pins dialog box) ■ Connectivity changes 	<p>Verilog ECO is performed when the Verilog file imported in SCM in Step 5, is modified because of the changes in the die design.</p> <p> <i>Important</i></p> <p>All logical modifications to the die must be done through Verilog ECO in SCM.</p> <p>Modifications such as adding, deleting, or moving IC pads, is only supported as Verilog ECOs imported in SCM.</p>
Step 16 Update SiP Layout design		<p> <i>Caution</i></p> <p><i>Changes such as adding, deleting, and moving IC bumps/pads are supported only through IO Planner.</i></p> <p>In SiP Layout, modifications, such as swapping IC bumps (for flipchip only), can be made to the co-design die.</p>

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Table 16-2 Design Tasks in SiP Logical Co-Design Flow, *continued*

Step	Tasks/Actions	Comments
Step 17 Synchronize the physical design with the changes in the logical design		Based on the modifications made to the logical or the physical design, Step 14 and Step 17 might have to be repeated multiple times before the SiP design is finalized.

PCB-Driven SiP Co-Design Flow

PCB — PKG — IC co-design flow using System Connectivity Manager co-design object in the PCB with ability to drive connectivity from PCB to SiP.

When to use

PCB Driven SiP co-design flow is used when the co-design SiP is instantiated as a component in the PCB. In this flow, the interface data is shared between the PCB and the co-design SiP in XML format. The steps in the design flow depend on who defines the initial pinout for SiP — PCB designer or the SiP designer. Changes in the SiP interface can be

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driven from PCB as well as from SiP. In the PCB driven SiP co-design flow, most of the SiP and PCB design tasks are done in parallel.

Table 16-3 Steps in the PCB Driven SiP-Co-Design Flow

SiP Design Tasks	PCB Design Tasks
1. Create a project in System Connectivity Manager, to capture the logical design for SiP.	Create a project in System Connectivity Manager, to capture the logical design for PCB.
2. Create a table block to represent the logical design for the SiP (Cadence recommended best practise)	Add standard components.
3. Ignore this step if initial pinout for the co-design SiP is not specified by PCB designer. ■ add a co-design block by importing interface data. For details, see Importing Interfaces in a Design on page 448.	■ create/instantiate a co-design block (for the SiP) in your design. ■ Export SiP interfaces. For details, see Exporting Interface Data on page 447.
4. Ignore this step if initial pinout for the co-design SiP is not specified by SiP designer: ■ Instantiate components and capture connectivity. The components added to the SiP design can be Of-The-Shelf components or the Known-Good-Dies to be included in the SiP. ■ <i>Export the SiP Interface data.</i> For details, see Exporting Interface Data on page 447.	If initial pinout is specified by SiP designer, add a co-design block by importing interface data. For details, see Importing Interfaces in a Design on page 448.
5.	Specify interconnectivity between SiP interfaces and the other components in the PCB design.

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Table 16-3 Steps in the PCB Driven SiP-Co-Design Flow, *continued*

SiP Design Tasks	PCB Design Tasks
<p>6. Export the design to generate the physical netlist for the SiP in Cadence SiP Digital Layout.</p> <p>For this, choose <i>Project – Export Physical – SiP Package</i>.</p> <p>For details, see Generating a Physical Netlist for SiP on page 451</p>	<p>Create the layout for PCB board in ALLEGRO PCB Editor. To do this, choose <i>Project – Export Physical – PCB Board</i>.</p>
<p>7. Create the physical layout for SiP in the SiP Layout.</p> <p>If the SiP design uses any co-design die, follow the steps listed in the SiP Physical Co-Design Flow on page 417.</p>	
<p>8. During the design process, if any changes are made to the SiP interface data, export the latest interface data so that the PCB design can be updated.</p> <p>To export the interface data, choose <i>Design – Export Interface</i> and follow the procedure Exporting Interface Data on page 447.</p>	<p>During the design process, if any changes are made to the SiP interface data, export the latest interface data so that the SiP design can be updated.</p> <p>To export the interface data, choose <i>Design – Export Interface</i> and follow the procedure Exporting Interface Data on page 447.</p>
<p>9. All further changes in the SiP interface are treated as ECOs.</p> <p>For details, see Importing Interface ECO Data on page 450.</p>	

Importing a Verilog File in System Connectivity Manager

You can create the logical implementation of a co-design block by importing the interface data from an existing Verilog file in System Connectivity Manager.

To create interface data from an existing Verilog file, perform the following steps:

1. Choose *Project – Import – Verilog – Netlist*.
2. In the Import Verilog dialog box, specify the path to the verilog file.
3. Select the library where you want to save the part created using the Verilog file.
4. To populate the Module Name list with the list of verilog modules in the specified verilog file, click the *Get* button.
5. From the Module Name drop-down list, select the verilog module name to be imported in System Connectivity Manager.
6. Click *OK*.
7. Parse the messages displayed in multiple message boxes.

The logical block is imported in the specified library.



Important
When you import a Verilog file as a block in System Connectivity Manager, a new cell is created in the library specified in [step 3](#). The cell has two views, `tbl_1` and `vlog_structural`. The `vlog_structural` view is used for simulating the co-design block.

8. Using Component Browser, add an instance of the imported module to the design.



Caution
The import process will fail if the library in which you are trying to import a Verilog module, already has a component or block with the same name as that of Verilog module.

Creating a Co-Design Block

While creating a SiP design in System Connectivity Manager, you can mark a block — representing a die that is still being developed — as a co-design block.

The steps for creating a co-design block in System Connectivity Manager are as listed below.

1. Import a Verilog file in System Connectivity Manager as a table block.

For detailed procedure, see [Importing a Verilog File in System Connectivity Manager](#) on page 436.

2. In the Hierarchy Viewer, right-click on the block and choose *Mark As Co-Design*.
3. If required, specify the power and ground pins on the co-design die and click *OK*.

A new co-design block is created.



Caution

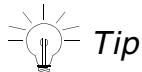
Mark As Co-Design option is not enabled if the design has more than one instance of the table block being marked as co-design object. It is also recommended that you should not have multiple instances of a co-design object in your design. This might cause problems in the flow.

When you mark an existing block as a co-design block, following changes are made to the design.

- The table icon associated with the block changes to the icon for the co-design block
- When you mark a block as a co-design block, System Connectivity Manager treats the block as a primitive. As a result in the component list pane, a reference designator is assigned to the co-design block.
- For a co-design block, instead of pin names, port names are listed in the Component Connectivity Details pane.
- The VERILOG_PORT_NAME property is attached to all the interface ports on the block.

Adding User-Defined Pins on a Co-Design Die

If a co-design die is added to the design in SiP Layout, and you update the logical design using the *Import Physical* command, System Connectivity Manager identifies the co-design die and instantiates it in the logical design as a co-design object.



Tip

In System Connectivity Manager, a co-design block is indicated using the following icon:

If required, you can modify the co-design object by adding user-defined ports on it. Using the System Connectivity Manager interface, you can add or delete user-defined pins on co-design objects.

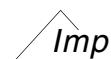
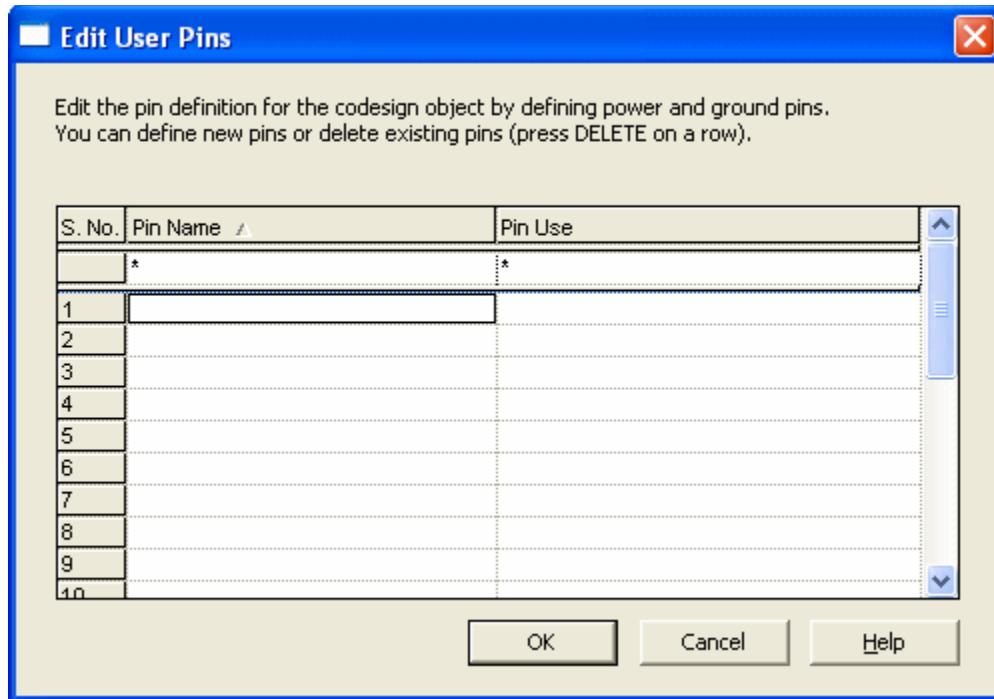


Important

Renaming a user-defined Power/Ground pin is not supported.

Adding New User-Defined Logical Pins

1. Right-click on the co-design block in the Component List pane.
2. From the pop-up menu, choose *Edit User Pins*.



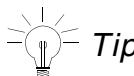
Important

The *Edit User Pins* menu command is available only for co-design objects.

The Edit User Pins dialog box lists all the user-defined pins added to the co-design die. Blank rows in the dialog box indicate that no user-defined pins have been added to the die. In case you open the dialog box multiple times, pins already added by you are listed in this dialog box. User pins added to the co-design die in SiP Layout are listed as non-editable pins in the Edit User Pins dialog box.

3. In the Pin Name column, add the name of the logical pins to be added.

The case of the pin name entered by you in the Pin Name column is reflected as is in the Component Connectivity Details pane. However, for generating the Pin Number, all uppercase alphabets are used. For example, if you enter the user Pin Name as Vcc. The pin name displayed in the Connectivity Details pane is Vcc, while the PIN Number is set to VCC.



Tip
Preserving the casing for the logical pin name ensures that when you launch I/O Planner from SiP Layout to define the IO drivers and bump array placements, the mapping of physical to logical pins is preserved.

4. In the Pin Use column, specify the pin type.
5. Click OK.
6. Save the design.

The modifications are visible in the Component Connectivity Details pane. If you now perform *Export Physical*, the changes made by you in the Edit User Pins pins dialog box, will be reported as ECOs in SiP Layout.



Important
Using the Edit User Pins dialog box, you can only modify the user-defined pins. Pins in the co-design die that are defined in the verilog file — used while building a die in I/O Planner — cannot be modified.

Adding User Pins to a Die With Unassigned Bumps

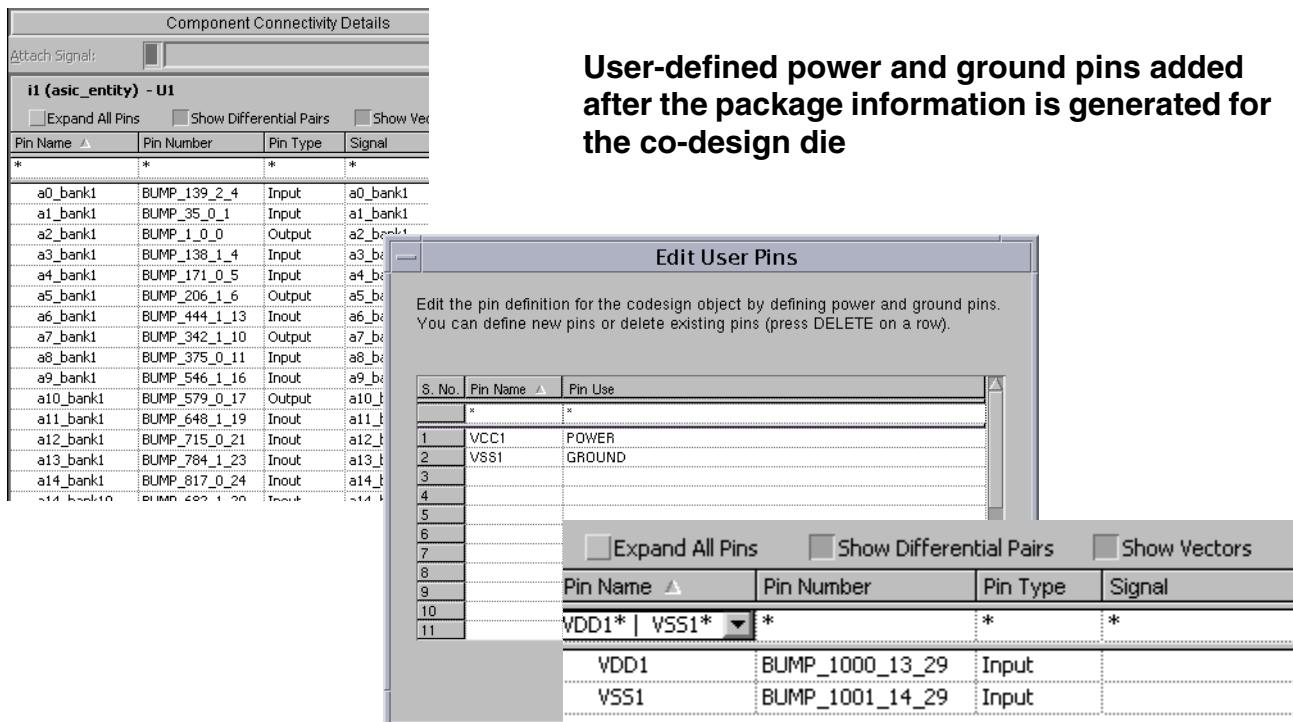
In the SiP Design cycle, user-defined pins may get added to a co-design at any stage of the design cycle. If you add user-defined pins, before the design is sent to SiP Layout and I/O Planner for packaging, the pin number for the user-defined pin is generated based on the pin name.

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However, once the design is sent to SiP Layout and I/O Planner for packaging and the logical design in SCM is updated with the changes made in SiP Layout and I/O Planner, the pin numbers of the co-design die are modified.

If you now add new user-defined pins to the co-design die, the new pin will automatically get assigned to an unassigned physical pin.



User pins mapped to unassigned bumps

This assignment cannot be modified in System Connectivity Manager. To modify the association of the logical and the physical pin, you need to open the die in I/O Planner and then modify the pin assignment.

Pins Added in SiP Layout

After you use the Import Physical command to update System Connectivity Manager with the modifications in the physical design, any user pins that are added to the co-design object in SiP Layout, are visible in the Component Connectivity Details pane. For these pins, the value of the VERILOG_PORT_NAME property is listed as pin name in the Component Connectivity Details pane. When you open the Edit User Pins dialog box on a co-design object, the pins added in SiP Layout are listed as non-editable pins as shown in the [Figure 16-5](#) on page 441.

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If the co-design object that has multiple pins added in SiP Layout with same pin name, for each pin name only one entry is listed in the Edit User Pins dialog box.

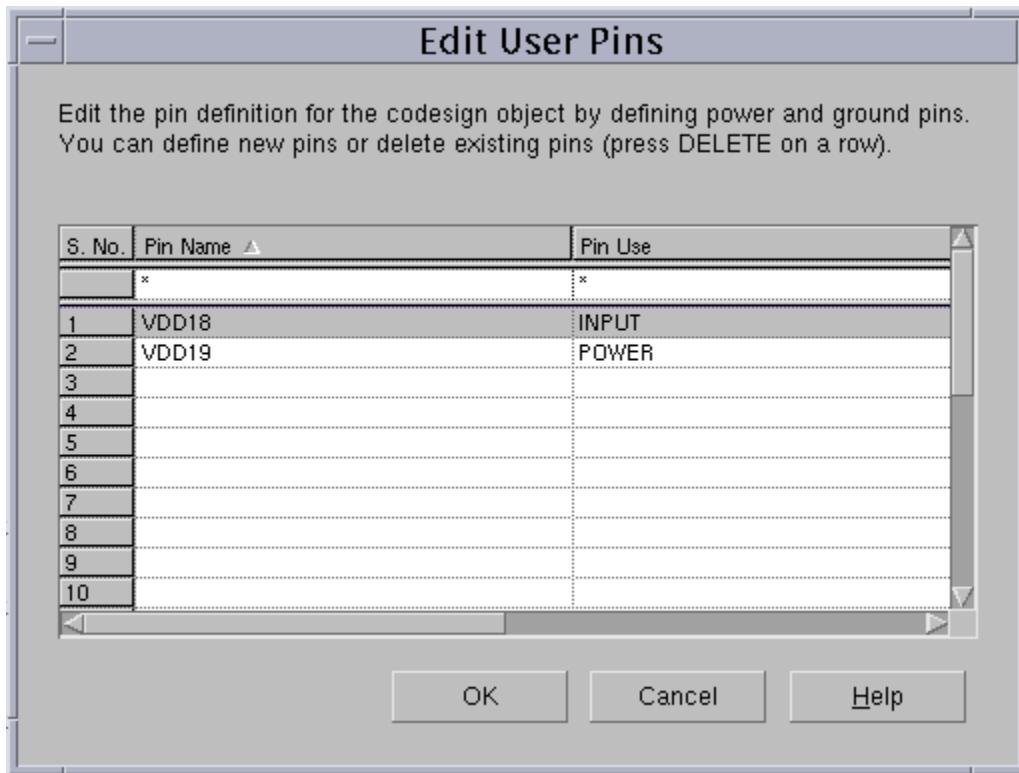


Figure 16-5 User Pin Added in SiP Layout Listed as Non-Editable Pin

Naming Convention for Pins Added to the Co-Design Block

While specifying the pin names in the Edit User Pins dialog box, ensure that the following characters should not be used as pin names.

- asterisk (*)
- ampersand (&)
- comma (,)
- forward slash (/)
- exclamation mark (!)
- <
- >

- colon (:)
- backward slash (\)
- single quotation mark (')
- double quotation mark (")
- All extended character sets

There are some characters that can be used as pin names, but while generating pin numbers, these characters are replaced by underscore(_).

Deleting User-Defined Pins from Co-Design Die

User-defined pins can be deleted only if they are not mapped to a physical pin of the co-design package. Once the packaging information is created for the co-design die, and the user-defined pins are mapped to physical pins of a package, they cannot be deleted.

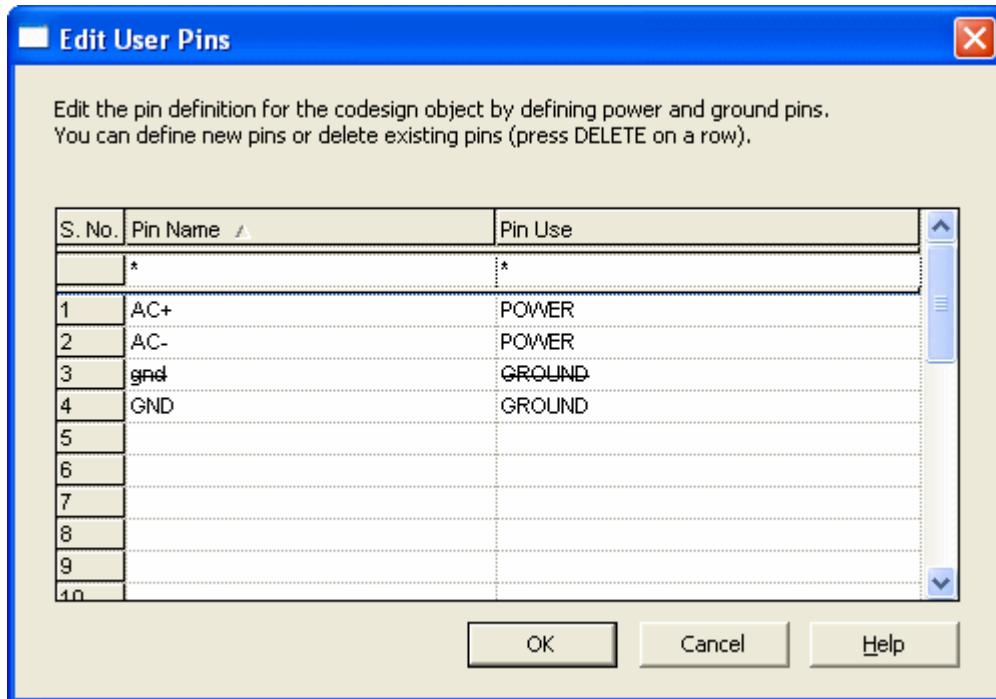
In case you want to remove a user-defined pin from the co-design object in System Connectivity Manager, complete the following steps.

1. Right-click on the co-design block in the Component List pane, and from the pop-up menu choose *Edit User Pins*.

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2. In the dialog box, select the row corresponding to the pin to be removed and press the Delete key.



3. Click OK.

The Pin Name that you deleted is removed from the Component Connectivity Details pane.

 *Important*

System Connectivity Manager does not throw error if you try to delete user-defined pins for which connectivity is specified.

4. Save the design.

Importing Changes to a Verilog File (Verilog ECO)

In the SiP design flow, Verilog ECO can be performed at any stage in the design cycle. However, modified Verilog file with logical changes must only be imported in SCM. This section lists the tasks to be performed for importing the Verilog ECOs in System Connectivity Manager.

Importing Verilog ECO in System Connectivity Manager

If the Verilog file that was imported in System Connectivity Manager, to create a co-design die gets modified, the modifications can be imported in the design as ECO changes.

To import the modifications in a Verilog file, perform the following steps.

1. In the Hierarchy Viewer, right-click on the table block created by importing the Verilog file in System Connectivity Manager.
2. From the pop-up menu, choose *Verilog ECO*.
3. In the Import Verilog ECO dialog box, specify the path to the Verilog file to be imported.
4. Click *OK*.

The Import Verilog ECO dialog box lists all the modifications made to the Verilog file.

5. To update the design with these changes, click *OK*.

The logical design is updated with the modifications in the Verilog file.

Note: Verilog ECO cannot be performed for co-design die that is instantiated multiple times in a design, or on a block that has components or blocks instantiated in it.

Synchronizing the Logical and Physical Designs After Verilog ECO

After importing the modifications to the Verilog file, as Verilog ECOs, perform the following steps to update the physical design in SiP Layout with the modifications.

1. In SCM, choose *Project – Export Physical – SiP Package*.
2. Select the *Update Layout (Netrev)* check box.
3. Select the *Open Layout in SiP Digital Layout* option and click *OK*.
4. In SiP Layout, choose *Edit – Die*.

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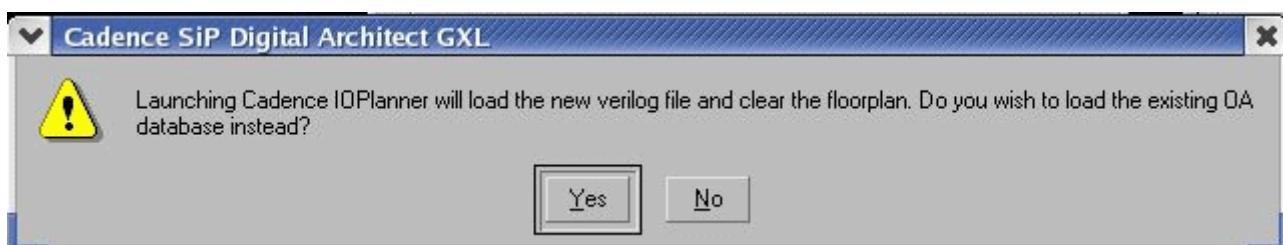
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The following message box appears.



5. Click Yes to launch IO Planner.

The following message box appears.



Click Yes to save the floorplan information before updating the co-design die. Click No to open IOP with new Verilog file.

6. Make the required changes in IO Planner, Update package and exit IO PLanner.
7. Save the design in SiP Layout.

Impact of Verilog ECO

[Table 16-4](#) on page 445 list the types of changes that can be made to the Verilog file and the impact on the design when these changes are imported as Verilog ECOs in System Connectivity Manager.

Table 16-4 Impact of Verilog ECO

Type Change	Result of importing ECO changes to the design
Size of a vectored port increased or a new port added	<ul style="list-style-type: none">■ A new port is added to the co-design block■ The connectivity and the associated components attached to the old ports is retained.

Table 16-4 Impact of Verilog ECO

Type Change	Result of importing ECO changes to the design
Port type changed	<ul style="list-style-type: none"> ■ Port type changed in the design. ■ The existing connectivity is retained.
Port deleted	<ul style="list-style-type: none"> ■ Port removed from the component ■ Connectivity data removed for the deleted port <p>Note: Signals connected to the deleted port continue to be in the design.</p>
Vector port changed to scalar port and other way round	<p>Connectivity data removed for the port.</p> <p>Note: Changing a scalar port to a vector port, or vector port to a scalar port has the same impact as deleting a port and adding a new port. Connectivity information lost for the port.</p>
User-defined port added as a port in the Verilog file	The user-defined port is replaced with the Verilog port and is not listed in the Edit User Pins dialog box.
Verilog port renamed	<p>The old port is deleted along with the connectivity information</p> <p>The renamed port is added as a new port.</p>

Exchanging Interface Data Between Projects

To enable the exchange of interface signal information and BGA package information across PCB and SiP projects, you need to perform the following procedures:

- [Exporting Interface Data](#) on page 447
- [Importing Interfaces in a Design](#) on page 448
- [Importing Interface ECO Data](#) on page 450



The vector notation specified in the General page of the *Setup dialog box (Project —Settings —General)* must be identical for the SiP and the PCB projects.

Exporting Interface Data

To export the interface definition of packaged component between PCB and SiP projects, perform the following steps.

1. Choose *Design – Export Codesign Interface*.

The Select Component to Export dialog box appears.

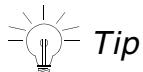
2. From the *Component* drop-down list, select the design component for which you want to export the interface data.



Note: Only BGAs are listed in the Component drop-down list.

3. Click *OK*.

A Save As dialog box appears. Specify a file name and location to save the XML file.



The generated XML file contains the interface definition and package component (BGA) information. It includes logical as well as physical information about the pins. Therefore, during the design cycle any change in the pin number or the pin name of the SiP will cause a change in the exported XML file.

To successfully export the interface data, ensure that all signals connected to the component pins are interface signals. Local signals are not exported. If the component for which the

interface data is to be exported has local signals connected to it, the following dialog box appears.



- To export all local signals connected to the component pins as interface signals, click *OK*.
- Note:** Export Interface command fails if you select *Cancel*.
- To modify the project settings, such that local signals are always exported as interface signals, select the *Always Export Signals as Inout* check box, and then select the *OK* button.

 **Important**

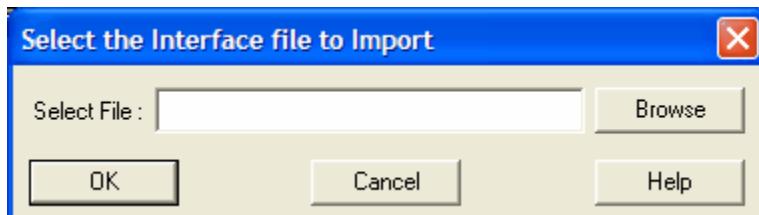
PCB and SiP projects follow different voltage ratings. Consequently, the power group properties attached to the power pins of the BGA component are not exported with the interface definition.

Importing Interfaces in a Design

To import interfaces in your project, do the following:

1. Open your project in System Connectivity Manager.
2. Choose the *Design — Import Interface* menu option.

The Select the Interface file to Import dialog box appears.



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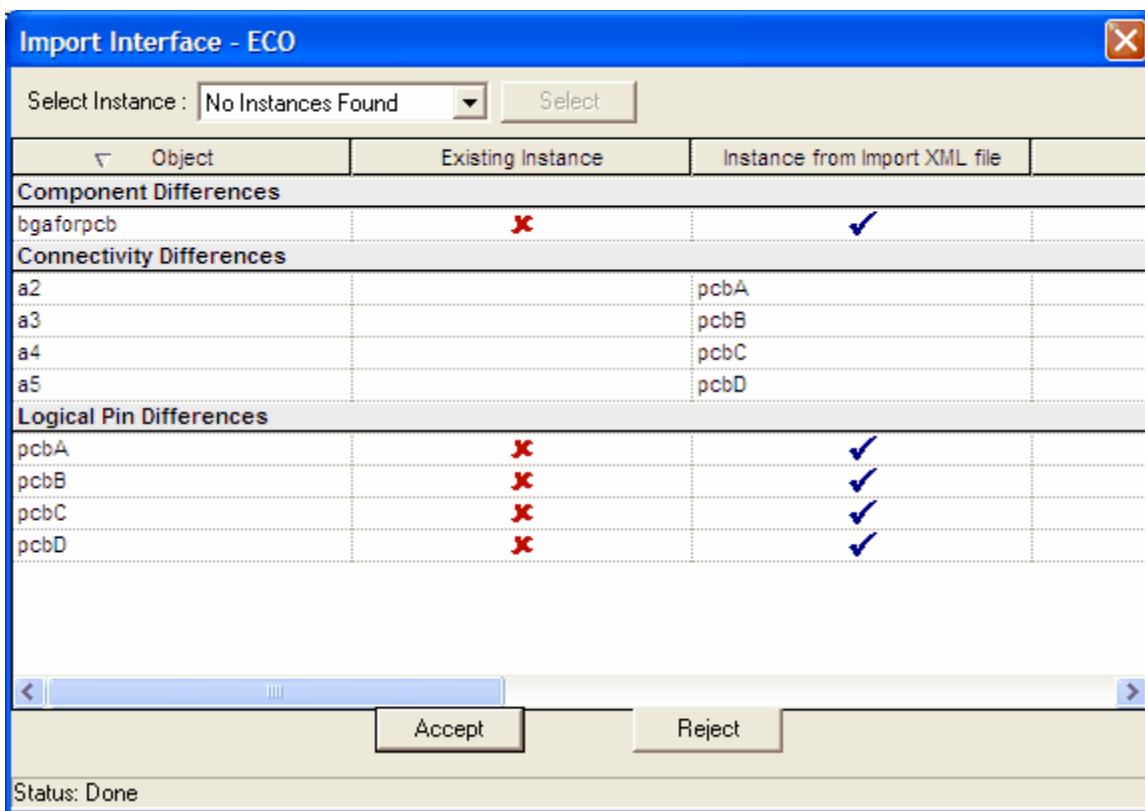
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3. Specify the name and location of the `.xml` file containing the interface definition of the SiP to be imported.

4. Click *OK*.

The Import Interface - ECO dialog box appears.

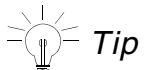
5. If the packaged component does not appear as a selected instance, then choose it from the *Select Instance* drop-down box and click *Select*.



The Import Interface - ECO dialog box lists the differences between the existing interface information and the data being imported. Depending on whether the package was already instantiated in the design or not, one of the following holds true:

- ❑ If the package is not instantiated in the design, the package specified in the `.xml` file is added to the design. Connectivity information of the package is also imported. The signals are created and listed in the Signal List pane. In this case, the package to be imported is listed below Component Differences.
- ❑ If the package is already instantiated in the design, the connectivity of the package in the design is verified with the connectivity details in the imported `.xml` file. In the Import Interface - ECO dialog box, select the instance name from the *Select*

Instance drop-down list and click *Select*. Differences, if any, are listed in the Import Interface - ECO dialog box.



Tip
The XML file contains the interface definition and package component (BGA) information. It includes logical as well as physical information about the pins.

6. To import the interface modifications to your design, click *Accept*.

The package and connectivity information is imported in the design.

Importing Interface ECO Data

The Import Interface - ECO dialog box reports differences for both nets and components. The following rules apply:

- Property differences are reported only for nets. The pin property differences are not reported while importing ECO changes.
- The component property differences are not reported and, as a consequence, these are not transferred between the PCB and SiP projects.
- The GLOBAL signals are imported as `INOUT` signals.
- Modifications in the signal scope or the signal type are not supported. For example, if you import an interface signal of type `INOUT` and a signal with the same name already exists in the design as an IN signal, only the signal connectivity modifications are imported and not the signal type.
- Importing a renamed signal is the same as importing a new signal. Therefore, if the xml being imported has a renamed signal, it will get added to the design while the old signal is still available in the design.

Example

If you modify the die interface and swap signals `pcbC` and `pcbD`

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Export the die interface and reimport the interface in the PCB design, the changes are reported as shown in the following figure.

The screenshot shows the 'Import Interface - ECO' dialog box. At the top, there is a table with columns: Pin Name, Pin Number, Pin Type, and Signal. Below this is a dropdown menu 'Select Instance : U1' with a 'Select' button. The main area is titled 'Connectivity Differences' and contains a table with two rows. The first row shows 'a4' as the object, 'pcbC' as the existing instance, and 'pcbD' as the instance from the import XML file. The second row shows 'a5' as the object, 'pcbD' as the existing instance, and 'pcbC' as the instance from the import XML file.

Pin Name	Pin Number	Pin Type	Signal
*	*	*	*
a1	A1	Inout	
a2	A2	Inout	pcbA
a3	A3	Inout	pcbB
a4	A4	Inout	pcbC
a5	A5	Inout	pcbD

Object	Existing Instance	Instance from Import XML file
a4	pcbC	pcbD
a5	pcbD	pcbC

After accepting the changes the design looks similar to the following figure.

Pin Name	Pin Number	Pin Type	Signal
*	*	*	*
a1	A1	Inout	
a2	A2	Inout	pcbA
a3	A3	Inout	pcbB
a4	A4	Inout	pcbD
-	-	-	-

Generating a Physical Netlist for SiP

To finalize the physical implementation of SiP, you need to open the design in Cadence SiP Digital Layout, which is the tool used for creating the physical layout for a SiP.

The steps for generating a physical netlist for the SiP design are as follows:

1. In System Connectivity Manager, choose *Project – Export Physical – SiP Package*.
2. In the *Output Board File* text box, specify the name of the .SIP file to be generated.
3. Specify other options in the Export Physical dialog box
4. To open the generated .SIP file in SiP Layout, select the *Open Package in SiP Digital Layout* option.

A .SIP file is generated and opened in SiP Layout. A .SIP file is a database file format used for storing the physical details about the SiP being developed as a co-design object.

5. Click *OK*.

A .SIP file is generated and opened in SiP Layout.

Synchronizing Logical and Physical Designs

To synchronize the logical SiP design in System Connectivity Manager with the physical layout for the SiP in SiP Layout, complete the following steps.

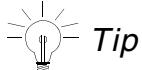
Updating a Logical Design with the Changes in the Physical Design

All packaging modifications and the changes made to the physical implementations of a co-design die, in SiP Layout are saved in the .SIP file. Therefore, to update the logical SiP design in System Connectivity Manager with the changes made to the physical layout of the SiP in SiP Layout, import the .SIP file from *Project – Import Physical*.

The changes are treated as ECO changes and are displayed in the Visual Design Differences pane in System Connectivity Manager. View the changes and update the logical design with the changes.

To know more about synchronizing the logical and physical designs, see [Chapter 18, “Transferring the Logical Design to a Board and Design Synchronization.”](#)

Updating a Physical Design with the Changes in the Logical Design



In the SiP design cycle, if the physical and logical implementations of the SiP are being design simultaneously, it is recommended that the *Export Physical* command is used once before capturing the connectivity data for SiP. Capturing connectivity information after doing *Export Physical* ensures that the connectivity information is not lost for further ECOs.

1. Capture connectivity in System Connectivity Manager by assigning nets to package pins.
2. To export logical-design changes in System Connectivity Manager, choose *Project – Export Physical – SiP Package*.
3. Open the .SIP file in SiP Digital Layout.

This step ensures that the generated `.SIP` file is updated with the modifications made to the logical design in System Connectivity Manager.

4. The SiP layout designer modifies the design connectivity in SiP Layout.

To know more about performing design tasks in SiP Digital Layout, see *SiP Digital Architect/SiP Layout User Guide*.

5. To import connectivity changes done in SiP Digital Layout to your project in System Connectivity Manager, choose *Project – Import Physical*.
6. Perform ECO updates.

Besides the connectivity changes, the other most common changes that can be made to the physical layout for SiP and the steps to be followed for synchronizing the logical and physical implementations of a SiP are listed below.

Case 1: Changes in Cadence I/O Planner

Change: New physical pins are added to a co-design die in Cadence I/O Planner

Synchronization steps:

- a. Backannotate these changes into SiP Layout along with a physical pin mapping.
- b. Backannotate SiP Layout modifications to System Connectivity Manager

Case 2: Changes in SiP Layout

Change: New co-design die added in SiP Layout.

Synchronization steps: Backannotate SiP Layout modifications to System Connectivity Manager.

- a. Save the physical layout in SiP Layout.

This ensures that the `.SIP` file is updated with the latest modifications in the board.

- b. In System Connectivity Manager, choose *Project – Import Physical* to backannotate the layout changes in System Connectivity Manager.

Adding RF Dies to a SiP

Cadence SiP Digital Architect allows you to add RF dies (created using *Cadence SiP RF Architect XL*) to a SiP design. For this release, you cannot add the RF dies directly in System

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Connectivity Manager. You need to add these dies in SiP layout and then annotate the information to System Connectivity Manager.

The sequence of steps to be followed is listed below.

1. Create the logical design for SiP in System Connectivity Manager.
2. Create the physical layout for the SiP design.
 - a. In System Connectivity Manager, choose *Project – Export Physical – SiP Package*.
 - b. In the Export Physical dialog box, provide required inputs along with the name of the .sip file to be generated.
For more information, see the chapter [Transferring the Logical Design to a Board and Design Synchronization](#).
 - c. Click *OK*.
3. Open the .SiP file in SiP Layout.
4. In the SiP Layout tool, instantiate the RF die.
To know more about how to add dies in SiP Digital Layout, see *SiP Digital Architect/SiP Layout User Guide*.
5. Edit die connectivity.
6. Save the .SIP file.

Synchronizing the Design in System Connectivity Manager and SiP Layout

1. Open the SiP project in System Connectivity Manager.
2. To import the changes, choose *Project – Import Physical*.

Design Reuse

This chapter discusses the following:

- [Overview](#) on page 456
- [Creating Reuse Blocks](#) on page 456
- [Using Reuse Blocks in Other Designs](#) on page 459
- [Setting Allegro PCB Editor Environment Variables](#) on page 463
- [Properties Controlling the Behavior of Modules](#) on page 464

Overview

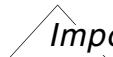
Design reuse is the process of creating standalone reusable physical blocks and using them in different designs. Reusable blocks are existing logical blocks that are associated with at least one placed-and-routed physical module. You can place these blocks within larger designs like you place components from libraries. For example, you will find design reuse particularly useful when creating telecommunication ports, where the same port is required to be used 32, 64, or 128 times in the design.

Whether you are a logic designer or a board designer, you will find that design reuse is an effective way to create complex designs because it helps in:

- **Simplifying the design process**—You can break a complex design into reusable blocks and test each reusable block independently. This increases quality.
- **Partitioning and team design**—You can utilize the design reuse methodology to partition large designs into smaller subcircuits that can be logically defined, placed, and routed in parallel, and then brought back into the final board as individual modules. This methodology is useful if you are creating a design in large teams. Different team members can create blocks of designs and these blocks can be reused across the team.
- **Reuse designs across other designs**—Each design you make is a potential input to future development. Rarely, if ever, will you create any design from scratch. When creating any design, you can reuse existing designs. The advantages of using reusable blocks in your design are faster turnaround time and better quality. The turnaround time decreases because you can use a reusable block in any design without having to re-create it. The quality is enhanced because you can validate a reusable block at the time of its creation and by the time you use it in your design, all design validation issues are resolved. With design reuse you can eliminate redundant effort, prevent repetitive errors, and reduce the cost for each new design.

Creating Reuse Blocks

The process of creating a reuse block in System Connectivity Manager and its corresponding physical module in Allegro PCB Editor involves the following tasks.



Important
This section describes the process of creating a spreadsheet or Verilog based reuse block. For information on creating a schematic based reuse block, see the *Design Reuse* chapter of the *Allegro PCB Design Flows User Guide*.

1. Creating and setting up the project that will contain the design for the reuse block. For more information, see [Creating and Setting Up the Project for the Reuse Block](#) on page 457.
2. Creating the logical design for the reuse block. For more information, see [Creating the Logical Design for the Reuse Block](#) on page 457.
3. Export the logical design for physical layout. For more information, see [Exporting the Logical Design for the Physical Layout](#) on page 457.
4. Creating the physical layout for the reuse block. For more information, see [Creating the Physical Layout for the Reuse Block](#) on page 458.
5. Synchronizing the logical design and the layout. For more information, see [Synchronizing the Logical Design and the Layout for the Reuse Block](#) on page 458.
6. Creating modules from the layout. For more information, see [Creating Physical Modules from the Layout](#) on page 458.

Creating and Setting Up the Project for the Reuse Block

You can do one of the following when creating a reuse block:

- Create a new project that will contain the logical design and physical layout for the reuse block. For information on creating projects in System Connectivity Manager, see [Chapter 3, “Project Creation and Setup.”](#)
- Create a reuse block of an existing design.
- Create a reuse block of one of the blocks in an existing design. For example, if you have a hierarchical design named CPU with the blocks ALU, CACHE, and CONTROLLER, you can create a reuse block of the CACHE block and reuse the block in other designs.

Creating the Logical Design for the Reuse Block

To reuse any design, you need to first create the logical design corresponding to it. This logical design is then exported to create the physical layout for the reuse block.

Exporting the Logical Design for the Physical Layout

After you create the logical design, export it for physical layout using *Export Physical* in System Connectivity Manager. For more information on running *Export Physical*, see [Chapter 18, “Transferring the Logical Design to a Board and Design Synchronization.”](#)



Before you run *Export Physical*, ensure that the logical design for the reuse block is set as the root design in System Connectivity Manager.

For example, if you have a hierarchical design named **CPU** with the blocks **ALU**, **CACHE**, and **CONTROLLER**, and you want to create a reuse block of the **CACHE** block, set the **CACHE** block as the root design before running *Export Physical*.

For more information on setting a design as the root design in System Connectivity Manager, see [Setting the Root Design](#) on page 372.

Creating the Physical Layout for the Reuse Block

After you have exported the logical design for physical layout, you need to complete the physical layout of the design and route it in Allegro PCB Editor. For more information on creating the physical layout for the design, see the Allegro PCB Editor user documentation.

Synchronizing the Logical Design and the Layout for the Reuse Block

Ensure that the logical design and the board are in synch. For more information on synchronizing the logical design in System Connectivity Manager and the board in Allegro PCB Editor, see [Chapter 18, “Transferring the Logical Design to a Board and Design Synchronization.”](#)

Creating Physical Modules from the Layout

A physical module is a board that contains special reuse properties, allowing it to be reused in other modules or designs. Use Allegro PCB Editor to create a module for the board file.

Note: You can create modules that do not have any etch. A module in Allegro PCB Editor can be fully routed, partially routed, or not routed at all. When you create a module using a routed board, you obtain the maximum benefit of design reuse. However, even if you do not route the board from which you create the module, you can reuse it in other layouts.

To create a module in Allegro PCB Editor, do the following:

1. Choose *Tools – Create Module* to start the process of creating a module.
2. Select the objects you want to include in the module.
3. Select the origin by clicking near the middle of the components.

The *Save As* dialog box appears.

4. Specify the location where the module (.mdd) file will be saved.

By default, the module file will be saved in the physical view of the design for the reuse block. Save the module in the directory defined by the Allegro PCB Editor environment variable MODULEPATH. For more information on setting the MODULEPATH environment variable, see [Setting Allegro PCB Editor Environment Variables](#) on page 463.



Ensure that the name of the module is the same as the name of the block in System Connectivity Manager. For example, if you are creating a module for the CACHE block, ensure that the module name is also CACHE.

Using Reuse Blocks in Other Designs

The process of using a reuse block in other designs involves the following tasks.

Note: To understand the process of using a reuse block in other designs, we will use an example of a reuse block named CACHE that you want to use in a design named CPU.

1. Creating the logical design in which you want to use the reuse block. For more information, see [Creating the Logical Design in which you want to use the Reuse Block](#) on page 459.
2. Adding the reuse block in the design. For more information, see [Adding the Reuse Block in the Design](#) on page 460.
3. Exporting the logical design for physical layout. For more information, see [Exporting the Logical Design for Physical Layout](#) on page 461.
4. Placing the reuse modules in the board. For more information, see [Placing the Reuse Modules in the Board](#) on page 462.
5. Completing the physical layout in the board. For more information, see [Completing the Physical Layout in the Board](#) on page 463.

Creating the Logical Design in which you want to use the Reuse Block

You can now create the logical design in which you want to use the reuse block. For example, if you want to add a reuse block named CACHE in a design named CPU, create a project in System Connectivity Manager with the root (top-level) design named CPU.

For information on creating projects in System Connectivity Manager, see [Chapter 3, “Project Creation and Setup.”](#) For information on setting a design as the root design in System Connectivity Manager, see [Setting the Root Design](#) on page 372.

Adding the Reuse Block in the Design

Use Part Information Manager to add the reuse block in the design. You can add multiple instances of a reuse block in your design. For example, for some blocks like telecommunication ports, the block can be used 32, 64 or 128 times. You can then wire the blocks as required.

For example, do the following to add the reuse block named CACHE in the design named CPU.

1. Do one of the following:

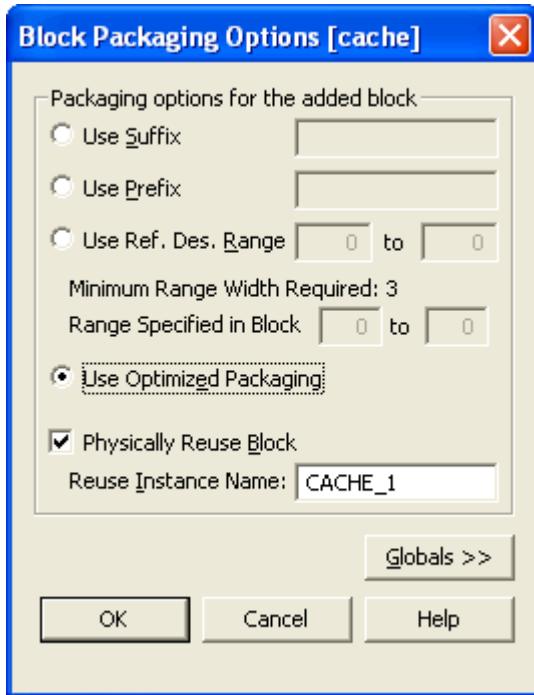
- Choose *Design – Add Component*.
- Click  on the toolbar.

Part Information Manager appears.

2. Select the library in which the reuse block CACHE exists, then select the CACHE block in Part Information Manager.

3. Click *Add*.

The *Block Packaging Options* dialog box appears.



The *Physically Reuse Block* check box is selected by default if the block you are adding is a reuse block.

The *Reuse Instance Name* field displays the unique ID CACHE_1 that System Connectivity Manager assigned for the instance of the CACHE reuse block you are adding in the design. Allegro PCB Editor uses this ID to identify the physical module corresponding to each instance of the reuse block you are add in the design.

Note: You can change the reuse instance name.

4. Specify the packaging options for the block and click *OK*.

System Connectivity Manager automatically packages the block and adds it in the design. For more information on specifying the packaging options for a block, see [Block Packaging Options](#) on page 687.

5. Close Part Information Manager.

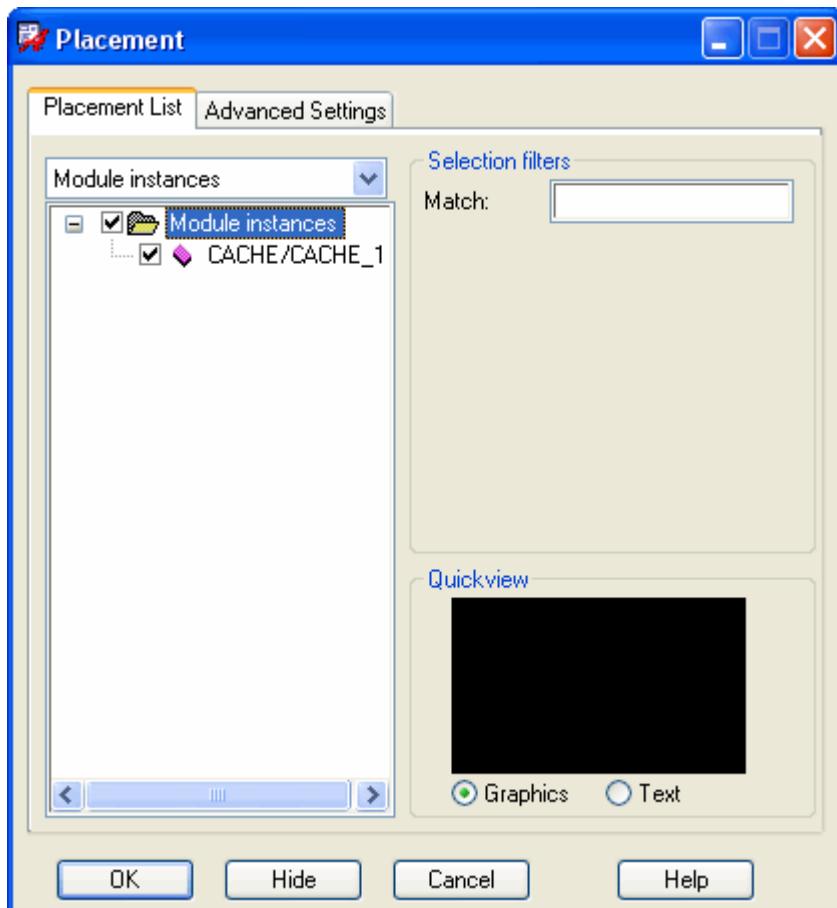
Exporting the Logical Design for Physical Layout

Export the logical design for physical layout using *Export Physical* in System Connectivity Manager. For more information on running *Export Physical*, see [Transferring the Logical Design to a Board and Design Synchronization](#) on page 463.

Placing the Reuse Modules in the Board

You can now place the reuse modules in the board.

1. Choose *Place – Manually* in Allegro PCB Editor to place the modules in the board.
The Placement dialog box appears.
2. From the *Placement List* drop-down list, choose *Module Instances*.



The list of modules corresponding to each instance of a reuse block you added in your logical design are displayed in the Placement dialog box. For example, the module instance CACHE/CACHE_1 displayed in the Placement dialog box indicates that the module named CACHE.MDD corresponds to the CACHE_1 instance of the CACHE reuse block you added in your logical design in System Connectivity Manager.

Completing the Physical Layout in the Board

Non-module based components and the rest of the physical design still needs to be added. You can place the remaining components before, during, or after the module placement.

Setting Allegro PCB Editor Environment Variables

You need to set the MODULEPATH Allegro PCB Editor environment variable for Allegro PCB Editor to be able to read the physical modules corresponding to each reuse block.

If you do not include the directory that contains the module (.mdd) files in the MODULEPATH, Allegro PCB Editor displays the following error when you try to place the module in the board:

Error: Module Definition <module_name> not found.

To set the MODULEPATH variable, do the following:

1. Choose *Setup – User Preferences* in Allegro PCB Editor.

The User Preferences Editor dialog box appears.

2. Click *Design_paths* in the *Categories* list.
3. Click the *Value* button next to *modulepath*.

The modulepath Items dialog box appears.

4. Click  to add a new module path.

Add the paths to the directories that contain the physical modules corresponding to the reuse blocks you are using in your design, or click the browse button to select the directory.

5. Click *OK* to close the modulepath Items dialog box.
6. Click *OK* to close the User Preferences Editor dialog box.

Properties Controlling the Behavior of Modules

The REUSE_INSTANCE property controls the behavior of reuse modules corresponding to the reuse blocks you add in your design.

REUSE_INSTANCE

The REUSE_INSTANCE property specifies the unique ID for an instance of a reuse block in your design. Allegro PCB Editor uses the REUSE_INSTANCE property to identify the physical module corresponding to each instance of a reuse block in your design.

The REUSE_INSTANCE property is assigned to every instance of a reuse block in your design. By default, System Connectivity Manager assigns

<reuse_block_name>_<number> as the value of the REUSE_INSTANCE property. For example, the first instance of a reuse block named CACHE you add in your design will be assigned the REUSE_INSTANCE=CACHE_1 property. The second instance will be assigned the REUSE_INSTANCE=CACHE_2 property, and so on. You can specify a different value for the REUSE_INSTANCE property in the *Reuse Instance Name* field of the [Block Packaging Options](#) dialog box.

Note: Unlike other properties, the REUSE_INSTANCE property defined on the highest level block wins in the case of nested blocks.

Transferring the Logical Design to a Board and Design Synchronization

This chapter describes the tasks you need to perform to transfer the logical design in System Connectivity Manager to a board or physical layout and keep the design in System Connectivity Manager and the board in synch. For creating a PCB, Allegro PCB Editor (`allegro`) is used. However, if you are using SCM to design a System - in- Package (SiP) the physical layout is done in SiP Layout (`cdnsip`).

The topics covered in this chapter are:

- [Overview](#) on page 466
- [Design Synchronization Tasks](#) on page 466
- [System Connectivity Manager to Allegro PCB Editor Flow](#) on page 467
- [Updating the Board with the Changes in the Logical Design](#) on page 469
- [Updating the Logical Design with the Changes in the Board](#) on page 474
- [Running Visual Design Differences](#) on page 481
- [Difference Categories](#) on page 488



Throughout this chapter we will refer to the design in System Connectivity Manager as the *logical design* and the physical layout in Allegro PCB Editor or Allegro PCB SI as the *board*. However, if you are using System Connectivity Manager from SiP Digital Architect (GXL or XL), the physical layout is done in SiP Layout.

Overview

The development of any design involves an iterative process of synchronizing the differences between the logical design and the board. Changes especially caused by Engineering Change Orders (ECOs) in the logical design need to be updated in the board. Similarly, changes in the board such as reference designator changes, constraint changes, and section and pin swaps require corresponding updates in the logical design.

Based on how you create a design, you can synchronize the logical design and the board in one of the following two ways:

1. The conventional or linear flow

In the conventional flow, you first create the logical design in System Connectivity Manager, make changes to it, get the logical design reviewed and approved. Next, you prepare the board and send it for manufacturing. When you prepare the board, last-minute changes, such as adding terminations or removing components, can cause property and connectivity differences between the logical design and the board. These changes need to be backannotated to the logical design.

2. The concurrent or parallel flow

In the parallel flow, the logic and board designers work in parallel. First, the logic designer starts work on the logical design. At some point in time, the board designer imports the logical design and uses it to create the board. Meanwhile, the logic designer starts work on the next module. Later, the logic designer might make changes to the logical design and the board designer might make changes to the board. Therefore, it is important to synchronize the logical design and the board.

Whether you follow the linear flow or the parallel flow, it is important that the logical design and the board are always synchronized. System Connectivity Manager lets you compare the logical design and the board. You can update changes from the logical design to the board or from the board to the logical design. However, you cannot update changes from one logical design to another or from one board to another.

Design Synchronization Tasks

The design synchronization process can involve the following tasks:

1. Exporting the logical design to translate it into a physical design ready for layout in Allegro PCB Editor or SiP Layout.

For more information, see [Updating the Board with the Changes in the Logical Design](#) on page 469.

2. Backannotating the changes made in the board to the logical design.

For more information, see [Updating the Logical Design with the Changes in the Board](#) on page 474.

3. Updating the changes made in the logical design, after initial packaging, to the board.

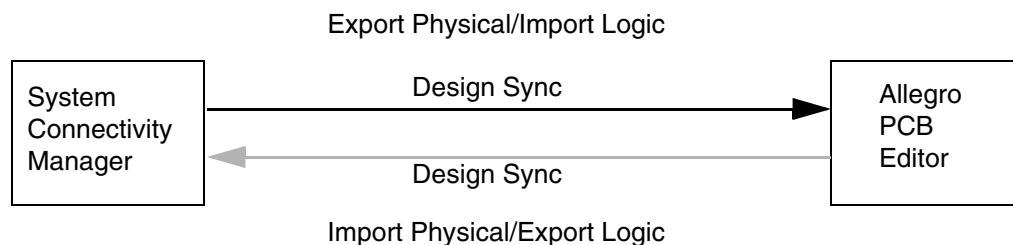
For more information, see [Updating the Board with the Changes in the Logical Design](#) on page 469.

While the translation is done only once, backannotation and updating can be done multiple times to bring the logical design and the board in sync.

System Connectivity Manager to Allegro PCB Editor Flow

The System Connectivity Manager to Allegro PCB Editor flow lets you compare the logical design and board information by comparing the logical design in System Connectivity Manager and the feedback files generated from the board using Allegro PCB Editor. Figure 18-1 provides an overview of flow from System Connectivity Manager to Allegro PCB Editor and back again.

Figure 18-1 System Connectivity Manager to Allegro PCB Editor Flow



When you run *Export Physical* (with the *Generate package files (pstdedb.cdsz)* check box selected), System Connectivity Manager creates the `pstdedb.cdsz` file. This file contains the following five `pst*.dat` packaging files in the packaged view of the root design. For information on running *Export Physical*, see [Updating the Board with the Changes in the Logical Design](#) on page 469.

- **pstchip.dat**—Contains a physical description for each physical part used in your design. System Connectivity Manager extracts this physical description from the `chips.prt` file, physical part table files, and properties on instances. This file contains a description of only the physical parts used in the logical design.
- **pstxprt.dat**—Lists each reference designator and the sections assigned to it.

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- **pstxnet.dat**—The `pstxnet.dat` file is the connectivity file. This file lists each net in the logical design, its properties, its attached nodes, and node properties. The list is ordered by physical net name and contains all net properties and the logic-to-physical binding of nets and nodes.
- **pstcmdb.dat**—Contains the definition of properties and electrical constraints in the logical design.
- **pstdmlmodels.dat**—Contains the signal integrity models assigned on components and pins in System Connectivity Manager.

The five `pst*.dat` files are used by Netrev to create or update the board. You can run Netrev from:

- System Connectivity Manager by running *Export Physical* (with the *Update Board (Netrev)* check box selected).
For more information on running *Export Physical*, see [Updating the Board with the Changes in the Logical Design](#) on page 469.
- Allegro PCB Editor by running Import Logic (Choose *File – Import – Logic* in Allegro PCB Editor).
For more information on running Import Logic, see the [Allegro PCB and Package User Guide: Transferring Logic Design Data](#).

You can make changes in Allegro PCB Editor and then feedback the changes in the board to the logical design by running:

- *Import Physical* from System Connectivity Manager (See, [Updating the Logical Design with the Changes in the Board](#) on page 474), or
- Export Logic from Allegro PCB Editor (choose *File – Export – Logic* in Allegro PCB Editor).
For more information on running Export Logic, see [Allegro PCB and Package User Guide: Transferring Logic Design Data](#).

When you feedback the changes in the board to the logical design, `genfeedformat` creates the following six feedback files:

- **pinview.dat**—Contains connectivity and pin instance properties information generated by Allegro PCB Editor.
- **netview.dat**—Contains property information for the nets generated by Allegro PCB Editor.
- **funcview.dat**—Contains property information for the instances in the logical design.

- **compview.dat**—Contains property information for the component instances generated by Allegro PCB Editor.
- **cmdbview.dat**—Describes the current electrical constraint information for the design. This file contains the latest electrical constraint information existing in the board.
- **cmbcview.dat**—Specifies the base copy of the electrical constraint information used by the Allegro PCB Editor board snapshot.

You can now use the feedback files to update the logical design with the changes in the board by running *Project – Import Physical* in System Connectivity Manager to do one of the following:

- Update the changes in the board to the logical design.
- Update the changes from the previously generated feedback files to the logical design.

When you run *Import Physical*, differences between the logical design and the board are displayed in the Visual Design Differences pane. The Visual Design Differences pane lets you view and update all the design differences between the logical design and the board.

Note: You cannot update the board using the Visual Design Differences pane.

For more information on running *Import Physical*, see [Updating the Logical Design with the Changes in the Board](#) on page 474. For more information on using the Visual Design Differences pane, see [Running Visual Design Differences](#) on page 481.

Updating the Board with the Changes in the Logical Design

In the design cycle, you first capture the logic design in System Connectivity Manager and then run *Export Physical* to export the logical design to translate it into a physical design ready for board layout in Allegro PCB Editor. To incorporate incremental changes in the logical design into the existing board, you can run *Export Physical* again.

Note: Properties that you add in System Connectivity Manager and that you define as transferable between System Connectivity Manager and the board in the [Property Flow](#) tab of the [Setup](#) dialog box are automatically passed to the board when you run *Export Physical*.

Setup tasks

Before you create the physical layout for your design in Allegro PCB Editor or SiP Digital Layout, you must ensure that the measurement units and the precision values used in Allegro

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PCB Editor (or SiP Digital Layout) must be the same as the measurement units and the precision values used in Constraint Manager while capturing constraints in the logical design. This synchronization of measurement units and the precision factor is required to avoid a display of false differences in the Visual Design Difference window.

Note: Synchronizing measurement units after you have created the board file does not remove the differences displayed in the VDD window.

- To view the measurement units used in the Constraint Manager, launch Constraint Manager from SCM and choose *Tools – Precision*.

To ensure that the measurement units used in the board layout tool are in sync with the units used in SCM, do the following.

1. Create an empty board in Allegro PCB Editor or SiP Layout.
2. Choose *Setup – Drawing Size*.
3. In the Drawing Parameters dialog box, set the measurement units.
 - a. From the *User Units* drop-down list select *Millimeter*.
 - b. Ensure that the value in the *Accuracy* field is the same as the precision value used in Constraint Manager when launched from System Connectivity Manager.
 - c. Click OK.
4. Save the board.

Use this board file, as the *Input Board File* during *Export Physical*.

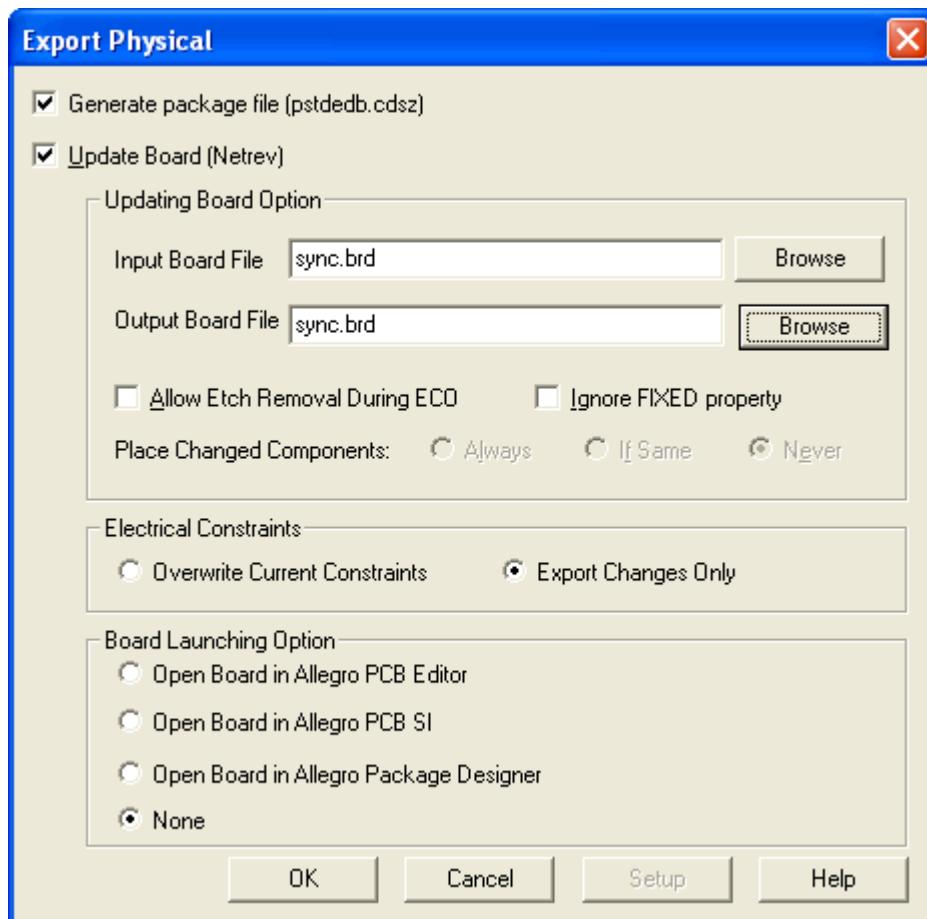
To update the board with the changes in the logical design

1. To update a PCB board, choose *Project – Export Physical – PCB Board*.
To update a SiP Layout with the changes in the logical SiP design, choose *Project – Physical – SiP Package*.

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The Export Physical dialog box appears.



2. To package your design before updating the layout data, select the *Generate package files (pstdedb*.cdsz)* check box.

System Connectivity Manager creates the `pstdedb.cdsz` file that contains the five packaging files (`pstchip.dat`, `pstxprt.dat`, `pstxnet.dat`, `pstcmdb.dat`, and `pstdmlmodels.dat`) in the packaged view of the root design when you click *OK*. For more information on the `pst*.dat` packaging files, see [System Connectivity Manager to Allegro PCB Editor Flow](#) on page 467.

Note: You can set the `DS_PRESERVE_PSTFILE` environment variable if you want System Connectivity Manager to create the `pstdedb.cdsz` file and the four packaging files (`pstchip.dat`, `pstxprt.dat`, `pstxnet.dat` and `pstcmdb.dat`) in the packaged view of the root design.

3. To update the board, select the *Update Board (Netrev)* check box.

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4. In the *Input Board File* field, enter the name and path to the existing board file that needs to be updated.

If the board file is being created for the first time, enter the name of the board created in [step 1 to step 4](#) of the [Setup tasks](#) on page 469, in the *Input Board File* field.

By default, the name of the board file that was created during a previous run of *Export Physical* is displayed in the *Input Board File* field. If the physical path to the board file is not displayed, it indicates that the board file is in the [physical](#) view of the root design.

To use another board file as the input board file, enter the name and path to the board file, or click *Browse* to select the file.

Note: If this is the first time you are running *Export Physical*, it is recommended that you create an empty board file using the steps listed in the [Setup tasks](#) section, and use it as the input board file. You can also start setting up your design by creating a board outline and defining the layers for the design.

5. In the *Output Board File* field, enter the name and path to the updated board file.

By default, the name of the board file that was created during a previous run of *Export Physical* is displayed in the *Output Board File* field. If the physical path to the board file is not displayed, it indicates that the board file is in the [physical](#) view of the root design.

If the input and output board file names are the same, System Connectivity Manager overwrites the existing board file. If you specify a new file name for the output board file, a new board file is created.

Note: If you specify a new file name for the output board file but do not specify the path where the file needs to be created, the output board file will be created in the [physical](#) view of the root design.

6. To make Allegro PCB Editor rip up an etch from a removed pin to the closest connection or pin, select the *Allow Etch Removal During ECO* check box and select the option for placing changed components in layout from those made available by System Connectivity Manager.

Always	If you load a new design logic into the Allegro PCB Editor layout, Allegro PCB Editor automatically replaces all components in the layout with the new components from System Connectivity Manager according to their reference designators.
--------	--

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If Same	Allegro PCB Editor automatically replaces all components in the layout with the new components from System Connectivity Manager but only if the replacement component matches the package symbol, value, and the tolerance of the component in the layout.
Never	This is the default selection. Allegro PCB Editor will never replace any components in the layout with new components. You must make the changes interactively.

7. Select the option for exporting constraints from the logical design to the board:

Overwrite Current Constraints

Deletes all existing electrical constraint information in the *Output Board File* and replaces it with the electrical constraint information currently available in the logical design.

Export Changes Only

Exports only the electrical constraint information that has changed in the logical design since the last export, and updates such constraints in the *Output Board File*.

8. Select the option for opening the board after the export process is completed.

Open Board in
Allegro PCB Editor

Opens the board in Allegro PCB Editor.

Open Board in
Allegro PCB SI

Opens the board in Allegro PCB SI.

Open Board in
Allegro Package
Designer

Opens the board in Allegro Package Designer.

Open Board in SiP
Digital Layout

Opens the board in SiP Digital Layout.

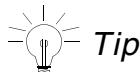
Note: This option is available only if you are using System Connectivity Manager to design a SiP.

None

Does not open the board after the export process is completed.

9. Click *OK*.

The progress of the export process is displayed in the Session Log window.



Tip

You can also generate the package files by selecting the *Generate package files (pstdedb.cdsz)* check box in the Export Physical dialog box and then run Import Logic (choose *File – Import – Logic*) in Allegro PCB Editor to update the board with the changes in the logical design. For more information on running Import Logic, see the *Allegro PCB and Package User Guide: Transferring Logic Design Data*.

Updating the Board with Changes in the Logical Design in the Silent Mode

If required, you can also save all in the design and package your design in the silent (nogui) mode by using Netrev command line arguments or a Tcl command. For example, you can use the following Netrev command:

```
netrev -proj "$PROJ_PATH/<projectname>.cpm" -u -y 1 -n -1  
"$PROJ_PATH/worklib/top/physical/<output>.brd" -$
```

Details of the Netrev command line arguments are available in the console.

Tcl command:

```
saveAll  
  
exportPhysical pcb genpkg updateBoard -I "$PROJECT_PATH/  
input.brd" -O "$PROJECT_PATH/output.brd" -P always -L None
```

For details of other Tcl commands, refer to the *System Connectivity Manager TCL Commands* Cadence document.

Updating the Logical Design with the Changes in the Board

The following changes may be made in the board layout in Allegro PCB Editor:

- Adding components
- Editing connectivity
- Renaming reference designators
- Swapping sections

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- Swapping differential pairs
- Swapping pins
- Updating property values
- Updating electrical constraints
- Adding, deleting or editing terminations

These changes need to be updated in the logical design. You can run *Import Physical* to update the logical design with the changes in the board. *Import Physical* lets you update the logical design in the following two ways.

- Update the changes in the board to the logical design.
- Update the changes from the feedback files that were generated during a previous run of *Import Physical* to the logical design.

When you run *Import Physical*, differences between the logical design and the board are displayed in the Visual Design Differences pane. The Visual Design Differences pane lets you view and update all the design differences between the logical design and the board. For more information on using the Visual Design Differences pane, see [Running Visual Design Differences](#) on page 481.

Note: You cannot update the board using the Visual Design Differences pane.

Preparing to Update the Logical Design with the Changes in the Board

Before you run *Import Physical* to update the logical design with the changes in the board, do the following:

- Define the user-defined properties (that you have set up as transferable between System Connectivity Manager and the board in the [Property Flow](#) tab of the [Setup](#) dialog box) that are added on components and pins in the design in a `pxlBA.txt` file located in the physical view of the root (top-level) design for the project. This is required to ensure that the user-defined properties you set up as transferable between System Connectivity Manager and PCB Editor are passed automatically from the board to the design in System Connectivity Manager.

Note: When you run *Import Physical*, the predefined properties that are set up as transferable between System Connectivity Manager and the board are automatically passed from the board to the logical design in System Connectivity Manager.

- If you have assigned signal integrity (SI) models to components, pins or nets in the board, ensure that the libraries containing the models are setup for your project in System Connectivity Manager by doing the following:

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- a. In Allegro PCB Editor or Allegro PCB SI, choose *Analyze – SI/EMI Sim – Model Dump/Refresh*.

The Model Dump/Refresh dialog box appears.

- b. Click the *Dump* button.

All the models assigned in the board are written to the `<boardname>.dml` file in the directory in which the board file is located. For example, if the name of the board file is `memb1k.brd`, the `memb1k.dml` file is created when you click the *Dump* button.

- c. Open your project in System Connectivity Manager and choose *Tools – Signal Integrity – SI Library Setup*.

The Library Setup (SI Analysis) dialog box appears.

- d. Add the `.dml` file generated from the board and click *OK*.

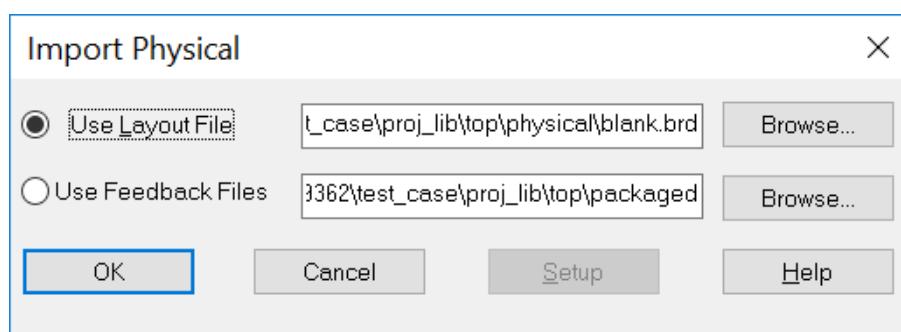
For more information on setting up SI model libraries in System Connectivity Manager, see [Setting Up SI Model Libraries](#) on page 320.

Updating the Logical Design with the Changes in the Board

To update the logical design with the changes in the board

1. From the *Project* menu in System Connectivity Manager, choose *Import Physical*.

The Import Physical dialog box appears displaying the path to the last created board file.

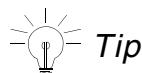


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2. Select the option for updating the logical design with the changes in the board.

Select	To
Use Board File	Update the logical design with the changes in the specified board file. Enter the name of the board file whose changes you want to update to the logical design, or click Browse to select the board file.
Use Feedback Files	Update the logical design with the changes in the feedback files created during a previous run of <i>Import Physical</i> .



Tip

You can also run Export Logic (choose *File – Export – Logic*) in Allegro PCB Editor to generate the feedback files. For more information on running Export Logic, see the *Allegro PCB and Package User Guide: Transferring Logic Design Data*.

3. Click *OK* to display the differences between the logical design and the board in the Visual Design Differences pane.

The Visual Design Differences pane lets you view and update all the design differences between the logical design and the board. For more information, see [Running Visual Design Differences](#) on page 481.

Note the following:

- If a signal that is not connected to any component pin exists in System Connectivity Manager, the difference is not reported in the Visual Design Differences pane.
- If a component is in the board but is not in System Connectivity Manager, the difference will be reported in the Visual Design Differences pane only if the component was added using the *Concept Components* browser in the Parts List dialog box (to access the Parts List dialog box in Allegro PCB Editor, choose *Logic – Part Logic*).

Updating the Logical Design with the Connectivity Changes

You can use the *Import ECO Netlist* command to import the connectivity changes in System Connectivity Manager. To successfully import the connectivity changes, the connectivity data in the netlist file must be stored using format shown below.

```
<refdes>.<pin_number> <signal_name>
```

Sample format for a file that can be imported using *Import ECO Netlist* command is shown in the figure given below.

```
D2.1 N1  
D2.2 N2  
D2.4 N4  
D2.5 N6  
D3.1 N6
```

The `<refdes>.<pin_number>` together represent the pin to which the signal is connected. For the connectivity data to be imported successfully, component pins must be specified using the reference designators and pin number separated by a period. Therefore, the statement `D2.1 N1` implies that signal `N1` is connected to pin 1 of a component for which reference designator is `D2`.

The pin data is separated from the `signal_name` using space as the delimiter. Any other delimiter is not supported. Signal names should also be as per the guidelines.

Note: To know about the guidelines for specifying valid signal names, see [Signal Naming Conventions](#) on page 144.

Importing ECO Netlist

The *Import ECO Netlist* command supports importing connectivity changes such as addition or deletion of pin net connections and addition of new nets. This section covers some of the same scenarios in which connectivity changes can be imported using the *Import ECO Netlist* command.

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Transferring the Logical Design to a Board and Design Synchronization

Case 1: Change in the connectivity due to addition of a new net.

The design connectivity, along with the connectivity changes are listed below.

Design Connectivity	Connectivity changes	Connectivity ECO Netlist
U2.1 net1	U3.1 abc	U2.1 net1
U2.2 net2	U3.2 net1	U2.2 net2
U2.4 net3		U2.4 net3
U2.5 net5		U2.5 net5
U3.1 net4		U3.1 abc U3.2 net1

In Case 1, a new net, abc, is connected to pin1 of the component with RefDes U3 and a new pin-net connection is created for pin U3.2. When you import these changes, the pin-net connection for U3.1 is modified and a new net is added to the design. If net4 is connected to any other pin, that connection is not modified, and the updated design has both the nets, net4 and abc. If net4 is not connected to any pin, even then it is not removed from the design and is reported as an unconnected net.

Case 2: Changes in the connectivity due to deletion of a pin-net connection.

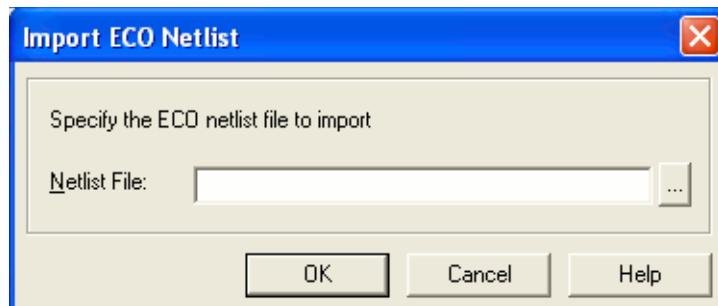
If you remove the connection of net 2 from U2.2 and connect the net to a new component U7.1, the changes will be as shown below. The assumption here is that the component with RefDes U7 is a new component and was not available in the design.

Design Connectivity	Connectivity changes	Connectivity ECO Netlist
U2.1 net1	U2.2	U2.1 net1
U2.2 Net2	U7.1 Net2	U2.2
U2.4 net4		U2.4 net4
U2.5 Net5		U2.5 Net5
U3.1 net4		U3.1 net4

Note that of the two changes, only the deletion of pin-net connection is imported in the design. The design is not updated with the change due to new pin-net connection U7.1 Net2. This is because the *Import ECO Netlist* command cannot be used to import differences related to addition or deletion of components.

To import connectivity changes

1. From the *File* menu, choose *Import ECO Netlist*.



2. In the Import ECO Netlist dialog box, use the browse button to select the file with connectivity changes.
3. Click *OK* to import the changes.

The changes being imported from the connectivity file are displayed in the Visual Design Differences pane. You can review these changes and then update the design with the changes.

Note: Release 17.0 onwards, you cannot choose the changes that you want to update. When updating a design, all changes will be updated.

To know how to use the Design Differences window, see [The Visual Design Differences Pane User Interface](#) on page 483.

Limitations of using the Import ECO Netlist command

The *Import ECO Netlist* command can only be used to import connectivity changes. Any differences related to addition or deletion of components, deletion of nets, changes in the connectivity of associated components, property modifications, and changes in schedule of a net cannot be imported.

For example, if you have added split part as a symbol in your design and a new pin-net connection has been added to a pin for which the symbol is not added to your design. If you now use the *Import ECO Netlist* command, the missing component and the new connection

will be reported as design differences. But the design update process will fail. To import such design changes, you first add the missing component to your design and then use the *Import ECO Netlist* command to update the design.

Similarly, if you change the pin-net connection of a resistor used as series termination, the connectivity changes will not be imported. This is because connectivity changes in the associated components, such as, terminations, pullups and pulldowns, and bypass capacitors, are not handled by the *Import ECO Netlist* command.

Running Visual Design Differences

You can use the Visual Design Differences pane in System Connectivity Manager to view the differences between the logical design and the board and update the differences in the logical design in System Connectivity Manager.

The following types of differences are displayed in the Visual Design Differences pane:

- Component, pin, net, reference designator, pin connectivity and termination differences.
- Property differences for components, nets, or pins.
- Swapping differences for functions, pins, reference designators, or differential pairs.
- Constraint, constraint object and constraint association differences.

The differences are grouped under various categories for easier viewing. For information on the categories of design differences and the types of differences that belong to each category, see [Difference Categories](#) on page 488. For information on displaying only the differences belonging to a particular category in the Visual Design Differences pane, see [Filtering Design Differences](#) on page 487.

You can update the entire logical design. For more information, see [Updating Design Differences in SCM](#) on page 484.

Note: You cannot update the board using the Visual Design Differences pane. To update the board with the changes in the logical design, you must run *Export Physical*. For more information on running *Export Physical*, see [Updating the Board with the Changes in the Logical Design](#) on page 469.

The following sections describe how you can use the Visual Design Differences pane to update design differences.

- [Viewing the Visual Design Differences Pane](#) on page 482
- [The Visual Design Differences Pane User Interface](#) on page 483

- [Updating Design Differences in SCM on page 484](#)
- [How Differences are Updated in System Connectivity Manager on page 486](#)
- [Filtering Design Differences on page 487](#)
- [Highlighting and Dehighlighting Objects on page 488](#)

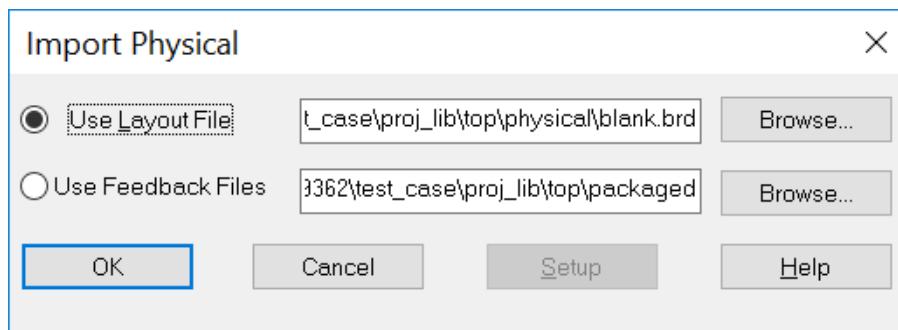
Viewing the Visual Design Differences Pane

To view differences between the logical design and the board, do the following:

1. From the *Project* menu in System Connectivity Manager, choose *Import Physical*.

System Connectivity Manager prompts you to save your design if there are any unsaved changes in the design.

The Import Physical dialog box appears.



2. Select the board file to compare the logical design with the latest changes in the selected board file. Enter the name of the board file or click *Browse* to select the board file.

When you run *Import Physical* with this option selected, `genfeedformat` generates the feedback files (`*view.dat` files) for the board. The packaging files (`pst*.dat` files) for the logical design are compared with the feedback files to report the differences in the Visual Design Differences pane. For more information on the packaging and feedback files, see [System Connectivity Manager to Allegro PCB Editor Flow on page 467](#).

3. If required, specify or select a feedback file by browsing to a directory. When you run *Import Physical* with this option selected, the packaging files (`pst*.dat` files) for the logical design are compared with the feedback files created during a previous run of *Import Physical* (with the *Use Board File* option selected) in System Connectivity Manager, or a previous run of *Export Logic* (choose *File – Export – Logic*) in Allegro PCB Editor, to report the differences in the Visual Design Differences pane.

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For more information on the packaging and feedback files, see [System Connectivity Manager to Allegro PCB Editor Flow](#) on page 467.

4. Click *OK* to display the differences between the logical design and the board in the Visual Design Differences pane.

The Visual Design Differences pane is displayed in the bottom half of the System Connectivity Manager workspace.

The Visual Design Differences Pane User Interface

Figure 18-2 Visual Design Differences Pane

Filter:		Update	Options	
	Status	Object	Logical Design(top)	Physical Design(blank.brd)
Component Differences (4/0)				
		D1 (prelmc100e34d)	✓	✗
		D3 (74c393)	✓	✗
		D4#1 (74hc4059)	✓	✗
Net Differences (6/0)				
		A	✓	✗

Table 18-1 Icons in the Visual Design Differences Pane

Icon	Description
ⓘ	Appears in the (ⓘ) column if an object in the <i>Object</i> column has other design differences. If you click ⓘ next to an object, the related design differences are displayed in the <i>Collections</i> or <i>Dependencies</i> dialog box. All these other differences are updated along with the object differences when you click the <i>Update</i> button.
✓	Appears in the <i>Logical Design</i> or <i>Physical Design</i> column and indicates that the object (component, net, or constraint object) exists in SCM or in the board. For example, if a component exists in SCM but does not exist in the board, the <i>Logical Design</i> column displays this icon (✓) next to the component.

Table 18-1 Icons in the Visual Design Differences Pane

Icon	Description
	Appears in the <i>Logical Design</i> or <i>Physical Design</i> column and indicates that the object (component, net, or constraint object) does not exist either in SCM or in the board. For example, if a component does not exist in SCM but exists in the board, the <i>Logical Design</i> column displays this icon () next to the component.
	Appears next to the difference in the <i>Status</i> column if a difference is successfully updated in SCM.
	Appears next to the difference in the <i>Status</i> column if the update of a difference fails.

Updating Design Differences in SCM

In SCM, you can update all or selected design differences using the *Visual Design Differences* pane.

Note: You cannot update the board using the Visual Design Differences pane. To update the board with the changes in the logical design, you must run *Export Physical*. For more information on running *Export Physical*, see [Updating the Board with the Changes in the Logical Design](#) on page 469.



If there are already renamed global signals in the board, it is recommended that you do not update them in the logical design. If you want to rename global signals, it is recommended that you rename them in the logical design and not on the board.

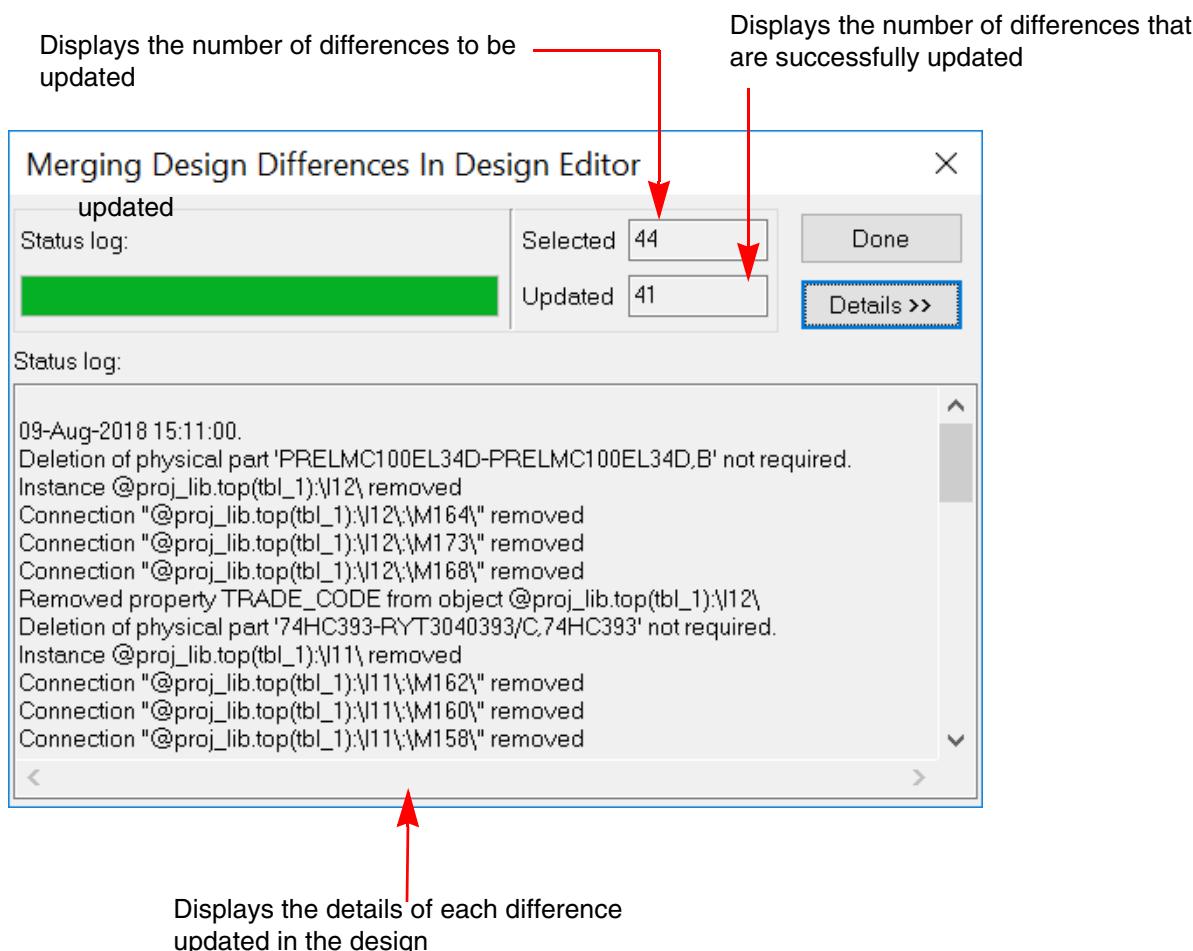
To update all design differences, do the following:

1. Click the *Update* button.

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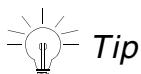
Transferring the Logical Design to a Board and Design Synchronization

The *Merging Design Differences in Design Editor* box appears displaying the progress of the update process.



2. Click *Done* to close the *Merging Design Differences in Design Editor* box.

If a difference is updated successfully, this icon (✓) appears next to the difference in the *Status* column and the difference is grayed out. If the update of a difference fails, this icon (✗) appears next to the difference in the *Status* column.



You can also select a row, right-click and choose *Update* from the shortcut menu to quickly update a difference. To view the details of the update, right-click and choose *Show Log* from the shortcut menu. The details of the update process are displayed in the *Detail Log* dialog box.

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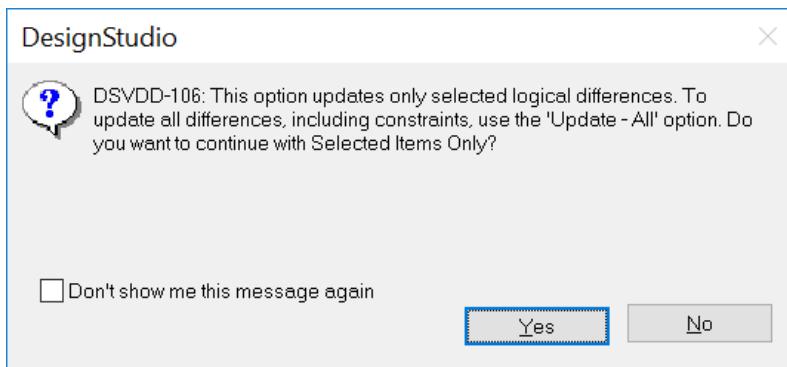
Transferring the Logical Design to a Board and Design Synchronization

To update selected design differences, do the following:

1. Choose *Update — Selected Items Only* in the *Visual Design Differences* pane.

Note: This option is enabled only if the `ENABLE_SEL_LOGICAL_UPDATE_VDD` directive is set to ON in the `.cpm` file. For more information about the directive, refer to the `ENABLE_SEL_LOGICAL_UPDATE_VDD` section of *Allegro Front-End CPM Directive Reference Guide*.

The following confirmation message appears:



2. Click Yes.

The *Merging Design Differences in Design Editor* box appears displaying the progress of the update process.

Note: Constraint differences cannot be updated with this option. Choose *Update — All* to update constraint differences.

3. Click *Done* to close the *Merging Design Differences in Design Editor* box.

All the selected design differences are updated.

How Differences are Updated in System Connectivity Manager

Note the following when you update the differences in the Visual Design Differences pane.

- If a difference is caused by a change that happened only in System Connectivity Manager and not in the board and you update differences, the change in System Connectivity Manager is deleted.

For example, if a constraint exists in System Connectivity Manager but not in the board, the constraint in System Connectivity Manager will be deleted if you update differences. Similarly, if a component exists in System Connectivity Manager but not in the board, the component in System Connectivity Manager will be deleted if you update differences.

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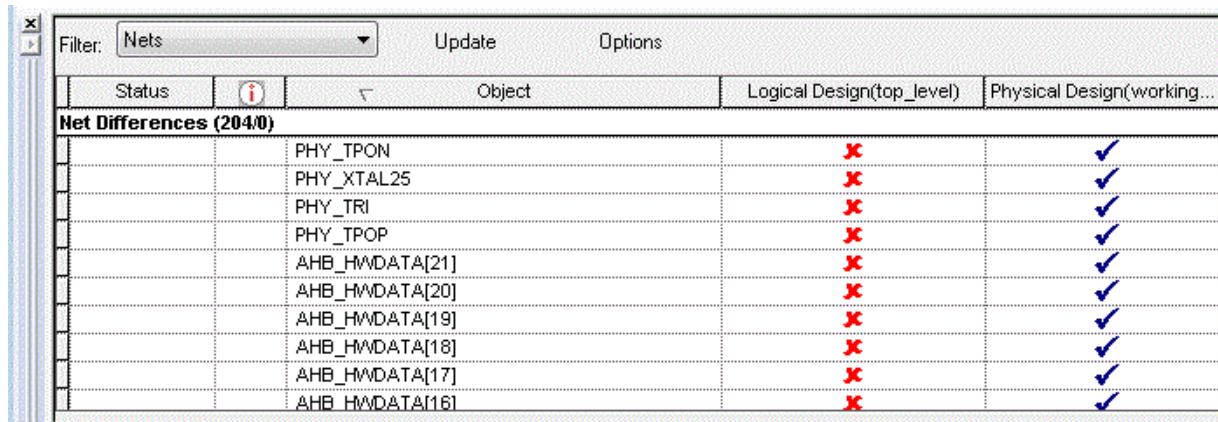
- If the difference is caused by a change in both System Connectivity Manager and in the board and you update differences, the changes in System Connectivity Manager are overwritten by the changes in the board.
- If there are differences for a component or net that exists in the board but not in System Connectivity Manager, you need to run *Export Physical* to update the board. If you do not run *Export Physical*, these differences will be reported in the Visual Design Differences pane when you run *Import Physical* later because of differences in canonical paths for the component or net.
- You can only update property and electrical constraint differences in schematic blocks, read-only blocks, and replicated blocks (blocks added more than once in the design) used in the design. The property and electrical constraint differences will be updated in the property file of the root design. You cannot update component and connectivity differences in read-only blocks, schematic blocks and replicated blocks.

Filtering Design Differences

You can filter the design differences to view differences that belong to a particular category in the Visual Design Differences pane.

1. To filter design differences, select the category for which you want to view the differences in the *Filter* drop-down list.

For example, if you select *Nets* in the *Filter* drop-down list, only net-related differences are displayed, as shown in the following figure.



The screenshot shows a software interface for managing design differences. At the top, there is a toolbar with a close button (X), a back arrow, and a forward arrow. Below the toolbar is a menu bar with 'Filter' (set to 'Nets'), 'Update', and 'Options'. A status bar at the bottom indicates 'Net Differences (204/0)'.

Status	Object	Logical Design(top_level)	Physical Design(working...)
	PHY_TPON	X	✓
	PHY_XTAL25	X	✓
	PHY_TRI	X	✓
	PHY_TPOP	X	✓
	AHB_HWDATA[21]	X	✓
	AHB_HWDATA[20]	X	✓
	AHB_HWDATA[19]	X	✓
	AHB_HWDATA[18]	X	✓
	AHB_HWDATA[17]	X	✓
	AHB_HWDATA[16]	X	✓

2. To view all design differences, select *All* in the *Filter* drop-down list.

Highlighting and Dehighlighting Objects

You can highlight or dehighlight the object (component, pin, or constraint object) corresponding to a difference. The object is highlighted in System Connectivity Manager. If you have opened Constraint Manager from System Connectivity Manager (choose *Design – Edit Constraints* in System Connectivity Manager), the object is highlighted in Constraint Manager.

Note: Signals are highlighted only in the Signal List and not in Constraint Manager. Click on the highlighted signal in the Signal List to highlight the signal in Constraint Manager.

Highlighting Objects

To highlight the object corresponding to a selected difference:

1. Select the difference in the Visual Design Differences pane.
2. Do one of the following:
 - Choose *Options – Highlight*.
 - Right-click and choose *Highlight* from the shortcut menu.

The object is highlighted in System Connectivity Manager. If you have launched Constraint Manager from System Connectivity Manager, the object is highlighted in Constraint Manager if the difference is a property, constraint, constraint object, or constraint association difference.

Dehighlighting Objects

To dehighlight the object corresponding to a selected difference:

1. Select the difference in the Visual Design Differences pane.
2. Do one of the following:
 - Choose *Options – Dehighlight*.
 - Right-click and choose *Dehighlight* from the shortcut menu.

The object is dehighlighted in System Connectivity Manager and Constraint Manager.

Difference Categories

The various types of design differences are grouped under the following categories.

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- [Component Differences](#) on page 490
- [Net Differences](#) on page 491
- [Reference Designator Differences](#) on page 492
- [Section Differences](#) on page 492
- [Pin Differences](#) on page 493
- [Connectivity Differences](#) on page 494
- [Differential Pair Differences](#) on page 494
- [Design Differences](#) on page 494
- [Design Constraint Differences](#) on page 495
- [Constraint Object Differences](#) on page 498
- [Constraint Association Differences](#) on page 499
- [Physical Part Differences](#) on page 501

The categories of design differences and the types of differences that belong to each category are described below.

Component Differences

Displays the following differences between components in the logical design and the board.

Difference	Description
Component Differences	<p>This difference occurs if a component exists in logical design but does not exist in the physical design, or vice versa. For example, if a component exists in System Connectivity Manager but not in the board, this difference occurs.</p> <p>When a component difference occurs, the <i>Object</i> column in the Visual Design Differences pane displays the component name as, for example:</p> <ul style="list-style-type: none">■ U2 (i5) if you have added the component as a package, where U2 is the reference designator and i5 is the instance name of the component.■ U4#3 (i5) if have added the component as a symbol, where U4 is the reference designator, 3 refers to the section number of the component, and i5 is the instance name of the component.
Component Property Differences	<p>This difference occurs if a property on a component exists in logical design but does not exist in the physical design, or vice versa, or if there is a difference between the value of the property on the component in the logical design and the value of the property on the component in physical design.</p> <p>For example, this difference occurs if a property <code>BOM_IGNORE=TRUE</code> exists on a component in System Connectivity Manager but does not exist on the component in the board.</p>
Component PhysPart Changed	<p>This difference occurs if the physical part name of a component is not the same in both logical design and the physical design.</p> <p>For example, this difference occurs if the physical part name (represented by the <code>PART_NAME</code> property) of a component in System Connectivity Manager is <code>LM101-BASE</code> and the physical part name of the component in the board is <code>LM-BASE</code>.</p>

Net Differences

Displays the following differences between nets in the logical design and the physical design.

Difference	Description
Net Differences	This difference occurs if a net exists in the logical design but does not exist in the physical design, or vice versa. Note: Differences in NC nets are not reported.
Net Physical Net Name Changed	This difference occurs if there is a difference between the physical net name (represented by the <code>PHYS_NET_NAME</code> property) of a net in the logical design and the physical net name of the corresponding net in the physical design.
Net Property Changed	This difference occurs if a property on a net exists in the logical design but does not exist in the physical design, or vice versa, or if there is a difference between the value of the property on the net in the logical design and the value of the property on the net in physical design. For example, this difference occurs if a property <code>VOLTAGE=5</code> exists on a net in System Connectivity Manager but does not exist on the net in the board.
Net Class Differences	This difference occurs if a net class exists in the logical design but does not exist in the physical design, or vice versa.
Net Swap	This difference occurs when you swap nets on the physical design. This is also reported when you perform a differential pair polarity swap on a packaged or BGA component. Note: If property <code>ALLOW_CONN_SWAP</code> is FALSE, all net swaps on the physical design are handled as Pin Swaps. For more information see <i>Allegro Platform Properties Reference</i> guide.

Reference Designator Differences

Displays the following differences in reference designators in the logical design and the physical design.

Difference	Description
Reference Designator Renamed	<p>This difference occurs if there is a difference between the reference designator of a component in the logical design and the component in the physical design.</p> <p>For example, if the reference designator is U1 in System Connectivity Manager and U8 in the board, this difference occurs.</p>
Reference Designator Swapped	<p>This difference occurs if you have done a component swap in the physical design but the swap is not reflected in the logical design.</p>

Section Differences

Displays the following differences in sections in the logical design and the physical design.

Difference	Description
Section Changed	<p>This difference occurs if the section number of a component (represented by the SEC property) is not the same in both the logical design and the physical design.</p> <p>For example, this difference occurs if the component U1 has the section number 1 in the logical design and the same component has the section number 2 in the physical design.</p>
Section Swap	<p>This difference occurs if there are section-swapping differences between the logical design and the physical design.</p> <p>For example, this difference occurs if you swap section 1 of component U1 with section 2 of the same component in the board but do not do the same in System Connectivity Manager.</p>

Pin Differences

Displays the following differences in pins in the logical design and the physical design.

Difference	Description
Pin Change	This difference occurs if the pin number of a pin on a component is not the same in both the logical design and the physical design.
Pin Swap	<p>This difference occurs if there are pin-swapping differences between the logical design and the physical design.</p> <p>For example, this difference occurs if you swap pin U1.1 with U1.5 in the board but do not do the same in System Connectivity Manager.</p> <p>This change is also indicated in case you perform a differential pair polarity swap on a non-packaged component on the board.</p> <p>Note: If property ALLOW_CONN_SWAP is TRUE, pin swaps on the board are handled as Net Swaps. For more information see <i>Allegro Platform Properties Reference</i> guide.</p>
Pin Property Changed	<p>This difference occurs if a property on a pin exists in the logical design but does not exist in the physical design, or vice versa, or if there is a difference between the value of the property on the pin in the logical design and the value of the property on the pin in the physical design.</p> <p>For example, this difference occurs if the NO_DRC property exists on a pin in the board but does not exist on the pin in System Connectivity Manager.</p>
Termination Differences	This difference occurs if you have added, say, a shunt termination on a pin in the logical design but the termination does not exist on the pin in the physical design, or vice versa.
Termination Modification Differences	This difference occurs if a termination added on a pin is modified in the logical design but not modified in the physical design, or vice versa.

Connectivity Differences

Displays the pin-net connectivity differences between the logical design in System Connectivity Manager and the physical design.

Differential Pair Differences

Displays the following differences in Differential Pairs in the logical design and the physical design.

Difference	Description
Differential Pair Swap	<p>This difference occurs when you swap two differential pairs in the physical design. Swapping two differential pairs in the physical design swaps one end of the differential pair, from one set of pins to another set.</p> <p>For example, if U1.1(A+) and U2.2(A-) comprise differential pair DP_A, and U1.4(B+) and U1.5(B-) comprise differential pair DP_B, swapping these two on the board will display the changed pin numbers. DP_A will be connected to U1.4(A+) and U1.5(A-) while DP_B will be connected to U1.1(B+) and U1.2(B-).</p> <p>Note: A differential pair swap is not detected in the absence of differential pair pins. This difference is reported only in the case of setup-defined, library-defined, and model-defined differential pairs. User-defined differential pair swaps are reported as connectivity differences.</p>

Design Differences

Displays the following differences in the design between the logical design and the physical design.

Design Unit Differences	This difference occurs if the design units or precision that exists in the logical design is not identical to that in the physical design.
Layer Stackup Changed	This difference occurs if the stackup that exists in the logical design is not identical to that in the physical design.

Design Constraint Differences

Displays the following differences in constraints in the logical design and the physical design.

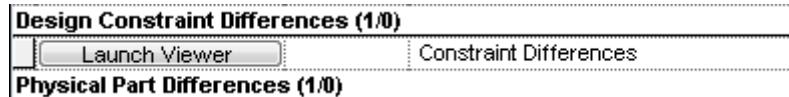
Difference	Description
Bus Constraint Differences	Displays the differences between constraints on bus objects in the logical design and the physical design.
Match Group Constraint Differences	Displays the differences between constraints on match groups in the logical design and the physical design.
Net Constraint Differences	Displays the differences between constraints on nets in the logical design and the physical design. For example, Min value of the Min First Switch timing constraint on a net in System Connectivity Manager is 0.25, 0.26 and the value of the constraint on the same net in the board is 0.24 : 0.26, MIN_FIRST_SWITCH=0.25, 0.26 is displayed in the <i>System Connectivity Manager</i> column and MIN_FIRST_SWITCH=0.24, 0.26 is displayed in the <i>Allegro</i> column.
Pin Constraint Differences	Displays the differences between constraints on pins in the logical design and the physical design.
XNet Constraint Differences	Displays the differences between constraints on XNets in the logical design and the physical design.
Pin Pair Constraint Differences	Displays the differences between constraints on pin pairs in the logical design and the physical design.
Diff Pair Constraint Differences	Displays the differences between constraints on differential pairs in the logical design and the physical design.
ECSet Constraint Differences	Displays the differences between the constraints in ECSets in the logical design and the physical design.
ECSet Pin Pair Constraint Differences	Displays the differences between the constraints on pin pairs created by assigning an ECSet in the logical design and the physical design.
ECSet Match Group Constraint Differences	Displays the differences between the constraints on match groups created by assigning an ECSet in the logical design and the physical design.
Net Class Constraint Differences	Displays the differences between the constraints on Net Classes in the logical design and the physical design.

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Difference	Description
Net Class-Class Constraint Difference	Displays the differences between the constraints on Net Class-Class objects in the logical design and the physical design.
Region Constraint Differences	Displays the differences between the constraints on Regions in the logical design and the physical design.
Region Class Constraint Differences	Displays the differences between the constraints on Region Classes in the logical design and the physical design.
Region Class-Class Constraint Differences	Displays the differences between the constraints on Region Class-Class objects in the logical design and the physical design.
PCSet Constraint Differences	Displays the differences between the constraints on PCSets in the logical design and the physical design.
SCSet Constraint Differences	Displays the differences between the constraints on SCSets in the logical design and the physical design.
SNSCSets Constraint Differences	Displays the differences between the constraints on SNSCSets (SameNet Spacing CSet) in the logical design and the physical design.
Layer Constraint Differences	Displays the differences between the constraints on layers in the logical design and the physical design.

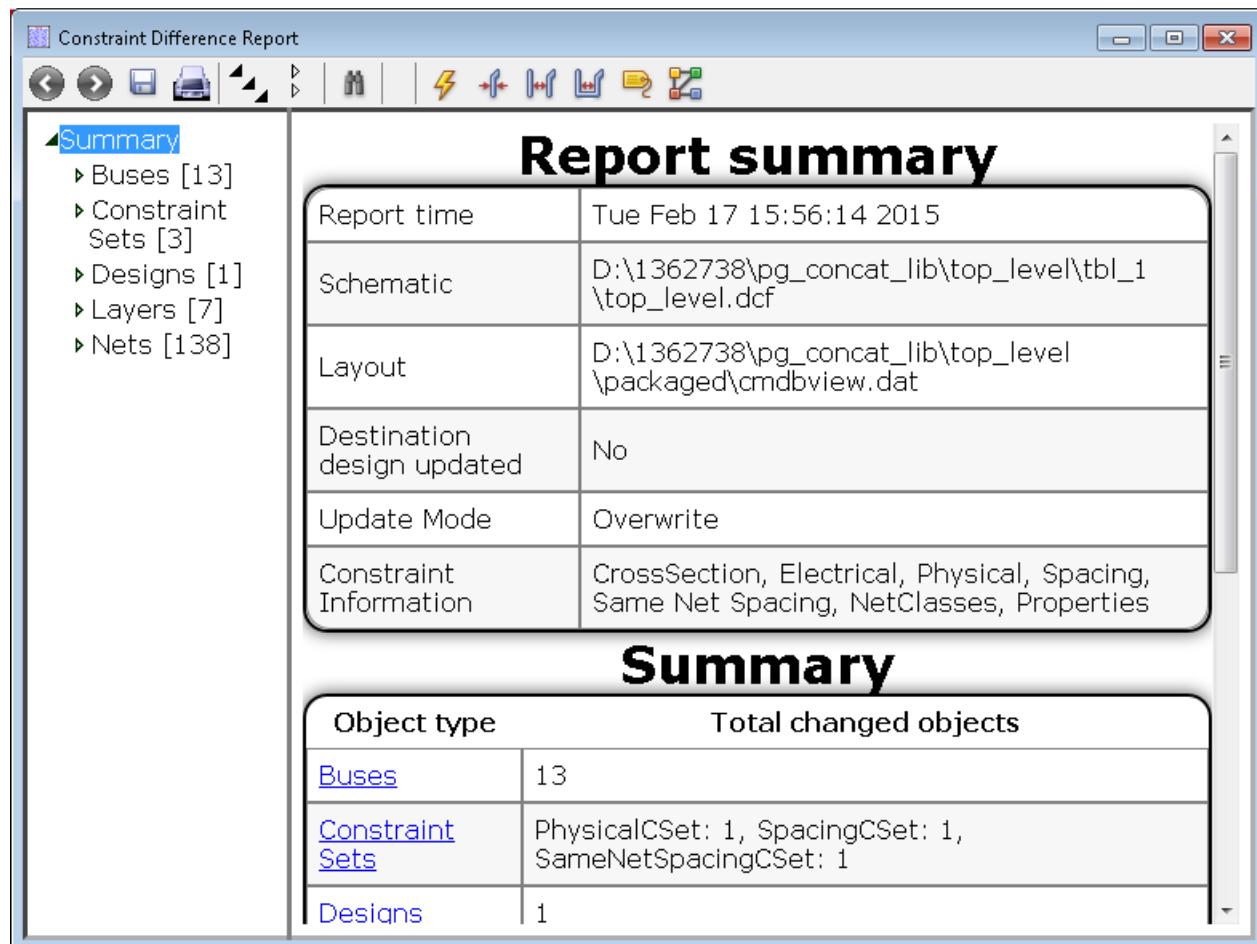
You can click the Launch Viewer button to view a report of all the constraint differences.



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When you click the button, the Constraint Different Report dialog is displayed.



You can click on each object type in the Summary box for details of the differences.

Constraint Object Differences

Constraint object differences occur if a constraint object does not exist in both the logical design and the physical design. For example, this difference occurs if an ECSet named DATA exists in System Connectivity Manager but not in the board.

Difference	Description
Diff Pair Rename Differences	This difference occurs if a differential pair in both the logical design and the physical design was renamed in the physical design but was not renamed in the logical design, or vice versa. For example, this difference occurs if you rename the differential pair DP_VCLK to DP_VCLK1 in the logical design but do not do the same in the physical design.
EC Set Differences	This difference occurs if an ECSet exists in the logical design but does not exist in the physical design, or vice versa.
EC Set Rename Differences	This difference occurs if an ECSet existing in both the logical design and the physical design was renamed in the physical design but not renamed in the logical design, or vice versa.
EC Set Pin Pair Differences	Displays the differences for pin pairs created by assigning an ECSet in the logical design and the physical design.
ECSet Match Group Differences	Displays the differences for match groups created by assigning an ECSet in the logical design and the physical design.
Net Class Differences	This difference occurs if a Net Class exists in the logical design but does not exist in the physical design, or vice versa.
Net Class Rename Differences	This difference occurs if a Net Class existing in both the logical design and the physical design was renamed in the physical design but not renamed in the logical design, or vice versa.
Net Class-Class Differences	This difference occurs if a Net Class-Class object exists in the logical design but does not exist in the physical design, or vice versa.
Region Class Differences	This difference occurs if a Region Class exists in the logical design but does not exist in the physical design, or vice versa.
Region Class-Class Differences	This difference occurs if a Region Class-Class object exists in the logical design but does not exist in the physical design, or vice versa.

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Difference	Description
PCSet Differences	This difference occurs if a PCSet exists in the logical design but does not exist in the physical design, or vice versa.
PCSet Rename Differences	This difference occurs if a PCSet existing in both the logical design and the physical design was renamed in the board but not renamed in the logical design, or vice versa.
SCSet Differences	This difference occurs if a SCSet exists in the logical design but does not exist in the physical design, or vice versa.
SCSet Rename Differences	This difference occurs if a SCSet existing in both the logical design and the physical design was renamed in the board but not renamed in the logical design, or vice versa.
SNSCSet Differences	This difference occurs if a SNSCSet exists in the logical design but does not exist in the physical design, or vice versa.
SNSCSet Rename Differences	This difference occurs if a SNSCSet existing in both the logical design and the physical design was renamed in the physical design but not renamed in the logical design, or vice versa.

Constraint Association Differences

Displays the following differences in constraint associations between the logical design and the physical design.

Difference	Description
Bus Association Differences	<p>This difference occurs if:</p> <ul style="list-style-type: none">■ A bus object exists in the logical design but does not exist in the physical design, or vice versa.■ The members of a bus in the logical design and the members of the same bus in the physical design are different.■ A bus object existing in both the logical design and the board was renamed in the physical design but not renamed in the logical design.
Pin Pair Association Differences	This difference occurs if the pins forming a pin pair in the logical design and the pins forming the same pin pair in the physical design are different.

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Difference	Description
Diff Pair Association Differences	<p>This difference occurs if:</p> <ul style="list-style-type: none">■ A differential pair object is in the logical design but is not in the physical design, or vice versa.■ The members of a differential pair in the logical design and the members of the same differential pair in the physical design are different. <p>For example, this difference is displayed if the nets <code>DATA</code> and <code>CLK</code> are members of the differential pair <code>DP1</code> in System Connectivity Manager but the differential pair <code>DP1</code> in the board has the nets named <code>DATA</code> and <code>ADDR</code> as its members.</p>
Match Group Association Differences	<p>This difference occurs if:</p> <ul style="list-style-type: none">■ A match group exists in the logical design but does not exist in the physical design, or vice versa.■ The members of a match group in the logical design and the members of the same match group in the physical design are different.
XNet Membership Changed	This difference occurs if the nets forming the XNet in the logical design are different from the nets forming the XNet in the physical design.
Net Class Association Differences	The difference occurs if the members of a net class in the logical design and the members of the net class in the physical design are different.
Net Class-Class Association Differences	The difference occurs if the members of a net class-class in the logical design and the members of the net class-class in the physical design are different.
Region Class Association Differences	The difference occurs if the members of a region class in the logical design and the members of the region class in the physical are different.
Region Class-Class Association Differences	The difference occurs if the members of a region class-class in the logical design and the members of the region class-class in the physical design are different.
PCSet Association Differences	The difference occurs if the members of a PCSet in the logical design and the members of the PCSet in the physical design are different.

Difference	Description
SCSet Association Differences	The difference occurs if the members of a SCSet in the logical design and the members of the SCSet in the physical design are different.
SNSCSet Association Differences	The difference occurs if the members of a SNSCSet in the logical design and the members of the SNSCSet in the physical design are different.

Physical Part Differences

Displays the physical differences in the parts that have same reference designators and connectivity in the logical design and in the physical design.

This difference occurs if the physical part name of a component is not the same in both the logical design and the physical design. For example, this difference occurs if the physical part name (represented by the `PART_NAME` property) of a component in System Connectivity Manager is `LM101-BASE` and the physical part name of the component in the board is `LM-BASE`.

Pin Swap in the back-to-front flow

Pin swaps on the board can be reported as either a pin swap or a net swap, depending on the following criteria:

- `ALLOW_CONN_SWAP` property. For details on this property, see *Property Reference Guide*.
- Component type: Co-design or non co-design.
- Whether the component pin name is the same as the pin number.

Pin Swap and Net Swap matrix

Net Swaps are meant for cases where the pin name is the same as the pin number. Net swaps retain the pin name and number naming consistency.

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	Co-design components	Components where Pin name is equal to Pin number	Components where Pin name is not equal to pin number
ALLOW_CONN_SWAP is not present	Pin Swap	Net Swap	Pin Swap
ALLOW_CONN_SWAP = True	Net Swap	Net Swap	Net Swap
ALLOW_CONN_SWAP = False	Pin Swap	Pin swap	Pin Swap

Note: Net swaps are not performed in the following cases:

- For parts that belong to read-only, concept, or reuse blocks.
- If parent differential pair pins have terminations attached.

Running Design Rule Checks

System Connectivity Manager lets you run design rule checks (DRCs) to identify connectivity and other errors in the design.

System Connectivity Manager provides a standard set of DRCs, and also lets you write your own custom DRCs in the Tcl language and run the custom DRCs from System Connectivity Manager.

You can enable or disable individual DRCs. When you run DRCs, the DRC errors are reported in the Violations window. You can also set the error severity level — Error, Warning or Information — to be reported in the Violations window if an enabled DRC fails. For example, if you set the error severity level for the Unconnected Nets DRC as Warning, System Connectivity Manager displays warning messages for each unconnected net in the Violations window.

Standard DRCs Provided with System Connectivity Manager

The following standard DRCs are provided with System Connectivity Manager. These standard DRCs are implemented as Tcl procedures. The implementations of the standard DRCs are in the `/share/cdssetup/tdd/rules` folder as `.tcl` files in your Cadence installation.

Table 19-1 Standard DRCs provided with System Connectivity Manager

DRC Name	Description
JEDEC Type	Checks that the <code>JEDEC_TYPE</code> property exists on every instance in the design.
Unconnected Nets	Reports signals that are not connected to any object.
Single Node Nets	Checks that every signal has at least two nodes (pins) attached to it.

Table 19-1 Standard DRCs provided with System Connectivity Manager

DRC Name	Description
Unconnected Pins	Reports all instances of unconnected pins in the design.
Missing Functions	Reports functions of an asymmetrical part that are not instantiated in the design.
Missing Section on a Split Part	Reports the sections of a split part that are not instantiated in the design.

Creating Custom DRCs

You can write your own DRCs in Tcl and run the custom DRCs from System Connectivity Manager.

To create a custom DRC for System Connectivity Manager

1. Write a Tcl procedure for the custom DRC and place the .tcl file containing the procedures in the `\share\cdssetup\tdd\custom_rules` folder in your Cadence installation, or `CDS_SITE` location.
2. Create a Tcl index for the .tcl files containing the procedures for the custom DRCs. For more information, see [Creating a Tcl Index for Custom DRC Tcl Files](#) on page 504.
3. Create or update the `custom_drc.txt` file. System Connectivity Manager reads the `custom_drc.txt` file to display the custom DRCs in the [Design Rule Checks](#) tab of the [Setup](#) dialog box. You can then enable or disable the custom DRCs for a design. For more information, see [Displaying the Custom DRCs in System Connectivity Manager](#) on page 505.

Creating a Tcl Index for Custom DRC Tcl Files

To create a Tcl index for custom DRC Tcl files

1. Place the .tcl files containing the procedures for custom DRCs in the `\share\cdssetup\tdd\custom_rules` folder in your Cadence installation or `CDS_SITE` location.
2. Open the Windows command prompt or a Unix terminal.
3. Change to the `\share\cdssetup\tdd\custom_rules` folder.

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4. Run the following command:

```
tclsh auto_mkindex . *.tcl
```

The Tcl index file named `tclIndex` is created in the `\share\cdssetup\tdd\custom_rules` folder.

Displaying the Custom DRCs in System Connectivity Manager

You can display the custom DRCs in the Design Rule Checks tab of the Setup dialog box and enable or disable the custom DRCs. For information on enabling or disabling DRCs, see Enabling and Disabling Design Rule Checks on page 507.

To display the custom DRCs in the Design Rule Checks tab of the Setup dialog box

1. Open a text editor application.
2. Enter the list of Tcl procedures for the custom DRCs in the following syntax:

```
(Custom_DRC
(
    ("<DRC_Display_Name>" "<DRC_Procedure_Name>")
    ("<DRC_Display_Name>" "<DRC_Procedure_Name>")
(
)
)
```

Where `DRC_Display_Name` is the name you want to be displayed for the custom DRC in the Design Rule Checks tab of the Setup dialog box, and `DRC_Procedure_Name` is the name of the Tcl procedure for the DRC.

For example, if you have created two Tcl procedures named `unconnected_pin` and `shorted_power_pin`, enter the list of Tcl procedures for the custom DRCs as below:

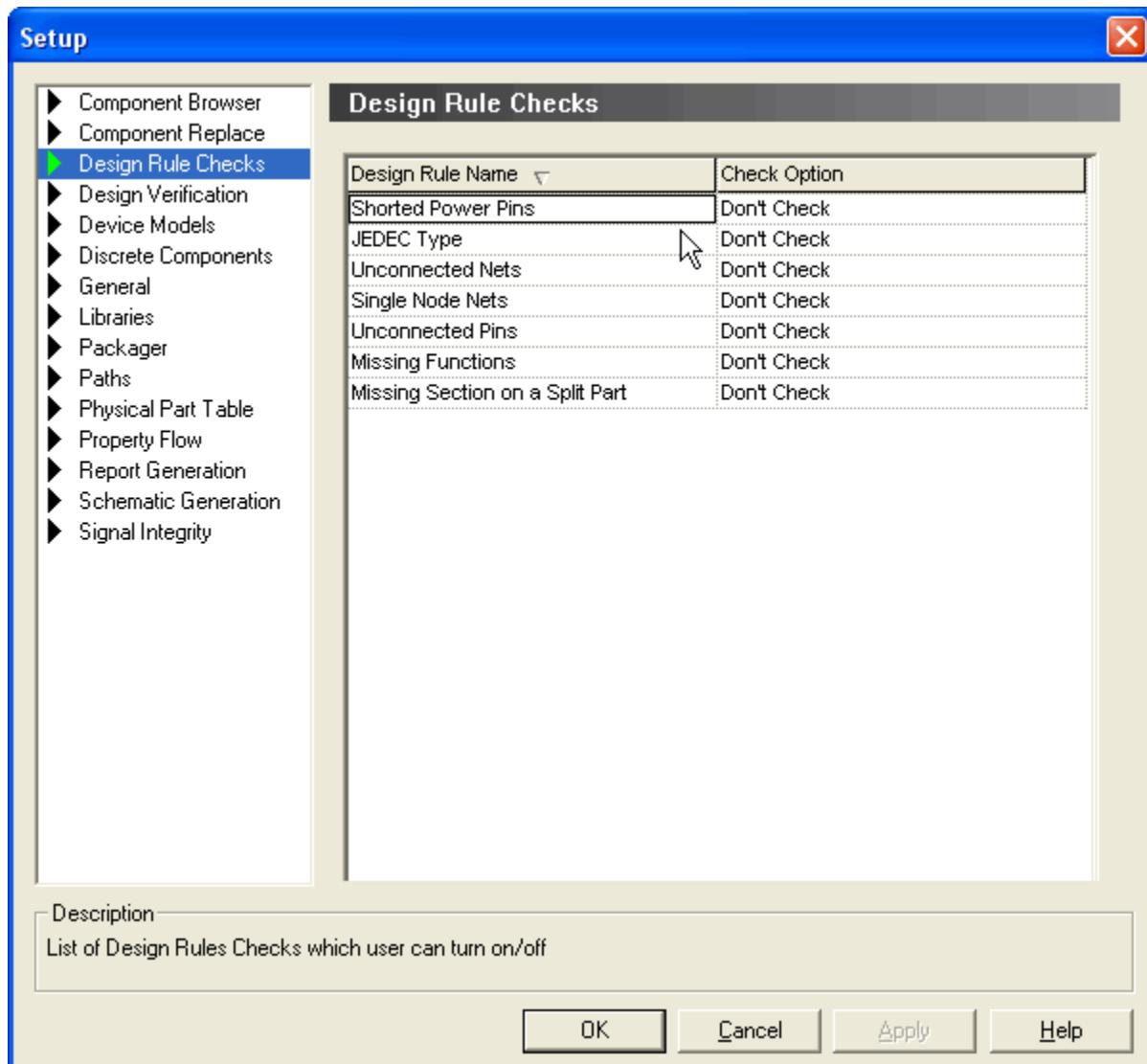
```
(Custom_DRC
(
    ("Unconnected Pins" "unconnected_pin")
    ("Shorted Power Pins" "shorted_power_pin")
(
)
)
```

3. Save the file as `custom_drc.txt` and place it in the `\share\cdssetup\tdd\custom_rules` folder in your Cadence installation.

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The custom DRCs Unconnected Pins and Shorted Power Pins are displayed in the Design Rule Checks tab of the Setup dialog box, as shown below:



Running Design Rule Checks

Before you run DRCs, you must enable the DRCs you want to run. For more information on enabling DRCs, see [Enabling and Disabling Design Rule Checks](#) on page 507.

To run the enabled DRCs

- Choose *Project – Design Rules Check*.
- Click the DRC toolbar button ().

Errors are reported in the Violations window if an enabled DRC fails.

Enabling and Disabling Design Rule Checks

To enable or disable a DRC

1. Choose *Project – Settings*.

The Setup dialog box appears.

2. Click the Design Rule Checks tab.

The standard and custom DRCs are displayed in the *Design Rule Name* column.

- To enable a DRC, click in the *Check Option* column next to a DRC and choose the error severity level—*Error*, *Warning* or *Information*—to be reported in the *Violations* window if the DRC fails. The DRC is enabled.
- To disable a DRC, click in the *Check Option* column next to a DRC and choose *Don't Check*.

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Creating Reports

This chapter contains the following sections:

- [Overview](#) on page 510
- [Creating a Report Template](#) on page 510
- [Modifying a Report Template](#) on page 524
- [Creating User-Defined Query Fields](#) on page 525
- [Setting Up the Report Format](#) on page 535
- [Generating Reports](#) on page 532
- [The .DSR \(Editable Report File\) Format](#) on page 536
- [Adding Headers and Footers in Reports](#) on page 546
- [Using the dsreportgen Command](#) on page 552

Overview

System Connectivity Manager lets you create report templates for each report you want to generate in System Connectivity Manager. The report templates can then be used to generate reports for any design.

For example, if you want to generate a block-based NC pin report in the following format:

U1.1
R22.1
R45.2
U2.6

you can create a report template then use the `dsreportgen` command from the command line to generate the report.

The `dsreportgen` command can be used to generate reports and to open the UIs for generating reports, creating and editing report templates and user-defined query fields. For more information, see [Using the dsreportgen Command](#) on page 552.

Creating a Report Template

You can create report templates for each report you want to generate in System Connectivity Manager. The report templates can then be used to generate reports for any design.

To create a report template

1. Do one of the following:

- Choose *Project – Reports – Create Template*.
- Choose *Project – Reports – Generate Reports* to display the Generate Report dialog box. Click the *Create New* button.
- Run the following command from the command line:

```
dsreportgen -def_tmplt
```

For more information on running the `dsreportgen` command, see [Using the dsreportgen Command](#) on page 552.

The Create Report Template dialog box appears.

2. Enter a name for the report in the *Report Name* field.

3. Do one of the following:

- Select *Design Based* if you want the report to be created for the entire design.
 - Select *Block Based* if want the report to be sorted by blocks in the design.
4. Specify the name and path to the file that contains the content you want to use as the title page for the report.
- You can use a text (.txt) file or a Editable Report Format (.dsr) file as the title page for the report.
5. Select the *Display RefDes as Range* check box if you want to display the range of reference designators in the report, instead of displaying individual reference designators.
6. Select the *Display Pin Number as Range* check box if you want to display the range of pin numbers in the report, instead of displaying individual pin numbers.
- Note:** You cannot select both the *Display RefDes as Range* and *Display Pin Number as Range* check boxes at the same time.
7. Select the *Remove Row if any Cell is Empty* check box if you want a row in the report to be automatically deleted if any cell in that row is empty.
8. Select the *Remove Row if all Cells are Empty* check box if you want a row in the report to be automatically deleted if all the cells in that row are empty.
9. Select the *Duplicate Cell Values* check box if you do not want duplicate values to be displayed in a column in the report.
10. Add keywords in the query grid. You must add one driver keyword that does not have a dependency. For more information, see [Adding a Keyword in the Query Grid](#) on page 513.
11. Specify the dependency for every keyword you add in the query grid, except the driver keyword. For more information, see [Specifying the Dependency for a Keyword](#) on page 515.
12. Specify the qualifier for the keywords for which you want to limit the query to a specific value or a set of values, and specify the qualifier value for each qualifier. For more information, see [Specifying the Qualifier for a Keyword](#) on page 516.
13. Select the check box in *Total* cell in the column for a keyword if you want the total count for the keyword to be displayed in the report.
- The total number of objects found for the keyword is displayed in the bottom of the report. The heading for the row in the report where the total count is displayed is named TOTAL.
14. Specify the title for each keyword in the *Title* row.

The default title for each keyword is displayed in the *Title* cell in the column for each keyword. The title for a keyword is used as the column name for the keyword in the report. You can modify the title for a keyword.

You can also enter the name of another keyword you have added in the query grid as `%keyword_name%` as the title for the keyword to generate a cross-tab report. For more information, see [Generating a Cross-tab Report](#) on page 516.

15. Specify the view order for the keywords in the *View Order* row.

The *View Order* row displays the order in which the columns for the keywords are displayed in the report. The keyword whose view order is 1 is displayed as the first column in the report, the keyword whose view order is 2 is displayed as the second column in the report, and so on.

You can modify the view order of the keywords.

16. Specify the sort order for the keywords in the *Sort Order* row.

The *Sort Order* row displays the order in which the data in the columns in the report are sorted. The data in the columns in the report will be first sorted by the keyword whose sort order is 1, then by the keyword whose sort order is 2, and so on.

You can modify the sort order of the keywords.

Note: The sort order must be a continuous sequence starting with 1.

17. Specify the width for the keywords in the *Width* row.

The *Width* row displays the width that will be used for displaying the column for each keyword in the report. The default width is 20 letters.

18. Specify the alignment for the keywords in the *Alignment* row.

The Alignment row displays how the text in the column for each keyword will be aligned in the report. The default alignment is LEFT.

To modify the alignment for a keyword, click on the alignment cell in the column for the keyword, and choose the alignment type from the drop-down list.

19. Select the check box in the *Visible* cell if you want the column for the keyword to be displayed in the report. Clear the check box if you do not want the column for the keyword to be displayed in the report.

20. Click *Save As*.

The Save Template File As dialog box appears.

21. Browse to the directory where you want to save the report template.

22. Enter the file name for the report template in the *File name* field and click *Save*.

By default, the report templates are saved in the project directory. You can also place the report templates in any of the following locations so that other users can access the report templates.

- <your_install_dir>\share\cdssetup\tdd\custom_templates\
Use this directory to store customized report templates that you want to make available to all users.
- Project directory
Use this directory to store customized report templates that you want to make available to a user who is working on the project.

Note: Report template files have the extension .tpt.

Setting Up the Report Template Query Grid

The following sections describe the procedures for setting up the query grid in the Create Report Template dialog box.

- [Adding a Keyword in the Query Grid](#) on page 513
- [Modifying a Keyword in the Query Grid](#) on page 515
- [Specifying the Dependency for a Keyword](#) on page 515
- [Specifying the Qualifier for a Keyword](#) on page 516
- [Generating a Cross-tab Report](#) on page 516
- [Adding Columns in the Query Grid](#) on page 519
- [Deleting Columns in the Query Grid](#) on page 519

Adding a Keyword in the Query Grid

You can add standard and user-defined query fields as keywords in the query grid. For more information on standard query fields, see [Standard Query Fields](#) on page 519. For more information on user-defined query fields, see [Creating User-Defined Query Fields](#) on page 525.

To add standard and user-defined query fields as keywords in the query grid, do one of the following:

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- Double-click on a query field in the *Standard Query Fields* list or the *User-Defined Fields* list.

The query field is added as a keyword in a new column.
- Click on a cell in the *Keyword* row in the query grid and select a standard or user-defined query field from the drop-down list.
- Select a query field in the *Standard Query Fields* list or the *User-Defined Fields* list and drag and drop it on a cell in the *Keyword* row in the query grid.

Note the following when you add keywords in the query grid:

- One of the keywords you add must be a driver keyword.

The driver keywords are displayed in bold blue letters in the *Standard Query Fields* list.

Note: You must not specify a dependency for the driver keyword.

Note: You can only add a standard query field as a driver keyword. You cannot add a user-defined query field as a driver keyword.

- If you have selected the *Design Based* option, you can add one of the following standard query fields as the driver keyword:
 - BLOCKNAME
 - COMMENT
 - PHYSNET
 - PHYSPART
 - POWERNET
 - REFDES
 - If you have selected the *Block Based* option, you can add one of the following standard query fields as the driver keyword:
 - BLOCKNAME
 - COMMENT
 - COMPONENT
 - NET

- A dependency you specify for a keyword must also be added as a keyword in the query grid. For example, if you specify COMPONENT as the dependency for the keyword PARTNUM, you must also add COMPONENT as a keyword in the query grid. If you do

not add COMPONENT as a keyword, the following error message appears when you save the report template:

PARTNUM depends on COMPONENT but COMPONENT has not been added to the query.

Modifying a Keyword in the Query Grid

To modify a keyword in the query grid, do one of the following:

- Click on the cell for the keyword you want to change in the *Keyword* row and select another standard or user-defined query field from the drop-down list.
- Select a query field in the *Standard Query Fields* list or the *User-Defined Fields* list and drag and drop it on the cell for the keyword you want to change in the *Keyword* row.

Specifying the Dependency for a Keyword

You must specify a dependency for every keyword you add in the query grid, except the driver keyword. For more information on driver keywords, see [Adding a Keyword in the Query Grid](#) on page 513.

Note: A dependency you specify for a keyword must also be added as a keyword in the query grid.

When you add a keyword in the query grid, another keyword you already added in the query grid may be automatically set as the dependency for the keyword. For example, assume that you have a keyword named REFDES in the query grid. When you add the keyword PINNUM in the query grid, REFDES is automatically set as the dependency for the PINNUM keyword. You can select another keyword as the dependency for the PINNUM keyword.

To specify a dependency for a keyword, do the following:

1. Click on the dependency cell below the keyword for which you want to specify the dependency.
2. Select the dependency for the keyword from the drop-down list.

Note: The drop-down list displays the standard query fields that you can specify as the dependency for the keyword. You cannot add any other query field as the dependency for the keyword.

Specifying the Qualifier for a Keyword

You can specify a qualifier for the keywords you add in the query grid to further refine the data displayed for the keyword in the report. The qualifier serves to limit the query to a specific value or a set of values.

To specify a qualifier for a keyword, do the following:

1. Click on the qualifier cell below the keyword for which you want to specify the qualifier.
2. Select the qualifier for the keyword from the drop-down list.

If you select PROP as the qualifier for a keyword, the Select Property dialog box appears. Select the property you want to use as the qualifier for the keyword from the drop-down list, or enter the name of the property. The property name is displayed in the qualifier cell and the  icon in the qualifier cell indicates that the qualifier is a property.

3. Click on the qualifier value cell below the qualifier cell.
4. Specify the qualifier value. To specify the qualifier value, click on the qualifier value cell below the qualifier cell and do one of the following:

- Enter the qualifier value in the qualifier value cell.

For example, if you select PROP as the qualifier for a keyword, enter the value for the property in the qualifier value cell.

Note: You can use wildcards in the qualifier value.

- Click on the  icon in the qualifier value cell if you want to specify more than one qualifier value or if you want to use regular expressions in qualifier values.

The Qualifier Values dialog box appears. Here you can enter more than one qualifier value. You can also use wildcards and regular expressions in the qualifier values. If you enter more than one qualifier value in the Qualifier Values dialog box, separate the values with commas. For example, if you want to use the qualifier values R* and D*, enter the values as:

R*, D*

The query for the keyword will be limited to the qualifier value.

Generating a Cross-tab Report

You can enter the name of another keyword you have added in the query grid as the title for a keyword to generate a cross-tab report. The title should be entered as %keyword_name% where keyword_name is the name of another keyword in the query grid.

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When you generate the report, the value of the keyword you entered as the title will be displayed as the column heading in the report. For example, if you enter %REFDES% as the title for the keyword PINNUM, the reference designators of components in the design are displayed as column headings in the report and the pin numbers of a given reference designator appear in the column for the reference designator. The process of creating a report template to generate a cross-tab report is described below using an example.

The following report displays which pin number of a given reference designator is connected to a specific signal:

Figure 20-1 Cross-tab Report Example

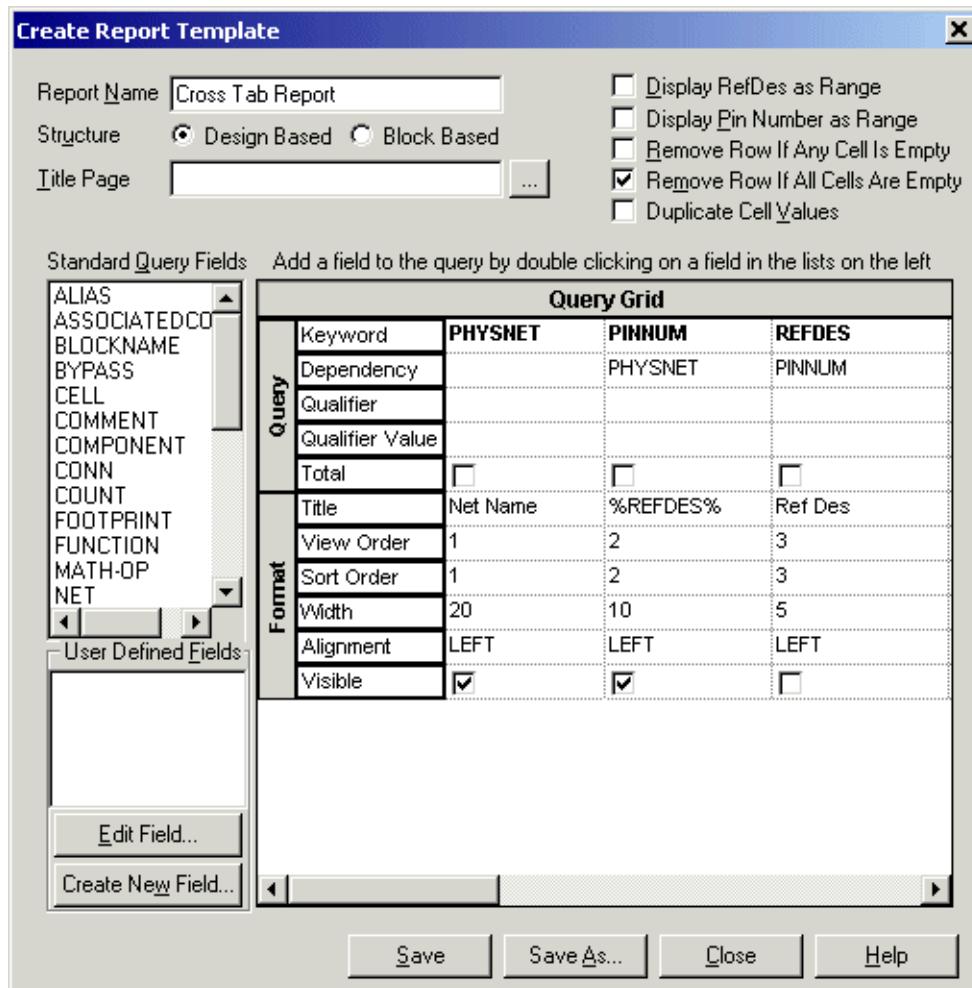
	Net Name	U2	U3	U1
1	ADDRESS	12	12	
2	ADDR		9	
3	CBDATA		1	13
4	CCLOCK	13	10	
5	DATA		4	12
6	RESET1		8	
7	RESET2		6	
8	RESET3		3	
9	RESET		11	11
10	SET		2	

To create a report template to generate such a report, setup the template query grid as shown below:

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Figure 20-2 Report Template for Generating Cross-tab Report



In the above report template, %REFDES% is used as the title for the PINNUM keyword. This results in the reference designators of components in the design appearing as column headings in the report, and the pin numbers of a given reference designator appearing in the column for the reference designator.

Note the following when creating a template for generating a cross-tab report:

- The %keyword_name% you enter as the title must be added as a keyword in the query grid.
For example, in the above report template, REFDES is added as a keyword in the query grid.

- Only the column for the driver keyword and the column for the keyword in which you have entered the title as %keyword_name% must be set as visible. Deselect the Visible check box in other columns in the query grid.

For example, in the above report template, the Visible check box in the column for the REFDES keyword is not selected.

Adding Columns in the Query Grid

To add columns in the query grid, do the following:

1. Click on the column to the left of which you want to add a column.
2. Do one of the following:
 - Right-click and choose *Insert Col* from the shortcut menu.
 - Press *Ctrl + I*

A column is added to the left of the selected column.

Deleting Columns in the Query Grid

To delete columns in the query grid, do the following:

1. Click on the column you want to delete.
2. Do one of the following:
 - Right-click and choose *Delete Col* from the shortcut menu.
 - Press *Ctrl + Delete*.

Standard Query Fields

The following table lists the standard query fields that can be added as keywords in the report template query grid and the data they represent.

The driver keywords are displayed in bold blue letters in the *Standard Query Fields* list. For more information on driver keywords, see [Adding a Keyword in the Query Grid](#) on page 513.

ALIAS	Displays the names of nets aliased to a net.
--------------	--

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ASSOCIATEDCOMP	Displays the type of associated component—bypass capacitors, terminations (Shunt, ShuntRC, PowerClampDiode, Thevinin, and so on) or pullup/pulldowns—attached to a component.
BLOCKNAME	Displays the name of the hierarchical block in which the object for the dependency exists. For example, if you specify NET as the dependency for the keyword BLOCKNAME, the name of the block in which a net exists is displayed in the report.
BYPASS	Displays whether bypass capacitors are attached to a component. The text Bypass in the report indicates that bypass capacitors are attached to a component.
CELL	Displays the cell name of the component.
COMMENT	Displays the comments added on the objects that belong to the dependency you use for the COMMENT keyword. For example, if you specify NET as the dependency for the keyword COMMENT, the comments added on the signals in the design are displayed in the report.
COMPONENT	Displays the component instance name. For example, i1, i2, and so on.
CONN	Displays the connection count of a signal.
CONSTRAINT	Displays constraints and properties on nets in the design. To display only the constraints on nets in the report, select the TYPE qualifier for the CONSTRAINT keyword and specify the qualifier value as C. To display only the properties on nets in the report, select the TYPE qualifier for the CONSTRAINT keyword and specify the qualifier value as P.
COUNT	Displays the count of the objects that belong to the dependency you use for the COUNT keyword. For example, if you specify BYPASS as the dependency for the keyword COUNT, the total number of bypass capacitors attached to a component are displayed in the report.

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FOOTPRINT	Displays the name of the footprint for a component.
FUNCTION	Displays the used or unused sections of a split component.
MATH-OP	Allows you to perform mathematical operations on keywords you have added in the query grid, and display the results in the report. This keyword is normally used in BOM reports. For example, if you want to find the cost of components for manufacturing three PCBs, do the following: <ol style="list-style-type: none">1. Add the property COST as a keyword in the query grid, with the dependency REFDES.2. Add MATH-OP as a keyword in the query grid.3. Click on the  icon in the dependency cell below the MATH-OP keyword. The Mathematical Operator dialog box appears.4. Select COST from the <i>Operand 1</i> drop-down list.5. Select * from the <i>Mathematical Operator</i> drop-down list.6. Enter 3 in the <i>Operand 2</i> field.7. Click <i>OK</i>.8. Select the check box in the total cell below the MATH-OP keyword. When you generate the report, the total cost of components for manufacturing three boards is displayed in the report.
NCPIN	Displays the NCPINS.
NET	Displays the logical net (signal) name.
PARTNUM	Displays the part number of a component.
PHYSNET	Displays the physical net name of a signal.
PHYSPART	Displays the physical part name of a component.
PINNAME	Displays the pin name of a component.
PINCOUNT	Displays the total number of pins on a component.
PINNUM	Displays the pin number of a component.
PORT	Displays the port name of a block.

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POWERNET	Displays the name of the power net connected to the pin of a component. A power net is a net that has a voltage property.
POWERPIN	Displays the power pins defined in the body section of the <code>chips.prt</code> file for the component.
PROP	Use this keyword if you want to specify a property name as a keyword in the report. If you add <code>PROP</code> as a keyword, the Select Property dialog box appears. Select the property you want to use as the keyword from the drop-down list, or enter the name of the property. The property name is displayed in the keyword cell and the  icon in the keyword cell indicates that the keyword is a property.
PUPD	Displays whether a pullup or pulldown is added on a pin of the component. The text <code>Pullup</code> in the report indicates that a pullup is added on a pin of the component. The text <code>Pulldown</code> indicates that a pulldown is added on a pin of the component.
REFDES	Displays the reference designator of a component.
REFDESPINNUM	Concatenates the reference designator and the Pin Number of a component and displays them as a single string.

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RELOP Allows you to perform logical operations on keywords you have added in the query grid, and display the results in the report. This keyword is normally used in BOM reports.

You can perform logical operations such as: =,!= <,>,>=,<=

To use this keyword:

1. Add RELOP as a keyword in the query grid.
2. Click on the  icon in the dependency cell below the RELOP keyword.
The Operator dialog box appears.
3. Select a column for Operand1 list.
4. Select an operator from the Operator drop-down list.

Select a column for Operand2 list.

1. Click *OK*.

When you generate the report, the result of the logical test are displayed in the report. Report displays a value of 1 for True and 0 for False.

SCOPE Displays the scope of a signal. The scope of a signal can be Global, Local, Input, Output, or Inout.

SECTION Displays the section in the `chips.prt` file in which a component has been packaged.

STRINGOP Allows you to perform string concatenate operations on keywords you have added in the query grid, and display the results in the report.

1. Add STRINGOP as a keyword in the query grid.
2. Click on the  icon in the dependency cell below the STRINGOP keyword.

The Operator dialog box appears.

3. Select Operand1, Operator, and Operand2.
4. Click *OK*.

In the report the values of Operand1 and Operand2 are concatenated and displayed.

TERMINATION	Displays the termination type—Shunt, ShuntRC, PowerClampDiode, Thevinin and so on—that is attached to a pin.
TYPE	Displays the type of pin or port. The type of a pin or port can be IN, OUT, or INOUT.

Modifying a Report Template

1. Choose *Project – Reports – Generate Reports*.

The *Generate Report* dialog box appears.

2. Select the report template you want to modify in the *Report Template* list.

If the report template is not displayed in the *Report Template* list, click the *Add Existing* button and add the report template you want to modify.

3. Click *Customize*.

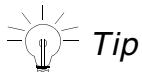
The Create Report Template dialog box appears.

4. Modify the report settings and the query grid settings as required.

For more information on setting up the query grid, see [Setting Up the Report Template Query Grid](#) on page 513.

5. Do one of the following:

- Click *Save* to save the changes to the current report template file.
- Click *Save As* to save to a new report template file.



Tip

It is recommended that you modify the report name in the *Report Name* field before you save to a new report template file. This is because, if two report templates have the same report name, two identical report names will be displayed in the *Report Template* list in the *Generate Report* dialog box. This may confuse you when you are generating reports using the *Generate Report* dialog box.

Creating User-Defined Query Fields

You can create user-defined query fields if you want to generate a report that has a column with sub-columns for information, as shown below:

Result of user-defined query-report that has a column with sub-columns

The diagram shows a report structure. At the top, a horizontal bar contains the text "Result of user-defined query-report that has a column with sub-columns". Below this, there is a table structure. The first row has a single cell containing "NET_SIGNAL_INTEGRITY". The second row starts with a header "Physical Net Name" followed by four columns labeled "PULSE_PARAM_FREQ", "PULSE_PARAM_PERIOD", "PULSE_PARAM_DUTY_CYCLE", and "PULSE_PARAM_JITTER". Below these two rows is a horizontal line. Underneath the line, there is another row with one cell for "Physical Net Name" (containing "CBDATA") and four cells for the sub-columns, each containing numerical values: 100.0, 50, and 2.000.

NET_SIGNAL_INTEGRITY				
Physical Net Name	PULSE_PARAM_FREQ	PULSE_PARAM_PERIOD	PULSE_PARAM_DUTY_CYCLE	PULSE_PARAM_JITTER
CBDATA	100.0	50	2.000	

To create a user-defined query field:

1. Do one of the following:

- Click the *Create New Field* button in the [Create Report Template](#) dialog box.
- Do one of the following:
 - Choose *Project – Reports – Create Custom Column* to display the [User Defined Columns](#) dialog box. Click the *New* button.
 - Run the following command from the command line:

```
dsreportgen -ccol
```

For more information on running the `dsreportgen` command, see [Using the dsreportgen Command](#) on page 552.

The [User Defined Query Field](#) dialog box appears.

2. Enter the name of the user-defined query field in the *Field Name* text box.

Note: Do not use spaces in the name. Also do not enter a name that is the same as that of a standard query field. For more information on standard query fields, see [Standard Query Fields](#) on page 519.

3. Add keywords in the query grid. For more information, see [Adding a Keyword in the Query Grid for User-Defined Query Fields](#) on page 527.

4. Specify the dependency for the keywords you add in the query grid. For more information, see [Specifying the Dependency for a Keyword](#) on page 528.

5. Specify the qualifier for the keywords for which you want to limit the query to a specific value or a set of values, and specify the qualifier value for each qualifier. For more information, see [Specifying the Qualifier for a Keyword](#) on page 529.

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6. Select the check box in *Total* cell in the column for a keyword if you want the total count for the keyword to be displayed in the report.

The total number of objects found for the keyword is displayed in the bottom of the report. The heading for the row in the report where the total count is displayed is named **TOTAL**.

7. Specify the title for each keyword in the *Title* row.

The default title for each keyword is displayed in the *Title* cell in the column for each keyword. The title for a keyword is used as the column name for the keyword in the report. You can modify the title for a keyword.

8. Specify the view order for the keywords in the *View Order* row.

The *View Order* row displays the order in which the columns for the keywords are displayed in the report. The keyword whose view order is 1 is displayed as the first column in the report, the keyword whose view order is 2 is displayed as the second column in the report, and so on.

You can modify the view order of the keywords.

9. Specify the sort order for the keywords in the *Sort Order* row.

The *Sort Order* row displays the order in which the data in the columns in the report are sorted. The data in the columns in the report will be first sorted by the keyword whose sort order is 1, then by the keyword whose sort order is 2, and so on.

You can modify the sort order of the keywords.

Note: The sort order must be a continuous sequence starting with 1.

10. Specify the width for the keywords in the *Width* row.

The *Width* row displays the width that will be used for displaying the column for each keyword in the report. The default width is 20 letters.

11. Specify the alignment for the keywords in the *Alignment* row.

The Alignment row displays how the text in the column for each keyword will be aligned in the report. The default alignment is **LEFT**.

To modify the alignment for a keyword, click on the alignment cell in the column for the keyword, and choose the alignment type from the drop-down list.

12. Select the check box in the *Visible* cell if you want the column for the keyword to be displayed in the report. Clear the check box if you do not want the column for the keyword to be displayed in the report.

13. Click **Save As**.

The Custom Column As dialog box appears.

14. Browse to the directory where you want to save the user-defined query file.
15. Enter the file name for the user-defined query in the *File name* field and click *Save*.

By default, the user-defined query files are saved in the project directory. You can also place the user-defined query files in any of the following locations so that other users can access them.

- <*your_install_dir*>\share\cdssetup\tdd\custom_templates\Use this directory to store user-defined query files that you want to make available all users.
- Project directoryUse this directory to store user-defined query files that you want to make available to a user who is working on the project.

Note: The user-defined query files have the extension .txt.

Setting Up the Query Grid for User-Defined Query Fields

The following sections describe the procedures for setting up the query grid in the Create Report Template dialog box.

- [Adding a Keyword in the Query Grid for User-Defined Query Fields](#) on page 527
- [Modifying a Keyword in the Query Grid for User-Defined Query Fields](#) on page 528
- [Specifying the Dependency for a Keyword](#) on page 528
- [Specifying the Qualifier for a Keyword](#) on page 529
- [Adding Columns in the Query Grid for User-Defined Query Fields](#) on page 530
- [Deleting Columns in the Query Grid for User-Defined Query Fields](#) on page 530

Adding a Keyword in the Query Grid for User-Defined Query Fields

You can add standard query fields as keywords in the query grid. For more information on standard query fields, see [Standard Query Fields](#) on page 519.

To add standard query fields as keywords in the query grid, do one of following:

- Double-click on a query field in the *Standard Query Fields* list.

The query field is added as a keyword in a new column.

- Click on a cell in the *Keyword* row in the query grid and select a standard query field from the drop-down list.
- Select a query field in the *Standard Query Fields* list and drag and drop it on a cell in the *Keyword* row in the query grid.

Modifying a Keyword in the Query Grid for User-Defined Query Fields

To modify a keyword in the query grid, do one of the following:

- Click on the cell for the keyword you want to change in the *Keyword* row and select another standard query field from the drop-down list.
- Select a query field in the *Standard Query Fields* list and drag and drop it on the cell for the keyword you want to change in the *Keyword* row.

Specifying the Dependency for a Keyword

When you add a keyword in the query grid, another keyword you already added in the query grid may be automatically set as the dependency for the keyword. For example, assume that you have a keyword named REFDES in the query grid. When you add the keyword PINNUM in the query grid, REFDES is automatically set as the dependency for the PINNUM keyword. You can select another keyword as the dependency for the PINNUM keyword.

To specify a dependency for a keyword, do the following:

1. Click on the dependency cell below the keyword for which you want to specify the dependency.
2. Select the dependency for the keyword from the drop-down list.

Note: The drop-down list displays the standard query fields that you can specify as the dependency for the keyword. You cannot add any other query field as the dependency for the keyword.

Note the following:

1. A dependency you specify for a keyword must also be added as a keyword in the query grid, or as a keyword in the query grid for the report template in which you want to use the user-defined query field. For example, if you specify a dependency REFDES for the keyword PINNUM, you must add REFDES as a keyword in the query grid for the user-defined query field, or as a keyword in the report template in which you want to use the

user-defined query field. For more information on creating report templates, see [Creating a Report Template](#) on page 510.

2. If you do not specify a dependency for a keyword, a query field that can be added as a dependency for the keyword must be specified as a keyword in the query grid for the report template in which you want to use the user-defined query field. For example, REFDES can be specified as a dependency for the keyword PINNUM. If you do not specify a dependency for the keyword PINNUM in the query grid for the user-defined query field, you must add REFDES as a keyword in the report template in which you want to use the user-defined query field. For more information on creating report templates, see [Creating a Report Template](#) on page 510.
3. If you do not specify the dependency for more than one keyword in the query grid, ensure that the keywords for which you did not specify the dependency have a common parent. For example, REFDES can be specified as the dependency for the keywords PINNUM and PINNAME. So you need not specify the dependency for the keywords PINNUM and PINNAME. However, ensure that you satisfy the condition specified in Note 2 above.

Specifying the Qualifier for a Keyword

You can specify a qualifier for the keywords you add in the query grid to further refine the data displayed for the keyword in the report. The qualifier serves to limit the query to a specific value or a set of values.

To specify a qualifier for a keyword, do the following:

1. Click on the qualifier cell below the keyword for which you want to specify the qualifier.
2. Select the qualifier for the keyword from the drop-down list.

If you select PROP as the qualifier for a keyword, the Select Property dialog box appears. Select the property you want to use as the qualifier for the keyword from the drop-down list, or enter the name of the property. The property name is displayed in the qualifier cell and the  icon in the qualifier cell indicates that the qualifier is a property.

3. Click on the qualifier value cell below the qualifier cell.
4. Specify the qualifier value. To specify the qualifier value, click on the qualifier value cell below the qualifier cell and do one of the following:
 - Enter the qualifier value in the qualifier value cell.

For example, if you select PROP as the qualifier for a keyword, enter the value for the property in the qualifier value cell.

Note: You can use wildcards in the qualifier value.

- ❑ Click on the  icon in the qualifier value cell if you want to specify more than one qualifier value or if you want to use regular expressions in qualifier values.

The Qualifier Values dialog box appears. Here you can enter more than one qualifier value. You can also use wildcards and regular expressions in the qualifier values.

Note: If you enter more than one qualifier value in the Qualifier Values dialog box, separate the values with commas. For example, if you want to use the qualifier values R* and D*, enter the values as:

R*, D*

The query for the keyword will be limited to the qualifier value.

Adding Columns in the Query Grid for User-Defined Query Fields

To add columns in the query grid, do the following:

1. Click on the column to the left of which you want to add a column.
2. Do one of the following:
 - ❑ Right-click and choose *Insert Col* from the shortcut menu.
 - ❑ Press *Ctrl + I*.

A column is added to the left of the selected column.

Deleting Columns in the Query Grid for User-Defined Query Fields

To delete columns in the query grid, do the following:

1. Click on the column you want to delete.
2. Do one of the following:
 - ❑ Right-click and choose *Delete Col* from the shortcut menu.
 - ❑ Press *Ctrl + Delete*.

Modifying User-Defined Query Fields

1. Do one of the following:
 - ❑ Select a user-defined query field in the Create Report Template dialog box and click the *Edit Field* button.

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- Do one of the following:
 - Choose *Project – Reports – Create Custom Column* to display the User Defined Columns dialog box. Select a user-defined query field in the *Existing Columns* list and click the *Edit* button.
 - Run the following command from the command line:

```
dsreportgen -ccol
```

The User Defined Columns dialog box appears. Select a user-defined query field in the *Existing Columns* list and click the *Edit* button.
For more information on running the `dsreportgen` command, see Using the dsreportgen Command on page 552.

The User Defined Query Field dialog box appears.

By default, the user-defined query files existing in the following locations are displayed in the Create Report Template dialog box and the User Defined Columns dialog box:

- `<your_install_dir>\share\cdssetup\tdd\report_templates\`
This directory contains the user-defined query files shipped with your Cadence installation.
- `<your_install_dir>\share\cdssetup\tdd\custom_templates\`
You can use this directory to store customized user-defined query files that you want to make available to all users.
- Current project directory
- Current working directory

The user-defined query files in the directory in which you run the `dsreportgen` command are displayed in the Create Report Template dialog box and the User Defined Columns dialog box. For more information on using the `dsreportgen` command, see Using the dsreportgen Command on page 552.

2. Modify the query grid settings as required.

For more information on setting up the query grid, see Setting Up the Query Grid for User-Defined Query Fields on page 527.

3. Do one of the following:

- Click *Save* to save the changes to the current user-defined query file.
- Click *Save As* to save to a new user-defined query file.

Note: You must modify the user-defined query field name in the *Field Name* field before you save to a new user-defined query file.

Generating Reports

System Connectivity Manager lets you generate reports using the report templates you have created. There are two ways in which you can generate reports in System Connectivity Manager:

- Using the Generate Report dialog box.
- Running the `dsreportgen` command from the command line.

For more information, see [Using the dsreportgen Command](#) on page 552.

Before you generate a report, you must setup the format in which you want to generate the report. For more information, see [Setting Up the Report Format](#) on page 535.

To generate reports using the Generate Report dialog box, do the following:

1. Do one of the following:
 - Choose *Project – Reports – Generate Reports*.
 - Run the following command from the command line:

```
dsreportgen -proj <project_file> -ui
```

where *project_file* should specify the path and name of the project (.cpm) file for the project for which you want to generate reports.
For more information on running the `dsreportgen` command, see [Using the dsreportgen Command](#) on page 552.

The *Generate Report* dialog box appears.

2. Select the report template using which you want to generate a report in the *Report Template* list.

You can select multiple report templates if you want to generate more than one report at the same time. To select multiple report templates, press the *Ctrl* or *Shift* key and click on the templates you want to use.

By default, the report templates existing in the following locations are displayed in the *Report Template* list:

- `<your_install_dir>\share\cdssetup\tdd\report_templates\`

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This directory contains the standard report templates shipped with your Cadence installation.

- <your_install_dir>\share\cdssetup\tdd\custom_templates\
- You can use this directory to store customized report templates that you want to make available to all users.

- Current project directory
- Current working directory

The report templates in the directory in which you run the `dsreportgen` command are displayed in the *Report Template* list. For more information on using the `dsreportgen` command, see [Using the dsreportgen Command](#) on page 552.

If the report template you want to use is not displayed in the *Report Template* list, click the *Add Existing* button to display the Select the Template File dialog box. Select the template file and click *Open* to add the template in the *Report Template* list.

3. Select the format in which you want the report to be generated.

You can generate reports in the following formats:

- DSR (Editable Report File) format
For more information, see [The .DSR \(Editable Report File\) Format](#) on page 536.
- CSV (Comma Separated Value) format
- Text file in tabular format
- HTML

4. Do one of the following:

- Select the *Report File* option if you want to create the report in a specific file. Enter the name and path to the file, or click the browse button to select the report file.

Note: You cannot select the *Report File* option if you have selected multiple report templates in the *Report Template* list.

- Select the *Location* option if you want to create the report in a specific location.

By default, the reports will be created in the project directory. If you want the report to be created in some other directory, enter the path for the directory, or click the browse button to select the directory.

The generated report will have the same file name as the report template file. For example, if you are generating a report using a report template named

BOM_Report.tpt for a root design named CPU, the report file name will be CPU_BOM_Report.html if you are generating a report in the HTML format.

5. Select the *Override Qualifier Value for Report Driver* check box if you want to override the qualifier or qualifier value for the driver keyword in the selected report template when you generate the report.

For more information on driver keywords in report templates, see [Adding a Keyword in the Query Grid](#) on page 513. For more information on keyword qualifiers and qualifier values in report templates, see [Specifying the Qualifier for a Keyword](#) on page 516.

6. Click *Setup* if you want to specify the sort order, currency, column and row separators, fonts and to define custom variables to be used in the generated report. For more information, see the following topics:
 - [Setting Up the Report Format](#) on page 535
 - [Defining Custom Variables for Headers and Footers in Reports](#) on page 551
7. Click *Generate* to generate the report using the selected report template.

If you have selected the *Override Qualifier Value for Report Driver* check box, the Qualify Report Parameter dialog box appears. The Qualify Report Parameter dialog box displays the report templates you selected in the Generate Report dialog box, the driver keyword for each report template, and the qualifier and qualifier value, if any, for the driver keyword for each report template.

Note: If you did not select the *Override Qualifier Value for Report Driver* check box, the report is generated.

- a. Change the qualifier for a driver keyword, if required. If a qualifier does not exist for a driver keyword, you can specify a qualifier for the keyword to further refine the data displayed for the keyword in the report. The qualifier serves to limit the query to a specific value or a set of values.

To change the qualifier or to specify a qualifier, click on the qualifier cell next to a driver keyword and select a qualifier from the drop-down list.

If you select PROP as the qualifier for a keyword, the Select Property dialog box appears. Select the property you want to use as the qualifier for the keyword from the drop-down list, or enter the name of the property. The property name is displayed in the qualifier cell and the  icon in the qualifier cell indicates that the qualifier is a property.

- b. Change or specify the qualifier value for a driver keyword, if required.

To change or specify the qualifier value, click on the qualifier value cell next to the driver keyword and do one of the following:

- Enter the qualifier value in the qualifier value cell.

For example, if you select PROP as the qualifier for a keyword, enter the value for the property in the qualifier value cell.

You can use wildcards in the qualifier value.

- Click on the  icon in the qualifier value cell if you want to specify more than one qualifier value or if you want to use regular expressions in qualifier values.

The Qualifier Values dialog box appears. Here you can enter more than one qualifier value. You can also use wildcards and regular expressions in the qualifier values.

If you enter more than one qualifier value in the Qualifier Values dialog box, separate the values with commas. For example, if you want to use the qualifier values R* and D*, enter the values as:

R*, D*

The query for the driver keyword will be limited to the qualifier value.

- c. Click *OK* to generate the report.

The report is generated in the selected format and displayed in System Connectivity Manager. For example, if you are generating a report in the HTML format for a root design named CPU, using a report template named BOM_Report.tpt, the CPU_BOM_Report.html report file is displayed in System Connectivity Manager.

Setting Up the Report Format

Before you generate a report, you must setup the format in which you want to generate the report.

1. Do one of the following:

- Choose *Project – Reports – Generate Reports* to display the *Generate Report* dialog box. Click *Setup* to display the Setup for Report Generation dialog box.
- Choose *Project – Settings* to display the Setup dialog box. Click *Report Generation*.

2. Click the General Settings tab.

3. Select the default format in which reports are generated in the *Report Format* drop-down list.

4. Select the order in which you want the data in reports to be sorted from the *Sort Order* drop-down list.

Select:

- Ascending*, to sort the data in the reports in ascending order.
- Descending*, to sort the data in the reports in descending order.

5. Enter the currency symbol you want to use in reports.
6. Select the *Hide Line Numbers* check box if you do not want line numbers to be displayed in the generated reports.
7. In the *Column Separator* field, enter the character you want to use as the column separator in Text File in Tabular Form reports.
8. In the *Row Separator* field, enter the character you want to use as the row separator in Text File in Tabular Form reports.
9. In the *Column Pad* field, enter the character you want to use as the column pad in Text File in Tabular Form reports. The column pad is the space between two columns in the report.
10. In the *Header Separator* field, enter the character you want to use as the separator for column headings in Text File in Tabular Form reports.
11. Select the font you want to use for displaying data in reports, and specify the font settings.
12. Click *OK* to save the settings.

The .DSR (Editable Report File) Format

System Connectivity Manager allows you to generate reports in the `.dsr` (Editable Report File) format. You can use reports in the `.dsr` format to do the following:

- [Debugging the Design using the .DSR Report File](#) on page 537
- [Adding Rows and Columns in the .DSR Report File](#) on page 537
- [Working with Text in New Rows and Columns in the .DSR Report File](#) on page 538
- [Changing Column Width and Row Height in the .DSR Report File](#) on page 540
- [Moving Rows and Columns in the .DSR Report File](#) on page 542
- [Deleting Rows and Columns in the .DSR Report File](#) on page 543
- [Viewing Two Parts of a .DSR Report File by Freezing Rows and Columns](#) on page 544

- [Saving a .DSR Report File in Other Formats](#) on page 545

Debugging the Design using the .DSR Report File

The reports you create in System Connectivity Manager might indicate errors in the design. Also, you might want to verify something that is displayed in the report.

System Connectivity Manager lets select an object in the report and then highlight the object in the design. This helps you in quickly debugging the design.

To highlight an object from a report, do the following:

1. Open the .dsr file for the report in System Connectivity Manager.

To open the .dsr file for the report in System Connectivity Manager, do one of the following:

- If the .dsr file is still open in the System Connectivity Manager workspace, click on the tab for the .dsr file to display it.
- Open the .dsr file from the *Reports* folder in the File Viewer.
For more information on using the File Viewer, see [Using the File Viewer](#) on page 230.
- Use the procedure described in [Generating Reports](#) on page 532.

2. Click on the cell for the object that you want to highlight in the design.

For example, if you want to highlight the net named CBDATA in the *Physical Net Name* column of the report, click on the cell for the net CBDATA.

3. Choose *Edit – Highlight*.

The object is highlighted in the design.

Adding Rows and Columns in the .DSR Report File

You can add rows and columns in the .dsr file to add notes, feedback, or other additional information, or to add whitespace in reports to improve readability.

To add rows and columns in the .dsr file, do the following:

1. Open the .dsr file for the report in System Connectivity Manager.

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To open the `.dsr` file for the report in System Connectivity Manager, do one of the following:

- If the `.dsr` file is still open in the System Connectivity Manager workspace, click on the tab for the `.dsr` file to display it.
- Open the `.dsr` file from the *Reports* folder in the File Viewer.

For more information on using the File Viewer, see [Using the File Viewer](#) on page 230.

- Use the procedure described in [Generating Reports](#) on page 532.

2. To add rows, do the following:

- a.** Click on the row above or below which you want to add a row.
- b.** Do one of the following:
 - Choose *Edit – Insert Row – Above* to add a row above the current row.
 - Choose *Edit – Insert Row – Below* to add a row below the current row.

3. To add columns, do the following:

- a.** Click on the column to the left or right of which you want to add a column.
- b.** Do one of the following:
 - Choose *Edit – Insert Column – To the Left* to add a column to the left of the current column.
 - Choose *Edit – Insert Column – To the Right* to add a column to the right of the current column.

The Insert Column dialog box appears.

- c.** Enter the column name and click OK.

Note: If you want to create a column without a column name, do not enter the column name and click OK.

Working with Text in New Rows and Columns in the .DSR Report File

You can enter, cut, copy, paste and clear the text in the new rows and columns you add in reports. You can also align and format the text in the new rows and columns.

Aligning Text in New Rows and Columns

To align text in a new row, column, or cell of a new row or column, do the following:

1. Select the new row, column, or cell of a new row or column in which you want to align the text.

- To select a new row, click on the row header.

Note: The header for a new row will not have a number.

- To select a new column, click on the column name.

- To select a cell of a new row or column, click on the cell.

2. Choose *Format – Align*, then choose:

Left To left align the text.

Right To right align the text.

Center To center the text.

Formatting Text in New Rows and Columns

To format text in a new row, column, or cell of a new row or column, do the following:

1. Select the new row, column, or cell of a new row or column in which you want to format the text.

- To select a new row, click on the row header.

Note: The header for a new row will not have a number.

- To select a new column, click on the column name.

- To select a cell of a new row or column, click on the cell.

2. Choose *Format – Style*, then choose:

Bold To apply bold formatting to the text.

Italic To apply italic formatting to the text.

Underline To underline the text.

Changing Column Width and Row Height in the .DSR Report File

You can change the column width and row height in the .dsr file to make the report more readable.

- Open the .dsr file for the report in System Connectivity Manager.

To open the .dsr file for the report in System Connectivity Manager, do one of the following:

- If the .dsr file is still open in the System Connectivity Manager workspace, click on the tab for the .dsr file to display it.
 - Open the .dsr file from the *Reports* folder in the File Viewer.
For more information on using the File Viewer, see [Using the File Viewer](#) on page 230.
 - Use the procedure described in [Generating Reports](#) on page 532.

To change the height of a row to fit its contents, do the following:

1. Select the row you want to change.
 - To select a row, click on the row heading.
 - To select more than one row at the same time, do one of the following:
 - Click on the heading of the first row you want to change, then press the *Ctrl* or *Shift* key and click on the heading of the remaining rows you want to change.
 - Click on the heading of the first row you want to change, then without releasing the mouse button, drag the mouse to select the remaining rows you want to change.
 - To select all the rows in the report, click the *Select All* button.
2. Choose *Format – Resize Rows*.

To change the height of a row according to your requirements, do the following:

- Drag the boundary below the row heading until the row is the height you want.

To change the height of multiple rows according to your requirements, do the following:

1. Select the rows you want to change.

To select more than one row at the same time, do one of the following:

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- Click on the heading of the first row you want to change, then press the *Ctrl* or *Shift* key and click on the heading of the remaining rows you want to change.
 - Click on the heading of the first row you want to change, then without releasing the mouse button, drag the mouse to select the remaining rows you want to change.
- 2.** Drag a boundary below a selected row heading.

To change the height of all the rows in the report according to your requirements, do the following:

- 1.** Click the *Select All* button.
- 2.** Drag a boundary below any row heading.

To change the width of a column to fit its contents, do the following:

- 1.** Select the column you want to change.
 - To select a column, click on the column heading.
 - To select more than one column at the same time, do one of the following:
 - Click on the heading of the first column you want to change, then press the *Ctrl* or *Shift* key and click on the name of the remaining columns you want to change.
 - Click on the heading of the first column you want to change, then without releasing the mouse button, drag the mouse to select the remaining columns you want to change.
 - To select all the columns in the report, click the *Select All* button.

2. Choose *Format – Resize Columns*.

To change the width of a column according to your requirements, do the following:

- Drag the boundary on the right side of the column heading until the column is the width you want.

To change the width of multiple columns according to your requirements, do the following:

- 1.** Select the columns you want to change.

To select more than one column at the same time, do one of the following:

 - Click on the heading of the first column you want to change, then press the *Ctrl* or *Shift* key and click on the name of the remaining columns you want to change.

- Click on the heading of the first column you want to change, then without releasing the mouse button, drag the mouse to select the remaining columns you want to change.
- 2. Drag the boundary to the right of a selected column heading.

To change the width of all the columns in the report according to your requirements, do the following:

1. Click the *Select All* button.
2. Drag the boundary of any column heading.

Moving Rows and Columns in the .DSR Report File

You can move rows and columns in the `.dsr` file.

Moving Rows in Reports

To move a row in a report, do the following:

1. Select the row you want to move.
 - To select a row, click on the row heading.
 - To select more than one row at the same time, do one of the following:
 - Click on the heading of the first row you want to move, then press the *Ctrl* or *Shift* key and click on the heading of the remaining rows you want to move.
 - Click on the heading of the first row you want to move, then without releasing the mouse button, drag the mouse to select the remaining rows you want to move.
2. Click on any of the selected rows and drag the mouse.

A red horizontal line will move from one row to the next.
3. When the red horizontal line is in the location you want the row(s) to move, release the mouse.

Moving Columns in Reports

To move a column in a report, do the following:

1. Select the column you want to move.

- To select a column, click on the column heading.
 - To select more than one column at the same time, do one of the following:
 - Click on the heading of the first column you want to move, then press the *Ctrl* or *Shift* key and click on the heading of the remaining columns you want to move.
 - Click on the heading of the first column you want to move, then without releasing the mouse button, drag the mouse to select the remaining columns you want to move.
2. Click on any of the selected columns and drag the mouse.
A red vertical line will move from one column to the next.
3. When the red vertical line is in the location you want the column(s) to move, release the mouse.

Deleting Rows and Columns in the .DSR Report File

You can delete the rows and columns in the reports using the procedure described in [Adding Headers and Footers in Reports](#) on page 546.

To delete a new row in a report, do the following:

1. Select the new row that you want to delete.

To select a new row, click on the row header.

Note: The header for a new row will not have a number.

2. Choose *Edit – Remove Rows*.

The new row is deleted from the report.

To delete a new column in a report, do the following:

1. Select the new column that you want to delete.

To select a new column, click on the column name.

2. Choose *Edit – Remove Columns*.

The new column is deleted from the report.

Viewing Two Parts of a .DSR Report File by Freezing Rows and Columns

Freezing Rows

If your report has many rows, it may be too long to view certain rows at the same time. You can prevent a row from scrolling by freezing it.

To freeze a row, do the following:

- 1.** Select the row you want to freeze.
 - To select a row, click on the row heading.
 - To select more than one row at the same time, do one of the following:
 - Click on the heading of the first row you want to freeze, then press the *Ctrl* or *Shift* key and click on the name of the remaining rows you want to freeze.
 - Click on the heading of the first row you want to freeze, then without releasing the mouse button, drag the mouse to select the remaining rows you want to freeze.
- 2.** Choose *Format – Freeze Columns*.

The frozen rows are displayed in the top of the report, allowing you to view the rows when you scroll through the report.

Unfreezing Rows

- To unfreeze rows, choose *Format – Unfreeze Rows*.

The frozen rows are placed at their original location.

Freezing Columns

If your report has many columns, it may be too wide to view certain columns at the same time. You can prevent a column from scrolling by freezing it.

To freeze a column, do the following:

- 1.** Select the column you want to freeze.
 - To select a column, click on the column heading.
 - To select more than one column at the same time, do one of the following:

- Click on the heading of the first column you want to freeze, then press the *Ctrl* or *Shift* key and click on the name of the remaining columns you want to freeze.
- Click on the heading of the first column you want to freeze, then without releasing the mouse button, drag to select the remaining columns you want to freeze.

2. Choose *Format – Freeze Columns*.

The frozen columns are displayed in the left side of the report, allowing you to view the columns when you scroll through the report.

Unfreezing Columns

- To unfreeze columns, choose *Format – Unfreeze Columns*.

The frozen columns are placed at their original location.

Saving a .DSR Report File in Other Formats

To create a report in other formats, do the following:

1. Choose *View – File Viewer* to display the File Viewer pane.
 2. Double-click on the Reports folder to display the reports you had created in System Connectivity Manager.
 3. Choose *File – Export File*.
- The Save As dialog box appears.
4. Browse to the location where you want to save the report.
 5. Choose the format in which you want to save the report in the *Save as type* drop-down list.

You can save the .dsr file in the following formats:

- HTML (.html, .htm)
- CSV (Comma Separated Values file format) (.csv)
- Formatted Text (.txt)

6. Enter the name of the report file in the *File Name* field and click *OK*.

The report file in the format you specified is saved and opened in a new tab in System Connectivity Manager.

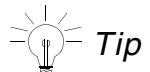
Adding Headers and Footers in Reports

To add headers and footers in reports, do the following:

1. Generate the report for which you want to add headers and footers.

For more information on generating reports in System Connectivity Manager, see [Generating Reports](#) on page 532.

When you generate a report, System Connectivity Manager creates an Editable Report (.dsr) file and a report file in report format you choose when generating the report. The .dsr file and the report file are opened in two different tabs.



If you have already generated the report for which you want to add headers and footers, open the .dsr file for the report in System Connectivity Manager. You can open the .dsr file from the *Reports* folder in the File Viewer or using the procedure described in [Generating Reports](#) on page 532. For more information on using the File Viewer, see [Using the File Viewer](#) on page 230.

2. Select the tab for the .dsr file.

Note: You can add headers and footers only in the .dsr file. For more information on the .dsr file, see [The .DSR \(Editable Report File\) Format](#) on page 536.

3. Choose *File – Header/Footer*.

The Header/Footer dialog box appears.

4. Select the Header tab to enter the header information, or select the Footer tab to enter the footer information.

You can use text or variables to enter the header or footer information. For more information on using variables to specify header or footer information in reports, see [Using Variables in Report Headers and Footers](#) on page 547.

5. To enter the header or footer information:

- Use the *Left Aligned* column to enter the header or footer information that should be left aligned in the report.

- Use the *Centered* column to enter the header or footer information that should be centered in the report.
 - Use the *Right Aligned* column to enter the header or footer information that should be right aligned in the report.
6. To specify the font settings for displaying the header or footer information in the report, do the following:
- a. Click on a cell in which you have entered the header or footer information if you want to specify the font settings only for that cell, or drag the mouse to select the cells for which you want to change the font settings.
 - b. Click on the *Font* button to display the Font dialog box.
 - c. Specify the font settings you want to use and click *OK*.
- Note:** The default font is Arial 8.
7. Specify the distance between the top of the page and the first line in the header in the *Header* field.

For example, if you specify the distance as 0 . 5, the distance between the top of the page and the first line in the header will be 0.5 inches.
8. Specify the distance between the bottom of the page and first line in the footer in the *Footer* field.

For example, if you specify the distance as 0 . 5, the distance between the bottom of the page and the first line in the footer will be 0.5 inches.
9. Enter the number from which the page numbering should start in the *First Page No.* field.
10. Select the *Save settings to profile* check box if you want to save the header footer settings in the Windows registry.
11. Click OK.

The header and footer information is displayed when you preview or print the .dsr file.

Using Variables in Report Headers and Footers

System Connectivity Manager provides standard variables that can be used in headers and footers in reports. You can also define custom variables for use in headers and footers in reports. For more information on defining custom variables, see [Defining Custom Variables for Headers and Footers in Reports](#) on page 551.

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Creating Reports

When you preview or print the `.dsr` file, System Connectivity Manager displays the value of the standard or custom variable. For example if you use the standard variable `<DESIGN_NAME>` in the header of the report, System Connectivity Manager displays the design name in the report header when you preview or print the report.

Note: When you use a standard or custom variable in the header or footer of a report, you must enclose the variable name in angle brackets. For example, if you have defined a custom variable named `USER_NAME` with the value `John Edwards`, you must enter the custom variable as `<USER_NAME>` when you enter the header or footer information in the [Header/Footer dialog box](#).

The following standard variables can be used for headers and footers in reports.

Standard Variable	Description
<code><DESIGN_LIBRARY></code>	Displays the name of the library in which the design is located.
<code><DESIGN_NAME></code>	Displays the name of the design.
<code><ENV>{env_name}</code>	Displays the value of the environment variable you specify in the {} braces. For example, if you have defined an environment variable <code>USER</code> with the value <code>James Parker</code> , you can display the text: <code>Printed by: James Parker</code> in the header or footer of your report by using the ENV variable as below: <code>Printed by: <ENV>{USER}</code>
<code><FILE_NAME></code>	Displays the name of the <code>.dsr</code> file you are previewing or printing.
<code>\$P</code>	Displays the page number. Note: Do not enclose the <code>\$P</code> variable in angle brackets.
<code><PROJ_LOCATION></code>	Displays the path to the project directory.
<code><PROJ_NAME></code>	Name of the design project. For example, if the name of your project file is <code>network_switch.cpm</code> , the project name will be displayed as <code>network_switch</code> .
<code><PROJ_PATHNAME></code>	Displays the name of the design project (<code>.cpm</code>) file. Example: <code>network_switch.cpm</code>

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Standard Variable	Description
<BMP>{ <i>path to .bmp file</i> }	Lets you display a .bmp (Windows bitmap) file in the report header or footer.
<DATE>{ <i>format</i> }	Displays the date or time information according to the formats used with the DATE variable. Enter the date formats within the {} braces. You can add text and spaces along with the date formats to customize the date or time information. For more information on the supported date formats, see Table 20-1 on page 549 .

Examples:

- To display the date as August 5, 2004, use the variable:
`<DATE>{ %B %d, %Y}`
Note that spaces and commas have been used in the above example to customize the date information.
- To display the time in 24-hour format, use the variable:
`<DATE>{ %H:%M Hours}`

Table 20-1 Formats for DATE Variable

Date Format	Description
%a	Displays the abbreviated weekday name. Example: Tue
%A	Displays the full weekday name. Example: Tuesday
%b	Displays the abbreviated month name. Example: Sep
%B	Displays the full month name. Example: September

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Creating Reports

Table 20-1 Formats for DATE Variable

Date Format	Description
%c	<p>Displays date and time according to the locale settings on your system.</p> <p>For example, if your locale setting is English (United States) the date and time is displayed as:</p> <p>09/07/2004 03:08:27 PM</p> <p>If your locale setting is English (United Kingdom) the date and time is displayed as:</p> <p>07/09/2004 15:08:27</p>
%d	<p>Displays the day of the month as a decimal number (from 01 to 31).</p> <p>For example, the seventh day of the month is displayed as 07.</p>
%H	<p>Displays the hour in 24-hour format (from 00 to 23).</p> <p>For example, 3 PM is displayed as 15.</p>
%I	<p>Displays the hour in 12-hour format (from 01 to 12).</p> <p>For example, 3 PM is displayed as 03.</p>
%j	<p>Displays the day of the year as a decimal number (from 001 to 366).</p>
%m	<p>Displays the month as a decimal number (from 01 to 12).</p>
%M	<p>Displays the minute as a decimal number (from 00 to 59).</p>
%p	<p>Displays the A.M./P.M. indicator for 12-hour clock.</p>
%S	<p>Displays the second as a decimal number (from 00 to 59).</p>
%U	<p>Displays the week of the year as a decimal number (from 00 to 51), with Sunday as first day of week</p>
%w	<p>Displays the weekday as a decimal number (from 0 to 6, with Sunday as 0)</p>
%W	<p>Displays the week of the year as a decimal number (from 00 to 51), with Monday as first day of week.</p>

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Creating Reports

Table 20-1 Formats for DATE Variable

Date Format	Description
%x	Displays the date in the format specified in the regional settings for your system. For example, if you have specified the date format as MM/DD/YYYY, the date will be displayed as, say, 09/07/2004.
%X	Displays the time in the format specified in the regional settings for your system. For example, if you have specified the time format as MM/DD/YYYY, the date will be displayed as, say, 09/07/2004.
%y	Displays the year without century, as a decimal number (from 00 to 99). For example, the year 2004 is displayed as 04.
%Y	Displays the year with century, as a decimal number For example, the year 2004 is displayed as 2004.
%z or %Z	Displays the full name or abbreviation of the time zone setting on your system. Nothing will be displayed if time zone is unknown. For example, if the time zone setting on your Windows system is (GMT-7) Mountain Time (US & Canada), the text Pacific Daylight Time is displayed. Note: If you changed the time zone settings on your system after starting System Connectivity Manager, you must restart System Connectivity Manager for the new time zone setting to be displayed.
%%	Displays the % sign.

Defining Custom Variables for Headers and Footers in Reports

System Connectivity Manager lets you define custom variables that can be used in the headers and footers in reports. For more information on adding headers and footers in reports, see [Adding Headers and Footers in Reports](#) on page 546.

To define custom variables:

1. Open the Custom Variables page using one of the following methods.
 - Choose *Project – Settings*.

The Setup dialog box appears.

- From the left pane, choose Report Generation.

The Report Generation page opens in the right pane of the dialog box.

- Click the Custom Variables tab.

- Choose *Project – Reports – Generate Reports*.

The Generate Report dialog box appears.

- Click the *Setup* button to display the Setup for Report Generation dialog box.

- Click the Custom Variables tab.

2. Specify the name of the custom variable in the *Name* field.

3. Specify the value of the custom variable in the *Value* field.

4. Click *OK*.

You can now use the custom variable in the header and footer for reports. For example, if you define a custom variable named `CONF` with the value `CONFIDENTIAL` and then use the variable `<CONF>` in the report footer, System Connectivity Manager displays the text `CONFIDENTIAL` in the report footer when you preview or print the report. For more information on adding headers and footers in reports, see [Adding Headers and Footers in Reports](#) on page 546.

Note: When you use a custom variable in the header or footer of a report, you must enclose the custom variable name in angle brackets. For example, if you have defined a custom variable named `USER_NAME` with the value `John Edwards`, you must enter the custom variable as `<USER_NAME>` when you enter the header or footer information in the [Header/Footer](#) dialog box.

Using the `dsreportgen` Command

You can use the `dsreportgen` command from the command line to generate reports and for opening the user interfaces for generating reports, creating and editing report templates and user-defined query fields.

The usage for the `dsreportgen` command is:

```
dsreportgen [-proj <project_file>] [-ui] [-def_tmplt] [-ccol]
            [-tpt <template_file>] [-format <DSR | CSV | TXT | HTML>]
            [-out <report_file_name>] [-qual <qualifier>]
            [-val_qual <comma separated list of qualifier values>]
            [-log <log_file_name>] [-help]
```

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Creating Reports

The options and arguments for the `dsreportgen` command are described below.

Table 20-2 dsreportgen Command Options and Arguments

Options and Arguments	Description
<code>-proj <project_file></code>	Specifies the path and project file (.cpm) name of the project for which you want to generate reports.
	Example:
	<code>-proj c:\network_switch\network_switch.cpm</code>
	Note: You can use absolute and relative paths to specify the path to the project file.
<code>-ui</code>	Opens the Generate Report dialog box. You can generate reports using this dialog box.
	If you do not specify the <code>-proj <project_file></code> option when you use the <code>-ui</code> option, you must specify the path and project file (.cpm) name of the project for which you want to generate reports in the Generate Report dialog box.
	For more information on using the Generate Report dialog box, see Generating Reports on page 532.
<code>-def_tmplt</code>	Opens the Create Report Template dialog box. You can create report templates using this dialog box. For more information on creating report templates using the Create Report Template dialog box, see Creating a Report Template on page 510.
	If you use the <code>-tpt</code> option along with this option, the report template file specified in the <code>-tpt</code> option will be opened for editing in the Create Report Template dialog box.
<code>-ccol</code>	Opens the User-Defined Columns dialog box. You can create and edit user-defined query fields using this dialog box.
	For more information on creating and editing user-defined query fields, see Creating User-Defined Query Fields on page 525.

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Creating Reports

Table 20-2 dsreportgen Command Options and Arguments

Options and Arguments	Description
<code>-tpt <template_file></code>	<p>Specifies the path and filename of the report template file you want to use.</p> <ul style="list-style-type: none">■ Use this option with the <code>-proj</code> and <code>-format</code> options if you want to generate a report using the template file.■ Use this option with the <code>-def_tmplt</code> option if you want to modify a report template using the Create Report Template dialog box. <p>Note: You can use absolute and relative paths to specify the path to the report template file.</p>
<code>-format <DSR CSV TXT HTML></code>	<p>Specifies the format in which you want to generate the report.</p> <p>You can generate reports in the following formats:</p> <ul style="list-style-type: none">■ DSR (Editable Report File) format For more information, see The .DSR (Editable Report File) Format on page 536.■ CSV (Comma Separated Value) format■ TXT (Text file in tabular format)■ HTML <p>Note: You must use the <code>-proj</code>, and <code>-tpt</code> options when you use this option.</p>

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Creating Reports

Table 20-2 dsreportgen Command Options and Arguments

Options and Arguments	Description
<code>-out<report_file_name></code>	<p>Specifies the path and filename of the report file that should be created when you run the <code>dsreportgen</code> command with the <code>-tpt</code> and <code>-format</code> options.</p>
	<p>Note: You must use the <code>-proj</code>, <code>-tpt</code> and <code>-format</code> options when you use this option.</p>
	<p>Note: If you do not use this option with the <code>-proj</code>, <code>-tpt</code> and <code>-format</code> options, the generated report will have the same file name as the report template file. For example, if you are generating a report using a report template named <code>BOM_Report.tpt</code> for a root design named <code>CPU</code>, the report file name will be <code>CPU_BOM_Report.html</code> if you are generating a report in the HTML format.</p>
	<p>Note: You can use absolute and relative paths to specify the path to the report file.</p>
<code>-qual <qualifier></code>	<p>Specifies the qualifier you want to use to override the qualifier specified for the driver keyword in the report template file you specified using the <code>-tpt</code> option.</p>
	<p>Note: You must use the <code>-proj</code>, <code>-tpt</code> and <code>-format</code> options when you use this option.</p>
	<p>Note: For this release you can use only <code>VALUE</code> as the qualifier.</p>
<code>-val_qual <comma separated list of qualifier values></code>	<p>Specifies the qualifier value you want to use to override the qualifier value specified for the driver keyword in the report template file you specified using the <code>-tpt</code> option.</p>
	<p>Note: You must use the <code>-proj</code>, <code>-tpt</code>, <code>-format</code> and <code>-qual</code> options when you use this option.</p>
	<p>Note: You can use wildcards and regular expressions in the qualifier values.</p>

dsreportgen Command Usage Examples

- To open the Generate Report dialog box for generating reports

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Creating Reports

```
dsreportgen -ui
```

- To open the Generate Report dialog box for generating reports for a specific project

```
dsreportgen -proj c:\network_switch\network_switch.cpm -ui
```

- To open the Create Report Template dialog box for creating report templates

```
dsreportgen -def_tmplt
```

- To open a report template for editing in the Create Report Template dialog box

```
dsreportgen -def_tmplt -tpt c:\network_switch\bom_report.tpt
```

- To open the User-Defined Columns dialog box for creating or editing user-defined query fields

```
dsreportgen -ccol
```

- To generate a report and store it in a specific .dsr file

```
dsreportgen -proj c:\network_switch\network_switch.cpm -tpt  
c:\network_switch\bom_report.tpt -format DSR -out  
c:\network_switch\bom_report.dsr
```

- To generate a report in the HTML format

```
dsreportgen -proj c:\network_switch\network_switch.cpm -tpt  
c:\network_switch\bom_report.tpt -format HTML
```

Generating Document Schematic for a Design

This chapter describes the following sections:

- [Overview](#) on page 558
- [Preparing Design for Document Schematic Generation](#) on page 559
- [Understanding Schematic Generation](#) on page 563
- [Generating Document Schematics](#) on page 570
- [Viewing Flat Document Schematics](#) on page 572
- [Features of the Document Schematic](#) on page 573
- [Generating Document Schematic in Preserve Mode](#) on page 585
- [Guidelines for Modifying Document Schematics](#) on page 586
- [Troubleshooting Document Schematic Generation](#) on page 588

Overview

System Connectivity Manager allows you to generate a schematic for your logical design. You can use the generated schematic for documentation purposes, or for communicating various aspects of the design to your team members or customers. Though the generated schematic is mainly for documentation purposes, if required, you can modify component placements and these can be preserved while regenerating the documentation schematic.



Document schematic must be used exclusively for documentation. While you can modify the placement of components and wires in the schematic, using document schematic for design tasks, and for running other tools and utilities is not supported. Also, documentation schematic does not contain constraint information captured using Constraint Manager launched from SCM.

The contents on the documentation schematic can be controlled using various setup options. For a detailed explanation of these options, see [Document Schematic Generation Setup](#) on page 810.

Using System Connectivity Manager, you can generate a flat schematic for your spreadsheet-based design. The process of generating document schematic is a two step process. In the first step, based on user preferences, schematic is generated for all table-based and verilog blocks in the design. These block-level schematics are created in the `docsch_1` view of each block.

Note: Document schematic is not generated for schematic blocks used in the design. This is because in case of schematic blocks, contents of the `sch_1` view are used as is in the document schematic.

In the second step, block-level schematics are used for generating a flat schematic for the complete project. The project-level schematic is a flat schematic created by concatenating the pages of all block-level schematic in the design. The project-level schematic is saved in the `sch_1` view of the `<root design>_doc` cell.

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Generating Document Schematic for a Design

Consider a MEMORY design that instantiates two blocks, CONTROL and ADDERGEN. If you generate document schematic for the MEMORY design, the view created will be as shown in the figure given below.



Important

`sch_1` view is available for project-level schematic, whereas only `docsch_1` view is available for blocks. To create the `sch_1` view for a block, do a change root in System Connectivity Manager to set the block as the root design and then generate the document schematic.

After you have generated the documentation schematic for the first time, for all other subsequent generations you can generate the documentation in the preserve mode. It is recommended that preserve mode must be used in cases where you have made placement modifications to the generated schematic and do not want these changes to be overridden. To know about the features of the document schematic generated in preserve mode, see [Generating Document Schematic in Preserve Mode on page 585](#).

Caution

To make placement modifications to a block-level document schematic, you need to open the block in master mode. All placement changes made to the master block are saved in the `docsch_1` view.

Preparing Design for Document Schematic Generation

Before you generate the document schematic for your design, do the following:

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Generating Document Schematic for a Design

- Ensure correct symbol association for each component used in the design. For example, if you have added a component as a package in the design, ensure that corresponding symbol for the package exists.
- Ensure that the libraries in which the page border and TAP symbols you want to use for generating the document schematic exist, are defined in the `cds.lib` file for your project and added to the list of project libraries. You can add libraries for the project using the Libraries tab of the Setup dialog box. You can specify the symbols you want to use for generating the document schematic in the Symbols tab in the Document Schematic Generation Setup tab of the Setup dialog box.
 - If the specified page border symbol is not found in the library, the document schematic will not be generated.
 - If the default TAP symbols are not found in the library, System Connectivity Manager generates the symbols in the design library where the cell for the root or top-level design exists.

Comment bodies used as CTAP is not supported in document schematic generation.

Note: If you are selecting symbols from any library other than the Cadence standard library, ensure that the symbols conform to the Cadence library standards described in the *Allegro Design Entry HDL Reference Guide*. Information on TAP symbols is available in the *TAP Symbols* section of *Appendix C, Using the Standard Library Symbols* of the user guide.

- Specify all the setup options required for document schematic generation. To know more about these options, see Document Schematic Generation Setup on page 810.
- To ensure that the VOLTAGE property attached to power nets is available in the generated document schematic, it is recommended that power symbols should be used in the generated document schematic. For specifying power symbols to be used in the design, use the Power tab of the Document Schematic Generation Setup dialog box.
- When generating the document schematic for a design, System Connectivity Manager uses the logic grid settings for schematic pages to place components and route the design. It is recommended that you use a smaller logic grid, as using a larger logic grid may result in irregular placement and routing in the document schematic. The recommended grid size is 50.

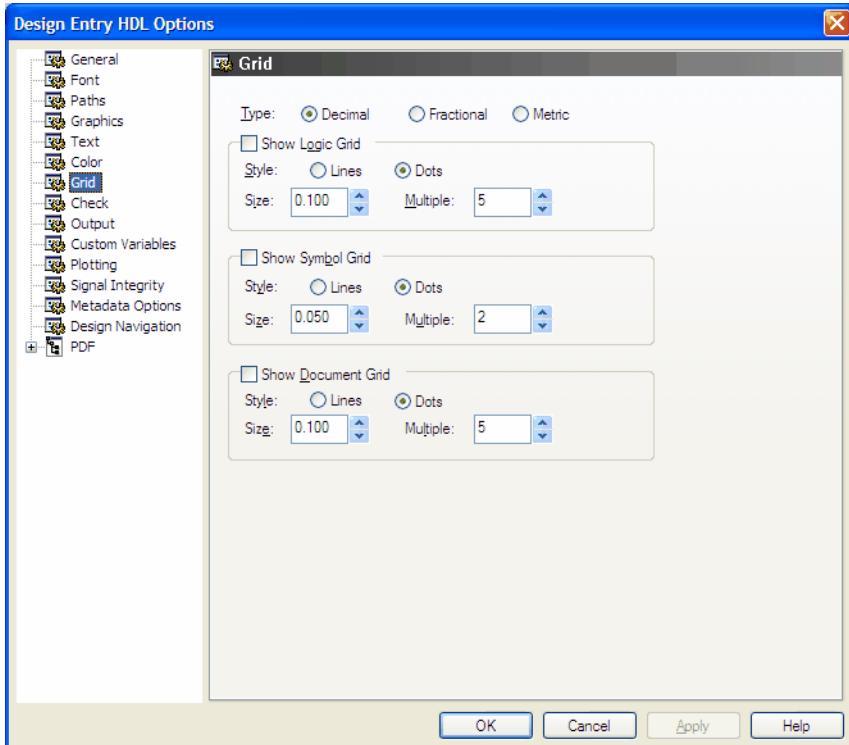
To specify the logic grid for the document schematic, do the following:

- a. Exit System Connectivity Manager.
- b. Open the project in Design Entry HDL.

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Generating Document Schematic for a Design

- c. Choose *Tools – Options*.
- d. Select the *Grid* from the navigation pane.



Note: The grid settings in SCM are independent of the grid settings in Design Entry HDL. There is no correlation between the grid settings in SCM and the grid settings in Design Entry HDL. When a schematic is generated, the grid settings of Design Entry HDL are not honored. To make sure that the components placed by SCM appear on the grid in Design Entry HDL, you may need to change the grid settings in Design Entry HDL. For example, for a SCM schematic grid setting of 25, you need to use the Logical Grid setting in Design Entry HDL to be 0.05 <> and multiple 2.

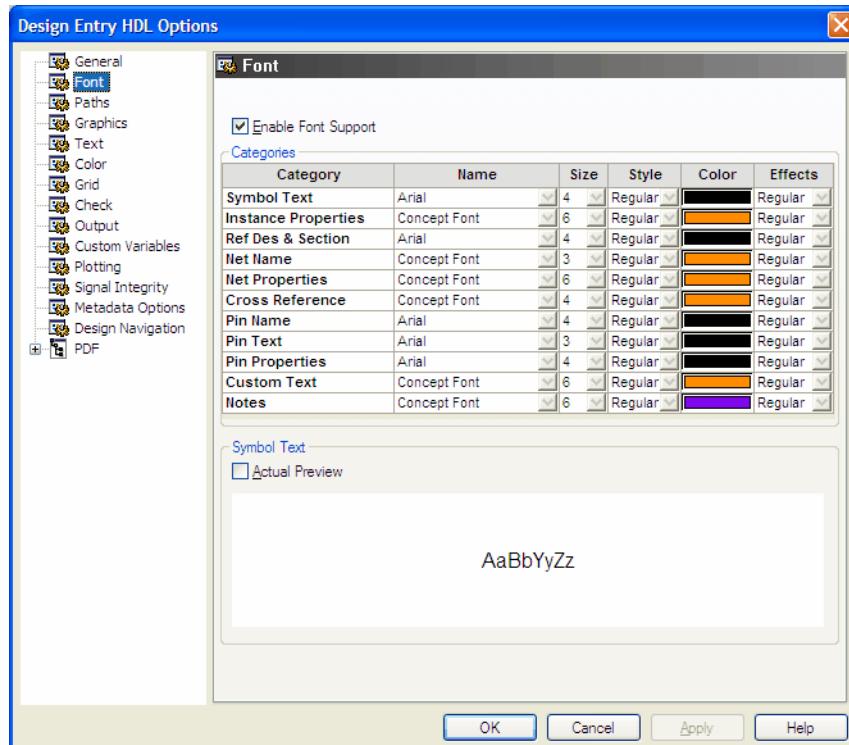
- e. Modify the logic grid settings, if required.
 - f. Click *OK*.
 - g. Exit Design Entry HDL.
 - h. Re-open the project in System Connectivity Manager.
- When generating the documentation schematic, you can specify the fonts to use in the the generated schematic.

To specify the font settings of the generated schematics, do the following:

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Generating Document Schematic for a Design

- a. Exit System Connectivity Manager.
- b. Open the project in Design Entry HDL.
- c. Choose *Tools – Options*.
- d. Select the *Font* from the navigation pane.



- e. Modify the Font settings, if required.
- f. Click *OK*.
- g. Exit Design Entry HDL.
- h. Re-open the project in System Connectivity Manager.

Understanding Schematic Generation

Schematics are generated based on inputs System Connectivity Manager gets from Setup options and design directives. A combination of these, along with the input design largely determine the look of the generated schematic. This section outlines the basics, and how you can tweak the generated schematic.

- [Placement and connectivity](#)
- [Placement of associated components](#)
- [Placement of components and groups](#)
- [Specifying area utilization](#)

Placement and connectivity

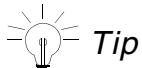
The connectivity of the symbols determine the placement in the generated schematic. If a component is connected to several other components, the most densely connected interface is placed first. This is followed by the next densely populated interface, and so on.

Placement of associated components

Associated components are placed on the generated schematic based on the following outlines.

Bypass capacitors

By default, bypass capacitors are placed on the page where the last symbol is instantiated. For most of the components, the last symbol is the power symbol, so bypass capacitors are usually placed on the page that contains the power symbols.



To place bypass capacitors with a specified symbol use the `PLACE_BYPASS_WITH_SYMBOL` property. For example, `PLACE_BYPASS_WITH_SYMBOL=3` places the bypass capacitors with `Sym3` of the instance.

Specifying number of bypass capacitors in a rail

You can also specify the number of bypass capacitors to be placed on a rail using the setup options.

In the Document Schematic Setup dialog box's *Associated Components* tab, specify the *Maximum number of components in a rail*.

Terminations and Pullups/Pulldown Resistors

The most common termination used is the series termination, and it is placed inline with the source. In case of buses and large number of signals, the placement of terminations is staggered.

Specifying number of terminations in a rail

You can also specify the number of terminations to be placed on a rail using the setup options. In the Document Schematic Setup dialog box's *Associated Components* tab, specify values the *Maximum number of components in a rail* area.

Placement of components and groups

You can control placement of the components on pages using several methods. Namely these are:

- [Force placement on same sheet](#)
- [Specifying placement as per design capture](#)
- [Specifying place order manually](#)
- [Placing different groups on different pages](#)
- [Ignoring Sections of Design in the Schematic](#)

Force placement on same sheet

By default, the component placement in the document schematic is based on connectivity. System Connectivity Manager provides you with the ability to specify components that are to be grouped together in the generated document schematic. You can use the SCHEMATIC_GROUP property to specify the component grouping. The value of this

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Generating Document Schematic for a Design

property can be set to any alphanumeric string. For example, 01CPU, 02CLOCK, 03MEMORY.

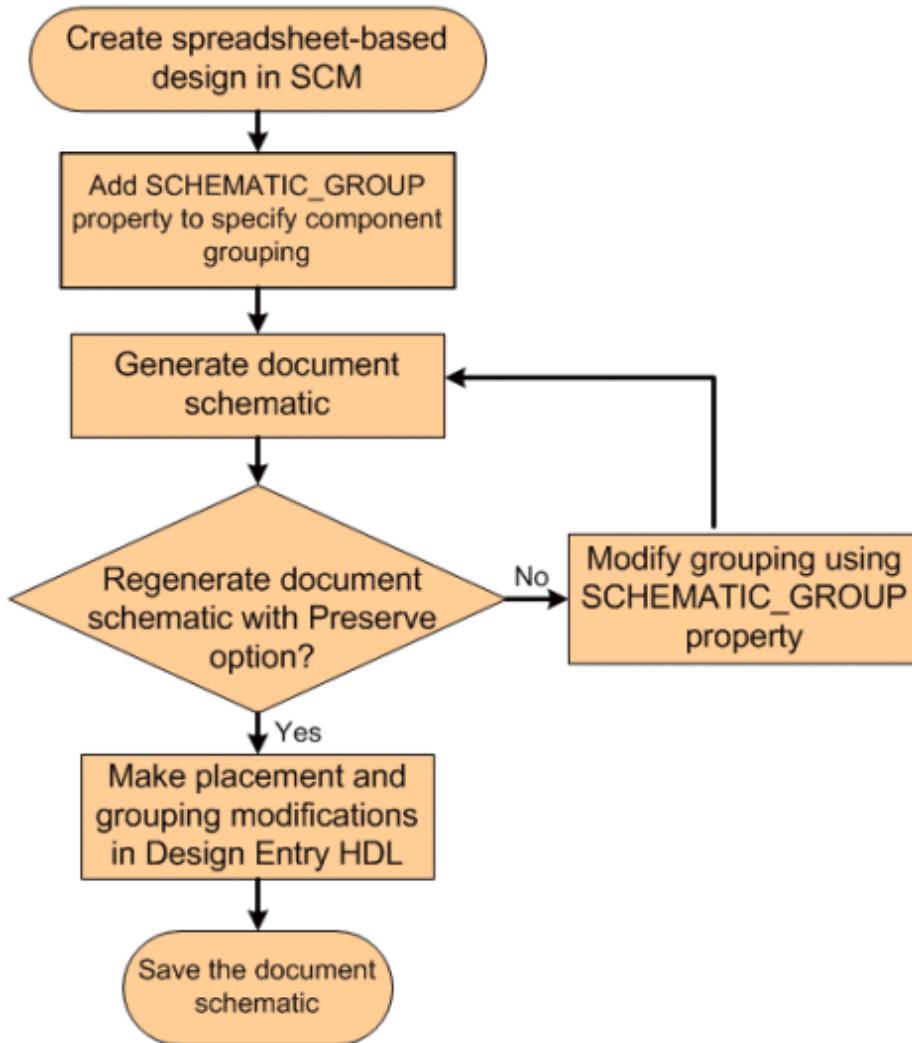


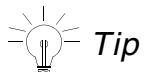
Figure 21-1 Using SCHEMATIC_GROUP property

To force a set of components to be placed together in the document schematic, the value of the SCHEMATIC_GROUP property attached to these components should be same. For example, if you want an instance of 1s00 and an instance of 1s04 to be placed together, assign the SCHEMATIC_GROUP property with its value set to 1GROUP for both these components.

In the generated schematic, the group that has the lower value for the SCHEMATIC_GROUP property is given a higher priority. For example, if there are two groups to be created based on the value of the SCHEMATIC_GROUP property. For one group the value of the SCHEMATIC_GROUP property is set to 2 and for the other group it is set to 3. In this case, in the generated document schematic group with the value of the SCHEMATIC_GROUP property is set to 2 will be placed first.

In the spreadsheet design, if you add the SCHEMATIC_GROUP property to a package, all symbols associated with that package are placed together in the generated document schematic.

If a single schematic page is not enough to accommodate all the components in a schematic group, then the spill over components are placed on the immediate next page. Within a schematic group, component placement is guided by the component connectivity. Tightly coupled components are usually placed together and least connected components spill over to next page.



Tip

If required, you can display the SCHEMATIC_GROUP property as a column in Component List pane. This column can then be used to quickly verify if the SCHEMATIC_GROUP property is attached to all the required components or not. To know how to customize System Connectivity Manager, to display a property as a column, see [Customizing the Spreadsheet Editor](#) on page 650. Similarly, you can also customize the Constraint Manager to display SCHEMATIC_GROUP property as a column in the worksheet. To know about the steps required to add a new attribute to a worksheet, see [System Connectivity Manager to Constraint Manager User Guide](#).

Besides using the SCHEMATIC_GROUP property, you can also use the Document Schematic setup options for controlling some aspect of component placement. For example, selecting the *Place each group of component on a separate page* check box, on the Placement tab of the Document Schematic Generation Setup dialog box, ensures that component groups are placed on separate schematic pages.

Specifying placement as per design capture

Manually edit the project file (*<project>.cpm*) to add the placement_within_group_using_order_in_design directive.

- Add the directive in the START_DSSCHGEN section of the *<project>.cpm* file.
- Set the value of the directive to 1.

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Generating Document Schematic for a Design

A section of the `<project>.cpm` file with the directive added is shown below.

```
START_DSSCHGEN
placement_within_group_using_order_in_design '1'
add_comments_to_pins '1'
use_block_symbol '1'
ignore_instance_with_errors '1'
ignore_blocks_without_schematic '1'
run_crossreferencer '1'
END_DSSCHGEN
```

When you generate the document schematic after adding the directive to the project file, component instances are placed in the schematic in the order in which they are added to the design. This implies that if the directive value is set to 1, the placement of components that belong to same schematic group is based on the instance values, as listed in Component List pane.



A side effect of this directive is that symbols that belong to the same chips instance will be placed on contiguous pages, and mixing of symbols with other instances might happen on first or last page in the set of pages that contain the chips instance symbols.

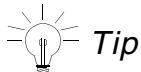


The cpm directive is always used along with the SCHEMATIC_GROUP property. Specifying cpm directive without using the SCHEMATIC_GROUP property, will not impact component placement in the generated schematic.

Specifying place order manually

You can use the SCHEMATIC_PLACE_ORDER property to explicitly specify the order in which components with in a group should be placed in the document schematic.

The component placement is based on the integer value assigned to the SCHEMATIC_PLACE_ORDER property. The components are placed in the ascending order of property values. Therefore, a component with the value of SCHEMATIC_PLACE_ORDER property set to 1 will be placed before the component with the property value set to 2.



Tip

In a design, if both — the cpm directive and the SCHEMATIC_PLACE_ORDER property — are specified, the SCHEMATIC_PLACE_ORDER property has a higher precedence over the cpm directive.

Recommendations

- In a schematic group, if more than one component has same place order specified then there are no set patterns about which component will be placed first. To avoid this ambiguity, it is recommended that within a schematic group, you should use unique values for the SCHEMATIC_PLACE_ORDER property.
- For a schematic group, if you want to override the placement order specified by the cpm directive, it is recommended that the SCHEMATIC_PLACE_ORDER property is specified for all the components in the group. This is required to ensure that no two components within a schematic group have the place order.

Within a schematic group, if the cpm directive for specifying placement order within a group is set, and the SCHEMATIC_PLACE_ORDER property is specified only for selected components, there might be a situation where a component has instance name as i5 and another component has the value of SCHEMATIC_PLACE_ORDER property set to 5. In this case, the required component placement order is not guaranteed as more than 1 component has same value for the place order.



Within a schematic group, you cannot specify the place order for instances that are added as a package in System Connectivity Manager, and map to multiple symbols.

Placing different groups on different pages

You can place different groups, specified by SCHEMATIC_GROUP property, on different pages by specifying this in the Setup options.

In the Document Schematic Setup dialog box's Placement tab, check *Place each group of components on a separate page* to enable this option.

Ignoring Sections of Design in the Schematic

When you generate the document schematic for a spreadsheet-based design, the document schematic is generated for all the components in your design. However, if required, you can specify the components or the blocks in your design that you want to ignore during the schematic generation process. To selectively ignore components or blocks for generation of the document schematic, add the IGNORE_IN_DOCSCHGEN property on all the components and blocks to be ignored.

In case you add the IGNORE_IN_DOCSCHGEN property on a hierarchical block, the complete block—including the sub-blocks—is ignored during the schematic generation process.

Specifying area utilization

There are several options that you can use to specify the area utilization and spacing between components that you can specify.

Specifying page margins

You can specify the margins on a page. The symbols are placed within the margins specified.

In the Document Schematic Setup dialog box's Placement tab, specify the *Page Margins* in the *Top, Left, Bottom and Right* fields.

Specifying spacing between components

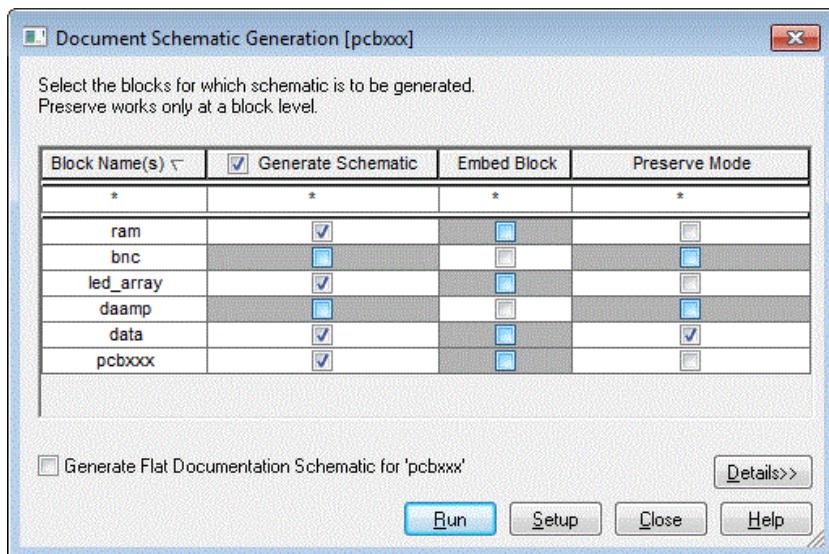
You can specify the minimum spacing between any two components that are placed on a schematic page.

In the Document Schematic Setup dialog box's Placement tab, specify the *Component to Component Spacing*. This is the grid spacing between any two components, as a multiple of the grid size.

Generating Document Schematics

1. Choose *Project – Generate Schematics*.

The Documentation Schematic Generation dialog box appears.



2. The Block Name(s) column lists all the blocks instantiated in the design at different levels. To generate the document schematic for a block, select the *Generate Schematic* check box for the corresponding check box.

Note: The first block in the list is the root design itself.

The document schematic for the selected blocks is generated in the `docsch_1` view.

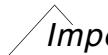
Note: If you are generating the project schematic for the first time, ensure that all document schematic is available for all lower level blocks. Therefore, it is recommended that all *Generate Schematic* check box should be selected for all lower-level blocks.

3. To replace the schematic blocks with actual schematic in the project level schematic, select the *Embed Block* check box.



The *Embed Block* check box is enabled only if the schematic block has a single page schematic. This option is not available for schematic blocks with multiple schematic pages.

4. If you are regenerating the schematic, select the *Preserve Mode* check box to prevent the placement modification made by you in the existing documentation schematic.

 *Important*

For the *Preserve* check box to be enabled, the `docsch_1` view containing the document schematic should be available.

To know more about generating document schematic using *Preserve Mode* option, see [Generating Document Schematic in Preserve Mode](#) on page 585.

5. Select the *Generate Flat Documentation Schematic for <root_block>* box if you want to generate a flat document schematic for the complete project in Design Entry HDL.

Note: The Flat documentation schematic is created in the `sch_1` view, of `<root_block>_doc` directory.

 *Caution*

The changes made to the Flat schematic cannot be preserved. Only the changes made to the block level schematics can be preserved.

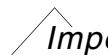
6. Click *Setup* to specify the settings for generating the document schematic for your design.

The Document Schematic Generation Setup dialog box appears. For more information on changing the settings for generating the document schematic, see [Document Schematic Generation Setup](#) on page 810.

Note: When you generate the document schematic, the schematic blocks in the design are copied without any changes into the document schematic. Hence the setup options you specify in the Document Schematic Generation Setup dialog box will not have any effect on the pages created for the schematic blocks in the document schematic.

7. Click *Run* to generate the document schematic for the design.

The Flat Documentation Schematic is created in the `sch_1` view of the `<root_block>_doc` cell for the root design. For each block, the Block Schematic (for Placement and routing preserve) is created in the `docsch_1` view of the block.

 *Important*

Constraint information captured in SCM is not passed to the generated document schematic.

Note: If the schematic generation fails for some component, ensure that correct library parts used. Some of the possible reasons for the failure of document schematic generation process are:

- Errors exist for the part.
- If the following error message is reported for a component in the Schematic Generation dialog box:

Instance <instance_name> was added as package. Unable to find appropriate symbol(s) for it.

Ensure that the association of the package with the symbol is correct.

Viewing Flat Document Schematics

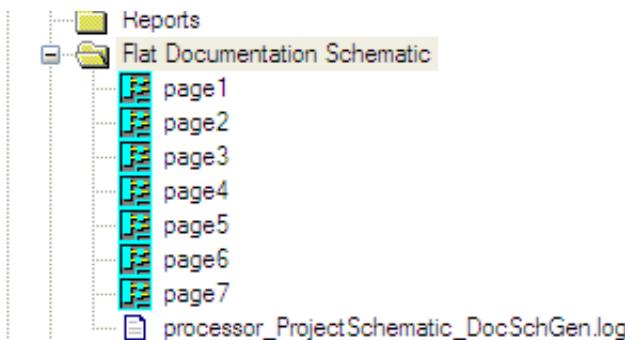
To view the document schematic in Design Entry HDL you can either select the appropriate *Launch Design Entry HDL* check box in the *Document Schematic Generation* dialog box or open the document schematic page from the File Viewer in System Connectivity Manager.

To know how to open the schematic document using the options in the *Document Schematic Generation* dialog box, see [Document Schematic Generation](#) on page 719.

You can view the document schematic for your design in System Connectivity Manager by doing the following:

1. Choose *View – File Viewer* to display the File Viewer.
2. Double-click on the *Output Files* folder.
3. To view the project schematic, double-click on the *Flat Document Schematic* folder.

The list of schematic pages in the document schematic for the project is displayed as shown in the figure below. Along with the schematic page a log file is also visible. This log file lists all the messages thrown during the document schematic generation process.



4. To open a schematic page for viewing in Design Entry HDL, double-click on the page.

Note: Alternatively, right-click on the page and choose *Launch Design Entry HDL*.

The page opens in Design Entry HDL. Using the Previous Page and Next Page tool buttons, you can view all the pages in the generated document schematic.

Viewing Block Schematics

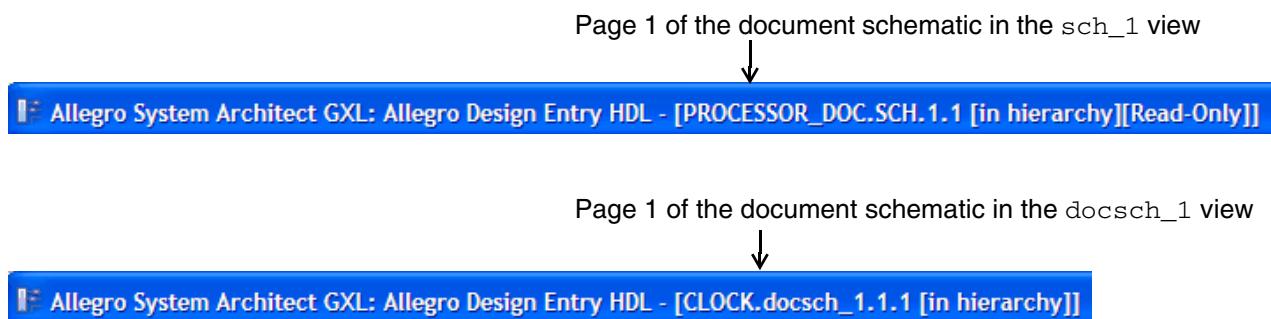
Document schematic for a block is generated only if you select the *Generate Schematic* check box for the corresponding block in the Document Schematic Generation dialog box. Pages for block-level schematic are listed below the Block Schematic folder.

To view a page in the Block Schematic folder:

- Double -click on a page below the *Block Schematic (for Placement and Routing preserve)* folder.

The schematic is displayed in Design Entry HDL.

When you open any page of the flat document schematic, the name of the root design, and the view containing the generated document schematic is visible in the title bar, as shown in the figure given below.



Features of the Document Schematic

The document schematic has the following features:

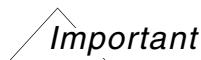
- The document schematic is only meant for documentation purposes. In the preserve mode, you can do placement modifications in the document schematic.
- Constraints added to the SCM design, are not available in the document schematic.
- The document schematic is always a flat design.

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Generating Document Schematic for a Design

If the source design in System Connectivity Manager is a hierarchical design, the design is flattened as described in [Representing Hierarchical Designs in the Document Schematic](#).

- The schematic blocks in the SCM design are copied without any changes into the document schematic.
- In the documentation schematic, connectivity is specified using net names. Physical net names, displayed near the component pins, are used for specifying net connections.



System Connectivity Manager supports signal names, such as `a<3>_1` and `*_1`, which are not supported in Design Entry HDL. To overcome this problem of mismatch in the naming convention used, the `SIG_NAME` property is added to the signals in the generated document schematic. For signal names that are supported both in SCM and DEHDL, the value assigned to the `SIG_NAME` property is the same as the value assigned to the `PHYS_NET_NAME` property. However, for signal names not supported in Design Entry HDL, the `SIG_NAME` property is assigned a different value that is acceptable in DEHDL.

- Schematic generation is done based on the physical design. As a result, net aliases are not tracked. Only base net names are used.
- Comments added to a design in System Connectivity Manager are displayed as notes in the document schematic, provided you had selected appropriate options in the [Comments](#) tab of the Document Schematic Generation Setup dialog box.
- Cross references are placed only on the project-level schematic.
- If document schematic has offpage connectors added to it, cross references are placed on the symbols for the offpage connectors.
- If offpage connectors are not available, and in the Cross Referencer Options dialog box the *Cref Signals not connected to Flagbodies* is selected, cross references are placed on the net ends.
- If you have selected the option to add offpage connectors, offpage connectors will only be added for signals that run across pages. For signals terminating on the left- or right side of the schematic page, the symbols specified in the setup dialog box for the right side or the left side are used.
- In the generated document schematic, offpage connectors are not added to global and template nets, and to nets with power bodies.
- Ports and IO pins are not placed in the documentation schematic. However, if ports and IO pins are present in the schematic blocks, they are not modified.

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Generating Document Schematic for a Design

- If required you can modify the schematic design to change component placement.
- You can plot the document schematic in Design Entry HDL. However, as the document schematic is a flat schematic, do not use the hierarchical plotting option in Design Entry HDL.
- You can also run PDF Publisher on the document schematic. However, before you need to reset module order from Design Entry HDL. To reset module order do the following:
 - a. Open the design in Design Entry HDL.
 - b. Right-click in the Hierarchy Viewer window.
 - c. From the pop-up menu, choose *Reset Module Order*.
- Properties on components and pins are displayed on the document schematic. The only signal property which is always visible, irrespective of the values defined in the setup options, is the `SIG_NAME` property.
- Similar to the `SIG_NAME` property, the `$LOCATION` and `$PN` properties are also not governed by the values specified in the setup dialog box. Irrespective of the setting, only the value of the `$LOCATION` is always displayed on the documented schematic. Similarly, the value of `$PN` property is also visible.
- If a property has a placeholder on the symbol for the component, the location, visibility, justification, rotation and color of the placeholder for the property will be retained in the document schematic, irrespective of the property color and display settings in the Document Schematic Generation Setup dialog box.

Note: Cadence recommends that you provide placeholders for pin properties on the symbol for the component so that properties are displayed without cluttering the document schematic.

- To prevent unnecessary clutter in the document schematic, any pin property, except the `PN` property, that does not have a placeholder on the symbol for the component will not be displayed on the document schematic.
- The `PN` property on a pin is handled in a special way in the document schematic. The value of the `PN` property will always be displayed on the schematic in white color, irrespective of the property color and display settings in the Document Schematic Generation Setup dialog box.
- If a symbol is larger than the page border size, an attempt is made to instantiate the symbol by rotating the symbol such that it fits within the page border size. In such cases, success is not always guaranteed.

Representing Associated Components in the Document Schematic

In the generated document schematic, associated components, such as bypass capacitors, terminations, and pull-up and pull-down resistors, are added as rails near the parent component. This arrangement is followed within a schematic group as well. For example, if you use the SCHEMATIC_GROUP property to create a schematic group containing two ICs and their associated components, in the generated document schematic, associated components will always be placed with the corresponding IC.

The rail formation depends on the separation between two components in a rail and also on the number of components that can be added to the rail. The separation and the number of components is specified using the setup options.

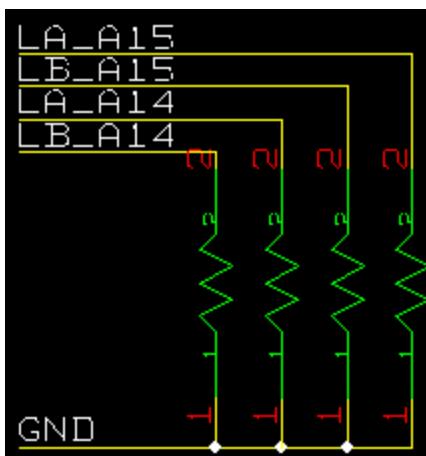
To know more about the setup options for placing associated components, see [Associated Components tab](#) on page 821.

Horizontal and Vertical Rails of Associated Components

Components when placed together in a column, they form a vertical rail. Components placed together in a row form a horizontal rail.

- Associated components of the same type are grouped together in a rail.

For example, all bypass capacitors related to the same parent symbol are grouped as a rail. Similarly, separate rails are generated for other associated components such as, terminations, pull-ups, and pull-downs.



- Rails of the component connected to a pin are placed on the side where the pin is located.

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Generating Document Schematic for a Design

- If the rail size is such that all the components in the rail cannot be accommodated in the same schematic page, then the components are placed in the next page.
- Loose Pullup/Pulldown are dumped in the last page of the document schematic.



Associated components are always placed near the parent symbol. This is TRUE even in case of schematic groups created using the SCHEMATIC_GROUP property.

If you use the SCHEMATIC_GROUP property to create a schematic group containing multiple ICs and their associated components, in the generated document schematic, associated components will always be placed with the corresponding IC.

Differential Pair Terminations in Document Schematic

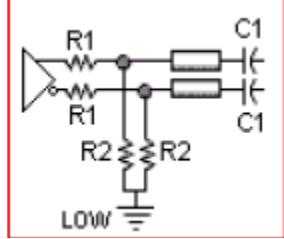
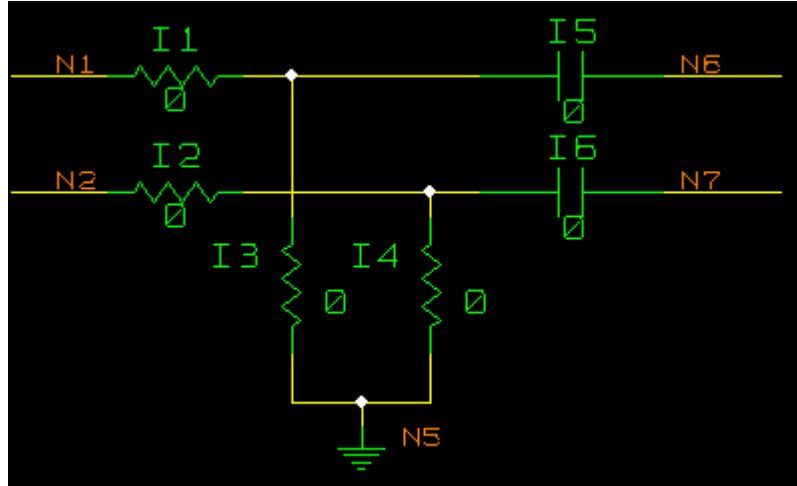
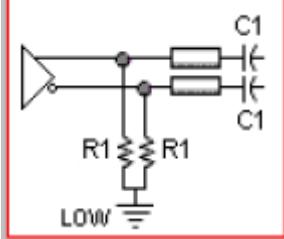
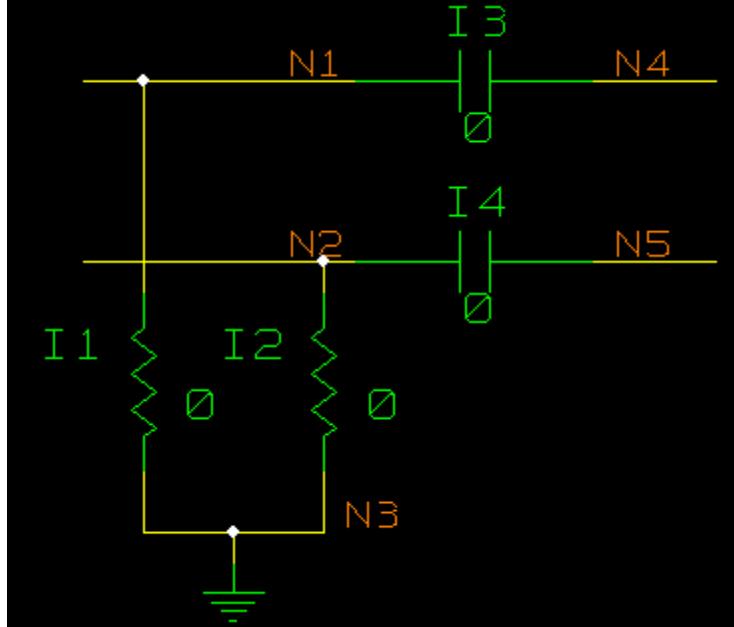
If your design has terminations applied to differential pair pins, the document schematic for these terminations is created using the predefined templates available at `<install_dir>/share/cdssetup/tdd/termination_templates`.

The mapping of the termination components to the schematic design is shown in the table given below.

Termination Type	Corresponding Schematic
AC Bias	

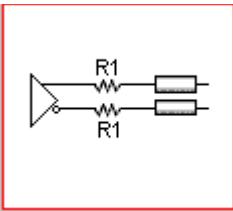
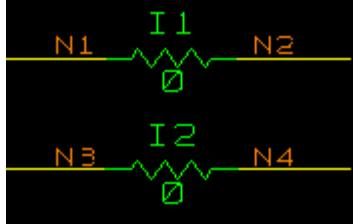
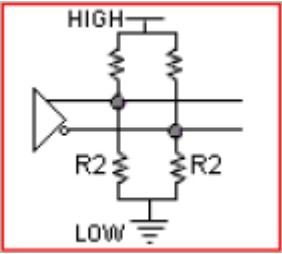
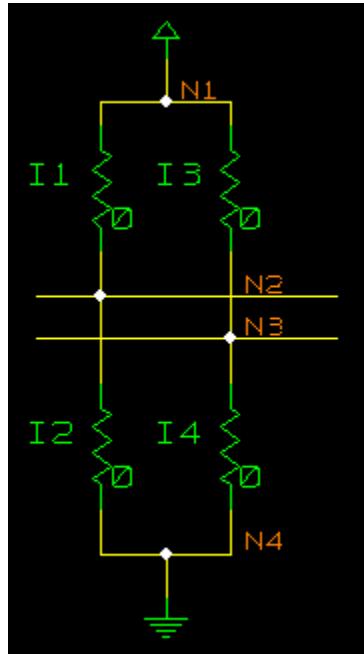
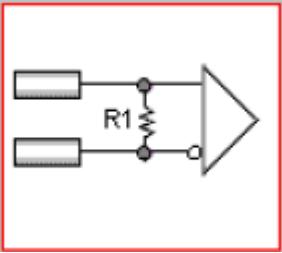
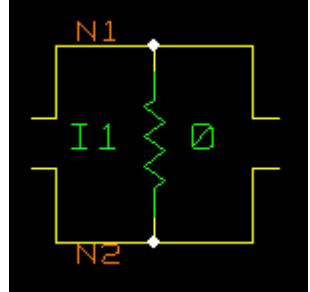
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Generating Document Schematic for a Design

Termination Type	Corresponding Schematic
ACCT1 (AC-Coupled Transmission Lines)	 
ACCT2	 

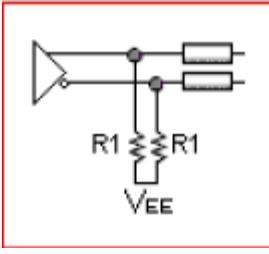
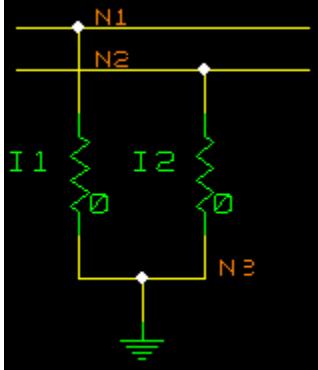
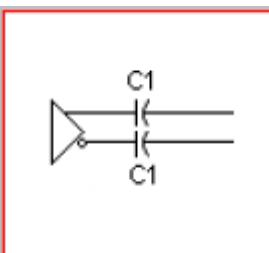
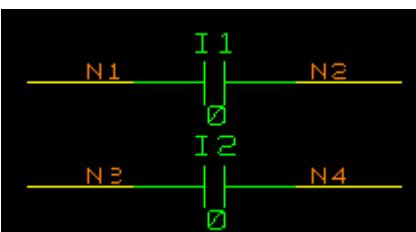
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Generating Document Schematic for a Design

Termination Type	Corresponding Schematic
DPSeries	 
DPThevenin	 
LVDS	 

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Generating Document Schematic for a Design

Termination Type	Corresponding Schematic
Parallel	 
SeriesCap	 

Note: If a design has long names for the nets attached to the differential pair terminations, then the generated document schematic might have wire names that extend beyond the stubs. This is because the stub size in the template schematic is not adjusted according to the signal name.

If for a termination, you want to modify the predefined schematic specified in the template, you can do so by following the procedures documented in the [Appendix B, “Customizing Termination Templates.”](#)

Representing Hierarchical Designs in the Document Schematic

The document schematic generated by System Connectivity Manager will always be a flat design.

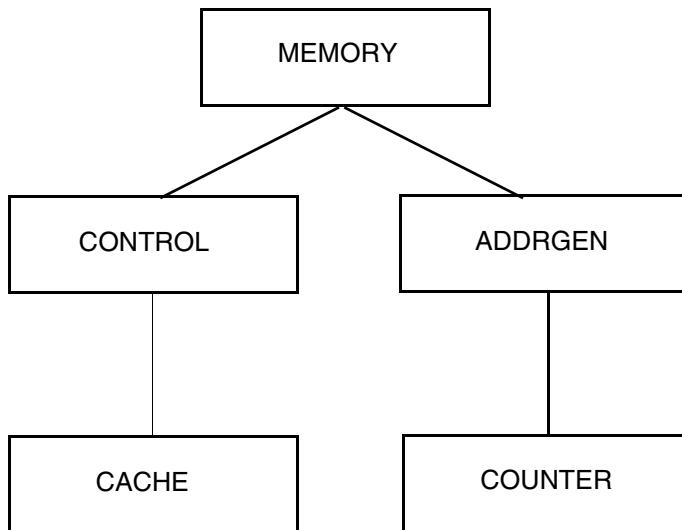
Hierarchical schematic generation is not supported. However, System Connectivity Manager supports generating documentation schematic at the project level as well as at the block level. Therefore, in case of hierarchical designs, you can generate a separate schematic for each hierarchical block and then create a project level design that instantiates each block.



When you open the project level schematic in Design Entry HDL, you cannot descend into the hierarchical block symbol instantiated in the project level schematic.

If the source design in System Connectivity Manager is a hierarchical design, the design is flattened in the order in which it is displayed in the Hierarchy Viewer.

For example, consider the hierarchical design shown in the figure given below.



The same design displayed in the Hierarchy Viewer of System Connectivity Manager is shown below.



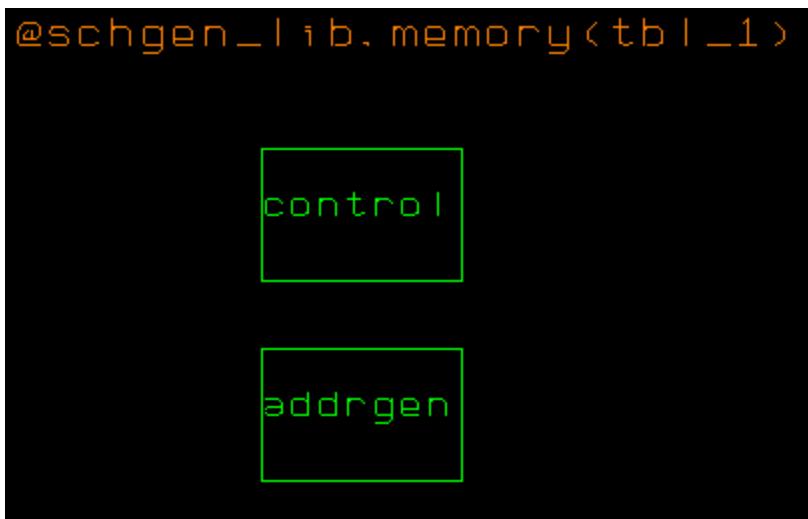
If you generate the document schematic for this design, the order of pages in the generated schematic will be as listed below.

1. First page has schematic for the root design `memory`.
2. Next, schematic page is for the `control` block.

3. Next, the schematic page for the `addrgen` block is added.
4. Next, the schematic page for the `cache` block is added.
5. Finally, the schematic page for the `counter` block is added.

The document schematic for a hierarchical design has the following features:

- Based on whether the setup option, *Create and add symbols for hierarchical blocks* check box, is selected or not, the generated schematic may or may not have the symbols created for each block in a design. For example, the following figure displays the block diagrams for the `control` and `addrgen` blocks in the schematic page for the `memory` block.



Note: The symbols are only for display purposes. You cannot descend into the blocks using the Descend toolbar button in Design Entry HDL to view the schematic pages for the block.

Adding Cross References to the Document Schematic

System Connectivity Manager provides support for adding cross references to the project-level document schematic. To add cross references to the document schematic, you need to:

- specify the `cref.dat` file to be used, and
- select the option to run Cross Referencer.

Specifying the `cref.dat` file

To specify the `cref.dat` file, modify the setup.

- 1.** Open the Document Schematic Generation Setup dialog box using one of the following methods.
 - Choose *Project – Settings* to display the Setup dialog box. Click the Schematic Generation tab.
 - Choose *Project – Generate Schematics* to display the Document Schematic Generation dialog box. Click the *Setup* button to display the Document Schematic Generation Setup dialog box.
- 2.** Select the General tab.
- 3.** In the *Page Border Information file* text box, specify the `cref.dat` file to be used.

Specifying the option to run Cross Referencer

To add cross references to the document schematic, you first need to specify appropriate setup options, and then generate the document schematic.

- a.** Open the Document Schematic Generation Setup dialog box.
- b.** Select the Cross Referencer tab.
- c.** Select the *Run Cross Referencer on the project schematic* check box.
- d.** If required, you can specify Cross Referencer options in the Cross Referencer Options dialog box. To launch this dialog box, click the *Cross Referencer Setup* button.
- e.** Click *OK* to save the modifications to the setup.

If you now generate the document schematic, cross references are added to the project schematic.

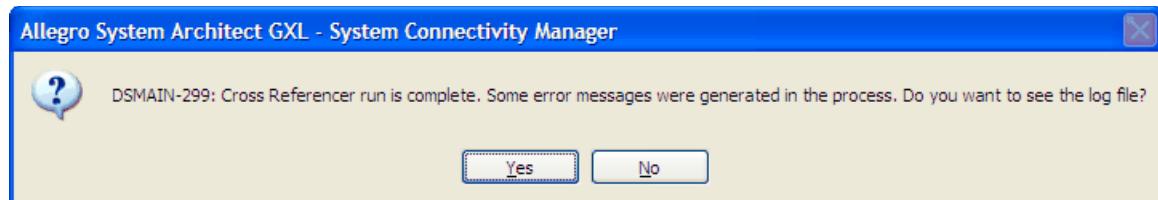
Adding Cross References to an Existing Document Schematic

To add cross references to a project schematic without having to regenerate the schematic, do the following.

- 1.** Choose *View – File Viewer*.
- 2.** In the File Viewer, right-click on the *Flat Document Schematic* folder.

3. From the pop-up menu, choose *Launch CreferHDL*.

The Cross Referencer tool runs from the command line. After the tool is run, following message is displayed.

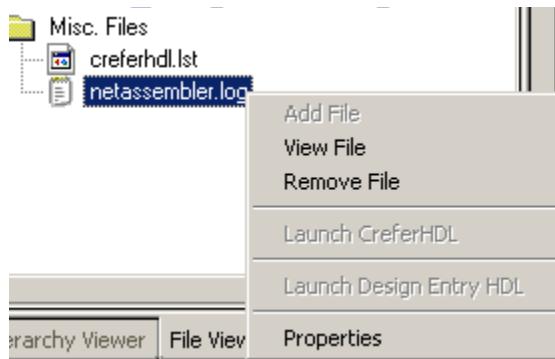


Selecting the Yes button opens the `netassembler.log` and `creferhdl.lst` files for viewing.

The files generated by Cross Referencer are also listed in the File Viewer. After you run Cross Referencer, the File Viewer is automatically updated to list any new files or schematic pages that might get added as a result of running cross referencer on the project-level document schematic.

For example, the log files are listed below the Miscellaneous Files folder.

- To open these files for viewing, right-click on the file name and from the pop-up menu choose *View File*.



Embedding Schematic Blocks

The block flattening or embedding feature is available for schematic blocks with a single page schematic that might or might not have a page border. For a schematic block, *Embed Block* option is enabled only if the following conditions are satisfied.

- The schematic block has a valid `sch_1` view.

Note: The block flattening option is not available for table blocks with `sch_1` view that

gets created after you generate the document schematic for the block.

- The schematic is a single page schematic. For this, the `sch_1` view of the schematic block should only have page1.
- The `sch_1` view must have a `.csb` file.

Note: This file is created when you save your schematic design in Design Entry HDL.

- Ideally, the schematic page should not have a page border, or the page border should be the same as the page border specified in the *General* tab of the Document Schematic Generation Setup dialog box.

Note: For blocks with page borders, page borders are ignored while reading the flattened block.

The block flattening option together with the `SCHEMATIC_GROUP` property can be used to place single-page schematics together on a single page, thereby reducing the page count in the generated document schematic.

 **Important**

If you select the *Embed Block* option, all instances of that block in the design are flattened. The flattening happens at the block-level to ensure that the placement modifications in the schematic block are preserved.

Generating Document Schematic in Preserve Mode

Preserve option is useful if you are regenerating your document schematic and want to preserve the modification done to the document schematic generated initially. In this mode, modifications made to the original document schematic are preserved.

 **Important**

Preserve option is valid for block level document schematic in the `docsch_1` view. The document schematic for the root design, available in the `sch_1` view cannot be preserved.

Features of Generating a Document Schematic with Preserve Option

- Component placement is always preserved.

- Routing changes are preserved only if there are no connectivity changes. In case of connectivity changes, the nets on the page for which connections have been modified, are rerouted.
- Only the comments originally added in System Connectivity Manager are preserved. Any new comments added to the design, or modifications made to the comments in the generated schematic are not preserved.
- Setup options related to number of associated components in a rail are valid for new components and schematics only. These do not hold true while regenerating a documentation schematic with preserve options. For example, consider that the setup option for document schematic generation is set to allow a maximum of 5 resistors in a rail. Any new rail that gets created will honour this directive. But an existing rail with 7 resistors will not be modified while recreating a documentation schematic with preserve options.
- Modifying page borders with preserve option on is not supported. This means that if the user changes the page border and also regenerates the schematic with preserve option selected, the schematic will not be preserved. In such scenarios, an error is thrown and the schematic generation process stops.
- New components added to the design are placed on the last page of the document schematic.
- New components added to an existing schematic group are placed in a new page added immediately after the page on which other components of the same group exist.
- In a design, if you add the IGNORE_IN_DOCSCHGEN property on a component and regenerate the document schematic with the preserve option selected, the output is the same as it is if the component was deleted from the spreadsheet design.

Guidelines for Modifying Document Schematics

It is recommended that all modifications to be made to a document schematic, should be done to the master block-level schematic, saved in the `docsch_1` view. This is because the Preserve option is available for block-level schematic only. The project schematic, saved in the `sch_1` view, is always regenerated based on the block-level schematic available in the `docsch_1` view. Some of the guidelines for modifying a document schematic are listed below.

- To add a Table of Contents (TOC) to the generated schematic:
 - If your design is not complete, add the TOC to the `docsch_1` view of the top-level block. Use the Preserve option to retain the TOC in subsequent generations.
 - If your design is complete, add the TOC to the `sch_1` view of the schematic.

System Connectivity Manager User Guide

Generating Document Schematic for a Design

Note: If your design has an imported Concept block that contains its own TOCs, those will get added to the schematic every time you regenerate. When you have a final version of the schematic, you can clean it up by deleting the TOCs that belong to the imported Concept blocks.

- By default, the component placement in the document schematic is based on connectivity. Therefore, while you are modifying the component placement, it is recommended that the signal flow should be from left to right or from driver to receiver.



Global routing is not supported.

- Placement and routing modifications involving components and nets that are the part of the flattened block are not preserved. This is because, the schematic block to be flattened is copied and pasted every time the document schematic is generated, with or without the Preserve option. Therefore, all modifications must be made to the schematic block and not in the flattened block.

Troubleshooting Document Schematic Generation

If the document schematic generation process fails for your design, the first task is to check the generated log file. This log file is named schgen.log and is located in the `temp` folder of the root design.

Table 21-1 Possible causes and resolutions for the failure of document schematic generation process

Problem	Cause and Troubleshooting steps...
Page border not specified.	<ul style="list-style-type: none">■ Specify the correct page border in the setup options.<ol style="list-style-type: none">a. Display the Document Schematic Generation Setup dialog box. (See Document Schematic Generation Setup on page 810.)b. In the Symbols tab, use the Browse button to specify the page border from Cadence standard libraries.<p style="text-align: center;">or</p>
Page size not sufficient to accommodate components	Specify a new page size using one of the methods listed above.
The nets in the generated schematic overlap with the page border.	<p>Reason: The drawing area is not computed properly.</p> <p>Solution: Use the <i>Page Border Information File</i> text box in the General tab of the Document Schematic Generation dialog box to specify the <code>cref.dat</code> file to be used.</p>

Table 21-1 Possible causes and resolutions for the failure of document schematic generation process, continued

Problem	Cause and Troubleshooting steps...
Incorrect symbols or symbols with packaging errors.	For generating document schematic, new symbols are not created. Symbols from the existing libraries are used. To generate document schematic, ensure that: <ol style="list-style-type: none">1. Basic pin-port mapping is correct2. Correct CTAP symbols are used. Comment bodies cannot be used as CTAP.3. Symbol linkages are correct. Every package used in the logical design, must have a corresponding symbol.
Setup option to stop the schematic generation process when an incorrect symbol or packaging error is encountered, is set.	Modify the setup options such that a warning is thrown for symbols with errors and the schematic generation process continues for the rest of the design. <ol style="list-style-type: none">1. Display the Document Schematic Generation Setup dialog box. (See Document Schematic Generation Setup on page 810.)2. In the General tab, deselect the <i>Report an error if proper symbol is not found for any instance in the design or if the instance has packaging errors</i> check box.
Split parts not coming together on same or contiguous page	Use the SCHEMATIC_GROUP property to group all symbols of a split part together. For more information on using SCHEMATIC_GROUP property, see Force placement on same sheet on page 564.

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Table 21-1 Possible causes and resolutions for the failure of document schematic generation process, continued

Problem	Cause and Troubleshooting steps...
Document Schematic generation stops with the following error message.	<p>The TAP symbol must have:</p> <ul style="list-style-type: none"> ■ Exactly two pins.
Document Schematic generation stopped as the Ctap symbol specified in the Setup is a comment body and is not supported. Choose a proper Ctap that conforms to the Ctap guidelines.	<ul style="list-style-type: none"> ■ The pin names of both the pins must have the \NAC property and the pin name of the first pin must also have the \NWC property. <p>For example, if the first pin is named B and the second pin is named S, enter the pin names as B \NAC \NWC and S \NWC.</p> <ul style="list-style-type: none"> ■ The first pin must be at the origin of the symbol and must not have the BN property. ■ The second pin must be on the x-axis and must have the BN property. ■ The second pin must have a positive x-coordinate and be on the grid.
In the document schematic, the properties attached to associated components appear rotated, thereby reducing readability.	<p>Note: Select the TAP component from the Cadence standard library if the TAP component in your library does not meet these requirements.</p> <p>Reason: This problem occurs when you add associated components as horizontal symbols. During document schematic generation process, these symbols are used as is from the spreadsheet-based design, and rotated appropriately to form rail.</p>
	<p>Solution: To ensure that the orientation of the property text in the generated document schematic is correct, all associated components, except series terminations, must be added as vertical symbols in the spreadsheet-design. This is because in the document schematic, all associated components, except series terminations, are added as vertical symbols in the rails. In case of series termination rails, horizontal symbols are used.</p>

Table 21-1 Possible causes and resolutions for the failure of document schematic generation process, continued

Problem	Cause and Troubleshooting steps...
Unable to find the component instance mentioned in the log files created during document schematic generation.	Reason: This problem occurs when due to non-availability of space, instead of displaying the signal name connected to the component, the signal named SIG_NAME, is added to a component instance. The instance name used in the error message, i63_0, refers to the instance i63, symbol version 0, in System Connectivity Manager.
An entry in the log file states: SIG_NAME added to the pin of the component i63_0.	<p>Solution: To locate the component in the generated document schematic, you can use one of the methods listed below.</p> <ul style="list-style-type: none"> ■ Search the design for the signal name listed in the error message. ■ Search the design using the Reference Designator value.
Due to some reason, if the schematic of the flattened block is updated such that it required a larger drawing area, it might lead to overlaps in the generated document schematic.	<p>Solution: To remove the overlaps, select the component that is the top most and the left most of the block and move it to a location with enough drawing space for the complete block. Regenerate the document schematic with Preserve option selected.</p>

Table 21-1 Possible causes and resolutions for the failure of document schematic generation process, continued

Problem	Cause and Troubleshooting steps...
<p>On using the <i>Embed Block</i> option, for some schematic blocks a lot of drawing space is left blank in the generated document schematic. This is a random behavior and is seen only for some specific blocks.</p>	<p>Reason: This error occurs when a schematic block has component properties that are placed at a distance from the components and are not made visible. Such placement of property increase the drawing area required to flatten the DEHDL schematic block.</p> <p>This is because for block flattening, the schematic block to be flatten is copied from the <code>sch_1</code> view and pasted in the <code>docsch_1</code> view such that the relative placements of components, wires, visible and invisible properties, notes, and images used in the flattened schematic block is not altered. Therefore, even if a property attached to a design component is invisible and is placed at a distance from the component, the total drawing area required will include the distance between the component and the property. Also the area used by the flattened block schematic is excluded from the available drawing area to ensure that there no overlaps.</p> <p>Solution: Check the location of the visible and invisible properties in the schematic block, ensure that the properties are placed in a manner to ensure optimum utilization of space, and regenerate document schematic.</p>

Exporting Schematics for a Design

This chapter contains the following sections:

- [Overview](#) on page 594
- [Export Schematic Flow](#) on page 596
- [Exporting Schematic Projects](#) on page 596
- [Troubleshooting](#) on page 599

Overview

The Generate Schematic process, discussed in [Chapter 21, “Generating Document Schematic for a Design.”](#) is used, mainly to generate a schematic used for documentation purposes. If you are looking at System Connectivity manager to quickly capture design logic, especially for high pin-count devices, but would rather continue with the traditional design process using schematics, then it is recommended that you use the export schematic process.

System Connectivity Manager allows you to export your spreadsheet-based design as a schematic. You can then open the exported schematic using Design Entry HDL and continue the design process. On exporting the design as a schematic, a new Design Entry HDL project is created with schematic pages, associated libraries, and other required files. You also need to understand that the export schematic is a one way process.



Changes made to the exported schematic cannot be back-annotated to the spreadsheet-based design.

The export schematic process leverages the block-level schematics created by the Generate Document Schematic process. If you have already generated block-level schematics those can be reused; else new block-level schematics are generated. You must keep the following in mind:

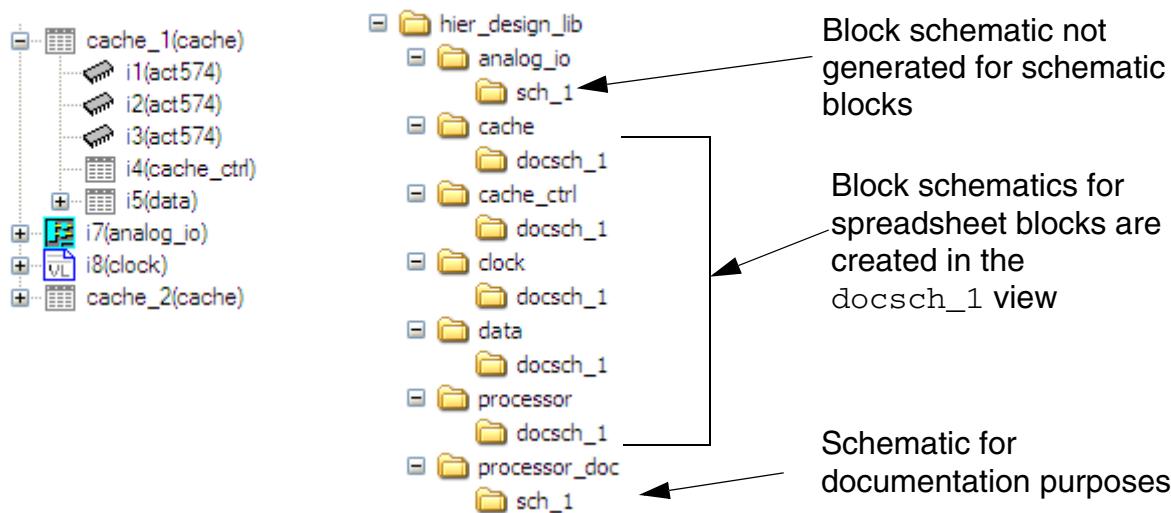
- Block-level schematics are created only for spreadsheet blocks and are stored in the `docsch_1` views of the cell.
- Block-level schematics for Design Entry HDL blocks are not generated. The `sch_1` views are used.
- The complete documentation schematic for the design is stored in the `<root design>_doc` cell under the `sch_1` view.

This is also illustrated in [Figure 22-1](#) on page 595.

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Exporting Schematics for a Design

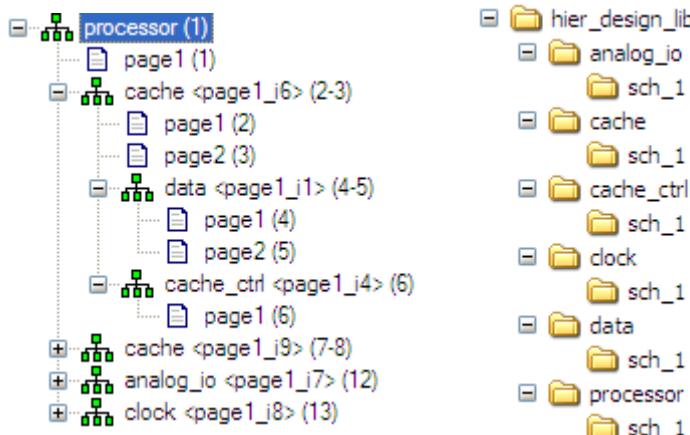
Figure 22-1 Block schematic directory structure



See the [Chapter 21, “Generating Document Schematic for a Design”](#) for details on generating block schematics.

The export schematic process assembles these schematic block views together, and creates a new schematic project. The schematics are stored in the `sch_1` view of the cells. This project contains all the libraries, views, and other associated files needed to work with this project. You can open this project using Design Entry HDL.

Figure 22-2 Hierarchy and library structure of the exported schematic project



Export Schematic Flow

The export schematic process is unidirectional. You cannot back annotate changes in the exported schematic to the spreadsheet-based design. It is recommended that you use Generate Schematics process to fine-tune the schematics using the *Preserve mode*, and when you are satisfied with the results, proceed with exporting the design as a schematic. See, [Chapter 21, “Generating Document Schematic in Preserve Mode.”](#) for more information.

The general flow is as follows:

1. Modify the design using System Connectivity Manager.
2. Use *Project — Generate Schematics* to create block-level schematics for the blocks.
3. Modify the placement in generated block-schematics using Design Entry HDL.
4. Regenerate schematics and use the *Preserve Mode* to retain the changes.
5. Export the design as a schematic to create a new Design Entry HDL project.
6. Capture design constraints in Design Entry HDL.

You now have a Design Entry HDL project that you can use in your schematic-based design flow.

Properties in the export schematic flow

In case of a hierarchical design in SCM, if you descend into a block and add a property, such properties are added to an OPF file in the exported project.

If you have added any non-synchronous properties in System Connectivity Manager and export the schematic, on opening the design in Design Entry HDL and opening Constraint Manager shows message to synchronize the design. Choose *Tools — Constraints — Synchronize* before opening Constraint Manager.

Exporting Schematic Projects

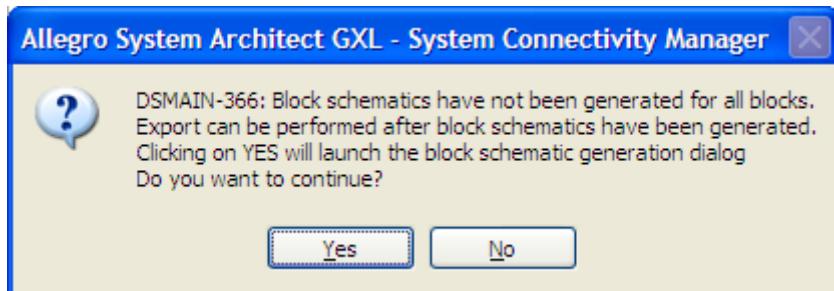
After you have captured your logic design using System Connectivity Manager, you can export it as a schematic project. To export a logical design as a schematic:

1. Choose *Project – Export – Schematics*.

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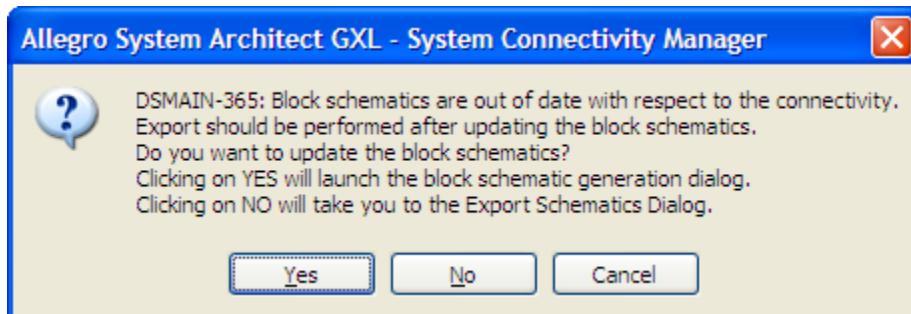
Exporting Schematics for a Design

- a. If you have not previously generated block schematics, a message displays. Click Yes to generate block schematics. If you clicked Yes, proceed to step b.

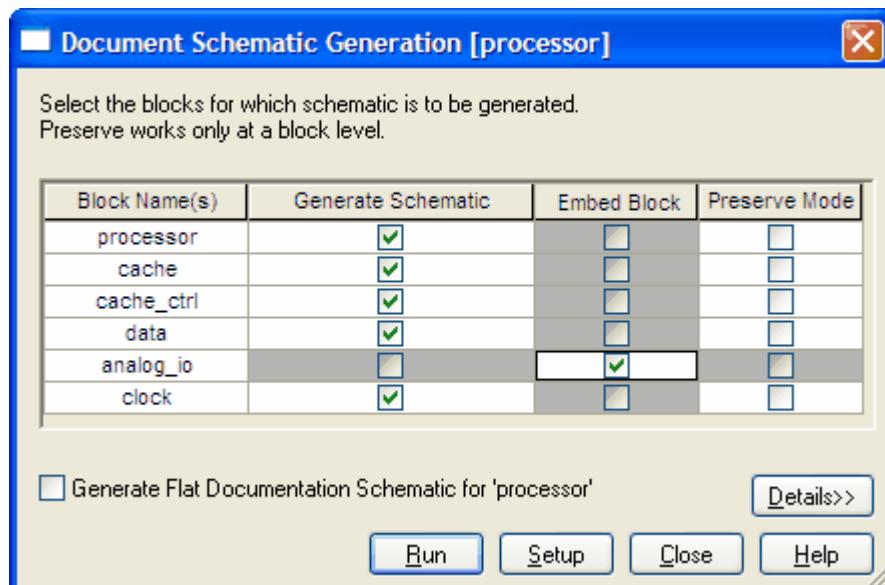


— OR —

If you have generated block schematics earlier, but they are out-of-date, a message displays. Click Yes to regenerate the block schematics or click No to use the existing block schematics. If you clicked No, proceed to step 2.



- b. The Documentation Schematic Generation dialog box appears.



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Exporting Schematics for a Design

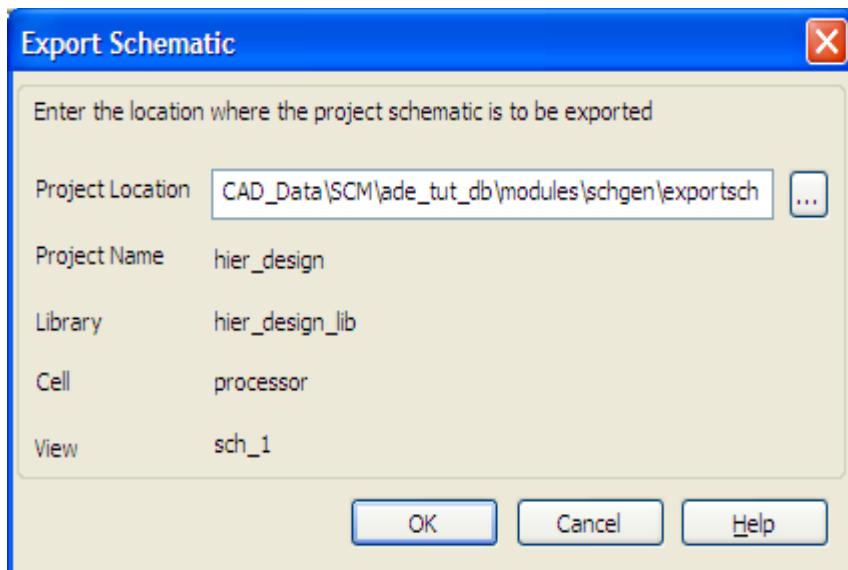
- c. Click *Run* to generate the block level schematics. For each block, the document schematic is created in the `docsch_1` view.

Click *Setup* to modify the schematic generation options. For details on the creating block level schematics see the previous chapter, [Generating Document Schematic for a Design](#) on page 555.

Note: If you are exporting a design that was created in a previous version of System Connectivity Manager, you must regenerate all the block schematics in the *Preserve Mode* before exporting the schematic.

- d. Click Close to dismiss this dialog box.

2. The Export Schematic dialog box appears.

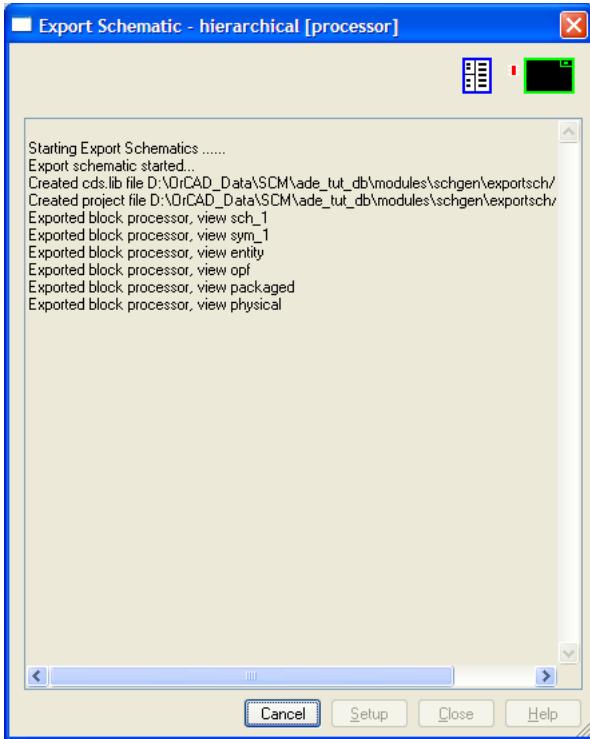


3. In the Project Location field, specify the directory to create the schematic project. By default the exported project is located in the `exportsch` directory located one level above the project folder.
4. The Project Name, Library, Cell, and View names are displayed for your reference.

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Exporting Schematics for a Design

5. Click *OK* to export the schematic. The Export Schematic dialog box displays the progress of the export process.



6. Click *Close* to dismiss the dialog box.

A new Design Entry HDL project is created.

A new option “Open Schematic” is available in the Export Schematics dialog box. Clicking this option launches DEHDL, and displays the schematic. This option is particularly useful if you want to verify the exported schematic quickly.

Troubleshooting

If the export schematic process fails for your design, you need to first check if the block schematics were created properly. For details on troubleshooting the block schematic generation, see [Possible causes and resolutions for the failure of document schematic generation process](#) on page 586.

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Exporting Schematics for a Design

The following table lists some issues and resolutions in the export schematic process.

Table 22-1 Possible causes and resolutions for the failure of export schematic process

Problem	Cause and Troubleshooting steps...
Problem in saving schematic	This could be due to insufficient permissions on the location where you are exporting the schematic project. Ensure that there is sufficient space and permissions on the export location.

Creating Parts from External Data Files

This chapter describes how you can create parts from files of different format that contain part information and add these parts in your design. The topics covered in this chapter are:

- [Creating Parts from FPGA Files and Adding them in the Design](#) on page 602
- [ECO of Standard FPGA Parts Created from FPGA Files](#) on page 607
- [Creating Parts from .CSV Files and Adding them in the Design](#) on page 612
- [Creating Parts from Text Files](#) on page 614
- [ECO of parts Created From Text File](#) on page 622
- [Creating Parts using Footprint Information](#) on page 624
- [ECO of Parts Created Using Footprint Data](#) on page 625
- [Creating Parts from DIE Text Files](#) on page 626
- [ECO of Parts Created Using DIE Text](#) on page 627

Creating Parts from FPGA Files and Adding them in the Design

System Connectivity Manager lets you use the place-and-route data created using tools from FPGA vendors Actel, Altera and Xilinx to create a part for an FPGA. You can then use the FPGA part in your design.

To create an FPGA part using the place-and-route data for the FPGA

1. From the *File* menu in System Connectivity Manager, choose *Import Part*.
The *Import and Export* page appears.
2. Select *Import FPGA* and click *Next*.
The *Select Source* page appears.
3. Choose the vendor for the place-and-route tool you used to create the place-and-route file for an FPGA. The following vendors are supported:
 - Actel
 - Altera

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Creating Parts from External Data Files

Xilinx

Do the following if you selected Actel as the vendor

- a. Select the Actel device family you used when creating the place-and-route file.
- b. Specify the name and path to the place-and-route file you created using the Actel place-and-route tool.
- c. Specify the name and path to the package file for the device family.

The default package file for the device family is displayed. You can specify a different package file.

Note: The package files for Actel device families are located at:

```
$CADENCE/share/library/actel/data/  
<device_family>.pkg
```

where \$CADENCE is the Cadence installation directory.

- d. Specify the name and path to the pin file to be used for the Actel device family.

The default pin file for the Actel device family is displayed. You can specify a different pin file.

Note: The default PGA pin files for Actel device families are located at:

```
$CADENCE/share/library/actel/data/  
actel.pga.pin
```

where \$CADENCE is the Cadence installation directory.

- a. Select the Altera place-and-route tool you used to create the place-and-route file.
- b. Specify the name and path to the place-and-route file you created using the Altera place-and-route tool.

Do the following if you selected Altera as the vendor

Do the following if you selected Xilinx as the vendor

- a. Specify the name and path to the pad file you created using the Xilinx place-and-route tool.

4. Click *Simulation Options* and specify the following:

- Specify the name and path to the Verilog HDL file that contains the functional description of the FPGA. This file will be used by the simulator.
- Specify the name and path to the SDF file that contains the delay information of the FPGA.

5. Click Next.

The *Select Destination* page appears.

6. You can now create a new schematic symbol for the FPGA or use an existing part as the schematic symbol for the FPGA.

Select	To
Generate Custom Component	<p>Create a new schematic symbol for the FPGA.</p> <p>Click <i>Default Properties</i> to display the <i>Default Properties</i> dialog box. Specify the default values for the following properties.</p> <ul style="list-style-type: none">■ DESCRIPTION■ FAMILY■ JEDEC_TYPE■ PART_NUMBER <p>To specify the value for a property, select a property from the <i>Name</i> drop-down list, then enter its value in the <i>Value</i> field.</p>

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Creating Parts from External Data Files

Select	To
Use standard component	<p>Use an existing part as the schematic symbol for the FPGA.</p> <p>Select the <i>Library</i> in which the part exists from the <i>Library</i> drop-down list, then select the part in the <i>Cell</i> drop-down list.</p> <p>Methodology</p> <p>System Connectivity Manager replicates the HDL views from the source component to the target component. In the target component, it creates the <code>pinlist.csv</code> file in the FPGA view.</p> <p>The <code>pinlist.csv</code> file contains a pin name to number mapping which is derived from the FPGA source file such as the pad, pin, or <code>.csv</code> file.</p> <p>Note: The <code>pinlist.csv</code> file contains only the pin information for the programmable pins. Standard programming pins and power pins are not included because their names are standard and do not change when programming the FPGA.</p> <p>There are some guidelines that must be followed:</p> <ul style="list-style-type: none">■ The primitive name is not changed when the source component is replicated. Therefore, it is important to ensure that the logical pin list of the destination component is always matching the source component. If the logical pin list is different and System Connectivity Manager finds the same primitive from two different places, the FPGA import will fail.■ The physical pins list of the target component should match the physical pin list of the FPGA view. This is required because System Connectivity Manager overlays the logical pins on the basis of the physical pin list in the FPGA view.■ In case of multiple primitives, all the primitives get copied and the <code>pinlist.csv</code> file is valid for all the primitives.

7. In the *Cell to be created* field, specify the name of the FPGA part you want to create.

By default, the name of the FPGA part will be the same as the name of the place-and-route or pad file you selected in [step 3](#).

8. In the *Destination Library* field, select the library in which you want the FPGA part to be created.
9. Do one of the following:

- Click *Next* if you have selected the *Generate Custom Component* option.

The *Preview of Import Data* page appears. Modify the pin information as required and click *Finish*.

For example, if a pin name is DXP~N, the pin name will be automatically changed to DXP_TILDA_N when you import the FPGA part. This translation is controlled through the `translate.cpm` file located at:

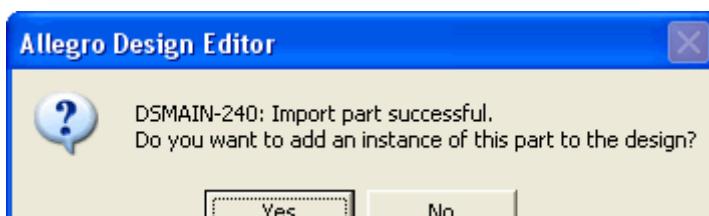
`<your_inst_dir>\share\cdssetup\LMAN\`

If you do not want to use the pin name DXP_TILDA_N, you can modify the pin name in the *Name* column of the *Preview of Import Data* page.

- Click *Finish* if you have selected the *Use standard component* option.

If there were errors in the FPGA import, the Errors & Warnings dialog box appears displaying the status of the FPGA import.

If the FPGA import is successful, the following message box appears:



10. Click *Yes*, if you want to add the FPGA part in your design.

Part Information Manager appears.

11. Click *Add* to add the FPGA part in your design.

Note: If you click *No*, you can later use Part Information Manager to add the FPGA part in your design.

ECO of Standard FPGA Parts Created from FPGA Files

System Connectivity Manager lets you use the place-and-route data created using tools from FPGA vendors Actel, Altera and Xilinx to create a part for an FPGA and then use the FPGA part in your design.

If you later modify the place-and-route data for the FPGA, you can use the *Import ECO-FPGA* option to ECO the FPGA part using the modified place-and-route data for the FPGA. When you ECO an FPGA part, all instances of the part in the design are replaced with the ECO'ed FPGA part.

Note: In System Connectivity Manager you can only ECO the standard FPGA parts (parts created using the *Use standard component* option). Use Part Developer to ECO the custom FPGA parts (parts created using the *Generate Custom Component* option).

To ECO an FPGA part

1. From the *File* menu in System Connectivity Manager, choose *Import Part*.

The *Import and Export* page appears.

2. Select *Import ECO - FPGA* and click *Next*.

The *Select Source for ECO* page appears.

3. Choose the vendor for the place-and-route tool you used to modify the place-and-route file for the FPGA for which you had created the part.

Do the following if you selected Actel as the vendor

- a. Select the Actel device family you used when modifying the place-and-route file.
- b. Specify the name and path to the place-and-route file you modified using the Actel place-and-route tool.
- c. Specify the name and path to the package file for the device family.

The default package file for the device family is displayed. You can specify a different package file.

- d. Specify the name and path to the pin file to be used for the Actel device family.

The default pin file for the Actel device family is displayed. You can specify a different pin file.

Do the following if you selected Altera as the vendor

- a. Select the Altera place-and-route tool you used to modify the place-and-route file.
- b. Specify the name and path to the place-and-route file you modified using the Altera place-and-route tool.

- a. Specify the name and path to the pad file you modified using the Xilinx place-and-route tool.

4. Click Next.

The *Select Destination for ECO* page appears.

5. In the *Select Component* group box, select an existing part you want to use to ECO the FPGA part.

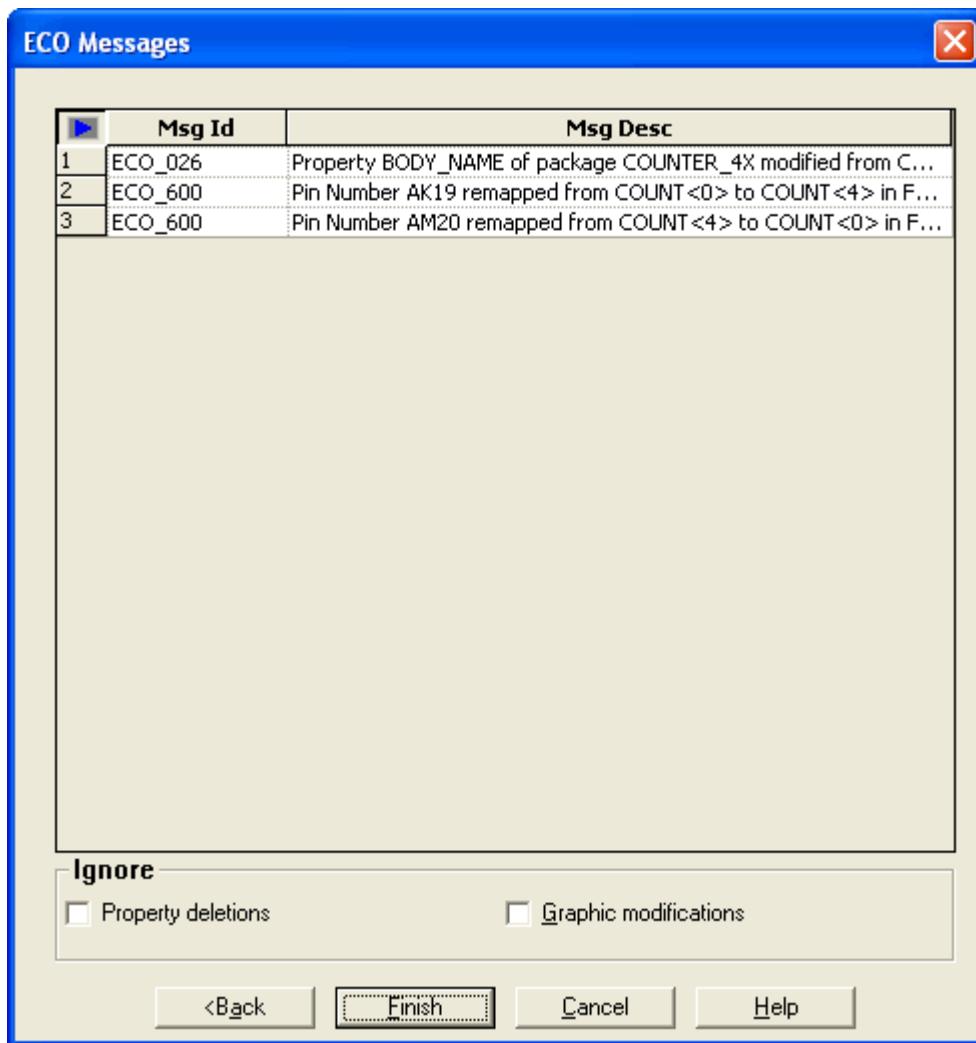
To do this, select the library in which the part exists from the *Library* drop-down list, then select the part in the *Cell* drop-down list.

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6. In the *Library* drop-down list in the *Specify Library and Cell Name* group box, select the library in which the FPGA part you want to ECO exists.
7. In the *Cell* drop-down list in the *Specify Library and Cell Name* group box, select the name of the FPGA part you want to ECO.
8. Click *Next*.

The ECO Messages page appears displaying the differences between the existing FPGA part and the FPGA file and part against which ECO is being done.

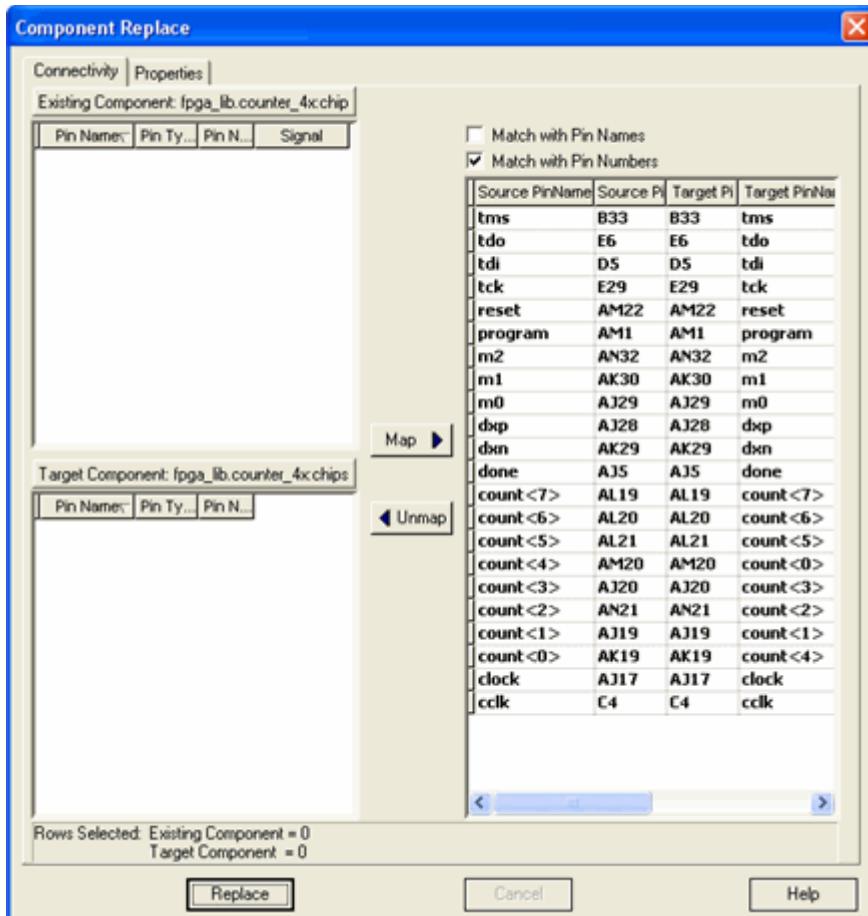


9. Click *Next*.

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The Component Replace dialog box appears.



The *Existing Component* list and the *Target Component* list display the connectivity differences that occurred because of the ECO.

10. Map the connectivity differences using the Component Replace dialog box.

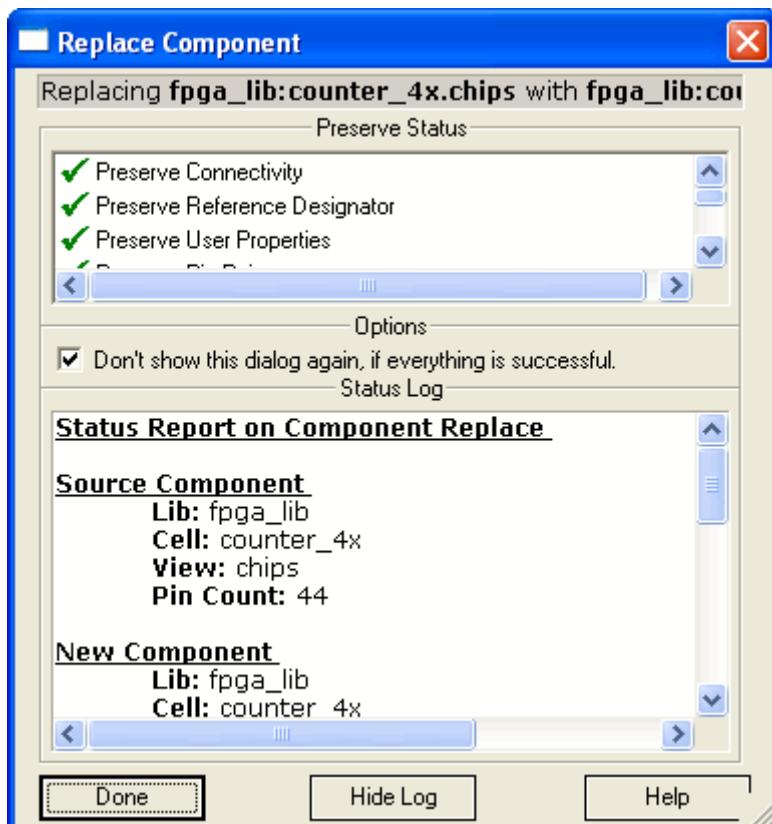
For more information on using the Component Replace dialog box, see [Using the Component Replace Dialog Box](#) on page 113.

11. Click *Replace*.

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The Replace Component dialog box appears displaying the details of the replace process.



12. Click *Done* to close the Replace Component dialog box.

The following message box appears.



13. Click *OK*.

Creating Parts from .CSV Files and Adding them in the Design

System Connectivity Manager can import part information stored in a comma separated value (.csv) file and create packages and symbols from it. You can then add the part in the design.

To create a part from a .csv file

1. From the *File* menu in System Connectivity Manager, choose *Import Part*.
The *Import and Export* page appears.
2. Select *Import Comma Separated Value (.csv) file* and click *Next*.
The *Select Source* page appears.
3. Browse and select the input CSV file.
The *Select Destination* page appears.
The name of the part to be created is seeded automatically. If required, change the part name.
4. Select the library in which the part is to be created and click *Next*.
The *Preview of Import Data* dialog box appears.
5. Click *Finish* to complete the part creation process.

You can now add the part in your design.

To add the part in your design

1. Do one of the following:
 - Choose *Design – Add Component*.
 - Click  on the toolbar.
Part Information Manager appears.
2. Click *Browse Libraries*.
3. Select the library in which you saved the part.

Note: If the part is not displayed in the *Cells* list, right-click in the *Library* list and choose

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Refresh Lib to display the imported block in the *Cells* list.

4. Select the part in the *Cells* list and click *Add*.

The part is added in the design.

Creating Parts from Text Files

While creating a design in System Connectivity Manager, you can import part information stored in a delimiter-separated text file and create packages and symbols from it. You can then add the part in the design.

Importing Text Data

To import part information stored in a text file, perform the steps listed below.

1. From the *File* menu, *Import Part*.

The *Import and Export* page appears.

2. Select the *Import Text File* option and click *Next*.

3. The *Select Source* page, specify the name and location of the text file containing part information and click *Next*.

4. In the *Select Destination* page, specify name of the cell to be created.

Note: The name of the part to be created is seeded automatically from the text file name. If required, you can change the name.

5. Select the library in which the cell is to be created and click *Next*.

6. In the *Select Rows* page, specify the rows in the text file that should be imported while creating part and click *Next*.

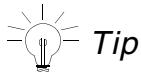
You can preview the contents of the text file to be imported in the Data Preview pane of the *Select Rows* page. To know more about the options in the Select Row page, see [Select Rows](#) on page 778.



If you want to seed in your format-specific preferences, you can do so by specifying the name and the location of the profile file in the *Select any profile to load* text box. If you select a profile, you can directly jump to [step 16](#). To know more about profiles, see [Profile Use Model](#) on page 619.

7. In the *Select Delimiter(s)* page, select the appropriate check box, to specify the delimiter that should be used to parse the import data. If multiple instances of the delimiter are used to separate columns, select the *Treat consecutive delimiters as one* check box.

Based on your selection, the data is parsed and displayed in rows and columns in the *Data Preview* area.



Tip

If your text file has more than one kind of delimiter, it is recommended that you select the *Treat consecutive delimiters as one* check box.

8. Click *Next*.

The *Select Columns* page appears.

9. Depending on the contents of the first row, you may want to select the *Set first row as header* check box.
10. If required, select the *Set pin number as pin name* check box.

Note: Since the pin name column is the only column required for the import process, selecting this option ensures that the import process is successful if the text file contains only the pin number column.

11. In the Data Preview area, choose the columns for import and click *Next*.
12. If you want a symbol for the part to be created, in the *Select Views* page, select the *Generate Symbol* check box.
13. Select the *Add Footprint* check box and choose a footprint from the list of footprints displayed from PSMPATH.

Note: The variable, PSMPATH, is set automatically when you install APD.

14. If you want to save your format-specific preferences, click the *Save Profile As* button, and specify the name of the file in which you want your settings to be saved.

Note: Your preferences are saved in a .prf file.

15. To move to the final step in the import process, click *Next*.

The *Preview of Derived Data* page appears. You can preview the data in *Logical Pins* and *Global Pins* grids.

16. Click *Finish* to complete the import process.

The message box appears stating that the part has been successfully imported and asking if you want an instance of the part added to the design.

Conversion Details

- The following headers are read and translated during text import:
 - pin_name

- pin_number
 - pin_type
 - pin_location
 - pin_position
 - symbol
- The minimum headers required are as follows:
- pin_name for flat or single-section parts
 - pin_name, pin_number, and symbol for multi-section parts

The package and symbol information is determined in the following way:

- By default, the package name is the same as the cell name to be created. It can be changed on the *Select Destination* page during text import.
- Entries under the pin_name column are used as pin names.
- Entries under the pin_number column are used as pin numbers.
- Entries under the pin_type column are used as pin types. Various pin types are automatically converted to supported pin types by using the definitions provided in the `propfile.prop` file. For example, if the pin type IO is specified in the text file, it is converted to BIDIR.
- Entries under the pin_location column are used to determine the location of pins (left, right, top, and bottom) on the symbol.
- Entries under the pin_position column are used to determine the position of pins with respect to the origin of the symbol. A pin_position column value appears as the value of the *Position* column in the Symbol Pins panel.
- If the symbol is not present as a column in the text file, the symbol is created only when the *Generate Symbol* option is selected on the Select Views page.
- If the symbol column value is not specified for a POWER, GROUND, or NC pin, the pin is moved to the global section. Otherwise, it is moved to the logical section.

Note: By default, power and NC pins in a DIE text file are imported as global pins and are only visible in the Assign Power dialog box in System Connectivity Manager. To ensure that all the pins in the DIE text file are available in the Component Connectivity Details pane, set the value of the `Import_Text_PwrGndNCPinsInGlobalSection` directive in the PDV section of the `<project>.cpm` file to FALSE.

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- If duplicate pins exist in the text file, the Duplicate Pin Resolver is used as in CSV import to resolve the problem.
- If a pin exists on multiple symbols with different pin types, one of the pin types is used and the rest is ignored. You should correct the text data before the import process.
- Pin names with invalid characters in them are automatically converted to valid pin names according to CSV rules by using the entries provided in the `translate.cpm` file, which is located at `<your_inst_dir>\share\cdssetup\lman`. For example, the character ! is translated to _EXCL_ because it is not a supported character in the Cadence flow.

Import Text File Example

Consider the file `HDLC_xc4vlx25_sf363.pad` that has entries as shown in the figure given below.

```
Mon Jun 06 20:20:15 2005
# NOTE: This file is designed to be imported into a spreadsheet program
# such as Microsoft Excel for viewing, printing and sorting. The |
# character is used as the data field separator. This file is also des
# to support parsing.
#
INPUT FILE:      HDLC_map.ncd
OUTPUT FILE:     HDLC.pad
PART TYPE:       xc4vlx25
SPEED GRADE:    -12
PACKAGE:         sf363
```

Pinout by Pin Number:

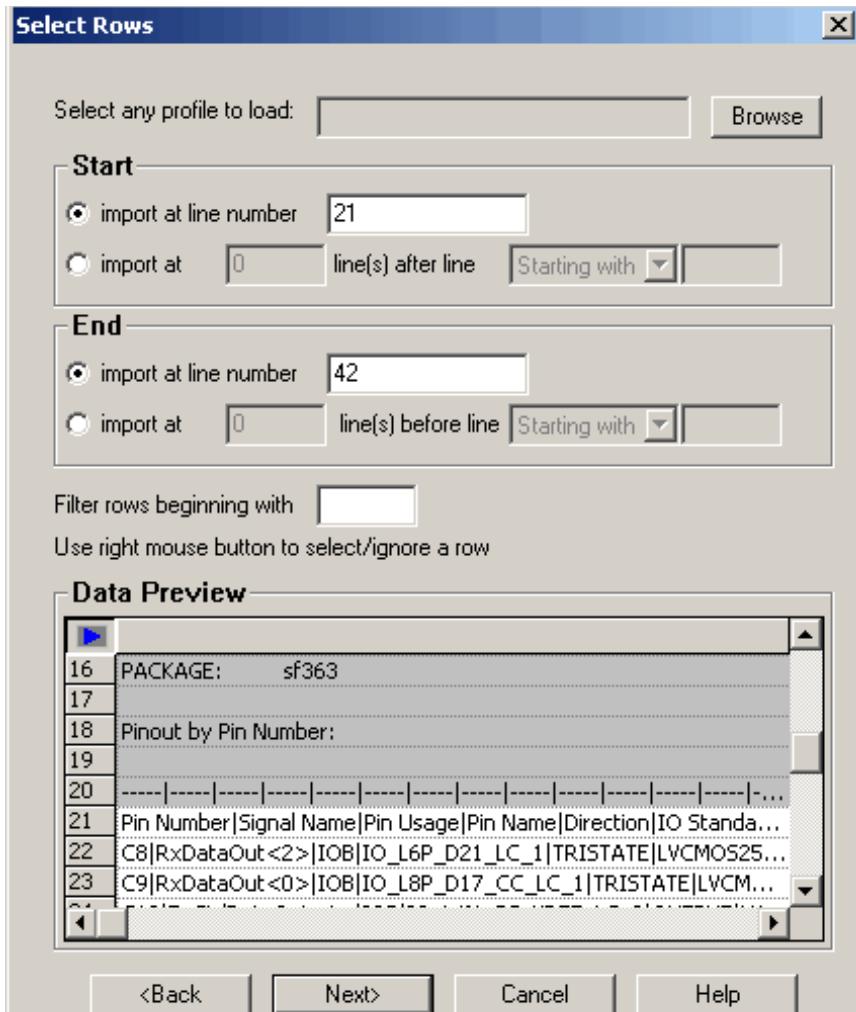
Pin Number	Signal Name	Pin Usage	Pin Name	Direction	IO Standard	IO Bank
C8	RxDataOut<2>	IOB	IO_L6P_D21_LC_1	TRISTATE	LVCMOS25	1 12 SLOW NONE**
C9	RxDataOut<0>	IOB	IO_L8P_D17_CC_LC_1	TRISTATE	LVCMOS25	1 12 SLOW NON
C10	TxCtrl1DataOut<1>	IOB	IO_L4N_GC_VREF_LC_3	OUTPUT	LVCMOS25	3 12 SLOW
C11	TxCtrl1DataIn<1>	IOB	IO_L3P_GC_LC_3	INPUT	LVCMOS25	3 NONE NO
C12	RxDataOut<1>	IOB	IO_L7N_D18_LC_1	TRISTATE	LVCMOS25	1 12 SLOW NONE*
D8	RxDataOut<3>	IOB	IO_L6N_D20_LC_1	TRISTATE	LVCMOS25	1 12 SLOW NONE**
D9	RxDataStrobe	IOB	IO_L8N_D16_CC_LC_1	OUTPUT	LVCMOS25	1 12 SLOW NONE*
D12	RxDataOut<2>	IOB	IO_L7P_D19_LC_1	TRISTATE	LVCMOS25	1 12 SLOW NONE*
N17	RxAddressIn<1>	IOB	IO_L29N_5	INPUT	LVCMOS25	5 NONE NO NONE
N18	RxAddressIn<0>	IOB	IO_L30P_5	INPUT	LVCMOS25	5 NONE NO NONE
P1	TxDatasheetIn	IOB	IO_L32N_6	OUTPUT	LVCMOS25	6 12 SLOW NONE** N

When you import this text file, a part with the same name as the text file is created unless you specify a different name during the import process. Note that the pin information in the text

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file is preceded by 20 lines of text, which needs to be ignored in the import process. To ensure this, specify the start import line number as 21.

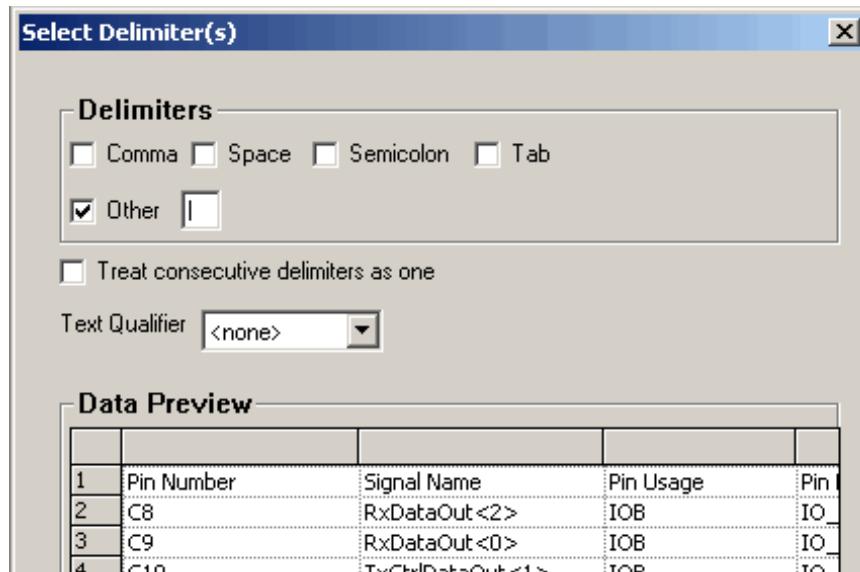


If you set the first row of the text file as the header, the text import wizard recognizes PIN_NUMBER, PIN_NAME, PIN_TYPE, PIN_LOCATION, and PIN_POSITION columns and translates them to appropriate properties. However, the last two are used only if you generate the symbol for the part using the text import wizard.

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The delimiter used in the file is | . When you specify the delimiter, the text import wizard parses the data and displays the data in a tabular format for preview.



If your text file has consecutive delimiters, selecting the *Treat consecutive delimiters as one* option treats multiple occurrences of the delimiter as one occurrence.

The *Text Qualifier* option enables you to import values that contain the characters you have specified as delimiters. Take the example of INPUT_LOAD and OUTPUT_LOAD values, such as "(1.0,1.0)" and "(0.01;0.01)". To import these values, you need to specify comma and semicolon, respectively, as a text qualifier. Currently, Part Developer supports only comma and double quotation mark as text qualifiers.

Profile Use Model

Profiles enable you to save your preferred settings for filtering the import data so that the same settings can be applied in later sessions of import by simply loading the profile files.

The following table lists the settings that are saved in a profile file and the corresponding directives:

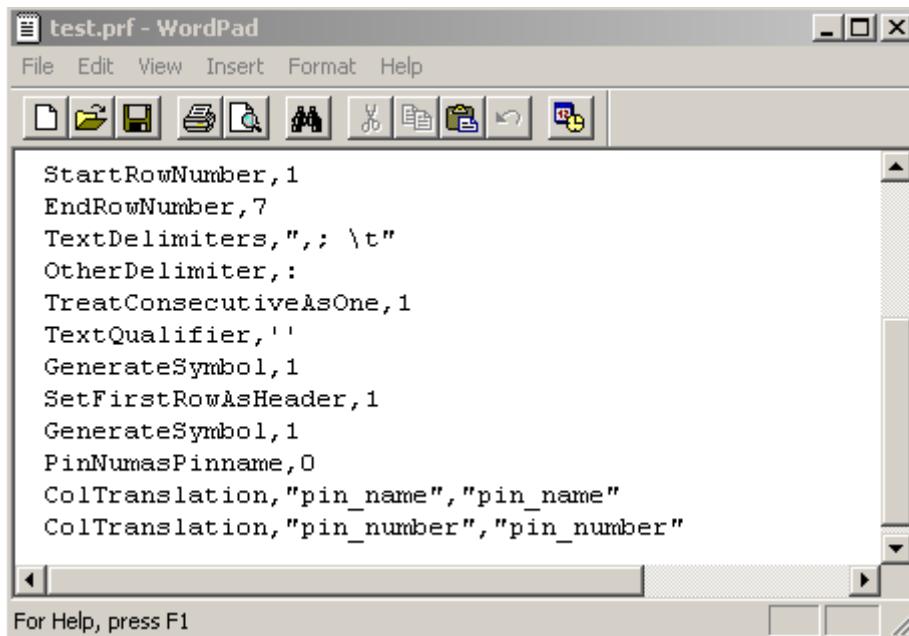
Settings	Directives
Range of data to be imported as specified using the options in Start and End areas	StartRowNumber EndRowNumber

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Delimiters to be used to parse data	TextDelimiters
	OtherDelimiter
Whether or not consecutive delimiters are to be treated as one	TreatConsecutiveAsOne
Text qualifier if any	TextQualifier
Whether or not a symbol is to be generated	GenerateSymbol
Whether or not the first row is to be set as the header	SetFirstRowAsHeader
Whether or not pin numbers are to be set as pin names	PinNumasPinname

The following example shows how various directives are specified in a profile file:



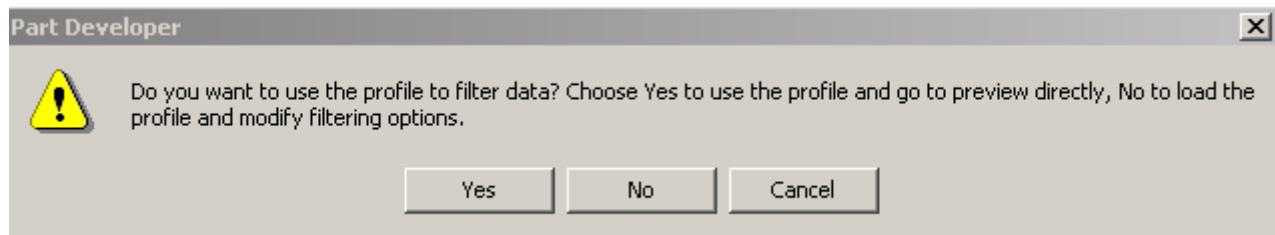
```
StartRowNumber,1
EndRowNumber,7
TextDelimiters,",; \t"
OtherDelimiter,:
TreatConsecutiveAsOne,1
TextQualifier,''
GenerateSymbol,1
SetFirstRowAsHeader,1
GenerateSymbol,1
PinNumasPinname,0
ColTranslation,"pin_name","pin_name"
ColTranslation,"pin_number","pin_number"
```

Note that the selection of rows and columns made in the Data Preview area by using the shortcut menu and the footprint specified for the part are not saved in the profile file.

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Therefore, if you want to add a footprint, you should choose the *No* option to load the profile file and modify the filtering options when the following message is displayed.



In this way, the profile settings will be loaded and the text import wizard will not jump to the Preview of Derived Data pane. You can then step through all the text import wizard panes and modify any profile settings if necessary.

ECO of parts Created From Text File

After you have instantiated a part created from a text file in your design, if required you can modify the part by importing the modified part data available in text files. To do this, follow the steps listed below.

To import text file ECO

1. Choose *File – Import and Export*.

The *Import and Export* page appears.

2. Select the *Import ECO –Text File* option and click *Next*.

3. In the *Select Source* page, browse and select the input text file.

The *Select Destination for ECO* page appears.

4. Select the library and part to be modified and click *Next*.

The *Select Rows* page appears.

Note that the text file data is displayed in the *Data Preview* area.

5. If you want to use your format-specific preferences, select a profile, specify the rows to be imported, and click *Next*.

The *Select Delimiter(s)* page appears.

6. Choose the delimiter that should be used to parse the import data and if required, select the *Treat consecutive delimiters as one* check box. Based on your selection, the data is parsed and displayed in rows and columns in the *Data Preview* area.

7. From the *Text Qualifier* drop-down list, select any character that you do not want Part Developer to treat as a delimiter and click *Next*.

The *Select Columns* page appears.

8. Select the *Set first row as header* check box if required.

9. Select the *Set pin number as pin name* check box.

10. In the *Data Preview* area, choose the columns for import and click *Next*.

The *Select Views* page appears.

11. Select the *Generate Symbol* check box.

12. Select the *Add Footprint* check box and specify a footprint.

13. Click the *Save Profile As* button, specify the name of the file in which you want Part Developer to save your format-specific preferences, and click *Next*.

The *Preview of Derived Data* page appears.

You can preview the data in *Logical Pins* and *Global Pins* grids.

14. Click *Next* to continue.

The ECO Messages page appears.

You can view the complete list of ECO modifications that are going to be done on the input cell. By default, Part Developer deletes the properties that are present in the cell but not in the input file and retains any symbol graphic modifications that have been done during ECO. You can turn off these default behaviors by using the *Property deletions* option and the *Graphic modifications* option in the Ignore section.

15. Click *Finish* to complete the ECO import process.

The Component Replace dialog box appears.

The *Existing Component* list and the *Target Component* list display the connectivity differences that occurred because of the ECO.

16. Use the Map and Unmap buttons to map the connectivity differences using the Component Replace dialog box.

For more information on using the Component Replace dialog box, see [Using the Component Replace Dialog Box](#) on page 113.

17. Click *Replace*.

The Replace Component dialog box appears displaying the details of the replace process.

18. Click *Done* to close the Replace Component dialog box.

The part is updated with the changes.

Creating Parts using Footprint Information

You can create new parts for your design using the footprints information.

Conversion Details

- The pin names are derived from the physical pin numbers of the imported footprint.
- The default pin type is BIDIR. However, it can be configured using the cpm directive Import_AllegroFtprint_DefaultPinType 'BIDIR'.
- By default, the cell name and the part name are the same as the name of the footprint being imported.

Procedure

The steps to be followed for created a part using footprint information are listed below:

1. Choose *File – Import Part*.

The *Import Wizard* appears.

2. Select *Import Allegro Footprint* and click *Next*.

The *Select Footprint* page displays all of the footprints in PSMPATH.

Note: To set the PSMPATH path, <your_work_area>/reference pcb/symbols

3. Select the footprint you want to import and click *Next*.

The *Select Destination* page appears.

4. Enter the name of the cell to be created and the library in which it should be created and click *Next*.

The *Preview of Import Data* page appears. You can preview the data in *Logical Pins* and *Global Pins* grids.

5. Click *Finish* to complete the import process.

The Cell Editor appears with the part information.

ECO of Parts Created Using Footprint Data

The *Import ECO - Allegro Footprint* option enables you to modify the parts created from Allegro footprints.

The steps are as follows:

1. Choose *File – Import Part*.

The *Import and Export* page appears.

2. Select *Import ECO – Allegro Footprint* and click *Next*.

The *Select Footprint* page displays all of the footprints in `PSMPATH`.

3. Select the footprint you want to import and click *Next*.

The *Select Destination* page appears.

4. Enter the name of the cell to be created and the library in which it should be created and click *Next*.

The *Preview of Import Data* page appears. You can preview the data in *Logical Pins* and *Global Pins* grids.

5. Click *Next* to continue.

The ECO Messages page appears. You can view the complete list of ECO modifications that are going to be done on the input cell. By default, Part Developer deletes the properties that are present in the cell but not in the input file and retains any symbol graphic modifications that have been done during ECO. You can turn off these default behaviors by using the *Property deletions* option and the *Graphic modifications* option in the Ignore section.

6. Click *Finish* to complete the import process.

The Component Replace dialog box appears.

The *Existing Component* list and the *Target Component* list display the connectivity differences that occurred because of the ECO.

7. Use the Map and Unmap buttons to map the connectivity differences using the Component Replace dialog box.

For more information on using the Component Replace dialog box, see [Using the Component Replace Dialog Box](#) on page 113.

8. Click *Replace*.

The Replace Component dialog box appears displaying the details of the replace process.

9. Click *Done* to close the Replace Component dialog box.

The part is updated with the changes.

Creating Parts from DIE Text Files

The *Import DIE Text* option enables you to import part information from a die file to create a part. The die file format is the standard format generated by Virtuoso or APD. Die files support only scalar and vector pins. They do not support sizeable pins.

Conversion Details

- The following headers are read from the die file:
 - Pin Number
 - Pin Use
 - Pin Name
 - Swap Code
- As Part Developer supports the entire APD-supported character set, no conversion is required for valid characters. However, if the die file being imported contains any invalid character in pin names, the pin names are translated to valid names.
- The character * is treated as the low-assertion character.

Steps

The steps are as follows:

1. Choose *File – Import Part*.
The *Import Wizard* appears.
2. Select *Import DIE Text* and click *Next*.
The *Select Source* page appears.
3. Browse to locate the die file and click *Next*.
The *Select Destination* page appears.

The name of the part to be created is seeded automatically from the die file name. If required, change the part name.

4. Enter the cell name, select the destination library, and click *Next*.

The Preview of Derived Data page appears.

5. Click *Finish* to complete the part creation process.

Note: By default, power pins in a DIE text file are imported as global pins and are only visible in the Assign Power dialog box in System Connectivity Manager. To ensure that all the pins in the DIE text file are available in the Component Connectivity Details pane, set the value of the `Import_Text_PwrGndNCPinsInGlobalSection` directive in the PDV section of the `<project>.cpm` file to FALSE.

ECO of Parts Created Using DIE Text

The *Import ECO - DIE Text* option enables you to modify parts created from die files.

The steps for importing DIE Text ECO are as follows:

1. Choose *File – Import Part*.

The *Import Wizard* appears.

2. Select *Import ECO - DIE Text* and click *Next*.

The *Select Source* page appears.

3. Browse to locate the die file and click *Next*.

The *Select Destination for ECO* page appears.

4. Enter the name of the part to be modified, select the destination library, and click *Next*.

The Preview of Import Data page appears.

5. Click *Next*.

If there are duplicate pins in the die file, Duplicate Pin Resolver Dialog appears. You need to resolve the duplicate pins.

The ECO Messages page appears. You can view the complete list of ECO modifications that are going to be done on the input cell. By default, Part Developer deletes the properties that are present in the cell but not in the input file and retains any symbol graphic modifications that have been done during ECO. You can turn off these default behaviors by using the *Property deletions* option and the *Graphic modifications* option in the Ignore section.

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6. Click *Finish* to complete the import process.

The Component Replace dialog box appears.

The *Existing Component* list and the *Target Component* list display the connectivity differences that occurred because of the ECO.

7. Use the Map and Unmap buttons to map the connectivity differences using the Component Replace dialog box.

For more information on using the Component Replace dialog box, see [Using the Component Replace Dialog Box](#) on page 113.

8. Click *Replace*.

The Replace Component dialog box appears displaying the details of the replace process.

9. Click *Done* to close the Replace Component dialog box.

The part is updated with the changes.

Archiving Projects

Any design project that you create can use two types of libraries—local and reference. Local libraries are stored in the project directory. Reference libraries are referenced from a central location. The project directory contains the `cds.lib` file, that includes links to the local and reference libraries used in the design. If you need to send a design to another person residing in a different geographical location, you will have to send the design along with all the libraries that it references. Each reference library contains hundreds of parts but your design may be using only a few parts. Archiving the project allows you to create a standalone project that includes only the parts used in the project from the reference libraries. For example, if your project uses only the `ls00` part in the `lsttl` reference library, the Archiver utility will copy only `ls00` to the project archive and not the entire `lsttl` reference library.

Another need for archiving arises because the reference libraries are updated from time to time. This may cause situations where your project references parts that have changed and, thereby, impact the functionality of the design. Archiving the project ensures that the design always uses the correct set of reference libraries.

The Archiver utility allows you to archive a project and all the parts that it uses without archiving entire reference libraries. Archiver identifies every physical part used in the project and then creates a local library containing only those parts. Archiving only the parts used in the project significantly reduces the amount of data that is to be archived, and considerably simplifies the archiving and restoration processes. An archived project can be used independent of reference libraries and other reference data. You can use this feature to store the project on a tape and use it later.

Archiving a Project

To archive a project

1. Do one of the following:
 - Choose *Project – Archive Project*.
 - Click *Archive a Project* in the System Connectivity Manager start page.

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Archiving Projects

The System Connectivity Manager start page is displayed when you start System Connectivity Manager. If a design is already open in System Connectivity Manager, click the tab for the System Connectivity Manager start page, or choose *Help – Display Start Page* to display the start page.

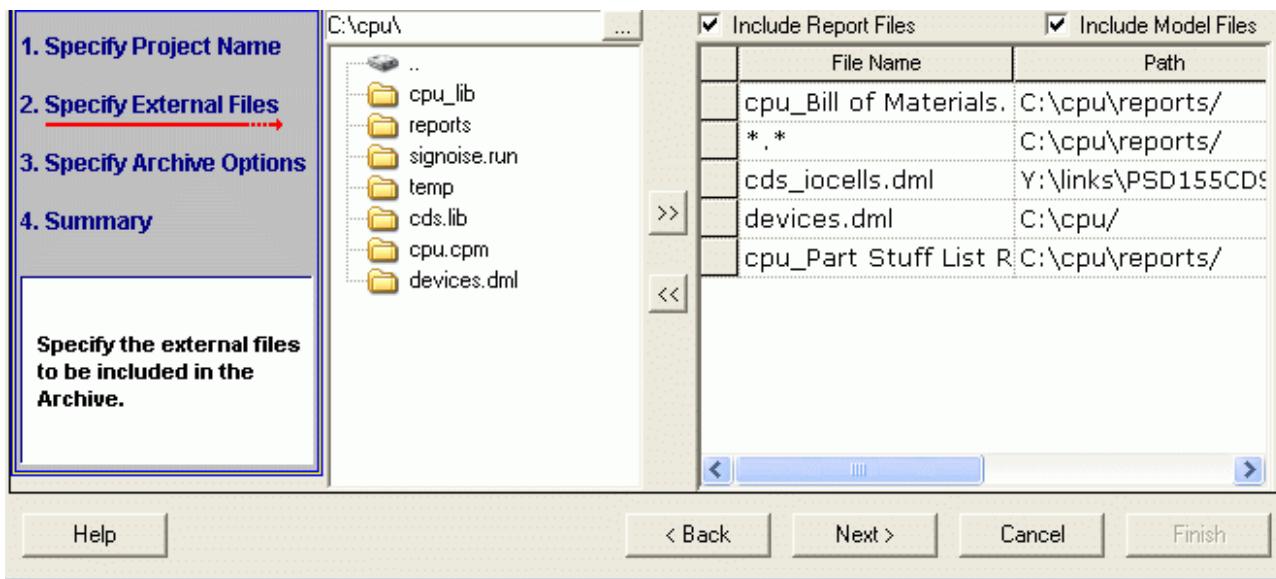
- ❑ Run the following command in the Windows, Unix or Linux command prompt:
dsarchiver

The Archiver: Specify Project Name window appears.

Note: If the project is already open in System Connectivity Manager and you choose *Project – Archive Project* or click *Archive a Project* in the System Connectivity Manager start page, the Archiver: Specify External Files window appears.

2. Enter the name and path to the project (.cpm) file for the project you want to archive, or click the browse button to select the file.
3. Click *Next*.

The Archiver: Specify External Files window appears.



Note: By default, the following files and directories are included in the archive. You can use the Archiver: Specify External Files window to include any other files and directories in the archive.

- ❑ <projectname>.cpm file
- ❑ cds.lib file

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Archiving Projects

- archiver.log file
- directories for working libraries for your project

Note: Only the components and blocks in the working libraries for your project that are used in the design are archived. The components and blocks in the working libraries that are not used in the design will not be archived.

- Components from the reference libraries used in the design and the page border, TAP, OFFPAGE, INPORT, OUTPORT and IOPORT symbols you specified in the Document Schematic Generation Setup tab of the Setup dialog box.

Note: Only the components in a reference library that are used in the design are archived.

4. Select the *Include Report Files* check box if you want to include all the report files in location for storing reports that you specified in the Report Generation page of the Setup dialog box.

Note: By default, reports are stored in the `reports` folder in the project directory.

5. Select the *Include Model Files* check box if you want to include all the signal integrity device model library (`.DML`) and device model library index (`.NDX`) files setup for your project.

For more information on setting up signal integrity (SI) model libraries for your project, see Setting Up SI Model Libraries on page 320.

6. To include any other file or directory in the archive, select the file or directory in the left pane and click . The file or directory is added in the right pane.

To select a file or directory that is outside the project directory, click the browse button in the left pane to select the directory in which the directory or file you want to include exists. The file or directory is displayed in the left pane. Select the file or directory in the left pane and click  to include it in the archive.

When you include a directory, the *File Name* field in the right pane displays `*.*`, indicating that all the files in the directory and all the files in the subdirectories under the directory will be archived. You can include only specific files in the directory and all the subdirectories under the directory by modifying the text in the *File Name* field. For example, if you want to include only the `.txt` files existing in a directory and all the subdirectories under the directory, enter `*.txt` in the *File Name* field.

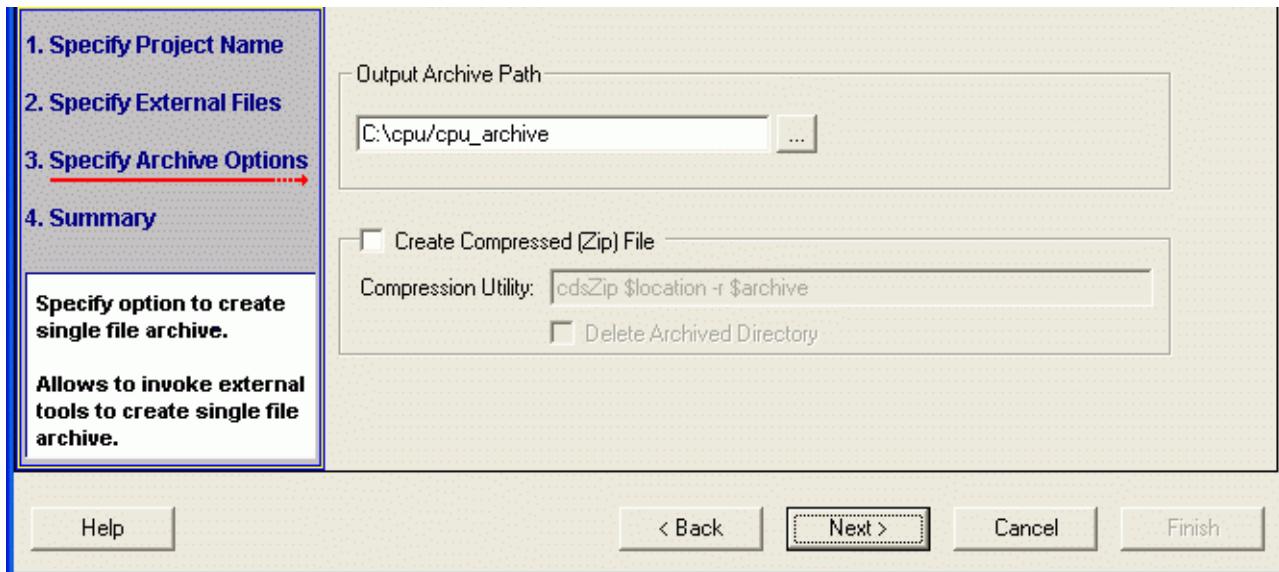
7. To exclude a file or directory from the archive, select the file or directory in the right pane and click . The file or directory is removed from the right pane.

8. Click *Next*.

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The Archiver: Specify Archive Options window appears.



9. In the *Output Archive Path* field, enter the path to the directory where you want the archive to be created, or click the browse button to select the directory.

By default, the archive is created in a directory named *<projectname>_archive* in the project directory. For example, if you are archiving a project named *cpu.cpm* located at *c:\cpu*, by default, the archive will be created at *c:\cpu\cpu_archive*.

10. Select the *Create Compressed (Zip) File* check box if you want to create a compressed archive of your project.

- a. By default, the *cdsZip* compression utility located in the *\tools\bin* folder of your Cadence installation directory is used to create the compressed archive.

The compressed file is named by adding *_compress* as a suffix to the archive design folder specified in the *Output Archive Path* text box.

For example, if you use the default values, the *cdsZip* compression utility creates a compressed archive file named *<projectname>_archive_compress.zip* in the project directory. But if you change the location of the output archive directory in the *Output Archive Path* field to a different directory, say *D:/work/memory_bank*, then the name of the compressed file created by the *cdszip* compression utility in the *work* directory will be *memory_bank_compress.zip*.

Note: For information on extracting the compressed archive, see [Extracting a Compressed Archive](#) on page 635.

To use any other compression utility to create the compressed archive, enter the command for the utility in the *Compression Utility* field. You can use the following variables in the *Compression Utility* field:

- \$location variable to pass the path to the archive you specified in the *Output Archive Path* field to the compression utility.
- \$archive variable to pass the name of the compressed archive file to the compression utility.

The compressed archive file will be named by adding the suffix _compress to the value of the variable specified in the *Output Archive Path* field. Depending on the compression utility used, the compressed archive file may or may not have a file extension.

For example, you can use the tar command using the following syntax

```
tar -cvf $archive $location
```

to create a <projectname>_archive_compress file.

Note: If you use any other compression utility to create the compressed archive, ensure that the utility is installed on your machine and that the executable for the compression utility is in the system path.

- b.** Select the *Delete Archived Directory* check box if you want the archive directory to be deleted after the compressed archive is created.

11. Click *Next*.

The Archiver: Summary window appears.

Review the options you selected for creating the archive.

12. Click *Finish*.

The progress of the archive process is displayed in the window. Check for any errors in the archiving process and click *Done*.

The archive is created in the location you specified. For information on the directory structure of the archived project, see [Directory Structure of Archived Project](#).

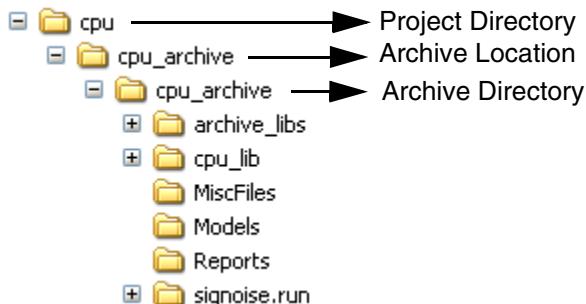
Directory Structure of Archived Project

The archived project has the following directory structure.

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Archiving Projects

Figure 24-1 Sample Directory Structure of Archived Project



The contents of the folders in the archive directory are described in the following table.

Folder	Contents of Folder
cpu_archive (archive directory)	<p>Contains all the files and folders for the archived project, and the following files and directories:</p> <ul style="list-style-type: none">■ <projectname>.cpm file■ cds.lib file■ archiver.log file■ directories for working libraries for your project <p>Note: Only the components and blocks in the working libraries for your project that are used in the design are archived. The components and blocks in the working libraries that are not used in the design will not be archived.</p> <p>In Figure 24-1, cpu_archive is the name of the archive directory you specified in the Archiver: Specify Archive Options window of the Archiver utility and cpu_lib is the working library for the project.</p>
archive_libs	<p>Contains the components from reference libraries used in the design and the page border, TAP, OFFPAGE, INPORT, OUTPORT and IOPORT symbols you specified in the <u>Document Schematic Generation Setup</u> tab of the <u>Setup</u> dialog box.</p> <p>Note: Only the components in a reference library that are used in the design are archived in this folder.</p>

Folder	Contents of Folder
MiscFiles	Contains the directories and files you selected in the Archiver: Specify External Files window of the Archiver utility. The MiscFiles folder also contains the files you added in the <i>Misc. Files</i> folder in the File Viewer. For more information on using the File Viewer, see Using the File Viewer on page 230.
Models	Contains the signal integrity device model library (.DML) and device model library index (.NDX) files setup for your project.
Reports	Contains the report files in location for storing reports that you specified in the Report Generation tab of the Setup dialog box.

Extracting a Compressed Archive

You can use the `cdsUnzip` utility located in the `\tools\bin` folder of your Cadence installation directory to extract the compressed archive of a project.

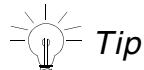
To extract a compressed archive

- Run the following command in the Windows, UNIX or LINUX command prompt:

```
cdsUnzip <archive_name>.zip
```

For example, to extract a compressed archive named `atm_archive.zip`, use the following command:

```
cdsUnzip atm_archive.zip
```



For more information on using the `cdsUnzip` utility, run the following command in the Windows, UNIX or LINUX command prompt:

```
cdsUnzip
```

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Archiving Projects

Customizing System Connectivity Manager

This chapter contain the following sections that help you in customizing System Connectivity Manager.

- [Customizing Menus in System Connectivity Manager](#) on page 638
- [Customizing Toolbars in System Connectivity Manager](#) on page 649
- [Customizing the Spreadsheet Editor](#) on page 652
- [Customizing System Connectivity Manager Tools](#) on page 654

Customizing Menus in System Connectivity Manager

You can customize the menus in System Connectivity Manager by:

- Adding new menu commands to a menu or submenu.
- Adding a new submenu to a menu and then adding menu commands to the submenu.
- Adding separators in a menu or submenu.

Each menu in System Connectivity Manager has a standard set of menu commands. You can add these menu commands in the existing menus or under an existing or new submenu.

Note the following:

- You cannot create a new menu in System Connectivity Manager. You can only create submenus under an existing menu.
- You can only add an existing menu command to a menu or a submenu. However, you can create new menu commands only for user tools and Tcl/Tk tools in System Connectivity Manager. For more information on adding, modifying and deleting menu entries for user tools and Tcl/Tk tools in the *Tools* menu see [Customizing System Connectivity Manager Tools](#) on page 654.

The following sections describe how you can customize menus in System Connectivity Manager:

- [Adding Menu Commands, Submenus and Menu Separators](#) on page 638
- [Modifying the Label of Menu Commands and Submenus](#) on page 643
- [Deleting Menu Commands, Submenus and Menu Separators](#) on page 645
- [Making Custom Menus Available to Users](#) on page 648

Adding Menu Commands, Submenus and Menu Separators

To add a menu command, submenu, or menu separator:

1. Choose *Tools – Customize – Menus*

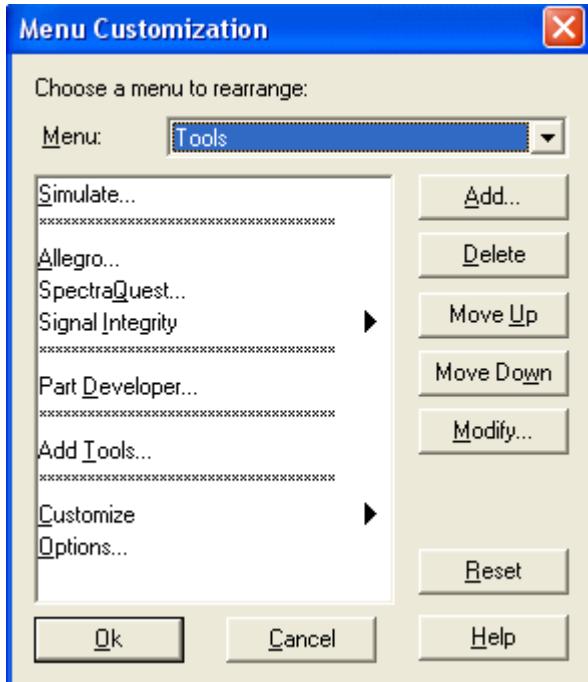
The Menu Customization dialog box appears.

2. From the *Menu* drop-down list, choose the menu or submenu under which you want to add a menu command, submenu or menu separator.

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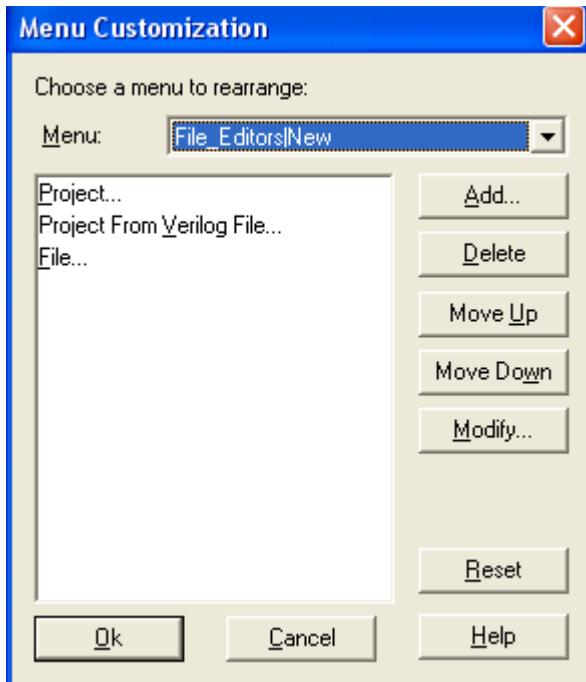
For example, if you want to add a menu command, submenu or menu separator in the *Tools* menu, choose *Tools* in the *Menu* drop-down list as shown below.



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If you want to add a menu command, submenu or menu separator under the New submenu in the File menu, choose *File_Editors/New* in the *Menu* drop-down list as shown below.



The menus displayed in *Menu* drop-down list in the Menu Customization dialog box are described below.

Menu	Description
File	Equivalent to <i>File</i> menu that appears when you start System Connectivity Manager without opening a project.
File_Editors	Equivalent to <i>File</i> menu that appears when a project is open in System Connectivity Manager.
File_ReportEditor	Equivalent to <i>File</i> menu that appears when a .dsr report file is open in System Connectivity Manager.
Edit	Equivalent to <i>Edit</i> menu that appears when a project is open in System Connectivity Manager.
Edit_Text	Equivalent to <i>Edit</i> menu that appears when you are editing a Verilog design in System Connectivity Manager.
Edit_Report	Equivalent to <i>Edit</i> menu that appears when a .dsr report file is open in System Connectivity Manager.

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Menu	Description
View_Text	Equivalent to <i>View</i> menu that appears when you are editing a Verilog design in System Connectivity Manager.
Format	Equivalent to <i>Format</i> menu that appears when a .dsr report file is open in System Connectivity Manager.
Project	Equivalent to <i>Project</i> menu that appears when a project is open in System Connectivity Manager.
Design_Text	Equivalent to <i>Design</i> menu that appears when you are editing a Verilog design in System Connectivity Manager.
Design_Table	Equivalent to <i>Design</i> menu that appears when you are editing a design in the spreadsheet editor.
Tools	Equivalent to <i>Tools</i> menu that appears when a project is open in System Connectivity Manager.
Window	Equivalent to <i>Window</i> menu that appears when a project is open in System Connectivity Manager.
Help	Equivalent to <i>Help</i> menu that appears when a project is open in System Connectivity Manager.

3. You can now add menu commands, submenus, or menu separators to the menu or submenu you selected in step 2.

To add a menu command

- a. Click *Add*.

The *Add Command* dialog box appears.

- b. Select the *Menu* option and choose the menu in which the command you want to add exists.

The commands in the selected menu are displayed in the *Command* list.

- c. In the *Command* list, select the menu command you want to add.

- d. Click *OK*.

The menu command is added to the menu or submenu you selected in step 2.

To add a new submenu

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- a. Click *Add*.

The *Add Command* dialog box appears.

- b. Select the *New Menu* option and enter the name of the menu in the text box.

Use the ampersand (&) character before the letter you want to use as the keyboard access key for the submenu. For example, if you want to use the letter U as the keyboard access key for a submenu named Utilities, enter the label for the menu command as &Utilities. The menu command will then appear as:

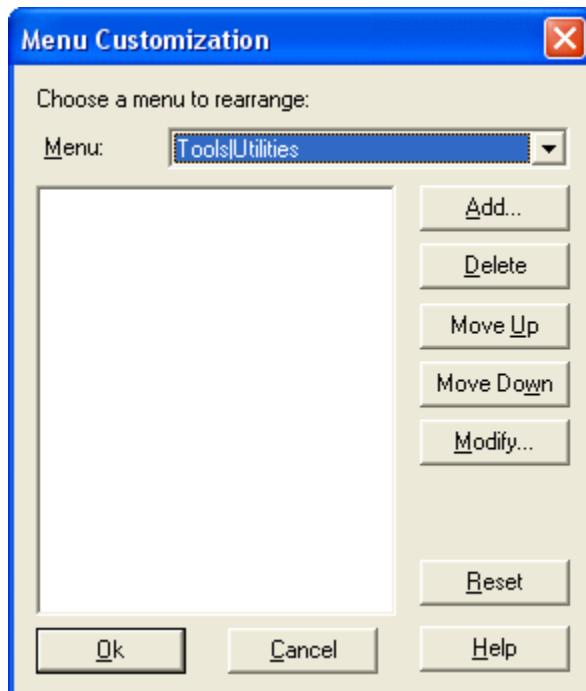
Ultilities

- c. Click *OK*.

The submenu is added to the menu or submenu you selected in [step 2](#).

- d. From the *Menu* drop-down list, choose the new submenu.

For example, if you have created a new submenu named *Utilities* in the *Tools* menu choose *Tools/Utilities* in the *Menu* drop-down list as shown below.



You can now add menu commands to the submenu by following the procedure described in [To add a menu command](#).

To add a menu separator

- a. Click *Add*.

The *Add Command* dialog box appears.

- b. Select the *Separator* option.
- c. Click *OK*.

The separator is added to the menu or submenu you selected in [step 2](#).

4. In the Menu Customization dialog box, select the command, submenu or separator you added and click the *Move Up* or *Move Down* button to move the command, submenu or separator to the desired location.
5. Click *OK* to save the changes.

For more information on making the custom menus available to users, see [Making Custom Menus Available to Users](#) on page 648.

Modifying the Label of Menu Commands and Submenus

To modify the label of a menu command or submenu:

1. Choose *Tools – Customize – Menus*

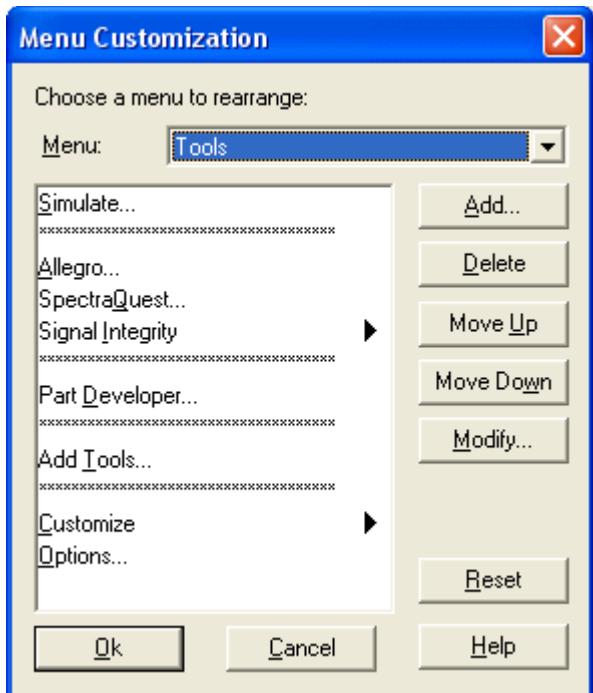
The Menu Customization dialog box appears.

2. From the *Menu* drop-down list, choose the menu or submenu under which the menu command or submenu you want to modify exists.

For example, if you want to modify a menu command or submenu in the *Tools* menu, choose *Tools* in the *Menu* drop-down list as shown below.

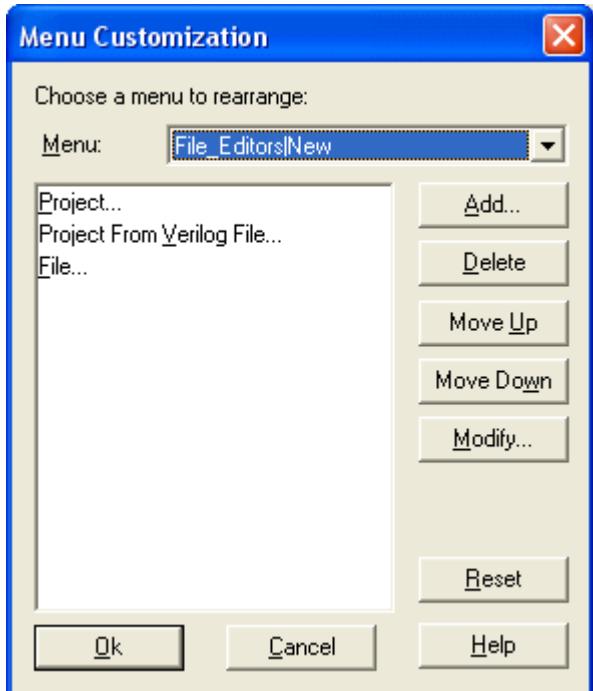
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All the commands and submenus in the *File* menu are displayed in the list.

If you want to modify a menu command or submenu under the *New* submenu in the *File* menu, choose *File_Editors/New* in the *Menu* drop-down list as shown below.



All the commands, submenus and menu separators in the *New* submenu are displayed in the list.

Note: The *Menu* drop-down list in the Menu Customization dialog box displays the menu names *File* and *File_Editors*. The commands listed in the *File* menu appear in the *File* menu in System Connectivity Manager when you start System Connectivity Manager without opening a project. The commands listed in the *File_Editors* menu appear in the *File* menu in System Connectivity Manager when you have opened a project in System Connectivity Manager. Hence, if you want to customize the *File* menu in System Connectivity Manager, choose *File_Editors* in the *Menu* drop-down list in the Menu Customization dialog box.

3. Select the menu command or submenu whose label you want to modify.

4. Click the *Modify* button.

The Modify Menu Label dialog box appears.

5. Modify the label for the menu command or submenu you selected in [step 3](#).

Use the ampersand (&) character before the letter you want to use as the keyboard access key for the menu command. For example, if you want to use the letter **D** as the keyboard access key for the menu command named Design Rules Check, enter the label for the menu command as &Design Rules Check. The menu command will then appear in the menu as:

Design Rules Check

6. Click *OK* to close the Modify Menu Label dialog box.

7. Click *OK* to close the Menu Customization dialog box.

For more information on making the custom menus available to users, see [Making Custom Menus Available to Users](#) on page 648.

Deleting Menu Commands, Submenus and Menu Separators

To delete a menu command, submenu, or menu separator:

1. Choose *Tools – Customize – Menus*

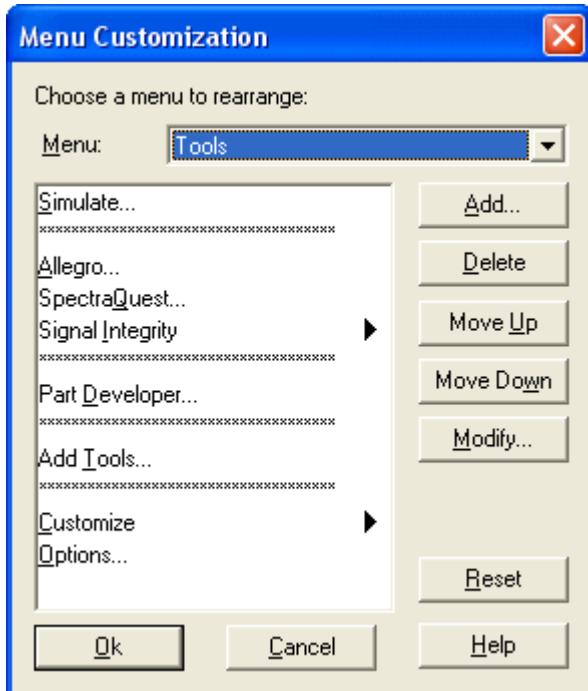
The Menu Customization dialog box appears.

2. From the *Menu* drop-down list, choose the menu or submenu under which you want to delete a menu command, submenu or menu separator.

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For example, if you want to delete a menu command, submenu or menu separator in the *Tools* menu, choose *Tools* in the *Menu* drop-down list as shown below.

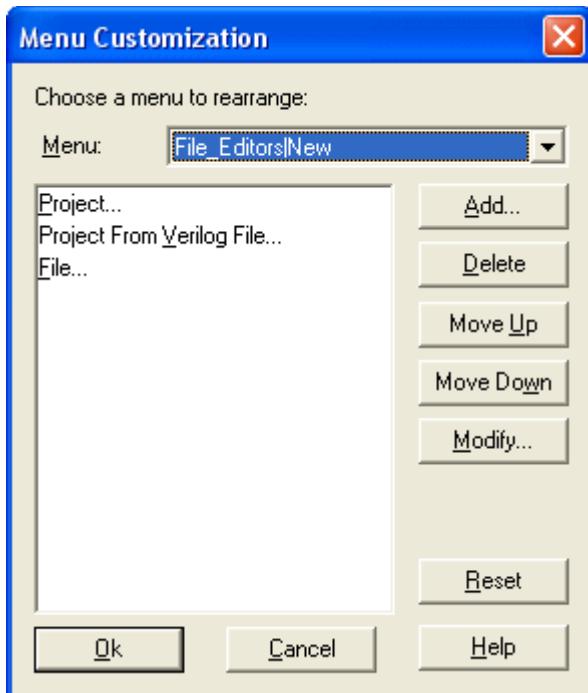


All the commands, submenus and menu separators in the File menu are displayed in the list.

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If you want to delete a menu command, submenu or menu separator under the New submenu in the File menu, choose *File_Editors/New* in the *Menu* drop-down list as shown below.



All the commands, submenus and menu separators in the New submenu are displayed in the list.

Note: The *Menu* drop-down list in the Menu Customization dialog box displays the menu names *File* and *File_Editors*. The commands listed in the *File* menu appear in the *File* menu in System Connectivity Manager when you start System Connectivity Manager without opening a project. The commands listed in the *File_Editors* menu appear in the *File* menu in System Connectivity Manager when you have opened a project in System Connectivity Manager. Hence, if you want to customize the *File* menu in System Connectivity Manager, choose *File_Editors* in the *Menu* drop-down list in the Menu Customization dialog box.

3. Select the command, submenu or menu separator you want to delete.
4. Click the *Delete* key.

Note: When you delete a menu command or submenu that is provided as part of the default System Connectivity Manager menus, the menu command or submenu is grayed out and not deleted from the menu. To undelete a menu command or submenu that is grayed out, select the menu command and click the *Undelete* button.

5. Click *OK*.

The menu command, submenu or separator you deleted is no longer displayed in the menu.

For more information on making the custom menus available to users, see [Making Custom Menus Available to Users](#) on page 648.

Making Custom Menus Available to Users

The settings for the custom menus are stored in the `tddMenus.txt` file and the settings for the menu entries for starting User and Tcl/Tk tools in the *Tools* menu are stored in the `tddCustomizeTBNEW.txt`. The `tddMenus.txt` and `tddCustomizeTBNEW.txt` files are located in the `\cdssetup\tdd` folder that is created in the directory specified by the `HOME` environment variable. For example, if the `HOME` environment variable is set to `c:\` the `tddMenus.txt` and `tddCustomizeTBNEW.txt` files will be located at `c:\cdssetup\tdd\`. The settings in the `tddMenus.txt` and `tddCustomizeTBNEW.txt` files at `$HOME\cdssetup\tdd\` are available only to the current user.

If you want to make the settings available to all users, copy the `tddMenus.txt` and `tddCustomizeTBNEW.txt` files from `$HOME\cdssetup\tdd` to the `\cdssetup\tdd` folder in your `CDS_SITE` location. For more information on the `CDS_SITE` environment variable, see [Creating a Custom Site Environment](#) on page 94.

By default, System Connectivity Manager uses the `tddMenus.txt` and `tddCustomizeTBNEW.txt` files located at `$HOME\cdssetup\tdd`. If the files do not exist at `$HOME\cdssetup\tdd`, it uses the `tddMenus.txt` and `tddCustomizeTBNEW.txt` files, if any, located at `$CDS_SITE\cdssetup\tdd`. If you want users to use only settings in the `tddMenus.txt` and `tddCustomizeTBNEW.txt` files located at `$CDS_SITE\cdssetup\tdd`, ensure that the `tddMenus.txt` and `tddCustomizeTBNEW.txt` files do not exist in the `$HOME\cdssetup\tdd` directory in each user's machine.

Note the following:

- Even if System Connectivity Manager is using the `tddMenus.txt` and `tddCustomizeTBNEW.txt` files located at `$CDS_SITE\cdssetup\tdd`, the changes you make to menus are always saved in the `tddMenus.txt` file located at `$HOME\cdssetup\tdd`, and the changes you make to the menu entries for starting User and Tcl/Tk tools in the *Tools* menu are always stored in the `tddCustomizeTBNEW.txt` file located at `$HOME\cdssetup\tdd`.

If you want to make the new settings available to all users, copy the `tddMenus.txt` and `tddCustomizeTBNEW.txt` files from `$HOME\cdssetup\tdd` to the `\cdssetup\tdd` folder in your `CDS_SITE` location.

Customizing Toolbars in System Connectivity Manager

Displaying and Hiding Toolbars

1. Choose *Tools – Customize – Toolbars*.

The Customize dialog box appears.

2. Click the Toolbars tab.

The *Toolbars* list displays the list of toolbars in System Connectivity Manager.

- Select the check box next to a toolbar to display it.
- Clear the check box next to a toolbar to hide it.

3. Click *OK*.

Creating Custom Toolbars

1. Choose *Tools – Customize – Toolbars*.

The Customize dialog box appears.

2. Click the Toolbars tab.

3. Click *New*.

The New Toolbar dialog box appears.

4. Enter the name of the toolbar and click *OK*.

System Connectivity Manager creates a new toolbar with the name you specified in the top left corner of the window.

5. Click the Commands tab.

6. Do one of the following:

- Add a button to the toolbar**

- a. Click a category in the *Categories* list.

- b. Drag the command you want from the *Commands* box to the toolbar.

Note: You can also press *Ctrl + Alt* and drag and drop the desired button from any other toolbar to the custom toolbar. You need not open the Customize dialog box to do this.

- **Add a built-in menu to the toolbar**
 - a. In the *Categories* list, click *Built-in Menus*.
 - b. Drag the menu you want from the *Commands* box to the toolbar.
- 7. Click *OK*.

Customizing Toolbars

You can use the following tips for adding and removing buttons in built-in (the toolbars provided with System Connectivity Manager) and custom toolbars, without opening the Customize dialog box.

- To add buttons to a built-in toolbar, press *Alt* and drag and drop the desired button from any other toolbar to the built-in toolbar.
- To add buttons to a custom toolbar, press *Ctrl + Alt* and drag and drop the desired button from any other toolbar to the custom toolbar.
- To remove a button from a toolbar, press *Alt* and drag and drop the desired button into an empty area in System Connectivity Manager.

Moving Toolbars

To move a toolbar, drag the move handle  on a docked toolbar, or the title bar on a floating toolbar, to the new location.

Note: If you drag the toolbar to the edge of the program window, it becomes a docked toolbar. When you move one docked toolbar, this might affect the location and size of other toolbars on the same row.

Deleting Toolbars

You can only delete the custom toolbars you created in System Connectivity Manager. You cannot delete the predefined toolbars in System Connectivity Manager.

1. Choose *Tools – Customize – Toolbars*.
The Customize dialog box appears.
2. Click the Toolbars tab.
3. In the *Toolbars* list select the custom toolbar you want to delete.

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Customizing System Connectivity Manager

4. Click *Delete*.

Customizing the Spreadsheet Editor

You can customize the view in the Component List, Signal List, Component Connectivity Details pane, Signal Connectivity Details pane, Physical Part List, Physical Net List, Physical Part Connectivity Details pane, and the Physical Net Connectivity Details pane by doing the following:

- [Hiding/Showing Columns](#) on page 652
- [Adding Columns to Display Property Values](#) on page 653



If you have customized the Component List in System Connectivity Manager Version 15.5, do the following when you open the design in System Connectivity Manager Version 15.5.1.

- a. Click in the Component List.
 - b. Choose *Table – Customize Columns*.
- The Customize Pane dialog box appears.
- c. Click the *Reset* button.
 - d. Redo the customization you made in the Component List.
 - e. Click *OK*.
 - f. Exit System Connectivity Manager and reopen the project in System Connectivity Manager.

Hiding/Showing Columns

You can hide and show columns in the Component List, Signal List, Component Connectivity Details pane, Signal Connectivity Details pane, Physical Part List, Physical Net List, Physical Part Connectivity Details pane, and the Physical Net Connectivity Details pane.

For example, the Component List shows four columns, a view icon, Instance, Ref Des, Cell, and Comments. To hide or show columns in the Component List, do the following:

1. Right-click on a column heading name.
2. Clear the check mark to the left of a column to hide the column or click a column to show it.

Adding Columns to Display Property Values

You can add new columns to display property values in the Component List, Signal List, Component Connectivity Details pane, Signal Connectivity Details pane, Physical Part List, Physical Net List, Physical Part Connectivity Details pane, and the Physical Net Connectivity Details pane.

To add a column for displaying property values

1. Click in the pane in which you want to add a column for displaying property values.

For example, if you want to add a column in the Component List, click in the Component List.

2. Choose *Table – Customize Columns*.

The Customize Pane dialog box appears.

3. Click the *Add New* button.

The Column Definition dialog box appears.

4. From the *Property Owner* drop-down list, select the object for which you want to display the list of properties in the *Property Name* field.

Select	If
Component	<p>You want to add a column for a component property.</p> <p>Component properties are displayed in the <i>Property Name</i> field.</p> <p>Note: You cannot add columns for component properties in the Signal List and the Physical Net List.</p>
Pin	<p>You want to add a column for a pin property.</p> <p>Pin properties are displayed in the <i>Property Name</i> field.</p> <p>Note: You cannot add columns for pin properties in the Component List, Physical Part List, Signal List and Physical Net List.</p>

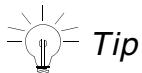
Select	If
Net	You want to add a column for a net property. Net properties are displayed in the <i>Property Name</i> field. Note: You cannot add columns for net properties in the Component List, Component Connectivity Details pane, and in the Physical Part List.

5. From the *Property Name* drop-down list, select the property for which you want to add a column.
6. Enter the width to be used for displaying the column.
7. Click *OK*.

The Customize Pane dialog box appears. The new column is displayed in the *Available Columns* list.

8. Select the new column in the *Available Columns* list and click *Add* to add the column in the *Added Columns* list.
9. Click *OK*.

The column for the property is displayed in the pane in which you added the column. For example, if you add a column for a component property in the Component List, the column for the property is displayed in the Component List. If you want to add a column for the same component property in the Component Connectivity Details pane or the Signal Connectivity Details pane, you must add the column again by performing the procedure described above.



Tip
Using the steps listed above, you can also display the a physical pin property and a user-defined pin property —present in the `chips.prt` file — in Component Connectivity Details Pane. However, if physical pin properties are displayed as read-only properties. You cannot edit these properties in System Connectivity Manger. For editing physical pin properties, use Allegro Part Developer.

Customizing System Connectivity Manager Tools

You can start tools such as Allegro Part Developer from the *Tools* menu in System Connectivity Manager. System Connectivity Manager lets you create menu entries for new tools in the *Tools* menu. You can create menu entries for user tools (tools with `.exe` and

.com file extensions) and Tcl/Tk tools. You can then start the tools from System Connectivity Manager. For more information, see the following sections:

- [Adding Menu Entries for New Tools in the Tools Menu](#) on page 655
- [Changing Tool Settings](#) on page 657
- [Deleting Menu Entries for Tools from the Tools Menu](#) on page 658

For more information on making the menu items for user and Tcl/Tk tools in the *Tools* menu available to users, see [Making Custom Menus Available to Users](#) on page 648.

Adding Menu Entries for New Tools in the Tools Menu

To add a new tool to the Tools menu, choose *Tools – Add Tools*.

The Add Tools dialog appears. In this dialog, you can add menu entries for user tools (tools with .exe and .com file extensions) and for Tcl/Tk tools.

For information on adding menu entries for user tools, see [Adding Menu Entries for User Tools in the Tools Menu](#) on page 655.

For information on adding menu entries for Tcl/Tk tools, see [Adding Menu Entries for Tcl/Tk Tools in the Tools Menu](#) on page 656.

Adding Menu Entries for User Tools in the Tools Menu

1. Select the User Tools tab.
2. Click *Add*.
3. In the *Menu Text* field, type the name of the tool as you want to appear in the *Tools* menu.

Use the ampersand (&) character before the letter you want to use as the keyboard access key for the menu command for the tool. For example, if you want to use the letter D as the keyboard access key for the menu command named Design Entry HDL, enter the label for the menu command as &Design Entry HDL. The menu command will then appear in the *Tools* menu as:

Design Entry HDL

4. In the *Command* field, type the path to the tool's executable file (.exe or .com), or click the browse button to select the executable file.

5. In the *Arguments* field, type the command arguments with which you want to start the tool from System Connectivity Manager.
6. In the *Initial Directory* field, type the path to the directory where you want the tool to start, or click the browse button to select the directory.
7. Select the *Project File* check box if you want to pass the current project file (<projectname>.cpm) as an argument to the tool when it is started from System Connectivity Manager. The tool will be started in the context of the project.
8. Select the *Mps Args* check box if you want to pass MPS (Message Passing Subsystem) arguments to the tool when it is started.

When you start the tool from System Connectivity Manager, the tool will run in the same MPS session as System Connectivity Manager. When tools run in the same MPS session, you can perform cross-probing between the tools.

Note: You can pass MPS arguments only to Cadence tools. Third-party tools do not support MPS arguments.

9. Click *OK*.

The menu entry for the tool is displayed in the *Tools* menu. You can now start the tool from System Connectivity Manager.

Note: The settings for the menu entries to start tools in the Tools menu are stored in the `tddCustomizeTBNEW.txt` file in the `\cdssetup\tdd` folder that is created in the directory specified by the `HOME` environment variable. For example, if the `HOME` environment variable is set to `c:\` the settings for the customized menus will be stored in:

`c:\cdssetup\tdd\tddCustomizeTBNEW.txt`

Adding Menu Entries for Tcl/Tk Tools in the Tools Menu

You can create menu entries for Tcl procedures in the *Tools* menu and run the procedures from System Connectivity Manager. When you run a Tcl procedure, System Connectivity Manager passes the name of the top-level or root design as an argument to the Tcl procedure. You can also use this functionality to run Tcl/Tk applications.

Note: Before you add a menu entry for a Tcl procedure in the *Tools* menu, you must setup the `.tcl` file containing the Tcl procedure as described in [Setting Up the .tcl Files for Tcl/Tk Procedures on page 657](#).

1. Select the Tcl/Tk Tools tab.
2. Click *Add*.

3. In the *Menu Text* field, type the name of the Tcl/Tk tool for which you want to create a menu entry in the *Tools* menu.

Use the ampersand (&) character before the letter you want to use as the keyboard access key for the menu command for the tool. For example, if you want to use the letter R as the keyboard access key for the menu command named `Process Reports`, enter the label for the menu command as `Process &Reports`. The menu command will appear in the *Tools* menu as:

Process Reports

4. In the *Tcl Function* field, enter the name of the Tcl procedure that you want to be run when you select the menu entry for the Tcl procedure in the *Tools* menu.

5. Click *OK*.

The menu entry for the Tcl/Tk procedure is displayed in the *Tools* menu. You can now run the procedure from System Connectivity Manager.

Note: The settings for the menu entries for starting Tcl tools in the Tools menu will be stored in the `tddCustomizeTBNEW.txt` file in the `\cdssetup\tdd` folder that is created in the directory specified by the `HOME` environment variable. For example, if the `HOME` environment variable is set to `c:\` the settings for the customized menus will be stored in:

`c:\cdssetup\tdd\tddCustomizeTBNEW.txt`

Setting Up the .tcl Files for Tcl/Tk Procedures

1. Place the `.tcl` file containing the Tcl procedures in the `\share\cdssetup\tdd\custom_rules` folder in your Cadence installation or `CDS_SITE` location.
2. Open the Windows command prompt or a Unix or Linux terminal.
3. Change to the `\share\cdssetup\tdd\custom_rules` folder.
4. Run the following command:

```
tclsh auto_mkindex *.tcl
```

The Tcl index file named `tclIndex` is created in the `\share\cdssetup\tdd\custom_rules` folder. The `tclIndex` file contains the list of Tcl procedures that can be run from System Connectivity Manager.

Changing Tool Settings

To change the settings of a tool for which you have added a menu entry in the Tools menu:

1. Choose *Tools – Add Tools*.

The Add Tools dialog box appears.

2. Do one of the following:

- Select the User Tools tab if you want to change the settings for a user tool (tool with .exe and .com file extensions).
- Select the Tcl/Tk Tools tab if you want to change the settings for a Tcl/Tk tool.

3. Select the menu entry for the tool in the *Menu Contents* list.

4. Change the tool settings and click *OK*.

Deleting Menu Entries for Tools from the Tools Menu

You can delete the menu entry that you added for a tool in the *Tools* menu in System Connectivity Manager.

To delete the menu entry for a tool from the Tools menu:

1. Choose *Tools – Add Tools*.

The Add Tools dialog box appears.

2. Do one of the following:

- Select the User Tools tab if you want to delete the menu entry for a user tool (tool with .exe and .com file extensions).
- Select the Tcl/Tk Tools tab if you want to delete the menu entry for Tcl/Tk tool.

3. Select the menu entry for the tool in the *Menu Contents* list.

4. Click *Remove*.

5. Click *OK*.

Dialog Box Descriptions

This appendix describes the dialog boxes in System Connectivity Manager. The dialog boxes are listed in alphabetical order.

Add Bypass Capacitors

Use this dialog box to add bypass capacitors to components.

Note: Before you add bypass capacitors, ensure that DC nets (nets with the VOLTAGE property) exist in your design.

How to Access

- Right-click on a component in the Component List and choose *Add Bypass Capacitor* from the shortcut menu.
- Select an object and choose *Object – Associate Components – Add Bypass Capacitors*



Click this icon to display the properties on the bypass capacitor in the Properties window.

Here you can add, modify or delete properties on the bypass capacitor. For more information on using the Properties window, see [Using System Connectivity Manager to Manage Properties](#) on page 253.

RefDes

Displays the reference designator of the bypass capacitor.

You can modify the reference designator.

Cell

Displays the name of the capacitor component.

Value

Displays the capacitance value.

System Connectivity Manager User Guide

Dialog Box Descriptions

Quantity	<p>Displays the number of instances of the bypass capacitor added on the component.</p> <p>When you add or paste a bypass capacitor, the quantity is displayed as 1. You can modify the quantity if you want to add multiple instances of the bypass capacitor on the component. For example, if you type 4 in the <i>Quantity</i> field, four instances of the bypass capacitor are displayed (in four separate rows) in the Add Bypass Capacitors dialog box when you click the <i>Apply</i> or <i>OK</i> button.</p> <p>Note: When you click the <i>Apply</i> or <i>OK</i> button, System Connectivity Manager automatically packages the bypass capacitors you added or pasted in the Add Bypass Capacitors dialog box and assigns reference designators to the bypass capacitors. Once a bypass capacitor is packaged, you cannot modify the quantity in the <i>Quantity</i> field. If you want to add more instances of a bypass capacitor that is packaged, select the row for the bypass capacitor, click the <i>Copy</i> button, click an empty row in the Add Bypass Capacitors dialog box, then click the <i>Paste</i> button.</p>
Pin 1	Displays the name of the first pin of the bypass capacitor.
Signal 1	Displays the name of the signal connected to the first pin of the bypass capacitor. <p>Click on the <i>Signal 1</i> field and select the signal you want to connect to the pin.</p> <p>Note: Ensure that the pins of the bypass capacitors are connected to signals before you click <i>OK</i> or <i>Apply</i>.</p>
Pin 2	Displays the name of the second pin of the bypass capacitor.
Signal 2	Displays the name of the signal connected to the second pin of the bypass capacitor. <p>Click on the <i>Signal 2</i> field and select the signal you want to connect to the pin.</p> <p>Note: Ensure that the pins of the bypass capacitors are connected to signals before you click <i>OK</i> or <i>Apply</i>.</p>

System Connectivity Manager User Guide

Dialog Box Descriptions

Add	Lets you add bypass capacitors on the component. When you click the <i>Add</i> button, Part Information Manager appears. <ol style="list-style-type: none">1. In the <i>Cells</i> list, select the capacitor component you want to add.2. In the <i>Search Results</i> pane, select the part table row that specifies the capacitance value you want to use.3. Click the <i>Add</i> button to display the capacitor in the Add Bypass Capacitors dialog box.
Delete	Select the rows for the bypass capacitors you want to delete and click this button to delete the bypass capacitors.
Copy	Select the rows for the bypass capacitors you want to copy and click this button to copy the bypass capacitors.
Paste	Select an empty row in the Add Bypass Capacitors dialog box and click this button to paste the rows for the bypass capacitors you copied using the <i>Copy</i> button. Note the following: <ul style="list-style-type: none">■ You cannot paste more than one instance of a row for a bypass capacitor you copied using the <i>Copy</i> button. For example, if you copy a row for a bypass capacitor, select more than one empty row in the Add Bypass Capacitors dialog box and click <i>Paste</i>, only one row is pasted. If you want to add more than one instance of the bypass capacitor you pasted, modify the quantity in the <i>Quantity</i> column in the pasted row.■ The pasted bypass capacitors are not automatically packaged. Click the <i>Apply</i> or <i>OK</i> button to package the bypass capacitors.

System Connectivity Manager User Guide

Dialog Box Descriptions

Modify	Lets you modify the capacitance value of the selected bypass capacitor. Select the row for the bypass capacitor whose capacitance value you want to modify and click the <i>Modify</i> button to display the Modify Component dialog box. <ol style="list-style-type: none">1. Select the part table row that specifies the capacitance value you want to use.2. Click the <i>Modify</i> button to display the new capacitance value in the Add Bypass Capacitors dialog box.
Setup	Displays the <u>Discrete Component Setup</u> dialog box where you can specify the discrete components (resistors, capacitors, diodes and inductors) that appear as the default selection in Part Information Manager when you apply terminations, bypass capacitors and pullups or pulldowns in your design.
Apply	Applies the changes you made in the Add Bypass Capacitors dialog box. When you click <i>Apply</i> , System Connectivity Manager automatically packages the bypass capacitors you added or pasted in the Add Bypass Capacitors dialog box and assigns reference designators to the bypass capacitors. Note: Once a bypass capacitor is packaged, you cannot modify the quantity in the <i>Quantity</i> field. If you want to add more instances of a bypass capacitor that is packaged, select the row for the bypass capacitor, click the <i>Copy</i> button, click an empty row in the Add Bypass Capacitors dialog box, then click the <i>Paste</i> button.

Add Command

Lets you add a new menu command or a separator to the menu you selected in the Menu Customization dialog box.

You can do the following:

- Add commands from an existing menu to the selected menu.
- Add a new menu command to the selected menu.
- Add a separator to the selected menu.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Click Add in the [Menu Customization](#) dialog box.

Menu	Lets you add commands from an existing menu to the menu you selected in the Menu Customization dialog box. Select this option and then select the menu from which you want to add commands. The commands in the menu are displayed in the <i>Command</i> list. Select the command you want to add to the menu you selected in the Menu Customization dialog box, and click <i>OK</i> .
New Menu	Lets you add a new menu command to the menu you selected in the Menu Customization dialog box. Select this option and enter the label for the new menu command in the text box. Use the ampersand (&) character before the letter you want to use as the keyboard access key for the menu command. For example, if you want to use the letter D as the keyboard access key for the menu command named Design Rules Check, enter the label for the menu command as &Design Rules Check. The menu command will then appear in the menu as: <u>Design Rules Check</u>
	Note: When you define the access key for a menu command, ensure that the same access key is not being used by any other command in the menu.
Separator	Select this option and click <i>OK</i> to add a separator to the menu you selected in the Menu Customization dialog box.
Command	If the <i>Menu</i> option is selected, displays the commands in the selected menu. Select the command you want to add to the menu you selected in the Menu Customization dialog box. If the <i>New Menu</i> option is selected, displays the label for the new menu command you want to add to the menu you selected in the Menu Customization dialog box. If the <i>Separator</i> option is selected, displays the separator you want to add to the menu you selected in the Menu Customization dialog box.

Add Ports

Lets you add the ports or interface signals for a block. The ports are displayed in the Signal List.

How to Access

- Choose *Design – Add Port*.

Port Name	Specify the port name. For more information on the naming conventions for ports, see Signal Naming Conventions on page 144.
Port Type	Select the port type as <i>IN</i> , <i>OUT</i> , <i>INOUT</i> . To select the port type, click in the <i>Port Type</i> cell and choose the port type in the drop-down list.
Voltage	Specify the voltage of the port. The default unit for voltage is Volts. To specify the voltage in millivolts, say, 75 Mv, enter the voltage as: 0.075 You can enter any numeric value. The use of the letter V for volts is optional. The voltage value you enter is rounded to three digits.

Add Pullup/PullDown

Pullups and pulldowns are used to reduce noise in the circuit. Use this dialog box to add a pullup or pulldown for the selected signal. The Add Pullup/Pulldown dialog box allows you to add, delete or modify pullups or pulldowns to a signal.

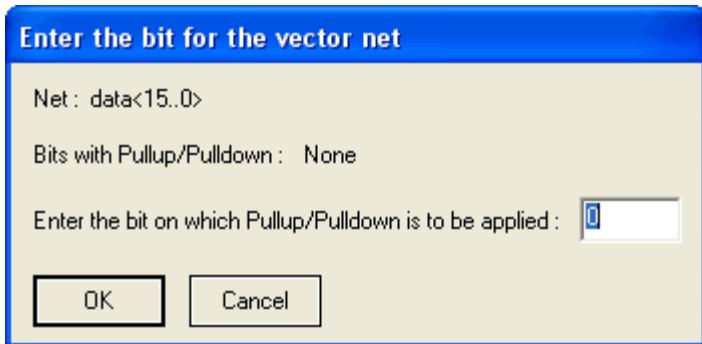
How to Access

- To add a pullup or pulldown for a single pin, do one of the following:
 - Select a signal in the Signal List and choose *Object – Associate Components – Add Pullup/Pulldown*.

System Connectivity Manager User Guide

Dialog Box Descriptions

If the selected signal is a vectored signal, the *Enter the bit for the vector net dialog box* appears. Enter the bit on which you want to add the pullup or pulldown and click *OK*.



- ❑ Double-click any cell in the Pullup/Pulldown column (the column with the  symbol) in the Component Connectivity Details pane.
or
Click on any cell in the Pullup/Pulldown column (the column with the  symbol) in the Component Connectivity Details pane and choose *Object – Associate Components – Add Pullup/Pulldown*.

If the pin is not connected to any signal, System Connectivity Manager connects the pin to a new signal named `signal_n` (where `n` is a number). For example, if the pin is not connected to a signal, System Connectivity Manager connects the pin to a new signal named `signal_1`.

- To add a pullup or pulldown to multiple pins, do the following:
 - a. Select the cell in the Pullup/Pulldown column (the column with the  symbol) next to each pin on which you want to add a pullup or pulldown.
 - b. Choose *Object – Associate Components – Add Pullup/Pulldown*.
 - If only one of the selected pins is not connected to any signal, System Connectivity Manager connects the pin to a new signal named `signal_n` (where `n` is a number). For example, System Connectivity Manager connects the unconnected pin to a new signal named `signal_1`.

System Connectivity Manager User Guide

Dialog Box Descriptions

- If two or more selected pins are not connected to any signal, System Connectivity Manager displays the following message:



Click *Yes* to wire the unconnected pins to the same signal. System Connectivity Manager connects the pins to a new signal named `signal_n` (where `n` is a number). For example, System Connectivity Manager connects the pins to a new signal named `signal_1`.

Click *No* to wire the unconnected pins to different signals. System Connectivity Manager connects the pins to new signals named `signal_n` (where `n` is a number). For example, if there are three unconnected pins, System Connectivity Manager connects the first pin to `signal_1`, the second pin to `signal_2` and the third pin to `signal_3`.

Click *Cancel* to cancel the process of adding the pullup or pulldown.

Type

Select between *Pullup* or *Pulldown*.

The following options are displayed in this drop-down list if you have selected multiple pins for adding pullups or pulldowns.

- Pulldown For Each Connection
- Pulldown For Each Unique Net
- Pullup For Each Connection
- Pullup For Each Unique Net

For more information on these options, see [Table 11-2](#) on page 308.

System Connectivity Manager User Guide

Dialog Box Descriptions

R1	<p>Click the <i>Part</i> button to select the resistor for the pullup or pulldown.</p> <p>When you click the <i>Part</i> button, Part Information Manager appears.</p> <ol style="list-style-type: none">1. In the <i>Cells</i> list, select the resistor component you want to use.2. In the <i>Search Results</i> pane, select the part table row that specifies the resistance value you want to use.3. Click the <i>Add</i> button.
DC Net	Select the DC net you want to use for the pullup or pulldown.
	Click this icon to display the Properties window where you can view, add, delete or modify properties on the resistor component you select for the pullup or pulldown.
Identifier	Displays the identifier for the resistor.
RefDes	Displays the reference designator of the resistor. You can enter the reference designator value or let System Connectivity Manager automatically assign the value.
	You can modify the reference designator value.
Section	Displays the section number of the resistor.
Pin Name	Displays the pin names of the resistor.
Pin No.	Displays the pin numbers of the resistor.
Signals	Displays the names of the signals connected to the resistor pins.
Apply	Applies the changes you made.
Setup	Displays the <u>Discrete Component Setup</u> dialog box where you can define the discrete components (resistors, capacitors and diodes) that appear as the default selection in Part Information Manager when you apply terminations, bypass capacitors, pullups or pulldowns in your design.

Add Signal(s)

Use this dialog box to add new signals in the design.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Click on the Signal List and choose *Design – Add Signal*.
- Right-click on the Signal List and choose Add Signal from the shortcut menu.



Differential Pair column

Select the check box in this column if you want to add a differential pair signal to the design.

Signal Name

Enter the name of the signal to be added.

Note: For information on the naming conventions for signals, see [Signal Naming Conventions](#) on page 144.

In case you are adding differential pair, enter the base name for the member nets of the differential pair. The names for the two member nets of the differential pair are generated by applying the [Format for Naming Differential Pair Signals](#) to the signal name specified in this text box.

Signal Type

Select the signal type as *IN*, *OUT*, *INOUT*, *LOCAL* or *GLOBAL*.

To select the signal type, click in the *Signal Type* cell and select a signal type in the drop-down list.

Voltage

Specify the voltage of the signal.

The default unit for voltage is Volts. To specify the voltage in millivolts, say, 75 Mv, enter the voltage as:

0.075

You can enter any numeric value. The use of the letter v for volts is optional. The voltage value you enter is rounded to three digits.

Differential Pair Name Lists the name for the differential pair signal to be added to the design.

Default name is generated by appending the signal name specified in the Signal Name column to the prefix value specified in the Prefixes For Differential Pair Names For Signals text box. If required, you can modify the default name and specify a different value.



This column is enabled only if the check box in the differential pair column is selected.

Add Termination

The Add Termination dialog box allows you to apply terminations to high speed nets. This will allow you to perform simulations early in the design cycle—right at the logic design capture stage.

How to Access

Do one of the following:

- Choose *Object – Associate Components – Add Termination*.
- Double-click in the *Termination* column in the Component Connectivity Details or Signal Connectivity Details pane.

System Connectivity Manager User Guide

Dialog Box Descriptions

- Right-click in the *Termination* column in the Component Connectivity Details or Signal Connectivity Details pane, and choose *Add Termination*.

Type Displays the valid termination types for the selected pin. You can select a termination type.

The termination types available for different pin types are:

- Input (receiver pin)—Shunt, Shunt RC, Thevenin, Ground Clamp Diode, Power Clamp Diode, and Dual Clamp Diode
- Output (driver pin)—Series
- Inout—Series, Shunt, Shunt RC, Thevenin, Ground Clamp Diode, Power Clamp Diode, and Dual Clamp Diode

System Connectivity Manager displays a thumbnail view of the selected termination type.

Note: You cannot add terminations on Unspec pins.

Delay Constraint (d) Specifies the time by which the constraint can be delayed without any information loss.

The delay constraint value is used to create a Propagation Delay constraint on a pin-pair that connects the terminating pin with the pin of the termination. Any future changes in value of the Propagation Delay constraint will automatically be reflected in the *Delay Constraint* field.

Value/Cutoff Voltage Displays the value of the resistors, capacitors or diodes used in the termination scheme.

Part Displays Part Information Manager where you can select the resistor, capacitors, or diodes to be used for terminations.

High/Low Select the higher or lower voltage based on available values.

Note: The High or Low fields appear based on the termination type you select.

Note: To add a new voltage value, you would have to define a new power signal.

Click this icon to display the Properties window where you can view, add, delete or modify properties on the resistor, capacitor, or diode component you selected for the termination.



System Connectivity Manager User Guide

Dialog Box Descriptions

Property Grid	Displays the following property values for the selected component. <ul style="list-style-type: none">■ Identifier—Displays the unique identifier for the termination component.■ Refdes—Displays the reference designator value.■ Section—Displays the section number.■ Pin Name—Displays the pin names of the termination component.■ Pin No.—Displays the pin numbers of the termination component.■ Signals—Displays the name of the signal that connects to each pin.
Apply	Applies the changes you made.
Setup	Displays the <u>Discrete Component Setup</u> dialog box where you can define the discrete components (resistors, capacitors and diodes) that appear as the default selection in Part Information Manager when you apply terminations, bypass capacitors, pullups or pulldowns in your design.

Add Tools

Lets you create menu entries for tools in the *Tools* menu. You can create menu entries for user tools (tools with .exe and .com file extensions) and Tcl/Tk tools. You can then start the tools from System Connectivity Manager.

Note: The settings for the menu entries for starting tools in the Tools menu will be stored in the `tddCustomizeTBNEW.txt` file in the `\cdssetup\tdd` folder that is created in the directory specified by the `HOME` environment variable. For example, if the `HOME` environment variable is set to `c:\` the settings for the customized menus will be stored in:

`c:\cdssetup\ade\tddCustomizeTBNEW.txt`

How to Access

- Choose *Tools – Add Tools*

System Connectivity Manager User Guide

Dialog Box Descriptions

User Tools

Lets you create menu entries for user tools (tools with .exe and .com file extensions) in the *Tools* menu in System Connectivity Manager. You can then start the tools from System Connectivity Manager.

Menu Contents	Displays the list of tools for which menu entries have been created in the <i>Tools</i> menu.
Menu Text	Type the name of the tool for which you want to create a menu entry in the <i>Tools</i> menu. You can modify the text to change the menu entry that appears in the <i>Tools</i> menu. Use the ampersand (&) character before the letter you want to use as the keyboard access key for the menu command for the tool. For example, if you want to use the letter D as the keyboard access key for the menu command named Design Entry HDL, enter the label for the menu command as &Design Entry HDL. The menu command will then appear in the <i>Tools</i> menu as:
	<u>Design Entry HDL</u>
	Note: When you define the access key for a menu command, ensure that the same access key is not being used by any other menu command in the Tools menu.
Command	Type the full path to the tool's executable file (.exe or .com), or click the browse button to select the executable file.
Arguments	Type the command arguments with which you want to start the tool from System Connectivity Manager.
Initial Directory	Type the path to the directory where you want the tool to start, or click the browse button to select the directory.
Add	Click to add a menu entry for a new tool.
Remove	Removes the menu entry for the selected tool from the <i>Tools</i> menu.
Move Up	Moves the menu entry for the selected tool, one level up in the <i>Tools</i> menu.
Move Down	Moves the menu entry for the selected tool, one level down in the <i>Tools</i> menu.

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Dialog Box Descriptions

Other Args

Project File Select this check box if you want to pass the current project file (`<projectname>.cpm`) as an argument to the tool when it is started from System Connectivity Manager. The tool will be started in the context of the project. Clear this box if you do not want to pass the current project file as an argument to the tool.

Mps Args Select this check box if you want to pass MPS (Message Passing Subsystem) arguments to the tool when it is started.

When you start the tool from System Connectivity Manager, the tool will run in the same MPS session as System Connectivity Manager. When tools run in the same MPS session, you can perform cross-probing between the tools.

Note: You can pass MPS arguments only to Cadence tools. Third-party tools do not support MPS arguments.

Tcl/Tk Tools

Lets you create menu entries for Tcl procedures in the *Tools* menu and run the procedures from System Connectivity Manager. When you run a Tcl procedure, System Connectivity Manager passes the name of the top-level or root design as an argument to the Tcl procedure. You can also use this functionality to run Tcl/Tk applications from System Connectivity Manager.

Note: Before you add a menu entry for a Tcl procedure in the *Tools* menu, you must setup the `.tcl` file containing the Tcl procedure as described in [Setting Up the .tcl Files for Tcl/Tk Procedures](#) on page 655.

Menu Contents Displays the list of Tcl/Tk procedures for which menu entries have been created in the *Tools* menu.

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Dialog Box Descriptions

Menu Text	Type the name of the Tcl/Tk procedure for which you want to create a menu entry in the <i>Tools</i> menu. You can modify the text to change the menu entry that appears in the <i>Tools</i> menu. Use the ampersand (&) character before the letter you want to use as the keyboard access key for the menu command for the tool. For example, if you want to use the letter R as the keyboard access key for the menu command named Process Reports , enter the label for the menu command as Process &Reports . The menu command will then appear in the <i>Tools</i> menu as: Process <u>R</u>eports
	Note: When you define the access key for a menu command, ensure that the same access key is not being used by any other menu command in the <i>Tools</i> menu.
Tcl Function	Enter the name of the Tcl procedure that you want to be run when you select the menu entry for the Tcl procedure in the <i>Tools</i> menu. System Connectivity Manager passes the name of the top-level or root design as an argument to the Tcl procedure.
Add	Click to add a menu entry for a new Tcl/Tk tool.
Remove	Removes the menu entry for the selected Tcl/Tk tool from the <i>Tools</i> menu.
Move Up	Moves the menu entry for the selected Tcl/Tk tool, one level up in the <i>Tools</i> menu.
Move Down	Moves the menu entry for the selected Tcl/Tk tool, one level down in the <i>Tools</i> menu.

Archiver: Specify Project Name

Lets you specify the project to be archived.

How to Access

Do one of the following:

- Choose *Project – Archive Project*.

System Connectivity Manager User Guide

Dialog Box Descriptions

- Click *Archive a Project* in the System Connectivity Manager start page.

The System Connectivity Manager start page is displayed when you start System Connectivity Manager. If a design is already open in System Connectivity Manager, click the tab for the System Connectivity Manager start page, or choose *Help – Display Start Page* to display the start page.

- Run the following command in the Windows, Unix or Linux command prompt:

```
dsarchiver
```

Note: If the project is already open in System Connectivity Manager and you choose *Project – Archive Project* or click *Archive a Project* in the System Connectivity Manager start page, the Archiver: Specify External Files window appears.

Project File Name

Enter the name and path to the project (.cpm) file for the project you want to archive, or click the browse button to select the file.

Archiver: Specify External Files

By default, the following files and directories are included in the archive. You can use the Archiver: Specify External Files window to include any other files and directories in the archive.

- <projectname>.cpm file.
- cds.lib file.
- archiver.log file.
- Directories for working libraries for your project.

Note: Only the components and blocks in the working libraries for your project that are used in the design are archived. The components and blocks in the working libraries that are not used in the design will not be archived.

- Components from the reference libraries used in the design and the page border, TAP, OFFPAGE, IMPORT, OUTPORT and IOPORT symbols you specified in the Document Schematic Generation Setup tab of the Setup dialog box.

Note: Only the components in a reference library that are used in the design are archived.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Click Next in the [Archiver: Specify Project Name](#) dialog box.

Include Report Files	Select this check box if you want to include all the report files in the location for storing reports that you specified in the Report Generation tab of the Setup dialog box.
	Note: By default, reports are stored in the <code>reports</code> folder in the project directory.
Include Model Files	Select this check box if you want to include all the signal integrity device model library (<code>.DML</code>) and device model library index (<code>.NDX</code>) files setup for your project.
	For more information on setting up signal integrity (SI) model libraries for your project, see Setting Up SI Model Libraries on page 320.
File Name	Displays the name of the file that you have included for archiving. If the <i>File Name</i> field displays the text <code>*.*</code> , it indicates that all the files in the directory displayed in the corresponding <i>Path</i> field, and all the files in the subdirectories under the directory will be archived.
Path	Displays the path to the directories whose files will be included in the archive.



To include a file or directory in the archive, select the file or directory in the left pane and click . The file or directory is added in the right pane.

To select a file or folder that is outside the project directory, click the browse button in the left pane to select the folder in which the directory or file you want to include exists. The file or directory is displayed in the left pane. Select the file or directory in the left pane and click to include it in the archive.

When you include a directory, the *File Name* field in the right pane displays *.*., indicating that all the files in the directory and all the files in the subdirectories under the directory will be archived. You can include only specific files in the directory by modifying the text in the *File Name* field. For example, if you want to include only the .txt files existing in a directory and all the subdirectories under the directory, enter *.txt in the *File Name* field.



To exclude a file or directory from the archive, select the file or directory in the right pane and click . The file or directory is removed from the right pane.

Archiver: Specify Archive Options

Lets you specify the options for archiving the project.

How to Access

- Click Next in the Archiver: Specify External Files dialog box.

Output Archive Path

Enter the path to the directory where you want the archive to be created, or click the browse button to select the directory.

By default, the archive is created in a directory named <projectname>_archive in the project directory. For example, if you are archiving a project named cpu.cpm located at c:\cpu\, by default, the archive will be created at c:\cpu\cpu_archive\.

Create Compressed (Zip) File

Select this check box if you want to create a compressed archive of your project.

System Connectivity Manager User Guide

Dialog Box Descriptions

Compression Utility

By default, the `cdsZip` compression utility located in the `\tools\bin` folder of your Cadence installation directory is used to create the compressed archive.

Note: The `cdsZip` compression utility creates a compressed archive file named `<projectname>_archive.zip` in the project directory. For information on extracting the compressed archive, see [Extracting a Compressed Archive](#) on page 633.

To use any other compression utility to create the compressed archive, enter the command for the utility in the *Compression Utility* field. You can use the following variables in the *Compression Utility* field:

- `$location` variable to pass the path to the archive you specified in the *Output Archive Path* field to the compression utility.
- `$archive` variable to pass the name of the compressed archive file to the compression utility.

The compressed archive file has the default name `<projectname>_archive`. For example, if you are archiving a project named `cpu.cpm` the compressed archive file will be named `cpu_archive` and will have the file extension assigned by the compression utility you are using.

For example, you can use the `tar` command using the following syntax

```
tar -cvf $archive $location  
to create a <projectname>_archive.tar file.
```

Note: If you use any other compression utility to create the compressed archive, ensure that the utility is installed on your machine and that the executable for the compression utility is in the system path.

Delete Archived Directory

Select this check box if you want the archive directory to be deleted after the compressed archive is created.

Archiver: Summary

Displays the options you selected for creating the archive.

How to Access

- Click Next in the Archiver: Specify Archive Options dialog box.

Finish	Click this button to create the archive. The progress of the archive process is displayed in the window.
Done	Click this button to close the Archiver window.

Assign Pin Number

Lets you exchange the location of two pins across two functions in a multi-function component by swapping the two pins. Swapping pins across functions lets you minimize the average net length when you route the board in Allegro PCB Editor.

How to Access

1. In the Component Connectivity Details pane, select the pin name or pin number of the pin that you want to swap with the pin in another function of the component.
2. Right-click and choose *Assign Pin Number*, then choose *More*.

Pin Name	Select the pin name of the pin that you want to swap with a pin in another section of the component.
Pin Number	Select the pin number of the pin with which you want to swap the pin you selected in the <i>Pin Name</i> field.
Function Summary	Displays the pin name, pin number and pin type of all the pins of the component.

Assign Power

Use this dialog box to change the assignment of the power and NC pins of a component. The Assign Power dialog box lets you:

- Assign a new power supply to power pins by assigning global signals in your design to the pins.
- Assign an NC pin as a power pin by specifying a power supply for the NC pin

System Connectivity Manager User Guide

Dialog Box Descriptions

- Assign a power pin as an NC pin.

How to Access

1. In the Component List select the component whose power and NC pin assignments you want to change.

Note: To change the power and NC pin assignments of more than one instance of the component simultaneously, select the instances of the component in the Component List.

2. Choose *Object – Assign Power*.

Filter Displays the instance names of the components you selected in the Component List.

Pin No. Displays the pin number of the power or NC pin.

Note: You must click the *Expand Power Pins* button to display the NC pins on the component.

Power Pins Displays the name of the power supply connected to the pin.

Power Names Displays the name of the new power supply assigned to the power pin, if any.

To assign a new power supply to a power pin, click in the *Power Names* cell next to the power pin and select a global signal in the drop-down list.

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Dialog Box Descriptions

NC Pins

Indicates whether a pin is an NC pin or a power pin.

If the *NC Pins* check box next to a pin is selected, the pin is an NC pin. If the *NC Pins* check box next to a pin is not selected, the pin is a power pin.

Note: You must click the *Expand Power Pins* button to display the NC pins on the component.

To assign an NC pin as a power pin, do the following:

1. Clear the check box next to the NC pin.
2. Click in the *Power Names* cell next to the NC pin and assign a power supply to the pin by selecting a global signal in the drop-down list.

To assign a power pin as an NC pin, do the following:

1. Select the NC Pins check box next to the power pin.

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Dialog Box Descriptions

Expand Power Pins

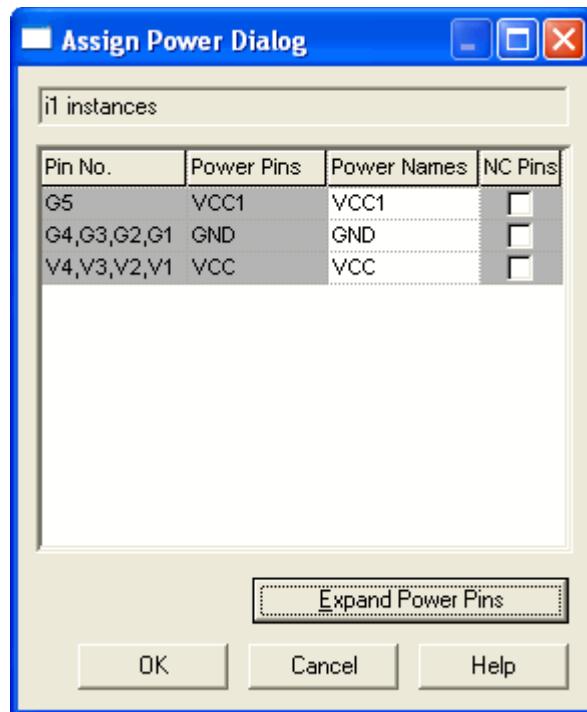
Click this button to display the power pins on the component in expanded format and to display the NC pins on the component. Displaying the power pins in expanded format lets you assign a new power supply to each pin connected to a power supply.

For example, if you have the following POWER_PINS properties in the `chips.prt` file for your component

```
POWER_PINS= ' (GND:G1..G4) ' ;
```

```
POWER_PINS= ' (VCC:V1..V4) ' ;
```

the Assign Power dialog box appears as shown below:

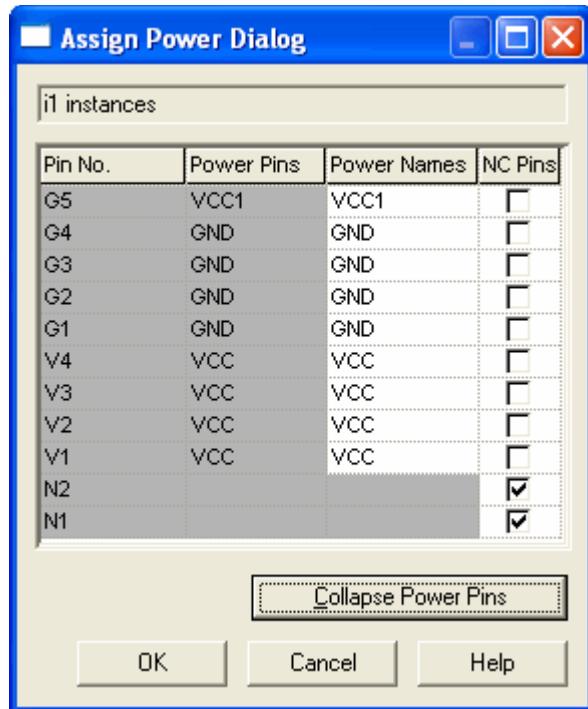


In the above example, the power supply GND is connected to the pins G1, G2, G3, and G4.

- To assign a new power supply to all the pins, click in the *Power Names* cell next to the pins and choose a global signal from the drop-down list.
- To assign a new power supply to each pin, click the *Expand Power Pins* button to display the power pins in expanded format as shown below:

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Dialog Box Descriptions



You can now assign a new power supply to each of the pins. To do this, click in the *Power Names* cell next to a pin and choose a global signal from the drop-down list.

To display the power pins in collapsed format, click the *Collapse Power Pins* button.

Assoc Comp Viewer

Lets you view the terminations, bypass capacitors, and pullups or pulldowns applied to objects (components, pins and signals) in the design.

How to Access

- Choose *View – Associated Components*

System Connectivity Manager User Guide

Dialog Box Descriptions

Bypass Caps

Select a component in the Component list (in the logical view) or the Physical Part List (in the physical view) to view the bypass capacitors added to it.

Parent	Displays the instance name of the component to which the bypass capacitor is attached.
RefDes	Displays the reference designator assigned to the bypass capacitor. You can modify the reference designator.
Value	Displays the capacitance value of the bypass capacitor.
Connectivity	
Pin	Displays the pin numbers of the bypass capacitor.
Physical Net	Displays the physical net name of the nets connected to the pins of the bypass capacitor.

Terminations

Select a pin in the Component Connectivity Details pane (in the logical view) or the Physical Part Connectivity Details pane (in the physical view) to view the terminations added on the pin.

Parent	Displays the name of the component on whose pin the termination is added.
Pin	Displays the pin number of the component on which the termination is added.
Type	Displays the type of termination added on the pin.
Connectivity	
RefDes	Displays the reference designator assigned to the component used for the termination. You can modify the reference designator.
Section	Displays the section number of the component used for the termination.
Value	Displays the value of the component used for the termination.

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Dialog Box Descriptions

Pin	Displays the pin number of the termination component to which the signal is connected.
Physical Net	Displays the physical net name for the signal connected to the pin of the termination component.

Pull-ups/Pull-downs

To view the pullups or pulldowns added on a signal, do one of the following:

- Select the signal in the Signal List (in the logical view) or the Physical Net List (in the physical view).
- Click in the Pullup/Pulldown column next to the signal (the column with the  symbol) in the Component Connectivity Details pane.

Type	Displays whether a pullup or pulldown is added to the signal.
RefDes	Displays the reference designator of the component used for the pullup or pulldown.
Section	Displays the section number of the component used for the pullup or pulldown.
Value	Displays the value of the component used for the pullup or pulldown.
Connectivity	
Pin	Displays the pin number of the component used for the pullup or pulldown.
Physical Net	Displays the physical net name for the signal connected to the component used for the pullup or pulldown.

Auto Model Assignment Details

Displays the results of running the *Auto Assign Models* command.

The *Auto Assign Models* command lets you automatically generate ESpice models for all two-pin discrete devices (resistors, capacitors, and inductors) in your design and assign the models to the discrete devices in the design. For more information on the *Auto Assign Models* command, see [Automatically Assigning Models for Discrete Devices and ICs](#) on page 330.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Choose *Tools – Signal Integrity – Auto Assign Models.*

Design Name	Displays the name of the top-level or root design.
Discretes	
Total	Displays the total number of two-pin discrete devices found in the design.
Auto Assigned	Displays the total number of discrete devices on which models were successfully assigned.
Failed	Displays the total number of discrete devices on which models could not be assigned.
ICs	Displays the number of IC components in the design on which models were automatically assigned. System Connectivity Manager automatically assign IBISDevice models to ICs in your design if the SI model libraries you have setup for your project contain an IBISDevice model that has the same name as the value of the PART_NAME property for an IC. For example, the 74ls00 component has the part name 74LS00. If you have an IBISDevice model named 74LS00 in the SI model libraries setup for your project, the model will be automatically assigned to the 74ls00 component.
Block	Displays the name of the block in which the discrete device or IC exists.
Type	Displays the type of two-pin discrete device (resistor, capacitor, or inductors) on which the model is assigned.
RefDes	Displays the reference designator of the discrete device or IC on which the model is assigned.
Value	Displays the value of the discrete device.
Status	Displays whether a model was automatically assigned to the discrete device. <ul style="list-style-type: none">■ The icon indicates that a model was successfully assigned to the discrete device.■ The icon indicates that a model could not be assigned to the discrete device.

Message	If a model was assigned to a discrete device, the name of the default model is displayed. If a model could not be assigned to a discrete device, the reason is displayed.
---------	--

Baseline Design

The Baseline Design dialog box lets you baseline the current design and all its sub-blocks. For more information on baselining designs, see [Baselining a Design](#) on page 399.

Note the following:

- You can baseline a design that is in a modified state. You cannot baseline a design that is already in a baselined state.

A design is said to be in a modified state if it was never baselined, or was modified after the last time you baselined it.
- You cannot baseline a read-only block in your design.

How to Access

- Choose *Design – Baseline Design*.

Baseline Versioning Options

Major Select this option if you want to baseline the design as a major version.

For example, if the current version number is 2 . 0, baselining the design as a major version will bump up the version number to 3 . 0.

You can baseline the design as a major version if you want to notify other designers that significant changes have been made in the design.

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Dialog Box Descriptions

Minor	<p>Select this option if you want to baseline the design as a minor version.</p> <p>For example, if the current version number is 2.0, baselining the design as a minor version will bump up the version number to 2.1.</p> <p>You can baseline the design as a minor version if you want to notify other designers that minor changes have been made in the design.</p>
Custom	<p>Select this option if you want to use a custom version number to baseline the design and enter the version number in the <i>This design will be baselined as Version</i> field.</p> <p>For example, if the current version number of the block is 2.0, the next major version will be 3.0. However, if you want to specify the next major version as 4.0, select the <i>Custom</i> option and enter 4.0 in the <i>This design will be baselined as Version</i> field.</p>
This design will be baselined as Version	<p>Displays the new version number for the design when the <i>Major</i> or <i>Minor</i> options are selected and lets you enter a custom version number when the <i>Custom</i> option is selected.</p>
Use the above information to baseline all sub-blocks	<p>Select this check box if you want to baseline all the sub-blocks used in the current design. For more information on how the version number of a sub-block changes when you baseline the top-level design, see How Version Numbers of Sub-Blocks Change When You Baseline a Design on page 689.</p> <p>Note the following:</p> <ul style="list-style-type: none">■ A sub-block that is in a modified state will be baselined when the top-level design is baselined. However, a sub-block that is already in a baselined state will not be baselined again when the top-level design is baselined. A sub-block is said to be in a modified state if it was never baselined, or was modified after the last time you baselined it.■ A sub-block that is a read-only block will not be baselined when the top-level design is baselined.
Baseline Comments	Enter the comments for baselining the design.

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Dialog Box Descriptions

How Version Numbers of Sub-Blocks Change When You Baseline a Design

The following table describes how the version number of a sub-block changes if the *Use the above information to baseline all sub-blocks* check box is selected. Please see the footnotes to the table to understand how the new version number for the top-level design impacts the version number of its sub-blocks.

Existing Version of Top-Level Design	Existing Version of Sub-Block	New Version of Top-Level Design	New Version of Sub-Block
2.0	1.0	3.0 ¹	2.0 ²
2.0	4.0	3.0 ³	5.0 ⁴
2.0	1.0	2.1 ⁵	1.1 ⁶
2.0	1.0	4.0 ⁷	4.0 ⁸
2.0	5.0	5.0 ⁹	ERROR ¹⁰

1. Major version change when Major option is selected.
2. Version of sub-block increments by 1 as the Major option is selected.
3. Major version change when Major option is selected.
4. Version of sub-block increments by 1 as Major option is selected.
5. Minor version change when Minor option is selected.
6. Version of sub-block increments by 0.1 as Minor option is selected.
7. Major version change using Custom option.
8. Version of sub-block increments to 4.0 as Custom option is selected.
9. Major version change using Custom option.
10. You cannot baseline the sub-blocks in the design if the current version number of the sub-block is the same as the new version number of the top-level design specified using the Custom option. In this example, you need to specify the custom version number 5.1 or above for the top-level design if you want to baseline all its sub-blocks.

Block Packaging Options

This dialog box lets you specify the options for packaging a block in your design and to alias or mask global signals in the block. For more information on working with blocks, see [Chapter 13, “Working with Hierarchical Designs.”](#)

How to Access

This dialog box appears when you:

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Dialog Box Descriptions

- Create a block and add it in your design.
- Add a block in your design.
- Copy a block in the Component List and paste it.
- Select a block in the Component List, and choose *Object – Block Packaging Options*.

Packaging options for the added block Lets you specify the prefix, suffix, and range options for controlling the value of the reference designators for instances in the block.

These options help you:

- Avoid packaging errors by ensuring that the same reference designator is not assigned to packages in different blocks.
- Easily identify the block in which a component having a specific reference designator exists. This is helpful when you are debugging the design with respect to the board as you can trace back parts on the board to a specific block in System Connectivity Manager.

For example, if you have a hierarchical design named `MEMORY` with two blocks named `ROM` and `CONTROLLER`, you can assign the suffix `ROM` to the reference designators of all components in the `ROM` block and the suffix `CNTR` to the reference designators of all the components in the `CONTROLLER` block. The reference designators of components in the `ROM` block will be `U1_ROM`, `U2_ROM`, and so on. The reference designators of components in the `CONTROLLER` block will be `U1_CNTR`, `U2_CNTR`, and so on. This ensures that the same reference designator is not assigned to packages in different blocks and helps you debug the design with respect to the board layout because you can easily identify the block in which a component having a specific reference designator exists.

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Dialog Box Descriptions

Use Suffix	<p>Select this option and enter the unique suffix to be used for reference designators of components in the block.</p> <p>For example, if you specify the suffix CNTR for a block named CONTROLLER, the reference designators of components in the CONTROLLLER block will be U1_CNTR, U2_CNTR, and so on.</p> <p>Note: By default, the underscore character (_) is used as the suffix separator. You can specify the default suffix separator to be used in the <u>Packager</u> tab of the <u>Setup</u> dialog box.</p> <p>Note: The same suffix should not be used for other blocks in the design.</p>
Use Prefix	<p>Select this option and enter the unique prefix to be used for reference designators of components in the block.</p> <p>For example, if you specify the prefix CNTR for a block named CONTROLLER, the reference designators of components in the CONTROLLLER block will be CNTR_U1, CNTR_U2, and so on.</p> <p>Note: By default, the underscore character (_) is used as the prefix separator. You can specify the default prefix separator to be used in the <u>Packager</u> tab of the <u>Setup</u> dialog box.</p> <p>Note: The same prefix should not be used for other blocks in the design.</p>
Use Ref. Des. Range	<p>Select this option and enter the range of reference designators to be used for components in the block or to modify the reference designator range that was specified when the block was created.</p> <p>For example, if you specify the reference designator range 1 to 100 for a block named ROM and the reference designator range 101 to 200 for a block named CACHE, the reference designators of components in the ROM block will start from, say, U1 and go up to U100. You cannot have a component with the reference designator U105 in the ROM block.</p> <p>Note: The same reference designator range should not be used for other blocks in the design.</p>

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Dialog Box Descriptions

Minimum Range Width Required	<p>Displays the minimum width for the reference designator range you must specify in the <i>Use Ref. Des. Range</i> field.</p> <p>For example, if the block has 12 components, the minimum range width required will be 12. This means that you must specify a reference designator range that has a width of 12, say 101 to 112 in the <i>Use Ref. Des. Range</i> field.</p>
Range Specified in Block	<p>Displays the reference designator range that was specified when the block was created.</p> <p>For more information on creating blocks in System Connectivity Manager, see Creating Blocks on page 339.</p>
Use Optimized Packaging	Preserves the reference designators of components in the block.
Physically Reuse Block	<p>This check box is selected by default if the block you are adding in the design is a reuse block. For more information on working with reuse blocks, see Chapter 17, “Design Reuse.”</p> <p>Clear this check box if you do not want to add the block as a reuse block.</p>
Reuse Instance Name	<p>Specifies the unique ID for the instance of the reuse block in your design. Allegro PCB Editor uses this ID to differentiate between multiple instances of a reuse module.</p> <p>By default, System Connectivity Manager assigns <code><reuse_block_name>_<number></code> as the reuse instance name. For example, the first instance of a reuse block named <code>BASE</code> you add in your design will be assigned the reuse instance name <code>BASE_1</code>. The second instance will be assigned the reuse instance name <code>BASE_2</code>, and so on. You can specify a different reuse instance name.</p> <p>System Connectivity Manager adds the <code>REUSE_INSTANCE</code> property on the instance of the reuse block.</p>

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Dialog Box Descriptions

Increment Values for Remaining Instances By	This check box and the corresponding spin box is activated if you simultaneously instantiate multiple instances of a logical block in a design, and select the <i>Use Suffix</i> or <i>Use Prefix</i> as the packaging options. This option is not available if <i>Use Ref. Des. Range</i> or <i>Use Optimized Packaging</i> are selected as packaging options.
	Select this check box if you want unique reference designators to be generated by incrementing the letter, numeral, or alphanumeric value, specified by you in the <i>Use Suffix</i> or <i>Use Prefix</i> text boxes. The reference designator values are incremented by the value entered in the spin box. To know more about how incremental suffix or prefix values are generated, see the section on Calculating incremental suffix values on page 367.
Globals	Click this button if you want to alias a global signal in the block to a signal in the design in which you are adding the block. The left column displays all the global signals in the block you are adding. Click in the right column next to each global signal to select the signal in the design (in which you are adding the block) to which you want to alias the global signal. By default, the right column displays only the global signals in the design in which you are adding the block. This lets you alias a global signal in the block (you are adding) to a global signal in the design in which you are adding the block. Select the <i>Use Local Nets for Global Masking</i> check box if you want to alias a global signal in the block (you are adding) to a local signal in the design in which you are adding the block. If you select the <i>Use Local Nets for Global Masking</i> check box, the right column displays all the local and global signals in the design in which you are adding the block. Note: If you select or clear the <i>Use Local Nets for Global Masking</i> check box, the global signal alias changes you made after opening the <i>Block Packaging Options</i> dialog box will be lost. For more information, see Aliasing and Masking Global Signals in Hierarchical Designs on page 376.

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Dialog Box Descriptions

Apply This button is activated if you use the Block Packaging Options dialog box for specifying packaging options for a single logical block.

Apply All This button is activated when you use the Block Packaging Options dialog box for specifying packaging options for multiple logical blocks simultaneously.

This happens when you simultaneously instantiate multiple instances of a logical block in your design.



For any scenario, either the Apply button or the Apply All button will be activated.

Block Save As

Lets you save a copy of a block you are editing in the master mode. For more information on editing blocks, see [Editing a Hierarchical Design](#) on page 356.

Note: You cannot save a copy of block of type schematic.

How to Access

- Choose *File – Save As*.

Block Name Enter the name for the copy of the block.

Block Library Select the library in which you want to save the new block.

Implementation Displays the implementation type of the block. The implementation type can be Spreadsheet or Verilog.

You cannot modify the implementation type.

Cadence Product Choices

Use this dialog box to choose a product suite from which you want to run System Connectivity Manager. All the product suites, for which you have licenses, and from which you can launch System Connectivity Manager, are listed in the Cadence Product Choices dialog box.

How to Access

The Cadence Product Choices dialog box is opened when:

- you are using the tool for the first time; and on all subsequent invocations unless you specify the default choice.
- you choose *File – Change Product*.

Setting a Default Product Choice

To prevent the Cadence Product Choices dialog box from appearing every time you run System Connectivity Manager, complete the following steps.

1. Select the product suite to be used as the default choice.
2. Select the *Use as Default* check box.
3. Click *OK*.

System Connectivity Manager is launched from the specified product suite. Selecting the *Use as Default* check box writes the product choice in registry. As a result, for all future invocations, the tool will open with this product suite unless you change the default setting.

To change the default product suite, open the Cadence Product Choices dialog box from System Connectivity Manager by selecting *File – Change Product*, and select the required product suite.

Specifying Product Choice from Command Line

If you open System Connectivity Manager from the command line, you can use the `-product` option to prevent the Cadence Product Choices dialog box from appearing every time.

The syntax for using this option is

```
scm -product "license_string"
```

The possible values of `license_string` for System Connectivity Manager are:

- Allegro Design Authoring with Design Authoring Hlgh Speed option and Design Authoring Mutli-Style Option
- Cadence SiP Digital Architect GXL
- Cadence SiP Digital Architect XL

System Connectivity Manager User Guide

Dialog Box Descriptions

Therefore, command line for invoking System Connectivity Manager from Allegro System Architect GXL, is `scm -product "Allegro System Architect GXL"`

Disabling License Check

To ensure that only the product suites for which you have licenses available, are displayed in the Cadence Product Choices dialog box, the application checks with the license server for available licenses. The process of populating the dialog box with the list of available licenses takes some time.

However, if the time taken for displaying the Cadence Product Choices dialog box is high, you can use the `CDS_IGNORE_LIC_FEATURE` environment variable, with its value set to TRUE, to disable the procedure of checking for the available licenses. Using this variable ensures that the dialog box appears instantly, but displays all the licenses using which you can launch System Connectivity Manager. From the list, you need to select the product suite for which you have the license available. For information on the available licenses, contact your license administrator.

Cell Revision Manager

Lets you update all the instances of the component used in the design with the latest version of the component in the component library.

How to Access

Do one of the following:

- Choose *Project – Validate Revisions*.
- Reopen the design in System Connectivity Manager.

The Cell Revision Manager dialog box appears if System Connectivity Manager finds any differences between the version of a component used in the design and the version of the component in the component library.

Cell	Displays the name of the component that has changed.
-------------	--

Revision	Displays the new version number of the component.
-----------------	---

System Connectivity Manager User Guide

Dialog Box Descriptions

Cell Info	<p>Displays the type of change in the component as a Major Change, Minor Change or Save Version.</p> <p>For example, if the component version changes from 1.1.0 to 2.0.0, the change is a Major Change. If the component version changes from 1.1.0 to 1.2.0, the change is a Minor Change. If the component version changes from 1.1.0 to 1.1.1, the change is displayed as Save Version.</p> <p>A component change that impacts the design flow is considered a major change. All other changes are considered as minor changes. For more information on the type of changes that constitute major and minor changes, see the <i>Part Logging and Versioning</i> chapter of the <i>Part Developer User Guide</i>.</p>
Update	<p>Select this check box if you want to replace all instances of the component in your design with the modified component.</p> <p>Note: You can only update all the instances of the component used in the design with the latest version of the component. You cannot update specific instances of a component used in the design with the latest version of the component.</p>
	<p> <i>Tip</i></p> <p>If you want to update a specific instance of a component used in the design with the latest version of the component, you must modify or replace the instance of the component with the latest version of the component. For more information on modifying a component, see Modifying Components on page 109. For more information on replacing components, see Replacing Components on page 110.</p>
Details	Select a component whose version has changed and click this button to view the instances of the component in the design.
Instance	Displays the instance number of the component used in the design.
Design	Displays the name of the design or block in which the instance of the component is used.
Version	Displays the version of the component used in the design.

Change Root

Lets you change the design opened in the Master mode. Use this dialog box to specify the cell to be opened in the master mode.

How to Access

- Choose *Project – Change Root*.
- In the *Hierarchy Viewer*, click the *Change Root* () button.

Library

Click the drop-down list to select the library that contains the block you want to open in master mode.

Cell

Select the block you want to open.

View

Displays the type of the block.

If the block is a Spreadsheet block, the *Table* option is selected.
If the block is a Verilog block, the *Verilog* option is selected.

Clipboard

Use this window to quickly paste any of the last 12 recorded actions.

How to Access

- Choose *Edit – Clipboard*.

Function

System Connectivity Manager records the data you copied in any application. Using the Clipboard you can quickly paste the copied data in System Connectivity Manager.

Clear All

Select this button to clear the Clipboard buffer.

System Connectivity Manager User Guide

Dialog Box Descriptions

- Click an item to paste** Select an individual action by clicking the drop-down button. A submenu with three commands appears:
- **Paste**—Click this command to paste the selected item in the cell selected in System Connectivity Manager. For example, if you select a cell in the *Signal* column in the Component Connectivity Details pane and click on an item in the clipboard, the data is pasted in the *Signal* column.
 - **Paste Special**—Click this command to use the paste special function to paste the data in the clipboard. For more information on using paste special, see the following topics:
 - [Using Paste Special to Paste Components](#) on page 127.
 - [Using Paste Special in the Signal List](#) on page 158.
 - [Using Paste Special in the Component Connectivity Details Pane](#) on page 159.
 - **Delete**—Click this command to remove the selected item from the Clipboard buffer.

Column Definition

Lets you add a column for displaying property values in the Component List, Signal List, Component Connectivity Details pane, Signal Connectivity Details pane, Matrix Connectivity View pane, Physical Part List, Physical Net List, Physical Part Connectivity Details pane, and the Physical Net Connectivity Details pane.

How to Access

- Click *Add New* in the [Customize Pane \[<name of pane>\]](#) dialog box.

Property Owner Select the object for which you want to display the list of properties in the *Property Name* field.

For example, select **Component** if you want to add a column for a component property. Component properties are displayed in the *Property Name* field.

Property Name Select the property for which you want to add a column.

System Connectivity Manager User Guide

Dialog Box Descriptions

Display Name	Displays the column heading name that will be used for the selected column.
Column Width	Enter the width to be used for displaying the column.

Comments

Use this dialog box to add or edit comments for the selected object.

How to Access

Do one of the following:

- Choose *Object – Comments – Insert Comments*.
- Double-click in the *Comments* column in the Component Connectivity Details pane.
- Select a component, signal or pin that has a comment added on it and choose *Object – Comments – Edit Comments*.

Component Replace

Use this dialog box to manually resolve discrepancies in connectivity and property information before replacing a component.

How to Access

Do the following:

1. Select the component you want to replace in the Component List or the Associated Component Viewer.
2. Choose *Object – Replace Component*.
Part Information Manager appears.
3. Select the component you want to use to replace the component in the design.
4. Click *Replace*.

This dialog box appears if any of the component replace preserve options you selected in the Replace Component tab of the Setup dialog box will not be honored when you replace a component.

Connectivity

Lets you map a pin on the existing component to a pin on the target component. When you map a pin on the existing component to a pin on the target component, the signals that are connected to the pin of the existing component are automatically connected to the pin on the target component when you replace the existing component with the target component.

Existing Component	Displays the name of the library, cell and view of the existing component in the following format: <code><library_name>. <cell_name> : <view_name></code>
Pin Name	Displays the pin names of the existing component.
Pin Type	Displays the pin type.
Pin Number	Displays the pin number.
Signal	Displays the name of the signal connected to a pin of the existing component.
Target Component	Displays the name of the library, cell and view of the target component in the following format: <code><library_name>. <cell_name> : <view_name></code>
Pin Name	Displays the pin names of the target component.
Pin Type	Displays the pin type.
Pin Number	Displays the pin number.
Signal	Displays the name of the signal that will be connected to a pin of the target component. You can also click on the <i>Signal</i> column next to a pin and select the signal you want to be connected to the pin.
Match with Pin Names	Select this check box if you want to automatically map a pin on the existing component that is connected to a signal, to a pin on the target component, if the pin name of the pin on the existing component and the pin name of the pin on the target component are the same. For example, assume that a pin named <code>shift</code> on the existing component is connected to a signal named <code>data</code> . If the target component has a pin with the name <code>shift</code> , both the pins are automatically mapped and displayed on the right side of the window. Note: If you deselect this check box, all the pin mappings are lost.

System Connectivity Manager User Guide

Dialog Box Descriptions

Match with Pin Numbers	Select this check box if you want to automatically map a pin on the existing component that is connected to a signal, to a pin on the target component, if the pin number of the pin on the existing component and the pin number of the pin on the target component are the same. For example, assume that a pin named <code>shift</code> with the pin number 23 on the existing component is connected to a signal named <code>data</code> . If the target component has a pin with the name <code>hold</code> and with the pin number 23, both the pins are automatically mapped and displayed on the right side of the window. Note: If you deselect this check box, all the pin mappings are lost. Note: Select both the Match with Pin Names and Match with Pin Numbers check boxes, if you want to automatically map a pin on the existing component that is connected to a signal, to a pin on the target component, if both the pin name and pin number of the pin on the existing component and the pin name and pin number of the pin on the target component are the same. For example, assume that a pin named <code>shift</code> with the pin number 23 on the existing component is connected to a signal named <code>data</code> . If the target component has a pin with the name <code>shift</code> and with the pin number 23, both the pins are automatically mapped and displayed on the right side of the window.
Map and Unmap	Select a pin in the connectivity information for the existing component, then select a pin in the connectivity information for the target component and click the <i>Map</i> button to map the pin on the existing component to the pin on the target component. When you map a pin on the existing component to a pin on the target component, the signals that are connected to the pin of the existing component are automatically connected to the pin on the target component when you replace the existing component with the target component. Select a mapped row on the right side of the window and click the <i>Unmap</i> button to remove the pin mapping.
Source Pin Name	Displays the name of the pin on the existing component.
Source Pin Number	Displays the number of the pin on the existing component.
Target Pin Name	Displays the name of the pin on the target component to which the signal connected to the pin on the existing component, if any, will be connected when you replace the component.

System Connectivity Manager User Guide

Dialog Box Descriptions

Target Pin Number	Displays the number of the pin on the target component to which the signal connected to the pin on the existing component, if any, will be connected when you replace the component.
Target Pin Type	Displays the type of the pin on the target component.
Signal	Displays the name of the signal that will be connected to the pin of the target component when you replace the component.
Replace	Click this button to save the changes and display the <u>Replace Component</u> dialog box.

Properties

Existing Component	Displays the name of the library, cell and view of the existing component in the following format: <library_name>. <cell_name> : <view_name>
Property Name	Displays the properties on the existing component.
Type	Displays the origin of the property on the existing component. For more information, see <u>Viewing the Origin of a Property in System Connectivity Manager</u> on page 260
Value	Displays the value of a property on the existing component.
Selected Component to Replace	Displays the name of the library, cell and view of the target component in the following format: <library_name>. <cell_name> : <view_name>
Property Name	Displays the properties on the target component.
Type	Displays the origin of the property on the target component. For more information, see <u>Viewing the Origin of a Property in System Connectivity Manager</u> on page 260
Value	Displays the value of a property on the target component.

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Dialog Box Descriptions

Map	The rows for the properties that can be added from the existing component to the target component are displayed in white color. The rows for the properties that cannot be added from the existing component to the target component are displayed in gray color.
	Select a property that can be added from the existing component to the target component and click this button to add the property on the target component.
Unmap	In the property information column for the target component, select a property you added from the existing component to the target component and click this button to remove the property from the target component.
Replace	Click this button to save the changes and display the <u>Replace Component</u> dialog box.

Create Block

Use this dialog box to create a new Spreadsheet, or schematic block in any library. For more information on working with blocks, see [Working with Hierarchical Designs](#) on page 337.

How to Access

Do one of the following:

- Choose *Project – Create Block*.

Use the *Project – Create Block* option if you want to create blocks without instantiating them in the current design. This option is usually used when you are creating a hierarchical design using bottom-up methodology. Using this approach, the block is saved in the specified library and can later be instantiated in the design.

- Click  on the toolbar.
- Choose *Design – Create Block*.

The *Design – Create Block* option is used when you want to create a block and instantiate it in the current design. This option is useful when you are create a hierarchical design using top-down methodology.

Block Name	Enter the name of the block.
Block Library	Select the library in which you want to create the block.

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Dialog Box Descriptions

Implementation	Select the implementation type of the block. You can select from Spreadsheet, or Schematic.
	<p>If you create a block of:</p> <ul style="list-style-type: none">■ Spreadsheet type, the design for the block is stored in the <code>tbl_1</code> view of the cell for the block in the design library.■ Schematic type, the schematic for the block is stored in the <code>sch_1</code> view of the cell for the block in the design library.
Inherit global signals from root design	<p>Select this check box if you want all the global signals in the root design to be automatically added in the new block.</p> <ol style="list-style-type: none">1. Click <i>Edit</i> if you want to select the list of global signals in the root design that have to be added in the new block. The Global Signals dialog box appears displaying the list of global signals in the root design.2. Clear the check box next to the global signals that you do not want to be added in the new block, and click <i>OK</i>. <p>Note: The <i>Inherit global signals from root design</i> check box is not available when you choose <i>Create Block</i> from the <i>Project</i> menu.</p>
Ref Des range	<p>Select this option and enter the range of reference designators to be used for components in the block.</p> <p>For example, if you specify the reference designator range 1 to 100 for a block named ROM and the reference designator range 101 to 200 for a block named CACHE, the reference designators of components in the ROM block will start from, say, U1 and go up to U100. You cannot have a component with the reference designator U105 in the ROM block.</p> <p>Note: The same reference designator range should not be used for other blocks in the design.</p>

System Connectivity Manager User Guide

Dialog Box Descriptions

Add Ports

Click this button to define the ports or interface signals for the block.

Available Signals: Displays the signals in the root design.

Note: The Available Signals list is displayed only when you creating a block for adding it in your design by choosing *Design – Create Block*. For more information, see [Creating a Block and Adding it in the Current Design](#) on page 341.

Add: Select signals from the *Available Signals* list and click this button to add the selected signals in the ports list.

Port Name: Lists the selected signals you defined as ports. You can add new signals to define the ports by entering the signal names in the Port Name list.

Port Type: Click the drop-down list to select the port type for each port name. Available values are `IN`, `OUT` or `INOUT`.

You can right-click and do the following:

- **Add Port**—Displays the Add Port dialog box where you can define a new interface port. Click *OK* to add the port in the port list.
- **Delete**—Deletes the selected port from the port list.
- **Modify Type**—Displays `IN`, `OUT` or `INOUT` as available port types. You can change the value.
- **Copy**—Copies the selected port name and port type to the Clipboard.
- **Paste**—Creates a new port in the port list using the port name and port type saved in the Clipboard.
- **Pick From List**—Allows you to quickly choose a port name from the available port names in the port list.

System Connectivity Manager User Guide

Dialog Box Descriptions

Add instance to design	<p>Select this check box to add the block being created as an instance in the current design. When you click <i>OK</i> the <u>Block Packaging Options</u> dialog box appears. Use this dialog box to define how the new block should be packaged in the design.</p> <p>If you do not select the <i>Add instance to design</i> check box, the new block is added to the library but is not instantiated in the current design.</p> <p>Note: The <i>Add instance to design</i> check box is not available when you choose <i>Create Block</i> from the <i>Project</i> menu. You can add the block in your design using Part Information Manager.</p>
Edit Connectivity	Select this check box to open a new tab for the block being created. You can use this tab to define connectivity for the block.

Create Report Template

How to Access

- Choose *Project – Reports – Create Template*.
- Click the *Create New* button in the Generate Report dialog box.

Report Name	Enter the name of the report.
Structure	
Design Based	Select this option if you want the report to be created for the entire design.
Block Based	Select this option if you want the report to be sorted by blocks in the design.
Title Page	<p>Specify the file that contains the content you want to use as title page for the report.</p> <p>Enter the name and path to the file or click the browse button to select the file.</p> <p>You can use a text (.txt) file or a Editable Report Format (.dsr) file as the title page for the report.</p>

System Connectivity Manager User Guide

Dialog Box Descriptions

Display RefDes as Range Select this check box if you want to display the range of reference designators in the report, instead of displaying individual reference designators.

For example, if your design has four components with the reference designators D1, D2, D3, and D4, the report displays the reference designators in four rows (one row for each reference designator). If you select this check box, the report displays the reference designators in a single row with the range:

D1–D4

If your design has eight components with the reference designators D1, D2, D3, D5, D6, D7, D10, and D11, the report displays the reference designators in seven rows (one row for each reference designator). If you select this check box, the report displays the reference designators in a single row with the range:

D1–D3, D5–D7, D10, D11

Note: Only the reference designators of components that have the same information in other columns in the report will be displayed as a range. For example, if your design has four components with the reference designators D1, D2, D3 and D4 and if the pin count of D1, D2, D3 is 64, but the pin count of D4 is 32, the report displays the reference designator range D1–D3 in a single row because these components have the same pin count, and displays the reference designator D4 in a separate row.

System Connectivity Manager User Guide

Dialog Box Descriptions

Display Pin Number as Range	<p>Select this check box if you want to display the range of pin numbers in the report, instead of displaying individual pin numbers.</p> <p>For example, if a component in your design has four pins with the numbers 1, 2, 3, and 4, the report displays the pin numbers in four rows (one row for each pin number). If you select this check box, the report displays the pin numbers in a single row with the range:</p> <p style="margin-left: 40px;">1–4</p> <p>If a component has five pins with the pin numbers 1, 2, 3, 6, and 7, the report displays the pin numbers in five rows (one row for each pin numbers). If you select this check box, the report displays the pin numbers in a single row with the range:</p> <p style="margin-left: 40px;">1–3, 6, 7</p> <p>Note: Only the pin numbers of a component that have the same information in other columns in the report will be displayed as a range. For example, if component has four pins with the numbers 1, 2, 3 and 4 and if the pins with the numbers 1, 2, 3 are connected to a signal named CBDATA, but the pin with the number 4 is connected to a signal named ADDRESS, the report displays the pin number range 1–3 in a single row because these pins connect to the same signal CBDATA, and displays the pin number 4 in a separate row.</p>
Remove Row if any Cell is Empty	Select this check box if you want a row in the report to be automatically deleted if any cell in that row is empty.
Remove Row if all Cells are Empty	Select this check box if you want a row in the report to be automatically deleted if all the cells in that row are empty.

System Connectivity Manager User Guide

Dialog Box Descriptions

- Duplicate Cell Values Select this check box if you want duplicate values to be displayed in a column in the report.
- For example, the following report displays the pin names of a component with the reference designator D1.
- If you select this check box, the reference designator D1 is duplicated in the *Ref Des* column in the report.

	Ref Des	Pin Name
1	D1	a<0>
2	D1	b<0>
3	D1	y*<0>

If you do not select this check box, the reference designator D1 is displayed only once in the *Ref Des* column in the report.

	Ref Des	Pin Name
1	D1	a<0>
2		b<0>
3		y*<0>

- Standard Query Fields Displays the fields that can be used to generate data for the report. These fields can be added as keywords in the report.
- The driver keywords are displayed in bold blue letters in the *Standard Query Fields* list. For more information on driver keywords, see [Adding a Keyword in the Query Grid](#) on page 511.
- For more information on the standard query fields, see [Standard Query Fields](#) on page 517.
- User Defined Fields Displays the user-defined query fields that can be used to generate data for the report. These fields can be added as keywords in the report.
- For more information on creating user-defined query fields, see [Creating User-Defined Query Fields](#) on page 523.
- Edit Field Select a user-defined query field in the *User Defined Fields* list and click this button to edit the field using the [User Defined Query Field](#) dialog box.

System Connectivity Manager User Guide

Dialog Box Descriptions

Create New Field	Click this button to create a new user-defined query field using the User Defined Query Field dialog box.
Query Grid	The keywords in the query grid, and the query and format settings for each keyword in the query grid determine how data will be displayed in your report. You can add the standard and user-defined query fields as keywords in the query grid.
Query	Displays the query settings for the keywords in the report.
Keyword	Add keywords in the query grid. You must add one driver keyword that does not have a dependency. For more information, see Adding a Keyword in the Query Grid on page 511.
Dependency	Specify the dependency for every keyword you add in the query grid, except the driver keyword. For more information, see Specifying the Dependency for a Keyword on page 513.
Qualifier	Specify the qualifier for the keywords for which you want to limit the query to a specific value or a set of values. For more information, see Specifying the Qualifier for a Keyword on page 514.
Qualifier Value	Specify the qualifier value for each qualifier. For more information, see Specifying the Qualifier for a Keyword on page 514.
Total	Lets you display the total of the data for the column in the report. Select this check box in the column for a keyword if you want the total count for the keyword to be displayed in the report. The total number of objects found for the keyword is displayed in the bottom of the report. The heading for the row in the report where the total count is displayed is named TOTAL .
Format	Displays the format settings for the keywords in the report. The format settings determine how data is displayed in the report.

System Connectivity Manager User Guide

Dialog Box Descriptions

Title	<p>The default title for each keyword is displayed in the <i>Title</i> cell in the column for each keyword. The title for a keyword is used as the column name for the keyword in the report. You can modify the title for a keyword.</p> <p>You can also enter the name of another keyword you have added in the query grid as %keyword_name% as the title for the keyword to generate a cross-tab report. For more information, see Generating a Cross-tab Report on page 514.</p>
View Order	<p>Specify the view order for the keywords in the <i>View Order</i> row.</p> <p>The <i>View Order</i> row displays the order in which the columns for the keywords are displayed in the report. The keyword whose view order is 1 is displayed as the first column in the report, the keyword whose view order is 2 is displayed as the second column in the report, and so on.</p> <p>You can modify the view order of the keywords.</p>
Sort Order	<p>Specify the sort order for the keywords in the <i>Sort Order</i> row.</p> <p>The <i>Sort Order</i> row displays the order in which the data in the columns in the report are sorted. The data in the columns in the report will be first sorted by the keyword whose sort order is 1, then by the keyword whose sort order is 2, and so on.</p> <p>You can modify the sort order of the keywords.</p> <p>Note: The sort order must be a continuous sequence starting with 1.</p>
Width	<p>Specify the width for the keywords in the <i>Width</i> row.</p> <p>The <i>Width</i> row displays the width that will be used for displaying the column for each keyword in the report. The default width is 20 characters.</p>
Alignment	<p>Specify the alignment for the keywords in the <i>Alignment</i> row.</p> <p>The <i>Alignment</i> row displays how the text in the column for each keyword will be aligned in the report. The default alignment is LEFT.</p> <p>To modify the alignment for a keyword, click on the alignment cell in the column for the keyword, and choose the alignment type from the drop-down list.</p>

System Connectivity Manager User Guide

Dialog Box Descriptions

Visible	Select this check box if you want the column for the keyword to be displayed in the report. Clear this check box if you do not want the column for the keyword to be displayed in the report.
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Create Sub-Project

When you are creating a hierarchical design in a team design environment, each designer in the design team has to create a project for the blocks assigned to him. This requires that the projects created by every designer must have the same settings. For example, all the projects must have the same packaging options, use the same list of component libraries, signal integrity model libraries, part table files, and so on.

The Create Sub-Project dialog box lets you specify the project settings in the project containing the top-level or root design for the hierarchical design and then create sub-projects for each block in the hierarchical design. The sub-projects will have the same project settings as that of the project containing the top-level design.

How to Access

- Choose *Project – Create Sub-Project*.

Block Name Enter the name of the block for which you want to create the sub-project.

The block will be set as the top-level or root design for the sub-project.

Block Library Enter the name of the library in which you want the block to be created in the sub-project.

The library will be set as the working library for the sub-project.

Implementation Select the implementation type of the block. You can select from Spreadsheet, or Schematic.

If you create a block of:

- Spreadsheet type, the design for the block is stored in the `tbl_1` view of the cell for the block in the design library.
- Schematic type, the schematic for the block is stored in the `sch_1` view of the cell for the block in the design library.

Project Name Enter the name for the sub-project.

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Dialog Box Descriptions

Project Location	Type the path to the directory in which you want to create the sub-project, or click the browse button to select the directory in which you want to create the sub-project.
Add Ports	<p>Click this button to define the ports or interface signals for the block.</p> <p>Port Name: Enter the port names in this column.</p> <p>Port Type: Click the drop-down list to select the port type for each port name. Available values are <code>IN</code>, <code>OUT</code> and <code>INOUT</code>.</p> <p>You can right-click and do the following:</p> <ul style="list-style-type: none">■ Add Port—Displays the Add Port dialog box where you can define a new port. Click <i>OK</i> to add the port in the port list.■ Delete—Deletes the selected port from the port list.■ Modify Type—Displays <code>IN</code>, <code>OUT</code> and <code>INOUT</code> as available port types. You can change the port type.■ Cut—Deletes the selected port name and port type and copies the information to the clipboard.■ Copy—Copies the selected port name and port type to the clipboard.■ Paste—Creates a new port in the port list using the port name and port type saved in the Clipboard.■ Pick From List—Allows you to quickly choose a port name from the available port names in the port list.

Create Matrix View

Use this dialog box to create a Matrix View for displaying design connectivity.

How to Access

- Choose *Table – Matrix View – Create*.

Temporary View	Select this option to create a matrix view temporarily for the current session of System Connectivity Manager. This view is not available once you exit the tool.
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System Connectivity Manager User Guide

Dialog Box Descriptions

Permanent View	Select this option to create a matrix view that is saved along with the design files. A permanent view is available every time you open the design in System Connectivity Manager.
	When you select this option, the corresponding text box is enabled. Use this text box to specify the name of the permanent view.
Components tab	Allows you to specify the components to be added in the Matrix View.
Available Objects	Lists all the components used in the design.
Selected Objects	Lists the components to be displayed in the Matrix Connectivity view
Signals tab	Allows you to specify the signals to be added to the Matrix Connectivity View.
Available Objects	Lists all the signals available in the design.
Selected Objects	Lists the signals for which connectivity information is displayed in the Matrix View.
Add	Select this button to move the selected object from the Available Objects list to Selected Objects list.
Add All	Select this button to move all the objects in the Available Objects list to Selected Objects list.
Remove	Select this button to move the selected object from the Selected Objects list to the Available Objects list.
Add All	Select this button to move all the objects in the Selected Objects list to the Available Objects list.
Up	Use these buttons to specify the position of a selected object in Selected Objects list.
Down	The sequence in which Signals or Components are displayed in the Matrix view matches the sequence in which the objects are listed in the Selected Objects List.

Customize

Lets you show and hide toolbars, create your own custom toolbars, and add buttons to toolbars.

How to Access

- Choose *Tools – Customize*, then select the *Toolbars* tab.

Toolbars

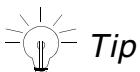
This tab lets you show and hide toolbars and create your own custom toolbars in System Connectivity Manager.

Toolbars	<p>Lists the available toolbars in System Connectivity Manager.</p> <ul style="list-style-type: none">■ Select the check box next to a toolbar to display the toolbar in System Connectivity Manager.■ Clear the check box next to a toolbar to hide the toolbar.
Show Tooltips	<p>Select this check box if you want System Connectivity Manager to display tooltips for the buttons in toolbars.</p> <p>Note: To view the tooltip for a button, hover the cursor over the button.</p>
Cool Look	<p>Select this check box to display the buttons in toolbars in the cool look mode.</p>
Large Buttons	<p>Select this check box to display larger size buttons in toolbars.</p>
New	<p>Click this button to create a custom toolbar. Specify the name of the toolbar in the <i>New Toolbar</i> dialog box and click <i>OK</i>.</p> <p>System Connectivity Manager creates a new toolbar with the name you specified in the top left corner of the window. You can select the <u>Commands</u> tab and drag and drop buttons from the <u>Commands</u> tab to the new toolbar.</p> <p>Note: If you create another new toolbar, System Connectivity Manager places the second toolbar over the first one.</p>

System Connectivity Manager User Guide

Dialog Box Descriptions

Reset	<p>Click this button to reset the selected built-in toolbar (a toolbar provided with System Connectivity Manager) to its original setting. For example, if you had added or removed buttons in a built-in toolbar, clicking <i>Reset</i> will remove the buttons you had added and restore the buttons you had deleted from the built-in toolbar.</p> <p>If you select a custom toolbar, the <i>Reset</i> button changes to <i>Delete</i>. To delete a custom toolbar, select the toolbar and click <i>Delete</i>.</p> <p>Note: You cannot delete the built-in toolbars in System Connectivity Manager.</p>
Toolbar Name	Displays the name of the selected toolbar.



Tip

You can use the following tips for adding and removing buttons in built-in (the toolbars provided with System Connectivity Manager) and custom toolbars, without opening the Customize dialog box.

- To add buttons to a built-in toolbar, press *Alt* and drag and drop the desired button from any other toolbar to the built-in toolbar.
- To add buttons to a custom toolbar, press *Ctrl + Alt* and drag and drop the desired button from any other toolbar to the custom toolbar.
- To remove a button from a toolbar, press *Alt* and drag and drop the desired button into an empty area in System Connectivity Manager.

New Toolbar

Lets you specify the name for a new custom toolbar.

How to Access

Click the *New* button in the Toolbars tab.

Commands

Lets you drag and drop buttons (for various commands) to toolbars.

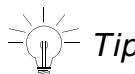
System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Choose *Tools – Customize*, then select the *Commands* tab.

Categories	Lists the categories of commands for which buttons are available.
Buttons	Lists the buttons available for commands in a category. Drag and drop a button to any area in System Connectivity Manager. If the button is dropped on an existing toolbar, System Connectivity Manager adds the new button to it. If the button is dropped in an open area and not on a toolbar, System Connectivity Manager creates a new toolbar with the new button.
Description	Describes the function of the selected button.



Tip
You can use the following tips for adding and removing buttons in built-in (the toolbars provided with System Connectivity Manager) and custom toolbars, without opening the Customize dialog box.

- ❑ To add buttons to a built-in toolbar, press *Alt* and drag and drop the desired button from any other toolbar to the built-in toolbar.
- ❑ To add buttons to a custom toolbar, press *Ctrl + Alt* and drag and drop the desired button from any other toolbar to the custom toolbar. You need not open the Customize dialog box to do this.
- ❑ To remove a button from a toolbar, press *Alt* and drag and drop the desired button into an empty area in System Connectivity Manager.

Customize Pane [<name_of_pane>]

Lets you select the columns to be displayed in the Component List, Signal List, Component Connectivity Details pane, the Signal Connectivity Details pane, and the Matrix Connectivity View. You can also use this dialog box to add columns for displaying property values.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

Do one of the following:

- Choose *Table – Customize Columns*.
- Right-click on a column heading name in the Component List, Signal List, Component Connectivity Details pane or the Signal Connectivity Details pane and choose *More*.

For example, if you want to select the columns to be displayed in the Component List, right-click on a column heading name in the Component List.

Available Columns	Displays the columns that can be displayed in the pane.
Added Columns	Displays the list of columns you have selected for displaying in the pane. The columns will be displayed in the pane in the order in which they are listed in the <i>Added Columns</i> list.
Display Name	Displays the column heading name that will be used for the selected column.
Add	Select a column in the <i>Available Columns</i> list and click this button to add the column in the <i>Added Columns</i> list.
Remove	Select a column in the <i>Added Columns</i> list and click this button to remove the column.
Move Up	Select a column in the <i>Added Columns</i> list to and click this button to move the column one level up in the list.
Move Down	Select a column in the <i>Added Columns</i> list to and click this button to move the column one level up in the list.
Add New	Click this button to add a column for a property. The <u>Column Definition</u> dialog box appears.
Delete	Select a column you added for a property and click this button to delete the column. Note: You cannot delete a predefined column.
Reset	Click this button to reset the display of columns to the predefined settings. The columns you added for user properties are deleted and the order of the columns in the <i>Added Columns</i> list is reset to the predefined order.

DC Voltage

Use this dialog box to specify the signal voltage.

How to Access

- Choose *Object – Change – DC Voltage*.
- In the Signal List pane, right-click on the signal name and choose *Change – DC Voltage*.

By default, the unit used is Volts. However, you can specify the voltage value in millivolts by specifying m

Voltage

Enter a numeric value to be used as signal voltage.

Note: To specify the voltage value in millivolts, enter mV along with the numeric value. For example, to specify the Voltage value as 10 millivolts, enter 10mV

Discrete Component Setup

Use this dialog box to associate library components for the resistors, capacitors, or diodes that will be used in adding terminations, bypass capacitors, and pullups or pulldowns. These components will appear as the default component when you are defining terminations, bypass capacitors, and pullups or pulldowns for any component.

For example, when you click the *Part* button in the Add Termination dialog box to select the resistor component you want to use for the termination, Part Information Manager appears. The resistor component you selected in the Discrete Component Setup dialog box will be selected by default. This helps in quickly selecting the discrete components you want to use for adding terminations, bypass capacitors, and pullups or pulldowns.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Select the Setup button from the *Add Bypass Capacitor* dialog box.

Resistor	Associate the library component for the resistor to be used in terminations. To associate a new component, click <i>Browse</i> . Part Information Manager opens where you can select a resistor.
Capacitor	Associate the library component for the capacitor to be used in terminations. You can use the <i>Browse</i> button to select a new component from Part Information Manager.
Diode	Associate the library component for the diode to be used in terminations. You can use the <i>Browse</i> button to select a new component from Part Information Manager.
Inductor	Associate the library component for the inductor to be used in terminations. You can use the <i>Browse</i> button to select a new component from Part Information Manager.

Document Schematic Generation

Use this dialog box to generate the document schematic for your design.

How to Access

- Choose *Project – Generate Schematics*.

Block Name	Displays the name of all the blocks in the logical design.
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The root design for which you are generating the document schematic is also treated as a block as it is listed as the first block.

GenerateSchematic	Select this check box for all the blocks for which you want the document schematic to be created.
--------------------------	---

Note: To generate the project-level schematic, ensure that the Generate Schematic check box is selected for block representing the root design.

System Connectivity Manager User Guide

Dialog Box Descriptions

Embed Block	Select this check box, to replace the schematic block in the project-level documentation schematic with single page schematic.
	 <p>This check box is enabled only for the schematic blocks that have a single page schematic. Block flattening is not supported for schematic blocks with multiple pages.</p>
Preserve Mode	This check box is useful only if you are regenerating the documentation schematic and want to preserve placement and routing modifications made to document schematic originally generated. Note: For the preserve option to work, <code>docsch_1</code> view should be available for the selected block. Also, preserve option is not valid for schematic blocks as these blocks are not recreated during schematic generation. If this check box is not selected, the <code>docsch_1</code> view is regenerated as a result all modifications made to the documentation schematic are overwritten.
Launch Design Entry HDL on Block Schematic	Select this check box if you want the generated document schematic for the block to be opened in Design Entry HDL. When you select this check box, the schematic saved in <code>docsch_1</code> view of the block is opened. You can make placement changes in this schematic and these will be preserved during subsequent regenerations of the document schematic for the block. Schematic for each block is opened in a separate instance of DEHDL. For Example, if you select this check box for 5 blocks, five instances of DEHDL will be launched.
Generate Flat Documentation Schematic for <root block>	Select this check box if you want to open the generate a Flat documentation schematic for the complete root design in Design Entry HDL. When you select this check box, the schematic is saved in <code>sch_1</code> view of the <code><root_block>_doc</code> cell. Changes made to this schematic cannot be preserved.
Run	Click this button to generate the document schematic for the root design.

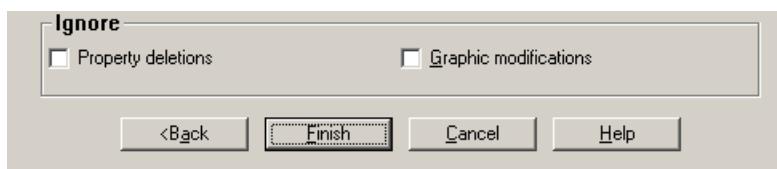
System Connectivity Manager User Guide

Dialog Box Descriptions

Setup	Click this button to display the <i>Document Schematic Generation Setup</i> dialog box. Here you can specify the options for generating the document schematic.
Details	Click this button if you want to view or hide the details of the document schematic generation process.

ECO Messages

The *ECO Messages* page displays the differences between the existing part and the source against which ECO is being done. By default, the properties not found in the source file but existing in the destination are deleted. You can turn off this behavior by selecting the *Property deletions* check box in the *Ignore* section. Similarly, select the *Graphic modifications* check box in the *Ignore* section if you want to turn off the default behavior of retaining the symbol graphic modifications that have been done during ECO.



Edit Alias

Use this dialog box to alias a net to multiple nets simultaneously.

For more information on aliasing nets, see [Aliasing Nets](#) on page 150.

How to Access

- Select a net in the Signal List, right-click and choose *Alias*.

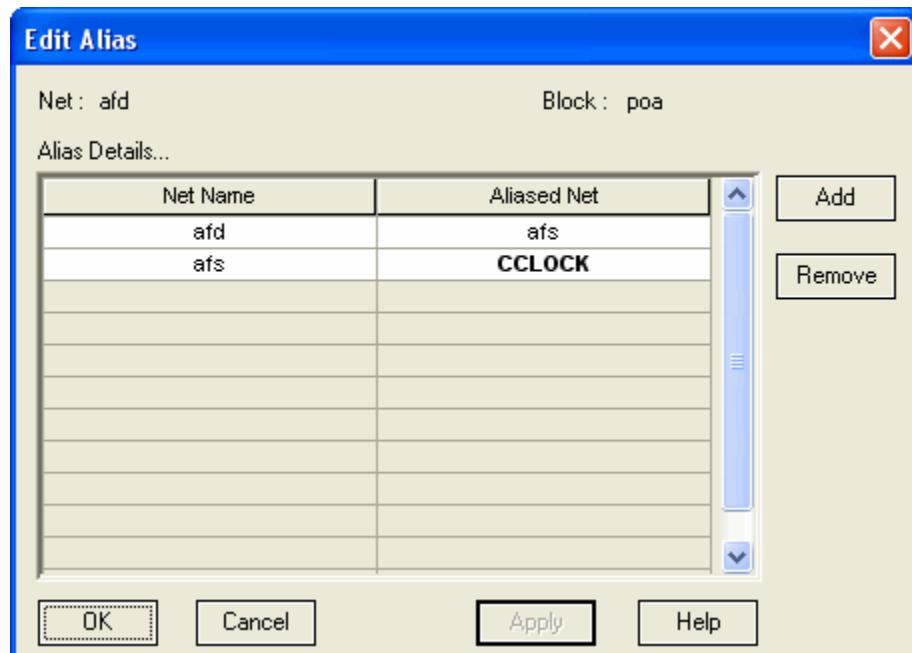
Net	Displays the name of the net being aliased.
Block	Displays the name of the block in which the net being aliased exists.
Alias Details	Displays the list of nets aliased to the net.

System Connectivity Manager User Guide

Dialog Box Descriptions

Net Name Displays the name of the net being aliased, and the name of an aliased net that in turn is aliased to another net.

For example, if the net **afd** is aliased to the net **afs** and the net **afs** is also aliased to the net **CCLOCK**, the Edit Alias dialog appears as shown below:



The net that is displayed in bold letters is a net that has been declared as the base net.

- Right-click on a net and choose *Make Base* to declare the net as a base net.
- To remove the base net declaration, right-click on the base net and choose *Clear Base*.

For more information on declaring a net as the base net, see [Declaring an Aliased Net as the Base Net](#) on page 153.

Aliased Net Displays the name of the net that is aliased to the net displayed in the *Net Name* column.

Add Click this button to display the [Provide Alias Details](#) dialog box. You can use this dialog box to select the net you want to alias to the net.

Remove	Select the row for the aliased net you want to remove and click the <i>Remove</i> button.
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Edit Block

Use this dialog box to select a block you want to edit from the libraries for the project. The block is opened for editing in the master mode.

For more information on working with blocks, see [Working with Hierarchical Designs](#) on page 337.

How to Access

- ▶ Choose *Project – Edit Block*

Library	Click the drop-down list to select the library that contains the block you want to edit.
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Cell	Select the block you want to edit.
-------------	------------------------------------

Edit Block Interface

Lets you edit the ports of a block and select the global signals you want the block to inherit from the parent block or design.

How to Access

- ▶ Open the block for editing in context or master mode and do one of the following:
 - Choose *Design – Edit Block Interface*.
 - Select the block in the *Hierarchy Viewer*, right-click and choose *Edit Block Interface*.

Ports tab

Lets you edit the ports of a block.

Existing Port Name	Displays the current port name.
New Port Name	You can do the following: <ul style="list-style-type: none">■ Enter a port name in a blank row to add a new port for the block.■ Enter a new port name next to an existing port name if you want to modify the port name.
	Note: For vectored ports, specify the width of the port name in angular brackets. For example, specify the width of a 8 bit vectored port named ADDRESS as ADDRESS<7..0>.
Port Type	Change the port type, if required. The port type can be one of the following: <ul style="list-style-type: none">■ IN■ OUT■ INOUT

Globals tab

Lets you select the global signals you want the block to inherit from the parent block or design.

Block	Displays the name of the block.
Globals	Displays the list of global signals in the parent block or design. Do one of the following: <ul style="list-style-type: none">■ Select the check box next to a global signal if you want the block to inherit the global signal from the parent design.■ Clear the check box next to a global signal if you do not want the block to inherit the global signal from the parent block or design.

Edit Design Ref Des Range

Lets you specify, modify, or remove the reference designator range you want to use for components in the block.

How to Access

Do the following:

1. Open the block for editing in context or master mode.
2. Choose *Design – Edit Block Refdes Range*.

Ref Des Range	Displays the reference designator range you specified when you create a block or add it in the design To specify a new reference designator range, select this option and enter the range.
Minimum Range Width Required	Displays the minimum width for the reference designator range you must specify in the <i>Ref Des Range</i> field. For example, if the block has 12 components, the minimum range width required will be 12. This means that you must specify a reference designator range that has a width of 12, say 101 to 112 in the <i>Use Ref Des Range</i> field.
Remove Ref Des Range	To remove the reference designator range specified for the block, select this option.

Edit Instance Name Dialog

Lets you modify the instance names of more than one component simultaneously.

How to Access

Do the following:

1. Select the components whose instance names you want to change in the Component List.

2. Choose *Object – Change – Name.*

Old Instance Name Value	Displays the instance names of the components you selected in the Component List.
New Instance Name Value	Enter the new instance name for a component. You can also copy instance names from another application such as Microsoft Excel and paste them in this column.

Edit RefDes Dialog

Lets you modify the reference designator values of more than one component simultaneously.

How to Access

Do the following:

1. Select the components whose reference designators you want to change in the Component List.
2. Choose *Object – Change – Ref Des – User Assigned.*

Instance Name	Displays the instance names of the components you selected in the Component List.
Old RefDes Value	Displays the reference designator values of the components you selected in the Component List.
New RefDes Value	Enter the new reference designator value for a component. You can also copy reference designator values from another application such as Microsoft Excel and paste them in this column.

Edit Signal Voltage

Lets you specify the voltage values for more than one signal simultaneously.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

Do the following:

1. Select the signals for which you want to specify voltage values in the Signal List.
2. Choose *Object – Change – DC Voltage*.

Signal Displays the names of the signals you selected in the Component List.

Voltage Specify the voltage value for a signals.

You can also copy voltage values from another application such as Microsoft Excel and paste them in this column.

Export Physical

Use this dialog box to export the logical design to translate it into a physical design ready for board layout in Allegro PCB Editor or in SiP Layout.

How to Access

- For designing a PCB board, choose *Project – Export Physical – PCB Board*.
- For designing a SiP Layout, choose *Project – Export Physical – SiP Package*.

Generate package files (pstdedb.cdsz) Select this check box if you want to package the System Connectivity Manager design before exporting it to the physical layout tool.

System Connectivity Manager creates the `pstdedb.cdsz` file that contains the four packaging files (`pstchip.dat`, `pstxprt.dat`, `pstxnet.dat` and `pstcmdb.dat`) in the packaged view of the root design when you click *OK*.

For more information on the `pst*.dat` packaging files, see [System Connectivity Manager to Allegro PCB Editor Flow](#) on page 465.

Note: You can set the `DS_PRESERVE_PSTFILE` environment variable if you want System Connectivity Manager to create the `pstdedb.cdsz` file and the four packaging files (`pstchip.dat`, `pstxprt.dat`, `pstxnet.dat` and `pstcmdb.dat`) in the packaged view of the root design.

System Connectivity Manager User Guide

Dialog Box Descriptions

Update Board (Netrev) Transfers the design in System Connectivity Manager design and updates the board in the board layout tool.

While designing a PCB, the board layout tool used in Allegro PCB Editor. For designing a SiP, SiP Layout is used as the board design tool.

Input Board File Specifies the name of the board file that you want to update. By default, the name of the board file that was created during a previous run of *Export Physical* is displayed in the *Input Board File* field. If the path to the board file is not displayed, it indicates that the board file exists in the physical view of the root design.

To use another board file as the input board file, enter the name and path to the board file, or click *Browse* to select the file.

Output Board File Specifies the name of the resulting updated board file. By default, the name of the board file that was created during a previous run of *Export Physical* is displayed in the *Output Board File* field. If the path to the board file is not displayed, it indicates that the board file exists in the physical view of the root design.

If the input and output board file names are the same, System Connectivity Manager overwrites the existing board file. If you specify a new file name for the output board file, a new board file is created.

Note: If you specify a new file name for the output board file, but do not specify the path where the file needs to be created, the output board file will be created in the physical view of the root design.

Allow Etch Removal During ECO Select this option:

- To specify what to do with the connect lines that connect to the pin if an engineering change order (ECO) removes a pin from a net.
- To save time and have the layout tool rip up this etch from a removed pin to the closest T connection or pin.

Note: Do not select this option if you want the layout tool to rip up etches interactively.

System Connectivity Manager User Guide

Dialog Box Descriptions

Place Changed Components	An ECO can result in a reference designator being assigned to a different type of device in the logical design than the device used in the board layout. This option specifies how to treat placed parts during the ECO process. Parts are compared to determine if there are any changes (new type/value, new package symbol, or both). If the part has not changed, it maintains its location in the physical layout tool. If the part has changed, you can select one of the following options: Always: The board layout tool automatically replaces all parts in the layout with the new parts from System Connectivity Manager according to their reference designators and at the same x/y location and rotation as the old part. If Same: The board layout tool automatically replaces all parts in the layout with the new parts from System Connectivity Manager but only if the replacement component matches the package symbol, value, and the tolerance of the component in the layout. If the package symbol has changed, the old part is removed from the layout, and the changed part is added to the Allegro PCB Editor database as an unplaced part. Never: Specifies that the board layout tool should not replace the components in the layout with new components. You must make the changes interactively.				
Electrical Constraints	<table><tr><td>Overwrite Current Constraints</td><td>Deletes all existing electrical constraint information in the <i>Output Board File</i> and replaces it with the electrical constraint information currently available in the logical design.</td></tr><tr><td>Export changes only</td><td>Exports only the electrical constraint information that has changed in the logical design since the last export, and updates such constraints in the <i>Output Board File</i>.</td></tr></table>	Overwrite Current Constraints	Deletes all existing electrical constraint information in the <i>Output Board File</i> and replaces it with the electrical constraint information currently available in the logical design.	Export changes only	Exports only the electrical constraint information that has changed in the logical design since the last export, and updates such constraints in the <i>Output Board File</i> .
Overwrite Current Constraints	Deletes all existing electrical constraint information in the <i>Output Board File</i> and replaces it with the electrical constraint information currently available in the logical design.				
Export changes only	Exports only the electrical constraint information that has changed in the logical design since the last export, and updates such constraints in the <i>Output Board File</i> .				
Board launching Option	Specifies the tool where <i>Export Physical</i> will open the board file after packaging it. You can set Export Physical to open the board file in Allegro PCB Editor, Allegro PCB SI, or Allegro Package Designer, or not to open the board. Note: While creating the board file for a SiP, the board file opens in SiP Layout.				

Export Schematic

Use this dialog box to export the logical design as a schematic project, along with the associated libraries and supporting files.

How to Access

- Choose *Project – Export – Schematics*.

Project Location Specify the location to create the Design Entry HDL project in. You can use the Browse button to choose a location.

By default, the exported project is created in the directory, exportsch, located one level above the current project.

Project Name Displays the name of the project that will be created. This is the same as the current System Connectivity Manager project name.

Library Displays the name of the library in the exported project where the schematic is located.

Cell Displays the name of the cell in the exported project where the schematic is located.

View Displays the name of the view in the exported project where the schematic is located.

OK Click to export the logical design

For more information on export schematics see [Chapter 22, “Exporting Schematics for a Design.”](#)

Edit User Pins

Use this dialog box to modify the user pins on a co-design object. All the logical pins added by you are listed in this dialog box. User pins added to the co-design object in SiP Layout, are also listed in this dialog box, but are not editable.

This dialog box can be used to add new user pins to the co-design object and also to remove existing user pins. This dialog box cannot be used to rename user pins, or to delete pins that are defined in the Verilog file used for creating a co-design die.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

Do one of the following:

- Select the co-design object in the Component List. Choose *Object – Edit User Pins*.
- Right-click on the co-design object in the Component List pane and choose *Edit User Pins*.

Note: The *Edit User Pins* command is available only for co-design objects. System Connectivity Manager when launched from the Cadence SiP Digital Architect GXL or XL products, provides support for co-design objects.

Pin Name Enter the name of the pin to be added to the co-design die

Pin Use Use this drop-down list to select a valid pin type for the pin to be added.

Find and Replace

Use this dialog box to search for specific property values and replace them with new values.

How to Access

- Press *Ctrl + F* (to display Find tab) and Press *Ctrl + H* (to display Replace tab)

Function

The Find and Replace dialog box is a quick way to find any property and replace that component or all matching instances with the new value.

Find What Type the property name or value that you want to search. You can select an old entry that you had previously searched from the list box.

Replace With Type the value that you would like to replace the searched value with. You can select an old entry that you had previously searched from the list box.

Replace All Select this button to replace all instances of the matching value entered in the *Find What* field with the value entered in the *replace With* field.

System Connectivity Manager User Guide

Dialog Box Descriptions

Replace	Select this button to replace the current component of the matching value entered in the <i>Find What</i> field with the value entered in the <i>replace With</i> field. Note: Select this option when you want to selectively review each occurrence of search text and need to replace only for specific occurrences.
Find All	Select this button to display the list of all instances that match the value entered in the <i>Find What</i> field.
Find Next	Select this button to scroll to the next occurrence of the searched text in the <i>Find What</i> field.
Close	Select this button to close the dialog box.
Options	Select this button to display additional options for refining the search criteria.
Within	Use this list box to specify whether you want to perform search only in instances or pins, or across all grids in System Connectivity Manager.
Search in	Use this list box to specify whether you want to perform search only in sheet, column, or row in System Connectivity Manager.
Search by	Use this list box to specify the search order as either column-first or row-first.
Match case	Select this check box to specify the search as case-sensitive. When the <i>Match Case</i> check box is selected, System Connectivity Manager only searches for text that match the exact capitalization as in the text entered in the <i>Find What</i> field.
Match entire cell contents	Select this check box to return only those cells in the search results that has only the content string as defined in the search criteria. For example, if you have “Hello World” as cell content and your search criteria is “Hello” or “World”, then there would not be any search results. If you enter only “Hello World” in the <i>Find What</i> field then the search would return the result. You can make the selection case-sensitive too by selecting the <i>Match case</i> check box.

Generate Report

Use this dialog box to generate reports using the report templates you have created.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Choose *Project – Reports – Generate Reports*.
- Run the `dsreportgen -proj <project_file> -ui` command from the command line.

For more information on the using the `dsreportgen` command, see [Using the dsreportgen Command](#) on page 550.

Project

Project File Displays the name of the project for which you are generating the report.

Report Template Displays the list of report templates you have added or created for the project.

By default, the report templates existing in the following locations are displayed in the *Report Template* list:

- `<your_install_dir>\share\cdssetup\tdd\report_templates\`
This directory contains the standard report templates shipped with your Cadence installation.
- `<your_install_dir>\share\cdssetup\tdd\custom_templates\`
You can use this directory to store customized report templates that you want to make available to your team members.
- Current project directory
- Current working directory

Customize Allows you to modify report templates.

Select a report template and click this button to open the [Create Report Template](#) dialog box. Here you can modify the report template. For more information on modifying report templates, see [Modifying a Report Template](#) on page 522.

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Dialog Box Descriptions

Add Existing	<p>Allows you to add existing report template files.</p> <p>Click this button to open the Select the Template File dialog box. Here you can add existing report template files to your project. Select the template file and click <i>Open</i> to add the template in the <i>Report Template</i> list.</p>
Create New	<p>Allows you to create new report templates.</p> <p>Click this button to open the <u>Create Report Template</u> dialog box. Here you can create a new report template. For more information on creating report templates, see <u>Creating a Report Template</u> on page 508.</p>
Remove from this list	<p>Allows you to remove report templates from the Report Template list.</p> <p>Select a report template in the Report Template list and click this button to remove the template from the list. To select multiple report templates, press the <i>Ctrl</i> or <i>Shift</i> key and click on the templates you want to remove.</p> <p>Note: The report template is only removed from the Report Template list. It is not deleted from the disk.</p>
Report Format	<p>Select the format in which you want the report to be generated. You can generate reports in the following formats:</p> <ul style="list-style-type: none">■ DSR (Editable Report File) format. For more information on this format, see <u>The .DSR (Editable Report File) Format</u> on page 534.■ CSV (Comma Separated Value format)■ Text File in Tabular Format■ HTML
Output	
Report File	<p>Select this option if you want to create the report in a specific report file.</p> <p>Enter the name and path to the file in which you want to create the report or click the browse button to select the report file.</p> <p>Note: You cannot select the <i>Report File</i> option if you have selected multiple report templates in the <i>Report Template</i> list.</p>

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Dialog Box Descriptions

Location	<p>Select this option if you want to create the report in a specific directory.</p> <p>By default, the reports will be created in the project directory. If you want the report to be created in some other directory, enter the path for the directory, or click the browse button to select the directory.</p> <p>The generated report will have the same file name as the report template file. For example, if you are generating a report using a report template named <code>BOM_Report.tpt</code> for a root design named <code>CPU</code>, the report file name will be <code>CPU_BOM_Report.html</code> if you are generating a report in the HTML format.</p>
Override Qualified Value for Report Driver	<p>Select this check box if you want to override the qualifier or qualifier value for the driver keyword in the selected report template when you generate the report.</p> <p>For more information on driver keywords in report templates, see Adding a Keyword in the Query Grid on page 511. For more information on keyword qualifiers and qualifier values in report templates, see Specifying the Qualifier for a Keyword on page 514.</p>
Setup	<p>Click this button if you want to specify the sort order, column and row separators, fonts and custom variables to be used in the generated report.</p> <p>For more information, see the following topics:</p> <ul style="list-style-type: none">■ Setting Up the Report Format on page 533■ Defining Custom Variables for Headers and Footers in Reports on page 549

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Dialog Box Descriptions

Generate	<p>Select one or more report templates in the <i>Report Template</i> list and click this button to generate reports using the selected report templates. To select multiple report templates, press the <i>Ctrl</i> or <i>Shift</i> key and click on the templates you want to use.</p> <ul style="list-style-type: none">■ If you have selected the <i>Override Qualifier Value for Report Driver</i> check box, the <u>Qualify Report Parameter</u> dialog box appears. Here you can override the qualifier or qualifier value for the driver keyword in the selected report template when you generate the report. When you click OK in the Qualify Report Parameter dialog box, the report is generated.■ If you did not select the <i>Override Qualifier Value for Report Driver</i> check box, the report is generated. <p>The report is generated in the selected format and displayed in System Connectivity Manager. For example, if you are generating a report in the HTML format for a root design named CPU, using a report template named <code>BOM_Report.tpt</code>, the <code>CPU_BOM_Report.html</code> report file is displayed in System Connectivity Manager.</p>
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Global Find

Use this dialog box to:

- Find blocks, components, nets, and properties across all the blocks in a design.
- Find associated components and highlight their respective parent components in the design.
- Review the search results in a list. You can also filter the search results to display only the search results for selected blocks in a hierarchical design.
- Locate each block, component, net or property listed in the search results. You can zoom in on a selected search result, which is highlighted in the design.
- Replace a selected component in the search results with another component.

Note: You cannot replace a block with another block.

You can use the * (asterisk) and ? wildcard characters to perform the search.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Choose *Project – Global Find*.

Select	Select the object (component, net, or property) you want to find in the design. You can use the * (asterisk) and ? wildcard characters to perform the search.
Components	Select this option if you want to perform a global search for components.
Library	Enter the name of the library if you want to restrict the search to a component that exists in the specified library.
Cell	Enter the name of the component you want to search in the design. For example, enter <code>1s04</code> to find all instances of the component <code>1s04</code> in your design.
View	Enter the name of the view if you want to restrict the search to a symbol or package for the component that exists in the specified view of the cell for the component. <ul style="list-style-type: none">■ Enter the name of the view for a symbol version if you want to restrict the search to a component that is instantiated using that symbol version of the component. For example, enter <code>sym_1</code>, if you want to restrict the search to a component that is instantiated using symbol version 1 of the component.■ Enter <code>chips</code> to restrict the search to a component that has been added as a package in the design.
Select	Click this button to display Part Information Manager. Select the component you want to search in the design and click <i>Replace</i> . The name of the component library, cell, and view are displayed in the <i>Library</i> , <i>Cell</i> and <i>View</i> fields.
Nets	Select this option if you want to perform a global search for nets.
Name	Enter the name of the net you want to search in the design. For example, to find a vectored signal <code>DATA<3..0></code> , enter <code>DATA</code> or <code>DATA<3..0></code> .
Properties	Select this option if you want to perform a global search for properties.
Name	Enter the name of the property you want to search in the design.

System Connectivity Manager User Guide

Dialog Box Descriptions

Value	<p>Enter the value of the property.</p> <p>Do one of the following:</p> <ul style="list-style-type: none">■ Enter the value of the property if you want to find only the properties having the specific value.■ Use the * and ? wildcard characters to specify the property value. <p>For example, enter * in the <i>Value</i> field to find all components, nets or pins having the specified property name with any value.</p>
Show Advanced Options	<p>Select this check box if you want to search for components or nets that have a specific property.</p>
Property Name	<p>Enter the name of the property to be searched.</p> <p>Do one of the following:</p> <ul style="list-style-type: none">■ Click on the property name cell and select a property from the drop-down list.■ Click on the property name cell and enter the property name. <p>You can use the * (asterisk) and ? wildcard characters to perform the search.</p>
Property Value	<p>Do one of the following:</p> <ul style="list-style-type: none">■ Enter the value of the property if you want to find only the properties having the specific value.■ Enter an * (asterisk) to find all components or nets having the specified property name with any value. You can also use the ? wildcard character to perform the search. <p>Click this button if you want to add additional rows for specifying more properties to be searched.</p> <p>This allows you restrict the search to only the components or nets that have the specified properties.</p> <p>Select a row and click this button to delete the row.</p>  

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Dialog Box Descriptions

Results	<p>Displays the search results. You can do the following:</p> <ul style="list-style-type: none">■ Select a row in the search results, right-click and choose <i>Highlight</i>, to highlight the object (component, net, or property) in the design. <p>Note: If the block in which the object exists is currently not opened for editing in System Connectivity Manager, the block is automatically opened in System Connectivity Manager.</p> <p>Note: If you are performing a global find for properties, the component or net that has the property will be highlighted in the design.</p> <ul style="list-style-type: none">■ Select a row in the search results, right-click and choose <i>Dehighlight</i>, to dehighlight the object (component, net, or property) in the design.■ If you are performing a global find for components select a row in the search results, right-click and choose <i>Replace Components</i>, to replace the component. For more information on replacing components, see Replacing a Component with another Component on page 110. <p>Note: Before replacing components, you must setup the options for replacing components in the Component Replace tab of the Setup dialog box.</p>
Filter Results	<p>Allows you to view the search results for only the selected blocks.</p> <ul style="list-style-type: none">■ Clear the check box next to a block name if you want to do not want to view the search results for that block.■ Select the check box next to a block name if you want to view the search results for that block.
Object Name	Displays the name of the component, signal or property found in the design.
Exists In	<p>Displays the name of the:</p> <ul style="list-style-type: none">■ Block in which a component or net exists■ Component or block on which a property exists.
Ref. Des	Displays the reference designator of the components found in the design when you perform a global search for components.

System Connectivity Manager User Guide

Dialog Box Descriptions

Hierarchical Path	Lists the results of the search by the full canonical name for each component or signal.
Search Now	Click this button to perform a global search.

Global Replace

Use this dialog box to:

- Find and replace components and properties across all the blocks in a design.
Note: Before replacing components, you must setup the options for replacing components in the Component Replace tab of the Setup dialog box.
- Find and rename nets across all the blocks in a design.
- Find associated components, and modify the component by selecting another PTF row from the same component.
- Review the list of replaced components, nets and properties. You can zoom in on a selected object in the list, which is highlighted in the design.

While working with the Associated Components, note the following:

- You cannot replace associated components with a different library component. You can only select another PTF row from the same component.
- You cannot modify associated components within schematic blocks or read-only blocks.
- Ensure that old and the new PTF rows have the same cell/view combination. If the cell/view combination is different, the component is not replaced a message is displayed in the *Violations* window.
- When you use wildcard characters (*), there is a 1:1 relationship between cell/view combinations of the old and replaced components. For example, if you search for `view=*` and replace it with `view= Sym_1`, the `Sym_1` view of the old component is replaced with the `Sym_1` view of the new component.

How to Access

- Choose *Project – Global Replace*.

System Connectivity Manager User Guide

Dialog Box Descriptions

Components tab

Use this tab to find and replace components across all blocks in a design.

Library	Enter the name of the library if you want to replace only the components that exist in the specified library.
Cell	Enter the name of the component you want to replace in the design. For example, enter <code>ls04</code> to replace all instances of the component <code>ls04</code> in your design.
View	Enter the name of the view if you want to replace a component that uses a symbol version or package in the specified view of the cell for the component. <ul style="list-style-type: none">■ Enter the name of the view for a symbol version if you want to replace a component that is instantiated using that symbol version of the component. For example, enter <code>sym_1</code>, if you want to replace a component that is instantiated using symbol version 1 of the component.■ Enter <code>chips</code> to replace a component that has been added as a package in the design.

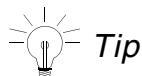
Select Component to Replace

Library	Displays the name of the library in which the component you want to use to replace the original component exists.
Cell	Displays the name of the cell in which the component you want to use to replace the original component exists.
View	Displays the name of the view of the component you want to use to replace the original component. For example, if the view name is <code>sym_1</code> , it means that you are using symbol version 1 of the component to replace the original component. If the view name is <code>chips</code> , it means that you are instantiating the component as a package to replace the original component.
Select	Click this button to display Part Information Manager. Select the component you want to use to replace the component and click <i>Replace</i> . The name of the component library, cell, and view are displayed in the <i>Library</i> , <i>Cell</i> and <i>View</i> fields.

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Dialog Box Descriptions

Show Advanced Options Select this check box if you want to replace components that have a specific property, or add new properties to the replaced component. For more information, see [Advanced Options](#).



Tip

If you want to add a new property on all instances of the 1s04 component, enter 1s04 in the *Name* field, click *Select* to select the 1s04 component using Part Information Manager, and enter the new property and its value in the *Add these Properties* list.

Nets tab

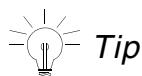
Use this tab to find and rename nets across all blocks in a design.

Name Enter the name of the net you want to rename in the design.

Select Net to Replace

Name Enter the new name for the net.

Show Advanced Options Select this check box if you want to rename nets that have a specific property or add new properties to the renamed net. For more information, see [Advanced Options](#).



Tip

If you want to add a new property on a net, enter the same net name in the *Name* field and enter the new property and its value in the *Add these Properties* list.

Properties tab

Use this tab to find and replace properties across all blocks in a design.

Name Enter the name of the property you want to replace in the design.

System Connectivity Manager User Guide

Dialog Box Descriptions

Value	Do one of the following: <ul style="list-style-type: none">■ Enter the value of the property if you want to replace only the properties having the specific value.■ Enter an * (asterisk) to replace properties having the specified property name with any value.
Select Property to Replace	
Name	Enter the name of the property you want to use to replace the original property.
Value	Enter the value for the new property.
	 <i>Tip</i> <p>If you want to modify only the value of a specific property, enter the same property name in the <i>Name</i> field and enter the new property value in the <i>Value</i> field.</p>
Show Advanced Options	Select this check box if you want to: <ul style="list-style-type: none">■ Replace properties on a component or net only if that component or net has a specific property■ Add a new property on a component or net on which you are replacing an existing property. <p>For more information, see Advanced Options.</p>

Advanced Options

Search with Properties	Lets you specify that: <ul style="list-style-type: none">■ A component or net should be replaced only if a specific property or properties exist on the component or net.■ A property should be replaced only if a component or net that has the property has another specific property or properties.
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Dialog Box Descriptions

Property Name	Enter the name of the property to be searched. Do one of the following: <ul style="list-style-type: none">■ Click on the property name cell and select a property from the drop-down list.■ Click on the property name cell and enter the property name.
Property Value	Do one of the following: <ul style="list-style-type: none">■ Enter the value of the property if you want to find only the properties having the specific value.■ Enter an * (asterisk) to find all components or nets having the specified property name with any value. You can also use the ? wildcard character to perform the search.
	Click this button if you want to add additional rows for specifying more properties to be searched.
	This allows you restrict the search to only the components or nets that have the specified properties. Select a row and click this button to delete the row.
Add these Properties	Lets you add properties when you are performing a global replace.
Property Name	Enter the name of the property you want to add on the component or net you are replacing. If you are performing a global replace for properties, enter the name of the property you want to add on a component or net on which the property you are replacing exists.
Property Value	Enter the value of the property you want to add. Click this button if you want to add additional rows for specifying more properties to be added.
	Select a row and click this button to delete the row.
	

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Dialog Box Descriptions

Results

Displays the global replace results. You can do the following:

- Select a row in the search results, right-click and choose *Highlight*, to highlight the object (component, net, or property) in the design.

Note: If the block in which the object exists is currently not opened for editing in System Connectivity Manager, the block is automatically opened in System Connectivity Manager.

Note: If you are performing a global replace for properties, the component or net that has the property will be highlighted in the design.

- Select a row in the search results, right-click and choose *Dehighlight*, to dehighlight the object (component, net, or property) in the design.

Filter Results Allows you to view the replace results for only the selected blocks.

- Clear the check box next to a block name if you want to do not want to view the replace results for that block.
- Select the check box next to a block name if you want to view the replace results for that block.

Object Name Displays the name of the component, signal or property replaced in the design.

Exists In Displays the name of the:

- Block in which a component or net exists
- Component or block on which a property exists.

Ref. Des Displays the reference designator of the components replaced in the design when you perform a global replace for components.

Hierarchical Path Lists the results of the search by the full canonical name for each component or signal.

Replace Click this button to perform global replace.

Global Signals

Lets you select the global signals you want the block to inherit from the parent block or design.

How to Access

- Select the *Inherit global signals from root design* check box in the [Create Block](#) dialog box and click the *Edit* button.

Select the global signals to be inherited Displays the list of global signals in the parent block or design.
Do one of the following:

- Select the check box next to a global signal if you want the block to inherit the global signal from the parent design.
- Clear the check box next to a global signal if you do not want the block to inherit the global signal from the parent block or design.

Header/Footer

Use this dialog box to enter the header and footer information you want to be displayed when you preview or print a report file in the .dsr (Editable Report File) format.

You can use text or variables to enter the header or footer information. For more information on using variables to specify header or footer information in reports, see [Using Variables in Report Headers and Footers](#) on page 545.

How to Access

Do the following:

1. Open a report file in the .dsr (Editable Report File) format.
2. Choose *File – Header/Footer*.

Header tab Lets you enter or modify the header information you want to be displayed when you preview or print a report file in the .dsr (Editable Report File) format.

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Dialog Box Descriptions

Footer tab	Lets you enter or modify the footer information you want to be displayed when you preview or print a report file in the .dsr (Editable Report File) format.
Left Aligned	Use this column to enter the header or footer information that should be left aligned in the report.
Centered	Use this column to enter the header or footer information that should be centered in the report.
Right Aligned	Use this column to enter the header or footer information that should be right aligned in the report.
Font	Click this button to change the font settings for displaying the header or footer information in the report. Click on a cell in which you have entered the header or footer information, if you want to specify the font settings only for that cell, or drag the mouse to select the cells for which you want to change the font settings. Click on the <i>Font</i> button to display the Font dialog box, change the font settings as required, and click <i>OK</i> . The default font is Arial 8.
Distance to Frame	
Header	Specify the distance between the top of the page and the first line in the header in the <i>Header</i> field. For example, if you specify the distance as 0.5, the distance between the top of the page and the first line in the header will be 0.5 inches.
Footer	Specify the distance between the bottom of the page and first line in the footer in the <i>Footer</i> field. For example, if you specify the distance as 0.5, the distance between the bottom of the page and the first line in the footer will be 0.5 inches.
Page Numbering	
First Page No.	Enter the number from which the page numbering should start in the <i>First Page No.</i> field.
Save settings to profile	Select this check box if you want to save the header and footer settings in the Windows registry.

Import Block: Step 1

Lets you to import a block from another project (.cpm) file or cds.lib file into the current design.

You can import a block as a read-only block or as a read-write block into your design. For more information, see [Importing a Block](#) on page 395.

How to Access

- Choose *File – Import Block*.

Import Block

Using Project File (*.cpm) Select this option if you want to import a block from another project (.cpm) file, then enter the name and path to the .cpm file for the other project in the *Location* field or click the browse button to select the .cpm file.

Note: You cannot import a block from the .cpm file for the current project.

Using Library File (cds.lib) Select this option if you want to import a block from the cds.lib file of another project, then enter the name and path to the cds.lib file in the *Location* field or click the browse button to select the cds.lib file.

Import Block: Step 2

Lets you select the block you want to import into your design. You can import a block as a read-only block or as a read-write block into your design. For more information, see [Importing a Block](#) on page 395.

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Dialog Box Descriptions

How to Access

- Click **Next** in the Import Block: Step 1 dialog box.

Library	Displays the list of libraries defined in the project (.cpm) file or the cds.lib file you selected in the <u>Import Block: Step 1</u> dialog box.
Blocks	Displays the list of blocks existing in the libraries displayed in the <i>Library</i> list. <ul style="list-style-type: none">■ To display only the blocks in a specific library, select the library in the Library list. If you select more than one library in the Library list, all the blocks in the selected libraries are displayed.■ To search for blocks by name, enter a search string using regular expressions or the wildcard characters * and ? in the filter field.
Import Options	Lets you specify the options for importing the block.
View	Displays the list of spreadsheet, schematic and Verilog views existing in the block you selected in the <i>Blocks</i> list. <p>Select the view of the block you want to import. For example:</p> <ul style="list-style-type: none">■ To import a spreadsheet view, select a spreadsheet view (tbl_1, tbl2 and so on).■ To import a schematic view, select a schematic view (sch_1, sch_2 and so on).■ To import a Verilog view, select the vlog_structural view.
Read-Only	Select this option if you want to import the block as a read-only block. <p>For more information about importing as a read-only block, see Importing as a Read-Only Block on page 396.</p>
ReadWrite	Select this option if you want to import the block as a read-write block. <p>For more information about importing as a read-write block, see Importing as a Read-Write Block on page 396.</p>

Import Block: Step 3

Displays the details of the block you have selected for importing into your design. For more information on importing blocks, see [Importing a Block](#) on page 395.

How to Access

Click *Next* in the [Import Block: Step 2](#) dialog box.

Library	Displays the name of the library from which you are importing the block.
Block	Displays the name of the block you have selected for importing into your design.
View	Displays the name of the view of the block you have selected for importing into your design.
Type	Displays whether you are importing the block as a read-only block or as a read-write block.

Import ECO Netlist

Use this dialog box to import the connectivity information stored in a netlist to SCM. The supported netlist format is <refdes>. <pin_number> <signal_name>.

How to Access

- Choose *File – Import ECO Netlist*

In the Netlist File text box specify the name and the location of the netlist file to be imported in SCM.

Import Interface - ECO

This dialog box is used to import the modification in the SiP interface data.

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Dialog Box Descriptions

How to Access

Accessing this dialog box is a two-step process.

- a. Choose *Design – Import Interface*.
- b. Specify the .xml file to be imported and click *OK*.

Select Instance	Lists the instances of BGAs that are to be updated with the imported interface data.
Component Differences	Lists the BGA components that are not present in the design being updated. Note: This category of design difference is reported if you are importing the interface data in your design for the first time, and the corresponding BGA component is not included in the design.
Logical Pin Differences	Lists the logical pin numbers for which connectivity information has changed. The existing connectivity in the current design is displayed in the Existing Instance column, whereas the connectivity details being imported are listed in the Instance from Import XML file column.
Net Physical Net Name Changed	Lists the modifications in the interface nets. All the nets that have been added or deleted
Net Property Changed	Lists the differences in the properties attached to the interface nets.
Accept	Click this button to update the design by importing all the changes listed in the Import Interface -ECO dialog box.
Reject	Click this button to reject all the interface data being imported.

Import Physical

Use this dialog box to transfer the physical design from the Allegro PCB Editor layout database to the logical design in System Connectivity Manager.

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Dialog Box Descriptions

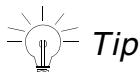
How to Access

- Choose *Project – Import Physical*

Use Board File Updates the logical design with the changes in the specified board file.

Enter the name of the board file whose changes you want to update to the logical design or click *Browse* to select the board file.

Use Feedback Files Updates the logical design with the changes in the feedback files created during a previous run of *Import Physical*.



Tip
You can also use *File – Export – Logic* in Allegro PCB Editor to generate the feedback files.

OK Click this button to display the differences between the logical design and the board in the Visual Design Differences pane.

The Visual Design Differences pane lets you view and update all the design differences between the logical design and the board. For more information, see [Running Visual Design Differences](#) on page 479.

Import Verilog

Lets you import a structural Verilog file into your design. System Connectivity Manager creates spreadsheet blocks for the modules in the Verilog file. You can then add the blocks in your design.



If you have captured component or net properties in the source Verilog file, System Connectivity Manager does not import these properties or PPT values. After importing the Verilog file, you need to assign the properties using the Properties window and the PPT values using Modify Component dialog box.

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Dialog Box Descriptions

How to Access

- Choose *Project – Import – Verilog – Netlist*

Verilog File

Specify the name and path to the Verilog file you want to import, or click the browse button to select the Verilog file.

Library

Specify the name of the library in which you want to create blocks for the modules in the Verilog file. By default, the blocks will be created in the working library (the library that contains the current root design (top-level design) for the project).

Blocks are created in the library for every module in the Verilog file. For example, if you import the following Verilog file, two blocks named `Top` and `Mid` are created in the library.

Contents of Verilog File

```
module Top ( x, y, carry_out, sum, carry_in);  
    input x, y;  
    output sum, carry_in, carry_out;  
endmodule  
  
module Mid ( x,y,carry,sum);  
    input x, y;  
    output sum, carry;  
endmodule
```

System Connectivity Manager User Guide

Dialog Box Descriptions

Use Instance Names as Reference Designator Select this check box if you want to use the instance names for components in the Verilog file as reference designators.

For example, if you select this check box and import the following Verilog file, the reference designator assigned for the resistors will be I1, I2, I3 and the reference designator for the capacitor will be I4.

Contents of Verilog File

```
module res (in, out);
    input in;
    output out;
    wire w1,w2;
    resistor i1 (in ,w1);
    resistor i2 (w2 ,out);
    resistor i3 (in ,out);
    capacitor i4 (in ,out);
endmodule
```

If you do not select this check box, the reference designators R1, R2 and R3 are assigned to the resistors and the reference designator C1 is assigned to the capacitor.

Note: This option is available only if you launch System Connectivity Manager from Allegro Design Authoring with the Design Authoring High Speed option and the Design Authoring Multi-Style Option.

Import Interfaces Only Select this check box if you want only the interface data stored in the Verilog file to be imported in SCM.

Note: This option is always selected and disabled when System Connectivity Manager is launched from Cadence SiP Digital Architect GXL or XL.

Module Name Specify the name of the module in the verilog file, that is to be imported in System Connectivity Manager.

This text box is required if you want to import a particular module from a multi-module verilog file.

Note: If you are using the SiP Digital Architect license to import a verilog block, you can only import the interface information of a specified module. The imported data gets instantiated as a verilog block.

System Connectivity Manager User Guide

Dialog Box Descriptions

Get	Click this button to populate the Module Name drop-down list.
Map Cells / Port Names	Select this check box if you want to map cell names and port names. System Connectivity Manager lets you use a map file to map component names in the Verilog file to cell (component) names in the libraries added for your project. You can also use the map file to map the port names of a component in the Verilog file to the port names of the cell (component) in a library.
Map File Name	Specify the name and path to the map file you want to use to map component names in the Verilog file to cell names, and port names in the Verilog files to port names of the cell. A sample Verilog file and the map file are listed below.

Contents of Verilog File

```
module example ();
    wire a,b,c;
    and_gate i1 (in1 (a),
                  in2 (b),
                  out1 (c));
endmodule
```

Contents of Map File

```
("and_gate" "ls00"
  (ports
    ("in1" "a")
    ("in2" "b")
    ("out1" "\y* ")
  )
)
```

If you import the Verilog file and select the `and_gate` map file, the following happens:

- A block named `example` is created in the selected library
- The component `and_gate` gets mapped to the cell (component) `ls00` in the libraries added for the project.
- The port `in1` `in2` of the component `and_gate` gets mapped to port `a` of the `ls00` cell.
- The port `in2` in the component `and_gate` gets mapped to port `b` of the `ls00` cell.
- The port `out1` in the component `and_gate` gets mapped to port `y*` of the `ls00` cell.



If you launch SCM using the Cadence SiP Digital Architect license, the *Use Instance Names as Reference Designator* check box is not selected and disabled. Similarly, the *Import Block as Table Block* and *Import Interface Only* check boxes are also not enabled but are selected. This is because using the SiP Digital Architect license, you can only import the interface information of a specified module. The imported data gets instantiated as a verilog block.

Import Wizard

The *Import Wizard* dialog box appears when you choose the *Import Part* option from the File menu. This page displays a list of supported data format that can be imported in SCM. Once you have imported the part information in your design, if required, you can also import the ECO data.

Mathematical Operator

Allows you to perform mathematical operations on keywords you have added in the report template query grid, and display the results in the report.

How to Access

Click on the  icon in the dependency cell below the MATH-OP keyword you have added in the report template query grid.

The fields in the dialog box is described using the following example:

If you want to find the cost of components for manufacturing three PCBs, do the following:

1. Add the property COST as a keyword in the query grid, with the dependency REFDES.
2. Add MATH-OP as a keyword in the query grid.
3. Click on the  icon in the dependency cell below the MATH-OP keyword.
The Mathematical Operator dialog box appears.
4. Select COST from the *Operand 1* drop-down list.
5. Select * from the *Mathematical Operator* drop-down list.
6. Enter 3 in the *Operand 2* field.
7. Click *OK*.
8. Select the check box in the total cell below the MATH-OP keyword.

When you generate the report, the total cost of components for manufacturing three boards is displayed in the report.

Menu Customization

Lets you customize the menus in System Connectivity Manager by:

- Adding new menu commands to a menu or submenu
- Adding a new submenu to a menu and then adding menu commands to the submenu.
- Adding separators in a menu or submenu,

Each menu in System Connectivity Manager has a standard set of menu commands. You can add these menu commands in the existing menus or under an existing or new submenu.

System Connectivity Manager User Guide

Dialog Box Descriptions

Note the following:

- You cannot create a new menu in System Connectivity Manager. You can only create submenus under an existing menu.
- You cannot create new menu commands in System Connectivity Manager. You can only add an existing menu command to a menu or a submenu.
- You cannot modify or delete the menu entries you added for user tools and Tcl/Tk tools in the *Tools* menu.

You can add, modify and delete the menu entries for user tools and Tcl/Tk tools in the *Tools* menu using the procedures described in [Customizing System Connectivity Manager Tools](#) on page 652.

Note: The settings for the customized menus will be stored in the `tddMenus.txt` file in the `\cdssetup\ade` folder that is created in the directory specified by the `HOME` environment variable. For example, if the `HOME` environment variable is set to `c:\` the settings for the customized menus will be stored in:

`c:\cdssetup\tdd\tddMenus.txt`

How to Access

- Choose *Tools – Customize – Menus*

Menu	Select the menu you want to customize. The commands, submenus and menu separators in the menu are displayed in the list. Note: The <i>Menu</i> drop-down list in the Menu Customization dialog box displays the menu names <i>File</i> and <i>File_Editors</i> . The commands listed in the <i>File</i> menu appear in the <i>File</i> menu in System Connectivity Manager when you start System Connectivity Manager without opening a project. The commands listed in the <i>File_Editors</i> menu appear in the <i>File</i> menu in System Connectivity Manager when you have opened a project in System Connectivity Manager. Hence, if you want to customize the <i>File</i> menu in System Connectivity Manager, choose <i>File_Editors</i> in the <i>Menu</i> drop-down list in the Menu Customization dialog box.
Add	Click this button to add a new menu command or a separator to the selected menu using the <u>Add Command</u> dialog box.

System Connectivity Manager User Guide

Dialog Box Descriptions

Delete/Undelete	Select a menu command or a separator and click this button to delete it from the menu. Note: When you delete a menu command that is provided as part of the default System Connectivity Manager menus, the menu command is grayed out and not deleted from the menu. To undelete a menu command that is grayed out, select the menu command and click the <i>Undelete</i> button.
Move Up	Select a menu command or a separator and click this button to move it one level up in the menu.
Move Down	Select a menu command or a separator and click this button to move it one level down in the menu.
Modify	Select a menu command and click this button to modify the label for the menu command using the <u>Modify Menu Label</u> dialog box.
Reset	Click this button to restore all the menus to their original state. All the changes you made to the menus are lost.

Modify Menu Label

Lets you modify the label for the menu command you selected in the [Menu Customization](#) dialog box.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Click *Modify* in the Menu Customization dialog box.

Enter a new label for the selected menu item Enter a new label for the menu command you selected in the Menu Customization dialog box.

Use the ampersand (&) character before the letter you want to use as the keyboard access key for the menu command. For example, if you want to use the letter D as the keyboard access key for the menu command named Design Rules Check, enter the label for the menu command as &Design Rules Check. The menu command will then appear in the menu as:

Design Rules Check

Note: When you define the access key for a menu command, ensure that the same access key is not being used by any other menu command in the menu.

New Project Wizard - Project Name, Location and Reference Library Location

Name Enter the name for the project that you are creating. For example, My_Project.

The project name can have only alphabets, numbers and the underscore ("_") character.

Project Location Enter the path to the folder in which you want to create the project, or click the browse button to select the folder in which you want to create the project.

If you want to create the project in a folder that does not exist in the path, add the name for the new folder to the path (for example: \cpu). The New Project Wizard will create the folder in the path.

System Connectivity Manager User Guide

Dialog Box Descriptions

Reference Libraries File Path	Specify the name and path to the <code>cds.lib</code> file containing the path to the reference libraries in your installation. The default reference library <code>cds.lib</code> file is located at <code><install_dir>\share\cdssetup\</code> .
-------------------------------	---

New Project Wizard - Project Libraries

This page lets you select the libraries for your project.

<i>Available Libraries</i>	<i>Available Libraries</i> are the libraries available for all projects, from which you select the libraries for each project. Available libraries are determined by the directives in the <code>cds.lib</code> file you selected in the <u>New Project Wizard - Project Name, Location and Reference Library Location</u> page.
<i>Project Libraries</i>	<i>Project Libraries</i> are the libraries you select for your project from the list of <i>Available Libraries</i> .
<i>Add</i>	Adds the libraries you select in <i>Available Libraries</i> list to the <i>Project Libraries</i> list. To select more than one library, press <i>Ctrl</i> and select the libraries in the <i>Available Libraries</i> list.
<i>Add All</i>	Adds all libraries in the <i>Available Libraries</i> list to the <i>Project Libraries</i> list.
<i>Remove</i>	Removes the selected libraries from the <i>Project Libraries</i> list. To select more than one library, press <i>Ctrl</i> and select the libraries in the <i>Project Libraries</i> list.
<i>Remove All</i>	Removes all the libraries from the <i>Project Libraries</i> list.
<i>Up</i>	Moves the selected library one level up in the <i>Project Libraries</i> list. The order in which the libraries are listed in the <i>Project Libraries</i> list determines their search order.

System Connectivity Manager User Guide

Dialog Box Descriptions

<i>Down</i>	Moves the selected library one level down in the <i>Project Libraries</i> list. The order in which the libraries are listed in the <i>Project Libraries</i> list determines their search order.
-------------	--

New Project Wizard - Project Work Libraries

This page lets you specify the working libraries for your project. These are the libraries in which System Connectivity Manager maintains the designs and libraries specific to your project.

Design Working Libraries	<p>Lists the working libraries for the project. By default, the <i>New Project Wizard</i> creates a working library named <projectname>_lib in the project location you specified in the <u>New Project Wizard - Project Name, Location and Reference Library Location</u> page.</p>
Add	Click <i>Add</i> , specify a library name in the <i>Enter the Working Library Name</i> dialog box and click <i>OK</i> , to add a working library for the project.
Remove	Select a library and click <i>Remove</i> to remove the library.

New Project Wizard - Design Name

This page lets you specify the working library, the top-level design name and the implementation type for your project.

Select Work Library Name	<p>Select the working library for your project. This is the libraries in which System Connectivity Manager maintains the designs and libraries specific to your project.</p>
Enter Top Level Design Name	<p>Enter the top-level design name for your project or click the browse button to select the design from the <i>Select a Design Name</i> dialog box. The top-level design will be the root design for your project.</p>

System Connectivity Manager User Guide

Dialog Box Descriptions

Implementation	Select the implementation type for the top-level design.
Spreadsheet	To create a spreadsheet based design.
Verilog	Capture your design in Verilog.
Vector Format	Select the vector format to be used for naming the vector pins and vector signals in your design. System Connectivity Manager supports square brackets as well as angular brackets in vector names. The naming format is important as it influences the physical net names.
Use square brackets as vector format	Select this check box if you want the use square brackets as the default naming convention for the vector signals and pins in the design. Note: When you launch System Connectivity Manager using one of the Cadence SiP Digital licenses, this check box is selected by default. For designs with co-design dies, it is recommended that square brackets should be used as the vector naming format.

New Project Wizard – Summary

The Summary page displays the details of the project. If you need to change any of the entries, you can go back and make the required changes.

Page Setup

Use this dialog box to setup the page layout that should be used when you preview or print a report file in the .dsr (Editable Report File) format.

How to Access

Do the following:

1. Open a report file in the .dsr (Editable Report File) format.
2. Choose *File – Page Setup*.

Margins

System Connectivity Manager User Guide

Dialog Box Descriptions

Left	Sets the distance between the left edge of the page and the left edge of left-aligned, unindented lines.
Right	Sets the distance between the right edge of the page and the right edge of right-aligned, unindented lines.
Top	Sets the distance between the top of the page and the top of the first line on the page.
Bottom	Sets the distance between the bottom of the page and the bottom of the last line on the page.

Titles and Gridlines

Row Headers	Select this check box if you want row headings to be printed in the report.
Column Headers	Select this check box if you want column headings to be printed in the report.
Print Frame	Prints the report outline.
Vertical Lines	Select this check box if you want vertical lines between columns to be printed in the report.
Horizontal Lines	Select this check box if you want horizontal lines between rows to be printed in the report.
Only Black and White	Select this check box if you want to report to be printed in black and white.
Page Order	If all the columns in a report cannot fit in a page, the columns will be printed across pages. Select one of the options below to specify the order in which you want the report to be printed.
First Rows, then Columns	Select this option if you want the rows in the report to be printed first and then the columns.
First Columns, then Rows	Select this option if you want the columns in the report to be printed first and then the rows.
Center on Page	Center the data on the page within the margins by selecting the <i>Vertically</i> check box, the <i>Horizontally</i> check box, or both.
Vertical	Select this check box if you want to center the data on the page within the top and bottom margins.
Horizontal	Select this check box if you want to center the data on the page within the left and right margins.

System Connectivity Manager User Guide

Dialog Box Descriptions

Save settings to profile	Select this check box if you want to save the page setup settings in the Windows registry.
Preview	Displays a preview of how the report will look when it is previewed or printed.

Physical View Block Selection

Lets you include or exclude blocks from the physical view. When you exclude a block from the physical view, the parts and nets in the excluded block are not displayed in the physical view. This helps you quickly debug the design by including only the blocks where errors are reported.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Choose *Design – Filter Blocks*, in the physical view

Hierarchy	<p>Displays the hierarchy of the blocks in the design.</p> <ul style="list-style-type: none">■ Select the check box next to a block to include the block in the physical view. If a block is not already included, right-click on a block and choose:<ul style="list-style-type: none"><input type="checkbox"/> <i>Include</i> to include the block<input type="checkbox"/> <i>Include All Occurrences</i> to include all occurrences of the block.<p>Note: If you include a top-level block, all the blocks under it will be automatically included.</p>
	<ul style="list-style-type: none">■ Clear the check box next to a block to exclude the block from the physical view. If a block is not already excluded, right-click on the block and choose:<ul style="list-style-type: none"><input type="checkbox"/> <i>Exclude</i> to exclude the block<input type="checkbox"/> <i>Exclude All Occurrences</i> to exclude all occurrences of the block<p>Note: If you exclude a top-level block, all the blocks under it will be automatically excluded.</p>
Exclude All	Excludes all blocks other than the root design from the physical view.
Include All	Includes all blocks in the physical view.

Note: If you have excluded blocks from the physical view, the System Connectivity Manager status bar displays the text FLTR as shown below.



Preview of Derived Data

This page gives a preview of the data that has been extracted from the source. If required, you can make modifications before actually creating the part.

Preview of Import Data

The *Preview of Import Data* page appears after selecting the destination part name and library. This page displays how the part will be created from the source file. If required, you can make changes on this page. This enables you to modify the part before its actual creation.

When you right-click on the pin information displayed on this page, the following menu is displayed:



Field	Description
Modify Values	Use this option to change the value of a selected cell.
Delete Selected Rows	Use this option to delete one or more rows of pin information. To cancel the operation, you need to go back to the previous step by clicking the <i>Back</i> button on the Preview of Import Data page and re-import the data.
Filter Rows	Use this option to display the Filter Rows dialog box and filter rows of pin information based on a pin detail. For example, you can specify a certain pin type in the Filter Rows dialog box to filter information for pins of that type only.
Select All	Use this option to select all the rows in the Logical Pins or Global Pins area.

System Connectivity Manager User Guide

Dialog Box Descriptions

Field	Description
DeSelect All	Use this option to clear the selection when all the rows are selected in the Logical Pins or Global Pins area.
Invert Selection	Use this option to clear the selected rows and select the rows that were not selected previously.
Hide Selected Cols	Use this option to hide one or more columns selected in the Logical Pins grid or the Global Pins grid.
Hide Selected Rows	Use this option to hide one or more rows selected in the Logical Pins grid or the Global Pins grid.
Unhide All Cols	Use this option to display all hidden columns in the current grid.
Unhide All Rows	Use this option to display all hidden rows in the current grid.
Insert Row After	Use this option to insert a row after the current row.
Insert Row Before	Use this option to insert a row before the current row.

Properties

Use this window to view or edit the properties on the selected component, pin or signal.

For more information on working with properties in the Properties window, see [Using System Connectivity Manager to Manage Properties](#) on page 253.

How to Access

Do one of the following:

- Choose *View – Properties*.
- Press *Ctrl + Alt + P*.

Drop-down List	Displays the name of the component, pin or signal you selected.
Name	Displays the properties on the selected object.
Value	Display the value of properties on the selected object.

Provide Alias Details

Use this dialog box to select the net you want to alias to a net.

How to Access

- Click *Add* in the [Edit Alias](#) dialog box.

Selected Net	Displays the details of the net to which you want to alias another net.
Net	Displays the name of the net to which you want to alias another net.
Start Bit	Displays the LSB (Least Significant Bit) of the selected net if the selected net is a vectored net.
End Bit	Displays the MSB (Most Significant Bit) of the selected net if the selected net is a vectored net.
Step Size	Modify the start bit or end bit of the selected net, or specify the step size to ensure that the width of the selected net and the width of the alias net are the same. For more information on using step size in net names, see Using Step Size to Connect or Alias Vectored Signals on page 185.
Alias Net	Displays the details of the net to which you want to alias the selected net.
Net	Click on the drop-down list to select the net to which you want to alias the selected net.
Start Bit	Displays the LSB (Least Significant Bit) of the alias net if the alias net is a vectored net.
End Bit	Displays the MSB (Most Significant Bit) of the alias net if the alias net is a vectored net.
Step Size	Modify the start bit or end bit of the alias net, or specify the step size to ensure that the width of the alias net and the width of the selected net are the same. For more information on using step size in net names, see Using Step Size to Connect or Alias Vectored Signals on page 185.

Pullup/Pulldown Information on the Net

Use this dialog box to get a quick snapshot of all pullup/pulldown components attached to the selected net.

How to Access

Do one of the following:

- Double-click in the cell displaying icons for pullups/pulldowns in the Component Connectivity Details pane.
- Select the *Edit Pullup/Pulldown* command in the context sensitive menu for a signal.

Function

The Pullup/Pulldown Information on the Net dialog box is used to provide information about all pullups and pulldowns associated with a net. You can also use this dialog box to add, delete or modify pullups or pulldowns associated to a net.

Pullup/Pulldown Details

The grid box displays information about the design name, net name, type of pullups or pulldowns (including whether inherited or not), references designators and property values for associated components.

The rows corresponding to *Design*, *Net*, *Type*, *Refdes*, and *Value* are editable. You can quickly fill these to add a new pullup/pulldown.

New

Displays the Add Pullup/Pulldown dialog box where you can add a pullup or pulldown and assign it to the selected net.

Delete

Removes the pullup or pulldown associated with the selected row.

Modify

Displays the Add Pullup/Pulldown dialog box where you can change the pullup or pulldown assigned with the selected net. You can also change the pin name and pin numbers.

Qualifier Values

How to Access

Click on the  icon in the qualifier value cell in one of the following dialog boxes:

- [Create Report Template](#)
- [Qualify Report Parameter](#)

Use this dialog box to specify more than one qualifier value for a keyword in a report template, or if you want to use regular expressions in qualifier values.

You can use wildcards and regular expressions in the qualifier values.

If you enter more than one qualifier value in this dialog box, separate the values with commas. For example, if you want to use the qualifier values R* and D*, enter the values as:

R* , D*

Qualify Report Parameter

Use this dialog box to override the qualifier or qualifier value for the driver keyword in a report template when you are generating a report using the report template.

How to Access

This dialog box appears if you have selected the *Override Qualifier Value for Report Driver* check box in the [Generate Report](#) dialog box.

Report Displays the names of the report templates you selected in the *Report Template* list in the [Generate Report](#) dialog box.

Keyword Displays the name of the driver keyword for the report template.

System Connectivity Manager User Guide

Dialog Box Descriptions

Qualifier	<p>Displays the name of the qualifier, if any, for the driver keyword.</p> <p>Change the qualifier for a driver keyword, if required. If a qualifier does not exist for a driver keyword, you can specify a qualifier for the keyword to further refine the data displayed for the keyword in the report. The qualifier serves to limit the query to a specific value or a set of values.</p> <p>To change the qualifier or to specify a qualifier, click on the qualifier cell next to a driver keyword and select a qualifier from the drop-down list.</p> <p>If you select PROP as the qualifier for a keyword, the Select Property dialog box appears. Select the property you want to use as the qualifier for the keyword from the drop-down list, or enter the name of the property. The property name is displayed in the qualifier cell and the  icon in the qualifier cell indicates that the qualifier is a property.</p>
Qualifier Value	<p>Displays the qualifier value for the driver keyword.</p> <p>To change or specify the qualifier value, click on the qualifier value cell next to the driver keyword and do one of the following:</p> <ul style="list-style-type: none">■ Enter the qualifier value in the qualifier value cell. For example, if you select PROP as the qualifier for a keyword, enter the value for the property in the qualifier value cell. You can use wildcards in the qualifier value.■ Click on the  icon in the qualifier value cell if you want to specify more than one qualifier value or if you want to use regular expressions in qualifier values. The <u>Qualifier Values</u> dialog box appears. Here you can enter more than one qualifier value. The query for the driver keyword will be limited to the qualifier value.

Reimport Verilog File

Allows you to import the modifications made to the Verilog file as ECOs in System Connectivity Manager.

How to Access

- Choose *Project – Import – Verilog – ECO*

Verilog Block	Name of the Verilog block to be updated with ECO changes.
Verilog File	Path to the updated Verilog file to be imported in System Connectivity Manager.
Library Name	Design library in which the Verilog file was originally imported as a spreadsheet block. This field is automatically seeded in the dialog box.

Replace (for Verilog Design Editor)

The Replace dialog box allows you to make text substitutions in the Verilog Design Editor.

How to Access

- Choose *Edit – Replace* when the cursor is in the Verilog Design Editor window.

Find what	Enter the text, along with wildcards or regular expressions, for which you want to search. Select the drop-down list to display the last 16 items entered.
Replace with	Enter the text, along with any wildcard or regular expressions, which you want to use as a replacement for the matches to the text entered into the <i>Find what</i> text box. Select the drop-down list to display the last 16 items entered.

System Connectivity Manager User Guide

Dialog Box Descriptions

Match whole word only	When selected, makes replacements only for whole words rather than text within words.
Match case	When selected, the search operation looks only for occurrences that match the uppercase and lowercase characters you enter in the <i>Find what</i> text box.
Regular Expression	When selected, indicates that the use of certain characters in the <i>Find what</i> text box represent notations for patterns of text rather than the literal character.
Replace In	
Selection	Makes replacements only in the selection within the Verilog Design Editor.
Whole File	Makes replacements throughout the file open in the Verilog Design Editor.
Find Next	Skips the current match and moves to the next match for replacement.
Replace	Replaces the current match with the text entered in the <i>Replace with</i> text box.
Replace All	Replaces all matches from a search. A message box appears, listing the total number of replacements.
Mark All	Adds a bookmark in the margin next to each line of code that contains a match for the text entered in the <i>Find what</i> text box.



Caution

Replace All replaces all search matches, including those you have skipped with the Find Next button.

Replace Component	
-------------------	--

Lets you replace one or more instances of a component in the design with another component.



Before replacing components, you must setup the options for replacing components in the Component Replace tab of the Setup dialog box.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Click the *Replace* button in the Component Replace dialog box.

Replacing <library_name:cell_name> with <library_name:cell_name>
view_name view_name Displays the library name, the component or cell name, and the view name of the component you selected in the Component List and the component you want to use to replace the selected component.

The view name `sym_1` indicates version 1 of the symbol view of a component, and the view name `chips` indicates the package view. For example, the text

Replacing `lsttl:ls00.sym_1` with `lsttl:ls00.chips`

indicates that you are going to replace version 1 of the symbol view of the `ls00` component in the `lsttl` library with the package view of the `ls00` component in the `lsttl` library.

Preserve Status

Displays whether the component replace preserve options you selected in the Replace Component tab of the Setup dialog box will be honored when you replace the component.

- The tick icon () next to a preserve option indicates that the preserve option will be honored.
- The cross icon () next to a preserve option indicates that the option will not be honored.

If you want to change the component replace preserve options before replacing a component, click *Cancel* to close the Replace Component dialog box, modify the preserve options in the Replace Component tab of the Setup dialog box, and then replace the component.

Options

Don't show this dialog again, if everything is successful. Select this check box if you do not want System Connectivity Manager to display this dialog box if all the component replace preserve options you selected in the Replace Component tab of the Setup dialog box will be honored when you replace a component.

If you later want System Connectivity Manager to display this dialog box when you replace components, deselect the *Don't show this dialog again, if everything is successful* check box in the Replace Component tab of the Setup dialog box.

System Connectivity Manager User Guide

Dialog Box Descriptions

Done	Click this button to replace the component. The details of the component replace process is displayed in <i>Status Log</i> .
Show Log	Click this button to view the details of the component replacement process in the <i>Status Log</i> .
Hide Log	Click this button if you do not want to view the details of the component replacement process.

Revision History

The Revision History dialog box displays the version history for the selected block or component.

How to Access

To view the version history of the current block:

- Choose *Design – Version History*.

To view the version history of any block or component

- Select the block or component in the Hierarchy Viewer or the Component List, right-click and choose *Version History*.

Revision	Displays the version number of the selected block or component.
Comments	Displays the comments for each version.

Select Columns

This page appears in the import process after the data to be imported is parsed using the delimiter of your choice and the parsed data is displayed in rows and columns. You can now select the columns you want to import and specify appropriate column headers.

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Dialog Box Descriptions

The Select Columns page has the following elements:

Element	Description
Set first row as header	Select this check box to define the first row of the selected import data as the header.
Set pin number as pin name	Select this check box to ensure successful import even if the file being imported does not have a pin_name column, which is a required column for text import.
Data Preview	Displays the data selected for import in tabular format. Select an appropriate header for each column from the drop-down list box displayed in the column. If a column header is not selected, the column is ignored.

Select Delimiter(s)

This page appears in the import process after you have specified the range of data you want to import. On this page, you can select or specify the delimiter that should be used to parse the data. After specifying the delimiter, you can view the parsed data in the *Data Preview* section of this page.

The Select Delimiter(s) page has the following elements:

Element	Description
Delimiters	Specify the delimiter by using the check boxes in this area.
Comma	Select this check box to specify comma as the delimiter.
Space	Select this check box to specify space as the delimiter.
Semicolon	Select this check box to specify semicolon as the delimiter.
Tab	Select this check box to specify tab as the delimiter.
Other	Select this check box to specify any character other than comma, space, semicolon, and tab as the delimiter.
Treat consecutive delimiters as one	Select this check box to allow multiple occurrences of the delimiter to be treated as one occurrence.

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Dialog Box Descriptions

Element	Description
Text Qualifier	Select this check box to import values that contain the characters you have specified as delimiters.

Select Destination

The *Select Destination* page appears after you select the source file from which to import the data. This dialog box enables you to select the location where you want to store the imported data.

Select Footprint

This page appears in the footprint import process. On this page, you can select the footprint you want to import from a list of footprints displayed using `PSMPATH`. The `PSMPATH` is automatically set, if you have Allegro PCB Editor or SiP Layout installed.

Select Property

Lets you select the property you want to specify as the qualifier for a keyword in a report template.

Select Rows

This page appears after you specify the destination of the file to be imported. On this page, you can specify the profile to load and the range of rows to be imported. You can also preview the contents of the file being imported and select or ignore rows for import.

The Select Rows page has the following elements:

Element	Description
Select any profile to load	Displays the name of the profile file to be used
Browse	Enables you to browse and select the profile file to be used

System Connectivity Manager User Guide

Dialog Box Descriptions

Element	Description
Start	Enables you to specify the beginning of the range of rows to be imported. You can specify the following: <ul style="list-style-type: none">■ import at line number■ import at line(s) after line <filter condition>
End	Enables you to specify the end of the range of rows to be imported. You can specify the following: <ul style="list-style-type: none">■ import at line number■ import at line(s) before line <filter condition>
Filter rows beginning with	Specifies the string that the wizard should use to filter the rows that begin with this string
Data Preview	Displays the data selected for import based on the conditions specified using the options displayed on the Select Rows page. You can select or ignore rows from the displayed data by using the options on the pop-up menu.

Select Source

The *Select Source* page appears when you select a import format in the *Import Export* wizard. This dialog box enables you to select the file that contains data in the format selected on the *Import and Export Wizard* page.

Select the Interface File to Import

Use this dialog box to specify the .xml file with the information about the interface data to be imported in the current project in System Connectivity Manager.

Note: This dialog box is available only if you launch System Connectivity Manager from the Cadence SiP Digital Architect GXL or XL product suite.

How to Access

- Choose *Design – Import Co-Design Interface*.

Select File Use this text box to specify the location of the .xml file to be imported.

Select Views

On this page, you can specify if you want Part Developer to generate a symbol for the part that is being created from imported data. You can also select a footprint from a list of footprints displayed using `PSMPATH` and specify if the import settings are to be saved in a profile file.

The Select Views page has the following elements:

Element	Description
Import Data	Displays the number of rows and columns selected for import
Rows to be imported	
Columns to be imported	
Generate	
Generate Chips	This check box is selected by default.
General Symbol	Select this check box to generate a symbol for the part that is being created in the import process.
Associate Footprint	Select this check box to associate a footprint with the part being created.

System Connectivity Manager User Guide

Dialog Box Descriptions

Element	Description
Save Profile As	Click this button to save the settings you specified at various stages of import in a profile file.
Data Preview	Displays the data selected for import in tabular format.

Session Log

Displays the details of activities for the current session. Information displayed includes the design files opened and the time when designs were packaged.

How to Access

Do one of the following:

- Choose *View – Session Log*.
- Press *Ctrl + Alt + L*.

Setup

This dialog box lets you setup various options in System Connectivity Manager. These settings are applicable to every project you open in System Connectivity Manager.

<u>General</u>	Lets you set options for System Connectivity Manager
<u>Spreadsheet Editor</u>	Lets you set options for the table editor
<u>Text Editor</u>	Lets you set the options for the Verilog Design Editor

How to Access

- Choose *Tools – Options*

General

Lets you set the options for System Connectivity Manager

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Choose *Tools – Options*, then select *General*.

On Paste Make New Name as “Copy of...”

If this check box is selected, when you copy a component in the Component List and paste it, System Connectivity Manager assigns the instance name `Copy_1_of_<instance_name>`. If you copy and paste the same object again, System Connectivity Manager pastes it as `Copy_2_of_<instance_name>` and so on.

For example, if you copy a component with the instance name `i18` and paste it, the new instance will have the instance name `Copy_1_of_i18`.

On Paste Prompt Before Overwriting

When you copy and paste something, System Connectivity Manager will prompt you if you are overwriting something during the paste operation.

For example, if you copy a signal from the *Signal List* and paste it in the *Component Connectivity Details* pane, System Connectivity Manager prompts you if the paste operation will overwrite a signal in the *Component Connectivity Details* pane.

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Dialog Box Descriptions

Remove Old Menu when Saving Newer Version

By default, when you save an updated custom menu, System Connectivity Manager creates a separate set of menu entries in the `tddMenus.txt` file for each version of System Connectivity Manager in which the custom menu was updated.

For example, when you customize the menus in System Connectivity Manager Version 15.5, System Connectivity Manager creates a set of menu entries for System Connectivity Manager Version 15.5 in the `tddMenus.txt` file. When you save the updated custom menus in System Connectivity Manager Version 15.5.1, System Connectivity Manager creates another set of menu entries for System Connectivity Manager Version 15.5.1 in the `tddMenus.txt` file.

As a result, when you open System Connectivity Manager Version 15.5, the menu entries for version 15.5 are used from the `tddMenus.txt` file. When you open System Connectivity Manager Version 15.5.1, the menu entries for version 15.5.1 are used from the `tddMenus.txt` file.

If you do not want the set of menu entries for earlier versions of System Connectivity Manager to be retained in the `tddMenus.txt` file when you save the updated custom menu in a later version of System Connectivity Manager, select the *Remove Older Version when Saving Newer Version* check box.

System Connectivity Manager User Guide

Dialog Box Descriptions

Prompt Before Saving Newer Menu Version

If you have customized the menus in an earlier version of System Connectivity Manager, and then open a later version of System Connectivity Manager, the following message box prompts you to save the custom menu when you close System Connectivity Manager:



If you want to click the *No* button and do not want to see this message box the next time you close System Connectivity Manager, select the *Don't show me this message again* check box.

Select the *Prompt Before Saving Newer Menu Version* check box if you later want to be prompted to save the custom menu when you close System Connectivity Manager.

Prompt On Save if Models Used in the Design are Missing

Select this check box, to ensure that a warning message is thrown every time you save the design that has some components with associated models, but the model information cannot be read.

Remember Last Selected Filters

Select this check box to ensure that the information about the filters last used in the Component List pane, Signal List pane, and Connectivity Details panes is retained in System Connectivity Manager.

Use Regular Expressions in Filters

Select this check box to use regular expressions in the filters in the Component List pane, Signal List pane, and Connectivity Details panes. Use regular expressions to create filters that enable you to use advanced pattern matching instead of simple wildcard-based filters.

Spreadsheet Editor

Lets you set options for the spreadsheet editor.

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Dialog Box Descriptions

How to Access

- Choose *Tools – Options*, then select *Spreadsheet Editor*.

Show row numbers in connectivity panes	Select this check box if you want the row numbers to be displayed in the connectivity panes.
Enable Auto Complete for Signal Names	When you type the signal name in the <i>Signal</i> column in the <i>Component Connectivity Details</i> pane, System Connectivity Manager auto completes the signal name based on the letters you have typed in. This lets you quickly capture connectivity information. For example, if the signals CLOCK and CCLOCK are listed in the <i>Signal List</i> , typing the letter C in the <i>Signal</i> column in the <i>Component Connectivity Details</i> pane will auto complete the signal name to CLOCK. If you type the letters CC, System Connectivity Manager auto completes the signal name to CCLOCK.
Show Signal Combo box in CCP signal column	Select this check box if you want to display a drop-down list of signals in the Signal column of the <i>Component Connectivity Details</i> pane. You can select signals from this drop-down list.
Move Selection After Enter Key is pressed in Direction	When you press <i>Enter</i> to finish working in a cell in the Spreadsheet Editor, the current cell remains selected. To move to an adjacent cell when you press <i>Enter</i> , select this select a direction from the drop-down list. For example, to move to the cell below when you press <i>Enter</i> , select <i>Down</i> from the drop-down list.
Show Differential Pair Signals in Signal List pane	Select this check box if you want the differential pair signals to be listed in the Signal List pane. If this check box is clear, instead of differential pairs only member nets are listed in the Signal List pane.
Show Differential Pair Pins in Component Connectivity pane	Select this check box if you want that for all projects, differential pair pins should to be listed in the Component Connectivity Details pane. If this check box is clear, instead of differential pairs, individual component pins are listed in the Component Connectivity Details pane.

Text Editor

Lets you set the options for the Verilog Design Editor.

How to Access

- Choose *Tools – Options*, then select *Text Editor*.

Color	Lets you choose the foreground and background color for regular text and selected text in the Verilog Design Editor.
Foreground	Select <i>Text</i> (to change the color for regular text) or <i>Text Selection</i> (to change the color for selected text), deselect the <i>Automatic</i> check box next to the <i>Foreground</i> list box and click the drop-down list to choose the foreground color for the text. Note: The color you set as the foreground color for regular text becomes the default background color for selected text. To set the default foreground color (black for regular text and white for selected text), select <i>Text</i> or <i>Text Selection</i> , and select the <i>Automatic</i> check box next to the <i>Foreground</i> list box.
Background	Select <i>Text</i> (to change the background color for regular text) or <i>Text Selection</i> (to change the background color for selected text), deselect the <i>Automatic</i> check box next to the <i>Background</i> list box and click the drop-down list to choose the background color for the text. Note: The color you set as the background color for regular text becomes the default foreground color for selected text. To set the default background color (white for regular text and black for selected text), select <i>Text</i> or <i>Text Selection</i> , and select the <i>Automatic</i> check box next to the <i>Background</i> list box.
Font	Lets you choose the font for text in the Verilog Design Editor.

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Dialog Box Descriptions

Choose Font	<p>Click this button to display the <i>Font</i> dialog box. Select the required font and font size.</p> <p>The following fonts are supported in the Verilog Design Editor:</p> <ul style="list-style-type: none">■ Courier■ Courier New■ Fixedsys■ Lucida Console■ Terminal
Reset All	<p>Click this button to reset the color and font settings for regular and selected text in the Verilog Design Editor to their default settings.</p> <p>The default color settings are:</p> <ul style="list-style-type: none">■ Foreground color: Black■ Background color: White <p>The default font settings are:</p> <ul style="list-style-type: none">■ Font: Courier■ Font size: 10
Show Line Numbers	Displays line numbers in the Verilog Design Editor.
Tab Width	Enter the number of space characters each tab or indent represents in the Verilog Design Editor.

Setup

This dialog box lets you set various options for your current project. These settings are applicable only to the current project.

How to Access

- Choose *Project – Settings*

<u>Component Replace</u>	Lets you set the default options to be used when you replace components in System Connectivity Manager.
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Dialog Box Descriptions

<u>Design Rule Checks</u>	Lets you enable design rule checks for connectivity and other errors in the design, and set the error type to be reported in the Violations window for the enabled design rule checks.
<u>Design Verification</u>	Lets you specify the options as to when you want System Connectivity Manager to report: <ul style="list-style-type: none">■ Differences in the version of a component used in the design and the version of the same component in the component library.■ Differences in the version of a read-only block imported into your design and the version of its source block.
<u>Device Models</u>	Lets you specify the default IBIS buffer models that will be assigned to a driver or receiver pin on which you have not specifically assigned an IBIS buffer model.
<u>Differential Pairs</u>	Lets you specify the naming conventions to be used for creating differential pairs in SCM.
<u>Discrete Components</u>	Lets you specify the discrete components (resistors, capacitors and diodes) to be used in terminations.
<u>Document Schematic Generation Setup</u>	Use this dialog box to setup the options for generating the document schematic for your design.
<u>General</u>	Lets you specify the general settings for SCM.
<u>Libraries</u>	Lets you do the following: <ul style="list-style-type: none">■ Select libraries for the project.■ Change the working library for the project.■ Change the root (top-level) design for a project.
<u>Packager</u>	Lets you specify the options for packaging the design.
<u>Paths</u>	Lets you specify the default path for files and directories used by System Connectivity Manager.
<u>Physical Part Table</u>	Lets you add the part table files for your project.
<u>Property Flow</u>	Lets you create, modify and delete user-defined properties, enable or disable the transfer of user-defined properties between System Connectivity Manager and Allegro PCB Editor, and specify the physical netlisting options for the properties.

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Dialog Box Descriptions

<u>Report Generation</u>	Lets you setup the options for formatting reports and to define custom variables you want to use in the headers and footers of reports.
<u>Library Setup (SI Analysis)</u>	Lets you setup signal integrity (SI) model libraries that contain the SI models you want to assign to components and pins in your design and to list the order in which they are searched by SigXplorer.
<u>Verilog NetList</u>	Lets you specify the options for generating the Verilog netlist for simulating the design.

Component Replace

Lets you set the default options to be used when you replace components in System Connectivity Manager.

How to Access

- Choose *Project – Settings*, then select *Component Replace*.

Preserve Options	Lets you specify the preserve options that should be honored when you replace a component. When you replace a component, System Connectivity Manager evaluates whether the preserve options you selected here will be honored and displays the status in the <i>Preserve Status</i> field of the <u>Replace Component</u> dialog box.
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System Connectivity Manager User Guide

Dialog Box Descriptions

Preserve Connectivity	Select this check box if you want that the connectivity should be preserved on the new component. For example, if the signal CBDATA is connected to pin named <code>rclk</code> with the pin number 14 on the original component, the connectivity of the signal CBDATA will be preserved as below: <ul style="list-style-type: none">■ If you are instantiating the new component as a symbol, the signal CBDATA will be connected to a pin that has the name <code>rclk</code> on the new component.■ If you are instantiating the new component as a package, the signal CBDATA will be connected to a pin that has the name <code>rclk</code> and the number 14 on the new component. If the above conditions cannot be met, the connectivity will not be preserved and you have to manually specify the connectivity using the Component Replace dialog box.
Preserve Reference Designator	Select this check box if you do not want the reference designator to be changed when a component is replaced.
Preserve User Properties	Select this check box if you want the properties you added on the original component to be added on to the new component. Note: If the same property exists on the new component, the property on the new component will be honored.
Preserve Terminations	Select this check box if you want the terminations you added on the original component to be preserved after it is replaced.
Preserve Pin Pair	<p> <i>Important</i></p> <p>If you do not select the <i>Preserve Connectivity</i> check box, terminations will not be preserved even if you have selected the <i>Preserve Terminations</i> check box.</p> <p>Select this check box if you want the pin-pairs you added on the original component to be preserved on the new component.</p> <p>Note: The pin-pairs will be preserved only if the new component has the same pin names.</p>

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Dialog Box Descriptions

Preserve Power Group	Select this check box if you want the power group you added on the original component to be preserved on the new component. Note: Power groups will be preserved only if the <code>chips.prt</code> file for the original and the new component have power or ground pins with the same power name.
Preserve Bypass Capacitors	Select this check box if you want the bypass capacitors you added on the original component to be preserved on the new component.
Dialog Options	
Don't show this dialog again, if everything is successful.	Select this check box if you do not want System Connectivity Manager to display the <u>Replace Component</u> dialog box if all the component replace preserve options you selected in this dialog box will be honored when you replace a component.

Design Rule Checks

Lets you enable design rule checks for connectivity problems and other errors in the design, and set the error type to be reported in the *Violations* window for the enabled design rule checks.

How to Access

- Choose *Project – Settings*, then select *Design Rule Checks*.

Design Rule Name	Displays the design rule checks that can be enabled for your design.
JEDEC Type	Checks that the JEDEC_TYPE property exists on every instance in the design.
Unconnected Nets	Reports signals that are not connected to any object.
Single Node Nets	Checks that every signal has at least two nodes (pins) attached to it.
Unconnected Pins	Reports all instances of unconnected pins in the design.
Missing Functions	Reports functions of an asymmetrical/symmetrical part that are not instantiated in the design.

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Dialog Box Descriptions

Missing Section on a Split Part	Reports the sections of a split part that are not instantiated in the design.
Check Option	Lets you enable or disable a DRC and set the error type to be reported in the <i>Violations</i> window for the enabled design rule checks.
Don't Check	Select this option to disable a DRC
Error	Select this option to enable a DRC and specify that an error should be reported in the Violations window if the DRC fails. Error messages indicate a problem in your design that must be corrected before continuing with your work.
Warning	Select this option to enable a DRC and specify that a warning message should be reported in the Violations window if the DRC fails. Warning messages indicate that there may be something wrong with your design—a potential error condition. You need to verify the warning and correct the problem, if required.
Information	Select this option to enable a DRC and specify that an information message should be reported in the Violations window if the DRC fails. Information messages provide information about your design and do not indicate a problem or potential problems in your design.

Design Verification

Lets you specify the options as to when you want System Connectivity Manager to report:

- Differences in the version of a component used in the design and the version of the same component in the component library.
- Differences in the version of a read-only block imported into your design and the version of its source block.

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Dialog Box Descriptions

How to Access

- Choose *Project – Settings*, then select *Design Verification*.

Run whenever a design is loaded	Select this check box if you want System Connectivity Manager to report changes in the versions of components in your design and read-only blocks imported into your design, only when you open the design in System Connectivity Manager.
Run at fixed intervals	<p>Select this check box if you want System Connectivity Manager to report changes in the versions of components in your design and read-only blocks imported into your design, at specified time intervals.</p> <p>Select the time interval from the drop-down list.</p>

Device Models

Use this dialog box to specify the default IO Cell models that will be assigned to a driver or receiver pin on which you have not specifically assigned an IO Cell model.

How to Access

- Choose *Project – Settings*, then select *Device Models*.

Default IO Cell Models	Displays the default IO Cell models for the six pinuse types: IN, OUT, BI, TRI, OCL, and OCA. Click the browse button next to the default model row for each pinuse type to select another IOCell model using the <u>SI Model Assignment</u> dialog box.
IN	Defines the default IOCell model for a pin with the PINUSE property value of IN. The default is CDSDefaultInput.
OUT	Defines the default IOCell model for a pin with a PINUSE property value of OUT. The default is CDSDefault Output.
BI	Defines the default IOCell model for a pin with a PINUSE property value of BI. The default is CDSDefaultIO.
TRI	Defines the default IOCell model for a pin with a PINUSE property value of TRI. The default is CDSDefaultTristate.

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Dialog Box Descriptions

OCL	Defines the default IOCell model for a pin with a PINUSE value of OCL. The default is CDSDefaultOpenDrain.
OCA	Defines the default IOCell model for a pin with a PINUSE value of OCA (open source). The default is CDSDefaultOpenSource.
Retain Existing Xnets and DiffPairs	This option is not applicable to System Connectivity Manager.

Differential Pairs

Use this for specifying the naming convention for differential pair pins as well as differential pair signals.

How to access

- Choose *Project – Settings* and in the Setup dialog box, select *Differential Pairs*.

Formats for naming Differential Pair Pins	Use this grid to specify the characters that are used as suffixes or prefixes with the pin names to indicate the pins of a differential pair.
Negative Pin	Use this column to specify the characters used to indicate the negative pin in the differential pin pair.
Location	Specify whether the characters entered in the Negative Pin column are added as a suffix or a prefix to the pin name.
Positive Pin	Use this column to enter the characters used to indicate the positive pin in a differential pair.
Location	Specify whether the characters entered in the Positive Pin column are added as a suffix or a prefix to the pin name.

For example, it may happen that in a design component, `_L` and `_H` are used to indicate the negative and positive pins of a differential pair pin. In the same design, another component might use `+` and `-` as prefixes to indicate the negative and positive pins of a differential pair pin. To ensure that appropriate pins of both the components are displayed

System Connectivity Manager User Guide

Dialog Box Descriptions

as differential pin pairs, you need to specify both the naming conventions in the setup dialog box, as shown in the table below.

Table A-1 Sample values in the Differential Pair Pin Syntax

Negative Pin	Location	Positive Pin	Location
_L	SUFFIX	_H	SUFFIX
-	PREFIX	+	PREFIX

Similarly, there can be many different combinations used by different companies to name differential pair pins in a component. [Table A-2](#) on page 797 lists the formats commonly used for naming differential pair pins or signals. Depending on the components used in your design, you may have multiple entries in the Formats for Naming Differential Pair Pins grid.

Table A-2 Commonly Used Differential Pairs Naming Conventions

Negative pins/signals are specified using ...	Positive pins/signals are specified using ...	as...
_L	_H	Suffix
_LOW	_HIGH	Suffix
_NEG	_POS	Suffix
_N	_P	Suffix
-	+	Suffix
-	+	Prefix

Format for Naming Differential Pair Signals

Use this grid to specify the characters that should be used as suffixes or prefixes with the signal names to indicate the member nets of a differential pair. SCM uses the differential pair signal naming convention specified in this grid when you add differential pair signals using the *Add Signal(s)* dialog box and also while capturing connectivity with the [Auto-connect differential pairs in Connectivity panes](#) option selected.

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Dialog Box Descriptions

Negative Signal	Specify the characters used to indicate the negative member net in the differential pair.
Positive Signal	Enter the characters used to name the positive member net in a differential pair.
Location	Specify whether the characters entered in the Negative and Positive signal columns will be added as a suffix or a prefix to the pin name.
Prefixes For Differential Pair Names	Use this text box to specify the prefix to be used while naming the differential pair for signals and pins.
For Pins	Specify the prefix to be used for naming differential pair for pins. For example if you enter DP_ as the prefix, the differential pair name for pins vin1+ and vin1-, is DP_vin1. If the prefix value is not specified, the differential pair name is vin1.
For Signals	Specify the prefix to be used for naming differential pair for signals.
Auto-connect differential pairs in Connectivity panes	Select this check box to ensure that when you connect one member net of a differential pair signal to a differential pair pin, the second member net automatically gets connected to the unconnected pin of a differential pair pin.

Important

Auto-connection works only if the component pin of the differential pair is unconnected. If a connection already exists, the existing connection is not replaced.

Discrete Components

Use this dialog box to associate library components for the resistors, capacitors, or diodes that will be used in terminations. These components will appear as available options when you are defining terminations or other discrete components for any component.

How to Access

- Choose *Project – Settings*, then select *Discrete Components*.

System Connectivity Manager User Guide

Dialog Box Descriptions

Resistor	Associate the library component for the resistor to be used in terminations. To associate a new component, click <i>Browse</i> . Part Information Manager opens where you can select a resistor. Note: If you have associated a resistor or capacitor to be used in terminations, the <i>Property Name For Value</i> field becomes active. The default name seeded in this field is VALUE . Typically, you may like to retain this. If required, change it by entering a new value.
Capacitor	Associate the library component for the capacitor to be used in terminations. You can use the <i>Browse</i> button to select a new component from Part Information Manager.
Diode	Associate the library component for the diode to be used in terminations. You can use the <i>Browse</i> button to select a new component from Part Information Manager.
Inductor	Associate the library component for the inductor to be used in terminations. You can use the <i>Browse</i> button to select a new component from Part Information Manager.

General

Remove violations from the Violations window if fixed	Select this check box to ensure that once the violations are fixed, they are removed from the Violations window.
Show vectors using	Use this option to specify the vector notation to be used for naming vector signals in your design. System Connectivity Manager provides support for using square or angular brackets for naming vector signals and pins. Note: For the new signals added to the design, the vector notation influences the physical net names generated automatically by System Connectivity Manager. However, changing vector notation does not automatically change the physical net names for the existing signals in the design.

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Dialog Box Descriptions

[] Select this option if you want to use square brackets in the vector signals in the design.

With this option selected, the vector signals as displayed as shown in the figure below.

 add[1]	ADD[1]
 add[2]	ADD[2]
 add[3]	ADD[3]
 add[4]	ADD[4]
 build[1]	BUILD[1]
 build[2]	BUILD[2]
 build[3]	BUILD[3]

< > Select this option if you want to use angular brackets in the vector signals in the design.

Export Interface This option is used when you export interface data of a BGA to a xml file.

Note: This option is enabled only if you are using the Cadence SiP Digital Architect XL or GXL licenses.

Export Local Signals as Inout Signals Select this check box to ensure that any local signal connected to the component pin of the BGA are exported as Inout pins.

Libraries

Lets you do the following:

- Select libraries for the project
- Change the working library for the project.
- Change the root (top-level) design for a project

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Dialog Box Descriptions

How to Access

- Choose *Project – Settings*, then select *Library*.

Project Name	Displays the name of the current project.
Project Location	Displays the location of the project.
Working Library Name	Displays the library that contains the current root design (top-level design) for the project. To change the root design, select a library from the drop-down list (only the working libraries for the current project are available in this list), and then specify the root design in the <i>Design Name</i> field.
Design Name	Displays the root (top-level) design for the project. To change the root design for the current project, click the browse button and select a design.
Reference Lib Location	Displays the <code>cds.lib</code> file for the project. The <code>cds.lib</code> file is created by System Connectivity Manager when you create the project. The <code>cds.lib</code> file determines the list of available libraries from which you choose the libraries for your project.
Reference Libraries	
Available Libraries	Available Libraries are the libraries available for the project. The available libraries are determined by the directives in the <code>cds.lib</code> file.
Project Libraries	Project Libraries are the libraries you select for your project from the <i>Available Libraries</i> list. You can use only the components in the project libraries in your design.
Add	Adds the libraries selected in the <i>Available Libraries</i> list to the <i>Project Libraries</i> list. To select more than one library, select a library, then press <i>Ctrl</i> or <i>Shift</i> and select the other libraries.
Remove	Removes the selected libraries from the <i>Project Libraries</i> list. To select more than one library, select a library, then press <i>Ctrl</i> or <i>Shift</i> and select the other libraries.
Add All	Adds all libraries in the <i>Available Libraries</i> list to the <i>Project Libraries</i> list.

System Connectivity Manager User Guide

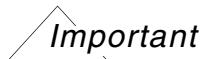
Dialog Box Descriptions

Remove All	Removes all the libraries from the <i>Project Libraries</i> list.
Up	Moves up the selected library in the <i>Project Libraries</i> list. The order in which the libraries are listed in the <i>Project Libraries</i> list determines their search order.
Down	Moves down the selected library in the <i>Project Libraries</i> list. The order in which the libraries are listed in the <i>Project Libraries</i> list determines their search order.

Packager

Lets you specify the options for packaging the design.

Note: The changes you make in the packager setup will impact only the future changes you make to the design. For example, a change in the reference designator prefix is applied only to the new components you add in the design. The reference designators of components that exist in the design will not be updated with the new reference designator prefix.



If you make any changes in the packager setup, you must close and reopen the project in System Connectivity Manager for the changes to become effective.

How to Access

- Choose *Project – Settings*, then click *Packager*.

Reuse Reference Designator's Numbers Select this check box if you want the reference designators for changed or deleted components to be reused for new components.

For example, suppose that you have four components in your design with reference designators U1, U2, U3, and U4 respectively. If you delete a component with the reference designator U3 and then add another component in your design, the reference designator U3 will be reused for the newly added component if this check box is selected. If this check box is not selected, the reference designator for the newly added component will be U5.

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Dialog Box Descriptions

Default Reference Designator Prefix	<p>Specify the default prefix for reference designators for components. System Connectivity Manager assigns a reference designator that has two parts, the base name as defined by the default reference designator prefix value and a number that is appended by System Connectivity Manager. For example, if you specify D as the default prefix for reference designators, the reference designators for components will start from D1, D2, D3, and so on.</p> <p>By default, System Connectivity Manager uses U as the reference designator prefix.</p> <p>Note: If the PHYS_DES_PREFIX property exists on a component, System Connectivity Manager assigns a reference designator that has two parts, the base name as defined by the PHYS_DES_PREFIX property and a number that is appended by System Connectivity Manager.</p> <p>Note: A change in the reference designator prefix is applied only to the new components you add in the design. The reference designators of components that exist in the design will not be updated with the new reference designator prefix.</p>
Reference Designator Length	<p>Specify the maximum number of characters for reference designators.</p> <p>By default, System Connectivity Manager uses a maximum of 31 characters for defining reference designators. You can have a maximum of 255 characters for reference designators.</p>
Physical Part Name Length	<p>Specify the maximum number of characters for defining physical part names.</p> <p>By default, System Connectivity Manager uses a maximum of 31 characters for defining physical part names.</p>
Net Name Length	<p>Specify the maximum number of characters for physical net names.</p> <p>By default, System Connectivity Manager uses a maximum length of 31 characters for defining net names.</p>

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Dialog Box Descriptions

Block Suffix Separator Select the separator to be suffixed to the reference designators of components in blocks, when System Connectivity Manager updates the reference designators of components in blocks.

By default, the underscore (_) character is used as the suffix separator. For example, if you add a block named `MEMORY` (that has a component with the reference designator `U1`) by selecting the *Use Suffix* option and entering `MEMORY` as the suffix in the Block Packaging Options dialog box, System Connectivity Manager automatically updates the reference designator of the component in the block as `U1_MEMORY`. The valid characters are: Plus (+), Underscore (_), Hyphen (-), Equals (=).

Note: A change in the block suffix separator is applied only to new blocks you add in the design. The reference designators of components that exist in the existing blocks will not be updated with the new block suffix separator, unless you change the packaging options for the block in the Block Packaging Options dialog box.

You can also define a different character to be suffixed to the reference designators by specifying the directive `SD_SUFFIX_SEPARATOR` in the `.cpm` file. For more information, refer to the `SD_SUFFIX_SEPARATOR` section of the *Allegro Front-End CPM Directive Reference Guide*.

System Connectivity Manager User Guide

Dialog Box Descriptions

Block Prefix Separator Select the separator to be prefixed to the reference designators of components in blocks, when System Connectivity Manager updates the reference designators of components in blocks.

By default, the underscore (_) character is used as the prefix separator. For example, if you add a block named `MEMORY` (that has a component with the reference designator `U1`) by selecting the *Use Prefix* option and entering `MEMORY` as the prefix in the Block Packaging Options dialog box, System Connectivity Manager automatically updates the reference designator of the component in the block as `MEMORY_U1`. The valid characters are: Plus (+), Underscore (_), Hyphen (-), Equals (=).

Note: A change in the block prefix separator is applied only to new blocks you add in the design. The reference designators of components that exist in the existing blocks will not be updated with the new block prefix separator, unless you change the packaging options for the block in the Block Packaging Options dialog box.

You can also define a different character to be prefixed to the reference designators by specifying the directive `SD_PREFIX_SEPARATOR` in the `.cpm` file. For more information, refer to the `SD_PREFIX_SEPARATOR` section of the *Allegro Front-End CPM Directive Reference Guide*.

Valid Net Characters

Specify special (non-alphanumeric) characters that can be used in defining physical net names.

- Click *Add* to display the *Add Valid Net Characters* dialog box, specify a valid character and click *OK* to add the character.
- Select a character from the list and click *Remove* to remove the character.

Paths

Lets you specify the default path for files and directories used by System Connectivity Manager.

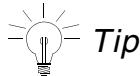
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Dialog Box Descriptions

How to Access

- Choose *Project – Settings*, then select *Paths*.

Temporary Directory	Specify the path to the directory in which Cadence tools store temporary files. If you do not specify a temporary directory, Cadence tools use the <code>temp</code> directory in your project directory.
PPT Option Set	Specify the path to the PPT Option Set file that you want System Connectivity Manager to use by default. This file stores the default display settings for physical properties in the design.
Category Path	Specify the path to the directory that contains the category (.cat) files used to organize components by category. The component categories are displayed in the <i>Category View</i> tab of the Part Information Manager dialog box. Part Information Manager also loads the category files located in the libraries that you use in your project. For more information on category files, see the <i>Allegro Design Entry HDL Libraries Reference</i> .



Tip

You can create and modify Category files using the Library Explorer tool. For more information, see the *Library Explorer User Guide*.

Physical Part Table

Use the Part Table tab to add or remove Physical Part Table (.ptf) files from a project. You can either add .ptf files directly or add directories that contain .ptf files. For example, if the `lsttl` directory contains the `lsttl.ptf` file, you can add either the complete path to the `lsttl.ptf` file or just the path to the `lsttl` directory. When you add a directory, all the .ptf files in that directory are added to the project. You can then exclude the ones you do not want.

System Connectivity Manager User Guide

Dialog Box Descriptions

How to Access

- Choose *Project – Settings*, then select *Physical Part Table*.

Physical Part Table Files Displays the .ptf files (and directories containing .ptf files) currently selected for this project.

Brings up the Add Physical Part Table dialog box, which you use to add .ptf files or directories that contain .ptf files.



To add a .ptf file, type its name and path in the *Enter physical part table file (.ptf) or directory to add* field, or click *File* and use the file browser to select the file. (If you type the path to more than one file, separate each path with a space; to select more than one file with the file browser, select the first file, then press *CTRL* and select the other files.)

To add a directory, type its name and path in the *Enter physical part table file (.ptf) or directory to add* field, or click *Directory* and use the file browser to select the directory. (If you type the path to more than one directory, separate each path with a space.)

When you add a directory, all the .ptf files contained in it are included in your project, unless you exclude some files with the *Exclude Part Table Files* option.



Removes the selected file or directory from the list of Physical Part Table files for the current project.

Exclude Part Tables

Use this option if your Physical Part Table Files list includes directories that contain several .ptf files and you want to exclude some of the files from your project. Use either this option to exclude files or the *Include Part Tables* option to include the files you want.

Add

Brings up the Exclude Physical Part Table dialog box.

Type the name of the part table file you want to exclude, then click *OK*. You can enter more than one file name; separate each name with a space. The files are added to the list of excluded files.

Remove

Removes the selected file from the *Exclude Part Tables* list.

System Connectivity Manager User Guide

Dialog Box Descriptions

<i>Include Part Tables</i>	Use this option if your Physical Part Table Files list includes directories that contain several .ptf files and you want to choose some files from them. Use either this option to include files or the Exclude Part Tables option to exclude unwanted files.
<i>Add</i>	Brings up the Include Physical Part Table dialog box. Type the name of the part table file you want to include, then click <i>OK</i> . You can enter more than one file name; separate each name with a space. The files are added to the list of included files.
<i>Remove</i>	Removes the selected file from the <i>Include Part Tables</i> list.
<i>Use Cell Level Physical Part Table Files</i>	Select this check box to include cell-level .ptf files for all the cells in the project. All the .ptf files contained in the Part Table view of the cells will be read by System Connectivity Manager.
<i>Merge Physical Part Table Files</i>	Select this check box to merge the information in all included Physical Part Table files. If this is not selected, and there is more than one file in the Physical Part Table Files list that has entries for the same components, the entry in the last file is picked up. If this is not selected, and the Use Cell Level Physical Part Table Files check box is selected, the .ptf files at the cell level are picked up.
<i>Perform Case-Sensitive Row Match</i>	Select this check box to perform a case-sensitive match of key properties for a part in the Physical Part Table files.

Property Flow

How to Access

- Choose *Project – Settings – Property Flow*.

When you click the *Property Setup* button, the *Setup Property Definitions* dialog is displayed.

For more information about the *Setup Property Definitions* dialog, refer to the [Tools – Setup Property Definitions](#) section of the *Allegro Constraint Manager Reference* guide.

Report Generation

Use this tab to setup the options for formatting reports and to define custom variables you want to use in the headers and footers of reports.

How to Access

Do one of the following:

- Choose *Project – Reports – Generate Reports* to display the *Generate Report* dialog box. Click *Setup* to display this dialog box.
- Choose *Project – Settings* to display the *Setup* dialog box. Click *Report Generation*.

General Settings tab

Use this tab to setup the options for formatting reports.

General

Report Format	Lets you specify the default format in which reports are generated in System Connectivity Manager. For example if you select DSR, the DSR (Editable Report File) option in the <u>Generate Report</u> dialog box will be selected by default. This means that by default, all reports will be generated in the .DSR format, unless you select another report format option in the <u>Generate Report</u> dialog box.
Sort Order	Specifies the order in which the data in the reports are sorted. Select: <ul style="list-style-type: none">■ <i>Ascending</i>, to sort the data in the reports in ascending order.■ <i>Descending</i>, to sort the data in the reports in descending order.
Currency Symbol	Enter the currency symbol you want to use in reports.
Hide Line Numbers	Select this check box if you do not want line numbers to be displayed in the generated reports.

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Dialog Box Descriptions

Report Location	Enter the path to the directory where you want the generated reports to be saved or click the browse button to select the directory. By default, reports are saved in the <code>reports</code> folder in the project directory.
Separator	
Column Separator	Enter the character you want to use as the column separator in reports generated in the Text File in Tabular Form report format.
Row Separator	Enter the character you want to use as the row separator in reports generated in the Text File in Tabular Form report format.
Column Pad	Enter the number of characters you want to use as the column pad in reports generated in the Text File in Tabular Form report format. The column pad is the space between two columns in the report.
Header Separator	Enter the character you want to use as the separator for column headings in reports generated in the Text File in Tabular Form report format.
Font	Select the font you want to use for displaying data in reports and specify the font settings.

Custom Variables tab

Use this tab to define the custom variables you want to use in the headers and footers of reports.

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Dialog Box Descriptions

Name	<p>Enter the name of the custom variable.</p> <p>Note: When you use a custom variable in the header or footer of a report, you must enclose the custom variable name in angle brackets. For example, if you have defined a custom variable named <code>USER_NAME</code> with the value <code>John Edwards</code>, you must enter the custom variable as <code><USER_NAME></code> when you enter the header or footer information in the Header/Footer dialog box.</p> <p>For more information on defining custom variables, see Defining Custom Variables for Headers and Footers in Reports on page 549.</p>
Value	<p>Enter the value of the custom variable.</p> <p>For example, if you define a custom variable named <code>CONF</code> with the value <code>CONFIDENTIAL</code> and then use the variable <code><CONF></code> in the report footer, System Connectivity Manager displays the text <code>CONFIDENTIAL</code> in the report footer when you preview or print the report.</p> <p>For more information on adding headers and footers in reports, see Adding Headers and Footers in Reports on page 544.</p>

Document Schematic Generation Setup

Use this dialog box to setup the options for generating the document schematic for your design.

Note: When you generate the document schematic, the schematic blocks in your design in System Connectivity Manager will be copied without any changes into the document schematic. Hence the options you specify in this dialog box will not have any effect on the pages created for the schematic blocks in the document schematic.

How to Access

Do one of the following:

- Choose *Project – Settings* to display the Setup dialog box. From the list, select *Document Schematic Generation*.
- Choose *Project – Generate Schematics* to display the Document Schematic Generation dialog box. Click the *Setup* button to display the Document Schematic Generation Setup dialog box.

General tab

Schematic Settings Allows you to specify the placement options for generating the document schematic.

Note: When you generate the document schematic, the schematic blocks in your design in System Connectivity Manager are copied without any changes into the document schematic. Therefore, placement options do not have any effect on the pages created for these schematic blocks in the document schematic. For example, while the connections in the document schematic are specified using net names, pages created for a schematic blocks in the document schematic can have component instances routed using wires.

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Dialog Box Descriptions

Create and add symbols for hierarchical blocks

Select this check box if you want block symbols to be added for the hierarchical blocks in a design.

If this check box is not selected, block symbols will not be added to the design.

For example, consider a root design `top` that instantiates five components and two blocks. If this check box is not selected, the generated schematic for `top` will only have five components. To add symbols for the two blocks, you need to select the *Create and add symbols for hierarchical blocks* check box.

Important

If you are planning to export the schematics, ensure this option is enabled for hierarchical designs.

Report an error if proper symbol is not found for any instance in the design or if the instance has packaging errors.

Select this check box if you want the schematic generation process to stop and flag an error when problems are encountered due to incorrect symbol or packaging errors.

If this check box is not selected, warning messages are thrown for instances with errors and the schematic generation process continues for rest of the design.

System Connectivity Manager User Guide

Dialog Box Descriptions

Include Block Diagram Select this check box if you want to add schematic block diagrams to the generated document schematic.

You might want the first page or the first set of pages in the document schematic to contain a block or flow diagram of the design, or introductory information of the design like company name, design name, designer name, date of creation, date of last modification, and so on.

Note: You can create schematic pages containing block diagrams using Design Entry HDL. Cadence recommends that the page border symbol you use for the schematic pages containing the block diagrams is the same as the page border symbol you selected in the Symbols tab.

Selecting this check box enables the Library and Cell text boxes.

1. Click the *Browse* button to display Part Information Manager.
2. Select the cell whose sch_1 view contains the schematic pages for the block diagram and click *Add*.

When you generate the document schematic, the schematic pages existing in the schematic view of the cell are automatically added as the first set of pages in the document schematic.

For example, assume that you have a root design named **CPU** with a block named **ALU**. If you specify that the block diagram schematic pages in the cell **CPU_BLK** in the **DIAG** library be included in the document schematic, then the document schematic first displays the pages in the **CPU_BLK**, then the pages for the **CPU** design, and finally the pages for the **ALU** design.

Note the following:

- System Connectivity Manager uses only the pages from the sch_1 view of the cell containing the schematic pages for the block diagram when generating the document schematic. The pages in additional schematic views such as sch_2, sch_3, and so on, will be ignored.

System Connectivity Manager User Guide

Dialog Box Descriptions

- The sch_1 view of the cell containing the schematic pages for the block diagram must contain the page*.csb files for the schematic pages.

If you do not have the page*.csb files for the block diagram, but have the page*.csa files for the block diagram, open the page*.csa files in Design Entry HDL and save the files to generate page*.csb files.

Page Border Information file

Use this text box to specify the customized exclude areas while generating document schematic. The page border information is read from the crefer.dat file specified in the text box.

Project Schematic

Allows you to specify the setup options for project-level document schematic.

Stop document schematic generation for the project if block level document schematic is not available.

Select this check box, if you want the schematic generation process to stop and an error to be flagged, when the block for which the document schematic is to be created does not have an existing document schematic.

If this check box is not selected, the documentation schematic is generated with a warning message.

Symbols tab

Use this tab to specify the default symbols that should be used for generating the document schematic. The library, cell and view of the selected symbols are displayed.

Note the following:

- The default symbols are selected from the Cadence standard library. If you want to use symbols from the standard library, ensure that the standard library is defined in the cds.lib for your project and added to the list of project libraries. You can add libraries for the project using the Libraries tab of the Setup dialog box.
- If the specified page border symbol is not found in the library, the document schematic will not be generated.
- If the default TAP or OFFPAGE symbols are not found in the library, System Connectivity Manager generates the symbols in the design library where the cell for the root or top-level design exists.
- You can use only symbol version 1 (sym_1 view) of the CTAP symbols. Even if you select other symbol versions for these symbols in Part Information Manager, System

System Connectivity Manager User Guide

Dialog Box Descriptions

Connectivity Manager will use only symbol version 1 of these symbols in the generated schematic.



If you are selecting symbols from any library other than the Cadence standard library, ensure that the symbols conform to the Cadence library standards described in the *Allegro Design Entry HDL Libraries Reference*.

Page Border	Specifies the page border symbol that will be used in the document schematic.
Ctap	<p>Specifies the TAP symbol that will be used in the document schematic.</p> <p>The TAP symbol must have:</p> <ul style="list-style-type: none">■ Exactly two pins.■ The pin names of both the pins must have the \NAC property and the pin name of the first pin must also have the \NWC property. <p>For example, if the first pin is named B and the second pin is named S, enter the pin names as B \NAC \NWC and S \NWC.</p> <ul style="list-style-type: none">■ The first pin must be at the origin of the symbol and must not have the BN property.■ The second pin must be on the x-axis and must have the BN property.■ The second pin must have a positive x-coordinate and be on the grid. <p>Note: Select the TAP component from the Cadence standard library if the TAP component in your library does not meet these requirements.</p>

System Connectivity Manager User Guide

Dialog Box Descriptions

Add Offpage Symbols Select this check box to include offpage symbols in the generated document schematic.

Selecting this check box enables the options for specifying the input, output and inout offpage symbols to be used on the left and right side of the document schematic.



The default symbols are from the Cadence standard library.

Input	Specifies the offpage symbol that will be used in the document schematic as INPUT offpage.
Output	Specifies the offpage symbol that will be used in the document schematic as OUTPUT offpage.
InOut	Specifies the offpage symbol that will be used in the document schematic as INOUT offpage.
Browse	<p>Use this button to launch Component Browser for specifying custom offpage connectors.</p> <ul style="list-style-type: none">■ Click the Browse button.■ In Part Information Manager select the symbol to be used as offpage connector and click OK.
Rotate By	<p>Use this drop-down list when you want to rotate a symbol by the 180 degree before using it as an offpage connector in your document schematic.</p> <p>For example, you can use this option to ensure that the input offpage symbol used on the right side of the document schematic is the same as the input offpage symbol used on the left-side but rotated by 180°.</p> <p>To rotate a symbol:</p> <ol style="list-style-type: none">a. Use the Browse button to specify the required offpage symbol.b. From the <i>Rotate By</i> drop-down list select the value by which you want the symbol to be rotated.

Note: Only 180 degree rotation is supported.

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Dialog Box Descriptions

Properties tab

Default Alignment	<p>Specifies the default option for aligning properties in the generated document schematic.</p> <p>Note the following:</p> <ul style="list-style-type: none">■ If System Connectivity Manager is unable to align notes or properties using the default option in the generated document schematic, it will place them where it finds adequate space in the generated document schematic.■ The alignment setting specified for a property on the symbol for a component will always win irrespective of the settings you specify here. For example, if the alignment for a property on the symbol is set to <i>Right</i>, the property will be right aligned on the document schematic even if you select <i>Left</i> as the default option in the <i>Default Alignment</i> field.
Size	<p>Specify the size of the text to be used for displaying properties in the schematic.</p> <p>The text size should be specified in 5000ths of an inch. The default size is 41.</p>
Default Visibility	<p>Specifies the default option for displaying property names and values in the generated document schematic.</p> <p>Select:</p> <ul style="list-style-type: none">■ None, if you do not want to display the names and values of properties.■ Name, if you want to display only the names of properties.■ Value, if you want to display only the values of properties.■ Both, if you want to display the names and values of properties. <p>Note: The visibility setting specified for a property on the symbol for a component will always win irrespective of the settings you specify here. For example, if the visibility of a property on the symbol is set to <i>Both</i>, the name and value of the property is displayed on the document schematic even if you select <i>Value</i> as the default option in the <i>Default Visibility</i> field.</p>

Colors tab

Use this tab to specify the colors for the drawing objects in the document schematic.

Note: Cadence recommends that the colors you select here are the same as the color settings you have specified for new drawing objects in Design Entry HDL. This will ensure that new drawing objects you add in the document schematic have the same colors as the existing objects in the document schematic. To specify color settings for new drawing objects in Design Entry HDL, choose *Tools – Options* in Design Entry HDL to display the Design Entry HDL Options dialog box. Select the Color tab to specify color settings for new drawing objects.

Color For Drawing Objects	Displays the color used for component symbols, wires, properties, comments, and the bounding box that will be drawn around associated components in the generated document schematic. <ul style="list-style-type: none">■ To change the color for an object, click on the color for the object to display the color palette. Click on the color you want to use in the color palette.■ To select the default color for an object, click on the color for the object to display the color palette. Click <i>Default</i> in the color palette.
Symbol Color	Displays the default color for component instances in the generated document schematic.
Wire Color	Displays the default color for wires in the generated document schematic.
Property Color	Displays the default color for properties in the generated document schematic.
Comment Color	Displays the default color for comments in the generated document schematic.
Bounding Box Color	Displays the default color for the bounding box that will be drawn around associated components in the generated document schematic if the <i>Use Bounding Box Around Associated Components</i> check box is selected in the <u>General tab</u> .

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Dialog Box Descriptions

Comments tab

Use this tab to specify the options for displaying comments on the document schematic.

Add Comments as Notes	Select this check box if you want comments in System Connectivity Manager to appear as notes in the generated document schematic.
Usage Options	Lets you select the objects whose comments should appear as notes in the document schematic.
Instance Comments	Select this check box if you want comments added on instances to appear as notes in the document schematic.
Pin Comments	Select this check box if you want comments added on pins to appear as notes in the document schematic.
Content Options	Lets you select the fields of a comment you want to appear in the note in the document schematic.
Text	Select this check box if you want the text of a comment to appear in the note in the document schematic.
Author	Select this check box if you want the name of the author of a comment to appear in the note in the document schematic.
Time	Select this check box if you want the time when the comment was added to appear in the note in the document schematic.
Date	Select this check box if you want the date on which the comment was added to appear in the note in the document schematic.

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Dialog Box Descriptions

Power tab

Use this tab to specify the options for displaying power symbols on the generated document schematic.

Use Power Symbols

By default, the signal names of power nets (nets with voltage property) are displayed in the document schematic.

Select this check box if you want power symbols to be displayed in the document schematic for power nets.



Tip

To ensure that the VOLTAGE property specified on a net is available in the generated document schematic, it is recommended that power symbols should be used in the generated document schematic. Using power symbols ensures that, the VOLTAGE property is attached to the power pin in the generated schematic.

Power Net

Displays the list of power nets in the design. You can select the power symbol for power nets.

To select the power symbol for a power net

1. Select the power net for which you want to select a power symbol to be used in the document schematic.
2. Click the *Browse* button.

Part Information Manager appears.

3. Select the power symbol you want to use and click *Add*.

To select the same power symbol for more than one power net

1. Select the power nets for which you want to use the same power symbol.

To select more than one power net, press the *Shift* or *Ctrl* key and click on the power nets.

2. Click the *Browse* button.

Part Information Manager appears.

3. Select the power symbol you want to use and click *Add*.

To delete the power symbol selected for a power net

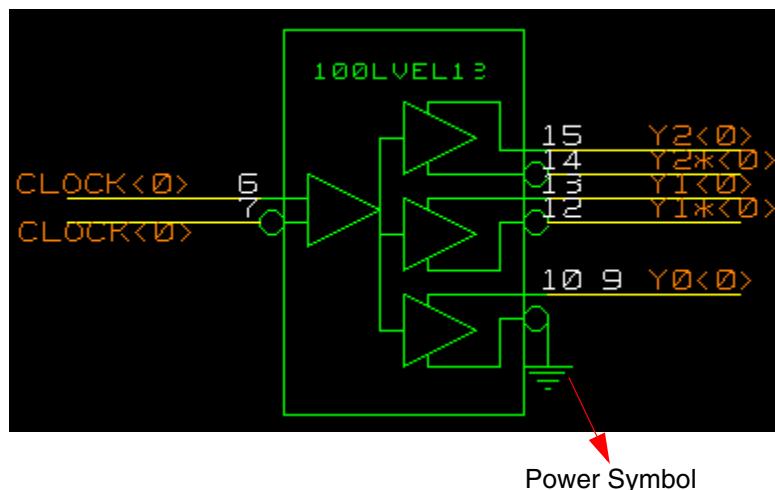
1. Select the power net and click the *Delete* button.

To delete the power symbol selected for more than one power net

1. Select the power nets and click the *Delete* button.

To select more than one power net, press the *Shift* or *Ctrl* key and click on the DC nets.

For example, if you select the `gnd_power` component from the Cadence standard library as the power symbol for a power net named GND, the GND signal is displayed in the document schematic as shown below:



Placement tab

Use this tab to specify the component placement options for placing components on the generated document schematic.

Component Group Placement

Allows you to specify the options for placing grouped components on the generated document schematic

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Dialog Box Descriptions

Place each group of components on a separate page	Select this check box if you want the component groups, specified using the SCHEMATIC_GROUP property, be placed on different pages of the document schematic. If this check box is not selected, the component groups are placed in a manner that ensures maximum utilization of the schematic pages.
Grid Size	Specify the grid size to use in the generated schematic. Note: This grid size is used internally by the Schematic Generator (schgen) and is independent of the grid size specified in Design Entry HDL.
Page Margins	Specify the page margins in grid multiples to determine the drawing area.
Top	Specify the top-most point on the desired drawing area as a multiple of the grid size.
Left	Specify the left-most point on the desired drawing area as a multiple of the grid size.
Bottom	Specify the bottom-most point on the desired drawing area as a multiple of the grid size.
Right	Specify the right-most point on the desired drawing area as a multiple of the grid size.
Component to Component Spacing	Specify the grid spacing between any two components, as a multiple of the grid size.

Associated Components tab

Use this tab to specify the placement and grouping options for placing associated components on the generated document schematic.

Maximum Number of Component in a Rail for	Associated components are placed as rails in generated document schematic. This section allows you to specify the number of associated components to be added in a single rail.
Bypass Capacitor	Specify the number of bypass capacitors to be added in a rail of bypass capacitors. The default value used for this option is 100.
Pullups	Specify the number of pullups to be added in a single rail.

System Connectivity Manager User Guide

Dialog Box Descriptions

Pulldowns	Specify the number of pull down resistors to be added in a single rail in the generated document schematic.
Terminations	Allows you to specify the number of terminations, such as shunt termination, to be grouped together as rails in the generated document schematic. By default, 5 a rail has five components.
Shunt	Specify the number of shunt terminations to be put together in a rail.
Series	Specify the number of series terminations to be put together in a rail.
Shunt RC	Specify the number of ShuntRC terminations to be put together in a rail.
Thevenin	Specify the number of Thevenin to be put together in a rail.
Ground Clamp	Specify the number of ground clamps to be put together in a rail.
Dual Clamp	Specify the number of dual clamps to be put together in a rail.
Power Clamp	Specify the number of power clamps to be put together in a rail.
Rail Pitch	Allows you to specify the space between two components in a rail
Number of Grids for Rail Pitch	<p>Use this text box to specify the space between two associated components in a rail. The spacing is specified in terms of grid. Therefore, actual spacing on the DEHDL page is calculated as:</p> $\text{number of grids} \times \text{grid size}$ <p>Note: Same value of the rail pitch is used for creating rails for all associated components.</p>

Routing tab

Use this tab to specify the routing options for the generated document schematic.

Stub Length for nets on the left	Use this text box to specify the maximum stub length for the nets that are connected to a pin on the left of the component. The value entered by you is the number of grids, therefore, the actual stub length is calculated as number of grids \times grid size.
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System Connectivity Manager User Guide

Dialog Box Descriptions

Stub Length for nets on the right	Specify the maximum of grids that can be used for drawing stubs for the nets connected to the pins on the right of the component.
Add dots at points of net short	Select this check box to ensure that net to net connections are indicated with a dot.
Short NC nets	Select this check box to ensure that the generated document schematic has all the unconnected pins short together.
Flatten all nets	Select this check box to flatten all nets in the generated schematic
Handle Concatenated Signals	Select this check box if you want to add a prefix to signals in case of concatenation of signal names.
Signal name prefix to be used for concatenation	Specify the value to prefix to the signal names in case of concatenation.
Show NC for unconnected bits	Select this check box if you want show NC for unconnected bits in the generated schematic.

Cross Referencer tab

Use this tab to specify the Cross Referencer settings.

Run Cross Referencer on Project Schematic	Select this check box if you want to run cross referencer on project-level document schematic. If this check box is selected, cross references are added to the project schematic. Selecting this check box enabled the <i>Cross Referencer Setup</i> button.
Cross Referencer Setup	Click this button to open the Cross Reference Options dialog box, used for specifying the options for running Cross Referencer.

Ports tab

Use this tab to specify the Port settings. These options enable you to specify the symbols for the input, output and inout port symbols to be used in the document schematic.



If you are selecting symbols from any library other than the Cadence standard library, ensure that the symbols conform to the Cadence library standards described in the *Allegro Design Entry HDL Libraries Reference*.

Input	Specifies the offpage symbol that will be used in the document schematic as INPUT offpage.
Output	Specifies the offpage symbol that will be used in the document schematic as OUTPUT offpage.
InOut	Specifies the offpage symbol that will be used in the document schematic as INOUT offpage.
Browse	<p>Use this button to launch Component Browser for specifying custom offpage connectors.</p> <ul style="list-style-type: none">■ Click the Browse button.■ In Part Information Manager select the symbol to be used as offpage connector and click OK.

Library Setup (SI Analysis)

Lets you setup signal integrity (SI) model libraries that contain the SI models you want to assign to components and pins in your design and to list the order in which they are searched by SigXplorer. The signal integrity device model library files contain the device models SigXplorer uses to build circuit simulations.

Libraries are searched starting at the top of the list. If a model is included in two or more libraries, you can use the search order to determine which library the SigXplorer searches first. SigXplorer uses the first model found.

You can also use this dialog box to set a particular library as the working library. A working library is the only library to which SigXplorer can add models. If you want to add to a library that is not the working library, you must make it the working library before you start the process of adding the model.

How to Access

- Choose *Project – Settings*, then select *Signal Integrity*.

System Connectivity Manager User Guide

Dialog Box Descriptions

■ Choose Tools – Signal Integrity – SI Library Setup



Displays a dialog box that lets you add a directory that contains signal integrity device model library (.DML) and device model library index (.NDX) files.

Note: Ensure that there are no spaces in the name of the .DML or .NDX file you are adding.

The standard Cadence signal integrity model libraries are installed at:

```
<install_dir>/share pcb/signal/SignalPartLib
```

For more information on the standard signal integrity model libraries, see the *SPECCTRAQuest Simulation and Analysis Reference*.

Removes the selected directory from the list.



Displays the Library Management dialog box that you can use to view and manage the .DML and .NDX files.



Moves up the selected directory in the list.

SigXplorer locates models by searching the libraries in the order in which they are listed.

If a model with the same name exists in more than one library, you change the search order to ensure that the correct model is used by SigXplorer.



Moves down the selected directory in the list. The order in which the libraries are listed determines their search order.

System Connectivity Manager User Guide

Dialog Box Descriptions

Working	<p>Displays the current working (active) library for the project. A working library is the library to which the models you create or the default models generated by System Connectivity Manager for discrete devices will be added.</p> <p>Note: When you create a project, System Connectivity Manager creates a default device model library named <code>devices.dml</code> in the project directory and sets it as the working library.</p> <p>Note: SigXplorer adds models to the working library only. Before you edit or add new models in a library, set the library as the working library.</p>
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Library Management

Library Name	Displays a list of signal integrity device model library (.DML) or device model library index (.NDX) files in the directories specified in the Library Setup (SI Analysis) dialog box.
Working Library check box	Select the check box next to the library that you want to specify as the working directory.
Ignore Library check box	Select the check box next to the library if you want to ignore the library during Signal Integrity analysis.
Launch Model Integrity	Launches Model Integrity for the selected .DML file.

Verilog NetList

Lets you specify the options for generating the Verilog netlist for simulating the design.

How to Access

- Choose *Project – Settings*, then select *Verilog Netlist*.

Ignore Bypass Capacitors	Select this check box if you want bypass capacitors in the design to be ignored when creating the netlist.
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System Connectivity Manager User Guide

Dialog Box Descriptions

Ignore Terminations	Select this check box if you want terminations in the design to be ignored when creating the netlist. Note: The nets connected to the pins of a resistor used in a series termination are aliased in the netlist.
Ignore Pull-ups / Pull-downs	Select this check box if you want Pull-ups and Pull-downs in the design to be ignored when creating the netlist.
Single File Netlist	If you have a hierarchical design, select this check box to generate a single file netlist named <code>verilog.v</code> that contains the modules for all the blocks in the hierarchical design. The single file netlist is created in the <code>sim_tb1_1</code> view of the root design for the project. Generating a single netlist file for the hierarchical design lets you simultaneously simulate all the blocks in the hierarchical design. If this check box is not selected, System Connectivity Manager generates separate netlist files named <code>verilog.v</code> in the <code>sim_tb1_1</code> view for each block in the hierarchical design. Generating separate netlist files for each block lets you separately simulate each block in the design.
Uppercase Identifiers	Select this check box to write all lowercase identifiers such as module names, signal names and instance names in uppercase in the netlist.
Position Mapping	Select this check box to map pins and model ports by position (based on the port order) in the Verilog netlist. If this check box is not selected, pins and ports will be mapped by name in the Verilog netlist. For more information on position mapping, see the description for the <code>PORT_ORDER</code> property in the <i>Allegro Platform Properties Reference</i> .
Regenerate Configuration	Select this check box to regenerate the <code>cfg_verilog</code> configuration view for the root design in the project.

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Dialog Box Descriptions

Ignore Component With Property	<p>Ignores the components that have the specified property when netlisting the design.</p> <p>For example, if you specify a property, say IGNORE_VERILOG, in the text box, all the components in the design on which the IGNORE_VERILOG property exists are ignored when netlisting the design.</p> <p>Note: Use upper case letters to specify the property name to be ignored.</p>
Default Net Type	<p>Specify the default logic type for all nets in the design. You can use any legal Verilog net type, such as WIRE, WAND, and WOR. The default value is WIRE.</p> <p>The specified net type applies to all the nets in the design. You can override the net type for individual nets by using the VLOG_NET_TYPE property on the nets.</p> <p>For more information on the VLOG_NET_TYPE property, see the <i>Allegro Platform Properties Reference</i>.</p>
Max Errors	<p>Specify the maximum number of netlisting errors that you want to allow in the design. The default number is 50.</p> <p>If the number of netlisting errors in the design exceeds the number specified here, System Connectivity Manager will not generate the netlist.</p>
Time Scale	<p>Specify the default time scale directive for the Verilog module. The default value is 1ns/1ns.</p> <p>The time scale directive specifies the time unit and time precision of the modules that follow it. The time unit is the unit of measurement for time values such as the simulation time and delay values.</p>
Name	<p>Displays the list of global signals in the design that are treated as Supply 0 or Supply 1 nets.</p>

System Connectivity Manager User Guide

Dialog Box Descriptions

Supply0	<p>Displays the list of signals to be treated as Supply 0 nets in the netlist.</p> <p>By default, the global signals in the design that have a voltage value less than 1.8 Volts are selected as Supply 0 nets.</p> <p>Do one of the following:</p> <ul style="list-style-type: none">■ Clear the check box next to a signal if you do not want to treat it as a Supply 0 net.■ Select the check box next to a signal to treat it as a Supply 0 net.
Supply1	<p>Displays the list of signals to be treated as Supply 1 nets in the netlist.</p> <p>By default, the global signals in the design that have a voltage value equal to or more than 1.8 Volts are selected as Supply 1 nets.</p> <p>Do one of the following:</p> <ul style="list-style-type: none">■ Clear the check box next to a signal if you do not want to treat it as a Supply 1 net.■ Select the check box next to a signal to treat it as a Supply 1 net.

SI Model Assignment

Lets you assign signal integrity (SI) models to components and pins in your design.

How to Access

Select a component or pin, right-click and choose *SI Models – Assign Models*.

SI Library	Lists the SI model libraries you have added for your project using the Library Setup (SI Analysis) dialog box.
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System Connectivity Manager User Guide

Dialog Box Descriptions

SI Model	<p>Lists the SI models in the libraries that are selected in the <i>SI Library</i> list.</p> <ul style="list-style-type: none">■ To display only the models in a specific library, select the library in the <i>SI Library</i> list. If you select more than one library in the <i>SI Library</i> list, all the models in the selected libraries are displayed.■ To search for models by name, select * in the <i>SI Model</i> drop-down list, enter a search string using the wildcard characters * and ?, and then press <i>Enter</i> to display only the models that meet the search criteria.
Model Type	<p>Displays the model type for the models listed in the <i>SI Model</i> list.</p> <ul style="list-style-type: none">■ To display only the models of a specific type, choose the model type in the <i>Model Type</i> drop-down list and press <i>Enter</i>. <p>You can select * in the <i>Model Type</i> drop-down list, enter a search string using the wildcard characters * and ?, and then press <i>Enter</i> to display only the models that belong to that model type.</p>

Update Block Location

The designer who is working on the block you have imported into your design as a read-only block might move the design containing the source block for the read-only block to a new location. If the location of the source block for a read-only block changes, Hierarchy Viewer displays the  icon next to the name of the block, when you do one of the following:

- Open the design in which you have imported the read-only block in System Connectivity Manager.
- Select the Run at fixed intervals check box in the Design Verification tab of the **Setup** dialog box.

The Update Block Location dialog box lets you specify the new location for the source block for the read-only block.

How to Access

- Select the read-only block in the Hierarchy Viewer, right-click and choose *Update Block Source*.

Select Block

Using Project File (*.cpm)	Select this option if you want to specify the location of the source block from another project (.cpm) file, then enter the name and path to the .cpm file for the project in the <i>Location</i> field or click the browse button to select the .cpm file.
Using Library File (cds.lib)	Select this option if you want to specify the location of the source block from another cds.lib file, then enter the name and path to the cds.lib file in the <i>Location</i> field or click the browse button to select the cds.lib file.

User Defined Columns

Use this dialog box to create or edit user-defined query fields that can be used in report templates. For more information on user-defined query fields, see [Creating User-Defined Query Fields](#) on page 523.

How to Access

Do one of the following:

- Choose *Project – Reports – Create Custom Column*.
- Run the dsreportgen -ccol command from the command line.

For more information on the using the dsreportgen command, see [Using the dsreportgen Command](#) on page 550.

Existing Columns	Displays the names of the existing user-defined query fields.
Location	Displays the location of the file for the selected user-defined query field.

System Connectivity Manager User Guide

Dialog Box Descriptions

Edit	Select a user-defined query field in the <i>Existing Columns</i> list and click this button to modify the user-defined query field. The <u>User Defined Query Field</u> dialog box appears. Here you can modify the user-defined query field.
New	Click this button to display the <u>User Defined Query Field</u> dialog box appears. Here you can create a new user-defined query field.

User Defined Query Field

Use this dialog box to create and edit user-defined query fields that you can use in report templates. For more information, see [Creating User-Defined Query Fields](#) on page 523.

How to Access

- Choose *Project – Reports – Create Custom Column* to display the User Defined Columns dialog box. Click the *New* button or select a user-defined query field in the *Existing Columns* list and click the *Edit* button.
- Click the *Create New Field* button in the Create Report Template dialog box.

Field Name	Enter the name of the user-defined query field. Note: Do not use spaces in the name. Also, do not enter a name that is the same as that of a standard query field. For more information on standard query fields, see Standard Query Fields on page 517.
Standard Query Fields	Displays the fields that can be used to generate data for the report. These fields can be added as keywords in the report. For more information on the standard query fields, see Standard Query Fields on page 517.
Query Grid	The keywords in the query grid, and the query and format settings for each keyword in the query grid determine how data will be displayed in your report. You can add the standard query fields as keywords in the query grid.
Query	Displays the query settings for the keywords in the report.

System Connectivity Manager User Guide

Dialog Box Descriptions

Keyword	Add keywords in the query grid. For more information, see Adding a Keyword in the Query Grid for User-Defined Query Fields on page 525.
Dependency	Specify the dependency for the keywords you add in the query grid. For more information, see Specifying the Dependency for a Keyword on page 526.
Qualifier	Specify the qualifier for the keywords for which you want to limit the query to a specific value or a set of values. For more information, see Specifying the Qualifier for a Keyword on page 527.
Qualifier Value	Specify the qualifier value for each qualifier. For more information, see Specifying the Qualifier for a Keyword on page 527.
Total	Lets you display the total of the data for the column in the report. Select this check box in the column for a keyword if you want the total count for the keyword to be displayed in the report. The total number of objects found for the keyword is displayed in the bottom of the report. The heading for the row in the report where the total count is displayed is named TOTAL.
Format	Displays the format settings for the keywords in the report. The format settings determine how data is displayed in the report.
Title	The default title for each keyword is displayed in the <i>Title</i> cell in the column for each keyword. The title for a keyword is used as the column name for the keyword in the report. You can modify the title for a keyword.
View Order	Specify the view order for the keywords in the <i>View Order</i> row. The <i>View Order</i> row displays the order in which the columns for the keywords are displayed in the report. The keyword whose view order is 1 is displayed as the first column in the report, the keyword whose view order is 2 is displayed as the second column in the report, and so on. You can modify the view order of the keywords.

System Connectivity Manager User Guide

Dialog Box Descriptions

Sort Order	<p>Specify the sort order for the keywords in the <i>Sort Order</i> row.</p> <p>The <i>Sort Order</i> row displays the order in which the data in the columns in the report are sorted. The data in the columns in the report will be first sorted by the keyword whose sort order is 1, then by the keyword whose sort order is 2, and so on.</p> <p>You can modify the sort order of the keywords.</p> <p>Note: The sort order must be a continuous sequence starting with 1.</p>
Width	<p>Specify the width for the keywords in the <i>Width</i> row.</p> <p>The <i>Width</i> row displays the width that will be used for displaying the column for each keyword in the report. The default width is 20 characters.</p>
Alignment	<p>Specify the alignment for the keywords in the <i>Alignment</i> row.</p> <p>The <i>Alignment</i> row displays how the text in the column for each keyword will be aligned in the report. The default alignment is LEFT.</p> <p>To modify the alignment for a keyword, click on the alignment cell in the column for the keyword, and choose the alignment type from the drop-down list.</p>
Visible	<p>Select this check box if you want the column for the keyword to be displayed in the report. Clear this check box if you do not want the column for the keyword to be displayed in the report.</p>

Violations

Displays the error, warning, and informational messages that occur while working in System Connectivity Manager.

How to Access

Do one of the following:

- Choose *View – Violations*.

System Connectivity Manager User Guide

Dialog Box Descriptions

- Press *Ctrl + Alt + V*.

Warnings	Clear this check box if you do not want warning messages to be displayed in the Violations window.
Informations	Clear this check box if you do not want informational messages to be displayed in the Violations window.
Serial Number	Lists the number of the error in the current session.
Type	Displays the severity of the message and the message number. The severity of a message can be Error, Warning or Information. System Connectivity Manager uses the following colors for differentiating between messages: <ul style="list-style-type: none">■ Red color for error messages■ Orange color for warning messages■ Green color for informational messages Click on the message number to view more information on the message.
Time	Lists the time when the error occurred.
Design	Displays the name of the design or block in which the error exists.
Message	Displays the message.
Action	If the error can be automatically corrected, the <i>Resolve</i> button is enabled. Click the <i>Resolve</i> button to automatically correct the error. If the error cannot be automatically corrected, the <i>Resolve</i> button is disabled.

Note the following:

- To sort the data in a column, click the column heading for the column.
- To highlight the objects causing the error, warning or informational message, double-click on the row for the message. If the object is in a block that is not open, System Connectivity Manager opens the block and highlights the object.

Visual Design Differences

Use the Visual Design Differences pane to view and update differences between the logical design and the board.

How to Access

Do one of the following:

- Click *OK* in the *Import Physical* dialog box, and click *Preview*.
- Choose *View – Visual Design Differences*

You might have run *Import Physical* during the current session. Use this command if you want to view the differences in the Visual Design Differences pane during the current session.

Note: If you close a project and reopen it in System Connectivity Manager and then choose *View – Visual Design Differences*, the Visual Design Differences pane will not display any differences.

- Press *Ctrl + Alt + I*

Filter	Let you display differences belonging to a particular category.
All	Displays all the differences between the logical design and the board.
Components	Displays the differences between the components in the logical design and the board. For more information, see Component Differences on page 488.
Nets	Displays the differences between the signals in the logical design and the board. For more information, see Net Differences on page 489.
Ref. Des.	Displays the differences between the reference designators in the logical design and the board. For more information, see Reference Designator Differences on page 490.

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Dialog Box Descriptions

Section	Displays the differences between the sections in the logical design and the board. For more information, see Section Differences on page 490.
Pins	Displays the differences between the pins in the logical design and the board. For more information, see Pin Differences on page 491.
Connectivity	Displays the connectivity differences between the logical design and the board. For more information, see Connectivity Differences on page 492.
Constraints	Displays the differences between constraints in the logical design and the board. For more information, see Design Constraint Differences on page 493.
Constraint Objects	Displays the differences between constraint objects in the logical design and the board. For more information, see Constraint Object Differences on page 496.
Constraint Association	Displays the differences between constraint objects in the logical design and the board. For more information, see Constraint Association Differences on page 497.
Update	Updates all the differences. The Merging Design Differences in Design Editor box displaying the progress of the update process. Click the Details button if you want to view the details of the update process. Click the same button again to hide the details. After the differences are updated, a tick icon (✓) appears next to the difference in the <i>Status</i> column and the difference is grayed out.
Options	

System Connectivity Manager User Guide

Dialog Box Descriptions

Highlight	Select a difference and choose this command to highlight the object (component, pin or signal) causing the difference. The object is highlighted in System Connectivity Manager and in Constraint Manager. If it is a property difference, the object is highlighted in Constraint Manager.
Dehighlight	Select a difference and choose this command to dehighlight the object (component, pin or signal) causing the difference. The object is dehighlighted in System Connectivity Manager and in Constraint Manager. If it is a property difference, the object is highlighted in Constraint Manager.
Status	Indicates whether a difference is successfully updated. If a difference is updated, a tick icon (✓) icon appears next to the difference in the <i>Status</i> column.
	This icon appears next to a difference. Click this icon to display the Collections or Dependencies dialog box. For more information on the Collections or Dependencies dialog box, see Icons in the Visual Design Differences Pane on page 481.
Object	<p>Displays the name of the object causing the difference.</p> <ul style="list-style-type: none">■ If the object causing the difference is a component, the reference designator of the component is displayed.■ If the object causing the difference is a section of a component, the reference designator of the component and the section number is displayed in the format <refdes>#<section_number>. For example, if the reference designator of the component is U1 and the section number is 4, the object name is displayed as U1#4.■ If the object causing the difference is a pin, the reference designator of the component and the pin number is displayed in the format <refdes>.<pin_number>. For example, if the reference designator of the component is U1 and the pin number is 4, the object name is displayed as U1.4.■ If the object causing the difference is a net, the physical net name of the net is displayed.

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Dialog Box Descriptions

System Connectivity Manager	Displays the value in the logical design in System Connectivity Manager.
	<ul style="list-style-type: none">■ If a component or net exists in System Connectivity Manager but not in the board, the System Connectivity Manager column displays a icon (✓).■ If a component or net does not exist in System Connectivity Manager but exists in the board, the System Connectivity Manager column displays a cross icon (✗).■ For all other differences, the value in the logical design is displayed.

Zoom

Use this dialog box to change the magnification of different objects in the Component List and Signal List. As you increase or decrease the magnification the size of objects displayed on the computer screen will increase or decrease.

How to Access

- Choose *View – Zoom*.

Function

The Zoom dialog box increases or decreases the size of objects displayed in the selected pane. You can have a different magnification for different panes. For example, you can set the

System Connectivity Manager User Guide

Dialog Box Descriptions

Component List to have magnification of 150% and the Signal List to have magnification of 125%.

Customizing Termination Templates

If you are generating document schematic for a design that has terminations added on the differential pair pins, then the document schematic generated for the differential pair terminations is based on the predefined schematics that are available for all differential pair terminations supported in System Connectivity Manager. In the installation hierarchy, these predefined schematics are available at `<install_dir>/share/cdssetup/tdd/termination_templates`.

In case you want to modify the default schematic for a termination type, you need to modify the schematic template for that differential pair termination.

The procedure for editing the default schematic is as listed below.

1. Copy the default template to be modified on your local disk.

For details, see [Copy the Template to be Modified](#).

2. Make changes to ensure that the symbols used in the template schematics are accessible as a project library.

For details, see [Setting up the Library](#).

3. Create a blank project is DE-HDL.

For details, see [Modifying Default Template Schematic in Design Entry HDL](#).

4. Copy the .csb file to be modified as page of the DE-HDL project.

For details, see [Modifying Default Template Schematic in Design Entry HDL](#).

5. Use the modified template schematic for generating documentation schematic for table-based designs.

Copy the Template to be Modified

To update the default template, supplied with the installation, you need write permissions for the files in the `termination_templates` folder. For this, copy the appropriate `.csb` file at a location where you have write permission.

The steps to be followed are:

1. Set the value of CDS_SITE environment variable to point to a location where you specify the default options to be used for projects created on your machine.

To know more CDS_SITE environment variable and the directory structure of the folder pointed to by the CDS_SITE environment variable, see [Site Project File](#) on page 93.

2. Copy the folder containing the default template from *install_dir/share/cdssetup/tdd/termination_templates* to *\$CDS_SITE/cdssetup/tdd/termination_templates*.

The schematic templates used for generating document schematic for a differential pair termination are available in the /termination_templates/schematic_templates folder as .csb files.

Setting up the Library

To open the default schematic template files in DE-HDL for editing, you need to ensure that the symbols used in these .csb pages are available in one of the project libraries. These symbols are available in the *\$CDS_SITE/cdssetup/tdd/termination_templates/symbol* folder.

To make the symbols available in one of the project libraries, modify the *cds.lib* available at *\$CDS_SITE/cdssetup* using the step listed below.

- Modify the *cds.lib* located at *\$CDS_SITE/cdssetup* by adding the following line.

```
DEFINE symbols ./tdd/termination_templates/symbols
```



Tip
The DEFINE statement should be added before the INCLUDE statement in *cds.lib*.

Modifying Default Template Schematic in Design Entry HDL

To modify the schematic template associated with the differential pair termination, you need to open the .csb file in Design Entry HDL.

1. Launch Design Entry HDL.
2. Create a blank new project.
3. Save the project and exit Design Entry HDL.

4. In the project folder, open the sch_1 view.

The folder will have page1.csa and page1.csb files.

5. Delete all page1.* files from the folder.

6. Copy the .csb file to be modified as page1.csb in the sch_1 view.

For example, to modify the default template for DPSeries termination, first copy DPSeries.csb in the sch_1 view, and then rename DPSeries.csb as page1.csb.

7. Open the project in Design Entry HDL.

8. Make the required changes in the schematic page.

9. Save the design and exit Design Entry HDL.

10. Copy the updated page1.csb from the sch_1 view, rename it to its original name, and paste it in the \$CDS_SITE/cdssetup/tdd/termination_templates/schematic_templates folder.

If you now generate the documentation schematic for a design with DPSeries termination, the generated schematic for the differential pair termination will be based on the schematic saved by you in step 9.

Do's and Don'ts While Modifying Template Schematic

It is recommended that template schematic should only be modified to make changes, such as adjusting the placement of components or nets to reduce the drawing size. Rerouting is not recommended.

- You can increase or decrease the spacing between two components or nets.
- You can adjust the spacing of the labels associated with nets or components.
- Do not modify the name of the .csb file. The capitalization of name should be preserved.

For example, if the name of the default .csb file is DPSeries.csb, it is recommended that after modification the name should not be changed to dpseries.csb.

- Do not delete any component or net.
- Do not modify the value of \$location property on components.
- Do not modify the value of SIG_NAME property on nets.
- Do not modify the TMPL_PIN property on the pins of the discrete symbols. This property is used to map the pins of the dummy symbols to the pins of the actual symbols.

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Customizing Termination Templates

- It is recommended that you should not reroute or replace the symbols used in the template schematic. However, in case this is to be done, ensure that appropriate properties are added on the component, pins, and nets of the template schematic to ensure that the connectivity defined in `csdesigntemplates.txt` file located at `<install_dir>/share/cdssetup/tdd` is maintained.

For example, if you are modifying the template schematic for AC-Coupled Transmission Line (ACCT2), you need to ensure the following:

- The resistors should have the value of the `$location` property set to `I1` and `I2`.
- Both the pins of resistor `I1` should have `TMPL_PIN` property attached to them, and the property value should be set to `T1` and `T2`, respectively.
- Resistor pin for which the value of the `TMPL_PIN` property is set to `T1` needs to be connected to net with `SIG_NAME` property set to `N1`.
- Similarly, the resistor pin with `TMPL_PIN` property set to `T2` must be connected to the net with `SIG_NAME` property set to `N3`.
- The value of the `$location` property for the two capacitors should be set to `I3` and `I4`.

The table below lists the connectivity and the property values that must be attached to each pin of the discrete components used in the template schematic for the differential pair termination, ACCT2.

Instance	Pins	Property attached...	Connected to net with...
I2	Pin1	<code>TMPL_PIN = T1</code>	<code>SIG_NAME = N2</code>
	Pin 2	<code>TMPL_PIN = T2</code>	<code>SIG_NAME = N3</code>
I3	Pin1	<code>TMPL_PIN = T3</code>	<code>SIG_NAME = N1</code>
	Pin2	<code>TMPL_PIN = T4</code>	<code>SIG_NAME = N4</code>
I4	Pin1	<code>TMPL_PIN = T3</code>	<code>SIG_NAME = N2</code>
	Pin2	<code>TMPL_PIN = T4</code>	<code>SIG_NAME = N5</code>

Verilog Netlist for Parts

This chapter introduces you to asymmetrical parts and split parts. Because of technological advances, it is now possible to have parts that have different logic for different sections. Such parts are called asymmetrical parts. Some parts also have the pincount going up to a few thousands of pins. Such parts are called large pin count devices. In this chapter, we will see how these System Connectivity Manager creates a verilog netlist for designs with asymmetrical parts and split parts.

Types of Parts

The parts covered in this chapter are:

- [Split Part](#)
- [Asymmetrical Part](#)
- [Multi-Section Parts with Common Pins](#)

Split Part

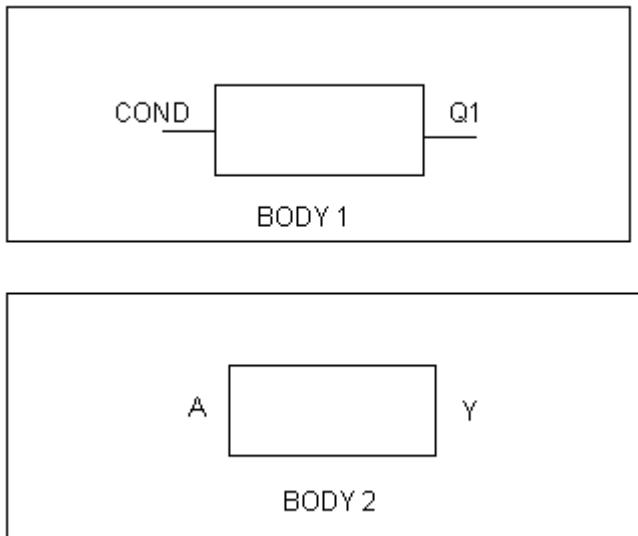
Whenever a device has a large pincount, it becomes impossible to instantiate the complete part as a single symbol in a schematic. Therefore, these parts are usually broken or split into multiple body drawings. Parts that can split into multiple symbols are called split parts.

In SCM, you can instantiate a split part either as a package or as a symbol. When instantiated as a package, both the hierarchical and the flat netlist has single instance of the part. The netlist is generated based on the reference designators used for split parts.

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Verilog Netlist for Parts

Figure C-1 Block Diagram Representing Split Parts



Asymmetrical Part

Parts that have different logic within a single package, such as an IC, are called asymmetrical parts. These parts are represented using multiple symbols where each symbol represents one logical function. You can simulate each section of an asymmetrical part individually.

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Verilog Netlist for Parts

Figure C-2 Asymmetrical Parts with Common Pins

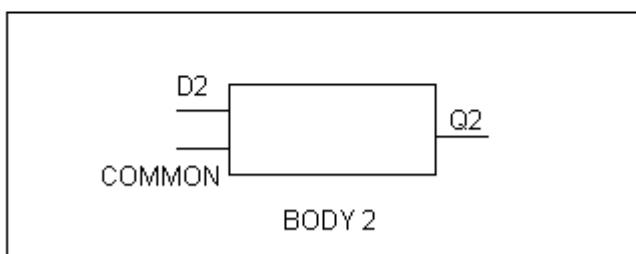
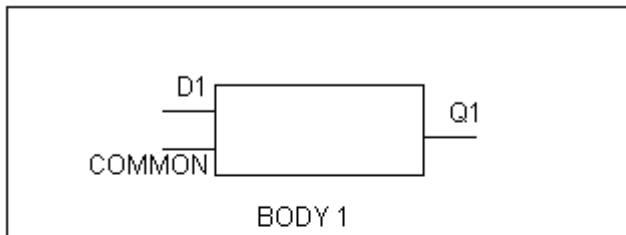
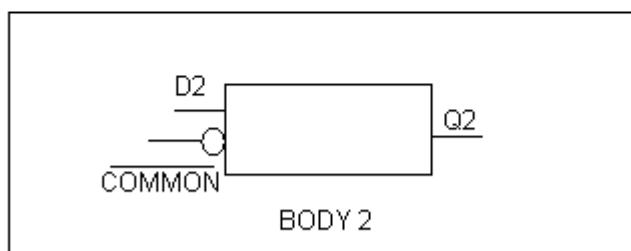
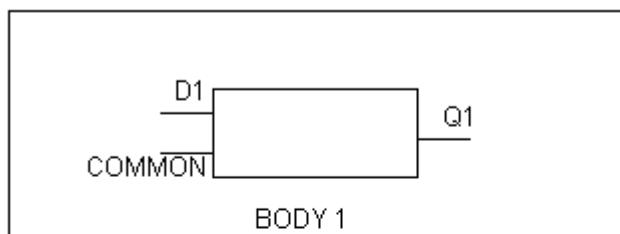


Figure C-3 Asymmetrical Parts with Different Assertions



Note: An asymmetrical part is split according to different logical units within it. Therefore, an asymmetrical part can be a split part but all split parts are not asymmetrical. A major difference between split parts and asymmetrical and multi-section parts and is that split parts

do not have the SECTION property attached to them whereas asymmetrical and multiple section parts have the SECTION property attached to them.

Multi-Section Parts with Common Pins

These are parts with multiple bodies having a common pin. These parts can be simulated separately.

Multi-section parts with common pins have the same assertion for the common pins. This is unlike asymmetrical parts that have different assertions for common pins.

Examples

Example of Split Parts

An example of the `chips.prt` file for a split part developed using Part Developer is shown below.

```
FILE_TYPE=LIBRARY_PARTS;
TIME=' Created/Modified on Wed May 15 11:51:58 2002' ;
primitive 'SPLITPART_NOCMMNPIN_DIP';
pin
'A1':
  PIN_NUMBER='(1,0,0)';
  INPUT_LOAD='(-0.01,0.01)';
  PIN_GROUP='1';
'A2':
  PIN_NUMBER='(2,0,0)';
  INPUT_LOAD='(-0.01,0.01)';
  PIN_GROUP='1';
'B1':
  PIN_NUMBER='(0,3,0)';
  INPUT_LOAD='(-0.01,0.01)';
  PIN_GROUP='1';
'B2':
  PIN_NUMBER='(0,4,0)';
  INPUT_LOAD='(-0.01,0.01)';
  PIN_GROUP='1';
'C1':
  PIN_NUMBER='(0,5,0);
```

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Verilog Netlist for Parts

```
INPUT_LOAD='(-0.01,0.01)';
PIN_GROUP='2';
'C2':
PIN_NUMBER='(0,6,0)';
INPUT_LOAD='(-0.01,0.01)';
PIN_GROUP='2';
'D1':
PIN_NUMBER='(0,0,7)';
INPUT_LOAD='(-0.01,0.01)';
PIN_GROUP='2';
'D2':
PIN_NUMBER='(0,0,14)';
INPUT_LOAD='(-0.01,0.01)';
PIN_GROUP='2';
end_pin;
body
NC_PINS='(13,12,11,10,9,8)';
CLASS='IC';
PART_NAME='SPLITPART_NOCMMNPIN';
PHYS_DES_PREFIX='U';
JEDEC_TYPE='dip14_3';
SWAP_INFO='(S1+S2+S3)';
end_body;
end_primitive;
END.
```

If you instantiate this part in system Connectivity Manager, the logical verilog netlist generated is as shown below.

```
splitpart_nocmmnpin_dip U1 (.a1/* unconnected */,
.a2/* unconnected */,
.b1/* unconnected */,
.b2/* unconnected */,
.c1/* unconnected */,
.c2/* unconnected */,
.d1/* unconnected */,
.d2/* unconnected */);
```



Irrespective of whether a section of the package or the complete package is instantiated in System Connectivity Manager, the generated Verilog netlist has information about all components pins.

Example of Asymmetrical Parts

Asymmetrical parts are also represented using split parts where each part represents a different logic. In case of asymmetrical parts, each of the split part can be simulated separately.

To simulate such parts, the `chips.prt` file is read for packaging information and the `map` file for pin-to-port mapping.

An example of an asymmetrical part is LS155. An excerpt of the `chips.prt` file for LS155 is listed below:

```
FILE_TYPE=LIBRARY_PARTS;
TIME=' COMPILE ON THU JAN 10 14:52:02 1991 ';
primitive '74LS155','74LS155_DIP';
pin
'-YB3':
  OUTPUT_LOAD='(8.0,-0.4)';
  PIN_NUMBER='(12,0)';
'-YB2':
  OUTPUT_LOAD='(8.0,-0.4)';
  PIN_NUMBER='(11,0)';
'-YB1':
  OUTPUT_LOAD='(8.0,-0.4)';
  PIN_NUMBER='(10,0)';
'-YB0':
  OUTPUT_LOAD='(8.0,-0.4)';
  PIN_NUMBER='(9,0)';
'-ENB2':
```

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Verilog Netlist for Parts

```
INPUT_LOAD='(-0.4,0.02)';
PIN_NUMBER='(14,0)';
'-ENB1':
INPUT_LOAD='(-0.4,0.02)';
PIN_NUMBER='(15,0)';
'S'<1>:
INPUT_LOAD='(-0.4,0.02)';
PIN_NUMBER='(3,3)';
'S'<0>:
INPUT_LOAD='(-0.4,0.02)';
PIN_NUMBER='(13,13)';
'ENA1':
INPUT_LOAD='(-0.4,0.02)';
PIN_NUMBER='(0,1)';
'-YA3':
OUTPUT_LOAD='(8.0,-0.4)';
PIN_NUMBER='(0,4)';
'-YA2':
OUTPUT_LOAD='(8.0,-0.4)';
PIN_NUMBER='(0,5)';
'-YA1':
OUTPUT_LOAD='(8.0,-0.4)';
PIN_NUMBER='(0,6)';
'-YA0':
OUTPUT_LOAD='(8.0,-0.4)';
PIN_NUMBER='(0,7)';
'-ENA2':
INPUT_LOAD='(-0.4,0.02)';
PIN_NUMBER='(0,2)';
end_pin;
body
POWER_PINS='(VCC:16;GND:8');
```

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Verilog Netlist for Parts

```
FAMILY='LSTTL';
PART_NAME='74LS155';
BODY_NAME='LS155';
DEFAULT_SIGNAL_MODEL='SN74LS155AN TI';
JEDEC_TYPE='DIP16_3';
CLASS='IC';
TECH='74LS';

end_body;
end_primitive;
...
...
END.
```

In the `chips.prt` file, you can observe that S1 and S0 are the only common pins. You can also observe that only symbols with mutually exclusive pins (besides common pins) can be merged together in the netlist.

The verilog netlist generated for the part is:

```
SN74LS155A i7 (.A(/* unconnected */),
    .B(/* unconnected */),
    ._1C(/* unconnected */),
    ._1G_/* unconnected */,
    ._1Y0/* unconnected */,
    ._1Y1/* unconnected */,
    ._1Y2/* unconnected */,
    ._1Y3/* unconnected */,
    ._2C_/* unconnected */,
    ._2G_/* unconnected */,
    ._2Y0/* unconnected */,
    ._2Y1/* unconnected */,
    ._2Y2/* unconnected */,
    ._2Y3/* unconnected */);
```

Asymmetrical parts may or may not have common pins. An example of asymmetrical part with no common pins between two versions is LS279 from the `lsttl` library.

Example of Multi-Section Parts

An example of an asymmetrical part with multiple sections is LS241. This is an asymmetrical part that has four versions (symbols), two vectored (sizeable) and two non-vectored (with the HAS_FIXED_SIZE property attached). Each of the nonvectored part represents a section of the complete part. Each section represents a Octal buffers/Line drivers with 3 state outputs. All the gates in a section have a common pin, OE0 and OE1 for section1 and section 2, respectively.

The chips.prt file for LS241 is listed below:

```
FILE_TYPE=LIBRARY_PARTS;
TIME=' COMPILATION ON THU JAN 10 14:52:02 1991  ';
primitive '74LS241','74LS241_DIP';
pin
'Y1'<0>:
  OUTPUT_LOAD='(24.0,-15.0)';
  INPUT_LOAD='(-0.02,0.02)';
  OUTPUT_TYPE='(TS,TS)';
  PIN_NUMBER='(12,14,16,18,0,0,0,0)';
'B'<0>:
  INPUT_LOAD='(-0.2,0.02)';
  PIN_NUMBER='(8,6,4,2,0,0,0,0)';
'-OE1':
  INPUT_LOAD='(-0.2,0.02)';
  PIN_NUMBER='(1,1,1,1,0,0,0,0)';
'Y0'<0>:
  OUTPUT_LOAD='(24.0,-15.0)';
  INPUT_LOAD='(-0.02,0.02)';
  OUTPUT_TYPE='(TS,TS)';
  PIN_NUMBER='(0,0,0,0,3,5,7,9)';
'OE0':
  INPUT_LOAD='(-0.2,0.02)';
  PIN_NUMBER='(0,0,0,0,19,19,19,19)';
'A'<0>:
  INPUT_LOAD='(-0.2,0.02)';
  PIN_NUMBER='(0,0,0,0,17,15,13,11)';
end_pin;
body
POWER_PINS='(VCC:20;GND:10);
```

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Verilog Netlist for Parts

```
FAMILY='LSTTL';
PART_NAME='74LS241';
BODY_NAME='LS241';
DEFAULT_SIGNAL_MODEL='SN74LS241N TI';
JEDEC_TYPE='DIP20_3';
CLASS='IC';
TECH='74LS';
end_body;
end_primitive;
...
...
```

If you instantiate this part in system Connectivity Manager, the logical verilog netlist generated is as shown below.

```
ls241 i3 (.a/* unconnected */,
            .oe0/* unconnected */,
            .y0/* unconnected */,
            .y1/* unconnected */,
            .b/* unconnected */,
            .\oe1* /* unconnected */);
```

Simulation Files

Some of the files that are created when you netlist the design are required for simulating the design. The files covered in this chapter are

■ Netlist Files

- <design_name>.v

When you run the netlister <design_name>.v file is created in the run directory that you specify for the simulation.

This is a single file Verilog netlist that is generated by concatenating the multiple netlist files for the hierarchical design. This netlist can be used to simulate your design using third-party Verilog simulators.

This file is created if you select the *Design Export* check box in the *Netlist* tab of the simulation interface setup dialog box.

■ Log Files

- netassembler.log

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Verilog Netlist for Parts

This file contains the debug messages that are logged when the design is netlisted.

- Map Files

- [Verilog Map File](#) on page 858
 - [Examples of Verilog Map Files](#) on page 864

Map Files

This section discusses the following:

- [Verilog Map File](#) on page 858
- [Examples of Verilog Map Files](#) on page 864

Verilog Map File

The Verilog map file (`verilog.map`) specifies pin-to-port mapping information and the parameters to be passed to the Verilog modules. Usually, this file is only necessary for externally defined libraries. This file can also be used for user-defined Verilog modules, but this is not usually necessary.

The Verilog map file must be located in the directory used to stop the expansion of the design (for example, `vlog_map`) and must be named `verilog.map`.

The following illustrates the format of a Verilog map file:

```
FILE_TYPE = VERILOG_MAP;
PRIMITIVE 'primitive_name' [ , 'primitive_name' ... ];
    DEFAULT_MODEL = "name";
    UPPER_CASE = 'TRUE';
    MODEL 'verilog_name' [ , 'verilog_name' ... ];
        PROPERTY
            PORT_ORDER = '(port1, port2, ... )';
            property_1 = value_1;
            ...
            property_n = value_n;
        END_PROPERTY;
        PIN_MAP
            body_pin_name_1 = verilog_port_name_1;
            ...
            body_pin_name_n = verilog_port_name_n;
        END_PIN;
    END_MODEL;
    MODEL 'verilog_name' [ , 'verilog_name' ... ];
    ...
END_PRIMITIVE;
PRIMITIVE 'primitive_name' [ , 'primitive_name' ... ];
...
END_PRIMITIVE;
END.
```

Note: If an entry is longer than one line, use a tilde (~) as a continuation character. The tilde can appear between any two characters in the entry but must be the last character in the line.

PRIMITIVE Section

The PRIMITIVE section describes all the information related to a specific primitive. The name used for the primitive is either the body name or the part name specified in the PART_NAME property. For example, in the *lstdt* library, LS00 has a PART_NAME = 74LS00 property and the primitive name 74LS00. You can modify this name by adding a PACK_TYPE property on a specific instance. For example, if an instance of LS00 has a PACK_TYPE = DIP property, the primitive name is 74LS00_DIP.

In the Verilog map file, you can describe several PRIMITIVE sections for different primitive names. For example, you can describe a primitive section for a 74LS00, another section for a 74LS00_DIP, and a third section for a 74LS00_SOIC. For an instance, entries are selected based on the primitive name for a specific instance.

For example, if there is no entry for a primitive called 74LS00_LCC, SCM looks for a 74LS00 entry. If it is not found, an error is generated. In most cases, this mechanism lets you specify only one primitive section as long as mapping information is independent of the PACK_TYPE.

You can specify two special properties in the PRIMITIVE section:

- The DEFAULT_MODEL property is used to specify the default name of the Verilog model.

This default name is used when no VERILOG_MODEL property has been used on an instance.

In case the DEFAULT_MODEL property is not used, first model in the last MODEL section is picked up.

For example, consider the part of the map file shown below.

```
PRIMITIVE '74HC125_SOIC';
  UPPER_CASE = TRUE;
  MODEL 'TTL125_SOIC','74HC125','CD74HC125';
    PROPERTY
      ...
    END_PROPERTY;
    PIN_MAP
      ...
    END_MODEL;
  MODEL 'TTL125','74HC125','CD74HC125';
    PROPERTY
      ...
    END_PROPERTY;
    PIN_MAP
```

```
    ...
    END_PIN;
    END_MODEL;
END_PRIMITIVE;
```

In the map file shown above, DEFAULT_MODEL is not defined. Therefore, TTL125 will be used as the default model. In cases where the DEFAULT_MODEL property is used but the model definition is not available, a warning message is generated and the first model in the last model definition is used.

- The UPPER_CASE property is used to specify that a Verilog module name needs to be made uppercase in the output netlist.

By default, all module names are in lowercase unless changed by an UPPER_CASE ='TRUE' property.

The following is an example of the PRIMITIVE section for an LS00:

```
FILE_TYPE = VERILOG_MAP;
PRIMITIVE '74LS00', '74LS00_DIP';
  DEFAULT_MODEL = 'SN74LS00';
  UPPER_CASE = 'TRUE';
  ...
END_PRIMITIVE;
END.
```

The output in the netlist is the following:

```
SN74LS00I1P(net1, net2, net3);
```

Note: The VERILOG_MODEL property value is case sensitive. If you do not take care of the casing while naming models, warnings may appear during netlist generation. For example, if you add the property, VERILOG_MODEL=vmodel, to a component instance, the corresponding verilog.map file must have a model defined as: MODEL 'vmodel'. An entry, such as MODEL 'VMODEL', will not work and warnings will be displayed during the generation of the simulation netlist.

MODEL Section

The MODEL section contains all information specific to one or several Verilog modules. You can specify several MODEL sections inside one PRIMITIVE section if you have several Verilog modules in a library that need different mapping information. At least one MODEL section must be described in the PRIMITIVE section.

The following is an example of the MODEL section for an LS00:

```
FILE_TYPE = VERILOG_MAP;
PRIMITIVE '74LS00';
  ...

```

```
MODEL 'SN74LS00', 'SIG74LS00' ;
...
END_MODEL
END_PRIMITIVE;
...
END.
```

PROPERTY Section

The PROPERTY section inside the MODEL section specifies local properties that apply to only one specific Verilog module. The PROPERTY section is optional.

You can add as many properties as you want. For example, if a COMPONENT property is defined in the property section, and if this property is added to any component instance, the this property as added as a parameter for the module using defparam in the Verilog netlist.

Two important properties are usually defined in this section:

- The VERILOG_NAME property specifies the actual name of the Verilog model.
 - Internally, all names for models are in lowercase.
 - If the name of the model you are using is either uppercase or contains a mixture of lowercase and uppercase characters, use the VERILOG_NAME property to specify how the model name will be written in the netlist.
- The PORT_ORDER property specifies the order of the Verilog model ports.

The following is an example of the PROPERTY section for an LS00:

```
FILE_TYPE = VERILOG_MAP;
PRIMITIVE '74LS00';
...
DEFAULT_MODEL = 'TTL00';
PROPERTY
    PORT_ORDER = '(1A, 1B, 1Y)';
    VERILOG_NAME = 'TTL00';
    COMPONENT = 'SN74LS00';
END_PROPERTY;
END_MODEL ;
...
END_PRIMITIVE;
...
END.
```

The output in the netlist is the following:

```
TTL00I4P(NET1, NET2, NET3);
defparamI4P.COMPONENT = "SN74LS00";
```

PIN MAP Section

The PIN MAP section allows mapping between pin names and Verilog port names and describes the Verilog port names used for each section of a multisection part.

The basic form for a pin map entry is

```
pin_name = ( port_name );
```

where *pin_name* is the name of the component pin. The syntax of the pin name is the same as that defined in the `chips.prt` file. If the pin represents a vector (multiple bits) rather than a scalar (single bit), the *pin_name* of the pin is specified as usual ($A<3..0>$). The *pin_name* uses the base name of the Compiler. For example, if a pin is specified as $A<SIZE-1..0>^*$, the pin name to use is $-A<0>$ to represent the low assertion character replaced by a minus sign (-), with the value 1 substituted for SIZE.

where *port_name* is the name of the Verilog port. If the port represents a vector (multiple bits) rather than a scalar (single bit), the *port_name* of the port is specified as follows:

```
pin_name = ( <port_name, port_name, port_name>, ... );
```

The enclosing angle brackets $<>$ indicate that the port represents multiple bits. The port names in the list are separated by commas.

For example, a 4-bit pin is specified as

```
'A'<3..0> = '( <A[0], A[1], A[2], A[3]> )';
```

Note: The LSB on the left maps to the first *port_name* on the right and the MSB on the LHS maps to the last *port_name* on the RHS. In this case, the $A<0>$ body pin maps to $A[0]$ and the $A<3>$ body pin maps to $A[3]$.

If the part has multiple sections, the *pin_map* must specify the *port_map* for each section. The form of the pin map for specifying sections is

```
pin_name = ( port_name, port_name, ... )
```

where *port_name* specifies the port name for the same pin but for a different section. For example, the output pin of a 74LS00 (a quad NAND gate) is specified as

```
'Y'<0> = '(_4Y, _3Y, _2Y, _1Y)';
```

You must specify four port names, because the part has four sections.

If a pin is common to each of the four sections, it must be given four port names; the port names are all identical. For example, the clock pin of a 74LS273 (an octal register) is specified as follows:

```
'CLOCK' = '(CLK, CLK, CLK, CLK, CLK, CLK, CLK, CLK)';
```

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Verilog Netlist for Parts

You must ensure that the port names are consistent for all ports of each section. Each name in the port name list specifies a different section.

If a sectioned part has vectored pins, its port names are specified in a similar manner. For example, a 3-bit pin in a part with two sections might be specified as

```
'A'<2..0> = '(<1A2, 1A1, 1A0>, <2A2, 2A1, 2A0>)';
```

Asymmetrical parts have multiple sections that are functionally different, such as the 74LS241, which has four buffers with active-high enables and four buffers with active-low enables. A different version of the body is defined for each section in the part. The pins in the different versions all have different pin names, so that a pin of a given name is present in only one section. The port map values for the pin specify all the sections of the part. Any port that is not present in a given section is specified with a port name of 0.

For example, the pin map section for an 74LS241 is the following:

```
PIN_MAP;
  'Y1'<0> = '(_1Y4, _1Y3, _1Y2, _1Y1, 0, 0, 0, 0 )';
  'B'<0> = '(_1A4, _1A3, _1A2, _1A1, 0, 0, 0, 0)';
  '-OE1' = '(_1G_, _1G_, _1G_, _1G_, 0, 0, 0, 0)';
  'Y0'<0> = '(0, 0, 0, 0, _2Y4, _2Y3, _2Y2, _2Y1)';
  'A'<0> = '(0, 0, 0, 0, _2A4, _2A3, _2A2, _2A1)';
  'OE0' = '(0, 0, 0, 0, _2G, _2G, _2G, _2G)';
END_PIN;
```

The syntax for port mapping also allows for a more compact syntax. In addition to the previous notation, the following features are also supported:

- Subranges

The port map (*Y4*, *Y3*, *Y2*, *Y1*) is equivalent to (*Y4..Y1*).

- Repeat sections

The port map (*OE*, *OE*, *OE*, *OE*) is equivalent to (*OE * 4*).

- Vectored pins

The port map (<*Y2..Y0*> * 2) is equivalent to (<*Y2*, *Y1*, *Y0*>, <*Y2*, *Y1*, *Y0*>).

For example, the previously described 74LS241 can be described using the following compact syntax:

```
PIN_MAP;
  'Y1'<0> = '(_1Y4 .. _1Y1, 0 * 4)';
  'B'<0> = '(_1A4, .. _1A1, 0 * 4)';
  '-OE1' = '(_1G * 4, _0 * 4)';
  'Y0'<0> = '(0 * 4, _2Y4 .. _2Y1)';
  'A'<0> = '(0 * 4, _2A4 .. _2A1)';
  'OE0' = '(0 * 4, _2G * 4)';
END_PIN;
```

In a Verilog map file, pin names that have 0 (zero) assigned to them, do not appear in the Verilog netlist.

For example, consider the following statements in the pin map section of a Verilog map file.

```
'X' = '(0);
```

This implies that the signal connected to the pin X will not be written in the Verilog netlist.

Examples of Verilog Map Files

This section contains examples of the following map files:

- [Verilog Model without Sections \(LS145\)](#)
- [Verilog Model with Sections \(LS153\)](#)
- [Verilog model for an Asymmetrical Part \(LS241\)](#)

Verilog Model without Sections

The following example is of a Verilog model without sections (LS145):

```
FILE_TYPE = VERILOG_MAP;
PRIMITIVE '74LS145';
  DEFAULT_MODEL = 'SN74LS145';
  UPPER_CASE = 'TRUE';
  MODEL 'SN74LS145';
    PIN_MAP
      'I'<3> = '(D)';
      'I'<2> = '(C)';
      'I'<1> = '(B)';
      'I'<0> = '(A)';
      '-Y9' = '(_9)';
      '-Y8' = '(_8)';
      '-Y7' = '(_7)';
      '-Y6' = '(_6)';
      '-Y5' = '(_5)';
      '-Y4' = '(_4)';
      '-Y3' = '(_3)';
      '-Y2' = '(_2)';
      '-Y1' = '(_1)';
      '-Y0' = '(_0)';
    END PIN;
  END_MODEL;
END_PRIMITIVE;
END.
```

The output in the netlist is the following:

```
SN74LS145 PAGE1_5P (.D(LS145_I[3]),
.C(LS145_I[2]),
```

```
.B(LS145_I[1]),  
.A(LS145_I[0]),  
.9(LS145_Y9),  
.8(LS145_Y8),  
....  
.0(LS145_Y0));
```

Verilog Model with Sections

The following example is a map file for a Verilog model for a part with sections (LS153):

```
FILE_TYPE = VERILOG_MAP;  
PRIMITIVE '74LS153';  
    DEFAULT_MODEL = 'SN74LS153';  
    UPPER_CASE = 'TRUE';  
    MODEL 'SN74LS153';  
        PIN_MAP  
            'Y'<0> = '(_2Y, _1Y)';  
            'S'<1> = '(_B, B)';  
            'S'<0> = '(A, A)';  
            'I3'<0> = '(_2C3, _1C3)';  
            'I2'<0> = '(_2C2, _1C2)';  
            'I1'<0> = '(_2C1, _1C1)';  
            'I0'<0> = '(_2C0, _1C0)';  
            '-E' = '(_2G_, _1G_);  
        END_PIN;  
    END_MODEL;  
END_PRIMITIVE;  
END.
```

Note: To operate on a part that contains sections, a `chips.prt` file must also be available. The Cadence standard parts library comes with a `chips.prt` file. So do not modify it.

Verilog model for an Asymmetrical Part

The following example is a map file for a Verilog model for the LS241 asymmetrical part.

```
FILE_TYPE=VERILOG_MAP;  
PRIMITIVE '74LS241';  
    DEFAULT_MODEL=SN74LS241;  
    UPPER_CASE=TRUE;  
    MODEL 'SN74LS241';  
        PIN_MAP  
            'Y1'<0>='(_1Y4,_1Y3,_1Y2,_1Y1,0,0,0,0)';  
            'B'<0>='(_1A4,_1A3,_1A2,_1A1,0,0,0,0)';  
            '-OE1'='(_1G_,_1G_,_1G_,_1G_,0,0,0,0)';  
            'Y0'<0>='(0,0,0,0,_2Y4,_2Y3,_2Y2,_2Y1)';  
            'OE0'='(0,0,0,0,_2G,_2G,_2G,_2G)';
```

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```
'A'<0>='(0,0,0,0,_2A4,_2A3,_2A2,_2A1)';
END_PIN;
END_MODEL;
END_PRIMITIVE;
END.
```

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