

AWR® Microwave Office®-Allegro® RF Design User Guide

Product Version 23.1

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AWR Microwave Office-Allegro RF Design User Guide

Creating RF Design Using AWR Microwave Office and Allegro PCB Design Applications

RF circuits are designed independent of the PCB designs in which they are used and follow additional guidelines to ensure good signal integrity performance of the PCB. The integration of Cadence® AWR® Microwave Office® software and Allegro® PCB Design applications provides a way to create complex PCBs with RF design.

Microwave Office is a circuit design application used for capturing RF design, circuit/system/EM analysis, and optimization. An electrical design created in Microwave Office contains layout and PCB stackup information along with physical design constraints. This RF design, when transferred to an Allegro PCB design application, can be used as part of a larger PCB. Microwave Office to Allegro RF Design flow helps you integrate an RF design with mixed-signal PCB designs with more accuracy and in lesser time than the traditional flow.

Advantages of Microwave Office-Allegro RF Design Flow

The Microwave Office-Allegro RF Design flow supports seamless data exchange between a PCB layout and RF circuit design and offers the following benefits over traditional RF PCB design flows:

- Creates RF design using Allegro libraries and technologies in Microwave Office.
- Uses the same libraries as Allegro PCB design for creating RF design in Microwave Office. The design components have identical symbols, footprints, and properties in Microwave Office and need not to be replaced when transferred to Allegro PCB Design applications for manufacturing.
- Ensures that the technology information is identical to the manufacturing technology and the same stackup information is provided for EM simulations.
- Provides manufacturable vias for placement and simulation. These vias can be transferred as it is with the RF design.

- Provides physical design constraints within Microwave Office for dynamic voiding of ground/power planes.
- Supports data transfer from Microwave Office to Allegro PCB Design applications of all library parts, RF metal, and vias, eliminating the need for time consuming and error prone manual re-entry or replacement of parts and vias.

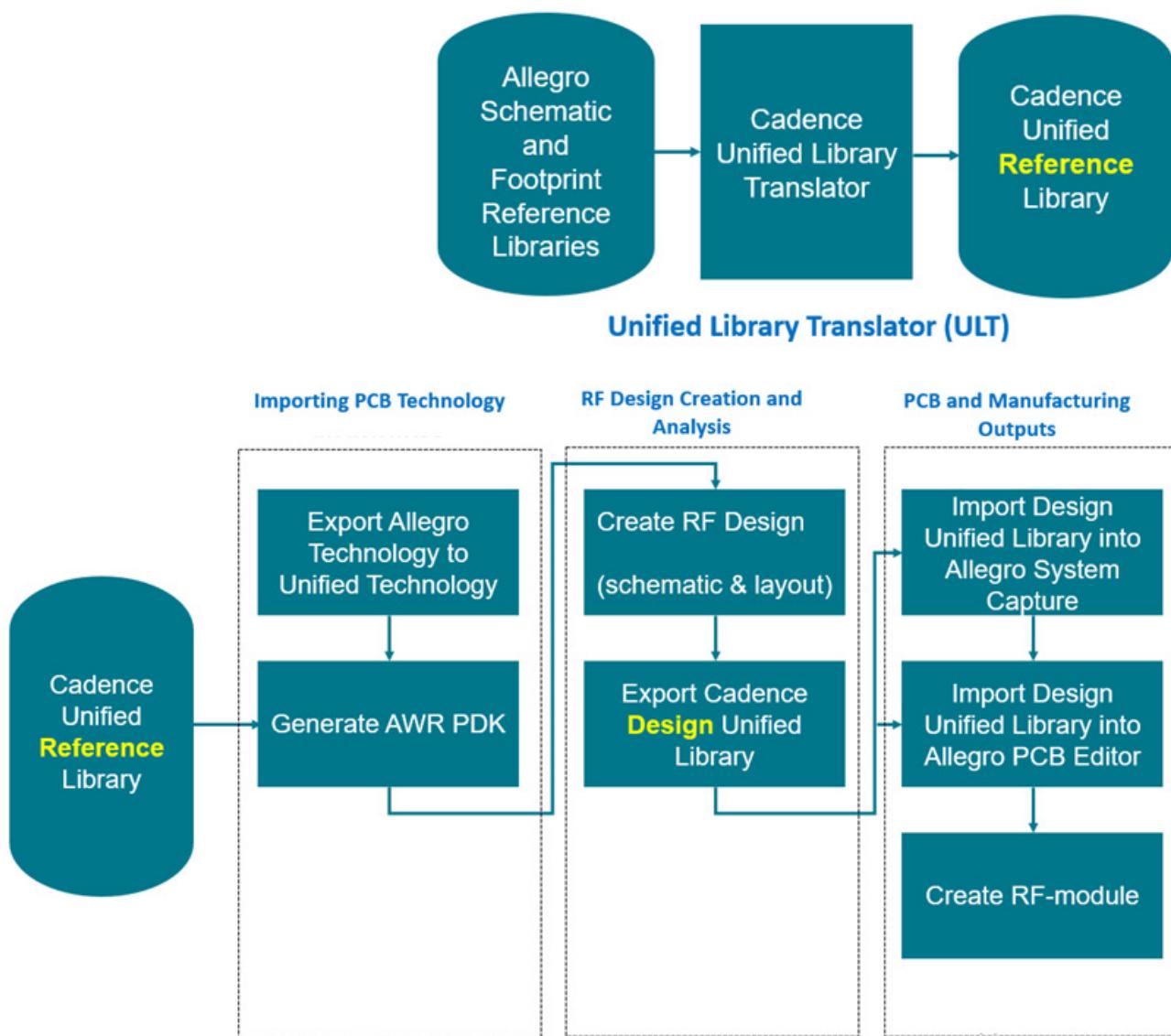
Design Flow

Microwave Office-Allegro RF Design flow uses the Cadence Unified Library solution. Unified libraries are common databases containing technology, components, and design information required to create and verify an RF design readable by both the applications.

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Creating RF Design Using AWR Microwave Office and Allegro PCB Design Applications

The following flow chart represents the design flow for an RF PCB design created in Microwave Office and Allegro PCB Design applications:



Cadence Unified Reference Library Creation

Cadence unified library is the foundation of the design flow. It is used to exchange data between Microwave Office and Allegro PCB Design applications. A unified reference library contains all the necessary information to design an RF schematic and a layout in Microwave Office, including PCB technology, manufacturable components, and vias. A unified reference library is generated by translating the Allegro schematic and footprint reference library of discrete components to the Cadence unified library format.

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Creating RF Design Using AWR Microwave Office and Allegro PCB Design Applications

PCB Technology Import

You import PCB technology to unified technology and generate Process Design Kit (PDK) for Microwave Office.

RF Design Creation and Analysis

Microwave Office PDK is used by Microwave Office to capture the RF schematic and to generate the layout using components and technology from Cadence unified library. The RF design is simulated for functional performance and exported in the unified library format in Allegro PCB Design applications.

PCB Creation and Generating Manufacturing Outputs

The unified library imported to Allegro System Capture and Allegro PCB Editor, creates schematic and layout, respectively. The RF design is saved as a PCB module to be used in larger PCB designs.

Software and System Requirements

The Microwave Office-Allegro RF Design flow requires following software and system variable settings:

Software Release Compatibility

To work with the Microwave Office-Allegro RF Design flow, ensure that the following released versions of the applications are installed on your system:

- AWR Microwave Office17 (17.03)
- OrCAD X/Allegro 23.1

Note: AWR Microwave Office is a Windows-based application.

Additional System Requirements

The Microwave Office-Allegro RF Design flow is a limited-release functionality. To enable the Microwave Office-Allegro RF Design flow, ensure that the following system environment variables are set on the system:

- MWO_ALLEGRO = 1

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In addition to the system variables, you need to set the following application variable under the [general] section in the user.ini file of Microwave Office:

```
CDSInterop=1
```

The user.ini file of Microwave Office can be accessed from *Help – Show Files/ Directories*.

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Creating RF Design Using AWR Microwave Office and Allegro PCB Design Applications

Generating Cadence Unified Libraries

The foundation of the Microwave Office-Allegro RF design flow is Cadence unified library that contains technology (stackup, constraints, and via) and component information required to design, simulate, and fabricate an RF PCB design. Cadence unified library is used for transferring design and technology between Microwave Office and Allegro PCB Design applications.

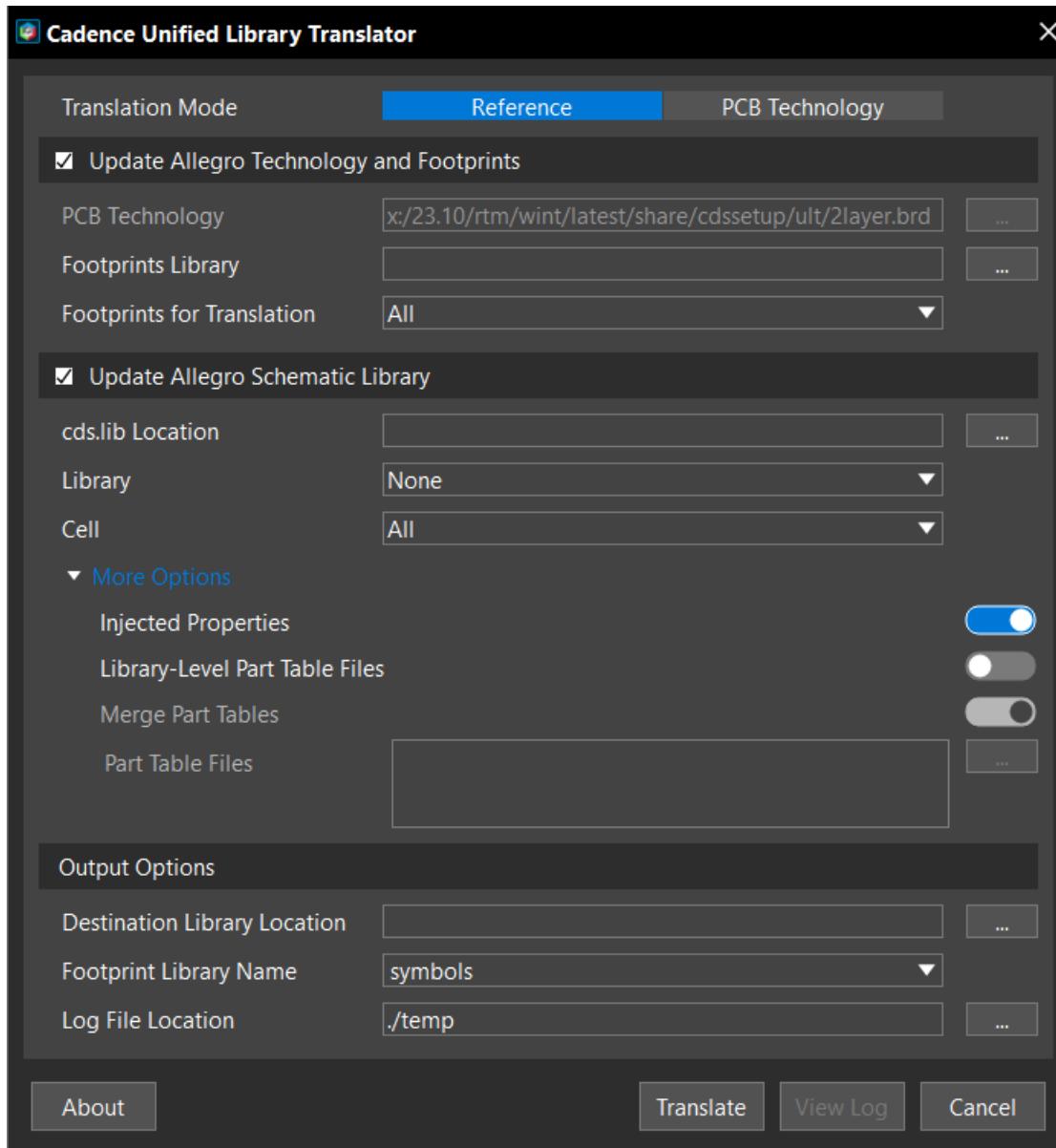
The process of creating Cadence unified library involves the following steps:

- Extracting layer definition by exporting a technology file from a PCB design (`.brd` or `.tcf`, or `.tcfx`).
- Converting the Allegro footprint library to the Cadence unified library format.
- Converting Allegro library of discrete components to the Cadence unified library format.

The library translation process creates additional views in the Allegro library of discrete components. These views are read by Microwave Office for creating an RF schematic and layout.

Unified Library Translator

The *Cadence Unified Library Translator* interface is used to selectively translate Allegro technology file, footprints libraries, and schematic libraries.



Library Translation Modes

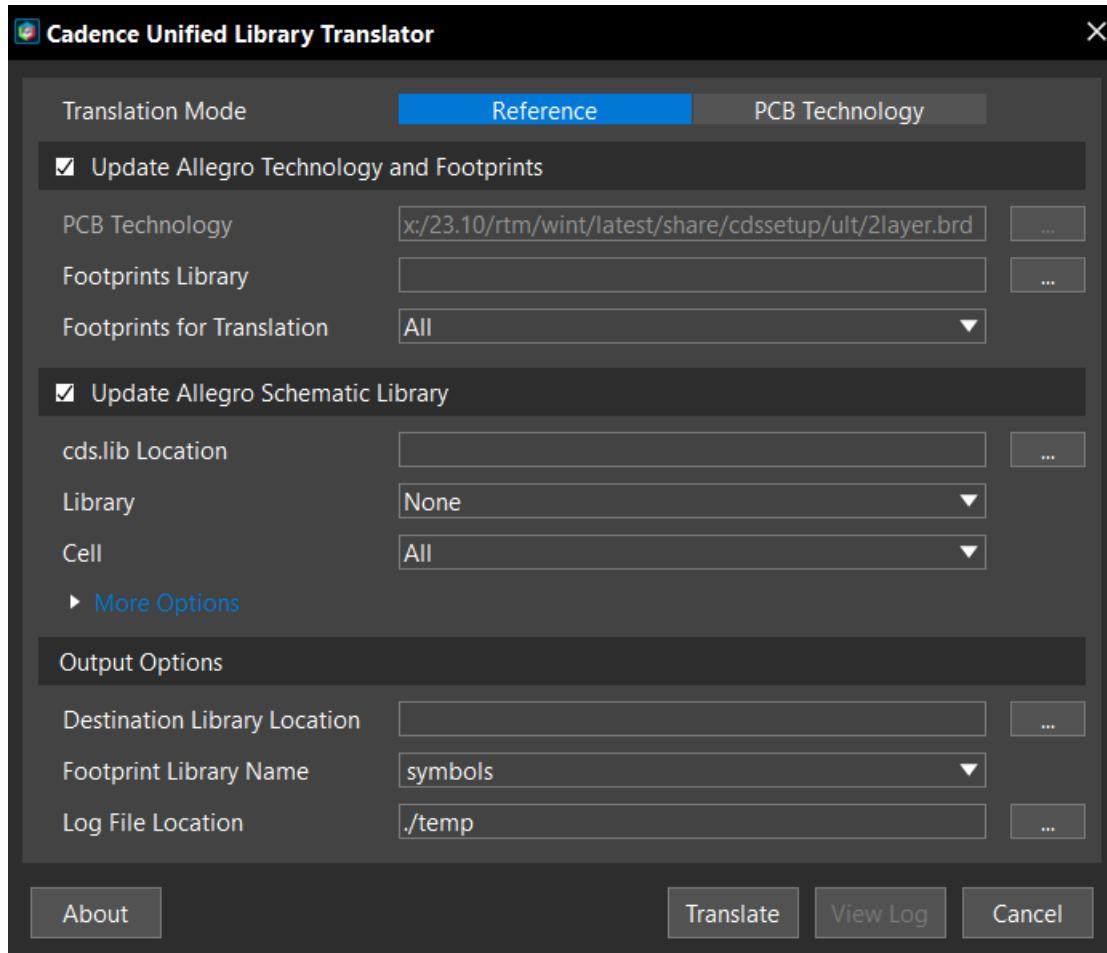
There are two modes to translate Allegro symbol libraries, the *Reference* and *PCB Technology*.

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Generating Cadence Unified Libraries

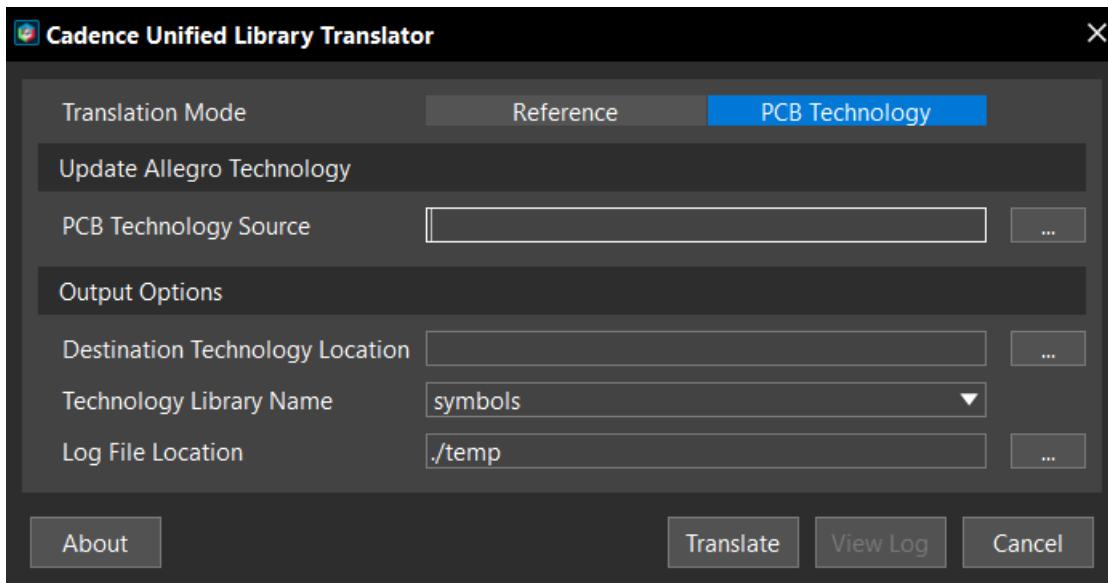
- **Reference Mode:** In this mode, the logic and footprint symbol libraries are translated. The translator uses a default two-layer board design file shipped with the installation located at: <insat11_directory>\share\cdssetup\ult.

This mode helps librarians translate entire schematic components and footprint symbols libraries independent of PCB technology. This is a one-time process.



- **PCB Technology Mode:** In this mode, the design-specific technology file is translated along with the logic and footprint symbol libraries. The translator uses a design technology specified in the *PCB Technology Source* field.

This mode helps designers extract technology file and vias from a multi-layer board. You can provide a board file (.brd) or a technology file (.tcfx or .tcf) as an input to Cadence Unified Library Translator.



Translating Allegro Libraries

Library translation can be done separately for schematic and footprint symbols by selecting either the *Reference* or *PCB Technology* library translation modes. This helps librarians to translate the complete schematic library, which is always available to designers for use. Designers, on the other hand, can select the *PCB Technology* mode to translate specific board design to transfer the PCB design requirements in Microwave Office to create RF design.

Prerequisites

Before translating Allegro reference libraries, manually complete the following two tasks critical to the Microwave Office-Allegro RF Design flow.

- Create the `cds.lib` file: The translation of Allegro libraries can be done by librarians and is a one-time task. The name and path of libraries that are to be translated should be defined in the `cds.lib` file. *Cadence Unified Library Translator* takes this file as an input and translates only those libraries that are specified in this file.
- Modify part table files: The Allegro component libraries contain packaging properties of a component, such as package types, manufacturers, part numbers, and any custom properties in the properties file (parts table file) of components. The physical parts table

(.ptf), by default, does not contain model information. Before running the translator, you need to modify the part table files to include the model information. This step is required to include simulation models for Allegro symbol footprints that are used in Microwave Office for analyzing the design. Files containing model information are required to update the PTF files. These files are available with Microwave Office.

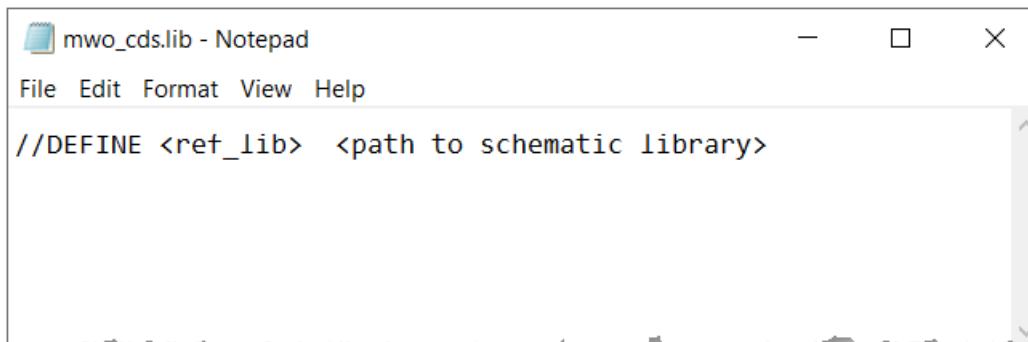
The part table files are stored either in a single directory or inside each component cell in a library. You can add model information in both library-level PTF and component-level PTF.

Creating cds.lib File for Translator

Cadence Unified Library Translator reads the `cds.lib` file to select schematic and footprint libraries for translation. You can create this `cds.lib` file using the sample file (`mwo_cds.lib`) that is shipped as part of the OrCAD X/Allegro 23.1 installation.

1. Navigate to the location of sample `mwo_cds.lib` file at
`<install_directory>\share\library`

The following image illustrates the content of the sample file.



A screenshot of a Windows Notepad window titled "mwo_cds.lib - Notepad". The window shows a single line of code: `//DEFINE <ref_lib> <path to schematic library>`. The Notepad interface includes a menu bar with File, Edit, Format, View, and Help, and standard window controls (minimize, maximize, close) at the top.

2. Copy the `mwo_cds.lib` in your working directory.
3. Rename the file as `cds.lib`.

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Generating Cadence Unified Libraries

4. Open the `cds.lib` file in a text editor and modify the name and path of the reference libraries. An example of `cds.lib` file is illustrated here:



```
cds.lib - Notepad
File Edit Format View Help
DEFINE 5g_library .\5g_library
```

5. Add name and the complete path of all the libraries. ‘

6. Save and close the `cds.lib` file.

Adding AWR Model Information to Allegro Part Table Files

PTFs are located in the part table directory of a part in a library. To add the model information in a PTF, do the following:

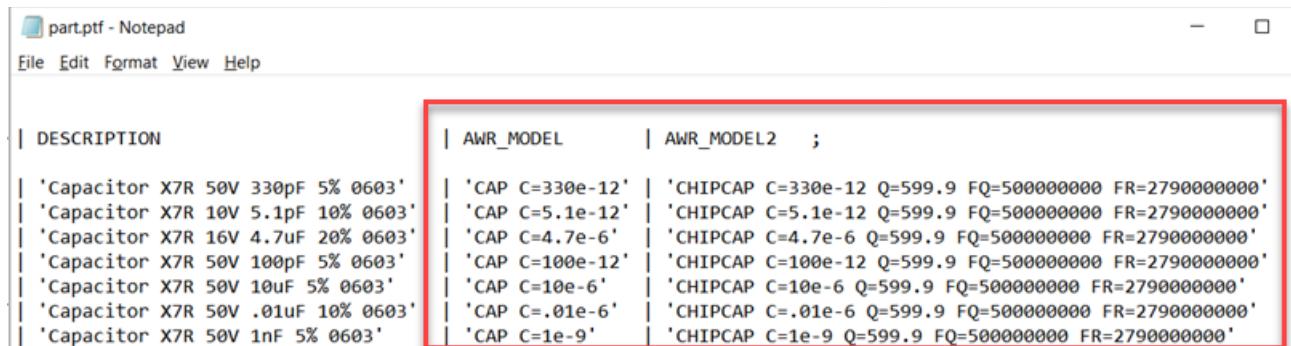
1. Open the built-in Allegro library of discrete components in Windows file explorer and select a part name.

The part library contains three folders: `chips`, `sym_1`, and `part_table`.

2. Open the `part_table` folder and open the `part.ptf` file in a text editor.

PTF is a text file that includes component attributes in a tabular format.

3. Add a new column at the end of the table specifying *AWR_MODEL* for including simulation views to Allegro library components, as illustrated in the following image:



DESCRIPTION	AWR_MODEL	AWR_MODEL2 ;
'Capacitor X7R 50V 330pF 5% 0603'	'CAP C=330e-12'	'CHIPCAP C=330e-12 Q=599.9 FQ=5000000000 FR=2790000000'
'Capacitor X7R 10V 5.1pF 10% 0603'	'CAP C=5.1e-12'	'CHIPCAP C=5.1e-12 Q=599.9 FQ=5000000000 FR=2790000000'
'Capacitor X7R 16V 4.7uF 20% 0603'	'CAP C=4.7e-6'	'CHIPCAP C=4.7e-6 Q=599.9 FQ=5000000000 FR=2790000000'
'Capacitor X7R 50V 100pF 5% 0603'	'CAP C=100e-12'	'CHIPCAP C=100e-12 Q=599.9 FQ=5000000000 FR=2790000000'
'Capacitor X7R 50V 10uF 5% 0603'	'CAP C=10e-6'	'CHIPCAP C=10e-6 Q=599.9 FQ=5000000000 FR=2790000000'
'Capacitor X7R 50V .01uF 10% 0603'	'CAP C=.01e-6'	'CHIPCAP C=.01e-6 Q=599.9 FQ=5000000000 FR=2790000000'
'Capacitor X7R 50V 1nF 5% 0603'	'CAP C=1e-9'	'CHIPCAP C=1e-9 Q=599.9 FQ=5000000000 FR=2790000000'

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Generating Cadence Unified Libraries

4. Model definition for each AWR_MODEL (AWR_MODEL, AWR_MODEL2) can be specified in one of the following ways:
- ❑ Specify the model definition that includes the name of a model and its parameters values.
 - ❑ Refer a model that includes the name of a model, pin configuration, and the variant name.

```
FILE_TYPE = MULTI_PHYS_TABLE;

PART 'POWER_NMOS'

{=====
:PART_NUMBER      = JEDEC_TYPE | ALT_SYMBOLS      | DESCRIPTION           | AWR_MODEL          ;
{=====
'NMOS65W'(!)    = 'SOT'        | '(SOT_1)'        | 'POWER LDMOS 65W'   | '(1 3 2 4) GENERIC_LDMOS' : WATTAGE = '65W'
'NMOS100W'(!)   = 'SOT_100W'  | '(SOT_100W_1)'  | 'POWER LDMOS 100W' | '(1 3 2 4) GENERIC_LDMOS' : WATTAGE = '100W'

END_PART

END.
```

5. Save the files.

For more information on model association, refer to [AWR Design Environment User Guide for version AWR 16](#) from the [Cadence Online Support](#) site.

Translating Allegro Libraries

To translate Allegro libraries to the Cadence unified library format you need to do the following:

1. Navigate to the following path of your installation directory:

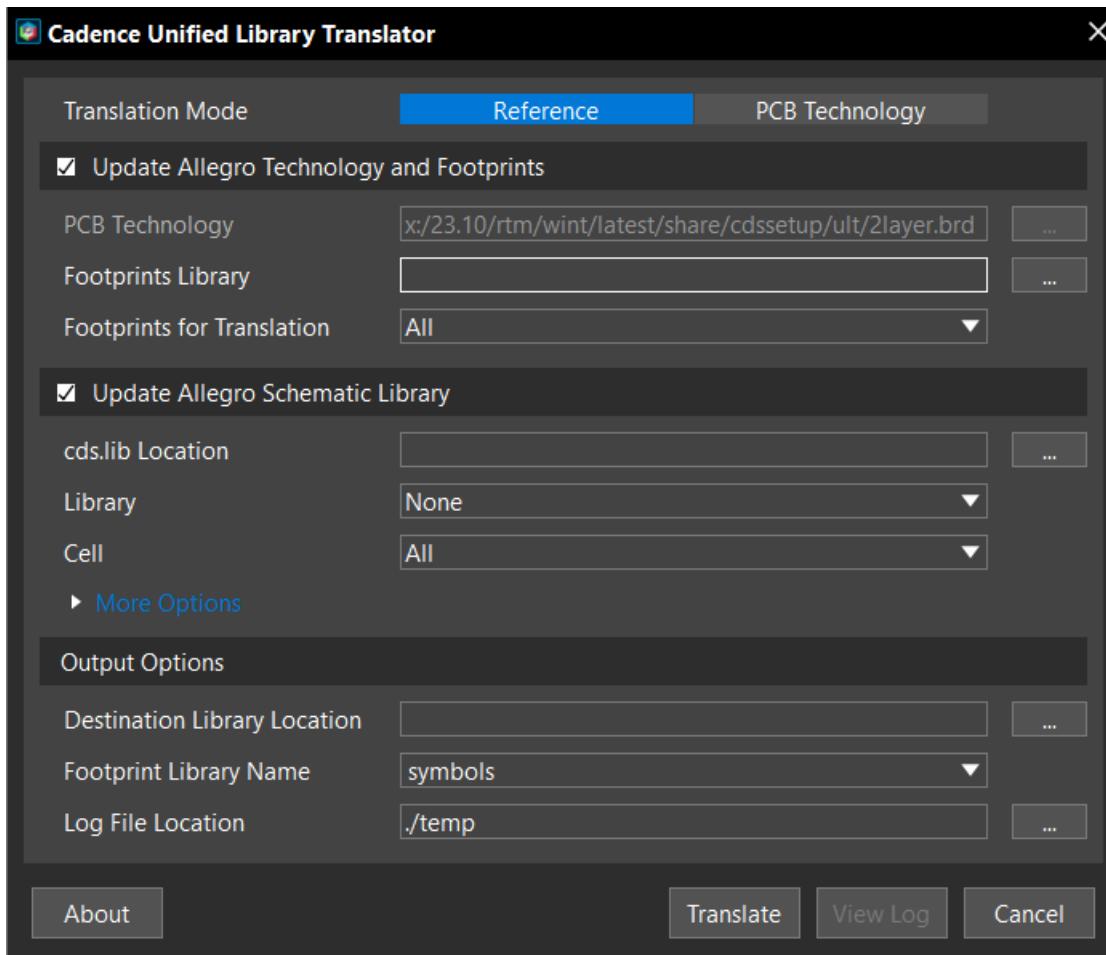
<install_directory>\tools\bin

2. Double-click ult.exe to open *Cadence Unified Library Translator*.

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Generating Cadence Unified Libraries

The *Cadence Unified Library Translator* dialog box opens with default settings.



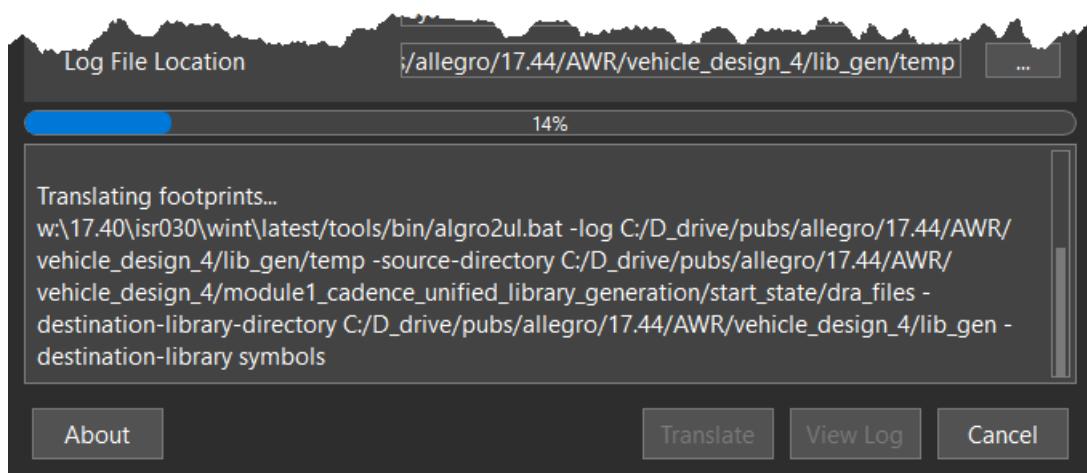
3. Select the *Translation Mode* as *Reference*.
4. Specify the location of the footprint symbols files (.dra, .pad, .fsm, .psm) in the *Footprint Library* field.
The *Footprints for Translation* field populates with a list of footprint names from the footprint library.
5. Choose a .dra file from the *Footprints for Translation* list. By default, *All* is selected.
6. Specify the path of the cds.lib file that contains name and path of reference library or libraries.
7. Choose a specific schematic library name or select *All* from the *Library* from the list.
The *Cell* field populates with symbol names from the selected schematic library.
8. Choose the schematic symbol name from the *Cell* list. By default, *All* is selected.

Note: Split symbols, sizeable parts, and asymmetric parts are not supported. These symbols cannot be translated into the Cadence unified library format.

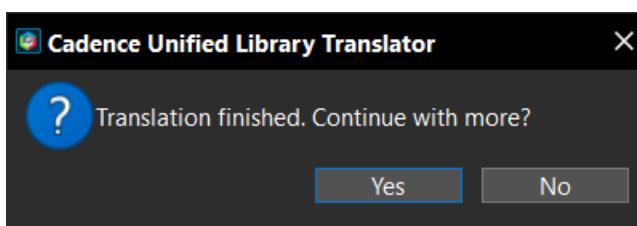
9. To define the *Output Options*, do the following:
 - a. Specify a path for the output directory in the *Destination Library Location*.
 - b. Specify a name for footprint library. A library with this name is created in the destination directory. The default name is *symbols*.
 - c. Create a directory with name `temp` in the destination directory and specify its path in the *Log File Location* field.

10. Click *Translate* to start the process.

A progress bar is displayed along with translation output in the extended dialog box.



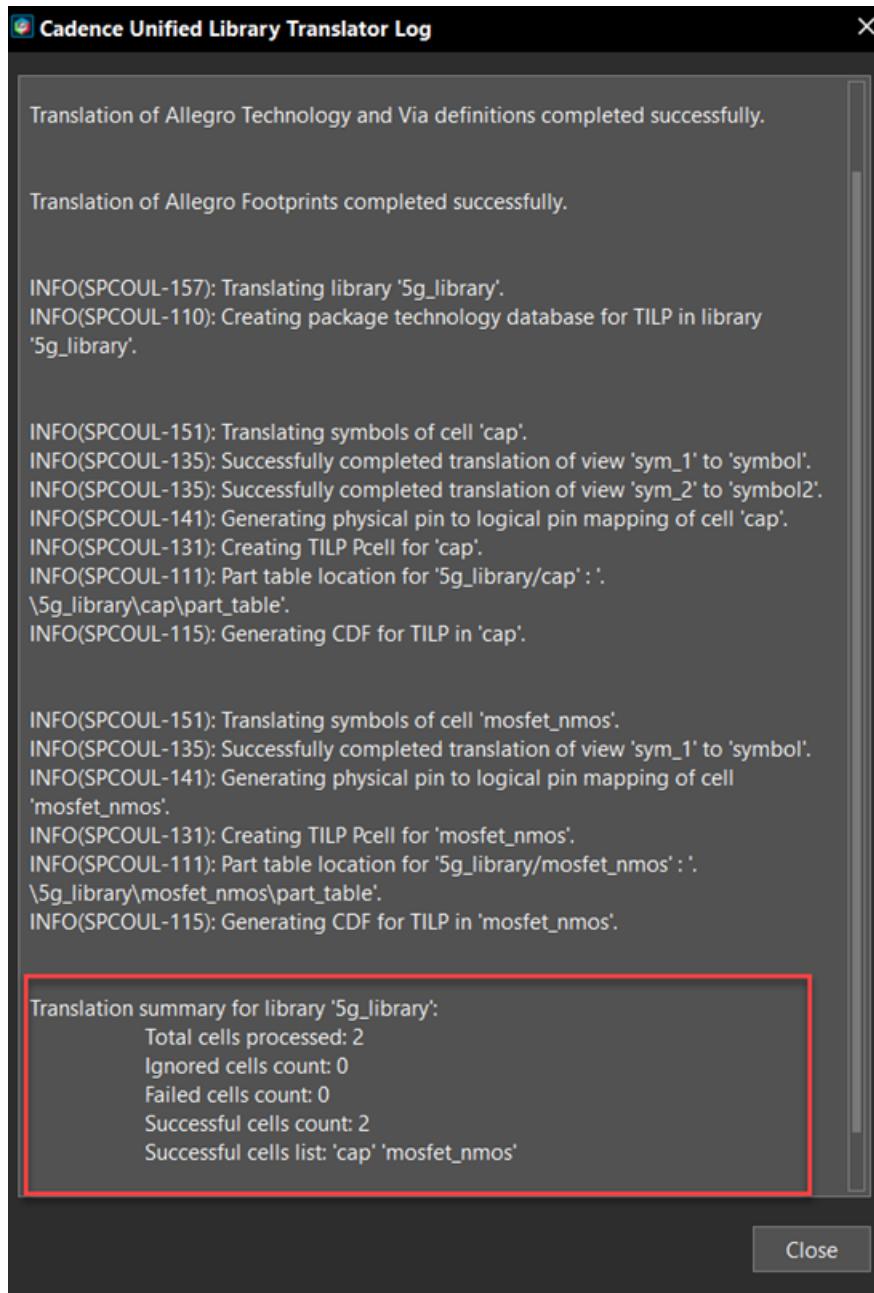
11. Click *No* in the message prompt that is displayed after the translation is completed.



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Generating Cadence Unified Libraries

12. To review the translator summary, click *View Log*.



13. After verifying the translation log, click *Close* in the *Cadence Unified Translator Log* dialog box.
14. Click *Close* in the *Cadence Unified Translator* dialog box.

Translating Allegro Technology File

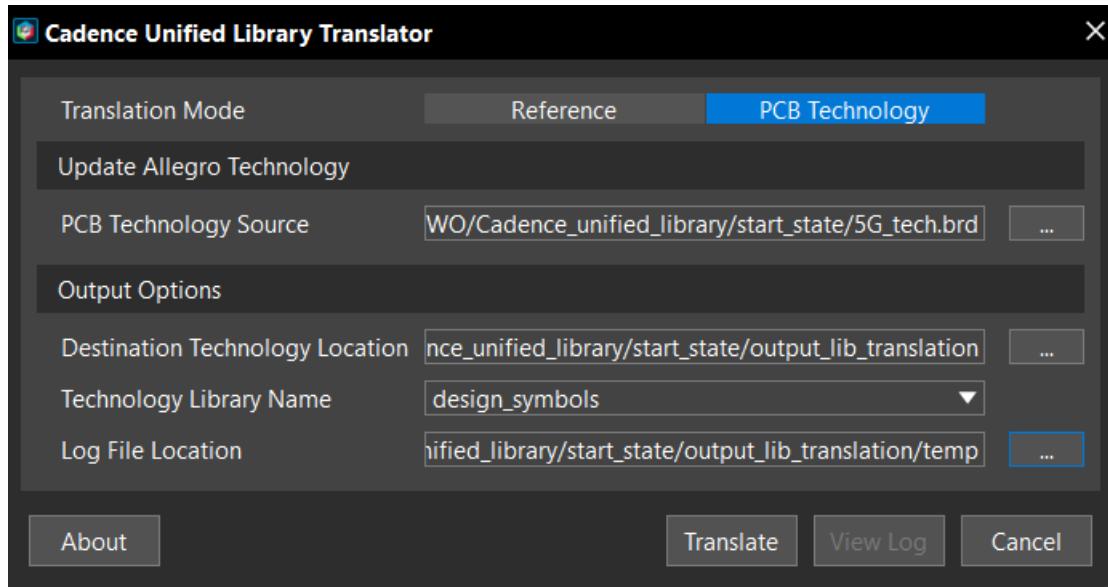
Design requirements, such as the number of layers along with via and constraint details can be exported to Microwave Office by translating the technology file to the Cadence unified library format.

The *PCB Technology* mode of *Cadence Unified Library Translator* is used to translate the technology information from a technology file using the following steps:

1. Navigate to the following path of your installation directory:

<installation_directory>/tools/bin

2. Double-click `ult.exe` to open *Cadence Unified Library Translator*.
3. Select the *Library Translation Mode* as *PCB Technology*.

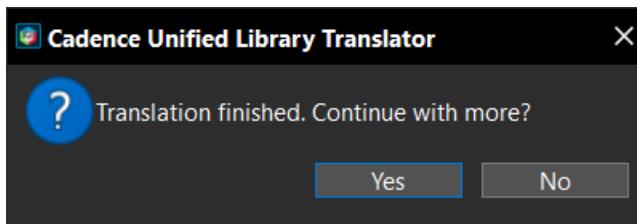


4. Specify the path of the `.brd` (or `.tcfx` or `.tcf`) file that has layer and via information.
5. To define the *Output Options*, do the following:

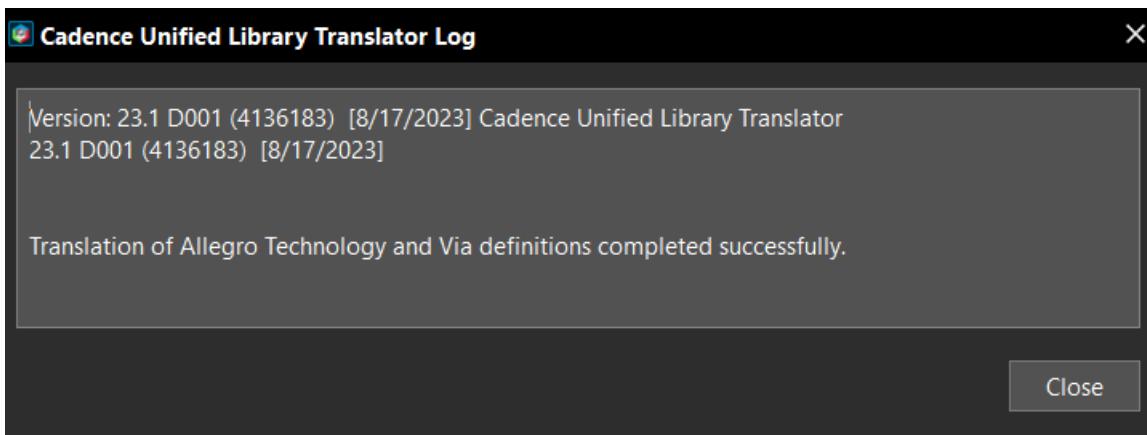
- a. Specify a path for the output directory in the *Destination Technology Location*. This can be the same directory as the one that stores the translated libraries.
- b. Specify *Technology Library Name*. A library with this name is created in the destination directory. The default name is *symbols*.

Note: The name and location of the technology library should be different from the one you specified when translating the Allegro library. Keeping Allegro and technology libraries at the different location helps you verify the translated output.

- c. Create a directory with name `temp` in the destination directory and specify its path in the *Log File Location* field.
6. Click *Translate* to start the process.
A progress bar is displayed along with translation output in the extended dialog box.
7. Click *No* in the message prompt that is displayed after the translation is completed.



8. To review the translator summary, click *View Log*.



9. After verifying the translation log, click *Close* in the *Cadence Unified Translator Log* dialog box.
10. Click *Close* in the *Cadence Unified Translator* dialog box.

Verifying Translated Libraries

The translation process creates a copy of the Allegro libraries in the destination directory and then uprevs the libraries. The following data is resulted as an output when you run *Cadence Unified Library Translator*:

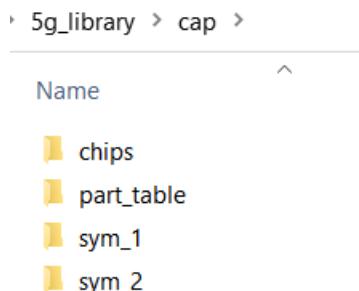
- Reference Mode
 - Reference schematic library/libraries

- Reference symbol library
- PCB Technology Mode
 - Design schematic library
 - Design symbol library
 - Design technology file and via information
 - Design symbols

To verify the translated output, open the Windows file browser and navigate to the destination directory to verify the translated output. Check for the following details:

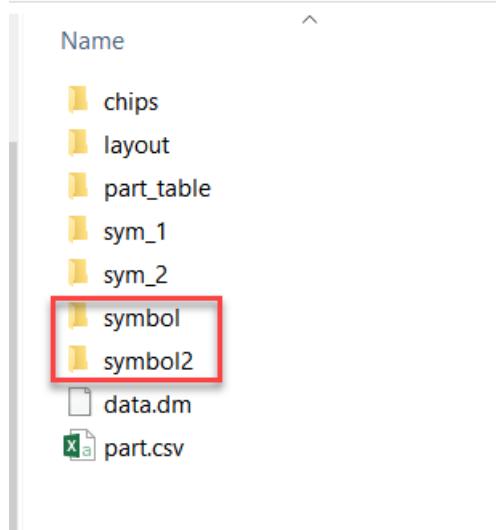
- The output `cds.lib` file contains reference to relevant library paths.
- Cadence unified library views are created in the cells selected for schematic library.

Input schematic library



Translated schematic library

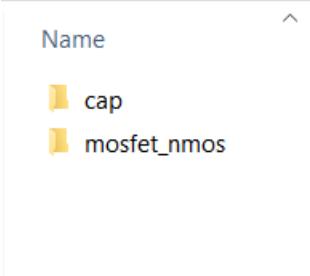
translated_libs > 5g_library > cap



- At the library-level, new views .oalib, data.dm, and tech.db are created in the destination directory. The data.dm file contains symbol pin mapping while .oalib contains data.settings for library management.

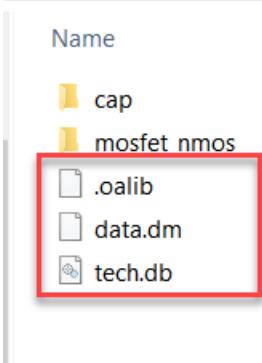
Input schematic library

> 5g_library



Translated schematic library

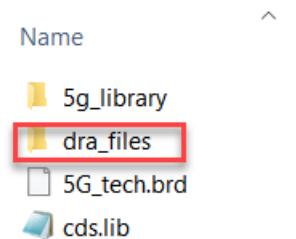
translated_libs > 5g_library >



- The symbols directory and lib.defs views are created for the footprint library.

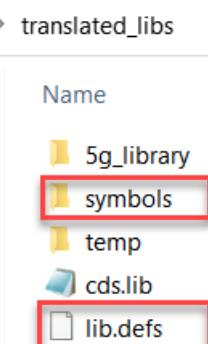
Input footprint library

start_state



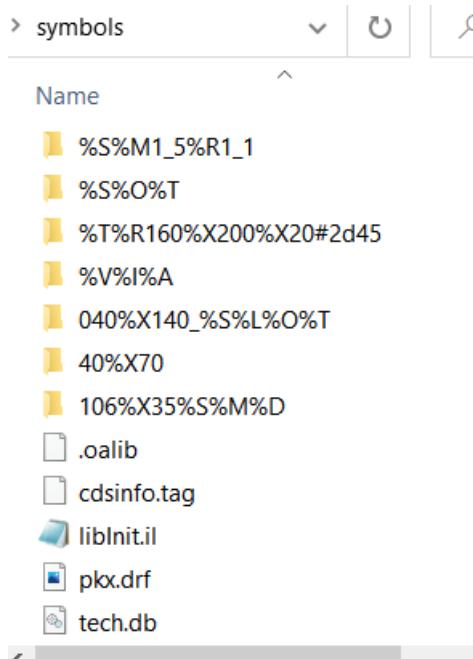
Translated footprint library

translated_libs



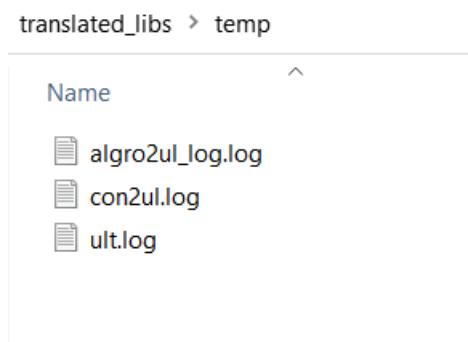
- The `symbols` directory contains layout view of all the footprint symbols and the `tech.db` file, which is extracted from the input board design file(`.brd`).

Translated footprint library containing layout view and `tech.db`



- The `temp` directory contains all the log files generated as a result of the translation process.

Translation logs



Translating Allegro Libraries in Batch Mode

Allegro libraries can be translated using batch commands. For more information, see [Command Line Reference](#).

AWR Microwave Office-Allegro RF Design User Guide
Generating Cadence Unified Libraries

Generating Microwave Office PDK

A Process Design Kit (PDK) contains component information to create schematic and layout in Microwave Office. It also includes associated schematic and layout views to simulate the design. PDKs are unique for a given technology. You need to generate different PDKs for different process technologies.

To create a new design with Allegro libraries in Microwave Office, you need to include the PDKs from Cadence unified library. A PDK is needed to use components, footprints, and models from Allegro libraries.

Associating PDK to create RF designs in Microwave Office involves two tasks:

- PDK generation from a Cadence unified library
- Associating PDK (.ini) to a new project

Prerequisite

Ensure that the `cds.lib` contains all the reference and design libraries that are translated by *Cadence Unified Library Translator*. You can also manually update the `cds.lib` file to include the required libraries.

Generating AWR PDKs from a Cadence Unified Library

To import a Cadence unified library and create AWR PDKs for design and technology libraries, do the following:

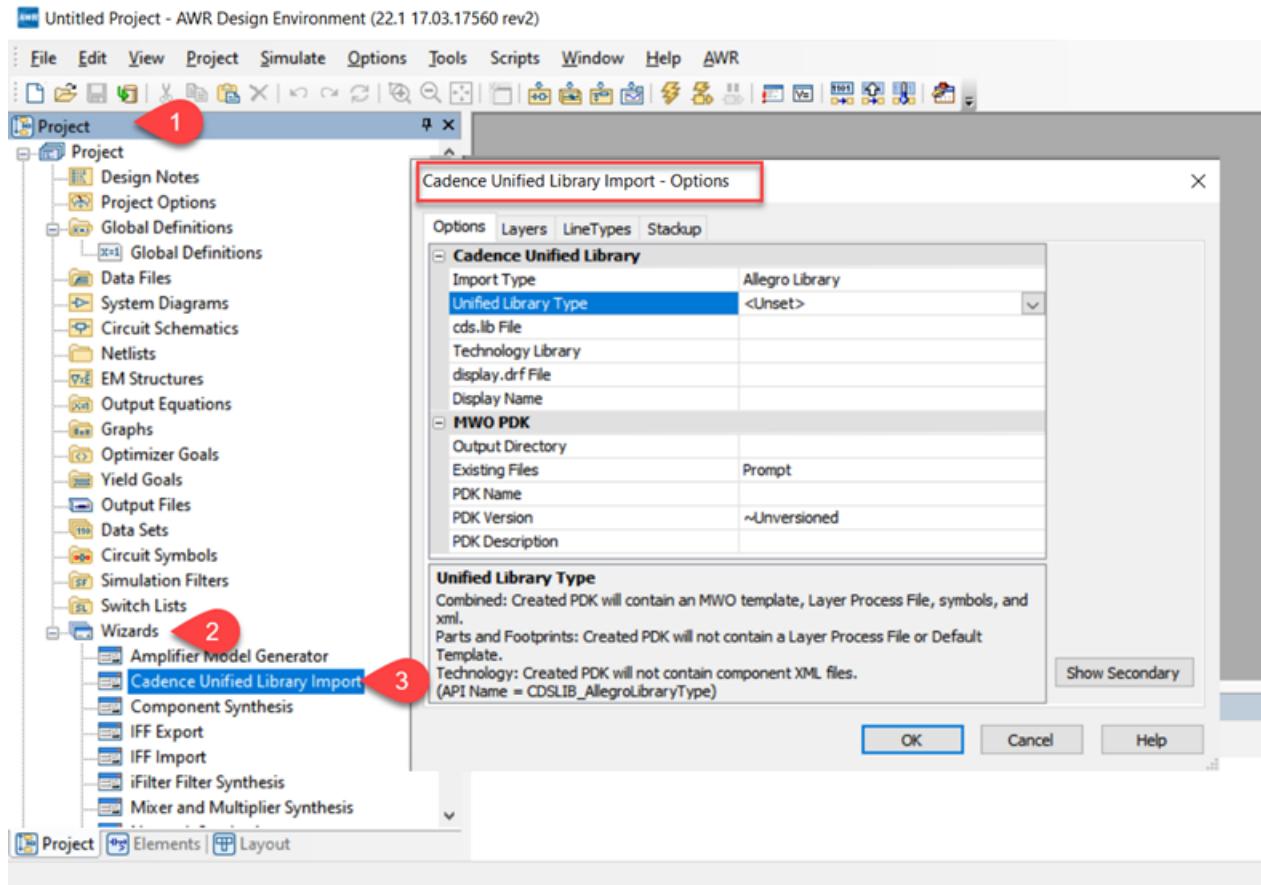
1. Start AWR Design Environment.

The AWR Design Environment main window opens with a blank project.

AWR Microwave Office-Allegro RF Design User Guide

Generating Microwave Office PDK

2. In the *Project* tab, expand the *Wizards* folder and double-click *Cadence Unified Library Import* to open the *Cadence Unified Library Import* wizard.



3. To view all the options in the *Cadence Unified Library Import - Options*, click *Show Secondary*.

Under the *Options* tab of the *Cadence Unified Library Import - Options*, additional fields are displayed.

4. To create PDK for design library, do the following:

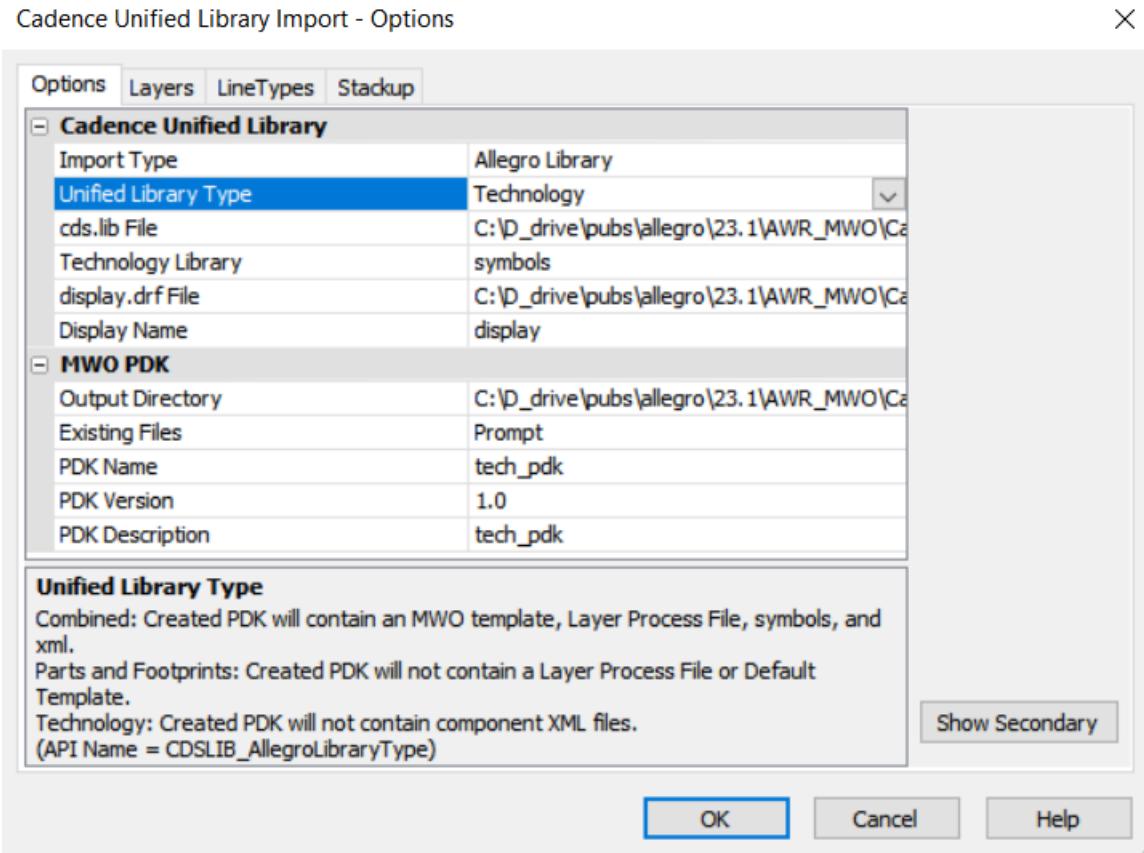
- a. Ensure that the *Import Type* is set as *Allegro Library*.
- b. Set *Unified Library Type* to *Technology*.
- c. Browse to the location of the `cds.lib` file that contains translated technology libraries.
- d. The *Technology Library* field is populated with the names of the library containing tech file (`tech.db`).

AWR Microwave Office-Allegro RF Design User Guide

Generating Microwave Office PDK

e. Specify the *Output Directory* path.

f. Specify the *PDK Version*.



g. Click *OK*.

A message displays when the process is complete and AWR PDK is generated in the output directory that contains the .ini file for PCB technology.

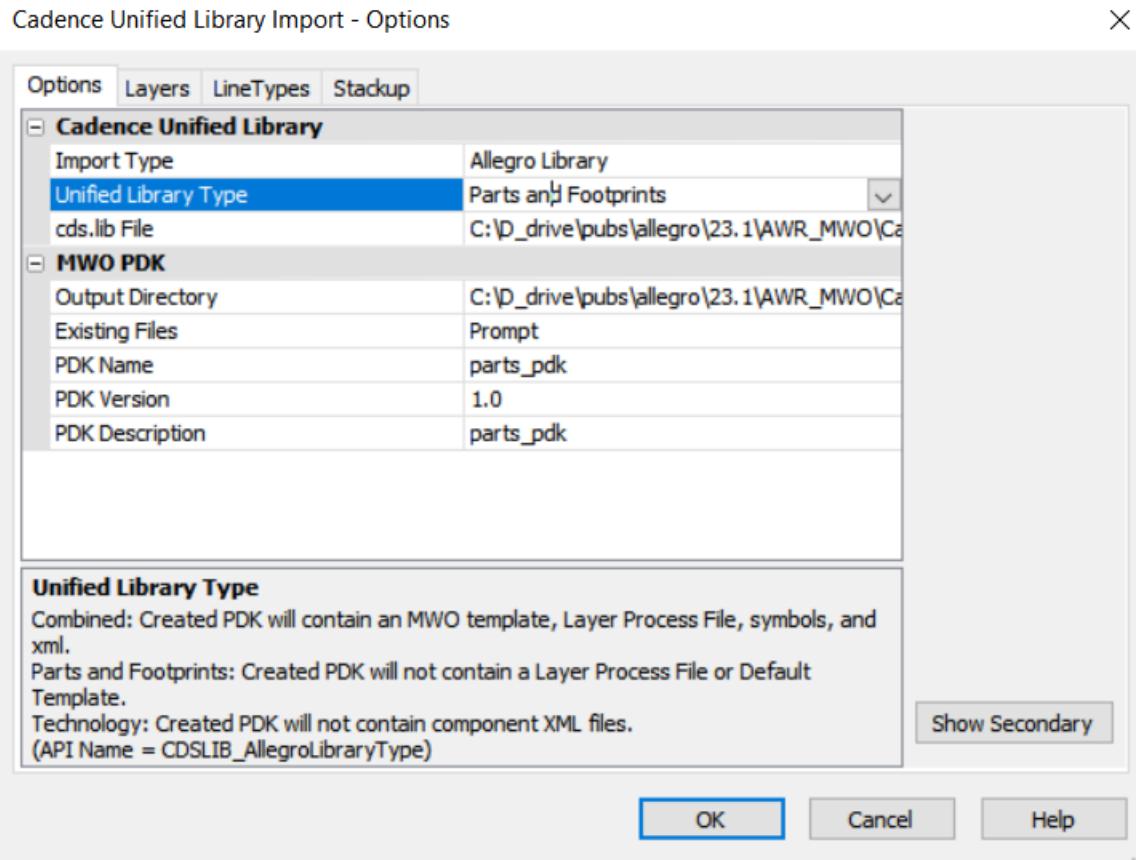
5. To create PDK for design library, do the following:

- a. Ensure that the *Import Type* is set as *Allegro Library*.
- b. Set *Unified Library Type* to *Parts and Footprints*.
- c. Specify the *Output Directory* path.

AWR Microwave Office-Allegro RF Design User Guide

Generating Microwave Office PDK

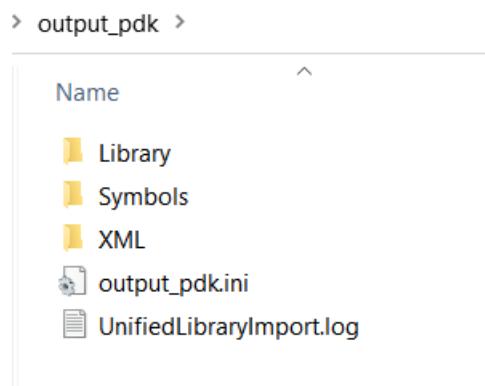
d. Specify the *PDK Version*.



e. Click *OK*.

A message displays when the process is complete and AWR PDK is generated in the output directory that contains the .ini file for parts and footprints.

PDK Structure



For more information about the *Cadence Unified Library Import* wizard, click the *Help* button to open the Cadence AWR Design Environment Help viewer or access help from the [Cadence Online Support](#) site.

Adding PDKs in Microwave Office

To include the AWR PDKs generated from Cadence unified library in AWR Design Environment, do the following:

1. Choose *File – New With Library – Browse* to select the configuration file (.ini) for design technology.
2. In the file browser, locate the .ini file and click *Select*.
A blank project is created.
3. Choose *Project – Process Library – Add/Remove Library*.

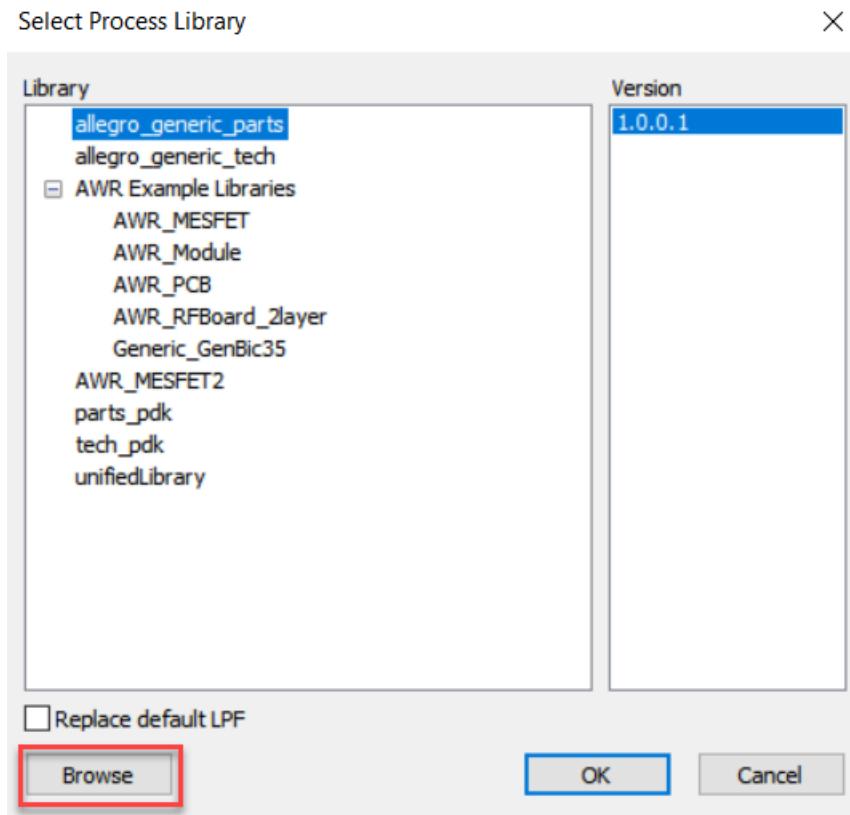
The *Add/Remove Process Library* dialog box opens and display the technology library.

4. Click *Add* to add the footprint and parts PDK.

AWR Microwave Office-Allegro RF Design User Guide

Generating Microwave Office PDK

The *Select Process Library* dialog box opens.



5. Click *Browse* to find and select the footprint and parts configuration file (.ini).
6. Click *OK* to close the *Select Process Library* dialog box.

Both technology and parts PDKs are added.

Add/Remove Process Library

Library Name	Version	Configuration File
tech_pdk	1.0	C:\D_drive\pubs\allegro\23.1\AWR_MWO\Cadence_unified_library\end_state\tech_pdk\tech_pdk.ini
parts_pdk	1.0	C:\D_drive\pubs\allegro\23.1\AWR_MWO\Cadence_unified_library\end_state\parts_pdk\parts_pdk.ini

7. Click *Browse* again to add more process libraries for your project. For example, you can add simulation libraries.
8. Click *OK* to close the *Add/Remove Process Library* dialog box.

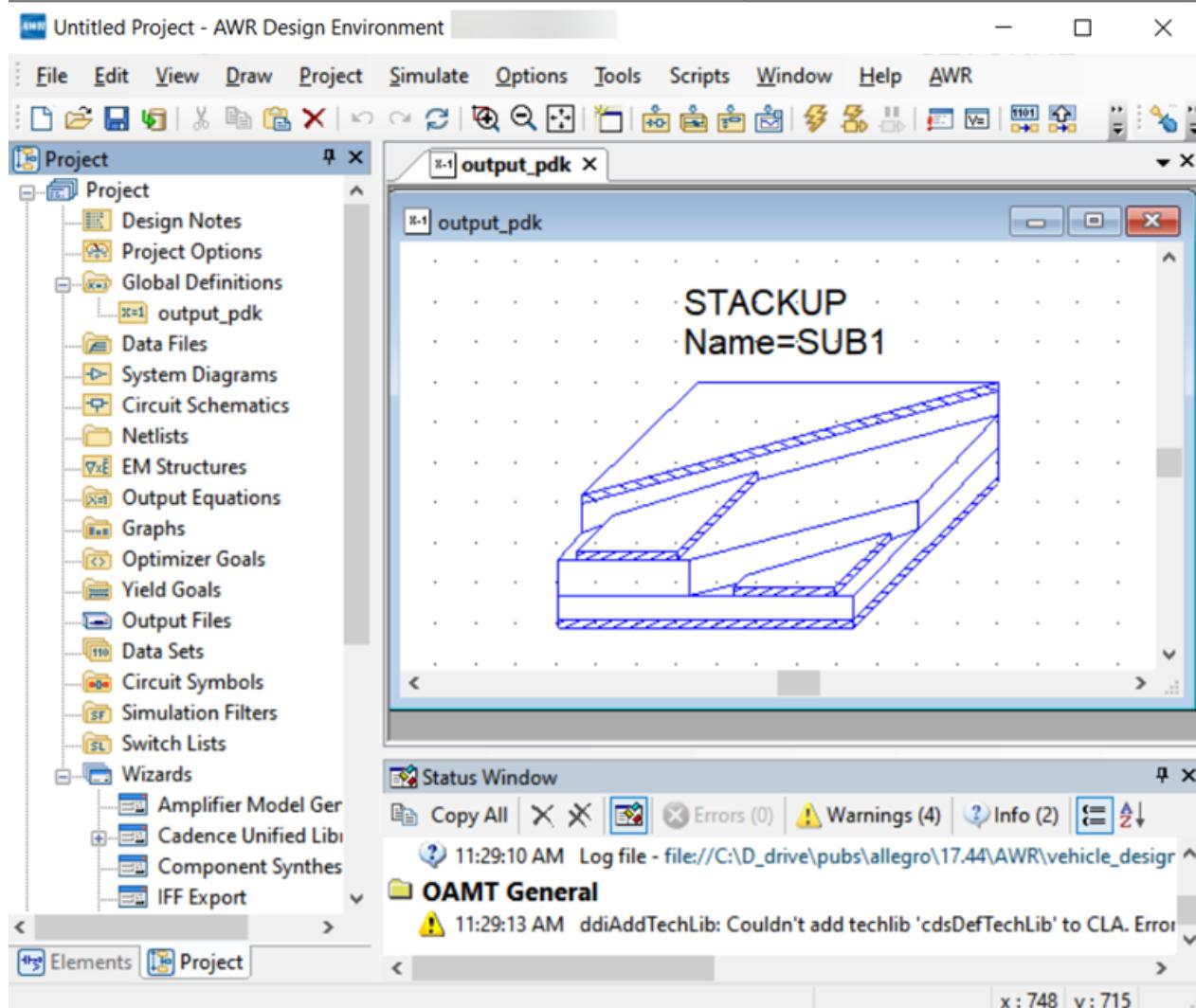
Verifying PDK Import

To check if the Allegro libraries and technology data is successfully imported, view `UnifiedLibraryImport.log` or verify it manually:

1. Click *Global Definitions* in the *Project* tab.

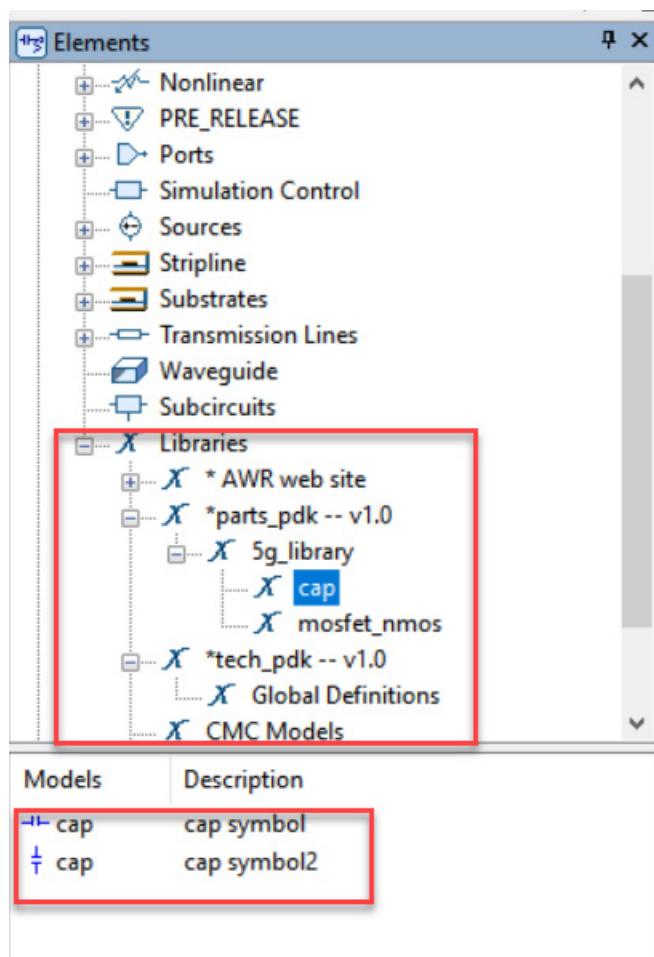
The stackup window opens in the workspace.

AWR project with Allegro stackup definition



2. Double-click stackup to open the *Element Options* dialog box.

3. Select the *EM Layer Mapping* tab to verify the layer information that was imported through Cadence Unified Library.
4. Click *OK* to close the *Element Options* dialog box.
5. In the *Elements* tab, expand the *Libraries* node.
Cadence unified library is displayed under AWR PDK.
6. Select the parts library node to view the parts that are translated from Allegro libraries.
The following image displays a sample node *5g_library*.



In the lower-left part of the window, all the versions of the component symbols are displayed.

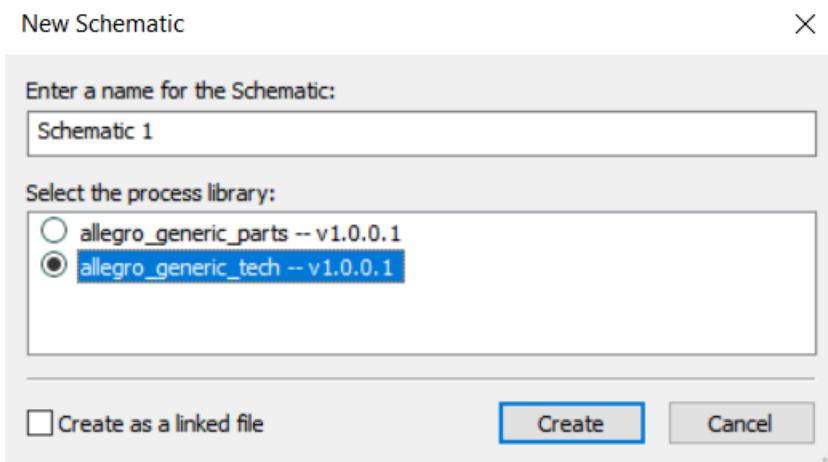
Creating RF Design Using Unified Libraries in Microwave Office

To create RF designs in Microwave Office using unified library PDK, start with creating a blank project. The new project contains manufacturable stackup and via information and a library of discrete components that was imported from Cadence unified library.

Creating Schematic in Microwave Office

Creating an RF design in Microwave Office using Cadence unified library requires the following steps:

1. In the *Project* tab, right-click *Circuit Schematics* and choose *New Schematic*.
2. The *New Schematic* dialog box opens displaying list of process libraries added to the project.
3. Optionally, specify a name for the schematic in the *New Schematic* dialog box.
4. Select the technology process library, always and click *Create*.

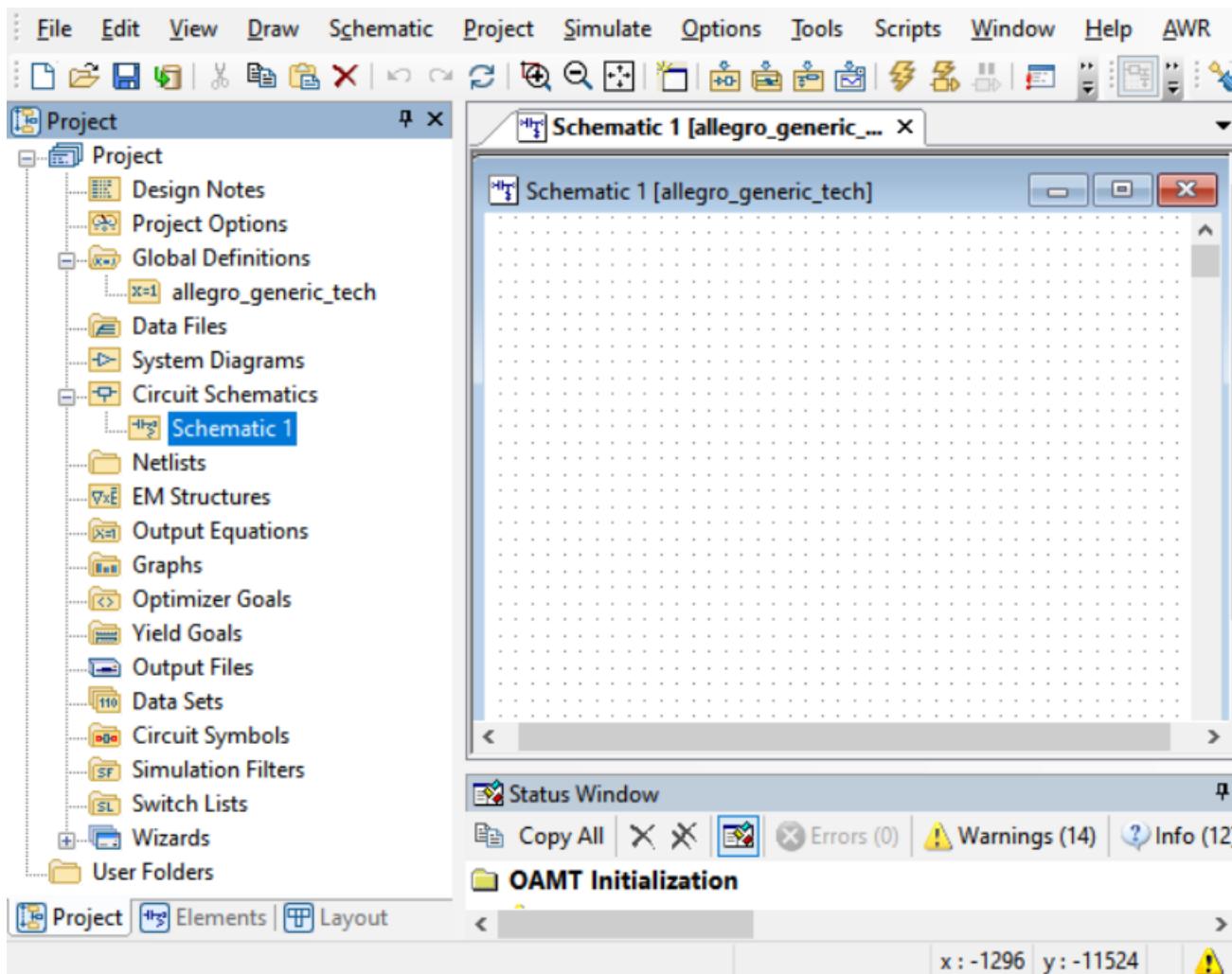


- 5.

AWR Microwave Office-Allegro RF Design User Guide

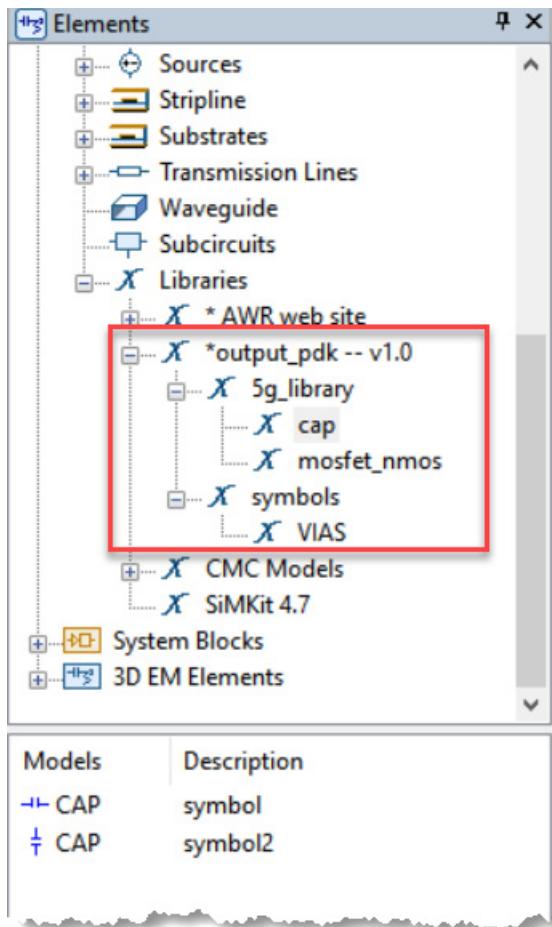
Creating RF Design Using Unified Libraries in Microwave Office

A blank schematic window opens in the workspace displaying the new schematic, and a schematic node is added under the *Circuit Schematics* in the *Project* tab.



6. To access the schematic elements, open the *Elements* tab and expand *Circuit Elements*, if required.

7. Expand the *Libraries* node to view the discrete components imported through the Cadence unified library.



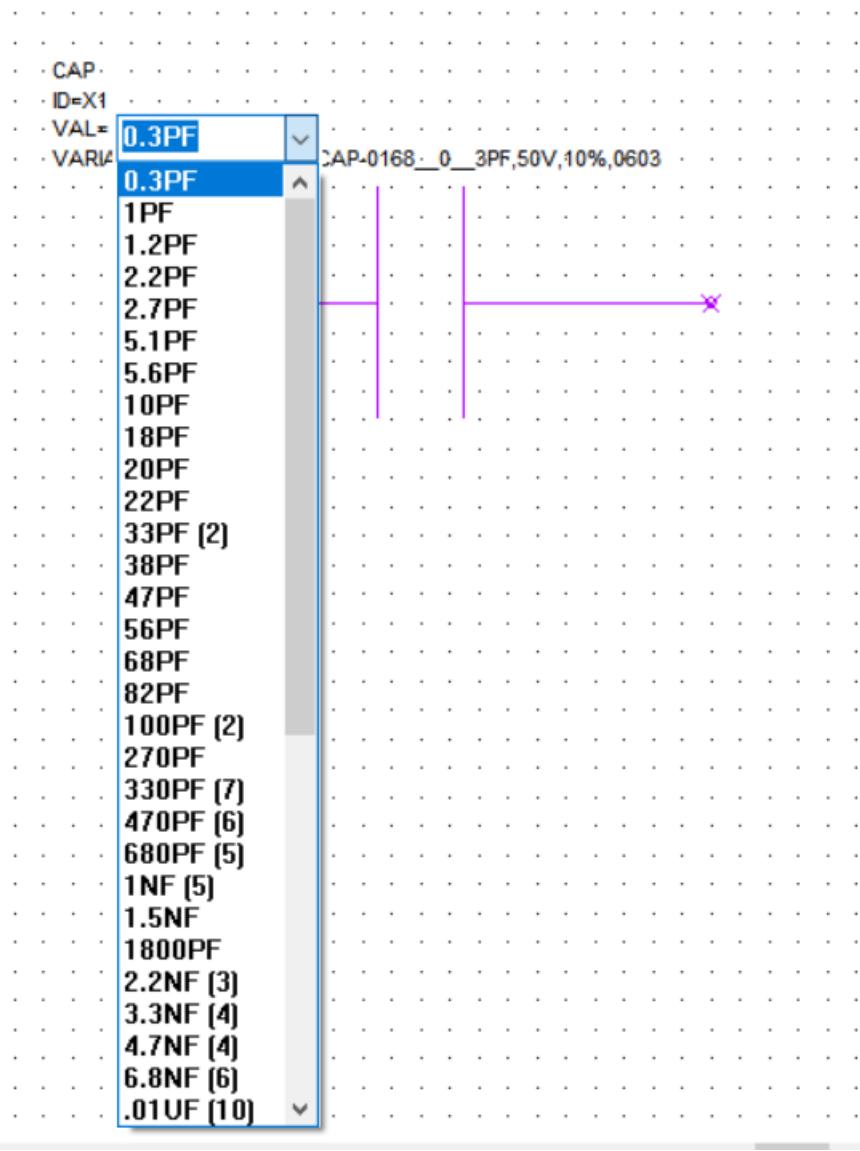
8. Double-click to expand the PDK generated from Cadence unified library to select a component for placement.

All the available versions of a component symbol display in the lower-left part of the window.

9. To place a discrete component, click to select it from the list of *Models* drag it into the schematic window, and click to place it.
10. To rotate, flip, or mirror the component, select the model in the schematic window and choose *Edit* menu commands.
11. You can modify the value of the placed component. To do so:
 - a. Double-click the *VAL* field.

The field becomes editable.

- b. Choose a value from a drop-down list populated from part table file.

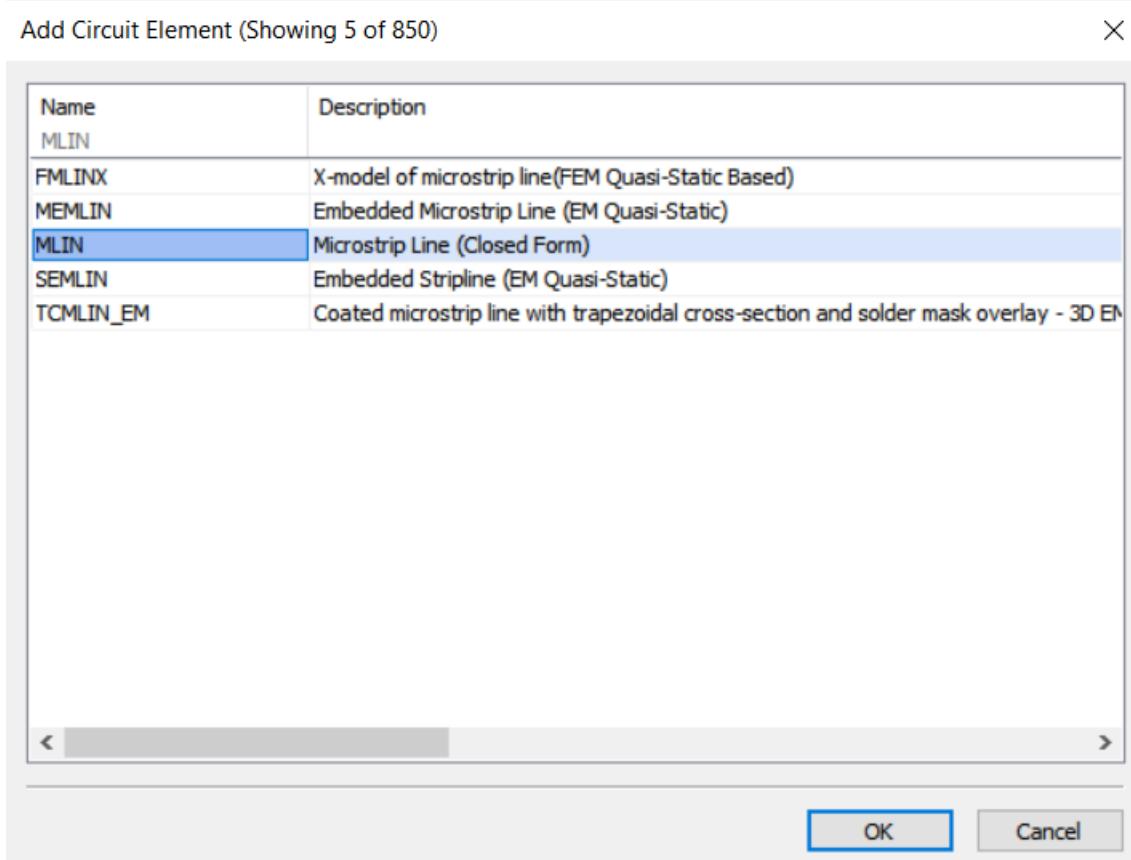


12. To place the default parameterized RF components, such as MLIN and STRIPLINE:

- Choose *Draw – More Elements* or click the *Element*  button from the Schematic Design toolbar.
- In the *Add Circuit Element* dialog box, click in the *Name* column to enable the filter.
- In the filter field, type `MLIN` or the name of the RF component and click *Enter*.

- d. Double-click an element row to select an MLIN or an RF component from the filtered list.

The dialog box closes and the selected component attaches to the cursor.



- e. Click to place the MLIN component in the schematic window and modify its width and size by double-clicking the W and L fields.

For information on how to add elements to the new schematic, see [Adding Elements Using the Elements Browser](#).

13. Similarly, add a via in the schematic:

- a. Search for `via` in the *Add Circuit Element* dialog box.
- b. Select a via from the filtered list.
- c. Place the via in the schematic.

14. To connect two elements with a wire:

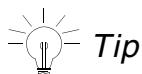
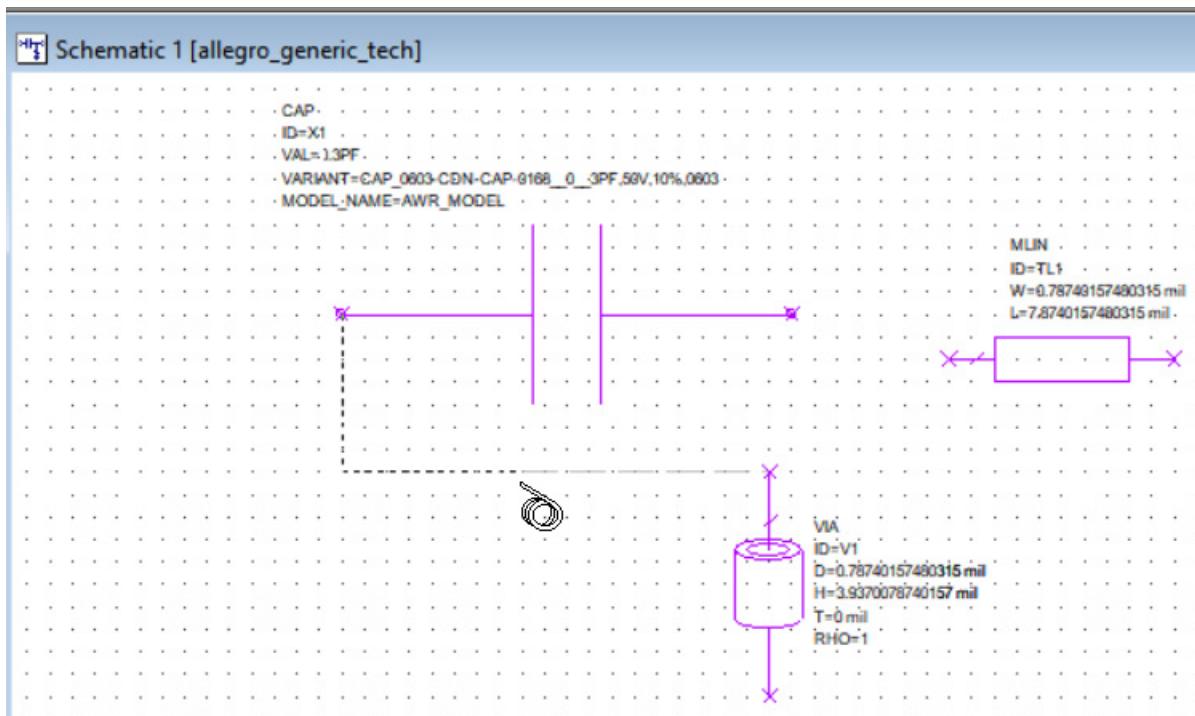
AWR Microwave Office-Allegro RF Design User Guide

Creating RF Design Using Unified Libraries in Microwave Office

- a. Place the cursor over a node in the schematic window.

The cursor displays as a wire coil symbol.

- b. Click to start a wire, drag the mouse, and click again to complete the connection.



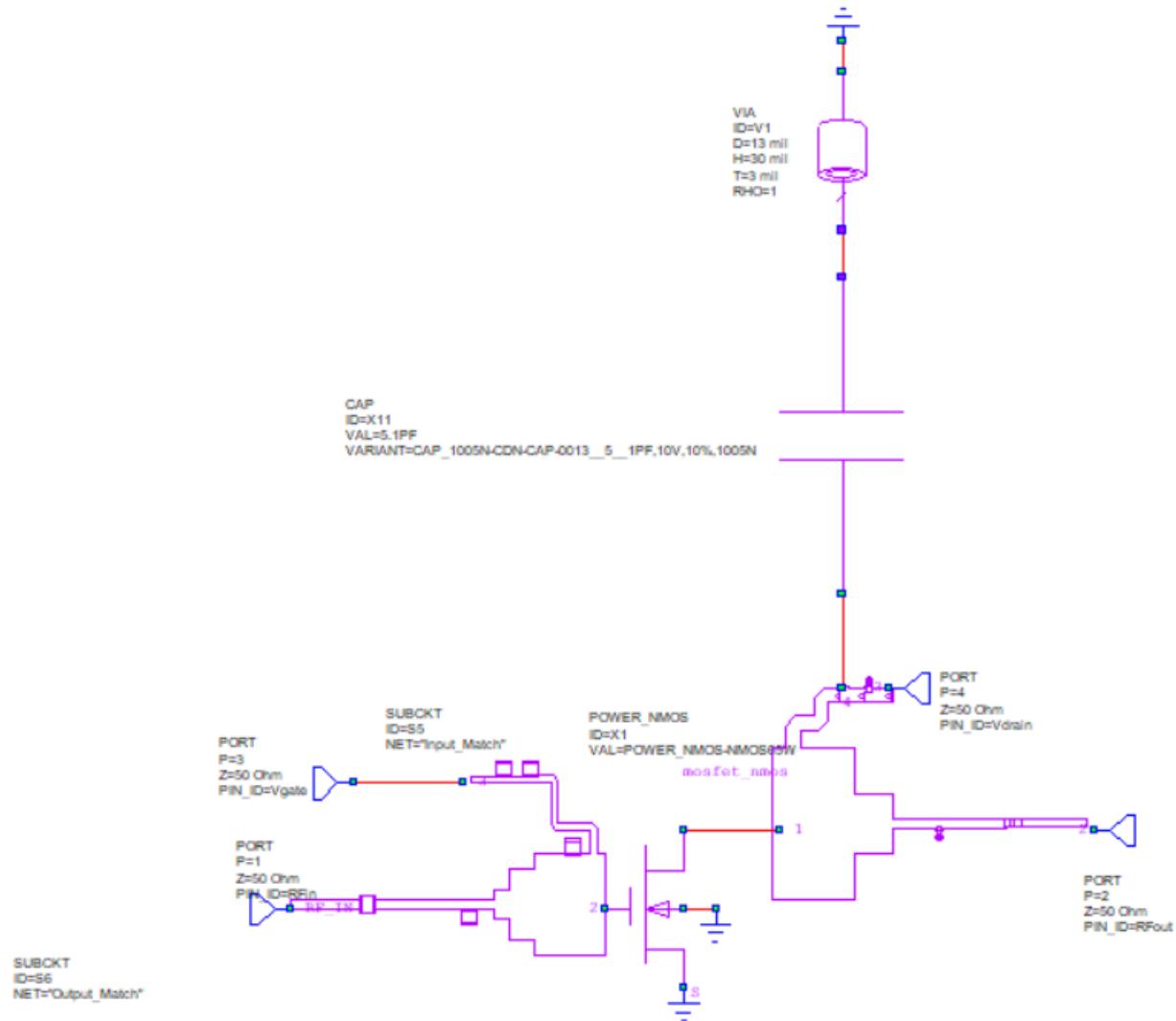
Tip
While placing a new component, a smart guide (dotted/dashed) line is displayed to ensure that the component is vertically or horizontally aligned with a node on an existing component. Holding the Shift key while adding the component at this point ensures that a wire connection is created.

15. Repeat steps 6 to 13 to create the complete RF schematic using the discrete components from the unified library PDK.

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Creating RF Design Using Unified Libraries in Microwave Office

The following illustration depicts a sample RF schematic created in Microwave Office using Cadence unified libraries.



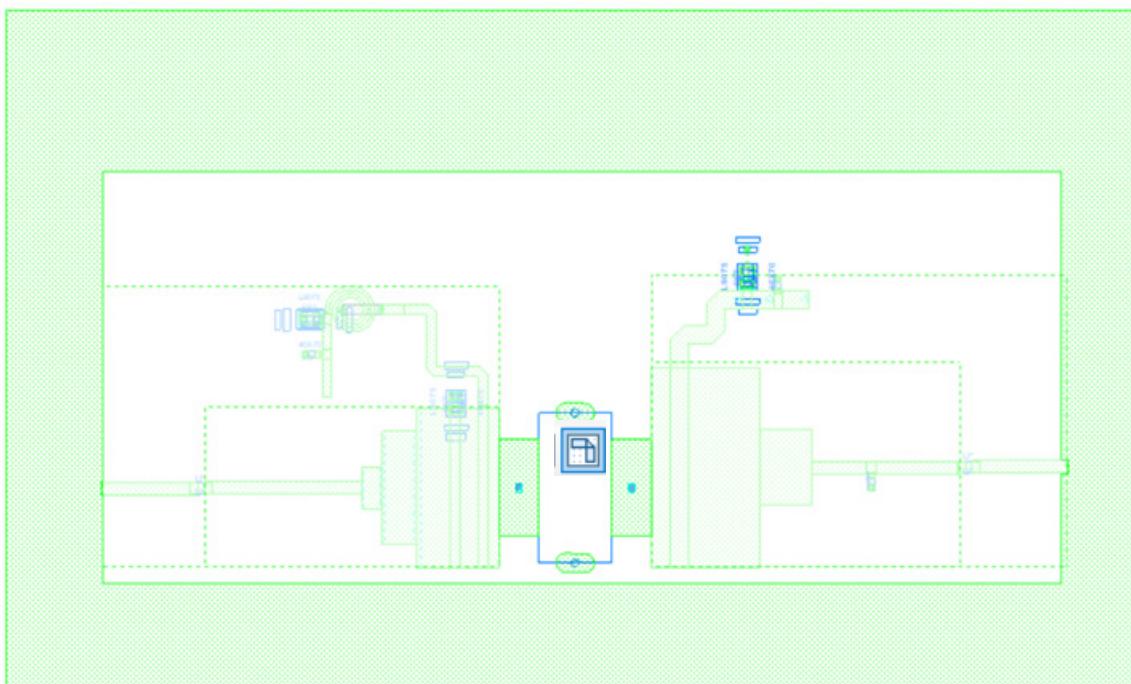
Managing Layout and Footprints in Microwave Office

The single intelligent database of Microwave Office automatically creates the physical view of the RF design as you add components and make connections between them in the schematic. The layout representations of the components already associated with their corresponding electrical symbols are placed and connected while you create the schematic. With a single database any change in the component is reflected in both the layout and the schematic simultaneously.

- To view the layout, choose *View – View Layout* or click the *View Layout*  button.

A new window *Layout View* opens displaying the layout representation of the schematic objects. For discrete components, the layout is added from the Cadence unified library that contains footprint symbols. For in-built parameterized RF components, the default layout representation is used.

The following image illustrates the layout view of the sample RF schematic.



The via used in the layout is specific to the PCB design used for translating Allegro libraries. The information of this via is embedded in the technology file and is translated when PDK is created. The connections between footprints in the layout are made using EM structures, iNets, and GDS components.

Both the layout and the schematic require updates to make the design simulation ready. You can do the following to modify the footprints or the connectivity elements.

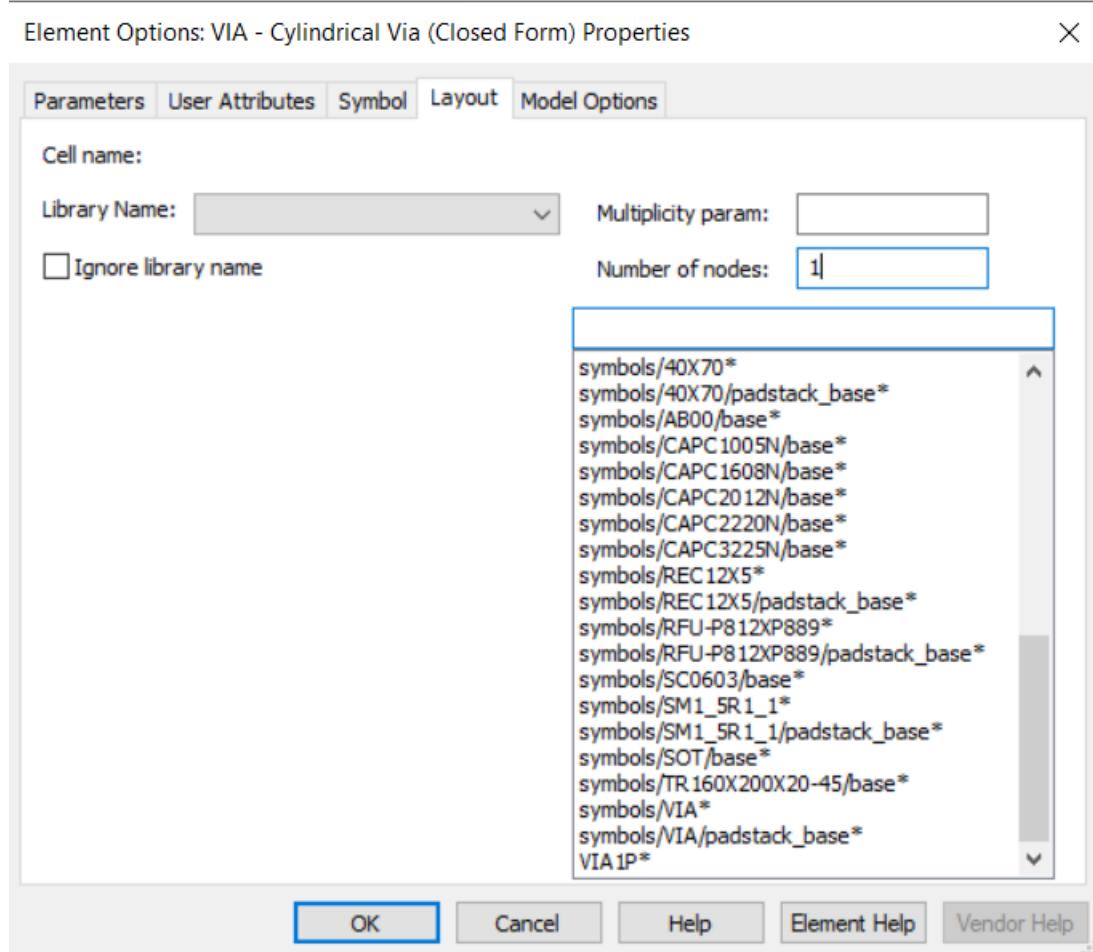
Adding Via Layout

To attach via layout with its schematic representation, do the following:

1. In the schematic window, select a placed via.
2. Right-click and choose *Properties*.

The *Element Options* dialog box is displayed.

3. Open the *Layout* tab, set the number of nodes to 1.
4. Select the layout from technology file (`techfile/VIA*`) from the list of available layouts for via.



5. Click *OK* in the *Elements Options* dialog box.

The design-specific via layout is attached to the via schematic symbol.

Modifying Footprint Parameters in Layout

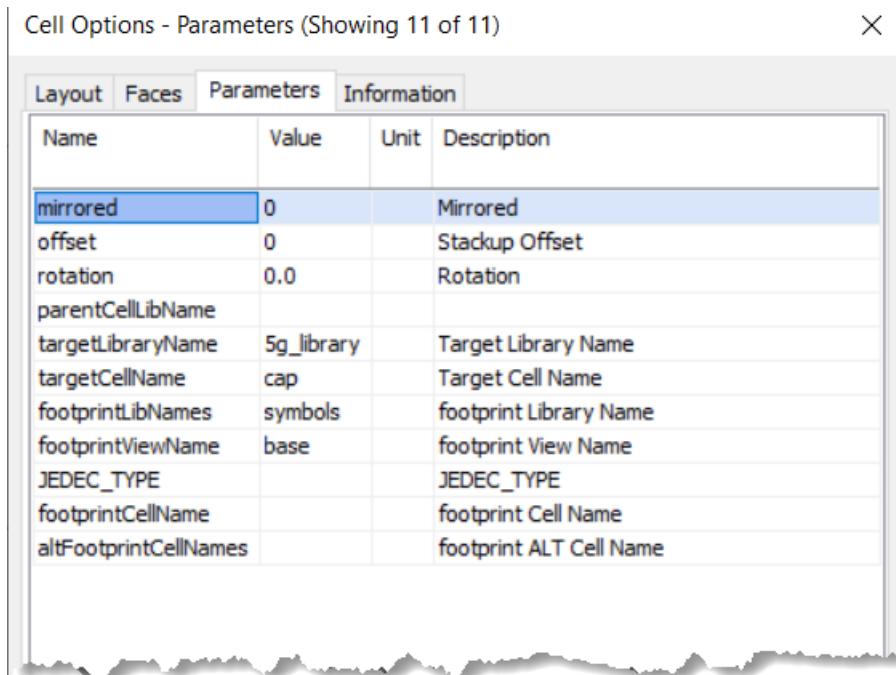
You can change the properties of the footprint symbol of discrete components in the layout view using the following steps:

1. Select the footprint of a discrete component in the layout.

2. Right-click and choose *Shape Properties*.

The *Cell Options* dialog box is displayed.

3. Open the *Parameters* tab and modify the mirror or rotation and click *OK*.



The selected component is rotated by the specified value or mirrored in the layout window.

Modifying Properties of RF Elements

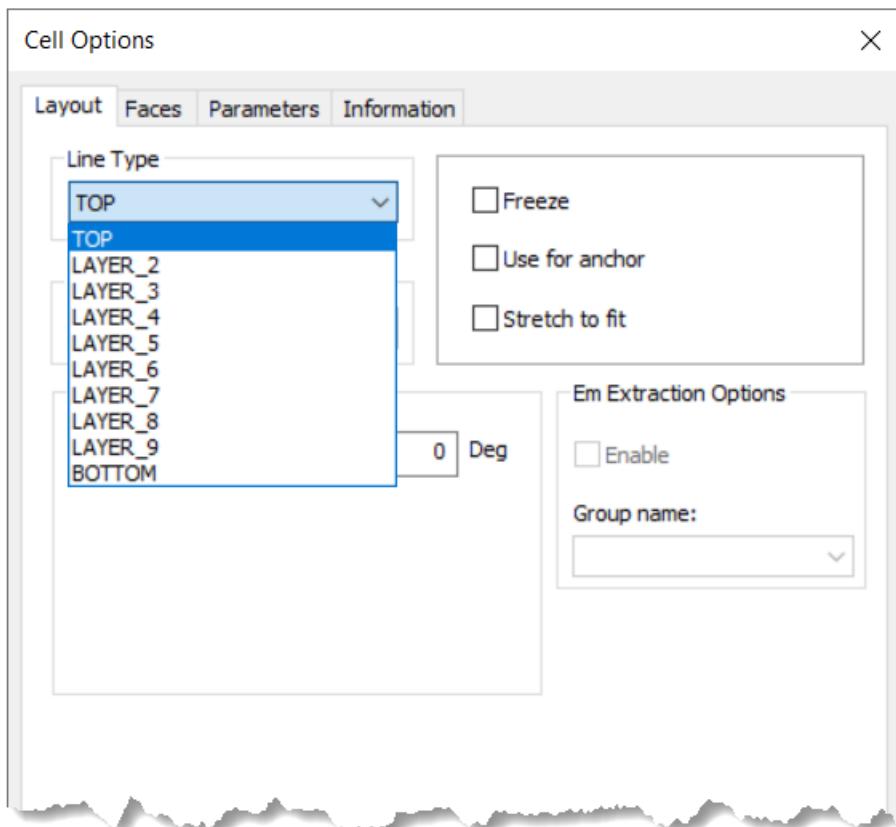
The size and placement of RF elements can be changed in the layout.

1. Select an MLIN component and open the *Cell Options* dialog box.

AWR Microwave Office-Allegro RF Design User Guide

Creating RF Design Using Unified Libraries in Microwave Office

2. In the *Layout* tab, change the layer name to move it from the layer on which it was placed.



3. Click *OK* in the *Cell Options* dialog box.
4. Choose *View – View 3D Layout* to verify that the MLIN is moved to the new layer.

For more information on creating and viewing layouts for RF schematic created in Microwave Office, refer to [AWR Microwave Office Layout Guide](#) on the [Cadence Online Support](#) site.

AWR Microwave Office-Allegro RF Design User Guide
Creating RF Design Using Unified Libraries in Microwave Office

Simulating RF Designs in Microwave Office

In Microwave Office, you can choose various measurements to run and analyze the output in a graphical or file format. The measurement you select to analyze is a computed data generated as a result of a simulation, such as gain, noise, power, or voltage that helps evaluate functionality of the RF design.

Simulating RF Design Using Graph

To create a new graph in Microwave Office, do the following:

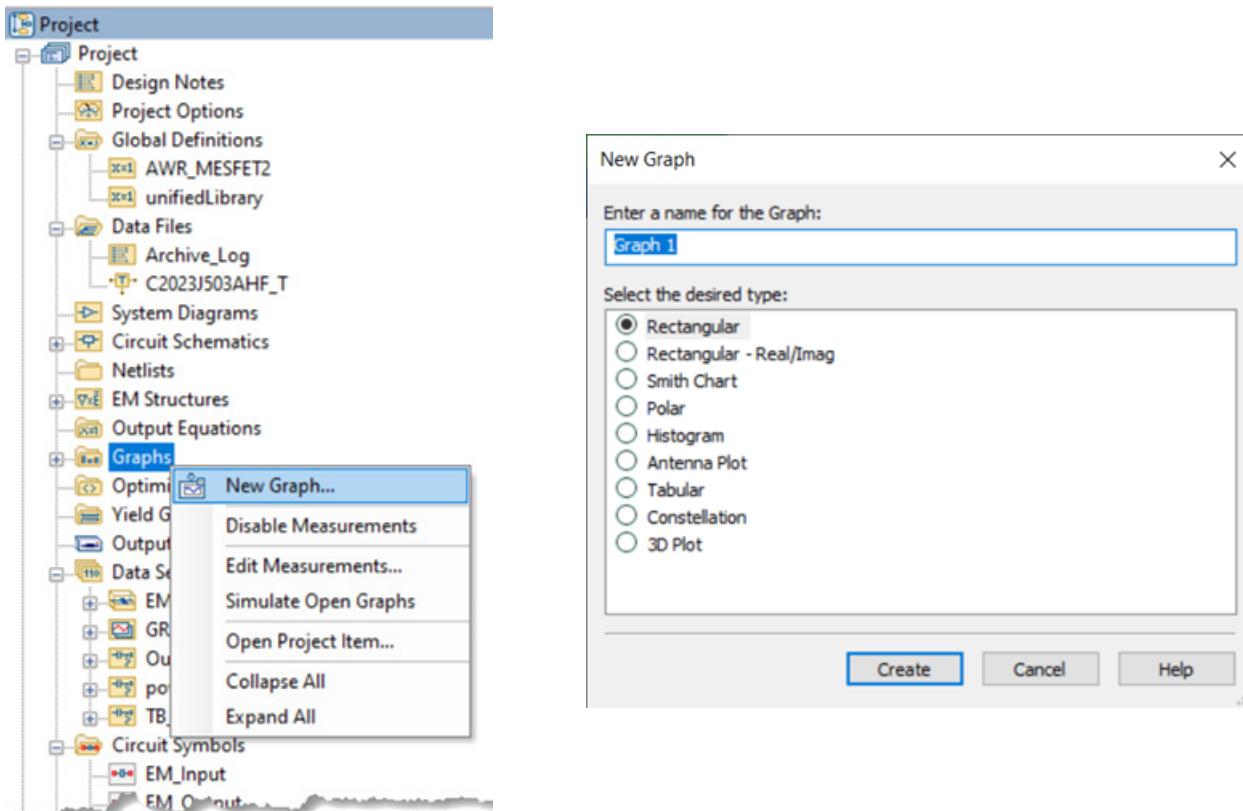
1. In the AWR Design Environment window, right-click *Graphs* in the *Project* tree, and choose *New Graph*.

The *New Graph* dialog box is displayed.

AWR Microwave Office-Allegro RF Design User Guide

Simulating RF Designs in Microwave Office

2. Specify a name for the graph, select a type and click *Create*.



An empty graph window opens and the new graph is added under the *Graphs* node in the *Project* browser.

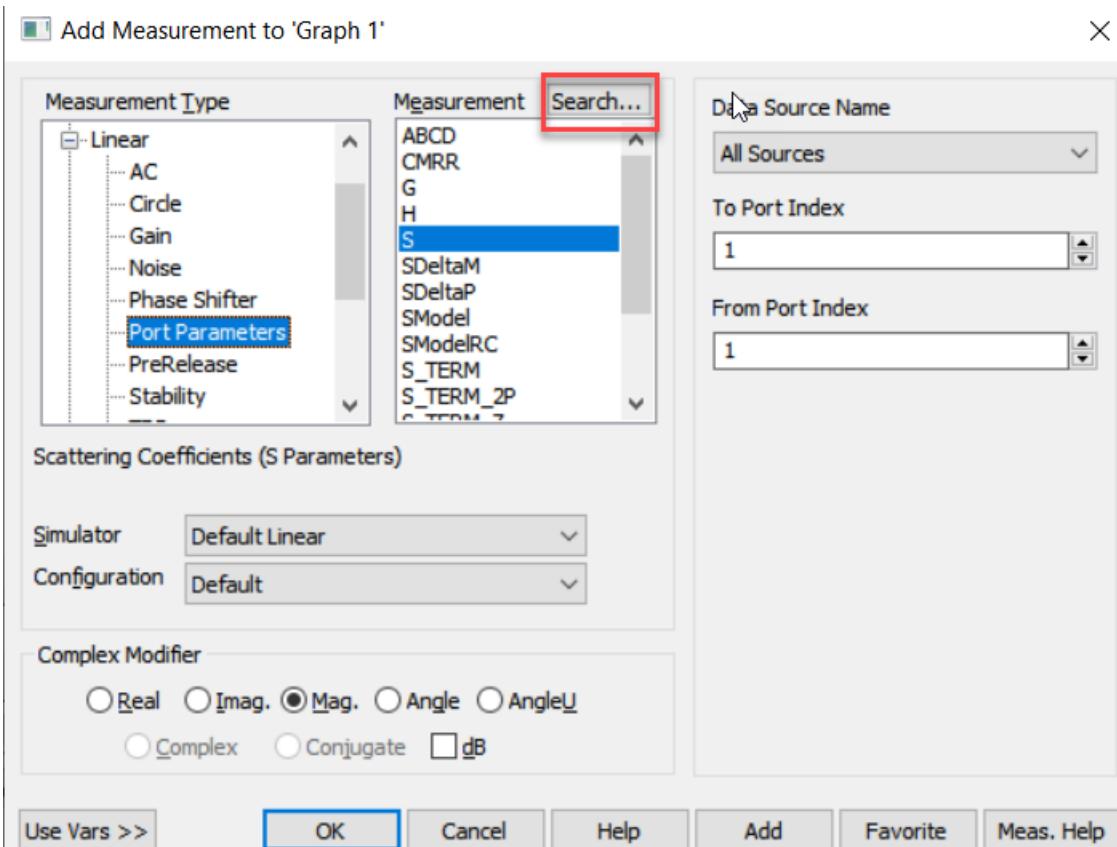
3. To add measurements to this graph, right-click the new graph node and choose *Add Measurement*.

The *Add Measurement* dialog box is displayed.

AWR Microwave Office-Allegro RF Design User Guide

Simulating RF Designs in Microwave Office

4. Click *Search* in the *Measurement* section to select a measurement by name, description, or category.

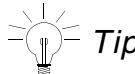
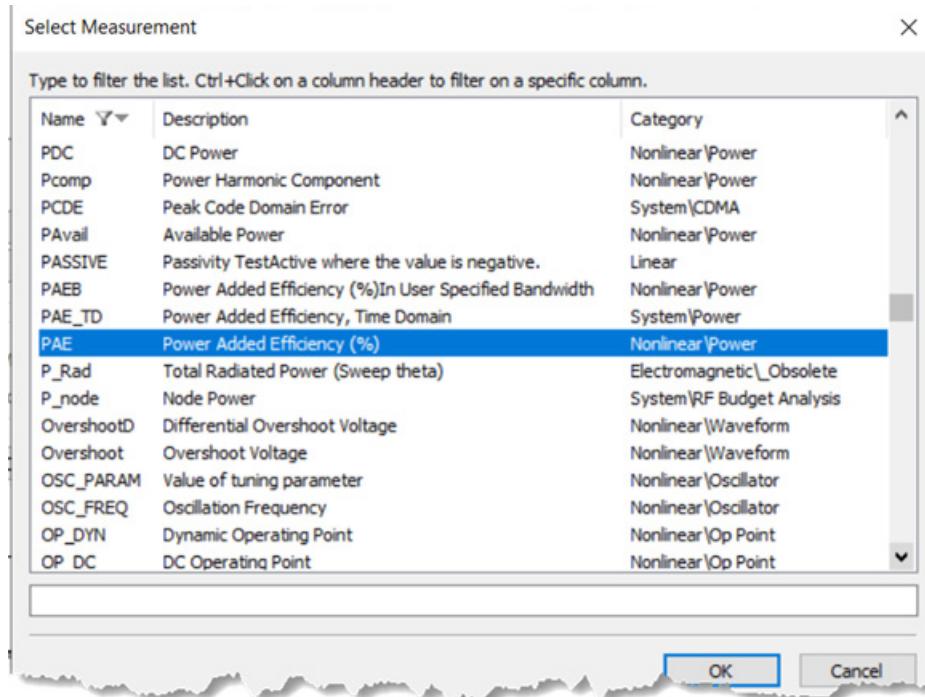


The *Select Measurement* dialog box opens.

AWR Microwave Office-Allegro RF Design User Guide

Simulating RF Designs in Microwave Office

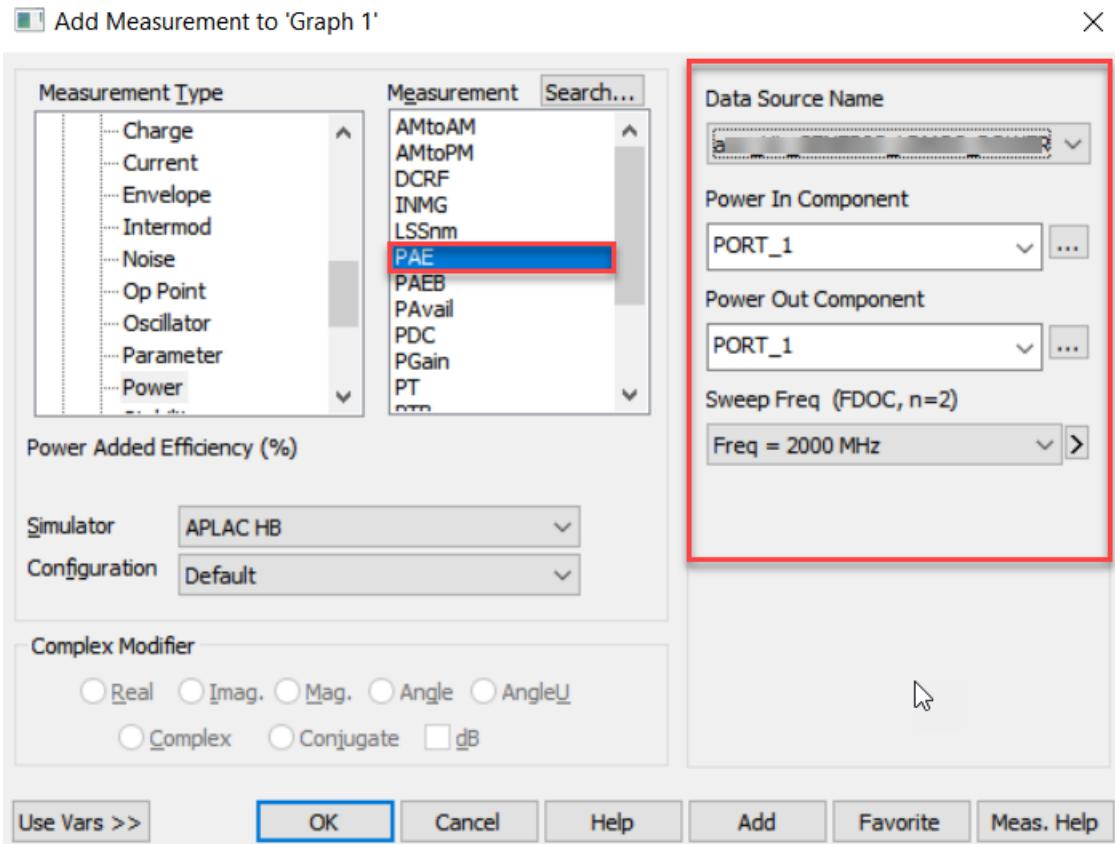
5. Select the measurement type and click *OK*.



Tip
For more details about a measurement, select its name and click the *Meas. Help* button. The Cadence AWR Design Environment Help viewer opens and displays the information on the selected measurement.

6. Specify the *Data Source Name*, which is the name of the RF design.

7. Choose the input and output components and sweep frequency, and click *OK*.



The measurement is added under the new graph in the *Project* browser.

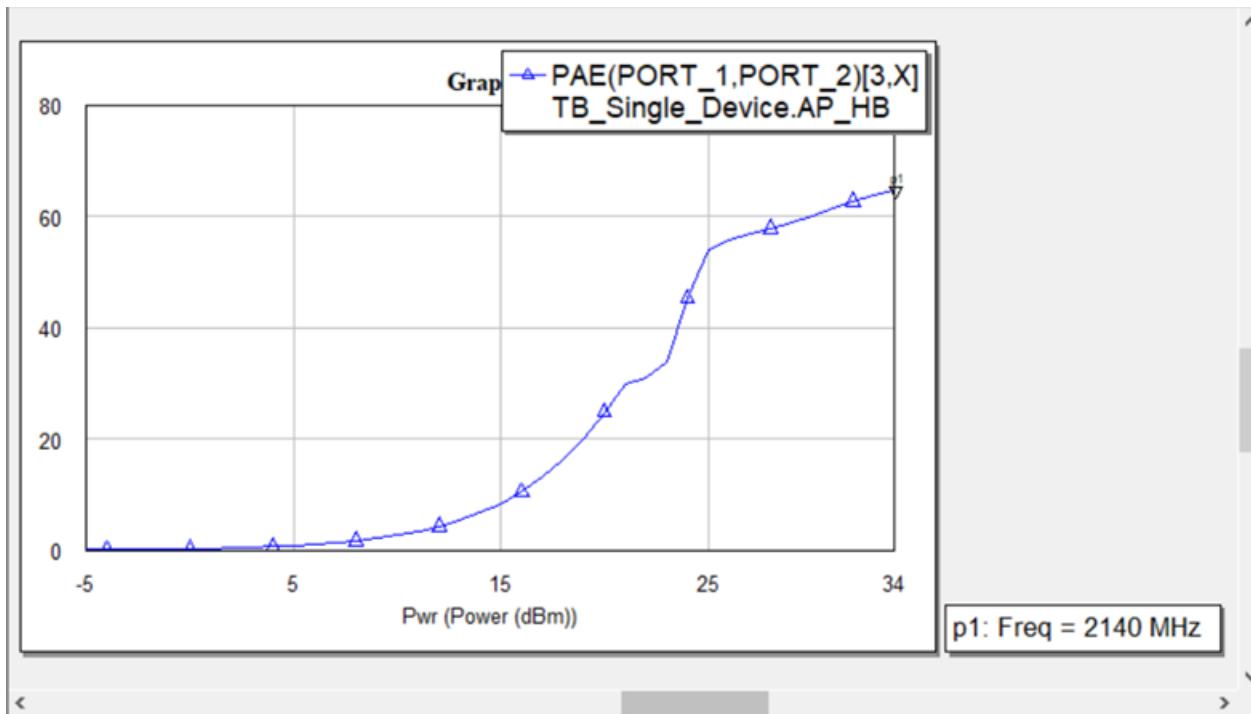
For more information about the *Add Measurement* dialog box, click the *Help* button to open the Cadence AWR Design Environment Help viewer or access the help from the [Cadence Online Support](#) site.

8. To simulate the graph, right-click and choose *Simulate for Measurement*.

AWR Microwave Office-Allegro RF Design User Guide

Simulating RF Designs in Microwave Office

The graph is generated when the simulation is completed. The following image illustrates PAE versus input power simulation results for the sample design.



9. To generate analysis results in file format, select *Output Files* in the *Project* browser.
10. Right-click *Output Files* and choose *Add Output File*.

The *Add Output File* dialog box opens.

11. Select a measurement that matches with the data file type.
12. Specify the *Data Source Name*, *File Name*, and other options.
13. Click *OK* in the *Add Output File* dialog box.

The output file is generated in the specified location.

For more information on Output Files, access the help from the [Cadence Online Support](#) site.

Exporting RF Design from Microwave Office

RF Design created in Microwave Office using Allegro libraries can be exported to Allegro PCB Design applications for creating PCBs. Microwave Office exports schematic and layout data in the form of Allegro Single Container (.asc) format.

Exporting RF Design from Microwave Office

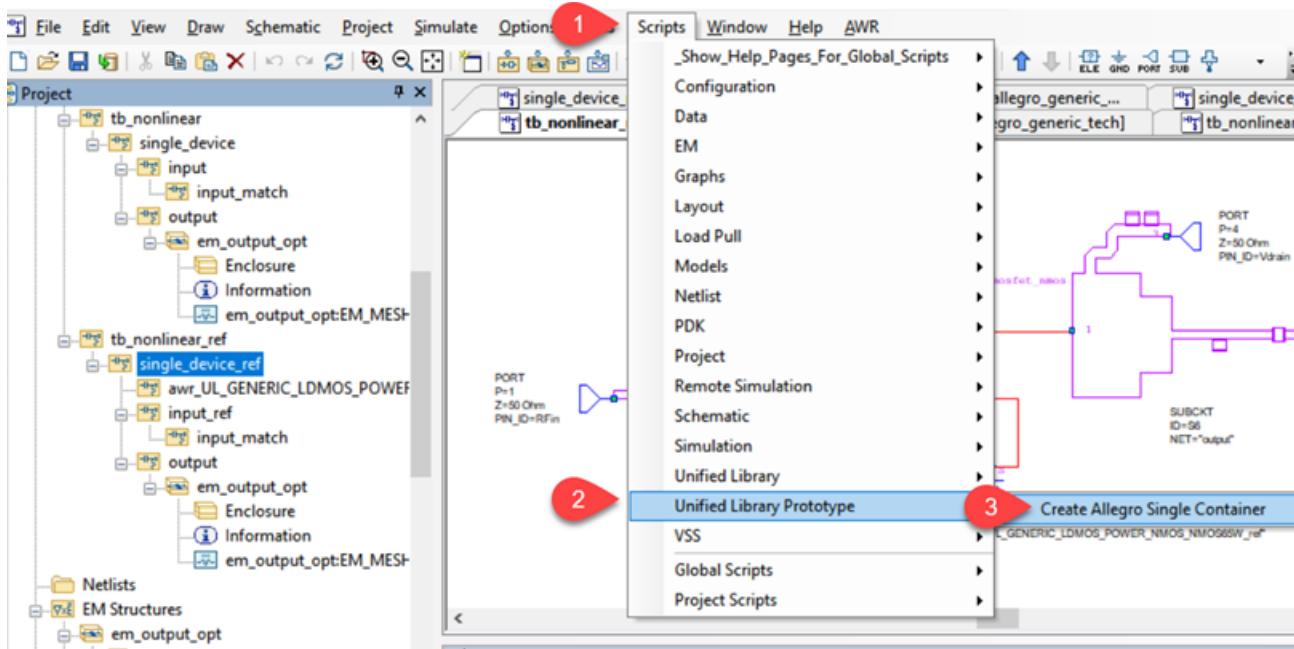
You can export an RF design from Microwave Office to Cadence unified library, which is consumed by Allegro PCB Design applications. To export the design data as a Allegro Single Container, do the following:

1. In the *Project* browser, expand the *Circuit Schematics* node and select the design name.

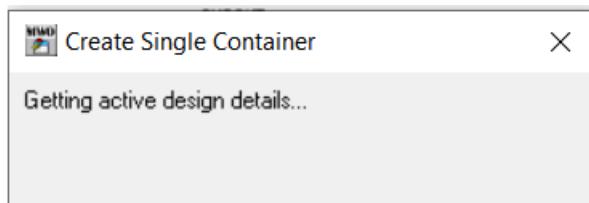
AWR Microwave Office-Allegro RF Design User Guide

Exporting RF Design from Microwave Office

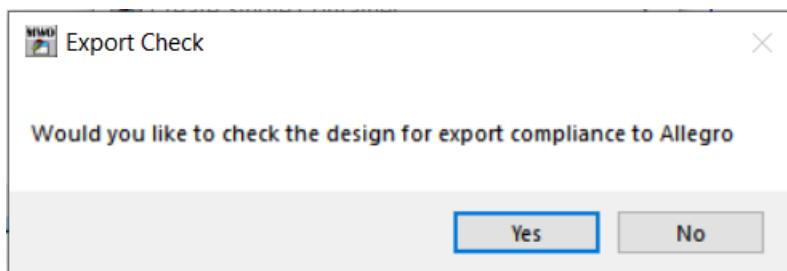
2. To export the RF schematic and layout, choose *Script – Unified Library Prototype – Create Allegro Single Container*.



The export process starts to generate Allegro Single Container.



3. Click *No* to skip the design checks in the message that appears.



A message is displayed when the export process is completed and Allegro Single Container is created for the design in the export directory location.

4. Click *OK* to close the message.

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Exporting RF Design from Microwave Office

A .asc file with the project name is created in the working directory.

5. In the *Status* window, click the link to view the `single_container.txt` file.

AWR Microwave Office-Allegro RF Design User Guide

Exporting RF Design from Microwave Office

Reusing Microwave Office RF Designs in Allegro Applications

RF design created in Microwave Office when imported as an Allegro Single Container into Allegro System Capture creates an RF block. The layout of the RF block can be created by importing Allegro Single Container to Allegro PCB Editor and saved as an RF module. The RF block, if marked for physical and logical reuse, can be instantiated as a reused RF block in an existing schematic design, which, when transferred to Allegro PCB Editor, allows the placement of reused RF modules inside a mother PCB.

Importing Cadence Unified Library to Allegro PCB Design Applications for RF Reuse

The RF design created in Microwave Office can be transferred to an existing Allegro PCB design tools by importing an ASC file.

Prerequisite

Ensure that the `cds.lib` contains all the reference and design libraries that are translated by Cadence Unified Library Translator. To include the necessary libraries for an Allegro System Capture project, you can set the system variable `CDS_SITE`, which points to the directory containing the `cds.lib` file or edit it manually.

The following steps guide you through the import process:

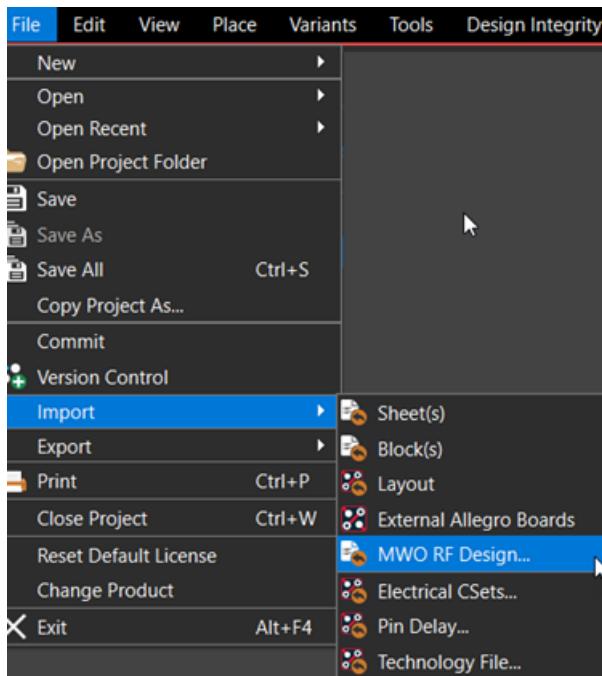
1. Start Allegro System Capture.
2. In the *Cadence Product Choices* dialog box, select *Allegro Design Authoring*.
3. Choose *File – Open Project* to open an existing non-RF schematic design in which you want to import the RF design created in Microwave Office.

Alternatively, create a new non-RF schematic design from scratch in Allegro System Capture.

AWR Microwave Office-Allegro RF Design User Guide

Reusing Microwave Office RF Designs in Allegro Applications

4. Choose *File – Import – MWO RF Design* to import the Allegro Single Container.



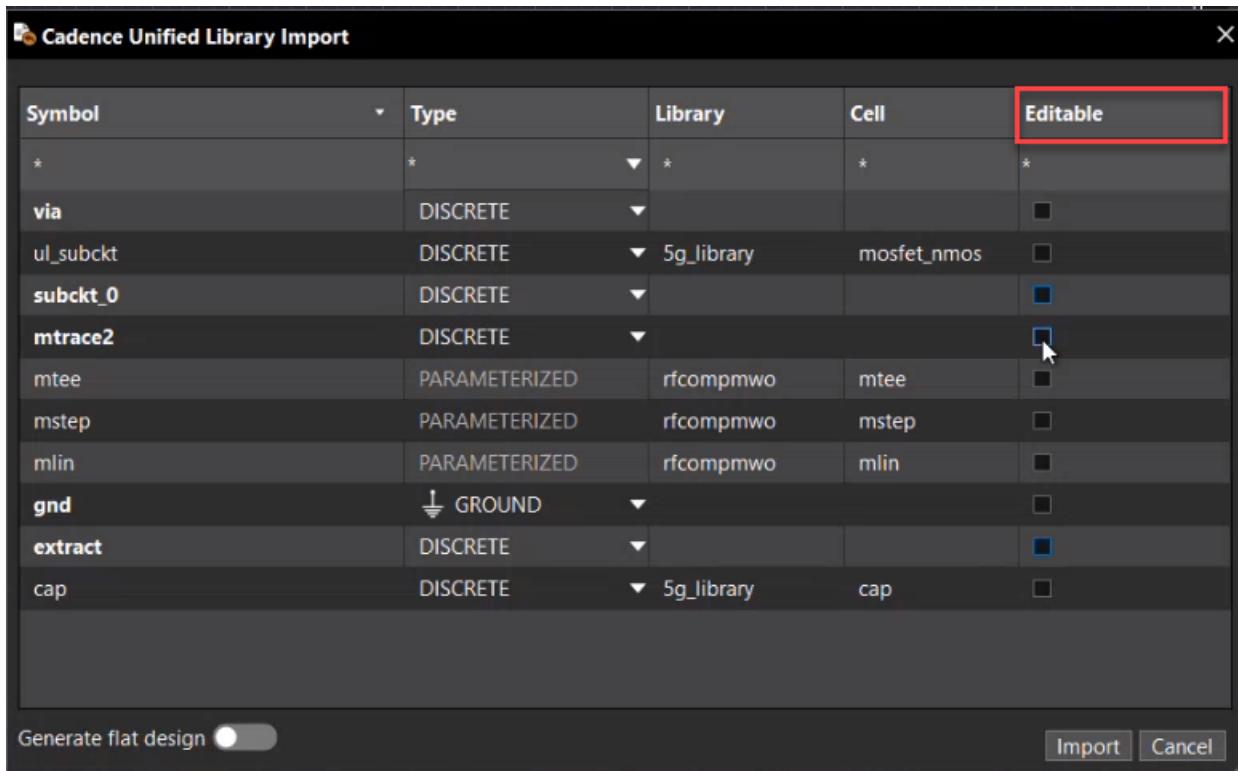
5. In the file browser that opens, browse to the location of the .asc file and click *Open*.

The *Cadence Unified Library Import* dialog box opens. The unmapped parts from the Allegro Single Container can be selected under the *Editable* column before the import

AWR Microwave Office-Allegro RF Design User Guide

Reusing Microwave Office RF Designs in Allegro Applications

process. Such components become unlocked and can later be replaced with components from Allegro libraries.



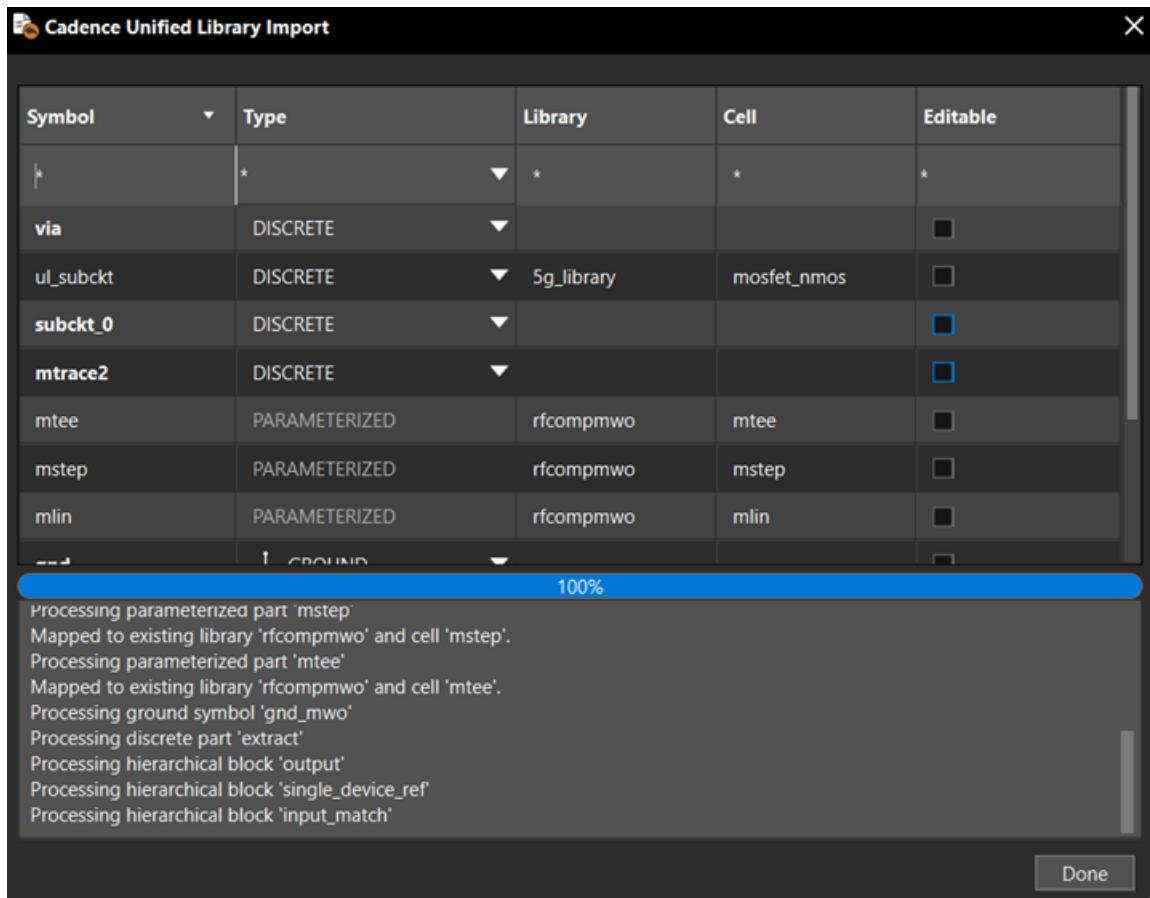
Note: When the *Generate flat design* option is selected, the RF design is imported as a flat design rather than as an RF block. However, this option works only when you import the RF design in a blank project.

6. Click *Import* to start the import process.

AWR Microwave Office-Allegro RF Design User Guide

Reusing Microwave Office RF Designs in Allegro Applications

7. Click *Done* after the import is completed.



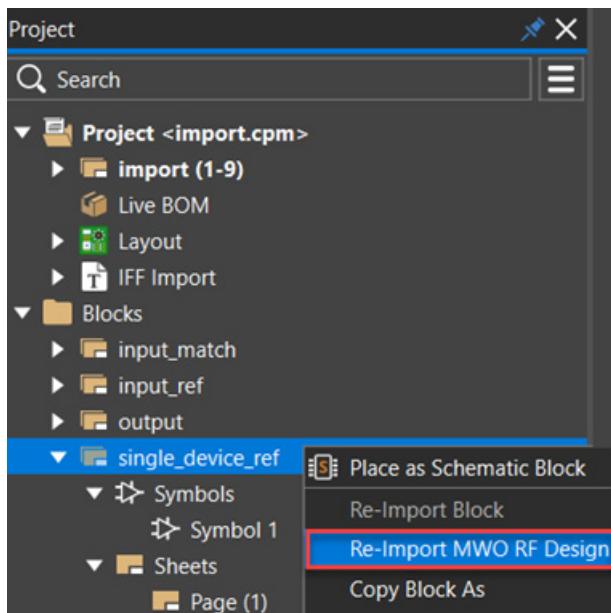
The RF design is imported as schematic block of the Allegro System Capture project.

Note: The same RF block can be re-imported to accommodate updates made to Microwave Office RF design after sign off. Only the top-level Microwave Office RF design

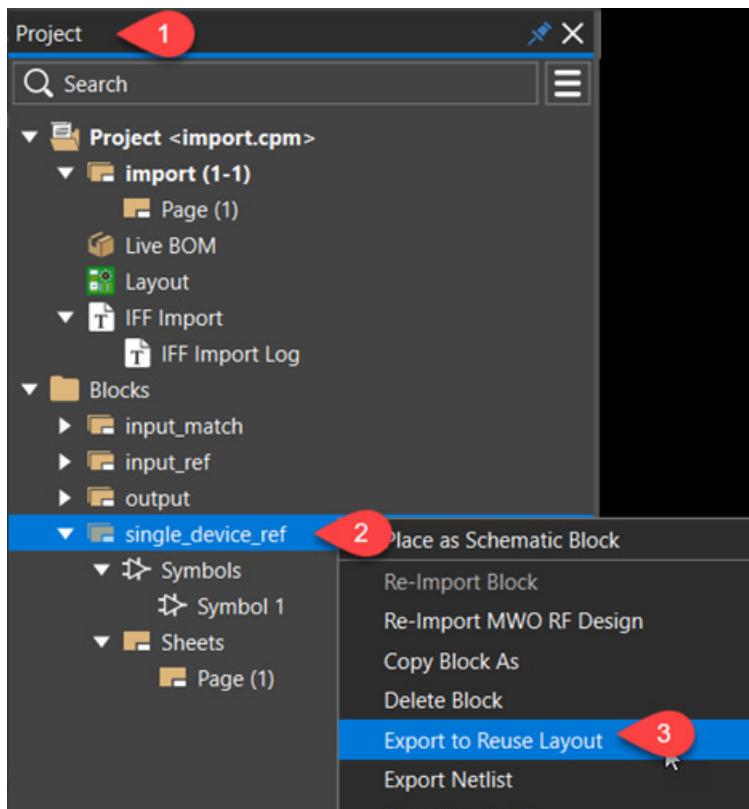
AWR Microwave Office-Allegro RF Design User Guide

Reusing Microwave Office RF Designs in Allegro Applications

can be re-imported.



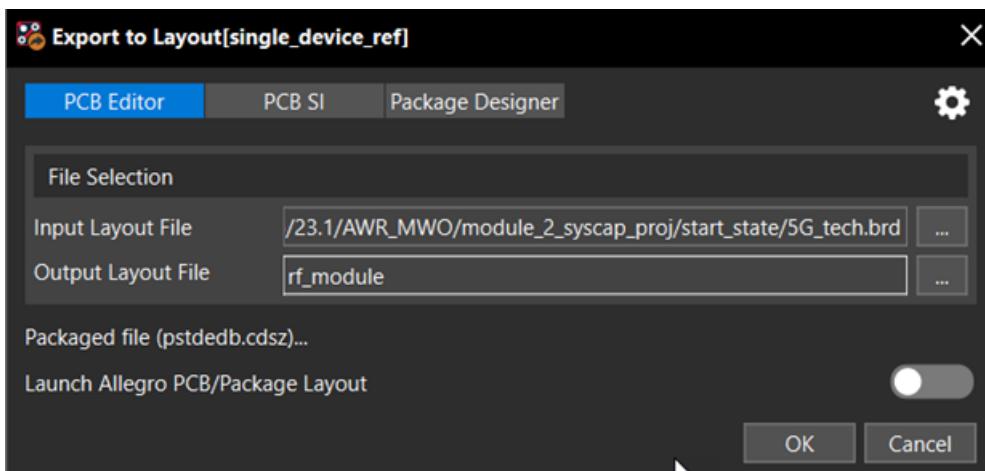
8. Select the RF block in the *Project* browser, right-click and choose *Export to Reuse Layout*.



The *Export to Layout* dialog box opens.

9. In the *PCB Editor* tab of the *Export to Layout* dialog box, do the following:

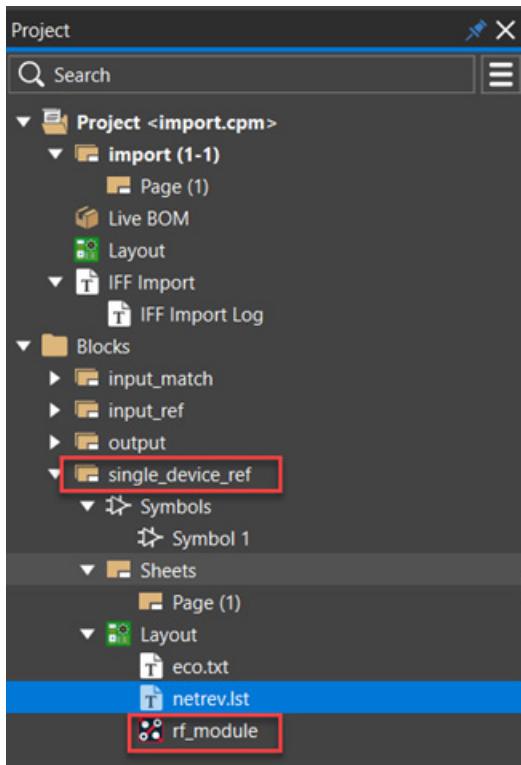
- a. Specify the path to the board design file (.brd) used for generating the unified library in the *Input Layout File* field
- b. Specify a name for *Output Layout File*.
- c. Click *OK* to start the export process.



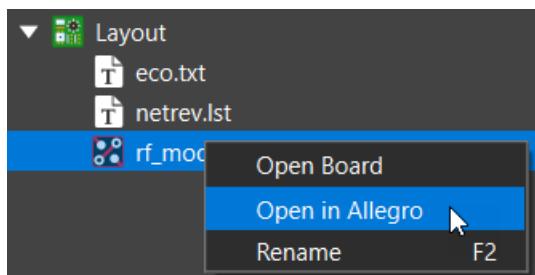
The output layout is created for the RF block and listed under it in the *Project* browser.

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10. Select the output layout file, right-click and choose *Open in Allegro*.



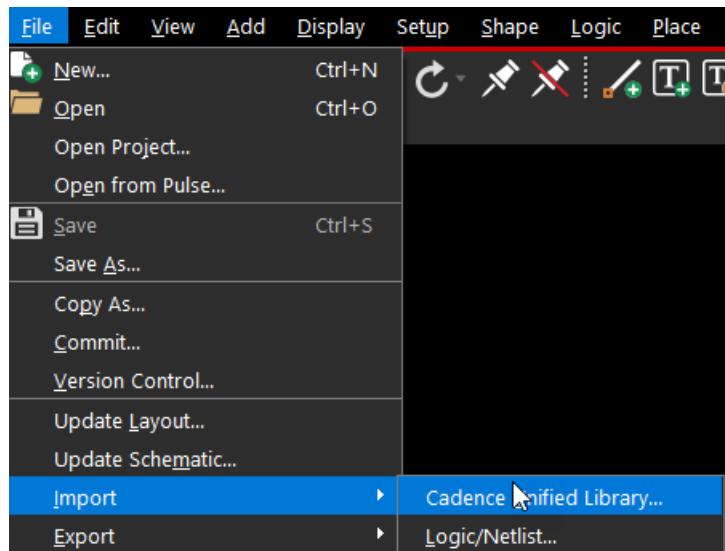
11. Select *Allegro PCB Venture* in the *Cadence 23.1 Allegro Product Choices* dialog box and click *OK*.

Allegro PCB Editor opens.

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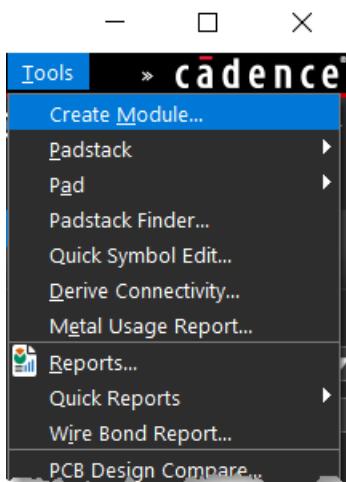
- 12.** Choose *File – Import – Cadence Unified Library*, to import Allegro Single Container.



- 13.** Browse and select the .asc file exported from Microwave Office in the file browser and click *Open*.

The RF layout of the block is placed in the design canvas when the import is completed.

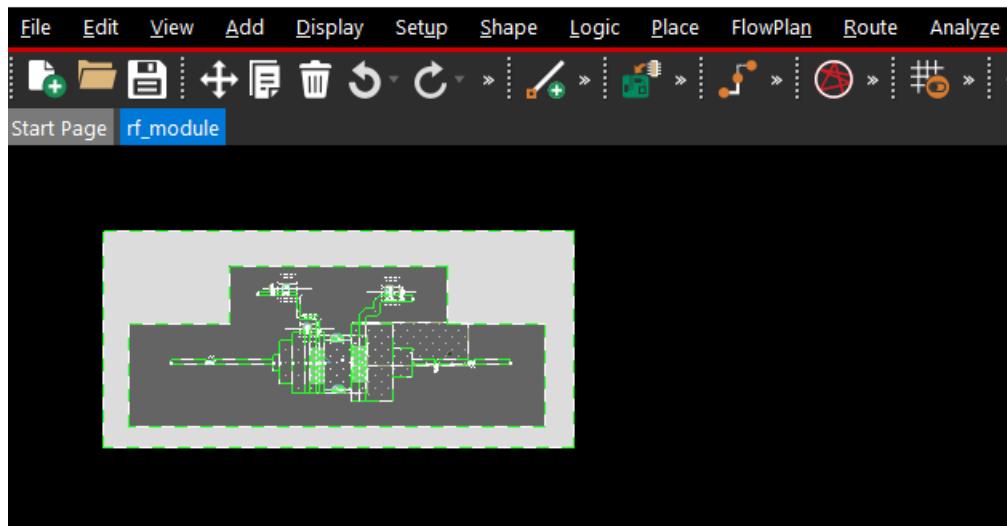
- 14.** Choose *Tools – Create Module* to create the module of the RF layout



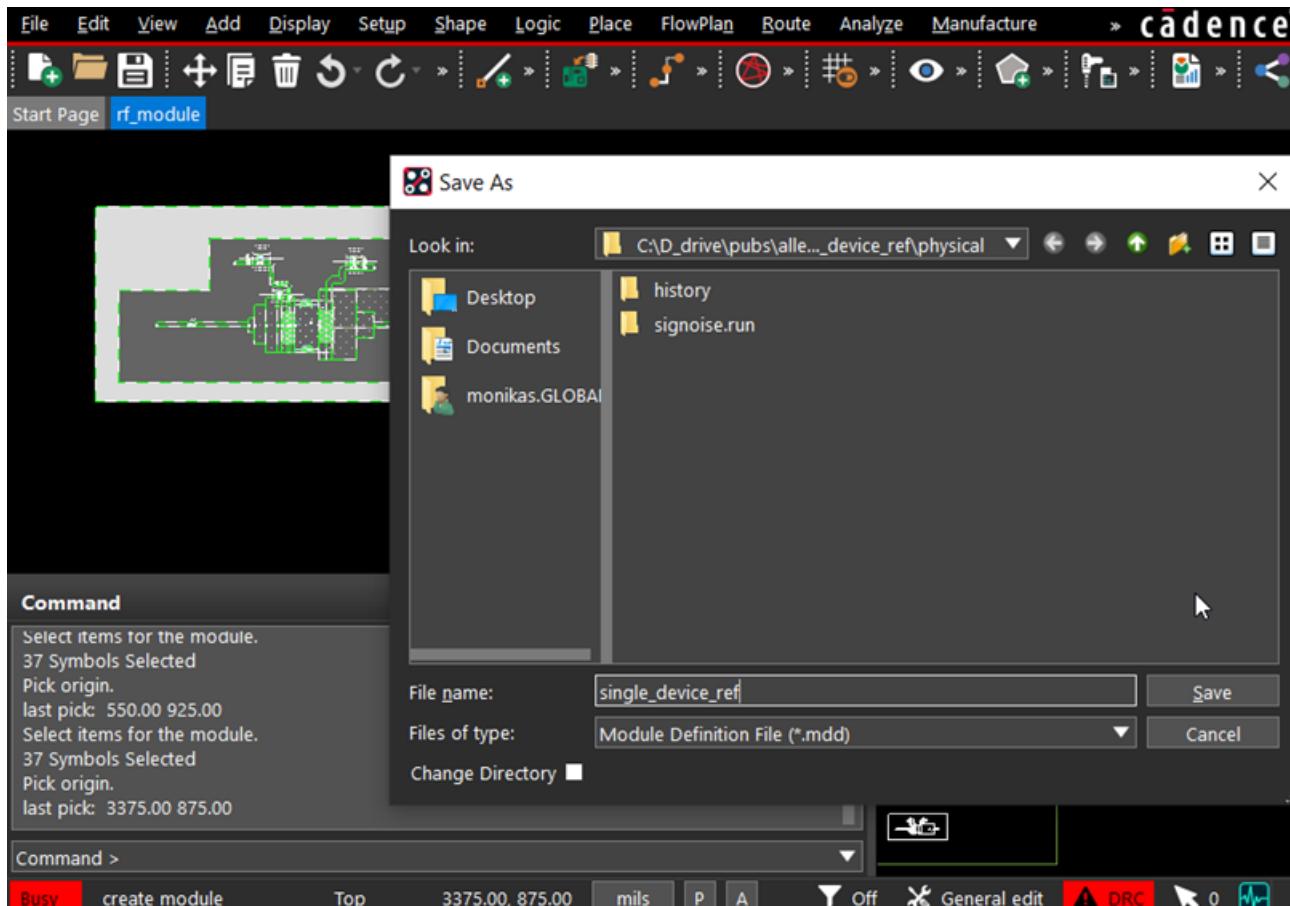
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15. Draw a rectangle around the RF layout to be included in the module and click again to pick the origin.



16. Specify the name of the RF block in the *Save As* file browser and click *Save* to save the module (.mdd) file.



The module is created and the (.mdd) is saved inside the *physical* directory of the RF block of the project.

Creating Mother PCB With Reused RF Block

To create a PCB design with reused RF block, do the following:

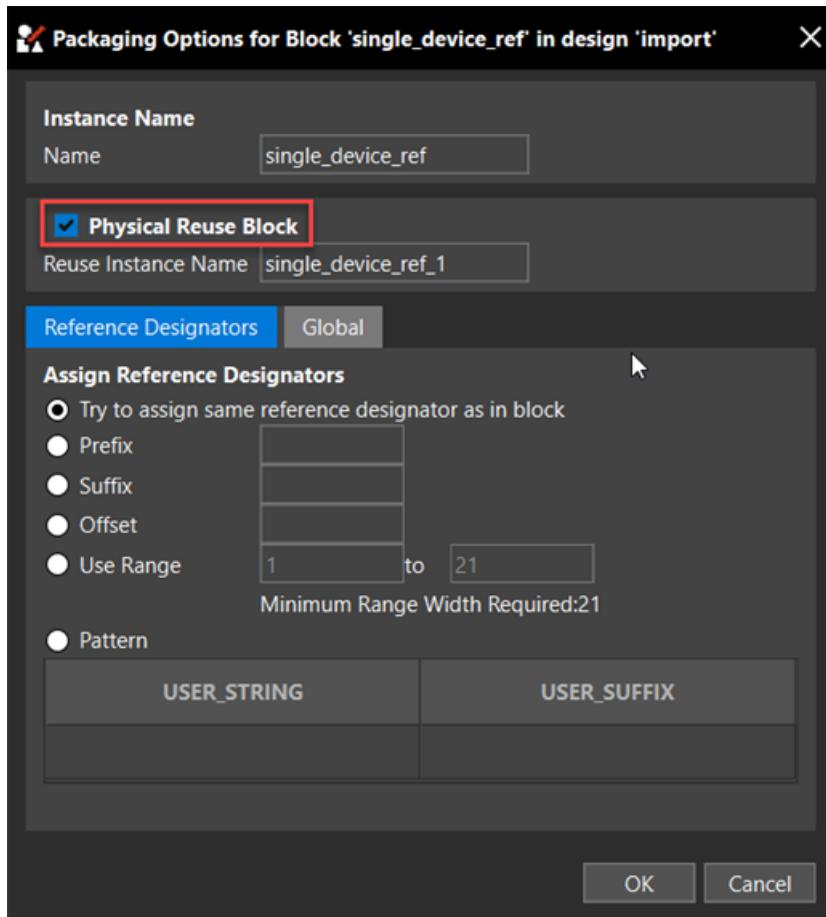
1. Copy the module file from the *physical* directory of the RF block to *physical* directory of the root block of the project.
2. Instantiate the RF block in Allegro System Capture root design, using the following steps:
 - a. Select the RF block in the *Project* browser.
 - b. Right-click and choose *Place as Schematic Block*.

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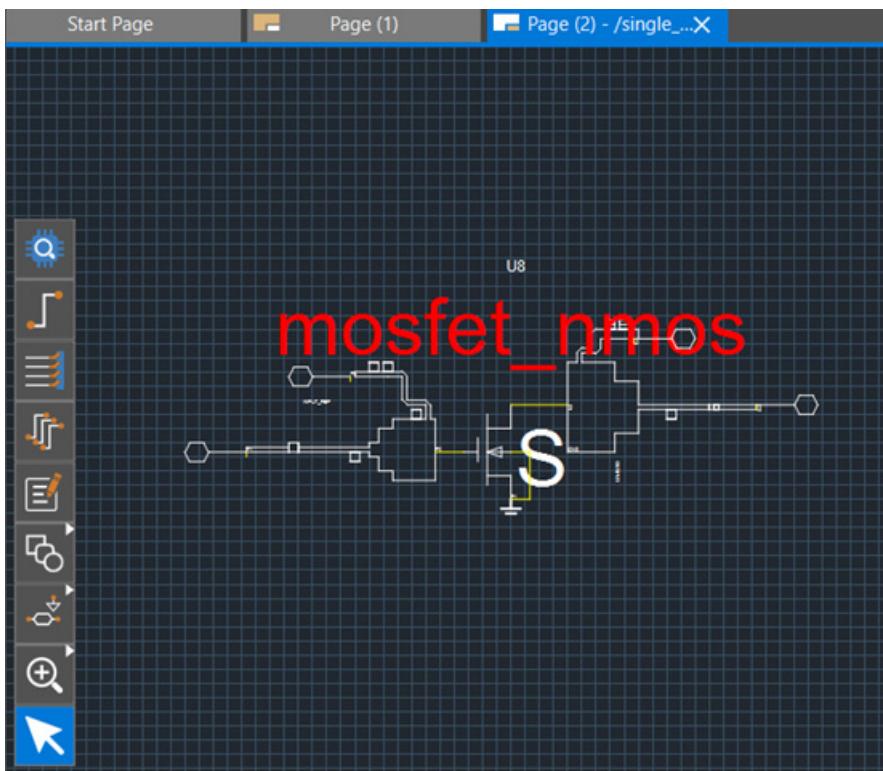
The RF block attaches to the cursor.

- c. Click to place the block in the design canvas.
- d. Select the *Physical Reuse Block* check box in the *Packaging Options for Block <block_name> in design <design_name>* dialog box that opens, and click *OK*.

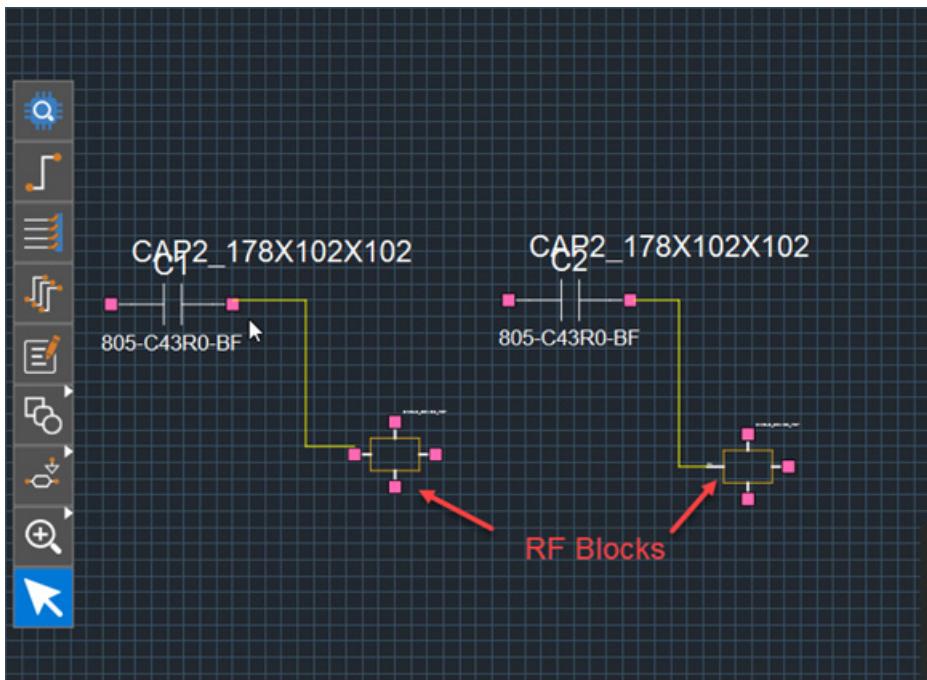


3. Repeat the above step to place more instance of the RF block in the design canvas.

4. Select an RF block instance in the canvas, right-click and choose *Descend*.



5. Make connections between RF blocks and schematic components to complete the schematic.



6. Choose *File – Export – Export to Layout* to package the schematic design.

The *Export to Layout* dialog box opens.

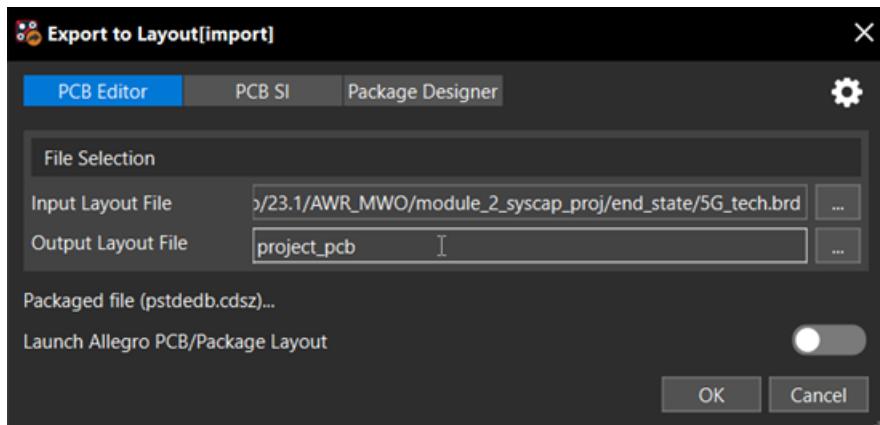
7. In the *Export to Layout* dialog box, do the following:

- Specify the path to the board design file (.brd) used for generating the unified library in the *Input Layout File* field.
- Specify a name for *Output Layout File*.

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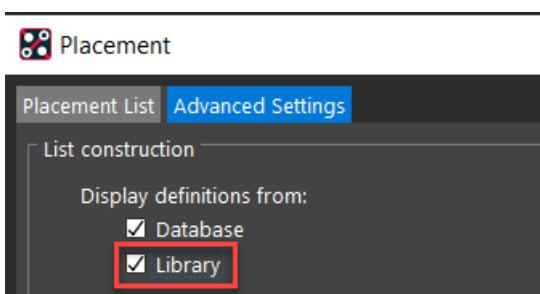
Reusing Microwave Office RF Designs in Allegro Applications

- c. Click *OK* to start the packaging process.



When completed, a new .brd file is created with connectivity information.

8. Select the board file in *Project* browser, right-click and choose *Open in Allegro*.
9. Select *Allegro PCB Venture* in the *Cadence 23.1Allegro Product Choices* dialog box.
The empty board and netlist is loaded in Allegro PCB Editor.
10. Choose *Place – Manually* to place components and RF modules.
Placement dialog box is displayed.
11. Open *Advanced Settings* tab and select the *Library* check box.

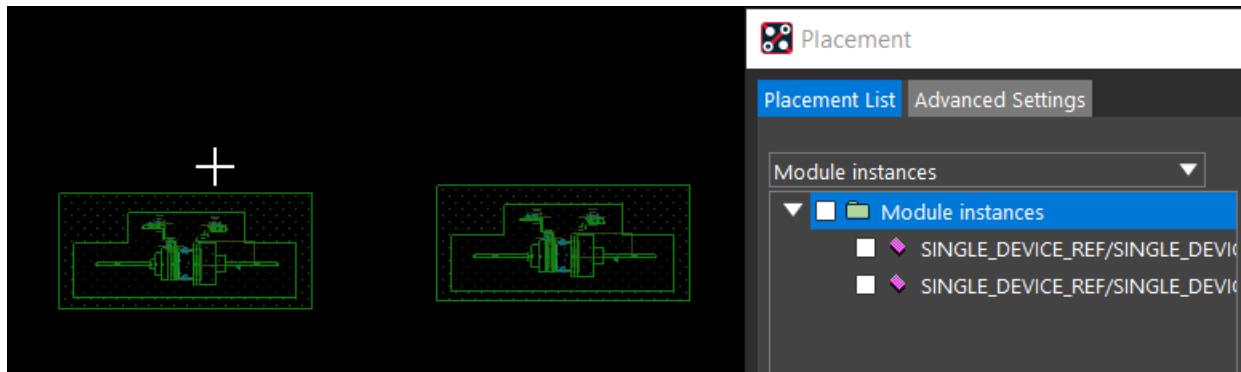


12. Open *Placement List* tab and select *Module Instances* from the pull-down list.

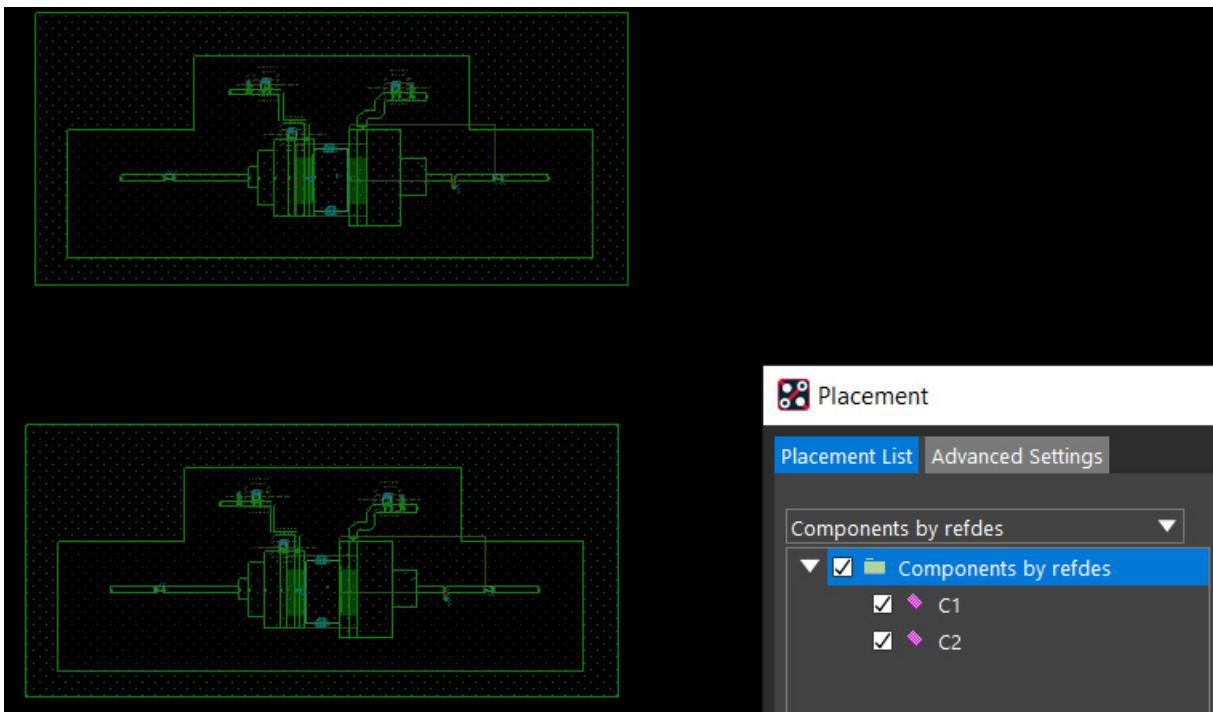
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13. Select the modules and place them in canvas.



14. Right-click and choose *Done*.
15. Reopen the *Placement* dialog box, select *Components by Refdes* from the pull-down list and start placing components by selecting their reference designators from the list.



The connectivity when placing components is displayed by ratsnest lines.

16. Right-click and choose *Done* to close the *Placement* dialog box.
17. Complete the layout design.

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A

Dialog Box References

Cadence Unified Library Translator

The *Cadence Unified Library Translator* dialog box is used to convert Allegro PCB design libraries into a format that is read by all the tools in the flow.

Access Using

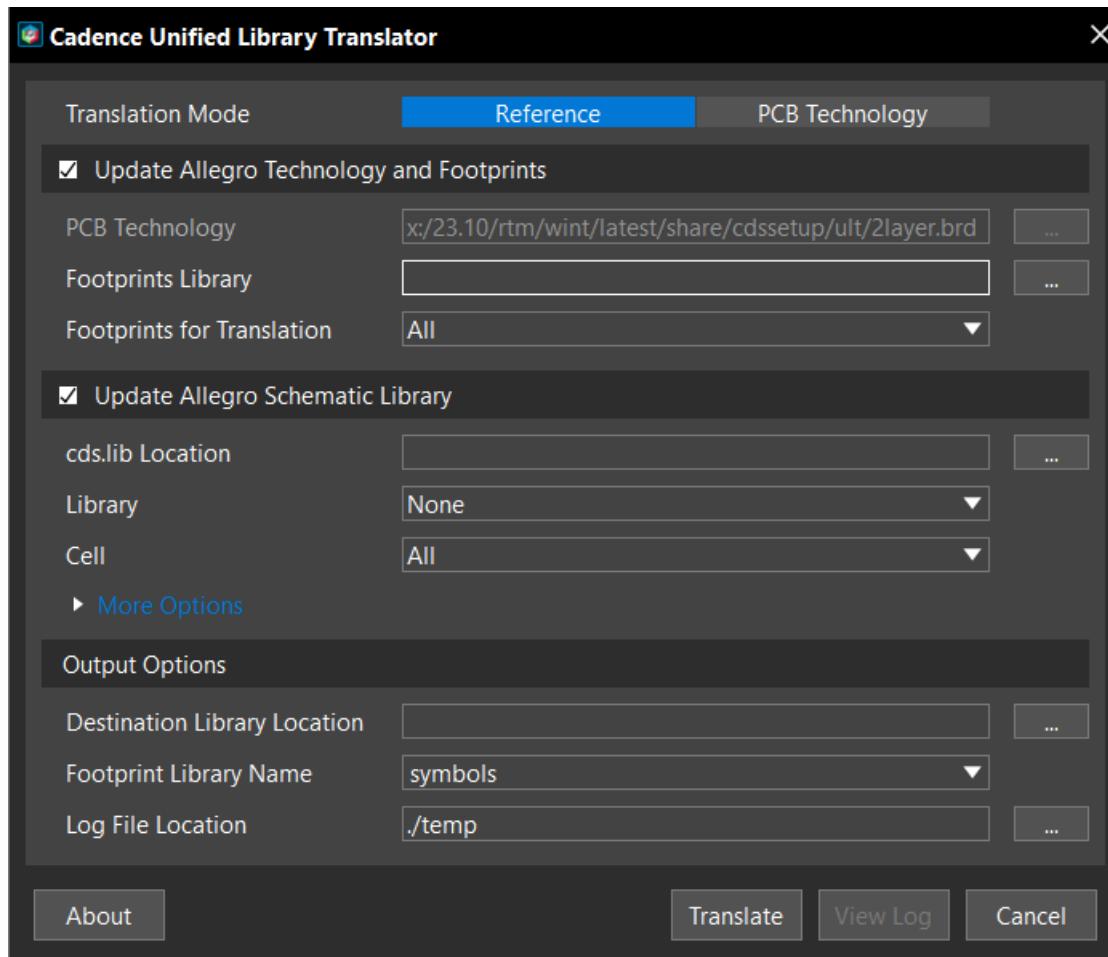
1. Navigate to the following path of your installation directory:

<install_directory>\tools\bin

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Dialog Box References

2. Double-click `ult.exe` to open *Cadence Unified Library Translator*.



Field	Description	
<i>Translation Mode</i>	<i>Reference</i>	Specifies the mode for translating Allegro schematic and footprint libraries.
	<i>PCB Technology</i>	Use this mode to translate design-specific technology file containing layer stackup and via information.
<i>Update Allegro Technology and Footprints</i>		Specifies options for footprint libraries and technology file translation.

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Dialog Box References

<i>PCB Technology</i>	Specifies the path of PCB technology file (.brd, or .tcfx, or .tcf) containing layer stackup and via information.
	Note: In the <i>Reference library</i> translation mode, this option is disabled and uses a default two-layer board design file, shipped with the installation located at <insat11_directory>\share\cdssetup\ult
<i>Footprints Library</i>	Choose the footprint library name from the pull-down list.
<i>Footprints for Translation</i>	Choose the footprint symbol name from the pull-down list. By default, <i>All</i> is selected.
<i>Update Allegro Schematic Library</i>	Specifies options for translating schematic symbols libraries.
<i>cds.lib Location</i>	Specifies the path of the cds.lib file that defines the path of schematic symbol libraries.
<i>Library</i>	Choose the schematic library name from the list. By default, <i>None</i> is selected.
<i>Cell</i>	Choose the schematic symbol cell name from the list. By default, <i>All</i> is selected.
<i>More Options</i>	Specifies additional options for PTFs translation.
	<i>Injected Properties</i> Enable to include injected properties specified in the PTFs for translation.
	<i>Library-level Part Table Files</i> Enable to include PTFs found in the logical symbols library for translation.
	<i>Merge Part Tables</i> Enable to merge all the PTFs that are found for translation.
	<i>Part Table Files</i> Specified the path for the PTFs used for translation.
<i>Common Options</i>	
<i>Destination Library Location</i>	Specified the path of the destination directory for the translated libraries.
<i>Footprint Library Name</i>	Specifies the name of the translated footprint library. By default, the name is <i>symbols</i> .
<i>Log File Location</i>	Specifies the path of a directory for creating log files.

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Dialog Box References

<i>About</i>	Click to display the name and version.
<i>Translate</i>	Click to start the translation process.
<i>View Log</i>	Click to view the translation details saved in the log files.
<i>Cancel</i>	Click to cancel the translation process.

Command Line Reference

con2ul_cmd

This batch command is used for translating an Allegro library into the Cadence Unified Library format.

Syntax

```
con2ul_cmd -l -p -t -i -f
```

General Arguments	Description
-h [--help]	Displays help message and exit.
-v [--version]	Displays version and exit.
Required	
-l [--lib]	Specifies name of the library for translation.
Optional Arguments	
-c [--cell]	Specifies a list of cells for translation.
-t [--tempdir]	Specifies the path of the temp directory to create log files.
-p [--ppt]	Specifies the path of the PTF or the directory containing the files.
-f [--footprintlib]	Specifies a logical name of the footprint library.
-r [--proj]	Specifies the path to the project (.cpm) file.
-m [--mergePptOff]	Specify whether the PTFs are be merged.
-u [--useLibPptOff]	Specify whether library-level PTFs are to be used for translation.

-i [--writeinjectedProp]	Specify to write injected properties to CDF.
-o [--destlib]	Specify output directory location to be translated

Example

```
con2ul_cmd -l 5g_library -p C:\project\5g_library\part_table.ptf -t temp -i -f symbols
```

Running con2ul_cmd Batch Command

To run the batch command for translating an Allegro schematic symbol library into the Cadence Unified Library format, do the following:

1. Open the Windows command prompt.
2. Change the directory to the location of the library.
3. Type the `con2ul_cmd` batch command with the required arguments and press the Enter key.

The batch command creates Cadence Unified Library views for the library cells specified in the batch command.

For more information see, [Verifying Translated Libraries](#).

algro2ul

This batch command is used for translating Allegro footprint library and PCB technology file into the Cadence Unified Library format.

Syntax

- For technology file conversion:

```
algro2ul -techfile -destination-library directory -destination-library
```

- For Allegro footprint library conversion:

```
algro2ul -source-directory -destination-library-directory -destination-library
```

-techfile	Specifies the complete path of board design file (.brd).
-destination-library-directory	Specifies the path of the destination directory.
-destination-library	Specifies the name of the directory containing the translated footprint library and the extracted technology file.
-source-directory	Specifies the path of the input footprint library directory containing symbol files (.dra, .psm, .pad, .psm).

Examples

- Translating technology file and via information:

```
algro2ul -techfile C:\project\5g_library\5g_tech.brd -destination-library-
directory C:\project\translated_lib -destination-library symbols
```

- Translating footprint library:

```
algro2ul --source-directory C:\project\5g_library\dra_files -destination-library-
directory C:\project\translated_lib -destination-library symbols
```

Running algro2ul Batch Command

To run the batch command for translating Allegro footprint libraries and technology file into the Cadence Unified Library format, do the following:

1. Open the Windows command prompt.
2. Change the directory to the location of the library.
3. Type the algro2ul batch command with the required arguments and press the Enter key.

The batch command creates Cadence Unified Library views for footprint libraries.

For more information see, [Verifying Translated Libraries](#).

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Command Line Reference

Troubleshooting

Why do I get the following error when importing an Microwave Office design in Allegro PCB Editor?

ERROR(SPMHIP-166) : Cannot place instance 'L1' (sch1/ind_0/layout) (Tech:symbols) with reference designator 'U1' because origin (X:-12635.25 Y:-11716.32) is outside design extents (MinX:-10000.00,MinY:-10000.00,MaxX:40000.00,MaxY:40000.00)

This error is flagged when you import an Microwave Office design in Allegro PCB Editor and the board design extent is not enough to place an imported symbol. The import process cannot automatically update the design extent and flags this error. To resolve this issue, manually increase the design extent according to the values specified in the error message and rerun the import process.

Why do MLine and Cap pads on one end not connected after importing Microwave Office OA in Allegro PCB Editor?

The connectivity model differs in Microwave Office and Allegro PCB Editor. In AWR, the connection point (faces) is on the border of the pin pad whereas in Allegro PCB Editor it is at the center of the pin pad. As a result, when a shape touches with outer border of a pin pad, it is considered connected in Microwave Office. As the connection is not made to the center of the pin pad, the two objects are not connected and rats are displayed.

For odd-size pads, the connectivity seems to be broken in Allegro PCB Editor. To resolve this issue, either change the pad size in Allegro PCB Editor or move the MLine to the middle of the pad in Microwave Office.

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Troubleshooting

D

Limitations of Cadence Unified Library Flow

The following limitations are applicable to the current versions of Allegro PCB design applications and Microwave Office:

Cadence Unified Library Export from Microwave Office

For successful export of Cadence Unified Library from Microwave Office, consider the following points:

- The s-parameters from extracted EM docs are not available with the design.
- AWR System Drawing Layers are not transferred to Allegro PCB design.
- Spaces are not supported in paths to the location where Microwave Office read and write Cadence unified libraries.
- Capital letters are not supported in paths to the location where Microwave Office read or write Cadence unified libraries.
- Special character, colon (:) is not supported in model names.
- Unsupported elements:
 - PORT_NAME
 - NCONN
 - Non-manufacturable parts (for example, bias supplies, ideal lumped elements, and so on) other than PORTx and GND element.
 - Elements with implicit ground nodes (for example, VIA1P)
- 3D shapes (for example, housings or SMA connectors) are not supported.

Limitations of Cadence Unified Library Import in Allegro PCB Design Applications

- RF design created in Microwave Office is considered read only in the Allegro PCB Design applications.
- Any changes in the connectivity or parts should be made in Microwave Office only.

Limitations of Cadence Unified Library

- Flow:
 - Technology or library component changes must be done in Allegro PCB Design applications.
 - Unit changes are not supported within Microwave Office.
- Unsupported Topology:
 - Sizable parts
 - Split parts/Asymmetrical parts
 - Parts with NC_PINS
 - Vectored parts