

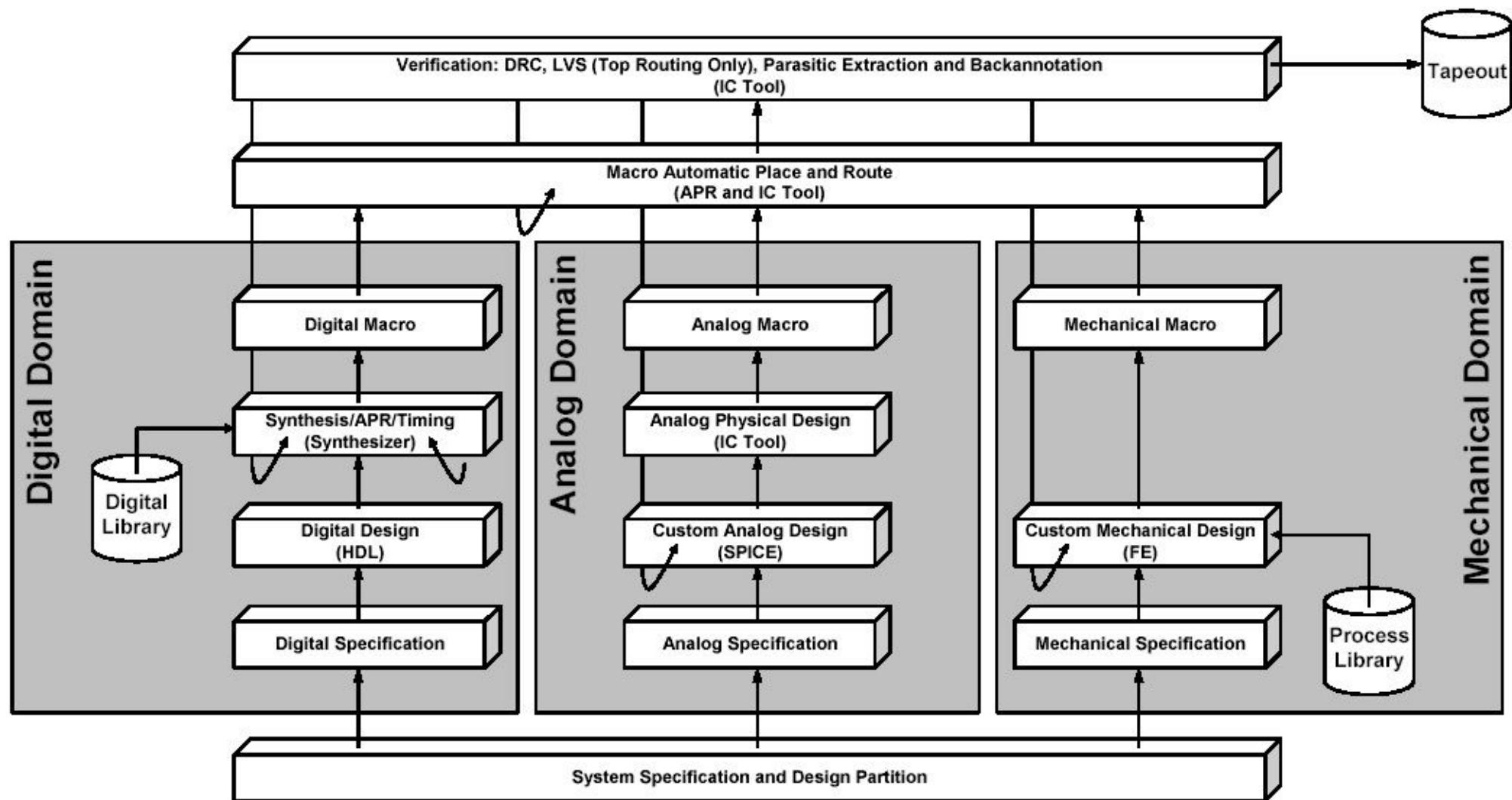
# **Automated Macromodelling Techniques for Design of Complex Analog and Mixed-Signal Integrated Systems**

# Outline

- Model-order reduction (MOR): on-chip interconnect
  - Direct and Krylov-based methods
- Advanced MOR: nonlinear circuits
  - I/O drivers
  - Pwr/ground noise
- Oscillators/PLLs
  - basics; phase macromodels
  - jitter, phase noise spectrum
  - jitter due to supply noise

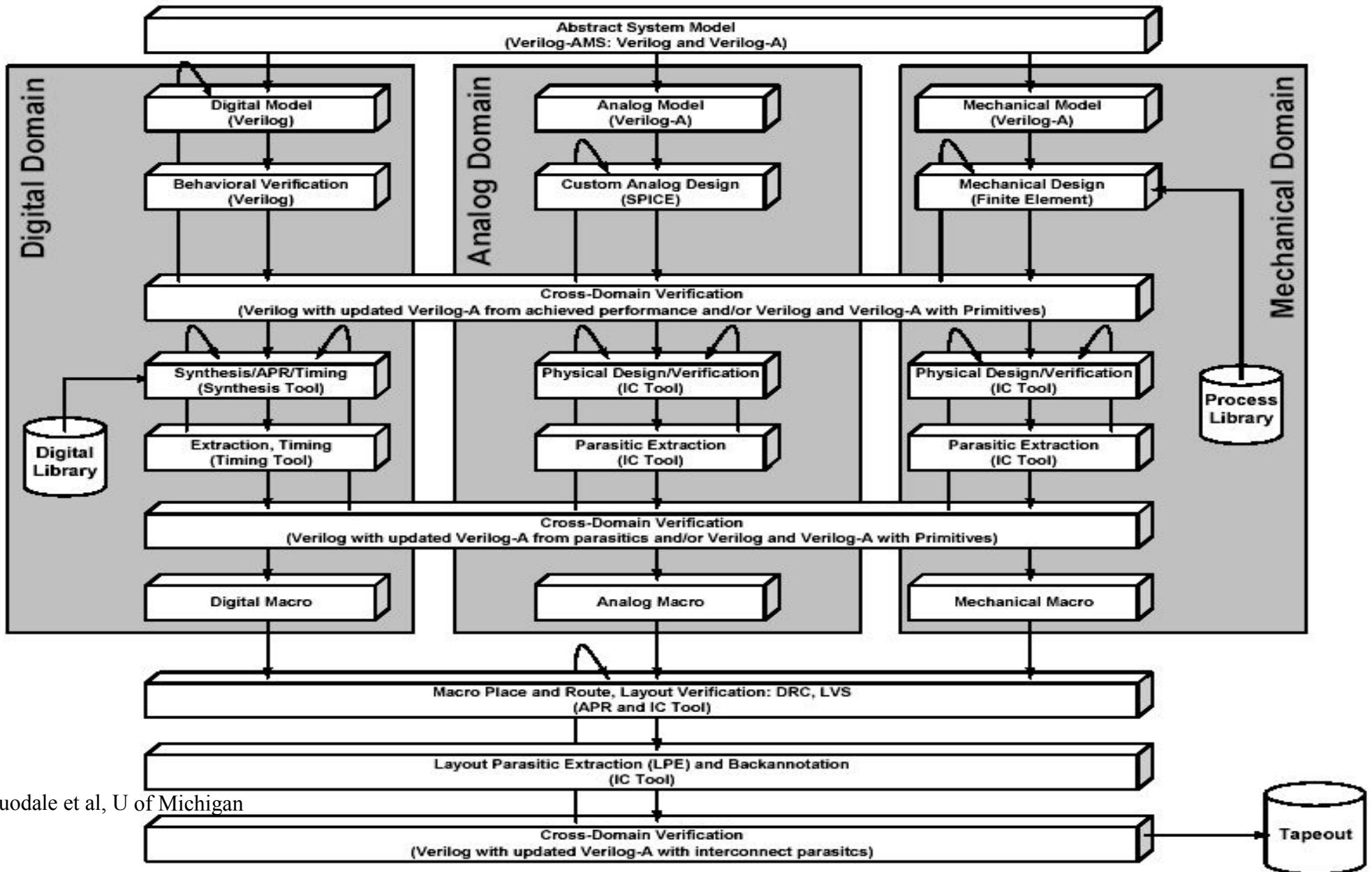
# Typical Design Process Today

McCorquodale et al, U of Michigan



- High-speed signalling (interconnect/analog/RF) related failure: common (3-5 spins is cutting edge!)

# What We'd Like Instead



McCorquodale et al, U of Michigan

# Accurate Yet Practical Interconnect, I/O, analog System-Level Verification

- One way: use “fast” simulators
  - large interconnect networks: SPICE completely impractical
  - HSIM/NanoSim: takes you some of the way
  - eg, full PLL takes a couple of days (much better than plain SPICE)
  - but need something *much faster* during design
- Solution: use reduced-order models
  - But: how to generate a good macromodel from a SPICE-level circuit block?

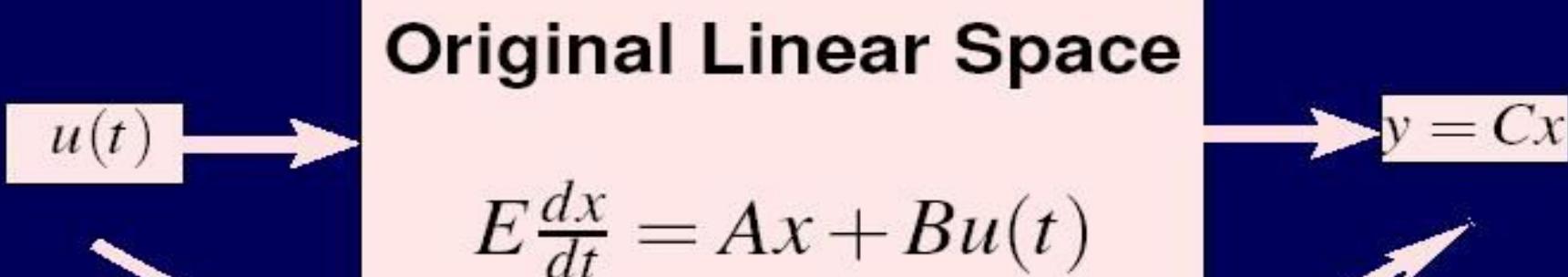
# **Model-order Reduction for fast simulation of Interconnect**

# Interconnect fall in the General Class of Linear Time Invariant Systems

- What is LTI?
  - Scale input waveform => scale output waveform
  - Time-shift input => time-shift output
- Interconnect, “linear” circuit elements
- Well understood: 50 years of theory
  - Laplace transforms, LTI ODEs, controllability/observability, ...
- Powers hand analysis by most designers

# LTI Reduced-Order Modelling

Credits: Ning Dong, UMN

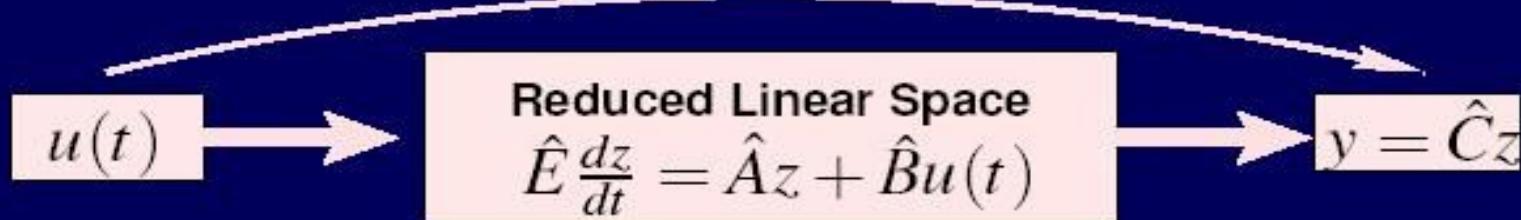


$$H(s) = C(sE - A)^{-1}B$$

$\downarrow$

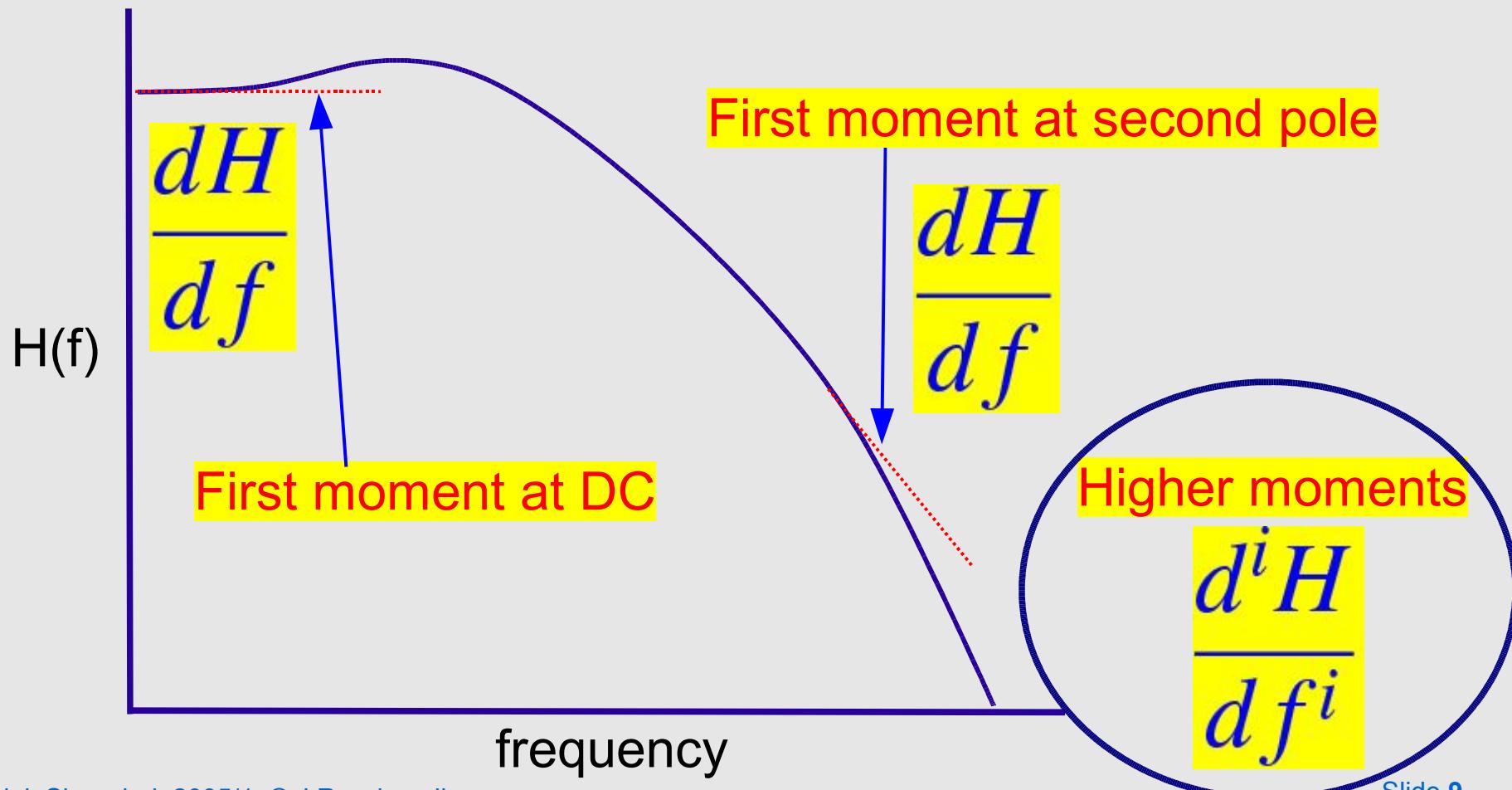
$$x = Vz, x \in \mathbf{R}^n, z \in \mathbf{R}^q$$

$$\hat{H}(s) = \hat{C}(s\hat{E} - \hat{A})^{-1}\hat{B}$$



# Model Order Reduction: the Concept of *Moments*

- Can't match the entire transfer function exactly
- so... **match useful metrics: moments**



# Moments and Model-Order Reduction

- Why focus on moments?
  - good measures of time-domain delay, skew, etc
- The idea behind MOR: **find small system that matches only a few moments**
  - (eg, matching 5 moments => reduced size = 5)
  - original circuit: typically very large (eg,  $10^6$ )
- Reduced transfer function is very good approximation to original
  - for what's important: delay, rise-time, etc
  - (even though MM size is much smaller)

# Synthesizing the Reduced-Order Model

- Different computational methods
  - “explicit” moment matching: AWE
  - “Krylov subspace methods” (implicit moment matching): PVL, PRIMA
  - “Truncated Balanced Realizations” (TBR) methods
- All achieve the same goal:
  - small macromodel of size  $q$
  - matches (about)  $q$  moments
- Other LTI issues: passivity, stability

# Asymptotic Waveform Evaluation

- AWE (Pillage/Rohrer ~1990)
- Preserve moments of LTI transfer function
  - frequency-domain xfer-fn derivatives
- Explicit moment matching
  - calculate moments of original system
  - run a Pade approximation: small rational function
  - map to small dynamical system macromodel

# LTI MM Accuracy/Stability

- Increasing size does not increase accuracy
  - explicit moment generation, Toeplitz-matrix based calculation numerically ill-conditioned
- Implicit moment matching: Krylov subspace methods
  - don't calculate moments: generate related Krylov subspaces robustly (Lanczos/Arnoldi methods)
  - generate macromodels directly - **moments matched implicitly**
- Pade-via-Lanczos (PVL)
  - Feldmann/Freund 1994/5

# LTI MM Stability/Passivity

- Interconnect basically R, L, C elements
  - Passive: can't generate energy
- But macromodels can!
  - small inaccuracies in MM parameters => qualitative stability problems => useless MM
  - passivity must be preserved
- Passivity for RC/RLC circuits
  - congruence transformations (Kerns/Yang 95)
  - PRIMA (Odabasioglu/Celik/Pileggi 97)
  - Others: PVL extensions, beyond RLC...

# LTI MM Optimality/Compactness

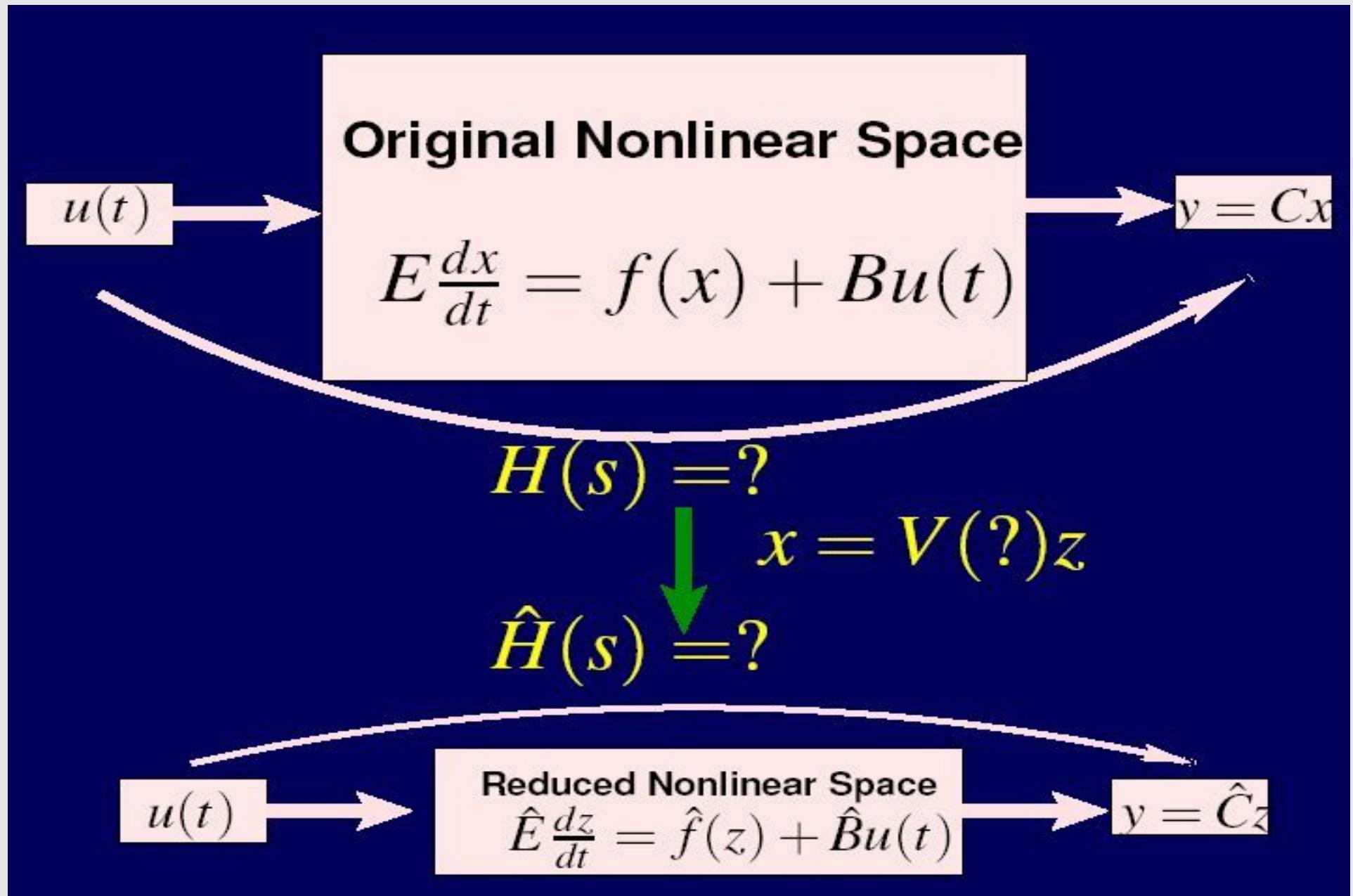
- Truncated Balanced Realizations (TBR)
  - Silveira/White et al
  - Trim internal states that are not controllable/observable
  - provably optimal: minimizes I/O norm error for given MM size
- But: TBR is computationally expensive
  - cubic in original size
- Mix and match: Krylov + TBR
  - Phillips et al 2002: first Krylov, then TBR
  - advantages of both

# LTI MM Summary

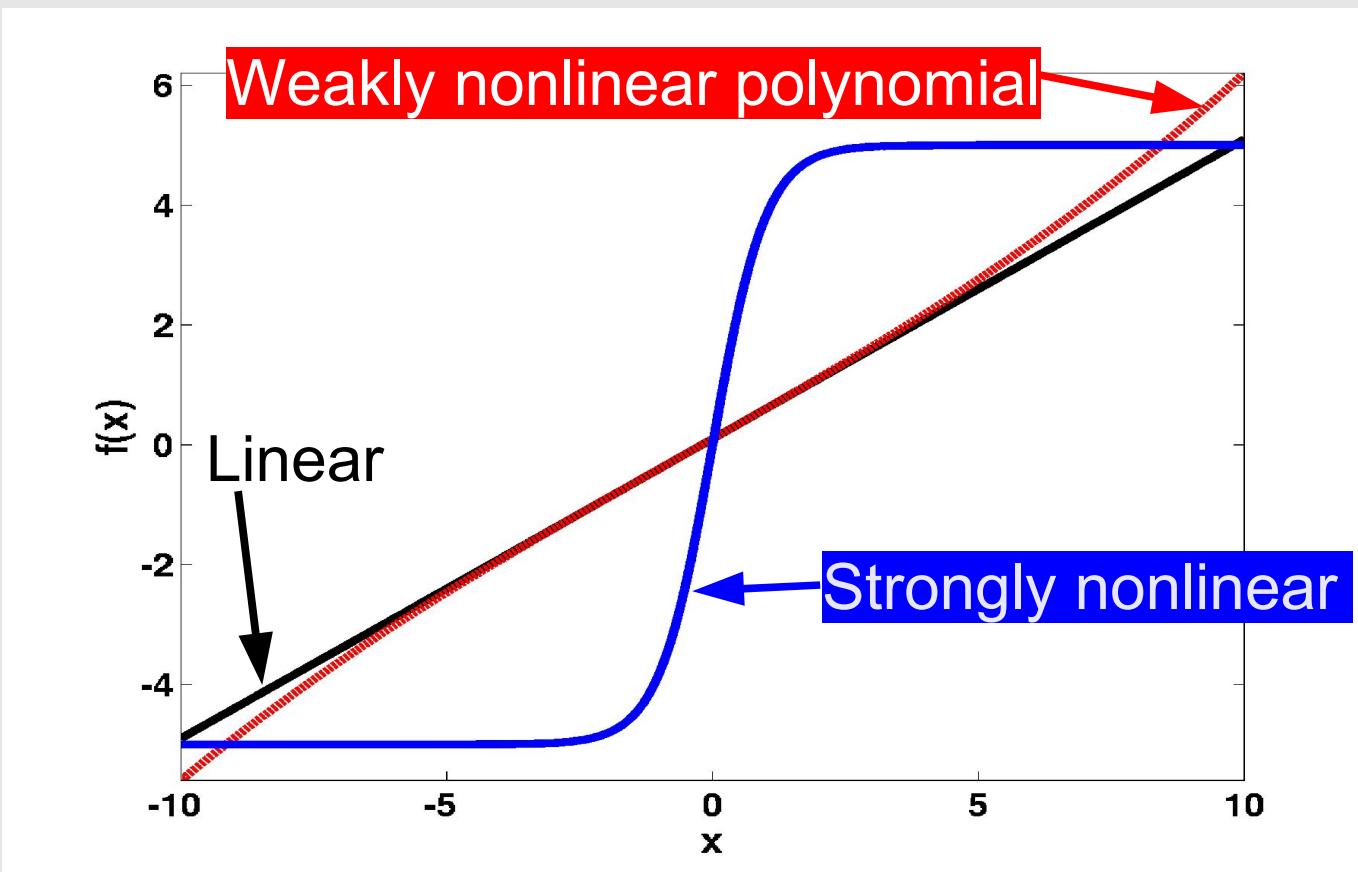
- Important features
  - Accuracy vs size tradeoff
  - MM scalability
  - MM passivity
- Computational properties
  - AWE, Krylov methods linear with system size
  - TBR methods cubic (but new results from Joel!)
- Relatively mature and practically usable
- Basis for nonlinear approaches

# **Modelling/Simulation of I/O Buffers**

# Nonlinear Macromodel Generation



# Strongly Nonlinear Systems

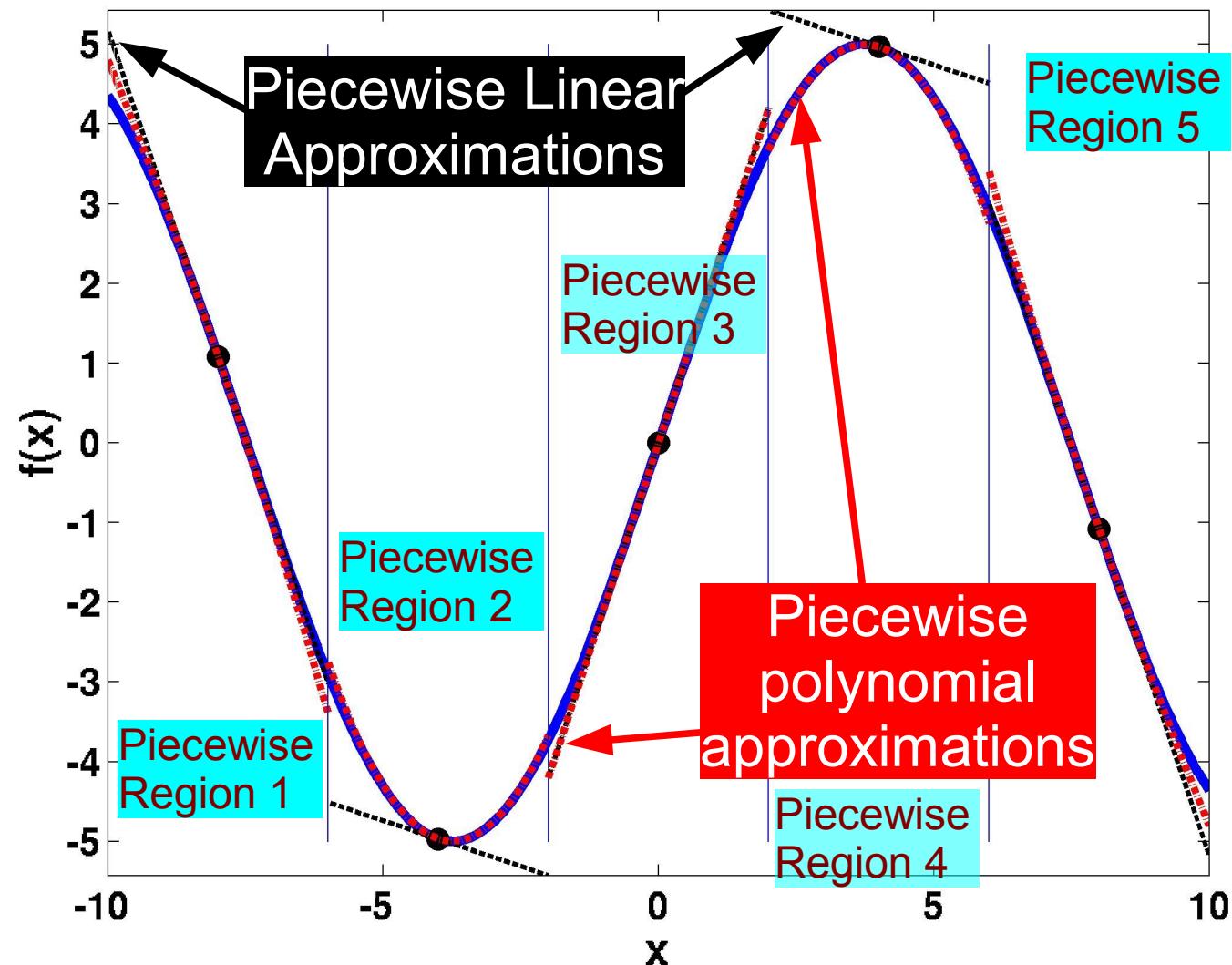


- Clipping, saturation, digital, slewing effects in circuits
- Global polynomials poor for strong nonlinearities

# Dealing with Strong Nonlinearities

- Use piecewise approximations

Piecewise: Good global fidelity for strong nonlinearities

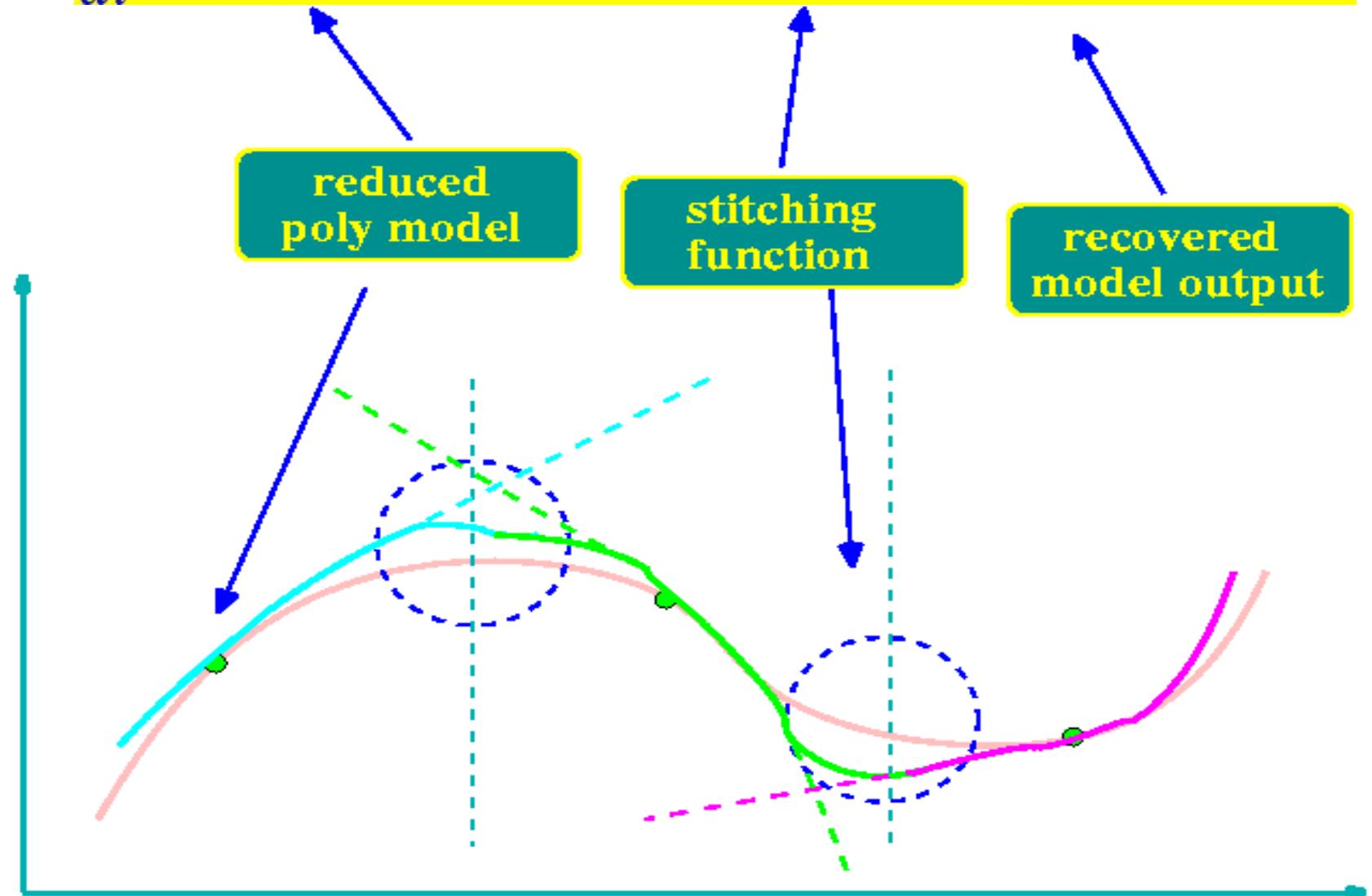


# Piecewise Reduced-Order Modelling

- Reduce each piecewise linear region
  - using LTI MOR techniques
  - (or use polynomial MOR reduction)
- Stitch together the separate reduced-order models
  - using scalar weight function [Rewienski/White 99-04]

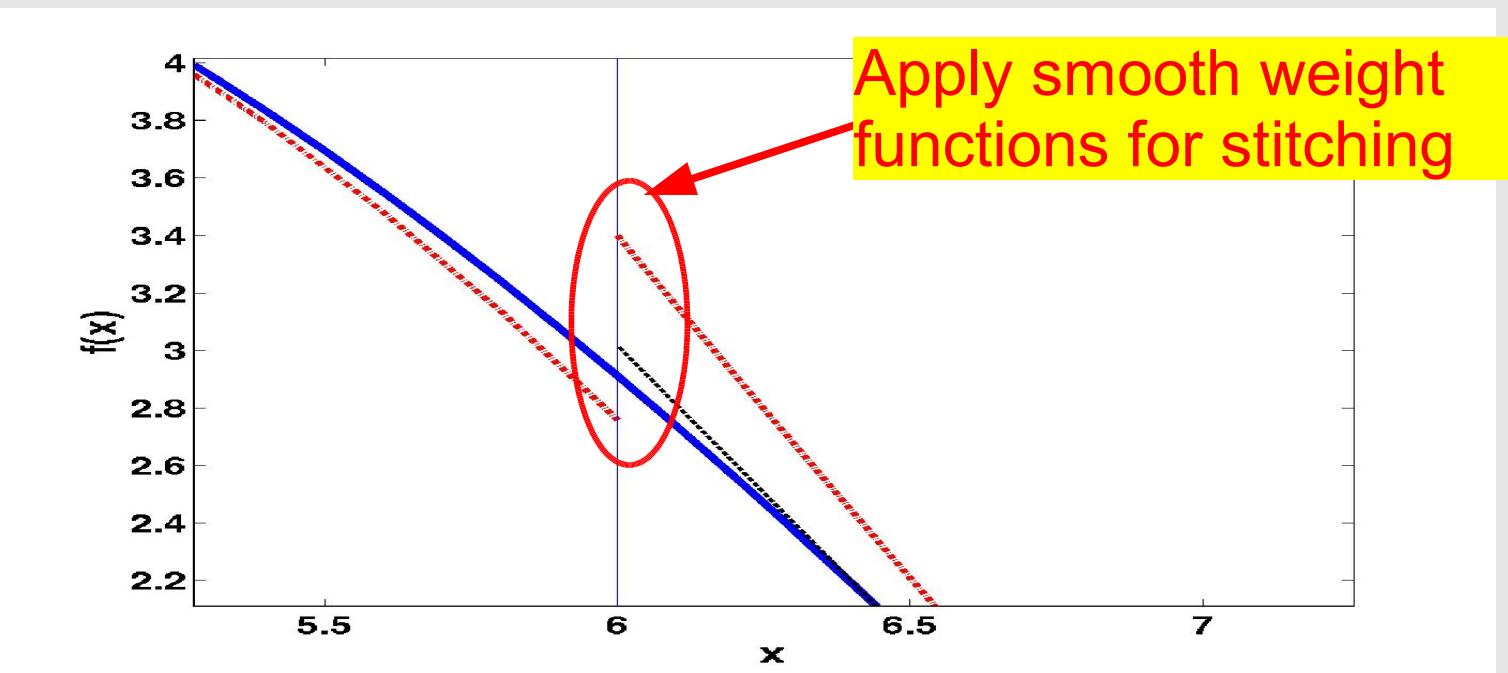
# Stitching Together Piecewise Models

$$\frac{dz}{dt} = \sum \underbrace{(\hat{A}_i z + \hat{b} u(t))}_{\text{reduced poly model}} \cdot \underbrace{w_i(z)}_{\text{stitching function}}, \quad y = \sum (\hat{c}_i z) w_i(z)$$



# Macromodelling Strongly Nonlinear Systems

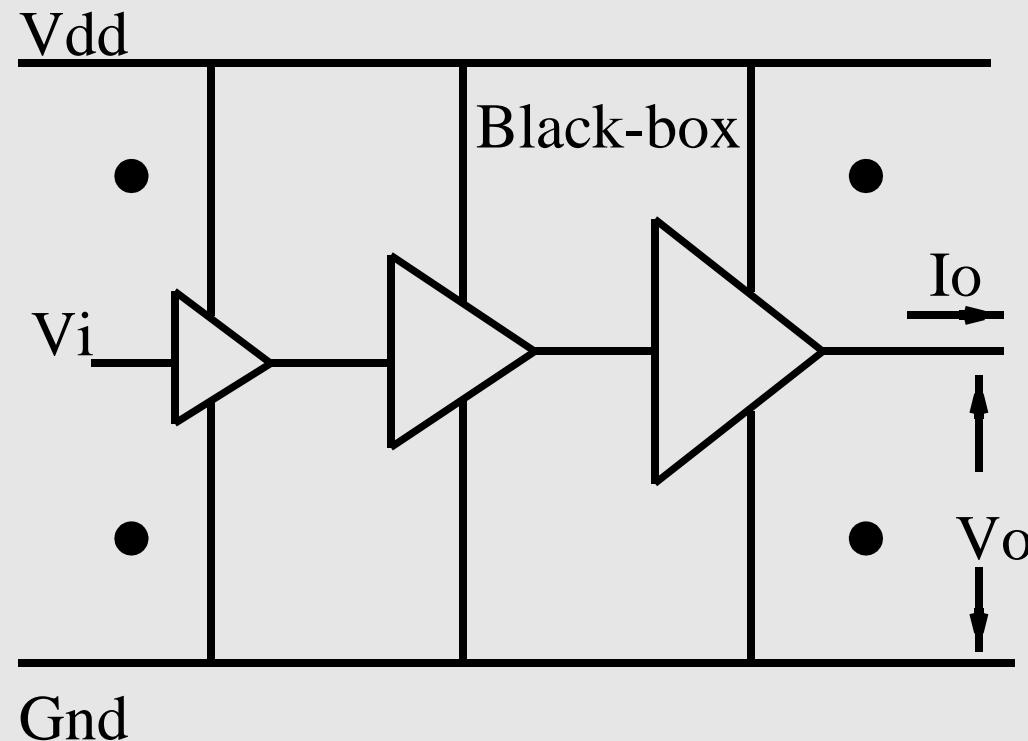
- New issue: stitching together macromodels of different piecewise regions can yield problems



# Goal: Drop-in Replacement Macromodels

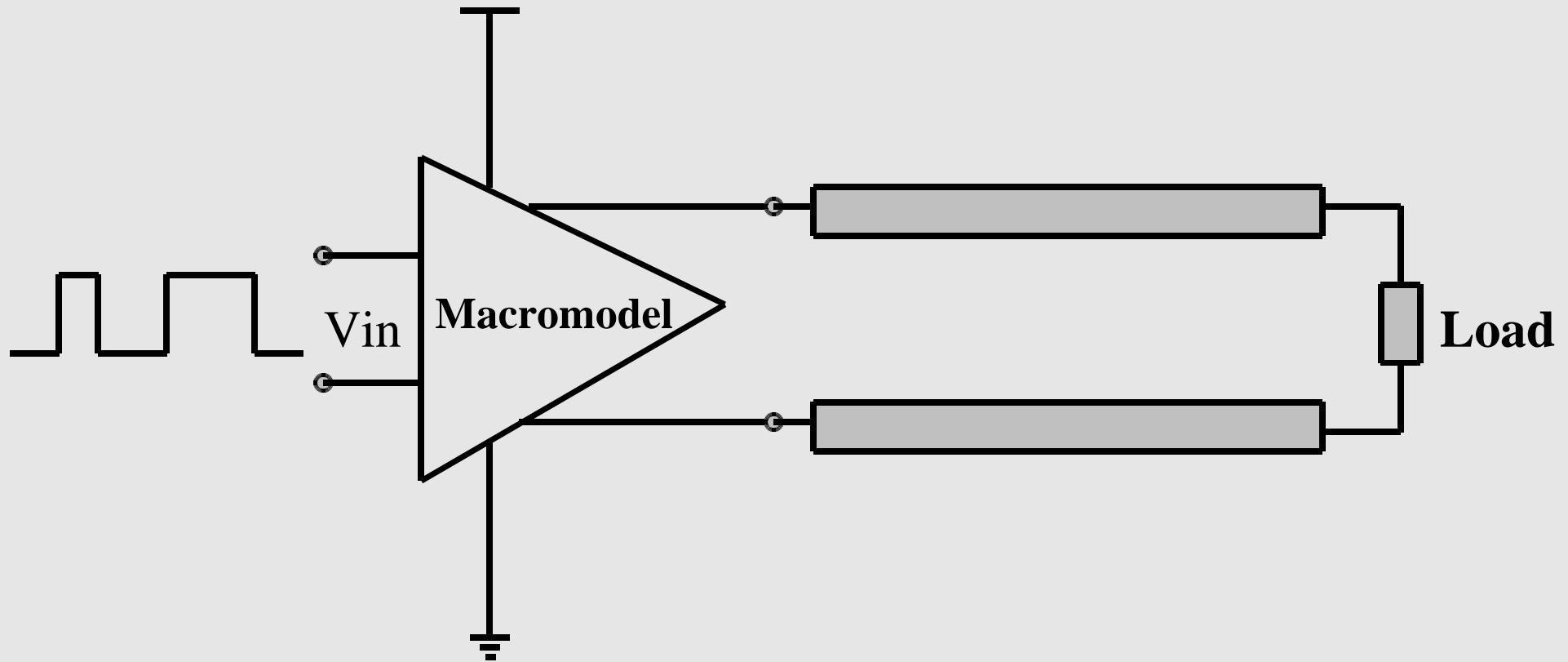
- Design process typically runs many simulations
  - DC (sweep), AC, small-signal distortion, transient
  - time- and frequency-domain analyses (harmonic balance, shooting, etc)
- Would like a **SINGLE extracted macromodel** to work for **ALL** analyses
  - don't want different “macromodels” for each analysis!

# Extracting Macromodels of I/O Buffers



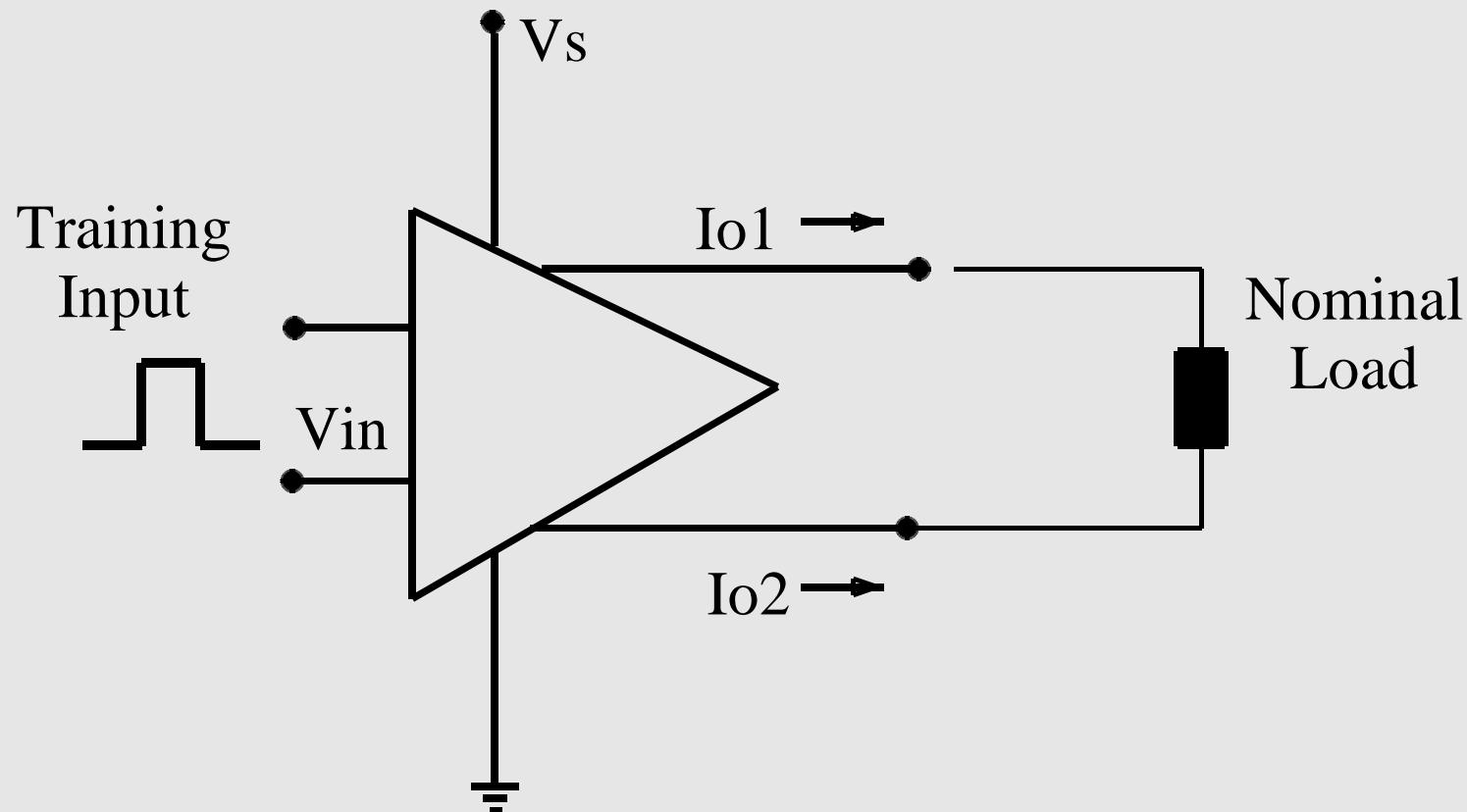
- High-speed, on or off-chip interconnect drivers
  - co-simulate with reduced interconnect
  - single macromodel to capture:
    - loading effects, power/gnd glitches, signal glitches

# Typical Loading of I/O Drivers



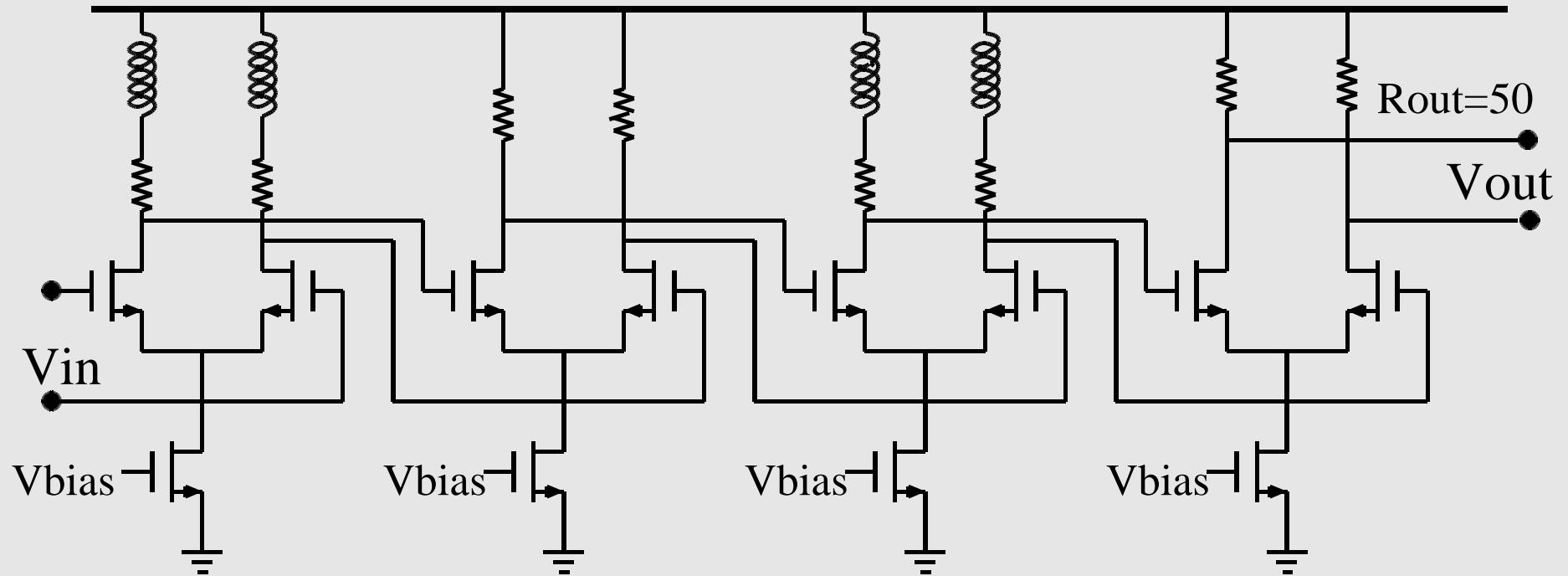
- Off-chip: transmission line connects to resistive/capacitive load
- On-chip: direct connection to RC interconnect network

# Setup for Macromodel Generation



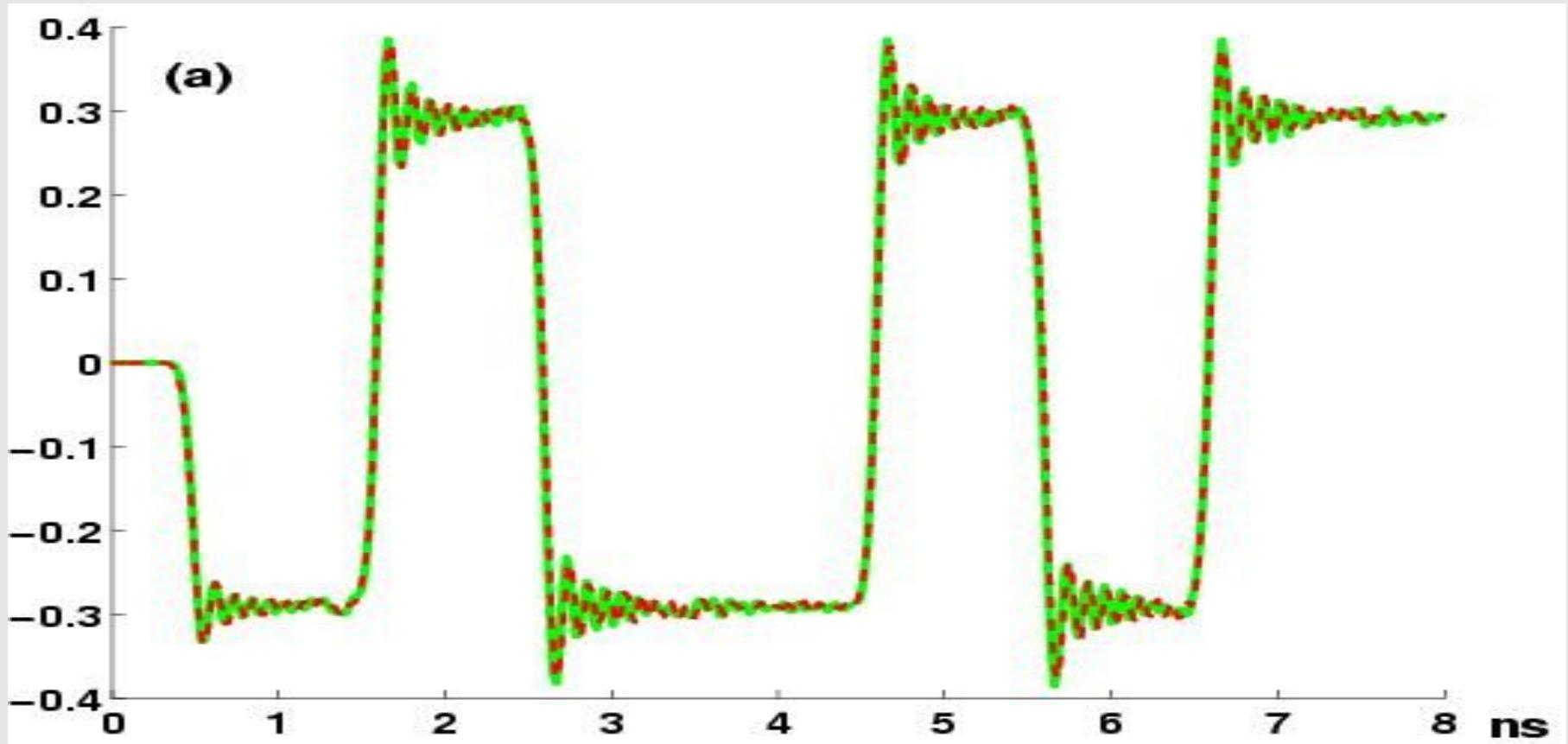
Single macromodel should work under a variety of loads/inputs

# Tapered CML Buffer Chain



- Stages sized to minimize buffer delay
  - output impedance = 50ohms

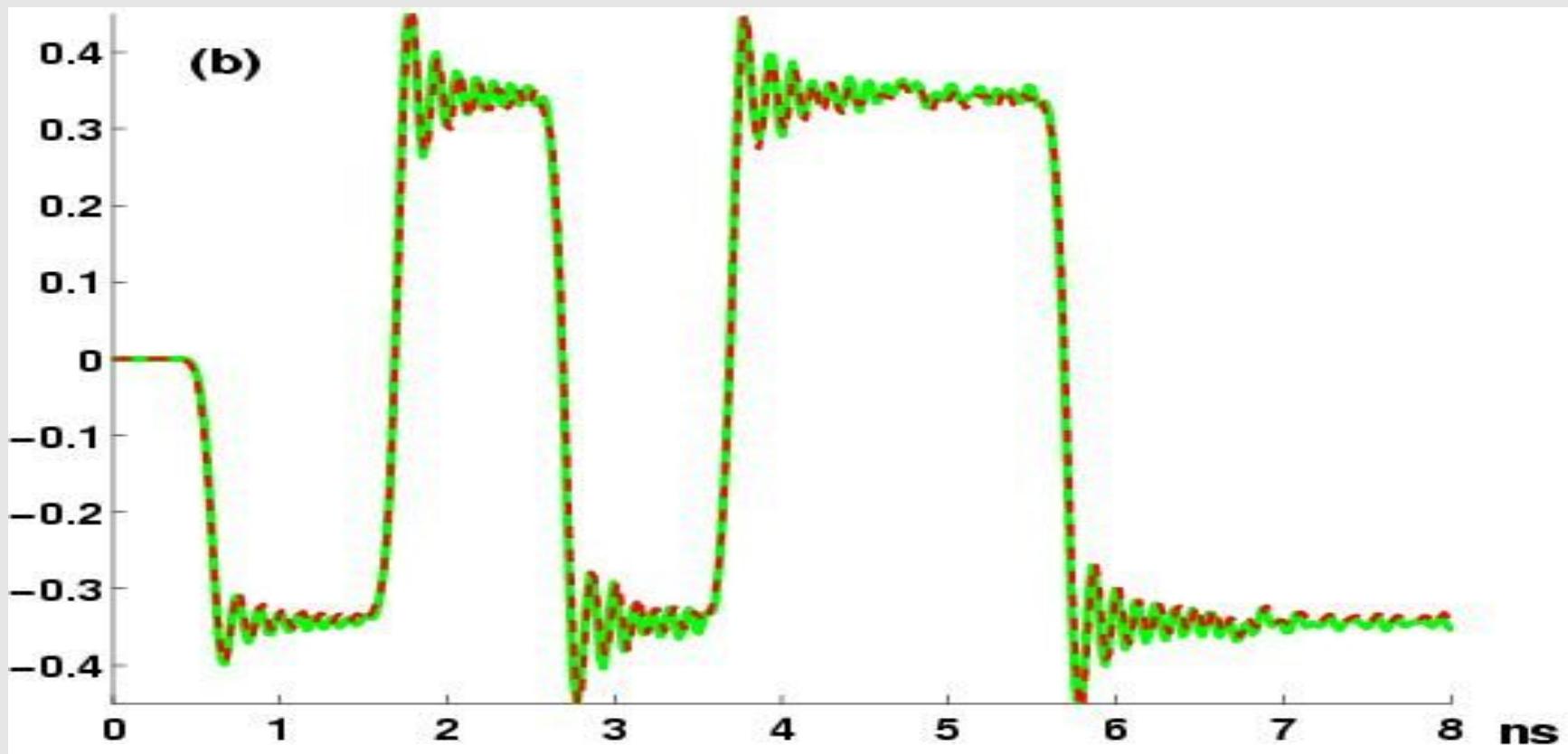
# CML buffer: lossless xline + matched resistive load, 75ohms



Input pattern: "0100101"      Ringing evident

8x speedup (MM over full)

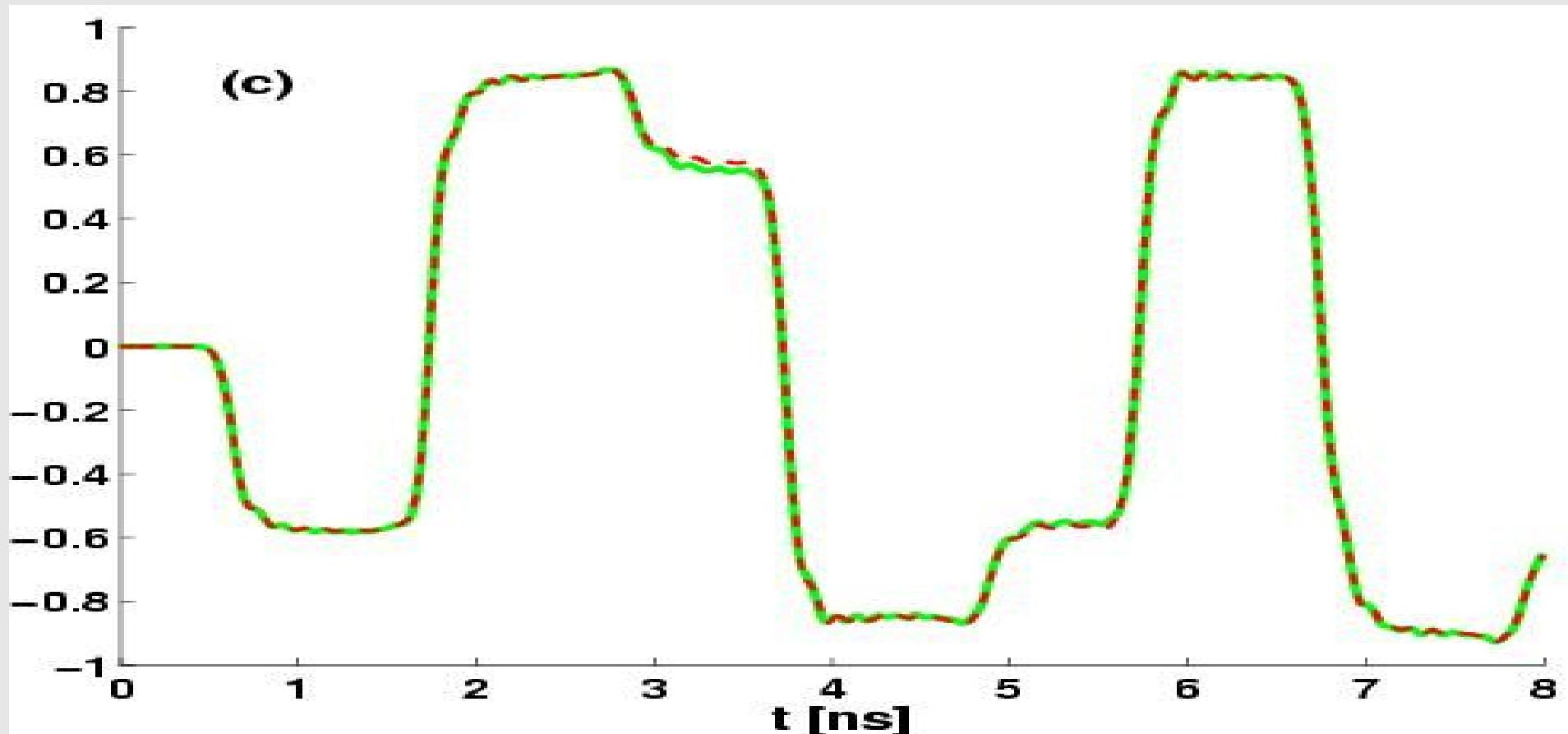
# CML buffer: lossy xline + matched resistive load, impedance=100ohms, loss=2ohms



Input pattern: “0101100”      Ringing still evident

8x speedup (MM over full)

**CML buffer: lossy xline + 1pF  
capacitive load, impedance=75ohms,  
loss=2ohms**

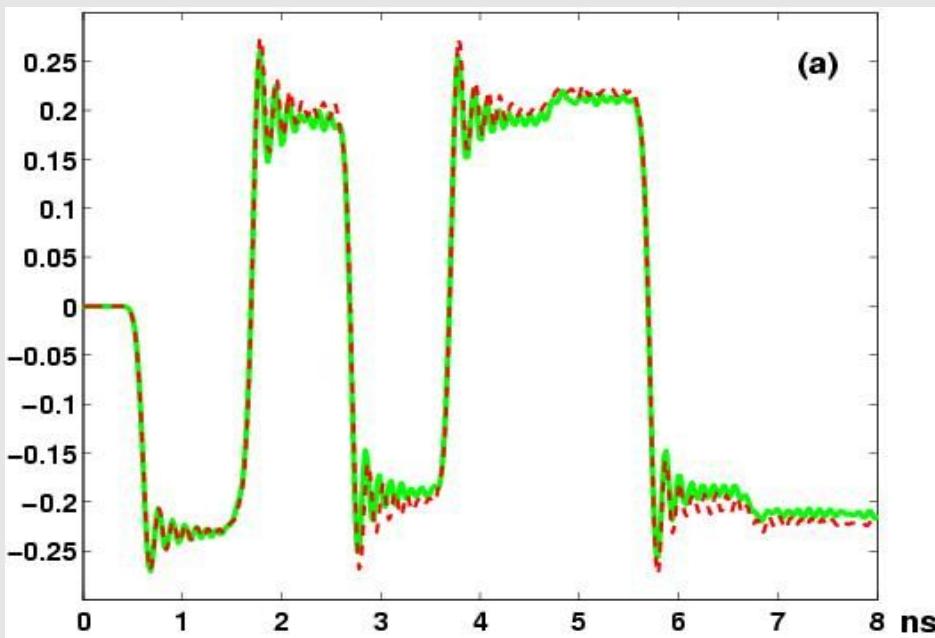
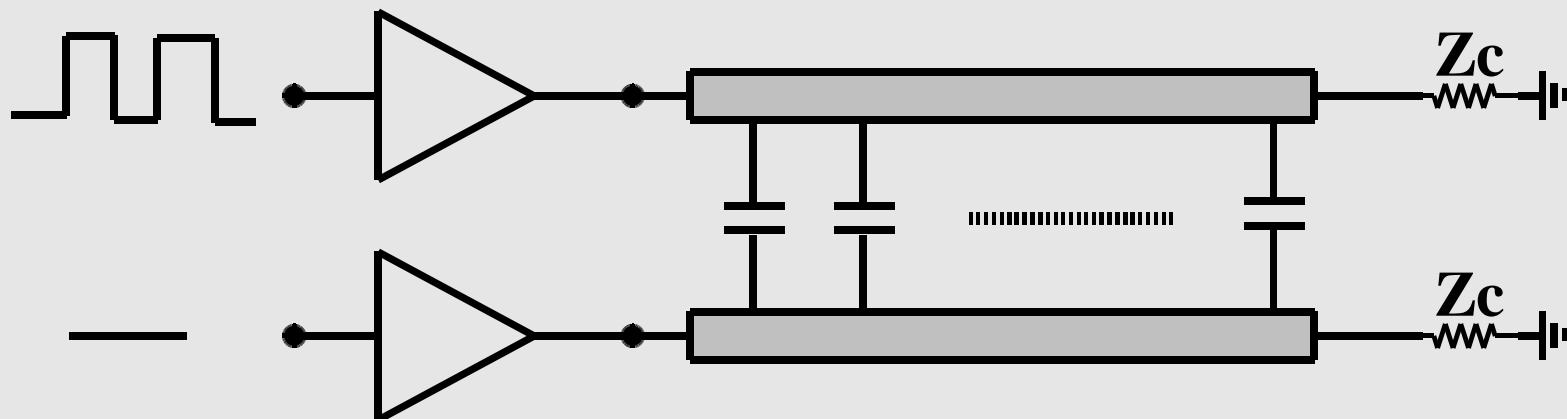


Input pattern: "0110010"

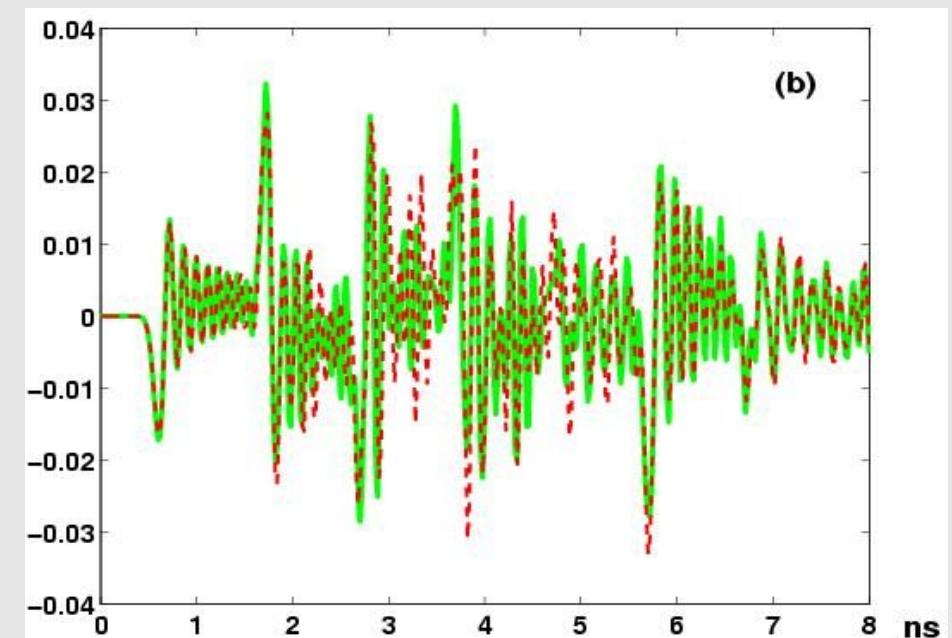
No ringing; note reflection effects

8x speedup (MM over full)

# Crosstalk Simulation

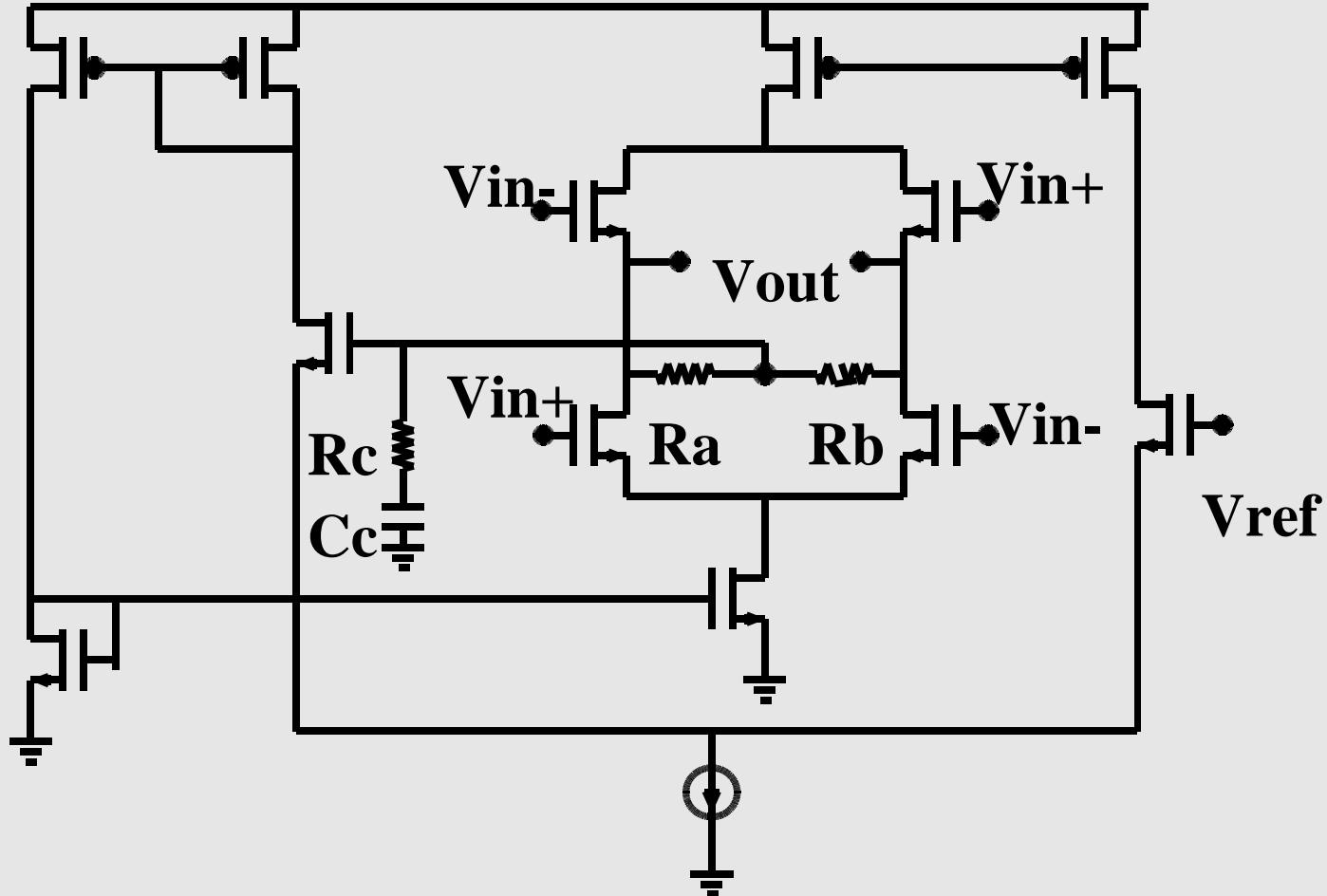


Load voltage, signal line



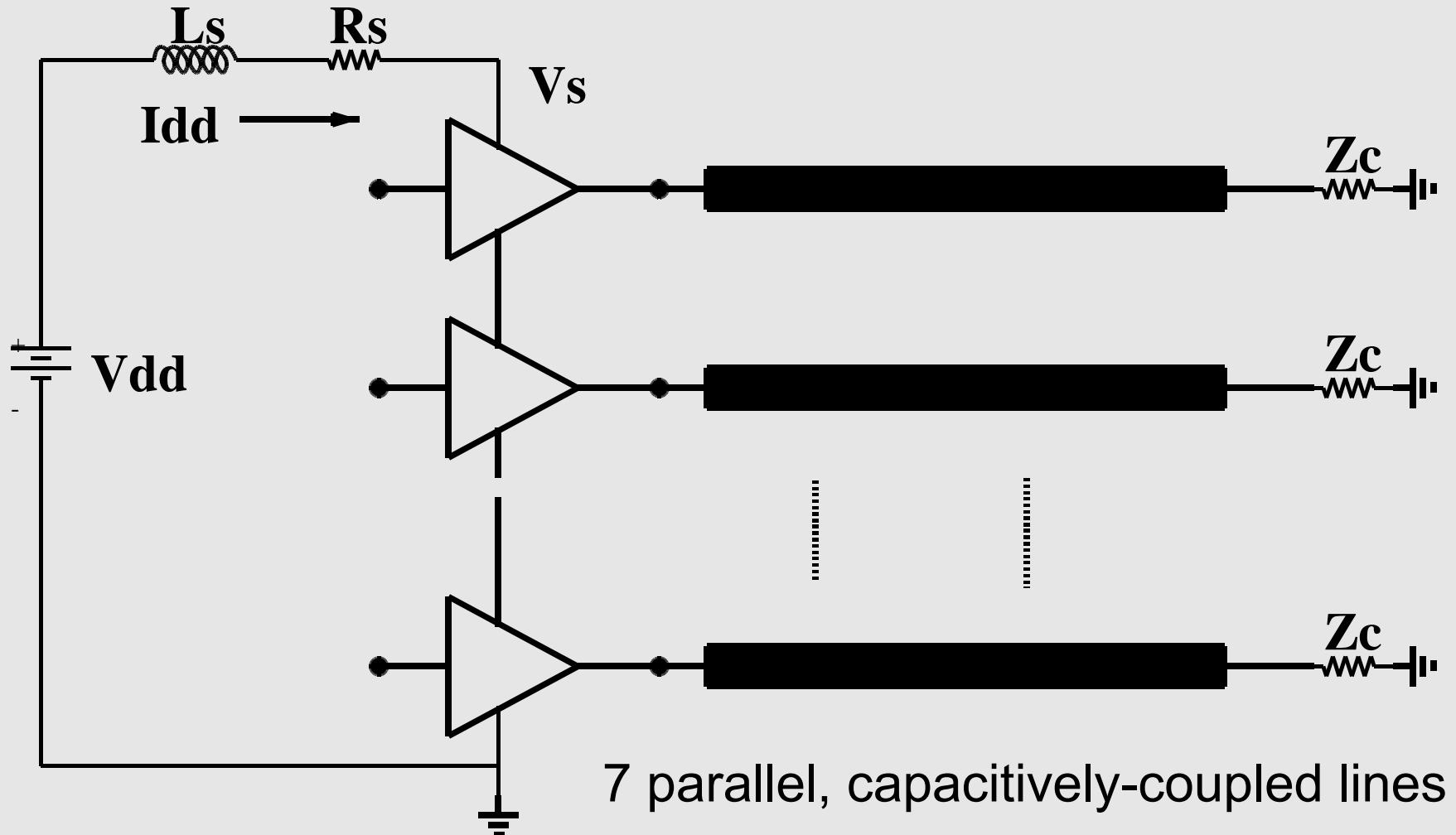
Load voltage, “quiet” line

# Low Voltage Differential Signalling (LVDS) I/O buffer

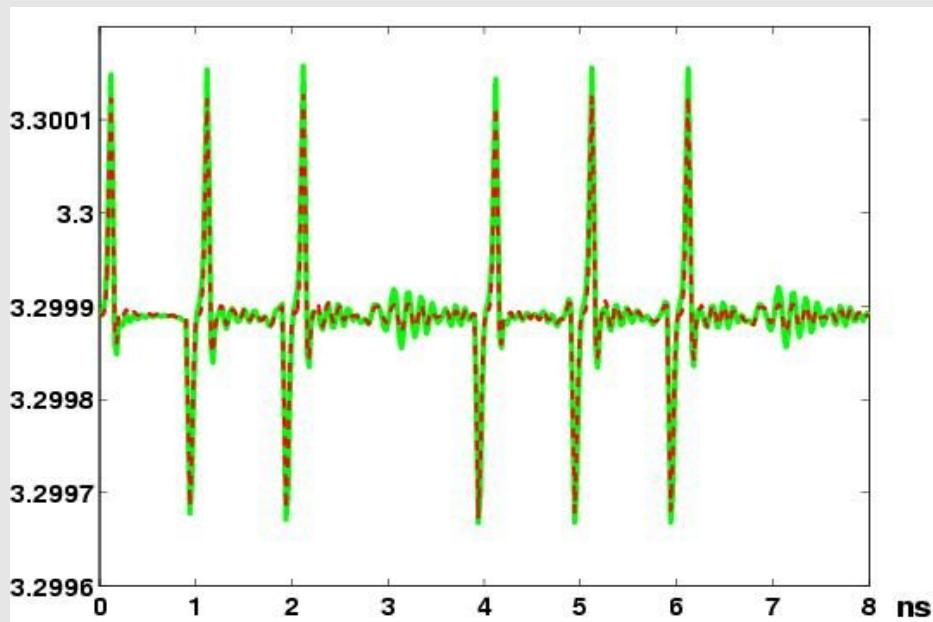


- Common-mode feedback; 50ohm drive

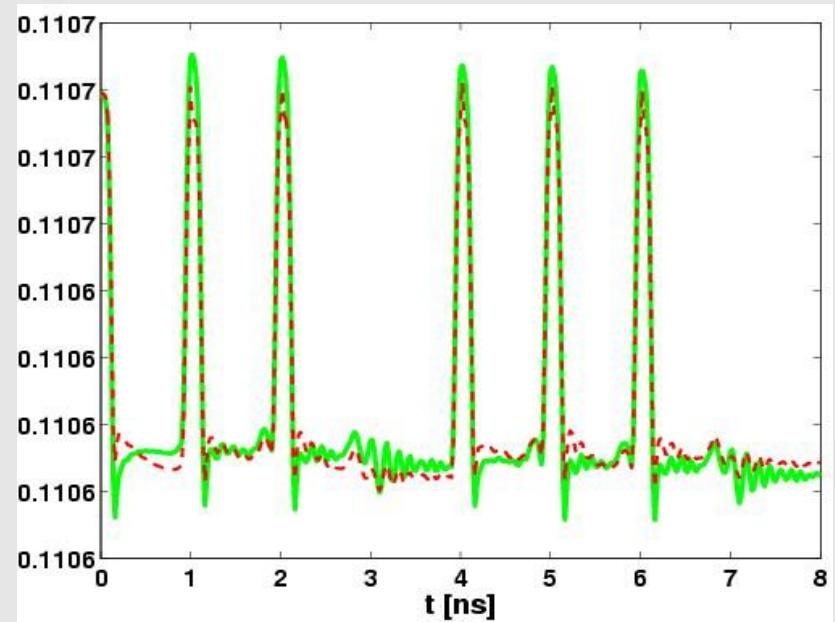
# LVDS buffer: SSN simulation setup



# SSN setup: near-end interference voltage/current

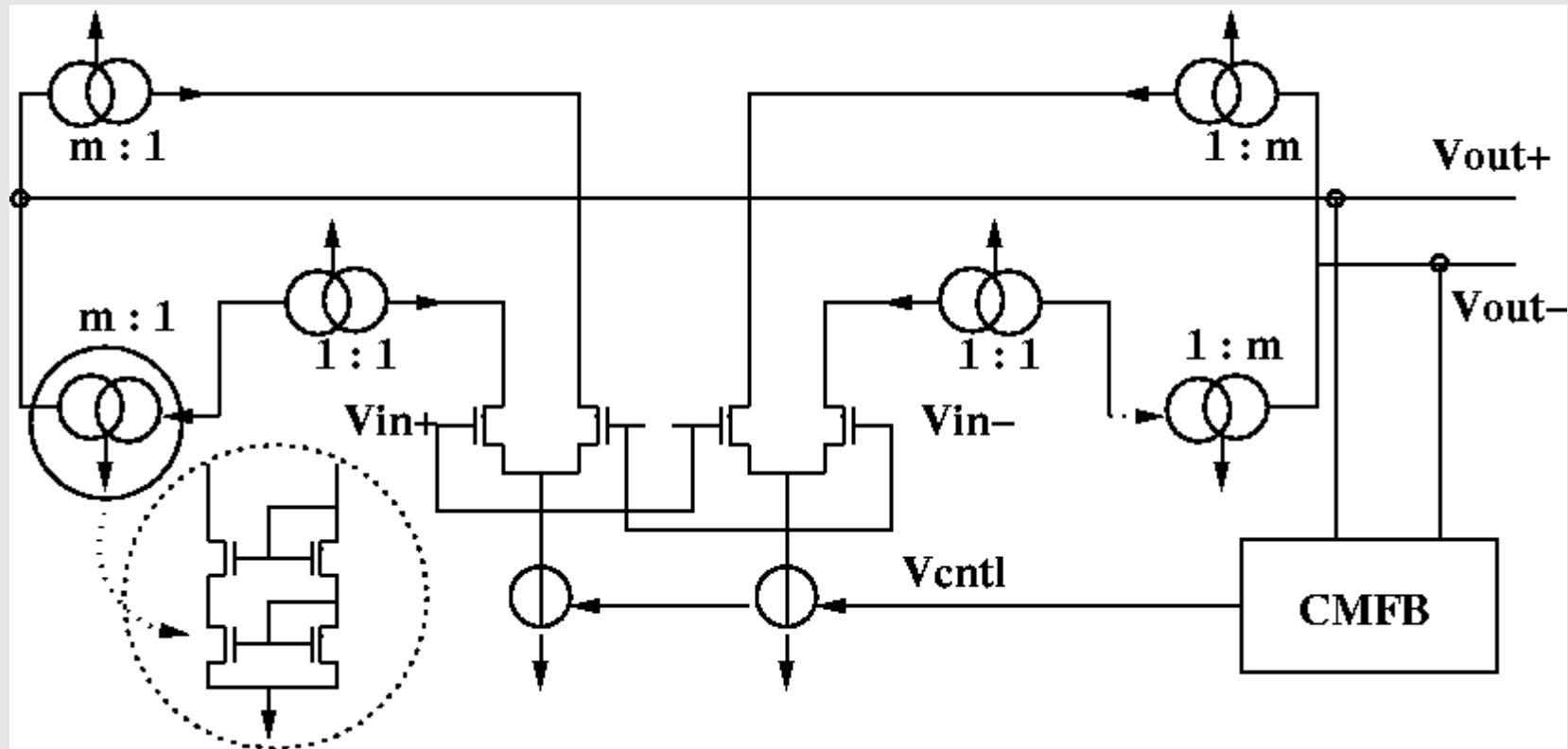


Near-end crosstalk voltage



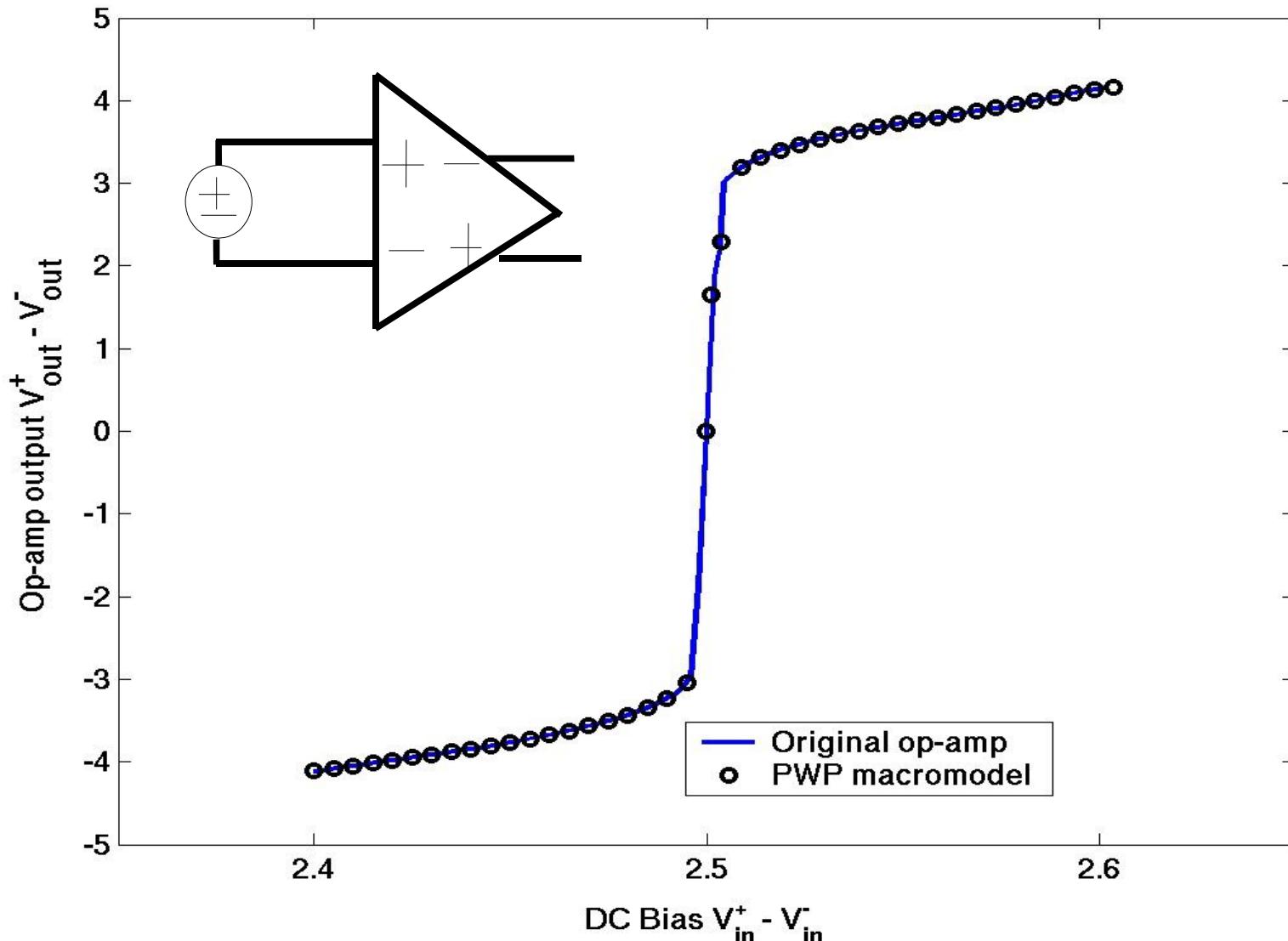
Near-end induced current

# Cascade Current-Mirror Op-Amp

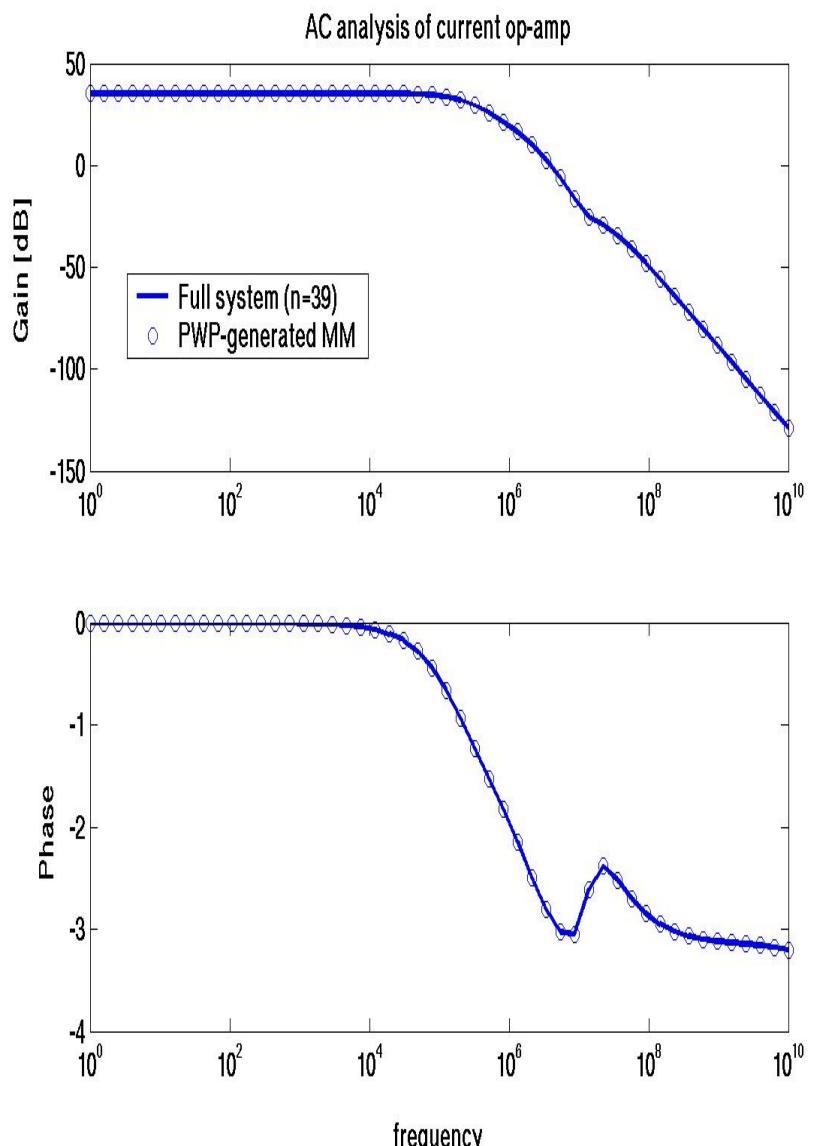
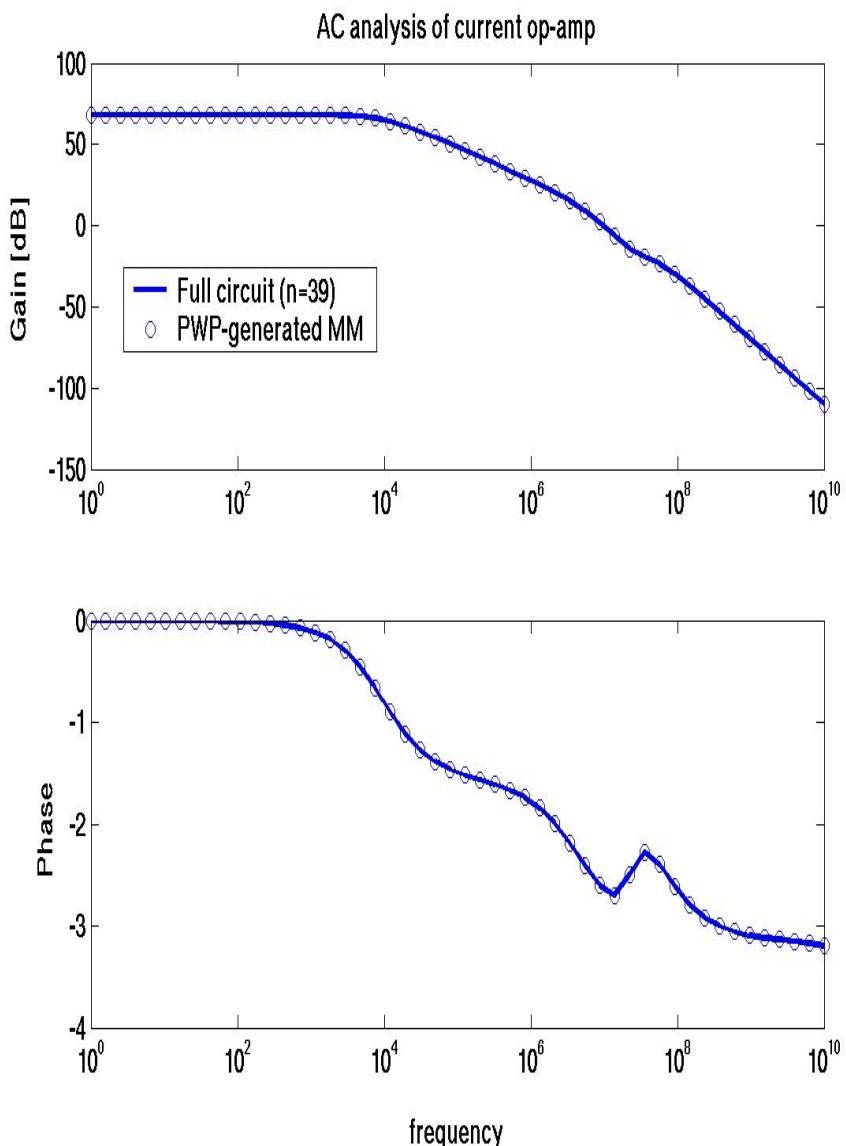


- 50 MOSFETs, 39 nodes

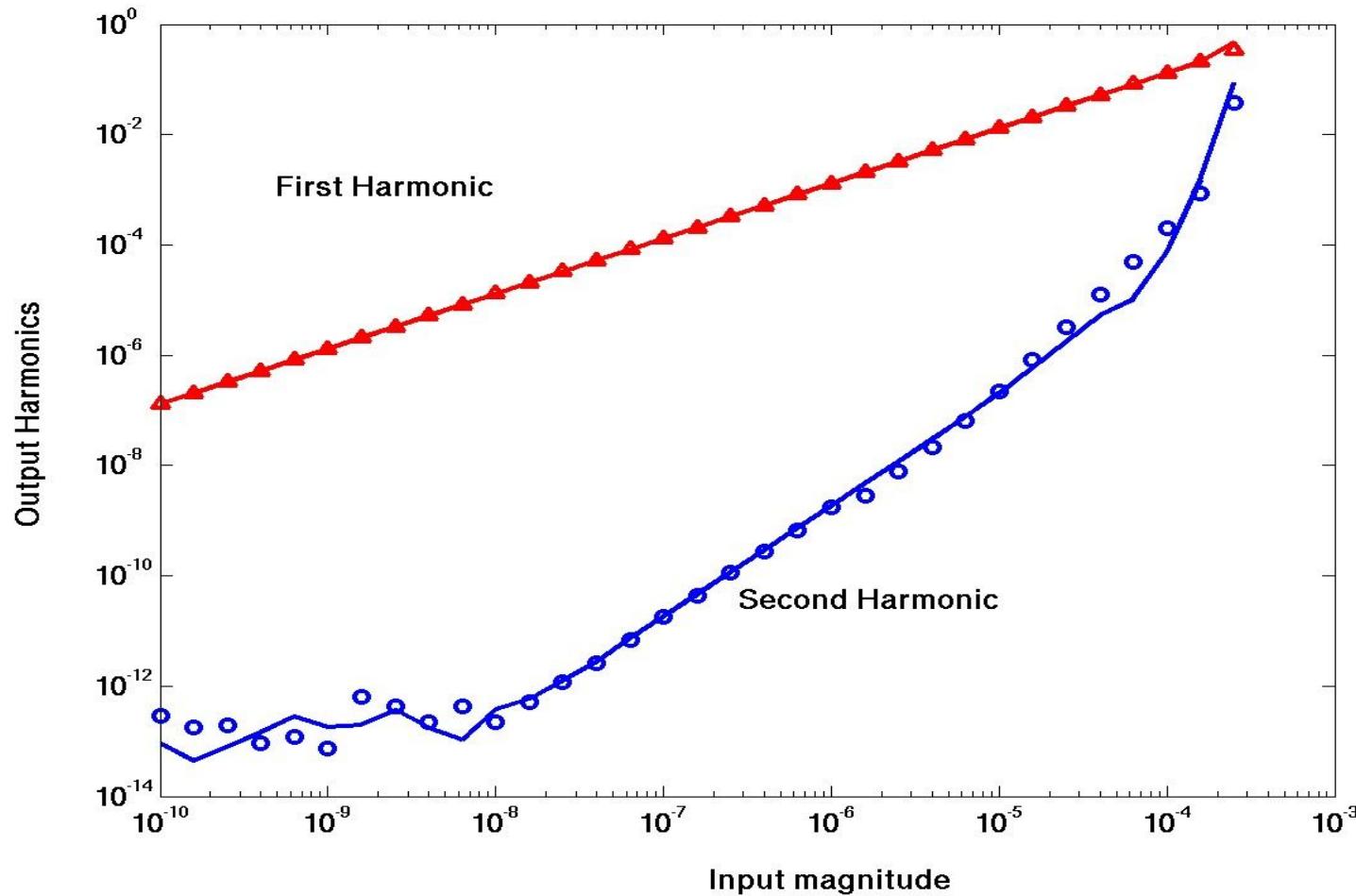
# DC Sweep



# AC Analyses at Different DC Bias Points



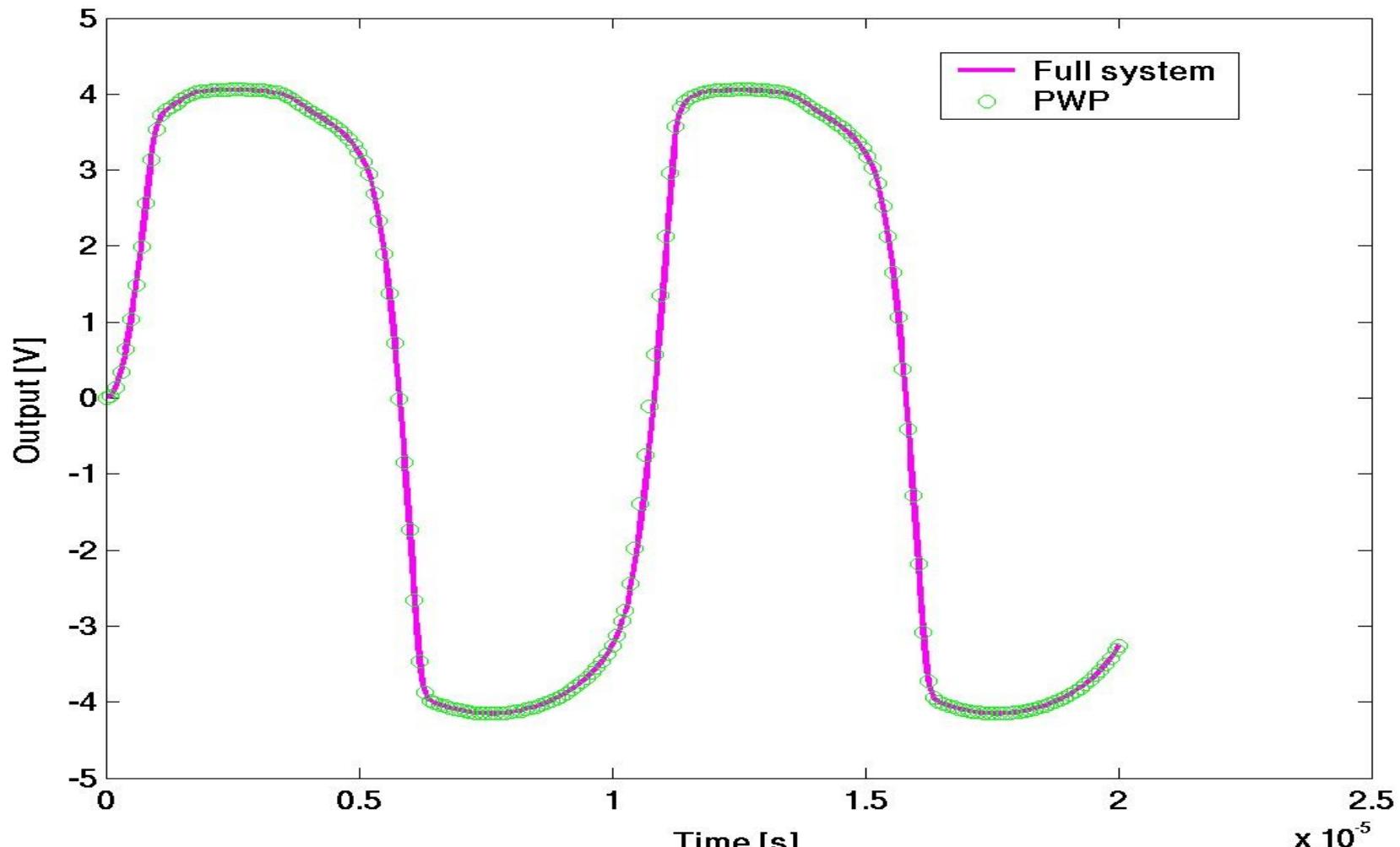
# Distortions via Harmonic Balance



$$V_{\text{in}}^+ - V_{\text{in}}^- = A \sin(2\pi 10^2 t)$$

125 sec (full system) vs. 16 sec (MM): 8x speedup

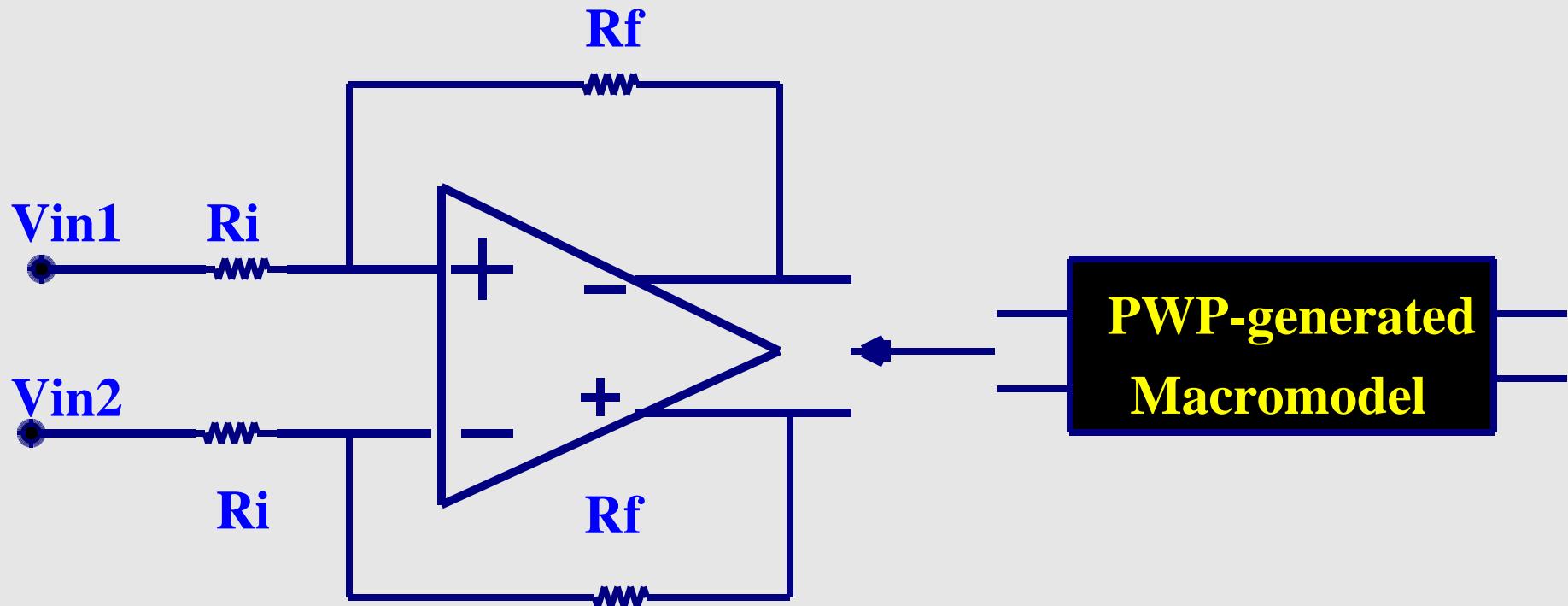
# Large Signal Transient



$$V_{\text{in}}^+ - V_{\text{in}}^- = 0.1 \sin(2\pi 10^5 t)$$

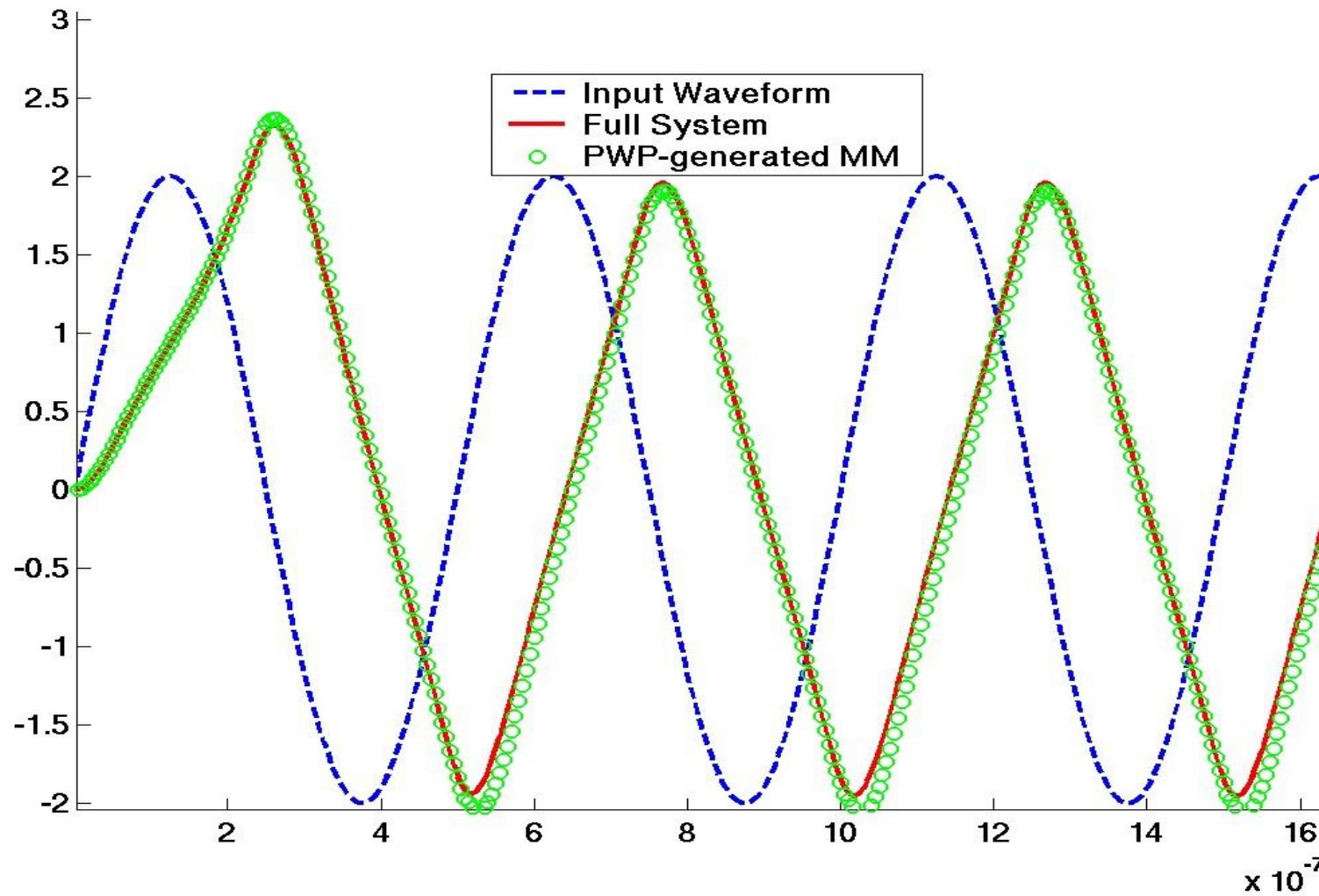
351 sec (full system) vs. 39 sec (MM): 9x speedup

# Embedded within External Feedback



- $R_f/R_i=10$ ,  $V_{in1} - V_{in2} = \sin(2\pi 10^6 t)$
- Vector I/O captures bidirectional loading effects

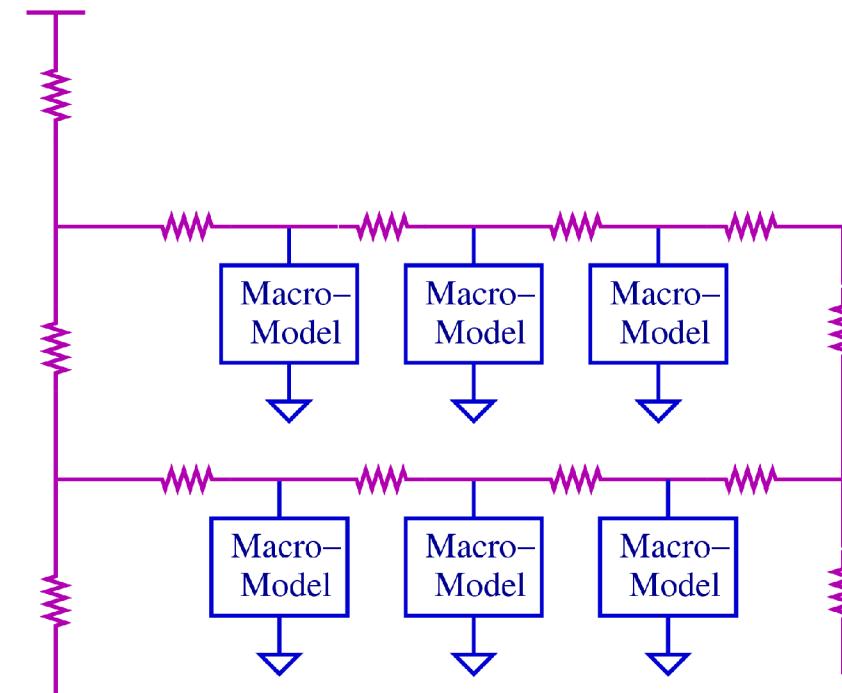
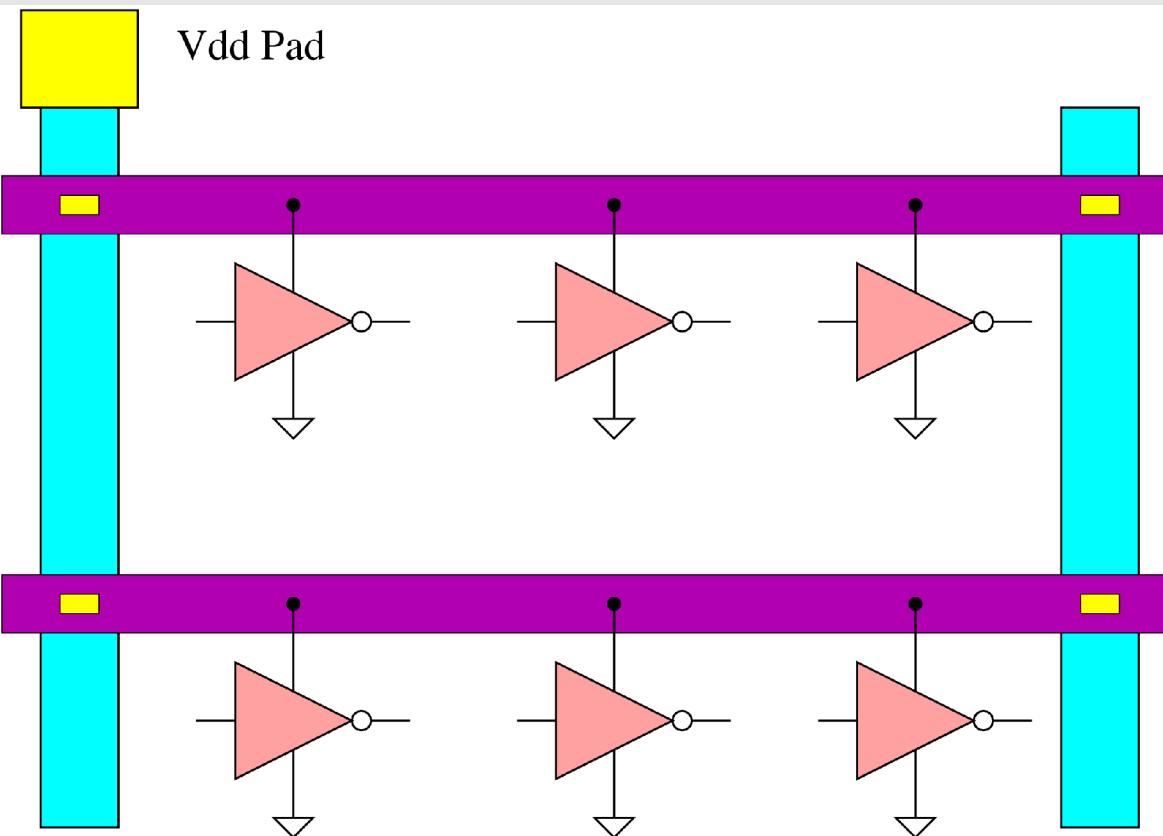
# Macromodel Captures Slewering



791 sec (full system) vs. 102 sec (MM): 7.7x speedup

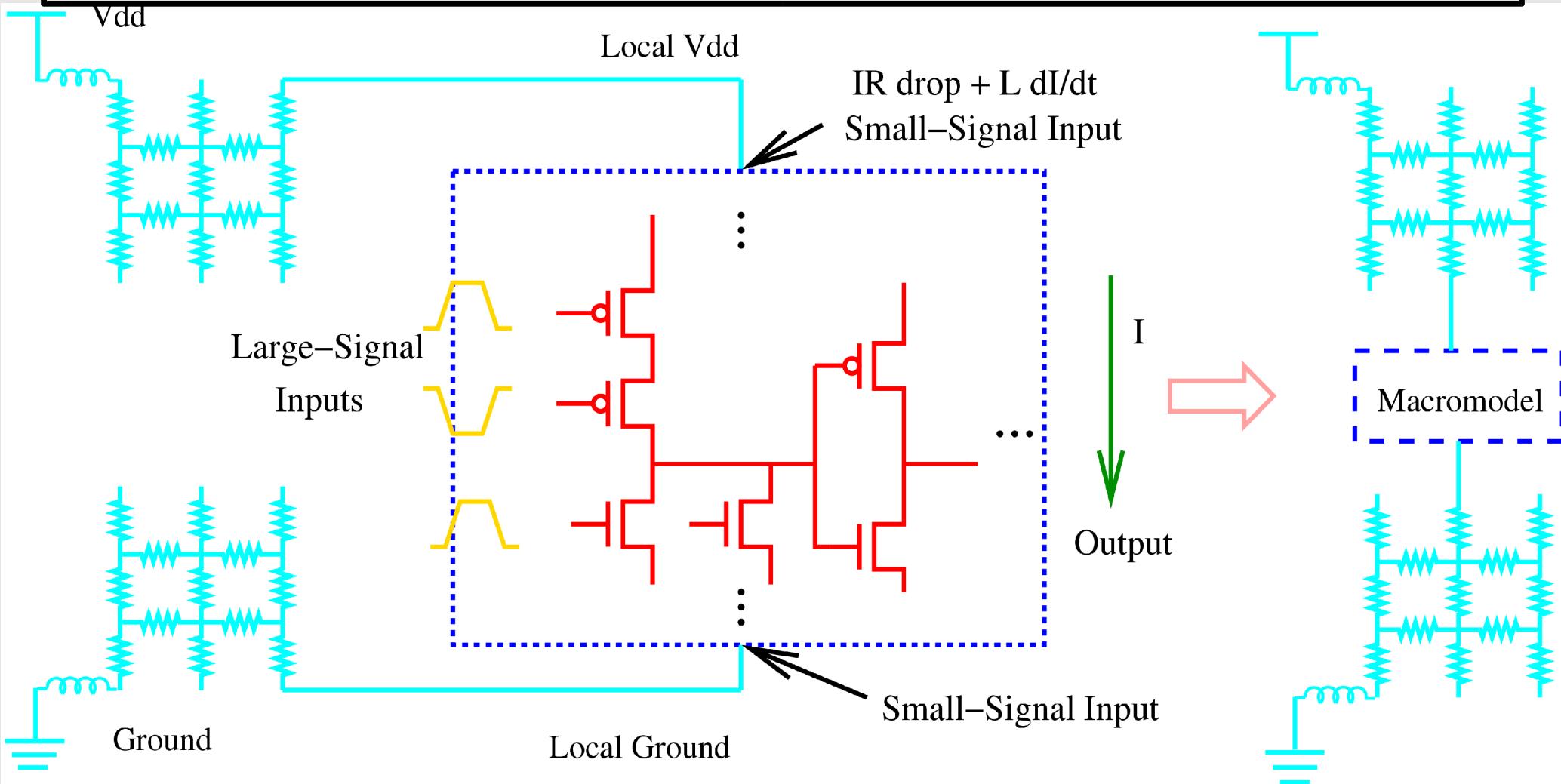
# **Modelling Power/Ground Noise due to digital switching using Time- Varying Linear Systems**

# Macromodelling Digital Noise Injection



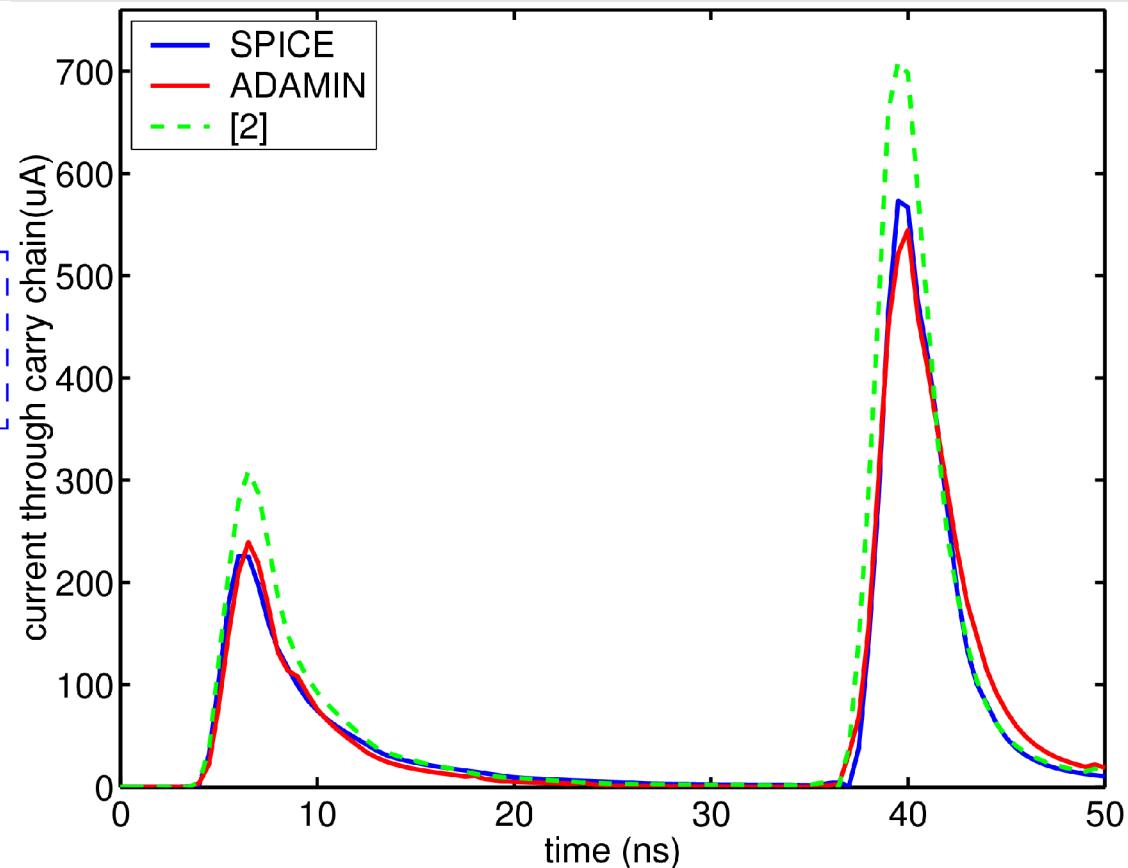
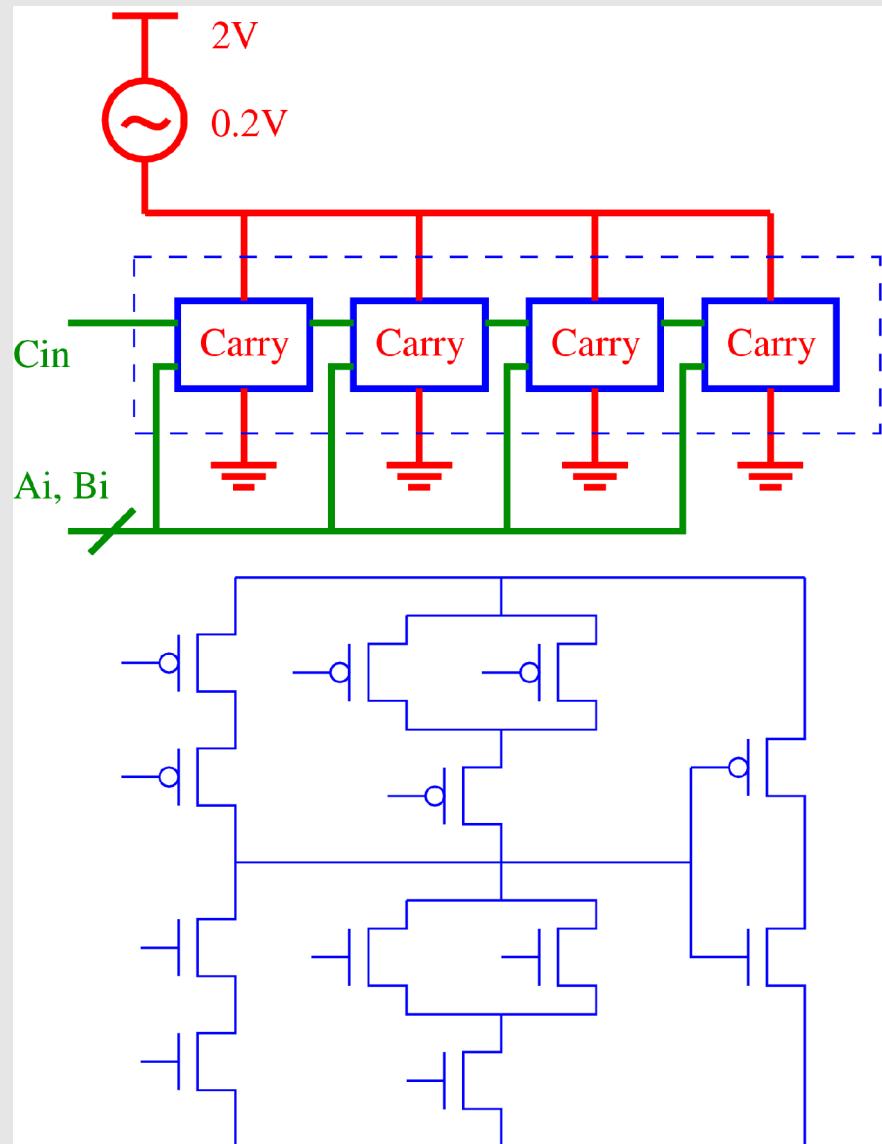
- Interested **only in interference injection aspect**
  - supply and substrate injections: analog waveforms
  - digital signals: system time variation
  - **LTV model captures switching behaviour well!**

# LTV Digital Aggressor Macromodels



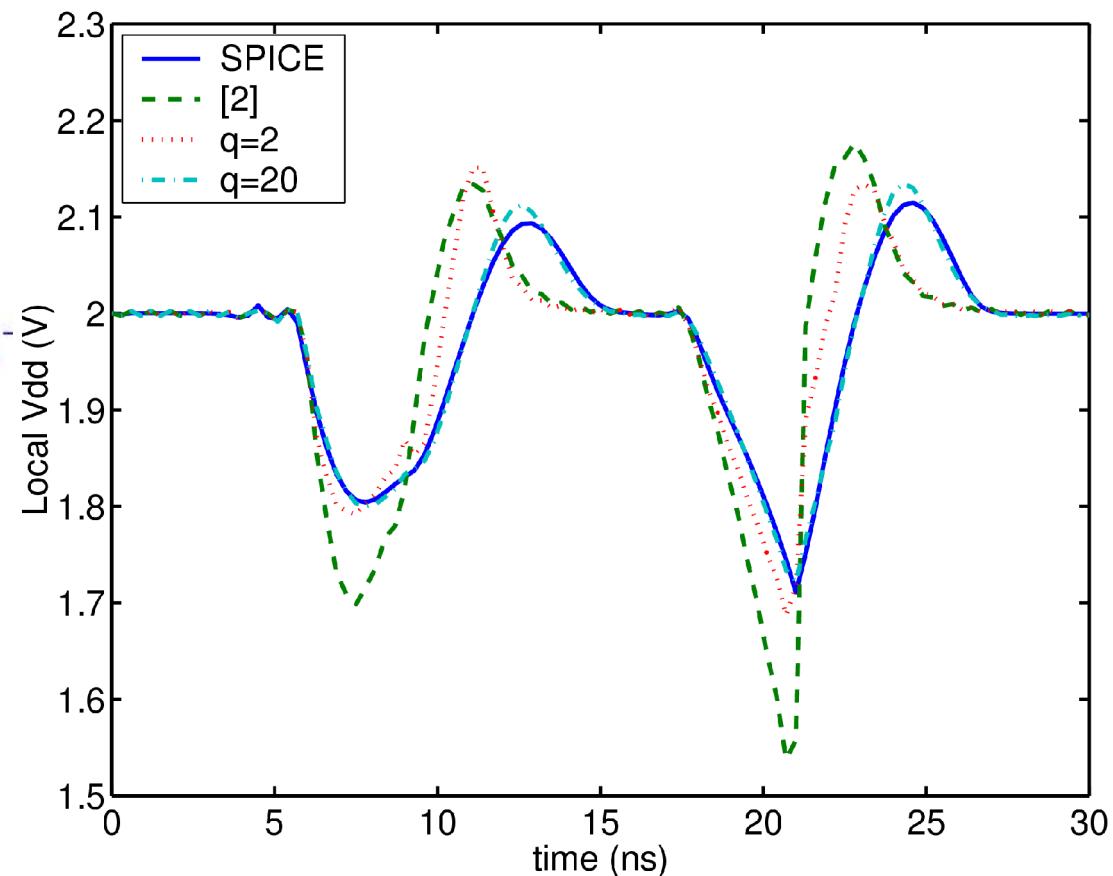
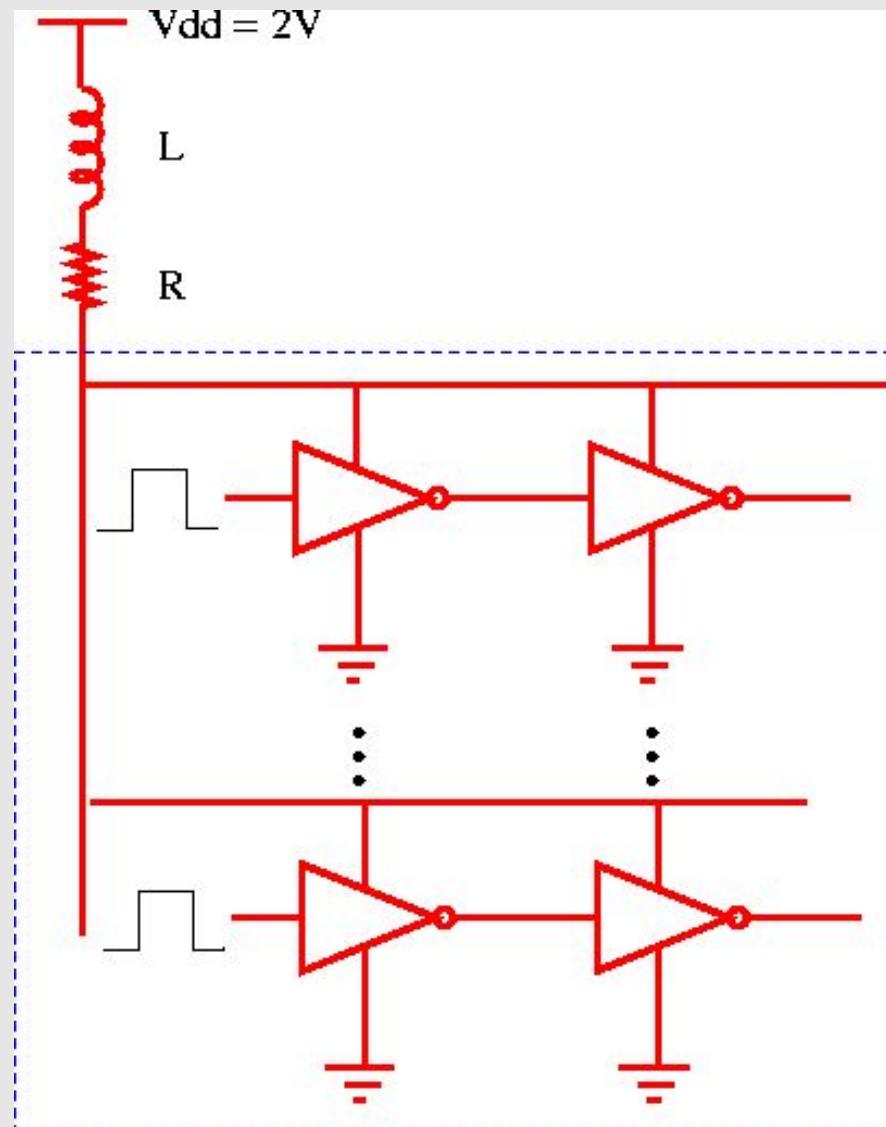
- Input: (eg) power supply voltage variation
- Output: resulting current variation
- MM: small time-varying system relating input to output

# Supply-noise Induced Currents: Carry Chain



- Considerable accuracy improvement over current-source macromodel [Dharchoudhury 98]

# Simulation with Inductive Supply Grid

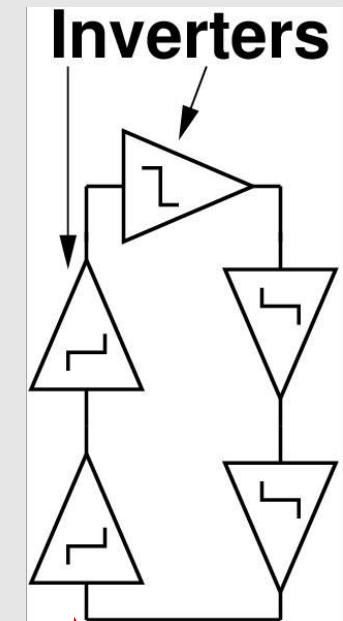
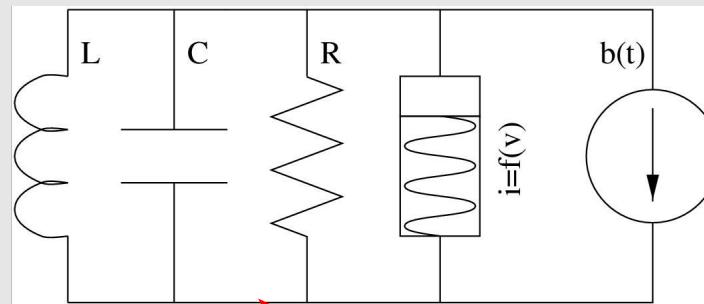


- size 2 MM: already better
- size 20: much more accurate
- 17000x speedup for 8000 gates

# Oscillators and PLLs: Modelling and Simulation

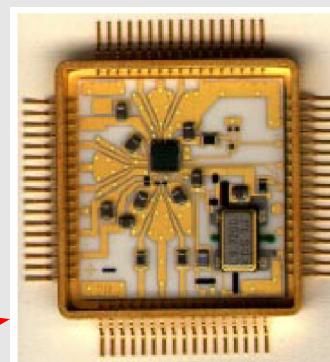
# Oscillators and PLLs

- Oscillators and PLLs: critical in comm. systems
  - VCOs
  - PLLs
- Applications
  - CDR ckts
  - synchronization loops
  - frequency synthesis



Rick Walker, HP/Agilent

PLLs



Rick Walker, HP/Agilent

# Why Oscillators/PLLs are a Special Simulation Challenge

- Computation/size/accuracy: much greater than amps/mixers
- Even 1-transistor oscillators (eg, UHF oscs, >100GHz)
  - long startups, tiny timesteps needed
  - 100K cycles of VCO typical for PLL simulation
  - on-chip RF: 100s to 1000s of transistors
- Complex dynamical phenomena
  - frequency capture/lock-in/freq-hopping
  - phase noise/jitter
  - injection locking
  - cycle slipping

**Phase Domain Macromodels  
offer huge speedups  
(even for small circuits)**

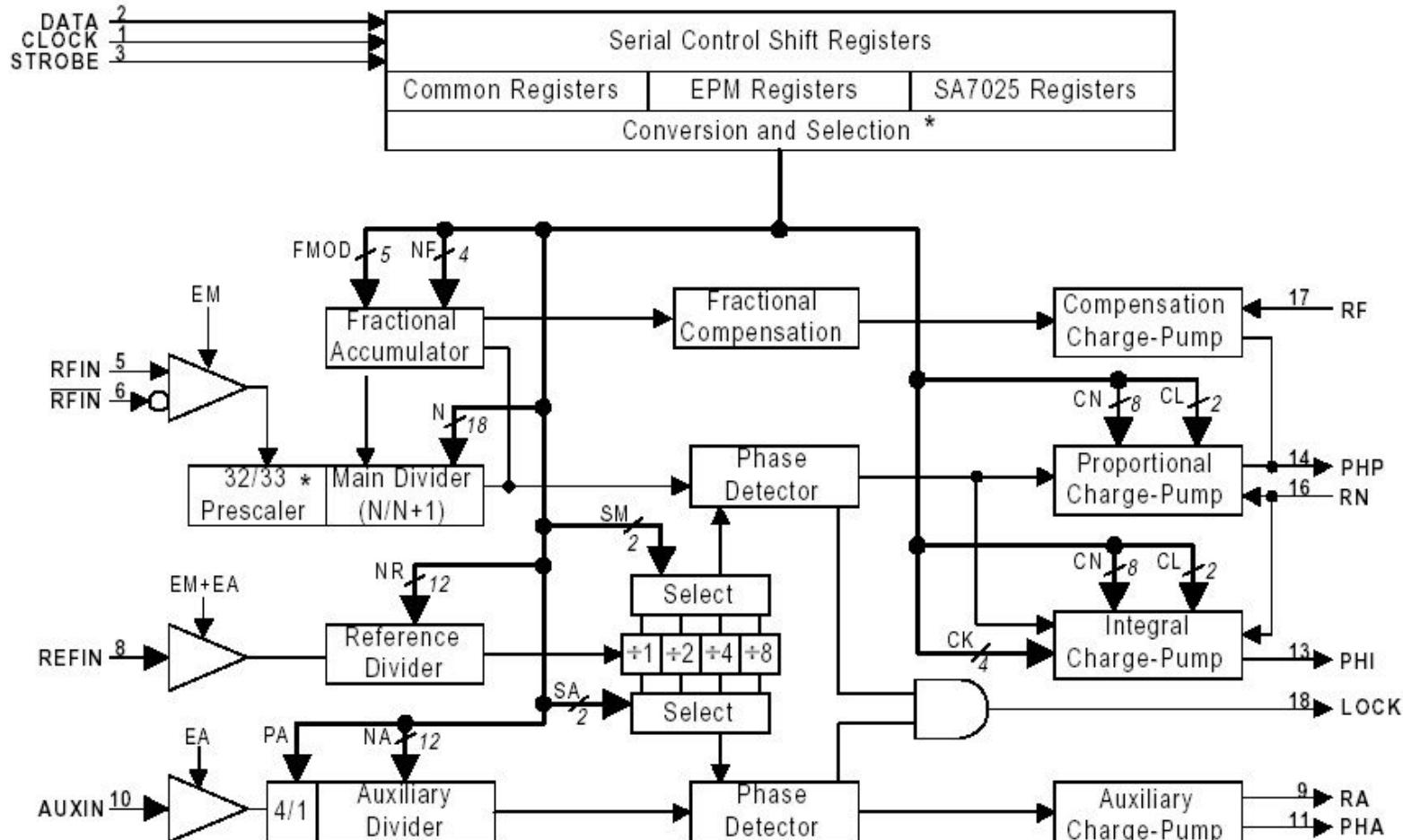
# PLL Applications

- Clock and data recovery (CDR)
  - synchronization: Costas Loop
  - applications: communication systems, disk-drive read-channels
- Frequency synthesizers
  - integer-N, fractional-N synthesizers
  - direct digital to GPSK modulation

# TI TRF-2050 Fractional-N PLL

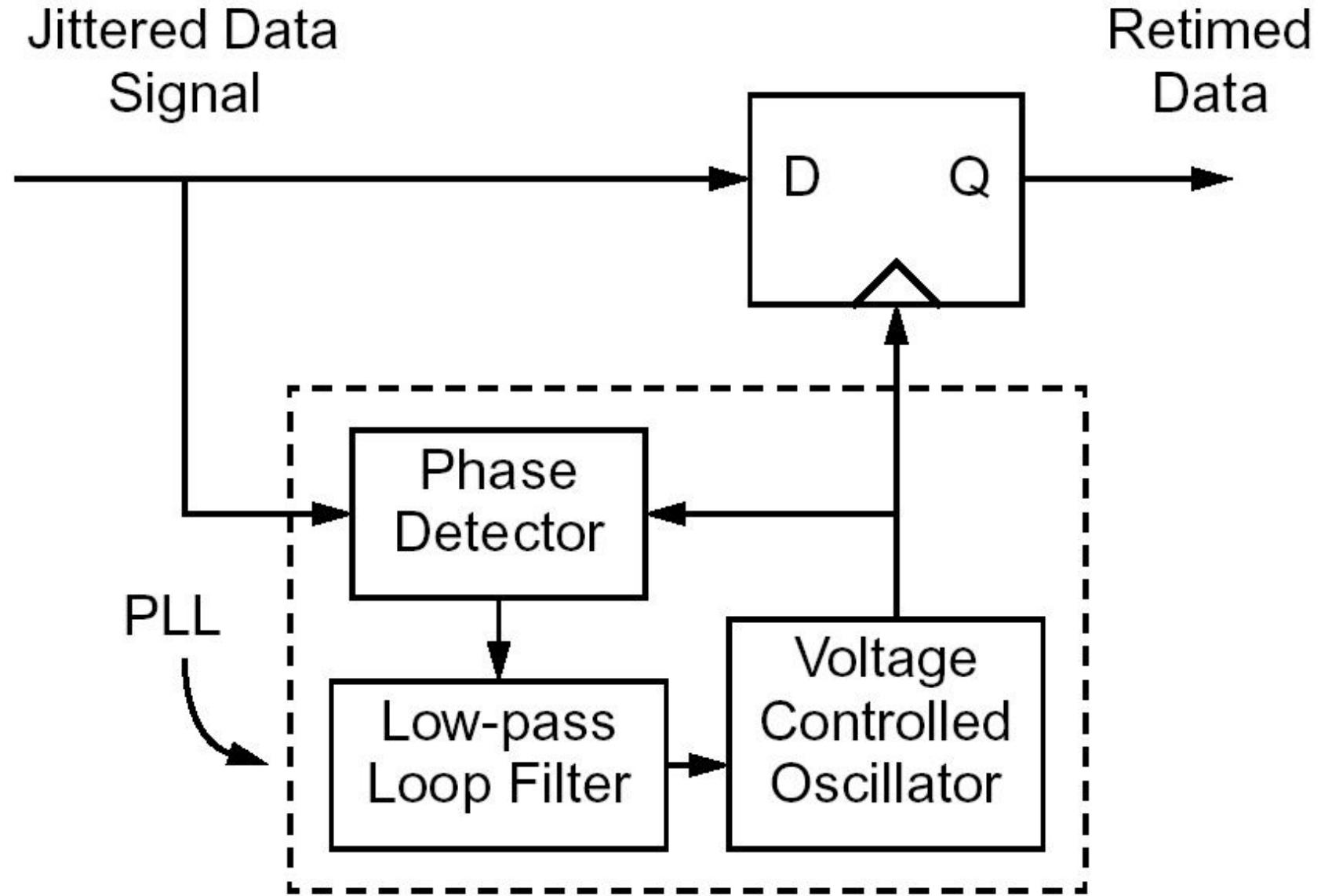
Figure 21. Fractional-N PLL - TI Model TRF2050

Texas Instruments



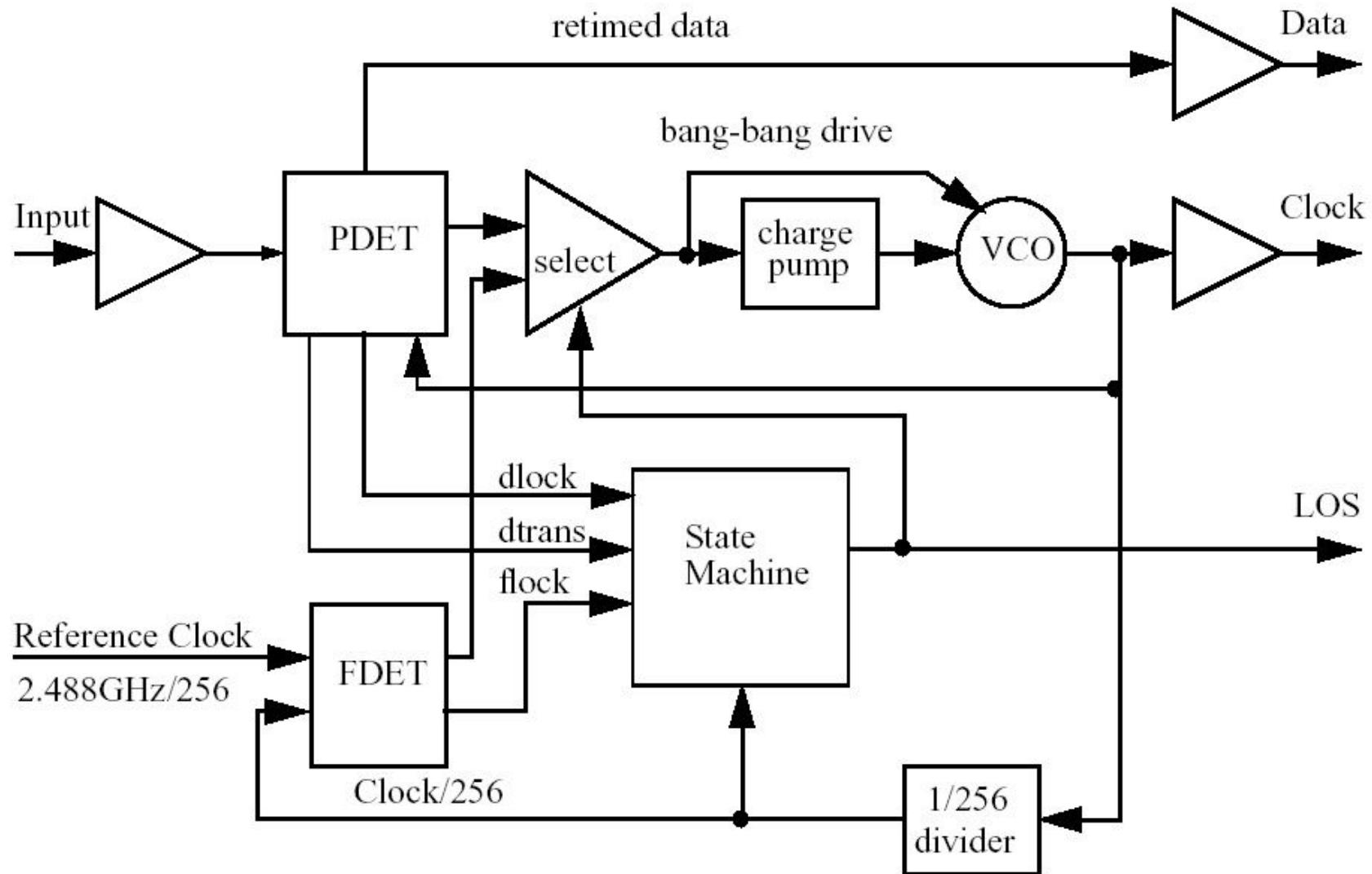
Large; complex; many interconnected functional blocks

# PLL-based CDR Operation



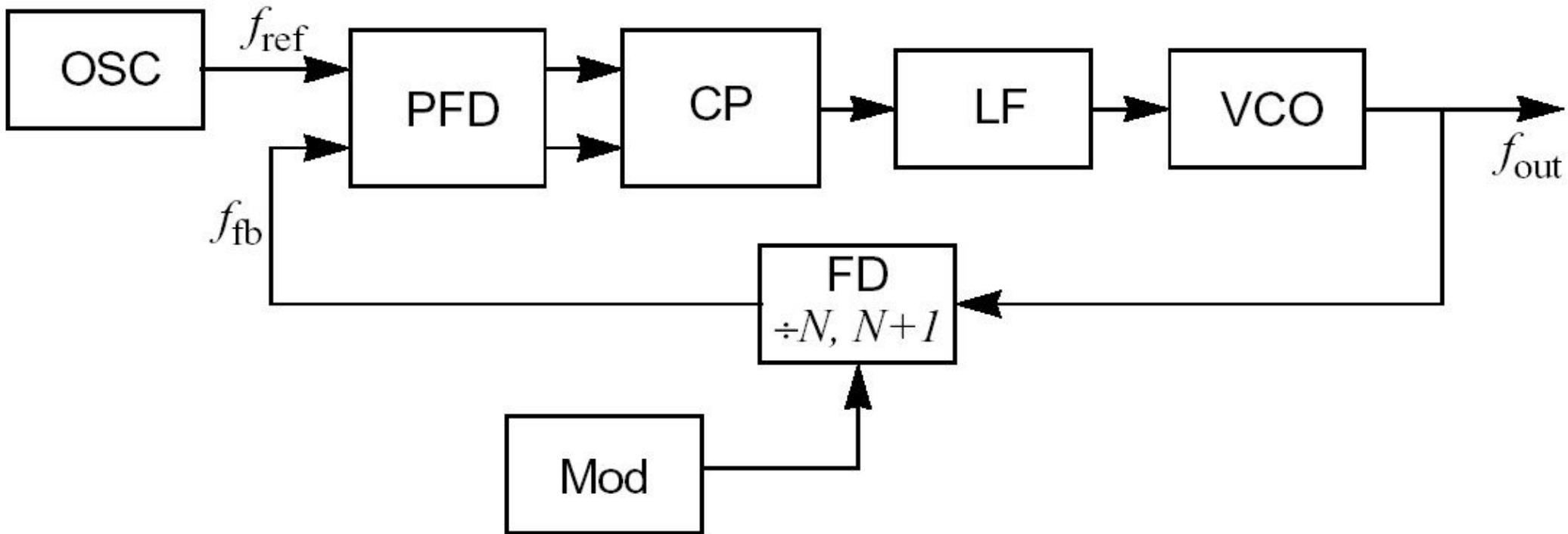
PLL recovers clock signal from asynchronous data

# Clock and Data Recovery (CDR) ckt



Mixed-signal PLL: very hard to simulate at ckt level

# Integer-N, Fractional-N PLL Synthesizers

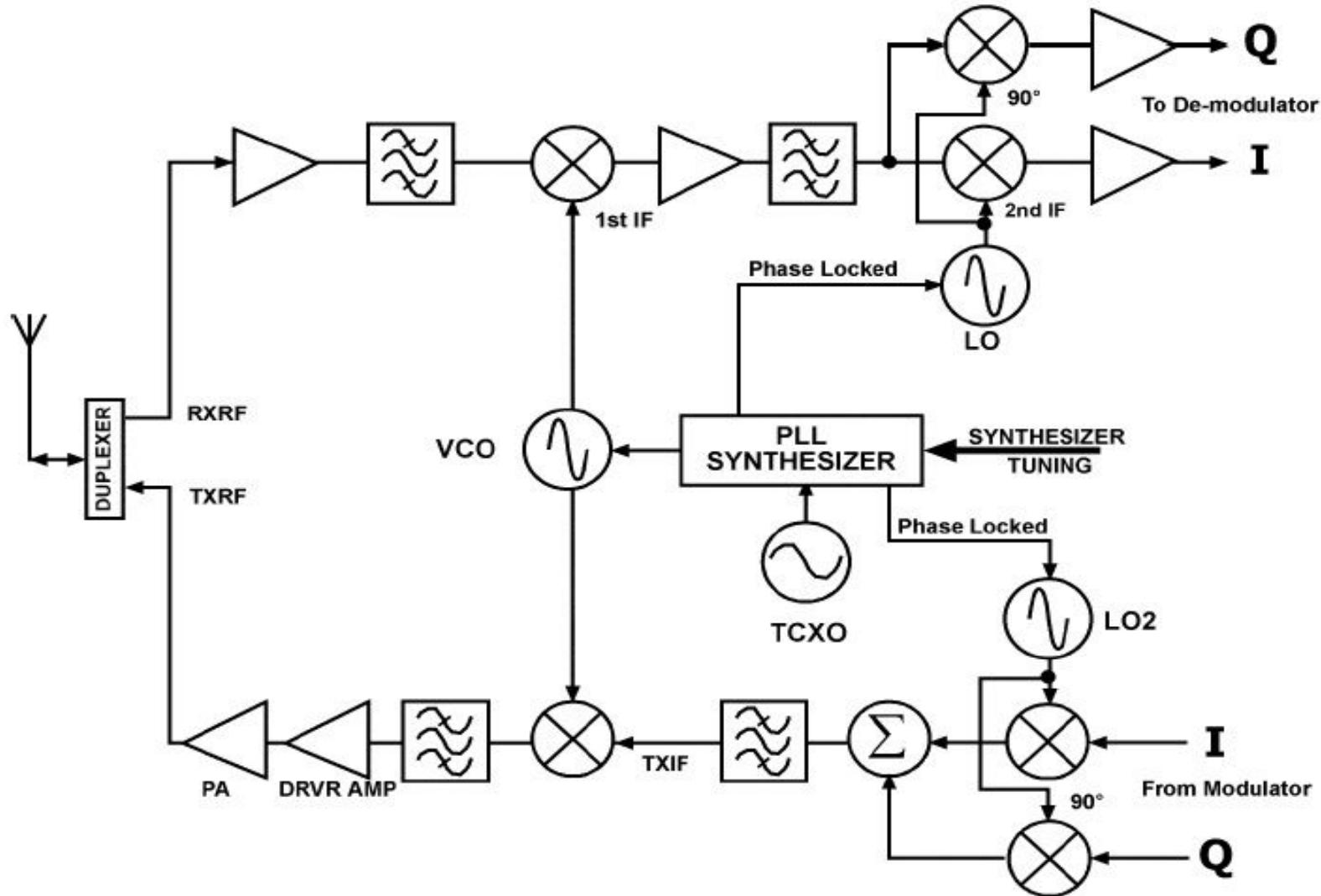


Ken Kundert, Cadence

Wide frequency programmability range

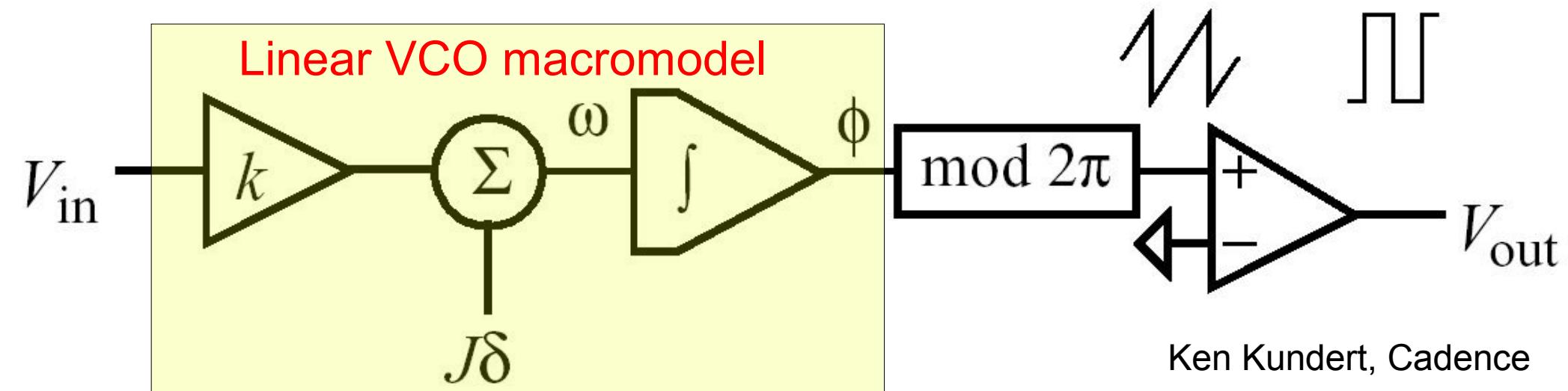
# PLL-based Synthesizers in Transceivers

Texas Instruments



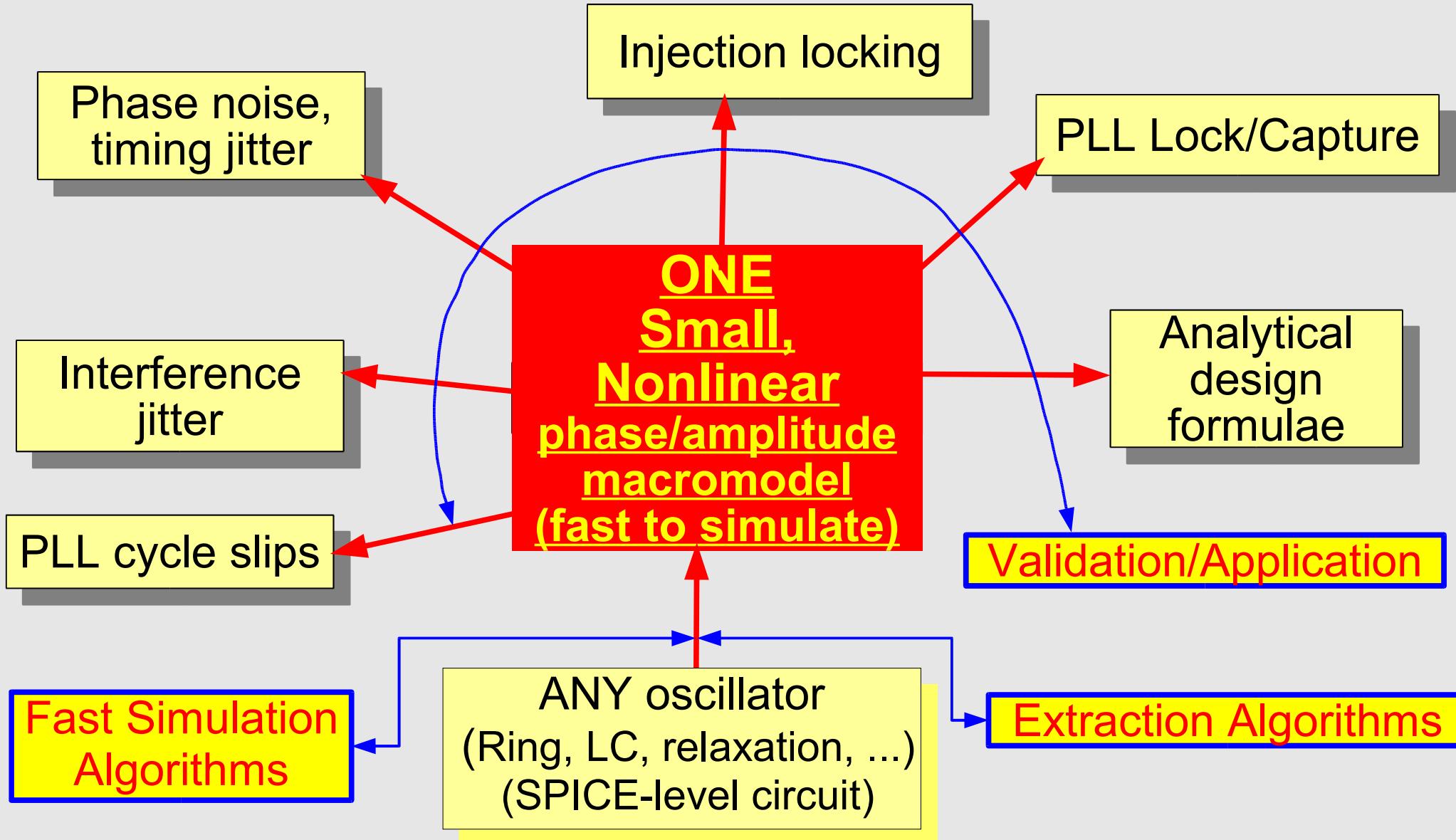
Fast frequency programmability; good jitter performance

# Linear Macromodelling of VCOs/PLLs



- Output VCO phase = integral of input control
- Good for intuition, hand calculations, noise trends
- **Cannot capture nonlinear phenomena**
  - (injection locking, jitter, cycle slips, power grid noise effects, ...)
- **Nonlinear phase macromodels: huge improvement**

# ONE Automatically Extracted Macromodel works for ALL effects, ALL oscillators



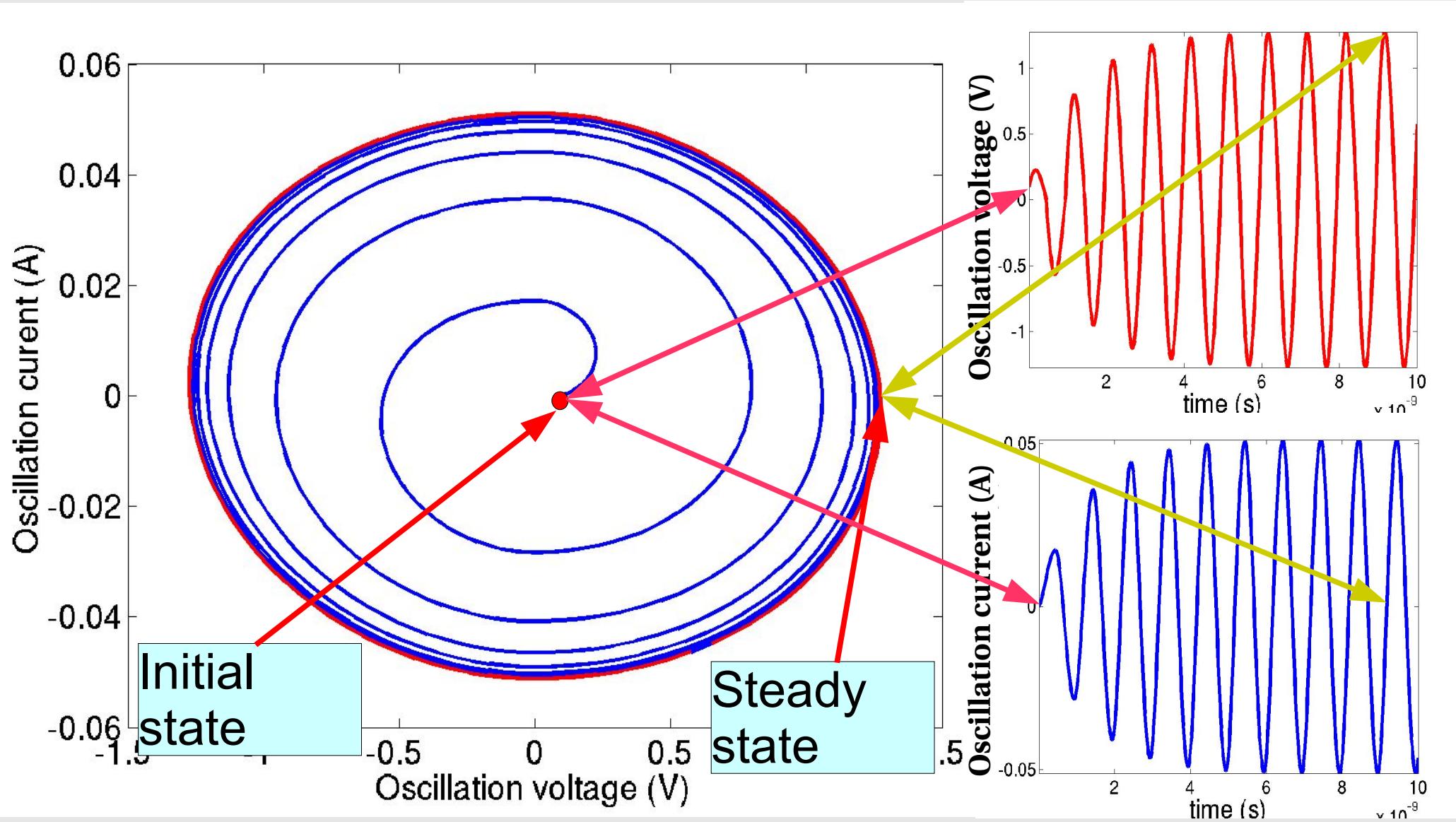
# Limitations of Linear Phase Macromodels

- Linear models are **not generally applicable** for all effects
  - LTI model: **narrow applicability**
  - LPTV models, including:
    - Kaertner's LPTV IRF
    - Hajimiri's closed-form ISF
    - better, but validity depends on circuit/dynamical effects
- Linear models cannot capture nonlinear dynamics

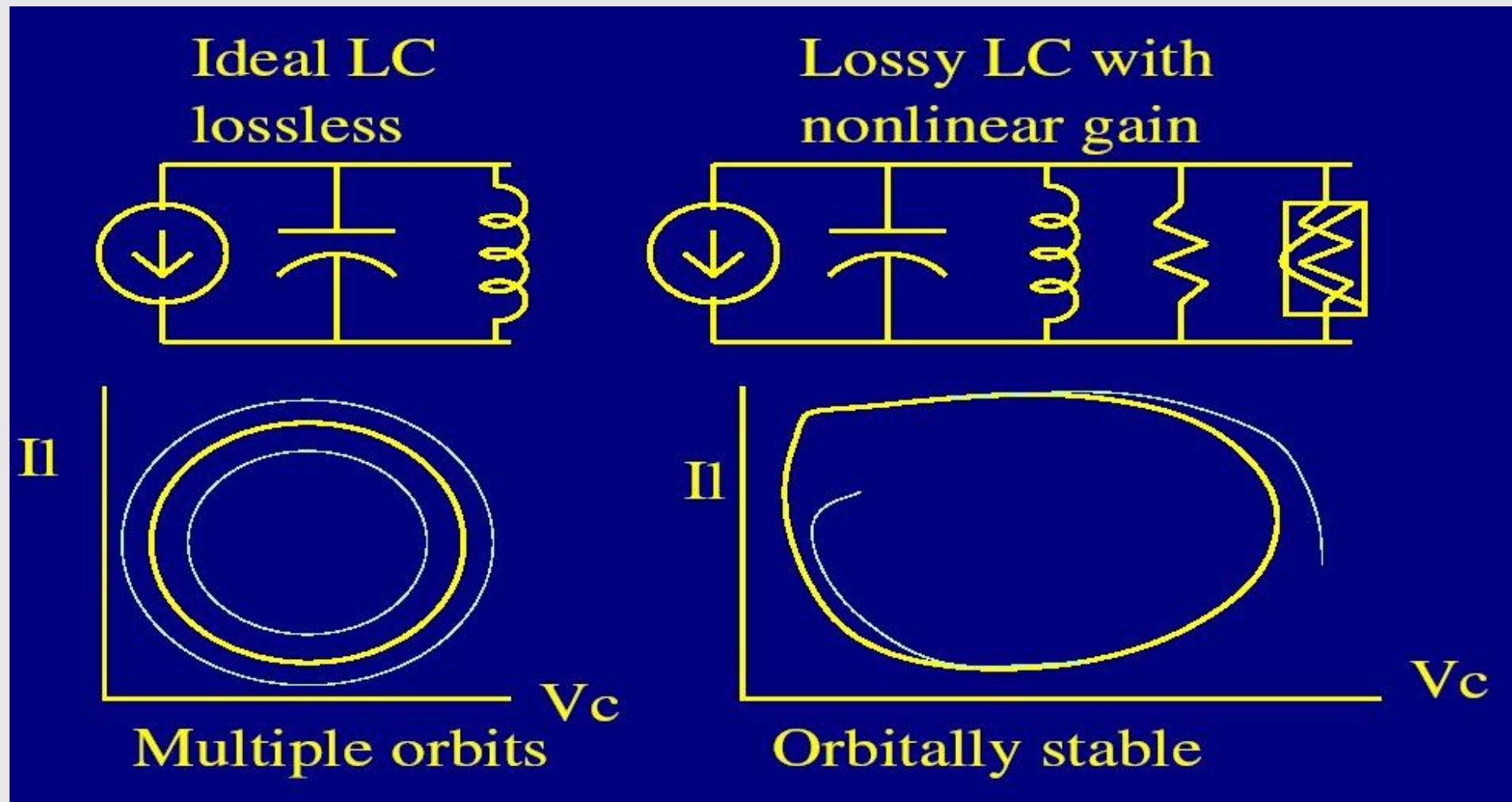
# Feature Comparison with Existing Methods

|                            | LTI       | LPTV      | Our approach |
|----------------------------|-----------|-----------|--------------|
| Jitter from white noise    | ✗         | ✓ ✗ ⓘ     | ✓            |
| Flicker/coloured jitter    | ✗         | ?         | ✓            |
| Supply interference jitter | ✗         | ✗ ✓ ⓘ     | ✓            |
| VCO frequency control      | ✓ ✗ ⓘ     | ✓ ⓘ       | ✓            |
| Injection locking          | ✗         | ✗         | ✓            |
| PLL lock/capture           | ✓ ⓘ       | ✓ ⓘ       | ✓            |
| Cycle slipping             | ✗ ⓘ       | ?         | ✓            |
| Amplitude effects          | NA        | NA        | ✓            |
|                            |           |           |              |
| Model generation speed     | Poor ⓘ    | Poor      | Excellent    |
| Model gen. robustness      | Poor      | Mediocre  | Good ⓘ       |
| Model simulation speed     | Excellent | Excellent | Excellent    |

# Phase Plane view of Oscillator Operation

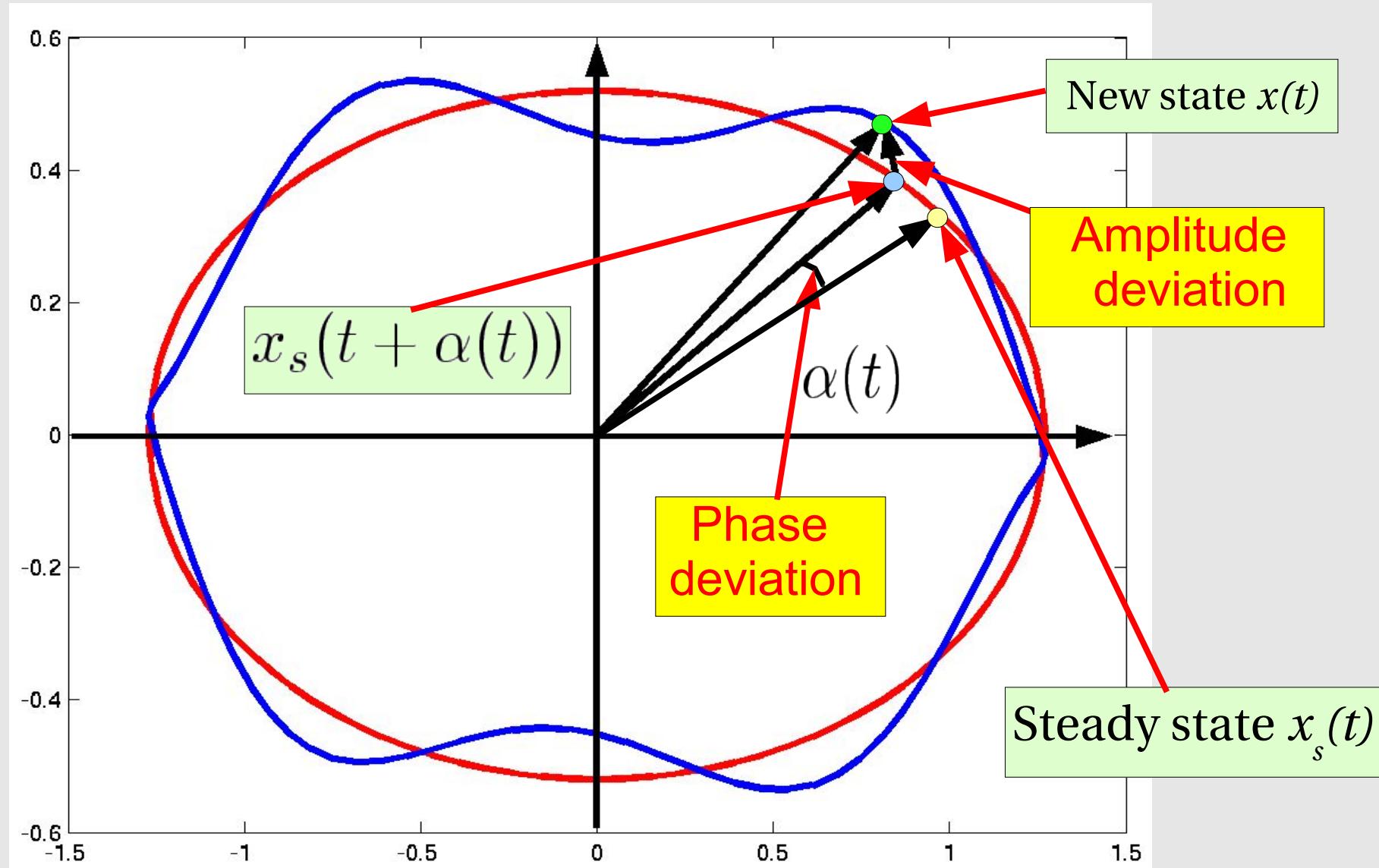


# “Ideal” vs Orbitally Stable Oscillators



Nonlinearity cannot be ignored – fundamental to oscillator operation

# Effect of Noise/Perturbation on Oscillator



# Extracting the Phase Deviation

Nonlinear scalar equation (macromodel)

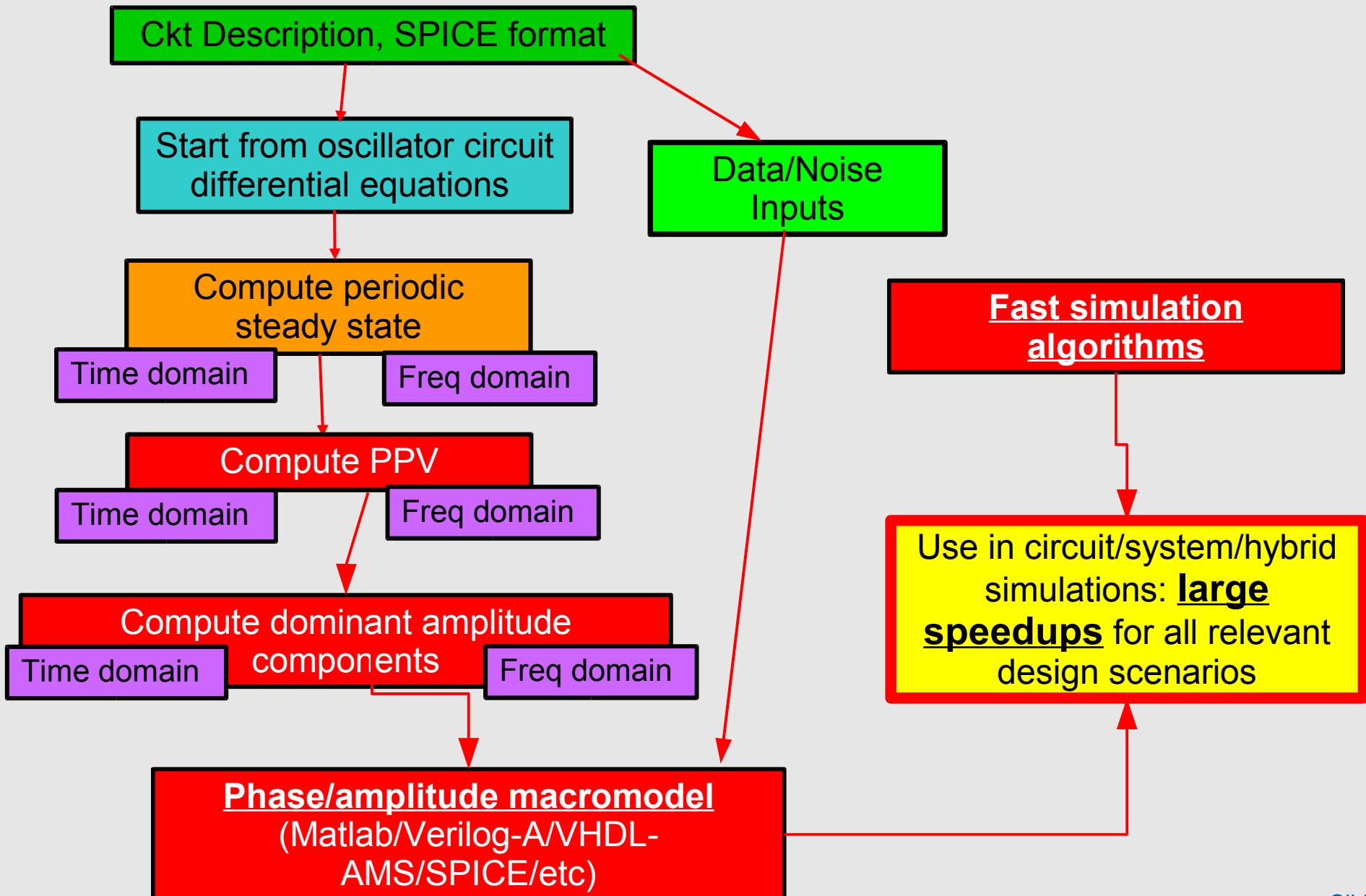
$$\dot{\alpha}(t) = v_1^T(t + \alpha(t)) \cdot b(t)$$

Phase error/jitter

Perturbation  
Projection Vector  
(PPV/NISF)

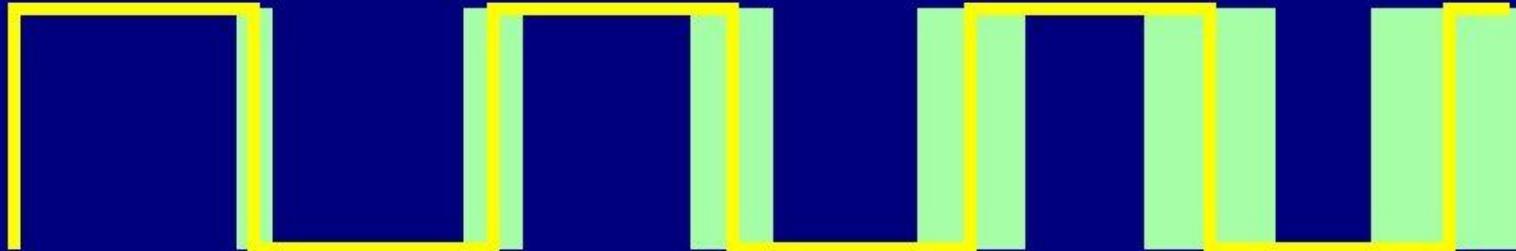
Noise “Input”

# Nonlinear Macromodel Extraction and Simulation Flow

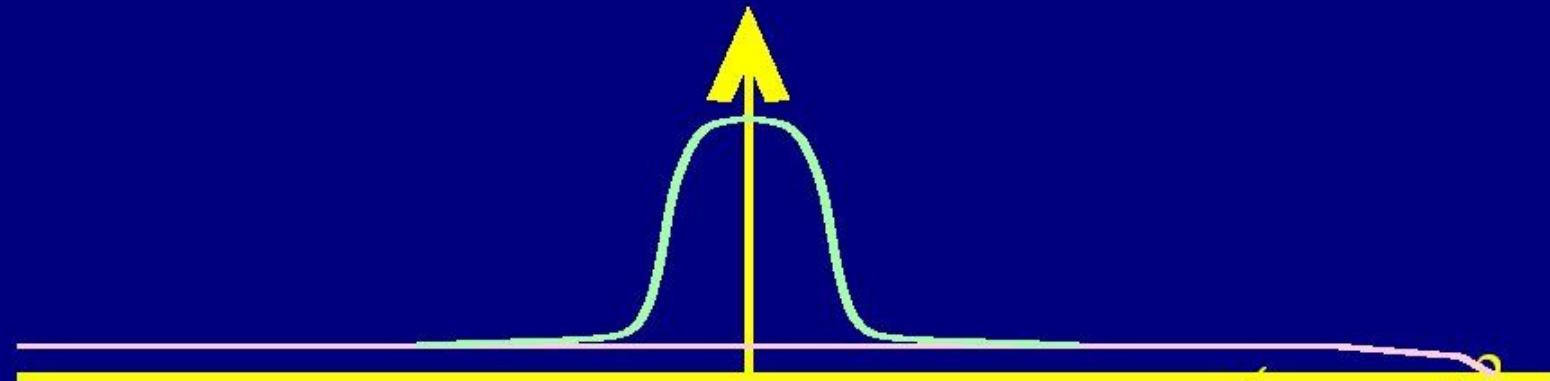


# Oscillators: Stochastic Phase Noise and Jitter

# Oscillator Phase Noise/Jitter

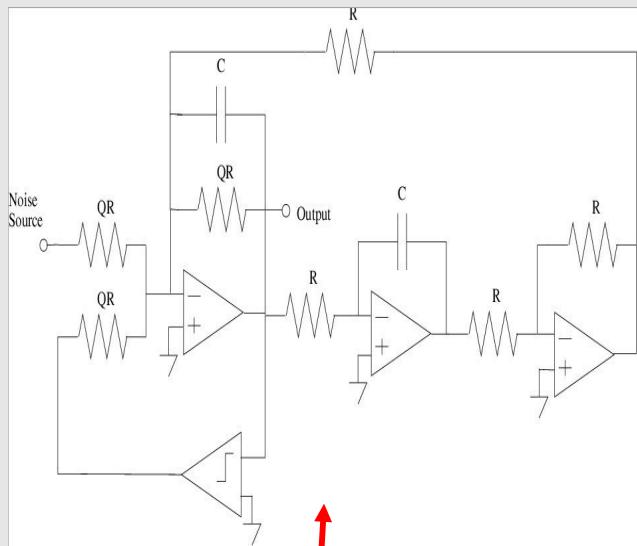


■ Timing jitter variance (per cycle) =  $cT$



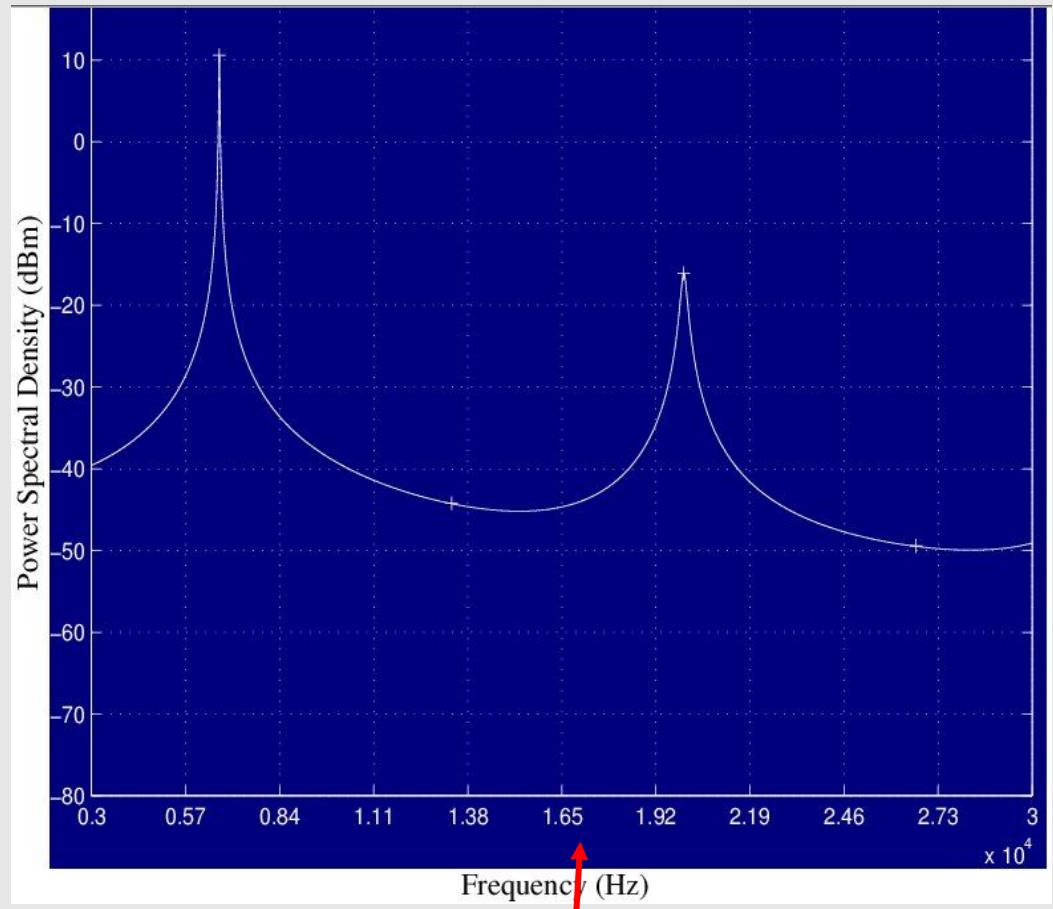
■ *Lorenzian spectrum:*  $\mathcal{L}(f_m) = 10 \log_{10} \left( \frac{f_0^2 c}{\pi^2 f_0^4 c^2 + f_m^2} \right)$

# Oscillator Phase Noise Spectrum



**Tow-Thomas  
oscillator**

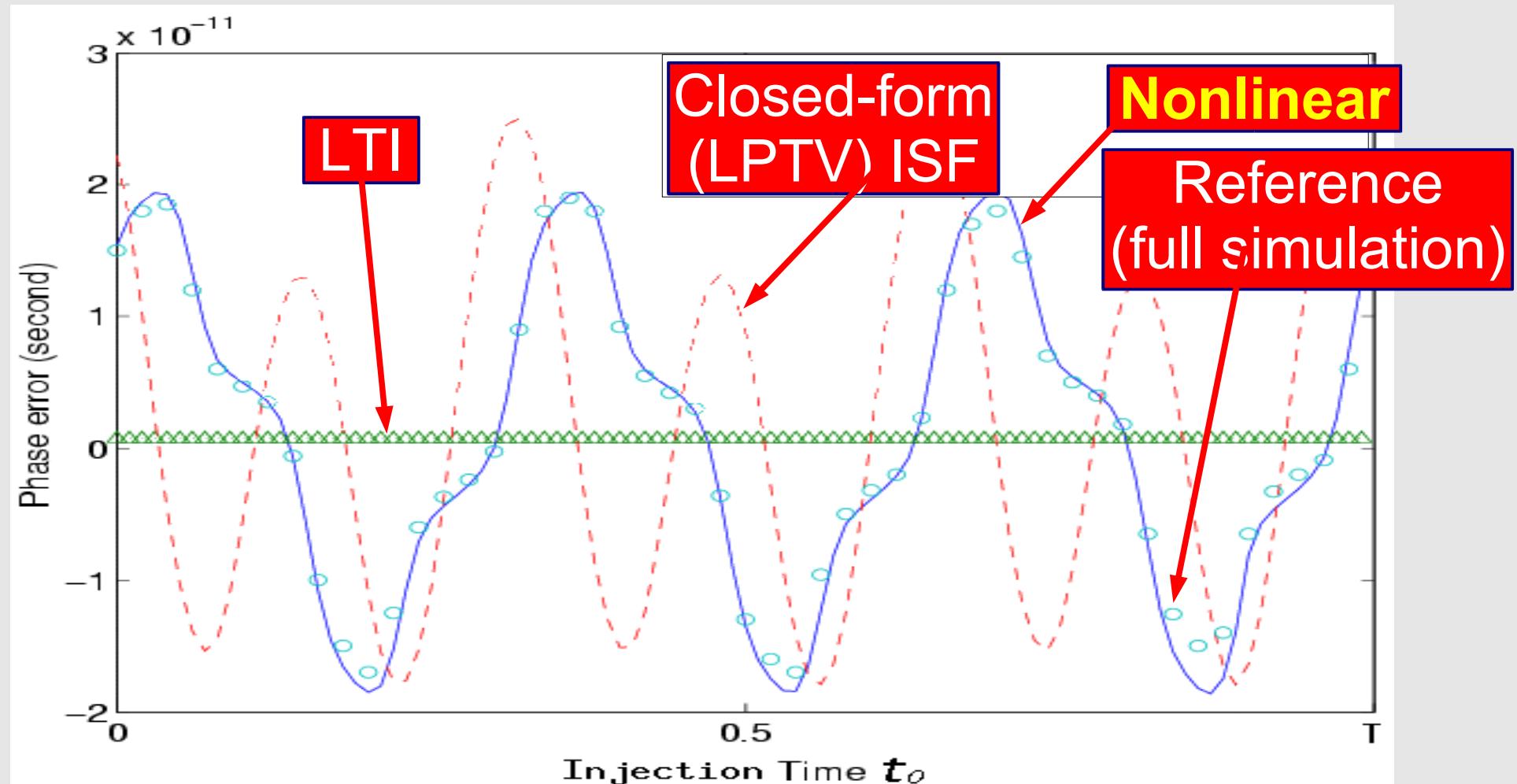
[Toth TCAS-1 1992]



**Phase noise  
spectrum**

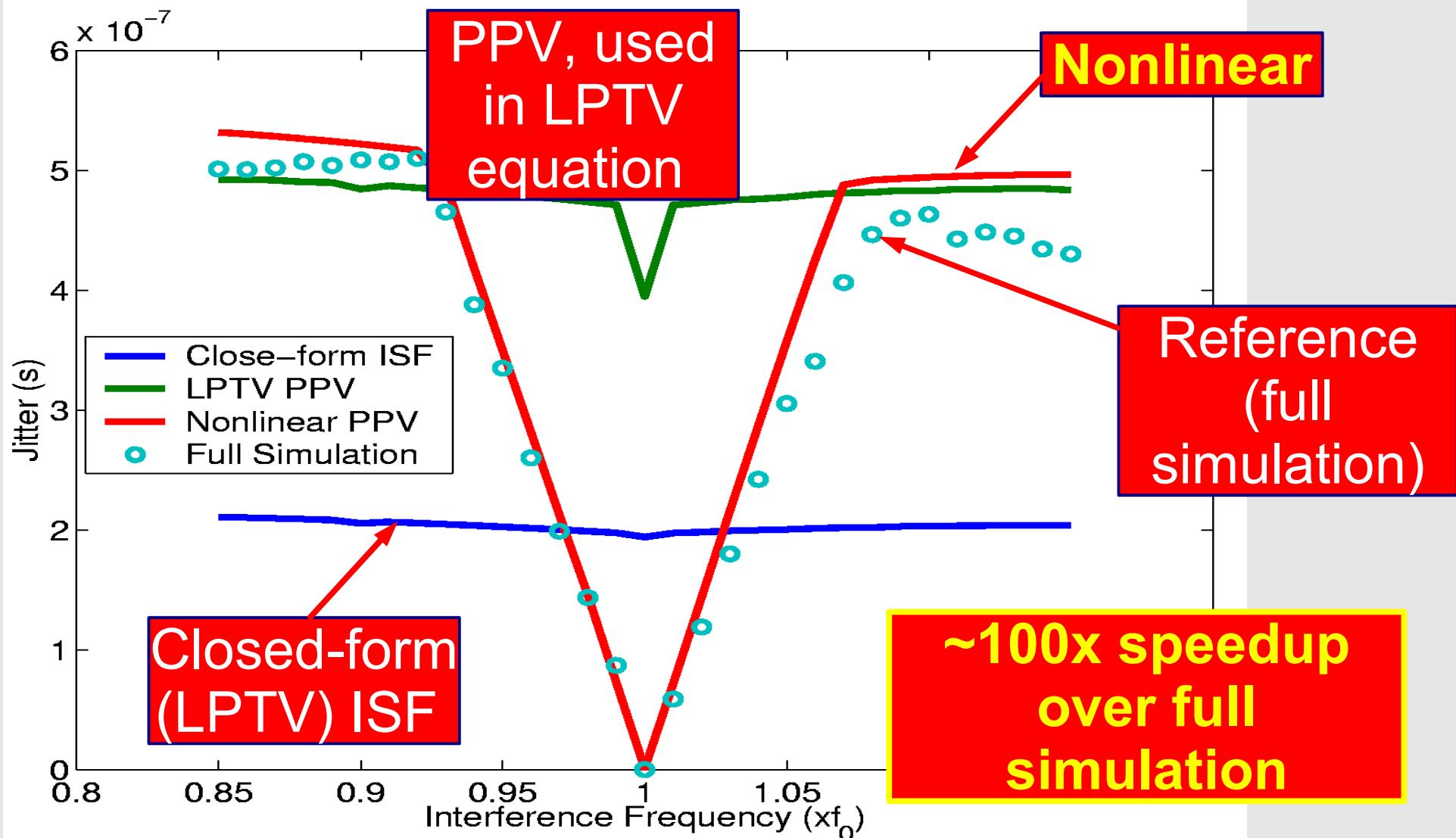
# Oscillator and PLL jitter due to Supply Interference

# Ring Oscillator: Jitter due to Momentary Impulses at Different Shifts

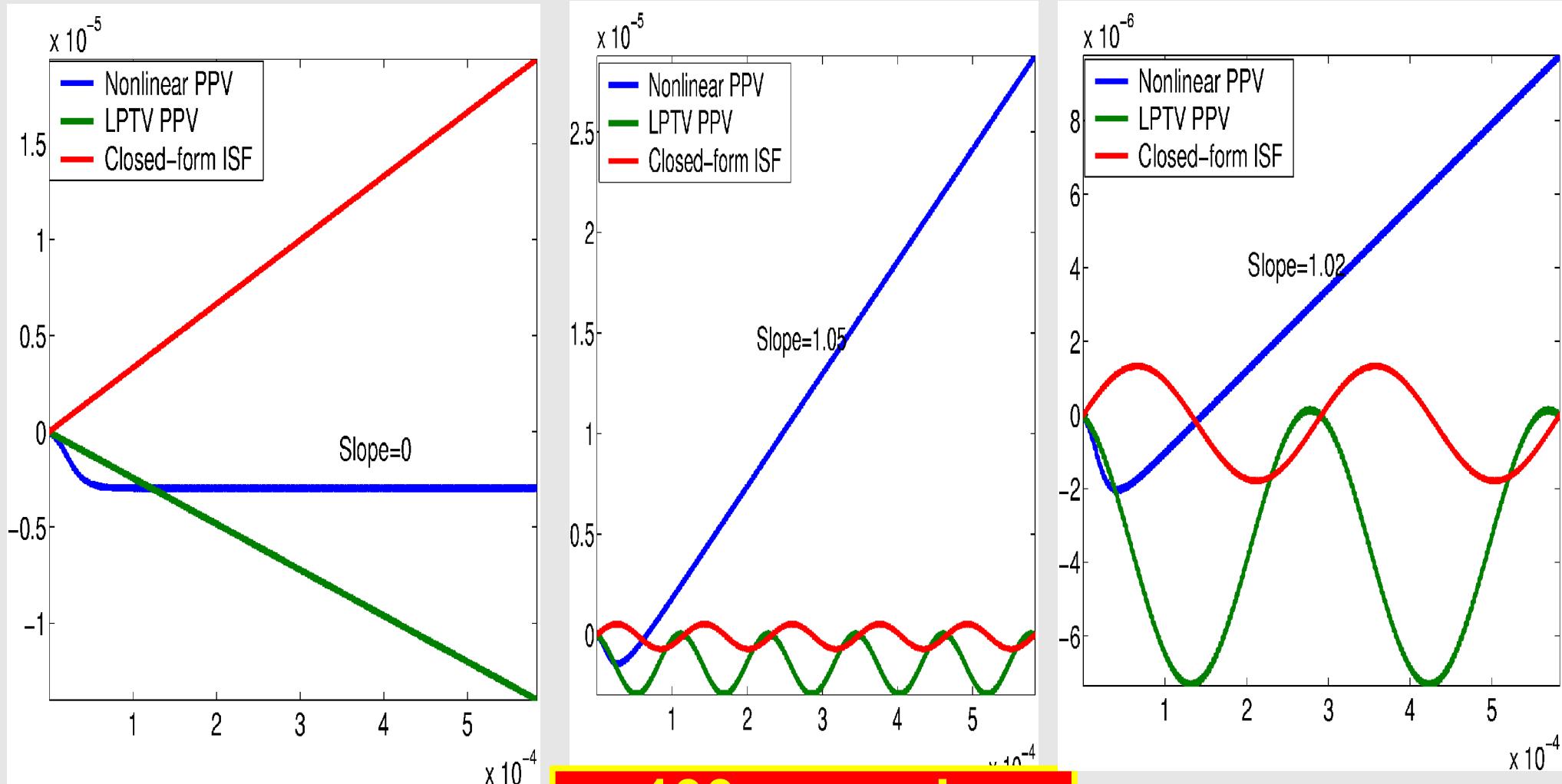


**~100x speedup over full simulation**

# Ring Oscillator: Per-cycle jitter as a function of sinusoidal supply interference frequency



# Ring Oscillator: Jitter due to Sinusoidal Interference Noise

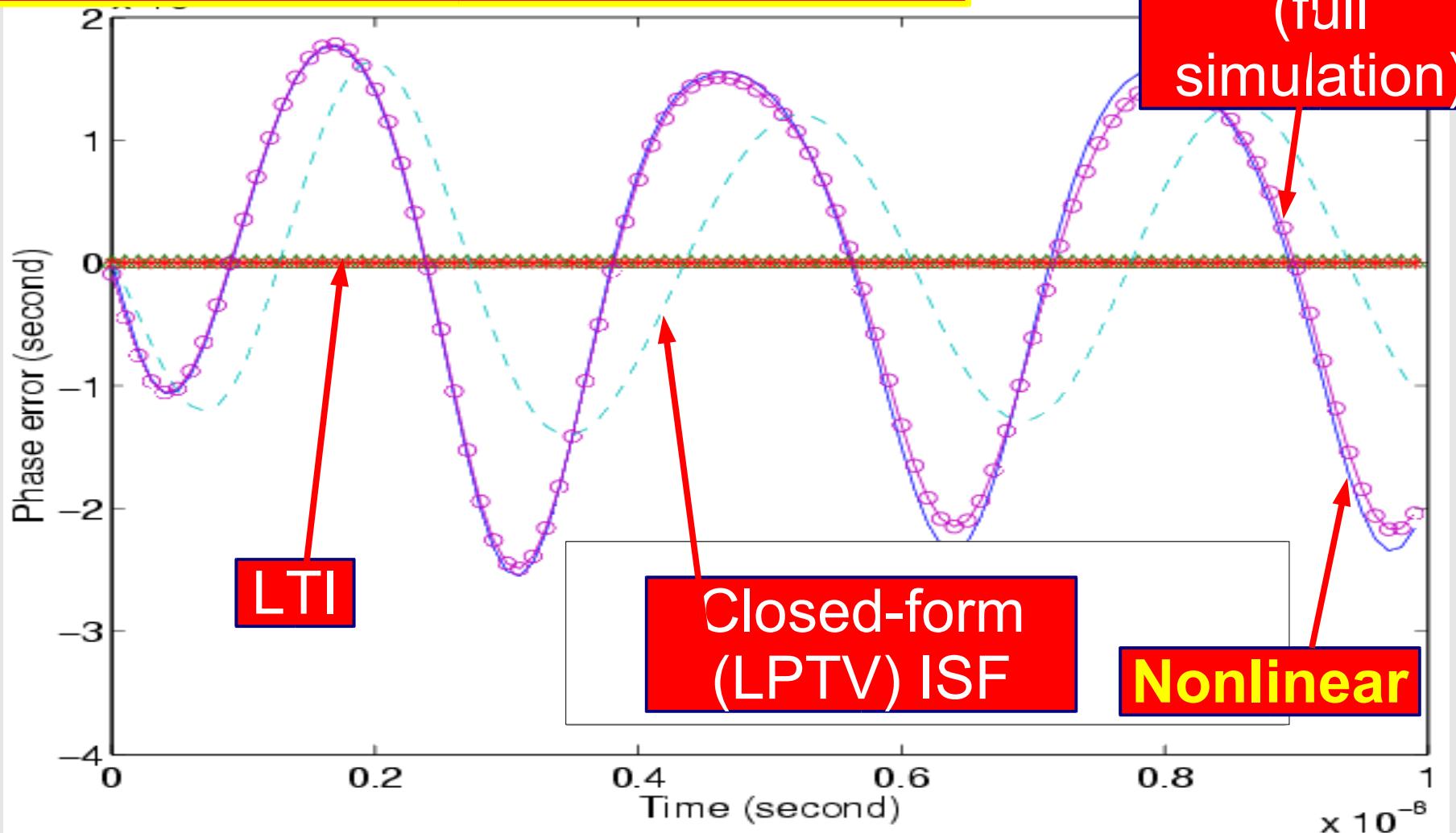


**~100x speedup  
over full  
simulation**

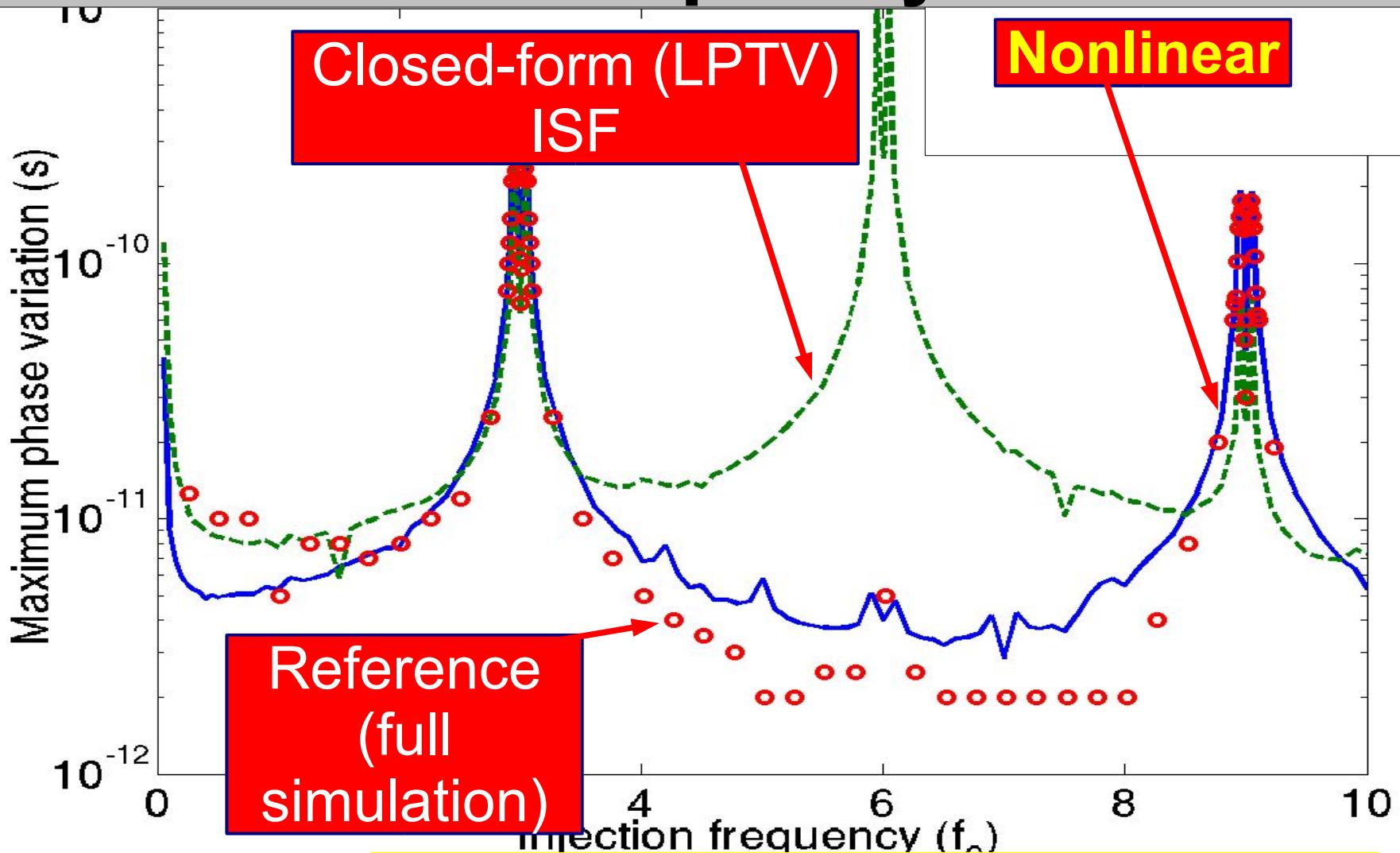
# PLL: Jitter due to Sinusoidal Interference

>1000x speedup over full simulation

Reference  
(full simulation)



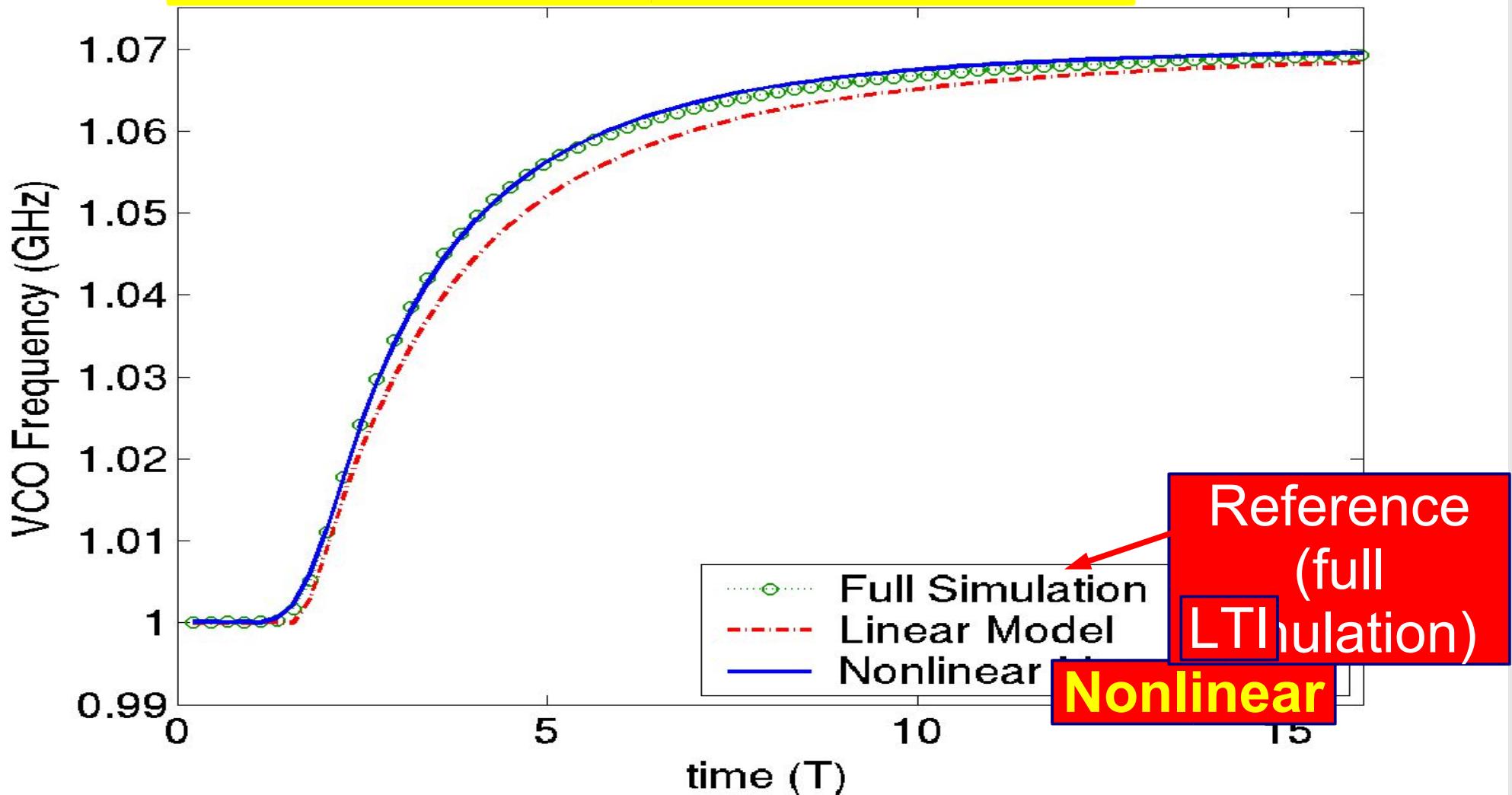
# PLL: Max jitter as a function of sinusoidal supply interference frequency



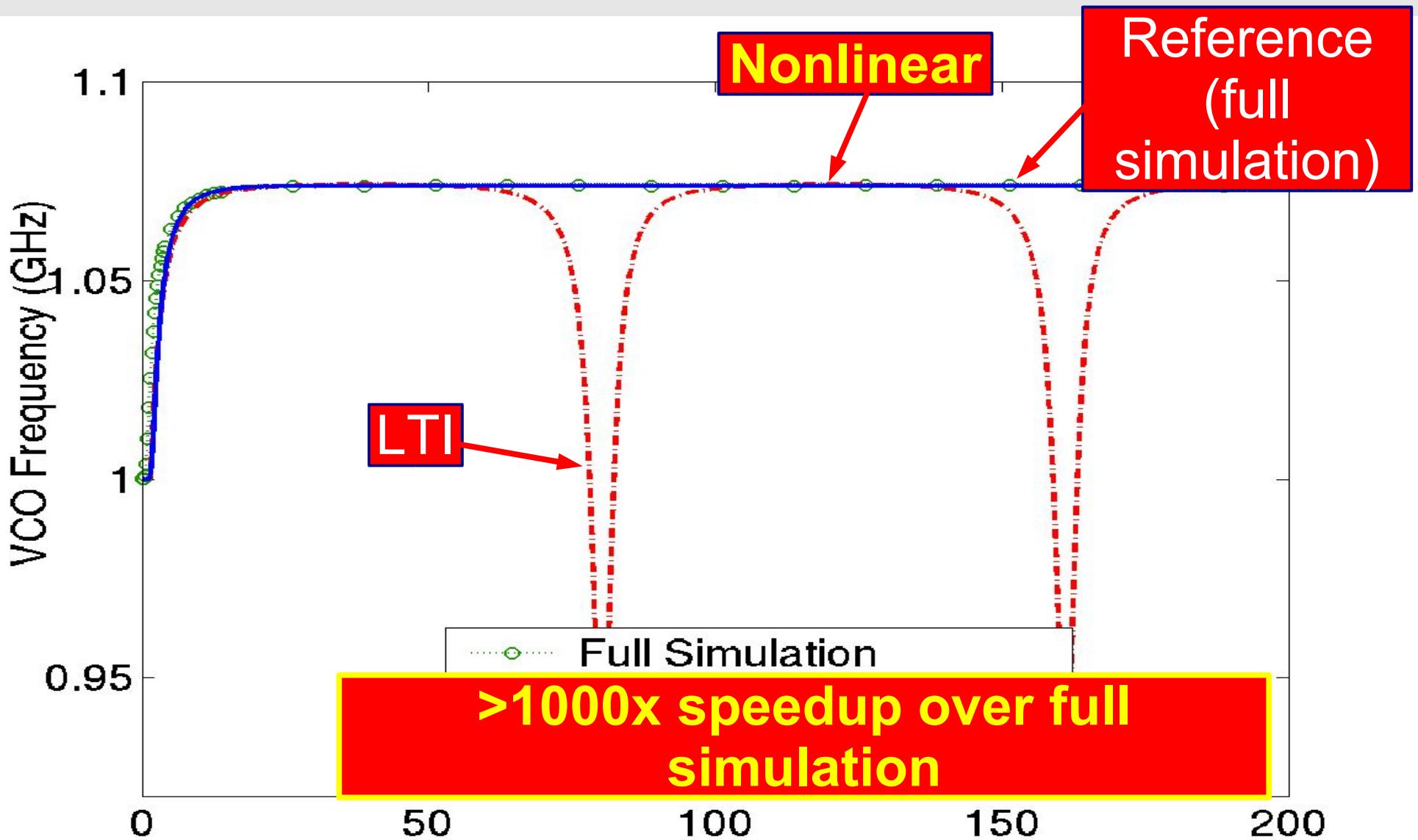
# **PLL Capture and Lock Transients**

# PLL Capture/Lock: $f_{ref}=1.07f_0$

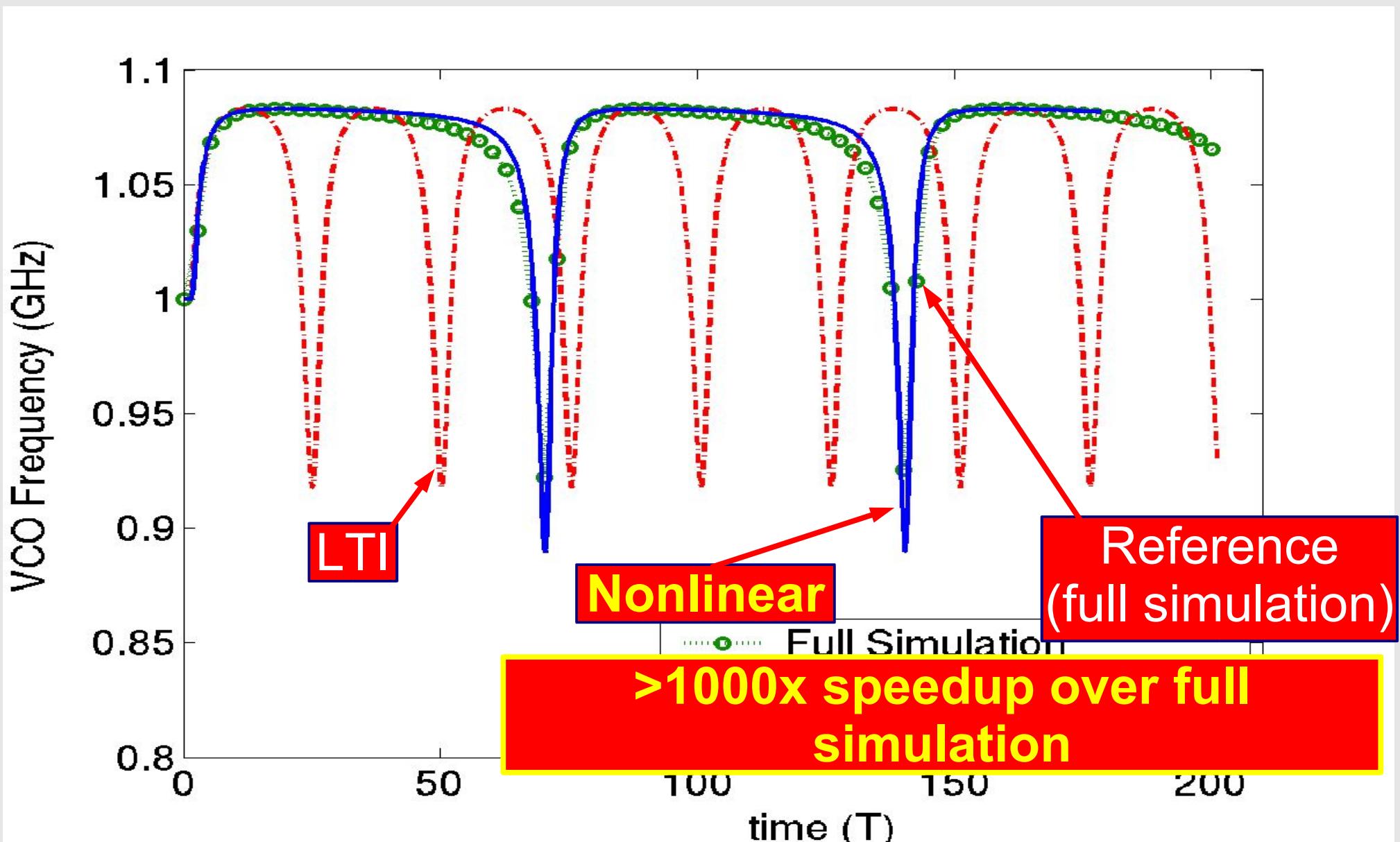
>1000x speedup over full simulation



# PLL Capture/Lock: $f_{ref} = 1.074 f_0$

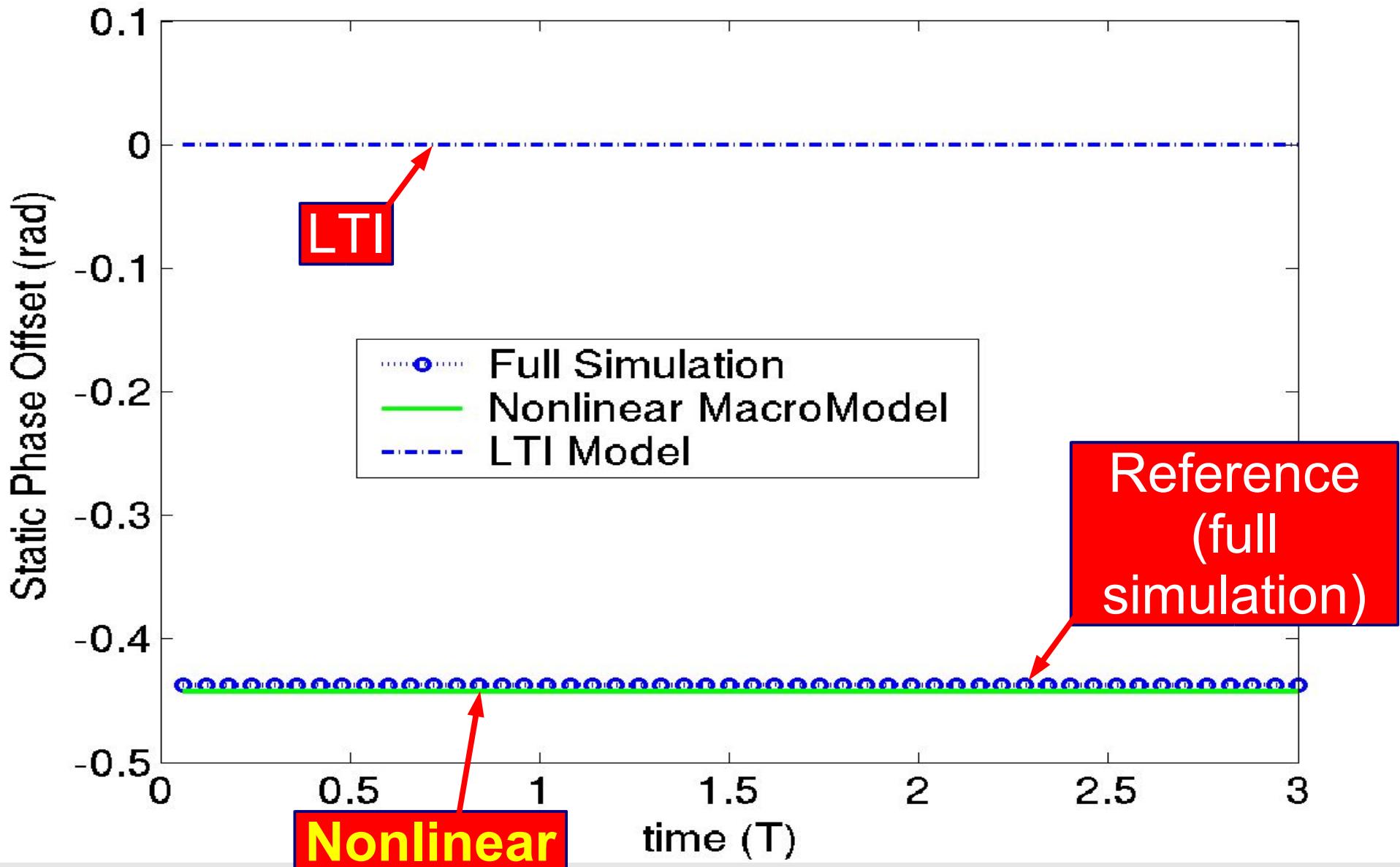


# PLL Capture/Lock: $f_{ref} = 1.083 f_0$

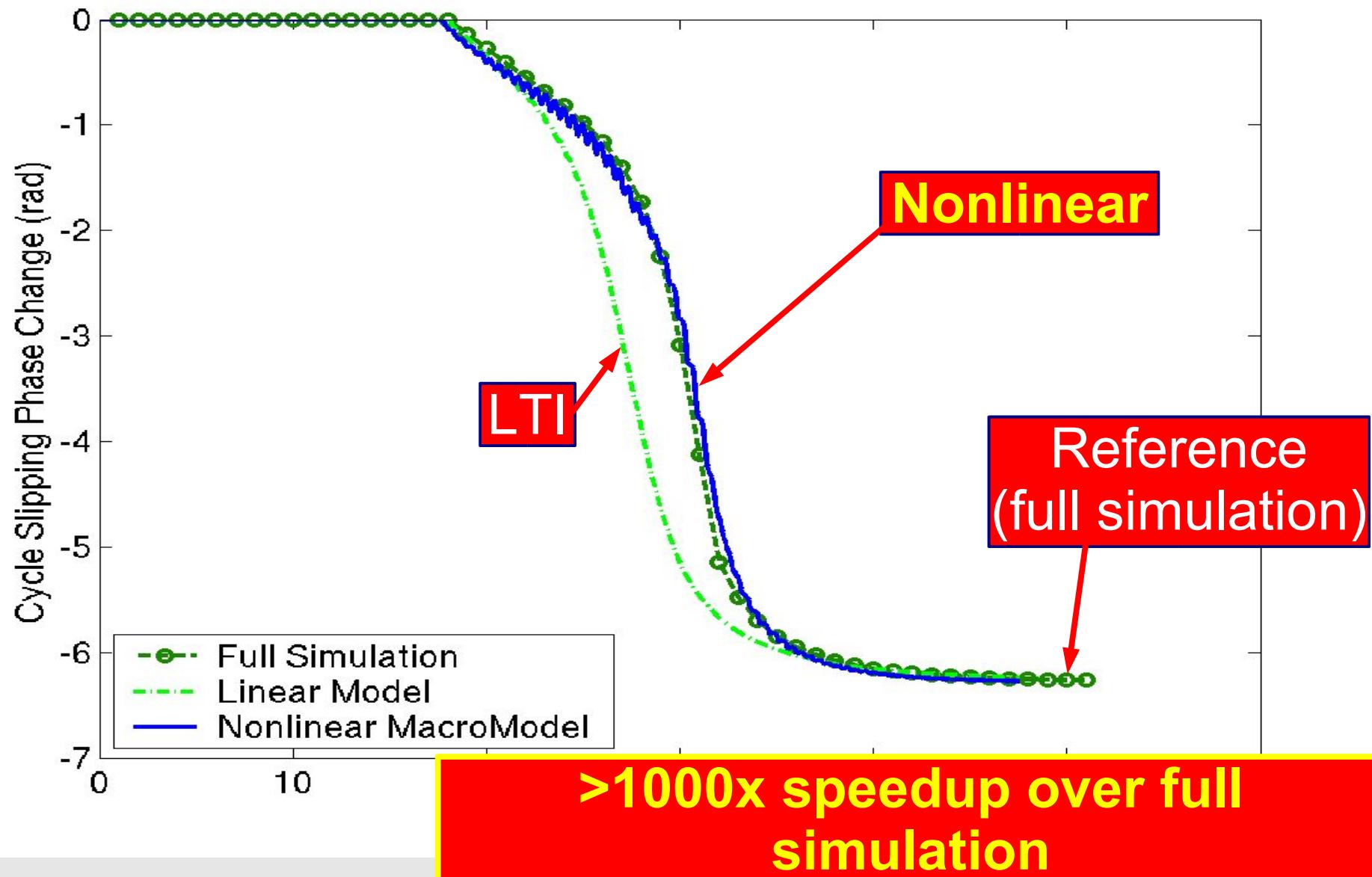


# **PLL Cycle Slipping**

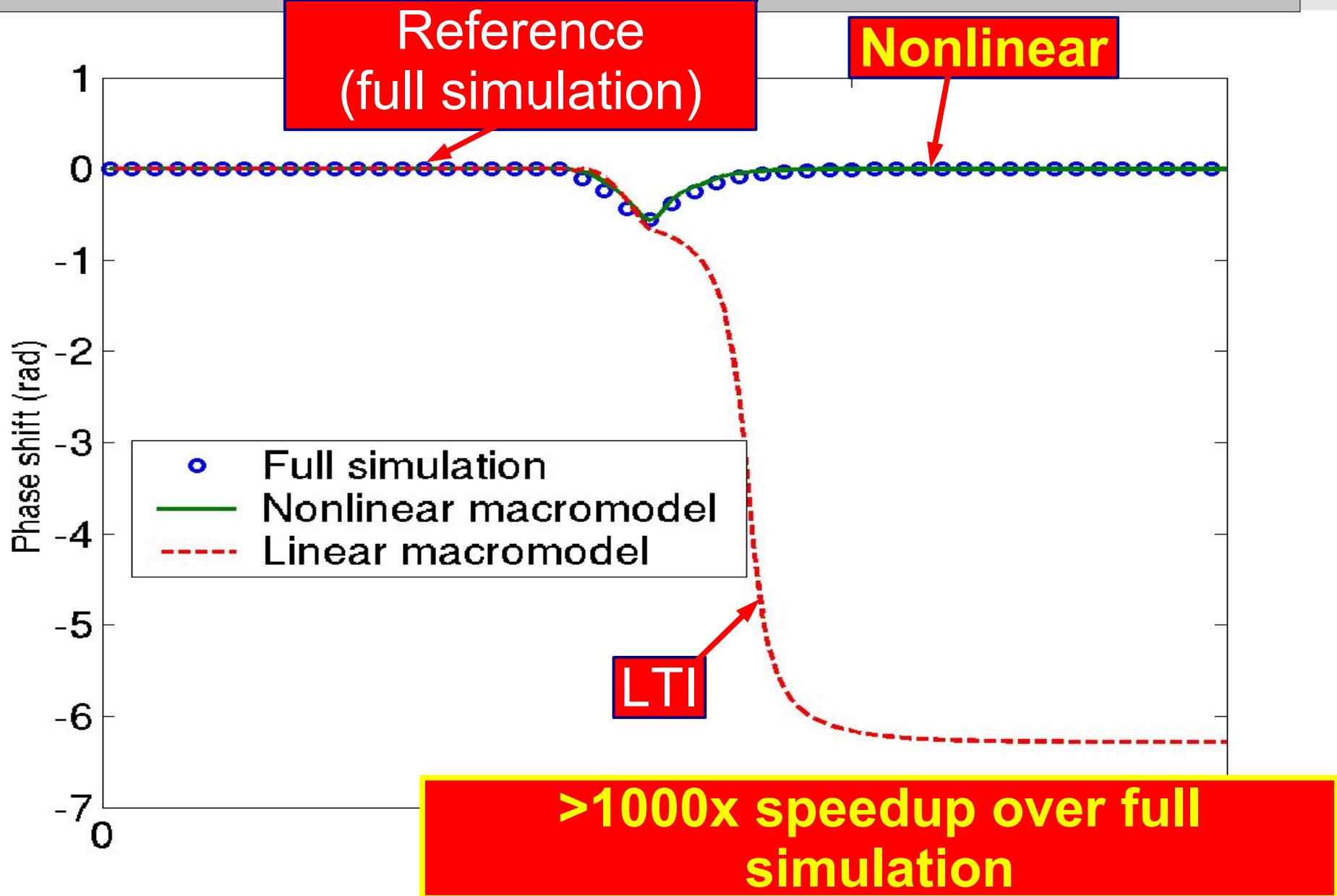
# PLL: static offset in lock



# PLL: cycle slipping (5mA, 10T shock)

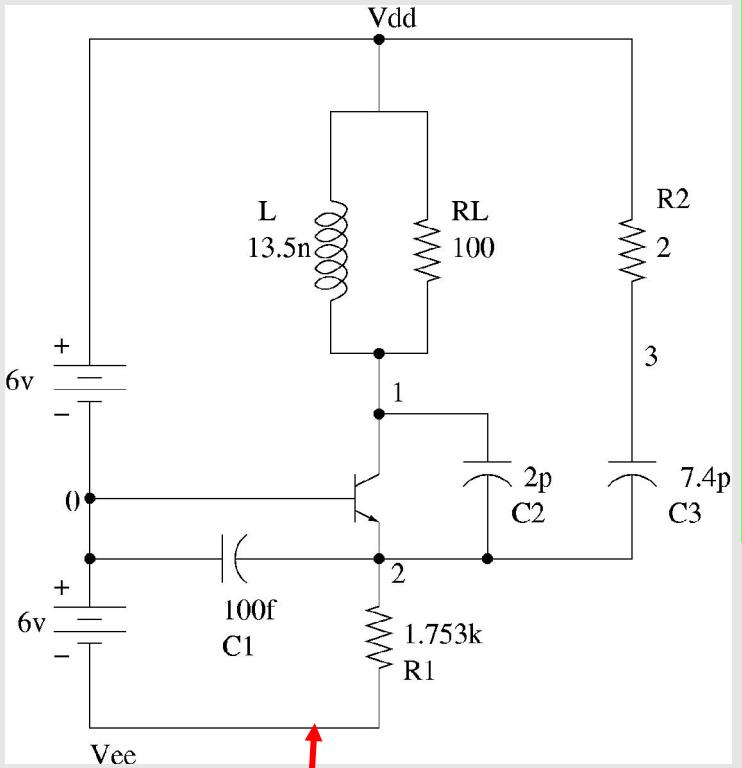


# PLL: cycle slipping (3mA, 10T shock)



# Injection Locking

# Colpitts Oscillator: Injection Locking

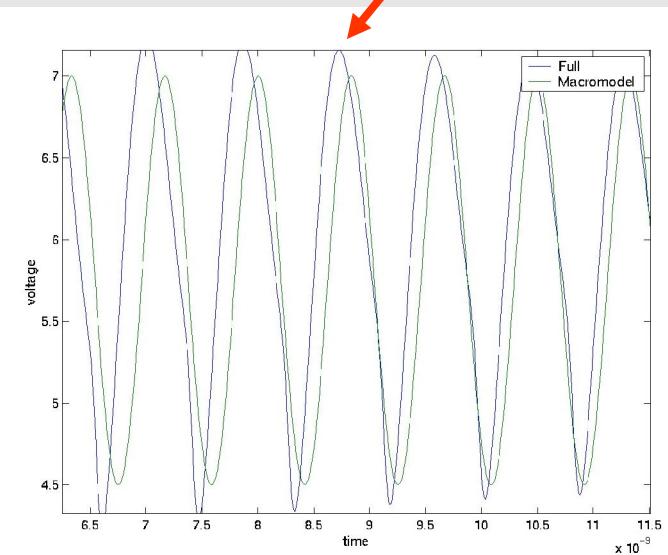
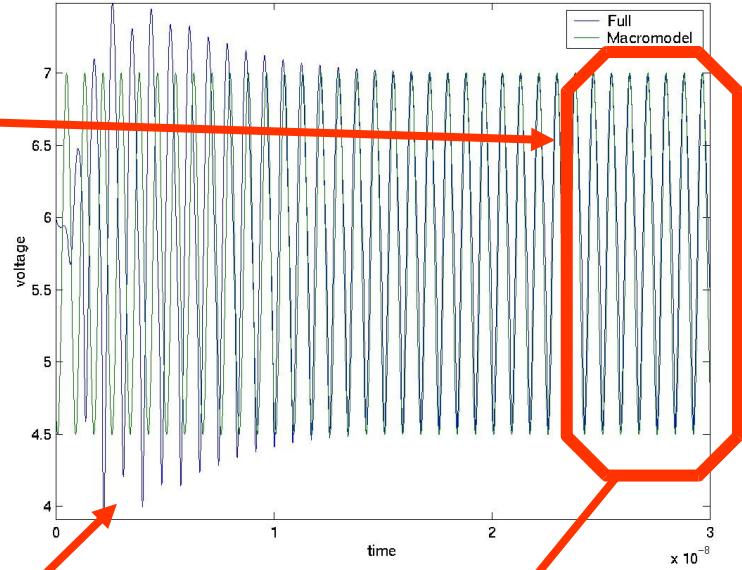


Colpitts oscillator

Nonlinear macromodel  
reproduces  
injection  
locking well  
(linear approaches cannot)

Full simulation vs macromodel

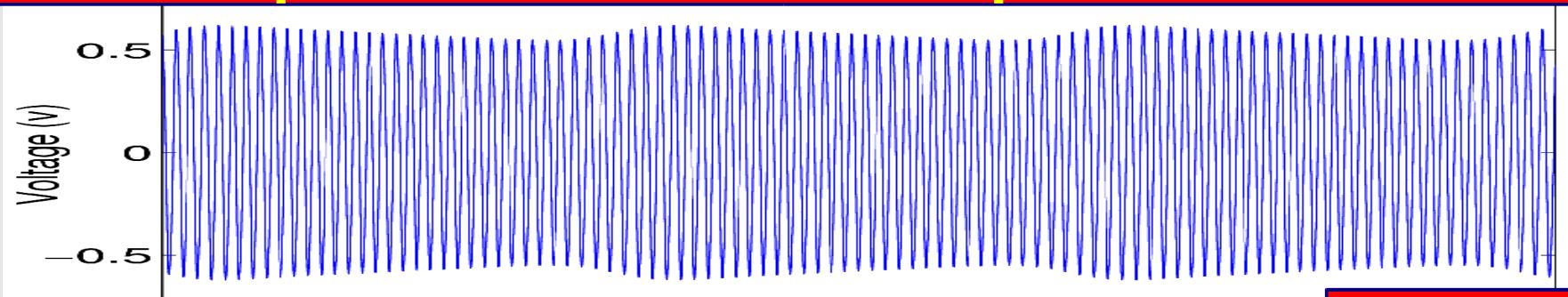
89x speedup over full simulation



# **Capturing slow amplitude modes**

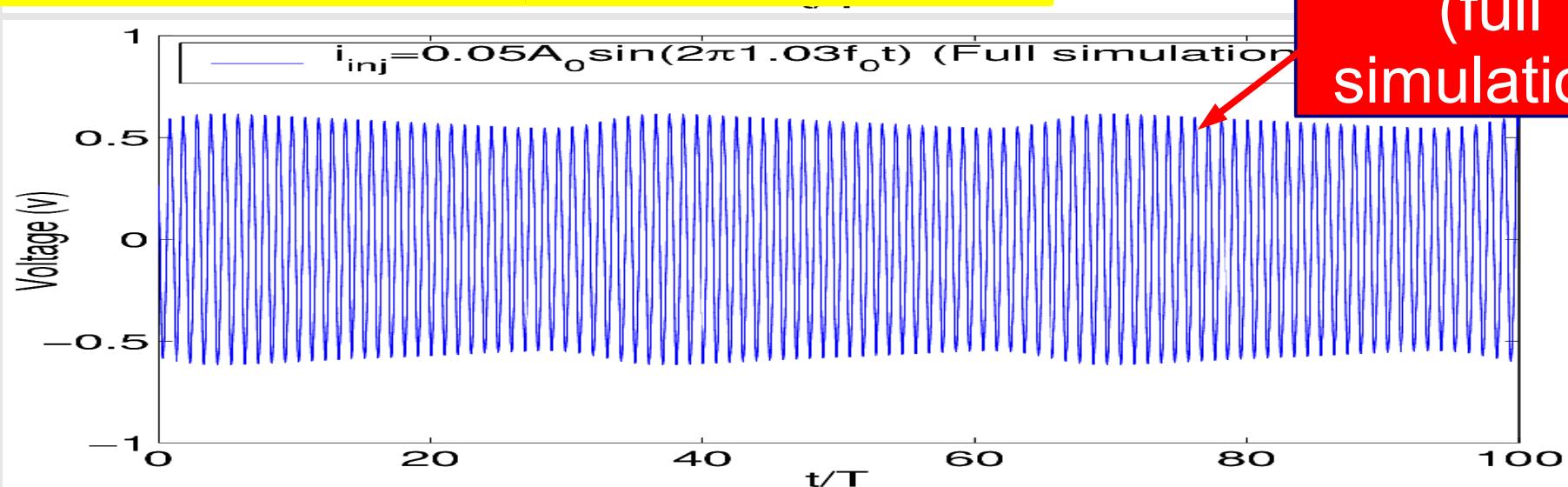
# Colpitts Oscillator: Reproducing slow amplitude (and phase) changes

Nonlinear phase + slow LPTV amplitude macromodel



~80x speedup over full simulation

Reference  
(full  
simulation)



# Conclusions

- Automatic macromodelling: an enabling technology
  - Interconnect reduction
  - Nonlinear system macromodelling
    - Op-amps, comparators
    - I/O drivers
    - oscillators/PLLs
- Further automated MM capabilities expected
  - research ongoing
  - maturing research transferring to industry

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