Macromodelling Digital Libraries for Substrate Noise Analysis

Jaijeet Roychowdhury

University of Minnesota

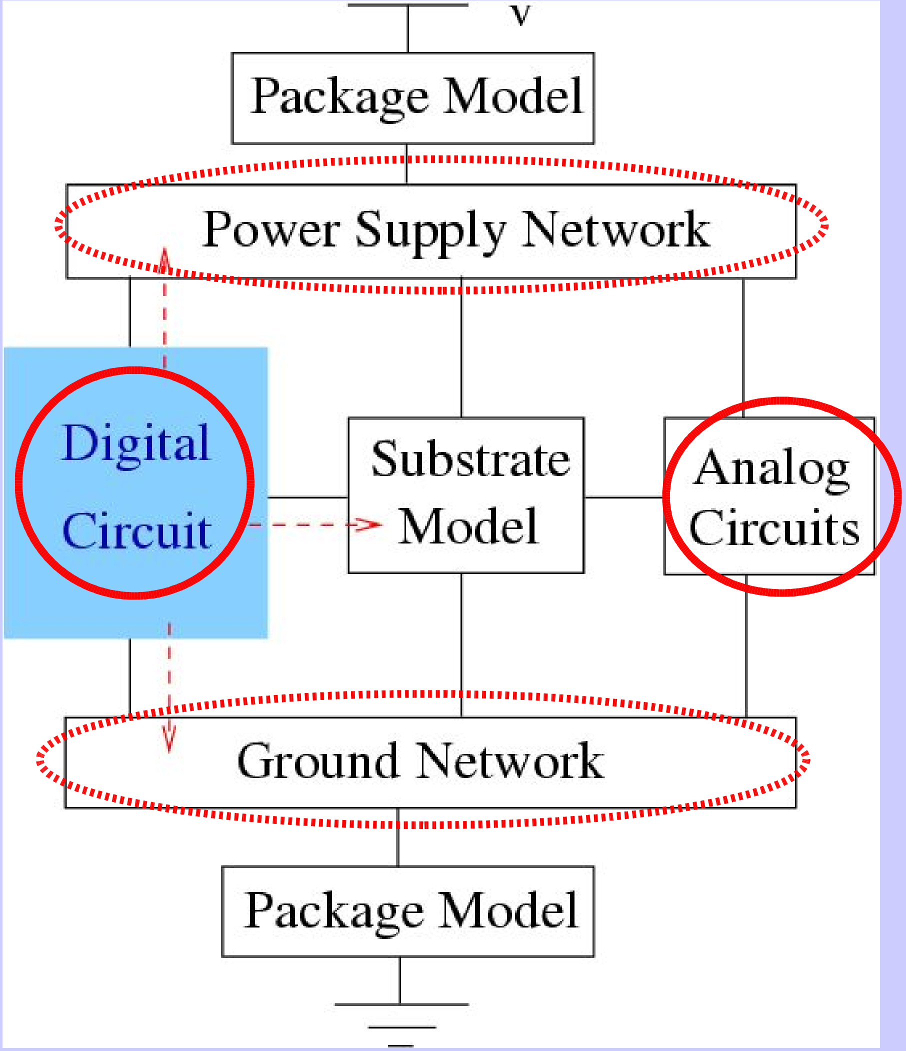
Latest slides downloadable from the web:

https://laoo.dtc.umn.edu/~jr/DATE05-tut.pdf

username: *ADAMIN* password: *date05tut*

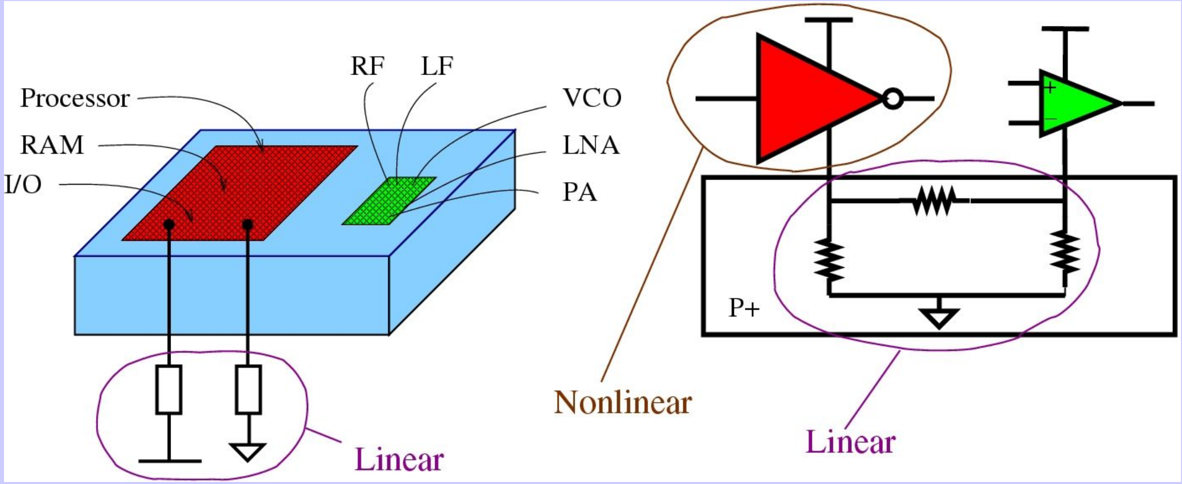
On-Chip Digital Switching Noise in SoCs

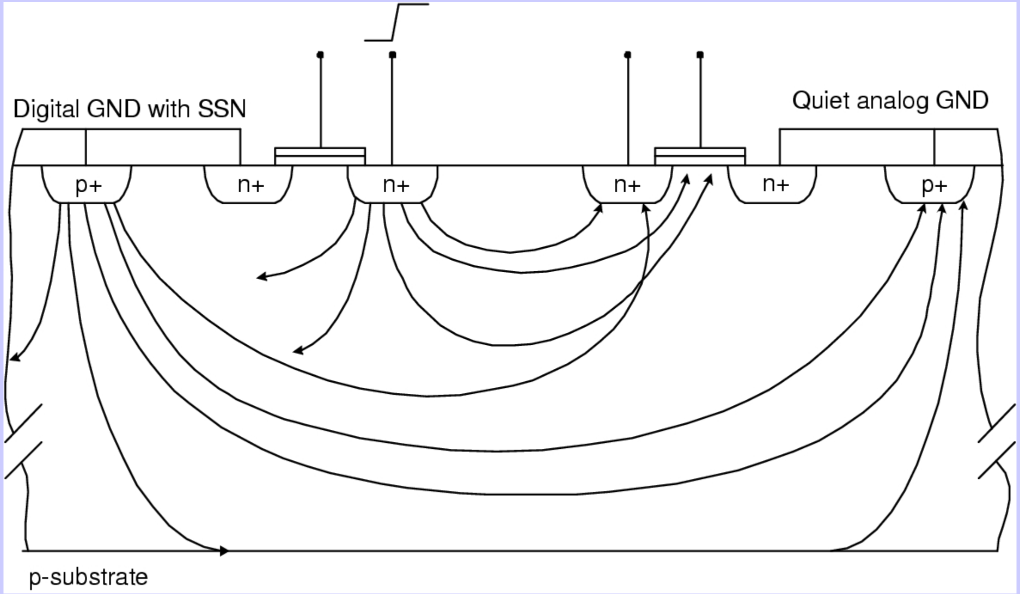
- Predicting substrate noise and supply noise generation by digital circuits accurately
- Substrate and supply noise: correlated
  - same generation mechanism
  - interaction between substrate and supply networks
- Predicting VCO and PLL performance degradation fast and accurately
- New methodology: **automated macromodelling**



Substrate/Supply Interference Noise Mechanisms

- Switching transients from digital “aggressors” inject current into bulk/substrate *and* into pwr/ground lines
  - noise travels long distances through distributed substrate
  - affects both digital and analog “victims”
  - substrate/supply “talk” to each other

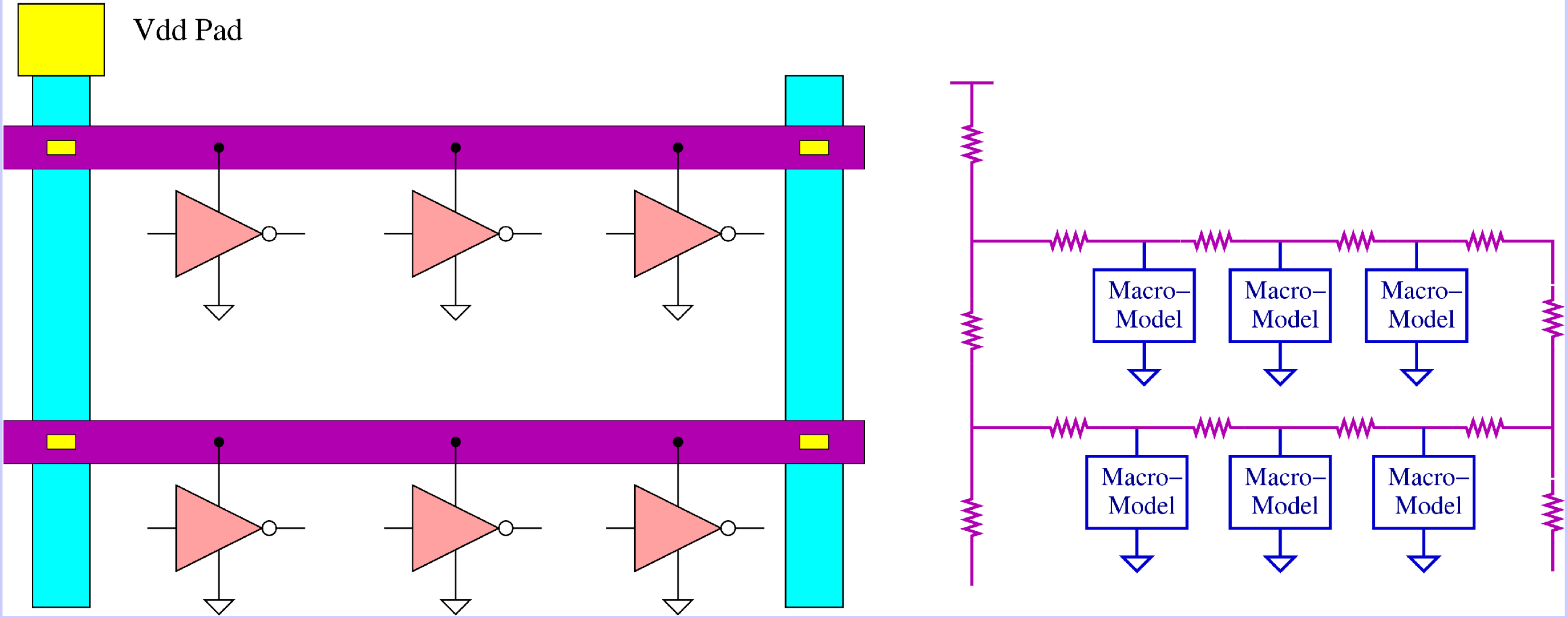




Predicting Interference Noise Quantitatively

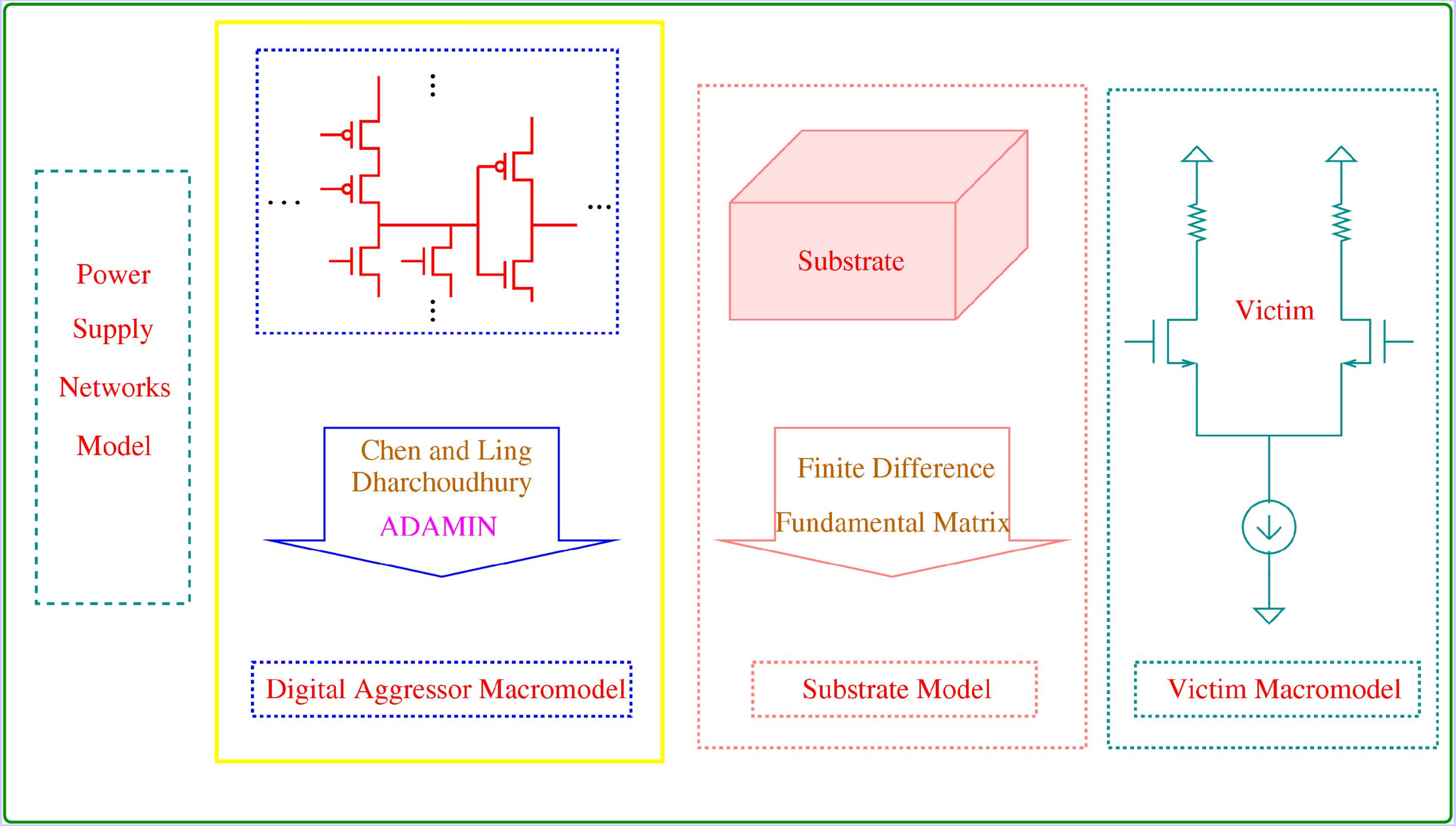
- Detailed circuit simulation with SPICE?
  - ✓ the accurate way
  - ✓ fully accounts for *nonlinear switching operation* of digital circuitry
  - ✗ but computationally infeasible: far too slow/expensive
- Millions/billions of MOSFETs today
  - Other approaches needed

Taming Complexity by Using Macromodels

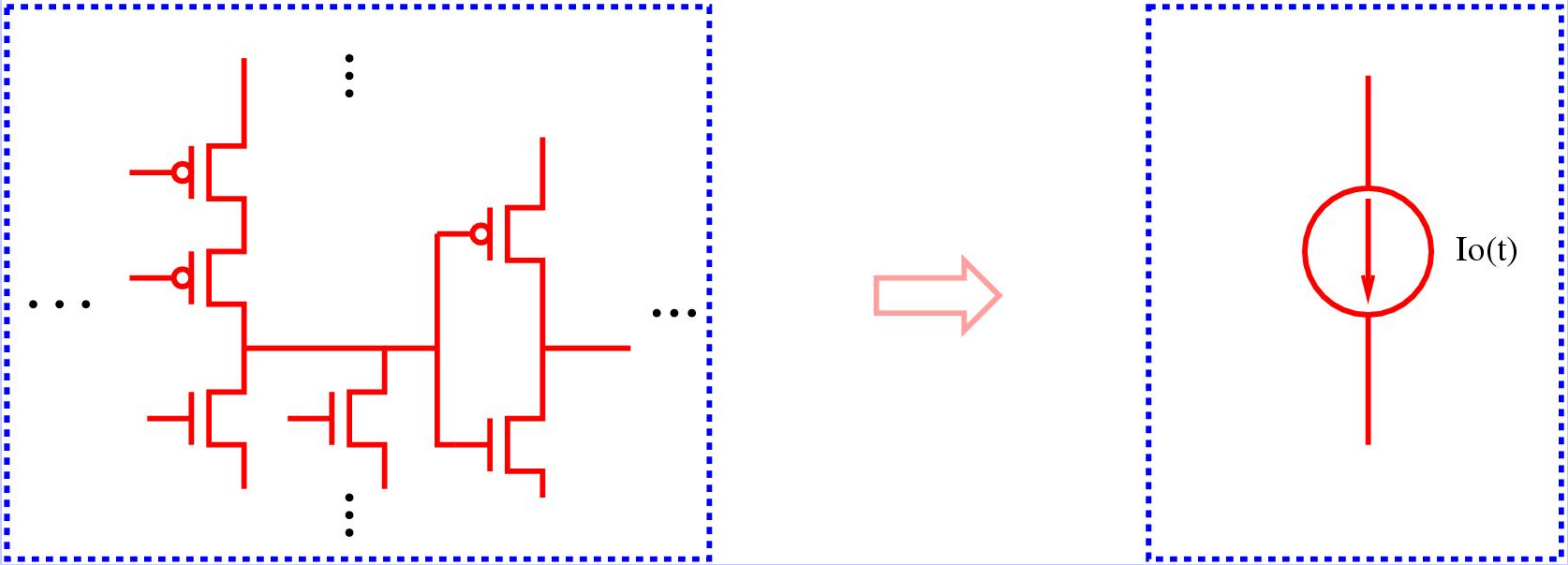


- Partition digital sections into blocks
  - 10s of thousands of gates each
- Use simple macromodels to replace each block
  - trade off some accuracy for computational speed
- Extract parasitics of power supply, substrate networks
- Simulate equivalent system constructed with macromodels

Macromodel-based Interference Noise Prediction



Digital Noise Macromodels – Prior Approaches

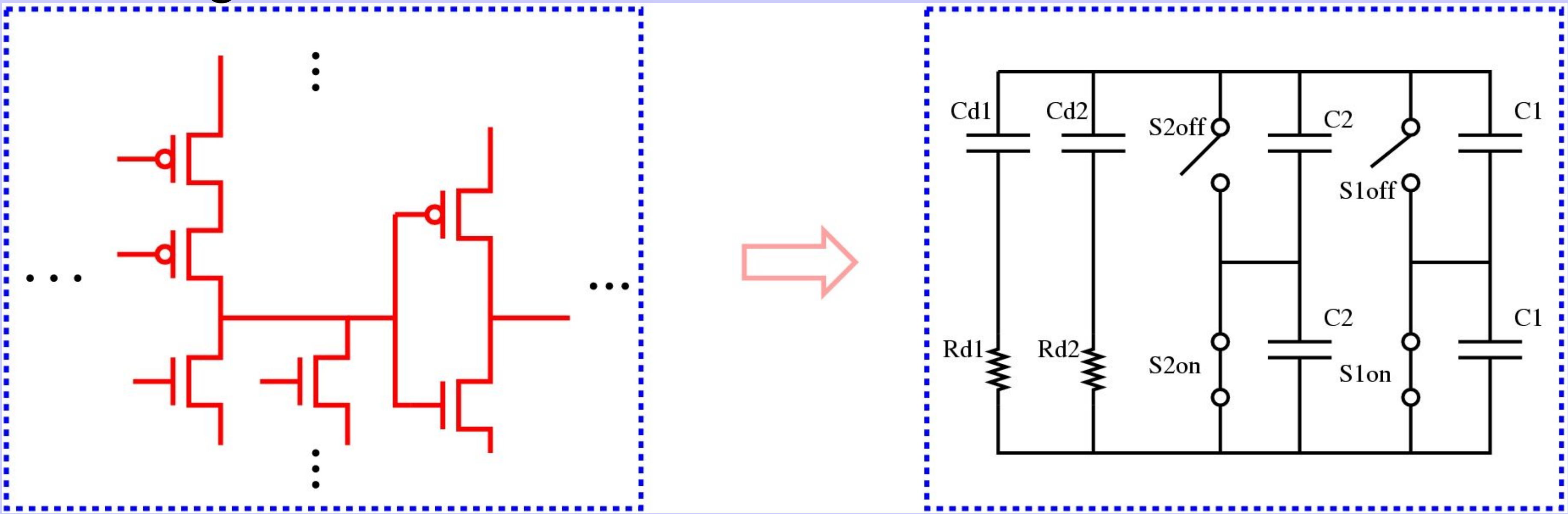


Dharchoudhury et al 98

- Digital blocks == current sources (from SPICE simulation)
  - ad-hoc: 10% to >100% errors in practice
  - Cannot respond to variations in substrate/supply networks
- Improvements: add resistive/capacitive elements
  - Nassif et al (IBM)
  - SWAN (IMEC)

Digital Noise Macromodels – Prior Approaches

Chen/Ling 97



- Replace MOS by ideal switches + resistors/capacitors
  - entire blocks replaced by small switched macromodel
- Elemental macromodel developed manually for each technology
  - ad-hoc collapsing of large clusters of switches

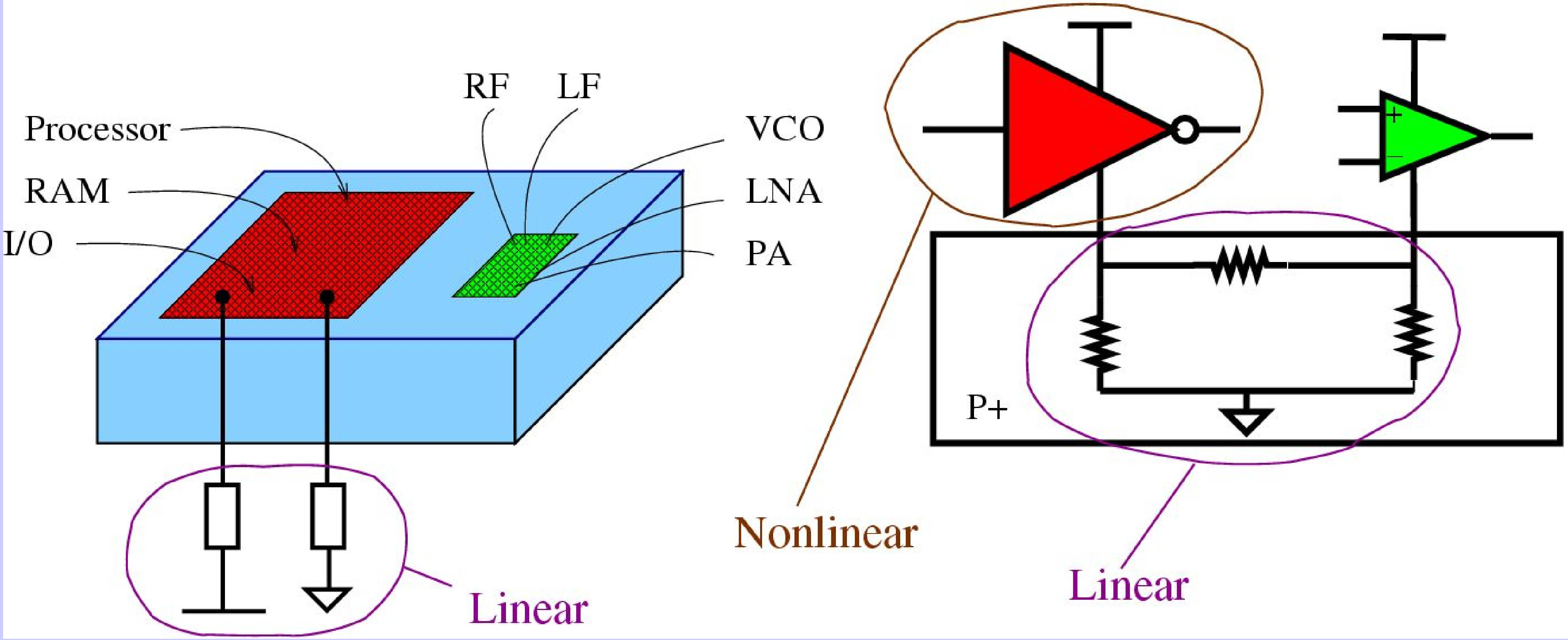
Push-Button Generation of Switching Models

- Dharchoudhury model very widely used
  - despite its known inaccuracy
  - key property: **convenience**
    - non-manual, easy to generate
- Automated, push-button generation is of key importance
- Switch-based models
  - recognize that switching activity is critical in noise generation
  - but limited in automated noise model “synthesis” capability
    - ad-hoc: no theory guaranteeing accuracy

ADAMIN: Automated Digital Aggressor Macromodelling for Interference Noise

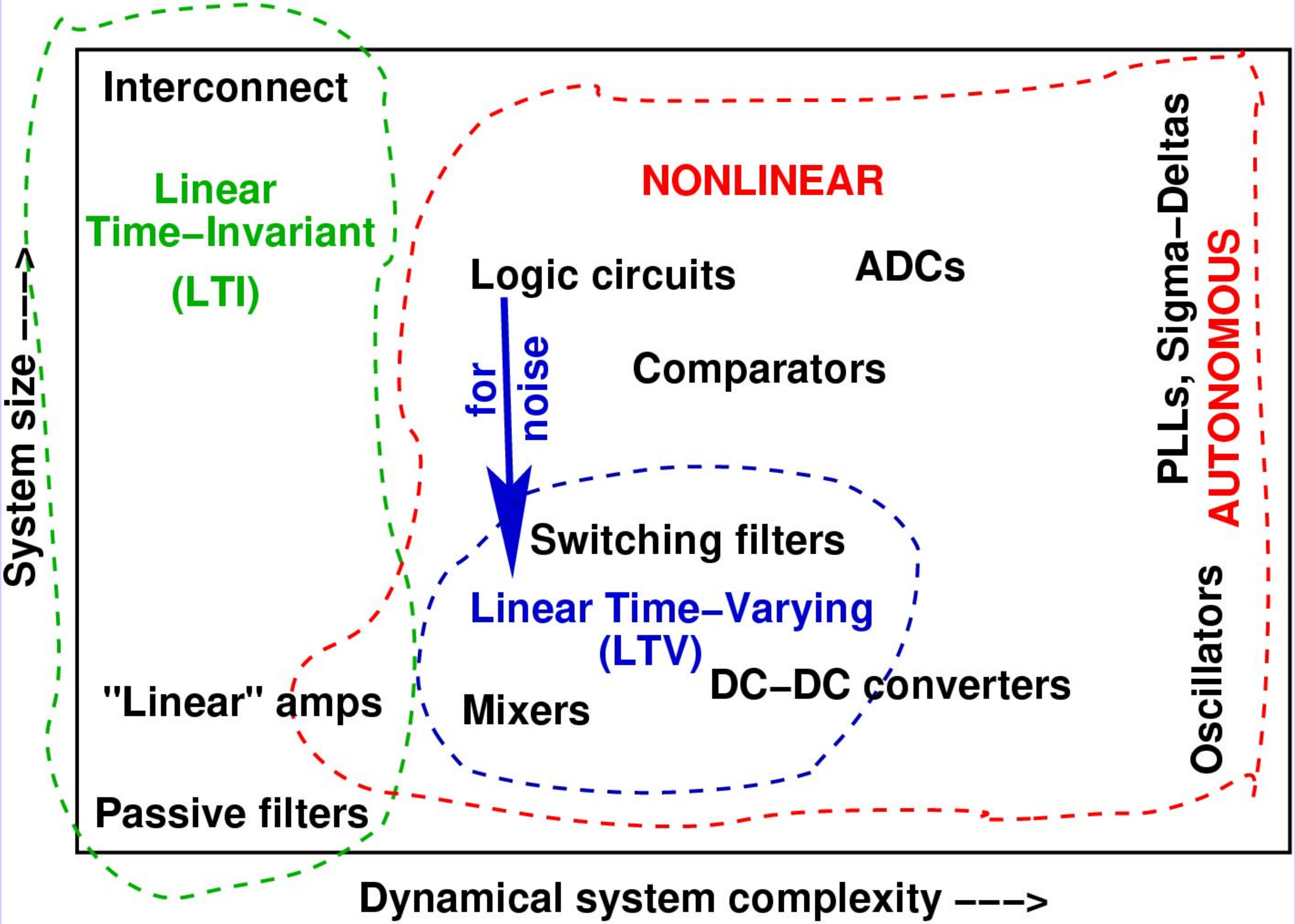
- Extract small-signal linear time-varying interference macromodel by mathematically-based algorithm
  - generalizes both switch-based and current-source approaches
  - **single macromodel captures substrate and power/gnd interference**
- Technique imported from mixed-signal/RF simulation
  - linear time-varying model-order reduction algorithm
  - SPICE in, digital noise macromodel out

Macromodel Generation: Linear vs Nonlinear



- Linear time invariant (LTI): power/ground/substrate RLC networks
- Nonlinear: digital circuits, switching effects
  - LTV models capture <u>changing R/C during switching</u>

Macromodelling of Classes of Systems



Macromodelling LTV Systems

$$\begin{bmatrix} & C(t) & \end{bmatrix} \begin{bmatrix} \dot{x} \end{bmatrix} + \begin{bmatrix} & G(t) & \end{bmatrix} \begin{bmatrix} x \end{bmatrix} = \begin{bmatrix} b(t) \end{bmatrix}$$

$$\Big\downarrow \text{TVP}$$

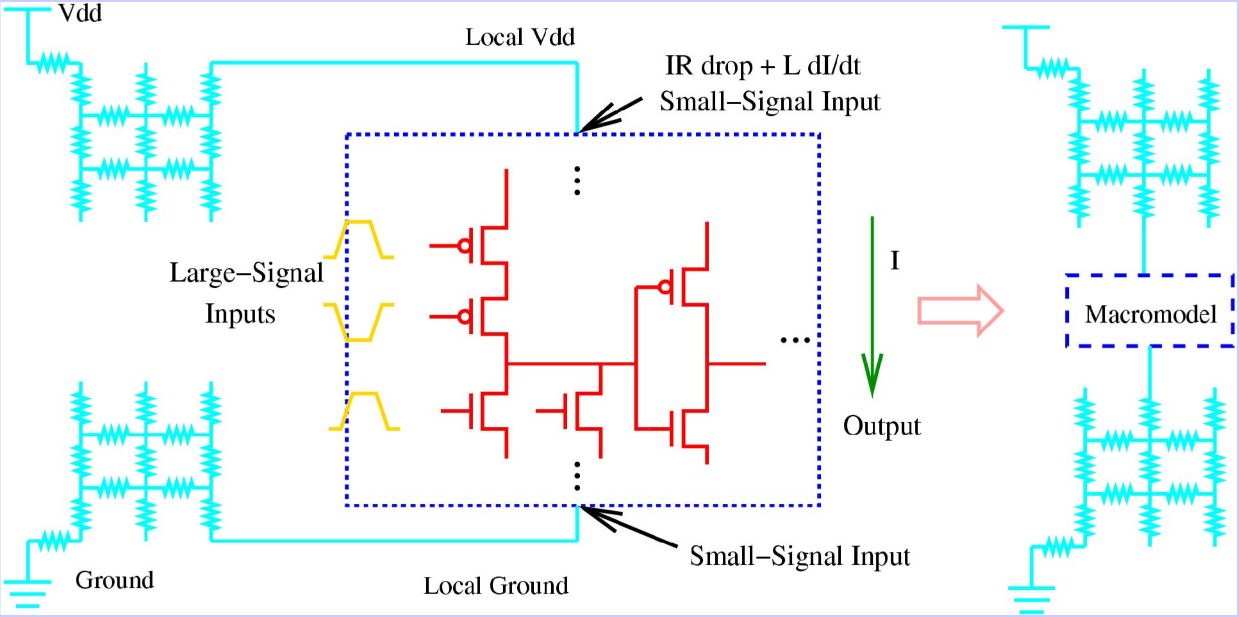
$$[C(t)][\dot{y}] + [G(t)][y] = [\hat{b}(t)]$$

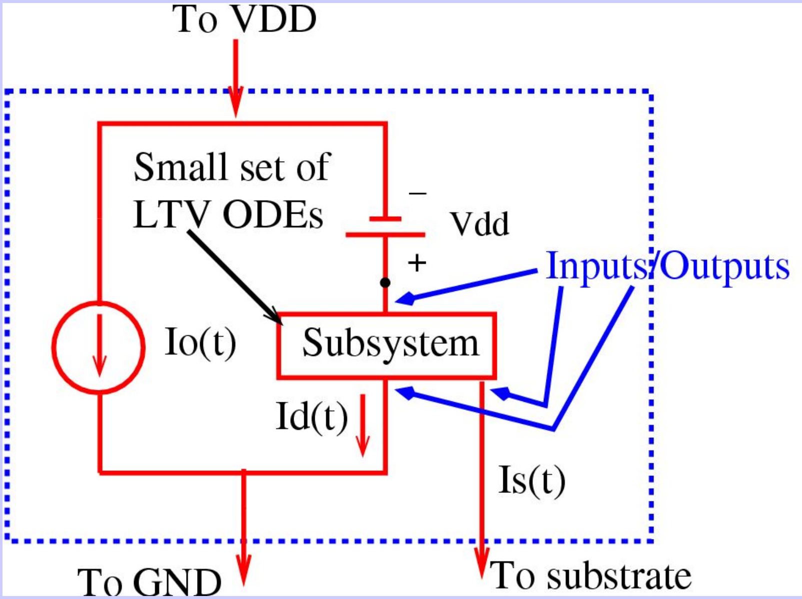
- G(t), C(t): changing resistances/capacitances (due to switching)
  - generalization of abrupt switching
- Perturbations from strongly nonlinear operation captured
  - appropriate for “small” noise
- Macromodelling algorithm: Time-Varying Pade (TVP)
  - originally used for mixers, switched-capacitor filters, etc..

Overview of Time-Varying Pade (TVP)

- Given: large circuit in SPICE (ie, differential equations)
- A few small-signal inputs/outputs of interest identified
  - key: identify ports connecting to substrate/supply
- Nominal large-signal (switching) response computed
- Small-signal time-varying transfer function captured
  - reduced to small macromodels via algorithm
  - technique: Krylov-subspace-based MOR methods
  - macromodel size/accuracy tradeoff
- (details: Wang/Roychowdhury, IEEE Trans CAD, Feb 2005)

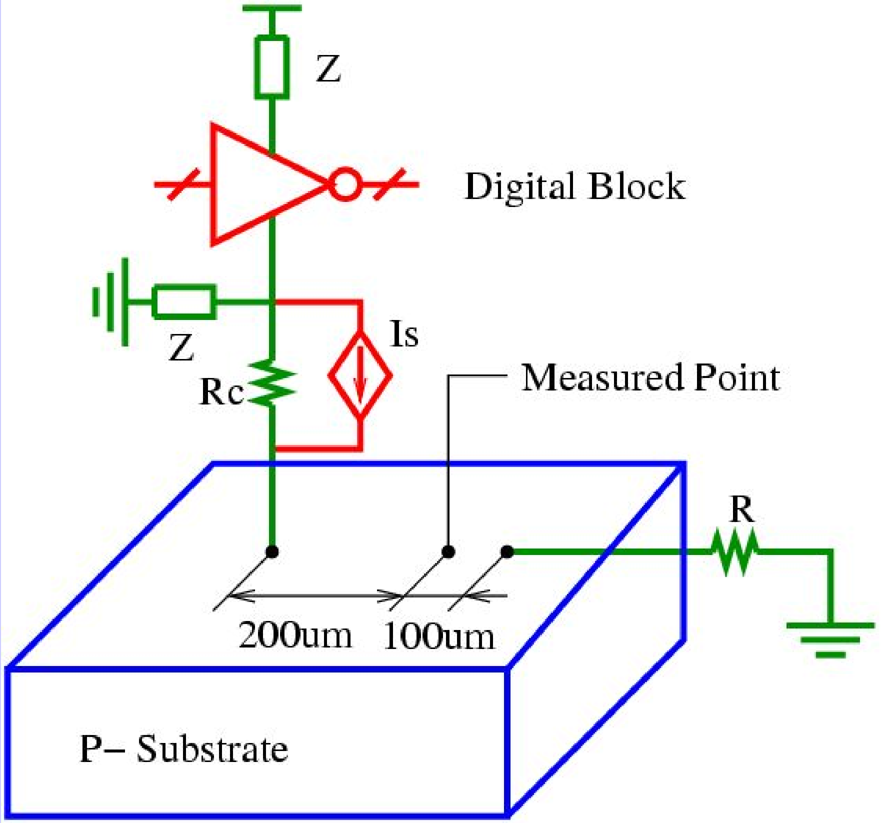
Connectivity and Form of Unified Substrate/Supply Interference Macromodel

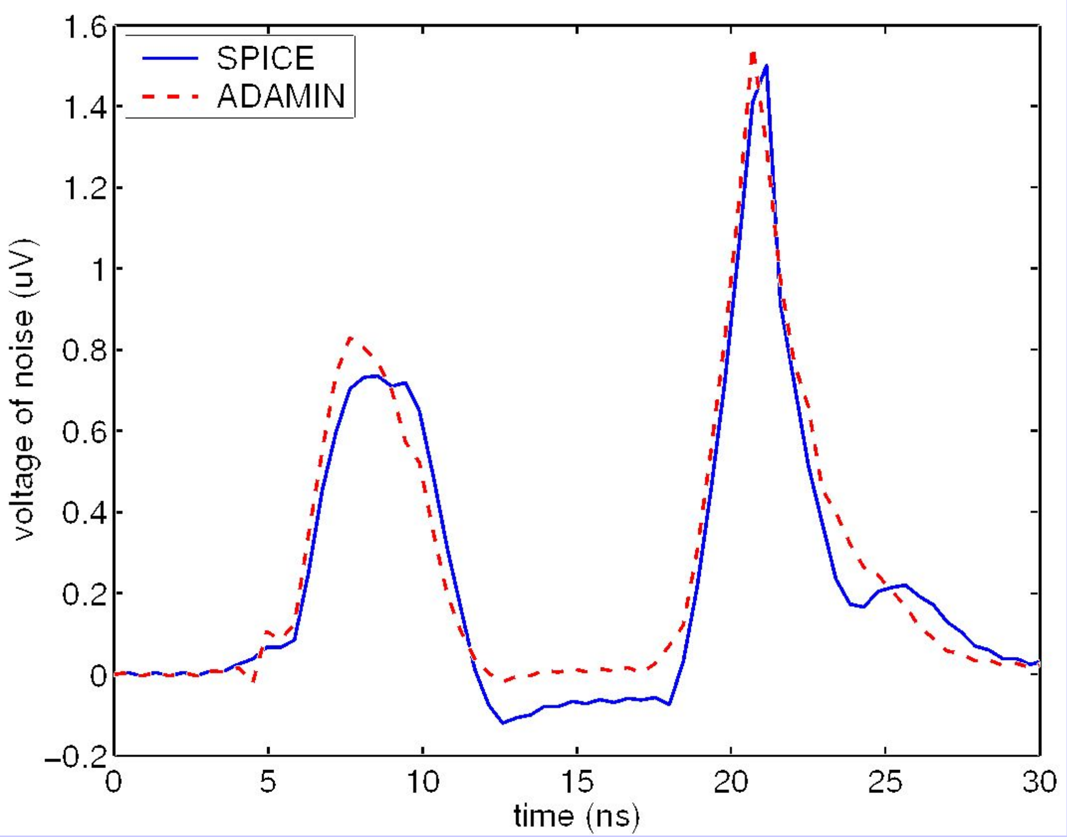




- Input: power supply/substrate voltage variation
- Output: resulting current variation
- MM: small time-varying system relating input to output

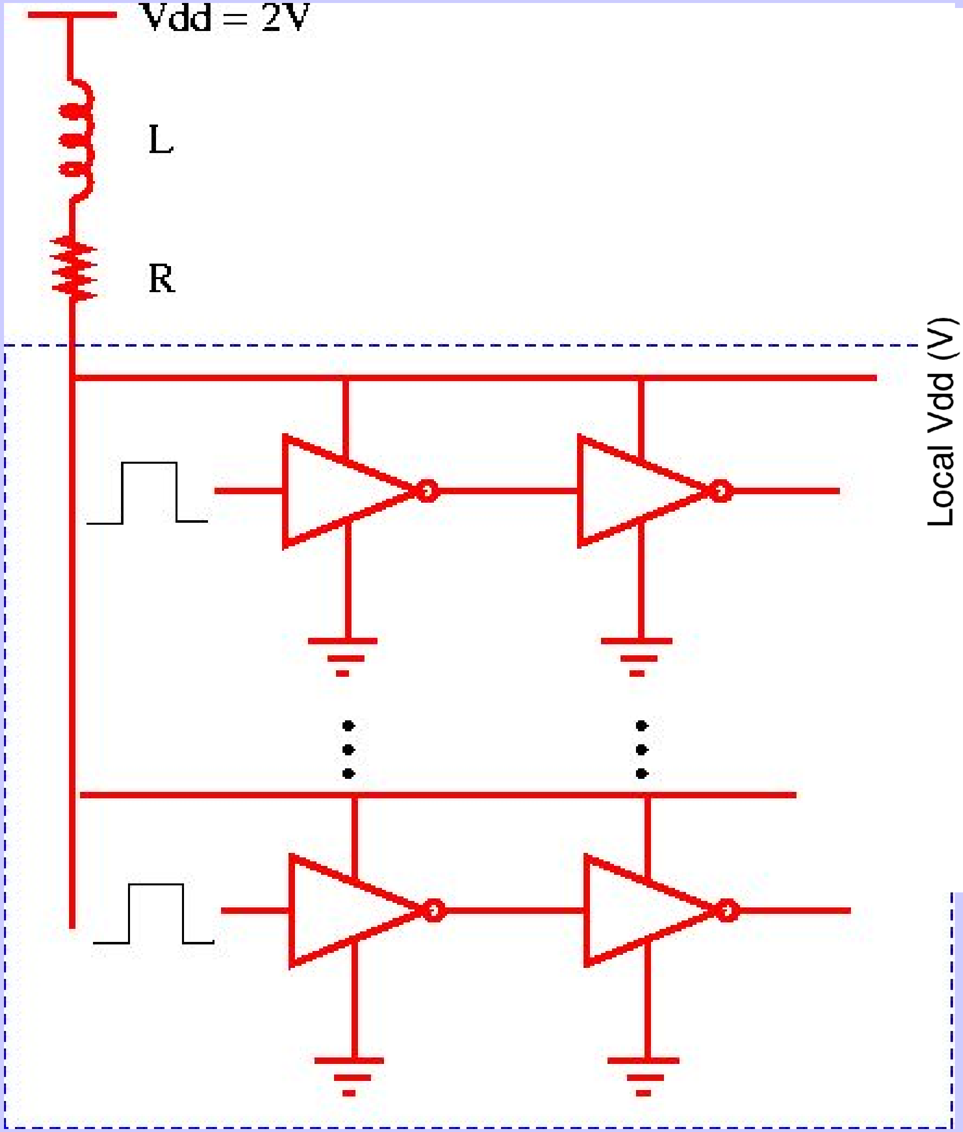
Substrate Injection: Block of 20 Inverters

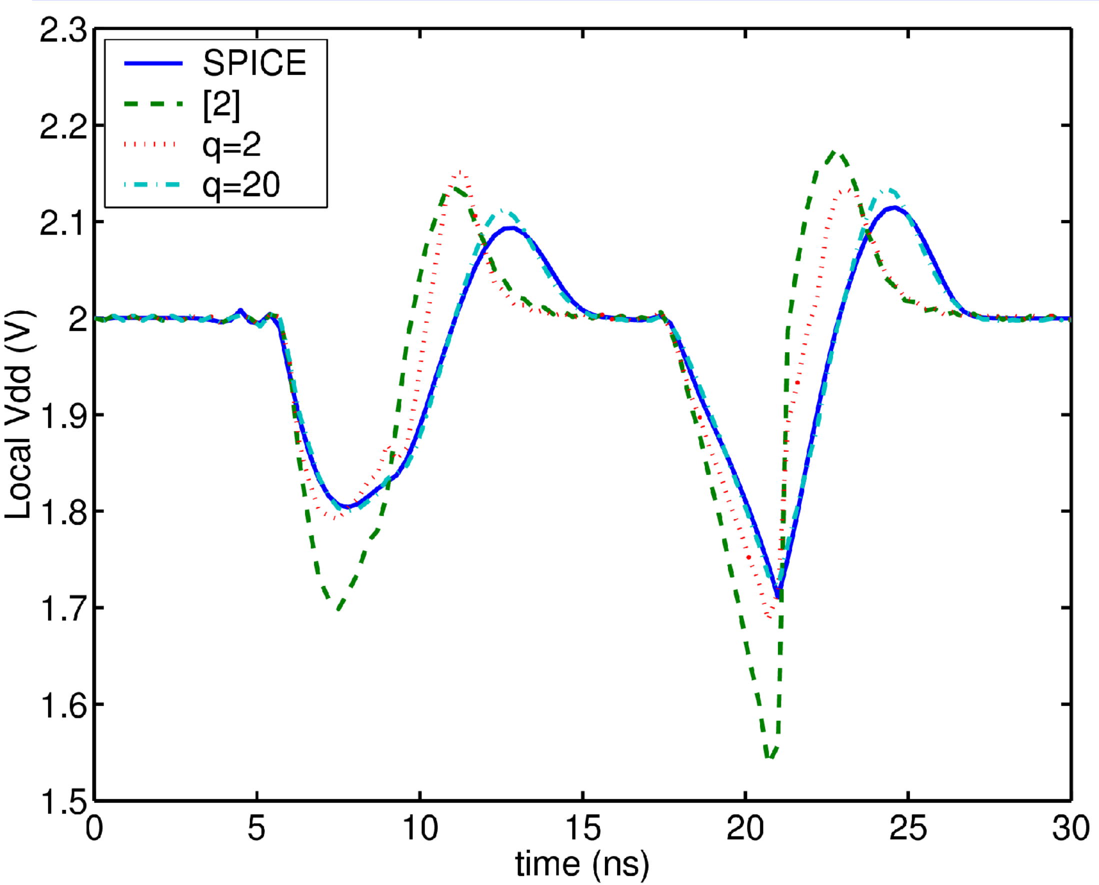




- Error = 3.21% and 70 times faster than original.

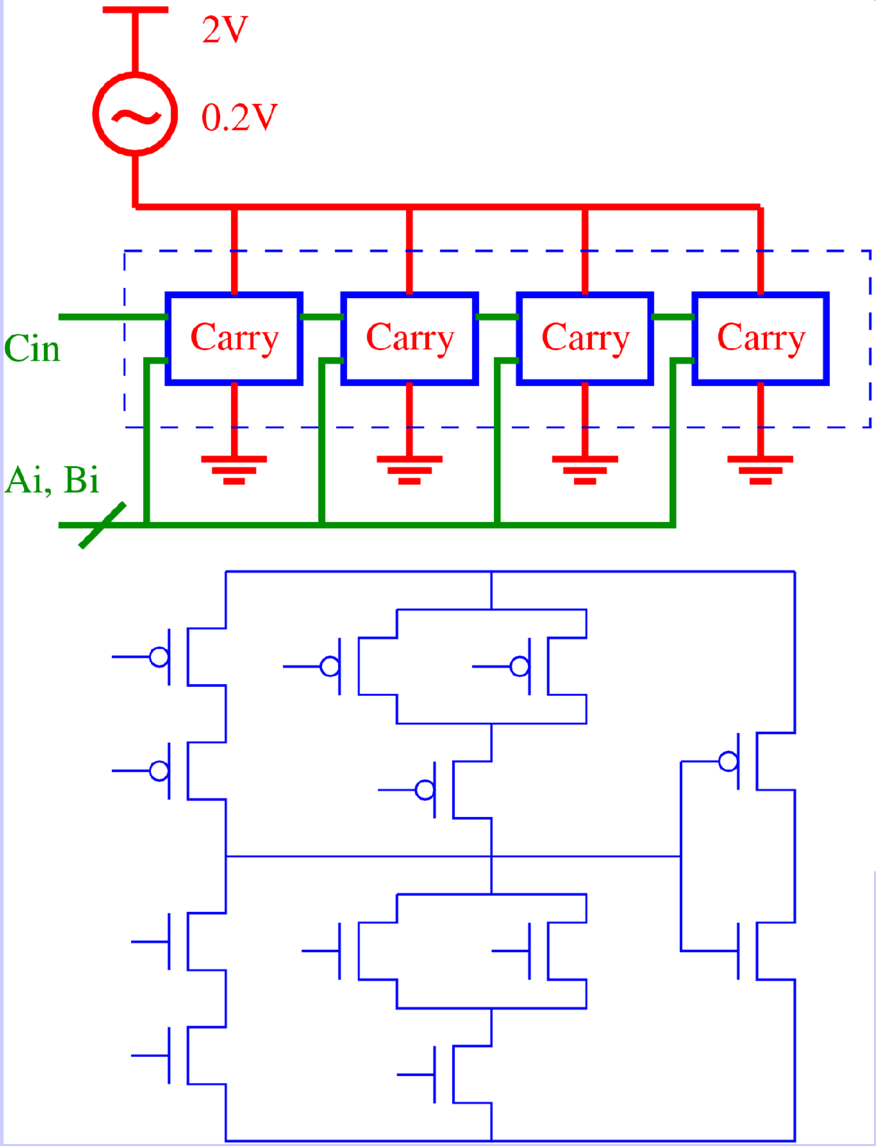
Supply Noise: Inductive Power Grid

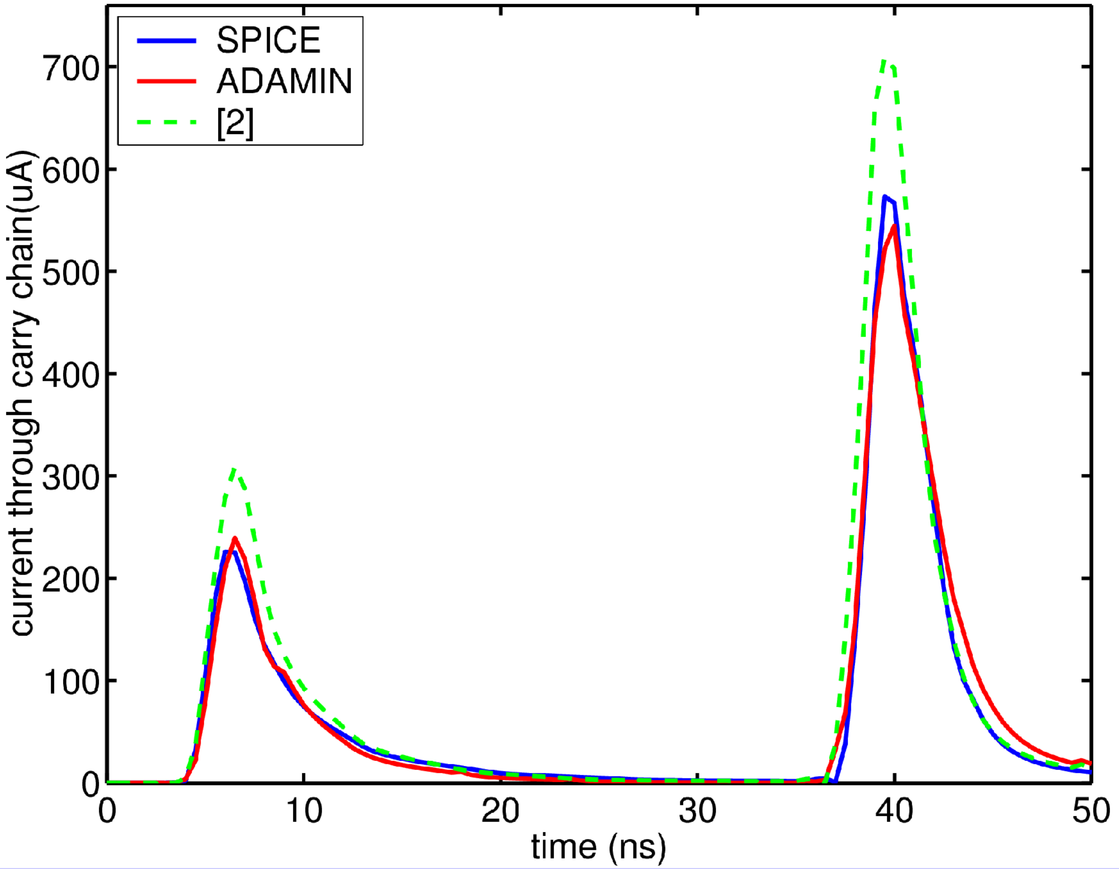




- size 2 MM: already better
- size 20: much more accurate
- 17000x speedup for 8000 gates

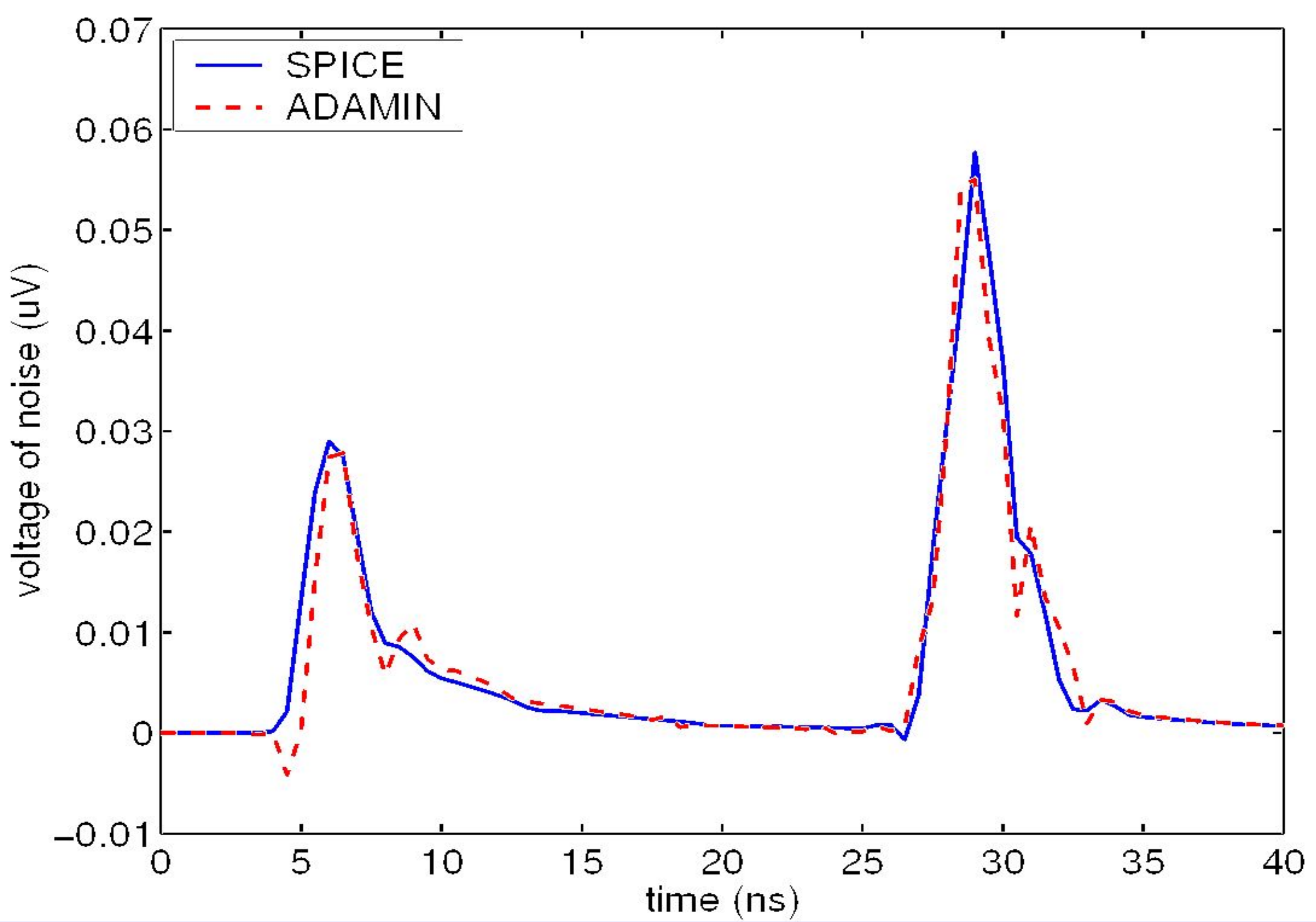
Carry-Chain Adder: Supply Noise Results





- Considerable accuracy improvement over current-source macromodel [Dharchoudhury 98]

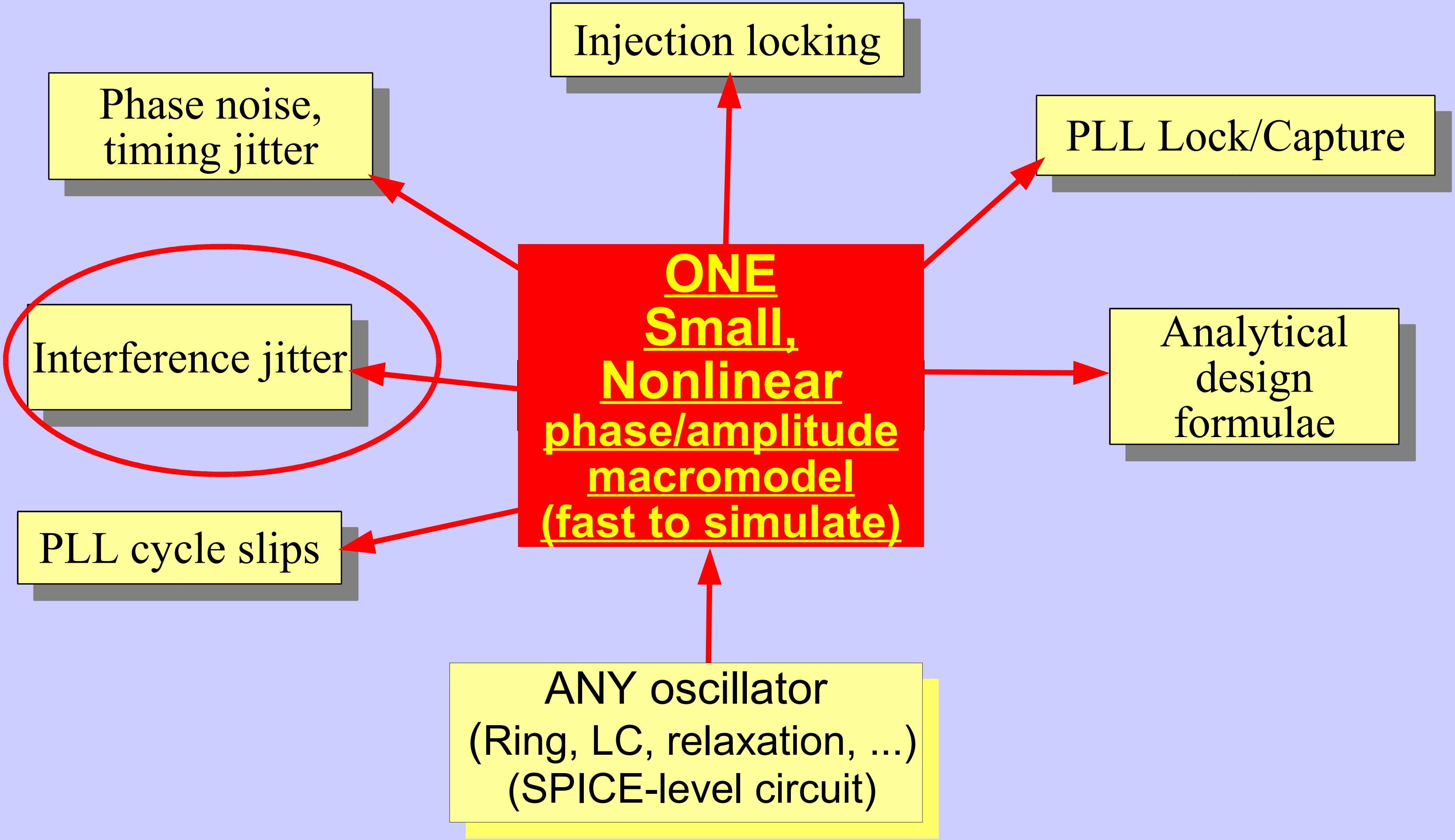
Carry-Chain Adder: Substrate Injection Results



- Error = 4.68% and 160 times faster than original.

Impact of Interference on Victims: using Macromodelling to predict VCO/PLL Performance Deterioration

Nonlinear Oscillator Macromodel



ONE Small, Nonlinear phase/amplitude macromodel (fast to simulate)

Injection locking

Phase noise, timing jitter

PLL Lock/Capture

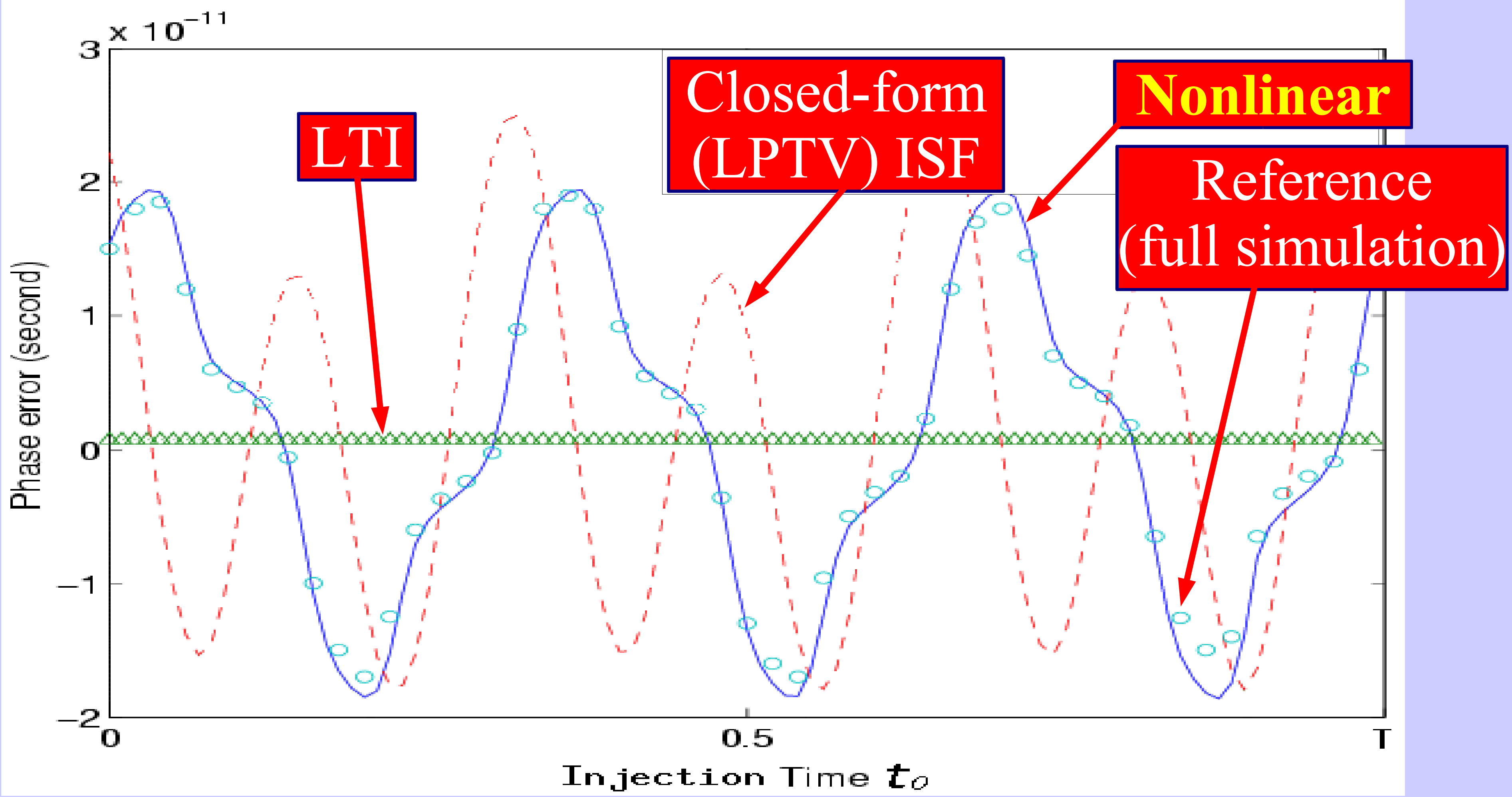
Interference jitter

Analytical design formulae

PLL cycle slips

ANY oscillator (Ring, LC, relaxation, ...) (SPICE-level circuit)

Ring Oscillator: Jitter due to Momentary Impulses at Different Shifts



LTI

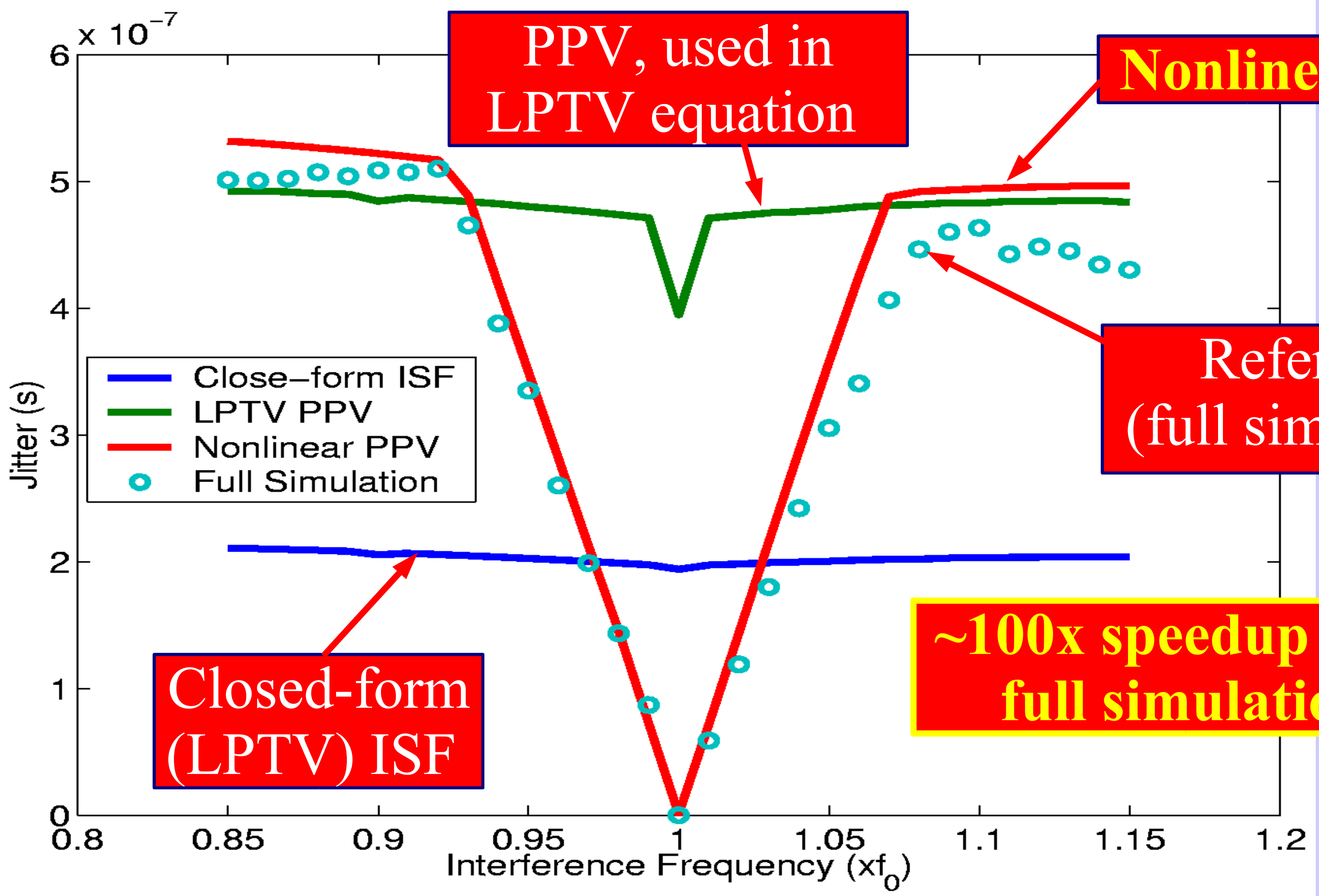
Closed-form (LPTV) ISF

Nonlinear

Reference (full simulation)

~100x speedup over full simulation

Ring Oscillator: Per-cycle jitter as a function of Sinusoidal Supply Interference



PPV, used in LPTV equation

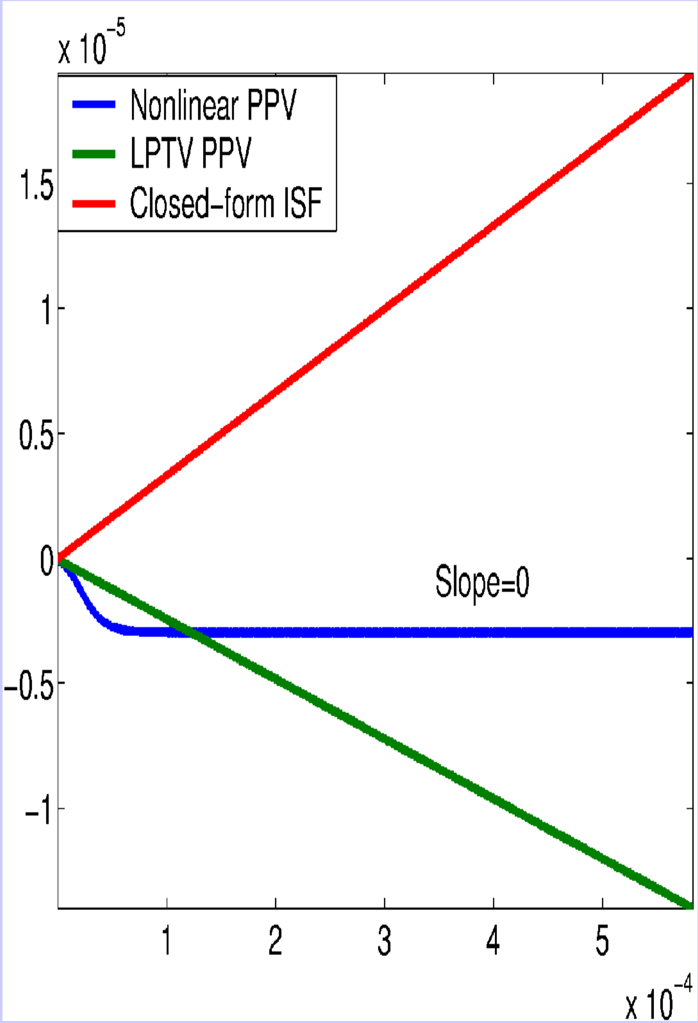
Nonlinear

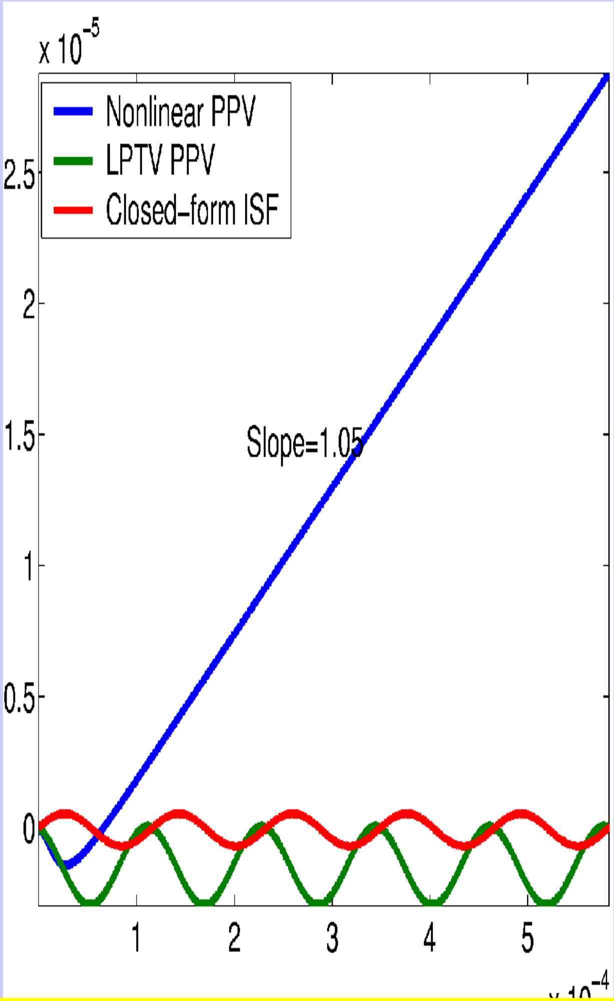
Reference (full simulation)

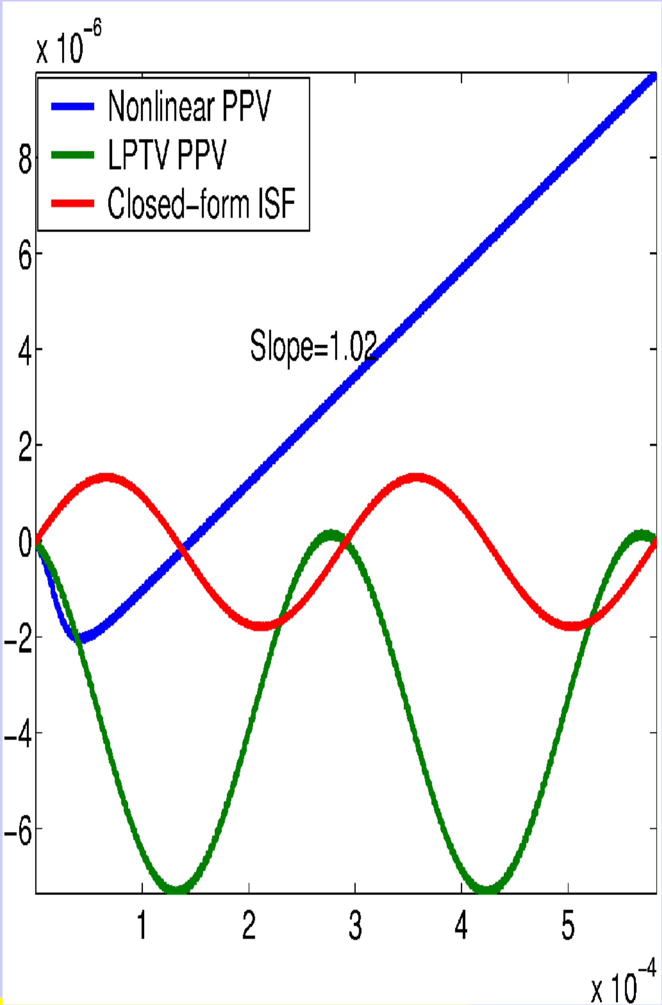
Closed-form (LPTV) ISF

~100x speedup over full simulation

Ring Oscillator: Jitter due to Sinusoidal Interference Noise



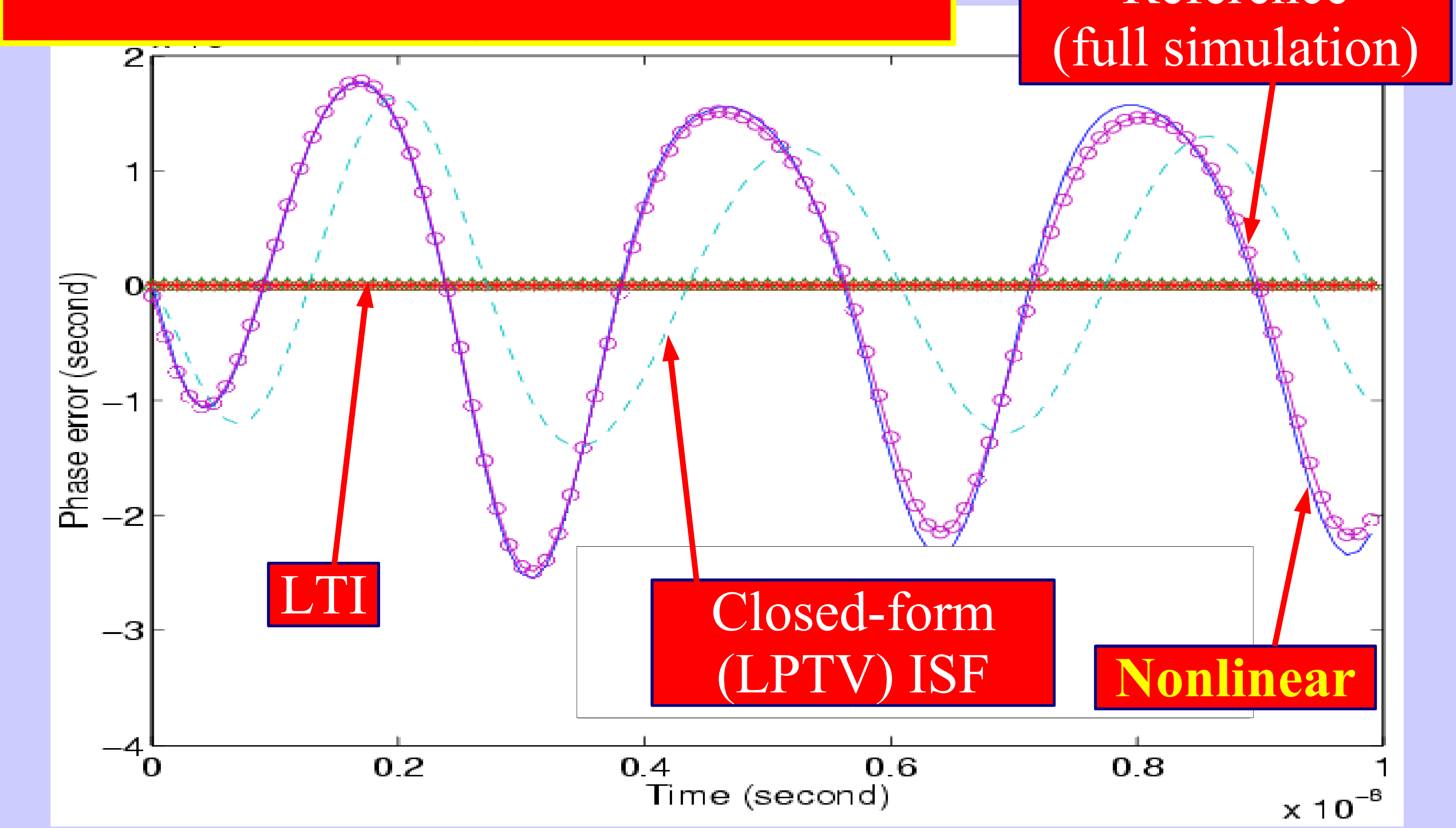




~100x speedup over full simulation

PLL: Jitter due to Sinusoidal Interference

>1000x speedup over full simulation



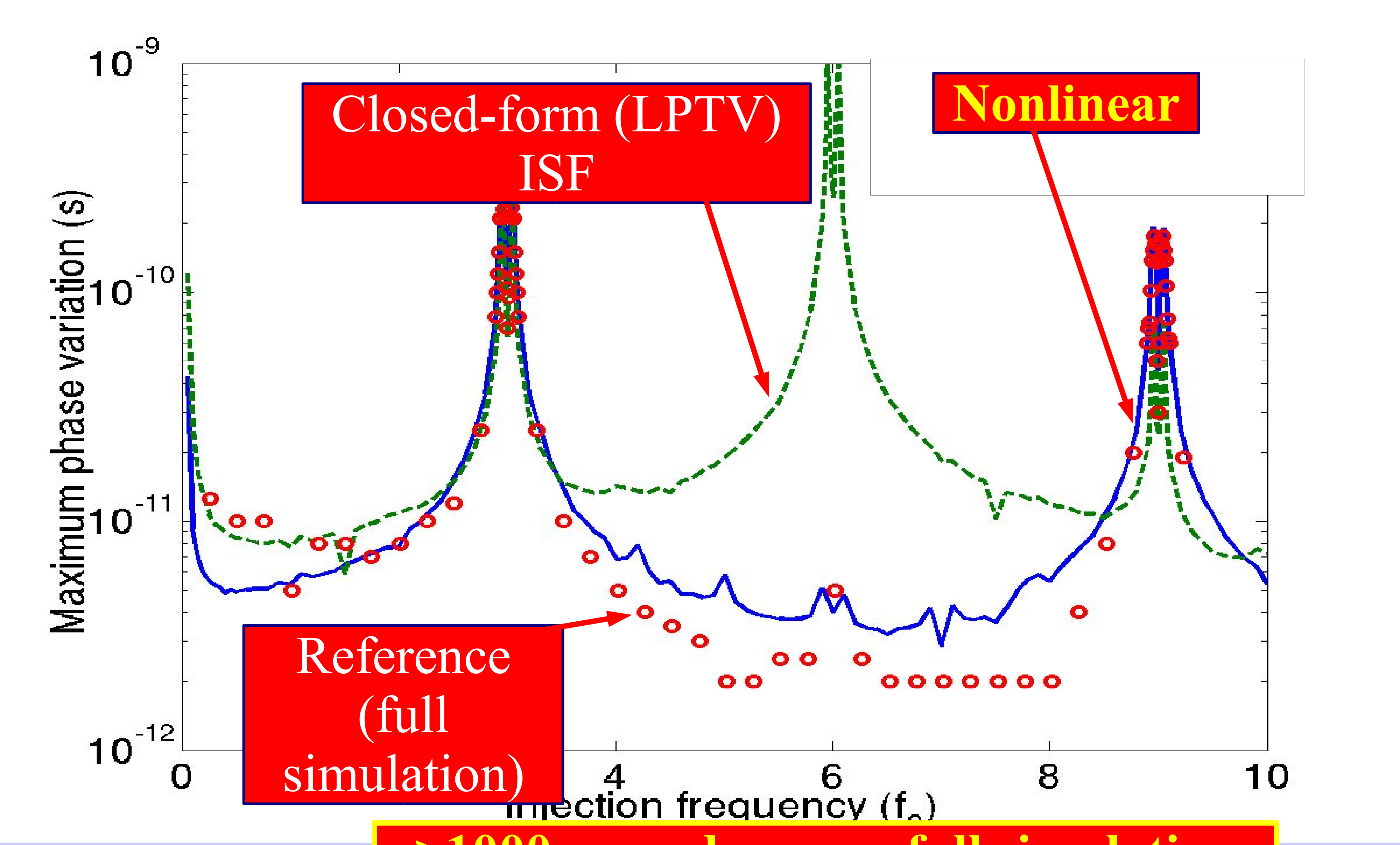
Reference (full simulation)

LTI

Closed-form (LPTV) ISF

Nonlinear

PLL: Max jitter as Function of Sinusoidal Supply Interference Frequency



Closed-form (LPTV) ISF

Nonlinear

Reference (full simulation)

>1000x speedup over full simulation

Conclusion

- Digital interference macromodel generation technique
  - fully automated generation, via algorithm
  - switching and “nonlinear loading” accounted for
- Accuracy/Speedup
  - well under 20% error, typically around 5%
  - 2 orders of magnitude speedup even for small ckts
  - 4-5 orders of magnitude speedup for ~17000 gates
- Macromodel generation and use
  - easily feasible with SPICE ckts of 1000s of nodes
  - hierarchical compaction of clusters of macromodels
  - good fit with cell library characterization methodologies
  - co-simulate with VCO/PLL nonlinear phase macromodels