Automated Macromodelling of Systems with Nonlinear Blocks

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Automated Macromodelling

- The dream: **push-button bottom-up model generation**
  - Rob's Red Button
  - prescribed accuracy guaranteed
  - trade off **speed vs accuracy**
- Needed for design sustainability
  - complexity exceeds manual ability to keep up

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"The Gap"

"At this point, you may wonder why you should bother with behavioral libraries and calibration. Why not just submit the transistor-level design to some smart software and let it come up with a model? Unfortunately, despite some claims to the contrary, practical model synthesis is still a long way off. Attempts at this technology rely on pre-existing templates, which are unlikely to exist for leading-edge or proprietary designs. There's no pushbutton approach to analog modeling, and from all indications, this will remain the case for some time to come." - EE Times, 2001

- Perhaps not quite so bleak!
- Automated macromodel generation **is** difficult

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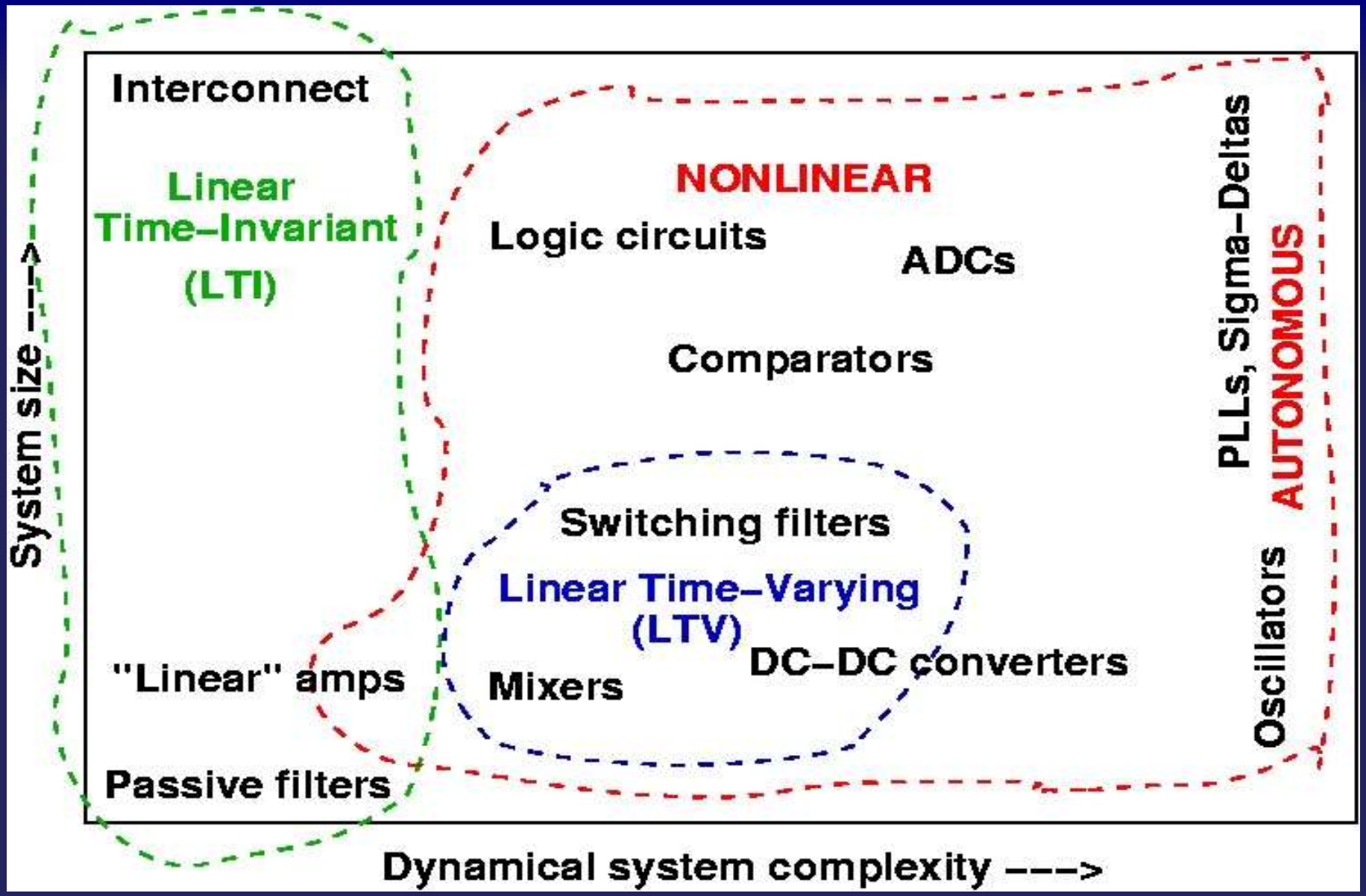
Why Difficult?



Approaches to Macromodelling

- **Black box** problems
  - samples of input-output pairs
  - from measurement and/or simulation
  - paucity of information
- **Extraction (bottom-up reduction)** problems
  - detailed circuit/simulation info available
  - eg, SPICE netlist: differential equations
  - surfeit of information
  - potential for better macromodels

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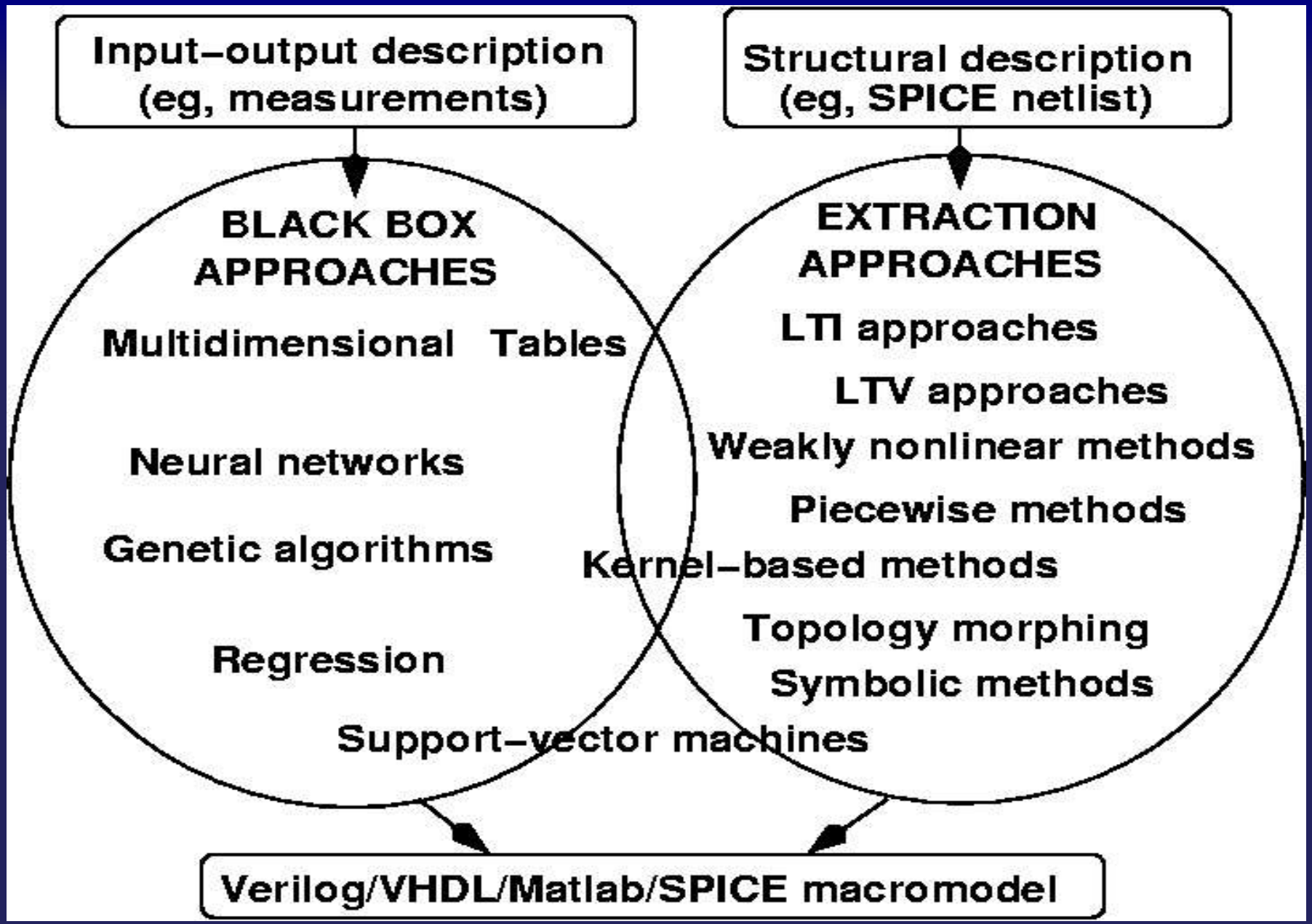
Automated MM Approaches



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Macromodelling Languages

- Output of macromodelling process
- AHDL languages – eg, Verilog-A, VHDL-AMS
  - the EDA choice
- Matlab/Simulink
  - widely used by designers
- SPICE(?)
- Fundamentally: (integro-)differential-algebraic equations

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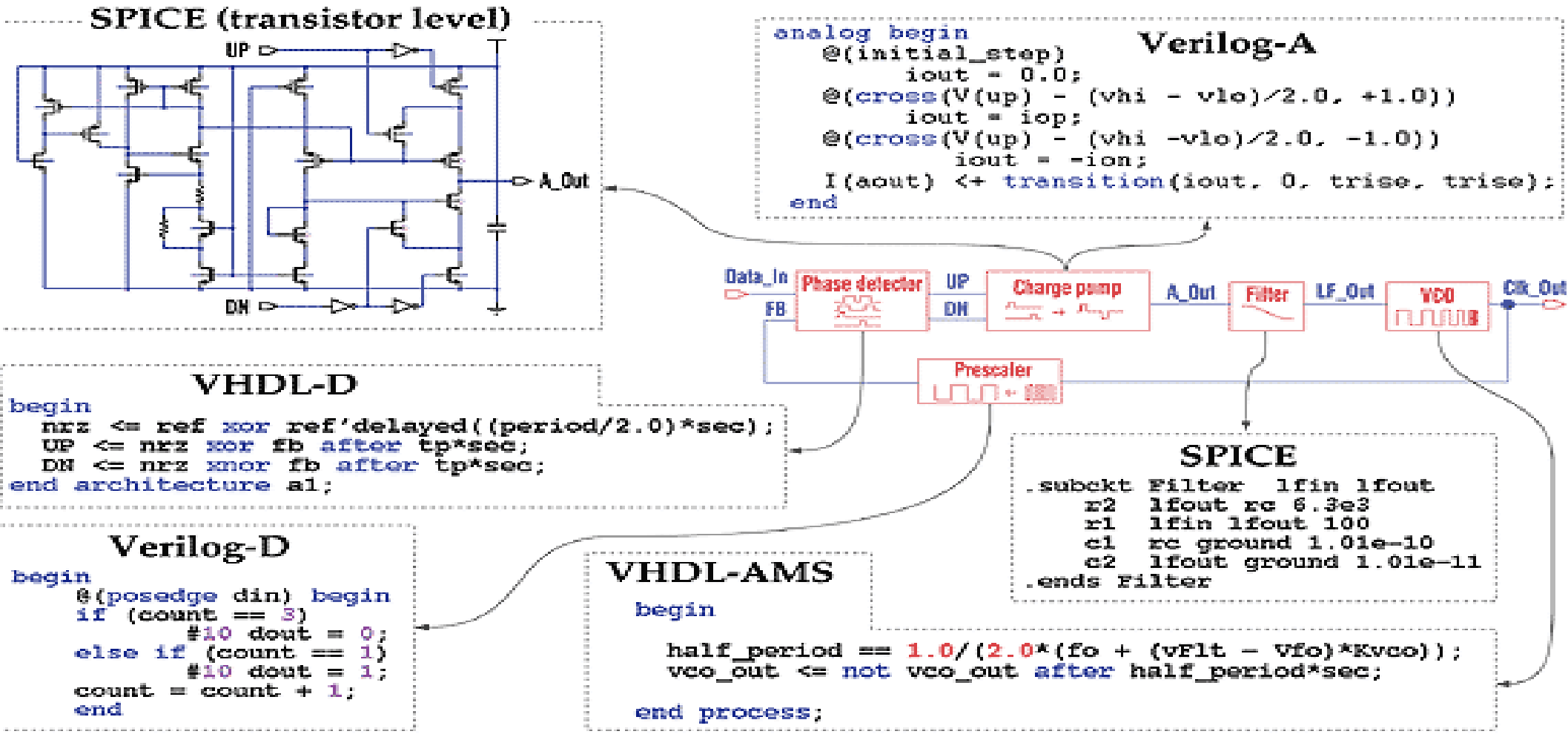
Macromodelling Languages



EE Times

Multiplicity of languages, should inter-operate

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"Algorithmic" Macromodelling Approaches

- **Mathematical algorithms** based on theory
- **Provably preserve some useful property**
  - eg, moments of transfer function
- **AWE:** first prominent method (LTI)
- Variety of nonlinear, LTV methods
- **Generally applicable** (eg, multi-physics)
  - not specific to a particular type of circuit/topology
  - eg: same oscillator MM technique works as well for a Colpitts oscillator as for a DFB laser or a grandfather clock

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Types of Algorithmic Macromodelling

- **Linear Time Invariant (LTI)**
  - application: interconnect (delay, crosstalk)
  - AWE, PVL, PRIMA, TBR
- **Linear Time Varying (LTV)**
  - mixers, sampling/switching circuits, (oscillators)
- **Weakly nonlinear (Volterra)**
  - companding ckts, amplifier/mixer gain compression
- **Strongly nonlinear (stable)**
  - everything else: comparators, switching, slewing, ...
- **Autonomous**
  - oscillators, PLLs, etc.: marginally stable

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Macromodelling Linear Time-Varying Systems

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Linear Time-Varying Macromodelling

- Useful abstraction for some nonlinear systems
  - mixers, switching filters, samplers, DC/DC converters
  - leverage LTI methods
  - frequency translation, sampling captured
  - signal-path nonlinearities **not** captured
- Input-output relationship linear
  - but **not** time-invariant

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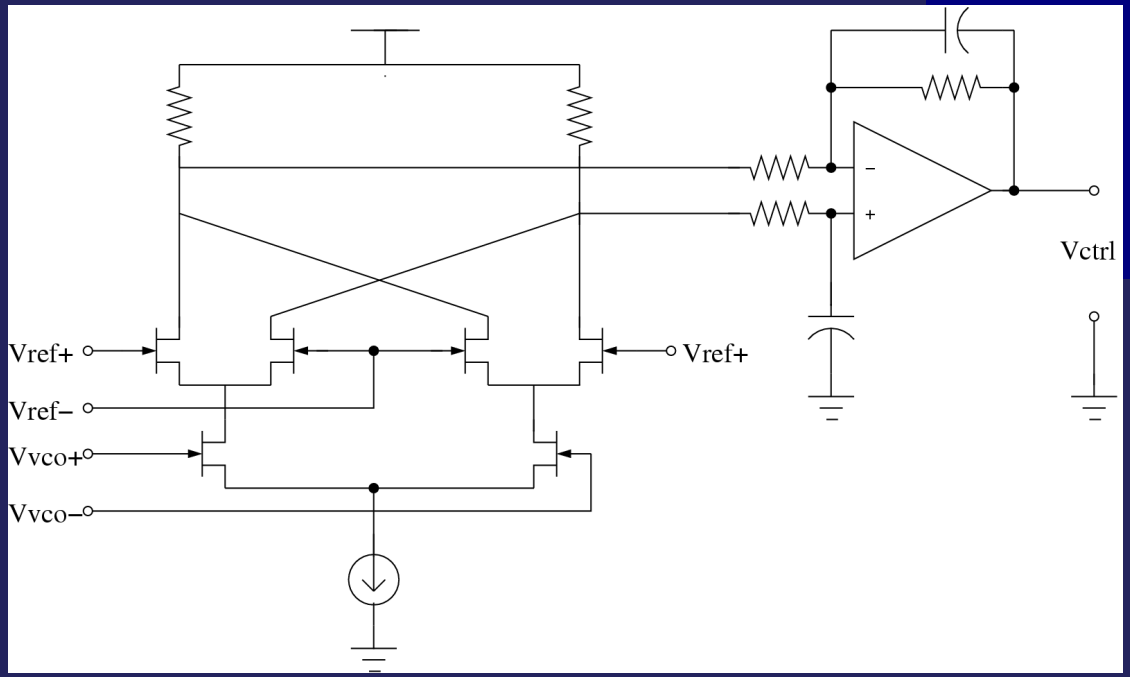
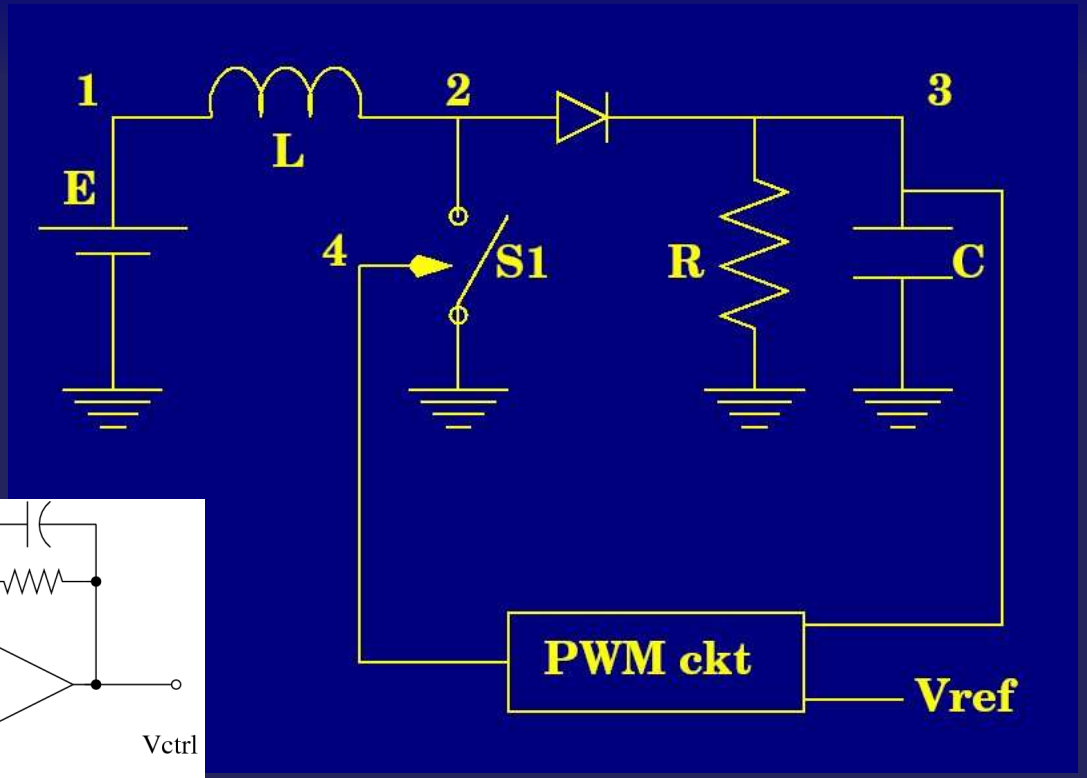
Example candidates for LTV Macromodelling

Gilbert Cell Mixer





DC-DC power converter

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Basic Principles of LTV Macromodelling

- LTV systems have time-varying (but linear) transfer functions
  - LTI transfer function H(s) --> H(t,s)
    - t captures system time variation
    - s captures input/output time variations
  - computationally useful form of H(t,s):
    - linear matrices C(t) and G(t): from transient simulation/steady state calculations

$$H(t_1, s) = d^T \left(\frac{\partial}{\partial t_1} C(t_1) + sC(t_1) + G(t_1) \right)^{-1} [b]$$

[Roychowdhury, Phillips ICCAD 98] [Roychowdhury TCAS-2 99]

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Reducing LTV Systems

- Matching moments of H(t,s)
  - Moments are w.r.t s (moments are functions of t)
  - One way to leverage LTI moment-matching MOR techniques
    - convert LTV system to artificial LTI system
    - increases number of "outputs" -- one output for each t
- Eg, for periodic LTV systems: Fourier basis
  - expand H(t,s) in Fourier series in t
  - SIMO/MIMO system, each F. harmonic is an "output"

$$H_{FD}(s) = D^T \left(sC_{FD} + J_{FD}\right)^{-1} B_{FD}$$

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Reducing LTV Systems (contd)

- Now reduce the (bigger, artificial) LTI system
  - with, eg, Krylov-subspace methods
  - get a smaller reduced system of size q
  - convert back to LTV form

$$-T_q \frac{\partial x_q}{\partial t} + x_q = r_q u(t), \quad y(t) \approx l_q^T(t) x_q(t)$$

Linear Time Invariant

Memoryless Multiplication

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LTV Reduction: Procedure

- Input: circuit description (SPICE)
- first: get nonlinear steady state (via HB/shooting/etc)
- find time-varying matrices (often automatic) C(t), G(t)
- create large TI-matrix system (implicitly) by stacking C(t), G(t) for various “samples” of t
- run LTI model reduction methods to get a reduced model – choice of methods
- map back to LTV form
- size-vs accuracy tradeoff (as for LTI)
- LTI + memoryless-TV form: implementation convenience

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LTV Macromodel of RF Mixer

- I-channel mixer and buffer block (Lucent 2013 RFIC)
  - 360 nodes
  - signal upto ~80kHz, LO at 178MHz
- **LTV macromodel accuracy (Time-Varying Pade)**
  - size 2: upconversion transfer function matches to 300kHz
  - size 10: upconversion transfer function matches to **400MHz**
- **Speedup more than 500x**

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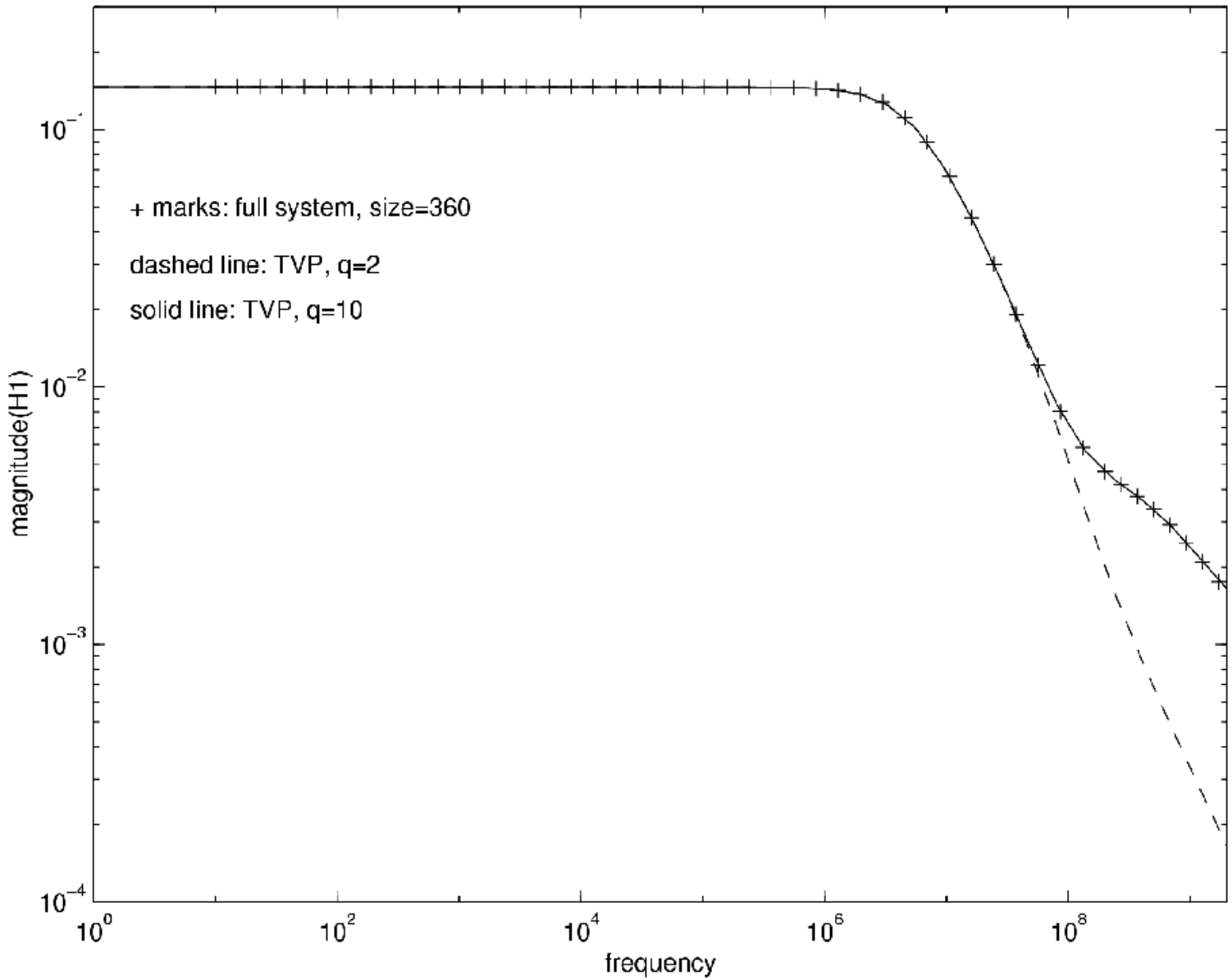
W2013 Upconversion Transfer Function



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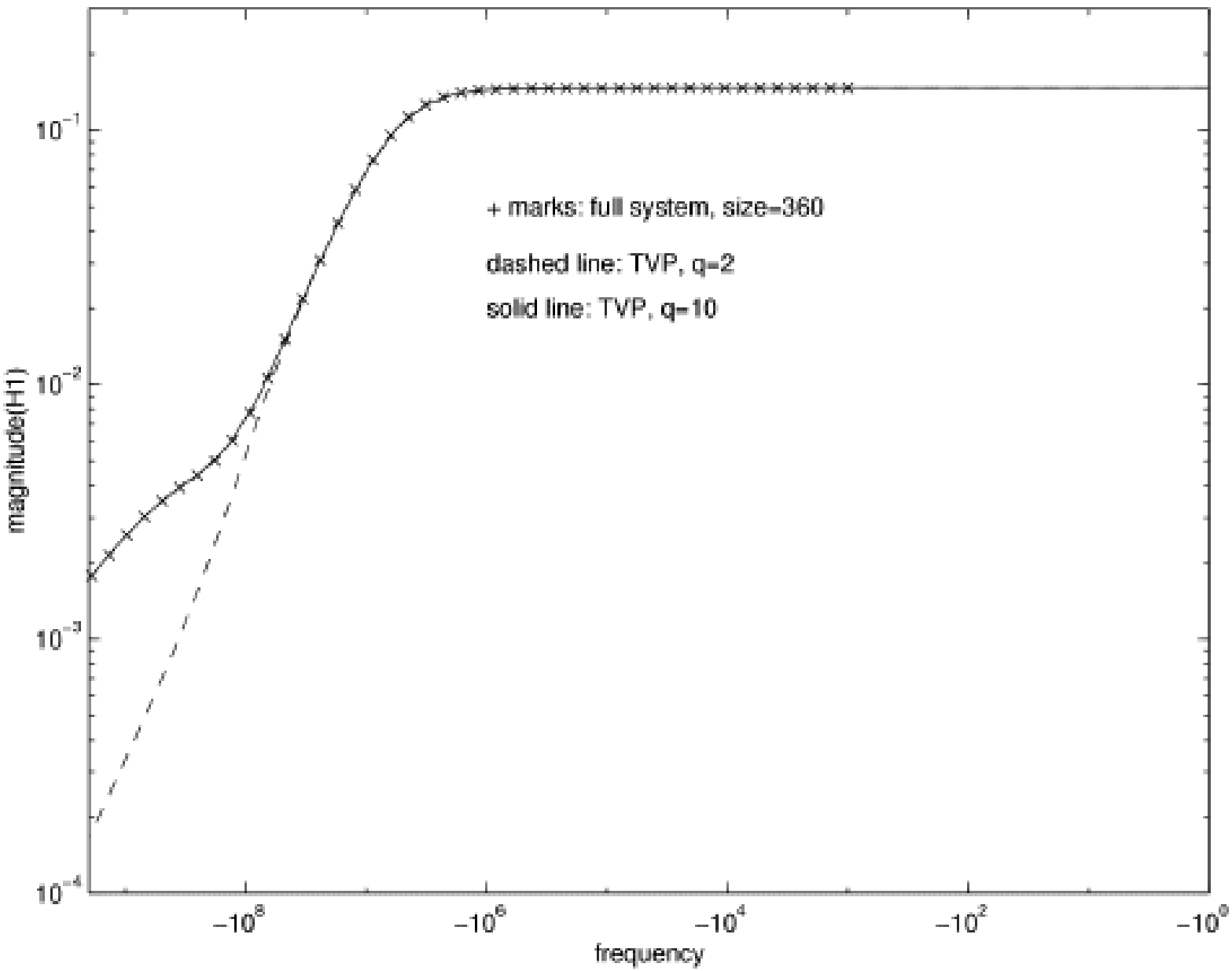
W2013 Downconversion Transfer Function



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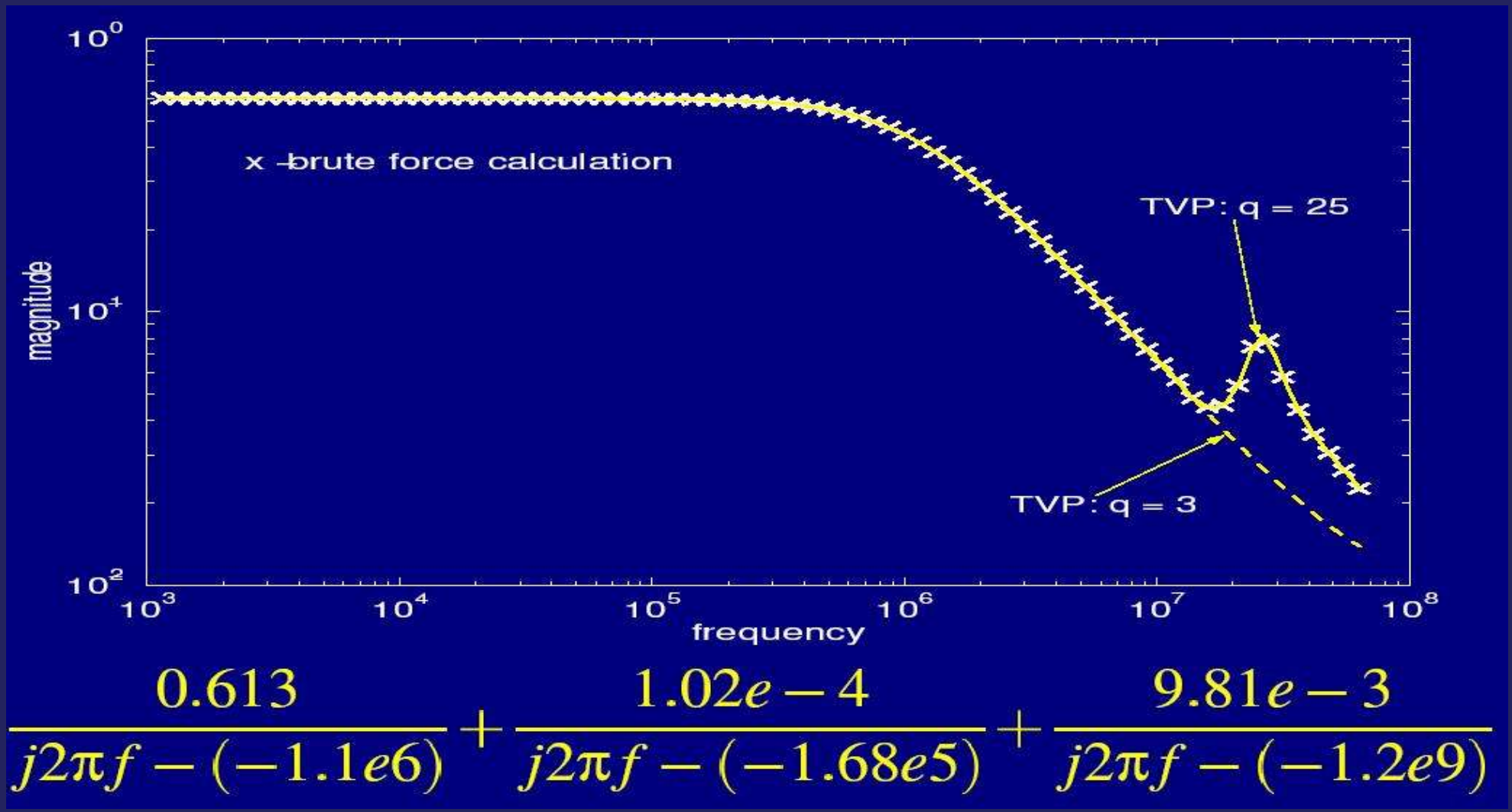
LTV Macromodel of Switched Capacitor Integrator Block

350 MOSFETS; clock=12.8MHz, signal=10KHz



$$\frac{0.613}{j2\pi f-(-1.1e6)}+\frac{1.02e-4}{j2\pi f-(-1.68e5)}+\frac{9.81e-3}{j2\pi f-(-1.2e9)}$$

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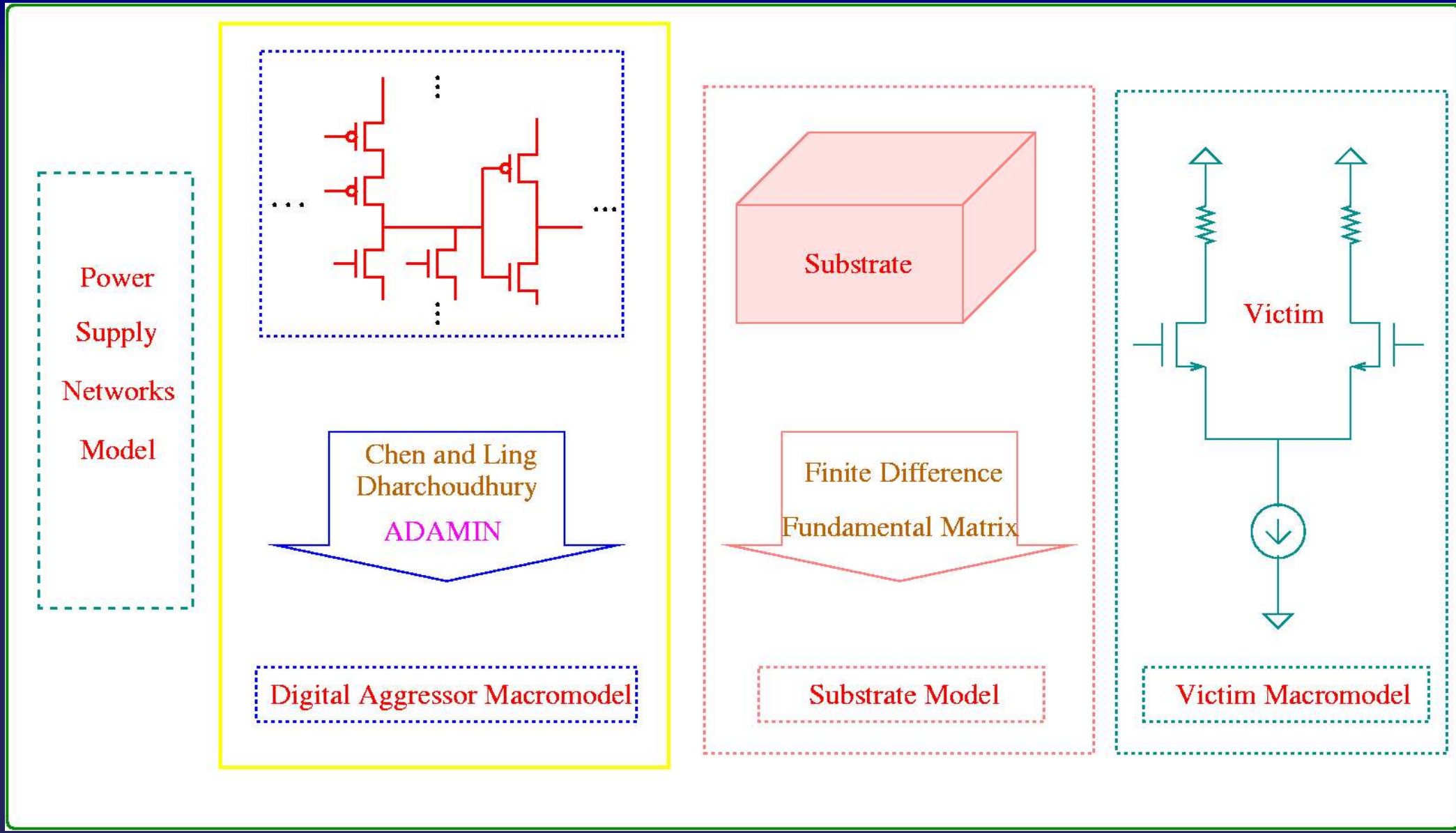
The Mixed Signal Interference Noise Problem



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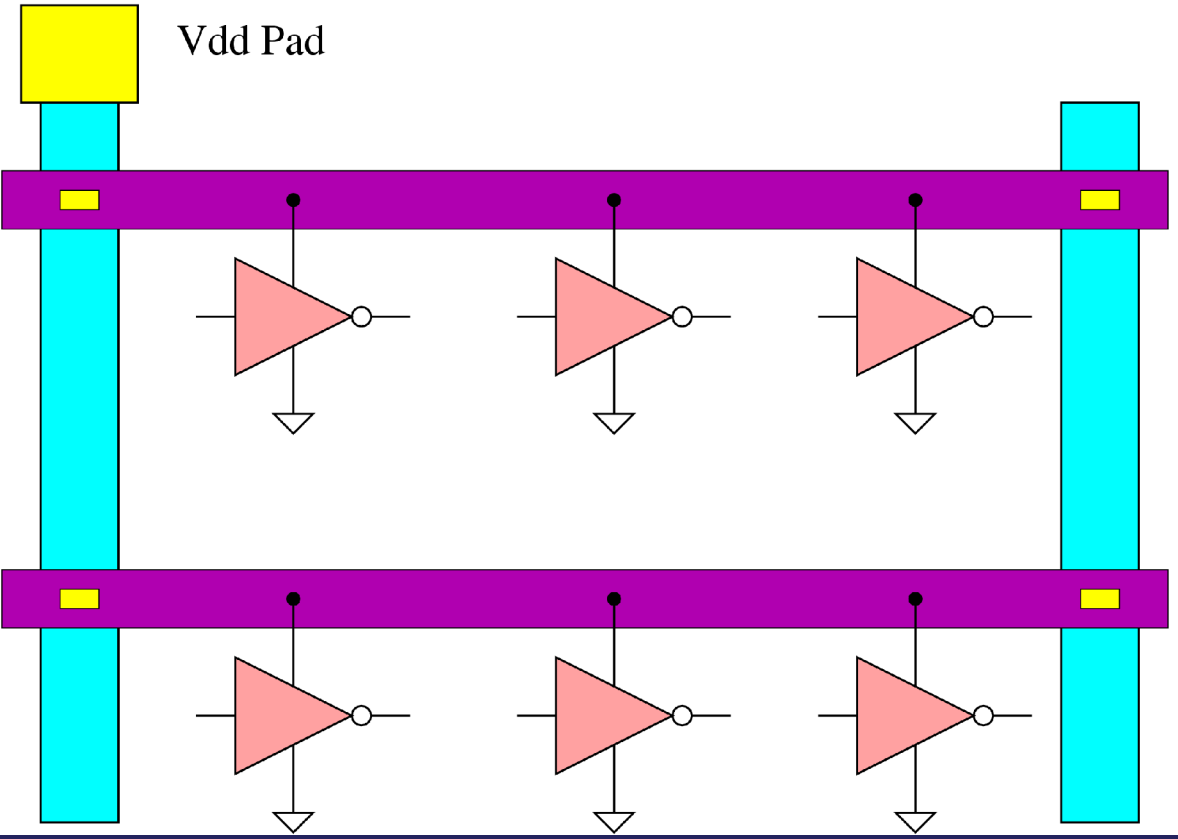
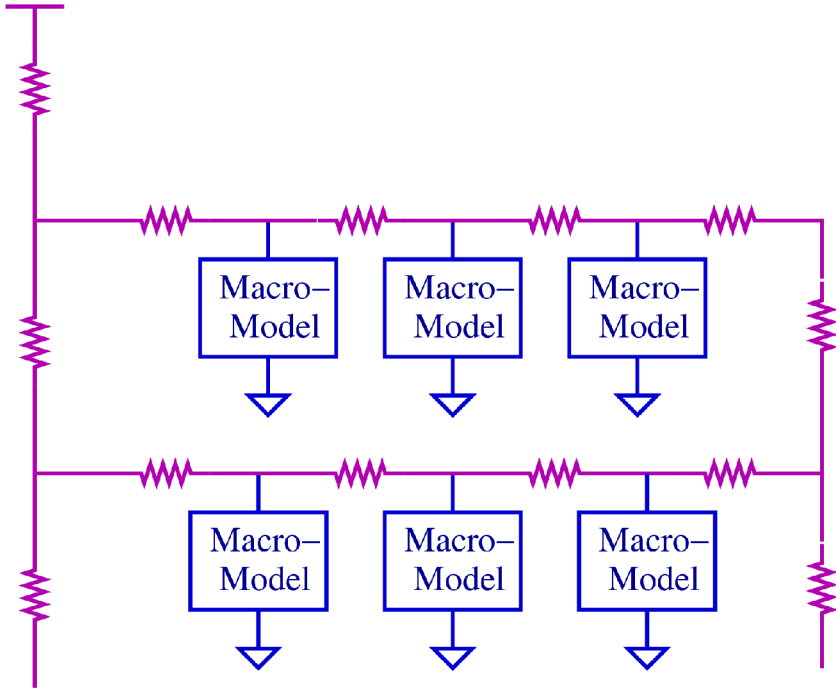
Macromodelling Digital Noise Injection





- Interested only in interference injection characteristics
  - supply and substrate injections: analog waveforms
  - digital signals: system time variation
  - LTV model captures switching behaviour well!

[Wang/Murgai/Roychowdhury DATE04]

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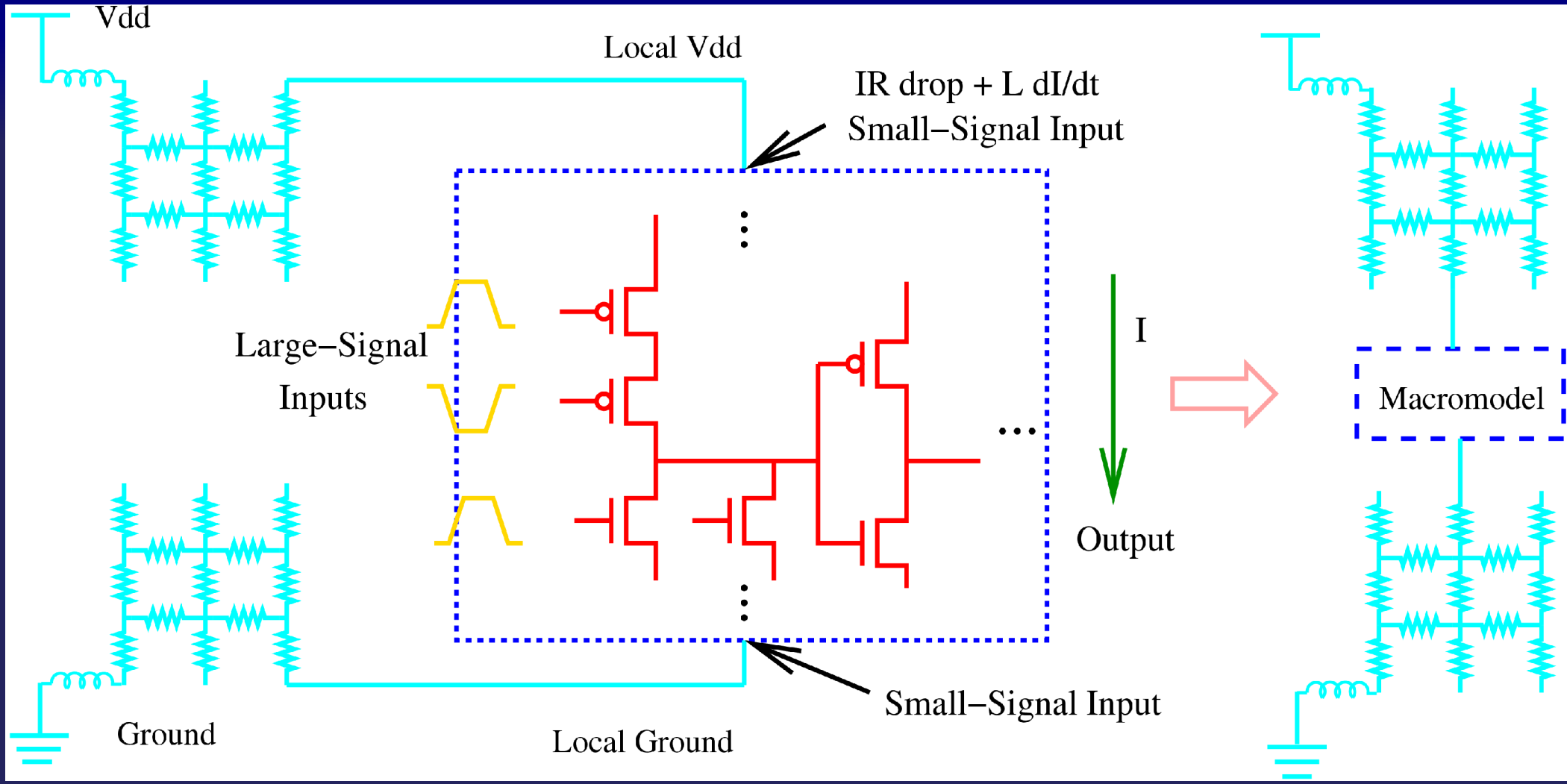
LTV Digital Aggressor Macromodels



- Input: (eg) power supply voltage variation
- Output: resulting current variation
- MM: small time-varying system relating input to output

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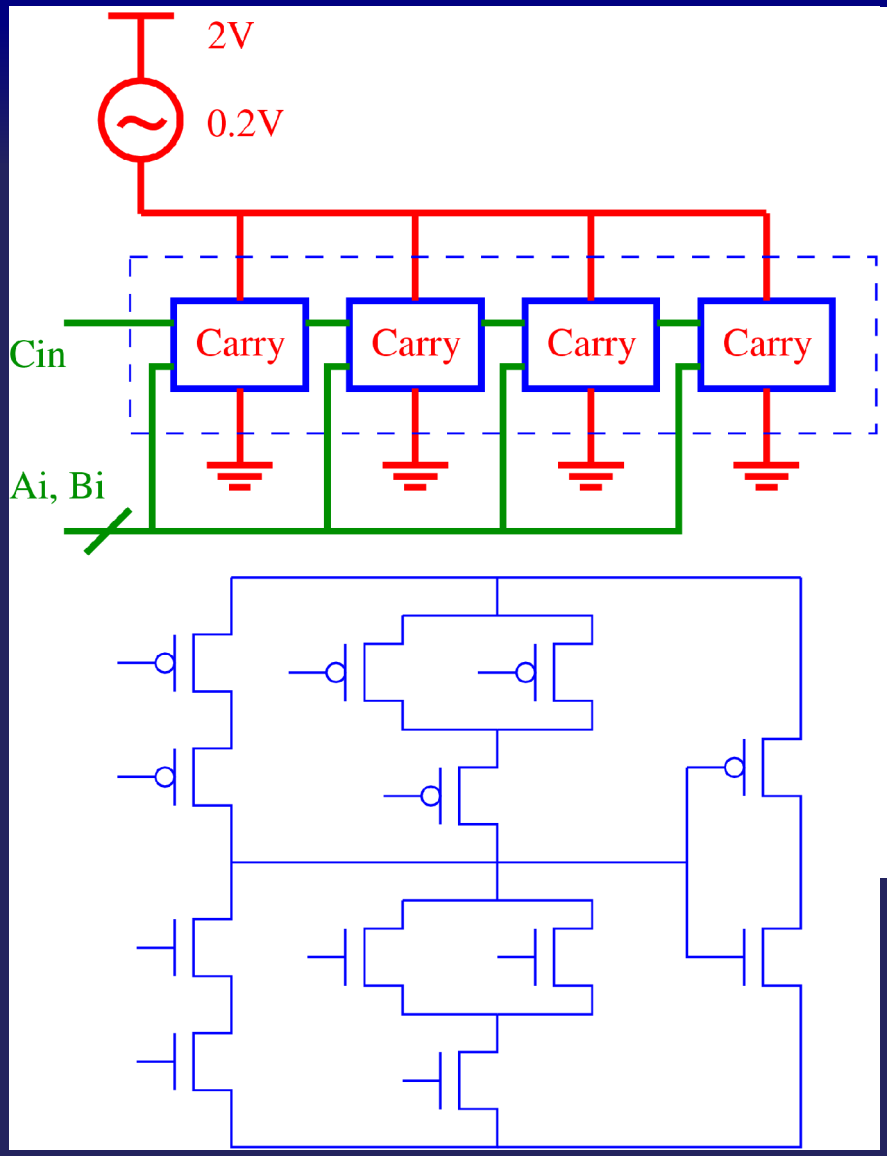
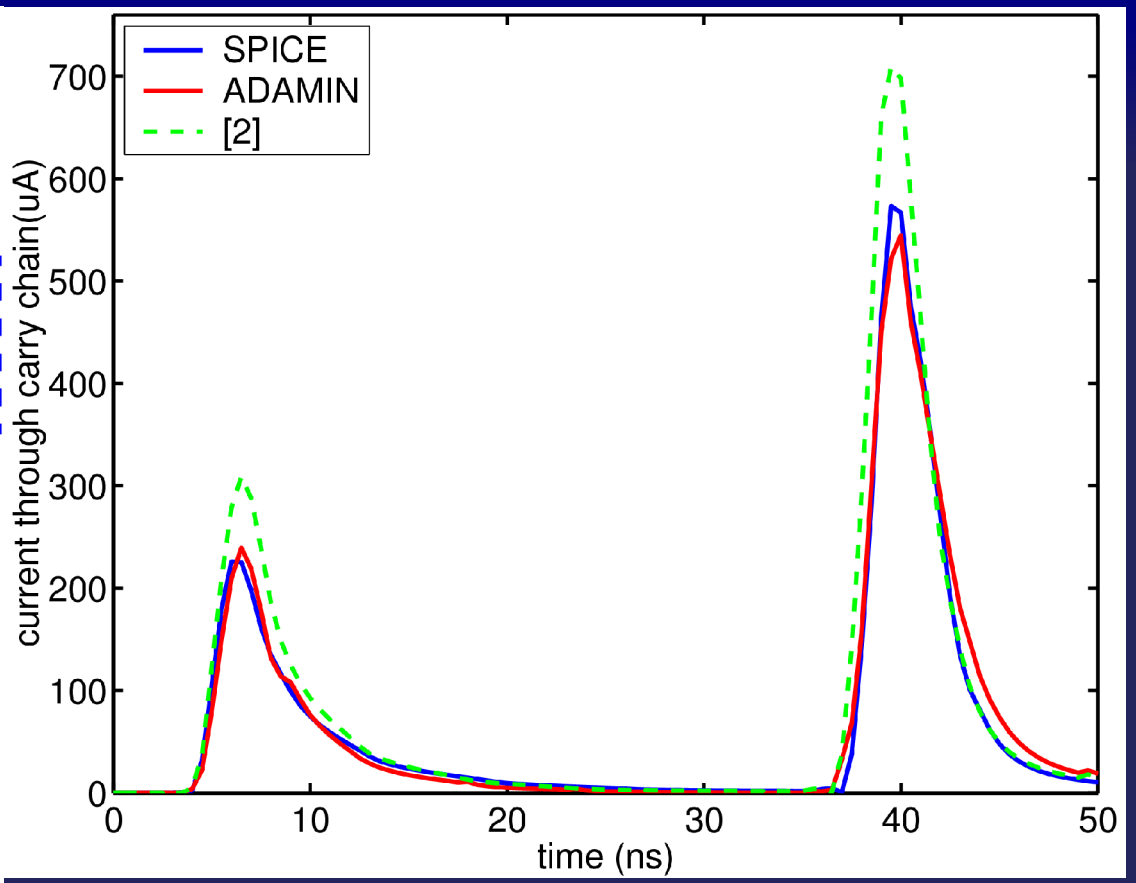
Supply-noise Induced Currents: Carry Chain





- Considerable accuracy improvement over current-source macromodel [Dharchoudhury 98]

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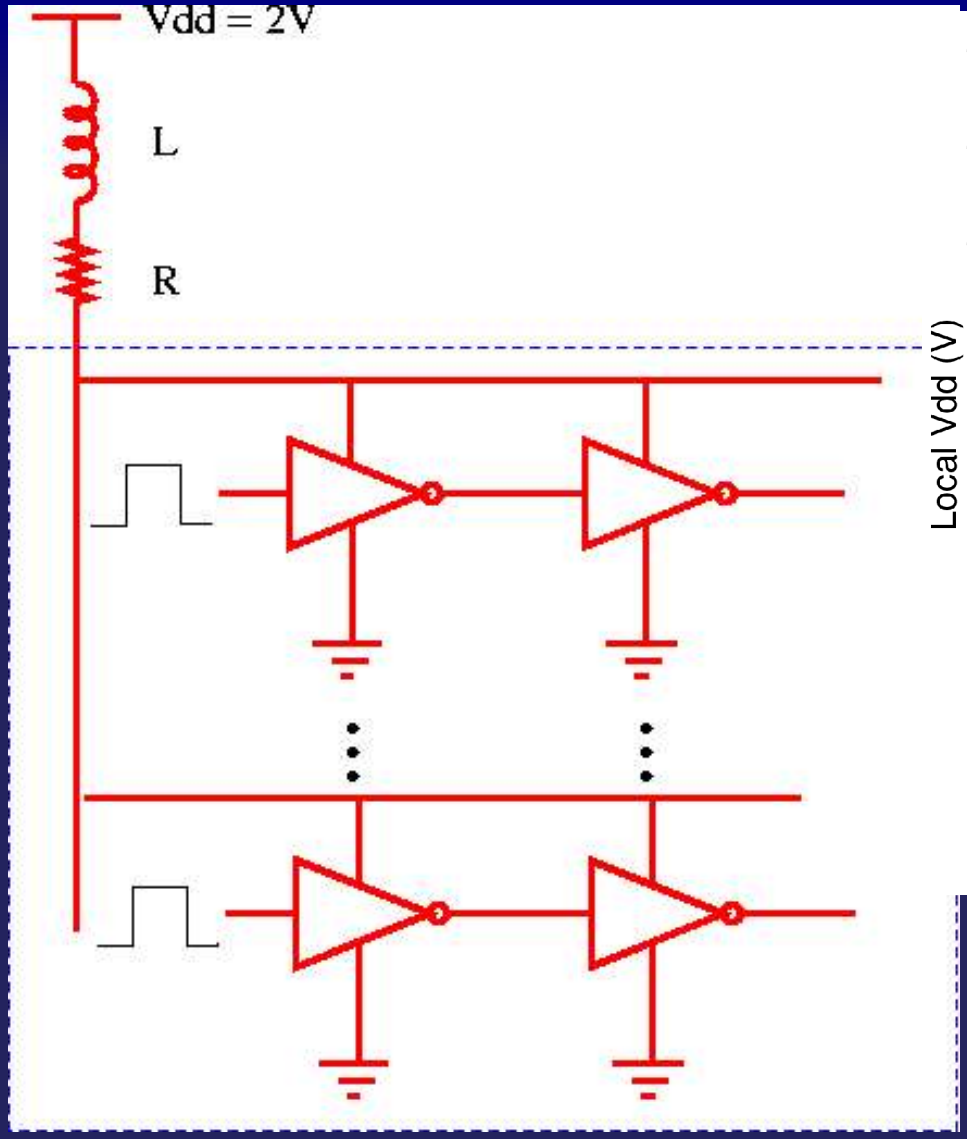
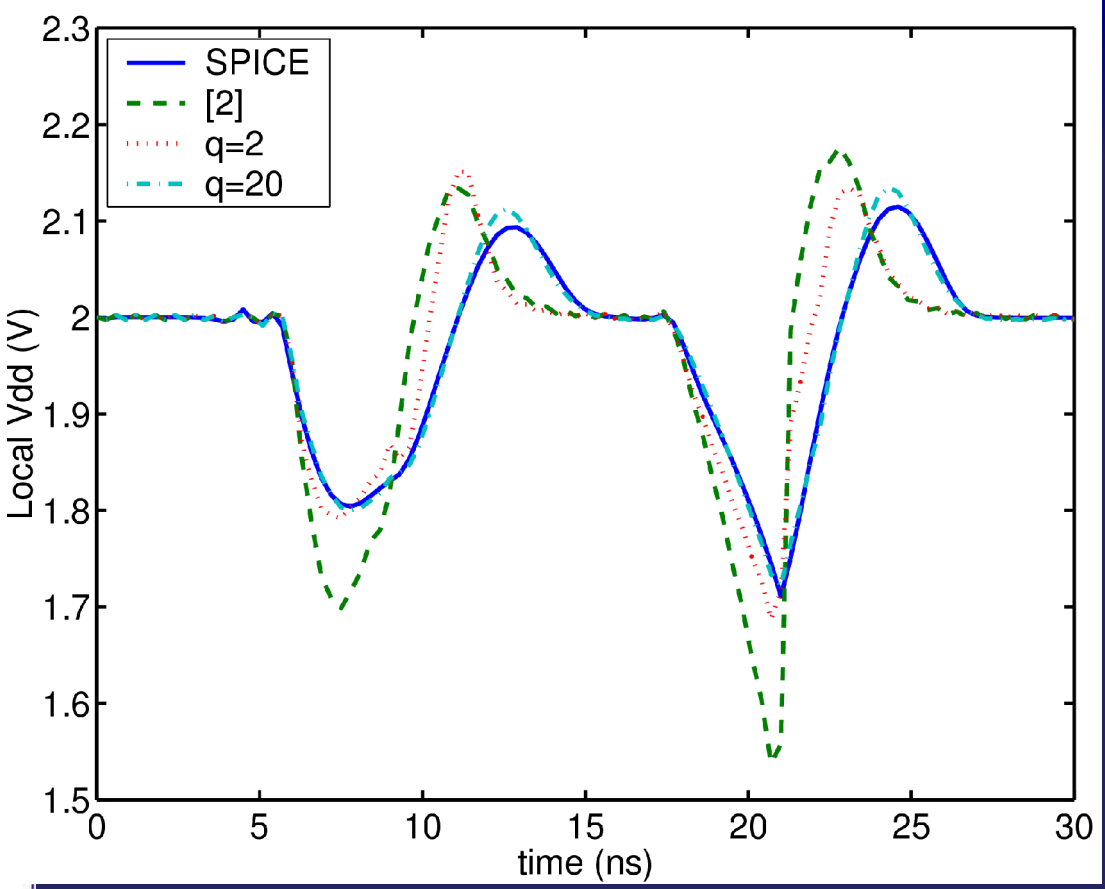
“System” Simulation with Inductive Supply





- size 2 MM: already better
- size 20: much more accurate
- 17000x speedup for 8000 gates

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Macromodelling Nonlinear Systems

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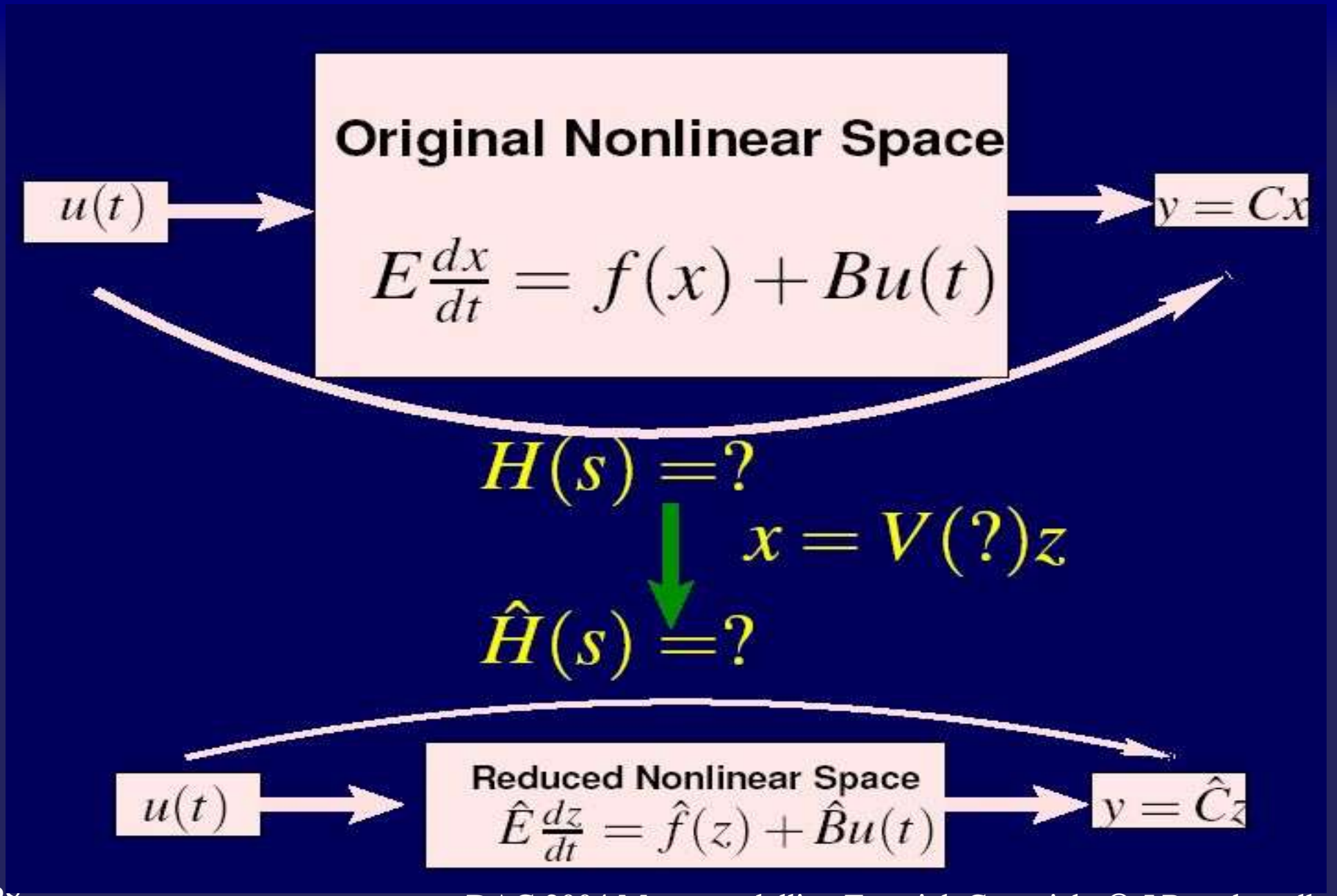
Nonlinear Macromodel Generation



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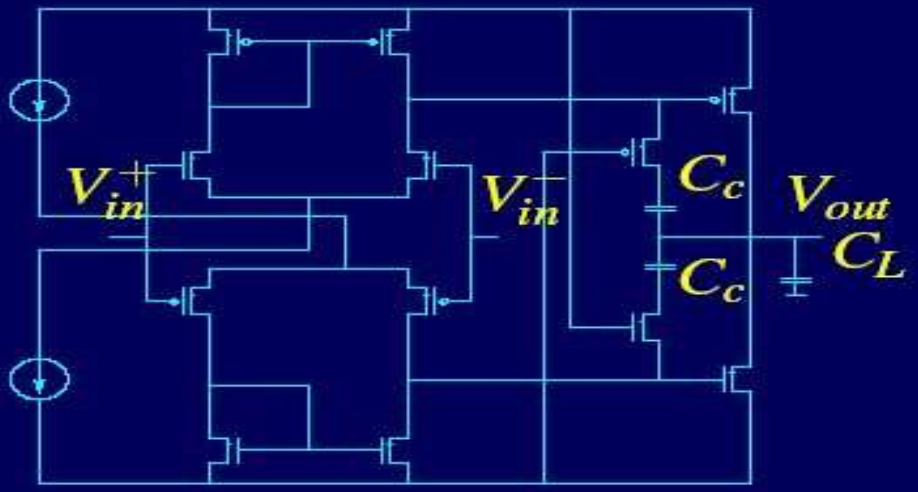
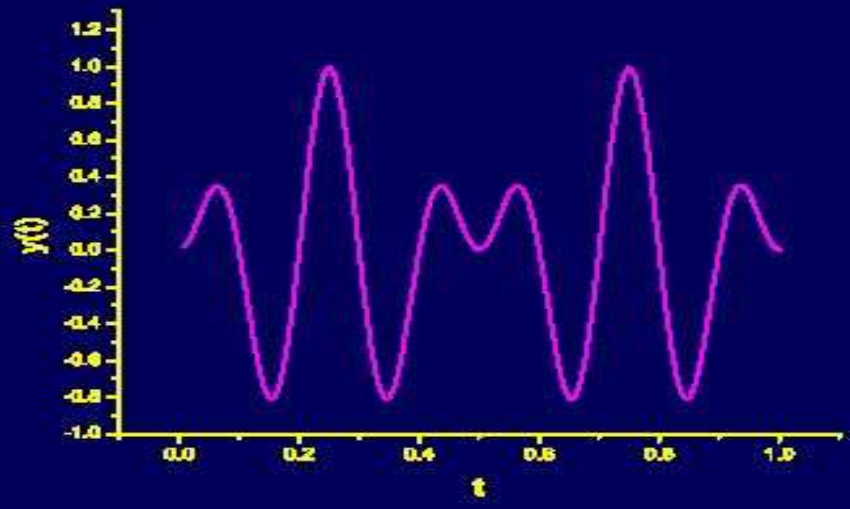
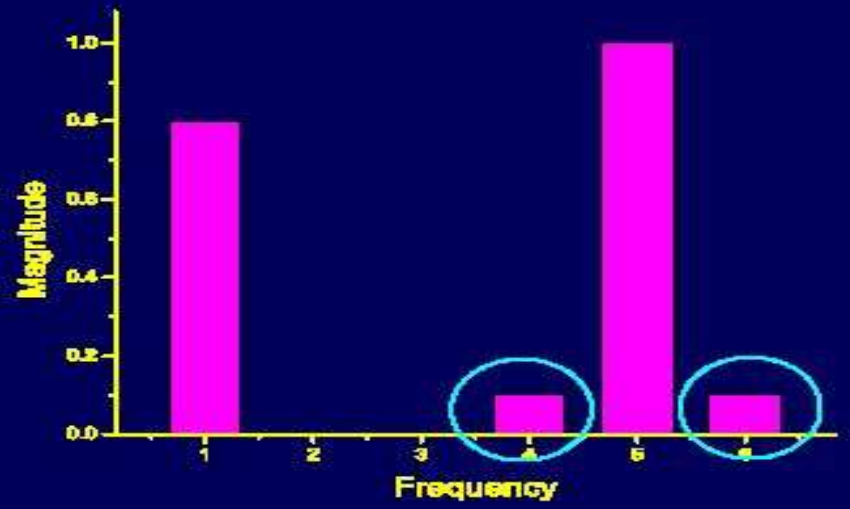
Weakly Nonlinear Systems







- Distortion, IM important!
- Must capture small distortion/IM

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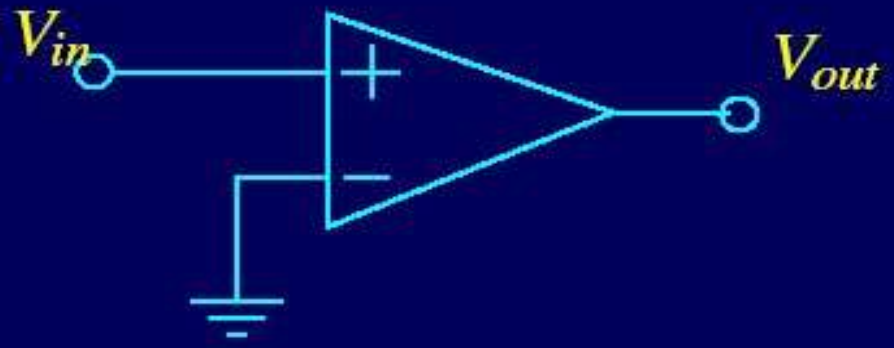
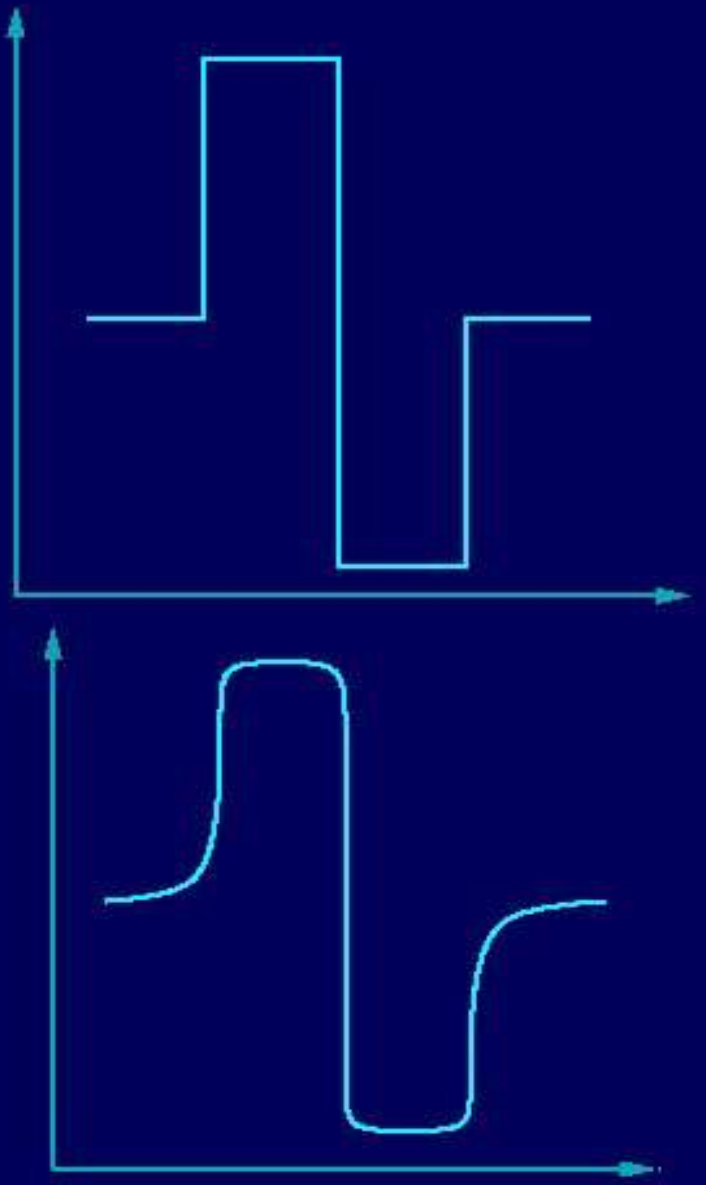
Strong Nonlinearities

Comparators, switching mixers





- Large signal clipping
- Must capture strong nonlinearities

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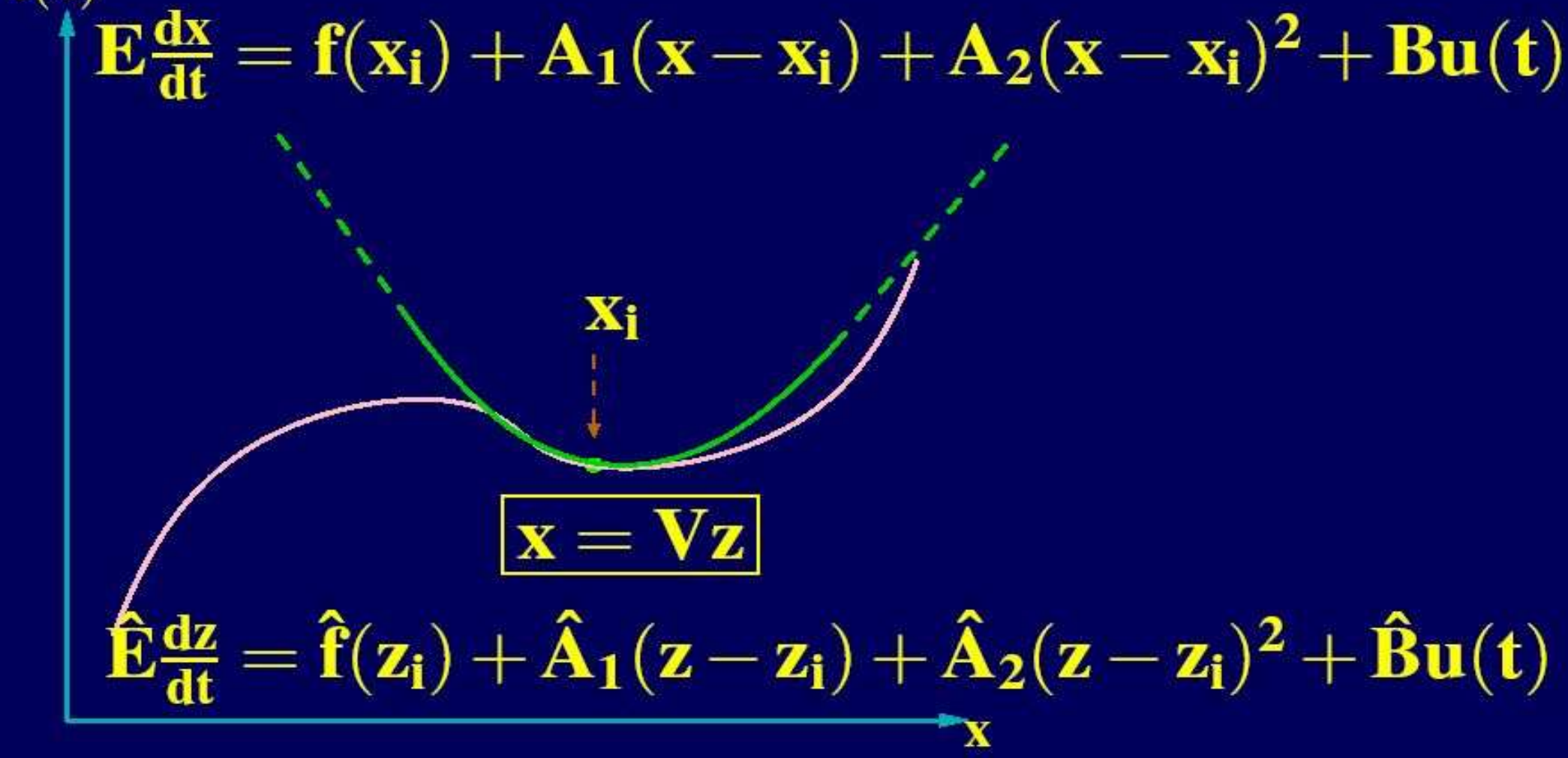
Polynomial (Volterra) Reduction

[Roychowdhury TCAS-2 99] [Phillips DAC 00] [Li/Pilleggi DAC 04]

$$E\frac{dx}{dt} = f(x_i) + A_1(x - x_i) + A_2(x - x_i)^2 + Bu(t)$$



- **Good for small distortion, Poor for large swing**

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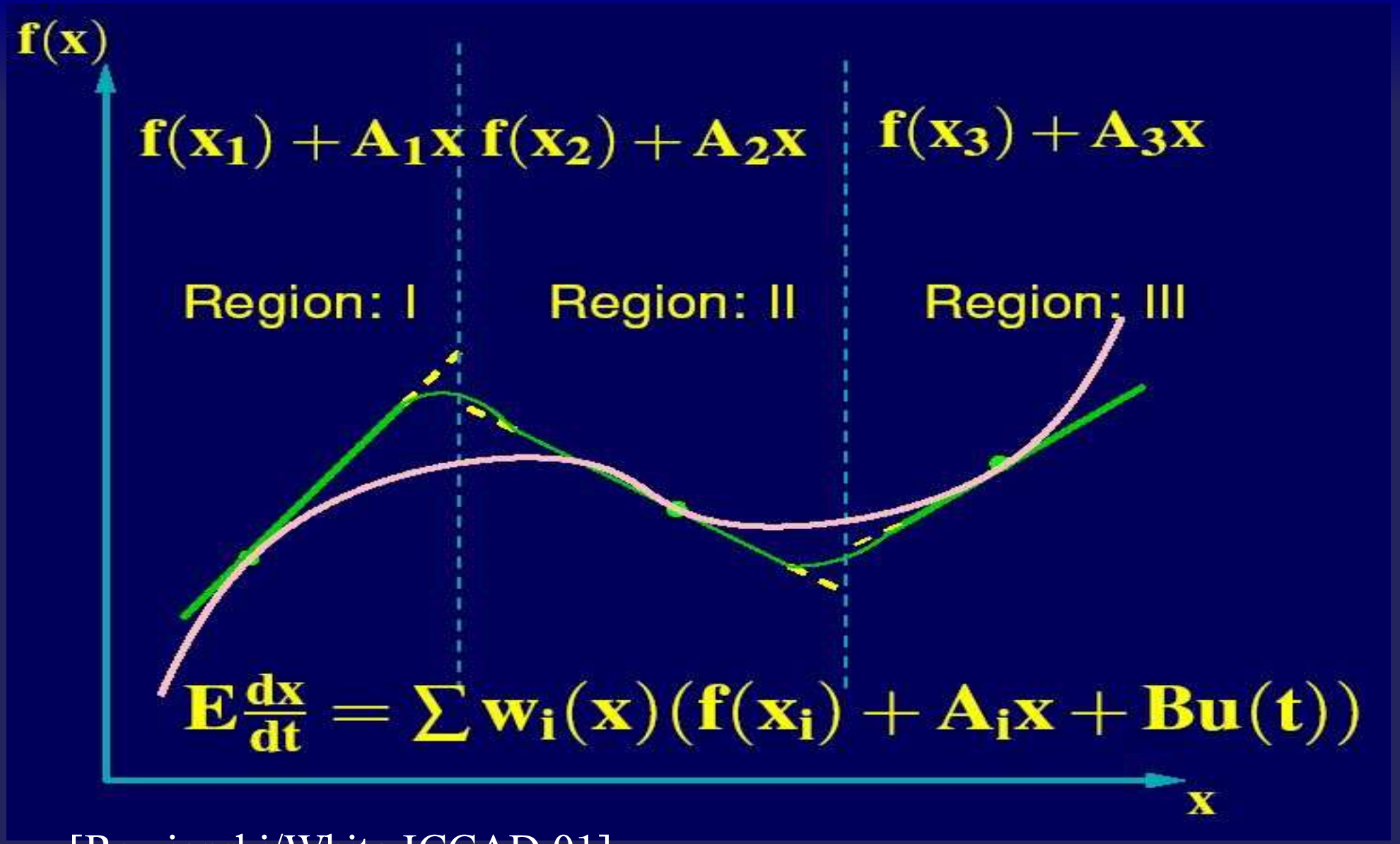
Trajectory Piecewise Linear MM



[Rewienski/White ICCAD 01]

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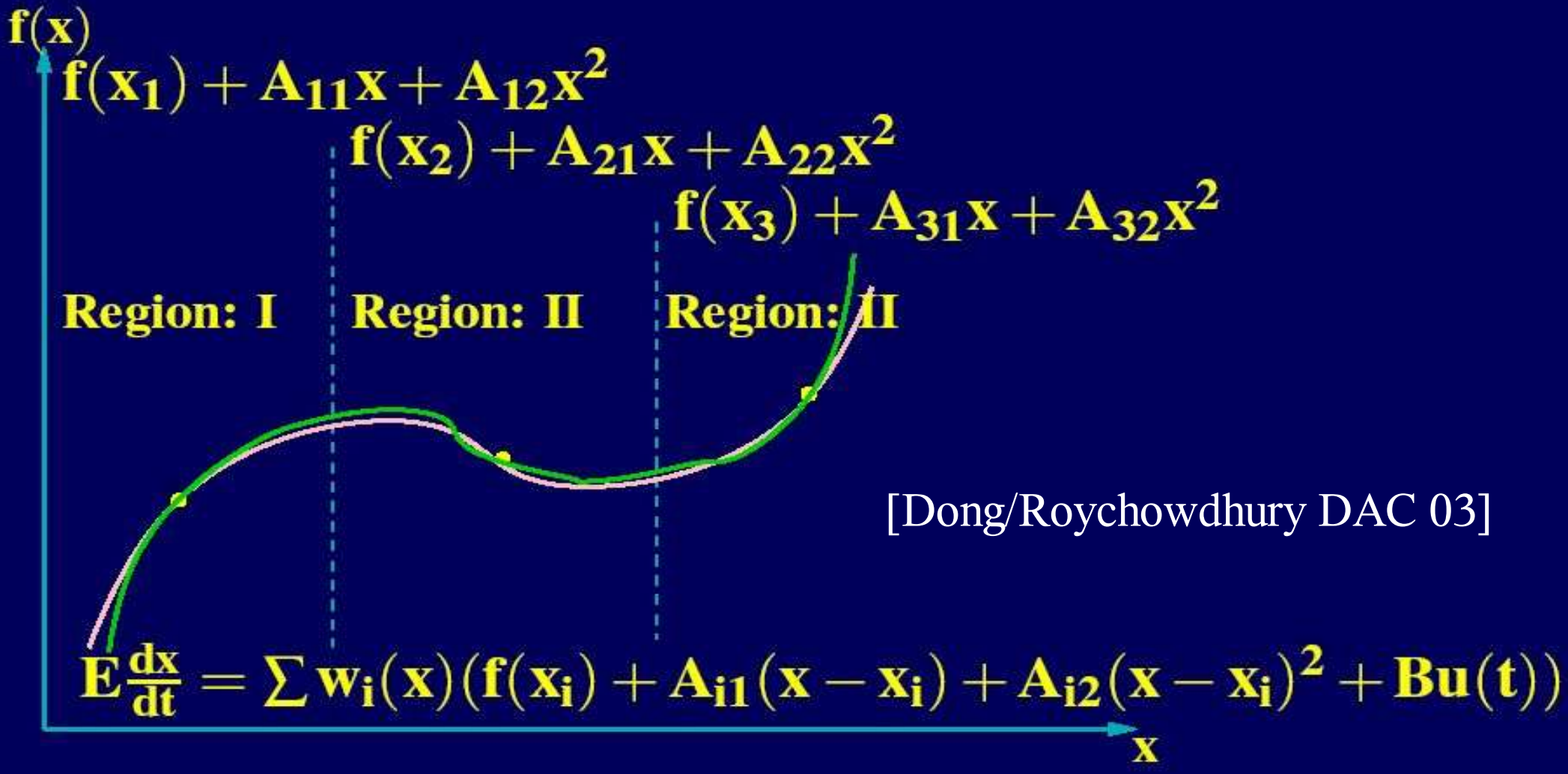
Piecewise Polynomial Macromodelling



[Dong/Roychowdhury DAC 03]

$$E\frac{dx}{dt} = \sum w_i(x)\left(f(x_i) + A_{i1}(x - x_i) + A_{i2}(x - x_i)^2 + Bu(t)\right)$$

- Good for small distortion, also good for large swing

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Drop-in Replacement Macromodels

- Design process typically runs many simulations
  - DC (sweep), AC, small-signal distortion, transient
  - time- and frequency-domain analyses
- Would like one extracted macromodel to work for all analyses
  - ie, a drop-in replacement for the original
  - PWP-generated macromodels: good candidates

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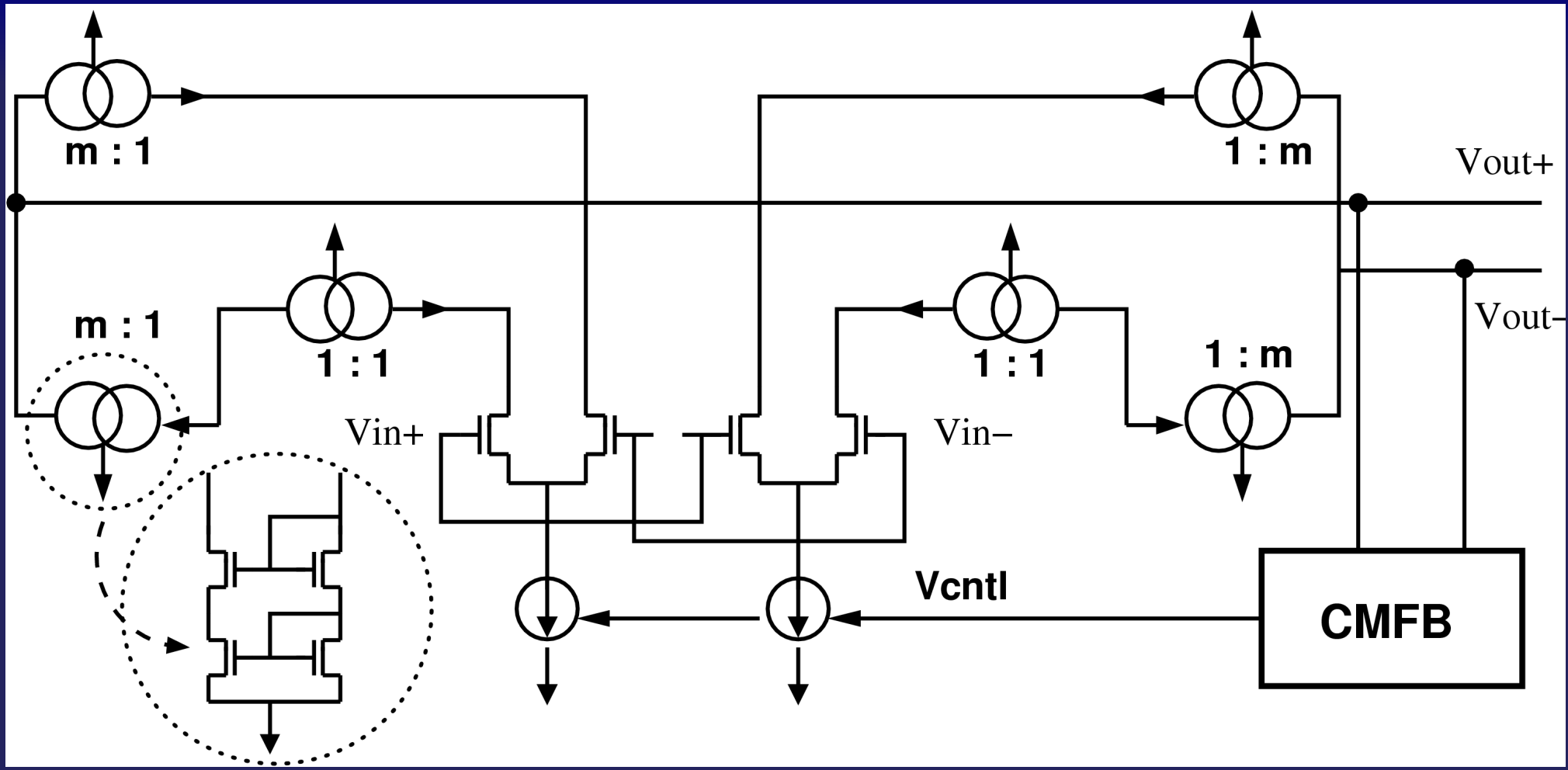
Current Mirror Op-Amp



Original: ~50 MOSFETs. Macromodel size: 19, 27 regions

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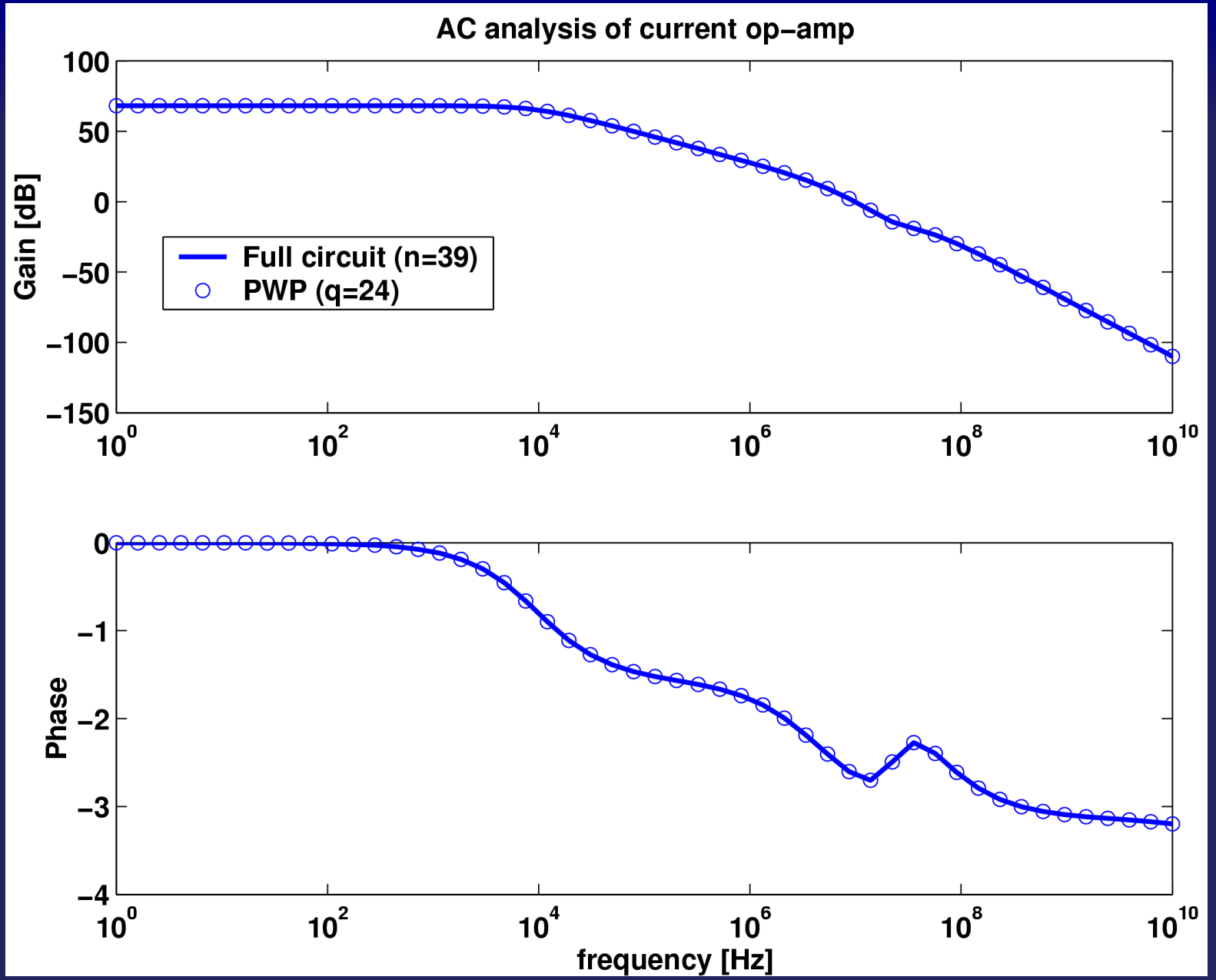
Macromodel vs Original: AC Sweep 1



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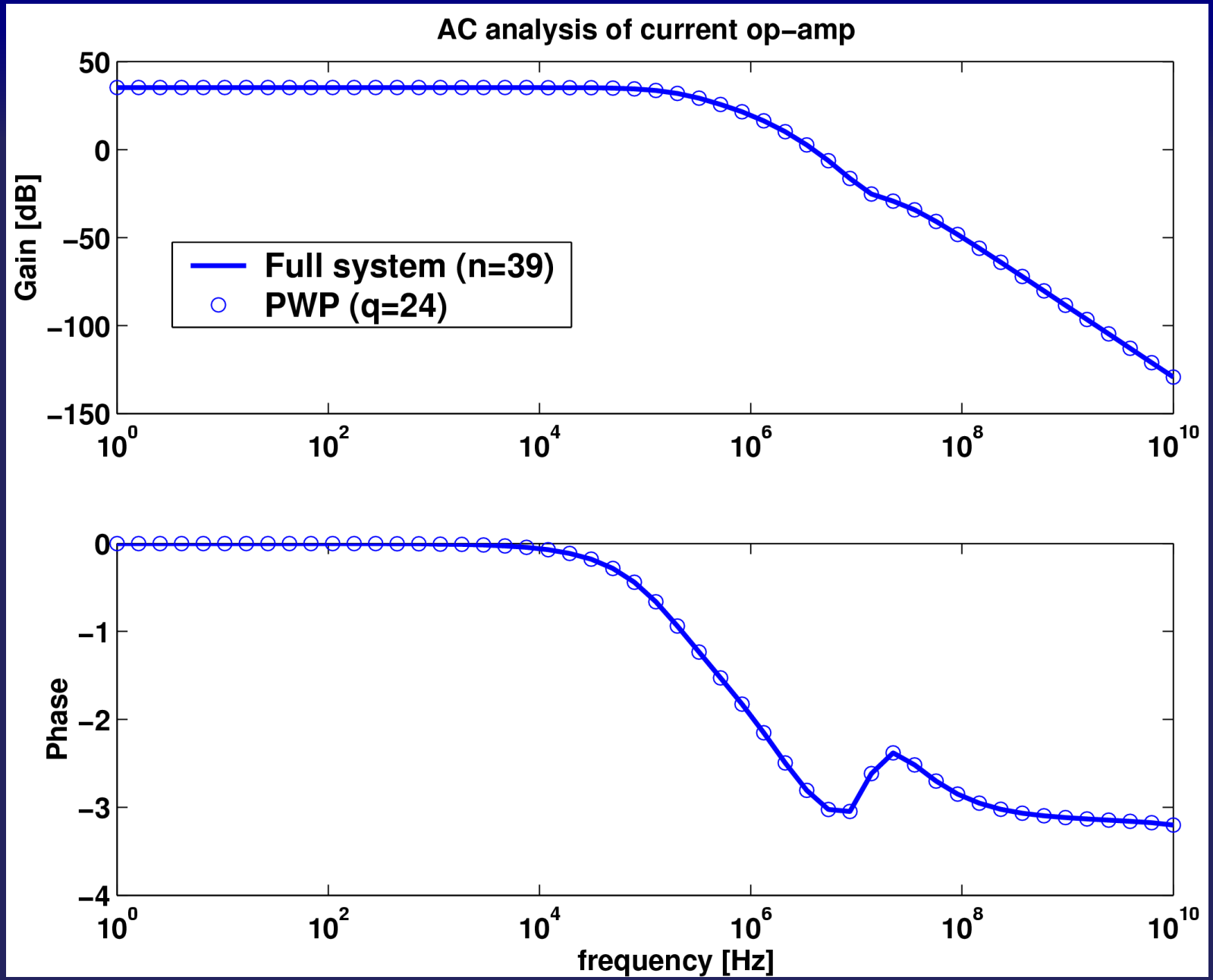
Macromodel vs Original: AC Sweep 2



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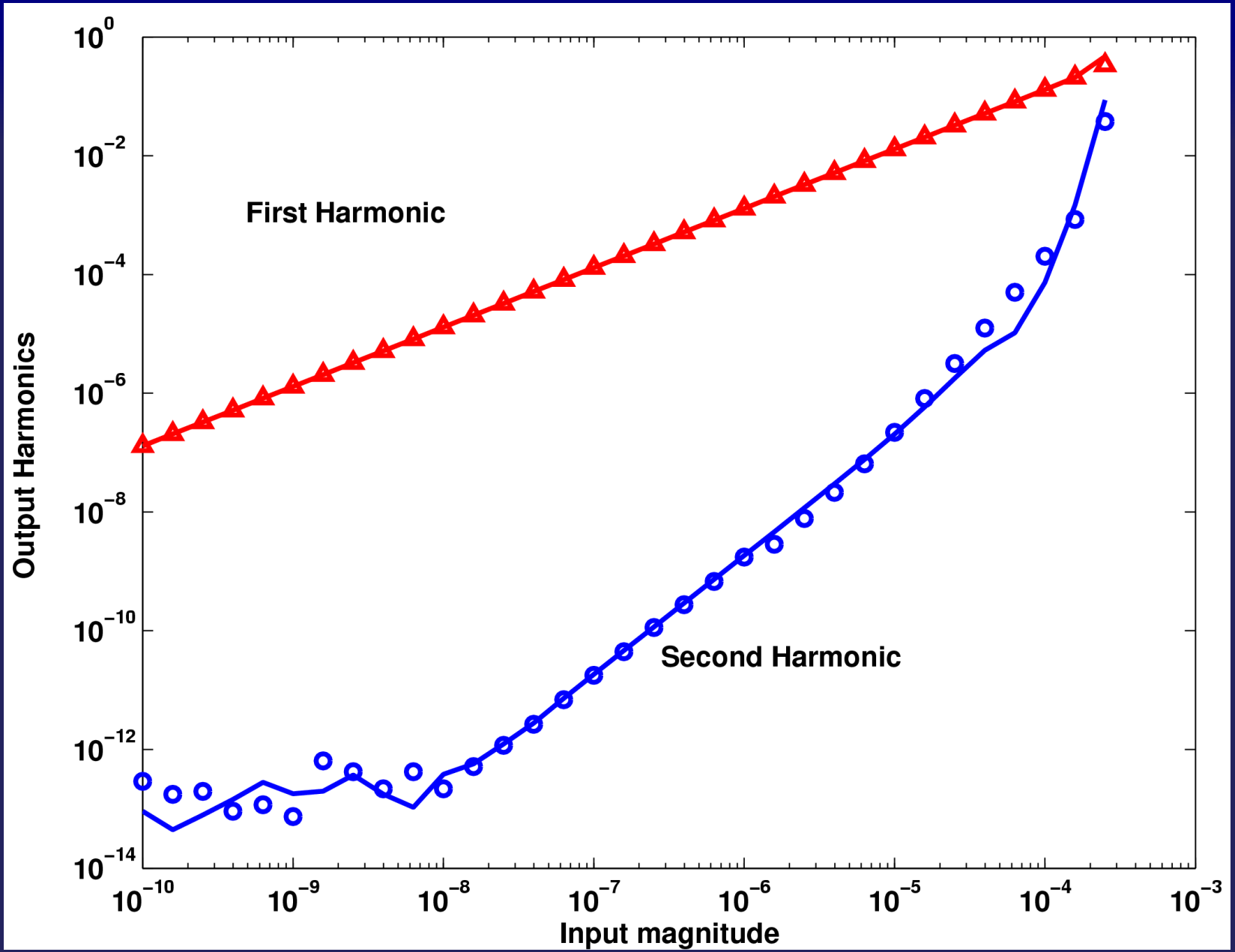
Macromodel vs Original: Distortion



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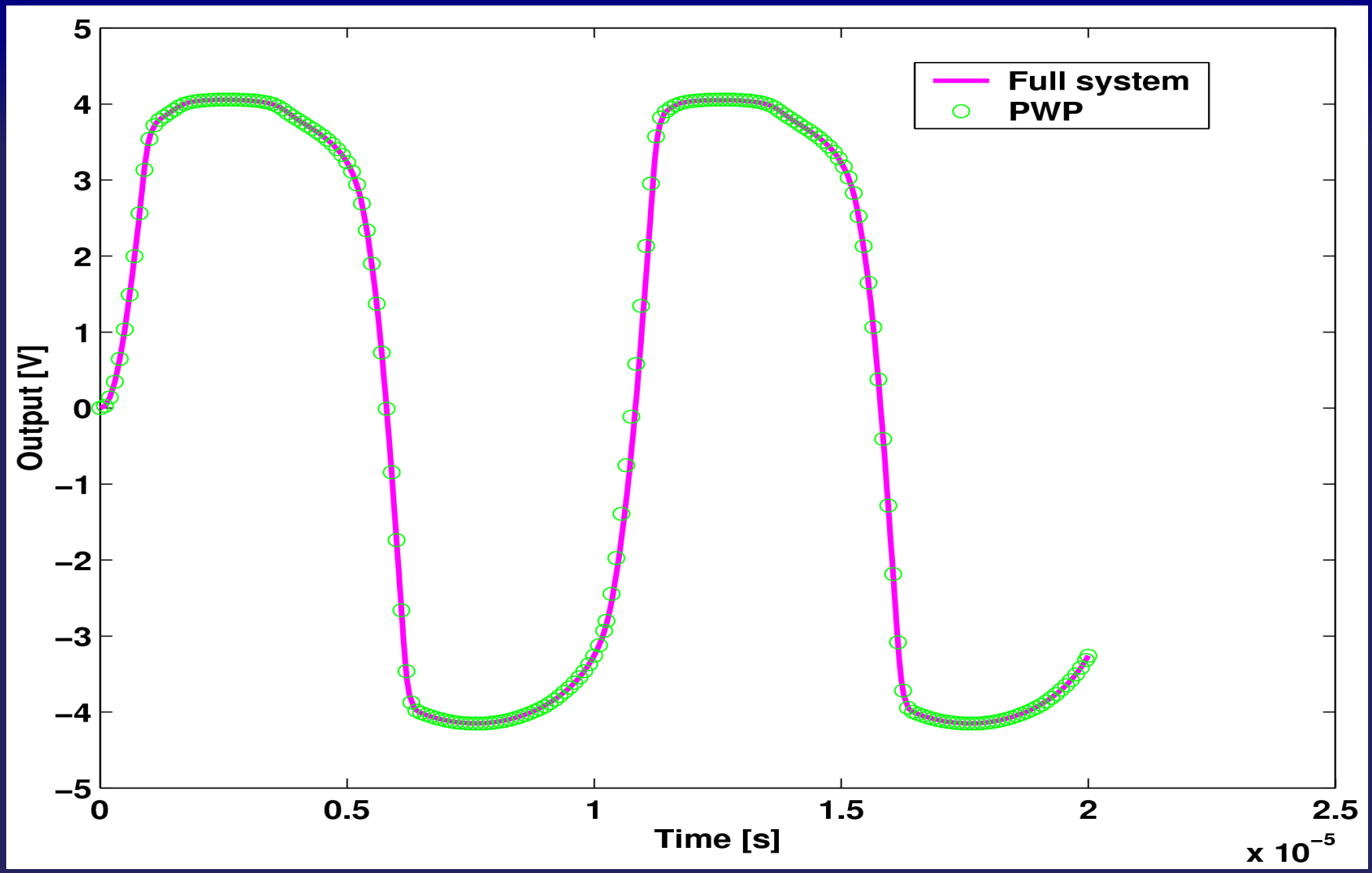
Macromodel vs Original: Transient



- ***speedup: 41x over original***

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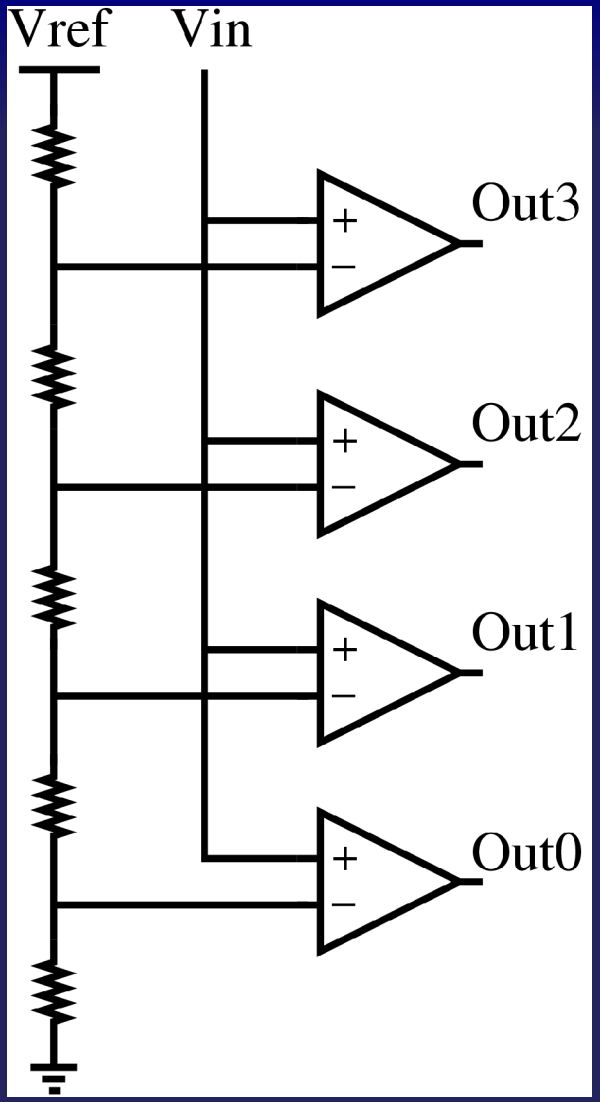
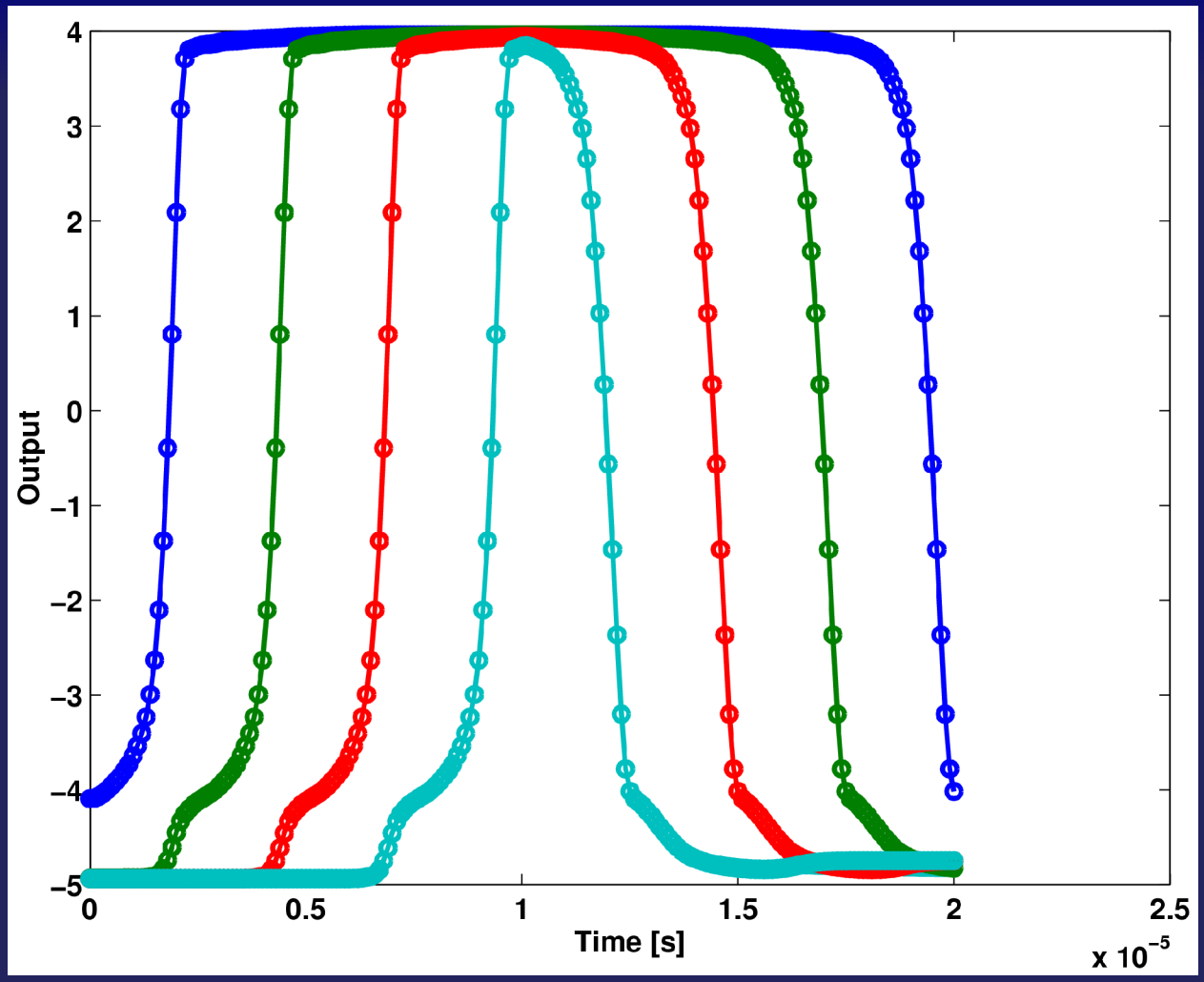
Small ADC: System-level Simulation





Excellent match between original and macromodel

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Macromodelling Oscillatory Systems

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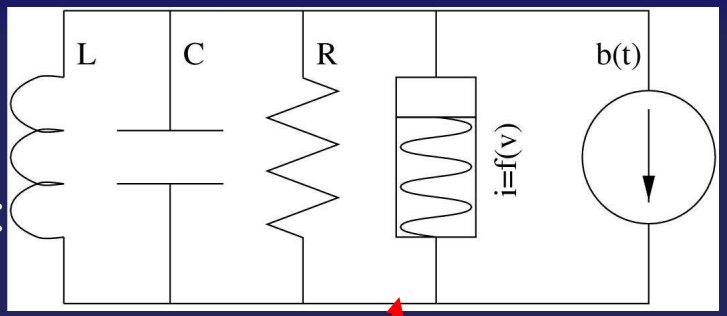
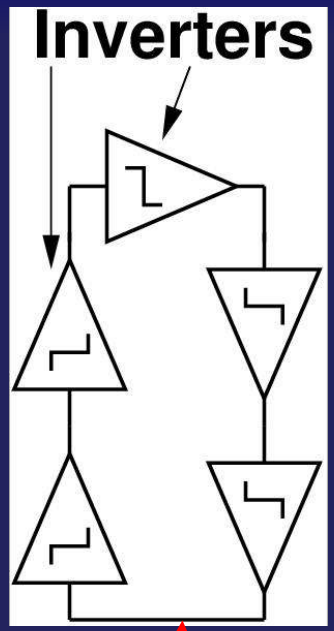
Oscillators

- Oscillators are critical in communication systems:
  - LC oscillators
  - Ring oscillators
  - Used everywhere:
    - VCOs, PLLs
    - CDR ckts
    - synchronization loops
  - ***Very slow*** to simulate
  - ***Noise prediction problematic***
- Needed:
  - Accurate/fast oscillator macromodelling capability
  - Accurate oscillator jitter/phase noise prediction



-ve feedback LC oscillator



Ring oscillator

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Why Oscillators are a Special Simulation Challenge

- Computation/size/accuracy: much greater than amps/mixers
- Even 1-transistor oscillators (eg, UHF oscs, >100GHz)
  - long startups, tiny timesteps needed
- On-chip RF: 100s to 1000s of transistors
  - VERY challenging to simulate
- Macromodelling offers dramatic speedup
  - Even for 1-transistor oscillator
- Oscillators feature complex phenomena: injection locking
  - oscillator's frequency “locks” to frequency of external input
  - if frequencies close enough, even if input is very small
  - can take extremely long to simulate
  - universal phenomenon: grandfather clocks, fireflies flashing, etc

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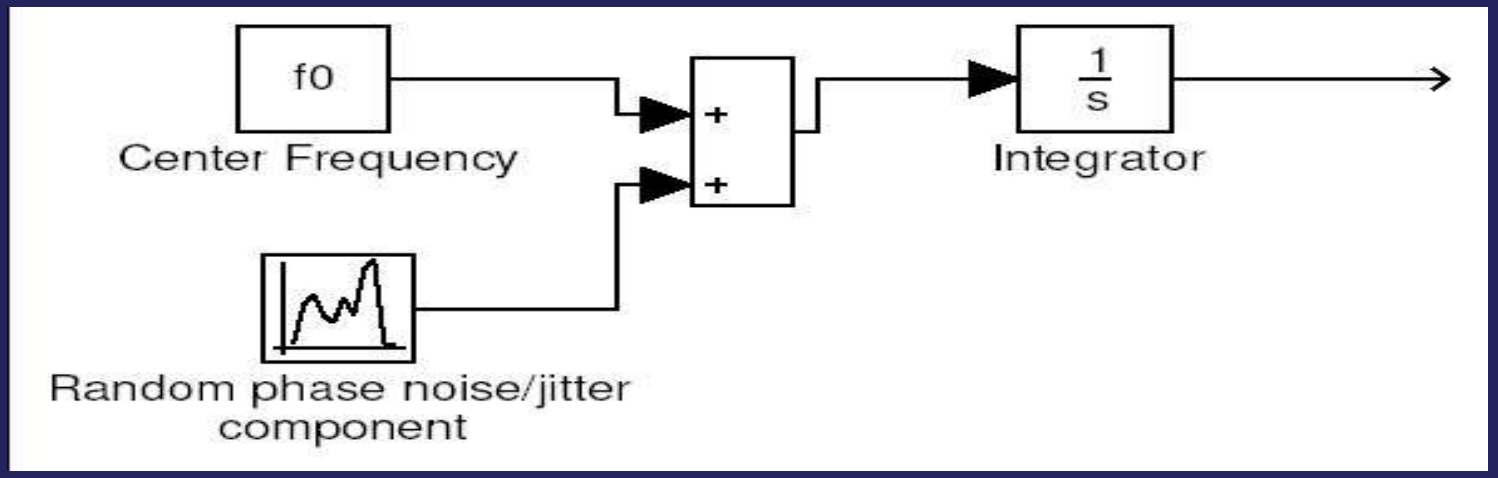
Limitations of Linear Macromodels

- Input to output relationship: **linear**



- **Does not capture important phase phenomena correctly**
  - Eg, injection locking, noise spectrum
  - Manually generated (tedious, error-prone, ...)

[Stensby] [Kundert 02]

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Automated Nonlinear Oscillator Macromodelling

- Nonlinear: **accurate** I/O capture
  - Injection locking, phase noise spectrum, ...
- Automated generation
  - **SPICE in, macromodel out (Verilog-A, MATLAB, SPICE, etc)**
- Small size
  - **Very fast to simulate compared to full SPICE oscillator circuit**

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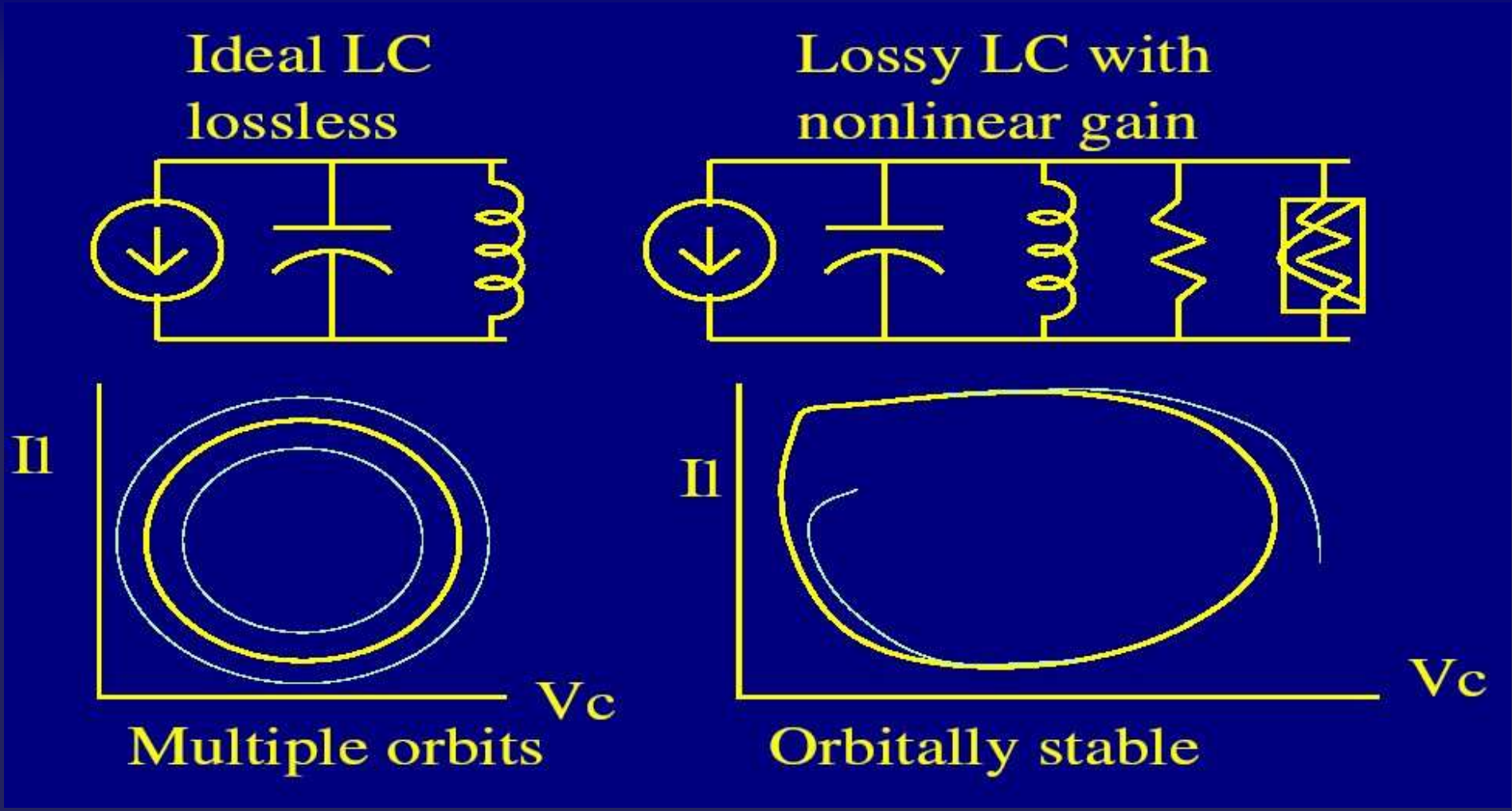
“Ideal” vs Orbitally Stable Oscillators



Nonlinearity cannot be ignored – fundamental to oscillator operation

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Quantifying Oscillator Response

How does the oscillator (VCO) respond to "inputs"?

$$\dot{x}(t) = f(x) + \underbrace{b(t)}_{\text{input perturbation}}$$

- No perturbation $\Rightarrow$ perfect periodic solution $x_s(t)$
- Small $b(t)$ perturbation:

$$x(t) = x_s(t + \underbrace{\alpha(t)}_{\text{growing phase error}}) + \underbrace{y(t)}_{\text{small}}$$

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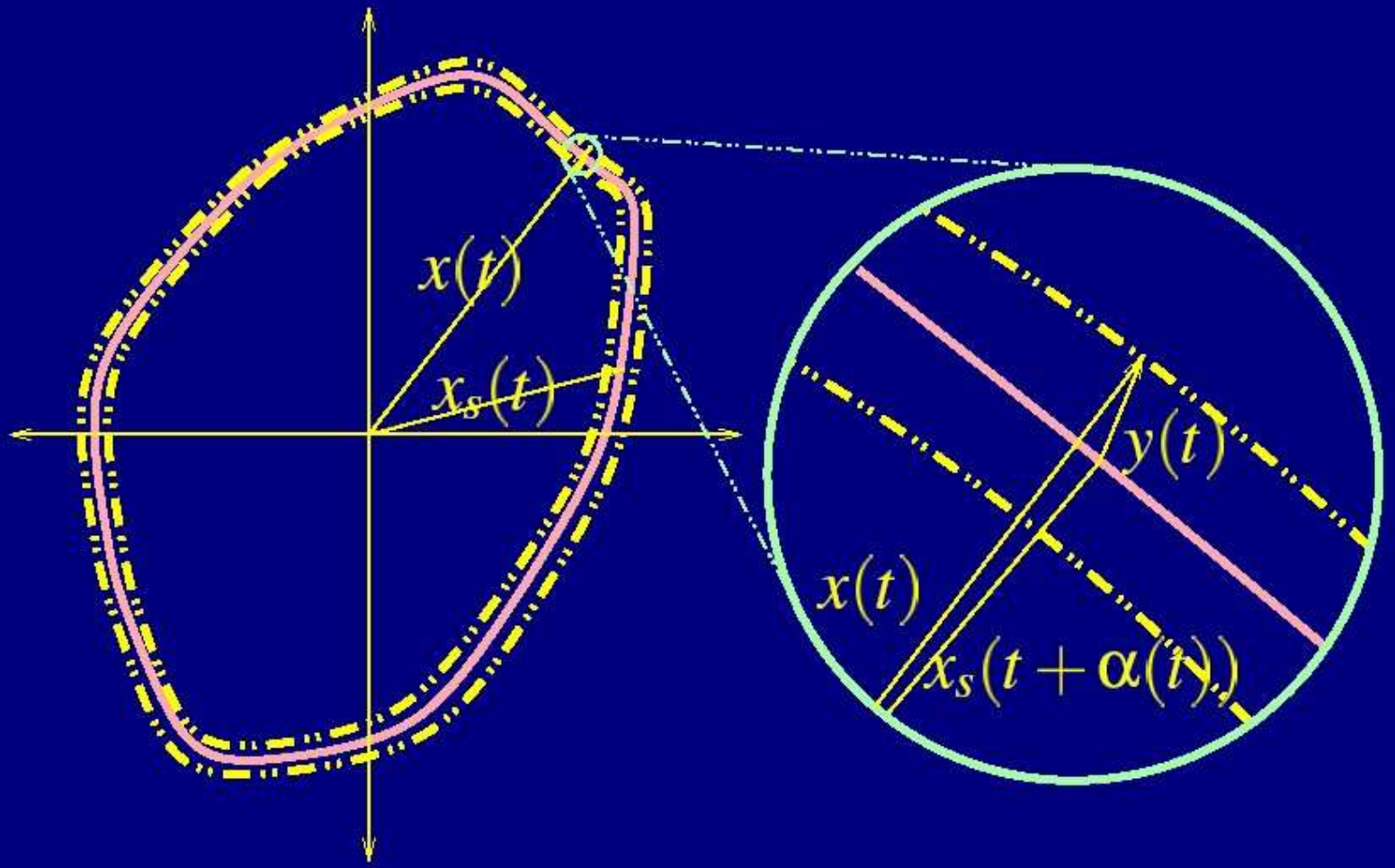
Oscillator: Response to "Inputs"



- Phase error $\alpha(t)$ *shifts track increasingly along limit cycle*
- $y(t)$ creates deviations from limit cycle that *remain small*

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Nonlinear Differential Equation for Phase

$$\dot{\alpha}(t) = v_1(t + \alpha(t)) \cdot b(t)$$

- *Scalar, nonlinear ODE* governs $\alpha(t)$
- $v_1(\cdot)$ is the *Perturbation Projection Vector (PPV)*
- *Projection* of noise perturbation onto PPV determines phase error growth
- PPV is *not obviously related* to anything!
  - periodic Floquet eigenvector of time-varying (linearized) adjoint system
  - PPV can be found from *purely LPTV analysis*
- But: periodicity of PPV makes α equation nonlinear

[Demir Mehrotra Roychowdhury 97, 01]

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The Perturbation Projection Vector

- $v_1(t)$: "transfer function" relating "input" to oscillator phase response
  - termed the PPV: Perturbation Projection Vector
  - procedure for calculating the PPV is not obvious
    - but computationally efficient
  - In general, PPV does NOT equal the tangent vector of the phase plane plot
    - ie, not equal to the "ISF" [Hajimiri 98]

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Computing the PPV

- PPV can be computed efficiently from oscillator steady-state quantities
  - first: find the periodic steady-state of oscillator
    - using, eg, HB, shooting, etc.
  - then obtain the same G(t) and C(t) used in LTV reduction
  - form a large block matrix A from "samples" of G(t) and C(t)
  - perform one single linear matrix solution with A
    - can be performed efficiently for large oscillators

[Demir Roychowdhury TCAD 03]

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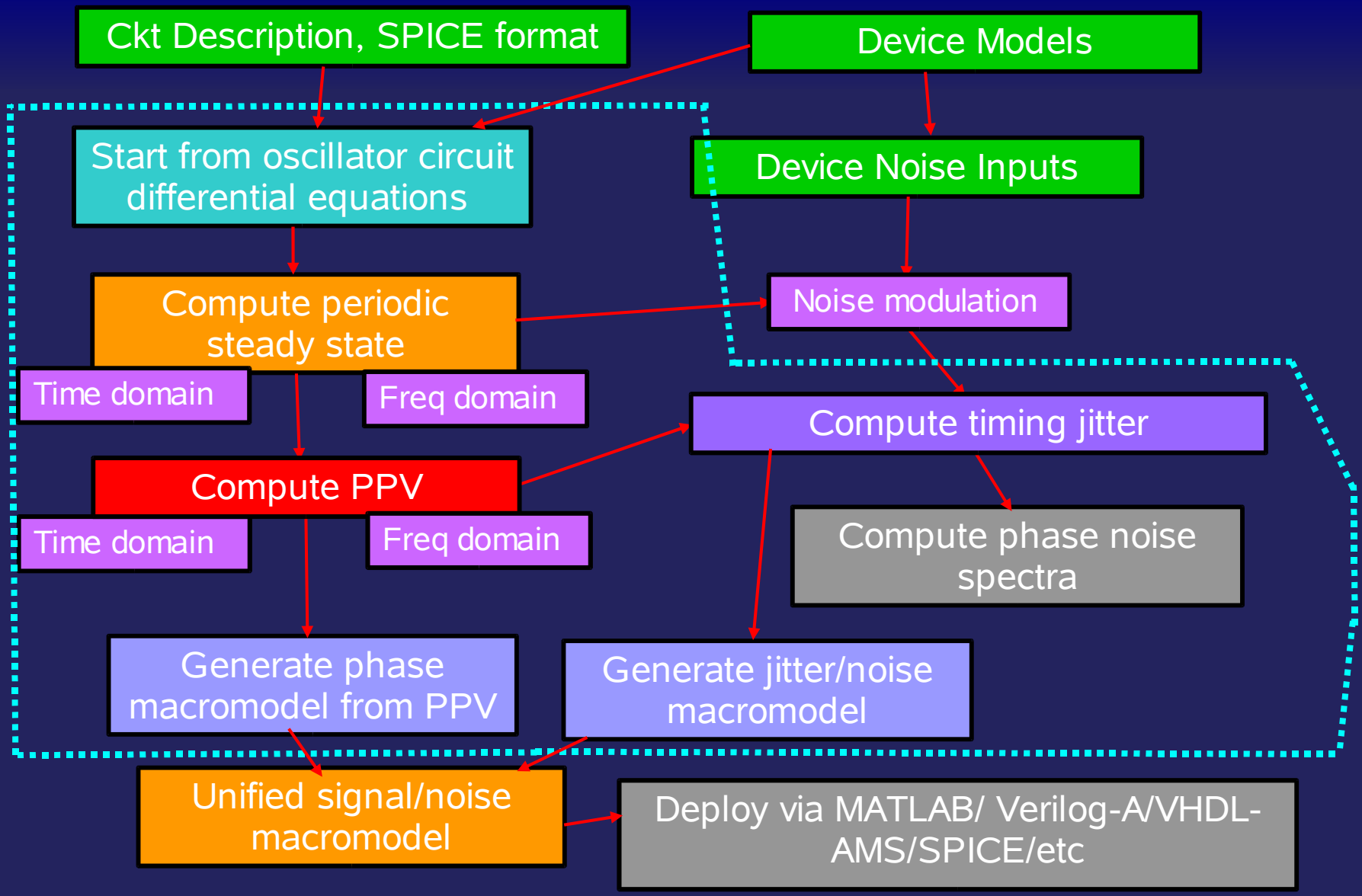
Oscillator Macromodelling Steps



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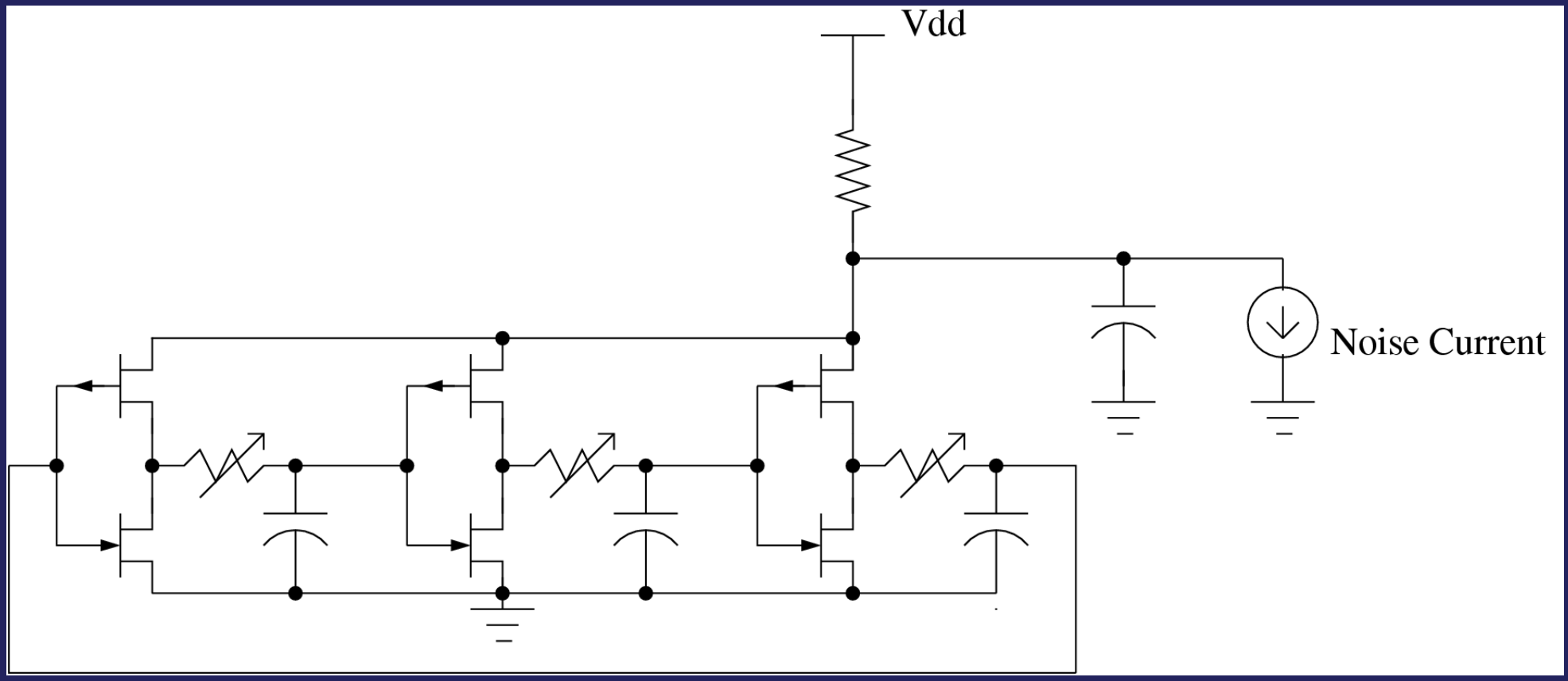
Example: Ring-Oscillator based VCO



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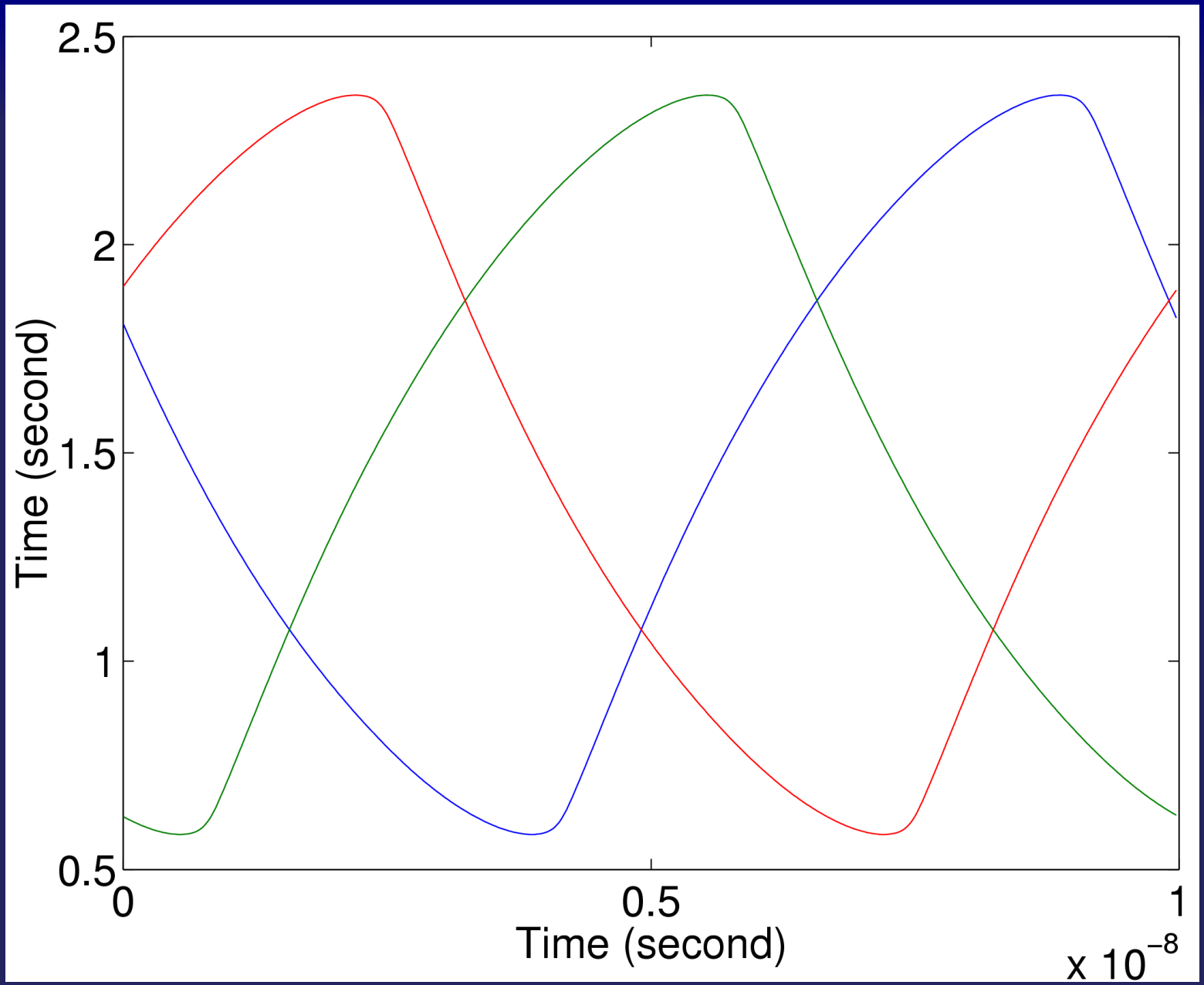
Ring Oscillator VCO: Steady State Oscillation



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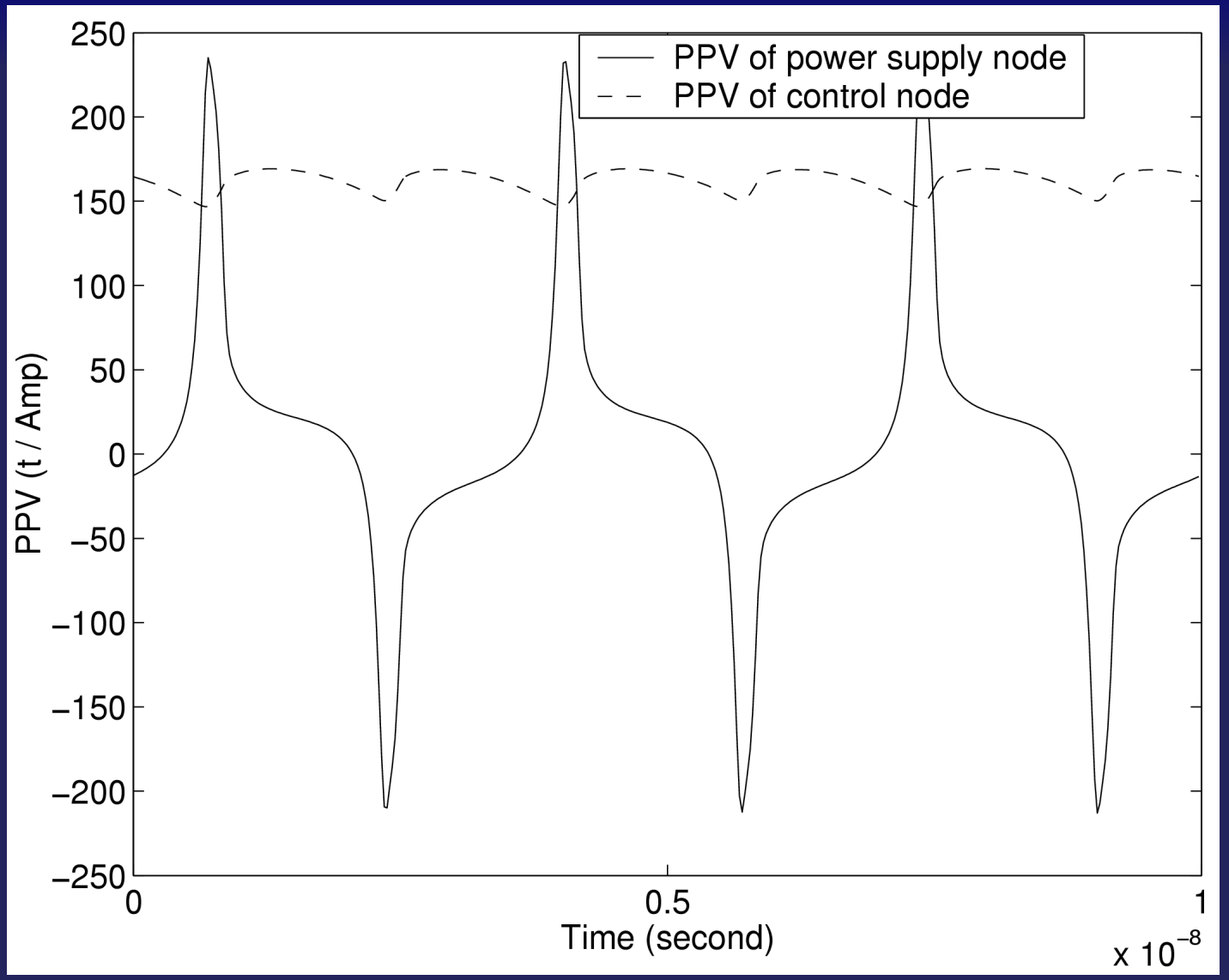
VCO Perturbation Projection Vectors: Control Node and Power Supply Components



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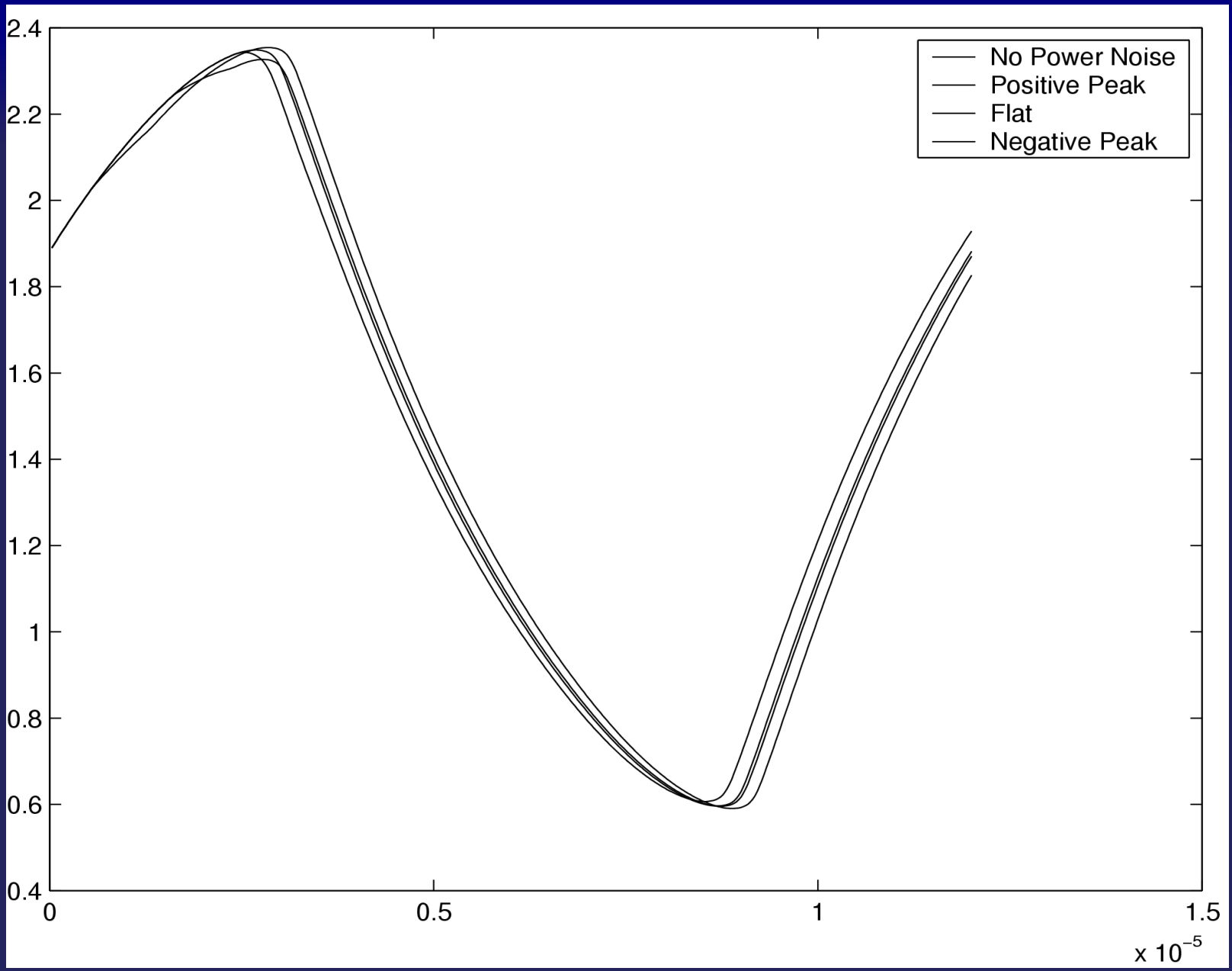
Ring Oscillator VCO: Shifts due to Supply Noise



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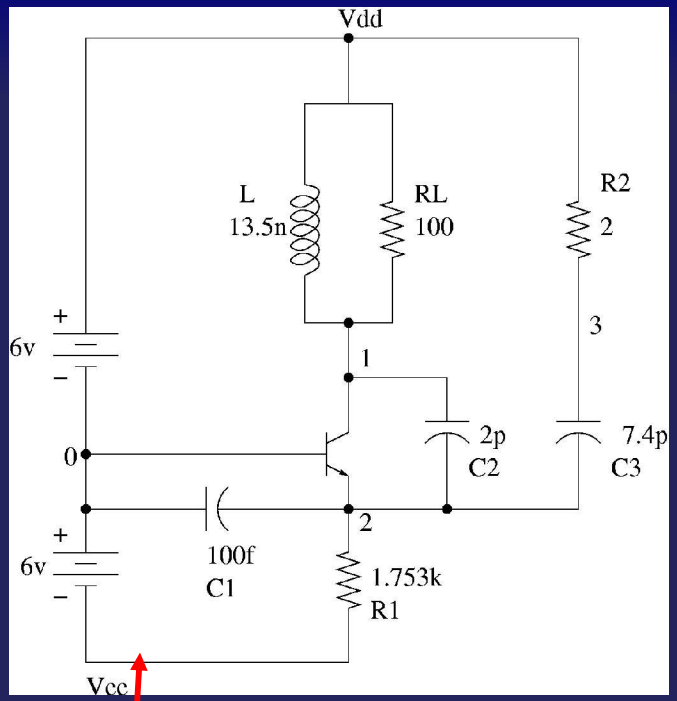
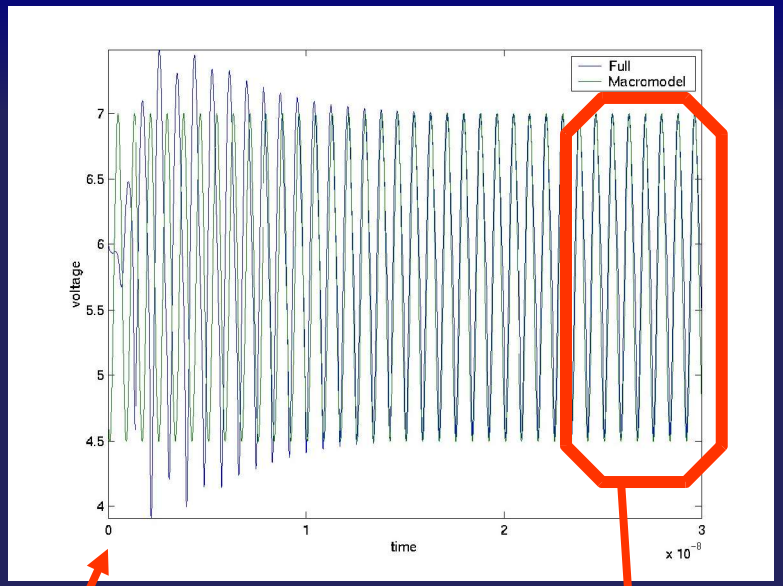
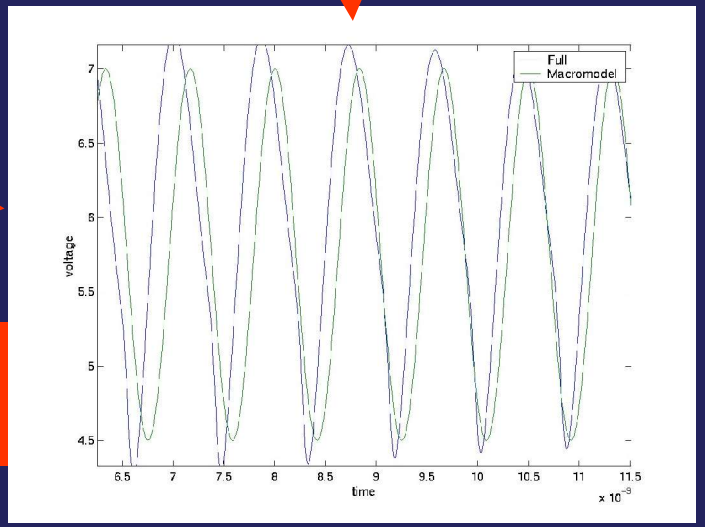
Capturing Injection Locking in a Colpitts (LC) Oscillator







Colpitts oscillator

Full simulation vs macromodel

- ***89x speedup over original***

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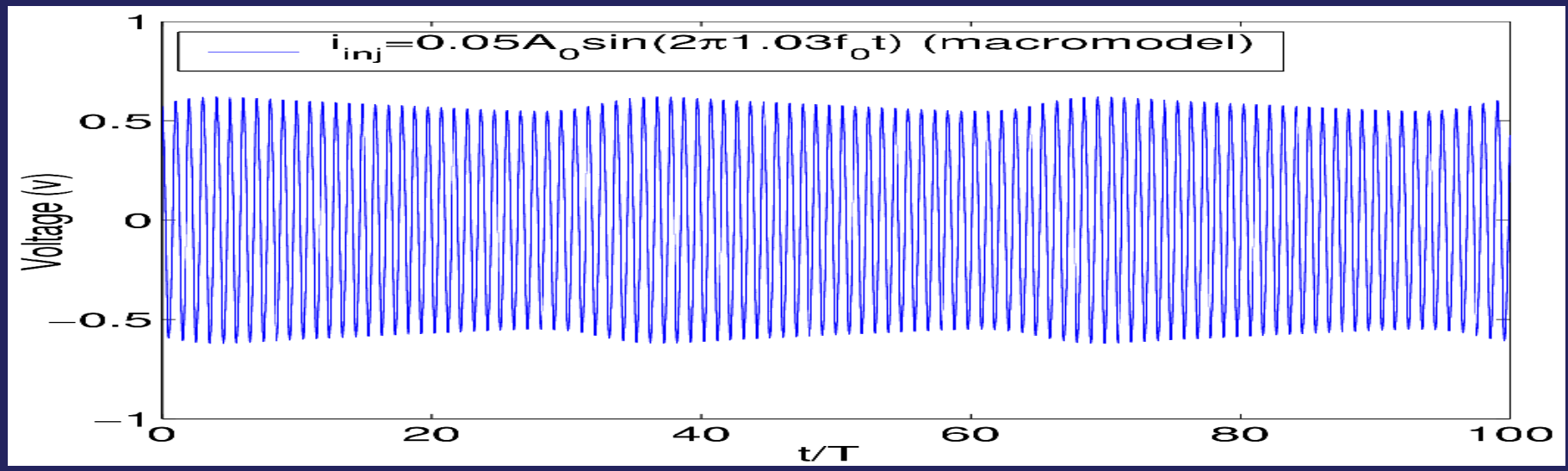
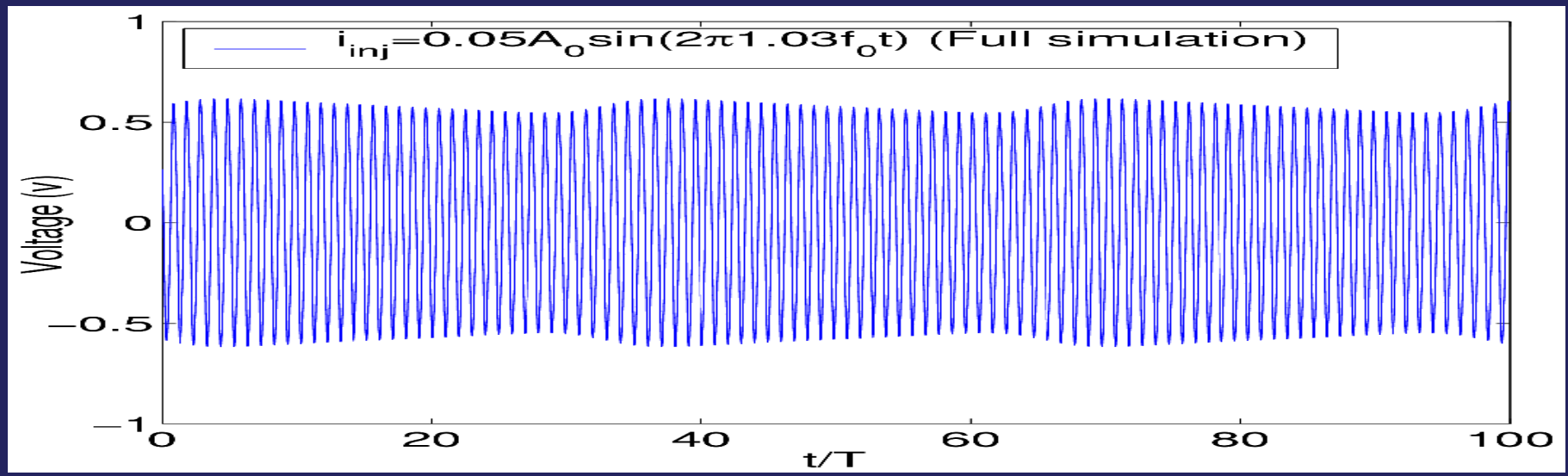
Capturing Amplitude Changes

- ***nonlinear phase + amplitude components (via LTV reduction)***





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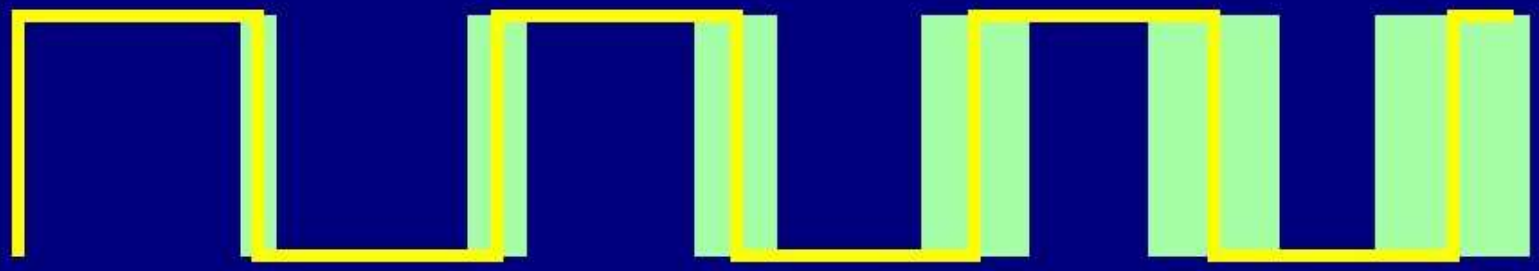
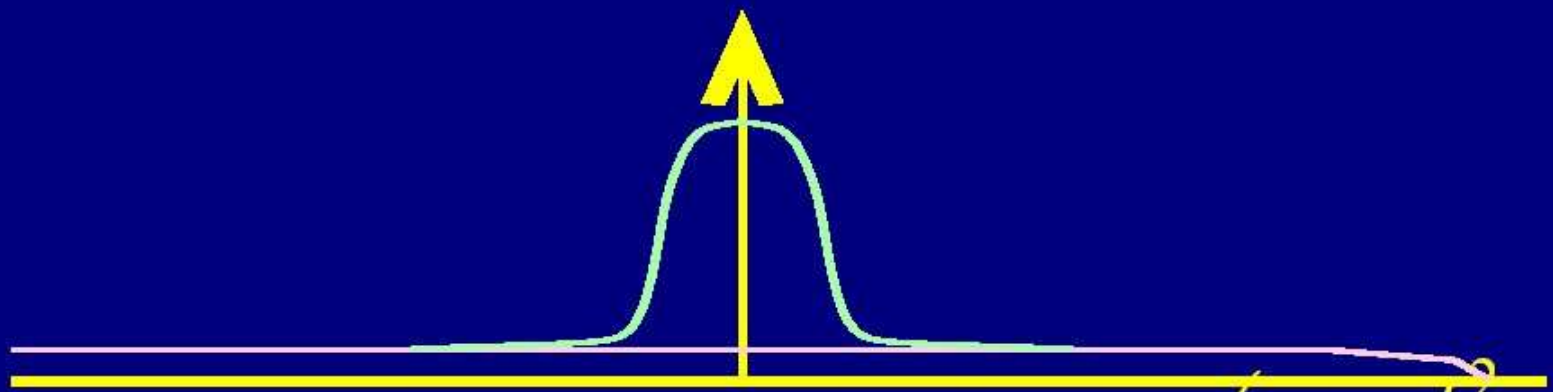
PPV useful for Phase Noise/Jitter MMing



- Timing jitter variance (per cycle) = cT



- *Lorenzian spectrum:* $\mathcal{L}(f_m) = 10 \log_{10} \left(\frac{f_0^2 c}{\pi^2 f_0^4 c^2 + f_m^2} \right)$

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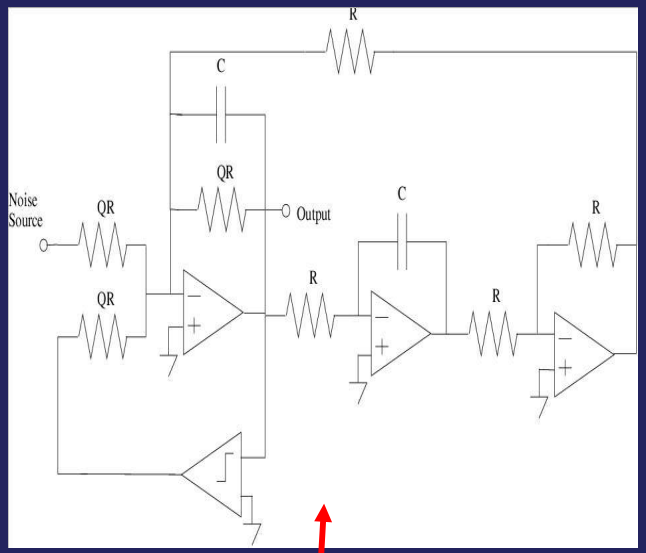
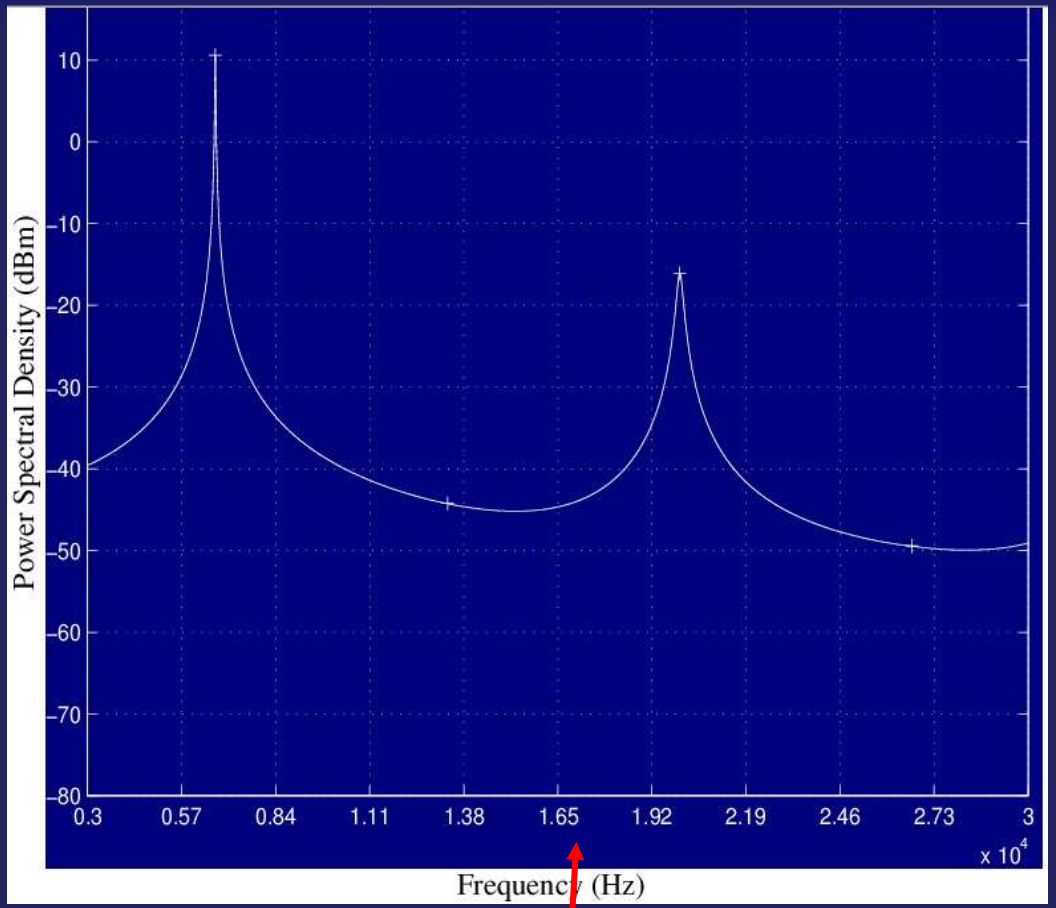
Oscillator Phase Noise Spectrum



Tow-Thomas oscillator

[Toth TCAS-1 1992]



Phase noise spectrum

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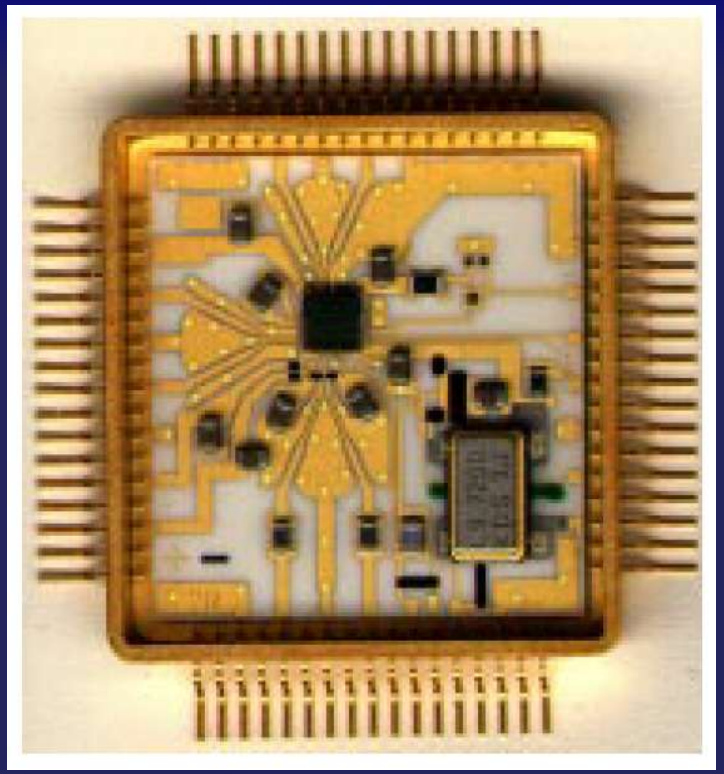
PLLs: Commodity, High-Margin

Rick Walker, HP/Agilent



Rick Walker, HP/Agilent

1.25Gbps Ethernet xcvr
<< $10

2.44Gbps SONET CDR
$500

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PLL Applications

- Clock and data recovery (CDR)
  - synchronization: Costas Loop
  - applications: communication systems, disk-drive read-channels
- Frequency synthesizers
  - integer-N, fractional-N synthesizers
  - direct digital to GPSK modulation

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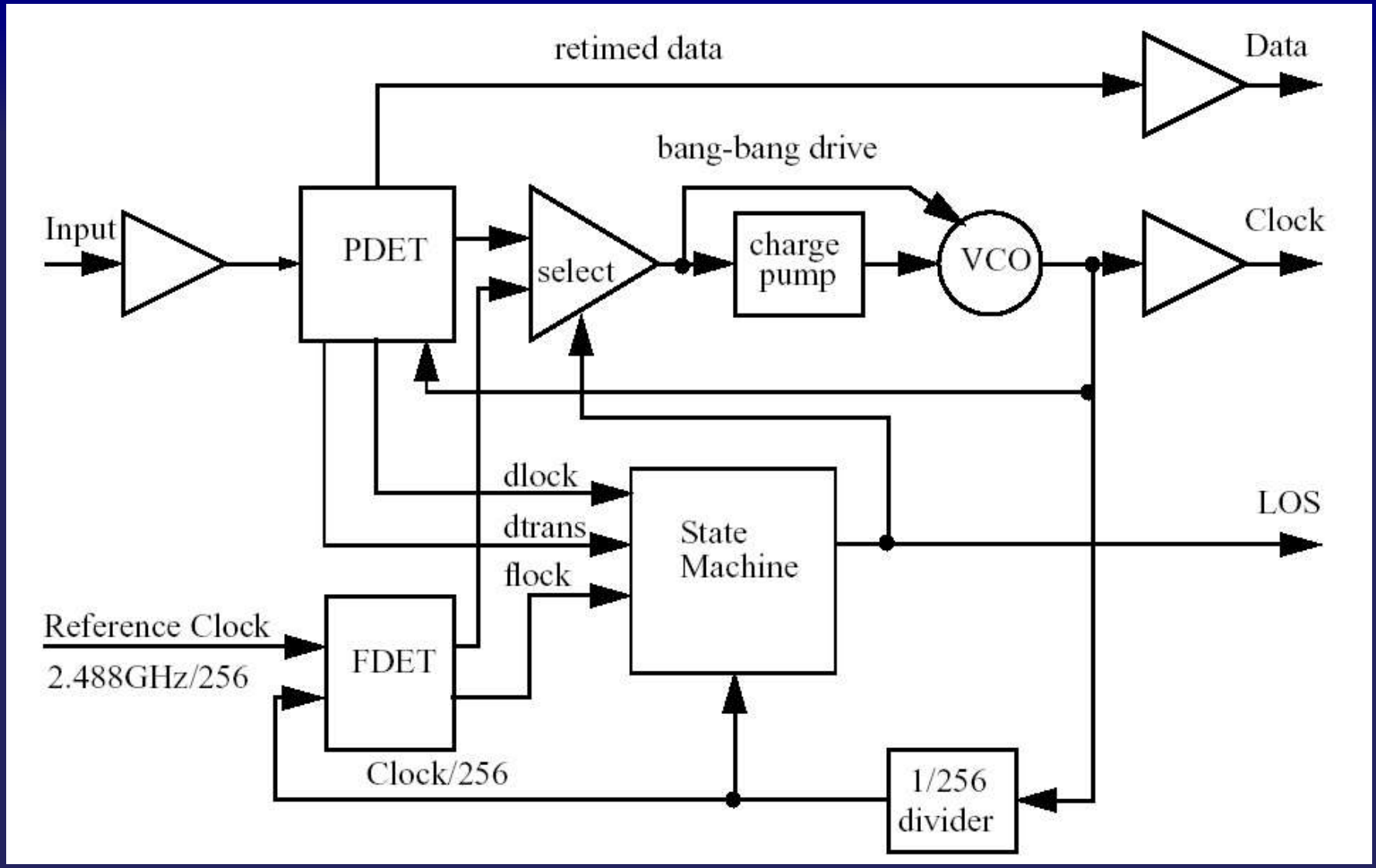
Clock and Data Recovery (CDR) ckt



Mixed-signal PLL: very hard to simulate at ckt level

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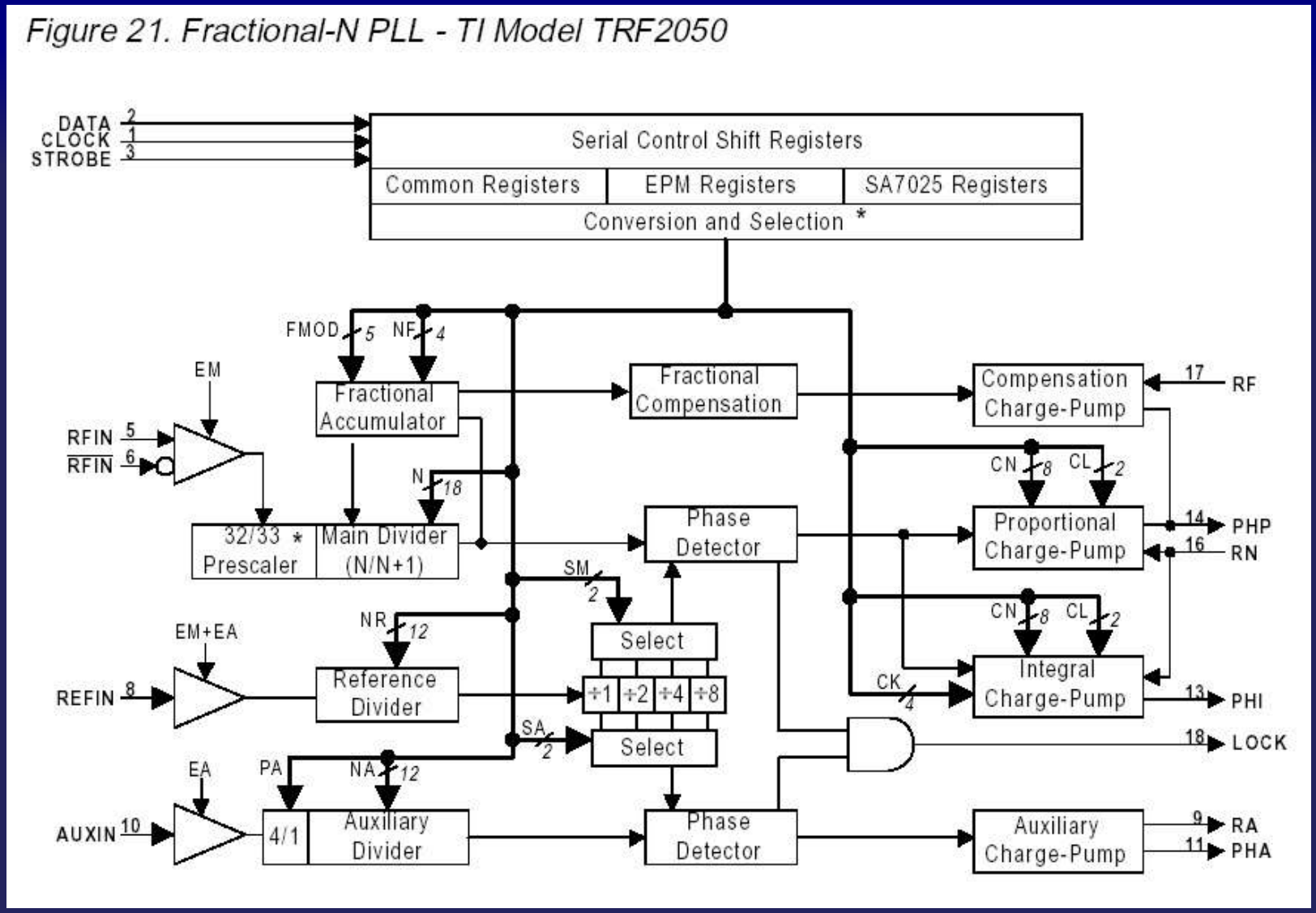
TI TRF-2050 Fractional-N PLL



Texas Instruments

Large; complex; many interconnected functional blocks

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PLL Simulation: Difficulties

- SPICE: Inaccurate + extremely time-consuming
  - biggest single culprit: VCO
    - 100K cycles of VCO typical for PLL simulation
  - combination of digital (PFD, dividers) and complicated analog (charge pump, VCO)
  - noise characterization (jitter) critical and difficult
  - capture/lock-in/freq-hopping dynamic phenomena
  - Injection-locking: 1st order PLL
- Full system with PLLs: very difficult today
  - Current macromodel-based approaches ad-hoc, manual, cannot capture dynamics, nonlinearity well

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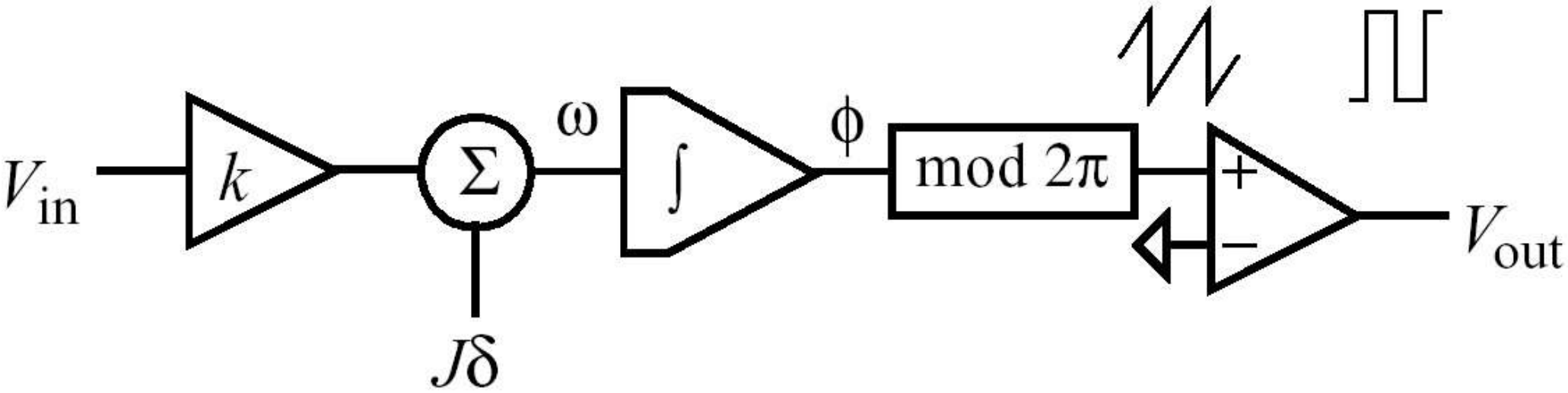
Linear Macromodelling of VCOs/PLLs



Ken Kundert, Cadence

[Kundert 02]

- Manually generated VCO macromodel
- Output VCO phase = integral of input control
- Linear => cannot capture nonlinear phenomena (injection locking)
- Good for intuition, hand calculations, noise trends
- Can be grossly wrong for jitter caused by power grid/substrate

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System Simulation with VCO Macromodels: PLLs

- Use nonlinear phase macromodel of VCO in phase macromodel for PLL [Lai/Roychowdhury 04]
  - PPV "extracted" by algorithm
  - amplitude components could also be used
- Replace other components (PFD, LPF, divider) also with macromodels if necessay
  - often, PFD and LPF small: keep full SPICE ckt
  - divider macromodel => simple scaling of phase
- Single VCO macromodel to capture desired and undesired influences

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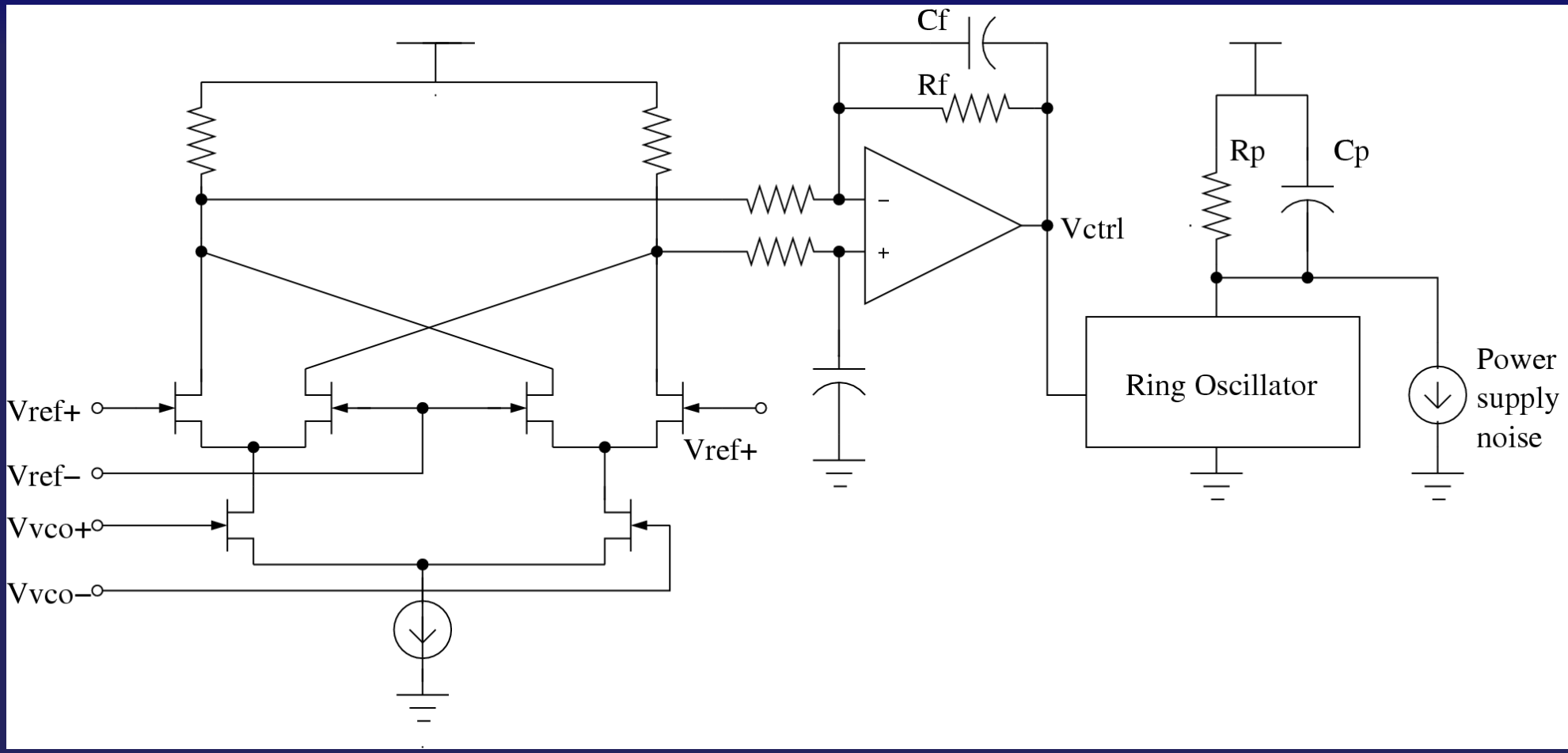
Simple Ring-Oscillator-based Phase-Locked Loop



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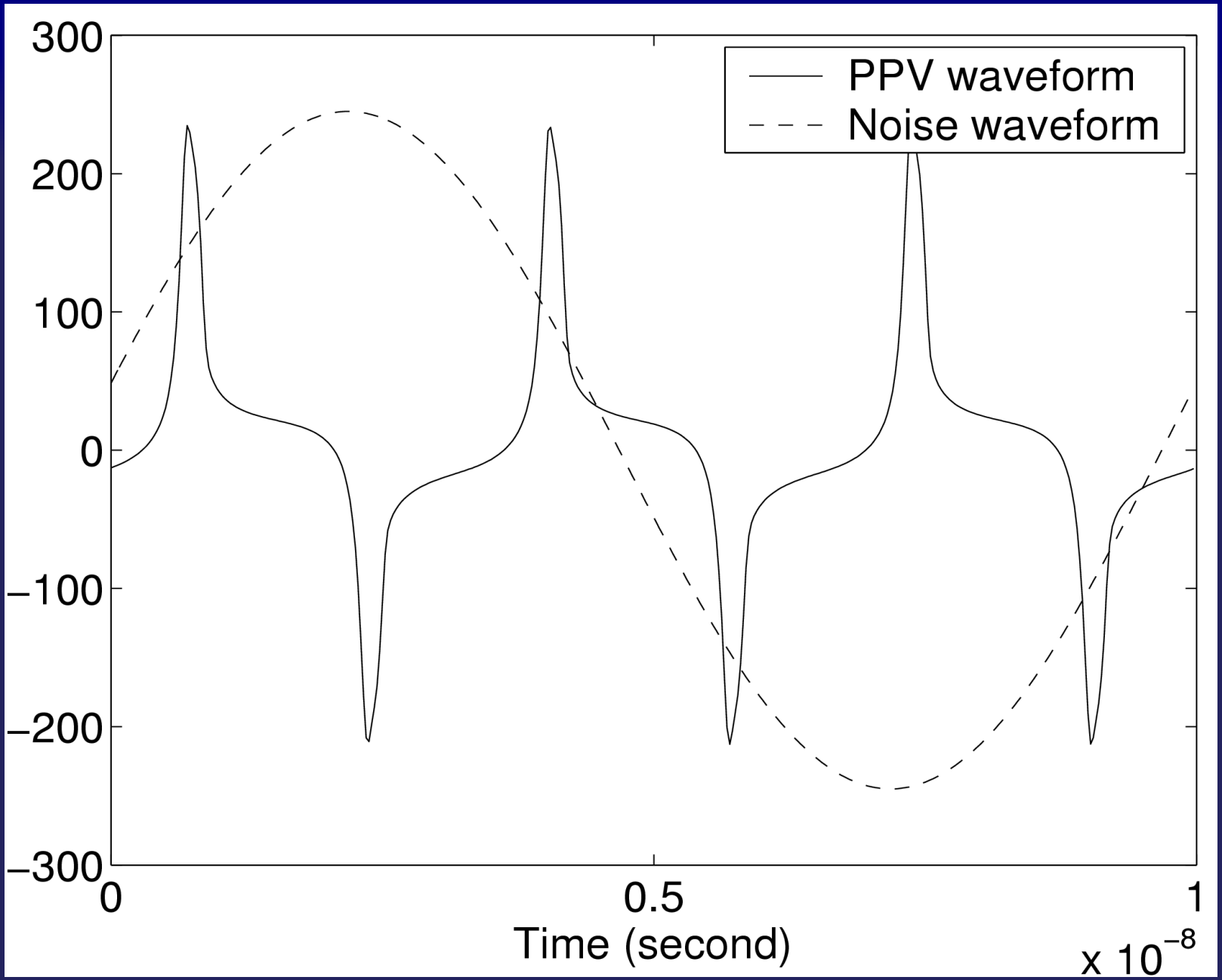
Expected Impact of 1st harmonic Supply Noise



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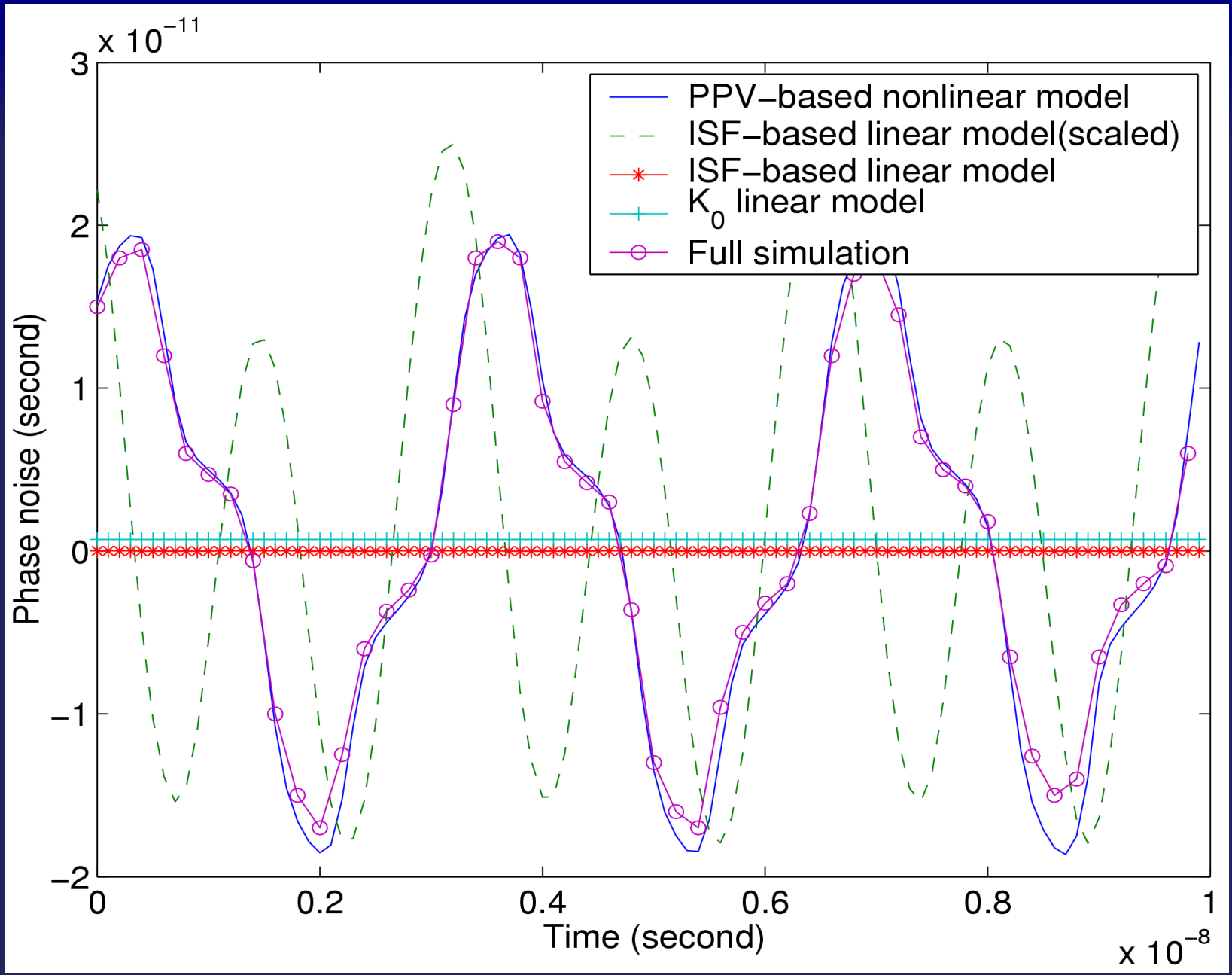
PLL Phase Reponse to Periodic Supply Noise



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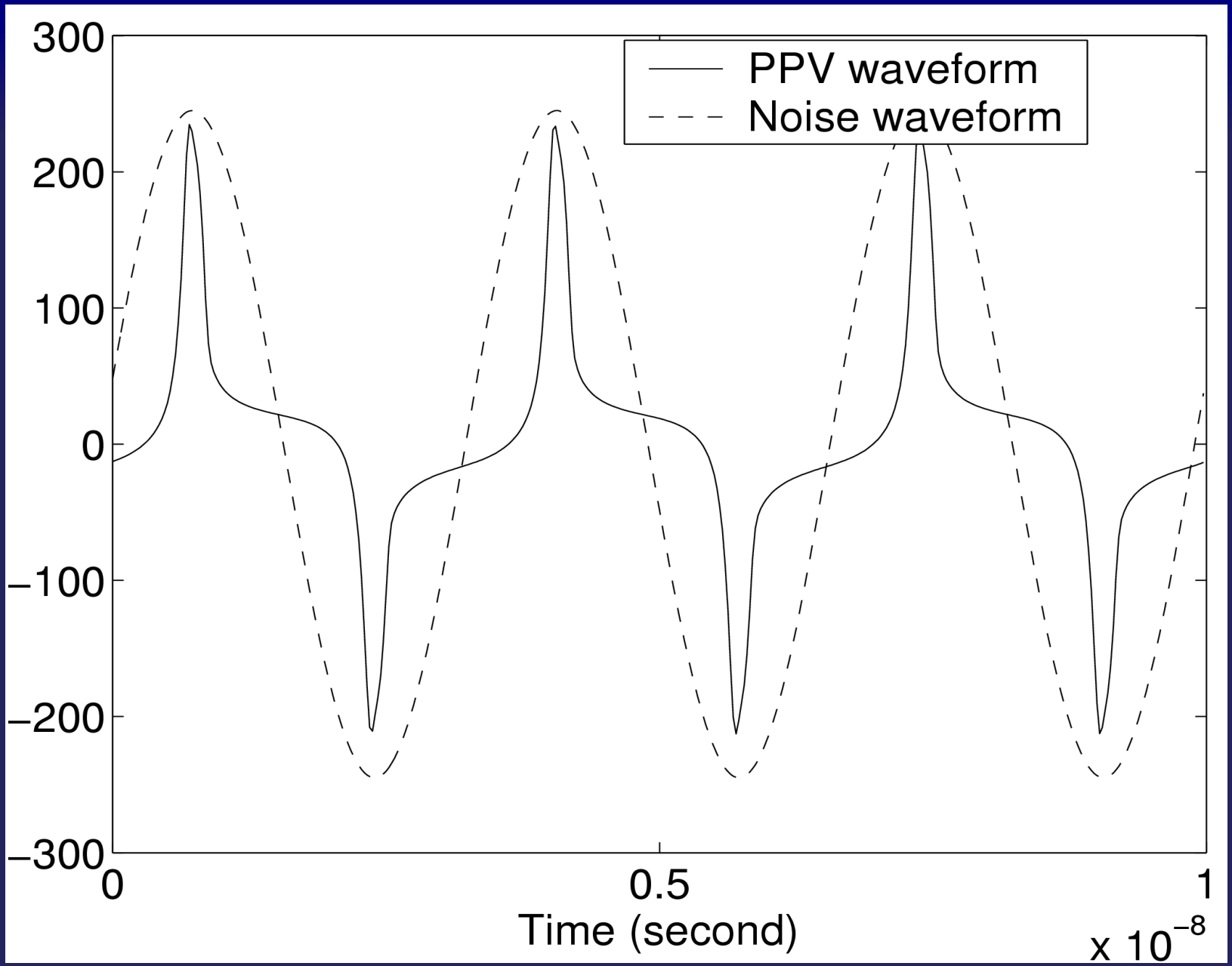
Expected Impact of 3rd Harmonic Supply Noise



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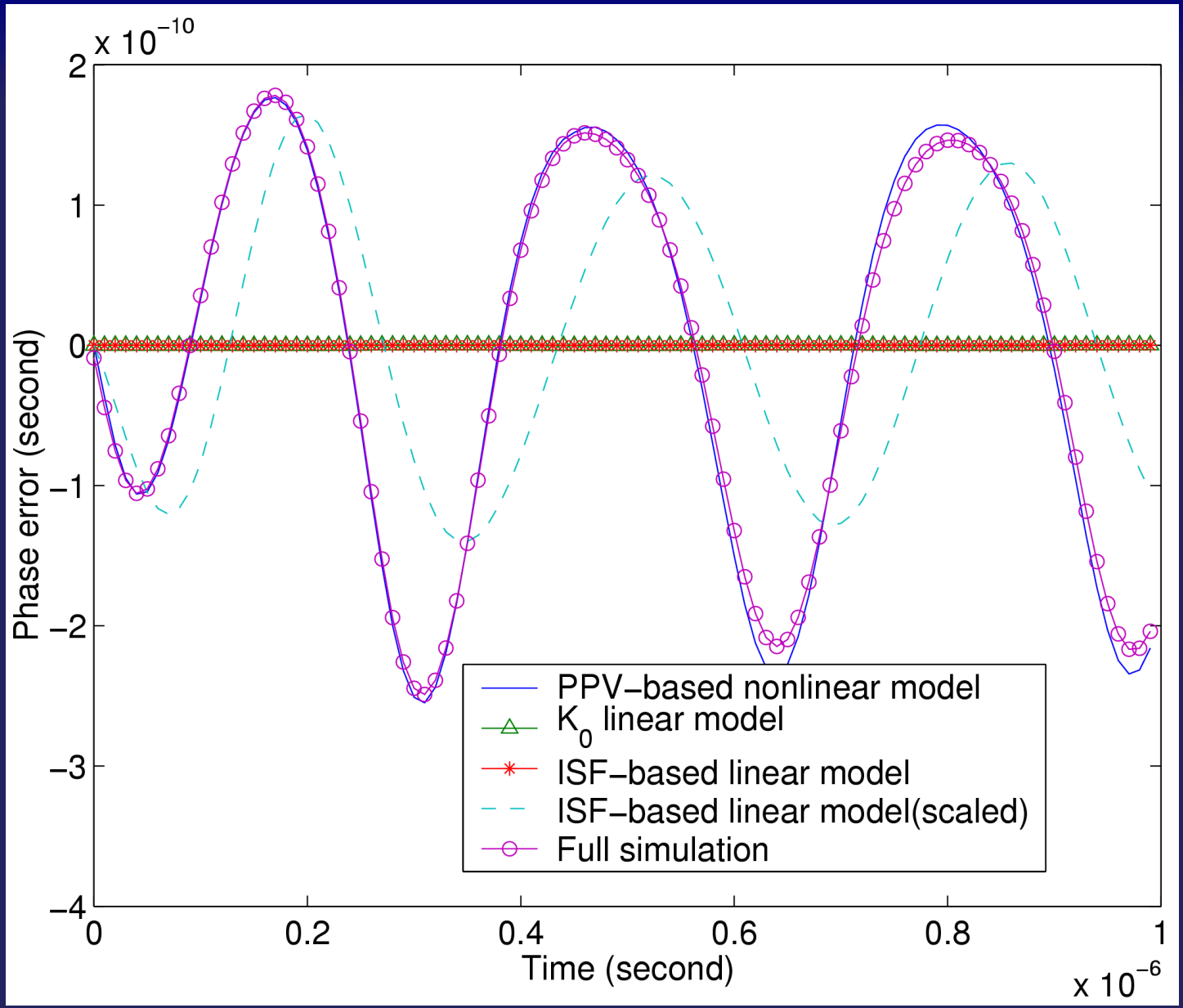
3rd Harmonic Supply Noise: Phase Macromodel vs Full PLL simulation



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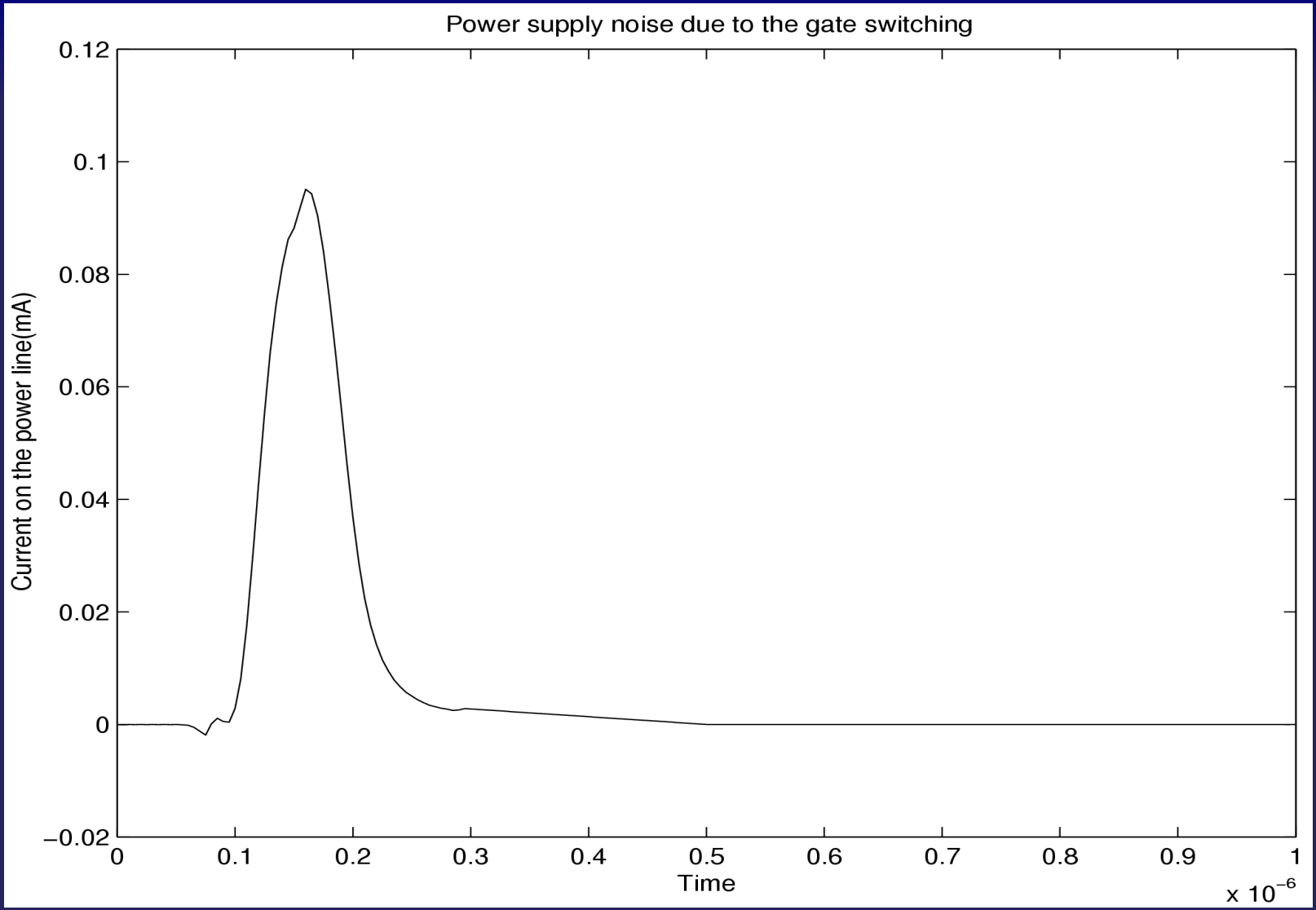
Power Supply Spike due to Single Switching



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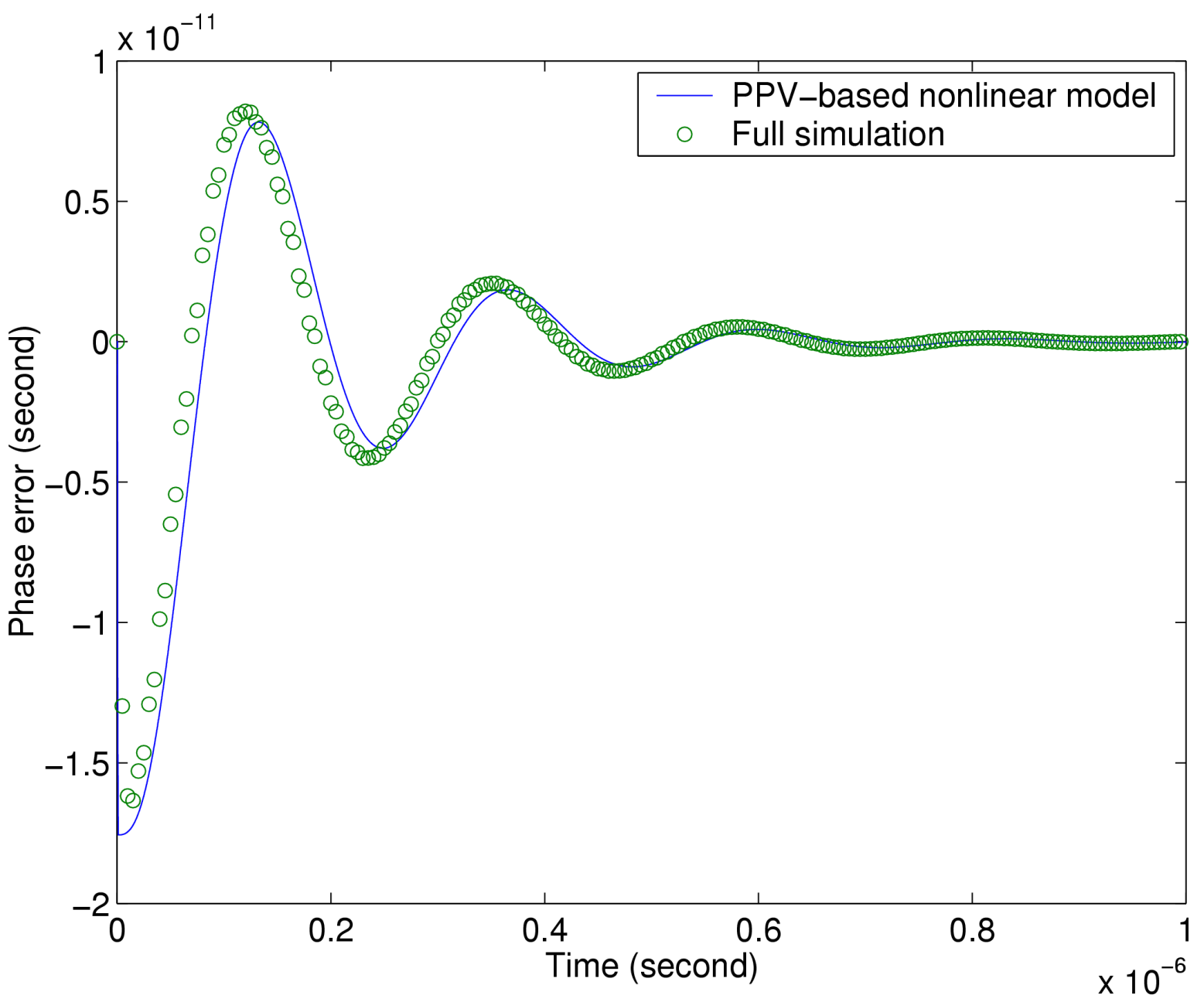
Phase Response of PLL to Supply Noise Spike



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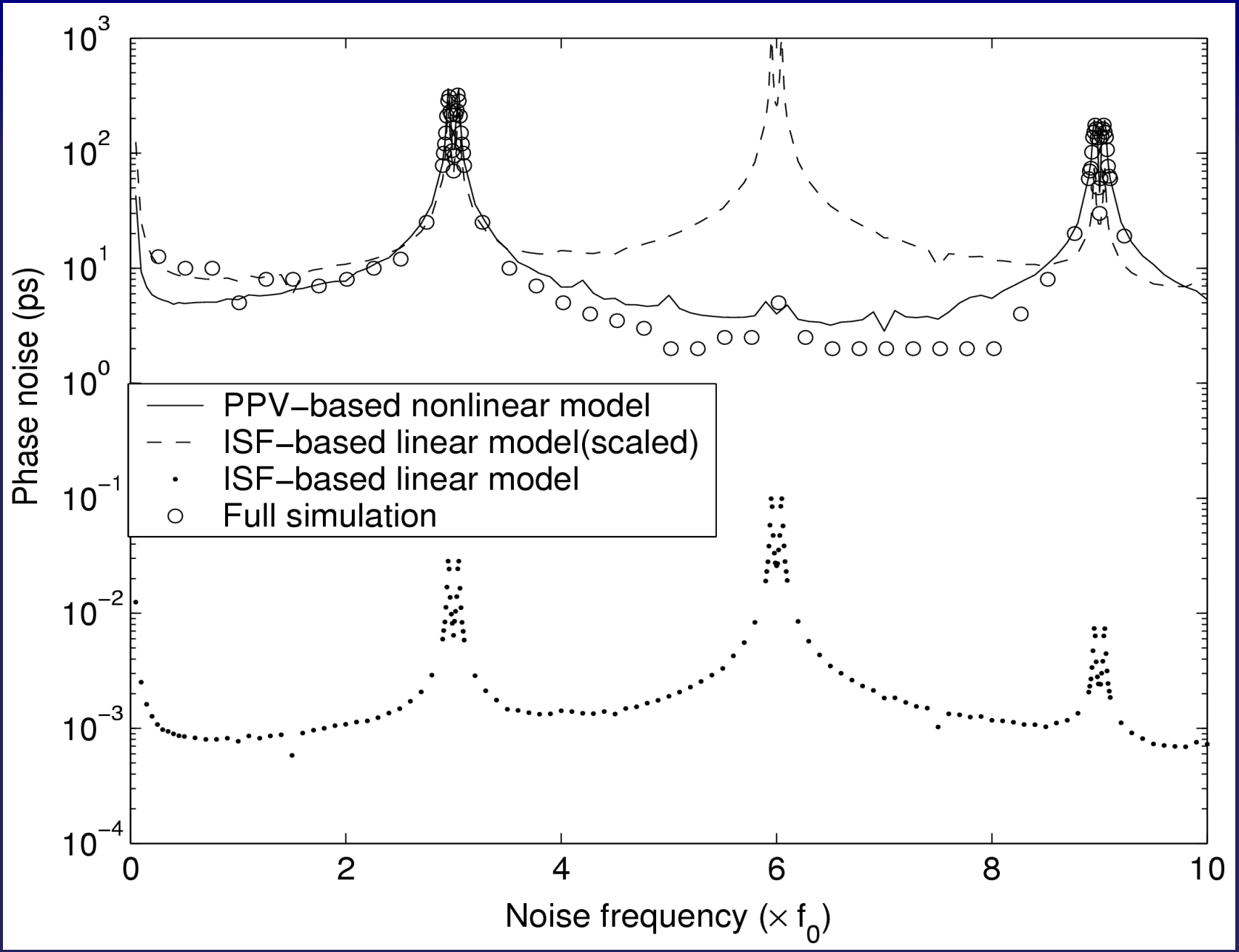
Sinusoidal Supply Noise: Effect on PLL Phase



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Conclusion

- Coming "soon": automated nonlinear macromodelling for...
  - op-amps, mixers, switching filters, comparators
  - oscillators, VCOs (any kind: LC/ring/relaxation/etc)
  - large digital aggressor blocks: interference macromodels
  - bottom-up "extracted" macromodels: much more accurate, second-order effects, ...
- Use of core macromodels for system simulation
  - ADCs/DACs/Sigma-Deltas
  - PLLs/Sigma-Deltas (incl jitter and noise)
  - SOCs
  - MATLAB/Simulink/Verilog-A/VHDL-AMS/etc
- Automated Macromodelling: the ONLY sustainable methodology for effective CAD support of nano-era analog, mixed-signal and RF design

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