Question 1 - Instruction Set 1 – x295 - SOLUTION

C. Evaluating our x295 instruction set using Memory Traffic criteria

Table 2

x295 program **(1 assembly instruction/ machine code instruction per row)**	**Fetch** **(number of word size memory accesses)** **+** **Provide an explanation explaining the count**	**Decode/Execute** **(number of word size memory accesses)** **+** **Provide an explanation explaining the count**

Assembly instruction:
`ADD x, y, tmp1`
 	
Machine code instruction:
`0001 <Dest 12 bits>`
`0000 <Src1 12 bits>`
`0000 <Src2 12 bits>`
	Count: 3
	
	Explanation: since the binary encoding of the ADD instruction is 3-word wide
		Count: 3
		
		Explanation: since the ADD instruction reads the value of two operands (16 bits each –> 1 word each) from memory and it writes its result (16 bits -> 1 word) to memory

Assembly instruction:
`SUB x, y, tmp2`
 	
Machine code instruction:
`0010 <Dest 12 bits>`
`0000 <Src1 12 bits>`
`0000 <Src2 12 bits>`
	Count: 3
	
	Explanation: since the binary encoding of the SUB instruction is 3-word wide
		Count: 3
		
		Explanation: since the SUB instruction reads the value of two operands (16 bits each –> 1 word each) from memory and it writes its result (16 bits -> 1 word) to memory

Assembly instruction:
`MUL tmp1, tmp2, z`
 	
Machine code instruction:
`0011 <Dest 12 bits>`
`0000 <Src1 12 bits>`
`0000 <Src2 12 bits>`
	Count: 3
	
	Explanation: since the binary encoding of the MUL instruction is 3-word wide
		Count: 3
		
		Explanation: since the MUL instruction reads the value of two operands (16 bits each –> 1 word each) from memory and it writes its result (16 bits -> 1 word) to memory

Grand Total: 18	**Total: 9**	**Total: 9**

Once completed, submit it on Crowdmark as your answer to Question 1.