Assignment 8 - SOLUTION

Assignment 8 - Objectives:

- Performance analysis of ...
  - Sequential Instruction Execution microprocessor
  - Staged Instruction Execution microprocessor
  - Pipelined Instruction Execution microprocessor (uniform and non-uniform length stages)

For each of our team-based assignments, you can either:

- Create a group with the same partner,
- Change your group (select a different partner), or
- Decide to work on you own.

Group of two (2):

- You can do Assignment 8 in a group of two (2) or you can work on your own.
- If you choose to work in a group of two (2):
  - Crowdmark will allow you to select your teammate (1). Both of you will only need to submit one assignment and when the TAs mark this one assignment, the marks will be distributed to both of you automatically.
  - You can always work with a student from the other section, but both of you will need to submit your assignment separately, i.e., Crowdmark will not consider the both of you as a group.

Requirements for this Assignment 8:

- Always show your work (as illustrated in lectures), if appropriate, and
- Make sure the pdf/jpeg/png documents you upload are of good quality, i.e., easy to read, therefore easy to mark! :) If the TA cannot read your work, the TA cannot mark your work and you will get 0. :(

Marking:

- All questions of this assignment will be marked for correctness.
- The amount of marks for each question is indicated as part of the question.
- A solution will be posted on Monday after the due date.

Deadline:

- Friday March 31 at 23:59:59 on Crowdmark.
- Late assignments will receive a grade of 0, but they will be marked (if they are submitted before the solutions are posted on Monday) in order to provide feedback to the student.

Enjoy!

Q1 (4 points)

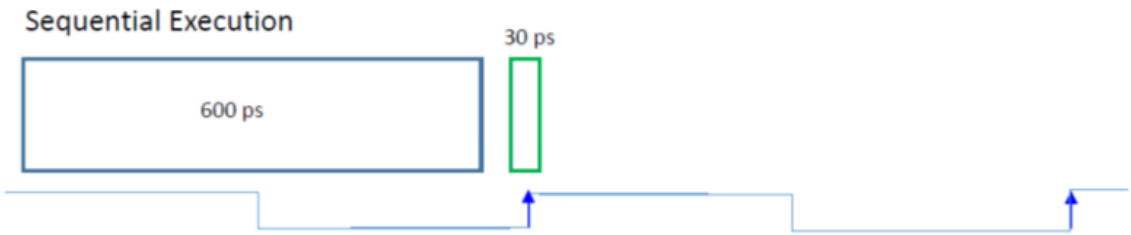
Sequential Instruction Execution and Staged Instruction Execution microprocessor

Part 1

Imagine we design a microprocessor, more specifically, we design its datapath, in such a way that the propagation delay of its entire combinational logic circuit is 600 ps and the propagation delay of the memory element we use is 30 ps. Note: The *memory element* is such that it remembers all the bits expressing the result of the combinational logic circuit.

- What is the minimum clock cycle time (in picoseconds), the latency (in picoseconds), the throughput (in GIPS) and the CPI of our microprocessor if it executes instructions sequentially, i.e., one instruction executed at a time?

Solution:



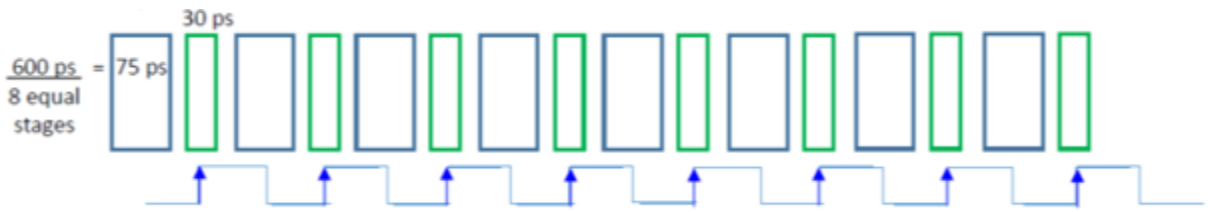
- minimum clock cycle time: 600 ps + 30 ps = 630 ps
- latency: 600 ps + 30 ps = 630 ps, 1 intruction takes 630 ps to execute (1 instruction per clock cycle)
- throughput: # of instructions executed per second
  = 1 instruction per 630 ps = 1/630 ps = 1.5873×10^{-3} instruction per picosecond
  = 1.5873×10^{9} instruction per second
  = 1.5873 GIPS
- CPI: 1

Part 2

Let's now divide the combinational logic circuit of our Sequential Instruction Execution microprocessor (designed in Part 1 above) into eight (8) equal stages. This new design produces a Staged Instruction Execution microprocessor. Note that this new microprocessor is still executing one instruction at a time. Also, whenever we needed a memory element in our new design, we used the same kind of memory elements we used in our sequential design, all with the same latency. Finally, in this question, we are not concerned about naming these eight stages.

- What is the minimum clock cycle time (in picoseconds), the latency (in picoseconds), the throughput (in GIPS) and the CPI of our newly designed Staged Instruction Execution microprocessor?

Solution:



- minimum clock cycle time: 600/8 ps + 30 ps = 75 ps + 30 ps = 105 ps
- latency: (600/8 ps + 30 ps) 8 = (105 ps) 8 = 840 ps, 1 intruction takes 840 ps to execute (1 instruction per 8 clock cycles)
- throughput: # of instructions executed per second
  = 1 instruction per 840 ps = 1/840 ps = 1.19 x 10^{-3} instruction per picosecond
  = 1.19 x 10^{9} instruction per second
  = 1.19 GIPS
- CPI: 8

Q2 (8 points)

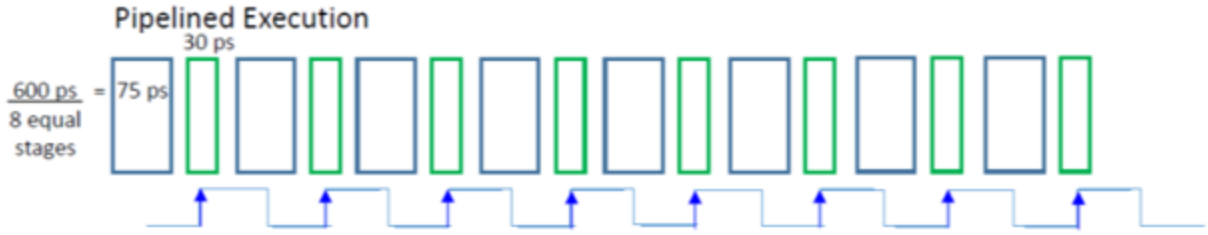
Pipelined Instruction Execution microprocessor (uniform and non-uniform length stages)

Part 1

Consider the Staged Instruction Execution microprocessor we designed in Part 2 of Question 1 above. Imagine now that this new microprocessor executes one instruction at every tick of the system clock. In other words, we have now designed a Pipelined Instruction Execution microprocessor with uniform length stages.

- What is the minimum clock cycle time (in picoseconds), the latency (in picoseconds), the throughput (in GIPS) and the CPI of this new Pipelined Instruction Execution microprocessor?

Solution:



- minimum clock cycle time: 600/8 ps + 30 ps = 75 ps + 30 ps = 105 ps
- latency: (600/8 ps + 30 ps) 8 = (105 ps) 8 = 840 ps, 1 intruction takes 840 ps to execute, i.e., to go through all 8 stages of its execution
- throughput: a fully pipelined processor (at steady state, i.e., when all stages are busy executing micro operations of the machine level instructions) can execute 1 instruction per clock cycle
  = 1 instruction per 105 ps = 1/105 ps = 9.5238×10^{-3} instruction per picosecond
  = 9.5238×10^{9} instruction per second
  = 9.5238 GIPS
- CPI: 1

Part 2

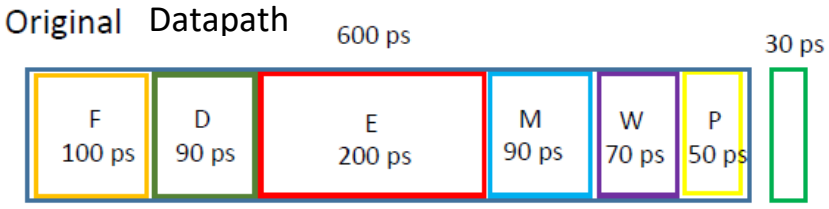
Requirement: First, read Section 4.4.3 (subsection on "Nonuniform Partitioning") of our textbook (Bryant and O'Hallaron) and do its Practice Problem 4.28.

Imagine we design a microprocessor, more specifically, we design its datapath, in such a way that the propagation delay of its entire combinational logic circuit is 600 ps and the propagation delay of the memory element we use is 30 ps.

This time, the datapath of this microprocessor has been divided into six (6) stages:

- stage F with a propagation delay of 100 ps,
- stage D with a propagation delay of 90 ps,
- stage E with a propagation delay of 200 ps,
- stage M with a propagation delay of 90 ps,
- stage W with a propagation delay of 70 ps, and
- stage P with a propagation delay of 50 ps.

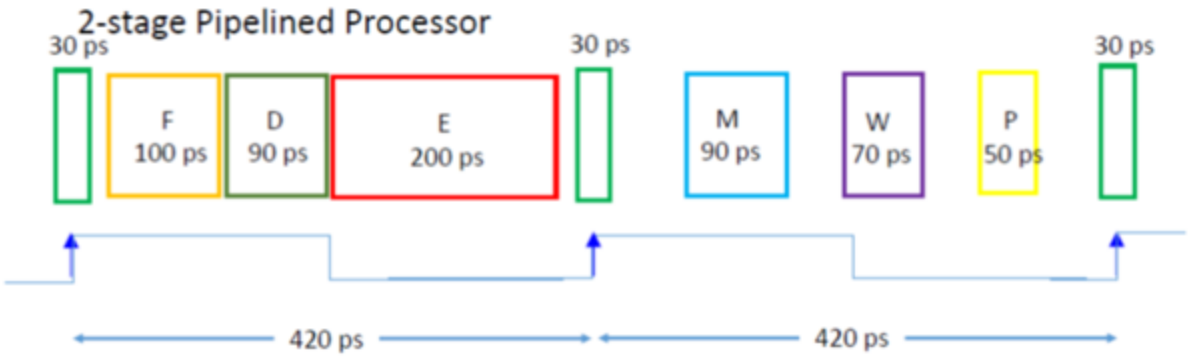
And so far, no pipeline registers have yet been placed between any of these 6 stages. Let's call the datapath of this microprocessor, as it is described above, its ***original datapath***.



Note: These six stages cannot be shuffled, i.e., their order is fixed: F – D – E – M – W – P

1. If we were to place a pipeline register between a pair of adjacent stages of this original datapath in order to form a 2-stage pipelined microprocessor, where would we place this pipeline register such that the clock cycle time is minimized? Compute the minimum clock cycle time and the maximum CPU throughput of this 2-stage pipelined microprocessor.

Solution:



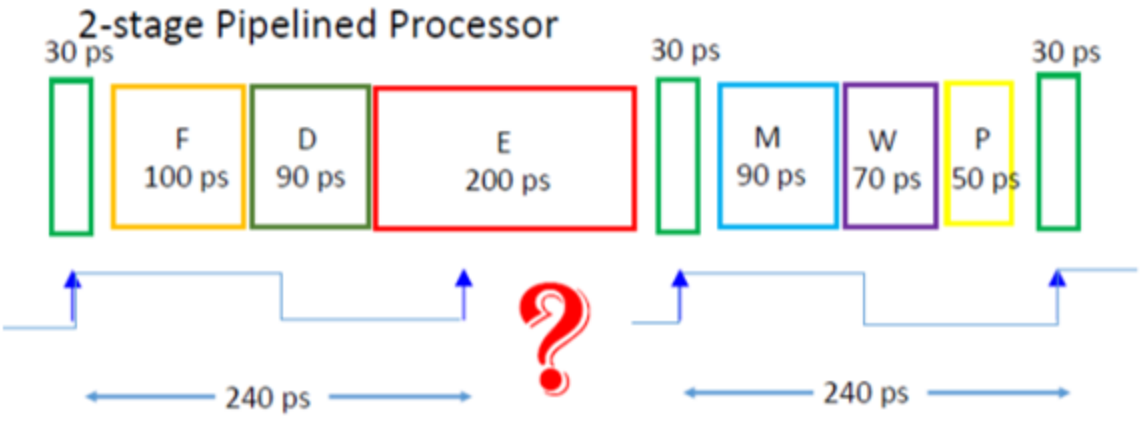
Note: These six stages cannot be shuffled, i.e., their order is fixed: F – D – E – M – W – P

- **Minimum clock cycle time**: (100+90+200) ps + 30 ps = 390 ps + 30 ps = 420 ps
- Why not (90+70+50) ps + 30 ps = 240 ps?

  Because 240 ps would be too fast (the clock would be ticking too fast). As you can see from the diagram below, the signals would not have time to get through the combinational logic cuircuit of F, D and E, in time for their output to be ready at the "door" of the clocked (or pipelined) register to their right. When this clocked register would get "clocked", i.e., activated by the rising edge of the clock cycle, it would not have received the proper input by then, hence it would not "remember" the proper result from F, D and E.

  Therefore, the ***minimum clock cycle time*** must be the largest of the two possible clock cycle times.

Clock cycle TOO FAST

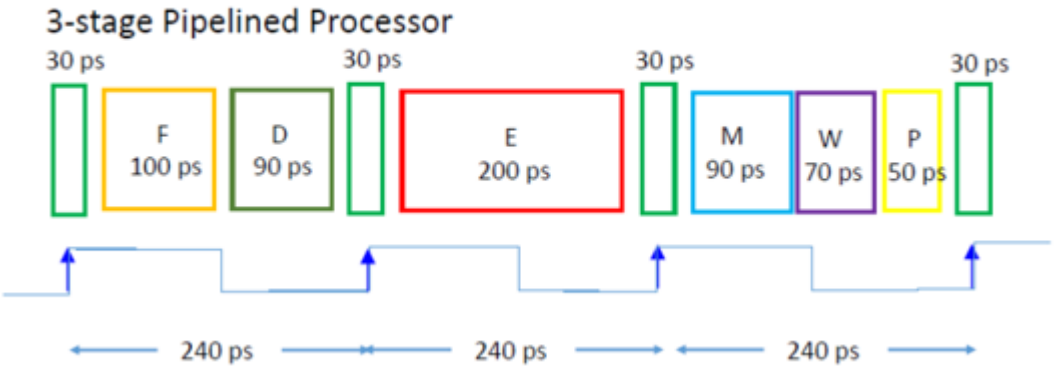


- Note that other ways of parting the F, D, E, M, W, P stages of the ***original datapath*** would create a slower clock cycle than 420 ps -> not good!
- Here are all the other ways of parting the F, D, E, M, W, P stages of the ***original datapath***:
  - F+D (190 ps) and E+M+W+P (410 ps), clock cycle that would work for both stages: 410 ps + 30 ps = 440 ps
  - F (100 ps) and E+M+W+P (500 ps), clock cycle that would work for both stages: 500 ps + 30 ps = 530 ps
  - F+D+E+M (480 ps) and W+P (120 ps)), clock cycle that would work for both stages: 480 ps + 30 ps = 510 ps
  - F+D+E+M+W (550 ps) and P (50 ps), clock cycle that would work for both stages: 550 ps + 30 ps = 580 ps
- Remember, we are computing the ***minimum clock cycle time***, so 420 ps is the minimum of all the possible clock cycle times we can get by parting the ***original datapath*** in various ways.
- **maximum CPU throughput**: 1/420 ps = 2.38 GIPS

  A fully pipelined microprocessor (at steady state, i.e., when the 2 "stages" are busy executing micro operations of the machine level instruction) can execute 1 instruction per clock cycle.

2. If we were to place two pipeline registers between the stages of the original datapath in order to form a 3-stage pipelined microprocessor, where would we place these two pipeline registers such that the clock cycle time is minimized? Compute the minimum clock cycle time and the maximum CPU throughput of this 3-stage pipelined microprocessor.

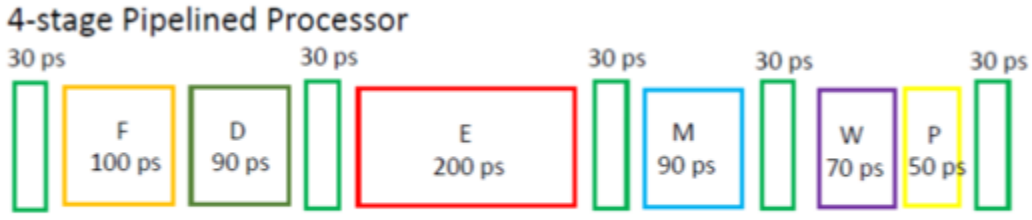
Solution:



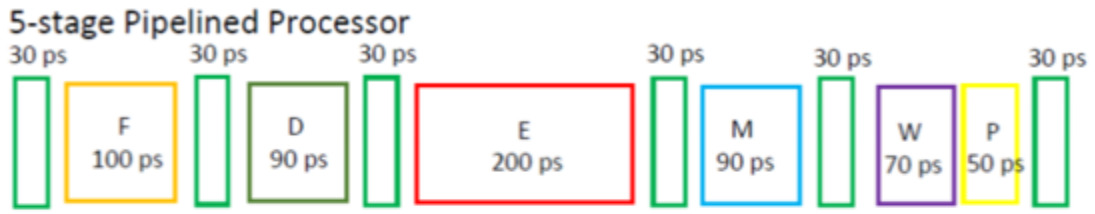
- **minimum clock cycle time**: (90 + 70 + 50) ps + 30 ps = 210 ps + 30 ps = 240 ps
  - The other possible clock cycles are too fast:
    - (100 + 90) ps + 30 ps = 220 ps
    - 200 ps + 30 ps = 230 ps
- **maximum CPU throughput**: 1/240 ps = 4.167 GIPS

3. If we were to place more and more pipeline registers between the stages of the original datapath in order to form greater staged-pipelined microprocessors, which stage would become a *limiting factor* on the minimum clock cycle time?
   Hint: Form a 4-stage pipelined microprocessor then a 5-stage pipelined processor and observe what happens. This may help you answer this question.

Solution:



Minimum clock cycle is 200 ps + 30 ps = 230 ps

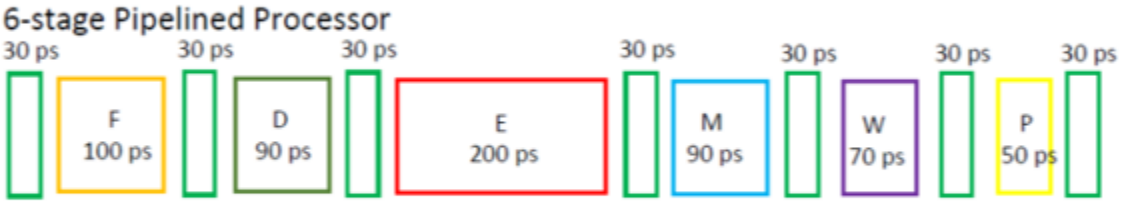


Minimum clock cycle is 200 ps + 30 ps = 230 ps

Solution: The stage E, the longest stage (in ps), is the limiting factor on the minimum clock cycle time since we compute the minimum clock cycle based on the longest stage of the pipelined register.

4. If we were to fully pipeline our original datapath (hence creating a 6-stage pipelined microprocessor), what would its minimum clock cycle time and its maximum CPU throughput be?

Solution:



- **minimum clock cycle time**: 200 ps + 30 ps = 230 ps
- **maximum CPU throughput**: 1/230 ps = 4.35 GIPS

Q3 (5 points)

Benchmark data sets and graph from our Lab 6 data

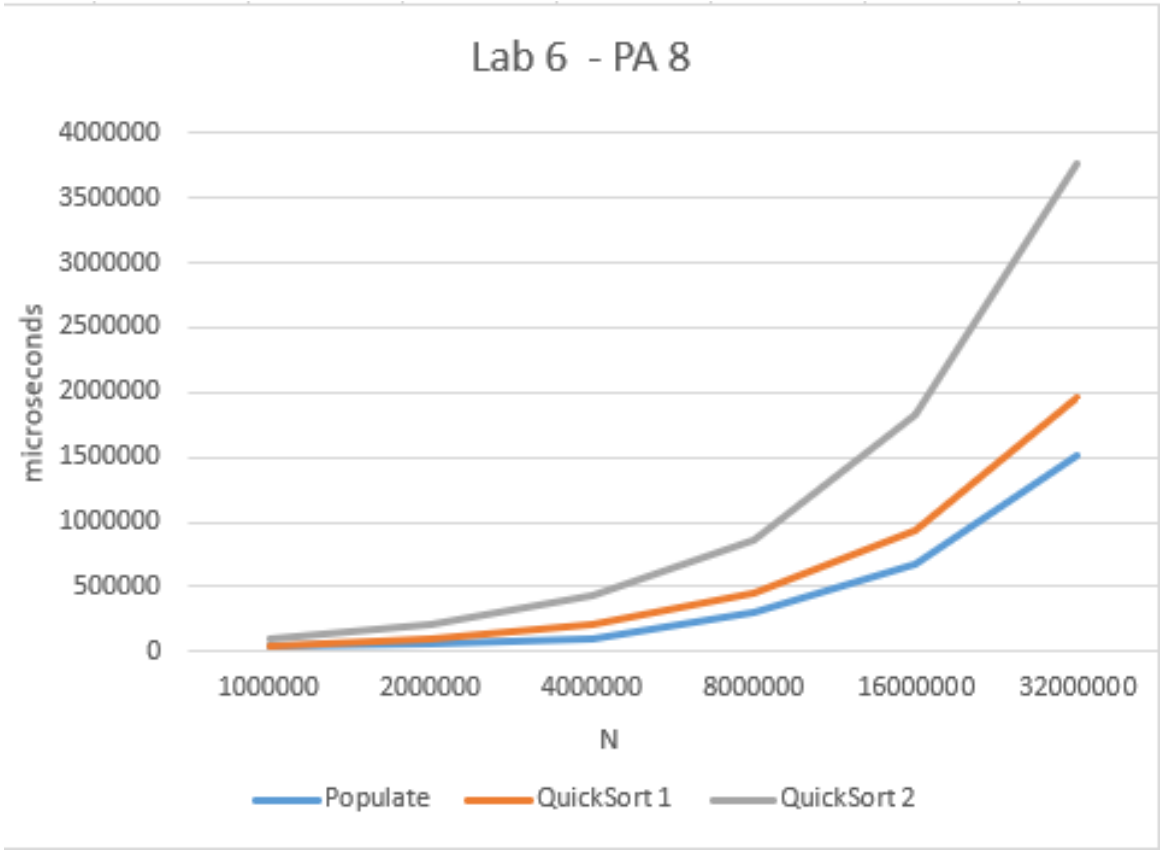
In Lab 6, you are asked to benchmark code and to graph your results.

In this question, upload the completed data sheet you built in Lab 6 as well as the graph you produced.

Make sure you graph all data sets onto the same graph and label each resulting line. This will ease comparison and allow you to promptly reach a conclusion.

Solution will vary depending on CSIL workstation used!

	A	B	C	D	E	F	G	H
1	Populate	1	2	3	4	5	6	μ
2	1000000	49488	47056	52450	23519	45802	51889	45034
3	2000000	76150	73229	78552	72232	54587	49314	67344
4	4000000	97857	96407	105976	99667	101900	97001	99801.33
5	8000000	312642	287318	290975	298144	304895	302680	299442.3
6	16000000	721089	759574	704826	619927	629285	626195	676816
7	32000000	1508477	1500443	1489173	1475720	1497560	1576051	1507904
8								
9	QSort1-H							
10	1000000	48010	47747	47535	50135	49518	47617	48427
11	2000000	101461	99814	98714	103188	101554	88451	98863.67
12	4000000	211590	208700	213392	215123	214492	220104	213900.2
13	8000000	425325	442047	453114	446919	455118	441223	443957.7
14	16000000	938661	938582	925453	959332	942000	934413	939740.2
15	32000000	1960368	1950993	1976591	1929515	1948972	1974663	1956850
16								
17	QSort2-L							
18	1000000	99759	106436	100647	107165	109513	102493	104335.5
19	2000000	208375	206205	205010	207303	205043	207094	206505
20	4000000	428195	430699	430608	427085	426414	424177	427863
21	8000000	880071	846917	850850	846867	872396	884813	863652.3
22	16000000	1805681	1832526	1795174	1852113	1838215	1809030	1822123
23	32000000	3759916	3780824	3788539	3788055	3671143	3779888	3761394
24								
25		Populate	QuickSort 1	QuickSort 2				
26	1000000	45034	48427	104335.5				
27	2000000	67344	98863.667	206505				
28	4000000	99801.3	213900.17	427863				
29	8000000	299442	443957.67	863652.33				
30	16000000	676816	939740.17	1822123.2				
31	32000000	1507904	1956850.3	3761394.2				


Lab 6 - PA 8
4000000
3500000
3000000
2500000
2000000
1500000
1000000
500000
0
microseconds
1000000
2000000
4000000
8000000
16000000
32000000
N
Populate
QuickSort 1
QuickSort 2