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CMPT 300 Assignment 4 Part 1

1. Address Translation Process

Virtual memory space: $2^{(32)}$ bytes

Physical memory: $2^{(18)}$ bytes

Page size: 4096 bytes

Virtual Address: 11123456 (Hexadecimal Base 16)

a) **Explain how the system establishes the corresponding physical location:**

Virtual Address to Binary:

If the virtual address is 11123456 (Hexadecimal Base 16), 11123456 in binary would be 0001 0001 0001 0010 0011 0100 0101 0110.

Get Page Number and Offset

The virtual address (in binary) is 0001 0001 0001 0010 0011 0100 0101 0110. The last 12 bits (0100 0101 0110) ends up being the offset while the virtual Page Number will be the last 20 bits (0001 0001 0001 0010 0011)

Steps with getting the physical location using TLB (Translation look-aside Buffer hardware)

The offset and page number given from the virtual address are separated in the logical address with the page number being set to the TLB. If the page number is not in the TLB, the frame number will end up being looked for in the page table in main memory. If the page number is in the TLB, we access the TLB to get the frame number. Finally, the offset is added with the frame number to get the physical address.

All these processes are hardware processes except for when the frame number is looked up in the page table in main memory (software).

2. Calculating Maximum Acceptable Page-Fault Rate

Empty or unmodified page service time: 8 ms

Modified page service time: 20 ms

Memory access time: 100 ns

Modified page rate: 70%

Effective access time: ≤200 ns

Effective Access Time (EAT) = (1 - Page Fault Rate) * (Memory Access Time) + (Page Fault Rate) * (Page Fault Service Time)

Let **p** be the page-fault rate, that means that p fault service time would be 0.3 x 8 + 0.7 x 20 = 2.4 + 14 = 16.4 ms

EAT = (1-p) x 100 + p x 16400000

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200 = 100 + p x (16400000 – 100)

100 = p x 16399900

P = 100/16399900

P = 6.1 x 10 ^ - 6 or 0.00061 percent