Question 2 - Instruction Set 2 – x295+ - SOLUTION

B. Compiling and assembling a C program using our x295+ instruction set

Table 1

C program	x295+ assembly program	x295+ machine code program
`z = (x + y) * (x - y);`	`LOAD x, r0`	`1010 000 XXX XXXXXX` `0000 <Src 12 bits>`
	`LOAD y, r1`	`1010 001 XXX XXXXXX` `0000 <Src 12 bits>`
	`ADD r0, r1, r2`	`0001 010 000 001 XXX`
	`SUB r0, r1, r3`	`0010 011 000 001 XXX`
	`MUL r2, r3, r4`	`0011 100 010 011 XXX`
	`STORE r4, z`	`1011 XXX 100 XXXXXX` `0000 <Src 12 bits>`

C. Evaluating our x295+ instruction set using Memory Traffic criteria

Table 2

x295+ program **(1 assembly instruction/ machine code instruction per row)**	**Fetch** **(number of word size memory accesses)** **+** **Provide an explanation explaining the count**	**Decode/Execute** **(number of word size memory accesses)** **+** **Provide an explanation explaining the count**

Assembly instruction:
`LOAD x, r0`
Machine code:
`1010 000 XXX XXXXXX`
`0000 <Src 12 bits>`
	Count: 2
	
	Explanation: fetching 1 instruction that is 2-word wide
		Count: 1
		
		Explanation: executing a LOAD requires 1 memory access -> reading value x (16 bits -> 1 word) from memory

Assembly instruction:
`LOAD y, r1`
Machine code:
`1010 001 XXX XXXXXX`
`0000 <Src 12 bits>`
	Count: 2
	
	Explanation: fetching 1 instruction that is 2-word wide
		Count: 1
		
		Explanation: executing a LOAD requires 1 memory access -> reading value y (16 bits -> 1 word) from memory

Assembly instruction:
`ADD r0, r1, r2`
Machine code:
`0001 010 000 001 XXX`
	Count: 1
	
	Explanation: fetching 1 instruction that is 1-word wide
		Count: 0
		
		Explanation: executing an ADD does not require memory access since it is manipulating values held in registers

Assembly instruction:
`SUB r0, r1, r3`
Machine code:
`0010 011 000 001 XXX`
	Count: 1
	
	Explanation: fetching 1 instruction that is 1-word wide
		Count: 0
		
		Explanation: executing an SUB does not require memory access since it is

		manipulating values held in registers

Assembly instruction:
`MUL r2, r3, r4`
Machine code:
`0011 100 010 011 XXX`
	Count: 1
	
	Explanation: fetching 1 instruction that is 1-word wide
		Count: 0
		
		Explanation: executing an MUL does not require memory access since it is manipulating values held in registers

Assembly instruction:
`STORE r4, z`
Machine code:
`1011 XXX 100 XXXXXX`
`0000 <Src 12 bits>`
	Count: 2
	
	Explanation: fetching 1 instruction that is 2-word wide
		Count: 1
		
		Explanation: executing a STORE requires 1 memory access -> writing value z (16 bits -> 1 word) to memory

Grand Total: 12	**Total: 9**	**Total: 3**

Once completed, submit it on Crowdmark as your answer to Question 2.