Question 2 - Instruction Set 2 – x295+

B. Compiling and assembling a C program using our x295+ instruction set

Table 1

C program	x295+ assembly program	x295+ machine code program
z = (x + y) * (x – y);	LOAD x, r0	1010 000 XXX XXXXXX 0000 <Src 12 bits>
	LOAD y, r1	1010 001 XXX XXXXXX 0000 <Src 12 bits>
	ADD r0, r1, r2	0001 010 000 001 XXX
	SUB r0, r1, r3	0010 011 000 001 XXX
	MUL r2, r3, r4	0011 100 010 011 XXX
	STORE r4, z	1011 XXX 100 XXXXXX A. <Src 12 bits>

C. Evaluating our x295+ instruction set using Memory Traffic criteria

Table 2

x295+ program (1 assembly instruction/ machine code instruction per row)	Fetch (number of word size memory accesses) + Provide an explanation explaining the count	Decode/Execute (number of word size memory accesses) + Provide an explanation explaining the count

Assembly instruction:
LOAD x, r0
 	
Machine code instruction:
`1010 000 XXX XXXXXX`
`0000 <Src 12 bits>`
	Count: 2
	
	Explanation: LOAD format is made of 32 bits (2 words)
		Count: 1
		
		Explanation: LOAD instruction accesses memory once, example:
		
		- LOAD a, rC = rC <- M[a]

Assembly instruction:
LOAD y, r1
 	
Machine code instruction:
`1010 001 XXX XXXXXX`
`0000 <Src 12 bits>`
	Count: 2
	
	Explanation: LOAD format is made of 32 bits (2 words)
		Count: 1
		
		Explanation: LOAD instruction accesses memory once, example:
		
		- LOAD a, rC = rC <- M[a]

Assembly instruction:
ADD r0, r1, r2
 	
Machine code instruction:
`0001 010 000 001 XXX`
	Count: 1
	
	Explanation: ADD format is made of 16 bits (1 word)
		Count: 0
		
		Explanation: ADD instruction does not access memory

Assembly instruction: SUB r0, r1, r3 **Machine code instruction:**	**Count:** 1 **Explanation:** SUB format is made of 16 bits (1 word)	**Count:** 0 **Explanation:** SUB instruction does not access memory

0010 011 000 001 XXX		
Assembly instruction: MUL r2, r3, r4 **Machine code instruction:** 0011 100 010 011 XXX	**Count:** 1 **Explanation:** MUL format is made of 16 bits (1 word)	**Count:** 0 **Explanation:** MUL instruction does not access memory
Assembly instruction: STORE r4, z **Machine code instruction:** 1011 XXX 100 XXXXXX 0000 <Src 12 bits>	**Count:** 2 **Explanation:** STORE format is made of 32 bits (2 words)	**Count:** 1 **Explanation:** STORE instruction accesses memory once, example: - STORE rA, c = M[c] <- rA
Grand Total: 12	**Total: 9**	**Total: 3**

Once completed, submit it on Crowdmark as your answer to Question 2.