VLSI Design 2EC501

Topic: 4 To 16 Decoder Using Verilog

Special Assignment 2024

Submitted to

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Submitted By

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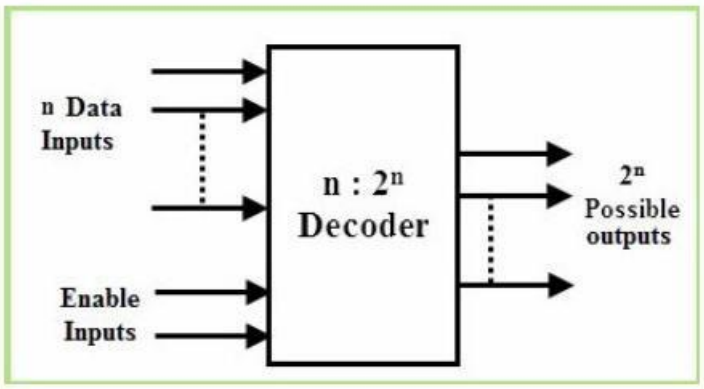
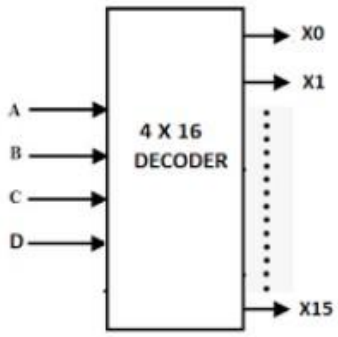
Introduction

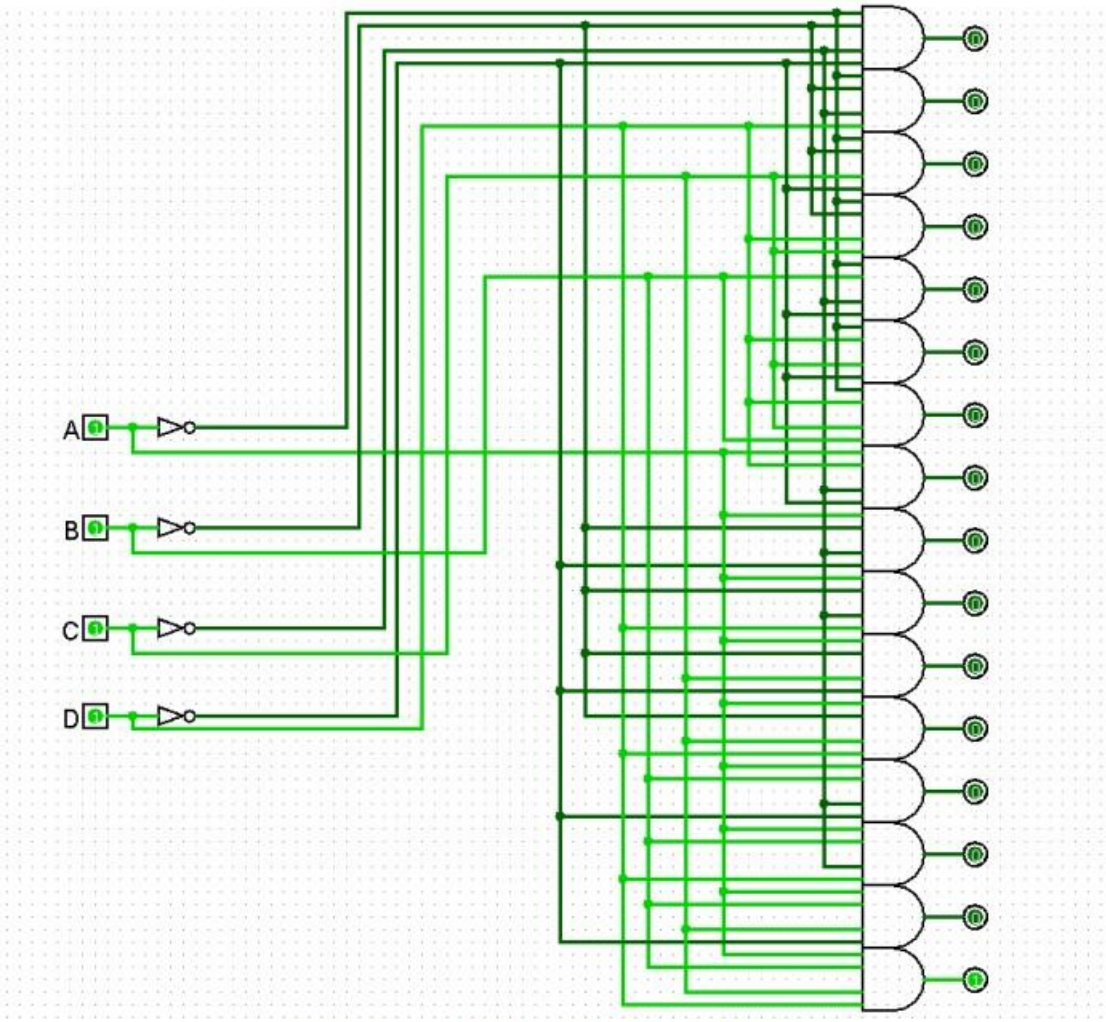
A decoder is a combinational circuit that has 'n' input lines and maximum of 2n output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code. The outputs of the decoder are nothing but the min terms of 'n' input variables lines.



A 4 to 16 decoder is a device which takes in 4 inputs in binary form and gives out the output in 16 bits, it has 4 input lines and 16 output lines. One of the major places its used is to demultiplex in a 4 to 16 demultiplexer, it's also a form to decode the 16-bit information which is encoded by the 4 to 16 encoder, all this is done to reduce the packets of information to be transmitted yet having the same amount of information we had before. These inputs are in sequence, assuming that A, B, C, D are the input then A is the MSB, and D is LSB, similarly if we take the output from O0, O1, O2 ……., O14, O15; O0 is the LSB and O15 is the MSB. Here the output is taken as Y0, Y1…. Y14, Y15 and it's in the same faction as before.



Logic Diagram



Logic Diagram of 4x16 Decoder in Logisim

The 4-to-16-line decoder can be constructed using either 2 to 4 decoder or 3 to 8 decoders. The truth table for the 4-to-16-line decoder is shown below. We have designed the 4 to 16 decoders using 4 not and 16 and gate in Logisim.

Truth Table

A	B	C	D	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

When all input is are 0 the output of the decoder Y1 and all input are 1 then the output is Y15.Decoder basically switches between 0 to 15 depending on the input. Now for implementing the decoder on the micro wind we write Verilog code on Quartus. The Verilog code for the 4-to-16-line decoder is given below.

Uses of Decoder:

Address Decoding in Microcontrollers and Microprocessors: Decoders are used to select specific memory locations or input/output ports in microcontrollers and microprocessors. They help determine which peripheral or memory location is being accessed.

Multiplexing and Demultiplexing: Decoders are often used in multiplexers and demultiplexers to select one data input from multiple sources and route it to a specific output line. In demultiplexing, a single input is split into multiple outputs.

Seven-Segment Display Drivers: In digital displays, such as seven-segment displays commonly found in calculators, digital clocks, and other devices, decoders are used to convert binary input data into the seven-segment display format, allowing you to show numbers and some letters.

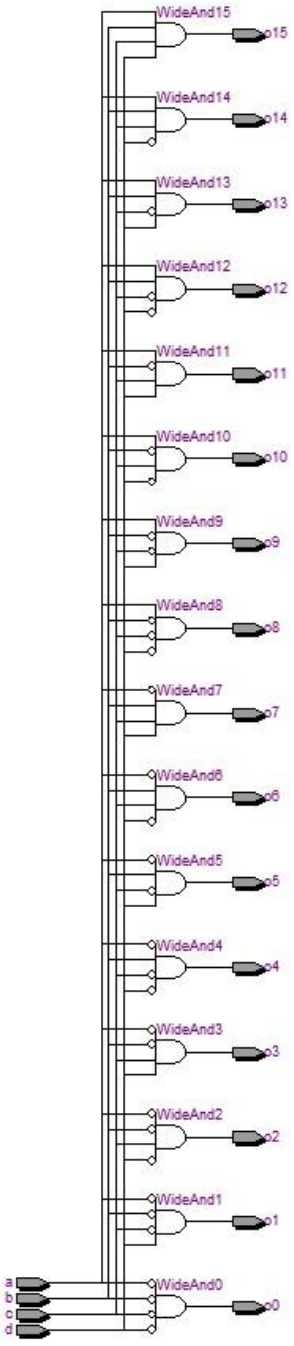
Memory Chip Select: In memory systems like RAM and ROM, decoders are used to enable or disable specific memory chips or banks, making it possible to access the desired data.

Verilog Code:

```
module decoder(a,b,c,d, o0,o1,o2,o3,o4,o5,o6,o7,o8,o9,o10,o11,o12,o13,o14,o15 ); input a,b,c,d; //4 Bit Input
```

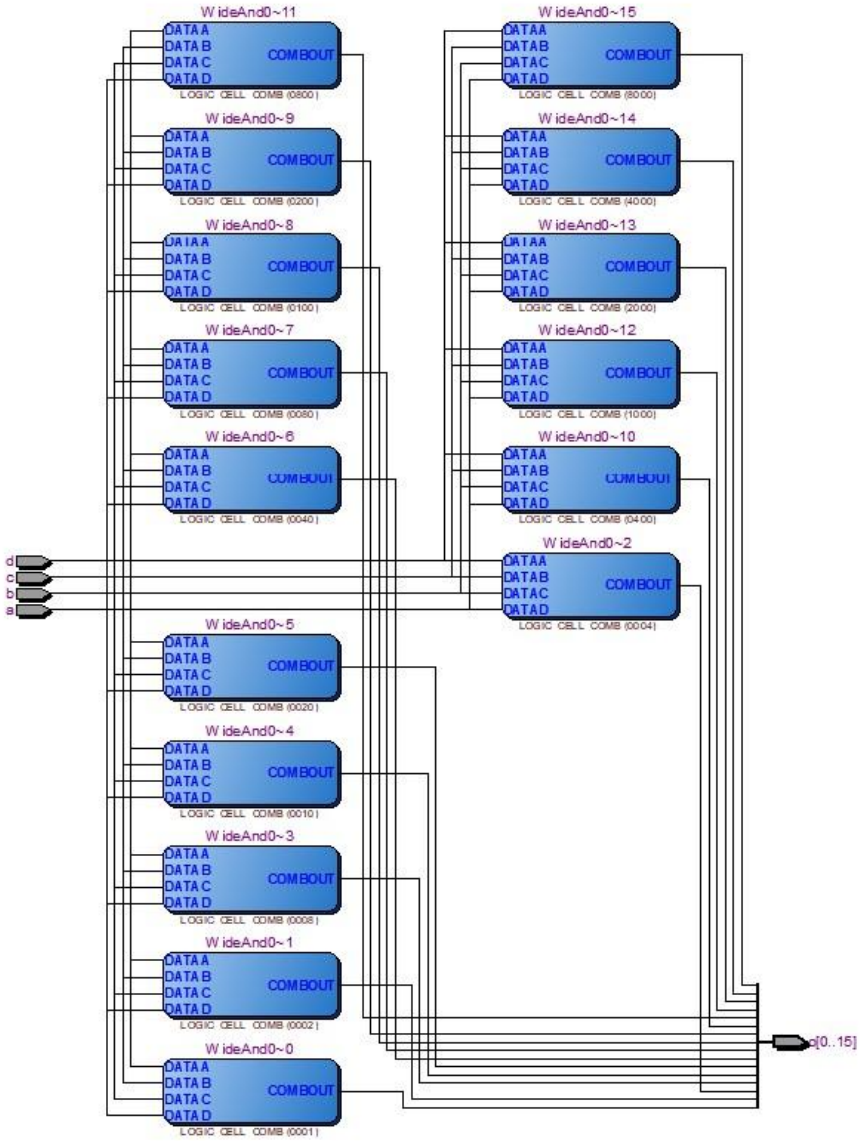
```
output o0,o1,o2,o3,o4,o5,o6,o7,o8,o9,o10,o11,o12,o13,o14,o15; //16 Bit Output
wire na,nb,nc,nd; not(na,a); not(nb,b); not(nc,c); not(nd,d);
and(o0,na,nb,nc,nd); and(o1,na,nb,nc,d); and(o2,na,nb,c,nd); and(o3,na,nb,c,d);
and(o4,na,b,nc,nd); and(o5,na,b,nc,d); and(o6,na,b,c,nd); and(o7,na,b,c,d);
and(o8,a,nb,nc,nd); and(o9,a,nb,nc,d); and(o10,a,nb,c,nd); and(o11,a,nb,c,d);
and(o12,a,b,nc,nd); and(o13,a,b,nc,d); and(o14,a,b,c,nd);
and(o15,a,b,c,d);
endmodule
```

RTL Viewer in Quartus:



RTL (Register Transfer Level) schematic show us the gate level schematic of the 4-to-16-line decoder.

Technology Map Viewer in Quartus



Technology schematics show us the architecture-specific schematic.

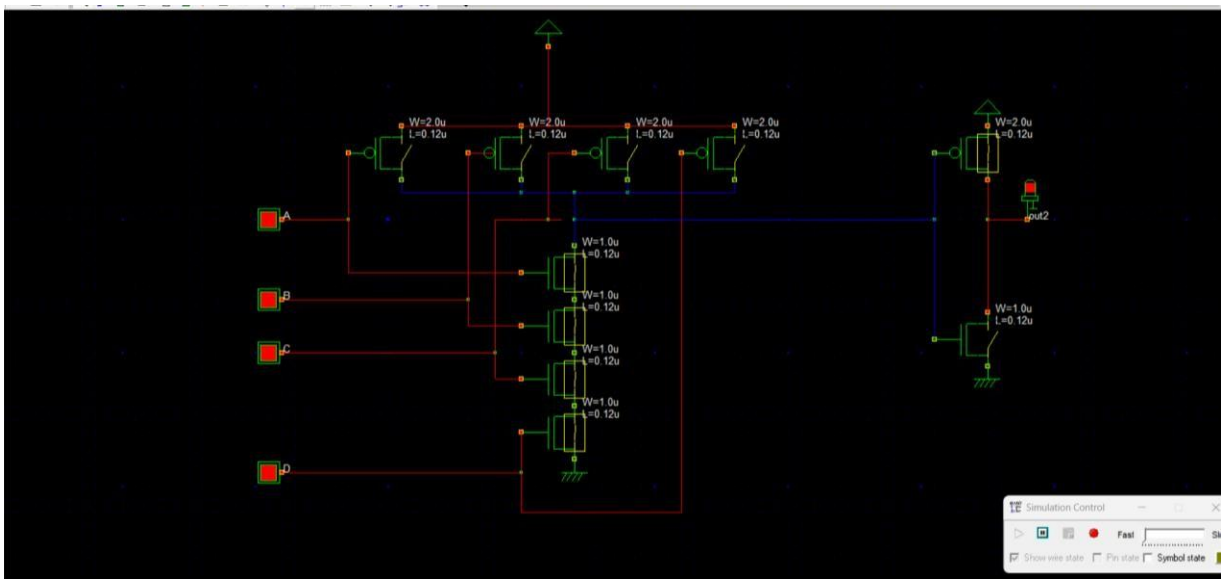
Questions:

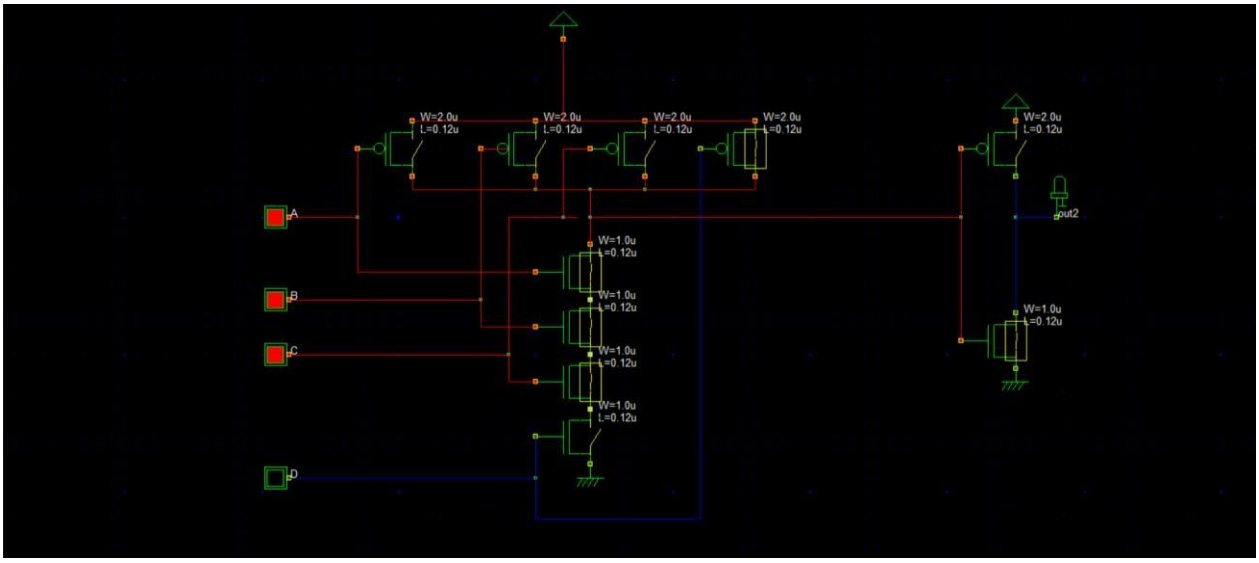
1) Find out the optimized Boolean equation:

For O0: O0 = A'B'C'D'
For O1: O1 = A'B'C'D

For O2: O2 = A'B'CD'
For O3: O3 = A'B'CD
For O4: O4 = A'BC'D'
For O5: O5 = A'BC'D
For O6: O6 = A'BCD'
For O7: O7 = A'BCD
For O8: O8 = AB'C'D'
For O9: O9 = AB'C'D
For O10: O10 = AB'CD'
For O11: O11 = AB'CD
For O12: O12 = ABC'D'
For O13: O13 = ABC'D
For O14: O14 = ABCD'
For O15: O15 = ABCD

2) Draw the transistor level schematic for CMOS/MOS'S implementation.

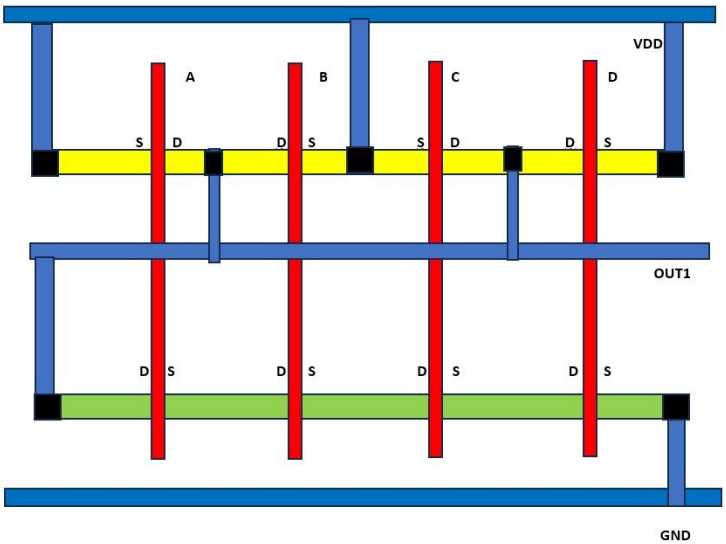


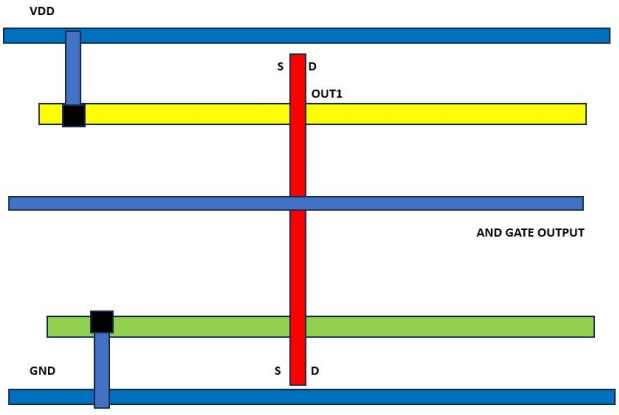


➢ As, I formed 4 input AND gate schematic, for first Boolean function. All the 16 are like the first one.

➢ This schematic is drawn or simulated on dsch03 software, as we can see that, if all buttons are pressed than led will glow, if single button is not pressed than led will not glow.

3) Draw stick diagram for above implementation level using proper color code.





4) State the various levels of VOL corresponding to various transistor statuses.

➢ In a 4-to-16 decoder, the levels of VOL (Output Low Voltage) can vary depending on the transistor statuses, which are influenced by the logic levels of the input lines. VOL represents the maximum voltage at which an output is considered "low." Here, I'll provide an overview of the transistor statuses and the corresponding VOL levels for each output line based on the input conditions:

Transistor ON (Active): When a transistor is ON (active), it means that the input combination selects that output line. In this case, the output level is typically close to ground (0V) since the transistor actively connects the output to ground. Therefore, VOL for an active output is typically very low, approaching 0V.

Transistor OFF (Inactive): When a transistor is OFF (inactive), it means that the input combination does not select that output line. In this case, the output line remains high or at its inactive state. VOL for an inactive output is typically closer to the supply voltage (VCC) or the high logic level, depending on the technology used. It's important to note that the VOL for an inactive output is not zero; it's closer to VCC.

It's crucial to understand that VOL for the active outputs is low (close to 0V), while VOL for the inactive outputs is relatively higher, typically close to the supply voltage (VCC). The specific voltage levels can vary based on the technology and the actual circuit implementation, but this general behavior is consistent with most digital logic circuits.

5) Find an equivalent CMOS inverter circuit.

➢ As we have not drawn the transistor level schematic, we can’t find the equivalent cmos inverter circuit.

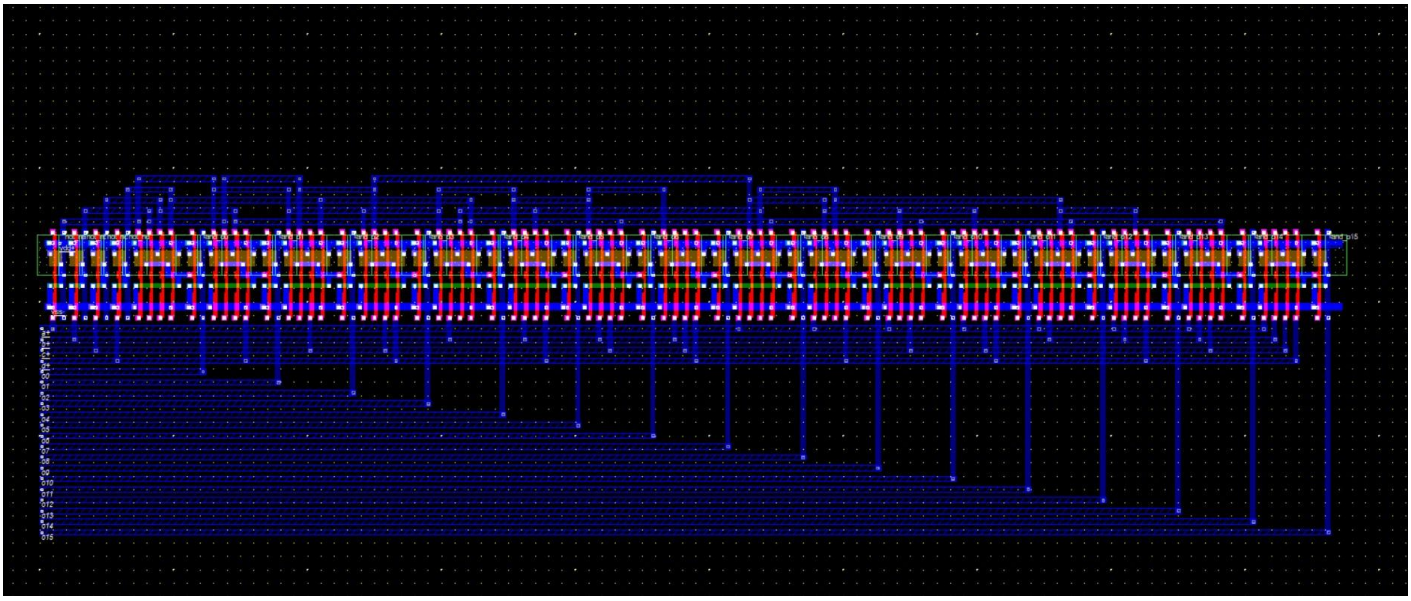
6) For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value of that resistance?

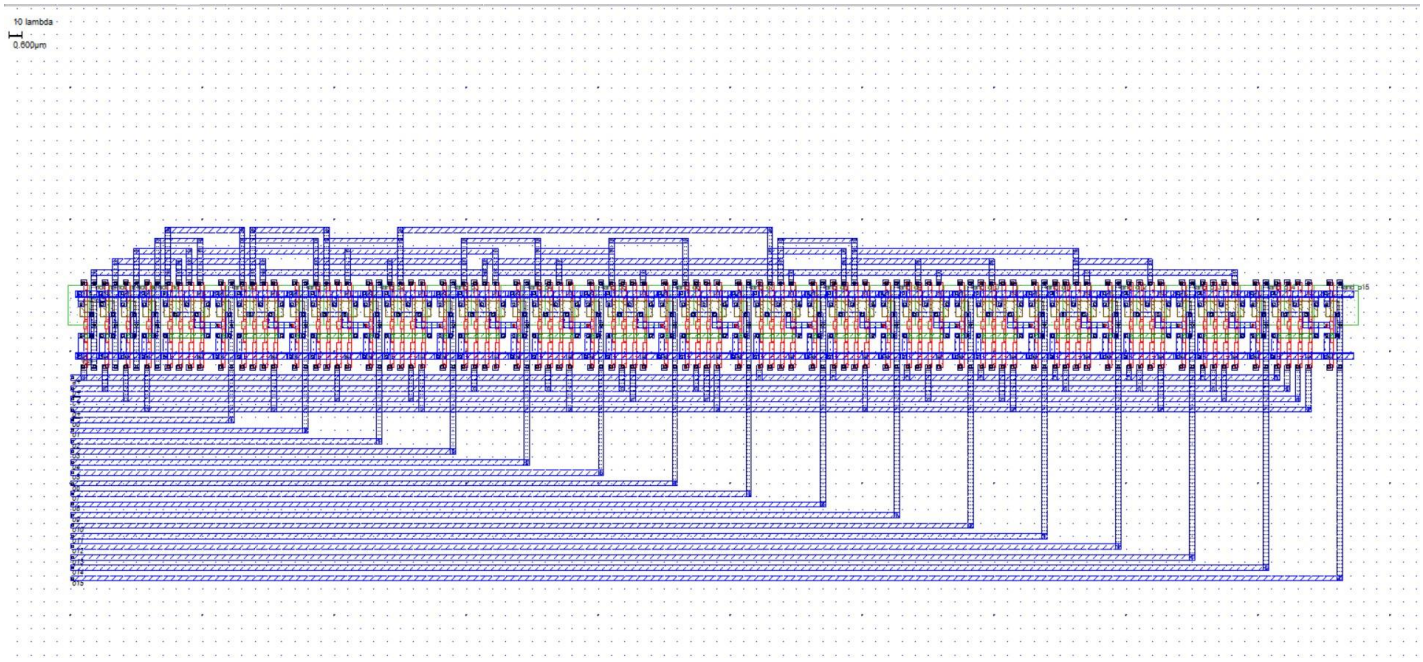
➢ As we have not implemented CMOS circuit this is not applicable.

7) For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the value of that resistance?

➢ As we have not implemented CMOS circuit this is not applicable.

8). Prepare the layout using Micro wind tool.

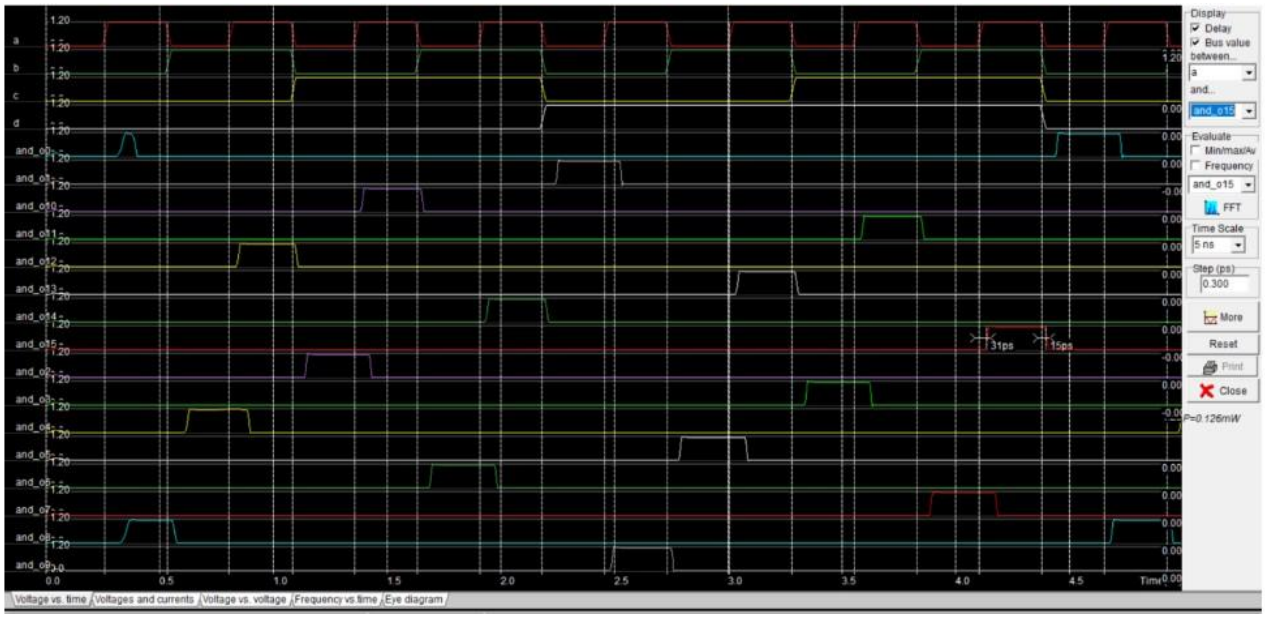




4 to 16 Decoder layout in Micro wind We Compile the Verilog code into micro wind and get these results. Here A, B, C, D are the inputs and o1 to o15 are output is shown. We prepare the 4-to-16-line decoder in 0.12 micrometer technology.

9)Simulate it for various combinations of inputs.

For ABCD=1000 then it active O8:



Here You can see when input is of ABCD is 1000 the output is o8 and when input of ABCD is 0100 then output is o4. For 16 combinations of the input, we have get the 16 output ranging from o0 to o15.

10) Measure the rise time, fall time, propagation delay and other parameters.

➢ In the above figure you can see that the rise time is 31ps and fall time is 15ps
Now propagation delay=rise time+fall time/2
So, propagation delay=31+15/2 =23 ps

➢ The propagation delay of the circuit is 23ps

Conclusion: The Main aim of this project is to generate/make the layout for the 4 to 16 decode. For 4 to 16 decoder first we have make truth table and from the truth table we have developed gate level circuit. To draw the transistor level schematic manually for such a big circuit isn't feasible. So, we have use Verilog. We have written Verilog code of 4 to 16 decoder using Gate level modelling in Quartus II tool and generate the RTL view of the circuit. It generates the most optimized circuit for this decoder. Then we compile this Verilog code in micro wind, and it generates the required CMOS and metal connections with wire as per the code written. In the simulation we have got the required results. For 16 combinations of the input we have get the 16 output ranging from o0 to o15. The raise time and fall time for this circuit is 31ps and 15ps respectively. The propagation delay of this circuit is 23ps.