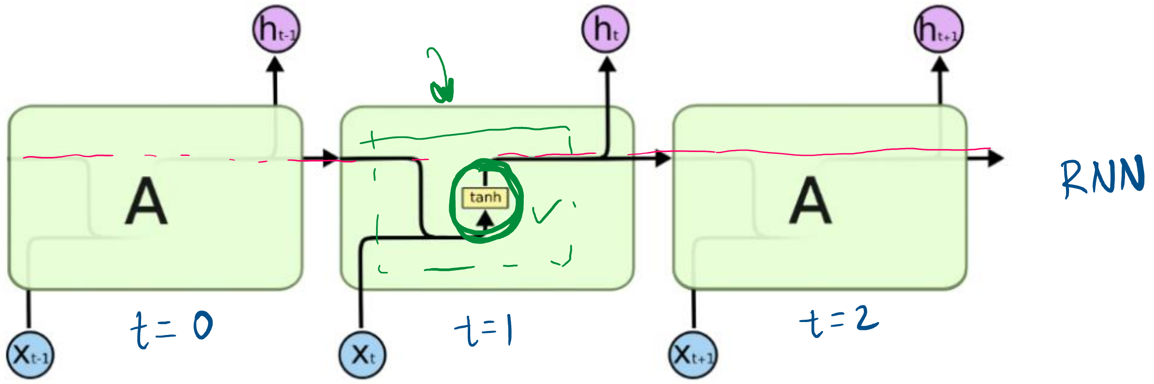
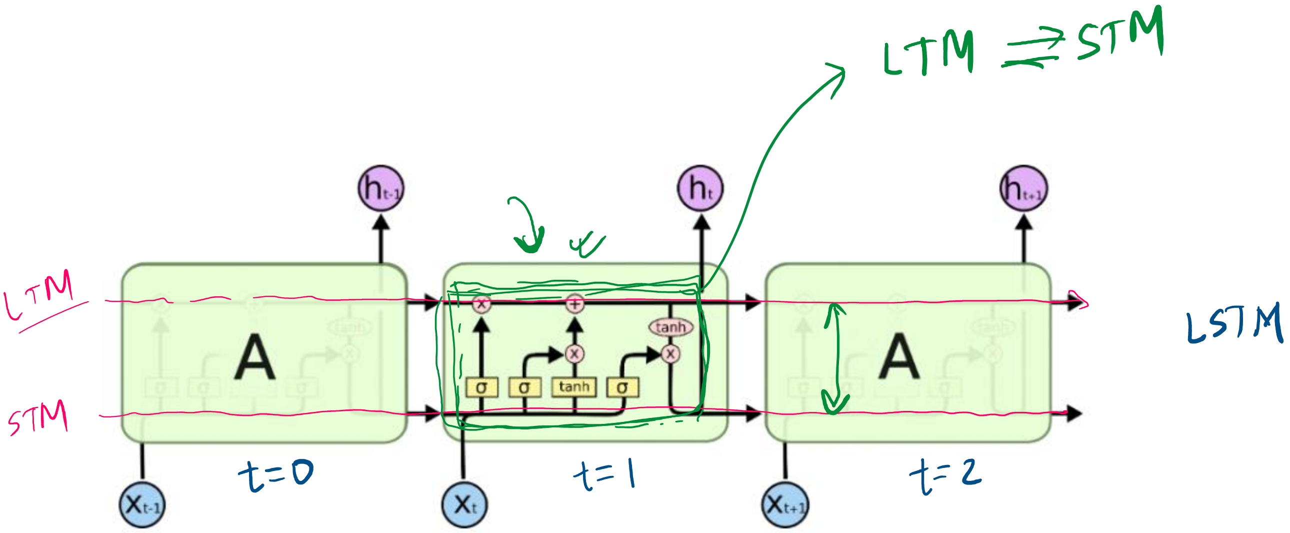
LSTM Architecture

21 August 2023 18:41

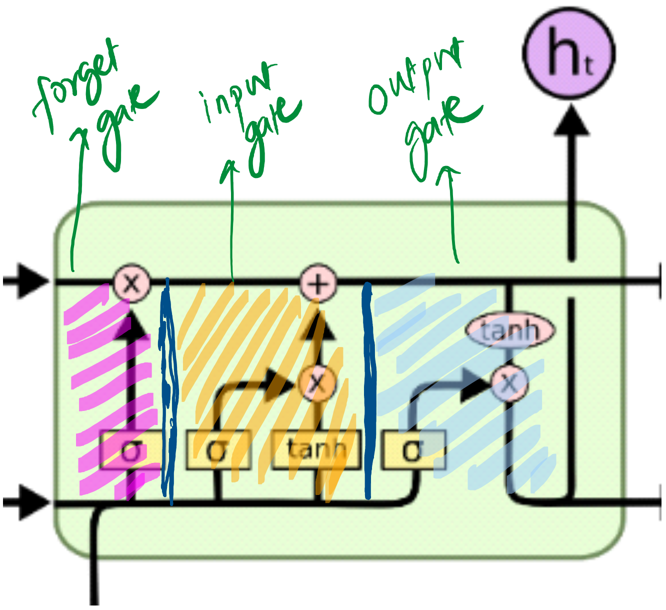


h_{t-1}
h_t
h_{t+1}
A
tanh
A
X_{t-1}
X_t
X_{t+1}
t= 0
t=1
t=2
RNN



LTM ⇄ STM
h_{t-1}
h_t
h_{t+1}
LTM
STM
A
tanh
σ
σ
tanh
σ
A
LSTM
X_{t-1}
X_t
X_{t+1}
t=0
t=1
t=2

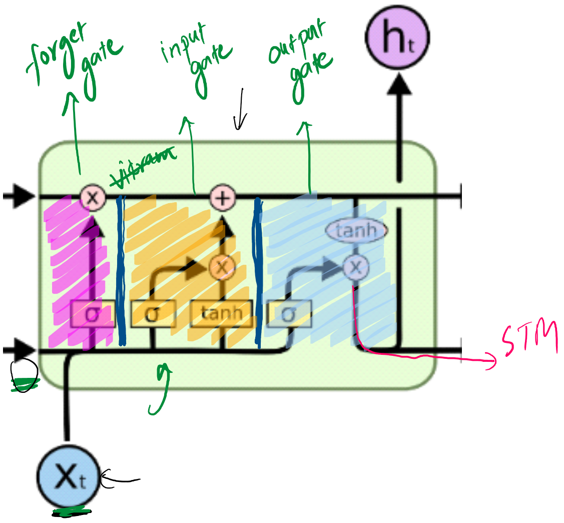
gates



forget gate
input gate
output gate
h_t
tanh
σ
σ
tanh
σ

LSTM Gates

21 August 2023 19:06


forget gate
input gate
output gate
~~vikram~~
h_t
σ
σ
tanh
σ
tanh
STM
X_t

forget

input

LTM

remove

1000 prapor vikram jr

yes

NO

input

output

output gate

↳ Short term memory

create

LTM

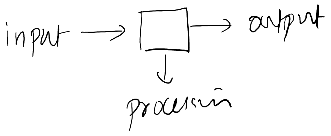
↓

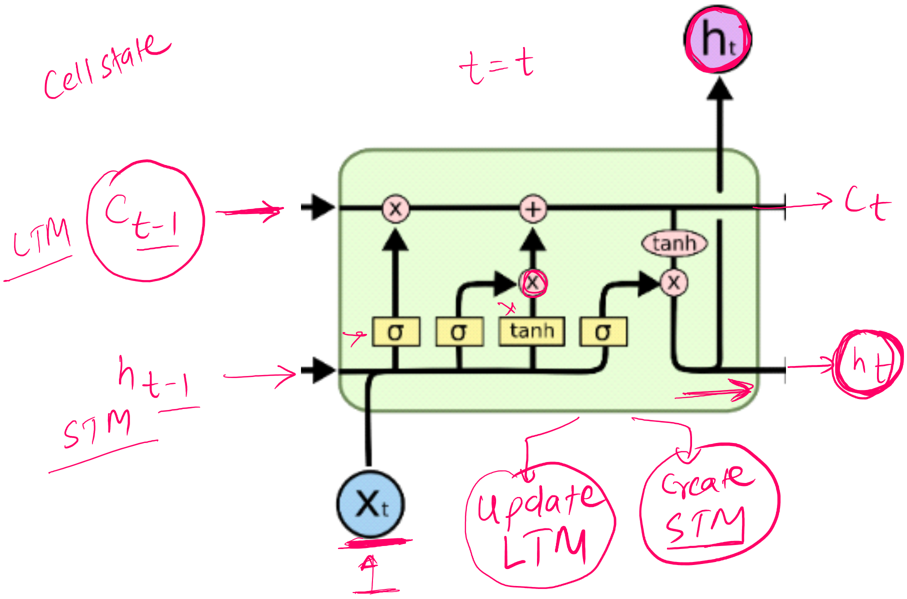
add

Summary

21 August 2023 19:29

LSTM


input
output
processin


Cell state
t=t
LTM
C_{t-1}
C_t
h_{t-1}
STM
h_t
h_t
σ
σ
tanh
σ
tanh
×
+
×
×
X_t
Update LTM
Create STM