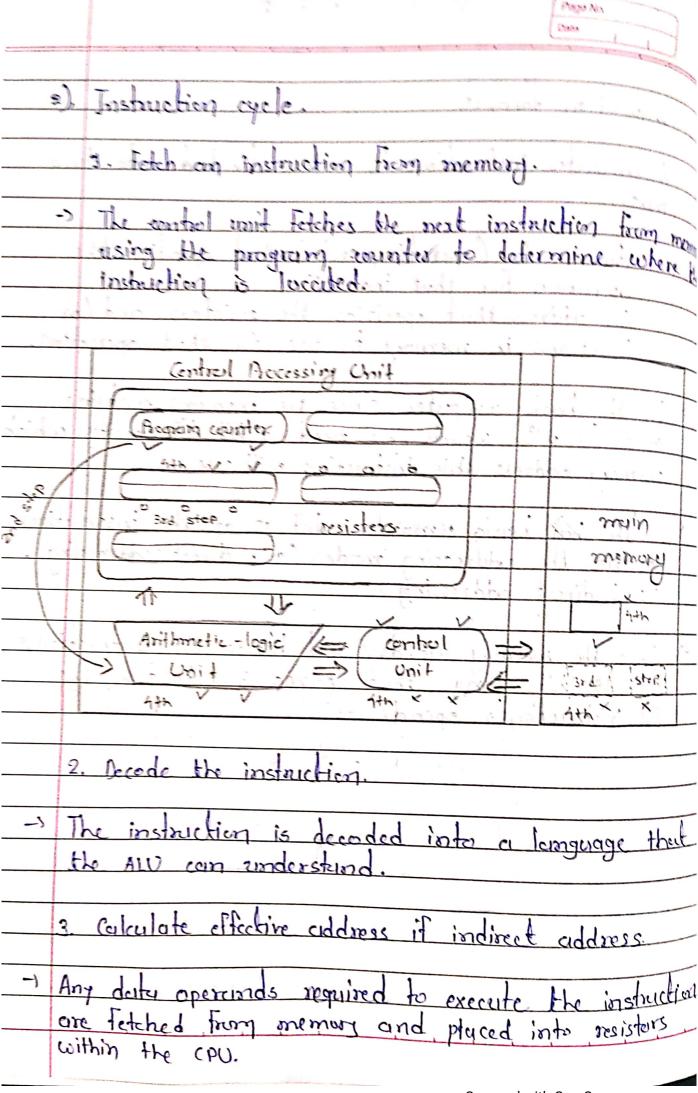
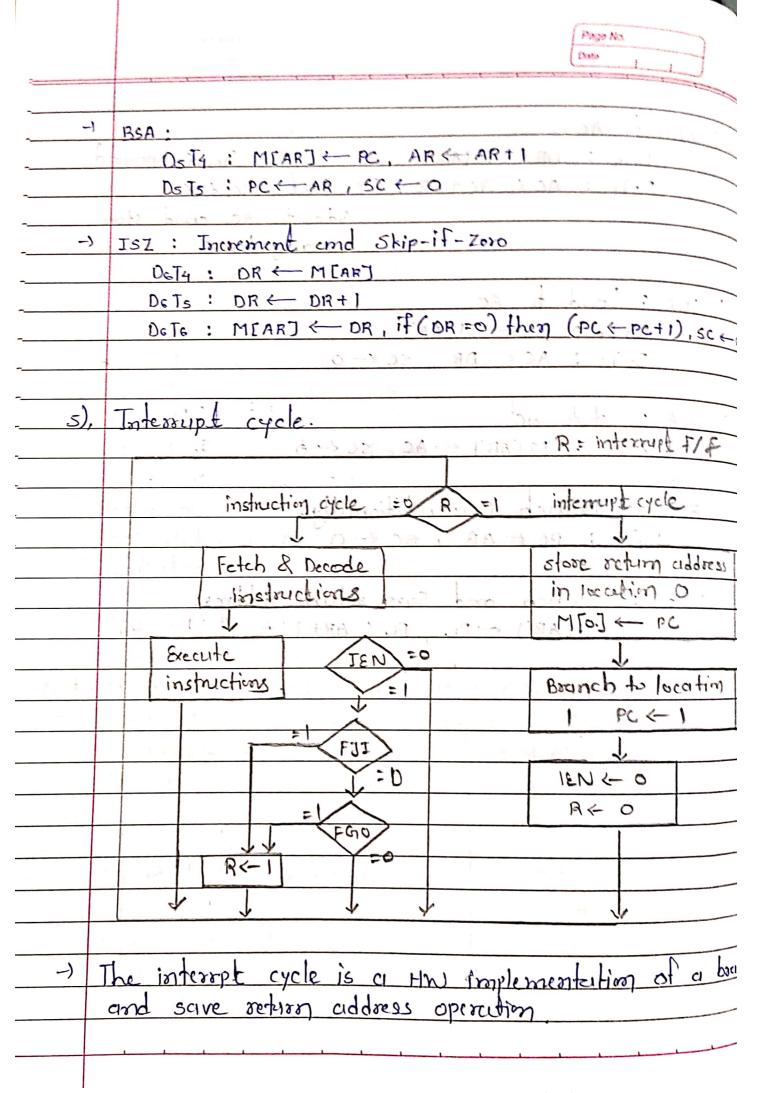
1	ch: 2.
1	(Basic Computer Organization & Dolyn)
-	
1),	Instruction formert.
->	A computer instruction is often divided into two
	and carried tens sid recipies many labour sin "
	operation for that instruction
	- An address that specifies the resisters and lox
	locations in memory to use for that operation.
-)	In the hasic computer, since the memory contains 4096 (= 212) words, we need 12 bit to specify which memory address this instruction will use
-> -	In the Kext beisic competer, bit is of the instruction
	specifies the addressing mode (o : direct addressing,
	1: Indirect addressing)
-)	Since the memory words, and hence the instructions, ever 16 bits long, that leaves 3 bits for the 16th instruction's opende
	eve 16 bits long, that leaves 3 bits for the
	Ex instruction's opcode
	Instruction forment.
	Instruction formale.
	15 14 12 11
bot	· province oprode ciddress
	1 , and the second of the seco
	addressing mode
	earthbo to sibrar to marches worlds stolicies &
ررودان	cheri all campa e trainger character pais
3.11	stores while the uty eyes a mineral prof bridger, son,
	150 militari



					Pa Dat	ge No.		
						T		
	4. Executo	instruc	tion.	en o-		T v Pi	s viril.	,
		Augai -	17 40 4	157 4	(1 1)	a de la companya de	· Freeze	0
1	The ALU	executes	the Instr	uction	and pla	uce s	result	מי ב
	registers	or mem	ory.		146		,	
			7					
		•	90	i			2	
3),	(ommon.	-bus cio	chitecture		1			
		1	- 80	Land and the second sec		1	1	
->	The regist	ers in	the basic	compu	ter are	CO	meded	
	rising a	bus.		1 / 1	(5)	<i>p</i>	1	
	51 .	71	ন্					
-1	This gives	sav	ings in a	breyita	y over	Con	mplete	
	connection	& beton	registers.		52-5	-4		
	out of the	.	1 11100 240		5, -5	Bus	- Eller	<i><-</i>
inst	is Korre	1 Total	micmory unit	151155 3	10	1	rock so	
	14 3 12 13 T	1		d Addr	201	6	hartest	
			write real	d noon				
5)	ed a'col		LAR ON	233	1 3891	"	51 241	1 -
. 7	itiand his	1 1/20	L'D INR GLI	041	1 dei	5/1	Of the	1
			PC	1		2		
-	i most h	obisol ai		A Prince	Trib A	301	Luxbi	
	· H.H - X	635717	DR	:0161	2 2 3 6 7 7	3	ion all	-
			LO INR CLI	3 [100	d state	
	2 4	<u> </u>		_				+
	5	ALU	AC			14	<u>, , , , , , , , , , , , , , , , , , , </u>	
			LO INRICL	R	34.34	:	mush	11
		INP	17					1
) IR			5	desa	
Ma	States Amos	3 1	LD	88 /1	H.L.	1	the i	
1	dia dua	1	TR	a JA		6	·lo.1	
13			> OUTR	CLRA				
			rp	manufacture in the same and a state of the same	cluck			
		4- 16	Pit consus	1 bus	5		42,000	

	Page No.
	Date
	Three control lines 52, S. and Sol control which
	resister the bus sclects as its input
	the sample been opidented at reference 114 its
<u> </u>	52 5, 50 Register . Marie 10
	0 0 0 ×
	O O I AR
	O 1 O PC 3 1 10 2 2 1 1 2 2 1 1 2 2 1 2 2 2 2 2 2
	O I I DR
	bytander so whomes Aciend it in anothers and a
	I O 1 IR
	1 0 TR
	ofologina y rom indimensing services is some
	emplement 16 lack to contraveno
	CITIES CONT. C. X.C. IVI.
	activated, or the memory will have its road signal
	activated
	1.00
)	The 12-bit resisters, AR and PC have o's loaded
	conto the bus in the high order 4 bit positions.
-)	
	the doite comes from the low order & - bits on
	the brus
4),	Memory reference instructions.
>	AND to AC
	DOTY: DR - MEARI
	DOTS: AC← ACA DR, SC←O AND with AC

				Page No.
				Date
ب	ant	to Ac		
				· A+4
		N.T.	CARTA . M - A CRA	Read operand
	_	DIS, AC	ICTOR, E - Coul	, sc + 0
			Add to	Ac example store
		. 055	in Time to baccing	y in s
->	Inn		I SIA LAG	· 80 : 11/30
	LUA	COUNTRY AC	1+R0	- AC LaCaC
		Do Tal DRZ	RJ C- DR , FRAZME	ATT : aleft
		D ₂ T ₅ : AC ←	DR , $SC \leftarrow O$	
<u> </u>	CT 0	1		
	5 A	: store AC		mi donastal de
		N3 14 : M[AIR]	$]\leftarrow AC$, $SC \leftarrow O$	
		2 1		
->	BUN	: Branch O	neonditionally.	
	1	D4T4 : PC ← A	A , 50 ← 0	
			255 A. S.	· · · · · · · · · · · · · · · · · · ·
-)	BSA	: Brunch ar	no Sare return	address
		M[AR] <	PC PC - AR+1	
			. '	
		Memory PC, AR a	t time Ty Mem	on PC, After execution
2	20			0 BSA 135
1	×=21	Next Instruction	21	Next Instruction
				-
412 =	115	¥ 1000	135	
117	135	Subscertine		Subscutine
+	136	SUBJECTIVE	PC = 136	
	ţ.	V		V
		1 BUN 135		1 BUN 135
0.1	b ten	Memory resistant	cycle is or Hy	Memory
	1	a situal	cycle is or the	ar and have
+		1 1 1 1 / 2	1000	Zela Mile
+				



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Date	

-> At the basis 1		
instruction that is mext inst	making and the	
instruction that is read from	accept cycle, the	
address y	memory is in	

a branch instruction that sends the control to an interrupt service reutine.

Memory

	Before interrupt		After interrupt		
0	1 c		D	256	1
1	0 BUN 1120	# 	PC = 1	0 BUN 1120	1
255	Main	2,74	255	Main	
256	Program	The second second	2.96	Progrem	
1120	1/0		1120	1/0	Ì
	- Program			program	
	7 BUN 0	0.28.0	178 119	T BUN O	

Register transfer statements for interrupt cycle.

-if 18N (FGI + FGO) To'T, 'T2' ←>

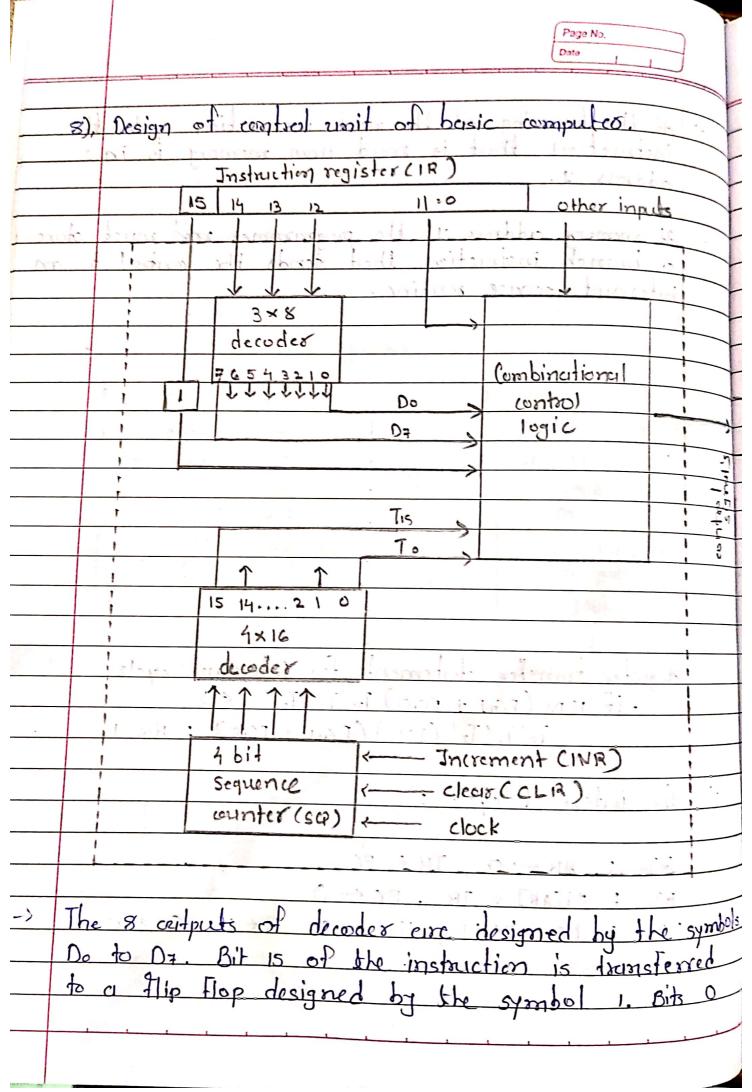
To'T, 'T2' (IEN) (FGI + FGO): R←1

The interrupt cycle:

RTO: AR CO TR CPC

RT, ; M[AR] - TR, PC - O

19T2 : PC+PC+1, IFN +O, R+O, SC+0



	Page No. Date
	through 15 are applied to the control logic gates. The
	4-bit sequence conjunter can count in binary from
	times inches
-1	100 18 14 8 01 10
	signals To through To
	J. D. L.
	remoit character Charact
(a)	Difference: Direct and Indirect addressing modes.
-67,	modes addressing modes
	Direct addressing Taling Andresing
	Direct addressing Indirect addressing
:	S. Hearborn Soul Mar Hearborn March 1900 Miles Miles
•	Allinger Halling I will of the all But I
1,	Address field contains the
1	the effective address of refference of effective
	operand. de besimps di caddress.
2.	Requires conty one memory 2. Requires two memory
- 1	references meterences
	Country Letts. Sols
3.	Fast addressing 3. Slower than direct
	addressing mode
N. V	5. Thereding Complex devoting Pricing deceding
4	No Further classification 4. Further classified into
1.	two categories
-	TWO CONEGONIES.
	1 F 11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
5.	No Eixther conculation 5. Régerire tinther conculation
	is required to perform to find the effective
	the operation. address.
	Suit of the

			Page No. Date
٦),	of isonid tal	Hardwired & microp	03 ((3)) (4)
lo	Attributes	Hardwired control	Microprogrammed control unit.
-Ci	all at the t	shout me where	old to give sit ?
┪.	Speed	Speed is Fast	Speed is sluw
2.	Cost of implementation	More costlier	Cheaper
	ion	Deel 1 1 1 packs a	on the Land
3.	Flexibility	Not flexible to	More flexible to
	winters black	system specification or new instruction	system specification or new instruction
		redesign is required	sets.
4.	Ability to a	Difficult to hundle	Easier to handle
Ĺ	handle	complex instruction	complex instruction
	complex	seb.	sets.

		accommodate new	accommodate new
14	wintern block	system specification	system specification
	withilly to		or new instruction
		redesign is required	sets. home
		4	
4.	Ability to	Difficult to hundle	Easier to handle
	handle	complex instruction	complex instruction
	complex	sels.	sets.
	instructions	Xarivala	palambha ini
	showe o	Vizzach han	Ü
5	Decoding	Complex decoding	Easier decoding and
estr	i beiliscola	and sequencing	sequencing logic
	23 , , , , , , , 6	logica	J. J.
	-	J	
6, 1	Applications	AISC Microprocessor	CISC Microprocessor
	without it	had of more proverting	of havinered i
7.	Instruction	Small	large.
	set of size		

No.

		. (soft ingress is	Page No. Date
8-	(ontrol	Absent	Present
9.	Chip circul	Scorenge so poli	dayes Moreshorsh
10,	Occurrence	Courrence of	is less.
	+ hateman	x) of in codina	in linerical decreed and
	1 it hot, we	कर उसे धरे थर वर्ष	Heradecinal mumi
		6.36	Turo poes assentien
1	in line entrolar	in shidney (son)	defined Code
		. considerations	and formal is some party.
			Scanned with CamScanner