Circuit Modeling Interview Homework

Introduction

As a part of your interview for a system modeling position we would like you to complete the following assignment. Note that this assignment **should not take more than 2 hours** to complete. We suggest putting the resulting code into GitHub and sharing the link with us. For privacy you may use a private repository and add **miaozxc** GitHub users as collaborators.

WARNING: all equations and codes should be done by you instead of copying and pasting from other places.

The goal

Please solve the circuit modeling questions below. Each question contains a circuit diagram in the corresponding figure, here is the guide to format your answers:

1. Write down the equation(s) to describe the current to ground Iout.
2. Implement the solution in Python or Octave
3. Verify your solution by testing different Vin and G values, save the corresponding Iout result. Then calculate ideal VMM I_ideal = Vin(1) * G(1) + Vin(2) * G(2) + … + Vin(N) * G(N). scatter plot Iout vs. I_ideal
    a. Assume Vin is in range of 0 - 1V, G is in range of 10 - 100 uS, Gwire = 0.1 S (or say, 10 ohm), N = 100
4. Additional requirements will be addressed in each question.

Q1: See Figure 1, please calculate Iout_a.

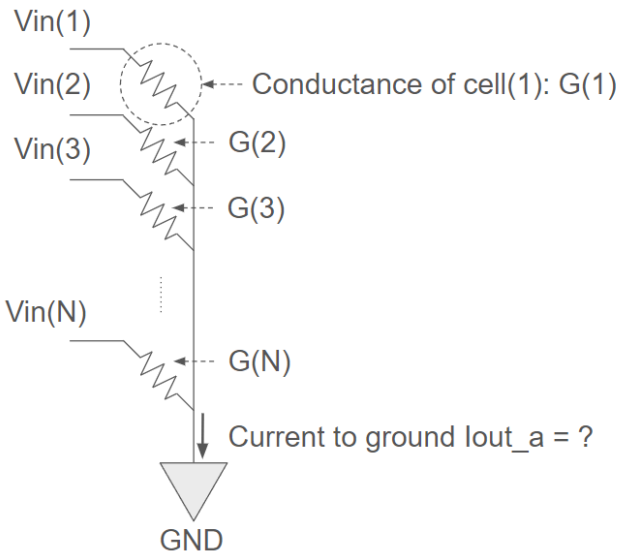

Figure 1. One-column resistor path circuit, no wire resistance.

Q2: Based on Q1, see figure 2, now we are considering wire conductance between cells. Please calculate Iout_b.

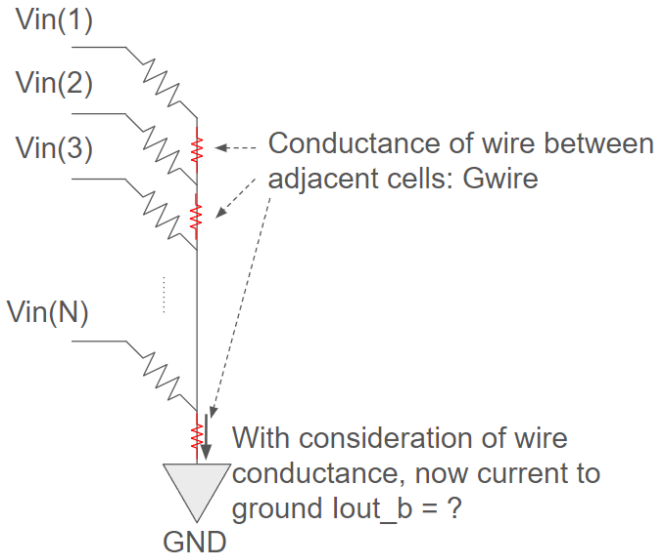

Figure 2. One-column resistor path circuit, with wire resistance.

Q3: Based on Q2, see figure 3, now we are considering two columns, and there is also wire conductance between the two columns. Please calculate the 2nd column current to ground Iout_c. Note in this question, G is no longer a vector, but a Nx2 matrix.

1: What will happen if the 1st column is not connected to perfect ground, but instead a ground with voltage offset V_offset, assume V_offset = 0.05 V.

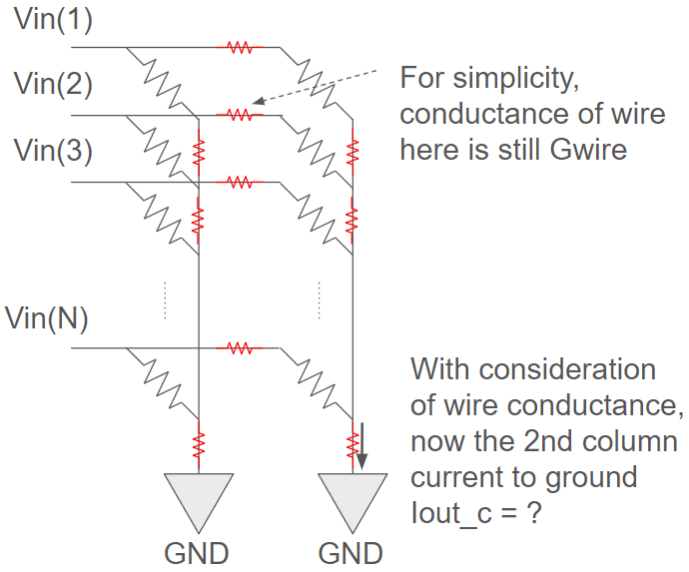

Figure 3. Two-column resistor path circuit, with wire resistance.

Q4: Based on Q3, see figure 4, now we change cells from the perfect resistor to 1T1R cell. It's fine that you skip the equation or code implementation here (if not enough time), but please answer the following questions:

1. Which 1T1R cell type (A or B) helps more to reduce the difference between Iout_d to I_ideal? Why?
2. Why does computation complexity increase when we change cells from perfect resistor to 1T1R cell?
3. If you have more time, how will you solve this problem numerically? You don't have to consider transistor gate control.

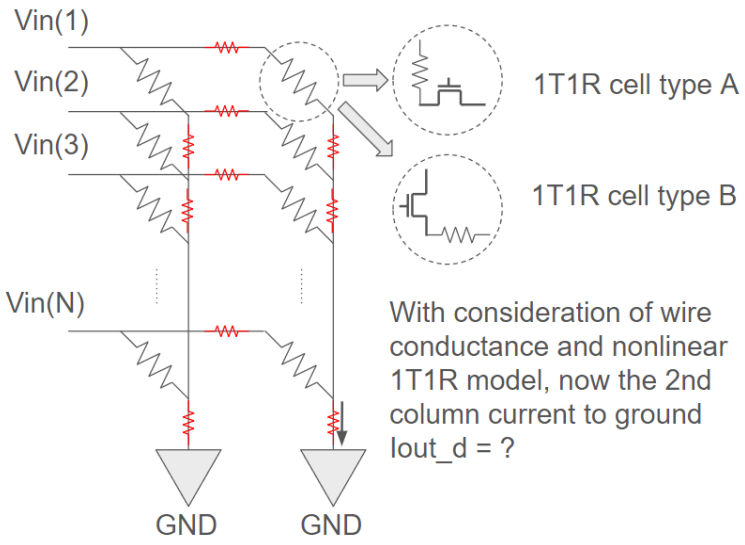

Figure 4. Two-column resistor path circuit, with wire resistance, with cell change to 1T1R cell.