ECE 115C – spring 2025

Final project Milestone 1 (20 points)

Deadline: May 24 2025, 11.59PM (Saturday)

(Late penalty: 5 points per day. Submission will be closed **1 day** after the deadline)

Version history: (Don't download this file. Always refer to the latest version directly from Bruin learn)

Date	**Change**
May 17, 2025	Original document

The parameters required to calculate the sizes and delays of the logic gates are given in the below Table1. These correspond to the gpdk45nm process that we have in cadence.

Cgate'	Cdiff'	Rn'	Rp'	tinv(used in logical effort normalization for VDD = 1.1V)
0.66fF/um	0.72fF/um	3.45 kohm-um	5.16kohm-um	3.92ps

Table 1. Hand-calculation parameters for the 45nm GPDK

Deliverables:

- Submit a report containing (max 3 pages):
  - tinv vs VDD plot (explained in previous document).
  - Pow_{FO1} vs VDD plot (explained below)
  - Architecture choice with explanation on why you chose the architecture
  - First cut logical effort calculation for worst case delay (C0 to C4 path)
  - First cut cadence schematic snapshot of your circuit
  - Note: You can change your architecture/design choices in your final submission later based on your reasoning. You will not be penalized for it.

Testing the circuit:

- The power/energy of the circuit will vary depending on the input pattern combination. So, to compare all your results easily, we will simulate and optimize just for one test case.
- Give G1 = G2 = G3 = G4 = 0; P0 = P1 = P2 = P3 = 1; Give a vpulse input for C0 with frequency of 100MHz.
- This combination will ensure that the input C0 change will propagate all the way till C4.
- Report all your power, delay, energy and EDP numbers with respect to this test case.

Estimating power for different VDD:

- **Do not sweep** your full circuit with different supply voltages. Instead follow the method mentioned below to estimate the power for different VDD
- Make a smaller testbench: Take a reference inverter and load it with the inverter of same size as shown below. Sweep the VDD and obtain the power consumption of this Fan out-1 (FO-1) inverter (only the first inverter) with 100MHz input DIN. Let's call this plot '$Pow_{FO1}(VDD)$'
- Take your full circuit and obtain the power with the given test pattern only for VDD = 1.1V. Call this $Pow_{full\text{-}chain}$(@VDD = 1.1).
- Now you can obtain the power of your full circuit with different VDD by just taking:
  - $Pow_{full-chain}(VDD) = \frac{Pow_{full-chain}(@VDD=1.1)}{Pow_{FO1}(@VDD=1.1)} * Pow_{FO1}(VDD)$