ECE 115C – spring 2025

Final project (80 points)

Deadline: May 30 2025, 11.59PM

(Late penalty: 10 points per day. Submission will be closed 2 days after the deadline)

(This will count towards 80 points out of 100 points for the project. This should be done in **groups of 2**)

Version history: (Don't download this file. Always refer to the latest version directly from Bruin learn)

Date	**Change**
May 9, 2025	Original document

The parameters required to calculate the sizes and delays of the logic gates are given in the below Table1. These correspond to the gpdk45nm process that we have in cadence.

Cgate'	Cdiff'	Rn'	Rp'	tinv(used in logical effort normalization for VDD = 1.1V)
0.66fF/um	0.72fF/um	3.45 kohm-um	5.16kohm-um	3.92ps

Table 1. Hand-calculation parameters for the 45nm GPDK

Context (Optional read. Only for those who are interested):

One of the most important blocks in an ALU is an adder. Generation of carry bits when adding and passing it to the next stage, so that the next stage can finish the operation is the main delay bottleneck in the adders. There have been many different architectures studied over the past 40 years to optimize the generation of the carry. You will learn some of these methods during our lectures as well.

Our project will focus on one such block which is used to reduce the carry generation delay with the trade-off of spending extra power and area. You can watch this video on carry look ahead adders if you're interested, after the basics of adders are covered in lectures. (**You don't need to watch or understand it to implement the project**). Carry Look Ahead Adder (CLA) Explained

Problem Statement:

Inputs (Total 9 inputs): G_0, G_1, G_2, G_3, P_0, P_1, P_2, P_3, C_0

Outputs (Total 4 outputs): C_1, C_2, C_3, C_4. All outputs have extra load of 20fF capacitance.

Outputs are related to inputs based on the below equations:

- $C_1 = G_0 + P_0.C_0$
- $C_2 = G_1 + P_1.C_1 = G_1 + P_1.G_0 + P_1.P_0.C_0$
- $C_3 = G_2 + P_2.C_2 = G_2 + P_2.G_1 + P_2.P_1.G_0 + P_2.P_1.P_0.C_0$
- $C_4 = G_3 + P_3.C_3 = G_3 + P_3.G_2 + P_3.P_2.G_1 + P_3.P_2.P_1.G_0 + P_3.P_2.P_1.P_0.C_0$

Tasks:

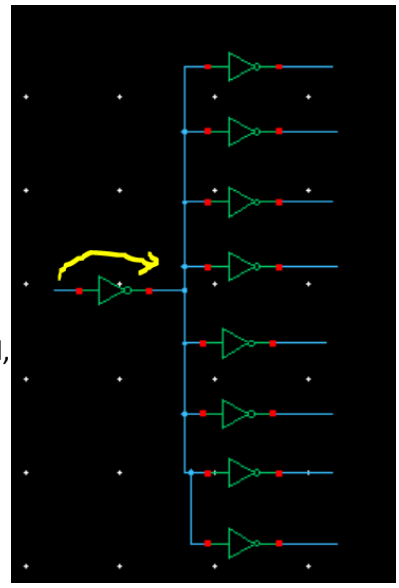
1. You have to implement this logic in cadence using the 45nm process and minimize the delay from the inputs to the final output C_4. (Use VDD = 1.1V for initial simulations)
2. You have to minimize the Energy-delay product (EDP) of the whole circuit.
3. Use stick diagrams to get an approximate area of your circuit.

Knobs you can control to optimize EDP:

- **Widths** of all the devices in your circuit are in your control. (Length should be kept fixed at L = 45nm). Optimize the delay without considering the power/energy first using the logical effort method hand calculations. **Note:** Brute force sizing of the gates to minimize delay will not be rewarded. You need to provide reason/calculation behind the sizes you chose in the report.
- **Supply (VDD)** voltage: You should NOT brute force sweep the VDD to optimize EDP. Instead follow the below method to obtain the optimum EDP.

EDP Optimization flow:

1. Obtain the 'tinv' (0.69*Rinv*Cinv) for different VDD values (VDD should be less than or equal to 1.1V). This can be obtained by simulating an inverter with fan-out N (choose large N>10) and measuring the input to output delay as shown and dividing this delay by N. This gives a reasonable approximation for tinv. Plot this as tinv vs VDD graph.
2. Using logical effort method and the above graph, plot the delay of your whole chain vs VDD. (**Note:** DO NOT brute force sweep VDD for your whole circuit to obtain this).
3. Hand-calculate the total energy dissipated vs VDD for your whole circuit. You can do this by estimating the total capacitances in your circuit from your sizing and extra load capacitances given, using the concepts taught in the lectures.
4. Finally combine both the graphs from 2 and 3 to obtain the Energy-delay product vs VDD graph using any software that you are familiar with (Excel, MATLAB, python, etc.)



5. Based on this graph, choose the optimum VDD.
6. Now simulate the energy, delay, and energy-delay product for nominal VDD (1.1V) and your chosen VDD. This gives the final EDP for your circuit. (Note that this value will not match exactly with your calculation and that's fine. Hand-calculation gives an approximate value to quickly optimize the EDP)
7. You can go back and optimize the architecture or sizing to improve your EDP. (**NOTE:** only educated resizing based on calculations. Brute force sizing without any explanation will be penalized)
8. Report the final EDP you obtained from simulation and hand-calculation.

Deliverables:

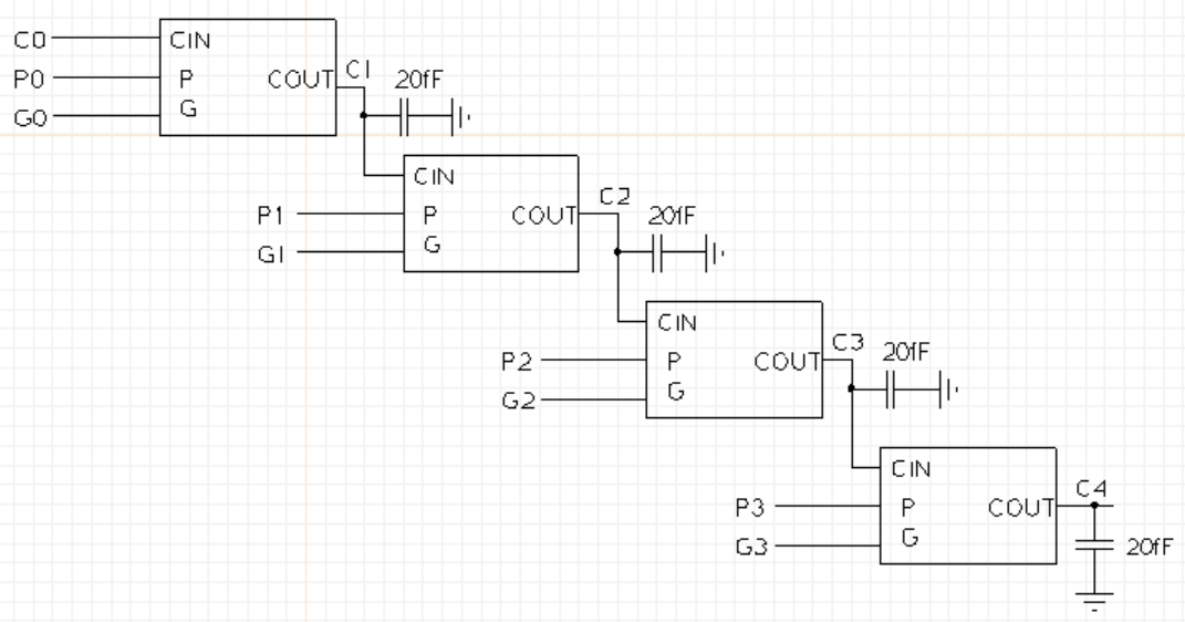
1. **Due date:** All deliverables are due on Friday of the 9th week (May 30, 2025), 11.59PM
2. **Schematics:** All your final cadence schematic files, testbenches, along with short 'readme' text file to help us run and evaluate your schematics. These should be submitted in bruinlearn as **zipped** file.
3. **Report (Template will be provided):**
    - Submit a concise report (Maximum 10 pages) summarizing your work.
    - **Pages 1-2:** should include your architecture, the final value of the VDD you chose, EDP value you obtained (hand calculated and simulated values), the delay from inputs to C4 output, and sizes of all the devices in your logic chain in a table.
    - **Pages 3-5:** Hand-calculation and all the theory and reasoning behind the sizing of the devices and scaling of your VDD**.** This should include the plots that you obtained for 'tinv vs VDD', 'energy vs VDD', 'EDP vs VDD'. Every device sizing should have a proper reasoning behind it. Brute forced sizes will be penalized.
    - **Pages 6-8:** You should attach supporting schematic screenshots, simulation results, waveforms, EDP simulations, or any image attachment that you feel are necessary to support your design choices and show your final results.
    - **Pages 9-10:** Stick diagrams and area estimate. This need not be very accurate. Use different colors to denote different layers.

Grading:

- Majority of your points (70%) will come from just having a functional circuit (Circuit that works and gives correct output).
- Minimizing the Energy-delay product (EDP) will be worth 15%
- Submitting a concise report with design procedure/approach you took and all the schematic, simulation waveforms and screenshots will be worth 10%
- Stick diagrams and area estimate will be worth 5%

Initial architecture idea:

- You can use the architecture shown below with chain of standardized carry generation blocks (with different size scaling for each stage if required) as a starting point. You can come up with whatever structure/type of logic that's used inside these carry blocks. You need not stick to static logic. You can try different types of logic implementation if you're interested.
- You are welcome to try different architectures as well. The below one is just a basic reference to start with and NOT a mandatory one that you need to stick to in your final design.



Project timeline guide:

Week 7: Decide on the top-level and gate level architecture. Size them using logical effort method, hand-calculate the delays for the chain and correlate with simulations in cadence.

Week 8: Obtain the 'tinv vs VDD', 'Energy vs VDD', 'EDP vs VDD' for your chain using hand-calculation. Obtain the optimum VDD and simulate and get the EDP in cadence. **Make sure** you have a complete working circuit by the end of week 8. DO NOT leave this until the end since it will not be possible to do all these in a week.

Week 9: Optimize the EDP using educated resizing.

FAQs

Q: Why is the Wp = 1.5Wn for the reference inverter and not 2Wn like we used in class?

A: Beta is not a fixed constant. It varies with process technology nodes. For the 45nm process kit we are using, beta obtained from simulation = 1.5

Q: Does this mean I should size all the NANDs and NORs or other gates also according to this?

A: Yes, if we are trying to make the pull-up and pull-down resistances equal, we size other gates also with respect to the above reference inverter (Wp = 1.5Wn). For this project, you can always assume that this is the case.

For more EE oriented people: The value of Wp = 1.5Wn might not give you the best critical path delay. So if you're interested in exploring, you can do so and change the sizing ratio as well. You don't need to mandatorily stick to the 1.5 ratio for the project. You can tweak this, but just explain why you chose some other value over this concisely. You will not be penalized for trying out different ratios. But, if you don't have an idea on how to tweak this, you can always stick to the standard 1.5 ratio for the project.

Q: Will the logical effort and parasitic effort of these gates be same as the ones provided in the slides?

A: No, the logical effort and parasitic effort provided in lecture slides assumes that beta = 2. Since the beta = 1.5 for our technology, these will be different.

Q: Should I hand-calculate the energy numbers?

A: Yes, you need to hand-calculate the energy numbers using theory learnt from the class. This will not perfectly match with simulation results, but gives a very good approximation to choose the optimum VDD to minimize EDP.

Q: Do we need to create separate schematic and symbol for all the logic gates?

A: That's your choice. It's not mandatory. As long as the final report shows the sizes of all the devices in all the logic gates clearly, I'm ok with it.

Q: Why is the Cdiff' more than Cgate'. In lecture we learned that Cdiff' = 0.2-0.8x Cgate'?

A: Again this varies with process technology. Cdiff' can be higher than Cgate' depending on technology.

Q: Can we use transmission gate logic for the gates?

A: You can use any type of logic gate for the project. More EE oriented people can even use the ones that are not taught in class: like domino logic if you're interested. You will not be penalized for choosing different architecture or logic gate type than the one taught in class.

Q: Why is my hand-calculation not matching with the simulated numbers? They are off by a lot sometimes.

A: Hand-calculation is just a quick way to get an approximation. We have made a lot of assumptions in the logical effort method delay calculations. For example, we have ignored internal parasitic capacitances, we assumed all gates have step input while in reality they all have finite rise fall times. Because of these reasons, the hand-calculations will not match the simulation numbers and that's fine.