N – 27852

Register No. | 2 | 2 | A | D | L | 1 | 3 | 4 |

BTech Degree Examination May 2024

Fourth Semester

Artificial Intelligence and Machine Learning & Artificial Intelligence and Data Science

22ALT42 – COMPUTER ORGANIZATION

(Regulations 2022)

Time: Three hours | Maximum: 100 marks

Answer all Questions

Part – A (10 × 2 = 20 marks)

1. Name the various functional units of computer. [CO1,K1]
2. List the steps needed to execute the given machine instruction. [CO1,K1]
   LOAD R2, LOC
3. Tell the expression for generate and propagate functions. [CO2,K1]
4. Recode the following number using booth algorithm and bit-pair recording of multipliers. [CO2,K3]
   0 1 0 1 1 1 0 0 1
5. Draw the control signals of instruction address generator. [CO3,K1]
6. Define hazard and list the types of hazards. [CO3,K1]
7. How DMA improves the memory access? [CO4,K2]
8. What is the purpose of tag field in addressing a cache memory? Assume that the processor generates 16 bit address and the cache memory is organized as a 64 blocks of 16 words in every block, identify the number of bits required for the tag field. [CO4,K3]
9. What is meant by memory-mapped I/O? [CO5,K1]
10. Infer the purpose of master ready and slave ready signals. [CO5,K2]

Part – B (5 × 16 = 80 marks)

11. a. Convert the following pairs of decimal numbers to 5-bit 2's complement numbers, then perform addition operation on each pair. Identify whether or not overflow occurs for each case. [CO1,K3] (16)
    1) 4 and 11
    2) 6 and 14
    3) -9 and -14
    4) -4 and 8

(OR)

b. Assume a two address format specified as source and destination. From the given following sequence of instructions identify the addressing modes used and summarize the operations performed in each instruction. [CO1,K3] (16)
   MOVE (R5)+,R0
   ADD (R5) +, R0
   MOVE R0, (R5)
   MOVE 16 (R5), R3
   ADD # 40, R5