ECE-6276 DSP Hardware System Design (Fall 2018)
Project Submission Requirements

As mentioned before, there will be three stages in the Project. Assignments will be created on T-square corresponding to all the three milestones. In each stage, there will be a template for you to fill out the contents. Meanwhile, there will be 4 groups selected to present their works at each stage. (11/12, 11/19, 11/28 on class) 10 minutes for each group + Q&A session.

Preliminary Design Review: Deadline 11/08/2018

Note that although a specific topic is assigned to you, the difficulties and features to be implemented will be varied. Therefore, your grade will also be graded accordingly. You should choose the difficulties based on your confidence and feasibility of the projects. The degree of completion will also be considered while grading. At the end of the project, I hope you can at least deliver a version that runs successfully on the Basys 3. Therefore, it is fine even if you choose an easy level and finish it to the maximum extent possible.

Deliverables:

1) Submit a Presentation (pptx) which should include the following:
    1. Project Title, Team members and Team number
    2. Features to be implemented (not necessary, and advanced features if time permitted)
    3. Specs (frequency, size for image, etc…)
    4. Expected Outcomes (and how to visualize your result)
    5. Preliminary architectures of your design, and functionality of individual clusters (cluster = a group of blocks that realize a specific function). Don't be too detailed on each individual block.
    6. Optimizations for any clusters if applicable
    7. Timeline for the project and work assignments for each team member
    8. Potential risks and plans taken to mitigate them
    9. Reference: description of prior work by others in the area and excerpts from their results (cite the full references)
    10. Any work that has been done and the results
2) Also, put your current codes (higher level verif/TB/design) into a directory and sort the codes properly in different sub-directory. Zip this directory and submit it. It is fine if you have not completed the code yet. As mentioned, the reference design could be in C++, Matlab, Python or any higher level. The test vectors and other relevant details should also be provided in the zip folder.

Only one member of the team should upload the pptx and zip file.

Critical Design Review: Deadline 11/22/2018

Submit a Presentation (pptx) which should include the following:

1. Architectures, and micro-architectures for each cluster (make it like a block diagram), memory design if applicable
2. Results of architectural alternatives – area, throughput
3. Current milestones (status) and risks met
4. Plan for the Final Design Review
5. Identify the percentage of the assigned work that has been completed by each member.

Also, submit a zip file which includes VHDL files and testbenches with the updated higher-level design files. The zip folder should also include test vectors and screenshots showing verifications/simulations.

Only one member of the team should upload the pptx and zip.

Final Design Review: Deadline 11/30/2018

For this stage, you must submit a PDF report which contains:

1. Project Title, Names of the members
2. Introduction of the topic
3. Final features that have been implemented
4. Target specs
5. Final design architecture and micro-architecture for clusters
6. Brief description of the functionalities for each micro-architecture
7. Implementation battles and workarounds or solutions
8. Details about the testbench
9. Functional simulation results, implemented area, power, timing results
10. Work distribution (be detailed!)

You also need to submit a zip file which includes all your codes (Higher Level, TB, Verif, Design) at the final stage. Sort them properly.

Only one member of the team should upload the report and the zip file.