



Search...

Courses

Tutorials

Practice

Jobs

Sign In

DSA Practice Problems C C++ Java Python JavaScript Data Science Machine Learning Courses Linux DevOps

Ace GATE 2027

Computer Organization and Architecture GATE CS PYQs

Single Server Architecture

DBMS Architecture &amp; Schema

Data Warehouse Architecture Quiz

Recovery and File Organization Techniques

File Organization GATE CS PYQ Quiz

Introduction to Computer Software and Hardware

Computer Components and SSDs Quiz

Computer Storage and Applications Quiz

GATE||Computer Network || Routing and Application Layer || Pyq ( 2010 to 2025 )

## Computer Organization and Architecture

Last Updated : Mar 22, 2024



### Question 1

The amount of ROM needed to implement a 4 bit multiplier is

- A 64 bits
- B 128 bits
- C 1 Kbits
- D 2 Kbits

### Question 2

A computer has a 256 KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. The number of bits in the tag field of an address is

- A 11
- B 14
- C 16
- D 27

### Question 3

Register renaming is done in pipelined processors

- A as an alternative to register allocation at compile time
- B for efficient access to function parameters and local variables
- C to handle certain kinds of hazards

**Adobe**

**Save ₹716/mo\* on Creative Cloud All Apps.**

Ends 30 July. First year only.  
Terms apply.

**Learn more****\*Annual, billed monthly**



as part of address translation

## Question 4

Consider the data given in [previous question](#). The size of the cache tag directory is

- A 160 Kbits
- B 136 bits
- C 40 Kbits
- D 32 bits

## Question 5

Which of the following DMA transfer modes and interrupt handling mechanisms will enable the highest I/O band-width?

- A Transparent DMA and Polling interrupts
- B Cycle-stealing and Vectored interrupts
- C Block transfer and Vectored interrupts
- D Block transfer and Polling interrupts

## Question 6

In a k-way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set (s+1). The main memory blocks are numbered 0 onwards. The main memory block numbered j must be mapped to any one of the cache lines from.

- A  $(j \bmod v) * k$  to  $(j \bmod v) * k + (k-1)$
- B  $(j \bmod v)$  to  $(j \bmod v) + (k-1)$
- C  $(j \bmod k)$  to  $(j \bmod k) + (v-1)$
- D  $(j \bmod k) * v$  to  $(j \bmod k) * v + (v-1)$

**Adobe Creative Cloud**

**Your work. Safely backed up.**

**Buy now**

Save to cloud documents

**Adobe**

**Save ₹716/mo\* on  
Creative Cloud  
All Apps.**

Ends 30 July. First year only.  
Terms apply.

**Learn more**\*Annual, billed monthly

Upcoming Courses

**Question 7**

Consider the following sequence of micro-operations.

MBR  $\leftarrow$  PC  
MAR  $\leftarrow$  X  
PC  $\leftarrow$  Y  
Memory  $\leftarrow$  MBR

Which one of the following is a possible operation performed by this sequence?

- A Instruction fetch
- B Operand fetch
- C Conditional branch
- D Initiation of interrupt service

**Question 8**

Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I1, I2, I3, ..., I12 is executed in this pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of

this program, the time (in ns) needed to complete the program is

- A 132
- B 165
- C 176
- D 328

**Question 9**

A RAM chip has a capacity of 1024 words of 8 bits each ( $1K \times 8$ ). The number of  $2 \times 4$  decoders with enable line needed to construct a  $16K \times 16$  RAM from  $1K \times 8$  RAM is

- A 4

**Tech Interview 101 -...**

Starting from - February 28, 2026

\* LIVE Get 90% Refund ...

4.9

**DSA to Development:...**

Starting from - February 28, 2026

\* LIVE Get 90% Refund ...

4.4

**Generative AI Trainin...**

Starting from - February 28, 2026

\* LIVE Get 90% Refund ...

5

[View All →](#)

Fresher Jobs

Experienced Jobs

**Technology Engineering...**

Equifax

Internship - Onsite - Pune (Maharashtra)

Apply by Fri Feb 27 2026

**React Intern**

PGAGI

Upto 0.5 Years • Remote

Apply by Sat Feb 28 2026

**Course Mentor**

GeeksforGeeks

Upto 0.5 Years • Onsite - Noida (Uttar...

Apply by Sat Feb 28 2026

[View All →](#)[View All →](#)

- A 5
- B 6
- C 7

### Question 10

The following code segment is executed on a processor which allows only register operands in its instructions. Each instruction can have atmost two source operands and one destination operand. Assume that all variables are dead after this code segment.

```
c = a + b;  
d = c * a;  
e = c + a;  
x = c * c;  
if (x > a) {  
    y = a * a;  
}  
else {  
    d = d * d;  
    e = e * e;  
}
```

Suppose the instruction set architecture of the processor has only two registers. The only allowed compiler optimization is code motion, which moves statements from one place to another while preserving correctness. What is the minimum number of spills to memory in the compiled code?

- A 0
- B 1
- C 2
- D 3

### Question 11

Consider the same data as [above question](#). What is the minimum number of registers needed in the instruction set architecture of the processor to compile this code segment without any spill to memory? Do not apply any optimization other than optimizing register allocation.

- A 3
- B 4

5 6**Question 12**

Consider a hypothetical processor with an instruction of type LW R1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for operand in memory?

 A Immediate Addressing B Register Addressing C Register Indirect Scaled Addressing D Base Indexed Addressing**Question 13**

On a non-pipelined sequential processor, a program segment, which is a part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

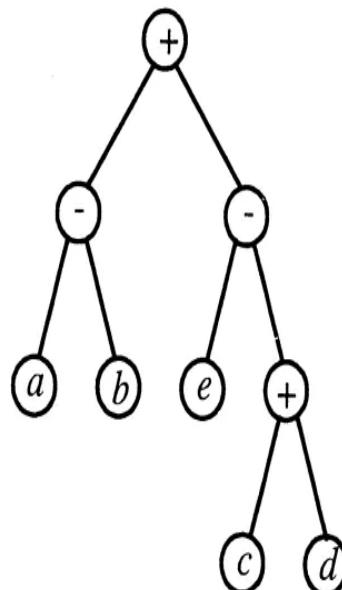
```
Initialize the address
Initialize the count to
LOOP: Load a byte from device
      Store in memory at address
      Increment the address register
      Decrement the count
      If count != 0 go to LOOP
```

Assume that each statement in this program is equivalent to machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute. The designer of the system also has an alternate approach of using DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory. What is the approximate speedup when the DMA controller based design is used in place of the interrupt driven program based input-output?

 A 3.4 B 4.4

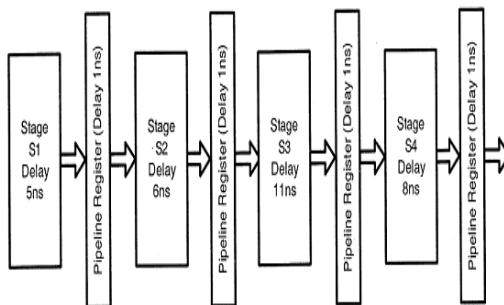
5.1 6.7**Question 14**

Consider evaluating the following expression tree on a machine with load-store architecture in which memory can be accessed only through load and store instructions. The variables a, b, c, d and e are initially stored in memory. The binary operators used in this expression tree can be evaluated by the machine only when the operands are in registers. The instructions produce results only in a register. If no intermediate results can be stored in memory, what is the minimum number of registers needed to evaluate this expression?

 A 2 B 9 C 5 D 3**Question 15**

Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between

only, the pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure:



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

- A 4.0
- B 2.5
- C 1.1
- D 3.0

#### Question 16

An 8KB direct-mapped write-back cache is organized as multiple blocks, each of size 32-bytes. The processor generates 32-bit addresses. The cache controller maintains the tag information for each cache block comprising of the following. 1 Valid bit 1 Modified bit As many bits as the minimum needed to identify the memory block mapped in the cache. What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

- A 4864 bits
- B 6144 bits
- C 6656 bits
- D 5376 bits

#### Question 17

A main memory unit with a capacity of 4 megabytes is built using  $1 \times 1$ -bit DRAM chips. Each DRAM

chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is:-

- A. 100 nanoseconds
- B.  $100 \times 2^{10}$  nanoseconds
- C.  $100 \times 2^{20}$  nanoseconds
- D.  $3200 \times 2^{20}$  nanoseconds

A

B

C

D

### Question 18

A 5-stage pipelined processor has Instruction Fetch(IF), Instruction Decode(ID), Operand Fetch(OF), Perform Operation(PO) and Write Operand(WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	Meaning of
I0 :MUL R2 ,R0 ,R1	$R2 \rightarrow R0$
I1 :DIV R5 ,R3 ,R4	$R5 \rightarrow R3$ ,
I2 :ADD R2 ,R5 ,R2	$R2 \rightarrow R5$ ,
I3 :SUB R5 ,R2 ,R6	$R5 \rightarrow R2$ ,

13

15

17

19

### Question 19

The program below uses six temporary variables a, b, c, d, e, f.

a = 1

b = 10

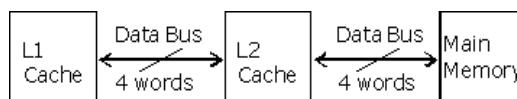
```
c = 20
d = a+b
e = c+d
f = c+e
b = c+e
e = b+f
d = 5+e
return d+f
```

Assuming that all operations take their operands from registers, what is the minimum number of registers needed to execute this program without spilling?

- A 2
- B 3
- C 4
- D 6

#### Question 20

A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively.



When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer?

- A 2 nanoseconds
- B 20 nanoseconds
- C 22 nanoseconds
- D 88 nanoseconds

#### Question 21

Consider the data from [above question](#). When there is a miss in both L1 cache and L2 cache, first a block is transferred from main memory to L2 cache, and then a block is transferred from L2 cache to L1 cache. What is the total time taken for these transfers?

- A 222 nanoseconds
- B 888 nanoseconds
- C 902 nanoseconds
- D 968 nanoseconds

### Question 22

How many 32K x 1 RAM chips are needed to provide a memory capacity of 256K-bytes?

- A 8
- B 32
- C 64
- D 128

### Question 23

Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop? For (i=1 to 2) {I1; I2; I3; I4;}

- A 16
- B 23
- C 28
- D 30

### Question 24

## Question 24

Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks is in the following order: 0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155. Which one of the following memory block will NOT be in cache if LRU replacement policy is used?

- A 3
- B 8
- C 129
- D 216

## Question 25

Where does the swap space reside?

- A RAM
- B Disk
- C ROM
- D On-chip cache

## Question 26

The Boolean function with the Karnaugh map

		AB	00	01	11	10
		CD	00	01	11	10
00	00	0	1	1	0	
	01	0	1	1	1	
11	00	1	1	1	1	
	01	0	1	1	0	

is:

- A  $(A+C).D+B$
- B  $(A+B).C+D$
- C  $(A+D).C+B$
- D  $(A+C).B+D$

## Question 27

Which of the following is/are true of the auto-increment addressing mode?

- I. It is useful in creating self-relocating programs.
- II. If it is included in an Instruction, then an additional ALU is required for the calculation.
- III. The amount of increment depends on the item accessed.

- A I only
- B II only
- C III Only
- D II and III only

#### Question 28

Which of the following must be true for the RFE (Return from Exception) instruction on a general purpose processor?

- I. It must be a trap instruction
- II. It must be a privileged instruction
- III. An exception cannot be allowed to execution of an RFE instruction

- A I only
- B II only
- C I and II only
- D I, II and III only

#### Question 29

For inclusion to hold between two cache levels L1 and L2 in a multi-level cache hierarchy, which of the following are necessary?

- I. L1 must be a write-through cache
- II. L2 must be a write-through cache
- III. The associativity of L2 must be greater than that of L1
- IV. The L2 cache must be at least as large as L1

- A IV only
- B I and IV only

C I, III and IV only D I, II, III and IV

### Question 30

Which of the following are NOT true in a pipelined processor?

- I. Bypassing can handle all RAW hazards.
- II. Register renaming can eliminate all carried WAR hazards.
- III. Control hazard penalties can be eliminated by dynamic branch prediction.

 A I and II only B I and III only C II and III only D I, II and III

### Question 31

The use of multiple register windows with overlap causes a reduction in the number of memory accesses for

- I. Function locals and parameters
- II. Register saves and restores
- III. Instruction fetches

 A I only B II only C III only D I, II and III

### Question 32

In an instruction execution pipeline, the earliest that the data TLB (Translation Lookaside Buffer) can be accessed is

 A before effective address calculation has started

- A during effective address calculation
- B after effective address calculation has completed
- C after data cache lookup has completed

### Question 33

Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
// Initialize array ARR to 0.0
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 Bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR. The total size of the tags in the cache directory is

- A 32 Kbits
- B 34 Kbits
- C 64 Kbits
- D 68 Kbits

### Question 34

The cache hit ratio for this initialization loop is

- A 0%
- B 25%
- C 50%
- D 75%

**Question 35**

Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively:

- A 9,6,5
- B 7,7,6
- C 7,5,8
- D 9,5,6

**Question 36**

Consider a pipelined processor with the following four stages:

IF: Instruction Fetch  
ID: Instruction Decode and Operand Fetch  
EX: Execute  
WB: Write Back

The IF, ID and WB stages take one clock cycle each

to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD R2, R1, R0	R2 $\leftarrow$ R0 + R1
MUL R4, R3, R2	R4 $\leftarrow$ R3 * R2
SUB R6, R5, R4	R6 $\leftarrow$ R5 - R4

- A 7
- B 8
- C 10
- D 14

**Question 37**

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

Instruction	Operation	Instruction size (no.of words)
MOV R1, (3000)	$R1 \leftarrow m[3000]$	2
LOOP: MOV R2, (R3)	$R2 \leftarrow M[R3]$	1
ADD R2, R1	$R2 \leftarrow R1 + R2$	1
MOV (R3), R2	$M[R3] \leftarrow R2$	1
INC R3	$R3 \leftarrow R3 + 1$	1
DEC R1	$R1 \leftarrow R1 - 1$	1
BNZ LOOP	Branch on not zero	2
HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal. Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is:

- A 10
- B 11
- C 20
- D 21

### Question 38

Consider the data given in above question. Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:

- A 100
- B 101
- C 102

110

### Question 39

Consider the data given in above questions. Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction “INC R3”, what return address will be pushed on to the stack?

- A 1005
- B 1020
- C 1024
- D 1040

### Question 40

Consider a machine with a byte addressable main memory of  $2^{16}$  bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A  $50 \times 50$  two-dimensional array of bytes is stored in the main memory starting from memory location 1100H. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

How many data cache misses will occur in total?

- A 40
- B 50
- C 56
- D 59

### Question 41

Consider the data given in above question. Which of the following lines of the data cache will be replaced by new blocks in accessing the array for the second time?

- A line 4 to line 11
- B line 4 to line 12

A line 0 to line 7 B line 0 to line 8**Question 42**

A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

 A 400 B 500 C 600 D 700**Question 43**

A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is

 A 16383 B 16338 C 16388 D 16484**Question 44**

Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instructions incur 2 pipeline stall cycles is

 A 4

- A 8
- B 6
- C 7

**Question 45**

A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is \_\_\_\_\_

- A 5
- B 15
- C 20
- D 25

**Question 46**

In designing a computer's cache system, the cache block (or cache line) size is an important parameter. Which one of the following statements is correct in this context?

- A A smaller block size implies better spatial locality
- B A smaller block size implies a smaller cache tag and hence lower cache tag overhead
- C A smaller block size implies a larger cache tag and hence lower cache hit time
- D A smaller block size incurs a lower cache miss penalty

**Question 47**

If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?

- A Width of tag comparator

- A Width of set index decoder
- B Width of way selection multiplexer
- C Width of processor to main memory data bus

**Question 48**

Consider a main memory system that consists of 8 memory modules attached to the system bus, which is one word wide. When a write request is made, the bus is occupied for 100 nanoseconds (ns) by the data, address, and control signals. During the same 100 ns, and for 500 ns thereafter, the addressed memory module executes one cycle accepting and storing the data. The (internal) operation of different memory modules may overlap in time, but only one request can be on the bus at any time. The maximum number of stores (of one word each) that can be initiated in 1 millisecond is \_\_\_\_\_

- A 1000
- B 10000
- C 100000
- D 100

**Question 49**

Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.

- P1: Four-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.
- P2: Four-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.
- P3: Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6
- P4: Five-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1

Which processor has the highest peak clock frequency?

- A P1
- B P2
- C P3
- D P4

**Question 50**

An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register writeback (WB) with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the ID/RF stage into three stages (ID, RF1, RF2) each of latency 2.2/3 ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds, respectively. The value of P/Q is \_\_\_\_\_.

- A 1.5
- B 1.4
- C 1.8
- D 2.5

**Question 51**

A CPU has a cache with block size 64 bytes. The main memory has  $k$  banks, each bank being  $c$  bytes wide. Consecutive  $c$  – byte chunks are mapped on consecutive banks with wrap-around. All the  $k$  banks can be accessed in parallel, but two accesses

to the same bank must be serialized. A cache block access may involve multiple iterations of parallel bank accesses depending on the amount of data obtained by accessing all the  $k$  banks in parallel. Each iteration requires decoding the bank numbers to be accessed in parallel and this takes.  $k/2$  ns The latency of one bank access is 80 ns. If  $c = 2$  and  $k = 24$ , the latency of retrieving a cache block starting at address zero from main memory is:

- A 92 ns
- B 104 ns

C 172 ns D 184 ns**Question 52**

A CPU has a five-stage pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes  $10^9$  instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, the total execution time of the program is:

 A 1.0 second B 1.2 seconds C 1.4 seconds D 1.6 seconds**Question 53**

Consider two cache organizations: The first one is 32 KB 2-way set associative with 32-byte block size. The second one is of the same size but direct mapped. The size of an address is 32 bits in both cases. A 2-to-1 multiplexer has a latency of 0.6 ns while a kbit comparator has a latency of  $k/10$  ns. The hit latency of the set associative organization is  $h_1$  while that of the direct mapped one is  $h_2$ . The value of  $h_1$  is:

 A 2.4 ns B 2.3 ns C 1.8 ns D 1.7 ns**Question 54**

Consider two cache organizations: The first one is

32 KB 2-way set associative with 32-byte block size. The second one is of the same size but direct mapped. The size of an address is 32 bits in both cases. A 2-to-1 multiplexer has a latency of 0.6 ns while a kbit comparator has a latency of  $k/10$  ns. The hit latency of the set associative organization is  $h_1$  while that of the direct mapped one is  $h_2$ . The value of  $h_1$  is:

- A 2.4 ns
- B 2.3
- C 1.8
- D 1.7

### Question 55

A CPU has a 32 KB direct mapped cache with 128-byte block size. Suppose A is a twodimensional array of size  $512 \times 512$  with elements that occupy 8-bytes each. Consider the following two C code segments, P1 and P2. P1:

```
for (i=0; i<512; i++) {
    for (j=0; j<512; j++) {
        x += A[i][j];
    }
}
```

P2:

```
for (i=0; i<512; i++) {
    for (j=0; j<512; j++) {
        x += A[j][i];
    }
}
```

P1 and P2 are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by P1 be M1 and that for P2 be M2 . The value of M1 is:

- A 0
- B 2048
- C 16384
- D 262144

**Question 56**

A CPU has a 32 KB direct mapped cache with 128-byte block size. Suppose A is a two-dimensional array of size  $512 \times 512$  with elements that occupy 8-bytes each. Consider the following two C code segments, P1 and P2. P1:

```
for (i=0; i<512; i++) {  
    for (j=0; j<512; j++) {  
        x += A[i][j];  
    }  
}
```

P2:

```
for (i=0; i<512; i++) {  
    for (j=0; j<512; j++) {  
        x += A[j][i];  
    }  
}
```

P1 and P2 are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by P1 be M1 and that for P2 be M2 . The value of the ratio M1/M2 is:

- A 0
- B 1/16
- C 1/8
- D 16

**Question 57**

Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line?

- A Neither vectored interrupt nor multiple interrupting devices are possible.
- B Vectored interrupts are not possible but multiple interrupting devices are possible.
- C Vectored interrupts and multiple interrupting devices are both possible.
- D Vectored interrupt is possible but multiple interrupting devices are not possible.

**Question 58**

Consider a three word machine instruction

ADD A[R0], @ B

The first operand (destination) "A [R0]" uses indexed addressing mode with R0 as the index register. The second operand (source) "@ B" uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand). The number of memory cycles needed during the execution cycle of the instruction is

- A 3
- B 4
- C 5
- D 6

**Question 59**

Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side.

- |                  |                    |
|------------------|--------------------|
| 1 A[1] = B[J];   | a Indirect address |
| 2 while [*A++];  | b Indexed, address |
| 3 int temp = *x; | c Autoincrement    |

- A (1, c), (2, b), (3, a)
- B (1, a), (2, c), (3, b)
- C (1, b), (2, c), (3, a)
- D (1, a), (2, b), (3, c)

**Question 60**

Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively

- A 10, 11
- B 10, 22
- C 15, 17
- D 5, 17

### Question 61

A 5 stage pipelined CPU has the following sequence of stages:

IF – Instruction fetch from instruction memory  
 RD – Instruction decode and register read  
 EX – Execute: ALU operation for data and control  
 MA – Data memory access – for write access at RD stage is used,  
 WB – Register write back.

Consider the following sequence of instructions:

I1 : L R0, 1oc1; R0 <= M[1oc1]  
 I2 : A R0, R0; R0 <= R0 + R6  
 I3 : S R2, R0; R2 <= R2 – R6

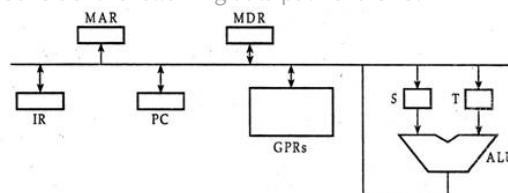
Let each stage take one clock cycle.

What is the number of clock cycles taken to complete the above sequence of instructions starting from the fetch of I1 ?

- A 8
- B 10
- C 12
- D 15

### Question 62

Consider the following data path of a CPU.



The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation - the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR 79. The instruction "call Rn, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the

instruction, its register transfer interpretation is

$R_n \leq PC + 1;$   
 $PC \leq M[PC];$

The minimum number of clock cycles needed for execution cycle of this instruction is.

- A 2
- B 3
- C 4
- D 5

#### Question 63

Consider a machine with byte addressable memory of  $2^{32}$  bytes divided into blocks of size 32 bytes. Assume a 2-set associative cache having 512 cache lines is used with this machine. The size of tag field in bits is \_\_\_\_\_

- A 18
- B 16
- C 19
- D 21

#### Question 64

A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be

- A 120.4 microseconds
- B 160.5 microseconds
- C 165.5 microseconds
- D 590.0 microseconds

**Question 65**

For a pipelined CPU with a single ALU, consider the following situations

1. The  $j + 1$ -st instruction uses the result of the  $j$ -th instruction as an operand
2. The execution of a conditional jump
3. The  $j$ -th and  $j + 1$ -st instructions take the same amount of time

Which of the above can cause a hazard ?

- A 1 and 2 only
- B 2 and 3 only
- C 3 only
- D All of above

**Question 66**

The performance of a pipelined processor suffers if :

- A the pipeline stages have different delays
- B consecutive instructions are dependent on each other
- C the pipeline stages share hardware resources
- D all of the above

**Question 67**

More than one word are put in one cache block to

- A exploit the temporal locality of reference in a program
- B exploit the spatial locality of reference in a program
- C reduce the miss penalty
- D none of the above

**Question 68**

Consider the following data path of a simple non-pipeline CPU. The registers A, B, A1, A2, MDR, the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size  $8 \times (2:1)$  and the DEMUX is of size  $8 \times (1:2)$ . Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and MDR (Memory Date Register). SP can be decremented locally.

The CPU instruction “push r”, where  $r = A$  or  $B$ , has the specification

$M[SP] \leftarrow r$

$SP \leftarrow SP - 1$

How many CPU clock cycles are needed to execute the “push r” instruction?

A 1

B 3

C 4

D 5

#### Question 69

Comparing the time  $T_1$  taken for a single instruction on a pipelined CPU with time  $T_2$  taken on a non pipelined but identical CPU, we can say that

A  $T_1 \leq T_2$

B  $T_1 \geq T_2$

C  $T_1 < T_2$

D  $T_1$  is  $T_2$  plus the time taken for one instruction fetch cycle

#### Question 70

The most appropriate matching for the following pairs

X: Indirect addressing 1 :

Y: Immediate addressing 2 :

Z: Auto decrement addressing 3: (

is

A X-3, Y-2, Z-1

B X-1, Y-3, Z-2

C X-2, Y-3, Z-1

X-3, Y-1, Z-2

### Question 71

For computers based on three-address instruction formats, each address field can be used to specify which of the following:

- S1: A memory operand
- S2: A processor register
- S3: An implied accumulator register

A Either S1 or S2

B Either S2 or S3

C Only S2 and S3

D All of S1, S2 and S3

### Question 72

Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is \_\_\_\_\_.

A 3.2

B 3.0

C 2.2

D 2.0

### Question 73

The least number of temporary variables required to create a three-address code in static single assignment form for the expression  $q + r/3 + s - t * 5 + u * v/w$  is

A 4

B 8

C 7 D 9**Question 74**

Assume that for a certain processor, a read request takes 50 nanoseconds on a cache miss and 5 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a cache hit. The average read access time in nanoseconds is\_\_\_\_\_.

 A 10 B 12 C 13 D 14**Question 75**

Consider a processor with byte-addressable memory. Assume that all registers, including Program Counter (PC) and Program Status Word (PSW), are of size 2 bytes. A stack in the main memory is implemented from memory location (0100)

16 and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is (016E)

16 . The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

- Store the current value of PC in
- Store the value of PSW register :
- Load the starting address of the

The content of PC just before the fetch of a CALL instruction is (5FA0)

16 . After execution of the CALL instruction, the value of the stack pointer is

A.  
(016A)

16

B.  
(016C)

16

C.  
(0170)

16

D.  
(0172)

16

A

B

C

D

### Question 76

Consider the sequence of machine instructions given below:

MUL R5, R0, R1  
DIV R6, R2, R3  
ADD R7, R5, R6  
SUB R8, R7, R4

In the above sequence, R0 to R8 are general purpose registers. In the instructions shown, the first register stores the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) Instruction Fetch and Decode (IF), (2) Operand Fetch (OF), (3) Perform Operation (PO) and (4) Write back the Result (WB). The IF, OF and WB stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD or SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage. The number of clock cycles taken for the execution of the above sequence of instructions is \_\_\_\_\_

11

12

13

14

### Question 77

Consider a machine with a byte addressable main memory of  $2^{20}$  bytes, block size of 16 bytes and a

direct mapped cache having  $2^{12}$  cache lines. Let the addresses of two consecutive bytes in main memory be  $(E201F)_{16}$  and  $(E2020)_{16}$ . What are the tag and cache line address (in hex) for main memory address  $(E201F)_{16}$ ?

- A E, 201
- B F, 201
- C E, E20
- D 2, 01F

### Question 78

Consider the following code sequence having five instructions I1 to I5. Each of these instructions has the following format.

OP Ri, Rj, Rk

where operation OP is performed on contents of registers Rj and Rk and the result is stored in register Ri.

I1 : ADD R1, R2, R3  
 I2 : MUL R7, R1, R3  
 I3 : SUB R4, R1, R5  
 I4 : ADD R3, R2, R4  
 I5 : MUL R7, R8, R9

Consider the following three statements:

- S1: There is an anti-dependence between I1 and I2.
- S2: There is an anti-dependence between I2 and I3.
- S3: Within an instruction pipeline an anti-dependence creates one or more stalls.

Which one of above statements is/are correct?

- A Only S1 is true
- B Only S2 is true
- C Only S1 and S2 are true
- D Only S2 and S3 are true

### Question 79

Consider the following reservation table for a pipeline having three stages S1, S2 and S3.

Time -->

-----  
1 2 3 4 5

S1		X					X	
S2			X		X			
S3				X				

The minimum average latency (MAL) is \_\_\_\_\_

A 3

B 2

C 1

D 4

#### Question 80

What is the minimum size of ROM required to store the complete truth table of an 8-bit x 8-bit multiplier?

A 32 K x 16 bits

B 64 K x 16 bits

C 16 K x 32 bits

D 64 K x 32 bits

#### Question 81

Consider a system with 2 level caches. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns, 10 ns, and 500 ns, respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9, respectively. What is the average access time of the system ignoring the search time within the cache?

A 13.0 ns

B 12.8 ns

C 12.6 ns

D 12.4 ns

#### Question 82

Consider a 4 stage pipeline processor. The

number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1:	1	2	1	2
I2:	2	1	2	1
I3:	1	1	2	1
I4:	2	1	2	1

What is the number of cycles needed to execute the following loop?

```
for (i = 1; i <= 1000; i++)
{I1, I2, I3, I4}
```

A 11 ns

B 12 ns

C 13 ns

D 28 ns

### Question 83

A CPU has only three instructions I1, I2 and I3, which use the following signals in time steps T1-T5:  
I1 : T1 : Ain, Bout, Cin T2 : PCout, Bin T3 : Zout, Ain  
T4 : Bin, Cout T5 : End I2 : T1 : Cin, Bout, Din T2 :  
Aout, Bin T3 : Zout, Ain T4 : Bin, Cout T5 : End I3 : T1  
: Din, Aout T2 : Ain, Bout T3 : Zout, Ain T4 : Dout, Ain  
T5 : End Which of the following logic functions will generate the hardwired control for the signal Ain ?

A  $T1.I1 + T2.I3 + T4.I3 + T3$

B  $(T1 + T2 + T3).I3 + T1.I1$

C  $(T1 + T2).I1 + (T2 + T4).I3 + T3$

D  $(T1 + T2).I2 + (T1 + T3).I1 + T3$

### Question 84

In an enhancement of a design of a CPU, the speed of a floating point unit has been increased by 20% and the speed of a fixed point unit has been increased by 10%. What is the overall speedup achieved if the ratio of the number of floating point operations to the number of fixed point operations is 2:3 and the floating point operation used to take twice the time taken by the fixed point operation in the original design?

- A 1.155
- B 1.185
- C 1.255
- D 1.285

#### Question 85

Using Booth's Algorithm for multiplication, the multiplier -57 will be recoded as

- A 0-100100-1
- B 11000111
- C 0-1001000
- D 0100-1001

#### Question 86

A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec. What percentage of the memory cycle time is used for refreshing?

- A 10
- B 6.4
- C 1
- D .64

#### Question 87

We have two designs D1 and D2 for a synchronous pipeline processor. D1 has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design D2 has 8 pipeline stages each with 2 nsec execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions?

- A 214 nsec
- B 202 nsec

86 nsec

- 200 nsec

### Question 88

A hardwired CPU uses 10 control signals S1 to S10, in various time steps T1 to T5, to implement 4 instructions I1 to I4 as shown below:

	T1	T2	T3	T4	T5
I1	S1, S3, S5	S2, S4, S6	S1, S7	S10	S3, S8
I2	S1, S3, S5	S8, S9, S10	S5, S6, S7	S6	S10
I3	S1, S3, S5	S7, S8, S10	S2, S6, S9	S10	S1, S3
I4	S1, S3, S5	S2, S6, S7	S5, S10	S6, S9	S10

Which of the following pairs of expressions represent the circuit for generating control signals S5 and S10 respectively?

((Ij+Ik)Tn indicates that the control signal should be generated in time step Tn if the instruction being executed is Ij or Ik)

- A  $S5 = T1 + I2 \cdot T3$  and  $S10 = (I1 + I3) \cdot T4 + (I2 + I4) \cdot T5$
- B  $S5 = T1 + (I2 + I4) \cdot T3$  and  $S10 = (I1 + I3) \cdot T4 + (I2 + I4) \cdot T5$
- C  $S5 = T1 + (I2 + I4) \cdot T3$  and  $S10 = (I2 + I3 + I4) \cdot T2 + (I1 + I3) \cdot T4 + (I2 + I4) \cdot T5$
- D  $S5 = T1 + (I2 + I4) \cdot T3$  and  $S10 = (I2 + I3) \cdot T2 + I4 \cdot T3 + (I1 + I3) \cdot T4 + (I2 + I4) \cdot T5$

### Question 89

An instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows:  
 Group 1 : 20 signals, Group 2 : 70 signals,  
 Group 3 : 2 signals, Group 4 : 10 signals,  
 Group 5 : 23 signals.

How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming?

- A 0
- B 103
- C 22
- D 55

### Question 90

In a computer system, four files of size 11050 bytes, 4990 bytes, 5170 bytes and 12640 bytes need to be stored. For storing these files on disk, we can use either 100 byte disk blocks or 200 byte disk blocks (but can't mix block sizes). For each block used to store a file, 4 bytes of bookkeeping information also needs to be stored on the disk. Thus, the total space used to store a file is the sum of the space taken to store the file and the space taken to store the book keeping information for the blocks allocated for storing the file. A disk block can store either bookkeeping information for a file or data from a file, but not both. What is the total space required for storing the files using 100 byte disk blocks and 200 byte disk blocks respectively?

- A 35400 and 35800 bytes
- B 35800 and 35400 bytes
- C 35600 and 35400 bytes
- D 35400 and 35600 bytes

### Question 91

A processor can support a maximum memory of 4 GB, where the memory is word-addressable (a word consists of two bytes). The size of the address bus of the processor is at \_\_\_\_ least bits. Note : This question was asked as Numerical Answer Type.

- A 16
- B 31
- C 32
- D None

**Question 92**

The size of the data count register of a DMA controller is 16 bits. The processor needs to transfer a file of 29,154 kilobytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is \_\_\_\_\_

Note : This question was asked as Numerical Answer Type.

- A 3644
- B 3645
- C 456
- D 1823

**Question 93**

The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput increase of the pipeline is \_\_\_\_\_ percent. [This Question was originally a Fill-in-the-Blanks question]

- A 33 or 34
- B 30 or 31
- C 38 or 39
- D 100

**Question 94**

A processor has 40 distinct instructions and 24 general purpose registers. A 32-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is \_\_\_\_\_ [This Question was originally a Fill-in-the-blanks Question]

- A 16
- B 8
- C 4

32**Question 95**

Suppose the functions F and G can be computed in 5 and 3 nanoseconds by functional units  $U_F$  and  $U_G$ , respectively. Given two instances of  $U_F$  and two instances of  $U_G$ , it is required to implement the computation  $F(G(X_i))$  for  $1 \leq i \leq 10$ . Ignoring all other delays, the minimum time required to complete this computation is \_\_\_\_\_ nanoseconds

[Note that this is originally a Fill-in-the-Blanks Question]

 A 28 B 20 C 18 D 30**Question 96**

Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is \_\_\_\_\_ [Note that this was originally a Fill-in-the-Blanks question]

 A 100 B 200 C 400 D 500**Question 97**

The width of the physical address on a machine is 40 bits. The width of the tag field in a 512 KB 8-way

set associative cache is \_\_\_\_\_ DITS

- A 24
- B 20
- C 30
- D 40

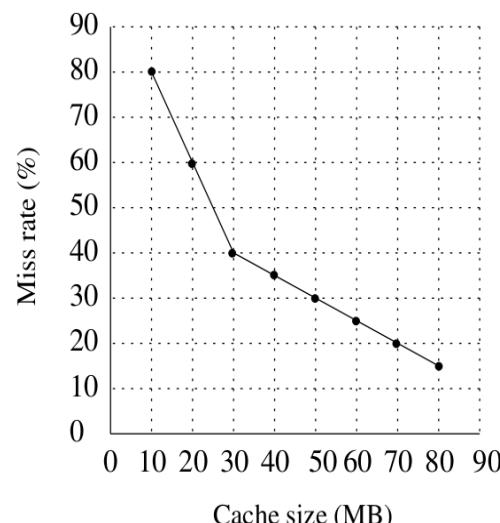
**Question 98**

Consider a 3 GHz (gigahertz) processor with a three-stage pipeline and stage latencies  $v_1$ ,  $v_2$ , and  $v_3$  such that  $v_1 = 3v_2/4 = 2v_3$ . If the longest pipeline stage is split into two pipeline stages of equal latency, the new frequency is \_\_\_\_\_ GHz, ignoring delays in the pipeline registers

- A 2
- B 4
- C 8
- D 16

**Question 99**

A file system uses an in-memory cache to cache disk blocks. The miss rate of the cache is shown in the figure. The latency to read a block from the cache is 1 ms and to read a block from the disk is 10 ms. Assume that the cost of checking whether a block exists in the cache is negligible. Available cache sizes are in multiples of 10 MB.



The smallest cache size required to ensure an average read latency of less than 6 ms is \_\_\_\_\_ MB.

- A 10
- B 20
- C 30
- D 40

### Question 100

When multiplicand Y is multiplied by multiplier X =  $x_{n-1}x_{n-2} \dots x_0$  using bit-pair recoding in Booth's algorithm, partial products are generated according to the following table.

Row	$x_{i+1}$	$x_i$	$x_{i-1}$	Partial Product
1	0	0	0	0
2	0	0	1	Y
3	0	1	0	Y
4	0	1	1	2Y
5	1	0	0	?
6	1	0	1	-Y
7	1	1	0	-Y
8	1	1	1	?

The partial products for rows 5 and 8 are

- A 2Y and Y
- B -2Y and 2Y
- C -2Y and 0
- D 0 and Y

### Question 101

Which of the following statements about relative addressing mode is FALSE?

- A It enables reduced instruction size
- B It allows indexing of array elements with same instruction
- C It enables easy relocation of data
- D It enables faster address calculations than absolute addressing

### Question 102

A cache line is 64 bytes. The main memory has latency 32ns and bandwidth 1G.Bytes/s. The time required to fetch the entire cache line from the main memory is

- A 32 ns
- B 64 ns
- C 96 ns
- D 128 ns

### Question 103

A computer system has a level-1 instruction cache (I-cache), a level-1 data cache (D-cache) and a level-2 cache (L2-cache) with the following specifications:

	Capacity	Mapping Method	Block size
I-cache	4K words	Direct mapping	4 Words
D-cache	4K words	2-way set associative mapping	4 Words
L2-cache	64K words	4-way set associative mapping	16 Words

The length of the physical address of a word in the main memory is 30 bits. The capacity of the tag memory in the I-cache, D-cache and L2-cache is, respectively,

- A 1 K x 18-bit, 1 K x 19-bit, 4 K x 16-bit
- B 1 K x 16-bit, 1 K x 19-bit, 4 K x 18-bit
- C 1 K x 16-bit, 512 x 18-bit, 1 K x 16-bit
- D 1 K x 18-bit, 512 x 18-bit, 1 K x 18-bit

**Question 104**

Which of the following systems is a most likely candidate example of a pipe and filter architecture?

- A Expert system
- B DB repository
- C Aircraft flight controller
- D Signal processing

**Question 105**

A processor takes 12 cycles to complete an instruction I. The corresponding pipelined processor uses 6 stages with the execution times of 3, 2, 5, 4, 6 and 2 cycles respectively. What is the asymptotic speedup assuming that a very large number of instructions are to be executed?

- A 1.83
- B 2
- C 3
- D 6

**Question 106**

A processor that has carry, overflow and sign flag bits as part of its program status word (PSW) performs addition of the following two 2's complement numbers 01001101 and 11101001. After the execution of this addition operation, the status of the carry, overflow and sign flags, respectively will be:

- A 1, 1, 0
- B 1, 0, 0
- C 0, 1, 0
- D 1, 0, 1

**Question 107**

The exponent of 11 in the prime factorization of  $300!$  is

- A 27
- B 28
- C 29
- D 30

#### Question 108

Assume that  $EA = (X) +$  is the effective address equal to the contents of location  $X$ , with  $X$  incremented by one word length after the effective address is calculated;  $EA = -(X)$  is the effective address equal to the contents of location  $X$ , with  $X$  decremented by one word length before the effective address is calculated;  $EA = (X) -$  is the effective address equal to the contents of location  $X$ , with  $X$  decremented by one word length after the effective address is calculated. The format of the instruction is (opcode, source, destination), which means (destination  $\leftarrow$  source op destination). Using  $X$  as a stack pointer, which of the following instructions can pop the top two elements from the stack, perform the addition operation and push the result back to the stack.

- A  $ADD (X) -, (X)$
- B  $ADD (X), (X) -$
- C  $ADD -(X), (X) +$
- D  $ADD -(X), (X) +$

#### Question 109

Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal microprogrammed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

- A 125, 7
- B 125, 10
- C 135, 7

135, 10

### Question 110

A non pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 nsec, 1.5 nsec, 2 nsec, 1.5 nsec and 2.5 nsec, respectively. The delay of the latches is 0.5 nsec. The speedup of the pipeline processor for a large number of instructions is

- A 4.5
- B 4.0
- C 3.33
- D 3.0

### Question 111

Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB. The number of bits in the TAG, SET and WORD fields, respectively are:

- A 7, 6, 7
- B 8, 5, 7
- C 8, 6, 6
- D 9, 4, 7

### Question 112

Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB. While accessing the memory location 0C795H by the CPU, the contents of the TAG field of the corresponding cache line is

- A 000011000
- B 110001111

C 00011000 D 110010101**Question 113**

Which of the following is an interrupt according to temporal relationship with system clock ?

 A Maskable interrupt B Periodic interrupt C Division by zero D Synchronous interrupt**Question 114**

The main memory of a computer has  $2^m$  blocks while the cache has  $2^c$  blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then the block  $k$  of main memory maps to the set:

 A  $(k \bmod m)$  of the cache B  $(k \bmod c)$  of the cache C  $(k \bmod 2^c)$  of the cache D  $(k \bmod 2^{cm})$  of the cache**Question 115**

Arrange the following configurations for CPU in decreasing order of operating speeds; Hardwired Control, vertical microprogramming, horizontal microprogramming

 A Hardwired control, Vertical microprogramming, Horizontal microprogramming. B Hardwired control, Horizontal microprogramming, Vertical microprogramming.

- C Horizontal microprogramming, Vertical microprogramming, Hardwired control.
- D Vertical microprogramming, Horizontal microprogramming, Hardwired control.

**Question 116**

The main difference(s) between a CISC and a RISC processor is/are that a USC processor typically: a) has fewer instructions b) has fewer addressing modes c) has more registers d) is easier to implement using hardwired control logic

- A a and b
- B b and c
- C a and d
- D a, b, c and d

**Question 117**

A certain processor supports only the immediate and the direct addressing modes. Which of the following programming language features cannot be implemented on this processor? a) Pointers b) Arrays c) Records d) Recursive procedures with local variables

- A Only a
- B a and b
- C c and d
- D a, b, c and d

**Question 118**

Which of the following addressing modes permits relocation without any change whatsoever in the code?

- A Indirect addressing

- B Indexed addressing
- C Base register addressing
- D PC relative addressing

**Question 119**

Which of the following is true?

- A Unless enabled, a CPU will not be able to process interrupts.
- B Loop instructions cannot be interrupted till they complete.
- C A processor checks for interrupts before executing a new instruction.
- D Only level triggered interrupts are possible in microprocessors.

**Question 120**

The address space of 8086 CPU is

- A One Megabyte
- B 256 Kilobytes
- C 1 K Megabytes
- D 64 Kilobytes

**Question 121**

If an instruction takes  $i$  microseconds and a page fault takes an additional  $j$  microseconds, the effective instruction time if on the average a page fault occurs every  $k$  instructions is:

- A  $i + j/k$
- B  $i + j * k$
- C  $(i + j)/k$

D $(i + j) * k$ **Question 122**

[5 Marks question] For a set-associative Cache Organization, the parameters are as follows:

$t_c$  – Cache access time  
 $t_m$  – Main memory access time  
 $l$  – number of sets  
 $b$  – block size  
 $k \times b$  – set size

Calculate the hit ratio for a loop executed 100 times where the size of the loop is  $n \times b$  and  $n = k \times m$  is a non-zero integer and  $1 < m \leq l$ . Given the value of the hit ratio for  $l = 1$ .

**Question 123**

RST 7.5 interrupt in 8085 microprocessor executes the interrupt service routine from interrupt vector location

 A

0000H

 B

0075H

 C

003CH

 D

0034H

**Question 124**

The correct matching for the following pairs is

- |                             |         |
|-----------------------------|---------|
| (A) DMA I/O                 | (1) Hiç |
| (B) Cache                   | (2) Dis |
| (C) Interrupt I/O           | (3) Pri |
| (D) Condition Code Register | (4) ALL |

Codes:

	A	B	C	D
a	4	3	1	2
b	2	1	3	4
c	4	3	2	1
d	2	3	4	1

- A a
- B b
- C c
- D d

**Question 125**

Contents of A register after the execution of the following 8085 microprocessor program is

```
MVI A, 55 H
MVI C, 25 H
ADD C
DAA
```

- A 7AH
- B 80H
- C 50H
- D 22H

**Question 126**

A micro instruction into be designed to specify *a*. none or one of the three micro operations of one kind and *b*. none or upto six micro operations of another kind The minimum number of bits in the micro-instruction is

- A 9
- B 5
- C 8
- D None of the above

**Question 127**

Relative mode of addressing is most relevant to writing

- A co-routines

- B position-independent code
- C shareable code
- D interrupt handlers

**Question 128**

Number of machine cycles required for RET instruction in 8085 microprocessor is

- A 1
- B 2
- C 3
- D 5

**Question 129**

For the daisy chain scheme of connecting I/O devices, which of the following statement is true?

- A It gives non-uniform priority to various devices
- B It gives uniform priority to all devices
- C It is only useful for connecting slow devices to a processor
- D It requires a separate interrupt pin on the processor for each device

**Question 130**

A micro program control unit is required to generate a total of 25 control signals. Assume that during any microinstruction , at most two control signals are active. Minimum number of bits required in the control word to generate the required control signals will be

- A 2
- B

A 2.5 B 10 C 12**Question 131**

An 8052 based system has an output port with address 00H. Consider the following assembly language program.

```
ORG 0100H
MVI A, 00H
LXI H, 0105H
OUT 00H
INR A
PCHL
HLT
```

- a) What does the program do with respect to the output port?
- b) Show the wave forms at the three levels.

**Question 132**

A hard disk is connected to a 50 MHz processor through a DMA controller. Assume that the initial set-up of a DMA transfer takes 1000 clock cycles for the processor, and assume that the handling of the interrupt at DMA completion requires 500 clock cycles for the processor. The hard disk has a transfer rate of 2000 Kbytes/sec and average block transferred is 4 K bytes. What fraction of the processor time is consumed by the disk, if the disk is actively transferring 100% of the time?

Level 1 (Cache memory)

Level 1 (Cache memory)

Access time = 50 nsec/byte      Access time = 200 nsec/byte

Size	Hit ratio	Size	Hit ratio
8 Kbytes	0.80	4 Kbytes	0.98
16 Kbytes	0.90	16 Kbytes	0.99
64 Kbytes	0.95	64 Kbytes	0.995

Size	Hit ratio
250 M bytes	1.0

 A 1.5% B 1% C 2.5% D 10%

**Question 133**

A computer system has a three level memory hierarchy, with access time and hit ratios as shown below:

Level 1 (Cache memory)		Level 2 (main memory)		Level 3	
Access time = 50 nsec/byte	Access time = 200 nsec/byte	Access time = 5 $\mu$ sec/byte			
Size	Hit ratio	Size	Hit ratio	Size	Hit ratio
8 M byte	0.80	4M byte	0.98	260 Mbyte	1.0
16 M byte	0.90	16 M byte	0.99		

- a) What should be the minimum sizes of level 1 and 2 memories to achieve an average access time of less than 100 nsec? b) What is the average access time achieved using the chosen sizes of level 1 and level 2 memories?

**Question 134**

Consider the following assembly codes : (P1) :

```
BYTE_VALUE  DB  150      // A byte value
WORD_VALUE  DW  300      // A word value
ADD  BYTE_VALUE, 65      // An immediate
MOV  AX, 45H              // Immediate co
```

(P2) :

```
MY_TABLE TIMES 10 DW 0  // Allocates 1
MOV EBX, [MY_TABLE]      // Effective A
MOV [EBX], 110           // MY_TABLE[0]
ADD EBX, 2                // EBX = EBX + 2
MOV [EBX], 123           // MY_TABLE[1]
```

Which of the following option is correct?

- A P1 uses immediate Addressing, and P2 uses Indirect Memory Addressing mode.
- B P1 uses immediate Addressing, and P2 uses Direct Memory Addressing mode.
- C P1 uses Direct Memory Addressing, and P2 uses Direct Memory Addressing mode.
- D None of these

**Question 135**

Consider the following collection of relation schemes:

professor(profname, deptname)  
 department(deptname, building)  
 committee(profname, commname)

Find all the professors who are in exactly (i.e., no more and no less) all those committees that Professor Smith is in.

- A  $R2 \leftarrow \Pi_{commname}(\sigma_{profname} = Smith(committee))$   
 $R3 \leftarrow \Pi_{commname}(committee) - R2$   
 $(committee / R2) - \Pi_{profname}(committee \bowtie R3)$
- B  $R2 \leftarrow \Pi_{commname}(\Pi_{commname}(committee))$   
 $R3 \leftarrow \sigma_{profname} = Smith(committee) - R2$   
 $(committee / R2) - \Pi_{profname}(committee \bowtie R3)$
- C  $R2 \leftarrow \Pi_{commname}(\Pi_{profname}(committee))$   
 $R3 \leftarrow \Pi_{commname}(committee) - R2$   
 $(committee / R2) - \sigma_{profname} = Smith(committee \bowtie R3)$
- D None of the above

### Question 136

Consider the following instruction sequence in a RISC machine :

Instr. No.	Instruction	Instruction size
i:	Add R1, R2, R4	4
i+1:	Sub R4, R5, R6	3
i+2:	<del>Cmp R0, R8, R9</del>	5
i+3:	<del>Mul R1, R9, R10</del>	1
i+4:	Beg R0, offset	3

Conditional and unconditional branch instructions use PC-relative addressing mode with Offset specified in bytes to the target location of the branch instruction. Further the Offset is always with respect to the address of the next instruction in the program sequence. If the target of the branch instruction is i, then the decimal value of the Offset is \_\_\_\_\_.

- A -16
- B 18
- C 1000
- D None of the above

**Question 137**

Consider an array  $A[999]$  & each element occupies 4 word. A 32 word cache is used and divided into 16 word blocks. What is the miss ratio for the following statement. Assume one block is read into cache in case of miss:

```
for(i=0; i < 1000; i++)
    A[i] = A[i] + 99
```

- A 0.50
- B 0.75
- C 0.875
- D 0.125

**Question 138**

A cache memory unit with capacity of  $N$  words and block size of  $B$  words is to be designed. If it is designed as a 16-way set-associative cache, the length of the TAG field is 10 bits. If the cache unit is now designed as direct mapped cache, the length of the TAG field is \_\_\_\_\_ bits.

- A 6
- B 14
- C 16
- D None of these

**Question 139**

Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI, WO are 1, 2, 3, 4, 5 respectively. The total time taken for the execution of an instruction is \_\_\_\_\_.

DI, FU, EI and WU are 5 ns, 17 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 100 instructions I1, I2, I3, ..., I100 is executed in this pipelined processor. Instruction I17 is the only branch instruction and its branch target is I91. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is \_\_\_\_\_.

- A 612
- B 1854
- C 1133
- D 578

#### Question 140

The read access times and the hit ratios for different caches in a memory hierarchy are as given below:

Cache	Read access time (in nanoseconds)	Hit Ratio
I-cache	2	0.8
D-cache	2	0.9
L2-cache	8	0.9

The read access time of main memory is 90 nanoseconds. Assume that the caches use the referred-word-first read policy and the writeback policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In execution of a program, 60% of memory reads are for instruction fetch and 40% are for memory operand fetch. What is total value of average data fetch time multiplied by average instruction fetch time?

- A 4.72
- B 16.89
- C 9.1
- D 19.98

#### Question 141

Consider a 4-way set associative cache (initially empty) with total 16 cache blocks.

The main memory consists of 256 blocks and

The main memory consists of 256 blocks and the request for memory blocks is in the following order: 0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155. Find the total number of hit(s) occurred in the cache using least recently used (LRU) page replacement algorithm?

- A 0
- B 1
- C 2
- D 3

#### Question 142

A 32 - bit wide main memory unit with a capacity of 1 GB is built using 256M X 4-bit DRAM chips. The number of rows of memory cells in the DRAM chip is  $2^{14}$ . The time taken to perform one refresh operation is 50 nanoseconds. The refresh period is 2 milliseconds. The percentage (rounded to the closest integer) of the time available for performing the memory read/write operations in the main memory unit is \_\_\_\_\_.

**Note** - This was Numerical Type question.

- A 59
- B 40
- C 99
- D None of these

#### Question 143

Consider the following processor design characteristics. I. Register-to-register arithmetic operations only II. Fixed-length instruction format III. Hardwired control unit Which of the characteristics above are used in the design of a RISC processor?

- A I and II only
- B II and III only
- C I and III only

I, II and III**Question 144**

A processor has 16 integer registers (R0, R1, ..., R15) and 64 floating point registers (F0, F1, ..., F63). It uses a 2-byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type 4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (1F).

The maximum value of N is \_\_\_\_\_ .

**Note** -This was Numerical Type question.

- A 32
- B 64
- C 256
- D 512

**Question 145**

The size of the physical address space of a processor is  $2^P$  bytes. The word length is  $2^W$  bytes. The capacity of cache memory is  $2^N$  bytes. The size of each cache block is  $2^M$  words. For a K-way set-associative cache memory, the length (in number of bits) of the tag field is

- A  $P - N - \log_2 K$
- B  $P - N + \log_2 K$
- C  $P - N - M - W - \log_2 K$
- D  $P - N - M - W + \log_2 K$

**Question 146**

The instruction pipeline of a RISC processor has the

following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards.

The number of clock cycles required for completion of execution of the sequence of instruction is \_\_\_\_\_.

**Note** - This was Numerical Type question.

- A 219
- B 104
- C 115
- D 220

#### Question 147

Consider the following program fragment in assembly language :

```
mov ax, 0h
mov cx, 0A h

doloop :
dec ax
loop doloop
```

What is the value of ax and cx registers after the completion of the doloop ?

- A ax=FFF5 h and cx=0 h
- B ax=FFF6 h and cx=0 h
- C ax=FFF7 h and cx=0A h
- D ax=FFF5 h and cx=0A h

#### Question 148

Consider the following assembly program fragment :

```
stc
mov al, 11010110b
```

```
mov cl, 2
rcl al, 3
rol al, 4
shr al, cl
mul cl
```

The contents of the destination register ax (in hexadecimal) and the status of Carry Flag (CF) after the execution of above instructions, are:

- A ax=003CH; CF=0
- B ax=001EH; CF=0
- C ax=007BH; CF=1
- D ax=00B7H; CF=1

#### Question 149

In Distributed system, the capacity of a system to adapt the increased service load is called \_\_\_\_\_ .

- A Tolerance
- B Scalability
- C Capability
- D Loading

#### Question 150

Which of the following Super Computers is the fastest Super Computer ?

- A Sun-way TaihuLight
- B Titan
- C Piz Daint
- D Sequoia

#### Question 151

Which speed up could be achieved according to Amdahl's Law for infinite number of processes if 5% of a program is sequential and the remaining part is ideally parallel ?

- A Infinite
- B 5
- C 20
- D 50

#### Question 152

A two way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The physical address space is 4 GB. The number of bits in the TAG, SET fields are

- A 20, 7
- B 19, 8
- C 20, 8
- D 21, 9

#### Question 153

A CPU has a 32 KB direct mapped cache with 128 byte block size. Suppose A is a 2 dimensional array of size  $512 \times 512$  with elements that occupy 8 bytes each. Consider the code segment

```
for (i =0; i < 512; i++) {  
    for (j =0; j < 512; j++) {  
        x += A[i][j];  
    }  
}
```

Assuming that array is stored in order  $A[0][0], A[0][1], A[0][2], \dots$ , the number of cache misses is

- A 16384
- B 512
- C 2048
- D 1024

**Question 154**

For a pipelines CPU with a single ALU, consider the following: A. The  $j + 1$ st instruction uses the result of  $j$ th instruction as an operand B. Conditional jump instruction C.  $j$ th and  $j + 1$ st instructions require ALU at the same time Which one of the above causes a hazard?

- A and B only
- B and C only
- B only
- A, B and C

**Question 155**

Consider an instruction of the type LW R1, 20(R2) which during execution reads a 32 bit word from memory and stores it in a 32 bit register R1. The effective address of the memory location is obtained by adding a constant 20 and contents of R2. Which of the following best reflects the addressing mode implemented by this instruction for operand in memory?

- A Immediate addressing
- B Register addressing
- C Register Indirect addressing
- D Indexed addressing

**Question 156**

Which of the following addressing mode is best suited to access elements of an array of contiguous memory locations ?

- A Indexed addressing mode
- B Base Register addressing mode
- C Relative address mode
- D Displacement mode

**Question 157**

Which of the following is correct statement ?

- A In memory - mapped I/O, the CPU can manipulate I/O data residing in interface registers that are not used to manipulate memory words.
- B The isolated I/O method isolates memory and I/O addresses so that memory address range is not affected by interface address assignment.
- C In asynchronous serial transfer of data the two units share a common clock.
- D In synchronous serial transmission of data the two units have different clocks.

**Question 158**

A micro-instruction format has micro-ops field which is divided into three subfields F1, F2, F3 each having seven distinct micro-operations, condition field CD for four status bits, branch field BR having four options used in conjunction with address field ADF. The address space is of 128 memory locations. The size of micro-instruction is:

- A 17
- B 20
- C 24
- D 32

**Question 159**

Which of the following is not a component of Memory tube display ?

- A Flooding gun
- B Collector
- C

A Ground B Liquid Crystal**Question 160**

Which of the following is not true in case of Oblique Projections?

- A Parallel projection rays are not perpendicular to the viewing plane.
- B Parallel lines in space appear parallel on the final projected image.
- C Used exclusively for pictorial purposes rather than formal working drawings.
- D Projectors are always perpendicular to the plane of projection.

**Question 161**

How many  $128 \times 8$  bit RAMs are required to design  $32\text{ K} \times 32$  bit RAM?

 A 512 B 1024 C 128 D 32**Question 162**

The most appropriate matching for the following pairs :

- |                               |       |
|-------------------------------|-------|
| X : Indirect Addressing       | 1. Lc |
| Y : Immediate Addressing      | 2. Po |
| Z : Auto Decrement Addressing | 3. Co |

 A X - 3, Y - 2, Z - 1 B X - 2, Y - 3, Z - 1 C X - 3, Y - 1, Z - 2



X - 2, Y - 1, Z - 3

**Question 163**

Which interrupt in 8085 Microprocessor is unmaskable?



RST 5.5



RST 7.5



TRAP



Both (a) and (b)

**Question 164**

A cache memory needs an access time of 30 ns and main memory 150 ns, what is the average access time of CPU (assume hit ratio = 80%)?



60



30



150



70

**Question 165**

Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speedup achieved in this pipelined processor is



3.2



3.0



2.2



2.0

**Question 166**

Relative mode of addressing is most relevant to writing

- A Co-routines
- B Position – independent code
- C Shareable code
- D Interrupt Handlers

**Question 167**

Match the following:

<b>Addressing Mode</b>		<b>Location of operand</b>
a. Implied	i.	Registers which are in CPU
b. Immediate	ii.	Register specifies the address of the operand.
c. Register	iii.	Specified in the register
d. Register Indirect	iv.	Specified implicitly in the definition of instruction

**Codes :**

- |     |    |     |     |
|-----|----|-----|-----|
| a   | b  | c   | d   |
| (1) | iv | iii | i   |
| (2) | iv | i   | iii |
| (3) | iv | ii  | i   |
| (4) | iv | iii | ii  |

- A (1)
- B (2)
- C (3)
- D (4)

**Question 168**

How many 32K X 1 RAM chips are needed to provide a memory capacity of 256K-bytes?

- A 8
- B 32
- C 64
- D 128

**Question 169**

The contents of the flag register after execution of the following program by 8085 microprocessor will be

Program  
SUB A  
MVI B,(01)<sub>H</sub>  
DCR B  
HLT

- A (54)<sub>H</sub>
- B (00)<sub>H</sub>
- C (01)<sub>H</sub>
- D (45)<sub>H</sub>

#### Question 170

The minimum time delay between the initiation of two independent memory operations is called

- A Access time
- B Cycle time
- C Rotational time
- D Latency time

#### Question 171

In  $X = (M + N \times O) / (P \times Q)$ , how many one-address instructions are required to evaluate it?

- A 4
- B 6
- C 8
- D 10

#### Question 172

Consider a 33 MHz CPU based system. What is the number of wait states required if it is interfaced with a 60 ns memory? Assume a maximum of 10 ns

with a 20 ns memory, assuming a maximum of 10 ns delay for additional circuitry like buffering and decoding.

- A 0
- B 1
- C 2
- D 3

#### Question 173

The number of logical CPUs in a computer having two physical quad-core chips with hyper threading enabled is

- A 1
- B 2
- C 8
- D 16

#### Question 174

If each address space represents one byte of storage space, how many address lines are needed to access RAM chips arranged in a  $4 \times 6$  array, where each chip is  $8K \times 4$  bits ?

- A 13
- B 15
- C 16
- D 17

#### Question 175

Suppose you want to build a memory with 4 byte words with a capacity of  $2^{21}$  bits. What is type of decoder required if the memory is built using  $2K \times 8$  RAM chips?

- A 5 to 32

- A - - -
- B 6 to 64
- C 4 to 64
- D 7 to 128

**Question 176**

The register that stores the bits required to mask the interrupts is \_\_\_\_\_.

- A Status register
- B Interrupt service register
- C Interrupt mask register
- D Interrupt request register

**Question 177**

In \_\_\_\_\_ addressing mode, the operands are stored in the memory. The address of the corresponding memory location is given in a register which is specified in the instruction.

- A Register direct
- B Register indirect
- C Base indexed
- D Displacement

**Question 178**

A processor is fetching instructions at the rate of 1 MIPS. A DMA module is used to transfer characters to RAM from a device transmitting at 9600 bps. How much time will the processor be slowed down due to DMA activity?

- A 9.6 ms
- B 4.8 ms
- C 2.4 ms

A 2.4 ms

B 1.2 ms

### Question 179

A pipeline P operating at 400 MHz has a speedup factor of 6 and operating at 70% efficiency. How many stages are there in the pipeline?

A 5

B 6

C 8

D 9

### Question 180

How much speed do we gain by using the cache, when cache is used 80% of the time? Assume cache is faster than main memory

A 5.27

B 2.00

C 4.16

D 6.09

### Question 181

Two eight bit bytes 1100 0011 and 0100 1100 are added. What are the values of the overflow, carry and zero flags respectively, if the arithmetic unit of the CPU uses 2's complement form? ISRO 2013

A 0, 1, 1

B 1, 1, 0

C 1, 0, 1

D 0, 1, 0

**Question 182**

The \_\_\_\_\_ addressing mode is similar to register indirect addressing mode, except that an offset is added to the contents of the register. The offset and register are specified in the instruction.

- A Base indexed
- B Base indexed plus displacement
- C Indexed
- D Displacement

**Question 183**

In \_\_\_\_\_ method, the word is written to the block in both the cache and main memory, in parallel.

- A Write through
- B Write back
- C Write protected
- D Direct mapping

**Question 184**

A particular parallel program computation requires 100 seconds when executed on a single CPU. If 20% of this computation is strictly sequential, then theoretically the best possible elapsed times for this program running on 2 CPUs and 4 CPUs respectively are

- A 55 and 45 seconds
- B 80 and 20 seconds
- C 75 and 25 seconds
- D 60 and 40 seconds

**Question 185**

A DMA controller transfers 32-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 4800 characters per second. The CPU is fetching and executing instructions at an average rate of one million instructions per second. By how much will the CPU be slowed down because of the DMA transfer?

- A 0.6%
- B 0.12%
- C 1.2%
- D 2.5%

**Question 186**

A CPU handles interrupt by executing interrupt service subroutine \_\_\_\_\_.

- A by checking interrupt register after execution of each instruction
- B by checking interrupt register at the end of the fetch cycle
- C whenever an interrupt is registered
- D by checking interrupt register at regular time interval

**Question 187**

Consider a direct mapped cache with 64 blocks and a block size of 16 bytes. To what block number does the byte address 1206 map to

- A does not map
- B 6
- C 11
- D 54

**Question 188**

In the case of parallelization, Amdahl's law states that if  $P$  is the proportion of a program that can be made parallel and  $(1 - P)$  is the proportion that cannot be parallelized, then the maximum speed-up that can be achieved by using  $N$  processors is:

- A  $\frac{1}{P} + (1 - P)N$
- B  $\frac{1}{N - 1}P + P$
- C  $\frac{1}{P} + \frac{1}{N}$
- D  $\frac{1}{P} + \frac{1}{1 - P}N$

**Question 189**

MOV [BX], AL type of data addressing is called ?

- A register
- B immediate
- C register indirect
- D register relative

**Question 190**

What is the raw throughput of USB 2.0 technology?

- A 480 Mbps
- B 400 Mbps
- C 200 Mbps
- D 12 Mbps

**Question 191**

A processor takes 12 cycles to complete an instruction I. The corresponding pipelined

processor uses 6 stages with the execution times of 3, 2, 5, 4, 6 and 2 cycles respectively. What is the asymptotic speedup assuming that a very large number of instructions are to be executed?

- A 1.83
- B 2
- C 3
- D 6

#### Question 192

If a microcomputer operates at 5 MHz with an 8-bit bus and a newer version operates at 20 MHz with a 32-bit bus, the maximum speed-up possible approximately will be

- A 2
- B 4
- C 8
- D 16

#### Question 193

The search concept used in associative memory is

- A Parallel search
- B Sequential search
- C Binary search
- D Selection search

#### Question 194

Number of chips (128 x 8 RAM) needed to provide a memory capacity of 2048 bytes

- A 2
- B 4
- C 8

8

16

**Question 195**

In DMA transfer scheme, the transfer scheme other than burst mode is

- A cycle technique
- B stealing technique
- C cycle stealing technique
- D cycle bypass technique

**Question 196**

Which of the following statements about synchronous and asynchronous I/O is NOT true?

- A An ISR is invoked on completion of I/O in synchronous I/O but not in asynchronous I/O
- B In both synchronous and asynchronous I/O, an ISR (Interrupt Service Routine) is invoked after completion of the I/O
- C A process making a synchronous I/O call waits until I/O is complete, but a process making an asynchronous I/O call does not wait for completion of the I/O
- D In the case of synchronous I/O, the process waiting for the completion of I/O is woken up by the ISR that is invoked after the completion of I/O

**Question 197**

In which addressing mode, the effective address of the operand is generated by adding a constant value to the content of a register?

- A Absolute mode
- B Indirect mode
- C Immediate mode



Index mode

**Question 198**

The process of organizing the memory into two banks to allow 8 and 16-bit data operation is called

- A Bank switching
- B Indexed mapping
- C Two-way memory interleaving
- D Memory segmentation

**Question 199**

The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields. a micro operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX. How many bits are there in the X and Y fields, and what is the size of the control memory in number of words

- A 10, 3, 1024
- B 8, 5, 256
- C 5, 8, 2048
- D 10, 3, 512

**Question 200**

A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

- A 400
- B 500
- C 600
- D 700

**Question 201**

Consider a pipelined processor with the following four stages:

IF: Instruction Fetch  
ID: Instruction Decode and Operand Fetch  
EX: Execute  
WB: Write Back

The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD	R2, R1, R0	R2 $\leftarrow$ R1 +
MUL	R4, R3, R2	R4 $\leftarrow$ R3 *
SUB	R6, R5, R4	R6 $\leftarrow$ R5 -

- A 7
- B 8
- C 10
- D 14

**Question 202**

The two numbers given below are multiplied using the Booth's algorithm  
Multiplicand: 0101 1010 1110  
1110 Multiplier: 0111 0111 1011 1101 How many additions/subtractions are required for the multiplication of the above two numbers?

- A 6
- B 8
- C 10
- D 12

**Question 203**

Which of the following statements about relative addressing mode is FALSE?

- A It enables reduced instruction size
- B It allows indexing of array element with same instruction
- C It enables easy relocation of data
- D It enables faster address calculation than absolute addressing

**Question 204**

On receiving an interrupt from an I/O device, the CPU

- A Halts for a predetermined time
- B Branches off to the interrupt service routine after completion of the current instruction
- C Branches off to the interrupt service routine immediately
- D Hands over control of address bus and data bus to the interrupting device

**Question 205**

Which of the following is/are true of the auto-increment addressing mode? I. It is useful in creating self-relocating code II. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation III. The amount of increment depends on the size of the data item accessed

- A I only
- B II only
- C III only
- D II and III only

**Question 206**

The performance of a pipelined processor suffers if

- A the pipeline stages have different delays
- B consecutive instructions are dependent on

- each other
- the pipeline stages share hardware resources
- All of the above

### Question 207

An interrupt in which the external device supplies its address as well as the interrupt requests is known as

- vectored interrupt
- maskable interrupt
- non-maskable interrupt
- designated interrupt

### Question 208

Consider the following Assembly language program

```
MVIA    30 H
ACI     30 H
XRA     A
POP     H
```

After the execution of the above program, the contents of the accumulator will be

- 30 H
- 60 H
- 00 H
- contents of stack

### Question 209

Which of the following architecture is/are not suitable for realising SIMD?

- Vector processor
- Array processor
- Von Neumann



All of the above

**Question 210**

The device which is used to connect a peripheral to bus is known as



control register



interface



communication protocol



none of these

**Question 211**

The Memory Address Register



is a hardware memory device which denotes the location of the current instruction being executed.



is a group of electrical circuit, that performs the intent of instructions fetched from memory



contains the address of the memory location that is to be read from or stored into



contains a copy of the designated memory location specified by the MAR after a "read" or the new contents of the memory prior to a "write"

**Question 212**

More than one word are put in one cache block to



exploit the temporal locality of reference in a program



exploit the spatial locality of reference in a program



reduce the miss penalty



none of these

**Question 213**

The CPU of a system having 1 MIPS execution rate needs 4 machine cycles on an average for executing an instruction. The fifty percent of the cycles use memory bus. A memory read/ write employs one machine cycle. For execution of the programs, the system utilizes 90 percent of the CPU time. For block data transfer, an IO device is attached to the system while CPU executes the background programs continuously. What is the maximum IO data transfer rate if programmed IO data transfer technique is used?

- A 500 Kbytes/sec
- B 2.2 Mbytes/sec
- C 125 Kbytes/sec
- D 250 Kbytes/sec

#### Question 214

In comparison with static RAM memory, the dynamic Ram memory has

- A lower bit density and higher power consumption
- B higher bit density and higher power consumption
- C lower bit density and lower power consumption
- D higher bit density and lower power consumption

#### Question 215

In the Big-Endian system, the computer stores

- A MSB of data in the lowest memory address of data unit
- B LSB of data in the lowest memory address of data unit
- C MSB of data in the highest memory address of data unit
- D LSB of data in the highest memory address of data unit

**Question 216**

How many PUSH and POP operations will be needed to evaluate the following expression by reverse polish notation in a stack machine  $(A * B) + (C * D / E)$ ?

- A 4 PUSH and 3 POP instructions
- B 5 PUSH and 4 POP instructions
- C 6 PUSH and 2 POP instructions
- D 5 PUSH and 3 POP instructions

**Question 217**

A hierarchical memory system that uses cache memory has cache access time of 50 nano seconds, main memory access time of 300 nano seconds, 75% of memory requests are for read, hit ratio of 0.8 for read access and the write-through scheme is used. What will be the average access time of the system both for read and write requests ?

- A 157.5 n.sec.
- B 110 n.sec.
- C 75 n.sec.
- D 82.5 n.sec.

**Question 218**

Temporal cohesion means

- A Coincidental cohesion
- B Cohesion between temporary variables
- C Cohesion between local variables
- D Cohesion with respect to time

**Question 219**

Various storage devices used by an operating system can be arranged as follows in increasing order of accessing speed:

- A Magnetic tapes → magnetic disks → optical disks → electronic disks → main memory → cache → registers
- B Magnetic tapes → magnetic disks → electronic disks → optical disks → main memory → cache → registers
- C Magnetic tapes → electronic disks → magnetic disks → optical disks → main memory → cache → registers
- D Magnetic tapes → optical disks → magnetic disks → electronic disks → main memory → cache → registers

**Question 220**

How many disk blocks are required to with 1 kB block size using linked list number is stored in 32 bits.

- A 1024 blocks
- B 16794 blocks
- C 20000 blocks
- D 1048576 blocks
- E ALL are correct.

**Question 221**

A computer uses ternary system instead of the traditional binary system. An  $n$  bit string in the binary system will occupy

- A  $3 + n$  ternary digits
- B  $2^n$  binary digits

- A  $2^{11} / 3$  ternary digits
- B  $n(\log_2 3)$  ternary digits
- C  $n(\log_3 2)$  ternary digits

### Question 222

Micro program is

- A the name of a source program in micro computers
- B set of micro instructions that defines the individual operations in response to a machine-language instruction
- C a primitive form of macros used in assembly language programming
- D a very small segment of machine code

### Question 223

Of the following, which best characterizes computers that use memory-mapped I/O?

- A The computer provides special instructions for manipulating I/O ports
- B I/O ports are placed at addresses on the bus and are accessed just like other memory locations
- C To perform I/O operations, it is sufficient to place the data in an address register and call channel to perform the operation
- D I/O can be performed only when memory management hardware is turned on

### Question 224

A byte addressable computer has a memory capacity of  $2^m$  KB (kbytes) and can perform  $2^m$  operations. An instruction involving 3 operands and one operator needs maximum of

- A  $3m$  bits
- B  $3m + n$  bits
- C  $m + n$  bits



none of the above

**Question 225**

A particular parallel program computation requires 100 sec when executed on a single processor. If 40% of this computation is inherently sequential (i.e. will not benefit from additional processors), then theoretically best possible elapsed times of this program running with 2 and 4 processors, respectively, are



20 sec and 10 sec



30 sec and 15 sec



50 sec and 25 sec



70 sec and 55 sec

**Question 226**

For a multi-processor architecture, In which protocol a write transaction is forwarded to only those processors that are known to possess a copy of newly altered cache line ?



Snoopy bus protocol



Cache coherency protocol



Directory based protocol



None of the above

**Question 227**

Normally user programs are prevented from handling I/O directly by I/O instructions in them. For CPUs having explicit I/O instructions, such I/O protection is ensured by having the I/O instructions privileged. In a CPU with memory mapped I/O, there is no explicit I/O instruction. Which one of the following is true for a CPU with memory mapped I/O ?



I/O protection is ensured by operating system routines.

- A I/O protection is ensured by a hardware trap.
- B I/O protection is ensured during system configuration.
- C I/O protection is not possible.

### Question 228

CMOS is a Computer Chip on the motherboard, which is:

- A RAM
- B ROM
- C EPROM
- D Auxiliary storage

### Question 229

Match the items in List - I and List - II:  
codes:

- | List - I  | List - II        |
|---|------------------|
| (a) Interrupts which can be delayed when a much highest priority interrupt has occurred | (i) Normal       |
| (b) Unplanned interrupts which occur while executing a program                          | (ii) Synchronous |
| (c) Source of interrupt is in phase with the system clock                               | (iii) Maskable   |
|   | (iv) Exception   |

- | (a) | (b)   | (c)  |
|-----|-------|------|
| (1) | (ii)  | (i)  |
| (2) | (ii)  | (iv) |
| (3) | (iii) | (i)  |
| (4) | (iii) | (iv) |

- A (1)
- B (2)
- C (3)

(4)**Question 230**

Which of the following mapping is not used for mapping process in cache memory?

- A Associative mapping
- B Direct mapping
- C Set-Associative mapping
- D Segmented - page mapping

**Question 231**

In 8085 microprocessor, what is the output of following program? LDA 8000H MVI B, 30H ADD B STA 8001H

- A Read a number from input port and store it in memory
- B Read a number from input device with address 8000H and store it in memory at location 8001H
- C Read a number from memory at location 8000H and store it in memory location 8001H
- D Load A with data from input device with address 8000H and display it on the output device with address 8001H

**Question 232**

A direct mapped cache memory of 1 MB has a block size of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes 20 ns to bring the first word of a block from the main memory, while each subsequent word takes 5 ns. The word size is 64 bits. The average memory access time in ns (round off to 1 decimal place) is \_\_\_\_\_.

**Note** - This question was Numerical Type

- A 13.5
- B 15.5
- C 23.5
- D 15.3

### Question 233

A computer system with a word length of 32 bits has a 16 MB byte- addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four

physical addresses represented in hexadecimal notation.

A1 = 0x42C8A4,  
A2 = 0x546888,  
A3 = 0x6A289C,  
A4 = 0x5E4880

Which one of the following is TRUE ?

- A A1 and A4 are mapped to different cache sets.
- B A2 and A3 are mapped to the same cache set.
- C A3 and A4 are mapped to the same cache set.
- D A1 and A3 are mapped to the same cache set.

### Question 234

Consider a non-pipelined processor operating at 2.5 GHz. It takes 5 clock cycles to complete an instruction. You are going to make a 5- stage pipeline out of this processor. Overheads associated with pipelining force you to operate the pipelined processor at 2 GHz. In a given program, assume that 30% are memory instructions, 60% are ALU instructions and the rest are branch instructions. 5% of the memory instructions cause stalls of 50 clock cycles each due to cache misses and 50% of the branch instructions cause stalls of 2 cycles each. Assume that there are no stalls associated with the execution of ALU instructions. For this program, the speedup achieved by the

pipelined processor over the non-pipelined processor (round off to 2 decimal places) is

\_\_\_\_\_ .

Note - This question was Numerical Type.

- A 2.16
- B 2.50
- C 1.50
- D 1.16

### Question 235

A processor has 64 registers and uses 16-bit instruction format. It has two types of instructions: I-type and R-type. Each I-type instruction contains an opcode, a register name, and a 4-bit immediate value. Each R-type instruction contains an opcode and two register names. If there are 8 distinct I-type opcodes, then the maximum number of distinct R-type opcodes is \_\_\_\_\_.

Note - This question was Numerical Type.

- A 14
- B 15
- C 16
- D 12

### Question 236

Consider the following instruction sequence where registers R1, R2 and R3 are general purpose and  $\text{MEMORY}[X]$  denotes the content at the memory location X.

Instruction	Semantics	Instruction Size (bytes)
MOV R1, (5000)	$R1 \leftarrow \text{MEMORY}[5000]$	4
MOV R2, (R3)	$R2 \leftarrow \text{MEMORY}[R3]$	4
ADD R2, R1	$R2 \leftarrow R1+R2$	2
MOV (R3), R2	$\text{MEMORY}[R3] \leftarrow R2$	4
INC R3	$R3 \leftarrow R3+1$	2
DEC R1	$R1 \leftarrow R1-1$	2
BNZ 1004	Branch if not zero to the given absolute address	2

HALT

Stop

1

Assume that the content of the memory location 5000 is 10, and the content of the register R3 is 30+00. The content of each of the memory locations from 3000 to 3010 is 50. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable.

After the execution of the program, the content of memory location 3010 is \_\_\_\_\_.

- A 50
- B 60
- C 51
- D 49

### Question 237

Answer the following: a. Draw the schematic of an 8085 based system that can be used to measure the width of a pulse. Assume that the pulse is given as a TTL compatible signal by the source which generates it. b. Write the 8085 Assembly Language program to measure the width of the pulse. State all your assumption clearly.

### Question 238

Assume a two-level inclusive cache hierarchy, L1 and L2, where L2 is the larger of the two. Consider the following statements.

- S1:** Read misses in a write through L1 cache do not result in writebacks of dirty lines to the L2
- S2:** Write allocate policy must be used in conjunction with write through caches and no-write allocate policy is used with writeback caches.

Which of the following statements is correct?

- A S1 is true and S2 is false
- B S1 is false and S2 is true
- C S1 is true and S2 is true
- D S1 is false and S2 is false

**Question 239**

Which one of the following facilitates the transfer of bulk data from hard disk to main memory with the highest throughput?

- A DMA based I/O transfer
- B Interrupt driven I/O transfer
- C Polling based I/O transfer
- D Programmed I/O transfer

**Question 240**

A processor X1 operating at 2 GHz has a standard 5-stage RISC instruction pipeline having a base CPI (cycles per instruction) of one without any pipeline hazards. For a given program P that has 30% branch instructions, control hazards incur 2 cycles stall for every branch. A new version of the processor X2 operating at same clock frequency has an additional branch predictor unit (BPU) that completely eliminates stalls for correctly predicted branches. There is neither any savings nor any additional stalls for wrong predictions. There are no structural hazards and data hazards for X1 and X2. If the BPU has a prediction accuracy of 80%, the speed up (rounded off to two decimal places) obtained by X2 over X1 in executing P is\_\_\_\_\_.

- A 1.43
- B 2.43
- C 2.54
- D 1.54

**Question 241**

Let WB and WT be two set associative cache organizations that use LRU algorithm for cache block replacement. WB is a write back cache and WT is a write through cache. Which of the following statements is/are FALSE?

- Each cache block in WB and WT has a dirty bit
- Every write hit in WB leads to a data transfer from cache to main memory.

— Eviction of a block from WT will not lead to

- EVICTION of a block from WB will not lead to data transfer from cache to main memory
- A read miss in WB will never lead to eviction of a dirty block from WB

[Submit](#)

**Tags:** Computer Organization and Architecture

There are 241 questions to complete.

Take a part in the  
ongoing discussion

[View All Discussion](#)



📍 **Corporate & Communications Address:**  
A-143, 7th Floor, Sovereign Corporate Tower, Sector- 136, Noida, Uttar Pradesh (201305)

📍 **Registered Address:**  
K 061, Tower K, Gulshan Vivante Apartment, Sector 137, Noida, Gautam Buddh Nagar, Uttar Pradesh, 201305



Company	Explore	Tutorials	Courses	Offline Centers	Preparation Corner
About Us	POTD	Programming	ML and Data Science	Noida	Interview
Legal	Practice	Languages	DSA and Placements	Bengaluru	Corner
Privacy	Problems	DSA	Web	Pune	Aptitude
Policy	Connect	Web	Technology	Hyderabad	Puzzles
Careers	Blogs	Technology	AI, ML & Data Science	Kolkata	GfG 160
Contact Us	90%	AI, ML & Data Science	Development		System Design
Corporate	Refund	DevOps	Programming		
Solution	on	CS Core	Languages		
Campus	Courses	Subjects	DevOps & GATE		
Training		School	Cloud		
		Subjects	GATE		
		Software and	Trending		
		Tools	Technologies		