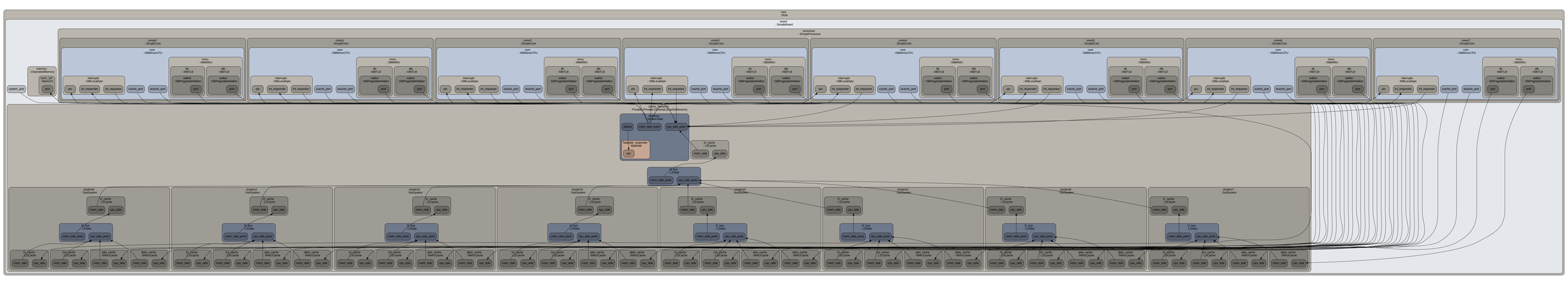

root
: Root
board
: SimpleBoard
system_port
memory
: ChanneledMemory
mem_ctrl
: MemCtrl
port
processor
: SimpleProcessor
cores0
: SimpleCore
core
: X86MinorCPU
interrupts
: X86LocalApic
pio
int_responder
int_requestor
icache_port
dcache_port
mmu
: X86MMU
itb
: X86TLB
walker
: X86PagetableWalker
port
dtb
: X86TLB
walker
: X86PagetableWalker
port
cores1
: SimpleCore
core
: X86MinorCPU
interrupts
: X86LocalApic
pio
int_responder
int_requestor
icache_port
dcache_port
mmu
: X86MMU
itb
: X86TLB
walker
: X86PagetableWalker
port
dtb
: X86TLB
walker
: X86PagetableWalker
port
cores2
: SimpleCore
core
: X86MinorCPU
interrupts
: X86LocalApic
pio
int_responder
int_requestor
icache_port
dcache_port
mmu
: X86MMU
itb
: X86TLB
walker
: X86PagetableWalker
port
dtb
: X86TLB
walker
: X86PagetableWalker
port
cores3
: SimpleCore
core
: X86MinorCPU
interrupts
: X86LocalApic
pio
int_responder
int_requestor
icache_port
dcache_port
mmu
: X86MMU
itb
: X86TLB
walker
: X86PagetableWalker
port
dtb
: X86TLB
walker
: X86PagetableWalker
port
cores4
: SimpleCore
core
: X86MinorCPU
interrupts
: X86LocalApic
pio
int_responder
int_requestor
icache_port
dcache_port
mmu
: X86MMU
itb
: X86TLB
walker
: X86PagetableWalker
port
dtb
: X86TLB
walker
: X86PagetableWalker
port
cores5
: SimpleCore
core
: X86MinorCPU
interrupts
: X86LocalApic
pio
int_responder
int_requestor
icache_port
dcache_port
mmu
: X86MMU
itb
: X86TLB
walker
: X86PagetableWalker
port
dtb
: X86TLB
walker
: X86PagetableWalker
port
cores6
: SimpleCore
core
: X86MinorCPU
interrupts
: X86LocalApic
pio
int_responder
int_requestor
icache_port
dcache_port
mmu
: X86MMU
itb
: X86TLB
walker
: X86PagetableWalker
port
dtb
: X86TLB
walker
: X86PagetableWalker
port
cores7
: SimpleCore
core
: X86MinorCPU
interrupts
: X86LocalApic
pio
int_responder
int_requestor
icache_port
dcache_port
mmu
: X86MMU
itb
: X86TLB
walker
: X86PagetableWalker
port
dtb
: X86TLB
walker
: X86PagetableWalker
port
cache_hierarchy
: PrivateL1PrivateL2SharedL3CacheHierarchy
membus
: SystemXBar
default
mem_side_ports
cpu_side_ports
badaddr_responder
: BadAddr
pio
l3_cache
: L3Cache
mem_side
cpu_side
l3_bus
: L2XBar
mem_side_ports
cpu_side_ports
clusters0
: SubSystem
l2_cache
: L2Cache
mem_side
cpu_side
l2_bus
: L2XBar
mem_side_ports
cpu_side_ports
l1i_cache
: L1ICache
mem_side
cpu_side
l1d_cache
: L1ICache
mem_side
cpu_side
iptw_cache
: MMUCache
mem_side
cpu_side
dptw_cache
: MMUCache
mem_side
cpu_side
clusters1
: SubSystem
l2_cache
: L2Cache
mem_side
cpu_side
l2_bus
: L2XBar
mem_side_ports
cpu_side_ports
l1i_cache
: L1ICache
mem_side
cpu_side
l1d_cache
: L1ICache
mem_side
cpu_side
iptw_cache
: MMUCache
mem_side
cpu_side
dptw_cache
: MMUCache
mem_side
cpu_side
clusters2
: SubSystem
l2_cache
: L2Cache
mem_side
cpu_side
l2_bus
: L2XBar
mem_side_ports
cpu_side_ports
l1i_cache
: L1ICache
mem_side
cpu_side
l1d_cache
: L1ICache
mem_side
cpu_side
iptw_cache
: MMUCache
mem_side
cpu_side
dptw_cache
: MMUCache
mem_side
cpu_side
clusters3
: SubSystem
l2_cache
: L2Cache
mem_side
cpu_side
l2_bus
: L2XBar
mem_side_ports
cpu_side_ports
l1i_cache
: L1ICache
mem_side
cpu_side
l1d_cache
: L1ICache
mem_side
cpu_side
iptw_cache
: MMUCache
mem_side
cpu_side
dptw_cache
: MMUCache
mem_side
cpu_side
clusters4
: SubSystem
l2_cache
: L2Cache
mem_side
cpu_side
l2_bus
: L2XBar
mem_side_ports
cpu_side_ports
l1i_cache
: L1ICache
mem_side
cpu_side
l1d_cache
: L1ICache
mem_side
cpu_side
iptw_cache
: MMUCache
mem_side
cpu_side
dptw_cache
: MMUCache
mem_side
cpu_side
clusters5
: SubSystem
l2_cache
: L2Cache
mem_side
cpu_side
l2_bus
: L2XBar
mem_side_ports
cpu_side_ports
l1i_cache
: L1ICache
mem_side
cpu_side
l1d_cache
: L1ICache
mem_side
cpu_side
iptw_cache
: MMUCache
mem_side
cpu_side
dptw_cache
: MMUCache
mem_side
cpu_side
clusters6
: SubSystem
l2_cache
: L2Cache
mem_side
cpu_side
l2_bus
: L2XBar
mem_side_ports
cpu_side_ports
l1i_cache
: L1ICache
mem_side
cpu_side
l1d_cache
: L1ICache
mem_side
cpu_side
iptw_cache
: MMUCache
mem_side
cpu_side
dptw_cache
: MMUCache
mem_side
cpu_side
clusters7
: SubSystem
l2_cache
: L2Cache
mem_side
cpu_side
l2_bus
: L2XBar
mem_side_ports
cpu_side_ports
l1i_cache
: L1ICache
mem_side
cpu_side
l1d_cache
: L1ICache
mem_side
cpu_side
iptw_cache
: MMUCache
mem_side
cpu_side
dptw_cache
: MMUCache
mem_side
cpu_side