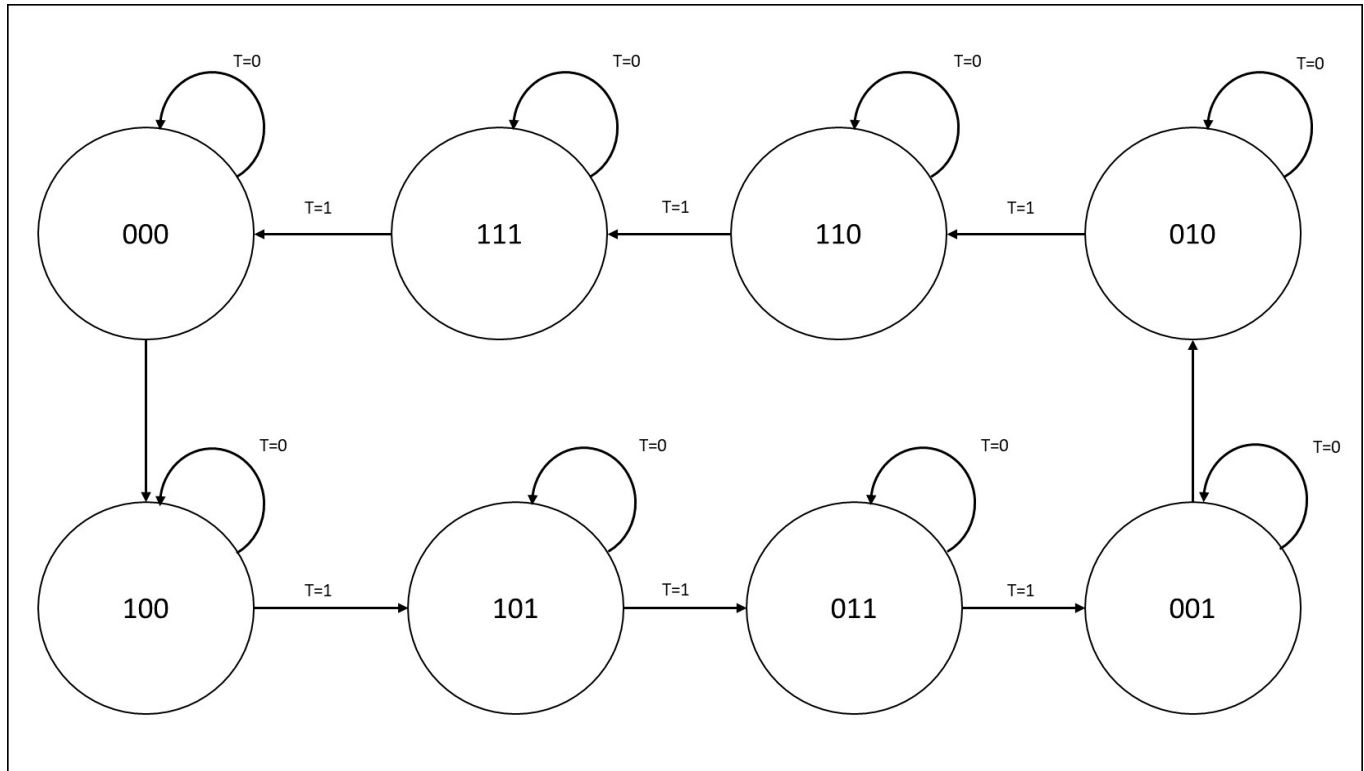
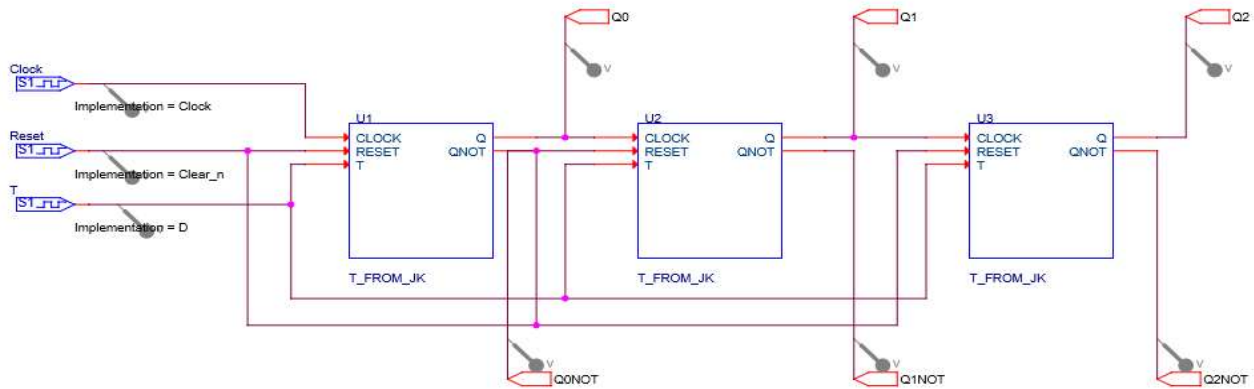


Lab 5: Circuit State Analysis

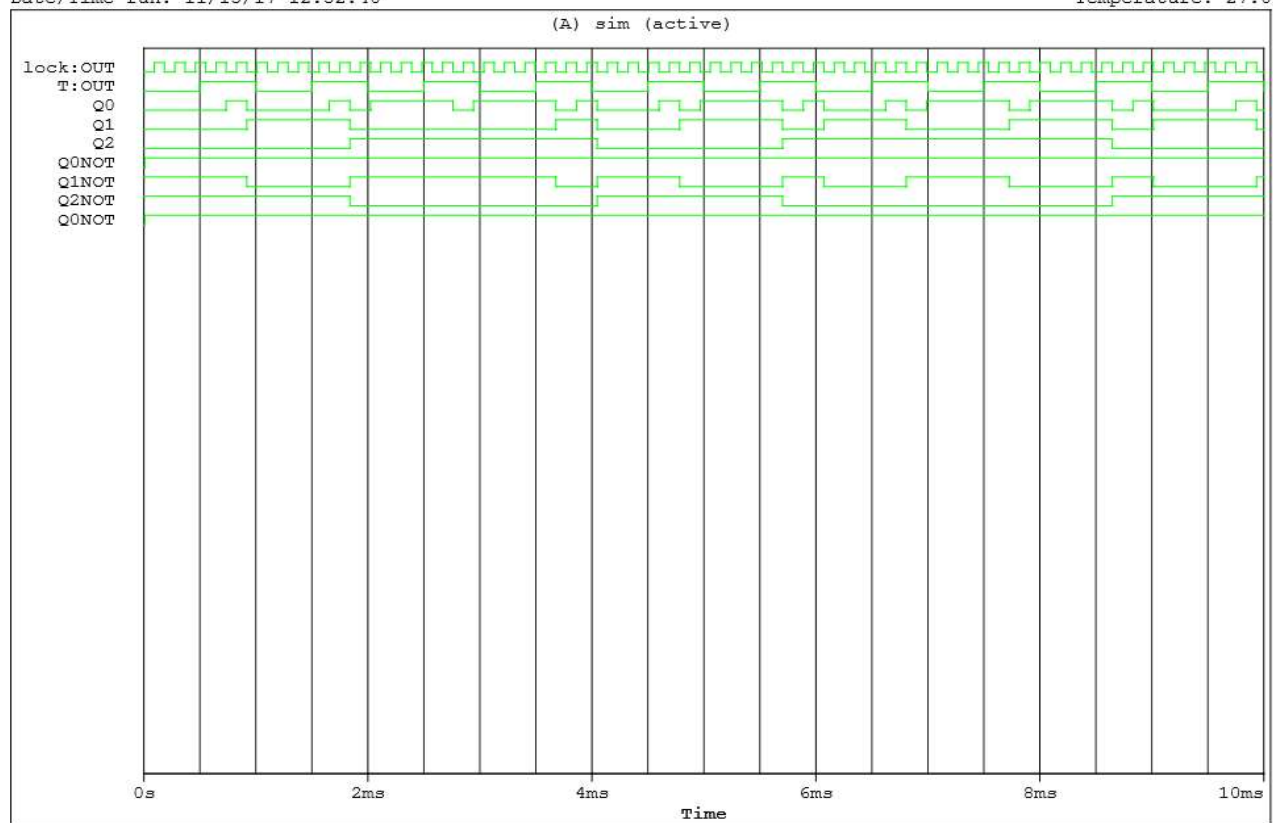
State			Inputs	Next State			Outputs					
A (U1)	B (U2)	C (U3)		A (U1)	B (U2)	C (U3)	Q0	Q1	Q2	Q0NOT	Q1NOT	Q2NOT
0	0	0	0	0	0	0	0	0	0	1	1	1
0	0	0	1	1	0	0	0	0	0	1	1	0
0	0	1	0	0	0	1	0	0	1	1	1	0
0	0	1	1	0	1	0	0	0	1	1	0	1
0	1	0	0	0	1	0	0	1	0	1	0	1
0	1	0	1	1	1	0	0	1	0	1	0	0
0	1	1	0	0	1	1	0	1	1	1	0	0
0	1	1	1	0	0	1	0	1	1	0	1	1
1	0	0	0	1	0	0	1	0	0	0	1	1
1	0	0	1	1	0	1	1	0	0	0	1	0
1	0	1	0	1	0	0	1	1	0	1	0	1
1	0	1	1	0	1	1	1	0	1	0	0	1
1	1	0	0	1	1	0	1	1	0	0	0	1
1	1	0	1	1	1	1	1	1	0	0	0	0
1	1	1	0	1	1	1	1	1	1	0	0	0
1	1	1	1	0	0	0	1	1	1	1	1	1



Lab 5: Circuit State Analysis



** Profile: "SCHEMATIC1-sim" [C:\Users\student\Desktop\temp-PSpiceFiles\SCHEMATIC1\sim.sim]
Date/Time run: 11/13/17 12:32:40 Temperature: 27.0



Date: November 13, 2017

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Time: 12:32:58