CSCI-1510 Lab 3

Be sure to read the below before starting.

PART 1

1. The circuit you are to design will output a 1 when 1 of the 4 inputs is not the same as the others. In other words, 3 of the inputs are the same. Note this does not say if the inputs are a 1 or a 0, just that they are the same.

2. You may use a K-map or algebraic manipulation to achieve the optimal circuit.

3. Create a design for this circuit. You may use 4 input NAND (7420) gates for this circuit as well as 2 input NAND gates ONLY. NO OTHER GATES ARE ALLOWED, i.e. 7404)

To accomplish this, I suggest drawing the circuit out on paper according to the result you got from your K-map and then do the distribution of bubbles to get the NAND equivalent circuit. Something to consider - NAND gates are not cascade-able so the extension to multiple inputs you used for the AND and the OR WILL NOT word for the NAND.

4. Simulate your design. This means you will have to build a stimulus file in order to test the circuit.

PART 2

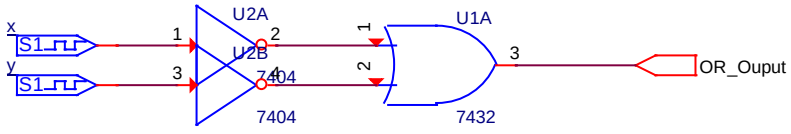
1. Design a circuit which generates a parity bit based on the values of the 3 inputs to the circuit. Information on parity generation can be found in section 3.9 of your book.

2. Add a new schematic folder to your project. Add a new page and using part 7486, build the circuit and simulate it. You may need to build a stimulus file with which to test your circuit.

NOTE: You may encounter an error that says something along the lines of too many parts. If you see this error, you need to consider how you can simplify the circuit.

HINT: Consider an OR gate with all its inputs inverted. The OR gate and the inverters on the input could be replaced by a single gate. Look at the lecture notes for Chapter three for ideas.

The OR gate and its associated inverters on the inputs can be replaced by a single gate.



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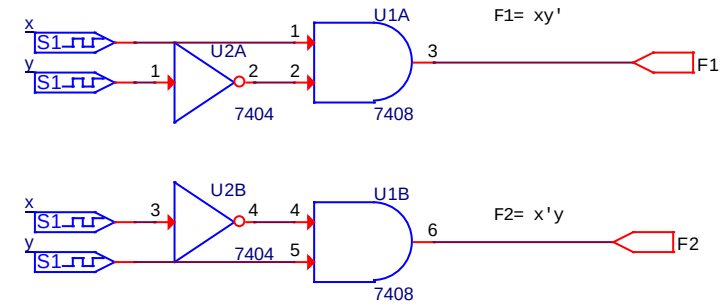
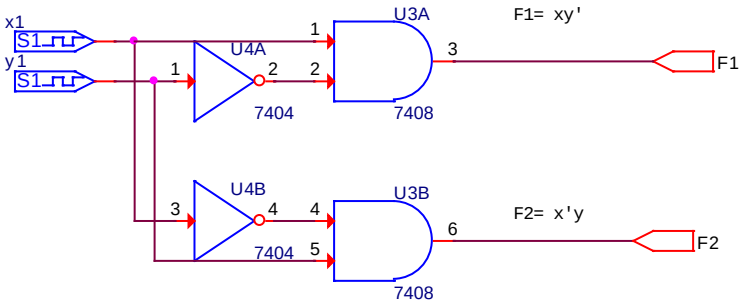
HINT: If you are using a port for every input to every gate. You can eliminate a bunch of parts (specifically ports) by using wires. See example below





Deliverables

1. Upload pdf's of your designs, stimulus files and simulation results to canvas. Remember, all pdfs must be named in such a way as to eliminate confusion, i.e. part 1 schematic, part 1 results, part 1 stimulus file, etc.

DO NOT upload the .stl file ONLY pdf's will be accepted for a grade. As always, no compressed files will be accepted – no zip etc.

PDF's will be in black and white (not greyscale) where possible.