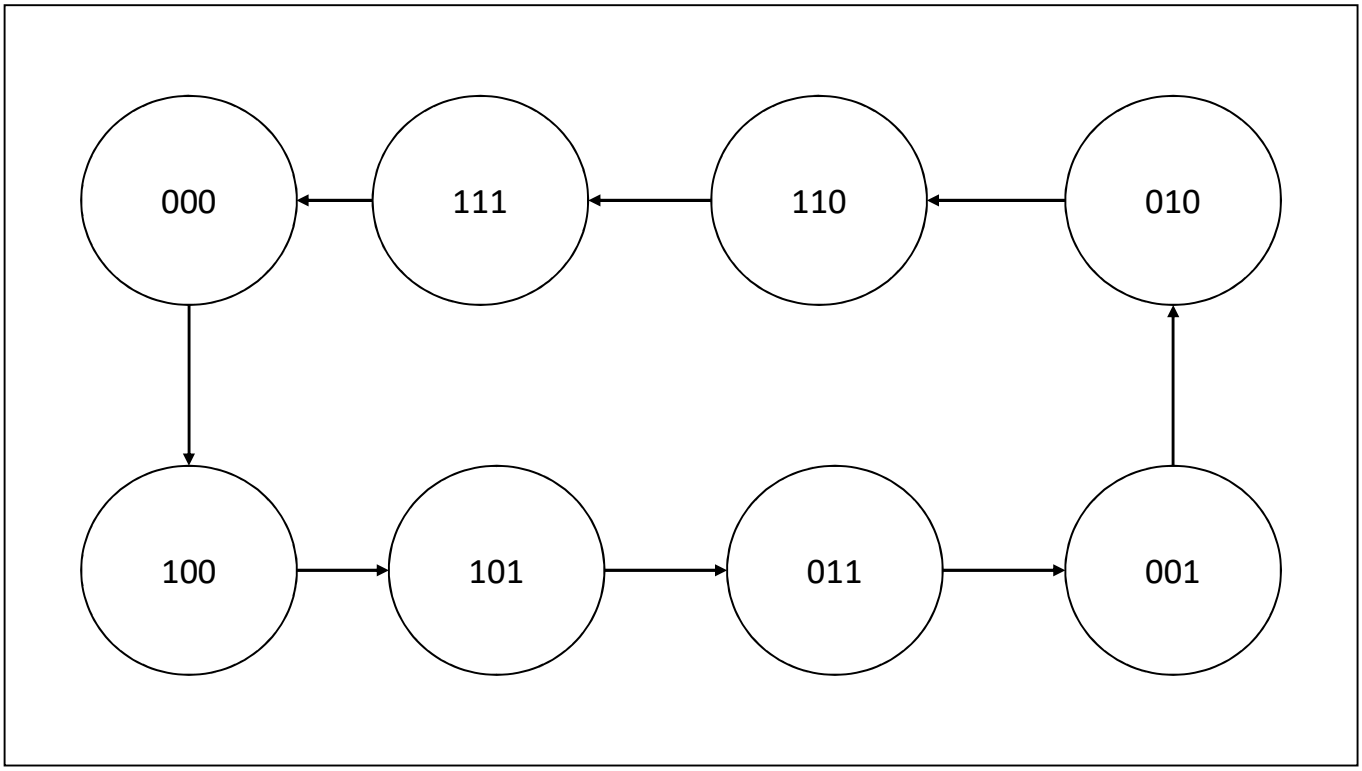
Jake Billings
11/15/2017
Logic Design

Lab 5: Circuit State Analysis

State			Inputs	Next State			Outputs					
A (U1)	**B (U2)**	**C (U3)**	**T**	**A (U1)**	**B (U2)**	**C (U3)**	**Q0**	**Q1**	**Q2**	**Q0NOT**	**Q1NOT**	**Q2NOT**
0	0	0	0	0	0	0	0	0	0	1	1	1
0	0	0	1	1	0	0	0	0	0	1	1	0
0	0	1	0	0	0	1	0	0	1	1	1	0
0	0	1	1	0	1	0	0	0	1	1	0	1
0	1	0	0	0	1	0	0	1	0	1	0	1
0	1	0	1	1	1	0	0	1	0	1	0	0
0	1	1	0	0	1	1	0	1	1	1	0	0
0	1	1	1	0	0	1	0	1	1	0	1	1
1	0	0	0	1	0	0	1	0	0	0	1	1
1	0	0	1	1	0	1	1	0	0	0	1	0
1	0	1	0	1	0	1	1	0	1	0	1	0
1	0	1	1	0	1	1	1	0	1	0	0	1
1	1	0	0	1	1	0	1	1	0	0	0	1
1	1	0	1	1	1	1	1	1	0	0	0	0
1	1	1	0	1	1	1	1	1	1	0	0	0
1	1	1	1	0	0	0	1	1	1	1	1	1



Jake Billings
11/15/2017
Logic Design

Lab 5: Circuit State Analysis