Lab 5 : Examining Flip-Flops and Latches

For this lab it is crucial that you put your flip-flop in a known state – either SET or RESET (Terminology: RESET = CLEAR).

For this lab, you will need to ensure that your clock signal is NOT a harmonic of your input signals AND that the clock signal is the highest frequency. For example, if working with a D flip-flop, the input to D could be 1000hz, but the clock could be 5436hz which is definitely not a harmonic, or multiple of 1000hz.

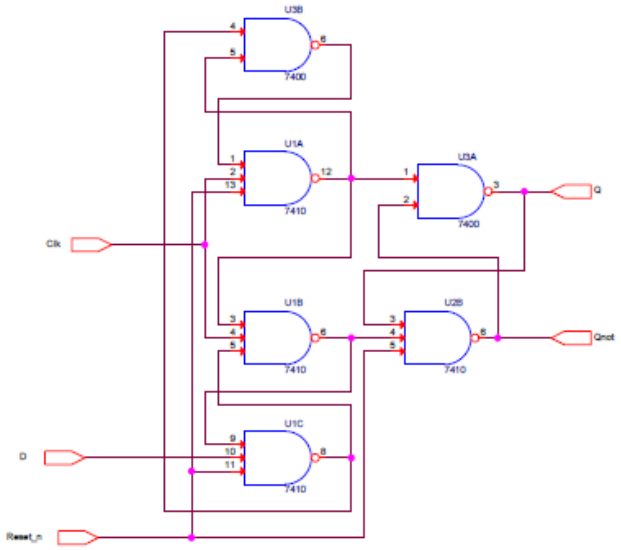
Part 1. – D Latches and Flip-flops

1. Build the D-Flip-flop shown below. NOTE: a pdf of this figure is available as a separate file on Canvas.

2. Create a part for the D-Flip-Flop.

3. Create a new page and a circuit which will test your D-Flip-flop. The part with appropriate Digital Stimulus will suffice. A .stl file with a sample clear stimulus will be provided to you. Do not make your own clear/reset stimulus.

4. Run a simulation.



Part 2 T and D from JK

1. Using part 74107 (JK flip-flop), build a T and a D-flip. Do NOT put both designs on the same schematic page or in the same folder.

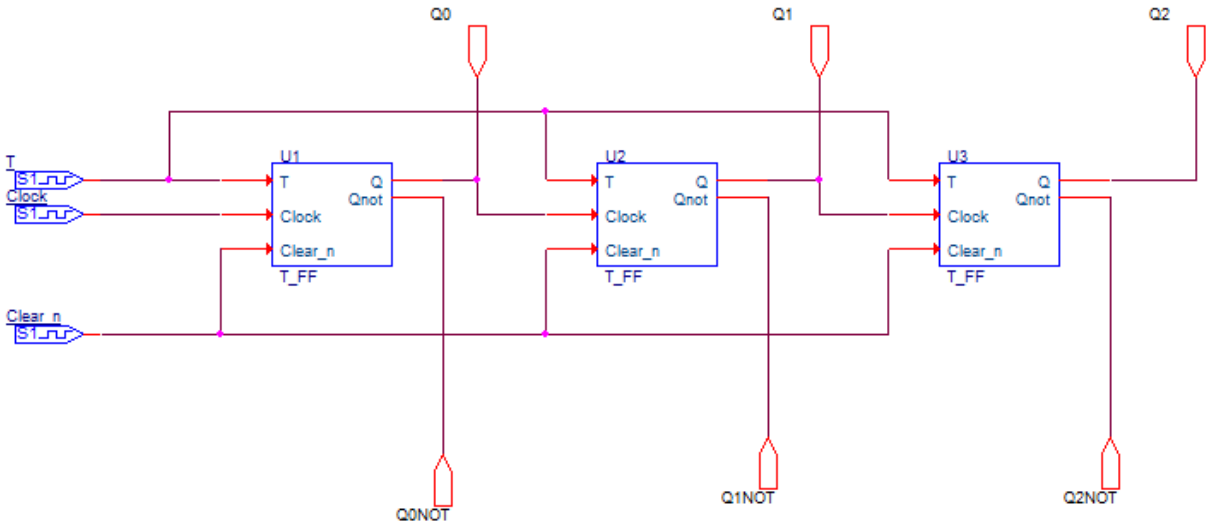
2. Create parts for each and run a simulation using the parts created.

Part 3. Mystery Circuit

1. Given the following design.

    a. Create a state table

    b. Create a state diagram



2. Build the circuit, using your T flip flop from Part 3.

3. Simulate the design.

Part 4 Deliverables - UPLOADED TO CANVAS

1. Pdf's of your designs, simulation results and your .stl file(s).

2. Online submission of the State Table and State Diagram. Use Word or Excel to create your state Table and use powerpoint to create the state Diagram. NO SCANS or PICTURES will be accepted for a grade.