CE1901 LABORATORY PROJECT

SUMMARY

In the 1960s, the integrated circuit started a new era in digital design because microminiaturization allowed multiple transistor switches to be integrated together in an enclosed package called a "chip." This integration allowed computers to shrink in size and helped spark the race to outer space, the desktop calculator and eventually the personal computer revolution. Integrated transistor density has followed Moore's law for many decades. Moore's law states that the number of transistors fabricated on chip will double every eighteen months. Table 1 shows the effect of this remarkable doubling law.

Table 1: The Growth of Integration Density

DEVICE CATEGORY	NUMBER OF TRANSISTORS	NUMBER OF LOGIC GATES	DECADE
Small Scale Integration (SSI)	10s	Just a few	mid-1960s
Medium Scale Integration (MSI)	100s	10 – 100	late-1960s
Large Scale Integration (LSI)	1000s	1,000 – 10,000	1970s
Very Large Scale Integration (VLSI)	100,000s	10,000 – 100,000	early-1980s
Ultra Large Scale Integration (ULSI)	1,000,000s+	100,000+	mid-1980s

As the number of devices fabricated on chip continues to grow according to Moore's Law, distinctions by acronym have become uncommon. **Today, we routinely fabricate chips with billions of transistors**, but most people simply state that we are in the VLSI technology era.

While modern digital logic design practice relies extensively on computer-aided design tools and VLSI field-programmable gate arrays (FPGAs) that contain tens-of-thousands of configurable logic components, simpler digital logic chips still play a modest role in digital design. These SSI and MSI chips are used in some system level designs as "glue logic" that helps interface input devices, output devices, and memory systems to the microprocessors that form the heart of modern computing. And, because engineers balance speed, size, power, and cost, some designs don't warrant the expense of FPGAs, microprocessors, or custom chips.

Thus, it is important that all electrical and computer engineering students know gate-level logic chips from the two historical standards. Texas Instruments created a standard family of chips called the 7400 family. RCA created a standard family of chips called the 4000 family. Each of these families provides a wide range of gates, arithmetic circuits, and other logic functions. Table 2 lists example chips from the 7400 and 4000 families. Every integrated circuit chip is identified in the industry by a unique part number. Engineers-in-training slowly memorize the part numbers as they complete product designs in their undergraduate classes. Note that the

number of gates on the chip is given as part of the function name. Thus, a hex inverter chip has six inverters while a quad 2-input NOR chip has four 2-input NOR gates.

Table 2: Example Logic Gates from the Standard Logic Families

FUNCTION	ACRONYM	7400 SERIES CHIP	4000 SERIES CHIP
Quad 2-input NAND gates	NAND2	7400	4011
Quad 2-input NOR gates	NOR2	7402	4001
Hex Inverter	NOT	7404	4049
Quad 2-input AND gates	AND2	7408	4081
Quad 2-input OR gates	OR2	7432	4071

Over the next few weeks, the SSI/MSI chips from the standard logic families will be used during in-lab build-wire-test exercises. You will also learn to use a waveform pattern generator to apply test voltages to your circuits. And you will learn to use a logic analyzer to verify that applied test voltages produce correct output voltages.

PRELABORATORY WORK

1. **Install** the software that will allow you to generate test waveforms from your laptop. **Browse** to http://www.digilentinc.com and download and install the Windows version of the Waveforms software from the Software menu.
2. **Complete** the preliminary laboratory reading sections that follow in this document.

PRELIMINARY LABORATORY READING: INTEGRATED CIRCUIT CHIPS

Integrated circuit chips encase a microscopic electric circuit in a plastic or ceramic case. During fabrication, industrial robots wire the internal electrical input and output signals from the microscopic circuit to metal pins on the surface of the chip. The metal pins can be organized along any number of chip sides. The arrangement of pins is known as the **package style.** When the pins are organized along the two longer sides of a rectangular shaped chip, the package style is called a **dual in-line pin** package (DIP). Figure 1 show an integrated circuit DIP chip correctly inserted into a type of prototyping environment known as a plug board or a breadboard.

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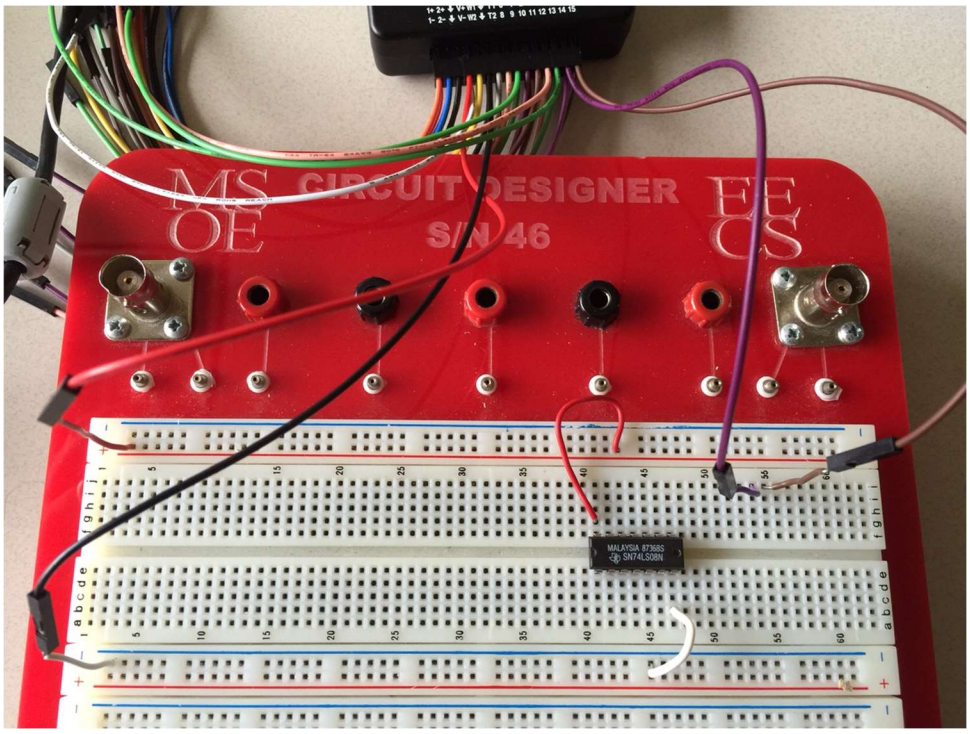

Figure 1: A Breadboard with IC

The breadboard allows electrical connections to be made without the need to heat a metal to a melting point capable of bonding items together. Instead, chips and wires can be inserted into the breadboard holes and spring-like contacts make the electrical connections.

The breadboard is divided into two halves – a top half and a bottom half. The bottom half has rows labeled **abcde** and the top half has rows labeled **fghij**. The halves are isolated from each other by a depression in the plastic – the chip gap. Each half contains sixty-four (64) columns.

Each column is a unique connection node for wires and chip pins. ***Any wire or chip pin plugged into the same column is electrically connected to everything else plugged into that column.*** Each column consists of five plug points. Each plug point in a column supports only one pin or wire. Figure 2 shows these lettered rows and numbered columns.

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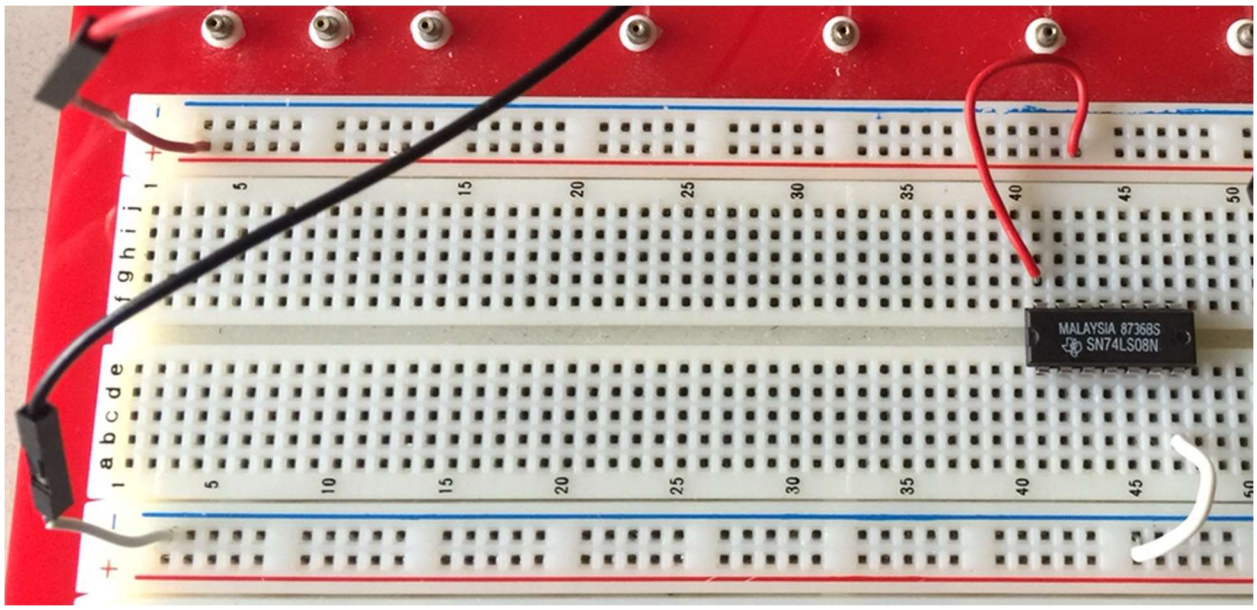

Figure 2: A Closer View of a Breadboard

Breadboards often contain power lines. In Figure 2, four power lines are visible: two red colored power lines and two blue colored power lines. Any plug point along the power line is connected to the power line. Thus, Figure 2 shows battery power coming onto the board from the Analog Discovery Kit along the left-hand side. **Red wire** is used in digital circuits to represent the hot terminal of the battery. This high energy terminal is usually called V+, VDD, VCC, or BAT+ on schematic diagrams. **Black, blue, or white wire** is used in digital circuits to represent the ground terminal of the battery. This ground terminal is usually called GND or VSS in schematic diagrams.

Thus, Figure 2 shows V+ and GND energizing “hot” and “cold” power lines running the horizontal length of the board. The IC chip sits across the chip gap with its pins aligned and inserted into unique columns. Battery power and ground have been connected to appropriate pins of the chip. Why were those pins chosen? The standard logic families place power and ground pins at standard locations on the chip. For 7400 family DIP chips, power is always the pin at the upper right and ground is always the pin at the lower left. That means there must be a way of “orienting” the chip so that “top”, “bottom”, “left”, and “right” can be identified. All

DIP chips have a notch cut into one short end or a depressed dot at one short end. Some chips have both a notch and a dot. The **notch always takes precedence** in chip packaging. Figure 3 shows the top of the chip up close.

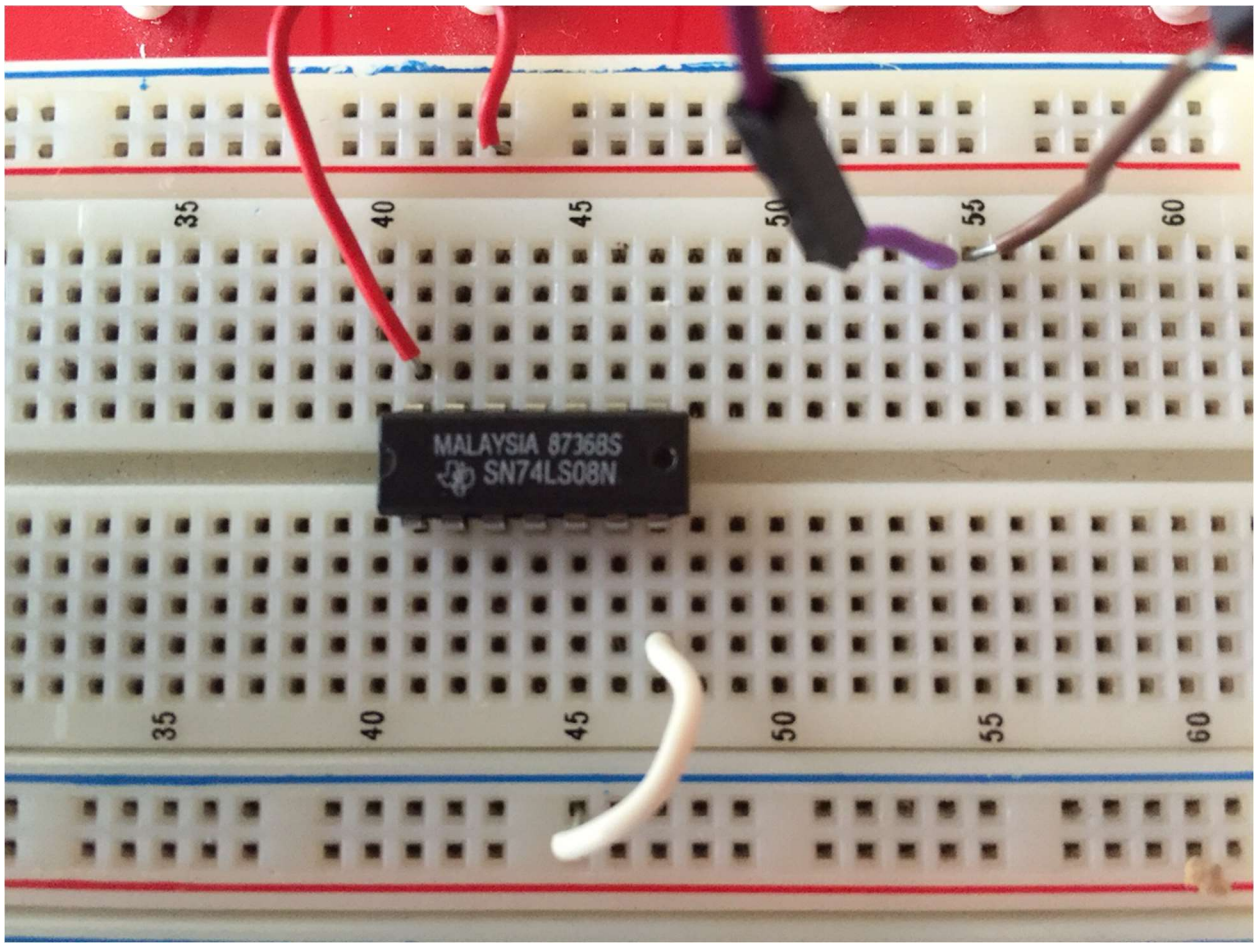

Figure 3: An Up Close View of an IC Chip

The chip in Figure 3 has both a notch and a dot. The notch takes precedence. **The notch marks the "top" of the chip**. The pins number counterclockwise beginning to the left of the notch. Thus, pin 1 is the top pin on the left side, pin 7 is the bottom pin on the left side, pin 8 is the bottom pin on the right side, and pin 14 is the top pin on the right side.

The chip package is silkscreened with its country of origin, fabrication date code, part number, and manufacturer. The date code is a 4-digit number in the format YYWW where YY represents year and WW represents the week of the year. The silkscreen of the chip in Figure 3 shows that it was fabricated in Malaysia in 1987 by Texas Instrument and is a 7408 quad 2-input AND chip. While it might seem that a 1987 chip is very old, 7400 family chips can last 50 to 60 years!

Chips are inserted in the breadboard by carefully bending and aligning the pins and then gently pushing downward until the chip pops into the board. Chips are removed from the breadboard

by using the chip remover in your laboratory kit or by using the index fingers and thumbs on opposite long sides of the chip to gently rock it back and forth across the chip gap.

Manufacturers produce datasheets to help engineers learn important information about their chips. Datasheets usually show the gate-level logic circuit, signal-to-pin diagrams, electrical characteristics, operation temperature range, and the transistor-level circuit.

- **Review** the 7404, 7408, and 7432 datasheets located in the Texas Instruments 74LSXX data book in the Manuals and Data Books Module in the Canvas course site.
- **Review** these key points about wiring chips.

KEY POINTS

Wiring is a skill that comes with practice. Remember these key points:

- each column is the ***same*** connection node
- a plug point supports only one wire or pin
- use intermediate columns to jump multiple wires to finish a connection
- use shorter wires and keep the wiring tight against the board

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PRELIMINARY LABORATORY READING: WAVEFORMS SOFTWARE

This section will describe the Waveforms software you installed during the pre-laboratory exercises. This software is used in the EECS laboratories with a product from Digilent, Inc. called the Analog Discovery kit.

- The EECS laboratories are equipped with sophisticated laboratory instruments that are used to test electrical circuits. These instruments are designed for high-speed signal sampling. The EECS laboratory equipment hangs from the benches. These benches can be raised and lowered to bring the equipment up into your workspace or lower it out of your workspace. You will learn to use all this equipment during your time at MSOE.
- The Analog Discovery kit provides a compact set of test instruments that operate at slower sampling speed. This is acceptable for most of the circuits that students build in the foundational digital logic and circuit theory courses.
- The Analog Discovery kit plugs into a USB port on your computer.
- The Analog Discovery kit provides a voltage pattern signal generator as one instrument. A voltage pattern signal generator produces patterns of 0 and 1 on circuit input signals.
- The Analog Discovery kit provides a digital logic analyzer as another instrument. A logic analyzer monitors the electrical voltage on signals and draws them on a plot of voltage versus time – a timing diagram.
- The Analog Discovery kit provides a power supply. A power supply provides battery voltages to circuits under test.

PRELIMINARY LABORATORY READING: USING THE WAVEFORMS SOFTWARE

This reading will describe using the Waveforms software. **Read** this section before lab to become familiar with the software. However, you will not be able to build circuits and follow along by using the software at home. Instead, **use** this reading material as reference during the laboratory period.

1. **Start** Waveform. The software will present you with an instrument panel if an Analog Discovery 2 or Analog Discovery 1 instrumentation kit is connected. These kits can be checked out from EECS Tech Support. The instrumentation panel is shown in Figure 4. Each instrument has a push button that opens its control panel. Also note the bottom status bar. In Figure 4, the status is reported as “OK” because an Analog Discover kit is connected to the computer and functioning properly.

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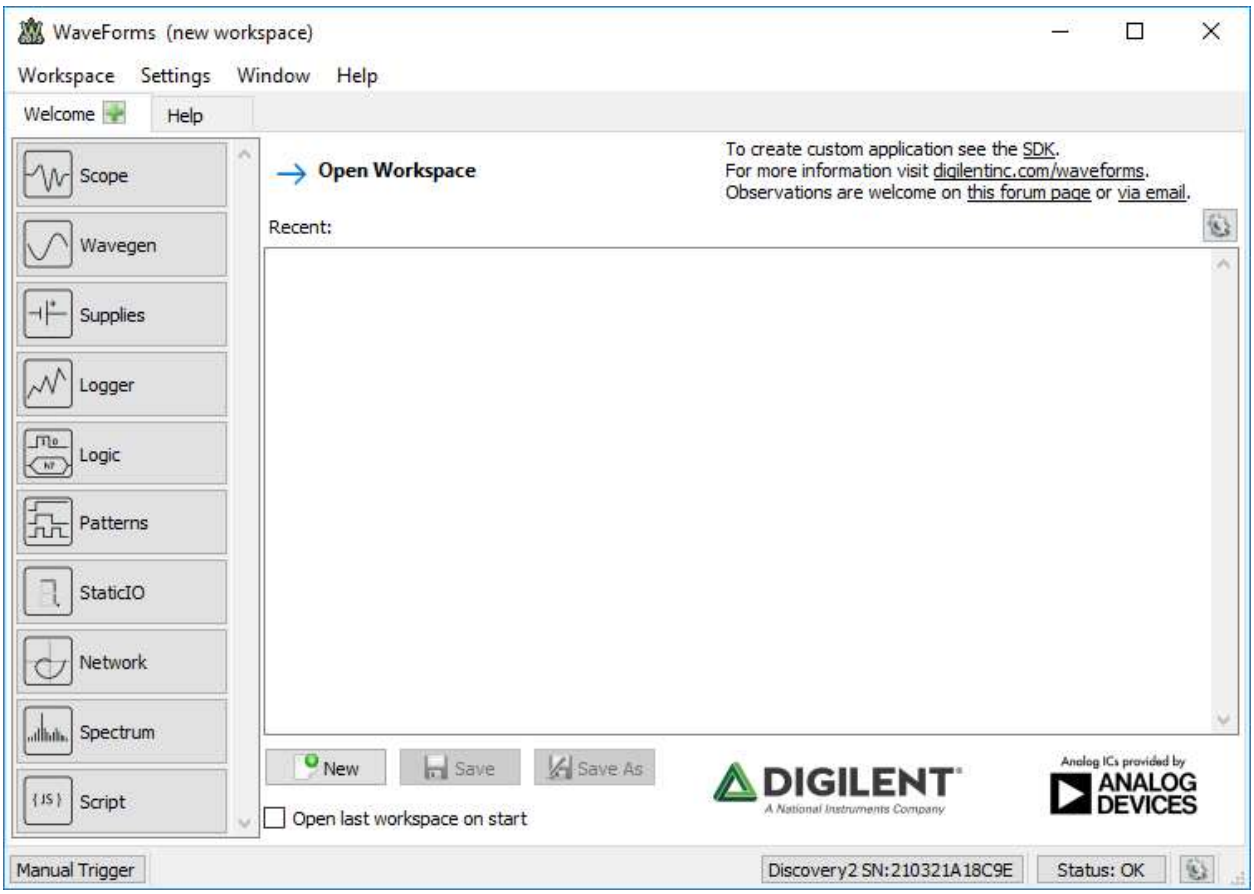

Figure 4: The Waveforms Instrument Panel

2. **Push** the buttons for Supplies (batteries), Patterns, and Logic Analyzer. Each time you press the button the focus moves to that instrument. You can return to instrument selection by clicking on the Welcome tab. **Figure 5** shows the instrument control panels open in separate tabs and the Welcome tab re-focused.

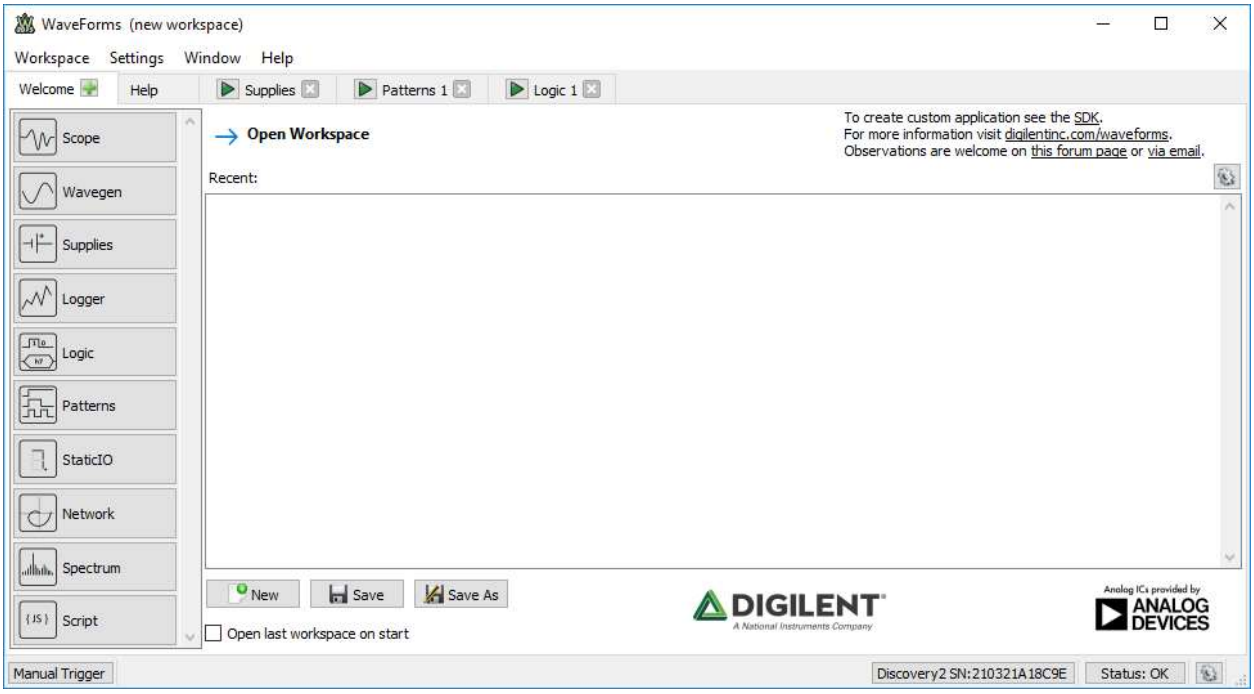

Figure 5: Waveforms with Voltage Supplies, Pattern Generator, and Logic Analyzer Tabs

3. **Remember** that all integrated circuit chips need battery power. They cannot switch (gate) energy on or off signal wires unless energy is provided! The **voltage panel** allows you to turn on a +5V battery called V+. The panel also allows you to turn on a -5V battery called V-. **Digital IC chips do not use negative voltage.** Thus, the V- battery will ***never be used*** in this course. Also **remember** that good wiring practice encourages all wiring be completed before turning batteries on.
4. The **pattern generator panel** allows you to create patterns of voltages to apply to circuit inputs. Signals and signal sets (**busses**) can either have arbitrary logic values or coordinated values like binary count sequences written onto them through time. These signals are applied as **inputs** to digital logic circuit chips.
5. The **logic analyzer panel** allows you to create signals and sets of signals to be monitored and displayed through time. In general, you apply inputs with the pattern generator and monitor outputs with the logic analyzer. The logic analyzer can simultaneously display inputs and outputs on one comprehensive voltage-versus-time graph – called a timing diagram.
6. **Build** the circuit shown in Figure 6. (**Remember**: just scan the reading during the pre-lab. You will follow these steps and **build the circuit during lab.**)
    a. The chip is the 7408 quad 2-input AND.
    b. Power (V+) is brought from the instrumentation kit to the breadboard. It is attached to the red power line. The 7408 chip is wired to power.

c. Ground is brought from the instrumentation kit to the breadboard. It is attached to the blue power line. It is marked on the instrumentation kit with something similar to a standard ground symbol, but it looks more like a downward pointing arrow (↓). The instrumentation kit provides four connections to ground – each of them a black wire. Only one is needed to connect the instrumentation kit to the blue power line on the breadboard. In the figure, the 7408 chip is shown wired to ground at the blue power line.
d. Digital input/output (DIO) signals 6 and 7 are brought to the board as AND gate inputs A and B. These are the purple and brown wires seen in the right-hand side of the figure. These signals are wired to 7408 pins 1 and 2 because the datasheet shows pins 1 and 2 as the two inputs of the first AND gate in the chip.
e. Digital input/output signal DIO1 is wired to the AND gate output on pin 3.

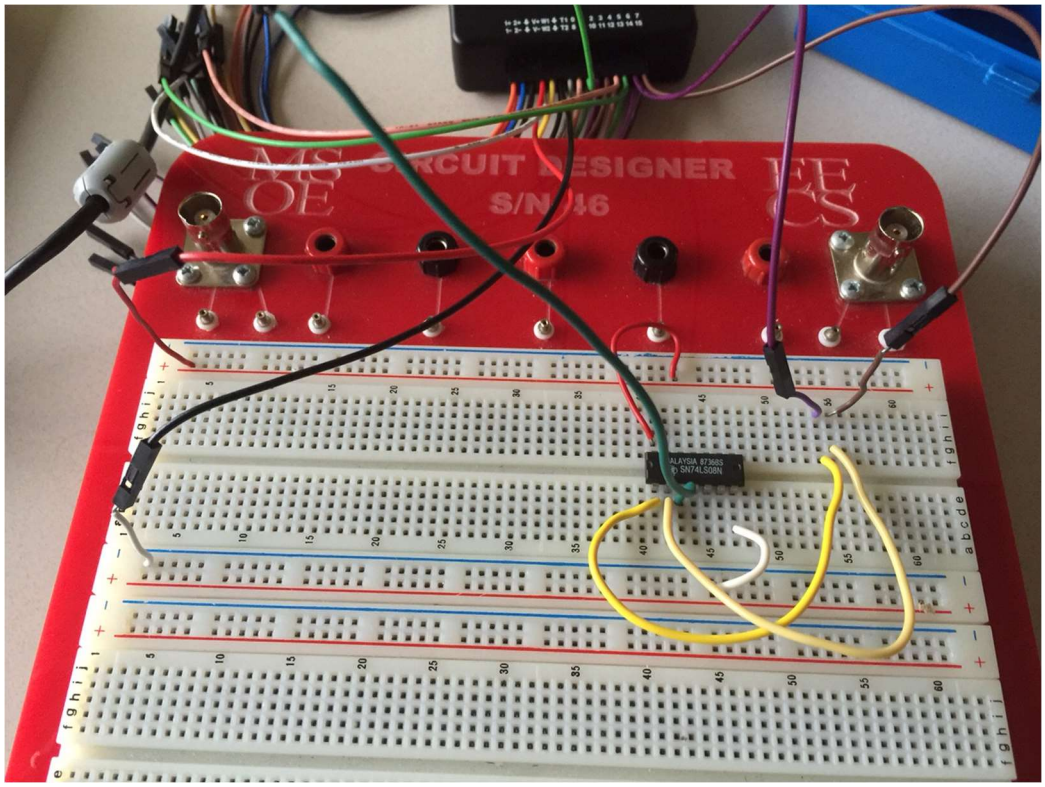

Figure 6: A 7408 AND IC Ready for Testing

7. **Configure** the pattern generator to generate voltages for circuit inputs A and B.
    a. **Move** to the Patterns tab.
    b. **Add** a bus. **Do not** add an "empty bus."
        i. **Add** digital input/output signal DIO7 to the "selected" column.
        ii. **Add** digital input/output signal DIO6 to the "selected" column.

iii. **Use** the green arrows to arrange DIO7 on top of DIO6 in the dialog box.
iv. **Close** the add selection dialog box.

c. **Push** the "constant" label in the "type" column. A pop-up menu appears.
d. **Select** "binary counter" to add a count sequence on the input signals.
e. **Note** that a 2-bit number line appears on signals DIO7 and DIO6. Remember that these signals are wired to AND gate input A and to AND gate input B. **Refer** to Figure 6 and Figure 7.

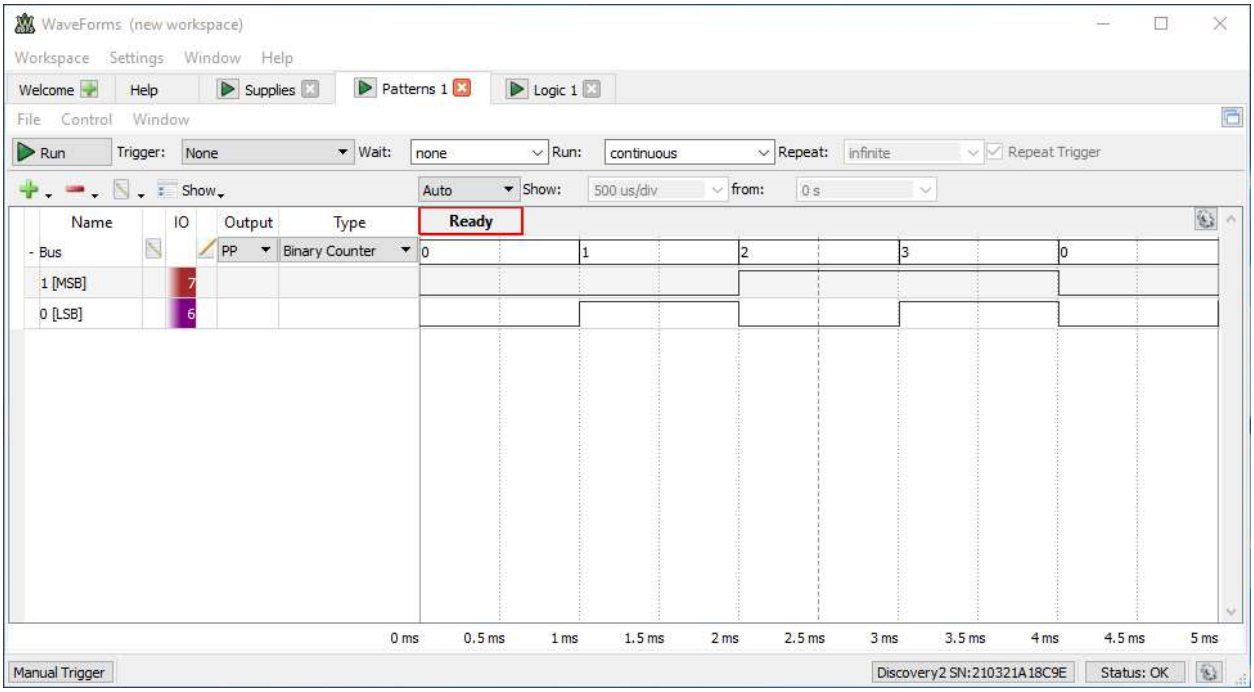

Figure 7: The Patterns instrument configured to generate a binary count sequence on the circuit input signals.

8. **Configure** the logic analyzer to monitor the circuit inputs and outputs.
   a. **Move** to the Logic tab.
   b. **Add** a bus. **Do not** add an "empty bus."
   c. **Add** DIO7 to the "selected" column.
   d. **Add** DIO6 to the "selected" column.
   e. **Use** the green arrows to move DIO7 on top and DIO6 on bottom in the dialog box.
   f. **Click** "ok" or "add" to finish adding the bus.
   g. **Add** a signal.
   h. **Add** DIO1 to the "selected" column.

i. **Click** "ok" or "add" to finish adding the signal.
j. **Compare** your work to Figure 8.

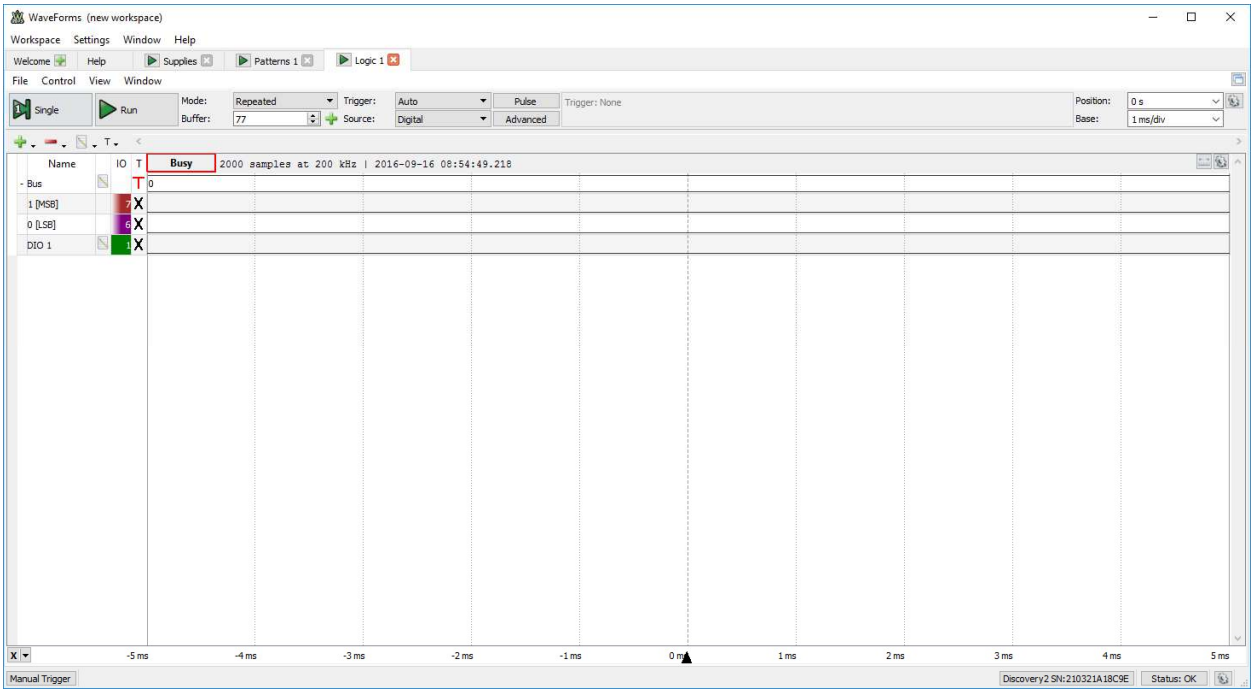

Figure 8: Logic Analyzer Ready to Draw the waveforms it samples at 7408 AND Gate

9. **Turn on** a 5V positive power supply in the Supplies tab. Standard 7400 logic chips expect a 5V energy to gate onto output signals. **Note** that there may be a "current surge" error message when the power supply is first turned on. If this occurs, just try again. **Refer** to Figure 9.

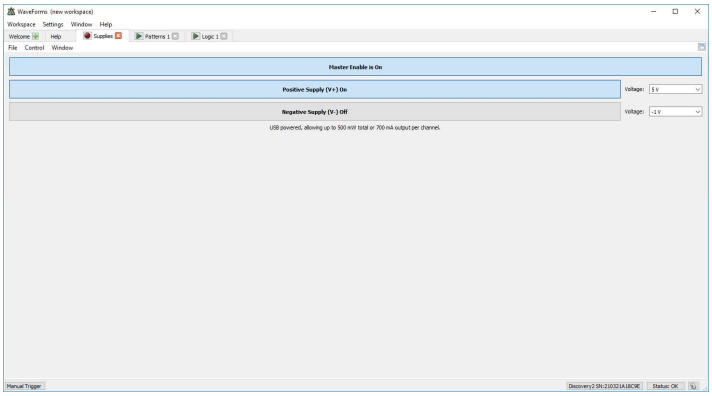

Figure 9: Power Supply Enabled at 5V

10. **Run** the circuit test.
    a. **Click** the "run" button on the pattern generator to begin applying voltages to the circuit.
    b. **Click** the "run" button on the logic analyzer to start sampling the circuit inputs and outputs in order to create a timing diagram.
    c. **Wait** a couple of seconds.
    d. **Click** the "stop" button on the logic analyzer to stop sampling and present a final timing diagram.
    e. **Verify** that the AND gate is functioning by comparing your logic analyzer timing diagram against the AND truth table. The timing diagram should look similar to Figure 10.

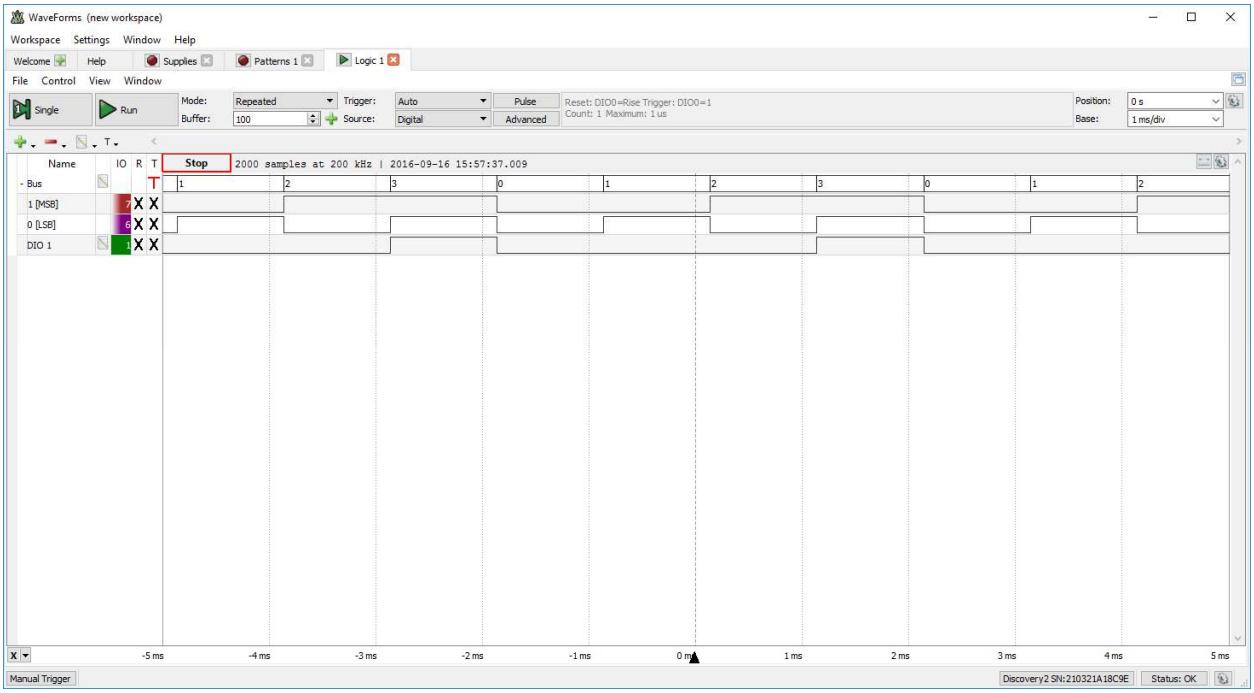

Figure 10: The Completed 7408 AND Gate Test

    f. **Note** that this simple circuit test could become much more complex. There are numerous options that can be set to control the test. You will learn more about these "trigger conditions" in later laboratories and courses.
    g. **Note** that the other three gates in the 7408 chip could be similarly tested to ensure they were operational. While you do not have to do this for this laboratory exercise, the process is simple. The DIO6 and DIO7 input wires would move to the next 7408 gate's input pins and the DIO1 output wire would move to the output pin. Continue through all gates. **Use** the 7408 data sheet to identify input-output pin sets by gate.

11. **Take a screenshot** to document your work.
    a. **Use** the Microsoft Windows "snipping tool" to grab a "new window snip".
    b. **Copy** the resulting snip to the clipboard.
    c. **Paste** the image into Microsoft Word or Microsoft OneNote as a figure with an appropriate label such as "Test of 7408 AND Gate."
12. **Stop all instruments** and **tear down** the circuit.
    a. **Click** to "stop" the logic analyzer and pattern generator.
    b. **Turn off** the power supply.
    c. **Remove** circuit wires and use your chip extractor to remove the chip.

This completes the preliminary laboratory reading.

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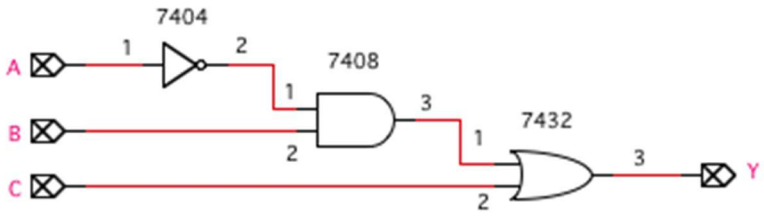
DELIVERABLES DUE DURING THE LABORATORY PERIOD

1. **Go** to EECS Tech Support and **check out** an Analog Discovery instrument kit. You will need your MSOE ID card.
2. **Complete** the Waveforms tutorial from the preliminary laboratory reading. **Build**, wire, and test the 7408 circuit. **Demonstrate** to the instructor.
3. **Build-wire-test** a prime number detector using this schematic blueprint as your guide.



   a. **Note** that the schematic shows chip numbers and suggested pin numbers. **Refer** to the 7400 family datasheets in the 74LSXX data book to see how the pin numbers were chosen. Each chip has multiple gates. Chip gates are simply assigned to schematic gates one at a time. Each gate's pins from the chip are added to the schematic. The schematic then guides wiring. **Don't forget** that each chip must be connected to battery power and ground.
   b. **Test** and **verify** the circuit using the Analog Discovery Kit.
      i. **Use** DIO signals DIO7, DIO6, and DIO5 to provide electrical input to signals A, B, C respectively with DIO7=A as the most significant bit.
      ii. **Use** DIO signal DIO1 to sample the circuit output Y.
      iii. **Use** a count sequence to apply all 8 number line values as voltages.
      iv. **Compare** the output to the energy expected for prime identification.
   c. **Demonstrate** your work to the instructor.
4. **Stop all instruments** and **tear down** the circuit.
   a. **Stop** the logic analyzer and pattern generator. **Turn off** the power supply.
   b. **Remove** circuit wires and gently remove the chips using the yellow chip extractor in your lab kit.
5. **Return** your Analog Discovery instrument kit to EECS Tech Support.
6. No laboratory report is due this week. Demonstration of the circuits earns full points.