

EE 331 Final Project

AC to DC Voltage Amplifying Converter

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Winter 2015: Picture taken on the day that the project was completed.

I. Purpose and Specifications

A. Purpose

The purpose of the design is to build an AC to DC load independent voltage supply with required specifications. The design consists of input rectifier, boost, and regulator stages. In the input stage, a rectifier with a capacitive filter is constructed to establish an unregulated DC voltage with a controlled ripple voltage. In the boost stage, the design employs a boost topology comprising a FET transistor switched inductor and a catch diode to establish a high voltage with a frequency in the accepted range. For the regulation stage, a load independent, adjustable output voltage with a strictly small ripple voltage is built using voltage regulators and op amp. The design will take an input voltage $\pm 7.5 \text{ VAC}$, obtained from the laboratory transformer and produce a minimum of $+10.0 \text{ V}_{DC}$ to a maximum of $+20.0 \text{ V}_{DC}$.

B. Required Specifications and Features

Input Stage:

1. Input voltage of $\pm 7.5 \text{ V}_{AC}$, obtained from the laboratory transformer.
2. Employ a rectifier to establish a DC voltage of approximately 10 V with a ripple of less than 1.0 V .

Timer Stage:

3. Employ an on-board oscillator with a frequency within the range of 10 kHz to 100 kHz

Boost Stage:

4. Employ a boost topology comprising a transistor switched inductor and a catch diode that feeds an output capacitor.

Regulation and Amplify Stage:

5. DC output voltage from 10 to 20 V .
6. The output voltage must be load independent, additional loads don't significantly affect the output voltage.
7. Output voltage is controlled through a single potentiometer. One side of the potentiometer will produce a 10.0 V_{DC} output and a full turn to the other side will produce a 20.0 V_{DC} output. (Independent of load)
8. The output voltage must always have less than 100 mV of ripple.

II. Block Diagram

Rectifier: The full wave-bridge rectifier converts AC source obtained from lab transformer with a magnitude $\sim 7.5 \text{ V}_{rms}$ and produces an DC output voltage of approximately 9.2 V_{DC} , creating a ripple voltage of 30 mV .

555-Timer: The 555 timer takes the input from the rectifier and outputs a square wave form with a certain frequency and Duty Cycle to the boost converter. This controls the switching of the transistor in the boost converter. This is an IC chip.

Boost converter: Takes the output voltage from the rectifier and amplifies it to a greater value. It also has an input from the 555 timer that is connected to its transistor, which acts as a switching mechanism allowing the inductor to charge and discharge.

Regulator and Amplifier: Takes the input from the inverter and regulates the voltage at $\sim 9.8 \text{ V}_{DC}$. The amplifier acts as a voltage divider to output a voltage from 10 to 20 V_{DC} using a single potentiometer to adjust the gain.

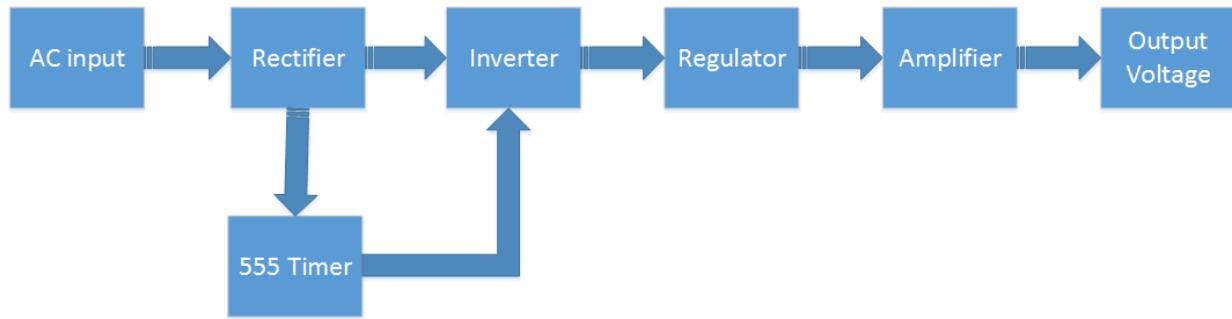


Figure - 1. AC to DC power supply block diagram

III. Schematic and description for each stage

Input Stage

Description:

The input voltage of $\pm 7.5 \text{ V}_{AC}$ comes from a transformer and is connected to a bridge rectifier, which transforms the line level AC voltage to a smaller $7.5 \text{ V}_{AC(rms)}$ signal. We then utilize a full wave bridge rectifier to convert the AC to a DC voltage ($\sim 10 \text{ V}_{DC}$ at no load). This design is implemented to prevent the voltage from being negative and thus effectively makes the input voltage only positive and closer to ideal DC. The purpose of the capacitor is to store charge in order to maintain a high level of voltage at the load with a minimal amount

of discharge. We attempted a couple of different capacitors in order to minimize our voltage ripple. We finally settled with a $470\ \mu F$ capacitor which set our ripple below $500\ mV$. Please note that our detailed data of circuit components is shown below the input stage diagram.

Calculations:

$$V_p = 7.5 * \sqrt{2} = 10.6$$

$$V_{on} = 0.7\ V$$

$$V_{dc} = V_p - 2 * V_{on} = 9.2V$$

$$V_r = (V_p - 2 * V_{on}) * \frac{T}{2 * R_f * C} = 800mV\ Max$$

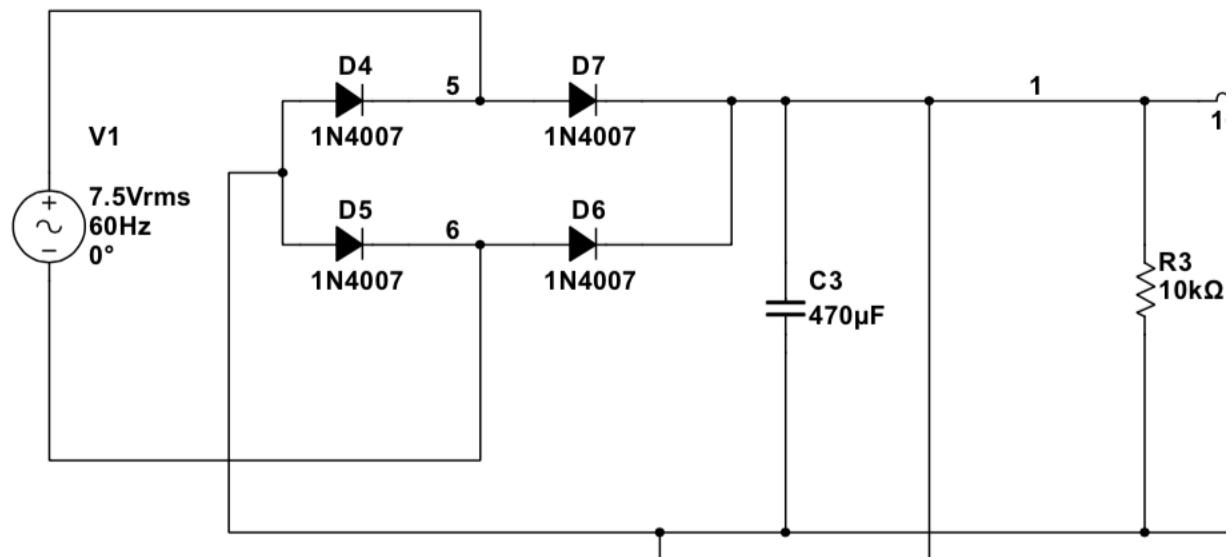


Figure - 2. Rectifier Schematic

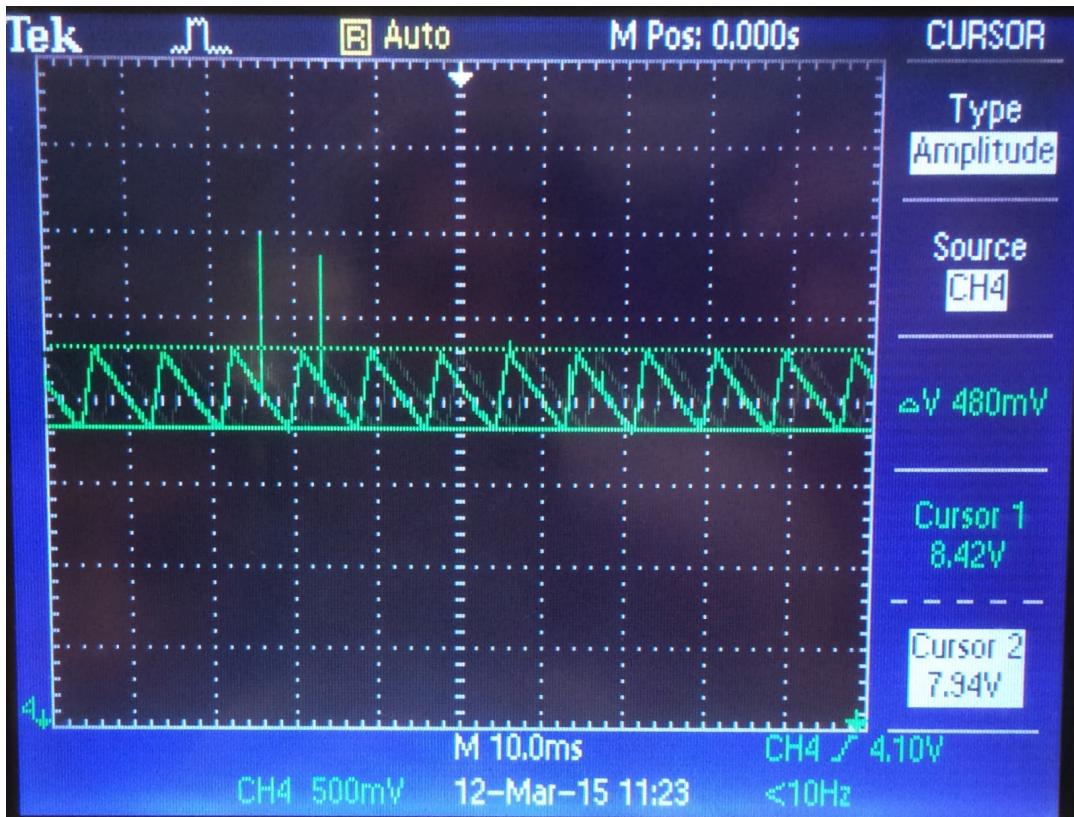


Figure - 3. Rectifier ripple voltage approximately 480 mV

Timer Stage

Description:

The timer (clock) takes the input of 10 VDC, approximately, from the input stage with a small ripple voltage to produce a square wave output voltage with a low value of 0 and a high of 10 (also affected by the small input ripple). To achieve this, we use a combination of a $6.2\text{ k}\Omega$ and a $10\text{ k}\Omega$ resistors. To dial in our duty cycle and frequency, we swapped in a 10k potentiometer and settled at a resistance of around 8k. At first, we use the default capacitor that's connected from the threshold gate with a value of 3.3 nF . But it doesn't produce the frequency that we want. Then we try several capacitors with different values and end up with a 1nF capacitor. The calculated frequency and duty cycle are given below, within the range of acceptance. The detailed schematic is shown below.

Calculations:

$$\text{Positive Time Interval } T_1 = 0.693 * (R_5 + R_8) * C$$

$$\text{Negative Time Interval } T_2 = 0.693 * R_8 C$$

$$\text{Frequency} = \frac{144}{((R_5+2*R_8)*C)} = 13.3\text{kHz}$$

$$\text{Duty Cycle} = 80\%$$

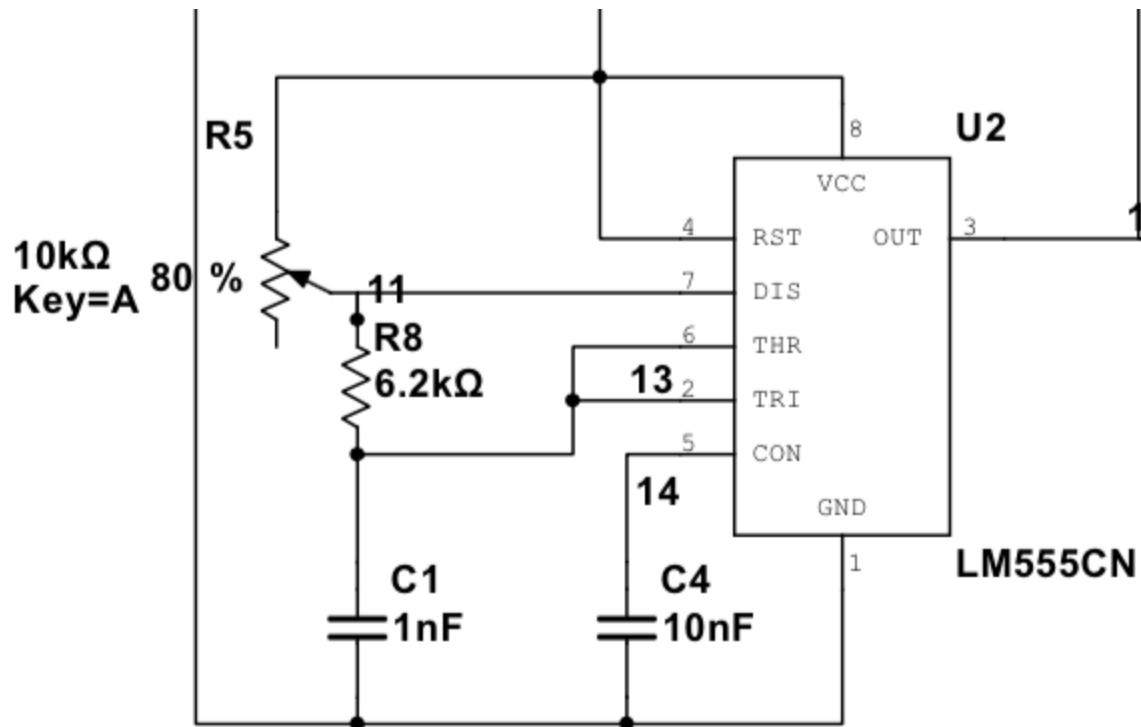


Figure - 4. Clock Schematic

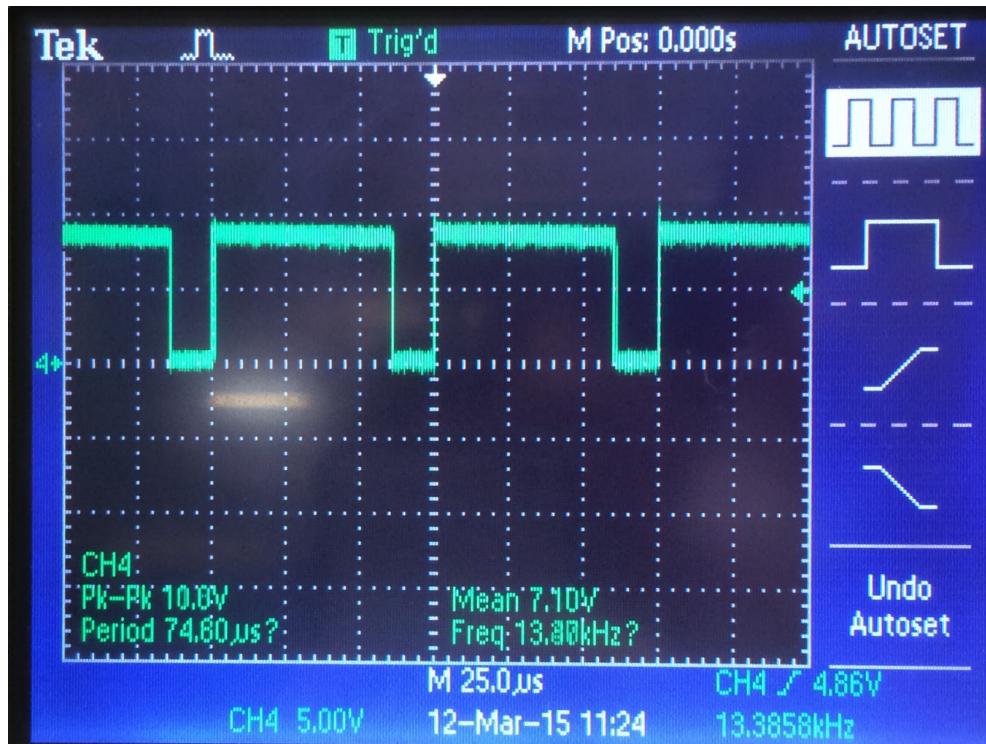


Figure - 5. Clock running at 13.4 kHz with an 81% duty cycle

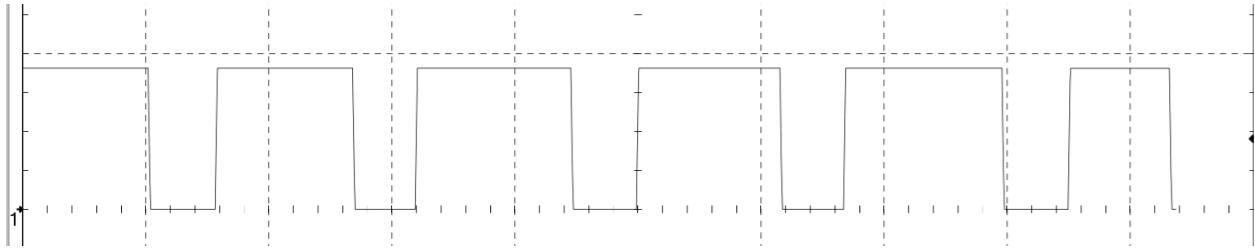


Figure - 6. Simulation of clock output running with 80% duty cycle at 11kHz

Boost Stage

Description:

The boost converter was used to boost the output voltage so that we could then regulate it to something more stable. To do this we created an inverter circuit that used the timer output to switch the mosfet between high and low. This charged and discharged the frequency dependent devices (inductor and capacitor) and resulted in a boost in our input voltage which came from the output of our rectifier stage. Specifically, this input voltage, goes through a 100 mHz inductor and the 1N4148 diode to prevent reverse current flow. The transistor used is a 2N7000 MOS transistor, in a series with 100Ω resistor, this, coupled with the timer gate input is what fuels the boost.

Calculations:

$$V_o = \frac{V_s}{1-\text{duty cycle}}, V_s = 8.5V$$

Duty Cycle = 80%

$$V_o = 30V$$

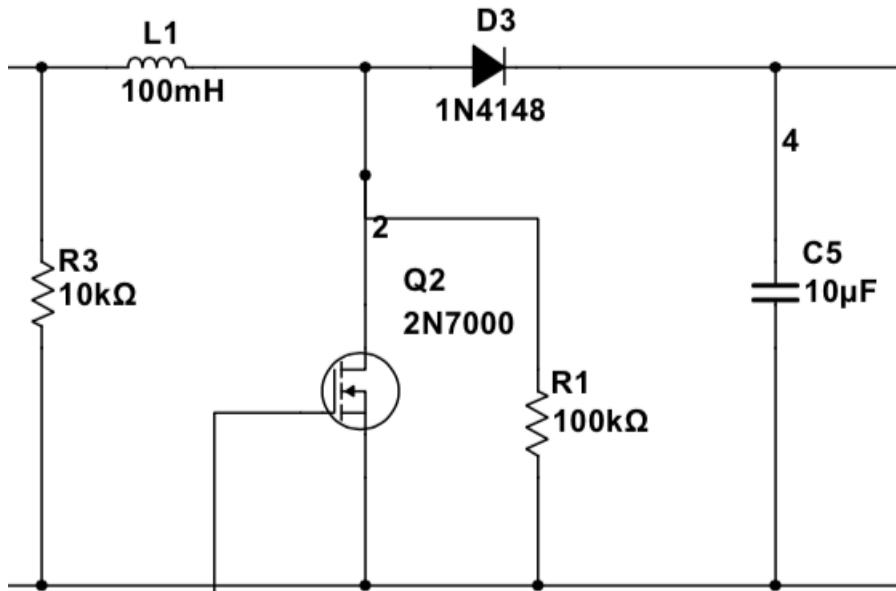


Figure - 7a. Boost Inverter Schematic

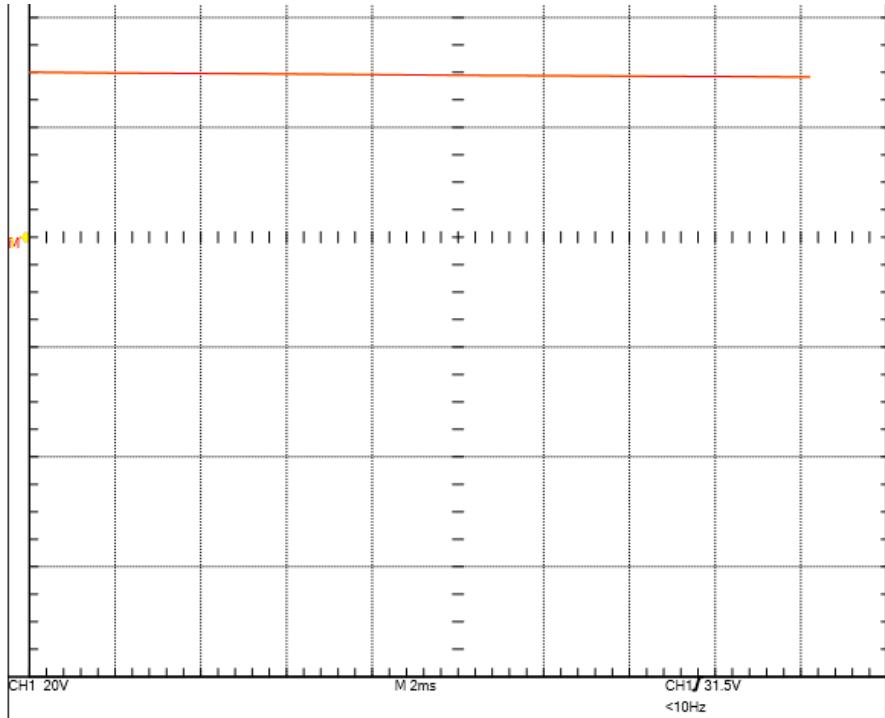


Figure 7b. - Boost stage output 31.5V

Regulated Output Amplifier

Description:

As for the output stage, it contains a regulator and amplifier. The regulator is to maintain the voltage around 10 V (our low output) for the input of amplifier, and the amplifier is to change the output voltage using a potentiometer controlled ratio that adjusted our output voltage between 10 and 20 V . Since the boosted voltage is too large and might damage our 10 V zener diode, we use a $10\text{ k}\Omega$ resistor in series with the diode. The output from the zener will be the positive input for the op amp and the negative input of the ohm amp will be grounded. Here we use a potentiometer of $100\text{ k}\Omega$ in series with a $2.3\text{ k}\Omega$ resistor, and it acts as a voltage divider with the $100\text{ k}\Omega$ resistor that's connected to the negative input of the op amp. A negative feedback voltage is produced and we can get our desired output. The 2.3k resistor gives us our minimum gain to have the low output be 10 V rather than 9.8 V which is our regulator voltage. Finally, we added a capacitor in parallel with our load to catch the ripples and lower them to a near trivial amplitude $\sim 10\text{ mV}$. In order to test the different loads, we added the required load resistances in a switchable configuration so we could easily test different load scenarios.

Calculations:

$$V_{reg} = 9.8\text{ V}$$

$$V_{out} = \left(1 + V_{in} * \left(\frac{R_{13}+R_6}{R_2}\right)\right), V_{in} = 9.8\text{ V}$$

$$V_{out} = 10.1 \text{ to } 20.1V$$

$$V_r = 30 \text{ mV}$$

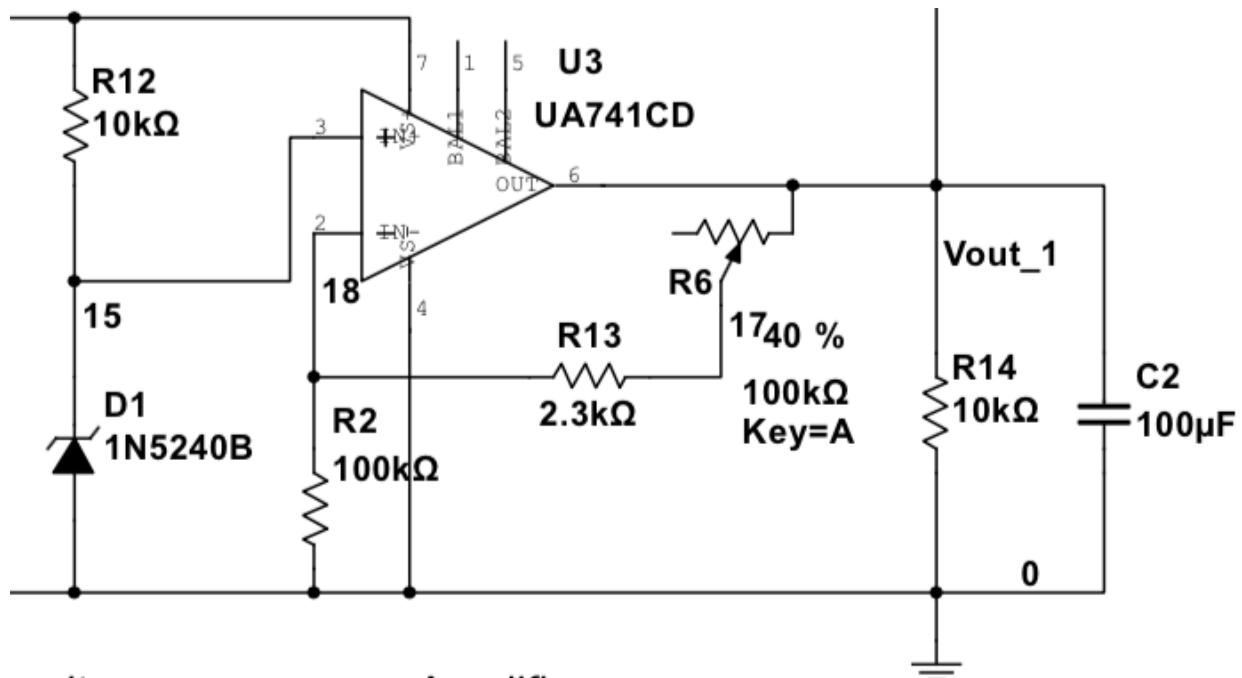


Figure - 8. Regulator and output amplifier schematic

Output Voltage



Figure - 9. 20k load at 20 V



Figure - 10. 10k load at 10 V

Extra Credit Explanation

In order to have our output adjustable between exactly 10 and 20 V via potentiometer, we employed a 741 operational amplifier with a finely tuned, adjustable ratio. This was added to the output of our regulator, which regulated the voltage near the low end, which was around 9.8 V (ideally 10.0 V). Since we were slightly below the optimal value of 10 V, we shifted our ratio (using a 2.3k resistor) so that the low side of the potentiometer was 10 V. With some trial and error, we were able to obtain a ratio that resulted in the above outputs which fairly precise to one decimal point. Since op amps to some degree are load independent, this seemed like a practical way to achieve the desired effect. It does, however, sort of diminish the benefits of the boost stage.

Alternatively (and more ideally), we could have regulated our output at the high end (20 V) and employed an output voltage PWM controlled clock for the boost stage. This way the output feedback would adjust the clock (via control pin) to keep the requested voltage constant no matter what load. This is more ideal for the constraints of our circuit constraints, but more difficult to calibrate. The end result is more efficient and scaleable for variable loads (like a motor or fan).

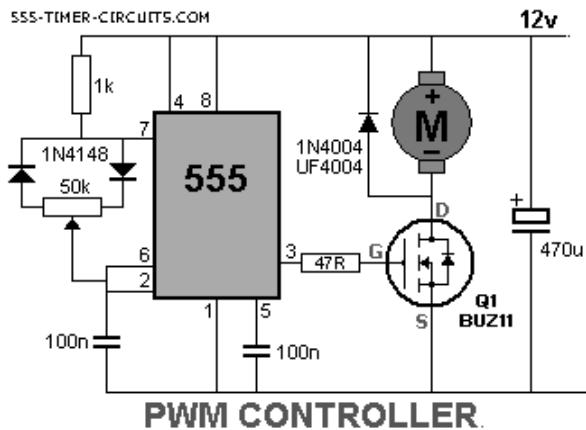


Figure - 11. Example voltage controlled pwm circuit

Final schematic:

We used multisim to generate the schematic shown below and to simulate and experiment with our circuit. For the most part it was accurate and behaved as our breadboard implementation. Multisim differed significantly in the timer stage and in order to get a similar clock behavior, we tweaked the multisim values. For some reason a 555 timer simulation under load doesn't abide to the calculations from the timer spec sheet. After getting around this issue, we built the rest of the simulation identical to our circuit. Our simulation results ranged between 10.1 and 20.1 V_{DC} which is very close to our demonstration results.

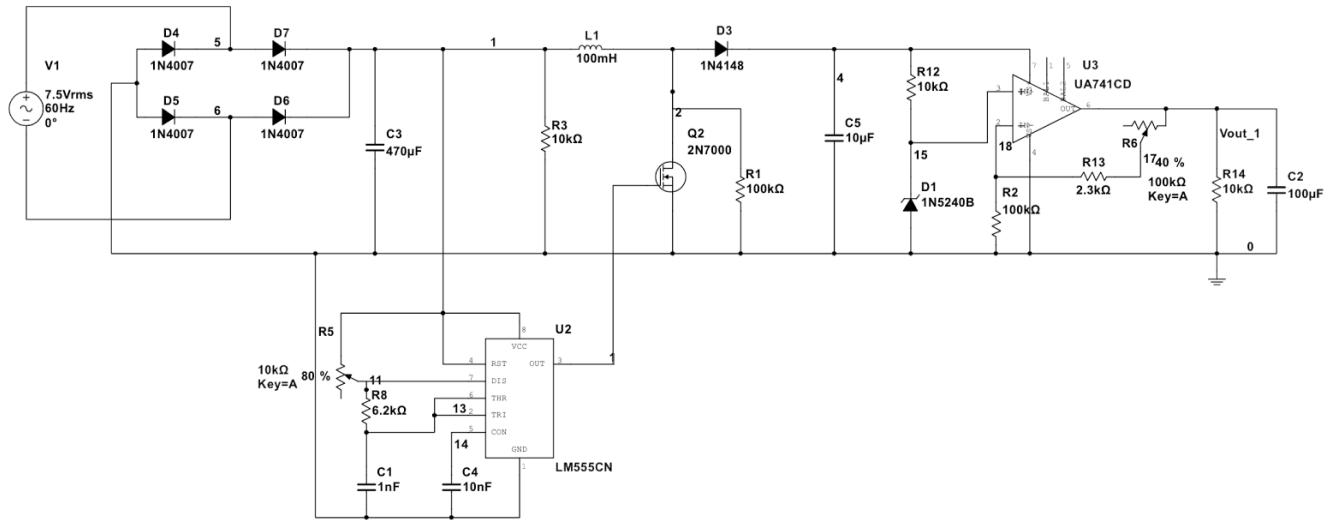


Figure - 12. Multisim schematic. Simulates with no errors and realistic output.

Final Breadboard Layout:

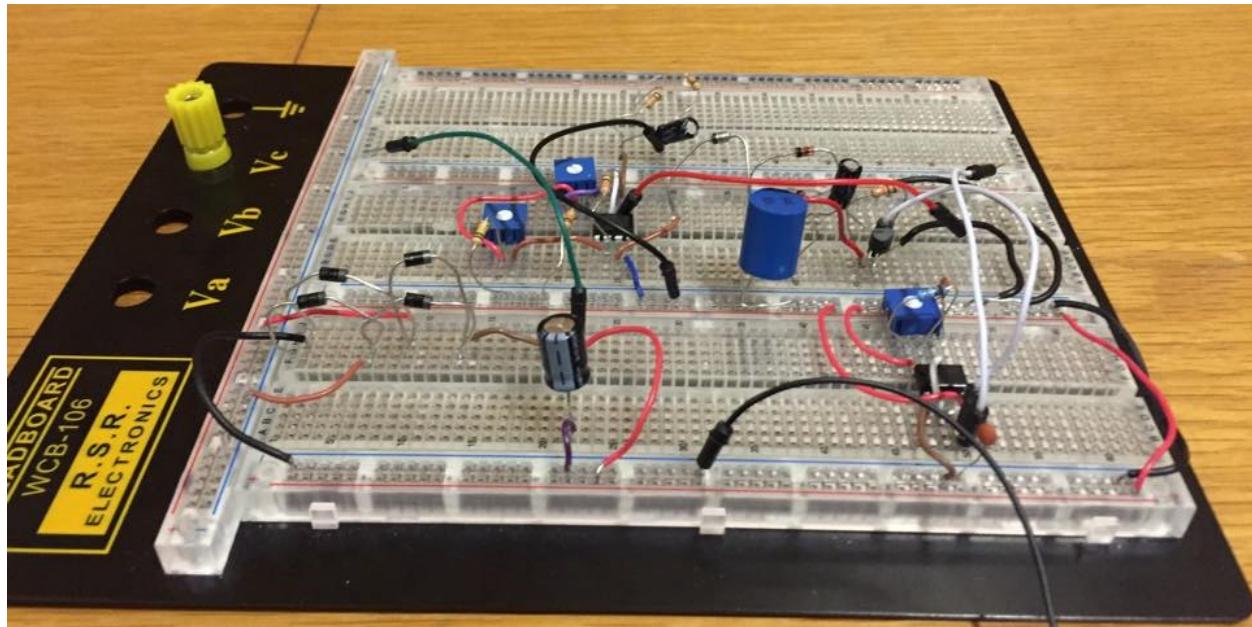


Figure - 13. Final breadboard layout. Features everything in the above schematic, plus test nodes

IV. Demonstration results

Here are the results that we got on our demonstration.

- Input Voltage:
- Output:
 - Low Voltage Limit:
 - Output voltage with open circuit: 10.08 V
 - Output voltage with $10\text{ k}\Omega$ load : 10.06 V
 - Ripple voltage with open circuit : 3.39 mV
 - Ripple voltage with $10\text{ k}\Omega$ load : 5.15 mV
 - High Voltage Limit:
 - Output voltage with open circuit: 20.13 V
 - Output voltage with $20\text{ k}\Omega$ load : 20.07 V
 - Ripple voltage with open circuit : 16.68 mV
 - Ripple voltage with $20\text{ k}\Omega$ load : 15.41 mV
- Rectifier/Filter:
 - Full Wave: 9.06 V
 - Ripple voltage on filter cap: 420 mV
- Oscillator:
 - Frequency measured: 13.3 kHz

V. Conclusion

In this project, we built an AC to DC voltage supply with required specifications. The design includes input, boost, and regulator/output stages. As for the input stage, the rectifier with a capacitive filter is constructed to establish an unregulated DC voltage with a controlled ripple voltage. In terms of the boost stage, the design is employed a boost topology comprising a transistor switched inductor and a catch diode to establish a high voltage with a frequency in the acceptance range. In the regulation stage, a load independent, adjustable output voltage with near trivial ripple voltage is built using voltage regulators and op amplifier. The design will take an input voltage $\pm 7.5\text{ V}_{AC}$, obtained from the laboratory transformer and produce the output voltage from $+10.0\text{ V}_{DC}$ (min) to the $+20.0\text{ V}_{DC}$ (max). All in all, in this lab, our team got familiar with constructing AC to DC transferred voltage supply by using our whole knowledge from the lecture along with additional skills obtained from the lab procedures and the internet.

Thanks for helping in the whole quarter.