CSE125 LAB 2 WRITEUP

Group 3:

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PART 1.

A Moore FSM is created to check the Regex expression (AB*C(A|(D(B|C|D))))*D where set S = {A,B,C,D}. Moore machines have an advantage over Mealy machines in the fact that they have a synchronous design, as the output is assigned to each state, making them more stable and predictable. This design will run through the entire expression before outputting the result even if a mismatch was already found. S0 through S3 are normal states where the FSM expects inputs matching the Regex expression. If a mismatch was found and last_symbol = 1, the FSM will enter S6, where done = 1 until negative edge res_n. If a mismatch was found and last_symbol = 0, FSM will go to S5 and wait for last_symbol to go high. The FSM will then transition to S6. 7 States are used using binary encoding. The FSM is implemented by using casex to reduce redundant statements. Each statement contain the next_state, result and done to avoid implicit latches.

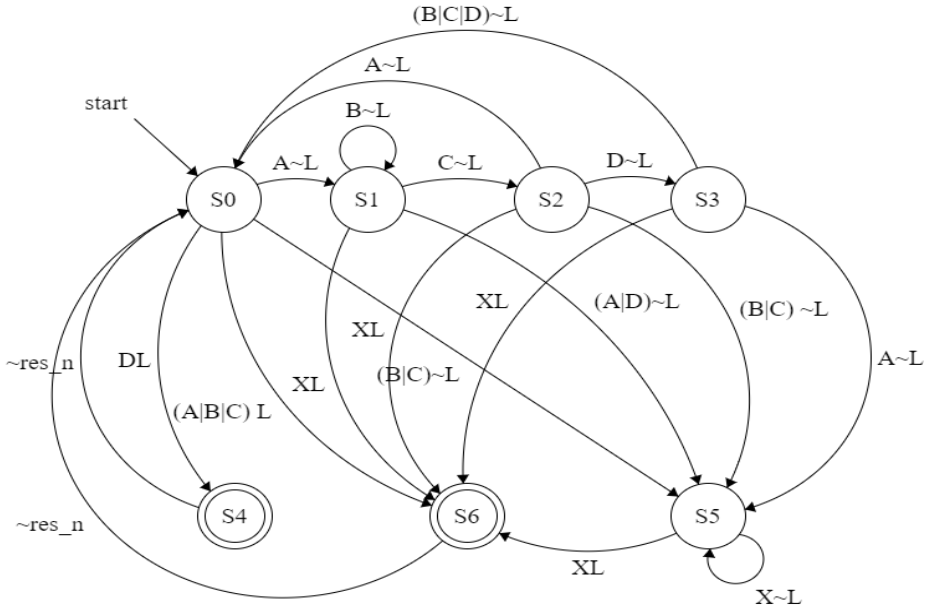

Figure 1: State Machine Diagram

STATE TABLE								
(A B* C (A + (D (B + C + D))))* D								
State	Description	Encoding	INPUT			NS	OUTPUT	
			symbol	last_ symbol	res_n		result	done
S0 - A	matching A or D	3'b000	A	0	X	B	0	0
			D	1	X	SUCCESS	0	0
			X	1	X	FAIL	0	0
			B|C	0	X	MIS	0	0
S1 - B	match A or B	3'b001	B	0	X	B	0	0
			C	0	X	C	0	0
			X	1	X	FAIL	0	0
			A|D	0	X	MIS	0	0
S2 - C	matched C	3'b010	A	0	X	A	0	0
			D	0	X	D	0	0
			X	1	X	FAIL	0	0
			B|C	0	X	MIS	0	0
S3 - D	matched D	3'b011	B|C|D	0	X	A	0	0
			X	1	X	FAIL	0	0
			A	0	X	MIS	0	0
S4 - Success	all matched	3'b100	X	X	!res_n	A	1	1
S5 - Mis	mismatch	3'b101	X	0	X	MIS	0	0
			X	1	X	FAIL	0	0
S6 - Fail	output fail	3'b110	X	X	!res_n	A	0	1

Figure 2: Detailed FSM input/output/state chart

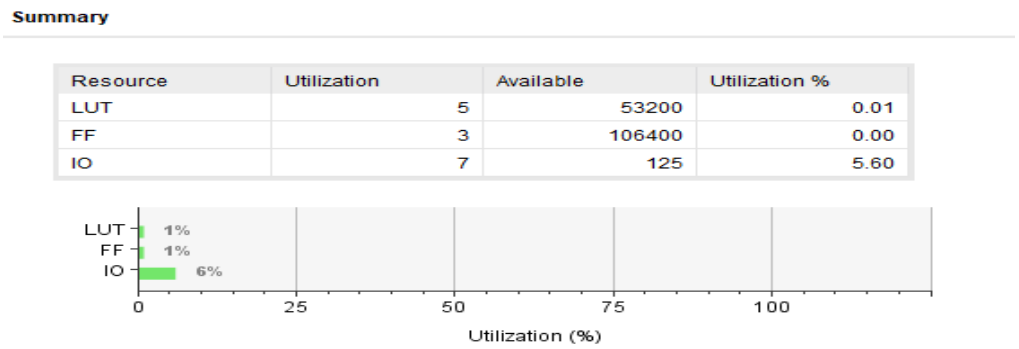

Figure 3: Resource Utilization

There were few resources used as the simple Moore Machine implementation combines the next state logic with the output logic, such that the only FFs needed were those to hold the current state, of which there were 3 to represent 7 different states in binary. This explains why there are more LUTs than FFs as more logic was necessary than memory. The constraints placed on this design had 0 in/output delay, and the clock was set to 125 MHz, this resulted in a 6.102 ns WNS. This means that the Fmax is 526 MHz.