Jake Liao

Mark Zakharov

Lab 2

4-22-20

PART 2 - TIMING

a.) A critical path is the limiting factor is circuit designs as it presents the greatest amount of delay. In the circuit presented there are two critical paths, though they are made up of the same logic block. One start to the critical path is seen as the output of R1, being fed into G2 and G3 adding one level of gate-delay, then the path continues through G4 adding another level of gate-delay, and finally finishes at the input of R1 going through G1 which creates three layers of gate-delay. The other critical path begins at the output of R2, and passes through G3, then through G2, and routes into R1 through G1 with three layers of gate-delay.

b.) Assuming this is a clock edge driven system with no skew, the values are first loaded in on the edge and must propagate through FFs R1 and R2 as they wait for the clock-to-Q delay. Once Q has been stabilized the signal from R2 goes into G3 and G1 and the signal from R1 goes into G2 and G3, each of which may present a minimum delay of 70 ps. Then the signals from G2 and G3 are presented with delay from G4 which can add a minimum of 70 ps, and that signal must then stabilize the value coming from G1 which takes another (minimum) 70 ps to propagate. Since G1 is the last signal to stabilize, after it there must be a setup time such that R1 can reliably latch the value. Adding the setup time, the clock-to-Q delay, and the three layers of gate delay gives (40+30+(3*70))=280 ps. This represents the lowest possible working delay for the circuit, setting the maximum clock frequency to be ~3.57 GHz.

c.) The input of both R1 and R2 has some form of combinatorial logic before them, with a propagation delay of at least 70-90 ps. This delay protects the FFs from any unexpected signal changes during the hold time, preventing any hold time violations. The only exception to this would be if the FFs had asynchronous, instantaneous resets, since if R2 were to be reset right at the beginning of R1s setup time, the reset signal could propagate through the 70 ps delay G1 and change the result as setup+hold time has to be 75 ps. That 5 ps difference can be fixed by changing the clock-to-Q delay to 35 ps which would have a total 285 ps delay, making a 3.5 GHz clock rate.