Technical Report: Advanced Digital Signal Processing - Practical Design-Oriented Questions

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***Abstract*—This report consolidates the solutions for three practical DSP design tasks: (Q1) a two-stage polyphase Sample-Rate Converter (96 kHz → 44.1 kHz); (Q2) an Fx-LMS adaptive Active Noise Cancellation (ANC) headset targeted for non-stationary road noise; and (Q3) a baseband receiver chain for 64-QAM OFDM (20 MHz, 64-subcarrier, CP=16). Each section presents the design philosophy, specification mapping, key results, complexity/implementation considerations.**

I. Overview and Method

For each problem we: (1) restated the specification succinctly; (2) reviewed the literature given for each question to understand the algorithm/architecture each question demands; (3) implemented solutions for each questions based on the understanding gotten from the literature and intensive review of a couple of sample projects on github; (4) evaluated performance of each system based on the question's demands.

Each question has a detailed report of it's own the various plots and performance details which are also provided in the submission bundle together with the code in the same repository.

The following sections summarise each task and show how the chosen designs satisfy the stated specs.

II. Q1: Two-Stage Polyphase SRC (96 kHz → 44.1 kHz)

A. Specs and design goal

Pass-band ripple ≤ 0.01 dB, stop-band attenuation ≥ 100 dB, computational budget ≤ 1 G MAC/s on a 200 MHz ARM-A55. Goal: produce an efficient two-stage polyphase converter with validated filter responses and complexity accounting.

B. Architecture choice and rationale

We factor the rational rate

$$\frac{44100}{96000} = \frac{147}{320}$$

into integer stages to relax transition widths per stage and enable polyphase acceleration. A practical choice is

$$\frac{147}{320} = \frac{21}{20} \times \frac{7}{16},$$

which yields an intermediate sampling rate of $f_1 = 96\text{k} \times 21/20 = 100.8\text{kHz}$ and final 44.1kHz. This cascade reduces peak filter orders compared to a single 147/320 stage while allowing efficient polyphase implementations that compute only necessary phases per output sample.

C. Filter design summary

Design method: Kaiser and Parks–McClellan (equiripple) designs were used iteratively with numerical verification by FFT:

- Stage 1: anti-alias/anti-image lowpass at f_1 with passband up to 20 kHz and a controlled transition region placed to avoid imaging into the audio band.
- Stage 2: sharper lowpass near the final Nyquist (22.05 kHz) to enforce the $\geq$100 dB stop-band criterion.

Exact filter lengths (computed by the attached scripts using the specified ripple/attenuation targets and precise normalized transition widths) are provided in the deliverables. The design flow enforces the spec by iterating transition width and window/remez parameters until both ripple and attenuation targets are met.

D. Polyphase efficiency and complexity

Polyphase decomposition is applied to each stage: for interpolation by L and decimation by M the MACs per *output* sample are approximately reduced from N to $\approx N/L$ (interpolator) or $\approx N/M$ (decimator) depending on implementation point. Using the measured filter lengths, the two-stage polyphase implementation yields an overall MACs/s well below the 1 G MAC/s budget on the ARM-A55 when using optimized fixed-point inner loops.

E. Numerical/fixed-point considerations

We estimate accumulator width using

$$B_a = B_s + B_c + \lceil \log_2 N_{\max} \rceil + G,$$

where G is headroom (e.g., 2 bits for a 12 dB crest factor limit). Coefficient quantization and dynamic range were simulated: 16–24 bit coefficient formats are supported; word-length choices are in the code and conservative accumulator widths are recommended for fixed-point deployment.

III. Q2: Adaptive Noise-Cancelling Headset (Fx-LMS)

A. Specs and design goal

Suppress road traffic broadband noise with $\geq$20 dB attenuation across 100–1000 Hz within 300 ms adaptation time; speech distortion $< 2\%$ (cepstral metric); target platform: constrained MIPS and 128 kB RAM; deployment on 24-bit fixed-point DSP in mind.

B. System model and algorithm choice

In line with the question's specification for the use of the Fx-LMS algorithm, we use a feedforward ANC architecture with:

$$d(k) = P(z) * \big(n(k) + s(k)\big), \qquad e(k) = d(k) - S(z) * y(k),$$

where $P(z)$ and $S(z)$ model the primary and secondary acoustic paths respectively. The adaptive filter $W(z)$ (256 taps in simulation) generates $y(k)$. Fx-LMS updates:

$$w(k+1) = w(k) + \mu(k)\, e(k)\, x_f(k),$$

with $x_f(k) = \hat{S}(z) * x(k)$ (filtered reference) and a normalized, variable step size $\mu(k)$ to guarantee stable and fast convergence. The Fx-LMS choice is justified over RLS because Fx-LMS is far more memory- and compute-efficient (linear complexity in taps), fits within 128 kB RAM for practical tap sizes and fixed-point accumulator widths, and meets the adaptation time requirement in simulation.

C. Implementation and performance

Simulation (Python/Numpy) used an 8 kHz sampling rate and a 256-tap adaptive filter. The requirement to use the CHiME-4 road-noise dataset as test input was not met because the dataset was not free, so in essence, the input signals were simulated. Results: measured broadband attenuation exceeded 20 dB in $\leq$150 ms; final measured speech distortion (cepstral metric) was 1.5%, meeting the specification. Spectrograms and attenuation-vs-time plots are included in the deliverables. The Fx-LMS loop adopts step-size normalization by instantaneous reference power and optional leakage to maintain stability in non-stationary noise.

D. Hardware mapping and quantisation

For deployment on a 24-bit fixed-point DSP we recommend:

- Coefficients quantised to 24 bits (or 16 bits with careful scaling) and accumulator widths sized per the formula in Section Q1.
- Secondary path identification ($S(z)$) performed offline or periodically during quiet intervals and stored in fixed-point form.
- Overflow detection by saturation arithmetic and occasional coefficient renormalisation to avoid long-term drift.

Detailed per-tap MAC counts and memory footprints for the selected tap lengths are reported in the Q2 memo pdf file.

IV. Q3: 64-QAM OFDM Baseband Receiver

A. Specs and design goal

Simulate a 64-subcarrier OFDM PHY in a 20 MHz band with cyclic prefix length 16 samples. Provide timing sync, CFO estimation (fractional + integer) reducing residual CFO to $< 2\%$ of subcarrier spacing, compare LS and MMSE pilot-based channel estimates, and present BER/ICI studies including mobility effects.

B. Receiver chain and algorithms

- **Timing sync:** Schmidl & Cox autocorrelation provides coarse timing; variance measured across Eb/N0 5–15 dB in simulation.
- **CFO:** Two-stage estimator — fractional estimate from long training symbol phase difference, then integer correction via pilot correlation — reduces residual CFO to negligible levels at moderate SNR.
- **Channel estimation:** Pilot-assisted LS and MMSE interpolation were implemented and compared; the MMSE method requires an accurate prior covariance (regularisation recommended).
- **Equalisation:** Per-tone ZF and MMSE equalizers were tested; MMSE is preferred in multipath/noise enhancement scenarios, while ZF is acceptable in near-flat channels.

Measured outputs included timing variance, residual CFO (in subcarrier units), MSE vs SNR for channel estimators, and uncoded BER curves versus Eb/N0; the ICI floor under Doppler (100–2000 Hz) is shown and discussed. All simulation scripts and plotted results are attached in the Q3 memo pdf file.

V. Deliverables

For each question the following accompany this consolidated report:

- **Q1:** Two MATLAB scripts for the single stage and two-stage SRC, short technical memo, and the various figure for the plots.
- **Q2:** Python(Jupyter notebook), various figures for the plots (attenuation vs time, spectrograms, etc.) and the technical memo.
- **Q3:** MATLAB script, BER/ICI plots and memo.

VI. Concluding Remarks

Although this was a tiring and challenging experience, alot was learned in the process and we are grateful for the opportunity. Each solution we presented was developed with a clear mapping from question specification to engineering choice. The supplied scripts were also written clear enough to enable easy and reproducible verification to make the assessment an easy and painless process.