XS1-L Hardware Design Checklist

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XMOS

1 Introduction

This document is intended for use by hardware designers using the XMOS XS1-L family of devices. It is a checklist of items that should be included in all XS1-L designs to ensure correct operation. For further details refer to the relevant device datasheet.

2 Checklist

Each of the following sections contains items to check for each design using an XS1-L series device.

2.1 Ground Pad

The centre ground pad for all XS1-L packages is the main device ground and must be connected to circuit ground. Multiple vias should be used from the centre pad to the circuit ground plane to minimise impedance and conduct heat away from the device.

2.2 Power supply sequencing

The VDDIO (and OTP_VDDIO if present) supply must be within specification (3.0V - 3.6V) before the VDD (core) supply is turned on. Specifically, the VDDIO supplies should be within specification before VDD core reaches 0.4V.

2.3 VDD ramp rate

The VDD (core) supply should ramp monotonically (constantly rising) from 0V to its final value (0.95V - 1.05V) within 10ms to ensure correct startup.

2.4 VDD (core) supply capability

The VDD (core) supply should be capable of supplying at least 300mA for an L1 and 600mA for an L2 device assuming they may be operating at full capacity.

2.5 Power supply decoupling

Ensure the design has multiple decoupling capacitors per supply placed close to the relevant supply pins. An example would be a minimum of 4 x 0402 or 0603 size surface mount capacitors of 100nF in value, per supply. The ground side of the decoupling capacitors should have as short a path back to the ground pins of the device (mainly the centre pad) as possible. A bulk decoupling capacitor of at least 10uF should be placed on each supply.

2.6 PLL_AVDD

A low pass filter is highly recommended on this pin to avoid noise affecting the internal PLL. An RC filter is used on the XMOS reference designs with a 1uF or 100nF ceramic capacitor and a 4.7R (L1) or 2.2R (L2) resistor. The filter (and especially the capacitor) should be placed close to the PLL_AVDD pin.

2.7 Power on reset

The RST_N and TRST_N pins must be asserted (low) during or after power up. The device should not be used until these resets have taken place.

As the errata in the datasheets show, the internal pullups on these two pins can occasionally provide stronger than normal pullup currents. For this reason, an RC type reset circuit is discouraged as behaviour would be unpredictable. A voltage supervisor type reset device is recommended to guarantee a good reset. This also has the benefit of resetting the system should the relevant supply go out of specification.

2.8 Clock input

The CLK input pin should be supplied with a clock with monotonic rising edges and low jitter levels. Note that the PCU_CLK pin (only on some packages) must also be supplied with a clock for the device to function correctly, even if the PCU is not being used. The main CLK input can be tied to the PCU_CLK input to satisfy this condition.

2.9 SPI boot

If booting the device from a SPI Flash, ensure the MODE pins are set correctly (MODE3 = 1, MODE2 = 1) and that the SPI Flash is connected to the correct ports as shown below:

Pin Name	SPI Signal	Description
X0D0	MISO	Data - Master In Slave Out
X0D1	SS	Slave Select
X0D10	SCLK	Clock
X0D11	MOSI	Data - Master Out Slave In

If code debug via JTAG is required (e.g. code development) then make sure the MODE pins are set to boot from JTAG (i.e. don't boot anything, wait to have code loaded over JTAG). This condition requires MODE3 = 0, MODE2 = 0 and can be set with a jumper or similar.

2.10 USB ULPI Mode

The XS1-L1 contains support for connecting to a USB transceiver using the UTMI+ Low Pin Interface (ULPI).

When using the XS1-L1 with ULPI, the ULPI signals must only be connected to specific ports as shown in the following table.

When using ULPI, some ports on the same core are used internally and so are not available for use by user software. These are shown greyed out in the table. The available ports are shown in green. All ports on other cores are unaffected.

Note that this limitation only applies when the ULPI is enabled, the greyed out ports can still be used before or after the ULPI is being used.

2.11 USB ULPI Port Table

Package	Ports					Signals
Pin Name	1b	4b	8b	16b	32b	
XnD0	P1A0					
XnD1	P1B0					
XnD2		P4A0	P8A0	P16A0	P32A20	Not available in ULPI mode
XnD3		P4A1	P8A1	P16A1	P32A21	
XnD4		P4B0	P8A2	P16A2	P32A22	
XnD5		P4B1	P8A3	P16A3	P32A23	
XnD6		P4B2	P8A4	P16A4	P32A24	
XnD7		P4B3	P8A5	P16A5	P32A25	
XnD8		P4A2	P8A6	P16A6	P32A26	
XnD9		P4A3	P8A7	P16A7	P32A27	
XnD10	P1C0					
XnD11	P1D0					
XnD12	P1E0					ULPI_STP
XnD13	P1F0					ULPI_NXT
XnD14		P4C0	P8B0	P16A8	P32A28	ULPI_DATA0
XnD15		P4C1	P8B1	P16A9	P32A29	ULPI_DATA1
XnD16		P4D0	P8B2	P16A10		ULPI_DATA2
XnD17		P4D1	P8B3	P16A11		ULPI_DATA3
XnD18		P4D2	P8B4	P16A12		ULPI_DATA4
XnD19		P4D3	P8B5	P16A13		ULPI_DATA5
XnD20		P4C2	P8B6	P16A14	P32A30	ULPI_DATA6
XnD21		P4C3	P8B7	P16A15	P32A31	ULPI_DATA7
XnD22	P1G0					ULPI_DIR
XnD23	P1H0					ULPI_CLK
XnD24	P1I0					
XnD25	P1J0					
XnD26		P4E0	P8C0	P16B0		Not available in ULPI mode
XnD27		P4E1	P8C1	P16B1		
X0D28		P4F0	P8C2	P16B2		
X0D29		P4F1	P8C3	P16B3		
X0D30		P4F2	P8C4	P16B4		
X0D31		P4F3	P8C5	P16B5		
XnD32		P4E2	P8C6	P16B6		
XnD33		P4E3	P8C7	P16B7		
XnD34	P1K0					
XnD35	P1L0					
XnD36	P1M0		P8D0	P16B8		
XnD37	P1N0		P8D1	P16B9		Not Available in ULPI mode
XnD38	P1O0		P8D2	P16B10		
XnD39	P1P0		P8D3	P16B11		
XnD40			P8D4	P16B12		
XnD41			P8D5	P16B13		
XnD42			P8D6	P16B14		
XnD43			P8D7	P16B15		
XnD49 - XnD70					P32A[19:0]	

3 Device Configuration

Example XS1-L designs including schematics and layouts can be found on the XMOS website at: http://xmos.com/support/silicon

4 Related Documents

Information about XMOS technology is primarily available from the XMOS website; please see http://xmos.com/documentation for the latest documents or click on one of the links below to find out more information.

Document	Document reference
XS1-L1 48TQFP Datasheet	xs1-l1-48tqfp-datasheet
XS1-L1 64LQFP Datasheet	xs1-l1-64lqfp-datasheet
XS1-L1 128TQFP Datasheet	xs1-l1-128tqfp-datasheet
XS1-L2 124QFN Datasheet	xs1-l2-124qfn-datasheet
XS1-L System Specification	xsysteml
XS1-L Clock Frequency Control Application Note	xs1l_clk
XS1 Port I/O Timing Application Note	xs1_port_timing
XS1-L Link Performance and Design Guidelines	xs1l_links
Estimating Power Consumption For XS1-L Devices	xs1l_power
Device Package User Guide	package_user_guide

5 Document History

Date	Release	Comment
2010-04-20	1.0	First release
2010-04-22	1.1	Added ULPI interface information
2011-04-26	1.2	Added XS1-L1-48TQFP & Device Package User Guide Links
2011-06-06	1.3	Added ground pad requirements