Design of a 4 MHz, 5V to 1V Monolithic Voltage Regulator Chip

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***Abstract*-- A versatile two-phase-monolithic voltage regulator (MVR) chip has been developed and fabricated using traditional 0.5micron CMOS technology. The chip is designed to work at up to 4Mhz and 5V to 1V power conversion with good efficiency. In this paper, the author will discuss some major design issues of this MVR chip, including the benefits and limitations of the sub micron CMOS technology in this kind of all in one power conversion application.**

I. INTRUDUCTION

With the drastic-changing of computer microprocessor technology, the requirement for its voltage regulator has become a big challenge for circuit design engineers. According to the newest Intel power road map [1], processors requiring 1V and 100~130A will be on the market in two to four years and the power can only be provided by multiphase, high frequency (3 MHz at minimum) voltage regulator to meet its even tighter transient requirement. Based on present power delivering scheme which separates the microprocessor and the on motherboard voltage regulator (VR) as shown in Figure 1 [2], one also has to encounter the bottle neck of the socket interconnection, whose parasitic inductance will ultimately slow down the whole transient response that a voltage regulator can provide. Further more, the one milliohm interconnect resistance will count for more than 10% power loss for future generation microprocessor.

One way to break through this bottleneck is the hybrid-integration of microprocessor with the voltage regulator into one package as show in Figure 2. In order to so, the output inductor has to be physically small enough to suit the integration, meanwhile, the output capacitors also need to be small.

All these lead to a higher switching frequency requirement, which also has the benefits of higher control bandwidth and better transient performance. However, higher switching frequency also means shorter switch transition time. The 20-40 nanoseconds transition period currently used in VRs may no longer be acceptable once the frequency reaches above four mega-hertz. On the other hand, the parasitic inductances of a discrete device (typically Ls, Ld are about 1nH and Lg about 2nH for SO8 Package) start to play a detrimental roll as the transition time becomes shorter.

This work is funded by NSF Career -Award EEC-9731677, SRC consortium, CPES VRM consortium and NSF ERC program.

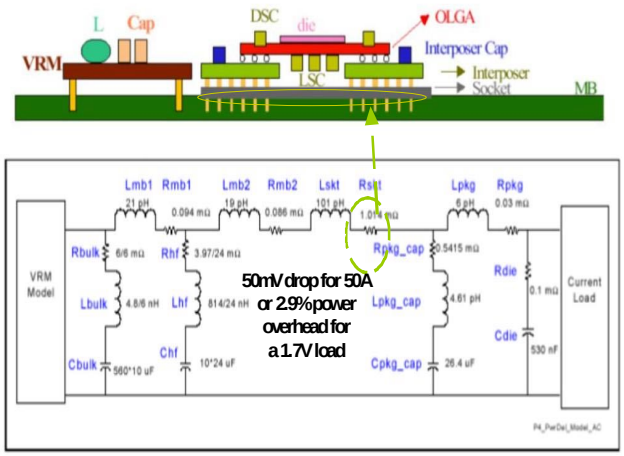

Figure 1. Power distribution model of on board voltage regulator. [2], for future microprocessor of 1V, 120 A, the loss due to socket inter-connecter will be over 10%.

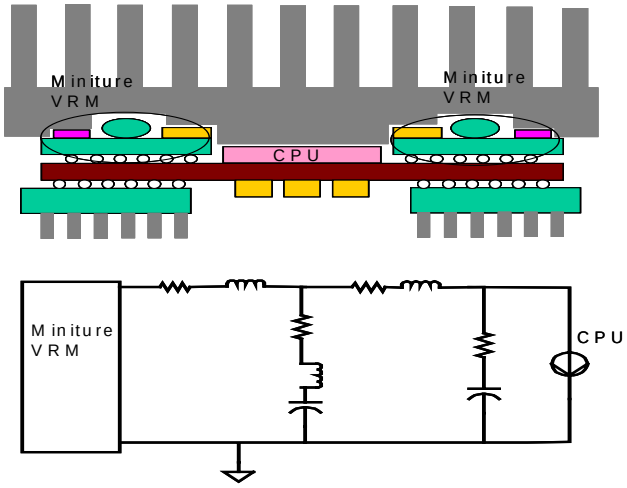

Figure 2. Power distribution model with voltage regulator packaged with microprocessor. The socket bottleneck has been drastically reduced.

In a normal synchronous buck configuration (Figure 3), the combination of Ls and Ld will generate a large voltage spike, therefore higher stress, because of extremely high di/dt for the top switch when it is turned off (Figure 4). Similarly, the existence of Lg of the synchronous switch may undesirably cause it to turn on due to high dV/dt at the turn-on of the top switch, which may cause shoot through.

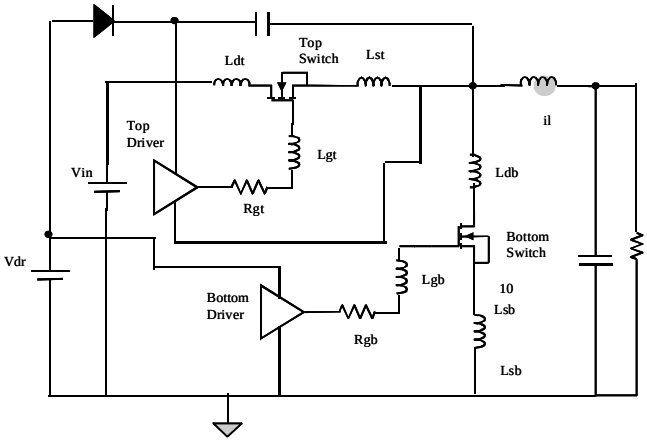

Figure 3. Schematics of a typical synchronous buck circuit with bootstrap driver

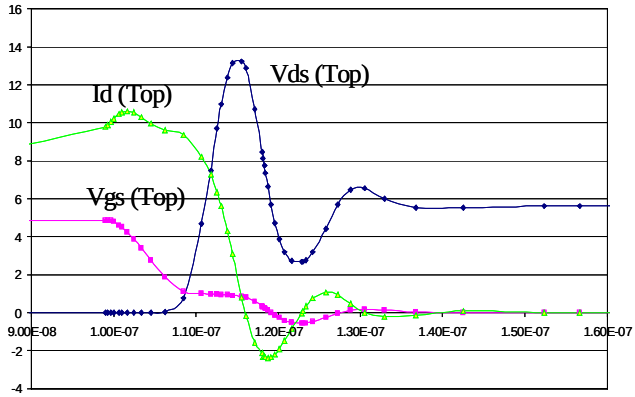

Figure 4. Simulated top switch voltage stress for typical trench MOSFET in SO8 packaging

Even with the improvement of single chip packaging, (e.g. using metal-strip SO8 instead of wire-bond SO8, the parasitic values can be reduced by about 30%, which are expected to decrease further as the DirectFET technology from International Rectifiers Inc. is used [3]), the separation of power switch from its driver still exists. Further integration is needed. Compared to the hybrid approach such as iP2001 module (still wire-bond inside) from International Rectifier [4], the monolithic integration can further shorten the interconnection between different functional modules.

II. MONOLITHIC VOLTAGE REGULATOR CHIP

As a proposed solution to the aforementioned issues, a two-phase monolithic voltage regulator (MVR) chip (Figure 5) is developed based on a 0.5-µm three metal digital CMOS process. The MVR chip includes a two-phase PWM controller, four power switches and their drivers. The functional block diagram of this all-in-one power chip is shown in Figure 6.

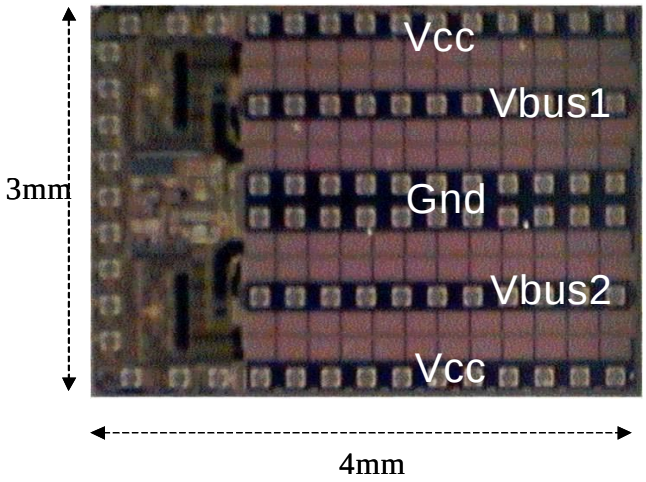

Figure 5. Top view of two-channel all-in-one power regulator chip using 0.5 µm CMOS process

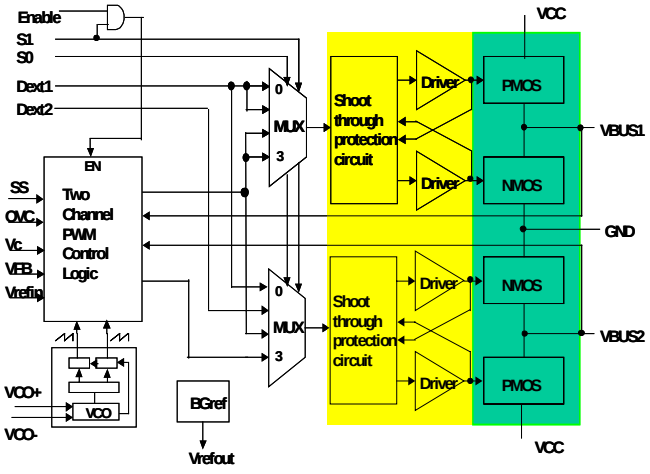

Figure 6. Functional block diagrams for the monolithic two-channel all-in-one power chip

This functional MVR chip has four working modes, namely, one-phase with external drive signal, two-phase with external drive signal, one-phase with internal drive signal and two-phase with internal drive signal. When the functional select pin S1 is connected to the ground, the chip is using external control, while the on chip PWM core being totally shut down with little or no extra power loss. The chip can be used as the power stage in a multi-phase step down converter. Once the S1 pin is connected to the VDD, the chip can be used as a self-sufficient power module, only need to add other passive components. By interleaving the two on chip channels (set S0 pin high), one can also take the advantage of the AC flux cancellation when the two output inductances are coupled into an E-I core [5].

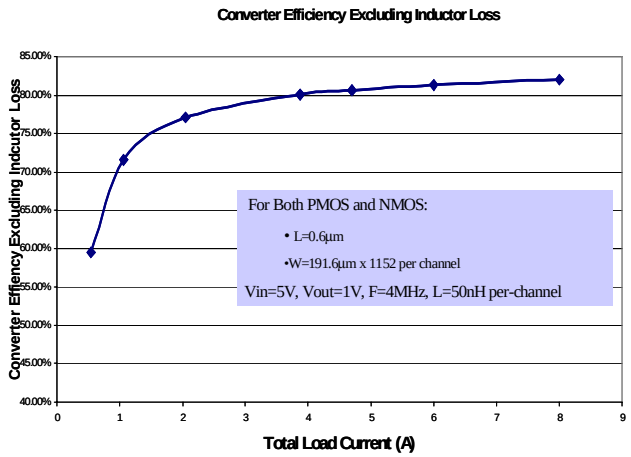

Figure 7. Converter efficiency excluding the loss due to inductor which is about another 1~2 percent based on critical inductance design [6]

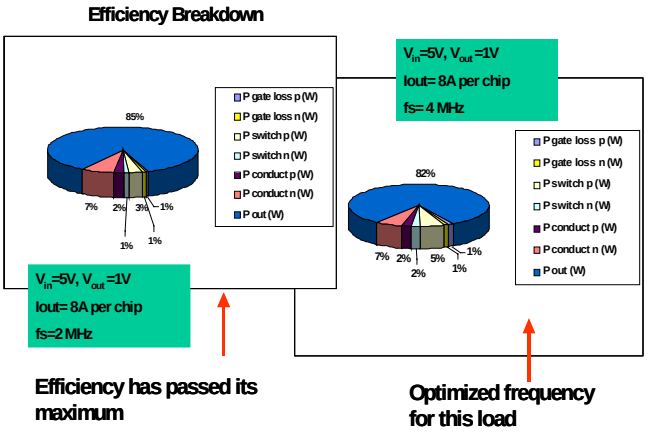

Figure 8 Loss break down at different frequency

The main electrical parameters of the power switches are summarized in Table 1 and the typical full load efficiency and loss break down based on Hspice simulation results are shown in Figure 7 and Figure 8.

Although this chip is designed for up to 8A output current (purely for conceptual demonstration purpose) and 3.5~5V to 1~1.5V conversion, the basic electrical parameters are scalable as long as the die level BGA flip chip packaging is followed. For larger output current rating, the efficiency will not degrade drastically once the chip size was scaled up accordingly based on the following discussion on the device sizing and their effects on the converter efficiency.

III. CHIP DESIGN CONSIDERATIONS

As in many other ASIC designs, the optimization for the specific application is also the major concern in this chip design, namely, the sizing of the power MOSFET and the speed of its driver to achieve ultimate efficiency at the full load and the targeting switching frequency.

Table 1. Main electrical parameter for the power switches used in the all-in-one power IC chip

Single Channel Parameters (V_{in}=5V, V_{out}=1V, V_f=0.6V)	**Bottom NMOS**	**Top PMOS**
W (cm)	22	22
L (um)	0.6	0.6
R_{dson} (mΩ)	18	30
Q_g ($\|V_{gs}\|$=5V) (nC)	1.93	1.95
Q_{gs1}($\|V_{gs1}\|$) (nC)	0.23 (0.9V)	0.29 (1.1V)
Q_{gth}($\|V_{gs}$) (nC)	0.17 (0.7V)	0.23 (0.9V)
Q_{gd}($\|V_{ds}\|$=5 to 0V) (nC)	0.3	0.3
Q_{rec} ($\|V_{ds}\|$ =-0.6 to 5 V) (nC) (mainly due to output cap)	2	
Figure of Merit1 (FOM1)= R_{dson}×(Q_g+Q_{gd}+Q_{gs1}-Q_{gth})		69.4 nCmΩ
Figure of Merit2 (FOM2)= R_{dson}×(Q_g-Q_{gd}+Q_{rec})	64.8 nCmΩ	
Technology Determined Specific Parameters		
R_{on_spec} (mΩ cm)	396	660
$C_{iss\_off\_spec}$ (pF/cm)	10.9	11.6
$C_{iss\_on\_spec}$ (pF/cm)	15.5	15.8
$C_{gd\_eff\_spec}$ (pF/cm)	2.73 (0-5V)	2.73 (0-5V)
$C_{oss\_eff\_spec}$ (pF/cm)	17 (-0.6-5V)	14.5 (0-5V)

Note:

(1) The R_{dson} has included the metal trace de-biasing effect and packaging contribution.

(2) The specific parameters are calculated as the following

$$R_{on\_spec} = R_{dson} \cdot W$$

$$C_{iss\_off\_spec} = \frac{Q_{gs1}}{V_{gs1} \cdot W}$$

$$C_{iss\_on\_spec} = \frac{Q_g - Q_{gs1} - Q_{gd}}{(Vg - Vgs1) \cdot W}$$

$$C_{gd\_eff\_spec} = \frac{Q_{gd}}{Vin \cdot W}$$

$$C_{oss\_eff\_spec} = \frac{\int_{V_{min}}^{V_{max}} C_{oss}\, dV}{(V_{max} - V_{min}) \cdot W}$$

where V_{gs1} is the plateau gate voltage while V_{ds} changing, V_{max}=V_{in} and V_{min}=0 for PMOS and –V_f for NMOS.

(3) Due to the strong sub-threshold current component during the body diode conducting and the barrier lowering effect, the diode reverse recovery storage charge is significantly reduced, only the junction capacitor playing the major role.

The loss on the power MOSFET can be categorized into two parts, one as the frequency independent conduction loss, which is inversely proportional to its total width, and the other as the frequency related loss, which is proportional to its total width. For certain device technology, there exists an optimal size (width) of the MOSFET such that at certain switching frequency and certain load current, the loss on the MOSFET reaches its minimum. As a result, the converter reaches to its optimum efficiency [7], which is not only determined by the specific electrical parameters of the device technology as shown in Table 1, but also by the circuit parameters such as, input/output voltage V_{in}/V_{out}, driver voltage V_g, driver capability, which directly related to the gate resistance R_g, load current, switching frequency f and so on.

For the bottom synchronous switch, it is desirable to limit the body diode conduction portion (d_{on} and d_{off}) to minimum without causing shoot through. Let

$$D = \frac{V_{out}}{V_{in}} \tag{1}$$

$$I_{rms} = \frac{1}{\sqrt{3}} \cdot \left(I_{max}^{\,2} + I_{max} \cdot I_{min} + I_{min}^{\,2} \right)^{\frac{1}{2}} \tag{2}$$

$$I_{avg} = \frac{1}{2} \cdot \left(I_{max} + I_{min} \right) \tag{3}$$

where the I_{max} and I_{min} are the peak and valley current of the out put inductor, which can be determined based on the critical inductance design [6].

By scaling the itemized loss according to the output power, we can further define the effective specific on resistance and the input and output capacitor for the bottom switch as the following equations (4-6), with V_f as the body diode forward drop:

$$R_{on\_N\_spec\_eff} = \left(1 - D - d_{on} - d_{off}\right) \cdot \frac{I_{rms}^{\,2}}{I_{avg}^{\,2}} \cdot R_{on\_N\_spec} \tag{4}$$

$$C_{iss\_N\_spec\_eff} = C_{iss\_off\_N\_spec} \cdot \left(\frac{V_{TN}}{V_{out}} \right)^2 + C_{iss\_on\_N\_spec} \cdot \left(\frac{V_g - V_{TN}}{V_{out}} \right)^2 \tag{5}$$

$$C_{oss\_N\_spec\_eff} = \frac{1}{2} \cdot C_{oss\_eff\_N\_spec} \cdot \left(\frac{1}{D} + \frac{V_f}{V_{out}} \right)^2 \tag{6}$$

where the V_{TN} is $V_{tn}+I_{ds}/g_{mn}$. In many cases, g_{mn} is large enough so that V_{tn} can be used instead. $R_{on\_N\_spec\_eff}$ is related to the bottom switching conduction loss while $C_{iss\_N\_spec\_eff}$ is related to the bottom switch gate drive loss and $C_{oss\_N\_spec\_eff}$ to the body diode reverse recovery. A new figure of merit τ_N can be introduced as the following to replace FOM2 in Table 1 to account the circuit contribution.

$$\tau_N = R_{on\_N\_spec\_eff} \cdot \left(C_{iss\_N\_spec\_eff} + C_{oss\_N\_spec\_eff} \right) \tag{7}$$

Further more, when the width of the bottom switch reaches to its optimal value as in equation (8), its loss is minimized.

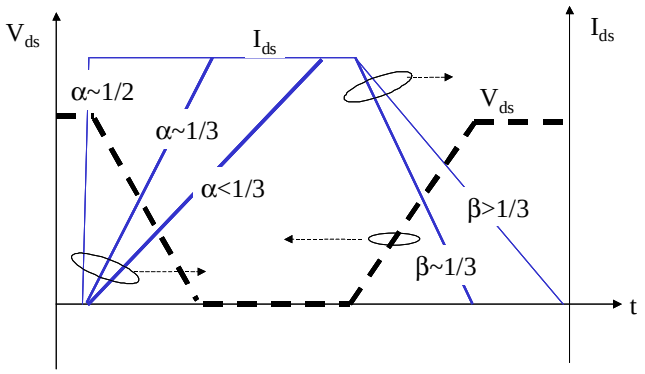

Figure 9. Typical I_{ds} vs V_{ds} cross over curve for top switch

$$W_{N\_opt} = \left[\frac{I_{avg}^{\,2} \cdot R_{on\_N\_spec\_eff}}{\left(C_{iss\_N\_spec\_eff} + C_{oss\_N\_spec\_eff} \right) \cdot V_{out}^{\,2} \cdot f} \right]^{\frac{1}{2}} \tag{8}$$

Therefore, we can define the percentage of power overhead due to the body diode conduction (Γ_{diode_cond}) and that of the bottom switch overall loss (Γ_N) as the following:

$$\Gamma_{diode\_cond} = \frac{P_{diode\_cond}}{P_{out}} = \frac{\left(I_{max} \cdot d_{on} + I_{min} \cdot d_{off} \right)}{I_{avg}} \cdot \frac{V_f}{V_{out}} \tag{9}$$

$$\Gamma_N = \frac{P_{loss\_N\_min}}{P_{out}} = 2\sqrt{\tau_N \cdot f} + \Gamma_{diode\_cond} \tag{10}$$

Similarly, we can define the effective specific on resistance and the input, output and miller capacitor for the top switch as well:

$$R_{on\_.P\_spec\_eff} = D \cdot \frac{I_{rms}^{\,2}}{I_{avg}^{\,2}} \cdot R_{on\_P\_spec} \tag{11}$$

$$C_{iss\_P\_spec\_eff} = C_{iss\_off\_P\_spec} \cdot \left(\frac{V_{TP}}{V_{out}} \right)^2 + C_{iss\_on\_P\_spec} \cdot \left(\frac{V_g - V_{TP}}{V_{out}} \right)^2 \tag{12}$$

$$C_{oss\_P\_spec\_eff} = \frac{1}{2} \cdot \frac{C_{oss\_eff\_P\_spec}}{D^2} \tag{13}$$

$$C_{rss\_P\_spec\_eff} = \left(\frac{\alpha \cdot I_{min}}{\frac{V_g - V_{TP}}{R_{gP}}} + \frac{\beta \cdot I_{max}}{\frac{V_{TP}}{R_{gP}}} \right) \cdot \frac{C_{gd\_eff\_P\_spec}}{D^2} \tag{14}$$

where $R_{on\_P\_spec\_eff}$ is related to the top switching conduction loss while $C_{iss\_Pspec\_eff}$ is related to the top switch gate drive loss, $C_{oss\_N\_spec\_eff}$ to the output capacitor loss and $C_{rss\_N\_spec\_eff}$ related to the switching crossover loss. The α and β are the integral coefficient constants determined by the actual shape of the I-V crossover during turn on and off respectively as shown in Figure 9. Typically, $0< \alpha<1$ and $0< \beta<1$. They can be quite small if soft switching schemes

are used, while in hard switching cases, they can reach 1/3 and larger.

Similar to τ_N, another time constant τ_P can be used as a new figure of merit to substitute the FOM1 in Table 1, with τ_P defined as the following,

$$\tau_P = R_{on\_P\_spec\_eff}\left(C_{iss\_P\_spec\_eff} + C_{oss\_P\_spec\_eff} + C_{rss\_P\_spec\_eff}\right) \quad (15)$$

We can also get the optimal width for the top switch as:

$$W_{P\_opt} = \left[\frac{I_{avg}^{2}\cdot R_{on\_P\_spec\_eff}}{\left(C_{iss\_P\_spec\_eff} + C_{oss\_P\_spec\_eff} + C_{rss\_P\_spec\_eff}\right)\cdot V_{out}^{2}\cdot f}\right]^{\frac{1}{2}} \quad (16)$$

With same token, the power overhead due to the top switch loss is:

$$\Gamma_P = \frac{P_{loss\_P\_min}}{P_{out}} = 2\sqrt{\tau_P \cdot f} \quad (17)$$

Consequently, the maximum converter efficiency excluding the inductor magnetic loss can be estimated by:

$$\eta_{max} = \frac{1}{1 + \Gamma_N + \Gamma_P} \quad (18)$$

or, more specifically,

$$\eta_{max} = \frac{1}{1 + 2\left(\sqrt{\tau_N} + \sqrt{\tau_P}\right)\cdot\sqrt{f} + \Gamma_{diode\_cond}} \quad (19)$$

Figure 10 shows the idealized maximum efficiency that a typical half-micron technology can achieve under hard switching condition, when both top and bottom switches are optimized as shown in Figure 11.

IV. POWER MOSFET STRESS AND THE LIMITATION OF THE SUB-MICRON DIGITAL PROCESS

The above discussion of the device optimization has neglected one important portion — the contribution of the parasitic inductance, which will cause larger V_{ds} and V_{gs} voltage spike during the switching transition period, resulting not only a larger switching therefore frequency related loss but also an increased device stress which will ultimately limit the transition speed and the application of the device.

A 3D Maxwell simulation has extracted about 0.5nH parasitic inductances due to the metal trace (C to D, or E to F) in our demo board with flip chip packaging as shown in Figure 12. With the extra 1nH ESL of the high frequency ceramic capacitor taken into account, the Hpsice simulation results (Figure 13 and 14) show very little safety margin left as compared to the typical CMOS SOA as shown in Figure 15.

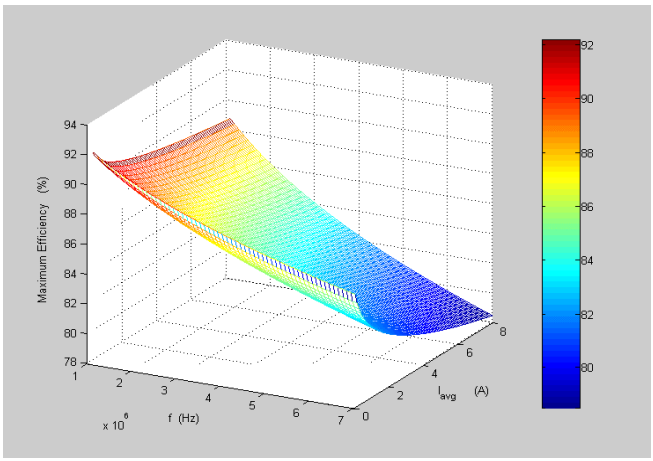

Figure 10. Maximum efficiency under ideal condition with 5V to 1V conversion. Here assuming R_{gp} inversely proportional to the square root of I_{avg}.

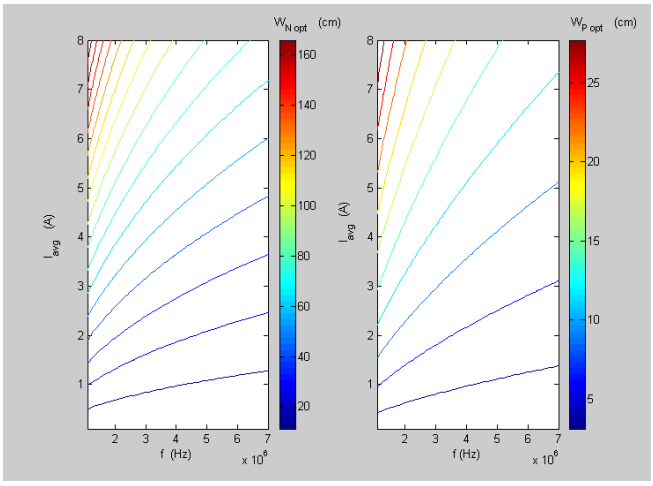

Figure 11. Calculated optimal width for bottom (left) and top (right) switches based on ideal condition with 5V to 1V conversion.

In order to fully take advantage of the benefit from the sub-micron CMOS technology, the die level flip-chip packaging is essential, while the input high frequency ceramic capacitor need to be put as close to the chip as possible. An extra on die capacitor (1.1 nF per extra 0.5mm^2 area) may also be very helpful to reduce the stress.

V. APPLICATION PROSPECT

Although most current voltage regulator uses 12V input voltage instead of 5V, a new trend is also emerging in which transformer is used in two stage topology instead of one stage step down, e.g. from 48 V bus to 5V or less then from 5V or less to about 1V [8]. This approach can help to solve the poor efficiency problem existing in most single 12V one step down conversion in multi-mega-hertz due to larger

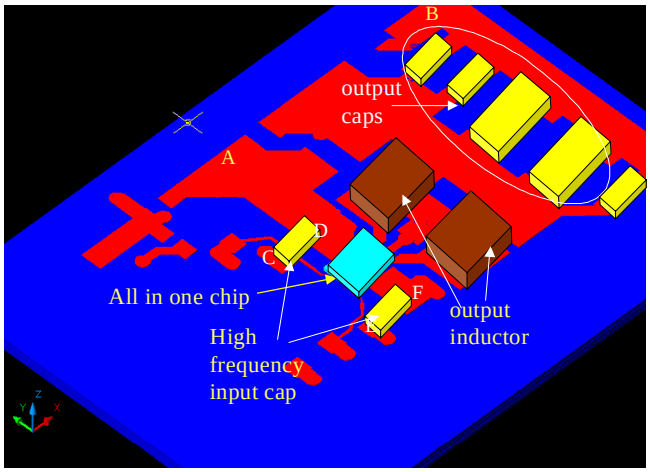

Figure 12. Simplified all-in-one demo board layout.

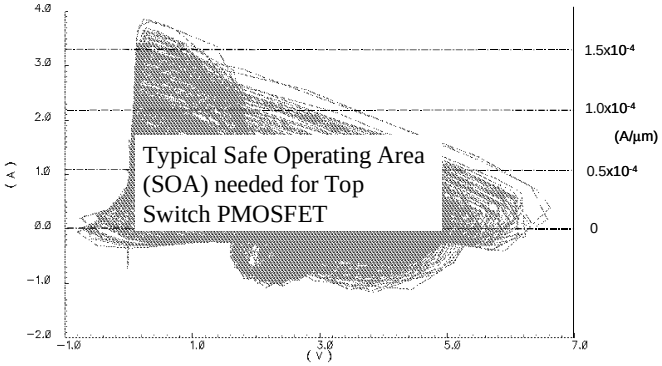

Figure 13. Hspice simulated SOA needed for the top PMOSFET, under 3.5 V to 1.2 V, 3A conversion including start up.

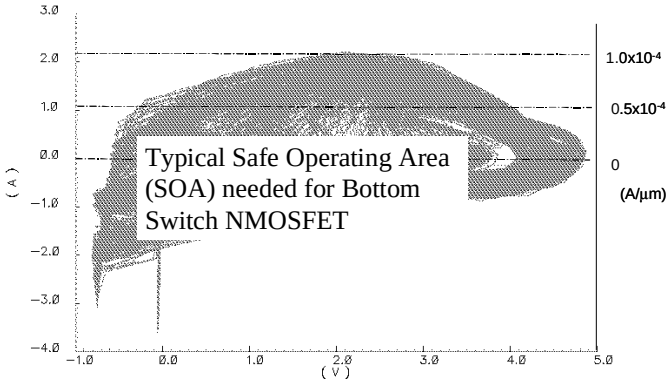

Figure 14. Hspice simulated SOA needed for the bottom NMOSFET, under 3.5 V to 1.2 V, 3A conversion including start up.

switching loss and gate drive loss. Therefore, the demonstrated 5V to 1V monolithic all-in-one MVR chip is a good candidate for this application. Furthermore, with the controller integrated together with the power stage, each chip can be used to build a stand alone voltage regulator, which can provide one more degree of freedom if multi-voltage levels are needed from different functional blocks

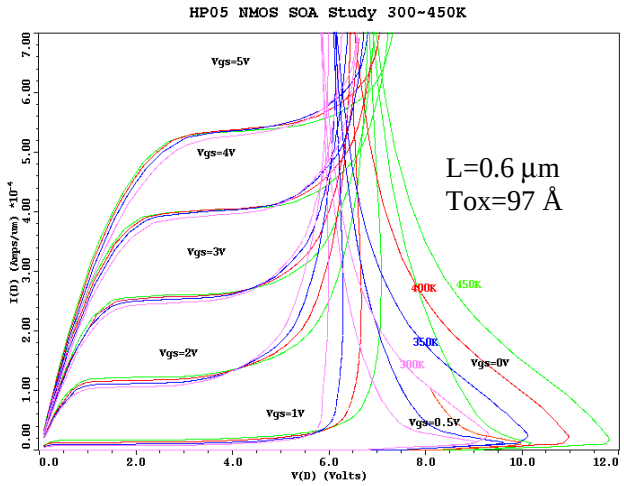

Figure 15. Typical SOA curve for half micron technology based on Medici™ simulation.

on one microprocessor. Each single MVR chip based miniature voltage regulator can deliver the power individually and cause less trouble in current sharing among the channels.

VI. CONCLUSION

A two-channel monolithic voltage regulator is developed based on half-micron digital CMOS process. The detailed power device optimization has been discussed. Two new figure of merit τ_N and τ_P are introduced, which contain not only the device technology based information but also are weighed by the actually circuit working condition. The power device stress has also been studied including discussions about the limitation of the sub-micron digital CMOS process and its application prospect.

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