



$mem\_wr = 1$  in state 1, 2, 3, 4  
 $mem\_rd = 1$  in state 6, 7, 8, 9  
 $comp = 1$  in state 0, 9  
 $stall = 1$  in 1, 2, 3, 4, 5, 6, 7, 8  
 $cache\_hit = 1$  if state 0 & hit

$cache\_wr = 1$  in 1, 2, 3, 4

I'm not sure this is correct, but I think it is  
 a good starting point. During implementation, I  
 think I will better understand state diagram