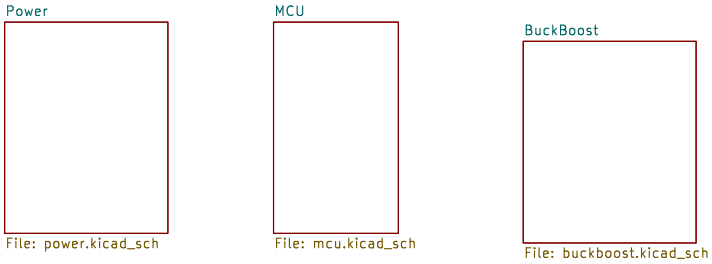

Sheet: /
File: JPBms2.kicad_sch

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Size: A4	Date:	**Rev:**
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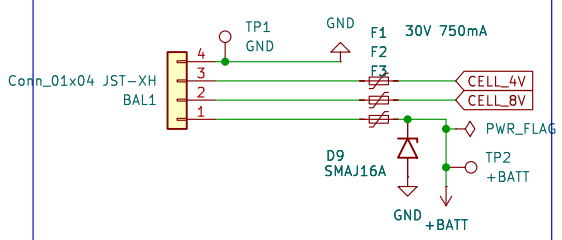
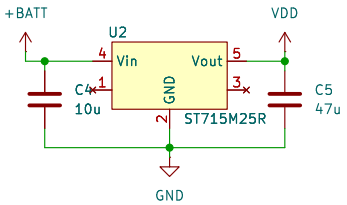
TVS diode is needed, because if you unplug the battery while the circuit is charging, the voltage can spike since nothing is there to absorb the load, damaging the multiplexer and other parts

Battery Balance Connector

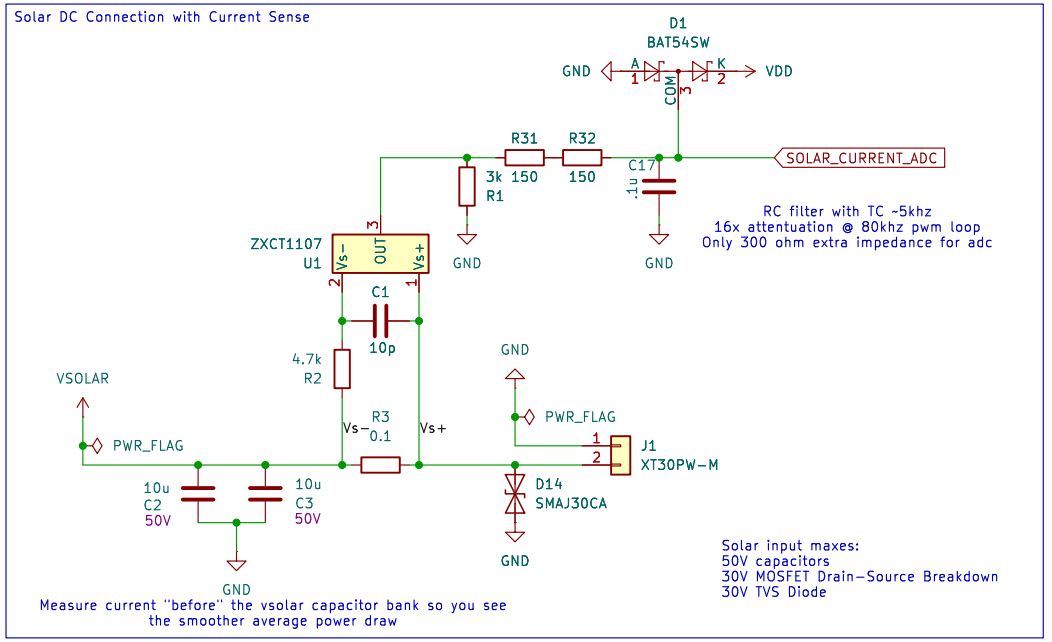


2.5V Regulator

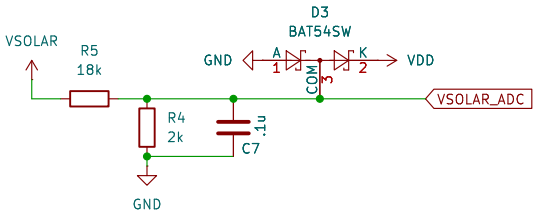


Rsense = .1 ohm, @ 2 amps = 0.2V
(Recommended for full range is 0.5V drop, but that's wasteful)
Iout = 0.004 * Vsense
so 3000 * .004*.2 = 2.4V @ 2 amps current

Solar DC Connection with Current Sense



VSolar ADC



25V*(2000/(20000))=2.5V
25V/20000ohms = 1.25mA current draw
~30mW power dissipation

1.8kohm Thevenin impedance

~1khz RC constant filter

Should sample in 12.5 cycles @16mhz adc.

Sheet: /Power/
File: power.kicad_sch

Title:

Size: A4	Date:	**Rev:**
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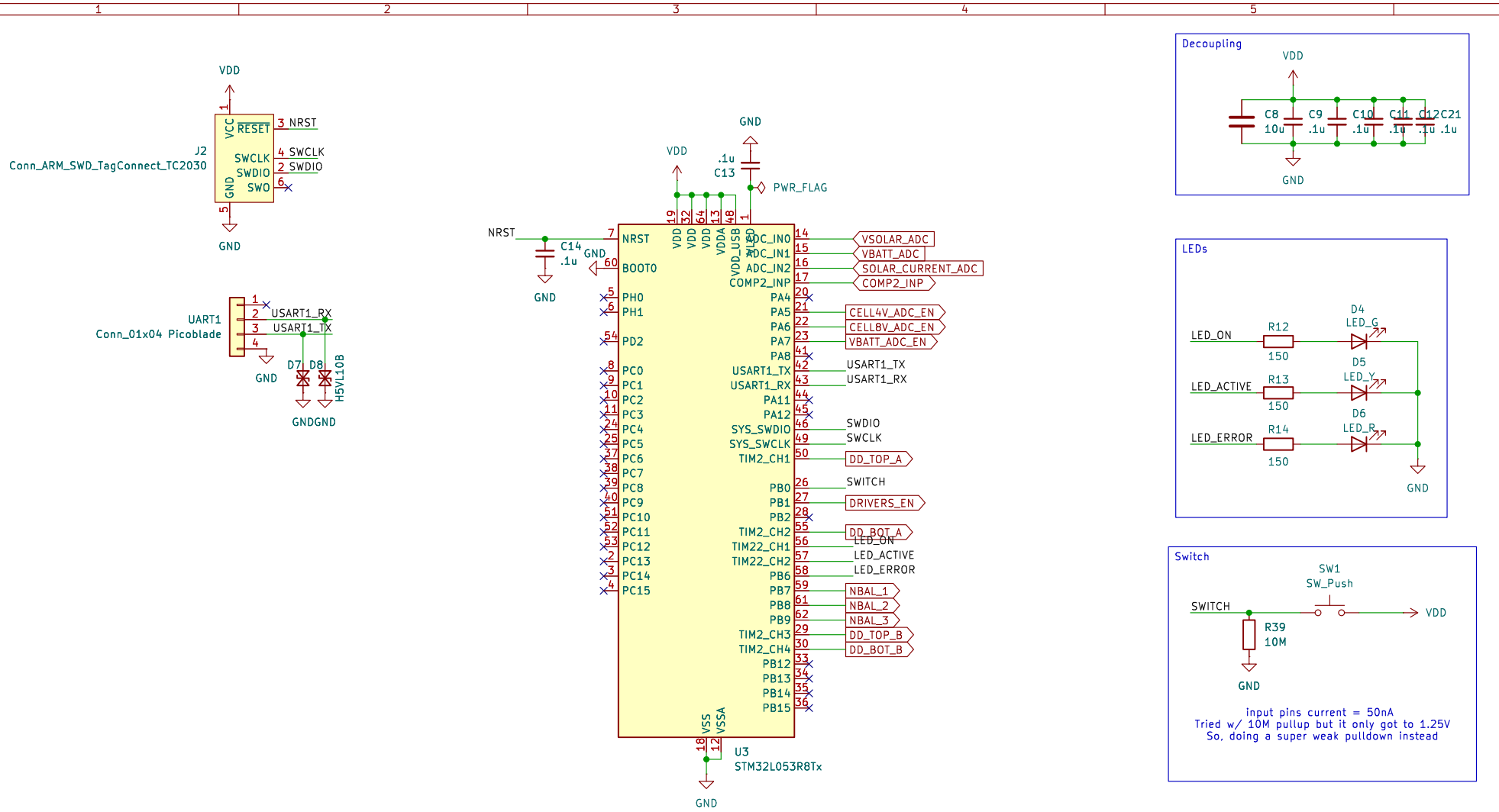
and there



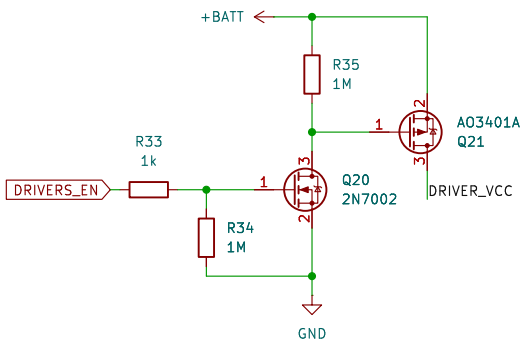
Sheet: /MCU/
File: mcu.kicad_sch

Title:

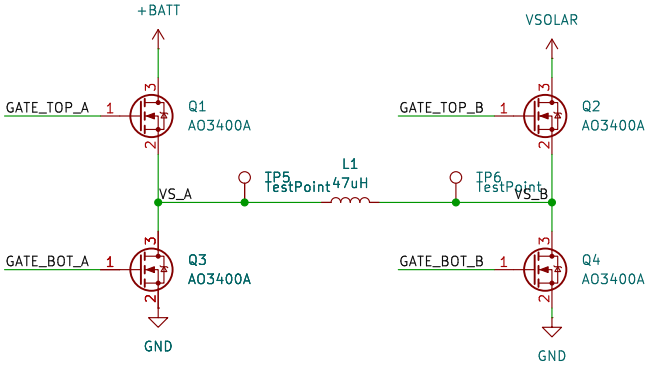
Size: A4 | Date: | **Rev:**
KiCad E.D.A. 8.0.3 | Id: 3/6

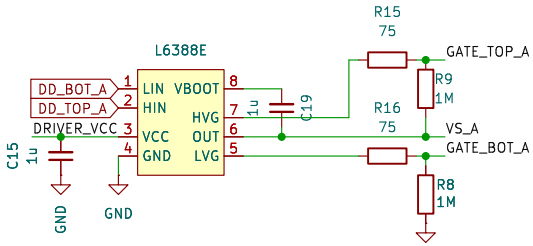
Originally, I wanted to avoid the bootstrap circuit and use PFETs on the top side.
But the IRS2003 has a dead-zone prevention, and since the PFETs are on
when the gate is GND, it wouldn't work logically.

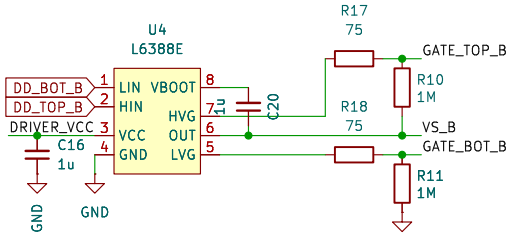
Also, the bootstrap works not as a "voltage doubler", but by adding Vbatt
to the source voltage of the top mosfet. Since Vbatt is around 12V
we'll always get a well-turned on mosfet.

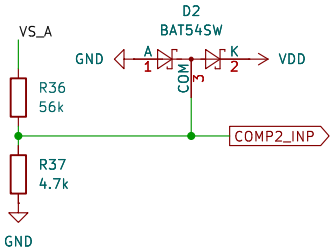


Inductor sizing:
Assume an 80khz pwm cycle.
We know we have a roughly 20V charging voltage
12V discharging voltage.
Need around 60uH for BCM operation









Vrefint = 1.224V
We want the comparator to trigger when VS_A is
just below the 16V TDS voltage.
15.8V * (4700/(56000+4700)) = 1.224

Cboot sizing:
AO3400A Gate Charge = 7nC max
Cext = 7nC / (12V Vbatt) = 600pF
Cboot >> Cext
Cboot = 1000nF

Sheet: /BuckBoost/
File: buckboost.kicad_sch

Title:

Size: A4	Date:	**Rev:**
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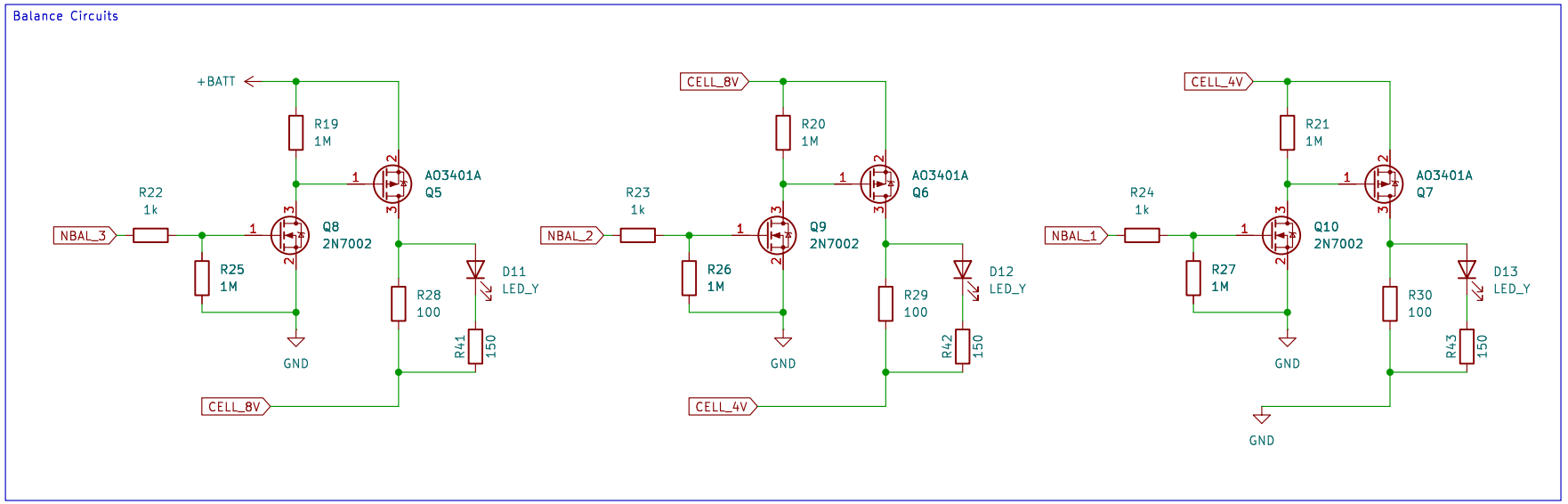

Sheet: /Balance/
File: balance.kicad_sch

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Size: A4	Date:	**Rev:**
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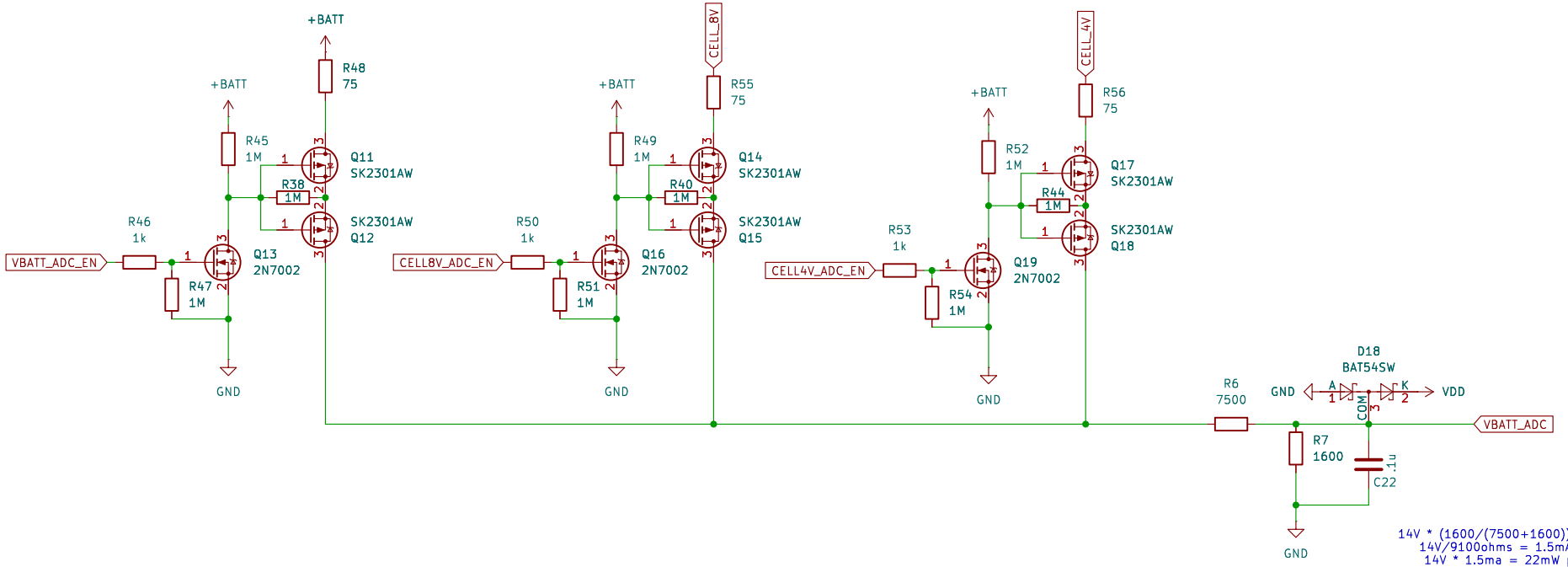
Multiplex any of the cell voltages to a single voltage divider and ADC pin
This makes it possible to get a really good comparison as long as the ADC is linear
75 ohm resistor to prevent large currents



14V * (1600/(7500+1600)) = 2.46V
14V/9100ohms = 1.5mA draw
14V * 1.5ma = 22mW power

1320 ohm Thevenin impedance
~1200Hz RC filter

You want ~1/6 ratio so that 12V comes to around 2V.
1.5kohm max total impedance, because you are sampling frequently
(Impedance goes to charge ~20pf adc capacitor, so that takes time, limiting sampling rate)
(Also, at 80khz sampling rate, you have ~4uA current, to charge the 20pf capacitor, leading to voltage drop)

Sheet: /ADC/		
File: adc.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.3		Id: 6/6