Remove this section

As per syllabus, we need to ensure the following:

- Don't Plagiarize (Only one of us will turn in the paper electronically). Perhaps we will both need printed form submissions? *Tables and Figures not required for electronic submission
- 15 Pages of text which does not include:
  - Cover Page, Table of Contents, List of Tables, List of figures (intro stuff)
  - Conclusion
  - References
  - Bibliography
  - Tables. Possibly tables and figures as the syllabus may be in error here.
- 11 Point font
- Double spaced, with Triple spacing after headings
- Margins: 1.5" left, 1" top right bottom (binding standard)
- Format:
  - Cover Page: title, abstract, course name and number, date
  - Table of Contents: page numbers for major headings
  - List of Tables: page numbers w/ captions
  - List of Figures: Page numbers w/ captions
  - Intro
  - Body w/ figures and tables
  - conclusion
  - references
  - bibliography
  - tables presented in order together
  - figures presented in order together
- "Typical Errors"
  - Did not reference sources in text/tables/figures
  - margins are wrong, spacing and triple spacing
  - grammar / spelling
  - did not follow format

Data Flow Architecture: Benefits, Limitations and Future Applications

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EEE285 - Micro-Computer System Design I

INSERT/ACTUAL/DATE

Abstract

Very little explanation is required to describe why the most prolific technology trends throughout history become so popular; from the adoption of Cloud-based data storage[1], to the micro-service architecture that supports 85% of large organizations worldwide[2], the most popular technological advances are those which provide a clear path to profit, and a user-friendly method for implementing the technology. Currently, the next ubiquitous technological advance is artificial intelligence (AI), and its ability to solve even the most complex problems through sheer brute force computation. But this level of computation comes at a cost; increasing transistor density is no longer a feasible method for increasing compute power [3]. In contrast to the traditional CPU architecture relying on smaller and denser transistors, Data Flow Architecture (DFA) is a hardware design which maximizes compute potential by reducing data movement, and increasing work efficiency through highly specialized chips.

Companies like SambaNova are at the forefront of this hardware technology, creating chips which can support AI models with up to 5 trillion parameters [4]; however, in order for this impressive technology to become trending, manufacturers need to overcome a host of challenges blocking the next generation of AI fueled technology. While the aforementioned processors at SambaNova are undoubtedly powerful, the lack of software support for most data flow architectures is creating a void between what's possible, versus what's practical. Data Flow Architectures have the potential to provide

immense compute capability for the field of AI and Machine Learning; however the fledgling software ecosystem to support this architecture creates a unique challenge for its practical use, thus stifling its potential mass consumerization. More traditional computer architectures, like the Von Neumann CPU architecture and GPU architecture, have a rich software backbone making it a more pragmatic choice for many companies with products the AI/ML space. Overcoming the current nascent software landscape will be a necessary step in the future of data flow architectures for AI/ML applications.

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College of Engineering

INSERT/ACTUAL/DATE

Keyword Index

Artificial Intelligence, compute, control flow architecture, CPU, data flow design, deep learning, dynamic dataflow, GPU, machine learning, machine vision, neural networks, scheduling, tensor flow

I. SECTION 1

Companies like SambaNova are at the forefront of this hardware technology, creating chips which can support AI models with up to 5 trillion parameters [4]; however, in order for this impressive technology to become trending, manufacturers need to overcome a host of challenges blocking the next generation of AI fueled technology. While the aforementioned processors at SambaNova are undoubtedly powerful, the lack of software support for most data flow architectures is creating a void between what's possible, versus what's practical. Data Flow Architectures have the potential to provide immense compute capability for the field of AI and Machine Learning; however the fledgling software ecosystem to support this architecture creates a unique challenge for its practical use, thus stifling its potential mass consumerization. More traditional computer architectures, like the Von Neumann CPU architecture and GPU architecture, have a rich software backbone making it a more pragmatic choice for many companies with products the AI/ML space. Overcoming the current nascent software landscape will be a necessary step in the future of data flow architectures for AI/ML applications.

II. SECTION 2

Companies like SambaNova are at the forefront of this hardware technology, creating chips which can support AI models with up to 5 trillion parameters [4]; however, in order for this impressive technology to become trending, manufacturers need to overcome a host of challenges blocking the next generation of AI fueled technology. While the aforementioned processors at SambaNova are undoubtedly powerful, the lack of software support for most data flow architectures is creating a void between what's possible, versus what's practical. Data Flow Architectures have the potential to provide immense compute capability for the field of AI and Machine Learning; however the fledgling software ecosystem to support this architecture creates a unique challenge for its practical use, thus stifling its potential mass consumerization. More traditional computer architectures, like the Von Neumann CPU architecture and GPU architecture, have a rich software backbone making it a more pragmatic choice for many companies with products the AI/ML space. Overcoming the current nascent software landscape will be a necessary step in the future of data flow architectures for AI/ML applications.

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